Series 54H/74H Circuits

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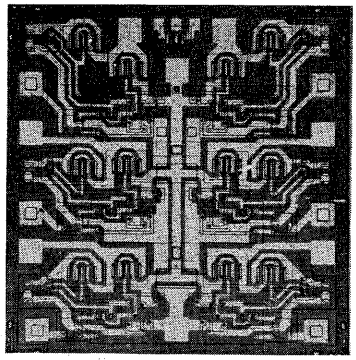
SERIES 54H, 74H
HIGH-SPEED TRANSISTOR-TRANSISTOR LOGIC

FOR GENERAL-PURPOSE DIGITAL SYSTEM APPLICATIONS

description

TYPICAL HEX INVERTER CIRCUIT BAR



Series 54H and 74H TTL integrated circuits are designed to be used in systems where very-high-speed saturated logic and high d-c noise margins are required. Definitive specifications are provided for operating characteristics over the full military temperature range (−55°C to 125°C) and the industrial temperature range (0°C to 70°C). This logic series includes the gates and flip-flop elements needed to perform all functions within general-purpose digital systems.

Series 54H and 74H are completely compatible with Series 54 and 74 TTL logic families and circuits are designed to operate at the same supply voltages, logic levels, and high d-c noise margins which are characteristic of Series 54/74 TTL circuits. Series 54H/74H circuits feature a darlington-connected, double-ended, high-speed output for improved switching speeds. Typical flip-flop clock frequencies are 30 and 50 megahertz.

Since the Series 54H/74H circuits are compatible with other products in the TTL family, these higher-speed devices may be selectively used in system locations requiring minimal propagation delay times. In other locations where speed is not critical, Series 54/74 circuits may be used, thus minimizing total system power dissipation.

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Further flexibility is provided by the addition of noninverting AND and AND-OR functions to the Series 54H/74H line. This eliminates, in so far as possible, the need for extra packages and resultant wiring to perform mere signal-inverting functions. In addition to improving speed, the low impedance of the double-ended output rejects capacitively coupled a-c pulses, ensures waveshape integrity, and provides the necessary additional drive capability.

features

LOW SYSTEM COST

- **multifunction gates and dual flip-flops offer low cost per function**
- **special circuit types (AND and AND-OR functions) reduce system package count**

OPTIMUM CIRCUIT PERFORMANCE

- **high speed — typical gate propagation delay times: 6 ns at C_L = 25 pF**
- **high d-c noise margin — typically one volt**
- **low output impedance provides low a-c noise susceptibility**
- **waveform integrity over full range of loading and temperature conditions**
- **power dissipation — typically 23 mW per NAND gate at 50% duty cycle**
- **fan-out — 10 Series 54H/74H or 54S/74S loads or 12 Series 54/74 loads**
- **compatible with standard Series 54/74 logic circuits**
- **all inputs are diode clamped to minimize transmission-line effects**
- **entirely compatible with Schottky TTL Series 54S/74S.**

SERIES 54H/74H
FEATURING 6 ns SPEED AND 22 mW PER GATE PERFORMANCE
SMALL SCALE INTEGRATION (SSI)

FUNCTION	OPERATING TEMPERATURE RANGE		PACKAGES*			SEC.-PAGE
	−55°C to 125°C	0°C to 70°C	Dual-In-Line		Flat	
NAND/NOR GATES						
Quadruple 2-Input Positive NAND Gates	SN54H00	SN74H00	J	N	W	7-5
Quadruple 2-Input Positive NAND Gates (with Open-Collector Output)	SN54H01	SN74H01	J	N	W	7-6
Hex Inverters	SN54H04	SN74H04	J	N	W	7-9
Hex Inverters (with Open-Collector Output)	SN54H05	SN74H05	J	N	W	7-10
Triple 3-Input Positive NAND Gates	SN54H10	SN74H10	J	N	W	7-11
Triple 3-Input Positive AND Gates	SN54H11	SN74H11	J	N	W	7-12
Dual 4-Input Positive NAND Gates	SN54H20	SN74H20	J	N	W	7-13
Dual 4-Input Positive AND Gates	SN54H21	SN74H21	J	N	W	7-14
Dual 4-Input Positive NAND Gates (with Open-Collector Output)	SN54H22	SN74H22	J	N	W	7-15
8-Input Positive NAND Gates	SN54H30	SN74H30	J	N	W	7-16
Dual 4-Input Positive NAND Buffers	SN54H40	SN74H40	J	N	W	7-17
AND-OR/AND-OR-INVERT GATES						
Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gates	SN54H50	SN74H50	J	N	W	7-18
Dual 2-Wide 2-Input AND-OR-INVERT Gates	SN54H51	SN74H51	J	N	W	7-18
Expandable 2-2-2-3-Input AND-OR Gates	SN54H52	SN74H52	J	N	W	7-20
Expandable 2-2-2-3-Input AND-OR-INVERT Gates	SN54H53	SN74H53	J	N	W	7-22
4-Wide 2-Input AND-OR-INVERT Gates	SN54H54	SN74H54	J	N	W	7-22
Expandable 2-Wide 4-Input AND-OR-INVERT Gates	SN54H55	SN74H55	J	N	W	7-24
EXPANDERS						
Dual 4-Input Expander	SN54H60		J	N	W	7-26
Dual 4-Input Expander		SN74H60	J	N	W	7-27
Triple 3-Input Expanders	SN54H61	SN74H61	J	N	W	7-28
3-2-2-3-Input AND-OR Expander	SN54H62		J	N	W	7-29
3-2-2-3-Input Expander		SN74H62	J	N	W	7-30

SEE PAGES 9-1, 9-2, AND 9-3 FOR LISTING OF TTL MSI CIRCUITS

*For outline drawings of all packages, see Section 1.

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

TEXAS INSTRUMENTS
INCORPORATED
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SERIES 54H/74H
FEATURING 6 ns SPEED AND 22 mW PER GATE PERFORMANCE
SMALL SCALE INTEGRATION (SSI)

FUNCTION	OPERATING TEMPERATURE RANGE		PACKAGES*			SEC.-PAGE
	–55°C to 125°C	0°C to 70°C	Dual-In-Line		Flat	
FLIP-FLOPS						
J-K Master-Slave Flip-Flops (AND-OR Inputs)	SN54H71	SN74H71	J	N	W	7-31
J-K Master-Slave Flip-Flops (AND Inputs)	SN54H72	SN74H72	J	N	W	7-34
Dual J-K Master-Slave Flip-Flops	SN54H73	SN74H73	J	N	W	7-37
Dual D-Type Edge-Triggered Flip-Flops	SN54H74	SN74H74	J	N	W	7-40
Dual J-K Master-Slave Flip-Flops with Preset and Clear	SN54H76	SN74H76	J	N	W	7-44
Dual J-K Master-Slave Flip-Flops (Common Clock)	SN54H78	SN74H78	J	N	W	7-47
J-K Negative Edge-Triggered Flip-Flops with AND-OR Inputs (50 MHz)	SN54H101	SN74H101	J	N	W	7-50
J-K Negative Edge-Triggered Flip-Flops with AND Inputs (50 MHz)	SN54H102	SN74H102	J	N	W	7-53
Dual J-K Negative Edge-Triggered Flip-Flops (50 MHz)	SN54H103	SN74H103	J	N	W	7-56
Dual J-K Negative Edge-Triggered Flip-Flops (50 MHz) with Preset and Clear	SN54H106	SN74H106	J	N	W	7-59
Dual J-K Negative Edge-Triggered Flip-Flops (50 MHz) (Common Clock)	SN54H108	SN74H108	J	N	W	7-62

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SEE PAGES 9-1, 9-2, AND 9-3 FOR LISTING OF TTL MSI CIRCUITS

*For outline drawings of all packages, see Section 1.

–SEE ORDERING INSTRUCTIONS PAGE 1-1–

absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1)	7 V
Input Voltage, V_{in} (See Notes 1 and 2)	5.5 V
Operating Free-Air Temperature Range: Series 54H	−55°C to 125°C
Series 74H	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

logic definition

Series 54H and 74H logic is defined in terms of standard POSITIVE LOGIC using the following definitions:

HIGH VOLTAGE = LOGICAL 1

LOW VOLTAGE = LOGICAL 0

unused inputs of NAND/AND gates

For optimum switching times and minimum noise susceptibility unused inputs should be maintained at a positive voltage greater than 2.4 V but not exceed the absolute maximum rating of 5.5 V. This eliminates the distributed capacitance associated with the floating input-transistor emitter, bond wire, and package lead, and ensures that no degradation will occur in the propagation delay times. Some possible ways of handling input emitters are:

a. Connect unused inputs to an independent supply voltage. Preferrably, this voltage should be between 2.4 V and 3.5 V.
b. Connect unused inputs to a used input if maximum fan-out of the driving output will not be exceeded. Each input presents a full load in the logical 1 state to the driving output.
c. Connect unused inputs to V_{CC} through a 1-kΩ resistor so that if a transient which exceeds the 5.5-V maximum rating should occur, the impedance will be high enough to protect the input. One to 25 unused inputs may be connected to each 1-kΩ resistor.

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input-current requirements

Input-current requirements reflect worst-case V_{CC} and temperature conditions. Each input, of the multiple-emitter input transistors which has a 2.8-kΩ base resistor, requires no more than a 2-mA flow out of the input at a logical 0 voltage level; therefore, one load (N = 1) is −2 mA maximum. Each input requires current into the output at a logical 1 voltage level. This current is 50 μA maximum for each emitter of input transistors with the 2.8-kΩ base resistor. Currents into the input terminals are specified as positive values.

fan-out capability

Fan-out (N) reflects the ability of an output to sink current from a number of Series 54H or 74H loads at a logical 0 voltage level and to supply current at a logical 1 voltage level. Each standard output is capable of sinking current or supplying current to 10 Series 54H or 74H loads (N = 10) or 12 Series 54 or 74 loads. Load currents (out of the output termina!) are specified as negative values.

TEXAS INSTRUMENTS
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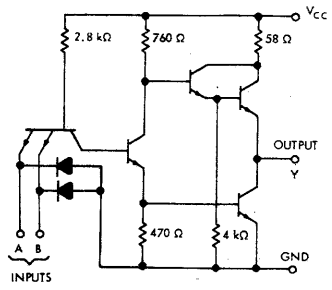
schematic (each gate)



NOTE: Component values shown are nominal

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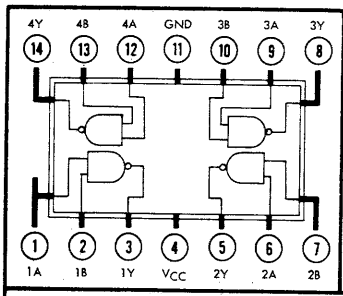
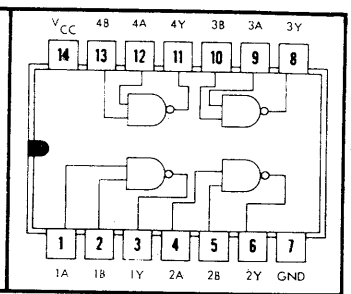
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{AB}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H00 Circuits	4.5	5	5.5	V
SN74H00 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54H00 Circuits	−55	25	125	°C
SN74H00 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

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PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP §	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1		2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2				0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −500 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 20 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.4 V			−2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{os}	Short-circuit output current‡	5	V_{CC} = MAX	−40		−100	mA
$I_{CC(0)}$	Logical 0 level supply current	6	V_{CC} = MAX, V_{in} = 4.5 V		26	40	mA
$I_{CC(1)}$	Logical 1 level supply current	6	V_{CC} = MAX, V_{in} = 0		10	16.8	mA

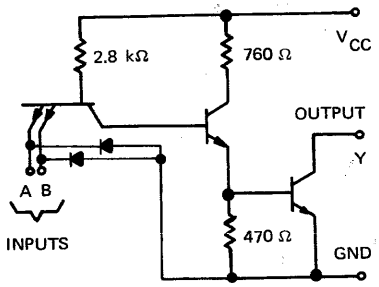
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	74	C_L = 25 pF, R_L = 280 Ω		6.2	10	ns
t_{pd1}	Propagation delay time to logical 1 level	74	C_L = 25 pF, R_L = 280 Ω		5.9	10	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

CIRCUIT TYPES SN54H01, SN74H01
QUADRUPLE 2-INPUT POSITIVE NAND GATES
(WITH OPEN-COLLECTOR OUTPUT)

schematic (each gate)



NOTE: Component values shown are nominal.

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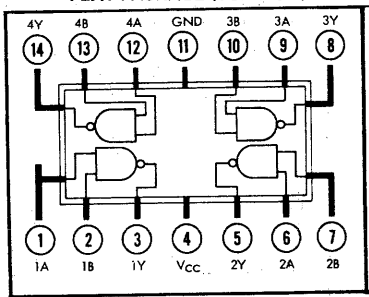
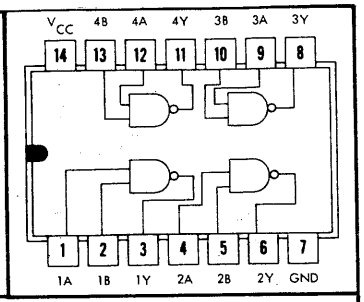
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{AB}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H01 Circuits	4.5	5	5.5	V
SN74H01 Circuits	4.75	5	5.25	V
Normalized Fan-Out from Each Output, N (and see pages 3-7 and 3-8)			10	
Operating Free-Air Temperature Range: SN54H01 Circuits	−55	25	125	°C
SN74H01 Circuits	0	25	70	°C

electrical characteristics (over operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP§	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals to ensure logical 0 (on) level at output	1		2			V
$V_{in(0)}$	Logical 0 input voltage required at either input terminal to ensure logical 1 (off) level at output	7				0.8	V
$I_{out(1)}$	Output reverse current	7	V_{CC} = MIN, V_{in} = 0.8 V, $V_{out(1)}$ = 5.5 V			250	μA
$V_{out(0)}$	Logical 0 output voltage (on level)	1	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 20 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.4 V			−2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{CC(0)}$	Logical 0 level supply current	6	V_{CC} = MAX, V_{in} = 4.5 V		26	40	mA
$I_{CC(1)}$	Logical 1 level supply current	6	V_{CC} = MAX, V_{in} = 0		6.8	10	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	74	C_L = 25 pF, R_L = 280 Ω		7.5	12	ns
t_{pd1}	Propagation delay time to logical 1 level	74	C_L = 25 pF, R_L = 280 Ω		10	15	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

APPLICATION DATA

combined fan-out and wire-AND capabilities

The open-collector TTL gate, when supplied with a proper load resistor (R_L), may be paralleled with other similar TTL gates to perform the wire-AND function and simultaneously, will drive from one to nine 54H or 74H loads. When no other open-collector gates are paralleled, this gate may be used to drive ten 54H or 74H loads. For any of these conditions an appropriate load-resistor value must be determined for the desired circuit configuration. A maximum resistor value must be determined which will ensure that sufficient load current (to loads) and I_{off} current (through paralleled outputs) will be available during a logical 1 level at the output. A minimum resistor value must be determined which will ensure that current through this resistor and sink current from the loads will not cause the output voltage to rise above the logical 0 level even if one of the paralleled outputs is sinking all the current.

In both conditions (logical 0 and logical 1) the value of R_L is determined by:

$$R_L = \frac{V_{RL}}{I_{RL}}$$

where: V_{RL} is voltage drop in volts, and I_{RL} is the current in amperes.

logical 1 (off level) circuit calculations (see figure A)

The allowable voltage drop across the load resistor (V_{RL}) is the difference between V_{CC} applied and the $V_{out(1)}$ level required at the load:

$$V_{RL} = V_{CC} - V_{out(1)\ \text{required}}$$

The total current through the load resistor (I_{RL}) is the sum of the load currents ($I_{in(1)}$) and off-level reverse currents ($I_{out(1)}$) through each of the wire-AND connected outputs:

$$I_{RL} = \eta \cdot I_{out(1)} + N \cdot I_{in(1)} \text{ to loads}$$

Therefore, calculations for the maximum value of R_L would be:

$$R_{L(max)} = \frac{V_{CC} - V_{out(1)\ \text{required}}}{\eta \cdot I_{out(1)} + N \cdot I_{in(1)}}$$

where: η = number of gates wire-AND connected, and N = number of 54H/74H loads

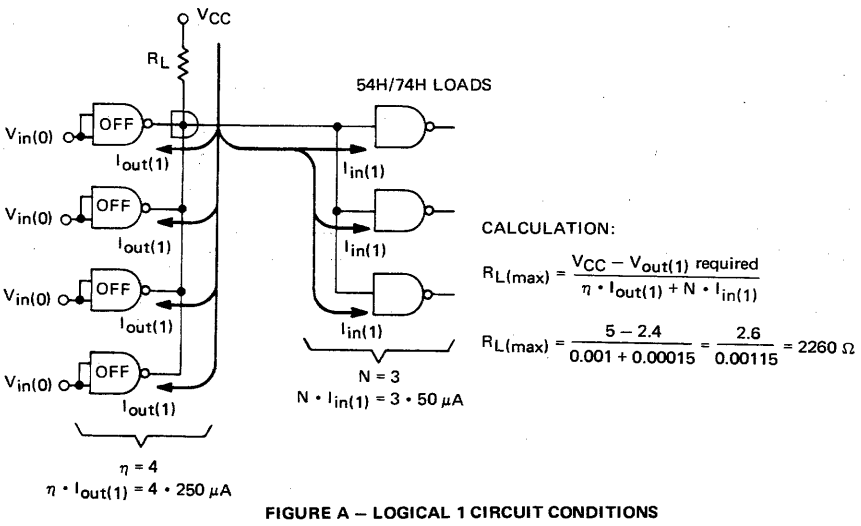


FIGURE A – LOGICAL 1 CIRCUIT CONDITIONS

APPLICATION DATA

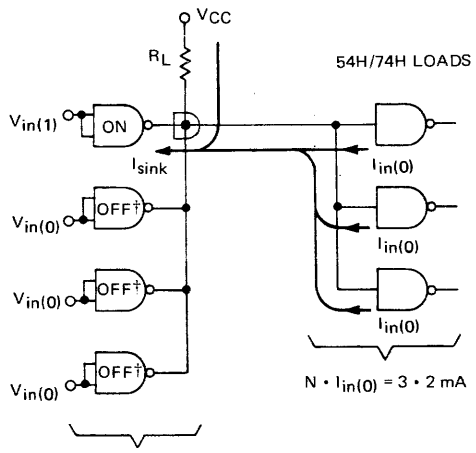
logical 0 (on level) circuit calculations (see figure B)

The current through the resistor must be limited to the maximum sink-current capability of one output transistor. Note that if several output transistors are wire-AND connected, the current through R_L may be shared by those paralleled transistors. However, unless it can be absolutely guaranteed that more than one transistor will be on during logical 0 periods, the current must be limited to 20 mA, the maximum current which will ensure a logical 0 maximum of 0.4 volts.

Also, fan-out must be considered. Part of the 20 mA will be supplied from the inputs which are being driven. This reduces the amount of current which can be allowed through R_L.

Therefore, the equation used to determine the minimum value of R_L would be:

$$R_{L(min)} = \frac{V_{CC} - V_{out(0)\ required}}{I_{sink\ capability} - I_{sink\ from\ loads}}$$



CALCULATION:

$$R_{L(min)} = \frac{V_{CC} - V_{out(0)\ required}}{I_{sink\ capability} - I_{sink\ from\ TTL\ loads}}$$

$$R_{L(min)} = \frac{5 - 0.4}{0.02 - 0.006} = \frac{4.6}{0.014} = 323\ \Omega$$

†Current into OFF outputs is negligible at logical 0.

FIGURE B – LOGICAL 0 CIRCUIT CONDITIONS

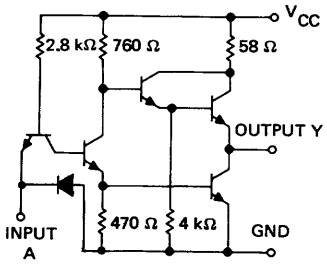
Table I provides minimum and maximum resistor values, calculated from equations shown above,for driving one to ten 54H/74H loads and wire-AND connecting two to seven parallel output. Each value shown for one wire-AND output is determined by the fan-out plus the cutoff current of a single output transistor. Extension beyond seven wire-AND connections is permitted with fan-outs of seven or less if a valid minimum and maximum R_L is possible. Fastest rise times are obtained when $R_{L(min)}$ is used. When fanning-out to ten 54H/74H loads, the calculation for the minimum value of R_L indicates that and infinite resistance should be used ($V_{R_L} \div 0 = \infty$); however, the use of a 3466 Ω resistor in this case will satisfy the logical 1 condition and limit the logical 0 voltage level to less than 0.42 V.

FAN-OUT TO 54H/74H LOADS	WIRE-AND OUTPUTS							
	1	2	3	4	5	6	7	1 to 7
1	8666	4727	3250	2476	2000	1677	1444	255
2	7428	4333	3058	2363	1925	1625	1405	288
3	6500	4000	2888	2260	1857	1575	1368	323
4	5777	3714	2736	2166	1793	1529	1333	384
5	5200	3466	2600	2080	1733	1485	1300	460
6	4727	3250	2476	2000	1677	1444	1268	578
7	4333	3058	2363	1925	1625	1405	1238	767
8	4000	2888	2260	1857	1575	1368	1209	1150
9	3714	2736	X	X	X	X	X	2300
10	3466	X	X	X	X	X	X	3466‡
	MAXIMUM							MIN
	LOAD RESISTOR VALUE IN OHMS							

TABLE I – LOAD RESISTOR VALUES

X – Not recommended or not possible.
‡ – The theoretical value is ∞. See explanation in text.
All values shown in the table are based on:
Logical 1 conditions: V_{CC} = 5 V, $V_{out(1)}$ required = 2.4 V
Logical 0 conditions: V_{CC} = 5 V, $V_{out(0)}$ required = 0.4 V

schematic (each inverter)



Component values shown are normal

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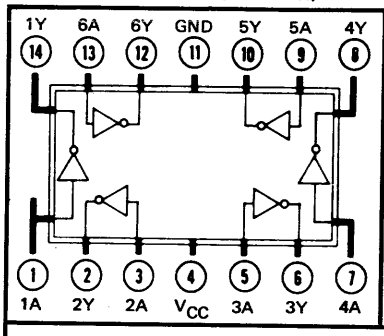
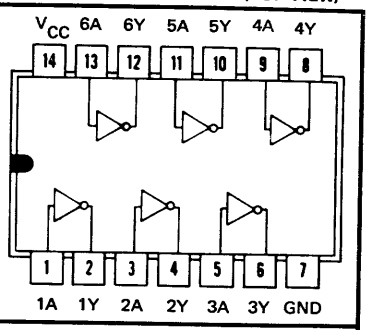
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{A}$

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	SN54H04 Circuits	4.5	5	5.5	V
	SN74H04 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N				10	
Operating Free-Air Temperature Range, T_A:	SN54H04 Circuits	−55	25	125	°C
	SN74H04 Circuits	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP§	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at input terminal to ensure logical 0 level at output	8		2			V
$V_{in(0)}$	Logical 0 input voltage required at input terminal to ensure logical 1 level at output	9				0.8	V
$V_{out(1)}$	Logical 1 output voltage	9	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −500 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	8	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 20 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current	11	V_{CC} = MAX, V_{in} = 0.4 V			−2	mA
$I_{in(1)}$	Logical 1 level input current	11	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current‡	12	V_{CC} = MAX	−40		−100	mA
$I_{CC(0)}$	Logical 0 level supply current	13	V_{CC} = MAX, V_{in} = 4.5 V		40	58	mA
$I_{CC(1)}$	Logical 1 level supply current	13	V_{CC} = MAX, V_{in} = 0		16	26	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	74	C_L = 25 pF, R_L = 280 Ω		6.5	10	ns
t_{pd1}	Propagation delay time to logical 1 level	74	C_L = 25 pF, R_L = 280 Ω		6	10	ns

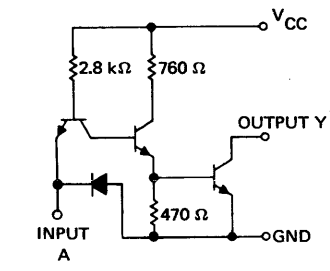
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

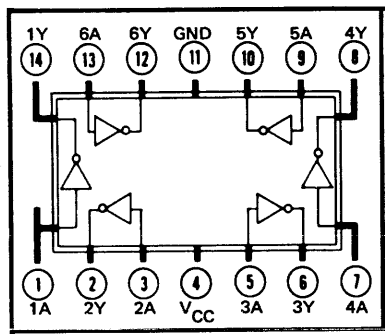
CIRCUIT TYPES SN54H05, SN74H05
HEX INVERTERS (WITH OPEN-COLLECTOR OUTPUT)

schematic (each inverter)

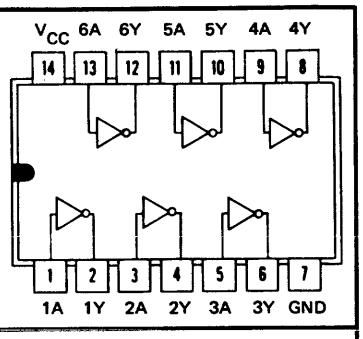


Component values shown are normal

W
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{A}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H05 Circuits	4.5	5	5.5	V
SN74H05 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N (and see pages 3-7 and 3-8)	−55	25	125	°C
Operating Free-Air Temperature Range, T_A: SN54H05 Circuits	0	25	70	°C
SN74H05 Circuits			10	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP§	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at input terminal to ensure logical 0 (on) level at output	8		2			V
$V_{in(0)}$	Logical 0 input voltage required at input terminal to ensure logical 1 (off) level at output	10				0.8	V
$I_{out(1)}$	Output reverse current	10	V_{CC} = MIN, V_{in} = 0.8 V, $V_{out(1)}$ = 5.5 V			250	μA
$V_{out(0)}$	Logical 0 output voltage (on level)	8	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 20 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current	11	V_{CC} = MAX, V_{in} = 0.4 V			−2	mA
$I_{in(1)}$	Logical 1 level input current	11	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{CC(0)}$	Logical 0 level supply current	13	V_{CC} = MAX, V_{in} = 4.5 V		40	58	mA
$I_{CC(1)}$	Logical 1 level supply current	13	V_{CC} = MAX, V_{in} = 0		16	26	mA

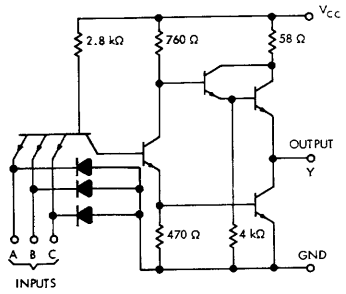
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	74	C_L = 25 pF, R_L = 280 Ω		7.5	12	ns
t_{pd1}	Propagation delay time to logical 1 level	74	C_L = 25 pF, R_L = 280 Ω		10	15	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

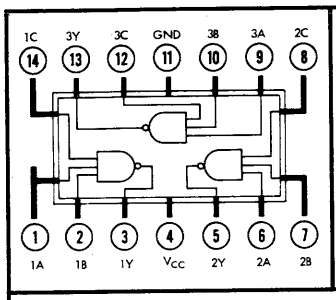
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

schematic (each gate)

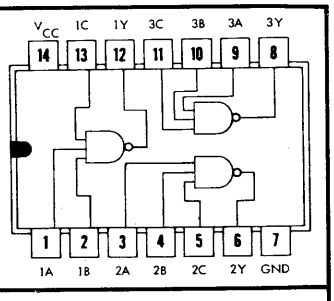


NOTE: Component values shown are nominal

W
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{ABC}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H10 Circuits	4.5	5	5.5	V
SN74H10 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54H10 Circuits	−55	25	125	°C
SN74H10 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP §	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1		2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2				0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −500 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 20 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.4 V			−2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{os}	Short-circuit output current‡	5	V_{CC} = MAX	−40		−100	mA
$I_{CC(0)}$	Logical 0 level supply current	6	V_{CC} = MAX, V_{in} = 4.5 V		19.5	30	mA
$I_{CC(1)}$	Logical 1 level supply current	6	V_{CC} = MAX, V_{in} = 0		7.5	12.6	mA

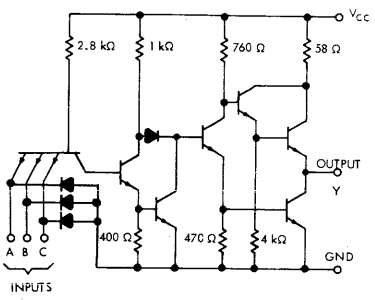
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	74	C_L = 25 pF, R_L = 280 Ω		6.3	10	ns
t_{pd1}	Propagation delay time to logical 1 level	74	C_L = 25 pF, R_L = 280 Ω		5.9	10	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

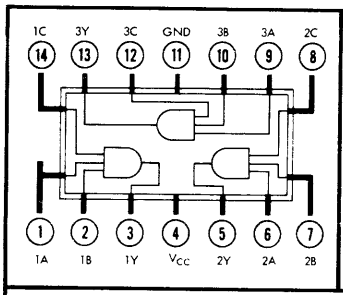
CIRCUIT TYPES SN54H11, SN74H11
TRIPLE 3-INPUT POSITIVE AND GATES

schematic (each gate)

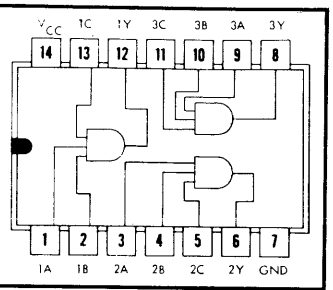


NOTE: Component values shown are nominal

W
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = ABC$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H11 Circuits	4.5	5	5.5	V
SN74H11 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54H11 Circuits	−55	25	125	°C
SN74H11 Circuits	0	25	70	°C

7

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP §	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 1 level at output	14		2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 0 level at output	15				0.8	V
$V_{out(1)}$	Logical 1 output voltage	14	V_{CC} = MIN, $V_{in(1)}$ = 2 V, I_{load} = −500 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	15	V_{CC} = MIN, $V_{in(0)}$ = 0.8 V, I_{sink} = 20 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	16	V_{CC} = MAX, V_{in} = 0.4 V			−2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	17	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current‡	18	V_{CC} = MAX, V_{in} = 4.5 V	−40		−100	mA
$I_{CC(0)}$	Logical 0 level supply current	19	V_{CC} = MAX, V_{in} = 0		30	48	mA
$I_{CC(1)}$	Logical 1 level supply current	19	V_{CC} = MAX, V_{in} = 4.5 V		18	30	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

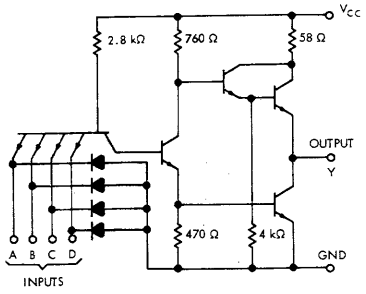
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	74	C_L = 25 pF, R_L = 280 Ω		8.8	12	ns
t_{pd1}	Propagation delay time to logical 1 level	74	C_L = 25 pF, R_L = 280 Ω		7.6	12	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

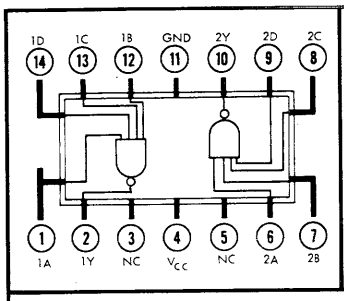
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

schematic (each gate)

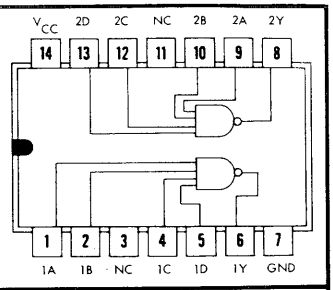


NOTES: 1. Component values shown are nominal
2. NC — No internal connection

W
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{ABCD}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H20 Circuits	4.5	5	5.5	V
SN74H20 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54H20 Circuits	−55	25	125	°C
SN74H20 Circuits	0	25	70	°C

7

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP§	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 output voltage	1		2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2				0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −500 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 20 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.4 V			−2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current‡	5	V_{CC} = MAX	−40		−100	mA
$I_{CC(0)}$	Logical 0 level supply current	6	V_{CC} = MAX, V_{in} = 4.5 V		13	20	mA
$I_{CC(1)}$	Logical 1 level supply current	6	V_{CC} = MAX, V_{in} = 0		5	8.4	mA

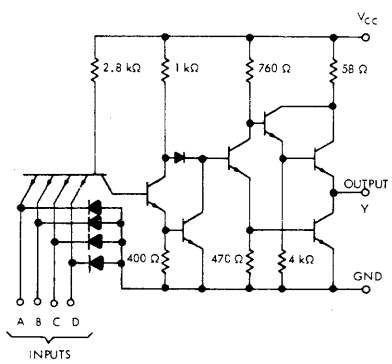
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	74	C_L = 25 pF, R_L = 280 Ω		7	10	ns
t_{pd1}	Propagation delay time to logical 1 level	74	C_L = 25 pF, R_L = 280 Ω		6	10	ns

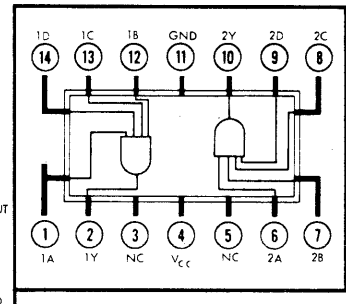
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.
§All typical values are at V_{CC} = 5 V, T_A = 25°C.

CIRCUIT TYPES SN54H21, SN74H21
DUAL 4-INPUT POSITIVE AND GATES

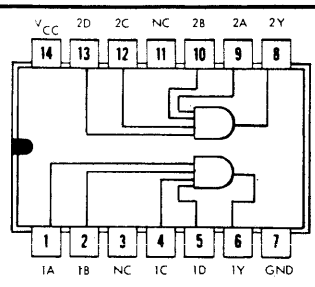
schematic (each gate)



W
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: Y = ABCD

NOTES: 1. Component values shown are nominal
2. NC — No internal connection

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H21 Circuits	4.5	5	5.5	V
SN74H21 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54H21 Circuits	−55	25	125	°C
SN74H21 Circuits	0	25	70	°C

7

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP §	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 1 level at output	14		2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 0 level at output	15				0.8	V
$V_{out(1)}$	Logical 1 output voltage	14	V_{CC} = MIN, $V_{in(1)}$ = 2 V, I_{load} = −500 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	15	V_{CC} = MIN, $V_{in(0)}$ = 0.8 V, I_{sink} = 20 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	16	V_{CC} = MAX, V_{in} = 0.4 V			−2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	17	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current‡	18	V_{CC} = MAX, V_{in} = 4.5 V	−40		−100	mA
$I_{CC(0)}$	Logical 0 level supply current	19	V_{CC} = MAX, V_{in} = 0		20	32	mA
$I_{CC(1)}$	Logical 1 level supply current	19	V_{CC} = MAX, V_{in} = 4.5 V		12	20	mA

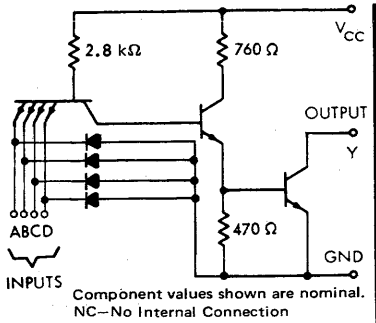
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	74	C_L = 25 pF, R_L = 280 Ω		8.8	12	ns
t_{pd1}	Propagation delay time to logical 1 level	74	C_L = 25 pF, R_L = 280 Ω		7.6	12	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

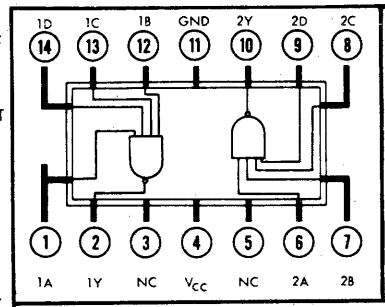
CIRCUIT TYPES SN54H22, SN74H22
DUAL 4-INPUT POSITIVE NAND GATES (WITH OPEN-COLLECTOR OUTPUT)

schematic (each gate)

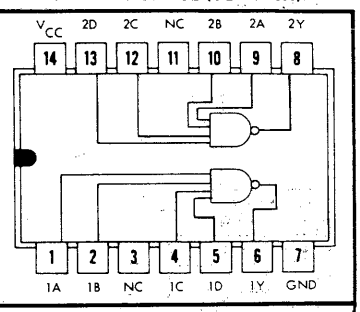


Component values shown are nominal.
NC—No Internal Connection

W
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-PACKAGE (TOP VIEW)



positive logic: $Y = \overline{ABCD}$

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	SN54H22 Circuits	4.5	5	5.5	V
	SN74H22 Circuits	4.75	5	5.25	V
Normalized Fan-Out from Each Output, N (and see pages 3-7 and 3-8)				10	
Operating Free-Air Temperature Range:	SN54H22 Circuits	−55	25	125	°C
	SN74H22 Circuits	0	25	70	°C

electrical characteristics (over operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP§	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 (on) level at output	1		2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 (off) level at output	7				0.8	V
$I_{out(1)}$	Output reverse current	7	V_{CC} = MIN, V_{in} = 0.8 V, $V_{out(1)}$ = 5.5 V			250	μA
$V_{out(0)}$	Logical 0 output voltage (on level)	1	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 20 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.4 V			−2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{CC(0)}$	Logical 0 level supply current	6	V_{CC} = MAX, V_{in} = 4.5 V		13	20	mA
$I_{CC(1)}$	Logical 1 level supply current	6	V_{CC} = MAX, V_{in} = 0		3.4	5	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

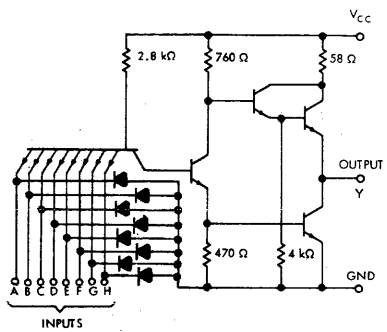
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	74	C_L = 25 pF, R_L = 280 Ω		7.5	12	ns
t_{pd1}	Propagation delay time to logical 1 level	74	C_L = 25 pF, R_L = 280 Ω		10	15	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

For Applications Data, see pages 3-7 and 3-8.

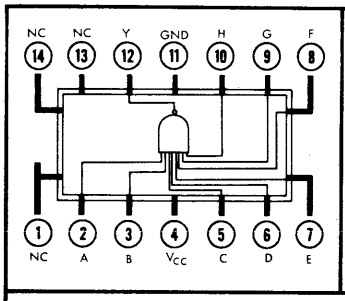
CIRCUIT TYPES SN54H30, SN74H30
8-INPUT POSITIVE NAND GATES

schematic

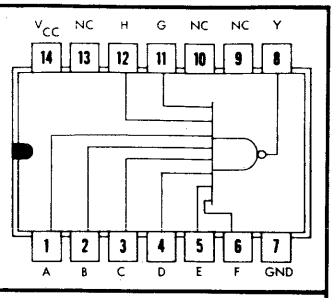


NOTES: 1. Component values shown are nominal
2. NC — No internal connection

W
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{ABCDEFGH}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H30 Circuits	4.5	5	5.5	V
SN74H30 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54H30 Circuits	−55	25	125	°C
SN74H30 Circuits	0	25	70	°C

7

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP §	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1		2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2				0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −500 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 20 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.4 V			−2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{os}	Short-circuit output current‡	5	V_{CC} = MAX	−40		−100	mA
$I_{CC(0)}$	Logical 0 level supply current	6	V_{CC} = MAX, V_{in} = 4.5 V		6.5	10	mA
$I_{CC(1)}$	Logical 1 level supply current	6	V_{CC} = MAX, V_{in} = 0		2.5	4.2	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

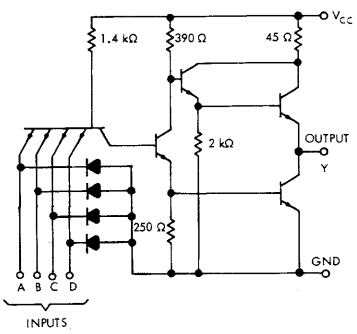
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	74	C_L = 25 pF, R_L = 280 Ω		8.9	12	ns
t_{pd1}	Propagation delay time to logical 1 level	74	C_L = 25 pF, R_L = 280 Ω		6.8	10	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡Duration of short-circuit test should not exceed 1 second.

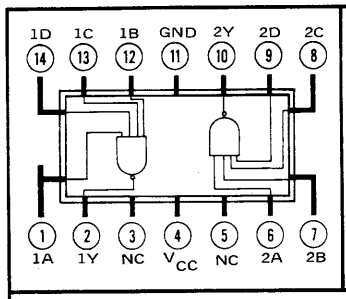
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

schematic (each gate)

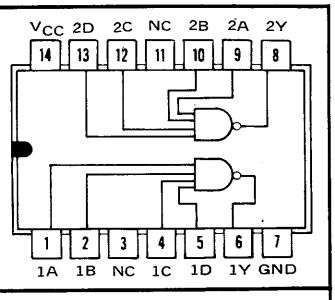


NOTES: 1. Component values shown are nominal
2. NC — No internal connection

W
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{ABCD}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H40 Circuits	4.5	5	5.5	V
SN74H40 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			30	
Operating Free-Air Temperature Range, T_A: SN54H40 Circuits	−55	25	125	°C
SN74H40 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP §	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1		2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2				0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −1.5 mA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 60 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.4 V			−4	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX, V_{in} = 2.4 V			100	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current‡	5	V_{CC} = MAX	−40		−125	mA
$I_{CC(0)}$	Logical 0 level supply current	6	V_{CC} = MAX, V_{in} = 4.5 V		25	40	mA
$I_{CC(1)}$	Logical 1 level supply current	6	V_{CC} = MAX, V_{in} = 0		10.4	16	mA

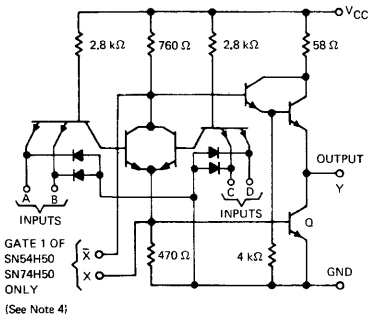
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 30

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	74	C_L = 25 pF, R_L = 93 Ω		6.5	12	ns
t_{pd1}	Propagation delay time to logical 1 level	74	C_L = 25 pF, R_L = 93 Ω		8.5	12	ns

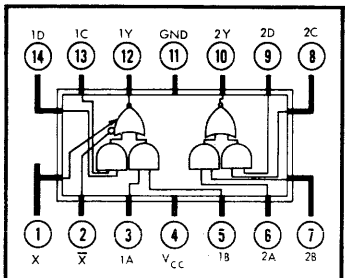
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.
§All typical values are at V_{CC} = 5 V, T_A = 25°C.

CIRCUIT TYPES SN54H50, SN54H51, SN74H50, SN74H51
DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATES

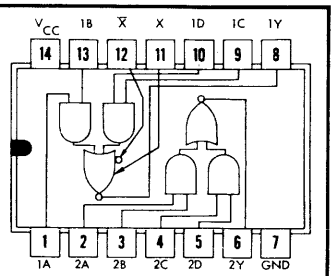
schematic (each gate)



W
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{(AB) + (CD) + (X)}$
(X = Output of SN54H60/SN74H60 or SN54H62/SN74H62)

NOTES: 1. Component values are nominal.
2. Both expander inputs are used simultaneously for expanding.
3. If expander is not used leave X and $\overline{X}$ pins open.
4. Expander inputs X and $\overline{X}$ are functional on the SN54H50 and SN75H50 circuits only. Make no external connection to X and $\overline{X}$ pins of the SN54H51 and SN74H51.
5. A total of four SN54H60/SN74H60 expander gates or one SN54H62/SN74H62 expander gate may be connected to the expander inputs.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H50, SN54H51 Circuits	4.5	5	5.5	V
SN74H50, SN74H51 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54H50, SN54H51 Circuits	−55	25	125	°C
SN74H50, SN74H51 Circuits	0	25	70	°C

7

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP§	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals of either AND section to ensure logical 0 at output	20		2			V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 at output	21				0.8	V
$V_{out(1)}$	Logical 1 output voltage	21	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −500 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	20	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 20 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	22	V_{CC} = MAX, V_{in} = 0.4 V			−2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	23	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{os}	Short-circuit output current‡	24	V_{CC} = MAX	−40		−100	mA
$I_{CC(0)}$	Logical 0 level supply current	25	V_{CC} = MAX, V_{in} = 4.5 V		15.2	24	mA
$I_{CC(1)}$	Logical 1 level supply current	26	V_{CC} = MAX, V_{in} = 0		8.2	12.8	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type. Expander pins are open.

‡Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

electrical characteristics (SN54H50 circuits only) using expander inputs, V_{CC} = 4.5 V, T_A = −55°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{in\overline{X}}$	Expander-node input current	27	$V_{\overline{X}}$ = 1.4 V			−5.85	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor Q	28	I_{sink} = 20 mA, I_1 = 700 μA, R_1 = 0			1	V
$V_{out(1)}$	Logical 1 output voltage	29	I_{load} = −500 μA, I_1 = 320 μA, I_2 = −320 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	28	I_{sink} = 20 mA, I_1 = 470 μA, R_1 = 68 Ω			0.4	V

electrical characteristics (SN74H50 circuits only) using expander inputs, V_{CC} = 4.75 V, T_A = 0°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{in\overline{X}}$	Expander-node input current	27	$V_{\overline{X}}$ = 1.4 V			−6.3	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor Q	28	I_{sink} = 20 mA, I_1 = 1.1 mA, R_1 = 0			1	V
$V_{out(1)}$	Logical 1 output voltage	29	I_{load} = −500 μA, I_1 = 570 μA, I_2 = −570 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	28	I_{sink} = 20 mA, I_1 = 600 μA, R_1 = 63 Ω			0.4	V

7

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10, expander pins are open

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	74	C_L = 25 pF, R_L = 280 Ω		6.2	11	ns
t_{pd1}	Propagation delay time to logical 1 level	74	C_L = 25 pF, R_L = 280 Ω		6.8	11	ns

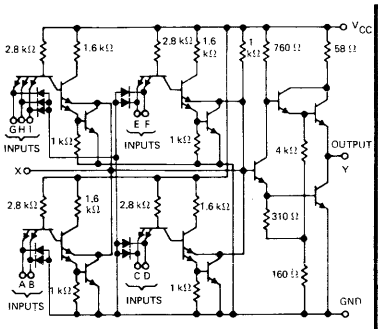
switching characteristics, (SN54H50/SN74H50 circuits only), V_{CC} = 5 V, T_A = 25°C, N = 10, $C_{\overline{X}}$ = 15 pF¶

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	75	C_L = 25 pF, R_L = 280 Ω		7.4		ns
t_{pd1}	Propagation delay time to logical 1 level	75	C_L = 25 pF, R_L = 280 Ω		11		ns

¶See curves on page 7-90 for effect of other values of $C_{\overline{X}}$.

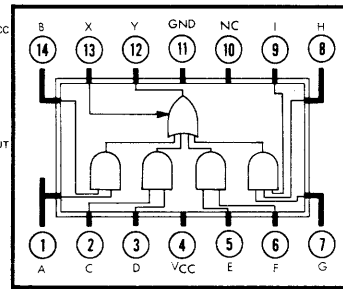
CIRCUIT TYPES SN54H52, SN74H52
EXPANDABLE 2-2-2-3-INPUT AND-OR GATES

schematic



NOTES: 1. Component values shown are nominal.
2. A total of six expander gates may be connected to the expander input X.
3. NC — No internal connection.

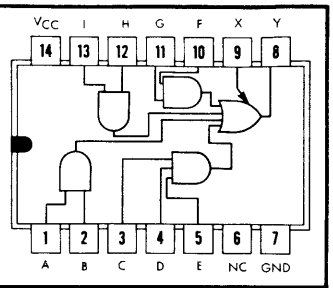
W
FLAT PACKAGE (TOP VIEW)



positive logic:

$Y = (AB) + (CD) + (EF) + (GHI) + (X)$
(X = Output of SN54H61/SN74H61)

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic:

$Y = (AB) + (CDE) + (FG) + (HI) + (X)$
(X = Output of SN54H61/SN74H61)

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H52 Circuits	4.5	5	5.5	V
SN74H52 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54H52 Circuits	−55	25	125	°C
SN74H52 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP§	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals of one AND section to ensure logical 1 at output	30		2			V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 0 at output	31				0.8	V
$V_{out(1)}$	Logical 1 output voltage	30	V_{CC} = MIN, V_{in} = 2 V, I_{load} = −500 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	31	V_{CC} = MIN, V_{in} = 0.8 V, I_{sink} = 20 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	32	V_{CC} = MAX, V_{in} = 0.4 V			−2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	33	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{os}	Short-circuit output current‡	34	V_{CC} = MAX, V_{in} = 4.5 V	−40		−100	mA
$I_{CC(0)}$	Logical 0 level supply current	35	V_{CC} = MAX, V_{in} = 0		15.2	24	mA
$I_{CC(1)}$	Logical 1 level supply current	35	V_{CC} = MAX, V_{in} = 4.5 V		20	31	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type. Expander pin is open.
‡Duration of short-circuit test should not exceed 1 second.
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

electrical characteristics (SN54H52 circuits only) using expander input, V_{CC} = 4.5 V

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{inX}	Expander-node input current	36	V_X = 1 V, I_{load} = −500 μA, T_A = −55°C	−2.7		−4.5	mA
$V_{out(1)}$	Logical 1 output voltage	36	V_X = 1 V, I_{load} = −500 μA, T_A = −55°C	2.4			V
$V_{out(0)}$	Logical 0 output voltage	37	I_{inX} = −300 μA, I_{sink} = 20 mA, T_A = 125°C			0.4	V

electrical characteristics (SN74H52 circuits only) using expander input, V_{CC} = 4.75 V

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{inX}	Expander-node input current	36	V_X = 1 V, I_{load} = −500 μA, T_A = 0°C	−2.9		−5.35	mA
$V_{out(1)}$	Logical 1 output voltage	36	V_X = 1 V, I_{load} = −500 μA, T_A = 0°C	2.4			V
$V_{out(0)}$	Logical 0 output voltage	37	I_{inX} = −300 μA, I_{sink} = 20 mA, T_A = 70°C			0.4	V

7

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10, expander pin is open

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	74	C_L = 25 pF, R_L = 280 Ω		9.2	15	ns
t_{pd1}	Propagation delay time to logical 1 level	74	C_L = 25 pF, R_L = 280 Ω		10.6	15	ns

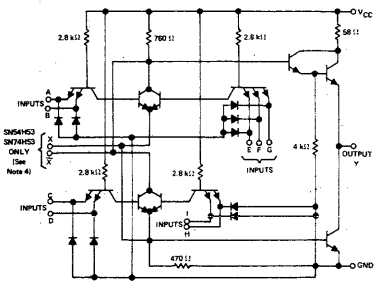
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10, C_X = 15 pF¶

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	76	C_L = 25 pF, R_L = 280 Ω		9.8		ns
t_{pd1}	Propagation delay time to logical 1 level	76	C_L = 25 pF, R_L = 280 Ω		14.8		ns

¶See curves on page 7-90 for effect of other values of C_X.

CIRCUIT TYPES SN54H53, SN54H54, SN74H53, SN74H54
EXPANDABLE 2-2-2-3-INPUT AND-OR-INVERT GATES

schematic



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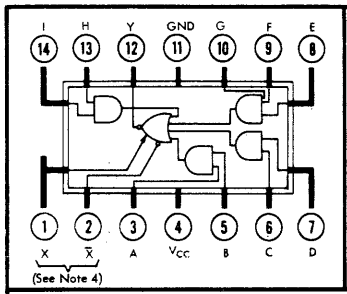
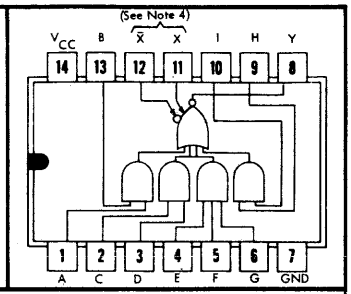
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{(AB) + (CD) + (EFG) + (HI) + (X)}$
(X = Output of SN54H60/SN74H60 or SN54H62/SN74H62)

NOTES: 1. Component values shown are nominal.
2. Both expander inputs are used simultaneously for expanding.
3. If expander is not used leave X and $\overline{X}$ pins open.
4. Expander inputs X and $\overline{X}$ are functional on the SN54H53 and SN74H53 circuits only. Make no external connection to X and $\overline{X}$ pins of the SN54H54 and SN74H54.
5. A total of four SN54H60/SN74H60 expander gates or one SN54H62/SN74H62 expander gate may be connected to the expander inputs.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H53, SN54H54 Circuits	4.5	5	5.5	V
SN74H53, SN74H54 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54H53, SN54H54 Circuits	−55	25	125	°C
SN74H53, SN74H54 Circuits	0	25	70	°C

7

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP §	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals of one AND section to ensure logical 0 at output	20		2			V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 at output	21				0.8	V
$V_{out(1)}$	Logical 1 output voltage	21	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −500 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	20	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 20 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	22	V_{CC} = MAX, V_{in} = 0.4 V			−2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	23	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{os}	Short-circuit output current‡	24	V_{CC} = MAX	−40		−100	mA
$I_{CC(0)}$	Logical 0 level supply current	25	V_{CC} = MAX V_{in} = 4.5 V		9.4	14	mA
$I_{CC(1)}$	Logical 1 level supply current	26	V_{CC} = MAX, V_{in} = 0		7.1	11	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type. Expander pins are open.
‡Duration of short-circuit test should not exceed 1 second.
§All typical values are at V_{CC} = 5 V, T_A = 25°C.

electrical characteristics (SN54H53 circuits only) using expander inputs, V_{CC} = 4.5 V, T_A = −55° C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{in\,\bar{x}}$	Expander-node input current	27	$V_{\bar{x}}$ = 1.4 V			−5.85	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor Q	28	I_{sink} = 20 mA, I_1 = 700 μA, R_1 = 0			1	V
$V_{out(1)}$	Logical 1 output voltage	29	I_{load} = −500 μA, I_1 = 320 μA, I_2 = −320 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	28	I_{sink} = 20 mA, I_1 = 470 μA, R_1 = 68 Ω			0.4	V

electrical characteristics (SN74H53 circuits only) using expander inputs, V_{CC} = 4.75 V, T_A = 0° C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{in\,\bar{x}}$	Expander-node input current	27	$V_{\bar{x}}$ = 1.4 V			−6.3	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor Q	28	I_{sink} = 20 mA, I_1 = 1.1 mA, R_1 = 0			1	V
$V_{out(1)}$	Logical 1 output voltage	29	I_{load} = −500 μA, I_1 = 570 μA, I_2 = −570 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	28	I_{sink} = 20 mA, I_1 = 600 μA, R_1 = 63 Ω			0.4	V

7

switching characteristics, V_{CC} = 5 V, T_A = 25° C, N = 10 , expander pins are open

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	74	C_L = 25 pF, R_L = 280 Ω		6.2	11	ns
t_{pd1}	Propagation delay time to logical 1 level	74	C_L = 25 pF, R_L = 280 Ω		7	11	ns

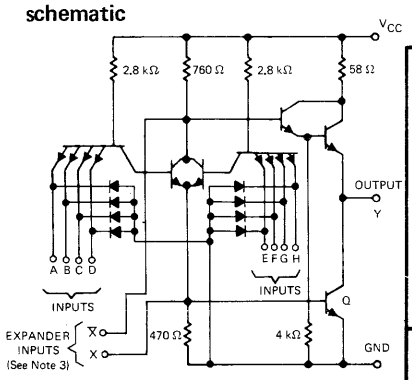
switching characteristics, (SN54H53/SN74H53 circuits only) V_{CC} = 5 V, T_A = 25°C, N = 10, $C_{\bar{x}}$ = 15 pF¶

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	75	C_L = 25 pF, R_L = 280 Ω		7.4		ns
t_{pd1}	Propagation delay time to logical 1 level	75	C_L = 25 pF, R_L = 280 Ω		11.4		ns

¶See curves on page 7-90 for effect of other values of $C_{\bar{x}}$.

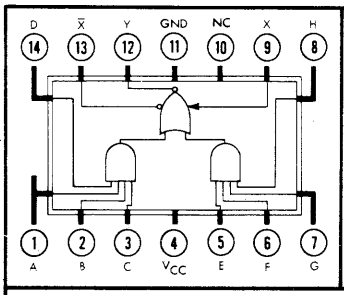
CIRCUIT TYPES SN54H55, SN74H55
EXPANDABLE 4-INPUT AND-OR-INVERT GATES

schematic

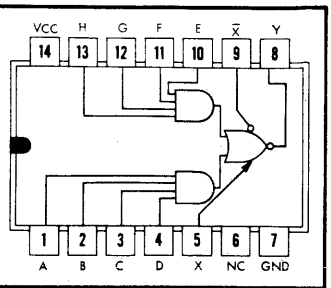


NOTES: 1. Component values shown are nominal.
2. Both expander inputs are used simultaneously for expanding.
3. If expander is not used, leave X and $\overline{X}$ pins open.
4. A total of four SN54H60/SN74H60 expander gates or one SN54H62/SN74H62 expander gate may be connected to the expander inputs.
5. NC — No internal connection.

W
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{(ABCD) + (EFGH) + (X)}$
X = Output of SN54H60/SN74H60 or SN54H62/SN74H62 circuit.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H55 Circuits	4.5	5	5.5	V
SN74H55 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54H55 Circuits	−55	25	125	°C
SN74H55 Circuits	0	25	70	°C

7

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP§	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals of either AND section to ensure logical 0 at output	20		2			V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 at output	21				0.8	V
$V_{out(1)}$	Logical 1 output voltage	21	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −500 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	20	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 20 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	22	V_{CC} = MAX, V_{in} = 0.4 V			−2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	23	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{os}	Short-circuit output current‡	24	V_{CC} = MAX	−40		−100	mA
$I_{CC(0)}$	Logical 0 level supply current	25	V_{CC} = MAX, V_{in} = 4.5 V		7.5	12	mA
$I_{CC(1)}$	Logical 1 level supply current	26	V_{CC} = MAX, V_{in} = 0		4.5	6.4	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type. Expander pins are open.
‡Duration of short-circuit test should not exceed 1 second.
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

electrical characteristics (SN54H55 circuits only) using expander inputs, V_{CC} = 4.5 V, T_A = –55°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{in\bar{x}}$	Expander-node input current	27	$V_{\bar{x}}$ = 1.4 V			–5.85	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor Q	28	I_{sink} = 20 mA, I_1 = 700 μA, R_1 = 0			1	V
$V_{out(1)}$	Logical 1 output voltage	29	I_{load} = –500 μA, I_1 = 320 μA, I_2 = –320 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	28	I_{sink} = 20 mA, I_1 = 470 μA, R_1 = 68 Ω			0.4	V

electrical characteristics (SN74H55 circuits only) using expander inputs, V_{CC} = 4.75 V, T_A = 0°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{in\bar{x}}$	Expander-node input current	27	$V_{\bar{x}}$ = 1.4 V			–6.3	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor Q	28	I_{sink} = 20 mA, I_1 = 1.1 mA, R_1 = 0			1	V
$V_{out(1)}$	Logical 1 output voltage	29	I_{load} = –500 μA, I_1 = 570 μA, I_2 = –570 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	28	I_{sink} = 20 mA, I_1 = 600 μA, R_1 = 63 Ω			0.4	V

7

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10, expander pins are open

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	74	C_L = 25 pF, R_L = 280 Ω		6.5	11	ns
t_{pd1}	Propagation delay time to logical 1 level	74	C_L = 25 pF, R_L = 280 Ω		7	11	ns

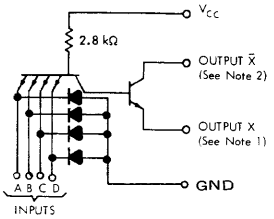
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10, $C_{\bar{x}}$ = 15 pF¶

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	75	C_L = 25 pF, R_L = 280 Ω		7.7		ns
t_{pd1}	Propagation delay time to logical 1 level	75	C_L = 25 pF, R_L = 280 Ω		11.4		ns

¶ See curves on page 7-90 for effect of other values of $C_{\bar{x}}$.

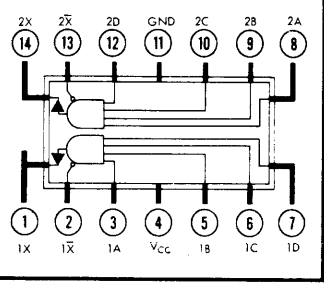
CIRCUIT TYPE SN54H60
DUAL 4-INPUT EXPANDER (FOR USE WITH SN54H50, SN54H53, SN54H55 CIRCUITS)

schematic (each expander)

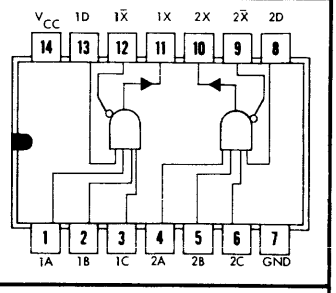


NOTES: 1. Connect to X input of SN54H50, SN54H53, or SN54H55 circuit.
2. Connect to $\bar{X}$ input of SN54H50, SN54H53, or SN54H55 circuit.
3. Component values shown are nominal.

W
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: X = ABCD
when connected to X and $\bar{X}$ pins of SN54H50, SN54H53, or SN54H55 circuit.

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.5 V to 5.5 V
Maximum number of expanders that may be fanned-in to one SN54H50, SN54H53, or SN54H55 circuit 4

electrical characteristics (unless otherwise noted T_A = –55°C to 125°C)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP §	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure output is in the on state	38		2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure output is in the off state	39				0.8	V
V_{on}	On-state output voltage	38	V_{CC} = 4.5 V, V_{in} = 2 V, V_1 = 1 V, I_{on} = 5.85 mA, T_A = –55°C			0.4	V
			V_{CC} = 5.5 V, V_{in} = 2 V, V_1 = 0.6 V, I_{on} = 7.85 mA, T_A = 125°C			0.4	V
I_{off}	Off-state output current	39	V_{CC} = 4.5 V, V_{in} = 0.8 V, V_1 = 4.5 V, R = 575 Ω, T_A = –55°C			320	μA
I_{on}	On-state output current	40	V_{CC} = 4.5 V, V_{in} = 2 V, V_1 = 1 V, T_A = –55°C	–470			μA
$I_{in(0)}$	Logical 0 level input current (each input)	39	V_{CC} = 5.5 V, V_{in} = 0.4 V			–2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	41	V_{CC} = 5.5 V, V_{in} = 2.4 V			50	μA
			V_{CC} = 5.5 V, V_{in} = 5.5 V			1	mA
$I_{CC(on)}$	On-state supply current	42	V_{CC} = 5.5 V, V_{in} = 4.5 V, V_1 = 0.85 V		1.9	3.5	mA
$I_{CC(off)}$	Off-state supply current	42	V_{CC} = 5.5 V, V_{in} = 0, V_1 = 0.85 V		3	4.5	mA

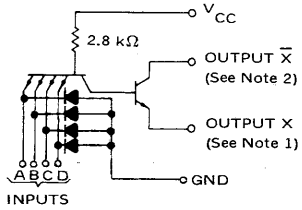
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

output capacitance, V_{CC} and GND terminals open, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$C_{\bar{X}}$	Effective capacitance of output transistor Q_1	79	f = 1 MHz		1.3		pF

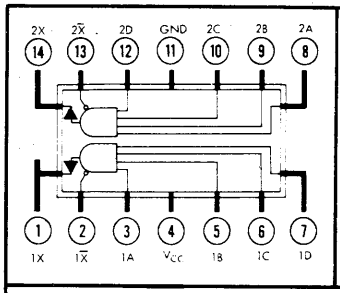
CIRCUIT TYPE SN74H60
DUAL 4-INPUT EXPANDER

schematic (each expander)

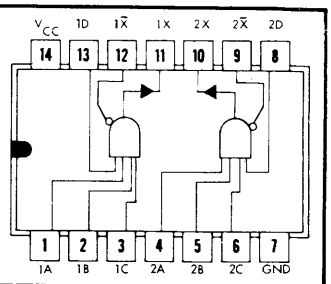


NOTES: 1. Connect to X input of SN74H50, SN74H53, or SN74H55 circuit.
2. Connect to $\overline{X}$ input of SN74H50, SN74H53, or SN74H55 circuit.
3. Component values shown are nominal.

W
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $X = \overline{ABCD}$
when connected to X and $\overline{X}$ pins of SN74H50, SN74H53, or SN74H55 circuits.

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.75 V to 5.25 V
Maximum number of expanders that may be fanned-in to one SN74H50, SN74H53, or SN74H55 circuit 4

electrical characteristics (unless otherwise noted T_A = 0°C to 70°C)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP §	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure output is in the on state	38		2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure output is in the off state	39				0.8	V
V_{on}	On-state output voltage	38	V_{CC} = 4.75 V, V_{in} = 2 V, V_I = 1 V, I_{on} = 6.3 mA, T_A = 0°C			0.4	V
			V_{CC} = 5.25 V, V_{in} = 2 V, V_I = 0.6 V, I_{on} = 7.4 mA, T_A = 70°C			0.4	V
I_{off}	Off-state output current	39	V_{CC} = 4.75 V, V_{in} = 0.8 V, V_I = 4.5 V, R = 575 Ω, T_A = 0°C			570	μA
I_{on}	On-state output current	40	V_{CC} = 4.75 V, V_{in} = 2 V, V_I = 1 V, T_A = 0°C	−600			μA
$I_{in(0)}$	Logical 0 level input current (each input)	39	V_{CC} = 5.25 V, V_{in} = 0.4 V			−2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	41	V_{CC} = 5.25 V, V_{in} = 2.4 V			50	μA
			V_{CC} = 5.25 V, V_{in} = 5.5 V			1	mA
$I_{CC(on)}$	On-state supply current	42	V_{CC} = 5.25 V, V_{in} = 4.5 V, V_I = 0.85 V		1.9	3.5	mA
$I_{CC(off)}$	Off-state supply current	42	V_{CC} = 5.25 V, V_{in} = 0, V_I = 0.85 V		3	4.5	mA

§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

output capacitance, V_{CC} and GND terminals open, T_A = 25°C

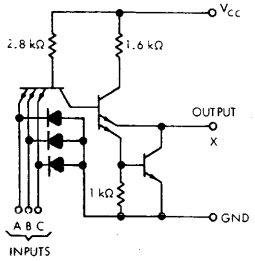
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$C_{\overline{x}}$	Effective capacitance of output transistor Q_1	79	f = 1 MHz		1.3		pF

7

CIRCUIT TYPES SN54H61, SN74H61
TRIPLE 3-INPUT EXPANDERS

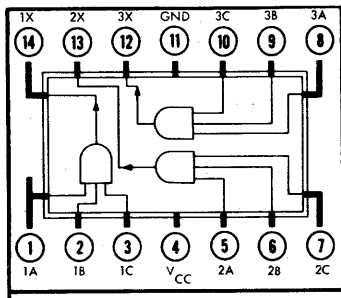
(FOR USE WITH SN54H52, SN74H52 CIRCUITS)

schematic (each expander)

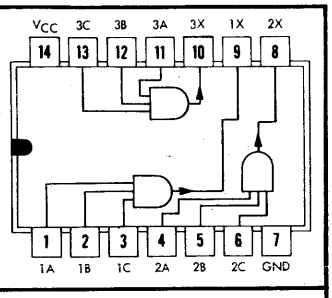


NOTES: 1. Component values shown are nominal.
2. A total of six expander gates may be connected to the SN54H52/SN74H52 expander input.

W
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: X = ABC
when connected to the X input of the SN54H52 or SN74H52 circuit.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H61 Circuits	4.5	5	5.5	V
SN74H61 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A: SN54H61 Circuits	−55	25	125	°C
SN74H61 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP§	MAX	UNIT
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure output is in the off state	43				0.8	V
I_{off}	Off-state reverse current	43	V_{CC} = MIN, $V_{in(0)}$ = 0.8 V, V_{off} = 2.2 V, T_A = MAX			50	μA
$I_{in(0)}$	Logical 0 level input current (each input)	44	V_{CC} = MAX, V_{in} = 0.4 V			−2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	45	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{CC(on)}$	On-state supply current	46	V_{CC} = MAX, V_{in} = 4.5 V		11	16	mA
$I_{CC(off)}$	Off-state supply current	46	V_{CC} = MAX, V_{in} = 0		5	7	mA

electrical characteristics SN54H61 circuits only

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure output is in the on state	47	V_{CC} = 4.5 V	2			V
V_{on}	On-state output voltage	47	V_{CC} = 4.5 V, $V_{in(1)}$ = 2 V, I_{on} = 4.5 mA, T_A = −55°C			1	V

electrical characteristics SN74H61 circuits only

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure output is in the on state	47	V_{CC} = 4.75 V	2			V
V_{on}	On-state output voltage	47	V_{CC} = 4.75 V, $V_{in(1)}$ = 2 V, I_{on} = 5.35 mA, T_A = 0°C			1	V

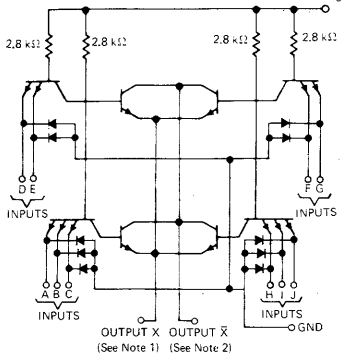
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

output capacitance, V_{CC} and GND terminals open, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_x	Effective capacitance of output transistor Q_1	80	f = 1 MHz		1.3		pF

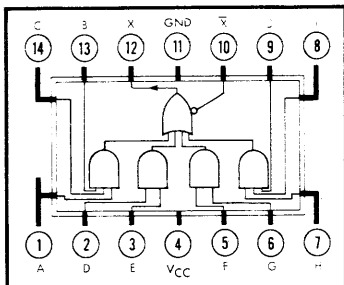
CIRCUIT TYPE SN54H62
3-2-2-3-INPUT AND-OR EXPANDER

schematic



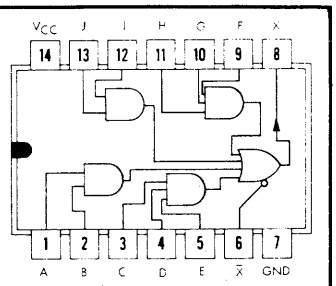
NOTES: 1. Connect to X input of SN54H50, SN54H53, or SN54H55 circuit.
2. Connect to $\overline{X}$ input of SN54H50, SN54H53, or SN54H55 circuit.
3. Component values shown are nominal.

W
FLAT PACKAGE (TOP VIEW)



positive logic:
X = (ABC) + (DE) + (FG) + (HIJ)
when connected to X and $\overline{X}$ pins of SN54H50, SN54H53, or SN54H55 circuit.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic:
X = (AB) + (CDE) + (FGH) + (IJ)
when connected to X and $\overline{X}$ pins of SN54H50, SN54H53, or SN54H55 circuit.

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.5 V to 5.5 V
Maximum number of expanders that may be fanned-in to one SN54H50, SN54H53, or SN54H55 circuit 1

electrical characteristics (unless otherwise noted $T_A = -55°C$ to $125°C$)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP§	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals of one AND section to ensure output is in the on state	48		2			V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure output is in the off state	49				0.8	V
V_{on}	On-state output voltage	48	V_{CC} = 4.5 V, V_{in} = 2 V, V_I = 1 V, I_{on} = 5.85 mA, T_A = −55°C			0.4	V
			V_{CC} = 5.5 V, V_{in} = 2 V, V_I = 0.6 V, I_{on} = 7.85 mA, T_A = 125°C			0.4	V
I_{off}	Off-state output current	49	V_{CC} = 4.5 V, V_{in} = 0.8 V, V_I = 4.5 V, R = 575 Ω, T_A = −55°C			320	μA
I_{on}	On-state output current	50	V_{CC} = 4.5 V, V_{in} = 2 V, V_I = 1 V, T_A = −55°C	−470			μA
$I_{in(0)}$	Logical 0 level input current (each input)	51	V_{CC} = 5.5 V, V_{in} = 0.4 V			−2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	52	V_{CC} = 5.5 V, V_{in} = 2.4 V			50	μA
			V_{CC} = 5.5 V, V_{in} = 5.5 V			1	mA
$I_{CC(on)}$	On-state supply current	53	V_{CC} = 5.5 V, V_{in} = 4.5 V, V_I = 0.85 V		3.8	7	mA
$I_{CC(off)}$	Off-state supply current	53	V_{CC} = 5.5 V, V_{in} = 0, V_I = 0.85 V		6	9	mA

§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

output capacitance, V_{CC} and GND terminals open, $T_A = 25°C$

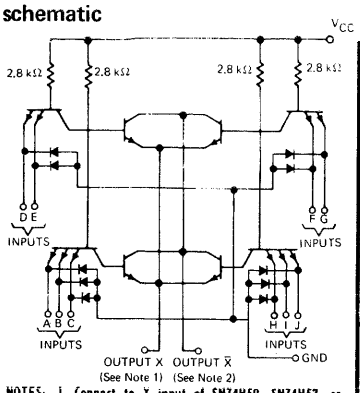
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$C_{\overline{X}}$	Effective capacitance of output transistor Q_1	79	f = 1 MHz		1.3		pF

7

CIRCUIT TYPE SN74H62
3-2-2-3-INPUT AND-OR EXPANDER

(FOR USE WITH SN74H50, SN74H53, SN74H55 CIRCUITS)

schematic

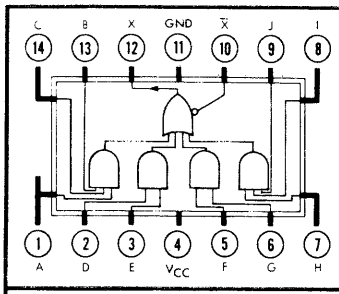


NOTES: 1. Connect to X input of SN74H50, SN74H53, or SN74H55 circuit.

2. Connect to $\overline{X}$ input of SN74H50, SN74H53, or SN74H55 circuit.

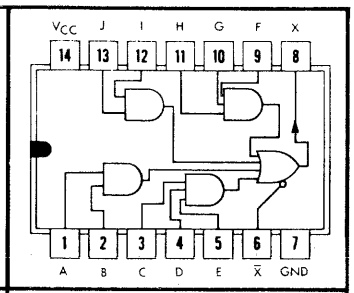
3. Component values shown are nominal.

W
FLAT PACKAGE (TOP VIEW)



positive logic:
X = (ABC) + (DE) + (FG) + (HIJ)
when connected to X and $\overline{X}$ pins of SN74H50, SN74H53, or SN74H55 circuit.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic:
X = (AB) + (CDE) + (FGH) + (IJ)
when connected to X and $\overline{X}$ pins of SN74H50, SN74H53, or SN74H55 circuit.

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.75 V to 5.25 V

Maximum number of expanders that may be fanned-in to one SN74H50, SN74H53, or SN74H55 circuit 1

electrical characteristics (unless otherwise noted T_A = 0°C to 70°C)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP §	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals of one AND section to ensure output is in the on state	48		2			V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure output is in the off state	49				0.8	V
V_{on}	On-state output voltage	48	V_{CC} = 4.75 V, V_{in} = 2 V, V_I = 1 V, I_{on} = 6.3 mA, T_A = 0°C			0.4	V
			V_{CC} = 5.25 V, V_{in} = 2 V, V_I = 0.6 V, I_{on} = 7.4 mA, T_A = 70°C			0.4	V
I_{off}	Off-state output current	49	V_{CC} = 4.75 V, V_{in} = 0.8 V, V_I = 4.5 V, R = 575 Ω, T_A = 0°C			570	μA
I_{on}	On-state output current	50	V_{CC} = 4.75 V, V_{in} = 2 V, V_I = 1 V, T_A = 0°C	−600			μA
$I_{in(0)}$	Logical 0 level input current (each input)	51	V_{CC} = 5.25 V, V_{in} = 0.4 V			−2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	52	V_{CC} = 5.25 V, V_{in} = 2.4 V			50	μA
			V_{CC} = 5.25 V, V_{in} = 5.5 V			1	mA
$I_{CC(on)}$	On-state supply current	53	V_{CC} = 5.25 V, V_{in} = 4.5 V, V_I = 0.85 V		3.8	7	mA
$I_{CC(off)}$	Off-state supply current	53	V_{CC} = 5.25 V, V_{in} = 0, V_I = 0.85 V		6	9	mA

§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

output capacitance, V_{CC} and GND terminals open, T_A = 25°C

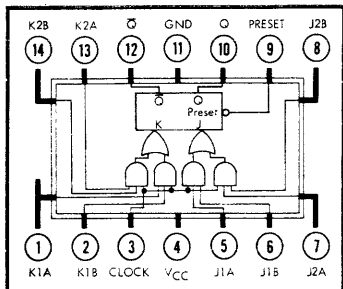
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$C_{\overline{x}}$	Effective capacitance of output transistor Q_1	79	f = 1 MHz		1.3		pF

logic

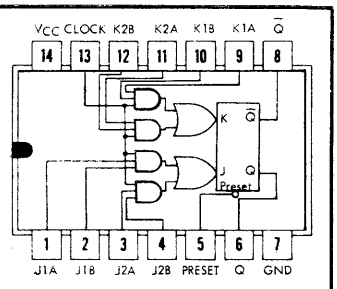
TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES: 1. J = (J1A • J1B) + (J2A • J2B)
2. K = (K1A • K1B) + (K2A • K2B)
3. t_n = Bit time before clock pulse.
4. t_{n+1} = Bit time after clock pulse.

W
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



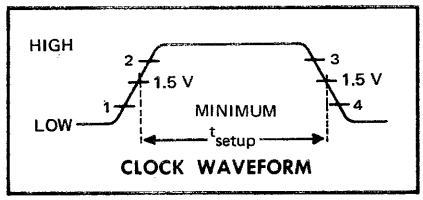
positive logic: Low input to preset sets Q to logical 1
Preset is independent of clock.

description

These J-K flip-flops are based on the master-slave principle. The AND-OR gate inputs for entry into the master section are controlled by the clock pulse. The clock pulse also regulates the circuitry which connects the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from AND-OR gate inputs to master
3. Disable AND-OR gate inputs
4. Transfer information from master to slave.

Logical state of J and K inputs must not be allowed to change when the clock pulse is in a high state.



CLOCK WAVEFORM

7

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H71 Circuits	4.5	5	5.5	V
SN74H71 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A: SN54H71 Circuits	−55	25	125	°C
SN74H71 Circuits	0	25	70	°C
Normalized Fan-Out From Each Output, N			10	
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 77)	12			ns
Width of Preset Pulse, $t_{p(preset)}$ (See Figure 78)	16			ns
Input Setup Time, t_{setup} (See Above)	≥ $t_{p(clock)}$			
Input Hold Time, t_{hold}	0			

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP§	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	54 and 55		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	54 and 55				0.8	V
$V_{out(1)}$	Logical 1 output voltage	54	V_{CC} = MIN, I_{load} = −500 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	55	V_{CC} = MIN, I_{sink} = 20 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current at J1A, J1B, J2A, J2B, K1A, K1B, K2A, or K2B	56	V_{CC} = MAX, V_{in} = 0.4 V			−2	mA
$I_{in(0)}$	Logical 0 level input current at preset	56	V_{CC} = MAX, V_{in} = 0.4 V			−6	mA
$I_{in(0)}$	Logical 0 level input current at clock	56	V_{CC} = MAX, V_{in} = 0.4 V			−4	mA
$I_{in(1)}$	Logical 1 level input current at J1A, J1B, J2A, J2B, K1A, K1B, K2A, or K2B	57	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at preset	57	V_{CC} = MAX, V_{in} = 2.4 V			150	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at clock	57	V_{CC} = MAX, V_{in} = 2.4 V			100	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{os}	Short-circuit output current‡	58	V_{CC} = MAX, V_{in} = 0	−40		−100	mA
I_{CC}	Supply current	57	V_{CC} = MAX		19	30	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

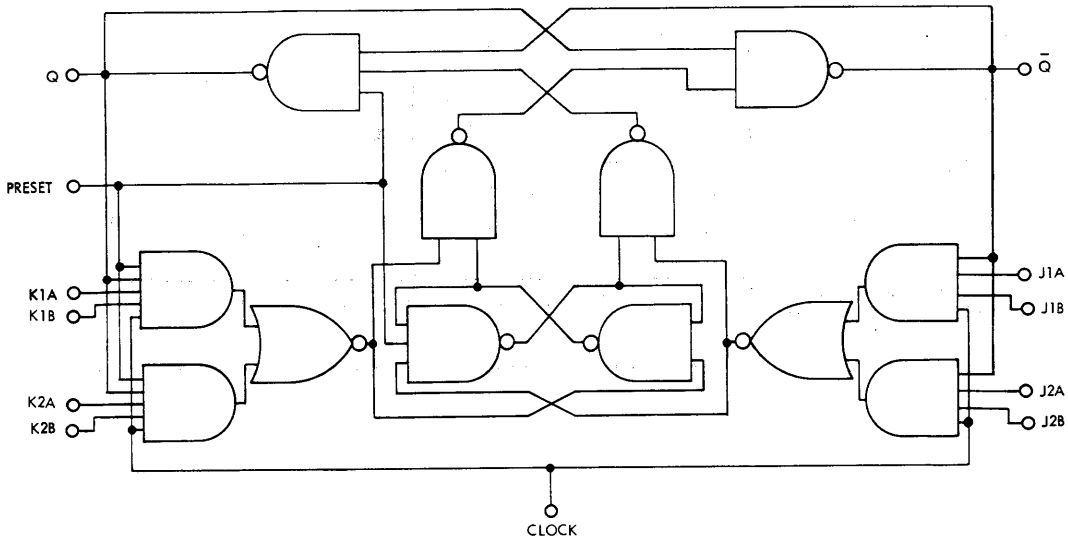
‡Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

§All typical values are at V_{CC} = 5 V, T_A = 25°C.

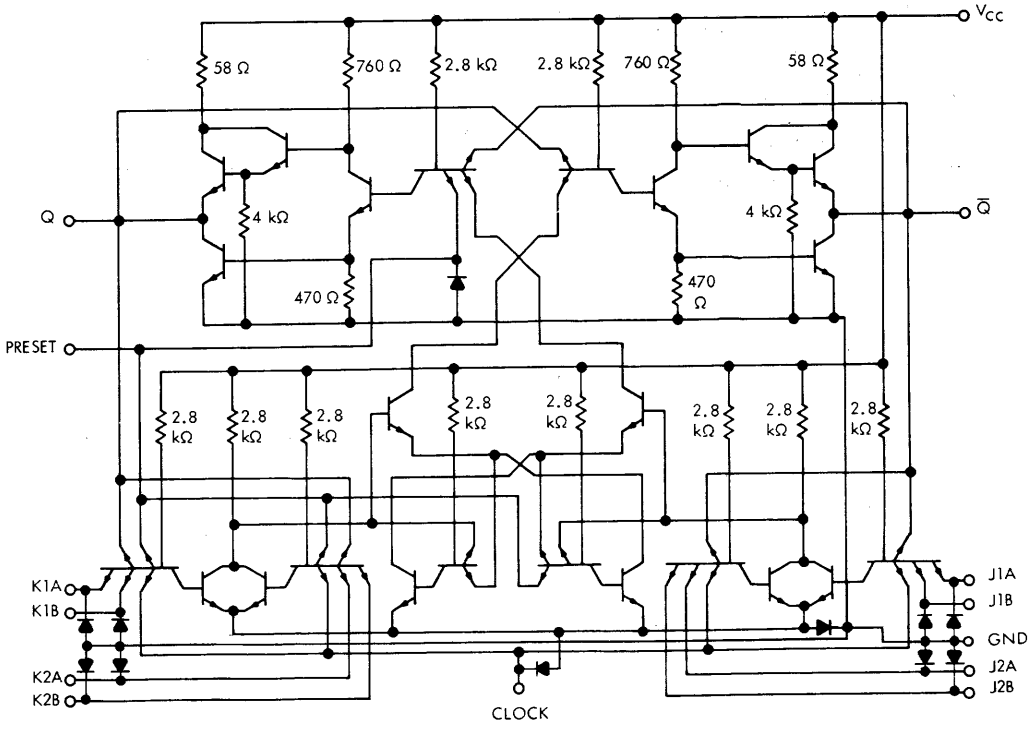
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	77	C_L = 25 pF, R_L = 280 Ω	25	30		MHz
t_{pd1}	Propagation delay time to logical 1 level from preset to output	78	C_L = 25 pF, R_L = 280 Ω		6	13	ns
t_{pd0}	Propagation delay time to logical 0 level from preset to output	78	C_L = 25 pF, R_L = 280 Ω		12	24	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	77	C_L = 25 pF, R_L = 280 Ω	6	14	21	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	77	C_L = 25 pF, R_L = 280 Ω	10	22	27	ns

functional block diagram



schematic



Component values shown are nominal.

7

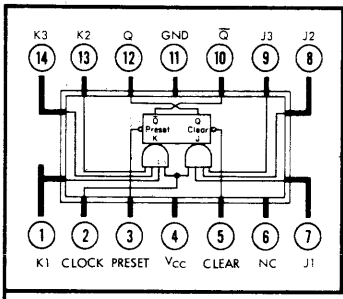
CIRCUIT TYPES SN54H72, SN74H72
J-K MASTER-SLAVE FLIP-FLOPS

logic

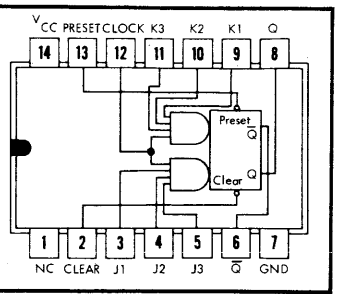
TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES: 1. $J = J1 \cdot J2 \cdot J3$
2. $K = K1 \cdot K2 \cdot K3$
3. t_n = Bit time before clock pulse.
4. t_{n+1} = Bit time after clock pulse.

W
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



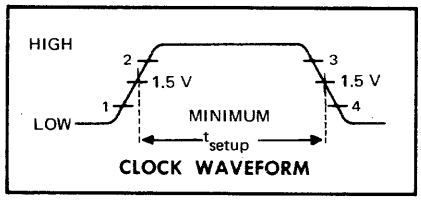
positive logic: Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Preset and clear are independent of clock

description

These J-K flip-flops are based on the master-slave principle. The AND gate inputs for entry into the master section are controlled by the clock pulse. The clock pulse also regulates the circuitry which connects the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from AND gate inputs to master
3. Disable AND gate inputs
4. Transfer information from master to slave.

Logical state of J and K inputs must not be allowed to change when the clock pulse is in a high state.



CLOCK WAVEFORM

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H72 Circuits	4.5	5	5.5	V
SN74H72 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A: SN54H72 Circuits	−55	25	125	°C
SN74H72 Circuits	0	25	70	°C
Normalized Fan-Out From Each Output, N			10	
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 77)	12			ns
Width of Preset Pulse, $t_{p(preset)}$ (See Figure 78)	16			ns
Width of Clear Pulse, $t_{p(clear)}$ (See Figure 78)	16			ns
Input Setup Time, t_{setup} (See Above)	≥ $t_{p(clock)}$			
Input Hold Time, t_{hold}	0			

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP§	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	59 and 60			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	59 and 60					0.8	V
$V_{out(1)}$	Logical 1 output voltage	59	V_{CC} = MIN,	I_{load} = −500 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	60	V_{CC} = MIN,	I_{sink} = 20 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current at J1, J2, J3, K1, K2, K3, or clock	61	V_{CC} = MAX,	V_{in} = 0.4 V			−2	mA
$I_{in(0)}$	Logical 0 level input current at preset or clear	61	V_{CC} = MAX,	V_{in} = 0.4 V			−4	mA
$I_{in(1)}$	Logical 1 level input current at J1, J2, J3, K1, K2, or K3	62	V_{CC} = MAX,	V_{in} = 2.4 V			50	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at clock	62	V_{CC} = MAX,	V_{in} = 2.4 V			50	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at preset or clear	62	V_{CC} = MAX,	V_{in} = 2.4 V			100	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current‡	63	V_{CC} = MAX,	V_{in} = 0	−40		−100	mA
I_{CC}	Supply current	62	V_{CC} = MAX			16	25	mA

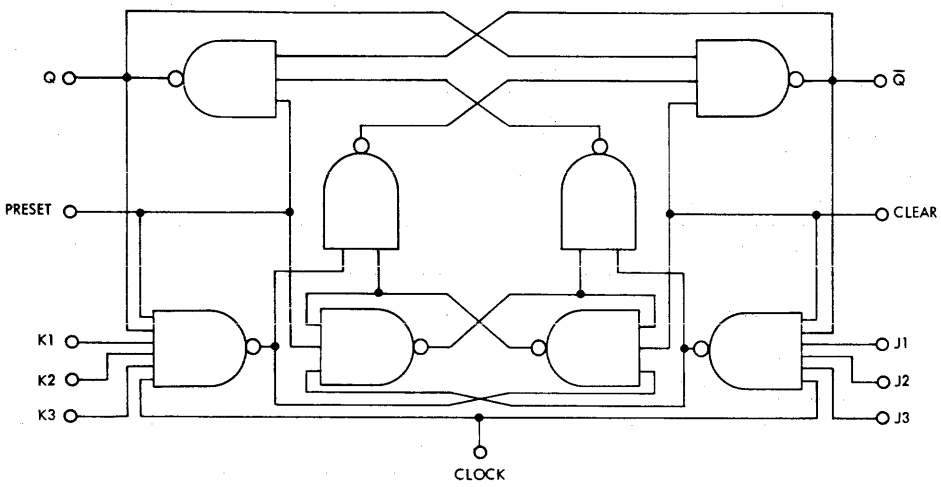
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.
§All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

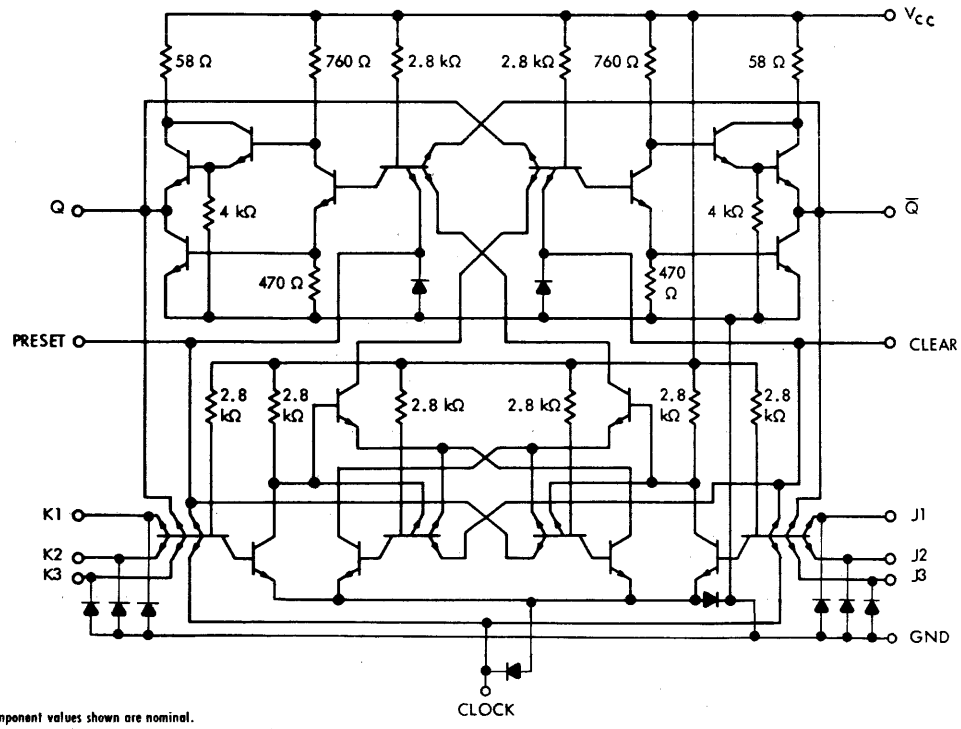
PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	77	C_L = 25 pF,	R_L = 280 Ω	25	30		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output	78	C_L = 25 pF,	R_L = 280 Ω		6	13	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output	78	C_L = 25 pF,	R_L = 280 Ω		12	24	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	77	C_L = 25 pF,	R_L = 280 Ω	6	14	21	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	77	C_L = 25 pF,	R_L = 280 Ω	10	22	27	ns

CIRCUIT TYPES SN54H72, SN74H72
J-K MASTER-SLAVE FLIP-FLOPS

functional block diagram



schematic



Component values shown are nominal.

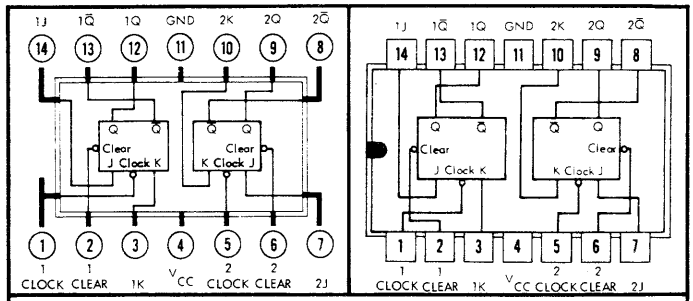
logic

TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES: 1. t_n = Bit time before clock pulse.
2. t_{n+1} = Bit time after clock pulse.

W
FLAT PACKAGE (TOP VIEW)

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: Low input to clear sets Q to logical 0
Clear is independent of clock

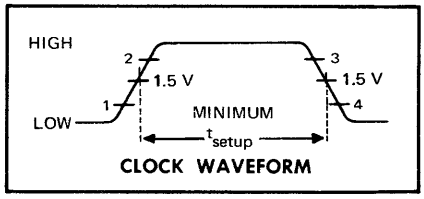
description

These J-K flip-flops are based on the master-slave principle. The AND gate inputs for entry into the master section are controlled by the clock pulse. The clock pulse also regulates the circuitry which connects the master and slave sections.

The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from AND gate inputs to master
3. Disable AND gate inputs
4. Transfer information from master to slave.

Logical state of J and K inputs must not be allowed to change when the clock pulse is in a high state.



CLOCK WAVEFORM

7

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H73 Circuits	4.5	5	5.5	V
SN74H73 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A: SN54H73 Circuits	−55	25	125	°C
SN74H73 Circuits	0	25	70	°C
Normalized Fan-Out From Each Output, N			10	
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 77)	12			ns
Width of Clear Pulse, $t_{p(clear)}$ (See Figure 78)	16			ns
Input Setup Time, t_{setup} (See Above)	≥ $t_{p(clock)}$			
Input Hold Time, t_{hold}	0			

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP §	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	64 and 65			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	64 and 65					0.8	V
$V_{out(1)}$	Logical 1 output voltage	64	V_{CC} = MIN,	I_{load} = −500 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	65	V_{CC} = MIN,	I_{sink} = 20 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current at J, K, or clock	66	V_{CC} = MAX,	V_{in} = 0.4 V			−2	mA
$I_{in(0)}$	Logical 0 level input current at clear	66	V_{CC} = MAX,	V_{in} = 0.4 V			−4	mA
$I_{in(1)}$	Logical 1 level input current at J or K	67	V_{CC} = MAX,	V_{in} = 2.4 V			50	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at clock	67	V_{CC} = MAX,	V_{in} = 2.4 V			50	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at clear	67	V_{CC} = MAX,	V_{in} = 2.4 V			100	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current‡	68	V_{CC} = MAX,	V_{in} = 0	−40		−100	mA
I_{CC}	Supply current	67	V_{CC} = MAX			32	50	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

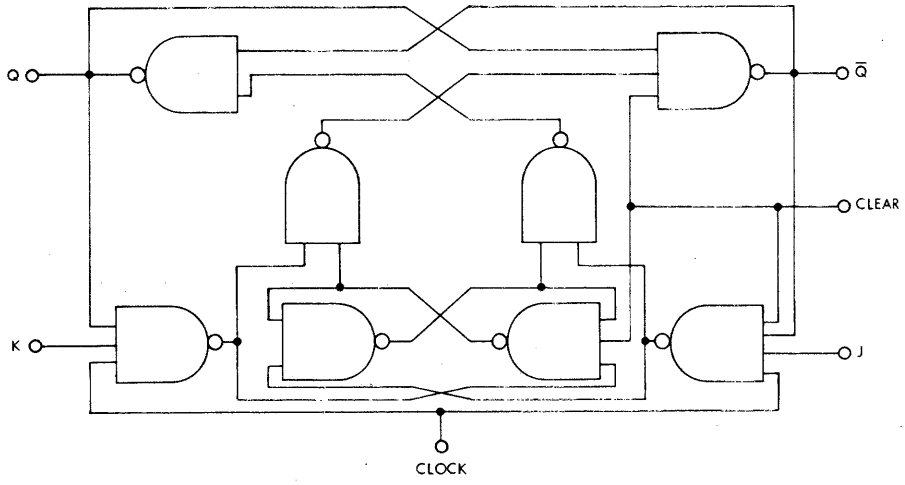
‡Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

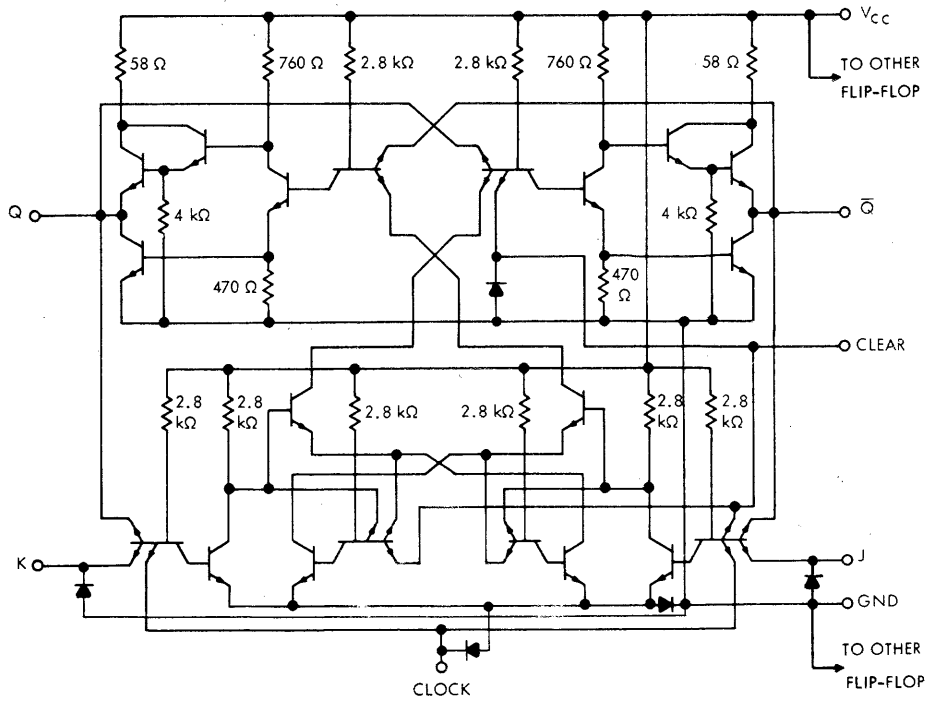
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	77	C_L = 25 pF,	R_L = 280 Ω	25	30		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear to output	78	C_L = 25 pF,	R_L = 280 Ω		6	13	ns
t_{pd0}	Propagation delay time to logical 0 level from clear to output	78	C_L = 25 pF,	R_L = 280 Ω		12	24	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	77	C_L = 25 pF,	R_L = 280 Ω	6	14	21	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	77	C_L = 25 pF,	R_L = 280 Ω	10	22	27	ns

functional block diagram (each flip-flop)



schematic (each flip-flop)



Component values shown are nominal.

7

CIRCUIT TYPES SN54H74, SN74H74
DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS

- Maximum Clock Frequency: 35 Megahertz
- Positive-Edge Triggering
- High-Fan-Out, Low-Impedance, Totem-Pole Outputs
- Input Clamping Diodes Simplify System Design
- Fully Compatible with most TTL and DTL Circuits
- Typical Power Dissipation: 75 Milliwatts per Flip-Flop

logic

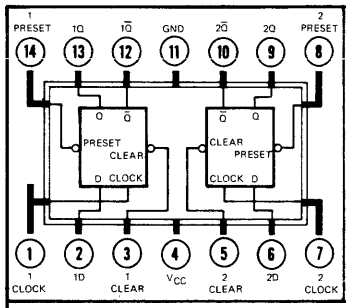
TRUTH TABLE (Each Flip-Flop)

t_n	t_{n+1}	
INPUT D	OUTPUT Q	OUTPUT $\overline{Q}$
L	L	H
H	H	L

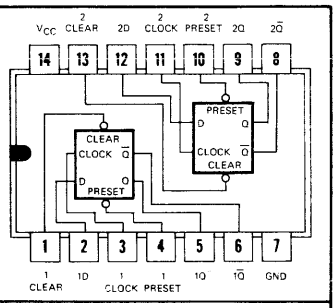
H = high level, L = low level

NOTES: A. t_n = bit time before clock pulse.
B. t_{n+1} = bit time after clock pulse.

W
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



asynchronous inputs: Low input to preset sets Q to high level
Low input to clear sets Q to low level
Preset and clear are independent of clock

description

These monolithic, high-speed, dual, edge-triggered flip-flops utilize TTL circuitry to perform D-type flip-flop logic. Each flip-flop has individual clear and preset inputs, and also complementary Q and $\overline{Q}$ outputs.

Information at input D is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D-input signal has no effect.

These circuits are fully compatible for use with most TTL or DTL circuits. Input clamping diodes are provided to minimize transmission line effects and thereby simplify systems design. A full fan-out to 10 normalized Series 54H/74H loads is available from each of the outputs in the low-level condition. In the high-level state, a fan-out of 20 is available to facilitate tying unused inputs to used inputs. Maximum clock frequency is 35 megahertz, with a typical power dissipation of 75 milliwatts per flip-flop.

The SN54H74 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74H74 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range, T_A: SN54H74 Circuits . . . . . −55°C to 125°C
SN74H74 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor.

recommended operating conditions

		SN54H74			SN74H74			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Clock frequency, f_{clock}		0		35	0		35	MHz
Width of clock pulse, $t_{w(clock)}$ (see Figure 87 or 88)		15			15			ns
Width of preset pulse, $t_{w(preset)}$ (see Figure 86)		25			25			ns
Width of clear pulse, $t_{w(clear)}$ (see Figure 86)		25			25			ns
Input setup time, t_{setup} (see Note 3)	High-level data (see Figure 87)	10			10			ns
	Low-level data (see Figure 88)	15			15			ns
Input hold time, t_{hold} (see Note 4 and Figures 87 and 88)		0			0			ns
Operating free-air temperature range, T_A		−55	25	125	0	25	70	°C

NOTES: 3. Setup time is the interval immediately preceding the positive-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.
4. Hold time is the interval immediately following the positive-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its continued recognition.

7

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage	81 and 82			2			V
V_{IL}	Low-level input voltage	81 and 82					0.8	V
V_{OH}	High-level output voltage	81	V_{CC} = MIN, I_{OH} = −1 mA		2.4	3.5		V
V_{OL}	Low-level output voltage	82	V_{CC} = MIN, I_{OL} = 20 mA			0.22	0.4	V
I_{IH}	High-level input current into D	83	V_{CC} = MAX, V_I = 2.4 V				50	μA
			V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current into preset or clock	83	V_{CC} = MAX, V_I = 2.4 V				100	μA
			V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current into clear	83	V_{CC} = MAX, V_I = 2.4 V				150	μA
			V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IL}	Low-level input current into preset or D	84	V_{CC} = MAX, V_I = 0.4 V				−2	mA
I_{IL}	Low-level input current into clear or clock	84	V_{CC} = MAX, V_I = 0.4 V				−4	mA
I_{OS}	Short-circuit output current§	85	V_{CC} = MAX		−40		−100	mA
I_{CC}	Supply current	83	V_{CC} = MAX	SN54H74		30	42	mA
				SN74H74		30	50	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

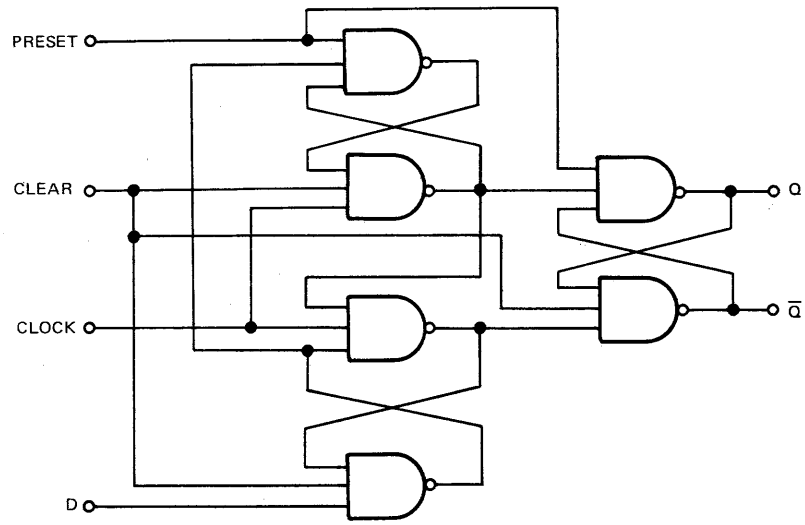
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

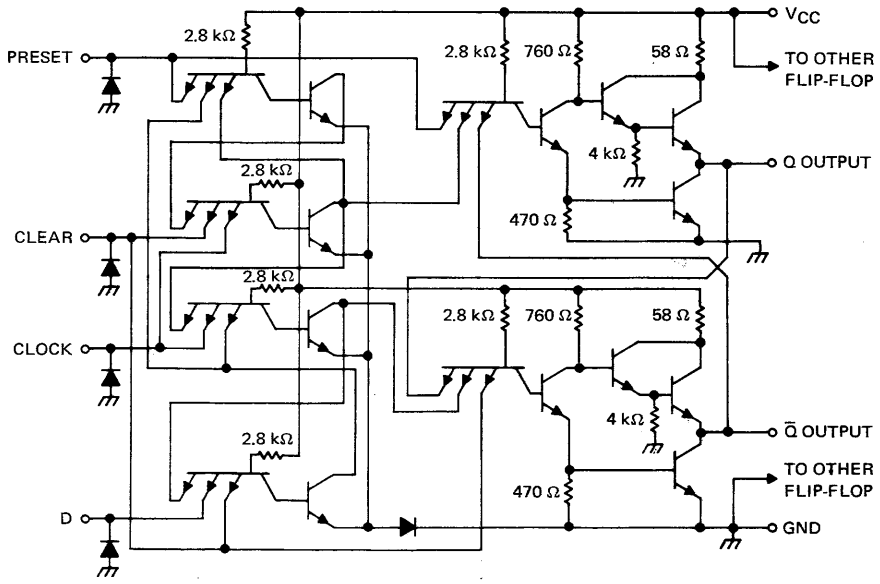
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	87 and 88	C_L = 25 pF, R_L = 280 Ω	35	43		MHz
t_{PLH}	Propagation delay time, low-to-high-level output, from clear or preset inputs	86				20	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from clear or preset inputs	86				30	ns
t_{PLH}	Propagation delay time, low-to-high-level output, from clock input	87 and 88		4	8.5	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from clock input	87 and 88		7	13	20	ns

functional block diagram (each flip-flop)



schematic (each flip-flop)



NOTE: Component values shown are nominal.

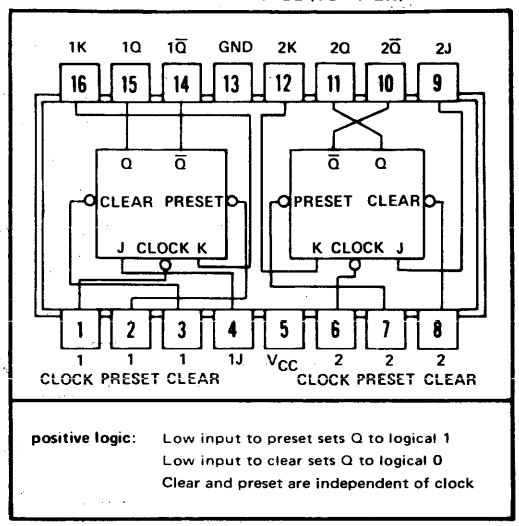
CIRCUIT TYPES SN54H76, SN74H76
DUAL J-K MASTER-SLAVE FLIP-FLOPS

logic

TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES: 1. t_n = Bit time before clock pulse
2. t_{n+1} = Bit time after clock pulse

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



positive logic: Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Clear and preset are independent of clock

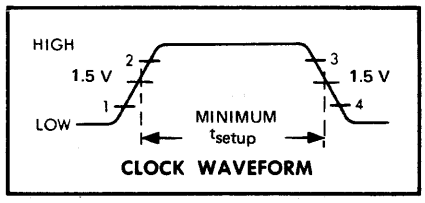
†Pin assignments for these circuits are the same for all packages.

description

These dual J-K flip-flops are based on the master-slave principle. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the circuitry which connects the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from J and K inputs to master
3. Disable J and K inputs
4. Transfer information from master to slave.

Logical state of J and K inputs must not be allowed to change when the clock pulse is in a high state.



CLOCK WAVEFORM

recommended operating conditions

	SN54H76			SN74H76			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N			10			10	
Width of clock pulse, $t_{p(clock)}$ (See Figure 77)	12			12			ns
Width of preset pulse, $t_{p(preset)}$ (See Figure 78)	16			16			ns
Width of clear pulse, $t_{p(clear)}$ (See Figure 78)	$\geq t_{p(clock)}$			$\geq t_{p(clock)}$			
Input setup time, t_{setup} (See Above)							
Input hold time, t_{hold}	0			0			
Operating free-air temperature range, T_A	−55	25	125	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP§	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	64 and 65		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	64 and 65				0.8	V
$V_{out(1)}$	Logical 1 output voltage	64	V_{CC} = MIN, I_{load} = −500 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	65	V_{CC} = MIN, I_{sink} = 20 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current at J, K, or clock	66	V_{CC} = MAX, V_{in} = 0.4 V			−2	mA
$I_{in(0)}$	Logical 0 level input current at clear or preset	66	V_{CC} = MAX, V_{in} = 0.4 V			−4	mA
$I_{in(1)}$	Logical 1 level input current at J, K, or clock	67	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at clear or preset	67	V_{CC} = MAX, V_{in} = 2.4 V			100	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current‡	68	V_{CC} = MAX, V_{in} = 0	−40		−100	mA
I_{CC}	Supply current	67	V_{CC} = MAX, V_{in} = 4.5 V		32	50	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ Not more than one output should be shorted at a time.

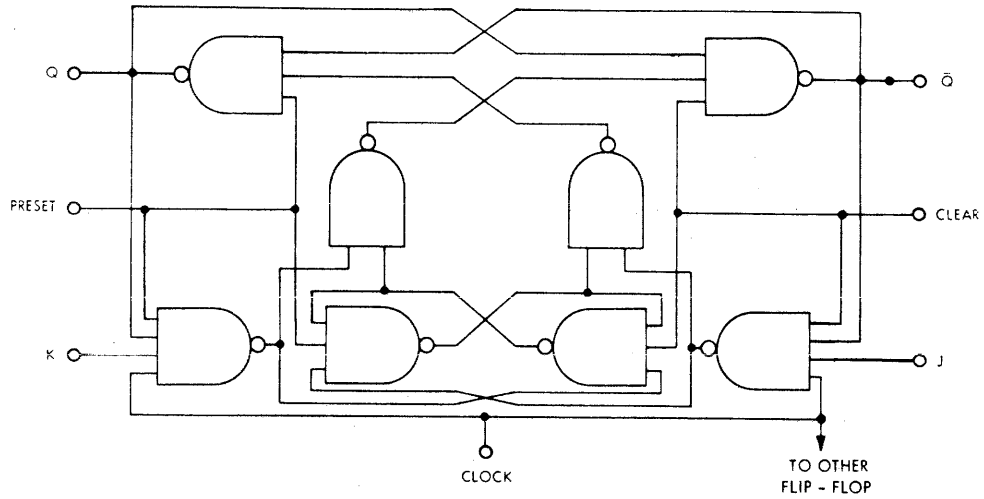
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

7

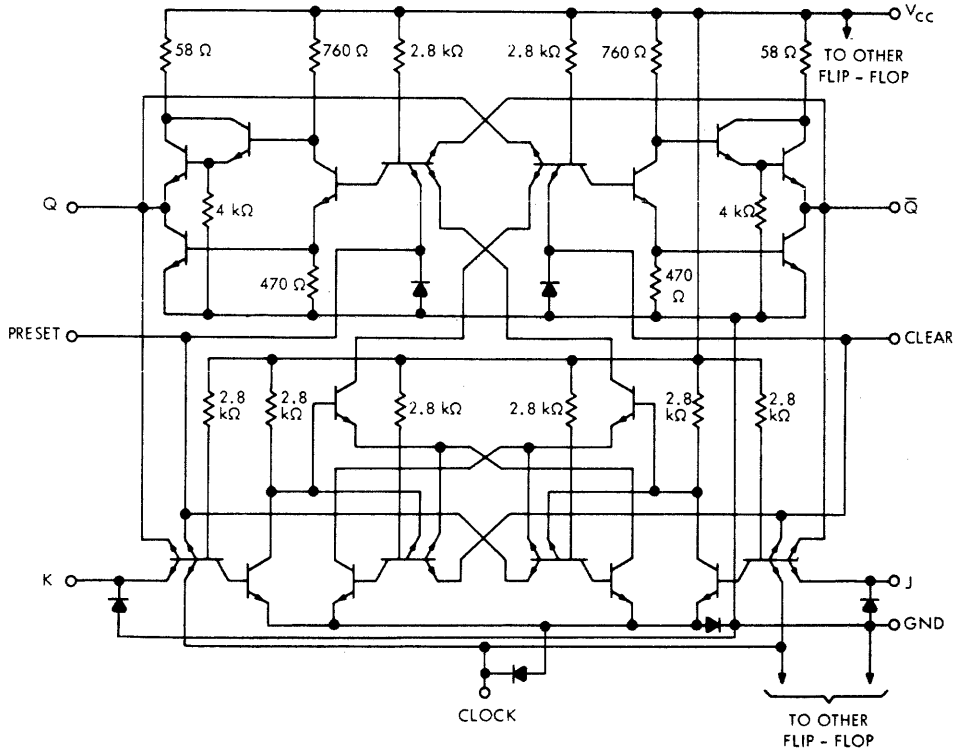
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	77	C_L = 25 pF, R_L = 280 Ω	25	30		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output	78	C_L = 25 pF, R_L = 280 Ω		6	13	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output	78	C_L = 25 pF, R_L = 280 Ω		12	24	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	77	C_L = 25 pF, R_L = 280 Ω	6	14	21	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	77	C_L = 25 pF, R_L = 280 Ω	10	22	27	ns

functional block diagram (each flip-flop)



schematic (each flip-flop)



Component values shown are nominal.

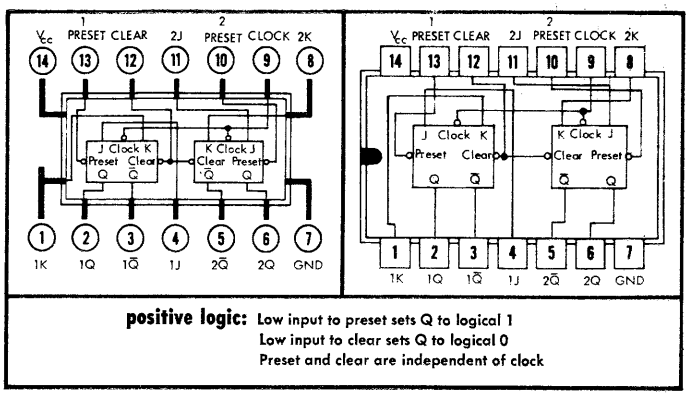
logic

TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES: 1. t_n = Bit time before clock pulse.
2. t_{n+1} = Bit time after clock pulse.

W
FLAT PACKAGE (TOP VIEW)

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



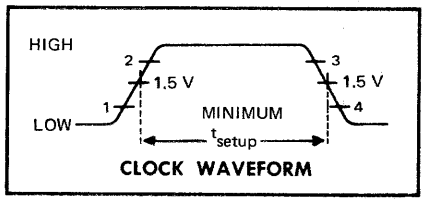
positive logic: Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Preset and clear are independent of clock

description

These J-K flip-flops are based on the master-slave principle. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the circuitry which connects the master and slave sections.
The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from J and K inputs to master
3. Disable J and K inputs
4. Transfer information from master to slave.

Logical state of J and K inputs must not be allowed to change when the clock pulse is in a high state.



CLOCK WAVEFORM

7

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	SN54H78 Circuits	4.5	5	5.5	V
	SN74H78 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A:	SN54H78 Circuits	−55	25	125	°C
	SN74H78 Circuits	0	25	70	°C
Normalized Fan-Out From Each Output, N				10	
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 77)		12			ns
Width of Preset Pulse, $t_{p(preset)}$ (See Figure 78)		16			ns
Width of Clear Pulse, $t_{p(clear)}$ (See Figure 78)		16			ns
Input Setup Time, t_{setup} (See Above)		$\geqslant t_{p(clock)}$			
Input Hold Time, t_{hold}		0			

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP§	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	64 and 65			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	64 and 65					0.8	V
$V_{out(1)}$	Logical 1 output voltage	64	V_{CC} = MIN,	I_{load} = −500 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	65	V_{CC} = MIN,	I_{sink} = 20 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current at J or K	66	V_{CC} = MAX,	V_{in} = 0.4 V			−2	mA
$I_{in(0)}$	Logical 0 level input current at preset or clock	66	V_{CC} = MAX,	V_{in} = 0.4 V			−4	mA
$I_{in(0)}$	Logical 0 level input current at clear	66	V_{CC} = MAX,	V_{in} = 0.4 V			−8	mA
$I_{in(1)}$	Logical 1 level input current at J or K	67	V_{CC} = MAX,	V_{in} = 2.4 V			50	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at preset or clock	67	V_{CC} = MAX,	V_{in} = 2.4 V			100	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at clear	67	V_{CC} = MAX,	V_{in} = 2.4 V			200	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current‡	69	V_{CC} = MAX,	V_{in} = 0	−40		−100	mA
I_{CC}	Supply current	67	V_{CC} = MAX			32	50	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

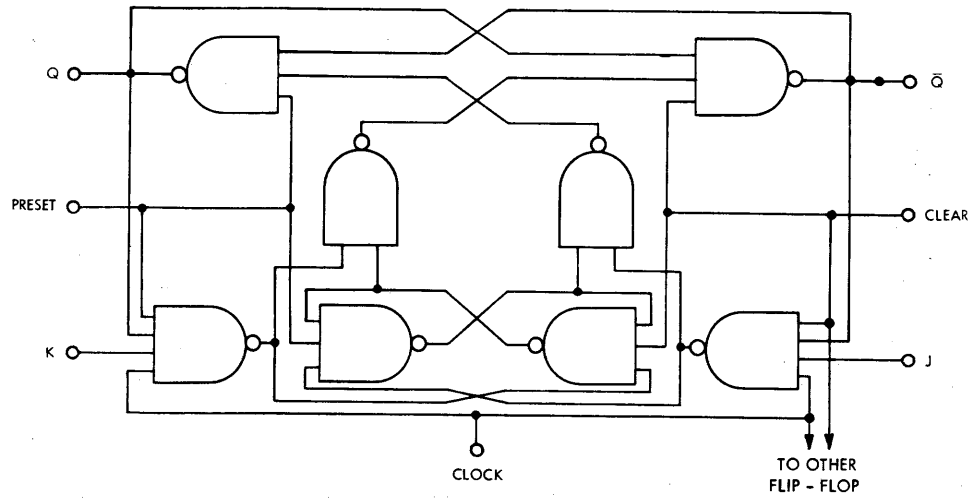
‡Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

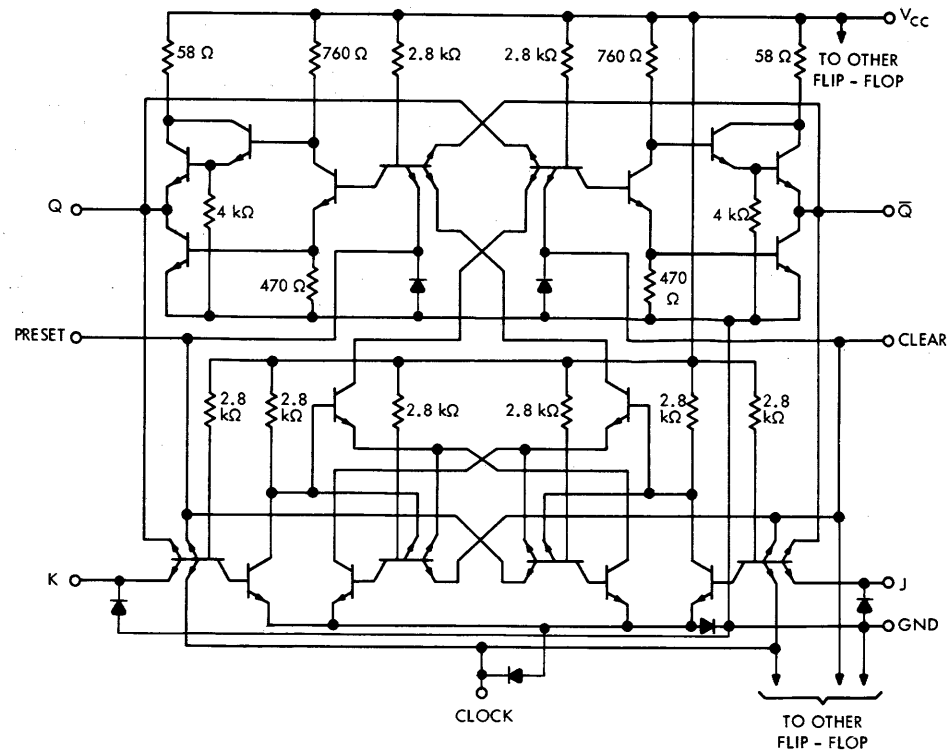
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	77	C_L = 25 pF,	R_L = 280 Ω	25	30		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear to output	78	C_L = 25 pF,	R_L = 280 Ω		6	13	ns
t_{pd0}	Propagation delay time to logical 0 level from clear to output	78	C_L = 25 pF,	R_L = 280 Ω		12	24	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	77	C_L = 25 pF,	R_L = 280 Ω	6	14	21	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	77	C_L = 25 pF,	R_L = 280 Ω	10	22	27	ns

functional block diagram (each flip-flop)



schematic (each flip-flop)



Component values shown are nominal.

7

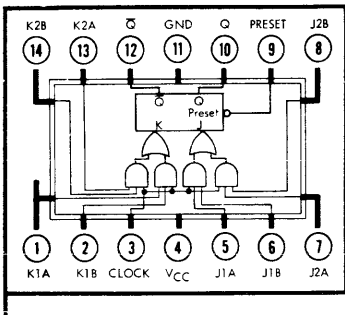
CIRCUIT TYPES SN54H101, SN74H101
J-K EDGE-TRIGGERED FLIP-FLOPS

logic

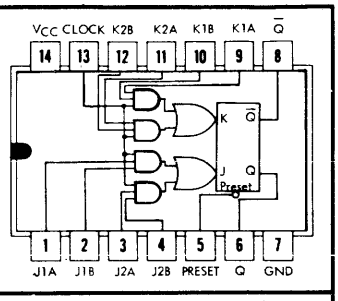
TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES: 1. J = (J1A • J1B) + (J2A • J2B)
2. K = (K1A • K1B) + (K2A • K2B)
3. t_n = Bit time before clock pulse
4. t_{n+1} = Bit time after clock pulse

W
FLAT PACKAGE (TOP VIEW)



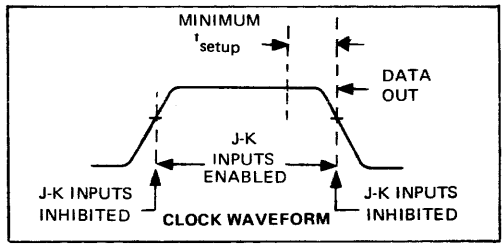
J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: Low input to preset sets Q to logical 1
Preset is independent of clock.

description

These monolithic J-K flip-flops are negative-edge-triggered. The AND-OR gate inputs are inhibited while the clock input is low; when the clock goes high, the inputs are enabled and data will be accepted. Logical state of J and K inputs may be allowed to change when the clock pulse is in a high state and bistable will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative edge of the clock pulse.



recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H101 Circuits	4.5	5	5.5	V
SN74H101 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A: SN54H101 Circuits	−55	25	125	°C
SN74H101 Circuits	0	25	70	°C
Normalized Fan-Out From Each Output, N			10	
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 77)	10			ns
Width of Preset Pulse, $t_{p(preset)}$ (See Figure 78)	16			ns
Input Setup Time, t_{setup} (See Above): Logical 1	10			ns
Logical 0	13			ns
Input Hold Time, t_{hold}	0			ns
Clock Pulse Transition Time, t_0 (See Figure 77)			150	ns

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP§	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	54 and 55		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	54 and 55				0.8	V
$V_{out(1)}$	Logical 1 output voltage	54	V_{CC} = MIN, I_{load} = −500 μA	2.4	3.2		V
$V_{out(0)}$	Logical 0 output voltage	55	V_{CC} = MIN, I_{sink} = 20 mA		0.25	0.4	V
$I_{in(0)}$	Logical 0 level input current at J1A, J1B, J2A, J2B, K1A, K1B, K2A, K2B,or preset	56	V_{CC} = MAX, V_{in} = 0.4 V		−1	−2	mA
$I_{in(0)}$	Logical 0 level input current at clock	56	V_{CC} = MAX, V_{in} = 0.4 V		−3	−4.8	mA
$I_{in(1)}$	Logical 1 level input current at J or K	57	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at preset	57	V_{CC} = MAX, V_{in} = 2.4 V			100	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at clock	57	V_{CC} = MAX, V_{in} = 2.4 V	0		−1	mA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current‡	58	V_{CC} = MAX, V_{in} = 0	−40		−100	mA
I_{CC}	Supply current	57	V_{CC} = MAX		20	38	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

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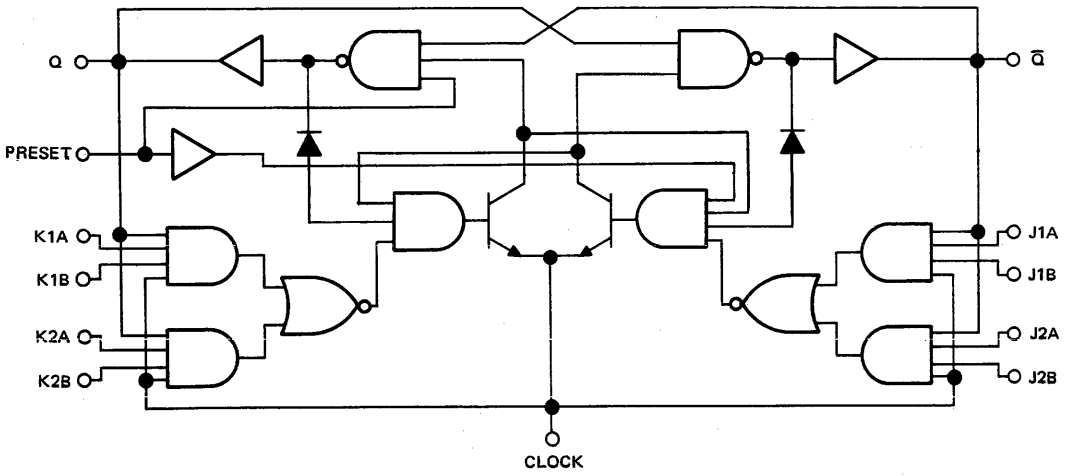
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

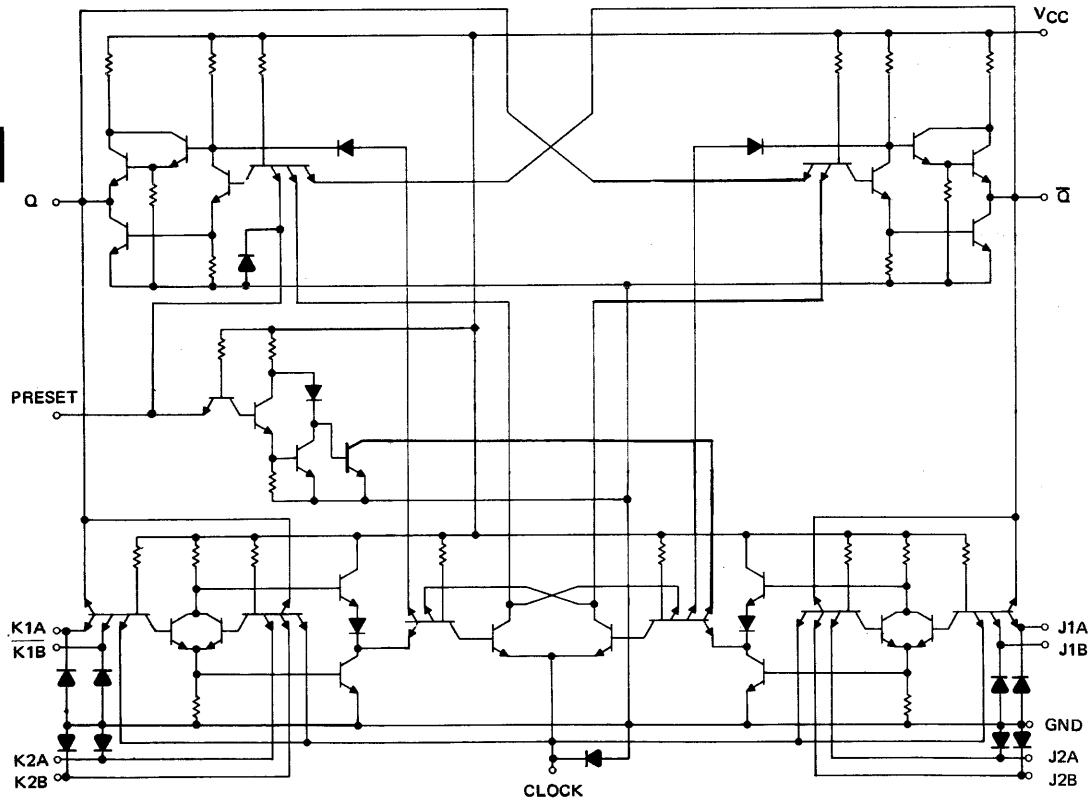
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clock}	Maximum input clock frequency	77	C_L = 25 pF, R_L = 280 Ω	40	50		MHz
t_{pd1}	Propagation delay time to logical 1 level from preset to output	78	C_L = 25 pF, R_L = 280 Ω		8	12	ns
t_{pd0}	Propagation delay time to logical 0 level from preset to output (clock low)	78	C_L = 25 pF, R_L = 280 Ω		23	35	ns
t_{pd0}	Propagation delay time to logical 0 level from preset to output (clock high)	78	C_L = 25 pF, R_L = 280 Ω		15	20	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	77	C_L = 25 pF, R_L = 280 Ω	5	10	15	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	77	C_L = 25 pF, R_L = 280 Ω	8	16	20	ns

CIRCUIT TYPES SN54H101, SN74H101
J-K EDGE-TRIGGERED FLIP-FLOPS

functional block diagram



schematic



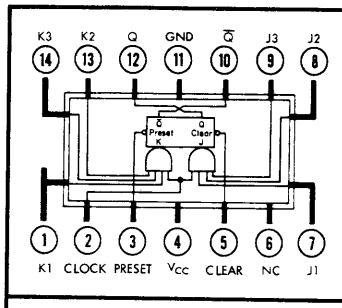
7

logic

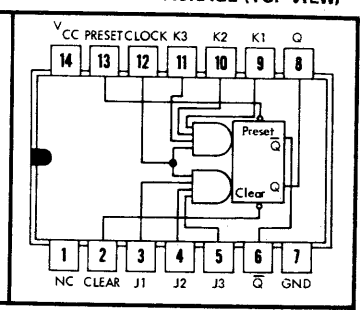
TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES: 1. J = J1 • J2 • J3
2. K = K1 • K2 • K3
3. t_n = Bit time before clock pulse
4. t_{n+1} = Bit time after clock pulse
5. NC—No Internal Connection

W
FLAT PACKAGE (TOP VIEW)



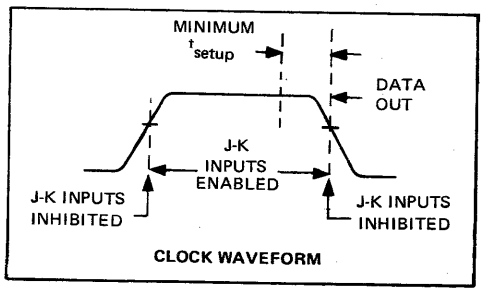
J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Preset and clear are independent of clock

description

These monolithic J-K flip-flops are negative edge-triggered. They feature gated J-K inputs and an asynchronous clear input. The AND gate inputs are inhibited while the clock input is low; when the clock goes high, the inputs are enabled and data will be accepted. Logical state of J and K inputs may be allowed to change when the clock pulse is in a high state and bistable will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative edge of the clock pulse.



CLOCK WAVEFORM

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H102 Circuits	4.5	5	5.5	V
SN74H102 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A: SN54H102 Circuits	−55	25	125	°C
SN74H102 Circuits	0	25	70	°C
Normalized Fan-Out From Each Output, N			10	
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 77)	10			ns
Width of Preset Pulse, $t_{p(preset)}$ (See Figure 78)	15			ns
Width of Clear Pulse, $t_{p(clear)}$ (See Figure 78)	15			ns
Input Setup Time, t_{setup} (See Above): Logical 1	10			ns
Logical 0	13			ns
Input Hold Time, t_{hold}	0			ns
Clock Pulse Transition Time, t_0 (See Figure 77)			150	ns

7

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP§	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	59 and 60		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	59 and 60				0.8	V
$V_{out(1)}$	Logical 1 output voltage	59	V_{CC} = MIN, I_{load} = −500 μA	2.4	3.2		V
$V_{out(0)}$	Logical 0 output voltage	60	V_{CC} = MIN, I_{sink} = 20 mA		0.25	0.4	V
$I_{in(0)}$	Logical 0 level input current at J1, J2, J3, K1, K2, K3, preset, or clear	61	V_{CC} = MAX, V_{in} = 0.4 V		−1	−2	mA
$I_{in(0)}$	Logical 0 level input current clock	61	V_{CC} = MAX, V_{in} = 0.4 V		−3	−4.8	mA
$I_{in(1)}$	Logical 1 level input current at J1, J2, J3, K1, K2, or K3	62	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at clock	62	V_{CC} = MAX, V_{in} = 2.4 V	0		−1	mA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at preset or clear	62	V_{CC} = MAX, V_{in} = 2.4 V			100	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current‡	63	V_{CC} = MAX, V_{in} = 0	−40		−100	mA
I_{CC}	Supply current	62	V_{CC} = MAX		20	38	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

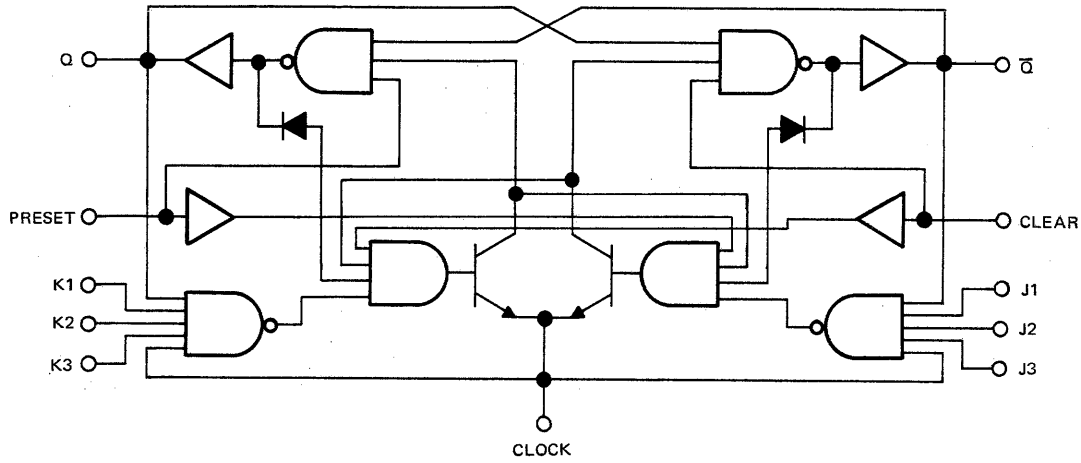
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

7

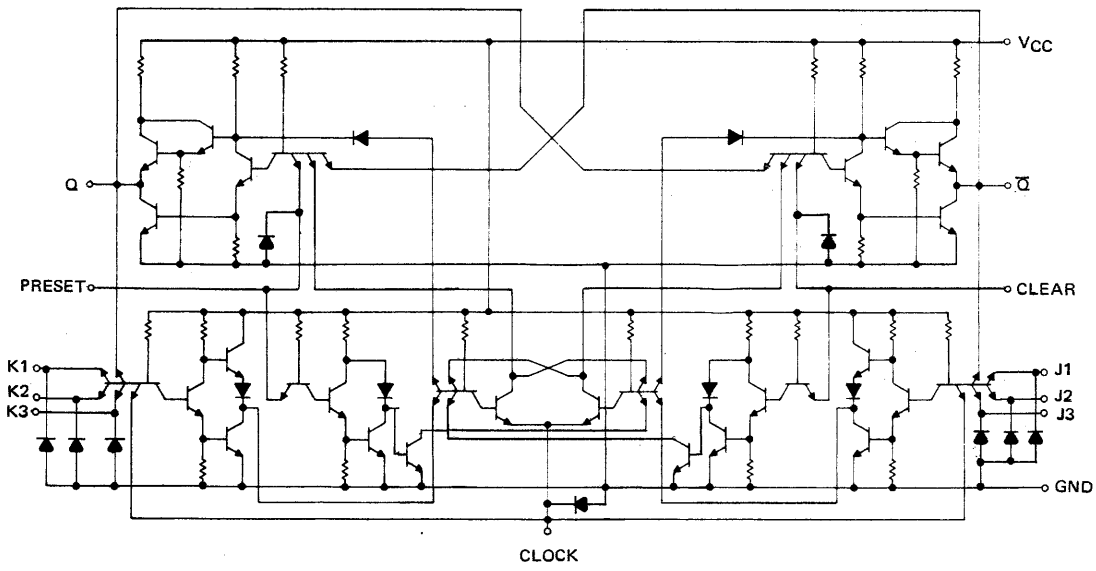
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clock}	Maximum input clock frequency	77	C_L = 25 pF, R_L = 280 Ω	40	50		MHz
t_{pd1}	Propagation delay time to logical 1 level from preset to output	78	C_L = 25 pF, R_L = 280 Ω		8	12	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output (clock low)	78	C_L = 25 pF, R_L = 280 Ω		23	35	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output (clock high)	78	C_L = 25 pF, R_L = 280 Ω		15	20	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	77	C_L = 25 pF, R_L = 280 Ω	5	10	15	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	77	C_L = 25 pF, R_L = 280 Ω	8	16	20	ns

functional block diagram



schematic



7

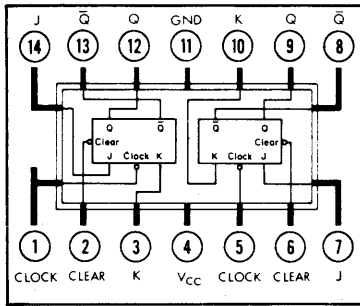
CIRCUIT TYPES SN54H103, SN74H103
DUAL J-K EDGE-TRIGGERED FLIP-FLOPS

logic

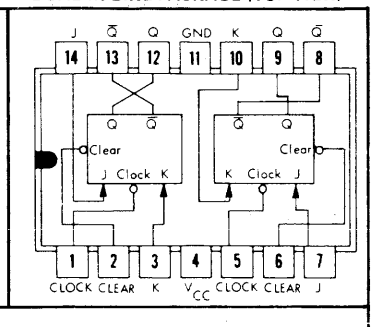
TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

NOTES: 1. t_n = Bit time before clock pulse
2. t_{n+1} = Bit time after clock pulse

W
FLAT PACKAGE (TOP VIEW)



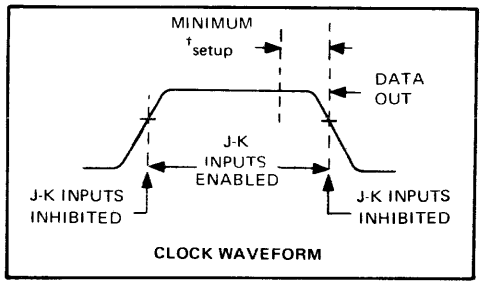
J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: Low input to clear sets Q to logical 0
Clear is independent of clock

description

These dual monolithic J-K flip-flops are negative-edge-triggered. They feature individual J, K, clock, and asynchronous clear inputs to each flip-flop. When the clock goes high, the inputs are enabled and data will be accepted. Logical state of J and K inputs may be allowed to change when the clock pulse is in a high state and bistable will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative edge of the clock pulse.



CLOCK WAVEFORM

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H103 Circuits	4.5	5	5.5	V
SN74H103 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A: SN54H103 Circuits	−55	25	125	°C
SN74H103 Circuits	0	25	70	°C
Normalized Fan-Out From Each Output, N			10	
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 77)	10			ns
Width of Clear Pulse, $t_{p(clear)}$ (See Figure 78)	16			ns
Input Setup Time, t_{setup} (See Figure 79): Logical 1	10			ns
Logical 0	13			ns
Input Hold Time, t_{hold}	0			ns
Clock Pulse Transition Time, t_0 (See Figure 77)			150	ns

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP§	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	64 and 65		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	64 and 65				0.8	V
$V_{out(1)}$	Logical 1 output voltage	64	V_{CC} = MIN, I_{load} = −500 μA	2.4	3.2		V
$V_{out(0)}$	Logical 0 output voltage	65	V_{CC} = MIN, I_{sink} = 20 mA		0.25	0.4	V
$I_{in(0)}$	Logical 0 level input current at J, K, or clear	66	V_{CC} = MAX, V_{in} = 0.4 V		−1	−2	mA
$I_{in(0)}$	Logical 0 level input current at clock	66	V_{CC} = MAX, V_{in} = 0.4 V		−3	−4.8	mA
$I_{in(1)}$	Logical 1 level input current at J or K	67	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at clock	67	V_{CC} = MAX, V_{in} = 2.4 V	0		−1	mA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at clear	67	V_{CC} = MAX, V_{in} = 2.4 V			100	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current‡	68	V_{CC} = MAX, V_{in} = 0	−40		−100	mA
I_{CC}	Supply current	67	V_{CC} = MAX		40	76	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

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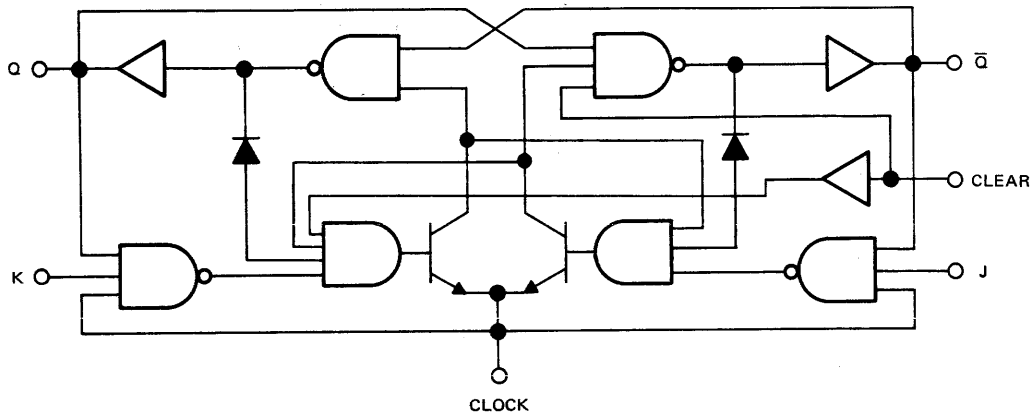
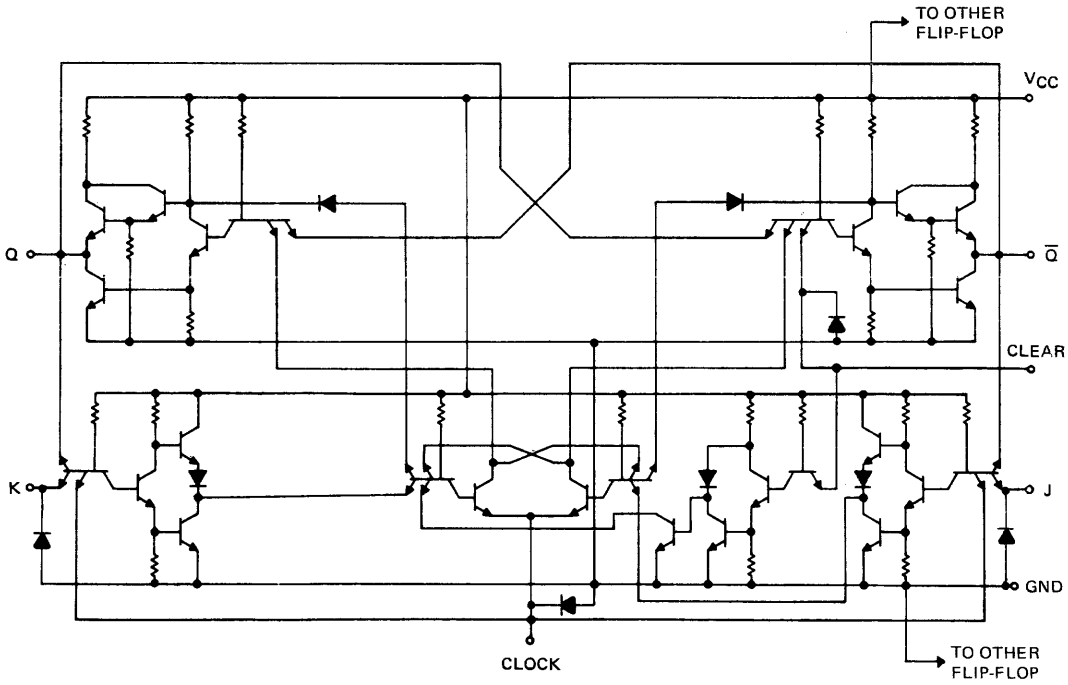
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clock}	Maximum input clock frequency	77	C_L = 25 pF, R_L = 280 Ω	40	50		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear to output	78	C_L = 25 pF, R_L = 280 Ω		8	12	ns
t_{pd0}	Propagation delay time to logical 0 level from clear to output (Clock low)	78	C_L = 25 pF, R_L = 280 Ω		23	35	ns
t_{pd0}	Propagation delay time to logical 0 level from clear to output (clock high)	78	C_L = 25 pF, R_L = 280 Ω		15	20	ns
t_{pd1}	Propagation delay time to locical 1 level from clock to output	77	C_L = 25 pF, R_L = 280 Ω	5	10	15	ns
t_{pd0}	Propagation delay time to locical 0 level from clock to output	77	C_L = 25 pF, R_L = 280 Ω	8	16	20	ns

functional block diagram (each flip-flop)



schematic (each flip-flop)

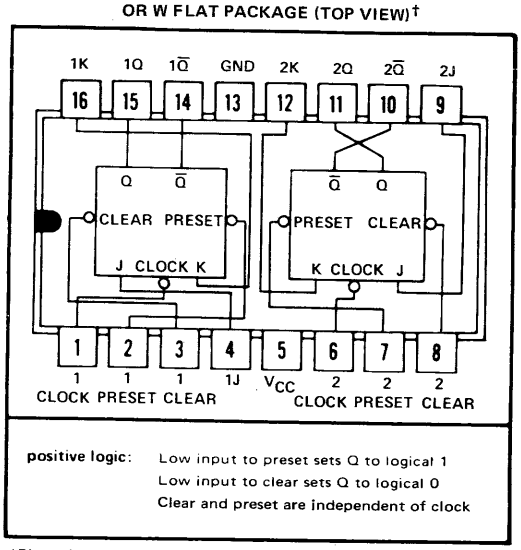


logic

TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

NOTES: 1. t_n = Bit time before clock pulse
2. t_{n+1} = Bit time after clock pulse

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†

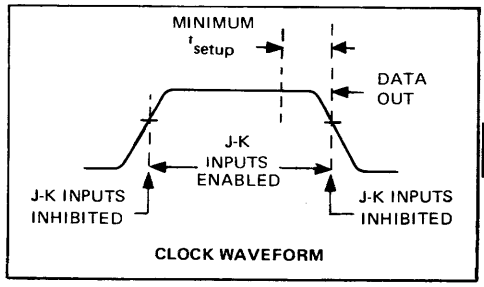


positive logic: Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Clear and preset are independent of clock

†Pin assignments for these circuits are the same for all packages.

description

These dual monolithic J-K flip-flops are negative-edge-triggered. They feature individual J, K, clock, and asynchronous preset and clear inputs to each flip-flop. When the clock goes high, the inputs are enabled and data will be accepted. Logical state of J and K inputs may be allowed to change when the clock pulse is in a high state and bistable will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative edge of the clock pulse.



CLOCK WAVEFORM

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	SN54H106 Circuits	4.5	5	5.5	V
	SN74H106 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A:	SN54H106 Circuits	−55	25	125	°C
	SN74H106 Circuits	0	25	70	°C
Normalized Fan-Out From Each Output, N				10	
Width of Clock Pulse, $t_{p(clock)}$	(See Figure 77)	10			ns
Width of Preset Pulse, $t_{p(preset)}$	(See Figure 78)	16			ns
Width of Clear Pulse, $t_{p(clear)}$	(See Figure 78)	16			ns
Input Setup Time, t_{setup}	(See Above): Logical 1	10			ns
	Logical 0	13			ns
Input Hold Time, t_{hold}		0			ns
Clock Pulse Transition Time, t_0	(See Figure 77)			150	ns

7

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP§	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	64 and 65		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	64 and 65				0.8	V
$V_{out(1)}$	Logical 1 output voltage	64	V_{CC} = MIN, I_{load} = −500 μA	2.4	3.2		V
$V_{out(0)}$	Logical 0 output voltage	65	V_{CC} = MIN, I_{sink} = 20 mA		0.25	0.4	V
$I_{in(0)}$	Logical 0 level input current at J, K, preset, or clear	66	V_{CC} = MAX, V_{in} = 0.4 V		−1	−2	mA
$I_{in(0)}$	Logical 0 level input current at clock	66	V_{CC} = MAX, V_{in} = 0.4 V		−3	−4.8	mA
$I_{in(1)}$	Logical 1 level input current at J or K	67	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at preset or clear	67	V_{CC} = MAX, V_{in} = 2.4 V			100	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at clock	67	V_{CC} = MAX, V_{in} = 2.4 V	0		−1	mA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current‡	69	V_{CC} = MAX, V_{in} = 0	−40		−100	mA
I_{CC}	Supply current	67	V_{CC} = MAX		40	76	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

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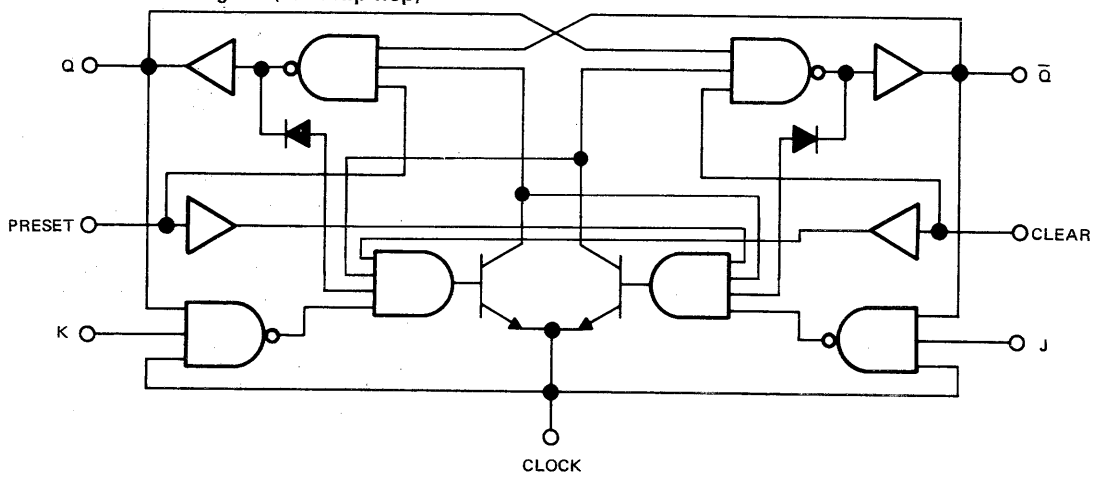
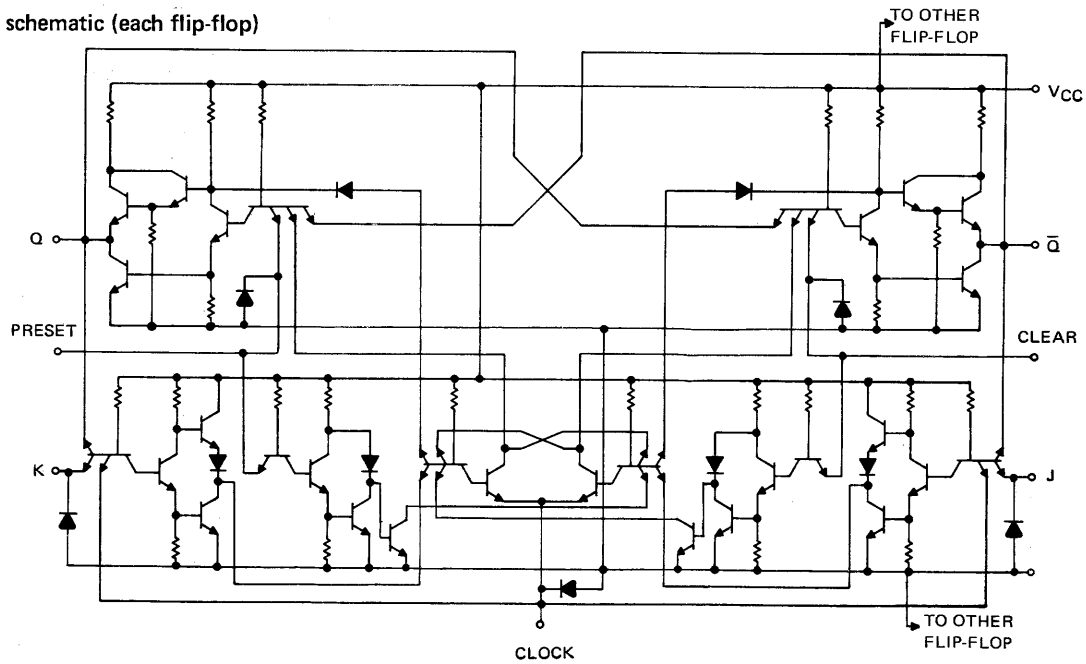
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clock}	Maximum input clock frequency	77	C_L = 25 pF, R_L = 280 Ω	40	50		MHz
t_{pd1}	Propagation delay time to logical 1 level from preset or clear to output	78	C_L = 25 pF, R_L = 280 Ω		8	12	ns
t_{pd0}	Propagation delay time to logical 0 level from preset or clear to output (clock low)	78	C_L = 25 pF, R_L = 280 Ω		23	35	ns
t_{pd0}	Propagation delay time to logical 0 level from preset or clear to output (clock high)	78	C_L = 25 pF, R_L = 280 Ω		15	20	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	77	C_L = 25 pF, R_L = 280 Ω	5	10	15	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	77	C_L = 25 pF, R_L = 280 Ω	8	16	20	ns

functional block diagram (each flip-flop)



schematic (each flip-flop)



7

CIRCUIT TYPES SN54H108, SN74H108
DUAL J-K EDGE-TRIGGERED FLIP-FLOPS

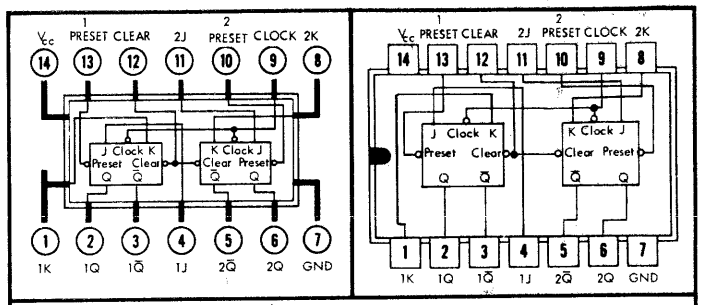
logic

TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

NOTES: 1. t_n = Bit time before clock pulse
2. t_{n+1} = Bit time after clock pulse

W
FLAT PACKAGE (TOP VIEW)

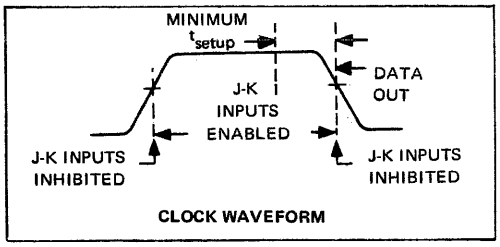
J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Preset and clear are independent of clock

description

These dual monolithic J-K flip-flops are negative-edge-triggered. They feature individual J, K, and asynchronous preset inputs to each flip-flop as well as common clock and asynchronous clear inputs. When the clock goes high, the inputs are enabled and data will be accepted. Logical state of J and K inputs may be allowed to change when the clock pulse is in a high state and bistable will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative edge of the clock pulse.



CLOCK WAVEFORM

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H108 Circuits	4.5	5	5.5	V
SN74H108 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A: SN54H108 Circuits	−55	25	125	°C
SN74H108 Circuits	0	25	70	°C
Normalized Fan-Out From Each Output, N			10	
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 77)	10			ns
Width of Preset Pulse, $t_{p(preset)}$ (See Figure 78)	15			ns
Width of Clear Pulse, $t_{p(clear)}$ (See Figure 78)	16			ns
Input Setup Time, t_{setup} (See above): Logical 1	10			ns
Logical 0	13			ns
Input Hold Time, t_{hold}	0			ns
Clock Pulse Transition Time, t_0 (See Figure 77)			150	ns

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP§	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	64 and 65		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	64 and 65				0.8	V
$V_{out(1)}$	Logical 1 output voltage	64	V_{CC} = MIN, I_{load} = −500 μA	2.4	3.2		V
$V_{out(0)}$	Logical 0 output voltage	65	V_{CC} = MIN, I_{sink} = 20 mA		0.25	0.4	V
$I_{in(0)}$	Logical 0 level input current at J, K, or preset	66	V_{CC} = MAX, V_{in} = 0.4 V		−1	−2	mA
$I_{in(0)}$	Logical 0 level input current at clock	66	V_{CC} = MAX, V_{in} = 0.4 V		−6	−9.6	mA
$I_{in(0)}$	Logical 0 level input current at clear	66	V_{CC} = MAX, V_{in} = 0.4 V		−2	−4	mA
$I_{in(1)}$	Logical 1 level input current at J or K	67	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at clock	67	V_{CC} = MAX, V_{in} = 2.4 V	0		−1	mA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at preset	67	V_{CC} = MAX, V_{in} = 2.4 V			100	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at clear	67	V_{CC} = MAX, V_{in} = 2.4 V			200	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current‡	69	V_{CC} = MAX, V_{in} = 0	−40		−100	mA
I_{CC}	Supply current	67	V_{CC} = MAX		40	76	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

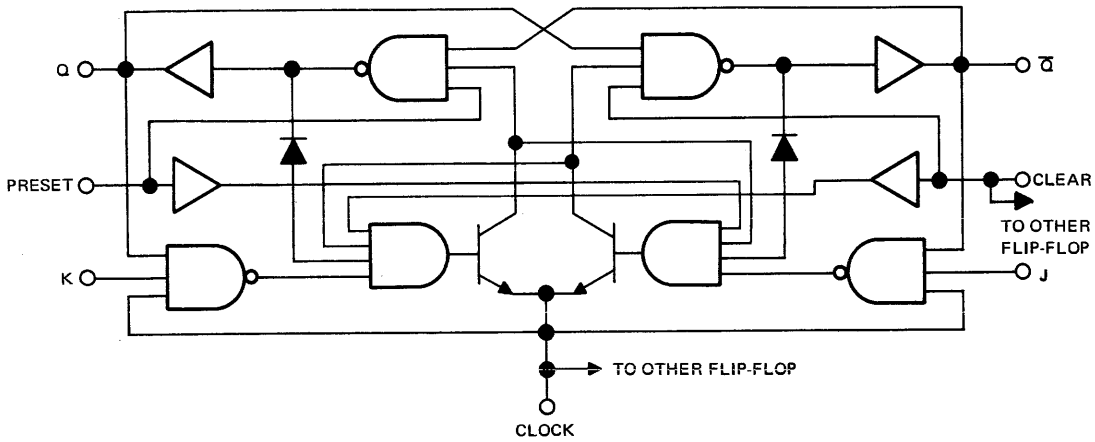
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

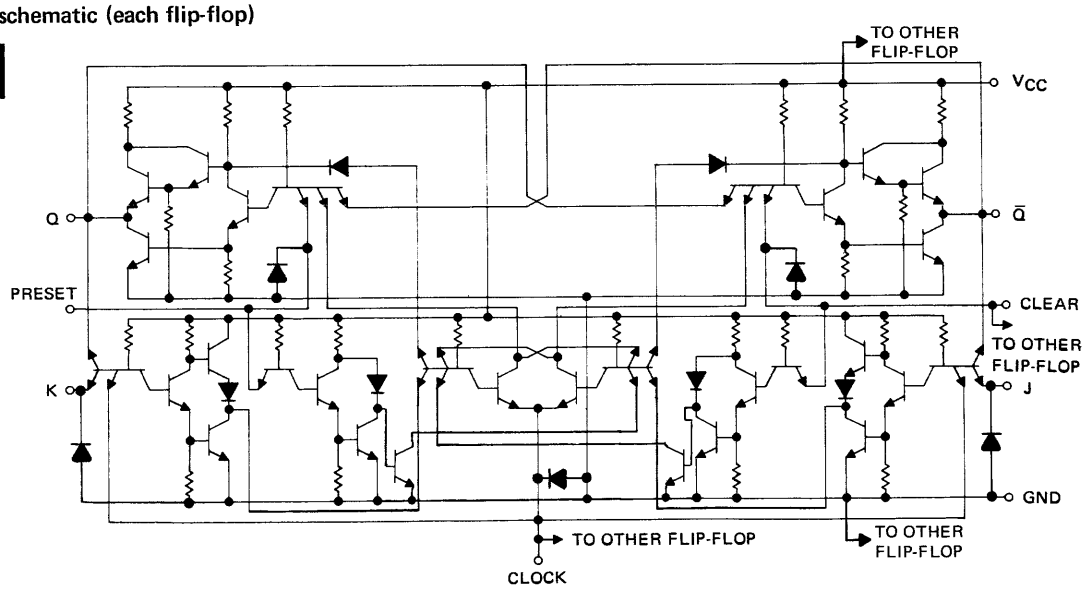
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clock}	Maximum input clock frequency	77	C_L = 25 pF, R_L = 280 Ω	40	50		MHz
t_{pd1}	Propagation delay time to logical 1 level from preset or clear to output	78	C_L = 25 pF, R_L = 280 Ω		8	12	ns
t_{pd0}	Propagation delay time to logical 0 level from preset or clear to output output (clock low)	78	C_L = 25 pF, R_L = 280 Ω		23	35	ns
t_{pd0}	Propagation delay time to logical 0 level from preset or clear to output output (clock high)	78	C_L = 25 pF, R_L = 280 Ω		15	20	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	77	C_L = 25 pF, R_L = 280 Ω	5	10	15	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	77	C_L = 25 pF, R_L = 280 Ω	8	16	20	ns

7

functional block diagram (each flip-flop)

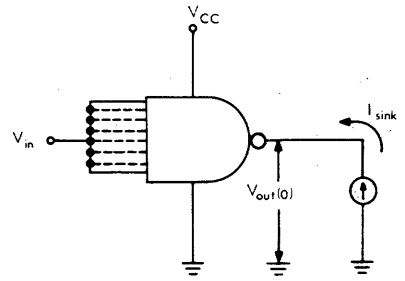


schematic (each flip-flop)



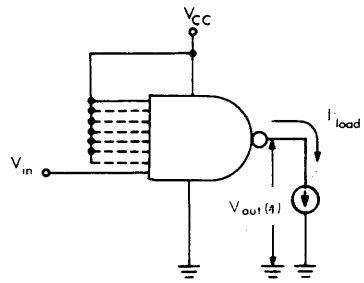
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§



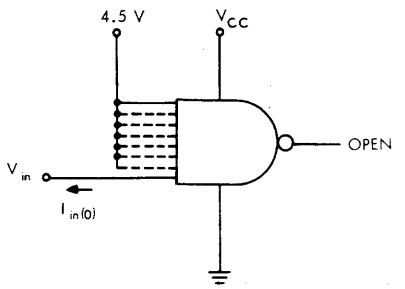
1. All inputs are tested simultaneously.

FIGURE 1



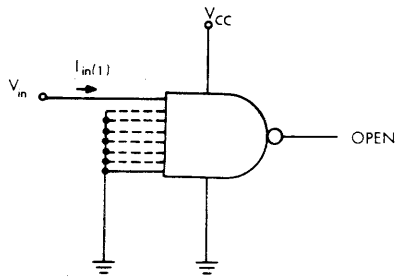
1. Each input is tested separately.

FIGURE 2



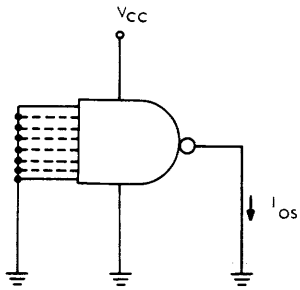
1. Each input is tested separately.

FIGURE 3



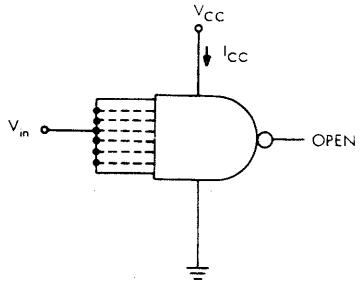
1. Each input is tested separately.

FIGURE 4



1. Each gate is tested separately.

FIGURE 5



1. Logical 0 and logical 1 conditions are tested.
2. All gates are tested simultaneously.

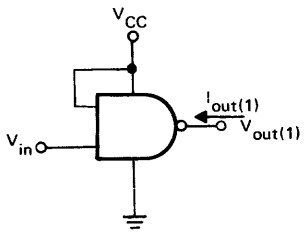
FIGURE 6

§Arrows indicate actual direction of current flow.

7

PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



1. Each input is tested separately.

FIGURE 7

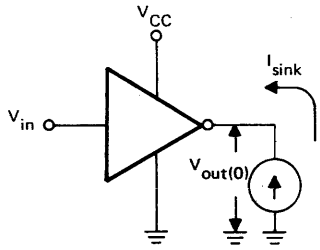


FIGURE 8

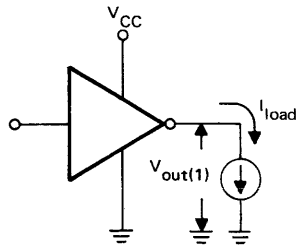


FIGURE 9

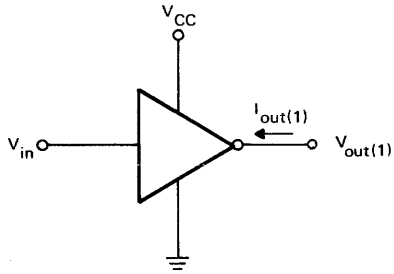


FIGURE 10

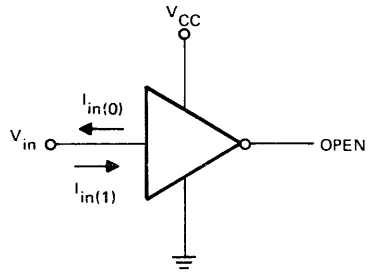
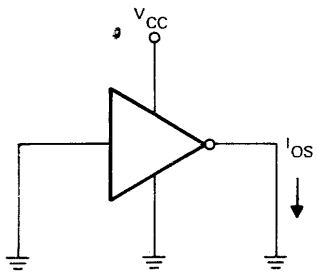
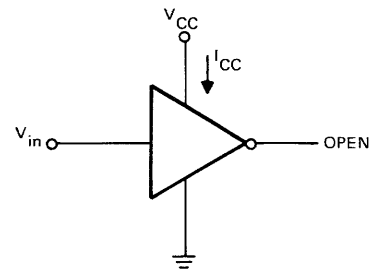


FIGURE 11



1. Each inverter is tested separately.

FIGURE 12



1. All inverters are tested simultaneously.

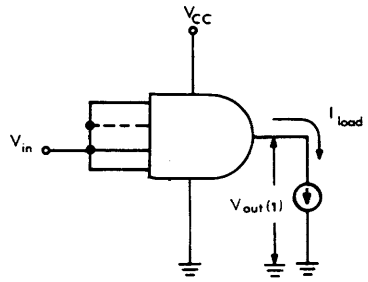
FIGURE 13

§Arrows indicate actual direction of current flow.

7

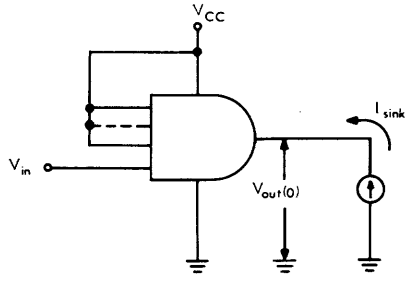
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



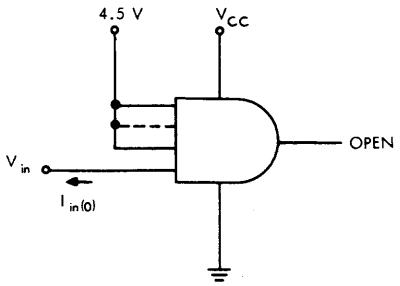
1. All inputs are tested simultaneously.

FIGURE 14



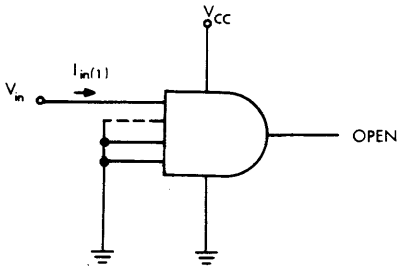
1. Each input is tested separately.

FIGURE 15



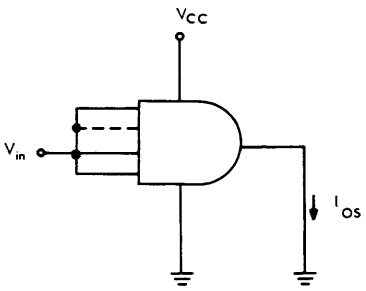
1. Each input is tested separately.

FIGURE 16



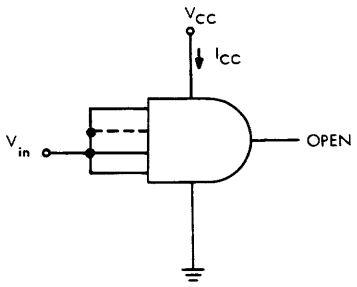
1. Each input is tested separately.

FIGURE 17



1. Each gate is tested separately.

FIGURE 18



1. Logical 0 and logical 1 conditions are tested.
2. All gates are tested simultaneously.

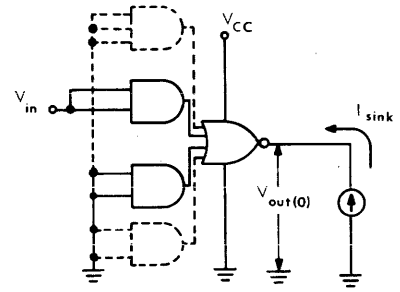
FIGURE 19

§Arrows indicate actual direction of current flow.

7

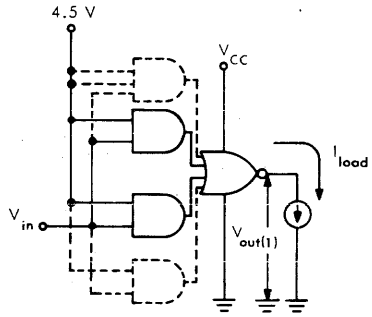
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



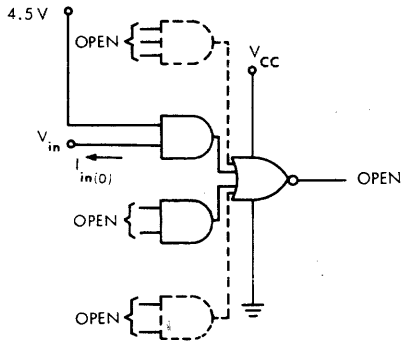
1. Each AND section is tested separately.

FIGURE 20



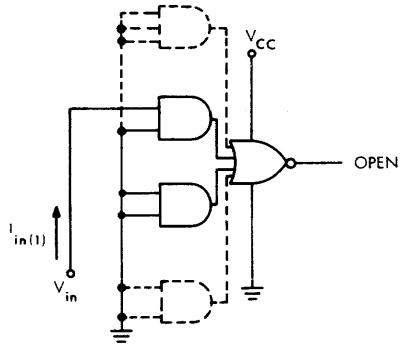
1. Each set of inputs is tested separately.

FIGURE 21



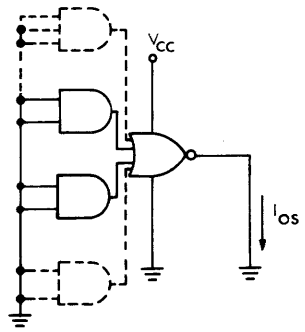
1. Each input is tested separately.

FIGURE 22



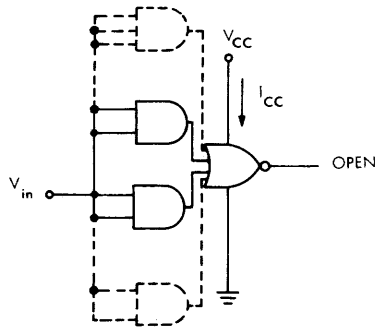
1. Each input is tested separately.

FIGURE 23



1. Each gate is tested separately.

FIGURE 24.



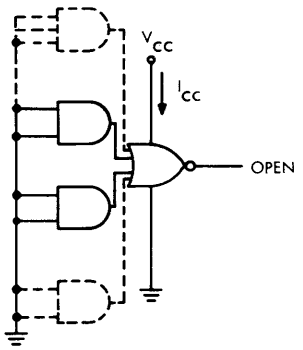
1. All gates are tested simultaneously

FIGURE 25

§Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



1. All gates are tested simultaneously.

FIGURE 26

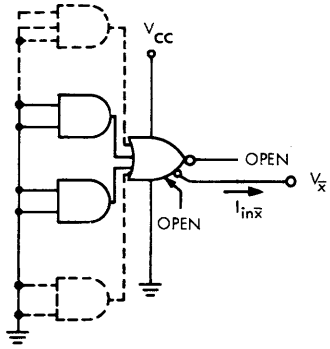


FIGURE 27

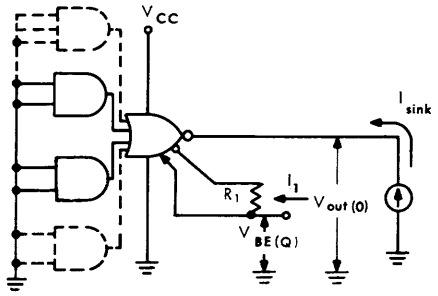


FIGURE 28

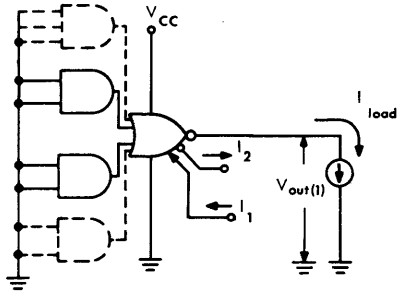
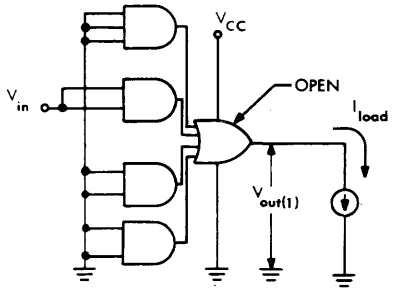
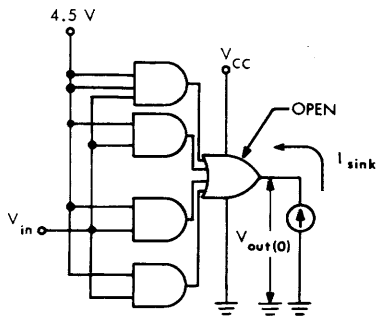


FIGURE 29



1. Each AND section is tested separately.

FIGURE 30



1. Each set of inputs is tested separately.

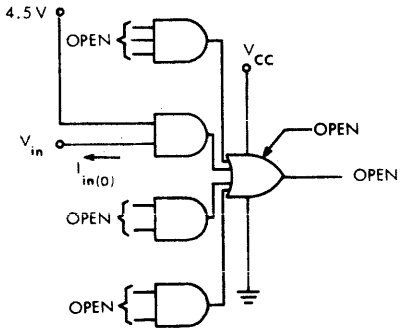
FIGURE 31

§Arrows indicate actual direction of current flow.

7

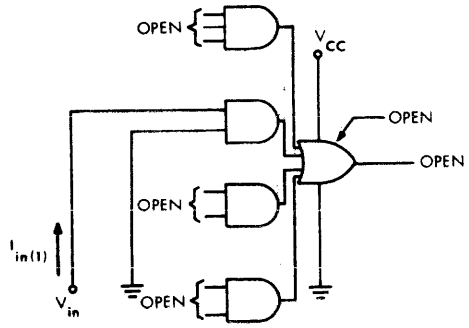
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



1. Each input of each AND section is tested separately.

FIGURE 32



1. Each input of each AND section is tested separately.

FIGURE 33

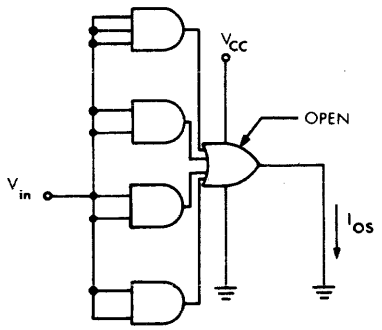
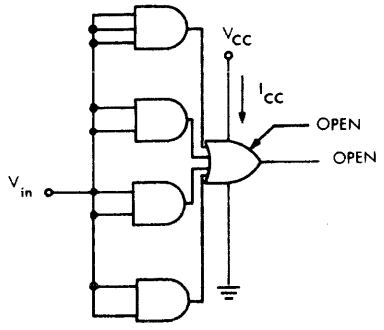


FIGURE 34



1. Logical 0 and logical 1 conditions are tested.

FIGURE 35

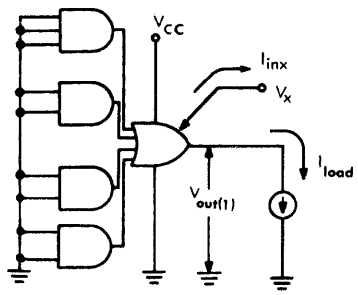


FIGURE 36

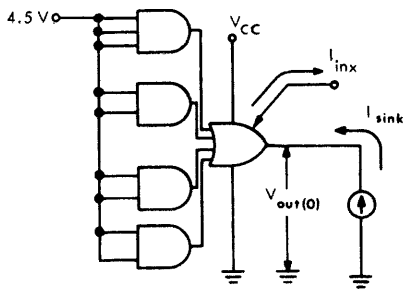
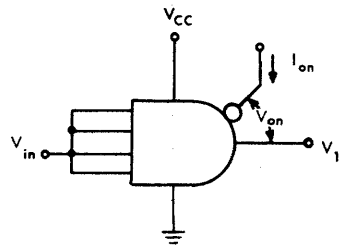


FIGURE 37

§Arrows indicate actual direction of current flow.

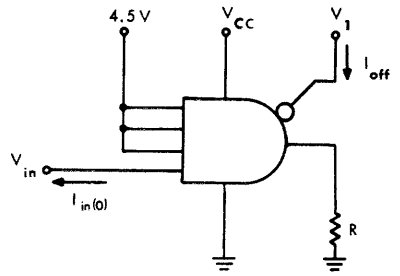
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



1. All inputs are tested simultaneously.

FIGURE 38



1. Each input is tested separately.

FIGURE 39

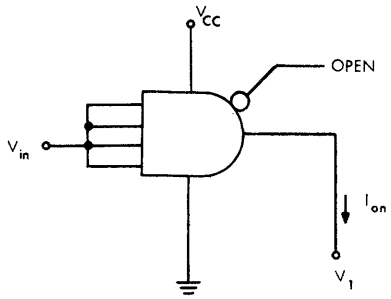
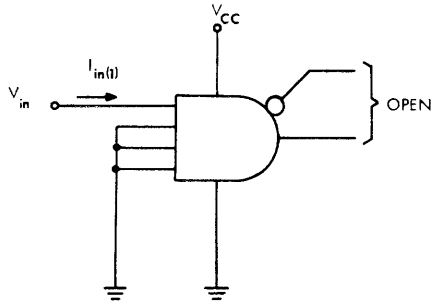
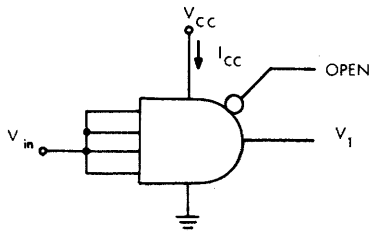


FIGURE 40



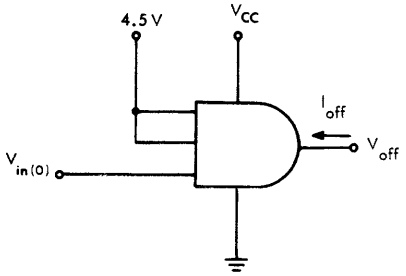
1. Each input is tested separately.

FIGURE 41



1. On and off conditions are tested separately.
2. All gates are tested simultaneously.

FIGURE 42



1. Each input is tested separately.

FIGURE 43

§Arrows indicate actual direction of current flow.

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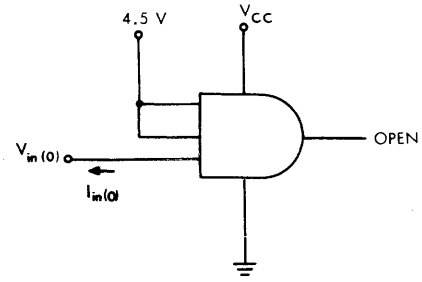
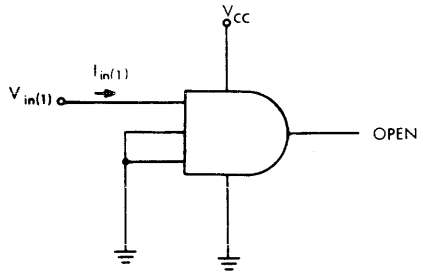
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



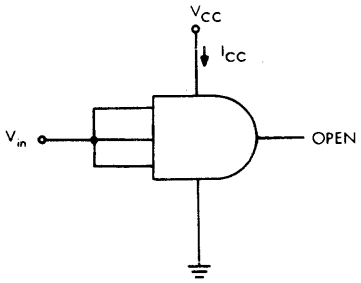
1. Each input is tested separately.

FIGURE 44



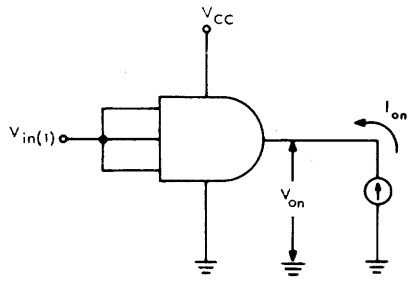
1. Each input is tested separately.

FIGURE 45



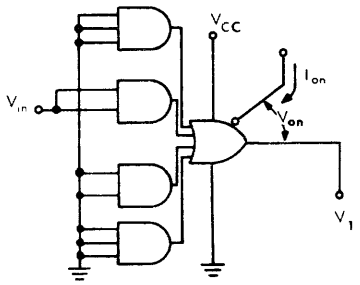
1. On and off conditions are tested separately.
2. All gates are tested simultaneously.

FIGURE 46



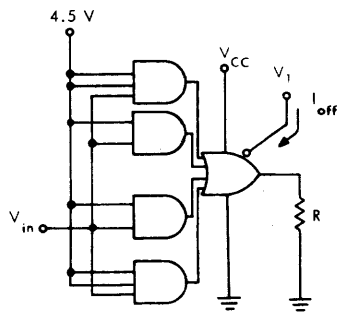
1. All inputs are tested simultaneously.

FIGURE 47



1. Each AND section is tested separately.

FIGURE 48



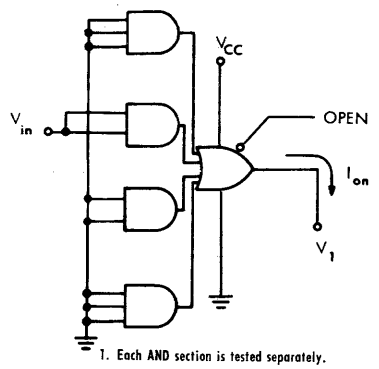
1. Each set of inputs is tested separately.

FIGURE 49

§Arrows indicate actual direction of current flow.

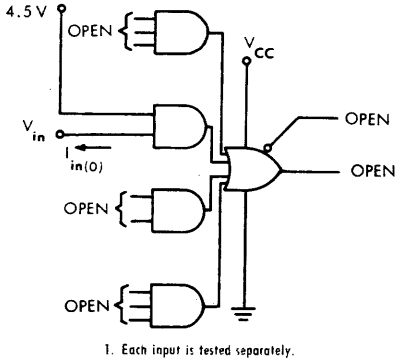
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



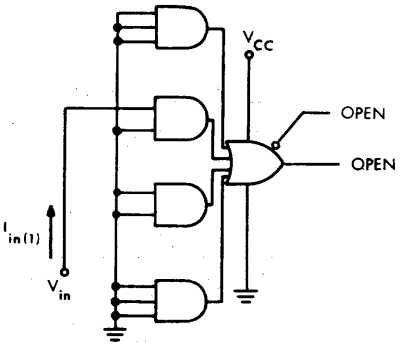
1. Each AND section is tested separately.

FIGURE 50



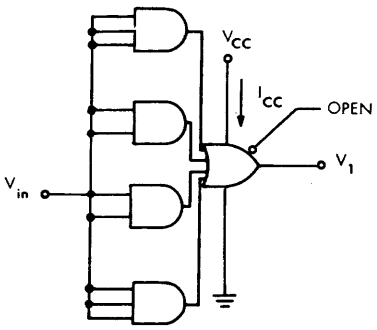
1. Each input is tested separately.

FIGURE 51



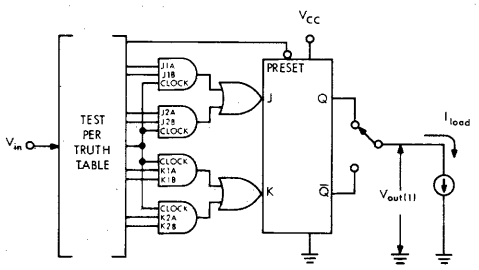
1. Each input is tested separately.

FIGURE 52



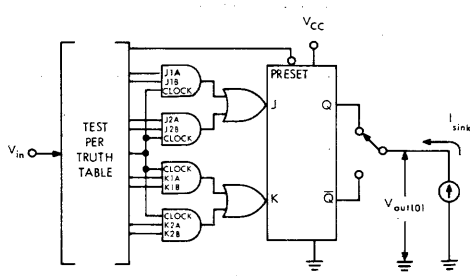
1. On and off conditions are tested separately.

FIGURE 53



1. Each output is tested separately.

FIGURE 54



1. Each output is tested separately.

FIGURE 55

§Arrows indicate actual direction of current flow.

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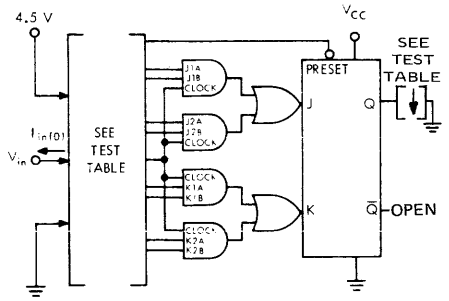
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



1. Each input is tested separately.

TEST TABLES†

SN54H71, SN74H71

Apply V_{in} (Test $I_{in(0)}$)	Apply 4.5 V	Apply Momentary GND then 4.5 V	GND
Clock	J1A, J1B, J2A, J2B, K1A, K1B, K2A, and K2B	Preset	None
Clock¶	J1A, J1B, J2A, J2B, K1A, K1B, K2A, K2B, and Preset	None	Q
Preset	J1A, J1B, J2A, J2B, K1A, K1B, K2A, K2B, and Clock	None	None
J1A¶	J1B and Clock	None	Q
J1B¶	J1A and Clock	None	Q
J2A¶	J2B and Clock	None	Q
J2B¶	J2A and Clock	None	Q
K1A	K1B and Clock	Preset	None
K1B	K1A and Clock	Preset	None
K2A	K2B and Clock	Preset	None
K2B	K2A and Clock	Preset	None

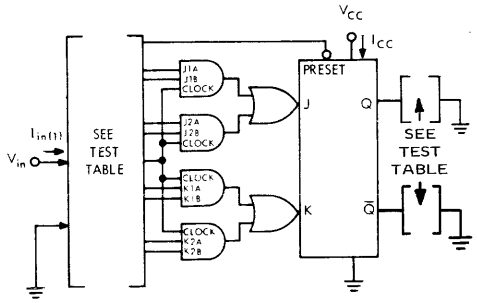
†Inputs and outputs not specified are open.
¶Duration of this test should not exceed 1 second.

SN54H101, SN74H101

Apply V_{in} (Test $I_{in(0)}$)	Apply 4.5 V	Ground
Clock	J1A, J1B, J2A, J2B, K1A, K1B, K2A, K2B	Preset
Preset	J1A, J1B, J2A, J2B, K1A, K1B, K2A, K2B, Clock	None
J1A¶	J1B, J2A, J2B, K1A, K1B, K2A, K2B, Clock, Preset	Q
J1B¶	J1A, J2A, J2B, K1A, K1B, K2A, K2B, Clock, Preset	Q
J2A¶	J1A, J1B, J2B, K1A, K1B, K2A, K2B, Clock, Preset	Q
J2B¶	J1A, J1B, J2A, K1A, K1B, K2A, K2B, Clock, Preset	Q
K1A	J1A, J1B, J2A, J2B, K1B, K2A, K2B, Clock	Preset
K1B	J1A, J1B, J2A, J2B, K1A, K2A, K2B, Clock	Preset
K2A	J1A, J1B, J2A, J2B, K1A, K1B, K2B, Clock	Preset
K2B	J1A, J1B, J2A, J2B, K1A, K1B, K2A, Clock	Preset

†Inputs and outputs not specified are open.
¶Duration of this test should not exceed 1 second.

FIGURE 56



1. Each input is tested separately.
2. I_{CC} is measured for each of the following conditions:
   a. J1A = J1B = J2A = J2B = K1A = K1B = K2A = K2B = Preset = 4.5 V, and Clock = momentary 4.5 V, then Gnd.

TEST TABLES†

SN54H71, SN74H71

Apply V_{in} (Test $I_{in(1)}$)	Ground
Clock	J1A, J1B, J2A, J2B, K1A, K1B, K2A, K2B, and Preset
Clock¶	J1A, J1B, J2A, J2B, K1A, K1B, K2A, K2B, Preset, and Q
Preset	K1A, K1B, K2A K2B, Clock, and Q
J1A	J1B, Clock, and Preset
J1B	J1A, Clock, and Preset
J2A	J2B, Clock, and Preset
J2B	J2A, Clock, and Preset
K1A¶	K1B, Clock, Preset, and Q
K1B¶	K1A, Clock, Preset, and Q
K2A¶	K2B, Clock, Preset, and Q
K2B¶	K2A, Clock, Preset, and Q

†Inputs and outputs not specified are open.
¶Duration of this test should not exceed one second.

SN54H101, SN74H101

Apply V_{in} (Test $I_{in(1)}$)	Ground	Apply 4.5 V
Clock	J1A, J1B, J2A, J2B, K1A, K1B, K2A, K2B, Preset	None
Preset¶	J1A, J1B, J2A, J2B, K1A, K1B, K2A, K2B, Q	Clock
J1A,	J1B, J2A, J2B, Preset, Clock	K1A, K1B, K2A, K2B
J1B	J1A, J2A, J2B, Preset, Clock	K1A, K1B, K2A, K2B
J2A	J1A, J1B, J2B, Preset, Clock	K1A, K1B, K2A, K2B
J2B	J1A, J1B, J2A, Preset, Clock	K1A, K1B, K2A, K2B
K1A	K1B, K2A, K2B, Clock	Preset J1A, J1B, J2A, J2B
K1B	K1A, K2A, K2B, Clock	Preset J1A, J1B, J2A, J2B
K2A	K1A, K1B, K2B, Clock	Preset J1A, J1B, J2A, J2B
K2B	K1A, K1B, K2A, Clock	Preset J1A, J1B, J2A, J2B

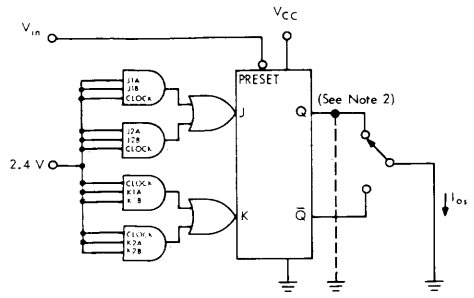
†Inputs and outputs not specified are open.
¶Duration of this test should not exceed 1 second.

FIGURE 57

§Arrows indicate actual direction of current flow.

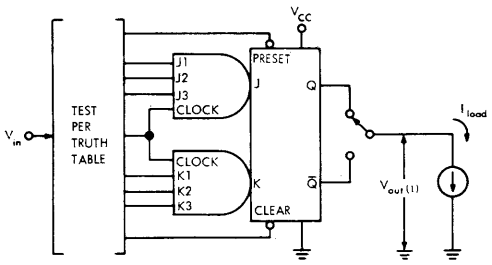
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



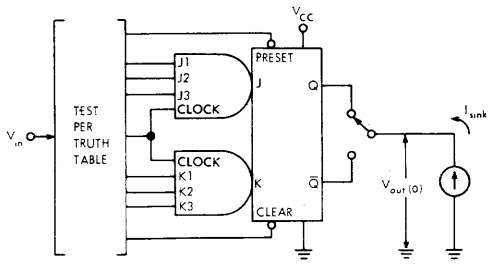
1. Each output is tested separately.
2. Test circuit shows setup for testing Q. When testing $\bar{Q}$, apply 2.4 V to Preset, ground Q, and limit duration of test to 100 ms.

FIGURE 58



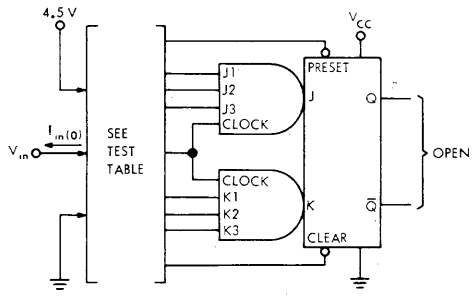
1. Each output is tested separately.

FIGURE 59



1. Each output is tested separately.

FIGURE 60



1. Each input is tested separately.

TEST TABLES

SN54H72, SN74H72

Apply V_{in} (Test $I_{in(0)}$)	Apply Momentary GND, then 4.5 V	Apply 4.5 V
Clock	Preset	J1, J2, J3, K1, K2, and K3
Clock	Clear	J1, J2, J3, K1, K2, and K3
Preset	None	J1, J2, J3, K1, K2, and K3
Clear	None	J1, J2, J3, K1, K2, and K3
J1	Clear	Clock, J2, and J3
J2	Clear	Clock, J1, and J3
J3	Clear	Clock, J1, and J2
K1	Preset	Clock, K2, and K3
K2	Preset	Clock, K1, and K3
K3	Preset	Clock, K1, and K2

SN54H102, SN74H102

Apply V_{in} (Test $I_{in(0)}$)	Apply 4.5 V	Ground
Clock	J1, J2, J3, K1, K2, K3, Clear	Preset
Clock	J1, J2, J3, K1, K2, K3, Preset	Clear
Preset	J1, J2, J3, K1, K2, K3, Clock, Clear	None
Clear	J1, J2, J3, K1, K2, K3, Clock, Preset	None
J1	J2, J3, K1, K2, K3, Clock, Preset	Clear
J2	J1, J3, K1, K2, K3, Clock, Preset	Clear
J3	J1, J2, K1, K2, K3, Clock, Preset	Clear
K1	J1, J2, J3, K2, K3, Clock, Clear	Preset
K2	J1, J2, J3, K1, K3, Clock, Clear	Preset
K3	J1, J2, J3, K1, K2, Clock, Clear	Preset

FIGURE 61

§ Arrows indicate actual direction of current flow.

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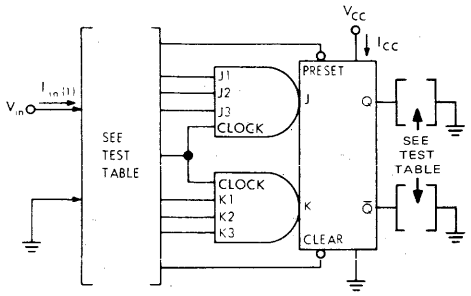
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



1. Each input is tested separately.
2. I_{CC} is measured for each of the following conditions:
   a. J1 = J2 = J3 = K1 = K2 = K3 = Clock = Preset = Gnd.
   b. J1 = J2 = J3 = K1 = K2 = K3 = Clock = Clear = Gnd.

TEST TABLES

SN54H72, SN74H72

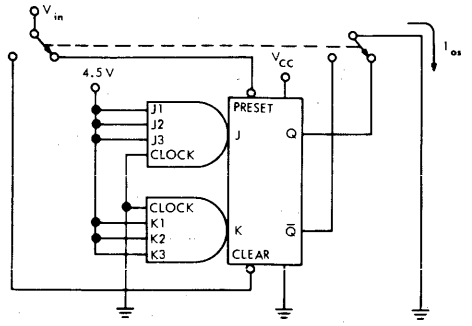
Apply V_{in} (Test $I_{in(1)}$)	Ground
Clock	Preset, Clear, J1, J2, J3, K1, K2, and K3
Preset	Clock, K1, K2,and K3
Clear	Clock,J1, J2, and J3
J1	Clock, Clear, J2,and J3
J2	Clock, Clear, J1, and J3
J3	Clock, Clear, J1, and J2
K1	Clock, Preset, K2, and K3
K2	Clock, Preset, K1, and K3
K3	Clock, Preset, K1, and K2

SN54H102, SN74H102

Apply V_{in} (Test $I_{in(1)}$)	Ground	4.5 V
Clock	J1, J2, J3, K1, K2, K3, Preset	Clear
Clock	J1, J2, J3, K1, K2, K3, Clear	Preset
Preset ¶	J1, J2, J3, K1, K2, K3, $\overline{Q}$	Clock, Clear
Clear ¶	J1, J2, J3, K1, K2, K3, Q	Clock, Preset
J1	J2, J3, Clock, Preset	K1, K2, K3, Clear
J2	J1, J3, Clock, Preset	K1, K2, K3, Clear
J3	J1, J2, Clock, Preset	K1, K2, K3, Clear
K1	K2, K3, Clock, Clear	J1, J2, J3, Preset
K2	K1, K3, Clock, Clear	J1, J2, J3, Preset
K3	K1, K2, Clock, Clear	J1, J2, J3, Preset

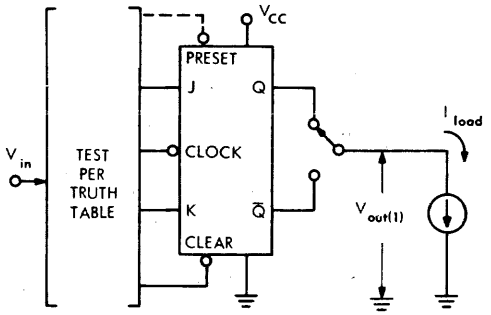
¶ Duration of this test should not exceed 1 second.

FIGURE 62



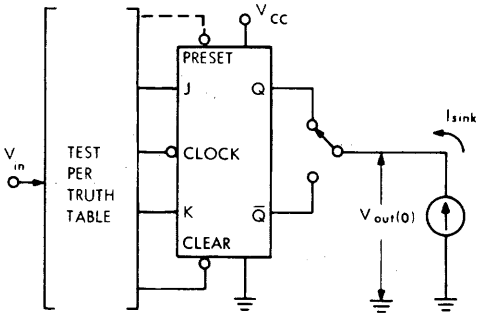
1. Each output is tested separately.

FIGURE 63



1. Each flip-flop is tested separately.
2. Each output is tested separately.
3. Preset is applicable for SN54H78/SN74H78 circuits only.

FIGURE 64



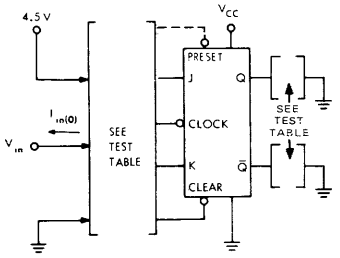
1. Each flip-flop is tested separately.
2. Each output is tested separately.
3. Preset is applicable for SN54H78/SN74H78 circuits only.

FIGURE 65

§ Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



TEST TABLES
SN54H73, SN74H73
SN54H76, SN74H76, SN54H78, SN74H78

Apply V_{in} (Test $I_{in(0)}$)	Apply Momentary GND	Apply 4.5 V
Clock	Clear (See Note 2)	J and K
Clear	None	Clock and J
Preset	None (See Note 5)	Clock and K
J	Q (See Note 3)	Clock and Clear
K	$\overline{Q}$ (See Note 3)	Clock and Clear

SN54H103, SN74H103

APPLY V_{in} TEST $I_{in(0)}$	APPLY GND	APPLY 4.5 V
Clock	Clear	J, K
Clear	None	Clock, J, K
J	Clear	Clock, K
K¶	$\overline{Q}$	Clock, Clear, J

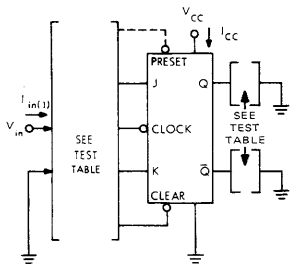
¶ Duration of this test should not exceed 1 second.

SN54H106, SN74H106
SN54H108, SN74H108

APPLY V_{in} TEST $I_{in(0)}$	APPLY GND	APPLY 4.5 V
Clock	Clear	J, K, Preset Note 6
Clock	Preset	J, K, Clear Note 6
Clear	None	Clock, Preset, J, K Note 6
Preset	None	Clock, Clear, J, K
J	Clear	Clock, K Preset
K	Preset	Clock, Clear, J

1. Each flip-flop is tested separately.
2. Apply momentary ground, then 4.5 V.
3. After application of momentary ground (< 1 second), Q and $\overline{Q}$ are left floating.
4. Ground all inputs of the unused flip-flop except where Note 6 is referenced.
5. Preset is not applicable for SN54H73 and SN74H73.
6. Apply the same conditions simultaneously to both flip-flops when testing the SN54H108 and SN74H108.

FIGURE 66



TEST TABLES
SN54H73, SN74H73
SN54H76, SN74H76, SN54H78, SN74H78

Apply V_{in} (Test $I_{in(1)}$)	Ground	Apply Momentary GND, then 4.5 V
Clock	Clear, J, and K	None
Clear	Clock and J	None
Preset (See Note 1)	Clock and K	None
J (See Note 1)	Clock and Clear	Preset
K (See Note 1)	Clock and Preset	Clear

SN54H103, SN74H103

APPLY V_{in} TEST $I_{in(1)}$	APPLY GND	APPLY 4.5 V
Clock	Clear, J, K	None
Clear¶	Q, J, K	Clock
J	Clock	Clear, K
K	Clock, Clear	J

SN54H106, SN74H106
SN54H108, SN74H108

APPLY V_{in} TEST $I_{in(1)}$	APPLY GND	APPLY 4.5 V
Clock	Clear, J, K	Preset, Note 4
Clock	Preset, J, K	Clear Note 4
Clear¶	Q, J, K	Preset, Clock Note 4
Preset¶	$\overline{Q}$, J, K	Clear, Clock
J	Clock, Preset	Clear, K
K	Clock, Clear	Preset, J

¶ Duration of this test should not exceed 1 second.

1. Preset is not applicable to SN54H73, SN74H73, SN54H103, SN74H103.
2. I_{CC} is measured (simultaneously for both flip-flops) for the following conditions:
   a. J = K = Clock = Clear = Gnd.
      Preset (when applicable) = 4.5 V.
   b. For SN54H73, SN74H73, SN54H103, and SN74H103: J = Clear = 4.5 V, K = Gnd, and apply momentary 4.5 V, then Gnd, to Clock. For SN54H76, SN74H76, SN54H78, SN74H78, SN54H108, SN74H108: J = K = Clock = Preset = Gnd, and Clear = 4.5 V.
3. Each flip-flop is tested separately except where Note 4 is referenced.
4. Apply the same conditions to both flip-flops when testing the SN54H108 and SN74H108.

FIGURE 67

§ Arrows indicate actual direction of current flow.

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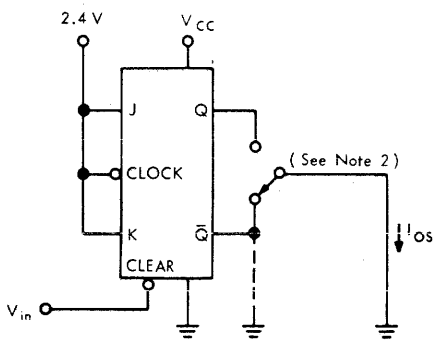
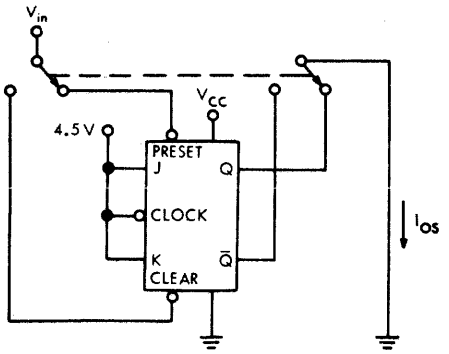
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



1. Each flip-flop is tested separately.
2. Test circuit shows setup for testing $\bar{Q}$. When testing Q, apply 4.5 V to Clear, ground $\bar{Q}$, and limit duration of test to 100 ms.

FIGURE 68



1. Each flip-flop is tested separately.

FIGURE 69

§ Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)

TEST TABLE

APPLY V_{in} (TEST $I_{in(1)}$)	CONDITIONS ON OTHER INPUTS AND OUTPUTS			
	4.5 V	S1	2 V	GND
Clock	None	Open	All K inputs	All J inputs and Preset
Clock	Preset	Closed	All J inputs	All K inputs, and momentarily GND Q, then open

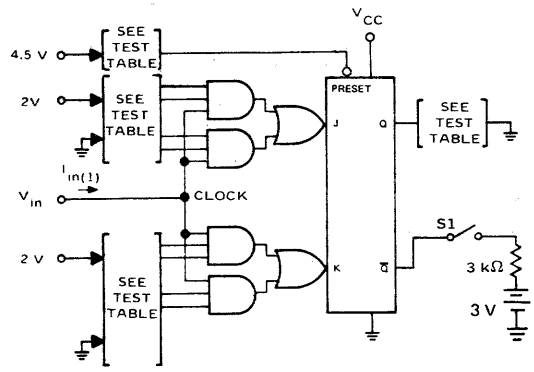


FIGURE 70

TEST TABLE

Apply V_{in} (TEST $I_{in(1)}$)	CONDITIONS ON OTHER INPUTS		
	4.5 V	2 V	GND
Clock	Clear	All K inputs	All J inputs and Preset
Clock	Preset	All J inputs	All K inputs and Clear

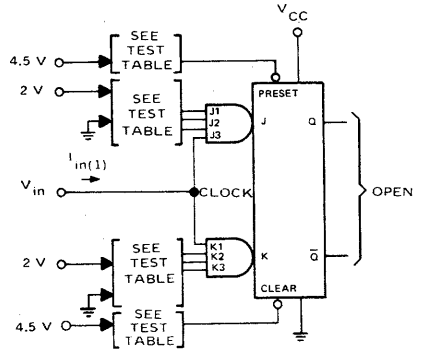


FIGURE 71

TEST TABLE

APPLY V_{in} (TEST $I_{in(1)}$)	CONDITIONS ON OTHER INPUTS AND OUTPUTS			
	4.5 V	S1	2 V	GND
Clock	None	Open	J	K and Clear
Clock	Clear	Closed	K	J, and momentarily GND A, then open

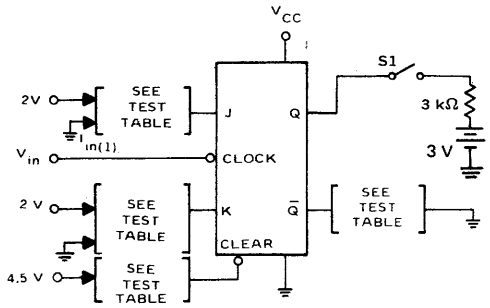


FIGURE 72

TEST TABLE

APPLY V_{in} (TEST $I_{in(1)}$)	CONDITIONS ON OTHER INPUTS		
	4.5 V	2 V	GND
Clock	Clear	K	J and Preset
Clock	Preset	J	K and Clear

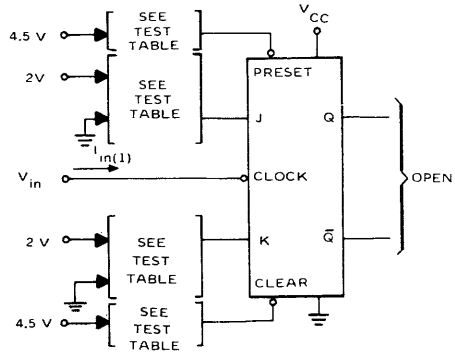
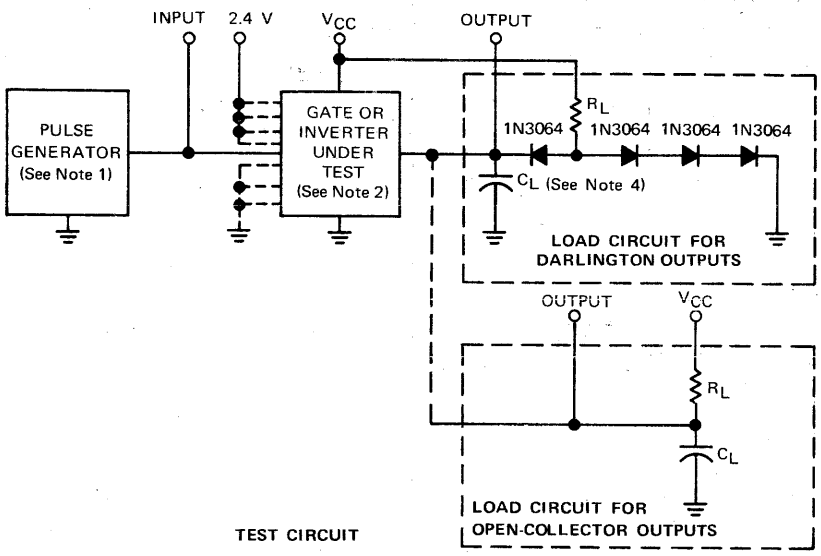


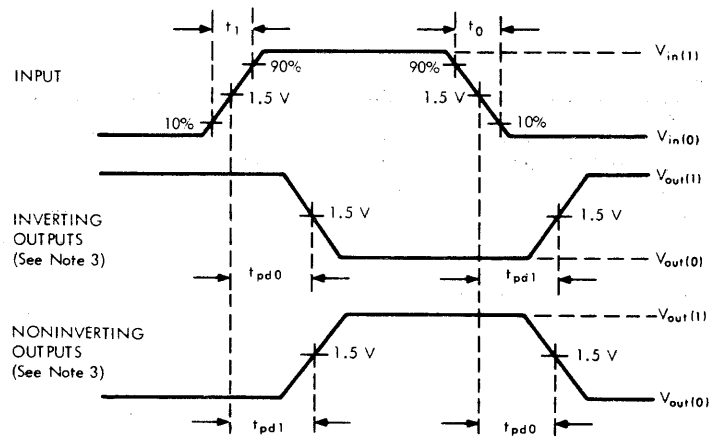
FIGURE 73

§Arrows indicate actual direction of current flow.

switching characteristics

PARAMETER MEASUREMENT INFORMATION





VOLTAGE WAVEFORMS

NOTES: 1. The pulse generator has the following characteristics: $V_{in(1)}$ = 3 V, $V_{in(0)}$ = 0 V, $t_1 = t_0$ = 7 ns, PRR = 1 MHz, duty cycle = 50%, and $Z_{out} \approx 50\ \Omega$.

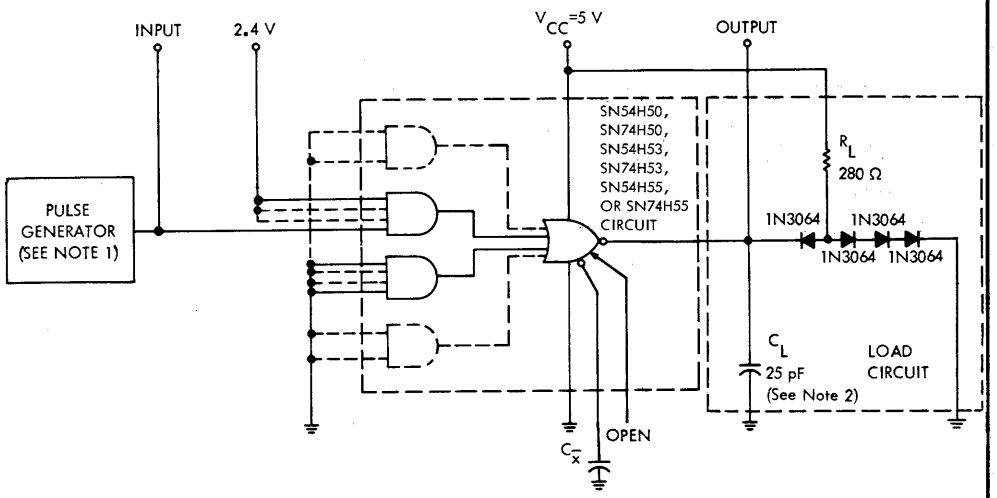
2. Input conditions are established for each gate as follows:
   a. Input pulse is applied to one input and 2.4 V is applied to all unused inputs of the SN54H00/SN74H00, SN54H01/SN74H01, SN54H04/SN74H04, SN54H05/SN74H05, SN54H10/SN74H10, SN54H11/SN74H11, SN54H20/SN74H20, SN54H21/SN74H21, SN54H22/SN74H22, SN54H30/SN74H30, or SN54H40/SN74H40 gate.
   b. Input pulse is applied to one input of one AND section, and 2.4 V is applied to all unused inputs of that AND section of the SN54H50/SN74H50, SN54H51/SN74H51, SN54H52/SN74H52, SN54H53/SN74H53, SN54H54/SN74H54, or SN54H55/SN74H55 gate. All inputs of all unused AND sections are grounded.
3. All gates are inverting except the SN54H11/SN74H11, SN54H21/SN74H21, and SN54H52/SN74H52 only.
4. C_L includes probe and jig capacitance.

FIGURE 74 – GATE PROPAGATION DELAY TIMES

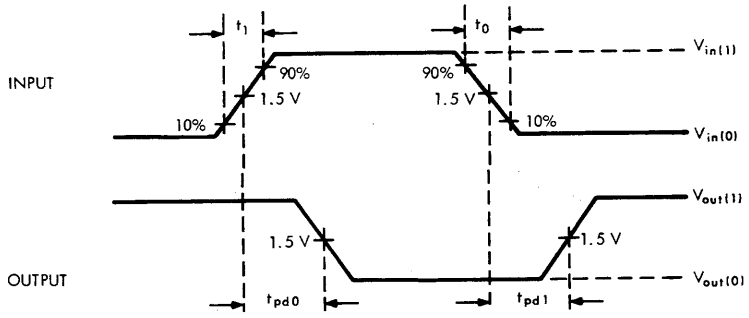
7

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: 1. The generator has the following characteristics: $V_{in(1)} = 3$ V, $V_{in(0)} = 0$ V, $t_0 = t_1 = 7$ ns, duty cycle = 50%, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
2. C_L includes probe and jig capacitance.
3. C_x includes jig capacitance.

FIGURE 75 – SN54H50/SN74H50, SN54H53/SN74H53, SN54H55/SN74H55
PROPAGATION DELAY TIMES

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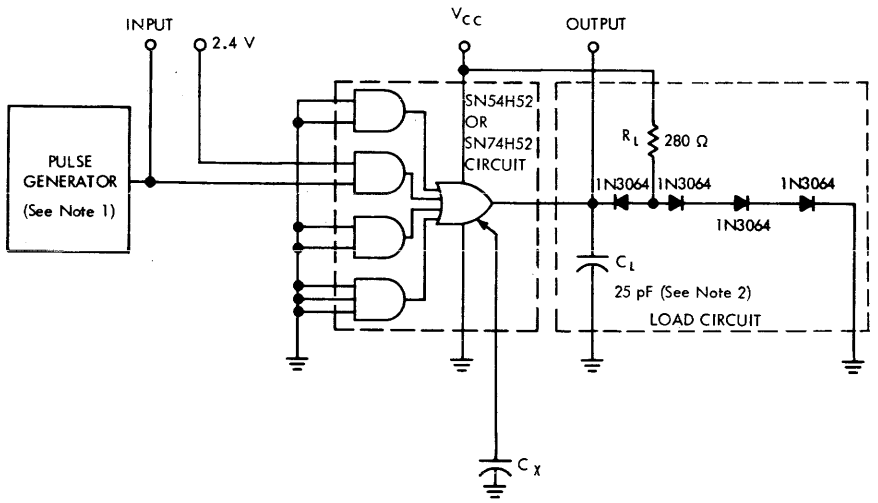
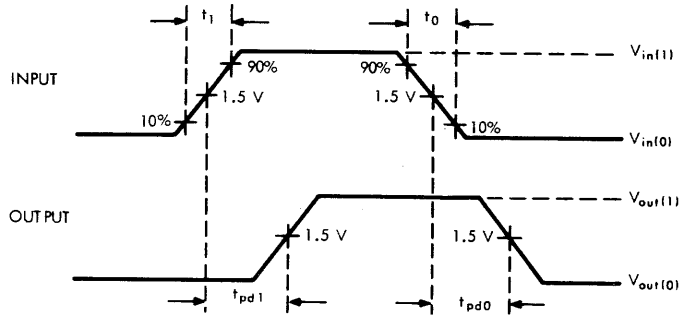
PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



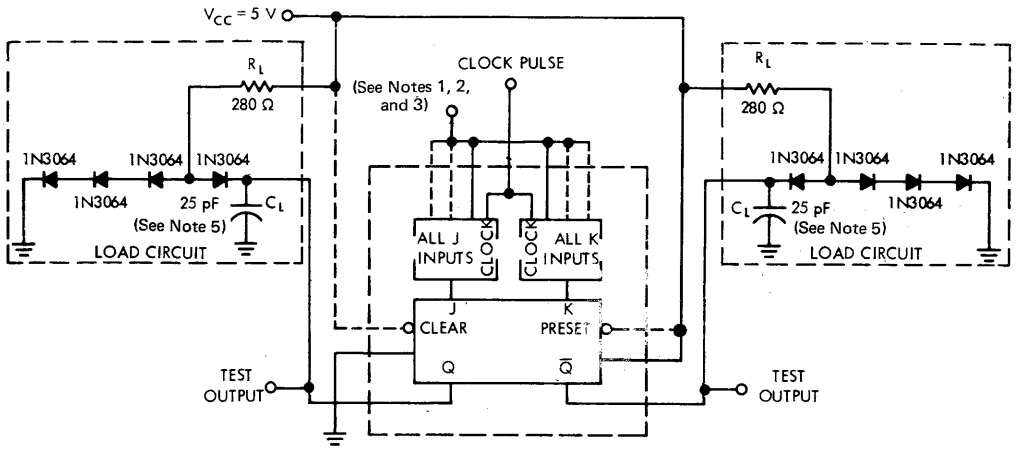
VOLTAGE WAVEFORMS

NOTES: 1. The generator has the following characteristics: $V_{in(1)} = 3$ V, $V_{in(0)} = 0$ V, $t_0 = t_1 = 7$ ns, duty cycle = 50%, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
2. C_L includes probe and jig capacitance.
3. C_X includes jig capacitance.

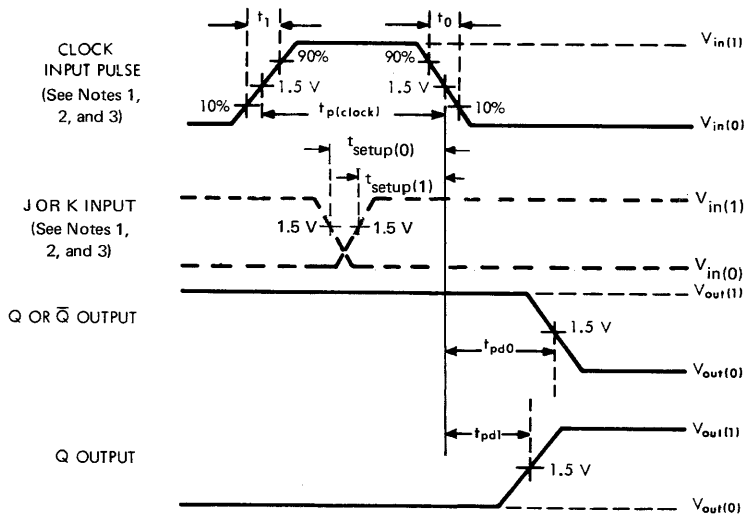
FIGURE 76 – SN54H52/SN74H52 PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

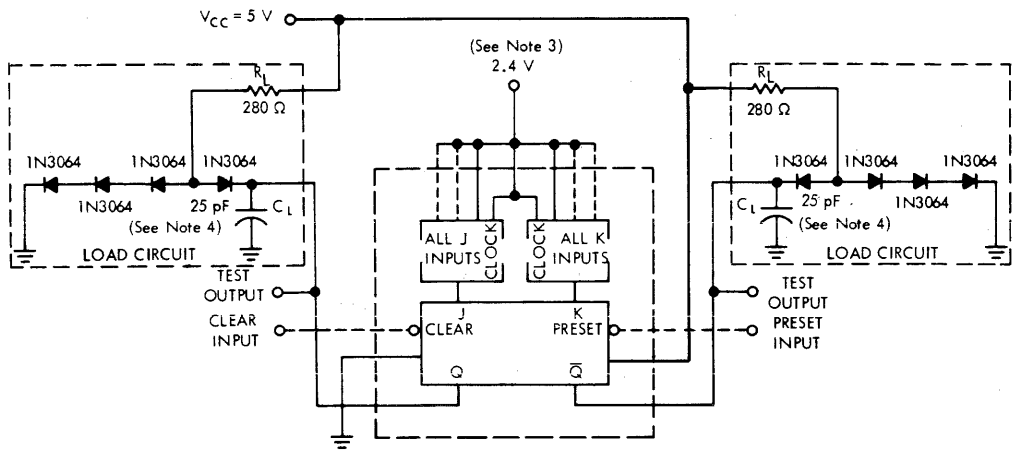
NOTES:
1. When testing t_{pd0} and t_{pd1} (all types), the clock input pulse characteristics are: $V_{in(1)}$ = 3 V, $V_{in(0)}$ = 0 V, $t_1 = t_0$ = 7ns, $t_{p(clock)}$ = 20 ns, and PRR = 1 MHz. When testing SN54H71/SN74H71, SN54H72/SN74H72, SN54H73/SN74H73, SN54H76/SN74H76, and SN54H78/SN74H78, all J and K inputs are at 2.4 V. When testing SN54H101/SN74H101, SN54H102/SN74H102, SN54H103/ SN74H103, SN54H106/SN74H106, and SN54H108/SN74H108, conditions are established to ensure that minimum setup times are verified.
2. When testing f_{clock} of SN54H71/SN74H71, SN54H72/SN74H72, SN54H73/SN74H73, SN54H76/SN74H76, and SN54H78/SN74H78, the clock input characteristics are: $V_{in(1)}$ = 3 V, $V_{in(0)}$ = 0 V, $t_1 = t_0$ = 3 ns, $t_{p(clock)}$ = 12 ns, and PRR = 25 MHz. All J and K inputs are at 2.4 V.
3. When testing f_{clock} of SN54H101/SN74H101, SN54H102/SN74H102, SN54H103/SN74H103, SN54H106/SN74H106, and SN54H108/SN74H108, the clock input characteristics are: $V_{in(1)}$ = 3 V, $V_{in(0)}$ = 0, $t_1 = t_0$ = 3 ns, $t_{p(clock)}$ = 10 ns, and PRR = 40 MHz. All J and K inputs are at 2.4 V.
4. See applicable circuit type for actual J and K input configuration and presence of preset or clear functions.
5. C_L includes probe and jig capacitance.

FIGURE 77—FLIP-FLOP PROPAGATION DELAY TIMES

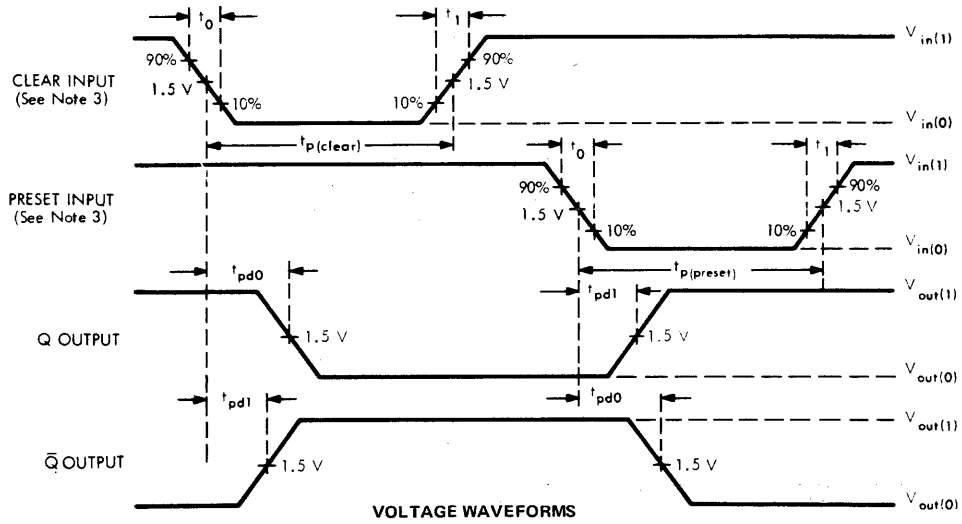
7

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



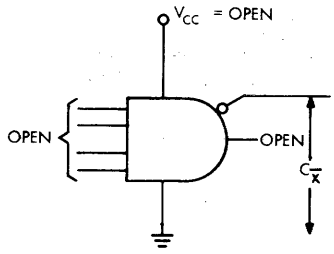
VOLTAGE WAVEFORMS

NOTES: 1. Clear or Preset inputs dominate regardless of the state of Clock or J-K inputs.
2. Clear or Preset input pulse characteristics: $V_{in(1)} = 3$ V, $V_{in(0)} = 0$ V, $t_1 = t_0 = 7$ ns, $t_{p(clear)} = t_{p(preset)} = 16$ ns, and PRR = 1 MHz.
3. See applicable circuit type for actual J and K input configuration and presence of Preset or Clear junctions.
4. C_L includes probe and jig capacitance.

FIGURE 78—FLIP-FLOP PRESET/CLEAR PROPAGATION DELAY TIMES

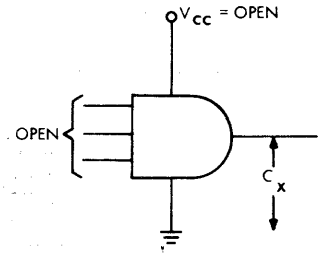
PARAMETER MEASUREMENT INFORMATION

switching time data test circuits



1. Each output is tested separately.

FIGURE 79

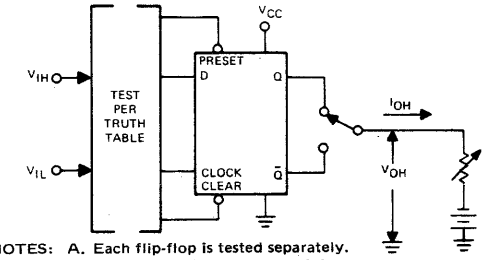


1. Each output is tested separately.

FIGURE 80

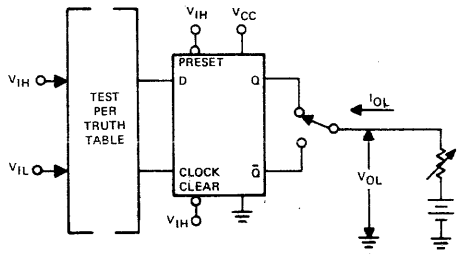
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



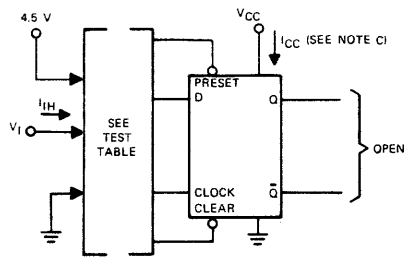
NOTES: A. Each flip-flop is tested separately.
B. Each output is tested separately.
C. V_{OH} is also tested using Clear and Preset inputs.

FIGURE 81–V_{IH}, V_{IL}, V_{OH}



NOTES: A. Each flip-flop is tested separately.
B. Each output is tested separately.

FIGURE 82–V_{IH}, V_{IL}, V_{OL}



TEST TABLE

APPLY V_I (TEST I_{IH})	APPLY 4.5 V	APPLY GND
Clock	Clear and D	Preset
Clock	Preset and D	Clear
Preset	Clear and D	Clock (See Note B)
Clear	Preset	Clock, D, and Q
Clear	Preset	D and Clock (See Note B)
D	Preset and Clock	Clear

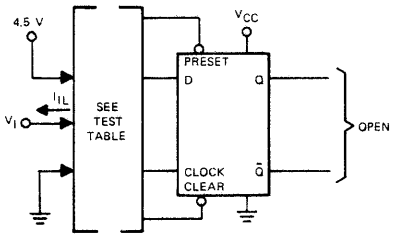
NOTES: A. Each input of each flip-flop is tested separately for I_{IH}.
B. GND is momentarily applied to Clock, then 4.5 V.
C. I_{CC} is measured simultaneously for both flip-flops with D, Clock, and Preset at GND; then with D, Clock, and Clear at GND.

FIGURE 83–I_{IH}, I_{CC}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

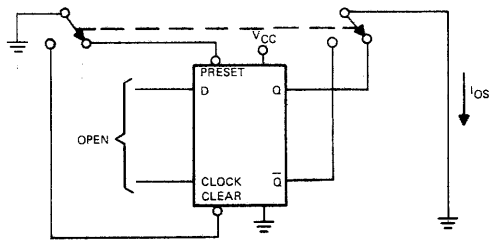


NOTES: A. Each flip-flop is tested separately.
B. Each input is tested separately.

TEST TABLE

APPLY V_{in} (TEST I_{IL})	APPLY 4.5 V	APPLY GND
Clock	Clear	Preset and D
Preset	Clear	Clock and D
Clear	Clock, D, and Preset	None
D	Clear and Clock	Preset

FIGURE 84–I_{IL}



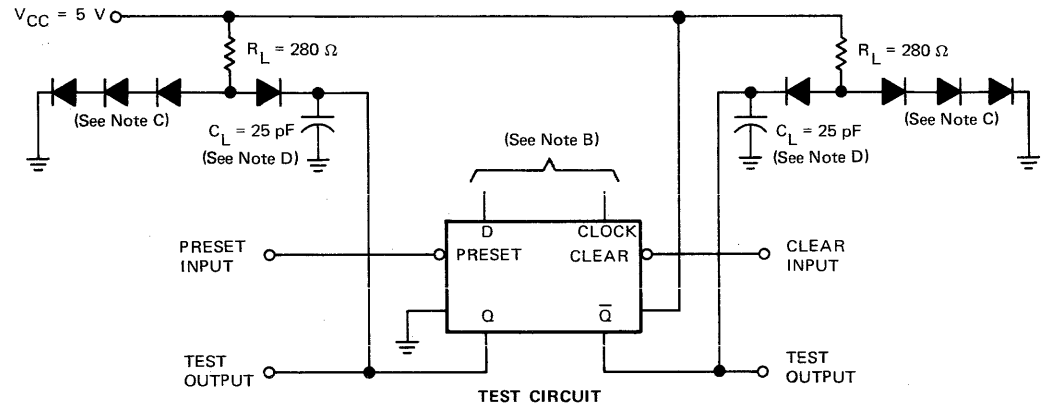
NOTE: Each output is tested separately.

FIGURE 85–I_{OS}

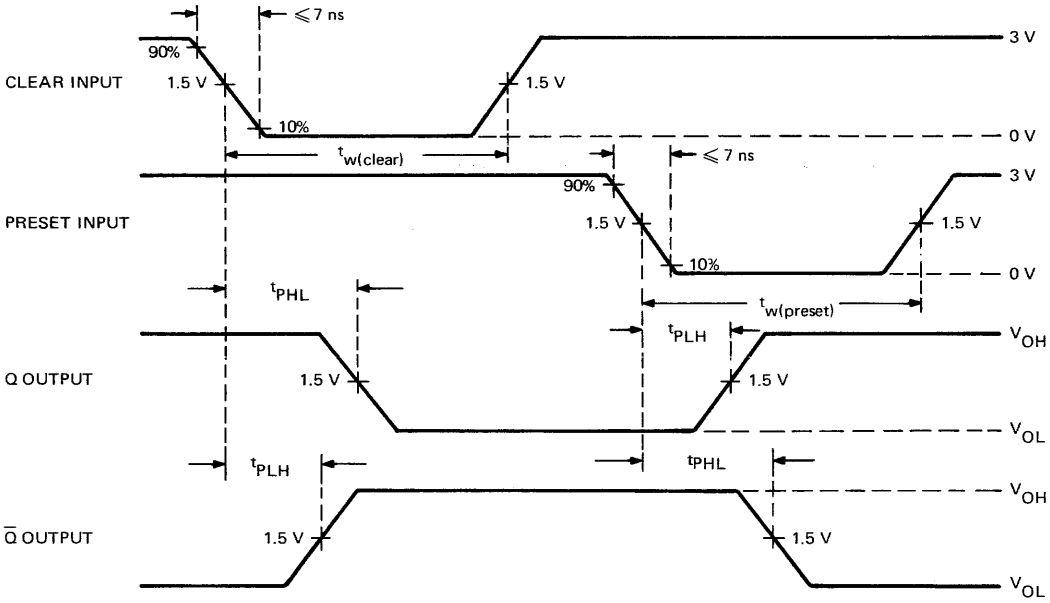
†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



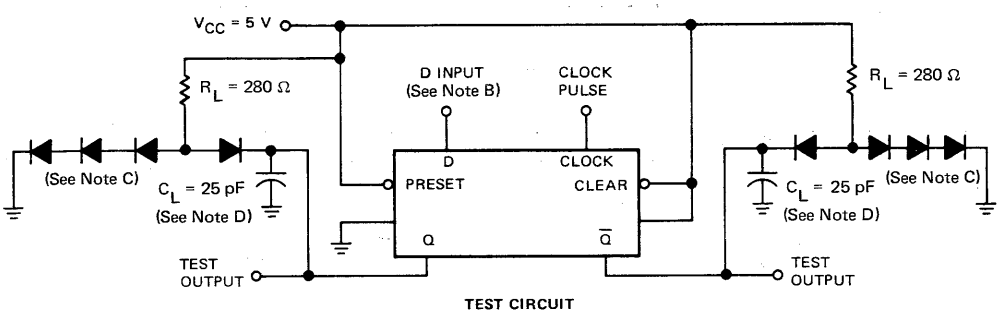
VOLTAGE WAVEFORMS

NOTES: A. Clear or Preset input pulse characteristics: $t_{w(clear)} = t_{w(preset)}$ = 25 ns, PRR = 1 MHz.
B. Clear and Preset inputs dominate regardless of the state of Clock or D inputs.
C. All diodes are 1N3064.
D. C_L includes probe and jig capacitance.

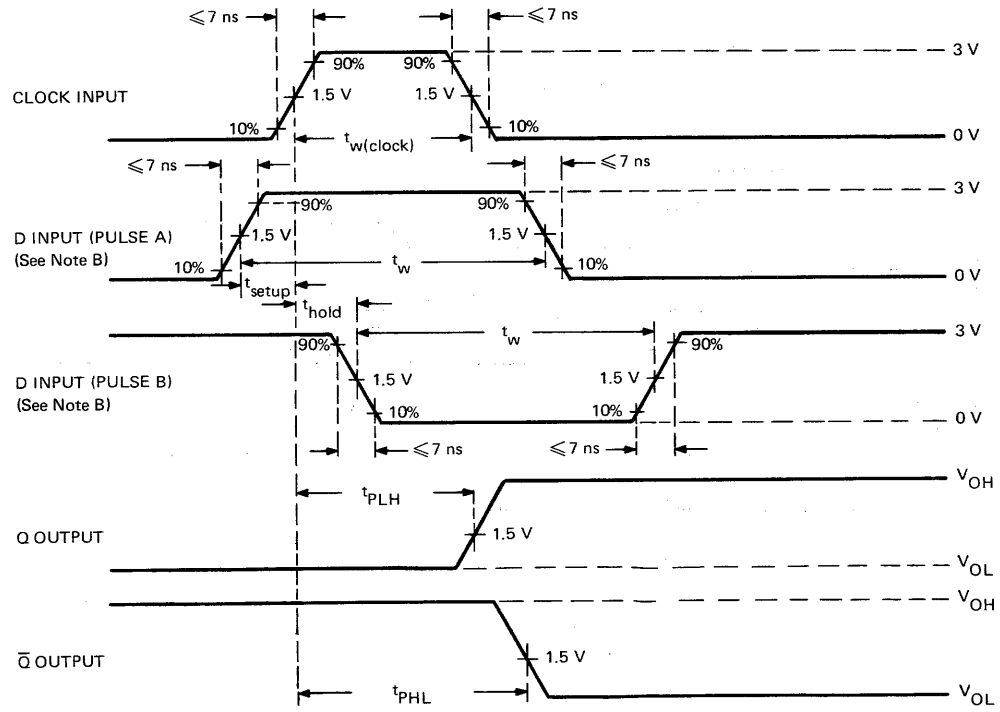
FIGURE 86–ASYNCHRONOUS INPUTS SWITCHING CHARACTERISTICS

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

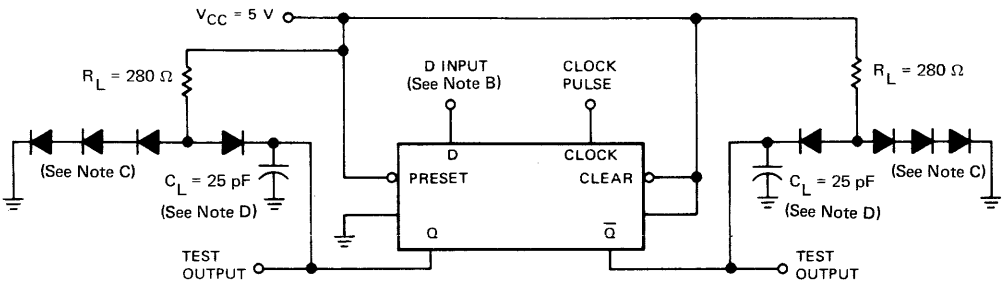
NOTES: A. Clock input pulse has the following characteristics: $t_{w(clock)}$ = 20 ns and PRR = 1 MHz. When testing f_{clock}, vary PRR.
B. D input (pulse A) has the following characteristics: t_{setup} = 10 ns, t_w = 60 ns, and PRR is 50% of the clock PRR. D input (pulse B) has the following characteristics: t_{hold} = 0 ns, t_w = 60 ns, and PRR is 50% of the clock PRR.
C. All diodes are 1N3064.
D. C_L includes probe and jig capacitance.

FIGURE 87–SWITCHING CHARACTERISTICS, CLOCK AND SYNCHRONOUS INPUTS (HIGH-LEVEL DATA)

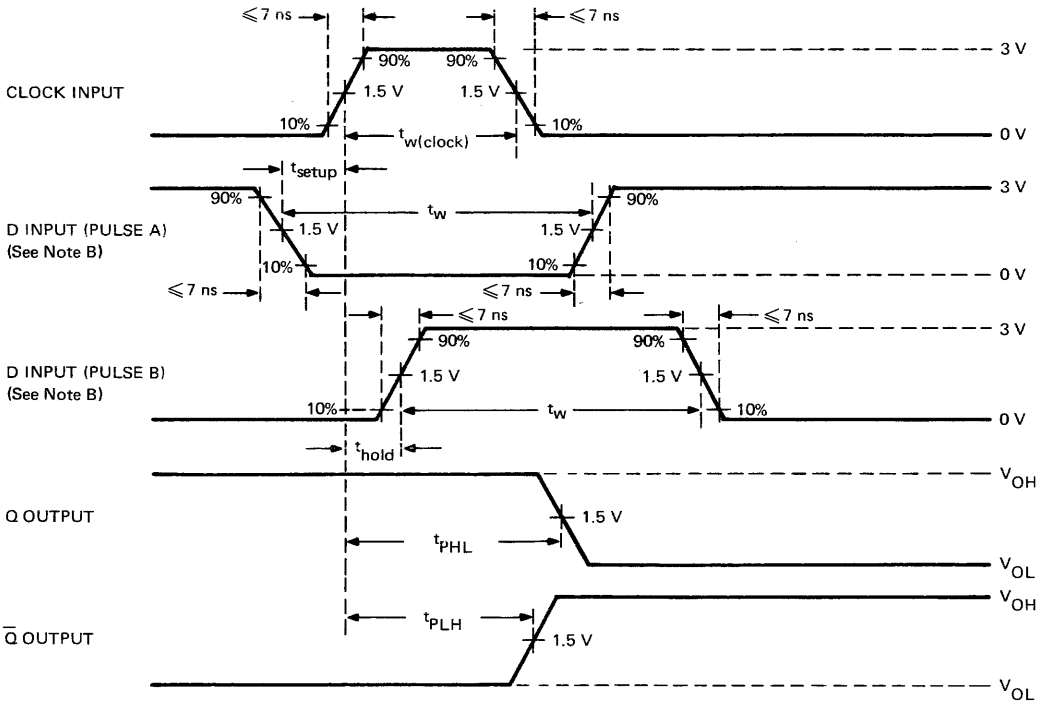
7

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



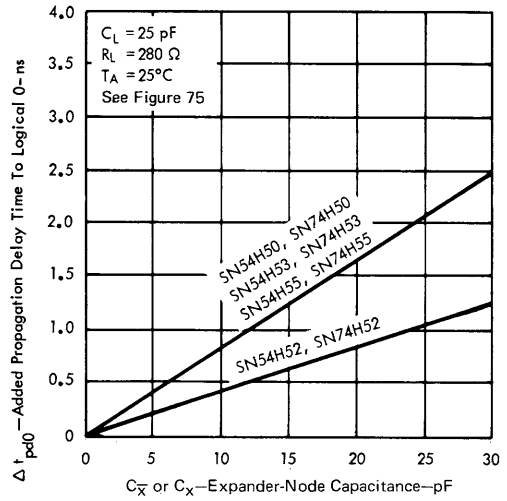
VOLTAGE WAVEFORMS

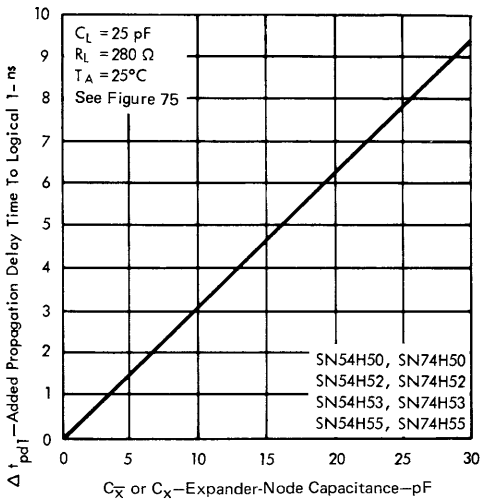
NOTES: A. Clock input pulse has the following characteristics: t_w = 20 ns and PRR = 1 MHz. When testing f_{clock}, vary PRR.
B. D input (pulse A) has the following characteristics: t_{setup} = 15 ns, t_w = 60 ns, and PRR is 50% of the clock PRR. D input (pulse B) has the following characteristics: t_{hold} = 0 ns, t_w = 60 ns, and PRR is 50% of the clock PRR.
C. All diodes are 1N3064.
D. C_L includes probe and jig capacitance.

FIGURE 88–SWITCHING CHARACTERISTICS, CLOCK AND SYNCHRONOUS INPUTS (LOW-LEVEL DATA)

TYPICAL CHARACTERISTICS

ADDED PROPAGATION DELAY TIME vs EXPANDER-NODE CAPACITANCE





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