TTL MSI Circuits

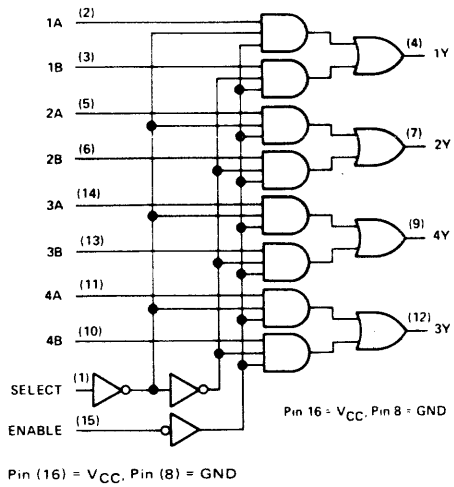
New TTL/MSI Now Available

SN54/74157 Quad 2-Line-To-1-Line Data Selector/Multiplexer With Strobe Control

- Pin-for-pin replacement for 9322-type multiplexers
- Selects bused data from one of two sources
- Ideal for controlling accumulator inputs
- Use to expand any data input point
- Generates four functions of two variables (one variable is common)
- Source programmable counters

LOGIC

SN54/74157



Pin (16) = V_{CC}, Pin (8) = GND

TYPICAL POWER: 125 mW
TYPICAL PROPAPATION DELAY
TIME 20 ns (SELECT TO OUTPUT)

Available in 16-pin
J, N, and W packages

TTL
MEDIUM SCALE INTEGRATION (MSI)

FUNCTION	OPERATING TEMPERATURE RANGE		PACKAGES*			SEC.-PAGE
	−55°C to 125°C	0°C to 70°C	Dual-In-Line		Flat	
ASYNCHRONOUS COUNTERS						
Decade Counters	SN5490	SN7490	J	N	W	9-4
Decade Counters (Low Power)	SN54L90	SN74L90	J	N	T	9-9
Divide-by-Twelve Counters	SN5492	SN7492	J	N	W	9-14
4-Bit Binary Counters	SN5493	SN7493	J	N	W	9-19
4-Bit Binary Counters (Low Power)	SN54L93	SN74L93	J	N	T	9-24
50-MHz Preset Table Decade Counters/Latches	SN54196	SN74196	J	N	W	9-29
50-MHz Preset Table 4-Bit Binary Counters/Latches	SN54197	SN74197	J	N	W	9-29
SYNCHRONOUS COUNTERS						
Synchronous 6-Bit Binary Rate Multiplier		SN7497	J	N	W	9-35
Sychronous Decade Counters	SN54160	SN74160	J	N	W	9-41
Synchronous 4-Bit Binary Counters	SN54161	SN74161	J	N	W	9-41
Fully Synchronous Decade Counters	SN54162	SN74162	J	N	W	9-41
Fully Synchronous 4-Bit Binary Counters	SN54163	SN74163	J	N	W	9-41
Synchronous Decade Decimal Rate Multiplier		SN74167	J	N	W	9-35
Synchronous Up/Down Decade Counters (Single Clock Line)	SN54190	SN74190	J	N	W	9-49
Synchronous Up/Down 4-Bit Binary Counters (Single Clock Line)	SN54191	SN74191	J	N	W	9-49
Synchronous Up/Down Decade Counters (Two Clock Lines)	SN54192	SN74192	J	N	W	9-57
Synchronous Up/Down 4-Bit Binary Counters (Two Clock Lines)	SN54193	SN74193	J	N	W	9-57
4-BIT, 5-BIT, 6-BIT SHIFT/STORAGE REGISTERS						
4-Bit Shift Registers (Parallel-In, Serial-Out)	SN5494	SN7494	J	N	W	9-58
4-Bit Universal Shift Registers (Parallel-In, Parallel-Out)	SN5495A	SN7495A	J	N	W	9-72
4-Bit Universal Shift Registers (Parallel-In, Parallel-Out) (Low Power)	SN54L95	SN74L95	J	N	T	9-79
5-Bit Shift Registers (Dual-Parallel-In, Parallel-Out)	SN5496	SN7496	J	N	W	9-86
4-Bit Data Selectors/Storage Registers (Low Power)	SN54L98	SN74L98	J	N		9-90
4-Bit Right-Shift Registers with J $\overline{K}$ and D (Low Power)	SN54L99	SN74L99	J	N		9-96
4-Bit Parallel-In, Parallel-Out Bidirectional Shift Registers	SN54194	SN74194	J	N	W	9-104
4-Bit Parallel-In, Parallel-Out Shift Register (J-$\overline{K}$ Inputs to First Stage)	SN54195	SN74195	J	N	W	9-108

*For outline drawings of all packages, see Section 1.

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—SEE ORDERING INSTRUCTIONS PAGE 1-1—

TTL MSI INDEX

TTL
MEDIUM SCALE INTEGRATION (MSI)

FUNCTION	OPERATING TEMPERATURE RANGE		PACKAGES*			SEC.-PAGE
	–55°C to 125°C	0°C to 70°C	Dual-In-Line		Flat	
8-BIT SHIFT REGISTERS						
8-Bit Shift Registers	SN5491A	SN7491A	J	N	W	9-112
8-Bit Shift Registers (Low Power)	SN54L91	SN74L91	J	N	T	9-117
8-Bit Parallel-Out Shift Registers	SN54164	SN74164	J	N	W	9-122
8-Bit Parallel-Out Shift Registers (Low Power)	SN54L164	SN74L164	J	N	T	9-126
Parallel-Load 8-Bit Shift Registers	SN54165	SN74165	J	N	W	9-130
Parallel-Load 8-Bit Shift Registers	SN54166	SN74166	J	N	W	9-134
8-Bit Parallel-In, Parallel-Out Bidirectional Shift Registers	SN54198	SN74198	J	N	W	9-134
8-Bit Parallel-In, Parallel-Out Shift Registers (J-$\overline{K}$ Inputs to First Stage)	SN54199	SN74199	J	N	W	9-134
CODE CONVERTERS						
BCD-to-Binary Converters	SN54184	SN74184	J	N	W	9-142
Binary-to-BCD Converters	SN54185A	SN74185A	J	N	W	9-142
DECODERS/DEMULTIPLEXERS						
BCD-to-Decimal Decoders	SN5442	SN7442	J	N	W	9-148
BCD-to-Decimal Decoders (Low Power)	SN54L42	SN74L42	J	N		9-154
Excess-3-to-Decimal Decoders	SN5443	SN7443	J	N	W	9-148
Excess-3-to-Decimal Decoders (Low Power)	SN54L43	SN74L43	J	N		9-154
Excess-3-Gray-to-Decimal Decoders	SN5444	SN7444	J	N	W	9-148
Excess-3-Gray-to-Decimal Decoders (Low Power)	SN54L44	SN74L44	J	N	W	9-154
4-Line-to-16-Line (1 of 16) Decoders/Demultiplexers	SN54154	SN74154	J	N	W	9-160
Dual 2-Line-to-4-Line Decoders/Demultiplexers	SN54155	SN74155	J	N	W	9-167
Dual 2-Line-to-4-Line Decoders/Demultiplexers (with Open-Collector Output)	SN54156	SN74156	J	N	W	9-167
DECODERS/LAMP DRIVERS/BUFFERS						
BCD-to-Decimal Decoders/Drivers with 30-V Output	SN5445	SN7445	J	N	W	9-175
BCD-to-Decimal Decoders/Drivers with 15-V Output	SN54145	SN74145	J	N	W	9-175
BCD-to-Seven-Segment Decoders/Drivers with 30-V Output	SN5446A	SN7446A	J	N	W	9-181
BCD-to-Seven-Segment Decoders/Drivers with 30-V Output (Low Power)	SN54L46	SN74L46	J	N		9-198
BCD-to-Seven-Segment Decoders/Drivers with 15 V Output	SN5447A	SN7447A	J	N	W	9-181
BCD-to-Seven-Segment Decoders/Drivers with 15-V Output (Low Power)	SN54L47	SN74L47	J	N		9-198
BCD-to-Seven-Segment Decoders	SN5448	SN7448	J	N	W	9-181
BCD-to-Seven-Segment Decoders (14-pin Function)	SN5449	SN7449	J	N	W	9-181
BCD-to-Decimal Decoder/Driver		SN74141	J	N	W	9-208

*For outline drawings of all packages, see Section 1.

–SEE ORDERING INSTRUCTIONS PAGE 1-1–

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TTL
MEDIUM SCALE INTEGRATION (MSI)

FUNCTION	OPERATING TEMPERATURE RANGE		PACKAGES*			SEC.-PAGE
	−55°C to 125°C	0°C to 70°C	Dual-In-Line		Flat	
LATCHES						
Quadruple Bistable Latches	SN5475	SN7475	J	N	W	9-213
Quadruple Bistable Latches (14-pin Function)	SN5477	SN7477			W	9-213
8-Bit Bistable Latches	SN54100	SN74100	J	N	W	9-213
MEMORIES						
16-Bit Random-Access Memories (16W by 1B)	SN5481	SN7481	J	N	W	9-221
16-Bit Random-Access Memories with Gated Write Inputs (16W by 1B)	SN5484	SN7484	J	N	W	9-221
64-Bit Random-Access Memory (16W by 4B)		SN7489	J	N	W	9-230
256-Bit Read-Only Memories (32W by 8B)	SN5488A	SN7488A		N		9-235
1024-Bit Read-Only Memories (256W by 4B)	SN54187	SN74187	J	N	W	9-244
4-By-4 Register Files	SN54170	SN74170	J	N	W	9-248
ARITHMETIC ELEMENTS						
Gated Full Adders	SN5480	SN7480	J	N	W	9-255
2-Bit Binary Full Adders	SN5482	SN7482	J	N	W	9-264
4-Bit Binary Full Adders	SN5483	SN7483	J	N	W	9-271
4-Bit Binary Full Adders (Low-Power Schottky)	SN54LS83	SN74LS83	J	N		9-279
4-Bit Magnitude Comparators	SN5485	SN7485	J	N	W	9-286
4-Bit Magnitude Comparators (Low Power)	SN54L85	SN74L85	J	N		9-289
Quadruple 2-Input Exclusive-OR Gates	SN5486	SN7486	J	N	W	9-296
Quadruple 2-Input Exclusive-OR Gates (Low Power)	SN54L86	SN74L86	J	N	T	9-300
4-Bit True/Complement Zero-One Elements	SN54H87	SN54H87	J	N	W	9-304
8-Bit Odd/Even Parity Generators/Checkers	SN54180	SN74180	J	N	W	9-309
4-Bit Arithmetic Logic Unit (ALU) and Function Generators	SN54181	SN74181	J	N	W	9-315
Look-Ahead Carry Generators (for ALU)	SN54182	SN74182	J	N	W	9-326
Dual Carry-Save Full Adders	SN54H183	SN74H183	J	N	W	9-332
DATA SELECTORS/MULTIPLEXERS						
16-Bit Data Selectors/Multiplexers	SN54150	SN74150	J	N	W	9-339
8-Bit Data Selectors/Multiplexers with Strobe	SN54151	SN74151	J	N	W	9-339
8-Bit Data Selectors/Multiplexers	SN54152	SN74152			W	9-339
Dual 4-Line-to-1-Line Data Selectors/Multiplexers	SN54153	SN74153	J	N	W	9-351
Dual 4-Line-to-1-Line Data Selectors/Multiplexers (Low Power)	SN54L153	SN74L153	J	N		9-358
LOGIC DIODE MATRICES						
Series TIDM1, TIDM2 Monolithic Diode Matrices			J		F, W	9-365

*For outline drawings of all packages, see Section 1.

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

CIRCUIT TYPES SN5490, SN7490
DECADE COUNTERS

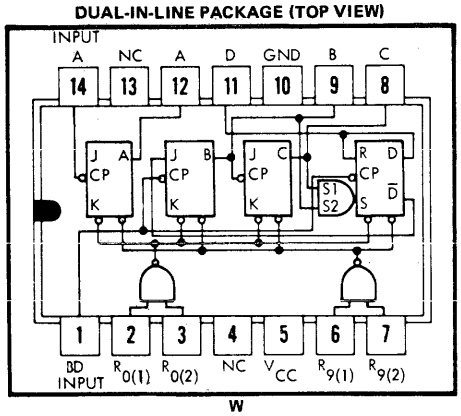
MSI TTL HIGH-SPEED DECADE COUNTERS

for applications in

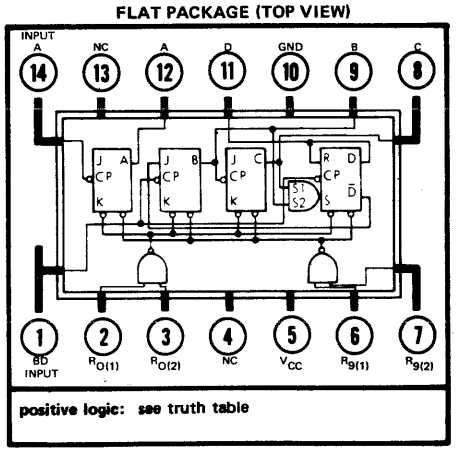
- Digital Computer Systems
- Data-Handling Systems
- Control Systems

logic

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



W
FLAT PACKAGE (TOP VIEW)



positive logic: see truth table

TRUTH TABLES

BCD COUNT SEQUENCE
(See Note 1)

COUNT	OUTPUT D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

RESET/COUNT (See Note 2)

RESET INPUTS $R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	OUTPUT D C B A
1	1	0	X	0 0 0 0
1	1	X	0	0 0 0 0
X	X	1	1	1 0 0 1
X	0	X	0	COUNT
0	X	0	X	COUNT
0	X	X	0	COUNT
X	0	0	X	COUNT

NC—No Internal Connection

NOTES: 1. Output A connected to input BD for BCD count.
2. X indicates that either a logical 1 or a logical 0 may be present.

description and typical count configurations

These high-speed, monolithic decade counters consist of four dual-rank, master-slave flip-flops internally interconnected to provide a divide-by-two counter and a divide-by-five counter. Gated direct reset lines are provided to inhibit count inputs and return all outputs to zero or to a binary coded decimal (BCD) count of 9. As the output from flip-flop A is not internally connected to the succeeding stages, the count may be separated in three independent count modes:

1. When used as a binary coded decimal decade counter, the BD input must be externally connected to the A output. The A input receives the incoming count, and a count sequence is obtained in accordance with the BCD count sequence truth table shown above. In addition to a conventional zero reset, inputs are provided to reset a BCD count for nine's complement decimal applications.

2. If a symmetrical divide-by-ten count is desired for frequency synthesizers or other applications requiring division of a binary count by a power of ten, the D output must be externally connected to the A input. The input count is then applied at the BD input and a divide-by-ten square wave is obtained at output A.

3. For operation as a divide-by-two counter and a divide-by-five counter, no external interconnections are required. Flip-flop A is used as a binary element for the divide-by-two function. The BD input is used to obtain binary divide-by-five operation at the B, C, and D outputs. In this mode, the two counters operate independently; however, all four flip-flops are reset simultaneously.

These circuits are completely compatible with Series 54/74 TTL and DTL logic families. Average power dissipation is 160 mW.

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absolute maximum ratings (over operating temperature range unless otherwise noted)

Supply Voltage V_{CC} (See Note 3) . . . . . 7 V
Input Voltage, V_{in} (See Notes 3 and 4) . . . . . 5.5 V
Operating Free-Air Temperature Range: SN5490 Circuits . . . . . −55°C to 125°C
SN7490 Circuits . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

NOTES: 3. These voltage values are with respect to network ground terminal.
4. Input signals must be zero or positive with respect to network ground terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 3): SN5490 Circuits	4.5	5	5.5	V
SN7490 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output (See Note 5)			10	
Width of Input Count Pulse, $t_{p(in)}$	50			ns
Width of Reset Pulse, $t_{p(reset)}$	50			ns

NOTE 5. Fan-out from output A to input BD and to 10 additional Series 54/74 loads is permitted.

electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	2					0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, I_{load} = −400 μA		2.4			V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, I_{sink} = 16 mA				0.4	V
$I_{in(1)}$	Logical 1 level input current at $R_{0(1)}$, $R_{0(2)}$, $R_{9(1)}$, or $R_{9(2)}$	3	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at input A	3	V_{CC} = MAX, V_{in} = 2.4 V				80	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at input BD	3	V_{CC} = MAX, V_{in} = 2.4 V				160	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(0)}$	Logical 0 level input current at $R_{0(1)}$, $R_{0(2)}$, $R_{9(1)}$, or $R_{9(2)}$	4	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(0)}$	Logical 0 level input current at input A	4	V_{CC} = MAX, V_{in} = 0.4 V				−3.2	mA
$I_{in(0)}$	Logical 0 level input current at input BD	4	V_{CC} = MAX, V_{in} = 0.4 V				−6.4	mA
I_{OS}	Short-circuit output current§	5	V_{CC} = MAX	SN5490	−20		−57	mA
				SN7490	−18		−57	mA
I_{CC}	Supply current	3	V_{CC} = MAX	SN5490		32	46	mA
				SN7490		32	53	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the particular circuit type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C
§ Not more than one output should be shorted at a time.

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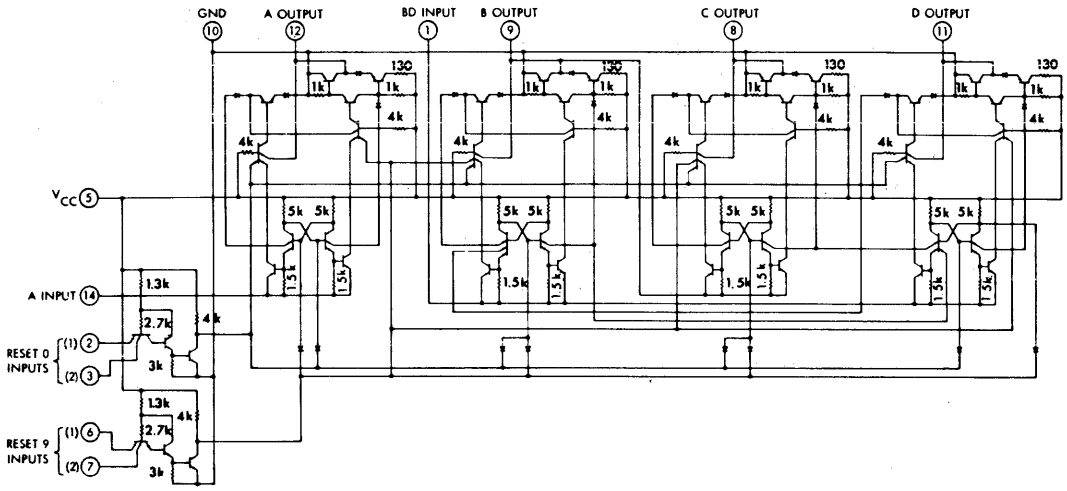
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum frequency of input count pulses		C_L = 15 pF, R_L = 400 Ω	10	18		MHz
t_{pd1}	Propagation delay time to logical 1 level from input count pulse to output C	6	C_L = 15 pF, R_L = 400 Ω		60	100	ns
t_{pd0}	Propagation delay time to logical 0 level from input count pulse to output C	6	C_L = 15 pF, R_L = 400 Ω		60	100	ns

schematic



Component values shown are nominal.
Resistor values are in ohms.

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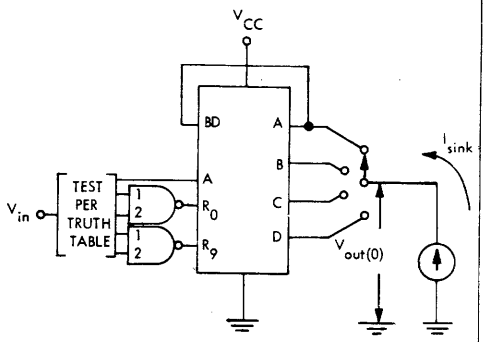
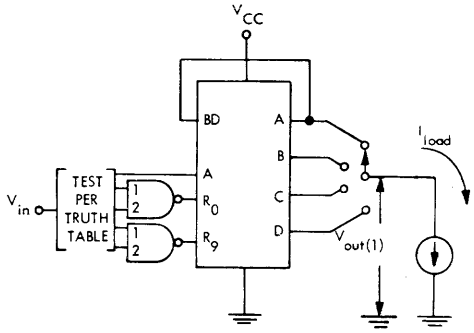
d-c test circuits†

PARAMETER MEASUREMENT INFORMATION



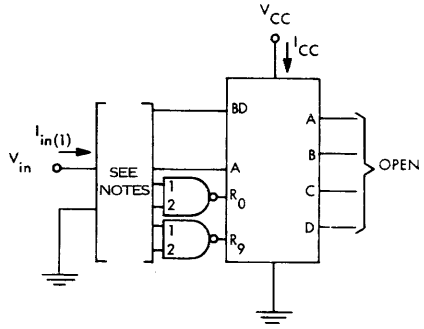
1. Each output is tested in the logical 0 state.

FIGURE 1



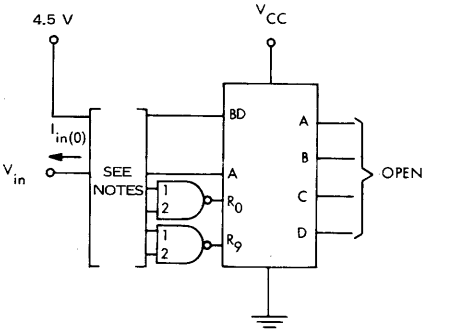
1. Each output is tested in the logical 1 state.

FIGURE 2



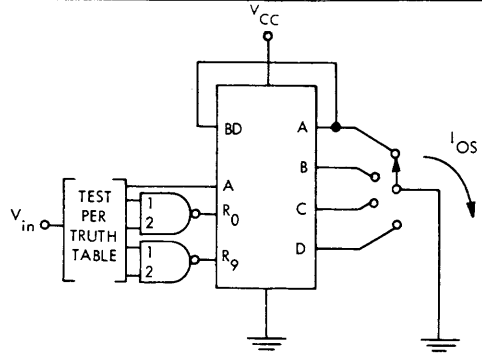
1. Each input is tested separately.
2. When testing $R_{0(1)}$ or $R_{9(1)}$, ground $R_{0(2)}$ or $R_{9(2)}$, respectively, and vice versa.
3. When testing I_{CC} reset all outputs to logical 0, ground all inputs, then measure I_{CC}.

FIGURE 3



1. Each input is tested separately.
2. When testing $R_{0(1)}$ or $R_{9(1)}$, apply 4.5 V to $R_{0(2)}$ or $R_{9(2)}$, respectively, and vice versa.

FIGURE 4



1. Each output is tested in the logical 1 state.

FIGURE 5

† Arrows indicate actual direction of current flow.

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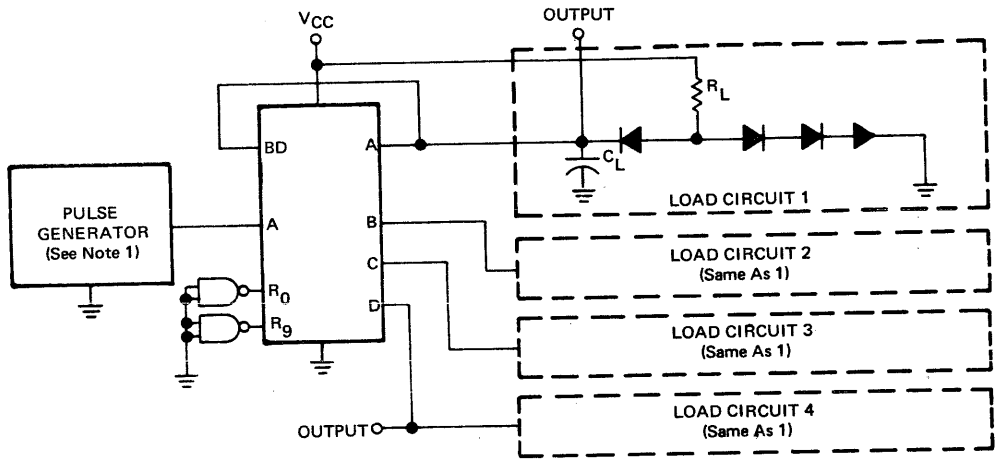
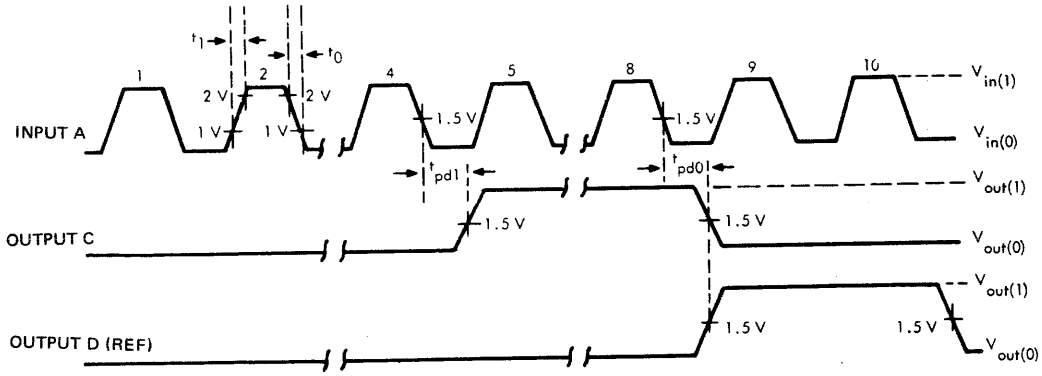
switching characteristics

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: 1. The pulse generator has the following characteristics: V_{gen} = 3 V, $t_0 = t_1 \leqslant 15$ ns, t_p = 0.5 µs, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
2. All diodes are 1N3064.
3. C_L includes probe and jig capacitance.
4. $t_{pd} = \frac{t_{pd0} + t_{pd1}}{2}$
5. Voltage values are with respect to ground terminal.

FIGURE 6-SWITCHING TIMES

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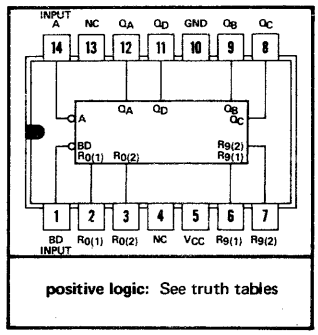
CIRCUIT TYPES SN54L90, SN74L90
DECADE COUNTERS

CIRCUIT TYPES SN54L90, SN74L90
BULLETIN NO. DL-S 7011373, NOVEMBER 1970

for applications in

- Digital Computer Systems
- Data-Handling Systems
- Control Systems

J OR N DUAL-IN-LINE OR
T FLAT PACKAGE (TOP VIEW)†



positive logic: See truth tables

NC—No internal connection
†Pin assignments for these circuits are the same for all packages.

logic

TRUTH TABLES

BCD COUNT SEQUENCE
(See Note A)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

BI-QUINARY (5-2)
(See Note B)

COUNT	OUTPUT			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

NOTES: A. Output Q_A is connected to input BD for BCD count.
B. Output Q_D is connected to input A for bi-quinary count.
C. H = high level, L = low level, X = irrelevant

RESET/COUNT FUNCTION TABLE

RESET INPUTS				OUTPUT			
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	D	C	B	A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

description and typical count configurations

These low-power monolithic decade counters consist of four dual-rank, master-slave flip-flops internally interconnected to provide a divide-by-two counter and a divide-by-five counter. Gated direct reset lines are provided to inhibit count inputs and return all outputs to zero or to a binary-coded-decimal (BCD) count of 9. As the output from flip-flop A is not internally connected to the succeeding stages, the counter may be operated in any one of three independent count modes:

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1. When used as a binary-coded-decimal decade counter, the BD input must be externally connected to the Q_A output. The A input receives the incoming count, and a count sequence is obtained in accordance with the BCD count sequence truth table shown above. In addition to a conventional zero reset, inputs are provided to reset a BCD count for nine's complement decimal applications.
2. If a symmetrical divide-by-ten count is desired for frequency synthesizers or other applications requiring division of a binary count by a power of ten, the Q_D output must be externally connected to the A input. The input count is then applied at the BD input and a divide-by-ten square wave is obtained at output Q_A in accordance with the bi-quinary truth table above.
3. For operation as a divide-by-two counter and a divide-by-five counter, no external interconnections are required. Flip-flop A is used as a binary element for the divide-by-two function. The BD input is used to obtain binary divide-by-five operation at the Q_B, Q_C, and Q_D outputs. In this mode, the two counters operate independently; however, all four flip-flops are reset simultaneously.

These circuits are compatible with most TTL and DTL logic families. Power dissipation is typically 20 mW. The SN54L90 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74L90 is characterized for operation from 0°C to 90°C.

TEXAS INSTRUMENTS
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CIRCUIT TYPES SN54L90, SN74L90
DECADE COUNTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 8 V
Input voltage (see Notes 1 and 2) . . . . . 5.5 V
Operating free-air temperature range: SN54L90 Circuits . . . . . −55°C to 125°C
SN74L90 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input voltages must be zero or positive with respect to network ground terminal.

recommended operating conditions

	SN54L90			SN74L90			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Input count frequency, f_{count}	0			0			MHz
Normalized fan-out from each output, N (see Note 3)			10			10	
Width of input count pulse, $t_{w(count)}$ (see Figure 6)	200			200			ns
Width of reset pulse, $t_{w(reset)}$	200			200			ns
Operating free-air temperature, T_A	−55	25	125	0	25	70	°C

NOTE 3: Fan-out capability from output Q_A to input BD and ten additional TTL loads is guaranteed.

electrical characteristics over recommended operating free-air temperature range

PARAMETER			TEST FIGURE	TEST CONDITIONS†		MIN	MAX	UNIT
V_{IH}	High-level input voltage		1 and 2			2		V
V_{IL}	Low-level input voltage						0.7	V
V_{OH}	High-level output voltage		2	V_{CC} = MIN, V_{IH} = 2 V,	I_{OH} = −100 μA, V_{IL} = 0.7 V	2.4		V
V_{OL}	Low-level output voltage		1	V_{CC} = MIN, V_{IH} = 2 V,	I_{OL} = 2 mA, V_{IL} = 0.7 V		0.3	V
I_I	Input current at maximum input voltage	Any reset input	3	V_{CC} = MAX,	V_I = 5.5 V		100	μA
		A input					300	
		BD input					600	
I_{IH}	High-level input current	Any reset input	3	V_{CC} = MAX,	V_I = 2.4 V		10	μA
		A input					30	
		BD input					60	
I_{IL}	Low-level input current	Any reset input	4	V_{CC} = MAX,	V_I = 0.3 V		−0.18	mA
		A input					−0.54	
		BD input					−1.08	
I_{OS}	Short-circuit output current§		5	V_{CC} = MAX		−3	−15	mA
I_{CC}	Supply current		3	V_{CC} = MAX			7.2	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.
§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum input count frequency				3		MHz
t_{PLH}	Propagation delay time, low-to-high-level output, from input A	6	C_L = 50 pF, R_L = 4 kΩ			340	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from input A	6				340	ns

See mechanical data and ordering instructions starting on page 1-1 of TTL Integrated Circuits Catalog (CC201) or page S1-1 of TTL Catalog Supplement (CC301).

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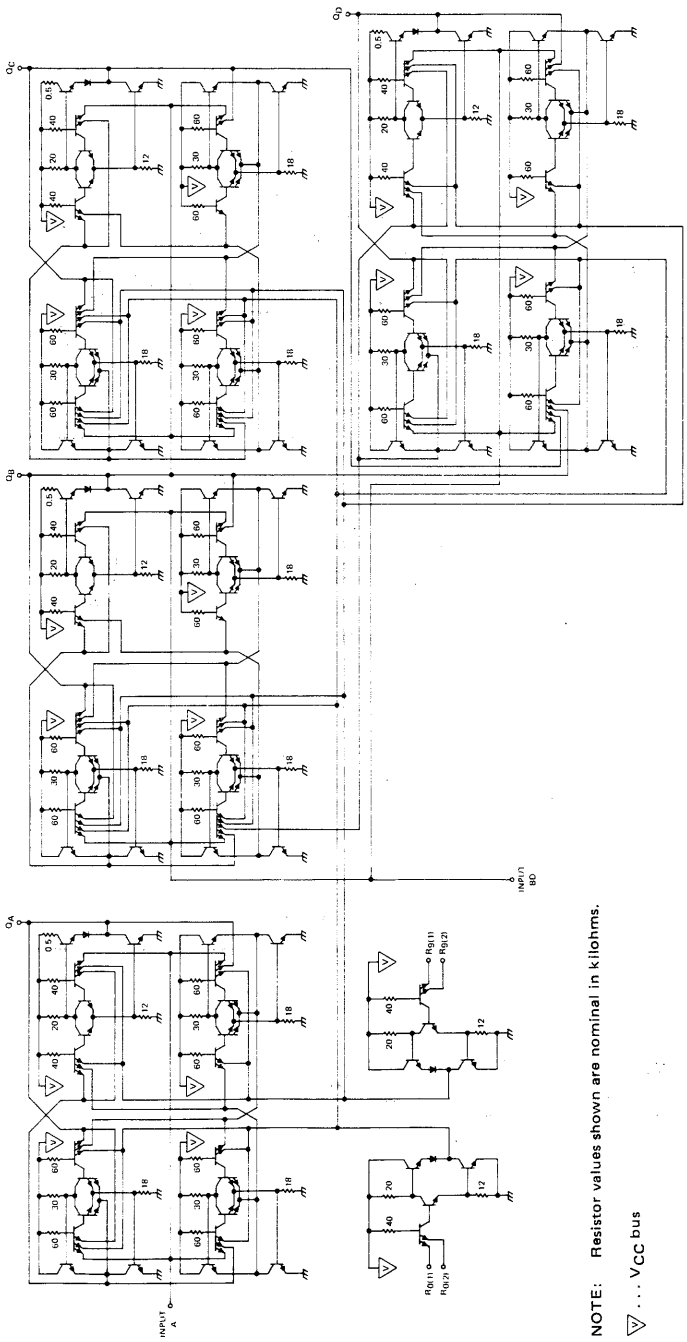
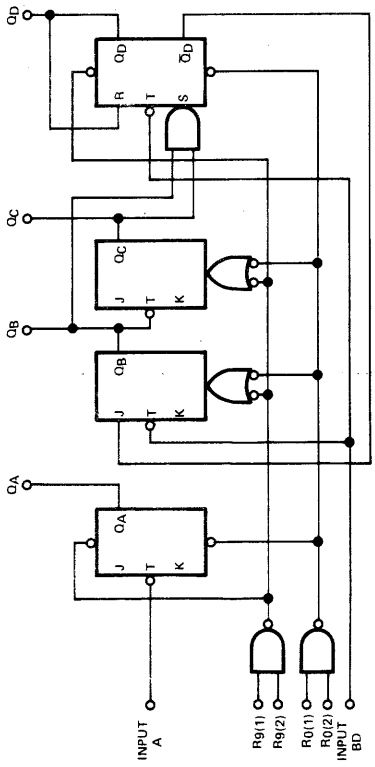
schematic and functional block diagram



NOTE: Resistor values shown are nominal in kilohms.

▽ . . . VCC bus



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PARAMETER MEASUREMENT INFORMATION

d-c test circuits†

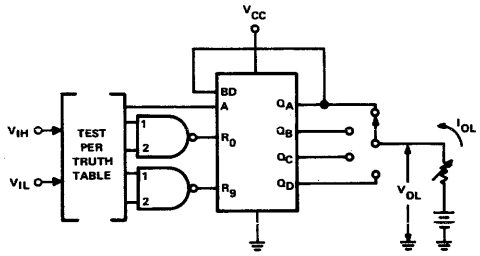


FIGURE 1–V_{IH}, V_{IL}, V_{OL}

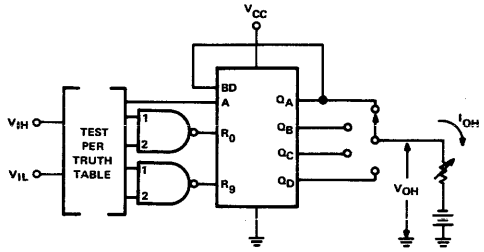
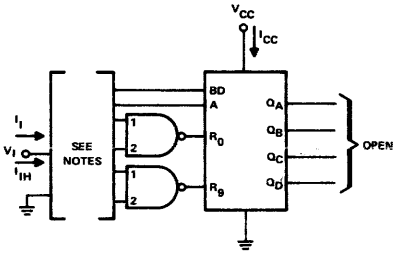
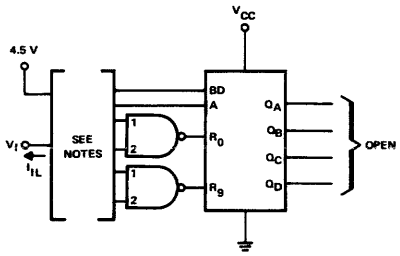


FIGURE 2–V_{IH}, V_{IL}, V_{OH}



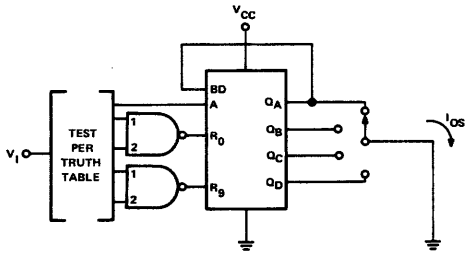
NOTES: A. Each input is tested separately.
B. When testing $R_{0(1)}$ or $R_{9(1)}$, ground $R_{0(2)}$ or $R_{9(2)}$ respectively and vice versa.
C. When testing I_{CC}, reset all outputs to low level, then ground all inputs and measure I_{CC}.

FIGURE 3–I_I, I_{IH}, I_{CC}



NOTES: A. Each input is tested separately.
B. When testing $R_{0(1)}$ or $R_{9(1)}$, apply 4.5 V to $R_{0(2)}$ or $R_{9(2)}$ respectively and vice versa.

FIGURE 4–I_{IL}



Each output is tested at the high level.

FIGURE 5–I_{OS}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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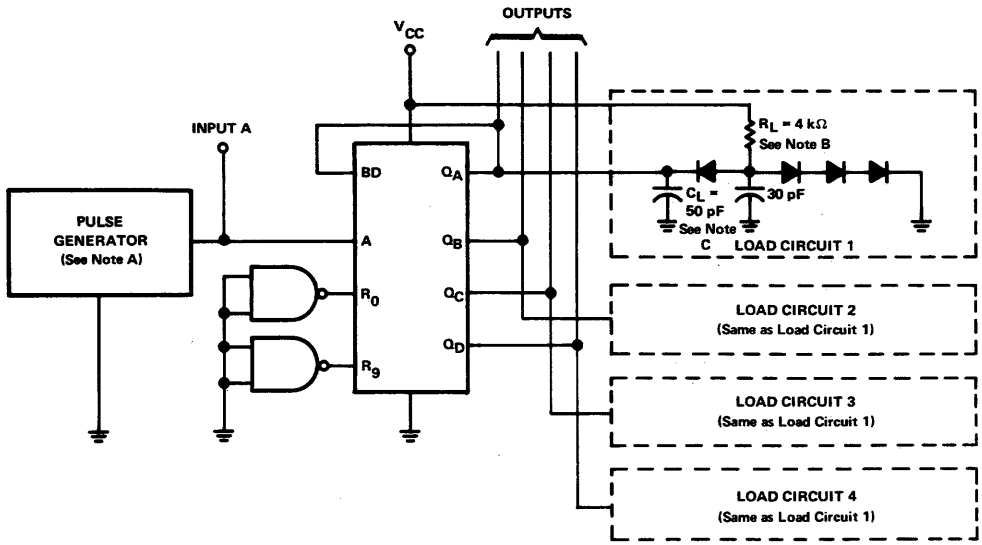
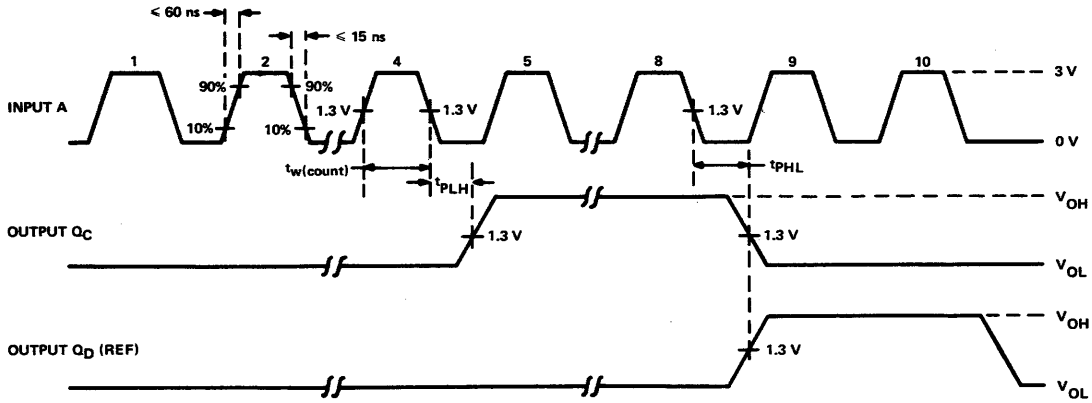
PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: t_w = 1 μs, PRR = 500 kHz, $Z_{out} \approx 50\ \Omega$.
B. All diodes are 1N3064.
C. C_L includes probe and jig capacitance.

FIGURE 6–SWITCHING TIMES

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TEXAS INSTRUMENTS
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CIRCUIT TYPES SN5492,SN7492
DIVIDE-BY-TWELVE COUNTERS
(DIVIDE-BY-TWO AND DIVIDE-BY-SIX)

MSI TTL HIGH-SPEED COUNTERS

for applications in

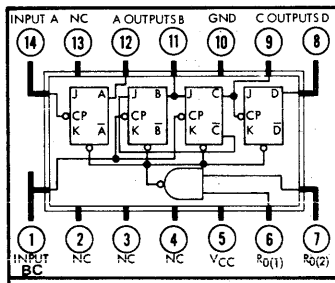
- Digital Computer Systems
- Data-Handling Systems
- Control Systems

logic

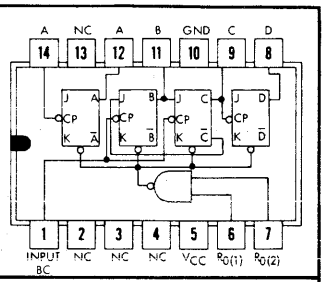
TRUTH TABLE (See Notes 1, 2, and 3)

COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	1	0	0	0
7	1	0	0	1
8	1	0	1	0
9	1	0	1	1
10	1	1	0	0
11	1	1	0	1

W
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: see truth table

NC—No Internal Connection

NOTES: 1. Output A connected to input B
2. To reset all outputs to logical 0 both $R_{0(1)}$ and $R_{0(2)}$ inputs must be at logical 1.
3. Either (or both) reset inputs $R_{0(1)}$ and $R_{0(2)}$ must be at a logical 0 to count.

description

These high-speed, monolithic 4-bit binary counters consist of four master slave flip-flops which are internally interconnected to provide a divide-by-two counter and a divide-by-six counter. A gated direct reset line is provided which inhibits the count inputs and simultaneously returns the four flip-flop outputs to a logical 0. As the output from flip-flop A is not internally connected to the succeeding flip-flops, the counter may be operated in two independent modes:

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1. When used as a divide-by-twelve counter, output A must be externally connected to input BC. The input count pulses are applied to input A. Simultaneous divisions of 2, 6, and 12 are performed at the A, C, and D outputs as shown in the truth table above.

2. When used as a divide-by-six counter, the input count pulses are applied to input BC. Simultaneously, frequency divisions of 3 and 6 are available at the C and D outputs. Independent use of flip-flop A is available if the reset function coincides with reset of the divide-by-six counter.

These circuits are completely compatible with Series 54/74 TTL and DTL logic families. Average power dissipation is 155 mW.

absolute maximum ratings (over operating temperature range unless otherwise noted)

Supply Voltage V_{CC} (See Note 4) . . . . . 7 V
Input Voltage V_{in} (See Notes 4 and 5) . . . . . 5.5 V
Operating Free-Air Temperature Range: SN5492 Circuits . . . . . −55°C to 125°C
SN7492 Circuits . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

NOTES: 4. These voltage values are with respect to network ground terminal.
5. Input signals must be zero or positive with respect to network ground terminal.

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recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 4): SN5492 Circuits	4.5	5	5.5	V
SN7492 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output (See Note 6)			10	
Width of Input Count Pulse, $t_{p(in)}$	50			ns
Width of Reset Pulse, $t_{p(reset)}$	50			ns

NOTE: 6. Fan-out from output A to input BC and to 10 additional Series 54/74 loads is permitted.

electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	2					0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, I_{load} = −400 μA		2.4			V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, I_{sink} = 16 mA				0.4	V
$I_{in(1)}$	Logical 1 level input current at $R_{0(1)}$ or $R_{0(2)}$ inputs	3	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at input A	3	V_{CC} = MAX, V_{in} = 2.4 V				80	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at input BC	3	V_{CC} = MAX, V_{in} = 2.4 V				160	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(0)}$	Logical 0 level input current at $R_{0(1)}$ or $R_{0(2)}$ inputs	4	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(0)}$	Logical 0 level input current input A	4	V_{CC} = MAX, V_{in} = 0.4 V				−3.2	mA
$I_{in(0)}$	Logical 0 level input current at input BC	4	V_{CC} = MAX, V_{in} = 0.4 V				−6.4	mA
I_{OS}	Short-circuit output current§	5	V_{CC} = MAX, V_{out} = 0	SN5492	−20		−57	mA
				SN7492	−18		−57	mA
I_{CC}	Supply current	3	V_{CC} = MAX, V_{in} = 4.5 V	SN5492		31	44	mA
				SN7492		31	51	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the particular circuit type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

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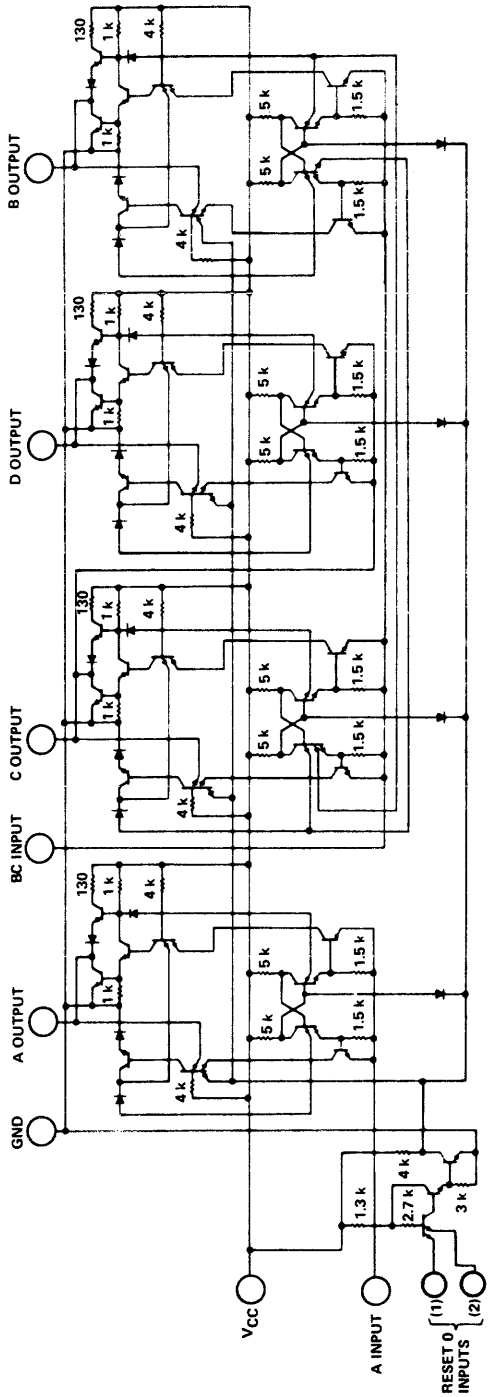
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum frequency of input count pulses		C_L = 15 pF, R_L = 400 Ω	10	18		MHz
t_{pd1}	Propagation delay time to logical 1 level from input count pulse to output D	6	C_L = 15 pF, R_L = 400 Ω		60	100	ns
t_{pd0}	Propagation delay time to logical 0 level from input count pulse to output D	6	C_L = 15 pF, R_L = 400 Ω		60	100	ns

CIRCUIT TYPES SN5492,SN7492
DIVIDE-BY-TWELVE COUNTERS
(DIVIDE-BY-TWO AND DIVIDE-BY-SIX)

schematic

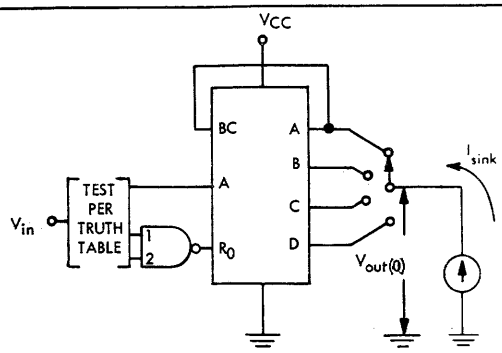


Component values shown are nominal.
Resistor values are in ohms.

9

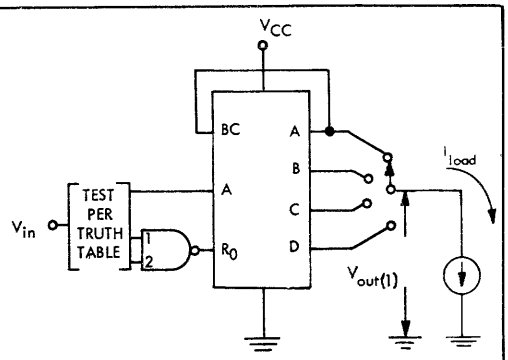
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



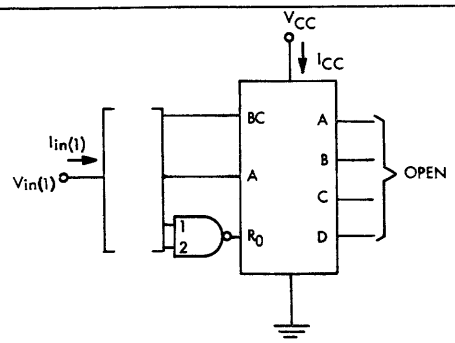
1. Each output is tested in the logical 0 state.

FIGURE 1



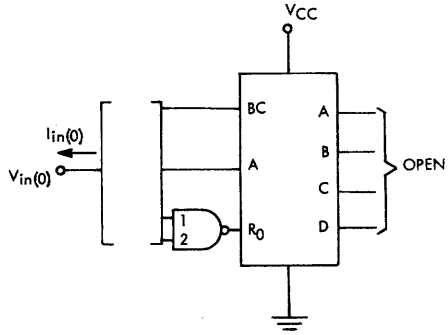
1. Each output is tested in the logical 1 state.

FIGURE 2



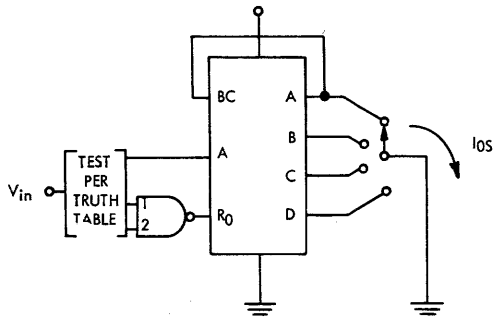
1. Each input is tested separately.
2. When testing $R_{0(1)}$ ground $R_{0(2)}$.
3. When testing $R_{0(2)}$ ground $R_{0(1)}$.
4. When testing I_{CC} reset all outputs to logical 0, ground all inputs, then measure I_{CC}.

FIGURE 3



1. Each input is tested separately.
2. When testing $R_{0(1)}$ apply 4.5 V to $R_{0(2)}$.
3. When testing $R_{0(2)}$ apply 4.5 V to $R_{0(1)}$.

FIGURE 4



1. Each output is tested in the logical 1 state.

FIGURE 5

†Arrows indicate actual direction of current flow

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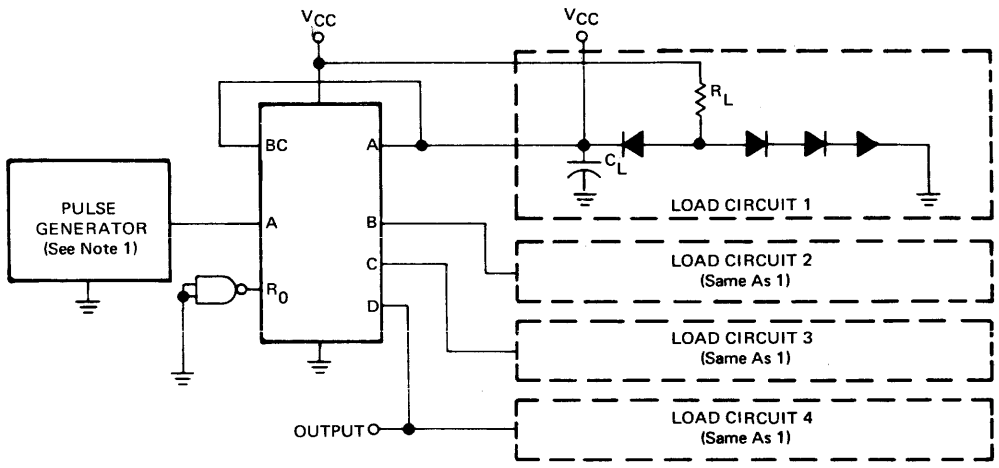
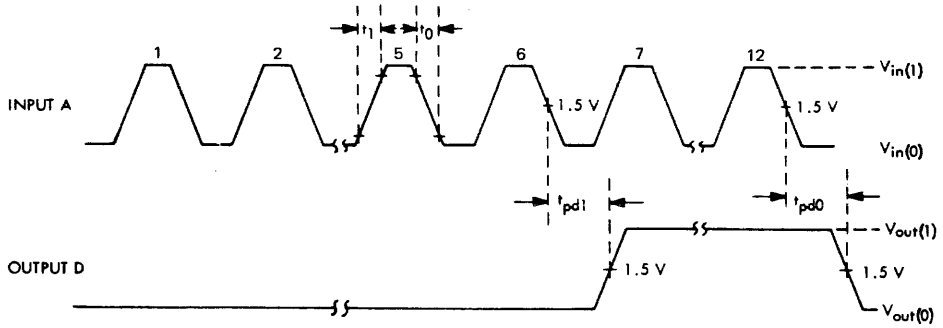
switching characteristics — PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: 1. The pulse generator has the following characteristics: V_{gen} = 3 V, $t_0 = t_1 \leq 15$ ns, t_p = 0.5 μs, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
2. All diodes are 1N3064.
3. C_L includes probe and jig capacitance.
4. $t_{pd} = \frac{t_{pd0} + t_{pd1}}{2}$
5. Voltage values are with respect to ground terminal.

FIGURE 6–SWITCHING TIMES

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CIRCUIT TYPES SN5493, SN7493
4-BIT BINARY COUNTERS

MSI TTL HIGH-SPEED RIPPLE-THROUGH COUNTERS

for applications in

- Digital Computer Systems
- Data-Handling Systems
- Control Systems

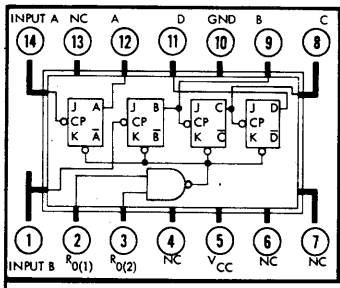
logic

TRUTH TABLE (See Notes 1, 2, and 3)

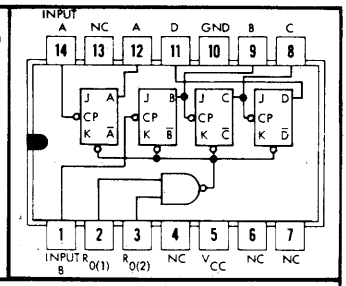
COUNT	OUTPUT D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

NOTES: 1. Output A connected to input B
2. To reset all outputs to logical 0 both $R_{0(1)}$ and $R_{0(2)}$ inputs must be at logical 1.
3. Either (or both) reset inputs $R_{0(1)}$ and $R_{0(2)}$ must be at a logical 0 to count.

W
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: see truth table

NC—No Internal Connection

description

These high-speed, monolithic 4-bit binary counters consist of four master-slave flip-flops which are internally interconnected to provide a divide-by-two counter and a divide-by-eight counter. A gated direct reset line is provided which inhibits the count inputs and simultaneously returns the four flip-flop outputs to a logical 0. As the output from flip-flop A is not internally connected to the succeeding flip-flops the counter may be operated in two independent modes:

1. When used as a 4-bit ripple-through counter, output A must be externally connected to input B. The input count pulses are applied to input A. Simultaneous divisions of 2, 4, 8, and 16 are performed at the A, B, C, and D outputs as shown in the truth table above.

2. When used as a 3-bit ripple-through counter, the input count pulses are applied to input B. Simultaneous frequency divisions of 2, 4, and 8 are available at the B, C, and D outputs. Independent use of flip-flop A is available if the reset function coincides with reset of the 3-bit ripple-through counter.

These circuits are completely compatible with Series 54/74 TTL and DTL logic families. Average power dissipation is 40 mW per flip-flop (160 mW total).

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absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 4)		7 V
Input Voltage, V_{in} (See Notes 4 and 5)		5.5 V
Operating Free-Air Temperature Range:	SN5493 Circuits	−55°C to 125°C
	SN7493 Circuits	0°C to 70°C
Storage Temperature Range		−65°C to 150°C

NOTES: 4. These voltage values are with respect to network ground terminal.
5. Input signals must be zero or positive with respect to network ground terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 4): SN5493 Circuits	4.5	5	5.5	V
SN7493 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output (See Note 6)			10	
Width of Input Count Pulse, $t_{p(in)}$	50			ns
Width of Reset Pulse, $t_{p(reset)}$	50			ns

NOTE: 6. Fan-out from output A to input B and to 10 additional Series 54/74 loads is permitted.

electrical characteristics over recommended operating temperature range (unless otherwise noted)

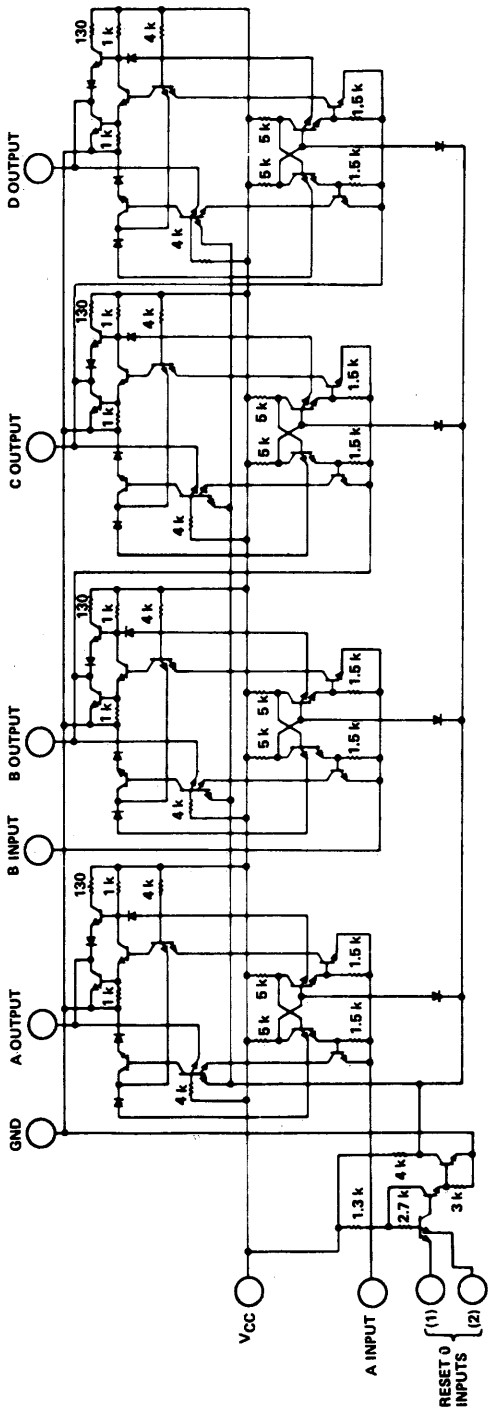
PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	2					0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, I_{load} = −400 μA		2.4			V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, I_{sink} = 16 mA				0.4	V
$I_{in(1)}$	Logical 1 level input current at $R_{0(1)}$ or $R_{0(2)}$ inputs	3	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at A or B inputs	3	V_{CC} = MAX, V_{in} = 2.4 V				80	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(0)}$	Logical 0 level input current at $R_{0(1)}$ or $R_{0(2)}$ inputs	4	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(0)}$	Logical 0 level input current at A or B inputs	4	V_{CC} = MAX, V_{in} = 0.4 V				−3.2	mA
I_{OS}	Short-circuit output current§	5	V_{CC} = MAX, V_{out}=0	SN5493	−20		−57	mA
				SN7493	−18		−57	mA
I_{CC}	Supply current	3	V_{CC} = MAX, V_{in} = 4.5 V	SN5493		32	46	mA
				SN7493		32	53	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum frequency of input count pulses		C_L = 15 pF, R_L = 400 Ω	10	18		MHz
t_{pd1}	Propagation delay time to logical 1 level from input count pulse to output D	6	C_L = 15 pF, R_L = 400 Ω		75	135	ns
t_{pd0}	Propagation delay time to logical 0 level from input count pulse to output D	6	C_L = 15 pF, R_L = 400 Ω		75	135	ns

schematic

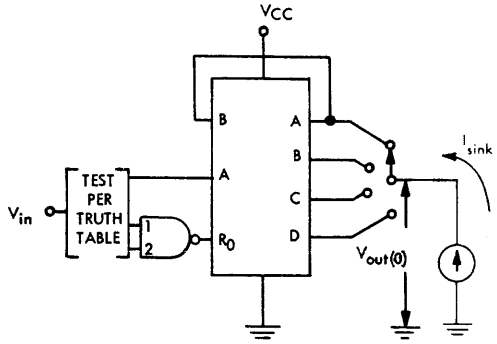


Component values shown are nominal.
Resistor values are in ohms.

9

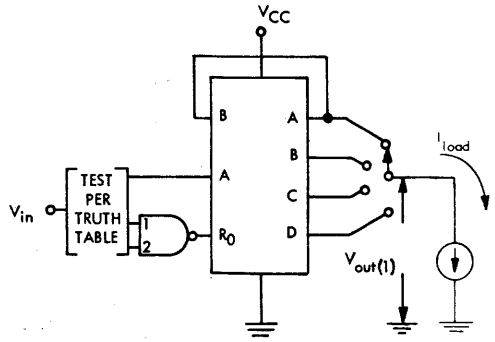
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



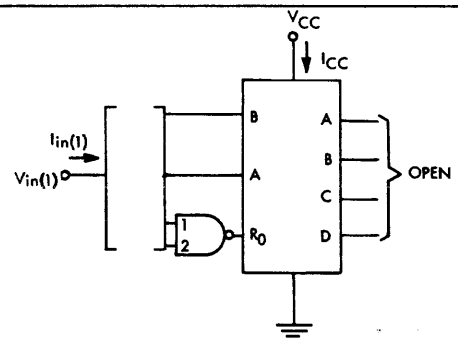
1. Each output is tested in the logical 0 state.

FIGURE 1



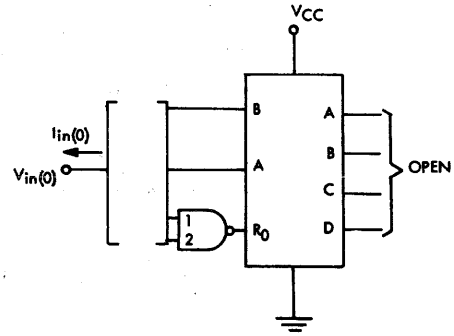
1. Each output is tested in the logical 1 state.

FIGURE 2



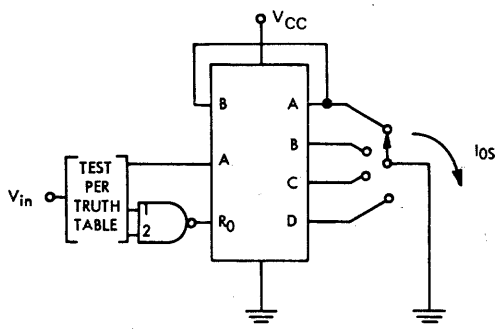
1. Each input is tested separately.
2. When testing $R_{0(1)}$ ground $R_{0(2)}$.
3. When testing $R_{0(2)}$ ground $R_{0(1)}$.
4. When testing I_{CC} all inputs and outputs are open.

FIGURE 3



1. Each input is tested separately.
2. When testing $R_{0(1)}$ apply 4.5 V to $R_{0(2)}$.
3. When testing $R_{0(2)}$ apply 4.5 V to $R_{0(1)}$.

FIGURE 4



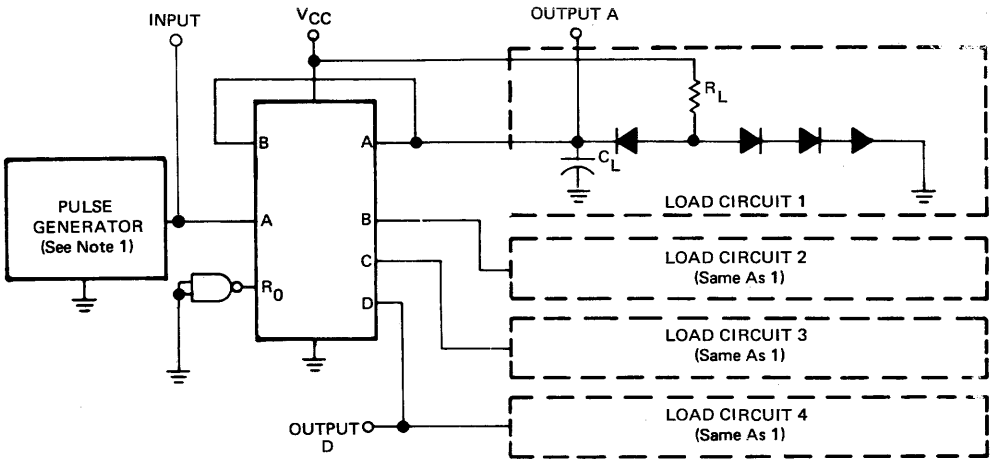
1. Each output is tested in the logical 1 state.

FIGURE 5

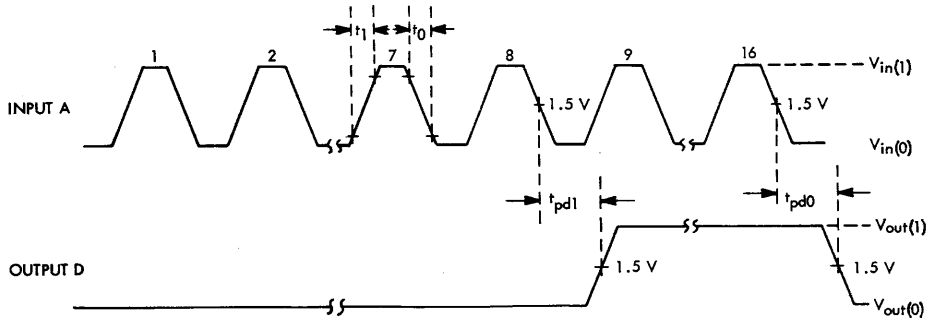
†Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: 1. The pulse generator has the following characteristics: V_{gen} = 3 V, $t_0 = t_1 \leqslant 15$ ns, t_p = 0.5 μs, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
2. All diodes are 1N3064
3. C_L includes probe and jig capacitance.
4. $t_{pd} = \frac{t_{pd0} + t_{pd1}}{2}$
5. Voltage values are with respect to ground terminal.

FIGURE 6–SWITCHING TIMES

9

CIRCUIT TYPES SN54L93, SN74L93
4-BIT BINARY COUNTERS

A SERIES 54L/74L TTL LOW-POWER RIPPLE-THROUGH COUNTER FOR APPLICATIONS IN

● Digital Computer Systems ● Data-Handling Systems ● Control Systems

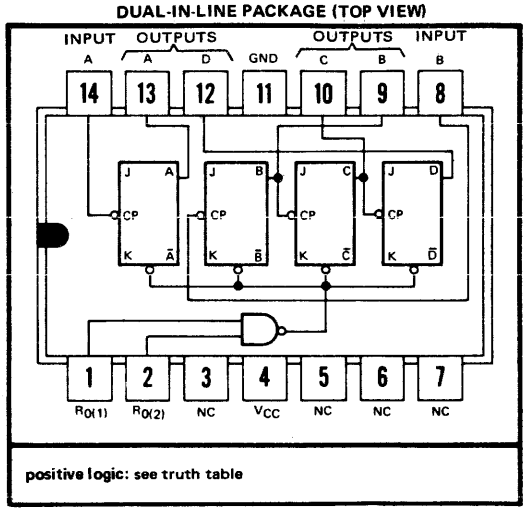
logic

TRUTH TABLE (See Notes 1 and 2)

COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

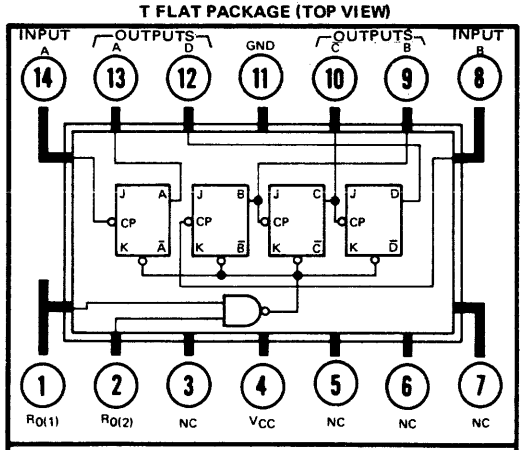
NOTES: 1. Output A connected to input B.
2. To reset all outputs to logical 0 both $R_{0(1)}$ and $R_{0(2)}$. Inputs must be at a logical 1.
3. Either (or both) reset inputs $R_{0(1)}$ and $R_{0(2)}$ must be at a logical 0 to count.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: see truth table

T FLAT PACKAGE (TOP VIEW)



positive logic: see truth table

NC—No Internal Connection

description

The SN54L93/SN74L93 are low-power TTL monolithic 4-bit binary counters consisting of four master-slave flip-flops which are internally interconnected to provide a divide-by-two counter and a divide-by-eight counter. A gated direct reset line is provided which inhibits the count inputs and simultaneously returns the four flip-flop outputs to a logical 0. As the output from flip-flop A is not internally connected to the succeeding flip-flops the counter may be operated in two independent modes:

1. When used as a 4-bit ripple-through counter, output A must be externally connected to input B. The input count pulses are applied to input A. Simultaneous divisions of 2, 4, 8, and 16 are performed at the A, B, C, and D outputs as shown in the truth table above.
2. When used as a 3-bit ripple-through counter, the input count pulses are applied to input B. Simultaneous frequency divisions of 2, 4, and 8 are available at the B, C, and D outputs. Independent use of flip-flop A is available if the reset function coincides with reset of the 3-bit ripple-through counter.

The SN54L93/SN74L93 is completely compatible with TTL and DTL logic families. Average power dissipation is typically 16 mW.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 4) . . . . . 8 V
Input Voltage, V_{in} (See Notes 4 and 5) . . . . . 5.5 V
Operating Free Air Temperature Ranges: SN54L93 Circuits . . . . . −55°C to 125°C
SN74L93 Circuits . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

NOTES: 4. These voltage values are with respect to network ground terminal.
5. Input signals must be zero or positive with respect to network ground terminal.

recommended operating conditions

Supply Voltage V_{CC}: SN54L93 Circuits . . . . . 4.5 V to 5.5 V
SN74L93 Circuits . . . . . 4.75 V to 5.25 V
Maximum Normalized Fan-Out From Each Output (See Note 6) 10
Width of Input Count Pulse, $t_{p(in)}$ . . . . . ⩾ 200 ns
Width of Reset Pulse, $t_{p(reset)}$ . . . . . ⩾ 200 ns

NOTE: 6. Fan-out from output A to input B and to 10 additional Series 54L/74L loads is permitted.

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 of any input	1		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 of any input	2				0.7	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, I_{load} = −100 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, I_{sink} = 2 mA			0.3	V
$I_{in(1)}$	Logical 1 level input current at $R_{0(1)}$ or $R_{0(2)}$ inputs	3	V_{CC} = MAX, V_{in} = 2.4 V			10	μA
			V_{CC} = MAX, V_{in} = 5.5 V			100	μA
$I_{in(1)}$	Logical 1 level input current at A or B inputs	3	V_{CC} = MAX, V_{in} = 2.4 V			20	μA
			V_{CC} = MAX, V_{in} = 5.5 V			200	μA
$I_{in(0)}$	Logical 0 level input current at $R_{0(1)}$ or $R_{0(2)}$ inputs	4	V_{CC} = MAX, V_{in} = 0.3 V			−0.18	mA
$I_{in(0)}$	Logical 0 level input current at A or B inputs	4	V_{CC} = MAX, V_{in} = 0.3 V			−0.36	mA
I_{OS}	Short-circuit output current	5	V_{CC} = MAX, V_{out} = 0	−3		−15	mA
I_{CC}	Supply current	3	V_{CC} = MAX		3.2	6.6	mA

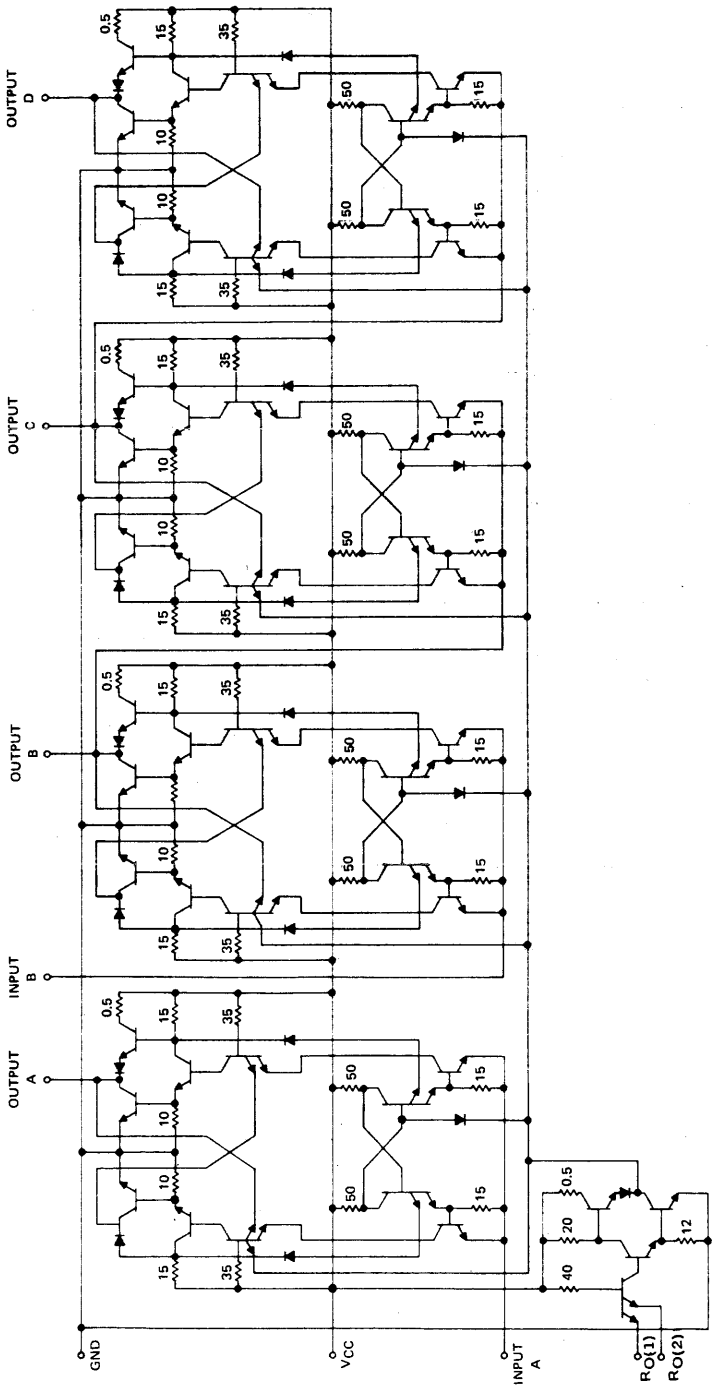
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ These typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum frequency of input count pulses		C_L = 50 pF, R_L = 4 kΩ		3		MHz
t_{pd1}	Propagation delay time to logical 1 level from input count pulse to output D	6	C_L = 50 pF, R_L = 4 kΩ		280	450	ns
t_{pd0}	Propagation delay time to logical 0 level from input count pulse to ouput D	6	C_L = 50 pF, R_L = 4 kΩ		280	450	ns

9

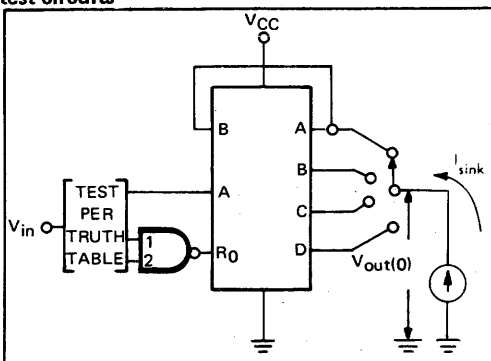
schematic



NOTES: 1. Component values shown are nominal.
2. All resistor values are in kΩ.

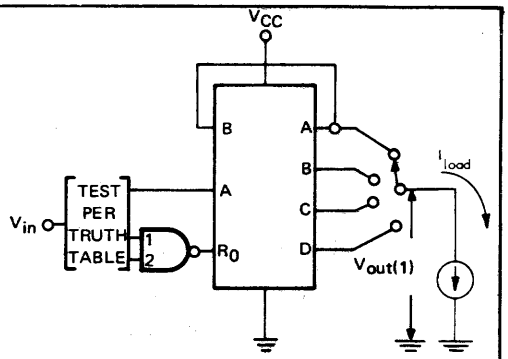
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



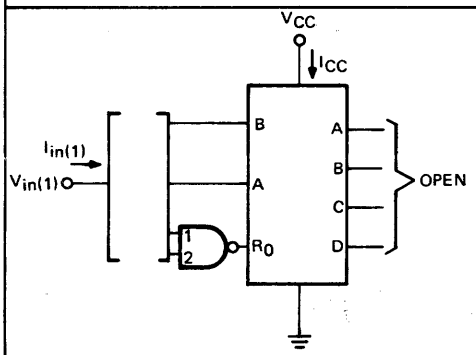
1. Each output is tested in the logical 0 state.

FIGURE 1



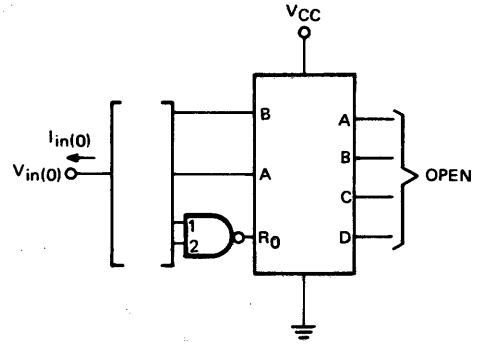
1. Each output is tested in the logical 1 state.

FIGURE 2



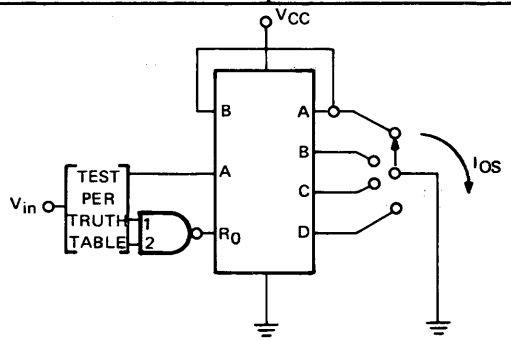
1. Each input is tested separately.
2. When testing $R_{0(1)}$ ground $R_{0(2)}$.
3. When testing $R_{0(2)}$ ground $R_{0(1)}$.
4. When testing I_{CC} all inputs and outputs are open.

FIGURE 3



1. Each input is tested separately.
2. When testing $R_{0(1)}$ apply 4.5 V to $R_{0(2)}$.
3. When testing $R_{0(2)}$ apply 4.5 V to $R_{0(1)}$.

FIGURE 4



1. Each output is tested in the logical 1 state.

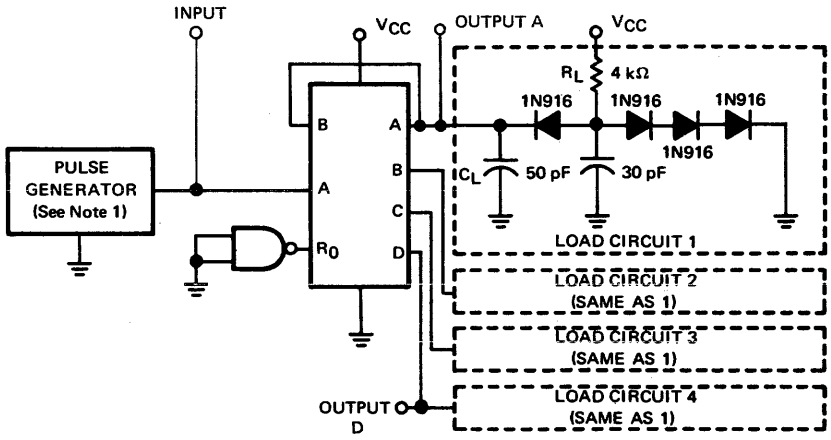
FIGURE 5

† Arrows indicate actual direction of current flow.

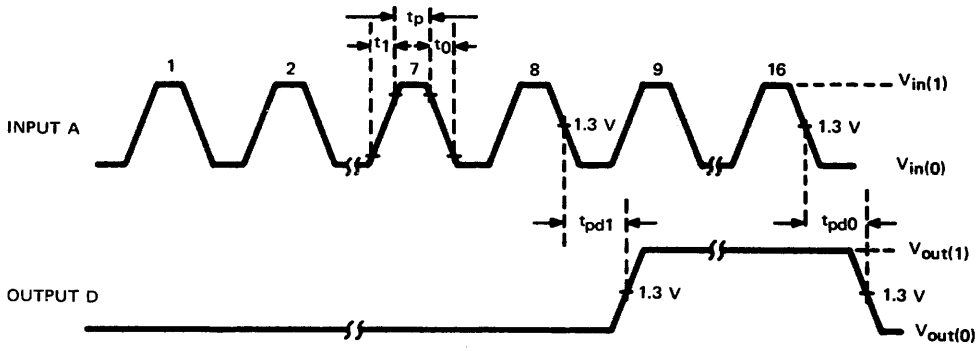
9

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: 1. The pulse generator has the following characteristics: $t_0 = t_1 = 15$ ns, PRR ≤ 500 kHz, $t_p \geq 200$ ns, and $Z_{out} \approx 50\ \Omega$.
2. Voltage values are with respect to network ground terminal.
3. C_L includes probe and jig capacitance.

FIGURE 6 – SWITCHING TIMES

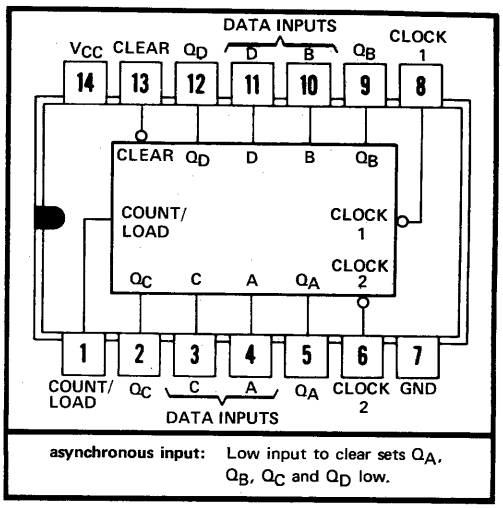
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN54196, SN54197, SN74196, SN74197
50-MHz PRESETTABLE DECADE AND BINARY COUNTERS/LATCHES

CIRCUIT TYPES SN54196, SN54197, SN74196, SN74197
BULLETIN NO. DL-S 7111369, OCTOBER 1970
REVISED JANUARY 1971

- Performs BCD, Bi-Quinary, or Binary Counting
- Fully Programmable
- Fully Independent Clear Input
- Guaranteed to Count at Input Frequencies from 0 to 50 MHz
- Input Clamping Diodes Simplify System Design
- Output Q_A Will Drive Clock-2 Input Plus Ten Series 54/74 Loads

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)†



†Pin assignments for these circuits are the same for all packages.

description

These high-speed monolithic counters consist of four d-c coupled, master-slave flip-flops which are internally interconnected to provide either a divide-by-two and a divide-by-five counter (SN54196, SN74196) or a divide-by-two and a divide-by-eight counter (SN54197, SN74197). These four counters are fully programmable; that is, the outputs may be preset to any state by placing a low on the count/load input and entering the desired data at the data inputs. The outputs will change to agree with the data inputs independent of the state of the clocks.

These counters may also be used as 4-bit latches by using the count/load input as the strobe and entering data at the data inputs. The outputs will directly follow the data inputs when the count/load is low, but will remain unchanged when the count/load is high and the clock inputs are inactive.

These high-speed counters will accept count frequencies of 0 to 50 megahertz at the clock-1 input and 0 to 25 megahertz at the clock-2 input. During the count operation, transfer of information to the ouputs occurs on the negative-going edge of the clock pulse. These counters feature a direct clear which, when taken low, sets all outputs low regardless of the states of the clocks.

All inputs are diode-clamped to minimize transmission-line effects and simplify system design. These circuits are compatible with most TTL and DTL logic families. Typical power dissipation is 240 milliwatts. The SN54196 and SN54197 circuits are characterized for operation over the full military temperature range of −55°C to 125°C; the SN74197 and SN74197 circuits are characterized for operation from 0°C to 70°C.

typical count configurations

SN54196 and SN74196

The output of flip-flop A is not internally connected to the succeeding flip-flops; therefore, the count may be operated in three independent modes:

1. When used as a binary-coded-decimal decade counter, the clock-2 input must be externally connected to the Q_A output. The clock-1 input receives the incoming count, and a count sequence is obtained in accordance with the BCD count sequence truth table shown at the right.
2. If a symmetrical divide-by-ten count is desired for frequency synthesizers (or other applications requiring division of a binary count by a power of ten), the Q_D output must be externally connected to the clock-1 input. The input count is then applied at the clock-2 input and a divide-by-ten square wave is obtained at output Q_A in accordance with the bi-quinary truth table above.

SN54196, SN74196
TRUTH TABLES

DECADE (BCD)
(See Note A)

COUNT	OUTPUT Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

BI-QUINARY (5-2)
(See Note B)

COUNT	OUTPUT Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

NOTES: A. Output Q_A connected to clock-2 input.
B. Output Q_D connected to clock-1 input.

3. For operation as a divide-by-two counter and a divide-by-five counter, no external interconnections are required. Flip-flop A is used as a binary element for the divide-by-two function. The clock-2 input is used to obtain binary divide-by-five operation at the Q_B, Q_C, and Q_D outputs. In this mode, the two counters operate independently; however, all four flip-flops are loaded and cleared simultaneously.

SN54197 and SN7419[illegible]

The output of flip-flop A is not internally connected to the succeeding flip-flops, therefore the counter may be operated in two independent modes:

1. When used as a high-speed 4-bit ripple-through counter, output Q_A must be externally connected to the clock-2 input. The input count pulses are applied to the clock-1 input. Simultaneous divisions by 2, 4, 8, and 16 are performed at the Q_A, Q_B, Q_C, Q_D output as shown in the truth table at right.
2. When used as a 3-bit ripple-through counter, the input count pulses are applied to the clock-2 input. Simultaneous frequency divisions by 2, 4, and 8 are available at the Q_B, Q_C, and Q_D outputs. Independent use of flip-flop A is available if the load and clear functions coincide with those of the 3-bit ripple-through counter.

SN54197, SN74197
TRUTH TABLE
(See Note A)

COUNT	OUTPUT Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

NOTE A: Output Q_A connected to clock-2 input.

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TEXAS INSTRUMENTS
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absolute maximum ratings (over operating free-air temperature range unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54196, SN54197 Circuits . . . . . −55°C to 125°C
SN74196, SN74197 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies between the clear and count/load inputs.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	SN54196, SN54197	4.5	5	5.5	V
	SN74196, SN74197	4.75	5	5.25	
Normalized fan-out from each output, N	High logic level			20	
	Low logic level			10	
Count frequency (see Figure 1)	Clock-1 input	0		50	MHz
	Clock-2 input	0		25	
Pulse width, t_w (see Figure 1)	Clock-1 input	10			ns
	Clock-2 input	20			
	Clear	15			
	Load	20			
Input hold time, t_{hold} (see Figure 1)	High-level data	$t_{w(load)}$			
	Low-level data	$t_{w(load)}$			
Input setup time, t_{setup} (see Figure 1)	High-level data	10			ns
	Low-level data	15			
Count enable time, t_{enable} (see Note 3 and Figure 1)		20			ns
Clock input pulse fall time, t_f (see Figure 1)				75	ns
Operating free-air temperature range, T_A	SN54196, SN54197	−55	25	125	°C
	SN74196, SN74197	0	25	70	

NOTE 3: Count enable time is the interval immediately preceding the negative-going edge of the clock pulse during which interval the count/load and clear inputs must be both high to ensure counting.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54196, SN74196			SN54197, SN74197			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_I	Input clamp voltage		V_{CC} = MAX, I_I = −12 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4			2.4			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA¶				0.4			0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current	data, count/load	V_{CC} = MAX, V_I = 2.4 V				40			40	μA
		clear, clock 1					80			80	
		clock 2					120			80	
I_{IL}	Low-level input current	data, count/load	V_{CC} = MAX, V_I = 0.4 V				−1.6			−1.6	mA
		clear					−3.2			−3.2	
		clock 1					−4.8			−4.8	
		clock 2					−6.4			−3.2	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	SN54196, SN54197	−20		−57	−20		−57	mA
				SN74196, SN74197	−18		−57	−18		−57	
I_{CC}	Supply current		V_{CC} = MAX, See Note 4			48	59		48	59	mA

NOTE 4: I_{CC} is measured with all inputs grounded and all outputs open.

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

¶Q_A outputs are tested at I_{OL} = 16 mA plus the limit value of I_{IL} for the clock-2 input. This permits driving the clock-2 input while fanning out to 10 Series 54/74 loads.

§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, R_L = 400 Ω, C_L = 15 pF, T_A = 25°C, N = 10, see figure 1

PARAMETER◊	FROM (INPUT)	TO (OUTPUT)	SN54196, SN74196			SN54197, SN74197			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}			50	70		50	70		MHz
t_{PLH}	Clock 1	Q_A		7	12		7	12	ns
t_{PHL}				10	15		10	15	
t_{PLH}	Clock 2	Q_B		12	18		12	18	ns
t_{PHL}				14	21		14	21	
t_{PLH}	Clock 2	Q_C		24	36		24	36	ns
t_{PHL}				28	42		28	42	
t_{PLH}	Clock 2	Q_D		14	21		36	54	ns
t_{PHL}				12	18		42	63	
t_{PLH}	A, B, C, D	Q_A, Q_B, Q_C, Q_D		16	24		16	24	ns
t_{PHL}				25	38		25	38	
t_{PLH}	Load	Any		22	33		22	33	ns
t_{PHL}				24	36		24	36	
t_{PHL}	Clear	Any		25	37		25	37	ns

◊f_{max} is maximum input count frequency
t_{PLH} is propagation delay time, low-to-high-level output
t_{PHL} is propagation delay time, high-to-low-level output

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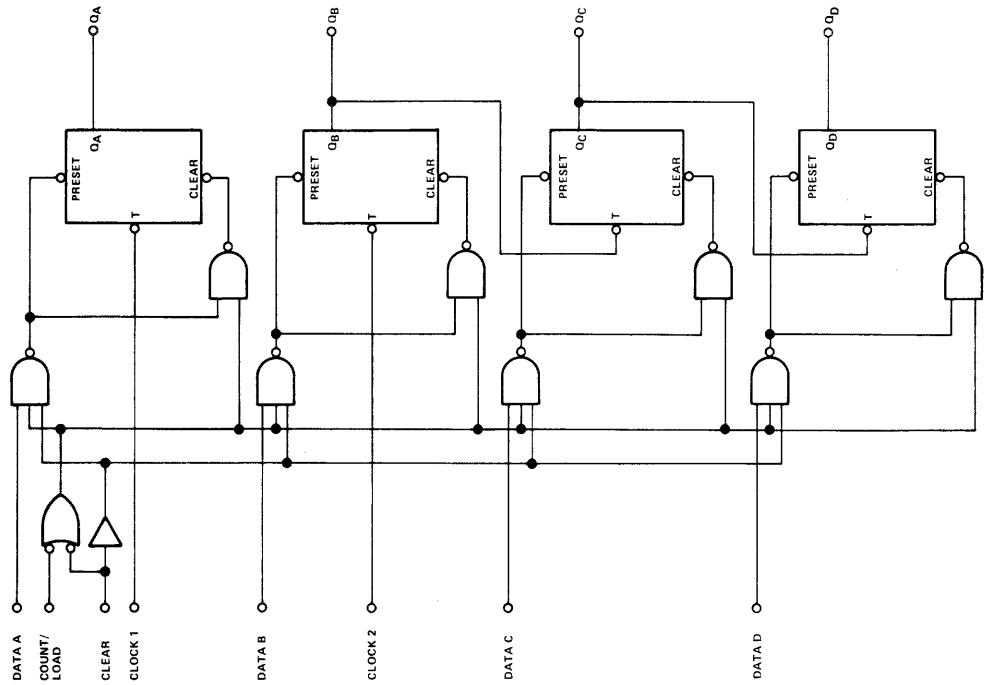
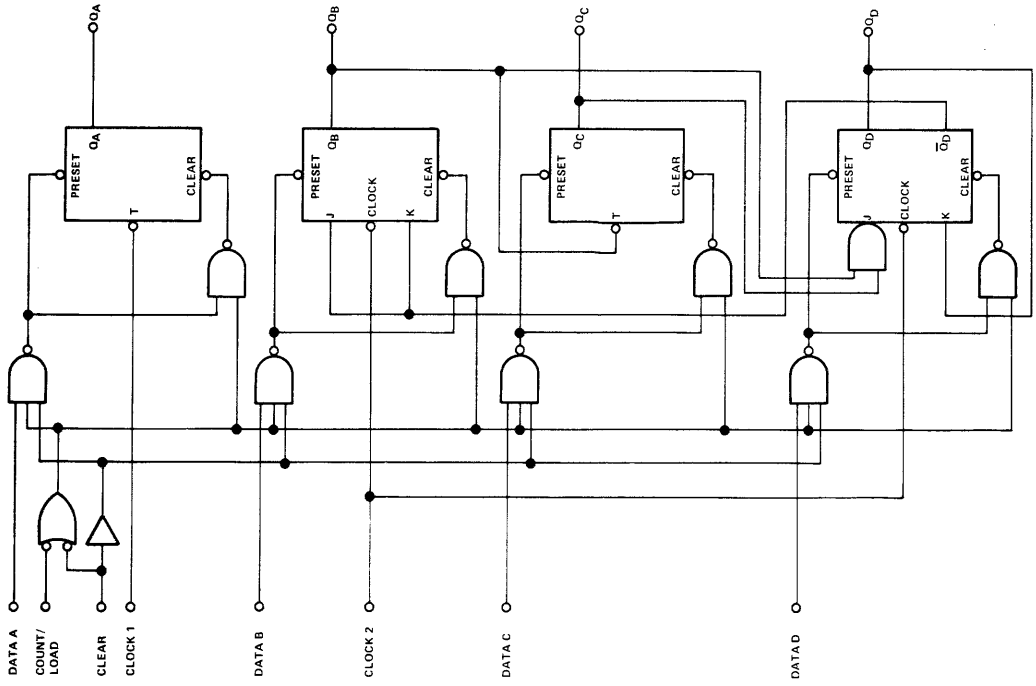
functional block diagrams

SN54197, SN74197



SN54196, SN74196



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070

PARAMETER MEASUREMENT INFORMATION

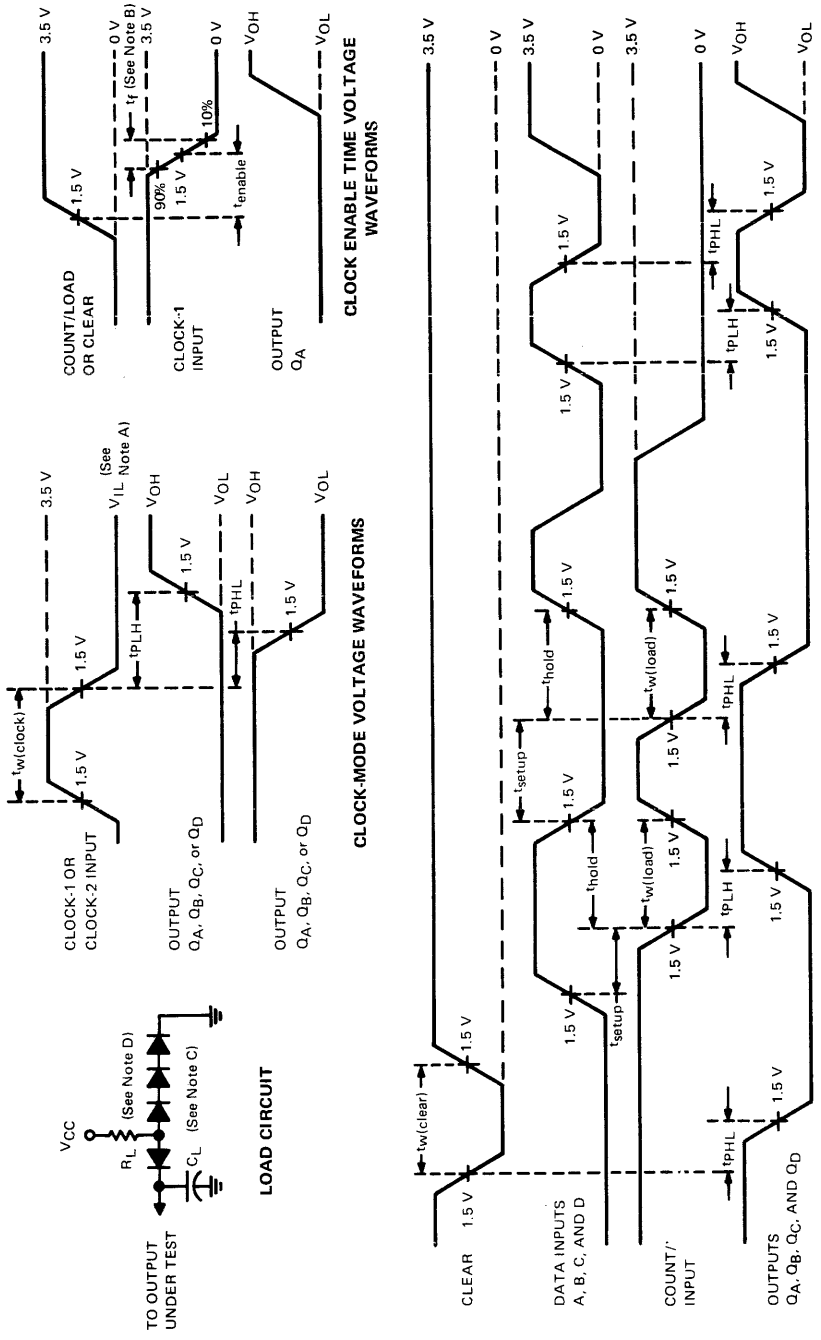

FIGURE 1

NOTES:
A. The input pulse generator has the following characteristics: for testing f_{max}, $V_{IL} = 0.3 \pm 0.1$ V, duty cycle = 50%, $t_r < 5$ ns, and $t_f < 5$ ns; for all other measurements, $V_{IL} = 0$, PRR ≤ 1 MHz, duty cycle ≤ 50%, $t_r < 5$ ns, and unless otherwise specified, $t_f < 5$ ns.
B. Fall time of clock 1 is measured with count/load and clear high. When measuring clock enable time, $t_f < 5$ ns.
C. C_L includes probe and jig capacitance.
D. All diodes are 1N3064.
E. Unless otherwise specified, Q_A is connected to clock 2.

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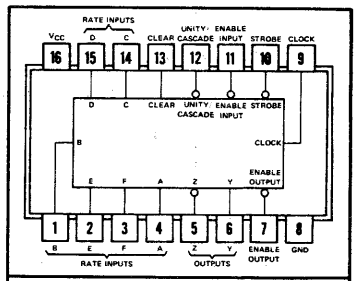
CIRCUIT TYPES SN7497, SN74167
SYNCHRONOUS RATE MULTIPLIERS

SN7497 . . . 6-BIT BINARY MULTIPLIER
SN74167 . . . DECADE MULTIPLIER

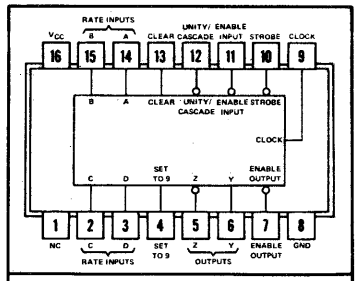
- Perform Fixed-Rate or Variable-Rate Frequency Division
- For Applications in Arithmetic, Radar, Digital-to-Analog (D/A), Analog-to-Digital (A/D), and other Conversion Operations
- Typical Maximum Clock Frequency . . . 32 Megahertz

SN7497
J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



positive logic: See description

SN74167
J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



positive logic: See description

NC—No internal connection

†Pin assignments for these circuits are the same for all packages.

description

These monolithic, fully synchronous, programmable counters utilize Series 54/74 TTL circuitry to achieve 32-megahertz typical maximum operating frequencies. The SN7497 is a six-bit serial binary counter; the SN74167 is a decade counter. These devices have buffered clock, clear, and enable inputs to control the operation of the counter, and a strobe input to enable or inhibit the rate input/decoding AND-OR-INVERT gates. The SN74167 also has a buffered set-to-nine input. The outputs have additional gating for cascading and transferring unity-count rates.

The counter is enabled when the clear, strobe, and enable inputs are low (for the decade counters, set-to-nine is also low). With the counter enabled the output frequency is equal to the input frequency multiplied by the rate input M and divided either by 64 (SN7497) or by 10 (SN74167), ie.:

$$\text{SN7497:}\quad f_{out} = \frac{M \cdot f_{in}}{64}$$

where: $M = F \cdot 2^5 + E \cdot 2^4 + D \cdot 2^3 + C \cdot 2^2 + B \cdot 2^1 + A \cdot 2^0$

$$\text{SN74167:}\quad f_{out} = \frac{M \cdot f_{in}}{10}$$

where: $M = D \cdot 2^3 + C \cdot 2^2 + B \cdot 2^1 + A \cdot 2^0$ for decimal zero through nine.

When the rate input is binary 0 (all rate inputs low), Z remains high. In order to cascade devices to perform 12-bit rate multiplication with the SN7497, or two-decade rate multiplication with the SN74167, the enable output is connected to the enable and strobe inputs of the next stage, the Z output of each stage is connected to the unity/cascade input of the other stage, and the sub-multiple frequency is taken from the Y output.

The unity/cascade input, when connected to the clock input, may be utilized to pass the clock frequency (inverted) to the Y output when the rate input/decoding gates are inhibited by the strobe. The unity/cascade input may also be used as a control for the Y output.

All of the inputs of these counters are diode-clamped, and each input, except the clock input, represents one normalized Series 54/74 load. The buffered clock input, used with the strobe gate, is only two Series 54/74 loads. Full fan-out to 10 Series 54/74 loads is available from each of the outputs. These devices are completely compatible with most TTL and DTL families. Typical power dissipation is 345 milliwatts for the SN7497, and 270 milliwatts for the SN74167. The SN7497 and SN74167 are characterized for operation from 0°C to 70°C.

description (continued)

SN7497

STATE AND/OR RATE TABLE (See Note A)

INPUTS										OUTPUTS			
			BINARY RATE					NUMBER OF	UNITY/	LOGIC LEVEL OR NUMBER OF PULSES			
CLEAR	ENABLE	STROBE	F	E	D	C	B	A	CLOCK PULSES	CASCADE	Y	Z	ENABLE	NOTES
H	X	H	X	X	X	X	X	X	X	H	L	H	H	B
L	L	L	L	L	L	L	L	L	64	H	L	H	1	C
L	L	L	L	L	L	L	L	H	64	H	1	1	1	C
L	L	L	L	L	L	L	H	L	64	H	2	2	1	C
L	L	L	L	L	L	H	L	L	64	H	4	4	1	C
L	L	L	L	L	H	L	L	L	64	H	8	8	1	C
L	L	L	L	H	L	L	L	L	64	H	16	16	1	C
L	L	L	H	L	L	L	L	L	64	H	32	32	1	C
L	L	L	H	H	H	H	H	H	64	H	63	63	1	C
L	L	L	H	H	H	H	H	H	64	L	H	63	1	E
L	L	L	H	L	H	L	L	L	64	H	40	40	1	F

SN74167

STATE AND/OR RATE TABLE (See Note A)

INPUTS								OUTPUTS				
			BCD RATE				NUMBER OF	UNITY/	LOGIC LEVEL OR NUMBER OF PULSES			
CLEAR	ENABLE	STROBE	D	C	B	A	CLOCK PULSES	CASCADE	Y	Z	ENABLE	NOTES
H	X	H	X	X	X	X	X	H	L	H	H	B
L	L	L	L	L	L	L	10	H	L	H	1	C
L	L	L	L	L	L	H	10	H	1	1	1	C
L	L	L	L	L	H	L	10	H	2	2	1	C
L	L	L	L	L	H	H	10	H	3	3	1	C
L	L	L	L	H	L	L	10	H	4	4	1	C
L	L	L	L	H	L	H	10	H	5	5	1	C
L	L	L	L	H	H	L	10	H	6	6	1	C
L	L	L	L	H	H	H	10	H	7	7	1	C
L	L	L	H	L	L	L	10	H	8	8	1	C
L	L	L	H	L	L	H	10	H	9	9	1	C
L	L	L	H	L	H	L	10	H	8	8	1	C, D
L	L	L	H	L	H	H	10	H	9	9	1	C, D
L	L	L	H	H	L	L	10	H	8	8	1	C, D
L	L	L	H	H	L	H	10	H	9	9	1	C, D
L	L	L	H	H	H	L	10	H	8	8	1	C, D
L	L	L	H	H	H	H	10	H	9	9	1	C, D
L	L	L	H	L	L	H	10	L	H	9	1	E

NOTES: A. H = high level, L = low level, X = irrelevant. All remaining entries are numeric counts.

B. This is a simplified illustration of the clear function. The states of clock and strobe can affect the logic level of Y and Z. A low (L) unity/cascade will cause output Y to remain high.

C. Each rate illustrated assumes a constant value at rate inputs; however, these illustrations in no way prohibit variable-rate inputs.

D. These input conditions exceed the range of the decimal rate inputs.

E. Unity/cascade is used to inhibit output Y.

F. $f_{out} = \frac{M \cdot f_{in}}{64} = \frac{(8 + 32)\, f_{in}}{64} = \frac{40\, f_{in}}{64} = 0.625\, f_{in}$

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Normalized fan-out from output, N				10	
Input clock frequency, f_{clock}		0		25	MHz
Width of clock pulse, $t_{w(clock)}$		20			ns
Width of clear pulse, $t_{w(clear)}$		15			ns
Width of set-to-nine pulse $t_{w(set\text{-}to\text{-}9)}$	SN74167	15			ns
Setup time, t_{setup}:	(See Figure 1)				
From positive-going transition of clock pulse		25			ns
From negative-going transition of previous clock pulse		0		$t_{w(clock)}-10$	ns
Hold time, t_{hold}:	(See Figure 1)				
From positive-going transition of clock pulse		0		$t_{w(clock)}-10$	ns
From negative-going transition of previous clock pulse		0		$t_{cp}-10$	ns
Operating free-air temperature, T_A		0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage		V_{CC} = MIN,	I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = −400 μA	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 16 mA			0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	clock input	V_{CC} = MAX,	V_I = 2.4 V			80	μA
		other inputs					40	
I_{IL}	Low-level input current	clock inputs	V_{CC} = MAX,	V_I = 0.4 V			−3.2	mA
		other inputs					−1.6	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−18		−55	mA
I_{CCH}	Supply current, high-level output		V_{CC} = MAX, See Note 2	SN7497		58		mA
				SN74167		43		
I_{CCL}	Supply current, low-level output		V_{CC} = MAX, See Note 3	SN7497		80	120	mA
				SN74167		65	99	

NOTES: 2. I_{CCH} is measured with outputs open and all inputs low.
3. I_{CCL} is measured with outputs open and all inputs high except the set-to-nine input of the SN74167, which is low.

†For test conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time.

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switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER¶	FROM INPUT	TO OUTPUT	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			C_L = 15 pF, R_L = 400 Ω, See Figure 1	25	32		MHz
t_{PLH}	Enable	Enable			13	20	ns
t_{PHL}					14	21	
t_{PLH}	Strobe	Z			12	18	ns
t_{PHL}					15	23	
t_{PLH}	Clock	Y			26	39	ns
t_{PHL}					20	30	
t_{PLH}	Clock	Z			12	18	ns
t_{PHL}					17	26	
t_{PLH}	Rate	Z			9	14	ns
t_{PHL}					6	10	
t_{PLH}	Unity/Cascade	Y			9	14	ns
t_{PHL}					6	10	
t_{PLH}	Strobe	Y			19	30	ns
t_{PHL}					22	33	
t_{PLH}	Clock	Enable			19	30	ns
t_{PHL}					22	33	
t_{PLH}	Clear	Y			24	36	ns
t_{PHL}		Z			15	23	
t_{PHL} (SN74167 only)	Set-to-9	Enable			18	27	ns
t_{PLH}	Any Rate Input	Y			15	23	ns
t_{PHL}					15	23	

¶ f_{max} is maximum input clock frequency.
t_{PLH} is propagation delay time, low-to-high-level output.
t_{PHL} is propagation delay time, high-to-low-level output.

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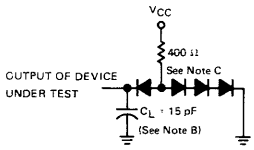
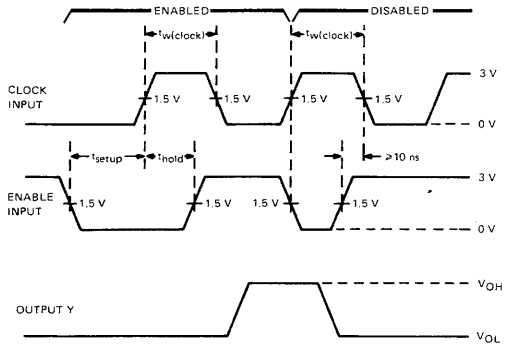
PARAMETER MEASUREMENT INFORMATION

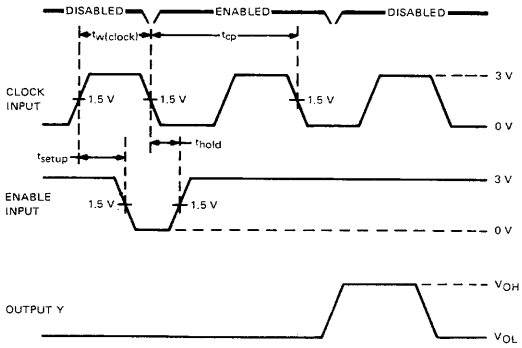


All three outputs are loaded during testing

LOAD CIRCUIT

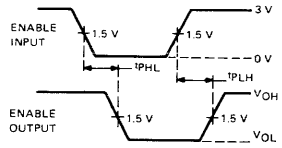


ENABLING FROM POSITIVE-GOING TRANSITION OF CLOCK PULSE



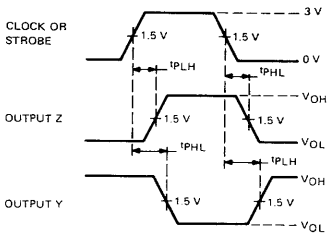
ENABLING FROM NEGATIVE-GOING TRANSITION OF PREVIOUS CLOCK PULSE

1. Unity/cascade and rate inputs are high, other inputs are low, and flip-flops are at any count other than maximum or one count before maximum.
2. Setup and hold times are illustrated for enabling a single clock pulse (count). Continued application of the enable function will enable subsequent clock pulses (counts) until disabling occurs (enable goes high). The total number of counts will be determined by the total number of positive-going clock transitions enabled.



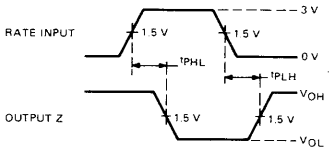
Flip-flops are at the maximum count. Other inputs are low.

PROPAGATION DELAY TIMES, ENABLE INPUT TO ENABLE OUTPUT



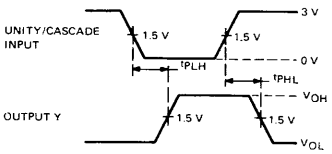
Unity/cascade and rate inputs are high, other inputs are low, and flip-flops are at any count other than maximum.

PROPAGATION DELAY TIMES, CLOCK TO Z AND Y, AND STROBE INPUT TO Z AND Y



Flip-flops are at a count so that all other inputs to the gate under test are high all other inputs, including other rate inputs, are low.

PROPAGATION DELAY TIMES, RATE INPUT TO Z



Output Z is high.

PROPAGATION DELAY TIMES, UNITY/CASCADE INPUT TO Y

NOTES: A. The input pulse generator has the following characteristics: $t_{w(clock)} = 20$ ns, $t_{TLH} \leq 10$ ns, $t_{THL} \leq 10$ ns, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.

FIGURE 1–SWITCHING TIMES

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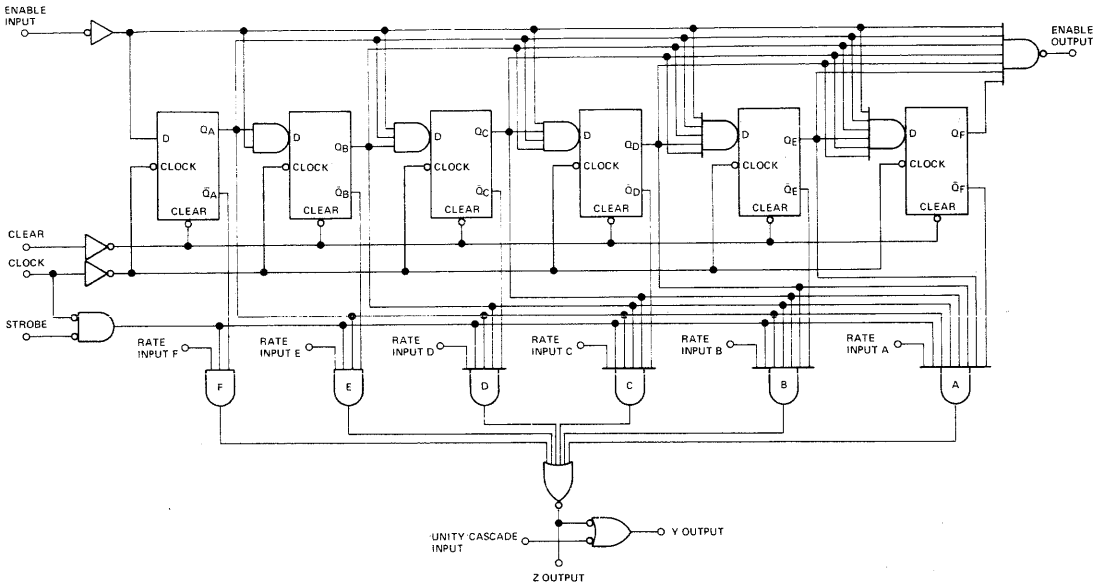
CIRCUIT TYPES SN7497, SN74167
SYNCHRONOUS RATE MULTIPLIERS

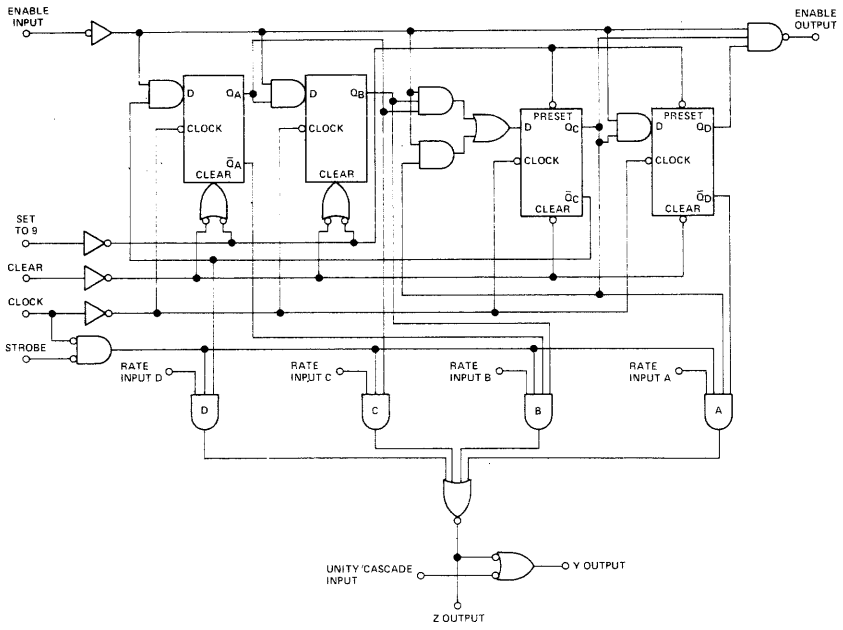
SN7497 BINARY COUNTER

functional block diagram



SN74167 DECADE COUNTER

functional block diagram



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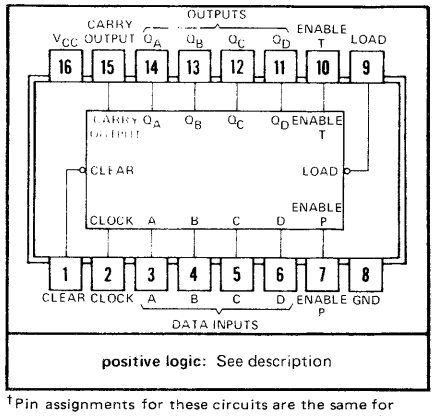
CIRCUIT TYPES SN54160 THRU SN54163, SN74160 THRU SN74163
SYNCHRONOUS 4-BIT COUNTERS

SN54160, SN54161, SN74160, SN74161, . . . SYNCHRONOUS COUNTERS WITH DIRECT CLEAR
SN54162, SN54163, SN74162, SN74163 . . . FULLY SYNCHRONOUS COUNTERS

- Internal Look-Ahead for Fast Counting Schemes
- Carry Output for n-Bit Cascading
- Synchronous Counting
- Synchronously Programmable
- Load Control Line
- Diode-Clamped Inputs
- Typical Maximum Input Clock Frequency . . . 32 MHz

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



positive logic: See description

†Pin assignments for these circuits are the same for all packages.

description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting schemes. The SN54160, SN54162, SN74160, and SN74162 are decade counters and the SN54161, SN54163, SN74161, and SN74163 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four J-K master-slave flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either state. As presetting is synchronous, placing a low level on the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse. The clear function for the SN54160, SN54161, SN74160, and SN74161 is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the state of the clock. The clear function for the SN54162, SN54163, SN74162, and SN74163 is synchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse. This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously set the counter to 0000 (LLLL).

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the carry output. The carry output thus enabled will produce a positive output pulse with a duration approximately equal to the positive portion of the Q_A output. This positive overflow carry pulse can be used to enable successive cascaded stages. High-to-low-level transitions at the enable P or T inputs should occur only when the clock input is high.

All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design. A full fan-out to ten normalized Series 54/74 loads is available from each of the outputs in the low-level state. A fan-out to 20 normalized Series 54/74 loads is provided in the high-level state to facilitate connection of unused inputs to used inputs. Input clock frequency is typically 32 megahertz and power dissipation is typically 325 milliwatts.

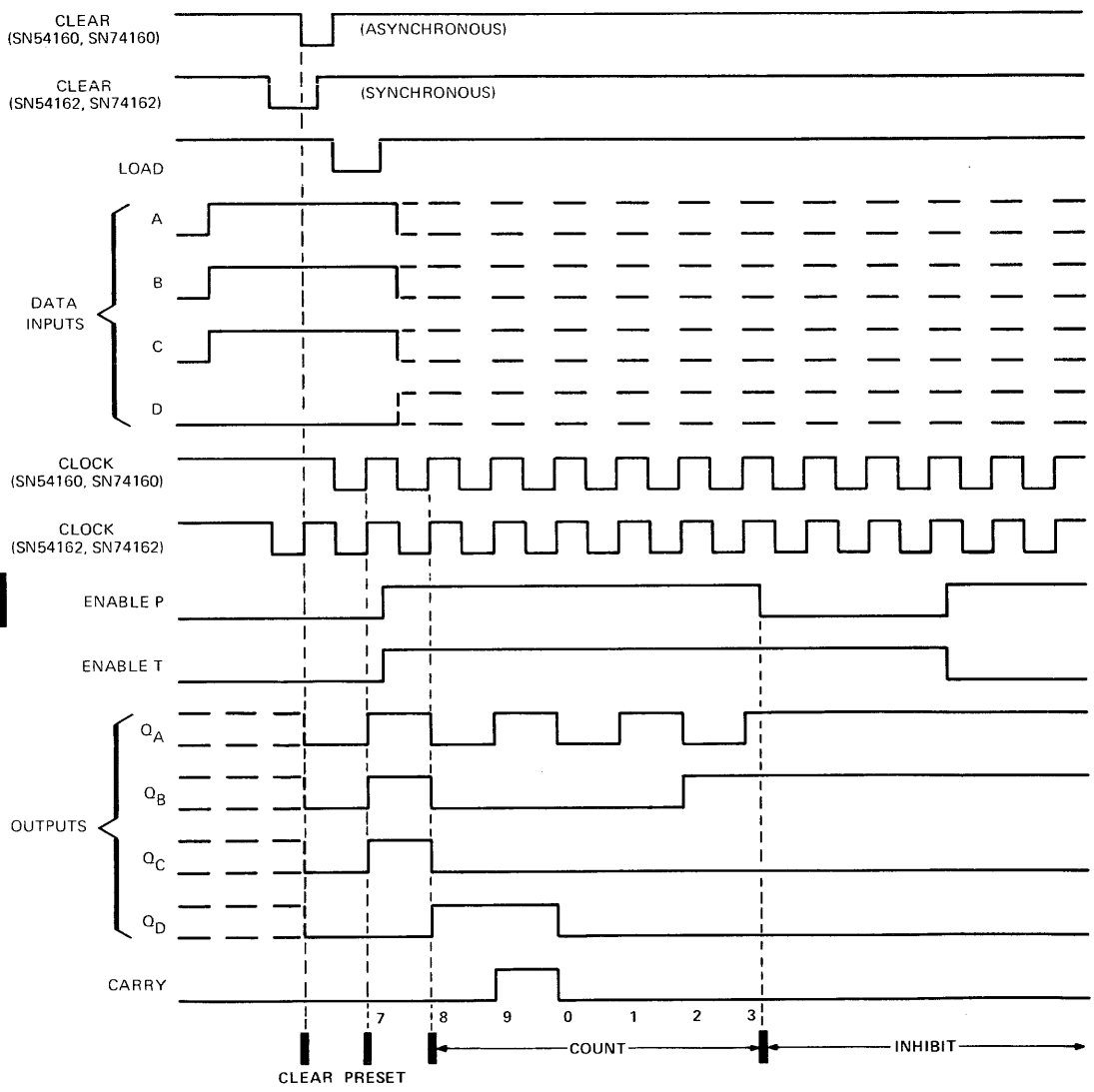
Series 54 circuits are characterized for operation over the full military temperature range of −55°C to 125°C; Series 74 circuits are characterized for operation from 0°C to 70°C.

SN54160, SN54162, SN74160, SN74162 SYNCHRONOUS DECADE COUNTERS

typical clear, preset, count, and inhibit sequences

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Preset to BCD seven.
3. Count to eight, nine, zero, one, two, and three.
4. Inhibit



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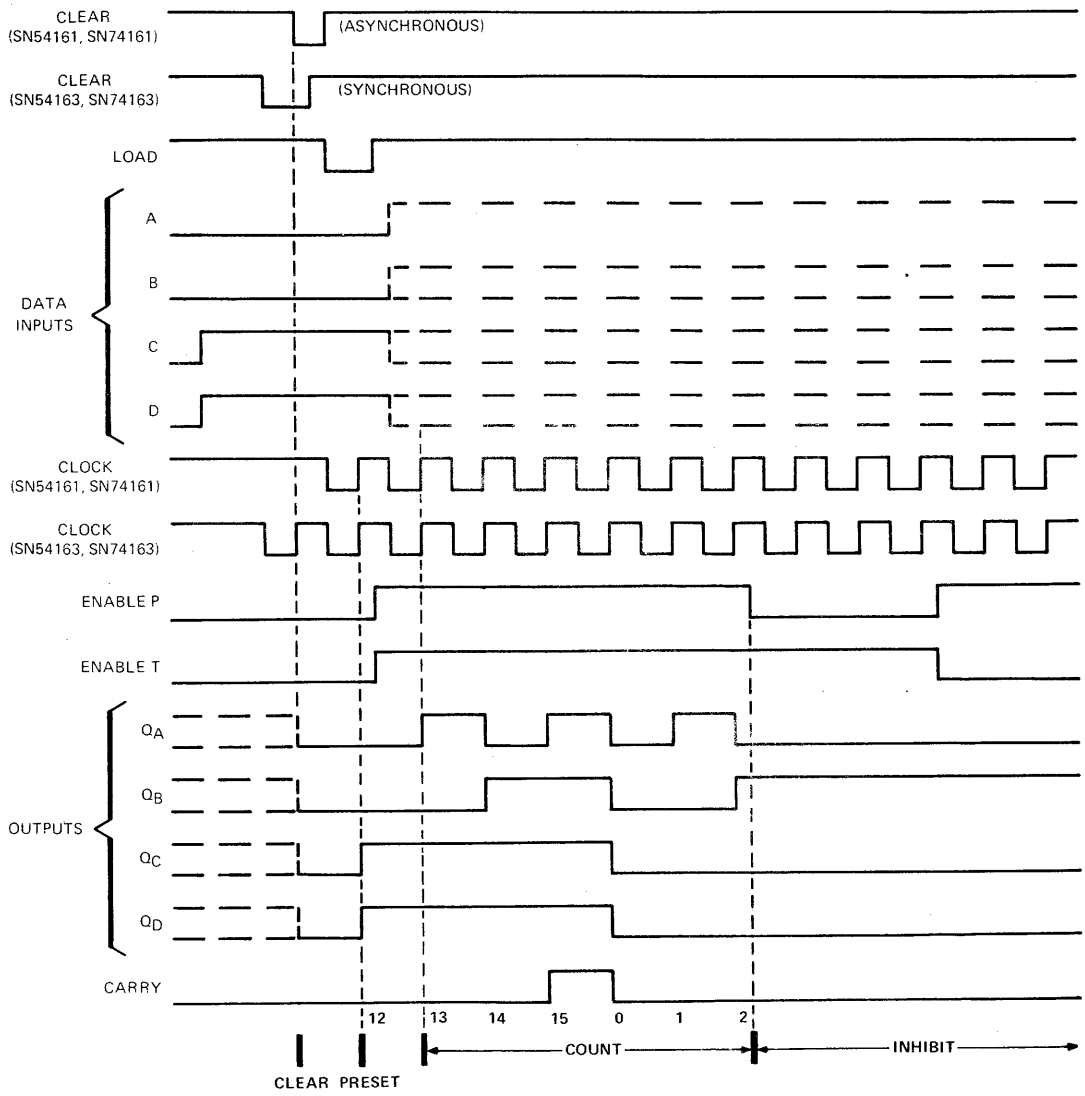
SN54161, SN54163, SN74161, SN74163 SYNCHRONOUS BINARY COUNTERS

typical clear, preset, count, and inhibit sequences

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Preset to binary twelve.
3. Count to thirteen, fourteen, fifteen, zero, one, and two.
4. Inhibit.



9

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range:
SN54160, SN54161, SN54162, SN54163 Circuits . . . . . −55°C to 125°C
SN74160, SN74161, SN74162, SN74163 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For these circuits, this rating applies between the count enable inputs P and T.

recommended operating conditions

		SN54160, SN54161, SN54162, SN54163			SN74160, SN74161, SN74162, SN74163			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Input clock frequency, f_{clock}		0		25	0		25	MHz
Width of clock pulse, $t_{w(clock)}$		25			25			ns
Width of clear pulse, $t_{w(clear)}$		20			20			ns
Setup time, t_{setup} (see Figures 1 and 3)	Data inputs A, B, C, D	15			15			ns
	Enable P	20			20			
	Load	15			15			
	Clear◇	20			20			
Hold time at any input, t_{hold}		0			0			ns
Operating free-air temperature, T_A		−55	25	125	0	25	70	°C

◇This applies only for SN54162, SN54163, SN74162, and SN74163 which have synchronous clear inputs.

electrical characteristics over recommended operating free-air temperature range (unless otherwise specified)

PARAMETER			TEST CONDITIONS†	SN54160, SN54161, SN54162, SN54163			SN74160, SN74161, SN74162, SN74163			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage		V_{CC} = MAX, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA	2.4			2.4			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.4			0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	Clock or enable T	V_{CC} = MAX, V_I = 2.4 V			80			80	μA
		Other inputs				40			40	
I_{IL}	Low-level input current	Clock or enable T	V_{CC} = MAX, V_I = 0.4 V			−3.2			−3.2	mA
		Other inputs				−1.6			−1.6	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	−20		−57	−18		−57	mA
I_{CCH}	Supply current, all outputs high		V_{CC} = MAX, See Note 3		59	85		59	94	mA
I_{CCL}	Supply current, all outputs low		V_{CC} = MAX, See Note 4		63	91		63	101	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

NOTES: 3. I_{CCH} is measured with the load input high, then again with the load input low, with all other inputs high and all outputs open.
4. I_{CCL} is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

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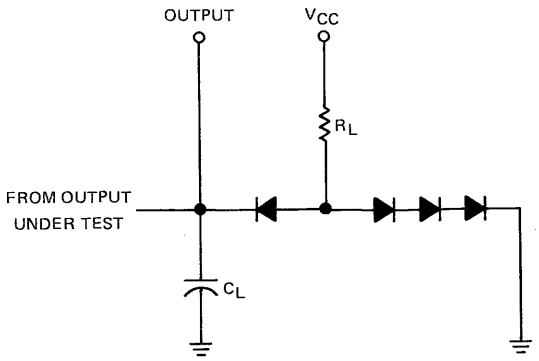
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum input clock frequency	1,2	C_L = 15 pF, R_L = 400 Ω	25	32		MHz
t_{PLH}	Propagation delay time, low-to-high-level carry output from clock	1,2			23	35	ns
t_{PHL}	Propagation delay time, high-to-low-level carry output from clock	1,2			23	35	
t_{PLH}	Propagation delay time, low-to-high-level Q output from clock	1,2			13	20	ns
t_{PHL}	Propagation delay time, high-to-low-level Q output from clock	1,2			15	23	
t_{PLH}	Propagation delay time, low-to-high-level carry output from enable T	1,3			8	13	ns
t_{PHL}	Propagation delay time, high-to-low-level carry output from enable T	1,3			10	15	
t_{PHL}	Propagation delay time, high-to-low-level Q output from clear	1,3			20	30	ns

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064.

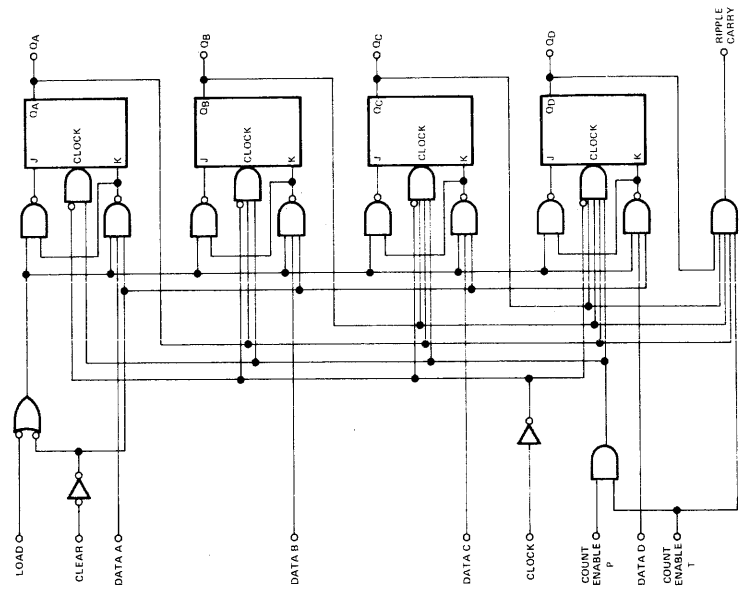
LOAD CIRCUIT FOR SWITCHING TESTS
FIGURE 1

9

functional block diagrams

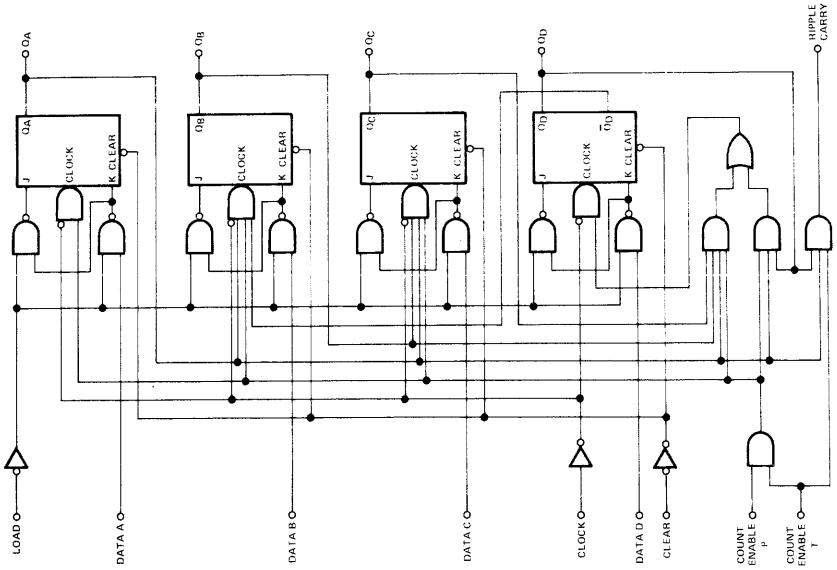
SN54163, SN74163 SYNCHRONOUS BINARY COUNTERS

SN54161, SN74161 synchronous binary counters are similar; however, the clear is asynchronous as shown for the SN54160, SN74160 decade counters at left.



SN54160, SN74160 SYNCHRONOUS DECADE COUNTERS

SN54162, SN74162 synchronous decade counters are similar; however the clear is synchronous as shown for the SN54163, SN74163 binary counters at right.



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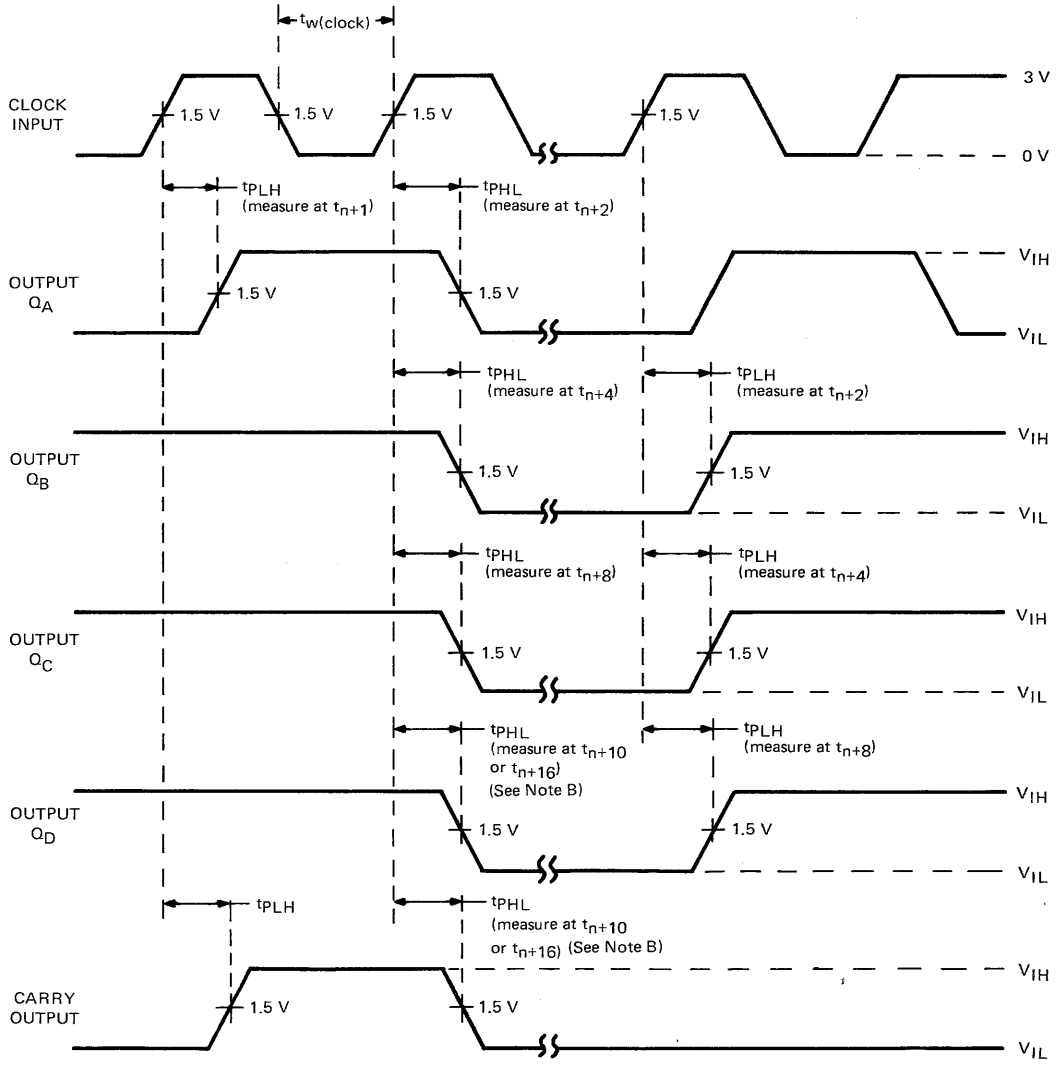
PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

NOTES: A. The input pulses are supplied by a generator having the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, PRR ≤ 1 MHz, duty cycle $\leq 50\%$, $Z_{out} \approx 50\ \Omega$. Vary PRR to measure f_{max}.

B. Outputs Q_D and carry are tested at t_{n+10} for the SN54160, SN54162, SN74160, and SN74162, and at t_{n+16} for the SN54161, SN54163, SN74161, and SN74163, where t_n is the bit time when all outputs are low.

FIGURE 2–SWITCHING TIMES

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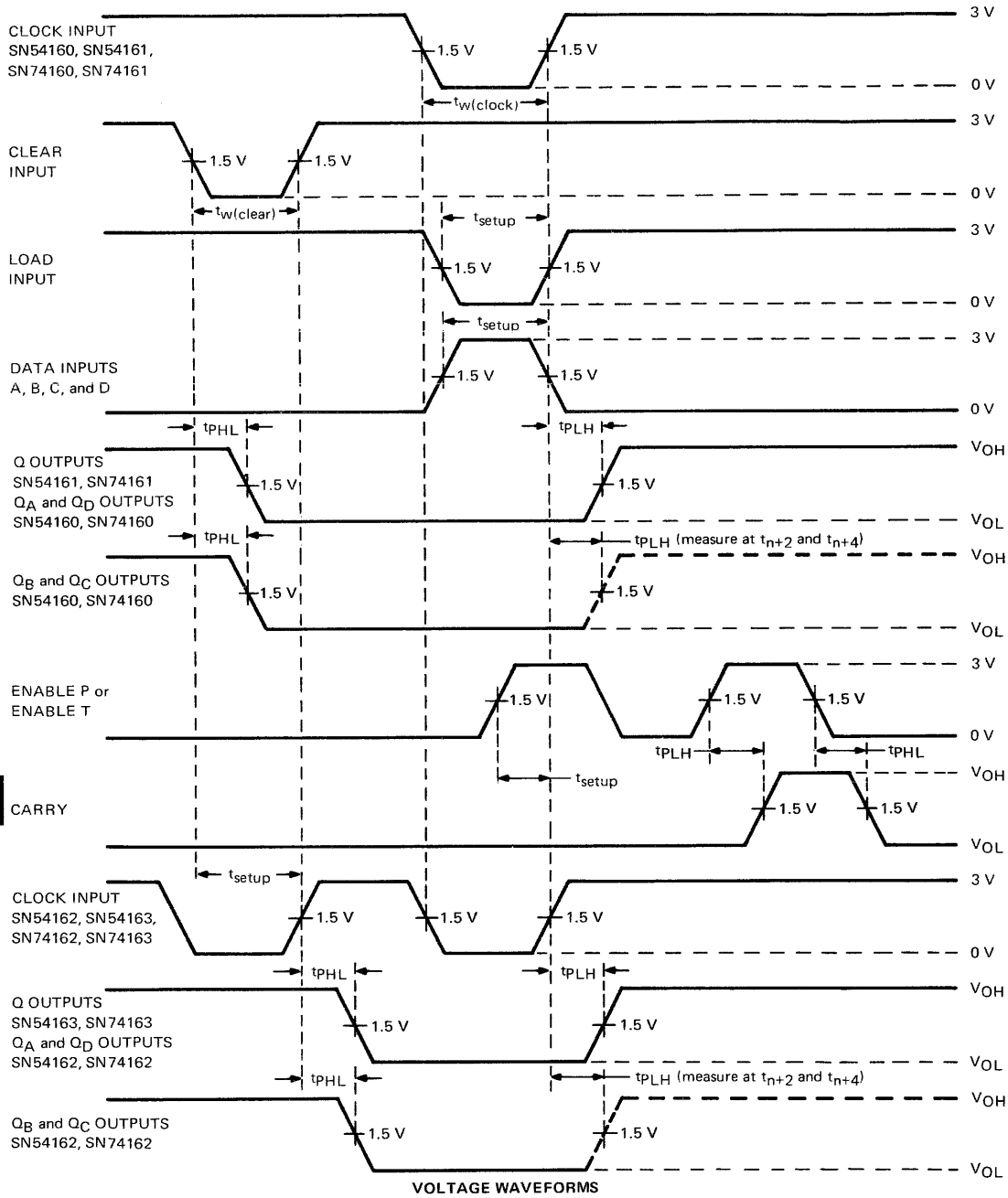
PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

NOTES: A. The input pulses are supplied by a generator having the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, PRR ≤ 1 MHz, duty cycle $\leq 50\%$, $Z_{out} \approx 50\ \Omega$.

B. Enable P and enable T setup times are measured at $t_n = 0$.

FIGURE 3–SWITCHING TIMES

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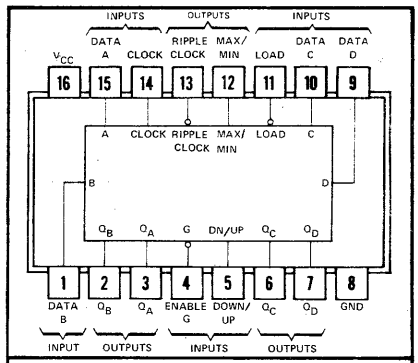
CIRCUIT TYPES SN54190, SN54191, SN74190, SN74191
SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

- Counts 8-4-2-1 BCD or Binary
- Single Down/Up Count Control Line
- Count Enable Control Input
- Ripple Clock Output for Cascading
- Asynchronously Presettable with Load Control
- Parallel Outputs
- Cascadable for n-Bit Applications
- Typical Average Propagation Delay (Clock to Q Output) . . . 20 ns
- Typical Power Dissipation . . . 325 mW
- Typical Maximum Clock Frequency . . . 25 MHz

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



asynchronous inputs: Low input to load sets Q_A=A, Q_B = B, Q_C = C, and Q_D = D

†Pin assignments for these circuits are the same for all packages.

description

The SN54190, SN54191, SN74190, and SN74191 are synchronous, reversible up/down counters having a complexity of 58 equivalent gates. The SN54191 and SN74191 are 4-bit binary counters and the SN54190 and SN74190 are BCD counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation will eliminate the output counting spikes which are normally associated with asynchronous (ripple clock) counters.

The outputs of the four master-slave flip-flops are triggered on a low-to-high-level transition of the clock input if the enable input is low. A high at the enable input inhibits counting. Level changes at the enable input should be made only when the clock input is high. The direction of the count is determined by the state of the down/up input. When low, the counter counts up and when high, it counts down.

These counters are fully programmable; that is, the outputs may be preset to any state by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the state of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

Input buffers have been used to lower the fan-in requirement to only one normalized Series 54/74 load at all inputs except enable. This is important when the output of the driving circuitry is somewhat limited.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

Power dissipation is typically 325 milliwatts for either the decade or binary version. Maximum input clock frequency is typically 25 megahertz and is guaranteed to be at least 20 megahertz.

The SN54190 and SN54191 are characterized for operation over the full military temperature range of −55°C to 125°C; the SN74190 and SN74191 are characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: SN54190, SN54191 . . . . . −55°C to 125°C
SN74190, SN74191 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

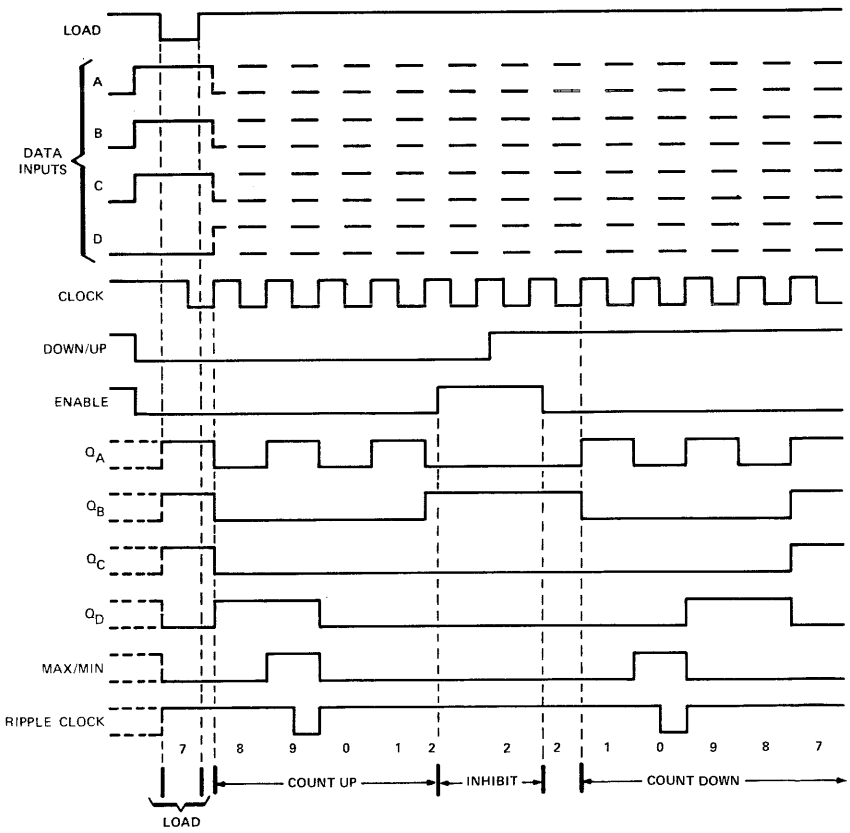
NOTE 1: Voltage values are with respect to network ground terminal.

SN54190, SN74190 DECADE COUNTERS

typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to BCD seven.
2. Count up to eight, nine (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), nine, eight, and seven.



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recommended operating conditions

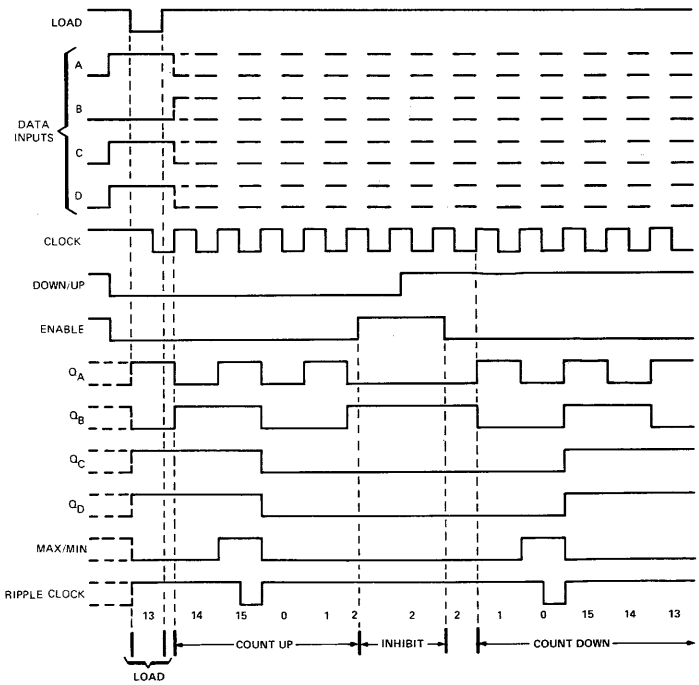
		SN54190, SN54191			SN74190, SN74191			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Input clock frequency, f_{clock}		0		20	0		20	MHz
Width of clock input pulse, $t_{w(clock)}$		25			25			ns
Width of load input pulse, $t_{w(load)}$		35			35			ns
Data setup time, t_{setup} (See Figures 1 and 2)		20			20			ns
Data hold time, t_{hold}		0			0			ns
Operating free-air temperature, T_A		−55	25	125	0	25	70	°C

SN54191, SN74191 BINARY COUNTERS

typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to binary thirteen.
2. Count up to fourteen, fifteen (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen.



9

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54190, SN54191			SN74190, SN74191			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage	V_{CC} = MIN	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = MIN			0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA	2.4			2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.4			0.4	V
I_I	High-level input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current at any input except enable	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IH}	High-level input current at enable input				120			120	μA
I_{IL}	Low-level input current at any input except enable	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
I_{IL}	Low-level input current at enable input				−4.8			−4.8	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	−20		−65	−18		−65	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2		65	105		65	105	mA

†For conditions shown as MAX or MIN, use appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with all inputs grounded and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			C_L = 15 pF, R_L = 400 Ω, See Figure 1 and Figures 3 thru 7	20	25		MHz
t_{PLH}	Load	Q_A, Q_B, Q_C, Q_D			22	33	ns
t_{PHL}					33	50	
t_{PLH}	Data A, B, C, D	Q_A, Q_B, Q_C, Q_D			14	22	ns
t_{PHL}					35	50	
t_{PLH}	Clock	Ripple Clock			13	20	ns
t_{PHL}					16	24	
t_{PLH}	Clock	Q_A, Q_B, Q_C, Q_D			16	24	ns
t_{PHL}					24	36	
t_{PLH}	Clock	Max/Min			28	42	ns
t_{PHL}					37	52	
t_{PLH}	Down/Up	Ripple Clock			30	45	ns
t_{PHL}					30	45	
t_{PLH}	Down/Up	Max/Min			21	33	ns
t_{PHL}					22	33	

¶f_{max} = maximum clock frequency
t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output

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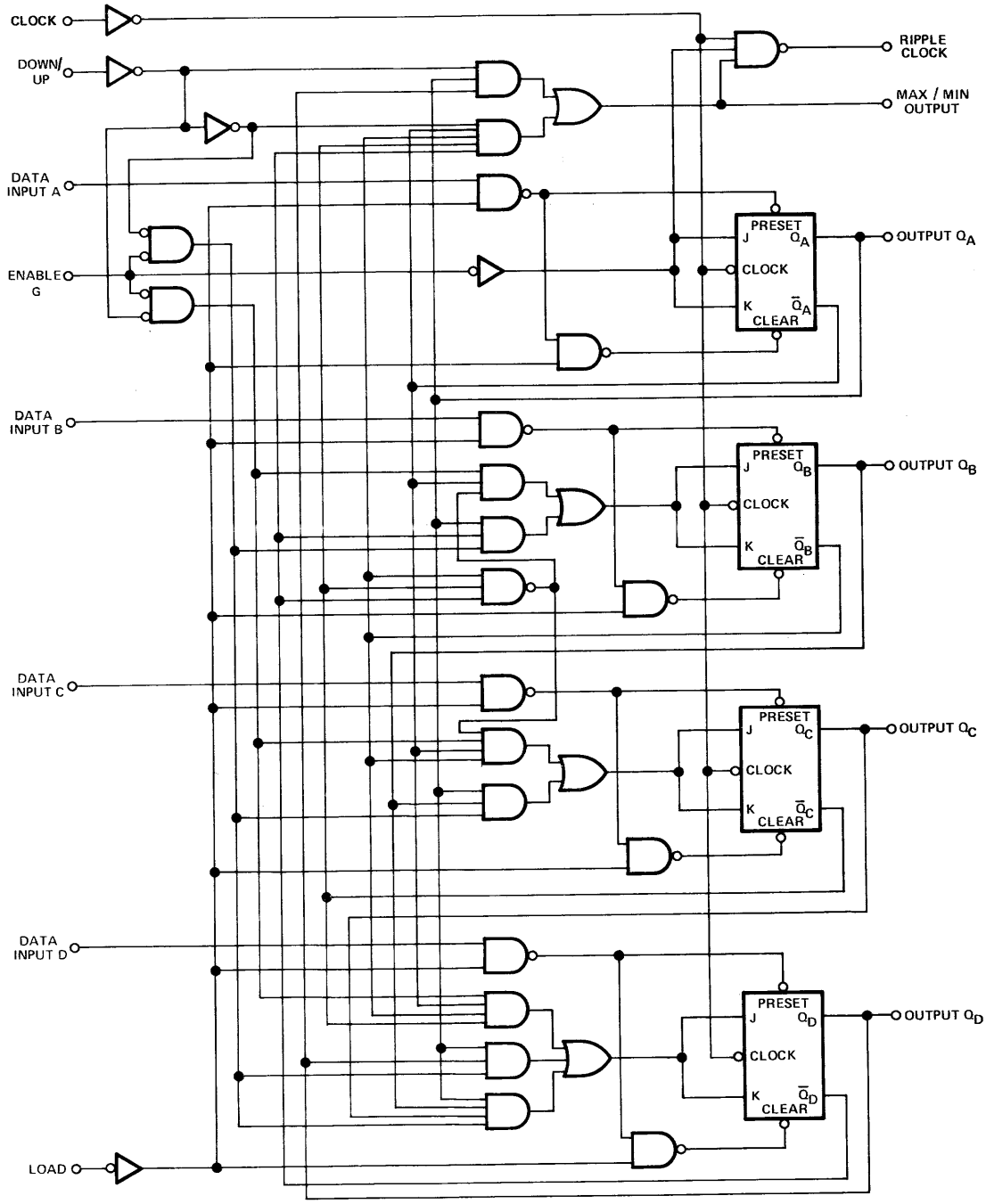
functional block diagram SN54190, SN74190 DECADE COUNTERS



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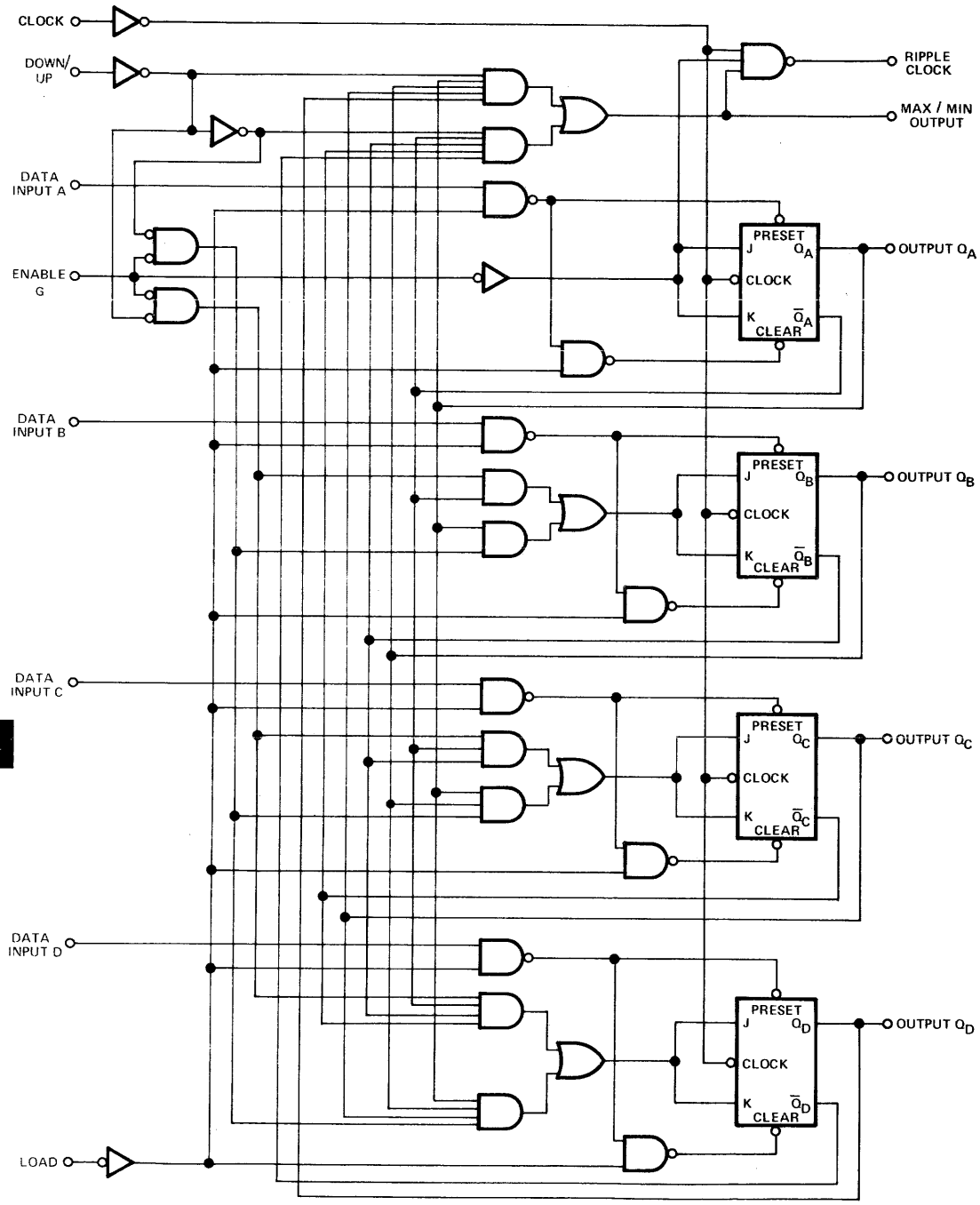
functional block diagram

SN54191, SN74191 BINARY COUNTERS



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PARAMETER MEASUREMENT INFORMATION

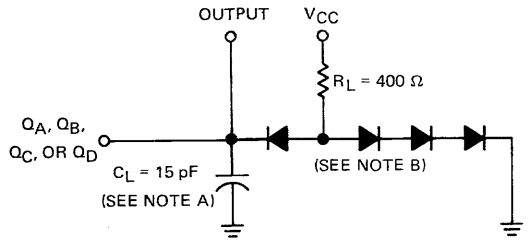


FIGURE 1–LOAD CIRCUIT
FOR SWITCHING TIME MEASUREMENT

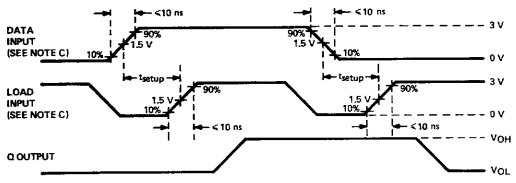
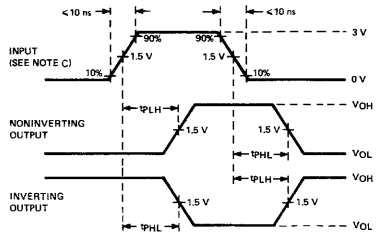


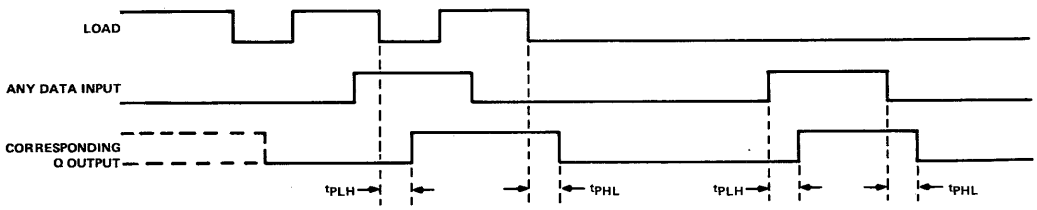
FIGURE 2–SETUP TIME VOLTAGE WAVEFORMS



See waveform sequences in figures 4 through 7 for propagation times from a specific input to a specific output. For simplification, pulse rise times, reference levels, etc., have not been shown in figures 4 through 7.

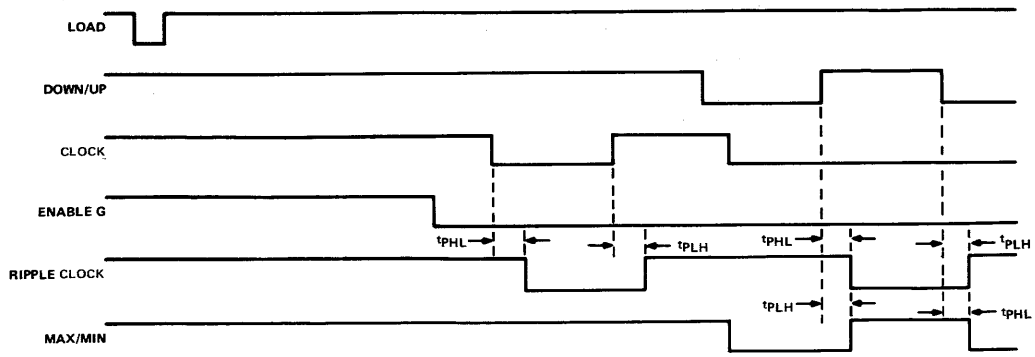
FIGURE 3–GENERAL VOLTAGE WAVEFORMS FOR PROPAGATION TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064.
C. The input pulses are supplied by generators having the following characteristics: Z_{out} = 50 Ω, duty cycle ≤ 50%, PRR ≤ 1 MHz.



NOTE D: Conditions on other inputs are irrelevant.

FIGURE 4–LOAD TO OUTPUT AND DATA TO OUTPUT



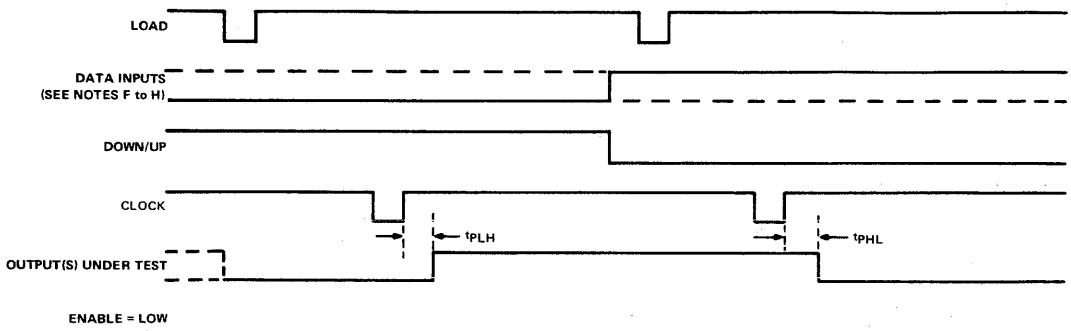
NOTE E: All data inputs are low.

FIGURE 5–ENABLE TO RIPPLE CLOCK, CLOCK TO RIPPLE CLOCK, DOWN/UP TO RIPPLE CLOCK, AND DOWN/UP TO MAX/MIN

9

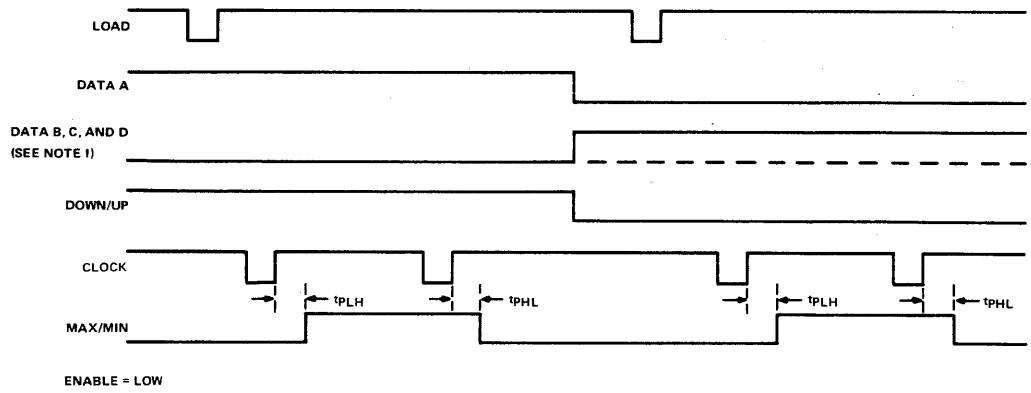
PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



NOTES: F. To test Q_A, Q_B, and Q_C outputs of SN54190: Data inputs A, B, and C are shown by the solid line. Data input D is shown by the dashed line.
G. To test Q_D output of SN54190: Data inputs A and D are shown by the solid line. Data inputs B and C are held at the low logic level.
H. To test Q_A, Q_B, Q_C, and Q_D outputs of SN54191: All four data inputs are shown by the solid line.

FIGURE 6–CLOCK TO OUTPUT



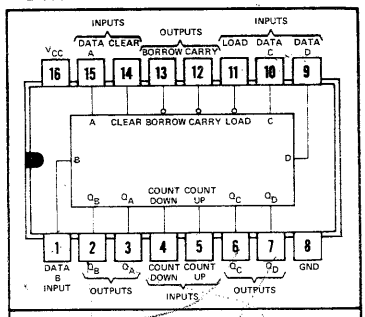
NOTE I: Data inputs B and C are shown by the dashed line for SN54190 and the solid line for SN54191. Data input D is shown by the solid line for both devices.

FIGURE 7–CLOCK TO MAX/MIN

CIRCUIT TYPES SN54192, SN54193, SN74192, SN74193
SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

- Cascading Circuitry Provided Internally
- Synchronous Operation
- Individual Preset to Each Flip-Flop
- Fully Independent Clear Input
- Typical Maximum Input Count Frequency . . . 32 MHz

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



logic: Low input to load sets Q_A = A, Q_B = B, Q_C = C, and Q_D = D

description

These monolithic circuits are synchronous reversible (up/down) counters having a complexity of 55 equivalent gates. The SN54192 and SN74192 are BCD counters and the SN54193 and SN74193 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple-clock) counters.

The outputs of the four master-slave flip-flops are triggered by a low-to-high-level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed while the other count input is high.

All four counters are fully programmable; that is, the outputs may be preset to any state by entering the desired data at the data inputs while the load input is low. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided which forces all outputs to the low level when a high level is applied. The clear function is independent of the count and load inputs. An input buffer has been placed on the clear, count, and load inputs to lower the drive requirements to one normalized Series 54/74 load. This is important when the output of the driving circuitry is somewhat limited.

These counters were designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up- and down-counting functions. The borrow output produces a pulse equal in width to the count-down input when the counter underflows. Similarly, the carry output produces a pulse equal in width to the count-up input when an overflow condition exists. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs respectively of the succeeding counter.

Power dissipation is typically 325 milliwatts for either the decade or binary version. Maximum input count frequency is typically 32 megahertz and is guaranteed to be 25 MHz minimum. All inputs are buffered and represent only one normalized Series 54/74 load. Input clamping diodes are provided to minimize transmission-line effects and thereby simplify system design. The SN54192 and SN54193 are characterized for operation over the full military temperature range of −55°C to 125°C; the SN74192 and SN74193 are characterized for operation from 0°C to 70°C.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1)		7 V
Input voltage (see Note 1)		5.5 V
Operating free-air temperature range:	SN54192 and SN54193 Circuits	−55°C to 125°C
	SN74192 and SN74193 Circuits	0°C to 70°C
Storage temperature range		−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

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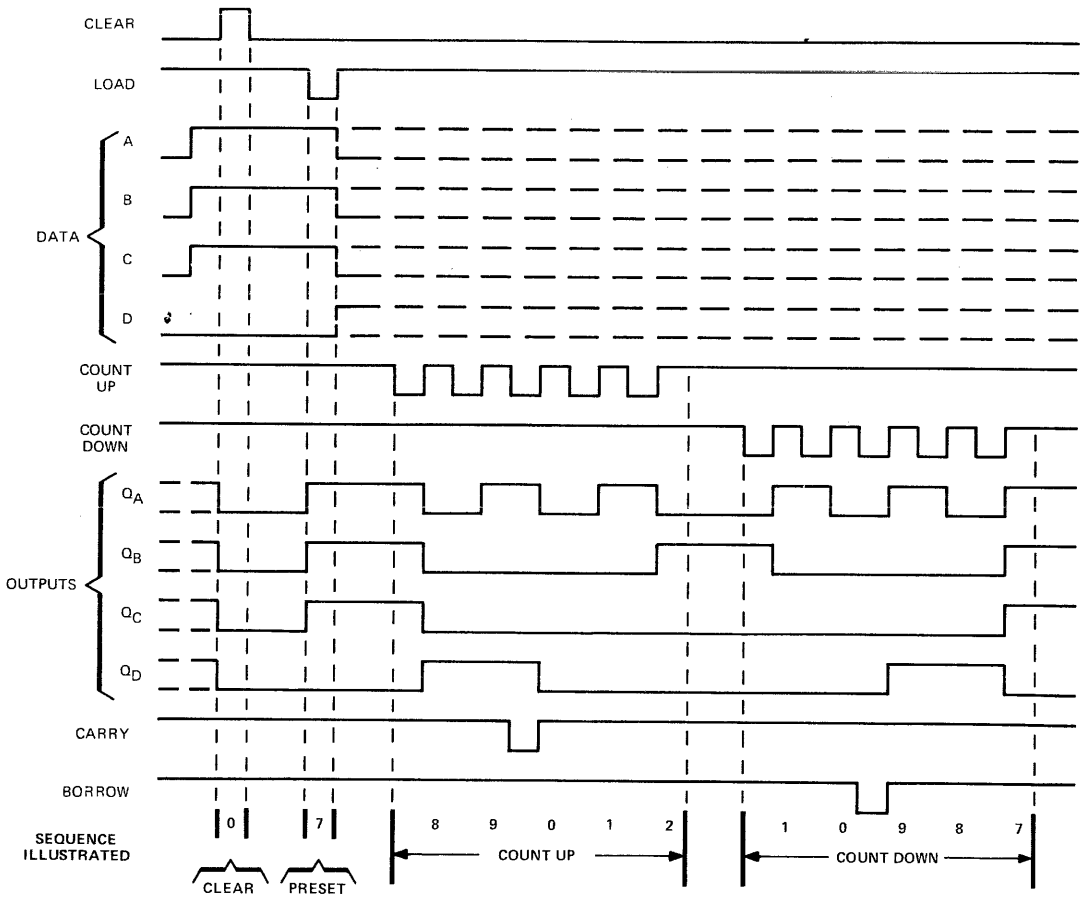
SN54192, SN74192 DECADE COUNTERS

typical clear, load, and count sequences

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to BCD seven.
3. Count up to eight, nine, carry, zero, one, and two.
4. Count down to one, zero, borrow, nine, eight, and seven.



NOTES: A. Clear overrides load, data, and count inputs.
B. When counting up, count-down input must be high; when counting down, count-up input must be high.

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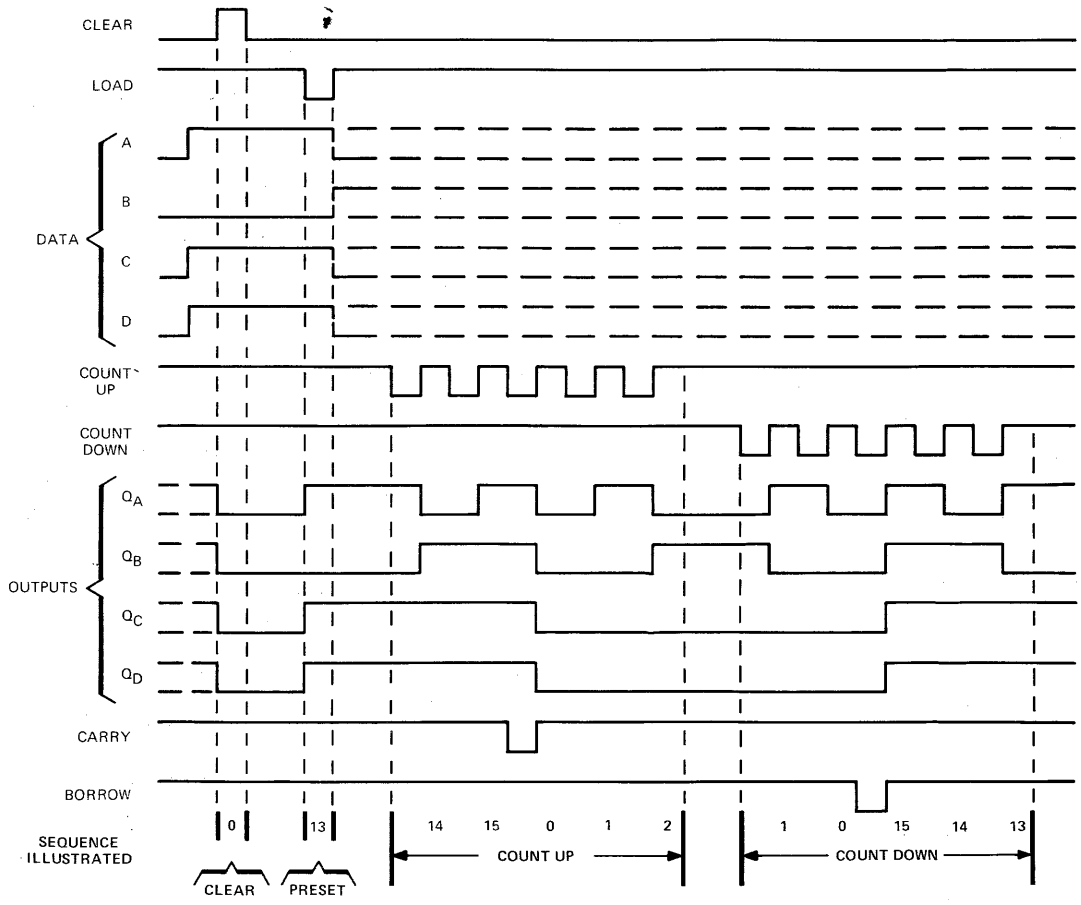
SN54193, SN74193 BINARY COUNTERS

typical clear, load, and count sequences

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to BCD thirteen.
3. Count up to fourteen, fifteen, carry, zero, one, and two.
4. Count down to one, zero, borrow, fifteen, fourteen, and thirteen.



NOTES: A. Clear overrides load, data, and count inputs.
B. When counting up, count-down input must be high; when counting down, count-up input must be high.

recommended operating conditions

	SN54192, SN54193			SN74192, SN74193			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N			10			10	
Input count frequency, f_{count}	0		25	0		25	MHz
Width of any input pulse, t_w	20			20			ns
Data setup time, t_{setup} (see Figure 7 and Note 2)	20			20			ns
Data hold time, t_{hold} (see Note 3)	0			0			ns
Operating free-air temperature range, T_A	−55	25	125	0	25	70	°C

NOTES: 2. Setup time is the interval immediately preceding the positive-going edge of the load pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.

3. Hold time is the interval immediately following the positive-going edge of the load pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	SN54192, SN54193			SN74192, SN74193			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage	1 and 2		2			2			V
V_{IL}	Low-level input voltage	1 and 2				0.8			0.8	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −400 μA	2.4			2.4			V
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.4			0.4	V
I_{IH}	High-level input current	3	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
			V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IL}	Low-level input current	4	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
I_{OS}	Short-circuit output current§	5	V_{CC} = MAX	−20		−65	−18		−65	mA
I_{CC}	Supply current	6	V_{CC} = MAX		65	89		65	102	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time.

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switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER¶	FROM INPUT	TO OUTPUT	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}				C_L = 15 pF, R_L = 400 Ω	25	32		MHz
t_{setup}			7			14	20	ns
t_{PLH}	Count-up	Carry	8			17	26	ns
t_{PHL}						16	24	
t_{PLH}	Count-down	Borrow	8			16	24	ns
t_{PHL}						16	24	
t_{PLH}	Either Count	Q	8			25	38	ns
t_{PHL}						31	47	
t_{PLH}	Load	Q	7			27	40	ns
t_{PLH}						29	40	
t_{PHL}	Clear	Q	7			22	35	ns

¶f_{max} = maximum clock frequency
t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output

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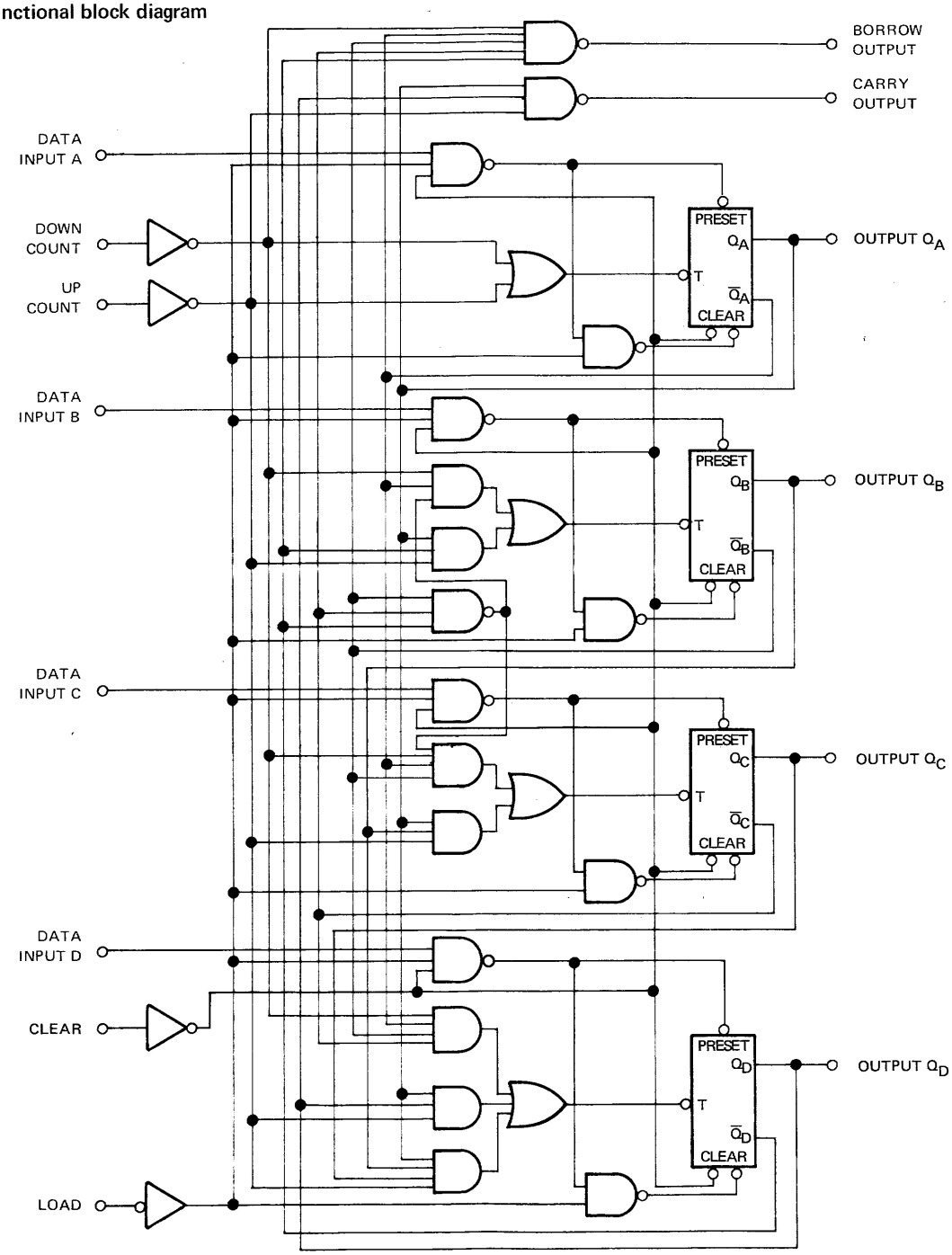
SN54192, SN74192 DECADE COUNTER

functional block diagram



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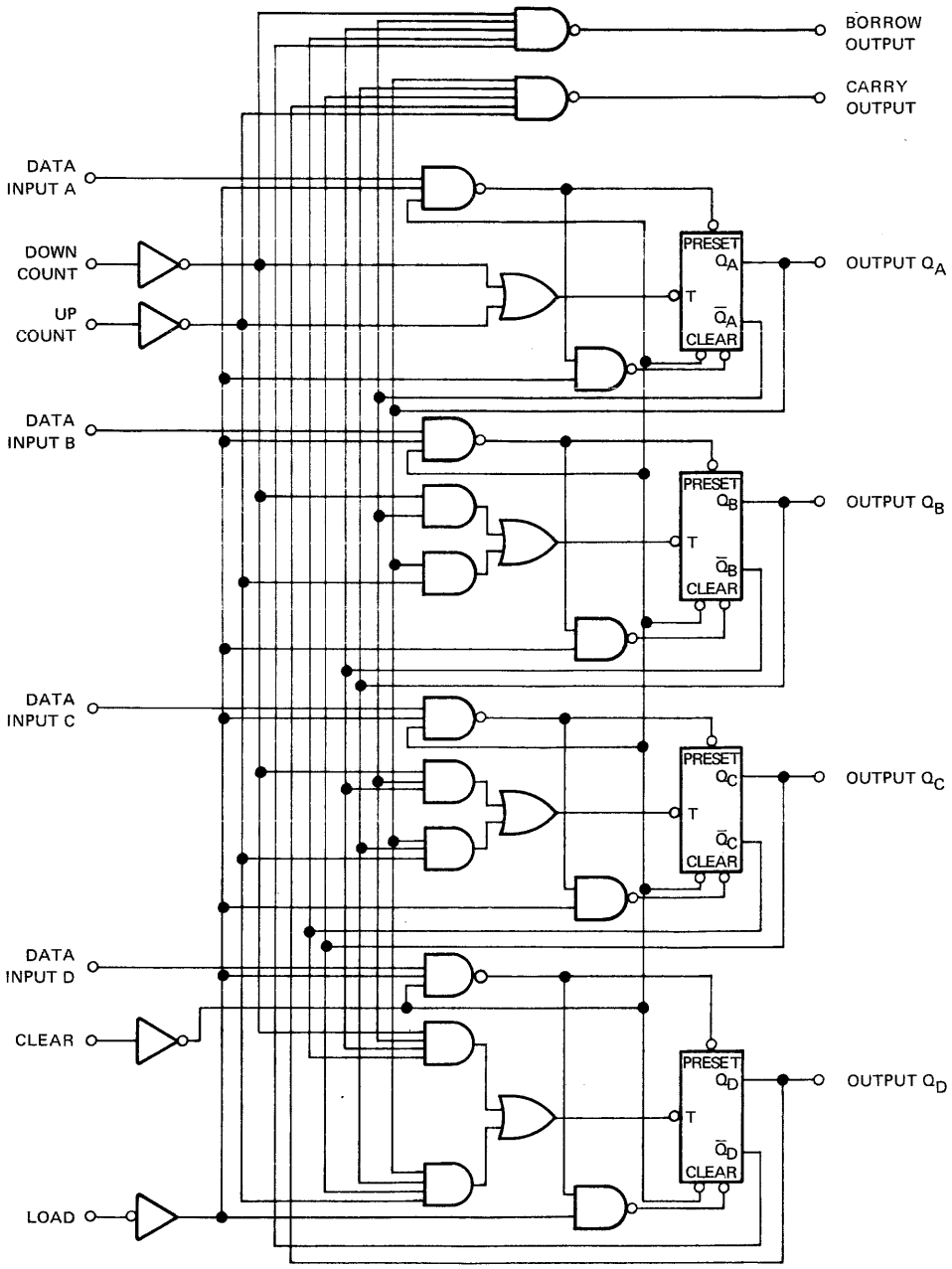
SN54193, SN74193 BINARY COUNTER

functional block diagram



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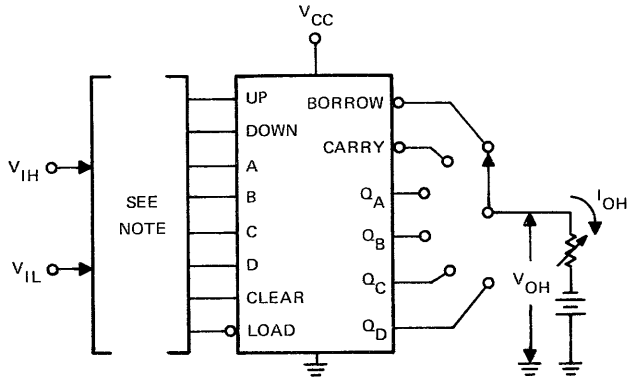
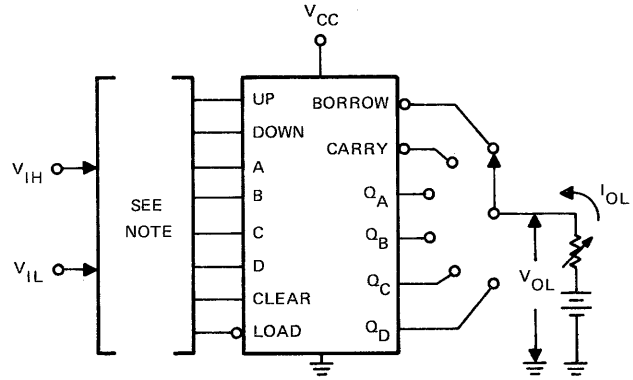
PARAMETER MEASUREMENT INFORMATION

d-c test circuits¶



Each output is tested separately.

FIGURE 1–V_{IH}, V_{IL}, V_{OH}



Each output is tested separately.

FIGURE 2–V_{IH}, V_{IL}, V_{OL}

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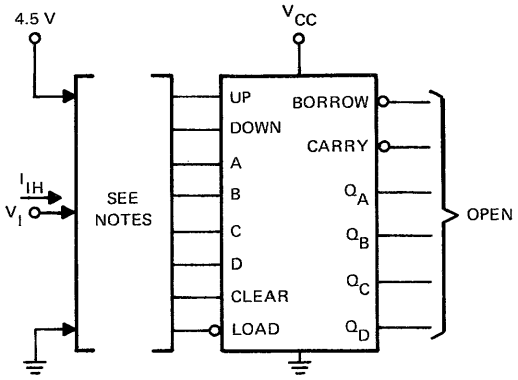


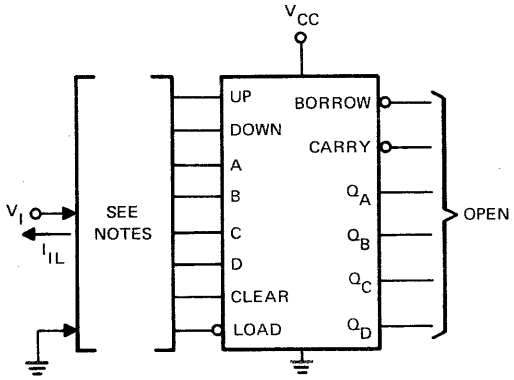
NOTES: A. Each input is tested separately.
B. Apply V_I to input under test, and ground other inputs except when testing data inputs, apply 4.5 V to clear and load inputs.

FIGURE 3–I_{IH}

¶Arrows indicate actual direction of current flow. Current into a ter. inal is a positive value.

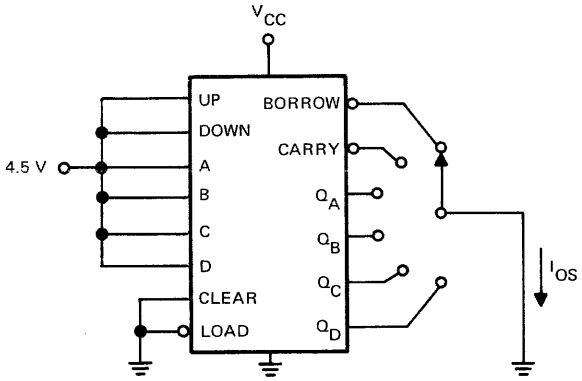
PARAMETER MEASUREMENT INFORMATION

d-c test circuits (continued)¶



NOTES: A. Each input is tested separately.
B. Apply V_I to input under test and ground other inputs.

FIGURE 4–I_{IL}



Each output is tested separately in the high-level state.

FIGURE 5–I_{OS}

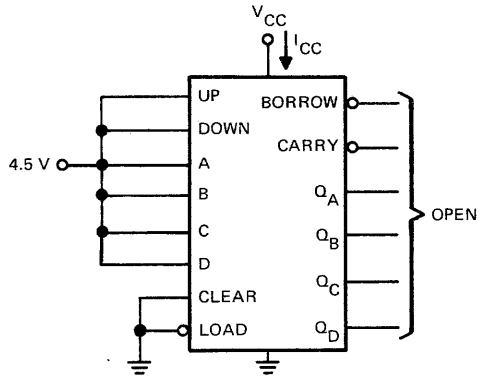


FIGURE 6–I_{CC}

¶ Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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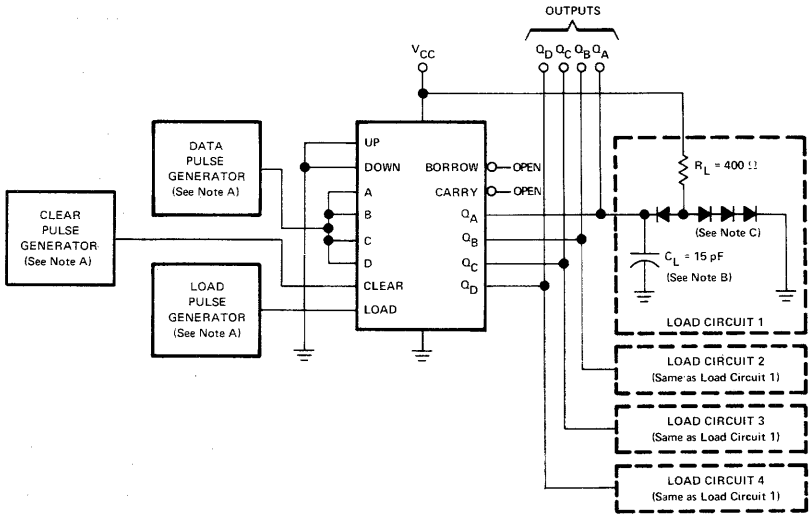
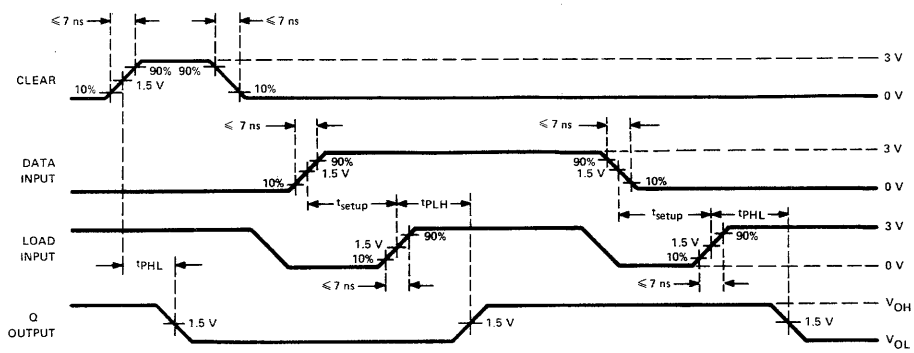
PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: $Z_{out} \approx 50\ \Omega$; for the data pulse generator, PRR = 500 kHz, duty cycle = 50%; for the load pulse generator, PRR = 1 MHz, duty cycle = 50%.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.

FIGURE 7–CLEAR, SETUP, AND LOAD TIMES

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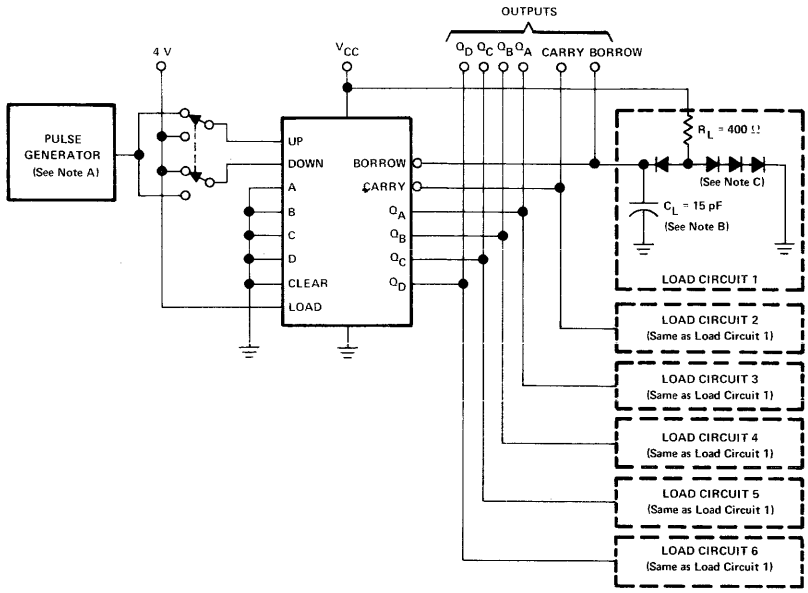
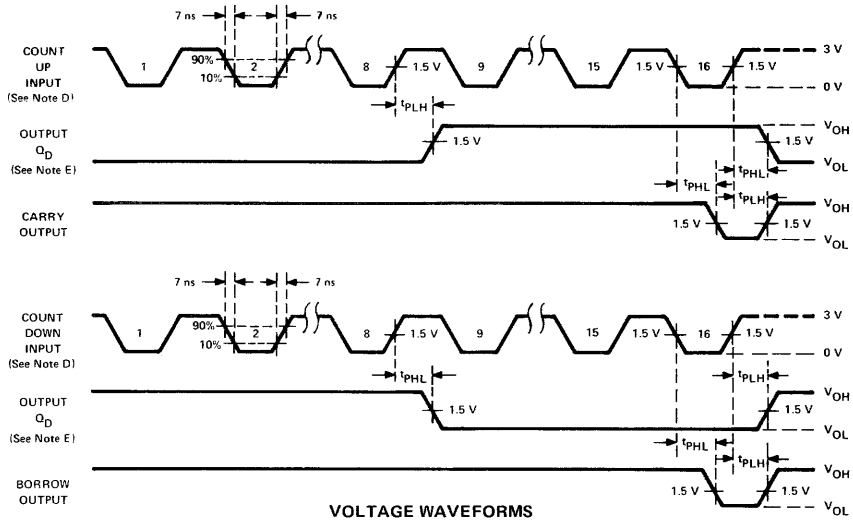
PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$, duty cycle = 50%.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.
D. Count-up and count-down pulses shown are for the SN54193/SN74193 binary counters. Count cycle for SN54192 decade counter is 1 through 10.
E. Waveforms for outputs Q_A, Q_B, and Q_C are omitted to simplify the drawing.

FIGURE 8–PROPAGATION DELAY TIMES

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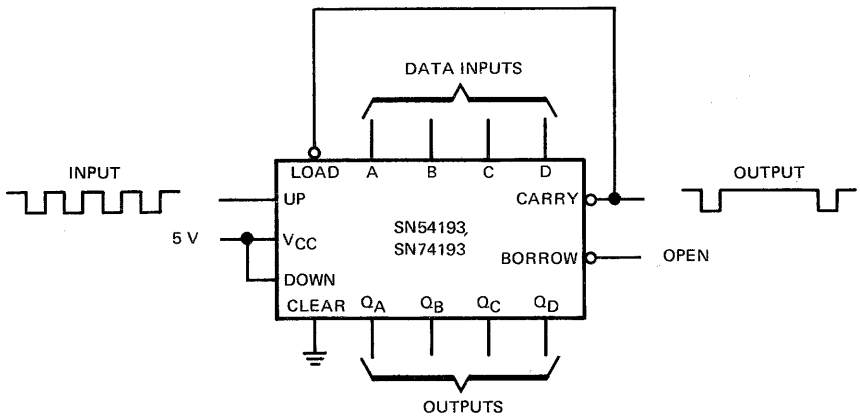
TYPICAL APPLICATION DATA

modulo-N divider

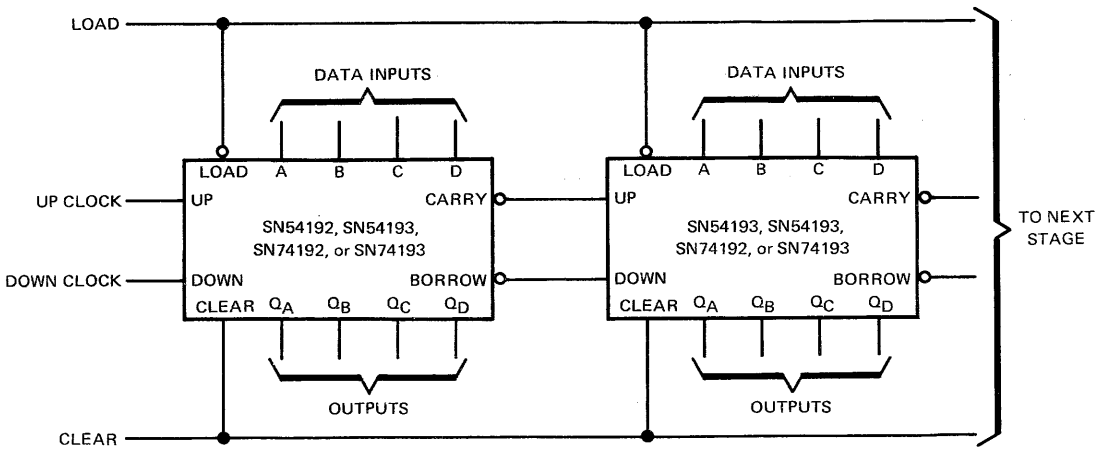
The SN54193/SN74193 can be used to divide an incoming count frequency by any integral number (N) from one to 16. This is done by modifying the count frequency occurring at the carry output by presetting the data inputs to 16 minus N. By connecting the carry output to the load input, the counter will count to the maximum state (15) and the data inputs will then be enabled on the succeeding clock pulse. The counter outputs are then preset to the levels applied at the data inputs and the count sequence is repeated.



The SN54192/SN74192 may be used in the same manner to perform division by any number from 1 to 10.

cascading

Circuitry is provided internally for cascading these counters. The mode of cascading shown below is ripple borrow/carry. No external components are required.



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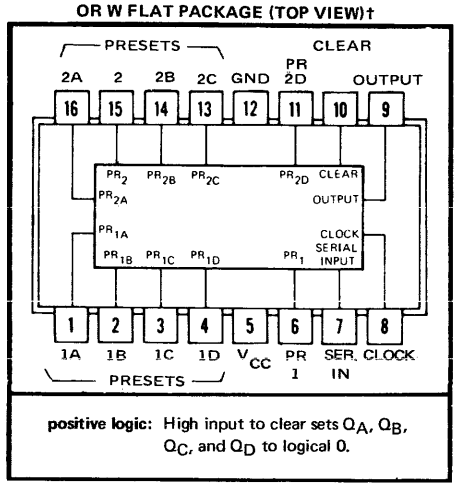
CIRCUIT TYPES SN5494, SN7494
4-BIT SHIFT REGISTERS

TTL MSI PARALLEL-IN SERIAL-OUT REGISTERS

for application as

- Dual-Source, Parallel-To-Serial Converter
- Serial-In Serial-Out Register

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



†Pin assignments for these circuits are the same for all packages.

description

This monolithic shift register, utilizing transistor-transistor logic (TTL) circuits in the familiar Series 74 configuration, is composed of four R-S master-slave flip-flops, four AND-OR-INVERT gates, and four inverter-drivers. Internal interconnections of these functions provide a versatile register which performs right-shift operations as a serial-in, serial-out register or as a dual-source, parallel-to-serial converter. A number of these registers may be connected in series to form an n-bit register.

All flip-flops are simultaneously set to the logical 0 state by applying a logical 1 voltage to the clear input. This condition may be applied independent of the state of the clock input, but not independent of state of the preset input. Preset input is independent of the clock and clear states.

The flip-flops are simultaneously set to the logical 1 state from either of two preset input sources. Preset inputs 1A through 1D are activated during the time that a positive pulse is applied to preset 1 if preset 2 is at a logical 0 level. When the logic levels at preset 1 and preset 2 are reversed, preset inputs 2A through 2D are active.

Transfer of information to the outputs occurs when the clock input goes from a logical 0 to a logical 1. Since the flip-flops are R-S master-slave circuits, the proper information must appear at the R-S inputs of each flip-flop prior to the rising edge of the clock input waveform. The serial input provides this information for the first flip-flop. The outputs of the subsequent flip-flops provide information for the remaining R-S inputs. The clear input, preset 1, and preset 2 must be at a logical 0 when clocking occurs.

This register is completely compatible for use with TTL and DTL logic circuits and when used with other TTL circuits, noise margins are typically one volt. Typical average power dissipation is 175 milliwatts, and propagation delay times from clock to output are typically 25 nanoseconds.

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absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1)		7 V
Input Voltage V_{in} (See Notes 1 and 2)		5.5 V
Operating Free-Air Temperature Range:	SN5494 Circuits	−55°C to 125°C
	SN7494 Circuits	0°C to 70°C
Storage Temperature Range		−65°C to 150°C

NOTES: 1. The voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

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recommended operating conditions

		MIN	TYP	MAX	UNIT
Supply Voltage V_{CC} (See Note 1):	SN5494 Circuits	4.5	5	5.5	V
	SN7494 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Output				10	
Width of Clock Pulse, $t_{p(clock)}$		35			ns
Width of Clear Pulse, $t_{p(clear)}$		30			ns
Width of Preset Pulse, $t_{p(preset)}$		30			ns
Serial Input Setup Time: $t_{setup(1)}$		35			ns
$t_{setup(0)}$		25			ns
Serial Input Hold Time, t_{hold}		0			

NOTE: 1. These voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating temperature range (unless otherwise noted)

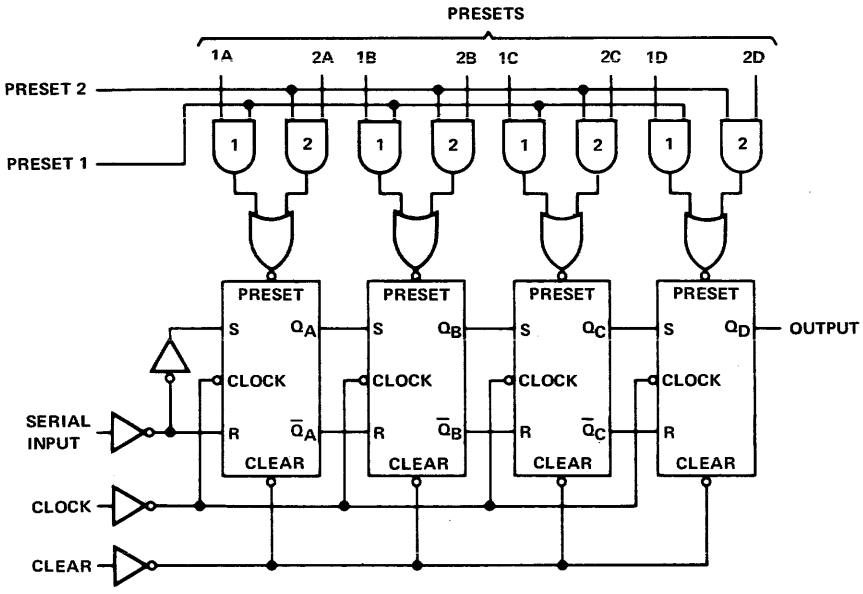
PARAMETER		TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal				2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal						0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = −400 μA		2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 16 mA			0.22	0.4	V
$I_{in(1)}$	Logical 1 level input current at any input except preset 1 and preset 2	V_{CC} = MAX,	V_{in} = 2.4 V				40	μA
		V_{CC} = MAX,	V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at preset 1 and preset 2	V_{CC} = MAX,	V_{in} = 2.4 V				160	μA
		V_{CC} = MAX,	V_{in} = 5.5 V				1	mA
$I_{in(0)}$	Logical 0 level input current at any input except preset 1 and preset 2	V_{CC} = MAX,	V_{in} = 0.4 V				−1.6	mA
$I_{in(0)}$	Logical 0 level input current at preset 1 and preset 2	V_{CC} = MAX,	V_{in} = 0.4 V				−6.4	mA
I_{OS}	Short-circuit input current§	V_{CC} = MAX,	V_{out} = 0	SN5494	−20		−57	mA
				SN7494	−18		−57	mA
I_{CC}	Supply current	V_{CC} = MAX		SN5494		35	50	mA
				SN7494		35	58	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the particular circuit type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

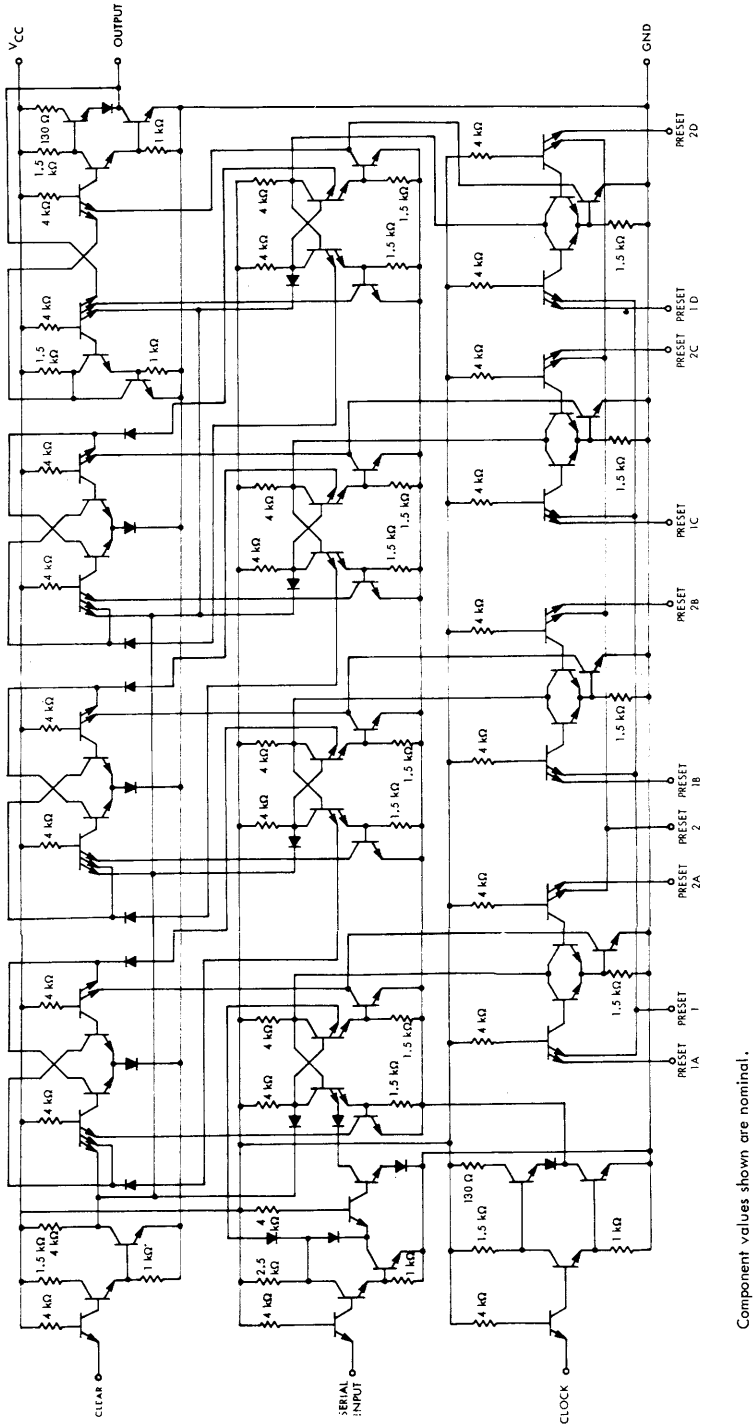
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF,	R_L = 400 Ω	10			MHz
t_{pd1}	Propagation delay time to logical 1 level from clock to output	C_L = 15 pF,	R_L = 400 Ω		25	40	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_L = 15 pF,	R_L = 400 Ω		25	40	ns
t_{pd1}	Propagation delay time to logical 1 level from preset to output	C_L = 15 pF,	R_L = 400 Ω			35	ns
t_{pd0}	Propagation delay time to logical 0 level from clear to output	C_L = 15 pF,	R_L = 400 Ω			40	ns

functional block diagram



schematic



Component values shown are nominal.

9

TEXAS INSTRUMENTS
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CIRCUIT TYPES SN5495A, SN7495A
4-BIT RIGHT-SHIFT LEFT-SHIFT REGISTERS

A TTL MSI PARALLEL-IN PARALLEL-OUT REGISTER

for application as

- N-Bit Serial-To-Parallel Converter
- N-Bit Parallel-To-Serial Converter
- N-Bit Storage Register

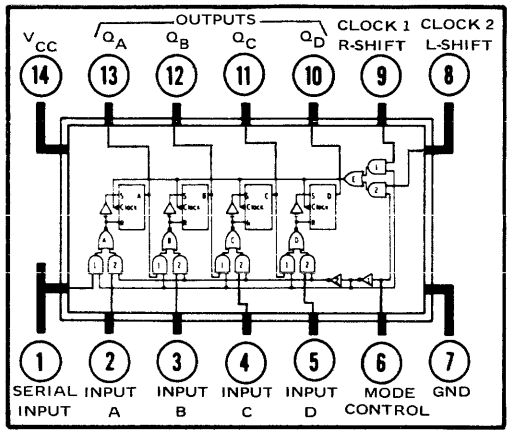
description

This monolithic shift register, utilizing transistor-transistor-logic (TTL) circuits in the familiar Series 54/74 configuration, is composed of four R-S master-slave flip-flops, four AND-OR-INVERT gates, one AND-OR gate, and six inverters-drivers. Internal interconnections of these functions provide a versatile register which will perform right-shift or left-shift operations dependent upon the logical input level to the mode control. A number of these registers may be connected in series to form an n-bit right-shift or left-shift register. This register can also be used as a parallel-in, parallel-out storage register with gate (mode) control.

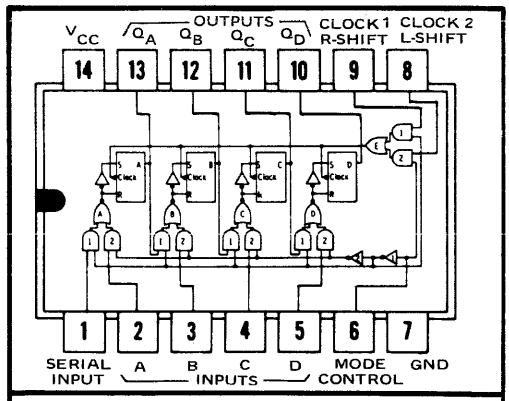
When a logical 0 level is applied to the mode control input, the number-1 AND gates are enabled and the number-2 AND gates are inhibited. In this mode the output of each flip-flop is coupled to the R-S inputs of the succeeding flip-flop and right-shift operation is performed by clocking at the clock 1 input. In this mode, serial data is entered at the serial input. Clock 2 and parallel inputs A through D are inhibited by the number-2 AND gates.

When a logical 1 level is applied to the mode control input, the number-1 AND gates are inhibited (decoupling the outputs from the succeeding R-S inputs to prevent right-shift) and the number-2 AND gates are enabled to allow entry of data through parallel inputs A through D and clock 2. This mode permits parallel loading of the register, or with external interconnection, shift-left operation. In this mode, shift-left can be accomplished by connecting the output of each flip-flop to the parallel input of the previous flip-flop (Q_D to input C, and etc.), and serial data is entered at input D.

W
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic

Mode control = 0 for right shift
Mode control = 1 for left shift or parallel load

Clocking for the shift register is accomplished through the AND-OR gate E which permits separate clock sources to be used for the shift-right and shift-left modes. If both modes can be clocked from the same source, the clock input may be applied commonly to clock 1 and clock 2. Information must be present at the R-S inputs of the master-slave flip-flops prior to clocking. Transfer of information to the output pins occurs when the clock input goes from a logical 1 to a logical 0.

This shift register is completely compatible with Series 54/74 TTL and DTL logic families. Average power dissipation is typically 195 milliwatts. The SN5495A and SN7495A are unilaterally interchangeable with and replace SN5495 and SN7495, respectively, but offer diode-clamped inputs, improved speed, and reduced power dissipation.

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absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1) . . . . . 7 V
Input Voltage V_{in} (See Notes 1 and 2) . . . . . 5.5 V
Operating Free-Air Temperature Range: SN5495A Circuits . . . . . −55°C to 125°C
SN7495A Circuits . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1): SN5495A Circuits	4.5	5	5.5	V
SN7495A Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output: High logic level			20	
Low logic level			10	
Width of Clock Pulse $t_{p(clock)}$ (See Figure 9): SN5495A Circuits	20	10		ns
SN7495A Circuits	15	10		ns
Setup Time Required at Serial, A, B, C, or D Inputs t_{setup} (See Figure 9)	10			ns
Hold Time Required at Serial, A, B, C, or D Inputs t_{hold} (See Figure 9)	0			ns
Logical 0 Level Setup Time Required at Mode Control (t1 in Figure 10) (With Respect to Clock 1 input)	15			ns
Logical 1 Level Setup Time Required at Mode Control (t2 in Figure 10) (With Respect to Clock 2 input)	15			ns
Logical 0 Level Setup Time Required at Mode Control (t3 in Figure 10) (With Respect to Clock 2 input)	5			ns
Logical 1 Level Setup Time Required at Mode Control (t4 in Figure 10) (With Respect to Clock 1 input)	5			ns

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input voltages must be zero or positive with respect to network ground terminal.

electrical characteristics over recommended operating temperature range (unless otherwise noted)

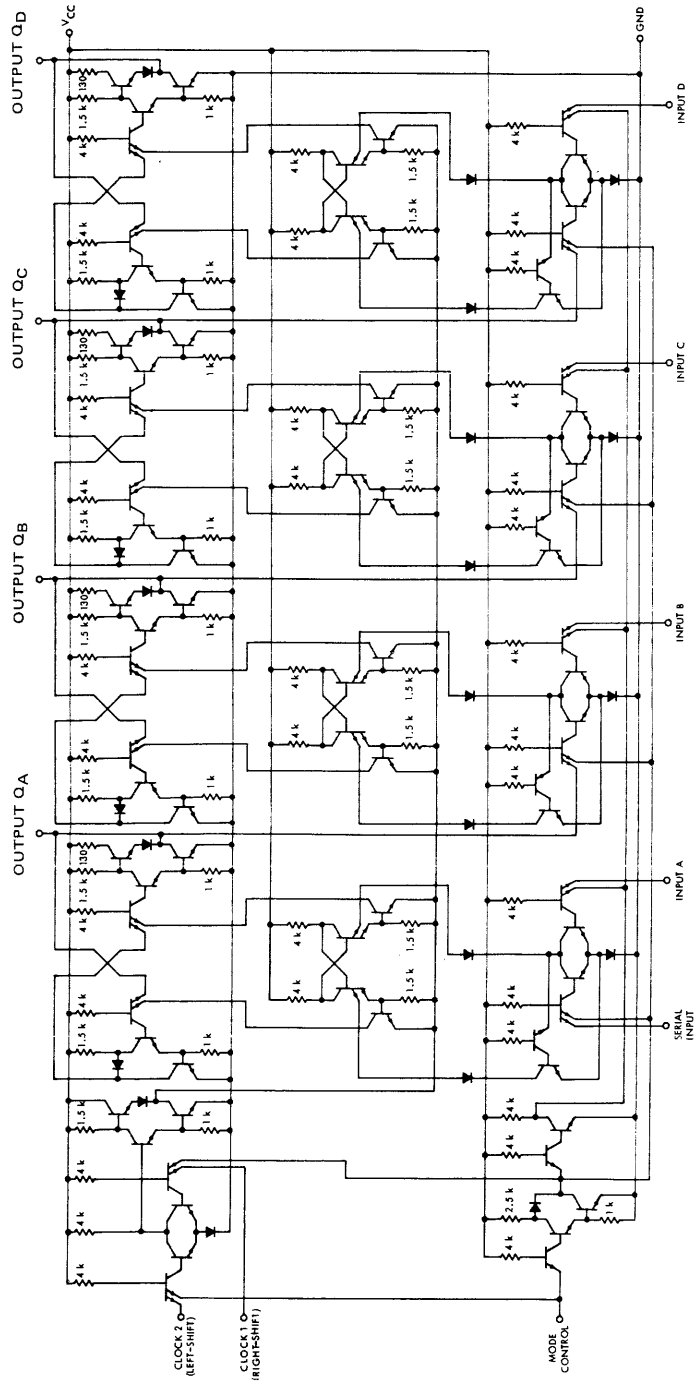
PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1 and 3		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	2 and 4				0.8	V
$V_{out(1)}$	Logical 1 output voltage	1 and 3	V_{CC} = MIN, I_{load} = −800 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	2 and 4	V_{CC} = MIN, I_{sink} = 16 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current at any input except mode control	5	V_{CC} = MAX, V_{in} = 0.4 V			−1.6	mA
$I_{in(0)}$	Logical 0 level input current at mode control	5	V_{CC} = MAX, V_{in} = 0.4 V			−3.2	mA
$I_{in(1)}$	Logical 1 level input current at any input except mode control	6	V_{CC} = MAX, V_{in} = 2.4 V			40	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at mode control	6	V_{CC} = MAX, V_{in} = 2.4 V			80	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current§	7	V_{CC} = MAX	−18		−57	mA
I_{CC}	Supply current	8	V_{CC} = MAX	39		63	mA

†For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions for the particular circuit type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS+	MIN	TYP	MAX	UNIT
f_{max}	Maximum shift frequency	9	C_L = 15 pF, R_L = 400 Ω	25	36		MHz
t_{pd1}	Propagation delay time to logical 1 level from clock 1 or clock 2 to outputs	9	C_L = 15 pF, R_L = 400 Ω		18	27	ns
t_{pd0}	Propagation delay time to logical 0 level from clock 1 or clock 2 to outputs	9	C_L = 15 pF, R_L = 400 Ω		21	32	ns

schematic



NOTES: 1. Resistor values are in ohms.
2. Component values shown are nominal.

d-c test circuits†

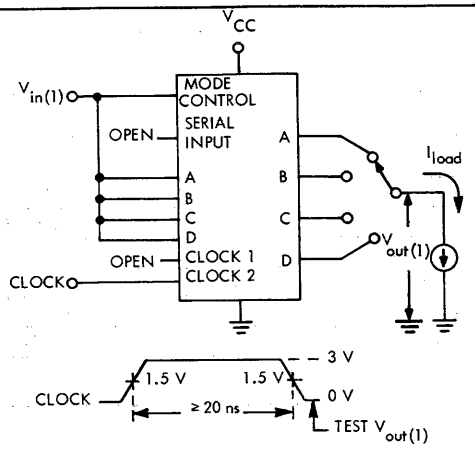


FIGURE 1

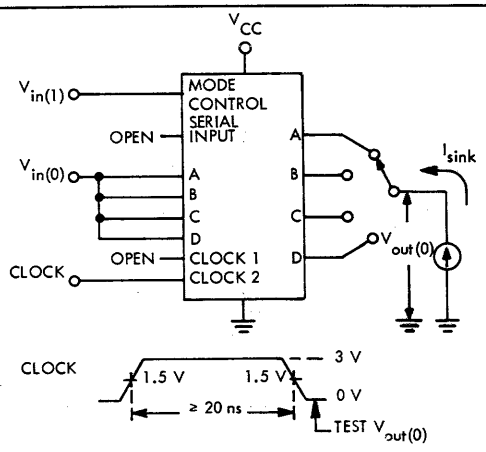


FIGURE 2

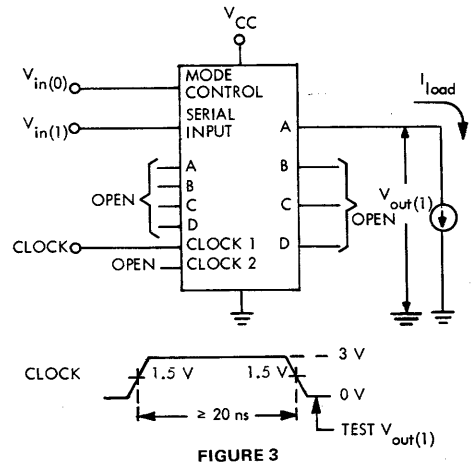


FIGURE 3

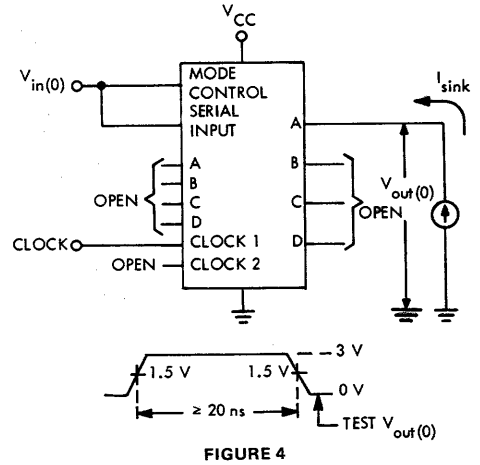
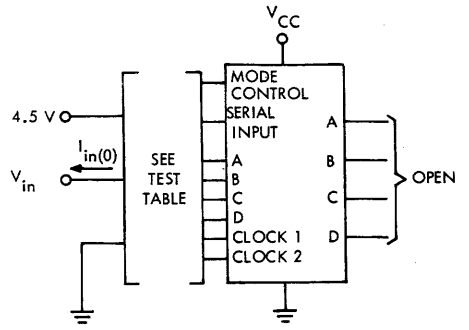


FIGURE 4



1. Each input is tested separately.

TEST TABLE

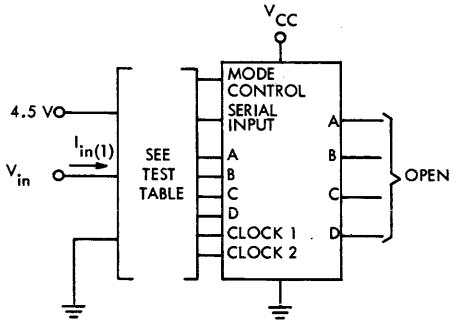
TEST	APPLY 4.5 V	APPLY GND
MODE CONTROL	CLOCK 2	NONE
SERIAL INPUT	NONE	MODE CONTROL
INPUT A	MODE CONTROL	NONE
INPUT B	MODE CONTROL	NONE
INPUT C	MODE CONTROL	NONE
INPUT D	MODE CONTROL	NONE
CLOCK 1	NONE	MODE CONTROL
CLOCK 2	MODE CONTROL	NONE

FIGURE 5

†Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

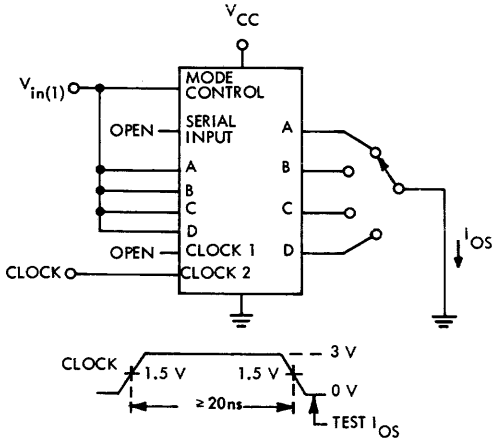
d-c test circuits† (continued)



TEST TABLE

TEST	APPLY 4.5 V	APPLY GND
MODE CONTROL	NONE	CLOCK 2
SERIAL INPUT	MODE CONTROL	NONE
INPUT A	NONE	MODE CONTROL
INPUT B	NONE	MODE CONTROL
INPUT C	NONE	MODE CONTROL
INPUT D	NONE	MODE CONTROL
CLOCK 1	MODE CONTROL	NONE
CLOCK 2	NONE	MODE CONTROL

FIGURE 6



1. Each output is tested separately.

FIGURE 7

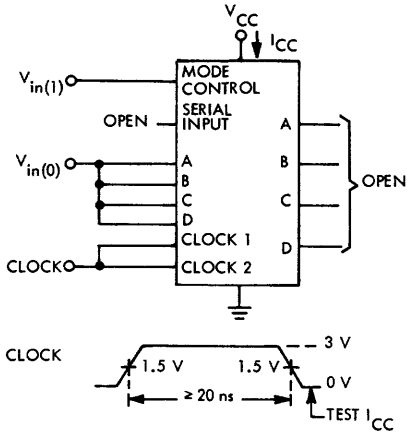
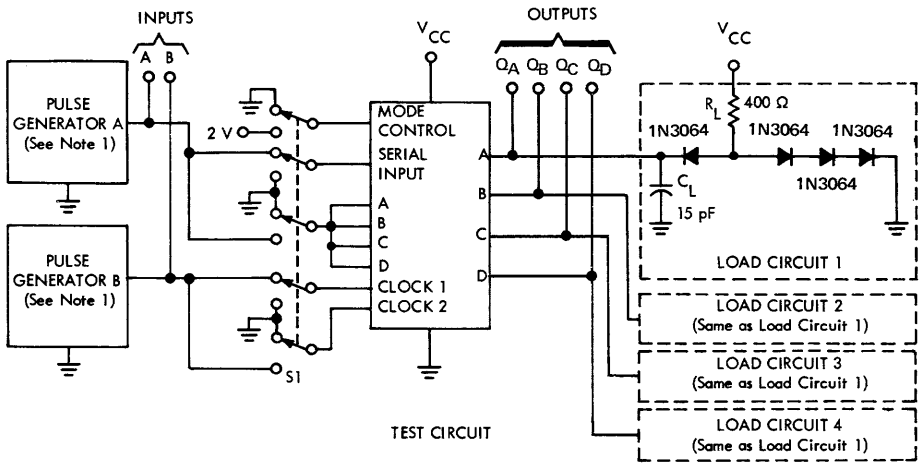


FIGURE 8

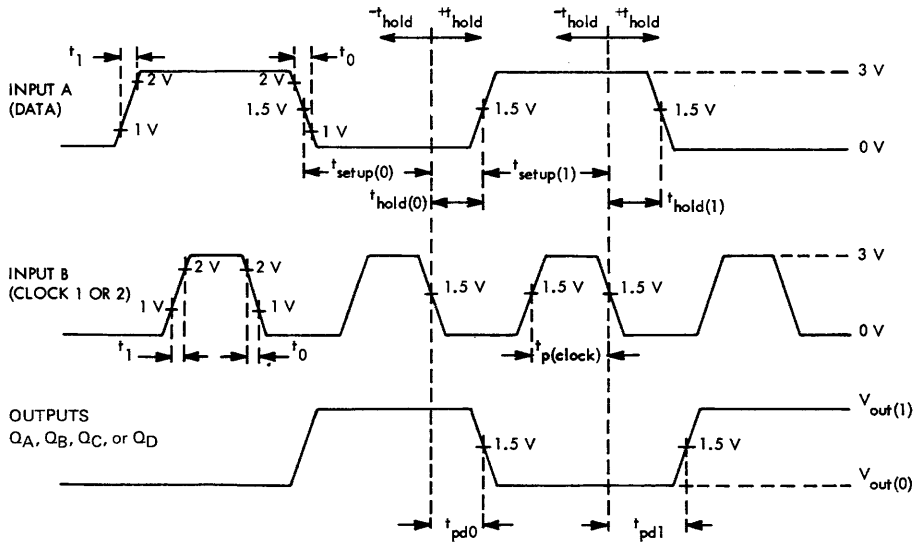
†Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

switching charateristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: 1. The pulse generators have the following characteristics: V_{gen} = 3 V, $t_1 = t_0 \leq$ 10 ns, and $Z_{out} \approx 50\ \Omega$. For pulse generator A : $t_p \geq$ 20 ns and PRR = 500 kHz. For pulse generator B : $t_p \geq$ 15 ns and PRR = 1 MHz. When testing f_{max} vary PRR.

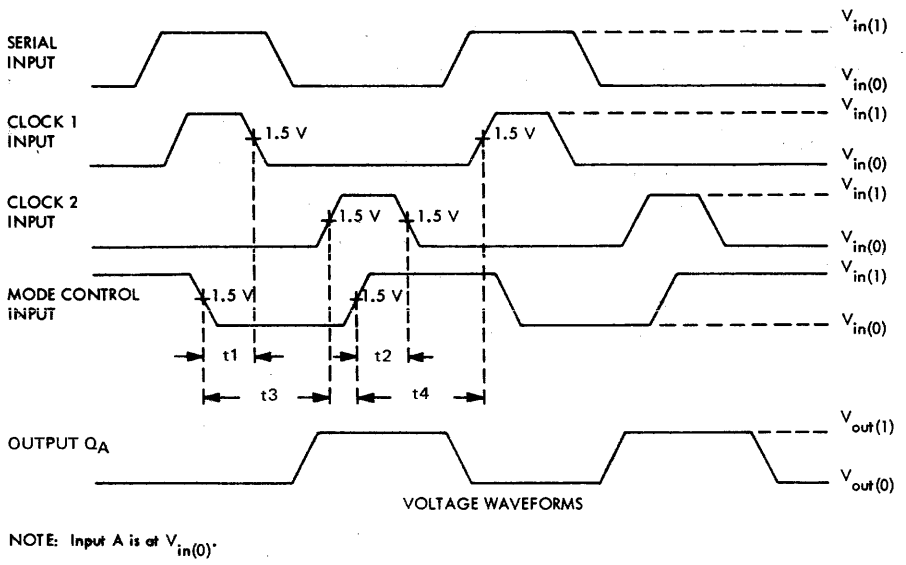
2. Voltage values are with respect to network ground terminal.
3. C_L includes probe and jig capacitance.

FIGURE 9–SWITCHING TIMES

9

PARAMETER MEASUREMENT INFORMATION

recommended mode control setup times



NOTE: Input A is at $V_{in(0)}$.

FIGURE 10–MODE CONTROL SETUP TIMES

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CIRCUIT TYPES SN54L95, SN74L95
4-BIT RIGHT-SHIFT LEFT-SHIFT REGISTERS

A SERIES 54L/74L PARALLEL-IN PARALLEL-OUT REGISTER
for application as

- N-Bit Serial-To-Parallel Converter
- N-Bit Parallel-To-Serial Converter
- N-Bit Storage Register

description

This monolithic shift register, utilizing transistor-transistor logic (TTL) circuits in the familiar Series 54L/74L configuration, is composed of four R-S master-slave flip-flops, four AND-OR-INVERT gates, one AND-OR gate, and six inverter-drivers. Internal interconnections of these functions provide a versatile register which will perform right-shift or left-shift operations dependent upon the logical input level to the mode control. A number of these registers may be connected in series to form an n-bit right-shift or left-shift register. This register can also be used as a parallel-in, parallel-out storage register with gate (mode) control.

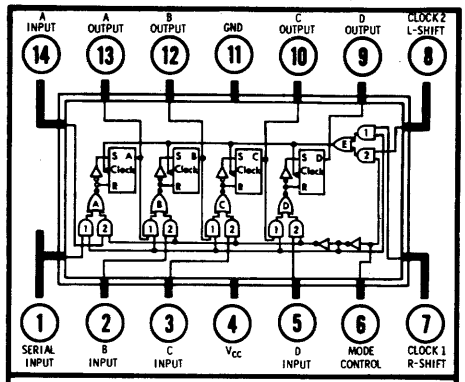
When a logical 0 level is applied to the mode control input, the number 1 AND gates are enabled and the number 2 AND gates are inhibited. In this mode the output of each flip-flip is coupled to the R-S inputs of the succeeding flip-flop, right-shift operation is performed by clocking at the clock 1 input, and serial data is entered at the serial input. Clock 2 and parallel inputs A through D are inhibited by the number 2 AND gates.

When a logical 1 level is applied to the mode-control input, the number 1 AND gates are inhibited (decoupling the outputs from the succeeding R-S inputs to prevent right-shift) and the number 2 AND gates are enabled to allow entry of data through parallel inputs A through D and clock 2. This mode permits parallel loading of the register or, with external interconnection, shift-left operation. In this mode, shift-left can be accomplished by connecting the output of each flip-flop to the parallel input of the previous flip-flop (D output to input C, and etc.), and serial data is entered at input D.

Clocking for the shift register is accomplished through the AND-OR gate E which permits separate clock sources to be used for the shift-right and shift-left modes. If both modes can be clocked from the same source, the clock input may be applied commonly to clock 1 and clock 2. Information must be present at the R-S inputs of the master-slave flip-flops prior to clocking.

The shift register is completely compatible for use with TTL and DTL logic families. Average power dissipation is typically 19 milliwatts.

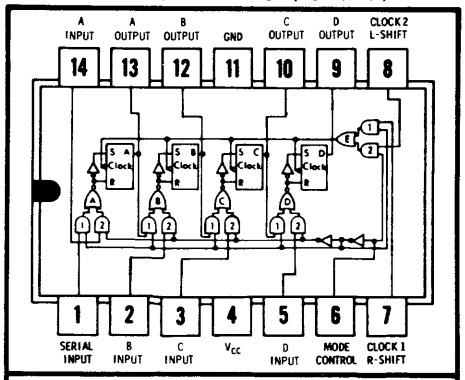
T
FLAT PACKAGE (TOP VIEW)



positive logic

Mode Control = 0 for right shift
Mode Control = 1 for left shift or parallel load

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic

Mode Control = 0 for right shift
Mode Control = 1 for left shift or parallel load

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1) . . . . . 8 V
Input Voltage, V_{in} (See Notes 1 and 2) . . . . . 5.5 V
Operating Free-Air Temperature Range: SN54L95 Circuits . . . . . -55°C to 125°C
SN74L95 Circuits . . . . . 0°C to 70°C
Storage Temperature Range . . . . . -65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input voltages must be zero or positive with respect to network ground terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1): SN54L95 Circuits	4.5	5	5.5	V
SN74L95 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output			10	
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 9)	200			ns
Logical 1 Setup Time Required at Serial, A, B, C, or D Inputs, $t_{setup(1)}$ (See Figure 9)	100			ns
Logical 0 Setup Time Required at Serial, A, B, C, or D Inputs, $t_{setup(0)}$	120			ns
Hold Time Required at Serial, A, B, C, or D Inputs, t_{hold} (See Figure 9)	0			ns
Logical 0 Level Setup Time Required at Mode Control (t1 in Figure 10) (With Respect to Clock 1 Input)	225			ns
Logical 1 Level Setup Time Required at Mode Control (t2 in Figure 10) (With Respect to Clock 2 Input)	200			ns
Logical 0 Level Setup Time Required at Mode Control (t3 in Figure 10) (With Respect to Clock 2 Input)	0			ns
Logical 1 Level Setup Time Required at Mode Control (t4 in Figure 10) (With Respect to Clock 1 Input)	100			ns

NOTE: 1. Voltage values are with respect to network ground terminal.

electrical characteristics (over operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS †	MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1 and 3		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	2 and 4				0.7	V
$V_{out(1)}$	Logical 1 output voltage	1 and 3	V_{CC} = MIN, $V_{in(1)}$ = 2 V, $V_{in(0)}$ = 0.7 V, I_{load} = −100 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	2 and 4	V_{CC} = MIN, $V_{in(1)}$ = 2 V, $V_{in(0)}$ = 0.7 V, I_{sink} = 2 mA		0.16	0.3	V
$I_{in(0)}$	Logical 0 level input current at any input except mode control	5	V_{CC} = MAX, V_{in} = 0.3 V			-0.18	mA
$I_{in(0)}$	Logical 0 level input current at mode control	5	V_{CC} = MAX, V_{in} = 0.3 V			-0.36	mA
$I_{in(1)}$	Logical 1 level input current at any input except mode control	6	V_{CC} = MAX, V_{in} = 2.4 V			10	μA
			V_{CC} = MAX, V_{in} = 5.5 V			100	μA
$I_{in(1)}$	Logical 1 level input current at mode control	6	V_{CC} = MAX, V_{in} = 2.4 V			20	μA
			V_{CC} = MAX, V_{in} = 5.5 V			200	μA
I_{OS}	Short-circuit output current §	7	V_{CC} = MAX, V_{in} = 4.5 V	-3		-15	mA
I_{CC}	Supply current	8	V_{CC} = MAX, $V_{in(1)}$ = 4.5 V, $V_{in(0)}$ = 0		3.8	9	mA

† For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions for the applicable device type.

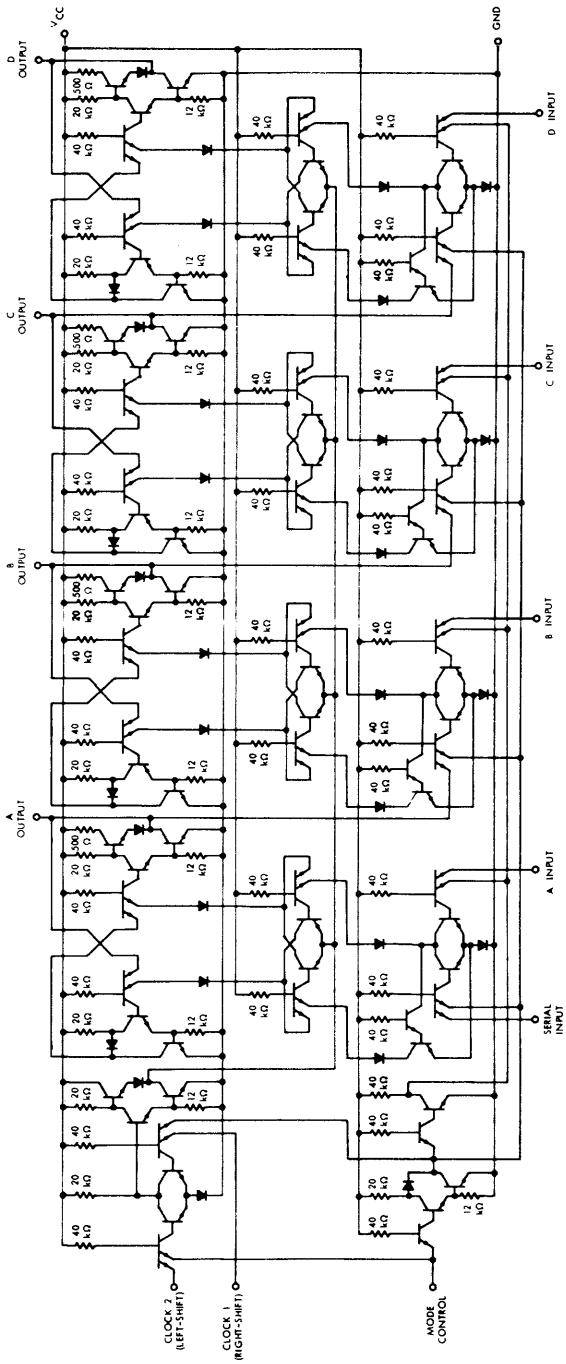
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum shift frequency	9	C_L = 50 pF, R_L = 4 kΩ	3	5		MHz
t_{pd1}	Propagation delay time to logical 1 level from clock 1 or clock 2 to outputs	9	C_L = 50 pF, R_L = 4 kΩ		115	200	ns
t_{pd0}	Propagation delay time to logical 0 level from clock 1 or clock 2 to outputs	9	C_L = 50 pF, R_L = 4 kΩ		125	200	ns

schematic



NOTE: Component values shown are nominal.

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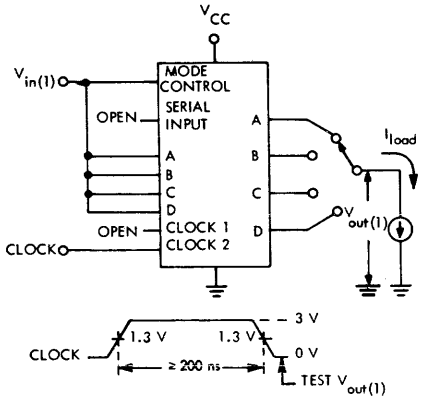
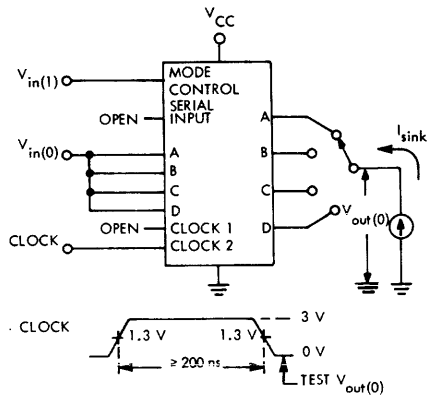
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



1. Each output is tested separately.

FIGURE 1



1. Each output is tested separately.

FIGURE 2

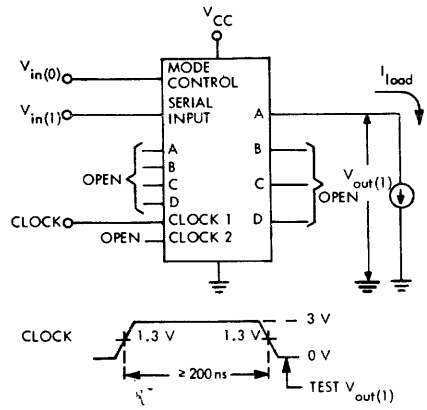


FIGURE 3

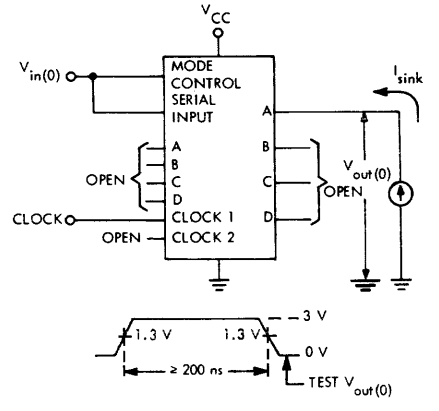
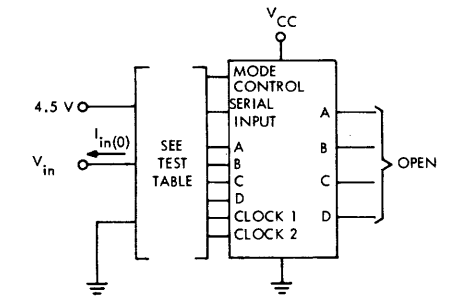


FIGURE 4



TEST TABLE

TEST	APPLY 4.5 V	APPLY GND
MODE CONTROL	CLOCK 2	NONE
SERIAL INPUT	NONE	MODE CONTROL
A INPUT	MODE CONTROL	NONE
B INPUT	MODE CONTROL	NONE
C INPUT	MODE CONTROL	NONE
D INPUT	MODE CONTROL	NONE
CLOCK 1	NONE	MODE CONTROL
CLOCK 2	MODE CONTROL	NONE

1. Each input is tested separately.

FIGURE 5

† Arrows indicate actual direction of current flow.

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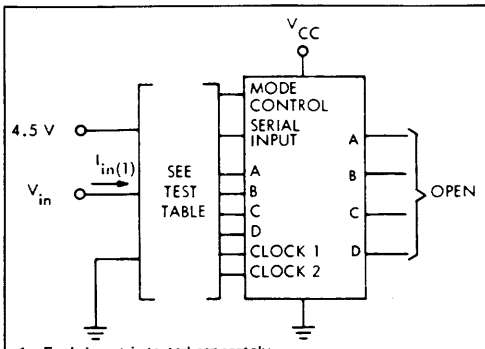
PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

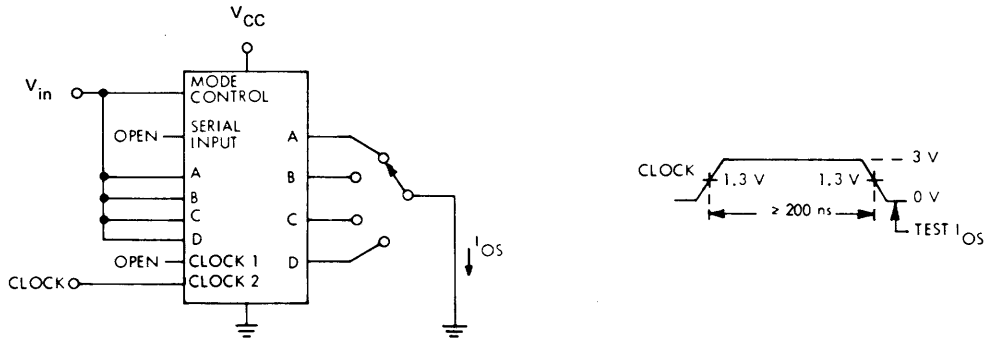


TEST TABLE

TEST	APPLY 4.5 V	APPLY GND
MODE CONTROL	NONE	CLOCK 2
SERIAL INPUT	MODE CONTROL	NONE
A INPUT	NONE	MODE CONTROL
B INPUT	NONE	MODE CONTROL
C INPUT	NONE	MODE CONTROL
D INPUT	NONE	MODE CONTROL
CLOCK 1	MODE CONTROL	NONE
CLOCK 2	NONE	MODE CONTROL

1. Each input is tested separately.

FIGURE 6



1. Each output is tested separately.

FIGURE 7

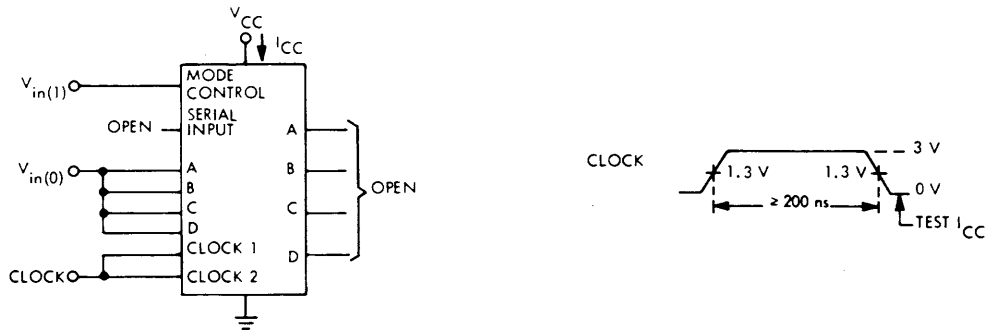


FIGURE 8

† Arrows indicate actual direction of current flow.

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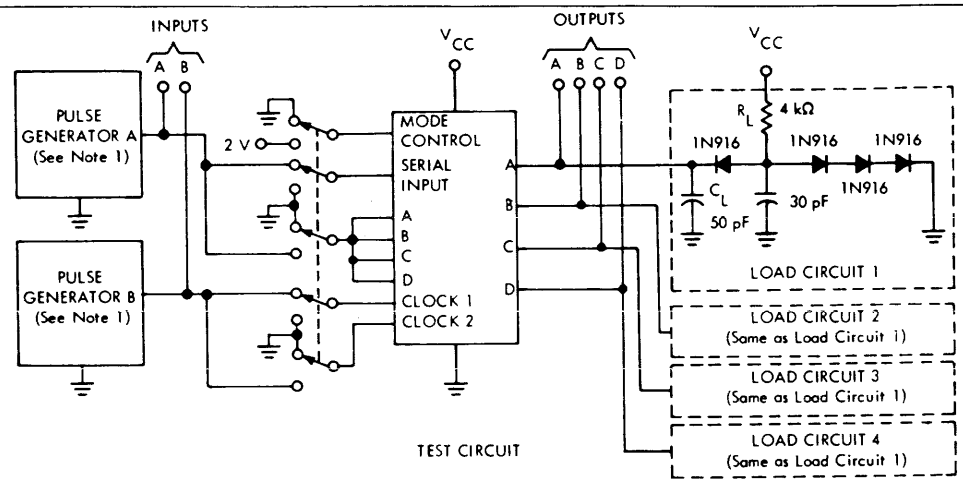
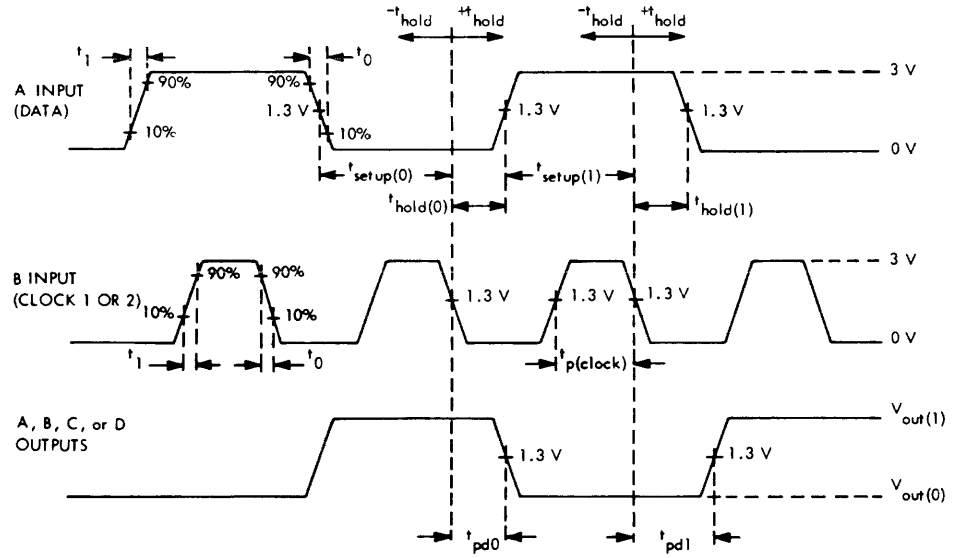
PARAMETER MEASUREMENT INFORMATION

switching characteristics





NOTES: 1. The pulse generators have the following characteristics: t_1 = 10 ns to 12 ns, t_0 = 10 ns to 12 ns, and $Z_{out} \approx 50\ \Omega$.
For pulse generator A : $t_p \geq 150$ ns and PRR $\leq$ 500 kHz. For pulse generator B : $t_p \geq 10$ ns and PRR $\leq$ 1 MHz.
When testing f_{max}, vary PRR.
2. Voltage values are with respect to network ground terminal.
3. C_L includes probe and jig capacitance.

FIGURE 9 – SWITCHING TIMES

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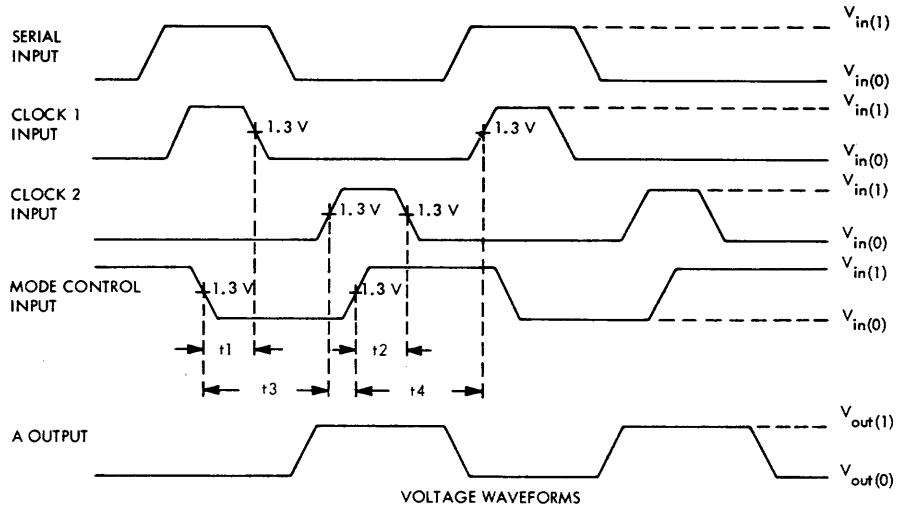
PARAMETER MEASUREMENT INFORMATION

recommended mode control setup times



NOTE: A Input is at $V_{in(0)}$.

FIGURE 10—MODE CONTROL SETUP TIMES

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CIRCUIT TYPES SN5496, SN7496
5-BIT SHIFT REGISTERS

TTL MSI MULTIFUNCTION SHIFT REGISTERS

for application as

- N-Bit Serial-To-Parallel Converter
- N-Bit Parallel-To-Serial Converter
- N-Bit Storage Register

description

This shift register consists of five R-S master-slave flip-flops connected to perform parallel-to-serial or serial-to-parallel conversion of binary data. Since both inputs and outputs to all flip-flops are accessible, parallel-in/parallel-out or serial-in/serial-out operation may be performed.

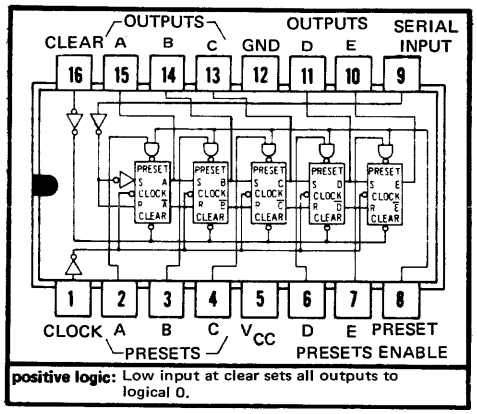
All flip-flops are simultaneously set to the logical 0 state by applying a logical 0 voltage to the clear input. This condition may be applied independent of the state of the clock input.

The flip-flops may be independently set to the logical 1 state by applying a logical 1 to both the preset input of the specific flip-flop and the common preset input. The preset-enable input is provided to allow flexibility of either setting each flip-flop independently or setting two or more flip-flops simultaneously. Preset is also independent of the state of the clock input or clear input.

Transfer of information to the output pins occurs when the clock input goes from a logical 0 to a logical 1. Since the flip-flops are R-S master-slave circuits, the proper information must appear at the R-S inputs of each flip-flop prior to the rising edge of the clock input voltage waveform. The serial input provides this information to the first flip-flop, while the outputs of the subsequent flip-flops provide information for the remaining R-S inputs. The clear input must be at a logical 1 and the preset input must be at a logical 0 when clocking occurs.

This shift register is completely compatible with Series 54/74 TTL and DTL logic families. Typically, average power dissipation is 240 milliwatts, and propagation delay time is 25 nanoseconds.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: Low input at clear sets all outputs to logical 0.

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absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1)		7 V
Input Voltage, V_{in} (See Notes 1 and 2)		5.5 V
Operating Free-Air Temperature Range:	SN5496 Circuits	−55°C to 125°C
	SN7496 Circuits	0°C to 70°C
Storage Temperature Range		−65°C to 150°C

NOTES: 1. These voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

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recommended operating conditions

	MIN	TYP	MAX	UNIT
Supply Voltage V_{CC} (See Note 1): SN5496 Circuits	4.5	5	5.5	V
SN7496 Circuits	4.75	5	5.25	V
Normalized Fan-Out from Output			10	
Width of Clock Pulse, $t_{p(clock)}$	35			ns
Width of Clear Pulse, $t_{p(clear)}$	30			ns
Width of Preset Pulse, $t_{p(preset)}$	30			ns
Serial Input Setup Time, t_{setup}	30			ns
Serial Input Hold Time, t_{hold}	0			ns

NOTE 1: This voltage value is with respect to network ground terminal.

electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage			2			V
$V_{in(0)}$	Logical 0 input voltage					0.8	
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = −400 μA		2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 16 mA			0.22	0.4	V
$I_{in(1)}$	Logical 1 level input current at any input except preset-enable	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
		V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at preset-enable	V_{CC} = MAX, V_{in} = 2.4 V				200	μA
		V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(0)}$	Logical 0 level input current at any input except preset-enable	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(0)}$	Logical 0 level input current at preset-enable	V_{CC} = MAX, V_{in} = 0.4 V				−8	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX, V_{out} = 0	SN5496	−20		−57	mA
			SN7496	−18		−57	mA
I_{CC}	Supply current	V_{CC} = MAX	SN5496		48	68	mA
			SN7496		48	79	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the particular circuit type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

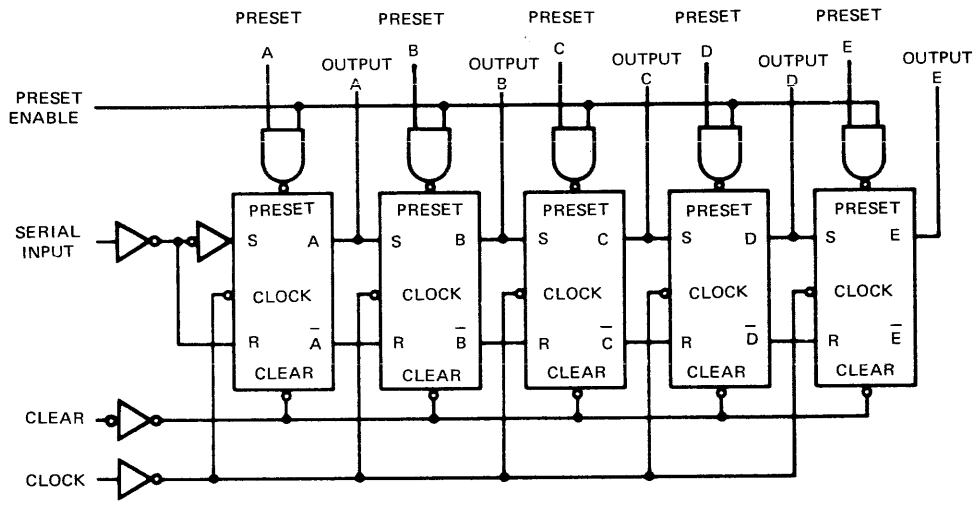
§ Not more than one output should be shorted at a time.

9

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 400 Ω	10			MHz
t_{pd1}	Propagation delay time to logical 1 level from clock to output	C_L = 15 pF, R_L = 400 Ω		25	40	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_L = 15 pF, R_L = 400 Ω		25	40	ns
t_{pd1}	Propagation delay time to logical 1 level from preset or preset-enable to output	C_L = 15 pF, R_L = 400 Ω		28	35	ns
t_{pd0}	Propagation delay time to logical 0 level from clear to output	C_L = 15 pF, R_L = 400 Ω			55	ns

functional block diagram



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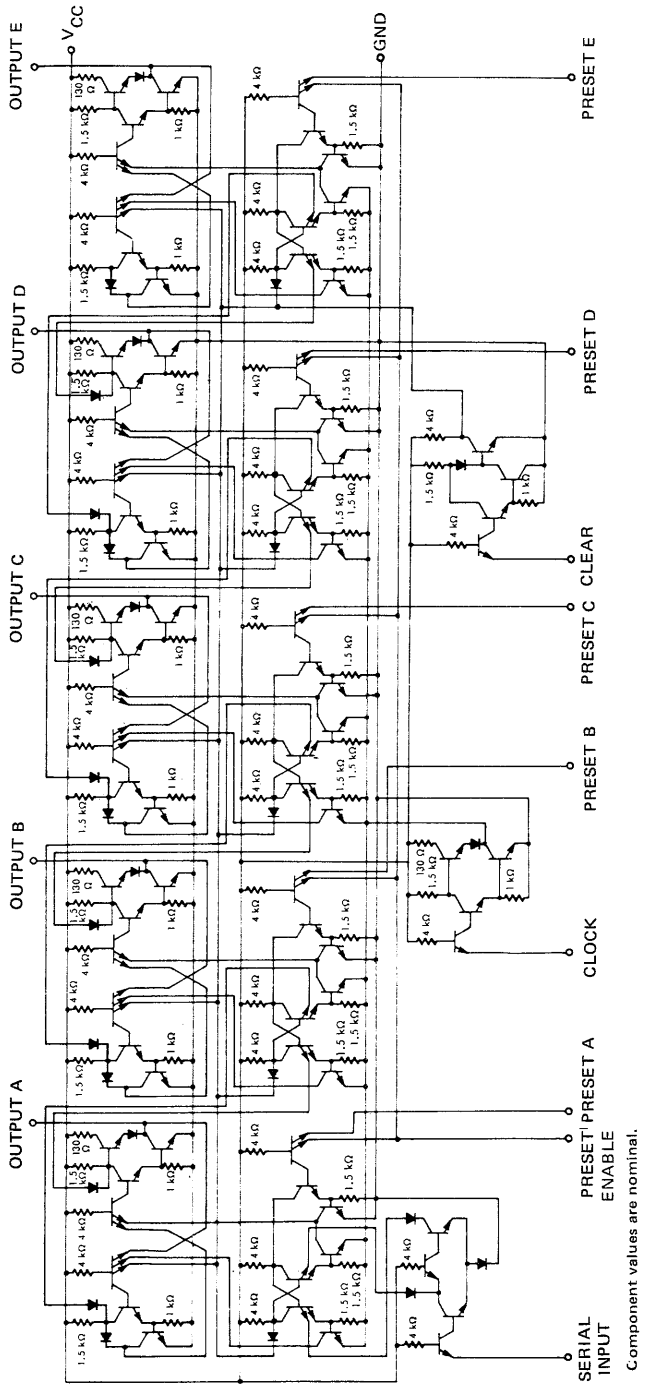
schematic



TEXAS INSTRUMENTS
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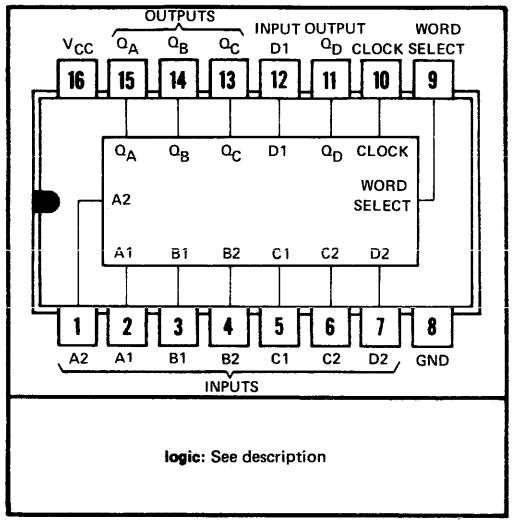
CIRCUIT TYPES SN54L98, SN74L98
4-BIT DATA SELECTORS/STORAGE REGISTERS

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



logic: See description

description

These monolithic data selectors/storage registers are composed of four S-R master-slave flip-flops, four AND-OR-INVERT gates, one buffer, and six inverter/drivers.

When the word select input is low, word 1 (A1, B1, C1, D1) is applied to the flip-flops. A high input to word select will cause the selection of word 2 (A2, B2, C2, D2). The selected word is shifted to the output terminals on the negative-going edge of the clock pulse.

Typical power dissipation is 25 mW. The SN54L98 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74L98 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) . . . . . 8 V
Input voltage (see Notes 1 and 2) . . . . . 5.5 V
Operating free-air temperature range: SN54L98 Circuits . . . . . −55°C to 125°C
SN74L98 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

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NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input voltages must be zero or positive with respect to network ground terminal.

recommended operating conditions

		SN54L98			SN74L98			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N				10			10	
Width of clock pulse, $t_{w(clock)}$ (see Figure 6)		200			200			ns
Setup time for high-level data, $t_{setup(H)}$ (see Note 3 and Figure 6)	at A, B, C, or D	100			100			ns
	at word select	150			150			
Setup time for low-level data, $t_{setup(L)}$ (see Note 3 and Figure 6)	at A, B, C, or D	120			120			ns
	at word select	100			100			
Operating free-air temperature range, T_A		−55	25	125	0	25	70	°C

NOTE 3: Setup time is the interval immediately preceding the negative-going edge of the clock pulse, during which interval the data to be recognized must be maintained at the input to ensure its recognition.

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electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
V_{IH}	High-level input voltage	1 and 2		2		V
V_{IL}	Low-level input voltage	1 and 2			0.7	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, I_{OH} = −100 μA	2.4		V
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, I_{OL} = 2 mA		0.3	V
I_{IH}	High-level input current into any input except word select	3	V_{CC} = MAX, V_I = 2.4 V		10	μA
			V_{CC} = MAX, V_I = 5.5 V		100	
I_{IH}	High-level input current into word select	3	V_{CC} = MAX, V_I = 2.4 V		20	μA
			V_{CC} = MAX, V_I = 5.5 V		200	
I_{IL}	Low-level input current into any input except word select	3	V_{CC} = MAX, V_I = 0.3 V		−0.18	mA
I_{IL}	Low-level input current into word select	3	V_{CC} = MAX, V_I = 0.3 V		−0.36	mA
I_{OS}	Short-circuit output current§	4	V_{CC} = MAX	−3	−15	mA
I_{CC}	Supply current	5	V_{CC} = MAX		9	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	6	C_L = 50 pF, R_L = 4 kΩ	3	5		MHz
t_{PLH}	Propagation delay time, low-to-high-level output, from clock input				115	200	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from clock input				125	200	ns

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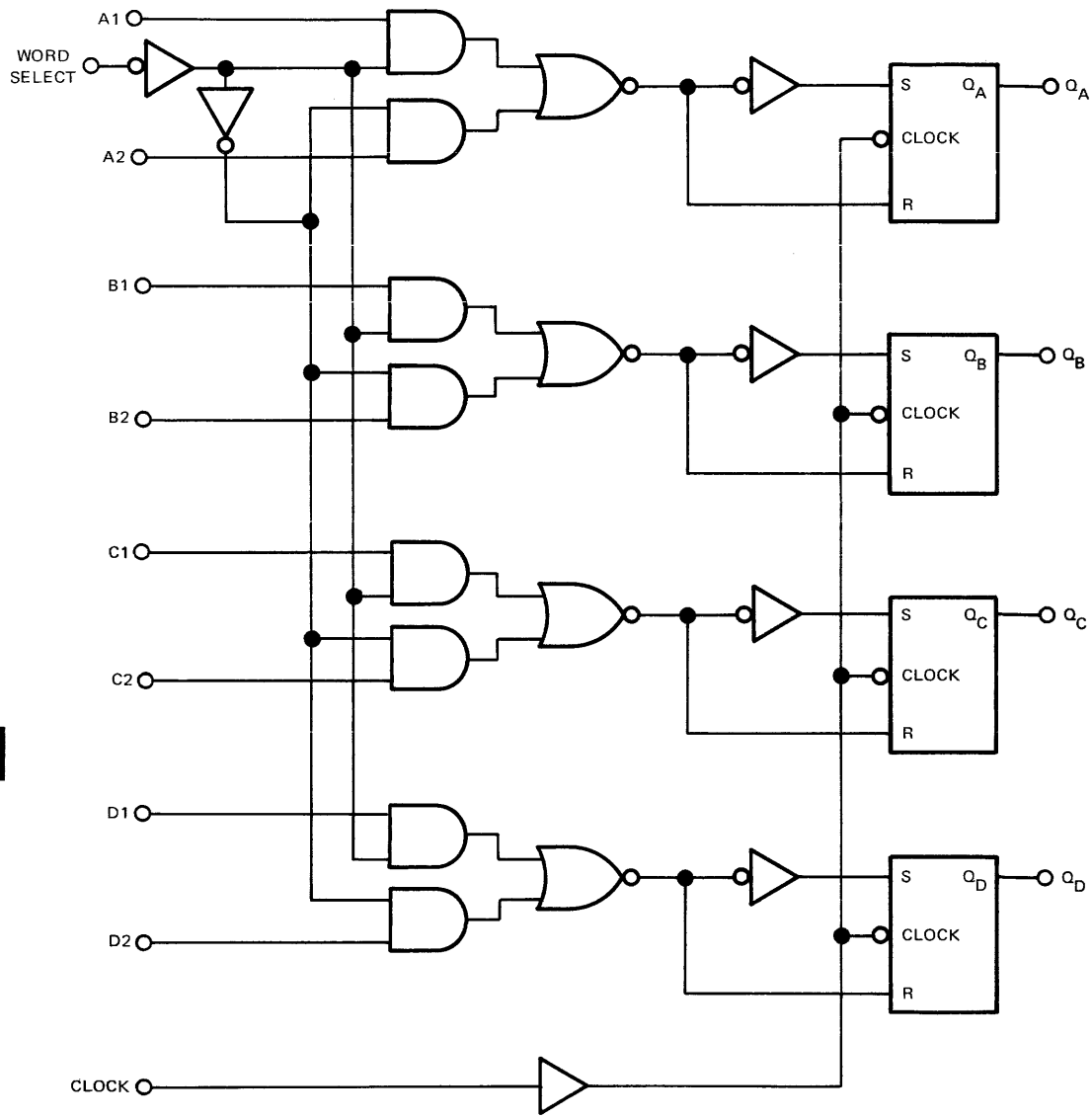
functional block diagram



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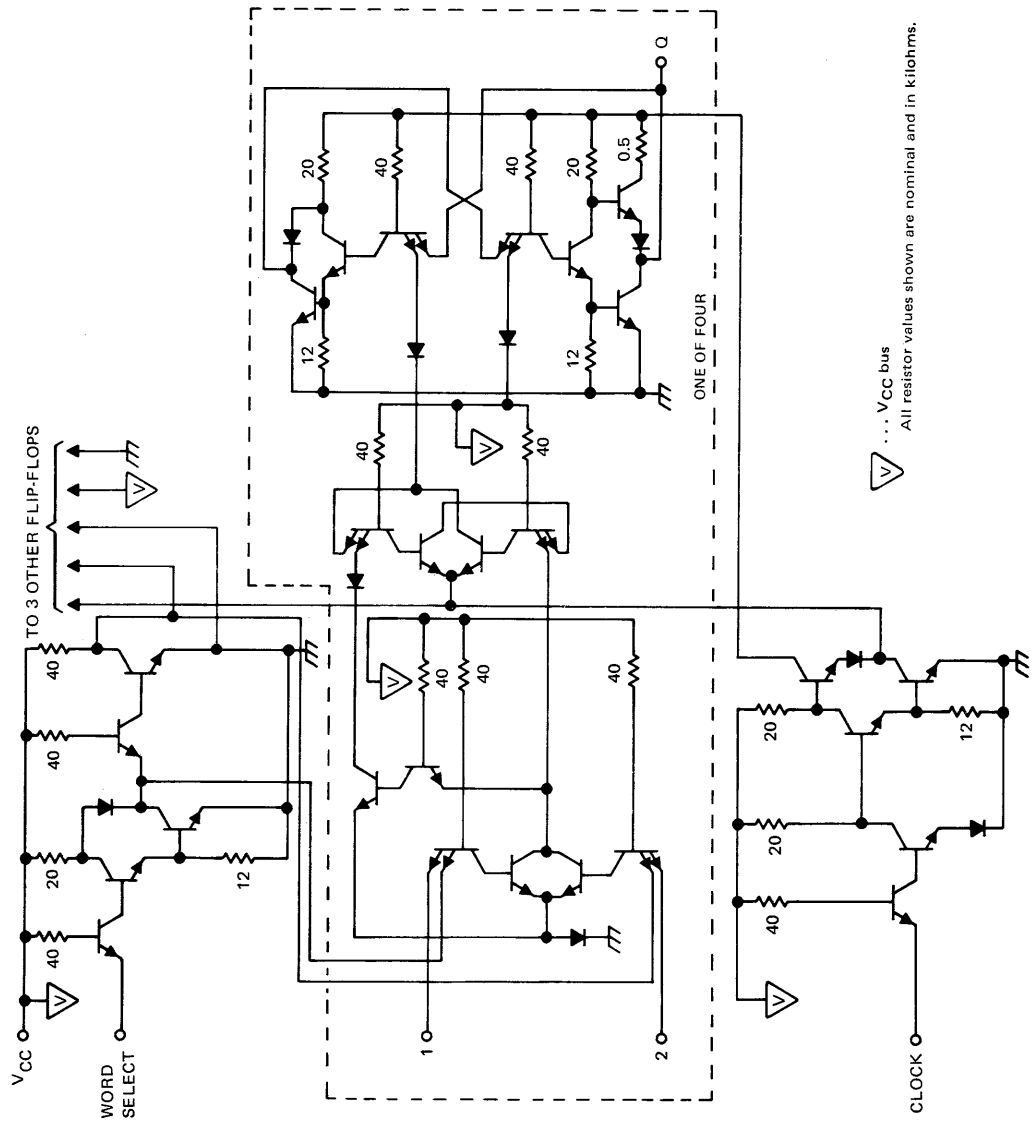
schematic


Q
ONE OF FOUR
TO 3 OTHER FLIP-FLOPS
V_{CC}
WORD SELECT
1
2
CLOCK
. . . V_{CC} bus
All resistor values shown are nominal and in kilohms.

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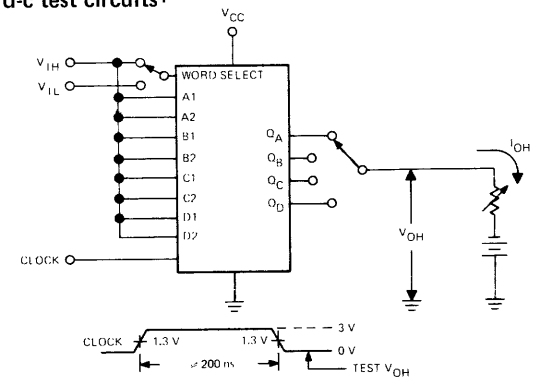
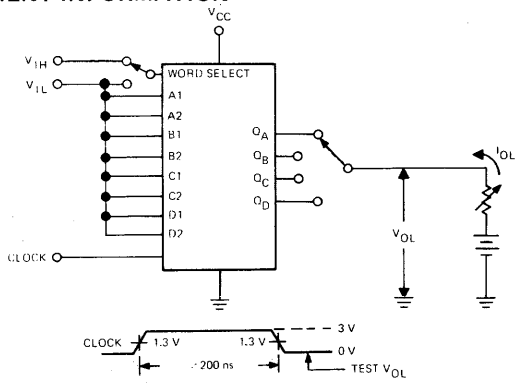
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



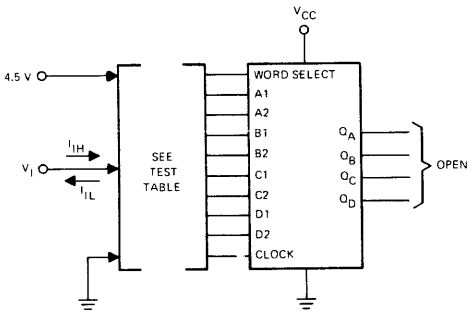
Each output is tested separately.

FIGURE 1–V_{IH}, V_{IL}, V_{OH}



Each output is tested separately.

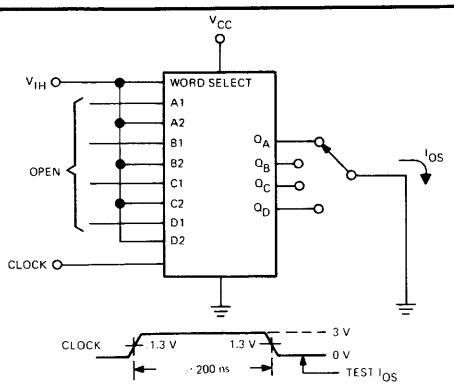
FIGURE 2–V_{IH}, V_{IL}, V_{OL}



TEST TABLE

APPLY V_I	TEST I_{IH}		TEST I_{IL}	
	APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND
A1, B1, C1, D1	WORD SELECT	NONE	NONE	WORD SELECT
A2, B2, C2, D2	NONE	WORD SELECT	WORD SELECT	NONE
WORD SELECT	NONE	NONE	NONE	NONE
CLOCK	NONE	NONE	NONE	NONE

FIGURE 3–I_{IH}, I_{IL}



Each output is tested separately.

FIGURE 4–I_{OS}

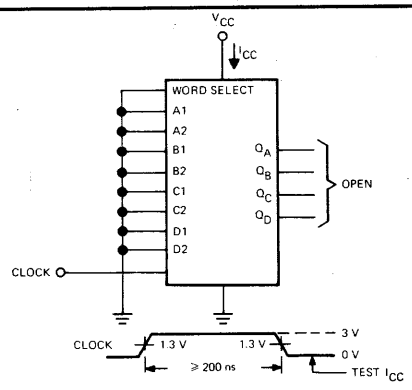


FIGURE 5–I_{CC}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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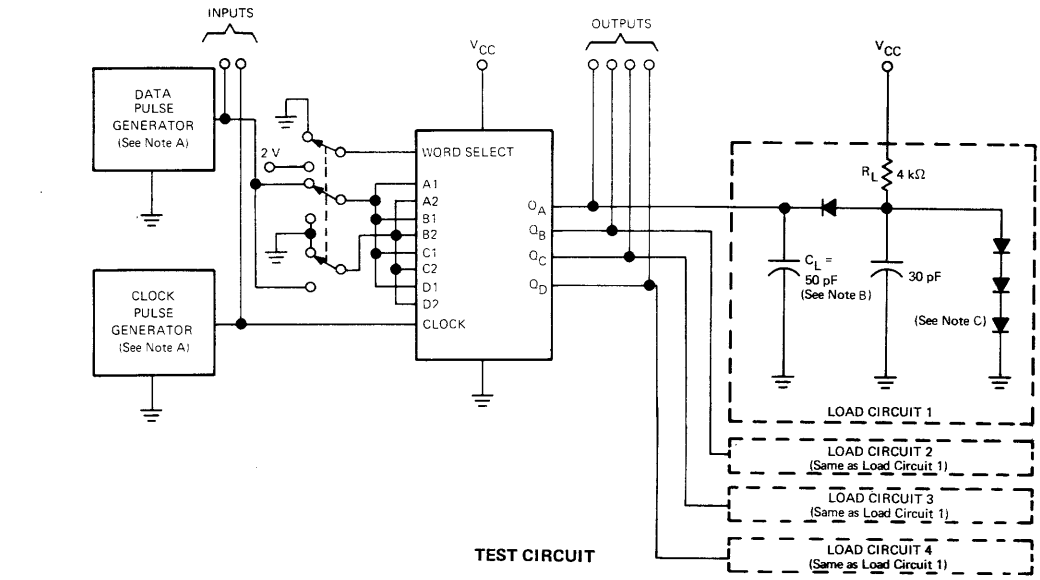
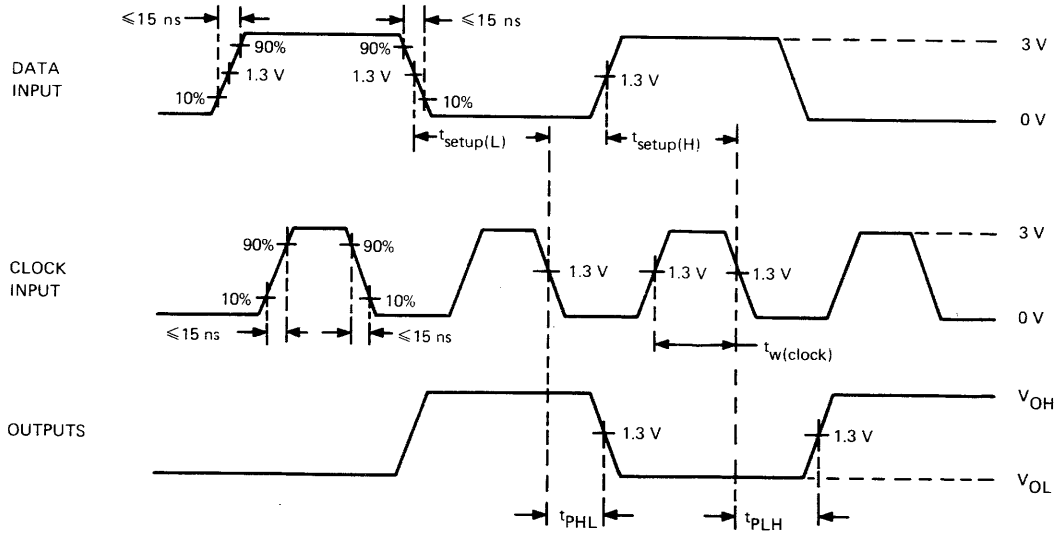
PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: $Z_{out} \approx 50\ \Omega$. For data pulse generator: $t_w \geq 150$ ns, PRR ≤ 500 kHz, $t_{setup(L)} = 120$ ns, and $t_{setup(H)} = 100$ ns. For clock pulse generator: $t_w \geq 200$ ns and PRR ≤ 1 MHz. When testing f_{max}, vary PRR.

B. C_L includes probe and jig capacitance.

C. All diodes are 1N916.

FIGURE 6–SWITCHING TIMES

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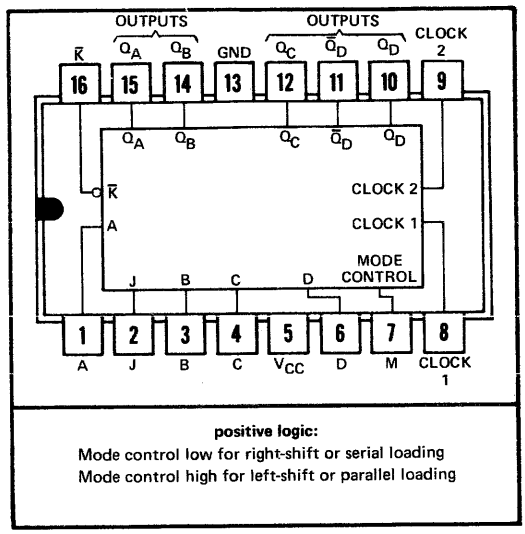
CIRCUIT TYPES SN54L99, SN74L99
4-BIT RIGHT-SHIFT LEFT-SHIFT REGISTERS

- N-Bit Serial-to-Parallel Converter
- N-Bit Parallel-to-Serial Converter
- N-Bit Storage Register
- J-$\overline{K}$ Serial Input

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic:
Mode control low for right-shift or serial loading
Mode control high for left-shift or parallel loading

description

This monolithic integrated circuit, utilizing transistor-transistor logic (TTL) in the familiar Series 54L/74L configuration, is composed of four master-slave flip-flops and the necessary gating to provide a versatile shift register or parallel-in, parallel-out storage register. The circuit has J and $\overline{K}$ inputs externally available. This permits the first stage to act as a J-$\overline{K}$, D-, or T-type flip-flop as shown in the following table. For additional examples, see the function tables on the last page of this data sheet.

Inputs at t_n			Outputs at t_{n+1}				
M	J	$\overline{K}$	Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
L	L	H	Q_{An}	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
L	L	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
L	H	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
L	H	L	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

H = high level, L = low level
NOTES: A. t_n = bit time before clock pulse
B. t_{n+1} = bit time after clock pulse
C. Q_{An} = state of Q_A at t_n

When a low-level input is applied to the mode control, the number 1 AND gates (see functional block diagram) are enabled and the number 2 AND gates are inhibited. In this mode, the output of each flip-flop is coupled to the S-R inputs of the succeeding flip-flop and right-shift operation is performed by clocking at the clock 1 input. Serial data is entered at the J-$\overline{K}$ inputs. Clock 2 and parallel inputs A through D are inhibited by the number 2 AND gates.

When a high-level input is applied to the mode control, the number 1 AND gates are inhibited (decoupling the outputs from the succeeding S-R inputs to prevent right-shift) and the number 2 AND gates are enabled to allow entry of data through parallel inputs A through D and clock 2. This mode permits parallel loading of the register or, with external interconnection, shift-left operation. In this mode, shift-left can be accomplished by connecting the output of each flip-flop to the parallel input of the previous flip-flop (Q_D to input C, and etc.), and serial data is entered at input D.

Clocking for the shift register is accomplished through an AND-OR gate which permits separate clock sources to be used for the shift-right and shift-left modes. If both modes can be clocked from the same source, the clock input may be applied commonly to clock 1 and 2. An inverted output is available from the last flip-flop.

This shift register is compatible for use with most TTL and DTL logic families. A number of these registers may be connected in series to form an n-bit right-shift or left-shift register. Average power dissipation is typically 19 mW.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) . . . . . 8 V
Input voltage (see Notes 1 and 2) . . . . . 5.5 V
Operating free-air temperature range: SN54L99 Circuits . . . . . −55°C to 125°C
SN74L99 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input voltages must be zero or positive with respect to network ground terminal.

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recommended operating conditions

	SN54L99			SN74L99			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Fan-out from each output, N			10			10	
Width of clock pulse, $t_{w(clock)}$ (see Figure 10)	200			200			ns
Setup time for high-level data at J, $\overline{K}$, A, B, C, or D inputs, $t_{setup(H)}$ (see Note 3 and Figure 10)	100			100			ns
Setup time for low-level data at J, $\overline{K}$, A, B, C, or D inputs, $t_{setup(L)}$ (see Note 3 and Figure 10)	120			120			ns
Hold time required at J, $\overline{K}$, A, B, C, or D inputs, t_{hold} (see Note 4 and Figure 10)	0			0			ns
Time to enable clock 1, $t_{enable\ 1}$ (see Figure 9)	225			225			ns
Time to enable clock 2, $t_{enable\ 2}$ (see Figure 9)	200			200			ns
Time to inhibit clock 1, $t_{inhibit\ 1}$ (see Figure 9)	100			100			ns
Time to inhibit clock 2, $t_{inhibit\ 2}$ (see Figure 9)	0			0			ns
Operating free-air temperature range, T_A	−55	25	125	0	25	70	°C

NOTES: 3. Setup time is the interval immediately preceeding the negative-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.

4. Hold time is the interval immediately following the negative-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its continued recognition.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS‡	MIN	TYP§	MAX	UNIT
V_{IH}	High-level input voltage	1 thru 3		2			V
V_{IL}	Low-level input voltage	2 thru 4				0.7	V
V_{OH}	High-level output voltage	1 and 2	V_{CC} = MIN, I_{OH} = −100 μA	2.4			V
V_{OL}	Low-level output voltage	3 and 4	V_{CC} = MIN, I_{OL} = 2 mA			0.3	V
I_{IH}	High-level input current into any input except M or A	5	V_{CC} = MAX, V_I = 2.4 V			10	μA
			V_{CC} = MAX, V_I = 5.5 V			100	
I_{IH}	High-level input current into M or A	5	V_{CC} = MAX, V_I = 2.4 V			20	μA
			V_{CC} = MAX, V_I = 5.5 V			200	
I_{IL}	Low-level input current into any input except M or A	6	V_{CC} = MAX, V_I = 0.3 V			−0.18	mA
I_{IL}	Low-level input current into M or A	6	V_{CC} = MAX, V_I = 0.3 V			−0.36	mA
I_{OS}	Short-circuit output current¶	7	V_{CC} = MAX	−3		−15	mA
I_{CC}	Supply current	8	V_{CC} = MAX		3.8	9	mA

‡For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

§This typical value is at V_{CC} = 5 V, T_A = 25°C.

¶Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	10	C_L = 50 pF, R_L = 4 kΩ	3	5		MHz
t_{PLH}	Propagation delay time, low-to-high-level output, from clock 1 or clock 2				115	200	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from clock 1 or clock 2				125	200	ns

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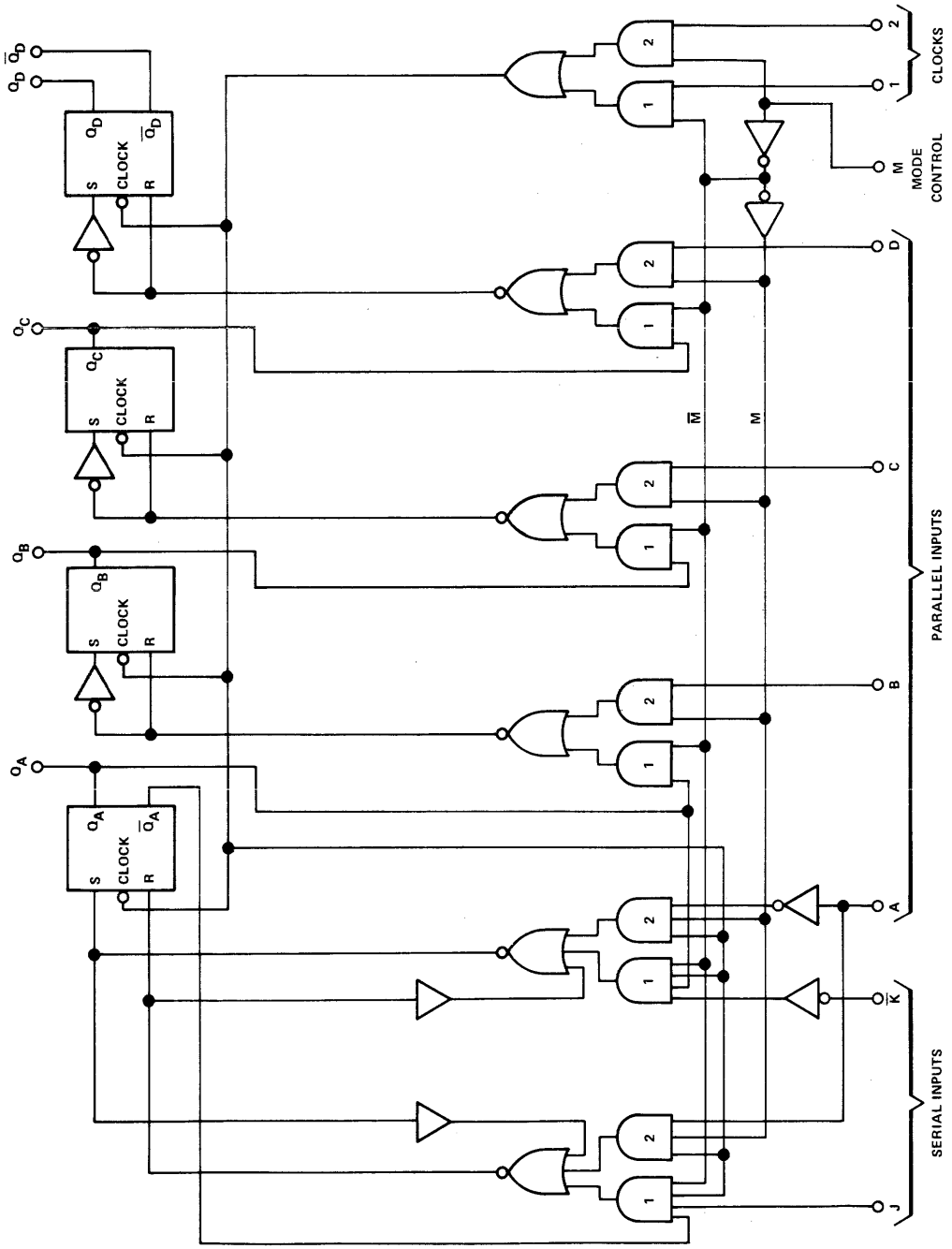
functional block diagram



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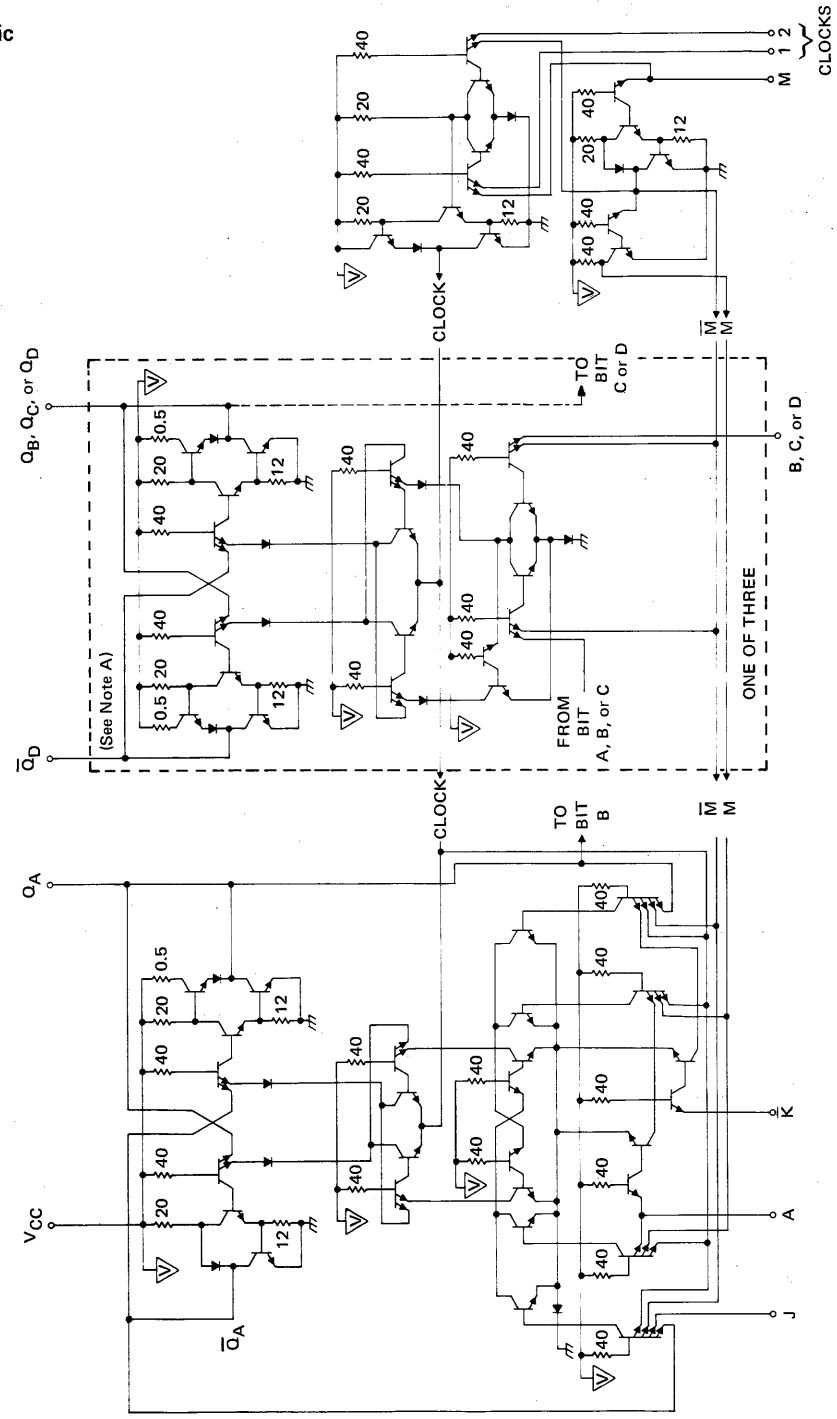
schematic

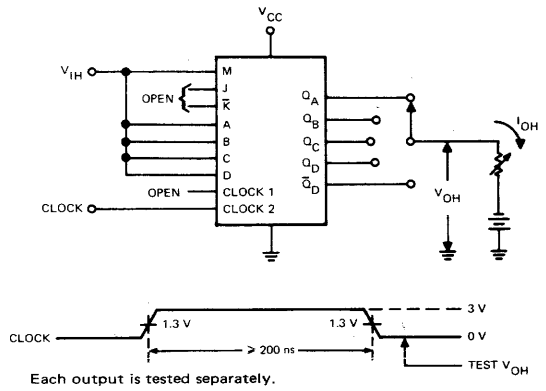


NOTES: A. Internal outputs $\bar{Q}_B$ and $\bar{Q}_C$ are as shown for $\bar{Q}_A$; i.e., they are not of the active-pullup type.
B. Resistor values shown are nominal in kilohms.
▽ ... V_{CC} bus

9

PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



Each output is tested separately.

FIGURE 1–V_{IH}, V_{OH}

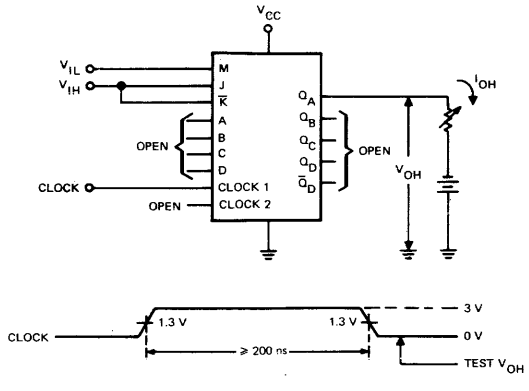
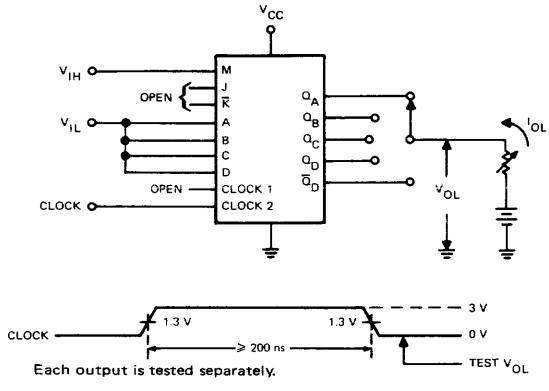


FIGURE 2–V_{IH}, V_{IL}, V_{OH}



Each output is tested separately.

FIGURE 3–V_{IH}, V_{IL}, V_{OL}

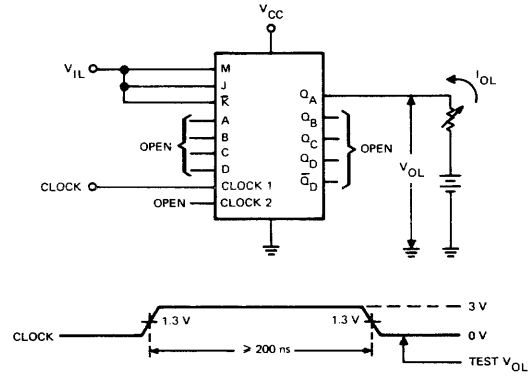
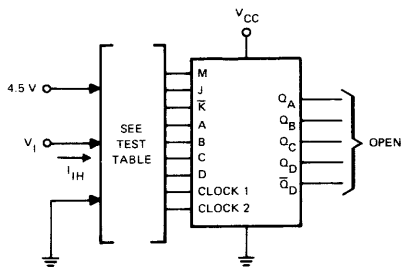


FIGURE 4–V_{IL}, V_{OL}



Each input is tested separately.

TEST TABLE

APPLY V_I	APPLY 4.5 V	APPLY GND
M	NONE	CLOCK 2
J	M and A	CLOCK 2 (Note)
$\overline{K}$	NONE	NONE
INPUT A	NONE	M and CLOCK 1
INPUTS B, C, or D	NONE	M
CLOCK 1	M	NONE
CLOCK 2	NONE	M

NOTE: Apply momentary high, then ground.

FIGURE 5–I_{IH}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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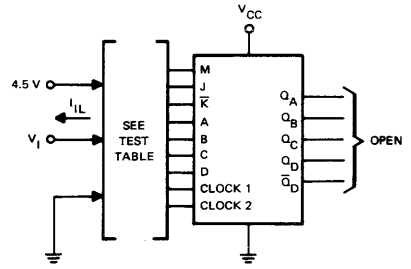
PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

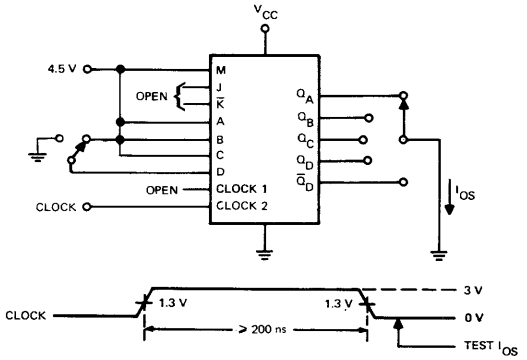


Each input is tested separately.

TEST TABLE

APPLY V_I	APPLY 4.5 V	APPLY GND
M	CLOCK 2	NONE
J	CLOCK 1	Q_A and M
$\overline{K}$	NONE	NONE
INPUT A	M and CLOCK 2	NONE
INPUTS B, C, or D	M	NONE
CLOCK 1	NONE	M
CLOCK 2	M	NONE

FIGURE 6–I_{IL}



NOTES: A. Each output is tested separately.
B. When testing Q_D or $\overline{Q}_D$, input D is connected to 4.5 V or ground, respectively.

FIGURE 7–I_{OS}

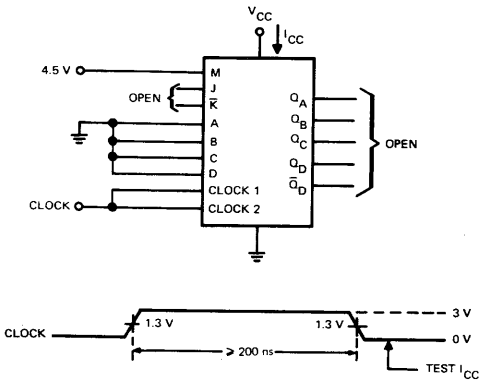
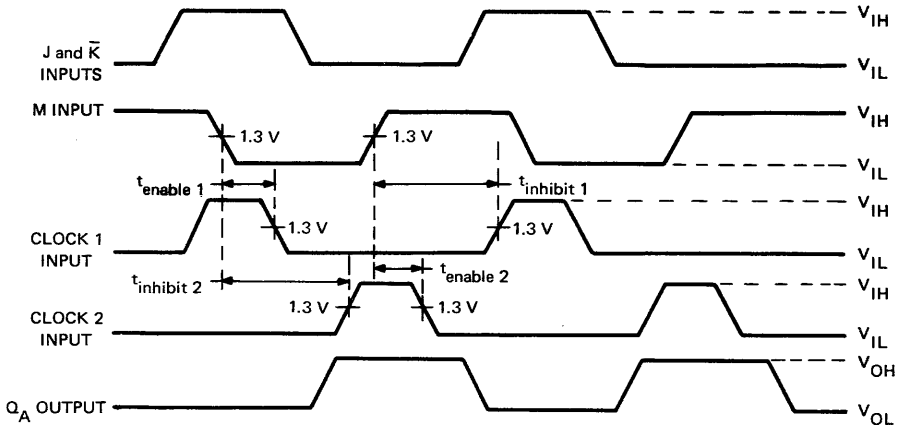


FIGURE 8–I_{CC}

recommended clock enable/input times



NOTE: A input is at the low level.

VOLTAGE WAVEFORMS

FIGURE 9–CLOCK ENABLE/INHIBIT TIMES

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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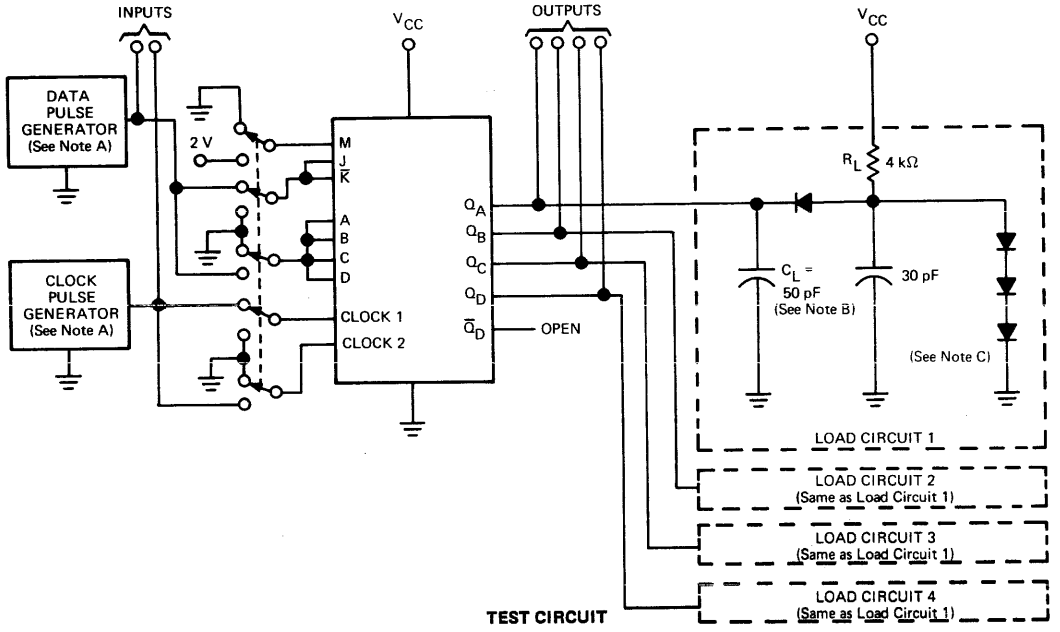
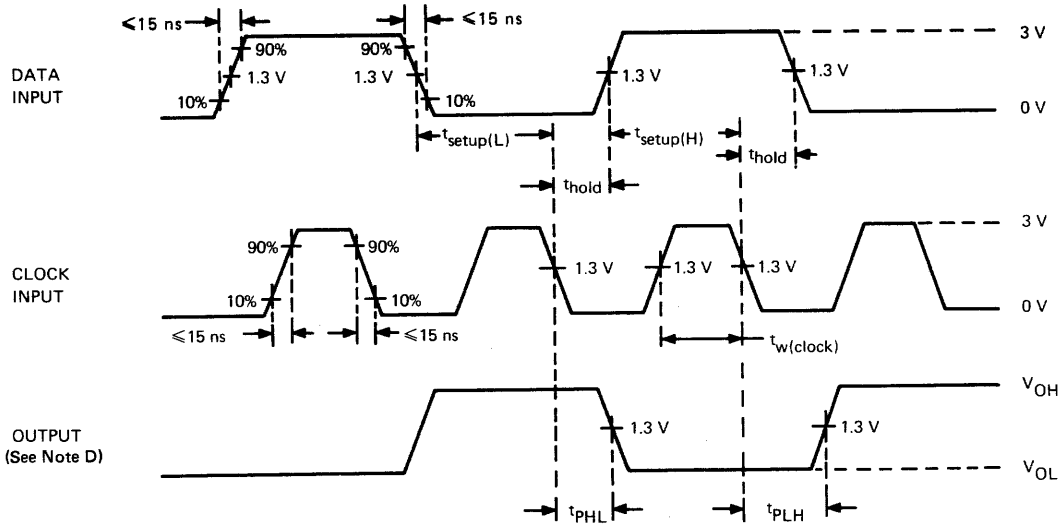
PARAMETER MEASUREMENT INFORMATION

switching characteristics





VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: $Z_{out} \approx 50\ \Omega$. For data pulse generator: $t_w \geq 150$ ns, PRR ≤ 500 kHz, $t_{setup(L)} = 120$ ns, and $t_{setup(H)} = 100$ ns. For clock pulse generator: $t_w \geq 200$ ns and PRR ≤ 1 MHz. When testing f_{max}, vary PRR.

B. C_L includes probe and jig capacitance.

C. All diodes are 1N916.

D. When data input is applied to J and $\overline{K}$ inputs, the output waveform applies only to output Q_A.

FIGURE 10–SWITCHING TIMES

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FUNCTION TABLES

BIT TIME	OPERATION AT NEXT BIT TIME	MODE CONTROL M	PARALLEL INPUTS A	B	C	D	SERIAL INPUTS J	$\overline{K}$	OUTPUTS Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
TABLE 1–PARALLEL LOADING													
n	Parallel load	H	A_n	B_n	C_n	D_n	X	X	X	X	X	X	X
n+1	Parallel load	H	A_{n+1}	B_{n+1}	C_{n+1}	D_{n+1}	X	X	A_n	B_n	C_n	D_n	$\overline{D}_n$
n+2	Parallel load	H	H	H	L	H	X	X	A_{n+1}	B_{n+1}	C_{n+1}	D_{n+1}	$\overline{D}_{n+1}$
n+3	Determined by M	X	X	X	X	X	X	X	H	H	L	H	L
TABLE 2–J-$\overline{K}$ SERIAL LOADING AND RIGHT SHIFT													
n	S.R., hold Q_A	L	X	X	X	X	L	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	$\overline{Q}_{Dn}$
n+1	S.R., set Q_A lo	L	X	X	X	X	L	L	Q_{An}	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
n+2	S.R., set Q_A hi	L	X	X	X	X	H	H	L	Q_{An}	Q_{An}	Q_{Bn}	$\overline{Q}_{Bn}$
n+3	S.R., set Q_A hi	L	X	X	X	X	H	H	H	L	Q_{An}	Q_{An}	$\overline{Q}_{An}$
n+4	S.R., set Q_A lo	L	X	X	X	X	L	L	H	H	L	Q_{An}	$\overline{Q}_{An}$
n+5	S.R., set Q_A lo	L	X	X	X	X	L	L	L	H	H	L	H
n+6	S.R., toggle Q_A	L	X	X	X	X	H	L	L	L	H	H	L
n+7	S.R., toggle Q_A	L	X	X	X	X	H	L	H	L	L	H	L
n+8	Determined by M	X	X	X	X	X	X	X	L	H	L	L	H
TABLE 3–SERIAL LOADING WITH D INPUT AND LEFT SHIFT (See Figure 11)													
n	S.L., set Q_D to D_n	H	Q_{Bn}	Q_{Cn}	Q_{Dn}	D_n	X	X	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	$\overline{Q}_{Dn}$
n+1	S.L., set Q_D lo	H	Q_{Cn}	Q_{Dn}	D_n	L	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	D_n	$\overline{D}_n$
n+2	S.L., set Q_D hi	H	Q_{Dn}	D_n	L	H	X	X	Q_{Cn}	Q_{Dn}	D_n	L	H
n+3	S.L., set Q_D hi	H	D_n	L	H	H	X	X	Q_{Dn}	D_n	L	H	L
n+4	S.L., set Q_D lo	H	L	H	H	L	X	X	D_n	L	H	H	L
n+5	Determined by M	X	X	X	X	X	X	X	L	H	H	L	H

H = high level, L = low level, X = irrelevant
A_n = state of input A at bit time n
S.R. = shift right, S.L. = shift left
Q_{An} = state of output Q_A at bit time n

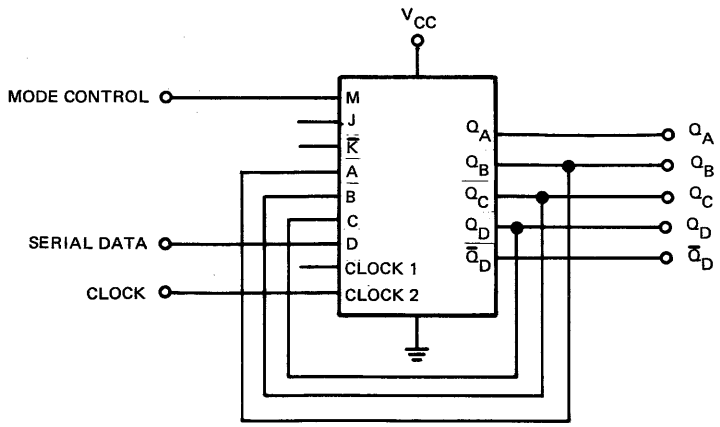

FIGURE 11–CONNECTIONS FOR LEFT SHIFT

9

TEXAS INSTRUMENTS
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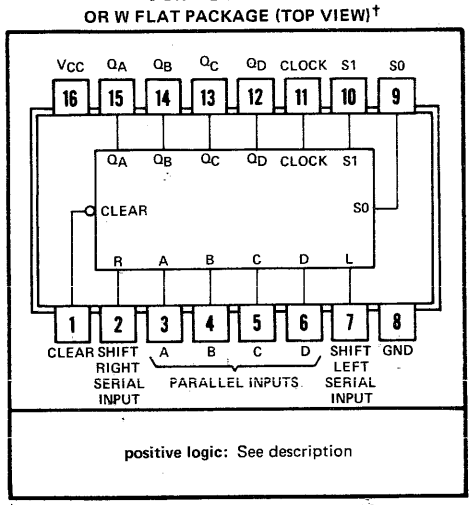
CIRCUIT TYPES SN54194, SN74194
4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

- Parallel Inputs and Outputs
- Four Operating Modes:
  - Synchronous Parallel Load
  - Left Shift
  - Right Shift
  - Do Nothing
- Positive Edge-Triggered Clocking
- Direct Overriding Clear

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



†Pin assignments for these circuits are the same for all packages.

description

These bidirectional shift registers are designed to incorporate virtually all of the features a system designer may want in a shift register. The circuit contains 46 equivalent gates and features parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

	MODE CONTROL	
	S1	S0
Parallel (Broadside) Load	H	H
Shift Right (In the direction Q_A toward Q_D)	L	H
Shift Left (In the direction Q_D toward Q_A)	H	L
Inhibit Clock (Do nothing)	L	L

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In the parallel-load mode, data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited. Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial input. Clocking of the flip-flops is inhibited when both mode-control inputs are low. The mode controls should be changed only while the clock input is high.

These four-bit shift registers are compatible with most other TTL and DTL logic families. All inputs are buffered to lower the drive requirements to one normalized Series 54/74 load, and input clamping diodes minimize switching transients to simplify system design. Maximum input clock frequency is typically 36 megahertz and power dissipation is typically 195 mW.

The SN54194 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74194 is characterized for operation from 0°C to 70°C.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: SN54194 Circuits . . . . . −55°C to 125°C
SN74194 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54194			SN74194			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Input clock frequency, f_{clock}		0		25	0		25	MHz
Width of clock or clear pulse, t_w		20			20			ns
Setup time, t_{setup} (see Figure 1)	Mode control	30			30			ns
	Serial and parallel data	20			20			ns
	Clear inactive-state	25			25			ns
Hold time at any input, t_{hold}		0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA				0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	SN54194	−20		−57	mA
			SN74194	−18		−57	
I_{CC}	Supply current	V_{CC} = MAX, See Note 2			39	63	mA

NOTE 2: With all outputs open, inputs A through D grounded, and 4.5 V applied to S0, S1, clear, and the serial inputs, I_{CC} is tested with a momentary ground, then 4.5 V, applied to clock.

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time.

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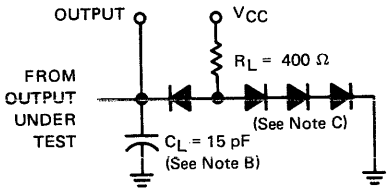
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum input clock frequency	C_L = 15 pF, R_L = 400 Ω, See Figure 1	25	36		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear			19	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock		7	14	22	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock		7	17	26	

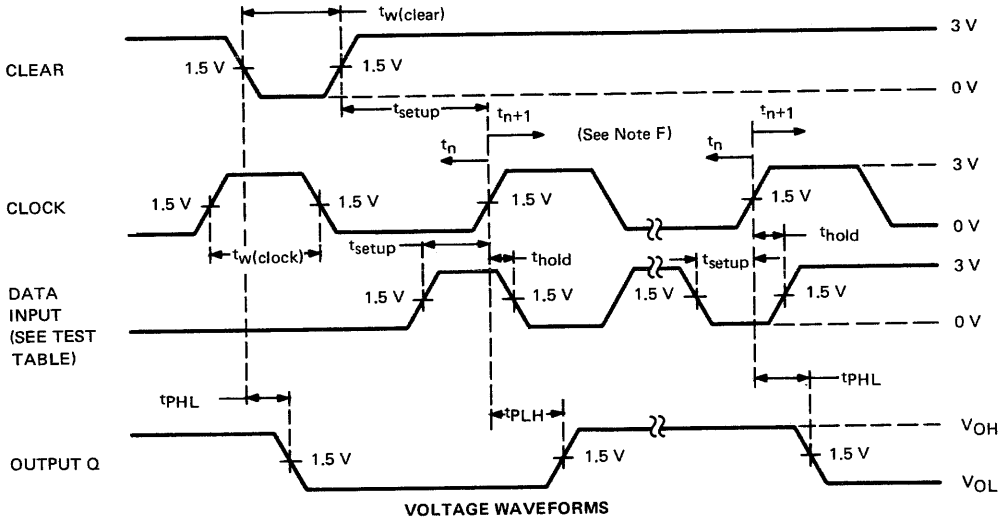
PARAMETER MEASUREMENT INFORMATION



LOAD FOR OUTPUT UNDER TEST

TEST TABLE FOR SYNCHRONOUS INPUTS

DATA INPUT FOR TEST	S1	S0	OUTPUT TESTED (SEE NOTE E)
A	4.5 V	4.5 V	Q_A at t_{n+1}
B	4.5 V	4.5 V	Q_B at t_{n+1}
C	4.5 V	4.5 V	Q_C at t_{n+1}
D	4.5 V	4.5 V	Q_D at t_{n+1}
L Serial Input	4.5 V	0 V	Q_A at t_{n+4}
R Serial Input	0 V	4.5 V	Q_D at t_{n+4}



VOLTAGE WAVEFORMS

NOTES A. The clock pulse has the following characteristics: $t_{w(clock)} \geq 20$ ns and PRR = 1 MHz. The clear pulse has the following characteristics: $t_{w(clear)} \geq 20$ ns and t_{hold} = 0 ns. When testing f_{max}, vary the clock PRR.

B. C_L includes probe and jig capacitance.

C. All diodes are 1N3064.

D. A clear pulse is applied prior to each test.

E. Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_{n+1}. Proper shifting of data is verified at t_{n+4} with a functional test.

F. t_n = bit time before clocking transition.
t_{n+1} = bit time after one clocking transition.
t_{n+4} = bit time after four clocking transitions.

FIGURE 1–SWITCHING TIMES

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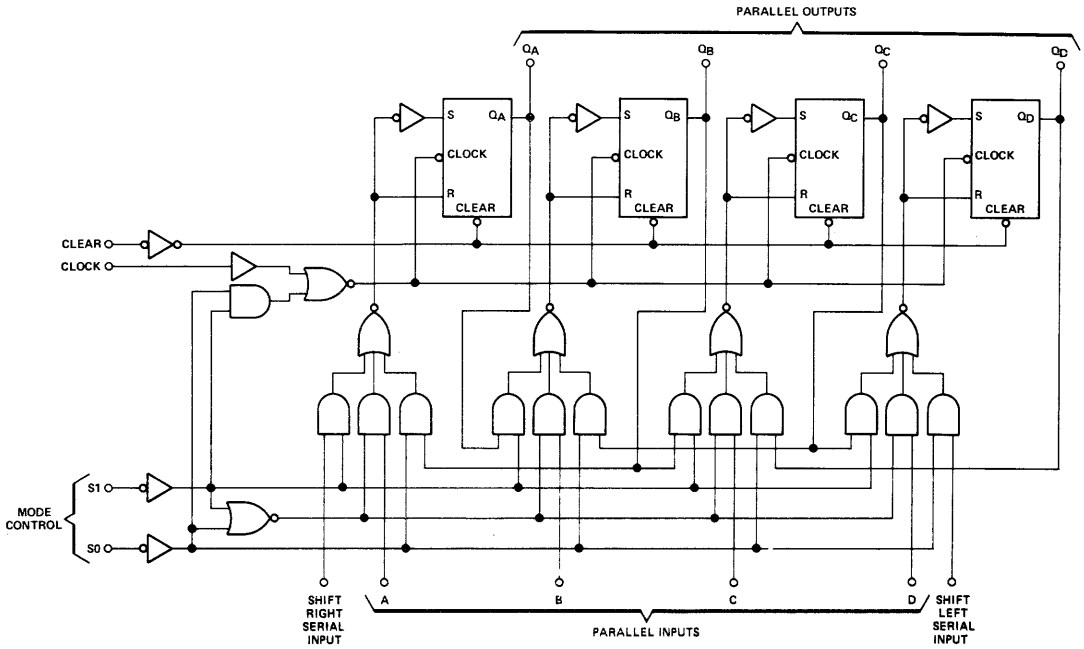
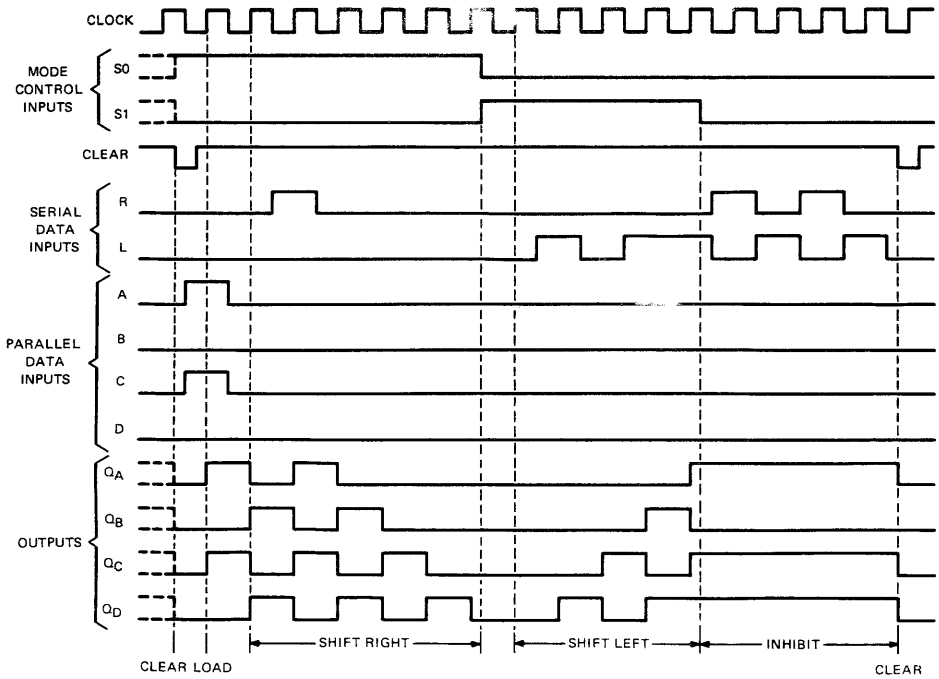
functional block diagram



typical clear, load, right-shift, left-shift, inhibit, and clear sequences



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TEXAS INSTRUMENTS
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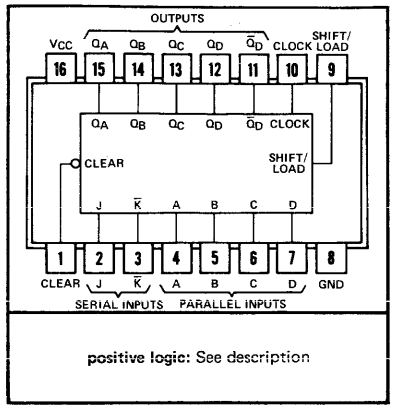
CIRCUIT TYPES SN54195, SN74195
4-BIT PARALLEL-ACCESS SHIFT REGISTERS

- Synchronous Parallel Load
- Positive Edge-Triggered Clocking
- Parallel Inputs and Outputs from Each Flip-Flop
- Direct Overriding Clear
- J and $\overline{K}$ Inputs to First Stage
- Complementary Outputs from Last Stage

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



†Pin assignments for these circuits are the same for all packages.

description

These 4-bit registers feature parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, shift/load control input, and a direct overriding clear. The registers have two modes of operation:

Parallel (Broadside) Load

Shift (In direction Q_A toward Q_D)

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-$\overline{K}$ inputs. These inputs permit the first stage to perform as a J-$\overline{K}$, D-, or T-type flip-flop as shown in the truth table.

9

These shift registers are fully compatible with most other TTL and DTL families. All inputs are buffered to lower the drive requirements to one normalized Series 54/74 load, including the clock input. Maximum input clock frequency is typically 39 megahertz and power dissipation is typically 195 milliwatts. The SN54195 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74195 is characterized for operation from 0°C to 70°C.

TRUTH TABLE

Inputs at t_n		Outputs at t_{n+1}				
J	$\overline{K}$	Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
L	H	Q_{An}	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
L	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	L	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

H = high level, L = low level

NOTES: A. t_n = bit time before clock pulse
B. t_{n+1} = bit time after clock pulse
C. Q_{An} = state of Q_A at t_n

TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: SN54195 Circuits . . . . . −55°C to 125°C
SN74195 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54195			SN74195			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Input clock frequency, f_{clock}		0		30	0		30	MHz
Width of clock input pulse, $t_{w(clock)}$		16			16			ns
Width of clear input pulse, $t_{w(clear)}$		12			12			ns
Setup time, t_{setup} (see Figure 1)	Shift/load	25			25			ns
	Serial and parallel data	15			15			
	Clear inactive-state	25			25			
Shift/load release time, $t_{release}$ (see Figure 1)				10			10	ns
Serial and parallel data hold time, t_{hold} (see Figure 1)		0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA				0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	SN54195	−20		−57	mA
			SN74195	−18		−57	
I_{CC}	Supply current	V_{CC} = MAX, See Note 2			39	63	mA

NOTE 2: With all outputs open, shift/load grounded, and 4.5 V applied to the J, $\overline{K}$, and data inputs, I_{CC} is measured by applying a momentary ground, followed by 4.5 V, to clear, and then applying a momentary ground, followed by 4.5 V, to clock.

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

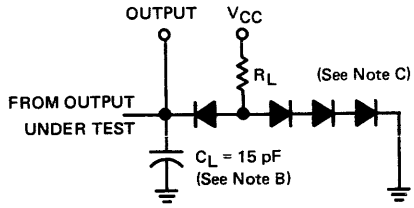
§Not more than one output should be shorted at a time.

9

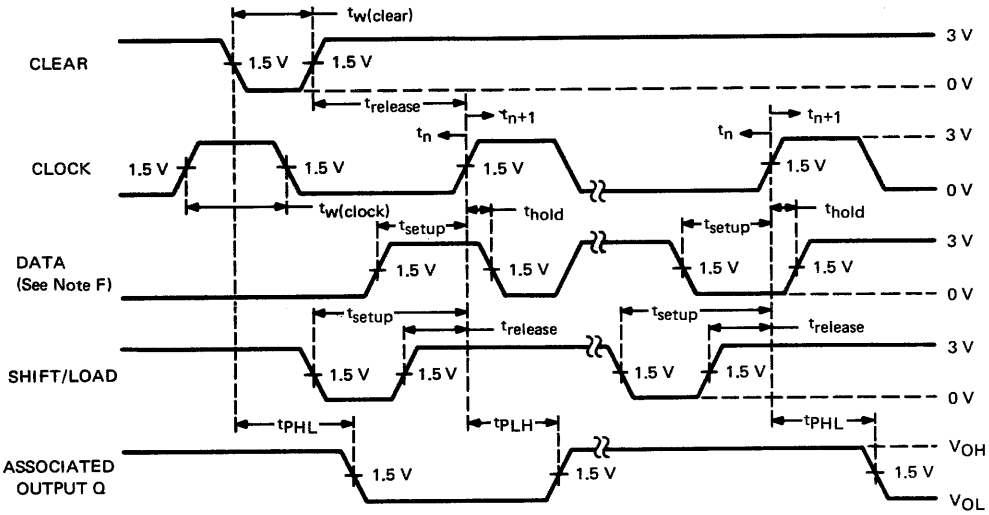
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum input clock frequency	C_L = 15 pF, R_L = 400 Ω, See Figure 1	30	39		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear			19	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock		6	14	22	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock		7	17	26	ns

PARAMETER MEASUREMENT INFORMATION



LOAD FOR OUTPUT UNDER TEST



VOLTAGE WAVEFORMS

NOTES: A. The clock pulse has the following characteristics: $t_{w(clock)} \geq$ 16 ns and PRR = 1 MHz. The clear pulse has the following characteristics: $t_{w(clear)} \geq$ 12 ns and t_{hold} = 0 ns. When testing f_{max}, vary the clock PRR.
B. C_L inlcudes probe and jig capacitance.
C. All diodes are 1N3064.
D. A clear pulse is applied prior to each test.
E. Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_{n+1}. Proper shifting of data is verified at t_{n+4} with a functional test.
F. J and $\overline{K}$ inputs are tested the same as data A, B, C, and D inputs except that shift/load input remains high.
G. t_n = bit time before clocking transition.
t_{n+1} = bit time after one clocking transition.
t_{n+4} = bit time after four clocking transitions.

FIGURE 1–SWITCHING TIMES

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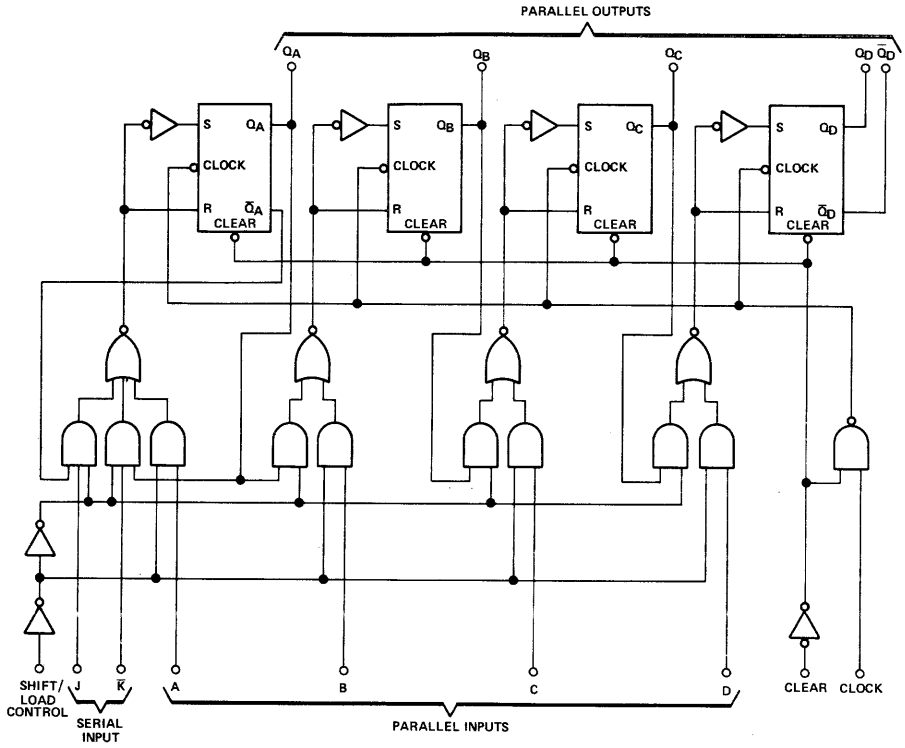
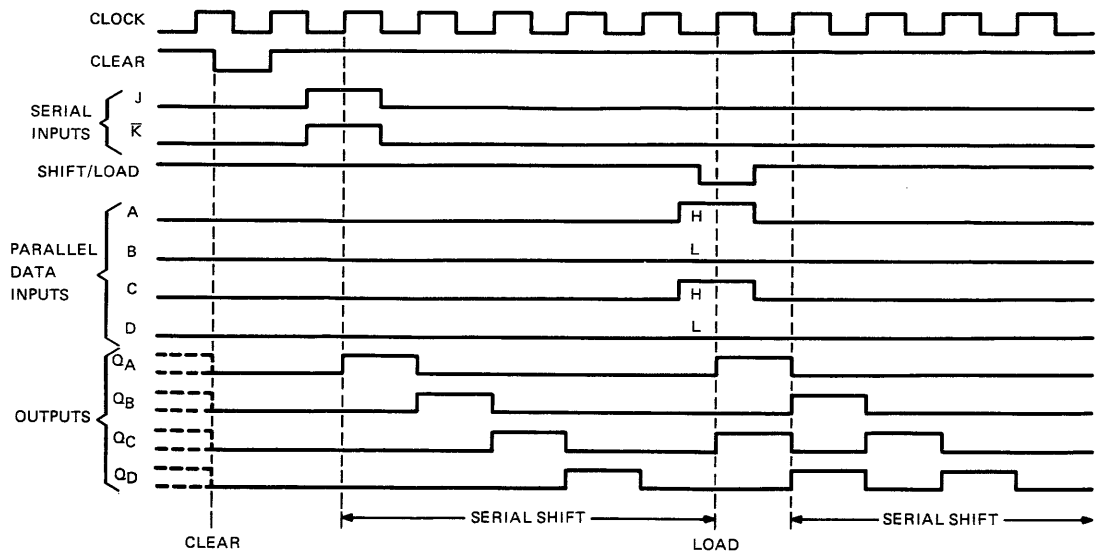
functional block diagram



typical clear, shift, and load sequences



9

CIRCUIT TYPES SN5491A, SN7491A
8-BIT SHIFT REGISTERS

MSI TTL SHIFT REGISTERS
for applications in

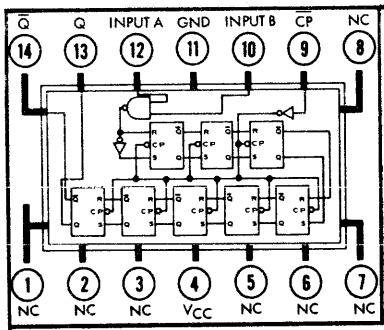
- Digital Computer Systems
- Data-Handling Systems
- Control Systems

logic

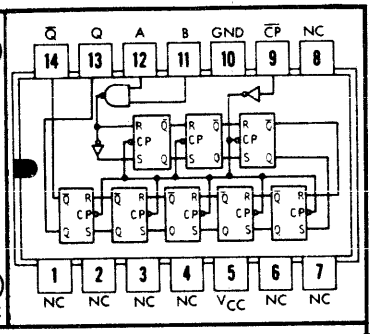
t_n		t_{n+8}
A	B	Q
0	0	0
0	1	0
1	0	0
1	1	1

NOTES:
1. t_n = bit time before clock.
2. t_{n+8} = bit time after 8 clock pulses.

W
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: See Truth Table

NC—No Internal Connection

description

These monolithic serial-in, serial-out, 8-bit shift registers utilizing transistor-transistor logic (TTL) circuits, are composed of eight R-S master-slave flip-flops, input gating, and a clock driver. The register is capable of storing and transferring data at clock rates up to 18 MHz while maintaining a typical noise-immunity level of 1 volt. Power dissipation is typically 175 milliwatts, and a full fan-out of 10 is available from the outputs.

Single-rail data and input control are gated through inputs A and B and an internal inverter to form the complementary inputs to the first bit of the shift register. Drive for the internal common clock line is provided by an inverting clock driver. Each of the inputs (A, B, and $\overline{CP}$) appear as only one TTL input load.

The clock pulse inverter/driver causes these circuits to shift information to the output on the positive edge of an input clock pulse, thus enabling the shift-register to be fully compatible with other edge-triggered synchronous functions.

9

absolute maximum ratings (over operating temperature range unless otherwise noted)

Supply Voltage V_{CC} (See Note 3) . . . . . 7 V
Input Voltage, V_{in} (See Notes 3 and 4) . . . . . 5.5 V
Operating Free-Air Temperature Range: SN5491A Circuits . . . . . −55°C to 125°C
SN7491A Circuits . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

NOTES: 3. These voltage values are with respect to network ground terminal.
4. Input signals must be zero or positive with respect to network ground terminal.

recommended operating conditions (over operating temperature range)

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 3): SN5491A Circuits	4.5	5	5.5	V
SN7491A Circuits	4.75	5	5.25	V
Normalized Fan-Out From Outputs			10	
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 7)	25			ns
Input Setup Time, t_{setup} (See Figure 7)	25			ns
Input Hold Time, t_{hold} (See Figure 7)	0			

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electrical characteristics over operating temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	2					0.8	V
$V_{out(1)}$	Logical 1 output voltage	1	V_{CC} = MIN, I_{load} = −400 μA		2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	2	V_{CC} = MIN, I_{sink} = 16 mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current	3	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(1)}$	Logical 1 level input current	4	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current§	5	V_{CC} = MAX, V_{out} = 0	SN5491A	−20		−57	mA
				SN7491A	−18		−57	mA
I_{CC}	Supply current	6	V_{CC} = MAX, V_{in} = 4.5 V	SN5491A		35	50	mA
				SN7491A		35	58	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum shift frequency		C_L = 15 pF, R_L = 400 Ω	10	18		MHz
t_{pd1}	Propagation delay time to logical 1 level from clock to output	7	C_L = 15 pF, R_L = 400 Ω		24	40	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	7	C_L = 15 pF, R_L = 400 Ω		27	40	ns

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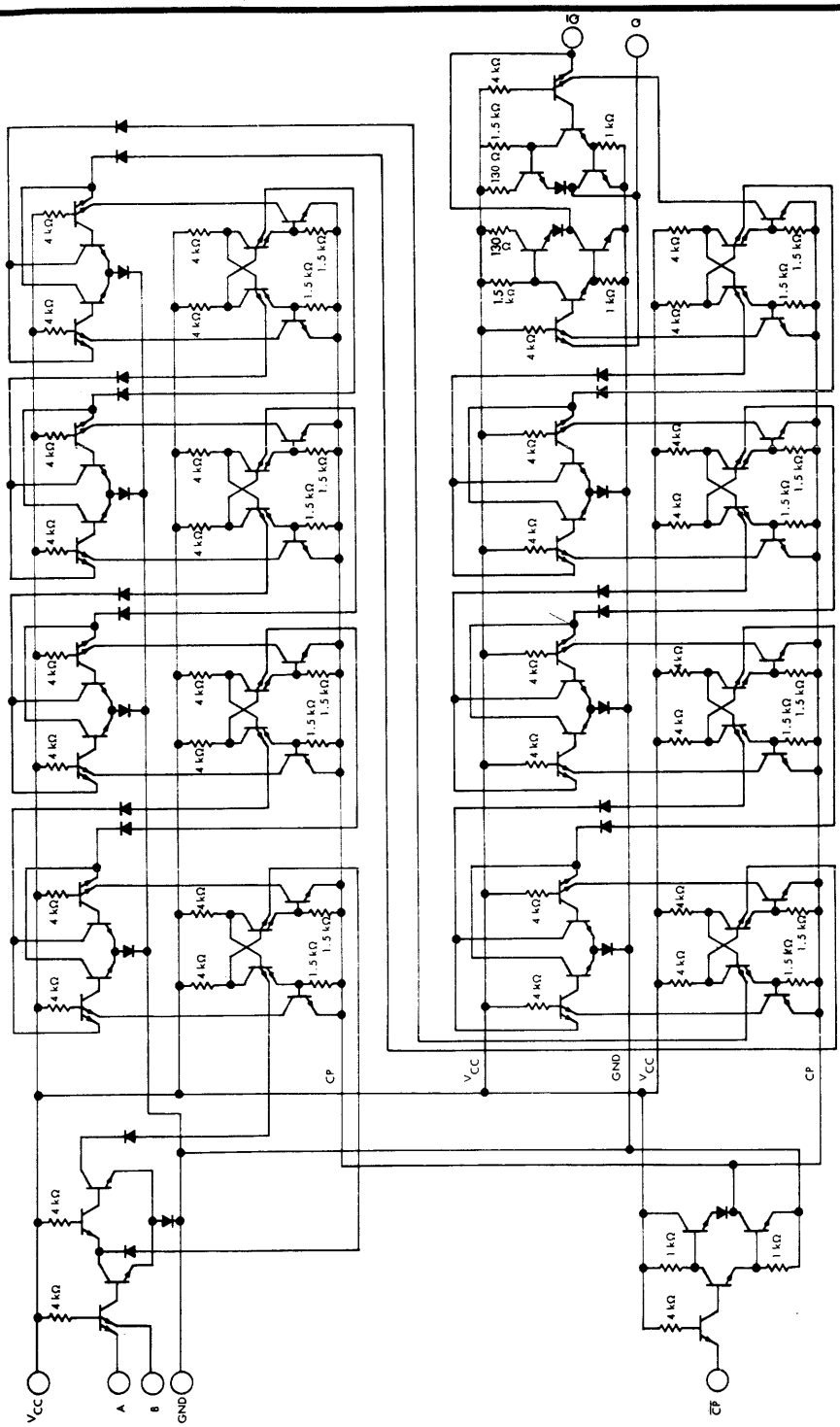
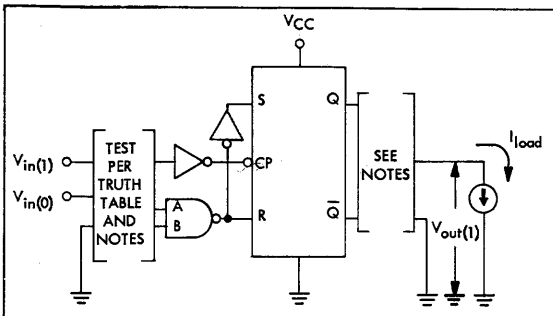
schematic



Component values shown are nominal.

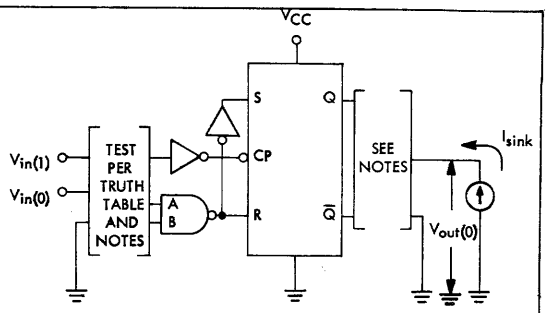
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



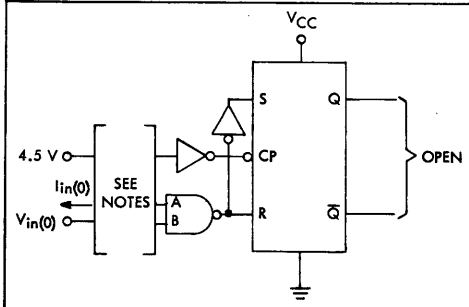
1. Each output is tested separately.
2. When testing $V_{out(1)}$ and I_{load}, ground all inputs and the unused output, then measure parameters specified.

FIGURE 1



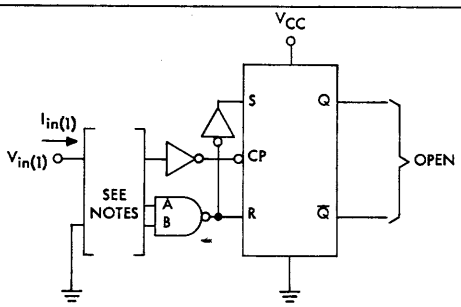
1. Each output is tested separately.
2. When testing $V_{out(0)}$ and I_{sink}, ground all inputs. Apply a momentary ground to the output to be tested then measure parameters specified.

FIGURE 2



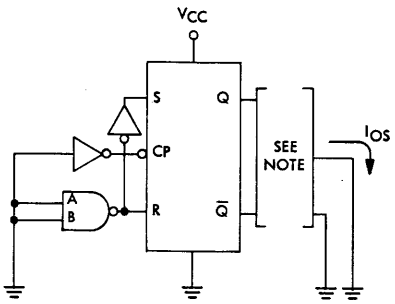
1. When testing input A apply 4.5 V to input B.
2. When testing input B apply 4.5 V to input A.

FIGURE 3



1. When testing input A ground input B.
2. When testing input B ground input A.

FIGURE 4



1. Ground the unused output then measure parameter specified.

FIGURE 5

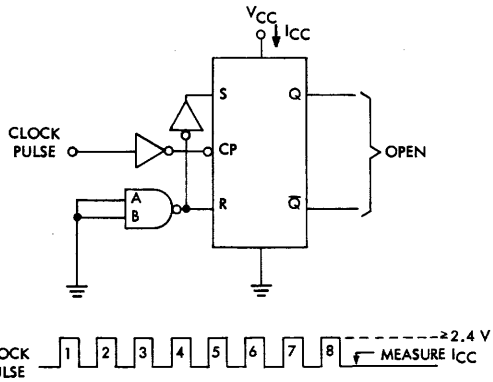


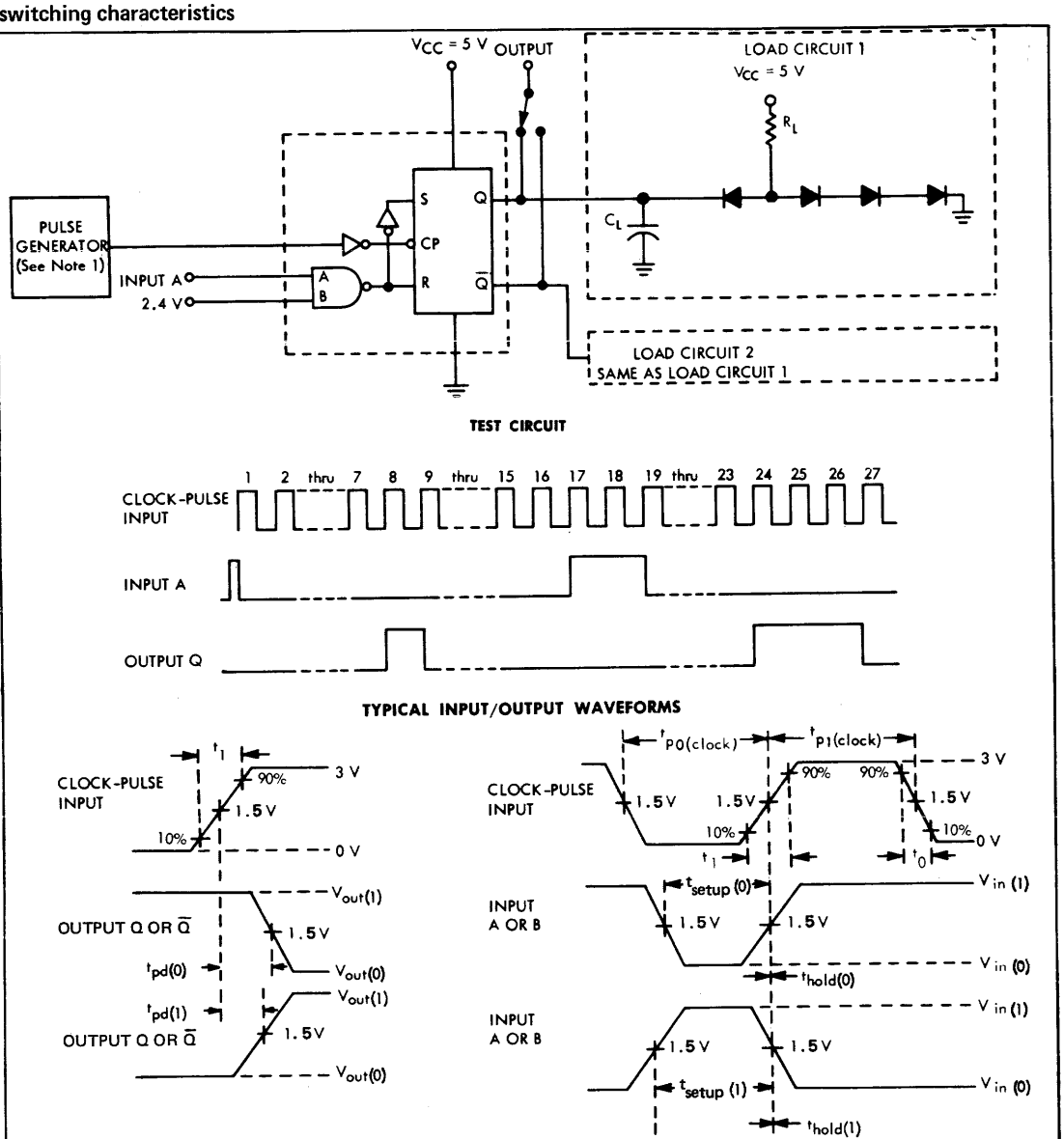
FIGURE 6

† Arrows indicate actual direction of current flow.

9

PARAMETER MEASUREMENT INFORMATION

switching characteristics



NOTES: 1. The generator has the following characteristics: $V_{in(0)} \leq 0.3$ V, $V_{in(1)} \geq 2.4$ V, $t_f = t_O = 10$ ns, $t_{P1(clock)} = 500$ ns, $t_{PO(clock)} = 500$ ns, PRR = 1 MHz, and $Z_{out} \approx 50\ \Omega$.
2. C_L includes probe and jig capacitance.
3. Each output is tested separately.
4. Voltage values are with respect to network ground terminal.
5. All diodes are 1N3064.

FIGURE 7 – SN5491A/SN7491A SWITCHING TIMES

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TEXAS INSTRUMENTS
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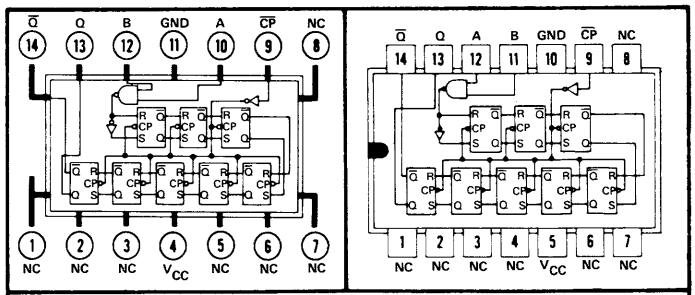
CIRCUIT TYPES SN54L91, SN74L91
8-BIT SHIFT REGISTERS

T
FLAT PACKAGE (TOP VIEW)

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



logic

TRUTH TABLE		
t_n		t_{n+8}
A	B	Q
0	0	0
0	1	0
1	0	0
1	1	1

NOTES:
1. t_n = Bit time before clock pulse.
2. t_{n+8} = Bit time after 8 clock pulses.
3. NC – No internal connection.

positive logic: see truth table

description

This monolithic serial-in, serial-out, 8-bit shift register utilizes low-power transistor-transistor logic (TTL) circuits. The shift register, composed of eight R-S master-slave flip-flops, includes input gating and a clock driver. The register is capable of storing and transferring data at typical clock rates of 6.5 MHz while maintaining a typical noise-immunity level of 0.9 volt. Power dissipation is typically 17.5 milliwatts, and full fan-out of 10 is available from the outputs.

Single-rail data and input control are gated through inputs A and B and an internal inverter to form the complementary inputs to the first bit of the shift register. Drive for the internal common clock line is provided by an inverting clock driver. Each of the inputs (A, B, and clock) appear as only one low-power TTL input load.

The clock pulse inverter/driver causes the register to shift information to the output on the positive edge of an input clock pulse, thus enabling the shift register to be fully compatible with edge-triggering flip-flops.

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recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54L91 Circuits	4.5	5	5.5	V
SN74L91 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Input Setup Time, t_{setup} (See Figure 7)	120			ns
Input Hold Time, t_{hold} (See Figure 7)	0			
Width of Logical 0 Level Clock Pulse, $t_{p0(clock)}$ (See Figure 7)	150			ns
Width of Logical 1 Level Clock Pulse, $t_{p1(clock)}$ (See Figure 7)	100			ns
Operating Free-Air Temperature Range, T_A: SN54L91 Circuits	–55	25	125	°C
SN74L91 Circuits	0	25	70	°C

absolute maximum ratings over recommended operating free-air temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1) . . . . . 8 V
Input Voltage, V_{in} (See Notes 1 and 2) . . . . . 5.5 V
Operating Free-Air Temperature Range: SN54L91 Circuits . . . . . −55°C to 125°C
SN74L91 Circuits . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

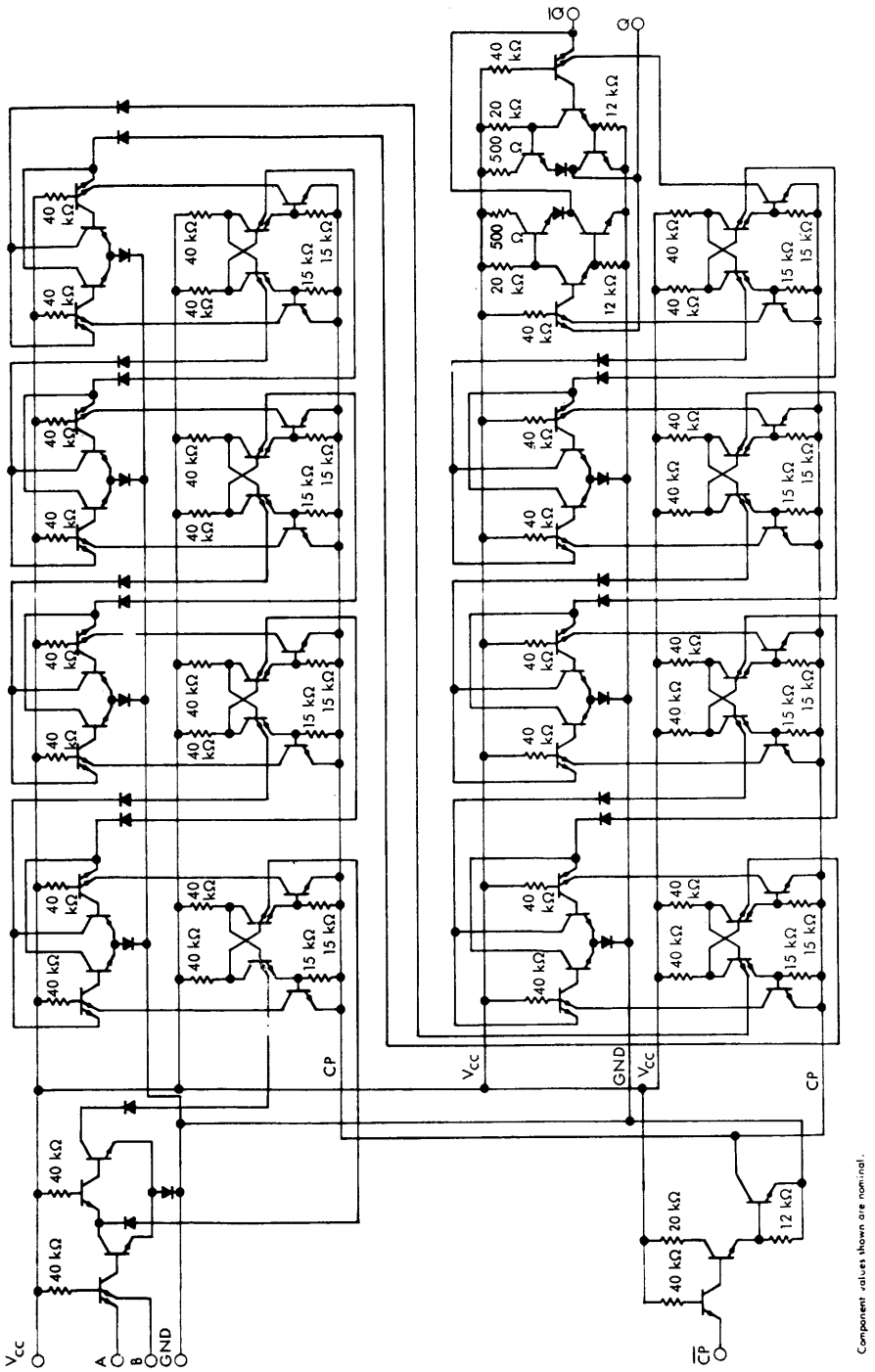
PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1		2		V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	2			0.7	V
$V_{out(1)}$	Logical 1 output voltage	1	V_{CC} = MIN, I_{load} = −100 μA	2.4		V
$V_{out(0)}$	Logical 0 output voltage	2	V_{CC} = MIN, I_{sink} = 2 mA		0.3	V
$I_{in(0)}$	Logical 0 level input current	3	V_{CC} = MAX, V_{in} = 0.3 V		-0.18	mA
$I_{in(1)}$	Logical 1 level input current	4	V_{CC} = MAX, V_{in} = 2.4 V		10	μA
			V_{CC} = MAX, V_{in} = 5.5 V		100	μA
I_{os}	Short-circuit output current	5	V_{CC} = MAX, V_{in} = 0, V_{out} = 0	−3	−15	mA
I_{CC}	Supply current	6	V_{CC} = MAX, V_{in} = 5 V		6.6	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{w0(clock)}$	Minimum width of logical 0 level clock pulse	7	C_L = 50 pF, R_L = 4 kΩ		105		ns
$t_{w1(clock)}$	Minimum width of logical 1 level clock pulse	7	C_L = 50 pF, R_L = 4 kΩ		45		ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	7	C_L = 50 pF, R_L = 4 kΩ		100	150	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	7	C_L = 50 pF, R_L = 4 kΩ		55	100	ns

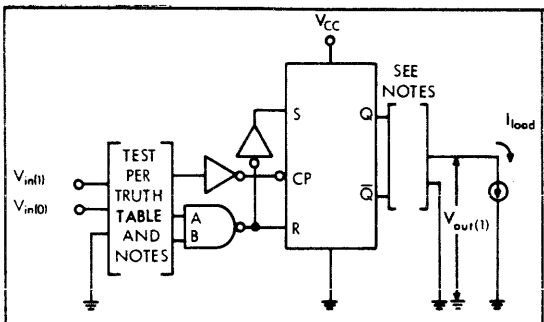
schematic


Vcc
A
B
GND
CP
Vcc
GND
Vcc
CP
1Q
Q
1CP
40 kΩ
20 kΩ
500 Ω
12 kΩ
15 kΩ
Component values shown are nominal.

9

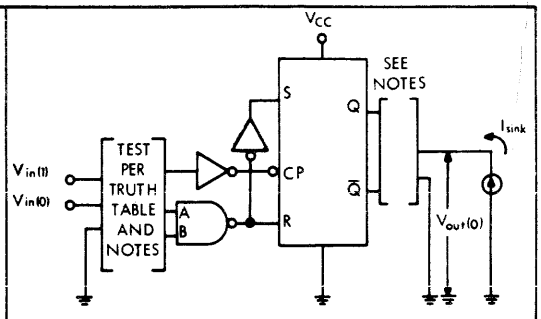
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§



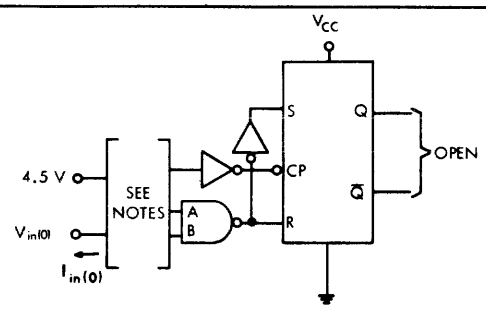
1. Each output is tested separately.
2. When testing $V_{out(1)}$ and I_{load}, ground all inputs and momentarily ground the unused output, then measure parameters specified.

FIGURE 1



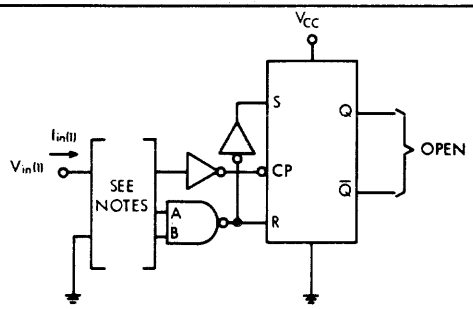
1. Each output is tested separately.
2. When testing $V_{out(0)}$ and I_{sink}, ground all inputs. Apply a momentary ground to the output to be tested, then measure parameters specified.

FIGURE 2



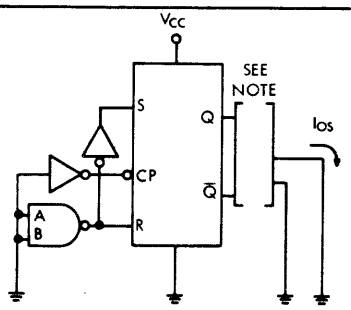
1. When testing input A apply 4.5 V to input B.
2. When testing input B apply 4.5 V to input A.

FIGURE 3



1. When testing input A ground input B.
2. When testing input B ground input A.

FIGURE 4



1. Ground the unused output, then measure parameters specified.

FIGURE 5

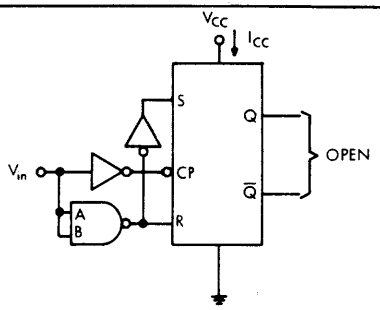
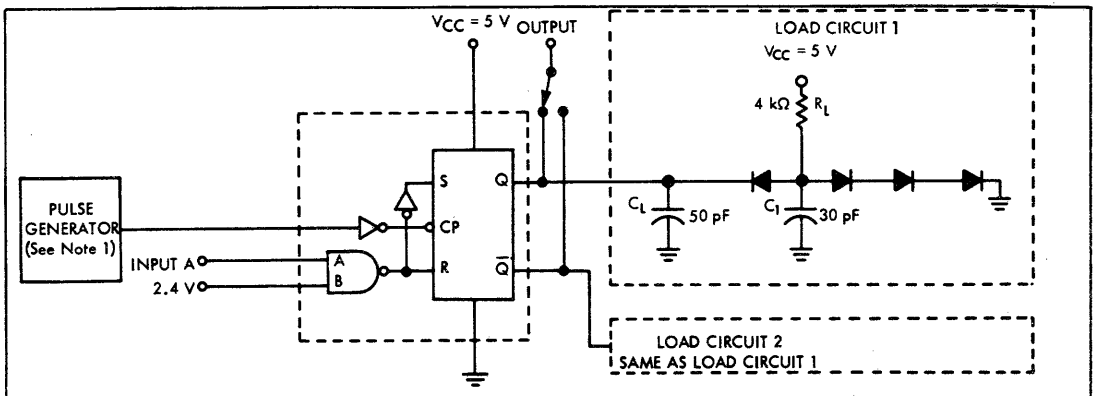


FIGURE 6

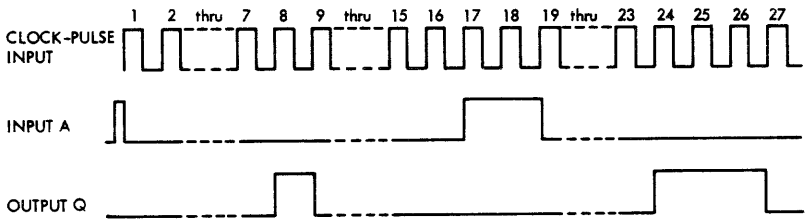
§Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

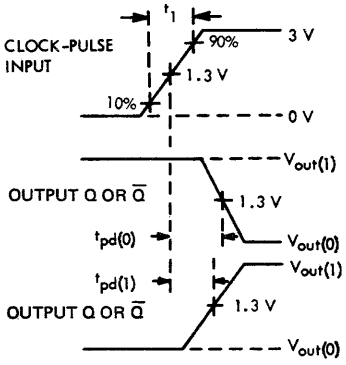
switching characteristics



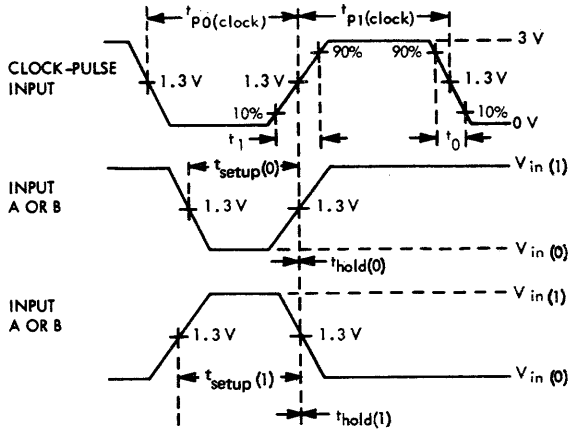
TEST CIRCUIT



TYPICAL INPUT/OUTPUT WAVEFORMS



PROPAGATION DELAY TIME VOLTAGE WAVEFORMS



SWITCHING TIME VOLTAGE WAVEFORMS

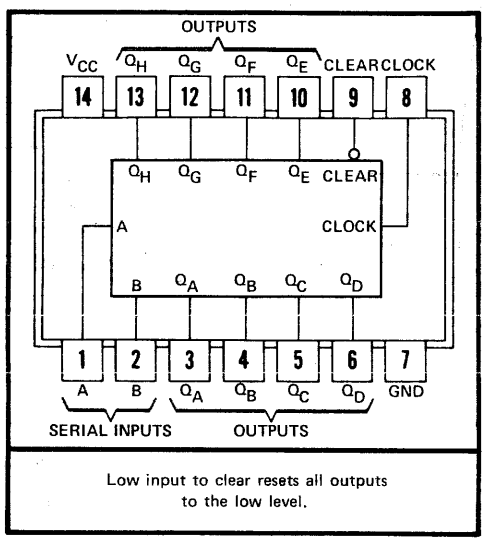
NOTES: 1. The generator has the following characteristics: $V_{in(0)} \leq 0.3$ V, $V_{in(1)} \geq 2.4$ V, $t_r = t_f = 15$ ns, $t_{p1(clock)} = 500$ ns, $t_{p0(clock)} = 500$ ns, PRR ≤ 1 MHz, and $Z_{out} \approx 50\ \Omega$.
2. C_L includes probe and jig capacitance.
3. Each output is tested separately.
4. Voltage values are with respect to network ground terminal.
5. All diodes are 1N916.

FIGURE 7 – SN54L91/SN74L91 SWITCHING TIMES

CIRCUIT TYPES SN54164, SN74164
8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

- Gated (Enable/Disable) Serial Inputs
- Fully Buffered Clock and Serial Inputs
- Asynchronous Clear
- Typical Maximum Input Clock Frequency . . . 36 MHz

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



†Pin assignments for these circuits are the same for all packages.

TRUTH TABLE
SERIAL INPUTS A AND B

INPUTS AT t_n		OUTPUT AT t_{n+1}
A	B	Q_A
H	H	H
L	H	L
H	L	L
L	L	L

description

These 8-bit shift registers feature gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data as a low at either (or both) input(s) inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high, but only information meeting the setup requirements will be entered. Clocking occurs on the low-to-high-level transition of the clock input.

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All inputs are diode-clamped to minimize transmission-line effects, and are buffered to represent only one Series 54/74 load which simplifies system design. Power dissipation is typically 21 milliwatts per bit. Maximum input clock frequency is typically 36 megahertz.

The SN54164 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74164 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: SN54164 Circuits . . . . . −55°C to 125°C
SN74164 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

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recommended operating conditions

		SN54164			SN74164			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			10			10	
	Low logic level			5			5	
Input clock frequency, f_{clock}		0		25	0		25	MHz
Width of clock or clear input pulse, t_w		20			20			ns
Data setup time, t_{setup} (see Figure 1)		15			15			ns
Data hold time, t_{hold} (see Figure 1)		0			0			ns
Operating free-air temperature, T_A		−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54164			SN74164			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MAX,	I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = −400 μA	2.4			2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 8 mA			0.4			0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−1.6			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−10		−27.5	−9		−27.5	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2	$V_{I(clock)}$ = 0.4 V		30			30		mA
			$V_{I(clock)}$ = 2.4 V		37	54		37	54	

NOTE 2: I_{CC} is measured with outputs open, serial inputs grounded, and a momentary ground, then 4.5 V, applied to clear.

†For conditions shown at MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than two outputs should be shorted at a time.

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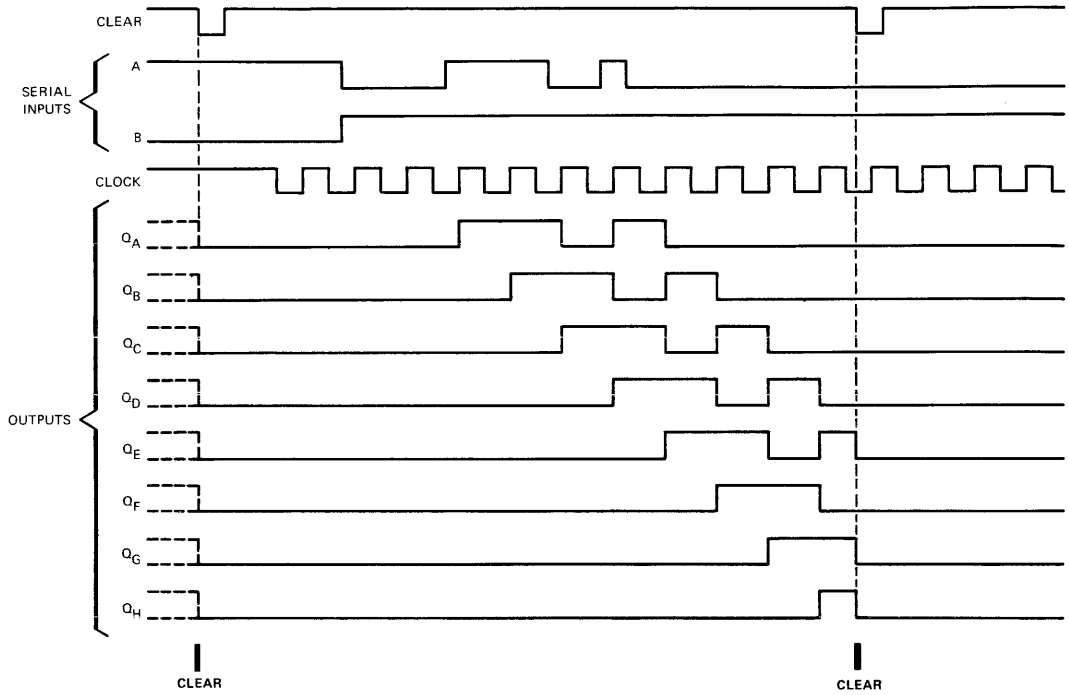
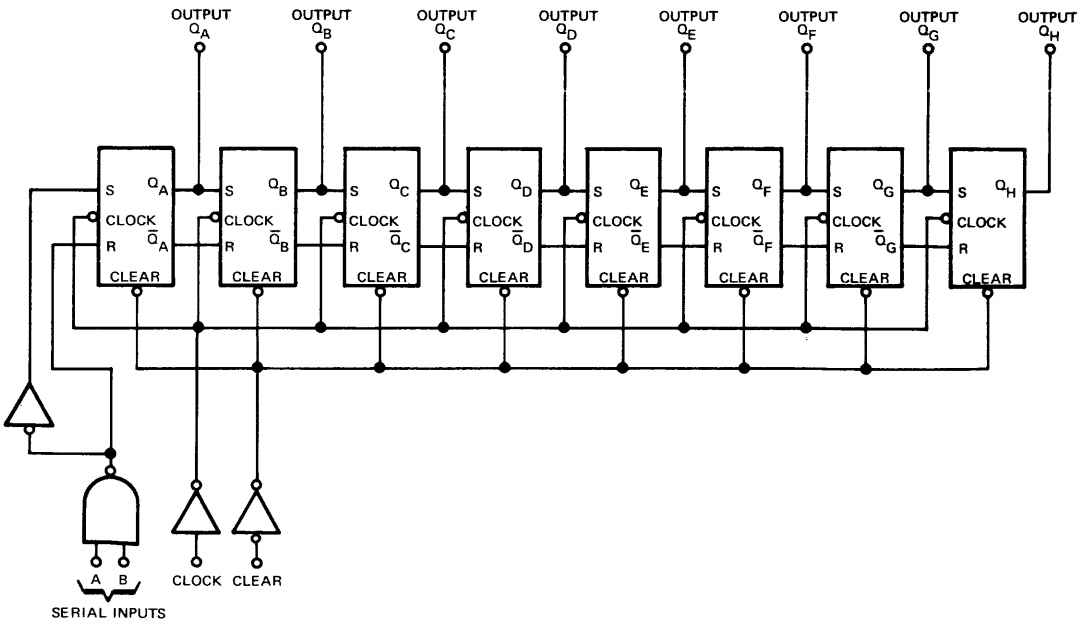
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 5

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Maximum input count frequency	R_L = 800 Ω, See Figure 1	C_L = 15 pF	25	36		MHz
t_{PHL}	Propagation delay time, high-to-low-level Q outputs from clear input		C_L = 15 pF		24	36	ns
			C_L = 50 pF		28	42	
t_{PLH}	Propagation delay time, low-to-high-level Q outputs from clock input		C_L = 15 pF	8	17	27	ns
			C_L = 50 pF	10	20	30	
t_{PHL}	Propagation delay time, high-to-low-level Q outputs from clock input		C_L = 15 pF	10	21	32	ns
			C_L = 50 pF	10	25	37	

typical clear, inhibit, shift, clear, and inhibit sequences



functional block diagram



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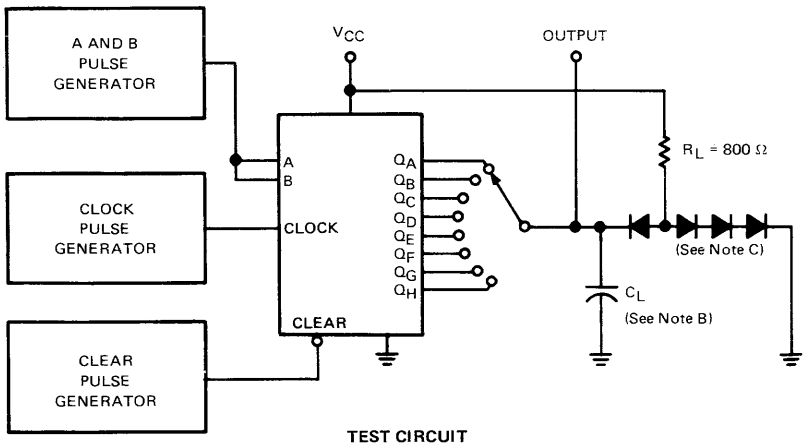
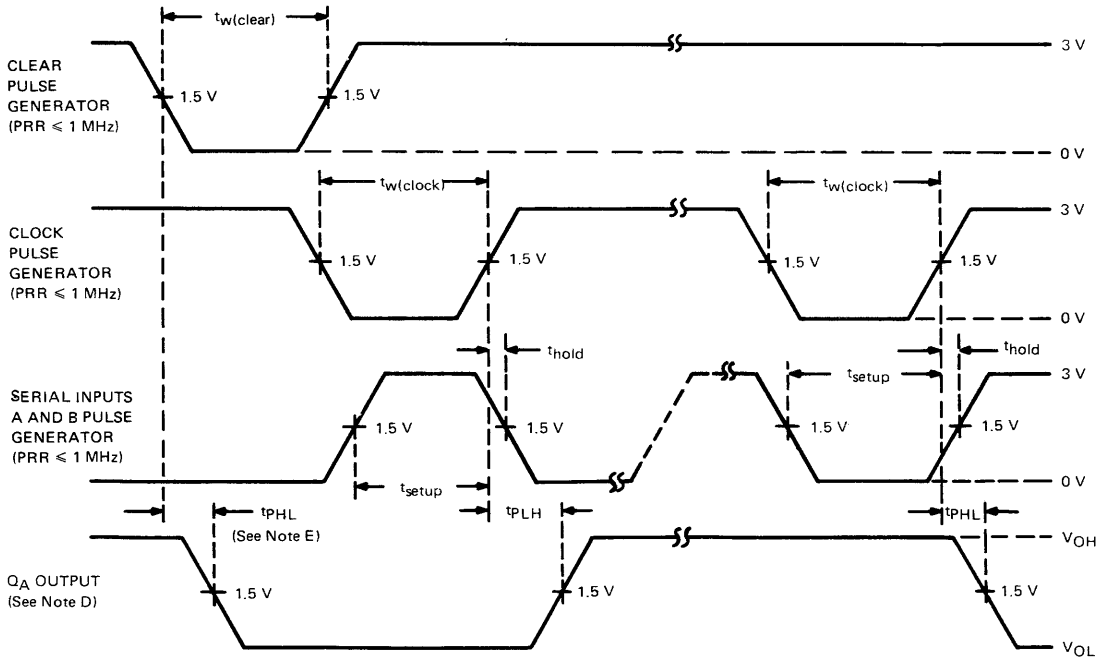
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.
D. Q_A output is illustrated. Relationship of serial input A and B data to other Q outputs is illustrated in the typical shift sequence.
E. Outputs are set to the high level prior to the measurement of t_{PHL} from the clear input.

FIGURE 1–SWITCHING TIMES

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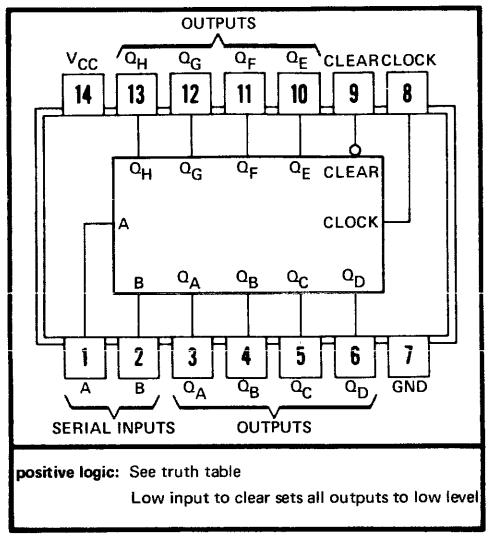
CIRCUIT TYPES SN54L164, SN74L164
8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

- Gated (Enable/Disable) Serial Inputs
- Fully Buffered Clock and Serial Inputs
- Asynchronous Clear
- Typical Maximum Input Clock Frequency . . . 18 MHz
- Typical Power Dissipation . . . 11 mW per Bit

J OR N DUAL-IN-LINE
OR T FLAT PACKAGE (TOP VIEW)†



†Pin assignments for these circuits are the same for all packages.

TRUTH TABLE
SERIAL INPUTS A AND B

INPUTS AT t_n		OUTPUT AT t_{n+1}
A	B	Q_A
H	H	H
L	H	L
H	L	L
L	L	L

description

These 8-bit shift registers feature gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data as a low at either (or both) input(s) inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high, but only information meeting the setup requirements will be entered. Clocking occurs on the low-to-high-level transition of the clock input.

The circuit is the same as for the SN54164/SN74164 except that all resistor values are doubled. All inputs are diode-clamped to minimize transmission-line effects, and are buffered to represent only one-half of one normalized Series 54/74 load, or approximately five Series 54L/74L loads at a low logic level, two Series 54L/74L loads at a high logic level. Power dissipation is typically 11 milliwatts per bit. Maximum input clock frequency is typically 18 megahertz.

The SN54L164 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74L164 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: SN54L164 Circuits . . . . . −55°C to 125°C
SN74L164 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

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recommended operating conditions

			SN54L164			SN74L164			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}			4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	Series 54L/74L Gates				20			20	
	Series 54L/74L Gates with 8-kΩ base resistors¶	High logic level			10			10	
		Low logic level			5			5	
Input clock frequency, f_{clock}			0		12	0		12	MHz
Width of clock or clear input pulse, t_w			40			40			ns
Data setup time, t_{setup} (see Figure 1)			30			30			ns
Data hold time, t_{hold} (see Figure 1)			0			0			ns
Operating free-air temperature, T_A			−55		125	0		70	°C

¶ This applies for all inputs of circuit types SN54L164 and SN74L164.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54L164			SN74L164			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MAX, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −200 μA	2.4			2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 4 mA			0.4			0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V			−0.8			−0.8	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	−5		−20	−4		−20	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2			27			27	mA

NOTE 2: I_{CC} is measured with outputs open, serial inputs grounded, the clock input at 2.4 V, and a momentary ground, then 4.5 V, applied to clear.

†For conditions shown at MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

§Not more than two outputs should be shorted at a time.

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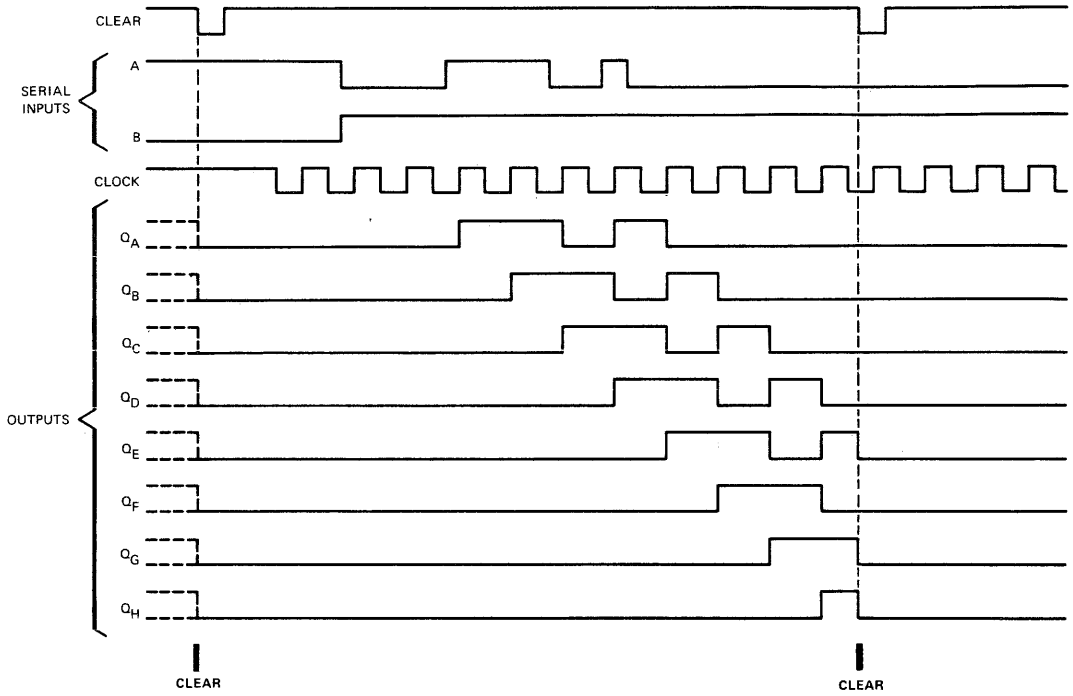
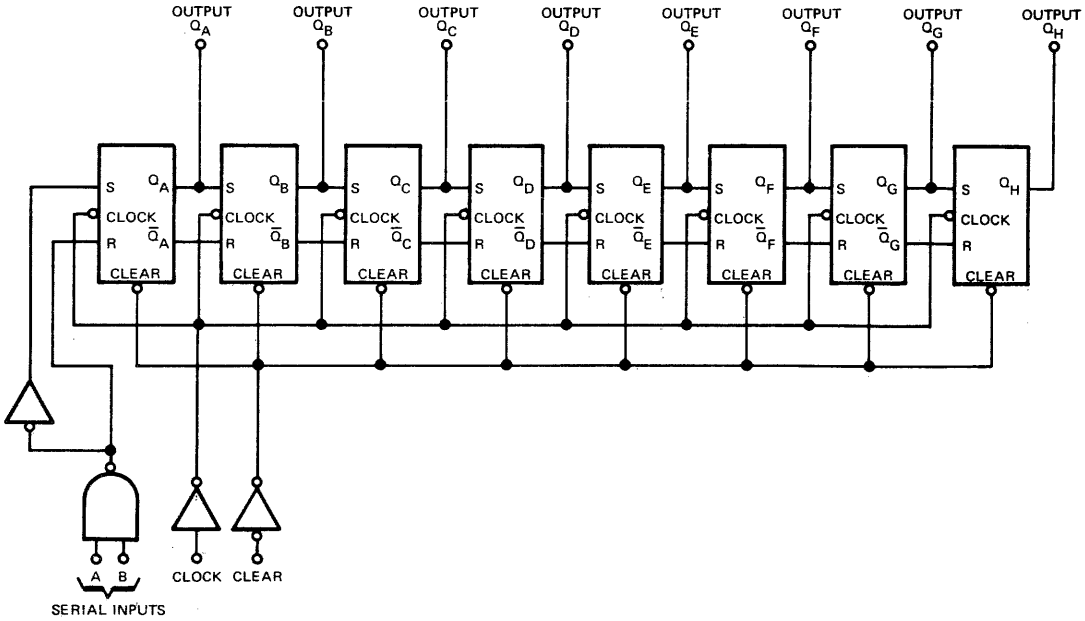
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 5

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Maximum input count frequency	R_L = 800 Ω, See Figure 1	C_L = 15 pF	12	18		MHz
t_{PHL}	Propagation delay time, high-to-low-level Q outputs from clear input		C_L = 15 pF			72	ns
			C_L = 50 pF			84	
t_{PLH}	Propagation delay time, low-to-high-level Q outputs from clock input		C_L = 15 pF	8		54	ns
			C_L = 50 pF	10		60	
t_{PHL}	Propagation delay time, high-to-low-level Q outputs from clock input		C_L = 15 pF	10		64	ns
			C_L = 50 pF	10		74	

typical clear, inhibit, shift, clear, and inhibit sequences



functional block diagram



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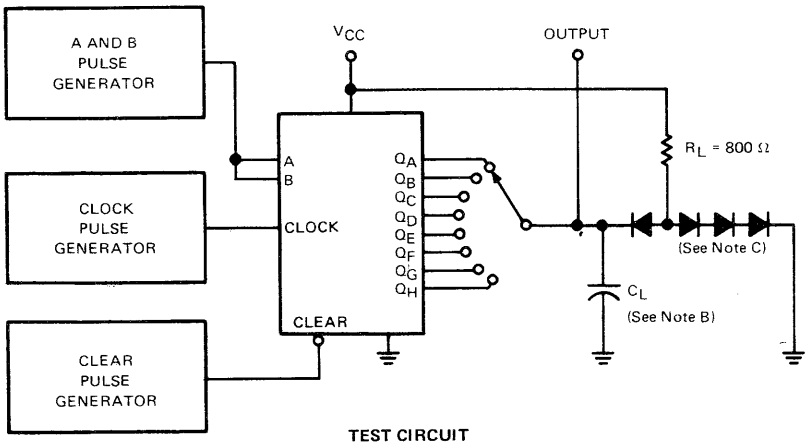
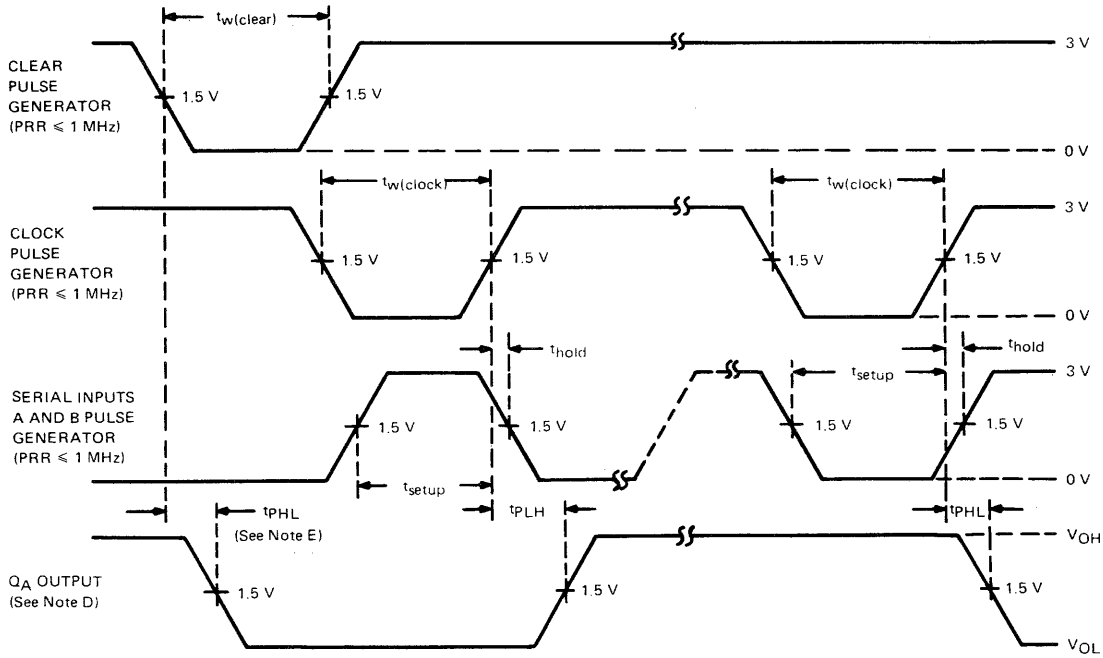
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916.
D. Q_A output is illustrated. Relationship of serial input A and B data to other Q outputs is illustrated in the typical shift sequence.
E. Outputs are set to the high level prior to the measurement of t_{PHL} from the clear input.

FIGURE 1–SWITCHING TIMES

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TEXAS INSTRUMENTS
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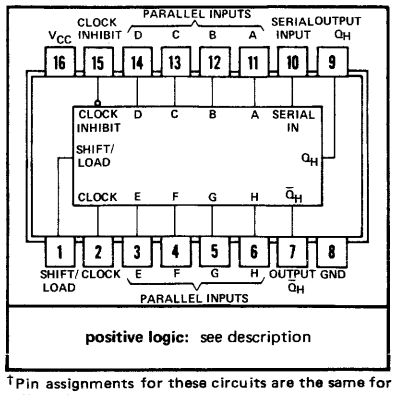
CIRCUIT TYPES SN54165, SN74165
PARALLEL-LOAD 8-BIT SHIFT REGISTERS

- Typical Maximum Input Clock Frequency . . . 26 MHz
- Complementary Outputs
- Direct Overriding Load (Data) Inputs
- Gated Clock Inputs
- Parallel-to-Serial Data Conversion

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



positive logic: see description

†Pin assignments for these circuits are the same for all packages.

description

The SN54165 and SN74165 are 8-bit serial shift registers which shift the data to the right when clocked. Parallel-in access to each stage is made available by eight individual direct data inputs which are enabled by a low level at the shift/load input. These registers also feature gated clock inputs and complementary outputs from the eighth bit.

Clocking is accomplished through a 2-input positive-NOR gate, permitting one input to be used as a clock-inhibit function. Holding either of the clock inputs high inhibits clocking, and holding either clock input low with the load input high enables the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. Parallel loading is inhibited as long as the load input is high. When taken low, data at the parallel inputs are loaded directly into the register independently of the state of the clock.

All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design. Power dissipation is typically 210 milliwatts and maximum input clock frequency is typically 26 megahertz. The SN54165 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74165 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54165 Circuits . . . . . −55°C to 125°C
SN74165 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies to the shift/load input in conjunction with the clock or clock-inhibit inputs.

recommended operating conditions

		SN54165			SN74165			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Input clock frequency, f_{clock}		0		20	0		20	MHz
Width of clock input pulse, $t_{w(clock)}$		25			25			ns
Width of load input pulse, $t_{w(load)}$		15			15			ns
Clock-enable setup time, t_{setup} (see Figure 1)		30			30			ns
Parallel input setup time, t_{setup} (see Figure 1)		10			10			ns
Serial input setup time, t_{setup} (see Figure 2)		20			20			ns
Shift setup time, t_{setup} (see Figure 2)		45			45			ns
Hold time at any input, t_{hold}		0			0			ns
Operating free-air temperature, T_A		−55	25	125	0	25	70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	SN54165			SN74165			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage		V_{CC} = MAX, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA	2.4			2.4			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.4			0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	Load input	V_{CC} = MAX, V_I = 2.4 V			80			80	μA
		Other inputs				40			40	
I_{IL}	Low-level input current	Load input	V_{CC} = MAX, V_I = 0.4 V			−3.2			−3.2	mA
		Other inputs				−1.6			−1.6	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	−20		−55	−18		−55	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 3		42	63		42	63	mA

NOTE 3: With the outputs open, clock inhibit and shift/load at 4.5 V, and a clock pulse applied to the clock input, I_{CC} is measured first with the parallel inputs at 4.5 V, then with the parallel inputs grounded.

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			C_L = 15 pF, R_L = 400 Ω, See figures 1 thru 3	20	26		MHz
t_{PLH}	Load	Any			21	31	ns
t_{PHL}					27	40	
t_{PLH}	Clock	Any			16	24	ns
t_{PHL}					21	31	
t_{PLH}	H	Q_H			11	17	ns
t_{PHL}					24	36	
t_{PLH}	H	$\overline{Q}_H$			18	27	ns
t_{PHL}					18	27	

¶f_{max} ≡ Maximum input count frequency
t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output

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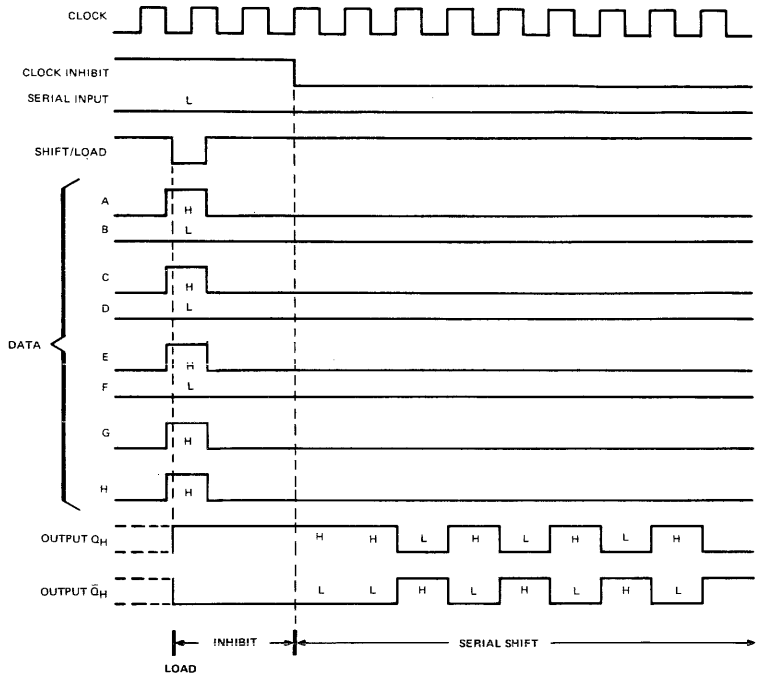
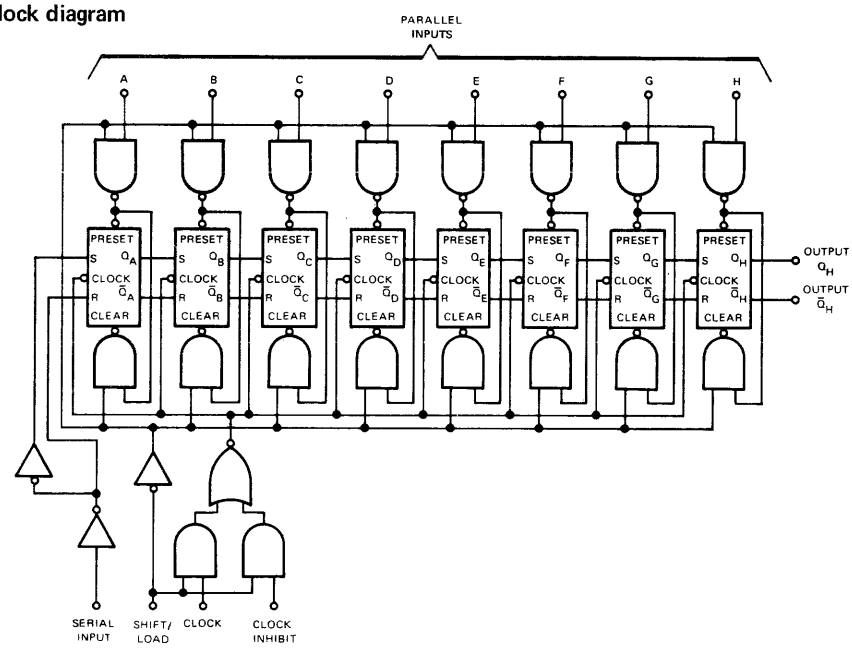
typical shift, load, and inhibit sequences



functional block diagram



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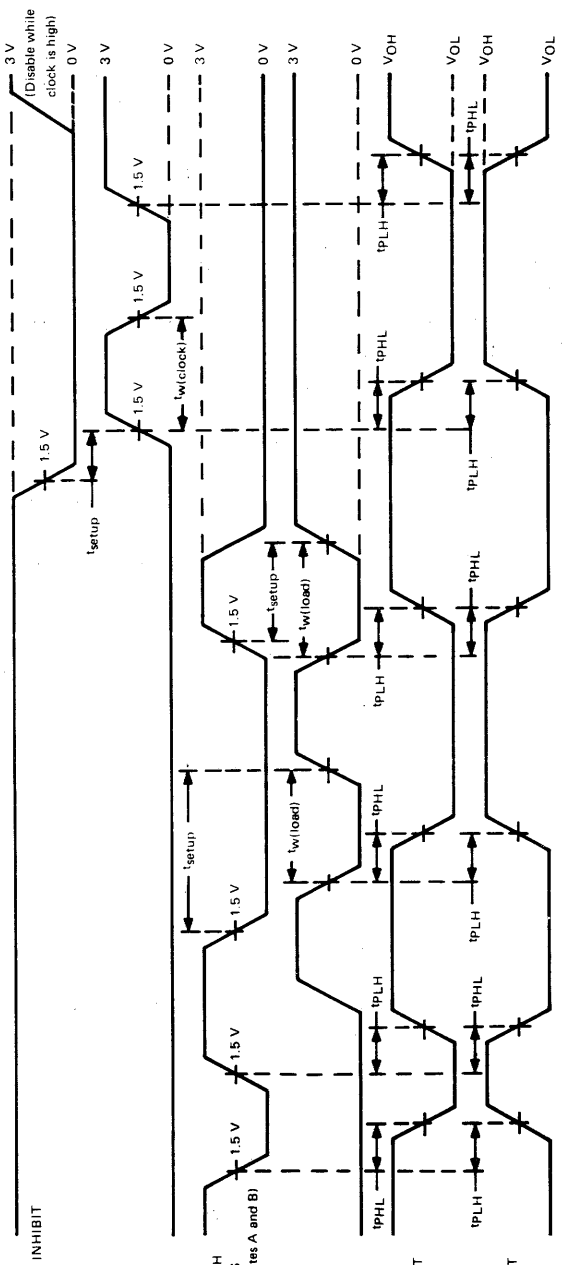
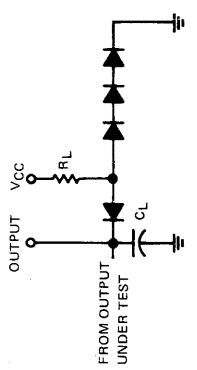
PARAMETER MEASUREMENT INFORMATION



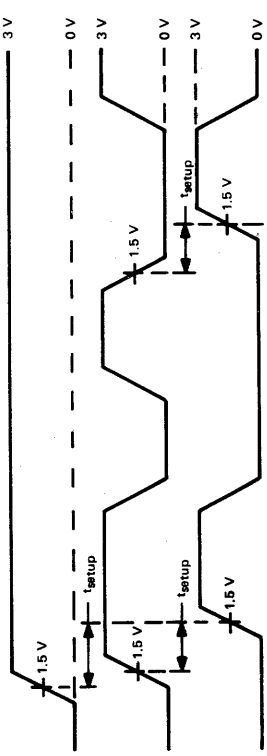
NOTES: A. The remaining six data inputs and the serial input are low.
B. Prior to test, high-level data is loaded into H input.
C. The input pulse generators have the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, PRR ≤ 1 MHz, duty cycle $\leq 50\%$, $Z_{out} \approx 50\ \Omega$. When testing f_{max}, vary clock PRR.

FIGURE 1–VOLTAGE WAVEFORMS



NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are IN3064.

FIGURE 3–LOAD CIRCUIT FOR SWITCHING TESTS



NOTES: A. The eight data inputs and the clock-inhibit input are low. Results are monitored at output Q_H at t_{n+7}.
B. The input pulse generators have the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, PRR ≤ 1 MHz, duty cycle $\leq 50\%$, $Z_{out} \approx 50\ \Omega$.

FIGURE 2–VOLTAGE WAVEFORMS

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CIRCUIT TYPES SN54166, SN74166, SN54198, SN74198, SN54199, SN74199
8-BIT SHIFT REGISTERS

description

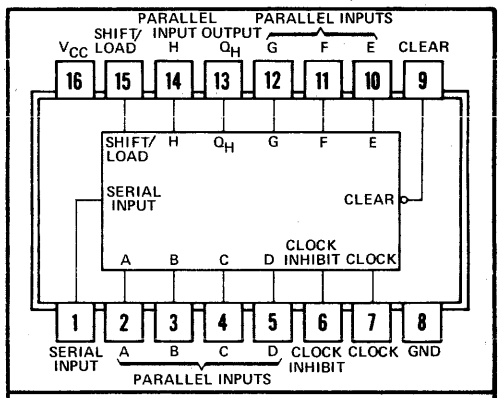
These 8-bit shift registers are compatible with most other TTL, DTL, and MSI logic families. All inputs are buffered to lower the drive requirements to one normalized Series 54/74 load, and input clamping diodes minimize switching transients to simplify system design. Maximum input clock frequency is typically 35 megahertz and power dissipation is typically 360 mW.

All Series 54 devices are characterized for operation over the full military temperature range of −55°C to 125°C; all Series 74 devices are characterized for operation from 0°C to 70°C.

SN54166 and SN74166

These parallel-in or serial-in, serial-out shift registers have a complexity of 77 equivalent gates on a monolithic chip. They feature gated clock inputs and an overriding clear input. The parallel-in or serial-in modes are established by the shift/load input. When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. When low, the parallel (broadside) data inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high-level edge of the clock pulse through a two-input positive NOR gate permitting one input to be used as a clock-enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This, of course, allows the system clock to be free-running and the register can be stopped on command with the gate input. The clock-inhibit input should be changed to the high level only while the clock input is high. A buffered, direct clear input overrides all other inputs, including the clock and sets all flip-flops to zero. Average power dissipation per gate is typically 4.7 mW.

SN54166 and SN74166
J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



positive logic: See description

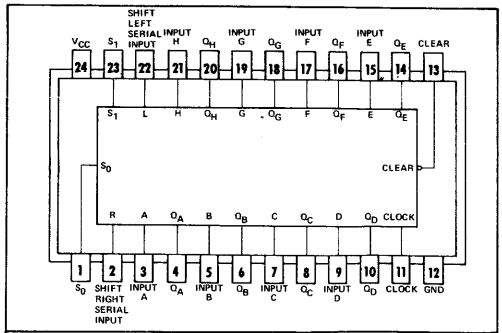
SN54198 and SN74198

The bidirectional registers are designed to incorporate virtually all of the features a system designer may want in a shift register. These circuits contains 87 equivalent gates and feature parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

Parallel (Broadside) Load
Shift Right (In the direction Q_A toward Q_H)
Shift Left (In the direction Q_H toward Q_A)
Inhibit Clock (Do nothing)

Synchronous parallel loading is accomplished by applying the eight bits of data and taking both mode control inputs, S_0 and S_1, high. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

SN54198 and SN74198
J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



positive logic: See truth table for mode control (S_0, S_1)

†Pin assignments for these circuits are the same for all packages.

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SN54198 and SN74198 (continued)

Shift right is accomplished synchronously with the rising edge of the clock pulse when S_0 is high and S_1 is low. Serial data for this mode is entered at the shift-right data input. When S_0 is low and S_1 is high, data shifts left synchronously and new data is entered at the shift-left serial input.

Clocking of the flip-flop is inhibited when both mode control inputs are low. The mode controls should be changed only while the clock input is high.

Average power dissipation per gate is typically 4.15 mW.

SN54198/SN74198
OPERATION OF MODE CONTROL

INPUTS		MODE
S_1	S_0	
L	L	INHIBIT CLOCK
L	H	SHIFT RIGHT
H	L	SHIFT LEFT
H	H	PARALLEL LOAD

SN54199 and SN74199

These synchronous 8-bit registers feature parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, shift/load control input, a direct overriding clear line, and gated clock inputs. The register has three modes of operation:

Parallel (Broadside) Load
Shift (In the direction Q_A toward Q_H)
Inhibit Clock (Do nothing)

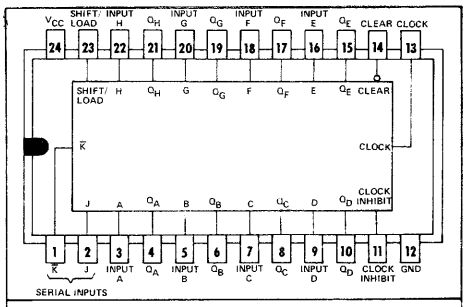
Parallel loading is accomplished by applying the eight bits of data and taking the shift/load control input low when the clock input is not inhibited. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shifting is accomplished synchronously when shift/load is high and the clock input is not inhibited. Serial data for this mode is entered at the J-$\overline{K}$ inputs. See the J-$\overline{K}$ inputs truth table for states required to enter serial data into the first flip-flop.

Both of the clock inputs are identical in function and may be used interchangeably to serve as clock or clock-inhibit inputs. Holding either high inhibits clocking, but when one is held low, a clock input applied to the other input is passed to the eight flip-flops of the register. The clock-inhibit input should be changed to the high level only while the clock input is high.

These shift registers contain the equivalent of 79 TTL gates. Average power dissipation per gate is typically 4.55 mW.

SN54199 and SN74199
J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



positive logic: See description

†Pin assignments for these circuits are the same for all packages.

SN54199/SN74199
TRUTH TABLE
J-$\overline{K}$ INPUTS

INPUTS at t_n		OUTPUT t_{n+1}
J	$\overline{K}$	Q_A
L	H	Q_{An}
L	L	L
H	H	H
H	L	$\overline{Q}_{An}$

H = high level, L = low level

NOTES: A. t_n = bit time before clock pulse
B. t_{n+1} = bit time after clock pulse

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Operating free-air temperature range:
SN54166, SN54198, and SN54199 Circuits . . . . . −55°C to 125°C
SN74166, SN74198, and SN74199 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54166 SN54198 SN54199			SN74166 SN74198 SN74199			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Input count frequency, f_{count}		0		25	0		25	MHz
Width of clock or clear pulse, t_w (see Figure 1)		20			20			ns
Mode-control setup time, t_{setup}		30			30			ns
Data setup time, t_{setup} (see Figure 1)		20			20			ns
Hold time at any input, t_{hold} (see Figure 1)		0			0			ns
Operating free-air temperature, T_A		−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54166 SN54198 SN54199			SN74166 SN74198 SN74199			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MAX, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA	2.4			2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.4			0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	−20		−57	−18		−57	mA
I_{CC}	Supply current	V_{CC} = MAX, See Table Below		72	104		72	116	mA

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† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

TEST CONDITIONS FOR I_{CC}
(ALL OUTPUTS ARE OPEN.)

TYPE	APPLY 4.5 V	FIRST GROUND, THEN APPLY 4.5 V	GROUND
SN54166, SN74166	Serial Input	Clock	All other inputs
SN54198, SN74198	Serial Input, S_0, S_1	Clock	Clear, Inputs A thru H
SN54199, SN74199	J, $\overline{K}$, Inputs A thru H	Clock	Clock Inhibit, Clear, Shift/Load

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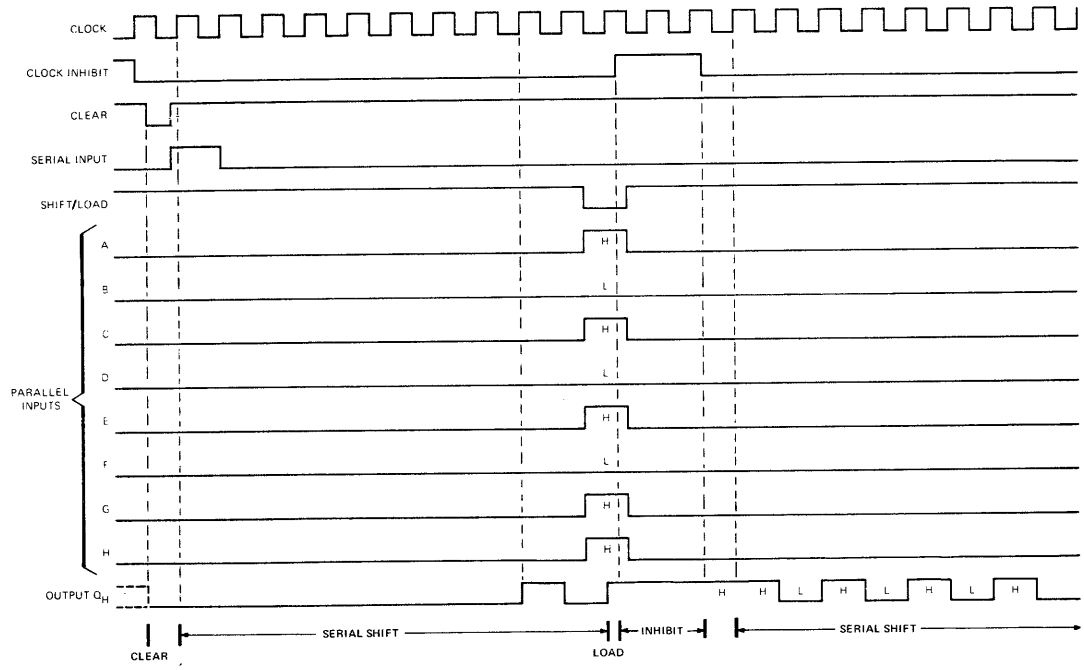
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum input count frequency	C_L = 15 pF, R_L = 400 Ω, See Figure 1	25	35		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear			23	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock		8	20	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock		8	17	26	ns

SN54166, SN74166

typical clear, shift, load, inhibit, and shift sequences



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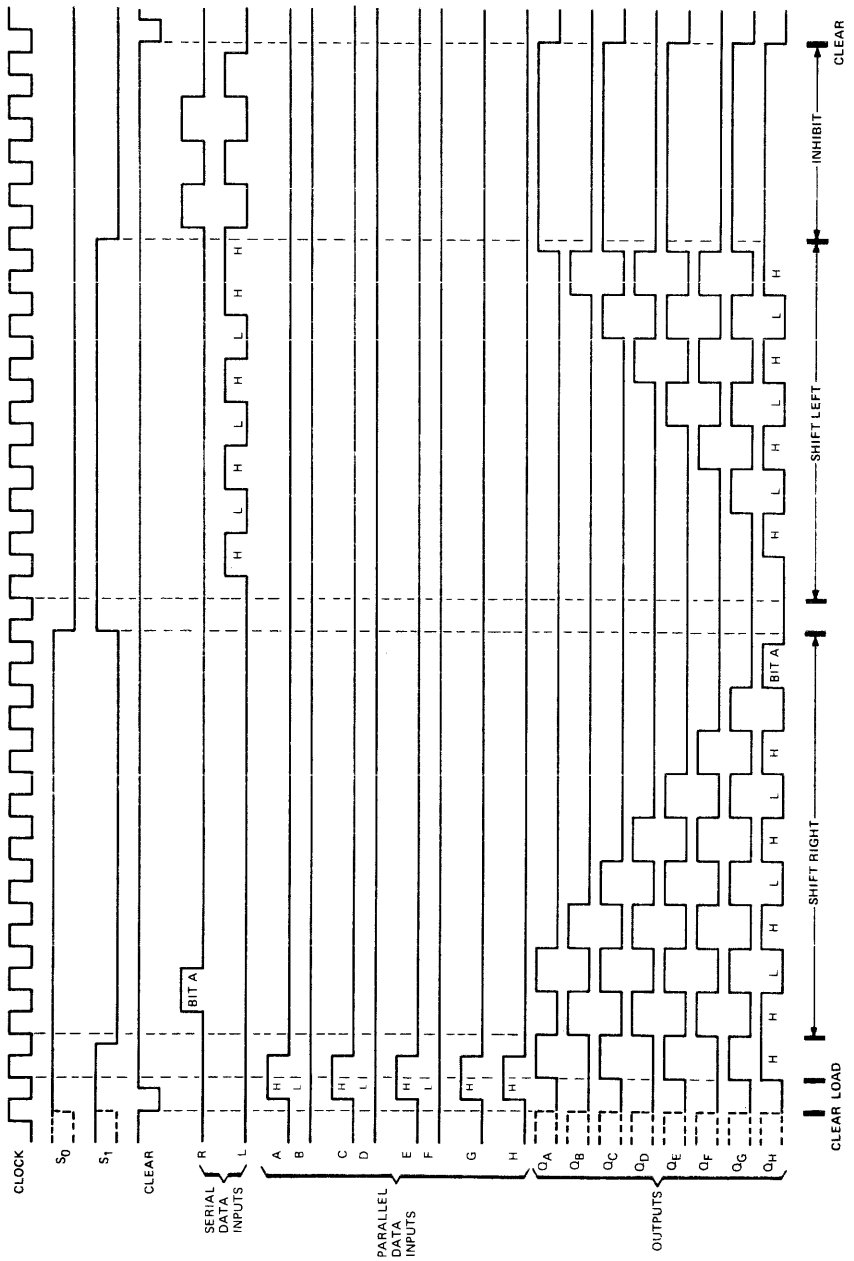
SN54198, SN74198

typical clear, load, right-shift, left-shift, inhibit, and clear sequences



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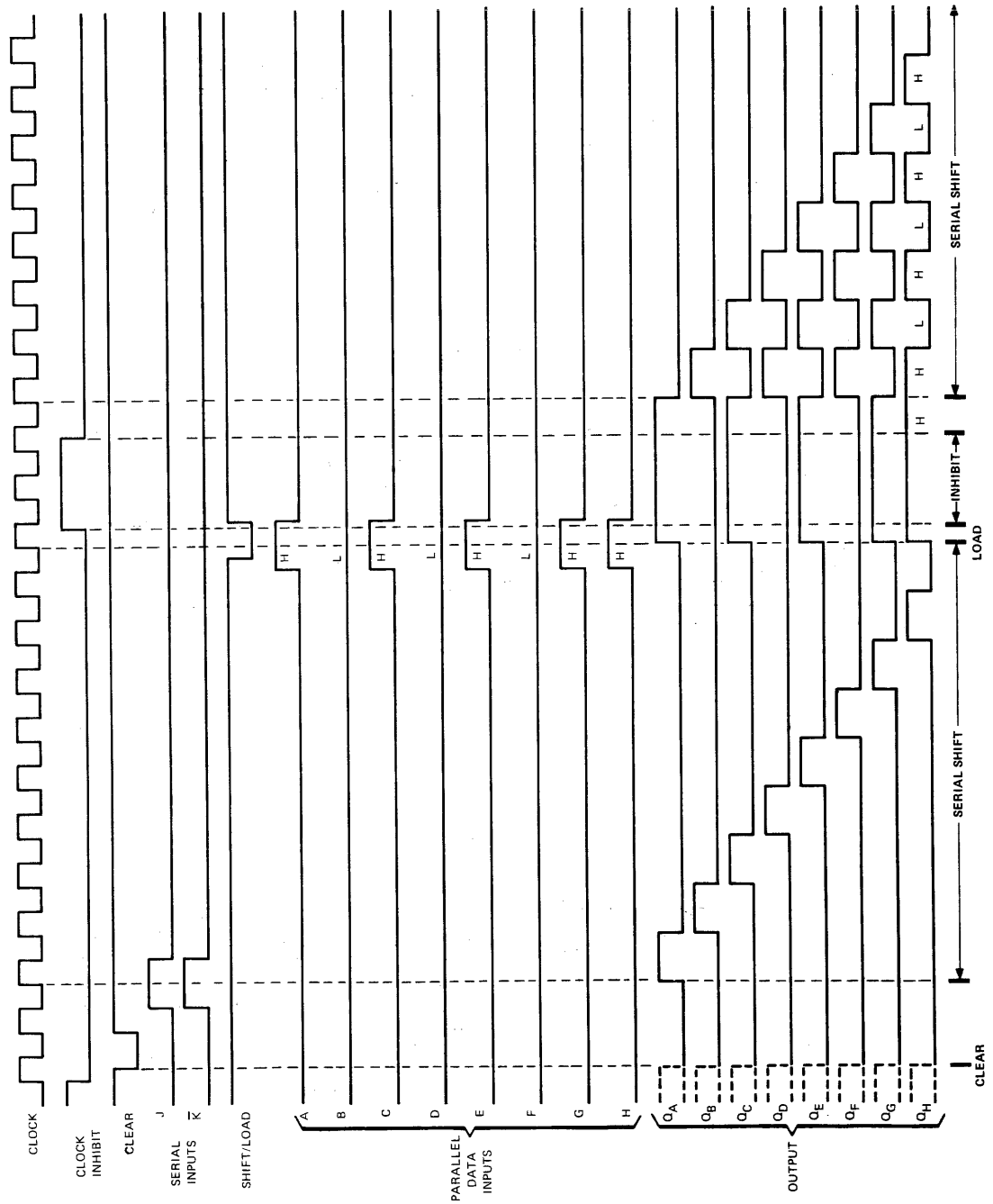
SN54199, SN74199

typical clear, shift, load, and inhibit sequences



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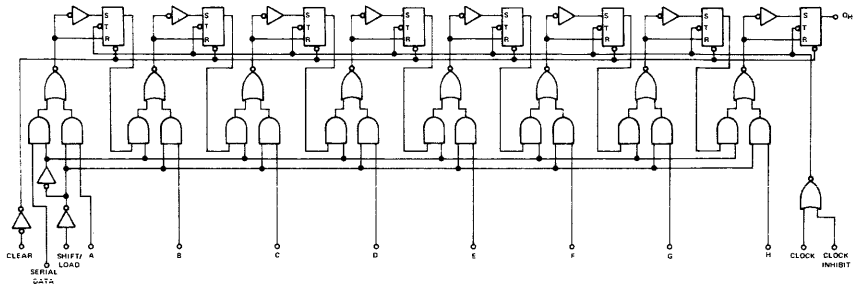
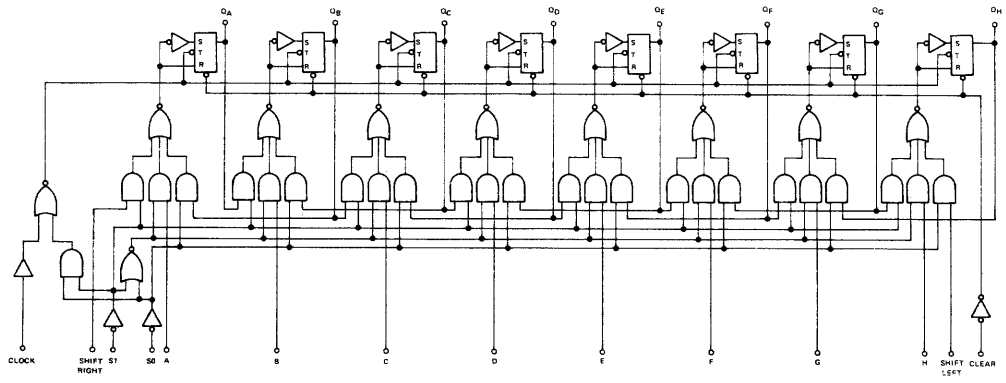
functional block diagrams

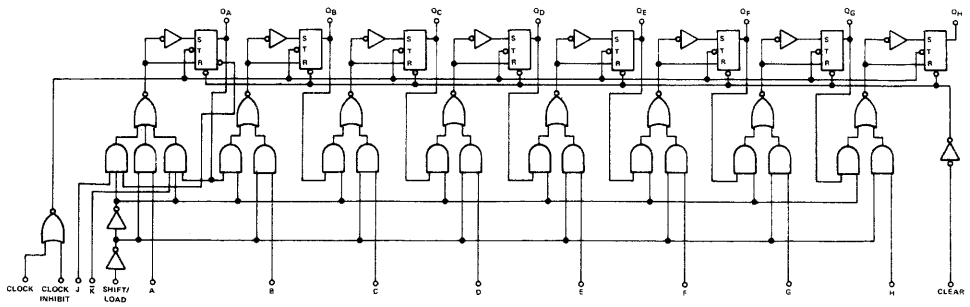
SN54166, SN74166



SN54198, SN74198



SN54199, SN74199



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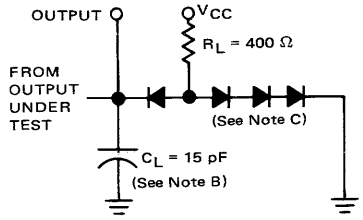
PARAMETER MEASUREMENT INFORMATION



LOAD FOR OUTPUT UNDER TEST

SN54166, SN74166
TEST TABLE FOR SYNCHRONOUS INPUTS

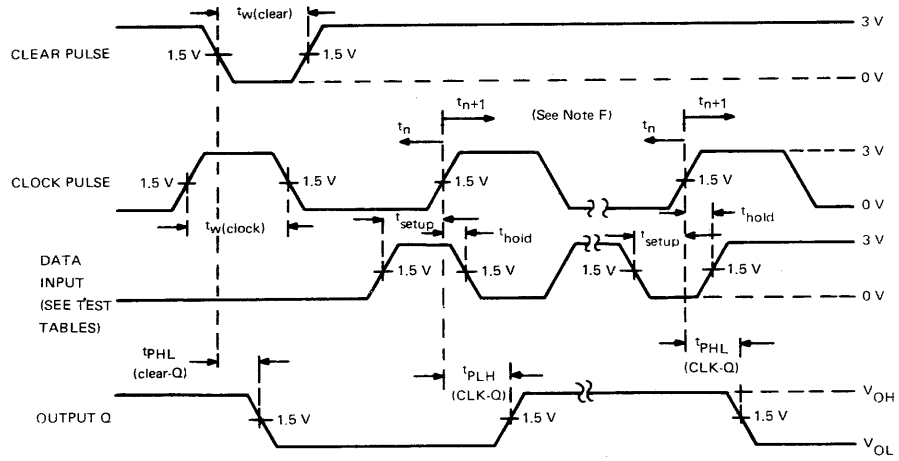
DATA INPUT FOR TEST	SHIFT/LOAD	OUTPUT TESTED (SEE NOTE E)
H	0 V	Q_H at t_{n+1}
Serial Input	4.5 V	Q_H at t_{n+8}

SN54198, SN74198
TEST TABLE FOR SYNCHRONOUS INPUTS

DATA INPUT FOR TEST	S_1	S_0	OUTPUT TESTED (SEE NOTE E)
A	4.5 V	4.5 V	Q_A at t_{n+1}
B	4.5 V	4.5 V	Q_B at t_{n+1}
C	4.5 V	4.5 V	Q_C at t_{n+1}
D	4.5 V	4.5 V	Q_D at t_{n+1}
E	4.5 V	4.5 V	Q_E at t_{n+1}
F	4.5 V	4.5 V	Q_F at t_{n+1}
G	4.5 V	4.5 V	Q_G at t_{n+1}
H	4.5 V	4.5 V	Q_H at t_{n+1}
L Serial Input	4.5 V	0 V	Q_A at t_{n+8}
R Serial Input	0 V	4.5 V	Q_H at t_{n+8}

SN54199, SN74199
TEST TABLE FOR SYNCHRONOUS INPUTS

DATA INPUT FOR TEST	SHIFT/LOAD	OUTPUT TESTED (SEE NOTE E)
A	0 V	Q_A at t_{n+1}
B	0 V	Q_B at t_{n+1}
C	0 V	Q_C at t_{n+1}
D	0 V	Q_D at t_{n+1}
E	0 V	Q_E at t_{n+1}
F	0 V	Q_F at t_{n+1}
G	0 V	Q_G at t_{n+1}
H	0 V	Q_H at t_{n+1}
J and $\overline{K}$	4.5 V	Q_H at t_{n+8}



VOLTAGE WAVEFORMS

NOTES: A. The clock pulse has the following characteristics: $t_{w(clock)} \geq 20$ ns and PRR = 1 MHz. The clear pulse has the following characteristics: $t_{w(clear)} \geq 20$ ns and $t_{hold} = 0$ ns. When testing f_{max}, vary the clock PRR.

B. C_L includes probe and jig capacitance.

C. All diodes are 1N3064.

D. A clear pulse is applied prior to each test.

E. Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_{n+1}. Proper shifting of data is verified at t_{n+8} with a functional test.

F. t_n = bit time before clocking transition
t_{n+1} = bit time after one clocking transition
t_{n+8} = bit time after eight clocking transitions

FIGURE 1

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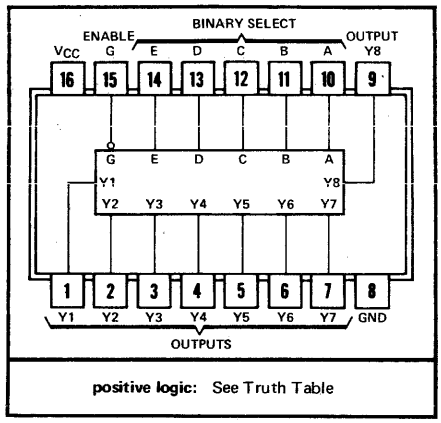
CIRCUIT TYPES SN54184, SN54185A, SN74184, SN74185A
BCD-TO-BINARY AND BINARY-TO-BCD CONVERTERS

SN54184, SN74184 BCD-TO-BINARY CONVERTERS
SN54185A, SN74185A BINARY-TO-BCD CONVERTERS

description

These monolithic converters are derived from the custom MSI 256-bit read-only memories SN5488 and SN7488. Emitter connections are made to provide direct read-out of converted codes at outputs Y8 through Y1 as shown in the truth tables. These converters demonstrate the versatility of a read-only memory in that an unlimited number of reference tables or conversion tables may be built into a system using economical, customized read-only memories. Both of these converters comprehend that the least significant bits (LSB) of the binary and BCD codes are logically equal, and in each case the LSB bypasses the converter as illustrated in the typical applications. This means that a 6-bit converter is produced in each case. Both devices are cascadable to N bits.

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)†



†Pin assignments for these circuits are the same for all packages.

An overriding enable input is provided on each converter which, when taken high inhibits the function, causing all outputs to go high. For this reason, and to minimize power consumption, unused outputs Y7 and Y8 of the SN54185A and SN54185A, and all "don't care" conditions of the SN54184 and SN74184 are programmed high. The outputs are of the open-collector type.

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The SN54184 and SN54185A are characterized for operation over the full military temperature range of −55°C to 125°C; the SN74184 and SN74185A are characterized for operation from 0°C to 70°C.

SN54184 and SN74184 BCD-to-binary converters

The 6-bit BCD-to-binary function of the SN54184 and SN74184 is analogous to the algorithm:

a. Shift BCD number right one bit and examine each decade. Subtract three from each 4-bit decade containing a binary value greater than seven.
b. Shift right, examine, and correct after each shift until the least significant decade contains a number smaller than eight and all other converted decades contain zeros.

TABLE I
SN54184, SN74184
PACKAGE COUNT AND DELAY TIMES
FOR BCD-TO-BINARY CONVERSION

INPUT (DECADES)	PACKAGES REQUIRED	TOTAL DELAY TIMES (ns)	
		TYP	MAX
2	2	50	80
3	6	125	200
4	11	175	280
5	19	250	400
6	28	325	520

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SN54185A and SN74185A binary-to-BCD converters

The function performed by these 6-bit binary-to-BCD converters is analogous to the algorithm:

a. Examine the three most significant bits. If the sum is greater than four, add three and shift left one bit.
b. Examine each BCD decade. If the sum is greater than four, add three and shift left one bit.
c. Repeat step b until the least-significant binary bit is in the least-significant BCD location.

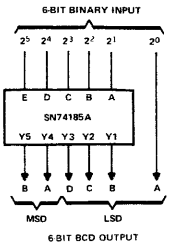
TABLE II

SN54185A, SN74185A

PACKAGE COUNT AND DELAY TIMES FOR BINARY-TO-BCD CONVERSION

INPUT (BITS)	PACKAGES REQUIRED	TOTAL DELAY TIME (ns)	
		TYP	MAX
4 to 6	1	25	40
7 or 8	3	50	80
9	4	75	120
10	6	100	160
11	7	125	200
12	8	125	200
13	10	150	240
14	12	175	280
15	14	175	280
16	16	200	320
17	19	225	360
18	21	225	360
19	24	250	400
20	27	275	440

6-BIT CONVERTER



TRUTH TABLE

BINARY WORDS	INPUTS						OUTPUTS						
	BINARY SELECT					ENABLE							
	E	D	C	B	A	G	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1
0 - 1	L	L	L	L	L	L	H	H	L	L	L	L	L	L
2 - 3	L	L	L	L	H	L	H	H	L	L	L	L	L	H
4 - 5	L	L	L	H	L	L	H	H	L	L	L	L	H	L
6 - 7	L	L	L	H	H	L	H	H	L	L	L	L	H	H
8 - 9	L	L	H	L	L	L	H	H	L	L	L	H	L	L
10 - 11	L	L	H	L	H	L	H	H	L	L	H	L	L	L
12 - 13	L	L	H	H	L	L	H	H	L	L	H	L	L	H
14 - 15	L	L	H	H	H	L	H	H	L	L	H	L	H	L
16 - 17	L	H	L	L	L	L	H	H	L	L	H	L	H	H
18 - 19	L	H	L	L	H	L	H	H	L	L	H	H	L	L
20 - 21	L	H	L	H	L	L	H	H	L	H	L	L	L	L
22 - 23	L	H	L	H	H	L	H	H	L	H	L	L	L	H
24 - 25	L	H	H	L	L	L	H	H	L	H	L	L	H	L
26 - 27	L	H	H	L	H	L	H	H	L	H	L	L	H	H
28 - 29	L	H	H	H	L	L	H	H	L	H	L	H	L	L
30 - 31	L	H	H	H	H	L	H	H	L	H	H	L	L	L
32 - 33	H	L	L	L	L	L	H	H	L	H	H	L	L	H
34 - 35	H	L	L	L	H	L	H	H	L	H	H	L	H	L
36 - 37	H	L	L	H	L	L	H	H	L	H	H	L	H	H
38 - 39	H	L	L	H	H	L	H	H	L	H	H	H	L	L
40 - 41	H	L	H	L	L	L	H	H	H	L	L	L	L	L
42 - 43	H	L	H	L	H	L	H	H	H	L	L	L	L	H
44 - 45	H	L	H	H	L	L	H	H	H	L	L	L	H	L
46 - 47	H	L	H	H	H	L	H	H	H	L	L	L	H	H
48 - 49	H	H	L	L	L	L	H	H	H	L	L	H	L	L
50 - 51	H	H	L	L	H	L	H	H	H	L	H	L	L	L
52 - 53	H	H	L	H	L	L	H	H	H	L	H	L	L	H
54 - 55	H	H	L	H	H	L	H	H	H	L	H	L	H	L
56 - 57	H	H	H	L	L	L	H	H	H	L	H	L	H	H
58 - 59	H	H	H	L	H	L	H	H	H	L	H	H	L	L
60 - 61	H	H	H	H	L	L	H	H	H	H	L	L	L	L
62 - 63	H	H	H	H	H	L	H	H	H	H	L	L	L	H
ALL	X	X	X	X	X	H	H	H	H	H	H	H	H	H

H = high level, L = low level, X = irrelevant

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: SN54184, SN54185A . . . . . −55°C to 125°C
SN74184, SN74185A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

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recommended operating conditions

	SN54184, SN54185A			SN74184, SN74185A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55	25	125	0	25	70	°C

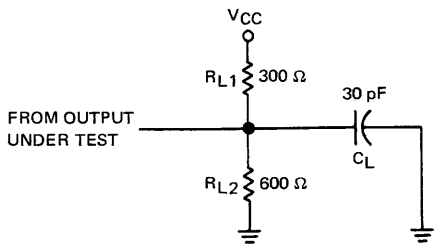
electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA			−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V,	V_{OH} = 5.5 V			100	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	I_{OL} = 12 mA			0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current (each input)	V_{CC} = MAX,	V_I = 2.4 V			40	μA
I_{IL}	Low-level input current (each input)	V_{CC} = MAX,	V_I = 0.4 V			−1	mA
I_{CCH}	Supply current, all outputs high	V_{CC} = MAX			50		mA
I_{CCL}	Supply current, all programmed outputs low				62	104	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25° C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from enable G	C_L = 30 pF, R_{L1} = 300 Ω, R_{L2} = 600 Ω		16	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output from enable G			22	35	ns
t_{PLH}	Propagation delay time, low-to-high-level output from binary select			25	40	ns
t_{PHL}	Propagation delay time, high-to-low-level output from binary select			20	32	ns



C_L includes probe and jig capacitance.

LOAD CIRCUIT

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TYPICAL APPLICATION DATA
SN54184, SN74184

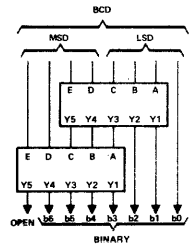

FIGURE 1–BCD-TO-BINARY CONVERTER
FOR TWO BCD DECADES

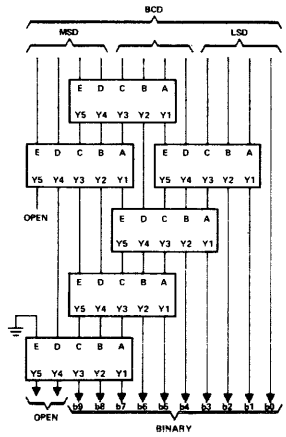

FIGURE 2–BCD-TO-BINARY CONVERTER
FOR THREE BCD DECADES

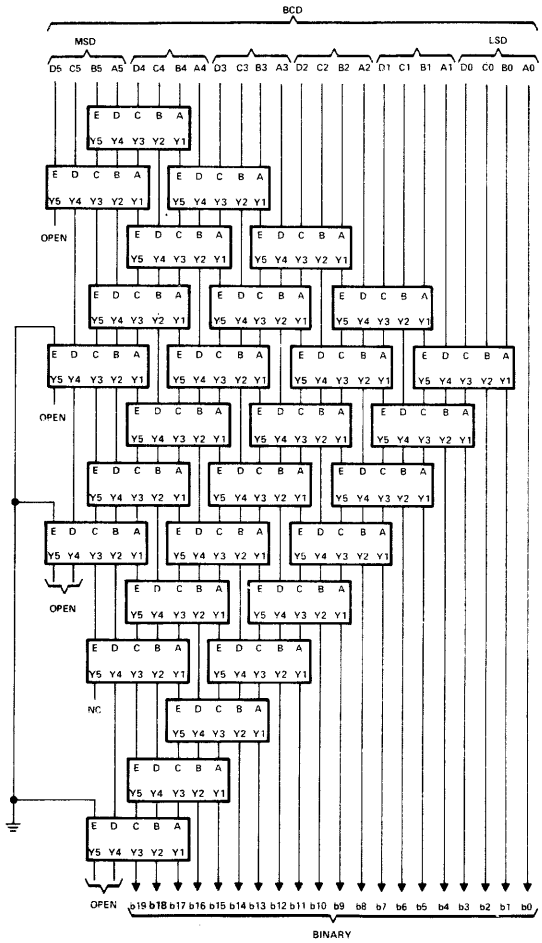

FIGURE 3–BCD-TO-BINARY CONVERTER
FOR SIX BCD DECADES

MSD–most significant decade
LSD–least significant decade
Each rectangle represents an SN54184 or SN74184.

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TYPICAL APPLICATION DATA
SN54185A, SN74185A

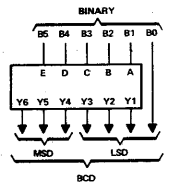

FIGURE 4—6-BIT BINARY-TO-BCD CONVERTER

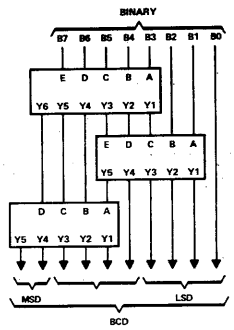

FIGURE 5—8-BIT BINARY-TO-BCD CONVERTER

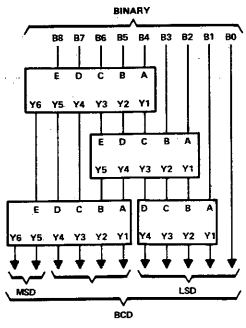

FIGURE 6—9-BIT BINARY-TO-BCD CONVERTER

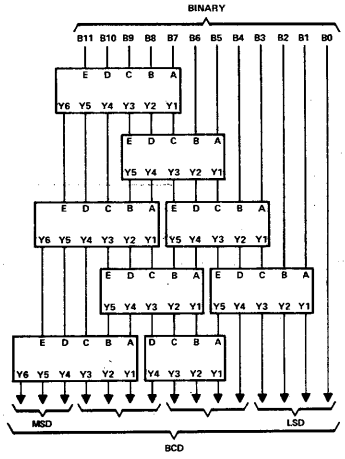

FIGURE 7—12-BIT BINARY-TO-BCD CONVERTER

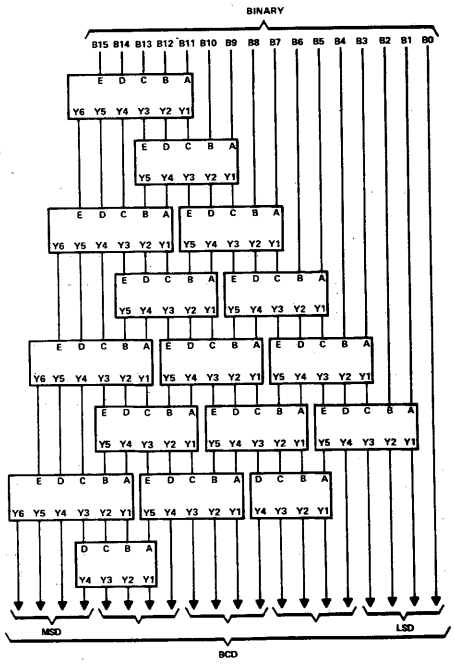

FIGURE 8—16-BIT BINARY-TO-BCD CONVERTER

MSD—Most significant decade
LSD—Least significant decade
Each rectangle represents an SN54185A or an SN74185A.

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CIRCUIT TYPES SN5442, SN5443, SN5444, SN7442, SN7443, SN7444
4-LINE-TO-10-LINE DECODERS (1-OF-10)

- BCD-to-Decimal
- Excess-3-to-Decimal
- Excess-3-Gray-to-Decimal

Also for applications as

- 4-Line-to-16-Line Decoders
- 3-Line to 8-Line Decoders

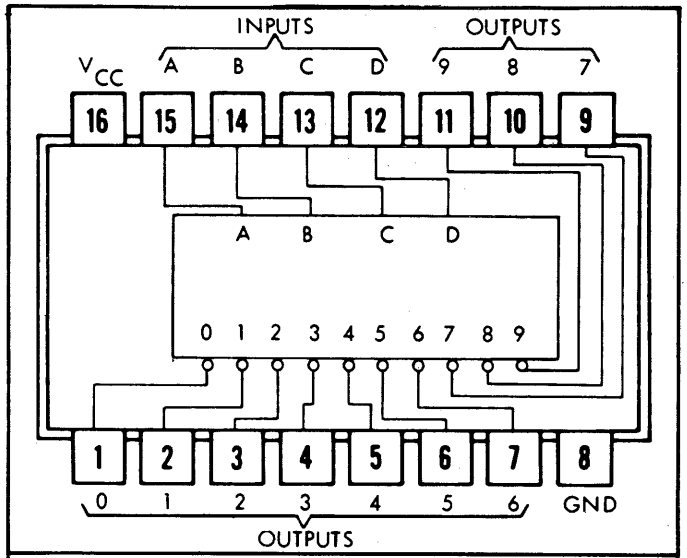
- featuring diode-clamped inputs

description

These monolithic decimal decoders consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all outputs remain off for all invalid input conditions.

The SN5442/SN7442 BCD-to-decimal, SN5443/SN7443 excess-3-to-decimal, and SN5444/SN7444 excess-3-gray-to-decimal decoders feature familiar transistor-transistor-logic (TTL) circuits with inputs and outputs which are compatible for use with other TTL and DTL circuits. D-c noise margins are typically one volt and power dissipation is typically 140 milliwatts. Full fan-out of 10 is available at all outputs.

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



positive logic: see truth tables

†Pin assignments for these circuits are the same for all packages.

SN5442/SN7442 BCD INPUT				SN5443/SN7443 EXCESS 3 INPUT				SN5444/SN7444 EXCESS 3 GRAY INPUT				ALL TYPES DECIMAL OUTPUT									
D	C	B	A	D	C	B	A	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	0	1	1	0	0	1	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	0	1	0	0	0	1	1	0	1	0	1	1	1	1	1	1	1	1
0	0	1	0	0	1	0	1	0	1	1	1	1	1	0	1	1	1	1	1	1	1
0	0	1	1	0	1	1	0	0	1	0	1	1	1	1	0	1	1	1	1	1	1
0	1	0	0	0	1	1	1	0	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	0	1	1	0	0	0	1	1	0	0	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	0	0	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1
0	1	1	1	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1
1	0	0	0	1	0	1	1	1	1	1	0	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	0	0	1	0	1	0	1	1	1	1	1	1	1	1	1	0
1	0	1	0	1	1	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	0	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
1	1	1	0	0	0	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	1	0	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

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absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply Voltage, V_{CC} (See Note 1) . . . . . 7 V
Input Voltage, V_{in} (See Note 1) . . . . . 5.5 V
Operating Free-Air Temperature Range: SN5442, SN5443, SN5444 Circuits . . . . . −55°C to 125°C
SN7442, SN7443, SN7444 Circuits . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1): SN5442, SN5443, SN5444 Circuits	4.5	5	5.5	V
SN7442, SN7443, SN7444 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each Output (N)			10	

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1 and 2			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	1 and 2					0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, $V_{in(1)}$ = 2 V, $V_{in(0)}$ = 0.8 V, I_{load} = −400 μA		2.4			V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, $V_{in(1)}$ = 2 V, $V_{in(0)}$ = 0.8 V, I_{sink} = 16 mA				0.4	V
$I_{in(1)}$	Logical 1 level input current (each input)	3	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(0)}$	Logical 0 level input current (each input)	4	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
I_{OS}	Short-circuit output current§	5	V_{CC} = MAX	SN5442, SN5443, SN5444	−20		−55	mA
				SN7442, SN7443, SN7444	−18		−55	mA
I_{CC}	Supply current	4	V_{CC} = MAX	SN5442, SN5443, SN5444		28	41	mA
				SN7442, SN7443, SN7444		28	56	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level through two logic levels	6	C_L = 15 pF, R_L = 400 Ω	10	22	30	ns
t_{pd0}	Propagation delay time to logical 0 level through three logic levels	6	C_L = 15 pF, R_L = 400 Ω		23	35	ns
t_{pd1}	Propagation delay time to logical 1 level through two logic levels	6	C_L = 15 pF, R_L = 400 Ω	10	17	25	ns
t_{pd1}	Propagation delay time to logical 1 level through three logic levels	6	C_L = 15 pF, R_L = 400 Ω		26	35	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

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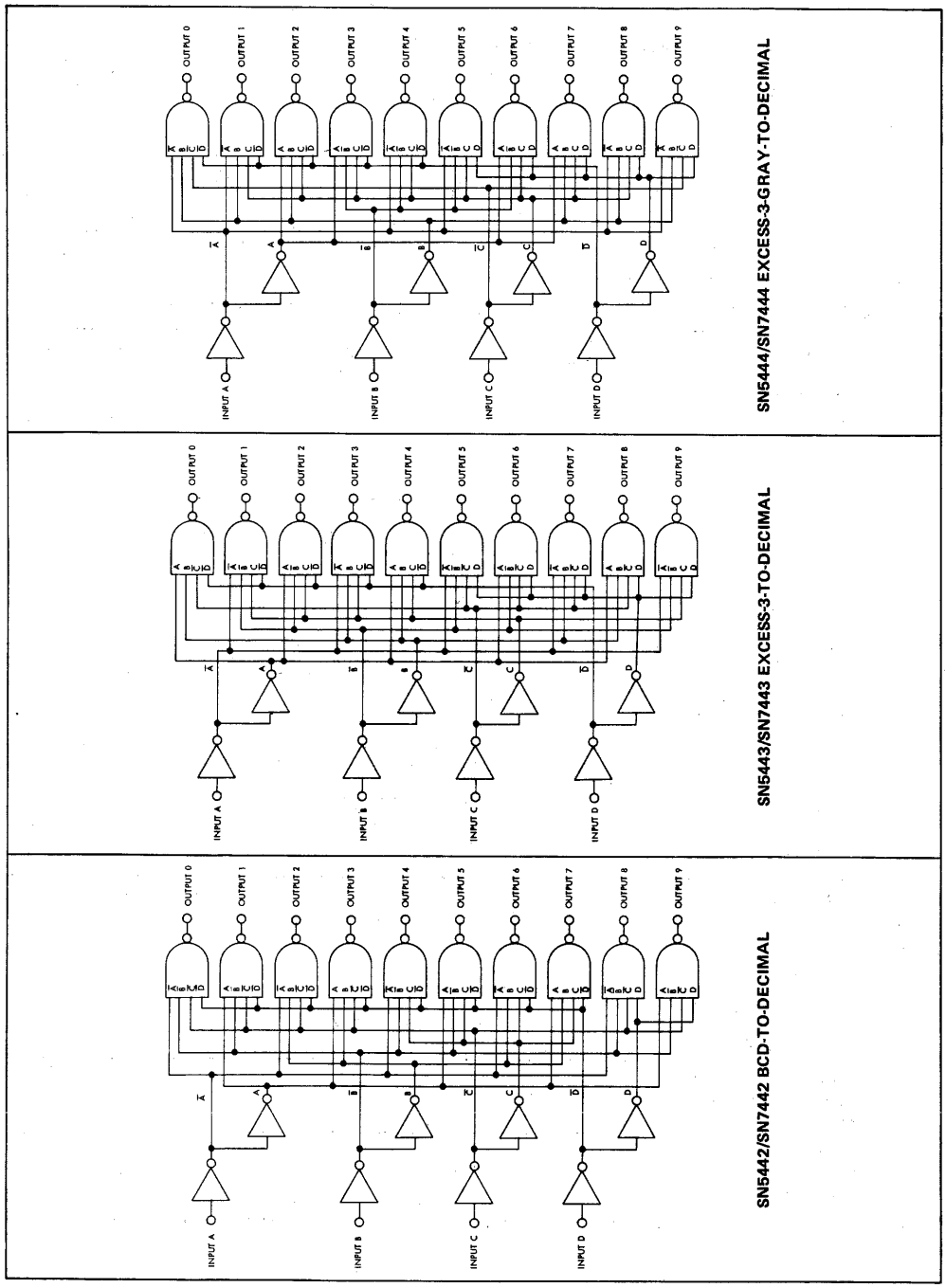
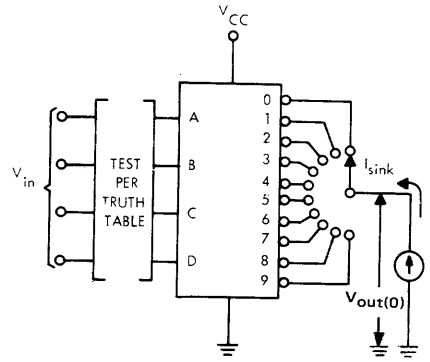
CIRCUIT TYPES SN5442, SN5443, SN5444, SN7442, SN7443, SN7444
4-LINE-TO-10-LINE DECODERS (1-OF-10)

functional block diagrams



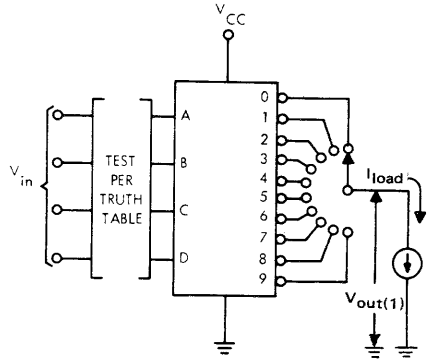
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



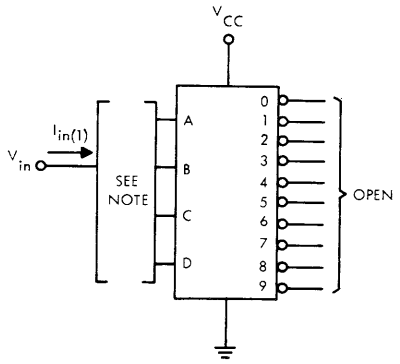
1. Each output is tested separately.

FIGURE 1



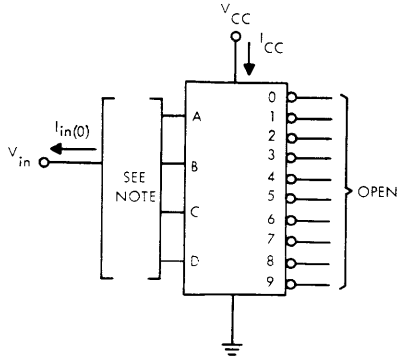
1. Each output is tested separately.

FIGURE 2



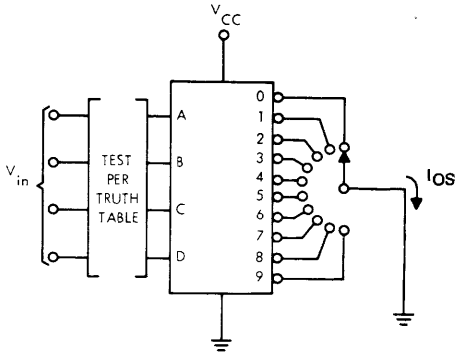
1. Each input is tested separately.

FIGURE 3



1. When testing $I_{in(0)}$ each input is tested separately.
2. When testing I_{CC} all inputs are grounded and outputs are open.

FIGURE 4



1. Each output is tested separately.

FIGURE 5

†Arrows indicate actual direction of current flow

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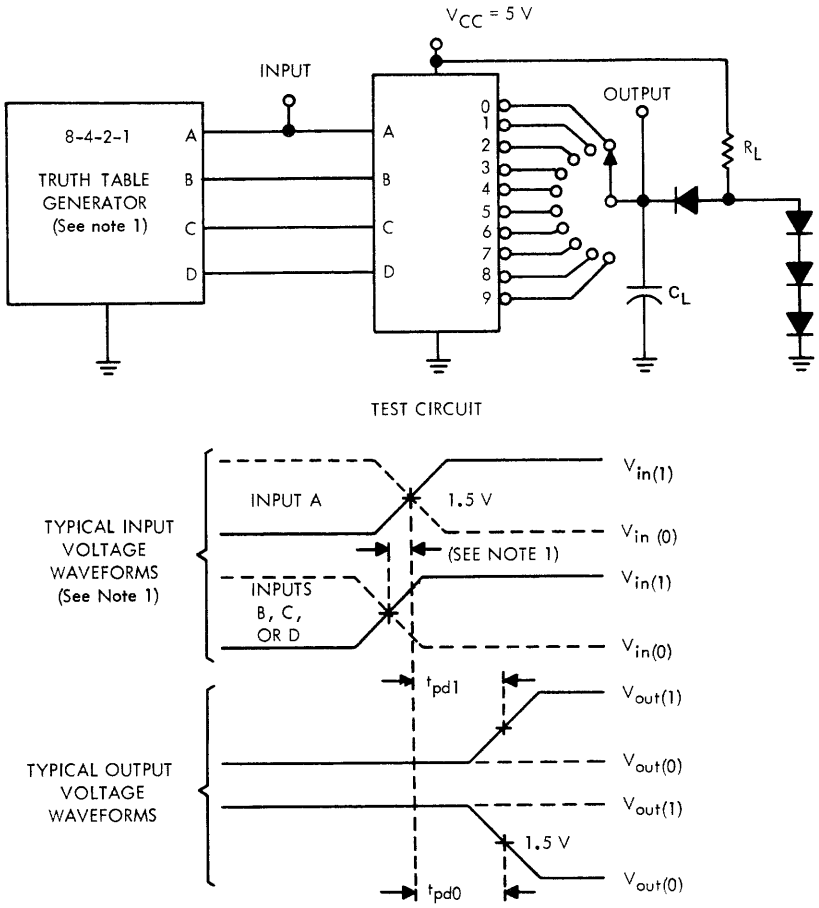
switching characteristics



NOTES: 1. The truth table generator has the following characteristics: $V_{out(1)} \geq 2.4$ V, $V_{out(0)} \leq 0.4$ V, t_r and $t_f < 10$ ns, and PRR = 1 MHz. Input B, C, and D transitions occur simultaneously with or prior to input A transistions.
2. C_L includes probe and jig capacitance.
3. All diodes are 1N3064.

FIGURE 6–SWITCHING TIMES

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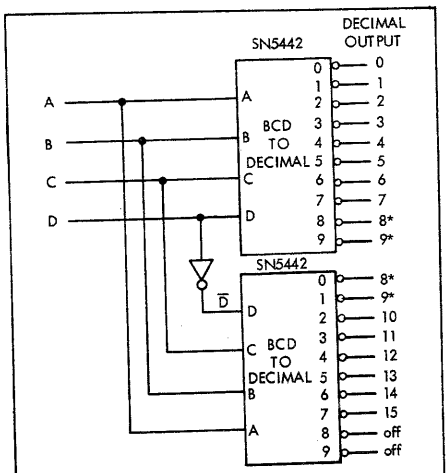
TYPICAL APPLICATIONS

decoding binary-to-decimal with SN5442/SN7442,

Figure A demonstrates a method for utilizing two SN5442/SN7442 decoders to perform 4-wire to 16-wire (1-of-16) decoding. Inputs A, B, and C of the two decoders are paralleled, D is applied to one decoder, and $\overline{D}$ is applied to the other as shown in figure A. Decimal equivalents are available as indicated. Note that decimal 8 and 9 are available from both decoders.



*These decimal outputs are available from both decoders.

FIGURE A

decoding 3-wire binary-to-octal

This application demonstrates a method for decoding 3-wire binary-to-octal using the SN5442/SN7442. See figure B. The binary code ABC is applied to the A, B, and C inputs and the D input is used as a strobe. When the strobe is taken to a logical 0 the octal data may be taken from outputs 0 through 7. Note that decimal outputs 8 and 9 are not used. See BCD truth table.

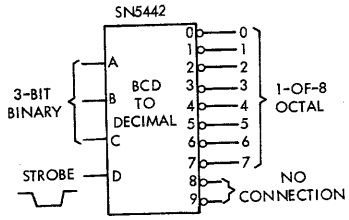


FIGURE B

This application demonstrates a method for decoding 3-wire binary-to-octal using the SN5444/SN7444. See figure C. The binary code ABC is applied to the A, B, and D inputs respectively and the C input is used as a strobe. When the strobe is taken to a logical 1 the octal data (as identified in figure C) may be taken from outputs 1 through 8. Note that outputs 0 and 9 are not used.

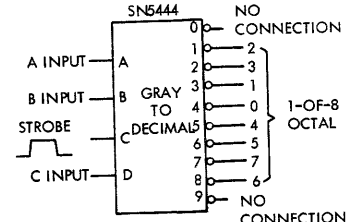


FIGURE C

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CIRCUIT TYPES SN54L42, SN54L43, SN54L44, SN74L42, SN74L43, SN74L44 4-LINE-TO-10-LINE DECODERS (1-OF-10)

SN54L42, SN74L42 . . . BCD-TO-DECIMAL

SN54L43, SN74L43 . . . EXCESS-3-TO-DECIMAL

SN54L44, SN74L44 . . . EXCESS-3-GRAY-TO-DECIMAL

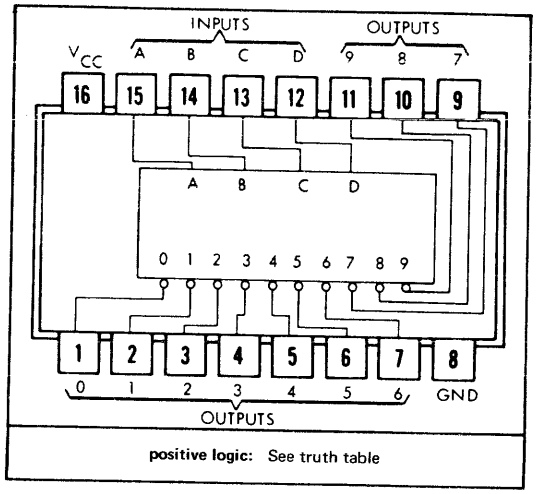
- Also for Applications as
  - 4-Line-to-16-Line Decoders
  - 3-Line-to-8-Line Decoders
- Diode-Clamped Inputs

description

These monolithic decimal decoders consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all outputs remain off for all invalid input conditions.

The SN54L42/SN74L42 BCD-to-decimal, SN54L43/SN74L43 excess-3-to-decimal, and SN54L44/SN74L44 excess-3-gray-to-decimal decoders feature familiar transistor-transistor logic (TTL) circuits with inputs and outputs which are compatible for use with other TTL and DTL circuits. D-c noise margins are typically one volt and power dissipation is typically 70 milliwatts. The diode-clamped inputs represent only one-half of one normalized Series 54/74 load, or approximately five Series 54L/74L gate loads at a low logic level, or two Series 54L/74L gate loads at a high logic level.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: See truth table

TRUTH TABLE

SN54L42/SN74L42 BCD INPUT				SN54L43/SN74L43 EXCESS-3-INPUT				SN54L44/SN74L44 EXCESS-3-GRAY INPUT				ALL TYPES DECIMAL OUTPUT									
D	C	B	A	D	C	B	A	D	C	B	A	0	1	2	3	4	5	6	7	8	9
L	L	L	L	L	L	H	H	L	L	H	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	L	L	L	H	H	L	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	H	L	H	H	L	L	H	L	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	L	H	H	H	L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	L	L	L	H	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	L	L	H	H	H	L	H	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	L	H	L	L	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	L	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H
H	H	H	L	L	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	H	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H

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absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: SN54L42, SN54L43, SN54L44 Circuits . . . . . −55°C to 125°C
SN74L42, SN74L43, SN74L44 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

			SN54L42, SN54L43, SN54L44			SN74L42, SN74L43, SN74L44			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}			4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	Series 54L/74L gates				40			40	
	Series 54L/74L inputs with 8-kΩ base resistors¶	High logic level			20			20	
		Low logic level			10			10	
Operating free-air temperature, T_A			−55		125	0		70	°C

¶ This applies to all inputs of all the circuit types on this data sheet.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	MAX	UNIT
V_{IH}	High-level input voltage	1 and 2			2		V
V_{IL}	Low-level input voltage	1 and 2				0.8	V
V_I	Input clamp voltage	3	V_{CC} = MIN, I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −400 μA		2.4		V
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 8 mA			0.4	V
I_I	Input current at maximum input voltage	3	V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	3	V_{CC} = MAX, V_I = 2.4 V			20	μA
I_{IL}	Low-level input current	3	V_{CC} = MAX, V_I = 0.4 V			−0.8	mA
I_{OS}	Short-circuit output current§	4	V_{CC} = MAX		−9	−28	mA
I_{CC}	Supply current	5	V_{CC} = MAX	SN54L42, SN54L43, SN54L44		22	mA
				SN74L42, SN74L43, SN74L44		28	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

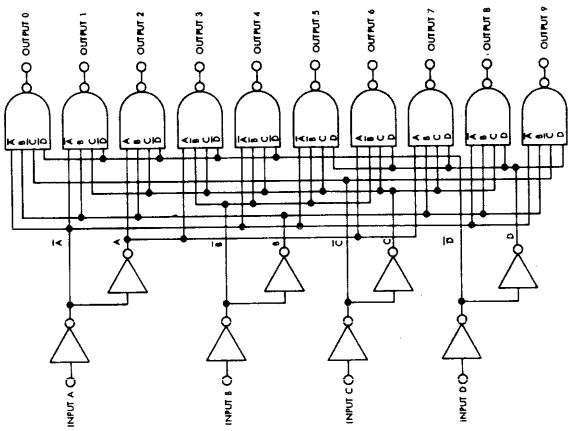
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level output from A, B, C, or D through 2 levels of logic	6	C_L = 15 pF, R_L = 400 Ω	10	60	ns
t_{PHL}	Propagation delay time, high-to-low-level output from A, B, C, or D through 3 levels of logic				70	ns
t_{PLH}	Propagation delay time, low-to-high-level output from A, B, C, and D through 2 levels of logic			10	50	ns
t_{PLH}	Propagation delay time, low-to-high-level output from A, B, C, and D through 3 levels of logic				70	ns

† For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions for the applicable device type.

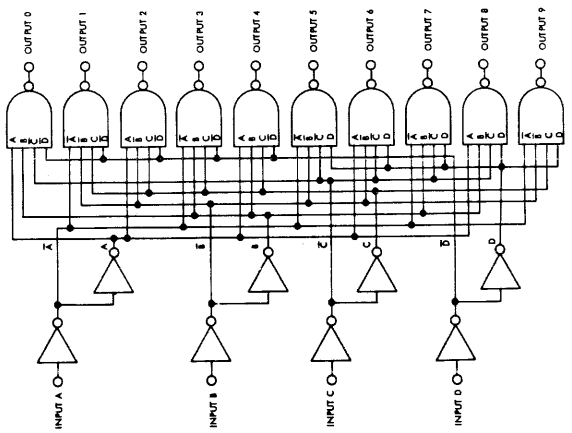
§ Not more than one output should be shorted at a time.

9

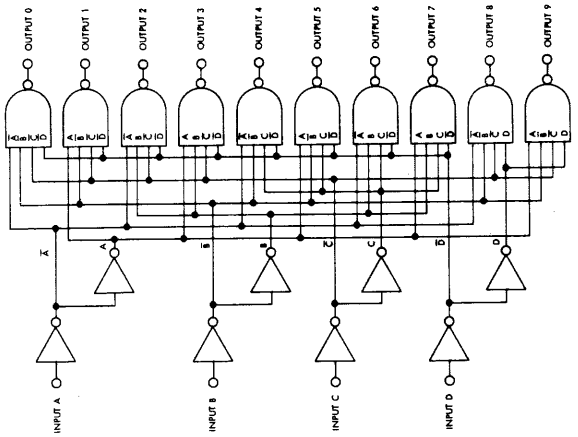
functional block diagrams



SN54L44/SN74L44 EXCESS-3-GRAY-TO-DECIMAL



SN54L43/SN74L43 EXCESS-3-TO-DECIMAL



SN54L42/SN74L42 BCD-TO-DECIMAL

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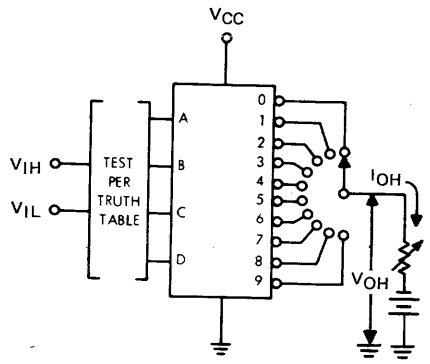
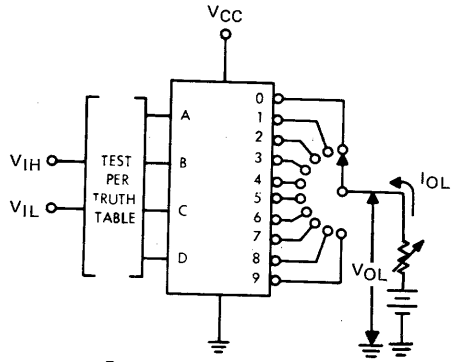
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



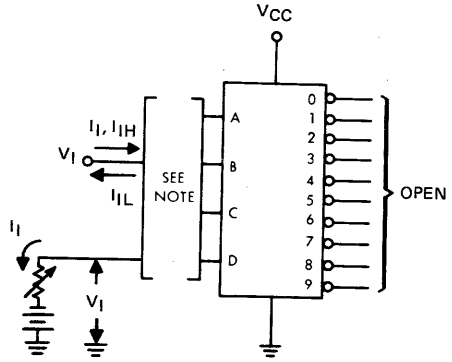
Each output is tested separately.

FIGURE 1–V_{IH}, V_{IL}, V_{OH}



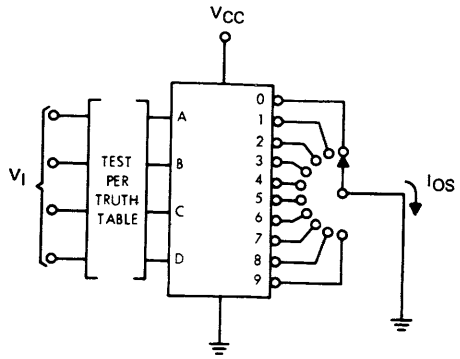
Each output is tested separately.

FIGURE 2–V_{IH}, V_{IL}, V_{OL}



Each input is tested separately for V_I, I_I, I_{IH}, and I_{IL}. Inputs not under test are grounded.

FIGURE 3–V_I, I_I, I_{IH}, I_{IL}



Each output is tested separately.

FIGURE 4–I_{OS}

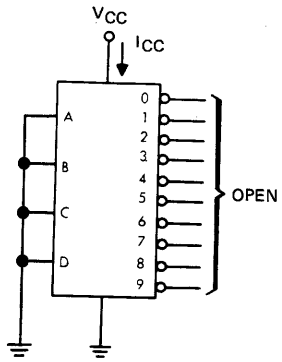
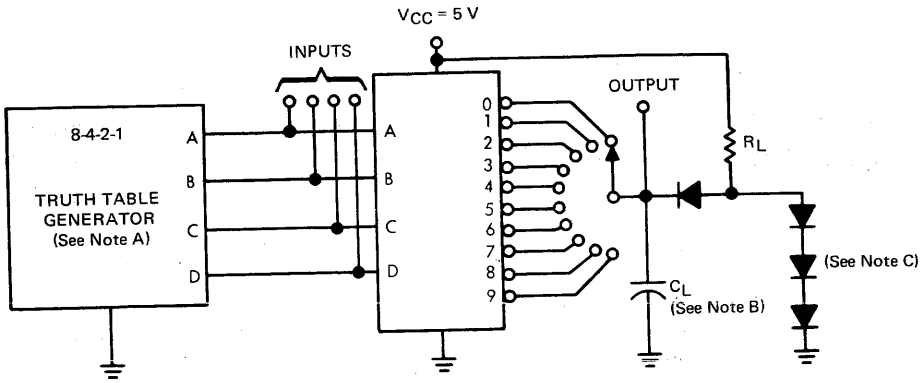


FIGURE 5–I_{CC}

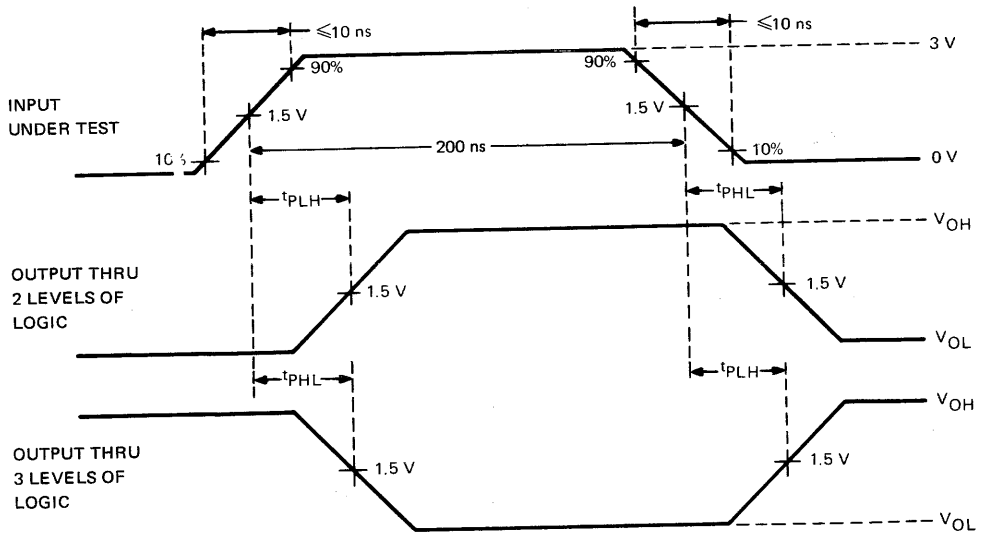
† Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The truth table generator has the following characteristics: PRR ≤ 1 MHz, $Z_{out} \approx 50\ \Omega$. Transition of the input under test must occur simultaneously with or following the transition of the other inputs.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N914.

FIGURE 6–SWITCHING TIMES

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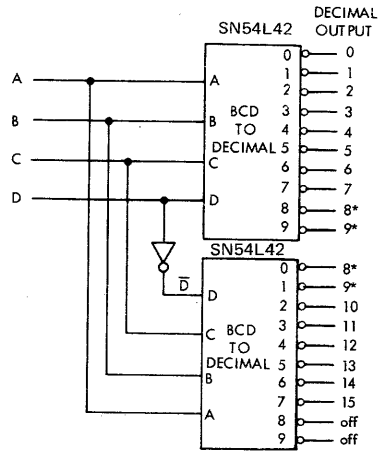
TYPICAL APPLICATIONS

decoding binary-to-decimal with SN54L42/SN74L42

Figure A demonstrates a method for utilizing two SN54L42/SN74L42 decoders to perform 4-wire-to-16-wire (1-of-16) decoding. Inputs A, B, and C of the two decoders are paralleled, D is applied to one decoder, and $\overline{D}$ is applied to the other. Decimal equivalents are available as indicated. Note that decimal 8 and 9 are available from both decoders.



*These decimal outputs are available from both decoders.

FIGURE A

decoding 3-wire binary-to-octal

Figure B demonstrates a method for decoding 3-wire binary-to-octal using the SN54L42/SN74L42. The binary code ABC is applied to the A, B, and C inputs and the D input is used as a strobe. When the strobe is taken to a low level, the octal data may be taken from outputs 0 through 7. Note that decimal outputs 8 and 9 are not used. See BCD truth table.

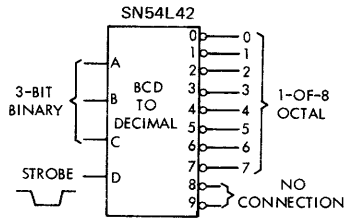


FIGURE B

Figure C demonstrates a method for decoding 3-wire binary-to-octal using the SN54L44/SN74L44. The binary code ABC is applied to the A, B, and D inputs, respectively, and the C input is used as a strobe. When the strobe is taken to a high level, the octal data (as identified in figure C) may be taken from outputs 1 through 8. Note that outputs 0 and 9 are not used.

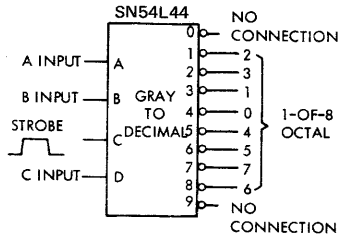


FIGURE C

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TEXAS INSTRUMENTS
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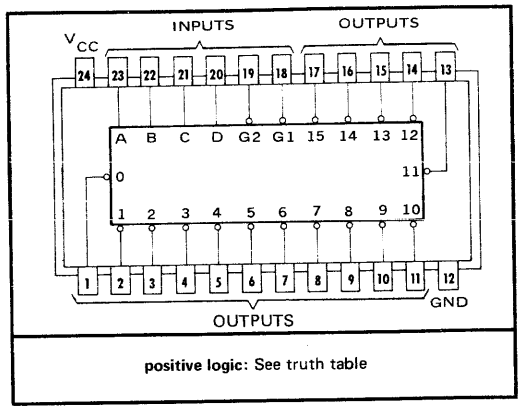
CIRCUIT TYPES SN54154, SN74154
4-LINE-TO-16-LINE DECODERS/DEMULTIPLEXERS

FOR APPLICATIONS IN COMMUNICATIONS EQUIPMENT,
COMPUTERS, AND ELECTRONIC INSTRUMENTATION

- Decodes 4 binary-coded inputs into one of 16 mutually exclusive outputs
- Performs the demultiplexing function by distributing data from one input line to any one of 16 outputs
- Input clamping diodes simplify system design
- High fan-out, low-impedance, totem-pole outputs
- Typical average propagation delay times:
  23 ns through 3 levels of logic
  19 ns from strobe input
- Typical power dissipation . . . 170 mW
- Fully compatible with most TTL, DTL, and MSI circuits

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



†Pin assignments for these circuits are the same for all packages.

description

Each of these monolithic, 4-line-to-16-line decoders utilizes TTL circuitry to decode four binary-coded inputs into one of sixteen mutually exclusive outputs when both the strobe inputs, G1 and G2, are low. The demultiplexing function is performed by using the 4 input lines to address the output line, passing data from one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high.

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These circuits are fully compatible for use with most other TTL and DTL circuits. Input clamping diodes are provided to minimize transmission-line effects and thereby simplify system design. Input buffers are used to lower the fan-in requirement to only one normalized Series 54/74 load. A fan-out to 10 normalized Series 54/74 loads in the low-level state and 20 in the high-level state is available from each of the sixteen outputs. Typical power dissipation is 170 mW.

The SN54154 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74154 is characterized for operation from 0°C to 70°C.

TEXAS INSTRUMENTS
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logic

TRUTH TABLE

INPUTS						OUTPUTS														
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = high, L = low, X = irrelevant

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: SN54154 Circuits . . . . . −55°C to 125°C
SN74154 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

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recommended operating conditions

		SN54154			SN74154			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Operating free-air temperature range		−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage	1 and 2			2			V
V_{IL}	Low-level input voltage	1 and 2					0.8	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4			V
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA				0.4	V
I_{IH}	High-level input current (each input)	3	V_{CC} = MAX, V_I = 2.4 V				40	μA
			V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IL}	Low-level input current (each input)	3	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
I_{OS}	Short-circuit output current§	4	V_{CC} = MAX	SN54154	−20		−55	mA
				SN74154	−18		−57	
I_{CC}	Supply current	5	V_{CC} = MAX	SN54154		34	49	mA
				SN74154		34	56	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output, from A, B, C, or D inputs through 3 levels of logic	6	C_L = 15 pF, R_L = 400 Ω		24	36	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from A, B, C, or D inputs through 3 levels of logic				22	33	ns
t_{PLH}	Propagation delay time, low-to-high-level output, from either strobe input				20	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from either strobe input				18	27	ns

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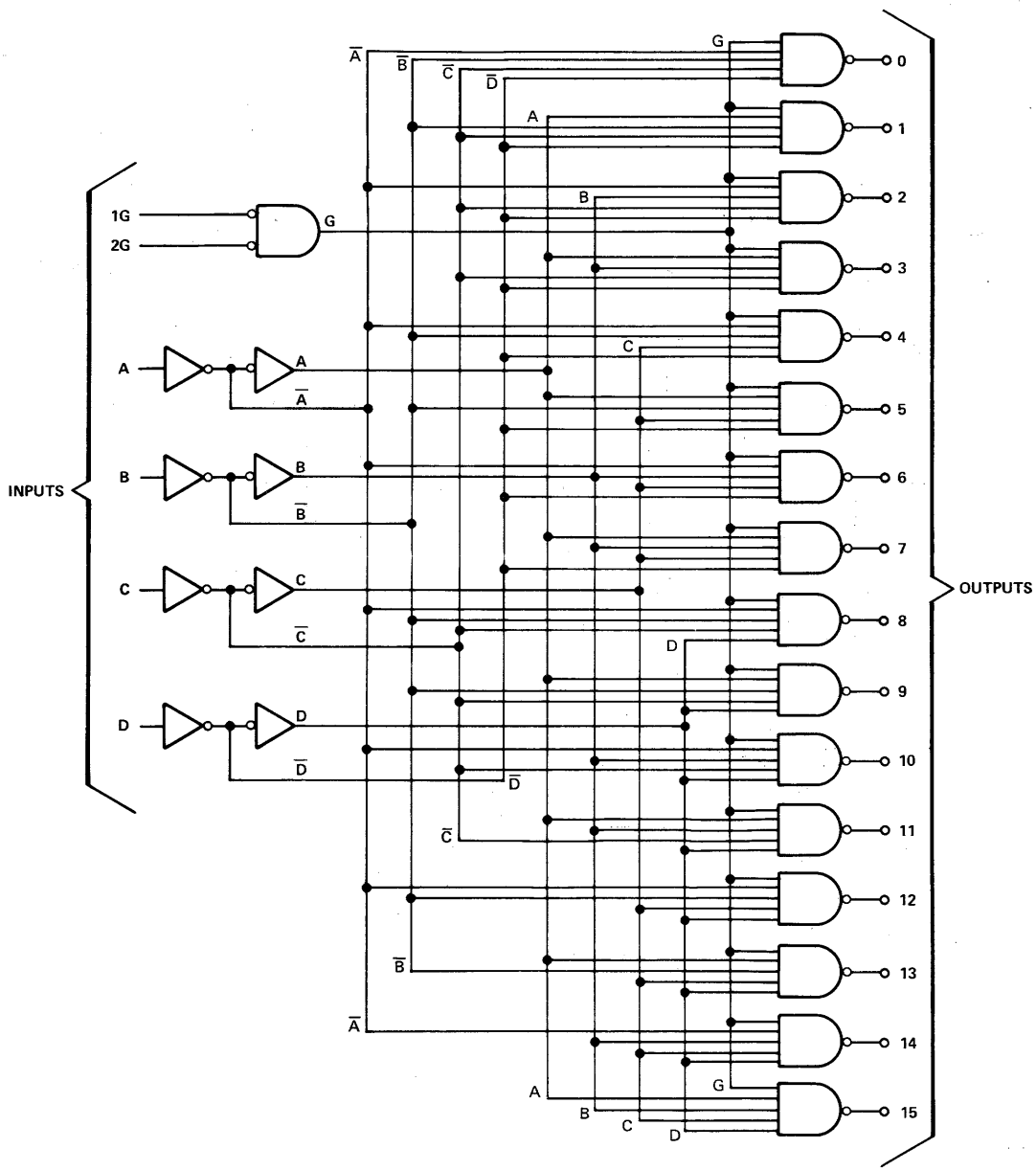
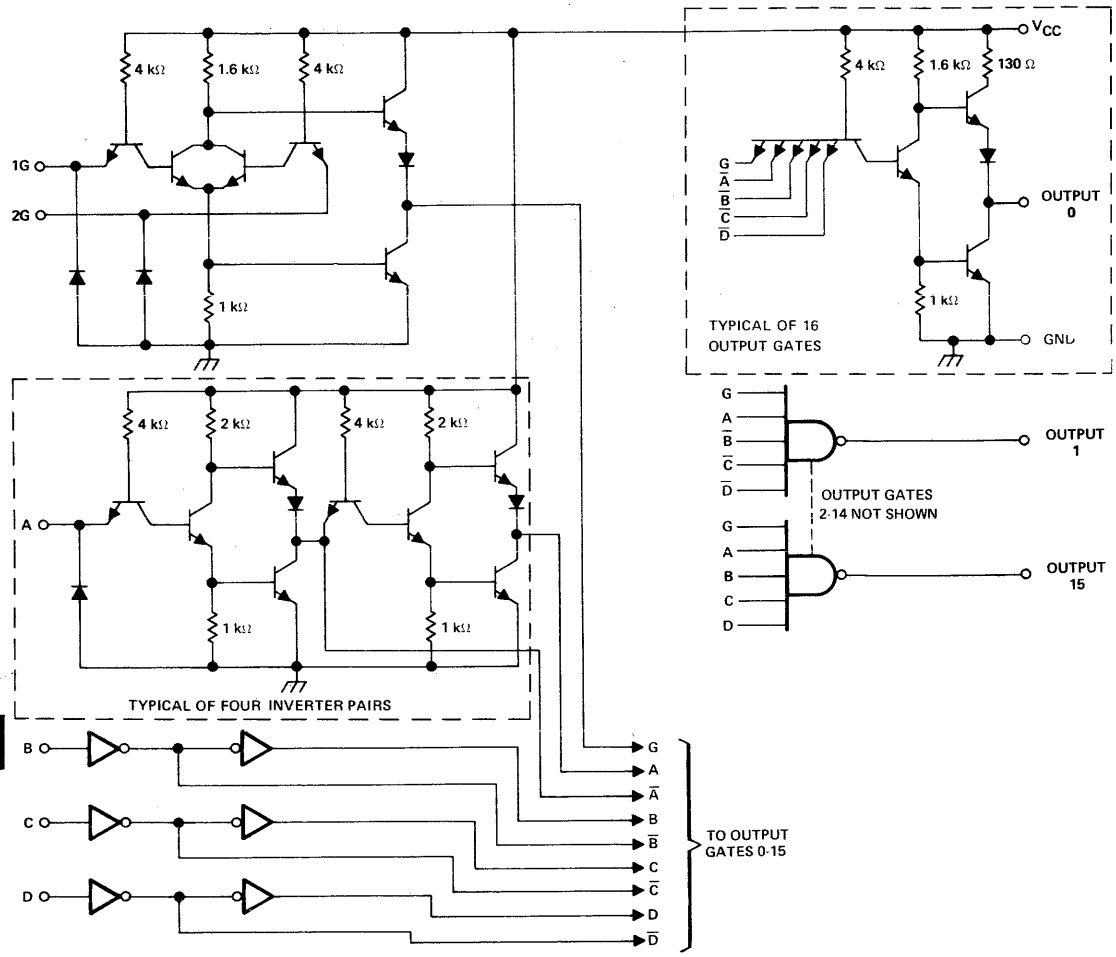
functional block diagram



schematic



Component values shown are nominal.

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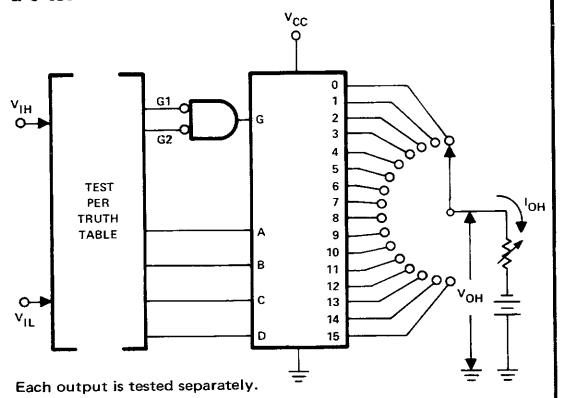
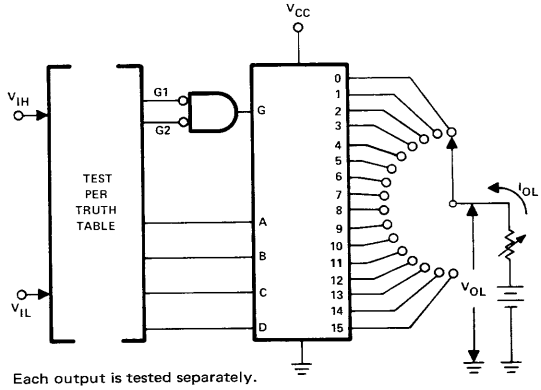
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



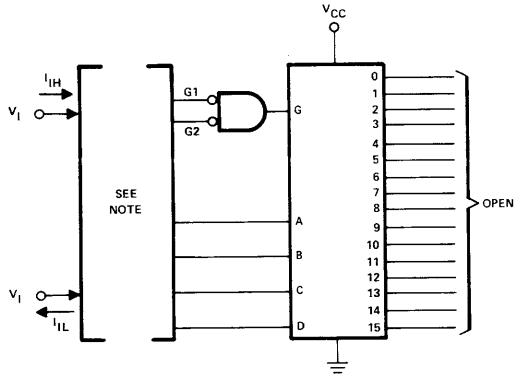
Each output is tested separately.

FIGURE 1–V_{IH}, V_{IL}, V_{OH}



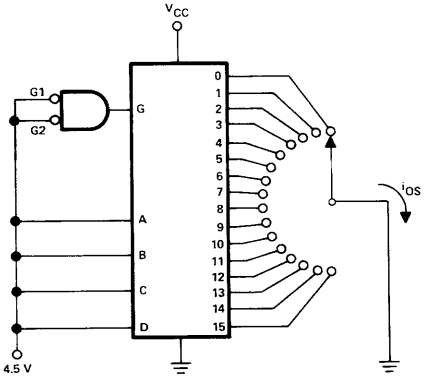
Each output is tested separately.

FIGURE 2–V_{IH}, V_{IL}, V_{OL}



Each input is tested separately for both I_{IH} and I_{IL}. Inputs not under test are grounded, with the exception that when testing I_{IL} of a strobe input, the other strobe is at 2.4 V.

FIGURE 3–I_{IH}, I_{IL}



Each output is tested separately.

FIGURE 4–I_{OS}

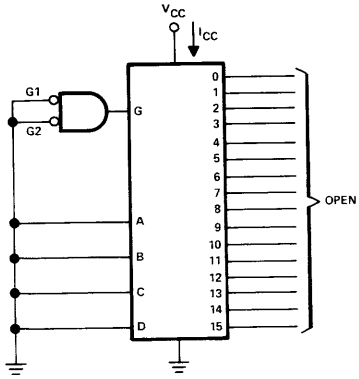


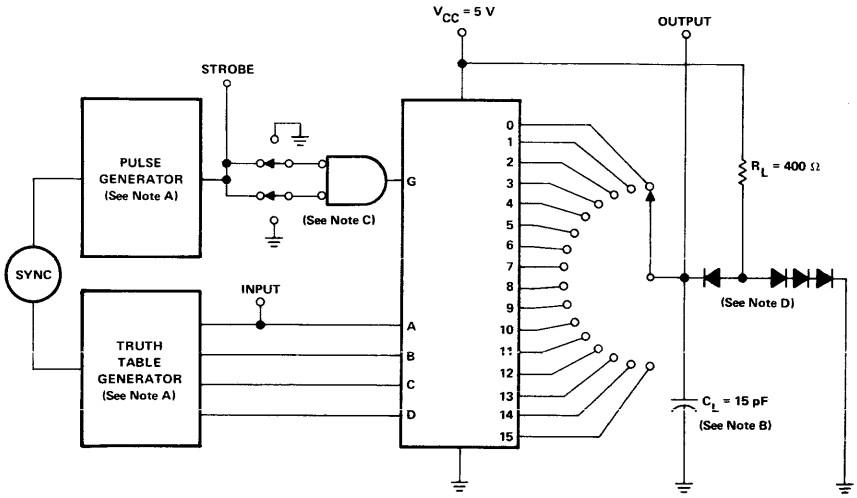
FIGURE 5–I_{CC}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

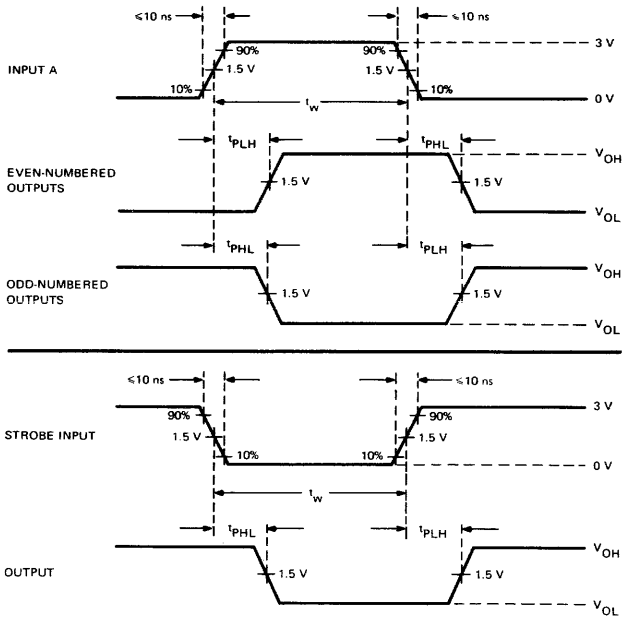
9

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The truth table generator and the pulse generator have the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$, t_w = 100 ns.
B. C_L includes probe and jig capacitance.
C. When measuring select-input-to-output times the strobe inputs are grounded. When measuring strobe-input-to-output times, the untested strobe input is grounded. Select inputs determine output under test through truth table generator.
D. All diodes are 1N3064.

FIGURE 6–SWITCHING TIMES

TEXAS INSTRUMENTS
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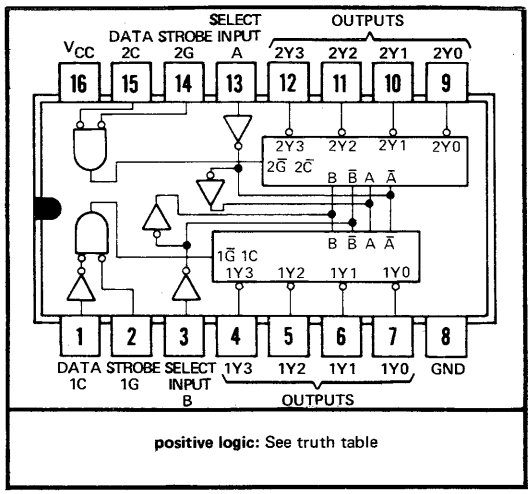
CIRCUIT TYPES SN54155, SN54156, SN74155, SN74156
DUAL 2-LINE-TO-4-LINE DECODERS/DEMULTIPLEXERS

CIRCUIT TYPES SN54155, SN54156, SN74155, SN74156
BULLETIN NO. DL-S 7011308, FEBRUARY 1970

- Applications:
  - Dual 2-to-4-Line Decoder
  - Dual 1-to-4-Line Demultiplexer
  - 3-to-8-Line Decoder
  - 1-to-8-Line Demultiplexer
- Individual Strobes Simplify Cascading for Decoding or Demultiplexing Larger Words
- Input Clamping Diodes Simplify System Design
- Choice of Outputs:
  - Totem Pole (SN54155, SN74155)
  - Open-Collector (SN54156, SN74156)
- Typical Average Propagation Delay Times:
  - 16 ns through 2 levels of logic
  - 21 ns through 3 levels of logic
- Typical Power Dissipation . . . 125 mW

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



†Pin assignments for these circuits are the same for all packages.

description

These monolithic transistor-transistor-logic (TTL) circuits feature dual 1-line-to-4-line demultiplexers with individual strobes and common binary-address inputs in a single 16-pin package. When both sections are enabled by the strobes, the common binary-address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input 1C is inverted at its outputs and data applied at 2C is not inverted through its outputs. The inverter following the 1C data input permits use as a 3-to-8-line decoder or 1-to-8-line demultiplexer without external gating. See typical applications data and the truth tables for more details.

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The SN54155/SN74155 circuits, with totem-pole outputs, are rated to fan-out to 10 normalized Series 54/74 loads in the low-level output state, and to 20 loads in the high-level output state. The SN54156/SN74156 circuits, with open-collector outputs, are rated to sink 16 milliamperes at a low-level output voltage of less than 0.4 volt. Input-clamping diodes are provided on all of these circuits to minimize transmission-line effects and simplify system design. Typical power dissipation is 125 milliwatts. Typical average propagation delay times are 16 nanoseconds through 2 levels of logic and 21 nanoseconds through 3 levels of logic for the SN54155/SN74155.

The SN54155 and SN54156 are characterized for operation over the full military temperature range of −55°C to 125°C; the SN74155 and SN74156 are characterized for operation from 0°C to 70°C.

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truth tables (H = high level, L = low level, X = irrelevant)

2-LINE-TO-4-LINE DECODER OR 1-LINE-TO-4-LINE DEMULTIPLEXER

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	1G	1C	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	2G	2C	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

3-LINE-TO-8-LINE DECODER TO 1-LINE-TO-8-LINE DEMULTIPLEXER

INPUTS				OUTPUTS							
SELECT			STROBE OR DATA	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C†	B	A	G‡	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

†C = inputs 1C and 2C connected together
‡G = inputs 1G and 2G connected together

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: SN54155, SN54156 Circuits . . . . . −55°C to 125°C
SN74155, SN74156 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54155			SN74155			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Operating free-air temperature range, T_A		−55	25	125	0	25	70	°C

	SN54156			SN74156			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature range, T_A	−55	25	125	0	25	70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		SN54155, SN74155 MIN	SN54155, SN74155 TYP‡	SN54155, SN74155 MAX	UNIT
V_{IH}	High-level input voltage	1 and 2			2			V
V_{IL}	Low-level input voltage	1 and 2					0.8	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, V_{IH} = 2 V, I_{OH} = −800 μA		2.4			V
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 16 mA				0.4	V
I_{IH}	High-level input current (each input)	4	V_{CC} = MAX, V_I = 2.4 V				40	μA
			V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IL}	Low-level input current (each input)	4	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
I_{OS}	Short-circuit output current§	5	V_{CC} = MAX	SN54155	−20		−55	mA
				SN74155	−18		−57	
I_{CC}	Supply current	6	V_{CC} = MAX	SN54155		25	35	mA
				SN74155		25	40	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		SN54156, SN74156 MIN	SN54156, SN74156 TYP‡	SN54156, SN74156 MAX	UNIT
V_{IH}	High-level input voltage	2 and 3			2			V
V_{IL}	Low-level input voltage	2					0.8	V
I_{OH}	High-level output current	3	V_{CC} = MIN, V_I = 2 V, V_{OH} = 5.5 V				250	μA
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 16 mA				0.4	V
I_{IH}	High-level input current (each input)	4	V_{CC} = MAX, V_I = 2.4 V				40	μA
			V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IL}	Low-level input current (each input)	4	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
I_{CC}	Supply current	6	V_{CC} = MAX	SN54156		25	35	mA
				SN74156		25	40	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

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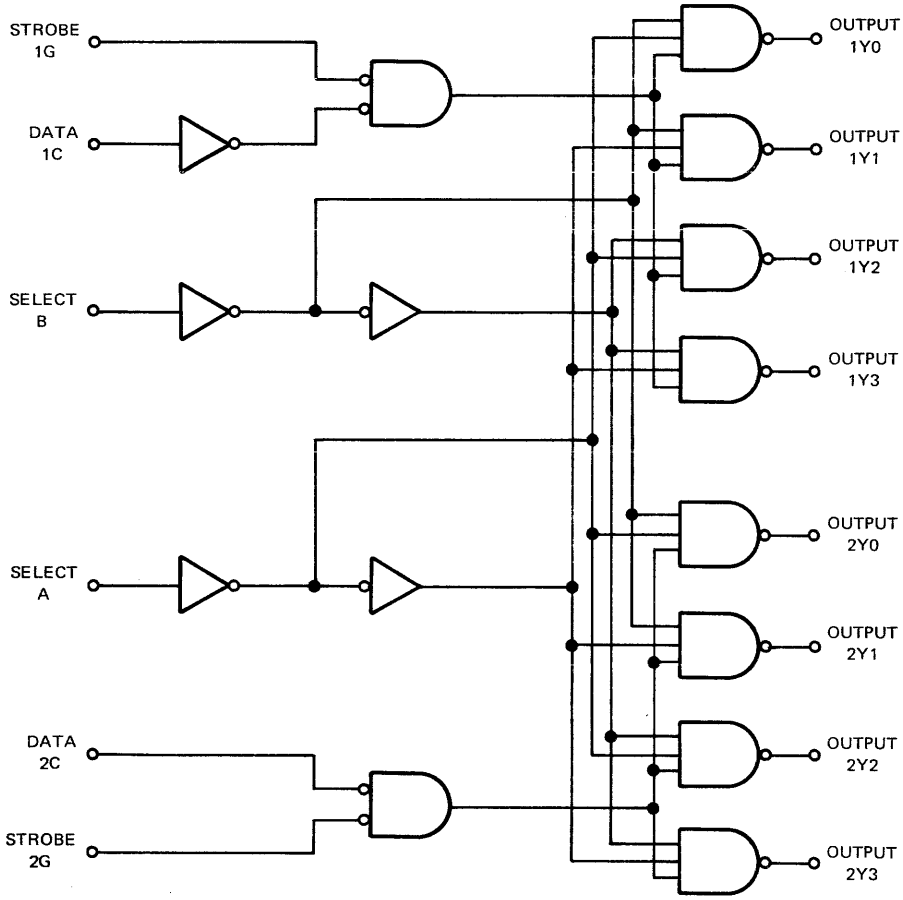
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	LEVELS OF LOGIC	TEST FIGURE	TEST CONDITIONS	SN54155 SN74155 MIN	SN54155 SN74155 TYP	SN54155 SN74155 MAX	SN54156 SN74156 MIN	SN54156 SN74156 TYP	SN54156 SN74156 MAX	UNIT
t_{PLH}	A, B, 2C, 1G, or 2G	Y	2	7	C_L = 15 pF, R_L = 400 Ω		13	20		15	23	ns
t_{PHL}	A, B, 2C, 1G, or 2G	Y	2				18	27		20	30	ns
t_{PLH}	A or B	Y	3				21	32		23	34	ns
t_{PHL}	A or B	Y	3				21	32		23	34	ns
t_{PLH}	1C	Y	3				16	24		18	27	ns
t_{PHL}	1C	Y	3				20	30		22	33	ns

¶t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output

functional block diagram



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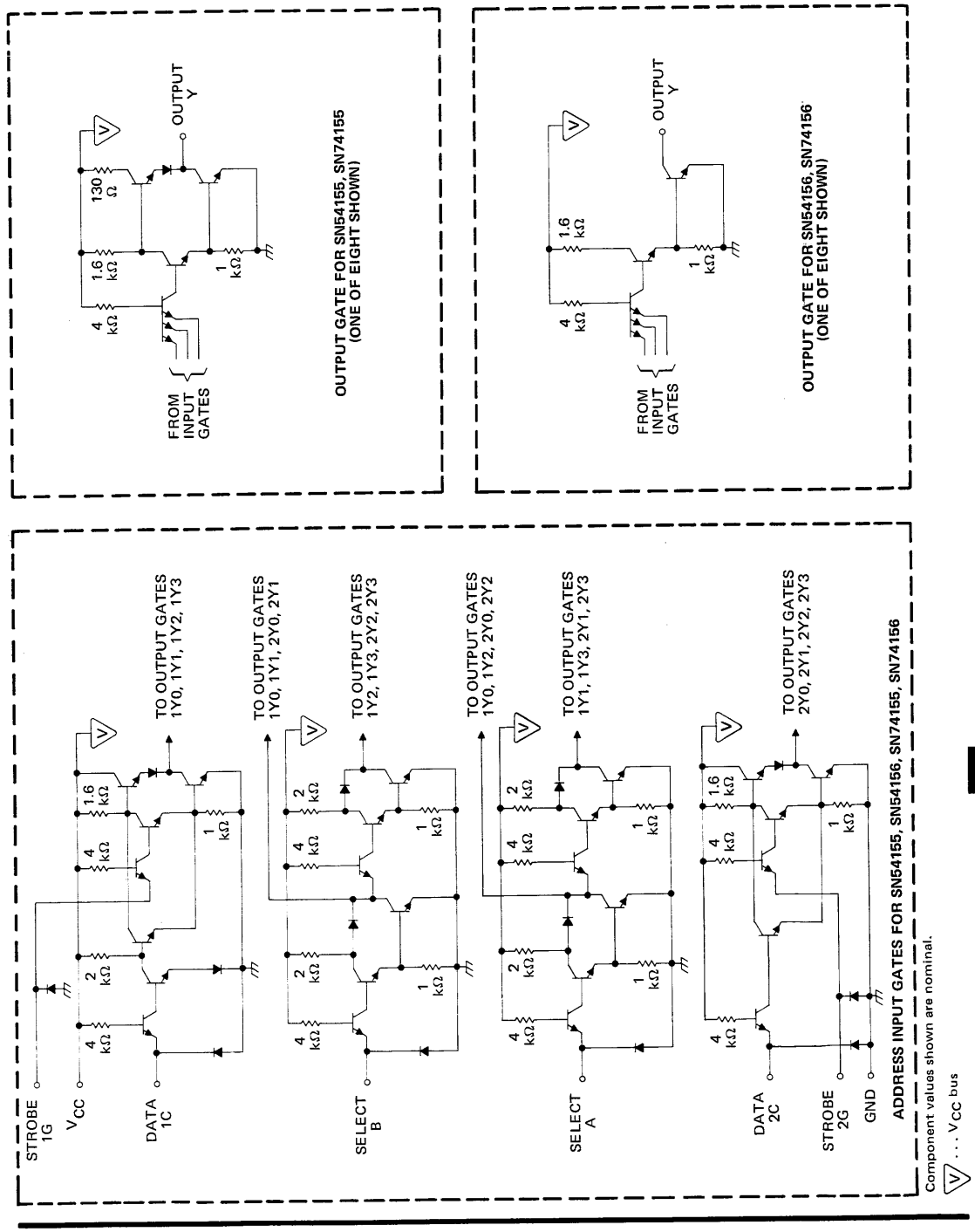
schematic


OUTPUT GATE FOR SN54155, SN74155
(ONE OF EIGHT SHOWN)
OUTPUT Y
130 Ω
1.6 kΩ
4 kΩ
1 kΩ
FROM INPUT GATES
OUTPUT GATE FOR SN54156, SN74156
(ONE OF EIGHT SHOWN)
ADDRESS INPUT GATES FOR SN54155, SN54156, SN74155, SN74156
TO OUTPUT GATES 1Y0, 1Y1, 1Y2, 1Y3
TO OUTPUT GATES 1Y0, 1Y1, 2Y0, 2Y1
TO OUTPUT GATES 1Y2, 1Y3, 2Y2, 2Y3
TO OUTPUT GATES 1Y0, 1Y2, 2Y0, 2Y2
TO OUTPUT GATES 1Y1, 1Y3, 2Y1, 2Y3
TO OUTPUT GATES 2Y0, 2Y1, 2Y2, 2Y3
2 kΩ
STROBE 1G
VCC
DATA 1C
SELECT B
SELECT A
DATA 2C
STROBE 2G
GND
Component values shown are nominal.
. . . VCC bus

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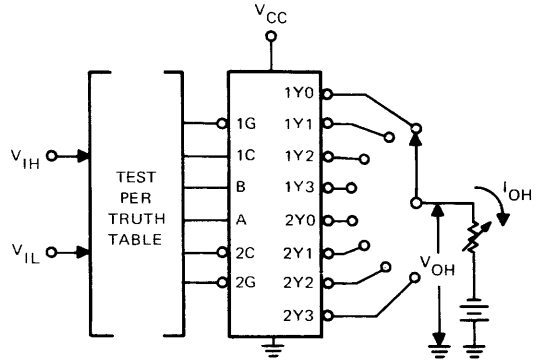
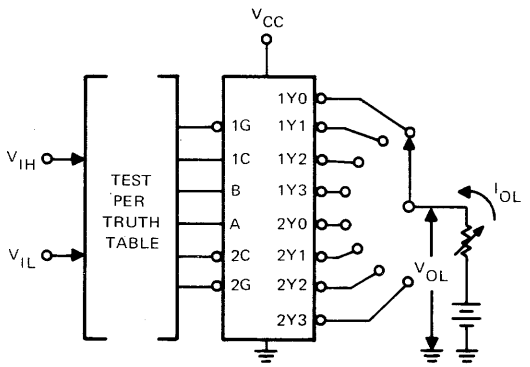
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



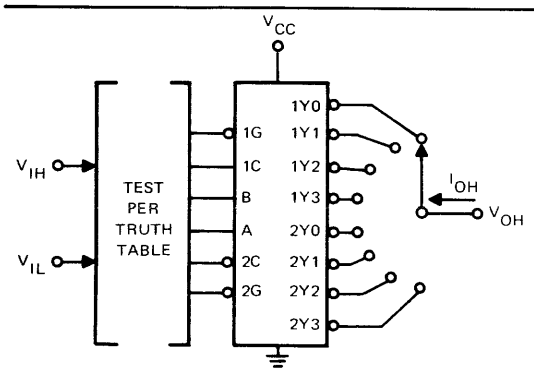
Each output is tested separately.

FIGURE 1–V_{IH}, V_{IL}, V_{OH}



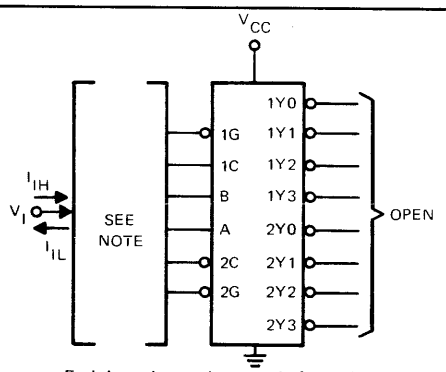
Each output is tested separately.

FIGURE 2–V_{IH}, V_{IL}, V_{OL}



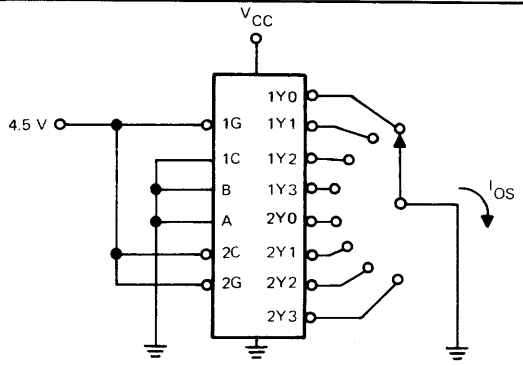
Each output is tested separately.

FIGURE 3–V_{IH}, V_{IL}, I_{OH}



Each input is tested separately for both I_{IH} and I_{IL}. Inputs not under test are grounded.

FIGURE 4–I_{IH}, I_{IL}



Each output is tested separately.

FIGURE 5–I_{OS}

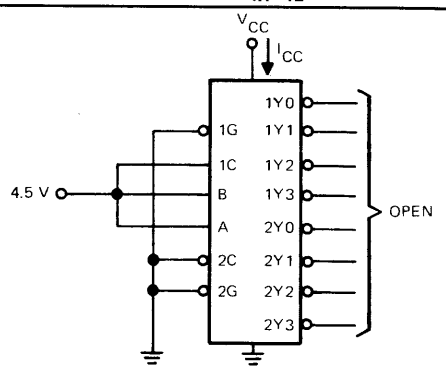


FIGURE 6–I_{CC}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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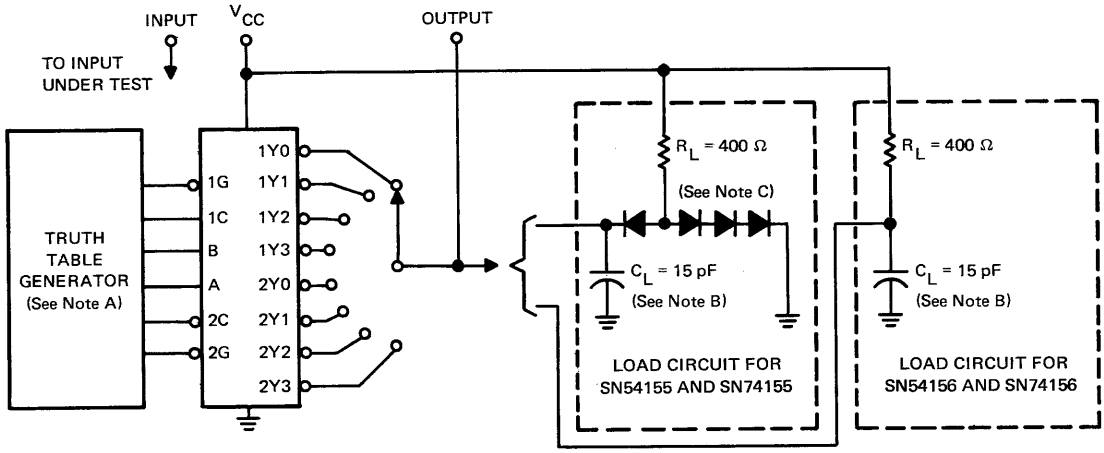
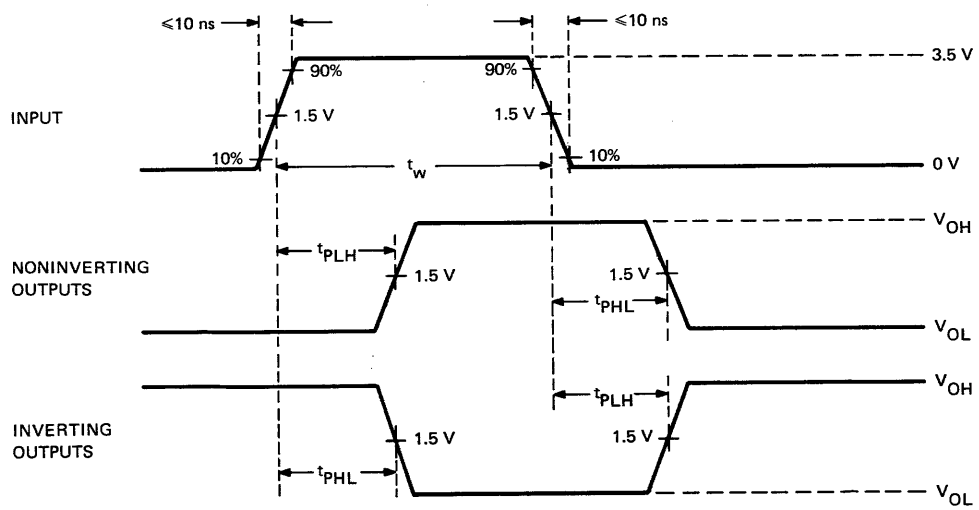
PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The truth table generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$, t_w = 100 ns.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.

FIGURE 7–PROPAGATION DELAY TIME

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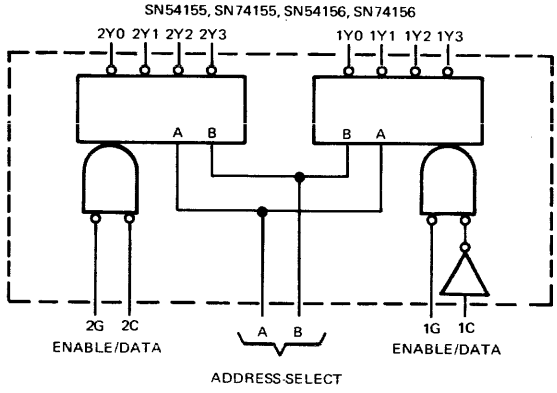
TYPICAL APPLICATION DATA

THE SN54155, SN74155, SN54156, or SN74156 may be used as a dual 2-line-to-4-line decoder or a 1-line-to-4-line demultiplexer. These applications are identical except as follows:

When decoding, the 2-line code is applied to select inputs A and B. The 4-line output section (1Y0, 1Y1, 1Y2, 1Y3) is enabled by taking strobe 1G low and input 1C high. The other 4-line output section (2Y0, 2Y1, 2Y2, 2Y3) is enabled by taking both strobe 2G and input 2C low. Note that the separate enable lines permit the user complete flexibility in decoding at either or both of the output sections. The strobe also permits cascading and allows disabling of the circuits until the addressing transients have passed.

When demultiplexing, the serial data is applied to the data inputs 1C and 2C and distribution to the outputs is controlled by the A and B select inputs. Again, the separate strobe inputs, 1G and 2G, permit demultiplexing to occur at either or both output sections, and cascading.

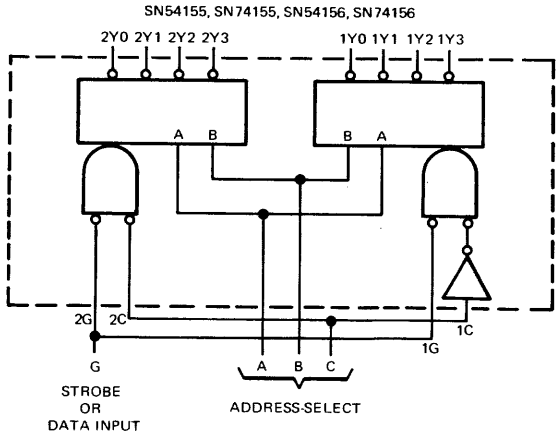


DUAL 2-LINE-TO-4-LINE DECODER/1-TO-4-LINE DEMULTIPLEXER

Any of these circuits may also be used as a 3-line-to-8-line decoder or a 1-line-to-8-line demultiplexer.

When used as a decoder, data inputs 1C and 2C are connected together and serve as the third (C) select line. The strobes are also connected together and are used for enabling and/or cascading.

When used as a demultiplexer, the common strobe line serves as the data input.



3-LINE-TO-8-LINE DECODER/1-TO-8-LINE DEMULTIPLEXER

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CIRCUIT TYPES SN5445, SN54145, SN7445, SN74145
BCD-TO-DECIMAL DECODER/DRIVERS

TTL MSI LAMP, LOGIC, OR MOS DRIVERS

featuring

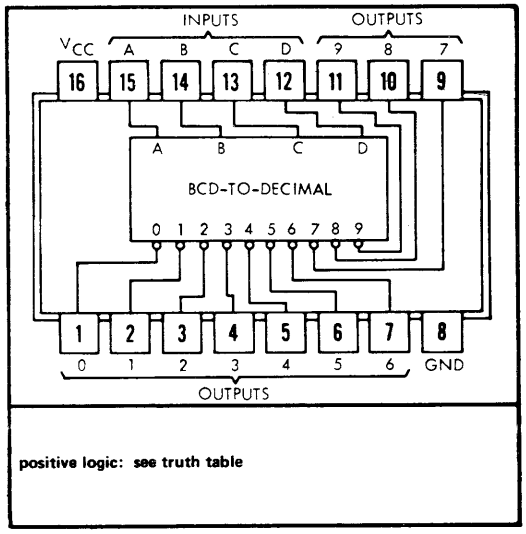
- Full Decoding of Input Logic
- 80 mA Sink-Current Capability

logic

TRUTH TABLE

INPUTS				OUTPUTS								
D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
0	1	1	1	1	1	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
1	0	1	0	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)†



†Pin assignments for these circuits are the same for all packages.

description

These monolithic BCD-to-decimal decoder/drivers consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid BCD input logic ensures that all outputs remain off for all invalid binary input conditions. These decoders feature TTL inputs and high-performance, n-p-n output transistors designed for use as indicator/relay drivers or as open-collector logic-circuit drivers. Each of the high-breakdown output transistors (SN5445, SN7445 = 30 volts and SN54145, SN74145 = 15 volts) will sink up to 80 milliamperes of current. Each input is one normalized Series 54/74 load. Inputs and outputs are entirely compatible for use with TTL or DTL logic circuits, and the outputs are compatible for interfacing with most MOS integrated circuits. Power dissipation is typically 215 milliwatts.

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1) . . . . . 7 V
Input Voltage, V_{in} (See Note 1) . . . . . 5.5 V
Maximum Current into each Output (See Note 2) . . . . . 1 mA
Operating Free-Air Temperature Range: SN5445, SN54145 Circuits . . . . . −55°C to 125°C
SN7445, SN74145 Circuits . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

NOTES: 1. These voltage values are with respect to network ground terminal.
2. This rating applies when the output is off.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1): SN5445, SN54145 Circuits	4.5	5	5.5	V
SN7445, SN74145 Circuits	4.75	5	5.25	V
Voltage on any Output (See Note 2): SN5445, SN7445 Circuits			30	V
SN54145, SN74145 Circuits			15	V

electrical characteristics over recommended operating temperature range (unless otherwise noted)

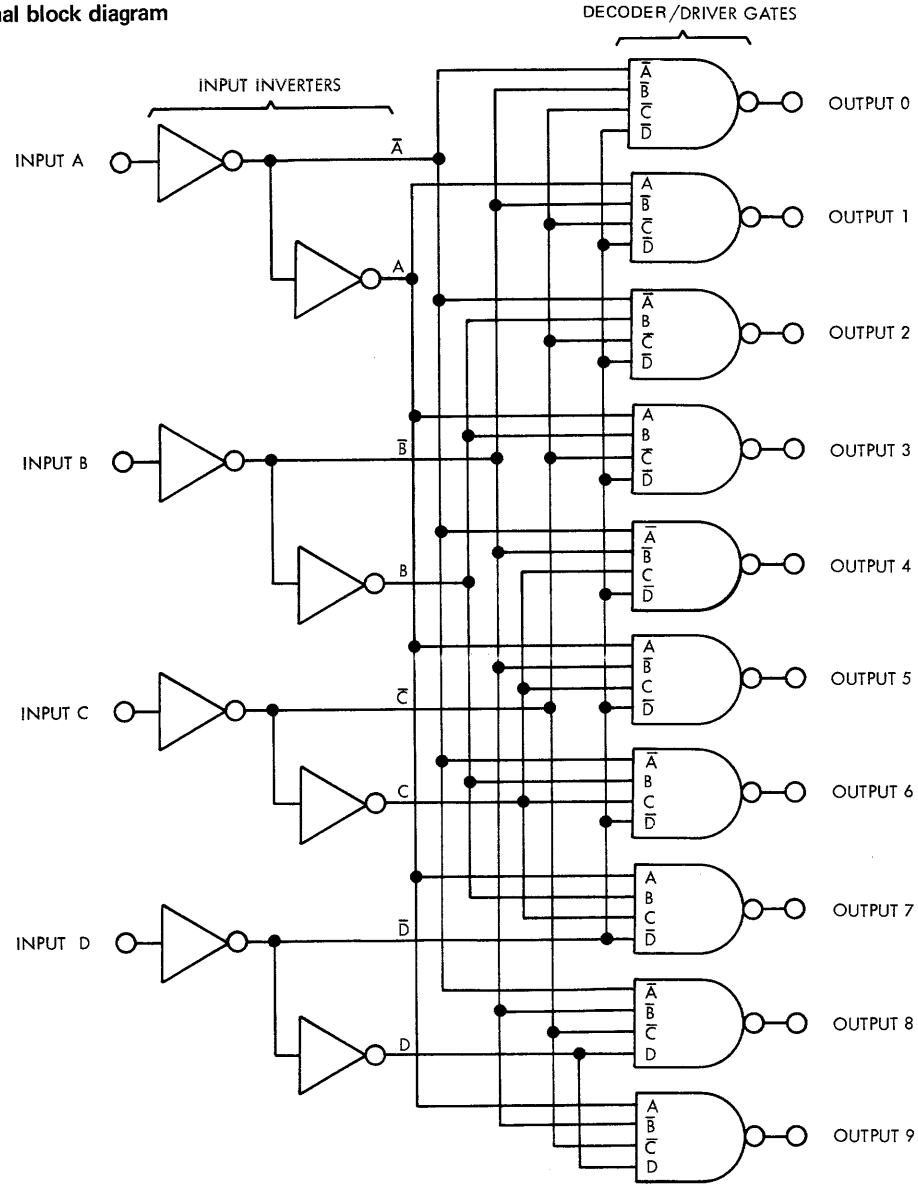
PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1 and 2			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	1 and 2					0.8	V
V_{on}	On-state output voltage	1	V_{CC} = MIN, I_{sink} = 80 mA			0.5	0.9	V
			V_{CC} = MIN, I_{sink} = 20 mA				0.4	V
V_{off}	Off-state output voltage (SN5445 or SN7445)	2	V_{CC} = MAX, I_{off} = 250 μA		30			V
V_{off}	Off-state output voltage (SN54145 or SN74145)	2	V_{CC} = MAX, I_{off} = 250 μA		15			V
$I_{in(1)}$	Logical 1 level input current (each input)	3	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(0)}$	Logical 0 level input current (each input)	4	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
I_{CC}	Supply current	4	V_{CC} = MAX	SN5445, SN54145		43	62	mA
				SN7445, SN74145		43	70	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C

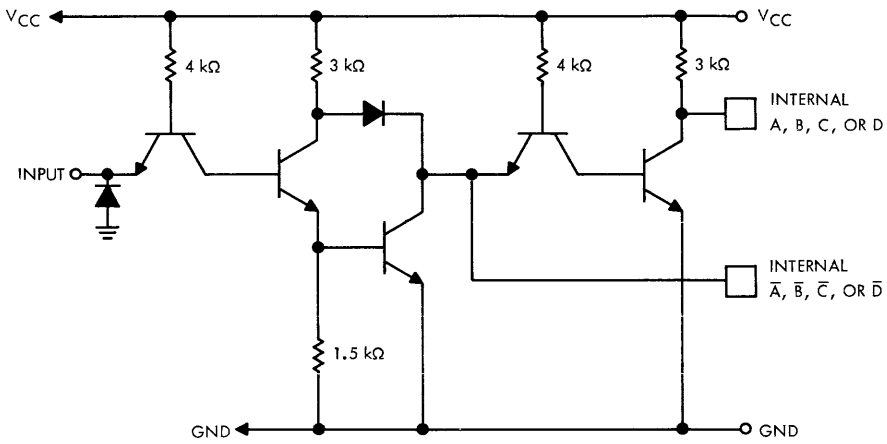
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd1}	Propagation delay time to logical 1 level	5	C_L = 15 pF, R_L = 100 Ω			50	ns
t_{pd0}	Propagation delay time to logical 0 level	5	C_L = 15 pF, R_L = 100 Ω			50	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

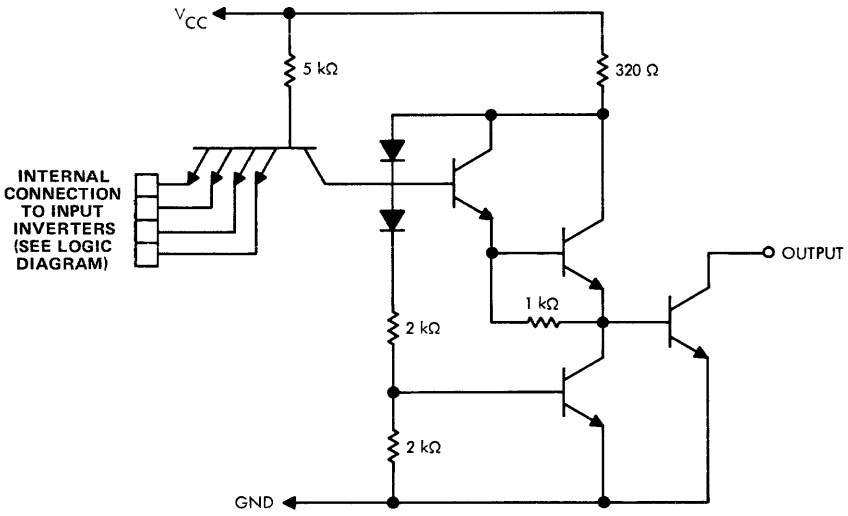
functional block diagram



schematic



EACH PAIR OF INPUT INVERTERS

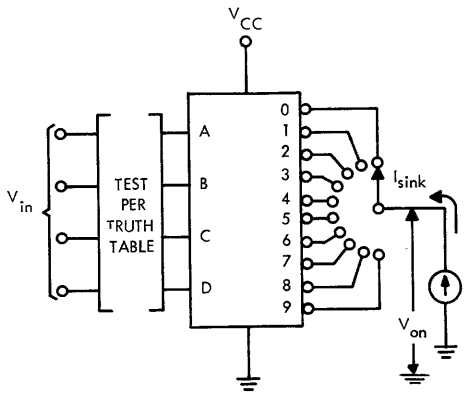


EACH DECODER/DRIVER GATE

NOTE: 1. Component values shown are nominal.

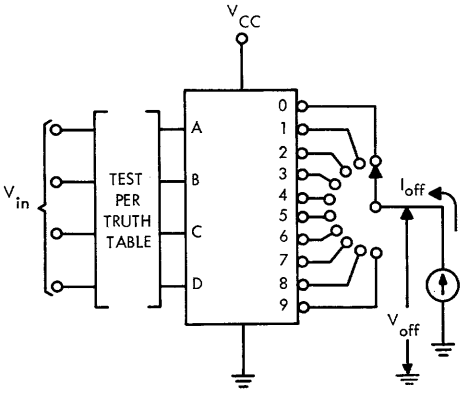
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



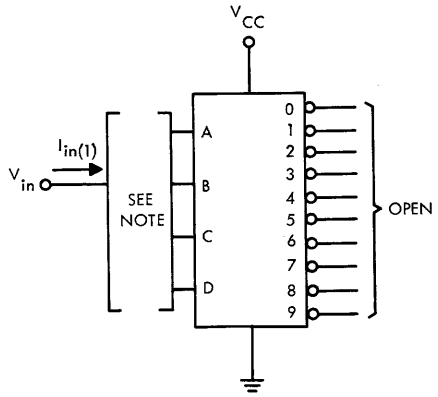
1. Each output is tested separately in the ON state.

FIGURE 1



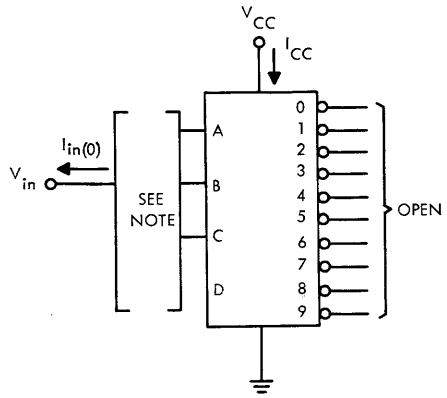
1. Each output is tested separately in the OFF state.

FIGURE 2



1. Each input is tested separately.

FIGURE 3



1. When testing $I_{in(0)}$ each input is tested separately.
2. When testing I_{CC} all inputs are grounded and outputs are open.

FIGURE 4

† Arrows indicate actual direction of current flow

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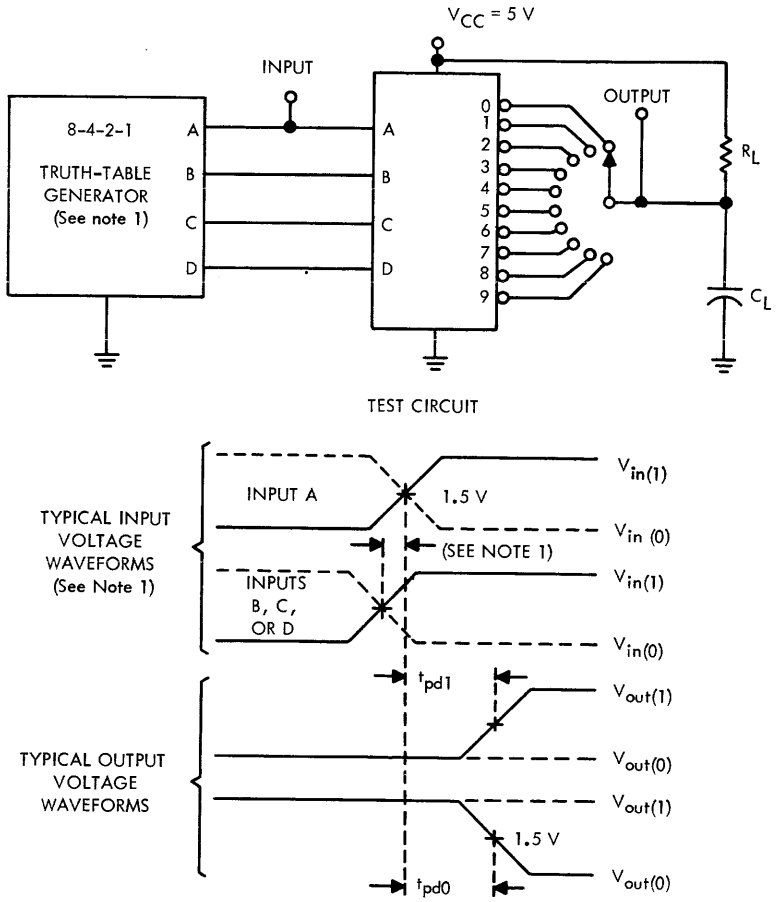
PARAMETER MEASUREMENT INFORMATION

switching characteristics



NOTES: 1. The truth-table generator has the following characteristics: $V_{out(1)} \geq 2.4$ V, $V_{out(0)} \leq 0.4$ V, t_r and $t_f < 10$ ns, and PRR = 1 MHz. Inputs B, C, and D transitions occur simultaneously with or prior to input A transitions.
2. C_L includes probe and jig capacitance.

FIGURE 5-SWITCHING TIMES

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TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN5446A, SN5447A, SN5448, SN5449
SN7446A, SN7447A, SN7448, SN7449
BCD-TO-SEVEN-SEGMENT DECODER/DRIVERS

SN5446A, SN5447A, SN7446A, SN7447A
featuring

- DIRECT DRIVE FOR INDICATORS
- OPEN-COLLECTOR OUTPUTS
- LAMP-TEST PROVISION
- LEADING/TRAILING ZERO SUPPRESSION
- CERAMIC OR PLASTIC DUAL-IN-LINE PACKAGES

SN5448, SN7448
featuring

- PASSIVE PULL-UP OUTPUTS
- LAMP-TEST PROVISION
- LEADING/TRAILING ZERO SUPPRESSION
- CERAMIC OR PLASTIC DUAL-IN-LINE PACKAGES

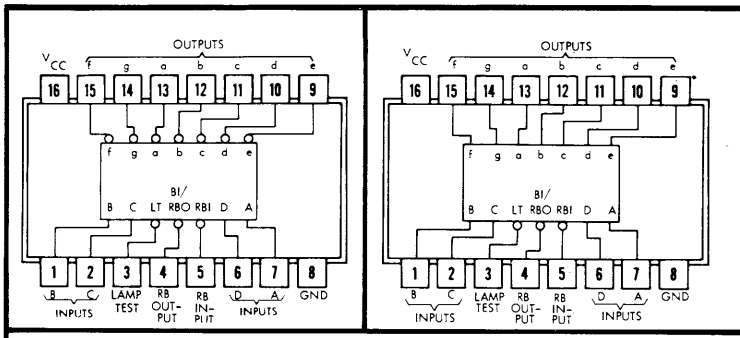
SN5449, SN7449
featuring

- OPEN-COLLECTOR OUTPUTS
- BLANKING INPUT
- WELDED FLAT PACKAGE

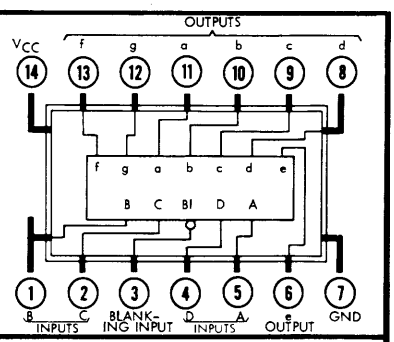
J OR N DUAL-IN-LINE OR W FLAT PACKAGE (TOP VIEW)†

SN5446A, SN5447A, SN7446A, SN7447A

SN5448, SN7448



SN5449, SN7449
W FLAT PACKAGE (TOP VIEW)



positive logic: see truth tables

†Pin assignments for these circuits are the same for all packages.

ALL CIRCUIT TYPES FEATURE:

- TTL-DTL COMPATIBILITY
- FULL DECODING OF ALL 16 INPUT COMBINATIONS
- LAMP INTENSITY MODULATION CAPABILITY

description

9

These monolithic, TTL, BCD-to-seven-segment decoder/drivers consist of NAND gates, input buffers, and seven AND-OR-INVERT gates. Three configurations offer active-low, high-sink-current outputs (SN5446A and SN5447A) for driving indicators directly; active-high, passive-pull-up outputs, (SN5448) and active-high, open-collector outputs (SN5449) for current-sourcing applications to drive logic circuits or discrete, active components. Seven NAND gates and one driver are connected in pairs to make BCD data and its complement available to the seven decoding AND-OR-INVERT gates, and the remaining NAND gate and three input buffers provide lamp test, blanking input/ripple-blanking output, and ripple-blanking input for the SN5446A, SN5447A and SN5448. Four NAND gates and four input buffers provide BCD data and its complement and a buffer provides blanking input for the SN5449. See functional block diagrams.

The circuits accept 4-bit binary-coded-decimal (BCD) and, depending on the state of the auxiliary inputs, decodes this data to drive a seven-segment display indicator (SN5446A and SN5447A) or other components (SN5448, SN5449). The relative positive-logic output levels, as well as conditions required at the auxiliary inputs, are shown in the truth tables. Output configurations of the SN5446A and SN5447A are designed to withstand the relatively high voltages required for seven segment indicators. The SN5446A outputs will withstand 30 volts, and the SN5447A will withstand 15 volts, with a maximum reverse current of 250 microamperes. Indicator segments requiring up to 40 milliamperes of current may be driven directly from the SN5446A or SN5447A high-performance output transistors. Segment identification with resultant displays are shown in Figure A. Display patterns for BCD input counts above 9 are unique symbols to authenticate input conditions.

description (continued)

The SN5446A, SN5447A, and SN5448 circuits incorporate automatic leading and/or trailing-edge zero-blanking control (RBI and RBO). Lamp test (LT) of these types may be performed at any time when the BI/RBO node is a logical 1. All types contain an overriding blanking input (BI) which can be used to control the lamp intensity or to inhibit the outputs. All inputs except the BI/RBO nodes are one normalized Series 54/74 load. Inputs and outputs are entirely compatible for use with TTL or DTL logic outputs. Power dissipation is typically 320 milliwatts (SN5446A, SN5447A, and SN5448) or 165 milliwatts (SN5449).

The SN5446A, SN5447A, SN5448 and SN5449 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN7446A, SN7447A, SN7448, and SN7449 (electrically identical to the corresponding Series 54 types) are for operation over the temperature range of 0°C to 70°C.

TRUTH TABLE SN5446A, SN5447A, SN7446A, SN7447A

	INPUTS							OUTPUTS							
DECIMAL OR FUNCTION	LT	RBI	D	C	B	A	BI/RBO	a	b	c	d	e	f	g	NOTE
0	1	1	0	0	0	0	1	0	0	0	0	0	0	1	1
1	1	X	0	0	0	1	1	1	0	0	1	1	1	1	1
2	1	X	0	0	1	0	1	0	0	1	0	0	1	0	
3	1	X	0	0	1	1	1	0	0	0	0	1	1	0	
4	1	X	0	1	0	0	1	1	0	0	1	1	0	0	
5	1	X	0	1	0	1	1	0	1	0	0	1	0	0	
6	1	X	0	1	1	0	1	1	1	0	0	0	0	0	
7	1	X	0	1	1	1	1	0	0	0	1	1	1	1	
8	1	X	1	0	0	0	1	0	0	0	0	0	0	0	
9	1	X	1	0	0	1	1	0	0	0	1	1	0	0	
10	1	X	1	0	1	0	1	1	1	1	0	0	1	0	
11	1	X	1	0	1	1	1	1	1	0	0	1	1	0	
12	1	X	1	1	0	0	1	1	0	1	1	1	0	0	
13	1	X	1	1	0	1	1	0	1	1	0	1	0	0	
14	1	X	1	1	1	0	1	1	1	1	0	0	0	0	
15	1	X	1	1	1	1	1	1	1	1	1	1	1	1	
BI	X	X	X	X	X	X	0	1	1	1	1	1	1	1	2
RBI	1	0	0	0	0	0	0	1	1	1	1	1	1	1	3
LT	0	X	X	X	X	X	1	0	0	0	0	0	0	0	4

NOTES: 1. BI/RBO is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO). The blanking input (BI) must be open or held at a logical 1 when output functions 0 through 15 are desired, and the ripple-blanking input (RBI) must be open or at a logical 1 if blanking of a decimal 0 is not desired. X = input may be high or low.

2. When a logical 0 is applied directly to the blanking input (forced condition) all segment outputs go to a logical 0 regardless of the state of any other input condition.

3. When the ripple-blanking input (RBI) and inputs A, B, C, and D are at logical 0, with the lamp test input at logical 1, all segment outputs go to a logical 1 and the ripple-blanking output (RBO) goes to a logical 0 (response condition).

4. When the blanking input/ripple-blanking output (BI/RBO) is open or held at a logical 1, and a logical 0 is applied to the lamp-test input, all segment outputs go to a logical 0.

TRUTH TABLE SN5448, SN7448

DECIMAL OR FUNCTION	INPUTS LT	RBI	D	C	B	A	BI/RBO	OUTPUTS a	b	c	d	e	f	g	NOTE
0	1	1	0	0	0	0	1	1	1	1	1	1	1	0	1
1	1	X	0	0	0	1	1	0	1	1	0	0	0	0	1
2	1	X	0	0	1	0	1	1	1	0	1	1	0	1	
3	1	X	0	0	1	1	1	1	1	1	1	0	0	1	
4	1	X	0	1	0	0	1	0	1	1	0	0	1	1	
5	1	X	0	1	0	1	1	1	0	1	1	0	1	1	
6	1	X	0	1	1	0	1	0	0	1	1	1	1	1	
7	1	X	0	1	1	1	1	1	1	1	0	0	0	0	
8	1	X	1	0	0	0	1	1	1	1	1	1	1	1	
9	1	X	1	0	0	1	1	1	1	1	0	0	1	1	
10	1	X	1	0	1	0	1	0	0	0	1	1	0	1	
11	1	X	1	0	1	1	1	0	0	1	1	0	0	1	
12	1	X	1	1	0	0	1	0	1	0	0	0	1	1	
13	1	X	1	1	0	1	1	1	0	0	1	0	1	1	
14	1	X	1	1	1	0	1	0	0	0	1	1	1	1	
15	1	X	1	1	1	1	1	0	0	0	0	0	0	0	
BI	X	X	X	X	X	X	0	0	0	0	0	0	0	0	2
RBI	1	0	0	0	0	0	0	0	0	0	0	0	0	0	3
LT	0	X	X	X	X	X	1	1	1	1	1	1	1	1	4

NOTES: 1. BI/RBO is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO). The blanking input (BI) must be open or held at a logical 1 when output functions 0 through 15 are desired, and the ripple-blanking input (RBI) must be open or at a logical 1 if blanking of a decimal 0 is not desired. X = input may be high or low.

2. When a logical 0 is applied directly to the blanking input (forced condition) all segment outputs go to a logical 0 regardless of the state of any other input condition.

3. When the ripple-blanking input (RBI) and inputs A, B, C, and D are at logical 0, with the lamp test at logical 1, all segment outputs go to a logical 0 and the ripple-blanking output (RBO) goes to a logical 0 (response condition).

4. When the blanking input/ripple-blanking output (BI/RBO) is open or held at a logical 1, and a logical 0 is applied to the lamp-test input, all segment outputs go to a logical 1.

TRUTH TABLE SN5449, SN7449

DECIMAL OR FUNCTION	INPUTS D	C	B	A	BI	OUTPUTS a	b	c	d	e	f	g	NOTE
0	0	0	0	0	1	1	1	1	1	1	1	0	1
1	0	0	0	1	1	0	1	1	0	0	0	0	
2	0	0	1	0	1	1	1	0	1	1	0	1	
3	0	0	1	1	1	1	1	1	1	0	0	1	
4	0	1	0	0	1	0	1	1	0	0	1	1	
5	0	1	0	1	1	1	0	1	1	0	1	1	
6	0	1	1	0	1	0	0	1	1	1	1	1	
7	0	1	1	1	1	1	1	1	0	0	0	0	
8	1	0	0	0	1	1	1	1	1	1	1	1	
9	1	0	0	1	1	1	1	1	0	0	1	1	
10	1	0	1	0	1	0	0	0	1	1	0	1	
11	1	0	1	1	1	0	0	1	1	0	0	1	
12	1	1	0	0	1	0	1	0	0	0	1	1	
13	1	1	0	1	1	1	0	0	1	0	1	1	
14	1	1	1	0	1	0	0	0	1	1	1	1	
15	1	1	1	1	1	0	0	0	0	0	0	0	
BI	X	X	X	X	0	0	0	0	0	0	0	0	2

NOTES: 1. The blanking input must be open or held at a logical 1 when output functions 0 through 15 are desired.

2. When a logical 0 is applied to the blanking input all segment outputs go to a logical 0 regardless of the state of any other input condition.
X = input may be high or low.

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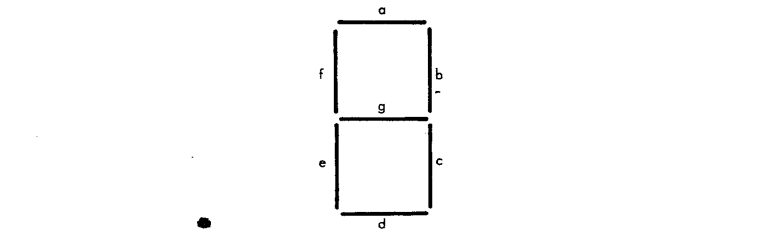
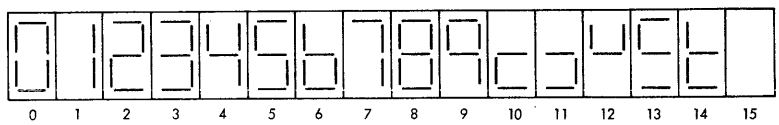


SEGMENT IDENTIFICATION



NUMERICAL DESIGNATIONS – RESULTANT DISPLAYS

FIGURE A

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1) . . . . . 7 V
Input Voltage, V_{in} (See Notes 1 and 2) . . . . . 5.5 V
Current Into any Output of SN5446A, SN7446A, SN5447A, SN7447A, SN5449, SN7449 Circuits (See Note 3) 1 mA
Operating Case Temperature Range: SN5449 Circuits . . . . . −55°C to 125°C
Operating Free-Air Temperature Range:
SN5446A, SN5447A, SN5448 Circuits . . . . . −55°C to 125°C
SN7446A, SN7447A, SN7448, SN7449 Circuits . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

NOTES: 1. These voltage values are with respect to network ground terminal.
2. Input voltage must be zero or positive with respect to network ground terminal.
3. This rating applies when the output is off.

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recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1):				
SN5446A, SN5447A, SN5448, SN5449 Circuits	4.5	5	5.5	V
SN7446A, SN7447A, SN7448, SN7449 Circuits	4.75	5	5.25	V
Continuous Voltage at Outputs a through g:				
SN5446A, SN7446A Circuits			30	V
SN5447A, SN7447A Circuits			15	V
SN5449, SN7449 Circuits			5.5	V
Normalized Fan-Out From Outputs a through g to Series 54/74 Loads:				
SN5446A, SN7446A, SN5447A, SN7447A Circuits			24	
SN5448, SN7448 Circuits			4	
SN5449, SN7449 Circuits			6	
Normalized Fan-Out From BI/RBO Node to Series 54/74 Loads:				
SN5446A, SN7446A, SN5447A, SN7447A, SN5448, SN7448 Circuits			5	
Output Sink Current, I_{sink}:				
SN5446A, SN7446A, SN5447A, SN7447A Outputs a through g			40	mA
SN5448, SN7448 Outputs a through g			6.4	mA
SN5449, SN7449 Outputs a through g			10	mA
SN5446A, SN7446A, SN5447A, SN7447A, SN5448, SN7448 BI/RBO Node			8	mA

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input	1 and 2			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input	1 and 2					0.8	V
V_{on}	On-state output voltage at outputs a through g	1	V_{CC}=MIN, I_{sink}=40 mA			0.3	0.4	V
$V_{out(0)}$	Logical 0 output voltage at BI/RBO node	1	V_{CC}=MIN, I_{sink}=8 mA			0.3	0.4	V
V_{off}	Off-state output voltage at outputs a through g (SN5446A and SN7446A only)	2	V_{CC}=MAX, I_{off}=250 µA		30			V
V_{off}	Off-state output voltage at outputs a through g (SN5447A and SN7447A only)	2	V_{CC}=MAX, I_{off}=250 µA		15			V
$V_{out(1)}$	Logical 1 output voltage at BI/RBO node	2	V_{CC}=MIN, I_{load}=-200 µA		2.4	3.7		V
$I_{in(0)}$	Logical 0 level input current at any input except BI/RBO node	3	V_{CC}=MAX, V_{in}=0.4 V				-1.6	mA
$I_{in(0)}$	Logical 0 level input current at BI/RBO node	3	V_{CC}=MAX, V_{in}=0.4 V				-4.2	mA
$I_{in(1)}$	Logical 1 level input current at any input except BI/RBO node	4	V_{CC}=MAX, V_{in}=2.4 V				40	µA
			V_{CC}=MAX, V_{in}=5.5 V				1	mA
I_{OS}	Short-circuit output current at BI/RBO node	5	V_{CC}=MAX				-4	mA
I_{CC}	Supply current	4	V_{CC}=MAX	SN5446A, SN5447A		64	85	mA
				SN7446A, SN7447A		64	103	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

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switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd1}	Propagation delay time to logical 1 level from A input to any output	6	C_L=15 pF, R_L=120 Ω			100	ns
t_{pd0}	Propagation delay time to logical 0 level from A input to any output	6	C_L=15 pF, R_L=120 Ω			100	ns
t_{pd1}	Propagation delay time to logical 1 level from RBI input to any output	6	C_L=15 pF, R_L=120 Ω			100	ns
t_{pd0}	Propagation delay time to logical 0 level from RBI input to any output	6	C_L=15 pF, R_L=120 Ω			100	ns

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS †		MIN	TYP ‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input	1 and 2			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input	1 and 2		SN5449			0.6	V
				All others			0.8	
$V_{out(0)}$	Logical 0 output voltage at any output (SN5448, SN7448 only)	1	V_{CC} = MIN, I_{sink} = MAX			0.27	0.4	V
V_{on}	On-state output voltage at any output (SN5449, SN7449 only)	1	V_{CC} = MIN, I_{sink} = MAX			0.27	0.4	V
$V_{out(1)}$	Logical 1 level output voltage at outputs a through g (SN5448, SN7448)	2	V_{CC} = MIN, I_{load} = -400 μA		2.4	4.2		V
$V_{out(1)}$	Logical 1 level output at BI/RBO node (SN5448, SN7448 only)	2	V_{CC} = MIN, I_{load} = -200 μA		2.4	3.7		V
I_{load}	Load current available at outputs a through g (SN5448, SN7448 only)	2	V_{CC} = MIN, V_{out} = 0.85 V		-1.3	-2		mA
V_{off}	Off-state output voltage at any output (SN5449, SN7449 only)	2	V_{CC} = MAX, I_{off} = 250 μA		5.5			V
$I_{in(0)}$	Logical 0 level input current at any input (except BI/RBO node of SN5448, SN7448)	3	V_{CC} = MAX, V_{in} = 0.4 V				-1.6	mA
$I_{in(0)}$	Logical 0 level input current at BI/RBO node (SN5448, SN7448 only)	3	V_{CC} = MAX, V_{in} = 0.4 V				-4.2	mA
$I_{in(1)}$	Logical 1 level input current at any input (except BI/RBO node of SN5448, SN7448)	4	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current at any output (except outputs a through g of SN5449, SN7449)	5	V_{CC} = MAX				-4	mA
I_{CC}	Supply current	4		SN5448		53	76	mA
				SN7448		53	90	mA
				SN5449		33	47	mA
				SN7449		33	56	mA

† For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ These typical values are at V_{CC} = 5 V, T_A = 25°C

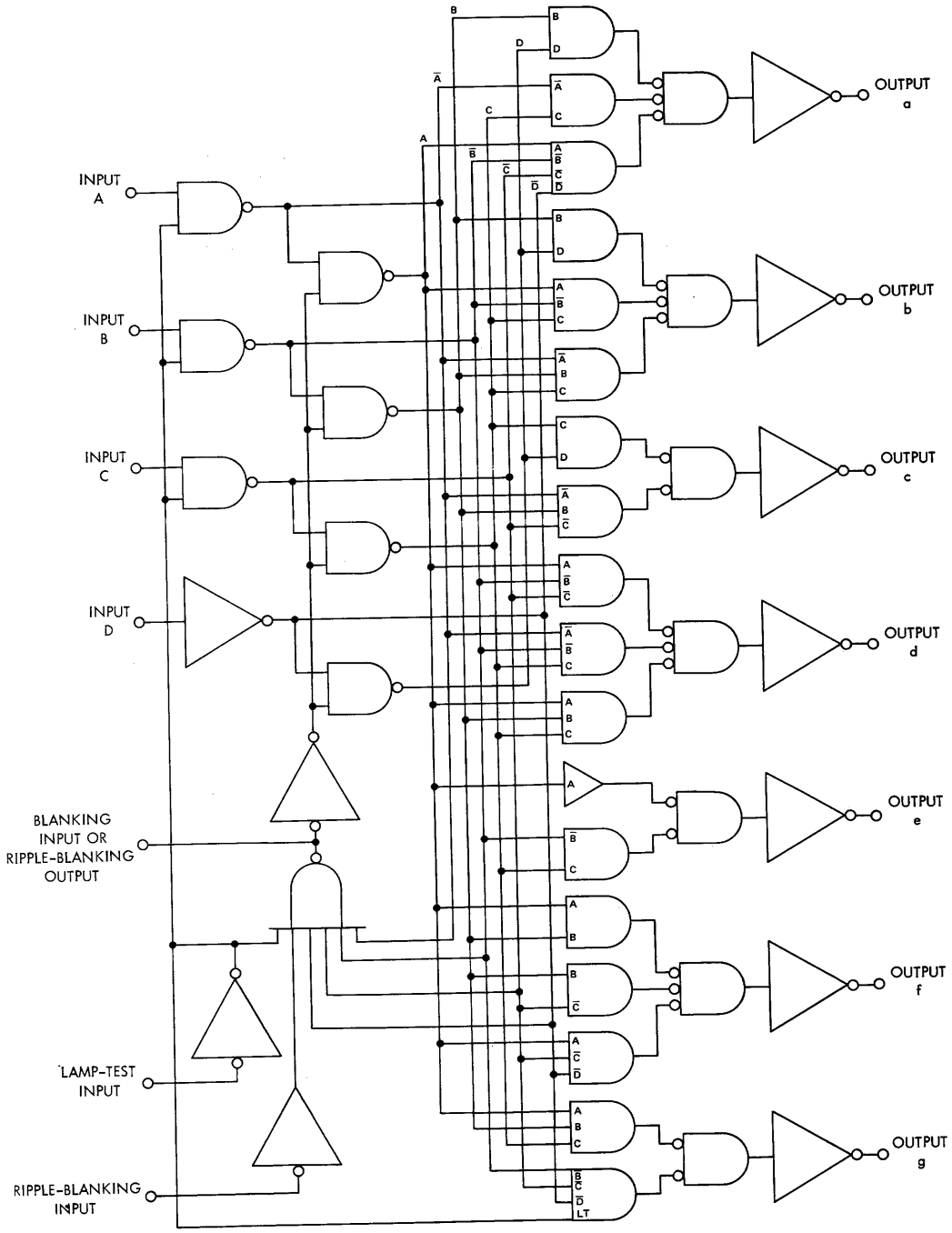
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS §	MIN	TYP	MAX	UNIT
t_{pd1}	Propagation delay time to logical 1 level from A input to any output	6	C_L = 15 pF			100	ns
t_{pd0}	Propagation delay time to logical 0 level from A input to any output	6	C_L = 15 pF			100	ns
t_{pd1}	Propagation delay time to logical 1 level from RBI input to any output	6	C_L = 15 pF			100	ns
t_{pd0}	Propagation delay time to logical 0 level from RBI input to any output	6	C_L = 15 pF			100	ns

§ R_L = 1 kΩ for SN5448 and SN5449; R_L = 667 Ω for SN7448 and SN7449.

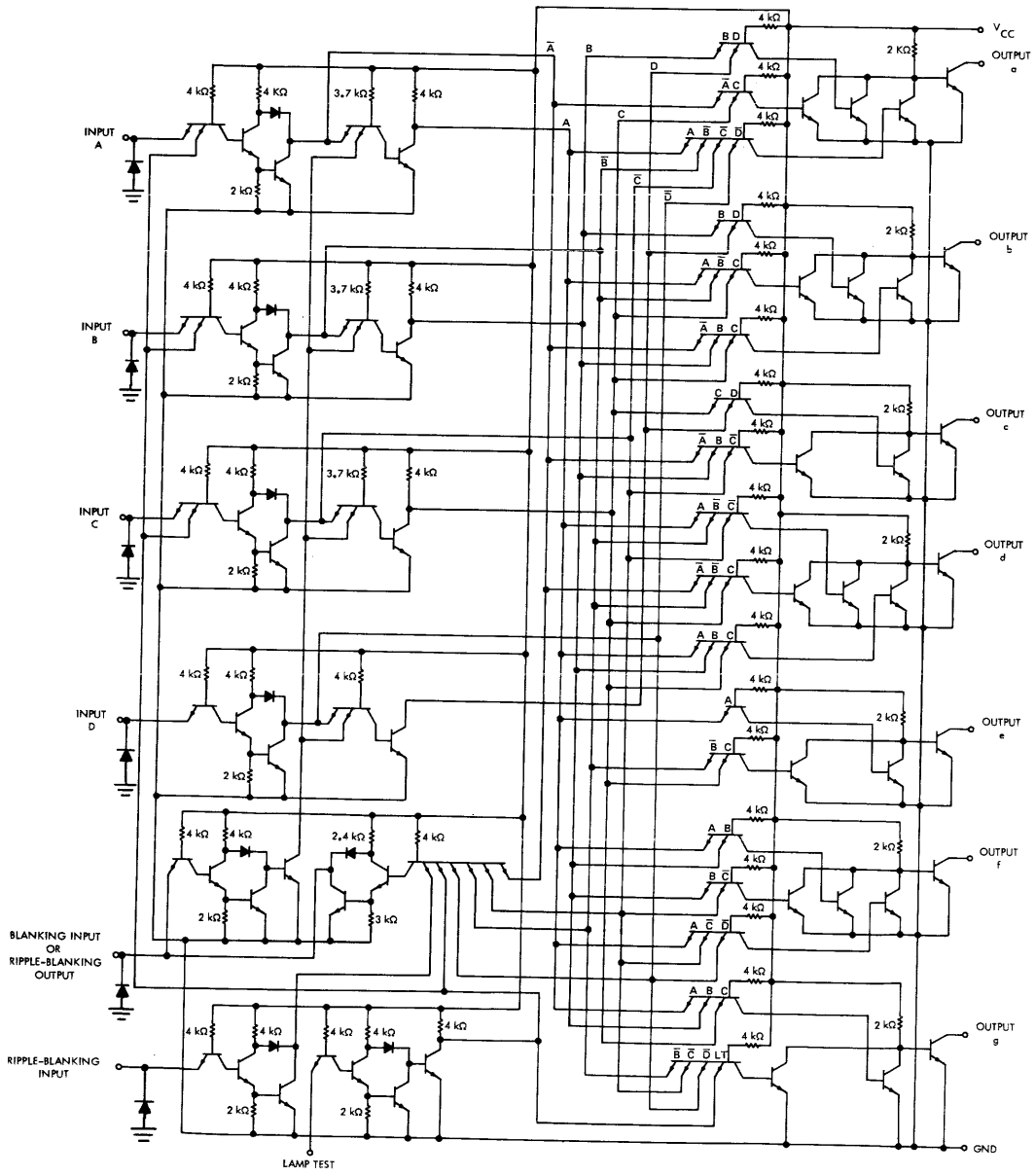
—SEE ORDERING INSTRUCTIONS PAGE 1-1—

functional block diagram



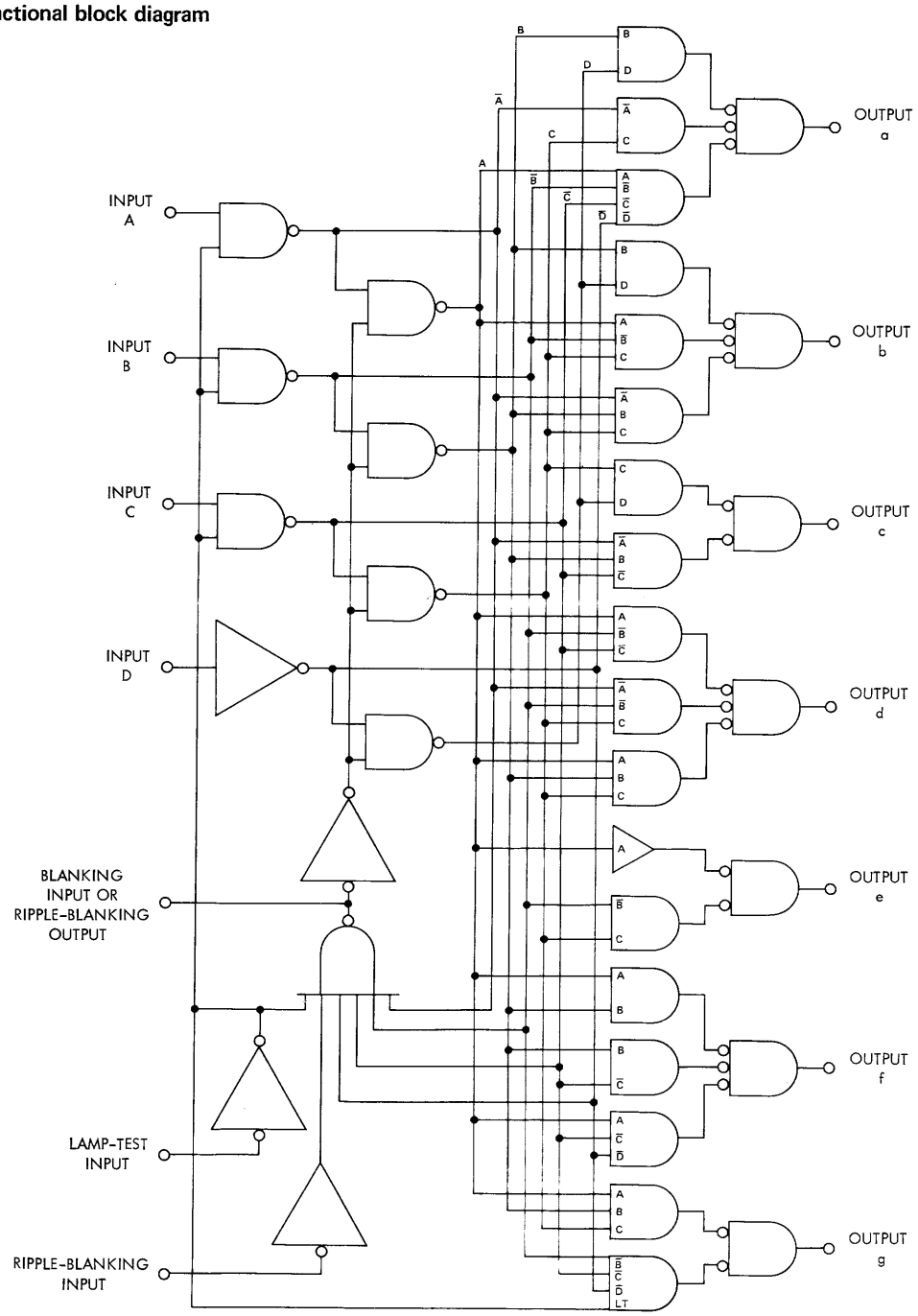
9

schematic diagram

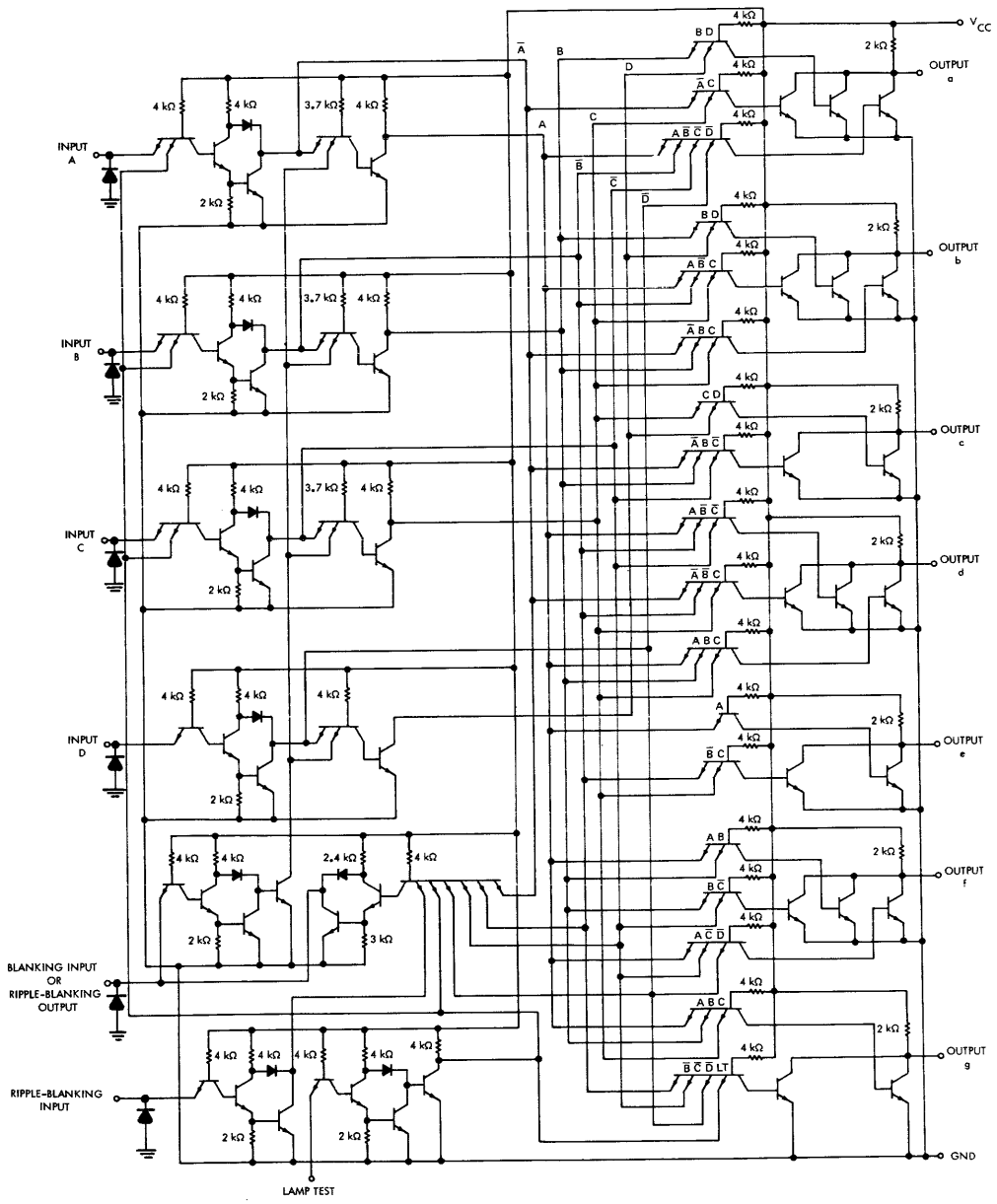


Component values shown are nominal

functional block diagram

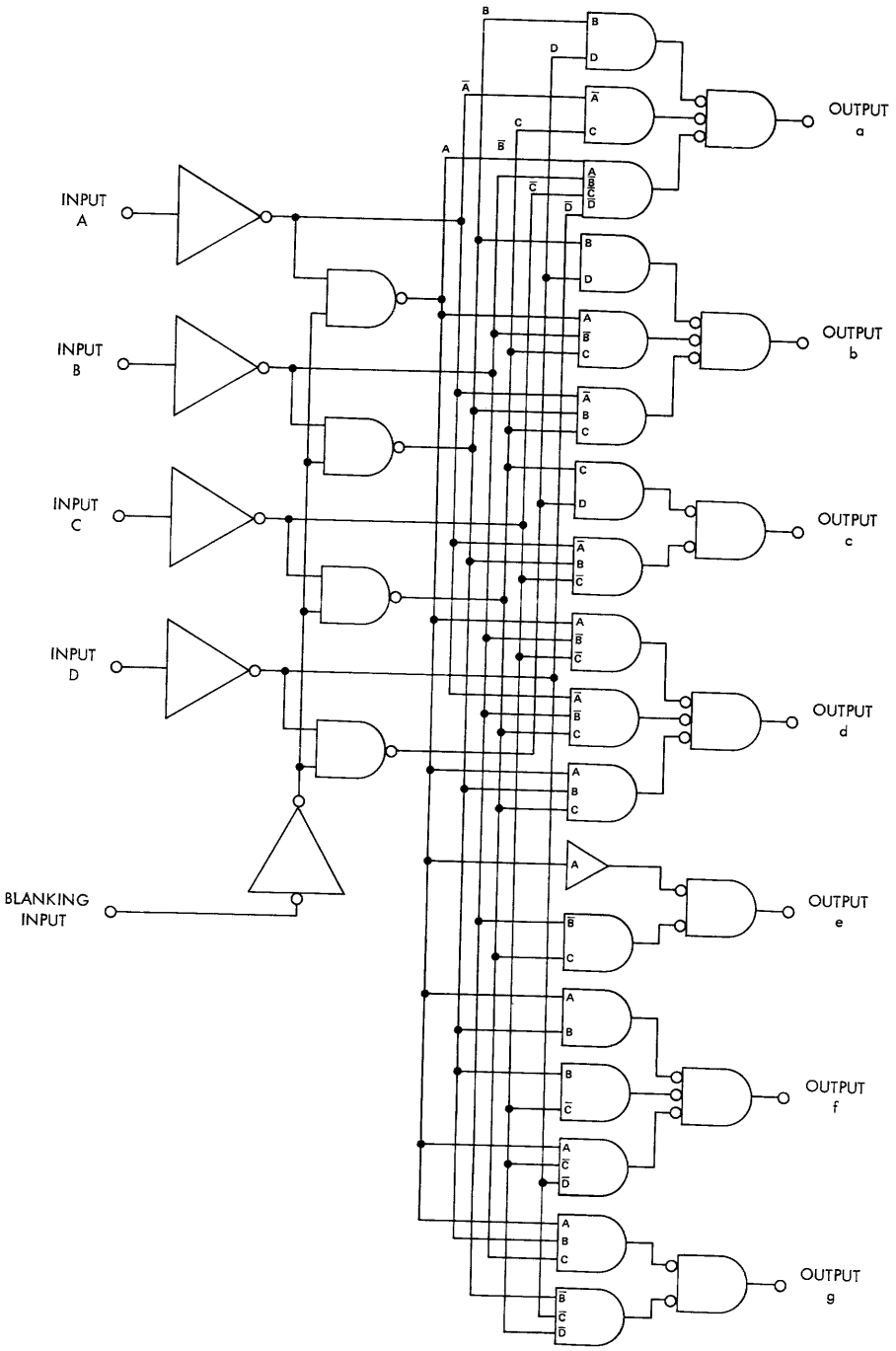


schematic diagram

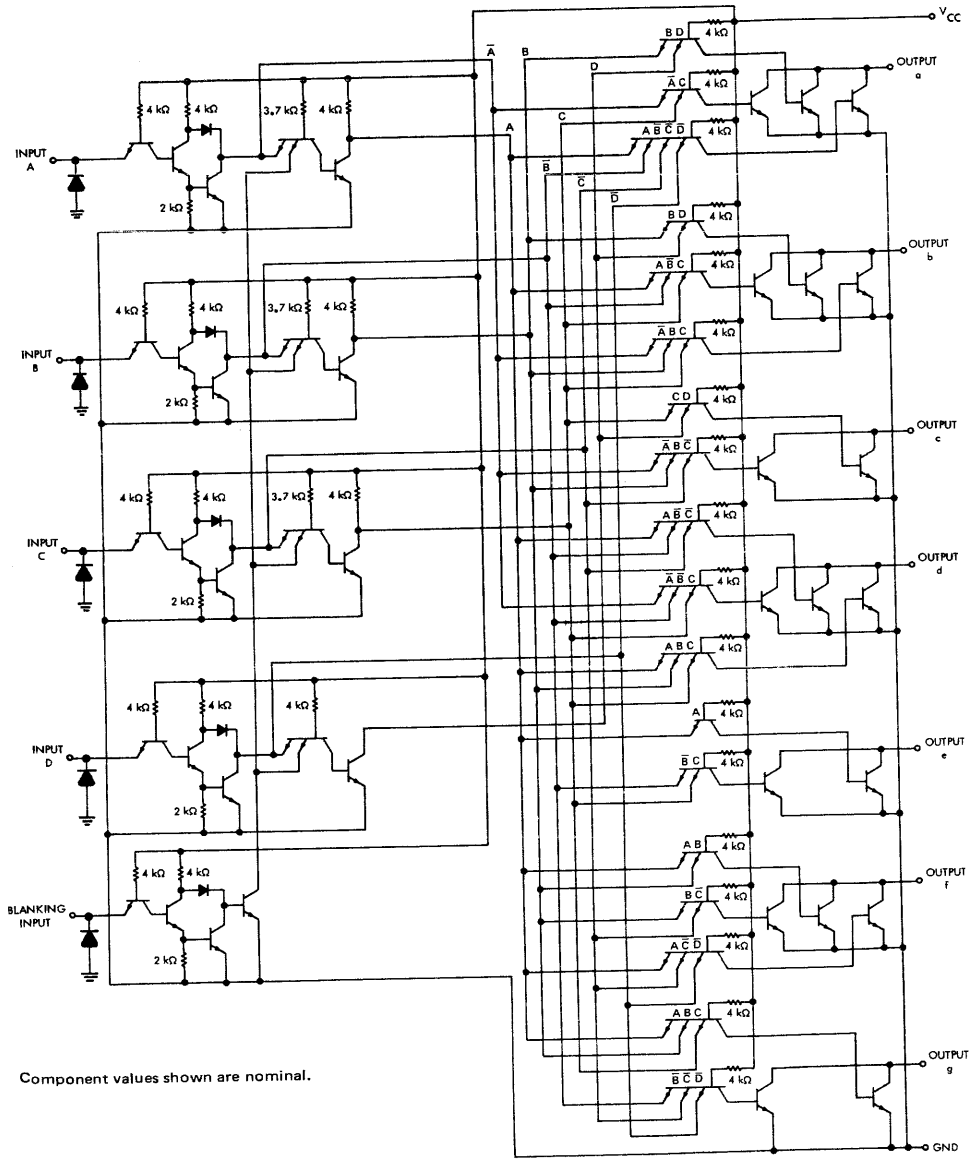


Compenent values shown are nominal

functional block diagram



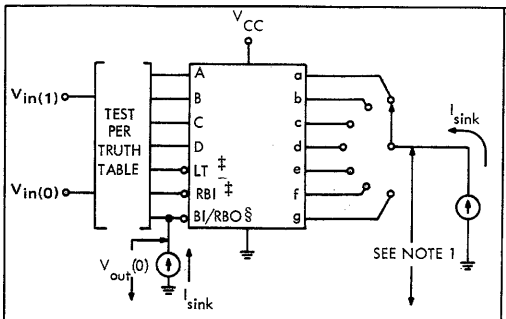
schematic diagram



Component values shown are nominal.

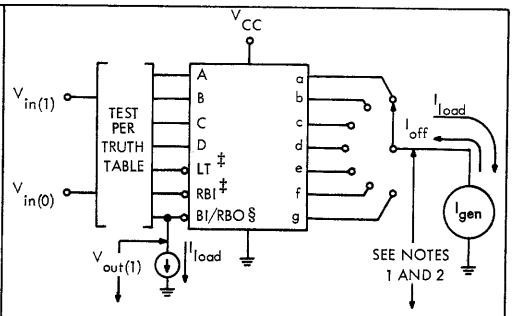
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



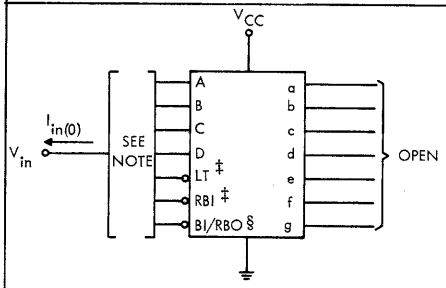
1. Measure V_{on} for SN5446A, SN5447A, SN5449, SN7446A, SN7447A, and SN7449. Measure $V_{out(0)}$ for SN5448 and SN7448.

FIGURE 1



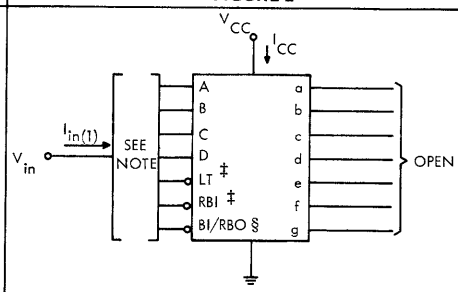
1. Measure V_{off} for SN5446A, SN5447A, SN5449, SN7446A, SN7447A, and SN7449.
2. Measure $V_{out(1)}$ for SN5448 and SN7448.

FIGURE 2



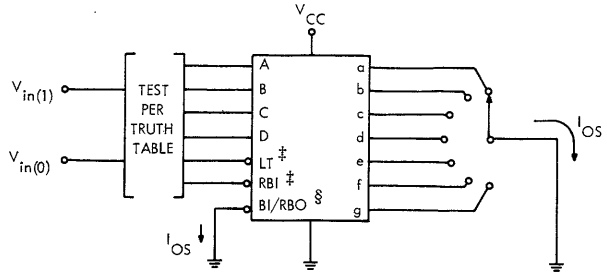
1. Each input is tested separately.

FIGURE 3



1. Each input is tested separately for $I_{in(1)}$.

FIGURE 4



1. Each output is tested separately.

FIGURE 5

†Arrows indicate actual direction of current flow. Logic symbol used is representative for all types.
‡Available on SN5446A, SN5447A, SN5448, SN7446A, SN7447A, and SN7448 only.
§BI is available on all types. RBO node is available on SN5446A, SN5447A, SN5448, SN7446A, SN7447A, and SN7448 only.

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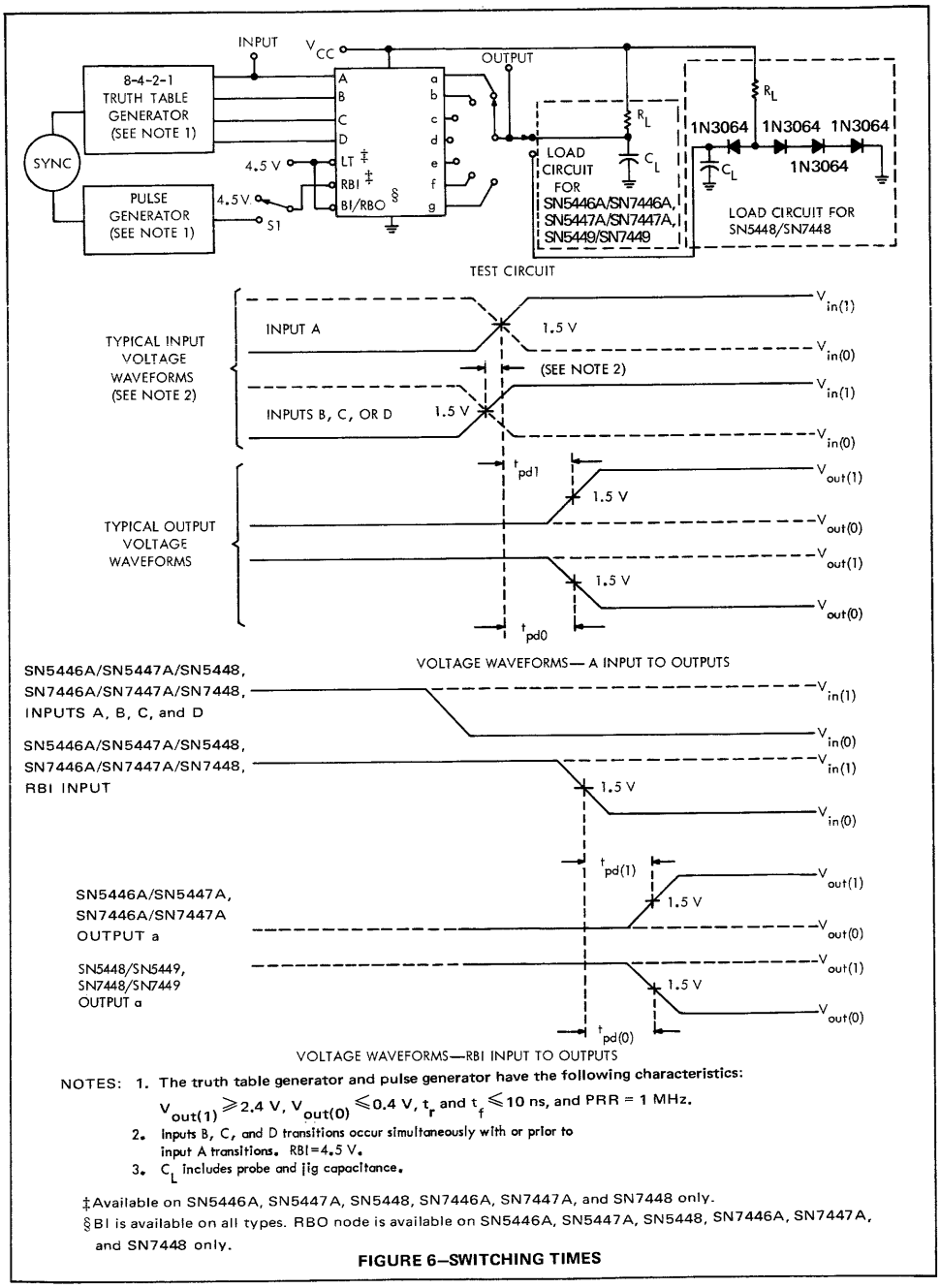
PARAMETER MEASUREMENT INFORMATION

switching characteristics



NOTES: 1. The truth table generator and pulse generator have the following characteristics:
$V_{out(1)} \geq 2.4$ V, $V_{out(0)} \leq 0.4$ V, t_r and $t_f \leq 10$ ns, and PRR = 1 MHz.
2. Inputs B, C, and D transitions occur simultaneously with or prior to input A transitions. RBI = 4.5 V.
3. C_L includes probe and jig capacitance.

‡Available on SN5446A, SN5447A, SN5448, SN7446A, SN7447A, and SN7448 only.
§BI is available on all types. RBO node is available on SN5446A, SN5447A, SN5448, SN7446A, SN7447A, and SN7448 only.

FIGURE 6—SWITCHING TIMES

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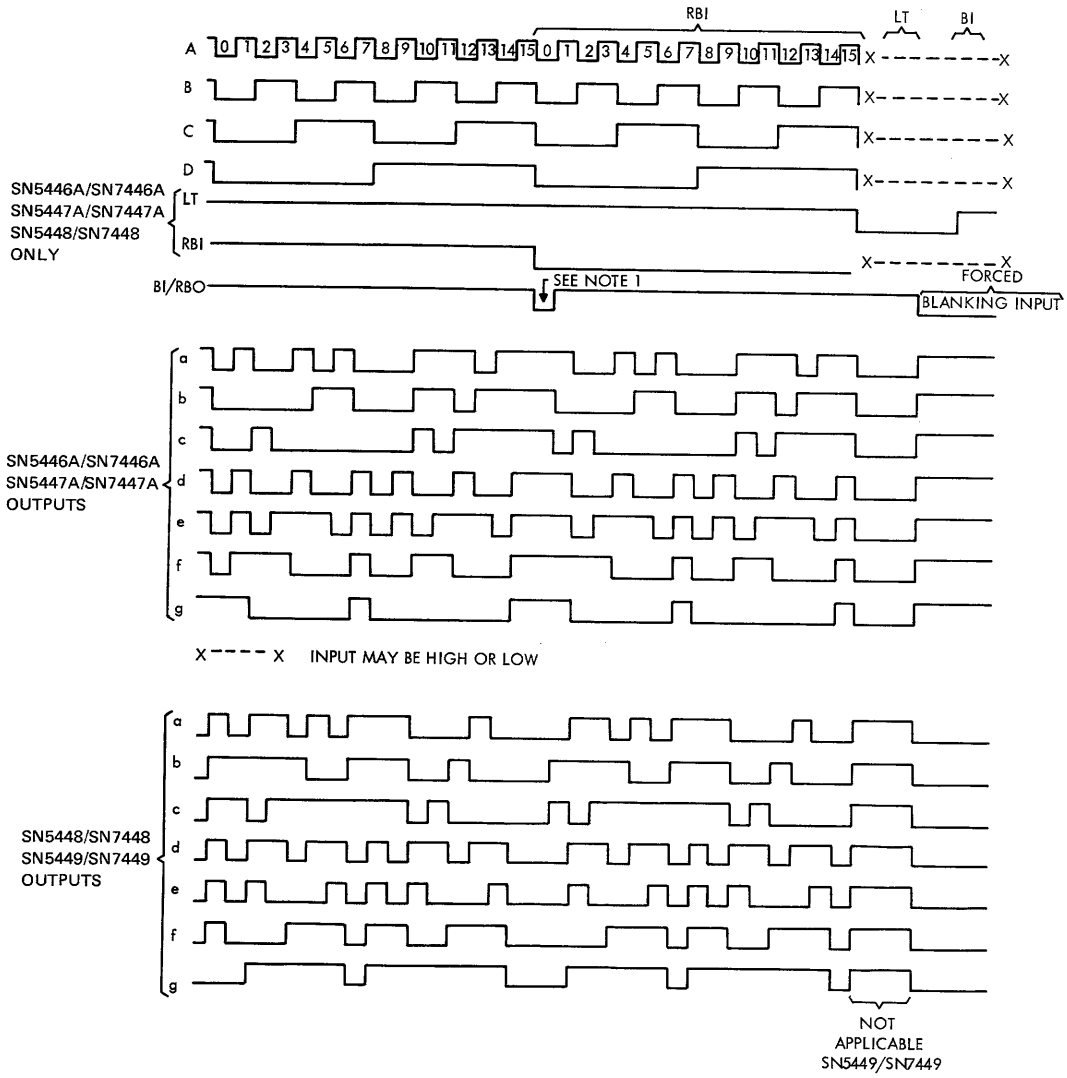
TYPICAL INPUT/OUTPUT VOLTAGE WAVEFORMS



NOTE 1: For the SN5446A, SN5447A, SN5448, SN7446A, SN7447A, and SN7448 this logical 0 represents the RBO response. For the SN5449 and SN7449 a logical 0 pulse is applied to the blanking input.

9

APPLICATIONS DATA

driving indicators directly (see Figure B)

This application demonstrates how the SN5446A or SN5447A may be used to drive seven-segment indicators directly. The output transistors of these two circuit types will sink up to 40 milliamperes of current; therefore, external components are not required.

Also illustrated is how the quadruple latch (SN5475) and decade counter (SN5490) may be utilized to acquire and store the numeral to be displayed. The method shown is typical of a single stage and a number of methods are possible for distributing the BCD data from the decade counter to the quadruple latch.

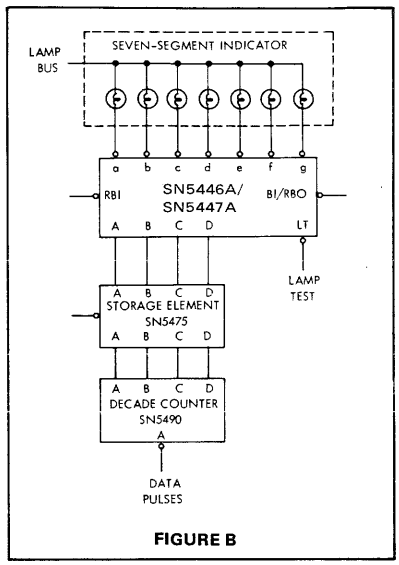


FIGURE B

n-digit display with leading-and trailing-edge blanking (see Figure C)

This application demonstrates a method for driving incandescent, seven-segment, display indicators directly from the output of the SN5446A, or SN5447A decoder with provisions for leading-edge and trailing-edge zero-blanking, intensity control, and lamp test.

Leading-edge and trailing-edge zero blanking is illustrated for a six-digit mixed integer with zero indications suppressed for the two most-significant decades (MSD) of the whole number and the two least-significant decades (LSD). This scheme causes the number to be displayed in its easily identified, common form. Blanking is accomplished by grounding RBI inputs of most-significant and least-significant decades and interconnecting the BI/BRO nodes of these two decades to the ripple-blanking inputs of the adjacent decades. This improves readability by inhibiting suppression of zeros occurring on either side of the decimal point. The ripple-blanking inputs of the decades on either side of the fixed decimal point are inhibited by connecting to a 5-volt d-c source.

Intensity control is accomplished at all six of the decoder/drivers by modulating the blanking input with a multivibrator. Best results are obtained with a modulation source in which the duty cycle can be varied. Individual drivers are required as they are wire-OR connected with the ripple-blanking functions.

As the lamp-test input is only one load, a number (up to ten) of these may be driven from a single Series 54/74 circuit.

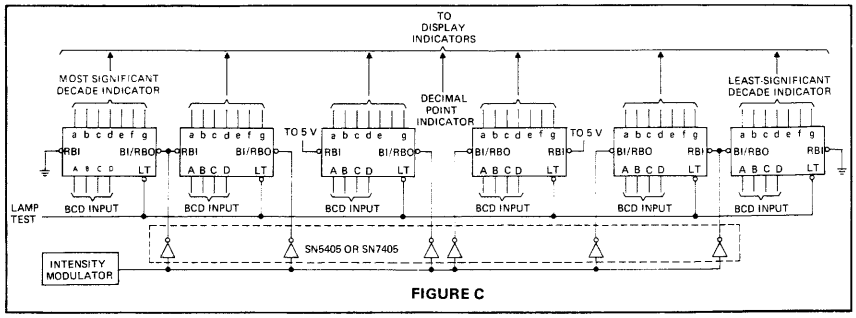


FIGURE C

APPLICATIONS DATA

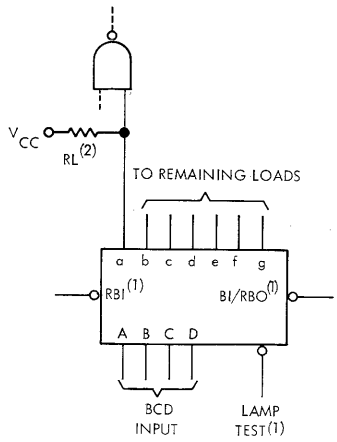
driving logic circuits (see Figure D)

These decoder/drivers may be used to drive other logic circuits. (See Figure D.) Value of the pull-up resistor (required on the open-collector outputs) may be calculated using the methods given for the SN5401 open-collector NAND gate.

driving buffer transistors (see Figures E and F)

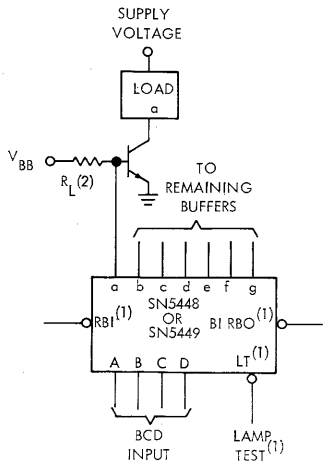
For applications requiring increased drive currents these decoder/drivers may be used with discrete drivers. A universal method of supplying base drive for a buffer transistor is illustrated in Figure E. Value of the base resistor (required on the open-collector outputs) may be calculated using the methods similar to those given for the SN5401 open-collector NAND gate. Increased base drive from the SN5448 is possible with the employment of external base resistor.

Circuitry for employing SCR's to drive electro-luminescent displays is illustrated in Figure F.



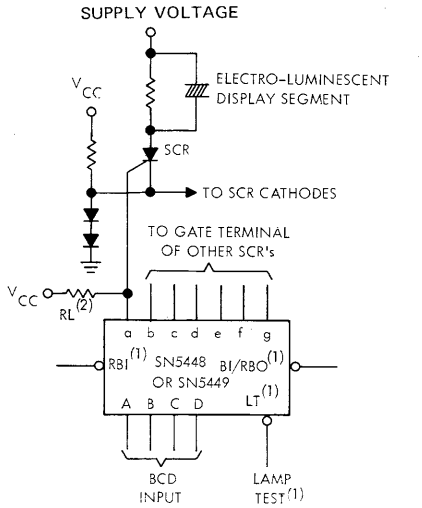
1. Available on SN5446A, SN5447A, SN5448, SN7446A, SN7447A, and SN7448 only.
2. Pull-up resistor is required with SN5446A, SN5447A, SN5449, SN7446A, SN7447A or SN7449, and is optional with SN5448 or SN7448.

FIGURE D



1. Available on SN5448 and SN7448 only.
2. Pull-up resistor is required with SN5449 or SN7449, and is optional with SN5448 or SN7448.

FIGURE E



1. Available on SN5448 and SN7448 only.
2. Pull-up resistor is required with SN5449 or SN7449, and is optional with SN5448 or SN7448.

FIGURE F

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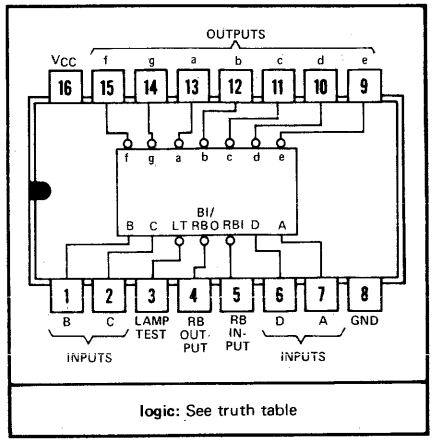
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN54L46, SN54L47, SN74L46, SN74L47 BCD-TO-SEVEN-SEGMENT DECODER/DRIVERS

- Direct Drive for Indicators
- Open-Collector Outputs
- Lamp-Test Provision
- Lamp Intensity Modulation Capability
- Full Decoding of All 16 Input Combinations
- Leading/Trailing Zero Suppression
- Fully Compatible with Most TTL and DTL Circuits
- Low Power Dissipation . . . 133 mW Typical

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



logic: See truth table

description

These monolithic, TTL, BCD-to-seven-segment decoder/drivers consist of NAND gates, input buffers, and seven AND-OR-INVERT gates. These devices offer high-sink-current outputs for driving indicators directly. Seven NAND gates and one driver are connected in pairs to make binary-coded-decimal (BCD) data and its complement available to the seven decoding AND-OR-INVERT gates. The remaining NAND gate and three input buffers provide lamp test blanking input/ripple-blanking output, and ripple-blanking inputs.

These circuits accept four-bit BCD data and, depending on the levels at the auxiliary inputs, decode this data to drive seven-segment display indicators. The output states, as well as conditions required at the auxiliary inputs, are shown in the truth table. The output circuitry is designed to withstand the relatively high voltages required for seven-segment indicators. The SN54L46/SN74L46 outputs will withstand 30 volts, and the SN54L47/SN74L47 outputs will withstand 15 volts, with a maximum reverse current of 250 microamperes. Indicator segments requiring up to 20 milliamperes of current may be driven directly from the outputs. Segment identification with resultant displays are shown in the figure on the following page. Display patterns for binary input counts above nine are unique symbols to authenticate input conditions.

These devices contain an overriding blanking input (BI) which can be used to control the lamp intensity (See Figure B of typical application data) or to inhibit the outputs. They also incorporate leading and/or trailing-edge zero-blanking control (RBI and RBO). Lamp test (LT) may be performed at any time when the BI/RBO node is at a high level. All inputs except the BI/RBO node are one-half of one normalized Series 54/74 load, or approximately five Series 54L/74L gate loads at a low logic level, two Series 54L/74L gate loads at a high logic level. The SN54L46 and SN54L47 are characterized for operation over the full military temperature range of −55°C to 125°C; the SN74L46 and SN74L47 are characterized for operation from 0°C to 70°C.

TEXAS INSTRUMENTS
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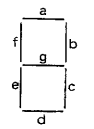
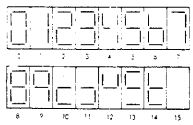
TRUTH TABLE

DECIMAL OR FUNCTION	INPUTS						BI/RBO†	OUTPUTS							NOTE
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	ON	ON	ON	ON	ON	ON	OFF	1
1	H	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF	1
2	H	X	L	L	H	L	H	ON	ON	OFF	ON	ON	OFF	ON	
3	H	X	L	L	H	H	H	ON	ON	ON	ON	OFF	OFF	ON	
4	H	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON	
5	H	X	L	H	L	H	H	ON	OFF	ON	ON	OFF	ON	ON	
6	H	X	L	H	H	L	H	OFF	OFF	ON	ON	ON	ON	ON	
7	H	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF	
8	H	X	H	L	L	L	H	ON	ON	ON	ON	ON	ON	ON	
9	H	X	H	L	L	H	H	ON	ON	ON	OFF	OFF	ON	ON	
10	H	X	H	L	H	L	H	OFF	OFF	OFF	ON	ON	OFF	ON	
11	H	X	H	L	H	H	H	OFF	OFF	ON	ON	OFF	OFF	ON	
12	H	X	H	H	L	L	H	OFF	ON	OFF	OFF	OFF	ON	ON	
13	H	X	H	H	L	H	H	ON	OFF	OFF	ON	OFF	ON	ON	
14	H	X	H	H	H	L	H	OFF	OFF	OFF	ON	ON	ON	ON	
15	H	X	H	H	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
BI	X	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	2
RBI	H	L	L	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	3
LT	L	X	X	X	X	X	H	ON	ON	ON	ON	ON	ON	ON	4



SEGMENT IDENTIFICATION



NUMERICAL DESIGNATIONS AND RESULTANT DISPLAYS

H = high level, L = low level, X = irrelevant

NOTES: 1. The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input (RBI) must be open or high if blanking of a decimal zero is not desired.
2. When a low logic level is applied directly to the blanking input (BI), all segment outputs are off regardless of the state of any other input condition.
3. When ripple-blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go off and the ripple-blanking output (RBO) goes to a low level (response condition).
4. When the blanking input/ripple blanking output (BI/RBO) is open or held high and a low is applied to the lamp-test input, all segment outputs are on.

†BI/RBO is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Peak output current ($t_w \leq 1$ ms, duty cycle $\leq 10\%$) . . . . . 200 mA
Current forced into any output in the off state . . . . . 1 mA
Operating free-air temperature range: SN54L46, SN54L47 Circuits . . . . . −55°C to 125°C
SN74L46, SN74L47 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54L46, SN54L47			SN74L46, SN74L47			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Off-state output voltage, $V_{O(off)}$, outputs a thru g	SN54L46, SN74L46			30			30	V
	SN54L47, SN74L47			15			15	
On-state output current, $I_{O(on)}$	a thru g			20			20	mA
Low-level output current, I_{OL}	BI/RBO			4			4	
Operating free-air temperature, T_A		−55		125	0		70	C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
V_{IH}	High-level input voltage		1 and 2		2		V
V_{IL}	Low-level input voltage		1 and 2			0.8	V
V_I	Input clamp voltage		3	V_{CC} = MIN, I_I = −12 mA		−1.5	V
V_{OH}	High-level output voltage	BI/RBO	1	V_{CC} = MIN, I_{OH} = −100 μA	2.4		V
V_{OL}	Low-level output voltage	BI/RBO	2	V_{CC} = MIN, I_{OL} = 4 mA		0.4	V
$I_{O(off)}$	Off-state output current	a thru g	1	V_{CC} = MAX, $V_{O(off)}$ = MAX		250	μA
$V_{O(on)}$	On-state output voltage	a thru g	2	V_{CC} = MIN, $I_{O(on)}$ = 20 mA		0.4	V
I_I	Input current at maximum input voltage	any input except BI/RBO	4	V_{CC} = MAX, V_I = 5.5 V		1	mA
I_{IH}	High-level input current	any input except BI/RBO	4	V_{CC} = MAX, V_I = 2.4 V		20	μA
I_{IL}	Low-level input current	any input except BI/RBO	3	V_{CC} = MAX, V_I = 0.4 V		−0.8	mA
		BI/RBO				−2.1	
I_{OS}	Short-circuit output current	BI/RBO	5	V_{CC} = MAX		−4	mA
I_{CC}	Supply current	SN54L46, SN54L47	6	V_{CC} = MAX		43	mA
		SN74L46, SN74L47				52	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{off}	Turn-off time from A input	7	C_L = 15 pF, R_L = 280 Ω		200	ns
t_{on}	Turn-on time from A input				200	ns
t_{off}	Turn-off time from RBI input				200	ns
t_{on}	Turn-on time from RBI input				200	ns

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TEXAS INSTRUMENTS
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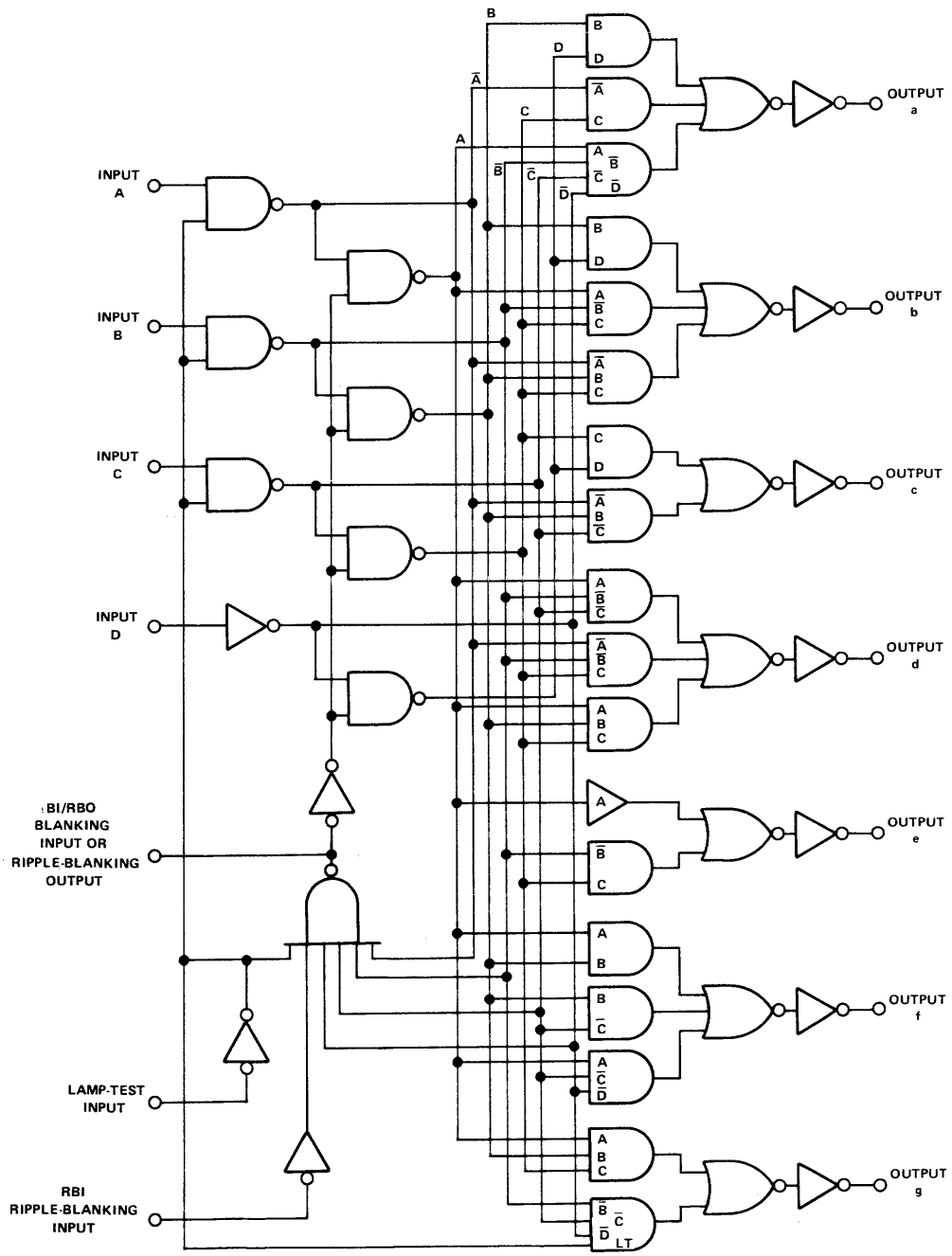
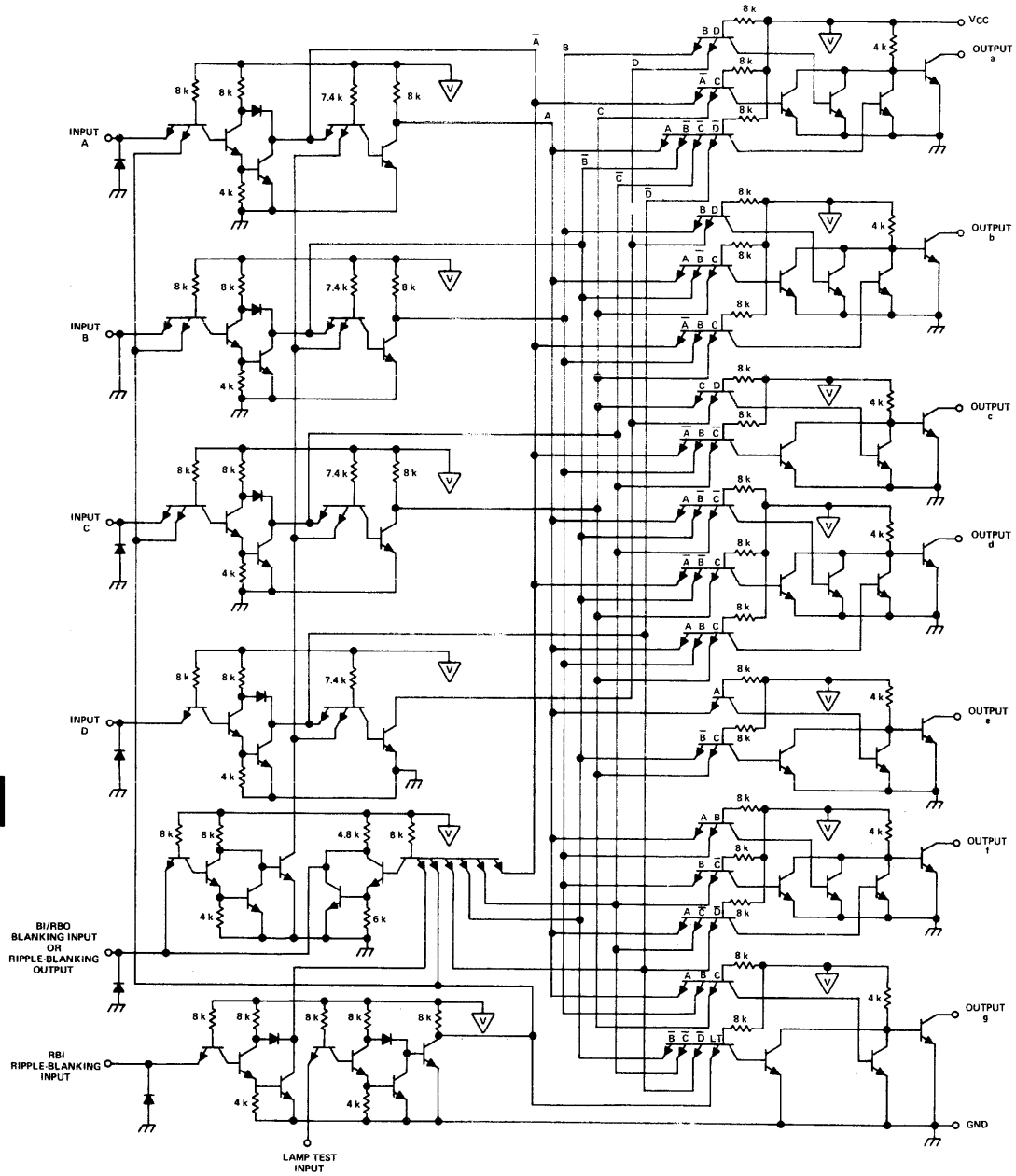
functional block diagram



9

schematic diagram



Resistor values shown are nominal in ohms.
▽ ...V_{CC} bus

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PARAMETER MEASUREMENT INFORMATION

d-c test circuits†

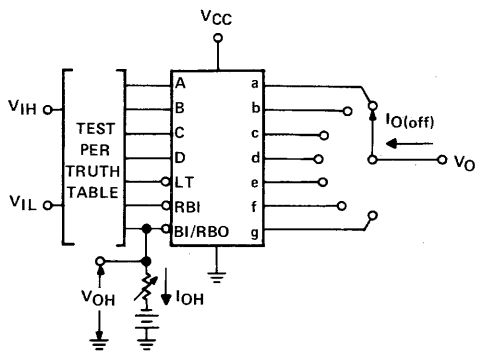


FIGURE 1

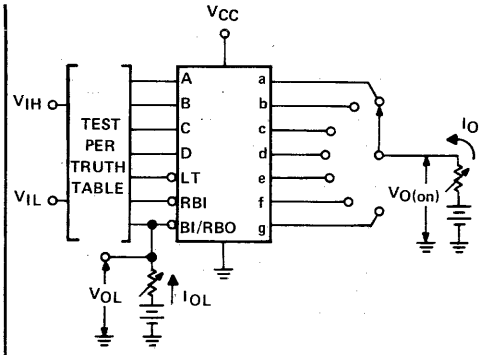
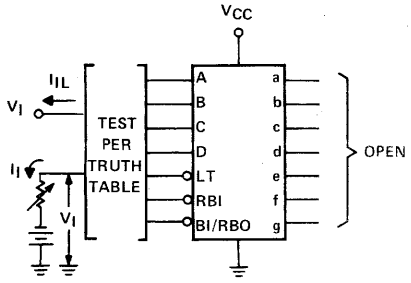
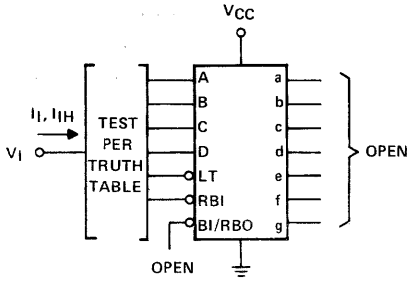


FIGURE 2



Each input is tested separately.

FIGURE 3



Each input is tested separately.

FIGURE 4

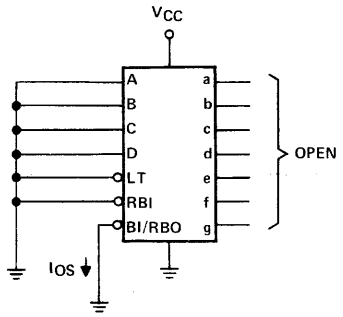


FIGURE 5

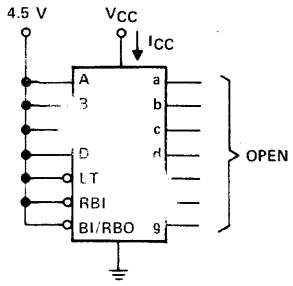


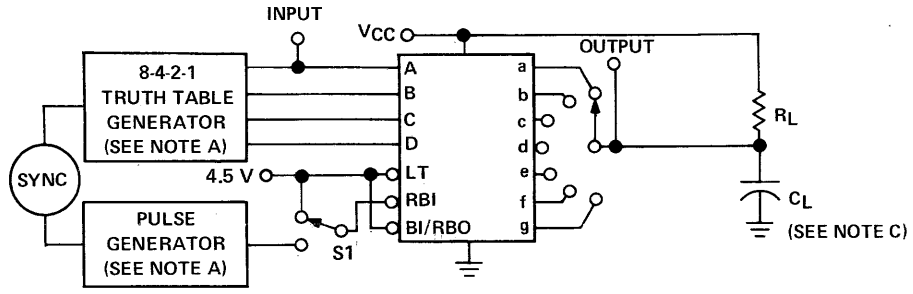
FIGURE 6

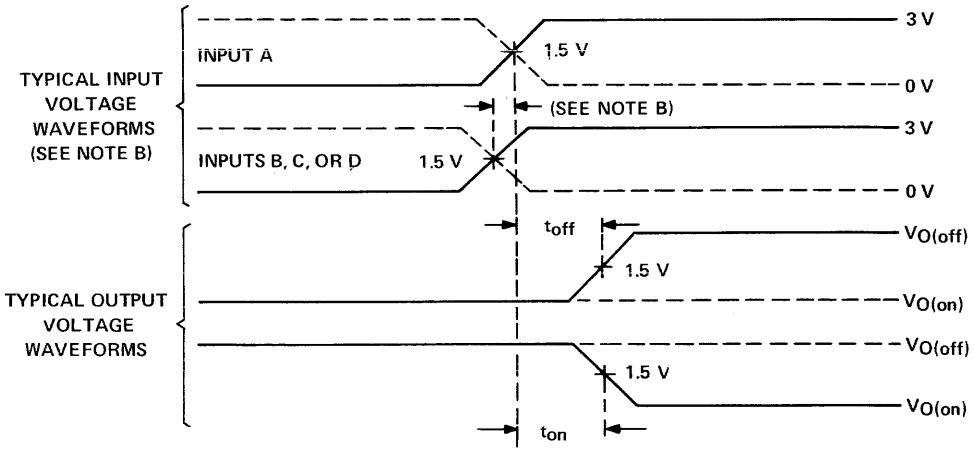
†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

9

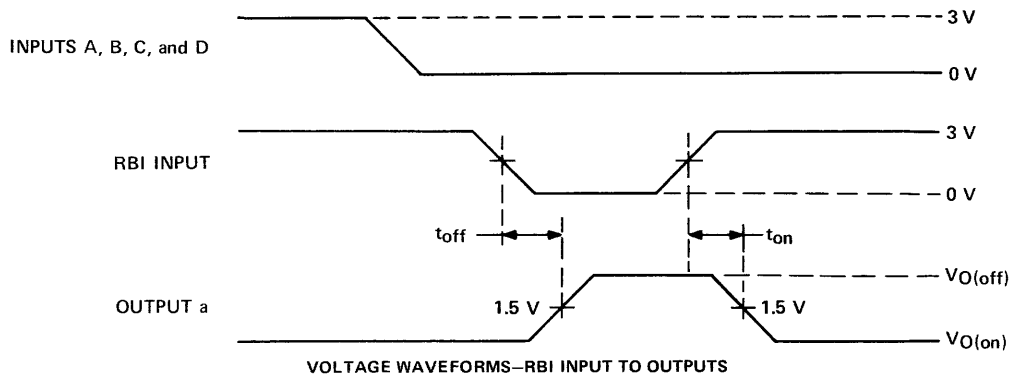
PARAMETER MEASUREMENT INFORMATION

switching characteristics





VOLTAGE WAVEFORMS—A INPUT TO OUTPUTS



VOLTAGE WAVEFORMS—RBI INPUT TO OUTPUTS

NOTES: A. The truth table generator and pulse generator have the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, and PRR ≤ 1 MHz, $Z_{out} = 50\ \Omega$.
B. Inputs B, C, and D transitions occur simultaneously with or prior to input A transitions. RBI = 4.5 V.
C. C_L includes probe and jig capacitance.

FIGURE 7—SWITCHING TIMES

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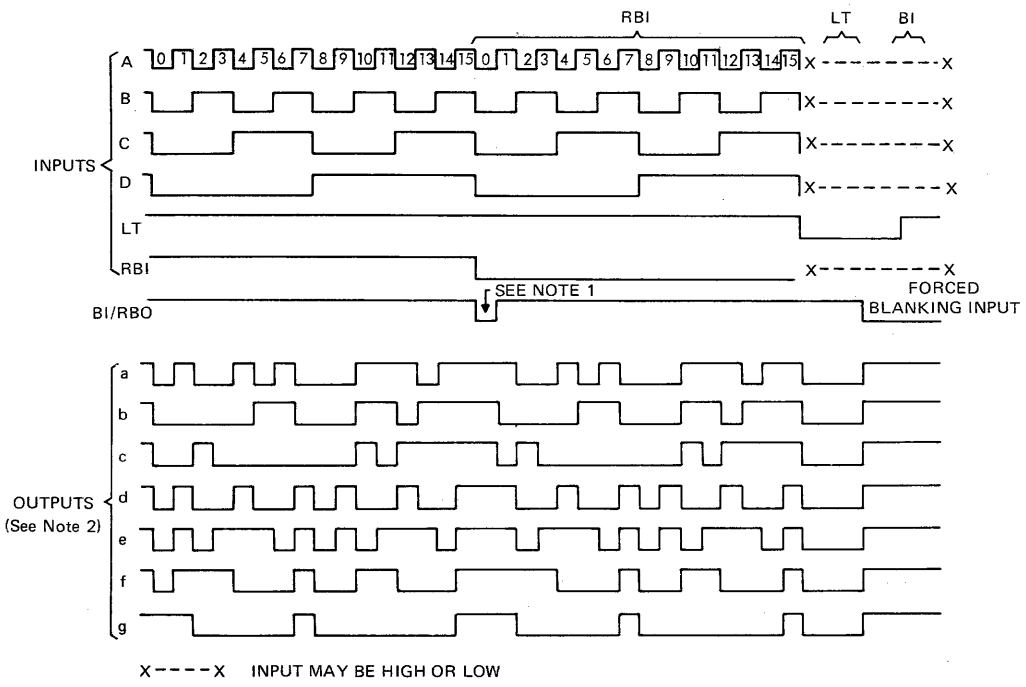
TYPICAL INPUT/OUTPUT VOLTAGE WAVEFORMS



NOTES: 1. This low-level pulse represents the RBO response.
2. For the outputs, a high level indicates the off state and a low level represents the on state.

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TYPICAL APPLICATION DATA

driving indicators directly (see Figure A)

This application demonstrates how the SN54L46 or SN54L47 may be used to drive seven-segment indicators directly. The output transistors of these two circuit types will sink up to 20 milliamperes of current; therefore, external components are not required.

Also illustrated is how the quadruple latch (SN5475) and decade counter (SN54L90) may be utilized to acquire and store the numeral to be displayed. The method shown is typical of a single stage and a number of methods are possible for distributing the BCD data from the decade counter to the quadruple latch.

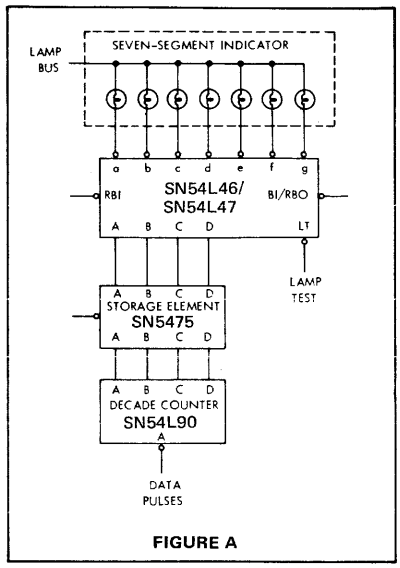

FIGURE A

n-digit display with leading and trailing-edge blanking (see Figure B)

This application demonstrates a method for driving seven-segment incandescent display indicators directly from the output of the SN54L46, or SN54L47 decoder with provisions for leading-edge and trailing-edge zero-blanking, intensity control, and lamp test.

Leading-edge and trailing-edge zero blanking is illustrated for a six-digit mixed integer with zero indications suppressed for the two most-significant decades (MSD) of the whole number and the two least-significant decades (LSD). This scheme causes the number to be displayed in its easily identified, common form. Blanking is accomplished by grounding RBI inputs of most-significant and least-significant decades and interconnecting the BI/BRO nodes of these two decades to the ripple-blanking inputs of the adjacent decades. This improves readability by inhibiting suppression of zeros occurring on either side of the decimal point. The ripple-blanking inputs of the decades on either side of the fixed decimal point are inhibited by connecting to a 5-volt d-c source.

9

Intensity control is accomplished at all six of the decoder/drivers by modulating the blanking input with a multivibrator. Best results are obtained with a modulation source in which the duty cycle can be varied. Individual drivers are required as they are wire-OR connected with the ripple blanking functions.

As the lamp-test input is only one load, any number of these (up to 20) may be driven from a single Series 54/74 circuit.

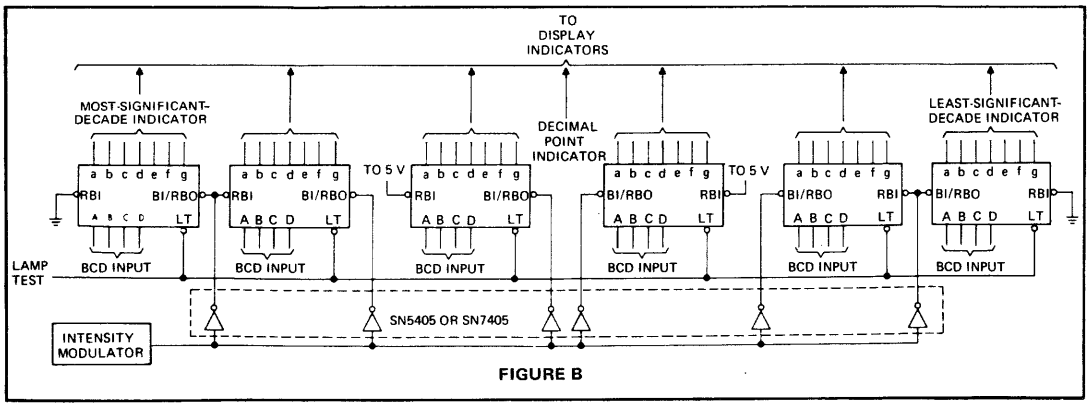

FIGURE B

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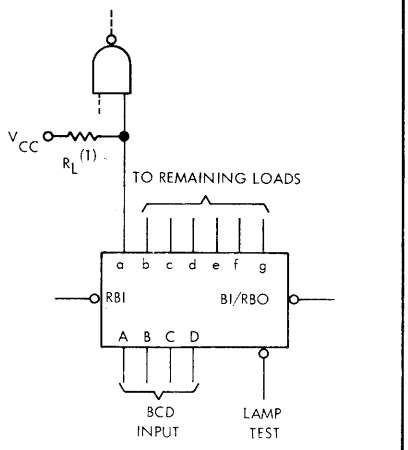
TYPICAL APPLICATION DATA

driving logic circuits (see Figure C)

These decoder/drivers may be used to drive other logic circuits. (See Figure C.) Value of the pull-up resistor (required on the open-collector outputs) may be calculated using the methods given for the SN54L01 open-collector NAND gate.



Pull-up resistor is required with open-collector outputs.

FIGURE C

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TEXAS INSTRUMENTS
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CIRCUIT TYPE SN74141
BCD-TO-DECIMAL DECODER/DRIVER

- Drives gas-filled cold-cathode indicator tubes directly
- Fully decoded inputs ensure all outputs are off for invalid codes
- Input clamping diodes minimize transmission-line effects
- Power dissipation typically 55 mW

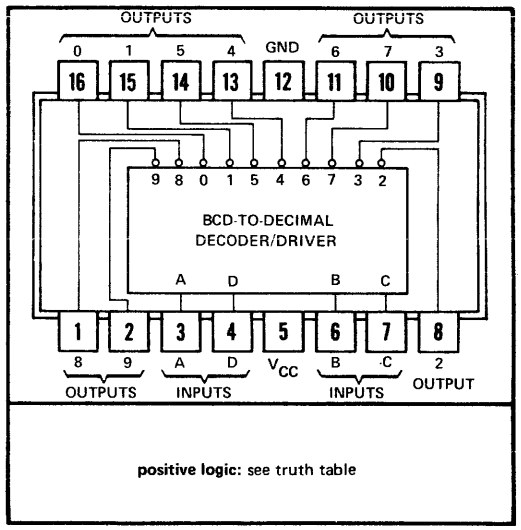
logic

TRUTH TABLE

INPUT				OUTPUT
D	C	B	A	ON†
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7
H	L	L	L	8
H	L	L	H	9
H	L	H	L	NONE
H	L	H	H	NONE
H	H	L	L	NONE
H	H	L	H	NONE
H	H	H	L	NONE
H	H	H	H	NONE

H = high level, L = low level
†All other outputs are off

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



†Pin assignments for these circuits are the same for all packages.

description

The SN74141 is a second-generation BCD-to-decimal decoder designed specifically to drive cold-cathode indicator tubes. This decoder demonstrates an improved capability to minimize switching transients in order to maintain a stable display.

Full decoding is provided for all possible input states. For binary inputs 10 through 15, all the outputs are off. Therefore the SN74141, combined with a minimum of external circuitry, can use these invalid codes in blanking leading- and/or trailing-edge zeros in a display as shown in the typical application data. The ten high-performance, n-p-n output transistors have a maximum reverse current of 50 microamperes at 55 volts.

Low-forward-impedance diodes are also provided for each input to clamp negative-voltage transitions in order to minimize transmission-line effects. Power dissipation is typically 55 milliwatts, which is about one-half the power requirement of earlier designs. The SN74141 is characterized for operation over the temperature range of 0°C to 70°C.

TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC}	7 V
Input voltage (see Note 1)	5.5 V
Current into any output (off-state)	2 mA
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage V_{CC} (see Note 1)	4.75	5	5.25	V
Output voltage (see Notes 1 and 2)			65	V
Operating free-air temperature range	0	25	70	°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the maximum voltage which should be applied to any output when it is in the off state.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage	1 and 2		2			V
V_{IL}	Low-level input voltage	1 and 2				0.8	V
$V_{O(on)}$	On-state output voltage	1	V_{CC} = MIN, I_O = 7 mA			2.5	V
$V_{O(off)}$	Off-state output voltage for input counts 0 thru 9	2	V_{CC} = MAX, I_O = 0.5 mA	60			V
$I_{O(off)}$	Off-state reverse current	2	V_{CC} = MAX, V_O = 55 V			50	μA
$I_{O(off)}$	Off-state reverse current for input counts 10 thru 15	2	V_{CC} = MAX, V_O = 30 V			5	μA
I_{IH}	High-level input current at A	3	V_{CC} = MAX, V_I = 2.4 V			40	μA
			V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IH}	High-level input current at B, C, or D	3	V_{CC} = MAX, V_I = 2.4 V			80	μA
			V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IL}	Low-level input current into A	4	V_{CC} = MAX, V_I = 0.4 V			−1.6	mA
I_{IL}	Low-level input current into B, C, or D					−3.2	mA
I_{CC}	Supply current	3	V_{CC} = MAX		16	25	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡This typical value is at V_{CC} = 5 V, T_A = 25°C.

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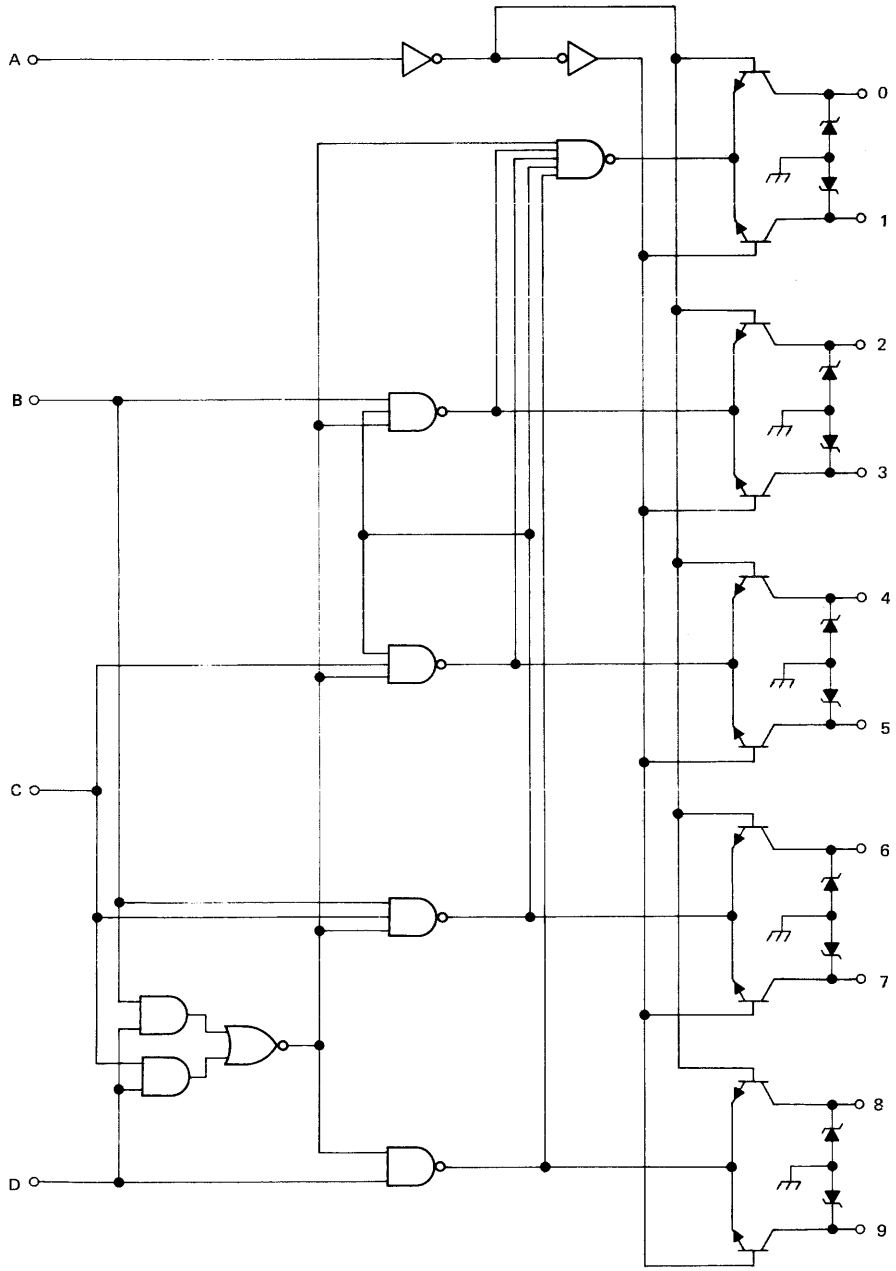
functional block diagram



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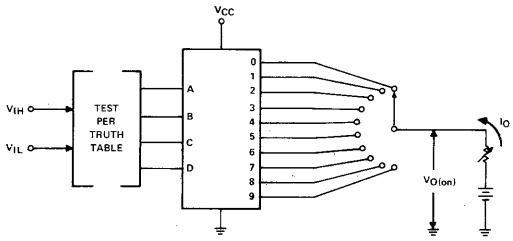
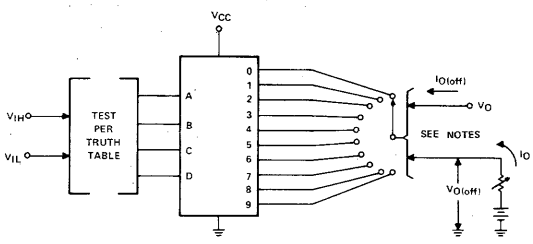
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§



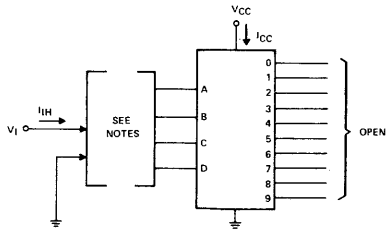
Each output is tested separately.

FIGURE 1–V_{IH}, V_{IL}, $V_{O(on)}$



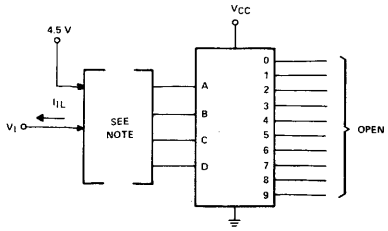
A. Each output is tested separately.
B. $V_{O(off)}$ is tested at I_O = 0.5 mA and $I_{O(off)}$ is tested at V_O = 55 V for all input counts. $I_{O(off)}$ is tested also at V_O = 30 V for input counts 10 through 15.

FIGURE 2–V_{IH}, V_{IL}, $I_{O(off)}$, $V_{O(off)}$



A. When testing I_{IH}, each input is tested separately with all other inputs grounded.
B. When testing I_{CC}, all inputs are grounded.

FIGURE 3–I_{IH}, I_{CC}



Each input is tested separately, with all other inputs at 4.5 V.

FIGURE 4–I_{IL}

§ Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

9

CIRCUIT TYPE SN74141
BCD-TO-DECIMAL DECODER/DRIVER

TYPICAL APPLICATION DATA

general

When these decoder/drivers are used in close proximity (on the same circuit board) with standard digital integrated circuits, care should be exercised to ensure that the impedance of the ground bus (including interconnections) is sufficiently low to absorb the normal energy levels resulting from switching the tube elements.

driving indicator tubes

As shown in figure A, the SN74141 requires no external components for driving cold-cathode indicator tubes. The versatility here is limited only by the system capability to control the data inputs.

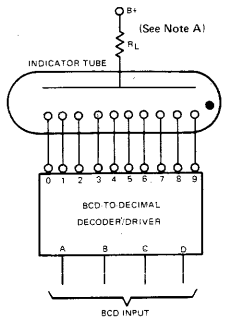


FIGURE A

A suggested method for blanking extraneous zeros is shown in figure B. Any input count above decimal 9 may be used for blanking. In the following application decimal 12 is used. When the most-significant bit (MSB) or the least-significant bit (LSB) is decimal 0(0000), that indicator is blanked while decimal 12 (binary 1100) is applied to the SN74141 inputs causing all the outputs to be off. If the MSB or LSB is decimal 0 and being blanked, this signal is gated with and blanks the next smaller digit. This scheme is easily expandable to n-digits.

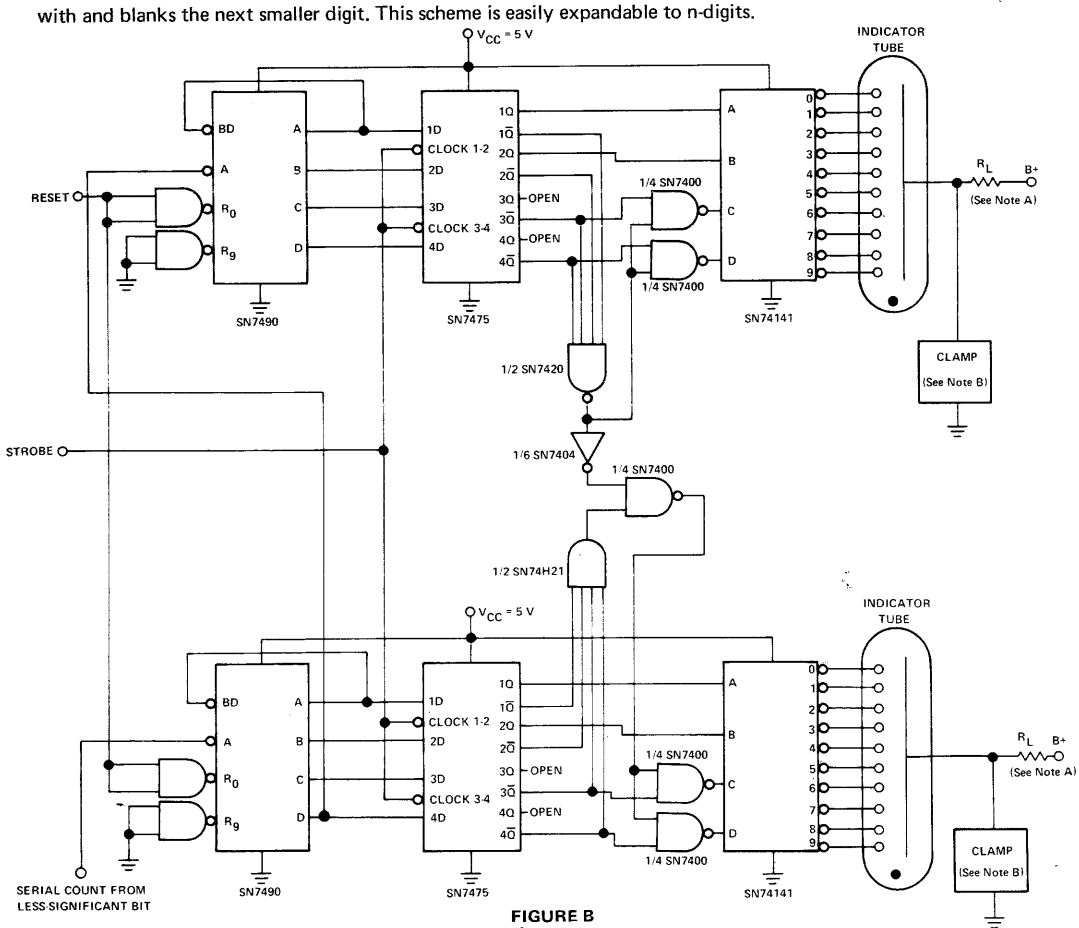


FIGURE B

NOTES: A. Values for B+ and R_L are as specified by the tube manufacturer.
B. Blanking is assured only if the anode of the indicator tube is clamped at 150 volts maximum.

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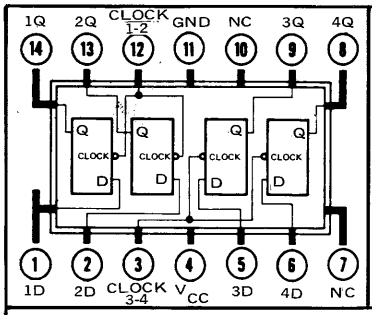
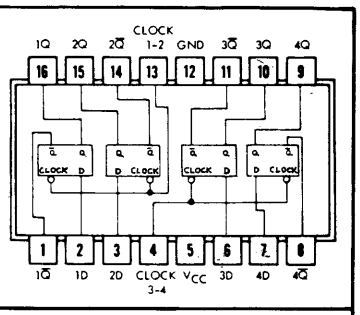
CIRCUIT TYPES SN5475, SN5477, SN54100, SN7475, SN7477, SN74100
8-BIT AND 4-BIT BISTABLE LATCHES

SN5477/SN7477
W FLAT PACKAGE
(TOP VIEW)



SN5475/SN7475
J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



positive logic: see truth table

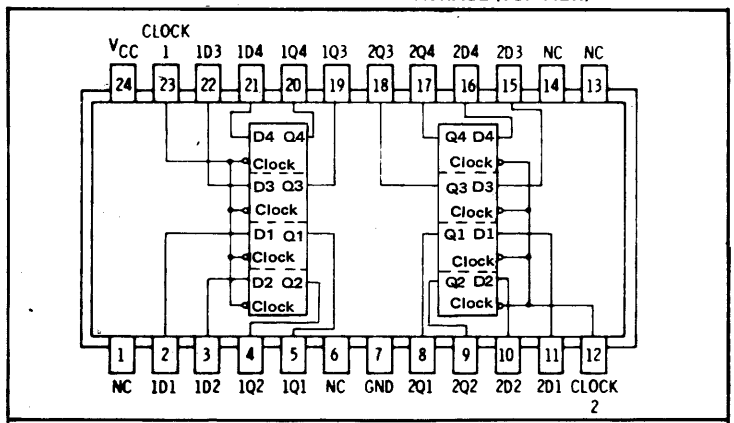
logic

TRUTH TABLE (Each Latch)	
t_n	t_{n+1}
D	Q
1	1
0	0

NOTES: 1. t_n = bit time before clock negative-going transition.
2. t_{n+1} = bit time after clock negative-going transition.

NC—No internal connection

SN54100/SN74100
J OR N DUAL-IN-LINE OR W FLAT PACKAGE (TOP VIEW)†



positive logic: see truth table

†Pin assigments for these circuits are the same for all packages

description

These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the clock is high, and the Q output will follow the data input as long as the clock remains high. When the clock goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the clock is permitted to go high.

The SN5475/SN7475 features complementary Q and $\overline{Q}$ outputs from a 4-bit latch, and is available in the 16-pin packages. For higher component density applications the SN5477/SN7477 4-bit latch is available in the 14-pin flat package. The SN54100/SN74100 features two independent quadruple latches in a single 24-pin dual-in-line package.

These circuits are completely compatible with all popular TTL or DTL families. Typical power dissipation is 40 milliwatts per latch. The Series 54 circuits are characterized for operation over the full military temperature range of −55°C to 125°C and Series 74 circuits are characterized for operation from 0°C to 70°C.

absolute maximum ratings (over operating temperature range unless otherwise noted)

Supply Voltage, V_{CC} (See Note 3) . . . . . 7 V
Input Voltage, V_{in} (See Notes 3 and 4) . . . . . 5.5 V
Operating Free-Air Temperature Range: SN5475 Circuits . . . . . −55°C to 125°C
SN7475 Circuits . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

NOTES: 3. These voltage values are with respect to network ground terminal.
4. Input signals must be zero or positive with respect to network ground terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 3): SN5475, SN5477, SN54100	4.5	5	5.5	V
SN7475, SN7477, SN74100	4.75	5	5.25	V
Normalized Fan-Out From Outputs			10	

NOTE: 3. These voltages are with respect to network ground terminal.

electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 level at any input terminal	1			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 level at any input terminal	2					0.8	V
$V_{out(1)}$	Logical 1 output voltage	1 and 2	V_{CC} = MIN, I_{load} = −400 μA		2.4			V
$V_{out(0)}$	Logical 0 output voltage	1 and 2	V_{CC} = MIN, I_{sink} = 16 mA				0.4	V
$I_{in(0)}$	Logical 0 level input current at D	3	V_{CC} = MAX, V_{in} = 0.4 V				−3.2	mA
$I_{in(0)}$	Logical 0 level input current at clock	3	V_{CC} = MAX,	SN5475, SN5477, SN7475, SN7477			−6.4	mA
				SN54100, SN74100			−12.8	mA
$I_{in(1)}$	Logical 1 level input current at D	3	V_{CC} = MAX, V_{in} = 2.4 V				80	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at clock	3	V_{CC} = MAX,	SN5475, SN5477, SN7475, SN7477			160	μA
			V_{in} = 2.4 V,	SN54100, SN74100			320	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current§	4	V_{CC} = MAX, V_{out} = 0	SN5475, SN5477, SN54100	−20		−57	mA
				SN7475, SN7477, SN74100	−18		−57	mA
I_{CC}	Supply current	5	V_{CC} = MAX,	SN5475, SN5477		32	46	mA
				SN54100		64	92	mA
				SN7475, SN7477		32	53	mA
				SN74100		64	106	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

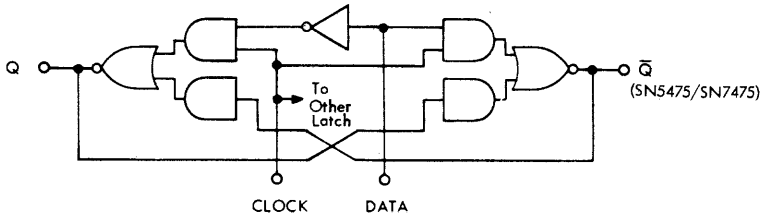
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

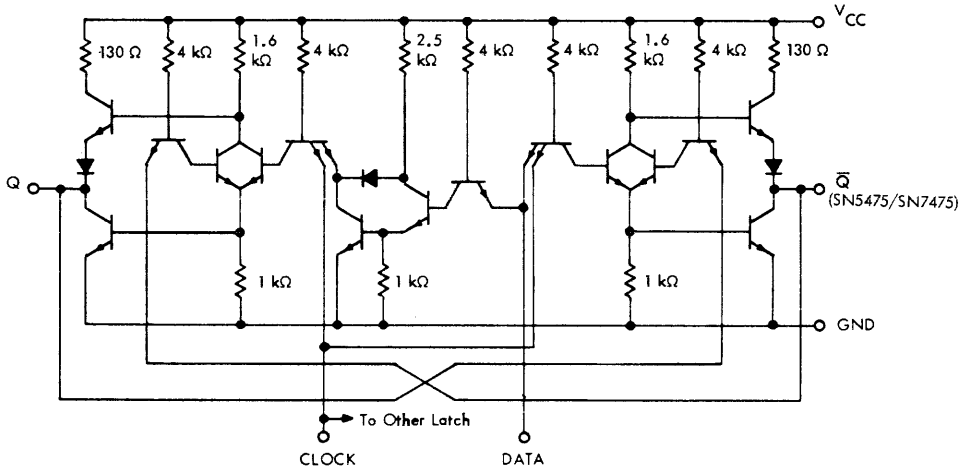
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{setup1}	Minimum logical 1 level input setup time at D input	6	C_L = 15 pF, R_L = 400 Ω		7	20	ns
t_{setup0}	Minimum logical 0 level input setup time at D input	6	C_L = 15 pF, R_L = 400 Ω		14	20	ns
t_{hold1}	Maximum logical 1 level input hold time required at D input	6	C_L = 15 pF, R_L = 400 Ω	0	15¶		ns
t_{hold0}	Maximum logical 0 level input hold time required at D input	6	C_L = 15 pF, R_L = 400 Ω	0	6¶		ns
$t_{pd1(D-Q)}$	Propagation delay time to logical 1 level from D input to Q output	6	C_L = 15 pF, R_L = 400 Ω		16	30	ns
$t_{pd0(D-Q)}$	Propagation delay time to logical 0 level from D input to Q output	6	C_L = 15 pF, R_L = 400 Ω		14	25	ns
$t_{pd1(D-\bar{Q})}$	Propagation delay time to logical 1 level from D input to $\bar{Q}$ output (SN5475, SN7475)	6	C_L = 15 pF, R_L = 400 Ω		24	40	ns
$t_{pd0(D-\bar{Q})}$	Propagation delay time to logical 0 level from D input to $\bar{Q}$ output (SN5475, SN7475,	6	C_L = 15 pF, R_L = 400 Ω		7	15	ns
$t_{pd1(C-Q)}$	Propagation delay time to logical 1 level from clock input to Q output	6	C_L = 15 pF, R_L = 400 Ω		16	30	ns
$t_{pd0(C-Q)}$	Propagation delay time to logical 0 level from clock input to Q output	6	C_L = 15 pF, R_L = 400 Ω		7	15	ns
$t_{pd1(C-\bar{Q})}$	Propagation delay time to logical 1 level from clock input to $\bar{Q}$ output (SN5475, SN7475)	6	C_L = 15 pF, R_L = 400 Ω		16	30	ns
$t_{pd0(C-\bar{Q})}$	Propagation delay time to logical 0 level from clock input to $\bar{Q}$ output (SN5475, SN7475)	6	C_L = 15 pF, R_L = 400 Ω		7	15	ns

¶ These typical times indicate that period occurring prior to the fall of clock pulse (t_0) below 1.5 V when data at the D input will still be recognized and stored.

functional block diagram (each latch)



schematic (each latch)

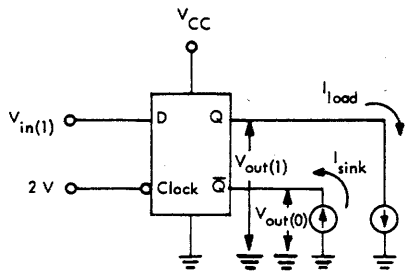


Component values shown are nominal.

9

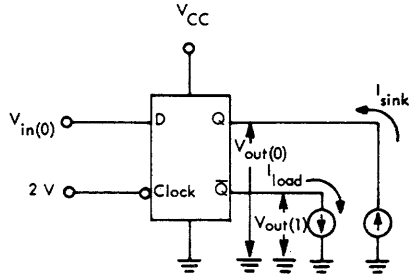
PARAMETER MEASUREMENT INFORMATION

d-c test circuits †



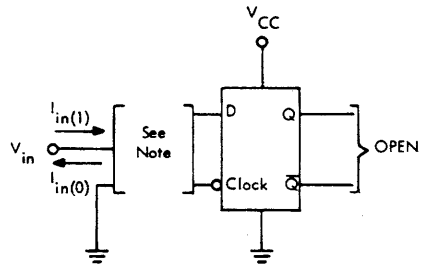
1. Each latch is tested separately.

FIGURE 1



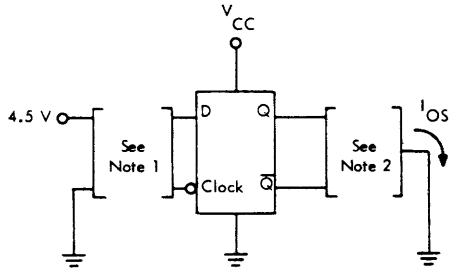
1. Each latch is tested separately.

FIGURE 2



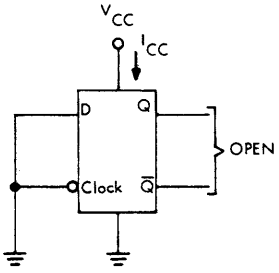
1. Each input is tested separately.
2. When testing $I_{in(1)}$ at D ground clock.
3. When testing $I_{in(1)}$ at clock ground all D inputs.

FIGURE 3



1. Input conditions are in accordance with truth table.
2. Each latch and each output is tested separately.

FIGURE 4



1. All latches are tested simultaneously.

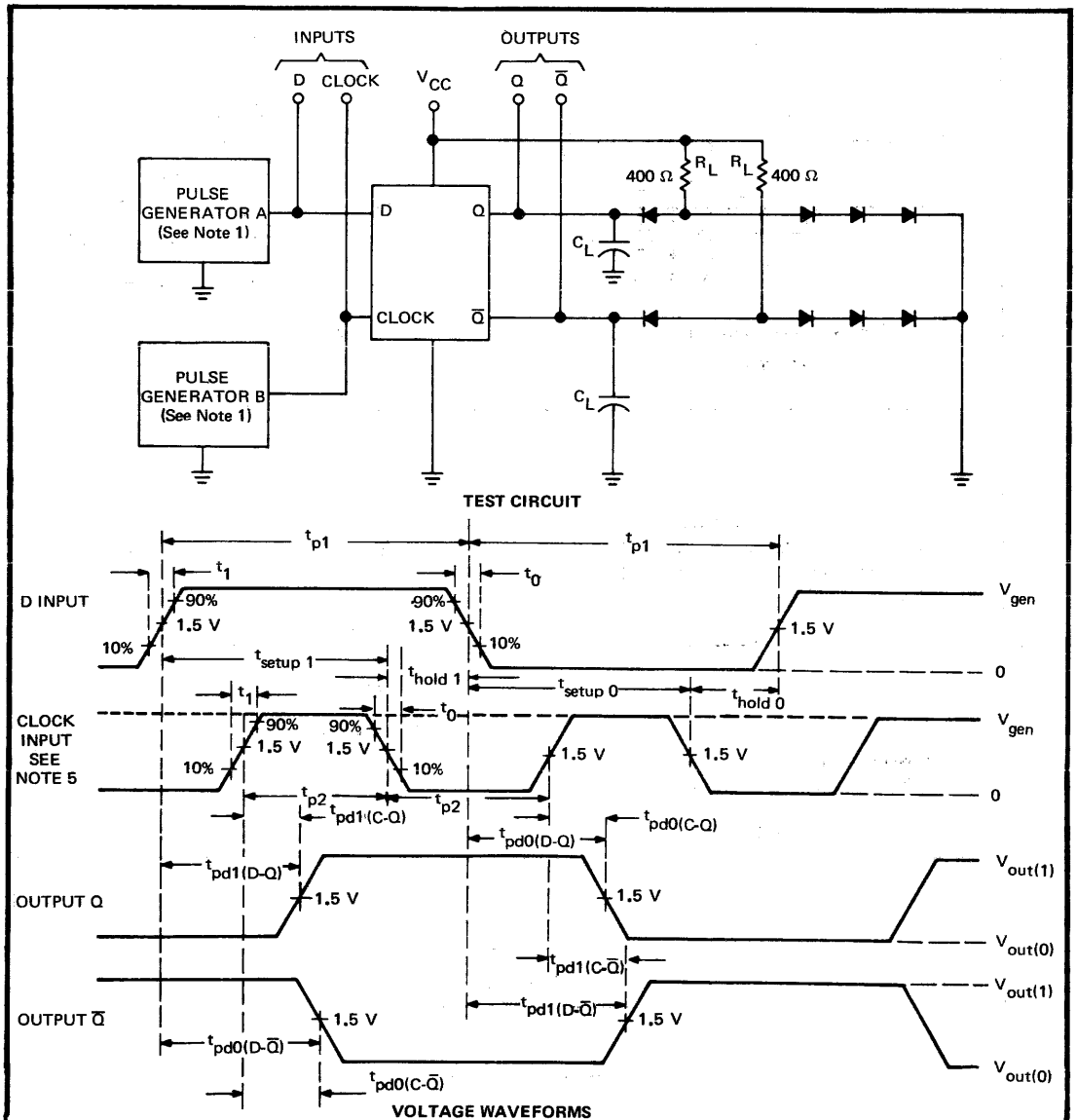
FIGURE 5

† Arrows indicate actual direction of current flow. Complementary $\overline{Q}$ outputs are available on the SN5475/SN7475.

9

PARAMETER MEASUREMENT INFORMATION

switching characteristics†



NOTES:
1. The pulse generators have the following characteristics: V_{gen} = 3 V, $t_1 = t_0 \leqslant 10$ ns, and $Z_{out} \approx 50\ \Omega$. For pulse generator A t_{p1} = 1 μs and PRR = 500 kHz. For pulse generator B, t_{p2} = 500 ns and PRR = 1 MHz. Positions of D-input and clock-input pulses are varied with respect to each other to verify setup and hold times.
2. Each latch is tested separately.
3. C_L includes probe and jig capacitance.
4. All diodes are 1N3064.
5. When measuring $t_{pd1(D-Q)}$ and $t_{pd0(D-Q)}$ (or $t_{pd0(D-\overline{Q})}$ and $t_{pd1(D-\overline{Q})}$ for the SN5475/SN7475), clock input must be held at logical 1.

FIGURE 6 – SWITCHING TIMES

†Complementary Q outputs are on the SN5475/SN7475 only.

TYPICAL APPLICATION

temporary storage of binary data

This application demonstrates the use of the SN7475 bistable latch as a temporary storage of binary-coded decimal data, from the SN7490 decade counter, which is to be decoded by the SN7441 decoder/driver. Temporary storage is desirable at this point for two reasons:

a. At counting frequencies above several cycles per second, it is sometimes desirable to eliminate the flicker on the display tube caused by reading an input count which is too fast to be recognized.

b. During the time that the latch is storing information the decade counter may start acquiring data for the next display.

A typical sequence of operation is illustrated (see Figure 7):

1. During t_1, reset decade counter to 0. At end of t_1, indicator will display "0".
2. During t_2, count BCD 3 at output of SN7490. Indicator still displays "0".
3. At start of t_3, indicator will display "3". At end of t_3, BCD 3 is committed to memory by SN7475 and the SN7490 may begin counting again.
4. During t_4, reset decade counter to 0 and count BCD 5 at output of SN7490. Indicator still displays "3".
5. At start of t_5, indicator will display "5". At end of t_5, BCD 5 is committed to memory by SN7475 and the SN7490 is released.

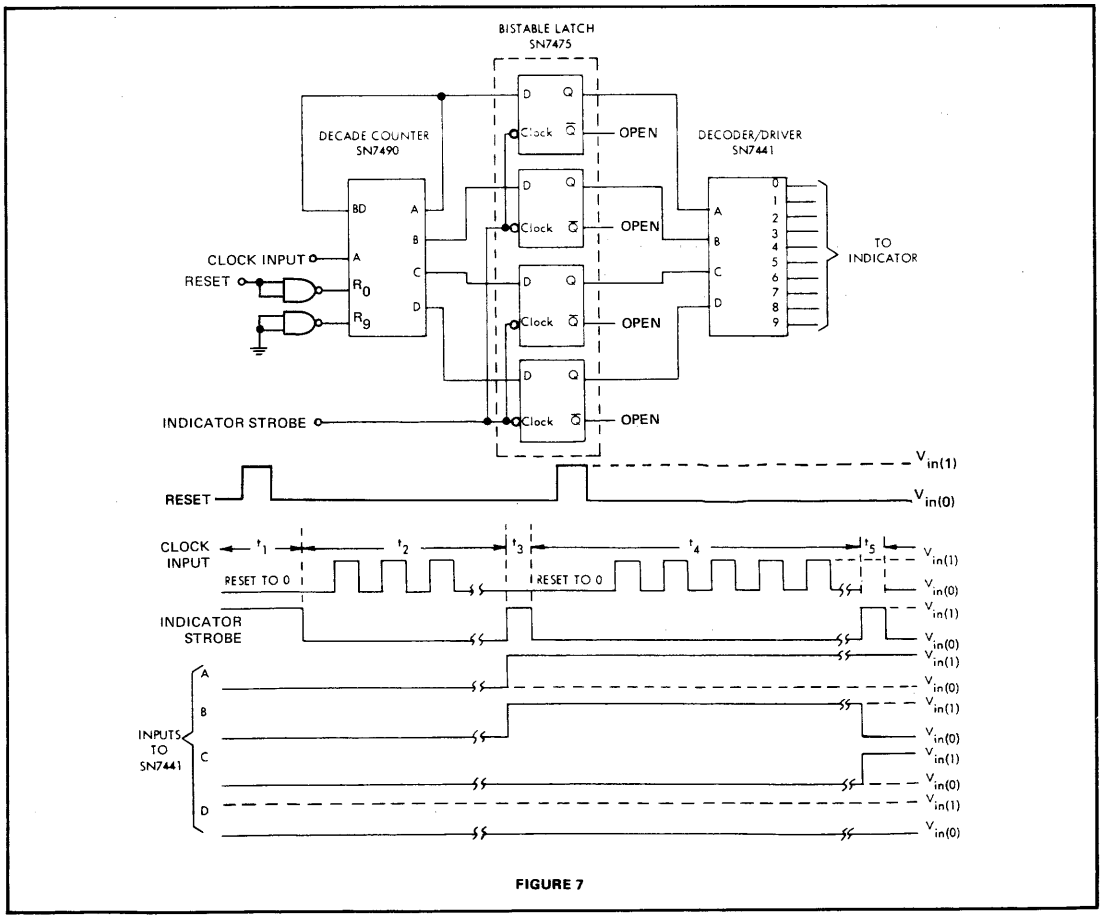


FIGURE 7

TYPICAL APPLICATION

dual D-type master-slave flip-flop

This application demonstrates the use of the SN7475 as a dual D-type master-slave flip-flop, provided that two-phase clocking is permissible. Each of the D-type flip-flops are formed by merely interconnecting the Q output of one of the latches (which serves as the master) to the data input of another latch (which serves as the slave). Each of these interconnected latches must have a separate clock line; therefore if a dual D-type master-slave flip-flop is constructed from a single package (see Figure 8) they must be operated synchronously.

A typical transfer of data is illustrated. Note that after the start of t_1 the data input is released to acquire new information as the master section has "locked up" the original data after clock pulse A_1. At the start of t_2 the data "locked up" in the master is transferred to the output, and at the end of t_2 (and for the duration of t_3) the slave retains the original data.

This type of flip-flop is desirable in applications where speed is not a primary requirement and where the additional clock skew, resulting from this delay between the two clock pulses, affords greater system reliability.

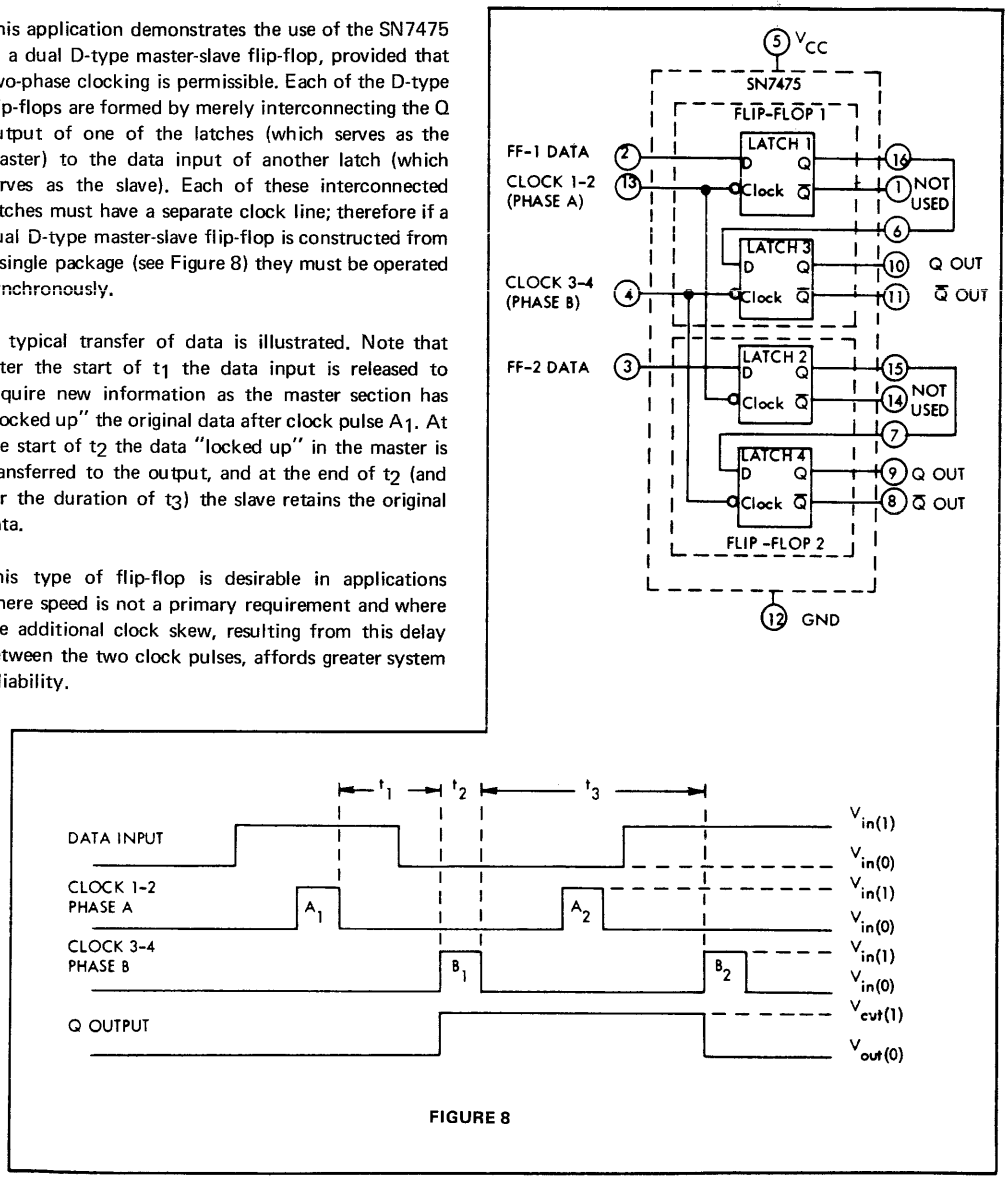


FIGURE 8

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TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

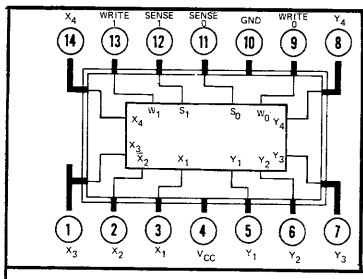
CIRCUIT TYPES SN5481, SN5484, SN7481, SN7484
16-BIT ACTIVE-ELEMENT MEMORIES

description

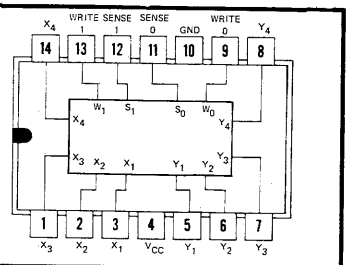
The 16-bit active-element memory is a monolithic, high-speed, transistor-transistor-logic (TTL) array of 16 flip-flops, and two write amplifiers interconnected to form a "scratch-pad" memory with direct-address and non-destructive read-out.

The flop-flops are arranged in a 4-by-4 matrix with each flip-flop representing one bit of 16 words. Four X-address lines and four Y-address lines permit the address of one bit at a time. Each flip-flop, composed of two cross-coupled 3-emitter transistors, is used to store one bit. To determine if a logical 1 or 0 has been stored, it is necessary to know which one of the two flip-flop transistors is conducting. One emitter of each of these transistors serves as the sensing output. All 16 of the logical 1 sensing outputs are connected to the sense logic 1 (S_1) amplifier input and all 16 of the logical0 sensing outputs are connected to the sense logical 0 (S_0) amplifier input. The two remaining emitters on each transistor are used to complete the matrix connections necessary for the X- and Y-address lines. Address line inputs are normally held low (logical 0) and currents from all conducting flip-flop transistors flow out these address lines.

SN5481/SN7481 CIRCUITS
W FLAT PACKAGE (TOP VIEW)

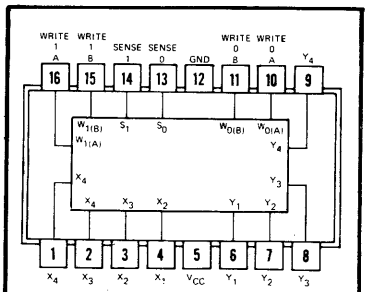


SN5481/SN7481 CIRCUITS
J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: see logic diagram

SN5484/SN7484 CIRCUITS
J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



positive logic: see logic diagram

†Pin assignments for these circuits are the same for all packages.

To address a flip-flop both the X- and Y-address lines associated with that flip-flop are taken to a logical 1 voltage. Due to the matrix nature of the circuit, at least one address line of all flip-flops except the one being addressed will continue to remain at a logical 0 level and no change will occur on those flip-flops. But, in the addressed flip-flop, the current in the conducting transistor diverts from the address lines to the appropriate sense line and then to one of the sense amplifiers. Thus, either the sense amplifier associated with a logical 1 or the sense amplifier associated with a logical 0 is activated. When this occurs, the output of the activated sense amplifier drops from a logical 1 to a logical 0 level. The memory is non-destructive as the states of the flip-flops are not disturbed during sensing. The memory is volatile and information will be lost if the supply voltage is removed.

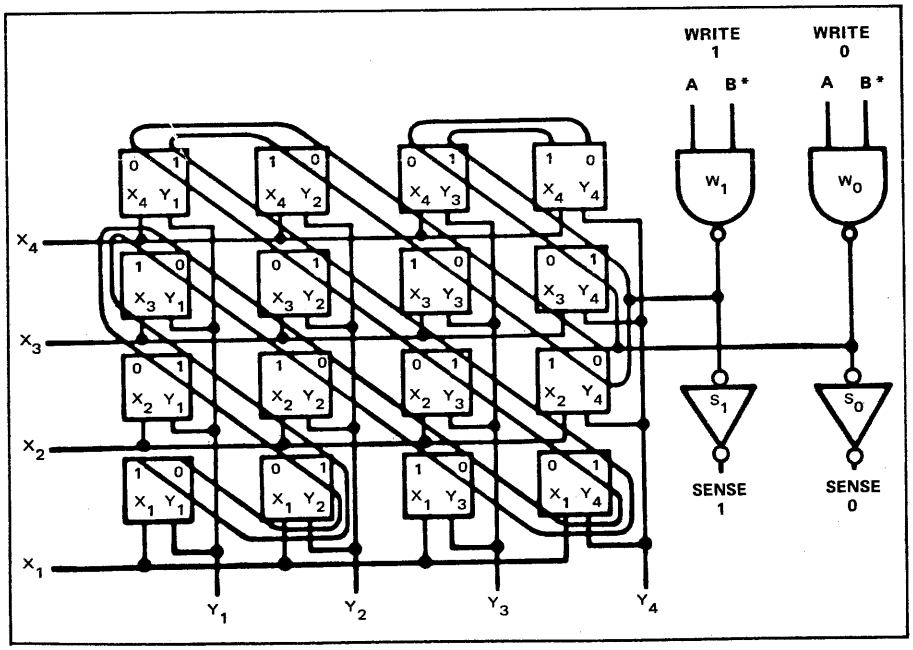
description (continued)

To store new information in a flip-flop, it is necessary to address it and apply logical 1 voltage to the appropriate write amplifier input. (The SN5484/SN7484 circuit has gated write-amplifier inputs). The output of the write amplifier responds by dropping to a logical 0 level. Since all logical 0 sense lines are connected to the output of the logical 0 write amplifier and all logical 1 sense lines are connected to the output of the logical 1 write amplifier, a logical 0 voltage on the output of a write amplifier will apply the same voltage to emitters of all flip-flop transistors connected to that amplifier. In all flip-flops except the one being addressed, this low voltage has no effect since at least one other emitter on each of the flip-flop transistors is held low by the address lines. But two possibilities exist with the flip-flop that is addressed. The flip-flop may already be in the desired state, in which case no change occurs. But if the flip-flop must be changed from one state to the other, the low voltage applied to the emitter of the transistor which is not conducting turns that transistor on causing the other transistor to turn off.

Since the connection between the output of the write amplifier and the sense line is common to the input of the sense amplifier, the memory cannot be used to provide information on the state of a bit while the write amplifiers are activated.

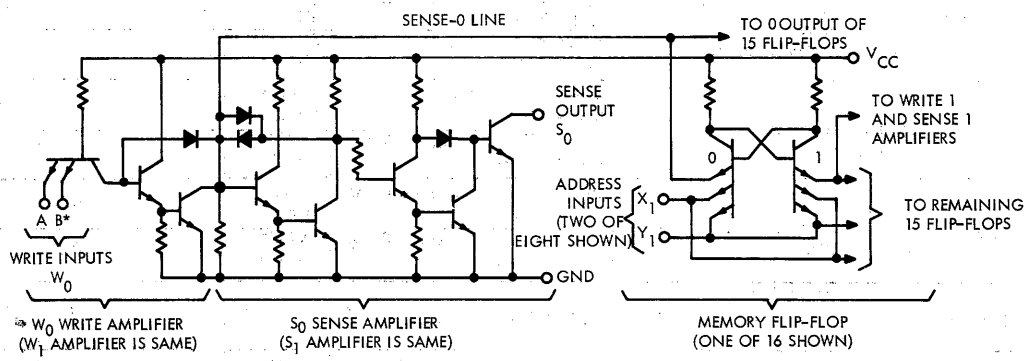
A number of active element memories may be paralleled to form the desired matrix size (number of words) and to form the desired word length (number of bits). Standard TTL circuitry, employed for the address line inputs, write amplifier inputs, and the saturating output transistors, provides complete TTL and DTL compatibility and maintains typical noise margins of one volt. Average power dissipation is 275 milliwatts (typical), and the open-collector outputs may be wire-OR connected to similar outputs. Internal circuitry of the write and sense amplifiers are operated within their linear range to improve speed. Sensing propagation delay times are typically 20 nanoseconds when operated at full fan-out and 30 picofarads of circuit capacitance.

logic diagram



*Gated inputs (as shown) are available on SN5484/SN7484 only.
The SN5481/SN7481 has one W_0 and one W_1 input.

schematic diagram



* Gated inputs (as shown) are available on SN5484/SN7484 only. The SN5481/SN7481 has one W_0 and one W_1 input.

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1)	7 V
Input Voltage V_{in} (See Notes 1 and 2)	5.5 V
Operating Free-Air Temperature Range: SN5481, SN5484 Circuits	−55°C to 125°C
SN7481, SN7484 Circuits	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

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recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1): SN5481, SN5484 Circuits	4.5	5	5.5	V
SN7481, SN7484 Circuits	4.75	5	5.25	V
Width of Write Pulse, $t_{p(write)}$ (See Figure 11)	25			ns
Address Lines Input Setup Time, t_{setup} (See Figure 11)	0			ns

NOTES: 1. These voltage values are with respect to ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)AW}$ or $V_{in(1)AS}$	Input voltage required at X or Y address lines to ensure writing or sensing	1	V_{CC} = MIN, $V_{out(0)} \leqslant 0.4$ V, I_{sink} = 20 mA	SN5481, SN5484	2.1			V
			V_{CC} = MIN, $V_{out(0)} \leqslant 0.4$ V, I_{sink} = 40 mA	SN7481, SN7484	2.1			V
$V_{in(1)W}$	Input voltage required at W_0 or W_1 inputs to ensure writing	1	V_{CC} = MIN, $V_{out(0)} \leqslant 0.4$ V, I_{sink} = 20 mA	SN5481, SN5484	2			V
			V_{CC} = MIN, $V_{out(0)} \leqslant 0.4$ V, I_{sink} = 40 mA	SN7481, SN7484	2			V
$V_{in(0)A\overline{W}}$	Input voltage required at X or Y address lines to prevent writing	2	V_{CC} = MIN, $V_{out(0)} \leqslant 0.4$ V, I_{sink} = 20 mA	SN5481, SN5484			0.8	V
			V_{CC} = MIN, $V_{out(0)} \leqslant 0.4$ V, I_{sink} = 40 mA	SN7481, SN7484			0.8	V
$V_{in(0)A\overline{S}}$	Input voltage required at X or Y address lines to prevent sensing	3	V_{CC} = MIN, $I_{out(1)}$ = 250 μA	V_{out} = 5.5 V			1	V
$V_{in(0)\overline{W}}$	Input voltage required at W_0 or W_1 to prevent writing	1	V_{CC} = MIN, $V_{out(0)} \leqslant 0.4$ V, I_{sink} = 20 mA	SN5481, SN5484			1	V
			V_{CC} = MIN, $V_{out(0)} \leqslant 0.4$ V, I_{sink} = 40 mA	SN7481, SN7484			1	V
$V_{out(1)}$	Logical 1 output voltage	3	V_{CC} = MIN, $I_{out(1)}$ = 250 μA		5.5			V
$V_{out(0)}$	Logical 0 output voltage (on level)	1 and 2	V_{CC} = MIN, I_{sink} = 20 mA	SN5481, SN5484			0.4	V
			V_{CC} = MIN, I_{sink} = 40 mA	SN7481, SN7484			0.4	V
$I_{in(0)}$	Logical 0 level input current at write 1 and write 0 (each input)	4	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(0)}$	Logical 0 level input current at all X or all Y address lines	5	V_{CC} = MAX, V_{in} = 0.4 V				−11	mA
$I_{in(1)}$	Logical 1 level input current at write 1 and write 0 (each input)	6	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at each X and each Y address line	6	V_{CC} = MAX, V_{in} = 4.5 V				400	μA
			V_{CC} = MAX, V_{in} = 5.5 V				3	mA
I_{CC}	Supply current	6	V_{CC} = MAX	SN5481, SN5484		55	78	mA
				SN7481, SN7484		55	91	mA

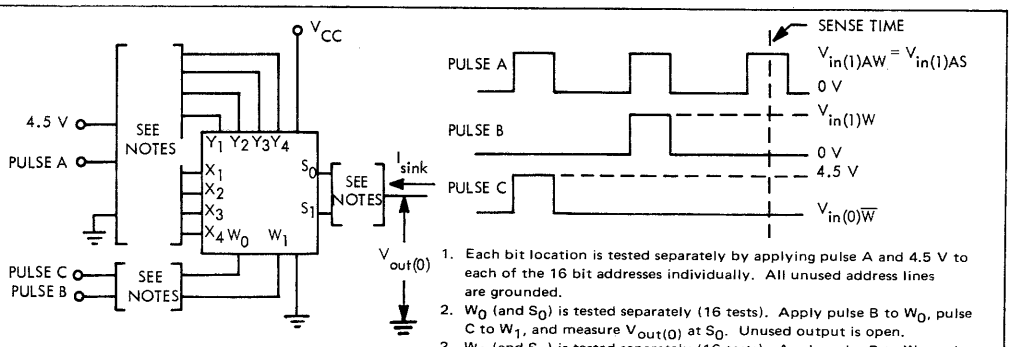
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics V_{CC} = 5 V, T_A = 25°C

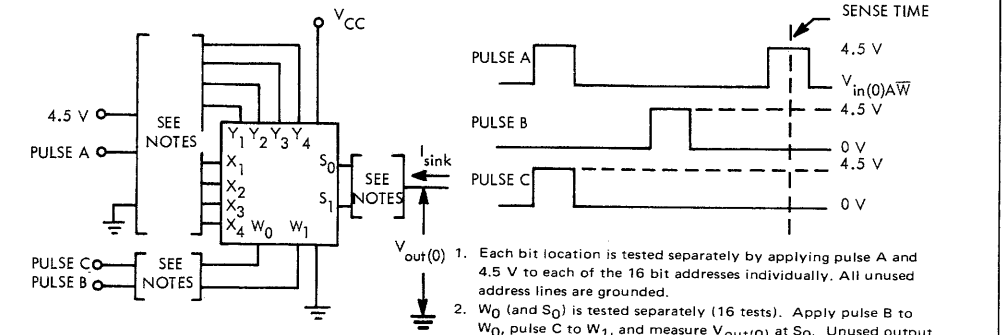
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{WR}	Write recovery time	7	C_L = 15 pF, X_1 - Y_1 location addressed		30	60	ns
t_{pd0}	Propagation delay time to logical 0 level from address-line inputs to S_0 or S_1 outputs	7	C_L = 15 pF, X_1 - Y_1 location addressed		22	45	ns
			C_L = 200 pF, X_1 - Y_1 location addressed		27	55	ns
t_{pd1}	Propagation delay time to logical 1 level from address-line inputs to S_0 or S_1 outputs	7	C_L = 15 pF, X_1 - Y_1 location addressed		15	25	ns
			C_L = 200 pF, X_1 - Y_1 location addressed		20	35	ns
t_{pd0}	Propagation delay time to logical 0 level from address-line inputs to S_0 or S_1 outputs	7	C_L = 15 pF, X_1 through X_4 and Y_1 locations addressed		20	30	ns

d-c test circuits† PARAMETER MEASUREMENT INFORMATION



1. Each bit location is tested separately by applying pulse A and 4.5 V to each of the 16 bit addresses individually. All unused address lines are grounded.
2. W_0 (and S_0) is tested separately (16 tests). Apply pulse B to W_0, pulse C to W_1, and measure $V_{out(0)}$ at S_0. Unused output is open.
3. W_1 (and S_1) is tested separately (16 tests). Apply pulse B to W_1, pulse C to W_0, and measure $V_{out(0)}$ at S_1. Unused output is open.
4. For the SN5484/SN7484, each of the two W_0 or two W_1 inputs are tested separately. Apply 4.5 V to unused W_0 or W_1 inputs.

FIGURE 1



1. Each bit location is tested separately by applying pulse A and 4.5 V to each of the 16 bit addresses individually. All unused address lines are grounded.
2. W_0 (and S_0) is tested separately (16 tests). Apply pulse B to W_0, pulse C to W_1, and measure $V_{out(0)}$ at S_0. Unused output is open.
3. W_1 (and S_1) are tested separately (16 tests). Apply pulse B to W_1, pulse C to W_0, and measure $V_{out(0)}$ at S_1. Unused output is open.
4. For the SN5484/SN7484, each of the two W_0 or two W_1 inputs are tested separately. Apply 4.5 V to unused W_0 or W_1 inputs.

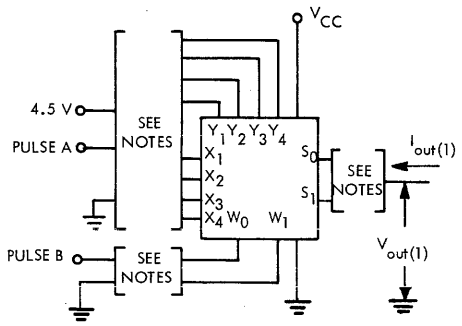
FIGURE 2

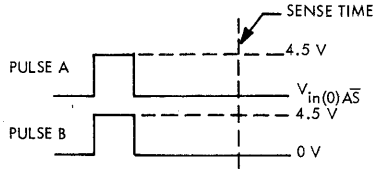
†Arrows indicate actual direction of current flow.

9

PARAMETER MEASUREMENT INFORMATION

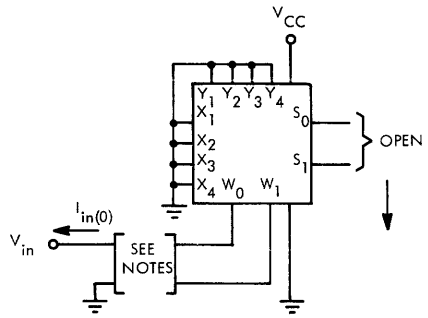
d-c test circuits† (continued)





1. Each bit location is tested separately by applying pulse A and 4.5 V to each of the 16 bit addresses individually. All unused address lines are grounded.
2. W_0 (and S_0) is tested separately (16 tests). Apply pulse B to W_0, ground W_1, and measure $V_{out(1)}$ at S_0. Unused output is open.
3. W_1 (and S_1) is tested separately (16 tests). Apply pulse B to W_1, ground W_0, and measure $V_{out(1)}$ at S_1. Unused output is open.
4. For the SN5484/SN7484, each of the two W_0 or two W_1 inputs are tested separately. Apply 4.5 V to the unused input of the gate under test and ground both inputs of the unused gate.

FIGURE 3



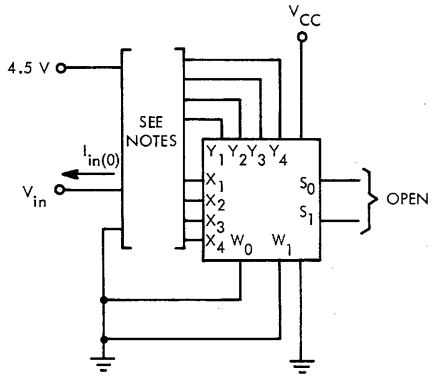
1. Each input is tested separately.
2. All unused inputs are grounded.

FIGURE 4

† Arrows indicate actual direction of current flow.

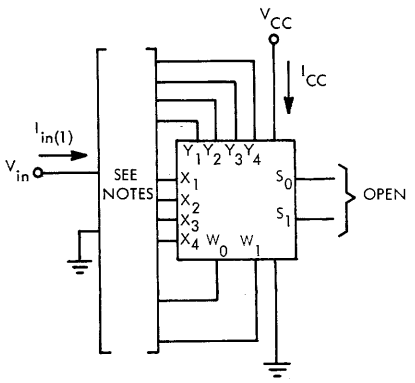
PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



1. Each X input is tested separately with the other three X inputs grounded and 4.5 V applied to all Y inputs.
2. Each Y input is tested separately with the other three Y inputs grounded and 4.5 V applied to all Y inputs.
3. For the SN5484/SN7484, both W_0 and both W_1 inputs are grounded.

FIGURE 5



1. Each input is tested separately for $I_{in(1)}$ with all unused inputs grounded.
2. When measuring I_{CC} all inputs are grounded.

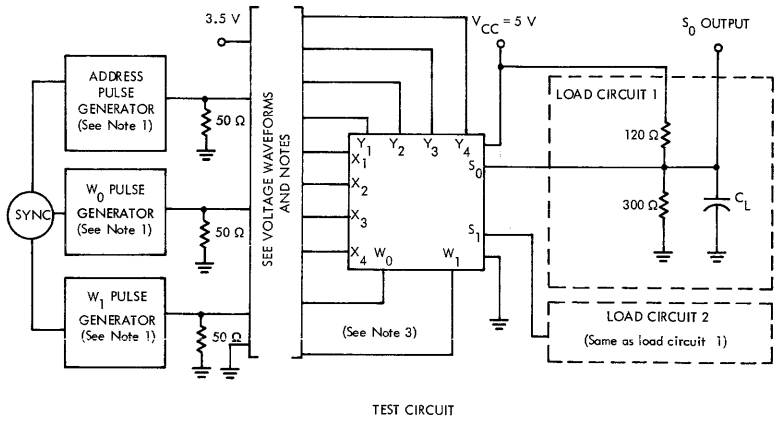
FIGURE 6

† Arrows indicate actual direction of current flow.

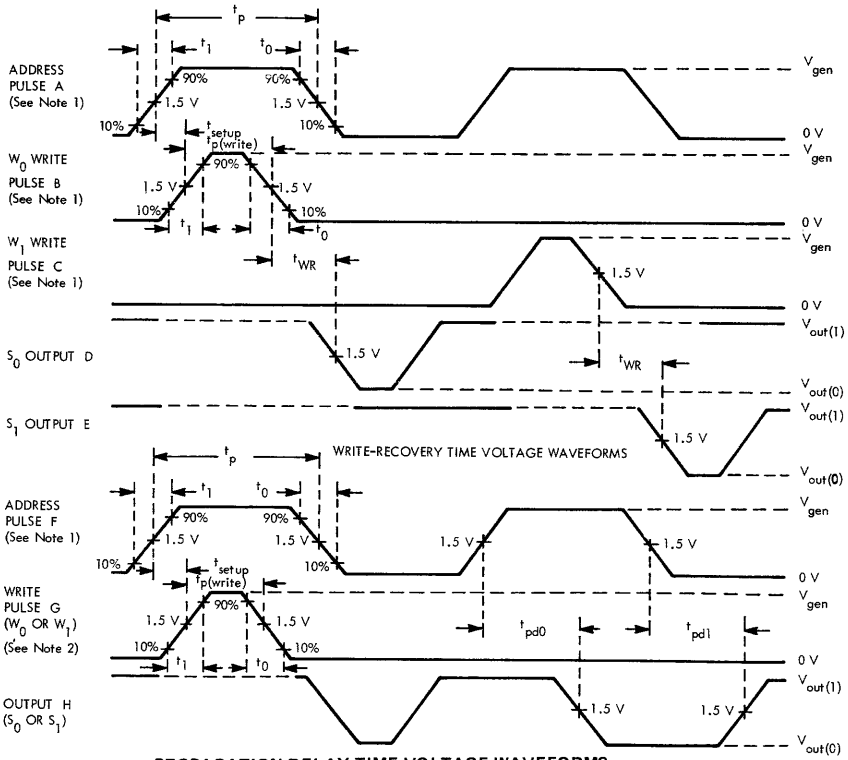
9

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



PROPAGATION DELAY TIME VOLTAGE WAVEFORMS

NOTES: 1. The pulse generators have the following characteristics: V_{gen} = 3 V, $t_1 = t_0$ = 10 ns, t_{setup} = 0 to 10 ns. For the address pulse generator, t_p = 100 ns and PRR = 2 MHz. For the W_0 and W_1 pulse generators, t_p = 25 ns and PRR = 1 MHz.

2. C_L includes probe and jig capacitance.

3. For the SN5484/SN7484, unused W_0 and W_1 inputs are 3.5 V.

FIGURE 7 – SWITCHING CHARACTERISTICS

TYPICAL APPLICATIONS

This application demonstrates use of the 16-bit active element memory to form a high-speed, direct-address, scratch-pad memory having a storage capability of m-words (in multiples of 16) of n-bit length. For purposes of this discussion, a memory is illustrated which will store 64 words each having a length of 8-bits. See Figure A. This storage capability may be increased or decreased using the patterns shown.

In this example, each of the planes consist of four 16-bit memory circuits connected in an 8-by-8 matrix. This organization provides 64 addresses (words) of 8-bits (word length) or a total bit capability of 512 bits (64 X 8).

Each bit plane (B_0 through B_7) is formed by paralleling the W_0, W_1 inputs, S_0, S_1 outputs, and completing the X-Y matrix connections. The matrix is completed by paralleling the X lines of Circuits A-B and C-D and the Y lines of A-C then B-D, to form the 64 addresses of plane B_0. Two pull-up resistors, one for S_0 and one for S_1, should be provided for wired-OR outputs. The other seven planes are identical to B_0.

The X and Y lines of the eight planes are paralleled so that all bits of each word are addressed simultaneously. Addressing of a particular word is accomplished by the X-Y decoder/drivers. For this particular example, the decoder could be a 1-of-8 decoder (see SN7442 and SN7444 applications) and the drivers may consist of discrete transistors, each capable of supplying current for 16 address inputs. A number of decoding/driving schemes are possible.

The SN5484/SN7484 has gated W_0 and W_1 inputs which may be used to perform the write enable function. External gating may be employed if enabling functions are required with the SN5481/SN7481.

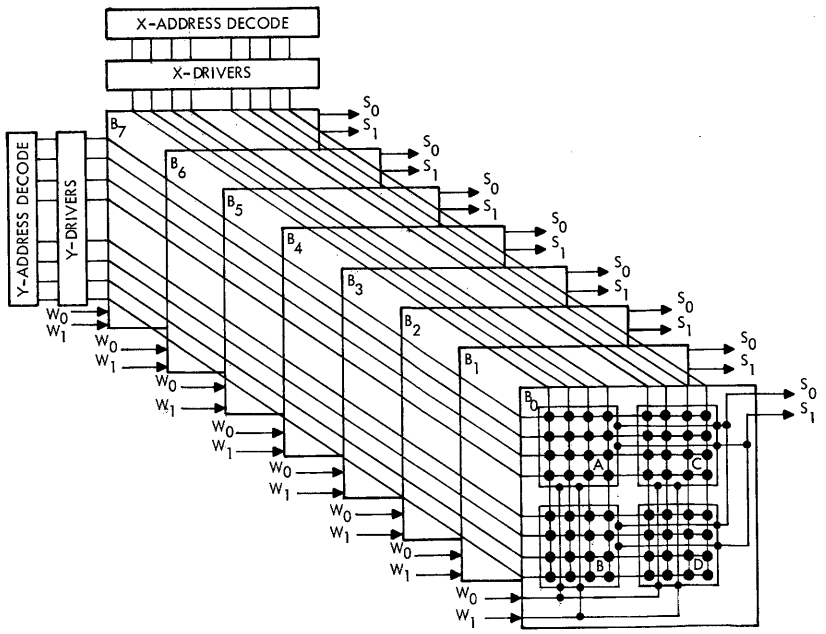


FIGURE A – TYPICAL MEMORY ORGANIZATION

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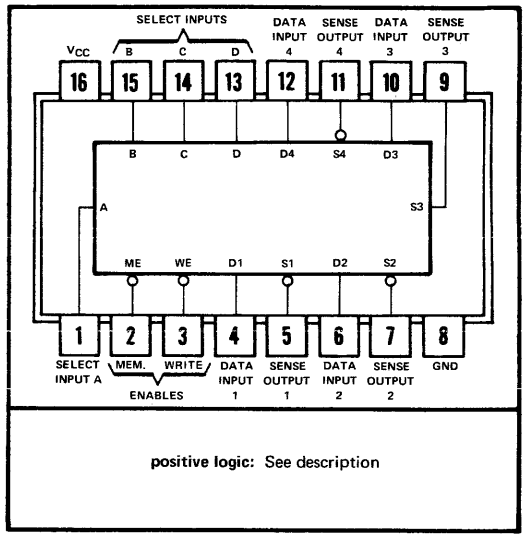
CIRCUIT TYPE SN7489
64-BIT READ/WRITE MEMORY

- For Application as a "Scratch Pad" Memory with Nondestructive Read-Out
- Fully Decoded Memory Organized as 16 Words of Four Bits Each
- Fast Access Time . . . 33 ns Typical
- Diode-Clamped, Buffered Inputs
- Open-Collector Outputs Provide Wire-AND Capability
- Typical Power Dissipation . . . 375 mW
- Compatible with Most TTL and DTL Circuits

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



positive logic: See description

†Pin assignments for these circuits are the same for all packages.

description

This 64-bit active-element memory is a monolithic, high-speed, transistor-transistor logic (TTL) array of 64 flip-flop memory cells organized in a matrix to provide 16 words of four bits each. Each of the 16 words is addressed in straight binary with full on-chip decoding.

The buffered memory inputs consist of four address lines, four data inputs, a write enable, and a memory enable for controlling the entry and access of data. The memory has open-collector outputs which may be wire-AND connected to permit expansion up to 4704 words of N-bit length without additional output buffering. The open-collector outputs may be utilized to drive external loads directly; however, dynamic reponse of an output can, in most cases, be improved by using an external pull-up resistor in conjunction with a partially loaded output. Access time is typically 33 nanoseconds; power dissipation is typically 375 milliwatts.

FUNCTION TABLE

ME	WE	OPERATION	CONDITION OF OUTPUTS
L	L	Write	Complement of Data Inputs
L	H	Read	Complement of Selected Word
H	L	Inhibit Storage	Complement of Data Inputs
H	H	Do Nothing	High

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write operation

Information present at the data inputs is written into the memory by addressing the desired word and holding both the memory enable and write enable low. Since the internal output of the data input gate is common to the input of the sense amplifier, the sense output will assume the opposite state of the information at the data inputs when the write enable is low.

read operation

The complement of the information which has been written into the memory is nondestructively read out at the four sense outputs. This is accomplished by holding the memory enable low, the write enable high, and selecting the desired address.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
High-level output voltage, V_{OH} (see Notes 1 and 2) . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the maximum voltage which should be applied to any output when it is in the off state.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Width of write-enable pulse, t_w	40			ns
Setup time, data input with respect to write enable, t_{setup} (see Figure 1)	40			ns
Hold time, data input with respect to write enable (see Figure 1)	5			ns
Select input setup time with respect to write enable, t_{setup}	0			ns
Select input hold time after writing, t_{hold} (see Figure 1)	5			ns
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,		I_I = −12 mA			−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IL} = 0.8 V,		V_{IH} = 2 V, V_{OH} = 5.5 V			20	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V,		I_{OL} = 12 mA			0.4	V
				I_{OL} = 16 mA			0.45	
I_I	Input current at maximum input voltage	V_{CC} = MAX,		V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,		V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,		V_I = 0.4 V			−1.6	mA
I_{CC}	Supply current	V_{CC} = MAX,		See Note 3		75	105	mA
C_o	Off-state output capacitance	V_{CC} = 5 V, f = 1 MHz		V_O = 2.4 V,		4		pF

NOTE 3: I_{CC} is measured with the memory enable grounded, all other inputs at 4.5 V, and all outputs open.

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from memory enable		C_L = 30 pF, R_{L1} = 300 Ω, R_{L2} = 600 Ω, See Figure 1		26	50	ns
t_{PHL}	Propagation delay time, high-to-low-level output from memory enable				33	50	
t_{PLH}	Propagation delay time, low-to-high-level output from select				30	60	ns
t_{PHL}	Propagation delay time, high-to-low-level output from select				35	60	
t_{SR}	Sense recovery time after writing	output initially high			39	70	ns
		output initially low			48	70	

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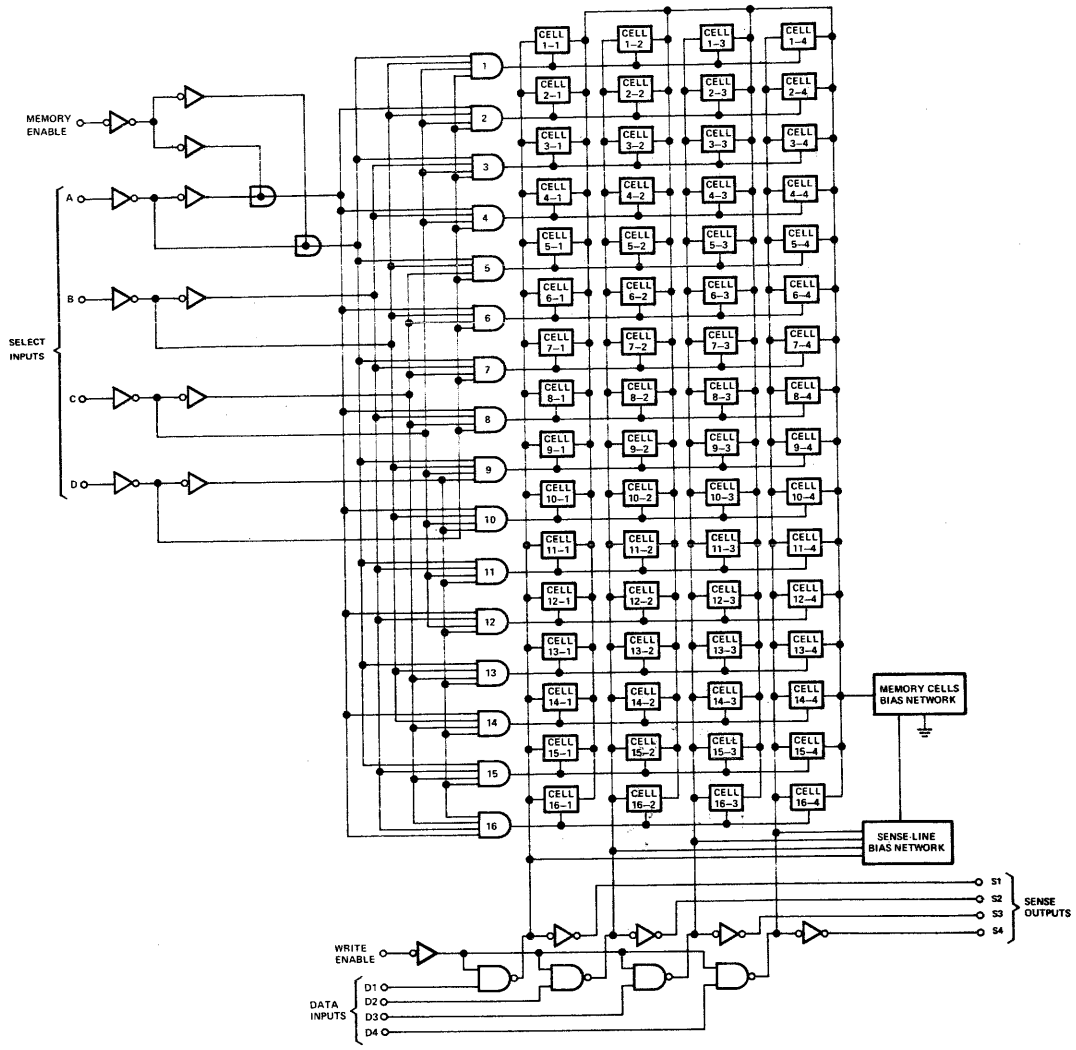
functional block diagram



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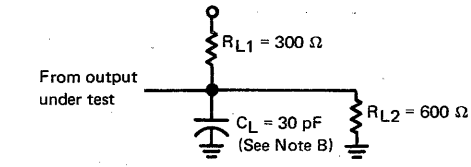
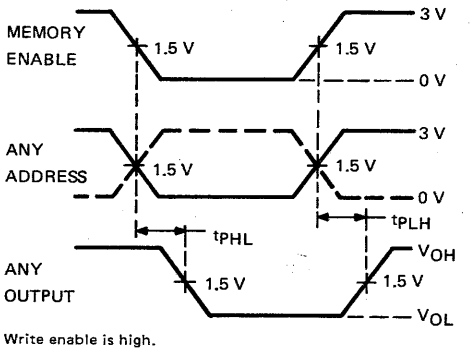
TYPICAL APPLICATION DATA

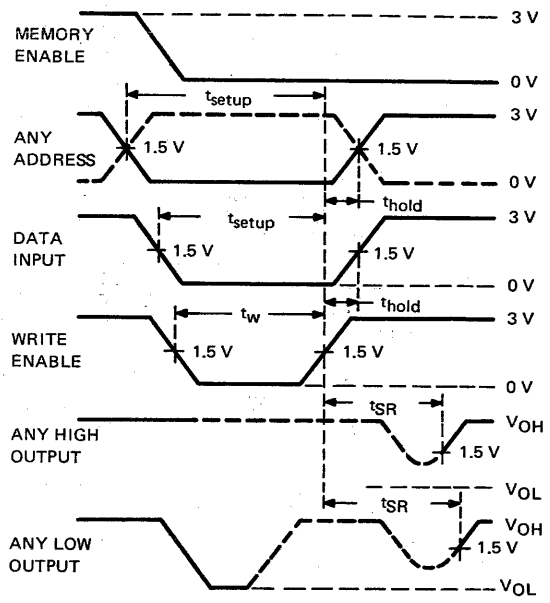


LOAD CIRCUIT



Write enable is high.

READ CYCLE



WRITE CYCLE FROM WRITE ENABLE

NOTES: A. The input pulse generators have the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 1–SWITCHING CHARACTERISTICS

TYPICAL CHARACTERISTICS

INPUT CURRENT vs INPUT VOLTAGE

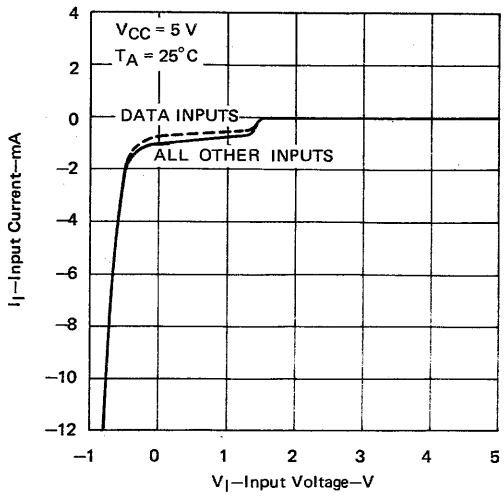


FIGURE 2

PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

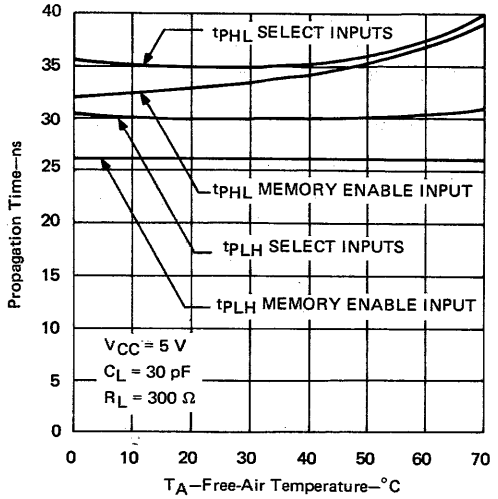
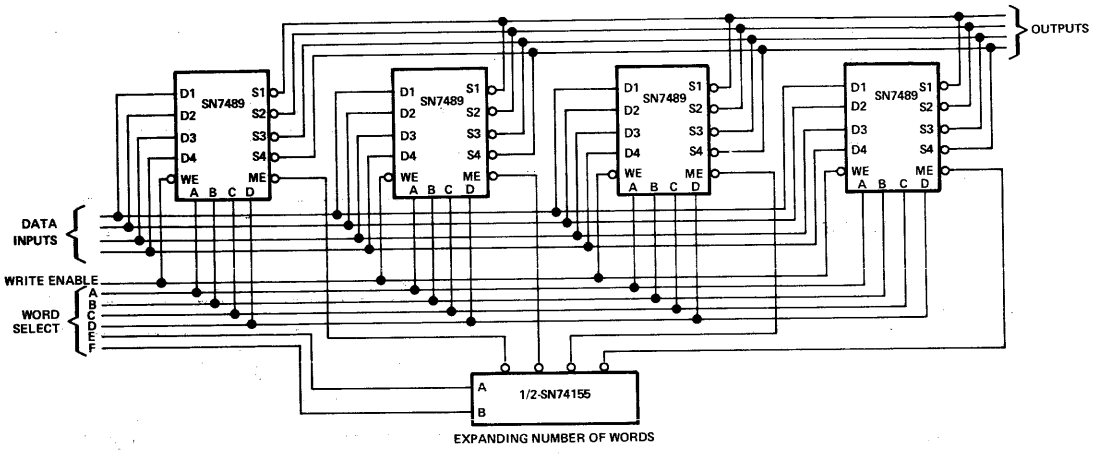


FIGURE 3

9

TYPICAL APPLICATION DATA



To increase word capacity, the outputs of a number of memories are wire-AND connected and each memory is enabled individually. The word capacity is limited only by the capability to wire-AND the outputs. In this case, the limiting parameter is the sink current capability of the memory, 12 milliamperes if the maximum low-level output voltage is limited to 0.4 V. Assuming that the output is driving only one Series 74 load (1.6 mA in the low state), the minimum value of the load resistor, R_L, will be 442 ohms.

$$R_L = \frac{V_{RL}}{I_{RL}} = \frac{V_{CC} - V_{OL}}{I_{sink} - I_{IL}(N_{TTL\ loads})} = \frac{5.0\ V - 0.4\ V}{0.012\ A - 0.0016\ A} = 442\ \Omega$$

In this case, the 442-ohm load resistor will supply sufficient high-level output current to wire-AND 292 outputs, providing a word capacity of 4672 words.

$$442 = \frac{V_{RL}}{I_{RL}} = \frac{V_{CC} - V_{OH}}{I_{OH}\,(N_{wire\text{-}ANDS}) + I_{IH}\,(N_{TTL\ loads})} = \frac{5.0\ V - 2.4\ V}{20\ \mu A\ (N_{wa}) + 40\ \mu A(1)}$$

therefore N_{wa} = 292 outputs

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When driving one or more standard TTL loads, the possibilities are shown below in increments of standard loads for both 12-mA and 16-mA sink current.

WORD CAPACITY vs TTL LOADS FOR V_{OL} = 0.4 V MAX

LOADS	R_L VALUE (OHMS)	MAX NO. OF WIRE-ANDS	MAX NO. OF WORDS
1	442	292	4672
2	522	245	3920
3	638	197	3152
4	821	150	2400
5	1150	103	1648
6	1916	55	880
7	5750	8	128

Where multiple SN7484 devices are used in a memory system, the memory enable input allows easy decoding of additional address bits.

WORD CAPACITY vs TTL LOADS FOR V_{OL} = 0.45 V MAX

LOADS	R_L VALUE (OHMS)	MAX NO. OF WIRE-ANDS	MAX NO. OF WORDS
1	316	409	6544
2	356	361	5776
3	406	314	5024
4	473	266	4256
5	569	218	3488
6	711	170	2720
7	948	123	1968
8	1422	75	1200
9	2844	27	432
10	4000	12	192

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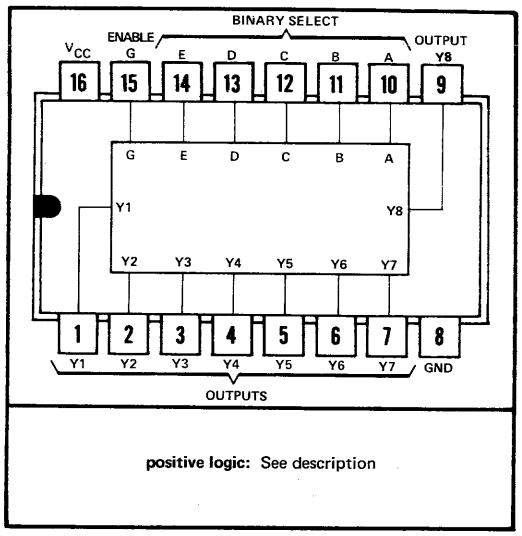
CIRCUIT TYPES SN5488A, SN7488A
256-BIT READ-ONLY MEMORIES

CIRCUIT TYPES SN5488A, SN7488A
BULLETIN NO. DL-S 7111445, JANUARY 1971
REPLACES BULLETIN NO. DL-S 7011299, FEBRUARY 1970

- Applications in Computer Subroutines
- Useful in Display Systems and Readouts
- Memory Organized as 32 Words of 8 Bits Each
- Input Clamping Diodes Simplify System Design
- Open-Collector Outputs Permit Wire-AND Capability
- Typical Access Time: 25 nanoseconds
- Typical Power Dissipation: 285 milliwatts
- Fully Compatible with Most TTL and DTL Circuits

N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: See description

description

These custom-programmed, 256-bit, read-only memories are organized as 32 words of eight bits each. Each monolithic, high-speed, transistor-transistor logic (TTL), 32-word memory array is addressed in straight 5-bit binary with full on-chip decoding. An overriding memory-enable input is provided which, when taken high, will inhibit the 32 address gates and cause all eight outputs to remain high. Data, as specified by the customer on the enclosed truth table/order blank, are permanently programmed into the monolithic structure for the 256 bit locations. This organization is expandable to n-words of N-bit length.

The address of an eight-bit word is accomplished through the buffered, binary select inputs which are decoded by the 32 five-input address gates. When the memory-enable input is high, all 32 gate outputs are low, turning off the eight output buffers.

Data are programmed into the memory at the emitters of 32 eight-emitter transistors. The programming process involves connecting or not connecting each of the 256 emitters. If an emitter is connected, a low-level voltage is read out of that bit location when its decoding gate is addressed. If the emitter is not connected, a high-level voltage is read when addressed. Those decoding-gate output emitters which are used are connected to their respective bit lines to drive the eight output buffers. Since only one decoding gate is addressed at a time, only one of the 32 transistors can supply current to the output buffers at a time.

This memory is fully compatible for use with most TTL or DTL circuits. Input clamping diodes are provided to minimize transmission-line effects and simplify system design. Input buffers lower the fan-in requirement to only one normalized Series 54/74 load for all inputs including enable (G). The open-collector outputs are capable of sinking 12 milliamperes of current and may be wire-AND connected to increase the number of words available. An external pull-up resistor from each output to the supply line (V_{CC}) is required to define the high-level output voltage. Where multiple SN7488 devices are used in a memory system, the enable input allows easy decoding of additional address bits. Access propagation delay time is typically 25 nanoseconds and power dissipation is typically 285 milliwatts.

The customer can specify the output level desired at each of the 256 bit locations by completing the enclosed truth table/order blank. Upon receipt of the order, Texas Instruments will assign a special device number to the device programmed according to the customer's order. The completed device will be marked with the TI special device number (not SN5488A or SN7448A). It is important that the customer specify not only the output levels desired at all 256-bit locations on the enclosed truth table/order blank, but also the other information requested.

Series 74 devices are characterized for operation from 0°C to 70°C.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: SN5488A Circuits . . . . . 55°C to 125°C
SN7488A Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN5488A			SN7488A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Operating free-air temperature range, T_A	−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage	1			2			V
V_{IL}	Low-level input voltage	1					0.8	V
V_I	Input clamp voltage	2	V_{CC} = MIN, I_I = −12 mA				−1.5	V
I_{OH}	High-level output current	1	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, V_{OH} = 5.5 V				40	μA
V_{OL}	Low-level output voltage	1	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V,	I_{OL} = 12 mA			0.4	V
I_{IH}	High-level input current (each input)	3	V_{CC} = MAX, V_I = 2.4 V				25	μA
			V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IL}	Low-level-input current (each input)	2	V_{CC} = MAX, V_I = 0.4 V				−1	mA
I_{CCH}	Supply current, all outputs high	4	V_{CC} = MAX			50		mA
I_{CCL}	Supply current, all outputs low (see Note 2)	5				64	80	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 2: All 32 words are addressed separately to ensure that the supply current does not exceed the stated maximum. The typical value shown is for the worst-case condition of all eight outputs driven low at one time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER§	FROM (INPUT)	TO (OUTPUT)	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Enable	Any	6	C_L = 15 pF, R_{L1} = 300 Ω, R_{L2} = 600 Ω		22	35	ns
t_{PHL}	Enable	Any				22	35	
t_{PLH}	Select	Any				29	45	
t_{PHL}	Select	Any				23	40	

§t_{PLH} = Propagation delay time, low-to-high level output.
t_{PHL} = Propagation delay time, high-to-low level output.

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TRUTH TABLE

The output levels are not shown on the truth table since the customer specifies the output condition he desires at each of the eight outputs for each of the 32 words (256 bits). The customer does this by filling out the TRUTH TABLE/ORDER BLANK at the back of this data sheet, and sending it in with his purchase order. The copy of the truth table on this page may be filled out and retained by the customer for his reference.

WORD	INPUTS						OUTPUTS							
	BINARY SELECT					ENABLE								
	E	D	C	B	A	G	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1
0	L	L	L	L	L	L								
1	L	L	L	L	H	L								
2	L	L	L	H	L	L								
3	L	L	L	H	H	L								
4	L	L	H	L	L	L								
5	L	L	H	L	H	L								
6	L	L	H	H	L	L								
7	L	L	H	H	H	L								
8	L	H	L	L	L	L								
9	L	H	L	L	H	L								
10	L	H	L	H	L	L								
11	L	H	L	H	H	L								
12	L	H	H	L	L	L								
13	L	H	H	L	H	L								
14	L	H	H	H	L	L								
15	L	H	H	H	H	L								
16	H	L	L	L	L	L								
17	H	L	L	L	H	L								
18	H	L	L	H	L	L								
19	H	L	L	H	H	L								
20	H	L	H	L	L	L								
21	H	L	H	L	H	L								
22	H	L	H	H	L	L								
23	H	L	H	H	H	L								
24	H	H	L	L	L	L								
25	H	H	L	L	H	L								
26	H	H	L	H	L	L								
27	H	H	L	H	H	L								
28	H	H	H	L	L	L								
29	H	H	H	L	H	L								
30	H	H	H	H	L	L								
31	H	H	H	H	H	L								
ALL	X	X	X	X	X	H	H	H	H	H	H	H	H	H

H = high level, L = low level, X = irrelevant

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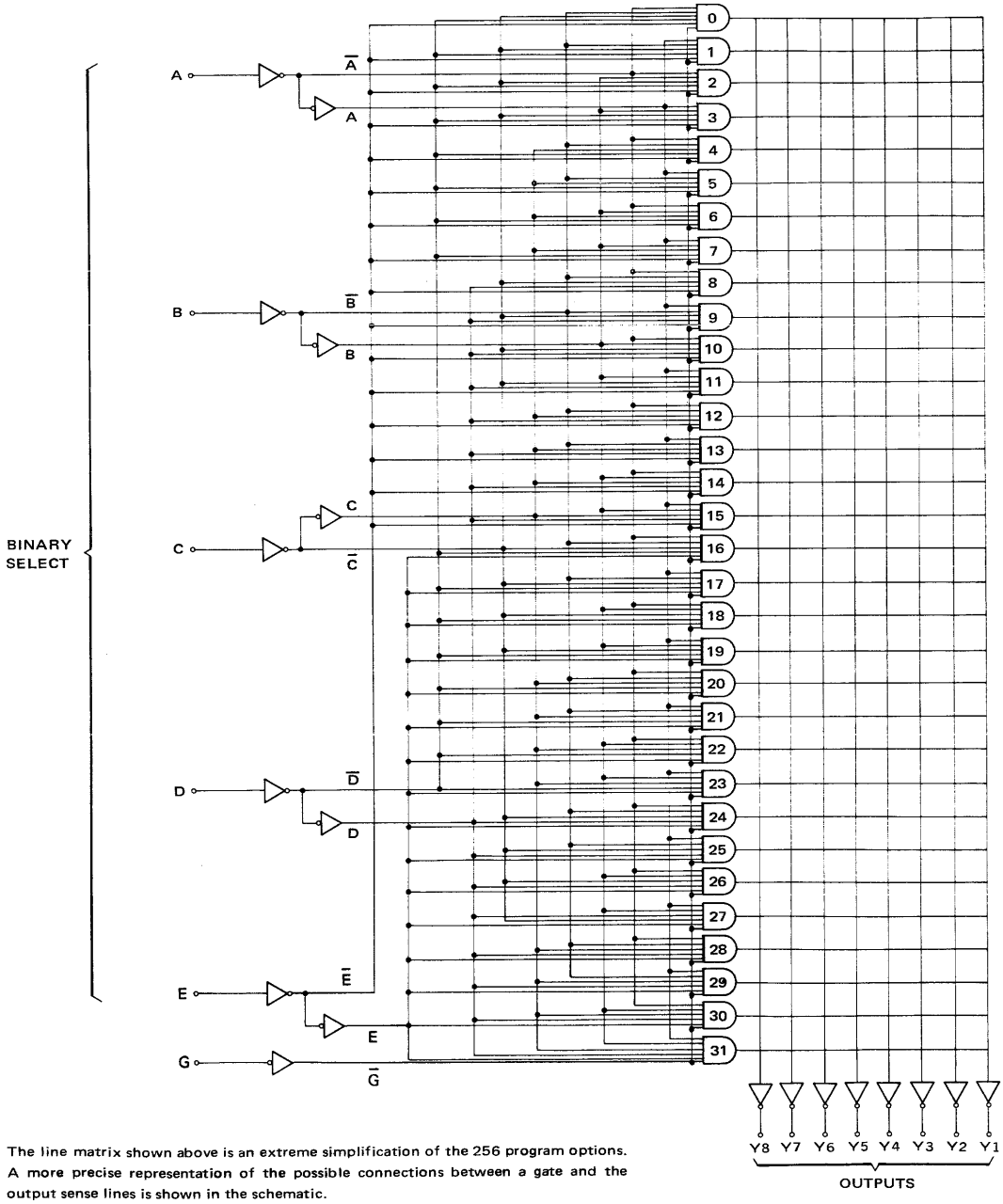
functional block diagram (programming not shown)



The line matrix shown above is an extreme simplification of the 256 program options. A more precise representation of the possible connections between a gate and the output sense lines is shown in the schematic.

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PARAMETER MEASUREMENT INFORMATION

d-c test circuits¶

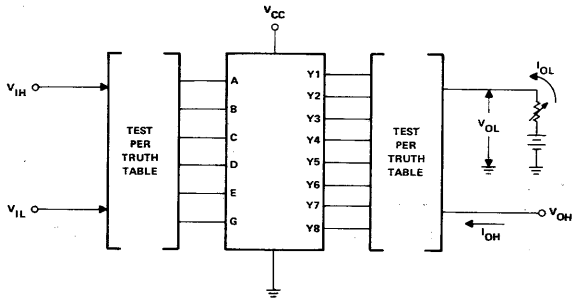
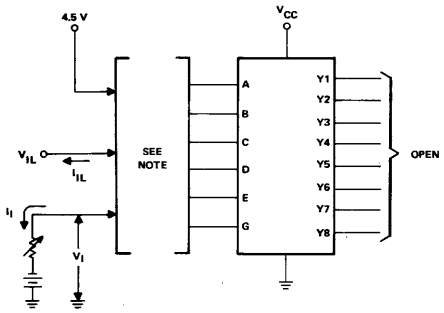
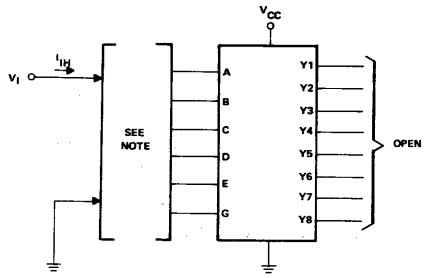


FIGURE 1–V_{IH}, V_{IL}, I_{OH}, V_{OL}



Each input is tested separately with all other inputs at 4.5 V.

FIGURE 2–V_I, I_{IL}



Each input is tested separately with all other inputs grounded.

FIGURE 3–I_{IH}

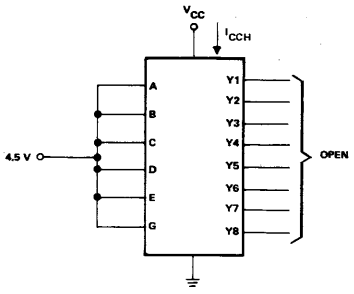
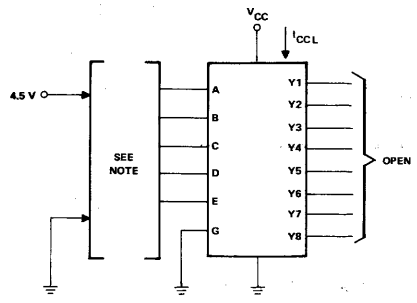


FIGURE 4–I_{CCH}



All 32 words are tested separately.

FIGURE 5–I_{CCL}

¶Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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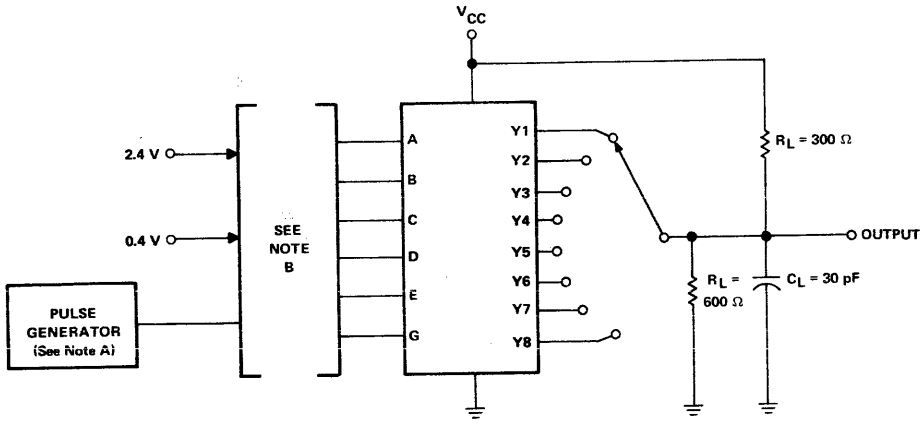
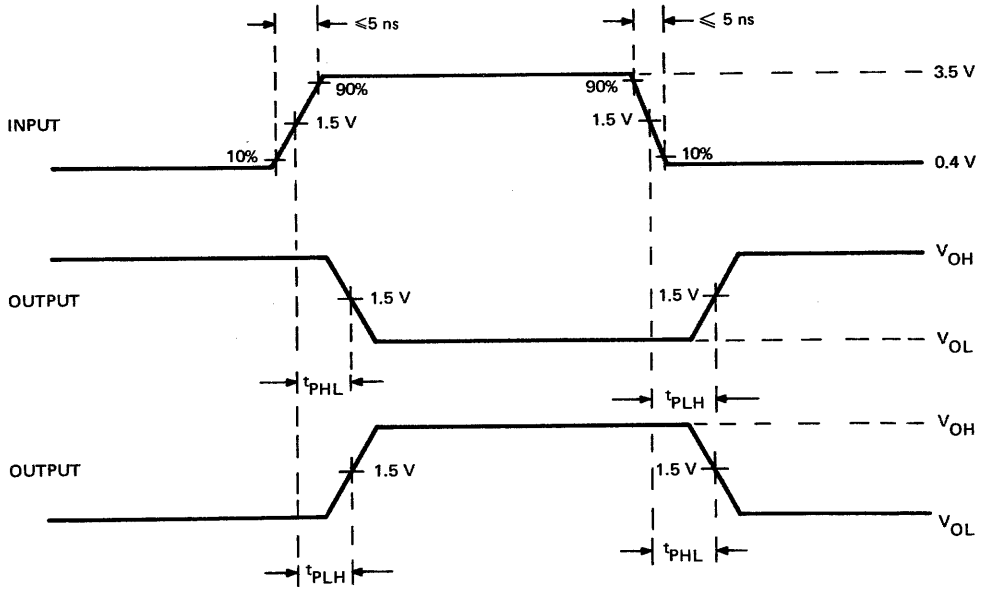
PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. The pulse generator is connected to the input under test. The other inputs, memory content permitting, are connected so that the input will switch the output under test.
C. C_L includes probe and jig capacitance.

FIGURE 6–PROPAGATION DELAY TIMES

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TYPICAL APPLICATION DATA

operation

Interconnection of the address buffers and decoding gates is already committed in the circuit design. Each decoding gate corresponds to one of the 32 eight-bit words which is programmed into the memory.

When a decoding gate is addressed, all its output emitters are high. All of the emitters connected to a particular output line form dot-OR connections with one another; that is, one high emitter is necessary and sufficient to carry the line high. This high is then inverted by an output buffer to produce a low-level output.

Assume that the gate shown in the schematic diagram is gate 31 and that word 31 is to be 10000001 using positive logic. This requires a high-level voltage at outputs 1 and 8. Therefore, emitters 1 and 8 of gate 31 would be left unconnected while the remaining emitters would be connected to their corresponding output lines.

expansion

Figure A illustrates how two memories may be connected to provide 32 words of 16 bits each. This scheme may be utilized to form words of N-bit length. Figure B shows how the enable input may be utilized to selectively activate the memory in applications requiring a larger number of words. Although 8-bit words are shown in Figure B, each word may be lengthened by the method illustrated in Figure A. One obvious limiting factor in this expansion scheme is the fan-out capability of the binary select register. The capability for further expansion above 512 words is available by utilizing a selective method for enabling the SN54154 or SN74154 four-line-to-16-line decoder. For smaller memory systems, the SN54154 or SN74154 may be replaced with SN5442 or SN7442 or standard TTL NAND gates.

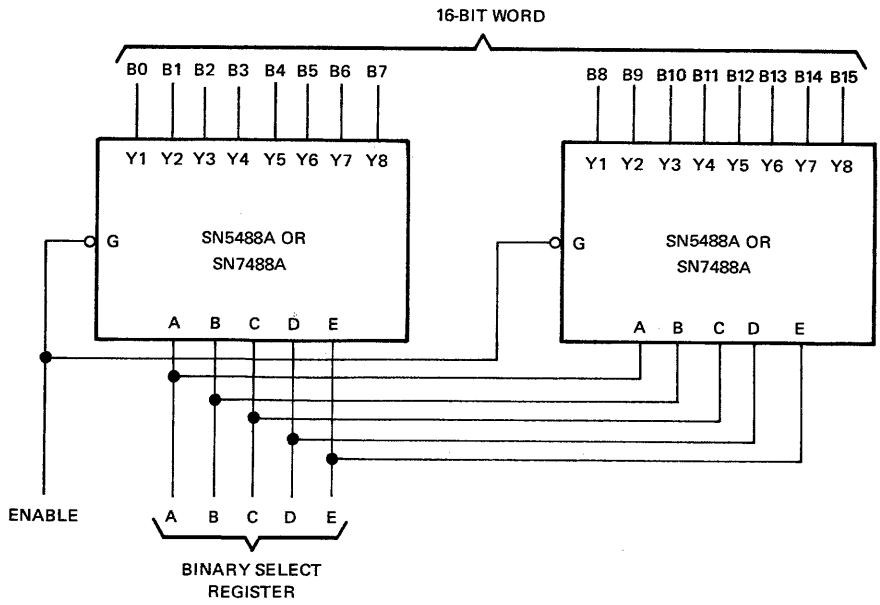

FIGURE A–INCREASING WORD LENGTH

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TYPICAL APPLICATION DATA

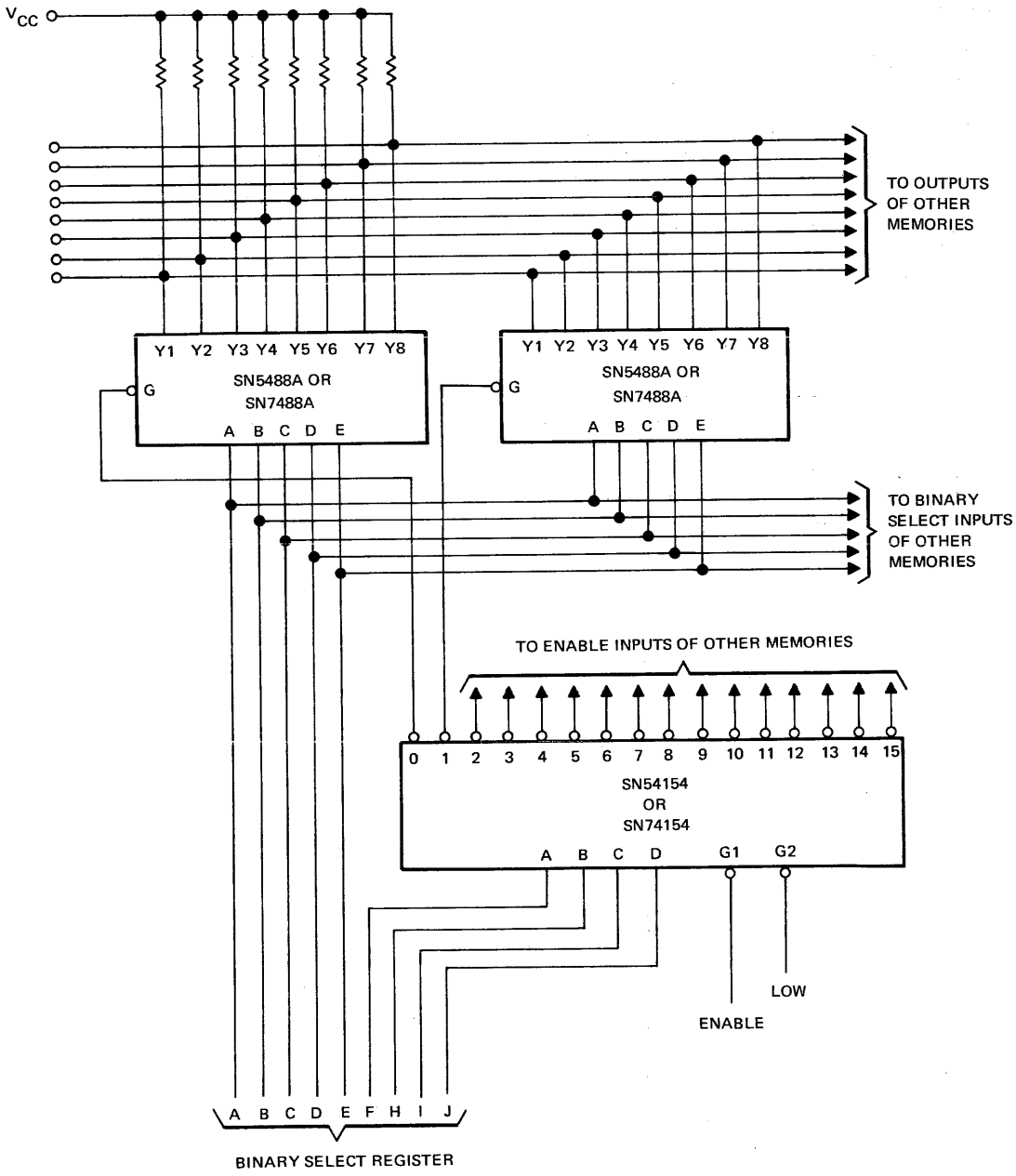

FIGURE B–INCREASING WORD CAPACITY

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TRUTH TABLE/ORDER BLANK

CUSTOMER _____

PURCHASE ORDER NO. _____

CUSTOMER PART NO. _____

THIS PORTION TO BE COMPLETED BY TI

TI PART NO.: _____

S.O. NO.: _____

DATE RECEIVED: _____

WORD	INPUTS						OUTPUTS							
	BINARY SELECT					ENABLE								
	E	D	C	B	A	G	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1
0	L	L	L	L	L	L								
1	L	L	L	L	H	L								
2	L	L	L	H	L	L								
3	L	L	L	H	H	L								
4	L	L	H	L	L	L								
5	L	L	H	L	H	L								
6	L	L	H	H	L	L								
7	L	L	H	H	H	L								
8	L	H	L	L	L	L								
9	L	H	L	L	H	L								
10	L	H	L	H	L	L								
11	L	H	L	H	H	L								
12	L	H	H	L	L	L								
13	L	H	H	L	H	L								
14	L	H	H	H	L	L								
15	L	H	H	H	H	L								
16	H	L	L	L	L	L								
17	H	L	L	L	H	L								
18	H	L	L	H	L	L								
19	H	L	L	H	H	L								
20	H	L	H	L	L	L								
21	H	L	H	L	H	L								
22	H	L	H	H	L	L								
23	H	L	H	H	H	L								
24	H	H	L	L	L	L								
25	H	H	L	L	H	L								
26	H	H	L	H	L	L								
27	H	H	L	H	H	L								
28	H	H	H	L	L	L								
29	H	H	H	L	H	L								
30	H	H	H	H	L	L								
31	H	H	H	H	H	L								
ALL	X	X	X	X	X	H	H	H	H	H	H	H	H	H

COMPLETE THE LOGIC DESIRED FOR 256 BITS.
INDICATE H FOR HIGH LEVEL OR L FOR LOW LEVEL.

H = high level, L = low level, X = irrelevant

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TEXAS INSTRUMENTS
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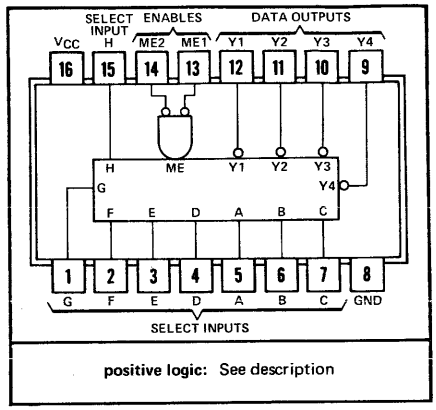
CIRCUIT TYPES SN54187, SN74187
1024-BIT READ-ONLY MEMORIES

- Typical Access Time . . . 40 ns
- Typical Power Dissipation . . . 0.46 mW/Bit
- Organized as 256 Words by 4 Bits
- Ideal for Microprogramming, Reference Tables, and Code Converters
- Easily Expandable
- Fully Decoded, Buffered Inputs
- Diode-Clamped Inputs
- Full Fan-Out, Open-Collector Outputs
- Fully Compatible with Most TTL and DTL Circuits

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)†



†Pin assignments for these circuits are the same for all packages.

description

The SN54187 and SN74187 circuits are custom-programmed, 1024-bit, read-only memories organized as 256 words of four bits each. These monolithic, high-speed transistor-transistor logic (TTL) memory arrays are addressed in straight eight-bit binary with full on-chip decoding. Two overriding memory-enable inputs are provided which, when either one or both are taken high, will inhibit the function causing all four outputs to remain high. Data, as specified by the customer, are permanently programmed into the monolithic structure for the 1024 bit locations. This organization is expandable to 41,472 words of n-bits with no additional output buffering.

The address of a four-bit word is accomplished through the buffered binary select inputs in coincidence with low-level voltages at both enable inputs. The most significant binary select inputs, D through H, are decoded internally in the X plane to select one-of-32 lines, and the least significant bits, A, B, and C, are internally decoded in the Y plane to accomplish one-of-eight decoding to drive the four output buffers. Where multiple SN54187 or SN74187 devices are used in a memory system, the enable input allows easy decoding of additional address bits.

Data are programmed into the memory cell at the emitters of 1024 transistors. The memory cell consists of a 32-by-32 matrix of transistors. In the X plane each of the 32 address decoding gate outputs supply common base drive to 32 transistors. In the Y plane the 32 transistors are arranged into four groups of eight. This permits each of the bit lines to be terminated in four one-of-eight decoders which achieves the four-bit word length.

The open-collector outputs are capable of sinking 16 milliamperes of current and may be wire-AND connected to increase the number of words available. The open-collector outputs may be utilized to drive external loads directly; however, dynamic response of the outputs can, in some cases, be improved by using an external pull-up resistor in conjunction with a partially loaded output.

The customer can specify the output logic level desired at each of the 1024 bit locations by completing the supplementary ordering data and a set of data cards punched in accordance with the data format shown under ordering instructions. Upon receipt of the order, Texas Instruments will assign a special device number to the device programmed according to the customer's order. The completed device will be marked with the TI special device number (not SN54187 or SN74187). It is important that the customer specify not only the output levels desired at all 1024 bit locations, but also the other information requested.

Access propagation delay time is typically 40 nanoseconds and power dissipation is typically 0.46 milliwatt per bit. The SN54187 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74187 is characterized for operation from 0°C to 70°C.

PRELIMINARY DATA SHEET:
Supplementary data will be published at a later date.

TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) 7V
Input voltage (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: SN54187 Circuits . . . . . −55°C to 125°C
SN74187 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54187			SN74187			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA			−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, V_{OH} = 5.5 V			40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	I_{OL} = 12 mA			0.4	V
			I_{OL} = 16 mA			0.45	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−1	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 2		92	130	mA
C_o	Off-state output capacitance	V_{CC} = 5 V, f = 1 MHz	V_O = 5 V,		6.5		pF

NOTE 2: With outputs open and both ME inputs grounded, I_{CC} is measured first by selecting a word which contains the maximum number of programmed high-level outputs, then by selecting a word which contains the maximum number of programmed low-level outputs.

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

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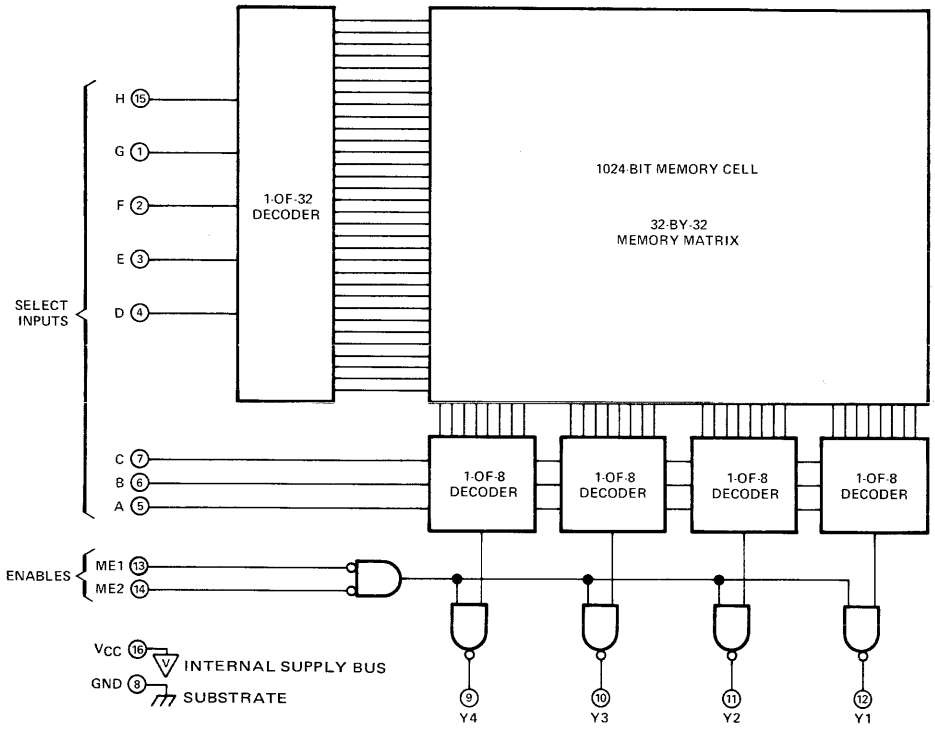
switching characteristics, V_{CC} = 5 V, T_A = 25°C

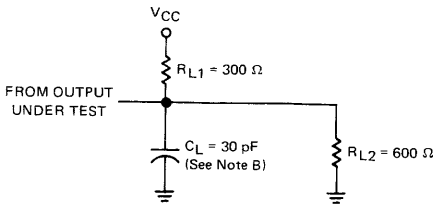
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from enable	C_L = 30 pF, R_{L1} = 300 Ω, R_{L2} = 600 Ω, See Figure 1		20	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output from enable			20	30	
t_{PLH}	Propagation delay time, low-to-high-level output from select			40	60	ns
t_{PHL}	Propagation delay time, high-to-low-level output from select			40	60	

functional block diagram

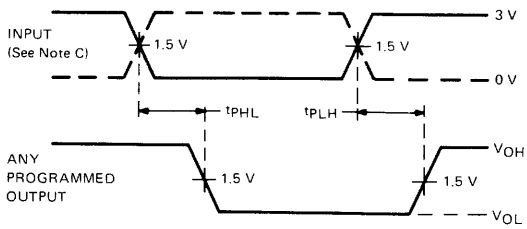


PARAMETER MEASUREMENT INFORMATION

9



LOAD CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The input pulse generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, PRR ≤ 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. The pulse generator is connected to the input under test. The other inputs, memory content permitting, are connected so that the input will switch the output under test.

FIGURE 1—PROPAGATION DELAY TIMES

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ORDERING INSTRUCTIONS

Programming instructions for the SN54187 or SN74187 are solicited in the form of a sequenced deck of 32 standard 80-column data cards providing the information requested under data card format, accompanied by a properly sequenced listing of these cards, and the supplementary ordering data. Upon receipt of these items, a computer run will be made from the deck of cards which will produce a complete truth table of the requested part. This truth table, showing output conditions for each of the 256 words, will be forwarded to the purchaser as verification of the input data as interpreted by the computer-automated design (CAD) program. This single run also generates mask and test program data; therefore, verification of the truth table should be completed promptly.

Each card in the data deck prepared by the purchaser identifies the eight words specified and describes the conditions at the four outputs for each of the eight words. All addresses must have all outputs defined and columns designated as "blank" must not be punched. Cards should be punched according to the data card format shown.

SUPPLEMENTARY ORDERING DATA

Submit the following information with the data cards:

a) Customer's name and address
b) Customer's purchase order number
c) Customer's drawing number.

The following information will be furnished to the customer by Texas Instruments:

a) TI part number
b) TI sales order number
c) Date received.

DATA CARD FORMAT

Column	
1- 3	Punch a right-justified integer representing the binary input address (000-248) for the first set of outputs described on the card.
4	Punch a "–" (Minus sign)
5- 7	Punch a right-justified integer representing the binary input address (0007-255) for the last set of outputs described on the card.
8- 9	Blank
10-13	Punch "H", "L", or "X" for bits four, three, two, and one (outputs Y4, Y3, Y2, and Y1 in that order) for the first set of outputs specified on the card. H = high-level output, L = low-level output, X = output level irrelevant.
14	Blank
15-18	Punch "H", "L", or "X" for the second set of outputs.
19	Blank
20-23	Punch "H", "L", or "X" for the third set of outputs.
24	Blank
25-28	Punch "H" "L", or "X" for the fourth set of outputs.
29	Blank
30-33	Punch "H", "L", or "X" for the fifth set of outputs.
34	Blank
35-38	Punch "H", "L", or "X" for the sixth set of outputs.
39	Blank
40-43	Punch "H", "L", or "X" for the seventh set of outputs.
44	Blank
45-48	Punch "H", "L", or "X" for the eighth set of outputs.
49	Blank
50-51	Punch a right-justified integer representing the current calendar day of the month.
52	Blank
53-55	Punch an alphabetic abbreviation representing the current month.
56	Blank
57-58	Punch the last two digits of the current year.
59	Blank
60-61	Punch "SN"
62-66	Punch a left-justified integer representing the Texas Instruments part number. This is supplied by the factory through a TI sales representative.
67-68	Blank
69-80	Preferably these columns should be punched to reflect the customer's part or specification-control number. This information is not essential.

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CIRCUIT TYPES SN54170, SN74170
4-BY-4 REGISTER FILES

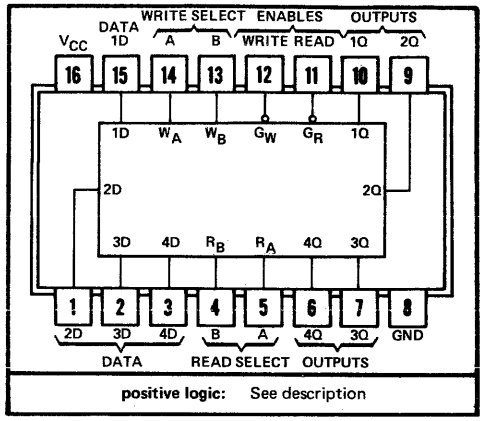
- Separate Read/Write Addressing Permits Simultaneous Reading and Writing
- Fast Access Times . . . Typically 20 ns
- Open-Collector Outputs with 30-μA Maximum Off-State Current
- Organized as 4 Words of 4 Bits
- Expandable to 1024 Words of n-Bits
- For Use as:

  Scratch-Pad Memory

  Buffer Storage between Processors

  Fast Multiplication Schemes

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



†Pin assigments for these circuits are the same for all packages.

description

The SN54170 and SN74170 MSI 16-bit TTL register files incorporate the equivalent of 98 gates on a monolithic chip measuring only 90 by 110 mils. The register file is organized as 4 words of 4 bits each and separate on-chip decoding is provided for addressing the four word locations to either write-in or retrieve data. This permits simultaneous writing into one location and reading from another word location.

Four data inputs are available which are used to supply the 4-bit word to be stored. Location of the word is determined by the write address inputs A and B in conjunction with a write-enable signal. Data applied at the inputs should be in its true form. That is, if a high-level signal is desired from the output, a high-level is applied at the data input for that particular bit location. The latch inputs are arranged so that new data will be accepted only if both internal address gate inputs are high. When this condition exists, data at the D input is transferred to the latch output. When the write enable input, G_W is high, the data inputs are inhibited and their states can cause no change in the information stored in the internal latches. When the read enable input, G_R, is high, the data outputs are inhibited and remain high.

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The individual address lines permit direct acquisition of data stored in any four of the latches. Four individual decoding gates are used to complete the address for reading a word. When the read address is made in conjunction with the read-enable signal, the word appears at the four outputs.

This arrangement—data-entry addressing separate from data-read addressing and individual sense line—eliminates recovery times, permits simultaneous reading and writing, and is limited in speed only by the write time (45 nanoseconds maximum) and the read time (35 nanoseconds maximum). The register file has a non-destructive readout in that data is not lost when addressed.

All inputs are buffered to lower the drive requirements to one normalized Series 54/74 load, and input-clamping diodes minimize switching transients to simplify system design. High-speed, double-ended AND-OR-INVERT gates are employed for the read-address function and drive high-sink-current, open-collector outputs. Up to 256 of these outputs may be wire-AND connected for increasing the capacity up to 1024 words. Any number of these registers may be paralleled to provide n-bit word length.

Power dissipation is typically 500 mW total or 5 mW per gate. The SN54170 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74170 is characterized for operation from 0°C to 70°C.

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logic

WRITE FUNCTION TABLE (SEE NOTES A, B, AND C)

WRITE INPUTS			WORD			
W_B	W_A	G_W	0	1	2	3
L	L	L	Q = D	Q_n	Q_n	Q_n
L	H	L	Q_n	Q = D	Q_n	Q_n
H	L	L	Q_n	Q_n	Q = D	Q_n
H	H	L	Q_n	Q_n	Q_n	Q = D
X	X	H	Q_n	Q_n	Q_n	Q_n

READ FUNCTION TABLE (SEE NOTES A AND D)

READ INPUTS			OUTPUTS			
R_B	R_A	G_R	1Q	2Q	3Q	4Q
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	H	H	H	H

NOTES: A. H = high level, L = low level, X = irrelevant
B. (Q = D) = The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.
C. Q_n = No change.
D. W0B1 = The first bit of word 0, etc.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Output voltage (see Notes 1 and 2) . . . . . 5.5 V
Operating free-air temperature range: SN54170J Circuits . . . . . −55°C to 125°C
SN74170J, N Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the maximum voltage which should be applied to any output when it is in the off state.

recommended operating conditions

		SN54170			SN74170			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Low-level output current, I_{OL}				16			16	mA
Width of write-enable or read-enable pulse, t_w		25			25			ns
Setup times, high- or low-level data (see Note 3 and Figure 1)	data input with respect to write enable, $t_{setup(D)}$	10			10			ns
	write select with respect to write enable, $t_{setup(W)}$	15			15			ns
	read select with respect to read enable, $t_{setup(R)}$	5			5			ns
Hold times, high- or low-level data (see Note 4 and Figure 1)	data input with respect to write enable, $t_{hold(D)}$	0			0			ns
	write select with respect to write enable, $t_{hold(W)}$	5			5			ns
	read select with respect to read enable, $t_{hold(R)}$	5			5			ns
Latch time for new data, t_{latch} (see Note 5)		25			25			ns
Operating free-air temperature range, T_A		−55	25	125	0	25	70	°C

NOTES: 3. Setup time is the interval immediately preceding the negative-going edge of the enable pulse during which interval the data or address to be recognized must be maintained at the input to ensure its recognition.
4. Hold time is the interval immediately following the positive-going edge of the enable pulse during which interval the data or address to be recognized must be maintained at the input to ensure its continued recognition.
5. Latch time is the time required for the internal output of the latch to assume the state of new data. See Figure 1. This is important only when attempting to read from a location immediately after that location has received new data.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA			−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN,	V_O = 5.5 V			30	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 16 mA	V_{IL} = 0.8 V,			0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−1.6	mA
I_{CC}	Supply current	V_{CC} = MAX, see Note 6	SN54170		127‡	140	mA
			SN74170		127‡	150	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡Typical power dissipation shown is an average for 50% duty cycle at V_{CC} = 5 V, T_A = 25°C.

NOTE 6: Maximum I_{CC} is guaranteed for the following worst-case conditions: 4.5 V is applied to all data inputs and both enable inputs, all address inputs are grounded, and all outputs are open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output, from read enable to any Q	C_L = 15 pF,	R_L = 400 Ω		10	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from read enable to any Q	C_L = 15 pF,	R_L = 400 Ω		20	30	ns

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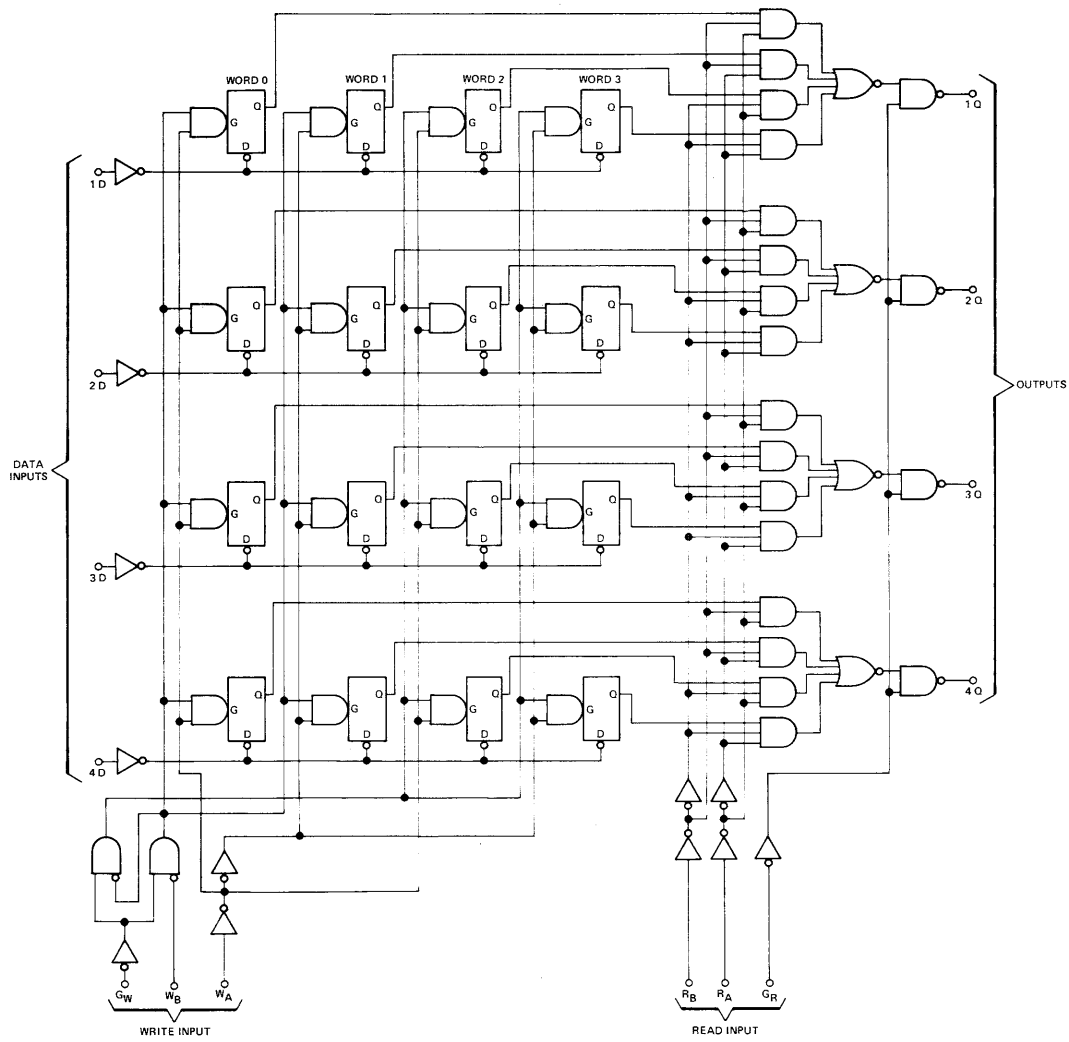
functional block diagram



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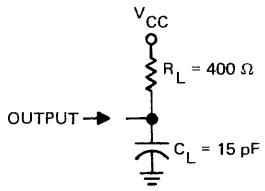
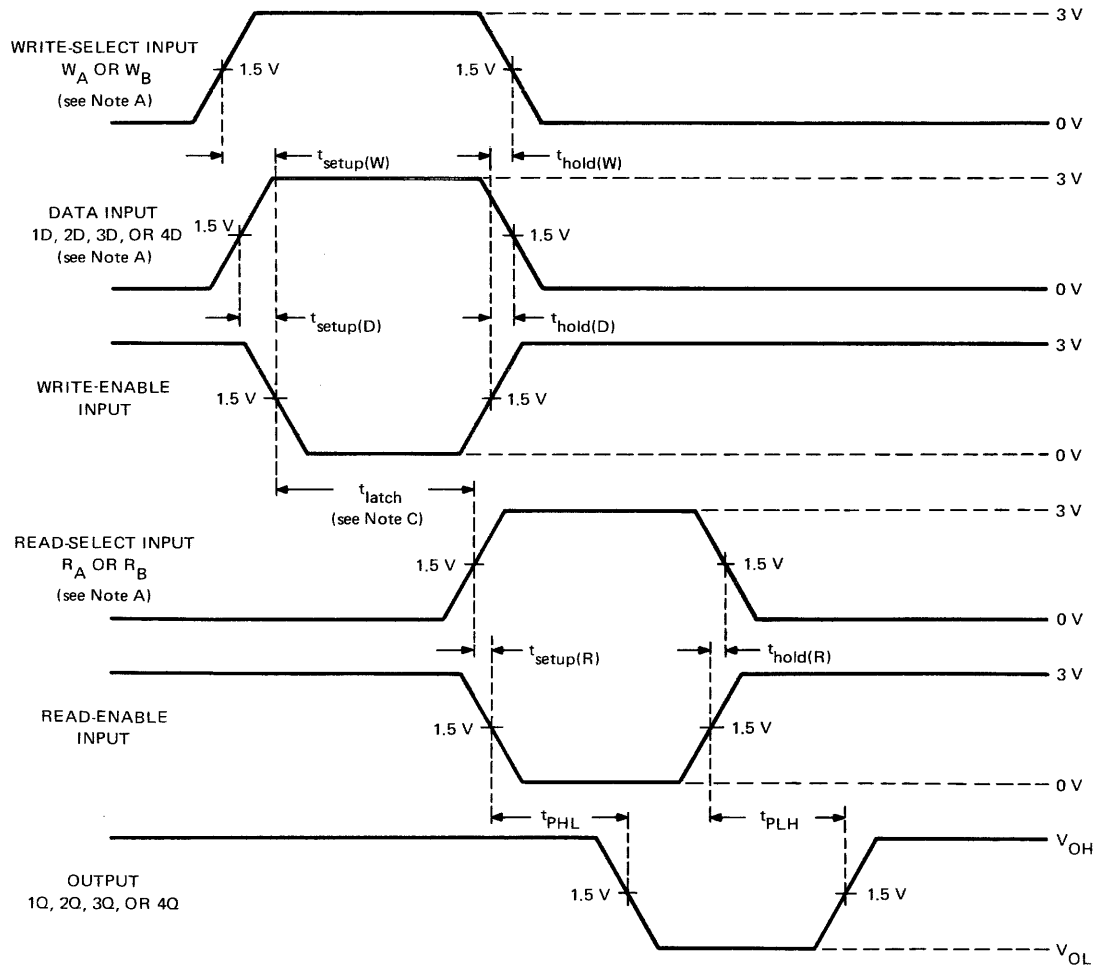
PARAMETER MEASUREMENT INFORMATION

switching characteristics



NOTE: C_L includes probe and jig capacitance.

LOAD FOR OUTPUT UNDER TEST



VOLTAGE WAVEFORMS

NOTES: A. High-level inputs are illustrated; however, low-level setup and hold times are the same.
B. Waveforms are supplied by generators with the following characteristics: PRR ≤ 1 MHz, $Z_{out} \approx 50\ \Omega$, duty cycle ≤ 50%, $t_r \leq 10$ ns, $t_f = 10$ ns.
C. This applies only when reading from a location immediately after that location has received new data.

FIGURE 1–SWITCHING TIMES

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TYPICAL APPLICATION DATA

general

These register files may be cascaded to form n-bit registers with capacities of 1024 words. Word capacity is increased by wire-AND connecting the four outputs of a number of register files (up to 256). One write-select and one read-select register is required for all the paralleled files.

For increased word length (number of bits), a number of files may be selected and enabled simultaneously to provide the desired word length. This scheme is compatible for using parallel files to provide more words also. All inputs and outputs, except the write-enable and read-enable lines, are paralleled to add word capacity. The enable lines are separate for each word.

These register files can be used with improved efficiency in most applications that require a scratch-pad-type memory. Because recovery times are eliminated, the cycle time is a function of the longer of the write or read time. In the case of the SN54170/SN74170, this is the write time which is 45 nanoseconds maximum. The separate write and read address inputs permit efficient usage in applications where new data is entered throughout the memory during each cycle. A familiar example of this is a display in which the information moves across a panel of lights. The first display data is stored in the file, and as it is being read and displayed, the next display data is being written into the memory. More realistically, the SN54170/SN74170 is capable of operating at speeds that permit its use as a high-speed buffer memory between main memories or peripheral stations. In addition, the register file could be used to acquire tabular data, as a complete table or on a partial basis, recycling to present the entire bank of data.

high-speed buffer memory

These register files may also be organized differently on the read inputs than on the write outputs. As shown in Figure A, for example, the SN54170/SN74170 is utilized to acquire 256-bit words from the main memory and make 32-bit words available to the central processor unit (CPU). The 256-bit word is transferred in parallel to the buffer memory. A typical access time to the main memory is in the order of one microsecond. The buffer memory is organized so that the 256 bits of data are made available to the CPU in 32-bit words. Access time to data stored in the buffer register is 35 nanoseconds. In terms of frequency, data may be transferred from core memory to buffer memory at typically one megahertz; however, the transfer rate from buffer register to CPU is typically 20 megahertz when data setup time at the CPU is considered (30 nanoseconds propagation delay time through the SN54170/SN74170 and 10 to 20 nanoseconds data setup time in the CPU).

This buffer memory provides the following advantages:

- ability to simultaneously read and write means that the CPU is not interrupted as the buffer memory is being re-programmed
- the flexibility of organizing the write inputs and read outputs differently gives an effective main-memory access time of 125 nanoseconds:

$$\left(\frac{32\text{ bits}}{256\text{ bits}} \times 1\ \mu s\right) \text{ for one CPU word (32 bits).}$$

The concept of this organization is illustrated in Figure B which shows a 16-bit word being made available in 4-bit words. The 16-bit word is written simultaneously into word locations A, B, C, and D by a common write signal. Any 4-bit word may then be selected from these word locations by separate read-enable strobes.

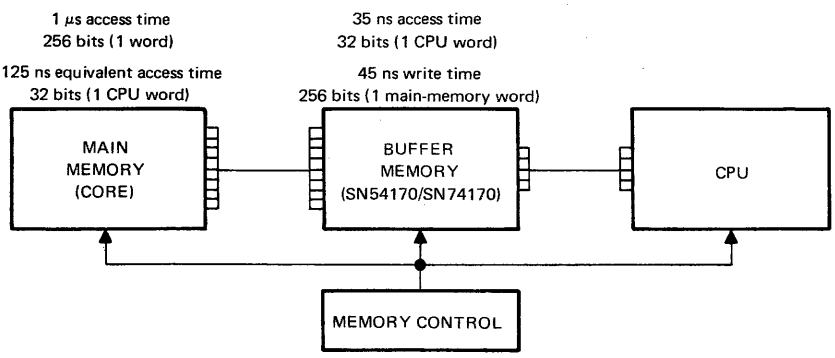

FIGURE A–HIGH-SPEED BUFFER MEMORY

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TYPICAL APPLICATION DATA

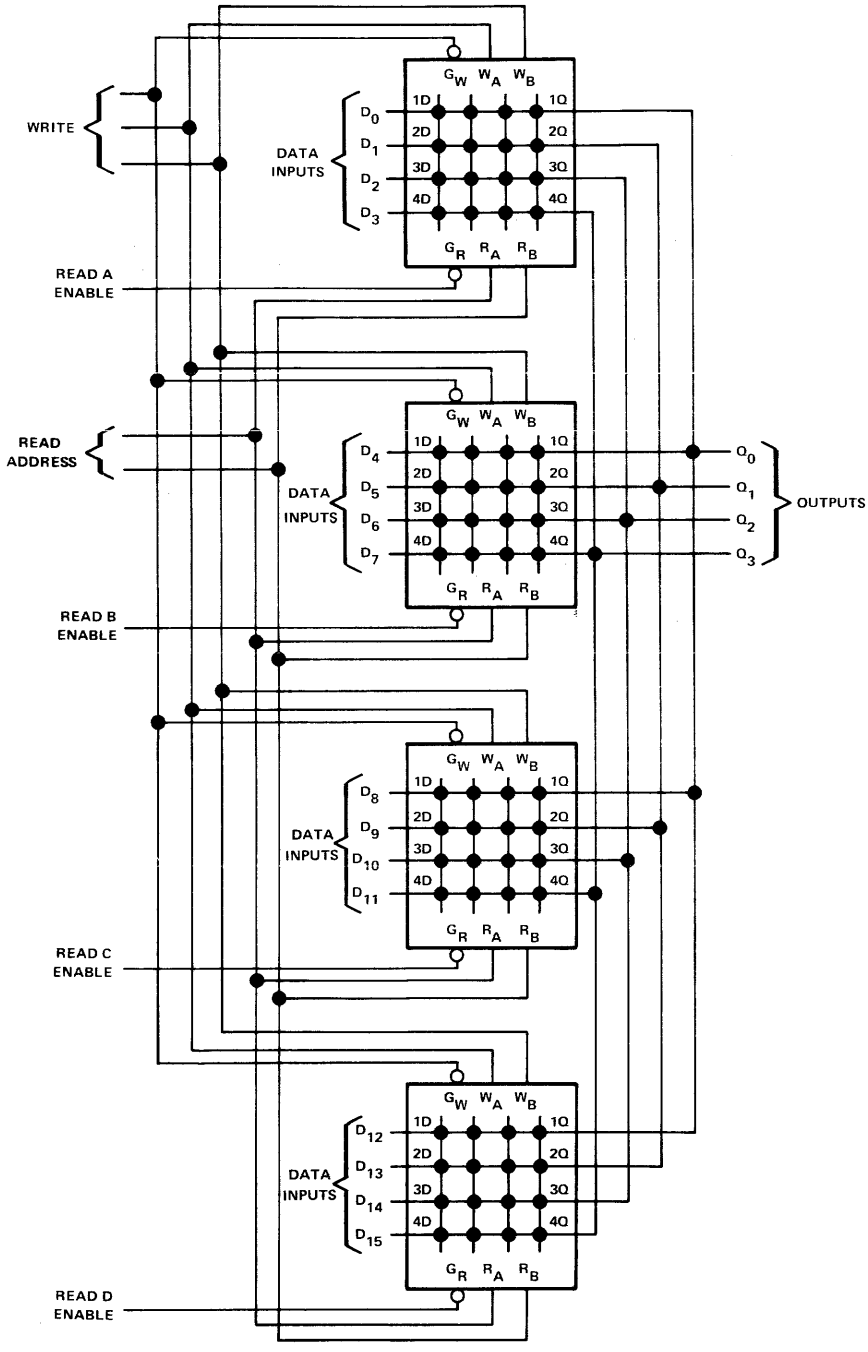

FIGURE 8—TYPICAL 16-BIT-WORD-TO-4-BIT-WORD BUFFER MEMORY

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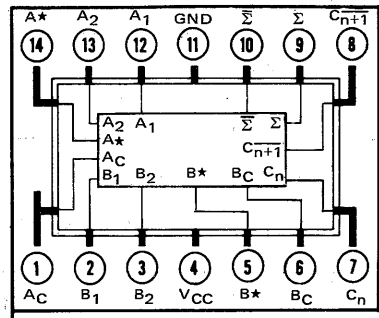
CIRCUIT TYPES SN5480, SN7480
GATED FULL ADDERS

logic

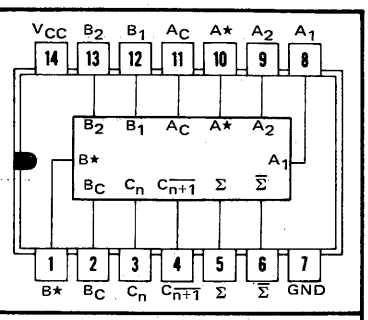
TRUTH TABLE
(See Notes 1, 2, and 3)

C_n	B	A	$\overline{C_{n+1}}$	$\overline{\Sigma}$	Σ
0	0	0	1	1	0
0	0	1	1	0	1
0	1	0	1	0	1
0	1	1	0	1	0
1	0	0	1	0	1
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	0	0	1

W
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: See truth table

NOTES: 1. $A = \overline{A★ \cdot A_C}$, $B = \overline{B★ \cdot B_C}$ where $A★ = \overline{A_1 \cdot A_2}$, $B★ = \overline{B_1 \cdot B_2}$
2. When A★ or B★ are used as inputs, A_1 and A_2 or B_1 and B_2 respectively must be connected to GND.
3. When A_1 and A_2 or B_1 and B_2 are used as inputs, A★or B★ respectively must be open or used to perform Dot-OR logic.

description

This single-bit, high-speed, binary full adder with gated complementary inputs, complementary sum (Σ and $\overline{\Sigma}$) outputs and inverted carry output is designed for medium- and high-speed, multiple-bit, parallel-add/serial-carry applications. The circuit (see schematic diagram) utilizes diode-transistor logic (DTL) for the gated inputs, and high-speed, high-fan-out transistor-transistor logic (TTL) for the sum and carry outputs. The circuit is entirely compatible with both DTL and TTL logic families. The implementation of a single-inversion, high-speed, Darlington-connected serial-carry circuit minimizes the necessity for extensive "look-ahead" and carry-cascading circuits.

absolute maximum ratings over operating temperature range (unless otherwise noted)

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Supply Voltage V_{CC} (See Note 4) . . . . . 7 V
Input Voltage, V_{in} (See Notes 4 and 5) . . . . . 5.5 V
Operating Free-Air Temperature Range: SN5480 Circuits . . . . . −55°C to 125°C
SN7480 Circuits . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN5480 Circuits	4.5	5	5.5	V
SN7480 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Outputs:				
$\overline{C_{n+1}}$, N			5	
Σ or $\overline{\Sigma}$, N			10	
A★ or B★, N			3	

NOTES: 4. The voltages are with respect to ground terminal.
5. Input signals must be zero or positive with respect to network ground terminal.

electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage	1 and 2			2			V
$V_{in(0)}$	Logical 0 input voltage	1 and 2					0.8	V
$V_{out(1)}$	Logical 1 output voltage	2			2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	1				0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current at A_1, A_2, B_1, B_2, A_c or B_c	3	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(0)}$	Logical 0 level input current at A* or B*	4	V_{CC} = MAX, V_{in} = 0.4 V				−2.6	mA
$I_{in(0)}$	Logical 0 level input current at C_n	4	V_{CC} = MAX, V_{in} = 0.4 V				−8	mA
$I_{in(1)}$	Logical 1 level input current at A_1, A_2, B_1, B_2, A_c or B_c	5	V_{CC} = MAX, V_{in} = 2.4 V				15	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at C_n	6	V_{CC} = MAX, V_{in} = 2.4 V				200	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current at Σ or $\overline{\Sigma}$§	7	V_{CC} = MAX	SN5480	−20		−57	mA
				SN7480	−18		−57	mA
I_{OS}	Short-circuit output current at $\overline{C_{n+1}}$§	7	V_{CC} = MAX	SN5480	−20		−70	mA
				SN7480	−18		−70	mA
I_{CC}	Supply current	8	V_{CC} = MAX	SN5480		21	31	mA
				SN7480		21	35	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

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switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM INPUT	TO OUTPUT	FIGURE 9 TEST NO.	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd1}	C_n	$\overline{C_{n+1}}$	1	C_L = 15 pF, R_L = 780 Ω		13	17	ns
t_{pd0}			2	C_L = 15 pF, R_L = 780 Ω		8	12	ns
t_{pd1}	B_C	$\overline{C_{n+1}}$	3	C_L = 15 pF, R_L = 780 Ω		18	25	ns
t_{pd0}			4	C_L = 15 pF, R_L = 780 Ω		38	55	ns
t_{pd1}	A_C	Σ	5	C_L = 15 pF, R_L = 400 Ω		52	70	ns
t_{pd0}			6	C_L = 15 pF, R_L = 400 Ω		62	80	ns
t_{pd1}	B_C	$\overline{\Sigma}$	7	C_L = 15 pF, R_L = 400 Ω		38	55	ns
t_{pd0}			8	C_L = 15 pF, R_L = 400 Ω		56	75	ns
t_{pd1}	A_1	A*	9	C_L = 15 pF		48	65	ns
t_{pd0}			10	C_L = 15 pF		17	25	ns
t_{pd1}	B_1	B*	11	C_L = 15 pF		48	65	ns
t_{pd0}			12	C_L = 15 pF		17	25	ns

¶ t_{pd1} is propagation delay time to logical 1 level. t_{pd0} is propagation delay time to logical 0 level.

TYPICAL APPLICATIONS

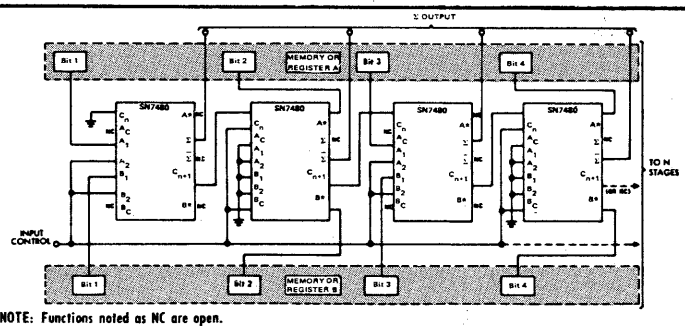
n-bit binary adder or subtractor (see figures A and B)

The SN7480 is designed specifically for N-bit adder or subtractor operations without external gates or inverters. In both applications, the sum or difference functions are generated in parallel while the carry functions are obtained serially. When the number of stages is small, the add or subtract time determines the maximum system clock rate. However, as the number of bits increases, the time required for the carry function to ripple through each bit becomes the limiting factor. Normally the ripple time of adders built with standard integrated circuits is excessive, and the resulting system speed is so slow that other more complex methods are required to perform these functions.

In the SN7480, two methods are used to reduce the carry delay. The carry circuit employs a high-speed Darlington output, and the logic gating has only one inversion between the C_n input and the $\overline{C_{n+1}}$ output. This logic configuration results in an inverted carry output, and consequently an inverted carry input to the succeeding stage. To counteract this inverted input without sacrificing propagation time through the carry, gates are provided within the circuit to invert the A and B inputs and the resulting sum or difference output. This interconnection method is illustrated by bit 2 and bit 4 of the adder (Figure A). The inverted carry output is a true carry from bit 2 and bit 4, enabling the use of noninverted A and B inputs for the odd-numbered bits.

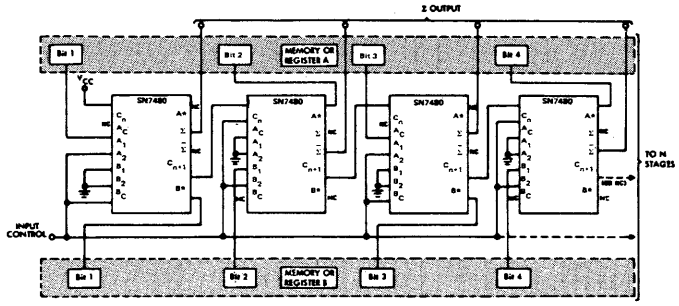
When performing subtraction (Figure B) the C_n input to bit 1 is connected to a logical 1 and input bits and input control functions for the subtrahend (memory or register B) are effectively inverted.

The input control is used to disable the A and B inputs when memory or register information is being shifted. A logical 0 applied to this line will bring each sum or difference output to a logical 0 condition and maintain this level regardless of the state of the input information into each bit. For the adder (Figure A), input control is applied to A_2 and B_2 of odd-numbered bits and to A_C and B_C of even numbered bits. For the subtractor (Figure B), input control is applied to A_2 and B_C of the odd-numbered bits and to A_C and B_2 of the even-numbered bits. These alternating patterns are necessary to complement the varying input sequence which they control.



NOTE: Functions noted as NC are open.

FIGURE A – N-BIT BINARY ADDER



NOTE: Functions noted as NC are open.

FIGURE B – N-BIT BINARY SUBTRACTOR

9

TYPICAL APPLICATIONS

n-bit binary adder with register selection (see figure C)

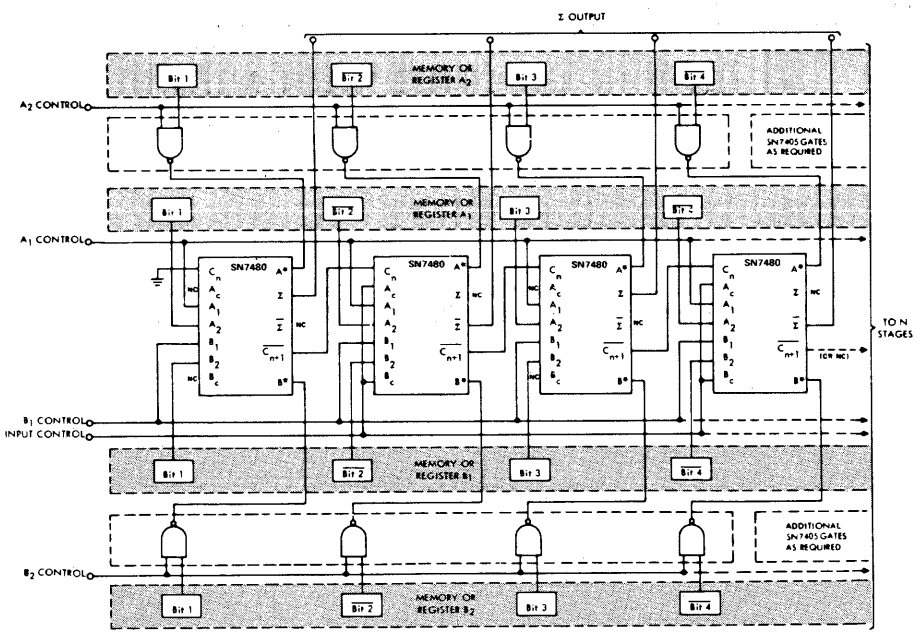
This application fully utilizes the flexibility of the input gating available within the SN7480. Two "A" registers and two "B" registers drive a single adder for each bit required. Register selection is performed internally for registers A_1 and B_1, and externally by a type SN7405 TTL gate for registers A_2 and B_2. Dot-OR logic is performed at the A★ and B★ nodes within the the adder when the register selection is made.

Operation is as follows: To add the contents of Register A_1 to Register B_1, A_2 and B_2 control lines are brought to the logical 0 state. In similar fashion, the contents of register A_1 are added to register B_2 by holding A_2 and B_1 control lines at a logical 0. Four register combinations may be used. Even-numbered input bits from each register must be inverted since the A★ and B★ inputs are being used to perform Dot-OR logic. This is not a configuration restriction for flip-flop type registers and memories, but may require additional logic elements if other storage configurations are used as inputs.

The input control function is available as in the previous application and is implemented by bringing all four register control lines and the input control line to a logical 0 level. This condition ensures a logical 0 at each Σ output regardless of "A" and "B" register logic levels.

Up to four "A" registers and four "B" registers may be implemented in a fashion analogous to that shown in Figure C. Inputs from the register-control gates (SN7405) of the additional registers would be Dot-OR connected with A_2 and B_2 registers at the A★ and B★ inputs.

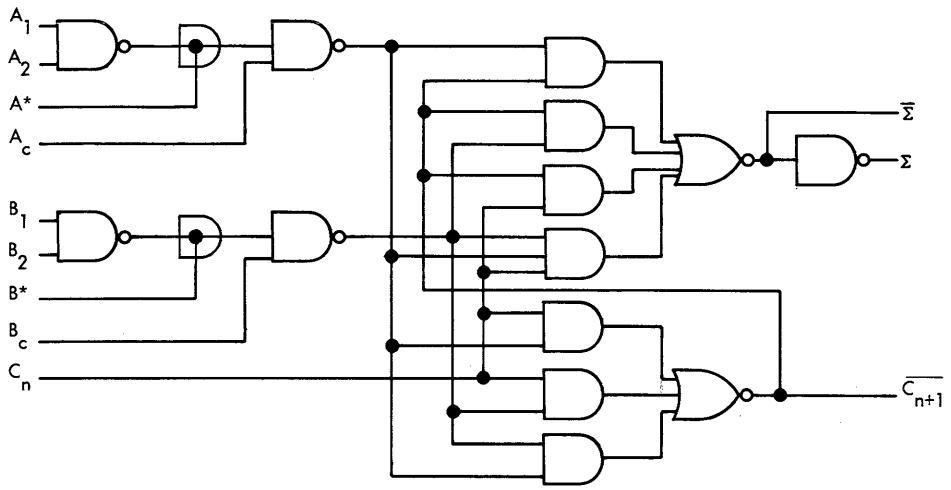
To perform N-bit subtraction, the C_n input at bit 1 is connected to a logical 1 and bit inputs from each register or memory used as a subtrahend must consist of the complement of bit inputs shown for the adder addend. Input control remains the same.



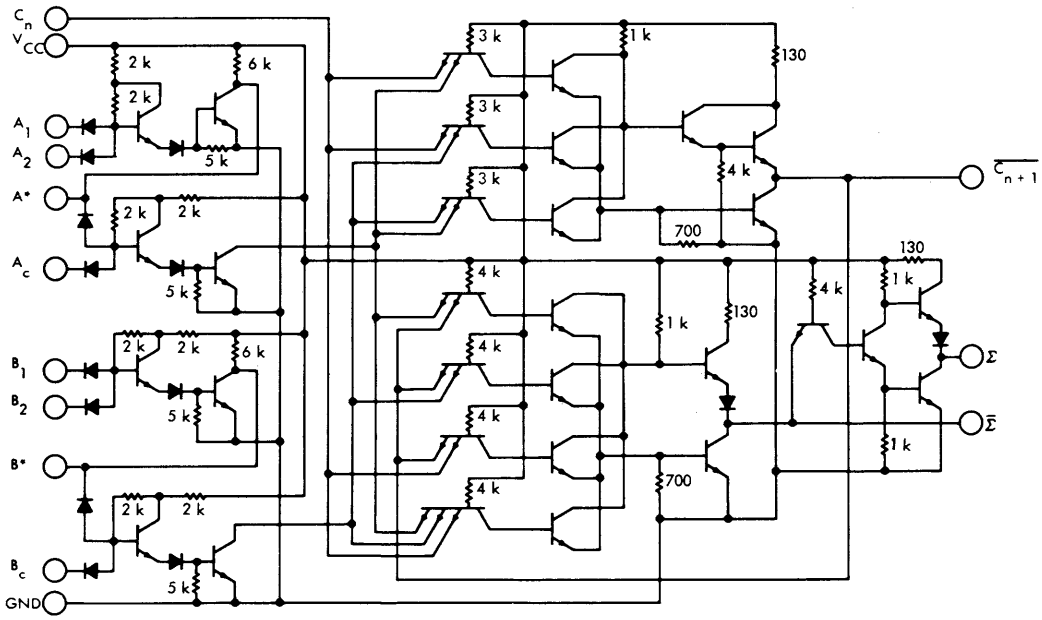
NOTE: Functions noted as NC are open.

FIGURE C–N-BIT ADDER WITH REGISTER SELECTION

functional block diagram



schematic

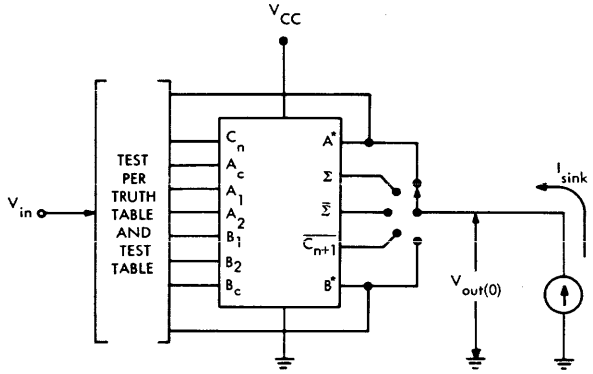


Component values shown are nominal.
Resistor values are in ohms.

9

PARAMETER MEASUREMENT INFORMATION

d-c test circuits§

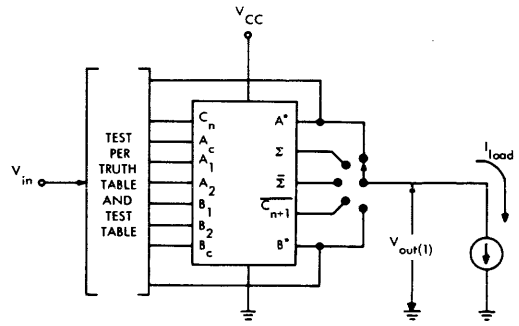


TEST TABLE

Output Under Test	I_{sink} (Min)
Σ or $\overline{\Sigma}$	16 mA
$\overline{C_{n+1}}$	8 mA
A★ or B★	4.8 mA

1. Each input or output is tested separately.
2. When A★ is tested A_1 and A_2 are at GND. When B★ is tested B_1 and B_2 are at GND.
3. When A_1 and A_2 or B_1 and B_2 is tested, A★ or B★ respectively, is open.

FIGURE 1



TEST TABLE

Output Under Test	I_{load} (Min)
Σ or $\overline{\Sigma}$	-400 μA
$\overline{C_{n+1}}$	-200 μA
A★ or B★	-120 μA

1. Each input or output is tested separately.
2. When A★ is tested A_1 and A_2 are at GND. When B★ is tested B_1 and B_2 are at GND.
3. When A_1 and A_2 or B_1 and B_2 are tested A★ or B★, respectively, is open.

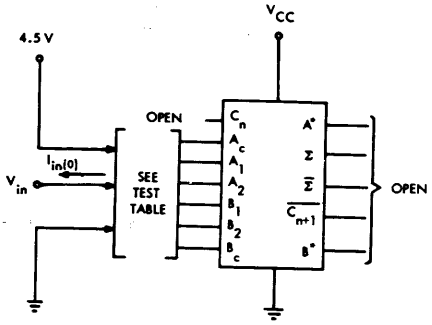
FIGURE 2

§Arrows indicate actual direction of current flow.

9

PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)

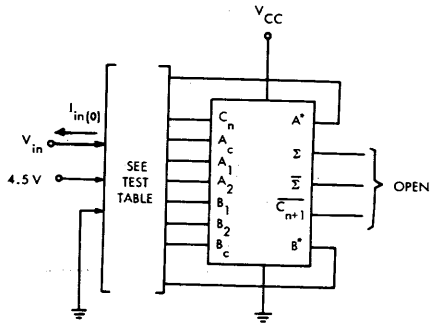


TEST TABLE

Apply V_{in} (Test $I_{in(0)}$)	Apply 4.5 V	GND
A_1	A_2	None
A_2	A_1	None
B_1	B_2	None
B_2	B_1	None
A_c	None	A_1 and A_2
B_c	None	B_1 and B_2

1. Each input is tested separately.

FIGURE 3



TEST TABLE

Apply V_{in} (Test $I_{in(0)}$)	Apply 4.5 V	GND
A★	A_c	A_1 and A_2
B★	B_c	B_1 and B_2
C_n	None	None

Unused inputs are open.

1. Each input is tested separately.

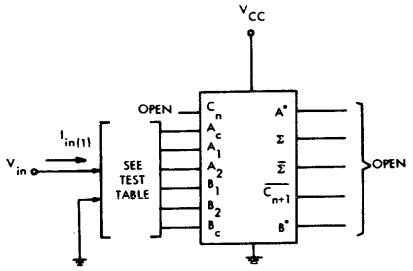
FIGURE 4

§Arrows indicate actual direction of current flow.

9

PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



1. Each input is tested separately.

TEST TABLE

Apply V_{in} (Test $I_{in(1)}$)	GND
A_1	A_2
A_2	A_1
B_1	B_2
B_2	B_1
A_c	A★
B_c	B★

FIGURE 5

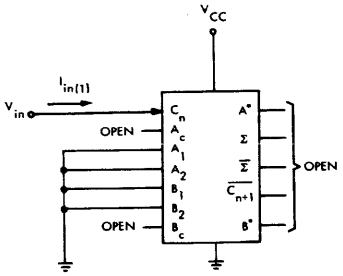
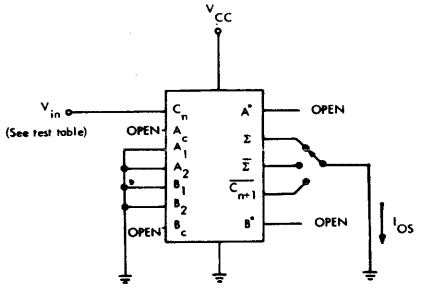


FIGURE 6



1. Each output is tested separately.

TEST TABLE

Output Under Test	V_{in} Value
$\overline{\Sigma}$	V_{CC}
$\overline{\Sigma}$ or $\overline{C_{n+1}}$	GND

FIGURE 7

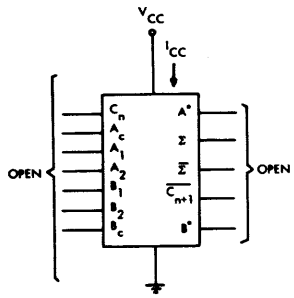


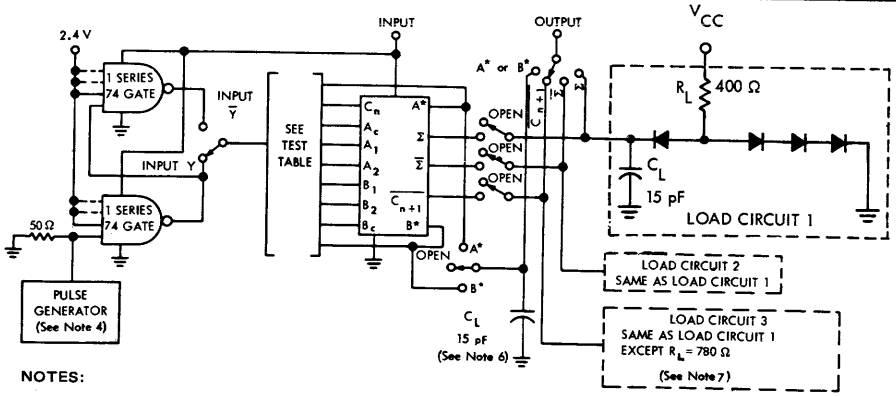
FIGURE 8

§ Arrows indicate actual direction of current flow.

9

PARAMETER MEASUREMENT INFORMATION

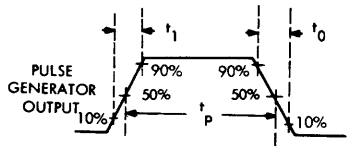
switching characteristics



NOTES:

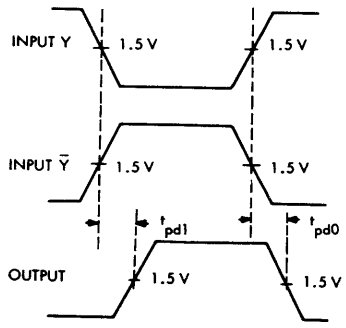
1. Perform test in accordance with test table.
2. Each output is tested separately.
3. Voltage values are with respect to network GND terminal.
4. The generator has the following characteristics: V_{gen} = 3 V, $t_1 = t_0 \leqslant 15$ ns, t_p = 0.5 μs, PRR = 1 MHz, and $Z_{out} \approx 50\ \Omega$.
5. Inputs and outputs not otherwise specified are open.
6. C_L includes probe and jig capacitance.
7. Load circuit 2 simulates output load of 5.
8. All diodes are 1N3064.

TEST CIRCUIT



TEST TABLE (See Note 5)

TEST NO.	OUTPUT UNDER TEST	APPLY INPUT $\overline{Y}$ TO	APPLY INPUT Y TO	APPLY +2.4 V TO	APPLY GND TO	APPLY OUTPUT LOADING TO
1	$\overline{C_{n+1}}$	None	C_n	None	B_1	$\overline{C_{n+1}}$ (N = 5)
2	$\overline{C_{n+1}}$	None	C_n	None	B_1	$\overline{C_{n+1}}$ (N = 5)
3	$\overline{C_{n+1}}$	B_c	None	C_n	A_1, B_1	$\overline{C_{n+1}}$ (N = 5)
4	$\overline{C_{n+1}}$	B_c	None	C_n	A_1, B_1	$\overline{C_{n+1}}$ (N = 5)
5	Σ	A_c	None	C_n	A_1, B_1	Σ (N = 10) $\overline{\Sigma}$ (N = 10) $\overline{C_{n+1}}$ (N = 5)
6	$\overline{\Sigma}$	A_c	None	C_n	A_1, B_1	Σ (N = 10) $\overline{\Sigma}$ (N = 10) $\overline{C_{n+1}}$ (N = 5)
7	$\overline{\Sigma}$	B_c	None	C_n	B_1	Σ (N = 10)
8	$\overline{\Sigma}$	B_c	None	C_n	B_1	$\overline{\Sigma}$ (N = 10)
9	A★	None	A_1	A_2	None	A★ (C_L = 15 pF)
10	A★	None	A_1	A_2	None	A★ (C_L = 15 pF)
11	B★	None	B_1	B_2	None	B★ (C_L = 15 pF)
12	B★	None	B_1	B_2	None	B★ (C_L = 15 pF)



VOLTAGE WAVEFORMS

FIGURE 9 – SWITCHING TIMES

9

CIRCUIT TYPES SN5482, SN7482
2-BIT BINARY FULL ADDERS

A HIGH-SPEED TTL 2-BIT FULL ADDER FOR APPLICATION IN

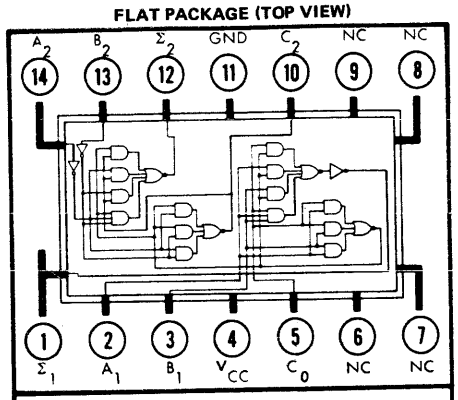
- Digital Computer Systems
- Data-Handling Systems
- Control Systems

logic

TRUTH TABLE

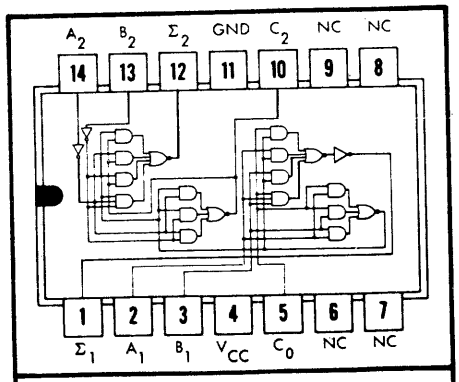
INPUT				OUTPUT					
				WHEN $C_0 = 0$			WHEN $C_0 = 1$		
A_1	B_1	A_2	B_2	Σ_1	Σ_2	C_2	Σ_1	Σ_2	C_2
0	0	0	0	0	0	0	1	0	0
1	0	0	0	1	0	0	0	1	0
0	1	0	0	1	0	0	0	1	0
1	1	0	0	0	1	0	1	1	0
0	0	1	0	0	1	0	1	1	0
1	0	1	0	1	1	0	0	0	1
0	1	1	0	1	1	0	0	0	1
1	1	1	0	0	0	1	1	0	1
0	0	0	1	0	1	0	1	1	0
1	0	0	1	1	1	0	0	0	1
0	1	0	1	1	1	0	0	0	1
1	1	0	1	0	0	1	1	0	1
0	0	1	1	0	0	1	1	0	1
1	0	1	1	1	0	1	0	1	1
0	1	1	1	1	0	1	0	1	1
1	1	1	1	0	1	1	1	1	1

W
FLAT PACKAGE (TOP VIEW)



positive logic: see truth table

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: see truth table

NC—No Internal Connection

9

description

This full adder performs the addition of two 2-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C_2) is obtained from the second bit. Designed for medium-to-high-speed, multiple-bit, parallel-add/serial-carry applications, the circuit utilizes high-speed, high-fan-out transistor-transistor logic (TTL) but is compatible with both DTL and TTL logic families. The implementation of a single-inversion, high-speed, Darlington-connected serial-carry circuit within each bit minimizes the necessity for extensive "look-ahead" and carry-cascading circuits. The power dissipation level has been maintained considerably below that attainable with equivalent standard integrated circuits connected to perform full-adder functions.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1) . . . . . 7 V
Input Voltage, V_{in} (See Notes 1 and 2) . . . . . 5.5 V
Operating Free-Air Temperature Range: SN5482 Circuits . . . . . −55°C to 125°C
SN7482 Circuits . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

NOTES: 1. These voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1): SN5482 Circuits	4.5	5	5.5	V
SN7482 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Outputs:				
C_2			5	
Σ_1 or Σ_2			10	

electrical characteristics over recommended temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1 and 2			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	1 and 2					0.8	V
$V_{out(1)}$	Logical 1 output voltage	2			2.4			V
$V_{out(0)}$	Logical 0 output voltage	1					0.4	V
$I_{in(0)}$	*Logical 0 level input current at A_1, B_1, or C_0	3	V_{CC} = MAX, V_{in} = 0.4 V				−6.4	mA
$I_{in(0)}$	Logical 0 level input current at A_2 or B_2	3	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(1)}$	Logical 1 level input current at A_1, B_1, or C_0	3	V_{CC} = MAX, V_{in} = 2.4 V				160	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at A_2 or B_2	3	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current at Σ_1 or Σ_2 §	4	V_{CC} = MAX	SN5482	−20		−55	mA
				SN7482	−18		−55	mA
I_{OS}	Short-circuit output current at C_2 §	4	V_{CC} = MAX	SN5482	−20		−70	mA
				SN7482	−18		−70	mA
I_{CC}	Supply Current	3	V_{CC} = MAX	SN5482		35	50	mA
				SN7482		35	58	mA

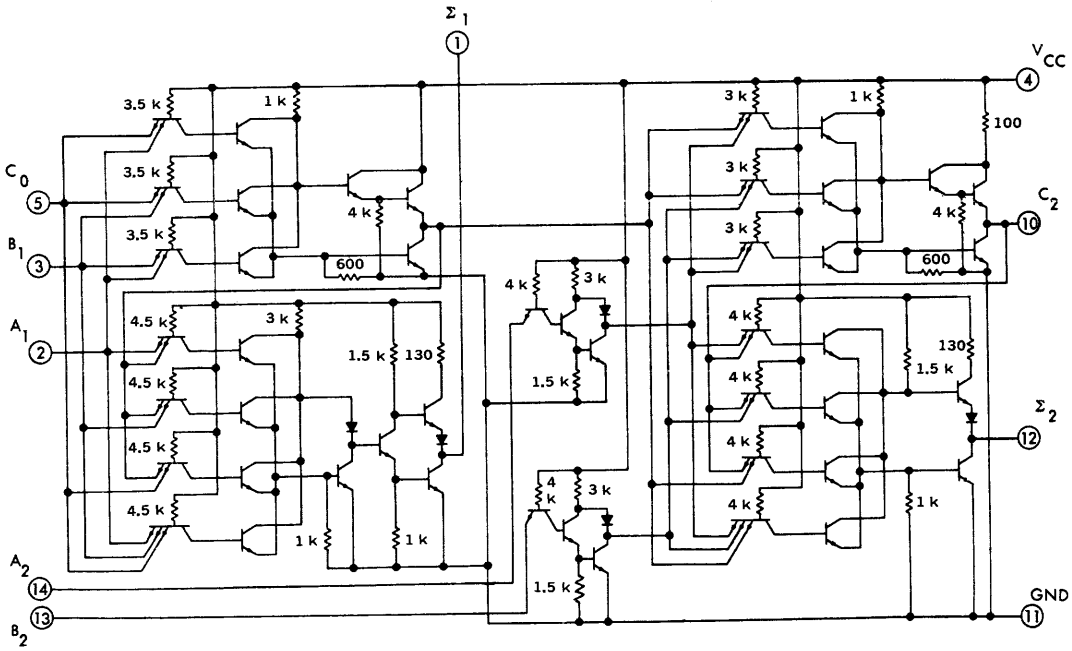
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (unless otherwise noted N = 10)

PARAMETER§	FROM (INPUT)	TO (OUTPUT)	FIGURE 5 TEST NO.	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd1}	C_0	Σ_1	1	C_L = 15 pF, R_L = 400 Ω			34	ns
t_{pd0}			2	C_L = 15 pF, R_L = 400 Ω			40	ns
t_{pd1}	B_2	Σ_2	3	C_L = 15 pF, R_L = 400 Ω			40	ns
t_{pd0}			4	C_L = 15 pF, R_L = 400 Ω			35	ns
t_{pd1}	C_0	Σ_2	5	C_L = 15 pF, R_L = 400 Ω			38	ns
t_{pd0}			6	C_L = 15 pF, R_L = 400 Ω			42	ns
t_{pd1}	C_0	C_2	7	C_L = 15 pF, R_L = 780 Ω		12	19	ns
t_{pd0}			8	C_L = 15 pF, R_L = 780 Ω		17	27	ns

§ t_{pd1} is propagation delay time to logical 1 level. t_{pd0} is propagation delay time to logical 0 level.

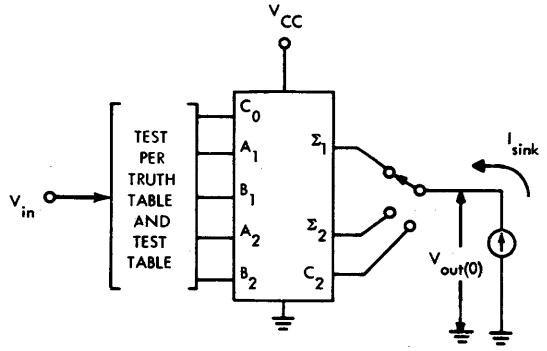
schematic



Component values shown are nominal.
Resistor values are in ohms.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits†

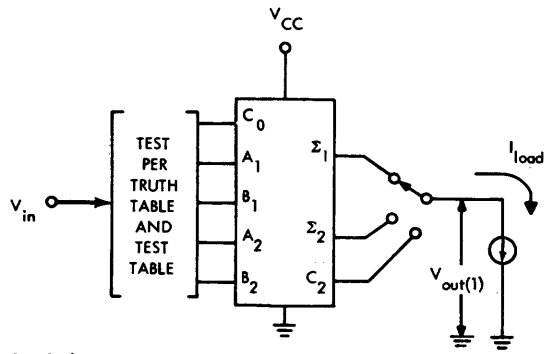


TEST TABLE

OUTPUT UNDER TEST	I_{sink}
Σ_1 or Σ_2	16 mA
C_2	8 mA

1. Each input or output is tested separately.

FIGURE 1



TEST TABLE

OUTPUT UNDER TEST	I_{load}
Σ_1 or Σ_2	−400 μA
C_2	−200 μA

1. Each input or output is tested separately.

FIGURE 2

†Arrows indicate actual direction of current flow.

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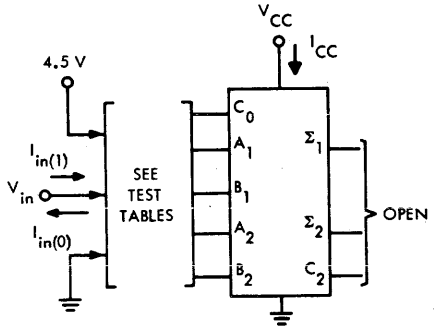
PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



$I_{in(0)}$ TEST TABLE

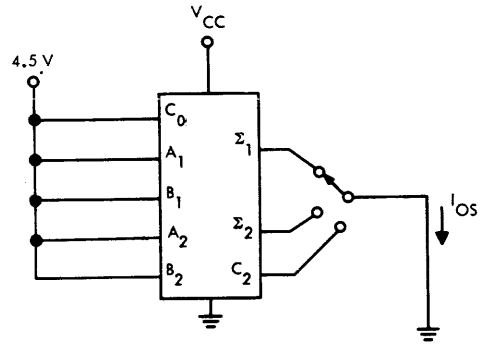
APPLY V_{in} TEST I_{in}	APPLY 4.5 V
C_0	A_1 and B_1
A_1	C_0 and B_1
B_1	C_0 and A_1
A_2	None
B_2	None

$I_{in(1)}$ TEST TABLE

APPLY V_{in} TEST I_{in}	GND
C_0	A_1 and B_1
A_1	C_0 and B_1
B_1	C_0 and A_1
A_2	None
B_2	None

1. Each input is tested separately.
2. When testing I_{CC} apply 4.5 V to A_1, A_2, and C_0; and ground B_1 and B_2.

FIGURE 3



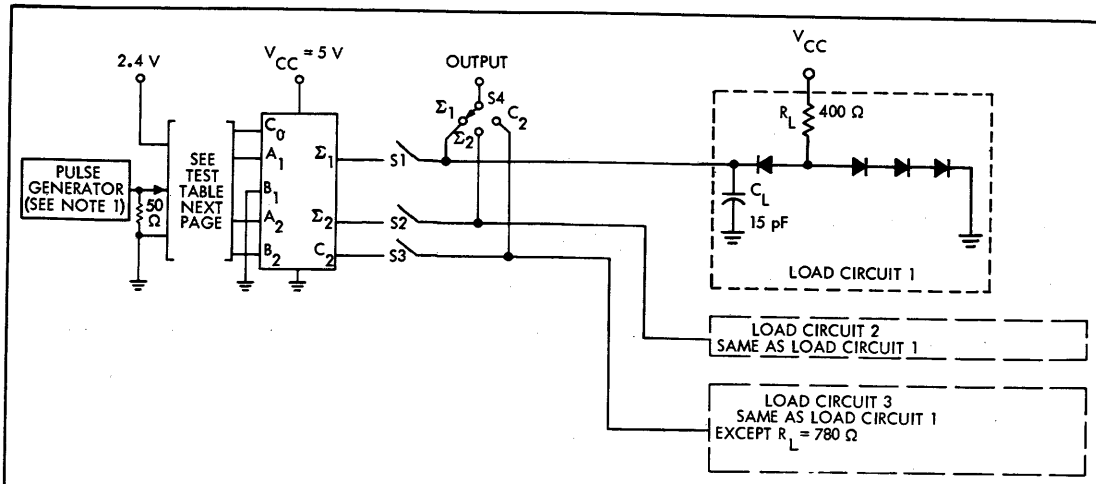
1. Each output is tested separately.

FIGURE 4

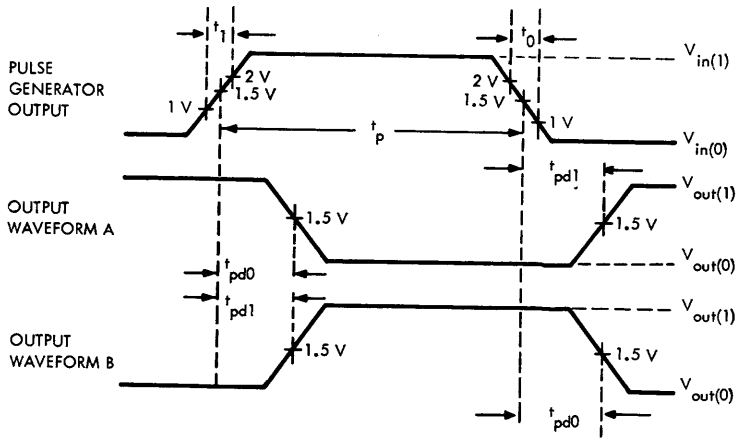
†Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES:
1. The generator has the following characteristics: $V_{in(1)} \geq 2.4$ V, $V_{in(0)} \leq 0.4$ V, t_1 = 8 to 15 ns, t_0 = 3 to 5 ns, PRR = 1 MHz, t_p = 200ns, and $Z_{out} \approx 50\ \Omega$.
2. Perform test in accordance with test table.
3. Each output is tested separately.
4. Voltage values are with respect to network ground terminal.
5. C_L includes probe and jig capacitance.
6. All diodes are 1N3064.

FIGURE 5—SWITCHING TIMES

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PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)

SWITCHING TIMES TEST TABLE (SEE NOTE 7)

TEST NO.	PARAMETER	APPLY PULSE GENERATOR OUTPUT TO	OUTPUT UNDER TEST (S4)	APPLY 2.4 V TO	APPLY GND TO	S1	S2	S3
1	t_{pd1}	C_0	Σ_1 (WAVEFORM A)	A_1	A_2, B_1, B_2	CLOSED	OPEN	OPEN
2	t_{pd0}							
3	t_{pd1}	B_2	Σ_2 (WAVEFORM B)	None	A_1, B_1, A_2 and C_0	OPEN	CLOSED	OPEN
4	t_{pd0}							
5	t_{pd1}	C_0	Σ_2 (WAVEFORM A)	A_1, A_2	B_1, B_2	OPEN	CLOSED	CLOSED
6	t_{pd0}							
7	t_{pd1}	C_0	C_2 (WAVEFORM B)	A_1, A_2	B_1, B_2	OPEN	OPEN	CLOSED
8	t_{pd0}							

NOTE 7: Inputs and outputs not otherwise specified are open.

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TEXAS INSTRUMENTS
INCORPORATED
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CIRCUIT TYPES SN5483, SN7483
4-BIT BINARY FULL ADDERS

HIGH-SPEED TTL 4-BIT FULL ADDERS FOR APPLICATION IN

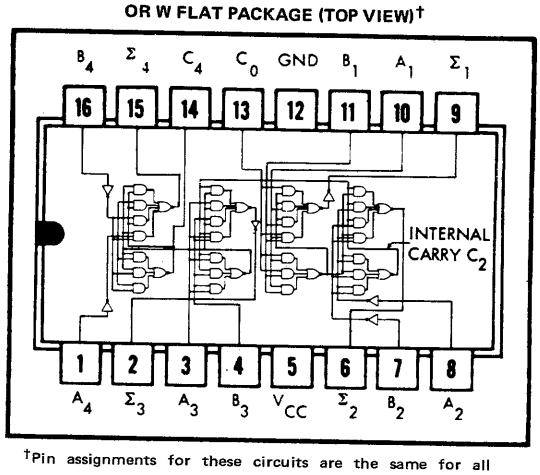
- Digital Computer Systems
- Data-Handling Systems
- Control Systems

logic

INPUT										
				WHEN $C_0 = 0$			WHEN $C_0 = 1$			
				WHEN $C_2 = 0$			WHEN $C_2 = 1$			
A_1 / A_3	B_1 / B_3	A_2 / A_4	B_2 / B_4	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_4	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_4
0	0	0	0	0	0	0	1	0	0
1	0	0	0	1	0	0	0	1	0
0	1	0	0	1	0	0	0	1	0
1	1	0	0	0	1	0	1	1	0
0	0	1	0	0	1	0	1	1	0
1	0	1	0	1	1	0	0	0	1
0	1	1	0	1	1	0	0	0	1
1	1	1	0	0	0	1	1	0	1
0	0	0	1	0	1	0	1	1	0
1	0	0	1	1	1	0	0	0	1
0	1	0	1	1	1	0	0	0	1
1	1	0	1	0	0	1	1	0	1
0	0	1	1	0	0	1	1	0	1
1	0	1	1	1	0	1	0	1	1
0	1	1	1	1	0	1	0	1	1
1	1	1	1	0	1	1	1	1	1

NOTE 1: Input conditions at A_1, A_2, B_1, B_2, and C_0 are used to determine outputs Σ_1 and Σ_2, and the value of the internal carry C_2. The values at C_2, A_3, B_3, A_4, and B_4, are then used to determine outputs Σ_3, Σ_4, and C_4.

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



†Pin assignments for these circuits are the same for all packages.

description

This full adder performs the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C_4) is obtained from the fourth bit. Designed for medium-to-high-speed, multiple-bit, parallel-add/serial-carry applications, the circuit utilizes high-speed, high-fan-out transistor-transistor logic (TTL) but is compatible with both DTL and TTL families. The implementation of a single-inversion, high-speed, Darlington-connected serial-carry circuit within each bit minimizes the necessity for extensive "look-ahead" and carry-cascading circuits. The power dissipation level has been maintained considerably below that attainable with equivalent standard integrated circuits connected to perform four-bit full-adder functions.

9

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1) . . . . . 7 V
Input Voltage, V_{in} (See Notes 1 and 2) . . . . . 5.5 V
Operating Free-Air Temperature Range: SN5483 Circuits . . . . . −55°C to 125°C
SN7483 Circuits . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

NOTES: 1. These voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: (See Note 1)	SN5483 Circuits	4.5	5	5.5	V
	SN7483 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Outputs:					
C_4				5	
$\Sigma_1, \Sigma_2, \Sigma_3$ or Σ_4				10	

electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1 and 2			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	1 and 2					0.8	V
$V_{out(1)}$	Logical 1 output voltage	2			2.4			V
$V_{out(0)}$	Logical 0 output voltage	1					0.4	V
$I_{in(0)}$	Logical 0 level input current at A_1, A_3, B_1, B_3, or C_0	3	V_{CC} = MAX,	V_{in} = 0.4 V			−6.4	mA
$I_{in(0)}$	Logical 0 level input current at A_2, A_4, B_2, or B_4	3	V_{CC} = MAX,	V_{in} = 0.4 V			−1.6	mA
$I_{in(1)}$	Logical 1 level input current at A_1, A_3, B_1, B_3, or C_0	3	V_{CC} = MAX,	V_{in} = 2.4 V			160	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at A_2, A_4, B_2, or B_4	3	V_{CC} = MAX,	V_{in} = 2.4 V			40	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current at $\Sigma_1, \Sigma_2, \Sigma_3$, or Σ_4§	4	V_{CC} = MAX	SN 5483	−20		−55	mA
				SN7483	−18		−55	mA
I_{OS}	Short-circuit output current at C_4§	4	V_{CC} = MAX	SN5483	−20		−70	mA
				SN7483	−18		−70	mA
I_{CC}	Supply Current	3	V_{CC} = MAX,	SN5483		78	110	mA
				SN7483		78	128	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (unless otherwise noted N = 10)

PARAMETER§	FROM (INPUT)	TO (OUTPUT)	FIGURE 5 TEST NO.	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd1}	C_0	1	1	C_L = 15 pF, R_L = 400 Ω			34	ns
t_{pd0}			2	C_L = 15 pF, R_L = 400 Ω			40	ns
t_{pd1}	C_0	2	3	C_L = 15 pF, R_L = 400 Ω			38	ns
t_{pd0}			4	C_L = 15 pF, R_L = 400 Ω			42	ns
t_{pd1}	C_0	3	5	C_L = 15 pF, R_L = 400 Ω			50	ns
t_{pd0}			6	C_L = 15 pF, R_L = 400 Ω			60	ns
t_{pd1}	C_0	4	7	C_L = 15 pF, R_L = 400 Ω			55	ns
t_{pd0}			8	C_L = 15 pF, R_L = 400 Ω			55	ns
t_{pd1}	C_0	C_4	9	C_L = 15 pF, R_L = 780 Ω		35	48	ns
t_{pd0}			10	C_L = 15 pF, R_L = 780 Ω		22	32	ns
t_{pd1}	A_2 or B_2	2	11 and 13	C_L = 15 pF, R_L = 400 Ω			40	ns
t_{pd0}			12 and 14	C_L = 15 pF, R_L = 400 Ω			35	ns
t_{pd1}	A_4 or B_4	4	15 and 17	C_L = 15 pF, R_L = 400 Ω			40	ns
t_{pd0}			16 and 18	C_L = 15 pF, R_L = 400 Ω			35	ns

§ t_{pd1} is propagation delay time to logical 1 level. t_{pd0} is propagation delay time to logical 0 level.

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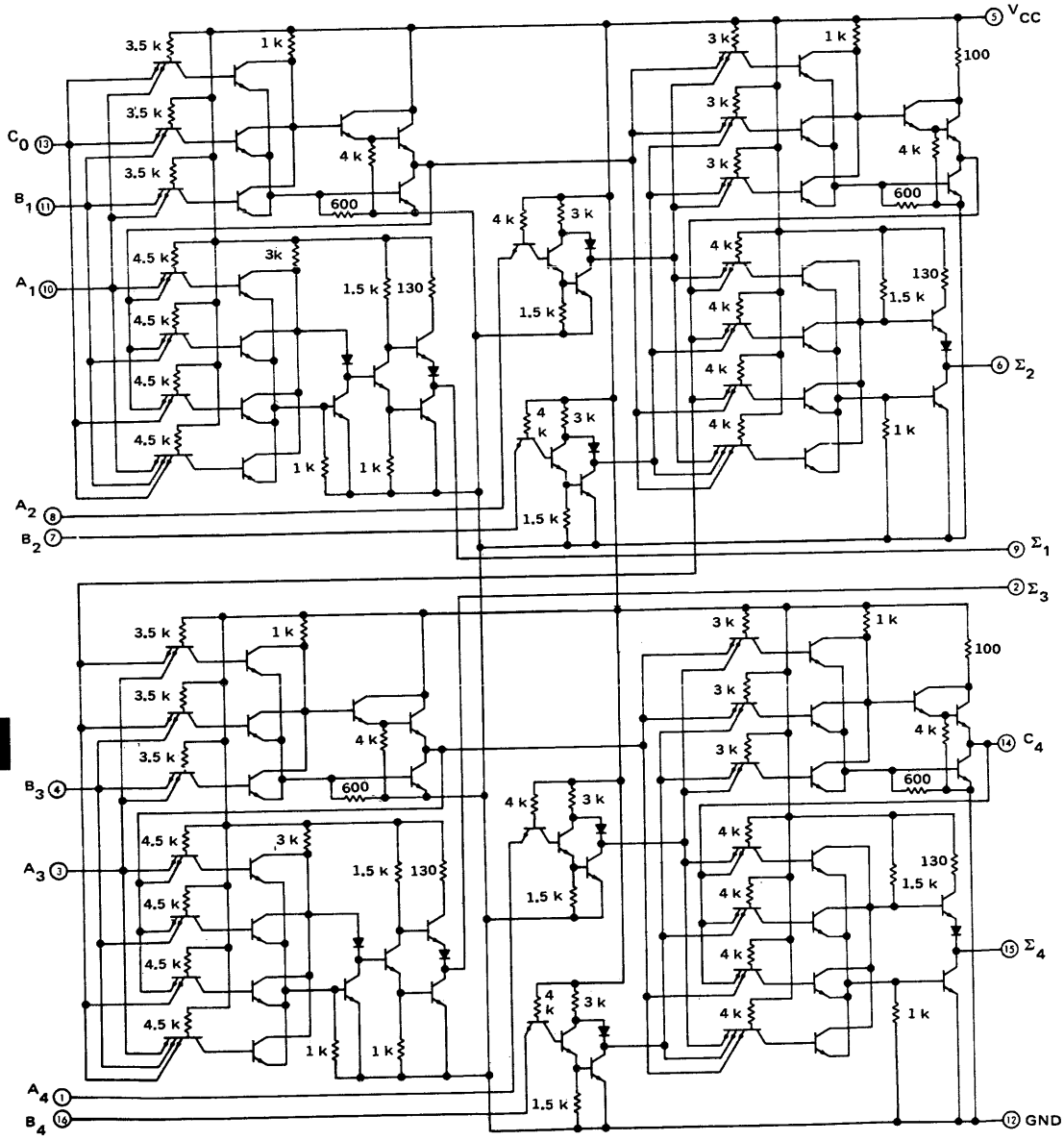
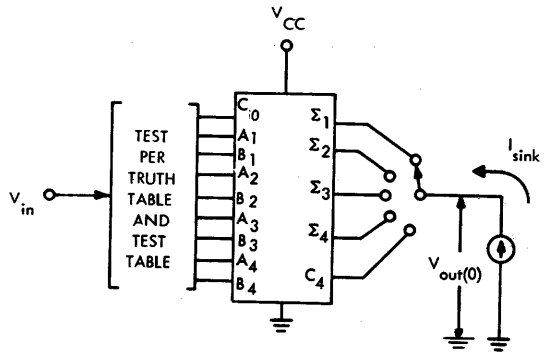
schematic



Component values shown are nominal.
Resistor values are in ohms.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits†

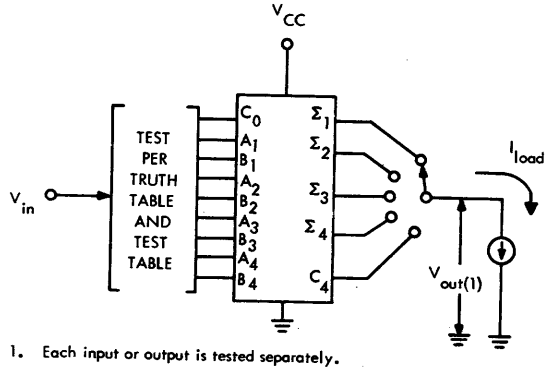


TEST TABLE

OUTPUT UNDER TEST	I_{sink}
Σ_1, Σ_2, Σ_3, or Σ_4	16 mA
C_4	8 mA

1. Each input or output is tested separately.

FIGURE 1



TEST TABLE

OUTPUT UNDER TEST	I_{load}
Σ_1, Σ_2, Σ_3, or Σ_4	− 400 μA
C_4	− 200 μA

1. Each input or output is tested separately.

FIGURE 2

†Arrows indicate actual direction of current flow.

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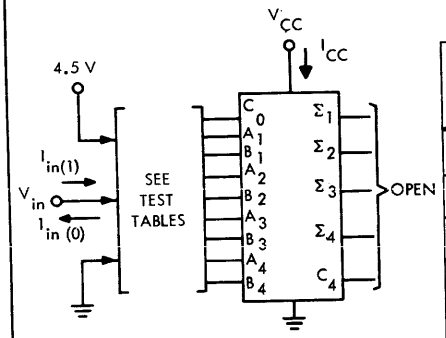
PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



1. Each input is tested separately.
2. When testing I_{CC} apply 4.5 V to A_1, A_2, A_3, A_4, and C_0; and ground B_1, B_2, B_3 and B_4.

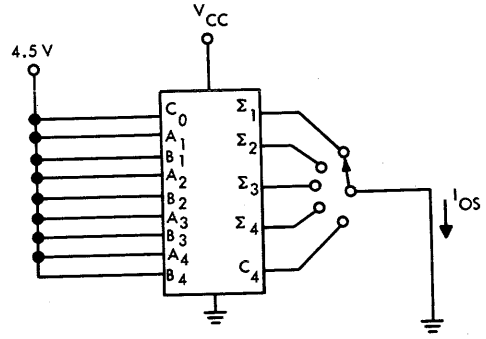
$I_{in(0)}$ TEST TABLE

APPLY V_{in} TEST I_{in}	APPLY 4.5 V
C_0	A_1 and B_1
A_1	C_0 and B_1
B_1	C_0 and A_1
A_2	None
B_2	None
A_3	A_2, B_2, and B_3
B_3	A_2, B_2, and A_3
A_4	None
B_4	None

$I_{in(1)}$ TEST TABLE

APPLY V_{in} TEST I_{in}	GND
C_0	A_1 and B_1
A_1	C_0 and B_1
B_1	C_0 and A_1
A_2	None
B_2	None
A_3	A_2, B_2, and B_3
B_3	A_2, B_2, and A_3
A_4	None
B_4	None

FIGURE 3



1. Each output is tested separately.

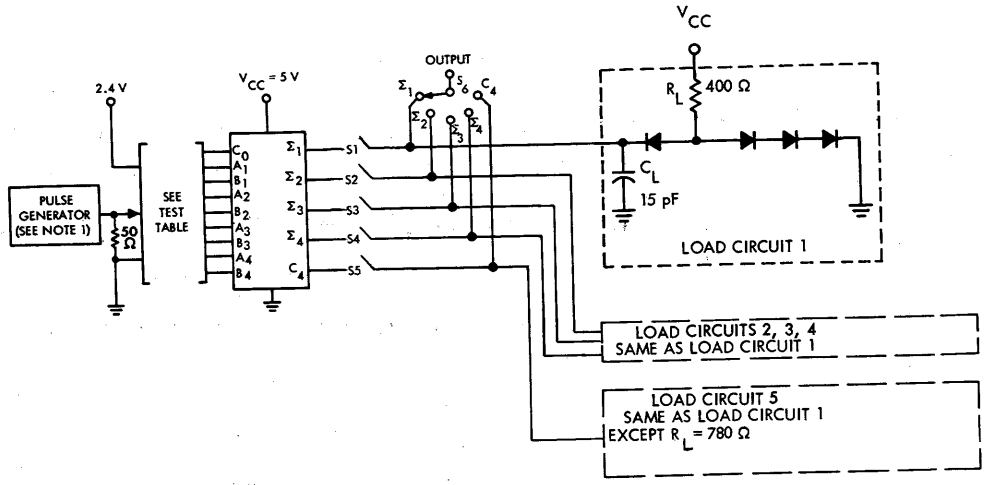
FIGURE 4

†Arrows indicate actual direction of current flow.

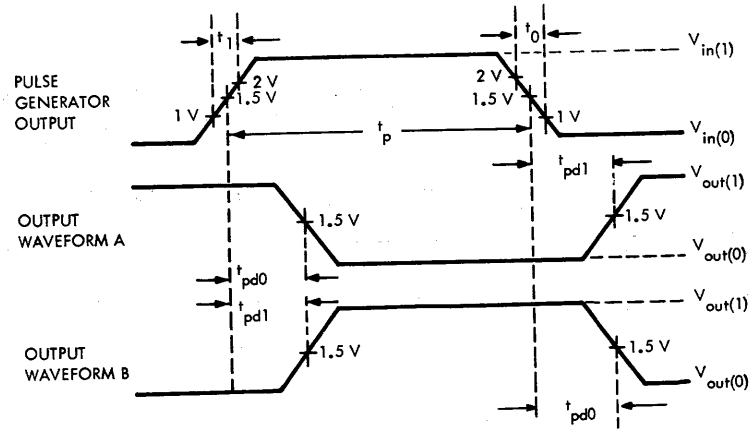
9

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES:
1. Pulse generator output pulse characteristics: $V_{in(1)} \geq$ 2.4 V, $V_{in(0)} \leq$ 0.4 V, t_1 = 8 to 15 ns, t_0 = 3 to 5 ns, PRR = 1 MHz, t_p = 200 ns, and $Z_{out} \approx$ 50 Ω.
2. Perform test in accordance with test table. (See sheet 2 of this figure.)
3. Each output is tested separately.
4. Voltage values are with respect to network ground terminal.
5. C_L includes probe and jig capacitance.
6. All diodes are 1N3064

FIGURE 5–SWITCHING TIMES (SHEET 1 OF 2)

9

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)

TEST TABLE (SEE NOTE 7)

TEST NO.	PARAMETER	APPLY PULSE GENERATOR OUTPUT TO	OUTPUT UNDER TEST (S6)	APPLY 2.4 V TO	APPLY GND TO	S1	S2	S3	S4	S5
1	t_{pd1}	C_0	Σ_1 (WAVEFORM A)	A_1	B_1, A_2, and B_2	CLOSED	OPEN	OPEN	OPEN	OPEN
2	t_{pd0}									
3	t_{pd1}	C_0	Σ_2 (WAVEFORM A)	A_1 and A_2	B_1 and B_2	OPEN	CLOSED	OPEN	OPEN	OPEN
4	t_{pd0}									
5	t_{pd1}	C_0	Σ_3 (WAVEFORM A)	A_1, A_2, and A_3	B_1, B_2, and B_3	OPEN	OPEN	CLOSED	OPEN	OPEN
6	t_{pd0}									
7	t_{pd1}	C_0	Σ_4 (WAVEFORM A)	A_1, A_2, A_3, and A_4	B_1, B_2, B_3, and B_4	OPEN	OPEN	OPEN	CLOSED	CLOSED
8	t_{pd0}									
9	t_{pd1}	C_0	C_4 (WAVEFORM B)	A_1, A_2, A3, and A_4	B_1, B_2, B_3, and B_4	OPEN	OPEN	OPEN	OPEN	CLOSED
10	t_{pd0}									
11	t_{pd1}	A_2	Σ_2 (WAVEFORM B)	None	A_1, B_1, B_2, and C_0	OPEN	CLOSED	OPEN	OPEN	OPEN
12	t_{pd0}									
13	t_{pd1}	B_2	Σ_2 (WAVEFORM B)	None	A_1, B_1, A_2, and C_0	OPEN	CLOSED	OPEN	OPEN	OPEN
14	t_{pd0}									
15	t_{pd1}	A_4	Σ_4 (WAVEFORM B)	None	A_3, B_3, and B_4	OPEN	OPEN	OPEN	CLOSED	OPEN
16	t_{pd0}									
17	t_{pd1}	B_4	Σ_4 (WAVEFORM B)	None	A_3, B_3, and A_4	OPEN	OPEN	OPEN	CLOSED	OPEN
18	t_{pd0}									

NOTE 7: Inputs and outputs not otherwise specified are open.

FIGURE 5 – SWITCHING TIMES (SHEET 2 of 2)

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN54LS83, SN74LS83 4-BIT BINARY FULL ADDERS

BULLETIN NO. DL-S 7111458, MARCH 1971

HIGH-SPEED TTL 4-BIT FULL ADDERS

- Schottky-Diode-Clamped Transistors †
- Low Power Dissipation 75 mW Typical

FOR APPLICATION IN

- Digital Computer Systems
- Data-Handling Systems
- Control Systems

description

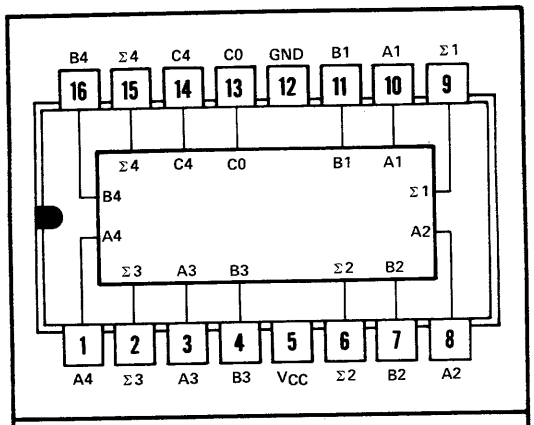
The SN54LS83 and SN74LS83 low-power Schottky TTL circuits are implemented with full Schottky-barrier-diode clamping to achieve speeds comparable to Standard Series 54/74 at one-fifth of the power. They retain the desirable features of, and are completely compatible with, most of the popular saturated logic circuits. Schottky TTL circuits currently offer the best speed-power products of any high-speed logic family.

Schottky-barrier-diode clamping prevents transistors from achieving classic saturation and thereby effectively eliminates excess charge storage and subsequent recovery times. These recovery times contribute significantly to overall propagation delays experienced with saturated digital-logic circuits.

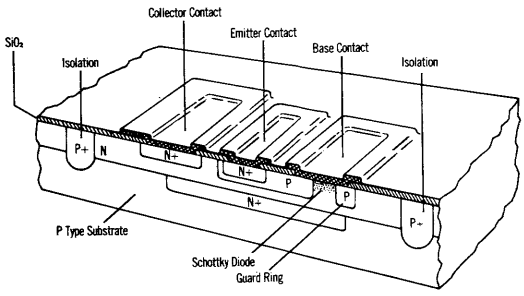
These full adders perform the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit. Designed for medium-to-high-speed, the circuit utilizes high-speed, high-fan-out transistor-transistor logic (TTL) but is compatible with both DTL and TTL families. The implementation of a single-inversion, high-speed, Darlington-connected serial-carry circuit within each bit minimizes the necessity for extensive "look-ahead" and carry-cascading circuits. The power dissipation level is an order of magnitude below that attainable with standard integrated circuits connected to perform four-bit full-adder functions.

The SN54LS83 and SN74LS83 are completely compatible with the Series 54/74, Series 54H/74H, Series 54L/74L, and Series 54S/74S logic families. The SN54LS83 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74LS83 is characterized for operation from 0°C to 70°C.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: See truth table



†The integrated Schottky-barrier-diode-clamped transistor is patented by Texas Instruments. U.S. patent number 3,463,975.

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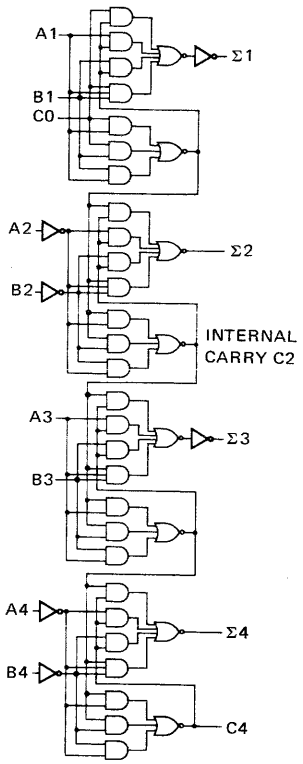
CIRCUIT TYPES SN54LS83, SN74LS83
4-BIT BINARY FULL ADDERS

functional block diagram



TRUTH TABLE

INPUT				OUTPUT					
				WHEN C0 = L			WHEN C0 = H		
						WHEN C2 = L			WHEN C2 = H
A1 / A3	B1 / B3	A2 / A4	B2 / B4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

NOTE 1: Input conditions at A1, A2, B2, and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4, are then used to determine outputs Σ3, Σ4, and C4.

9 absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54LS83 Circuits . . . . . −55°C to 125°C
SN74LS83 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter input transistor.

recommended operating conditions

	SN54LS83			SN74LS83			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−200			−200	μA
Low-level output current, I_{OL}			4			4	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

TEXAS INSTRUMENTS
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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH} High-level input voltage		1 and 2			2			V
V_{IL} Low-level input voltage		1 and 2					0.9	V
V_I Input clamp voltage		3	V_{CC} = MIN, I_I = −18 mA				−1.2	V
V_{OH} High-level output voltage		2	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.9 V, I_{OH} = −200 μA		2.4			V
V_{OL} Low-level output voltage		1	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.9 V, I_{OL} = 4 mA				0.5	V
I_I Input current at maximum input voltage		3	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH} High-level input current	A1, A3, B1, B3, or C0	3	V_{CC} = MAX, V_I = 2.4 V				160	μA
	A2, A4, B2, or B4						40	
I_{IL} Low-level input current	A1, A3, B1, B3, or C0	3	V_{CC} = MAX, V_I = 0.5 V				−1.44	mA
	A2, A4, B2, or B4						−0.36	
I_{OS} Short-circuit output current§		4	V_{CC} = MAX		−6		−40	mA
I_{CC} Supply current		5	V_{CC} = MAX	SN54LS83		15	22	mA
				SN74LS83		15	26	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (unless otherwise noted N = 10)

PARAMETER¶	FROM INPUT	TO OUTPUT	FIGURE 6 TEST NO.	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	C0	Σ1	1	C_L = 50 pF, R_L = 2 kΩ		31		ns
t_{PHL}			2			38		ns
t_{PLH}	C0	Σ2	3			49		ns
t_{PHL}			4			45		ns
t_{PLH}	C0	Σ3	5			53		ns
t_{PHL}			6			66		ns
t_{PLH}	C0	Σ4	7			70		ns
t_{PHL}			8			69		ns
t_{PLH}	C0	C4	9			50		ns
t_{PHL}			10			50		ns
t_{PLH}	A2 or B2	Σ2	11 and 13			35		ns
t_{PHL}			12 and 14			30		ns
t_{PLH}	A4 or B4	Σ4	15 and 17			35		ns
t_{PHL}			16 and 18			30		ns

¶t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output.

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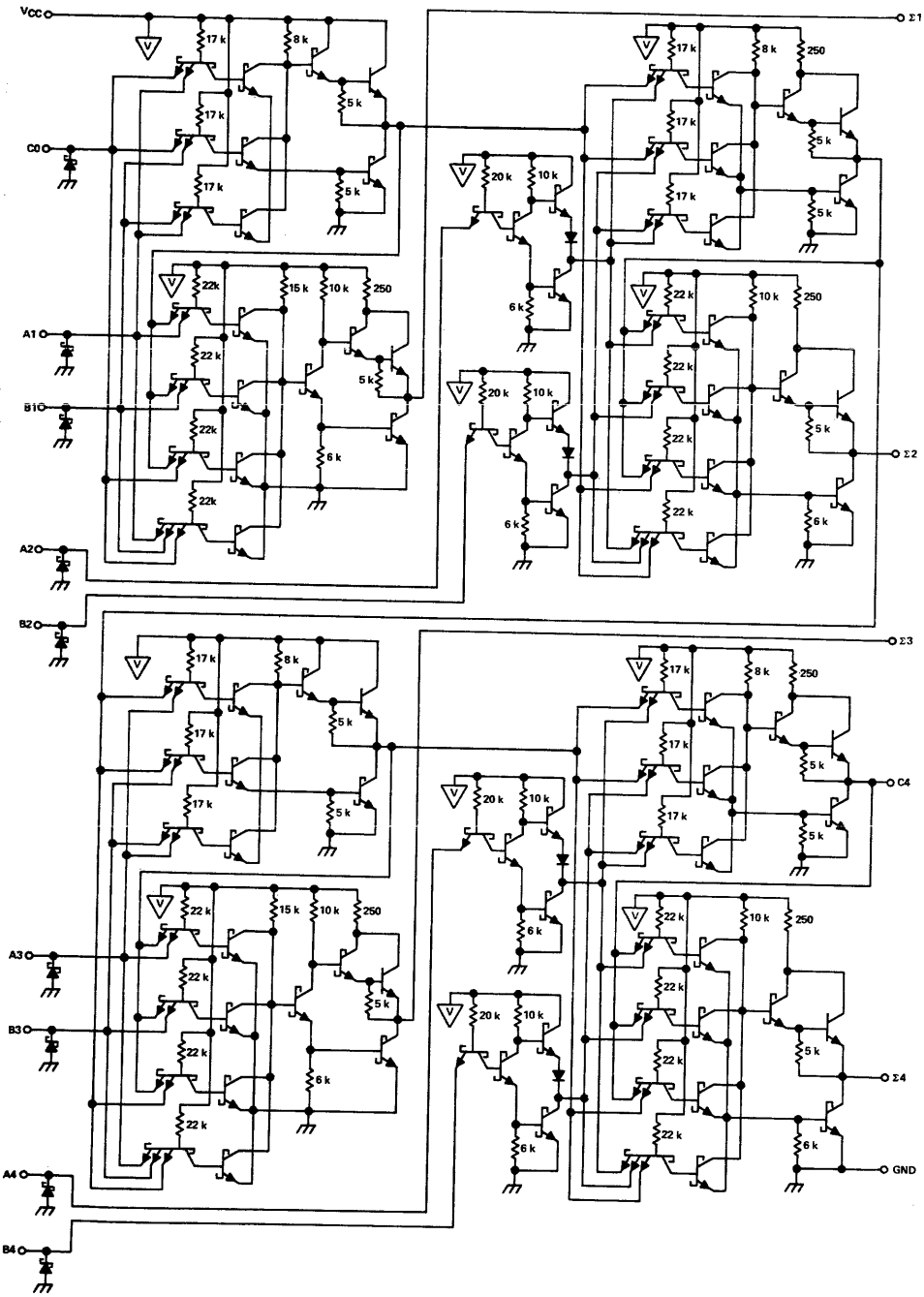
CIRCUIT TYPES SN54LS83, SN74LS83
4-BIT BINARY FULL ADDERS

schematic



▽ . . . V_{CC} bus

Resistor values are nominal in ohms.

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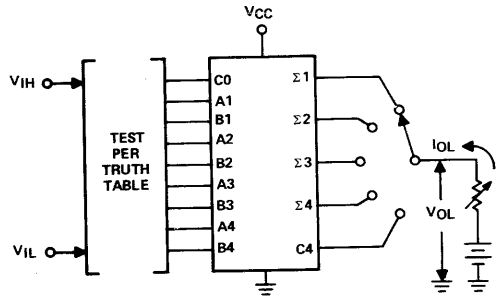
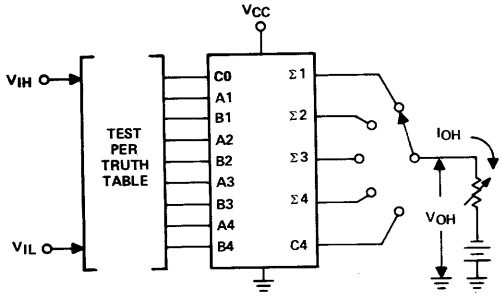
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



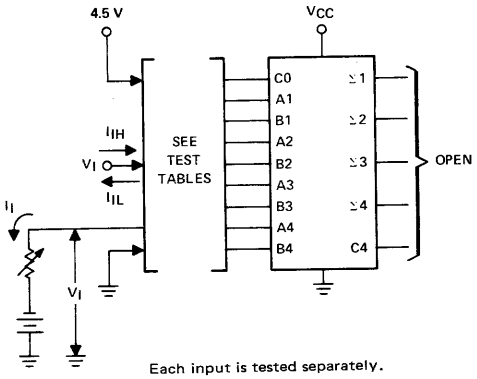
Each input or output is tested separately.

FIGURE 1–V_{IH}, V_{IL}, V_{OL}



Each input or output is tested separately.

FIGURE 2–V_{IH}, V_{IL}, V_{OH}



Each input is tested separately.

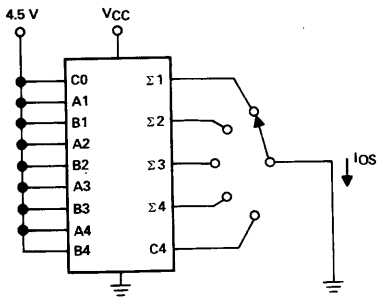
V_I, I_{IL} TEST TABLE

APPLY I_I, TEST V_I OR APPLY V_I, TEST I_{IL}	APPLY 4.5 V
C0	A1 and B1
A1	C0 and B1
B1	C0 and A1
A2	None
B2	None
A3	A2, B2, and B3
B3	A2, B2, and A3
A4	None
B4	None

I_{IH} TEST TABLE

APPLY V_I TEST I_{IH}	GND
C0	A1 and B1
A1	C0 and B1
B1	C0 and A1
A2	None
B2	None
A3	A2, B2, and B3
B3	A2, B2, and A3
A4	None
B4	None

FIGURE 3–V_I, I_{IL}, I_{IH}



Each output is tested separately.

FIGURE 4–I_{OS}

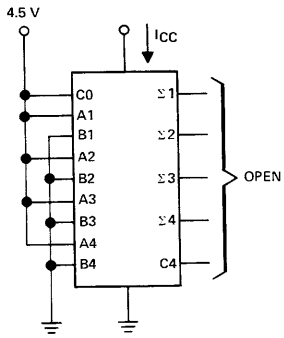
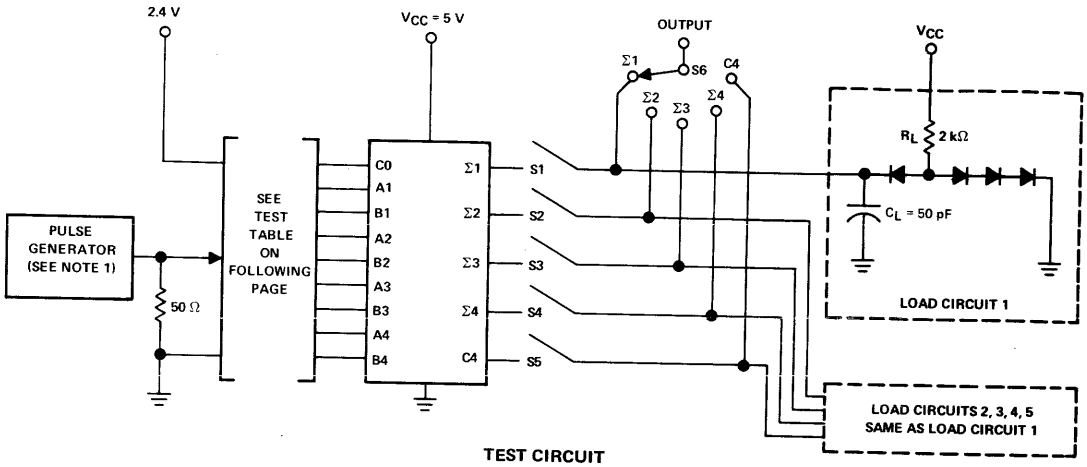


FIGURE 5–I_{CC}

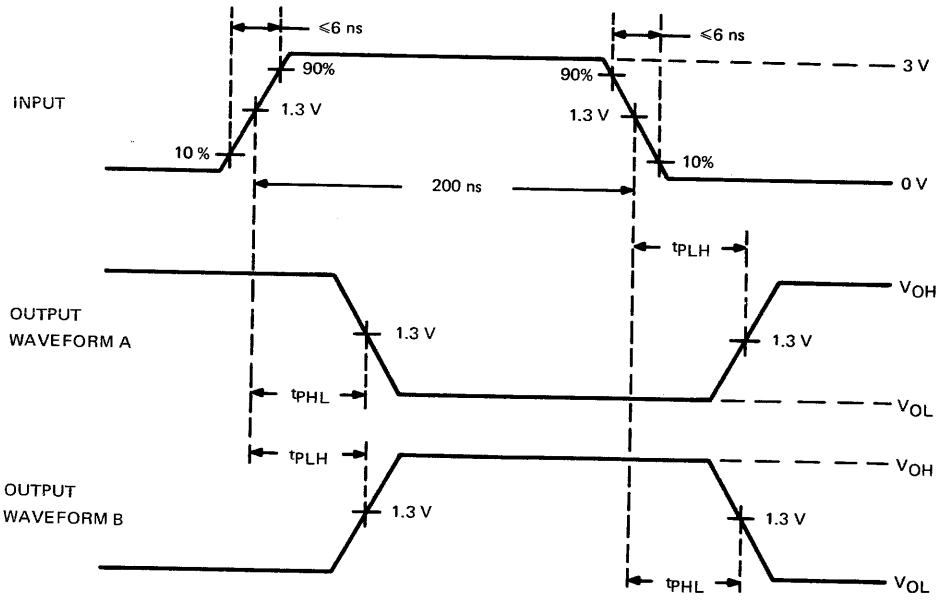
†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES
1. The pulse generator has the following characteristics: PRR ≤ 1 MHz, $Z_{out} \approx 50\ \Omega$.
2. Perform test in accordance with test table. (See sheet 2 of this figure.)
3. Each output is tested separately.
4. Voltage values are with respect to network ground terminal.
5. C_L includes probe and jig capacitance.
6. All diodes are 1N3064.

FIGURE 6—SWITCHING TIMES (SHEET 1 OF 2)

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)

TEST TABLE (SEE NOTE 7)

TEST NO.	PARAMETER	INPUT UNDER TEST	OUTPUT UNDER TEST (S6)	APPLY 2.4 V TO	APPLY GND TO	S1	S2	S3	S4	S5
1	t_{PLH}	C0	$\Sigma 1$ (Waveform A)	A1	B1, A2, and B2	Closed	Open	Open	Open	Open
2	t_{PHL}									
3	t_{PLH}	C0	$\Sigma 2$ (Waveform A)	A1 and A2	B1 and B2	Open	Closed	Open	Open	Open
4	t_{PHL}									
5	t_{PLH}	C0	$\Sigma 3$ (Waveform A)	A1, A2, and A3	B1, B2, and B3	Open	Open	Closed	Open	Open
6	t_{PHL}									
7	t_{PLH}	C0	$\Sigma 4$ (Waveform A)	A1, A2, A3, and A4	B1, B2, B3, and B4	Open	Open	Open	Closed	Closed
8	t_{PHL}									
9	t_{PLH}	C0	C4 (Waveform B)	A1, A2, A3, and A4	B1, B2, B3, and B4	Open	Open	Open	Open	Closed
10	t_{PHL}									
11	t_{PLH}	A2	$\Sigma 2$ (Waveform B)	None	A1, B1, B2, and C0	Open	Closed	Open	Open	Open
12	t_{PHL}									
13	t_{PLH}	B2	$\Sigma 2$ (Waveform B)	None	A1, B1, A2, and C0	Open	Closed	Open	Open	Open
14	t_{PHL}									
15	t_{PLH}	A4	$\Sigma 4$ (Waveform B)	None	A3, B3, and B4	Open	Open	Open	Closed	Open
16	t_{PHL}									
17	t_{PLH}	B4	$\Sigma 4$ (Waveform B)	None	A3, B3, and A4	Open	Open	Open	Closed	Open
18	t_{PHL}									

NOTE 7: Inputs and outputs are open unless otherwise specified.

FIGURE 5–SWITCHING TIMES (SHEET 2 OF 2)

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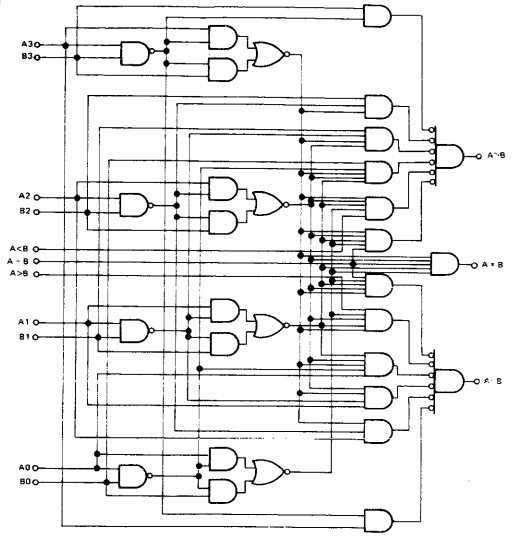
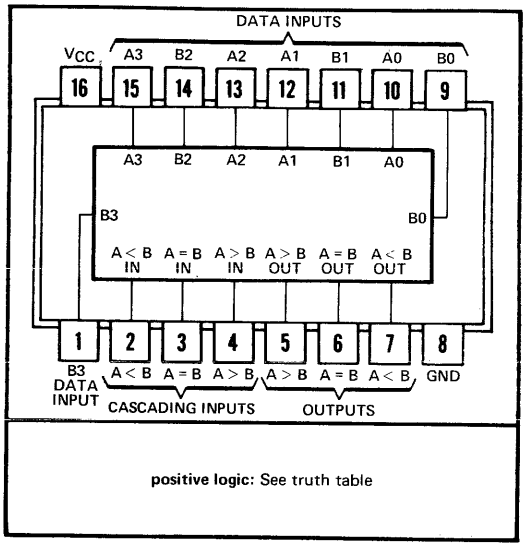
CIRCUIT TYPES SN5485, SN7485
4-BIT MAGNITUDE COMPARTORS

functional block diagram



J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)†



positive logic: See truth table

†Pin assignments for these circuits are the same for all packages.

description

The SN5485 and SN7485 perform magnitude comparison of straight binary and straight BCD (8421) codes. Three fully decoded decisions about two 4-bit words (A, B) are made and are externally available at three outputs. These devices are fully expandable to any number of bits without external gates. When cascaded, the total time for comparison is the function of the word length; however, only a two-gate-level delay (12 ns) is added for each four-bit expansion.

These circuits are completely compatible with most TTL and DTL families. Typical average power dissipation is 275 milliwatts. The SN5485 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN7485 is characterized for operation from 0°C to 70°C.

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TRUTH TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H

NOTE: H = high level, L = low level, X = irrelevant

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN5485 Circuits . . . . . −55°C to 125°C
SN7485 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter input transistor.

recommended operating conditions

	SN5485			SN7485			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N			10			10	
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage					2			V
V_{IL}	Low-level input voltage							0.8	V
V_I	Input clamp voltage		V_{CC} = MIN,	I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = −400 μA		2.4			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 16 mA				0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V				1	mA
I_{IH}	High-level input current	A < B, A > B inputs	V_{CC} = MAX,	V_I = 2.4 V				40	μA
		all other inputs						120	
I_{IL}	Low-level input current	A < B, A > B inputs	V_{CC} = MAX,	V_I = 0.4 V				−1.6	mA
		all other inputs						−4.8	
I_{OS}	Short-circuit output current§		V_{CC} = MAX,	V_O = 0	SN5485	−20		−55	mA
					SN7485	−18		−55	
I_{CC}	Supply current		V_{CC} = MAX,	See Note 3			55	88	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 3: I_{CC} is measured with outputs open, A = B grounded, and all other inputs at 4.5 V.

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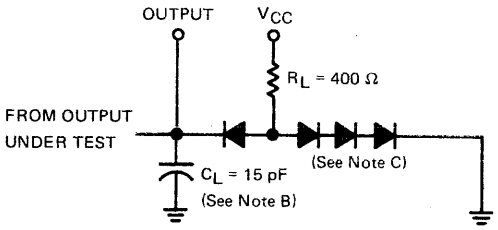
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

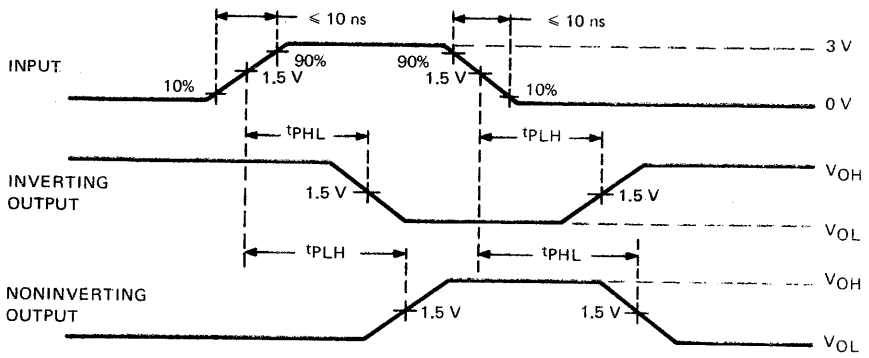
PARAMETER¶	FROM INPUT	TO OUTPUT	NUMBER OF GATE LEVELS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any A or B data input	A < B, A > B	1	C_L = 15 pF, R_L = 400 Ω, See Figure 1		7		ns
			2			12		
			3			17	26	
		A = B	4			23	35	
t_{PHL}	Any A or B data input	A < B, A > B	1			11		ns
			2			15		
			3			20	30	
		A = B	4			20	30	
t_{PLH}	A < B or A = B	A > B	1			7	11	ns
t_{PHL}	A < B or A = B	A > B	1			11	17	ns
t_{PLH}	A = B	A = B	2			13	20	ns
t_{PHL}	A = B	A = B	2			11	17	ns
t_{PLH}	A > B or A = B	A < B	1			7	11	ns
t_{PHL}	A > B or A = B	A < B	1			11	17	ns

¶ t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output.

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. Input pulses are supplied by a pulse generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.

FIGURE 1–PROPAGATION DELAY TIMES

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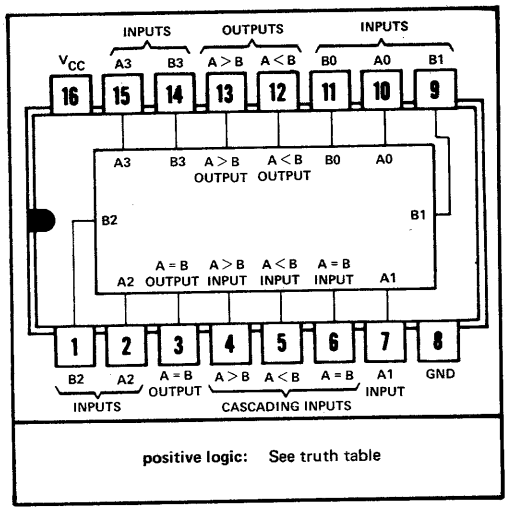
CIRCUIT TYPES SN54L85, SN74L85
4-BIT MAGNITUDE COMPARATORS

description

These 4-bit magnitude comparators compare two 4-bit words and determine their relative magnitude with the result being indicated by a high-level voltage at the A > B, A < B, or A = B output. Words of greater length may be compared by connecting comparators in cascade. The A > B, A < B, and A = B outputs of a stage handling less significant bits are connected to the corresponding A > B, A < B, and A = B inputs of the next stage handling more significant bits. The stage handling the least significant bits must have a low-level voltage applied to the A > B and A < B inputs and a high-level voltage applied to the A = B input.

These circuits utilize low-power transistor-transistor-logic (TTL), but are fully compatible with most TTL and DTL families. Power dissipation is typically 20 mW per package. The SN54L85 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74L85 is characterized for operation from 0°C to 70°C.

J OR N
DUAL-IN-LINE PACKAGE



positive logic: See truth table

logic

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H

NOTE: H = high level, L = low level, X = irrelevant

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) . . . . . 8 V
Input voltage (see Notes 1 and 2) . . . . . 5.5 V
Operating free-air temperature range: SN54L85 Circuits . . . . . −55°C to 125°C
SN74L85 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input voltages must be zero or positive with respect to network ground terminal.

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recommended operating conditions

	SN54L85			SN74L85			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N			10			10	
Operating free-air temperature range, T_A	−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
V_{IH}	High-level input voltage	1		2		V
V_{IL}	Low-level input voltage	2			0.7	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, I_{OH} = −100 μA	2.4		V
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, I_{OL} = 2 mA		0.3	V
I_{IH}	High-level input current into any A or B input	3	V_{CC} = MAX, V_I = 2.4 V		30	μA
			V_{CC} = MAX, V_I = 5.5 V		300	
I_{IH}	High-level input current into A > B, A < B, or A = B input	3	V_{CC} = MAX, V_I = 2.4 V		10	μA
			V_{CC} = MAX, V_I = 5.5 V		100	
I_{IL}	Low-level input current into any A or B input	3	V_{CC} = MAX, V_I = 0.3 V		−0.54	mA
I_{IL}	Low-level input current into A > B, A < B, or A = B input	3	V_{CC} = MAX, V_I = 0.3 V		−0.18	mA
I_{OS}	Short-circuit output current§	4	V_{CC} = MAX	−3	−15	mA
I_{CC}	Supply current	5	V_{CC} = MAX, V_I = 4.5 V		7.7	mA
			V_{CC} = MAX, V_I = 0		7.2	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

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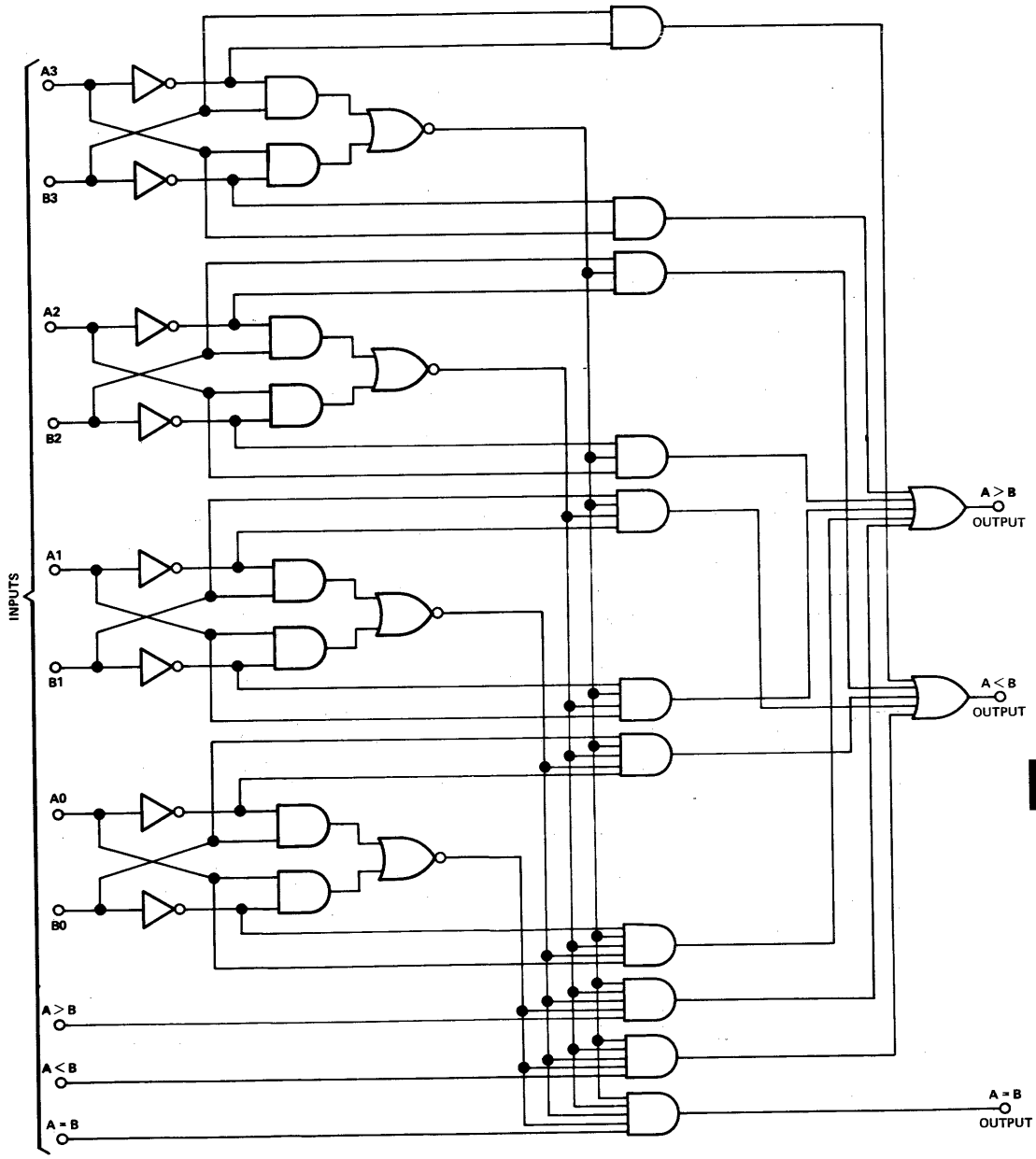
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output, from any A or B input	6	C_L = 50 pF, R_L = 4 kΩ		90	150	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from any A or B input	6			75	150	ns
t_{PLH}	Propagation delay time, low-to-high-level output, from A > B, A < B, or A = B inputs	7			75	150	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from A > B, A < B, or A = B inputs	7			55	100	ns

functional block diagram



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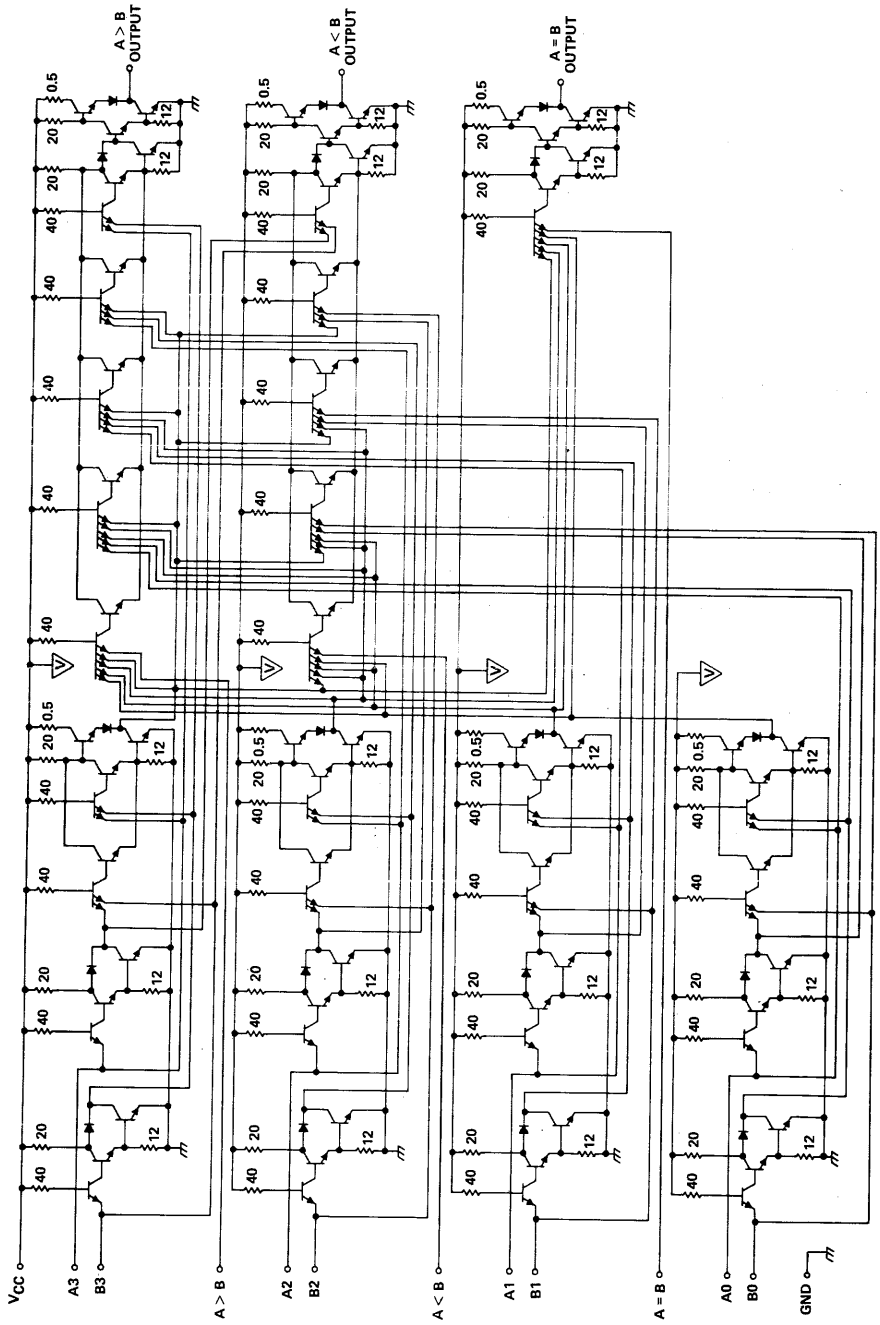
schematic



All resistor values shown are nominal and in kilohms.
▽ ... V_{CC} bus

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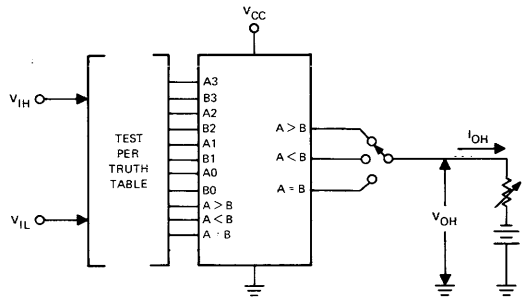
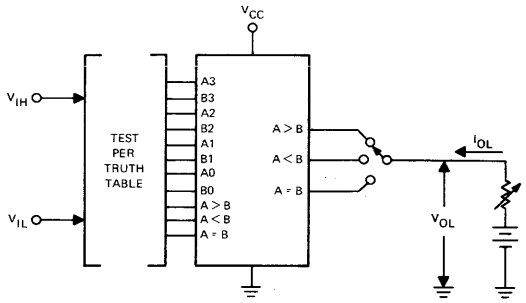
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§



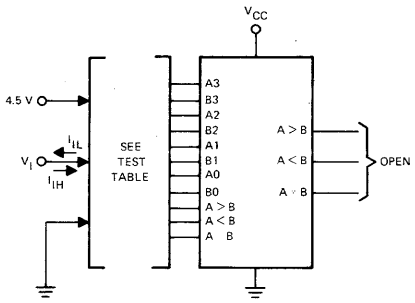
Each input is tested separately.

FIGURE 1–V_{IH}, V_{IL}, V_{OH}



Each input is tested separately.

FIGURE 2–V_{IH}, V_{IL}, V_{OL}

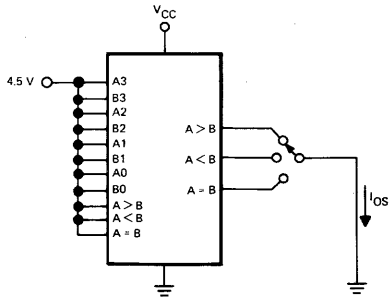


Each input is tested separately.

TEST TABLE

APPLY V_I	TEST I_{IH}		TEST I_{IL}	
	APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND
A3, A2, A1, A0	ALL OTHER INPUTS	NONE	NONE	ALL OTHER INPUTS
B3, B2, B1, B0	ALL OTHER INPUTS	NONE	NONE	ALL OTHER INPUTS
A > B	A3, A2, A1, AND A0	B3, B2, B1, AND B0	ALL OTHER INPUTS	NONE
A < B			ALL OTHER INPUTS	NONE
A = B			ALL OTHER INPUTS	NONE

FIGURE 3–I_{IH}, I_{IL}



Each output is tested separately.

FIGURE 4–I_{OS}

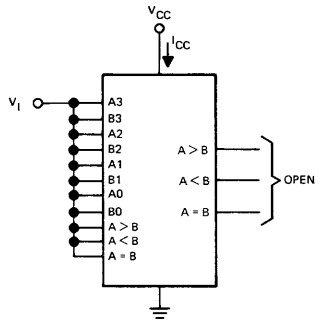


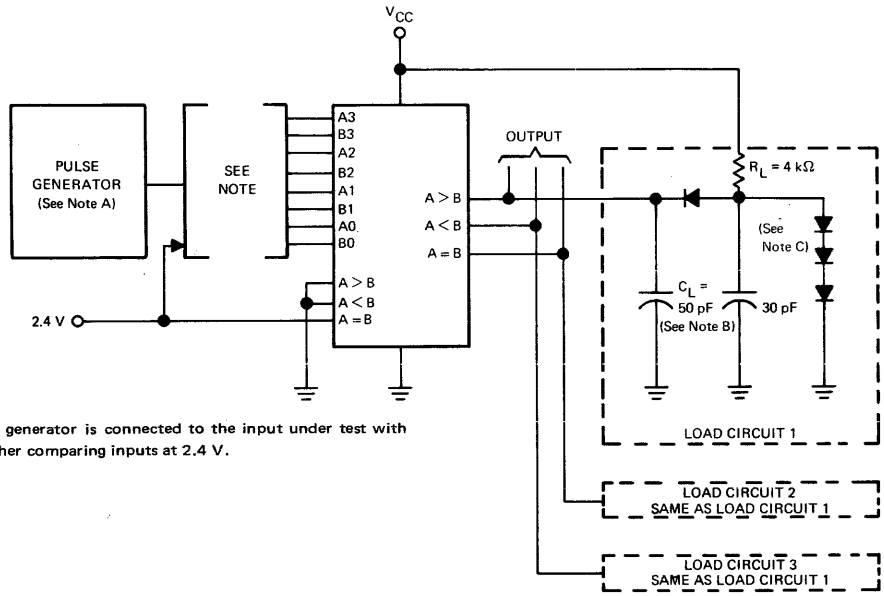
FIGURE 5–I_{CC}

§ Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

9

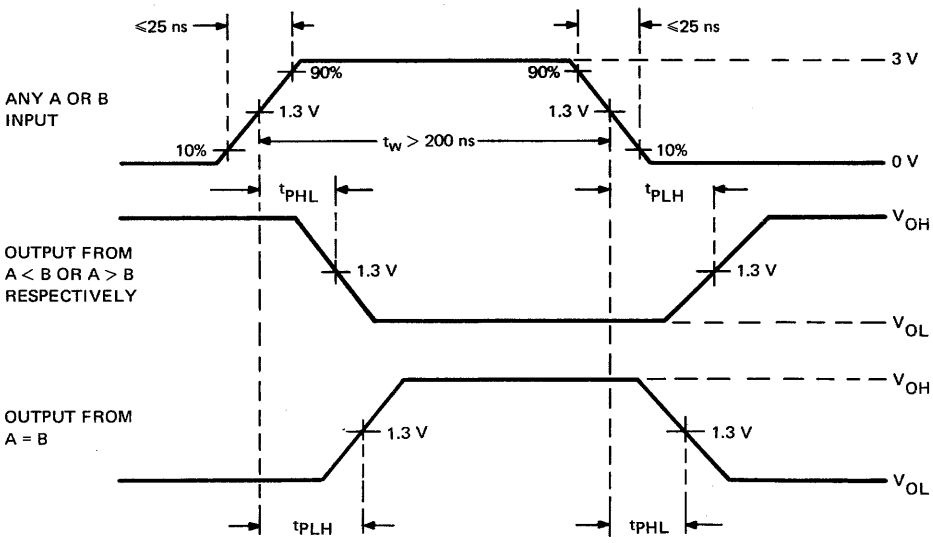
PARAMETER MEASUREMENT INFORMATION

switching characteristics



NOTE: Pulse generator is connected to the input under test with all other comparing inputs at 2.4 V.

TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR ≤ 500 kHz, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916.
D. Each output is tested separately.

FIGURE 6–PROPAGATION TIMES FROM COMPARING INPUTS

9

TEXAS INSTRUMENTS
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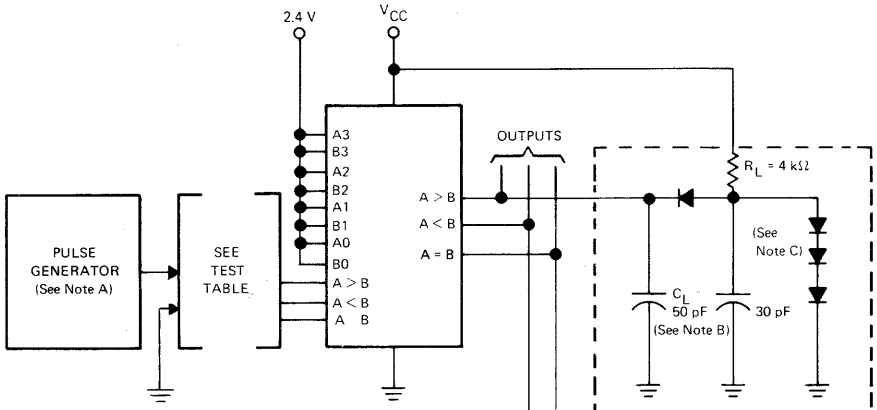
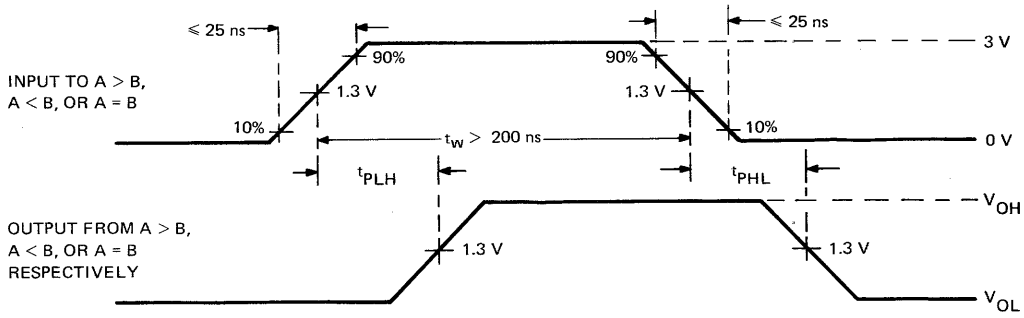
PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT

APPLY PULSE GENERATOR TO	GROUND	TEST
A > B INPUT	UNUSED INPUTS	A > B OUTPUT
A < B INPUT	UNUSED INPUTS	A < B OUTPUT
A = B INPUT	UNUSED INPUTS	A = B OUTPUT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR ⩽ 500 kHz, Z_{out} ≈ 50 Ω.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916.
D. Each output is tested separately.

FIGURE 7–PROPAGATION TIMES FROM CASCADING INPUTS

9

CIRCUIT TYPES SN5486, SN7486
QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

- Input-Clamping Diodes Simplify System Design
- Fully Compatible with TTL, DTL, and Other MSI Circuits
- Typical Propagation Delay Times: 12 ns

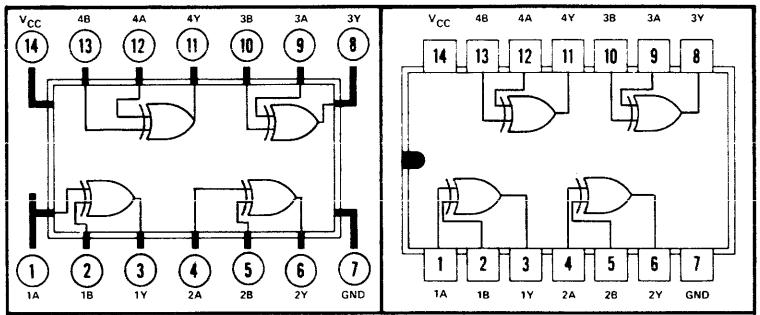
logic

TRUTH TABLE

INPUTS		OUTPUT
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

W
FLAT PACKAGE (TOP VIEW)

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = A \oplus B$

description

Each of these monolithic, quadruple 2-input exclusive-OR gates utilize TTL circuitry to perform the function: $Y = A\overline{B} + \overline{A}B$. When the input states are complementary, the output goes to a logical 1.

9

These circuits are fully compatible for use with other TTL or DTL circuits. Input clamping diodes are provided to minimize transmission line effects and thereby simplify system design. Input buffers are used to lower the fan-in requirement to only one normalized series 54/74 load. A full fan-out to 10 normalized series 54/74 loads is available from each of the outputs in the logical 0 state. A fan-out of 20 is provided in the logical 1 state to facilitate connection of unused inputs to used inputs. Propagation delay is 12 nanoseconds and power dissipation is 37.5 miiliwatts typically for each exclusive-OR function.

The SN5486 is characterized for operation over the full military temperature range of −55°C to 125°C and the SN7486 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1)		7 V
Input Voltage, V_{in} (See Note 1)		5.5 V
Operating Free-Air Temperature Range:	SN5486 Circuits	−55°C to 125°C
	SN7486 Circuits	0°C to 70°C
Storage Temperature Range		−65°C to 150°C

NOTE 1: These voltage values are with respect to network ground terminal.

TEXAS INSTRUMENTS
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recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1): SN5486 Circuits	4.5	5	5.5	V
SN7486 Circuits	4.75	5	5.25	V
Normalized Fan-out from each output,N: Logical 0			10	
Logical 1			20	

electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS †		MIN	TYP ‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	1					0.8	V
$V_{out(1)}$	Logical 1 output voltage	1	V_{CC} = MIN, $V_{in(1)}$ = 2 V, $V_{in(0)}$ = 0.8 V, I_{load} = −800 μA		2.4			V
$V_{out(0)}$	Logical 0 output voltage	2	V_{CC} = MIN, $V_{in(1)}$ = 2 V, $V_{in(0)}$ = 0.8 V, I_{sink} = 16 mA				0.4	V
$I_{in(1)}$	Logical 1 level input current (each input)	3	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(0)}$	Logical 0 level input current (each input)	4	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
I_{OS}	Short circuit output current §	5	V_{CC} = MAX, $V_{in(1)}$ = 4.5 V, $V_{in(0)}$ = 0	SN5486	−20		−55	mA
				SN7486	−18		−55	mA
I_{CC}	Supply current	6	V_{CC} = MAX, V_{in} = 4.5 V	SN5486		30	43	mA
				SN7486		30	50	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

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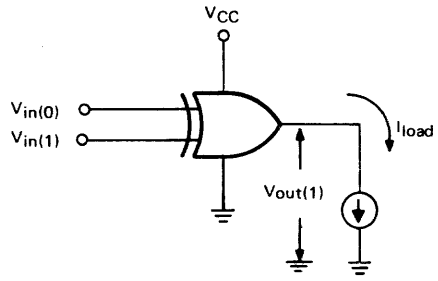
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level (other input low)	7	C_L = 15 pF, R_L = 400 Ω		11	17	ns
t_{pd1}	Propagation delay time to logical 1 level (other input low)	7	C_L = 15 pF, R_L = 400 Ω		15	23	ns
t_{pd0}	Propagation delay time to logical 0 level (other input high)	7	C_L = 15 pF, R_L = 400 Ω		13	22	ns
t_{pd1}	Propagation delay time to logical 1 level (other input high)	7	C_L = 15 pF, R_L = 400 Ω		18	30	ns

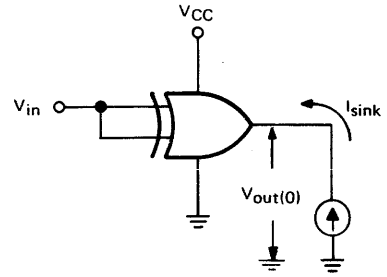
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



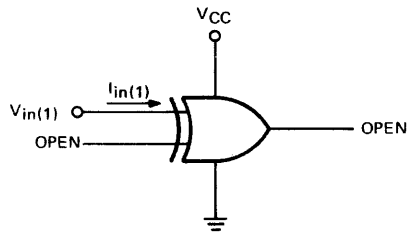
1. Each input is tested separately.

FIGURE 1



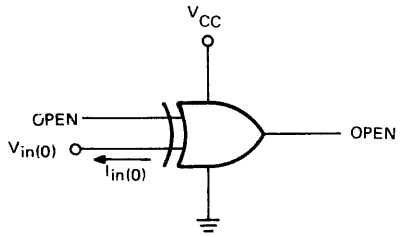
1. Logical 0 and logical 1 input conditions are tested.

FIGURE 2



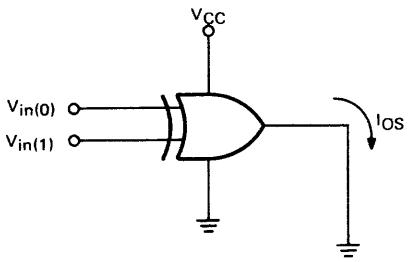
1. Each input is tested separately.

FIGURE 3



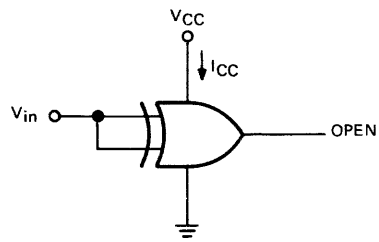
1. Each input is tested separately.

FIGURE 4



1. Each gate is tested separately.

FIGURE 5



1. Logical 0 and logical 1 input conditions are tested.

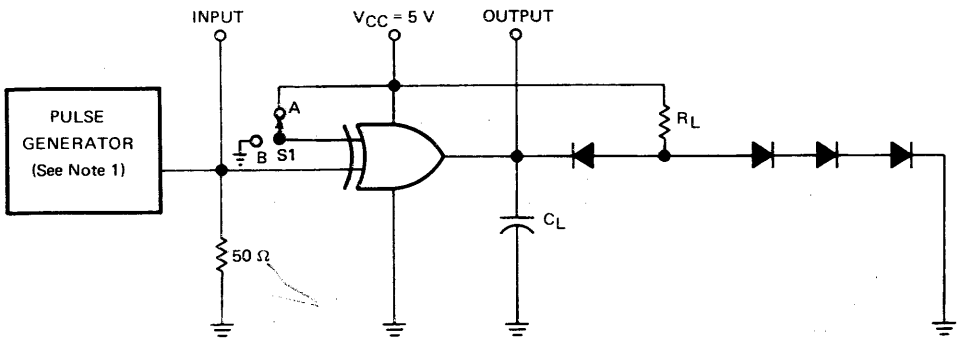
FIGURE 6

† Arrows indicate actual direction of current flow.

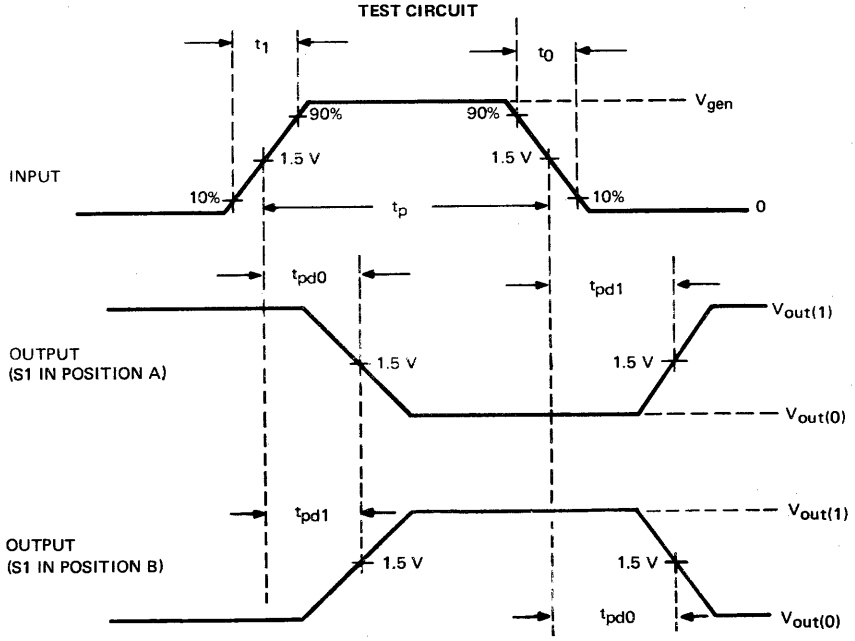
9

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: 1. The generator has the following characteristics: V_{gen} = 3 V, $t_0 = t_1 \leqslant 15$ ns, t_p = 0.5 μs, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
2. All diodes are 1N3064
3. $t_{pd} = \dfrac{t_{pd0} + t_{pd1}}{2}$
4. C_L includes probe and jig capacitance.
5. Each gate tested separately.

FIGURE 7

9

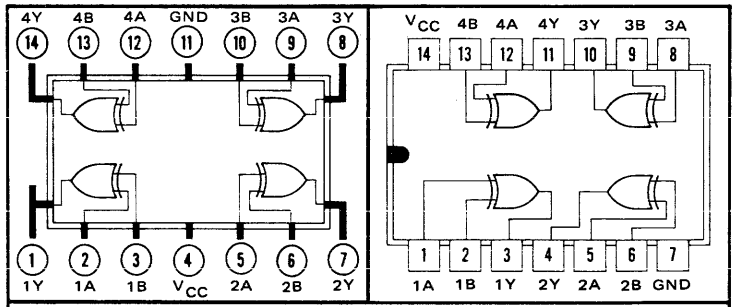
CIRCUIT TYPES SN54L86, SN74L86
QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

- Fully Compatible with TTL, DTL, and Other MSI Circuits
- Typical Propagation Delay Time: 43 ns

logic

T
FLAT PACKAGE (TOP VIEW)

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW



positive logic: $Y = A \oplus B$

TRUTH TABLE

INPUTS		OUTPUT
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

description

Each of these low-power, monolithic, quadruple 2-input exclusive–OR gates utilize TTL circuitry to perform the function: $Y = A\overline{B} + \overline{A}B$. When the input states are complementary the output goes to a logical 1.

These circuits are fully compatible for use with other TTL or DTL circuits. A full fan-out to 10 series 54L/74L loads is available from each of the outputs. Typical power dissipation is 3.75 milliwatts for each exclusive-OR function.

The SN54L86 is characterized for operation over the full military temperature range of –55°C to 125°C and the SN74L86 is characterized for operation from 0°C to 70°C.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1) . . . . . 8 V
Input Voltage, V_{in} (See Note 1) . . . . . 5.5 V
Operating Free-Air Temperature Range: SN54L86 Circuits . . . . . –55°C to 125°C
SN74L86 Circuits . . . . . 0°C to 70°C
Storage Temperature Range . . . . . –65°C to 150°C

NOTE 1: These voltage values are with respect to network ground terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1): SN54L86	4.5	5	5.5	V
SN74L86	4.75	5	5.25	V
Normalized Fan-out from each output, N			10	

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electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	1				0.7	V
$V_{out(1)}$	Logical 1 output voltage	1	V_{CC} = MIN, $V_{in(1)}$ = 2 V, $V_{in(0)}$ = 0.7 V, I_{load} = −100 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	2	V_{CC} = MIN, $V_{in(1)}$ = 2 V, $V_{in(0)}$ = 0.7 V, I_{sink} = 2 mA			0.3	V
$I_{in(1)}$	Logical 1 level input current (each input)	3	V_{CC} = MAX, V_{in} = 2.4 V			20	μA
			V_{CC} = MAX, V_{in} = 5.5 V			200	μA
$I_{in(0)}$	Logical 0 level input current (each input)	4	V_{CC} = MAX, V_{in} = 0.3 V			−0.36	mA
I_{OS}	Short circuit output current	5	V_{CC} = MAX, $V_{in(1)}$ = 4.5 V, $V_{in(0)}$ = 0	−3		−15	mA
$I_{CC(0)}$	Supply current (average per gate)	6	V_{CC} = MAX, V_{in} = 4.5 V			1.67	mA
$I_{CC(1)}$	Supply current (average per gate)	5	V_{CC} = MAX $V_{in(1)}$ = 4.5 V, $V_{in(0)}$ = 0			1.1	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

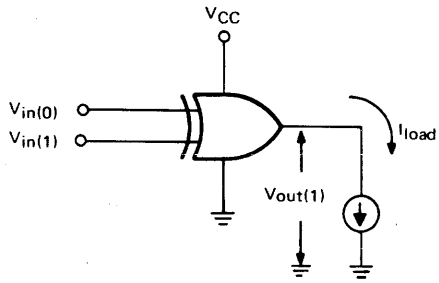
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

9

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level (other input low)	7	C_L = 50 pF, R_L = 4 kΩ		60	150	ns
t_{pd1}	Propagation delay time to logical 1 level (other input low)	7	C_L = 50 pF, R_L = 4 kΩ		75	150	ns
t_{pd0}	Propagation delay time to logical 0 level (other input high)	7	C_L = 50 pF, R_L = 4 kΩ		35	60	ns
t_{pd1}	Propagation delay time to logical 1 level (other input high)	7	C_L = 50 pF, R_L = 4 kΩ		50	90	ns

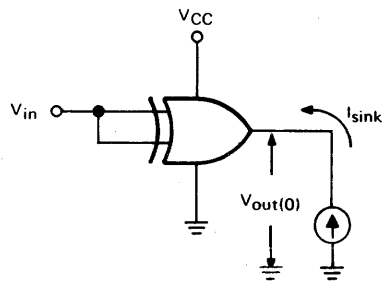
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



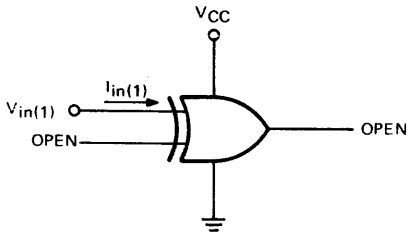
1. Each input is tested separately.

FIGURE 1



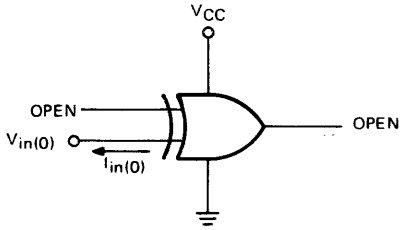
1. Logical 0 and logical 1 input conditions are tested.

FIGURE 2



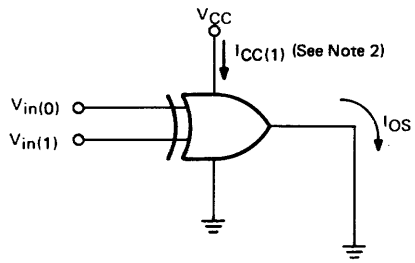
1. Each input is tested separately.

FIGURE 3



1. Each input is tested separately.

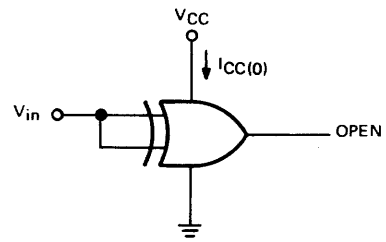
FIGURE 4



NOTES: 1. Each gate is tested separately for I_{OS}.
2. When testing $I_{CC(1)}$, the output is open,

the average-per-gate value = $\frac{I_{CC\ total}}{\text{number of gates in package}}$

FIGURE 5



NOTES: 1. Logical 0 and logical 1 input conditions are tested.

2. The average-per gate value = $\frac{I_{CC\ total}}{\text{number of gates in package}}$

FIGURE 6

†Arrows indicate actual direction of current flow.

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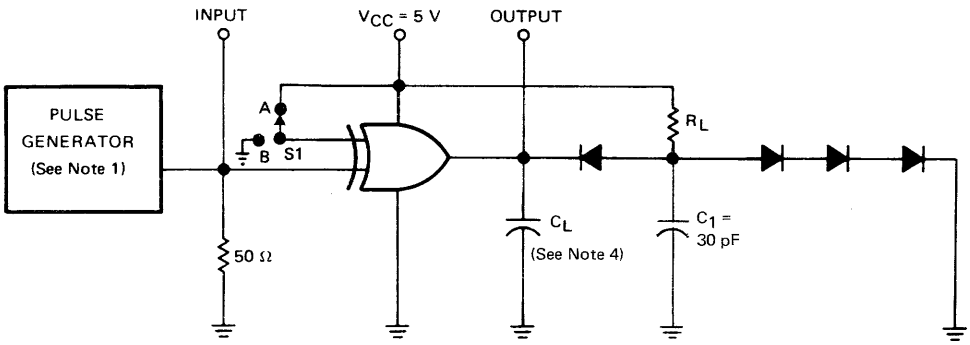
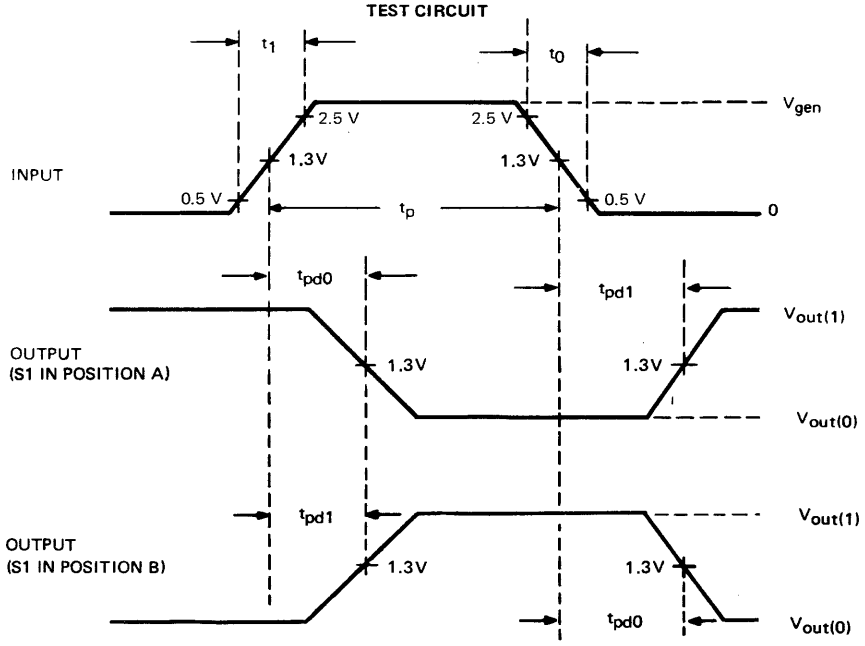
PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: 1. The generator has the following characteristics: V_{gen} = 3 V, $t_0 = t_1 \leq 60$ ns, t_p = 1 μs, PRR ≤ 500 kHz, $Z_{out} \approx 50\ \Omega$.
2. All diodes are 1N916.
3. $t_{pd} = \frac{t_{pd0} + t_{pd1}}{2}$
4. C_L includes probe and jig capacitance.
5. Each gate tested separately.

FIGURE 7

9

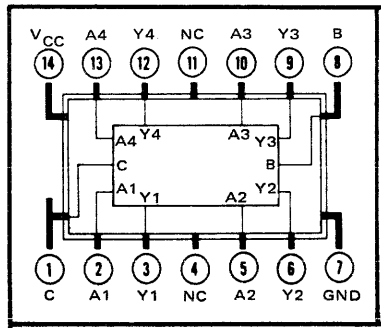
CIRCUIT TYPES SN54H87, SN74H87
4-BIT TRUE/COMPLEMENT, ZERO/ONE ELEMENT

logic

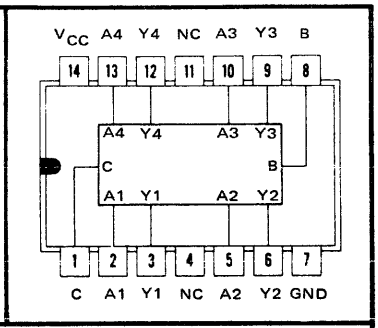
TRUTH TABLE

CONTROL INPUTS		OUTPUTS			
B	C	Y1	Y2	Y3	Y4
0	0	$\overline{A1}$	$\overline{A2}$	$\overline{A3}$	$\overline{A4}$
0	1	A1	A2	A3	A4
1	0	1	1	1	1
1	1	0	0	0	0

W
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: See truth table

description

These monolithic 4-bit true/complement elements, with the use of the two control lines (B, C), will transfer a 4-bit binary input (A) to the output (Y) in either true or complementary form. Furthermore, the control lines will also set all outputs to either a logical 0 or logical 1 independent of the state of the data inputs.

These circuits are fully compatible for use with other TTL or DTL circuits. Input clamping diodes are provided to minimize transmission line effects and thereby simplify system design. Each input represents only one normalized series 54H/74H load, and full fan-out to 10 series 54H/74H loads is available from each of the outputs in the logical 0 condition. In the logical 1 state, a fan-out of 20 is available to facilitate tying unused inputs to used inputs.

9

Power dissipation is 270 mW typically with an average propagation delay of 14 ns from data inputs to output.

The SN54H87 is characterized for operation over the full military temperature range of −55°C to 125°C, and the SN74H87 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1)		7 V
Input Voltage, V_{in} (See Note 1)		5.5 V
Operating Free-Air Temperature Range:	SN54H87 Circuits	−55°C to 125°C
	SN74H87 Circuits	0°C to 70°C
Storage Temperature Range		−65°C to 150°C

Note 1: These voltage values are with respect to network ground terminal.

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recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1): SN54H87 Circuits	4.5	5	5.5	V
SN74H87 Circuits	4.75	5	5.25	V
Normalized Fan-Out from Each Output (N): Logical 0			10	
Logical 1			20	

NOTE 1: These voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	1				0.8	V
$V_{out(1)}$	Logical 1 output voltage	1	V_{CC} = MIN, $V_{in(1)}$ = 2 V, $V_{in(0)}$ = 0.8 V, I_{load} = −1 mA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, $V_{in(1)}$ = 2 V, $V_{in(0)}$ = 0.8 V, I_{sink} = 20 mA			0.4	V
$I_{in(1)}$	Logical 1 level input current (each input)	2	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.4 V			−2	mA
I_{OS}	Short circuit output current§	4	V_{CC} = MAX, V_{out} = 0	−40		−100	mA
I_{CC}	Supply current (SN54H87)	5	V_{CC} = MAX		54	78	mA
I_{CC}	Supply current (SN74H87)	5	V_{CC} = MAX		54	89	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level from data inputs to outputs	6	C_L = 25 pF, R_L = 280 Ω		13	19	ns
t_{pd1}	Propagation delay time to logical 1 level from data inputs to outputs	6	C_L = 25 pF, R_L = 280 Ω		14	20	ns
t_{pd0}	Propagation delay time to logical 0 level from control inputs to outputs	6	C_L = 25 pF, R_L = 280 Ω		17	25	ns
t_{pd1}	Propagation delay time to logical 1 level from control inputs to outputs	6	C_L = 25 pF, R_L = 280 Ω		17	25	ns

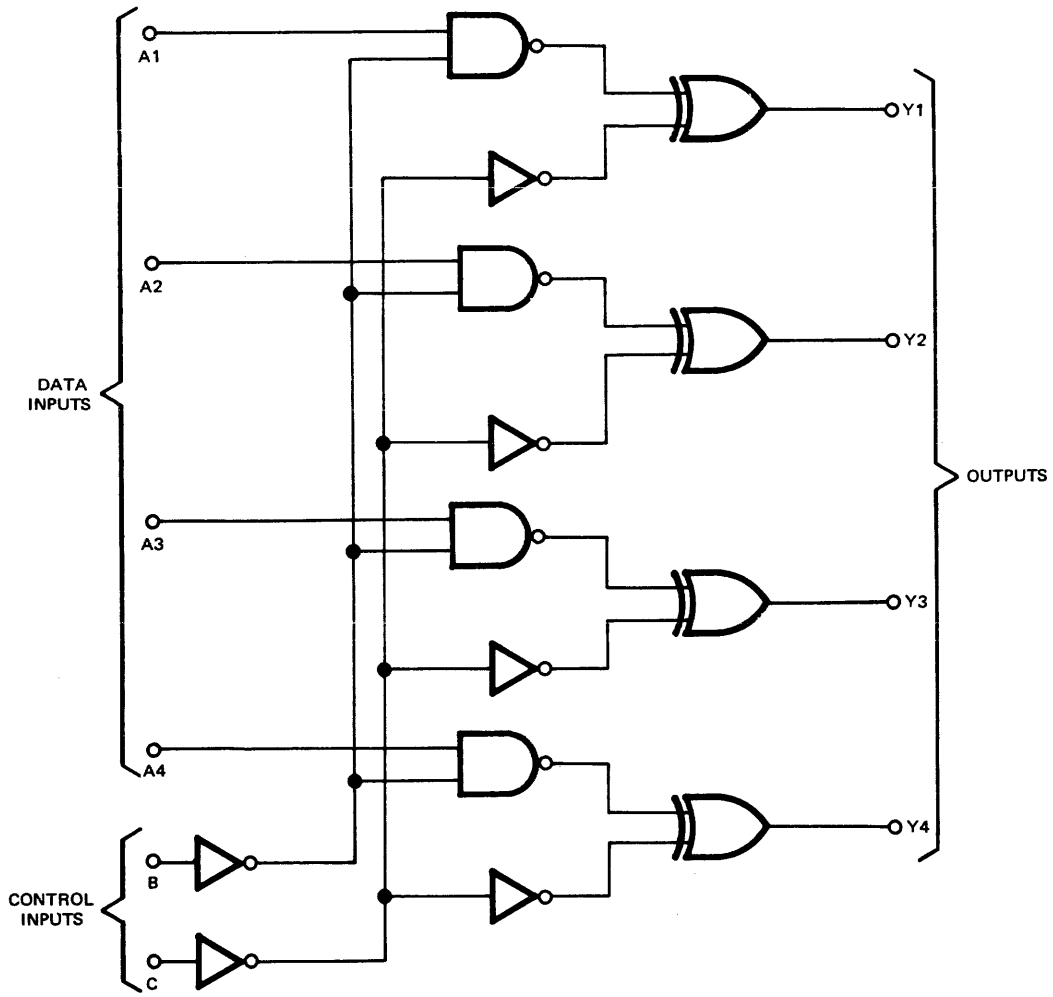
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C

§ Not more than one output should be shorted at a time.

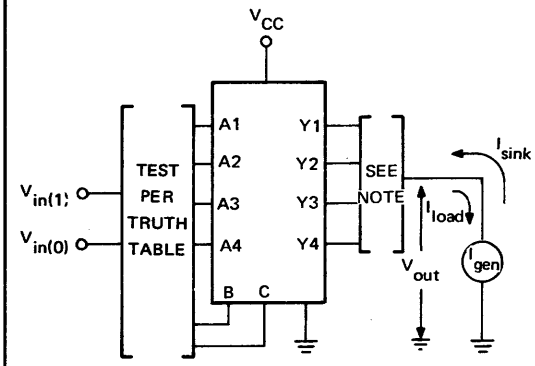
9

functional block diagram



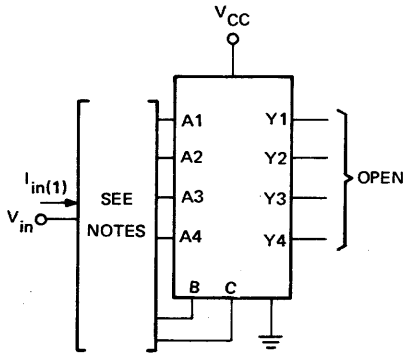
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



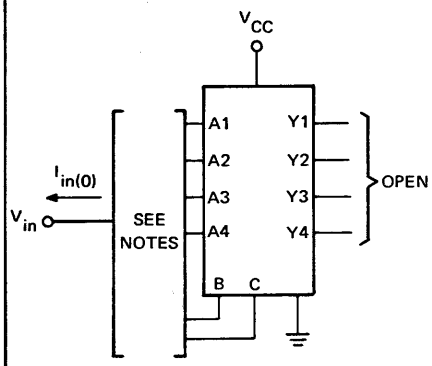
1. Each output is tested separately.

FIGURE 1



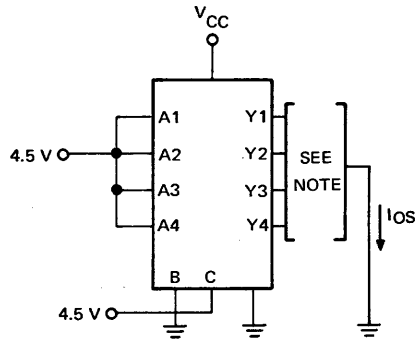
1. Each input is tested separately.
2. When testing A1, A2, A3, or A4 input B is at 4.5 V.

FIGURE 2



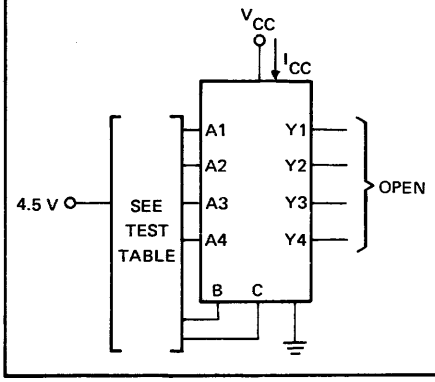
1. Each input is tested separately
2. When testing A1, A2, A3, or A4 input B is grounded.

FIGURE 3



1. Each output is tested separately.

FIGURE 4



TEST TABLE

TEST NO.	APPLY 4.5 V	GROUND
1	A1, A2, A3, A4	B, C
2	B, C	A1, A2, A3, A4

FIGURE 5

† Arrows indicate actual direction of current flow.

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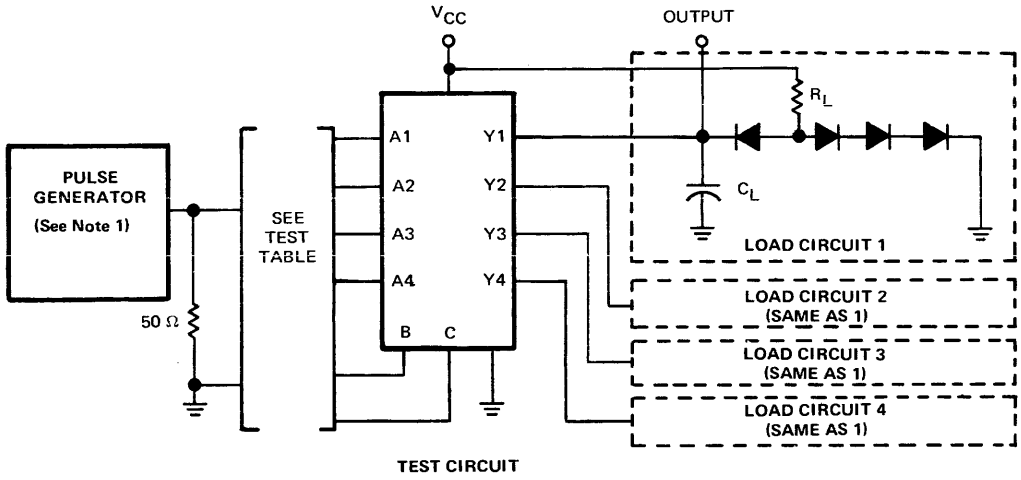
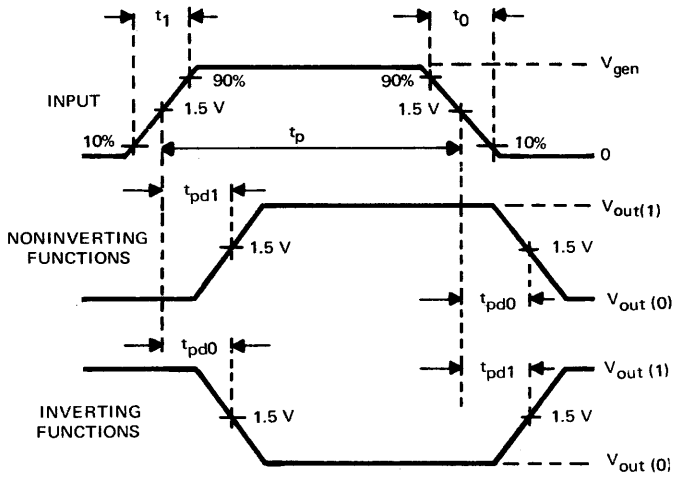
PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

TEST TABLE (See Note 2)

GND	INPUT	OUTPUT
B, C	A1	Y1
B, C	A2	Y2
B, C	A3	Y3
B, C	A4	Y4
C	B	Y1
C	B	Y2
C	B	Y3
C	B	Y4
B	C	Y1
B	C	Y2
B	C	Y3
B	C	Y4

NOTES: 1. The pulse generator has the following characteristics: V_{gen} = 3 V, $t_1 = t_0$ = 7 ns, t_p = 500 ns, PRR = 1 MHz, and $Z_{out} \approx 50\Omega$.
2. Inputs not specified are open.
3. C_L includes probe and jig capacitance.
4. All diodes are 1N3064.

FIGURE 6 – SWITCHING TIMES

TEXAS INSTRUMENTS
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CIRCUIT TYPES SN54180, SN74180
8-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

logic

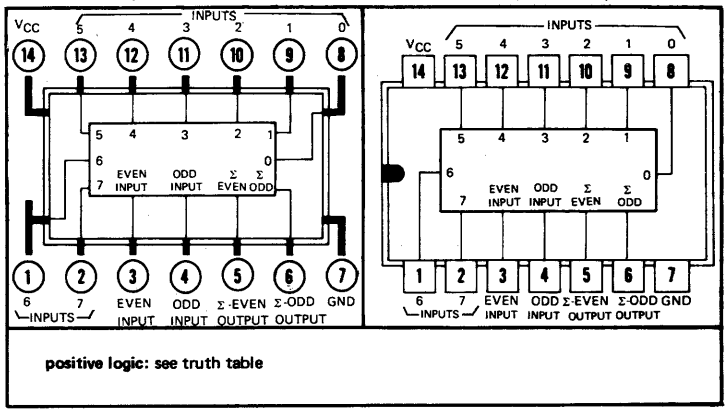
TRUTH TABLE

INPUTS			OUTPUTS	
Σ OF 1's AT 0 THRU 7	EVEN	ODD	Σ EVEN	Σ ODD
EVEN	1	0	1	0
ODD	1	0	0	1
EVEN	0	1	0	1
ODD	0	1	1	0
X	1	1	0	0
X	0	0	1	1

X= irrelevant

W FLAT PACKAGE
(TOP VIEW)

J OR N DUAL-IN-LINE PACKAGES
(TOP VIEW)



positive logic: see truth table

description

These universal, monolithic, 8-bit parity generators/checkers, utilizing familiar Series 54/74 TTL circuitry, feature odd/even outputs and control inputs to facilitate operation in either odd- or even-parity applications. The word-length capability is easily expanded by cascading. Typical applications are shown for these parity circuits being used to generate and check parity.

The SN54180/74180 are fully compatible with other TTL or DTL circuits. Input buffers are provided so that each data input represents only one normalized series 54/74 load. A full fan-out to 10 normalized series 54/74 loads is available from each of the outputs in the logical 0 state. A fan-out to 20 normalized loads is provided in the logical 1 state to facilitate the connection of unused inputs to used inputs. Typical power dissipation is 170 mW.

The SN54180 is characterized for operation over the full military temperature range of −55°C to 125°C; and the SN74180 is characterized for operation from 0°C to 70°C.

9

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1) . . . . . 7 V
Input Voltage, V_{in} (See Note 1) . . . . . 5.5 V
Operating Free-Air Temperature Range: SN54180 Circuits . . . . . −55°C to 125°C
SN74180 Circuits . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

NOTE 1: These voltage values are with respect to network ground terminal.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1):	SN54180	4.5	5	5.5	V
	SN74180	4.75	5	5.25	V
Normalized Fan-Out from Each Output (N):	Logical 0			10	V
	Logical 1			20	V

electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	1					0.8	V
$V_{out(1)}$	Logical 1 output voltage	1	V_{CC} = MIN, $V_{in(1)}$ = 2 V, $V_{in(0)}$ = 0.8 V, I_{load} = −800 μA		2.4			V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, $V_{in(1)}$ = 2 V, $V_{in(0)}$ = 0.8 V, I_{sink} = 16 mA				0.4	V
$I_{in(1)}$	Logical 1 level input current at each data input	2	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(0)}$	Logical 0 level input current at each data input	2	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(1)}$	Logical 1 level input current at even or odd input	2	V_{CC} = MAX, V_{in} = 2.4 V				80	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(0)}$	Logical 0 level input current at even or odd input	2	V_{CC} = MAX, V_{in} = 0.4 V				−3.2	mA
I_{OS}	Short circuit output current§	3	V_{CC} = MAX	SN54180	−20		−55	mA
				SN74180	−18		−55	mA
I_{CC}	Supply current	3 and 4	V_{CC} = MAX	SN54180		34	49	mA
				SN74180		34	56	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the particular circuit type.

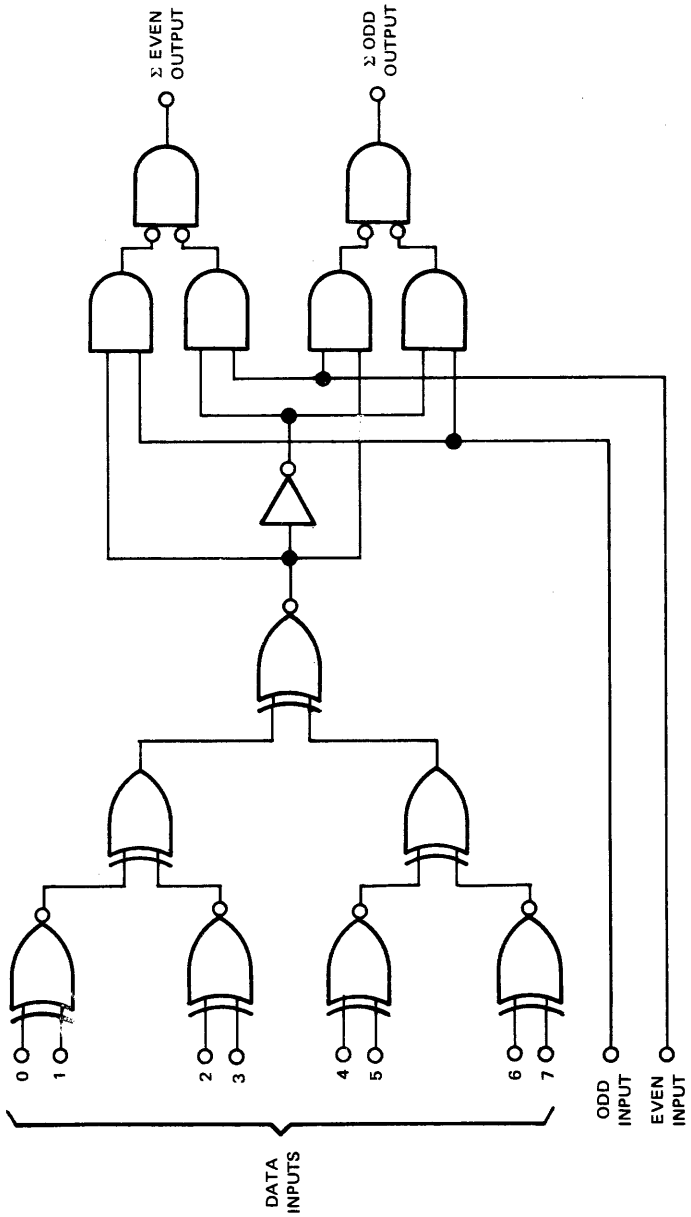
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER	FROM INPUT	TO OUTPUT	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd1}	Data	Σ Even	5	C_L = 15 pF, R_L = 400 Ω, Odd input grounded		40	60	ns
t_{pd0}						45	68	
t_{pd1}	Data	Σ Odd				32	48	ns
t_{pd0}						25	38	
t_{pd1}	Data	Σ Even	5	C_L = 15 pF, R_L = 400 Ω, Even input grounded		32	48	ns
t_{pd0}						25	38	
t_{pd1}	Data	Σ Odd				40	60	ns
t_{pd0}						45	68	
t_{pd1}	Even or Odd	Σ Even or Σ Odd	5	C_L = 15 pF, R_L = 400 Ω		13	20	ns
t_{pd0}	Even or Odd	Σ Even or Σ Odd				7	10	ns

functional block diagram



PARAMETER MEASUREMENT INFORMATION

d-c test circuits†

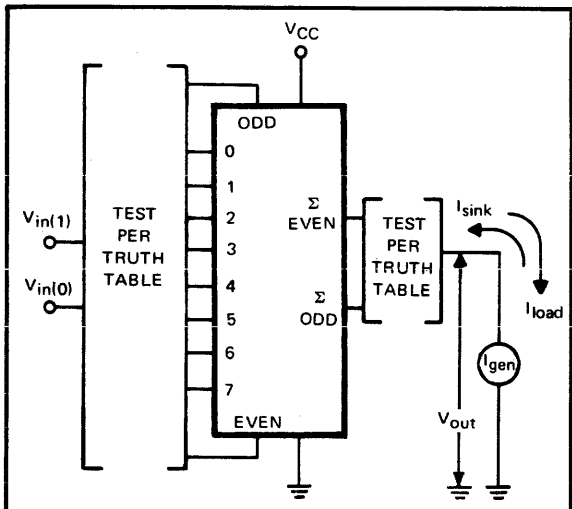
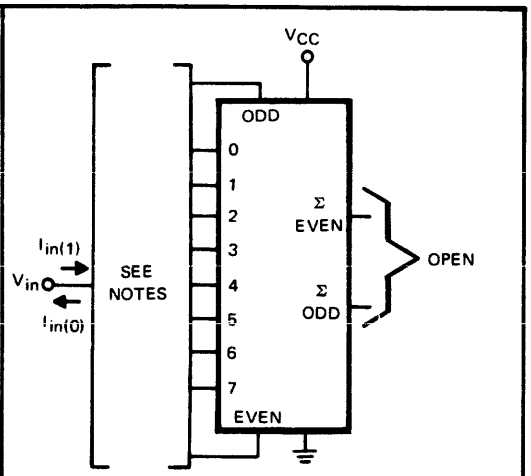
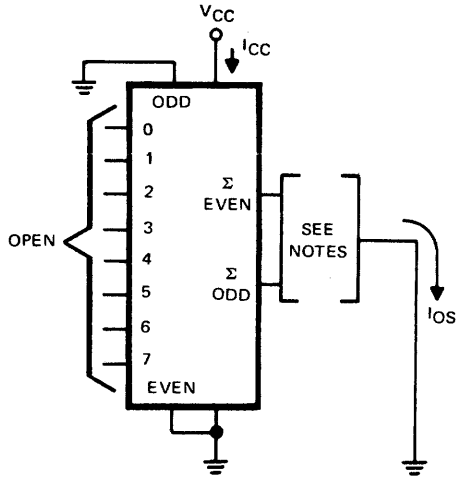


FIGURE 1



NOTES: 1. Each input is tested separately.
2. Odd and even inputs are each tested for $I_{in(1)}$ and $I_{in(0)}$ with both an even-code and an odd-code applied at the data inputs.

FIGURE 2



NOTES: 1. Each output is tested separately.
2. When testing I_{CC} both outputs are open.

FIGURE 3

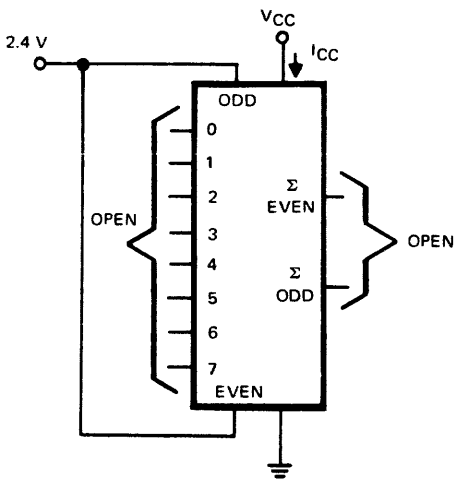


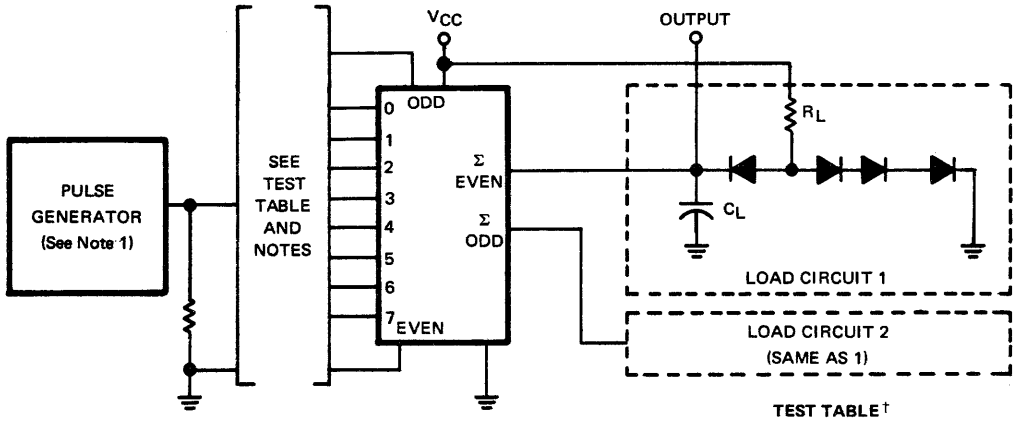
FIGURE 4

†Arrows indicate actual direction of current flow.

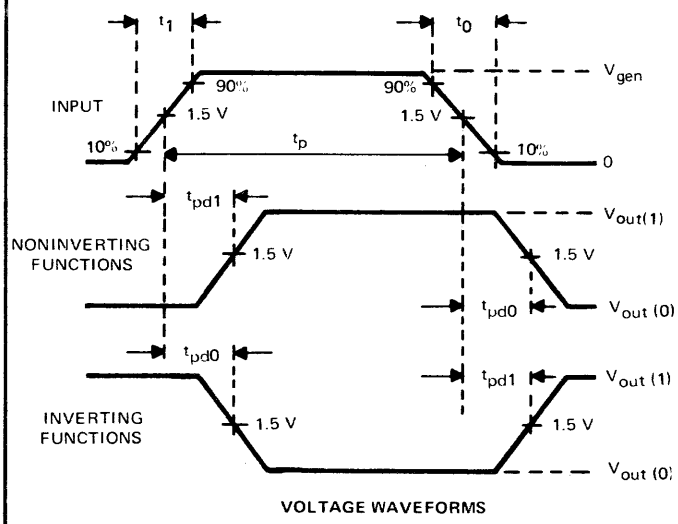
9

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

TEST TABLE†

INPUT CONDITIONS		OUTPUT
APPLY PULSE	GND	TESTED
0	ODD	Σ EVEN
1	ODD	Σ EVEN
2	ODD	Σ EVEN
3	ODD	Σ EVEN
4	ODD	Σ EVEN
5	ODD	Σ EVEN
6	ODD	Σ EVEN
7	ODD	Σ EVEN
0	ODD	Σ ODD
1	ODD	Σ ODD
2	ODD	Σ ODD
3	ODD	Σ ODD
4	ODD	Σ ODD
5	ODD	Σ ODD
6	ODD	Σ ODD
7	ODD	Σ ODD
EVEN	0	Σ EVEN
ODD	NONE	Σ EVEN
EVEN	NONE	Σ ODD
ODD	0	Σ ODD

†Repeat all but the last 4 tests with the even input grounded.

NOTES: 1. The pulse generator has the following characteristics: V_{gen} = 3 V, $t_1 = t_0$ = 10 ns, t_p = 500 ns, PRR = 1 MHz, and $Z_{out} \approx 50\ \Omega$.
2. Inputs not specified are open.
3. C_L includes probe and jig capacitance.
4. All diodes are 1N3064.

FIGURE 5 – SWITCHING TIMES

9

TYPICAL APPLICATIONS

verifying transmitted data

In this example (Figure A), data is being transmitted from data register A to data register B. Parity generators A1 and A2 are connected to generate an even-parity bit Q_{16} which is transmitted to register B. Parity checkers B1 and B2 verify the accuracy of the transmitted data and generate an even true (logical 1) or false (logical 0) parity output signal.

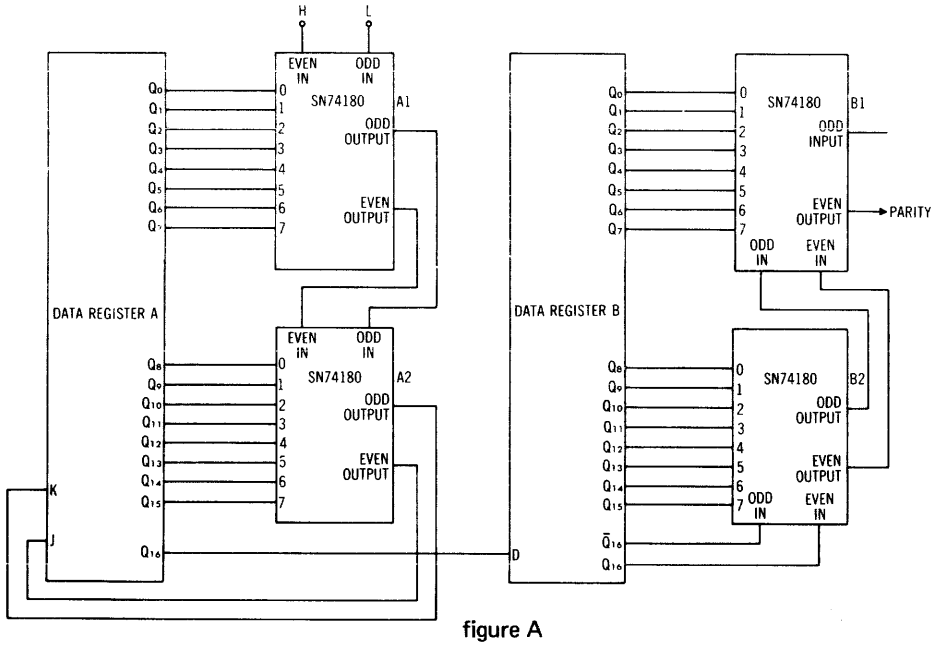


figure A

cascading for longer word lengths

The parity generator/checker may be cascaded for applications requiring longer word lengths. See Figure B. The ODD IN control is grounded for even parity generation and the EVEN IN control is grounded for odd parity generation. Two control inputs and two outputs ensure faster operation when cascading for word lengths over 8 bits, as only one gate delay is added for each additional 8-bit group. For a 32-bit word, parity can be generated in approximately 65 ns.

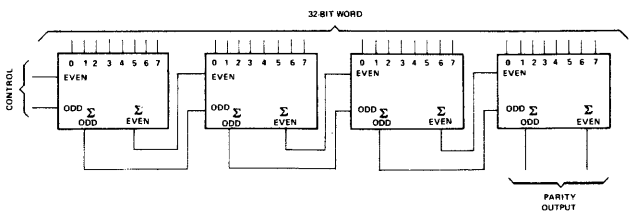


figure B

TEXAS INSTRUMENTS
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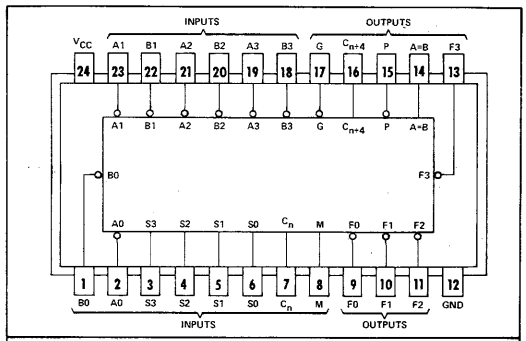
CIRCUIT TYPES SN54181, SN74181
ARITHMETIC LOGIC UNITS/ FUNCTION GENERATORS

PIN DESIGNATIONS

DESIGNATION	PIN NOS.	FUNCTION
A3, A2, A1, A0	19, 21, 23, 2	WORD A INPUTS
B3, B2, B1, B0	18, 20, 22, 1	WORD B INPUTS
S3, S2, S1, S0	3, 4, 5, 6	FUNCTION-SELECT INPUTS
C_n	7	INV. CARRY INPUT
M	8	MODE CONTROL INPUT
F3, F2, F1, F0	13, 11, 10, 9	FUNCTION OUTPUTS
A = B	14	COMPARATOR OUTPUT
P	15	CARRY PROPAGATE OUTPUT
C_{n+4}	16	INV. CARRY OUTPUT
G	17	CARRY GENERATE OUTPUT
V_{CC}	24	SUPPLY VOLTAGE
GND	12	GROUND

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



logic: see function tables

†Pin assignments for these circuits are the same for all packages.

- Full Look-Ahead for High-Speed Operations on Long Words
- Input Clamping Diodes Minimize Transmission-Line Effects
- Darlington Outputs Reduce Turn-Off Time
- Arithmetic Operating Modes:
  - Addition
  - Subtraction
  - Shift Operand A One Position
  - Magnitude Comparison
  - Plus Twelve Other Arithmetic Operations
- Logic Function Modes:
  - Exclusive-OR
  - Comparator
  - AND, NAND, OR, NOR
  - Plus Ten Other Logical Operations
- Typical Add Time for Four Bits . . . . 24 ns
- Typical Carry Time for Four Bits . . . . 12 ns

9

description

The SN54181 and SN74181 are high-speed arithmetic logic units (ALU)/function generators which have a complexity of 75 equivalent gates on a monolithic chip. This circuit performs 16 binary arithmetic operations on two 4-bit words as shown in the function table. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in the SN54/SN74181 for fast, simultaneous carry generation by means of two cascade-outputs (pin 15 and 17) for the four bits in the package. When used in conjunction with the SN54182 or SN74182 full carry look-ahead circuits, high-speed arithmetic operations can be performed. For example, the typical addition time for the SN54181/SN74181 is 24 nanoseconds for four bits. When expanding to 16-bit addition with the SN54182/SN74182, only 13 nanoseconds further delay is added so that the total addition time is 37 nanoseconds, or 2.2 nanoseconds per bit. One SN54182/SN74182 is needed for every 16 bit (four SN54181/SN74181 circuits).

If high speed is not of importance, a ripple-carry input (C_n) and a ripple-carry output (C_{n+4}) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be

description (continued)

performed without external circuitry. The typical delay for the ripple carry is 12 nanoseconds for four bits. With a typical addition time of 24 nanoseconds for four bits, addition of two 8-bit words is accomplished typically in 36 nanoseconds when employing the ripple carry.

The SN54181 and SN74181 will accommodate active-high or active-low data if the pin-designations are reinterpreted as follows:

PIN NUMBER	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-high data (Figure I)	A_0	B_0	A_1	B_1	A_2	B_2	A_3	B_3	F_0	F_1	F_2	F_3	$\overline{C_n}$	$\overline{C_{n+4}}$	X	Y
Active-low data (Figure II)	$\overline{A_0}$	$\overline{B_0}$	$\overline{A_1}$	$\overline{B_1}$	$\overline{A_2}$	$\overline{B_2}$	$\overline{A_3}$	$\overline{B_3}$	$\overline{F_0}$	$\overline{F_1}$	$\overline{F_2}$	$\overline{F_3}$	C_n	C_{n+4}	$\overline{P}$	$\overline{G}$

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A–B–1 which requires an end-around or forced carry to provide A–B.

The SN54181 or SN74181 can also be utilized as a comparator. The A = B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high-level state to indicate equality (A = B). The SN54181/SN74181 should be in the subtract mode when performing this comparison. The A = B output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subtract mode by placing the control lines at LHHL.

	Input C_n	Output C_{n+4}	Indicates
Active-High Data (Figure I)	H	H	A ≤ B
	L	H	A < B
	H	L	A > B
	L	L	A ≥ B
Active-Low Data (Figure II)	L	L	A ≤ B
	H	L	A < B
	L	H	A > B
	H	H	A ≥ B

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in the function table and include exclusive-OR, NAND, AND, NOR, and OR functions.

The SN54181/SN74181 is designed with a Darlington output configuration (54H/74H type) to reduce the high-logic-level output impedance and thereby improve the turn-off propagation delay time. All outputs are rated at a normalized fan-out of ten at the low logic level and increased to a fan-out of 20 at the high logic level. The increased high-logic-level fan-out allows the system designer more freedom in tying unused inputs to driven inputs.

The SN54181 is characterized for operation over the full military temperature range of –55°C to 125°C; the SN74181 is characterized for operation from 0°C to 70°C.

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description (continued)

ALU Signal Designations

The SN54181 and SN74181 can be used with either the signal designations as shown in Figures I or II.

The logic functions and arithmetic operations obtained with signal designations as in Figure I are given in Table I; those obtained with the signal designations of Figure II are given in Table II.

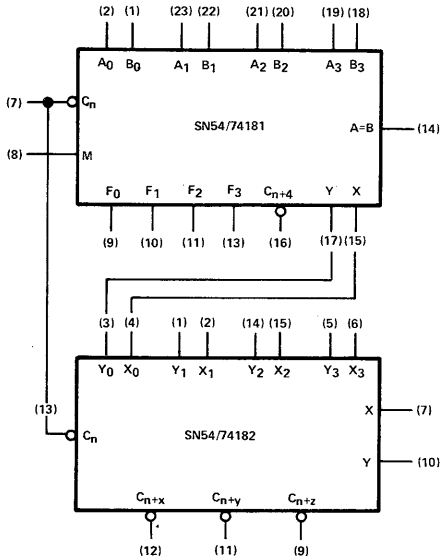

FIGURE I
(FOR TABLE I)

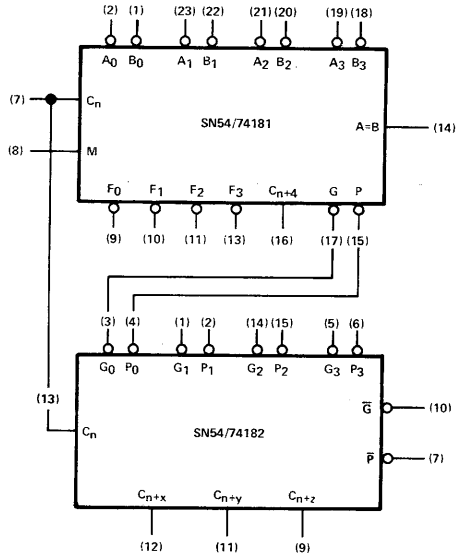

FIGURE II
(FOR TABLE II)

TABLE I

SELECTION S3 S2 S1 S0	ACTIVE-HIGH DATA: M = H LOGIC FUNCTIONS	M = L; ARITHMETIC OPERATIONS: Cn = 0, Cn = 1 = H	Cn = 1, Cn = 0 = L
L L L L	F = $\overline{A}$	F = A	F = A PLUS 1
L L L H	F = $\overline{A+B}$	F = A + B	F = (A + B) PLUS 1
L L H L	F = $\overline{A}B$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
L L H H	F = 0	F = MINUS 1 (2's COMPL)	F = ZERO
L H L L	F = $\overline{AB}$	F = A PLUS A$\overline{B}$	F = A PLUS A$\overline{B}$ PLUS 1
L H L H	F = $\overline{B}$	F = (A + B) PLUS A$\overline{B}$	F = (A + B) PLUS A$\overline{B}$ PLUS 1
L H H L	F = A ⊕ B	F = A MINUS B MINUS 1	F = A MINUS B
L H H H	F = A$\overline{B}$	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
H L L L	F = $\overline{A}$ + B	F = A PLUS AB	F = A PLUS AB PLUS 1
H L L H	F = $\overline{A \oplus B}$	F = A PLUS B	F = A PLUS B PLUS 1
H L H L	F = B	F = (A + $\overline{B}$) PLUS AB	F = (A + $\overline{B}$) PLUS AB PLUS 1
H L H H	F = AB	F = AB MINUS 1	F = AB
H H L L	F = 1	F = A PLUS A*	F = A PLUS A PLUS 1
H H L H	F = A + $\overline{B}$	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1
H H H L	F = A + B	F = (A + $\overline{B}$) PLUS A	F = (A + $\overline{B}$) PLUS A PLUS 1
H H H H	F = A	F = A MINUS 1	F = A

* Each bit is shifted to the next more significant position.

TABLE II

SELECTION S3 S2 S1 S0	ACTIVE-LOW DATA: M = H LOGIC FUNCTIONS	M = L; ARITHMETIC OPERATIONS: Cn = 0 = L	Cn = 1 = H
L L L L	F = $\overline{A}$	F = A MINUS 1	F = A
L L L H	F = $\overline{AB}$	F = AB MINUS 1	F = AB
L L H L	F = $\overline{A}$ + B	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
L L H H	F = 1	F = MINUS 1 (2's COMP)	F = ZERO
L H L L	F = $\overline{A+B}$	F = A PLUS (A + $\overline{B}$)	F = A PLUS (A + $\overline{B}$) PLUS 1
L H L H	F = $\overline{B}$	F = AB PLUS (A + $\overline{B}$)	F = AB PLUS (A + $\overline{B}$) PLUS 1
L H H L	F = $\overline{A \oplus B}$	F = A MINUS B MINUS 1	F = A MINUS B
L H H H	F = A + $\overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
H L L L	F = $\overline{A}$B	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1
H L L H	F = A ⊕ B	F = A PLUS B	F = A PLUS B PLUS 1
H L H L	F = B	F = A$\overline{B}$ PLUS (A + B)	F = A$\overline{B}$ PLUS (A + B) PLUS 1
H L H H	F = A + B	F = A + B	F = (A + B) PLUS 1
H H L L	F = 0	F = A PLUS A*	F = A PLUS A PLUS 1
H H L H	F = A$\overline{B}$	F = AB PLUS A	F = AB PLUS A PLUS 1
H H H L	F = AB	F = A$\overline{B}$ PLUS A	F = A$\overline{B}$ PLUS A PLUS 1
H H H H	F = A	F = A	F = A PLUS 1

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absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54181 Circuits . . . . . −55°C to 125°C
SN74181 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies to each A input in conjunction with inputs S2 or S3, and to each B input in conjunction with inputs S0 or S3.

recommended operating conditions

		SN54181			SN74181			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Operating temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage	1 and 2			2			V
V_{IL}	Low-level input voltage	1 and 2					0.8	V
V_{OH}	High-level output voltage, any output except A = B	1	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4			V
I_{OH}	High-level output current, A = B output only	1	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, V_{OH} = 5.5 V				250	μA
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA				0.4	V
I_{IH}	High-level input current (mode input)	3	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IH}	High-level input current (any A or B input)						120	μA
I_{IH}	High-level input current (any S input)						160	μA
I_{IH}	High-level input current (carry input)						200	μA
I_{IH}	High-level input current (any input)	3	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IL}	Low-level input current (mode input)	3	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
I_{IL}	Low-level input current (any A or B input)						−4.8	mA
I_{IL}	Low-level input current (any S input)						−6.4	mA
I_{IL}	Low-level input current (carry input)						−8	mA
I_{OS}	Short-circuit output current§	4	V_{CC} = MAX	SN54181	−20		−55	mA
				SN74181	−18		−57	
I_{CC}	Supply current	5	V_{CC} = MAX	SN54181		88	127	mA
				SN74181		88	140	
I_{CC}	Supply current	6	V_{CC} = MAX	SN54181		94	135	mA
				SN74181		94	150	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

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switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10 (C_L = 15 pF, R_L = 400 Ω)

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	C_n	C_{n+4}	7			12	18	ns
t_{PHL}						13	19	
t_{PLH}	C_n	Any F		M = 0 V (SUM or DIFF mode)		13	19	ns
t_{PHL}						12	18	
t_{PLH}	Any A or B	G		M = 0 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V (SUM mode)		13	19	ns
t_{PHL}						13	19	
t_{PLH}	Any A or B	G		M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V (DIFF mode)		17	25	ns
t_{PHL}						17	25	
t_{PLH}	Any A or B	P		M = 0 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V (SUM mode)		13	19	ns
t_{PHL}						17	25	
t_{PLH}	Any A or B	P		M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V (DIFF mode)		17	25	ns
t_{PHL}						17	25	
t_{PLH}	Any A or B	Any F		M = 0 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V (SUM mode)		28	42	ns
t_{PHL}						21	32	
t_{PLH}	Any A or B	Any F		M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V (DIFF mode)		32	48	ns
t_{PHL}						23	34	
t_{PLH}	Any A or B	Any F		M = 4.5 V (logic mode)		32	48	ns
t_{PHL}						23	34	
t_{PLH}	Any A or B	A = B		M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V (DIFF mode)		35	50	ns
t_{PHL}						32	48	

¶ t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output

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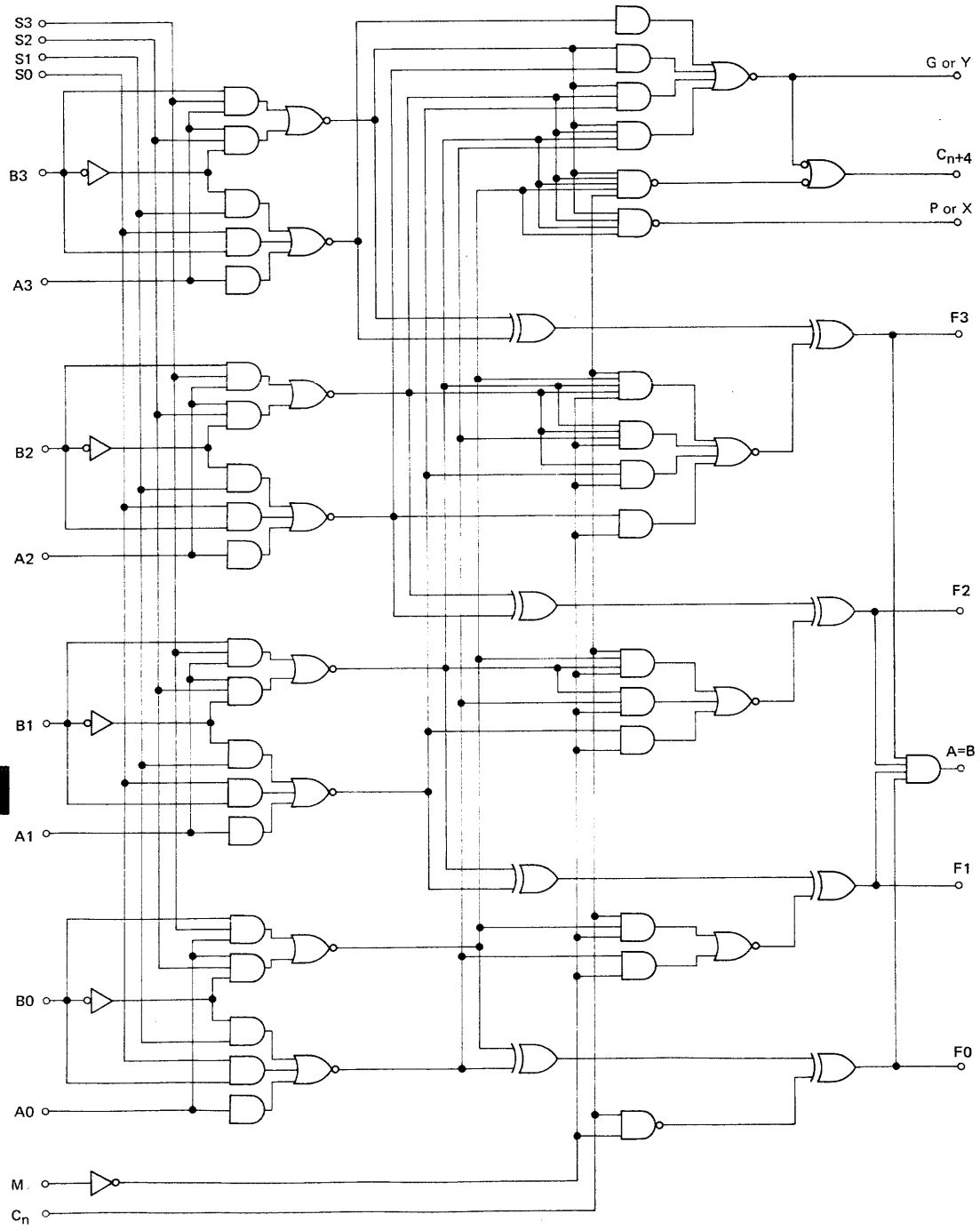
functional block diagram



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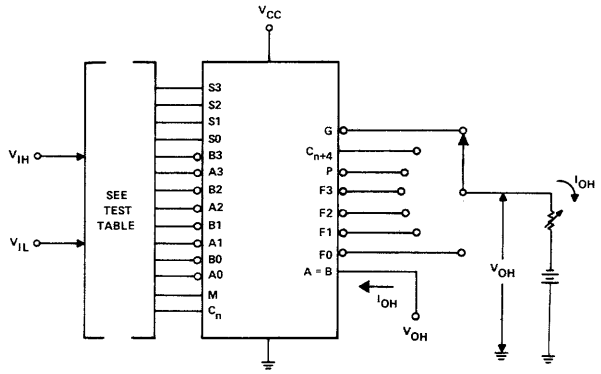
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



TEST TABLE

OUTPUT UNDER TEST	APPLY V_{IH}	APPLY V_{IL}
G	S3, B3, A3	S2, S1, S0, B2, A2, B1, A1, B0, A0
C_{n+4}	S3, S2, B3, B2, A2, B1, A1, B0, A0	S1, S0, A3, C_n
P	S3, S2, B3, A3, B2, A2, B1, A1, B0, A0	NONE
any F or A = B	S3, S2, S1, S0, A3, A2, A1, A0, M	NONE

Inputs not otherwise specified are connected to ground.

FIGURE 1–V_{IH}, V_{IL}, V_{OH}

TEST TABLE

OUTPUT UNDER TEST	APPLY V_{IH}	APPLY V_{IL}
G	S3, S2, S0, B2, A2, B1, A1, B0, A0	S1, B3, A3
C_{n+4}	S3, A3, A2, A1, B0, A0	S2, S1, S0, B3, B2, B1
P	S2, B3, A3, B2, A2, B1, A1, B0, A0	S3
any F	S3, S2, S1, S0, M, C_n	A3, A2, A1, A0
A = B	S3, S2, S1, S0, A3, A2, A1, M, C_n	A0

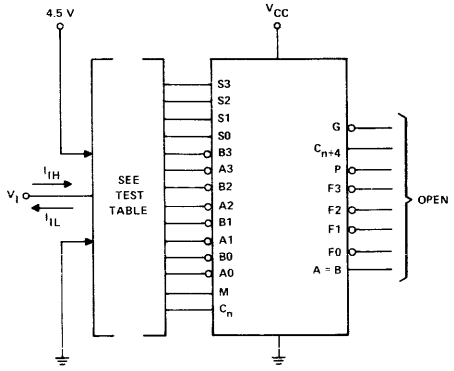
Inputs not otherwise specified are connected to ground.

FIGURE 2–V_{IH}, V_{IL}, V_{OL}

† Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

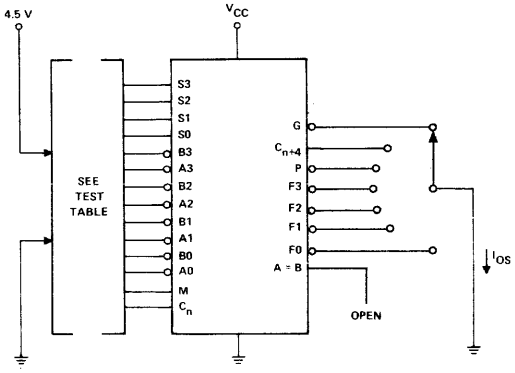


TEST TABLE

APPLY V_I MEASURE I_{IH} OR I_{IL}	CONDITIONS ON OTHER INPUTS FOR I_{IH}		CONDITIONS ON OTHER INPUTS FOR I_{IL}	
	APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND
S0, S3, any A, any B, or M	NONE	ALL OTHER INPUTS	ALL OTHER INPUTS	NONE
S1, S2	B0, B1, B2, B3	ALL OTHER INPUTS	A0, A1, A2, A3	ALL OTHER INPUTS
C_n	ALL OTHER INPUTS	NONE	NONE	ALL OTHER INPUTS

Each input is tested separately.

FIGURE 3–I_{IH}, I_{IL}



TEST TABLE

OUTPUT UNDER TEST	APPLY 4.5 V	APPLY GND
G	S3, A3, B3	ALL OTHER INPUTS
C_{n+4}	NONE	ALL OTHER INPUTS
P, F0, F1, F2, or F3	ALL OTHER INPUTS	NONE

FIGURE 4–I_{OS}

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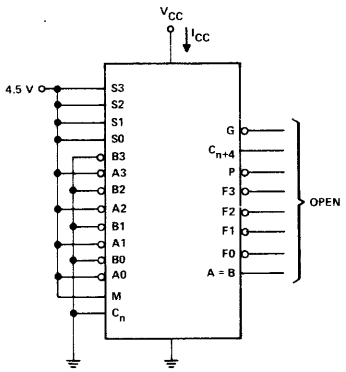

FIGURE 5–I_{CC}

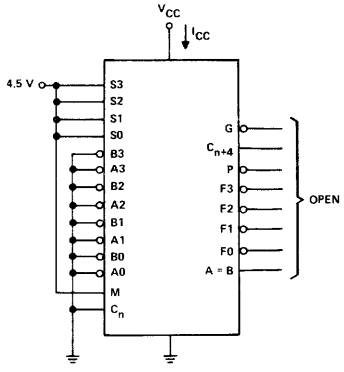

FIGURE 6–I_{CC}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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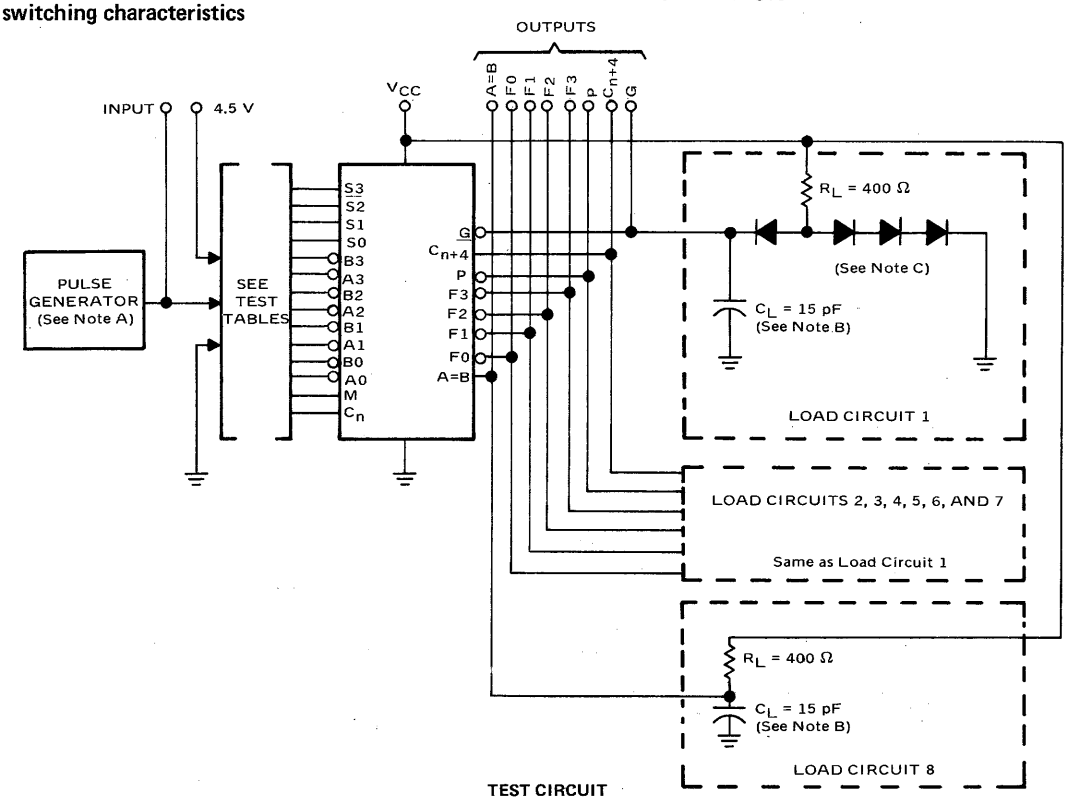
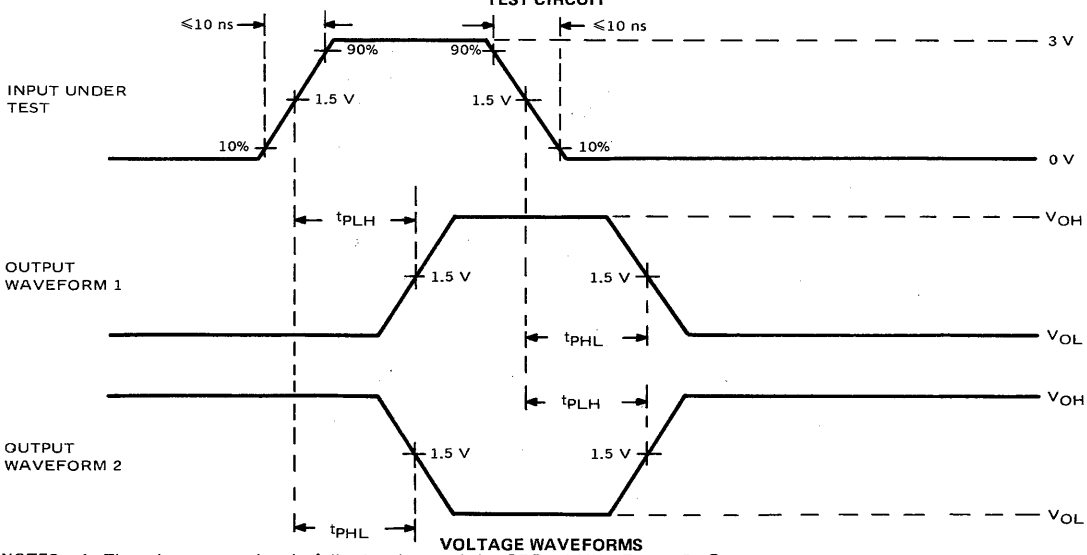
PARAMETER MEASUREMENT INFORMATION

switching characteristics





VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.

FIGURE 7–PROPAGATION DELAY TIMES

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PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)

$\overline{\text{SUM}}$ MODE TEST TABLE

FUNCTION INPUTS: S0 = S3 = 4.5 V, S1 = S2 = M = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} / t_{PHL}	A	B	None	Remaining A and B	C_n	Any F	1
t_{PLH} / t_{PHL}	B	A	None	Remaining A and B	C_n	Any F	1
t_{PLH} / t_{PHL}	A	B	None	None	Remaining A and B, C_n	P	1
t_{PLH} / t_{PHL}	B	A	None	None	Remaining A and B, C_n	P	1
t_{PLH} / t_{PHL}	A	None	B	Remaining B	Remaining A, C_n	G	1
t_{PLH} / t_{PHL}	B	None	A	Remaining B	Remaining A, C_n	G	1
t_{PLH} / t_{PHL}	C_n	None	None	All A	All B	Any F or C_{n+4}	1

$\overline{\text{DIFF}}$ MODE TEST TABLE

FUNCTION INPUTS: S1 = S2 = 4.5 V, S0 = S3 = M = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} / t_{PHL}	A	None	B	Remaining A	Remaining B, C_n	Any F	1
t_{PLH} / t_{PHL}	B	A	None	Remaining A	Remaining B, C_n	Any F	2
t_{PLH} / t_{PHL}	A	None	B	None	Remaining A and B, C_n	P	1
t_{PLH} / t_{PHL}	B	A	None	None	Remaining A and B, C_n	P	2
t_{PLH} / t_{PHL}	A	B	None	None	Remaining A and B, C_n	G	1
t_{PLH} / t_{PHL}	B	None	A	None	Remaining A and B, C_n	G	2
t_{PLH} / t_{PHL}	A	B	None	Remaining A	Remaining B, C_n	A = B	2
t_{PLH} / t_{PHL}	B	A	None	Remaining A	Remaining B, C_n	A = B	2
t_{PLH} / t_{PHL}	C_n	None	None	All A and B	None	C_{n+4}	2

LOGIC MODE TEST TABLE

FUNCTION INPUTS: S1 = S3 = M = 4.5 V, S0 = S2 = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} / t_{PHL}	A	None	B	None	Remaining A and B, C_n	Any F	2
t_{PLH} / t_{PHL}	B	None	A	None	Remaining A and B, C_n	Any F	2

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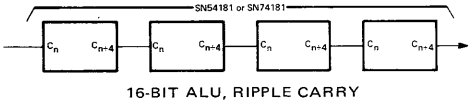
TYPICAL APPLICATION DATA

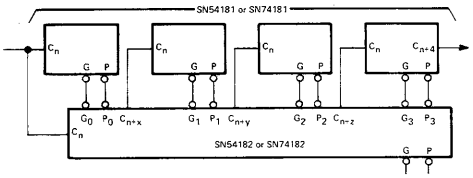
Typical addition times for various configurations are given in the table below. Subtraction times are in the same range as summation times.

TYPICAL ADDITION TIMES

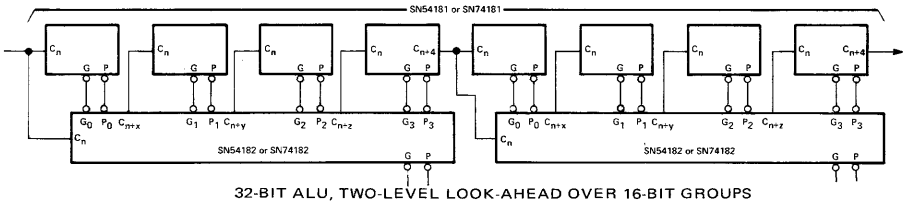
NO. OF BITS	TOTAL ADDITION TIME (ns)	ADD TIME PER BIT (ns)	PACKAGE COUNT		CARRY BETWEEN ALU's
			SN54181/ SN74181	SN54182/ SN74182	
4	24	6.0	1		NONE
8	36	4.5	2		RIPPLE
12	48	4.0	3		RIPPLE
12	36	3.0	3	1	FULL LOOK-AHEAD
16	60	3.8	4		RIPPLE
16	36	2.2	4	1	FULL LOOK-AHEAD
32	120	3.8	8		RIPPLE
32	96	3.0	8	1	PARTIAL LOOK-AHEAD
32	72	2.2	8	2	PARTIAL LOOK-AHEAD
32	60	1.9	8	3	FULL LOOK-AHEAD



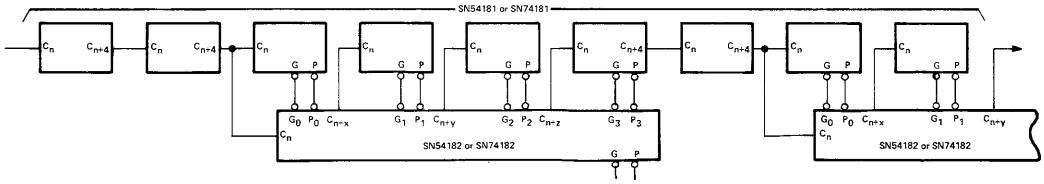
16-BIT ALU, RIPPLE CARRY



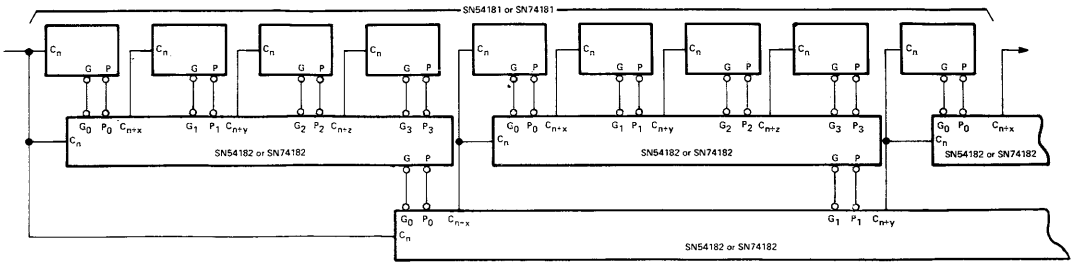
16-BIT ALU, TWO-LEVEL LOOK-AHEAD



32-BIT ALU, TWO-LEVEL LOOK-AHEAD OVER 16-BIT GROUPS



COMBINED TWO-LEVEL LOOK-AHEAD AND RIPPLE-CARRY ALU



64-BIT ALU, FULL-CARRY LOOK-AHEAD IN THREE LEVELS

A and B inputs and F outputs are not shown.

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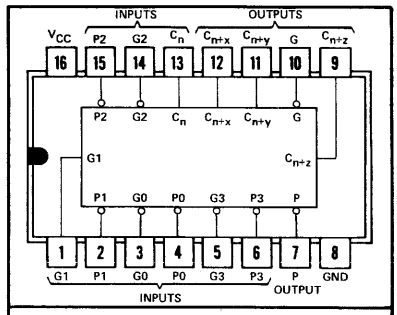
CIRCUIT TYPES SN54182, SN74182
LOOK-AHEAD CARRY GENERATORS

PIN DESIGNATIONS

DESIGNATION	PIN NOS.	FUNCTION
G0, G1, G2, G3	3, 1, 14, 5	ACTIVE-LOW CARRY GENERATE INPUTS
P0, P1, P2, P3	4, 2, 15, 6	ACTIVE-LOW CARRY PROPAGATE INPUTS
C_n	13	CARRY INPUT
C_{n+x}, C_{n+y}, C_{n+z}	12, 11, 9	CARRY OUTPUTS
G	10	ACTIVE-LOW CARRY GENERATE OUTPUT
P	7	ACTIVE-LOW CARRY PROPAGATE OUTPUT
V_{CC}	16	SUPPLY VOLTAGE
GND	8	GROUND

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



logic: see description

†Pin assignments for these circuits are the same for all packages.

description

The SN54182, SN74182 is a high-speed, look-ahead carry generator capable of anticipating a carry across four binary adders or group of adders. It is cascadable to perform full look-ahead across n-bit adders, with only 13 nanoseconds delay for each level of look-ahead. Carry, generate-carry, and propagate-carry functions are provided as enumerated in the pin designation table above.

The SN54182 or SN74182, when used in conjunction with the SN54181 or SN74181 arithmetic logic unit (ALU), provides full high-speed carry look-ahead capability for up to n-bit words. Each SN54182/SN74182 generates the look-ahead (anticipated carry) across a group of four ALUs and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n-bits. Applications data for the SN54181/SN74181 illustrates cascading of SN54182/SN74182 circuits to perform multi-level look-ahead.

Carry inputs and outputs of the SN54181/SN74181 are in their true form and the carry propagate (P) and carry generate (G) are in negated form; therefore, the carry (input, outputs, generate, and propagate) functions of the look-ahead circuit are implemented in the compatible forms. Reinterpretations of carry functions at the SN54181/SN74181 are also applicable and compatible with the look-ahead package. Logic equations are:

$$C_{n+x} = G_0 + P_0C_n$$
$$C_{n+y} = G_1 + P_1G_0 + P_1P_0C_n$$
$$C_{n+z} = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$$
$$\overline{G} = \overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$$
$$\overline{P} = \overline{P_3P_2P_1P_0}$$

Inputs of the SN54182/SN74182 are diode-clamped to minimize transmission-line effects, and Darlington outputs are employed to improve turn-off times and reduce propagation delay times. Typically, the average carry time is 13 nanoseconds, and power dissipation is typically 180 milliwatts or 11 milliwatts per gate. The SN54182 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74182 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54182 Circuits . . . . . −55°C to 125°C
SN74182 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies to each G input in conjunction with any other G input or in conjunction with any P input.

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recommended operating conditions

		SN54182			SN74182			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Operating free-air temperature range, T_A		−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

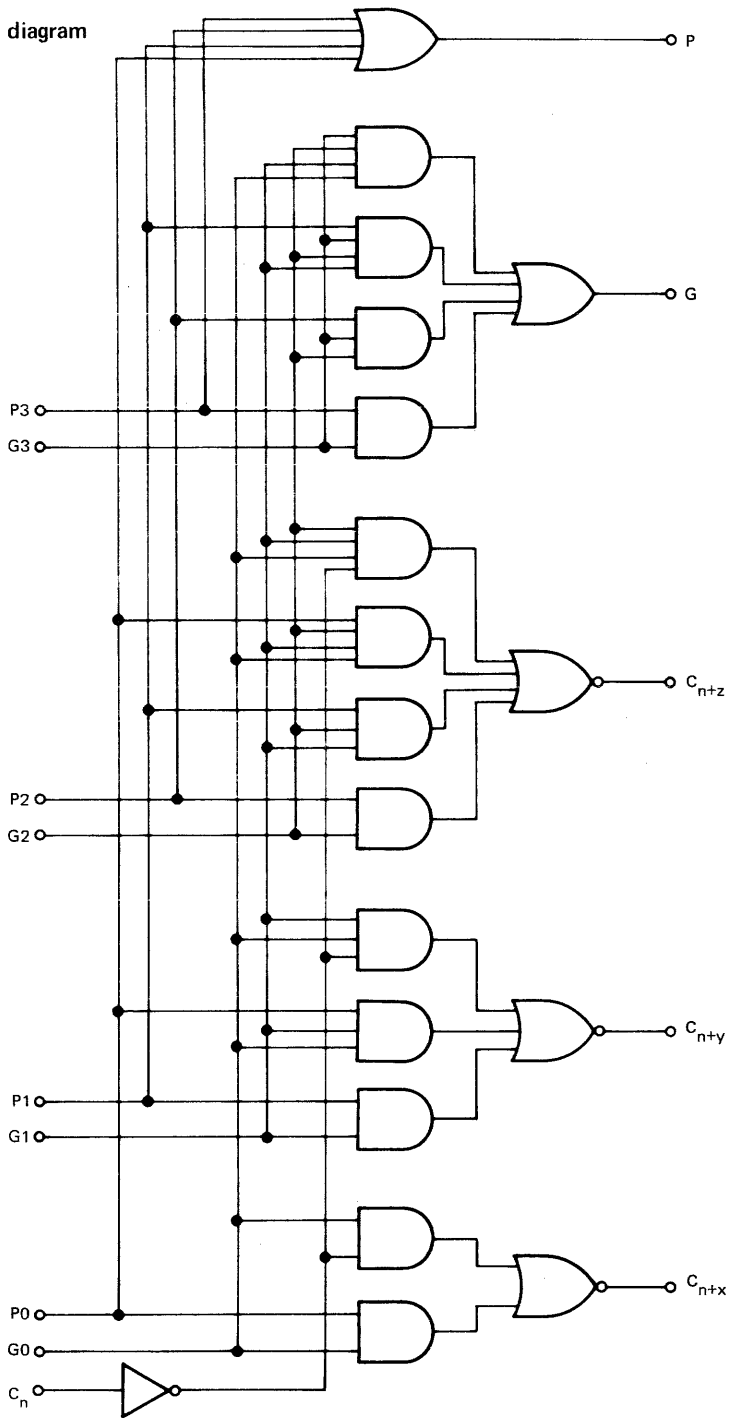
PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage	1 and 2			2			V
V_{IL}	Low-level input voltage	1 and 2					0.8	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4			V
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA				0.4	V
I_{IH}	High-level input current (C_n input)	3	V_{CC} = MAX, V_I = 2.4 V				80	μA
I_{IH}	High-level input current (P3 input)						120	μA
I_{IH}	High-level input current (P2 input)						160	μA
I_{IH}	High-level input current (P0, P1, or G3 input)						200	μA
I_{IH}	High-level input current (G0 or G2 input)						360	μA
I_{IH}	High-level input current (G1 input)						400	μA
I_{IH}	High-level input current (any input)	3	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IL}	Low-level input current (C_n input)	3	V_{CC} = MAX, V_I = 0.4 V				−3.2	mA
I_{IL}	Low-level input current (P3 input)						−4.8	mA
I_{IL}	Low-level input current (P2 input)						−6.4	mA
I_{IL}	Low-level input current (P0, P1, or G3 input)						−8	mA
I_{IL}	Low-level input current (G0 or G2 input)						−14.4	mA
I_{IL}	Low-level input current (G1 input)						−16	mA
I_{OS}	Short-circuit output current§	4	V_{CC} = MAX		−40		−100	mA
I_{CCH}	Supply current, all outputs high	5	V_{CC} = MAX	SN54182		27		mA
				SN74182		27		
I_{CCL}	Supply current, all outputs low	6	V_{CC} = MAX	SN54182		45	65	mA
				SN74182		45	72	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of the short-circuit test should not exceed 1 second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	7	C_L = 15 pF, R_L = 400 Ω		11	17	ns
t_{PHL}	Propagation delay time, high-to-low-level output				15	22	ns

functional block diagram



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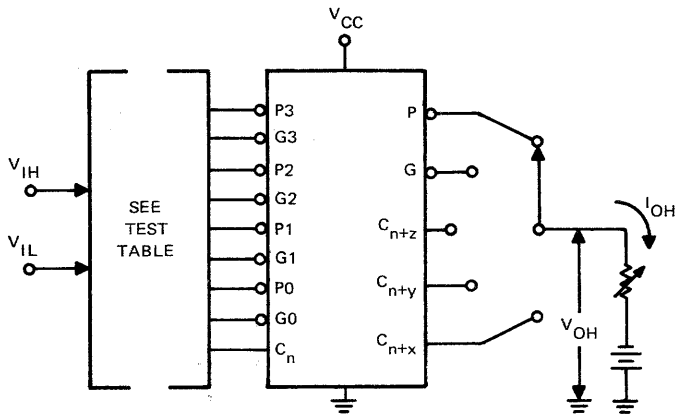
PARAMETER MEASUREMENT INFORMATION

d-c test circuits¶

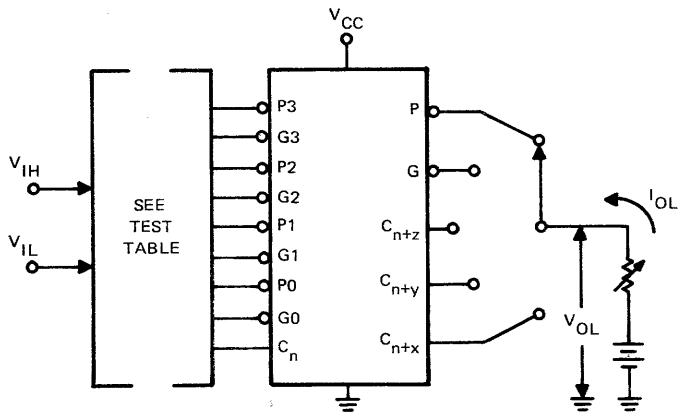


TEST TABLE

OUTPUT UNDER TEST	APPLY V_{IH}	APPLY V_{IL}
P	P0	P3, P2, P1
G	P3, G3	P2, P1, G2, G1, G0
C_{n+z}	P2, P1, P0, G1, G0	G2, C_n
C_{n+y}	P1, P0, G0	G1, C_n
C_{n+x}	P0	G0, C_n

Inputs not otherwise specified are connected to ground.

FIGURE 1–V_{IH}, V_{IL}, V_{OH}



TEST TABLE

OUTPUT UNDER TEST	APPLY V_{IH}	APPLY V_{IL}
P	NONE	P3, P2, P1, P0
G	P3, P2, P1, G2, G1, P0, G0	G3
C_{n+z}	P2, G2, C_n	P1, G1, P0, G0
C_{n+y}	P1, G1, C_n	P0, G0
C_{n+x}	P0, G0, C_n	NONE

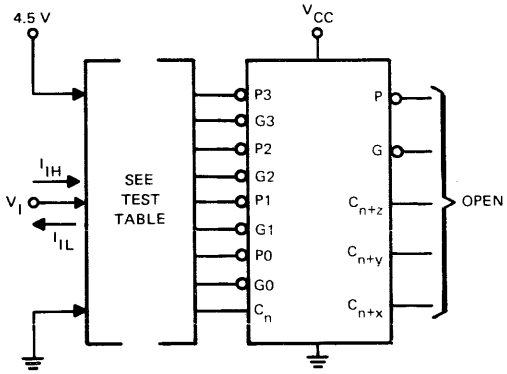
Inputs not otherwise specified are connected to ground.

FIGURE 2–V_{IH}, V_{IL}, V_{OL}

¶Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)

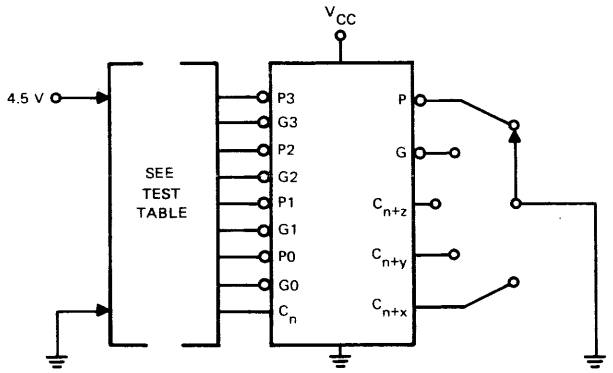


TEST TABLE

APPLY V_I, MEASURE	CONDITIONS ON OTHER INPUTS FOR I_{IH}		CONDITIONS ON OTHER INPUTS FOR I_{IL}	
I_{IH}, I_{IL}	APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND
any P, or C_n	NONE	ALL OTHER INPUTS	ALL OTHER INPUTS	NONE
any G	C_n	ALL OTHER INPUTS	ALL OTHER INPUTS	C_n

Each input is tested separately.

FIGURE 3–I_{IH}, I_{IL}



TEST TABLE

OUTPUT UNDER TEST	APPLY 4.5 V	APPLY GND
P	P3, P2, P1, P0	ALL OTHER INPUTS
G	ALL OTHER INPUTS	C_n
C_{n+z}	C_n	ALL OTHER INPUTS
C_{n+y}	C_n	ALL OTHER INPUTS
C_{n+x}	C_n	ALL OTHER INPUTS

FIGURE 4–I_{OS}

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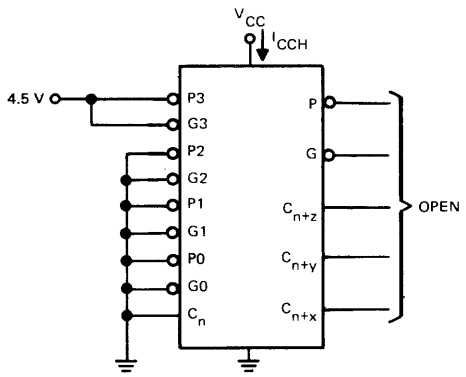

FIGURE 5–I_{CCH}

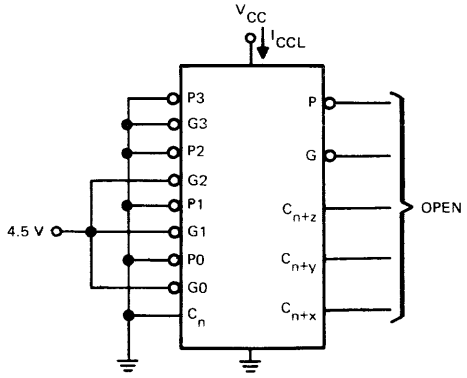

FIGURE 6–I_{CCL}

§ Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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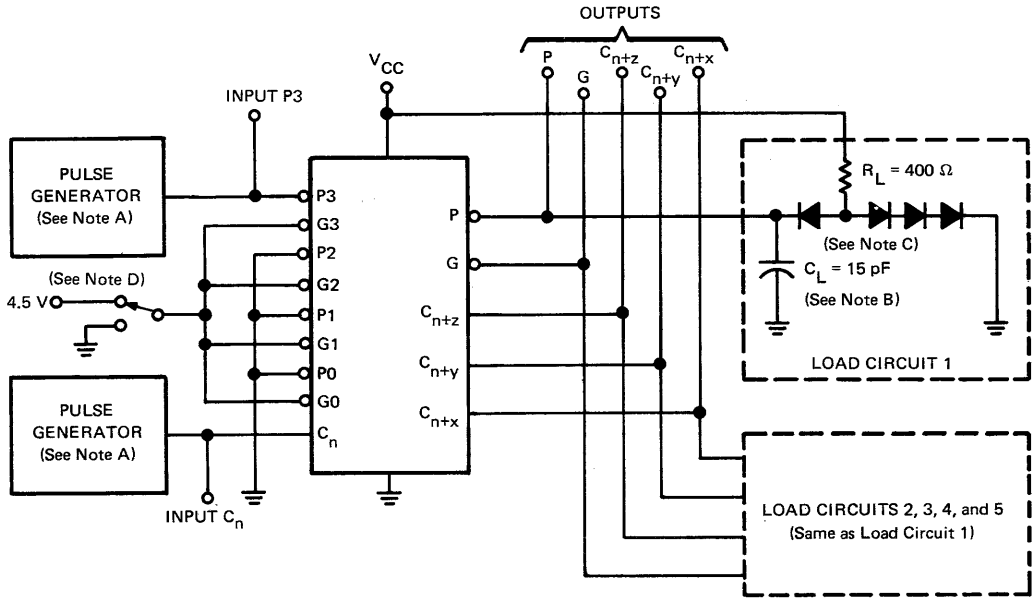
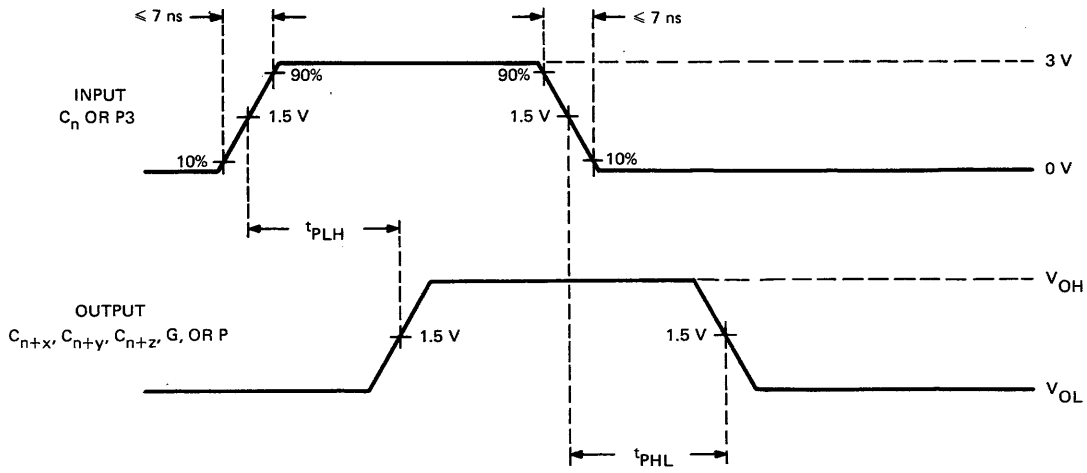
PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$, duty cycle = 50%.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.
D. Apply 4.5 V for all tests except G output. When testing G output, apply ground.

FIGURE 7–PROPAGATION DELAY TIMES

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CIRCUIT TYPES SN54H183, SN74H183
DUAL CARRY-SAVE FULL ADDERS

- For Use in Multiple-Input Carry-Save Adders
- High-Speed, High-Fan-Out Darlington Outputs
- Input Clamping Diodes Simplify System Design
- Compatible with Most TTL and DTL Circuits
- Typical Average Sum and Carry Propagation Delays: 11 ns
- Typical Power Dissipation: 110 mW per Bit

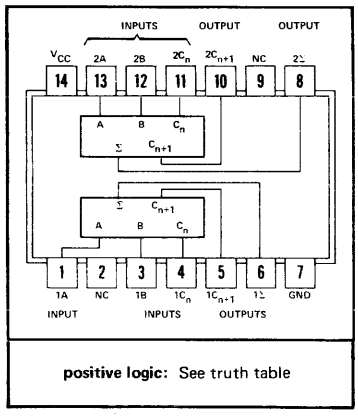
logic

TRUTH TABLE

INPUTS			OUTPUTS	
C_n	B	A	Σ	C_{n+1}
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

H = high level, L = low level

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



positive logic: See truth table

NC—No internal connection

†Pin assignments for these circuits are the same for all packages.

description

This dual full adder features an individual carry output from each bit for use in multiple-input, carry-save techniques to produce the true sum and true carry outputs with no more than two levels of logic. The circuit utilizes high-speed, high-fan-out, transistor-transistor logic (TTL), but is compatible with both DTL and TTL families. Typical average sum and carry propagation delay times are 11 nanoseconds each. Typical power dissipation is 110 milliwatts per bit. The SN54H183 is characterized for operation over the full military temperature range of −55°C to 125°C, and the SN74H183 is characterized for operation from 0°C to 70°C.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range, T_A: SN54H183 Circuits . . . . . −55°C to 125°C
SN74H183 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor.

recommended operating conditions

		SN54H183			SN74H183			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Operating free-air temperature range, T_A		−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

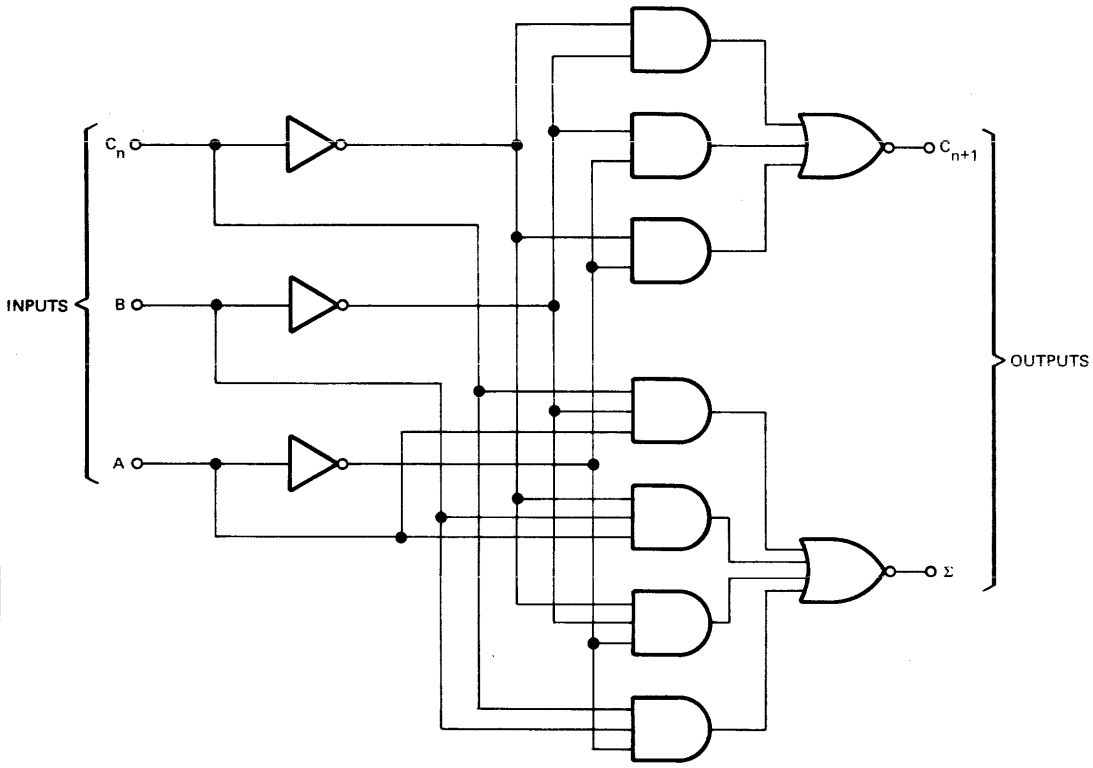
PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage	1			2			V
V_{IL}	Low-level input voltage	2					0.8	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, V_{IH} = 2 V, I_{OH} = −1 mA		2.4			V
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 20 mA				0.4	V
I_{IH}	High-level input current at any input	3	V_{CC} = MAX, V_I = 2.4 V				150	μA
			V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IL}	Low-level input current at any input	3	V_{CC} = MAX, V_I = 0.4 V				−6	mA
I_{OS}	Short-circuit output current§	4	V_{CC} = MAX		−40		−100	mA
I_{CCL}	Supply current, all outputs low	5	V_{CC} = MAX, V_I = 0	SN54H183		48	69	mA
				SN74H183		48	75	
I_{CCH}	Supply current, all outputs high	5	V_{CC} = MAX, V_I = 4.5 V			40		mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short circuit test should not exceed 1 second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	6	C_L = 25 pF, R_L = 280 Ω		10	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output				12	18	ns

functional block diagram (each adder)



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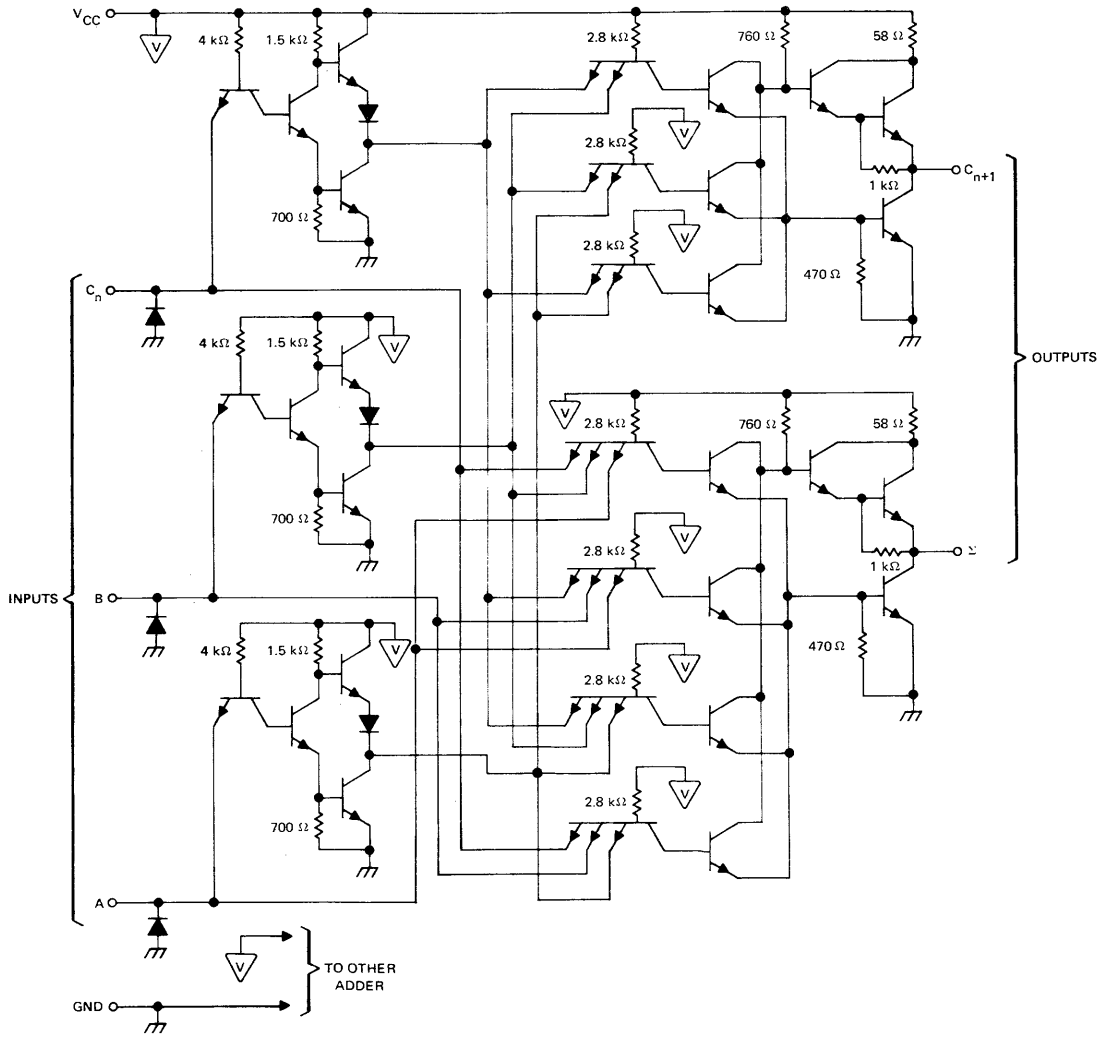
schematic (each adder)



Component values shown are nominal.

▽... V_{CC} bus

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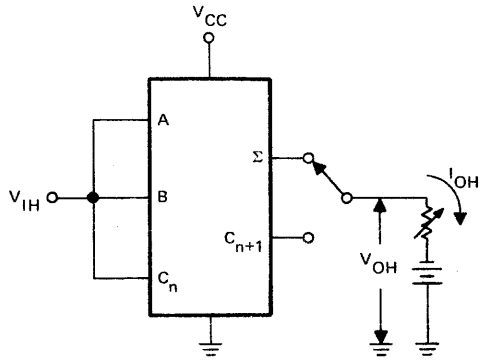
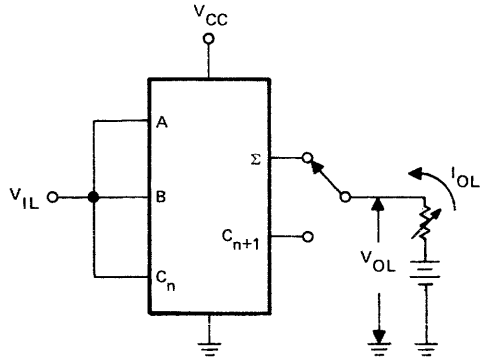
PARAMETER MEASUREMENT INFORMATION

d-c test circuits¶



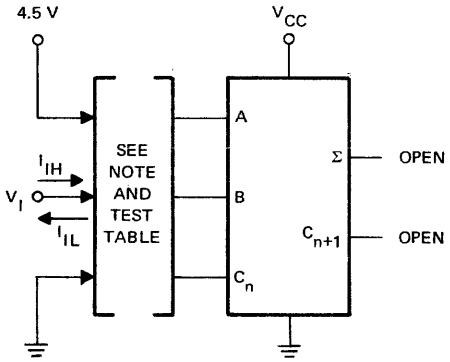
Each output is tested separately.

FIGURE 1–V_{IH}, V_{OH}



Each output is tested separately.

FIGURE 2–V_{IL}, V_{OL}

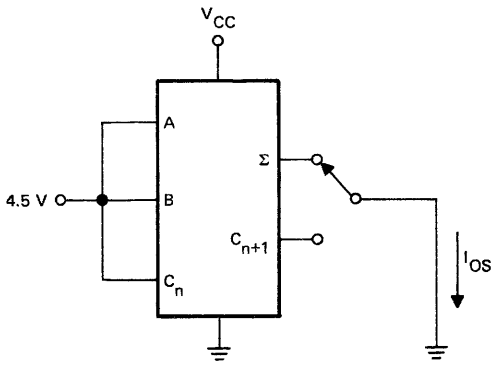


Each input is tested for both combinations of states of the other inputs.

TEST TABLE

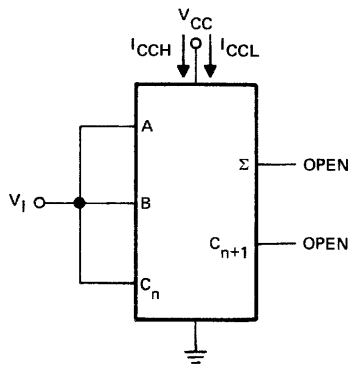
APPLY V_I, MEASURE I_{IH}/I_{IL}	CONDITIONS ON OTHER INPUTS	
	4.5 V	GND
A	B, C_n	NONE
	B	C_n
	C_n	B
	NONE	B, C_n
B	A, C_n	NONE
	A	C_n
	C_n	A
	NONE	A, C_n
C_n	A, B	NONE
	A	B
	B	A
	NONE	A, B

FIGURE 3–I_{IH}, I_{IL}



Each output is tested separately.

FIGURE 4–I_{OS}



Both adders are tested simultaneously.

FIGURE 5–I_{CCH}, I_{CCL}

¶ Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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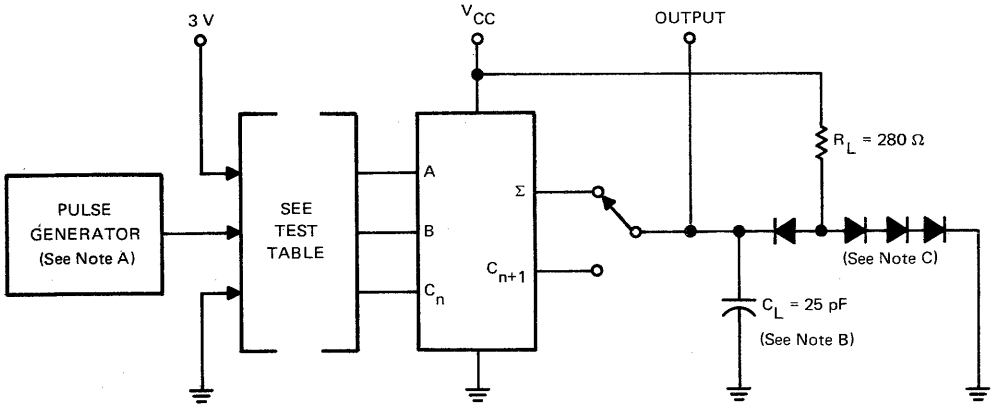
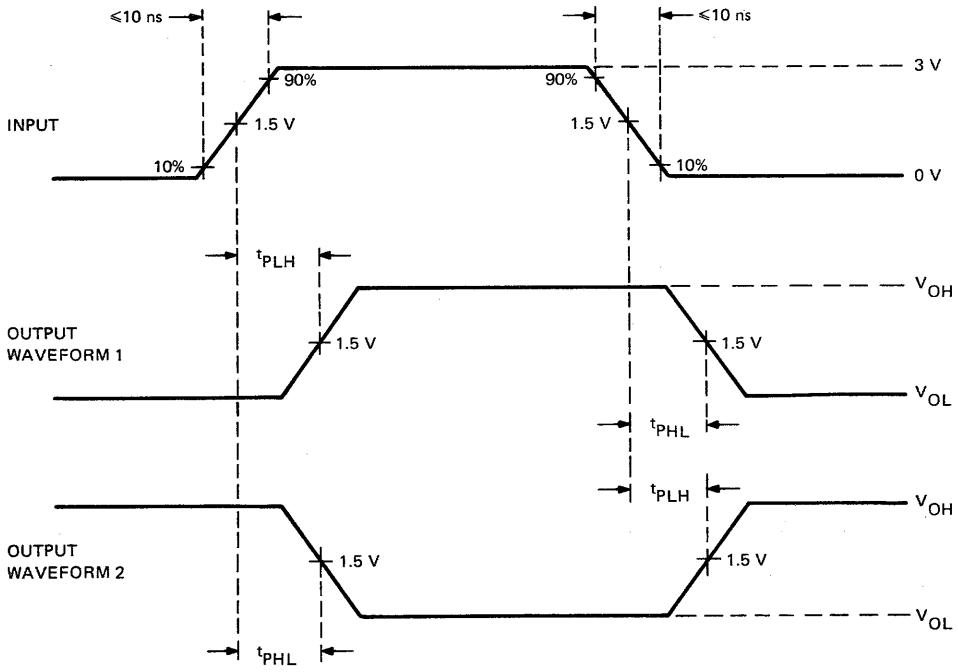
PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.

FIGURE 6–PROPAGATION DELAY TIMES

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PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)

TEST TABLE FOR FIGURE 6 (EACH ADDER)

TEST NO.	PARAMETER	APPLY PULSE GENERATOR	APPLY 3 V	APPLY GND	OUTPUT UNDER TEST	OUTPUT WAVEFORM
1	t_{PLH}	A	B, C_n		Σ	1
2	t_{PHL}					
3	t_{PLH}	A	B	C_n	Σ	2
4	t_{PHL}					
5	t_{PLH}	A	C_n	B	Σ	2
6	t_{PHL}					
7	t_{PLH}	A		B, C_n	Σ	1
8	t_{PHL}					
9	t_{PLH}	A	B	C_n	C_{n+1}	1
10	t_{PHL}					
11	t_{PLH}	A	C_n	B	C_{n+1}	1
12	t_{PHL}					
13	t_{PLH}	B	A, C_n		Σ	1
14	t_{PHL}					
15	t_{PLH}	B	A	C_n	Σ	2
16	t_{PHL}					
17	t_{PLH}	B	C_n	A	Σ	2
18	t_{PHL}					
19	t_{PLH}	B		A, C_n	Σ	1
20	t_{PHL}					
21	t_{PLH}	B	A	C_n	C_{n+1}	1
22	t_{PHL}					
23	t_{PLH}	B	C_n	A	C_{n+1}	1
24	t_{PHL}					
25	t_{PLH}	C_n	A, B		Σ	1
26	t_{PHL}					
27	t_{PLH}	C_n	A	B	Σ	2
28	t_{PHL}					
29	t_{PLH}	C_n	B	A	Σ	2
30	t_{PHL}					
31	t_{PLH}	C_n		A, B	Σ	1
32	t_{PHL}					
33	t_{PLH}	C_n	A	B	C_{n+1}	1
34	t_{PHL}					
35	t_{PLH}	C_n	B	A	C_{n+1}	1
36	t_{PHL}					

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CIRCUIT TYPES SN54150, SN54151, SN54152, SN74150, SN74151, SN74152
DATA SELECTORS/MULTIPLEXERS

features

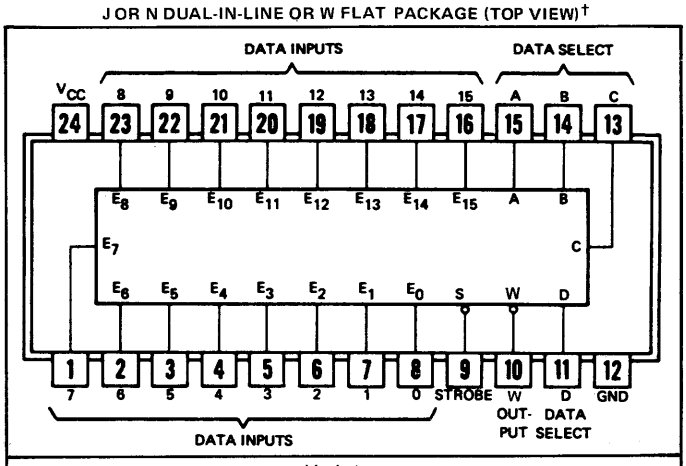
- selects one-of-sixteen (or one-of-eight) data sources
- serves as a five-variable-function generator (SN54150, SN74150)
- performs parallel-to-serial conversion
- permits multiplexing from N lines to 1 line
- input-clamping diodes simplify system design
- typical propagation delay times:

  through 4 select levels – 28 ns

  through 3 select levels – 20 ns

  data input to output – 10 ns
- high fan-out, low impedance, totem-pole outputs
- fully compatible with TTL, DTL and other MSI circuits

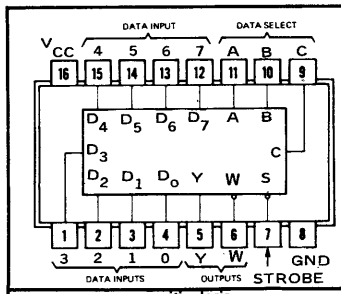
SN54150, SN74150
J OR N DUAL-IN-LINE OR W FLAT PACKAGE (TOP VIEW)†



positive logic

$$W = S(\bar{A}\bar{B}\bar{C}\bar{D}E_0 + A\bar{B}\bar{C}\bar{D}E_1 + \bar{A}B\bar{C}\bar{D}E_2 + AB\bar{C}\bar{D}E_3 + \bar{A}\bar{B}C\bar{D}E_4 + A\bar{B}C\bar{D}E_5 + \bar{A}BC\bar{D}E_6 + ABC\bar{D}E_7$$
$$\bar{A}\bar{B}\bar{C}DE_8 + A\bar{B}\bar{C}DE_9 + \bar{A}B\bar{C}DE_{10} + AB\bar{C}DE_{11} + \bar{A}\bar{B}CDE_{12} + A\bar{B}CDE_{13} + \bar{A}BCDE_{14} + ABCDE_{15})$$

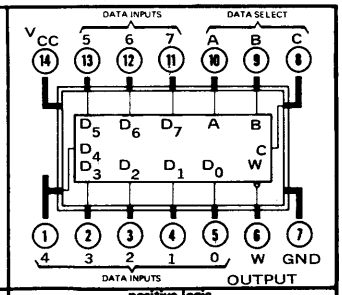
SN54151, SN74151
J OR N DUAL-IN-LINE OR W FLAT PACKAGE (TOP VIEW)†



positive logic

$$Y = \bar{S}(\bar{A}\bar{B}\bar{C}D_0 + A\bar{B}\bar{C}D_1 + \bar{A}B\bar{C}D_2 + AB\bar{C}D_3 + \bar{A}\bar{B}CD_4 + A\bar{B}CD_5 + \bar{A}BCD_6 + ABCD_7) \quad W = \bar{Y}$$

SN54152, SN74152
W FLAT PACKAGE
(TOP VIEW)



positive logic

$$W = (\bar{A}\bar{B}\bar{C}D_0 + A\bar{B}\bar{C}D_1 + AB\bar{C}D_3 + \bar{A}\bar{B}CD_4 + A\bar{B}CD_5 + \bar{A}BCD_6 + ABCD_7)$$

†Pin assigments for these circuits are the same for all packages.

description

Each of these monolithic, data selectors/multiplexers contain inverter/drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-INVERT gate. The SN54151/74151 features complementary outputs whereas the SN54150/SN74150 and SN54152/SN74152 have inverted outputs only. The SN54150/SN74150 and SN54151/SN74151 circuits are provided with a strobe-input which, when taken to a logical 0, enables the function of these multiplexers.

These data selectors/multiplexers are fully compatible for use with other TTL or DTL circuits. Each input represents only one normalized Series 54/74 load, and full fan-out to 10 normalized Series 54/74 loads is available from each of the outputs in the logical 0 state. A fan-out to 20 normalized Series 54/74 loads is provided in the logical 1 state to facilitate connection of unused inputs to used inputs. Typical power dissipations are:

SN54150/SN74150 – 200 milliwatts
SN54151/SN74151 – 145 milliwatts
SN54152/SN74152 – 130 milliwatts

These data selectors feature Series 54H/74H circuitry for the OR function. This is done to minimize the capacitive effects of paralleling the phase-splitter transistors and thus reduce the propagation delay time. The SN54150, SN54151, and SN54152 are characterized for operation over the full military temperature range of −55°C to 125°C; and the SN74150, SN74151 and SN74152 are characterized for operation from 0°C to 70°C.

logic

TRUTH TABLE (SN54150/SN74150 ONLY)

INPUTS																		OUTPUT
D	C	B	A	STROBE	E_0	E_1	E_2	E_3	E_4	E_5	E_6	E_7	E_8	E_9	E_{10}	E_{11}	E_{12}	E_{13}	E_{14}	E_{15}	W
X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	0	1	0	X	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	1	0	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	1	0	0	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	1	0	0	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	1	1	0	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	1	1	0	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	0
0	1	0	0	0	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	1
0	1	0	0	0	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	0
0	1	0	1	0	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	1
0	1	0	1	0	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	0
0	1	1	0	0	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	1
0	1	1	0	0	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	0
0	1	1	1	0	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	1
0	1	1	1	0	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	0
1	0	0	0	0	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	1
1	0	0	0	0	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	0
1	0	0	1	0	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	1
1	0	0	1	0	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	0
1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	1
1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	0
1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	1
1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	0
1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	1
1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	0
1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	1
1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	0
1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	1
1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	0
1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	1
1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	0

When used to indicate an input condition, X = LOGICAL 1 OR LOGICAL 0

logic (continued)

TRUTH TABLE (SN54151/SN74151 AND SN54152/SN74152 ONLY)

INPUTS												OUTPUTS	
C	B	A	STROBE(1)	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Y(1)	W
X	X	X	1	X	X	X	X	X	X	X	X	0	1
0	0	0	0	0	X	X	X	X	X	X	X	0	1
0	0	0	0	1	X	X	X	X	X	X	X	1	0
0	0	1	0	X	0	X	X	X	X	X	X	0	1
0	0	1	0	X	1	X	X	X	X	X	X	1	0
0	1	0	0	X	X	0	X	X	X	X	X	0	1
0	1	0	0	X	X	1	X	X	X	X	X	1	0
0	1	1	0	X	X	X	0	X	X	X	X	0	1
0	1	1	0	X	X	X	1	X	X	X	X	1	0
1	0	0	0	X	X	X	X	0	X	X	X	0	1
1	0	0	0	X	X	X	X	1	X	X	X	1	0
1	0	1	0	X	X	X	X	X	0	X	X	0	1
1	0	1	0	X	X	X	X	X	1	X	X	1	0
1	1	0	0	X	X	X	X	X	X	0	X	0	1
1	1	0	0	X	X	X	X	X	X	1	X	1	0
1	1	1	0	X	X	X	X	X	X	X	0	0	1
1	1	1	0	X	X	X	X	X	X	X	1	1	0

NOTES: 1. SN54151/SN74151 only.
2. When used to indicate an input, X = irrelevant.

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absolute maximum ratings (over operating temperature range unless otherwise noted)

Supply Voltage V_{CC} (See Note 1) . . . . . 7 V
Input Voltage, V_{in} (See Note 1) . . . . . 5.5 V
Operating Free-Air Temperature Range: SN54150, SN54151, SN54152 Circuits . . . . . −55°C to 125°C
SN74150, SN74151, SN74152 Circuits . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1):	SN54150, SN54151, SN54152 Circuits	4.5	5	5.5	V
	SN74150, SN74151, SN74152 Circuits	4.75	5	5.25	V
Normalized Fan-Out from Each Output (N):	Logical 0			10	
	Logical 1			20	

electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	2					0.8	V
$V_{out(1)}$	Logical 1 output voltage	1 AND 2	V_{CC} = MIN, $V_{in(1)}$ = 2 V, $V_{in(0)}$ = 0.8 V, I_{load} = −800 μA		2.4			V
$V_{out(0)}$	Logical 0 output voltage	1 AND 2	V_{CC} = MIN, $V_{in(1)}$ = 2 V, $V_{in(0)}$ = 0.8 V, I_{sink} = 16 mA				0.4	V
$I_{in(1)}$	Logical 1 level input current (each input)	3	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
I_{OS}	Short circuit output current §	4	V_{CC} = MAX, V_{out} = 0	SN54150, SN54151, SN54152	−20		−55	mA
				SN74150, SN74151, SN74152	−18		−55	mA
I_{CC}	Supply current (SN54150/SN74150)	5	V_{CC} = MAX, V_{in} = 4.5 V			40	68	mA
I_{CC}	Supply current (SN54151/SN74151)	5	V_{CC} = MAX, V_{in} = 4.5 V			29	48	mA
I_{CC}	Supply current (SN54152/SN74152)	5	V_{CC} = MAX, V_{in} = 4.5 V			26	43	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

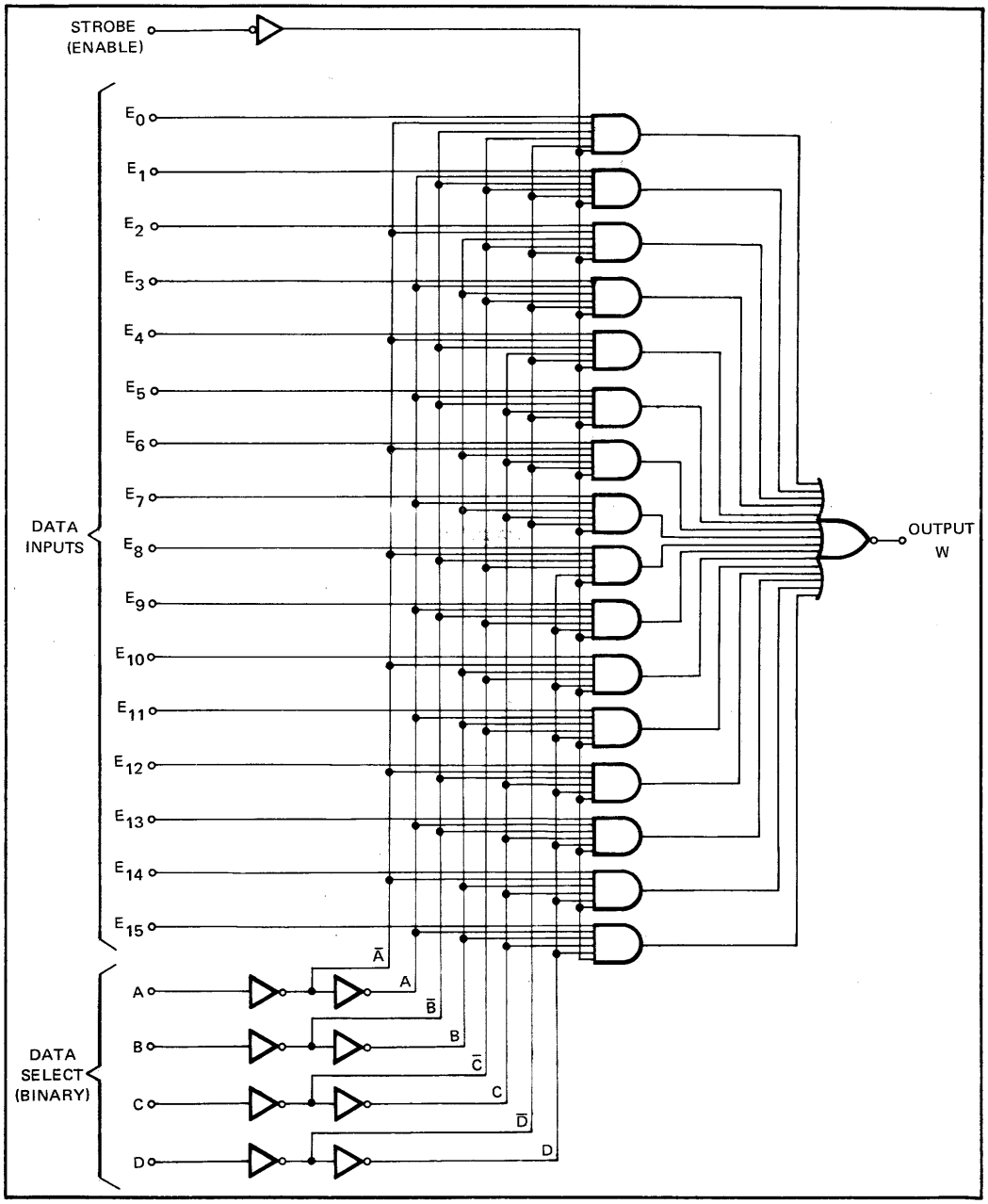
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	A, B, or C (4 levels)	Y	6	C_L = 15 pF, R_L = 400 Ω		20	30	ns
t_{pd1}	A, B, or C (4 levels)	Y				35	52	ns
t_{pd0}	A, B, C, or D (3 levels)	W				22	33	ns
t_{pd1}	A, B, C, or D (3 levels)	W				23	35	ns
t_{pd0}	STROBE	Y				19	30	ns
t_{pd1}	STROBE	Y				35	52	ns
t_{pd0}	STROBE	W				21	30	ns
t_{pd1}	STROBE	W				15.5	24	ns
t_{pd0}	D_0 thru D_7	Y				16	24	ns
t_{pd1}	D_0 thru D_7	Y				19	29	ns
t_{pd0}	E_0 thru E_{15}, D_0 thru D_7	W				8.5	14	ns
t_{pd1}	E_0 thru E_{15}, D_0 thru D_7	W				13	20	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

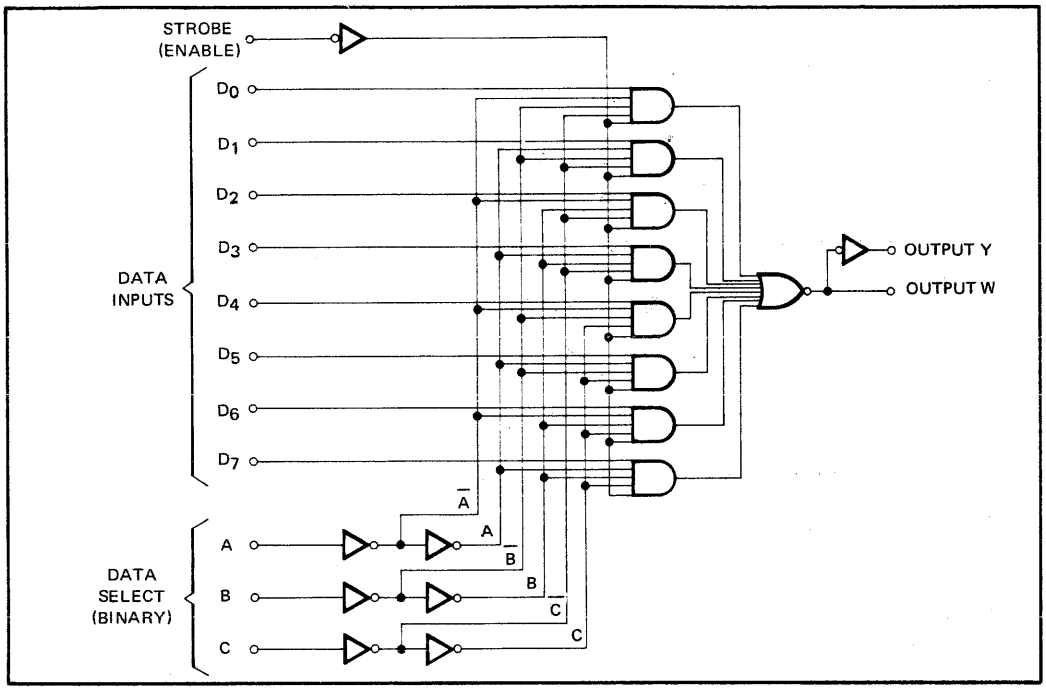
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output of the SN54151/SN74151 should be shorted at a time.

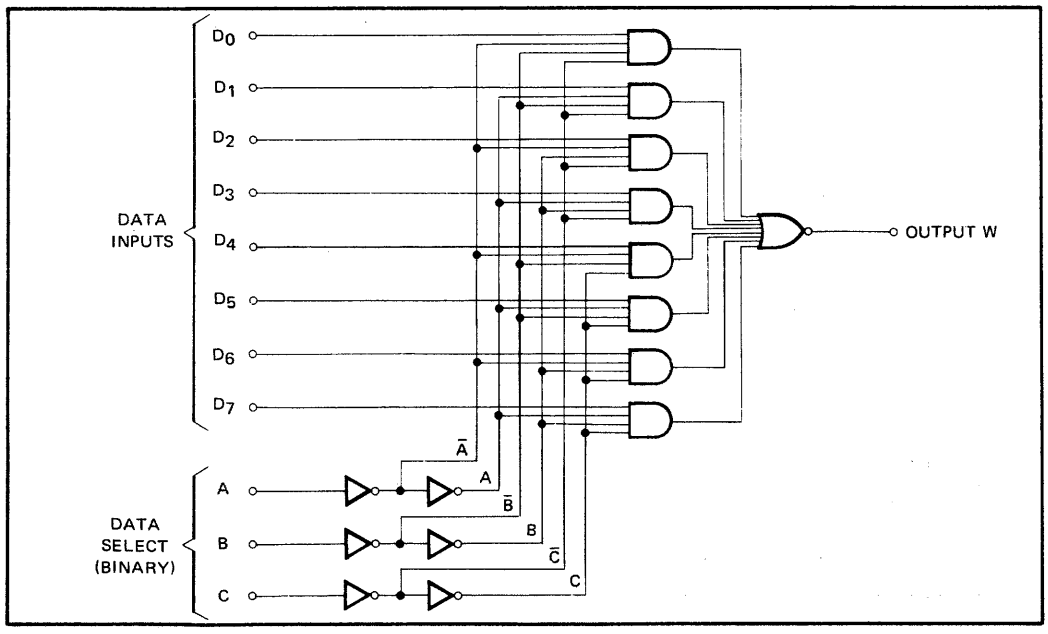
functional block diagram



functional block diagram (SN54151, SN74151)



functional block diagram (SN54152, SN74152)



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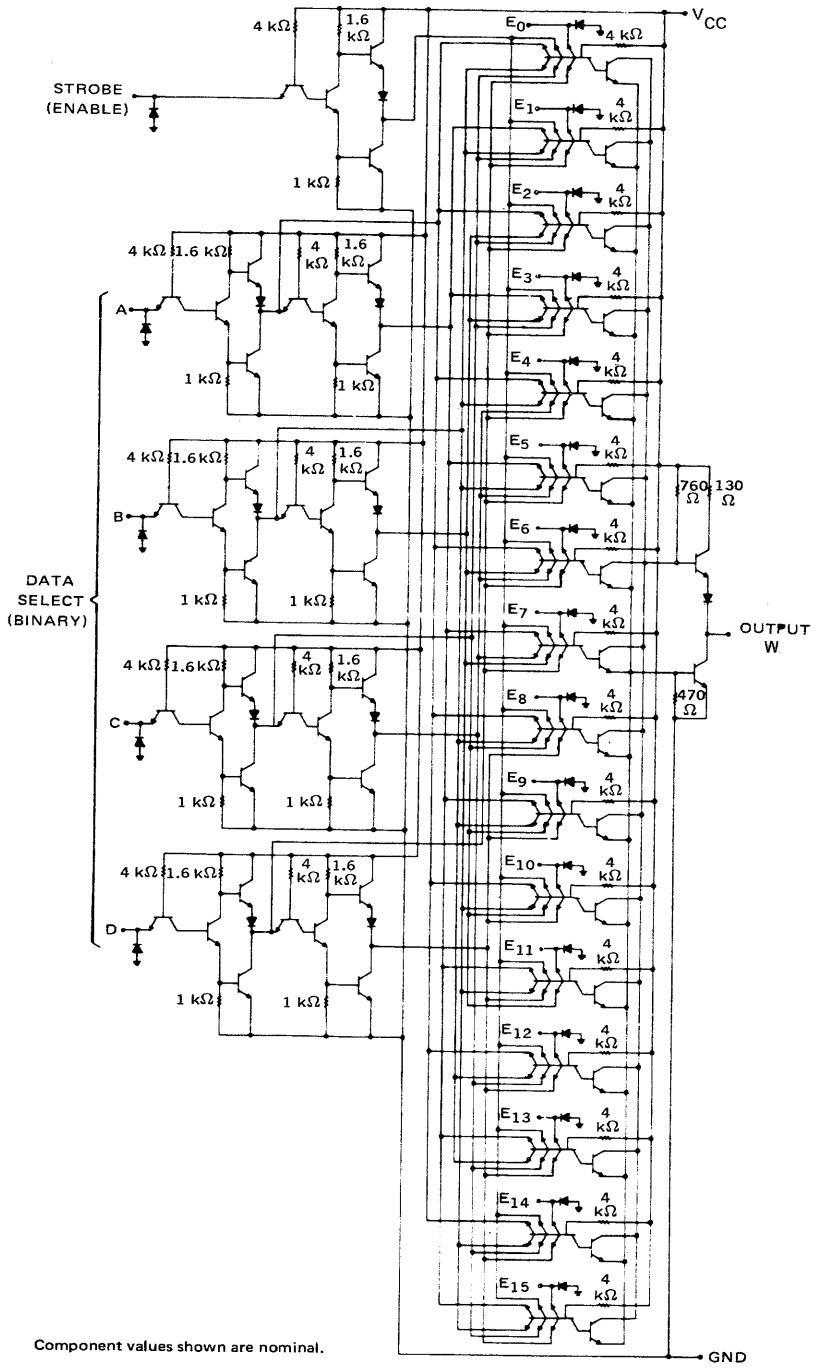
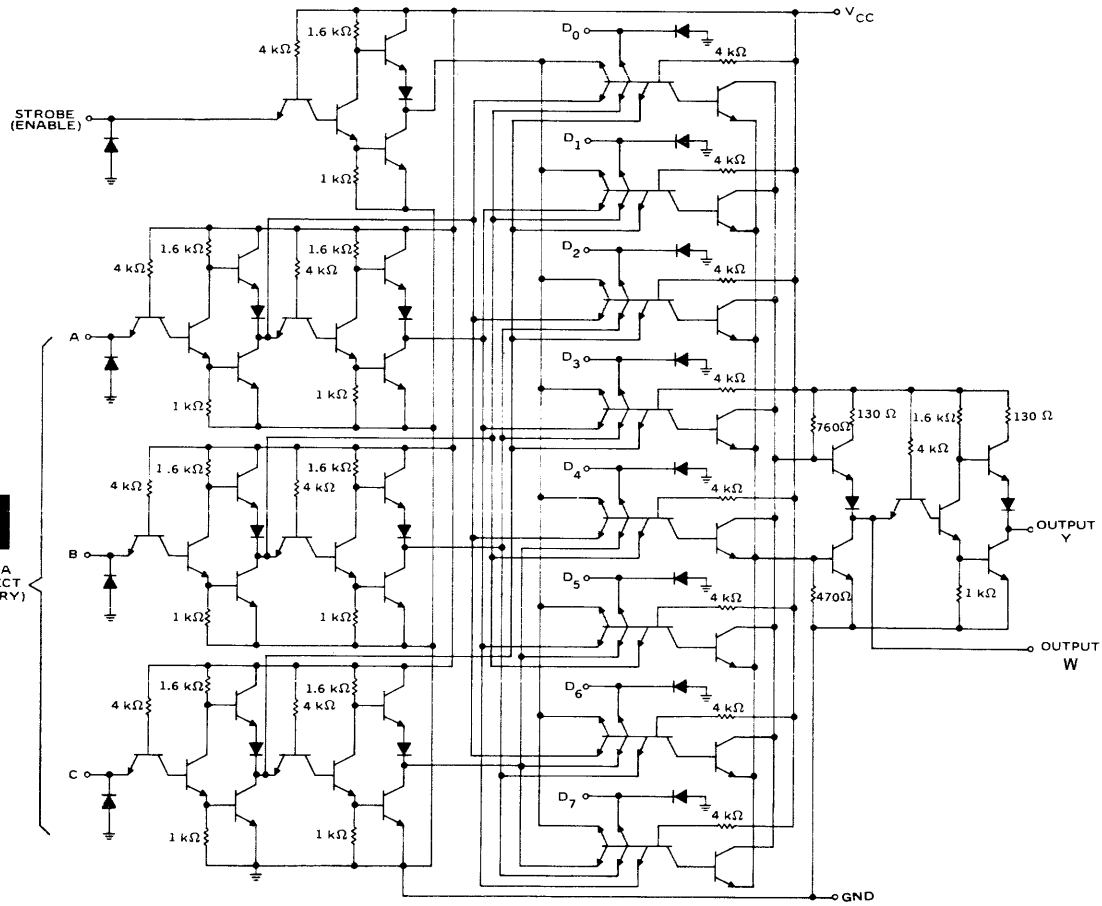
schematic



Component values shown are nominal.

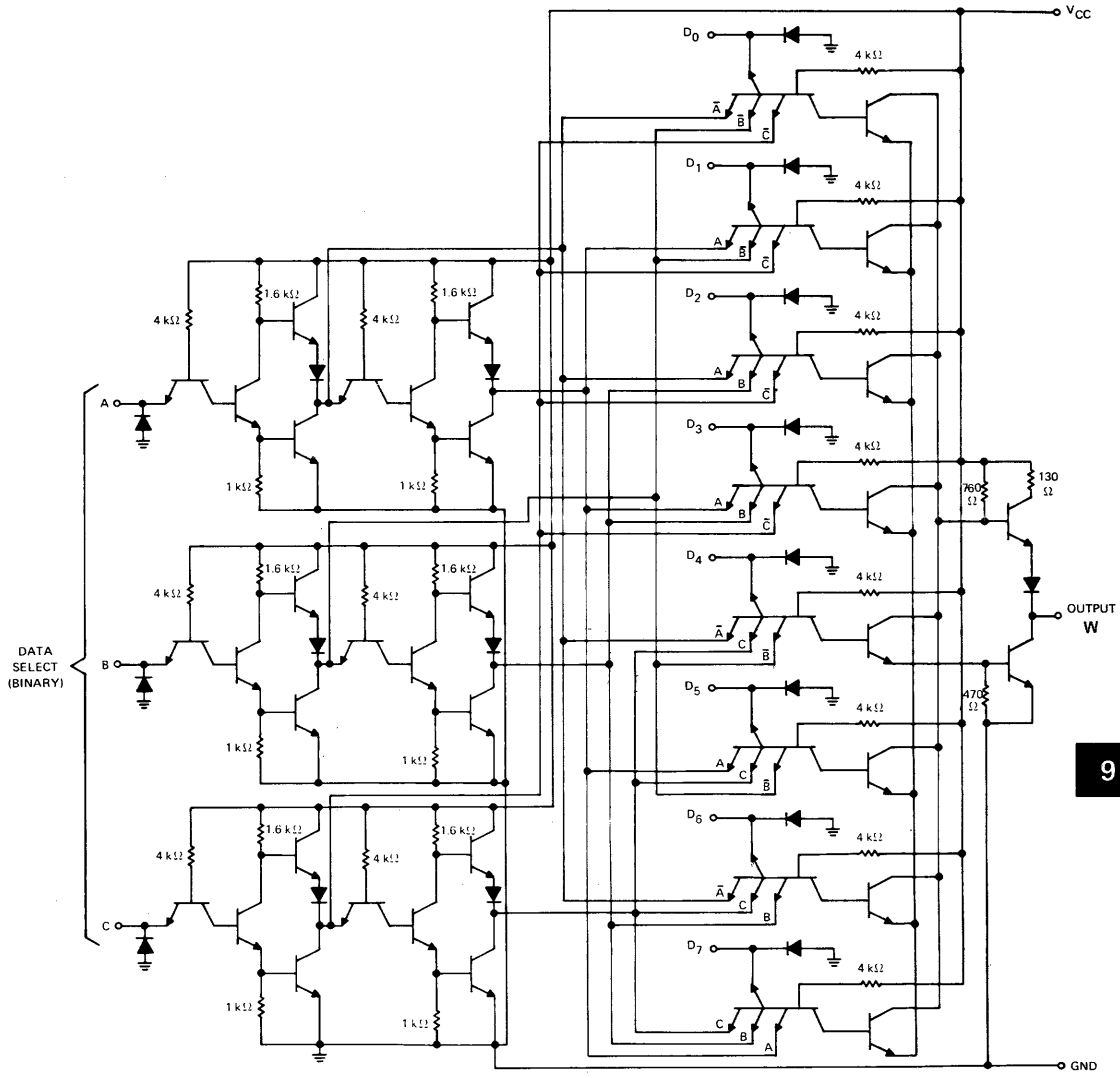
9

schematic



Component values shown are nominal.

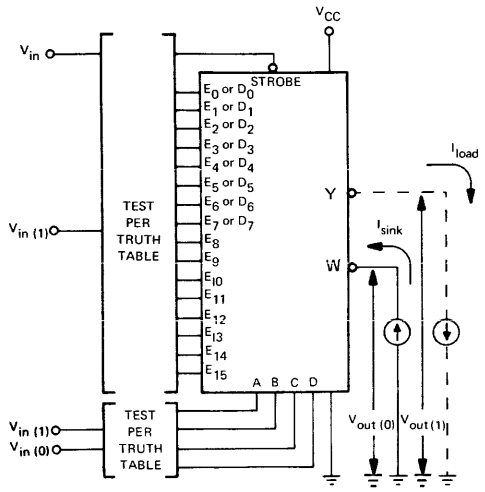
schematic



Component values shown are nominal.

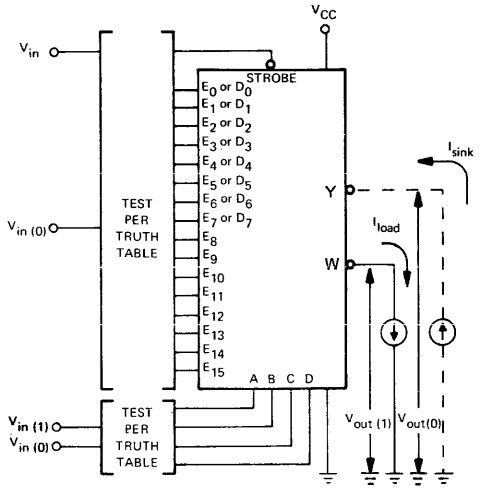
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



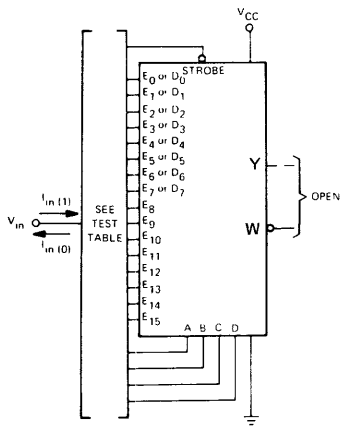
1. $V_{in(0)}$ is applied to STROBE; 8-4-2-1 code is applied to A, B, C, D; and input/output condition is tested for each step of the code.
2. $V_{in(1)}$ is applied to STROBE at which time $V_{out(0)}$ is measured at Y and $V_{out(1)}$ is measured at W.

FIGURE 1



1. $V_{in(0)}$ is applied to STROBE; 8-4-2-1 is applied to A, B, C, D; and input/output condition is tested for each step of the code.

FIGURE 2



TEST TABLE

INPUT CONDITIONS				TEST	
A	B	C	D	$I_{in(0)}$	$I_{in(1)}$
0	0	0	0	E_0 or D_0	E_{15} or D_7
1	0	0	0	E_1 or D_1	E_{14} or D_6
0	1	0	0	E_2 or D_2	E_{13} or D_5
1	1	0	0	E_3 or D_3	E_{12} or D_4
0	0	1	0	E_4 or D_4	E_{11} or D_3
1	0	1	0	E_5 or D_5	E_{10} or D_2
0	1	1	0	E_6 or D_6	E_9 or D_1
1	1	1	0	E_7 or D_7	E_8 or D_0
0	0	0	1	E_8	E_7
1	0	0	1	E_9	E_6
0	1	0	1	E_{10}	E_5
1	1	0	1	E_{11}	E_4

INPUT CONDITIONS				TEST	
A	B	C	D	$I_{in(0)}$	$I_{in(1)}$
0	0	1	1	E_{12}	E_3
1	0	1	1	E_{13}	E_2
0	1	1	1	E_{14}	E_1
1	1	1	1	E_{15}	E_0
0				A	
	0			B	
		0		C	
			0	D	
1					A
	1				B
		1			C
			1		D

1. When testing strobe input, all other inputs are open.

FIGURE 3

† Arrows indicate actual direction of current flow. Tests as shown, are for the SN54150/SN74150. Identical tests as applicable are performed for the SN54151/SN74151 and SN54152/SN74152.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

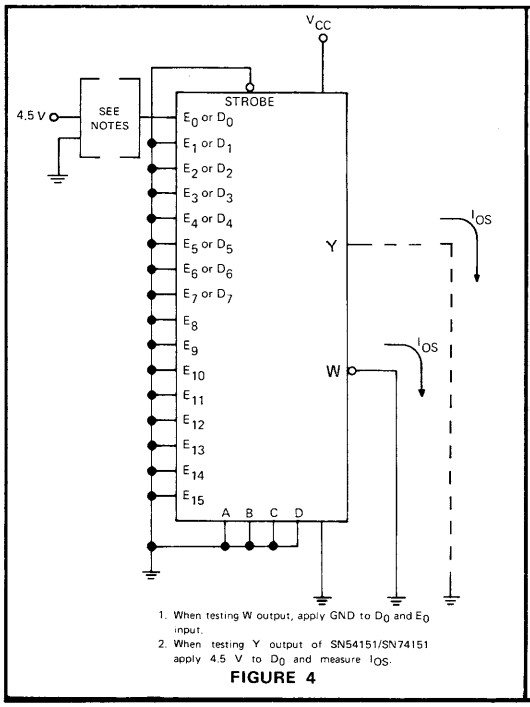


FIGURE 4

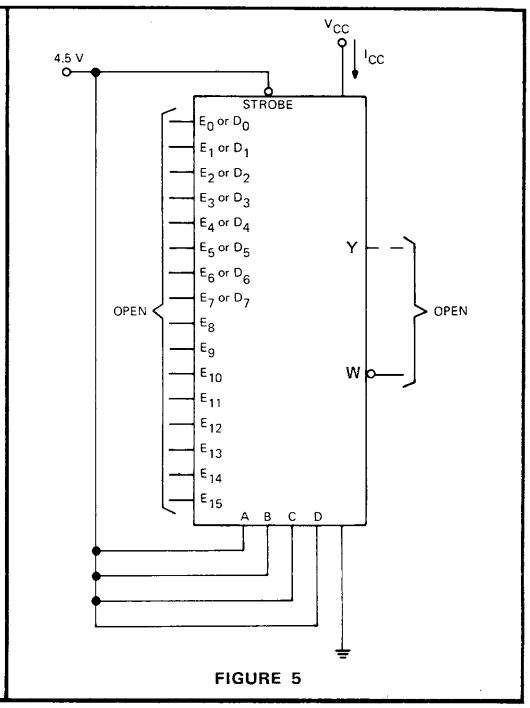


FIGURE 5

† Arrows indicate actual direction of current flow. Tests, as shown are for the SN54150/SN74150. Identical tests as applicable are performed for the SN54151/SN74151 and SN54152/SN74152.

switching characteristics†

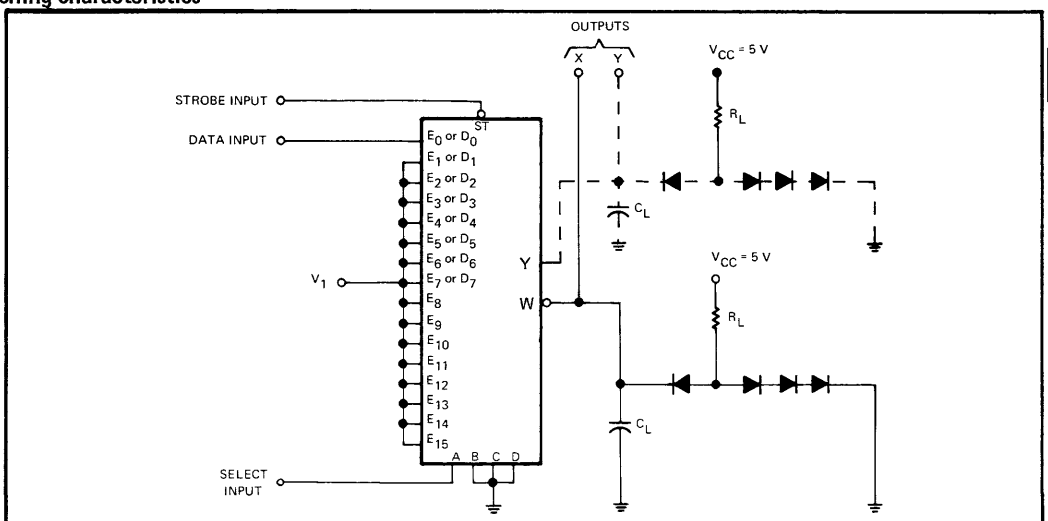


FIGURE 6–SWITCHING TIMES (SHEET 1 OF 2)

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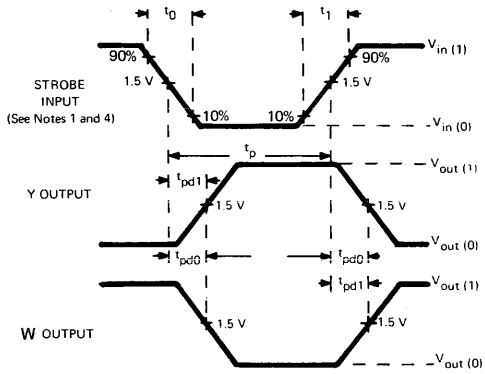
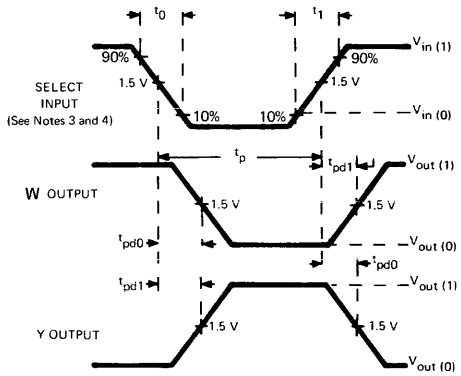
PARAMETER MEASUREMENT INFORMATION

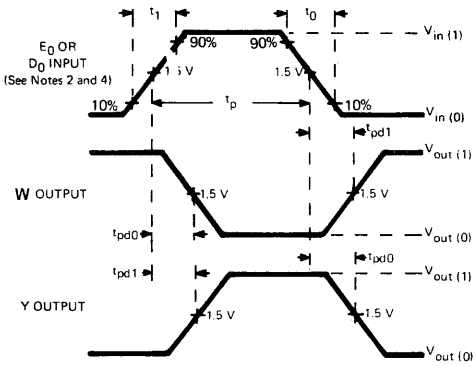
switching characteristics (continued)



STROBE-TO-OUTPUT VOLTAGE WAVEFORMS



SELECT INPUT-TO-OUTPUT VOLTAGE WAVEFORMS



DATA INPUT-TO-OUTPUT VOLTAGE WAVEFORMS

NOTES:
1. When measuring strobe-to-output times select input is at a logical 0, E_0 or D_0 is at a logical 1, V_1 = 4.5 V.
2. When measuring data input-to-output times strobe and select inputs are at a logical 0, and V_1 = 4.5 V.
3. When measuring select input-to-output times strobe input is at a logical 0, data input is at a logical 1, and V_1 = 0.
4. The input pulse has the following characteristics: $V_{in(1)}$ = 3 V, $V_{in(0)}$ = 0 V, $t_1 = t_0$ = 10 ns, PRR = 1 MHz, duty cycle = 50%, and generator $Z_{out} \approx 50\ \Omega$.
5. C_L includes probe and jig capacitance.
6. All diodes are 1N3064.

FIGURE 6–SWITCHING TIMES (SHEET 2 OF 2)

† Tests, as shown, are for the SN54150/SN74150, Identical tests as applicable are performed for the SN54151/SN74151 and SN54152/SN74152.

CIRCUIT TYPES SN54153, SN74153
DUAL 4-LINE-TO-1-LINE DATA SELECTORS/MULTIPLEXERS

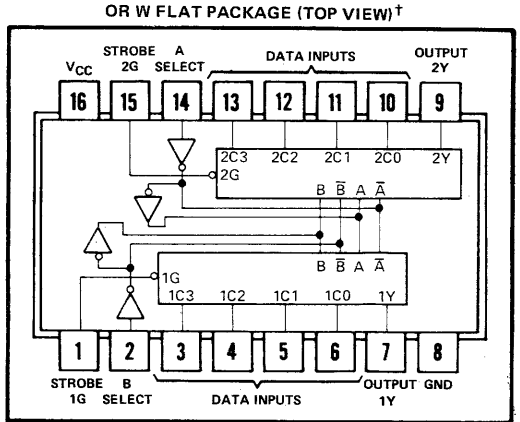
CIRCUIT TYPES SN54153, SN74153
BULLETIN NO. DL-S 7011282, FEBRUARY 1970
REVISED JANUARY 1971

- Permits Multiplexing from N lines to 1 line
- Performs Parallel-to-Serial Conversion
- Strobe (Enable) Line Provided for Cascading (N lines to n lines)
- Typical Average Propagation Delay Times:

Data Input to Output	14 ns
Strobe Input to Output	17 ns
Select Input to Output	22 ns

- High-Fan-Out, Low-Impedance, Totem-Pole Outputs
- Fully Compatible with most TTL and DTL Circuits

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



positive logic: See truth table

†Pin assigments for these circuits are the same for all packages.

description

Each of these monolithic, data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs are provided for each of the two four-line sections.

These data selectors/multiplexers are fully compatible for use with most TTL and DTL circuits. Each diode-clamped input represents only one normalized Series 54/74 load, and full fan-out to 10 normalized Series 54/74 loads is available from each of the outputs in the low-level state. A fan-out to 20 normalized Series 54/74 loads is provided in the high-level state to facilitate connection of unused inputs to used inputs. Typical power dissipation is 180 milliwatts.

TRUTH TABLE

ADDRESS INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs A and B are common to both sections.
H = high level, L = low level, X = irrelevant

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Resistor values in the OR function have been reduced to values used with Series 54H. This minimizes the capacitive effects of paralleling the phase-splitter transistors and reduces the propagation delay times. The SN54153 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74153 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Operating free-air temperature range: SN54153 Circuits	−55°C to 125°C
SN74153 Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

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recommended operating conditions

		SN54153			SN74153			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Operating free-air temperature range, T_A		−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage	1 and 2			2			V
V_{IL}	Low-level input voltage	1 and 2					0.8	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4	3.1		V
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.2	0.4	V
I_{IH}	High-level input current (each input)	3	V_{CC} = MAX, V_I = 2.4 V				40	μA
			V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IL}	Low-level input current (each input)	3	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
I_{OS}	Short-circuit output current§	4	V_{CC} = MAX	SN54153	−20		−55	mA
				SN74153	−18		−57	
I_{CCL}	Supply current, low-level output	5	V_{CC} = MAX	SN54153		36	52	mA
				SN74153		36	60	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time.

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switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Data	Y	6	C_L = 30 pF, R_L = 400 Ω		12	18	ns
t_{PHL}	Data	Y				15	23	ns
t_{PLH}	Address	Y				22	34	ns
t_{PHL}	Address	Y				22	34	ns
t_{PLH}	Strobe	Y				19	30	ns
t_{PHL}	Strobe	Y				15	23	ns

¶t_{PLH} = propagation delay time, low-to-high-level output.
t_{PHL} = propagation delay time, high-to-low-level output.

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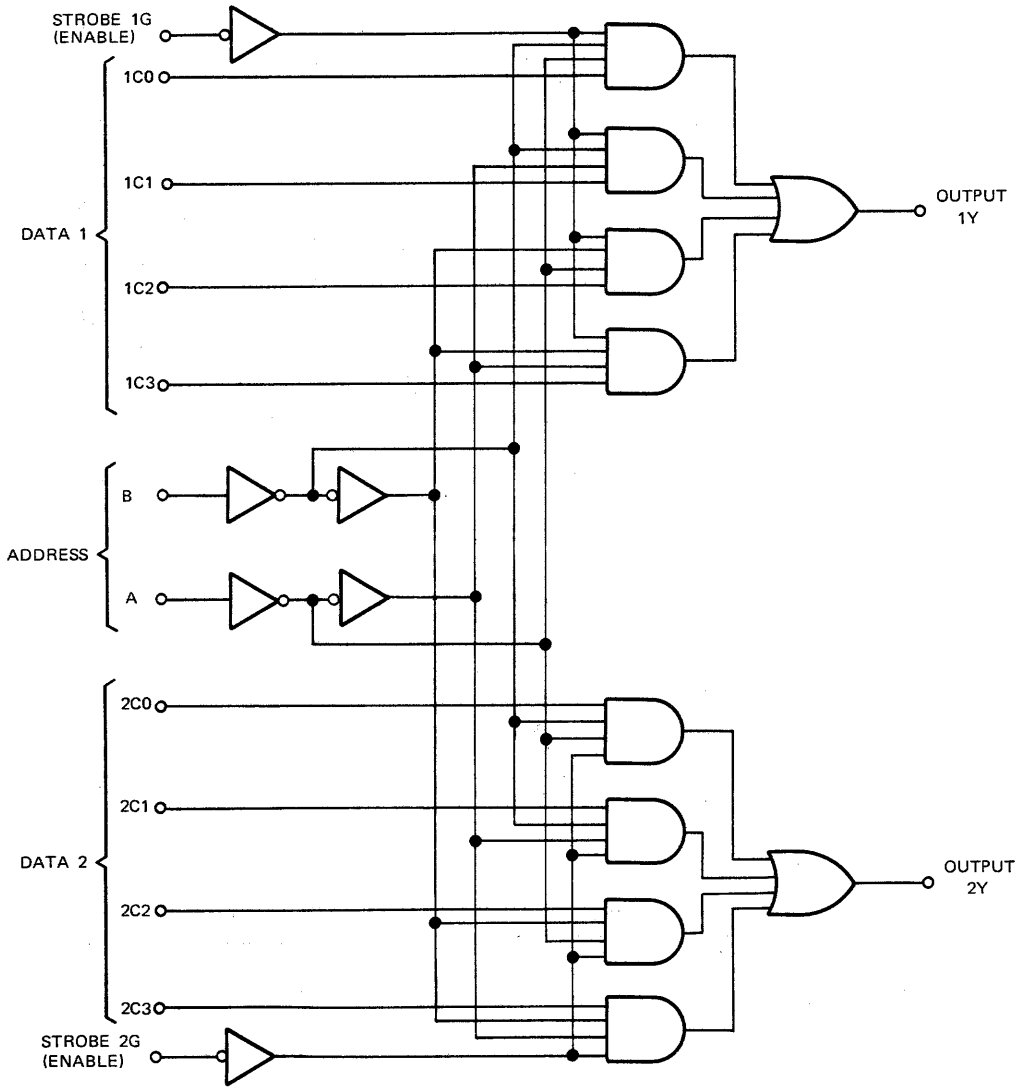
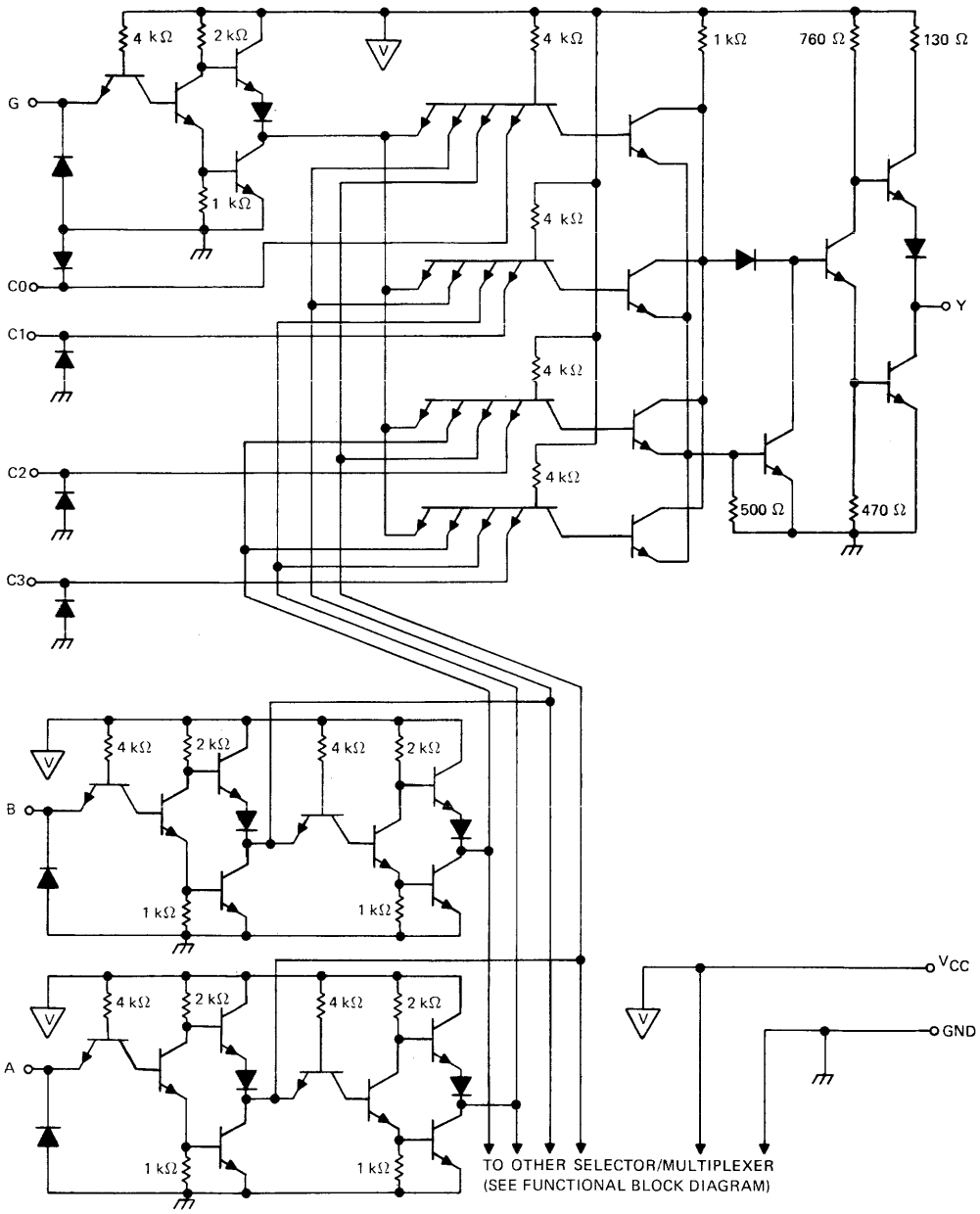
functional block diagram



9

schematic (each selector/multiplexer, and the common address section)



NOTE: Component values shown are nominal.

▽ $-V_{CC}$ bus

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PARAMETER MEASUREMENT INFORMATION

d-c test circuits†

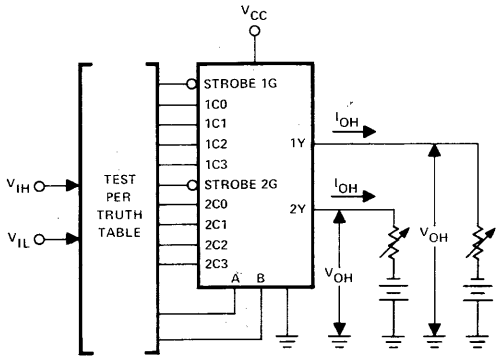


FIGURE 1–V_{IH}, V_{IL}, V_{OH}

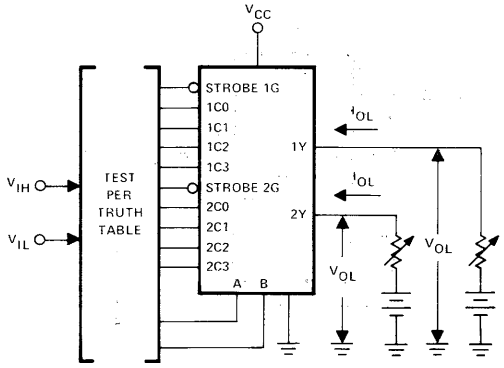
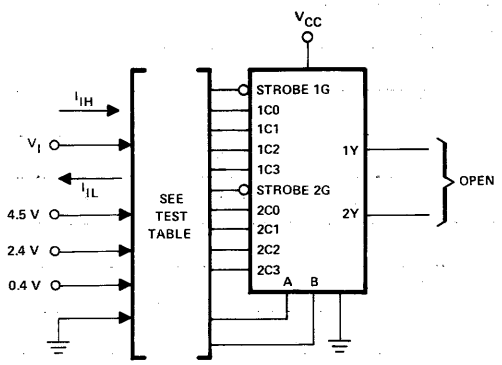


FIGURE 2–V_{IH}, V_{IL}, V_{OL}



TEST TABLE

INPUT CONDITIONS				APPLY V_I	
B	A	1G	2G	TEST I_{IL}	TEST I_{IH}
L	L	H	H		1C3, 2C3
L	H	H	H		1C2, 2C2
H	L	H	H		1C1, 2C1
H	H	H	H		A, B, 1G, 2G, 1C0, 2C0
L	L	L	L	A, B, 1G, 2G, 1C0, 2C0	
L	H	L	L	1C1, 2C1	
H	L	L	L	1C2, 2C2	
H	H	L	L	1C3, 2C3	

H = 2.4 V, L = 0.4 V

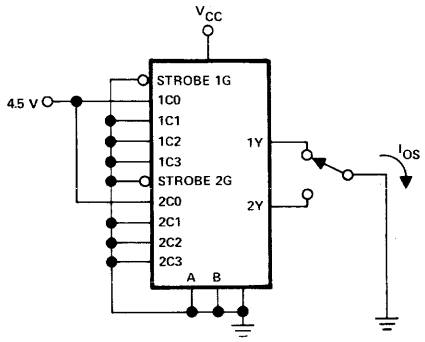
NOTE: Each input is tested separately. When I_{IH} is tested, all C inputs not under test are grounded. When I_{IL} is tested, all C inputs not under test are at 4.5 V.

FIGURE 3 –I_{IH}, I_{IL}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



NOTE: Each output is tested separately.

FIGURE 4 – I_{OS}

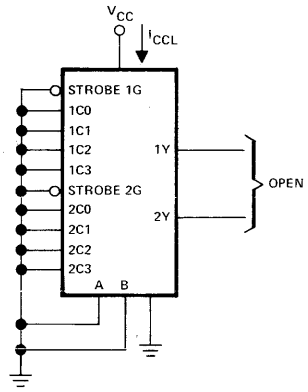


FIGURE 5 – I_{CCL}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

TEST TABLE FOR FIGURE 6

INPUTS							OUTPUT Y WAVEFORM
B	A	C0	C1	C2	C3	G	
GND	GND	INPUT	X	X	X	GND	A
GND	4.5 V	X	INPUT	X	X	GND	A
4.5 V	GND	X	X	INPUT	X	GND	A
4.5 V	4.5 V	X	X	X	INPUT	GND	A
GND	INPUT	GND	4.5 V	X	X	GND	A
INPUT	GND	GND	X	4.5 V	X	GND	A
GND	GND	4.5 V	X	X	X	INPUT	B

X = irrelevant

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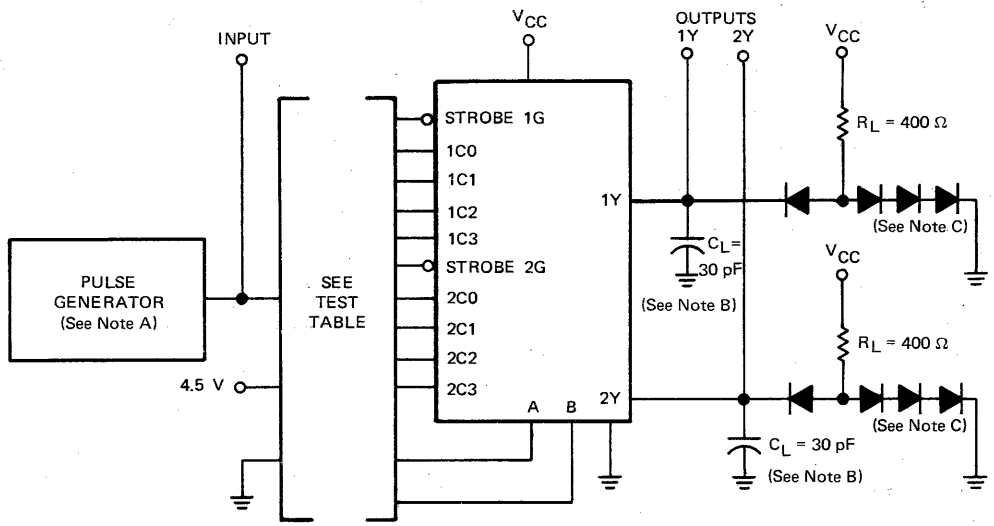
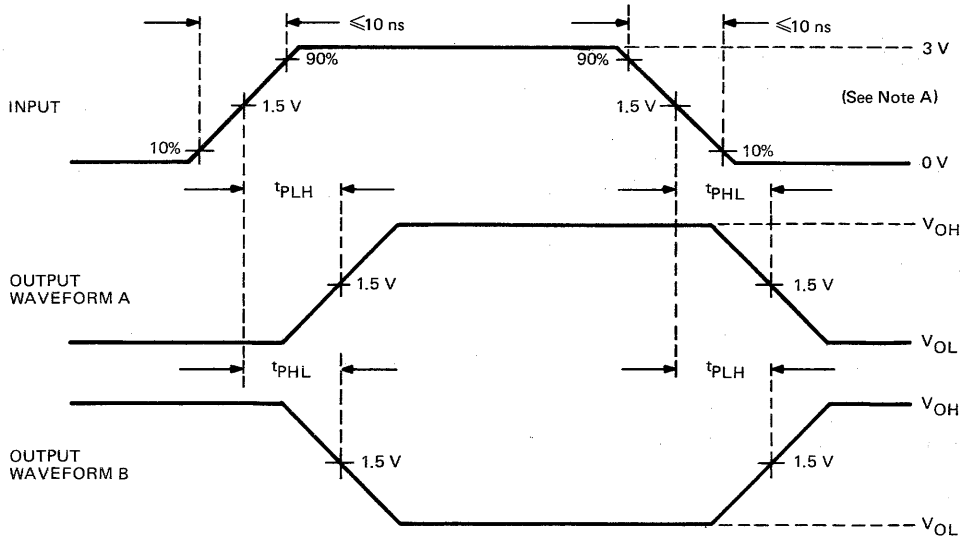
PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, duty cycle = 50%, and $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.

FIGURE 6–SWITCHING TIMES

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TEXAS INSTRUMENTS
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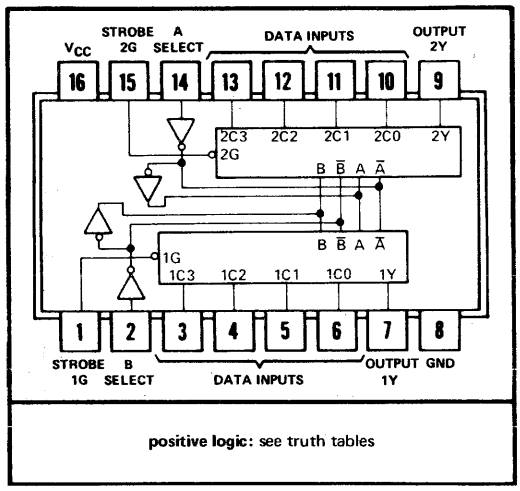
CIRCUIT TYPES SN54L153, SN74L153
DUAL 4-LINE-TO-1-LINE DATA SELECTORS/MULTIPLEXERS

- Permits Multiplexing from N lines to 1 line
- Performs Parallel-to-Serial Conversion
- Strobe (Enable) Line Provided for Cascading (N lines to n lines)
- Typical Average Propagation Delay Times:
  - Data Input to Output . . . 27 ns
  - Strobe Input to Output . . . 34 ns
  - Select Input to Output . . . 44 ns
- High-Fan-Out, Low-Impedance, Totem-Pole Outputs
- Fully Compatible with most TTL and DTL Circuits
- Low Power Dissipation . . . 90 mW Typical

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: see truth tables

description

Each of these monolithic, data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR gates. Separate strobe inputs are provided for each of the two four-line sections.

These data selectors/multiplexers are fully compatible for use with most TTL and DTL circuits. Each diode-clamped input represents only one-half of one normalized Series 54/74 load, or approximately five Series 54L/74L gate loads at a low logic level, or two Series 54L/74L gate loads at a high logic level. A fan-out to 5 normalized Series 54/74 loads in the low-level state and 10 in the high-level state is available from each output. Typical power dissipation is 90 milliwatts.

TRUTH TABLE

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.
H = high level, L = low level, X = irrelevant

Resistor values in the OR function have been reduced to minimize the capactive effects of paralleling the phase-splitter transistors and to reduce the propagation delay times. The SN54L153 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74L153 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: SN54L153 Circuits . . . . . −55°C to 125°C
SN74L153 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

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recommended operating conditions

			SN54L153			SN74L153			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}			4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	Series 54L74L gates				40			40	
	Series 54L/74L inputs with 8-kΩ base resistors¶	High logic level			20			20	
		Low logic level			10			10	
Operating free-air temperature T_A			−55		125	0		70	°C

¶ This applies for all inputs of circuit types SN54L153 and SN74L153.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage	1 and 2			2			V
V_{IL}	Low-level input voltage	1 and 2					0.8	V
V_I	Input clamp voltage	3	V_{CC} = MIN, I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −400 μA		2.4			V
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 8 mA				0.4	V
I_I	Input current at maximum input voltage	3	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current (each input)	3	V_{CC} = MAX, V_I = 2.4 V				20	μA
I_{IL}	Low-level input current (each input)	3	V_{CC} = MAX, V_I = 0.4 V				−0.8	mA
I_{OS}	Short-circuit output current§	4	V_{CC} = MAX	SN54L153	−10		−28	mA
				SN74L153	−9		−30	
I_{CCL}	Supply current, low-level output	5	V_{CC} = MAX	SN54L153			26	mA
				SN74L153		18	30	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

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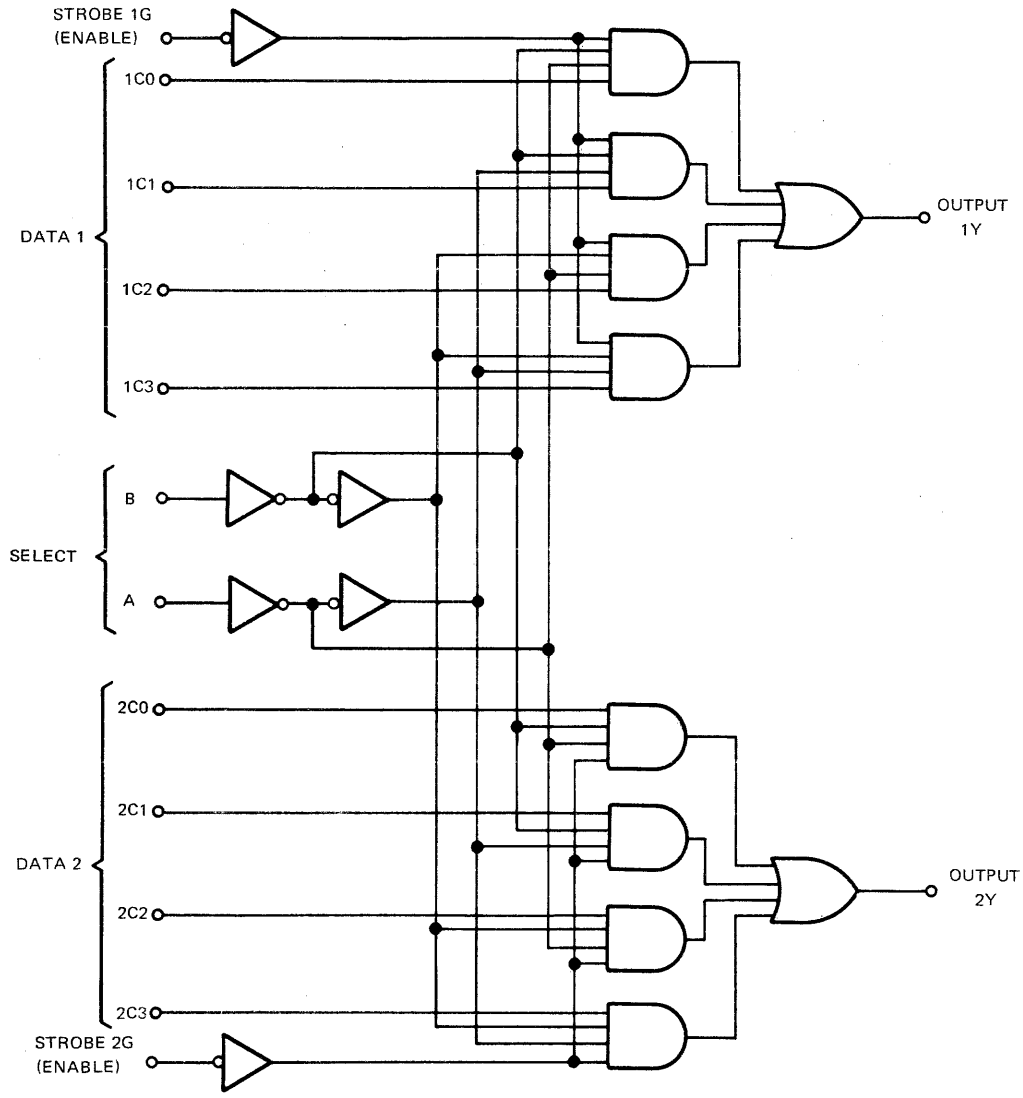
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER¶	FROM INPUT	TO OUTPUT	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Data	Y	6	C_L = 30 pF, R_L = 400 Ω		24	36	ns
t_{PHL}	Data	Y				30	46	ns
t_{PLH}	Select	Y				44	68	ns
t_{PHL}	Select	Y				44	68	ns
t_{PLH}	Strobe	Y				38	60	ns
t_{PHL}	Strobe	Y				30	46	ns

¶ t_{PLH} = propagation delay time, low-to-high-level output.
t_{PHL} = propagation delay time, high-to-low-level output.

functional block diagram



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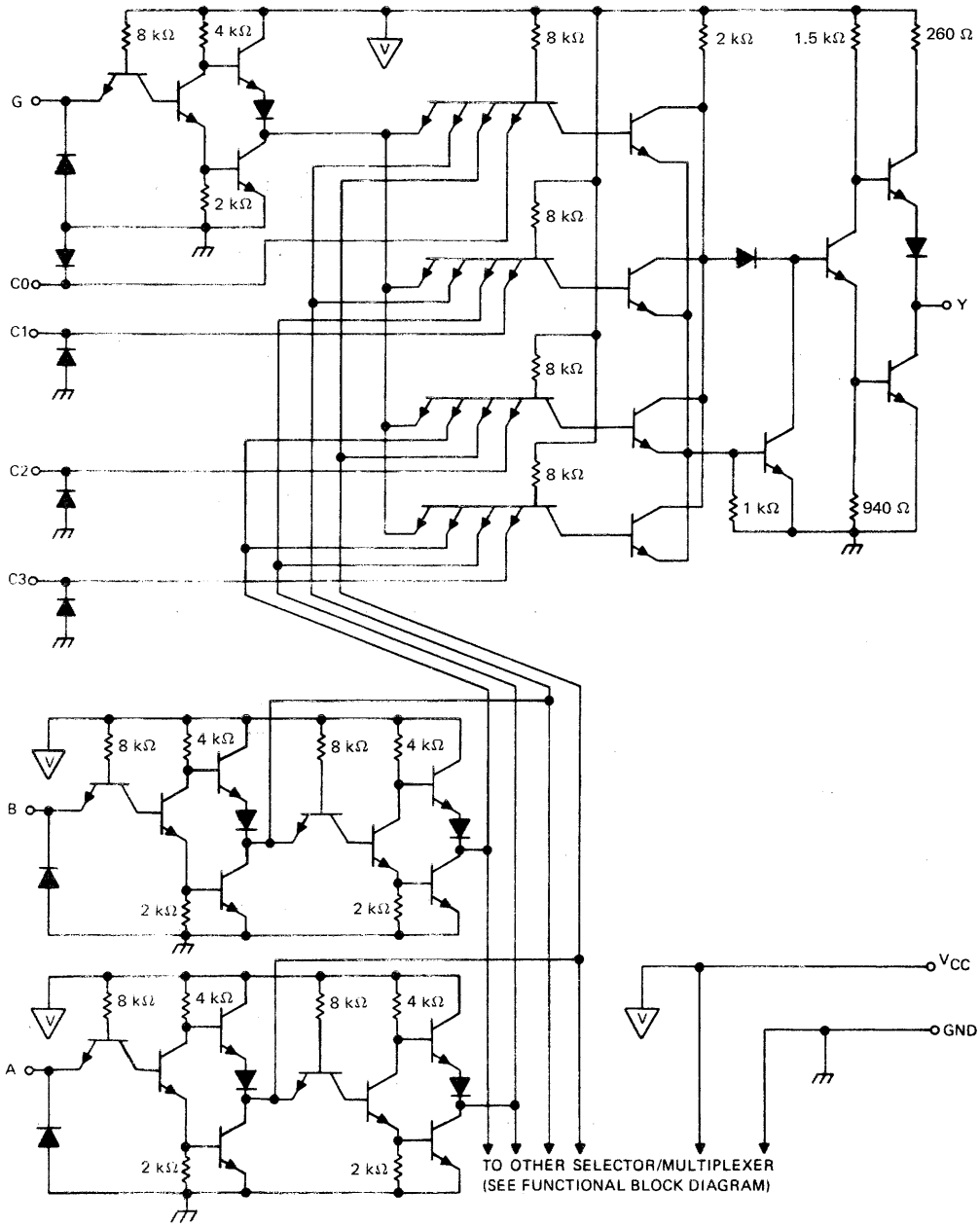
schematic (each selector/multiplexer, and the common select section)



NOTE: Component values shown are nominal.

▽ ... V_{CC} bus

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PARAMETER MEASUREMENT INFORMATION

d-c test circuits†

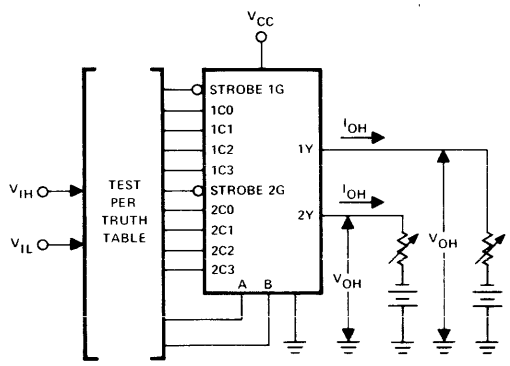


FIGURE 1–V_{IH}, V_{IL}, V_{OH}

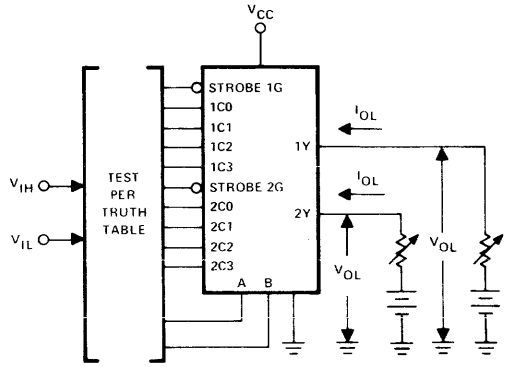
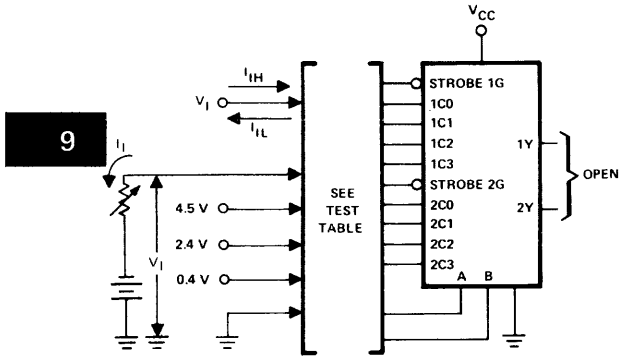


FIGURE 2–V_{IH}, V_{IL}, V_{OL}



TEST TABLE

INPUT CONDITIONS				APPLY I_I	APPLY V_I	
B	A	1G	2G	TEST V_I	TEST I_I, I_{IH}	TEST I_{IL}
L	L	H	H		1C3, 2C3	
L	H	H	H		1C2, 2C2	
H	L	H	H		1C1, 2C1	
H	H	H	H		A, B, 1G, 2G, 1C0, 2C0	
L	L	L	L	A, B, 1G, 2G, 1C0, 2C0		A, B, 1G, 2G, 1C0, 2C0
L	H	L	L	1C1, 2C1		1C1, 2C1
H	L	L	L	1C2, 2C2		1C2, 2C2
H	H	L	L	1C3, 2C3		1C3, 2C3

H = 2.4 V, L = 0.4 V

NOTE: Each input is tested separately. When I_{IH} is tested, all C inputs not under test are grounded. When I_{IL} is tested, all C inputs not under test are at 4.5 V.

FIGURE 3–V_I, I_I, I_{IH}, I_{IL}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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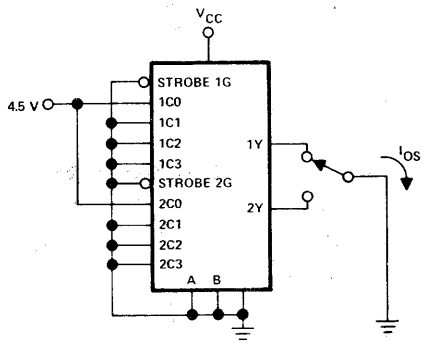
PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



NOTE: Each output is tested separately.

FIGURE 4 – I_{OS}

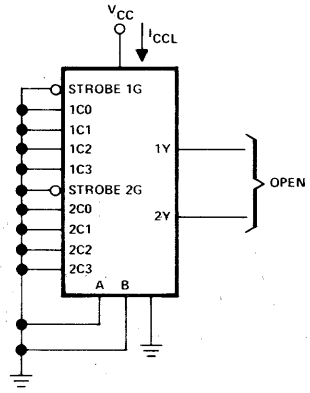


FIGURE 5 – I_{CCL}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

TEST TABLE FOR FIGURE 6

INPUTS							OUTPUT Y WAVEFORM
B	A	C0	C1	C2	C3	G	
GND	GND	INPUT	X	X	X	GND	A
GND	4.5 V	X	INPUT	X	X	GND	A
4.5 V	GND	X	X	INPUT	X	GND	A
4.5 V	4.5 V	X	X	X	INPUT	GND	A
GND	INPUT	GND	4.5 V	X	X	GND	A
INPUT	GND	GND	X	4.5 V	X	GND	A
GND	GND	4.5 V	X	X	X	INPUT	B

X = irrelevant

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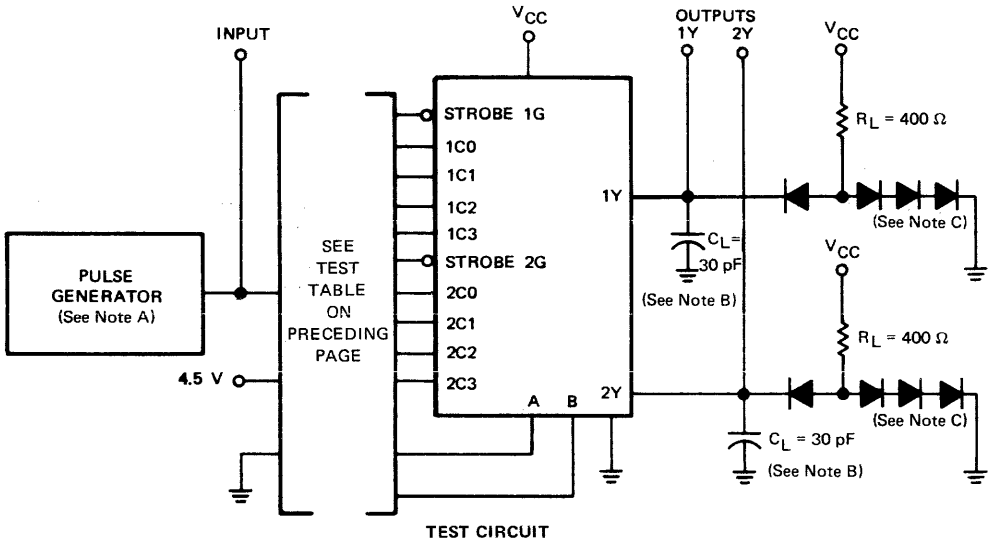
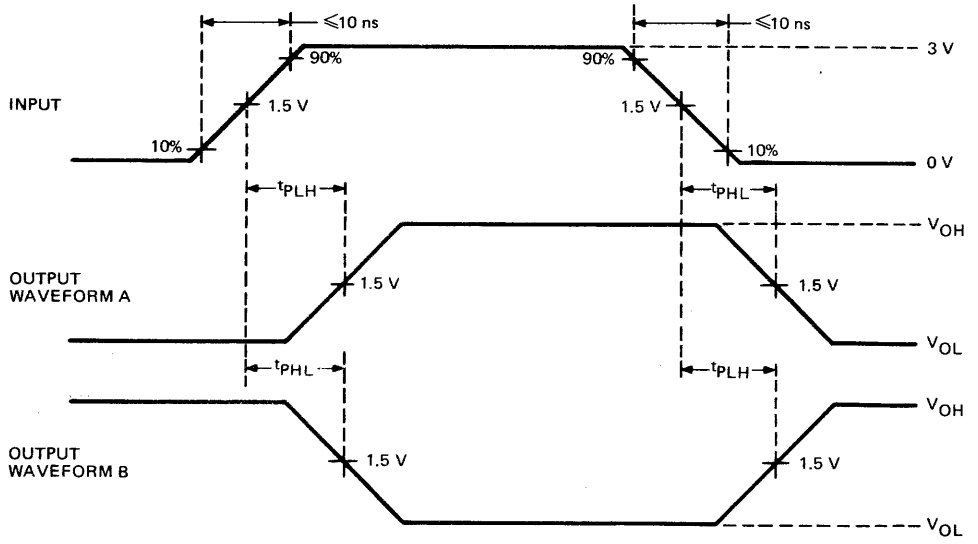
PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR≤ 1 MHz, duty cycle = 50%, and $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N914.

FIGURE 6–SWITCHING TIMES

SERIES TIDM1, TIDM2
BULLETIN NO. DL-S 7111434, JANUARY 1971

MONOLITHIC DIODE MATRICES

For Application As

- Programmable Read-Only Memories
- Alphanumeric Character Generators
- Frequency Generators
- Logic Interface Circuits

For Use In

- CRT Displays
- Minicomputers
- Peripheral Equipment
- Solid-State Memories

description

These monolithic dielectrically isolated diode matrices are fabricated using epitaxial techniques. The desired matrix patterns are programmed by selectively opening the fusible link in series with each diode. This may be done by the user by following the fusing procedure described herein, or custom-programmed matrices may be ordered by sending in a schematic diagram with circles around the diodes to be deleted. Automatic equipment at Texas Instruments can provide instantaneous code-pattern customizing of devices. Only unprogrammed matrices will be symbolized with the type numbers shown in the table below. Circuits custom-programmed to a particular pattern will be assigned a special device number by Texas Instruments, and this number will appear on the device.

Both the high-speed Series TIDM1 and medium-speed Series TIDM2 matrices are available in hermetically sealed metal flat packages (F), ceramic dual-in-line packages (J), or ceramic flat packages (W). See Section 1 for ordering instructions and outline drawings of all packages.

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absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

5 X 5 MATRICES 6 X 6 MATRICES 6 X 8 MATRICES 8 X 5 MATRICES 8 X 6 MATRICES	TIDM155 TIDM166 TIDM168 TIDM185 TIDM186	TIDM255 TIDM266 TIDM268 TIDM285 TIDM286	UNIT
Peak Reverse Voltage (See Note 1)	45	35	V
Steady-State Reverse Voltage, V_R	25		V
Peak Forward Current per Diode at (or below) 25°C Free-Air Temperature (See Note 1)	100		mA
Continuous Power Dissipation at (or below) 25°C Free-Air Temperature (See Notes 2 and 3)	400		mW
Operating Free-Air Temperature Range	−65 to 150		°C
Storage Temperature Range	−65 to 200		°C
Lead Temperature 1/16 Inch from Case for 10 Seconds	300		°C

NOTES: 1. These values apply for 100-μs pulses, duty cycle ⩽ 20%.
2. The values shown for total device apply for any combination provided the ratings of individual diodes are not exceeded.
3. Derate linearly to 150°C free-air temperature at the rate of 3.2 mW/°C.

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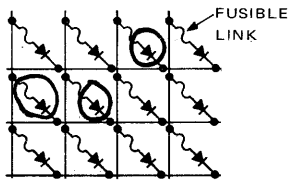
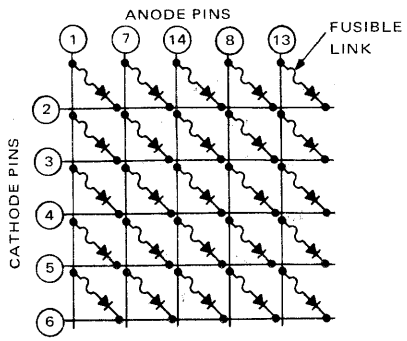
SERIES TIDM1, TIDM2
DIODE MATRICES

CUSTOMIZED CIRCUITS

To order custom programmed circuits, circle the diodes to be elimated in the appropriate schematic as shown in the example below.

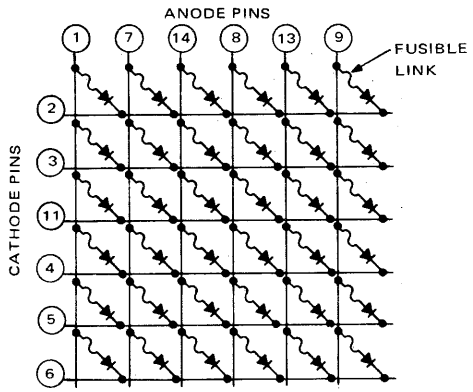


TIDM155, TIDM255 5 X 5 MATRICES



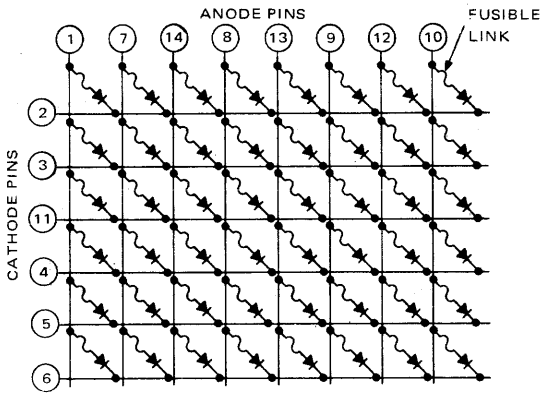
9 10 11 12 Make no external connection

TIDM166, TIDM266 6 X 6 MATRICES

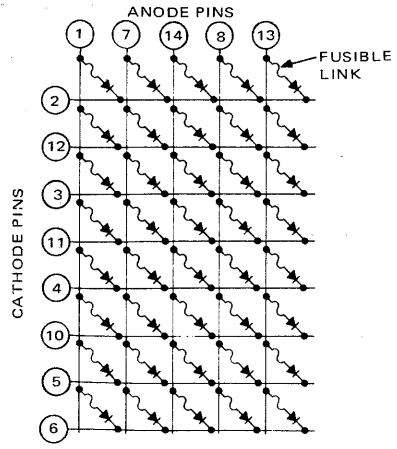


9 10 12 Make no external connection

TIDM168, TIDM268 6 X 8 MATRICES

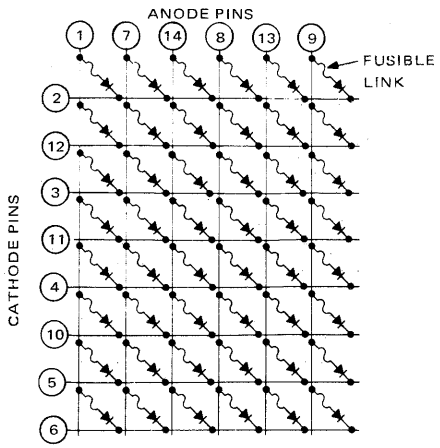


TIDM185, TIDM285 8 X 5 MATRICES



9 Make no external connection

TIDM186, TIDM286 8 X 6 MATRICES



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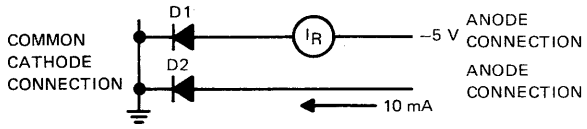
electrical characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	SERIES TIDM1			SERIES TIDM2			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{(BR)}$	Reverse Breakdown Voltage	I_R = 100 μA	45			35			V
I_R	Static Reverse Current	V_R = 25 V			20			50	nA
I_R	Static Reverse Current (with Adjacent Diode Conducting)	See Figure 1		20			50		nA
V_F	Static Forward Voltage	I_F = 1 mA			0.8			0.9	V
		I_F = 20 mA			1.5			1.7	
C_T	Total Capacitance between Any Anode Terminal and Any Cathode Terminal	V_R = 5 V, f = 1 MHz			4			4	pF

switching characteristics at 25°C free-air temperature

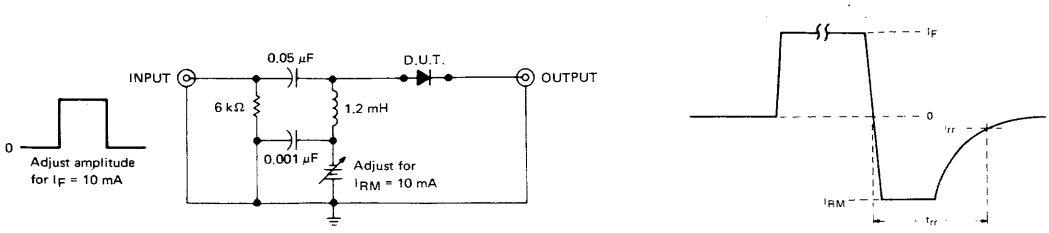
PARAMETER		TEST CONDITIONS	SERIES TIDM1			SERIES TIDM2			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{rr}	Reverse Recovery Time	I_F = 10 mA, I_{RM} = 10 mA, R_L = 100 Ω, i_{rr} = 1 mA, See Figure 2			10			25	ns

PARAMETER MEASUREMENT INFORMATION



NOTE: D1 and D2 are any two adjacent diodes with a common cathode connection.

FIGURE 1



INPUT VOLTAGE WAVEFORM | TEST CIRCUIT | OUTPUT CURRENT WAVEFORM

FIGURE 2–REVERSE RECOVERY TIME

NOTES: a. The input pulse is supplied by a generator with the following characteristics: $t_f \leq 1$ ns, Z_{out} = 50 Ω, t_w = 200 ns, duty cycle ≤ 1%.

b. The output waveform is monitored on an oscilloscope with the following characteristics: $t_r \leq 0.4$ ns, R_{in} = 50 Ω.

FUSING PROCEDURE

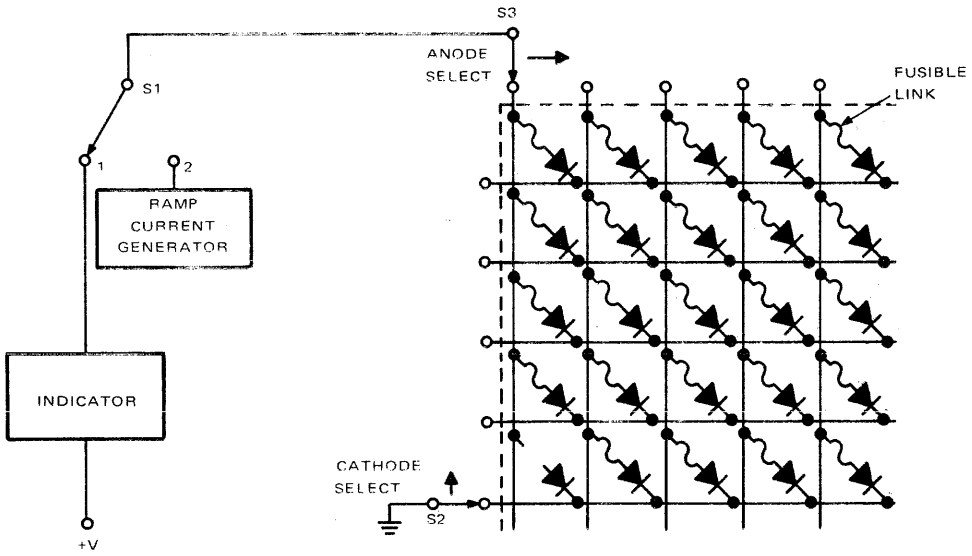


FIGURE 3

A ramp current generator provides the fusing current. The diode to be eliminated is selected by setting switches S2 and S3. When S1 is activated to position 2, current through the fusible link opens the link in series with the selected diode. The peak fusing current required to open a fusible link is approximately 750 milliamperes. Switch S1 in position 1 gives a visual indication of the condition of the selected diode before and after fusing.

TYPICAL CHARACTERISTICS

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REVERSE CURRENT
vs
FREE-AIR TEMPERATURE

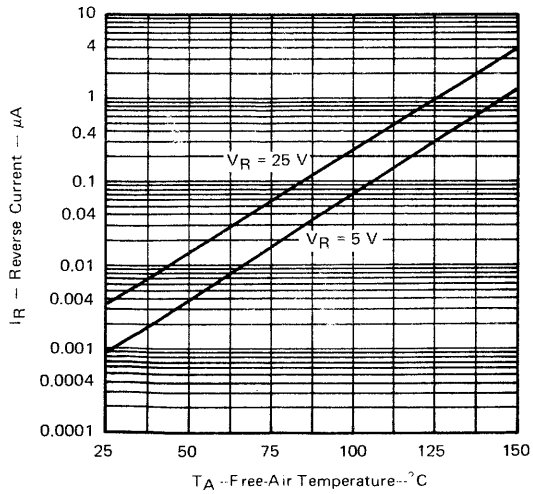

FIGURE 4

FORWARD CONDUCTION CHARACTERISTICS

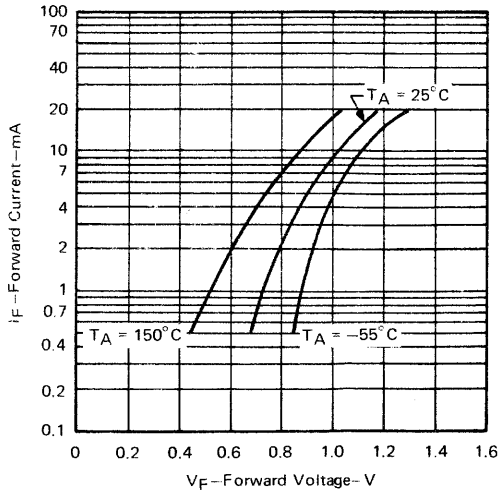

FIGURE 5

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