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for

Design Engineers

First Edition

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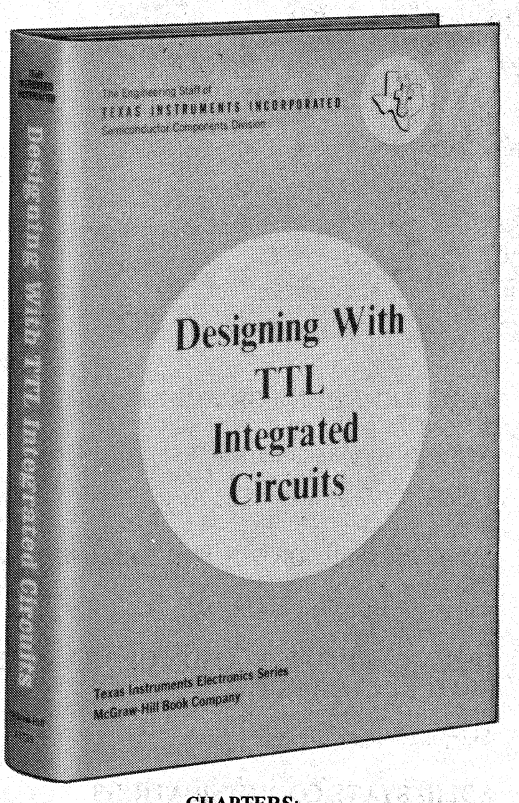

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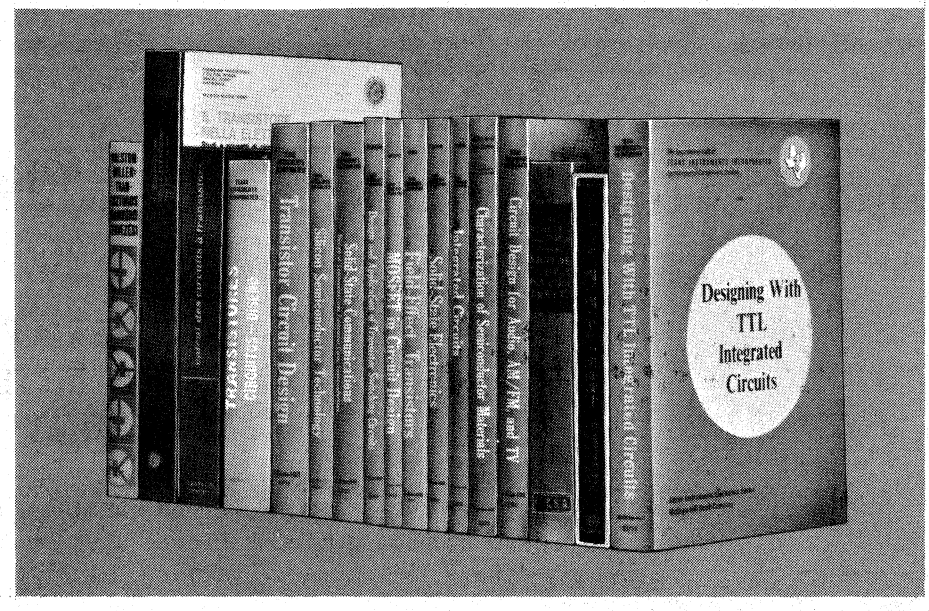

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General Information

A

THE INTEGRATED CIRCUITS CATALOG

In this 1616-page data book, Texas Instruments is pleased to present important technical information on industry's broadest line of integrated circuits.

You'll find essential design information on TTL (including Standard 54/74, low-power, high-speed, and Schottky), Linear, MOS, ECL, Hybrid, and Radiation Hardened–plus Systems Interface circuits and line summaries of DTL, High-Noise-Immunity Logic and SNF/SNG.

The indexes are designed for ease in circuit selection with margin tabs to guide you quickly to general circuit catagories, and numerical and functional indexes to help you locate specific circuits. Selection and cross-reference guides for many circuits are presented to help you identify TI's nearest equivalent to competitive circuits.

High reliability of ICs is covered in a section devoted to the MACH IV Procurement Specification in accordance with MIL STD 883 – a program initiated by TI to ensure that quality and reliability are *built* into, not *tested* into integrated circuits.

In addition to the circuits included in this catalog, TI's extensive custom capability is structured to manufacture circuits to individual customers' specification. For more information on how TI can design, build, and test circuits tailored to your specific requirements, contact your TI field sales engineer.

Although this volume offers design and specification data only for integrated circuits, we provide a listing of all TI standard discrete semiconductors and components in the section immediately following the IC indexes. The discrete listing includes a breakout by classification and application of the popular *Preferred* line of TI semiconductors and components. Complete technical data for any of these Preferred Semiconductors and Components are available from your nearest TI field sales office, local authorized TI distributor, or by writing direct to: Marketing and Information Services, Texas Instruments Incorporated, P. O. Box 5012, MS 308, Dallas, Texas. 75222.

We sincerely hope you will find The Integrated Circuits Catalog for Design Engineers a meaningful addition to your technical library. It represents fourteen years of continuing circuit innovation, refinement, and sophistication by TI engineers.

LETTER SYMBOLS, TERMS, AND DEFINITIONS FOR DIGITAL INTEGRATED CIRCUITS

The material which follows applies particularly to the following product lines: TTL, DTL, ECL, and interface circuits having TTL-compatible inputs or outputs.

When several letter symbols are shown, the first is the symbol used on the more recently issued data sheets; the symbol in parentheses was used on earlier data sheets and has the same meaning. Many of these older symbols contain a numeral one or zero which represents the binary logic level, assuming positive logic (1 = high level, 0 = low level). The newer symbols are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for national use and by the International Electrotechnical Commission (IEC) for international use.

The final section contains definitions relating to the classification of circuits by degree of complexity. The definitions for MSI and LSI have been agreed by the JEDEC Council.

VOLTAGES

V_{IH}, ($V_{in(1)}$) High-level input voltage

An input voltage level within the more positive (less negative) of the two ranges of values used to represent the binary variables. A minimum value is specified which is the least-positive (most-negative) value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{IL}, ($V_{in(0)}$) Low-level input voltage

An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables. A maximum value is specified which is the most-positive (least-negative) value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{T+} Positive-going threshold voltage

The voltage level at a transition-operated input which, as the input voltage rises from the defined low level, causes operation of the logic element according to specification.

V_{T-} Negative-going threshold voltage

The voltage level at a transition-operated input which, as the input voltage falls from the defined high level, causes operation of the logic element according to specification.

V_{OH}, ($V_{out(1)}$) High-level output voltage

The voltage at an output terminal for a specified output current I_{OH} (I_{load}) with input conditions applied which according to the product specification will establish a high level at the output.

V_{OL}, ($V_{out(0)}$) Low-level output voltage

The voltage at an output terminal for a specified output current I_{OL} (I_{sink}) with input conditions applied which according to the product specification will establish a low level at the output.

$V_{O(on)}$, (V_{on}) On-state output voltage

The voltage at an output terminal for a specified output current with input conditions applied which according to the product specification will cause the output switching element to be in the on state.

Note: This characteristic is usually specified only for outputs not having internal pull-up elements.

$V_{O(off)}$, (V_{off}) Off-state output voltage

The voltage at an output terminal for a specified output current with input conditions applied which according to the product specification will cause the output switching element to be in the off state.

Note: This characteristic is usually specified only for outputs not having internal pull-up elements.

CURRENTS

I_{IH}, ($I_{in(1)}$) High-level input current
The current flowing into* an input when a specified high-level voltage is applied to that input.

I_{IL}, ($I_{in(0)}$) Low-level input current
The current flowing into* an input when a specified low-level voltage is applied to that input.

I_{OH}, ($I_{out(1)}$) High-level output current
The current flowing into* the output with a specified high-level output voltage V_{OH} ($V_{out(1)}$) applied.

Note: This parameter is usually specified for outputs intended to drive other logic circuits.

$I_{O(off)}$, (I_{off}) Off-state output current
The current flowing into* an output with a specified output voltage applied and input conditions applied which according to the product specification will cause the output switching element to be in the off state.

Note: This parameter is usually specified for outputs intended to drive devices other than logic circuits.

I_{OS} Short-circuit output current
The current which flows into* an output when that output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potential).

I_{CCH}, ($I_{CC(1)}$), I_{EEH} etc. Supply current, high-level output
The current flowing into* the indicated supply terminal of a microcircuit when the output is (or all outputs are) at a high-level voltage.

I_{CCL}, ($I_{CC(0)}$), I_{EEL} etc. Supply current, low-level output
The current flowing into* the indicated supply terminal of a microcircuit when the output is (or all outputs are) at a low-level voltage.

DYNAMIC CHARACTERISTICS

f_{max} Maximum clock frequency (previously shown as "f_{clock}" under "switching characteristics")
The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output in accordance with the truth table or specified logic rules.

t_{TLH}, (t_1) Transition time, low-to-high-level (step or output)
The time between a specified low-level voltage and a specified high-level voltage on a waveform which is changing from the defined low level to the defined high level.

t_{THL}, (t_0) Transition time, high-to-low-level (step or output)
The time between a specified high-level voltage and a specified low-level voltage on a waveform which is changing from the defined high level to the defined low level.

t_{PLH}, ($t_{pd(1)}$) Propagation delay time, low-to-high-level output
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.

*Current flowing out of a terminal is a negative value.

DYNAMIC CHARACTERISTICS (continued)

t_{PHL}, ($t_{pd(0)}$) Propagation delay time, high-to-low-level output
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

t_w, (t_p) Average pulse width
The time between 50-percent-amplitude points (or other specified reference points) on the leading and trailing edges of a pulse.

t_{hold} Hold time
The interval immediately following the active transition of the timing pulse (usually the clock pulse) during which interval the data to be recognized must be maintained at the input to ensure its continued recognition. For a dynamic (transition-operated) input, this is the interval immediately following the transition which constitutes the dynamic input, during which interval a steady-state logic level must be maintained at the input to ensure recognition of the transition.

t_{setup} Setup time
The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) during which interval the data to be recognized must be maintained at the input (unless release is specifically permitted) to ensure its recognition. For a dynamic (transition-operated) input, this is the interval immediately preceding the transition which constitutes the dynamic input, during which interval a steady-state logic level must be maintained at the input to ensure recognition of the transition.

$t_{release}$ Release time
The interval between the release of data and the active transition of the timing pulse (usually the clock pulse), this interval being sufficiently short to ensure recognition of the released data.

Note: When specified, the interval designated "release time" falls within the setup interval and constitutes, in effect, a negative hold time.

CLASSIFICATION OF CIRCUIT COMPLEXITY

Gate equivalent circuit
A basic unit-of-measure of relative digital-circuit complexity. The number of gate equivalent circuits is that number of individual logic gates that would have to be interconnected to perform the same function.

LSI Large-scale integration
A concept whereby a complete major subsystem or system function is fabricated as a single microcircuit. In this context a major subsystem or system, whether logical or linear, is considered to be one that contains 100 or more equivalent gates or circuitry of similar complexity.

MSI Medium-scale integration
A concept whereby a complete subsystem or system function is fabricated as a single microcircuit. The subsystem or system is smaller than for LSI, but whether digital or linear, is considered to be one that contains 12 or more equivalent gates or circuitry of similar complexity.

SSI Small-scale integration
Integrated circuits of less complexity than medium-scale integration (MSI).

Typical thermal resistance values of standard integrated circuit packages are shown in the table below. The values shown do not imply any guarantee, but represent the latest and best available data. Steady-state thermal conditions are implied in the resistance measurements. Also, the following definitions apply:

$R_{\theta JC}$ – thermal resistance from junction to case using freon as a heat sink. This parameter offers good repeatability and a high degree (±5%) of correlation.

$R_{\theta JX}$ – thermal resistance from junction to still air (25°C ambient) with package in a specified socket. This parameter is highly dependent on test conditions which are difficult to reproduce accurately.

BIPOLAR PRODUCTS
TYPICAL THERMAL RESISTANCES

PACKAGE DESCRIPTION	PACKAGE DESIGNATION	°C/WATT		SOCKET USED FOR $R_{\theta JX}$ MEASUREMENT	POWER (mW)
		$R_{\theta JC}$ ±5%	$R_{\theta JX}$ ±15%		
8-Pin Plastic DIP	P	52	95	Augat	300
14- or 16-Pin Plastic DIP	N	45	90	Augat	300
24-Pin Plastic DIP	N	35	65	Barnes	500
14- or 16-Pin Ceramic DIP	J	20	70	Augat	300
14- or 16-Pin Ceramic Flat Pak (Alloy Mounted)	W, U	45	160	Barnes Carrier/ Contactor	500
14-Pin Ceramic Flat Pak (Glass Mounted)	Z	70	190	Mech-Pak Carrier	300
8- or 10-Pin Plug-In (Alloy Mounted)	L	40	120	Barnes	400
8- or 10-Pin Plug-In (Glass Mounted)	L	90	170	Barnes	700

Special test chips were used to obtain the above information.

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	−55°C to 125°C	0°C to 70°C	Dual-In-Line			Plug-In	Flat	
OPERATIONAL AMPLIFIERS								
General Purpose Operational Amplifiers	SN52702A			N		L	S	3-18
	SN52702	SN72702		N		L	S	3-18
High-Performance Operational Amplifiers	SN52101A	SN72301A	J	N	P	L	Z	3-5
	SN52107	SN72307	J	N	P	L	Z	3-9
	SN52709A			N	P	L	S	3-27
	SN52709	SN72709		N	P	L	S	3-27
	SN52741	SN72741	J	N	P	L	Z	3-34
	SN52748	SN72748	J	N	P	L	Z	3-43
	SN52770	SN72770	J	N	P	L	Z	3-47
	SN52771	SN72771	J	N	P	L	Z	3-53
Dual High-Performance Operational Amplifiers	SN52558	SN72558			P	L		3-13
	SN52747	SN72747	J	N				3-39
DIFFERENTIAL COMPARATORS								
Differential Comparators	SN52710	SN72710	J	N		L	S	3-68
	SN52810	SN72810	J	N	P	L	Z	3-79
Differential Comparators with Strobes	SN52510	SN72510	J	N	P	L	Z	3-60
Dual-Channel Differential Comparators with Strobes	SN52711	SN72711	J	N		L	S	3-72
	SN52811	SN72811	J	N		L		3-85
Dual Differential Comparators		SN72720		N				3-77
	SN52820	SN72820	J	N				3-91
Dual Differential Comparators with Strobes	SN52514	SN72514	J	N				3-66
VIDEO AMPLIFIERS								
Differential Video Amplifiers	SN52733	SN72733		N		L		3-94
	SN5510					L	F	3-101
		SN7510				L	F	3-108
	SN5511	SN7511		N		L	F	3-115
	SM5512	SM7512				L		3-121
	SN5514	SN7514				L		3-121
LINE CIRCUITS								
Dual Line Drivers	SN55109		J					3-130
		SN75109	J	N				3-130
	SN55110		J					3-130
		SN75110	J	N				3-130
Dual Line Receivers	SN55107A		J					3-130
		SN75107A	J	N				3-130
	SN55108A		J					3-130
		SN75108A	J	N				3-130
		SN75150	J	N	P			3-149
Dual Differential Line Receiver		SN75100L				L		3-126
Quadruple Line Receiver		SN75154	J	N				3-153

*For outline drawings of all packages, see Section 1.

LINEAR CIRCUITS
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FUNCTION	OPERATING TEMPERATURE RANGE		PACKAGES*					SEC.-PAGE
	−55°C to 125°C	0°C to 70°C	Dual-In-Line		Plug-In		Flat	
SENSE AMPLIFIERS								
Dual-Channel Sense Amplifiers		SN7522	J	N				3-166
		SN7523	J	N				3-166
Dual-Channel Sense Amplifiers with Complementary Outputs		SN7520	J	N				3-164
		SN7521	J	N				3-164
Dual-Channel Sense Amplifiers with Output Registers		SN7526	J	N				3-172
		SN7527	J	N				3-172
Dual Sense Amplifiers		SN7524	J	N				3-170
		SN7525	J	N				3-170
		SN75234	J	N				3-176
		SN75235	J	N				3-176
Dual Sense Amplifiers with Preamplifier Test Points		SN7528	J	N				3-174
		SN7529	J	N				3-174
		SN75238	J	N				3-178
		SN75239	J	N				3-178
MEMORY AND PERIPHERAL DRIVERS								
2 X 4 Transistor Arrays		SN75303		N			S	3-212
		SN75308	J	N				3-217
Memory Driver		SN75325						3-230
Memory Driver with Decode Inputs		SN75324						3-222
Dual Peripheral Drivers		SN75450A		N				3-247
		SN75451A			P			3-249
		SN75452		P	P			3-250
		SN75453			P			3-251
		SN75454			P			3-252
Diode Arrays	TID21A Series			N			F	3-264
VOLTAGE REGULATOR								
Voltage Regulator		SN72400		N		L		3-270
COMMUNICATIONS CIRCUITS								
Logarithmic Amplifiers	SN56502	SN76502	J	N				3-277
Balanced Mixers	SN56514	SN76514	J	N		L		3-284
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Consumer Circuits Summary								3-289
Stereo Demodulator		SN76110		N				3-290

*For outline drawings of all packages, see Section 1.

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SERIES 54S/74S CIRCUITS
FUNCTIONAL INDEX

SERIES 54S/74S
FEATURING 3-ns SPEED AND 20-mW-PER-GATE PERFORMANCE
SMALL SCALE INTEGRATION (SSI)

*For outline drawings of all packages, see Section 1.

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SERIES 54/74
FEATURING 10 ns SPEED AND 10 mW PER GATE PERFORMANCE
SMALL SCALE INTEGRATION (SSI)

FUNCTION	OPERATING TEMPERATURE RANGES		PACKAGES*			SEC.-PAGE
	−55°C to 125°C	0°C to 70°C	Dual-In-Line		Flat	
NAND/NOR/AND/OR GATES AND BUFFERS						
Quadruple 2-Input Positive NAND Gates	SN5400	SN7400	J	N	W	6-5
Quadruple 2-Input Positive NAND Gates (with Open-Collector Output)	SN5401	SN7401	J	N	W	6-6
Quadruple 2-Input Positive NOR Gates	SN5402	SN7402	J	N	W	6-9
Quadruple 2-Input Positive NAND Gates (with Open-Collector Output)	SN5403	SN7403	J	N		6-10
Hex Inverters	SN5404	SN7404	J	N	W	6-11
Hex Inverters (with Open-Collector Output)	SN5405	SN7405	J	N	W	6-12
Hex Inverter Buffers/Drivers (with Open-Collector High-Voltage Output)	SN5406	SN7406	J	N	W	6-13
Hex Buffers/Drivers (with Open-Collector High-Voltage Output)	SN5407	SN7407	J	N	W	6-15
Quadruple 2-Input Positive AND Gates	SN5408	SN7408	J	N	W	6-17
Quadruple 2-Input Positive AND Gates	SN5409	SN7409	J	N	W	6-17
Triple 3-Input Positive NAND Gates	SN5410	SN7410	J	N	W	6-20
Triple 3-Input Positive NAND Gates (with Open-Collector Output)	SN5412	SN7412	J	N	W	6-21
Dual NAND Schmitt Triggers	SN5413	SN7413	J	N	W	6-22
Hex Inverter Buffers/Drivers (with Open-Collector High-Voltage Output)	SN5416	SN7416	J	N	W	6-13
Hex Buffers/Drivers (with Open-Collector High-Voltage Output)	SN5417	SN7417	J	N	W	6-15
Dual 4-Input Positive NAND Gates	SN5420	SN7420	J	N	W	6-26
Expandable Dual 4-Input Positive NOR Gates (with Strobe)	SN5423	SN7423	J	N	W	6-27
Dual 4-Input Positive NOR Gates	SN5425	SN7425	J	N	W	6-27
Quadruple 2-Input High-Voltage Interface NAND Gates	SN5426	SN7426	J	N		6-30
Triple 3-Input Positive NOR Gates	SN5427	SN7427	J	N	W	6-32
8-Input Positive NAND Gates	SN5430	SN7430	J	N	W	6-34
Quadruple 2-Input Positive OR Gates	SN5432	SN7432	J	N	W	6-35
Quadruple 2-Input Positive NAND Buffers	SN5437	SN7437	J	N	W	6-37
Quadruple 2-Input Positive NAND Buffers (with Open-Collector Output)	SN5438	SN7438	J	N	W	6-37
Dual 4-Input Positive NAND Buffers	SN5440	SN7440	J	N	W	6-39

*For outline drawings of all packages, see Section 1.

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SERIES 54/74
FEATURING 10 ns SPEED AND 10 mW PER GATE PERFORMANCE
SMALL SCALE INTEGRATION (SSI)

FUNCTION	OPERATING TEMPERATURE RANGES		PACKAGES*			SEC.-PAGE
	–55°C to 125°C	0°C to 70°C	Dual-In-Line		Flat	
AND-OR-INVERT GATES						
Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gates	SN5450	SN7450	J	N	W	6-40
Dual 2-Wide 2-Input AND-OR-INVERT Gates	SN5451	SN7451	J	N	W	6-40
Expandable 4-Wide 2-Input AND-OR-INVERT Gates	SN5453	SN7453	J	N	W	6-42
4-Wide 2-Input AND-OR-INVERT Gates	SN5454	SN7454	J	N	W	6-42
EXPANDERS						
Dual 4-Input Expander	SN5460		J	N	W	6-44
Dual 4-Input Expander		SN7460	J	N	W	6-45
FLIP-FLOPS						
Positive Edge-Triggered J-K Flip-Flops (AND Inputs)	SN5470	SN7470	J	N	W	6-46
J-K Master-Slave Flip-Flops (AND Inputs)	SN5472	SN7472	J	N	W	6-49
Dual J-K Master-Slave Flip-Flops	SN5473	SN7473	J	N	W	6-52
Dual D-Type Edge-Triggered Flip-Flops	SN5474	SN7474	J	N	W	6-55
Dual-J-K Master-Slave Flip-Flops with Preset and Clear	SN5476	SN7476	J	N	W	6-58
Gated J-K Master-Slave Flip-Flops	SN54104	SN74104	J	N	W	6-61
Gated J-K Master-Slave Flip-Flops	SN54105	SN74105	J	N	W	6-61
Dual J-K Master-Slave Flip-Flops (V_{CC}-14, Gnd-7)	SN54107	SN74107	J	N		6-52
Gated J-K Master-Slave Flip-Flops with Data Lockout	SN54110	SN74110	J	N	W	6-66
Dual J-K Master-Slave Flip-Flops with Data Lockout	SN54111	SN74111	J	N	W	6-69
Monostable Multivibrators	SN54121	SN74121	J	N	W	6-72
Retriggerable Monostable Multivibrators with Clear	SN54122	SN74122	J	N	W	6-79
Dual Retriggerable Monostable Multivibrators with Clear	SN54123	SN74123	J	N	W	6-79

*For outline drawings of all packages, see Section 1.

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SERIES 54H/74H
FEATURING 6 ns SPEED AND 22 mW PER GATE PERFORMANCE
SMALL SCALE INTEGRATION (SSI)

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FUNCTION	OPERATING TEMPERATURE RANGE		PACKAGES*			SEC.-PAGE
	−55°C to 125°C	0°C to 70°C	Dual-In-Line		Flat	
NAND/NOR GATES						
Quadruple 2-Input Positive NAND Gates	SN54H00	SN74H00	J	N	W	7-5
Quadruple 2-Input Positive NAND Gates (with Open-Collector Output)	SN54H01	SN74H01	J	N	W	7-6
Hex Inverters	SN54H04	SN74H04	J	N	W	7-9
Hex Inverters (with Open-Collector Output)	SN54H05	SN74H05	J	N	W	7-10
Triple 3-Input Positive NAND Gates	SN54H10	SN74H10	J	N	W	7-11
Triple 3-Input Positive AND Gates	SN54H11	SN74H11	J	N	W	7-12
Dual 4-Input Positive NAND Gates	SN54H20	SN74H20	J	N	W	7-13
Dual 4-Input Positive AND Gates	SN54H21	SN74H21	J	N	W	7-14
Dual 4-Input Positive NAND Gates (with Open-Collector Output)	SN54H22	SN74H22	J	N	W	7-15
8-Input Positive NAND Gates	SN54H30	SN74H30	J	N	W	7-16
Dual 4-Input Positive NAND Buffers	SN54H40	SN74H40	J	N	W	7-17
AND-OR/AND-OR-INVERT GATES						
Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gates	SN54H50	SN74H50	J	N	W	7-18
Dual 2-Wide 2-Input AND-OR-INVERT Gates	SN54H51	SN74H51	J	N	W	7-18
Expandable 2-2-2-3-Input AND-OR Gates	SN54H52	SN74H52	J	N	W	7-20
Expandable 2-2-2-3-Input AND-OR-INVERT Gates	SN54H53	SN74H53	J	N	W	7-22
4-Wide 2-Input AND-OR-INVERT Gates	SN54H54	SN74H54	J	N	W	7-22
Expandable 2-Wide 4-Input AND-OR-INVERT Gates	SN54H55	SN74H55	J	N	W	7-24
EXPANDERS						
Dual 4-Input Expander	SN54H60		J	N	W	7-26
Dual 4-Input Expander		SN74H60	J	N	W	7-27
Triple 3-Input Expanders	SN54H61	SN74H61	J	N	W	7-28
3-2-2-3-Input AND-OR Expander	SN54H62		J	N	W	7-29
3-2-2-3-Input Expander		SN74H62	J	N	W	7-30

*For outline drawings of all packages, see Section 1.

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SERIES 54H/74H
FEATURING 6 ns SPEED AND 22 mW PER GATE PERFORMANCE
SMALL SCALE INTEGRATION (SSI)

FUNCTION	OPERATING TEMPERATURE RANGE		PACKAGES*			SEC.-PAGE
	–55°C to 125°C	0°C to 70°C	Dual-In-Line		Flat	
FLIP-FLOPS						
J-K Master-Slave Flip-Flops (AND-OR Inputs)	SN54H71	SN74H71	J	N	W	7-31
J-K Master-Slave Flip-Flops (AND Inputs)	SN54H72	SN74H72	J	N	W	7-34
Dual J-K Master-Slave Flip-Flops	SN54H73	SN74H73	J	N	W	7-37
Dual D-Type Edge-Triggered Flip-Flops	SN54H74	SN74H74	J	N	W	7-40
Dual J-K Master-Slave Flip-Flops with Preset and Clear	SN54H76	SN74H76	J	N	W	7-44
Dual J-K Master-Slave Flip-Flops (Common Clock)	SN54H78	SN74H78	J	N	W	7-47
J-K Negative Edge-Triggered Flip-Flops with AND-OR Inputs (50 MHz)	SN54H101	SN74H101	J	N	W	7-50
J-K Negative Edge-Triggered Flip-Flops with AND Inputs (50 MHz)	SN54H102	SN74H102	J	N	W	7-53
Dual J-K Negative Edge-Triggered Flip-Flops (50 MHz)	SN54H103	SN74H103	J	N	W	7-56
Dual J-K Negative Edge-Triggered Flip-Flops (50 MHz) with Preset and Clear	SN54H106	SN74H106	J	N	W	7-59
Dual J-K Negative Edge-Triggered Flip-Flops (50 MHz) (Common Clock)	SN54H108	SN74H108	J	N	W	7-62

*For outline drawings of all packages, see Section 1.

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SERIES 54L/74L
FEATURING 1 mW AND 33 ns PER GATE PERFORMANCE
SMALL SCALE INTEGRATION (SSI)

FUNCTION	OPERATING TEMPERATURE RANGE		PACKAGES*			SEC.-PAGE
	−55°C to 125°C	0°C to 70°C	Dual-In-Line		Flat	
NAND/NOR GATES						
Quadruple 2-Input Positive NAND Gates	SN54L00	SN74L00	J	N	T	8-4
Quadruple 2-Input Positive NAND Gates (with Open-Collector Output)	SN54L01	SN74L01	J	N	T	8-5
Quadruple 2-Input Positive NOR Gates	SN54L02	SN74L02	J	N	T	8-6
Quadruple 2-Input Positive NAND Gates (with Open-Collector Output)	SN54L03	SN74L03	J	N	T	8-5
Hex Inverters	SN54L04	SN74L04	J	N	T	8-9
Triple 3-Input Positive NAND Gates	SN54L10	SN74L10	J	N	T	8-10
Dual 4-Input Positive NAND Gates	SN54L20	SN74L20	J	N	T	8-11
8-Input Positive NAND Gates	SN54L30	SN74L30	J	N	T	8-12
AND-OR-INVERT GATES						
Dual 2-Wide AND-OR-INVERT Gates	SN54L51	SN74L51	J	N	T	8-13
4-Wide 3-2-2-3-Input AND-OR-INVERT Gates	SN54L54	SN74L54	J	N	T	8-14
2-Wide 4-Input AND-OR-INVERT Gates	SN54L55	SN74L55	J	N	T	8-15
FLIP-FLOPS						
R-S Master-Slave Flip-Flops	SN54L71	SN74L71	J	N	T	8-16
J-K Master-Slave Flip-Flops	SN54L72	SN74L72	J	N	T	8-19
Dual J-K Master-Slave Flip-Flops	SN54L73	SN74L73	J	N	T	8-22
Dual D-Type Edge-Triggered Flip-Flops	SN54L74	SN74L74	J	N	T	8-25
Dual J-K Master-Slave Flip-Flops (Common Clock)	SN54L78	SN74L78	J	N	T	8-28
Retriggerable Monostable Multivibrators with Clear	SN54L122	SN74L122	J	N	T	8-31

*For outline drawings of all packages, see Section 1.

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MEDIUM SCALE INTEGRATION (MSI)

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FUNCTION	OPERATING TEMPERATURE RANGE		PACKAGES*			SEC.-PAGE
	–55°C to 125°C	0°C to 70°C	Dual-In-Line		Flat	
ASYNCHRONOUS COUNTERS						
Decade Counters	SN5490	SN7490	J	N	W	9-4
Decade Counters (Low Power)	SN54L90	SN74L90	J	N	T	9-9
Divide-by-Twelve Counters	SN5492	SN7492	J	N	W	9-14
4-Bit Binary Counters	SN5493	SN7493	J	N	W	9-19
4-Bit Binary Counters (Low Power)	SN54L93	SN74L93	J	N	T	9-24
50-MHz Preset Table Decade Counters/Latches	SN54196	SN74196	J	N	W	9-29
50-MHz Preset Table 4-Bit Binary Counters/Latches	SN54197	SN74197	J	N	W	9-29
SYNCHRONOUS COUNTERS						
Synchronous 6-Bit Binary Rate Multiplier		SN7497	J	N	W	9-35
Sychronous Decade Counters	SN54160	SN74160	J	N	W	9-41
Synchronous 4-Bit Binary Counters	SN54161	SN74161	J	N	W	9-41
Fully Synchronous Decade Counters	SN54162	SN74162	J	N	W	9-41
Fully Synchronous 4-Bit Binary Counters	SN54163	SN74163	J	N	W	9-41
Synchronous Decade Decimal Rate Multiplier		SN74167	J	N	W	9-35
Synchronous Up/Down Decade Counters (Single Clock Line)	SN54190	SN74190	J	N	W	9-49
Synchronous Up/Down 4-Bit Binary Counters (Single Clock Line)	SN54191	SN74191	J	N	W	9-49
Synchronous Up/Down Decade Counters (Two Clock Lines)	SN54192	SN74192	J	N	W	9-57
Synchronous Up/Down 4-Bit Binary Counters (Two Clock Lines)	SN54193	SN74193	J	N	W	9-57
4-BIT, 5-BIT, 6-BIT SHIFT/STORAGE REGISTERS						
4-Bit Shift Registers (Parallel-In, Serial-Out)	SN5494	SN7494	J	N	W	9-58
4-Bit Universal Shift Registers (Parallel-In, Parallel-Out)	SN5495A	SN7495A	J	N	W	9-72
4-Bit Universal Shift Registers (Parallel-In, Parallel-Out) (Low Power)	SN54L95	SN74L95	J	N	T	9-79
5-Bit Shift Registers (Dual-Parallel-In, Parallel-Out)	SN5496	SN7496	J	N	W	9-86
4-Bit Data Selectors/Storage Registers (Low Power)	SN54L98	SN74L98	J	N		9-90
4-Bit Right-Shift Registers with J K and D (Low Power)	SN54L99	SN74L99	J	N		9-96
4-Bit Parallel-In, Parallel-Out Bidirectional Shift Registers	SN54194	SN74194	J	N	W	9-104
4-Bit Parallel-In, Parallel-Out Shift Register (J-K Inputs to First Stage)	SN54195	SN74195	J	N	W	9-108

*For outline drawings of all packages, see Section 1.

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FUNCTION	OPERATING TEMPERATURE RANGE		PACKAGES*			SEC.-PAGE
	–55°C to 125°C	0°C to 70°C	Dual-In-Line		Flat	
8-BIT SHIFT REGISTERS						
8-Bit Shift Registers	SN5491A	SN7491A	J	N	W	9-112
8-Bit Shift Registers (Low Power)	SN54L91	SN74L91	J	N	T	9-117
8-Bit Parallel-Out Shift Registers	SN54164	SN74164	J	N	W	9-122
8-Bit Parallel-Out Shift Registers (Low Power)	SN54L164	SN74L164	J	N	T	9-126
Parallel-Load 8-Bit Shift Registers	SN54165	SN74165	J	N	W	9-130
Parallel-Load 8-Bit Shift Registers	SN54166	SN74166	J	N	W	9-134
8-Bit Parallel-In, Parallel-Out Bidirectional Shift Registers	SN54198	SN74198	J	N	W	9-134
8-Bit Parallel-In, Parallel-Out Shift Registers (J-K Inputs to First Stage)	SN54199	SN74199	J	N	W	9-134
CODE CONVERTERS						
BCD-to-Binary Converters	SN54184	SN74184	J	N	W	9-142
Binary-to-BCD Converters	SN54185A	SN74185A	J	N	W	9-142
DECODERS/DEMULTIPLEXERS						
BCD-to-Decimal Decoders	SN5442	SN7442	J	N	W	9-148
BCD-to-Decimal Decoders (Low Power)	SN54L42	SN74L42	J	N		9-154
Excess-3-to-Decimal Decoders	SN5443	SN7443	J	N	W	9-148
Excess-3-to-Decimal Decoders (Low Power)	SN54L43	SN74L43	J	N		9-154
Excess-3-Gray-to-Decimal Decoders	SN5444	SN7444	J	N	W	9-148
Excess-3-Gray-to-Decimal Decoders (Low Power)	SN54L44	SN74L44	J	N	W	9-154
4-Line-to-16-Line (1 of 16) Decoders/Demultiplexers	SN54154	SN74154	J	N	W	9-160
Dual 2-Line-to-4-Line Decoders/Demultiplexers	SN54155	SN74155	J	N	W	9-167
Dual 2-Line-to-4-Line Decoders/Demultiplexers (with Open-Collector Output)	SN54156	SN74156	J	N	W	9-167
DECODERS/LAMP DRIVERS/BUFFERS						
BCD-to-Decimal Decoders/Drivers with 30-V Output	SN5445	SN7445	J	N	W	9-175
BCD-to-Decimal Decoders/Drivers with 15-V Output	SN54145	SN74145	J	N	W	9-175
BCD-to-Seven-Segment Decoders/Drivers with 30-V Output	SN5446A	SN7446A	J	N	W	9-181
BCD-to-Seven-Segment Decoders/Drivers with 30-V Output (Low Power)	SN54L46	SN74L46	J	N		9-198
BCD-to-Seven-Segment Decoders/Drivers with 15 V Output	SN5447A	SN7447A	J	N	W	9-181
BCD-to-Seven-Segment Decoders/Drivers with 15-V Output (Low Power)	SN54L47	SN74L47	J	N		9-198
BCD-to-Seven-Segment Decoders	SN5448	SN7448	J	N	W	9-181
BCD-to-Seven-Segment Decoders (14-pin Function)	SN5449	SN7449	J	N	W	9-181
BCD-to-Decimal Decoder/Driver		SN74141	J	N	W	9-208

*For outline drawings of all packages, see Section 1.

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MEDIUM SCALE INTEGRATION (MSI)

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FUNCTION	OPERATING TEMPERATURE RANGE		PACKAGES*			SEC.-PAGE
	−55°C to 125°C	0°C to 70°C	Dual-In-Line		Flat	
LATCHES						
Quadruple Bistable Latches	SN5475	SN7475	J	N	W	9-213
Quadruple Bistable Latches (14-pin Function)	SN5477	SN7477			W	9-213
8-Bit Bistable Latches	SN54100	SN74100	J	N	W	9-213
MEMORIES						
16-Bit Random-Access Memories (16W by 1B)	SN5481	SN7481	J	N	W	9-221
16-Bit Random-Access Memories with Gated Write Inputs (16W by 1B)	SN5484	SN7484	J	N	W	9-221
64-Bit Random-Access Memory (16W by 4B)		SN7489	J	N	W	9-230
256-Bit Read-Only Memories (32W by 8B)	SN5488A	SN7488A		N		9-235
1024-Bit Read-Only Memories (256W by 4B)	SN54187	SN74187	J	N	W	9-244
4-By-4 Register Files	SN54170	SN74170	J	N	W	9-248
ARITHMETIC ELEMENTS						
Gated Full Adders	SN5480	SN7480	J	N	W	9-255
2-Bit Binary Full Adders	SN5482	SN7482	J	N	W	9-264
4-Bit Binary Full Adders	SN5483	SN7483	J	N	W	9-271
4-Bit Binary Full Adders (Low-Power Schottky)	SN54LS83	SN74LS83	J	N		9-279
4-Bit Magnitude Comparators	SN5485	SN7485	J	N	W	9-286
4-Bit Magnitude Comparators (Low Power)	SN54L85	SN74L85	J	N		9-289
Quadruple 2-Input Exclusive-OR Gates	SN5486	SN7486	J	N	W	9-296
Quadruple 2-Input Exclusive-OR Gates (Low Power)	SN54L86	SN74L86	J	N	T	9-300
4-Bit True/Complement Zero-One Elements	SN54H87	SN54H87	J	N	W	9-304
8-Bit Odd/Even Parity Generators/Checkers	SN54180	SN74180	J	N	W	9-309
4-Bit Arithmetic Logic Unit (ALU) and Function Generators	SN54181	SN74181	J	N	W	9-315
Look-Ahead Carry Generators (for ALU)	SN54182	SN74182	J	N	W	9-326
Dual Carry-Save Full Adders	SN54H183	SN74H183	J	N	W	9-332
DATA SELECTORS/MULTIPLEXERS						
16-Bit Data Selectors/Multiplexers	SN54150	SN74150	J	N	W	9-339
8-Bit Data Selectors/Multiplexers with Strobe	SN54151	SN74151	J	N	W	9-339
8-Bit Data Selectors/Multiplexers	SN54152	SN74152			W	9-339
Dual 4-Line-to-1-Line Data Selectors/Multiplexers	SN54153	SN74153	J	N	W	9-351
Dual 4-Line-to-1-Line Data Selectors/Multiplexers (Low Power)	SN54L153	SN74L153	J	N		9-358
LOGIC DIODE MATRICES						
Series TIDM1, TIDM2 Monolithic Diode Matrices			J		F, W	9-365

*For outline drawings of all packages, see Section 1.

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FUNCTION	TYPE NO.	PACKAGE	SEC.-PAGE
LINEAR CIRCUITS			
High-Performance Operational Amplifier	RSN52709	H	10-58
Threshold Detector	RSN55909	H	10-55
Dual-Channel Switched Preamplifier	RSN55910	H	10-55
D-C Coupled 4-Channel Sense Amplifier	RSN55920	H	10-55
TL CIRCUITS			
Quadruple 2-Input Positive-NAND Gates	RSN5400	H	10-6
	RSN54H00	H	10-6
	RSN54L00	H	10-32
Hex Inverters	RSN5404	H	10-8
	RSN54H04	H	10-8
Triple 3-Input Positive-NAND Gates	RSN5410	H	10-6
	RSN54H10	H	10-6
	RSN54L10	H	10-32
Dual 4-Input Positive-NAND Gates	RSN5420	H	10-6
	RSN54H20	H	10-6
	RSN54L20	H	10-32
11-Input Positive-NAND Gates	RSN5431	H	10-6
	RSN54H31	H	10-6
Dual 4-Input Positive-NAND Buffers	RSN5440	H	10-9
	RSN54H40	H	10-9
2-Wide 3-Input, 2-Wide 2-Input, Dual AND-OR-INVERT Gates	RSN5456	H	10-10
	RSN54H56	H	10-10
3-3-2-3-Input AND-OR-INVERT Gates	RSN5457	H	10-10
	RSN54H57	H	10-10
3-3-3-2-Input AND-OR-INVERT Gate	RSN54L57	H	10-34
2-Wide 4-Input AND-OR-INVERT Gates	RSN5458	H	10-10
	RSN54H58	H	10-10
R-S Master-Slave Flip-Flop	RSN54L71	H	10-35
J-K Master-Slave Flip-Flop	RSN54L72	H	10-38
Dual D-Type Edge-Triggered Flip-Flops	RSN5474	H	10-12
	RSN54H74	H	10-12
	RSN54L74	H	10-41
Dual J-K Edge-Triggered Flip-Flop	RSN54H103	H	10-15
Dual 3-Input Positive-NAND Gate	RSN54L130	H	10-32
Dual Expandable 3-Input Positive-NAND Gate	RSN54L131	H	10-32
TL CIRCUITS			
Expandable Dual 4-Input NAND Gate	RSN15930	H	10-57
Expandable Dual 4-Input NAND Buffer Gate	RSN15932	H	10-57
Expandable Dual 4-Input NAND Power Gate	RSN15944	H	10-57
J-K/S-R Flip-Flop	RSN15945	H	10-57
Triple 3-Input NAND Gate	RSN15962	H	10-57
IODE ARRAYS			
7-Diode Array	RSN14925	H	10-57
16-Diode Array	RSN14097	H	10-57

DTL CIRCUITS
FUNCTIONAL INDEX

Function	Operating Temperature Ranges		Packages*		
	−55°C to 125°C	0°C to 75°C	Dual-In-Line		Flat
GATES WITH 6-kΩ PULL-UP RESISTORS					
Expandable Dual 4-Input NAND Gates	SN15930	SN15830	J	N	U
Quadruple 2-Input NAND Gates	SN15946	SN15846	J	N	U
Triple 3-Input NAND Gates	SN15962	SN15862	J	N	U
Dual 5-Input NAND Gates	SN151900	SN151800	J	N	U
Expandable 8-Input NAND Gates	SN151902	SN151802	J	N	U
10-Input NAND Gates	SN151904	SN151804	J	N	U
Quadruple 2-Input AND Gates	SN151906	SN151806	J	N	U
Quadruple 2-Input OR Gates	SN151908	SN151808	J	N	U
Quadruple 2-Input NOR Gates	SN151910	SN151810	J	N	U
Quadruple 2-Input Exclusive-OR Gates	SN151912	SN151812	J	N	U
GATES WITH 2-kΩ PULL-UP RESISTORS					
Quadruple 2-Input NAND Gates	SN15949	SN15849	J	N	U
Expandable Dual 4-Input NAND Gates	SN15961	SN15861	J	N	U
Triple 3-Input NAND Gates	SN15963	SN15863	J	N	U
Dual 5-Input NAND Gates	SN151901	SN151801	J	N	U
Expandable 8-Input NAND Gates	SN151903	SN151803	J	N	U
10-Input NAND Gates	SN151905	SN151805	J	N	U
Quadruple 2-Input AND Gates	SN151907	SN151807	J	N	U
Quadruple 2-Input OR Gates	SN151909	SN151809	J	N	U
Quadruple 2-Input NOR Gates	SN151911	SN151811	J	N	U
POWER/BUFFER GATES					
Expandable Dual 4-Input NAND Buffer Gates	SN15932	SN15832	J	N	U
Expandable Dual 4-Input NAND Power Gates	SN15944	SN15844	J	N	U
Quadruple 2-Input NAND Buffer Gates	SN15957	SN15857	J	N	U
Quadruple 2-Input NAND Power Gates	SN15958	SN15858	J	N	U
HEX INVERTERS					
6-kΩ Pull-Up Resistors	SN15934	SN15834	J	N	U
Expandable (Open-Base) or Translator Inputs	SN15935	SN15835	J	N	U
6-kΩ Pull-Up Resistors	SN15936	SN15836	J	N	U
2-kΩ Pull-Up Resistors	SN15937	SN15837	J	N	U
Open-Collector Outputs	SN15938	SN15838	J	N	U
EXPANDERS					
Dual 4-Input Expanders	SN15933	SN15833	J	N	U
FLIP-FLOPS					
Gated J-K/R-S (6-kΩ Pull-Up Resistors)	SN15931	SN15831	J	N	U
Gated J-K/R-S (6-kΩ Pull-Up Resistors)	SN15945	SN15845	J	N	U
Gated J-K/R-S (2-kΩ Pull-Up Resistors)	SN15948	SN15848	J	N	U
Pulse-Triggered Binary (Active Pull-Up)	SN15950	SN15850	J	N	U
Dual J-K, Individual Clocks and Presets (6-kΩ Pull-Up Resistors)	SN159093	SN158093	J	N	U
Dual J-K, Individual Clocks and Presets (2-kΩ Pull-Up Resistors)	SN159094	SN158094	J	N	U
Dual J-K, Common Clocks and Clears (2-kΩ Pull-Up Resistors)	SN159097	SN158097	J	N	U
Dual J-K, Common Clocks and Clears (6-kΩ Pull-Up Resistors)	SN159099	SN158099	J	N	U
MONOSTABLE MULTIVIBRATORS					
Gated, Negative-Edge-Triggered	SN15951	SN15851	J	N	U

*For outline drawings of all packages, see Section 1.

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FUNCTIONS	OPERATING TEMPERATURE RANGE −55°C to 125°C	FAN-OUT	OPERATING TEMPERATURE RANGE 0°C to 75°C	FAN-OUT	PACKAGES‡ Dual-In-Line		Flat
Dual 4-Input NAND Gates	SNG40 SNG41	15 7	SNG42 SNG43	12 6	J	N	U
Expandable 2-2-2-3-Input AND-OR-INVERT Gates	SNG50 SNG51	15 7	SNG52 SNG53	12 6	J	N	U
8-Input NAND Gates	SNG60 SNG61	15 7	SNG62 SNG63	12 6	J	N	U
Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gates	SNG70 SNG71	15 7	SNG72 SNG73	12 6	J	N	U
Dual Pulse Shaper/Delay AND Gates	SNG80 SNG81	15 7	SNG82 SNG83	12 6	J	N	U
2-Wide 3-Input AND-OR-INVERT Gates with 2-Input Gated Complement	SNG90 SNG91	15 7	SNG92 SNG93	12 6	J	N	U
Expandable 3-Wide 3-Input AND-OR-INVERT Gates	SNG100 SNG101	15 7	SNG102 SNG103	12 6	J	N	U
Expandable 2-Wide 4-Input AND-OR-INVERT Gates	SNG110 SNG111	15 7	SNG112 SNG113	12 6	J	N	U
Expandable 8-Input NAND Gates	SNG120 SNG121	15 7	SNG122 SNG123	12 6	J	N	U
Dual 4-Input Line Drivers	SNG130 SNG131	30 15	SNG132 SNG133	24 12	J	N	U
Quadruple 2-Input NAND Gates	SNG140 SNG141	15 7	SNG142 SNG143	12 6	J	N	U
3-2-2-3-Input Expanders for AND-OR-INVERT Gates	SNG150 SNG151		SNG152 SNG153		J	N	U
Triple 2-Input NAND Drivers	SNG160 SNG161	15 7	SNG162 SNG163	12 6	J	N	U
Dual 4-Input Expanders for AND-OR-INVERT Gates	SNG170 SNG171		SNG172 SNG173		J	N	U
Dual 4-Input Expanders for NAND Gates	SNG180 SNG181		SNG182 SNG183		J	N	U
Triple 3-Input NAND Gates	SNG190 SNG191	15 7	SNG192 SNG193	12 6	J	N	U
Expandable 8-Input NAND Gates	SNG200 SNG201	11 6	SNG202 SNG203	9 5	J	N	U
Expandable 2-Wide 4-Input AND-OR-INVERT Gates	SNG210 SNG211	11 6	SNG212 SNG213	9 5	J	N	U
Quadruple 2-Input NAND Gates	SNG220 SNG221	11 6	SNG222 SNG223	9 5	J	N	U
3-2-2-3-Input Expanders for AND-OR-INVERT Gates	SNG230 SNG231		SNG232 SNG233		J	N	U
Dual 4-Input NAND Gates	SNG240 SNG241	11 6	SNG242 SNG243	9 5	J	N	U
Expandable 2-2-2-3-Input AND-OR-INVERT Gates	SNG250 SNG251	11 6	SNG252 SNG253	9 5	J	N	U
8-Input NAND Gates	SNG260 SNG261	11 6	SNG262 SNG263	9 5	J	N	U
Dual 4-Input Expanders for AND-OR-INVERT Gates	SNG270 SNG271		SNG272 SNG273		J	N	U
OR-Expandable Dual 4-Input AND Gates	SNG280 SNG281	15 7	SNG282 SNG283	12 6	J	N	U
Dual 2-3-Input Expanders for OR Expandable AND Gates	SNG290 SNG291		SNG292 SNG293		J	N	U
Expandable 3-Wide 3-Input AND-OR-INVERT Gates	SNG300 SNG301	11 6	SNG302 SNG303	9 5	J	N	U
Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gates	SNG310 SNG311	11 6	SNG312 SNG313	9 5	J	N	U
Triple 3-Input NAND Gates	SNG320 SNG321	11 6	SNG322 SNG323	9 5	J	N	U
Quadruple 2-Input NAND Lamp/Line Drivers	SNG351	30	SNG353	24	J	N	U

MOS/LSI CIRCUITS
FUNCTIONAL INDEX

B

TEXAS INSTRUMENTS
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CROSS-REFERENCE GUIDE

(alphabetically by manufacturers)

Direct replacements were selected as pin-for-pin equivalent circuits based on similarity of electrical and mechanical characteristics as shown in currently published data. Interchangability in particular applications is not guaranteed. Before using a substitute, the user should compare the specifications of the substitute device with the detailed specifications of the original device.

B

TI makes no warranty as to the information furnished and buyer assumes all risk in the use thereof. No liability is assumed for damages resulting from the use of the information contained in this list.

LINEAR CIRCUITS

Fairchild

Type Number	Direct TI Replacement	Nearest TI Replacement	Sec.
UA702	SN52702		3
UA702C	SN72702		3
UA703		SN76603	3
UA703C	SN76603		3
UA708		SN76665	3
UA709	SN52709		3
UA709C	SN72709		3
UA709A	SN52709A		3
UA710	SN52710		3
UA710C	SN72710		3
UA710A		SN52810	3
UA711	SN52711		3
UA711C	SN72711		3
UA715		SN5511	3
UA715C		SN7511	3
UA719		SN76619	3
UA719C	SN76619		3
UA723		SN72400	3
UA723C		SN72400	3
UA729C		SN76110	3
UA730		SN5510	3
UA730C		SN7510	3
UA732C		SN76110	3
UA733	SN52733		3
UA733C	SN72733		3
UA739C	SN76131		3
UA740		SN52770	3
UA740C		SN72770	3
UA741	SN52741		3
UA741C	SN72741		3
UA746C	SN76246		3
UA747	SN52747		3
UA747C	SN72747		3
UA748	SN52748		3
UA748C	SN72748		3
UA749		SN52747	3
UA749C		SN72747	3
UA751C		SN7510	3
UA754C		SN76665	3
UA761C	SN7524		3
UA767	SN76110		3
UA796		SN56514	3
UA796C		SN76514	3
9614	SN75114		3
9615	SN75115		3
9620	SN75120		3
9621		SN75109	3
9622		SN75107	3
9624		SN75450	3
9625		SN75450	3

Motorola

Type Number	Direct TI Replacement	Nearest TI Replacement	Sec.
MC130L		SN76131	3
MC1304P	SN76104		3
MC1305P	SN76105		3
MC1306P		SN76010	3
MC1307P	SN76110		3
MC1316P		SN76003	3
MC1325P		SN76246	3
MC1326P		SN76246	3
MC1328P	SN76246		3
MC1330P	SN76530		3
MC1350P	SN76600		3
MC1351P		SN76665	3
MC1352P	SN76650		3
MC1357	SN76642		3
MC1410	SN7510		3
MC1414L	SN72514		3
MC1429G		SN7511	3
MC1430		SN72702	3
MC1431		SN72702	3
MC1433		SN72709	3
MC1439		SN72748	3
MC1440		SN7524	3
MC1441		SN7520	3
MC1454G		SN76010	3
MC1455G	SN72771		3
MC1458	SN72558		3
MC1460		SN72400	3
MC1461		SN72400	3
MC1488L		SN75150	3
MC1489L		SN75154	3
MC1509		SN5510	3
MC1510	SN5510		3
MC1514L	SN52514		3
MC1520		SN5511	3
MC1524G		SN76010	3
MC1525G		SN52733	3
MC1526G		SN52733	3
MC1529G		SN5511	3
MC1530		SN52702	3
MC1531		SN52702	3
MC1533		SN52709	3
MC1539		SN52748	3
MC1540		SN5524	3
MC1541		SN5520	3

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Motorola, Cont.

Type Number	Direct TI Replacement	Nearest TI Replacement	Sec.
MC1552G		SN52733	3
MC1553G		SN52733	3
MC1554G		SN76010	3
MC1556G	SN52771		3
MC1558	SN52558		3
MC1560		SN72400	3
MC1561		SN72400	3
MC1580L		SN55107-110	3
MC1582L		SN55109-110	3
MC1583L		SN55108	3
MC1584L		SN55107	3
MC1590G	SN76600		3
MC1596G		SN56514L	3
MC1709	SN52709		3
MC1709C	SN72709		3
MC1710	SN52710		3
MC1710C	SN72710		3
MC1711	SN52711		3
MC1711C	SN72711		3
MC1712	SN52702		3
MC1712C	SN72702		3
MC1723		SN72400	3
MC1741	SN52741		3
MC1741C	SN72741		3
MC7520	SN7520		3
MC7521	SN7521		3
MC7524	SN7524		3
MC7525	SN7525		3
MCH1439G		SN72741	3
MCH1539G		SN52741	3
MFC4000P		SN76010	3
MFC4010P		SN7514	3
MFC6000		SN76010	3
MFC6010		SN76641	3
MFC8000P		SN76131	3
MFC8001P		SN76131	3
MFC8002P		SN76131	3
MFC8010		SN76010	3
MFC9000		SN76005	3
MFC9010		SN76005	3

National

Type Number	Direct TI Replacement	Nearest TI Replacement	Sec.
LH101	SN52741		3
LM101	SN52748		3
LM101A	SN52101A		3
LM106	SN52106		3
LM107	SN52107		3
LM108		SN52770	3
LM111		SN52810	3
LM112		SN52771	3
LH201	SN52741		3
LM201	SN52748		3
LM201A	SN52101A		3
LM205		SN72400	3
LM206	SN52106		3
LM207	SN52107		3
LM208		SN52770	3
LM211		SN52810	3
LM212		SN52771	3
LM301A	SN72301A		3
LM305		SN72400	3
LM305A		SN72400	3
LM306	SN72306		3
LM307	SN72307		3
LM308		SN72770	3
LM311		SN72810	3
LM312		SN72771	3
LM1304	SN76104		3
LM1458	SN72558		3
LM1558	SN52558		3
LM3065	SN76665		3
LM709	SN52709		3
LM709A	SN52709A		3
LM709C	SN72709		3
LM709CN	SN72709N		3
LM710	SN52710		3
LM710A		SN52810	3
LM710C	SN72710		3
LM710CN	SN72710N		3
LM711	SN52711		3
LM711C	SN72711		3
LM711CN	SN72711N		3
LM723		SN72400	3
LM723C		SN72400	3
LM741	SN52741		3
LM741C	SN72741		3
LM741CN	SN72741N		3
LM747	SN52747		3
LM747D	SN52747J		3
LM747C	SN72747		3
LM747CD	SN72747J		3
LM747CN	SN72747N		3
LM748	SN52748		3
LM748C	SN72748		3
LM5520D	SN5520J		3
LM5521D	SN5521J		3
LM5522D	SN5522J		3
LM5523D	SN5523J		3
LM5524D	SN5524J		3
LM5525D	SN5525J		3
LM5528D	SN5528J		3
LM5529D	SN5529J		3
LM7520D	SN7520J		3
LM7520N	SN7520N		3
LM7521D	SN7521J		3
LM7521N	SN7521N		3
LM7522D	SN7522J		3
LM7522N	SN7522N		3
LM7523D	SN7523J		3
LM7523N	SN7523N		3
LM7524D	SN7524J		3
LM7524N	SN7524N		3
LM7525D	SN7525J		3
LM7525N	SN7525N		3
LM7528D	SN7528J		3
LM7528N	SN7528N		3

LINEAR CIRCUITS

National, Cont.

Type Number	Direct TI Replacement	Nearest TI Replacement	Sec.
LM7529D	SN7529J		3
LM7529N	SN7529N		3
LM7534	SN75234		3
LM7535	SN75235		3
LM7538	SN75238		3
LM7539	SN75239		3
DM7800		SN75450	3
DM7820		SN55115	3
DM7830		SN55114	3
DM8800		SN75450	3
DM8820		SN75115	3
DM8822		SN75154	3
DM8830		SN75114	3
DM8831		SN75113	3
DM8832		SN75150	3
NH0002	HIC037		15
NH0006		SN75451	3
NH0006C		SN75451L	3
NH0006CN		SN75451P	3
NH0008		HIC040	15
NH0008C		HIC040	15
NH0008CN		HIC040	15
NH0011		SN75451	3
NH0011C		SN75451	3
NH0011CN		SN75451	3
NH0016CN		SN75451	3
NH0017CN		HIC040	15
NH0018CN		HIC040	15

Signetics

Type Number	Direct TI Replacement	Nearest TI Replacement	Sec.
N5101A	SN72748N		3
N5101T	SN72748L		3
N5101V	SN72748P		3
N5111A	SN76643		3
N5556T	SN72771L		3
N5556V	SN72771P		3
N5558T	SN72558L		3
N5558V	SN72558P		3
N5596A		SN76514N	3
N5709A	SN72709N		3
N5709T	SN72709L		3
N5710A	SN72710N		3
N5710T	SN72710L		3
N5711A	SN72711N		3
N5711T	SN72711L		3
N5723A		SN72400N	3
N5723L		SN72400N	3
N5733A	SN72733N		3
N5733K	SN72733L		3
N5741A	SN72741N		3
N5741T	SN72741L		3
N5741V	SN72741P		3
N5748A	SN72748N		3
N5748T	SN72748L		3
N5748V	SN72748P		3
N7520B	SN7520N		3
N7521B	SN7521N		3
N7522B	SN7522N		3
N7523B	SN7523N		3
N7524B	SN7524N		3
N7525B	SN7525N		3
S5101T	SN52748L		3
S5556T	SN52771L		3
S5558T	SN52558L		3
S5596T		SN56514L	3
S5709T	SN52709L		3
S5710T	SN52710L		3
S5711T	SN52711L		3
S5723L		SN72400N	3
S5733K	SN52733L		3
S5741T	SN52741L		3
S5748T	SN52748L		3
NE501		SN7511	3
NE510		SN76600	3
NE511B		SN76600	3
NE515		SN7511	3
NE516		SN7511	3
NE518		SN75107	3
NE525		SN7524	3
NE526		SN75107	3
NE550L		SN72400N	3
SE501		SN5511	3
SE510		SN76600	3
SE511B		SN76600	3
SE515		SN5511	3
SE516		SN5511	3
SE518		SN55107	3
SE526		SN55107	3
SE550L		SN72400N	3
8T15		SN75150	3
8T16		SN75154	3

TEXAS INSTRUMENTS
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DTL/TTL CIRCUITS

Fairchild DTL

Type Number	Direct Replacement	Recommended for New Designs	Sec.
U3I909351X	SN159093U	SN5473W	6
U3I909359X	SN158093U	SN7473W	6
U3I909451X	SN159094U	SN5473W	6
U3I909459X	SN158094U	SN7473W	6
U3I909751X	SN159097U	SN5476W	6
U3I909759X	SN158097U	SN7476W	6
U3I909951X	SN159099U	SN5476W	6
U3I909959X	SN158099U	SN7476W	6
U3I993051X	SN15930U	SN5420W	6
U3I993059X	SN15830U	SN7420W	6
U3I993151X	SN15931U	SN54110W	6
U3I993159X	SN15831U	SN74110W	6
U3I993251X	SN15932U	SN5440W	6
U3I993259X	SN15832U	SN7440W	6
U3I993351X	SN15933U	SN5460W	6
U3I993359X	SN15833U	SN7460W	6
U3I993551X	SN15935U	SN5405W	6
U3I993559X	SN15835U	SN7405W	6
U3I993651X	SN15936U	SN5405W	6
U3I993659X	SN15836U	SN7405W	6
U3I993751X	SN15937U	SN5405W	6
U3I993759X	SN15837U	SN7405W	6
U3I994451X	SN15944U	SN5440W	6
U3I994459X	SN15844U	SN7440W	6
U3I994551X	SN15945U	SN54110W	6
U3I994559X	SN15845U	SN74110W	6
U3I994651X	SN15946U	SN5400W	6
U3I994659X	SN15846U	SN7400W	6
U3I994851X	SN15948U	SN54110W	6
U3I994859X	SN15848U	SN74110W	6
U3I994951X	SN15949U	SN5400W	6
U3I994959X	SN15849U	SN7400W	6
U3I995051X	SN15950U	SN54H101W	7
U3I995059X	SN15850U	SN74H101W	7
U3I995151X	SN15951U	SN54121W	6
U3I995159X	SN15851U	SN74121W	6
U3I996151X	SN15961U	SN5420W	6
U3I996159X	SN15861U	SN7420W	6
U3I996251X	SN15962U	SN5410W	6
U3I996259X	SN15862U	SN7410W	6
U3I996351X	SN15963U	SN5410W	6
U3I996359X	SN15863U	SN7410W	6

Type Number	Direct Replacement	Recommended for New Designs	Sec.
U6A909351X	SN159093J, N	SN5473J, N	6
U6A909359X	SN158093J, N	SN7473J, N	6
U6A909451X	SN159094J, N	SN5473J, N	6
U6A909459X	SN158094J, N	SN7473J, N	6
U6A909751X	SN159097J, N	SN5476J, N	6
U6A909759X	SN158097J, N	SN7476J, N	6
U6A909951X	SN159099J, N	SN5476J, N	6
U6A909959X	SN158099J, N	SN7476J, N	6
U6A993051X	SN15930J, N	SN5420J, N	6
U6A993059X	SN15830J, N	SN7420J, N	6
U6A993151X	SN15931J, N	SN54110J, N	6
U6A993159X	SN15831J, N	SN74110J, N	6
U6A993251X	SN15932J, N	SN5440J, N	6
U6A993259X	SN15832J, N	SN7440J, N	6
U6A993351X	SN15933J, N	SN5460J, N	6
U6A993359X	SN15833J, N	SN7460J, N	6
U6A993551X	SN15935J, N	SN5405J, N	6
U6A993559X	SN15835J, N	SN7405J, N	6
U6A993651X	SN15936J, N	SN5405J, N	6
U6A993659X	SN15836J, N	SN7405J, N	6
U6A993751X	SN15937J, N	SN5405J, N	6
U6A993759X	SN15837J, N	SN7405J, N	6
U6A994451X	SN15944J, N	SN5440J, N	6
U6A994459X	SN15844J, N	SN7440J, N	6
U6A994551X	SN15945J, N	SN54110J, N	6
U6A994559X	SN15845J, N	SN74110J, N	6
U6A994651X	SN15946J, N	SN5400J, N	6
U6A994659X	SN15846J, N	SN7400J, N	6
U6A994851X	SN15948J, N	SN54110J, N	6
U6A994859X	SN15848J, N	SN74110J, N	6
U6A994951X	SN15949J, N	SN5400J, N	6
U6A994959X	SN15849J, N	SN7400J, N	6
U6A995051X	SN15950J, N	SN54H101J, N	7
U6A995059X	SN15850J, N	SN74H101J, N	7
U6A995151X	SN15951J, N	SN54121J, N	6
U6A995159X	SN15851J, N	SN74121J, N	6
U6A996151X	SN15961J, N	SN5420J, N	6
U6A996159X	SN15861J, N	SN7420J, N	6
U6A996251X	SN15962J, N	SN5410J, N	6
U6A996259X	SN15862J, N	SN7410J, N	6
U6A996351X	SN15963J, N	SN5410J, N	6
U6A996359X	SN15863J, N	SN7410J, N	6

Fairchild TTL

Type Number	Direct Replacement	Recommended for New Designs	Sec.
A3I9033512	SN5481W	SN5489W	9
A3I9033591	SN7481W	SN7489W	9
A3I9033592	SN7481W	SN7489W	9
A4L410359X	SN7489W	SN7489W	9
A6A9033512	SN5481W	SN5489W	9
A6A9033591	SN7481W	SN7489W	9
A6A9033592	SN7481W	SN7489W	9
A7B410359X	SN7489J, N	SN7489J, N	9
A7B9034A1B	SN5488AW	SN5488AW	9
A7B9034A9B	SN7488AW	SN7488AW	9
U3I540051X	SN5400W	SN5400W	6
U3I540151X	SN5401W	SN5401W	6
U3I540251X	SN5402W	SN5402W	6
U3I540451X	SN5404W	SN5404W	6
U3I540551X	SN5405W	SN5405W	6

Type Number	Direct Replacement	Recommended For New Designs	Sec.
U3I540851X	SN5408W	SN5408W	6
U3I5410451X	SN54104W	SN54104W	6
U3I541051X	SN5410W	SN5410W	6
U3I5410551X	SN54105W	SN54105W	6
U3I542051X	SN5420W	SN5420W	6
U3I543051X	SN5430W	SN5430W	6
U3I544051X	SN5440W	SN5440W	6
U3I544951X	SN5449W	SN5449W	9
U3I545051X	SN5450W	SN5450W	6
U3I545151X	SN5451W	SN5451W	6
U3I545351X	SN5453W	SN5453W	6
U3I545451X	SN5454W	SN5454W	6
U3I546051X	SN5460W	SN5460W	6
U3I547051X	SN5470W	SN5470W	6
U3I547251X	SN5472W	SN5472W	6

Fairchild TTL, Cont.

Type Number	Direct Replacement	Recommended for New Designs	Sec.
U3I547351X	SN5473W	SN5473W	6
U3I547451X	SN5474W	SN5474W	6
U3I547751X	SN5477W	SN5477W	9
U3I548051X	SN5480W	SN5480W	9
U31548251X	SN5482W	SN5482W	9
U31548651X	SN5486W	SN5486W	9
U3I549051X	SN5490W	SN5490W	9
U3I549151X	SN5491AW	SN5491AW	9
U3I549251X	SN5492W	SN5492W	9
U3I549351X	SN5493W	SN5493W	9
U3I549551X	SN5495AW	SN5495AW	9
U3I740059X	SN7400W	SN7400W	6
U3I740159X	SN7401W	SN7401W	6
U3I740459X	SN7404W	SN7404W	6
U3I740559X	SN7405W	SN7405W	6
U3I740859X	SN7408W	SN7408W	6
U3I7410459X	SN74104W	SN74104W	6
U3I7410559X	SN74105W	SN74105W	6
U3I741059X	SN7410W	SN7410W	6
U3I742059X	SN7420W	SN7420W	6
U3I743059X	SN7430W	SN7430W	6
U3I744059X	SN7440W	SN7440W	6
U3I744959X	SN7449W	SN7449W	9
U3I745059X	SN7450W	SN7450W	6
U3I745159X	SN7451W	SN7451W	6
U3I745359X	SN7453W	SN7453W	6
U3I745459X	SN7454W	SN7454W	6
U3I746059X	SN7460W	SN7460W	6
U3I747059X	SN7470W	SN7470W	6
U3I747259X	SN7472W	SN7472W	6
U3I747359X	SN7473W	SN7473W	6
U3I747459X	SN7474W	SN7474W	6
U3I747759X	SN7477W	SN7477W	9
U3I748059X	SN7480W	SN7480W	9
U31748259X	SN7482W	SN7482W	9
U3I748659X	SN7486W	SN7486W	9
U3I749059X	SN7490W	SN7490W	9
U3I749159X	SN7491AW	SN7491AW	9
U3I749259X	SN7492W	SN7492W	9
U3I749359X	SN7493W	SN7493W	9
U3I749559X	SN7495AW	SN7495AW	9
U3I9N0051X	SN5400W	SN5400W	6
U3I9N0059X	SN7400W	SN7400W	6
U3I9N0151X	SN5401W	SN5401W	6
U3I9N0159X	SN7401W	SN7401W	6
U3I9N0251X	SN5402W	SN5402W	6
U3I9N0259X	SN7402W	SN7402W	6
U3I9N0451X	SN5404W	SN5404W	6
U3I9N0459X	SN7404W	SN7404W	6
U3I9N0551X	SN5405W	SN5405W	6
U3I9N0559X	SN7405W	SN7405W	6
U3I9N0851X	SN5408W	SN5408W	6
U3I9N0859X	SN7408W	SN7408W	6
U3I9N10451X	SN54104W	SN54104W	6
U3I9N10459X	SN74104W	SN74104W	6
U3I9N1051X	SN5410W	SN5410W	6
U3I9N10551X	SN54105W	SN54105W	6
U3I9N10559X	SN74105W	SN74105W	6
U3I9N1059X	SN7410W	SN7410W	6
U3I9N2051X	SN5420W	SN5420W	6
U3I9N2059X	SN7420W	SN7420W	6
U3I9N3051X	SN5430W	SN5430W	6
U3I9N3059X	SN7430W	SN7430W	6
U3I9N4051X	SN5440W	SN5440W	6
U3I9N4059X	SN7440W	SN7440W	6
U3I9N5051X	SN5450W	SN5450W	6
U3I9N5059X	SN7450W	SN7450W	6
U3I9N5151X	SN5451W	SN5451W	6
U3I9N5159X	SN7451W	SN7451W	6
U3I9N5351X	SN5453W	SN5453W	6
U3I9N5359X	SN7453W	SN7453W	6
U3I9N5451X	SN5454W	SN5454W	6
U3I9N5459X	SN7454W	SN7454W	6
U3I9N6051X	SN5460W	SN5460W	6
U3I9N6059X	SN7460W	SN7460W	6
U3I9N7051X	SN5470W	SN5470W	6
U3I9N7059X	SN7470W	SN7470W	6
U3I9N7251X	SN5472W	SN5472W	6
U3I9N7259X	SN7472W	SN7472W	6
U3I9N7351X	SN5473W	SN5473W	6
U3I9N7359X	SN7473W	SN7473W	6
U3I9N7451X	SN5474W	SN5474W	6
U3I9N7459X	SN7474W	SN7474W	6
U3I9N8651X	SN5486W	SN5486W	9
U3I9N8659X	SN7486W	SN7486W	9
U3I900051X	SN54104W	SN54104W	6
U3I900059X	SN74104W	SN74104W	6
U31900151X	SN54105W	SN54105W	6
U3I900159X	SN74105W	SN74105W	6
U3I900251X		SN5400W	6
U3I900259X		SN7400W	6
U3I900351X		SN5410W	6
U3I900359X		SN7410W	6
U3I900451X		SN5420W	6
U3I900459X		SN7420W	6
U3I900551X		SN5450W	6
U3I900559X		SN7450W	6
U3I900651X		SN5460W	6
U3I900659X		SN7460W	6
U3I900751X		SN5430W	6
U3I900759X		SN7430W	6
U3I900851X		SN5453W	6
U3I900859X		SN7453W	6
U3I900951X		SN5440W	6
U3I900959X		SN7440W	6
U3I901251X		SN5401W	6
U3I901259X		SN7401W	6
U3I901651X		SN5404W	6
U3I901659X		SN7404W	6
U3I901751X		SN5405W	6
U3I901759X		SN7405W	6
U3I935951X	SN5449W	SN5449W	9
U3I935959X	SN7449W	SN7449W	9
U3I937751X	SN5477W	SN5477W	9
U3I937759X	SN7477W	SN7477W	9
U3I938051X	SN5480W	SN5480W	9
U3I938059X	SN7480W	SN7480W	9
U3I938251X	SN5482W	SN5482W	9
U3I938259X	SN7482W	SN7482W	9
U3I939051X	SN5490W	SN5490W	9
U31939059X	SN7490W	SN7490W	9
U3I939151X	SN5491AW	SN5491AW	9
U3I939159X	SN7491AW	SN7491AW	9
U3I939251X	SN5492W	SN5492W	9
U3I939259X	SN7492W	SN7492W	9
U3I939351X	SN5493W	SN5493W	9
U3I939359X	SN7493W	SN7493W	9
U3I939551X	SN5495AW	SN5495AW	9
U3I939559X	SN7495W	SN7495W	9
U3I960051X		SN54122W	6
U3I960059X		SN74122W	6
U3I960151X	SN54122W	SN54122W	6
U3I960159X	SN74122W	SN74122W	6
U4L5418251X	SN54182W	SN54182W	9

TEXAS INSTRUMENTS
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DTL/TTL CIRCUITS

Fairchild TTL, Cont.

Type Number	Direct Replacement	Recommended for New Designs	Sec.
U4L5419251X	SN54192W	SN54192W	9
U4L5419351X	SN54193W	SN54193W	9
U4L548351X	SN5483W	SN5483W	9
U4L549451X	SN5494W	SN5494W	9
U4L549651X	SN5496W	SN5496W	9
U4L7418259X	SN74182W	SN74182W	9
U4L7419259X	SN74192W	SN74192W	9
U4L7419359X	SN74193W	SN74193W	9
U4L901451X		SN5486W	9
U4L901459X		SN7486W	9
U4L902051X		SN54111W	6
U4L902059X		SN74111W	6
U4L902251X		SN54111W	6
U4L902259X		SN74111W	6
U4L902451X		SN54111W	6
U4L902459X		SN74111W	6
U4L930051X	SN54195W	SN54195W	9
U4L930059X	SN74195W	SN75195W	9
U4L930151X		SN5442W	9
U4L930159X		SN7442W	9
U4L930451X		SN5482W	9
U4L930459X		SN7482W	9
U4L930651X		SN54190W	9
U4L930659X		SN74190W	9
U4L930751X	SN5448W	SN5448W	9
U4L930759X	SN7448W	SN7448W	9
U4L930951X		SN54153W	9
U4L930959X		SN74153W	9
U4L931051X	SN54160W	SN54160W	9
U4L931059X	SN74160W	SN74160W	9
U4L931251X		SN54151W	9
U4L931259X		SN74151W	9
U4L931451X		SN5475W	9
U4L931459X		SN7475W	9
U4L931559X	SN74141W	SN74141W	9
U4L931651X	SN54161W	SN54163W	9
U4L931659X	SN74161W	SN74163W	9
U4L9317511	SN5446AW	SN5446AW	9
U4L9317512	SN5447AW	SN5447AW	9
U4L9317513	SN5446AW	SN5446AW	9
U4L9317514	SN5447AW	SN5447AW	9
U4L9317591	SN7446AW	SN7446AW	9
U4L9317592	SN7447AW	SN7447AW	9
U4L9317593	SN7446AW	SN7446AW	9
U4L9317594	SN7447AW	SN7447AW	9
U4L932151X		SN54153W	9
U4L932159X		SN74153W	9
U4L932251X		SN54153W	9
U4L932259X		SN74153W	9
U4L932451X		SN5485W	9
U4L932459X		SN7485W	9
U4L932559X	SN74141W	SN74141W	9
U4L9327511	SN5448W	SN5448W	9
U4L9327512	SN5448W	SN5448W	9
U4L9327591	SN7448W	SN7448W	9
U4L9327592	SN7448W	SN7448W	9
U4L932851X		SN5491AW	9
U4L932859X		SN7491AW	9
U4L934251X	SN54182W	SN54182W	9
U4L934259X	SN74182W	SN74182W	9
U4L934851X		SN54180W	9
U4L934859X		SN74180W	9
U4L936051X	SN54192W	SN54192W	9
U4L936059X	SN74192W	SN74192W	9
U4L936651X	SN54193W	SN54193W	9
U4L936659X	SN74193W	SN74193W	9
U4L960251X		SN54123W	6
U4L960259X		SN74123W	6
U4M5418151X	SN54181W	SN54181W	9
U4M7418159X	SN74181W	SN74181W	9
U4M931151X		SN54150W	9
U4M931159X		SN74150W	9
U4M934051X		SN54181W	9
U4M934059X		SN74181W	9
U4M934151X	SN54181W	SN54181W	9
U4M934159X	SN74181W	SN74181W	9
U6A540051X	SN5400J, N	SN5400J, N	6
U6A540151X	SN5401J, N	SN5401J, N	6
U6A540251X	SN5402J, N	SN5402J, N	6
U6A540351X	SN5403J, N	SN5403J, N	6
U6A540451X	SN5404J, N	SN5404J, N	6
U6A540551X	SN5405J, N	SN5405J, N	6
U6A540851X	SN5408J, N	SN5408J, N	6
U6A5410451X	SN54104J, N	SN54104J, N	6
U6A541051X	SN5410J, N	SN5410J, N	6
U6A5410551X	SN54105J, N	SN54105J, N	6
U6A5410751X	SN54107J, N	SN54107J, N	6
U6A542051X	SN5420J, N	SN5420J, N	6
U6A543051X	SN5430J, N	SN5430J, N	6
U6A544051X	SN5440J, N	SN5440J, N	6
U6A545051X	SN5450J, N	SN5450J, N	6
U6A545151X	SN5451J, N	SN5451J, N	6
U6A545351X	SN5453J, N	SN5453J, N	6
U6A545451X	SN5454J, N	SN5454J, N	6
U6A546051X	SN5460J, N	SN5460J, N	6
U6A547051X	SN5470J, N	SN5470J, N	6
U6A547251X	SN5472J, N	SN5472J, N	6
U6A547351X	SN5473J, N	SN5473J, N	6
U6A547451X	SN5474J, N	SN5474J, N	6
U6A548051X	SN5480J, N	SN5480J, N	9
U6A548251X	SN5482J, N	SN5482J, N	9
U6A548651X	SN5486J, N	SN5486J, N	9
U6A549051X	SN5490J, N	SN5490J, N	9
U6A549151X	SN5491AJ, N	SN5491AJ, N	9
U6A549251X	SN5492J, N	SN5492J, N	9
U6A549351X	SN5493J, N	SN5493J, N	9
U6A549551X	SN5495AJ, N	SN5495AJ, N	9
U6A740059X	SN7400J, N	SN7400J, N	6
U6A740159X	SN7401J, N	SN7401J, N	6
U6A740259X	SN7402J, N	SN7402J, N	6
U6A740359X	SN7403J, N	SN7403J, N	6
U6A740459X	SN7404J, N	SN7404J, N	6
U6A740559X	SN7405J, N	SN7405J, N	6
U6A740859X	SN7408J, N	SN7408J, N	6
U6A7410459X	SN74104J, N	SN74104J, N	6
U6A7410559X	SN74105J, N	SN74105J, N	6
U6A741059X	SN7410J, N	SN7410J, N	6
U6A7410759X	SN74107J, N	SN74107J, N	6
U6A742059X	SN7420J, N	SN7420J, N	6
U6A743059X	SN7430J, N	SN7430J, N	6
U6A744059X	SN7440J, N	SN7440J, N	6
U6A745059X	SN7450J, N	SN7450J, N	6
U6A745159X	SN7451J, N	SN7451J, N	6
U6A745359X	SN7453J, N	SN7453J, N	6
U6A745459X	SN7454J, N	SN7454J, N	6
U6A746059X	SN7460J, N	SN7460J, N	6
U6A747059X	SN7470J, N	SN7470J, N	6
U6A747259X	SN7472J, N	SN7472J, N	6
U6A747359X	SN7473J, N	SN7473J, N	6
U6A747459X	SN7474J, N	SN7474J, N	6
U6A748059X	SN7480J, N	SN7480J, N	9
U6A748259X	SN7482J, N	SN7482J, N	9
U6A748659X	SN7486J, N	SN7486J, N	9
U6A749059X	SN7490J, N	SN7490J, N	9

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B

Type Number	Direct Replacement	Recommended for New Designs	Sec.
U6A749159X	SN7491AJ, N	SN7491AJ, N	9
U6A749259X	SN7492J, N	SN7492J, N	9
U6A749359X	SN7493J, N	SN7493J, N	9
U6A749559X	SN7495AJ, N	SN7495AJ, N	9
U6A9N0051X	SN5400J, N	SN5400J, N	6
U6A9N0059X	SN7400J, N	SN7400J, N	6
U6A9N0151X	SN5401J, N	SN5401J, N	6
U6A9N0159X	SN7401J, N	SN7401J, N	6
U6A9N0251X	SN5402J, N	SN5402J, N	6
U6A9N0259X	SN7402J, N	SN7402J, N	6
U6A9N0351X	SN5403J, N	SN5403J, N	6
U6A9N0359X	SN7403J, N	SN7403J, N	6
U6A9N0451X	SN5404J, N	SN5404J, N	6
U6A9N0459X	SN7404J, N	SN7404J, N	6
U6A9N0551X	SN5405J, N	SN5405J, N	6
U6A9N0559X	SN7405J, N	SN7405J, N	6
U6A9N0851X	SN5408J, N	SN5408J, N	6
U6A9N0859X	SN7408J, N	SN7408J, N	6
U6A9N10451X	SN54104J, N	SN54104J, N	6
U6A9N10459X	SN74104J, N	SN74104J, N	6
U6A9N1051X	SN5410J, N	SN5410J, N	6
U6A9N10551X	SN54105J, N	SN54105J, N	6
U6A9N10559X	SN74105J, N	SN74105J, N	6
U6A9N1059X	SN7410J, N	SN7410J, N	6
U6A9N10751X	SN54107J, N	SN54107J, N	6
U6A9N10759X	SN74107J, N	SN74107J, N	6
U6A9N2051X	SN5420J, N	SN5420J, N	6
U6A9N2059X	SN7420J, N	SN7420J, N	6
U6A9N3051X	SN5430J, N	SN5430J, N	6
U6A9N3059X	SN7430J, N	SN7430J, N	6
U6A9N4051X	SN5440J, N	SN5440J, N	6
U6A9N4059X	SN7440J, N	SN7440J, N	6
U6A9N5051X	SN5450J, N	SN5450J, N	6
U6A9N5059X	SN7450J, N	SN7450J, N	6
U6A9N5151X	SN5451J, N	SN5451J, N	6
U6A9N5159X	SN7451J, N	SN7451J, N	6
U6A9N5351X	SN5453J, N	SN5453J, N	6
U6A9N5359X	SN7453J, N	SN7453J, N	6
U6A9N5451X	SN5454J, N	SN5454J, N	6
U6A9N5459X	SN7454J, N	SN7454J, N	6
U6A9N6051X	SN5460J, N	SN5460J, N	6
U6A9N6059X	SN7460J, N	SN7460J, N	6
U6A9N7051X	SN5470J, N	SN5470J, N	6
U6A9N7059X	SN7470J, N	SN7470J, N	6
U6A9N7251X	SN5472J, N	SN5472J, N	6
U6A9N7259X	SN7472J, N	SN7472J, N	6
U6A9N7351X	SN5473J, N	SN5473J, N	6
U6A9N7359X	SN7473J, N	SN7473J, N	6
U6A9N7451X	SN5474J, N	SN5474J, N	6
U6A9N7459X	SN7474J, N	SN7474J, N	6
U6A9N8651X	SN5486J, N	SN5486J, N	9
U6A9N8659X	SN7486J, N	SN7486J, N	9
U6A900051X	SN54104J, N	SN54104J, N	6
U6A900059X	SN74104J, N	SN74104J, N	6
U6A900151X	SN54105J, N	SN54105J, N	6
U6A900159X	SN74105J, N	SN74105J, N	6
U6A900251X	SN5400J, N	SN5400J, N	6
U6A900259X	SN7400J, N	SN7400J, N	6
U6A900351X	SN5410J, N	SN5410J, N	6
U6A900359X	SN7410J, N	SN7410J, N	6
U6A900451X	SN5420J, N	SN5420J, N	6
U6A900459X	SN7420J, N	SN7420J, N	6
U6A900551X	SN5450J, N	SN5450J, N	6
U6A900559X	SN7450J, N	SN7450J, N	6
U6A900651X	SN5460J, N	SN5460J, N	6
U6A900659X	SN7460J, N	SN7460J, N	6
U6A900751X		SN5430J, N	6

Type Number	Direct Replacement	Recommended for New Designs	Sec.
U6A900759X		SN7430J, N	6
U6A900851X	SN54H53J, N	SN5453J, N	6
U6A900859X	SN74H53J, N	SN7453J, N	6
U6A900951X	SN5440J, N	SN5440J, N	6
U6A900959X	SN7440J, N	SN7440J, N	6
U6A901251X	SN5403J, N	SN5401J, N	6
U6A901259X	SN7403J, N	SN7401J, N	6
U6A901651X	SN5404J, N	SN5404J, N	6
U6A901659X	SN7404J, N	SN7404J, N	6
U6A901751X	SN5405J, N	SN5405J, N	6
U6A901759X	SN7405J, N	SN7405J, N	6
U6A938051X	SN5480J, N	SN5480J, N	9
U6A938059X	SN7480J, N	SN7480J, N	9
U6A938251X	SN5482J, N	SN5482J, N	9
U6A938259X	SN7482J, N	SN7482J, N	9
U6A939051X	SN5490J, N	SN5490J, N	9
U6A939059X	SN7490J, N	SN7490J, N	9
U6A939151X	SN5491AJ, N	SN5491AJ, N	9
U6A939159X	SN7491AJ, N	SN7491AJ, N	9
U6A939251X	SN5492J, N	SN5492J, N	9
U6A939259X	SN7492J, N	SN7492J, N	9
U6A939351X	SN5493J, N	SN5493J, N	9
U6A939359X	SN7493J, N	SN7493J, N	9
U6A939551X	SN5495AJ, N	SN5495AJ, N	9
U6A939559X	SN7495AJ, N	SN7495AJ, N	9
U6A960051X		SN54122J, N	6
U6A960059X		SN74122J, N	6
U6A960151X	SN54122J, N	SN54122J, N	6
U6A960159X	SN74122J, N	SN74122J, N	6
U6B9N7651X	SN5476J, N	SN5476J, N	6
U6B9N7659X	SN7476J, N	SN7476J, N	6
U6B547551X	SN5475J, N	SN5475J, N	9
U6B547651X	SN5476J, N	SN5476J, N	6
U6B548351X	SN5483J, N	SN5483J, N	9
U6B7414159X	SN74141J, N	SN74141J, N	9
U6B744159X	SN74141J, N	SN74141J, N	9
U6B747559X	SN7475J, N	SN7475J, N	9
U6B747659X	SN7476J, N	SN7476J, N	6
U6B748359X	SN7483J, N	SN7483J, N	9
U6B901451X		SN5486J, N	9
U6B901459X		SN7486J, N	9
U6B901551X		SN5402J, N	6
U6B901559X		SN7402J, N	6
U6B930451X		SN5482J, N	9
U6B930459X		SN7482J, N	9
U6B930751X	SN5448J, N	SN5448J, N	9
U6B930759X	SN7448J, N	SN7448J, N	9
U6B930951X		SN54153J, N	9
U6B930959X		SN74153J, N	9
U6B931559X	SN74141J, N	SN74141J, N	9
U6B932559X	SN74141J, N	SN74141J, N	9
U6B934851X		SN54180J, N	9
U6B934859X		SN74180J, N	9
U6B937551X	SN5475J, N	SN5475J, N	9
U6B937559X	SN7475J, N	SN7475J, N	9
U6B938351X	SN5483J, N	SN5483J, N	9
U6B938359X	SN7483J, N	SN7483J, N	9
U6N5418151X	SN54181J, N	SN54181J, N	9
U6N7418159X	SN74181J, N	SN74181J, N	9
U6N930651X		SN54190J, N	9
U6N930659X		SN74190J, N	9
U6N931151X	SN54154J, N	SN54154J, N	9
U6N931159X	SN74154J, N	SN74154J, N	9
U6N934051X		SN54181J, N	9
U6N934059X		SN74181J, N	9
U6N934151X	SN54181J, N	SN54181J, N	9
U6N934159X	SN74181J, N	SN74181J, N	9

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Type Number	Direct Replacement	Recommended for New Designs	Sec.
U7A935051X		SN5490J, N	9
U7A935059X		SN7490J, N	9
U7A935651X		SN5493J, N	9
U7A935659X		SN7493J, N	9
U7B5418251X	SN54182J, N	SN54182J, N	9
U7B5419251X	SN54192J, N	SN54192J, N	9
U7B5419351X	SN54193J, N	SN54193J, N	9
U7B544251X	SN5442J, N	SN5442J, N	9
U7B544351X	SN5443J, N	SN5443J, N	9
U7B544451X	SN5444J, N	SN5444J, N	9
U7B544651X	SN5446J, N	SN5446J, N	9
U7B544751X	SN5447J, N	SN5447J, N	9
U7B544851X	SN5448J, N	SN5448J, N	9
U7B549451X	SN5494J, N	SN5494J, N	9
U7B549651X	SN5496J, N	SN5496J, N	9
U7B7418259X	SN74182J, N	SN74182J, N	9
U7B7419259X	SN74192J, N	SN74192J, N	9
U7B7419359X	SN74193J, N	SN74193J, N	9
U7B744259X	SN7442J, N	SN7442J, N	9
U7B744359X	SN7443J, N	SN7443J, N	9
U7B744459X	SN7444J, N	SN7444J, N	9
U7B744659X	SN7446J, N	SN7446J, N	9
U7B744759X	SN7447J, N	SN7447J, N	9
U7B744859X	SN7448J, N	SN7448J, N	9
U7B749459X	SN7494J, N	SN7494J, N	9
U7B749659X	SN7496J, N	SN7496J, N	9
U7B902051X		SN54111J, N	6
U7B902059X		SN74111J, N	6
U7B902251X		SN54111J, N	6
U7B902259X		SN74111J, N	6
U7B902451X		SN54111J, N	6
U7B902459X		SN74111J, N	6
U7B930051X	SN54195J, N	SN54195J, N	9
U7B930059X	SN74195J, N	SN74195J, N	9
U7B930151X		SN5442J, N	9
U7B930159X		SN7442J, N	9
U7B931051X	SN54160J, N	SN54160J, N	9
U7B931059X	SN74160J, N	SN74160J, N	9
U7B931251X		SN54151J, N	9
U7B931259X		SN74151J, N	9
U7B931451X		SN5475J, N	9
U7B931459X		SN7475J, N	9
U7B931651X	SN54161J, N	SN54161J, N	9
U7B931659X	SN74161J, N	SN74161J, N	9

Type Number	Direct Replacement	Recommended for New Designs	Sec.
U7B9317511	SN5446AJ, N	SN5446AJ, N	9
U7B9317512	SN5447AJ, N	SN5447AJ, N	9
U7B9317513	SN5446AJ, N	SN5446AJ, N	9
U7B9317514	SN5447AJ, N	SN5447AJ, N	9
U7B9317591	SN7446AJ, N	SN7446AJ, N	9
U7B9317592	SN7447AJ, N	SN7447AJ, N	9
U7B9317593	SN7446AJ, N	SN7446AJ, N	9
U7B9317594	SN7447AJ, N	SN7447AJ, N	9
U7B932151X		SN54153J, N	9
U7B932159X		SN74153J, N	9
U7B932251X		SN54153J, N	9
U7B932259X		SN74153J, N	9
U7B932451X		SN5485J, N	9
U7B932459X		SN7485J, N	9
U7B9327511	SN5448J, N	SN5448J, N	9
U7B9327512	SN5448J, N	SN5448J, N	9
U7B9327591	SN7448J, N	SN7448J, N	9
U7B9327592	SN7448J, N	SN7448J, N	9
U7B932851X		SN5491AJ, N	9
U7B932859X		SN7491AJ, N	9
U7B934251X	SN54182J, N	SN54182J, N	9
U7B934259X	SN74182J, N	SN74182J, N	9
U7B935251X	SN5442J, N	SN5442J, N	9
U7B935259X	SN7442J, N	SN7442J, N	9
U7B935351X	SN5443J, N	SN5443J, N	9
U7B935359X	SN7443J, N	SN7443J, N	9
U7B935451X	SN5444J, N	SN5444J, N	9
U7B935459X	SN7444J, N	SN7444J, N	9
U7B9357511	SN5446AJ, N	SN5446AJ, N	9
U7B9357512	SN5447AJ, N	SN5447AJ, N	9
U7B9357591	SN7446AJ, N	SN7446AJ, N	9
U7B9357592	SN7447AJ, N	SN7447AJ, N	9
U7B935851X	SN5448J, N	SN5448J, N	9
U7B935859X	SN7448J, N	SN7448J, N	9
U7B936051X	SN54192J, N	SN54192J, N	9
U7B936059X	SN74192J, N	SN74192J, N	9
U7B936651X	SN54193J, N	SN54193J, N	9
U7B936659X	SN74193J, N	SN74193J, N	9
U7B939451X	SN5494J, N	SN5494J, N	9
U7B939459X	SN7494J, N	SN7494J, N	9
U7B939651X	SN5496J, N	SN5496J, N	9
U7B939659X	SN7496J, N	SN7496J, N	9
U7B960251X		SN54123J, N	6
U7B960259X		SN74123J, N	6

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Type Number	Direct Replacement	Recommended for New Designs	Sec.
MC830F	SN15830U	SN7420W	6
MC830L, P	SN15830J, N	SN7420J, N	6
MC831F	SN15831U	SN74110W	6
MC831L, P	SN15831J, N	SN74110J, N	6
MC832F	SN15832U	SN7440W	6
MC832L, P	SN15832J, N	SN7440J, N	6
MC833F	SN15833U	SN7460W	6
MC833L, P	SN15833J, N	SN7460J, N	6
MC834F	SN15834U	SN7405W	6
MC834L, P	SN15834J, N	SN7405J, N	6
MC835F	SN15838U	SN7405W	6
MC835L, P	SN15838J, N	SN7405J, N	6
MC836F	SN15836U	SN7405W	6

Type Number	Direct Replacement	Recommended for New Designs	Sec.
MC836L, P	SN15836J, N	SN7405J, N	6
MC837F	SN15837U	SN7405W	6
MC837L, P	SN15837J, N	SN7405J, N	6
MC838F		SN74162W	9
MC838L, P		SN74162J, N	9
MC839F		SN74163W	9
MC839L, P		SN74163J, N	9
MC840F	SN15835U	SN7405W	6
MC840L, P	SN15835J, N	SN7405J, N	6
MC842F		SN7474W	6
MC842L, P		SN7474J, N	6
MC844F	SN15844U	SN7440W	6
MC844L, P	SN15844J, N	SN7440J, N	6

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Type Number	Direct Replacement	Recommended for New Designs	Sec.
MC845F	SN15845U	SN74110W	6
MC845L, P	SN15846J, N	SN74110J, N	6
MC846F	SN15846W	SN7400W	6
MC846L, P	SN15846J, N	SN7400J, N	6
MC848F	SN15848U	SN74110W	6
MC848L, P	SN15848J, N	SN74110J, N	6
MC849F	SN15849U	SN7400W	6
MC849L, P	SN15849J, N	SN7400J, N	6
MC850F	SN15850U	SN74110W	6
MC850L, P	SN15850J, N	SN74110J, N	6
MC851F	SN15851U	SN74121W	6
MC851L, P	SN15851J, N	SN74121J, W	6
MC852F	SN158099U	SN7476W	6
MC852L, P	SN158099J, N	SN7476J, N	6
MC853F	SN158093U	SN7473W	6
MC853L, P	SN158093J, N	SN7473J, N	6
MC855F	SN158097U	SN7476W	6
MC855L, P	SN158097J, N	SN7476J, N	6
MC856F	SN158094U	SN7473W	6
MC856L, P	SN158094J, N	SN7473J, N	6
MC857F	SN15857U	SN7437W	6
MC857L, P	SN15857J, N	SN7437J, N	6
MC858F	SN15858U	SN7437W	6
MC858L, P	SN15858J, N	SN7437J, N	6
MC860F		SN74H103W	7
MC860L, P		SN74H103J, N	7
MC861F	SN15861U	SN7420W	6
MC861L, P	SN15861J, N	SN7420J, N	6
MC862F	SN15862U	SN7410W	6
MC862L, P	SN15862J, N	SN7410J, N	6
MC863F	SN15863U	SN7410W	6
MC863L, P	SN15863J, N	SN7410J, N	6
MC1800F	SN151800U	SN7420W	6
MC1800L, P	SN151800J, N	SN7420J, N	6
MC1801F	SN151801U	SN7420W	6
MC1801L, P	SN151801J, N	SN7420J, N	6
MC1802F	SN151802U	SN7430W	6
MC1802L, P	SN151802J, N	SN7430J, N	6
MC1803F	SN151803U	SN7430W	6
MC1803L, P	SN151803J, N	SN7430J, N	6
MC1804F	SN151804U	SN7430W	6
MC1804L, P	SN151804J, N	SN7430J, N	6
MC1805F	SN151805U	SN7430W	6
MC1805L, P	SN151805J, N	SN7430J, N	6
MC1806F	SN151806U	SN7408W	6
MC1806L, P	SN151806J, N	SN7408J, N	6
MC1807F	SN151807U	SN7408W	6
MC1807L, P	SN151807J, N	SN7408J, N	6
MC1808F	SN151808U	SN7432W	6
MC1808L, P	SN151808J, N	SN7432J, N	6
MC1809F	SN151809U	SN7432W	6
MC1809L, P	SN151809J, N	SN7432J, N	6
MC1810F	SN151810U	SN7402W	6
MC1810L, P	SN151810J, N	SN7402J, N	6
MC1811F	SN151811U	SN7402W	6
MC1811L, P	SN151811J, N	SN7402J, N	6
MC1812F	SN151812U	SN7486W	9
MC1812L, P	SN151812J, N	SN7486J, N	9
MC1813L, P		SN7475J, N	9
MC1814F		SN7475W	9
MC1814L, P		SN7475J, N	9
MC1815F		SN74H101W	7
MC1815L, P		SN74H101J, N	7
MC1816F		SN74H101W	7
MC1816L, P		SN74H101J, N	7
MC1818F		SN7403W	6
MC1820L, P		SN7403J, N	6
MC1820L, P	SN151820J, N	SN7406J, N	6

Type Number	Direct Replacement	Recommended for New Designs	Sec.
MC930F	SN15930U	SN5420W	6
MC930L	SN15930J, N	SN5420J, N	6
MC931F	SN15931U	SN54110W	6
MC931L	SN15931J, N	SN54110J, N	6
MC932F	SN15932U	SN5440W	6
MC932L	SN15932J, N	SN5440J, N	6
MC933F	SN15933U	SN5460W	6
MC933L	SN15933J, N	SN5460J, N	6
MC934F	SN15934U	SN5405W	6
MC934L	SN15934J, N	SN5405J, N	6
MC935F	SN15938U	SN5405W	6
MC935L	SN15938J, N	SN5405J, N	6
MC936F	SN15936U	SN5405W	6
MC936L	SN15936J, N	SN5405J, N	6
MC937F	SN15937U	SN5405W	6
MC937L	SN15937J, N	SN5405J, N	6
MC938F		SN54162W	9
MC938L		SN54162J, N	9
MC939F		SN54163W	9
MC939L		SN54163J, N	9
MC940F	SN15935U	SN5405W	6
MC940L	SN15935J, N	SN5405J, N	6
MC842F		SN5474W	6
MC842L		SN5474J, N	6
MC944F	SN15944U	SN5440W	6
MC944L	SN15944J, N	SN5440J, N	6
MC945F	SN15945U	SN54110W	6
MC945L	SN15945J, N	SN54110J, N	6
MC946F	SN15946U	SN5400W	6
MC946L	SN15946J, N	SN5400J, N	6
MC948F	SN15948U	SN54110W	6
MC948L	SN15948J, N	SN54110J, N	6
MC949F	SN15949U	SN5400W	6
MC949L	SN15949J, N	SN5400J, N	6
MC950F	SN15950U	SN54110W	6
MC950L	SN15950J, N	SN54110J, N	6
MC951F	SN15951U	SN54121W	6
MC951L	SN15951J, N	SN5412J, N	6
MC952F	SN159099U	SN5476W	6
MC952L	SN159099J, N	SN5476J, N	6
MC953F	SN159093U	SN5473W	6
MC953L	SN159093J, N	SN5473J, N	6
MC955F	SN159097U	SN5476W	6
MC955L	SN159097J, N	SN5476J, N	6
MC956F	SN159094U	SN5473W	6
MC956L	SN159094J, N	SN5473J, N	6
MC957F	SN15957U	SN5437W	6
MC957L	SN15957J, N	SN5437J, N	6
MC958F	SN15958U	SN5437W	6
MC958L	SN15958J, N	SN5437J, N	6
MC860F		SN54H103W	7
MC860L		SN54H103J, N	7
MC961F	SN15961U	SN5420W	6
MC961L	SN15961J, N	SN5420J, N	6
MC962F	SN15962U	SN5410W	6
MC962L	SN15962J, N	SN5410J, N	6
MC963F	SN15963U	SN5410W	6
MC963L	SN15963J, N	SN5410J, N	6
MC1900F	SN151900U	SN5420W	6
MC1900L	SN151900J, N	SN5420J, N	6
MC1901F	SN151901U	SN5420W	6
MC1901L	SN151901J, N	SN5420J, N	6
MC1902F	SN151902U	SN5430W	6
MC1902L	SN151902J, N	SN5430J, N	6
MC1903F	SN151903U	SN5430W	6
MC1903L	SN151903J, N	SN5430J, N	6
MC1904F	SN151904U	SN5430W	6
MC1904L	SN151904J, N	SN5430J, N	6

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Type Number	Direct Replacement	Recommended for New Designs	Sec.
MC1905F	SN151905U	SN5430W	6
MC1905L	SN151905J, N	SN5430J, N	6
MC1906F	SN151906U	SN5408W	6
MC1906L	SN151906J, N	SN5408J, N	6
MC1907F	SN151907U	SN5408W	6
MC1907L	SN151907J, N	SN5408J, N	6
MC1908F	SN151908U	SN5432W	6
MC1908L	SN151908J, N	SN5432J, N	6
MC1909F	SN151909U	SN5432W	6
MC1909L	SN151909J, N	SN5432J, N	6
MC1910F	SN151910U	SN5402W	6
MC1910L	SN151910J, N	SN5402J, N	6
MC1911F	SN151911U	SN5402W	6
MC1911L	SN151911J, N	SN5402J, N	6
MC1912L	SN151912U	SN5486W	9
MC1912L	SN151912J, N	SN5486J, N	9
MC1913F		SN5475W	9
MC1913L		SN5475J, N	9
MC1914F		SN5475W	9
MC1914L		SN5475J, N	9
MC1915F		SN54H101W	7
MC1915L		SN54H101J, N	7
MC1916F		SN54H101W	7
MC1916L		SN54H101J, N	7
MC1918F		SN5403W	6
MC1918L		SN5403J, N	6
MC1920L	SN151920J, N	SN5406J, N	6

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Type Number	Direct Replacement	Recommended For New Designs	Sec. Page
MC400F	SNG42U	SN7420W	6
MC400L, P	SNG42J, N	SN7420J, N	6
MC401F	SNG52U	SN7453W	6
MC401L, P	SNG52J, N	SN7453J, N	6
MC402F	SNG62U	SN7430W	6
MC402L, P	SNG62J, N	SN7430J, N	6
MC403F	SNG92U	SN7486W	9
MC403L, P	SNG92J, N	SN7486J, N	9
MC404F	SNG102U	SN7453W	6
MC404L, P	SNG102J, N	SN7453J, N	6
MC405F	SNG112U	SN74H55W	7
MC405L, P	SNG112J, N	SN74H55J, N	6
MC406F	SNG122U	SN7430W	6
MC406L, P	SNG122J, N	SN7430J, N	6
MC407F	SNG132U	SN74S140W	5
MC407L, P	SNG132J, N	SN74S140J, N	5
MC408F	SNG142U	SN7400W	6
MC408L, P	SNG142J, N	SN7400J, N	6
MC409F	SNG152U	SN74H62W	7
MC409L, P	SNG152J, N	SN74H62J, N	7
MC410F	SNG172U	SN7460W	6
MC410L, P	SNG172J, N	SN7460J, N	6
MC411F	SNG182U	SN7430W	6
MC411L, P	SNG182J, N	SN7430J, N	6
MC412F	SNG192U	SN7410W	6
MC412L, P	SNG192J, N	SN7410J, N	6
MC413F	SNF12U	SN7472W	6
MC413L, P	SNF12J, N	SN7472J, N	6
MC414F	SNF22U	SN7472W	6
MC414L, P	SNF22J, N	SN7472J, N	6
MC415F	SNF52U	SN7472W	6
MC415L, P	SNF52J, N	SN7472J, N	6
MC416F	SNF62U	SN74H101W	7
MC416L, P	SNF62J, N	SN74H101J, N	7
MC417F		SN74105W	6
MC417L, P		SN74105J, N	6
MC419F	SNG162U	SN7438W	6
MC419L, P	SNG162J, N	SN7438J, N	6
MC420F	SNG72U	SN7450W	6
MC420L, P	SNG72J, N	SN7450J, N	6
MC421F	SNF32U	SN74104W	6
MC421L, P	SNF32J, N	SN74104J, N	6
MC422F		SN7474W	6
MC422L, P		SN7474J, N	6
MC423F	SNF102U	SN7473W	6
MC423L, P	SNF102J, N	SN7473J, N	6
MC424F	SNF112U	SN7476W	6
MC424L, P	SNF112J, N	SN7476J, N	6
MC425F		SN7404W	6
MC425L, P		SN7404J, N	6
MC426F	SNG82U	SN7413W	6
MC426L, P	SNG82J, N	SN7413J, N	6
MC427F	SNG282U	SN74H52W	7
MC427L, P	SNG282J, N	SN74H52J, N	7
MC428F		SN74H61W	7
MC428L, P		SN74H61J, N	7
MC450F	SNG43U	SN7420W	6
MC450L, P	SNG43J, N	SN7420J, N	6
MC451F	SNG53U	SN7453J, N	6
MC451L, P	SNG53J, N	SN7453J, N	6
MC452F	SNG63U	SN7430W	6
MC452L, P	SNG63J, N	SN7430J, N	6
MC453F	SNG93U	SN7486W	9
MC453L, P	SNG93J, N	SN7486J, N	9
MC454F	SNG103U	SN7453W	6
MC454L, P	SNG103J, N	SN7453J, N	6
MC455F	SNG113U	SN74H55W	7
MC455L, P	SNG113J, N	SN74H55J, N	7
MC456F	SNG123U	SN7430W	6
MC456L, P	SNG123J, N	SN7430J, N	6
MC457F	SNG133U	SN75S140W	5
MC4571L, P	SNG133J, N	SN74S140J, N	5
MC458F	SNG143U	SN7400W	6
MC458L, P	SNG143J, N	SN7400J, N	6
MC459F	SNG153U	SN74H62W	7
MC459L, P	SNG153J, N	SN74H62J, N	7
MC460F	SNG173U	SN7460W	6
MC460L, P	SNG173J, N	SN7460J, N	6
MC461F	SNG183U	SN7430W	6
MC461L, P	SNG183J, N	SN7430J, N	6
MC462F	SNG193U	SN7410W	6
MC462L, P	SNG193J, N	SN7410J, N	6
MC463F	SNF13U	SN7472W	6
MC463L, P	SNF13J, N	SN7472J, N	6
MC464F	SNF23U	SN7472W	6
MC464F	SNF23J, N	SN7472J, N	6
MC465F	SNF53U	SN7472W	6
MC465L, P	SNF53J, N	SN7472J, N	6

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Type Number	Direct Replacement	Recommended for New Designs	Sec.
MC466F	SNF63U	SN74H101W	7
MC466L, P	SNF63J, N	SN74H101J, N	7
MC467F		SN74105W	6
MC467L, P		SN74105J, N	6
MC469F	SNG163U	SN7438W	6
MC469L, P	SNG163J, N	SN7438J, N	6
MC470F	SNG73U	SN7450W	6
MC470L, P	SNG73J, N	SN7450J, N	6
MC471F	SNF33U	SN74104W	6
MC471L, P	SNF33J, N	SN74104J, N	6
MC472F		SN7474W	6
MC472L, P		SN7474J, N	6
MC473F	SNF103U	SN7473W	6
MC473L, P	SNF103J, N	SN7473J, N	6
MC474F	SNF113U	SN7476W	6
MC474L, P	SNF113J, N	SN7476J, N	6
MC475F		SN7404W	6
MC475L, P		SN7404J, N	6
MC476F	SNG83U	SN7413W	6
MC476L, P	SNG83J, N	SN7413J, N	6
MC477F	SNG283U	SN74H52W	7
MC477L, P	SNG283J, N	SN74H52J, N	7
MC478F		SN74H61W	7
MC478L, P		SN74H61J, N	7
MC500F	SNG40U	SN5420W	6
MC500L	SNG40J, N	SN5420J, N	6
MC501F	SNG50U	SN5453W	6
MC501L	SNG50J, N	SN5453J, N	6
MC502F	SNG60U	SN5430W	6
MC502L	SNG60J, N	SN5430J, N	6
MC503F	SNG90U	SN5486W	9
MC503L	SNG90J, N	SN5486J, N	9
MC504F	SNG100U	SN5453W	6
MC504L	SNG100J, N	SN5453J, N	6
MC505F	SNG110U	SN54H55W	7
MC505L	SNG110J, N	SN54H55J, N	7
MC506F	SNG120U	SN5430W	6
MC506L	SNG120J, N	SN5430J, N	6
MC507F	SNG130U	SN54S140W	5
MC507L	SNG130J, N	SN54S140J, N	5
MC508F	SNG140U	SN5400W	6
MC508L	SNG140J, N	SN5400J, N	6
MC509F	SNG150U	SN54H62W	7
MC509L	SNG150J, N	SN54H62J, N	7
MC510F	SNG170U	SN5460W	6
MC510L	SNG170J, N	SN5460J, N	6
MC511F	SNG180U	SN5430W	6
MC511L	SNG180J, N	SN5430J, N	6
MC512F	SNG190U	SN5410W	6
MC512L	SNG190J, N	SN5410J, N	6
MC513F	SNF10U	SN5472W	6
MC513L	SNF10J, N	SN5472J, N	6
MC514F	SNF20U	SN5472W	6
MC514L	SNF20J, N	SN5472J, N	6
MC515F	SNF50U	SN5472W	6
MC515L	SNF50J, N	SN5472J, N	6
MC516F	SNF60U	SN54H101W	7
MC516L	SNF60J, N	SN54H101J, N	7
MC517F		SN54105W	6
MC517L		SN54105J, N	6
MC519F	SNG160U	SN5438W	6
MC519L	SNG160J, N	SN5438J, N	6
MC520F	SNG70U	SN5450W	6
MC520L	SNG70J, N	SN5450J, N	6
MC521F	SNF30U	SN54104W	6
MC521L	SNF30J, N	SN54104J, N	6
MC522F		SN5474W	6
MC522L		SN5474J, N	6
MC523F	SNF100U	SN5473W	6
MC523L	SNF100J, N	SN5473J, N	6
MC524F	SNF110U	SN5476W	6
MC524L	SNF110J, N	SN5476J, N	6
MC525F		SN5404W	6
MC525L		SN5404J, N	6
MC526F	SNG80U	SN5413W	6
MC526L	SNG80J, N	SN5413J, N	6
MC527F	SNG280U	SN54H52W	7
MC527L	SNG280J, N	SN54H52J, N	7
MC528F		SN54H61W	7
MC528L		SN54H61J, N	7
MC550F	SNG41U	SN5420W	6
MC550L	SNG41J, N	SN5420J, N	6
MC551F	SNG51U	SN5453W	6
MC551L	SNG51J, N	SN5453J, N	6
MC552F	SNG61U	SN5430W	6
MC552L	SNG61J, N	SN5430J, N	6
MC553F	SNG91U	SN5486W	9
MC553L	SNG91J, N	SN5486J, N	9
MC554F	SNG101U	SN5453W	6
MC554L	SNG101J, N	SN5453J, N	6
MC55F	SNG111U	SN54H55W	7
MC55L	SNG111J, N	SN54H55J, N	7
MC556F	SNG121U	SN5430W	6
MC556L	SNG121J, N	SN5430J, N	6
MC557F	SNG131U	SN54S140W	5
MC557L	SNG131J, N	SN54S140J, N	5
MC558F	SNG141W	SN5400W	6
MC558L	SNG141J, N	SN5400J, N	6
MC559F	SNG151U	SN54H62W	7
MC559L	SNG151J, N	SN54H62J, N	7
MC560F	SNG171U	SN5460W	6
MC560L	SNG171J, N	SN5460J, N	6
MC561F	SNG181U	SN5430W	6
MC561L	SNG181J, N	SN5430J, N	6
MC562F	SNG191U	SN5410W	6
MC562L	SNG191J, N	SN5410J, N	6
MC563F	SNF11U	SN5472W	6
MC563L	SNF11J, N	SN5472J, N	6
MC564F	SNF21U	SN5472W	6
MC564L	SNF21J, N	SN5472J, N	6
MC565F	SNF51U	SN5472W	6
MC565L	SNF51J, N	SN5472J, N	6
MC566F	SNF61U	SN54H101W	7
MC566L	SNF61J, N	SN54H101J, N	7
MC567F		SN54105W	6
MC567L		SN54105J, N	6
MC569F	SNG161U	SN5438W	6
MC569L	SNG161J, N	SN5438J, N	6
MC570F	SNG71U	SN5450W	6
MC570L	SNG71J, N	SN5450J, N	6
MC571F	SNF31U	SN54104W	6
MC571L	SNF31J, N	SN54104J, N	6
MC572F		SN5474W	6
MC572L		SN5474J, N	6
MC573F	SNF101U	SN5473W	6
MC573L	SNF101J, N	SN5473J, N	6
MC574F	SNF111U	SN5476W	6
MC574L	SNF111J, N	SN5476J, N	6
MC575F		SN5404W	6
MC575L		SN5404J, N	6
MC576F	SNG81U	SN5413W	6
MC576L	SNG81J, N	SN5413J, N	6
MC577F	SNG281U	SN54H52W	7
MC577L	SNG281J, N	SN54H52J, N	7

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MC578F		SN54H61W	7
MC578L		SN54H61J, N	7
MC2000F	SNG212U	SN74H55W	7
MC2000L, P	SNG212J, N	SN74H55J, N	7
MC2001F	SNG222U	SN74H00W	7
MC2001L, P	SNG222J, N	SN74H00J, N	7
MC2002F	SNG232U	SN74H62W	7
MC2002L, P	SNG232J, N	SN74H62J, N	7
MC2003F	SNG242U	SN74H20W	7
MC2003L, P	SNG242J, N	SN74H20J, N	7
MC2004F	SNG252U	SN74H53W	7
MC2004L, P	SNG252J, N	SN74H53J, N	7
MC2005F	SNG262U	SN74H30W	7
MC2005L, P	SNG262J, N	SN74H30J, N	7
MC2006F	SNG272U	SN74H60W	7
MC2006L, P	SNG272J, N	SN74H60J, N	7
MC2007F	SNG322U	SN74H10W	7
MC2007L, P	SNG322J, N	SN74H10J, N	7
MC2008F		SN74H04W	7
MC2008L, P		SN74H04J, N	7
MC2009F	SNF252U	SN74H102W	7
MC2009L, P	SNF252J, N	SN74H102J, N	7
MC2010F	SNF262U	SN74H101W	7
MC2010L, P	SNF262J, N	SN74H101J, N	7
MC2011F	SNG202U	SN74H30W	7
MC2011L, P	SNG202J, N	SN74H30J, N	7
MC2012F	SNG302U	SN74H53W	7
MC2012L, P	SNG302J, N	SN74H53J, N	7
MC2013F	SNG312U	SN74H50W	7
MC2013L, P	SNG312J, N	SN74H50J, N	7
MC2023F	SNF122U	SN74H103W	7
MC2023L, P	SNF122J, N	SN74H103J, N	7
MC2024F	SNF132U	SN74H108W	7
MC2024L, P	SNF132J, N	SN74H108J, N	7
MC2025F	SNF202U	SN74H102W	7
MC2025L, P	SNF202J, N	SN74H102J, N	7
MC2026F	SNF212U	SN74H101W	7
MC2026L, P	SNF212J, N	SN74H101J, N	7
MC2028F		SN74H101W	7
MC2028L, P		SN74H101J, N	7
MC2050F	SNG213U	SN74H55W	7
MC2050L, P	SNG213J, N	SN74H55J, N	7
MC2051F	SNG223U	SN74H00W	7
MC2051L, P	SNG223J, N	SN74H00J, N	7
MC2052F	SNG233U	SN74H62W	7
MC2052L, P	SNG233J, N	SN74H62J, N	7
MC2053F	SNG243U	SN74H20W	7
MC2053L, P	SNG243J, N	SN74H20J, N	7
MC2054F	SNG253U	SN74H53W	7
MC2054L, P	SNG253J, N	SN74H53J, N	7
MC2055F	SNG263U	SN74H30W	7
MC2055L, P	SNG263J, N	SN74H30J, N	7
MC2056F	SNG273U	SN74H60W	7
MC2056L, P	SNG273J, N	SN74H60J, N	7
MC2057F	SNG323U	SN74H10W	7
MC2057L, P	SNG323J, N	SN74H10J, N	7
MC2058F		SN74H04W	7
MC2058L, P		SN74H04J, N	7
MC2059F	SNF253U	SN74H102W	7
MC2059L, P	SNF253J, N	SN74H102J, N	7
MC2060F	SNF263U	SN74H101W	7
MC2060L, P	SNF263J, N	SN74H101J, N	7
MC2061F	SNG203U	SN74H30W	7
MC2061L, P	SNG203J, N	SN74H30J, N	7
MC2062F	SNG303U	SN74H53W	7
MC2062L, P	SNG303J, N	SN74H53J, N	7
MC2063F	SNG313U	SN74H50W	7
MC2063L, P	SNG313J, N	SN74H50J, N	7

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MC2073F	SNF123U	SN74H103W	7
MC2073L, P	SNF123J, N	SN74H103J, N	7
MC2074F	SNF133U	SN74H108W	7
MC2074L, P	SNF133J, N	SN74H108J, N	7
MC2075F	SNF203U	SN74H102W	7
MC2075L, P	SNF203J, N	SN74H102J, N	7
MC2076F	SNF213U	SN74H101W	7
MC2076L, P	SNF213J, N	SN74H101J, N	7
MC2078F		SN74H101W	7
MC2078L, P		SN74H101J, N	7
MC2100F	SNG210U	SN54H55W	7
MC2100L	SNG210J, N	SN54H55J, N	7
MC2101F	SNG220U	SN54H00W	7
MC2101L	SNG220J, N	SN54H00J, N	7
MC2102F	SNG230U	SN54H62W	7
MC2102L	SNG230J, N	SN54H62J, N	7
MC2103F	SNG240U	SN54H20W	7
MC2103L	SNG240J, N	SN54H20J, N	7
MC2104F	SNG250U	SN54H53W	7
MC2104L	SNG250J, N	SN54H53J, N	7
MC2105F	SNG260U	SN54H30W	7
MC2105L	SNG260J, N	SN54H30J, N	7
MC2106F	SNG270U	SN54H60W	7
MC2106L	SNG270J, N	SN54H60J, N	7
MC2107F	SNG370U	SN54H10W	7
MC2107L	SNG320J, N	SN54H10J, N	7
MC2108F		SN54H04W	7
MC2108L		SN54H04J, N	7
MC2109F	SNF250U	SN54H102W	7
MC2109L	SNF250J, N	SN54H102J, N	7
MC2110F	SNF260U	SN54H101W	7
MC2110L	SNF260J, N	SN54H101J, N	7
MC2111F	SNG200U	SN54H30W	7
MC2111L	SNG200J, N	SN54H30J, N	7
MC2112F	SNG300U	SN54H53W	7
MC2112L	SNG300J, N	SN54H53J, N	7
MC2113F	SNG310U	SN54H50W	7
MC2113L	SNG310J, N	SN54H50J, N	7
MC2123F	SNF120U	SN54H103W	7
MC2123L	SNF120J, N	SN54H103J, N	7
MC2124F	SNF130U	SN54H108W	7
MC2124L	SNF130J, N	SN54H108J, N	7
MC2125F	SNF200U	SN54H102W	7
MC2125L	SNF200J, N	SN54H102J, N	7
MC2126F	SNF210U	SN54H101W	7
MC2126L	SNF210J, N	SN54H101J, N	7
MC2128F		SN54H101W	7
MC2128L		SN54H101J, N	7
MC2150F	SNG211U	SN54H55W	7
MC2150L	SNG211J, N	SN54H55J, N	7
MC2151F	SNG221U	SN54H00W	7
MC2151L	SNG221J, N	SN54H00J, N	7
MC2152F	SNG231U	SN54H62W	7
MC2152L	SNG231J, N	SN54H62J, N	7
MC2153F	SNG241U	SN54H20W	7
MC2153L	SNG241J, N	SN54H20J, N	7
MC2154F	SNG251U	SN54H53W	7
MC2154L	SNG251J, N	SN54H53J, N	7
MC2155F	SNG251U	SN54H30W	7
MC2155L	SNG261J, N	SN54H30J, N	7
MC2156F	SNG271U	SN54H60W	7
MC2156L	SNG271J, N	SN54H60J, N	7
MC2157F	SNG321U	SN54H10W	7
MC2157L	SNG321J, N	SN54H10J, N	7
MC2158F		SN54H04W	7
MC2158L		SN54H04J, N	7
MC2159F	SNF251U	SN54H102W	7
MC2159L	SNF251J, N	SN54H102J, N	7

DTL/TTL CIRCUITS

Motorola TTL, Cont.

B

Type Number	Direct Replacement	Recommended for New Designs	Sec.
MC2160F	SNF261U	SN54H101W	7
MC2160L	SNF261J, N	SN54H101J, N	7
MC2161F	SNG201U	SN54H30W	7
MC2161L	SNG201J, N	SN54H30J, N	7
MC2162F	SNG301U	SN54H53W	7
MC2162L	SNG301J, N	SN54H53J, N	7
MC2163F	SNG311U	SN54H50W	7
MC2163L	SNG311J, N	SN54H50J, N	7
MC2173F	SNF121U	SN54H103W	7
MC2173L	SNF121J, N	SN54H103J, N	7
MC2174F	SNF131U	SN54H108W	7
MC2174L	SNF131J, N	SN54H108J, N	7
MC2175F	SNF201U	SN54H102W	7
MC2175L	SNF201J, N	SN54H102J, N	7
MC2176F	SNF211U	SN54H101W	7
MC2176L	SNF211J, N	SN54H101J, N	7
MC2178F		SN54H101W	7
MC2178L		SN54H101J, N	7
MC3000F	SN74H00W	SN74H00W	7
MC3000L	SN74H00J, N	SN74H00J, N	7
MC3004F	SN74H01W	SN74H03W	7
MC3004L, P	SN74H01J, N	SN74H03J, N	7
MC3005F	SN74H10W	SN74H10W	7
MC3005L, P	SN74H10J, N	SN74H10J, N	7
MC3006F	SN74H11W	SN74H11W	7
MC3006L, P	SN74H11J, N	SN74H11J, N	7
MC3008F	SN74H04W	SN74H04W	7
MC3008F	SN74H04J, N	SN74H04J, N	7
MC3009F	SN74H05W	SN74H05W	7
MC3009L, P	SN74H05J, N	SN74H05J, N	7
MC3010F	SN74H20W	SN74H20W	7
MC3010L, P	SN74H20J, N	SN74H20J, N	7
MC3009F	SN74H05W	SN74H05W	7
MC3009L, P	SN74H05J, N	SN74H05J, N	7
MC3010F	SN74H20W	SN74H20W	7
MC3010L, P	SN74H20J, N	SN74H20J, N	7
MC3011F	SN74H21W	SN74H21W	7
MC3011L, P	SN74H21J, N	SN74H21J, N	7
MC3012F	SN74H22W	SN74H22W	7
MC3012L, P	SN74H22J, N	SN74H22J, N	7
MC3016F	SN74H30W	SN74H30W	7
MC3016L, P	SN74H30J, N	SN74H30J, N	7
MC3018F	SN74H62W	SN74H62W	7
MC3018L, P	SN74H62J, N	SN74H62J, N	7
MC3019F	SN74H61W	SN74H61W	7
MC3019L, P	SN74H61J, N	SN74H61J, N	7
MC3020F	SN74H50W	SN74H50W	7
MC3020L, P	SN74H50J, N	SN74H50J, N	7
MC3021F	SN7486W	SN7486W	9
MC3021L,	SN7486J, N	SN7486J, N	9
MC3023F	SN74H51W	SN74H51W	7
MC3023L, P	SN74H51J, N	SN74H51J, N	7
MC3024F	SN74H40W	SN74H40W	7
MC3024L, P	SN74H40J, N	SN74H40J, N	7
MC3025F	SN74H40W	SN74H40W	7
MC3025L, P	SN74H40J, N	SN74H40J, N	7
MC3030F	SN74H60W	SN74H60W	7
MC3030L, P	SN74H60J, N	SN74H60J, N	7
MC3031F	SN74H52W	SN74H52W	7
MC3031L, P	SN74H52J, N	SN74H52J, N	7
MC3032F	SN74H53W	SN74H53W	7
MC3032L, P	SN74H53J, N	SN74H53J, N	7
MC3033F	SN74H54W	SN74H54W	7
MC3033L, P	SN74H54J, N	SN74H54J, N	7
MC3034F	SN74H55W	SN74H55W	7
MC3034L, P	SN74H55J, N	SN74H55J, N	7
MC3050F		SN74H72W	7
MC3050L, P		SN74H72J, N	7

Type Number	Direct Replacement	Recommended for New Designs	Sec.
MC3051F		SN74H102W	7
MC3051L, P		SN74H102J, N	7
MC3052F		SN74H102W	7
MC3052L, P		SN74H102J, N	7
MC3054F	SN74H71W	SN74H71W	7
MC3054L, P	SN74H71J, N	SN74H71J, N	7
MC3055F	SN74H72W	SN74H72W	7
MC3055L, P	SN74H72J, N	SN74H72J, N	7
MC3060F	SN74H74W	SN74H74W	7
MC3060L, P	SN74H74J, N	SN74H74J, N	7
MC3061F	SN74S114W	SN74S114W	5
MC3061L, P	SN74S114J, N	SN74S114J, N	5
MC3062F	SN74S113W	SN74S113W	5
MC3062L, P	SN74S113J, N	SN74S113J, N	5
MC3100F	SN54H00W	SN54H00W	7
MC3100L	SN54H00J, N	SN54H00J, N	7
MC3104F	SN54H01W	SN54H01W	7
MC3104L	SN54H01J, N	SN54H01J, N	7
MC3105F	SN54H10W	SN54H10W	7
MC3105L	SN54H10J, N	SN54H10J, N	7
MC3106F	SN54H11W	SN54H11W	7
MC3106L	SM54H11J, N	SN54H11J, N	7
MC3108F	SN54H04W	SN54H04W	7
MC3108L	SN54H04J, N	SN54H04J, N	7
MC3109F	SN54H05W	SN54H05W	7
MC3109L	SN54H05J, N	SN54H05J, N	7
MC3110F	SN54H20W	SN54H20W	7
MC3110L	SN54H20J, N	SN54H20J, N	7
MC3111F	SN54H21W	SN54H21W	7
MC3111L	SN54H21J, N	SN54H21J, N	7
MC3112F	SN54H22W	SN54H22W	7
MC3112L	SN54H22J, N	SN54H22J, N	7
MC3116F	SN54H30W	SN54H30W	7
MC3116L	SN54H30J, N	SN54H30J, N	7
MC3118F	SN54H62W	SN54H62W	7
MC3118L	SN54H62J, N	SN54H62J, N	7
MC3119F	SN54H61W	SN54H61W	7
MC3119L	SN54H61J, N	SN54H61J, N	7
MC3120F	SN54H50W	SN54H50W	7
MC3120L	SN54H50J, N	SN54H50J, N	7
MC3121F	SN5486W	SN5486W	9
MC3121L	SN5486J, N	SN5486J, N	9
MC3123F	SN54H51W	SN54H51W	7
MC3123L	SN54H51J, N	SN54H51J, N	7
MC3124F	SN54H40W	SN54H40W	7
MC3124L	SN54H40J, N	SN54H40J, N	7
MC3125F	SN54H40W	SN54H40W	7
MC3125L	SN54H40J, N	SN54H40J, N	7
MC3130F	SN54H60W	SN54H60W	7
MC3130L	SN54H60J, N	SN54H60J, N	7
MC3131F	SN54H52W	SN54H52W	7
MC3131L	SN54H52J, N	SN54H52J, N	7
MC3132F	SN54H53W	SN54H53W	7
MC3132L	SN54H53J, N	SN54H53J, N	7
MC3133F	SN54H54W	SN54H54W	7
MC3133L	SN54H54J, N	SN54H54J, N	7
MC3134F	SN54H55W	SN54H55W	7
MC3134L	SN54H55J, N	SN54H55J, N	7
MC3150F		SN54H72W	7
MC3150L		SN54H72J, N	7
MC3151F		SN54H102W	7
MC3151L		SN54H102J, N	7
MC3152F		SN54H102W	7
MC3152L		SN54H102J, N	7
MC3154F	SN54H71W	SN54H71W	7
MC3154L	SN54H71J, N	SN54H71J, N	7
MC3155F	SN54H72W	SN54H72W	7
MC3155L	SN54H72J, N	SN54H72J, N	7

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DTL/TTL CIRCUITS

Motorola TTL, Cont.

Type Number	Direct Replacement	Recommended for New Designs	Sec.
MC3160F	SN54H74W	SN54H74W	7
MC3160L	SN54H74J, N	SN54H74J, N	7
MC3161F	SN54S114W	SN54S114W	5
MC3161L	SN54S114J, N	SN54S114J, N	5
MC3162F	SN54S113W	SN54S113W	5
MC3162L	SN54S113J, N	SN54S113J, N	5
MC5400F	SN5400W	SN5400W	6
MC5400L	SN5400J, N	SN5400J, N	6
MC5401F	SN5401W	SN5401W	6
MC5401L	SN5401J, N	SN5401J, N	6
MC5402F	SN5402W	SN5402W	6
MC5402L	SN5402J, N	SN5402J, N	6
MC5403L	SN5403J, N	SN5403J, N	6
MC5404F	SN5404W	SN5404W	6
MC5404L	SN5404J, N	SN5404J, N	6
MC5405F	SN5405W	SN5405W	6
MC5405L	SN5405J, N	SN5405J, N	6
MC5410F	SN5410W	SN5410W	6
MC5410L	SN5410J, N	SN5410J, N	6
MC5420F	SN5420W	SN5420W	6
MC5420L	SN5420J, N	SN5420J, N	6
MC5430F	SN5430W	SN5430W	6
MC5430L	SN5430J, N	SN5430J, N	6
MC5440F	SN5440W	SN5440W	6
MC5440L	SN5440J, N	SN5440J, N	6
MC5442L	SN5442J, N	SN5442J, N	9
MC5443L	SN5443J, N	SN5443J, N	9
MC5444L	SN5444J, N	SN5444J, N	9
MC5445L	SN5445J, N	SN5445J, N	9
MC5446L	SN5446AJ, N	SN5446AJ, N	9
MC5447L	SN5447AJ, N	SN5447AJ, N	9
MC5450F	SN5450W	SN5450W	6
MC5450L	SN5450J, N	SN5450J, N	6
MC5451F	SN5451W	SN5451W	6
MC5451L	SN5451J, N	SN5451J, N	6
MC5453F	SN5453W	SN5453W	6
MC5453L	SN5453J, N	SN5453J, N	6
MC5454F	SN5454W	SN5454W	6
MC5454L	SN5454J, N	SN5454J, N	6
MC5460F	SN5460W	SN5460W	6
MC5460L	SN5460J, N	SN5460J, N	6
MC5472F	SN5472W	SN5472W	6
MC5472L	SN5472J, N	SN5472J, N	6
MC5473F	SN5473W	SN5473W	6
MC5473L	SN5473J, N	SN5473J, N	6
MC5480L	SN5480J, N	SN5480J, N	9
SN5483L	SN5483J, N	SN5483J, N	9
MC5490L	SN5490W	SN5490W	9
MC5490L	SN5490J, N	SN5490J, N	9
MC5491AL	SN5491AJ, N	SN5491AJ, N	9
MC5492F	SN5492W	SN5492W	9
MC5492L	SN5492J, N	SN5492J, N	9
MC5493L	SN5493J, N	SN5493J, N	9
MC5494L	SN5494J, N	SN5494J, N	9
MC5495F	SN5495AW	SN5495AW	9
MC5495L	SN5495AJ, N	SN5495AJ, N	9
MC5496L	SN5496J, N	SN5496J, N	9
MC15842L	SN5482J, N	SN5482J, N	9
MC54107L	SN54107J, N	SN54107J, N	6
MC54121F	SN54121W	SN54121W	6
MC54121L	SN54121J, N	SN54121J, N	6
MC54150L	SN54150J, N	SN54150J, N	9
MC54151L	SN54151J, N	SN54151J, N	9
MC54192L	SN54192J, N	SN54192J, N	9
MC54193L	SN54193J, N	SN54193J, N	9
MC7400F	SN7400W	SN7400W	6
MC7400L, P	SN7400J, N	SN7400J, N	6
MC7401F	SN7401W	SN7401W	6
MC7401L, P	SN7401J, N	SN7401J, N	6
MC7402F	SN7402W	SN7402W	6
MC7402L, P	SN7402J, N	SN7402J, N	6
MC7403L, P	SN7403J, N	SN7403J, N	6
MC7404F	SN7404W	SN7404W	6
MC7404L, P	SN7404J, N	SN7404J, N	6
MC7405F	SN7405W	SN7405W	6
MC7405L, P	SN7405J, N	SN7405J, N	6
MC7410F	SN7410W	SN7410W	6
MC7410L, P	MC7410J, N	SN7410J, N	6
MC7420F	SN7420W	SN7420W	6
MC7420L, P	SN7420J, N	SN7420J, N	6
MC7430F	SN7430W	SN7430W	6
MC7430L, P	SN7430J, N	SN7430J, N	6
MC7440F	SN7440W	SN7440W	6
MC7440L, P	SN7440J, N	SN7440J, N	6
MC7441AL, P	SN74141J, N	SN74141J, N	9
MC7442L, P	SN7442J, N	SN7442J, N	9
MC7443L, P	SN7443J, N	SN7443J, N	9
MC7444L, P	SN7444J, N	SN7444J, N	9
MC7445L, P	SN7445J, N	SN7445J, N	9
MC7446L, P	SN7446AJ, N	SN7446AJ, N	9
MC7447L, P	SN7447AJ, N	SN7447AJ, N	9
MC7450F	SN7450W	SN7450W	6
MC7450L, P	SN7450J, N	SN7450J, N	6
MC7451F	SN7451W	SN7451W	6
MC7451L, P	SN7451J, N	SN7451J, N	6
MC7453F	SN7453W	SN7453W	6
MC7453L, P	SN7453J, N	SN7453J, N	6
MC7454F	SN7454W	SN7454W	6
MC7454L, P	SN7454J, N	SN7454J, N	6
MC7460F	SN7460W	SN7460W	6
MC7460L, P	SN7460J, N	SN7460J, N	6
MC7472F	SN7472W	SN7472W	6
MC7472L, P	SN7472J, N	SN7472J, N	6
MC7473F	SN7473W	SN7473W	6
MC7473L, P	SN7473J, N	SN7473J, N	6
MC7480L, P	SN7480J, N	SN7480J, N	9
SN7483L, P	SN7483J, N	SN7483J, N	9
MC7490F	SN7490W	SN7490W	9
MC7490L, P	SN7490J, N	SN7490J, N	9
MC7491AL, P	SN7491AJ, N	SN7491AJ, N	9
MC7492F	SN7492W	SN7492W	9
MC7492L, P	SN7492J, N	SN7492J, N	9
MC7493L, P	SN7493J, N	SN7493J, N	9
SN7494L, P	SN7494J, N	SN7494J, N	9
SN7495F	SN7495AW	SN7495AW	9
SN7495L, P	SN7495AJ, N	SN7495AJ, N	9
SN7496L, P	SN7496J, N	SN7496J, N	9
MC17482L	SN7482J, N	SN7482J, N	9
MC74107L, P	SN74107J, N	SN74107J, N	6
MC74121F	SN74121W	SN74121W	6
MC74121L, P	SN74121J, N	SN74121J, N	6
MC74150L	SN74150J, N	SN74150J, N	9
MC74151L, P	SN74151J, N	SN74151J, N	9
MC74192L, P	SN74192J, N	SN74192J, N	9
MC74193L, P	SN74193J, N	SN74193J, N	9

DTL/TTL CIRCUITS

Motorola Complex Functions

B

Type Number	Direct Replacement	Recommended For New Designs	Sec.
MC4000F		SN74153W	9
MC4000L, P		SN74153J, N	9
MC4001L, P		SN74184J, N or SN74185A,J, N	9
MC4002F		SN74155W	9
MC4002L, P		SN74155J, N	9
MC4004F	SN7481W	SN7481W	9
MC4004L, P	SN7481J, N	SN7481J, N	9
MC4005F	SN7481W	SN7481W	9
MC4005L, P	SN7481J, W	SN7481J, N	9
MC4006F		SN74155W	9
MC4006L, P		SN74155J, N	9
MC4007L, P		SN74155J, N	9
MC4008F		SN74180W	9
MC4008L, P		SN74180J, N	9
MC4010F		SN74180W	9
MC4010L, P		SN74180J, N	9
MC4012F		SN7495AW	9
MC4012L, P		SN7495AJ, N	9
MC4015L, P		SN7475J, N	9
MC4016L, P		SN74190J, N	9
MC4018L, P		SN74191J, N	9
MC4023F		SN7492W	9
MC4023L, P		SN7492J, N	9
MC4026F		SN74H183W	9
MC4026L, P		SN74H183J, N	9
MC4027F		SN74H183W	9
MC4027L, P		SN74H183J, N	9
MC4028F		SN74181W	9
MC4028L, P		SN74181J, N	9
MC4029F		SN74181W	9
MC4029L, P		SN74181J, N	9
MC4030F		SN74181W	9
MC4030L, P		SN74181J, N	9
MC4031F		SN74181W	9
MC4031L, P		SN74181J, N	9
MC4032F		SN74182W	9
MC4032L, P		SN74182J, N	9
MC4035F		SN7475W	9
MC4035L, P		SN7475J, N	9
MC4037F		SN7475W	9
MC4037L, P		SN7415J, N	9
MC4039P		SN7448J, N	9
MC4304F	SN5481W	SN5481W	9
MC4304L	SN5481J, N	SN5481J, N	9
MC4305F	SN5481W	SN5481W	9
MC4305L	SN5481J, N	SN5481J, N	9
MC316L, P		SN54190J, N	9
MC4318L, P		SN54191J, N	9
MC4326F		SN54H183W	9
MC4326L		SN54H183J, N	9
MC4327F		SN54H183W	9
MC4327L		SN54H183J, N	9
MC4328F		SN54181W	9
MC4328L		SN54181J, N	9
MC4329F		SN54181W	9
MC4329L		SN54181J, N	9
MC4330F		SN54181W	9
MC4330L		SN54181J, N	9
MC4331F		SN54181W	9
MC4331L		SN54181J, N	9
MC4332F		SN54182W	9
MC4332L		SN54182J, N	9
MC4335F		SN5475W	9
MC4335L, P		SN5475J, N	9
MC4337F		SN5475W	9
MC4337L, P		SN5475J, N	9
MC8300L, P	SN74195J, N	SN74195J, N	9
MC8301L, P		SN7442J, N	9
MC8304L, P		SN7482J, N	9
MC8309L, P		SN74153J, N	9
MC8312L, P		SN74151J, N	9
MC8601F	SN74122W	SN74122W	6
MC8601L, P	SN74122J, N	SN74122J, N	6
MC9300L	SN54195J, N	SN54195J, N	9
MC9301L		SN5442J, N	9
MC9304L		SN5482J, N	9
MC9309L		SN54153J, N	9
MC9312L		SN54151J, N	9
MC9601F	SN54122W	SN54122W	6
MC9601L	SN54122J, N	SN54122J, N	6

National DTL

Type Number	Direct Replacement	Recommended For New Designs	Sec.
DM930N	SN15830J, N	SN7420J, N	6
DM932N	SN15832J, N	SN7440J, N	6
DM933N	SN15833J, N	SN7460J, N	6
DM935N	SN15840J, N	SN7405J, N	6
DM936N	SN15836J, N	SN7405J, N	6
DM937N	SN15837J, N	SN7405J, N	6
DM944N	SN15844J, N	SN7440J, N	6
DM945N	SN15845J, N	SN74110J, N	6
DM946N	SN15846J, N	SN7400J, N	6
DM948N	SN15848J, N	SN74110J, N	6
DM949N	SN15849J, N	SN7400J, N	6
DM957N	SN15857J, N	SN7437J, N	6
DM958N	SN15858J, N	SN7437J, N	6
DM961N	SN15861J, N	SN7420J, N	6
DM962N	SN15862J, N	SN7410J, N	6
DM963N	SN15863J, N	SN7410J, N	6
DM1800N	SN151800J, N	SN7420J, N	6
DM1801N	SN151801J, N	SN7420J, N	6
DM9093N	SN158093J, N	SN7473J, N	6
DM9094N	SN158094J, N	SN7473J, N	6
DM9097N	SN158097J, N	SN7476J, N	6
DM9099N	SN158099J, N	SN7476J, N	6

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Type Number†	Direct Replacement	Recommended for New Designs	Sec.
DM5400D, N (7000)	SN5400J, N	SN5400J, N	6
DM5401D, N (7001)	SN5401J, N	SN5401J, N	6
DM5402D, N (7002)	SN5402J, N	SN5402J, N	6
DM5403D, N (7003)	SN5403J, N	SN5403J, N	6
DM5404D, N (7004)	SN5404J, N	SN5404J, N	6
DM5405D, N (7005)	SN5405J, N	SN5405J, N	6
DM5408D, N (7008)	SN5408J, N	SN5408J, N	6
DM5409D, N (7009)	SN5409J, N	SN5409J, N	6
DM5410D, N (7010)	SN5410J, N	SN5410J, N	6
DM5420D, N (7020)	SN5420J, N	SN5420J, N	6
DM5430D, N (7030)	SN5430J, N	SN5430J, N	6
DM5440D, N (7040)	SN5440J, N	SN5440J, N	6
DM5442D, N (7842)	SN5442J, N	SN5442J, N	9
DM5446D, N (7846)	SN5446AJ, N	SN5446AJ, N	9
DM5447D, N (7847)	SN5447AJ, N	SN5447AJ, N	9
DM5448D, N (7848)	SN5448J, N	SN5448J, N	9
DM5450D, N (7050)	SN5450J, N	SN5450J, N	6
DM5451D, N (7051)	SN5451J, N	SN5451J, N	6
DM5453D, N (7053)	SN5453J, N	SN5453J, N	6
DM5454D, N (7054)	SN5454J, N	SN5454J, N	6
DM5460D, N (7060)	SN5460J, N	SN5460J, N	6
DM5472D, N (7540)	SN5472J, N	SN5472J, N	6
DM5473D, N (7501)	SN5473J, N	SN5473J, N	6
DM5474D, N (7510)	SN5474J, N	SN5474J, N	6
DM5475D, N (7550)	SN5475J, N	SN5475J, N	9
DM5476D, N (7500)	SN5476J, N	SN5476J, N	6
DM5483D, N (7283)	SN5483J, N	SN5483J, N	9
DM5486D, N (7086)	SN5486J, N	SN5486J, N	9
DM5488D, N (7588)	SN5488J, N	SN5488J, N	9
DM5490D, N (7530)	SN5490J, N	SN5490J, N	9
DM5491AD, N	SN5491AJ, N	SN5491AJ, N	9
DM5492D, N (7532)	SN5492J, N	SN5492J, N	9
DM5493D, N (7533)	SN5493J, N	SN5493J, N	9
DM5495D, N (7580)	SN5495AJ, N	SN5495AJ, N	9
DM54107D, N (7502)	SN54107J, N	SN54107J, N	6
DM54121D, N	SN54121J, N	SN54121J, N	6
DM54153D, N (7212)	SN54153J, N	SN54153J, N	9
DM54154D, N (7213)	SN54154J, N	SN54154J, N	9
DM7200D, N		SN5485J, N	9
DM7210D, N		SN54151J, N	9
DM7220D, N		SN54180J, N	9
DM7280D, N (8680)		SN54196J, N	9
DM7281D, N (8681)		SN54197J, N	9
DM7288D, N (8688)		SN54197J, N	9
DM7400D, N (8000)	SN7400J, N	SN7400J, N	6
DM7401D, N (8001)	SN7401J, N	SN7401J, N	6
DM7402D, N (8002)	SN7402J, N	SN7402J, N	6
DM7403D, N (8003)	SN7403J, N	SN7403J, N	6
DM7404D, N (8004)	SN7404J, N	SN7404J, N	6
DM7405D, N (8005)	SN7405J, N	SN7405J, N	6
DM7408D, N (8008)	SN7408J, N	SN7408J, N	6
DM7409D, N (8009)	SN7409J, N	SN7409J, N	6
DM7410D, N (8010)	SN7410J, N	SN7410J, N	6
DM7420D, N (8020)	SN7420J, N	SN7420J, N	6
DM7430D, N (8030)	SN7430J, N	SN7430J, N	6
DM7440D, N (8040)	SN7440J, N	SN7440J, N	6
DM7441D, N (8841)	SN74141J, N	SN74141J, N	9
DM7442D, N (8842)	SN7442J, N	SN7442J, N	9
DM7446D, N (8846)	SN7446AJ, N	SN7446AJ, N	9
DM7447D, N (8847)	SN7447AJ, N	SN7447AJ, N	9
DM7448D, N (8848)	SN7448J, N	SN7448J, N	9
DM7450D, N (8050)	SN7450J, N	SN7450J, N	6
DM7451D, N (8051)	SN7451J, N	SN7451J, N	6
DM7453D, N (8053)	SN7453J, N	SN7453J, N	6
DM7454D, N (8054)	SN7454J, N	SN7454J, N	6
DM7460D, N (8060)	SN7460J, N	SN7460J, N	6
DM7472D, N (8540)	SN7472J, N	SN7472J, N	6
DM7473D, N (8501)	SN7473J, N	SN7473J, N	6
DM7474D, N (8510)	SN7474J, N	SN7474J, N	6
DM7475D, N (8550)	SN7475J, N	SN7475J, N	9
DM7476D, N (8500)	SN7476J, N	SN7476J, N	6
DM7483D, N (8283)	SN7483J, N	SN7483J, N	9
DM7486D, N (8086)	SN7486J, N	SN7486J, N	9
DM7488D, N (8588)	SN7488J, N	SN7488J, N	9
DM7490D, N (8530)	SN7490J, N	SN7490J, N	9
DM7491AD, N	SN7491AJ, N	SN7491AJ, N	9
DM7492D, N (8532)	SN7492J, N	SN7492J, N	9
DM7493D, N (8533)	SN7493J, N	SN7493J, N	9
DM7495D, N (8580)	SN7495AJ, N	SN7495AJ, N	9
DM74107D, N (8502)	SN74107J, N	SN74107J, N	6
DM74121D, N	SN74121J, N	SN74121J, N	6
DM74153D, N (8212)	SN74153J, N	SN74153J, N	9
DM74154D, N (8213)	SN74154J, N	SN74154J, N	9
DM7520D, N		SN5497J, N	9
DM7551D, N		SN5475J, N	9
DM7560D, N	SN54192J, N	SN54192J, N	9
DM7563D, N	SN54193J, N	SN54193J, N	9
DM7570D, N	SN54164J, N	SN54164J, N	9
DM7588D, N	SN5488J, N	SN5488J, N	9
DM7590D, N	SN54165J, N	SN54165J, N	9
DM7598D, N		SN5488J, N	9
DM7599D, N		SN5489J, N	9
DM8200D, N		SN7485J, N	9
DM8210D, N		SN74151J, N	9
DM8220D, N		SN74180J, N	9
DM8280D, N (7680)		SN54196J, N	9
DM8281D, N (7681)		SN54197J, N	9
DM8288D, N (7688)		SN54197J, N	9
DM8300D, N (8600)	SN74195J, N	SN74195J, N	9
DM8311D, N (8213)	SN74154J, N	SN74154J, N	9
DM8520D, N		SN7497J, N	9
DM8551D, N		SN7475J, N	9
DM8560D, N	SN74192J, N	SN74192J, N	9
DM8563D, N	SN74193J, N	SN74193J, N	9
DM8570D, N	SN74164J, N	SN74164J, N	9
DM8588D, N	SN7488J, N	SN7488J, N	9
DM8590D, N	SN74165J, N	SN74165J, N	9
DM8598D, N		SN7488J, N	9
DM8599D, N		SN7489J, N	9
DM8601D, N (8850)	SN74122J, N	SN74122J, N	6
DM9300D, N (7600)	SN54195J, N	SN54195J, N	9
DM9311D, N (7213)	SN54154J, N	SN54154J, N	9
DM9601D, N (7850)	SN54122J, N	SN54122J, N	6

†Number in parentheses is an obsolete type number.

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Type Number	Direct Replacement	Recommended For New Designs	Sec.
RC930D, P	SN15830J, N	SN7420J, N	6
RC930J	SN15830U	SN7420W	6
RC932D, P	SN15832J, N	SN7440J, N	6
RC932J	SN15832U	SN7440W	6
RC933D, P	SN15833J, N	SN7460J, N	6
RC933J	SN15833U	SN7460W	6
RC934D, P	SN15834J, N	SN7405J, N	6
RC934J	SN15834U	SN7405W	6
RC935D, P	SN15838J, N	SN7405J, N	6
RC935J	SN15838U	SN7405W	6
RC936D, P	SN15836J, N	SN7405J, N	6
RC936J	SN15836U	SN7405W	6
RC937D, P	SN15837J, N	SN7405J, N	6
RC937J	SN15837U	SN7405W	6
RC940D, P	SN15835J, N	SN7405J, N	6
RC940J	SN15835U	SN7405W	6
RC941D, P	SN15841J, N		11
RC941J	SN15841U		11
RC944D, P	SN15844J, N	SN7440J, N	6
RC944J	SN15844U	SN7440W	6
RC945D, P	SN15845J, N	SN74110J, N	6
RC945J	SN15845U	SN74110W	6
RC946D, P	SN15846J, N	SN7400J, N	6
RC946J	SN15846U	SN7400W	6
RC948D, P	SN15848J, N	SN74110J, N	6
RC948J	SN15848U	SN74110W	6
RC949D, P	SN15849J, N	SN7400J, N	6
RC949J	SN15849U	SN7400W	6
RC950D, P	SN15850J, N	SN74110J, N	6
RC950J	SN15850U	SN74110W	6
RC951D, P	SN15851J, N	SN74121J, N	6
RC951J	SN15851U	SN74121W	6
RC957J	SN15857J, N	SN7437J, N	6
RC957J	SN15857U	SN7437W	6
RC958D, P	SN15858J, N	SN7437J, N	6
RC958J	SN15858U	SN7437W	6
RC961D, P	SN15861J, N	SN7420J, N	6
RC961J	SN15861U	SN7420W	6
RC962D, P	SN15862J, N	SN7410J, N	6
RC962J	SN15862U	SN7410W	6
RC9630D, P	SN15863J, N	SN7410J, N	6
RC963J	SN15863U	SN7410W	6
RC993D, P	SN158093J, N	SN7473J, N	6
RC993J	SN158093U	SN7473W	6
RC994D, P	SN158094J, N	SN7473J, N	6
RC994J	SN158094U	SN7473W	6
RC997D, P	SN158097J, N	SN7476J, N	6
RC997J	SN158097U	SN7476W	6
RC999D, P	SN158099J, N	SN7476J, N	6
RC999J	SN158099U	SN7476W	6
RC1900D, P	SN151800J, N	SN7420J, N	6
RC1900J	SN151800U	SN7420W	6
RC1901D, P	SN151801J, N	SN7420J, N	6
RC1901J	SN151801U	SN7420W	6
RC1902D, P	SN151802J, N	SN7430J, N	6
RC1902J	SN151802U	SN7430W	6
RC1903D, P	SN151803J, N	SN7430J, N	6
RC1903J	SN151803U	SN7430W	6
RC1904D, P	SN151804J, N	SN7430J, N	6
RC1904J	SN151804U	SN7430J, N	6
RC1905D, P	SN151805J, N	SN7430J, N	6
RC1905J	SN151805U	SN7430W	6

Type Number	Direct Replacement	Recommended for New Designs	Sec.
RM930D, P	SN15930J, N	SN5420J, N	6
RM930J	SN15930U	SN5420J, N	6
RM932D, P	SN15932J, N	SN5440J, N	6
RM932J	SN15932U	SN5440W	6
RM933D, P	SN15933J, N	SN5460J, N	6
RM933J	SN15933U	SN5460W	6
RM934D, P	SN15934J, N	SN5405J, N	6
RM934J	SN15934U	SN5405W	6
RM935D, P	SN15938J, N	SN5405J, N	6
RM935J	SN15938U	SN5405W	6
RM936D, P	SN15936J, N	SN5405J, N	6
RM936J	SN15936U	SN5405W	6
RM937D, P	SN15937J, N	SN5405J, N	6
RM937J	SN15937U	SN5405W	6
RM940D, P	SN15935J, N	SN5405J, N	6
RM940J	SN15935U	SN5405W	6
RM941D, P	SN15941J, N		11
RM941J	SN15941U		11
RM944D, P	SN15944J, N	SN5440J, N	6
RM944J	SN15944U	SN5440W	6
RM945D, P	SN15945J, N	SN54110J, N	6
RM945J	SN15945U	SN54110W	6
RM946D, P	SN15946J, N	SN5400J, N	6
RM946J	SN15946U	SN5400W	6
RM948D, P	SN15948J, N	SN54110J, N	6
RM948J	SN15948U	SN54110W	6
RM949D, P	SN15949J, N	SN5400J, N	6
RM949J	SN15949U	SN5400W	6
RM950D, P	SN15950J, N	SN54110J, N	6
RM950J	SN15950U	SN54110W	6
RM951D, P	SN15951J, N	SN54121J, N	6
RM951J	SN15951U	SN54121W	6
RM957D, P	SN15957J, N	SN5437J, N	6
RM957J	SN15957U	SN5437W	6
RM958D, P	SN15958J, N	SN5437J, N	6
RM958J	SN15958U	SN5437W	6
RM961D, P	SN15961J, N	SN5420J, N	6
RM961J	SN15961U	SN5420W	6
RM962D, P	SN15962J, N	SN5410J, N	6
RM962J	SN15962U	SN5410W	6
RM963D, P	SN15963J, N	SN5410J, N	6
RM963J	SN15963U	SN5410W	6
RM993D, P	SN159093J, N	SN5473J, N	6
RM993J	SN159093U	SN5473W	6
RM994D, P	SN159094J, N	SN5473J, N	6
RM994J	SN159094U	SN5473W	6
RM997D, P	SN159097J, N	SN5476J, N	6
RM977J	SN159097U	SN5476W	6
RM999D, P	SN159099J, N	SN5476J, N	6
RM999J	SN159099U	SN5476W	6
RM1900D, P	SN151900J, N	SN5420J, N	6
RM1900J	SN151900U	SN5420W	6
RM1901D, P	SN151901J, N	SN5420J, N	6
RM1901J	SN151901U	SN5420W	6
RM1902D, P	SN151902J, N	SN5430J, N	6
RM1902J	SN151902U	SN5430W	6
RM1903D, P	SN151903J, N	SN5430J, N	6
RM1903J	SN151903U	SN5430W	6
RM1904D, P	SN151904J, N	SN5430J, N	6
RM1904J	SN151904U	SN5430W	6
RM1905D, P	SN151905J, N	SN5430J, N	6
RM1905J	SN151905U	SN5430W	6

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RF10D, P	SNF10J, N	SN5472J, N	6
RF10K	SNF10U	SN5472W	6
RF11D, P	SNF11J, N	SN5472J, N	6
RF11K	SNF11U	SN5472W	6
RF12D, P	SNF12J, N	SN7472J, N	6
RF12K	SNF12U	SN7472W	6
RF13D, P	SNF13J, N	SN7472J, N	6
RF13K	SNF13U	SN7472W	6
RF20D, P	SNF20J, N	SN5472J, N	6
RF20K	SNF20U	SN5472W	6
RF21D, P	SNF21J, N	SN5472J, N	6
RF21K	SNF21U	SN5472W	6
RF22D, P	SNF22J, N	SN7472J, N	6
RF22K	SNF22U	SN7472W	6
RF23D, P	SNF23J, N	SN7472J, N	6
RF23K	SNF23U	SN7472W	6
RF30D, P	SNF30J, N	SN54104J, N	6
RF30K	SNF30U	SN54104W	6
RF31D, P	SNF31J, N	SN54104J, N	6
RF31K	SNF31U	SN54104W	6
RF32D, P	SNF32J, N	SN74104J, N	6
RF32K	SNF32U	SN74104W	6
RF33D, P	SNF32J, N	SN74104J, N	6
RF33K	SNF32U	SN74104W	6
RF50D, P	SNF50J, N	SN5470J, N	6
RF50K	SNF50U	SN5470W	6
RF51D, P	SNF51J, N	SN5470J, N	6
RF51K	SNF51U	SN5470W	6
RF52D, P	SNF52J, N	SN7470J, N	6
RF52K	SNF52U	SN7470W	6
RF53D, P	SNF53J, N	SN7470J, N	6
RF53K	SNF53U	SN7470W	6
RF60D, P	SNF60J, N	SN54H101J, N	7
RF60K	SNF60U	SN54H101W	7
RF61D, P	SNF61J, N	SN54H101J, N	7
RF61K	SNF61U	SN54H101W	7
RF62D, P	SNF62J, N	SN74H101J, N	7
RF62K	SNF62U	SN74H101W	7
RF63D, P	SNF63J, N	SN74H101J, N	7
RF63K	SNF63U	SN74H101W	7
RF100D, P	SNF100J, N	SN54H103J, N	7
RF100K	SNF100U	SN54H103W	7
RF101D, P	SNF101J, N	SN54H103J, N	7
RF101K	SNF101U	SN54H103W	7
RF102D, P	SNF102J, N	SN74H103J, N	7
RF102K	SNF102U	SN74H103W	7
RF103D, P	SNF103J, N	SN74H103J, N	7
RF103K	SNF103U	SN74H103W	7
RF110D, P	SNF110J, N	SN54H108J, N	7
RF110K	SNF110U	SN54H108W	7
RF111D, P	SNF111J, N	SN54H108J, N	7
RF111K	SNF111U	SN54H108W	7
RF112D, P	SNF112J, N	SN74H108J, N	7
RF112K	SNF112U	SN74H108W	7
RF113K, P	SNF113J, N	SN74H108J, N	7
RF113K	SNF113U	SN74H108W	7
RF120D, P	SNF120J, N	SN54H103J, N	7
RF120K	SNF120U	SN54H103W	7
RF121D, P	SNF121J, N	SN54H103J, N	7
RF121K	SNF121U	SN54H103W	7
RF122D, P	SNF122J, N	SN74H103J, N	7
RF122K	SNF122U	SN74H103W	7
RF123D, P	SNF123J, N	SN74H103J, N	7
RF123K	SNF123U	SN74H103W	7
RF130D, P	SNF130J, N	SN54H108J, N	7
RF130K	SNF130U	SN54H108W	7
RF131D, P	SNF131J, N	SN54H108J, N	7
RF131K	SNF131U	SN54H108W	7
RF132D, P	SNF132J, N	SN74H108J, N	7
RF132K	SNG132U	SN74H108W	7
RF133D, P	SNF133J, N	SN74H108J, N	7
RF133K	SNF133U	SN74H108W	7
RF200D, P	SNF200J, N	SN54H102J, N	7
RF200K	SNF200U	SN54H102W	7
RF201D, P	SNF201J, N	SN54H102J, N	7
RF201K	SNF201U	SN54H102W	7
RF202D, P	SNF202J, N	SN74H102J, N	7
RF202K	SNF202U	SN74H102W	7
RF203D, P	SNF203J, N	SN74H102J, N	7
RF203K	SNF203U	SN74H102W	7
RF210D, P	SNF210J, N	SN54H101J, N	7
RF210K	SNF210U	SN54H101W	7
RF211D, P	SNF211J, N	SN54H101J, N	7
RF211K	SNF211U	SN54H101W	7
RF212D, P	SNF212J, N	SN74H101J, N	7
RF212K	SNF212U	SN74H101W	7
RF213D, P	SNF213J, N	SN74H101J, N	7
RF213K	SNF213U	SN74H101W	7
RF250D, P	SNF250J, N	SN54H102J, N	7
RF250K	SNF250U	SN54H102W	7
RF251D, P	SNF251J, N	SN54H102J, N	7
RF251K	SNF251U	SN54H102W	7
RF252D, P	SNF252J, N	SN74H102J, N	7
RF252K	SNF252U	SN74H102W	7
RF253D, P	SNF253J, N	SN74H102J, N	7
RF253K	SNF253U	SN74H102W	7
RF260D, P	SNF260J, N	SN54H101J, N	7
RF260K	SNF260U	SN54H101W	7
RF261D, P	SNF261J, N	SN54H101J, N	7
RF261K	SNF261U	SN54H101W	7
RF262D, P	SNF262J, N	SN74H101J, N	7
RF262K	SNF262U	SN74H101W	7
RF263D, P	SNF263J, N	SN74H101J, N	7
RF263K	SNF263U	SN74H101W	7
RF3120D, P		SN54S112J, N	5
RF3120K		SN54S112W	5
RF3122D, P		SN74S112J, N	5
RF3122K		SN74S112W	5
RF3130D, P		SN54S114J, N	5
RF3130K		SN54S114W	5
RF3132D, P		SN74S114J, N	5
RF3132K		SN74S114W	5
RF3200D, P		SN54S112J, N	5
RF3200K		SN54S112J, N	5
RF3202D, P		SN74S112J, N	5
RF3202K		SN74S112W	5
RF3210D, P		SN54S112J, N	5
RF3210K		SN54S112W	5
RF3212D, P		SN74S112J, N	5
RF3212K		SN74S112W	5
RF3220D, P		SN54S74J, N	5
RF3220K		SN54S74W	5
RF3222D, P		SN74S74J, N	5
RF3222K		SN74S74W	5
RG40D, P	SNG40J, N	SN5420J, N	6
RG40K	SNG40U	SN5420W	6
RG41D, P	SNG41J, N	SN5420J, N	6
RG41K	SNG41U	SN5420W	6
RG42D, P	SNG42J, N	SN7420J, N	6
RG42K	SNG42U	SN7420W	6
RG43D, P	SNG43J, N	SN7420J, N	6
RG43K	SNG43U	SN7420W	6
RG50D, P	SNG50J, N	SN5453J, N	6
RG50K	SNG50U	SN5453W	6

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Type Number	Direct Replacement	Recommended for New Designs	Sec.
RG51D, P	SNG51J, N	SN5453J, N	6
RG51K	SNG51U	SN5453W	6
RG52D, P	SNG52J, N	SN7453J, N	6
RG52K	SNG52U	SN7453W	6
RG53D, P	SNG53J, N	SN7453J, N	6
RG53K	SNG53U	SN7453W	6
RG60D, P	SNG60J, N	SN5430J, N	6
RG60K	SNG60U	SN5430W	6
RG61D, P	SNG61J, N	SN5430J, N	6
RG61K	SNG61U	SN5430W	6
RG62D, P	SNG62J, N	SN7430J, N	6
RG62K	SNG62U	SN7430W	6
RG63D, P	SNG63J, N	SN7430J, N	6
RG63K	SNG63U	SN7430W	6
RG70D, P	SNG70J, N	SN5450J, N	6
RG70K	SNG70U	SN5450W	6
RG71D, P	SNG71J, N	SN5450J, N	6
RG71K	SNG71U	SN5450W	6
RG72D, P	SNG72J, N	SN7450J, N	6
RG72K	SNG72U	SN7450W	6
RG73D, P	SNG73J, N	SN7450J, N	6
RG73K	SNG73U	SN7450W	6
RG80D, P	SNG80J, N	SN5413J, N	6
RG80K	SNG80U	SN5413W	6
RG81D, P	SNG81J, N	SN5413J, N	6
RG81K	SNG81U	SN5413W	6
RG82D, P	SNG82J, N	SN7413J, N	6
RG82K	SNG82U	SN7413W	6
RG83D, P	SNG83J, N	SN7413J, N	6
RG83K	SNG83U	SN7413W	6
RG90D, P	SNG90J, N	SN5486J, N	9
RG90K	SNG90U	SN5486W	9
RG91D, P	SNG91J, N	SN5486J, N	9
RG91K	SNG91U	SN5486W	9
RG92D, P	SNG92J, N	SN7486J, N	9
RG92K	SNG92	SN7486W	9
RG93D, P	SNG93J, N	SN7486J, N	9
RG93K	SNG93U	SN7486W	9
RG100D, P	SNG100J, N	SN5453J, N	6
RG100K	SNG100U	SN5453W	6
RG101D, P	SNG101J, N	SN5453J, N	6
RG101K	SNG101U	SN5453W	6
RG102D, P	SNG102J, N	SN5453J, N	6
RG102K	SNG102U	SN5453W	6
RG103D, P	SNG103J, N	SN7454J, N	6
RG103K	SNG103U	SN7453W	6
RG110D, P	SNG110J, N	SN54H55J, N	7
RG110K	SNG110U	SN54H55W	7
RG111D, P	SNG111J, N	SN54H55J, N	7
RG111K	SNG111U	SN54H55W	7
RG112D, P	SNG112J, N	SN74H55J, N	7
RG112K	SNG112U	SN74H55W	7
RG113D, P	SNG113J, N	SN74H55J, N	7
RG113K	SNG113U	SN74H55W	7
RG120D, P	SNG120J, N	SN5430J, N	6
RG120K	SNG120U	SN5430W	6
RG121D, P	SNG121J, N	SN5430J, N	6
RG121K	SNG121U	SN5430W	6
RG122D, P	SNG122J, N	SN7430J, N	6
RG122K	SNG122U	SN7430W	6
RG123D, P	SNG123J, N	SN7430J, N	6
RG123K	SNG123U	SN7430W	6
RG130D, P	SNG130J, N	SN54S140J, N	5
RG130K	SNG130U	SN54S140W	5
RG131D, P	SNG131J, N	SN54S140J, N	5
RG131K	SNG131U	SN54S140W	5
RG132D, P	SNG132J, N	SN74S140J, N	5
RG132K	SNG132U	SN74S140W	5
RG133D, P	SNG133J, N	SN74S140J, N	5
RG133K	SNG133U	SN74S140W	5
RG140D, P	SNG140J, N	SN5400J, N	6
RG140K	SNG140U	SN5400W	6
RG141D, P	SNG141J, N	SN5400J, N	6
RG141K	SNG141U	SN5400W	6
RG142D, P	SNG142J, N	SN7400J, N	6
RG142K	SNG142U	SN7400W	6
RG143D, P	SNG143J, N	SN7400J, N	6
RG143K	SNG143U	SN7400W	6
RG150D, P	SNG150J, N	SN54H62J, N	7
RG150K	SNG150U	SN54H62W	7
RG151D, P	SNG151J, N	SN54H62J, N	7
RG151K	SNG151U	SN54H62W	7
RG152D, P	SNG152J, N	SN74H62J, N	7
RG152K	SNG152U	SN74H62W	7
RG153D, P	SNG153J, N	SN74H62J, N	7
RG153K	SNG153U	SN74H62W	7
RG160D, P	SNG160J, N	SN5438J, N	6
RG160K	SNG160U	SN5438W	6
RG161D, P	SNG161J, N	SN5438J, N	6
RG161K	SNG161U	SN5438W	6
RG162D, P	SNG162J, N	SN7438J, N	6
RG162K	SNG162U	SN7438W	6
RG163D, P	SNG163J, N	SN7438J, N	6
RG163K	SNG153U	SN7438W	6
RG170D, P	SNG170J, N	SN5460J, N	6
RG170K	SNG170U	SN5460W	6
RG171D, P	SNG171J, N	SN5460J, N	6
RG171K	SNG171U	SN5460W	6
RG172D, P	SNG172J, N	SN7460J, N	6
RG172K	SNG172U	SN7460W	6
RG173D, P	SNG173J, N	SN7460J, N	6
RG173K	SNG173U	SN7460W	6
RG180D, P	SNG180J, N	SN5430J, N	6
RG180K	SNG180U	SN5430W	6
RG181D, P	SNG181J, N	SN5430J, N	6
RG181K	SNG181U	SN5430W	6
RG182D, P	SNG182J, N	SN7430J, N	6
RG182K	SNG182U	SN7430W	6
RG183D, P	SNG183J, N	SN7430J, N	6
RG183K	SNG183U	SN7430W	6
RG190D, P	SNG190J, N	SN5410J, N	6
RG190K	SNG191U	SN5410W	6
EG191D, P	SNG191J, N	SN5410J, N	6
RG191K	SNG191U	SN5410W	6
RG192D, P	SNG192J, N	SN7410J, N	6
RG192K	SNG192U	SN7410W	6
RG193D, P	SNG193J, N	SN7410J, N	6
RG193K	SNG193U	SN7410W	6
RG200D, P	SNG200J, N	SN54H30J, N	7
RG200K	SNG200U	SN54H30W	7
RG201D, P	SNG201J, N	SN54H30J, N	7
RG201K	SNG201U	SN54H30W	7
RG202D, P	SNG202J, N	SN74H30J, N	7
RG202K	SNG202U	SN74H30W	7
RG203D, P	SNG203J, N	SN74H30J, N	7
RG203K	SNG203U	SN74H30W	7
RG210D, P	SNG210J, N	SN54H55J, N	7
RG210K	SNG210U	SN54H55W	7
RG211D, P	SNG211J, N	SN54H55J, N	7
RG211K	SNG211U	SN54H55W	7
RG212D, P	SNG212J, N	SN74H55J, N	7
RG212K	SNG212U	SN74H55W	7
RG213D, P	SNG213J, N	SN74H55J, N	7
RG213K	SNG213U	SN74H55W	7
RG220D, P	SNG220J, N	SN54H00J, N	7
RG220K	SNG220U	SN54H00W	7

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Type Number	Direct Replacement	Recommended for New Designs	Sec.
RG221D, P	SNG221J, N	SN54H00J, N	7
RG221K	SNG221U	SN54H00W	7
RG222D, P	SNG222J, N	SN74H00J, N	7
RG222K	SNG222U	SN74H00W	7
RG223D, P	SNG223J, N	SN74H00J, N	7
RG223K	SNG223U	SN74H00W	7
RG230D, P	SNG230J, N	SN74H62J, N	7
RG230K	SNG230U	SN74H62W	7
RG231D, P	SNG231J, N	SN54H62J, N	7
RG231K	SNG231U	SN54H62W	7
RG232D, P	SNG232J, N	SN74H62J, N	7
RG232K	SNG232U	SN74H62W	7
RG233D, P	SNG233J, N	SN74H62J, N	7
RG233K	SNG233U	SN74H62W	7
RG240D, P	SNG240J, N	SN54H20J, N	7
RG240K	SNG240U	SN54H20W	7
RG241D, P	SNG241J, N	SN54H20J, N	7
RG241K	SNG241U	SN54H20W	7
RG242D, P	SNG242J, N	SN74H20J, N	7
RG242K	SNG242U	SN74H20W	7
RG243D, P	SNG243J, N	SN74H20J, N	7
RG243K	SNG243U	SN74H20W	7
RG250D, P	SNG250J, N	SN54H53J, N	7
RG250K	SNG250U	SN54H53W	7
RG251D, P	SNG251J, N	SN54H53J, N	7
RG251K	SNG251U	SN54H53W	7
RG252D, P	SNG252J, N	SN74H53J, N	7
RG252K	SNG252U	SN74H53W	7
RG253D, P	SNG253J, N	SN74H53J, N	7
RG253K	SNG253U	SN74H53W	7
RG260D, P	SNG260J, N	SN54H30J, N	7
RG260K	SNG260U	SN54H30W	7
RG261D, P	SNG261J, N	SN54H30J, N	7
RG261K	SNG261U	SN54H30W	7
RG262D, P	SNG262J, N	SN74H30J, N	7
RG262K	SNG262U	SN74H30W	7
RG263D, P	SNG263J, N	SN74H30J, N	7
RG263K	SNG263U	SN74H30W	7
RG270D, P	SNG270J, N	SN54H60J, N	7
RG270K	SNG270U	SN54H60W	7
RG271D, P	SNG271J, N	SN54H60J, N	7
RG271K	SNG271U	SN54H60W	7
RG272D, P	SNG272J, N	SN74H60J, N	7
RG272K	SNG272U	SN74H60W	7
RG273D, P	SNG273J, N	SN74H60J, N	7
RG273K	SNG273U	SN74H60W	7
RG280D, P	SNG280J, N	SN54H52J, N	7
RG280K	SNG280U	SN54H52J, N	7
RG281D, P	SNG281J, N	SN54H52J, N	7
RG281K	SNG281U	SN54H52W	7
RG282D, P	SNG282J, N	SN74H52J, N	7
RG282K	SNG282U	SN74H52W	7
RG283D, P	SNG283J, N	SN74H52J, N	7
RG283K	SNG283U	SN74H52W	7
RG290D, P	SNG290J, N	SN54H62J, N	7
RG290K	SNG290U	SN54H62W	7
RG291D, P	SNG291J, N	SN54H62J, N	7
RG291K	SNG291U	SN54H62W	7
RG292D, P	SNG292J, N	SN74H62J, N	7
RG292K	SNG292U	SN74H62W	7
RG293D, P	SNG293J, N	SN74H62J, N	7
RG293K	SNG293U	SN74H62W	7
RG300D, P	SNG300J, N	SN54H53J, N	7
RG300K	SNG300U	SN54H53W	7
RG301D, P	SNG301J, N	SN54H53J, N	7
RG301K	SNG301U	SN54H53W	7
RG302D, P	SNG302J, N	SN74H53J, N	7
RG302K	SNG302U	SN74H53W	7
RG303D, P	SNG303J, N	SN74H53J, N	7
RG303K	SNG303U	SN74H53W	7
RG310D, P	SNG310J, N	SN54H50J, N	7
RG310K	SNG310U	SN54H50W	7
RG311D, P	SNG311J, N	SN54H50J, N	7
RG311K	SNG311U	SN54H50W	7
RG312D, P	SNG312J, N	SN74H50J, N	7
RG312K	SNG312U	SN74H50W	7
RG313D, P	SNG313J, N	SN74H50J, N	7
RG313K	SNG313U	SN74H50W	7
RG320D, P	SNG320J, N	SN54H10J, N	7
RG320K	SNG320U	SN54H10W	7
RG321D, P	SNG321J, N	SN54H10J, N	7
RG321K	SNG321U	SN54H10W	7
RG322D, P	SNG322J, N	SN74H10J, N	7
RG322K	SNG322U	SN74H10W	7
RG323D, P	SNG323J, N	SN74H10J, N	7
RG323K	SNG323U	SN74H10W	7
RG370D, P	SNG370J, N	SN5404J, N	6
RG370K	SNG370U	SN5404W	6
RG371D, P	SNG371J, N	SN5404J, N	6
RG371K	SNG371U	SN5404W	6
RG372D, P	SNG372J, N	SN7404J, N	6
RG372K	SNG372U	SN7404W	6
RG373D, P	SNG373J, N	SN7404J, N	6
RG373K	SNG373U	SN7404W	6
RG380D, P	SNG380J, N	SN54H04J, N	7
RG380K	SNG380U	SN54H04W	7
RG381D, P	SNG381J, N	SN54H04J, N	7
RG381K	SNG381U	SN54H04W	7
RG382D, P	SNG382J, N	SN74H04J, N	7
RG382K	SNG382U	SN74H04W	7
RG383D, P	SNG383J, N	SN74H04J, N	7
RG383K	SNG383U	SN74H04W	7
RG3180D, P		SN54S15J, N	5
RG3180K		SN54S15W	5
RG3182D, P		SN74S15J, N	5
RG3182K		SN74S15W	5
RG3200D, P		SN54H30J, N	7
RG3200K		SN54H30W	7
RG3202D, P		SN74H30J, N	7
RG3202K		SN74H30W	7
RG3210D, P		SN54S65J, N	5
RG3210K		SN54S65W	5
RG3212D, P		SN74S65J, N	5
RG3212K		SN74S65W	5
RG3220D, P		SN54S00J, N	5
RG3220K		SN54SooW	5
RG3222D, P		SN74S00J, N	5
RG3222K		SN74S00W	5
RG3230D, P		SN54S65J, N	5
RG3230K		SN54S65W	5
RG3232D, P		SN74S65J, N	5
RG3232K		SN74S65W	5
RG3240D, P		SN54S20J, N	5
RG3240K		SN54S20W	5
RG3242D, P		SN74S20J, N	5
RG3242K		SN74S20W	5
RG3250D, P		SN54S65J, N	5
RG3250K		SN54S65W	5
RG3252D, P		SN74S65J, N	5
RG3252K		SN74S65W	5
RG3260D, P		SN54H30J, N	7
RG3260K		SN54H30W	7
RG3262D, P		SN74H30J, N	7
RG3262K		SN74H30W	7

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Type Number	Direct Replacement	Recommended for New Designs	Sec.
RG3270D, P		SN54S65J, N	5
RG3270K		SN54S65W	5
RG3272D, P		SN74S65J, N	5
RG3272K		SN74S65W	5
RG3310D, P		SN54S65J, N	5
RG3310K		SN54S65W	5
RG3312D, P		SN74S65J, N	5
RG3312K		SN74S65W	5
RG3320D, P		SN54S10J, N	5
RG3320K		SN54S10W	5
RG3322D, P		SN74S10J, N	5
RG3322K		SN74S10W	5
RG3380D, P		SN54S04J, N	5
RG3380K		SN54S04W	5
RG3382D, P		SN74S04J, N	5
RG3382K		SN74S04W	5
RG3390D, P		SN54S15J, N	5
RG3390K		SN54S15W	5
RG3392D, P		SN74S15J, N	5
RG3392K		SN74S15W	5
RG3400D, P		SN54S15J, N	5
RG3400K		SN54S15W	5
RG3402D, P		SN74S15J, N	5
RG3402K		SN74S15W	5
RG3420D, P		SN54S22J, N	5
RG3420K		SN54S22W	5
RG3422D, P		SN74S22J, N	5
RG3422K		SN74S22W	5
RG3440D, P		SN54S65J, N	5
RG3440K		SN54S65W	5
RG3442D, P		SN74S65J, N	5
RG3442K		SN74S65W	5
RL10D, P		SN54H183J, N	9
RL10K		SN54H183W	9
RL11D, P		SN54H183J, N	9
RL11K		SN54H183W	9
RL12D, P		SN74H183J, N	9
RL12K		SN74H183W	9
RL13D, P		SN74H183J, N	9
RL13K		SN74H183W	9
RL20D, P	SNG20J, N	SN54181J, N	9
RL20K	SNG20U	SN54181W	9
RL21D, P	SNG21J, N	SN54181J, N	9
RL21K	SNG21U	SN54181W	9
RL22D, P	SNG22J, N	SN74181J, N	9
RL22K	SNG22U	SN74181W	9
RL23D, P	SNG23J, N	SN74181J, N	9
RL23K	SNG23U	SN74181W	9
RL30D, P	SNG30J, N	SN54181J, N	9
RL30K	SNG30U	SN54181W	9
RL31D, P	SNG31J, N	SN54181J, N	9
RL31K	SNG31U	SN54181W	9
RL32D, P	SNG32J, N	SN74181J, N	9
RL32K	SNG32U	SN74181W	9
RL33D, P	SNG33J, N	SN74181J, N	9
RL33K	SNG33U	SN74181W	9
RL40D, P	SNG40J, N	SN54182J, N	9
RL40K	SNG40U	SN54182W	9
RL41D, P	SNG41J, N	SN54182J, N	9
RL41K	SNG41U	SN54182W	9
RL42D, P	SNG42J, N	SN74182J, N	9
RL42K	SNG42U	SN74182W	9
RL43D, P	SNG43J, N	SN74182J, N	9
RL43K	SNG43U	SN74182W	9
RL60D, P	SNG60J, N	SN5475J, N	9
RL60K	SNG60U	SN5475W	9
RL61D, P	SNG61J, N	SN5475J, N	9
RL61K	SNG61U	SN5475W	9
RL62D, P	SNG62J, N	SN7475J, N	9
RL62K	SNG62U	SN7475W	9
RL63D, P	SNG63J, N	SN7475J, N	9
RL63K	SNG63U	SN7475W	9
RL70D, P	SNG70J, N	SN5475J, N	9
RL70K	SNG70U	SN5475W	9
RL71D, P	SNG71J, N	SN5475J, N	9
RL71K	SNG71U	SN5475W	9
RL72D, P	SNG72J, N	SN7475J, N	9
RL72K	SNG72U	SN7475W	9
RL73D, P	SNG73J, N	SN7475J, N	9
RL73K	SNG73U	SN7475W	9
RL80D, P	SNG80J, N	SN5489J, N	9
RL80K	SNG80U	SN5489W	9
RL81D, P	SNG81J, N	SN5489J, N	9
RL81K	SNG81U	SN5489W	9
RL82D, P	SNG82J, N	SN7489J, N	9
RL82K	SNG82U	SN7489W	9
RL83D, P	SNG83J, N	SN7489J, N	9
RL83K	SNG83U	SN7489W	9

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Type Number	Direct Replacement	Recommended for New Designs	Sec.
N8H16A	SN74H20J, N	SN74H20J, N	7
N8H16J		SN74H20W	7
N8H20Q		SN74H103W	7
N8H21A		SN74H108J, N	7
N8H21Q		SN74H108W	7
N8H22B		SN74H106J, N	7
N8H70A	SN74H11J, N	SN74H11J, N	7
N8H70J		SN74H11W	7
N8H80A	SN74H00J, N	SN74H00J, N	7
N8H80J		SN74H00W	7
N8H90A	SN74H04J, N	SN74H04J, N	7
N8H90J	SN74H04W	SN74H04W	7
N8T01B		SN74141J, N	9
N8T04B		SN7447AJ, N	9
N8T04R		SN7447AJ, N	9
N8T05B		SN7448J, N	9
N8T05R		SN7448W	9
N8T13B		SN74S140J, N	5
N8T13R		SN74S140W	5
N8T14B		SN7413J, N	6
N8T14R		SN7413W	6
N8T80A		SN7426J, N	6
N8T80J		SN7426W	6
N8T90A		SN7406J, N	6
N8T90J		SN7406W	6
N1283A		SN7484J, N	9
N8162A		SN74121J, N	6
N8162J		SN74121W	6

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DTL/TTL CIRCUITS

Signetics DCL, Cont.

Type Number	Direct Replacement	Recommended for New Designs	Sec.
N8200P		SN74198W	9
N8200Y		SN74198J, N	9
N8201P		SN74198W	9
N8201Y		SN74198J, N	9
N8202P		SN74198W	9
N8202Y		SN74198J, N	9
N8203P		SN74198W	9
N8203Y		SN74198J, N	9
N8224B	SN7488AJ, N	SN7488AJ, N	9
N8224R	SN7488W	SN7488W	9
N8230B		SN74151J, N	9
N8231B		SN74151J, N	9
N8232B		SN74151J, N	9
N8233B		SN74153J, N	9
N8234B		SN74153J, N	9
N8235B		SN74153J, N	9
N8241A		SN7486J, N	9
N8241Q		SN7486W	9
N8242A		SN7485J, N	9
N8242Q		SN7485W	9
N8243P		SN74198W	9
N8243Y		SN74198J, N	9
N8250A		SN7442J, N	9
N8250J		SN7442W	9
N8251B		SN7442J, N	9
N8260P		SN74181W	9
N8261A		SN74182J, N	9
N8261Q		SN74182W	9
N8262A		SN74180J, N	9
N8262Q		SN74180W	9
N8263P		SN74153W	9
N8263Y		SN74153J, N	9
N8264P		SN74153W	9
N8264Y		SN74153J, N	9
N8266B		SN74153J, N	9
N8266R		SN74153J, N	9
N8267B		SN74153J, N	9
N8267R		SN74153W	9
N8268A	SN7480J, N	SN74181J, N	9
N8268Q	SN7480W	SN74181W	9
N8270A		SN74194J, N	9
N8270J		SN74194W	9
N8271B		SN74194J, N	9
N8275B		SN7475J, N	9
N8275R		SN7475W	9
N8276A		SN7491AJ, N	9
N8276Q		SN7491A, W	9
N8280A		SN74196J, N	9
N8280J		SN74196W	9
N8281A		SN74197J, N	9
N8281J		SN74197W	9
N8284A		SN74191J, N	9
N8284Q		SN74191W	9
N8285A		SN74190J, N	9
N8285Q		SN74190W	9
N8288A		SN74163J, N	9
N8288Q		SN74163W	9
N8290A	SN74196J, N	SN74196J, N	9
N8290Q	SN74196W	SN74196W	9
N8291A	SN74197J, N	SN74197J, N	9
N8291Q	SN74197W	SN74197W	9
N8292A		SN74L90J, N	9
N8292Q		SN74L90R	9
N8293A		SN74197J, N	9
N8293Q		SN74197R	9
N8415A	SN151800J, N	SN7420J, N	6
N8415J		SN7420W	6
N8416A	SN15830J, N	SN7420J, N	6
N8416J		SN7420J, N	6
N8417A		SN7410J, N	6
N8417J		SN7410W	6
N8424A		SN74111J, N	6
N8424J		SN74111W	6
N8425A		SN74111J, N	6
N8425J		SN74111W	6
N8440A		SN7450J, N	6
N8440J		SN7450W	6
N8455A	SN7440J, N	SN7440J, N	6
N8455J		SN7440W	6
N8470A, F	SN7410J, N	SN7410J, N	6
N8470J		SN7410J, N	6
N8471A	SN7412J, N	SN7412J, N	6
N8471J		SN7412W	6
N8480A	SN7400J, N	SN7400J, N	6
N8480J		SN7400J, N	6
N8481A	SN7403J, N	SN7403J, N	6
N8481J		SN7403W	6
N8490A	SN7404J, N	SN7404J, N	6
N8490J	SN7404W	SN7404W	6
N8706A		SN7460J, N	6
N8706J		SN7460W	6
N8731A		SN7460J, N	6
N8731J		SN7460W	6
N8806J	SN7460W	SN7460W	6
N8808A	SN7430J, N	SN7430J, N	6
N8808J	SN7430W	SN7430W	6
N8815A	SN7425J, N	SN7425J, N	6
N8815J		SN7425W	6
N8816A		SN7420J, N	6
N8816J	SN7420W	SN7420W	6
N8821J		SN7476W	6
N8822A		SN7473J, N	6
N8822J	SN7473W	SN7473W	6
N8824B		SN7476J, N	6
N8825A	SN7470J, N	SN7470J, N	6
N8825J	SN7470W	SN7470W	6
N8826A		SN74107J, N	6
N8826J		SN7473W	6
N8827A		SN7476J, N	6
N8827J		SN7476W	6
N8824A	SN7474J, N	SN7474J, N	6
N8824J	SN7474W	SN7474W	6
N8829A	SN74110J, N	SN74110J, N	6
N8829J		SN74110W	6
N8840A	SN7450J, N	SN7450J, N	6
N8840J	SN7450W	SN7450W	6
N8848A	SN74H54J, N	SN74H54J, N	7
N8848J	SN74H54W	SN74H54W	7
N8855A		SN7440J, N	6
N8855J	SN7440W	SN7440W	6
N8870A		SN7410J, N	6
N8870J		SN7410W	6
N8875A	SN7427J, N	SN7427J, N	6
N8875J		SN7427W	6
N8880A		SN7400J, N	6
N8880J	SN7400W	SN7400W	6
N8881A	SN7401J, N	SN7401J, N	6
N8881J	SN7401W	SN7401W	6
N8885A		SN7402J, N	6
N8885J		SN7402W	6
N8890A	SN7404J, N	SN7404J, N	6
N8890Q	SN7404W	SN7404W	6
N8891A	SN7405J, N	SN7405J, N	6

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B

Type Number	Direct Replacement	Recommended for New Designs	Sec.
N8891Q	SN7405W	SN7405W	6
S8H16A, F	SN54H20J, N	SN54H20J, N	7
S8H16J		SN54H20W	7
58H20Q		SN54H103W	7
S8H21A, F		SN54H108J, N	7
S8H21Q		SN54H108W	7
S8H22B, E		SN54H106J, N	7
S8H70A, F	SN54H11J, N	SN54H11J, N	7
S8H70J		SN54H11W	7
S8H80A, F	SN54H00J, N	SN54H00J, N	7
S8H80J		SN54H00W	7
S8H90A, F	SN54H04J, N	SN54H04J, N	7
S8H90J	SN54H04W	SN54H04W	7
S8T01B		SN74141J, N	9
S8T04B, E		SN5447AJ, N	9
S8T04R		SN5447AJ, N	9
S8T05B, E		SN5448J, N	9
S8T05R		SN5448W	9
S8T13B, E		SN54S140J, N	5
S8T13R		SN54S140W	5
S8T14B		SN5413J, N	6
S8T14R		SN5413W	6
S8T80A, F		SN5426J, N	6
S8T80J		SN5426W	6
S8T90A, F		SN5406J, N	6
S8T90J		SN5406W	6
S8162A, F		SN54121J, N	6
S8162J		SN54121W	6
S8200P		SN54198W	9
S8200Y		SN54198J, N	9
S8201P		SN54198W	9
S8201Y		SN54198J, N	9
S8202P		SN54198W	9
S8202Y		SN54198J, N	9
S8203P		SN54198W	9
S8203Y		SN54198J, N	9
S8224B	SN5488AJ, N	SN7488AJ, N	9
S8224R	SN5488W	SN5488W	9
S8230B, E		SN54151J, N	9
S8231B, E		SN54151J, N	9
S8232B, E		SN54151J, N	9
S8233B, E		SN54153J, N	9
S8234B, E		SN54153J, N	9
S8235B, E		SN54153J, N	9
S8241A, F		SN5486J, N	9
S8241Q		SN5486W	9
S8242A, F		SN5485J, N	9
S8242Q		SN5485W	9
S8243P		SN54198W	9
S8243Y		SN54198J, N	9
S8250A		SN5442J, N	9
S8250J		SN5442W	9
S8251B		SN5442J, N	9
S8260P		SN54181W	9
S8261A, F		SN54182J, N	9
S8261Q		SN54182W	9
S8262A, F		SN54180J, N	9
S8262Q		SN54180W	9
S8263P		SN54153W	9
S8263Y		SN54153J, N	9
S8264P		SN54153W	9
S8264Y		SN54153J, N	9
S8266B, E		SN54153J, N	9
S8267R		SN54153W	9
S8268A, F	SN5480J, N	SN54181J, N	9
S8268Q	SN5480W	SN54181W	9
S8270A		SN54194J, N	9
S8270J		SN54194W	9
S8271B		SN54194J, N	9
S8275B, E		SN5475J, N	9
S8275R		SN5475W	9
S8276A, F		SN5491J, N	9
S8276Q		SN5491A, W	9
S8280A		SN54196J, N	9
S8280J		SN54196W	9
S8281A		SN54197J, N	9
S8281J		SN54197W	9
S8284A		SN54191J, N	9
S8284Q		SN54191W	9
S8285A		SN54190J, N	9
S8285Q		SN54190W	9
S8288A		SN54163J, N	9
S8288Q		SN54163W	9
S8290A	SN54196J, N	SN54196J, N	9
S8290Q	SN54196W	SN54196W	9
S8291A	SN54197J, N	SN54197J, N	9
S8291Q	SN54197W	SN54197W	9
S8292A		SN54L90J, N	9
S8292Q		SN54L90R	9
S8293A		SN54197J, N	9
S8293Q		SN54197R	9
S8415A	SN151900J, N	SN5420J, N	6
S8415J		SN5420W	6
S8416A	SN15930J, N	SN5420J, N	6
S8416J		SN5420J, N	6
S8417A		SN5410J, N	6
S8417J		SN5410W	6
S8424A		SN54111J, N	6
S8424J		SN54111W	6
S8425A		SN54111J, N	6
S8425J		SN54111W	6
S8440A, F		SN5450J, N	6
S8440J		SN5450W	6
S8455A, F	SN5440J, N	SN5440J, N	6
S8455J		SN5440W	6
S8470A, F	SN5410J, N	SN5410J, N	6
S8470J		SN5410J, N	6
S8471A, F	SN5412J, N	SN5412J, N	6
S8471J		SN5412W	6
S8480A, F	SN5400J, N	SN5400J, N	6
S8480J		SN5400J, N	6
S8481A, F	SN5403J, N	SN5403J, N	6
S8481J		SN5403W	6
S8490A, F	SN5404J, N	SN5404J, N	6
S8490J	SN5404W	SN5404W	6
S8706A, F		SN5460J, N	6
S8706J		SN5460W	6
S8731A, F		SN5460J, N	6
S8731J		SN5460W	6
S8806A, F	SN5460J, N	SN5460J, N	6
S8806J	SN5460W	SN5460W	6
S8808A, F	SN5430J, N	SN5430J, N	6
S8808J	SN5430W	SN5430W	6
S8815A, F	SN5425J, N	SN5425J, N	6
S8815J		SN5425W	6
S8816A, F		SN5420J, N	6
S8816J	SN5420W	SN5420W	6
S8821J		SN5476W	6
S8822A, F		SN5473J, N	6
S8822J	SN5473W	SN5473W	6
S8824B		SN5476J, N	6
S8825A, F	SN5470J, N	SN5470J, N	6
S8825J	SN5470W	SN5470W	6
S8826A, F		SN54107J, N	6

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Type Number	Direct Replacement	Recommended for New Designs	Sec.
S8826J		SN5473W	6
S8827A, F		SN5476J, N	6
S8827J		SN5476W	6
S8824A, F	SN5474J, N	SN5474J, N	6
S8824J	SN5474W	SN5474W	6
S8829A, F	SN54110J, N	SN54110J, N	6
S8829J		SN54110W	6
S8840A, F	SN5450J, N	SN5450J, N	6
S8840J	SN5450W	SN5450W	6
S8848A, F	SN54H54J, N	SN54H54J, N	7
S8848J	SN54H54W	SN54H54W	7
S8855A, F		SN5440J, N	6
S8855J	SN5440W	SN5440W	6
S8870A, F		SN5410J, N	6
S8870J		SN5410W	6
S8875A, F	SN5427J, N	SN5427J, N	6
S8875J		SN5427W	6
S8880A, F		SN5400J, N	6
S8880J	SN5400W	SN5400W	6
S8881A, F	SN5401J, N	SN5401J, N	6
S8881J	SN5401W	SN5401W	6
S8885A, F		SN5402J, N	6
S8885J		SN5402W	6
S8890A, F	SN5404J, N	SN5404J, N	6
S8890Q	SN5404W	SN5404W	6
S8891A, F	SN5405J, N	SN5405J, N	6
S8891Q	SN5405W	SN5405W	6

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Type Number	Direct Replacement	Recommended for New Designs	Sec.
N7400A	SN7400J, N	SN7400J, N	6
N7400J	SN7400W	SN7400W	6
N7401A	SN7401J, N	SN7401J, N	6
N7401J	SN7401W	SN7401W	6
N7402A	SN7402J, N	SN7402J, N	6
N7402Q	SN7402W	SN7402W	6
N7403A	SN7403J, N	SN7403J, N	6
N7404A	SN7404J, N	SN7404J, N	6
N7404Q	SN7404W	SN7404W	6
N7405A	SN7405J, N	SN7405J, N	6
N7405Q	SN7405W	SN7405W	6
N7408A	SN7408J, N	SN7408J, N	6
N7408Q	SN7408W	SN7408W	6
N7410A	SN7410J, N	SN7410J, N	6
N7410J	SN7410W	SN7410W	6
N7420A	SN7420J, N	SN7420J, N	6
N7420J	SN7420W	SN7420W	6
N7430A	SN7430J, N	SN7430J, N	6
N7430J	SN7430W	SN7430W	6
N7440A	SN7440J, N	SN7440J, N	6
N7440Q	SN7440W	SN7440W	6
N7441B	SN7441J, N	SN7441J, N	9
N7450A	SN7450J, N	SN7450J, N	6
N7450J	SN7450W	SN7450W	6
N7451A	SN7451J, N	SN7451J, N	6
N7451J	SN7451W	SN7451W	6
N7453A	SN7453J, N	SN7453J, N	6
N7453J	SN7453W	SN7453W	6
N7454A	SN7454J, N	SN7454J, N	6
N7454J	SN7454W	SN7454W	6
N7460A	SN7460J, N	SN7460J, N	6
N7460J	SN7460W	SN7460W	6
N7470A	SN7470J, N	SN7470J, N	6
N7470J	SN7470W	SN7470W	6
N7472A	SN7472J, N	SN7472J, N	6
N7472J	SN7472W	SN7472W	6
N7473A	SN7473J, N	SN7473J, N	6
N7473J	SN7473W	SN7473W	6
N7474A	SN7474J, N	SN7474J, N	6
N7474J	SN7474W	SN7474W	6
N7475B	SN7575J, N	SN7475J, N	9
N7476B	SN7476J, N	SN7476J, N	6
N4777Q	SN7477W	SN7477W	9
N7480A	SN7480J, N	SN7480J, N	9
N7480Q	SN7480W	SN7480W	9
N7490A	SN7490J, N	SN7490J, N	9
N7490Q	SN7490W	SN7490W	9
N7491A	SN7491J, N	SN7491J, N	9
N7491Q	SN7491W	SN7491W	9
N7492A	SN7492J, N	SN7492J, N	9
N7492Q	SN7492W	SN7492W	9
N7493A	SN7493J, N	SN7493J, N	9
N7493Q	SN7493W	SN7493W	9
N74107A	SN74107J, N	SN74107J, N	6
N74H00A	SN74H00J, N	SN74H00J, N	7
N74H00Q	SN74H00W	SN74H00W	7
N74H01A	SN74H01J, N	SN74H01J, N	7
N74H01Q	SN74H01W	SN74H01W	7
N74H04A	SN74H04J, N	SN74H04J, N	7
N74H04Q	SN74H04W	SN74H04W	7
N74H05A	SN74H05J, N	SN74H05J, N	7
N74H05Q	SN74H05W	SN74H05W	7
N74H10A	SN74H10J, N	SN74H10J, N	7
N74H10Q	SN74H10W	SN74H10W	7
N74H11A	SN74H11J, N	SN74H11J, N	7
N74H11Q	SN74H11W	SN74H11W	7
N74H20A	SN74H20J, N	SN74H20J, N	7
N74H20Q	SN74H20W	SN74H20W	7
N74H21A	SN74H21J, N	SN74H21J, N	7
N74H21Q	SN74H21W	SN74H21W	7
N74H22A	SN74H22J, N	SN74H22J, N	7
N74H22Q	SN74H22W	SN74H22W	7
N74H30A	SN74H30J, N	SN74H30J, N	7
N74H30J	SN74H30W	SN74H30W	7
N74H40A	SN74H40J, N	SN74H40J, N	7
N74H40Q	SN74H40W	SN74H40W	7
N74H50A	SN74H50J, N	SN74H50J, N	7
N74H50Q	SN74H50W	SN74H50W	7
N74H51A	SN74H51J, N	SN74H51J, N	7
N74H51Q	SN74H51W	SN74H51W	7
N74H52A	SN74H52J, N	SN74H52J, N	7
N74H52Q	SN74H52W	SN74H52W	7
N74H53A	SN74H53J, N	SN74H53J, N	7
N74H53J	SN74H53W	SN74H53W	7
N74H54A	SN74H54J, N	SN74H54J, N	7
N74H54J	SN74H54W	SN74H54W	7
N74H55A	SN74H55J, N	SN74H55J, N	7
N74H55J	SN74H55W	SN74H55W	7

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B

Type Number	Direct Replacement	Recommended for New Designs	Sec.
N74H60A	SN74H60J, N	SN74H60J, N	7
N74H60J	SN74H60W	SN74H60W	7
N74H61A	SN74H61J, N	SN74H61J, N	7
N74H61J	SN74H61W	SN74H61W	7
N74H62A	SN74H62J, N	SN74H62J, N	7
N74H62J	SN74H62W	SN74H62W	7
N74H72A	SN74H72J, N	SN74H72J, N	7
N74H72Q	SN74H72W	SN74H72W	7
N74H73A	SN74H73J, N	SN74H73J, N	7
N74H73Q	SN74H73W	SN74H73W	7
N74H74A	SN74H74J, N	SN74H74J, N	7
N74H74Q	SN74H74W	SN74H74W	7
N74H76B	SN74H76J, N	SN74H76J, N	7
S5400A	SN5400J, N	SN5400J, N	6
S5400J	SN5400W	SN5400W	6
S5401A	SN5401J, N	SN5401J, N	6
S5401J	SN5401W	SN5401W	6
S5402A	SN5402J, N	SN5402J, N	6
S5402Q	SN5402W	SN5402W	6
S5403A	SN5403J, N	SN5403J, N	6
S5404A	SN5404J, N	SN5404J, N	6
S5404Q	SN5404W	SN5404W	6
S5405A	SN5405J, N	SN5405J, N	6
S5405Q	SN5405W	SN5405W	6
S5408A	SN5408J, N	SN5408J, N	6
S5408Q	SN5408W	SN5408W	6
S5410A	SN5410J, N	SN5410J, N	6
S5410J	SN5410W	SN5410W	6
S5420A	SN5420J, N	SN5420J, N	6
S5420J	SN5420W	SN5420W	6
S5430A	SN5430J, N	SN5430J, N	6
S5430J	SN5430W	SN5430W	6
S5440A	SN5440J, N	SN5440J, N	6
S5440J	SN5440W	SN5440W	6
S5450A	SN5450J, N	SN5450J, N	6
S5450J	SN5450W	SN5450W	6
S5451A	SN5451J, N	SN5451J, N	6
S5451J	SN5451W	SN5451W	6
S5453A	SN5453J, N	SN5453J, N	6
S5453J	SN5453W	SN5453W	6
S5454A	SN5453J, N	SN5454J, N	6
S5354J	SN5454W	SN5454W	6
S5460A	SN5460J, N	SN5460J, N	6
S5460J	SN5460W	SN5460W	6
S5470A	SN5470J, N	SN5470J, N	6
S5470J	SN5470W	SN5470W	6
S5472A	SN5472J, N	SN5472J, N	6
S5472J	SN5472W	SN5472W	6
S5473A	SN5473J, N	SN5473J, N	6
S5473J	SN5473W	SN5473W	6
S5474A	SN5474J, N	SN5474J, N	6
S5474J	SN5474W	SN5474W	6
S5475B	SN5475J, N	SN5475J, N	9
S5476B	SN5476J, N	SN5476J, N	6
S5477Q	SN5477W	SN5477W	9
S5480A	SN5480J, N	SN5480J, N	9
S5480Q	SN5480W	SN5480W	9
S5490A	SN5490J, N	SN5490J, N	9
S5490Q	SN5490W	SN5490W	9
S5491A	SN5491J, N	SN5491J, N	9
S5491Q	SN5491W	SN5491W	9
S5492A	SN5492J, N	SN5492J, N	9
S5492Q	SN5492W	SN5492W	9
S5493A	SN5493J, N	SN5493J, N	9
S5493Q	SN5493W	SN5493W	9
S54107A	SN54107J, N	SN54107J, N	7
S54H00A	SN54H00J, N	SN54H00J, N	7
S54H00Q	SN54H00W	SN54H00W	7
S54H01A	SN54H01J, N	SN54H01J, N	7
S54H01Q	SN54H01W	SN54H01W	7
S54H04A	SN54H04J, N	SN54H04J, N	7
S54H04Q	SN54H04W	SN54H04W	7
S54H05A	SN54H05J, N	SN54H05J, N	7
S54H05Q	SN54H05W	SN54H05W	7
S54H10A	SN54H10J, N	SN54H10J, N	7
S54H10Q	SN54H10W	SN54H10W	7
S54H11A	SN54H11J, N	SN54H11J, N	7
S54H11Q	SN54H11W	SN54H11W	7
S54H20A	SN54H20J, N	SN54H20J, N	7
S54H20Q	SN54H20W	SN54H20W	7
S54H21A	SN54H21J, N	SN54H21J, N	7
S54H21Q	SN54H21W	SN54H21W	7
S54H22A	SN54H22J, N	SN54H22J, N	7
S54H22Q	SN54H22W	SN54H22W	7
S54H30A	SN54H30J, N	SN54H30J, N	7
S54H30Q	SN54H30W	SN54H30W	7
S54H50A	SN54H50J, N	SN54H50J, N	7
S54H50Q	SN54H50W	SN54H50W	7
S54H51A	SN54H51J, N	SN54H51J, N	7
S54H51Q	SN54H51W	SN54H51W	7
S54H52A	SN54H52J, N	SN54H52J, N	7
S54H52Q	SN54H52W	SN54H52W	7
S54H53A	SN54H53J, N	SN54H53J, N	7
S54H53J	SN54H53W	SN54H53W	7
S54H54A	SN54H54J, N	SN54H54J, N	7
S54H54J	SN54H54W	SN54H54W	7
S54H55A	SN54H55J, N	SN54H55J, N	7
S54H55J	SN54H55W	SN54H55W	7
S54H60A	SN54H60J, N	SN54H60J, N	7
S54H60J	SN54H60W	SN54H60W	7
S54H61A	SN54H61J, N	SN54H61J, N	7
S54H61J	SN54H61W	SN54H61W	7
S54H62A	SN54H62J, N	SN54H62J, N	7
S54H62J	SN54H62W	SN54H62W	7
S54H72A	SN54H72J, N	SN54H72J, N	7
S54H72Q	SN54H72W	SN54H72W	7
S54H73A	SN54H73J, N	SN54H73J, N	7
S54H73Q	SN54H73W	SN54H73W	7
S54H74A	SN54H74J, N	SN54H74J, N	7
S54H74Q	SN54H74W	SN54H74W	7
S54H76B	SN54H76J, N	SN54H76J, N	7

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Type Number	Direct Replacement	Recommended for New Designs	Sec.
US5400A	SN5400J, N	SN5400J, N	6
US5400J	SN5400W	SN5400W	6
US5401A	US5401J, N	SN5401J, N	6
US5401J	US5401W	SN5401W	6
US5402A	SN5402J, N	SN5402J, N	6
US5402J	SN5402W	SN5402W	6
US5403A	SN5403J, N	SN5403J, N	6
US5404A	SN5404J, N	SN5404J, N	6
US5404J	SN5404W	SN5404W	6
US5405A	SN5405J, N	SN5405J, N	6
US5405J	SN5405W	SN5405W	6
US5408A	SN5408J, N	SN5408J, N	6
US5408J		SN5408W	6
US5409A	SN5409J, N	SN5409J, N	6
US5409J		SN5409W	6
US5410A	SN5410J, N	SN5410J, N	6
US5410J	SN5410W	SN5410W	6
US5420A	SN5420J, N	SN5420J, N	6
US5420J	SN5420W	SN5420W	6
US5426A	SN5426J, N	SN5426J, N	6
US5427A	SN5427J, N	SN5427J, N	6
US5427J		SN5427W	6
US5429A	SN5425J, N	SN5425J, N	6
US5429J		SN5425W	6
US5430A	SN5430J, N	SN5430J, N	6
US5430J	SN5430W	SN5430W	6
US5432A	SN5432J, N	SN5432J, N	6
US5432J		SN5432W	6
US5438A	SN5438J, N	SN5438J, N	6
US5438J		SN5438W	6
US5439A		SN5438J, N	6
US5439J		SN5438W	6
US5440A	SN5440J, N	SN5440J, N	6
US5440J	SN5440W	SN5440W	6
US5442A	SN5442J, N	SN5442J, N	9
US5442J	SN5442W	SN5442W	9
US5443A	SN5443J, N	SN5443J, N	9
US5443J	SN5443W	SN5443W	9
US5444A	SN5444J, N	SN5444J, N	9
US5444J	SN5444W	SN5444W	9
US5445A	SN5445J, N	SN5445J, N	9
US5445J	SN5445W	SN5445W	9
US5446A	SN5446AJ, N	SN5446AJ, N	9
US5446J	SN5446AW	SN5446AW	9
US5447A	SN5447AJ, N	SN5447AJ, N	9
US5447J	SN5447AW	SN5447AW	9
US5448A	SN5448J, N	SN5448J, N	9
US5448J	SN5448W	SN5448W	9
US5450A	SN5450J, N	SN5450J, N	6
US5450J	SN5450W	SN5450W	6
US5451A	SN5451J, N	SN5451J, N	6
US5451J	SN5451W	SN5451W	6
US5453A	SN5453J, N	SN5453J, N	6
US5453J	SN5453W	SN5453W	6
US5454A	SN5454J, N	SN5454J, N	6
US5454J	SN5454W	SN5454W	6
US5459A		SN5451J, N	6
US5459J		SN5451W	6
US5460A	SN5460J, N	SN5460J, N	6
US5460J	SN5460W	SN5460W	6
US5470A	SN5470J, N	SN5470J, N	6
US5470J	SN5470W	SN5470W	6
US5472A	SN5472J, N	SN5472J, N	6
US5472J	SN5472W	SN5472W	6
US5473A	SN5473J, N	SN5473J, N	6
US5473J	SN5473W	SN5473W	6
US5474A	SN5474J, N	SN5474J, N	6
US5474J	SN5474W	SN5474W	6

Type Number	Direct Replacement	Recommended for New Designs	Sec.
US5475A	SN5475J, N	SN5475J, N	9
US5476A	SN5476J, N	SN5476J, N	6
US5477J	SN5477W	SN5477W	9
US5480A	SN5480J, N	SN5480J, N	9
US5480J	SN5480W	SN5480W	9
US5481A	SN5481J, N	SN5481J, N	9
US5481J	SN5481W	SN5481W	9
US5482A	SN5482J, N	SN5482J, N	9
US5482J	SN5482W	SN5482W	9
US5483A	SN5483J, N	SN5483J, N	9
US5484A	SN5484J, N	SN5484J, N	9
US5484J	SN5484W	SN5484W	9
US5486A	SN5486J, N	SN5486J, N	9
US5486J	SN5486W	SN5486W	9
US5490A	SN5490J, N	SN5490J, N	9
US5490J	SN5490W	SN5490W	9
US5491A	SN5491AJ, N	SN5491AJ, N	9
US5491J	SN5491AW	SN5491AW	9
US5492A	SN5492J, N	SN5492J, N	9
US5492J	SN5492W	SN5492W	9
US5493A	SN5493J, N	SN5493J, N	9
US5493J	SN5493W	SN5493W	9
US5494A	SN5494J, N	SN5494J, N	9
US5494J	SN5494W	SN5494W	9
US5495A	SN5495AJ, N	SN5495AJ, N	9
US5495J	SN5495AW	SN5495AW	9
US5496A	SN5496J, N	SN5496J, N	9
US5496J	SN5496W	SN5496W	9
US54107A	SN54107J, N	SN54107J, N	6
US54121A	SN54121J, N	SN54121J, N	6
US54121J	SN54121W	SN54121W	6
US54122A	SN54122J, N	SN54122J, N	6
US54122J	SN54122W	SN54122W	6
US54123A	SN54123J, N	SN54123J, N	6
US54123J	SN54123W	SN54123W	6
US54145A	SN54145J, N	SN54145J, N	9
US54145J	SN54145W	SN54145W	9
US54150A	SN54150J, N	SN54150J, N	9
US54150J	SN54150W	SN54150W	9
US54151A	SN54151J, N	SN54151J, N	9
US54151J	SN54151W	SN54151W	9
US54153A	SN54153J, N	SN54153J, N	9
US54153J	SN54153W	SN54153W	9
US54154A	SN54154J, N	SN54154J, N	9
US54154J	SN54154W	SN54154W	9
US54164A	SN54164J, N	SN54164J, N	9
US54164J	SN54164W	SN54164W	9
US54165A	SN54165J, N	SN54165J, N	9
US54165J	SN54165W	SN54165W	9
US54180A	SN54180J, N	SN54180J, N	9
US54180J	SN54180W	SN54180W	9
US54181A	SN54181J, N	SN54181J, N	9
US54181J	SN54181W	SN54181W	9
US54182A	SN54182J, N	SN54182J, N	9
US54182J	SN54182W	SN54182W	9
US54192A	SN54192J, N	SN54192J, N	9
US54192J	SN54192W	SN54192W	9
US54193A	SN54193J, N	SN54193J, N	9
US54193J	SN54193W	SN54193W	9
US7400A	SN7400J, N	SN7400J, N	6
US7400J	SN7400W	SN7400W	6
US7401A	SN7401J, N	SN7401J, N	6
US7401J	SN7401W	SN7401W	6
US7402A	SN7402J, N	SN7402J, N	6
US7402J	SN7402W	SN7402W	6
US7403A	SN7403J, N	SN7403J, N	6
US7404A	SN7404J, N	SN7404J, N	6
US7404J	SN7404W	SN7404W	6

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Type Number	Direct Replacement	Recommended for New Designs	Sec.
US7405A	SN7405J, N	SN7405J, N	6
US7405J	SN7405W	SN7405W	6
US7408A	SN7408J, N	SN7408J, N	6
US7408J		SN7408W	6
US7409A	SN7409J, N	SN7409J, N	6
US7409J		SN7409W	6
US7410A	SN7410J, N	SN7410J, N	6
US7410J	SN7410W	SN7410W	6
US7420A	SN7420J, N	SN7420J, N	6
US7420J	SN7420W	SN7420W	6
US7426J	SN7426J, N	SN7426J, N	6
US7427A	SN7427J, N	SN7427J, N	6
US7427J		SN7427W	6
US7429A	SN7425J, N	SN425J, N	6
US7429J		SN425W	6
US7430A	SN7430J, N	SN7430J, N	6
US7430J	SN7430W	SN7430W	6
US7432A	SN7432J, N	SN7432J, N	6
US7432J		SN7432W	6
US7438A	SN7438J, N	SN7438J, N	6
US7438J		SN7438W	6
US7439A		SN7438J, N	6
US7439J		SN7438W	6
US7440A	SN7440J, N	SN7440J, N	6
US7440J	SN7440W	SN7440W	6
US7441A	SN74141J, N	SN74141J, N	9
US7442A	SN7442J, N	SN7442J, N	9
US7442J	SN7442W	SN7442W	9
US7443A	SN7443J, N	SN7443J, N	9
US7443J	SN7443W	SN7443W	9
US7444A	SN7444J, N	SN7444J, N	9
US7444J	SN7444W	SN7444W	9
US7445A	SN7445J, N	SN7445J, N	9
US7445J	SN7445W	SN7445W	9
US7446A	SN7446AJ, N	SN7446AJ, N	9
US7446J	SN7446AW	SN7446AW	9
US7447A	SN7447AJ, N	SN7447AJ, N	9
US7447J	SN7447AW	SN7447AW	9
US7448A	SN7448J, N	SN7448J, N	9
US7448J	SN7448W	SN7448W	9
US7450A	SN7450J, N	SN7450J, N	6
US7450J	SN7450W	SN7450W	6
US7451A	SN7451J, N	SN7451J, N	6
US7451J	SN7451W	SN7451W	6
US7453A	SN7453J, N	SN7453J, N	6
US7453J	SN7453W	SN7453W	6
US7454A	SN7454J, N	SN7454J, N	6
US7454J	SN7454W	SN7454W	6
US7459A		SN7451J, N	6
US7459J		SN7451W	6
US7460A	SN7460J, N	SN7460J, N	6
US7460J	SN7460W	SN7460W	6
US7470A	SN7470J, N	SN7470J, N	6
US7470J	SN7470W	SN7470W	6
US7472A	SN7472J, N	SN7472J, N	6
US7472J	SN7472W	SN7472W	6
US7473A	SN7473J, N	SN7473J, N	6
US7473J	SN7473W	SN7473W	6
US7474A	SN7474J, N	SN7474J, N	6
US7474J	SN7474W	SN7474W	6
US7475A	SN7475J, N	SN7475J, N	9
US7476A	SN7476J, N	SN7476J, N	6
US7477J	SN7477W	SN7477W	9
US7480A	SN7480J, N	SN7480J, N	9
US7480J	SN7480W	SN7480	9
US7481A	SN7481J, N	SN7481J, N	9
US7481J	SN7481W	SN7481W	9
US7482A	SN7482J, N	SN7482J, N	9
US7482J	SN7482W	SN7482W	9
US7483A	SN7483J, N	SN7483J, N	9
US7484A	SN7484J, N	SN7484J, N	9
US7484J	SN7484W	SN7484W	9
US7486A	SN7486J, N	SN7486J, N	9
US7486J	SN7486W	SN7486W	9
US7490A	SN7490J, N	SN7490J, N	9
US7490J	SN7490W	SN7490W	9
US7491A	SN7491AJ, N	SN7491AJ, N	9
US7491J	SN7491AW	SN7491AW	9
US7492A	SN7492J, N	SN7492J, N	9
US7492J	SN7492W	SN7492W	9
US7493A	SN7493J, N	SN7493J, N	9
US7493J	SN7493W	SN7493W	9
US7494A	SN7494J, N	SN7494J, N	9
US7494J	SN7494W	SN7494W	9
US7495A	SN7495AJ, N	SN7495AJ, N	9
US7495J	SN7495AW	SN7495AW	9
US7496A	SN7496J, N	SN7596J, N	9
US7496J	SN7496W	SN7496W	9
US74107A	SN74107J, N	SN74107J, N	6
US74121A	SN74121J, N	SN74121J, N	6
US74121J	SN74121W	SN74121W	6
US74122A	SN74122J, N	SN74122J, N	6
US75122J	SN74122W	SN74122W	6
US74123A	SN74123J, N	SN74123J, N	6
US74123J	SN74123W	SN74123W	6
US74145A	SN74145J, N	SN74145J, N	9
US74150A	SN74150J, N	SN74150J, N	9
US74150J	SN74150W	SN74150W	9
US74151A	SN74151J, N	SN74151J, N	9
US74151J	SN74151W	SN74151W	9
US74153A	SN74153J, N	SN74153J, N	9
US74153J	SN74153W	SN74153W	9
US74154A	SN74154J, N	SN74154J, N	9
US74154J	SN74154W	SN74154W	9
US74164A	SN74164J, N	SN74164J, N	9
US74164J	SN74164W	SN74164W	9
US74165A	SN74165J, N	SN74165J, N	9
US74165J	SN74165W	SN74165W	9
US74180A	SN74180J, N	SN74180J, N	9
US74180J	SN74180W	SN74180W	9
US74181A	SN74181J, N	SN74181J, N	9
US74181J	SN74181W	SN74181W	9
US74182A	SN74182J, N	SN74182J, N	9
US74182J	SN74182W	SN74182W	9
US74192A	SN74192J, N	SN74192J, N	9
US74192J	SN74192W	SN74192W	9
US74193A	SN74193J, N	SN74193J, N	9
US74193J	SN74193W	SN74193W	9
US54H00A	SN54H00J, N	SN54H00J, N	7
US54H00J	SN54H00W	SN54H00W	7
US54H01A	SN54H01J, N	SN54H01J, N	7
US54H01J	SN54H01W	SN54H01W	7
US54H04A	SN54H04J, N	SN54H04J, N	7
US54H04J	SN54H04W	SN54H04W	7
US54H05A	SN54H05J, N	SN54H05J, N	7
US54H05J	SN54H05W	SN54H05W	7
US54H10A	SN54H10J, N	SN54H10J, N	7
US54H10J	SN54H10W	SN54H10W	7
US54H11A	SN54H11J, N	SN54H11J, N	7
US54H11J	SN54H11W	SN54H11W	7
US54H20A	SN54H20J, N	SN54H20J, N	7
US54H20J	SN54H20W	SN54H20W	7
US54H21A	SN54H21J, N	SN54H21J, N	7
US54H21J	SN54H21W	SN54H21W	7
US54H22A	SN54H22J, N	SN54H22J, N	7
US54H22J	SN54H22W	SN54H22W	7

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US54H30A	SN54H30J, N	SN54H30J, N	7
US54H30J	SN54H30W	SN54H30W	7
US54H40A	SN54H40J, N	SN54H40J, N	7
US54H40J	SN54H40W	SN54H40W	7
US54H50A	SN54H50J, N	SN54H50J, N	7
US54H50J	SN54H50W	SN54H50W	7
US54H51A	SN54H51J, N	SN54H51J, N	7
US54H51J	SN54H51W	SN54H51W	7
US54H52A	SN54H52J, N	SN54H52J, N	7
US54H52J	SN54H52W	SN54H52W	7
US54H53A	SN54H53J, N	SN54H52J, N	7
US54H53J	SN54H53W	SN54H53W	7
US54H54A	SN54H54J, N	SN54H54J, N	7
US54H54J	SN54H54W	SN54H54W	7
US54H55A	SN54H55J, N	SN54H55J, N	7
US54H55J	SN54H55W	SN54H55W	7
US54H60A	SN54H60J, N	SN54H60J, N	7
US54H60J	SN54H60W	SN54H60W	7
US54H61A	SN54H61J, N	SN54H61J, N	7
US54H61J	SN54H61W	SN54H61W	7
US54H62A	SN54H62J, N	SN54H62J, N	7
US54H62J	SN54H62W	SN54H62W	7
US54H71A	SN54H71J, N	SN54H71J, N	7
US54H71J	SN54H71W	SN54H71W	7
US54H72A	SN54H72J, N	SN54H72J, N	7
US54H72J	SN54H72W	SN54H72W	7
US54H73A	SN54H73J, N	SN54H73J, N	7
US54H73J	SN54H73W	SN54H73W	7
US54H76A	SN54H76J, N	SN54H76J, N	7
US54H76J	SN54H76W	SN54H76W	7
US54H78A	SN54H78J, N	SN54H78J, N	7
US54H78J	SN54H78W	SN54H78W	7
US74H00A	SN74H00J, N	SN74H00J, N	7
US74H00J	SN74H00W	SN74H00W	7
US74H01A	SN74H01J, N	SN74H01J, N	7
US74H01J	SN74H01W	SN74H01W	7
US74H04A	SN74H04J, N	SN74H04J, N	7
US74H04J	SN74H04W	SN74H04W	7
US74H05A	SN74H05J, N	SN74H05J, N	7
US74H05J	SN74H05W	SN74H05W	7
US74H10A	SN74H10J, N	SN74H10J, N	7
US74H10J	SN74H10W	SN74H10W	7
US74H11A	SN74H11J, N	SN74H11J, N	7
US74H11J	SN74H11W	SN74H11W	7
US74H20A	SN74H20J, N	SN74H20J, N	7
US74H20J	SN74H20W	SN74H20W	7
US74H21A	SN74H21J, N	SN74H21J, N	7
US74H21J	SN74H21W	SN74H21W	7
US74H22A	SN74H22J, N	SN74H22J, N	7
US74H22J	SN74H22W	SN74H22W	7
US74H30A	SN74H30J, N	SN74H30J, N	7
US74H30J	SN74H30W	SN74H30W	7
US74H40A	SN74H40J, N	SN74H40J, N	7
US74H40J	SN74H40W	SN74H40W	7
US74H50A	SN74H50J, N	SN74H50J, N	7
US74H50J	SN74H50W	SN74H50W	7
US74H51A	SN74H51J, N	SN74H51J, N	7
US74H51J	SN74H51W	SN74H51W	7
US74H52A	SN74H52J, N	SN74H52J, N	7
US74H52J	SN74H52W	SN74H52W	7
US74H53A	SN74H53J, N	SN74H53J, N	7
US74H53J	SN74H53W	SN74H53W	7
US74H54A	SN74H54J, N	SN74H54J, N	7
US74H54J	SN74H54W	SN74H54W	7
US74H55A	SN74H55J, N	SN74H55J, N	7
US74H55J	SN74H55W	SN74H55W	7
US74H60A	SN75H60J, N	SN74H60J, N	7
US74H60J	SN74H60W	SN74H60W	7
US74H61A	SN74H61J, N	SN74H61J, N	7
US74H61J	SN74H61W	SN74H61W	7
US74H62A	SN74H62J, N	SN74H62J, N	7
US74H62J	SN74H62W	SN74H62W	7
US74H71A	SN74H71J, N	SN74H71J, N	7
US74H71J	SN74H71W	SN74H71W	7
US74H72A	SN74H72J, N	SN74H72J, N	7
US74H72J	SN74H72W	SN74H72W	7
US74H73A	SN74H73J, N	SN74H73J, N	7
US74H73J	SN74H73W	SN74H73W	7
US74H76A	SN74H76J, N	SN74H76J, N	7
US75H76J	SN74H76W	SN74H76W	7
US74H78A	SN74H78J, N	US74H78J, N	7
US74H78J	SN74H78W	US74H78W	7

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Type Number	Direct Replacement	Recommended for New Designs	Sec.
SN5400F	SN5400W	SN5400W	6
SN5400J, N	SN5400J, N	SN5400J, N	6
SN5401F	SN5401W	SN5401W	6
SN5401J, N	SN5401J, N	SN5401J, N	6
SN5402F	SN5402W	SN5402W	6
SN5402J, N	SN5402J, N	SN5402J, N	6
SN5404F	SN5404W	SN5404W	6
SN5404J, N	SN5404J, N	SN5404J, N	6
SN5405F	SN5405W	SN5405W	6
SN5405J, N	SN5405J, N	SN5405J, N	6
SN5410F	SN5410W	SN5410W	6
SN5410J, N	SN5410J, N	SN5410J, N	6
SN5420F	SN5420W	SN5420W	6
SN5420J, N	SN5420J, N	SN5420J, N	6
SN5430F	SN5430W	SN5430W	6
SN5430J, N	SN5430J, N	SN5430J, N	6
SN5440F	SN5440W	SN5440W	6
SN5440J, N	SN5440J, N	SN5440J, N	6
SN5441AJ, N	SN54141J, N	SN54141J, N	9
SN5442J, N	SN5442J, N	SN5442J, N	9
SN5443J, N	SN5443J, N	SN5443J, N	9
SN5444J, N	SN5444J, N	SN5444J, N	9
SN5450F	SN5450W	SN5450W	6
SN5450J, N	SN5450J, N	SN5450J, N	6
SN5451F	SN5451W	SN5451W	6
SN5451J, N	SN5451J, N	SN5451J, N	6
SN5453F	SN5453W	SN5453W	6
SN5453J, N	SN5453J, N	SN5453J, N	6
SN5454F	SN5454W	SN5454W	6
SN5454J, N	SN5454J, N	SN5454J, N	6
SN5460F	SN5460W	SN5460W	6
SN5460J, N	SN5460J, N	SN5460J, N	6
SN5470F	SN5470W	SN5470W	6
SN5470J, N	SN5470J, N	SN5470J, N	6

DTL/TTL CIRCUITS

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B

Type Number	Direct Replacement	Recommended for New Designs	Sec.
SN5472F	SN5472W	SN5472W	6
SN5472J, N	SN5472J, N	SN5472J, N	6
SN5473F	SN5473W	SN5473W	6
SN5473J, N	SN5473J, N	SN5473J, N	6
SN5474F	SN5474W	SN5474W	6
SN5474J, N	SN5474J, N	SN5474J, N	6
SN5475J, N	SN5475J, N	SN5475J, N	9
SN5476J, N	SN5476J, N	SN5476J, N	6
SN5480F	SN5480W	SN5480W	9
SN5480J, N	SN5480J, N	SN5480J, N	9
SN5482F	SN5482W	SN5482W	9
SN5482J, N	SN5482J, N	SN5482J, N	9
SN5483J, N	SN5483J, N	SN5483J, N	9
SN5490F	SN5490W	SN5490W	9
SN5490J, N	SN5490J, N	SN5490J, N	9
SN5491AF	SN5491AW	SN5491AW	9
SN5491AJ, N	SN5491AJ, N	SN5491AJ, N	9
SN5492F	SN5492W	SN5492W	9
SN5492J, N	SN5492J, N	SN5492J, N	9
SN5493F	SN5493W	SN5493W	9
SN5493J, N	SN5493J, N	SN5493J, N	9
SN5494J, N	SN5494J, N	SN5494J, N	9
SN5495F	SN5495AW	SN5495AW	9
SN5495J, N	SN5495AJ, N	SN5495AJ, N	9
SN5496J, N	SN5496J, N	SN5496J, N	9
SN54107J, N	SN54107J, N	SN54107J, N	6
SN54121F	SN54121W	SN54121W	6
SN54121J, N	SN54121J, N	SN54121J, N	6
SN542511F		SN54197W	9
SN542511J, N		SN54197J, N	9
SN542515F		SN54196W	9
SN542515J, N		SN54196J, N	9
SN542525F		SN54194W	9
SN542525J, N		SN54194J, N	9
SN543163F	SN5481W	SN5489W	9
SN543163J, N	SN5481J, N	SN5489J, N	9
SN545511F		SN5437W	6
SN545511J, N		SN5437J, N	6
SN545611F		SN5438W	6
SN545611J, N		SN5438J, N	6
SN548280F		SN54196W	9
SN548280J, N		SN54196J, N	9
SN548281F		SN54197W	9
SN548281J, N		SN54197J, N	9
SN7400F	SN7400W	SN7400W	6
SN7400J, N	SN7400J, N	SN7400J, N	6
SN7401F	SN7401W	SN7401W	6
SN7401J, N	SN7401J, N	SN7401J, N	6
SN7402F	SN7402W	SN7402W	6
SN7402J, N	SN7402J, N	SN7402J, N	6
SN7404F	SN7404W	SN7404W	6
SN7404J, N	SN7404J, N	SN7404J, N	6
SN7405F	SN7405W	SN7405W	6
SN7405J, N	SN7405J, N	SN7405J, N	6
SN7410F	SN7410W	SN7410W	6
SN7410J, N	SN7410J, N	SN7410J, N	6
SN7420F	SN7420W	SN7420W	6
SN7420J, N	SN7420J, N	SN7420J, N	6
SN7430F	SN7430W	SN7430W	6
SN7430J, N	SN7430J, N	SN7430J, N	6
SN7440F	SN7440W	SN7440W	6
SN7440J, N	SN7440J, N	SN7440J, N	6
SN7441AJ, N	SN74141J, N	SN74141J, N	9
SN7442J, N	SN7442J, N	SN7442J, N	9
SN7443J, N	SN7443J, N	SN7443J, N	9
SN7444J, N	SN7444J, N	SN7444J, N	9
SN7450F	SN7450W	SN7450W	6
SN7450J, N	SN7450J, N	SN7450J, N	6
SN7451F	SN7451W	SN7451W	6
SN7451J, N	SN7451J, N	SN7451J, N	6
SN7453F	SN7453W	SN7453W	6
SN7453J, N	SN7453J, N	SN7453J, N	6
SN7454F	SN7454W	SN7454W	6
SN7454J, N	SN7454J, N	SN7454J, N	6
SN7460F	SN7460W	SN7460W	6
SN7460J, N	SN7460J, N	SN7460J, N	6
SN7470F	SN7470W	SN7470W	6
SN7470J, N	SN7470J, N	SN7470J, N	6
SN7472F	SN7472W	SN7472W	6
SN7472J, N	SN7472J, N	SN7472J, N	6
SN7473F	SN7473W	SN7473W	6
SN7473J, N	SN7473J, N	SN7473J, N	6
SN7474F	SN7474W	SN7474W	6
SN7474J, N	SN7474J, N	SN7474J, N	6
SN7475J, N	SN7475J, N	SN7475J, N	9
SN7476J, N	SN7476J, N	SN7476J, N	6
SN7480F	SN7480W	SN7480W	9
SN7480J, N	SN7480J, N	SN7480J, N	9
SN7482F	SN7482W	SN7482W	9
SN7482J, N	SN7482J, N	SN7482J, N	9
SN7483J, N	SN7483J, N	SN7483J, N	9
SN7490F	SN7490W	SN7490W	9
SN7490J, N	SN7490J, N	SN7490J, N	9
SN7491AF	SN7491AW	SN7491AW	9
SN7491AJ, N	SN7491AJ, N	SN7491AJ, N	9
SN7492F	SN7492W	SN7492W	9
SN7492J, N	SN7492J, N	SN7492J, N	9
SN7493F	SN7493W	SN7493W	9
SN7493J, N	SN7493J, N	SN7493J, N	9
SN7494J, N	SN7494J, N	SN7494J, N	9
SN7495F	SN7495AW	SN7495AW	9
SN7495J, N	SN7495AJ, N	SN7495AJ, N	9
SN7496J, N	SN7496J, N	SN7496J, N	9
SN74107J, N	SN74107J, N	SN74107J, N	6
SN74121F	SN74121W	SN74121W	6
SN74121J, N	SN74121J, N	SN74121J, N	6
SN742512F		SN74197W	9
SN74212J, N		SN74197J, N	9
SN742516F		SN74196W	9
SN742516J, N		SN74196J, N	9
SN742526F		SN74194W	9
SN742526J, N		SN74194J, N	9
SN743162F	SN7481W	SN7489W	9
SN743162J, N	SN7481J, N	SN7489J, N	9
SN743164F	SN7481W	SN7489W	9
SN743164J, N	SN7481J, N	SN7489J, N	9
SN745512F		SN7437W	6
SN745512J, N		SN7437J, N	6
SN745612F		SN7438W	6
SN745612J, N		SN7438J, N	6
SN748280F		SN74196W	9
SN748280J, N		SN74196J, N	9
SN748281F		SN74197W	9
SN748281J, N		SN74197J, N	9
TA10E, J		SN54H183J, N	9
TA10F		SN54H183W	9
TA11E, J		SN54H183J, N	9
TA11F		SN54H183W	9
TA12E, J		SN74H183J, N	9
TA12F		SN74H183W	9
TA13E, J		SN74H183J, N	9
TA13F		SN74H183W	9
TA20E, J	SNE20J, N	SN54181J, N	9
TA20F	SNE20U	SN54181W	9

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Type Number	Direct Replacement	Recommended for New Designs	Sec.
TA21E, J	SNE21J, N	SN54181J, N	9
TA21F	SNE21U	SN54181W	9
TA22E, J	SNE22J, N	SN74181J, N	9
TA22F	SNE22U	SN74181W	9
TA23E, J	SNE23J, N	SN74181J, N	9
TA23F	SNE23U	SN74181W	9
TA30E, J	SNE30J, N	SN54181J, N	9
TA30F	SNE30U	SN54181W	9
TA31E, J	SNE31J, N	SN54181J, N	9
TA31F	SNE31U	SN54181W	9
TA32E, J	SNE32J, N	SN74181J, N	9
TA32F	SNE32U	SN74181W	9
TA33E, J	SNE33J, N	SN74181J, N	9
TA33F	SNE33U	SN74181W	9
TC11E, J		SN54163J, N	9
TC11F		SN54163W	9
TC12E, J		SN74163J, N	9
TC12F		SN74163W	9
TC13E, J		SN54163J, N	9
TC13F		SN54163W	9
TC14E, J		SN74163J, N	9
TC14F		SN74163W	9
TC15E, J		SN54162J, N	9
TC15F		SN54162W	9
TC16E, J		SN74162J, N	9
TC16F		SN74162W	9
TC17E, J		SN54162J, N	9
TC17F		SN54162W	9
TC18E, J		SN74162J, N	9
TC18F		SN74162W	9
TD40E, J	SNE40J, N	SN54182J, N	9
TD40F	SNE40U	SN54182W	9
TD42E, J	SNE42J, N	SN74182J, N	9
TD42F	SNE42U	SN74182W	9
TF20E, J	SNF20J, N	SN5472J, N	6
TF20F	SNF20U	SN5472W	6
TF21E, J	SNF21J, N	SN5472J, N	6
TF21F	SNF21U	SN5472W	6
TF22E, J	SNF22J, N	SN7472J, N	6
TF22F	SNF22U	SN7472W	6
TF23E, J	SNF23J, N	SN7472J, N	6
TF23F	SNF23U	SN7472W	6
TF50E, J	SNF50J, N	SN5470J, N	6
TF50F	SNF50U	SN5470W	6
TF51E, J	SNF51J, N	SN5470J, N	6
TF51F	SNF51U	SN5470W	6
TF52E, J	SNF52J, N	SN7470J, N	6
TF52F	SNF52U	SN7470W	6
TF53E, J	SNF53J, N	SN7470J, N	6
TF53F	SNF53U	SN7470W	6
TF60E, J	SNF60J, N	SN54H101J, N	7
TF60F	SNF60U	SN54H101W	7
TF61E, J	SNF61J, N	SN54H101J, N	7
TF61F	SNF61U	SN54H101W	7
TF62E, J	SNF62J, N	SN74H101J, N	7
TF62F	SNF62U	SN74H101W	7
TF63E, J	SNF63J, N	SN74H101J, N	7
TF63F	SNF63U	SN74H101W	7
TF100E, J	SNF100J, N	SN54H103J, N	7
TF100F	SNF100U	SN54H103W	7
TF101E, J	SNF101J, N	SN54H103J, N	7
TF101F	SNF101U	SN54H103W	7
TF102E, J	SNF102J, N	SN74H103J, N	7
TF102F	SNF102U	SN74H103W	7
TF103E, J	SNF103J, N	SN74H103J, N	7
TF103F	SNF103U	SN74H103W	7

Type Number	Direct Replacement	Recommended for New Designs	Sec.
TF110E, J	SNF110J, N	SN54H108J, N	7
TF110F	SNF110U	SN54H108W	7
TF111E, J	SNF111J, N	SN54H108J, N	7
TF111F	SNF111U	SN54H108W	7
TF112E, J	SNF112J, N	SN74H108J, N	7
TF112F	SNF112U	SN74H108W	7
TF113E, J	SNF113J, N	SN74H108J, N	7
TF113F	SNF113U	SN74H108W	7
TF120E, J	SNF120J, N	SN54H103J, N	7
TF120F	SNF120U	SN54H103W	7
TF121E, J	SNF121J, N	SN54H103J, N	7
TF121F	SNF121U	SN54H103W	7
TF122E, J	SNF122J, N	SN74H103J, N	7
TF122F	SNF122U	SN74H103W	7
TF123E, J	SNF123J, N	SN74H103J, N	7
TF123F	SNF123U	SN74H103W	7
TF130E, J	SNF130J, N	SN54H108J, N	7
TF130F	SNF130U	SN54H108W	7
TF131E, J	SNF131J, N	SN54H108J, N	7
TF131F	SNF131U	SN54H108W	7
TF132E, J	SNF132J, N	SN74H108J, N	7
TF132F	SNF132U	SN74H108W	7
TF133E, J	SNF133J, N	SN74H108J, N	7
TF133F	SNF133U	SN74H108W	7
TF200E, J	SNF200J, N	SN54H102J, N	7
TF200F	SNF200U	SN54H102W	7
TF201E, J	SNF201J, N	SN54H102J, N	7
TF201F	SNF201U	SN54H102W	7
TF202E, J	SNF202J, N	SN74H102J, N	7
TF202F	SNF202U	SN74H102W	7
TF203E, J	SNF203J, N	SN74H102J, N	7
TF203F	SNF203U	SN74H102W	7
TF210E, J	SNF210J, N	SN54H101J, N	7
TF210F	SNF210U	SN54H101W	7
TF211E, J	SNF211J, N	SN54H101J, N	7
TF211F	SNF211U	SN54H101W	7
TF212E, J	SNF212J, N	SN74H101J, N	7
TF212F	SNF212U	SN74H101W	7
TF213E, J	SNF213J, N	SN74H101J, N	7
TF213F	SNF213U	SN74H101W	7
TF250E, J	SNF250J, N	SN54H102J, N	7
TF250F	SNF250U	SN54H102W	7
TF251E, J	SNF251J, N	SN54H102J, N	7
TF251F	SNF251U	SN54H102W	7
TF252E, J	SNF252J, N	SN74H102J, N	7
TF252F	SNF252U	SN74H102W	7
TF253E, J	SNF253J, N	SN74H102J, N	7
TF253F	SNF253U	SN74H102W	7
TF260E, J	SNF260J, N	SN54H101J, N	7
TF260F	SNF260U	SN54H101W	7
TF261E, J	SNF261J, N	SN54H101J, N	7
TF261F	SNF261U	SN54H101W	7
TF262E, J	SNF262J, N	SN74H101J, N	7
TF262F	SNF262U	SN74H101W	7
TF263E, J	SNF263J, N	SN74101J, N	7
TF263F	SNF263U	SN74H101W	7
TG40E, J	SNG40J, N	SN5420J, N	6
TG40F	SNG40U	SN5420W	6
TG41E, J	SNG41J, N	SN5420J, N	6
TG41F	SNG41U	SN5420W	6
TG42E, J	SNG42J, N	SN7420J, N	6
TG42F	SNG42U	SN7420W	6
TG43E, J	SNG43J, N	SN7420J, N	6
TG43F	SNG43U	SN7420W	6
TG50E, J	SN50J, N	SN5453J, N	6
TG50F	SNG50U	SN5453W	6

DTL/TTL CIRCUITS

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Type Number	Direct Replacement	Recommended for New Designs	Sec.
TG51E, J	SNG51J, N	SN5453J, N	6
TG51F	SNG51U	SN5453W	6
TG52E, J	SNG52J, N	SN7453J, N	6
TG52F	SNG52U	SN7453W	6
TG53E, J	SNG53J, N	SN7453J, N	6
TG53F	SNG53U	SN7453W	6
TG60E, J	SNG60J, N	SN5430J, N	6
TG60F	SNG60U	SN5430W	6
TG61E, J	SNG61J, N	SN5430J, N	6
TG61F	SNG61U	SN5430W	6
TG62E, J	SNG62J, N	SN7430J, N	6
TG62F	SNG62U	SN7430W	6
TG63E, J	SNG63J, N	SN7430J, N	6
TG63F	SNG63U	SN7430W	6
TG70E, J	SNG70J, N	SN5450J, N	6
TG70F	SNG70U	SN5450W	6
TG71E, J	SNG71J, N	SN5450J, N	6
TG71F	SNG71U	SN5450W	6
TG72E, J	SNG72J, N	SN7450J, N	6
TG72F	SNG72U	SN7450W	6
TG73E, J	SNG73J, N	SN7450J, N	6
TG73F	SNG73U	SN7450W	6
TG80E, J	SNG80J, N	SN5413J, N	6
TG80F	SNG80U	SN5413W	6
TG81E, J	SNG81J, N	SN5413J, N	6
TG81F	SNG81U	SN5413W	6
TG82E, J	SNG82J, N	SN7413J, N	6
TG82F	SNG82U	SN7413W	6
TG83E, J	SNG83J, N	SN7413J, N	6
TG83F	SNG83U	SN7413W	6
TG90E, J	SNG90J, N	SN5486J, N	9
TG90F	SNG90U	SN5486W	9
TG91E, J	SNG91J, N	SN5486J, N	9
TG91F	SNG91U	SN5486W	9
TG92E, J	SNG92J, N	SN7486J, N	9
TG92F	SNG92U	SN7486W	9
TG93E, J	SNG93J, N	SN7486J, N	9
TG93F	SNG93U	SN7486W	9
TG100E, J	SNG100J, N	SN5453J, N	6
TG100F	SNG100U	SN5453W	6
TG101E, J	SNG101J, N	SN5453J, N	6
TG101F	SNG101U	SN5453W	6
TG102E, J	SNG102J, N	SN7453J, N	6
TG102F	SNG102U	SN7453W	6
TG103E, J	SNG103J, N	SN7453J, N	6
TG103F	SNG103U	SN7453W	6
TG110E, J	SNG110J, N	SN54H55J, N	7
TG110F	SNG110U	SN54H55W	7
TG111E, J	SNG111J, N	SN54H55J, N	7
TG111F	SNG111U	SN54H55W	7
TG112E, J	SNG112J, N	SN74H55J, N	7
TG112F	SNG112U	SN74H55W	7
TG113E, J	SNG113J, N	SN74H55J, N	7
TG113F	SNG113U	SN74H55W	7
TG120E, J	SNG120J, N	SN5430J, N	6
TG120F	SNG120U	SN5430W	6
TG121E, J	SNG121J, N	SN5430J, N	6
TG121F	SNG121U	SN5430W	6
TG122E, J	SNG122J, N	SN7430J, N	6
TG122F	SNG122U	SN7430W	6
TG123E, J	SNG123J, N	SN7430J, N	6
TG123F	SNG123U	SN7430W	6
TG130E, J	SNG130J, N	SN54S140J, N	5
TG130F	SNG130U	SN54S140W	5
TG131E, J	SNG131J, N	SN54S140J, N	5
TG131F	SNG131U	SN54S140W	5
TG132E, J	SNG132J, N	SN74S140J, N	5
TG132F	SNG132U	SN74S140W	5
TG133E, J	SNG133J, N	SN74S140J, N	5
TG133F	SNG133U	SN74S140W	5
TG140E, J	SNG140J, N	SN5400J, N	6
TG140F	SNG140U	SN5400W	6
TG141E, J	SNG141J, N	SN5400J, N	6
TG141F	SNG141U	SN5400W	6
TG142E, J	SNG142J, N	SN7400J, N	6
TG142F	SNG142U	SN7400W	6
TG143E, J	SNG143J, N	SN7400J, N	6
TG143F	SNG143U	SN7400W	6
TG150E, J	SNG150J, N	SN54H62J, N	7
TG150F	SNG150U	SN54H62W	7
TG151E, J	SNG151J, N	SN54H62J, N	7
TG151F	SNG151U	SN54H62W	7
TG152E, J	SNG152J, N	SN74H62J, N	7
TG152F	SNG152U	SN74H62W	7
TG153E, J	SNG153J, N	SN74H62J, N	7
TG153F	SNG153U	SN74H62W	7
TG160E, J	SNG160J, N	SN5438J, N	6
TG160F	SNG160U	SN5438W	6
TG161E, J	SNG161J, N	SN5438J, N	6
TG161F	SNG161U	SN5438W	6
TG162E, J	SNG162J, N	SN7438J, N	6
TG162F	SNG162U	SN7438W	6
TG163E, J	SNG163J, N	SN7438J, N	6
TG163F	SNG163U	SN7438W	6
TG170E, J	SNG170J, N	SN5460J, N	6
TG170F	SNG170U	SN5460W	6
TG171E, J	SNG171J, N	SN5460J, N	6
TG171F	SNG171U	SN5460W	6
TG172E, J	SNG172J, N	SN7460J, N	6
TG172F	SNG172U	SN7460W	6
TG173E, J	SNG173J, N	SN7460J, N	6
TG173F	SNG173U	SN7460W	6
TG180E, J	SNG180J, N	SN5430J, N	6
TG180F	SNG180U	SN5430W	6
TG181E, J	SNG181J, N	SN5430J, N	6
TG181F	SNG181U	SN5430W	6
TG182E, J	SNG182J, N	SN7430J, N	6
TG182F	SNG182U	SN7430W	6
TG183E, J	SNG183J, N	SN7430J, N	6
TG183F	SNG183U	SN7430W	6
TG190E, J	SNG190J, N	SN5410J, N	6
TG190F	SNG190U	SN5410W	6
TG191E, J	SNG191J, N	SN5410J, N	6
TG191F	SNG191U	SN5410W	6
TG192E, J	SNG192J, N	SN7410J, N	6
TG192F	SNG192U	SN7410W	6
TG193E, J	SNG193J, N	SN7410J, N	6
TG193F	SNG193U	SN7410W	6
TG200E, J	SNG200J, N	SN54H30J, N	7
TG200F	SNG200U	SN54H30W	7
TG201E, J	SNG201J, N	SN54H30J, N	7
TG201F	SNG201W	SN54H30W	7
TG202E, J	SNG202J, N	SN74H30J, N	7
TG202F	SNG202U	SN74H30W	7
TG203E, J	SNG203J, N	SN74H30J, N	7
TG203F	SNG203U	SN74H30W	7
TG210E, J	SNG210J, N	SN5455J, N	7
TG210F	SNG210U	SN54H55W	7
TG211E, J	SNG211J, N	SN54H55J, N	7
TG211F	SNG211U	SN54H55W	7
TG212E, J	SNG212J, N	SN74H55J, N	7
TG212F	SNG212U	SN74H55W	7
TG213E, J	SNG213J, N	SN74H55J, N	7
TG213F	SNG213U	SN74H55W	7
TG220E, J	SNG220J, N	SN54H00J, N	7
TG220F	SNG220U	SN54H00W	7

TEXAS INSTRUMENTS
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DTL/TTL CIRCUITS

Transitron TTL, Cont.

Type Number	Direct Replacement	Recommended for New Designs	Sec.
TG221E, J	SNG221J, N	SN54H00J, N	7
TG221F	SNG221U	SN54H00W	7
TG222E, J	SNG222J, N	SN74H00J, N	7
TG222F	SNG222U	SN74H00W	7
TG223E, J	SNG223J, N	SN74H00J, N	7
TG223F	SNG223U	SN74H00W	7
TG230E, J	SGN230J, N	SN54H62J, N	7
TG230F	SNG230U	SN54H62W	7
TG231E, J	SNG231J, N	SN54H62J, N	7
TG231F	SNG231U	SN54H62W	7
TG232E, J	SNG232J, N	SN74H62J, N	7
TG232F	SNG232U	SN74H62W	7
TG233E, J	SNG233J, N	SN74H62J, N	7
TG233F	SNG233W	SN74H62W	7
TG240E, J	SNG240J, N	SN54H20J, N	7
TG240F	SNG240U	SN54H20W	7
TG241E, J	SNG241J, N	SN54H20J, N	7
TG241F	SNG241U	SN54H20W	7
TG242E, J	SNG242J, N	SN74H20J, N	7
TG242F	SNG242U	SN74H20W	7
TG243E, J	SNG243J, N	SN74H20J, N	7
TG243F	SNG243U	SN74H20W	7
TG250E, J	SNG250J, N	SN54H53J, N	7
TG250F	SNG250U	SN54H53W	7
TG251E, J	SNG251J, N	SN54H53J, N	7
TG251F	SNG251U	SN54H53W	7
TG252E, J	SNG252J, N	SN74H53J, N	7
TG252F	SNG252U	SN74H53W	7
TG253E, J	SNG253J, N	SN74H53J, N	7
TG253F	SNG253U	SN74H53W	7
TG260E, J	SNG260J, N	SN54H30J, N	7
TG260F	SNG260U	SN54H30W	7
TG261E, J	SNG261J, N	SN54H30J, N	7
TG261F	SNG261U	SN54H30W	7
TG262E, J	SNG262J, N	SN74H30J, N	7
TG262F	SNG262U	SN74H30W	7
TG263E, J	SNG263J, N	SN74H30J, N	7
TG263F	SNG263U	SN74H30W	7
TG270E, J	SNG270J, N	SN54H60J, N	7
TG270F	SNG270U	SN54H60W	7
TG271E, J	SNG271J, N	SN54H60J, N	7
TG271F	SNG271W	SN54H60W	7
TG272E, J	SNG272J, N	SN74H60J, N	7
TG272F	SNG272U	SN74H60W	7
TG273E, J	SNG273J, N	SN74H60J, N	7
TG273F	SNG273U	SN74H60W	7
TG280E, J	SNG280J, N	SN54H52J, N	7
TG280F	SNG280U	SN54H52W	7
TG281E, J	SNG281J, N	SN54H52J, N	7
TG281F	SNG281U	SN54H52W	7
TG282E, J	SNG282J, N	SN74H52J, N	7
TG282F	SNG282U	SN74H52W	7
TG283E, J	SNG283J, N	SN74H52J, N	7
TG283F	SNG283U	SN74H52W	7
TG290E, J	SNG290J, N	SN54H62J, N	7
TG290F	SNG290U	SN54H62W	7
TG291E, J	SNG291J, N	SN54H62J, N	7
TG291F	SNG291U	SN54H62W	7
TG292E, J	SNG292J, N	SN74H62J, N	7
TG292F	SNG292U	SN74H62W	7
TG293E, J	SNG293J, N	SN74H62J, N	7
TG293F	SNG293U	SN74H62W	7
TG300E, J	SNG300J, N	SN54H53J, N	7
TG300F	SNG300U	SN54H53W	7
TG301E, J	SNG301J, N	SN54H53J, N	7
TG301F	SNG301U	SN54H53W	7
TG302E, J	SNG302J, N	SN74H53J, N	7
TG302F	SNG302U	SN74H53W	7
TG303E, J	SNG303J, N	SN74H53J, N	7
TG303F	SNG303U	SN74H53W	7
TG310E, J	SNG310J, N	SN54H50J, N	7
TG310F	SNG310U	SN54H50W	7
TG311E, J	SNG311J, N	SN54H50J, N	7
TG311F	SNG311U	SN54H50W	7
TG312E, J	SNG312J, N	SN74H50J, N	7
TG312F	SNG312U	SN74H50W	7
TG313E, J	SNG313J, N	SN74H50J, N	7
TG313F	SNG313U	SN74H50W	7
TG320E, J	SNG320J, N	SN54H10J, N	7
TG320F	SNG320U	SN54H10W	7
TG321E, J	SNG321J, N	SN54H10J, N	7
TG321F	SNG321U	SN54H10W	7
TG322E, J	SNG322J, N	SN74H10J, N	7
TG322F	SNG322U	SN74H10W	7
TG323E, J	SNG323J, N	SN74H10J, N	7
TG323F	SNG323U	SN74H10W	7
TG350E, J	SNG351J, N	SN54S140J, N	5
TG350F	SNG351U	SN54S140W	5
TG352E, J	SNG353J, N	SN74S140J, N	5
TG352F	SNG353U	SN74S140W	5

MOS/LSI CIRCUITS

AMI

Type Number	Direct Replacement	Recommended for New Designs	Sec.
RD55		TMS 3002 LR	14
RD57		TMS 3002 LR	14
RD58		TMS 3002 LR	14
RD60		TMS 3002 LR	14
RD62		TMS 3104 LC/NC	14
RD63	TMS 3304 LR	TMS 3304 LR	14
RD64		TMS 3114 JC/NC	14
RD65		TMS 3401 LC/NC	14
MA51	TMS 2300 JC/NC	TMS 2300 JC/NC	14
MB51		TMS 2600 JC/NC	14
MX52		TMS 6009 JC/NC	14
MX53		TMS 6000 JC/NC	14
MX54		TMS 6009 JC/NC	14

A.M.S.

Type Number	Direct Replacement	Recommended for New Designs	Sec.
AMD 91600111		TMS 4023 NC	14

CMI

Type Number	Direct Replacement	Recommended for New Designs	Sec.
CM1101	TMS 1101 JC	TMS 1101 JC/NC	14

Electronic Arrays

Type Number	Direct Replacement	Recommended for New Designs	Sec.
EA1003		TMS 3112 JC/NC	14
EA1007		TMS 3112 JC/NC	14
EA1004		TMS 3101 LC/NC	14
EA1005		TMS 3101 LC/NC	14
EA1200		TMS 3112 JC/NC	14
EA1201		TMS 3112 JC/NC	14
EA1204		TMS 3114 JC/NC	14
EA1205		TMS 3114 JC/NC	14
EA1206		TMS 3413 LC/NC	14
EA1208		TMS 3016 LR	14
EA1210		TMS 3412 JC/NC	14
EA1212		TMS 3412 JC/NC	14
EA1221		TMS 3101 JC/NC	14
EA1400		TMS 1101 JC/NC	14
EA1800		TMS 2200 JC/NC	14
EA1801		TMS 2200 JC/NC	14
EA1804		TMS 2200 JN/NC	14
EA1806		TMJ 2200 JC/NC	14
EA3001		TMS 2500 JC/NC	14
EA3101		TMS 2602 JC/NC	14
EA3300		TMS 4400 JC/NC	14
EA3307		TMS 2604 JC/NC	14
EA3500		TMS 2500 JC/NC	14

Electronic Arrays, Cont.

Type Number	Direct Replacement	Recommended for New Designs	Sec.
EA3501		TMS 2501 JC/NC	14
EA3700		TMS 4100 JC/NC	14
EA3701		TMS 4103 JC/NC	14
EA4000		TMS 4400 JC/NC	14

Fairchild

Type Number	Direct Replacement	Recommended for New Designs	Sec.
3250		TMS 2500 JC/NC	14
3251		TMS 4400 JC/NC	14
3254		TMS 2500 JC/NC	14
3255		TMS 4100 JC/NC	14
3256		TMS 4100 JC/NC	14
3257		TMS 4100 JC/NC	14
3258		TMS 2500 JC/NC	14
3300		TMS 3000 LR	14
3303		TMS 3000 LR	14
3304		TMS 3016 LR	14
3305		TMS 3016 LR	14
3306		TMS 3016 LR	14
3307		TMS 3101 LC/NC	14
3320		TMS 3103 LC/NC	14
3325		TMS 3417 JC/NC	14
3326	TMS 3304 LC	TMS 3304 LC/NC	14
3330		TMS 3403 LC	14
3331		TMS 3402 LC/NC	14
3332		TMS 3305 LC	14
3377		TMS 3401 LC	
3383		TMS 3412 JC/NC	14
3501		TMS 2800 JC/NC	14
3507		TMS 2600 JC/NC	14
3512		TMS 2500 JC/NC	14
3513		TMS 2500 JC/NC	14
3514		TMS 2500 JC/NC	14
3530		TMS 1101 JC/NC	14
3532		TMS 1101 JC/NC	14
3580	TMS 2600 JC	TMS 2600 JC/NC	14
3584	TMS 2600 JC	TMS 2600 JC/NC	14
3700		TMS 6005 JC/NC	14
3701		TMS 6005 JC/NC	14
3810		TMS 2700 JC/NC	14

GI

Type Number	Direct Replacement	Recommended for New Designs	Sec.
DL-5-0406	TMS 3406 LC	TMS 3101 LC/NC	14
DL-5-1200		TMS 3101 LC/NC	14
DL-7-1200		TMS 3101 LC/NC	14
DL-5-1512		TMS 3401 LC/NC	14
DL-7-1512		TMS 3401 LC/NC	14
SL-6-2050		TMS 3002 LR	
SL-6-2064		TMS 3103 LC/NC	14
DL-6-2100		TMS 3101 LC/NC	14
RO-1-2240		TMS 2500 JC/NC	14
MU-6-2281		TMS 6000 JC/NC	14
DL-0-3066	TMS 3304 LR	TMS 3304 LR	14

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MOS/LSI CIRCUITS

GI, Cont.

Type Number	Direct Replacement	Recommended for New Designs	Sec.
SL-7-4025		TMS 3000 LR	14
SL-7-4032		TMS 3112 JC/NC	14
SS-6-8211		TMS 3016 LR	14
SS-6-8211		TMS 3016 LR	14
MEM2009		TMS 6003 JC/NC	14
MEM2017		TMS 6009 JC/NC	14
MEM3016	TMS 3016 LR	TMS 3016 LR	14
MEM3021	TMS 3021 LR	TMS 3021 LR	14
MEM3032-D2		TMS 3112 JC/NC	14
MEM3032-D5		TMS 3112 JC/NC	14
MEM3025		TMS 3000 LR	
MEM3064		TMS 3103 LC/NC	14
MEM3064 LR	TMS 3027 JC	TMS 3027 JC	14
MEM3064-2B		TMS 3103 LC/NC	14
MEM3100		TMS 3002 LR	14
MEM3100A2		TMS 3002 LR	14
MEM3128		TMS 3114 JC/NC	14
MEM3128-2		TMS 3114 JC/NC	14
MEM5021		TMS 5700 JC/NC	14

Intel

Type Number	Direct Replacement	Recommended for New Designs	Sec.
1101	TMS 1101 JC	TMS 1101 JC/NC	14
11001	TMS 1101 JC	TMS 1101 JC/NC	14
1103	TMS 1103 NC	TMS 1103 JC/NC	14
1301		TMS 2600 JC/NC	14
1402	TMS 3412 JC/NC	TMS 3412 JC/NC	14
1403	TMS 3413 JC	TMS 3413 JC/NC	14
1404	TMS 3414 JC	TMS 3414 JC/NC	14
1405		TMS 3401 LC/NC	14
1406	TMS 3406 LC	TMS 3101 LC/NC	14
1407	TMS 3407 LC	TMS 3101 LC/NC	14
1506	TMS 3406 LM	TMS 3101 LC/NC	14
1507	TMS 3407 LM	TMS 3101 LC/NC	14

Mostek

Type Number	Direct Replacement	Recommended for New Designs	Sec.
MK1001L	TMS 3304 LR	TMS 3304 LR	14
MK1002P	TMS 3414 JC	TMS 3414 JC/NC	14
MK1003P		TMS 3412 LC/NC	14
MK2000P		TMS 4100 JC/NC	14
MK2001P		TMS 4103 JC/NC	14
MK2100P		TMS 2500 JC/NC	14
MK2101P		TMS 2501 JC/NC	14
MKB2300P		TMS 4100 JC/NC	14
TMS2302P		TMS 4103 JC/NC	14
TMS2400P	TMS 2300 JC/NC	TMS 2300 JC/NC	14
MK3100P		TMS 2500 JC/NC	14
MK3101P		TMS 2501 JC/NC	14
MK4001P	TMS 4003 JC	TMS 4003 JC/NC	14
MK4003P		TMS 4024 JC/NC	14

Motorola

Type Number	Direct Replacement	Recommended for New Designs	Sec.
MCM1110	TMS 2600 JC	TMS 2600 JC/NC	14
MCM1120	TMS 2400 JC	TMS 2500 JC/NC	14
MCM1121	TMS 2400 JC	TMS 2500 JC/NC	14
MCM1122	TMS 2403 JC	TMS 2501 JC/NC	14
MC1124L		TMS 3802 LC	14
MC1125L		TMS 3802 LC	14
MCM1130	TMS 4100 JC	TMS 4100 JC/NC	14
MCM1131	TMS 4100 JC	TMS 4100 JC/NC	14
MCM1132	TMS 4103 JC	TMS 4103 JC/NC	14
MC1141G	TMS 3305 LR	TMS 3305 LR	14
MC1142G		TMS 3401 LC/NC	14
MC1150L		TMS 6000 JC/NC	14
MCM1150	TMS 2300 JC	TMS 2300 JC/NC	14
MC1160G	TMS 3003 LR	TMS 3101 LC/NC	14
MC1161G	TMS 3002 LR	TMS 3002 LR	14
MCM1170		TMS 1101 JC/NC	14
MCM1173		TMS 4023 NC	
MC2244G		TMS 3401 LC/NC	14
MC2246		TMS 3417 JC/NC	14
MCM2340		TMS 4400 JC/NC	14
MC2360G		TMS 3101 LC/NC	14
MC2362G		TMS 3412 JC/NC	14
MC2363G		TMS 3114 JC/NC	14
MCM2372	TMS 1103 NC	TMS 1103 NC	14
MC2380G		TMS 3101 LC/NC	14
MC2381G		TMS 3101 LC/NC	14
MC2384L	TMS 3412 JC	TMS 3412 JC/NC	14
MC2385G	TMS 3413 JC	TMS 3414 LC/NC	14
MC2386G	TMS 3414 JC	TMS 3414 LC/NC	14

National

Type Number	Direct Replacement	Recommended for New Designs	Sec.
MM400/500		TMS 3000 LR	14
MM403/503		TMS 3002 LR	14
MM404/504		TMS 3016 LR	14
MM405/505		TMS 3112 JC/NC	14
MM406/506	TMS 3406 LC	TMS 3101 LC/NC	14
MM410/510		TMS 3103 LC/NC	14
MM421/521	TMS 2800 JC	TMS 2800 JC/NC	14
MM422/522		TMS 2600 JC/NC	14
MM422/522AP		TMS 2605 JC/NC	14
MM422BL/522BL		TMS 2607 JC/NC	14
MM422BN/522BN		TMS 2608 JC/NC	14
MM422DE/522DE		TMS 2605 JC/NC	14
MM422EK/522EK		TMS 2606 JC/NC	14
MM423/523	TMS 2600 JC	TMS 2600 JC/NC	14
MM423BO/523BO	TMS 2609 JC	TMS 2609 JC/NC	14
MM423FE/523FE	TMS 2610 JC	TMS 2610 JC/NC	14
MM4001/5001		TMS 3102 LC/NC	14
MM4006/5006		TMS 3101 LC/NC	14
MM400GD/500GD		TMS 3101 LC/NC	14
MM4010/5010		TMS 3103 LC/NC	14
MM4015A/5015A		TMS 3314 JC/NC	14
MM4016/5016		TMS 3401 LC/NC	14
MM4016D/5016D		TMS 3401 LC/NC	14
MM4018/5018		TMS 3103 LC/NC	14
MM4040/5040		TMS 3016 LR	14

MOS/LSI CIRCUITS

National, Cont.

Type Number	Direct Replacement	Recommended for New Designs	Sec.
MM4050/5050		TMS 3112 JC/NC	14
MM4051/5051		TMS 3112 JC/NC	14
MM4051D/5051D		TMS 3112 JC/NC	14
MM4052/5052		TMS 3102 LC/NC	14
MM4053/5053		TMS 3101 LC/NC	14
MM5105		TMS 3403 LC/NC	14
MM4210/5210		TMS 2800 JC/NC	14
MM4211/5211		TMS 2600 JC/NC	14
MM4230/5230		TMS 2500 JC/NC	14
MM4231/5231		TMS 2500 JC/NC	14
MM4232/5232		TMS 4400 JC/NC	14
MM4240/5240		TMS 2500 JC/NC	14
MM4241/5241		TMS 2700 JC/NC	14
MM4250/5250	TMS 1101 JC	TMS 1101 JC/NC	14

Signetics

Type Number	Direct Replacement	Recommended for New Designs	Sec.
2001	TMS 3016 LR	TMS 3016 LR	14
2002	TMS 3000 LR	TMS 3000 LR	14
2003	TMS 3000 LR	TMS 3112 JC/NC	14
2004	TMS 3002 LR	TMS 3002 LR	14
2005	TMS 3003 LR	TMS 3101 LC/NC	14
2501	TMS 1101 JC	TMS 1101 JC/NC	14
2502	TMS 3412 JC	TMS 3412 JC/NC	14
2503	TMS 3413 LC	TMS 3413 LC/NC	14
2504	TMS 3414 LC	TMS 3414 LC/NC	14
2505		TMS 3401 LC/NC	14
2506		TMS 3101 LC/NC	14
2507		TMS 3101 LC/NC	14
2508		TMS 1103 NC	14
2509		TMS 3002 LR	14
2510		TMS 3101 LC/NC	14
2511		TMS 3101 LC/NC	14
2512		TMS 3414 LC/NC	14
2513		TMS 2500 JC/NC	14
2514		TMS 2500 JC/NC	14

Solitron

Type Number	Direct Replacement	Recommended for New Designs	Sec.
UC6525/7525		TMS 2600 JC/NC	14
UC6548/7548		TMS 2600 JC/NC	14
UC6550/7550	TMS 4026 JC	TMS 4026 JC/NC	14
UC6572/7572	TMS 2700 JC	TMS 2700 JC/NC	14
UC6596/7596		TMS 4400 JC/NC	14
UC65965/7596		TMS 4400 JC/NC	14
UC6577/7577		TMS 2500 JC/NC	14
UC7310		TMS 3413 JC/NC	14
UC7315		TMS 3112 JC/NC	14
UC7316		TMS 3016 LR	14
UC7320		TMS 3002 LR	14
UC7350		TMS 3417 JC/NC	14

Unisem

Type Number	Direct Replacement	Recommended for New Designs	Sec.
UA2524/3524		TMS 1103 NC	14
UA2525/3525		TMS 2600 JC/NC	14
UA2548/3548		TMS 2600 JC/NC	14
UA2552/3552		TMS 3113 LC/NC	14
UA2556/3556	TMS 1101 JC	TMS 1101 JC/NC	14
UA2564/3564		TMS 4026 JC/NC	14
UA2572/3572	TMS 2700 JC/NC	TMS 2700 JC/NC	14
UA2596/3596		TMS 4400 JC/NC	14
UA2664/3664	TMS 4026 JC	TMS 4026 JC/NC	14
UA3540		TMS 2500 JC/NC	14

TEXAS INSTRUMENTS
INCORPORATED
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Discrete Semiconductors and Components

c

DISCRETE SEMICONDUCTORS AND COMPONENTS MANUFACTURED BY TEXAS INSTRUMENTS

In addition to its leadership position in integrated circuits, Texas Instruments is the world's largest supplier of discrete semiconductors and components.

Devices shown below represent TI's standard discrete semiconductors beginning with the 1N series, followed by 2N, in-house, and the resistor product lines. Note that consecutive type numbers are shown in condensed form: e.g. 1N253, 1N254, 1N255, and 1N256 devices are listed as 1N253—1N256.

1N251
1N253—1N256
1N332—1N349
1N440B—1N445B
1N456—1N459
1N456A—1N459A
1N461—1N464
1N461A—1N464A
1N482—1N485
1N482A—1N485A
1N482B—1N485B
1N530—1N540
1N547
1N550—1N555
1N599—1N606
1N599A—1N606A
1N607—1N614
1N607A—1N614A
1N607R—1N614R
1N607AR—1N614AR
1N625—1N629
1N643
1N645
1N645A
1N646—1N649
1N568—1N663
1N702—1N716
1N702A—1N716A
1N746—1N759
1N746A—1N759A
1N761—1N766
1N914—1N916
1N914A—1N916A
1N914B—1N916B
1N917
1N957—1N961
1N957A—1N961A
1N957B—1N961B
1N1095—1N1096
1N1100—1N1105
1N1115—1N1120
1N1124A—1N1128A
1N1124AR—1N1128AR
1N1487—1N1492
1N1581—1N1587
1N1612—1N1616
1N1692—1N1697
1N1816—1N1836
1N1816A—1N1836A
1N1816C—1N1836C
1N1816CA—1N1836CA
1N2069—1N2071
1N2069A—1N2071A
1N2175
1N2970—1N3011
1N2970A—1N3011A
1N2970B—1N3011B
1N3064
1N3070
1N3506—1N3517
1N3518—1N3520
1N4001—1N4007
1N4099
1N4100—1N4106
1N4148—1N4154
1N4305
1N4360
1N4370—1N4372
1N4370A—1N4372A
1N4444
1N4446—1N4449
1N4454
1N4531—1N4534
1N4536
1N4606
1N4727
1N4938
2N117—2N120
2N122
2N243—2N244
2N250—2N251
2N250A—2N251A
2N263—2N264
2N315A
2N317A
2N332—2N336
2N332A—2N336A
2N337—2N341
2N342
2N342A
2N343
2N377
2N388—2N389
2N388A—2N389A
2N395—2N397
2N398
2N398A
2N398B
2N404
2N404A
2N424
2N424A
2N426—2N428
2N438
2N438A
2N439—2N440
2N456A—2N458A
2N456B—2N458B
2N470—2N480
2N489—2N493
2N489A—2N493A
2N489B—2N493B
2N494
2N494A
2N494B
2N494C
2N497—2N498
2N497A—2N498A
2N508
2N511—2N512
2N511A—2N512A
2N511B—2N512B
2N520
2N520A
2N522A
2N541—2N543
2N581—2N582
2N587
2N594—2N596
2N634A—2N636A
2N656—2N657
2N656A—2N657A
2N658—2N662
2N696—2N699
2N705
2N706
2N706A
2N706B
2N708—2N710
2N711
2N711A
2N711B
2N717
2N718—2N720
2N718A—2N720A
2N721—2N722
2N730—2N731
2N743—2N744
2N797
2N849—2N852
2N870—2N871
2N910—2N912
2N914
2N917—2N918
2N929—2N930
2N929A—2N930A
2N956
2N960—2N975
2N985
2N997
2N1021—2N1022
2N1021A-2N1022A
2N1038—2N1045
2N1046—2N1050
2N1046A—2N1050A
2N1046B—2N1050B
2N1131—2N1132
2N1141—2N1143
2N1141A—2N1143A
2N1149—2N1156
2N1195
2N1273—2N1274
2N1276—2N1279
2N1302—2N1309
2N1370—2N1383
2N1404
2N1420
2N1507
2N1529—2N1548
2N1586—2N1599
2N1605
2N1613
2N1671
2N1671A
2N1671B
2N1690—2N1691
2N1711
2N1714—2N1721
2N1722
2N1722A
2N1723
2N1724
2N1724A
2N1725
2N1889—2N1893
2N1907—2N1908
2N1936—2N1937
2N1973—2N1975
2N1993—2N2001
2N2060
2N2102
2N2102A
2N2150—2N2151
2N2160
2N2188—2N2191
2N2192—2N2194
2N2192A—2N2194A
2N2217
2N2218—2N2219
2N2218A—2N2219A
2N2220
2N2221—2N2223
2N2221A—2N2223A
2N2243
2N2243A
2N2270
2N2303
2N2322—2N2326
2N2369
2N2369A
2N2386
2N2386A
2N2387—2N2390
2N2393—2N2396
2N2411—2N2412
2N2415—2N2416
2N2432
2N2432A
2N2453
2N2481
2N2483—2N2484
2N2497—2N2500
2N2537—2N2540
2N2552—2N2567
2N2586
2N2604—2N2605
2N2608—2N2609
2N2635
2N2639—2N2644
2N2646—2N2647
2N2659—2N2670
2N2802—2N2807
2N2861—2N2862
2N2880
2N2894
2N2904—2N2907
2N2904A—2N2907A
2N2913—2N2914
2N2915—2N2916
2N2915A—2N2916A
2N2917—2N2918
2N2919—2N2920
2N2919A—2N2920A
2N2944—2N2946
2N2944A—2N2946A
2N2972—2N2979
2N2987—2N2994
2N2996—2N3008
2N3010—2N3015
2N3036—2N3040
2N3043—2N3053
2N3114
2N3117
2N3146—2N3147
2N3244—2N3245
2N3250—2N3251
2N3250A—2N3251A
2N3252—2N3253
2N3328—2N3336
2N3347—2N3352
2N3371
2N3375
2N3418—2N3421
2N3444
2N3458—2N3460
2N3467—2N3468
2N3485—2N3486
2N3485A—2N3486A
2N3494—2N3497
2N3502—2N3505
2N3551—2N3562
2N3570—2N3576
2N3632
2N3680
2N3702—2N3716
2N3724—2N3725
2N3724A—2N3725A
2N3733
2N3789—2N3792
2N3798—2N3799
2N3806—2N3811
2N3819—2N3824
2N3829
2N3833—2N3835
2N3838
2N3846—2N3847
2N3866
2N3903—2N3906
2N3909
2N3909A
2N3962—2N3966
2N3970—2N3972
2N3980
2N3993—2N3994
2N3993A—2N3994A
2N3996—2N4005
2N4040—2N4041
2N4058—2N4062
2N4091—2N4093
2N4104
2N4138
2N4220—2N4222
2N4220A—2N4222A
2N4223—2N4224
2N4252—2N4253
2N4300—2N4301
2N4391—2N4393
2N4398—2N4399
2N4416
2N4416A
2N4418—2N4423
2N4851—2N4855
2N4856—2N4861
2N4856A—2N4861A
2N4874—2N4876
2N4891—2N4894
2N4901—2N4906
2N4913—2N4915
2N4947—2N4949
2N4994—2N4997
2N5043—2N5047
2N5058—2N5059
2N5245—2N5248
2N5273—2N5275
2N5301—2N5303
2N5332—2N5333

DISCRETE SEMICONDUTORS AND COMPONENTS MANUFACTURED BY TEXAS INSTRUMENTS (Contd)

2N5384—2N5390
2N5399
2N5447—2N5451
2N5543—2N5549
2N5938—2N5940
2N5949—2N5953
3N34—3N35
3N74—3N79
3N108—3N111
3N160—3N161
3N174
3N201—3N203
600C—601C
604C
606C
608C
610C
612C
614C
616C
618C
620C
622C
624C
650—653
650C0—650C7
651
651C0—651C9
652
652C0—652C9
653
653C0—653C9
654C9
655C9
A3T918
A3T929
A3T930
A3T2221—A3T2222
A3T2221A—A3T2222A
A3T2484
A3T2894
A3T2906—A3T2907
A3T2906A—A3T2907A
A3T3011
A4T918
A4T930
A4T1893
A4T2219A
A4T2243
A4T2369
A4T2432
A4T2484
A4T2605
A4T2894
A4T2907A
A4T2945
A4T3013
A4T3015

A4T3251A
A4T3570
A4T3702—A4T3716
A4T3725
A4T3822—A4T3823
A4T3829
A4T3890
A4T3993
A4T4058—A4T4062
A4T4416
A4T4496—A4T4497
A4T4857
A5T2222
A5T2907
A5T3644—A5T3645
A5T3903—A5T3906
A5T5058—A5T5059
A516—A517
A600—A602
A610—A612
A706—A713
A900—A903
A905—A908
G129—G130
H11
H35
H38
H60—H62
LSX400
LSX600
LSX900
TI51—TI60
TI71—TI75
SERIES TI145
TI156
TI156L
TI159—TI162
TI363—TI365
TI390—TI391
TI395
TI397—TI403
TI480—TI484
TI486—TI487
TI492—TI496
TI550—TI551
TI1121—TI1126
TI1131—TI1136
TI1141—TI1146
TI1151—TI1156
TI3027—TI3031
TIC35—TIC36
TIC44—TIC47
SERIES TIC250
SERIES TIC252
SERIES TIC260
SERIES TIC262
SERIES TIC270
SERIES TIC272

TID17—TID20
TID21A—TID26A
TID29A—TID30A
TID31—TID45
TID121—TID126
TID129—TID134
TIL23—TIL24
TIL58
TIL63—TIL67
TIL102—TIL103
TIL107—TIL108
TIL201—TIL208
TIL601—TIL616
TIP29—TIP36
TIP29A—TIP36A
TIP29B—TIP36B
TIP29C—TIP36C
TIP41—TIP42
TIP41A—TIP42A
TIP41B—TIP42B
TIP41C—TIP42C
TIP3055
TIS05
TIS14
TIS25—TIS27
TIS37—TIS39
TIS43
TIS56—TIS59
TIS62—TIS64
TIS68—TIS70
TIS73—TIS75
TIS78—TIS79
TIS84
TIS86—TIS87
TIS90—TIS93
TIS90M—TIS93M
TIS97—TIS101
TIS104—TIS119
TIV306—TIV308
TIXL05—TIXL06
TIXL12—TIXL22
TIXL26—TIXL30
TIXL51—TIXL53
TIXL55—TIXL57
TIXL59
TIXL68—TIXL76
TIXL104—TIXL106
TIXL109
TIXL151—TIXL152
TIXL301—TIXL302
TIXM101
TIXS33
TIXS35—TIXS36
TIXS80—TIXS81
TIXV01—TIXV04
XD500-XD502

RESISTORS AND SENSISTOR® RESISTORS

CD1/2MR—RN20X
CD1/2MR—RN20X
CD1/2MR—RN20X
CG1/8—RN55G
CG1/8—RN550—G
CG1/8—RN550—G
CG1/4—RN60D—G
CG1/4—RN60D—G
CG1/2—RN65D—G
CG1/2—RN65D—G
CG1/2—RN65D—G
MC50C—RN50C
MC50D
MC50E
MC55C—RN55C
MC55D—RN55D
MC55D—RC07
MC55E—RN55E
MC58C
MC58D
MC58E
MC60C—RN60C
MC60D—RN60D
MC60E—RN60E
MC61C
MC61D
MC61D—RL20
MC61E
MC65C—RN65C
MC65D—RN65D
MC65E—RN65E
MC65F—RN65F
MC66C
MC66D
MC66D—RL32
MC66E
MM60C—RN60C
MM60D
MM60E
MM65C—RN65C
MM65D
MM65E—RN65E
MM70C—RN70C
MM70D
MM70E—RN70E
P100 10 PCT
P100 5 PCT
TG1/8 10 PCT
TG1/8 5 PCT
TM1/8 10 PCT
TM1/8 5 PCT
TM1/4 10 PCT
TM1/4 5 PCT

LISTING OF PREFERRED SEMICONDUCTORS AND COMPONENTS BY DEVICE CLASSIFICATION

SILICON LOW-POWER N-P-N

TIS62	1025*
TIS63	1025
TIS84	1033
TIS86	1041
TIS87	1041
TIS97	1053
TIS98	1053
TIS99	1053
TIS100	1061
TIS101	1061
TIS108	1033
2N697	1201
2N930	1263
2N1613	1201
2N2219	1305
A3T2221	1313
A3T2221A	1317
2N2222	1305
A3T2222	1313
A3T2222A	1317
2N2243A	1301
2N2369A	1327
2N2432	1337
2N2484	1349
A3T2484	1269
A3T3011	1405
2N3013	1409
2N3015	1413
2N3704	1433
2N3705	1433
2N3706	1433
2N3707	1435
2N3708	1435
2N3709	1435
2N3710	1435
2N3711	1435
2N3725	1437
2N4252	1445
2N4994	1503
2N4995	1503
2N4996	1511
2N4997	1511
2N5449	1701
2N5450	1701
2N5451	1701

SILICON LOW-POWER P-N-P

TIS37	2001
TIS38	2001
2N2605	2119
2N2894	2125
A3T2894	2127
2N2905	2131
A3T2906	2135
A3T2906A	2135
2N2907	2131
A3T2907	2135
A3T2907A	2135
2N2945	2139
2N3250	2209*
2N3702	2225
2N3703	2225
2N3829	2235
2N4058	2301
2N4059	2301
2N4060	2301
2N4061	2301
2N4062	2301
2N5447	2305
2N5448	2305

SILICON UHF TRANSISTORS

2N918	3201
A3T918	3203
2N3570	3401
2N3866	3501
2N4875	3701

SILICON MULTIPLE AND MULTI-ELEMENT TRANSISTORS

3N79	4101
TIS92	4015
TIS92M	4105
TIS93	4105
TIS93M	4105
3N111	4109
2N997	4301
2N2060	4401
2N2223	4401
2N2639	4405
2N2642	4405
2N2643	4405
2N2920	4409
2N2977	4409
2N2979	4409
2N3350	4507
2N3680	4509
2N3838	4517
2N4854	4701

SILICON FIELD-EFFECT TRANSISTORS

TIS58	6091
TIS59	6091
TIS73	6103
TIS74	6103
TIS75	6103
3N160	6201
2N2386	6301
2N2498	6303
2N3330	6305
2N3819	6401
2N3820	6403
2N3822	6405
2N3823	6407
2N3909	6413
2N3993A	6501
2N4416	6503
2N4857	6511
2N5045	6601
2N5245	6703*
2N5246	6703
2N5247	6703
2N5248	6711

SILICON UNIJUNCTION

2N491A	7101
2N492A	7101
2N1671B	7109
2N3980	7201

GERMANIUM LOW-POWER ALLOY-JUNCTION TRANSISTORS

2N398	9101
2N404	9105
2N1302	9205
2N1303	9205
2N1304	9205
2N1305	9205
2N1306	9205
2N1307	9205
2N1308	9205
2N1309	9205
2N1377	9213
2N1997	9301
2N2000	9307

GERMANIUM MESA AND PLANAR SWITCHING TRANSISTORS

2N797	12101
2N964	12105
2N2635	12301

GERMANIUM UHF/MICROWAVE TRANSISTORS

2N5043	14401

SILICON POWER TRANSISTORS

TIP29A,B,C	16101
TIP30A,B,C	16105
TIP31A,B,C	16109
TIP32A,B,C	16113
TIP33A,B,C	16117
TIP34A,B,C	16121
TIP35A,B,C	16125
TIP36A,B,C	16129
2N1724	16301
TIP3055	
2N2987	16401*
2N2988	16401
2N2989	16401
2N2990	16401
2N2991	16401
2N2992	16401
2N2993	16401
2N2994	16401
2N3418	16501
2N3419	16501
2N3420	16501
2N3421	16501
2N3551	16507
2N3552	16507
2N3713	16511
2N3714	16511
2N3715	16511
2N3716	16511
2N3789	16557
2N3790	16557
2N3791	16557
2N3792	16557
2N3846	16579
2N3847	16579
2N3996	16601
2N3997	16601
2N3998	16601
2N3999	16601
2N4000	16607
2N4001	16607
2N4002	16613
2N4003	16613
2N4300	16625
2N4301	16631
2N4398	16645
2N4399	16645
2N5301	16687
2N5302	16687
2N5303	16687
2N5333	16701
2N5384	16707
2N5385	16707
2N5386	16711
2N5387	16715
2N5388	16715

GERMANIUM POWER TRANSISTORS

2N456A	17101
2N1038	17201
2N1539	17223
2N1907	17231
TI3027	17301

GENERAL PURPOSE DIODES

1N456	18101
1N457	18101
1N458	18101
1N459	18101
1N482	18109

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C

GENERAL PURPOSE DIODES (Cont'd.)

1N483	18109*
1N484	18109
1N485	18109
1N645	18113
1N646	18113
1N647	18113
1N648	18113
1N649	18113

SWITCHING DIODES

1N251	19101
1N661	19151
1N914	19201
1N914B	19201
1N3070	19303
1N4148	19401
1N4154	19403
1N4448	19401
1N4454	19405

MULTIPLE DIODES

TID21	20005
TID22	20005
TID23	20005
TID24	20005
TID25	20009
TID26	20009
TID29	20013
TID30	20013

TUNING DIODES

TIV306	21205
TIV307	21205
TIV308	21205

REGULATOR DIODES

1N746	23109
1N746A	23109
1N747	23109
1N747A	23109
1N748	23109
1N748A	23109
1N749	23109
1N749A	23109
1N750	23109
1N750A	23109
1N751	23109
1N751A	23109
1N752	23109
1N752A	23109
1N753	23109
1N753A	23109
1N754	23109
1N754A	23109
1N755	23109
1N755A	23109
1N756	23109
1N756A	23109*
1N757	23109
1N757A	23109
1N758	23109
1N758A	23109
1N759	23109
1N759A	23109
1N4370	23601
1N4370A	23601
1N4371	23601
1N4371A	23601
1N4372	23601
1N4372A	23601

THYRISTORS AND TRIGGER DIODES

TI42A	24105
TI43A	24105
TIC44	24109
TIC45	24109
TIC46	24109
TIC47	24109
2N3001	24401
2N3002	24401
2N3003	24401
2N3004	24401
2N3005	24407
2N3006	24407
2N3007	24407
2N3008	24407
2N3555	24417
2N3556	24417
2N3557	24417
2N3558	24417
2N3559	24425
2N3560	24425
2N3561	24425
2N3562	24425

SILICON RECTIFIERS

1N4001	25401
1N4002	25401
1N4003	25401
1N4004	25401
1N4005	25401
1N4006	25401
1N4007	25401

OPTOELECTRONIC DEVICES

TIL01	27001
TIL09	27009
LS400	27401
LS600	27501
TIL601	27503
TIL602	27503
TIL603	27503
TIL604	27503
TIL605	27503
TIL606	27503*
TIL607	27503
TIL608	27503
1N2175	27801

PRECISION FILM RESISTORS

CG1/8	28201
CG1/4	28201
CG1/2	28201
MC50	28401
MC55	28401
MC60	28401
MC65	28401

TEMPERATURE-SENSING SILICON RESISTORS

TG1/8	29001
TM1/8	29001
TM1/4	29001

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APPLICATIONS GUIDE TO PREFERRED SEMICONDUCTORS AND COMPONENTS

APPLICATION	DEVICE RECOMMENDATION							
	BIPOLAR				FET			
	N-P-N		P-N-P		N-CHANNEL		P-CHANNEL	
	Type No.	Page No.*	Type No.	Page No.*	Type No.	Page No.*	Type No.	Page No.*
Small-Signal Transistor:	•A3T2484	1269	•A3T2906	2135	TIS58	6091	2N2386	6301
Amplifier:	•TIS92	4105	•A3T2907	2135	TIS59	6091	•2N2498	6303
	•TIS92M	4105	•A3T2906A	2135	•2N3819	6401	•2N3330	6305
DC to 1 MHz	•TIS97	1053	•A3T2907A	2135	•2N3822	6405	•2N3820	6403
	•TIS98	1053	•TIS93	4105			2N3909	6413
	TIS99	1053	•TIS93M	4105				
	2N697	1201	2N404	9105				
	2N930	1263	2N1303	9205				
	•2N997	4301	2N1305	9205				
	•2N1302	9205	2N1307	9205				
	•2N1304	9205	2N1309	9205				
	•2N1306	9205	2N2000	9307				
	•2N1308	9205	2N2605	2119				
	•2N2484	1349	•2N2905	2131				
	2N3704	1433	•2N2907	2131				
	2N3705	1433	2N3702	2225				
	2N3706	1433	2N3703	2225				
	2N3707	1435	•2N4058-62	2301				
	2N3708	1435	•2N5447	2305				
	2N3709	1435	2N5448	2305				
	2N3710	1435						
	2N3711	1435						
	•2N5449	1701						
	•2N5450	1701						
	•2N5451	1701						
1 MHz to 10 MHz	•A3T2484	1269	•TIS37	2001	TIS58	6091	2N2386	6301
	2N697	1201	2N404	9105	TIS59	6091	•2N2498	6303
	2N930	1263	2N1303	9205	•2N3819	6401	•2N3330	6305
	2N1302	9205	2N1305	9205	•2N3822	6405	•2N3820	6403
	2N1304	9205	2N1307	9205	•2N3823	6407	2N3909	6413
	2N1306	9205	2N1309	9205	•2N4416	6503		
	2N1308	9205	2N1377	9213	•2N5245	6703		
	2N1613	1201	2N1997	9301	•2N5246	6703		
	•2N2484	1349	2N2605	2119	•2N5247	6703		
	2N3704	1433	•2N2905	2131	•2N5248	6711		
	2N3705	1433	2N3702	2225				
	2N3706	1433	2N3703	2225				
	2N4994	1503	2N5447	2305				
	•2N4995	1503	2N5448	2305				
	•2N4996	1511						
	•2N4997	1511						
	2N5449	1701						
	2N5450	1701						
	2N5451	1701						
10 MHz to 50 MHz	TIS63	1025	•TIS37	2001	TIS58	6091	•2N2498	6303
	•TIS84	1033	•2N5043	14401	TIS59	6091	•2N3330	6305
	•TIS86	1041			•2N3819	6401		
	•TIS87	1041			•2N3822	6405		
	•TIS108	1033			•2N3823	6407		
	2N918	3201			•2N4416	6503		
	•2N2219	1305			•2N5245	6703		
	•2N2222	1305			•2N5246	6703		
	•2N2243A	1301			•2N5247	6703		
	2N4252	1445			•2N5248	6711		
	•2N4996	1511						
	•2N4997	1511						
50 MHz to 100 MHz	•TIS63	1025	•2N2905	2131	•2N3823	6407	•2N2498	6303
	•TIS86	1041	•2N2907	2131	•2N4416	6503	•2N3330	6305
	•TIS87	1041	•2N5043	14401	•2N5245	6703		
	•TIS108	1033			•2N5246	6703		
	2N918	3201			•2N5247	6703		
	•2N2219	1305						
	•2N2222	1305						
	2N4252	1445						
	•2N4875	3701						
	•2N4996	1511						
	•2N4997	1511						

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APPLICATIONS GUIDE TO PREFERRED SEMICONDUCTORS AND COMPONENTS (Cont'd.)

APPLICATION	DEVICE RECOMMENDATION							
	BIPOLAR				FET			
	N-P-N		P-N-P		N-CHANNEL		P-CHANNEL	
	Type No.	Page No.*	Type No.	Page No.*	Type No.	Page No.*	Type No.	Page No.*
100 MHz to 5 GHz	•TIS84	1033	•2N5043	14401	•2N3823	6407		
	2N918	3201			•2N4416	6503		
	•2N3570	3401			•2N5245	6703		
	2N4252	1445			•2N5246	6703		
	•2N4875	3701			•2N5247	6703		
Low-Noise Amplifier:	•A3T2484	1269	•TIS37	2001	•2N3822	6405	•2N2498	6303
	•TIS97	1053	2N2605	2119	•2N4416	6503	•2N3330	6305
0 to 10 MHz	2N930	1263	•2N4058-62	2301	•2N5248	6711		
	•2N2484	1349						
	2N3707	1435						
10 MHz to 50 MHz	•A3T918	3203	•TIS37	2001	•2N3822	6405		
	•TIS62	1025			•2N3823	6407		
	•TIS86	1041			•2N4416	6503		
	2N918	3201			•2N5245	6703		
	•2N4252	1445			•2N5246	6703		
	•2N4875	3701			•2N5247	6703		
	•2N4997	1511			•2N5248	6711		
50 MHz to 100 MHz	•A3T918	3203	•2N5043	14401	•2N3823	6407		
	•TIS62	1025			•2N4416	6503		
	•TIS86	1041			•2N5245	6703		
	2N918	3201			•2N5246	6703		
	•2N3570	3401			•2N5247	6703		
	2N4252	1445			•2N5248	6711		
	•2N4875	3701						
	•2N4997	1511						
100 MHz to 1 GHz	•A3T918	3203	•2N5043	14401	•2N3823	6407		
	•TIS86	1041			•2N4416	6503		
	2N918	3201			•2N5245	6703		
	•2N3570	3401			•2N5246	6703		
	•2N4875	3701			•2N5247	6703		
Mixer and Converter:	2N918	3201	•TIS37	2001	TIS58	6091	•2N2498	6303
0 to 10 MHz	•2N4995	1503			TIS59	6091	•2N3330	6305
					•2N3823	6407		
					•2N4416	6503		
10 MHz to 50 MHz	•TIS63	1025	•TIS37	2001	TIS58	6091	•2N3820	6403
	•TIS86	1041			TIS59	6091		
	2N4252	1445			•2N3823	6407		
	•2N4875	3701			•2N4416	6503		
	•2N4994	1503			•2N5245	6703		
	•2N4995	1503			•2N5246	6703		
					•2N5247	6703		
					•2N5248	6711		
50 MHz to 100 MHz	•TIS63	1025	•2N5043	14401	•2N3823	6407		
	•TIS86	1041			•2N4416	6503		
	•2N3570	3401			•2N5245	6703		
	2N4252	1445			•2N5246	6703		
	•2N4875	3701			•2N5247	6703		
	•2N4997	1511			•2N5248	6711		
100 MHz to 5 GHz	•A3T918	3203	•2N5043	14401	•2N3823	6407		
	•TIS86	1041			•2N4416	6503		
	2N918	3201			•2N5246	6703		
	•2N3570	3401			•2N5247	6703		
	2N4252	1445			•2N5248	6711		
	•2N4875	3701						
	•2N4997	1511						
Oscillator:	•TIS98	1053	•TIS38	2001	•2N3819	6401	•2N2498	6303
0 to 10 MHz	2N697	1201	•2N2905	2131	•2N3822	6405	•2N3330	6305
	2N1613	1201	2N3702	2225	•2N3823	6407		
	•2N2484	1349	•2N5447	2305	•2N4416	6503		
	2N3704	1433			•2N5248	6711		
	2N3711	1435						
	•2N5449	1701						

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APPLICATION	DEVICE RECOMMENDATION							
	BIPOLAR				FET			
	N-P-N		P-N-P		N-CHANNEL		P-CHANNEL	
	Type No.	Page No.*	Type No.	Page No.*	Type No.	Page No.*		
10 MHz to 50 MHz	•A3T918	3203	•TIS38	2001	•2N3822	6405		
	•TIS63	1025	•2N2905	2131	•2N3823	6407		
	•TIS98	1053	•2N2907	2131	•2N4416	6503		
	2N918	3201	•2N5447	2305	•2N5245	6703		
	•2N2219	1305			•2N5246	6703		
	•2N2222	1305			•2N5247	6703		
	2N3704	1433			•2N5248	6711		
	•2N4875	3701						
	•2N4994	1503						
	•2N5449	1701						
50 MHz to 100 MHz	•A3T918	3203	2N3702	2225	•2N3823	6407		
	•TIS63	1025	•2N5043	14401	•2N4416	6503		
	•TIS86	1041	•2N5447	2305	•2N5245	6703		
	2N918	3201			•2N5246	6703		
	2N3704	1433			•2N5247	6703		
	•2N4875	3701			•2N5248	6711		
	•2N5449	1701						
100 MHz to 5 GHz	•A3T918	3203	•2N5043	14401	•2N3823	6407		
	•TIS63	1025			•2N4416	6503		
	•TIS86	1041			•2N5245	6703		
	2N918	3201			•2N5246	6703		
	•2N3570	3401			•2N5247	6703		
	•2N4875	3701						
	•2N4997	1511						
Power Oscillator:	•2N3866	3501						
Power Amplifier:	•2N3866	3501						
Radio Frequency	•2N4875	3701						
Audio Frequency	•TIP29	16101	•TIP30	16105	•2N4857	6511		
	•TIP29A,B,C	16101	•TIP30A,B,C	16105				
	•TIP31	16109	•TIP32	16113				
	•TIP31A,B,C	16109	•TIP32A,B,C	16113				
	•TIP33	16117	•TIP34	16121				
	•TIP33A,B,C	16117	•TIP34A,B,C	16121				
	•TIP35	16125	•TIP36	16129				
	•TIP35A,B,C	16125	•TIP36A,B,C	16129				
	2N697	1201	2N456A	17101				
	2N1613	1201	2N1038	17201				
	•2N5301	16687	•2N2905	2131				
	•2N5302	16687	•2N2907	2131				
	•2N5303	16687	TI3027	17301				
			•2N3789	16557				
			•2N3790	16557				
			•2N3791	16557				
			•2N3792	16557				
			•2N3846	16579				
			•2N4398	16645				

	BIPOLAR				OTHER DEVICES		
	N-P-N		P-N-P				
	Type No.	Page No.*	Type No.	Page No.*	Type No.	Page No.*	Classification
Switching:	•A3T2221	1313	•A3T2894	2127	•2N3980	7201	UJT
Multivibrator,	•A3T2221A	1317	•A3T2906	2135	•2N4416	6503	N-FET
Pulse Generator,	•A3T2222	1313	•A3T2906A	2135	•2N4857	6511	N-FET
Schmitt Trigger	•A3T2222A	1317	•A3T2907	2135			
	•A3T3011	1405	•A3T2907A	2135			
	2N1302	9205	2N404	9105			
	2N1304	9205	2N1303	9205			
	2N1306	9205	2N1305	9205			
	2N1308	9205	2N1307	9205			
	•2N2219	1305	2N1309	9205			
	•2N2222	1305	2N1997	9301			
	•2N2369A	1327	2N2000	9307			

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APPLICATIONS GUIDE TO PREFERRED SEMICONDUCTORS AND COMPONENTS (Cont'd.)

APPLICATION	DEVICE RECOMMENDATION					
	BIPOLAR				OTHER DEVICES	
	N-P-N		P-N-P			
	Type No.	Page No.*	Type No.	Page No.*	Type No. Page No.	Classification
	•2N3013	1409	2N2635	12301		
	•2N3725	1437	•2N2894	2125		
			•2N2905	2131		
			•2N2907	2131		
			•2N3829	2235		
Ring Counter/ Latching Amplifier	2N930	1263	•2N2894	2125	•2N3001-4 24401	SCR
	•2N2369A	1327	•2N2905	2131	•2N3555-8 24417	SCR
	•2N3013	1409	•2N3250	2209	•2N4416 6503	N-FET
	2N3704	1433	2N3702	2225	•2N4857 6511	N-FET
	•2N5449	1701	•2N3829	2235	•TIS73 6103	N-FET
			•2N4058-62	2301	TIS74 6103	N-FET
			•2N5447	2305	TIS75 6103	N-FET
Relaxation Oscillator					•TI42A 24105	Trigger Diode
					•TI43A 24105	Trigger Diode
					2N1671B 7109	UJT
					•2N3980 7201	UJT
Pulse Amplifier	•2N2243A	1301	2N1907	17231	•2N4857 6511	N-FET
	•2N2369A	1327	•2N2894	2125		
			•2N2905	2131		
			•2N3829	2235		
			•2N5333	16701		
			•2N5384	16707		
			•2N5386	16711		
Chopper	•TIP29	16101	•TIP30	16105	2N3993A 6501	P-FET
	•TIP29A,B,C	16101	•TIP30A,B,C	16105	•2N4857 6511	N-FET
	•TIP31	16109	•TIP32	16113		
	•TIP31A,B,C	16109	•TIP32A,B,C	16113		
	•TIP33	16117	•TIP34	16121		
	•TIP33A,B,C	16117	•TIP34A,B,C	16121		
	•TIP35	16125	•TIP36	16129		
	•TIP35A,B,C	16125	•TIP36A,B,C	16129		
	•2N2432	1337	•2N2945	2139		
	•2N5301	16687	•2N3789	16557		
	•2N5302	16687	•2N3790	16557		
	•2N5303	16687	•2N3791	16557		
	•3N79	4101	•2N3792	16557		
			•2N4398	16645		
			•2N4399	16645		
			•3N111	4109		
Computer Memory Driver	•2N3013	1409			•TIS73 6103	N-FET
	•2N3015	1413			TIS74 6103	N-FET
	•2N3725	1437			TIS75 6103	N-FET
					•2N4857 6511	N-FET
Power Control/ Regulator (See Selection Guide on pages 11-14)	•TIP29	16101	•TIP30	16105	•TIC44-7 24109	SCR
	•TIP29A,B,C	16101	•TIP30A,B,C	16105	•2N3001-4 24401	SCR
	•TIP31	16109	•TIP32	16113	•2N3005-8 24407	SCR
	•TIP31A,B,C	16109	•TIP32A,B,C	16113	•2N3555-8 24417	SCR
	•TIP33	16117	•TIP34	16121	•2N3559-62 24425	SCR
	•TIP33A,B,C	16117	•TIP34A,B,C	16121		
	•TIP35	16125	•TIP36	16129		
	•TIP35A,B,C	16125	•TIP36A,B,C	16129		
	2N1724	16301	2N456A	17101		
	•2N2987-94	16401	2N1539	17223		
	•2N3418-21	16501	2N1907	17231		
	•2N3551,2	16507	TI3027	17301		
	•2N3713-16	16511	•2N3789	16557		
	•2N3996-9	16601	•2N3790	16557		
	•2N4000,1	16607	•2N3791	16557		
	•2N4002,3	16613	•2N3792	16557		
	•2N4300	16625	•2N4398	16645		
	•2N4301	16631	•2N4399	16645		
	•2N5301	16687	•2N5333	16701		

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APPLICATION	DEVICE RECOMMENDATION						
	BIPOLAR				OTHER DEVICES		
	N-P-N		P-N-P				
	Type No.	Page No.*	Type No.	Page No.*	Type No.	Page No.*	Classification
	•2N5302	16687	•2N5384	16707			
	•2N5303	16687	•2N5385	16707			
	•2N5387,8	16715	•2N5386	16711			
Computer Logic Switch	2N797	12101	2N404	9105	•TIS73	6103	N-FET
	2N1302	9205	2N964	12105	TIS74	6103	N-FET
	2N1304	9205	2N1303	9205	TIS75	6103	N-FET
	2N1306	9205	2N1305	9205	•2N4857	6511	N-FET
	2N1308	9205	2N1307	9205			
	•2N2369A	1327	2N1309	9205			
	•2N3013	1409	2N1997	9301			
			2N2635	12301			
			•2N2894	2125			
			•2N3250	2209			
			•2N3829	2235			
Series Shunt Regulator	•TIP29	16101	•TIP30	16105	•2N4857	6511	N-FET
	•TIP29A,B,C	16101	•TIP30A,B,C	16105			
	•TIP31	16109	•TIP32	16113			
	•TIP31A,B,C	16109	•TIP32A,B,C	16113			
	•TIP33	16117	•TIP34	16121			
	•TIP33A,B,C	16117	•TIP36	16125			
	•TIP35	16125	•TIP36A,B,C	16129			
	•TIP35A,B,C	16125	2N456A	17101			
	2N1724	16301	2N1038	17201			
	•2N2987-94	16401	2N1539	17223			
	•2N3418-21	16501	2N1907	17231			
	•2N3551,2	16507	TI3027	17301			
	•2N3713-16	16511	•2N5333	16701			
	•2N3996-9	16601	•2N5384	16707			
	•2N4000,1	16607	•2N5385	16707			
	•2N4002,3	16613	•2N5386	16711			
	•2N4300	16625					
	•2N4301	16631					
	•2N5387,8	16715					
Lamp Driver (Nixie Driver) High Voltage	•TIS100	1061	2N398	9101	•2N4857	6511	N-FET
	•TIS101	1061					
	•2N2243A	1301					
Linear Application: Demodulator	•3N79	4101	2N1907	17231	•2N4857	6511	N-FET
	•2N2432	1337					
Differential Amplifier	•2N2060	4401	•2N3350	4507	•2N5045	6601	N-FET
	•2N2642	4405					
	•2N3680	4509					
	•2N3838	4517					
	•2N2920	4409					
	•2N2977	4409					
	•2N2979	4409					
Operational Amplifier	•2N2060	4401	•2N3350	4507	•2N4854	4701	NPN-PNP
	•2N2223	4401			•2N5045	6601	N-FET
	•2N2642	4405					
	•2N3680	4509					
Servo Amplifier	•2N2060	4401	2N1038	17201	•2N5045	6601	N-FET
	•2N2223	4401	2N1907	17231			
	•2N2642	4405	•2N3350	4507			
	•2N3680	4509					
Sense Amplifier/ Comparator	•2N2060	4401	•2N3350	4507	•2N4416	6503	N-FET
	•2N2642	4405			•2N5045	6601	N-FET
	•2N3680	4509					
	•2N3838	4517					
	•2N2920	4409					
	•2N2977	4409					
	•2N2979	4409					
Waveform Generator/ Clipper/Compressor	2N930	1263	2N3702	2225	•2N4416	6503	N-FET
	2N3707	1435	•2N5447	2305	•2N4857	6511	N-FET

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APPLICATION	DEVICE RECOMMENDATION						
	BIPOLAR				OTHER DEVICES		
	N-P-N		P-N-P				
	Type No.	Page No.*	Type No.	Page No.*	Type No.	Page No.*	Classification
	2N3704	1433					
	2N3708	1435			•2N5245	6703	N-FET
	2N3709	1435			•2N5246	6703	N-FET
	2N3711	1435			•2N5247	6703	N-FET
	•2N5449	1701			•2N5248	6711	N-FET
					•2N492A	7101	UJT
Diode:							
Mixer/Converter					1N456-9	18101	
					1N482-5	18109	
					1N914	19201	
Detector					1N456-8	18101	
					•1N459	18101	
					1N914	19201	
					•1N4148	19401	
					•1N4448	19401	
Switch					•1N251	19101	
					•1N661	19151	
					1N914	19201	
					•1N3070	19303	200 V
					•1N4148	19401	
					•1N4448	19401	
					•1N4154	19403	
Tuning					•TIV306-8	21205	Voltage Variable
Voltage Regulator					1N746-1N759	23109	
					•1N746A-1N759A	23109	
					1N4370	23601	
					•1N4370A	23601	
Rectifier							
					1N456-9	18101	
					1N482-5	18109	
					•1N645-9	18113	
					•1N4001-7	25401	
Computer					•TID21-24	20005	8-Diode Array
					•TID25-26	20009	16-Diode Array
					•TID29-30	20013	20-Diode Array
					1N914	19201	
Transistor Biasing					•1N746A-1N759A	23109	
TV "Color Killer"					•1N3070	19303	
Power Supply					•1N645-9	18113	
Logarithmic					•1N645-9	18113	
					•1N746A-1N759A	23109	
Light Sensor					•LS400	27401	
					•LS600	27501	
					•TIL601	27503	
					•TIL602	27503	
					•TIL603	27503	
					•TIL604	27503	
					•TIL605	27503	
					•TIL606	27503	
					•TIL607	27503	
					•TIL608	27503	
					•1N2175	27801	
Infrared Source					•TIL01	27001	
					•TIL09	27009	

• Devices especially recommended for new design

* Preferred Semiconductors and Components Catalog

The following curves, arranged in ascending order of rated power dissipation at 100°C case temperature, show typical h_{FE} versus collector current at 25°C case temperature. Listed above each curve are the standard open-base collector-emitter voltage ratings available from among the device types listed.

N-P-N
2N2987-2N2994
10 W at 100°C
15 W at 25°C
V_{CEO}: 80 V and 100 V

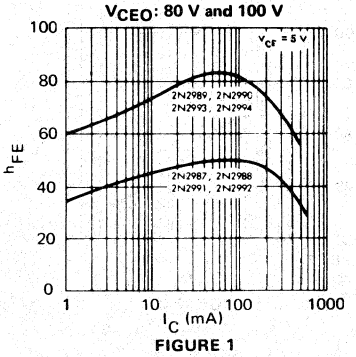


FIGURE 1

N-P-N
2N3418-2N3421
10 W at 100°C
15 W at 25°C
V_{CEO}: 60 V and 80 V

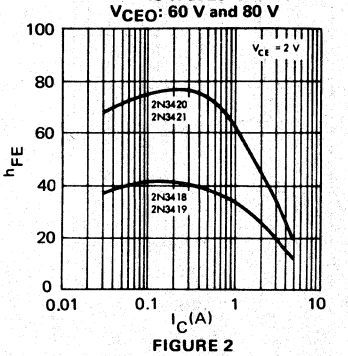


FIGURE 2

N-P-N
TIP29, TIP29A
12 W at 100°C
30 W at 25°C
V_{CEO}: 40 V and 60 V

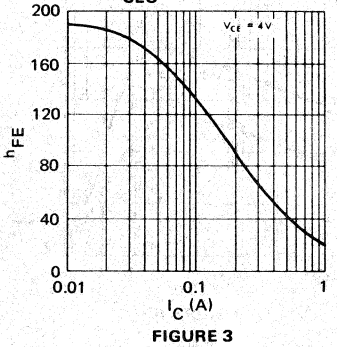


FIGURE 3

P-N-P
TIP30, TIP30A
12 W at 100°C
30 W at 25°C
V_{CEO}: 40 V and 60 V

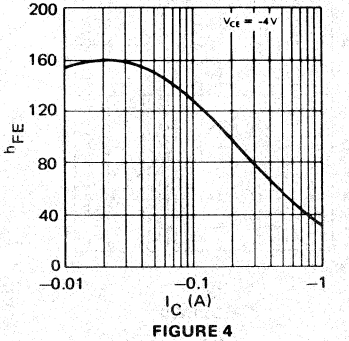


FIGURE 4

N-P-N
2N4000-2N4001
15 W at 100°C
V_{CEO}: 80 V and 100 V

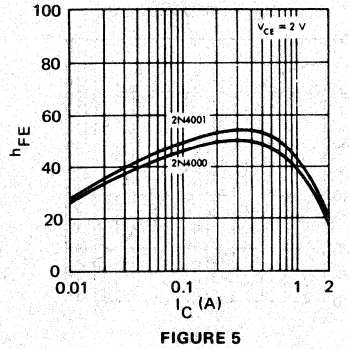


FIGURE 5

N-P-N
2N4300
15 W at 100°C
V_{CEO}: 80 V

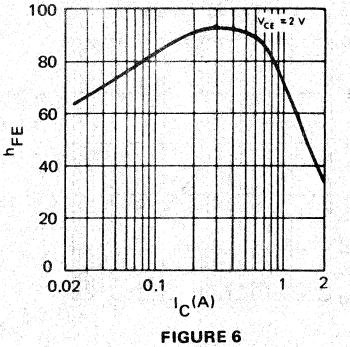


FIGURE 6

C

P-N-P
2N5333
15 W at 100°C
V_{CEO}: 80 V

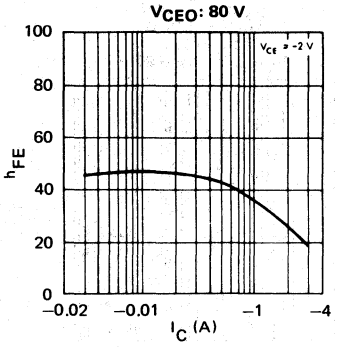


FIGURE 7

N-P-N
TIP31, TIP31A
16 W at 100°C
40 W at 25°C
V_{CEO}: 40 V and 60 V

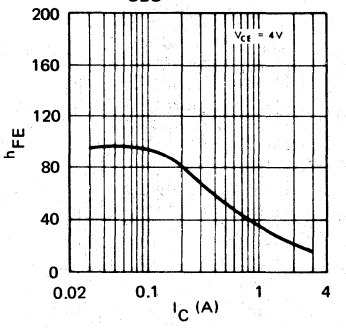


FIGURE 8

P-N-P
TIP32, TIP32A
16 W at 100°C
40 W at 25°C
V_{CEO}: 40 V and 60 V

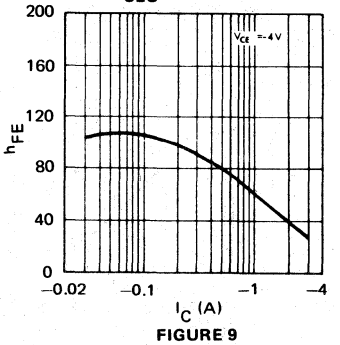


FIGURE 9

N-P-N
2N3996-2N3999
30 W at 100°C
V_{CEO}: 80 V

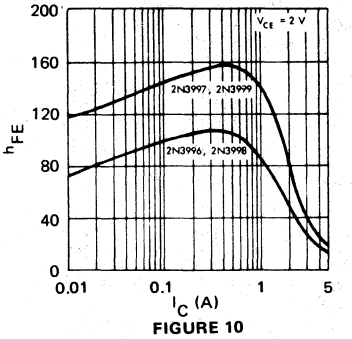


FIGURE 10

N-P-N
TIP33, TIP33A
32 W at 100°C
80 W at 25°C
V_{CEO}: 40 V and 60 V

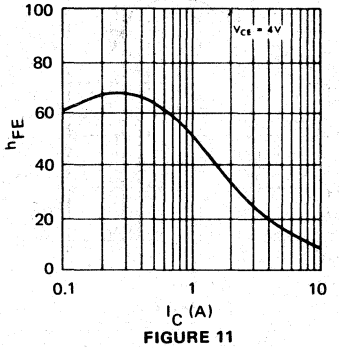


FIGURE 11

P-N-P
TIP34, TIP34A
32 W at 100°C
80 W at 25°C
V_{CEO}: 40 V and 60 V

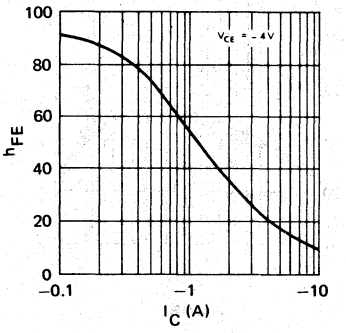


FIGURE 12

N-P-N
TIP35, TIP35A
36 W at 100°C
90 W at 25°C
V_{CEO}: 40 V and 60 V

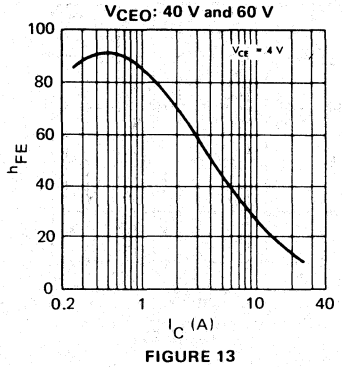


FIGURE 13

P-N-P
TIP36, TIP36A
36 W at 100°C
90 W at 25°C
V_{CEO}: 40 V and 60 V

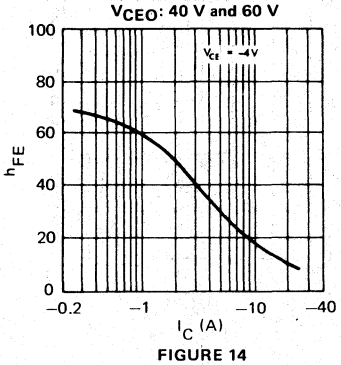


FIGURE 14

N-P-N
2N3551-2N3552
40 W at 100°C
V_{CEO}: 60 V and 80 V

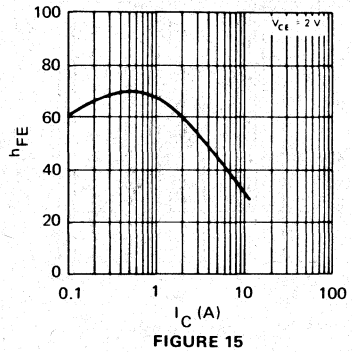


FIGURE 15

N-P-N
2N1724
50 W at 100°C
V_{CEO}: 80 V

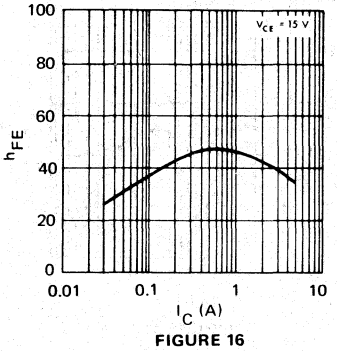


FIGURE 16

N-P-N
2N4301
50 W at 100°C
V_{CEO}: 80 V

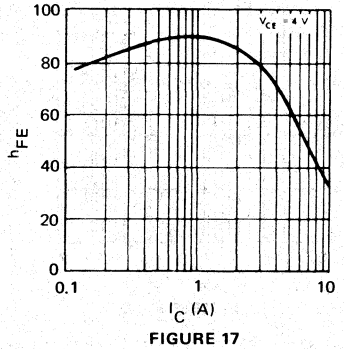


FIGURE 17

N-P-N
2N3713-2N3716
85 W at 100°C
150 W at 25°C
V_{CEO}: 60 V and 80 V

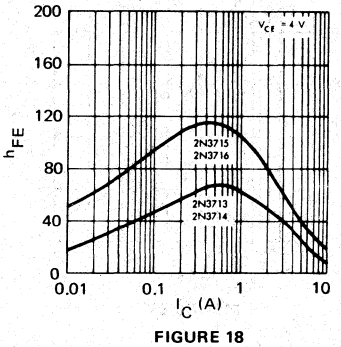


FIGURE 18

SELECTION GUIDE
SILICON POWER TRANSISTORS

C

P-N-P
2N3789-2N3792
85 W at 100°C
150 W at 25°C
V_{CEO}: 60 V and 80 V

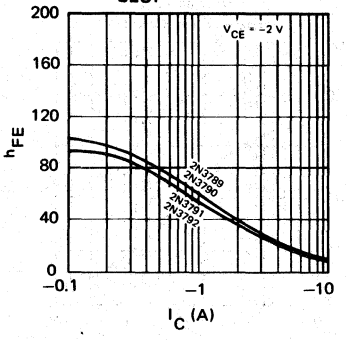


FIGURE 19

N-P-N
2N4002-2N4003
100 W at 100°C
V_{CEO}: 80 V and 100 V

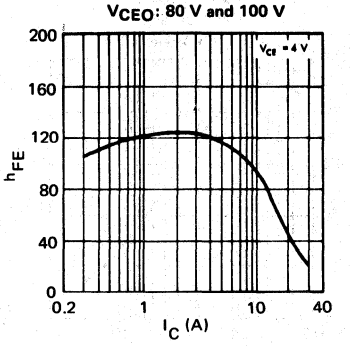


FIGURE 20

N-P-N
2N5387-2N5388
100 W at 100°C
V_{CEO}: 200 V and 250 V

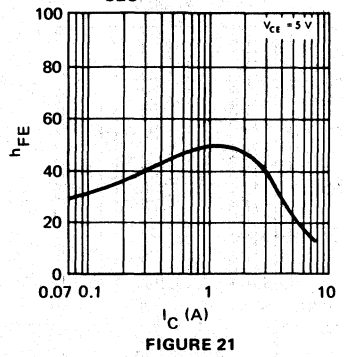


FIGURE 21

N-P-N
2N5301-2N5303
114 W at 100°C
200 W at 25°C
V_{CEO}: 40 V, 60 V, and 80 V

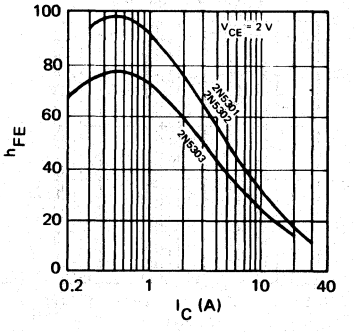


FIGURE 22

P-N-P
2N4398-2N4399
115 W at 100°C
200 W at 25°C
V_{CEO}: 40 V and 60 V

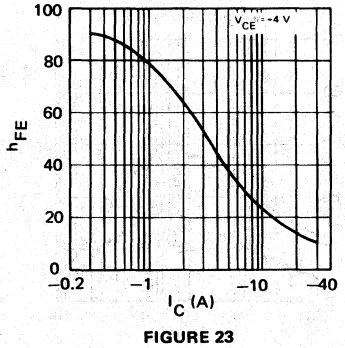


FIGURE 23

N-P-N
2N3846, 2N3847
150 W at 100°C
V_{CEO}: 200 V and 300 V

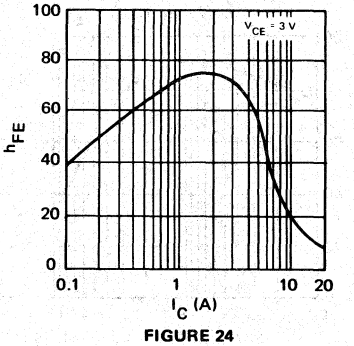


FIGURE 24

Ordering Instructions and Mechanical Data

ORDERING INSTRUCTIONS

Electrical characteristics presented in this catalog, unless otherwise noted, apply for circuit type(s) listed in the page heading regardless of package. Except for diode arrays, ECL, and MOS devices, the availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section. Other designations and packages are shown on individual data sheets.

Factory orders for circuits described in this catalog should include a four-part type number as explained in the following example.

EXAMPLE: SN 54H72 N –00

1. Prefix

MUST CONTAIN TWO OR THREE LETTERS
(From Individual Data Sheet)

RSN	Radiation-Hardened Circuit
SN	Standard Prefix
SNM	Mach IV, Level I
SNA	Mach IV, Level II
SNC	Mach IV, Level III
SNH	Mach IV, Level IV
SNX	Experimental Circuit

2. Unique Circuit Description

MUST CONTAIN THREE TO SIX CHARACTERS
(From Individual Data Sheet)

Examples: F50
G50
5410
74H10
54S112
54L78
15830
75450A

3. Package

MUST CONTAIN A SINGLE LETTER
F, H, J, L, N, P, S, T, U, W, or Z
(From Pin-Connection Diagram on Individual Data Sheet)

4. Instructions (Dash No.)

MUST CONTAIN TWO NUMBERS
(From Dash No. Column of Following Table)

PACKAGES	FORMED LEADS	SOLDER-DIPPED LEADS	INSULATOR	CARRIER	ORDER DASH NO.
METAL FLAT PACKAGES					
F, S, T	No	No	No	†	00
F, S, T	Yes	No	Yes	†	01
F, S, T	No	No	No	Mech-Pak	02
F, S, T	No	No	Yes	Mech-Pak	03
F, S, T	Yes	No	No	Mech-Pak	04
F, S, T	Yes	No	Yes	Mech-Pak	05
F, S, T	No	No	Yes	†	06
F, S, T	Yes	No	No	†	07
F, S, T	No	Yes	No	†	10
F, S, T	Yes	Yes	Yes	†	11
F, S, T	No	Yes	No	Mech-Pak	12
F, S, T	No	Yes	Yes	Mech-Pak	13
F, S, T	Yes	Yes	No	Mech-Pak	14
F, S, T	Yes	Yes	Yes	Mech-Pak	15
F, S, T	No	Yes	Yes	†	16
F, S, T	Yes	Yes	No	†	17
CERAMIC FLAT PACKAGES					
H, U, W, Z	No	No	N/A	†	00
H	No	No	N/A	Mech-Pak	02
H, U, W, Z	No	Yes	N/A	†	10
DUAL-IN-LINE PACKAGES					
J, N, P	No	No	N/A	†	00
N	Yes	No	N/A	†	07
J, N, P	No	Yes	N/A	†	10
N	Yes	Yes	N/A	†	17
PLUG-IN PACKAGES					
L	No	No	N/A	†	00
L	No	Yes	N/A	†	10

†These circuits are shipped in one of the carriers shown below. Unless a specific method of shipment is specified by the customer (with possible additional costs), circuits will be shipped in the most practical carrier. Please contact your TI sales representative for the method which will best suit your particular needs.

Flat (F, H, S, T, U, W, Z)
–Mech-Pakette
–Barnes Carrier
–Milton Ross Carrier

Dual-in-line (J, N, P)
–Slide Magazines
–A-Channel Plastic Tubing
–Barnes Carrier
–Sectioned Cardboard Box
–Individual Plastic Box

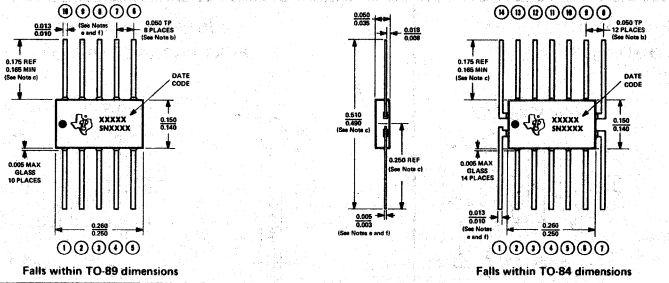
Plug-in (L)
–Barnes Carrier
–Sectioned Cardboard Box
–Individual Plastic Box

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

F, S, and T flat packages

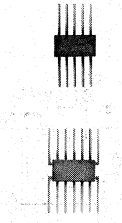
These hermetic packages feature glass-to-metal seals and welded construction. Package body and leads are gold-plated F-15‡ glass-sealing alloy. Approximate weight is 0.1 gram.

10- AND 14-PIN F AND S FLAT PACKAGE OUTLINES

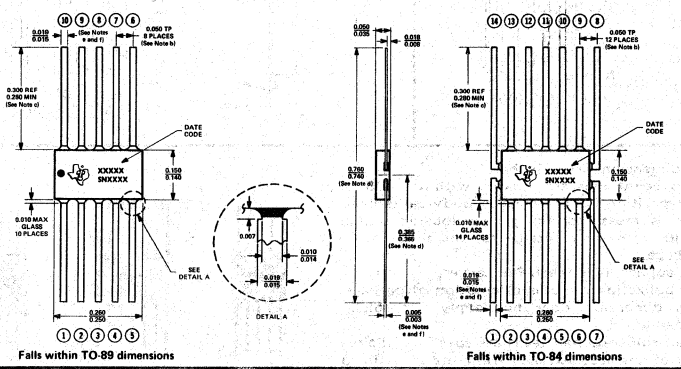


Falls within TO-89 dimensions

Falls within TO-84 dimensions

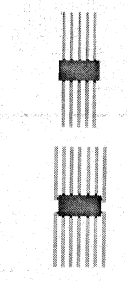


10- AND 14-PIN T FLAT PACKAGE OUTLINES



Falls within TO-89 dimensions

Falls within TO-84 dimensions



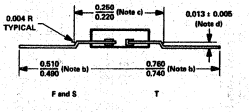
CIRCUIT SUBSTRATE IS ELECTRICALLY INSULATED FROM THE BODY OF THE F PACKAGE.
CIRCUIT SUBSTRATE IS IN ELECTRICAL CONTACT WITH THE BODY OF THE S AND T PACKAGES.

NOTES:
a. All dimensions are in inches.
b. Lead centerlines are located within 0.005 of true position (TP) relative to body centerlines. This is measured along lines located within 0.030 from (and parallel to) the sides of the package.
c. Not applicable in Mech-Pak carrier.
d. Symbolization denotes orientation of package.
e. This dimension does not apply for solder-dipped leads.
f. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to within 0.050 of the package body.

F, S, and T package leads

Gold-plated F-15‡ leads require no additional cleaning or processing when used in soldered or welded assembly. Solder-dipped leads are also available. Formed leads are available to facilitate planar mounting of networks on flat circuit boards. Circuits can be removed from Mech-Pak carriers with lead lengths up to 0.175 inch for the F and S packages and up to 0.300 inch for the T package.

FORMED LEADS



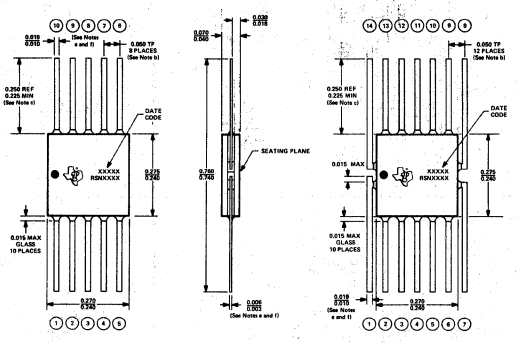
NOTES:
a. All dimensions are in inches.
b. Not applicable in Mech-Pak carrier.
c. Measured from centerline of outside bends.
d. Measured from center of lead to bottom of package where lead emerges from body.
e. When solder-dipped leads are specified, dipped area of lead extends from lead tip to outside bend (minimum).

‡F-15 is the ASTM designation for an iron-nickel-cobalt alloy containing nominally 53% iron, 29% nickel, and 17% cobalt.

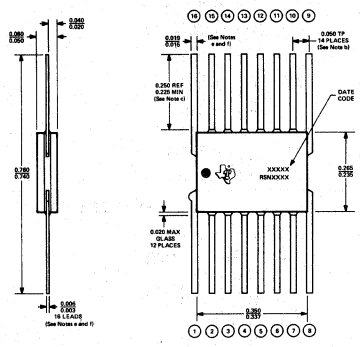
H flat packages

These packages each consist of a ceramic base, ceramic cap, and a 10- or 14-lead frame. Hermetic sealing is accomplished with glass. Gold-plated leads (–00) require no additional cleaning or processing when used in welded or soldered assembly.

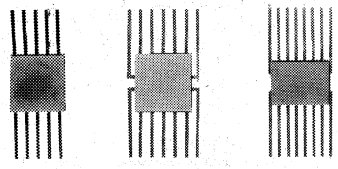
10- AND 14-PIN H CERAMIC FLAT PACKAGE OUTLINES



16-PIN H CERAMIC FLAT PACKAGE OUTLINE



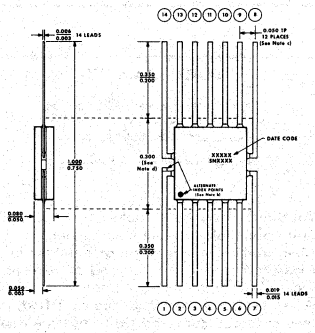
NOTES:
a. All dimensions are in inches.
b. Lead centerlines are located within 0.005 of true position (TP) relative to body centerlines. This is measured along lines located within 0.030 from (and parallel to) the sides of the package.
c. Not applicable in Mech-Pak carrier.
d. Symbolization denotes orientation of package.
e. This dimension does not apply for solder-dipped leads.
f. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to within 0.050 of the package body.



U and Z flat packages

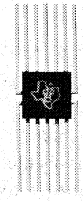
These flat packages consist of a ceramic base, ceramic cap, and 14-lead frame. Circuit bars are alloy-mounted in the U package and glass-mounted in the Z package. Hermetic sealing is accomplished with glass. Tin-plated leads require no additional cleaning or processing when used in soldered assembly.

14-PIN U AND Z CERAMIC FLAT PACKAGE OUTLINES



NOTES:
a. All dimensions are in inches.
b. Terminal identification is provided by either an index tab on pin 1 or an index dot.
c. Leads are within 0.005 radius of true position (TP) at maximum material condition.
d. This dimension determines a zone within which all body and lead irregularities lie.

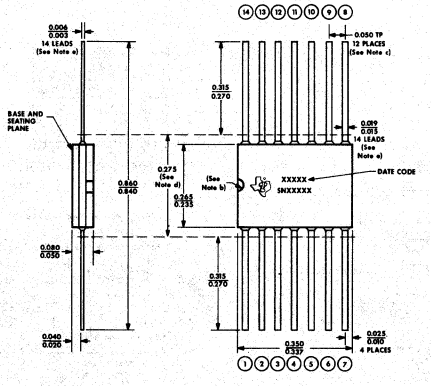
Falls Within
MO-004AA Dimensions



W ceramic flat packages

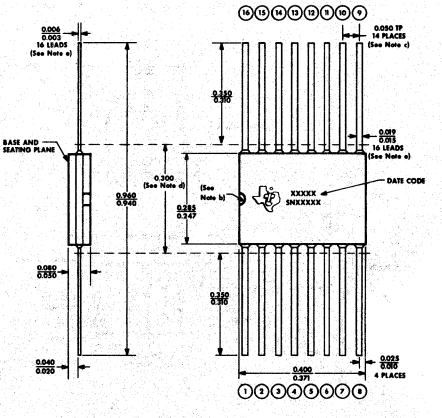
These hermetically sealed flat packages consist of an electrically nonconductive ceramic base and cap, and a 14-, 16- or 24-lead frame. Hermetic sealing is accomplished with glass. Tin-plated ("bright-dipped") leads (–00) require no additional cleaning or processing when used in soldered assembly.

14-PIN W CERAMIC FLAT PACKAGE OUTLINE



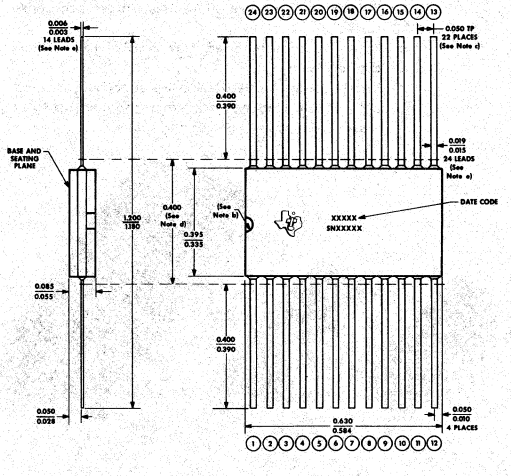
Falls Within
JEDEC MO-004AA Dimensions

16-PIN W CERAMIC FLAT PACKAGE OUTLINE



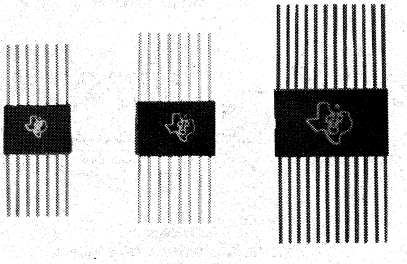
Falls Within
JEDEC MO-004AG Dimensions

24-PIN W CERAMIC FLAT PACKAGE OUTLINE



Falls Within
JEDEC MO-019AA Dimensions

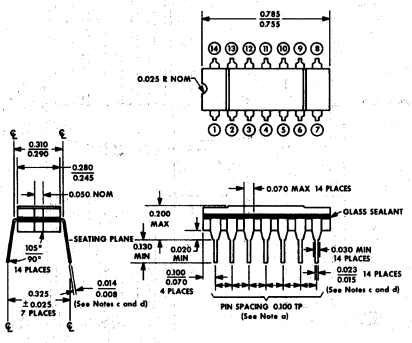
NOTES: a. All dimensions are in inches.
b. Index point is provided on cap for terminal identification only.
c. Leads are within 0.005 radius of true position (TP) at maximum material condition.
d. This dimension determines a zone within which all body and lead irregularities lie.
e. Not applicable for solder-dipped leads.
f. When solder-dipped leads are specified, dipped area extends from lead tip to within 0.050 of package body.



J ceramic dual-in-line packages

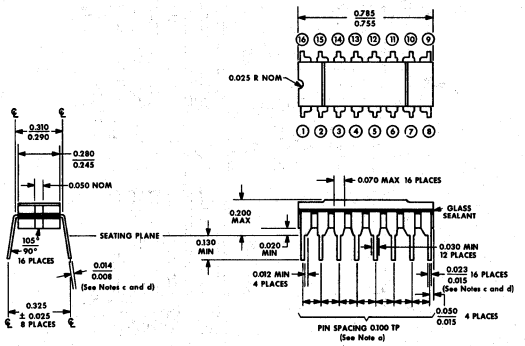
These hermetically-sealed, dual-in line packages consist of a ceramic base, ceramic cap, and a 14-, 16-, or 24-lead frame. The circuit bar is alloy-mounted to the base and hermetic sealing is accomplished with glass. This package is intended for insertion in mounting-hole rows on 0.300-inch centers. Once the leads are compressed to 0.300-inch separation and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads (–00) require no additional cleaning or processing when used in soldered assembly.

14-PIN J CERAMIC DUAL-IN-LINE PACKAGE OUTLINE

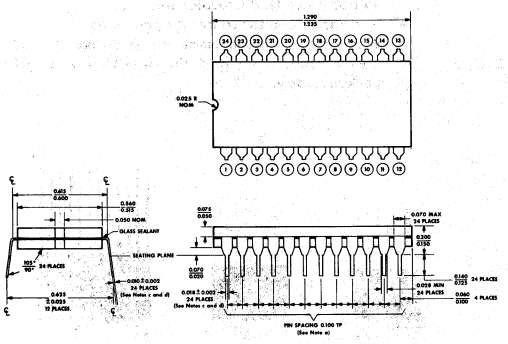


Falls Within JEDEC TO-116 and MO-001AA Dimensions

16-PIN J CERAMIC DUAL-IN-LINE PACKAGE OUTLINE

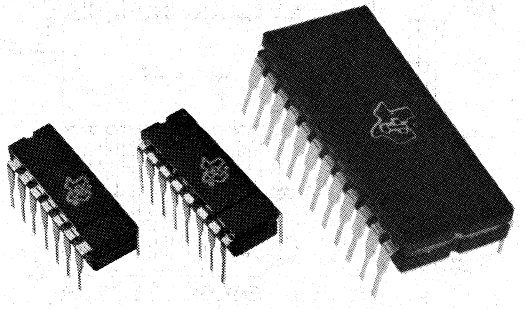


24-PIN J CERAMIC DUAL-IN-LINE PACKAGE OUTLINE



Falls Within JEDEC MO-015AA Dimensions

NOTES:
a. Each pin centerline is located within 0.010 of its true longitudinal position.
b. All dimensions are in inches unless otherwise noted.
c. This dimension does not apply for solder-dipped leads.
d. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0.020 above the seating plane.



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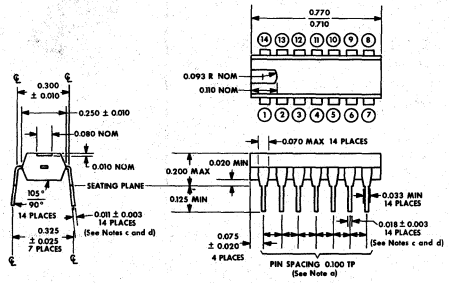
N plastic dual-in-line packages

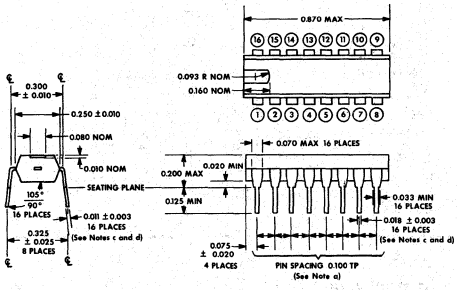
These dual-in-line packages consist of a circuit mounted on a 14-, 16-, or 24-lead frame and encapsulated within an electrically nonconductive, plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. These packages are intended for insertion in mounting-hole rows on 0.300-inch (or 0.600-inch) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Silver-plated leads (–00) require no additional cleaning or processing when used in soldered assembly.

14-PIN N PLASTIC DUAL-IN-LINE PACKAGE OUTLINE

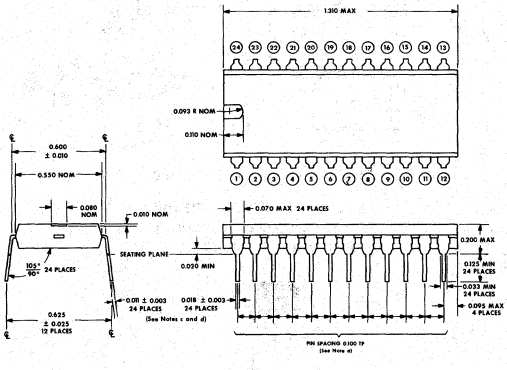


Falls Within JEDEC TO-116 and MO-001AA Dimensions

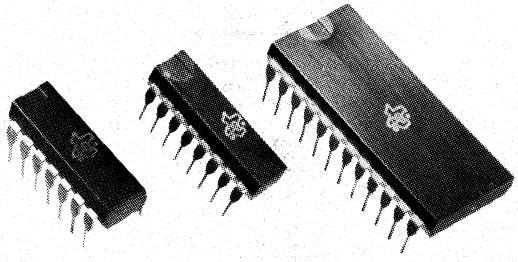
16-PIN N PLASTIC DUAL-IN-LINE PACKAGE OUTLINE



24-PIN N PLASTIC DUAL-IN-LINE PACKAGE OUTLINE



NOTES:
a. Each pin centerline is located within 0.010 of its true longitudinal position.
b. All dimensions are in inches unless otherwise noted.
c. This dimension does not apply for solder-dipped leads.
d. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0.020 above the seating plane.

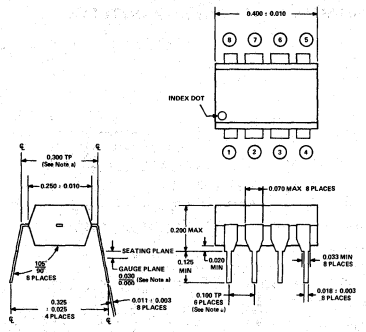


P plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a 8-lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. This package is intended for insertion in mounting-hole rows on 0.300-inch centers. Once the leads are compressed to 0.300-inch separation and inserted, sufficient tension is provided to secure the package in the board during soldering. Silver-plated leads require no additional cleaning or processing when used in soldered assembly.

1

8-PIN P PLASTIC DUAL-IN-LINE PACKAGE OUTLINE

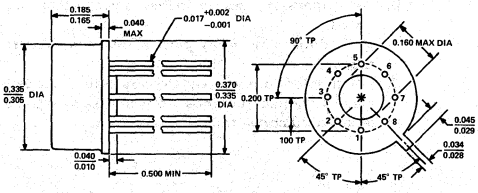


NOTES: a. Each pin is within 0.005 radius of true position (TP) at the guage plane with maximum material condition and unit installed.
b. All dimensions are in inches unless otherwise noted.

L plug-in packages

These hermetically sealed, plug-in packages each consist of a welded metal base and cap with individual leads secured by an insulating glass sealant. The gold-plated leads (–00) require no additional cleaning or processing when used in soldered assembly.

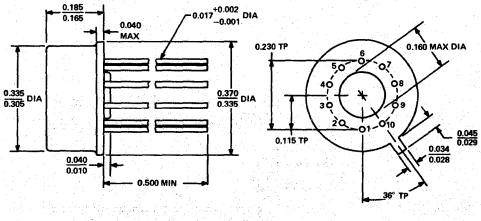
8-PIN L PLUG-IN PACKAGE OUTLINE



ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED.

Same as JEDEC TO-99 and MO-002AK except for diameter of standoff

10-PIN L PLUG-IN PACKAGE OUTLINE



ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED.

Same as JEDEC TO-100 and MO-006AD except for diameter of standoff

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Mach IV Procurement Specification

CONTENTS

MACH IV PROGRAM

1.0 SCOPE

1.1 This specification establishes standards for materials, workmanship, performance capabilities, identification and processing of high reliability, monolithic integrated circuits.

1.2 Intent

The intent of this document is such as to recognize that quality and reliability are *built* into, not *tested* into, a product. There is no specification or screening procedure that can substitute for inherent, built-in reliability. However, it must be realized that irrespective of lot quality, there will always be some small percentage of devices that are subject to early failure (infant mortality). A well engineered screening procedure will eliminate most, if not all, of these early failures. Secondly, the screening and acceptance testing described herein will also serve to demonstrate, with a high degree of statistical confidence, that the required levels of quality and reliability have, in fact, been built into the product.

2.0 APPLICABLE DOCUMENTS

2.1 The following specifications and standards, of the issue in effect on the date of invitation for bids or request for proposal, form a part of this specification to the extend specified herein:

2.2 Specifications

Military

MIL-M-55565	Microcircuits, Packaging of
MIL-M-38510	Microcircuits Devices, General Specification for

2.3 Standards

Military

MIL-STD-105	Sampling Procedures and Tables for Inspection by Attributes
MIL-STD-883	Test Methods and Procedures for Microelectronics (dated November 20, 1969)
MIL-STD-790	Reliability Assurance Program for Electronic Parts Specification
MIL-STD-1276	Leads, Weldable, for Electronic Components Parts
MIL-STD-1313	Microelectronics Terms and Definitions
MSFC-STD-355	Radiographic Inspection Standard for Electronic Parts

Detail Specifications

SNXXXX	Detail Specification for a Particular Part Type (e.g., Manufacturer's (Data Sheet)

2.4 Precedence of Documents

For the purpose of interpretation, in case of any conflicts, the following order of precedence shall apply:

a)	Purchase Order	—The purchase order shall have precedence over any referenced specification.
b)	Detail Specification	—The detail specification shall have precedence over this specification and other referenced specifications.
c)	This Specification	—This specification shall have precedence over all referenced specifications.
d)	Referenced Specifications	—Referenced Specifications shall apply to the extend specified herein.

2.5 Federal and/or military specifications and standards required shall be obtained from the usual government sources.

3.0 GENERAL REQUIREMENTS

The individual item requirements shall be as specified herein and in accordance with the applicable detail specification. In the event of any conflict between the requirements of this specification and the detail specification, the latter shall govern. The static and dynamic electrical performance requirements of the integrated circuits plus absolute maximum ratings and test methods shall be as specified in the detail specifications.

3.1.1 Definitions

a)	LTPD	Lot Tolerance Percent Defective shall be as defined by MIL-M-38510.
b)	λ	Lambda, stated in percent per 1000 hours as defined by MIL-M-38210.
c)	MRN	Minimum Reject Number as defined by MIL-M-38210
d)	Production Lot	For the purpose of this specification, a production lot shall be defined per MIL-M-38510.
f)	C	Acceptance number as defined by MIL-M-38510

3.1.2 Terms and Definitions

Terms and definitions shall be as defined in MIL-STD-1313.

3.1.3 Classification of Requirements

The requirements for the integrated circuits are classified herein as follows:

Requirement	Paragraph
Processing Conditioning, Testing and Screening	3.2
Qualification	3.3
Design and Construction	3.4
Marking of Integrated Circuits	3.5
Product Assurance	3.6
Workmanship	3.7
Performance Capabilities	3.8

3.2 Process Conditioning, Testing and Screening

Four levels of quality assurance for integrated circuits are provided for in this specification. Process conditioning, testing and screening shall be as specified in 4.3 and the applicable figure for the appropriate quality assurance level stated on the purchase order and defined as follows:

Prefix	Quality Assurance Process Level	Applicable Process Flow Chart
SNM	I	Figure 1
SNA	II	Figure 2
SNC	III	Figure 3
SNH	IV	Figure 4

3.3 Qualification

Vendor qualification for delivery of integrated circuits to this specification shall be as specified in paragraph 4.2.

3.4 Design and Construction

Integrated circuit design and construction shall be in accordance with the requirements specified herein and in the applicable detail specification.

3.4.1 Topography

Integrated circuits furnished under this specification shall have topography information available for review by procuring activity. The information made available shall provide sufficient data for thorough circuit design, application, performance, and failure analysis studies.

3.4.1.1 Monolithic Die Topography

An enlarged photograph or drawing (to scale) with a minimum magnification of 80 times the die (chip) size showning the topography of elements formed on the silicon monolithic die shall be available for review. This shall be identified with the specific detail integrated circuit part-type in which it is used and the applicable detail specification.

3.4.1.2 Die Intraconnection Pattern

An enlarged photograph or drawing (to scale) with a minimum magnification of 80 times the die (chip) size showing the specific intraconnection pattern utilized to intraconnect the elements in the circuit. This shall be in the same scale as the die topography 3.4.1.1 so that the elements utilized and those not being used can easily be determined.

3.4.2 Materials

Materials shall be inherently non-nutrient to fungus and shall not blister, crack, outgas, soften, flow or exhibit other immediate or latent defects that adversely affect storage, operation or environmental capabilities of integrated circuits.

3.4.2.1 Material Section

Materials selected for use in the construction of the integrated circuits shall be chosen for maximum suitability for the application. This shall include consideration of the best balance for:

a) Electrical performance

b) Thermal compatibility and conductivity

c) Chemical stability including resistance to deleterious interactions with other materials

d) Metallurgical stability with respect to adjacent materials and change in crystal configuration

e) Maximum stability with regard to continued uniform performance through the specified environmental conditions and life.

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PROCESS FLOW CHART FOR LEVEL I (SNM)

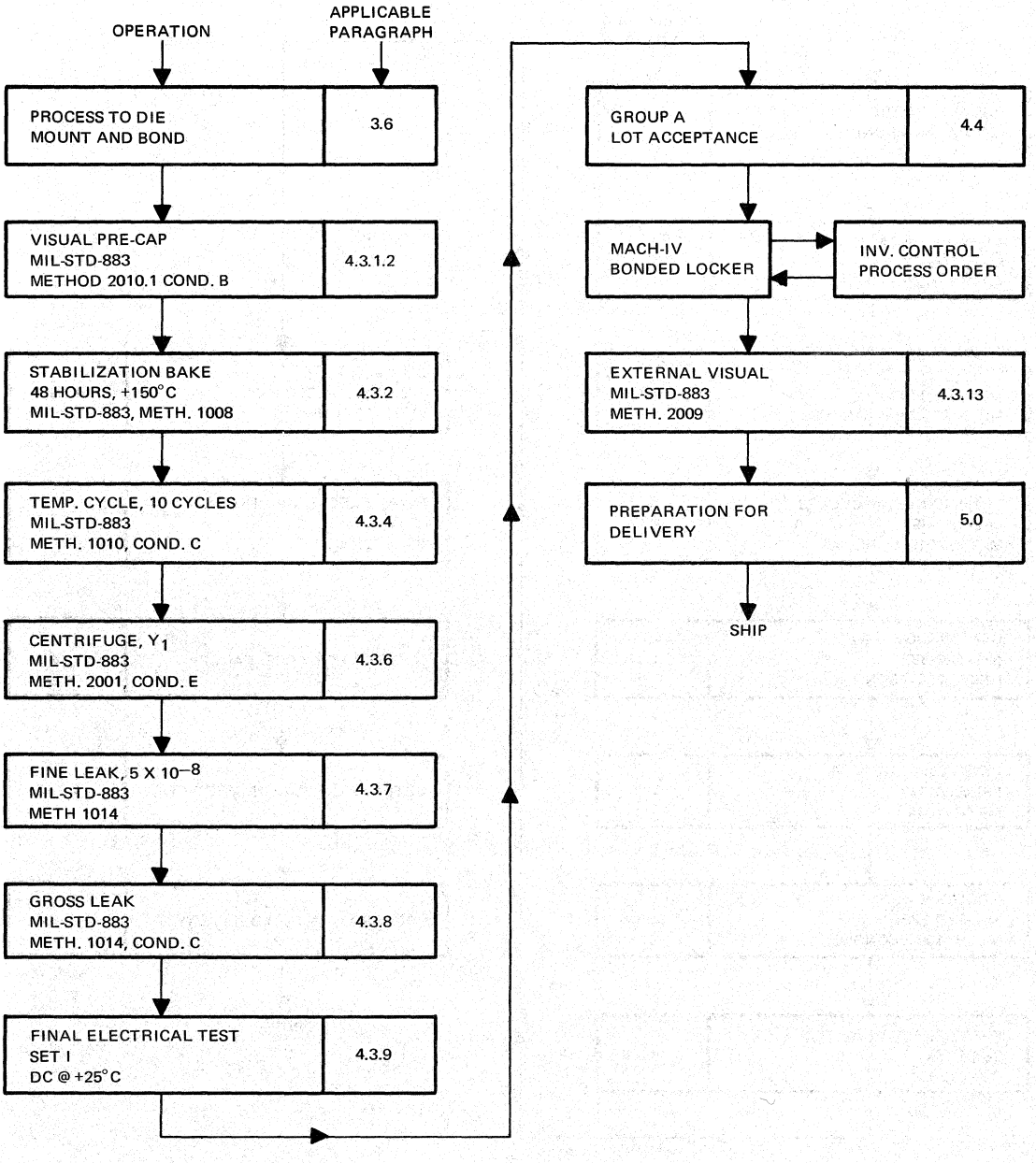

FIGURE 1

PROCESS FLOW CHART FOR LEVEL II (SNA)

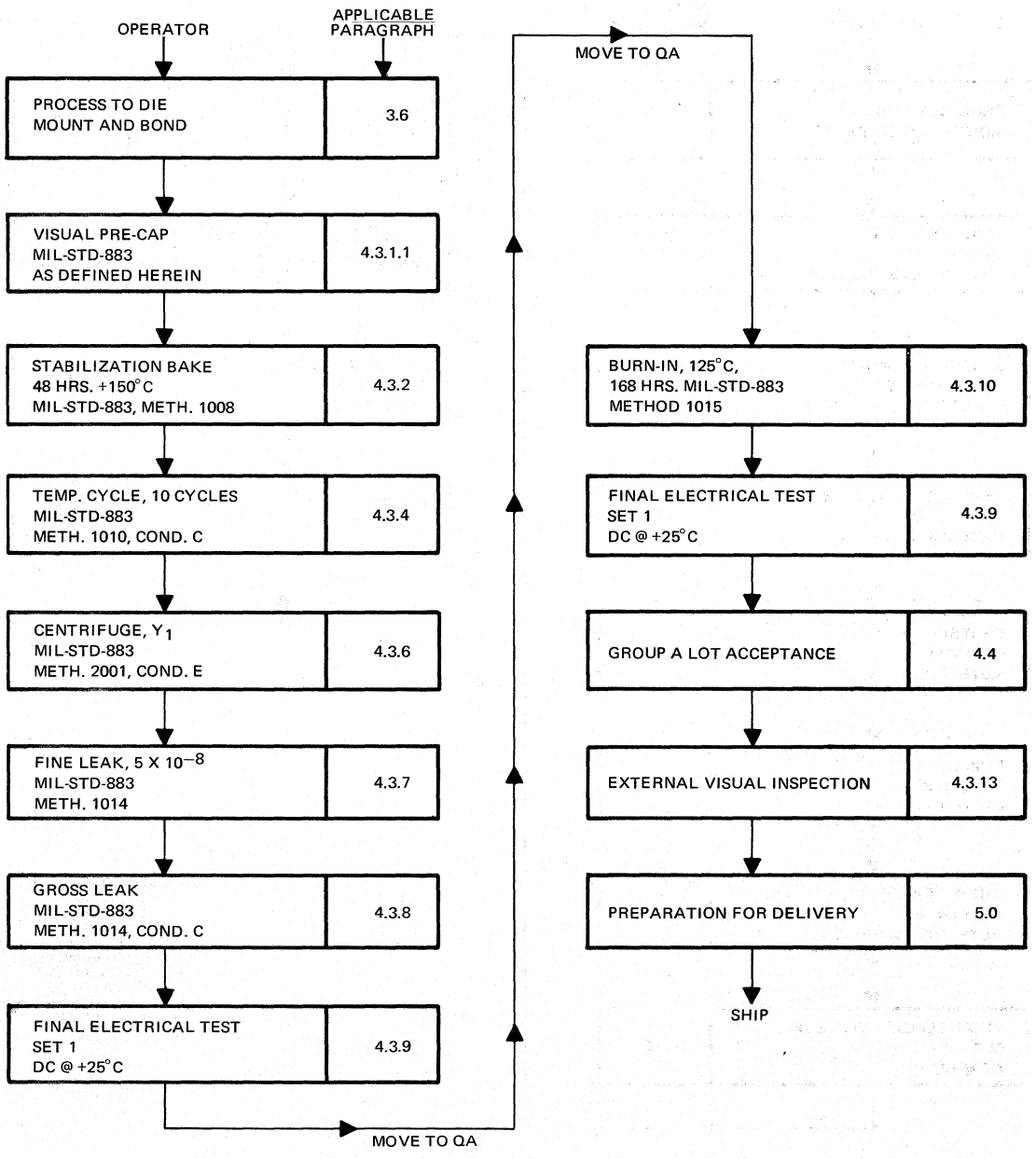

FIGURE 2

PROCESS FLOW CHART FOR LEVEL III (SNC)

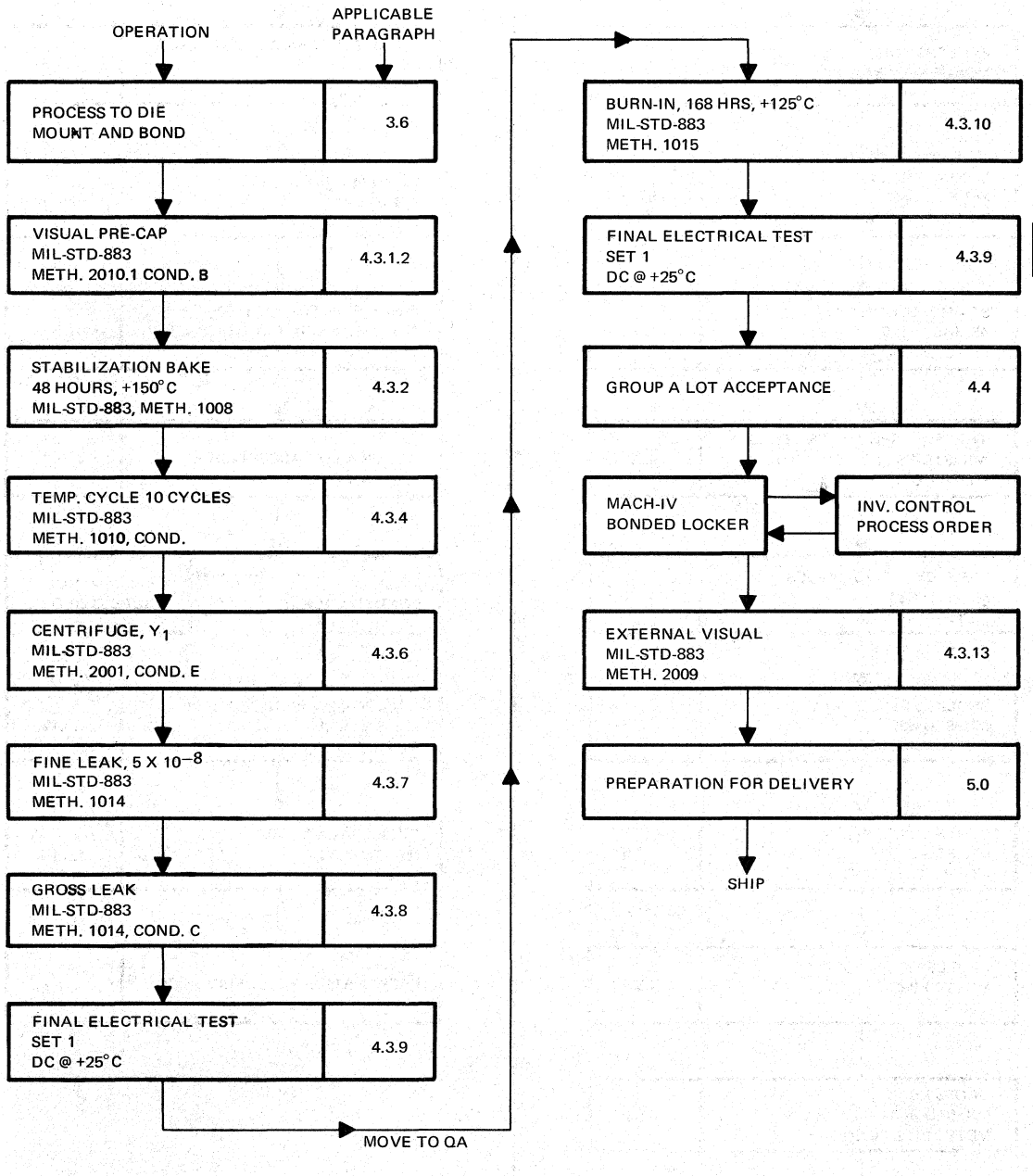

FIGURE 3

PROCESS FLOW CHART FOR LEVEL IV (SNH)

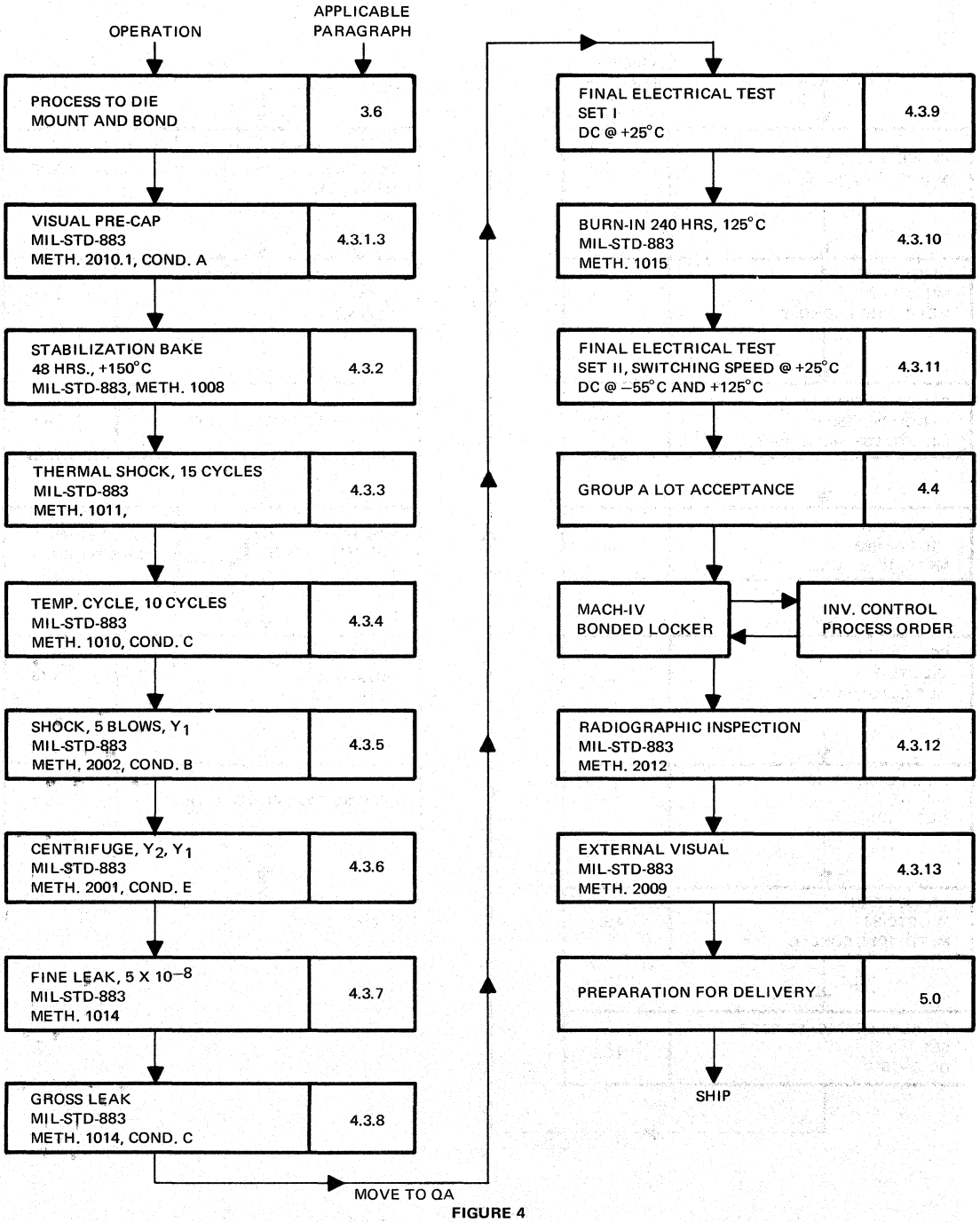

FIGURE 4

3.4.2.2 Foreign Materials

No lacquer, grease, paste, desiccant or other similar foreign encapsulant or coating material shall be included in the circuit enclosure nor applied to any part of the internal circuit assembly.

3.4.3 Mechanical

3.4.3.1 Case

Each integrated circuit shall be securely mounted and hermetically sealed within a case designed and constructed to conform to the outline and physical dimensions shown in the detailed specification. External surfaces of the integrated circuit case shall be unpainted except for markings.

3.4.3.2 Interconnections

Interconnections within the integrated circuit case shall be minimized and there shall be no wire crossovers. Circuit intraconnections by means of wire jumpers shall not be used. (See Note 6.2)

3.4.3.3 Leads

Lead material, construction, and outline shall be as specified on the detail specification and shall be capable of meeting the solderability test of MIL-STD-883, Method 20-3. (See Note 6.4).

3.4.3.3.1 Lead Size

Lead outline and dimensions shall be as specified in the detail specification.

3.4.3.3.2 Lead Surface Condition

Leads shall be free of the following defects over their entire length when inspected under a minimum of 4X magnification:

a) Foreign materials adhering to the leads such as paint, film, deposits and dust. Where adherence of such foreign materials is in question, leads may be subjected to a clean, contaminant-free (e.g., oil, dust, etc.), filtered air stream (suction or expulsion) or 88 feet per second maximum, or a wash/rinse as necessary and reinspected.

b) Nicks, cuts, scratches or other surface defacing defects which expose the base metal.

3.4.3.3.3 Lead Straightness

Leads shall be aligned within a 0.050-inch diameter, 0.050-inch length cylinder concentric to the point of lead emergence from the case and the X-axis (the axis parallel to the lead axis). Along the remaining lead length, there shall be no unspecified bend whose raduis is less than 0.10 inch and no twist whose angle is greater than 10° (ribbon leads, only).

3.4.3.3.4 Preformed Leads

Preformed leads, when specified, shall be in accordance with the detail specification. The part number of the integrated circuit shall remain as specified in the applicable detail specification or purchase order, the applicable suffix designation shall appear on the purchase order but shall not be marked on the device.

3.4.3.3.5 Carriers (Mech-Pak Carrier)

Carrier-matrix assemblies consisting of individually mounted integrated circuits shall be furnished when so specified by purchase order. The individual carrier shall have provisions for use with automatic test equipment contacts. Devices supplied "clipped-out" of the Mech-Pak Carrier shall be supplied in the Barnes Carrier type 029-188 or equivalent. (Applicable for Flat Packs only.)

3.5 Marking of Integrated Circuits

3.5.1 Legibility

All marking shall be permanent in nature and remain legible when subjected to specified operating, storage, and environmental requirements. All markings shall be insoluble in standard solvents such as trichlorethylene, water and xylene.

3.5.2 Marking Details

Marking of the integrated circuits shall be located as follows unless otherwise specified in the detail specification:

a) TO-100 (TO-5) and similar "can" cases shall be marked on the top of the case. Where space limitations exist, the side of the case may be used.

b) Flat Packs shall be marked on the top of the case. Where space limitation exists, the bottom of the package may be utilized as necessary. As a minimum the top of the package shall show the manufacturer's identification mark or symbol, the device part number, date code, and pin 1 orientation mark (where applicable).

c) Dual in-line plug-in packages shall be marked in the same manner as flat packs.

3.5.3 Required Device Marking

a) Index point indicating the starting point for numbering of leads shall be as indicated in the detail specification. The indexing point may be a tab, color dot, or other suitable indicator.

b) Manufacturer's identification mark or symbol.

c) A four or five digit alpha-numeric lot date code indicating the week of initial Group A acceptance. The date code shall be as follows:

1) EIA four digit date code, the first two numbers shall be the last two digits of the year, the last two numbers shall indicate the calendar week.

2) A Gothic letter which identifies separate lots of the same device type processed within the same calendar week. (If no more than one lot is processed through Lot Acceptance in a given calendar week, the Gothic letter may be omitted).

d) Manufacturer's part number.

e) Individual device serial number (if required)

f) A dot to indicate acceptance to Radiographic inspection

NOTE:

When a color dot is used to identify pin one, the radiographic inspection acceptance dot shall be placed on the bottom of the package.

3.6 Product Assurance

The manufacturer shall establish and maintain a reliability assurance program that complies with the basic intent of MIL-STD-790. Furthermore, it is intended that each integrated circuit delivered shall be free of any defect in design, material, manufacturing process, testing and handling, which would degrade or otherwise limit its performance when used within the specified limits.

3.6.1 Visual and Mechanical Examination

Integrated circuits shall be examined to verify that material, design, construction, physical dimensions, marking and workmanship are in accordance with the specified acceptance criteria.

3.6.2 Test Equipment

The manufacturer shall prepare and maintain a current list, by name and drawing number or other unique identification, of test equipment used in the manufacturing and testing of devices submitted for acceptance inspection under this specification. This list shall be made available to the procuring activity representative upon request.

3.6.3 Process Control

Each integrated circuit shall be constructed by manufacturing processes which are under the surveillance of the manufacturer's Quality Control department. The processes shall be monitored and controlled by use of statistical techniques in accordance with published specifications and procedures. The manufacturer shall prepare and maintain suitable documentation (such as quality control manuals, inspection instructions, control charts, etc.) covering all phases of incoming part and material inspection and in-process inspections required to assure that product quality meets the requirements of this specification. The procuring activity may verify, with the permission of and in the company of the manufacturer's designated representative, that suitable documentation exists and is being applied. Information designated as proprietary by the manufacturer will be made available to the procuring activity or its representative only with the written permission of the manufacturer.

Process control is recognized as being vital to the concept of "built-in" quality. Appendix A defines an acceptable process-control system. Devices delivered to this specification shall be manufactured in a controlled system similar to that set forth in Appendix A.

3.6.4 Production Changes

The manufacturer shall advise the procuring activity of the time at which any major change(s) in production or QC methods or documentation become effective during the period of device production for delivery against any given purchase order referencing this specification.

3.7 Workmanship

Integrated circuits shall be manufactured and processed in a careful and workmanlike manner, in accordance with the production processes, workmanship instructions, inspection and test procedures, and training aids prepared by the manufacturer in fulfillment of the reliability assurance program established by paragraph 3.6.

3.7.1 Personnel Certification

The manufacturer shall be responsible for training, testing and certification of personnel involved in producing integrated circuits. Training shall be commensurate and consistent with the requirements of this specification and in conformance to the basic intent of MIL-STD-790. Training aids in the form of satifactory criteria shall be available for operator and inspector review at any time.

3.7.2 Personnel Evaluation

The supplier shall maintain a continuous evaluation of the proficiency of personnel concerned with production and inspection. Retraining of an operator or inspector shall be required when this evaluation establishes that a degree of proficiency necessary to meet the requirements of this specification is not being exercised.

3.7.3 Rework Provisions

3.7.3.1 Rework

All rework on microcircuits manufactured under this specification shall be accomplished in accordance with paragraph 3.7.1 of MIL-M-38510 except as defined herein.

3.7.3.2 Rebonding

Rebonding of integrated circuits shall be permitted with the following limitations:

a) No scratches, open or discontinuance metallization paths or conductor patterns shall be repaired by bridging with or addition of bonded wire or ribbon.

b) Rebonding at individual bonding pad locations shall be limited to a maximum of 3 rebonds for 14 pin devices, 4 rebonds for 16 pin devices, 7 rebonds for devices with more than 16 pins, and 2 rebonds for devices with less than 14 pins.

c) Rebonding shall be limited to not more than one rebond attempt at any single bond pad location.

d) Rebonding shall be limited to level I, II and III devices only. Rebonding of level IV (class A type) devices shall not be permitted.

3.8 Performance Capabilities

The integrated circuits delivered to this specification shall be designed to be capable of meeting the environmental requirements specified in Table II. The manufacturer need not perform these tests specifically for the contract or specification, but shall provide data which demonstrates the ability of the integrated circuits to pass the environmental tests. The data shall have been generated on devices from the same generic family as the circuits being supplied to this specification, and the package configuration shall be the same as for the delivered parts. (i.e., Flat Pack, TO-100, etc.).

3.9 Quality and Reliability Assurance Program Plan

The manufacturer shall establish and implement a Quality and Reliability Assurance Program Plan that meets the intent of MIL-M-38510, Appendix A. Submission of the program plan to the procuring activity shall not be a requirement of this specification; however, the program plan shall be maintained by the manufacturer and shall be available for review by the procuring activity.

4.0 QUALITY ASSURANCE PROVISIONS

4.1 Responsibility for Inspection

Unless otherwise specified in the contract or purchase order, the manufacturer is responsible for the performance of all inspection requirements specified herein. Except as otherwise specified, the manufacturer may utilize his own facilities or any commercial laboratory acceptable to the procuring activity. The procuring activity may, at its discretion, perform any of the inspections set forth in the specification where such inspections are deemed necessary to assure supplies and services conform to prescribed requirements.

4.1.2 Inspection at Point of Delivery

The procuring activity may, at its discretion, reinspect any or all of the delivered parts. (Excluding Group B destructive samples as defined by MIL-STD-883). All parts found to be defective and/or lacking specified documentation (such as test documentation) may be returned to the manufacturer at the manufacturer's expense.

4.1.3 Inspection Records

The manufacturer shall maintain a reliability data and records library. This library shall have on file, for review by the procuring activity, records of examination, qualification test results, variables data (when required) and all other pertinent data generated on devices manufactured to this specification.

4.1.4 Control of Procurement Sources

The manufacturer shall be responsible for assuring that all supplies and services conform to this specification, the detail specification and the manufacturer's procurement requirements.

4.1.4.1 Manufacturer's Receiving Inspection

Purchased supplies shall be subjected to inspection after receipt as necessary to assure conformance to contract requirements. In selecting sampling plans, consideration shall be given to the controls exercised by the procurement source and evidence of sustained quality conformance.

4.1.4.2 The manufacturer shall provide procedures for withholding from use all incoming supplies pending completion of required tests or receipt of necessary certification or test records and their evaluation.

4.1.4.3 The manufacturer shall initiate corrective action with the procurement source depending upon the nature and frequency of receipt of nonconforming supplies.

4.1.5 Procuring Activity Quality Assurance Representative

The procuring activity, may, at its discretion, place quality assurance representatives in the manufacturer's plant as deemed necessary to assure conformance to contract requirements in any non-proprietary phase of design, fabrication, processing, inspection, testing, and reliability of the integrated circuits being produced. The manufacturer shall provide reasonable facilities and assistance for the safety and convenience of such personnel in the performance of their duties. Inspection and test procedures shall be made available for review by the quality assurance representative.

4.2 Qualification and Quality Conformance Inspection

4.2.1 Qualification

Manufacturer's qualification shall be based on compliance with the established reliability test program requirements of paragraph 4.2.1.1 herein. The manufacturer may, at his discretion, substitute the qualification test plan of paragraph 4.2.1.2 in order to establish initial qualification. However, the substitution of parapraph 4.2.1.2 does not relieve the manufacturer from the responsibility of establishing an in-house reliability evaluation program as defined by paragraph 4.2.1.1.

4.2.1.1 Established Reliability Test Program

The manufacturer shall have an established and well defined in-house reliability program. This program shall be so designed as to demonstrate that the manufacturer's product is capable of meeting, as a minimum, the environmental and minimum life requirements listed in Table I herein. The reliability program may be modeled after the test procedure of Table I or it may take the form of a step-stress testing program similar to that defined by MIL-STD-883, Method T5006. The program shall be on-going in nature; that is, at specified intervals the manufacturer shall randomly select product that is representative of current production techniques, and subject the devices to the specified tests. Sampling shall be done on each generic family.

4.2.1.2 Qualification Test Program

In lieu of meeting the requirements of 4.2.1.1, the manufacturer may establish qualification by performing an initial, one-time qualification test in accordance with Table I herein. Qualification testing shall be performed on each generic family supplied to this specification. Upon successful completion of the qualification program, the manufacturer shall remain qualified for a period not to exceed 12 calendar months. Continued qualification shall then be based on compliance with the requirements of paragraph 4.2.1.1.

4.2.1.3.1 Procedures and Definitions

4.2.1.3.1 Sampling Procedure

Device selection for the qualification procedure of 4.2.1.1 or 4.2.1.2 shall be based on a random sampling technique. Testing shall be done on a mixture of device types that adequately represent the entire generic family. The following is a recommended mix ratio:

Gates	:	65% of total sample
Flip-Flops	:	25% of total sample
MSI	:	10% of total sample

4.2.1.3.2 Generic Family

Electrically and structurally similar devices shall be said to comprise a generic family (e.g., TTL) if they meet the following criteria:

a) Are designed with the same basic circuit-element configuration such as TTL, DTL, ECL, or Linear, and differ only in the number or complexity of specified circuits which they contain.

b) Are designed for the same supply, bias and signal voltage, and for input/output capability with each other under an established set of loading rules.

c) Are enclosed in housing (packages) of the same basic construction (e.g., hermetically sealed flat packages, dual-in-line cermaic, dual-in-line plastic) and outline, differing only in the number of active housing terminals included and/or utilized.

4.2.2 Quality Conformance Inspection (Lot Inspection)

When specifically called out on the purchase order or contract, the manufacturer shall perform the lot qualification inspections, Group B and/or Group C in Table II.

4.2.2.1 Lot Acceptance Sampling

Statistical sampling for Group B and/or Group C lot acceptance inspections shall be in accordance with MIL-M-38510 Table B-1.

Group B samples shall be selected from sub-lots that have successfully completed all of the 100% processing steps, up to and including Group A Lot Acceptance, specified on the applicable process flow chart.

4.2.2.2 Resubmission/Failed Lots

Where a lot fails any one of the sub-group qualification requirements of Table II, it may be resubmitted a maximum of one time for qualification to that particular sub-group provided an analysis is performed to determine the failure mechanism for each reject device in the sub-group, and that it is determined that the failures are due to one of the following:

a) Testing error resulting in electrical damage to devices,

b) A defect that can effectively be removed by rescreening the lot,

c) Random defects which do not reflect poor basic device designs or poor workmanship.

4.2.2.3 Early Shipments

When lot qualification inspection is being performed for a specific contract or purchase order, the accepted Group A devices that are awaiting shipment pending successful completion of Group B and/or Group C, shall be stored in the MACH IV bonded locker. Under no circumstances shall such parts be shipped prior to the successful completion of the Group B tests.

4.2.2.4 Group B Test Data

All data generated by Group B and/or Group C testing shall accompany the initial shipment of devices. This data shall consist, at a minimum, of the following:

a) Attributes data for Group B. Endpoints for the subgroups are visual per the applicable MIL-STD-883 test method.

b) Variables data for Group C subgroups 1, 2, 4, and 5. Endpoints for these subgroups shall be "critical eletrical parameters" only. These parameters are designated by an asterisk (*) on the detail specification.

4.2.2.5 Procedure In Case Of Test Equipment Failure Or Operator Error

Where an integrated circuit is believed to have failed as a result of faulty test equipment or operator error, the failure shall be entered in the test record which shall be retained for review along with a complete explanation verifying why the failure is believed to be invalid. If it is determined that the failure is invalid, a replacement integrated circuit from the same inspection lot may be added to the sample. The replacement integrated circuit shall be subjected to all those tests to which the discarded integrated circuit was submitted prior to its failure, and any remaining specified test to which the discarded integrated circuit was not subjected prior to its failure.

4.3 Quality Assurance Processing, Methods and Procedures

This section establishes the test methods and conditions to be used for the 100% processing (screening) requirements specified by the applicable process flow chart.

4.3.1 Precap Visual Inspection

Each microcircuit shall be required to pass the appropriate precap visual inspection defined as follows. Precap Lot Acceptance shall be per paragraph 4.6.

4.3.1.1 Level II devices shall be visually inspected in accordance with the criteria listed in Section 6.1.3 of this specification. Inspection procedures and equipment requirements shall be as defined in MIL-STD-883.

4.3.1.2 Level I and III devices shall be visually inspected in accordance with MIL-STD-883, Method 2010.1, Condition B as defined by Revision Notice 2 dated November 20, 1969. (See Note 6.1.2.)

4.3.1.3 Level IV devices (designated for NASA type applications) shall be visually inspected in accordance with MIL-STD-883, Method 2010.1, Condition A as defined by Revision Notice 2 dated November 20, 1969. (See Note 6.1.1.)

4.3.2 Stabilization Bake

The purpose of this test is to determine the effect on microelectronic devices of baking at elevated temperatures without electrical stress applied. Test shall be performed in accordance with MIL-STD-883, Method 1008, Condition C.

4.3.3 Thermal Shock

The purpose of this test is to determine the resistance of the device to sudden exposure to extreme changes in temperature. Test shall be performed in accordance with MIL-STD-883, Method 1011, Condition A.

4.3.4 Temperature Cycle

This test is conducted for the purpose of determining the resistance of a part to exposures at extremes of high and low temperatures, and to the effect of alternate exposures to these extremes, such as would be experienced when equipment or parts are transferred to and from heated shelters in arctic areas. Test shall be performed in accordance with MIL-STD-883, Method 1010, Condition C, minimum of 10 cycles.

4.3.5 Mechanical Shock

The shock test is intended to determine the suitability of the devices for use in electronic equipment which may be subjected to moderately severe shocks as a result of suddenly applied forces or abrupt changes in motion produced by rough handling, transportation, or field operation. Test shall be performed in accordance with MIL-STD-883, Method 2002, Condition B, five blows minimum.

4.3.6 Centrifuge

The centrifuge test is used to determine the effects on microelectronic devices of a centrifugal force. This test is designed to indicate structural and mechanical weaknesses not necessarily detected in shock and vibration tests. Test shall be performed in accordance with MIL-STD-883, Method 2001, Condition E.

4.3.7 Fine Leak Test

Each integrated circuit shall be subject to a fine leak test in accordance with paragraph 4.3.7.1 or 4.3.7.2. The method shall be optional providing it is consistent with and capable of detecting the specified leak rate of the applicable process flow chart.

4.3.7.1 Helium Leak Test

Helium leak test shall be performed in accordance with MIL-STD-883, Method 1014, Condition A. Helium bomb pressure shall be 30 psig maximum, bomb time shall be 4 hours minimum.

4.3.7.2 Radiflo Leak Test

Radiflo leak test shall be performed in accordance with MIL-STD-883, Method 1014, Condition B. Krypton 85 bomb pressure and dwell time are a function of the radioactivity level and shall be selected so as to conform to the equations given in Condition B.

4.3.8 Gross Leak Test

Each integrated circuit shall be subjected to the appropriate gross-leak test of paragraphs 4.3.8.1 or 4.3.8.2. The manufacturer may, at his option, perform gross-leak testing after the Set I Final Electrical Tests of paragraph 4.3.9.

4.3.8.1 Glass to metal hermetic flat packs shall be tested in accordance with MIL-STD-883, Method 1014, Condition C, Step 2. Units will be bombed 4 hours minimum at 30 psi in FC-78. Units will then be immersed in FC-40 at +125°C ±5°C for 20 seconds minimum and observed for one large bubble or a continuous stream of small bubbles.

4.3.8.2 Glass to glass (ceramic) hermetic package shall be tested in accordance with MIL-STD-883, Method 1014, Condition C, Step 1.

4.3.9 Final Electrical Test (Set I)

Each integrated circuit shall be required to pass the electrical requirements of Subgroup 1 of the detail specification (DC @ +25°C). The manufacturer shall also perform such additional testing necessary to assure the parts will meet the temperature extreme limits.

4.3.10 Burn-In

2

The burn-in screen is performed for the purpose of eliminating marginal devices, those and early life failures evidenced as time and stress dependent. Test shall be in accordance with MIL-STD-883, Method 1015, Condition D or E at 125 ± 5°C for 168 hours minimum. The bias shall be removed from the devices prior to their return to 25°C. (See Note 6.3)

4.3.11 Final Electrical Test (Set II)

Each integrated circuit shall be required to pass the electrical requirements of the detail specifications. The following tests shall be performed as a minimum: d-c at maximum and minimum rated temperatures, and switching parameters at 25°C.

The manufacturer may, when deemed necessary, elect to perform additional electrical testing over and above the requirements stated herein.

4.3.12 Radiographic Inspection (X-ray)

Test shall be performed in accordance with MIL-STD-883, Method 2012. The integrated circuit shall be required to pass a radiographic inspection to these requirements. In addition, the acceptance criteria shall meet, as a minimum, the requirements of NASA MSFC specification MSFC-STD-355.

4.3.13 External Visual Inspection

The purpose of this examination is to verify that materials, construction, marking, and general workmanship are as specified. Examination shall be in accordance with MIL-STD-883, Method 2009.

4.4 Group A Lot Acceptance

Each lot of integrated circuits shall be sampled by Quality Control to the LTPD's given below:

GROUP A ACCEPTANCE

SUBGROUP	LTPD LEVEL I & II	LTPD LEVEL III & IV
Subgroup 1 25°C, d-c	7%	5%
Subgroup 2 +125°C, d-c	7%	5%
Subgroup 3 −55°C, d-c	7%	5%
Subgroup 4 Switching Speed @ +25°C	15%	10%

NOTE: Functional tests included in d-c tests.

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TABLE I
MANUFACTURERS QUALIFICATION PROCEDURE

TEST	MIL-STD-883 METHOD	CONDITIONS	LTPD
Subgroup 1			
Physical Dimensions Visual and Mechanical	2008	Condition A & B	15
Subgroup 2†			
Solderability	2003		15
Subgroup 3†			
Thermal Shock	1011	Condition B	
Temperature Cycling	1010	Condition C	
Moisture Resistance	1004	Omit step 7B and Initial Conditioning	
Critical Electrical Parameters	5004	25°C, DC	15
Subgroup 4‡			
Mechanical Shock	2002	Condition B	
Vibration Variable Freq.	2007	Condition A	
Constant Acceleration	2001	Condition E	
Critical Electrical Parameters	5004	25°, DC	15
Subgroup 5†			
Lead Fatigue	2004	Condition B2	
Fine Leak	1014	Condition A, Per Para. 4.3.7 Herein	
Gross Leak	1014	Condition C, Per Para. 4.3.7 Herein	15
Subgroup 6†			
Salt Atmosphere	1009	Condition A, Omit Initial Conditioning	15
Subgroup 7‡			
Storage Life	1008	150°C, 1000 Hrs. Minimum	
Critical Electrical Parameters	5004	25°C, DC	10
Subgroup 8‡			
Operating Life	1005	125°C, 1000 Hrs. Minimum Return to 25°C without bias	
Critical Electrical Parameters	5004	25°C, DC	10
Subgroup 9†			
Bond Strength			10 devices not greater than 1% defective
a. Thermocompressions	2011	Condition B, D	
b. Ultrasonic	2011	Condition B, D	

†Visual and/or hermetic end points hence electrical or visual rejects may be used. Reference MIL-STD-883. Method 5005, Para. 3.4.

‡Electrical end points only.

TABLE II
LOT ACCEPTANCE/PERIODIC QUALIFICATION TEST
(GROUP B/GROUP C)

GROUP B

TEST	MIL-STD-883 METHOD	CONDITIONS	LTPD LEVEL I & II	LTPD LEVEL III & IV
Subgroup 1				
Physical Dimensions Visual and Mechanical	2008	Condition A	15	10
Subgroup 2				
Marking Permanency	2008	Condition B, para. 3.2.1		
Visual and Mechanical	2008	Condition B per applicable detail specification		
Bond Strength	2011	Condition B or D 2 grams for Au bonds 1 gram for Al bonds	15	5
Subgroup 3†				
Solderability	2003		15	10
Subgroup 4†				
Lead Fatigue	2004	Conditions B2		
Fine Leak	1014	Condition A, per para. 4.3.7 of this spec.		
Gross Leak	1014	Condition C, per para. 4.3.8 of this spec.	15	10

GROUP C

Subgroup 1‡				
Thermal Shock	1011	Condition B		
Temp. Cycle	1010	Condition C		
Moisture Resistance	1004	Omit Initial Cond. & step 7B		
Critical Electrical Parameters	5004	25°C, DC	15	10
Subgroup 2‡				
Mechanical Shock	2002	Condition B		
Vibration Variable Freq.	2007	Condition A		
Constant Acceleration	2001	Condition E		
Critical Electrical Parameters	5004	25°C, DC	15	10
Subgroup 3				
Salt Atmosphere	1009	Condition A Omit Initial Conditioning	15	10
Subgroup 4‡				
High Temp. Storage	1008	150°C, 1000 Hrs.		
Critical Electrical Parameters	5004	25°C, DC	10	7
Subgroup 5‡				
Operating Life Test	1005	125°C, 1000 Hrs. Minimum		
Critical Electrical Parameters		25°C, DC	10	7

†Visual and/or hermetic end points hence electrical or visual rejects may be used. Reference MIL-STD-883. Method 5005, Para. 3.4.

‡Electrical end points only.

4.5 Certification

The manufacturer shall include a certificate of compliance with each shipment of parts. This certificate shall indicate that all specified tests and requirements of this specification have been made or met, and that the lot of devices (identified by lot and/or batch number) are acceptable. The certificate shall bear the name and signature of the manufacturer's Quality Control representative, the date of acceptance or signing, and any pertinent notes as applicable.

4.6 Precap Lot Acceptance

After each precap inspection the lot of devices shall be sampled by quality control and inspected for the specified visual criteria. The sampling plan shall be:

40X criteria – 1.0% AQL
100X criteria – 1.0% AQL

5.0 PREPARATION FOR DELIVERY

5.1 Final Visual Shipping Inspection

Each lot of microcircuits and its associated documentation shall be sampled by Quality Control and visually inspected for the following:

a) Scratched, nicked or bent leads
b) Damaged header (packages)
c) All test data specified in section 4.0
d) Certificate of Compliance as specified in section 4.0
e) All other pertinent documentation required and specified by this specification.

5.2 Packing Requirements

Parts shall be packed in containers of the type, size, and kind commonly used which will ensure acceptance by common carriers and safe delivery at the destination and in accordance with MIL-M-55565, Level C. The containers shall be clearly marked with manufacturer's name or symbol. The manufacturer's FEDERAL SUPPLY CODE FOR MANUFACTURER (FSCM) shall be included if applicable.

5.3 Preservation and Package Identification

The package shall be marked with the following:

The country of origin if other and U.S.A.
Procuring activity parts number
Purchase order number
Material nomenclature
Quantity
Lot number
Date code

This information shall appear on the label or shall be directly marked on each container. Method is optional.

6.0 NOTES

6.1 Precap Visual Method 2010.1

The following precap criteria may be in conflict with the circuit design topology and construction techniques of some microcircuit manufacturers. Where such a conflict does exist, the inspection criteria listed herein may be waived. (Reference paragraph 3.0 of MIL-STD-883, Method 2010.1)

6.1.1 Preseal Visual Inspection, Test Condition A (Level IV)

6.1.1.1 Paragraph 3.1.6.3 is clarified as follows:

When the criteria of 3.1.6.3(b) is in conflict with 3.1.6.3(a), the criteria of 3.1.6.3(a) shall take precedence. (Note: This clarification is with respect to die symmetry only.)

6.1.1.2 Paragraphs 3.1.1.1(a) and 3.1.1.2(a) are clarified as follows:

"Any scratch or void in the metallization that leaves less than 50 (75) percent of the original metal width undisturbed" shall be rejected. When a bi-metallization system is used (e.g. Moly-Gold) the scratch or void must penetrate entirely through the gold and expose moly or oxide.

6.1.1.3 Paragraph 3.1.4.3(c) delete: (Applicable to gold ball bonds only) "Bonds in the fillet area (or the point where metallizations exits from the bonding pad) which reduces the major distance between the bond periphery and edge of fillet to less than 50 percent of the narrowest normal width of the interconnecting metallization."

6.1.2 Preseal Visual Inspection, Test Condition B (Levels I & III)

2

6.1.2.1 Paragraph 3.2.1.7(a) delete the 40 percent perimeter requirement. (Selected devices only)

6.1.2.2 Paragraph 3.2.4.3(a) substitute the following criteria: "Bonds placed so that the wire exiting from the bond appears to come closer than two wire diameters to another wire, bonding pad, or package land, after a distance of 10 mils from the die surface.

6.1.2.3 Paragraph 3.2.4.3(c) delete. "Bonds in the fillet area (or the point where metallizations exits from the bonding pad) which do not exhibit a line of undisturbed metallization visible between the periphery of the bond and at least one side of the fillet (or one side of the connecting stripe) when viewed from above."

6.1.3 Preseal Visual Inspection, Test Condition B (Level II)

The same comments of 6.1.2 are applicable here plus the following:

6.1.3.1 Paragraph 3.2.1.1(a) change to read as follows: "Scrathces or voids in metallization exposing oxide for more than 50 percent of the lead width or alternately, a scratch or void greater than 0.5 mils in length exposing oxide."

6.1.3.2 Paragraph 3.2.1.1(b) change to read as follows:

"Any scratch in the metallization over an oxide step which leaves less than 50 percent of the original metal width undisturbed."

6.1.3.3 Paragraph 3.2.1.2(b) change to read as follows:

"Any void in the metallization over an oxide step which leaves less than 50 percent of the remaining metal undisturbed."

6.1.3.4 Paragraph 3.2.3(d) delete.

"Any crack which exceeds 1.0 mil in length inside the scribe grid or scribe line that points toward active metallization or circuit area."

6.1.3.5 Paragraph 3.2.6.1(b) change to read as follows:

"Attached gold or silicon material that appears to bridge any two unpassivated metallization areas, two package leads, or any lead to package metallization."

6.2 Interconnections

Circuit intraconnections (metallization pattern) shall be designed so that no properly fabricated connection shall experience a current density greater than 5×10^5 amperes/cm2, including allowances for worst case conductor composition, normal production tolerances on design dimensions, and nominal thickness at critical areas such as contact windows.

6.3 Burn-in Method 1015

Condition D parallel excitation or Condition E ring oscillator burn-in circuits will be used. The requirement to return the device to 25°C room ambient temperature with bias still applied should be omitted. Indications are that for most saturated logic integrated circuits the high temperature bake after bias has been removed does not allow defective devices to recover and become good.

6.4 Salt Atmosphere Test, Method 1009.

Where package design consideration necessitate (such as .75" tip-to-tip metal flat packs), there may be a conformal coating applied prior to the salt atmosphere test.

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APPENDIX A

PROCESS CONTROL SYSTEM

INTEGRATED CIRCUITS PROCESS CONTROL

The integrated circuits industry has had over seven years experience in manufacturing and represents a high volume, mass production sector of electronics. We have overcome the usual new product growing pains and learned a great deal about process control systems from our experience. This article presents the philosophy and the basic elements of a process control system which has been found to be the most practical one for integrated circuits manufacturing. It should also be applicable to any semiconductor process which must produce devices for a high reliability market.

Integrated circuits were originally developed for the aerospace market and these are still the volume users. Hundreds of thousands of integrated circuits have already been delivered for use in Minuteman and Apollo alone. At the same time, the high volume commercial and consumer market for integrated circuits is developing very rapidly. Although most of the integrated circuits from a given manufacturer are built on a single production line, there are many different types and families: digital, linear, flip flops, choppers, gates, buffers, amplifiers, double epitaxial, monolithic, hybrids, TTL, DTL, ECL—hundreds of possibilities.

The key to success in today's integrated circuits business appears to be an efficient and effective process/product control system.

PRODUCT CONTROL VS. PROCESS CONTROL

Although it is not universally understood, *product* control is not the same as *process* control. They not only have different means, but their ends are entirely different. True, under the proper conditions, they can be interfaced and made more efficient, but let us first define the terminology.

PRODUCT CONTROL

Product control is the inspection and sorting of material (product) to cull unacceptable material from the acceptable. It is the age-old task of inspection, screening, detailing, or culling. With a state-of-the-art product such as integrated circuits, this inspection will usually take the form of go-no-go checking for various defects. The end result of product control is to eliminate from succeeding steps of the process that material which the preceding steps of the process have not constructed properly. The basic element of a product control system is where the inspection station is removing most of the product which was processed improperly by the preceding manufacturing operation.

It will be noted that this inspection has no control over the *process–only the product*. If the manufacturing operation should happen to start producing 100% bad product, the inspection station would remove this product, but would not correct the basic problem.

If the results of the inspection station, in the form of yield (or loss) data is monitored, analyzed, and compared to a standard set of circumstances, action can be taken to correct any degradation of the manufacturing operation. This feedback of information effects a degree of *process control* i.e., a control over the process which is not directly concerned with removing defective product.

The feedback of product control results for process control purposes helps achieve control over processes.

Product control in the manufacturing area is composed of:

1) Manufacturing Inspection
2) Quality Control Lot Acceptance Following Manufacturing Inspections.

1. Manufacturing Inspection

This inspection is performed by production personnel to go-no-go defect criteria. Even in this least severe level of product control, the closed loop feedback is utilized. The medium for this control is the product yield report and process control management system (PCMS), which has daily and weekly management, engineering, and quality control visibility.

Examples of these controls are diffusion, bar inspection, slice electrical probe, pre-encapsulation, hermetic seal, and electrical inspections performed in the manufacturing process.

2. Quality Control Lot Acceptance Following Manufacturing Inspection

In areas more critical in nature, the manufacturing inspection described in (1) is sometimes followed by Lot Acceptance. Here, decisions are made on lots of inspected product with regard to engineering specifications and predetermined quality levels.In this medium of control, feedback is two-fold: (1) Rejected lots are immediately identified for attention and manufacturing, engineering, and quality control are alerted as to whether process or inspection changes may have taken place, (2) PCMS shows trends of the quality control results and is distributed weekly to all levels of department management. Percentages are statistically compared to past averages and significant points are noted and corrective action implemented.

Examples of such control points are QC lot acceptance at epitaxial, bar inspection, pre-encapsulation, hermetic seal and electrical testing.

It should be pointed out that this "Product Control" concept is also an Inspection Control concept. The inspectors which are checked by a lot acceptance get instant feedback if the quality of their inspection degrades. Also, through the use of reject analysis and yield reporting, excessive losses are noted and thus both acceptable and rejectable material is monitored.

PROCESS CONTROL

Process control is the activity which controls the process itself and is not directly concerned with removing the defective product, but in preventing the manufacture of defective product which aids the subsequent product controls. It was noted previously that even in the case of pure *Product Control*, some process control can be effected by the proper use of feedback tools.

In integrated circuits manufacturing at Texas Instruments, *Process Control* is provided by the following:

1) Quality Control Surveillance Points During Manufacture
2) Engineering Evaluation of Manufacturing Process
3) Manufacturing Controls
4) Failure Analysis of Discrepant Devices

1. Quality Control Surveillance Points During Manufacture

Process Controls examines the manufacturing process to point out the problem areas. For example: If thirty operators are bonding, we inspect products from all thirty operators and point out the worst three bonders to the manufacturing supervisor daily. This concentrates the supervisor's effort on the quality problem operator each day. This type of control is called operator control.

A control where the worst machine or machines are pinpointed for corrective action by repair and maintenance personnel is called machine control. Examples of such controls are: $\bar{X}$–R chart control of diffusion furnaces, visual surveillance of product from each mounting operator, bond strength tests on bonded Integrated Circuits, hermetic seal checks on lid welders.

2. Engineering Evaluation of Manufacturing Process

Engineering maintains sample or pilot analysis at several critical points of manufacture. Here, electrical parameters are measured on a lot by lot basis to maintain control at that point. An example of this is the analysis performed in diffusion to control this portion of the manufacturing process.

3. Manufacturing Controls

Regular controls by manufacturing for operator performance, line balance, inventory control, and line comparison enhance the quality of the device.

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4. Failure Analysis of Discrepant Devices

Another portion of the feedback loop is through the analysis of failed devices. Regular life testing with failure analysis of test failures is performed on representative device series. In addition, device failures from selected points in the process are given to the failure analysis lab on a routine basis. By this media, *Product* and *Process Controls* can be adjusted to correct mechanisms which might not be discovered until actual application of the devices.

An analysis of the complete QC process control system is shown in the attached flow charts. These charts describe the QC Process Control System and a brief description of each control point.

The PCMS is a computerized report of the control points on a weekly basis. These control points have their trends analyzed by comparing the current percentage to past averages and calculating significant differences. Points analyzed as significantly different are further detailed as to exact defect descriptions. These points are then analyzed and corrective action developed as necessary. This weekly analysis is circulated to all levels of department management. This reporting system plus the immediate feedback which occurs "on-line" provides an effective follow-up scheme.

It should be noted that the details of this system are flexible and not essential to the basic philosophy of a composite control system. As experience is gained in the various inspection areas and as process improvements are made, it will be found advantageous to suitably modify the system to keep pace with these changes. As time passes, sample sizes will be changed; inspection points will be added and deleted; defect criteria will be made less subjective, and new defect criteria will be added to the inspection procedure. But none of these affect the basic philosophy of the product/process control system.

ADVANTAGES OF THE SYSTEM

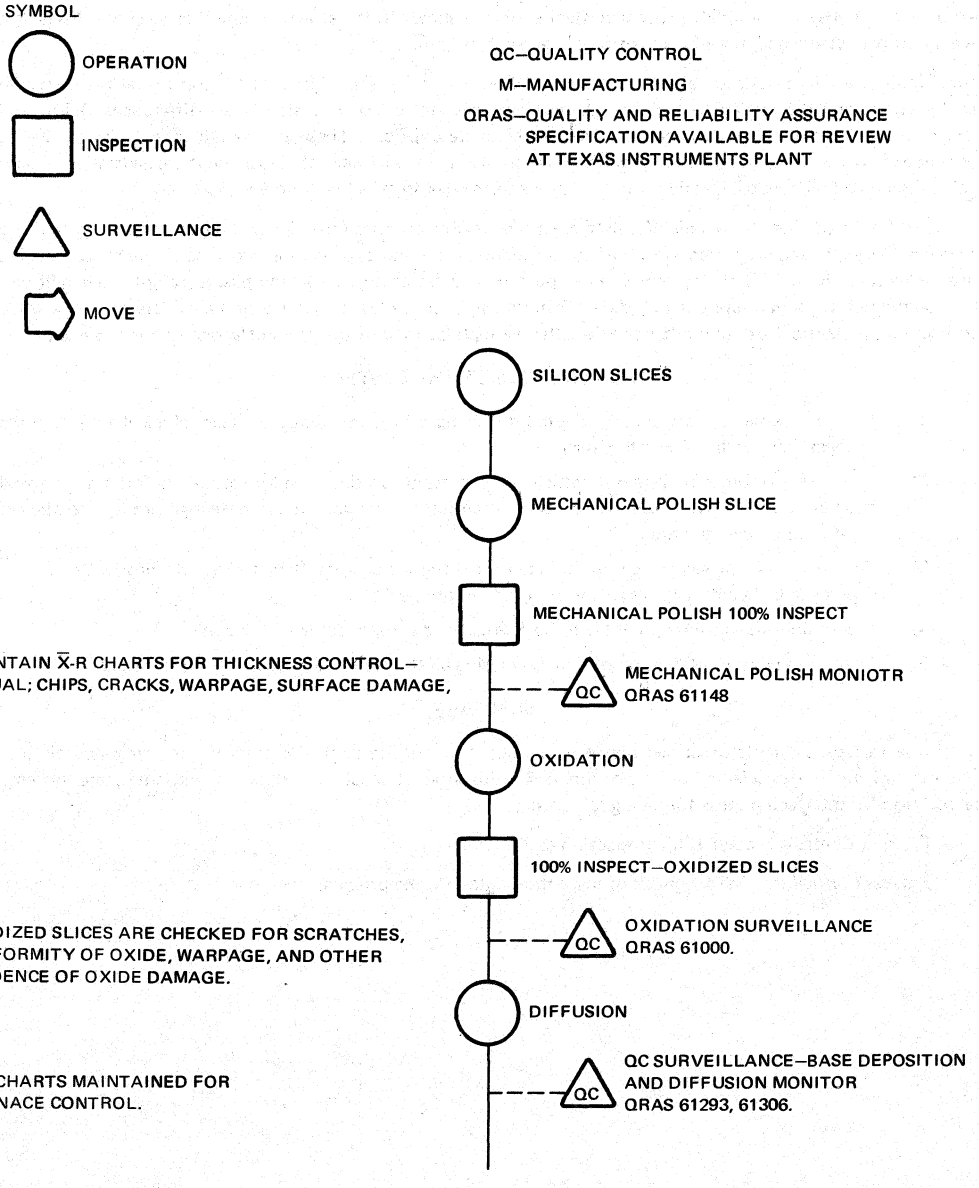
1) It is a flexible system easily adapted to changes brought about by technological improvements or by changes dictated by the system itself.
2) It is a cost optimized system in which the process or product can be stopped before unwarranted labor is expended. In addition, the system calls attention to the reason for defective product so that corrective action can be implemented.
3) The same general system can be utilized for different degrees of maturity of a product and for different degrees of criticality with regard to product requirements.
4) It combines the advantages of both the product and process control concepts.
5) There is maximum utilization of data by closing all the feedback loops with corrective action.

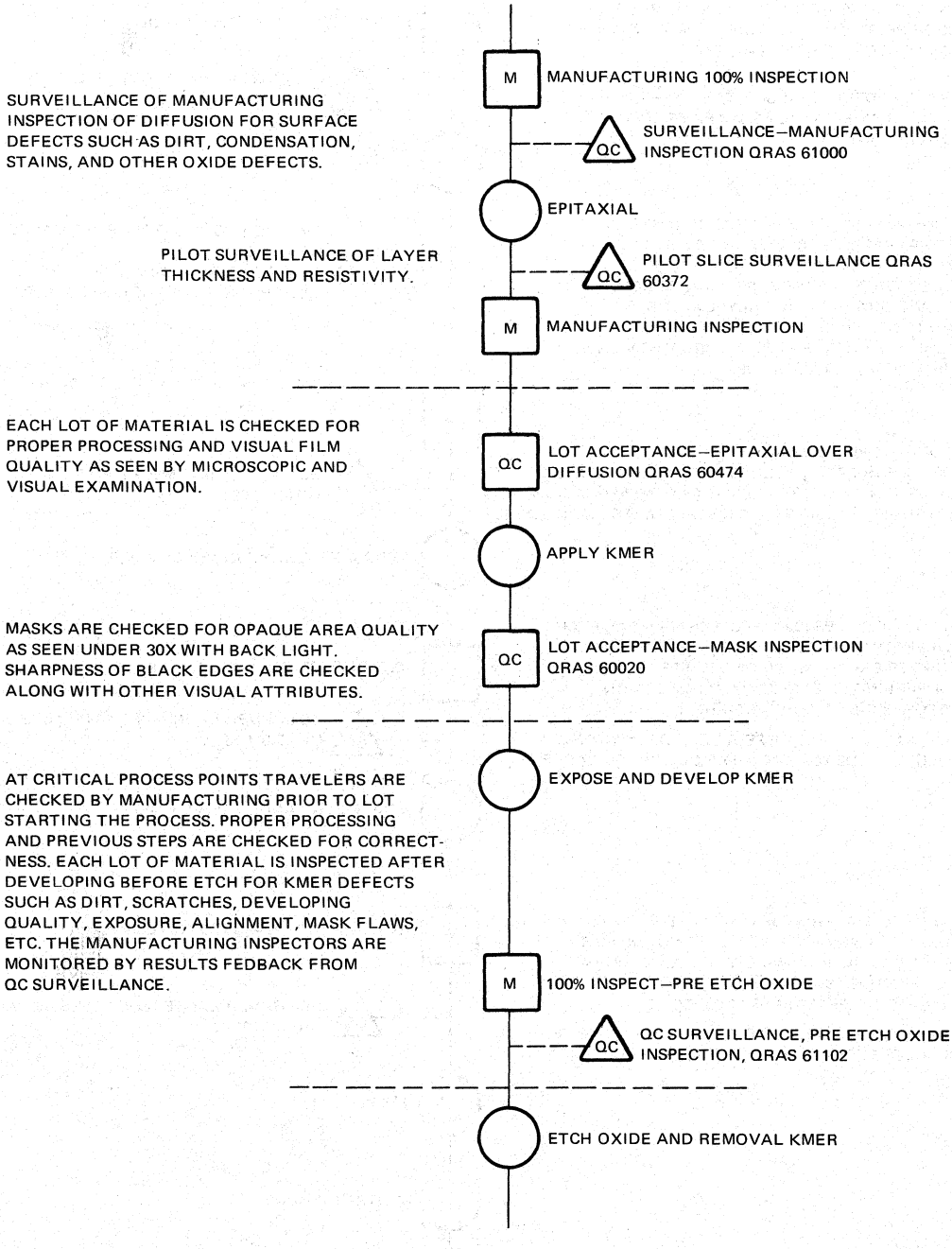
SUMMARY

Using the various elements described above to develop a composite control system for an integrated circuits process results in maximizing the efficiency of inspection and utilization of inspection data. In particular, the system offers a practical solution for interfacing these following features:

Product Control through 100% inspection and sorting.

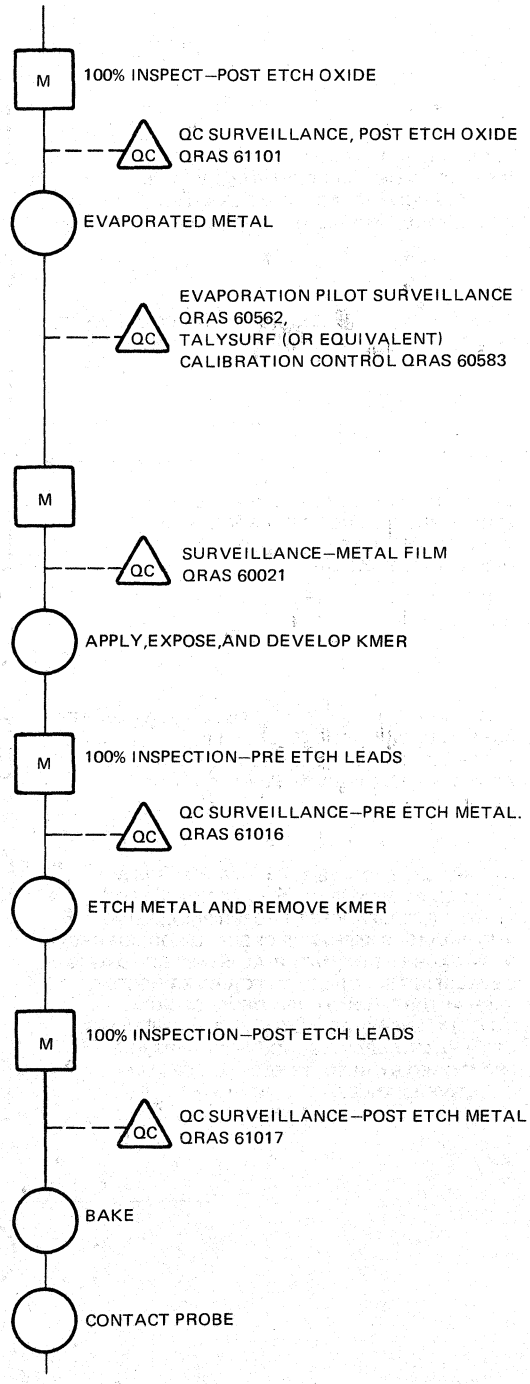
Process Control through feedback of inspection data into the process.


SYMBOL
OPERATION
INSPECTION
SURVEILLANCE
MOVE
QC–QUALITY CONTROL
M–MANUFACTURING
QRAS–QUALITY AND RELIABILITY ASSURANCE SPECIFICATION AVAILABLE FOR REVIEW AT TEXAS INSTRUMENTS PLANT
SILICON SLICES
MECHANICAL POLISH SLICE
MECHANICAL POLISH 100% INSPECT
MAINTAIN X̄-R CHARTS FOR THICKNESS CONTROL–VISUAL; CHIPS, CRACKS, WARPAGE, SURFACE DAMAGE, ETC.
QC
MECHANICAL POLISH MONIOTR QRAS 61148
OXIDATION
100% INSPECT–OXIDIZED SLICES
OXIDIZED SLICES ARE CHECKED FOR SCRATCHES, UNIFORMITY OF OXIDE, WARPAGE, AND OTHER EVIDENCE OF OXIDE DAMAGE.
QC
OXIDATION SURVEILLANCE QRAS 61000.
DIFFUSION
X̄-R CHARTS MAINTAINED FOR FURNACE CONTROL.
QC
QC SURVEILLANCE–BASE DEPOSITION AND DIFFUSION MONITOR QRAS 61293, 61306.


M
MANUFACTURING 100% INSPECTION
SURVEILLANCE OF MANUFACTURING INSPECTION OF DIFFUSION FOR SURFACE DEFECTS SUCH AS DIRT, CONDENSATION, STAINS, AND OTHER OXIDE DEFECTS.
QC
SURVEILLANCE–MANUFACTURING INSPECTION QRAS 61000
EPITAXIAL
PILOT SURVEILLANCE OF LAYER THICKNESS AND RESISTIVITY.
QC
PILOT SLICE SURVEILLANCE QRAS 60372
M
MANUFACTURING INSPECTION
EACH LOT OF MATERIAL IS CHECKED FOR PROPER PROCESSING AND VISUAL FILM QUALITY AS SEEN BY MICROSCOPIC AND VISUAL EXAMINATION.
QC
LOT ACCEPTANCE–EPITAXIAL OVER DIFFUSION QRAS 60474
APPLY KMER
MASKS ARE CHECKED FOR OPAQUE AREA QUALITY AS SEEN UNDER 30X WITH BACK LIGHT. SHARPNESS OF BLACK EDGES ARE CHECKED ALONG WITH OTHER VISUAL ATTRIBUTES.
QC
LOT ACCEPTANCE–MASK INSPECTION QRAS 60020
EXPOSE AND DEVELOP KMER
AT CRITICAL PROCESS POINTS TRAVELERS ARE CHECKED BY MANUFACTURING PRIOR TO LOT STARTING THE PROCESS. PROPER PROCESSING AND PREVIOUS STEPS ARE CHECKED FOR CORRECTNESS. EACH LOT OF MATERIAL IS INSPECTED AFTER DEVELOPING BEFORE ETCH FOR KMER DEFECTS SUCH AS DIRT, SCRATCHES, DEVELOPING QUALITY, EXPOSURE, ALIGNMENT, MASK FLAWS, ETC. THE MANUFACTURING INSPECTORS ARE MONITORED BY RESULTS FEDBACK FROM QC SURVEILLANCE.
M
100% INSPECT–PRE ETCH OXIDE
QC
QC SURVEILLANCE, PRE ETCH OXIDE INSPECTION, QRAS 61102
ETCH OXIDE AND REMOVAL KMER

EACH LOT OF MATERIAL IS INSPECTED BY MANUFACTURING AFTER OXIDE REMOVAL FOR OXIDE DEFECTS SUCH AS UNDERCUT, ALIGNMENT, INCOMPLETE OXIDE REMOVAL, DIRT, ETC.

THE MANUFACTURING INSPECTORS ARE MONITORED BY RESULTS FEDBACK FROM THE QC SURVEILLANCE.



2

THIS CHECK IS A SURVEILLANCE OF TESTING EVAPORATION PILOT SLICES TO DETERMINE METAL THICKNESS. PILOTS ARE DOUBLE CHECKED TWICE PER WEEK PER SHIFT FROM EACH EVAPORATOR. THE TALYSURF (OR EQUIVALENT) WHICH MEASURES METAL FILM THICKNESS IS CHECKED FOR CALIBRATION ONCE PER SHIFT USING STANDARDS.

SAMPLES ARE PULLED ONCE PER EVAPORATOR PER SHIFT FOR EFFECTIVENESS OF MANUFACTURING 100% INSPECTION. DEFECTS SUCH AS CONTAMINATION, SPLATTERING, FOREIGN PARTICLES, ETC, ARE MONITORED

EACH LOT OF SLICES IS INSPECTED AT METAL ETCH FOR DEFECTS SUCH AS MISALIGNMENT, OVER AND UNDER EXPOSURE, WRONG PATTERN, RESIST PEELING, ETC. THIS KMER INSPECTION IS PERFORMED BY MANUFACTURING.

THE MANUFACTURING INSPECTORS ARE MONITORED BY RESULTS FEDBACK FROM THE QC SURVEILLANCE.

EACH LOT OF MATERIAL IS INSPECTED BY MANUFACTURING AFTER METAL REMOVAL FOR DEFECTS SUCH AS INCOMPLETE METAL REMOVAL, LEADS TOUCHING SILICON OUTSIDE CONTACTS, MISALIGNMENT, PEELING LEADS, ETC.

THE MANUFACTURING INSPECTORS ARE MONITORED BY RESULTS FEDBACK FROM THE QC SURVEILLANCE.

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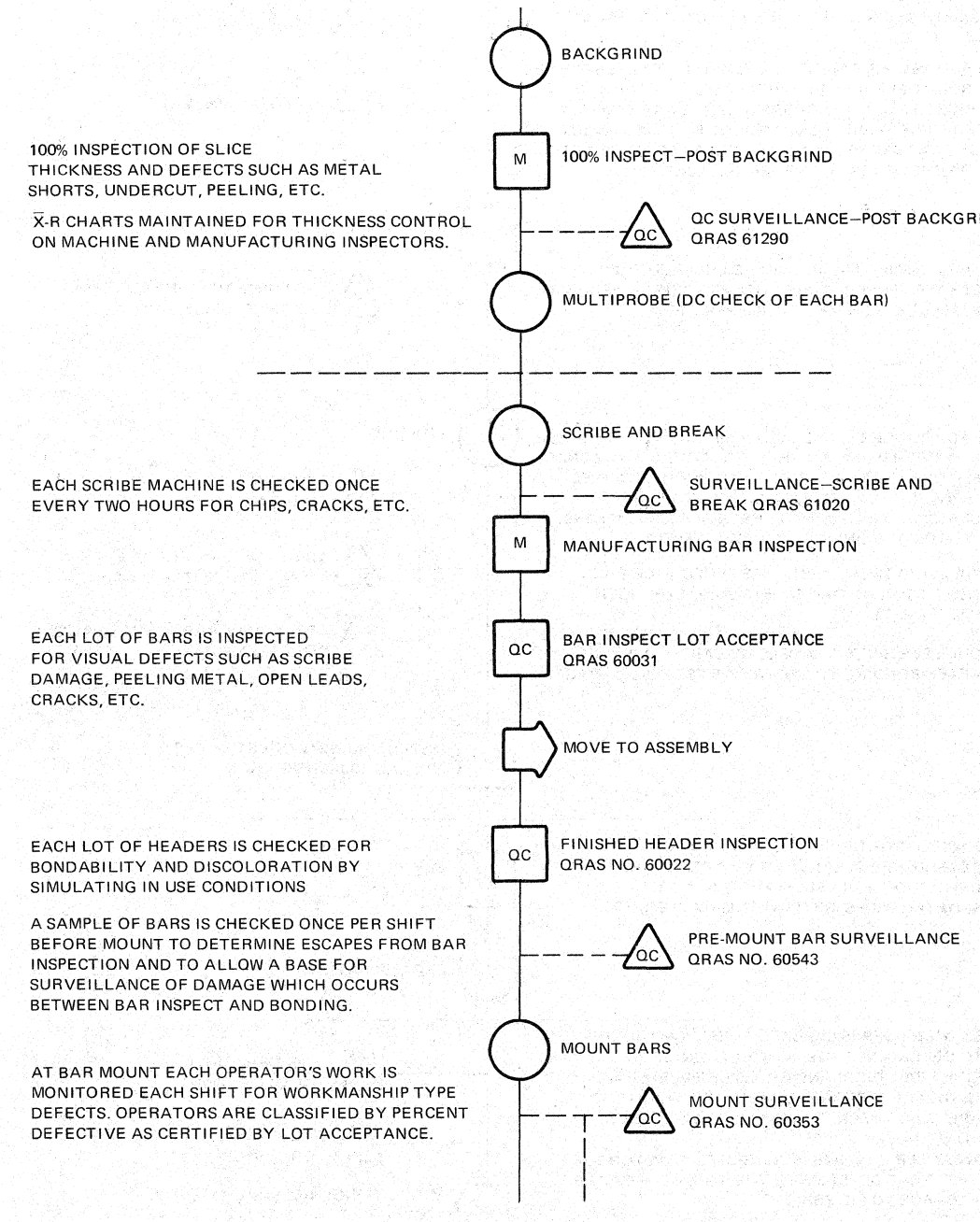
BACKGRIND
M
100% INSPECT–POST BACKGRIND
100% INSPECTION OF SLICE THICKNESS AND DEFECTS SUCH AS METAL SHORTS, UNDERCUT, PEELING, ETC.
X̄-R CHARTS MAINTAINED FOR THICKNESS CONTROL ON MACHINE AND MANUFACTURING INSPECTORS.
QC
QC SURVEILLANCE–POST BACKGRIND QRAS 61290
MULTIPROBE (DC CHECK OF EACH BAR)
SCRIBE AND BREAK
EACH SCRIBE MACHINE IS CHECKED ONCE EVERY TWO HOURS FOR CHIPS, CRACKS, ETC.
QC
SURVEILLANCE–SCRIBE AND BREAK QRAS 61020
M
MANUFACTURING BAR INSPECTION
EACH LOT OF BARS IS INSPECTED FOR VISUAL DEFECTS SUCH AS SCRIBE DAMAGE, PEELING METAL, OPEN LEADS, CRACKS, ETC.
QC
BAR INSPECT LOT ACCEPTANCE QRAS 60031
MOVE TO ASSEMBLY
EACH LOT OF HEADERS IS CHECKED FOR BONDABILITY AND DISCOLORATION BY SIMULATING IN USE CONDITIONS
QC
FINISHED HEADER INSPECTION QRAS NO. 60022
A SAMPLE OF BARS IS CHECKED ONCE PER SHIFT BEFORE MOUNT TO DETERMINE ESCAPES FROM BAR INSPECTION AND TO ALLOW A BASE FOR SURVEILLANCE OF DAMAGE WHICH OCCURS BETWEEN BAR INSPECT AND BONDING.
QC
PRE-MOUNT BAR SURVEILLANCE QRAS NO. 60543
MOUNT BARS
AT BAR MOUNT EACH OPERATOR'S WORK IS MONITORED EACH SHIFT FOR WORKMANSHIP TYPE DEFECTS. OPERATORS ARE CLASSIFIED BY PERCENT DEFECTIVE AS CERTIFIED BY LOT ACCEPTANCE.
QC
MOUNT SURVEILLANCE QRAS NO. 60353

THE ALLOY MACHINES ARE CHECKED TWICE PER SHIFT FOR DEFECTS SUCH AS INCOMPLETE ALLOY, BAR ORIENTATION, SCRATCHES, ALLOY MATERIAL ON THE BAR, ETC.

EACH NEW FRIT MIXTURE HAS A USE TEST PERFORMED FROM IT BEFORE BEING RELEASED TO PRODUCTION. ONCE PER DAY A MICROSTRUCTURE ANALYSIS IS PERFORMED FROM EACH MOUNT FURNACE. TWICE PER SHIFT A SAMPLE FROM EACH FURNACE IS SUBJECTED TO TORQUE TEST FOR FURNACE CONTROL.

QC — ALLOY MOUNT QRAS 60413

QC — FRIT CONTROL QRAS NO. 60824

M — POST MOUNT INSPECTION

THE BONDING MACHINES ARE CHECKED FOR SUBSTRATE TEMPERATURE ONCE PER SHIFT. CAPILLARY PRESSURE IS CHECKED ONCE PER WEEK.

QC — BONDING MACHINE CONTROL QRAS NO. 60494

BONDING

EACH BONDER IS CHECKED A MINIMUM OF TWICE PER SHIFT FOR WORKMANSHIP DEFECTS SUCH AS BONDS 50% OFF THE PAD, TIGHT WIRES, SHORTED WIRES, IMPROPER BOND SIZE, ETC. OPERATORS ARE CLASSIFIED DAILY INTO THREE CLASSIFICATIONS; CERTIFIED, MONITOR AND 100% INSPECT.

PULL AND SHEAR TESTS ARE PERFORMED EACH SHIFT TO MONITOR PROCESS BOND STRENGTH VARIABILITY.

ONCE PER SHIFT A SAMPLE OF BARS IS CHECKED AFTER BONDING TO DETERMINE PROCESS DAMAGE.

QC — BONDING SURVEILLANCE QRAS NO. 60033

QC — BOND STRENGTH TESTS QRAS NOS. 60034 & 60543

QC — POST BOND BAR SURVEILLANCE QRAS NO. 60543

M — INSPECTING NETWORKS PRE-CAP 40X AND 100X INSPECTION.

EACH LOT OF DEVICES IS SAMPLED TO DETERMINE ACCEPTABILITY TO STANDARD DEFECT CRITERIA SUCH AS OPEN WIRES, SHORTED WIRES, EXTRANEOUS MATTER, ETC.

QC — PRE CAP LOT ACCEPTANCE QRAS NO. 60035

ENCAPSULATION

EACH WELDER IS CHECKED EVERY TWO HOURS TO DETERMINE PROPER OPERATION. BOTH FINE LEAK TESTS AND GROSS (BUBBLE) LEAK TESTS ARE PERFORMED. MOISTURE MONITORS ARE ALSO CHECKED AND VISUAL WELD QUALITY MONITORED.
A SAMPLE OF UNITS IS SUBJECTED TO A TORQUE TEST THAT DETERMINES THE STRENGTH OF THE PACKAGE TO LID SEAL.

QC — WELDER CONTROL QRAS NO. 60036

QC — C-DIP TORQUE TEST QRAS 61019

MOVE TO HIGH RELIABILITY FINAL TEST AREA.

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Linear Circuits

INDEX

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General Purpose Operational Amplifiers	SN52702A			N		L	S	3-18
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*For outline drawings of all packages, see Section 1.

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FUNCTION	OPERATING TEMPERATURE RANGE −55°C to 125°C	OPERATING TEMPERATURE RANGE 0°C to 70°C	PACKAGES* Dual-In-Line		Plug-In		Flat	SEC.-PAGE
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*For outline drawings of all packages, see Section 1.

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OPERATIONAL AMPLIFIER SELECTION GUIDE

Series 52

TYPE	SN52702	SN52709	SN52741	SN52747	SN52748	SN52770	SN52771	SN52558	SN52101A	SN52107	
FEATURES	Wide BW, General Purpose	General Purpose	Internally Compensated Gen. Pur.	Dual SN52741	Extended BW, Gen. Pur.	Super β	Super β	Dual 741 in 8-pin Package	Precision Op Amp	Internally Compensated	UNIT
Input Offset Voltage, Max	5	5	5	5	5	4	4	5	2	2	mV
Input Offset Current, Max	500	200	200	200	200	2	2	200	10	10	nA
Temperature Coefficient of Input Offset Voltage, Typ	10	6	7	7	7	10	10	7	3	3	μV/°C
Input Bias Current, Max	10,000	500	500	500	500	15	15	500	75	75	nA
Voltage Amplification, Min	1.4	25	50	50	50	50	50	50	50	50	V/mV
Slew Rate at Unity Gain, Typ	1.7	0.3	0.5	0.5	0.5	2.5	2.5	0.5	0.5	0.5	V/μs
Unity-Gain Bandwidth, Typ	30	5	1	1	1	1.3	1.3	1	1	1	MHz
Min Supply Voltage	+6, −3	±9	±5	±5	±5	±3	±3	±5	±3	±3	V
Max Supply Voltage	+14, −7	±18	±22	±22	±22	±22	±22	±22	±22	±22	V
Input Voltage Range, Min	0.5 to −4	±8	±12	±12	±12	±12	±12	±12	±15	±15	V
Differential Input Voltage Rating	±5	±5	±30	±30	±30	±30	±30	±30	±30	±30	V
Internal Compensation	No	No	Yes	Yes	No	No	Yes	Yes	No	Yes	
Offset Adjust	No	No	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes	
Input Protection	No	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	
Output Protection	No	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	

3

Series 72

TYPE	SN72702	SN72709	SN72741	SN72747	SN72748	SN72770	SN72771	SN72558	SN72301A	SN72307	
FEATURES	Wide BW, General Purpose	General Purpose	Internally Compensated, Gen. Pur.	Dual SN72741	Extended BW, Gen. Pur.	Super β	Super β	Dual 741 in 8-pin Package	Precision Op Amp	Internally Compensated	UNIT
Input Offset Voltage, Max	5	7.5	6	6	6	10	10	6	7.5	7.5	mV
Input Offset Current, Max	500	500	200	200	200	10	10	200	50	50	nA
Temperature Coefficient of Input Offset Voltage, Typ	5	6	7	7	7	10	10	7	6	6	μV/°C
Input Bias Current, Max	15,000	1500	500	500	500	30	30	500	250	250	nA
Voltage Amplification, Min	1	15	20	20	20	35	35	20	25	25	V/mV
Slew Rate at Unity Gain, Typ	1.7	0.3	0.5	0.5	0.5	2.5	2.5	0.5	0.5	0.5	V/μs
Unity-Gain Bandwidth, Typ	30	5	1	1	1	1.3	1.3	1	1	1	MHz
Min Supply Voltage	+6, −3	±9	±5	±5	±5	±3	±3	±5	±3	±3	V
Max Supply Voltage	+14, −7	±18	±18	±18	±18	±18	±18	±18	±18	±18	V
Input Voltage Range, Min	0.5 to −4	±8	±12	±12	±12	±11	±11	±12	±12	±12	V
Differential Input Voltage Rating	±5	±5	±30	±30	±30	±30	±30	±30	±30	±30	V
Internal Compensation	No	No	Yes	Yes	No	No	Yes	Yes	No	Yes	
Offset Adjust	No	No	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes	
Input Protection	No	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	
Output Protection	No	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	

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CIRCUIT TYPES SN52101A, SN72301A
HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

- Low Input Currents
- Low Input Offset Parameters
- Frequency and Transient Response Characteristics Adjustable
- Short-Circuit Protection
- Offset-Voltage Null Capability
- Designed to be Interchangeable with National Semiconductor LM101A and LM301A
- No Latch-Up
- Large Common-Mode and Differential Voltage Ranges
- Same Pin Assignments as SN52709 and SN72709

description

The SN52101A and SN727301A are high-performance operational amplifiers, featuring very low input bias current and input offset voltage and current to improve the accuracy of high-impedance circuits using these devices.

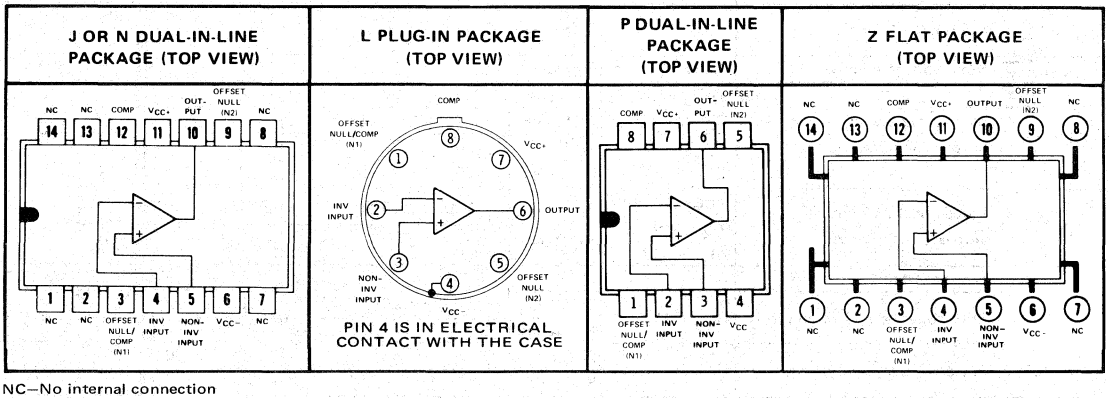
The high common-mode input voltage range and the absence of latch-up make the SN52101A and SN72301A ideal for voltage-follower applications. The devices are protected to withstand short-circuits at the output. The external compensation of the SN52101A and the SN72301A allows the changing of the frequency response (when the closed-loop gain is greater than unity) for applications requiring wider bandwidth or higher slew rate.

A potentiometer may be connected between the offset-null inputs (N1 and N2), as shown in Figure 8, to null out the offset voltage.

The SN52101A is characterized for operation over the full military temperature range of −55°C to 125°C; the SN72301A is characterized for operation from 0°C to 70°C.

3

terminal assignments



NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN52101A	SN72301A	UNIT
Supply voltage V_{CC+} (see Note 1)		22	18	V
Supply voltage V_{CC-} (see Note 1)		−22	−18	V
Differential input voltage (see Note 2)		±30	±30	V
Input voltage (either input, see Notes 1 and 3)		±15	±15	V
Voltage between either offset null terminal (N1/N2) and V_{CC-}		−0.5 to 2	−0.5 to 2	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	
Continuous total power dissipation at (or below) 55°C free-air temperature (see Note 5)		500	500	mW
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J, L, or Z Package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N or P Package	260	260	°C

NOTES:
1. All voltage values, unless otherwise noted, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or either power supply. For the SN52101A only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.
5. For operation above 55°C free-air temperature, refer to Dissipation Derating Curve, Figure 1.

voltages specified

Throughout this data sheet, supply voltages are specified either as a range or as a specific value. A positive voltage within the specified range (or of the specified value) is applied to V_{CC+}, and an equal negative voltage is applied to V_{CC-}.

electrical characteristics at specified free-air temperature (see note 6)

PARAMETER		TEST CONDITIONS†		SN52101A			SN72301A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	R_S = 50 kΩ	25°C		0.6	2		2.0	7.5	mV
			Full range			3			10	
α_{VIO}	Average temperature coefficient of input offset voltage		Full range		3	15		6	30	μV/°C
I_{IO}	Input offset current		25°C		1.5	10		3	50	nA
			Full range			20			70	
α_{IIO}	Average temperature coefficient of input offset current	T_A = −55°C to 25°C			0.02	0.2				nA/°C
		T_A = 25°C to 125°C			0.01	0.1				
		T_A = 0°C to 25°C						0.02	0.6	
		T_A = 25°C to 70°C						0.01	0.3	
I_{IB}	Input bias current		25°C		30	75		70	250	nA
			Full range			100			300	
V_I	Input voltage range	See Note 7	Full range	±15			±12			V
V_{OPP}	Maximum peak-to-peak output voltage swing	$V_{CC\pm}$ = ±15 V, R_L = 10 kΩ	25°C	24	28		24	28		V
			Full range	24			24			
		$V_{CC\pm}$ = ±15 V, R_L = 2 kΩ	25°C	20	26		20	26		
			Full range	20			20			
A_{VD}	Large-signal differential voltage amplification	$V_{CC\pm}$ = ±15 V, V_O = ±10 V, $R_L \geq$ 2 kΩ	25°C	50,000	200,000		25,000	200,000		
			Full range	25,000			15,000			
r_i	Input resistance		25°C	1.5	4		0.5	2		MΩ
CMRR	Common-mode rejection ratio	R_S = 50 kΩ	25°C	80	98		70	90		dB
			Full range	80			70			
$\Delta V_{CC}/\Delta V_{IO}$	Power supply rejection ratio	R_S = 50 kΩ	25°C	80	98		70	96		dB
			Full range	80			70			
I_{CC}	Supply current	No load, No signal, See Note 7	25°C		1.8	3		1.8	3	mA
			125°C		1.2	2.5				

†All characteristics are specified under open-loop operation. Full range for SN52101A is −55°C to 125°C and for SN72301A is 0°C to 70°C.

NOTES: 6. Unless otherwise noted, $V_{CC\pm}$ = ±5 V to ±20 V for SN52101A and $V_{CC\pm}$ = ±5 V to ±15 V for SN72301A. All typical values are at $V_{CC\pm}$ = ±15 V.
7. For SN52101A, $V_{CC\pm}$ = ±20 V. For SN72301A, $V_{CC\pm}$ = ±15 V.

For ordering instructions and mechanical data, see the SN52741/SN72741 data sheet dated November 1970.

TEXAS INSTRUMENTS
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DEFINITION OF TERMS

Input Offset Voltage (V_{IO}) The d-c voltage which must be applied between the input terminals to force the quiescent d-c output voltage to zero. The input offset voltage may also be defined for the case where two equal resistances (R_S) are inserted in series with the input leads.

Average Temperature Coefficient of Input Offset Voltage (α_{VIO}) The ratio of the change in input offset voltage to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{VIO} = \left| \frac{(V_{IO} @ T_{A(1)}) - (V_{IO} @ T_{A(2)})}{T_{A(1)} - T_{A(2)}} \right|$$ where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

Input Offset Current (I_{IO}) The difference between the currents into the two input terminals with the output at zero volts.

Average Temperature Coefficient Of Input Offset Current (α_{IIO}) The ratio of the change in input offset current to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{IIO} = \left| \frac{(I_{IO} @ T_{A(1)}) - (I_{IO} @ T_{A(2)})}{T_{A(1)} - T_{A(2)}} \right|$$ where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

Input Bias Current (I_{IB}) The average of the currents into the two input terminals with the output at zero volts.

Input Voltage Range (V_I) The range of voltage which, if exceeded at either input terminal, will cause the amplifier to cease functioning properly.

Maximum Peak-to-Peak Output Voltage Swing (V_{OPP}) The maximum peak-to-peak output voltage which can be obtained without waveform clipping when the quiescent d-c output voltage is zero.

Large-Signal Differential Voltage Amplification (A_{VD}) The ratio of the peak-to-peak output voltage swing to the change in differential input voltage required to drive the output.

Input Resistance (r_i) The resistance between the input terminals with either input grounded.

Common-Mode Rejection Ratio (CMRR) The ratio of differential voltage amplification to common-mode voltage amplification. This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.

Supply Voltage Rejection Ratio ($\Delta V_{CC}/\Delta V_{IO}$) The ratio of the change in power supply voltages to the change in input offset voltage. For these devices, both supply voltages are varied symmetrically.

THERMAL INFORMATION

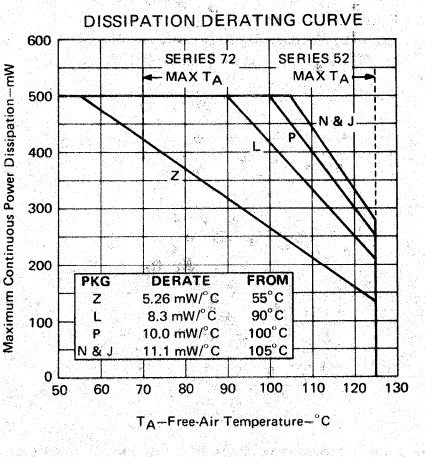


FIGURE 1

TYPICAL CHARACTERISTICS

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

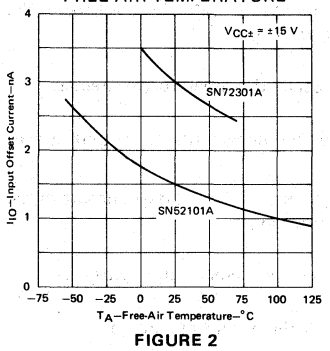


FIGURE 2

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

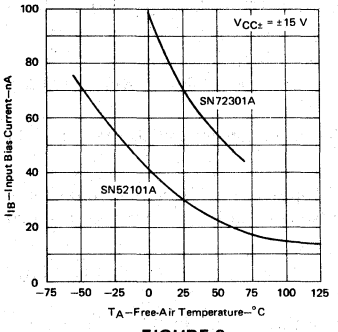


FIGURE 3

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE (WITH
SINGLE-POLE COMPENSATION)
vs FREQUENCY

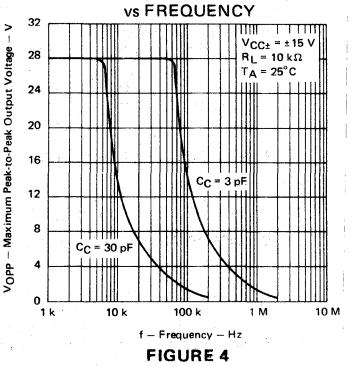


FIGURE 4

OPEN-LOOP LARGE-SIGNAL
DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

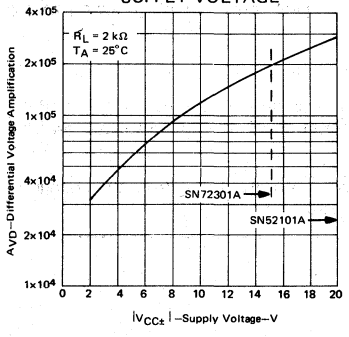


FIGURE 5

OPEN-LOOP LARGE-SIGNAL
DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
FREQUENCY

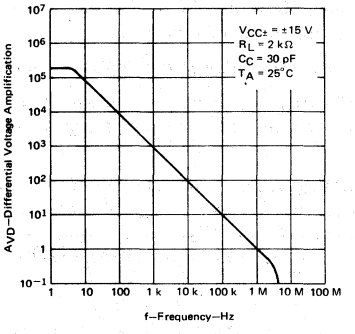


FIGURE 6

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

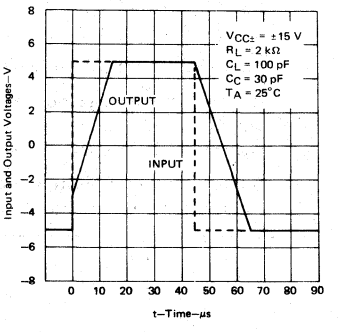
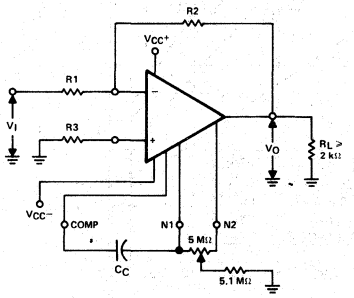


FIGURE 7

TYPICAL APPLICATION DATA



$$\frac{V_O}{V_I} = -\frac{R2}{R1}$$

$$C_C \geqslant \frac{R1 \cdot 30\ pF}{R1+R2}$$

$$R3 = \frac{R1 \cdot R2}{R1+R2}$$

FIGURE 8 – INVERTING CIRCUIT WITH ADJUSTABLE GAIN, SINGLE-POLE COMPENSATION, AND OFFSET ADJUSTMENT

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CIRCUIT TYPES SN52107, SN72307
HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

- Low Input Currents
- No Frequency Compensation Required
- Offset-Voltage Null Capability
- Low Input Offset Parameters
- Designed to be Interchangeable with National Semiconductor LM107 and LM307
- Short-Circuit Protection
- No Latch-Up
- Large Common-Mode and Differential Voltage Ranges
- Same Pin Assignments as SN52741 and SN72741

description

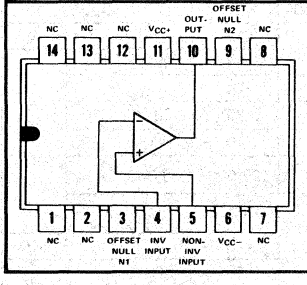
The SN52107 and SN72307 are high-performance operational amplifiers, featuring very low input bias current and input offset voltage and current to improve the accuracy of high-impedance circuits using these devices.

The high common-mode input voltage range and the absence of latch-up make the SN52107 and SN72307 ideal for voltage-follower applications. The devices are short-circuit protected and the internal frequency compensation ensures stability without external components. A low-value potentiometer may be connected between the offset-null inputs, as shown in Figure 2, to null out the offset voltage.

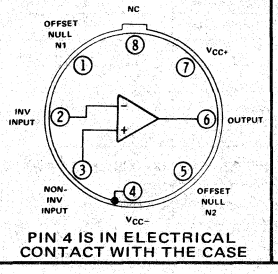
The SN52107 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN72307 is characterized for operation from 0°C to 70°C.

terminal assignments

J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)

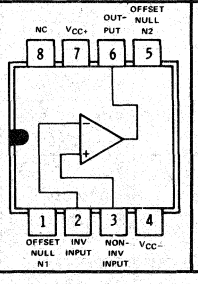


L PLUG-IN PACKAGE (TOP VIEW)

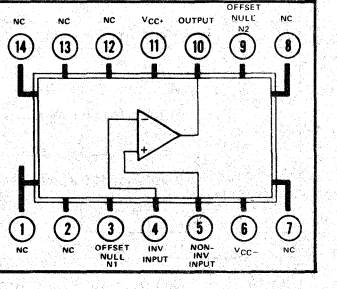


PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE

P DUAL-IN-LINE PACKAGE (TOP VIEW)



Z FLAT PACKAGE (TOP VIEW)



NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN52107	SN72307	UNIT
Supply voltage V_{CC+} (see Note 1)		22	18	V
Supply voltage V_{CC-} (see Note 1)		−22	−18	V
Differential input voltage (see Note 2)		±30	±30	V
Input voltage (either input, see Notes 1 and 3)		±15	±15	V
Voltage between either offset null terminal (N1/N2) and V_{CC-}		±0.5	±0.5	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	
Continuous total dissipation at (or below) 55°C free-air temperature (see Note 5)		500	500	mW
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J, L, or Z Package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N or P Package	260	260	°C

NOTES:
1. All voltage values, unless otherwise noted, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or either power supply. For the SN52107 only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.
5. For operation above 55°C free-air temperature, refer to Dissipation Derating Curve, Figure 1.

voltages specified

Throughout this data sheet, supply voltages are specified either as a range or as a specific value. A positive voltage within the specified range (or of the specified value) is applied to V_{CC+}, and an equal negative voltage is applied to V_{CC-}.

electrical characteristics at specified free-air temperature (see note 6)

PARAMETER		TEST CONDITIONS†		SN52107			SN72307			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	R_S = 50 kΩ	25°C		0.6	2		2	7.5	mV
			Full range			3			10	
α_{VIO}	Average temperature coefficient of input offset voltage		Full range		3	15		6	30	μV/°C
I_{IO}	Input offset current		25°C		1.5	10		3	50	nA
			Full range			20			70	
α_{IIO}	Average temperature coefficient of input offset current	T_A = −55°C to 25°C			0.02	0.2				nA/°C
		T_A = 25°C to 125°C			0.01	0.1				
		T_A = 0°C to 25°C						0.02	0.6	
		T_A = 25°C to 70°C						0.01	0.3	
I_{IB}	Input bias current		25°C		30	75		70	250	nA
			Full range			100			300	
V_I	Input voltage range	See Note 7	Full range	±15			±12			V
V_{OPP}	Maximum peak-to-peak output voltage swing	$V_{CC\pm}$ = ±15 V, R_L = 10 kΩ	25°C	24	28		24	28		V
			Full range	24			24			
		$V_{CC\pm}$ = ±15 V, R_L = 2 kΩ	25°C	20	26		20	26		
			Full range	20			20			
A_{VD}	Large-signal differential voltage amplification	$V_{CC\pm}$ = ±15 V, V_O = ±10 V, $R_L \geq$ 2 kΩ	25°C	50,000	200,000		25,000	200,000		
			Full range	25,000			15,000			
r_i	Input resistance		25°C	1.5	4		0.5	2		MΩ
CMRR	Common-mode rejection ratio	R_S = 50 kΩ	25°C	80	98		70	90		dB
			Full range	80			70			
$\Delta V_{CC}/\Delta V_{IO}$	Power supply rejection ratio	R_S = 50 kΩ	25°C	80	98		70	96		dB
			Full range	80			70			
I_{CC}	Supply current	No load, No signal, See Note 7	25°C		1.8	3		1.8	3	mA
			125°C		1.2	2.5				

†All characteristics are specified under open-loop operation. Full range for SN52107 is −55°C to 125°C and for SN72307 is 0°C to 70°C.

NOTES: 6. Unless otherwise noted $V_{CC\pm}$ = ±5 V to ±20 V for SN52107 and $V_{CC\pm}$ = ±5 V to ±15 V for SN72307. All typical values are at $V_{CC\pm}$ = ±15 V.

7. For SN52107, $V_{CC\pm}$ = ±20 V. For SN72307, $V_{CC\pm}$ = ±15 V.

For ordering instructions and mechanical data, see the SN52741/SN72741 data sheet dated November 1970.

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DEFINITION OF TERMS

Input Offset Voltage (V_{IO}) The d-c voltage which must be applied between the input terminals to force the quiescent d-c output voltage to zero. The input offset voltage may also be defined for the case where two equal resistances (R_S) are inserted in series with the input leads.

Average Temperature Coefficient of Input Offset Voltage (α_{VIO}) The ratio of the change in input offset voltage to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{VIO} = \left| \frac{(V_{IO} @ T_{A(1)}) - (V_{IO} @ T_{A(2)})}{T_{A(1)} - T_{A(2)}} \right|$$ where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

Input Offset Current (I_{IO}) The difference between the currents into the two input terminals with the output at zero volts.

Average Temperature Coefficient Of Input Offset Current (α_{IIO}) The ratio of the change in input offset current to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{IIO} = \left| \frac{(I_{IO} @ T_{A(1)}) - (I_{IO} @ T_{A(2)})}{T_{A(1)} - T_{A(2)}} \right|$$ where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

3

Input Bias Current (I_{IB}) The average of the currents into the two input terminals with the output at zero volts.

Input Voltage Range (V_I) The range of voltage which, if exceeded at either input terminal, will cause the amplifier to cease functioning properly.

Maximum Peak-to-Peak Output Voltage Swing (V_{OPP}) The maximum peak-to-peak output voltage which can be obtained without waveform clipping when the quiescent d-c output voltage is zero.

Large-Signal Differential Voltage Amplification (A_{VD}) The ratio of the peak-to-peak output voltage swing to the change in differential input voltage required to drive the output.

Input Resistance (r_i) The resistance between the input terminals with either input grounded.

Common-Mode Rejection Ratio (CMRR) The ratio of differential voltage amplification to common-mode voltage amplification. This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.

Supply Voltage Rejection Ratio ($\Delta V_{CC}/\Delta V_{IO}$) The ratio of the change in power supply voltages to the change in input offset voltage. For these devices, both supply voltages are varied symmetrically.

THERMAL INFORMATION

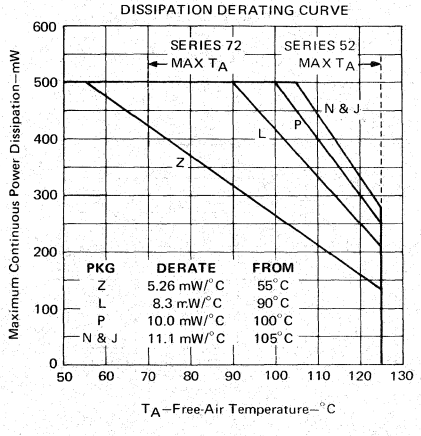

FIGURE 1

TYPICAL APPLICATION DATA

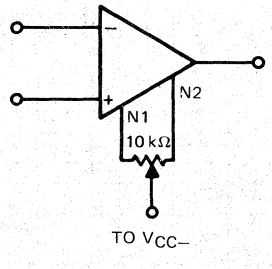

FIGURE 2–INPUT OFFSET VOLTAGE NULL CIRCUIT

TYPICAL CHARACTERISTICS

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

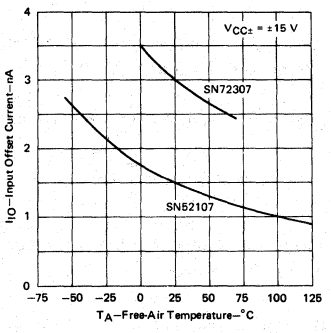

FIGURE 3

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

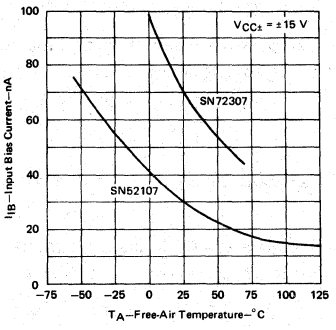

FIGURE 4

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE
vs
FREQUENCY

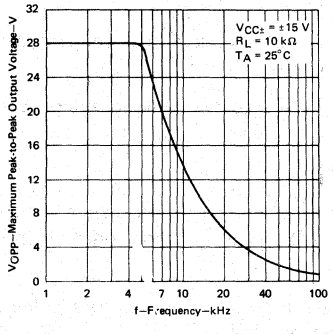

FIGURE 5

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

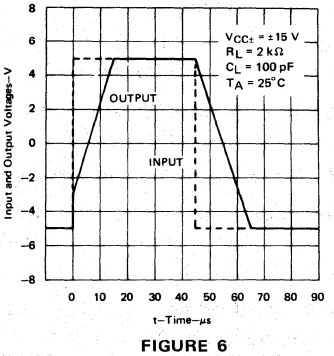

FIGURE 6

OPEN-LOOP LARGE-SIGNAL
DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

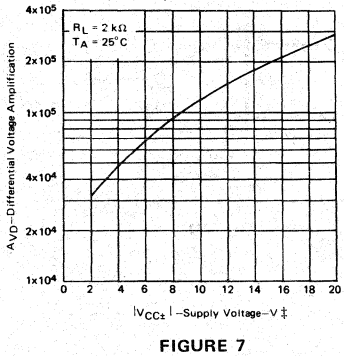

FIGURE 7

OPEN-LOOP LARGE-SIGNAL
DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
FREQUENCY

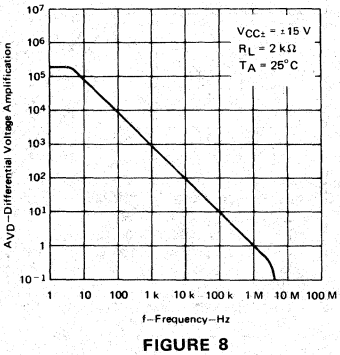

FIGURE 8

‡ Data for supply voltages greater than 15 V is applicable to SN52107 circuits only.

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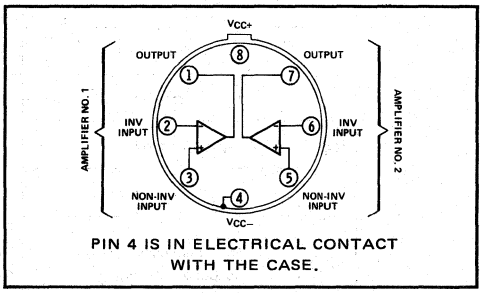
CIRCUIT TYPES SN52558, SN72558
DUAL HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

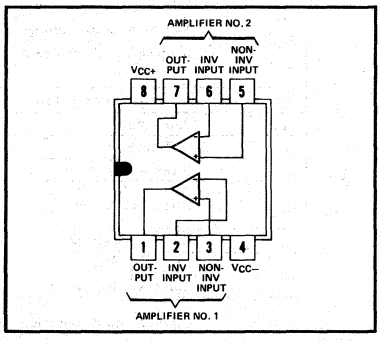
- Short-Circuit Protection
- Large Common-Mode and Differential Voltage Ranges
- No Frequency Compensation Required
- Low Power Consumption
- No Latch-up
- Designed to be Interchangeable with Motorola MC1558/MC1458 and Signetics S5558/N5558

L PLUG-IN PACKAGE
(TOP VIEW)



PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE.

P DUAL-IN-LINE PACKAGE
(TOP VIEW)



3

description

The SN52558 and SN72558 are dual high-performance operational amplifiers with each half electrically similar to SN52741/SN72741 except that offset null capability is not provided.

The high common-mode input voltage range and the absence of latch-up make these amplifiers ideal for voltage-follower applications. The devices are short-circuit protected and the internal frequency compensation ensures stability without external components.

The SN52558 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN72558 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN52558	SN72558	UNIT
Supply voltage V_{CC+} (see Note 1)		22	18	V
Supply voltage V_{CC-} (see Note 1)		−22	−18	V
Differential input voltage (see Note 2)		±30	±30	V
Input voltage (either input, see Notes 1 and 3)		±15	±15	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	
Continuous total dissipation at (or below) 70°C free-air temperature range (see Note 5)	Each amplifier	500	500	mW
	Total package	680	680	
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	L Package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	P Package	260	260	°C

NOTES:
1. All voltage values, unless otherwise noted, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or either power supply. For the SN52558 only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.
5. For operation of SN52558 above 70°C free-air temperature, refer to Dissipation Derating Curve, Figure 1.

electrical characteristics at specified free-air temperature, V_{CC+} = 15 V, V_{CC-} = −15 V

PARAMETER		TEST CONDITIONS†		SN52558			SN72558			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S \leq 10\ k\Omega$	25°C		1	5		1	6	mV
			Full range			6			7.5	
I_{IO}	Input offset current		25°C		20	200		20	200	nA
			Full range			500			300	
I_{IB}	Input bias current		25°C		80	500		80	500	nA
			Full range			1500			800	
V_I	Input voltage range		25°C	±12	±13		±12	±13		V
			Full range	±12			±12			
V_{OPP}	Maximum peak-to-peak output voltage swing	R_L = 10 kΩ	25°C	24	28		24	28		V
		$R_L \geq$ 10 kΩ	Full range	24			24			
		R_L = 2 kΩ	25°C	20	26		20	26		
		$R_L \geq$ 2 kΩ	Full range	20			20			
A_{VD}	Large-signal differential voltage amplification	$R_L \geq$ 2 kΩ, V_O = ±10 V	25°C	50,000	200,000		20,000	200,000		
			Full range	25,000			15,000			
B_{OM}	Maximum-output-swing bandwidth (closed-loop)	R_L = 2 kΩ, $V_O \geq$ ±10 V, A_{VD} = 1, THD ≤ 5%	25°C		14			14		kHz
B_1	Unity-gain bandwidth		25°C		1			1		MHz
ϕ_m	Phase margin	A_{VD} = 1	25°C		65°			65°		
A_m	Gain margin		25°C		11			11		dB
r_i	Input resistance		25°C	0.3	2		0.3	2		MΩ
r_o	Output resistance	V_O = 0, See Note 5	25°C		75			75		Ω
C_i	Input capacitance		25°C		1.4			1.4		pF
z_{ic}	Common-mode input impedance	f = 20 Hz	25°C		200			200		MΩ
CMRR	Common-mode rejection ratio	$R_S \leq 10\ k\Omega$	25°C	70	90		70	90		dB
			Full range	70			70			
$\Delta V_{IO}/\Delta V_{CC}$	Power supply sensitivity	$R_S \leq 10\ k\Omega$	25°C		30	150		30	150	μV/V
			Full range			150			150	
e_n	Equivalent input noise voltage (closed-loop)	A_{VD} = 100, R_S = 0, f = 1 kHz, BW = 1 Hz	25°C		45			45		$nV/\sqrt{Hz}$
I_{OS}	Short-circuit output current		25°C		±25	±40		±25	±40	mA
I_{CC}	Supply current (Both amplifiers)	No load, No signal	25°C		3.4	5.6		3.4	5.6	mA
			Full range			6.6			6.6	
P_D	Total power dissipation (Both amplifiers)	No load, No signal	25°C		100	170		100	170	mW
			Full range			200			200	
V_{o1}/V_{o2}	Channel separation		25°C		120			120		dB

†All characteristics are specified under open-loop operation, unless otherwise noted. Full range for SN52558 is −55°C to 125°C and for SN72558 is 0°C to 70°C.

NOTE 5: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

operating characteristics, V_{CC+} = 15 V, V_{CC-} = −15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	SN52558			SN72558			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	V_I = 20 mV, R_L = 2 kΩ,		0.3			0.3		μs
	Overshoot	C_L = 100 pF, See Figure 2		5%			5%		
SR	Slew rate at unity gain	V_I = 10 V, R_L = 2 kΩ, C_L = 100 pF, See Figure 2		0.5			0.5		V/μs

For mechanical data and ordering instructions, see the SN52741/SN72741 data sheet dated November 1970.

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DEFINITION OF TERMS

Input Offset Voltage (V_{IO}) The d-c voltage which must be applied between the input terminals to force the quiescent d-c output voltage to zero. The input offset voltage may also be defined for the case where two equal resistances (R_S) are inserted in series with the input leads.

Input Offset Current (I_{IO}) The difference between the currents into the two input terminals with the output at zero volts.

Input Bias Current (I_{IB}) The average of the currents into the two input terminals with the output at zero volts.

Input Voltage Range (V_I) The range of voltage which if exceeded at either input terminal will cause the amplifier to cease functioning properly.

Maximum Peak-to-Peak Output Voltage Swing (V_{OPP}) The maximum peak-to-peak output voltage which can be obtained without waveform clipping when the quiescent d-c output voltage is zero.

Large-Signal Differential Voltage Amplification (A_{VD}) The ratio of the peak-to-peak output voltage swing to the change in differential input voltage required to drive the output.

3

Maximum-Output-Swing Bandwidth (B_{OM}) The range of frequencies within which the maximum output voltage swing is above a specified value.

Unity-Gain Bandwidth (B_1) The range of frequencies within which the voltage amplification is greater than unity.

Phase Margin (ϕ_m) A figure equal to 180° minus the absolute value of the phase shift measured around the loop at that frequency at which the magnitude of the loop gain is unity.

Gain Margin (A_m) The reciprocal of the differential voltage amplification at that frequency where the absolute value of the phase shift measured around the loop is 180°.

Input Resistance (r_i) The resistance between the input terminals with either input grounded.

Output Resistance (r_o) The resistance between the output terminal and ground.

Input Capacitance (C_i) The capacitance between the input terminals with either input grounded.

Common-Mode Input Impedance (z_{ic}) The parallel sum of the small-signal impedances between each input terminal and ground.

Common-Mode Rejection Ratio (CMRR) The ratio of differential voltage amplification to common-mode voltage amplification. This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.

Power Supply Sensitivity ($\Delta V_{IO}/\Delta V_{CC}$) The ratio of the change in input offset voltage to the change in supply voltages producing it. For these devices, both supply voltages are varied symmetrically.

Short-Circuit Output Current (I_{OS}) The maximum output current available from the amplifier with the output shorted to ground or to either supply.

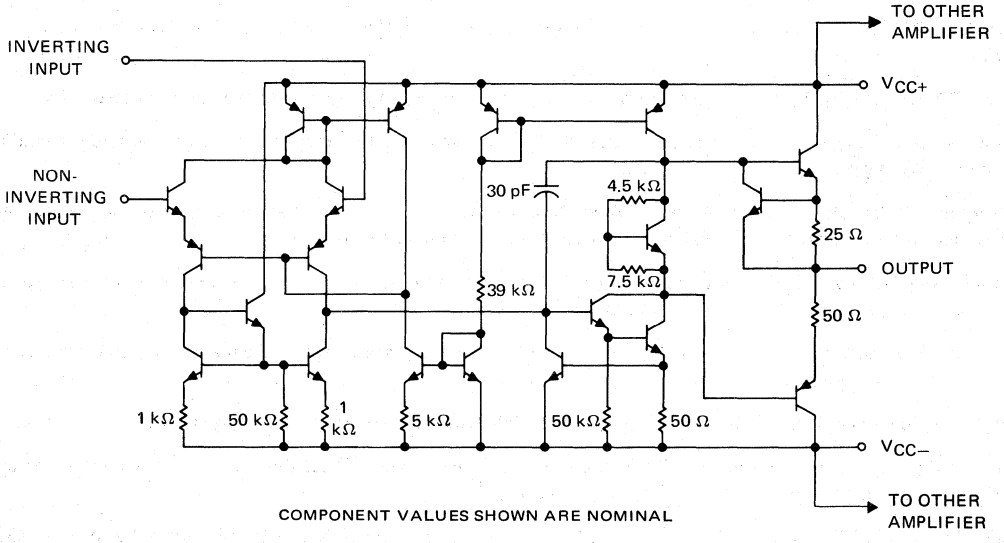
Total Power Dissipation (P_D) The total d-c power supplied to the device less any power delivered from the device to a load. At no load: $P_D = V_{CC+} \cdot I_{CC+} + V_{CC-} \cdot I_{CC-}$.

Rise Time (t_r) The time required for an output voltage step to change from 10% to 90% of its final value.

Overshoot The quotient of: (1) the largest deviation of the output signal value from its steady-state value after a step-function change of the input signal, and (2) the difference between the output signal values in the steady state before and after the step-function change of the input signal.

Slew Rate (SR) The average time rate of change of the closed-loop amplifier output voltage for a step-signal input. Slew rate is measured between specified output levels (0 and 10 volts for this device) with feedback adjusted for unity gain.

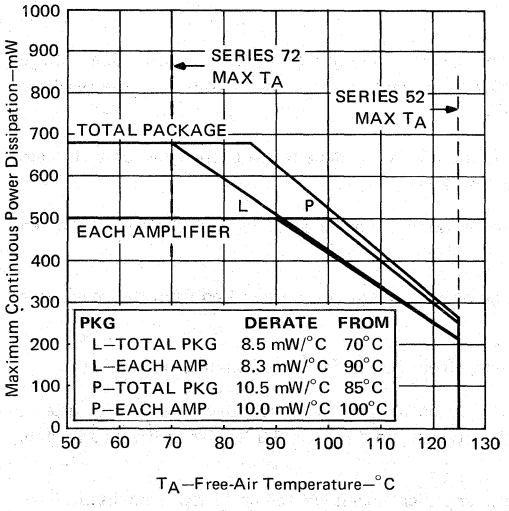
schematic (each amplifier)



COMPONENT VALUES SHOWN ARE NOMINAL

THERMAL INFORMATION

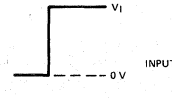
DISSIPATION DERATING CURVE



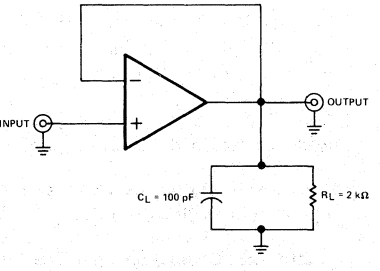
PKG	DERATE	FROM
L—TOTAL PKG	8.5 mW/°C	70°C
L—EACH AMP	8.3 mW/°C	90°C
P—TOTAL PKG	10.5 mW/°C	85°C
P—EACH AMP	10.0 mW/°C	100°C

FIGURE 1

PARAMETER MEASUREMENT INFORMATION



INPUT VOLTAGE WAVEFORM



TEST CIRCUIT

FIGURE 2–RISE TIME, OVERSHOOT, AND SLEW RATE

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TYPICAL CHARACTERISTICS

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

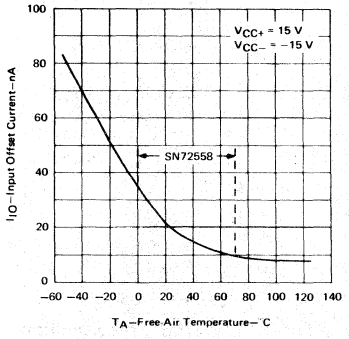

FIGURE 3

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

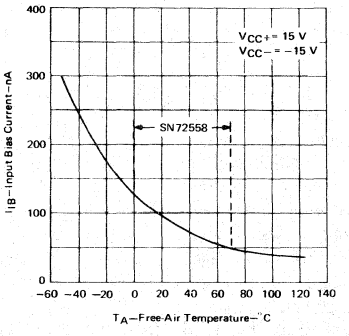

FIGURE 4

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE
vs
LOAD RESISTANCE

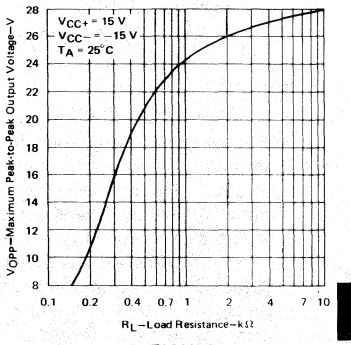

FIGURE 5

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE
vs
FREQUENCY

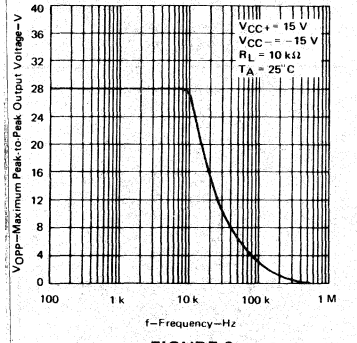

FIGURE 6

OPEN-LOOP LARGE-SIGNAL
DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

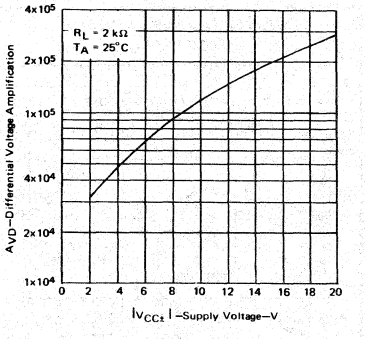

FIGURE 7

OPEN-LOOP LARGE-SIGNAL
DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
FREQUENCY

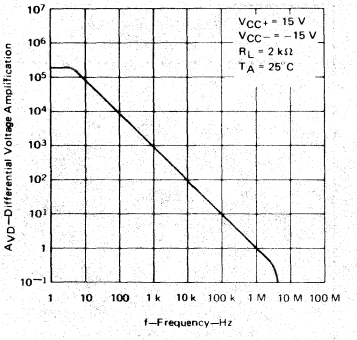

FIGURE 8

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

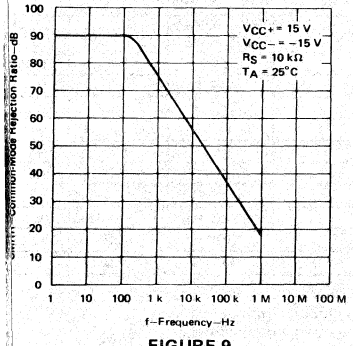

FIGURE 9

OUTPUT VOLTAGE
vs
ELAPSED TIME

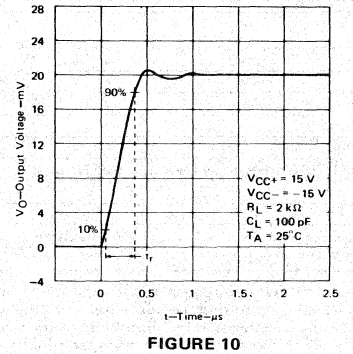

FIGURE 10

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

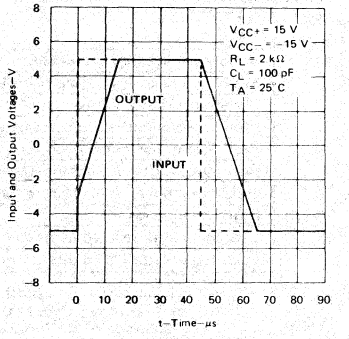

FIGURE 11

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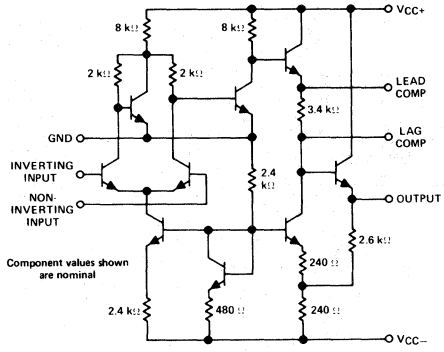
CIRCUIT TYPES SN52702A, SN52702, SN72702 GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

SN52702A features

- Open-Loop Voltage Amplification . . . 3600 Typ
- Designed to be Interchangeable With Fairchild μA702A
- CMRR . . . 100 dB Typ

schematic



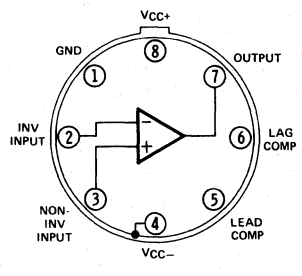
description

The SN52702A, SN52702 and SN72702 circuits are high-gain, wideband operational amplifiers, each having differential inputs and single-ended emitter-follower outputs. Provisions are incorporated within the circuit whereby external components may be used to compensate the amplifier for stable operation under various feedback or load conditions. Component matching, inherent in silicon monolithic circuit-fabrication techniques, produces an amplifier with low-drift and low-offset characteristics. The SN52702A is an improved version of the SN52702. These amplifiers are particularly useful for applications requiring transfer or generation of linear and non-linear functions up to a frequency of 30 MHz.

The SN52702A and SN52702 circuits are characterized for operation over the full military temperature range of –55°C to 125°C. The SN72702 circuit is characterized for operation over the temperature range of 0°C to 70°C.

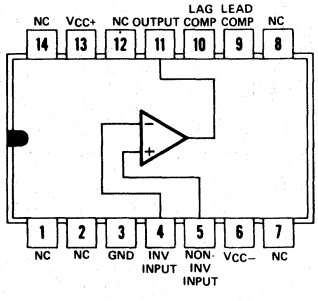
terminal assignments

L PLUG-IN PACKAGE (TOP VIEW)

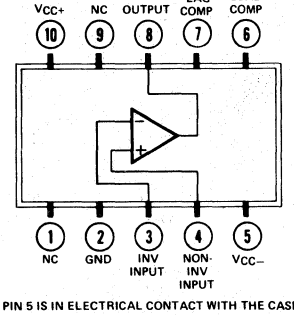


PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE

N DUAL-IN-LINE PACKAGE (TOP VIEW)



S FLAT PACKAGE (TOP VIEW)



PIN 5 IS IN ELECTRICAL CONTACT WITH THE CASE

NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN52702A, SN52702	SN72702	UNIT
Supply voltage V_{CC+} (see Note 1)		14	14	V
Supply voltage V_{CC-} (see Note 1)		–7	–7	V
Differential input voltage (see Note 2)		±5	±5	V
Input voltage (either input, see Notes 1 and 3)		–6 to 1.5	–6 to 1.5	V
Peak output current ($t_w \leq 1$ S)		50	50	mA
Continuous total dissipation at (or below) 70°C free-air temperature (see Note 4)		300	300	mW
Operating free-air temperature range		–55 to 125	0 to 70	°C
Storage temperature range		–65 to 150	–65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	L or S Package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N Package	260	260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the lesser of the two supply voltages.
4. For operation of SN52702A and SN52702 above 70°C free-air temperature, refer to Dissipation Derating Curve, Figure 3.

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SN52702A

electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS†			SN52702A V_{CC+} = 12 V, V_{CC-} = −6 V MIN	SN52702A V_{CC+} = 12 V, V_{CC-} = −6 V TYP	SN52702A V_{CC+} = 12 V, V_{CC-} = −6 V MAX	SN52702A V_{CC+} = 6 V, V_{CC-} = −3 V MIN	SN52702A V_{CC+} = 6 V, V_{CC-} = −3 V TYP	SN52702A V_{CC+} = 6 V, V_{CC-} = −3 V MAX	UNIT
V_{IO}	Input offset voltage	$R_S \leq 2\ k\Omega$		25°C		0.5	2		0.7	3	mV
				Full range			3			4	
α_{VIO}	Average temperature coefficient of input offset voltage	$R_S = 50\ \Omega$		−55°C to 25°C		2	10		3	15	μV/°C
				25°C to 125°C		2.5	10		3.5	15	
I_{IO}	Input offset current			25°C		0.2	0.5		0.12	0.5	μA
				−55°C		0.4	1.5		0.3	1.5	
				125°C		0.08	0.5		0.05	0.5	
α_{IIO}	Average temperature coefficient of input offset current			−55°C to 25°C		3	16		2	13	nA/°C
				25°C to 125°C		1	5		0.7	4	
I_{IB}	Input bias current			25°C		2	5		1.2	3.5	μA
				−55°C		4.3	10		2.6	7.5	
V_I	Input voltage range	Positive swing		25°C	0.5	1		0.5	1		V
		Negative swing			−4	−5		−1.5	−2		
V_{OPP}	Maximum peak-to-peak output voltage swing	$R_L \geq 100\ k\Omega$		25°C	10	10.6		5	5.4		V
				Full range	10			5			
		$R_L = 10\ k\Omega$		25°C	7	8		3	4		
		$R_L \geq 10\ k\Omega$		Full range	7			3			
A_{VD}	Large-signal differential voltage amplification	$R_L \geq 100\ k\Omega$	$V_O = \pm 5$ V	25°C	2500	3600	6000				
				Full range	2000		7000				
			$V_O = \pm 2.5$ V	25°C				600	900	1500	
				Full range				500		1750	
r_i	Input resistance			25°C	16	40		22	67		kΩ
				Full range	6			8			
r_o	Output resistance	$V_O = 0$,	See Note 3	25°C		200	500		300	700	Ω
CMRR	Common-mode rejection ratio	$R_S \leq 2\ k\Omega$		25°C	80	100		80	100		dB
				Full range	70			70			
$\Delta V_{IO}/\Delta V_{CC}$	Power supply sensitivity	$R_S \leq 2\ k\Omega$		25°C		75			75		μV/V
				Full range			200			200	
I_{CC}	Supply current	No load,	No signal	25°C		5	6.7		2.1	3.3	mA
				−55°C		5	7.5		2.1	3.9	
				125°C		4.4	6.7		1.7	3.3	
P_D	Total power dissipation	No load,	No signal	25°C		90	120		19	30	mW
				−55°C		90	135		19	35	
				125°C		80	120		15	30	

All characteristics are specified under open-loop operation. Full range for SN52702A is −55°C to 125°C.

NOTE 3: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

SN52702

electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS†			SN52702 V_{CC+} = 12 V, V_{CC-} = −6 V			SN52702 V_{CC+} = 6 V, V_{CC-} = −3 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S \leq 2\ k\Omega$		25°C		2	5		2	5	mV
				Full range			6			6	
α_{VIO}	Average temperature coefficient of input offset voltage	$R_S = 50\ \Omega$		−55°C to 25°C		10			10		µV/°C
				25°C to 125°C		5			5		
I_{IO}	Input offset current			25°C		0.5	2		0.3	2	µA
				−55°C		1	3			3	
				125°C		0.2	3			3	
α_{IIO}	Average temperature coefficient of input offset current			−55°C to 25°C		6			5		nA/°C
				25°C to 125°C		3			2		
I_{IB}	Input bias current			25°C		4	10		2.5	7	µA
				−55°C		6.5	20			14	
V_I	Input voltage range	Positive swing		25°C	0.5	1		0.5	1		V
		Negative swing			−4	−5		−1.5	−2		
V_{OPP}	Maximum peak-to-peak output voltage swing	$R_L \geq 100\ k\Omega$			10	10.6		5	5.4		V
		$R_L = 10\ k\Omega$				8			4		
A_{VD}	Large-signal differential voltage amplification	$R_L \geq 100\ k\Omega$	$V_O = \pm 5$ V	25°C	1400	2600					
				Full range	1000						
			$V_O = \pm 2.5$ V	25°C				380	700		
r_i	Input resistance			25°C	8	25		12	40		kΩ
				Full range	3			4			
r_o	Output resistance	$V_O = 0$,	See Note 3	25°C		200	500		300	700	Ω
CMRR	Common-mode rejection ratio	$R_S \leq 2\ k\Omega$		25°C	70	80		70	80		dB
$\Delta V_{IO}/\Delta V_{CC}$	Power supply sensitivity	$R_S \leq 2\ k\Omega$		25°C		60	300		60	300	µV/V
I_{CC}	Supply current	No load,	No signal	25°C		5	6.7		2.1	3.9	mA
P_D	Total power dissipation	No load,	No signal	25°C		90	120		19	35	mW

†All characteristics are specified under open-loop operation. Full range for SN52702 is −55°C to 125°C.

NOTE 3: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

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SN72702

lectrical characteristics at specified free-air temperature, V_{CC+} = 12 V, V_{CC-} = −6 V

PARAMETER		TEST CONDITIONS†			SN72702 MIN	SN72702 TYP	SN72702 MAX	UNIT
V_{IO}	Input offset voltage	$R_S \leq 2\ k\Omega$		25°C		5	10	mV
				Full Range			15	
α_{VIO}	Average temperature coefficient of input offset voltage	$R_S = 50\ \Omega$		Full Range		5		μV/°C
I_{IO}	Input offset current			25°C		0.5	5	μA
				Full Range			7.5	
α_{IIO}	Average temperature coefficient of input offset current			0°C to 25°C		5		nA/°C
				25°C to 70°C		3		
I_{IB}	Input bias current			25°C		4	15	μA
				0°C		4.5	20	
V_I	Input voltage range	Positive swing		25°C	0.5	1		V
		Negative swing			−4	−5		
V_{OPP}	Maximum peak-to-peak output voltage swing	$R_L \geq 100\ k\Omega$		25°C	10	10.6		V
A_{VD}	Large-signal differential voltage amplification	$R_L \geq 100\ k\Omega$,	$V_O = \pm 5$ V	25°C	1000	2600		
				Full Range	800			
r_i	Input resistance			25°C	6	25		kΩ
				Full Range	3.5			
r_o	Output resistance	V_O = 0,	See Note 3	25°C		200	600	Ω
CMRR	Common-mode rejection ratio	$R_S \leq 2\ k\Omega$		25°C	65	80		dB
$\Delta V_{IO}/\Delta V_{CC}$	Power supply sensitivity	$R_S \leq 2\ k\Omega$		25°C		60	300	μV/V
I_{CC}	Supply current	No load,	No signal	25°C		5	7	mA
P_D	Total power dissipation	No load,	No signal	25°C		90	125	mW

All characteristics are specified under open-loop operation. Full range for SN72702 is 0°C to 70°C.
OTE 3: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

SN52702A, SN52702, SN72702

perating characteristics V_{CC+} = 12 V, V_{CC-} = −6 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS		ALL TYPES MIN	ALL TYPES TYP	ALL TYPES MAX	UNIT
t_r	Rise time	1	V_I = 10 mV,	C_L = 0		25	120	ns
		2	V_I = 1 mV			10	30	ns
	Overshoot	1	V_I = 10 mV,	C_L = 100 pF		10%	50%	
		2	V_I = 1 mV			20%	40%	
SR	Slew rate	1	V_I = 6 V,	C_L = 100 pF		1.7		V/μs
		2	V_I = 100 mV			11		

PARAMETER MEASUREMENT INFORMATION

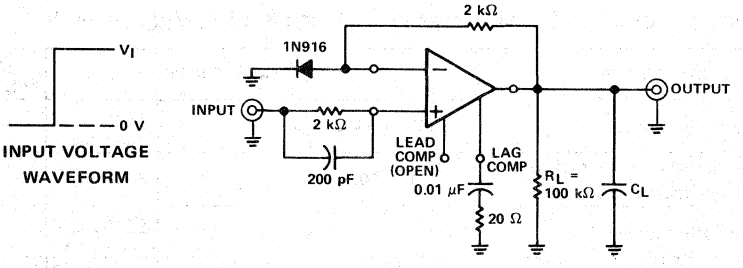

FIGURE 1–UNITY-GAIN AMPLIFIER

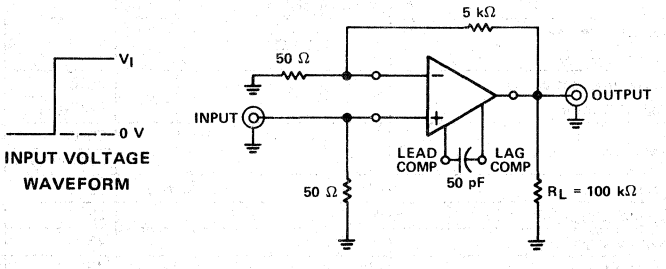

FIGURE 2–GAIN-OF-100 AMPLIFIER

THERMAL INFORMATION

SN52702A, SN52702
DISSIPATION DERATING CURVE

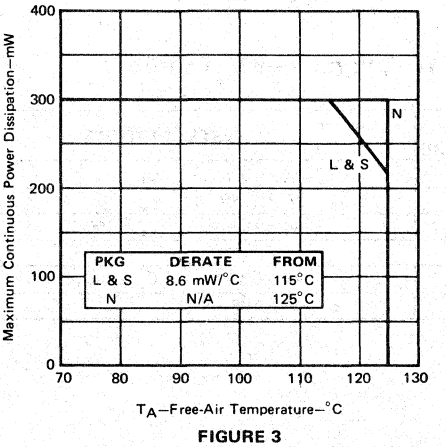

FIGURE 3

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DEFINITION OF TERMS

Input Offset Voltage (V_{IO}) The d-c voltage which must be applied between the input terminals to force the quiescent d-c output voltage to zero. The input offset voltage may also be defined for the case where two equal resistances (R_S) are inserted in series with the input leads.

Average Temperature Coefficient of Input Offset Voltage (α_{VIO}) The ratio of the change in input offset voltage to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{VIO} = \left| \frac{(V_{IO} @ T_{A(1)}) - (V_{IO} @ T_{A(2)})}{T_{A(1)} - T_{A(2)}} \right|$$ where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

Input Offset Current (I_{IO}) The difference between the currents into the two input terminals with the output at zero volts.

Average Temperature Coefficient Of Input Offset Current (α_{IIO}) The ratio of the change in input offset current to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{IIO} = \left| \frac{(I_{IO} @ T_{A(1)}) - (I_{IO} @ T_{A(2)})}{T_{A(1)} - T_{A(2)}} \right|$$ where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

Input Bias Current (I_{IB}) The average of the currents into the two input terminals with the output at zero volts.

Input Voltage Range (V_I) The range of voltage which if exceeded at either input terminal will cause the amplifier to cease functioning properly.

Maximum Peak-to-Peak Output Voltage Swing (V_{OPP}) The maximum peak-to-peak output voltage which can be obtained without waveform clipping when the quiescent d-c output voltage is zero.

Large-Signal Differential Voltage Amplification (A_{VD}) The ratio of the peak-to-peak output voltage swing to the change in differential input voltage required to drive the output.

Input Resistance (r_i) The resistance between the input terminals with either input grounded.

Output Resistance (r_o) The resistance between the output terminal and ground.

Common-Mode Rejection Ratio (CMRR) The ratio of differential voltage amplification to common-mode voltage amplification. This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.

Power Supply Sensitivity ($\Delta V_{IO}/\Delta V_{CC}$) The ratio of the change in input offset voltage to the change in supply voltages producing it. For these devices, both supply voltages are varied symmetrically.

Total Power Dissipation (P_D) The total d-c power supplied to the device less any power delivered from the device to a load. At no load: $P_D = V_{CC+} \cdot I_{CC+} + V_{CC-} \cdot I_{CC-}$.

Rise Time (t_r) The time required for an output voltage step to change from 10% to 90% of its final value.

Overshoot The quotient of: (1) the largest deviation of the output signal value from its steady-state value after a step-function change of the input signal, and (2) the difference between the output signal values in the steady state before and after the step-function change of the input signal.

Slew Rate (SR) The average time rate of change of the closed-loop amplifier output voltage for a step-signal input. Slew rate is measured between specified output levels (0 and 10 volts for this device) with feedback adjusted for unity gain.

TYPICAL CHARACTERISTICS

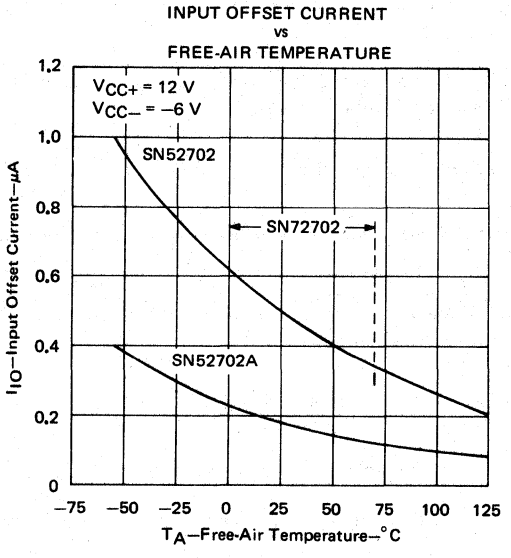


FIGURE 4

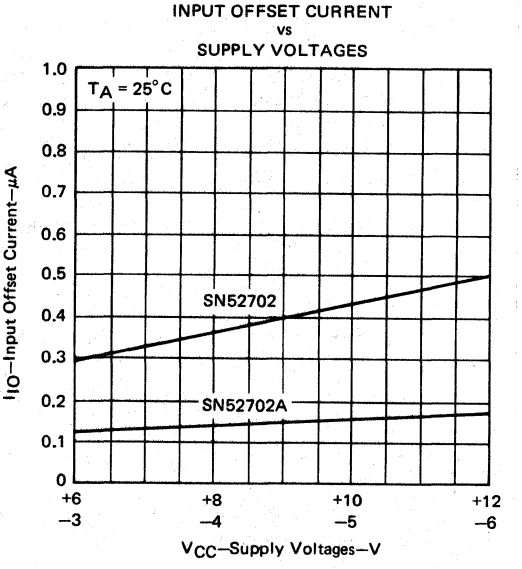


FIGURE 5

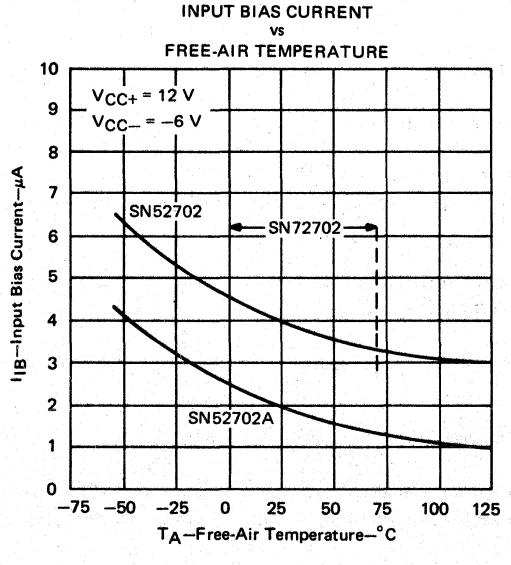


FIGURE 6

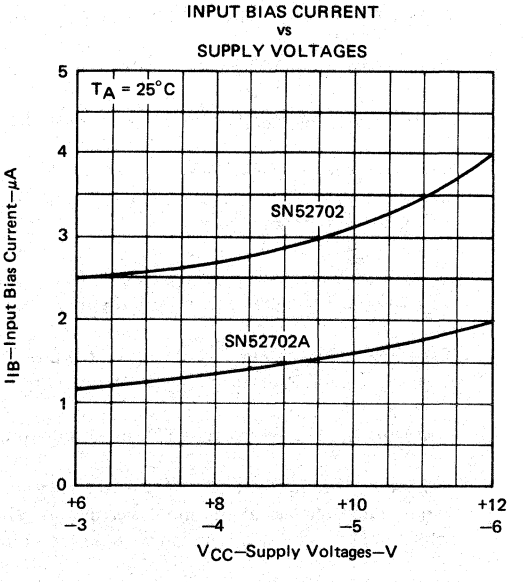


FIGURE 7

TYPICAL CHARACTERISTICS

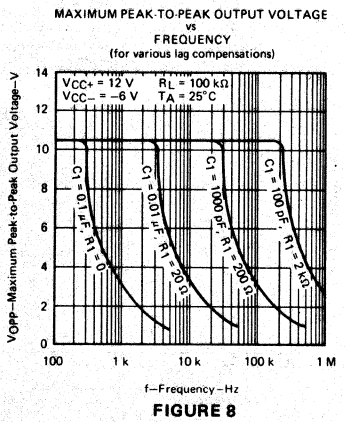
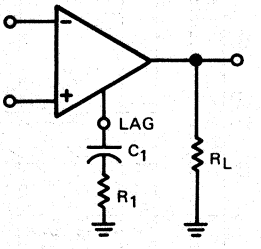


FIGURE 8



LAG COMPENSATION CIRCUIT FOR FIGURES 8, 9, AND 10

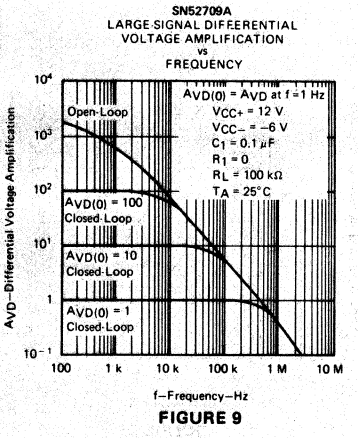


FIGURE 9

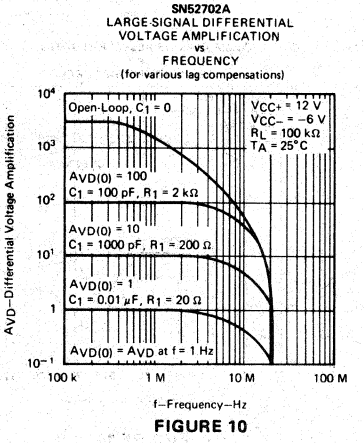


FIGURE 10

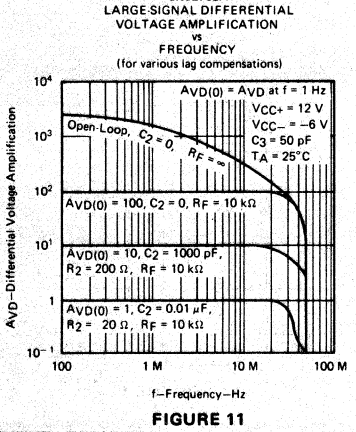
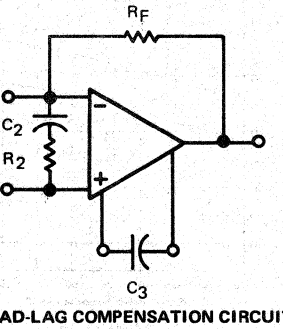


FIGURE 11



LEAD-LAG COMPENSATION CIRCUIT FOR FIGURE 11

TYPICAL CHARACTERISTICS

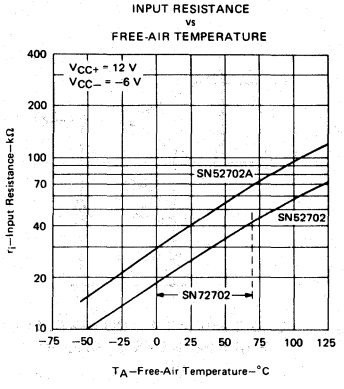


FIGURE 12

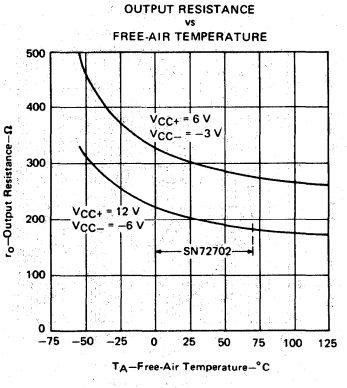


FIGURE 13

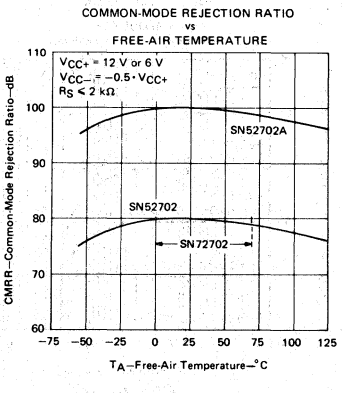


FIGURE 14

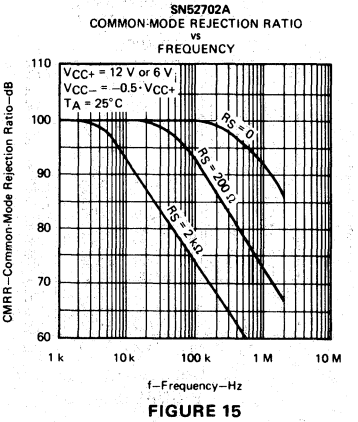


FIGURE 15

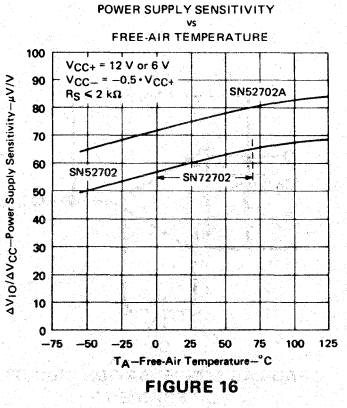


FIGURE 16

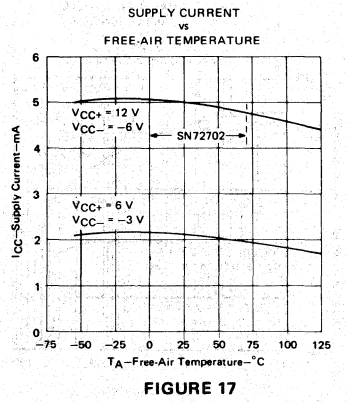


FIGURE 17

TEXAS INSTRUMENTS
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SERIES 52/72 OPERATIONAL AMPLIFIERS
featuring

- Common-Mode Input Range . . . ±10 V Typical
- Designed to be Interchangeable with Fairchild μA709A, μA709, and μA709C
- Maximum Peak-to-Peak Output Voltage Swing . . . 28 V Typical with 15 V Supplies

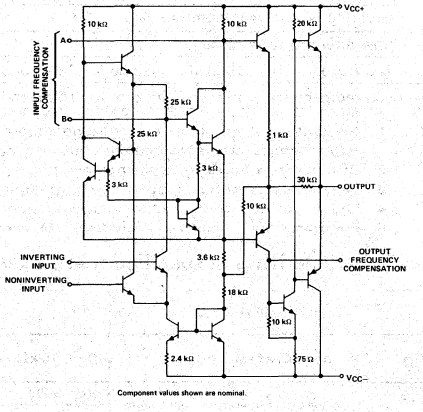
description

These circuits are high-performance operational amplifiers, each having high-impedance differential inputs and a low-impedance output. Component matching, inherent with silicon monolithic circuit-fabrication techniques, produces an amplifier with low-drift and low-offset characteristics. Provisions are incorporated within the circuit whereby external components may be used to compensate the amplifier for stable operation under various feedback or load conditions. These amplifiers are particularly useful for applications requiring transfer or generation of linear or nonlinear functions.

The SN52709A circuit features improved offset characteristics, reduced input-current requirements, and lower power dissipation when compared to the SN52709 circuit. In addition, maximum values of the average temperature coefficients of offset voltage and current are guaranteed.

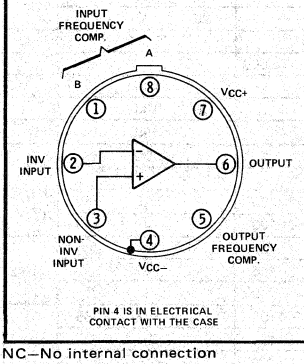
The SN52709A and SN52709 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN72709 is characterized for operation from 0°C to 70°C.

schematic

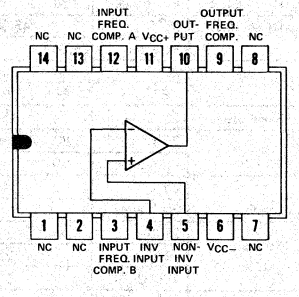


terminal assignments

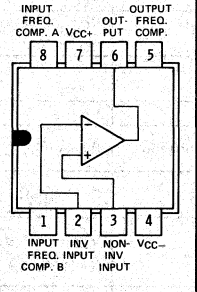
L — PLUG-IN PACKAGE (TOP VIEW)



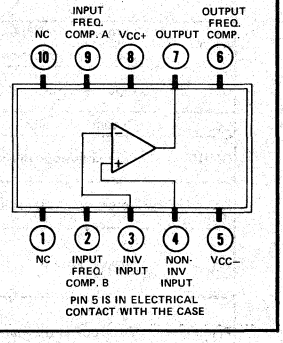
N — DUAL-IN-LINE PACKAGE (TOP VIEW)



P — DUAL-IN-LINE PACKAGE (TOP VIEW)



S — FLAT PACKAGE (TOP VIEW)



NC—No internal connection

voltages specified

Throughout this data sheet, supply voltages are specified either as a range or as a specific value. A positive voltage within the specified range (or of the specified value) is applied to V_{CC+}, and an equal negative voltage is applied to V_{CC-}.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN52709A, SN52709	SN72709	UNIT
Supply voltage V_{CC+} (see Note 1)		18	18	V
Supply voltage V_{CC-} (see Note 1)		−18	−18	V
Differential input voltage (see Note 2)		±5	±5	V
Input voltage (either input, see Notes 1 and 3)		±10	±10	V
Duration of output short-circuit (see Note 4)		5	5	s
Continuous total dissipation at (or below) 70°C free-air temperature (see Note 5)		300	300	mW
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	L or S Package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N or P Package	260	260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 10 volts, whichever is less.
4. The output may be shorted to ground or either power supply.
5. For operation of SN52709A and SN52709 above 70°C free-air temperature, refer to Dissipation Derating Curve, Figure 1.

3

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±9 V to ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN52709A MIN	SN52709A TYP‡	SN52709A MAX	SN52709 MIN	SN52709 TYP‡	SN52709 MAX	UNIT
V_{IO}	Input offset voltage	$R_S \leq 10$ kΩ	25°C		0.6	2		1	5	mV
			Full range			3			6	
α_{VIO}	Average temperature coefficient of input offset voltage	R_S = 50 Ω	Full range		1.8	10		3		μV/°C
		R_S = 10 kΩ	−55°C to 25°C		4.8	25		6		
			25°C to 125°C		2	15		6		
I_{IO}	Input offset current		25°C		10	50		50	200	nA
			−55°C		40	250		100	500	
			125°C		3.5	50		20	200	
α_{IIO}	Average temperature coefficient of input offset current		−55°C to 25°C		0.45	2.8				nA/°C
			25°C to 125°C		0.08	0.5				
I_{IB}	Input bias current		25°C		0.1	0.2		0.2	0.5	μA
			−55°C		0.3	0.6		0.5	1.5	
V_I	Input voltage range	$V_{CC\pm}$ = ±15 V	25°C	±8	±10		±8	±10		V
			Full range	±8			±8			
V_{OPP}	Maximum peak-to-peak output voltage swing	$V_{CC\pm}$ = ±15 V, $R_L \geqslant 10$ kΩ	25°C	24	28		24	28		V
			Full range	24			24			
		$V_{CC\pm}$ = ±15 V, R_L = 2 kΩ	25°C	20	26		20	26		
		$V_{CC\pm}$ = ±15 V, $R_L \geqslant 2$ kΩ	Full range	20			20			
A_{VD}	Large-signal differential voltage amplification	$V_{CC\pm}$ = ±15 V, $R_L \geqslant 2$ kΩ, V_O = ±10 V	25°C		45,000			45,000		
			Full range	25,000		70,000	25,000		70,000	
r_i	Input resistance		25°C	350	750		150	400		kΩ
			−55°C	85	185		40	100		
r_o	Output resistance	V_O = 0, See Note 6	25°C		150			150		Ω
CMRR	Common-mode rejection ratio	$R_S \leq 10$ kΩ	25°C	80	110		70	90		dB
			Full range	80			70			
$\Delta V_{IO}/\Delta V_{CC}$	Power supply sensitivity	$R_S \leq 10$ kΩ	25°C		40	100		25	150	μV/V
			Full range			100			150	
I_{CC}	Supply current	$V_{CC\pm}$ = ±15 V, No load, No signal	25°C		2.5	3.6		2.6	5.5	mA
			−55°C		2.7	4.5				
			125°C		2.1	3				
P_D	Total power dissipation	$V_{CC\pm}$ = ±15 V, No load, No signal	25°C		75	108		78	165	mW
			−55°C		81	135				
			125°C		63	90				

†All characteristics are specified under open-loop operation. Full range for SN52709A and SN52709 is −55°C to 125°C.

‡All typical values are at $V_{CC\pm}$ = ±15 V.

Note 6: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

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electrical characteristics at specified free-air temperature (unless otherwise noted $V_{CC\pm} = \pm 15$ V)

PARAMETER		TEST CONDITIONS†		SN72709			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{CC\pm} = \pm 9$ V to ± 15 V, $R_S \leq 10$ kΩ	25°C		2	7.5	mV
			Full range			10	
I_{IO}	Input offset current	$V_{CC\pm} = \pm 9$ V to ± 15 V	25°C		100	500	nA
			Full range			750	
I_{IB}	Input bias current	$V_{CC\pm} = \pm 9$ V to ± 15 V	25°C		0.3	1.5	μA
			Full range			2	
V_I	Input voltage range		25°C	±8	±10		V
V_{OPP}	Maximum peak-to-peak output voltage swing	$R_L \geq 10$ kΩ	25°C	24	28		V
			Full range	24			
		$R_L = 2$ kΩ	25°C	20	26		
		$R_L \geq 2$ kΩ	Full range	20			
A_{VD}	Large-signal differential voltage amplification	$R_L \leq 2$ kΩ, $V_O = \pm 10$ V	25°C	15,000	45,000		
			Full range	12,000			
r_i	Input resistance		25°C	50	250		kΩ
			Full range	35			
r_o	Output resistance	$V_O = 0$, See Note 6	25°C		150		Ω
CMRR	Common-mode rejection ratio	$R_S \leq 10$ kΩ	25°C	65	90		dB
$\Delta V_{IO}/\Delta V_{CC}$	Power supply sensitivity	$R_S \leq 10$ kΩ	25°C		25	200	μV/V
P_D	Total power dissipation	No load, No signal	25°C		80	200	mW

†All characteristics are specified under open-loop operation. Full range for SN72709 is 0°C to 70°C.

NOTE 6: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

operating characteristics $V_{CC\pm} = \pm 9$ V to ± 15 V, $T_A = 25$°C

PARAMETER		TEST CONDITIONS		SN52709A SN52709 SN72709			UNIT
				MIN	TYP	MAX	
t_r	Rise time	$V_I = 20$ mV, $R_L = 2$ kΩ, See Figure 2	$C_L = 0$		0.3	1	μs
	Overshoot		$C_L = 100$ pF		6%	30%	

THERMAL INFORMATION

SN52709A, SN52709
DISSIPATION DERATING CURVE

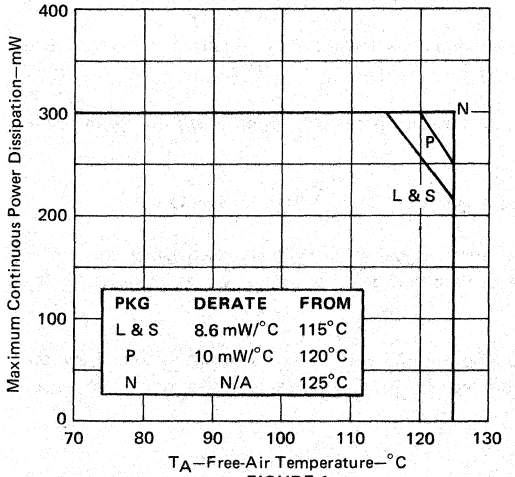

FIGURE 1

PARAMETER MEASUREMENT INFORMATION

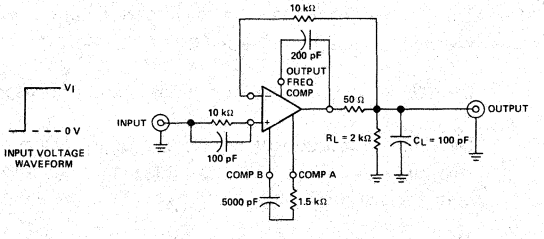

FIGURE 2–RISE TIME AND SLEW RATE

DEFINITION OF TERMS

Input Offset Voltage (V_{IO}) The d-c voltage which must be applied between the input terminals to force the quiescent d-c output voltage to zero. The input offset voltage may also be defined for the case where two equal resistances (R_S) are inserted in series with the input leads.

Average Temperature Coefficient of Input Offset Voltage (α_{VIO}) The ratio of the change in input offset voltage to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{VIO} = \left| \frac{(V_{IO} @ T_{A(1)}) - (V_{IO} @ T_{A(2)})}{T_{A(1)} - T_{A(2)}} \right|$$ where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

Input Offset Current (I_{IO}) The difference between the currents into the two input terminals with the output at zero volts.

Average Temperature Coefficient Of Input Offset Current (α_{IIO}) The ratio of the change in input offset current to the change in free-air temperature. This is an average value for the specified temperature range.

3

$$\alpha_{IIO} = \left| \frac{(I_{IO} @ T_{A(1)}) - (I_{IO} @ T_{A(2)})}{T_{A(1)} - T_{A(2)}} \right|$$ where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

Input Bias Current (I_{IB}) The average of the currents into the two input terminals with the output at zero volts.

Input Voltage Range (V_I) The range of voltage which if exceeded at either input terminal will cause the amplifier to cease functioning properly.

Maximum Peak-to-Peak Output Voltage Swing (V_{OPP}) The maximum peak-to-peak output voltage which can be obtained without waveform clipping when the quiescent d-c output voltage is zero.

Large-Signal Differential Voltage Amplification (A_{VD}) The ratio of the peak-to-peak output voltage swing to the change in differential input voltage required to drive the output.

Input Resistance (r_i) The resistance between the input terminals with either input grounded.

Output Resistance (r_o) The resistance between the output terminal and ground.

Common-Mode Rejection Ratio (CMRR) The ratio of differential voltage amplification to common-mode voltage amplification. This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.

Power Supply Sensitivity ($\Delta V_{IO}/\Delta V_{CC}$) The ratio of the change in input offset voltage to the change in supply voltages producing it. For these devices, both supply voltages are varied symmetrically.

Total Power Dissipation (P_D) The total d-c power supplied to the device less any power delivered from the device to a load. At no load: $P_D = V_{CC+} \cdot I_{CC+} + V_{CC-} \cdot I_{CC-}$.

Rise Time (t_r) The time required for an output voltage step to change from 10% to 90% of its final value.

Overshoot The quotient of: (1) the largest deviation of the output signal value from its steady-state value after a step-function change of the input signal, and (2) the difference between the output signal values in the steady state before and after the step-function change of the input signal.

Slew Rate (SR) The average time rate of change of the closed-loop amplifier output for a step-signal input. Slew rate is measured between specified output levels (0 and 10 volts for this device) with feedback adjusted for unity gain.

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TYPICAL CHARACTERISTICS
(unless designated maximum or minimum)

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

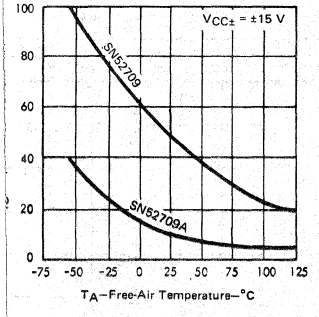


FIGURE 3

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

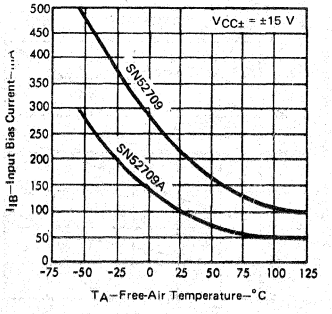


FIGURE 4

INPUT BIAS CURRENT
vs
SUPPLY VOLTAGE

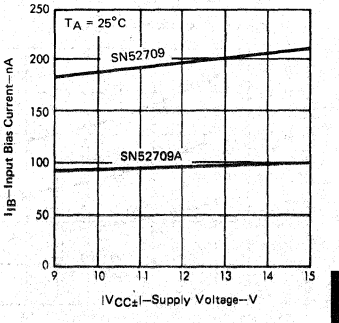


FIGURE 5

INPUT VOLTAGE RANGE
vs
SUPPLY VOLTAGE

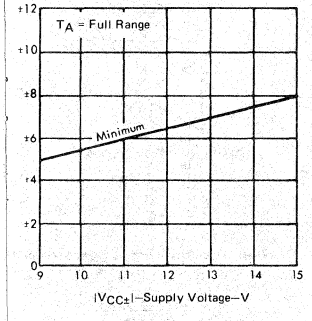


FIGURE 6

INPUT RESISTANCE
vs
FREE-AIR TEMPERATURE

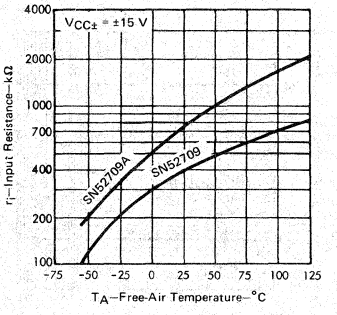


FIGURE 7

SN52709A
COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

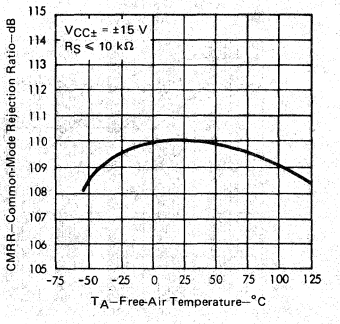


FIGURE 8

TOTAL POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

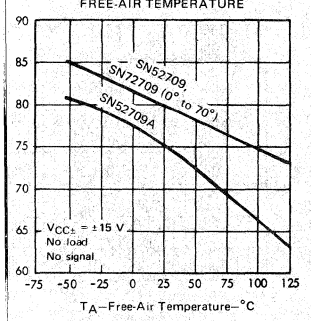


FIGURE 9

SN52709A
TOTAL POWER DISSIPATION
vs
SUPPLY VOLTAGE

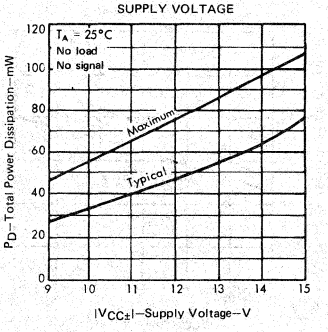


FIGURE 10

SN52709, SN72709
TOTAL POWER DISSIPATION
vs
SUPPLY VOLTAGE

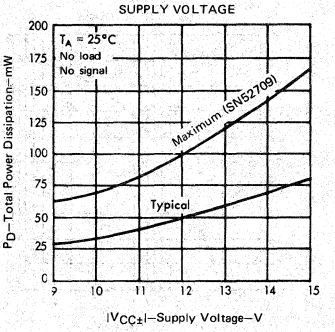


FIGURE 11

TYPICAL CHARACTERISTICS
(unless designated maximum or minimum)

OPEN-LOOP LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

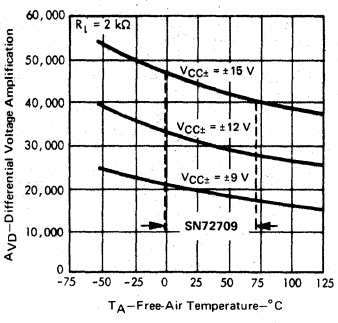


FIGURE 12

SN52709A, SN52709
OPEN-LOOP LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

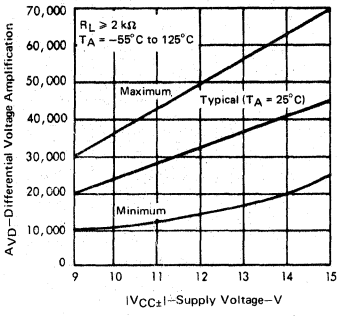


FIGURE 13

SN72709
OPEN-LOOP LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

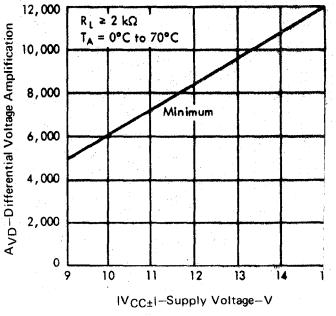


FIGURE 14

OPEN-LOOP LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREQUENCY

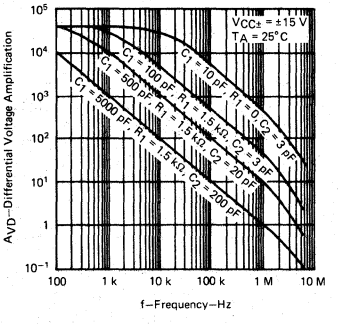


FIGURE 15

CLOSED-LOOP LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREQUENCY

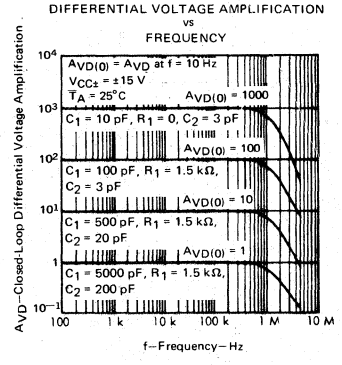
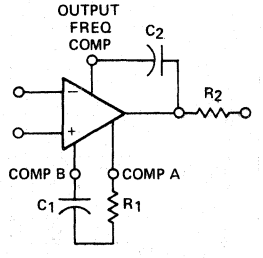


FIGURE 16



When the amplifier is operated with capacitive loading, R_2 = 50 Ω.

FREQUENCY COMPENSATION CIRCUIT FOR FIGURES 15, 16, AND 19

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs LOAD RESISTANCE

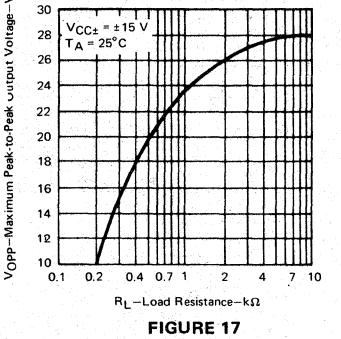


FIGURE 17

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs SUPPLY VOLTAGE

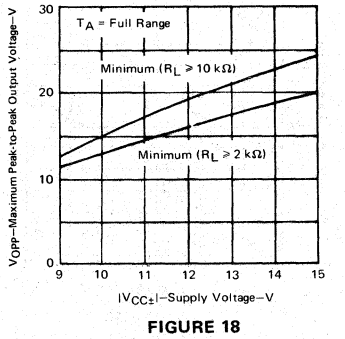


FIGURE 18

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

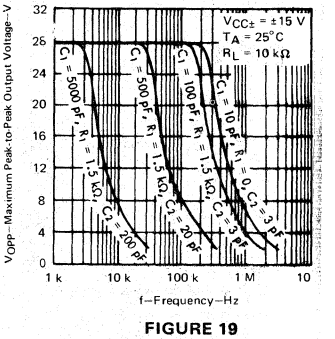


FIGURE 19

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TYPICAL CHARACTERISTICS

SN52709A, SN52709
VOLTAGE TRANSFER CHARACTERISTICS

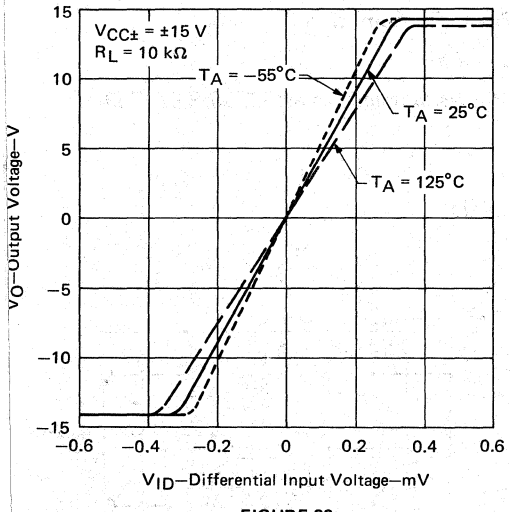


FIGURE 20

SN72709
VOLTAGE TRANSFER CHARACTERISTICS

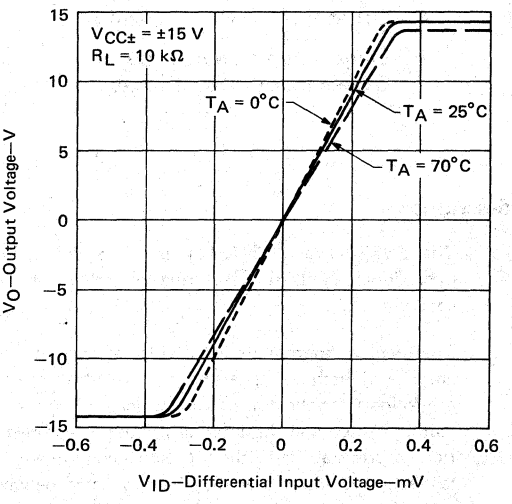


FIGURE 21

RELATIVE OUTPUT SWING vs ELAPSED TIME

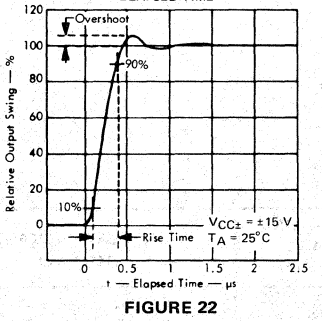


FIGURE 22

SLEW RATE vs CLOSED-LOOP DIFFERENTIAL VOLTAGE AMPLIFICATION

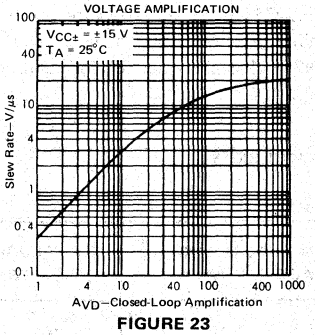


FIGURE 23

NORMALIZED FREQUENCY CHARACTERISTICS vs FREE-AIR TEMPERATURE

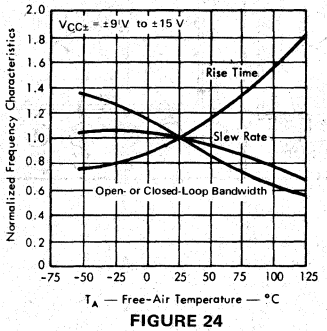


FIGURE 24

NORMALIZED FREQUENCY CHARACTERISTICS vs SUPPLY VOLTAGE

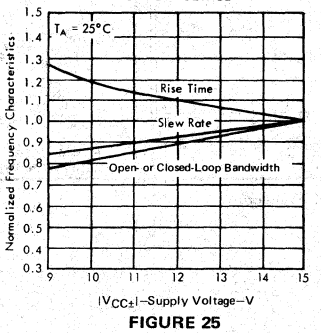


FIGURE 25

CIRCUIT TYPES SN52741, SN72741
HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

- Short-Circuit Protection
- Offset-Voltage Null Capability
- Large Common-Mode and Differential Voltage Ranges
- No Frequency Compensation Required
- Low Power Consumption
- No Latch-up
- Same Pin Assignments as SN52709/SN72709

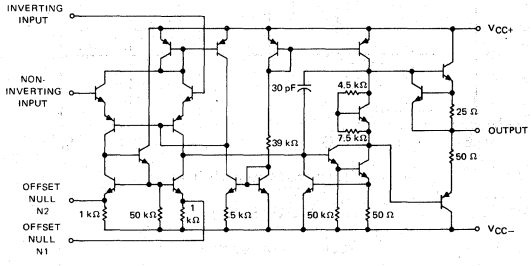
description

The SN52741 and SN72741 are high-performance operational amplifiers, featuring offset-voltage null capability.

The high common-mode input voltage range and the absence of latch-up make the amplifier ideal for voltage-follower applications. The devices are short-circuit protected and the internal frequency compensation ensures stability without external components. A low-value potentiometer may be connected between the offset null inputs to null out the offset voltage as shown in Figure 11.

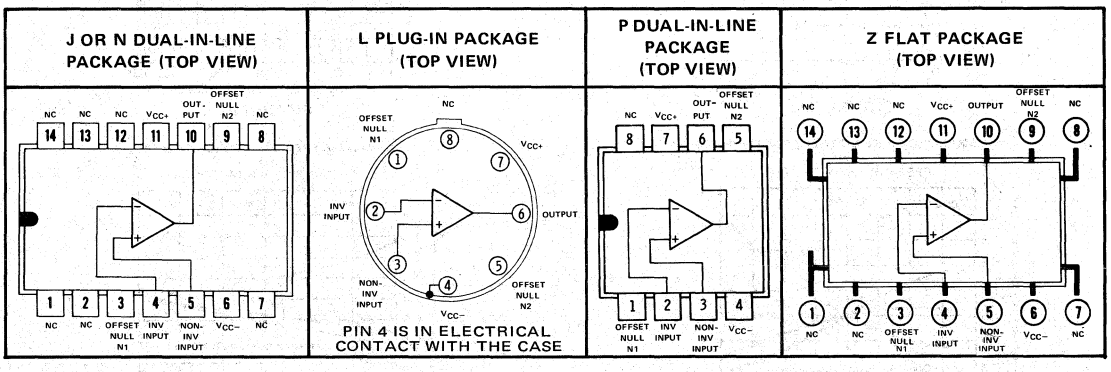
The SN52741 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN72741 is characterized for operation from 0°C to 70°C.

schematic



COMPONENT VALUES SHOWN ARE NOMINAL

terminal assignments



NC—No internal connection

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN52741	SN72741	UNIT
Supply voltage V_{CC+} (see Note 1)		22	18	V
Supply voltage V_{CC-} (see Note 1)		−22	−18	V
Differential input voltage (see Note 2)		±30	±30	V
Input voltage (either input, see Notes 1 and 3)		±15	±15	V
Voltage between either offset null terminal (N1/N2) and V_{CC-}		±0.5	±0.5	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	
Continuous total power dissipation at (or below) 55°C free-air temperature (see Note 5)		500	500	mW
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J, L, or Z Package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N or P Package	260	260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or either power supply. For the SN52741 only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.
5. For operation above 55°C free-air temperature, refer to Dissipation Derating Curve, Figure 12.

3

electrical characteristics at specified free-air temperature, V_{CC+} = 15 V, V_{CC-} = −15 V

PARAMETER		TEST CONDITIONS†		SN52741			SN72741			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S \leq 10$ kΩ	25°C		1	5		1	6	mV
			Full range			6			7.5	
$\Delta V_{IO(adj)}$	Offset voltage adjust range		25°C		±15			±15		mV
I_{IO}	Input offset current		25°C		20	200		20	200	nA
			Full range			500			300	
I_{IB}	Input bias current		25°C		80	500		80	500	nA
			Full range			1500			800	
V_I	Input voltage range		25°C	±12	±13		±12	±13		V
			Full range	±12			±12			
V_{OPP}	Maximum peak-to-peak output voltage swing	R_L = 10 kΩ	25°C	24	28		24	28		V
		$R_L \geq 10$ kΩ	Full range	24			24			
		R_L = 2 kΩ	25°C	20	26		20	26		
		$R_L \geq 2$ kΩ	Full range	20			20			
A_{VD}	Large-signal differential voltage amplification	$R_L \geq 2$ kΩ, V_O = ±10 V	25°C	50,000	200,000		20,000	200,000		
			Full range	25,000			15,000			
r_i	Input resistance		25°C	0.3	2		0.3	2		MΩ
r_o	Output resistance	V_O = 0 V, See Note 5	25°C		75			75		Ω
C_i	Input capacitance		25°C		1.4			1.4		pF
CMRR	Common-mode rejection ratio	$R_S \leq 10$ kΩ	25°C	70	90		70	90		dB
			Full range	70			70			
$\Delta V_{IO}/\Delta V_{CC}$	Power supply sensitivity	$R_S \leq 10$ kΩ	25°C		30	150		30	150	μV/V
			Full range			150			150	
I_{OS}	Short-circuit output current		25°C		±25	±40		±25	±40	mA
I_{CC}	Supply current	No load, No signal	25°C		1.7	2.8		1.7	2.8	mA
			Full range			3.3			3.3	
P_D	Total power dissipation	No load, No signal	25°C		50	85		50	85	mW
			Full range			100			100	

†All characteristics are specified under open-loop operation. Full range for SN52741 is −55°C to 125°C and for SN72741 is 0°C to 70°C.
NOTE 5: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

operating characteristics, V_{CC+} = 15 V, V_{CC-} = −15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	SN52741			SN72741			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	V_I = 20 mV, R_L = 2 kΩ,		0.3			0.3		μs
	Overshoot	C_L = 100 pF, See Figure 1		5%			5%		
SR	Slew rate at unity gain	V_I = 10 V, R_L = 2 kΩ, C_L = 100 pF, See Figure 1		0.5			0.5		V/μs

DEFINITION OF TERMS

Input Offset Voltage (V_{IO}) The d-c voltage which must be applied between the input terminals to force the quiescent d-c output voltage to zero. The input offset voltage may also be defined for the case where two equal resistances (R_S) are inserted in series with the input leads.

Input Offset Current (I_{IO}) The difference between the currents into the two input terminals with the output at zero volts.

Input Bias Current (I_{IB}) The average of the currents into the two input terminals with the output at zero volts.

Input Voltage Range (V_I) The range of voltage which, if exceeded at either input terminal, will cause the amplifier to cease functioning properly.

Maximum Peak-to-Peak Output Voltage Swing (V_{OPP}) The maximum peak-to-peak output voltage which can be obtained without waveform clipping when the quiescent d-c output voltage is zero.

Large-Signal Differential Voltage Amplification (A_{VD}) The ratio of the peak-to-peak output voltage swing to the change in differential input voltage required to drive the output.

Input Resistance (r_i) The resistance between the input terminals with either input grounded.

Output Resistance (r_o) The resistance between the output terminal and ground.

Input Capacitance (C_i) The capacitance between the input terminals with either input grounded.

Common-Mode Rejection Ratio (CMRR) The ratio of differential voltage amplification to common-mode voltage amplification. This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.

Power Supply Sensitivity ($\Delta V_{IO}/\Delta V_{CC}$) The ratio of the change in input offset voltage to the change in supply voltages producing it. For these devices, both supply voltages are varied symmetrically.

Short-Circuit Output Current (I_{OS}) The maximum output current available from the amplifier with the output shorted to ground or to either supply.

Total Power Dissipation (P_D) The total d-c power supplied to the device less any power delivered from the device to a load. At no load: $P_D = V_{CC+} \cdot I_{CC+} + V_{CC-} \cdot I_{CC-}$.

Rise Time (t_r) The time required for an output voltage step to change from 10% to 90% of its final value.

Overshoot The quotient of: (1) the largest deviation of the output signal value from its steady-state value after a step-function change of the input signal, and (2) the difference between the output signal values in the steady state before and after the step-function change of the input signal.

Slew Rate (SR) The average time rate of change of the closed-loop amplifier output voltage for a step-signal input. Slew rate is measured between specified output levels (0 and 10 volts for this device) with feedback adjusted for unity gain.

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PARAMETER MEASUREMENT INFORMATION

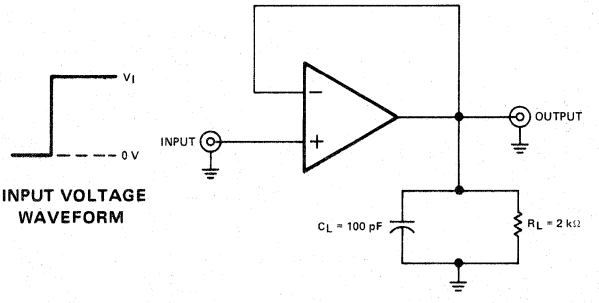


FIGURE 1–RISE TIME, OVERSHOOT, AND SLEW RATE

TYPICAL CHARACTERISTICS

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

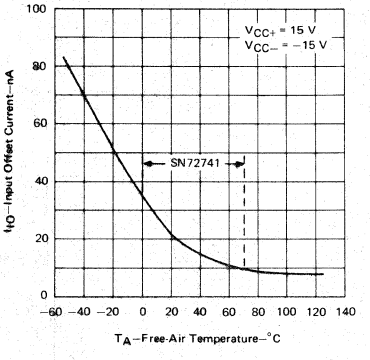


FIGURE 2

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

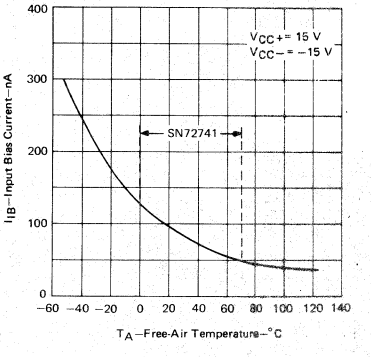


FIGURE 3

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
LOAD RESISTANCE

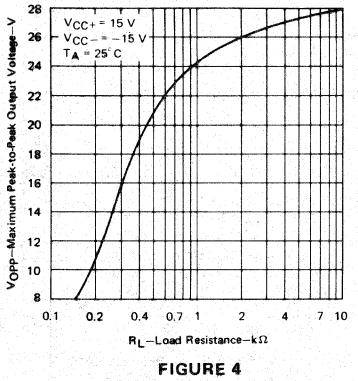


FIGURE 4

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

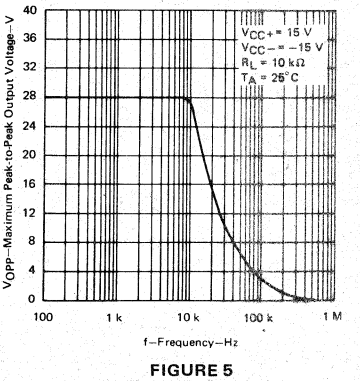


FIGURE 5

TYPICAL CHARACTERISTICS

OPEN-LOOP LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

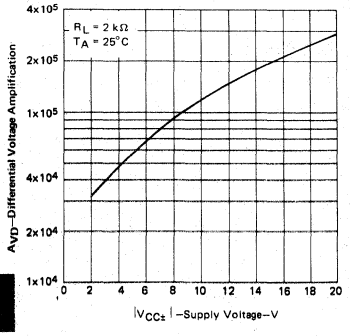


FIGURE 6

COMMON-MODE REJECTION RATIO vs FREQUENCY

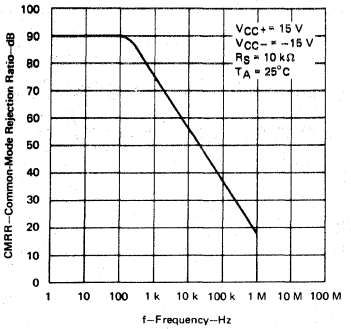


FIGURE 8

OPEN-LOOP LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREQUENCY

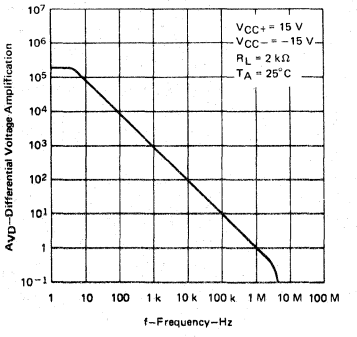


FIGURE 7

OUTPUT VOLTAGE vs ELAPSED TIME

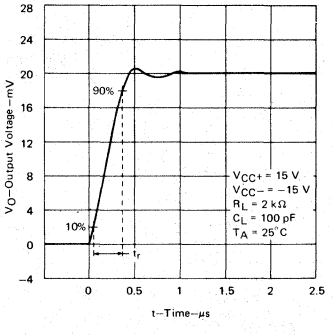


FIGURE 9

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

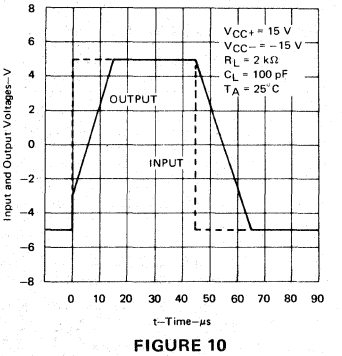


FIGURE 10

TYPICAL APPLICATION DATA

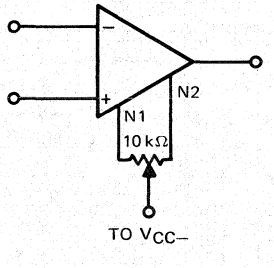
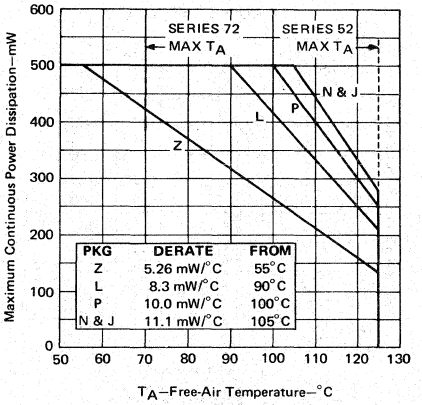


FIGURE 11–INPUT OFFSET VOLTAGE NULL CIRCUIT

THERMAL INFORMATION

DISSIPATION DERATING CURVE



PKG	DERATE	FROM
Z	5.26 mW/°C	55°C
L	8.3 mW/°C	90°C
P	10.0 mW/°C	100°C
N & J	11.1 mW/°C	105°C

FIGURE 12

TEXAS INSTRUMENTS
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- No frequency Compensation Required
- Low Power Consumption
- Short-Circuit Protection
- Offset-Voltage Null Capability
- Large Common-Mode and Differential Voltage Ranges
- No Latch-up
- Designed to be Interchangeable with Fairchild μA747 and μA747C

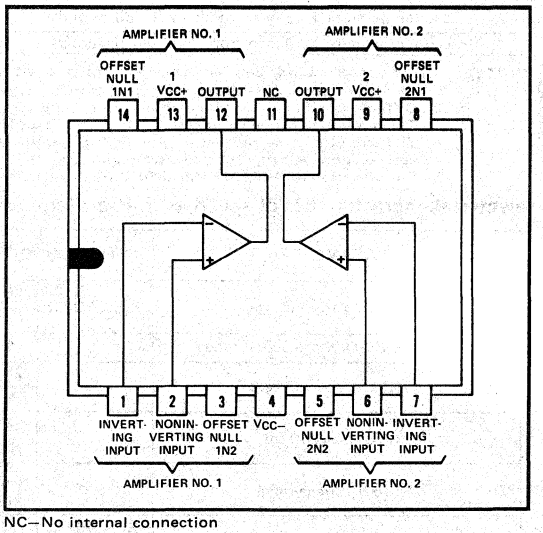
description

The SN52747 and SN72747 are dual high-performance operational amplifiers, featuring offset-voltage null capability. Each half is electrically similar to SN52741/SN72741.

The high common-mode input voltage range and the absence of latch-up make the amplifiers ideal for voltage-follower applications. The devices are short-circuit protected and the internal frequency compensation ensures stability without external components. A low-value potentiometer may be connected between the offset null inputs to null out the offset voltage as shown in Figure 3.

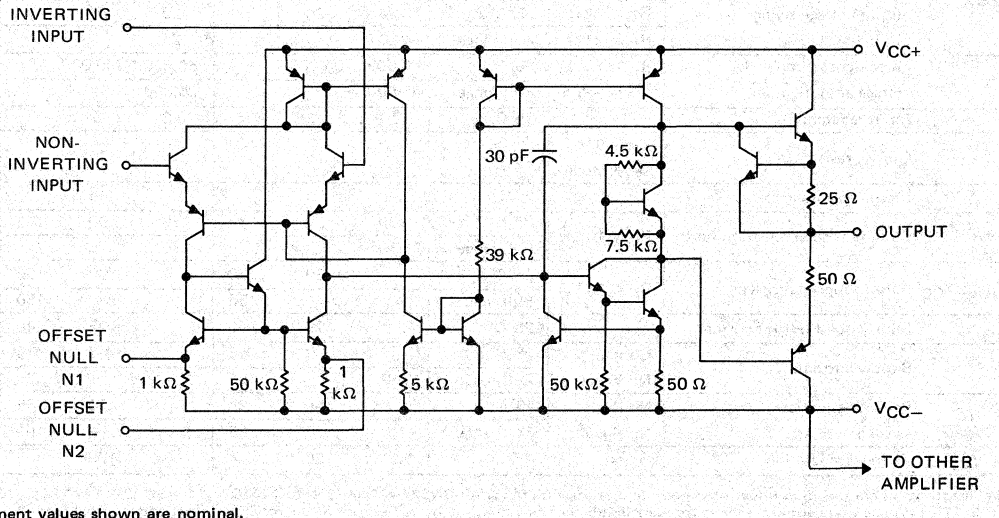
The SN52747 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN72747 is characterized for operation from 0°C to 70°C.

J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)



NC—No internal connection

schematic (each amplifier)



Component values shown are nominal.

CIRCUIT TYPES SN52747, SN72747
DUAL HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN52747	SN72747	UNIT
Supply voltage V_{CC+} (see Note 1)		22	18	V
Supply voltage V_{CC-} (see Note 1)		−22	−18	V
Differential input voltage (see Note 2)		±30	±30	V
Input voltage (either input, see Notes 1 and 3)		±15	±15	V
Voltage between either offset null terminal (N1/N2) and V_{CC-}		±0.5	±0.5	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	
Continuous total dissipation at (or below) 70°C free-air temperature (see Note 5)	Each amplifier	500	500	mW
	Total package	800	800	
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N package	260	260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or either power supply. For the SN52747 only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.
5. For operation of SN52747 above 70°C free-air temperature. refer to Dissipation Derating Curve, Figure 2.

electrical characteristics at specified free-air temperature, V_{CC+} = 15 V, V_{CC-} = −15 V

PARAMETER		TEST CONDITIONS†		SN52747			SN72747			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S \leq 10\ k\Omega$	25°C		1	5		1	6	mV
			Full range			6			7.5	
$\Delta V_{IO(adj)}$	Offset voltage adjust range		25°C		±15			±15		mV
I_{IO}	Input offset current		25°C		20	200		20	200	nA
			Full range			500			300	
I_{IB}	Input bias current		25°C		80	500		80	500	nA
			Full range			1500			800	
V_I	Input voltage range		25°C	±12	±13		±12	±13		V
			Full range	±12			±12			
V_{OPP}	Maximum peak-to-peak output voltage swing	R_L = 10 kΩ	25°C	24	28		24	28		V
		$R_L \geq$ 10 kΩ	Full range	24			24			
		R_L = 2 kΩ	25°C	20	26		20	26		
		$R_L \geq$ 2 kΩ	Full range	20			20			
A_{VD}	Large-signal differential voltage amplification	$R_L \geq$ 2 kΩ, V_O = ±10 V	25°C	50,000	200,000		50,000	200,000		
			Full range	25,000			25,000			
r_i	Input resistance		25°C	0.3	2		0.3	2		MΩ
r_o	Output resistance	V_O = 0 V, See Note 5	25°C		75			75		Ω
C_i	Input capacitance		25°C		1.4			1.4		pF
CMRR	Common-mode rejection ratio	$R_S \leq 10\ k\Omega$	25°C	70	90		70	90		dB
			Full range	70			70			
$\Delta V_{IO}/\Delta V_{CC}$	Power supply sensitivity	$R_S \leq 10\ k\Omega$	25°C		30	150		30	150	μV/V
			Full range			150			150	
I_{OS}	Short-circuit output current		25°C		±25	±40		±25	±40	mA
I_{CC}	Supply current	No load, No signal	25°C		1.7	2.8		1.7	2.8	mA
			Full range			3.3			3.3	
P_D	Power dissipation (each amplifier)	No load, No signal	25°C		50	85		50	85	mW
			Full range			100			100	
V_{o1}/V_{o2}	Channel separation		25°C		120			120		dB

† All characteristics are specified under open-loop operation. Full range for SN52747 is −55°C to 125°C and for SN72747 is 0°C to 70°C.
NOTE 5: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.
For definitions of terms, mechanical data, and ordering instructions, see the SN52741/SN72741 data sheet dated November 1970.

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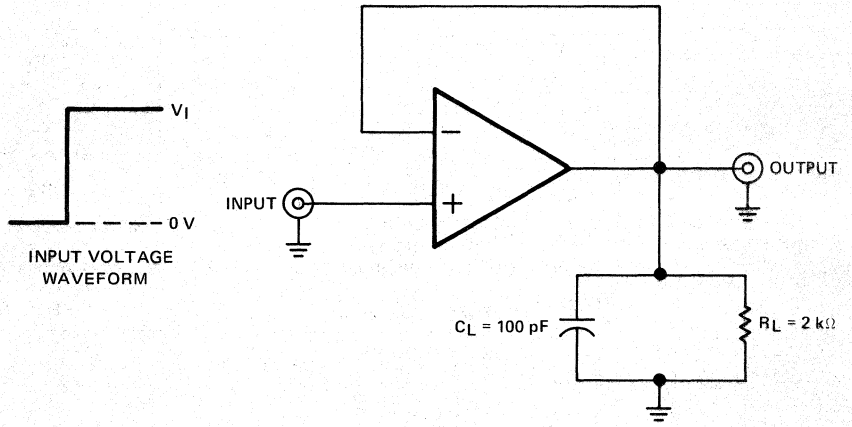
operating characteristics, V_{CC+} = 15 V, V_{CC-} = −15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	SN52747			SN72747			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	V_I = 20 mV, R_L = 2 kΩ,		0.3			0.3		μs
	Overshoot	C_L = 100 pF, See Figure 1		5%			5%		
SR	Slew rate at unity gain	V_I = 10 V, R_L = 2 kΩ, C_L = 100 pF, See Figure 1		0.5			0.5		V/μs

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

FIGURE 1–RISE TIME, OVERSHOOT, AND SLEW RATE

THERMAL INFORMATION

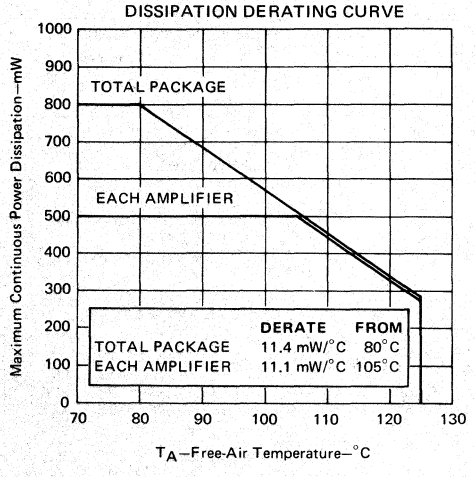


FIGURE 2

TYPICAL APPLICATION DATA

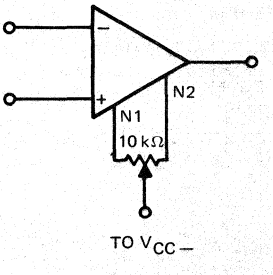


FIGURE 3–INPUT OFFSET VOLTAGE NULL CIRCUIT

TYPICAL CHARACTERISTICS

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

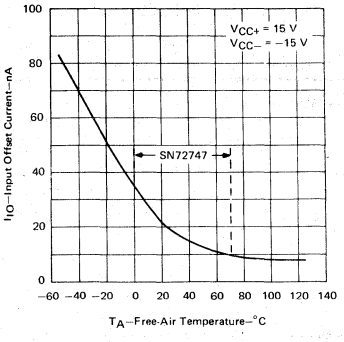


FIGURE 4

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

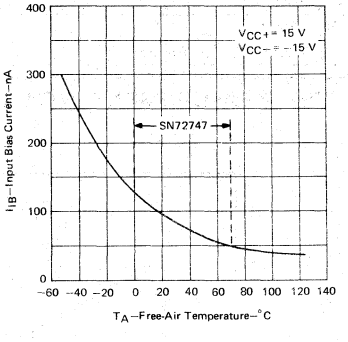


FIGURE 5

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE
vs
LOAD RESISTANCE

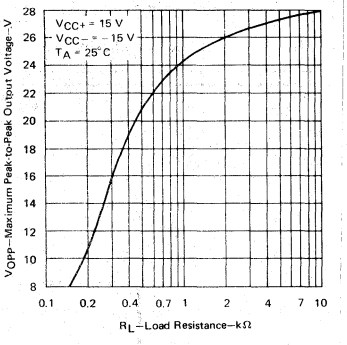


FIGURE 6

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE
vs
FREQUENCY

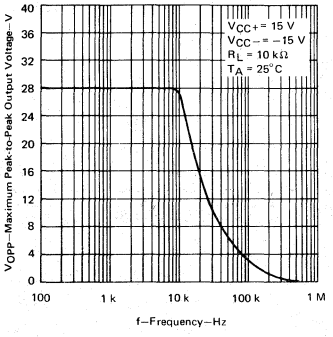


FIGURE 7

OPEN-LOOP LARGE-SIGNAL
DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

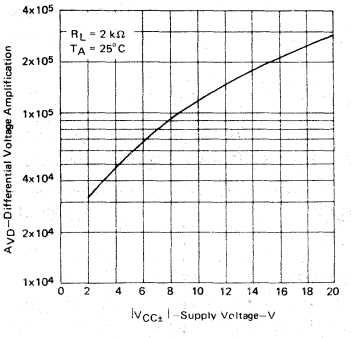


FIGURE 8

OPEN-LOOP LARGE-SIGNAL
DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
FREQUENCY

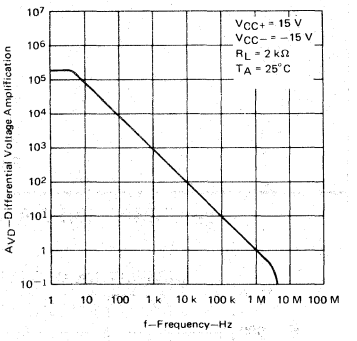


FIGURE 9

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

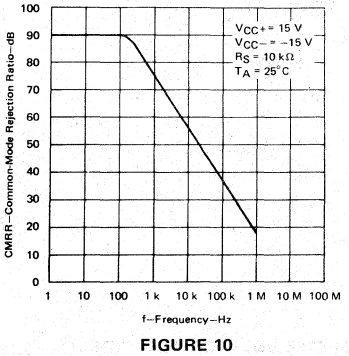


FIGURE 10

OUTPUT VOLTAGE
vs
ELAPSED TIME

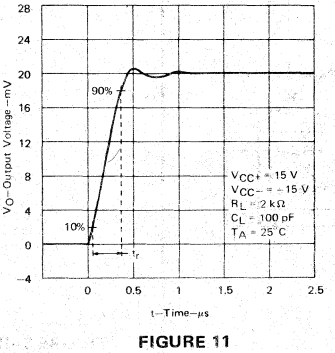


FIGURE 11

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

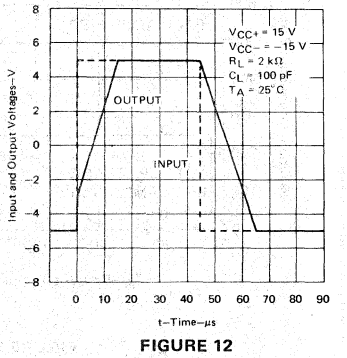


FIGURE 12

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CIRCUIT TYPES SN52748, SN72748
HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

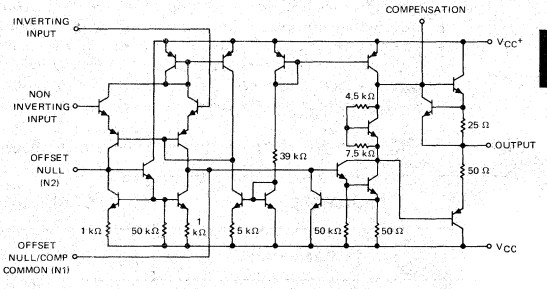
- Frequency and Transient Response Characteristics Adjustabie
- Short-Circuit Protection
- Offset-Voltage Null Capability
- Large Common-Mode and Differential Voltage Ranges
- Low Power Consumption
- No Latch-up
- Same Pin Assignments as SN52709/SN72709

description

The SN52748 and SN72748 are high-performance operational amplifiers. They offer the same advantages and desirable features as the SN52741 and SN72741 with the exception of internal compensation. The external compensation of the SN52748 and SN72748 allows the changing of the frequency response (when the closed-loop gain is greater than unity) for applications requiring wider bandwidth or higher slew rate. These circuits feature high gain, large differential and common-mode input voltage range, output short-circuit protection, and may be compensated under unity-gain conditions with a single 30-pF capacitor. A potentiometer may be connected between the offset null inputs, as shown in Figure 12, to null out the offset voltage.

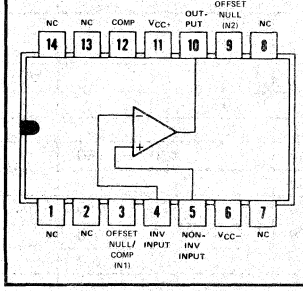
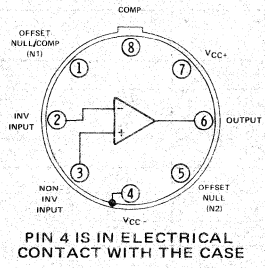
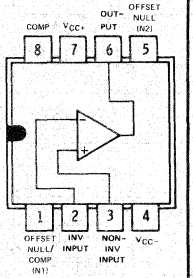
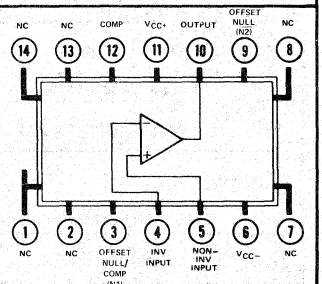
The SN52748 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN72748 is characterized for operation from 0°C to 70°C.

schematic



COMPONENT VALUES SHOWN ARE NOMINAL

terminal assignments

J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)	L PLUG-IN PACKAGE (TOP VIEW)	P DUAL-IN-LINE PACKAGE (TOP VIEW)	Z FLAT PACKAGE (TOP VIEW)
			

NC—No internal connection

CIRCUIT TYPES SN52748, SN72748
HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN52748	SN72748	UNIT
Supply voltage V_{CC+} (see Note 1)		22	18	V
Supply voltage V_{CC-} (see Note 1)		−22	−18	V
Differential input voltage (see Note 2)		±30	±30	V
Input voltage (either input, see Notes 1 and 3)		±15	±15	V
Voltage between either offset null terminal (N1/N2) and V_{CC-}		−0.5 to 2	−0.5 to 2	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	
Continuous total power dissipation at (or below) 55°C free-air temperature (see Note 5)		500	500	mW
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J, L, or Z Package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N or P Package	260	260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or either power supply. For the SN52748 only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.
5. For operation above 55°C free-air temperature, refer to Dissipation Derating Curve, Figure 13.

electrical characteristics at specified free-air temperature, V_{CC+} = 15 V, V_{CC-} = −15 V

PARAMETER		TEST CONDITIONS†		SN52748			SN72748			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S \leq 10$ kΩ	25°C		1	5		1	6	mV
			Full range			6			7.5	
I_{IO}	Input offset current		25°C		20	200		20	200	nA
			Full range			500			300	
I_{IB}	Input bias current		25°C		80	500		80	500	nA
			Full range			1500			800	
V_I	Input voltage range		25°C	±12	±13		±12	±13		V
			Full range	±12			±12			
V_{OPP}	Maximum peak-to-peak output voltage swing	R_L = 10 kΩ	25°C	24	28		24	28		V
		$R_L \geq$ 10 kΩ	Full range	24			24			
		R_L = 2 kΩ	25°C	20	26		20	26		
		$R_L \geq$ 2 kΩ	Full range	20			20			
A_{VD}	Large-signal differential voltage amplification	$R_L \geq$ 2 kΩ, V_O = ±10 V	25°C	50,000	200,000		50,000	200,000		
			Full range	25,000			25,000			
r_i	Input resistance		25°C	0.3	2		0.3	2		MΩ
r_o	Output resistance	V_O = 0 V, See Note 5	25°C		75			75		Ω
C_i	Input capacitance		25°C		1.4			1.4		pF
CMRR	Common-mode rejection ratio	$R_S \leq 10$ kΩ	25°C	70	90		70	90		dB
			Full range	70			70			
$\Delta V_{IO}/\Delta V_{CC}$	Power supply sensitivity	$R_S \leq 10$ kΩ	25°C		30	150		30	150	μV/V
			Full range			150			150	
I_{OS}	Short-circuit output current		25°C		±25	±40		±25	±40	mA
I_{CC}	Supply current	No load, No signal	25°C		1.7	2.8		1.7	2.8	mA
			Full range			3.3			3.3	
P_D	Total power dissipation	No load, No signal	25°C		50	85		50	85	mW
			Full range			100			100	

† All characteristics are specified under open-loop operation. Full range for SN52748 is −55°C to 125°C and for SN72748 is 0°C to 70°C.
NOTE 5: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

For definitions of terms, mechanical data, and ordering instructions, see SN52741/SN72741 data sheet dated November, 1970.

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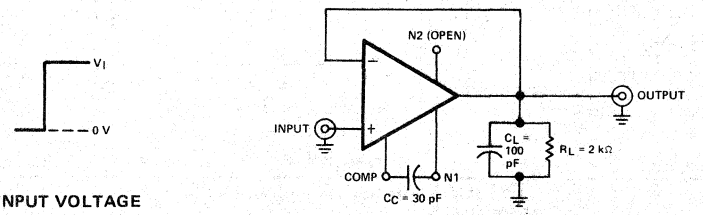
operating characteristics, V_{CC+} = 15 V, V_{CC-} = −15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	SN52748			SN72748			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	V_I = 20 mV, R_L = 2 kΩ, C_L = 100 pF, C_C = 30 pF, See Figure 1		0.3			0.3		μs
	Overshoot			5%			5%		
SR	Slew rate at unity gain	V_I = 10 V, R_L = 2 kΩ, C_L = 100 pF, C_C = 30 pF, See Figure 1		0.5			0.5		V/μs

PARAMETER MEASUREMENT INFORMATION



INPUT VOLTAGE WAVEFORM

TEST CIRCUIT

FIGURE 1—RISE TIME, OVERSHOOT, AND SLEW RATE

TYPICAL CHARACTERISTICS

INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

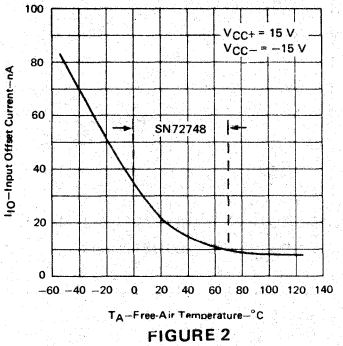


FIGURE 2

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

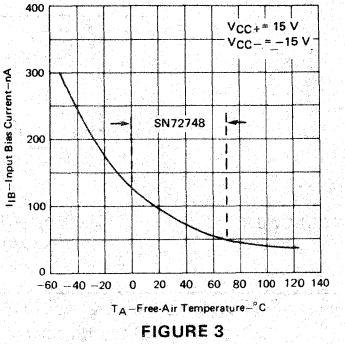


FIGURE 3

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs LOAD RESISTANCE

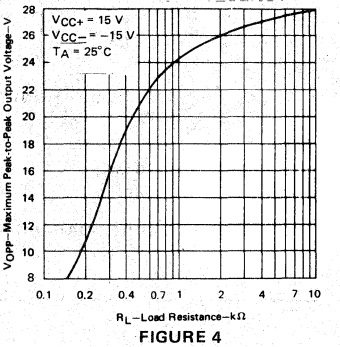


FIGURE 4

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

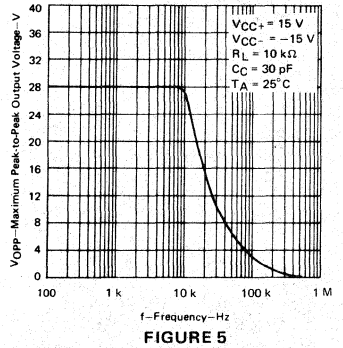


FIGURE 5

OPEN-LOOP LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

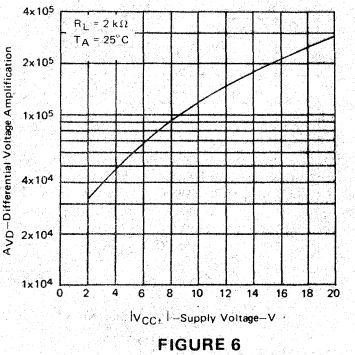


FIGURE 6

OPEN-LOOP LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREQUENCY

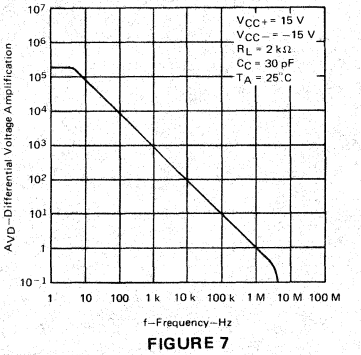


FIGURE 7

TYPICAL CHARACTERISTICS

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

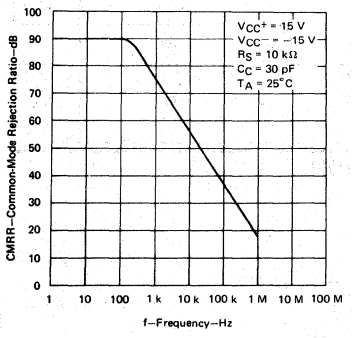


FIGURE 8

OUTPUT VOLTAGE
vs
ELAPSED TIME

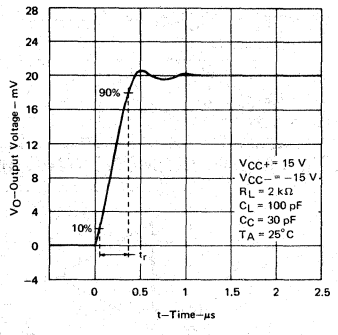


FIGURE 9

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

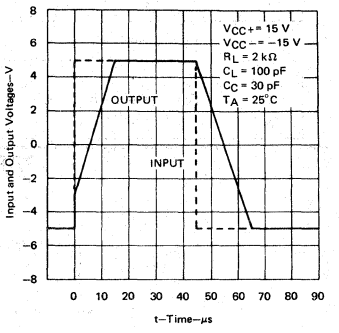
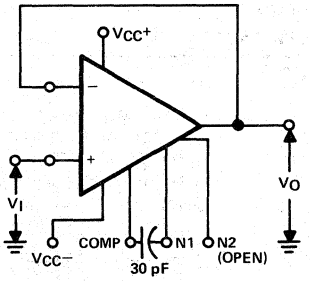


FIGURE 10

3

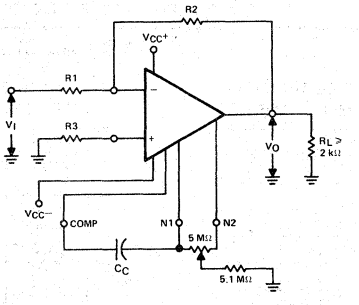
TYPICAL APPLICATION DATA



r_i = 400 MΩ,
C_i = 1 pF,

r_o < 1 Ω,
BW = 1 MHz

FIGURE 11–UNITY-GAIN VOLTAGE FOLLOWER



$$\frac{V_O}{V_I} = -\frac{R2}{R1}$$

$$C_C \geq \frac{R1 \cdot 30\ pF}{R1+R2}$$

$$R3 = \frac{R1 \cdot R2}{R1+R2}$$

FIGURE 12–INVERTING CIRCUIT WITH ADJUSTABLE GAIN, COMPENSATION, AND OFFSET ADJUSTMENT

THERMAL INFORMATION

DISSIPATION DERATING CURVE

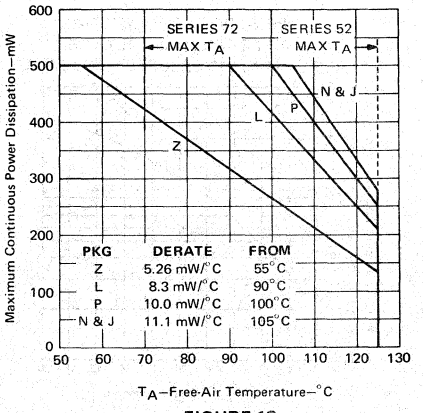


FIGURE 13

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CIRCUIT TYPES SN52770, SN7277
HIGH-PERFORMANCE OPERATIONAL AMPLIFIER

- Adjustable Frequency and Transient Response Characteristics
- Offset-Voltage Null Capability
- No Latch-Up
- Low Power Consumption
- High Slew Rates
- Very Low Input Bias Currents
- Very Low Input Offset Parameters
- Short-Circuit Protection
- Large Common-Mode and Differential Voltage Ranges

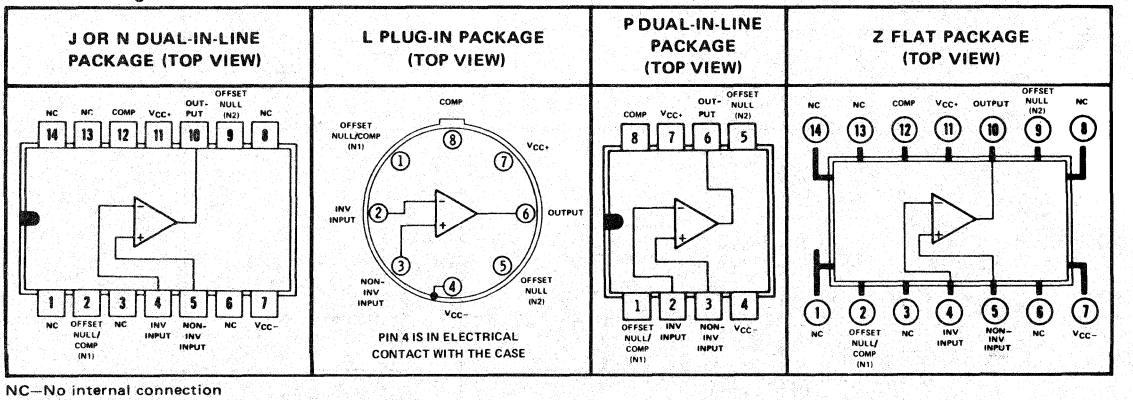
description

The SN52770 and SN72770 are high-performance general purpose integrated-circuit operational amplifiers. They offer the same advantages and desirable features as the SN52771 and SN72771 with the exception of internal compensation. The external compensation of the SN52770 and SN72770 allows the changing of the frequency response (when the closed-loop gain is greater than unity) for applications requiring wider bandwidth or higher slew rate. Unity-gain compensation is accomplished by means of a single 30-pF capacitor, and for higher gains, smaller capacitors may be used to obtain increased slew rate and bandwidth. High slew rate makes these amplifiers ideal for fast-rise-time signals, or large signals at high frequency. Very low input currents make them ideal for sample and hold, logarithmic amplifiers, and other low-level applications. A potentiometer may be connected between the offset null inputs, as shown in Figure 12, to null out the offset voltage.

The SN52770 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN72770 is characterized for operation from 0°C to 70°C.

3

terminal assignments



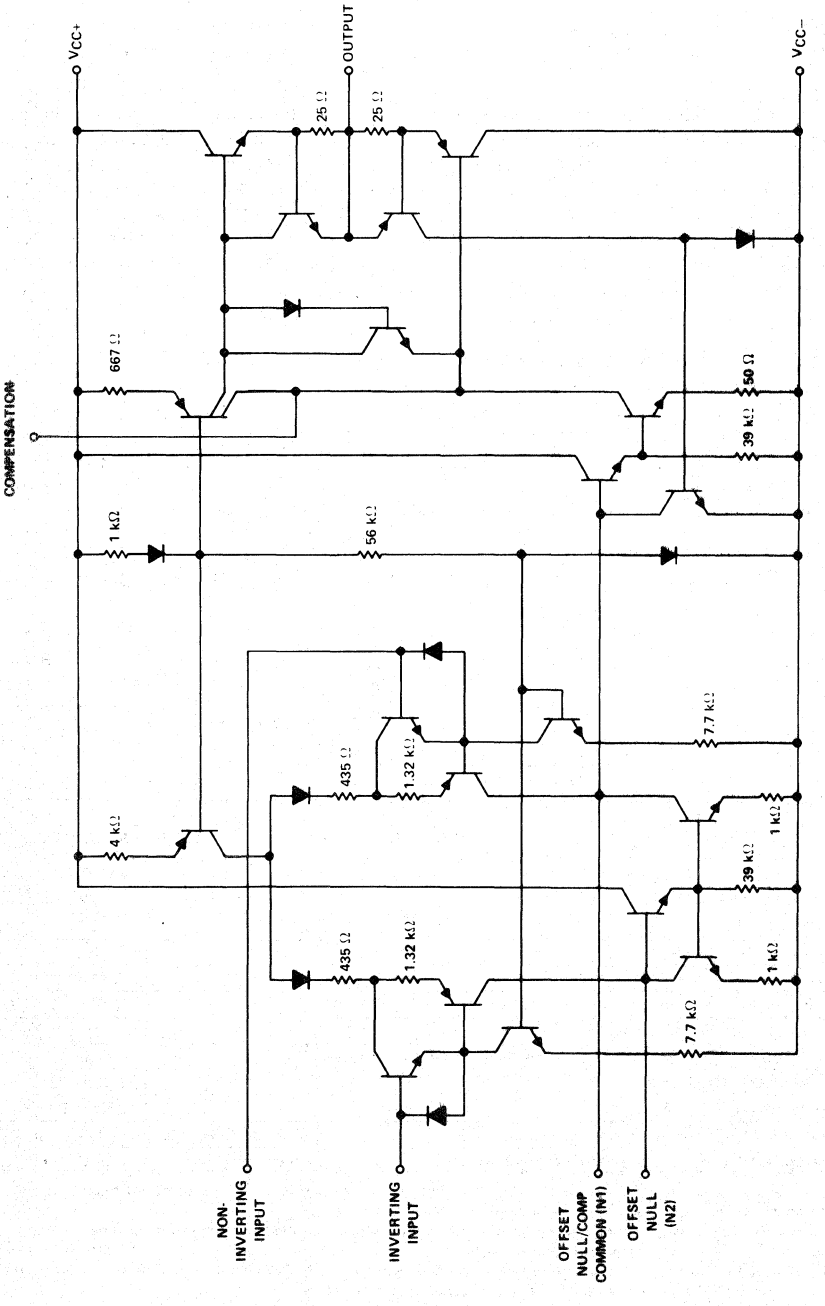
NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN52770	SN72770	UNIT
Supply voltage V_{CC+} (see Note 1)		22	18	V
Supply voltage V_{CC-} (see Note 1)		−22	−18	V
Differential input voltage (see Note 2)		±30	±30	V
Input voltage (either input, see Notes 1 and 3)		±15	±15	V
Voltage between either offset null terminal (N1/N2) and V_{CC-}		−0.5 to 2	−0.5 to 2	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	
Continuous total dissipation at (or below) 55°C free-air temperature (see Note 5)		500	500	mW
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J, L, or Z Package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N or P Package	260	260	°C

NOTES:
1. All voltage values, unless otherwise noted, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or either power supply. For the SN52770 only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.
5. For operation above 55°C free-air temperature, refer to Dissipation Derating Curve, Figure 1.

schematic



Component values shown are nominal.

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electrical characteristics at specified free-air temperature, V_{CC+} = 15 V, V_{CC-} = −15 V

PARAMETER		TEST CONDITIONS†		SN52770			SN72770			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S \leq 10\ k\Omega$	25°C		2	4		5	10	mV
			Full range			7			14	
I_{IO}	Input offset current		25°C		1	2		5	10	nA
			Full range			5			14	
I_{IB}	Input bias current		25°C		8	15		15	30	nA
			Full range			35			40	
V_{ICR}	Common-mode input voltage range		25°C	±12	±14		±11			V
V_{OPP}	Maximum peak-to-peak output voltage swing	$R_L = 2\ k\Omega$	25°C	24	26.5		22	26.5		
		$R_L \geq 2\ k\Omega$	Full range	24			22			
A_{VD}	Large-signal differential voltage amplification	$R_L = 2\ k\Omega$, $V_O = \pm 10$ V	25°C	50,000	100,000		35,000	100,000		
		$R_L \geq 2\ k\Omega$, $V_O = \pm 10$ V	Full range	25,000			25,000			
B_{OM}	Maximum-output-swing bandwidth (closed loop)	$R_L = 2\ k\Omega$, $V_O \geq \pm 10$ V, $A_{VD} = 1$, THD ≤ 5%	25°C		40			40		kHz
B_1	Unity-gain bandwidth		25°C		1.3			1.3		MHz
r_{id}	Differential input resistance		25°C		100			100		MΩ
z_{ic}	Common-mode input impedance	f = 10 Hz	25°C		500			500		MΩ
z_o	Output impedance	f = 10 Hz	25°C		2			2		kΩ
CMRR	Common-mode rejection ratio	$R_S \leq 10\ k\Omega$	25°C	80	100		70	100		dB
$\Delta V_{IO}/\Delta V_{CC}$	Power supply sensitivity	$R_S \leq 10\ k\Omega$	25°C		80	150			200	μV/V
e_n	Equivalent input noise voltage (closed loop)	$A_{VD} = 100$, BW = 1 Hz, f = 1 kHz	25°C		40			40		$nV/\sqrt{Hz}$
I_{OS}	Short-circuit output current	To V_{CC+}	25°C		24			24		mA
		To V_{CC-}			−20			−20		
I_{CC}	Supply current	No load, No signal	25°C		1.3	2		1.7	4	mA
P_D	Total power dissipation	No load, No signal	25°C		40	60		50	120	mW

†All characteristics are specified under open-loop operation unless otherwise noted. Full range for SN52770 is −55°C to 125°C and for SN72770 is 0°C to 70°C.

operating characteristics, V_{CC+} = 15 V, V_{CC-} = −15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	SN52770			SN72770			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	V_I = 200 mV, R_L = 2 kΩ, C_L = 200 pF, C_C = 30 pF, See Figure 2		130			130		ns
SR	Slew rate at unity gain	V_I = 10 V, R_L = 2 kΩ, C_L = 200 pF, C_C = 30 pF, See Figure 2		2.5			2.5		V/μs

DEFINITION OF TERMS

Input Offset Voltage (V_{IO}) The d-c voltage which must be applied between the input terminals to force the quiescent d-c output voltage to zero. The input offset voltage may also be defined for the case where two equal resistances (R_S) are inserted in series with the input leads.

Input Offset Current (I_{IO}) The difference between the currents into the two input terminals with the output at zero volts.

Input Bias Current (I_{IB}) The average of the currents into the two input terminals with the output at zero volts.

Common-Mode Input Voltage Range (V_{ICR}) The range of common-mode voltage which if exceeded will cause the amplifier to cease functioning properly.

Maximum Peak-to-Peak Output Voltage Swing (V_{OPP}) The maximum peak-to-peak output voltage which can be obtained without waveform clipping when the quiescent d-c output voltage is zero.

3

Large-Signal Differential Voltage Amplification (A_{VD}) The ratio of the peak-to-peak output voltage swing to the change in differential input voltage required to drive the output.

Maximum-Output-Swing Bandwidth (B_{OM}) The range of frequencies within which the maximum output voltage swing is above a specified value.

Unity-Gain Bandwidth (B_1) The range of frequencies within which the voltage amplification is greater than unity.

Differential Input Resistance (r_{id}) The small-signal resistance between the two ungrounded input terminals.

Common-Mode Input Impedance (z_{ic}) The parallel sum of the small-signal impedances between each input terminal and ground.

Output Impedance (z_o) The small-signal impedance between the output terminal and ground.

Common-Mode Rejection Ratio (CMRR) The ratio of differential voltage amplification to common-mode voltage amplification. This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.

Power Supply Sensitivity ($\Delta V_{IO}/\Delta V_{CC}$) The ratio of the change in input offset voltage to the change in supply voltages producing it. For these devices, both supply voltages are varied symmetrically.

Short-Circuit Output Current (I_{OS}) The maximum output current available from the amplifier with the output shorted to the specified supply.

Total Power Dissipation (P_D) The total d-c power supplied to the device less any power delivered from the device to a load. At no load: $P_D = V_{CC+} \cdot I_{CC+} + V_{CC-} \cdot I_{CC-}$.

Rise Time (t_r) The time required for an output voltage step to change from 10% to 90% of its final value.

Slew Rate (SR) The average time rate of change of the closed-loop amplifier output voltage for a step-signal input. Slew rate is measured between specified output levels (0 and 10 volts for this device) with feedback adjusted for unity gain.

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THERMAL INFORMATION

DISSIPATION DERATING CURVE

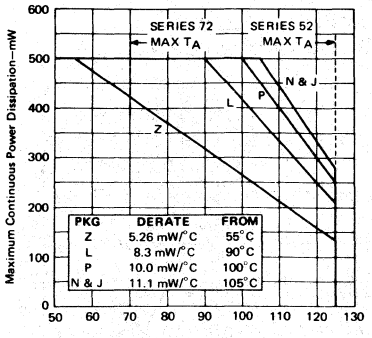
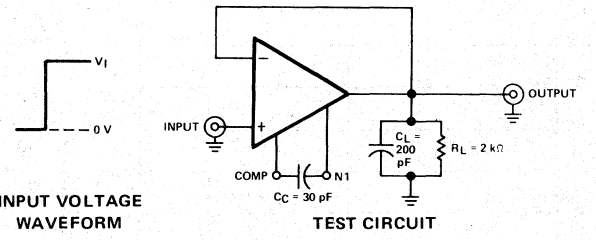


FIGURE 1

PARAMETER MEASUREMENT INFORMATION



INPUT VOLTAGE WAVEFORM

TEST CIRCUIT

FIGURE 2—BANDWIDTH, RISE TIME, AND SLEW RATE

3

TYPICAL CHARACTERISTICS

SN72770
COMMON-MODE INPUT VOLTAGE RANGE
vs
SUPPLY VOLTAGE

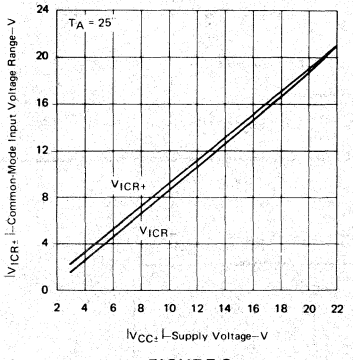


FIGURE 3

MAXIMUM OUTPUT VOLTAGE SWING
vs
SUPPLY VOLTAGE

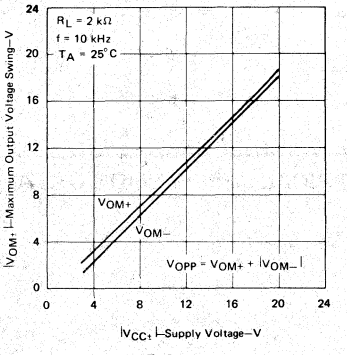


FIGURE 4

MAXIMUM PEAK-TO-PEAK OUTPUT
VOLTAGE SWING
vs
FREQUENCY

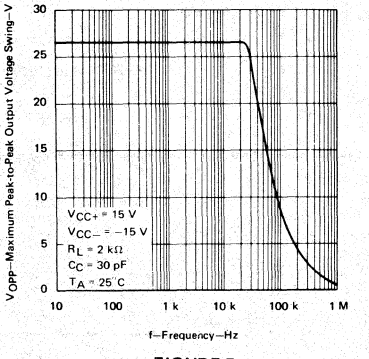


FIGURE 5

OPEN-LOOP LARGE-SIGNAL
DIFFERENTIAL VOLTAGE
AMPLIFICATION
vs
SUPPLY VOLTAGE

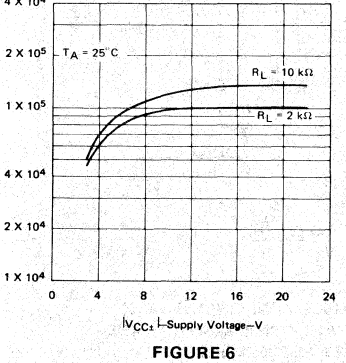


FIGURE 6

LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
FREQUENCY

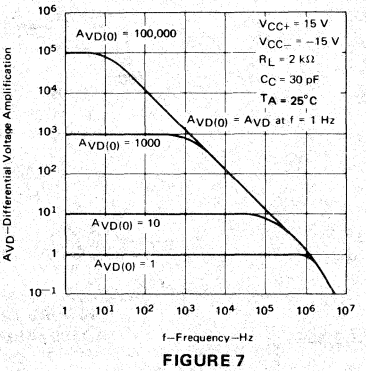


FIGURE 7

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

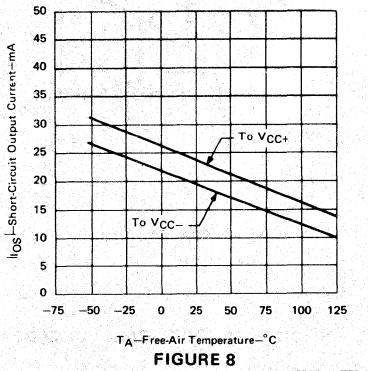


FIGURE 8

TYPICAL CHARACTERISTICS

TOTAL POWER DISSIPATION
vs
SUPPLY VOLTAGE

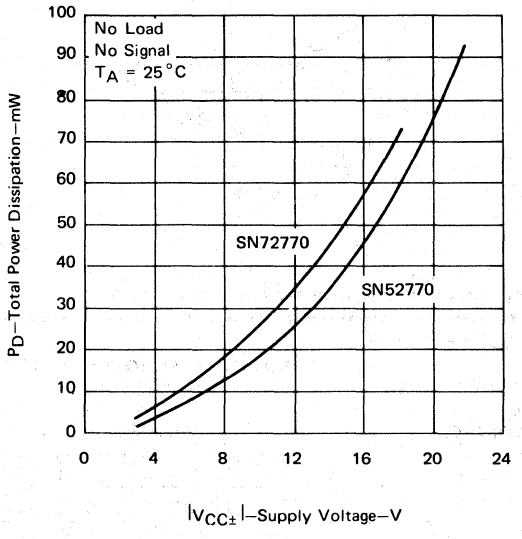


FIGURE 9

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

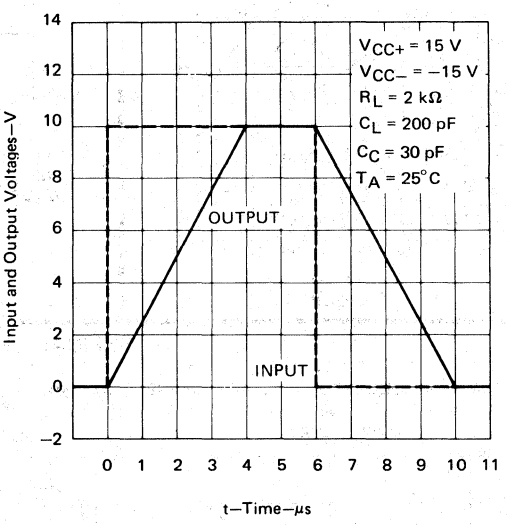
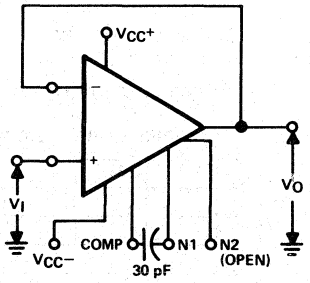


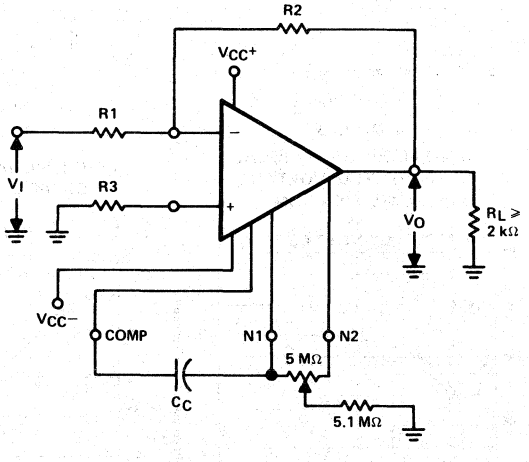
FIGURE 10

TYPICAL APPLICATION DATA



$r_i \approx 5{,}000$ MΩ at 10 Hz $r_o << 1$ Ω
$C_L \approx 1.5$ pF $B_1 \approx 1.3$ MHz

FIGURE 11–UNITY-GAIN VOLTAGE FOLLOWER



$$R3 = \frac{R1 \cdot R2}{R1 + R2} \qquad \frac{V_O}{V_1} = -\frac{R2}{R1} \qquad C_C \geq \frac{R1 \cdot 30\text{ pF}}{R1 + R2}$$

FIGURE 12–INVERTING CIRCUIT WITH ADJUSTABLE GAIN, COMPENSATION, AND OFFSET ADJUSTMENT

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CIRCUIT TYPES SN52771, SN72771
HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

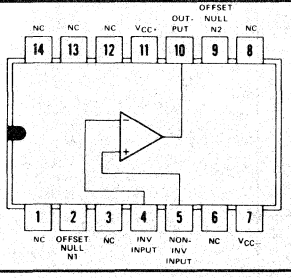
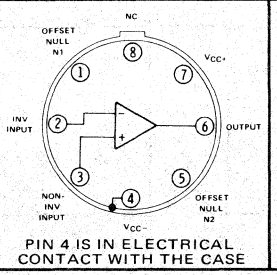
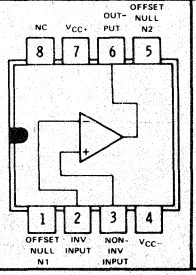
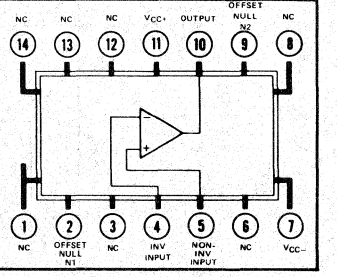
- Very Low Input Bias Currents
- 6-dB Roll-Off Insures Stability
- No Frequency Compensation Required
- Offset-Voltage Null Capability
- Low Power Consumption
- High Slew Rates
- Very Low Input Offset Parameters
- Short-Circuit Protection
- No Latch-Up
- Large Common-Mode and Differential Voltage Ranges

description

The SN52771 and SN72771 are high-performance general purpose integrated-circuit operational amplifiers. Very low input currents make these amplifiers ideal for sample and hold, logarithmic amplifiers, and other low-level applications. High slew rate makes them ideal for fast-rise-time signals, or large signals at high frequency. Internal compensation provides a 6-dB roll-off for stability under all closed-loop conditions. A potentiometer may be connected between the offset null inputs, as shown in Figure 11, to null out the offset voltage.

The SN52771 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN72771 is characterized for operation from 0°C to 70°C.

terminal assignments

J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)	L PLUG-IN PACKAGE (TOP VIEW)	P DUAL-IN-LINE PACKAGE (TOP VIEW)	Z FLAT PACKAGE (TOP VIEW)
			

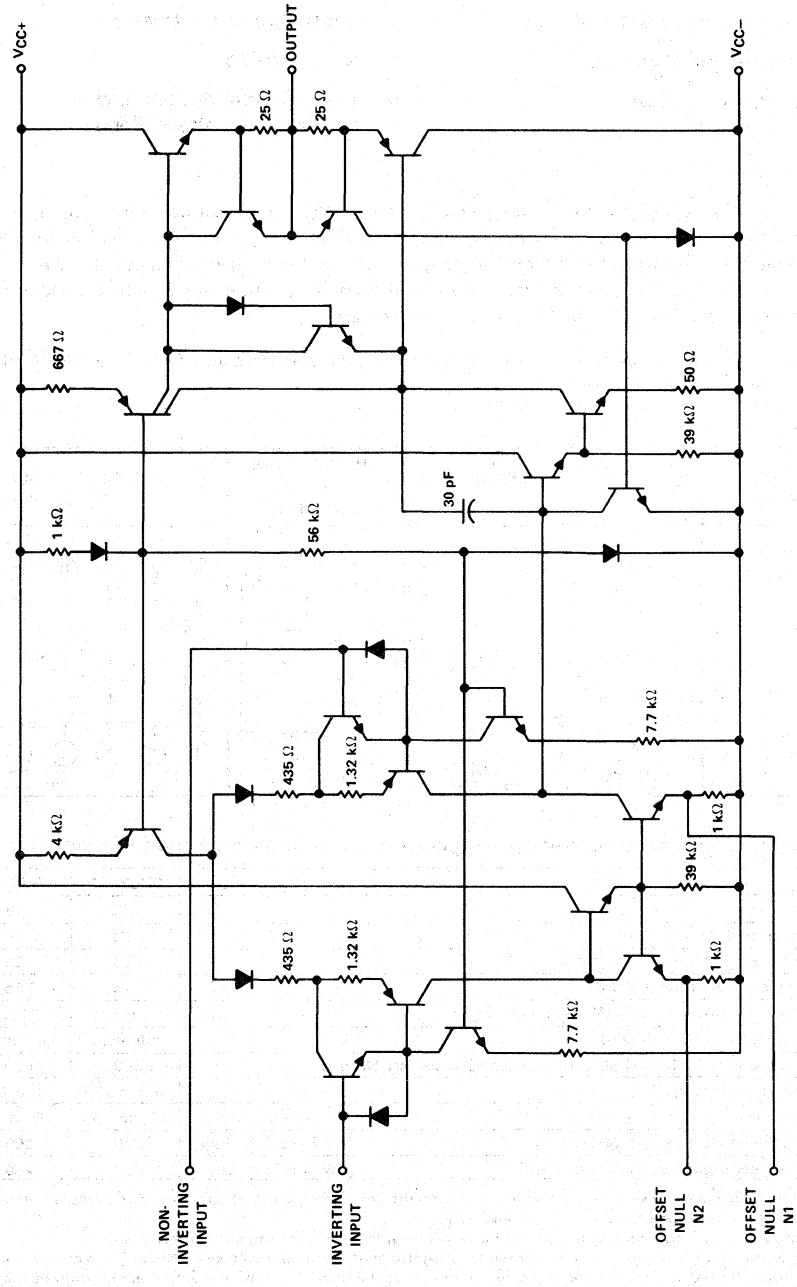
NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN52771	SN72771	UNIT
Supply voltage V_{CC+} (see Note 1)		22	18	V
Supply voltage V_{CC-} (see Note 1)		−22	−18	V
Differential input voltage (see Note 2)		±30	±30	V
Input voltage (either input, see Notes 1 and 3)		±15	±15	V
Voltage between either offset null terminal (N1/N2) and V_{CC-}		±0.5	±0.5	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	
Continuous total dissipation at (or below) 55°C free-air temperature (see Note 5)		500	500	mW
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J, L, or Z Package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N or P Package	260	260	°C

NOTES:
1. All voltage values, unless otherwise noted, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or either power supply. For the SN52771 only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.
5. For operation above 55°C free-air temperature, refer to Dissipation Derating Curve, Figure 1.

schematic



Component values shown are nominal.

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electrical characteristics at specified free-air temperature, V_{CC+} = 15 V, V_{CC-} = −15 V

PARAMETER		TEST CONDITIONS†		SN52771			SN72771			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S \leq 10$ kΩ	25°C		2	4		5	10	mV
			Full range			7			14	
I_{IO}	Input offset current		25°C		1	2		5	10	nA
			Full range			5			14	
I_{IB}	Input bias current		25°C		8	15		15	30	nA
			Full range			35			40	
V_{ICR}	Common-mode input voltage range		25°C	±12	±14		±11			V
V_{OPP}	Maximum peak-to-peak output voltage swing	R_L = 2 kΩ	25°C	24	26.5		22	26.5		
		$R_L \geq$ 2 kΩ	Full range	24			22			
A_{VD}	Large-signal differential voltage amplification	R_L = 2 kΩ, V_O = ±10 V	25°C	50,000	100,000		35,000	100,000		
		$R_L \geq$ 2 kΩ, V_O = ±10 V	Full range	25,000			25,000			
B_{OM}	Maximum-output-swing bandwidth (closed loop)	R_L = 2 kΩ, $V_O \geq$ ±10 V, A_{VD} = 1, THD ≤ 5%	25°C		40			40		kHz
B_1	Unity-gain bandwidth		25°C		1.3			1.3		MHz
r_{id}	Differential input resistance		25°C		100			100		MΩ
z_{ic}	Common-mode input impedance	f = 10 Hz	25°C		500			500		MΩ
z_o	Output impedance	f = 10 Hz	25°C		2			2		kΩ
CMRR	Common-mode rejection ratio	$R_S \leq$ 10 kΩ	25°C	80	100		70	100		dB
$\Delta V_{IO}/\Delta V_{CC}$	Power supply sensitivity	$R_S \leq$ 10 kΩ	25°C		80	150			200	μV/V
e_n	Equivalent input noise voltage (closed loop)	A_{VD} = 100, BW = 1 Hz, f = 1 kHz	25°C		40			40		nV/√Hz
I_{OS}	Short-circuit output current	To V_{CC+}	25°C		24			24		mA
		To V_{CC-}			−20			−20		
I_{CC}	Supply current	No load, No signal	25°C		1.3	2		1.7	4	mA
P_D	Total power dissipation	No load, No signal	25°C		40	60		50	120	mW

†All characteristics are specified under open-loop operation unless otherwise noted. Full range for SN52771 is −55°C to 125°C and for SN72771 is 0°C to 70°C.

operating characteristics, V_{CC+} = 15 V, V_{CC-} = −15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	SN52771			SN72771			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	V_I = 200 mV, R_L = 2 kΩ, C_L = 200 pF, C_C = 30 pF, See Figure 2		130			130		ns
SR	Slew rate at unity gain	V_I = 10 V, R_L = 2 kΩ, C_L = 200 pF, C_C = 30 pF, See Figure 2		2.5			2.5		V/μs

For ordering instructions and mechanical data, refer to Section 1.

DEFINITION OF TERMS

Input Offset Voltage (V_{IO}) The d-c voltage which must be applied between the input terminals to force the quiescent d-c output voltage to zero. The input offset voltage may also be defined for the case where two equal resistances (R_S) are inserted in series with the input leads.

Input Offset Current (I_{IO}) The difference between the currents into the two input terminals with the output at zero volts.

Input Bias Current (I_{IB}) The average of the currents into the two input terminals with the output at zero volts.

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Maximum Peak-to-Peak Output Voltage Swing (V_{OPP}) The maximum peak-to-peak output voltage which can be obtained without waveform clipping when the quiescent d-c output voltage is zero.

Large-Signal Differential Voltage Amplification (A_{VD}) The ratio of the peak-to-peak output voltage swing to the change in differential input voltage required to drive the output.

Maximum-Output-Swing Bandwidth (B_{OM}) The range of frequencies within which the maximum output voltage swing is above a specified value.

Unity-Gain Bandwidth (B_1) The range of frequencies within which the voltage amplification is greater than unity.

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Output Impedance (z_o) The impedance between the output terminal and ground.

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Rise Time (t_r) The time required for an output voltage step to change from 10% to 90% of its final value.

Slew Rate (SR) The average time rate of change of the closed-loop amplifier output voltage for a step-signal input. Slew rate is measured between specified output levels (0 and 10 volts for this device) with feedback adjusted for unity gain.

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THERMAL INFORMATION

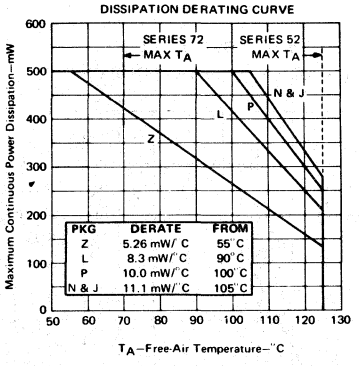


FIGURE 1

PARAMETER MEASUREMENT INFORMATION

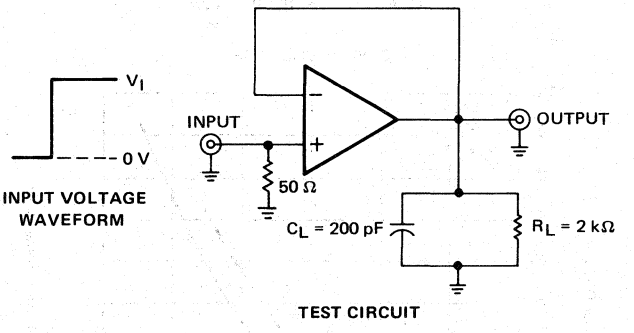


FIGURE 2—BANDWIDTH, RISE TIME, AND SLEW RATE

3

TYPICAL CHARACTERISTICS

SN52771

COMMON-MODE INPUT VOLTAGE RANGE vs SUPPLY VOLTAGE

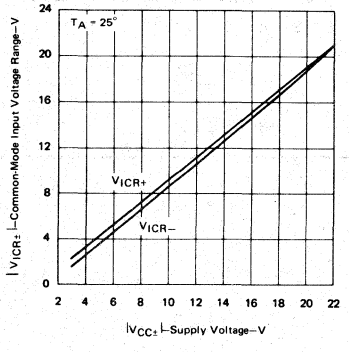


FIGURE 3

MAXIMUM OUTPUT VOLTAGE SWING vs SUPPLY VOLTAGE

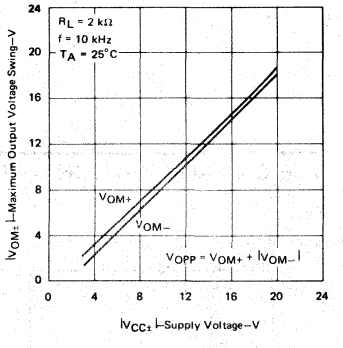


FIGURE 4

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE SWING vs FREQUENCY

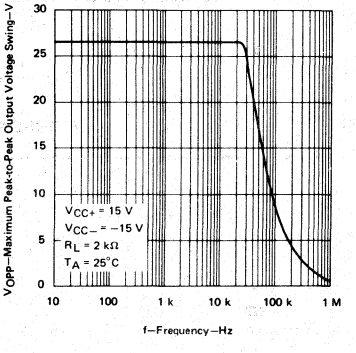


FIGURE 5

OPEN-LOOP LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

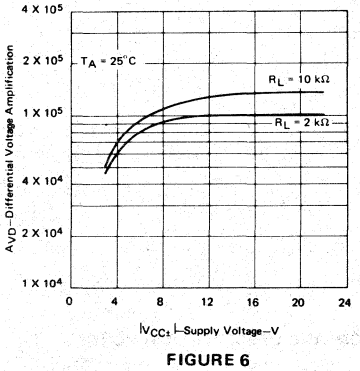


FIGURE 6

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREQUENCY

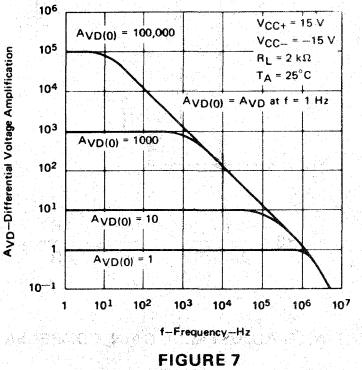


FIGURE 7

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

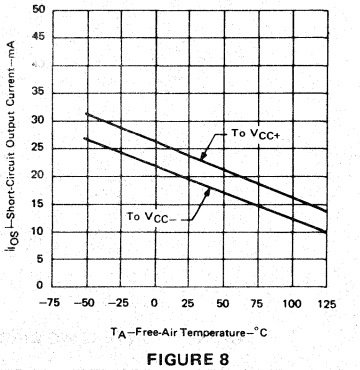


FIGURE 8

TYPICAL CHARACTERISTICS

TOTAL POWER DISSIPATION
vs
SUPPLY VOLTAGE

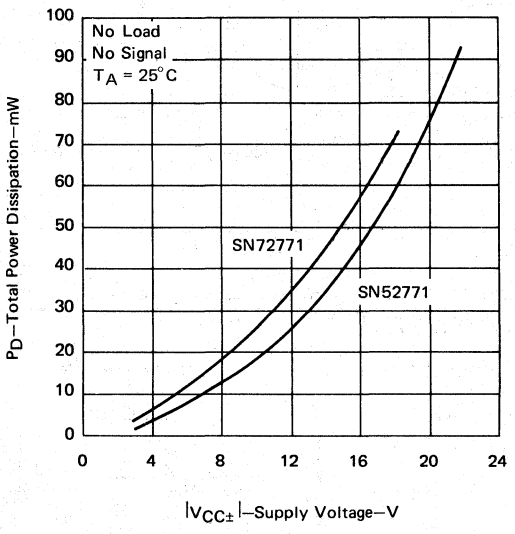


FIGURE 9

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

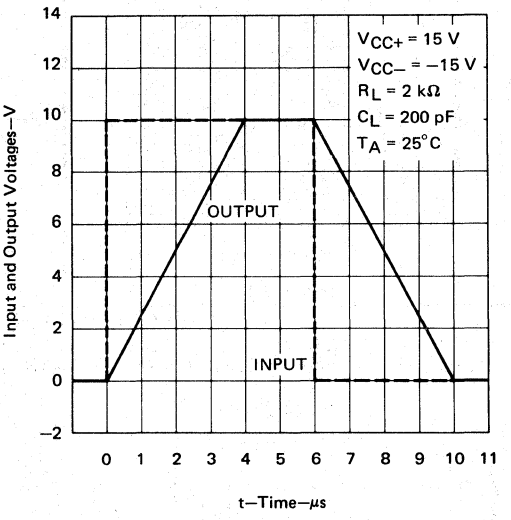
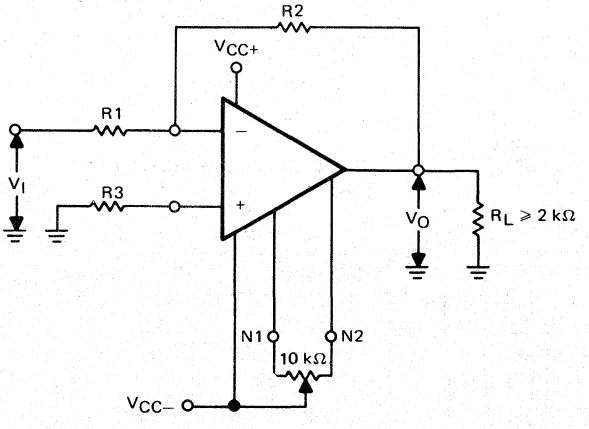


FIGURE 10

TYPICAL APPLICATION DATA



$$R3 = \frac{R1 \cdot R2}{R1 + R2} \qquad \frac{V_O}{V_I} = -\frac{R2}{R1}$$

FIGURE 11–INVERTING CIRCUIT WITH ADJUSTABLE GAIN, COMPENSATION, AND OFFSET ADJUSTMENT

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Series 52 and Series 55

TYPE	SINGLE				DUAL CHANNEL		DUAL				UNIT
	SN52710	SN52510	SN52810	SN52106*	SN52711	SN52811	SN52820	SN52514	SN52506*	SN55107A†	
Input Offset Voltage, Max	5	2	2	2	3.5	3.5	2	2	2	25	mV
Input Offset Current, Max	10	3	3	3	10	3	3	3	3	10	μA
Input Bias Current, Max	75	15	15	20	75	20	15	15	20	75	μA
Voltage Amplification, Min	750	12,500	12,500	40,000 Typ	750	12,500	12,500	12,500	40,000 Typ		
Common-Mode Input Voltage Range, Min	±5	±5	±5	±5	±5	±5	±5	±5	±5	±3	V
Output Sink Current, Min	1.6	2	2	100 Typ	0.5	0.5	2	2	100 Typ	16	mA
Input-Output Response Time, Typ	40	30	30	40	40	33	30	30	40	17	ns
Fan-Out to Series 54 TTL	1	1	1	10	1	1	1	1	10	10	
Power Supplies Required	12	12	12	12	12	12	12	12	12	5	V_{CC+}
	6	6	6	3 to 12	6	6	6	6	3 to 12	5	V_{CC-}
Packages	J, L, N, S	J, L, N, P, Z	J, L, N, P, Z	J, L, N, Z	J, L, N, S	J, L, N	J, N, Z	J, N, Z	N, J, Z	J, N	

3

Series 72 and Series 75

TYPE	SINGLE				DUAL CHANNEL		DUAL					UNIT
	SN72710	SN72510	SN72810	SN72306*	SN72711	SN72811	SN72720	SN72820	SN72514	SN72506*	SN75107A†	
Input Offset Voltage, Max	7.5	3.5	5	5	5	5	7.5	3.5	3.5	5	25	mV
Input Offset Current, Max	15	5	5	5	15	5	15	5	5	5	10	μA
Input Bias Current, Max	100	20	20	25	100	30	100	20	20	25	75	μA
Voltage Amplification, Min	700	10,000	10,000	40,000 Typ	700	10,000	700	10,000	10,000	40,000 Typ		
Common-Mode Input Voltage Range, Min	±5	±5	±5	±5	±5	±5	±5	±5	±5	±5	±3	V
Output Sink Current, Min	1.6	1.6	1.6	100 Typ	0.5	0.5		1.6	1.6	100	16	mA
Input-Output Response Time, Typ	40	30	30	40	40	33	40	30	30	40	17	ns
Fan-Out to Series 74 TTL	1	1	1	10	1	1	1	1	1	10	10	
Power Supplies Required	12	12	12	12	12	12	12	12	12	12	5	V_{CC+}
	6	6	6	3 to 12	6	6	6	6	6	3 to 12	5	V_{CC-}
Packages	J, L, N, S	J, L, N, P, Z	J, L, N, P, Z	J, L, N, Z	J, L, N, S	J, L, N	N	J, N, Z	J, N, Z	J, N, Z	J, N	

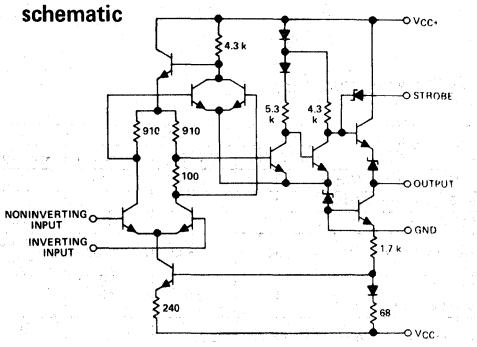
*To be announced soon

†Data sheet in the line circuits section.

CIRCUIT TYPES SN52510, SN72510 DIFFERENTIAL COMPARATORS WITH STROBE

- Low Offset Characteristics
- High Differential Voltage Amplification
- Fast Response Times
- Output Compatible with Most TTL and DTL Circuits

schematic



Resistor values are nominal in ohms.

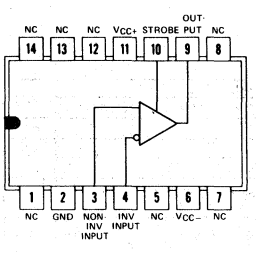
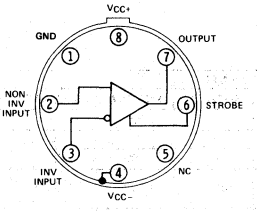
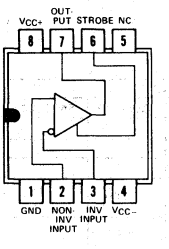
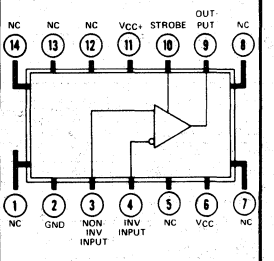
description

The SN52510 and SN72510 monolithic high-speed voltage comparators are improved versions of the SN52710 and SN72710 with an extra stage added to increase voltage amplification and accuracy, and a strobe input for greater flexibility. Typical voltage amplification is 33,000. Since the output cannot be more positive than the strobe, a low-level input at the strobe will cause the output to go low regardless of the differential input. Component matching, inherent in integrated circuit fabrication techniques, produces a comparator with low-drift and low-offset characteristics. These circuits are particularly useful for applications requiring an amplitude discriminator, memory sense amplifier, or a high-speed limit detector.

3

The SN52510 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN72510 is characterized for operation from 0°C to 70°C.

terminal assignments

J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)	L PLUG-IN PACKAGE (TOP VIEW)	P DUAL-IN-LINE PACKAGE (TOP VIEW)	Z FLAT PACKAGE (TOP VIEW)
	 PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE		

NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1)	14 V
Supply voltage V_{CC-} (see Note 1)	−7 V
Differential input voltage (see Note 2)	±5 V
Input voltage (either input, see Note 1)	±7 V
Strobe Voltage (see Note 1)	6 V
Peak output current ($t_W \leq 1$ s)	10 mA
Continuous total power dissipation at (or below) 70°C free-air temperature (see Note 3)	300 mW
Operating free-air temperature range: SN52510 Circuits	−55°C to 125°C
SN72510 Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J, L, or Z package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N or P package	260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. For operation of the SN52510 above 70°C free-air temperature, refer to Dissipating Derating Curve, Figure 13.

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electrical characteristics at specified free-air temperature, V_{CC+} = 12 V, V_{CC-} = −6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN52510			SN72510			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S \leq 200\ \Omega$, See Note 4	25°C		0.6	2		1.6	3.5	mV
			Full range			3			4.5	
α_{VIO}	Average temperature coefficient of input offset voltage	R_S = 50 Ω, See Note 4	MIN to 25°C		3	10		3	20	μV/°C
			25°C to MAX		3	10		3	20	
I_{IO}	Input offset current	See Note 4	25°C		0.75	3		1.8	5	μA
			MIN		1.8	7			7.5	
			MAX		0.25	3			7.5	
α_{IIO}	Average temperature coefficient of input offset current	See Note 4	MIN to 25°C		15	75		24	100	nA/°C
			25°C to MAX		5	25		15	50	
I_{IB}	Input bias current	See Note 4	25°C		7	15		7	20	μA
			MIN		12	25		9	30	
I_{SH}	High-level strobe current	$V_{(strobe)}$ = 5 V, V_{ID} = −5 mV	25°C			±100			±100	μA
I_{SL}	Low-level strobe current	$V_{(strobe)}$ = −100 mV, V_{ID} = 5 mV	25°C		−1	−2.5		−1	−2.5	mA
V_{ICR}	Common-mode input voltage range	V_{CC-} = −7 V	Full range	±5			±5			V
V_{ID}	Differential input voltage range		Full range	±5			±5			V
A_{VD}	Large-signal differential voltage amplification	No load, V_O = 0 to 2.5 V	25°C	12,500	33,000		10,000	33,000		
			Full range	10,000			8,000			
V_{OH}	High-level output voltage	V_{ID} = 5 mV, I_{OH} = 0	Full range		4§	5		4§	5	V
		V_{ID} = 5 mV, I_{OH} = −5 mA	Full range	2.5	3.6§		2.5	3.6§		
V_{OL}	Low-level output voltage	V_{ID} = −5 mV, I_{OL} = 0	Full range	−1	−0.5§	0‡	−1	−0.5§	0‡	V
		$V_{(strobe)}$ = 0.3 V, V_{ID} = 5 mV, I_{OL} = 0	Full range	−1		0‡	−1		0‡	V
I_{OL}	Low-level output current	V_{ID} = −5 mV, V_O = 0	25°C	2	2.4		1.6	2.4		mA
			MIN	1	2.3		0.5	2.4		
			MAX	0.5	2.3		0.5	2.4		
r_o	Output resistance	V_O = 1.4 V	25°C		200			200		Ω
CMRR	Common-mode rejection ratio	$R_S \leq 200\ \Omega$	Full range	80	100§		70	100§		dB
I_{CC+}	Supply current from V_{CC+}	V_{ID} = −5 mV, No load	Full range		5.5§	9		5.5§	9	mA
I_{CC-}	Supply current from V_{CC-}		Full range		−3.5§	−7		−3.5§	−7	mA
P_D	Total power dissipation		Full range		90§	150		90§	150	mW

†Unless otherwise noted, all characteristics are measured with the strobe open. Full range (MIN to MAX) for SN52510 is −55°C to 125°C and for the SN72510 is 0°C to 70°C.

‡The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic levels only, e.g., when 0 V is the maximum, the minimum limit is a more-negative voltage.

§These typical values are at T_A = 25°C.

NOTE 4: These characteristics are verified by measurements at the following temperatures and output voltage levels: for SN52510, V_O = 1.8 V at T_A = −55°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1 V at T_A = 125°C; for SN72510, V_O = 1.5 V at T_A = 0°C, V_O = 1.4 V at 25°C, and V_O = 1.2 V at T_A = 70°C. These output voltage levels were selected to approximate the logic threshold voltages of the types of digital logic circuits these comparators are intended to drive.

switching characteristics, V_{CC+} = 12 V, V_{CC-} = −6 V, T_A = 25°C

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
Response time	R_L = ∞,	C_L = 5 pF,	See Note 5		30	80	ns
Strobe release time	R_L = ∞,	C_L = 5 pF,	See Note 6		5	25	ns

NOTES: 5. The response time specified is for a 100-mV input step with 5-mV overdrive.

6. For testing purposes, the input bias conditions are selected to produce an output voltage of 1.4 V. A 5-mV overdrive is then added to the input bias voltage to produce an output voltage which rises above 1.4 V. The time interval is measured from the 50% point of the strobe voltage curve to the point where the overdriven output voltage crosses the 1.4 V level.

DEFINITION OF TERMS

Input Offset Voltage (V_{IO}) The d-c voltage which must be applied between the input terminals to force the quiescent d-c output voltage to the specified level. The input offset voltage may also be defined for the case where two equal resistances (R_S) are inserted in series with the input leads.

Average Temperature Coefficient of Input Offset Voltage (α_{VIO}) The ratio of the change in input offset voltage to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{VIO} = \left| \frac{(V_{IO} @ T_{A(1)}) - (V_{IO} @ T_{A(2)})}{T_{A(1)} - T_{A(2)}} \right|$$

where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

Input offset Current (I_{IO}) The difference between the currents into the two input terminals with the output at the specified level.

Average Temperature Coefficient of Input Offset Current (α_{IIO}) The ratio of the change in input offset current to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{IIO} = \left| \frac{(I_{IO} @ T_{A(1)}) - (I_{IO} @ T_{A(2)})}{T_{A(1)} - T_{A(2)}} \right|$$

where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

Input Bias Current (I_{IB}) The average of the currents into the two input terminals with the output at the specified level.

High-Level Strobe Current (I_{SH}) The current flowing into or out of the strobe at a high-level voltage.

Low-Level Strobe Current (I_{SL}) The current flowing out of the strobe at a low-level voltage.

Common-Mode Input Voltage Range (V_{ICR}) The range of common-mode voltage which if exceeded will cause the amplifier to cease functioning properly.

Differential Input Voltage Range (V_{ID}) The range of voltage between the two input terminals which if exceeded will cause the comparator to cease functioning properly.

Large-Signal Differential Voltage Amplification (A_{VD}) The ratio of the change in output voltage to the change in differential input voltage producing it.

High-Level Output Voltage (V_{OH}) The voltage at the output with the specified input conditions applied which should establish a high level at the output.

Low-Level Output Voltage (V_{OL}) The voltage at the output with the specified input conditions applied which should establish a low level at the output.

Low-Level Output Current (I_{OL}) The current flowing into the output at a specified low-level output voltage.

Output Resistance (r_o) The resistance between the output terminal and ground.

Common-Mode Rejection Ratio (CMRR) The ratio of differential voltage amplification to common-mode voltage amplification. This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.

Total Power Dissipation (P_D) The total d-c power supplied to the device less any power delivered from the device to a load. At no load: $P_D = V_{CC+} \cdot I_{CC+} + V_{CC-} \cdot I_{CC-}$.

Response Time The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial condition sufficient to saturate the output to an input level just barely in excess of that required to bring the output back to the logic threshold voltage. This excess is referred to as the voltage overdrive.

Strobe Release Time The time required for the output to rise to the logic threshold voltage after the strobe terminal has been driven from the low logic level to the high logic level. Appropriate input conditions are assumed.

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TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

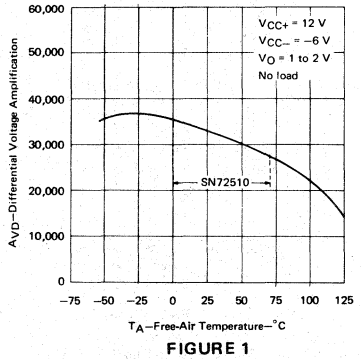


FIGURE 1

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

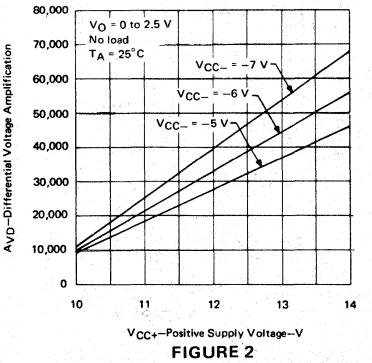


FIGURE 2

OUTPUT VOLTAGE LEVELS vs FREE-AIR TEMPERATURE

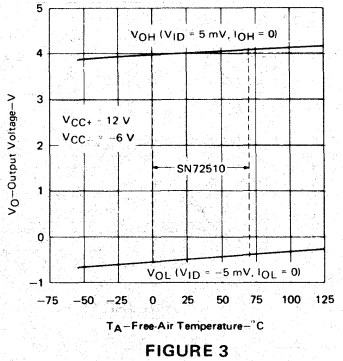


FIGURE 3

LOW-LEVEL OUTPUT CURRENT vs FREE-AIR TEMPERATURE

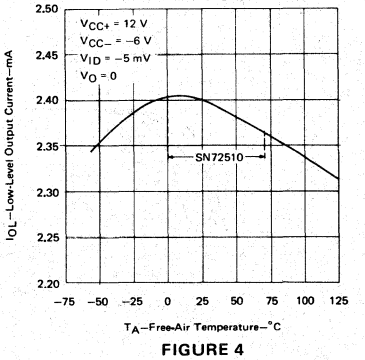


FIGURE 4

SN52510
VOLTAGE TRANSFER CHARACTERISTICS

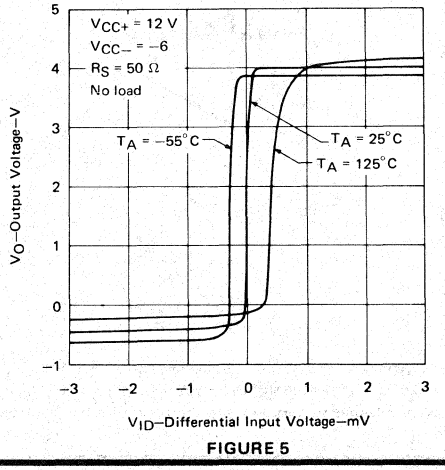


FIGURE 5

SN72510
VOLTAGE TRANSFER CHARACTERISTICS

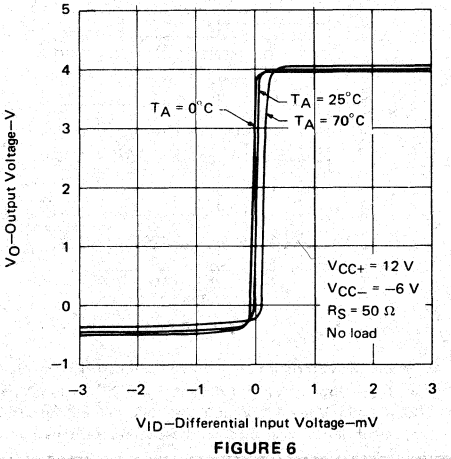


FIGURE 6

TYPICAL CHARACTERISTICS

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

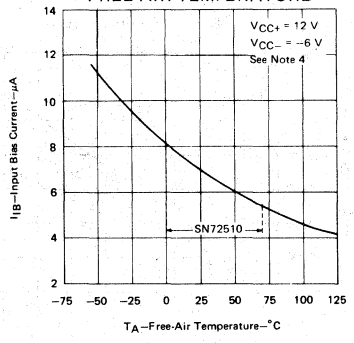


FIGURE 7

COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

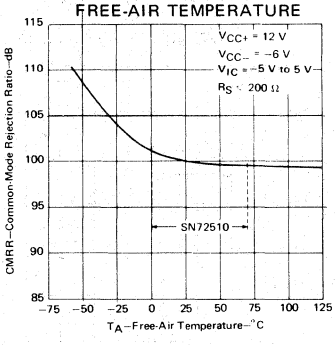


FIGURE 8

OUTPUT RESPONSE FOR
VARIOUS INPUT OVERDRIVES

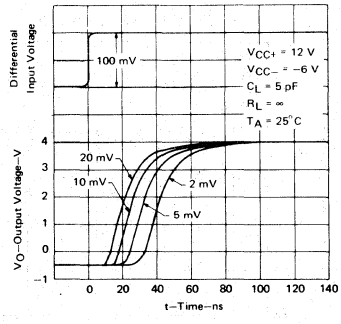


FIGURE 9

STROBE RELEASE TIME
FOR VARIOUS INPUT OVERDRIVES

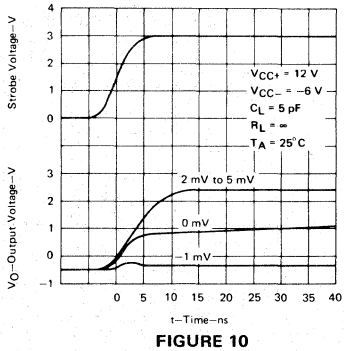


FIGURE 10

COMMON-MODE PULSE RESPONSE

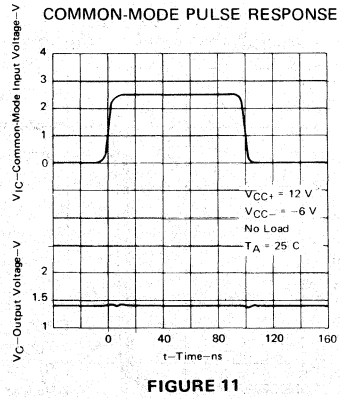
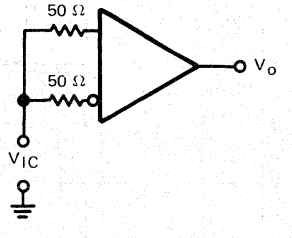


FIGURE 11



TEST CIRCUIT
FOR FIGURE 11

NOTE 4: These characteristics are verified by measurements at the following temperatures and output voltage levels: for SN52510, V_O = 1.8 V at T_A = −55°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1V at T_A = 125°C; for SN72510, V_O = 1.5 V at T_A = 0°C, V_O = 1.4 V at 25°C, and V_O = 1.2 V at T_A = 70°C. These output voltage levels were selected to approximate the logic threshold voltages of the types of digital logic circuits these comparators are intended to drive.

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TYPICAL CHARACTERISTICS

TOTAL POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

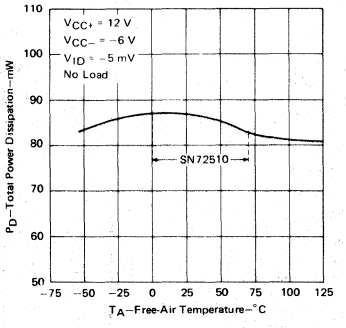

FIGURE 12

THERMAL INFORMATION

SN52510
DISSIPATION DERATING CURVE

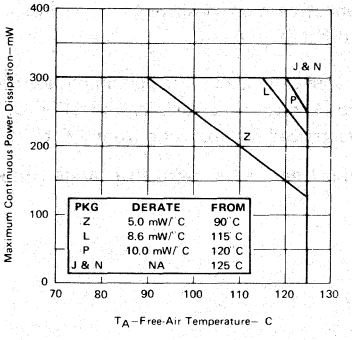

FIGURE 13

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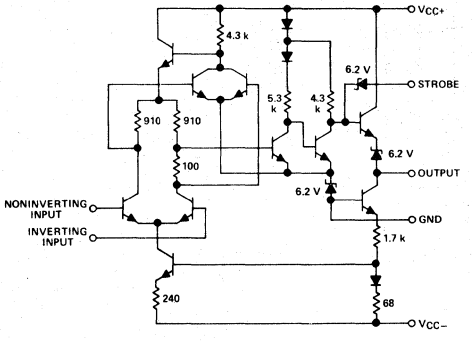
CIRCUIT TYPES SN52514, SN72514
DUAL DIFFERENTIAL COMPARATORS WITH STROBES

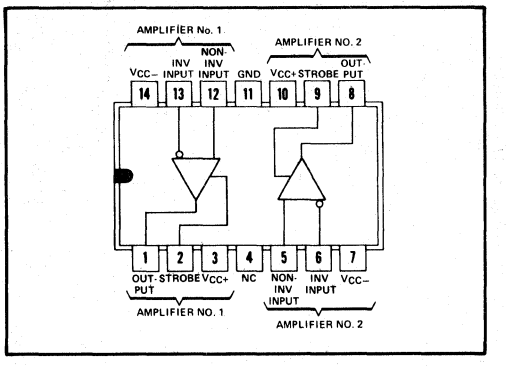
- Fast Response Times
- High Differential Voltage Amplification
- Low Offset Characteristics
- Outputs Compatible with Most TTL and DTL Circuits

schematic (each comparator)



Resistor values are in ohms.
Component values shown are nominal.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



NC—No internal connection

description

The SN52514 and SN72514 are improved versions of the SN72720 dual high-speed voltage comparator. When compared with the SN72720, these circuits feature higher amplification (typically 33,000) due to an extra amplification stage, increased accuracy because of lower offset characterisitcs, and greater flexibility with the addition of a strobe to each comparator. Since the output cannot be more positive than the strobe, a low-level input at the strobe will cause the output to go low regardless of the differential input.

These circuits are especially useful in applications requiring an amplitude discriminator, memory sense amplifier, or a high-speed limit detector. The SN52514 is characterized for operation over the full military temperature range of –55°C to 125°C; the SN72514 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1)	14 V
Supply voltage V_{CC-} (see Note 1)	–7 V
Differential input voltage (see Note 2)	±5 V
Input voltage (either input, see Note 1)	±7 V
Strobe voltage (see Note 1)	6 V
Peak output current ($t_w \leq 1$ s)	10 mA
Continuous total power dissipation: each comparator	300 mW
total package (see Note 3)	600 mW
Operating free-air temperature range: SN52514 Circuits	–55°C to 125°C
SN72714 Circuits	0°C to 70°C
Storage temperature range	–65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. For SN52514, this rating applies at (or below) 95°C free-air temperature. For operation above this temperature, derate linearly at the rate of 10.9 mW/°C. For SN72514, this rating applies at (or below) 70°C free-air temperature without derating.

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electrical characteristics at specified free-air temperature, V_{CC+} = 12 V, V_{CC-} = −6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN52514			SN72514			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S \leq 200\ \Omega$, See Note 4	25°C		0.6	2		1.6	3.5	mV
			Full range			3			4.5	
αV_{IO}	Average temperature coefficient of input offset voltage	R_S = 50 Ω, See Note 4	MIN to 25°C		3	10		3	20	μV/°C
			25°C to MAX		3	10		3	20	
I_{IO}	Input offset current	See Note 4	25°C		0.75	3		1.8	5	μA
			MIN		1.8	7			7.5	
			MAX		0.25	3			7.5	
αI_{IO}	Average temperature coefficient of input offset current	See Note 4	MIN to 25°C		15	75		24	100	nA/°C
			25°C to MAX		5	25		15	50	
I_{IB}	Input bias current	See Note 4	25°C		7	15		7	20	μA
			MIN		12	25		9	30	
I_{SH}	High-level strobe current	$V_{(strobe)}$ = 5 V, V_{ID} = −5 mV	25°C			±100			±100	μA
I_{SL}	Low-level strobe current	$V_{(strobe)}$ = −100 mV, V_{ID} = 5 mV	25°C		−1	−2.5		−1	−2.5	mA
V_{ICR}	Common-mode input voltage range	V_{CC-} = −7 V	Full range	±5			±5			V
V_{ID}	Differential input voltage range		Full range	±5			±5			V
A_{VD}	Large-signal differential voltage amplification	No load, V_O = 0 to 2.5 V	25°C	12,500	33,000		10,000	33,000		
			Full range	10,000			8,000			
V_{OH}	High-level output voltage	V_{ID} = 5 mV, I_{OH} = 0	Full range		4§	5		4§	5	V
		V_{ID} = 5 mV, I_{OH} = −5 mA	Full range	2.5	3.6§		2.5	3.6§		
V_{OL}	Low-level output voltage	V_{ID} = −5 mV, I_{OL} = 0	Full range	−1	−0.5§	0‡	−1	−0.5§	0‡	V
		$V_{(strobe)}$ = 0.3 V, V_{ID} = 5 mV, I_{OL} = 0	Full range	−1		0‡	−1		0‡	V
I_{OL}	Low-level output current	V_{ID} = −5 mV, V_O = 0	25°C	2	2.4		1.6	2.4		mA
			MIN	1	2.3		0.5	2.4		
			MAX	0.5	2.3		0.5	2.4		
r_o	Output resistance	V_O = 1.4 V	25°C		200			200		Ω
CMRR	Common-mode rejection ratio	$R_S \leq 200\ \Omega$	Full range	80	100§		70	100§		dB
I_{CC+}	Supply current from V_{CC+} ¶	V_{ID} = −5 mV, No load	Full range		5.5§	9		5.5§	9	mA
I_{CC-}	Supply current from V_{CC-} ¶		Full range		−3.5§	−7		−3.5§	−7	mA
P_D	Total power dissipation ¶		Full range		90§	150		90§	150	mW

†Unless otherwise noted, all characteristics are measured with the strobe open. Full range (MIN to MAX) for SN52514 is −55°C to 125°C and for the SN72514 is 0°C to 70°C.

‡The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic levels only, e.g., when 0 V is the maximum, the minimum limit is a more-negative voltage.

§These typical values are at T_A = 25°C.

¶Suppy current and power dissipation limits apply for each comparator.

NOTE 4: These characteristics are verified by measurements at the following temperatures and output voltage levels: for SN52514, V_O = 1.8 V at T_A = −55°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1V at T_A = 125°C; for SN72514, V_O = 1.5 V at T_A = 0°C, V_O = 1.4 V at 25°C, and V_O = 1.2 V at T_A = 70°C. These output voltage levels were selected to approximate the logic threshold voltages of the types of digital logic circuits these comparators are intended to drive.

switching characteristics, V_{CC+} = 12 V, V_{CC-} = −6 V, T_A = 25°C

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
Response time	R_L = ∞,	C_L = 5 pF,	See Note 5		30	80	ns
Strobe release time	R_L = ∞,	C_L = 5 pF,	See Note 6		5	25	ns

NOTES: 5. The response time specified is for a 100-mV input step with 5-mV overdrive.

6. For testing purposes, the input bias conditions are selected to produce an output voltage of 1.4 V. A 5-mV overdrive is then added to the input bias voltage to produce an output voltage which rises above 1.4 V. The time interval is measured from the 50% point of the strobe voltage curve to the point where the overdriven output voltage crosses the 1.4 V level.

For definition of terms and typical characteristic curves, see the SN52510/SN72510 data sheet on page 3-60.

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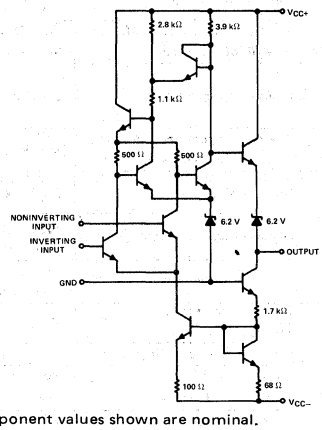
CIRCUIT TYPES SN52710, SN72710 DIFFERENTIAL COMPARATORS

- Fast Response Times
- Low Offset Characteristics
- Output Compatible with Most TTL and DTL Circuits

description

The SN52710 and SN72710 are monolithic high-speed comparators having differential inputs and a low-impedance output. Component matching, inherent in silicon integrated circuit fabrication techniques, produces a comparator with low-drift and low-offset characteristics. These circuits are especially useful for applications requiring an amplitude discriminator, memory sense amplifier, or a high-speed voltage comparator. The SN52710 is characterised for operation over the full military temperature range of −55°C to 125°C; the SN72710 is characterized for operation from 0°C to 70°C.

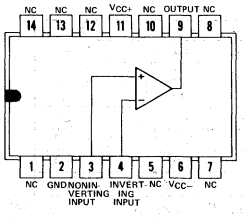
schematic



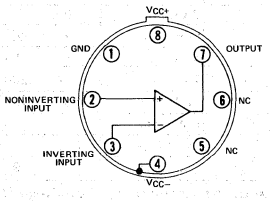
Component values shown are nominal.

terminal assignments

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)

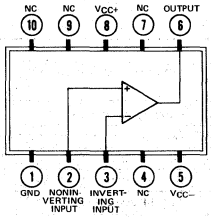


L
PLUG-IN PACKAGE (TOP VIEW)



PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE

S
FLAT PACKAGE (TOP VIEW)



PIN 5 IS IN ELECTRICAL CONTACT WITH THE CASE

NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN52710	SN72710	UNIT
Supply voltage V_{CC+} (see Note 1)		14	14	V
Supply voltage V_{CC-} (see Note 1)		−7	−7	V
Differential input voltage (see Note 2)		±5	±5	V
Input voltage (either input, see Note 1)		±7	±7	V
Peak output current ($t_w \leq 1$ s)		10	10	mA
Continuous total power dissipation at (or below) 70°C free-air temperature (see Note 3)		300	300	mW
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J, L, or S package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N package	260	260	°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. For operation of the SN52710 above 70°C free-air temperature, refer to Dissipation Derating Curve, Figure 8.

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electrical characteristics at specified free-air temperature, V_{CC+} = 12 V, V_{CC-} = −6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN52710			SN72710			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S \leq 200\ \Omega$, See Note 4	25°C		2	5		2	7.5	mV
			Full range			6			10	
α_{VIO}	Average temperature coefficient of input offset voltage	$R_S \leq 200\ \Omega$, See Note 4	Full range		5			7.5		μV/°C
I_{IO}	Input offset current	See Note 4	25°C		1	10		1	15	μA
			Full range			20			25	
I_{IB}	Input bias current	See Note 4	25°C		25	75		25	100	μA
			Full range			150			150	
V_I	Input voltage range	V_{CC-} = −7 V	25°C	±5			±5			V
V_{ID}	Differential input voltage range		25°C	±5			±5			V
A_{VD}	Large-signal differential voltage amplification	No load, See Note 4	25°C	750	1500		700	1500		
			Full range	500			500			
V_{OH}	High-level output voltage	V_{ID} = 15 mV, I_{OH} = −0.5 mA	25°C	2.5	3.2	4	2.5	3.2	4	V
V_{OL}	Low-level output voltage	V_{ID} = −15 mV, I_{OL} = 0	25°C	−1	−0.5	0‡	−1	−0.5	0‡	V
I_{OL}	Low-level output current	V_{ID} = −15 mV, V_O = 0	25°C	1.6	2.5					mA
r_o	Output resistance	V_O = 1.4 V	25°C		200			200		Ω
CMRR	Common-mode rejection ratio	$R_S \leq 200\ \Omega$	25°C	70	90		65	90		dB
I_{CC+}	Supply current from V_{CC+}	V_{ID} = −5 V to 5 V (−10 mV for typ), No load	25°C		5.4	10.1		5.4		mA
I_{CC-}	Supply current from V_{CC-}		25°C		−3.8	−8.9		−3.8		mA
P_D	Total power dissipation		25°C		88	175		88		mW

NOTE 4: These characteristics are verified by measurements at the following temperatures and output voltage levels: for SN52710, V_O = 1.8 V at T_A = −55°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1 V at T_A = 125°C; for SN72710, V_O = 1.5 V at T_A = 0°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1.2 V at T_A = 70°C. These output voltage levels were selected to approximate the logic threshold voltages of the types of digital logic circuits these comparators are intended to drive.

†Full range for SN52710 is −55°C to 125°C and for SN72710 is 0°C to 70°C.

‡The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic levels only, e.g., when 0 V is the maximum, the minimum limit is a more-negative voltage.

switching characteristics, V_{CC+} = 12 V, V_{CC-} = −6 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	SN52710	SN72710	UNIT
		TYP	TYP	
Response time	No load, See Note 5	40	40	ns

NOTE 5: The response time specified is for a 100-mV input step with 5-mV overdrive.

For definitions of terms, mechanical data and ordering instructions, see SN52711/SN72711 data sheet dated February 1971.

TYPICAL CHARACTERISTICS

OUTPUT RESPONSE FOR VARIOUS
INPUT OVERDRIVES

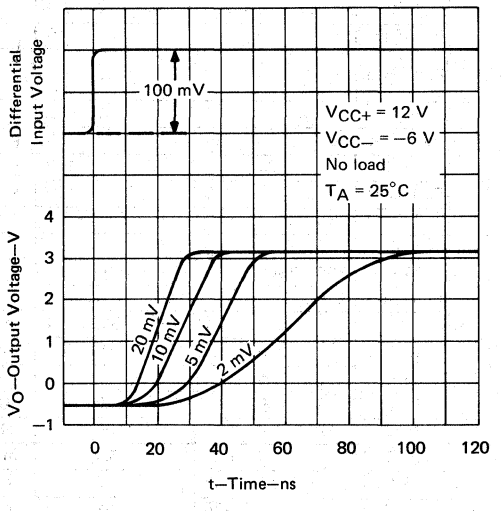

FIGURE 1

OUTPUT RESPONSE FOR VARIOUS
INPUT OVERDRIVES

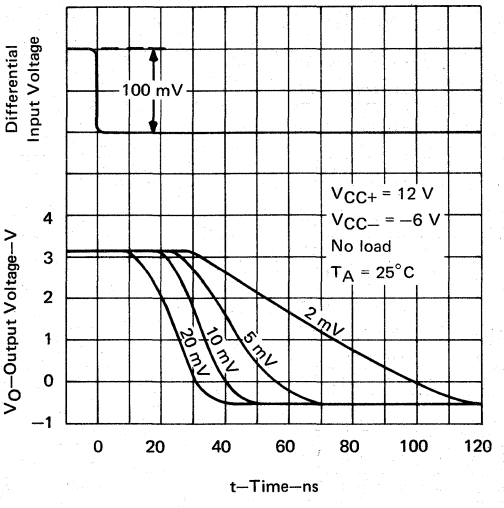

FIGURE 2

COMMON-MODE PULSE RESPONSE
vs
ELAPSED TIME

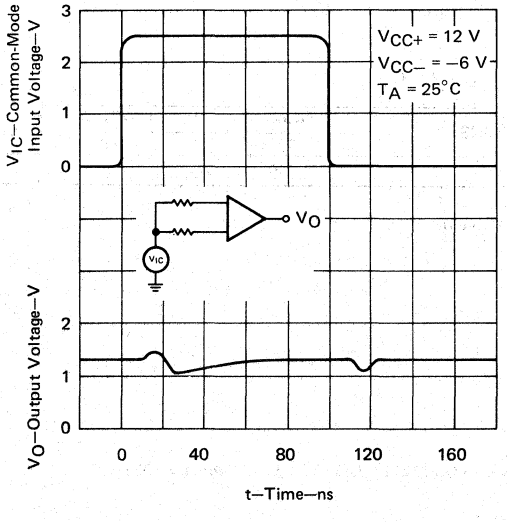

FIGURE 3

OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

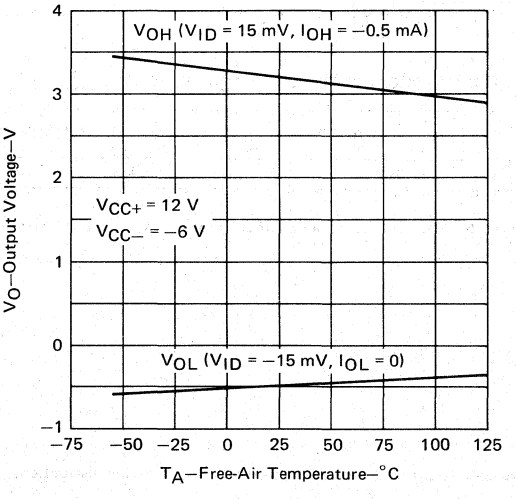

FIGURE 4

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TYPICAL CHARACTERISTICS

SN52710

VOLTAGE TRANSFER CHARACTERISTICS

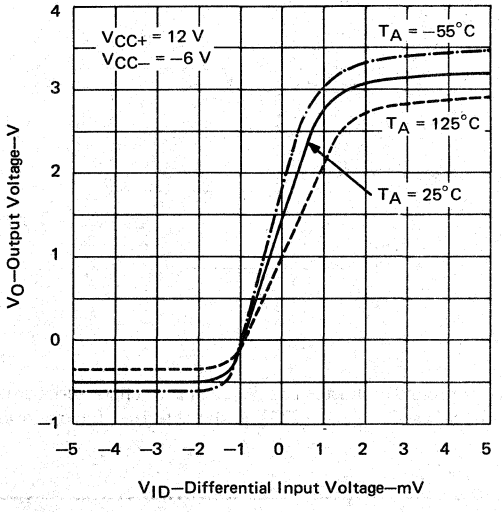

FIGURE 5

SN72710

VOLTAGE TRANSFER CHARACTERISTICS

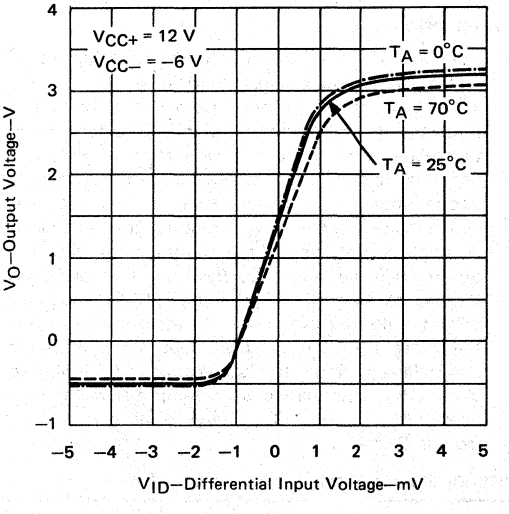

FIGURE 6

TOTAL POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

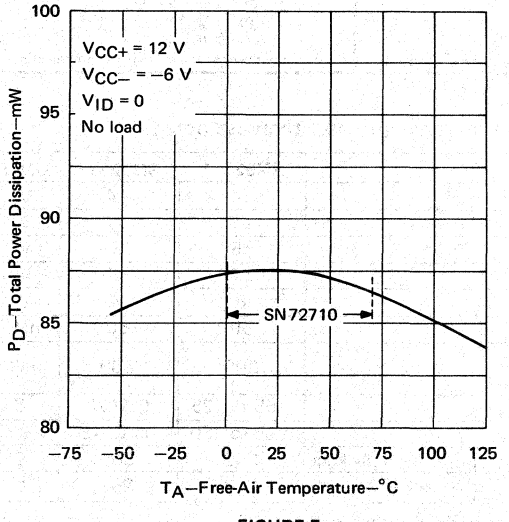

FIGURE 7

THERMAL INFORMATION

DISSIPATION DERATING CURVE

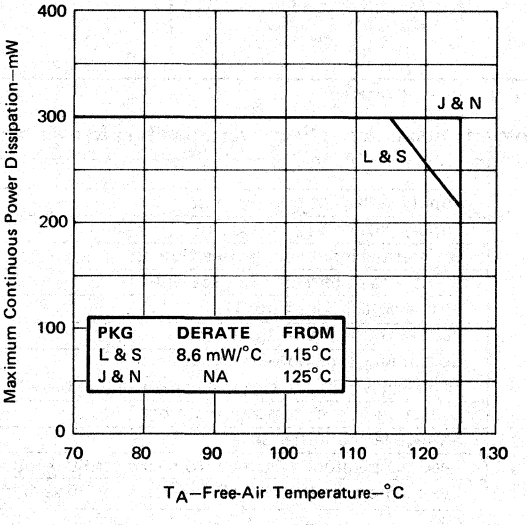

FIGURE 8

TEXAS INSTRUMENTS
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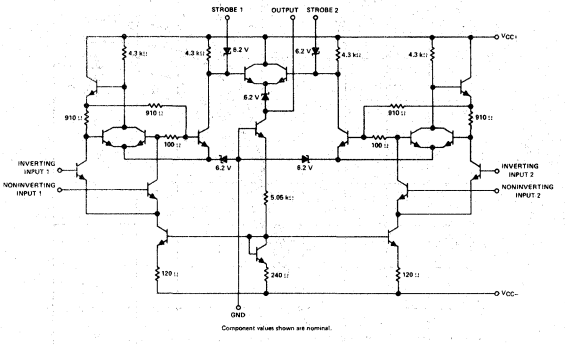
CIRCUIT TYPES SN52711, SN72711 DUAL-CHANNEL DIFFERENTIAL COMPARATORS WITH STROBES

- Fast Response Times
- Low Offset Characteristics
- Output Compatible with Most TTL and DTL Circuits
- Designed to be Interchangeable with Fairchild μA711 and μA711C

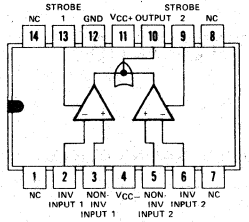
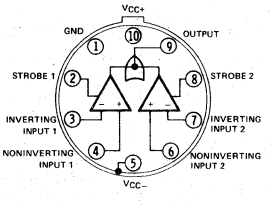
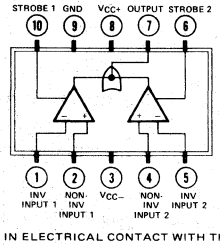
description

The SN52711 and SN72711 circuits are high-speed dual-channel comparators with differential inputs and a low-impedance output. Component matching, inherent with silicon monolithic circuit fabrication techniques, produces a comparator circuit with low-drift and low-offset characteristics. An independent strobe input is provided for each of the two channels, which when taken low, inhibits the associated channel. If both strobes are simultaneously low, the output will be low regardless of the conditions applied to the differential inputs. The comparator output pulse width may be "stretched" by varying the capacitive loading. These dual comparators are particularly useful for applications requiring an amplitude-discriminating sense amplifier with an adjustable threshold voltage. The SN52711 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN72711 is characterized for operation from 0°C to 70°C.

schematic



terminal assignments

J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)	L PLUG-IN PACKAGE (TOP VIEW)	S FLAT PACKAGE (TOP VIEW)
		
	PIN 5 IS IN ELECTRICAL CONTACT WITH THE CASE	PIN 3 IS IN ELECTRICAL CONTACT WITH THE CASE

NC—No Internal Connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN52711	SN72711	UNIT
Supply voltage V_{CC+} (see Note 1)		14	14	V
Supply voltage V_{CC-} (see Note 1)		−7	−7	V
Differential input voltage (see Note 2)		±5	±5	V
Input voltage (either input, see Note 1)		±7	±7	V
Strobe voltage (see Note 1)		6	6	V
Peak output current ($t_w \leq 1$ s)		50	50	mA
Continuous total power dissipation at (or below) 70°C free-air temperature (see Note 3)		300	300	mW
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J, L, or S package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N package	260	260	°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. For operation of SN52711 above 70°C free-air temperature, refer to Dissipation Derating Curve, Figure 9.

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electrical characteristics at specified free-air temperature, V_{CC+} = 12 V, V_{CC-} = −6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN52711			SN72711			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S \leq 200\ \Omega$, V_{IC} = 0, See Note 4		25°C		1	3.5		1	5	mV
				Full range			4.5			6	
		$R_S \leq 200\ \Omega$, See Note 4		25°C		1	5		1	7.5	
				Full range			6			10	
α_{VIO}	Average temperature coefficient of input offset voltage	$R_S \leq 200\ \Omega$, V_{IC} = 0, See Note 4		Full range		5			5		μV/°C
I_{IO}	Input offset current	See Note 4		25°C		0.5	10		0.5	15	μA
				Full range			20			25	
I_{IB}	Input bias current	See Note 4		25°C		25	75		25	100	μA
				Full range			150			150	
I_{SL}	Low-level strobe current	$V_{(strobe)}$ = 0,	V_{ID} = 10 mV	25°C		−1.2	−2.5		−1.2	−2.5	mA
V_I	Input voltage range	V_{CC-} = −7 V		25°C	±5			±5			V
V_{ID}	Differential input voltage range			25°C	±5			±5			V
A_{VD}	Large-signal differential voltage amplification	No load, V_O = 0 to 2.5 V		25°C	750	1500		700	1500		
				Full range	500			500			
V_{OH}	High-level output voltage	V_{ID} = 10 mV,	I_{OH} = 0	25°C		4.5	5		4.5	5	V
		V_{ID} = 10 mV,	I_{OH} = −5 mA	25°C	2.5	3.5		2.5	3.5		
V_{OL}	Low-level output voltage	V_{ID} = −10 mV,	I_{OL} = 0	25°C	−1	−0.5	0‡	−1	−0.5	0‡	V
		V_{ID} = 10 mV, I_{OL} = 0	$V_{(strobe)}$ = 0.3 V,	25°C	−1		0‡	−1		0‡	
I_{OL}	Low-level output current	V_{ID} = −10 mV,	V_O = 0	25°C	0.5	0.8		0.5	0.8		mA
r_o	Output resistance	V_O = 1.4 V		25°C		200			200		Ω
CMRR	Common-mode rejection ratio	$R_S \leq 200\ \Omega$		25°C	70	90		65	90		dB
I_{CC+}	Supply current from V_{CC+}	V_{ID} = −5 V to 5 V (−10 mV for typ), Strobes alternately grounded,		25°C		9			9		mA
I_{CC-}	Supply current from V_{CC-}			25°C		−4			−4		mA
P_D	Total power dissipation	No load		25°C		130	200		130	230	mW

NOTE 4: These characteristics are verified by measurements at the following temperatures and output voltage levels: for SN52711, V_O = 1.8 V at T_A = −55°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1 V at T_A = 125°C; for SN72711, V_O = 1.5 V at T_A = 0°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1.2 V at 70°C. These output voltage levels were selected to approximate the logic threshold voltages of the types of digital logic circuits these comparators are intended to drive.

†Unless otherwise noted, all characteristics are measured with the strobe of the channel under test open. The strobe of the other channel is grounded. Full range for SN52711 is −55°C to 125°C and for the SN72711 is 0°C to 70°C.

‡The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic levels only, e.g., when 0 V is the maximum, the minimum limit is a more-negative voltage.

switching characteristics, V_{CC+} = 12 V, V_{CC-} = −6 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		SN52711			SN72711			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Response time	No load,	See Note 5		40	80		40		ns
Strobe release time	No load,	See Note 6		7	25		7		ns

NOTES: 5. The response time specified is for a 100-mV input step with 5-mV overdrive.

6. For testing purposes, the input bias conditions are selected to produce an output voltage of 1.4 V. A 5-mV overdrive is then added to the input bias voltage to produce an output voltage which rises above 1.4 V. The time interval is measured from the 50% point of the strobe voltage curve to the point where the overdriven output voltage crosses the 1.4 V level.

DEFINITION OF TERMS

Input Offset Voltage (V_{IO}) The d-c voltage which must be applied between the input terminals to force the quiescent d-c output voltage to the specified level. The input offset voltage may also be defined for the case where two equal resistances (R_S) are inserted in series with the input leads.

Average Temperature Coefficient of Input Offset Voltage (α_{VIO}) The ratio of the change in input offset voltage to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{VIO} = \left| \frac{(V_{IO} @ T_{A(1)}) - (V_{IO} @ T_{A(2)})}{T_{A(1)} - T_{A(2)}} \right|$$ where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

Input offset Current (I_{IO}) The difference between the currents into the two input terminals with the output at the specified level.

Input Bias Current (I_{IB}) The average of the currents into the two input terminals with the output at the specified level.

3

Low-Level Strobe Current (I_{SL}) The current flowing out of the strobe at a low-level voltage.

Input Voltage Range (V_I) The range of voltage which if exceeded at either input terminal will cause the comparator to cease functioning properly.

Differential Input Voltage Range (V_{ID}) The range of voltage between the two input terminals which if exceeded will cause the comparator to cease functioning properly.

Large-Signal Differential Voltage Amplification (A_{VD}) The ratio of the change in output voltage to the change in differential input voltage producing it.

High-Level Output Voltage (V_{OH}) The voltage at the output with the specified input conditions applied which should establish a high level at the output.

Low-Level Output Voltage (V_{OL}) The voltage at the output with the specified input conditions applied which should establish a low level at the output.

Low-Level Output Current (I_{OL}) The current flowing into the output at a specified low-level output voltage.

Output Resistance (r_o) The resistance between the output terminal and ground.

Common-Mode Rejection Ratio (CMRR) The ratio of differential voltage amplification to common-mode voltage amplification. This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.

Total Power Dissipation (P_D) The total d-c power supplied to the device less any power delivered from the device to a load. At no load: $P_D = V_{CC+} \cdot I_{CC+} + V_{CC-} \cdot I_{CC-}$.

Response Time The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial condition sufficient to saturate the output to an input level just barely in excess of that required to bring the output back to the logic threshold voltage. This excess is referred to as the voltage overdrive.

Strobe Release Time The time required for the output to rise to the logic threshold voltage after the strobe terminal has been driven from the low logic level to the high logic level. Appropriate input conditions are assumed.

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TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

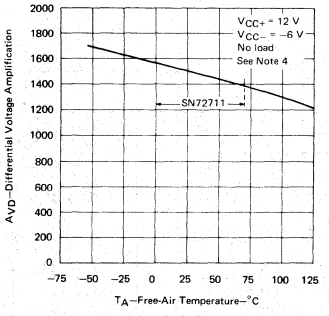

FIGURE 1

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

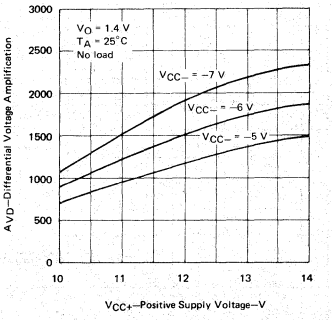

FIGURE 2

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

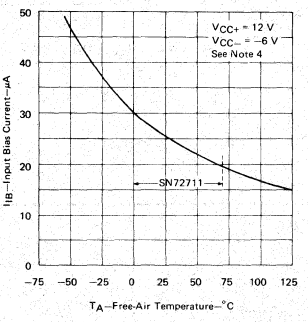

FIGURE 3

TOTAL POWER DISSIPATION vs FREE-AIR TEMPERATURE

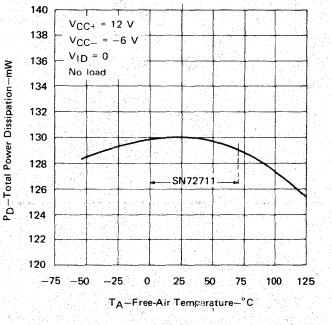

FIGURE 4

SN52711 VOLTAGE TRANSFER CHARACTERISTICS

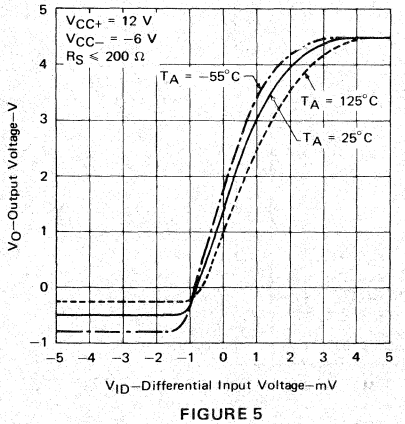

FIGURE 5

SN72711 VOLTAGE TRANSFER CHARACTERISTICS

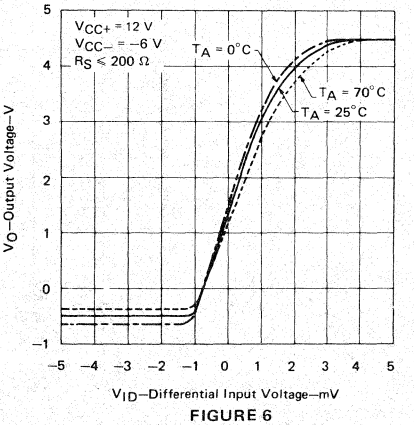

FIGURE 6

NOTE 4: These characteristics are verified by measurements at the following temperatures and output voltage levels: for SN52711, V_O = 1.8 V at T_A = −55°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1 V at T_A = 125°C; for SN72711, V_O = 1.5 V at T_A = 0°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1.2 V at 70°C. These output voltage levels were selected to approximate the logic threshold voltages of the types of digital logic circuits these comparators are intended to drive.

TYPICAL CHARACTERISTICS

OUTPUT RESPONSE FOR
VARIOUS INPUT OVERDRIVES

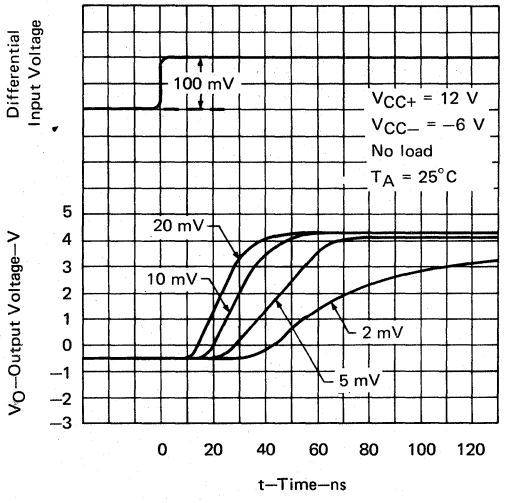

FIGURE 7

STROBE RELEASE TIME
FOR VARIOUS INPUT OVERDRIVES

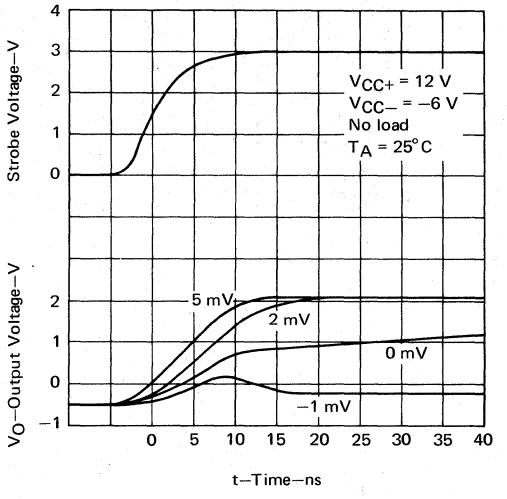

FIGURE 8

THERMAL INFORMATION

SN52711
DISSIPATION DERATING CURVE

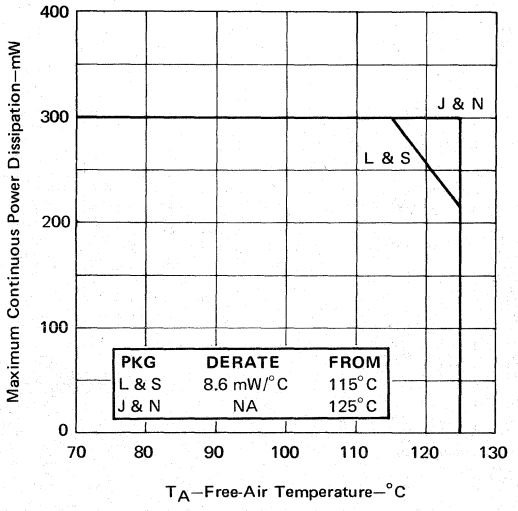

FIGURE 9

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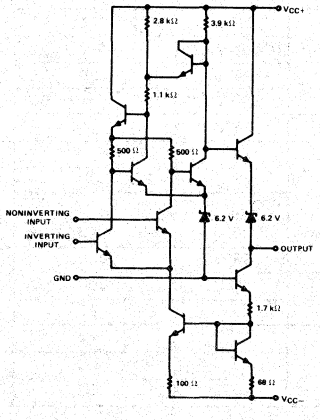
CIRCUIT TYPE SN72720
DUAL DIFFERENTIAL COMPARATORS

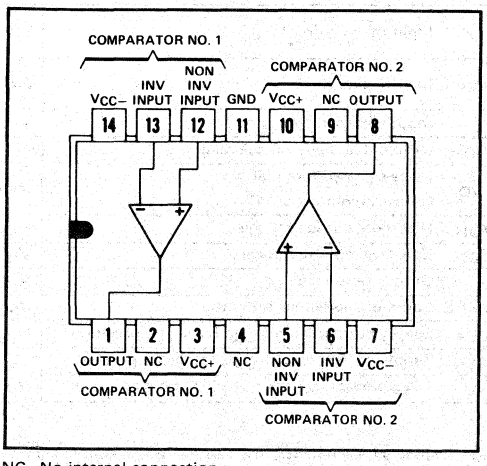
- Fast Response Times
- Low Offset Characteristics
- Output Compatible with Most TTL and DTL Circuits

schematic (each comparator)



Component values shown are nominal.

N
DUAL-IN-LINE PACKAGE (TOP VIEW)



NC—No internal connection

description

The SN72720 is two high-speed comparators in a single package, each electrically identical to the SN72710 and having differential inputs and a low-impedance output. Component matching, inherent in silicon monolithic circuit fabrication techniques, produces a comparator with low-drift and low-offset characteristics. This circuit is especially useful for applications requiring an amplitude discriminator, memory sense amplifier, or a high-speed voltage comparator. The SN72720 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1)	14 V
Supply voltage V_{CC-} (see Note 1)	−7 V
Differential input voltage (see Note 2)	±5 V
Input voltage (either input, see Note 1)	±7 V
Peak output current, each comparator ($t_W \leq 1$ s)	10 mA
Continuous total power dissipation: each comparator	300 mW
total package	600 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 10 seconds	260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.

CIRCUIT TYPE SN72720
DUAL DIFFERENTIAL COMPARATORS

electrical characteristics at specified free-air temperature, V_{CC+} = 12 V, V_{CC-} = −6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$R_S \leq 200\ \Omega$, See Note 3	25°C		2	7.5	mV
			0°C to 70°C			10	
α_{VIO}	Average temperature coefficient of input offset voltage	$R_S \leq 200\ \Omega$, See Note 3	0°C to 70°C		7.5		μV/°C
I_{IO}	Input offset current	See Note 3	25°C		1	15	μA
			0°C to 70°C			25	
I_{IB}	Input bias current	See Note 3	25°C		25	100	μA
			0°C to 70°C			150	
V_I	Input voltage range	V_{CC-} = −7 V	25°C	±5			V
V_{ID}	Differential input voltage range		25°C	±5			V
A_{VD}	Large-signal differential voltage amplification	No load, See Note 3	25°C	700	1500		
			0°C to 70°C	500			
V_{OH}	High-level output voltage	V_{ID} = 15 mV, I_{OH} = −0.5 mA	25°C	2.5	3.2	4	V
V_{OL}	Low-level output voltage	V_{ID} = −15 mV, I_{OL} = 0	25°C	−1	−0.5	0‡	V
r_o	Output resistance	V_O = 1.4 V	25°C		200		Ω
CMRR	Common-mode rejection ratio	$R_S \leq 200\ \Omega$	25°C	65	90		dB
I_{CC+}	Supply current from V_{CC+} (each comparator)	V_{ID} = −5 V to 5 V (−10 mV for typ), No load	25°C		5.4		mA
I_{CC-}	Supply current from V_{CC-} (each comparator)		25°C		−3.8		mA
P_D	Total power dissipation (each comparator)		25°C		88		mW

NOTE 3: These characteristics are verified by measurements at the following temperatures and output voltage levels: V_O = 1.5 V at T_A = 0°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1.2 V at T_A = 70°C. These output voltage levels were selected to approximate the logic threshold voltages of the types of digital logic circuits these comparators are intended to drive.

‡The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic levels only, e.g., when 0 V is the maximum, the minimum limit is a more-negative voltage.

switching characteristics, V_{CC+} = 12 V, V_{CC-} = −6 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
Response time	No load, See Note 4	40	ns

NOTE 4: The response time specified is for a 100-mV input step with 5-mV overdrive.

For definition of terms, refer to page of the SN52711/SN72711 data sheet. Typical characteristic curves on the SN72710 data sheet, pages 3-70 and 3-71, are applicable for the SN72720.

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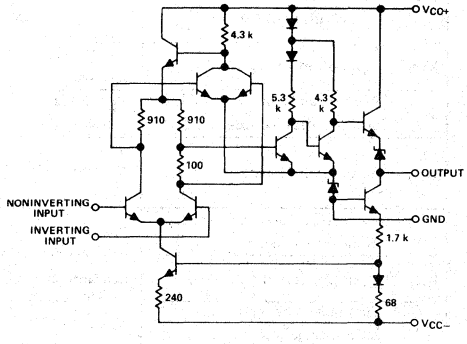
CIRCUIT TYPES SN52810, SN7281
DIFFERENTIAL COMPARATOR

- Low Offset Characteristics
- High Differential Voltage Amplification
- Fast Response Times
- Output Compatible with Most TTL and DTL Circuits

schematic



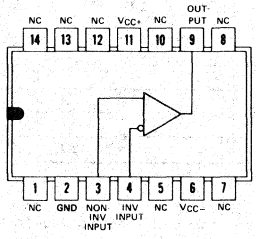
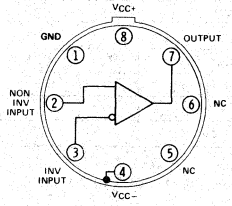
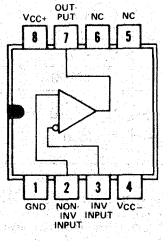
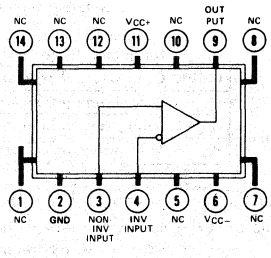
Resistor values are nominal in ohms.

description

The SN52810 and SN72810 are improved versions of the SN52710 and SN72710 high-speed voltage comparators with an extra stage added to increase voltage amplification and accuracy. Typical amplification is 33,000. Component matching, inherent in monolithic integrated circuit fabrication techniques, produces a comparator with low-drift and low-offset characteristics. These circuits are particularly useful for applications requiring an amplitude discriminator, memory sense amplifier, or a high-speed limit detector.

The SN52810 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN72810 is characterized for operation from 0°C to 70°C.

terminal assignments

J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)	L PLUG-IN PACKAGE (TOP VIEW)	P DUAL-IN-LINE PACKAGE (TOP VIEW)	Z FLAT PACKAGE (TOP VIEW)
	 PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE		

NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1)	14 V
Supply voltage V_{CC-} (see Note 1)	−7 V
Differential input voltage (see Note 2)	±5 V
Input voltage (either input, see Note 1)	±7 V
Peak output current ($t_w \leq 1$ s)	10 mA
Continuous total power dissipation at (or below) 70°C free-air temperature (see Note 3)	300 mW
Operating free-air temperature range: SN52810 Circuits	−55°C to 125°C
SN72810 Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J, L, or Z package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N or P package	260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. For operation of the SN52810 above 70°C free-air temperature, refer to Dissipating Derating Curve, Figure 1.

electrical characteristics at specified free-air temperature, V_{CC+} = 12 V, V_{CC-} = −6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN52810			SN72810			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S \leq 200\ \Omega$, See Note 4	25°C		0.6	2		1.6	3.5	mV
			Full range			3			4.5	
α_{VIO}	Average temperature coefficient of input offset voltage	$R_S = 50\ \Omega$, See Note 4	MIN to 25°C		3	10		3	20	μV/°C
			25°C to MAX		3	10		3	20	
I_{IO}	Input offset current	See Note 4	25°C		0.75	3		1.8	5	μA
			MIN		1.8	7			7.5	
			MAX		0.25	3			7.5	
α_{IIO}	Average temperature coefficient of input offset current	See Note 4	MIN to 25°C		15	75		24	100	nA/°C
			25°C to MAX		5	25		15	50	
I_{IB}	Input bias current	See Note 4	25°C		7	15		7	20	μA
			MIN		12	25		9	30	
V_{ICR}	Common-mode input voltage range	$V_{CC-} = -7$ V	Full range	±5			±5			V
V_{ID}	Differential input voltage range		Full range	±5			±5			V
A_{VD}	Large-signal differential voltage amplification	No load, V_O = 0 to 2.5 V	25°C	12,500	33,000		10,000	33,000		
			Full range	10,000			8,000			
V_{OH}	High-level output voltage	V_{ID} = 5 mV, I_{OH} = 0	Full range		4§	5		4§	5	V
		V_{ID} = 5 mV, I_{OH} = −5 mA	Full range	2.5	3.6§		2.5	3.6§		
V_{OL}	Low-level output voltage	V_{ID} = −5 mV, I_{OL} = 0	Full range	−1	−0.5§	0‡	−1	−0.5§	0‡	V
I_{OL}	Low-level output current	V_{ID} = −5 mV, V_O = 0	25°C	2	2.4		1.6	2.4		mA
			MIN	1	2.3		0.5	2.4		
			MAX	0.5	2.3		0.5	2.4		
r_o	Output resistance	V_O = 1.4 V	25°C		200			200		Ω
CMRR	Common-mode rejection ratio	$R_S \leq 200\ \Omega$	Full range	80	100§		70	100§		dB
I_{CC+}	Supply current from V_{CC+}	V_{ID} = −5 mV, No load	Full range		5.5§	9		5.5§	9	mA
I_{CC-}	Supply current from V_{CC-}		Full range		−3.5§	−7		−3.5§	−7	mA
P_D	Total power dissipation		Full range		90§	150		90§	150	mW

† Full range (MIN to MAX) for SN52810 is −55°C to 125°C and for the SN72810 is 0°C to 70°C.

‡ The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic levels only, e.g., when 0 V is the maximum, the minimum limit is a more-negative voltage.

§ These typical values are at T_A = 25°C.

NOTE 4: These characteristics are verified by measurements at the following temperatures and output voltage levels: for SN52810, V_O = 1.8 V at T_A = −55°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1V at T_A = 125°C; for SN72810, V_O = 1.5 V at T_A = 0°C, V_O = 1.4 V at 25°C, and V_O = 1.2 V at T_A = 70°C. These output voltage levels were selected to approximate the logic threshold voltages of the types of digital logic circuits these comparators are intended to drive.

switching characteristics, V_{CC+} = 12 V, V_{CC-} = −6 V, T_A = 25°C

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
Response time	$R_L = \infty$,	C_L = 5 pF,	See Note 5		30	80	ns

NOTE 5: The response time specified is for a 100-mV input step with 5-mV overdrive.

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DEFINITION OF TERMS

Input Offset Voltage (V_{IO}) The d-c voltage which must be applied between the input terminals to force the quiescent d-c output voltage to the specified level. The input offset voltage may also be defined for the case where two equal resistances (R_S) are inserted in series with the input leads.

Average Temperature Coefficient of Input Offset Voltage (α_{VIO}) The ratio of the change in input offset voltage to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{VIO} = \left| \frac{(V_{IO} @ T_{A(1)}) - (V_{IO} @ T_{A(2)})}{T_{A(1)} - T_{A(2)}} \right|$$ where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

Input offset Current (I_{IO}) The difference between the currents into the two input terminals with the output at the specified level.

Average Temperature Coefficient of Input Offset Current (α_{IIO}) The ratio of the change in input offset current to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{IIO} = \left| \frac{(I_{IO} @ T_{A(1)}) - (I_{IO} @ T_{A(2)})}{T_{A(1)} - T_{A(2)}} \right|$$ where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

Input Bias Current (I_{IB}) The average of the currents into the two input terminals with the output at the specified level.

Input Voltage Range (V_I) The range of voltage which if exceeded at either input terminal will cause the comparator to cease functioning properly.

Differential Input Voltage Range (V_{ID}) The range of voltage between the two input terminals which if exceeded will cause the comparator to cease functioning properly.

Large-Signal Differential Voltage Amplification (A_{VD}) The ratio of the change in output voltage to the change in differential input voltage producing it.

High-Level Output Voltage (V_{OH}) The voltage at the output with the specified input conditions applied which should establish a high level at the output.

Low-Level Output Voltage (V_{OL}) The voltage at the output with the specified input conditions applied which should establish a low level at the output.

Low-Level Output Current (I_{OL}) The current flowing into the output at a specified low-level output voltage.

Output Resistance (r_o) The resistance between the output terminal and ground.

Common-Mode Rejection Ratio (CMRR) The ratio of differential voltage amplification to common-mode voltage amplification. This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.

Total Power Dissipation (P_D) The total d-c power supplied to the device less any power delivered from the device to a load. At no load: $P_D = V_{CC+} \cdot I_{CC+} + V_{CC-} \cdot I_{CC-}$.

Response Time The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial condition sufficient to saturate the output to an input level just barely in excess of that required to bring the output back to the logic threshold voltage. This excess is referred to as the voltage overdrive.

THERMAL INFORMATION

SN52810
DISSIPATION DERATING CURVE

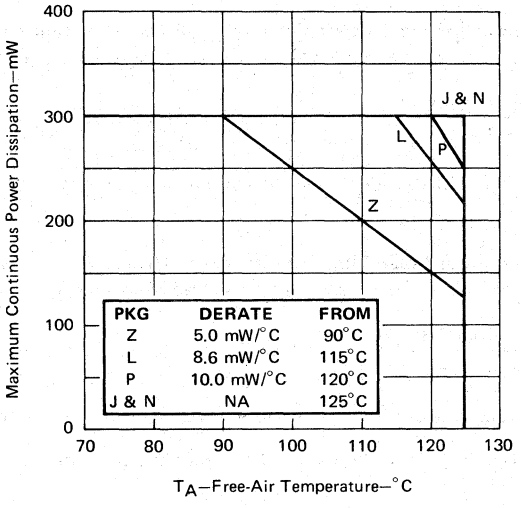

FIGURE 1

TYPICAL CHARACTERISTICS

TOTAL POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

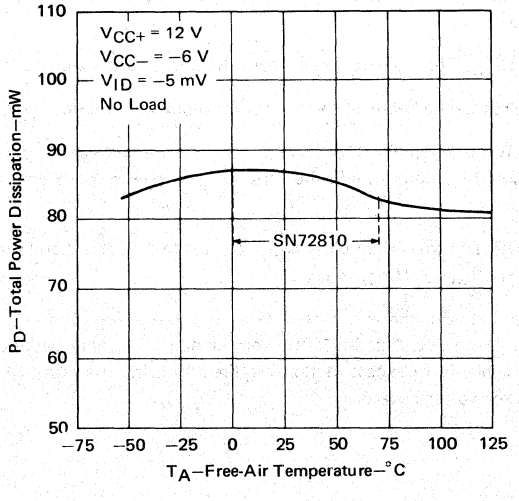

FIGURE 2

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TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

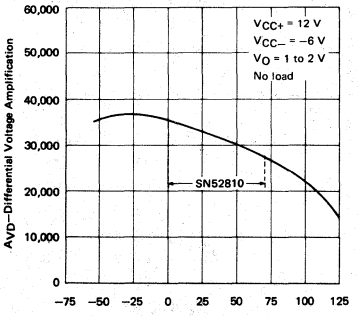


FIGURE 3

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

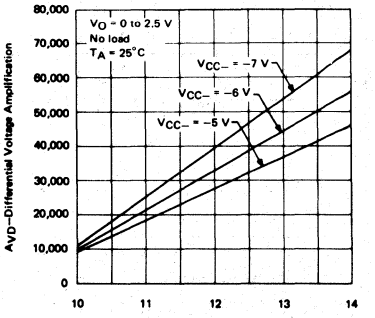


FIGURE 4

OUTPUT VOLTAGE LEVELS vs FREE-AIR TEMPERATURE

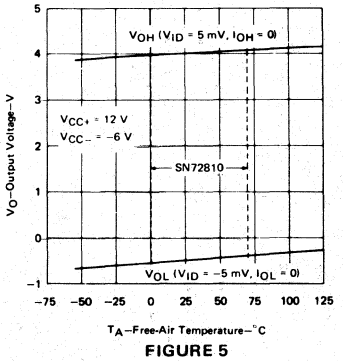


FIGURE 5

LOW-LEVEL OUTPUT CURRENT vs FREE-AIR TEMPERATURE

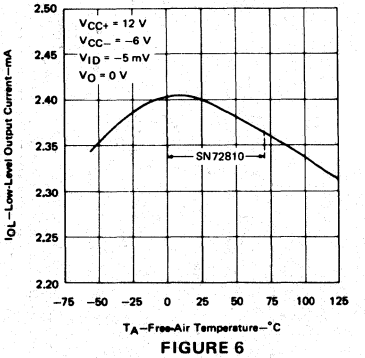


FIGURE 6

SN52810 VOLTAGE TRANSFER CHARACTERISTICS

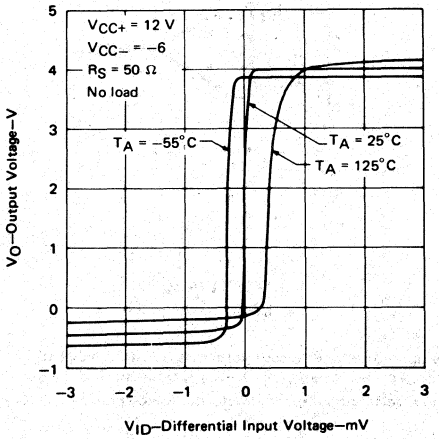


FIGURE 7

SN72810 VOLTAGE TRANSFER CHARACTERISTICS

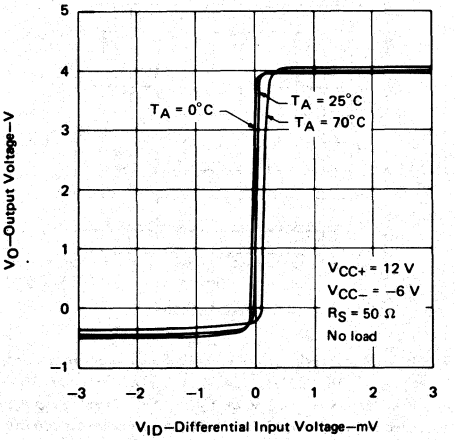


FIGURE 8

TYPICAL CHARACTERISTICS

INPUT BIAS CURRENT
VS
FREE-AIR TEMPERATURE

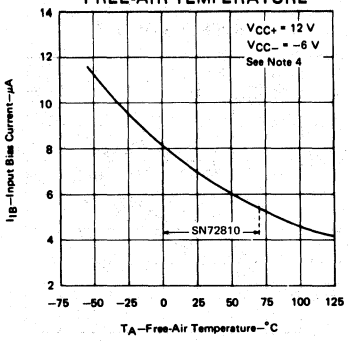


FIGURE 9

COMMON-MODE REJECTION RATIO
VS
FREE-AIR TEMPERATURE

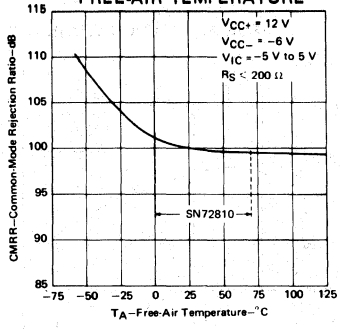


FIGURE 10

3

OUTPUT RESPONSE FOR
VARIOUS INPUT OVERDRIVES

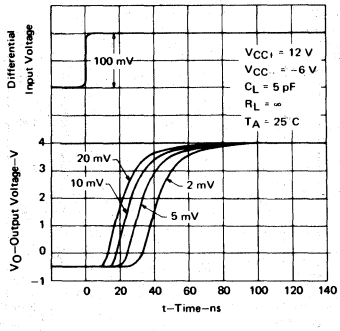


FIGURE 11

COMMON-MODE PULSE RESPONSE

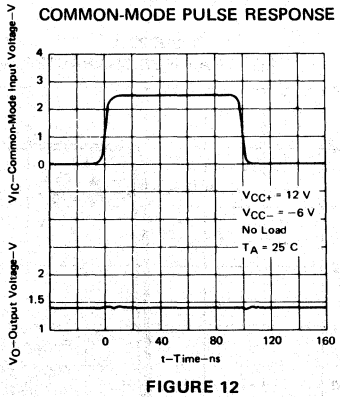
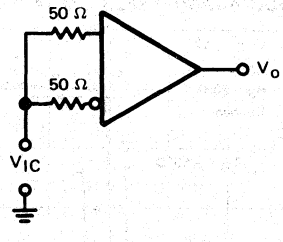


FIGURE 12



TEST CIRCUIT
FOR FIGURE 12

NOTE 4: These characteristics are verified by measurements at the following temperatures and output voltage levels: for SN52810, V_O = 1.8 V at T_A = −55°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1V at T_A = 125°C; for SN72810, V_O = 1.5 V at T_A = 0°C, V_O = 1.4 V at 25°C, and V_O = 1.2 V at T_A = 70°C. These output voltage levels were selected to approximate the logic threshold voltages of the types of digital logic circuits these comparators are intended to drive.

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CIRCUIT TYPES SN52811, SN72811
DUAL-CHANNEL DIFFERENTIAL COMPARATORS WITH STROBES

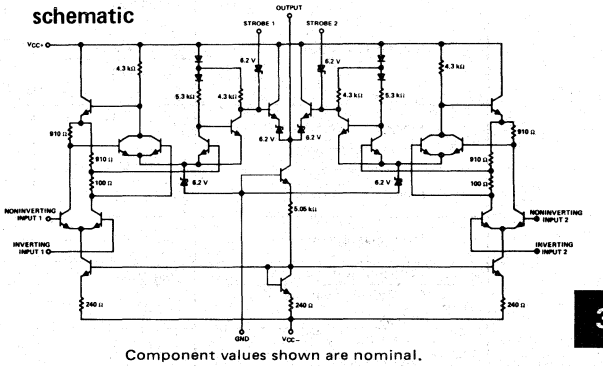
- Fast Response Times
- Improved Voltage Amplification and Offset Characteristics
- Output Compatible with Most TTL and DTL Circuits

description

The SN52811 and SN72811 are improved versions of the SN52711 and SN72711 high-speed dual-channel voltage comparators. Voltage amplification is higher (typically 17,500) due to an extra stage, increasing the comparator accuracy. The output pulse width may be "stretched" by varying the capacitive loading.

Each channel has differential inputs, a strobe input, and an output in common with the other channel. When either strobe is taken low, it inhibits the associated channel. If both strobes are simultaneously low, the output will be low regardless of the conditions applied to the differential inputs.

schematic



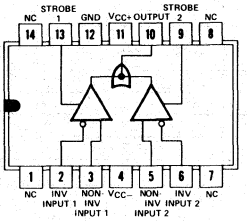
Component values shown are nominal.

These dual-channel voltage comparators are particularly attractive for applications requiring an amplitude-discriminating sense amplifier with an adjustable threshold voltage.

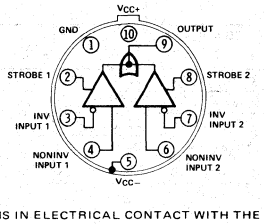
The SN52811 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN72811 is characterized for operation from 0°C to 70°C.

terminal assignments

J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)

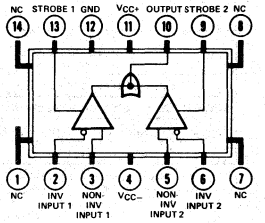


L PLUG-IN PACKAGE (TOP VIEW)



PIN 5 IS IN ELECTRICAL CONTACT WITH THE CASE

Z FLAT PACKAGE (TOP VIEW)



NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1)	14 V
Supply voltage V_{CC-} (see Note 1)	−7 V
Differential input voltage (see Note 2)	±5 V
Input voltage (either input, see Note 1)	±7 V
Strobe Voltage (see Note 1)	6 V
Peak output current ($t_w \leq 1$ s)	50 mA
Continuous total power dissipation at (or below) 70°C free-air temperature (see Note 3)	300 mW
Operating free-air temperature range: SN52811 Circuits	−55°C to 125°C
SN72811 Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J, L, or Z package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTES:
1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. For operation of the SN52811 above 70°C free-air temperature, refer to Dissipating Derating Curve, Figure 10.

electrical characteristics at specified free-air temperature, V_{CC+} = 12 V, V_{CC-} = −6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN52811			SN72811			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S \leq 200\ \Omega$, V_{IC} = 0, See Note 4	25°C		1	3.5		1	5	mV
			Full range			4.5			6	
		$R_S \leq 200\ \Omega$, See Note 4	25°C		1	5		1	7.5	
			Full range			6			10	
α_{VIO}	Average temperature coefficient of input offset voltage	$R_S \leq 200\ \Omega$, V_{IC} = 0, See Note 4	Full range		5			5		μV/°C
I_{IO}	Input offset current	See Note 4	25°C		0.5	3		0.5	5	μA
			Full range			5			10	
I_{IB}	Input bias current	See Note 4	25°C		7	20		7	30	μA
			Full range			30			50	
I_{SL}	Low-level strobe current	$V_{(strobe)}$ = −100 mV	25°C		−1.2	−2.5		−1.2	−2.5	mA
V_{ICR}	Common-mode input voltage range	V_{CC-} = −7 V	25°C	±5			±5			V
V_{ID}	Differential input voltage range		25°C	±5			±5			V
A_{VD}	Large-signal differential voltage amplification	V_O = 0 to 2.5 V, No load	25°C	12,500	17,500		10,000	17,500		
			Full range	8,000			5,000			
V_{OH}	High-level output voltage	V_{ID} = 10 mV, I_{OH} = 0	25°C		4	5		4	5	V
		V_{ID} = 10 mV, I_{OH} = −5 mA	25°C	2.5	3.6		2.5	3.6		
V_{OL}	Low-level output voltage	V_{ID} = −10 mV, I_{OL} = 0	25°C	−1	−0.4	0‡	−1	−0.4	0‡	V
		V_{ID} = 10 mV, $V_{(strobe)}$ = 0.3 V, I_{OL} = 0	25°C	−1		0‡	−1		0‡	
I_{OL}	Low-level output current	V_{ID} = −10 mV, V_O = 0	25°C	0.5	0.8		0.5	0.8		mA
r_o	Output resistance	V_O = 1.4 V	25°C		200			200		Ω
CMRR	Common-mode rejection ratio	$R_S \leq 200\ \Omega$	25°C	70	90		65	90		dB
I_{CC+}	Supply current from V_{CC+}	V_{ID} = −5 to 5 V (−10 mV for typ),	25°C		6.5			6.5		mA
I_{CC-}	Supply current from V_{CC-}		25°C		−2.7			−2.7		mA
P_D	Total power dissipation	No load, See Note 5	25°C		94	150		94	200	mW

†Unless otherwise noted, all characteristics are measured with the strobe of the channel under test open, the strobe of the other channel grounded. Full range for SN52811 is −55°C to 125°C and for the SN72811 is 0°C to 70°C.

‡The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic leve only, e.g., when 0 V is the maximum, the minimum limit is a more-negative voltage.

NOTES: 4. These characteristics are verified by measurements at the following temperatures and output voltage levels: for SN5281 V_O = 1.8 V at T_A = −55°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1 V at T_A = 125°C; for SN72811, V_O = 1.5 V at T_A = 0° V_O = 1.4 V at T_A = 25°C, and V_O = 1.2 V at 70°C. These output voltage levels were selected to approximate the logic thresho voltages of the types of digital logic circuits these comparators are intended to drive.

5. The strobes are alternately grounded.

switching characteristics, V_{CC+} = 12 V, V_{CC-} = −6 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	SN52811			SN72811			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Response time	R_L = ∞, C_L = 5 pF, See Note 6		33	80		33		ns
Strobe release time	R_L = ∞, C_L = 5 pF, See Note 7		5	25		5		ns

NOTES: 6. The response time specified is for a 100-mV input step with 5-mV overdrive.

7. For testing purposes, the input bias conditions are selected to produce an output voltage of 1.4 V. A 5-mV overdrive is th added to the input bias voltage to produce an output voltage which rises above 1.4 V. The time interval is measured from the 5(point of the strobe voltage curve to the point where the overdriven output voltage crosses the 1.4 V level.

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DEFINITION OF TERMS

Input Offset Voltage (V_{IO}) The d-c voltage which must be applied between the input terminals to force the quiescent d-c output voltage to the specified level. The input offset voltage may also be defined for the case where two equal resistances (R_S) are inserted in series with the input leads.

Average Temperature Coefficient of Input Offset Voltage (α_{VIO}) The ratio of the change in input offset voltage to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{VIO} = \left| \frac{(V_{IO} @ T_{A(1)}) - (V_{IO} @ T_{A(2)})}{T_{A(1)} - T_{A(2)}} \right|$$ where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

Input offset Current (I_{IO}) The difference between the currents into the two input terminals with the output at the specified level.

Input Bias Current (I_{IB}) The average of the currents into the two input terminals with the output at the specified level.

Low-Level Strobe Current (I_{SL}) The current flowing out of the strobe at a low-level voltage.

Common-Mode Input Voltage Range (V_{ICR}) The range of common-mode voltage which if exceeded will cause the amplifier to cease functioning properly.

Differential Input Voltage Range (V_{ID}) The range of voltage between the two input terminals which if exceeded will cause the comparator to cease functioning properly.

Large-Signal Differential Voltage Amplification (A_{VD}) The ratio of the change in output voltage to the change in differential input voltage producing it.

High-Level Output Voltage (V_{OH}) The voltage at the output with the specified input conditions applied which should establish a high level at the output.

Low-Level Output Voltage (V_{OL}) The voltage at the output with the specified input conditions applied which should establish a low level at the output.

Low-Level Output Current (I_{OL}) The current flowing into the output at a specified low-level output voltage.

Output Resistance (r_o) The resistance between the output terminal and ground.

Common-Mode Rejection Ratio (CMRR) The ratio of differential voltage amplification to common-mode voltage amplification. This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.

Total Power Dissipation (P_D) The total d-c power supplied to the device less any power delivered from the device to a load. At no load: $P_D = V_{CC+} \cdot I_{CC+} + V_{CC-} \cdot I_{CC-}$.

Response Time The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial condition sufficient to saturate the output to an input level just barely in excess of that required to bring the output back to the logic threshold voltage. This excess is referred to as the voltage overdrive.

Strobe Release Time The time required for the output to rise to the logic threshold voltage after the strobe terminal has been driven from the low logic level to the high logic level. Appropriate input conditions are assumed.

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

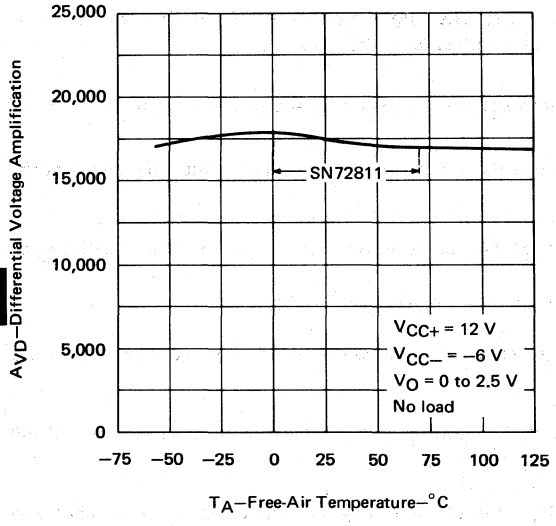

FIGURE 1

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

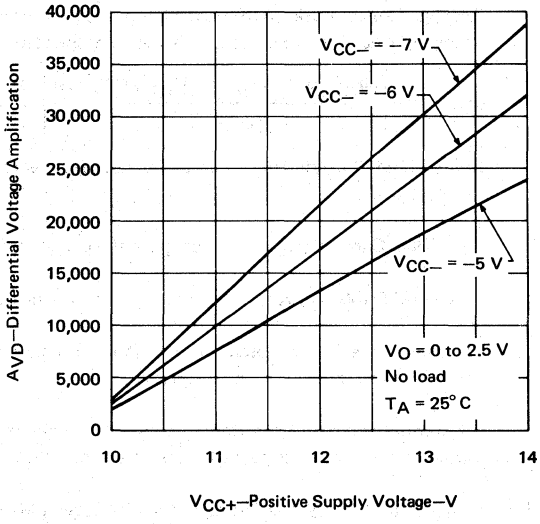

FIGURE 2

SN52811 VOLTAGE TRANSFER CHARACTERISTICS

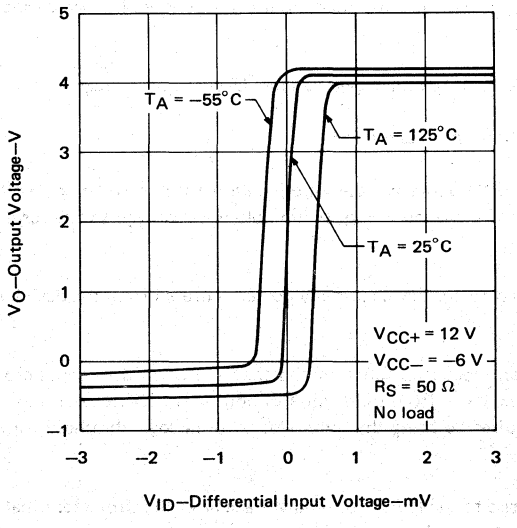

FIGURE 3

SN72811 VOLTAGE TRANSFER CHARACTERISTICS

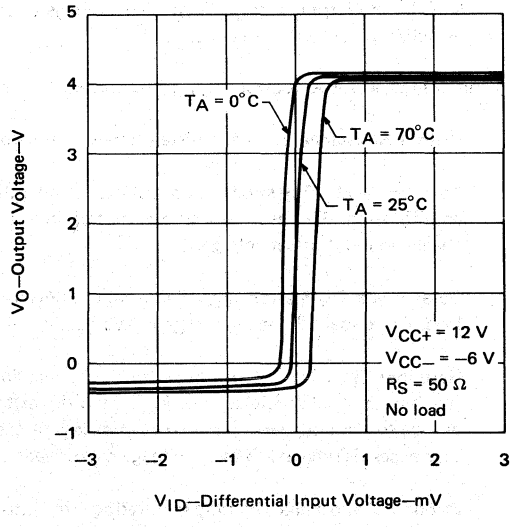

FIGURE 4

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TYPICAL CHARACTERISTICS

OUTPUT RESPONSE FOR
VARIOUS INPUT OVERDRIVES

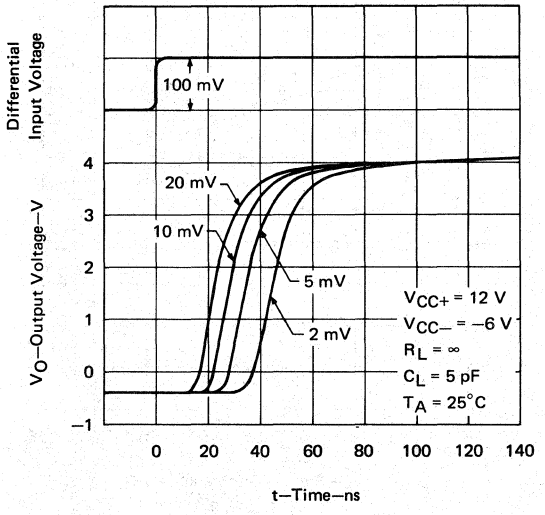


FIGURE 5

STROBE RELEASE TIME
FOR VARIOUS INPUT OVERDRIVES

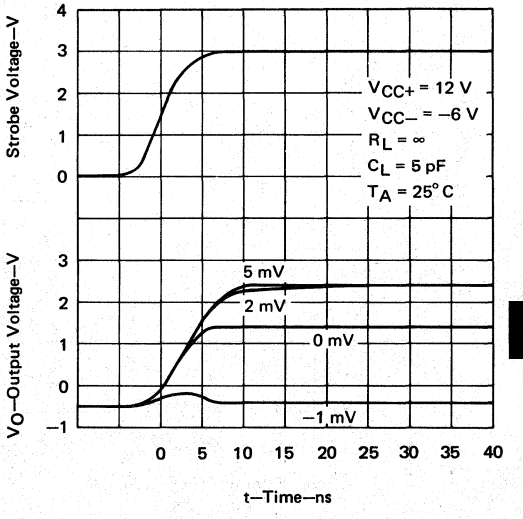


FIGURE 6

COMMON-MODE PULSE RESPONSE

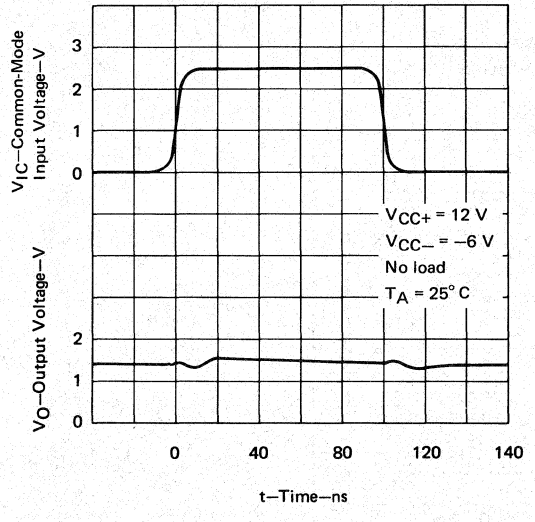
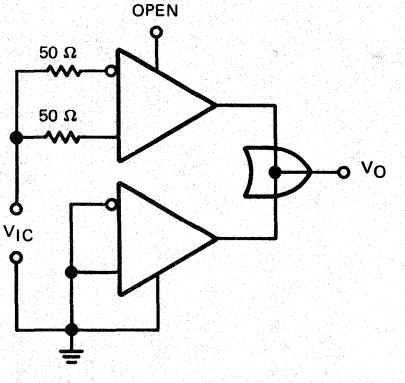


FIGURE 7



TEST CIRCUIT
FOR FIGURE 7

TYPICAL CHARACTERISTICS

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

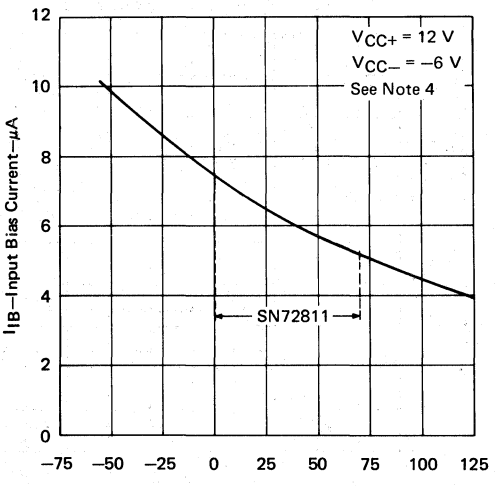


FIGURE 8

TOTAL POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

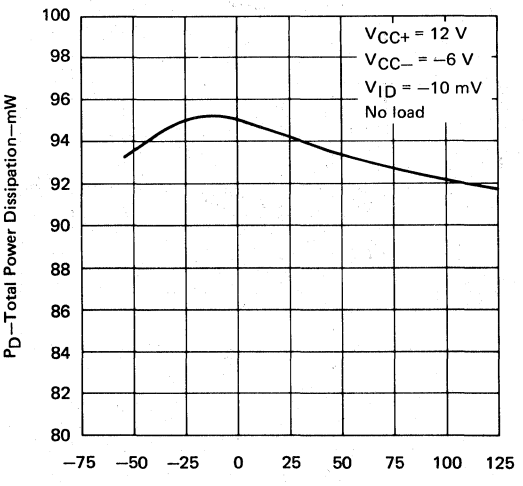


FIGURE 9

NOTE 4. These characteristics are verified by measurements at the following temperatures and output voltage levels: for SN52811, V_O = 1.8 V at T_A = −55°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1 V at T_A = 125°C; for SN72811, V_O = 1.5 V at T_A = 0°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1.2 V at 70°C. These output voltage levels were selected to approximate the logic threshold voltages of the types of digital logic circuits these comparators are intended to drive.

THERMAL INFORMATION

SN52811
DISSIPATION DERATING CURVE

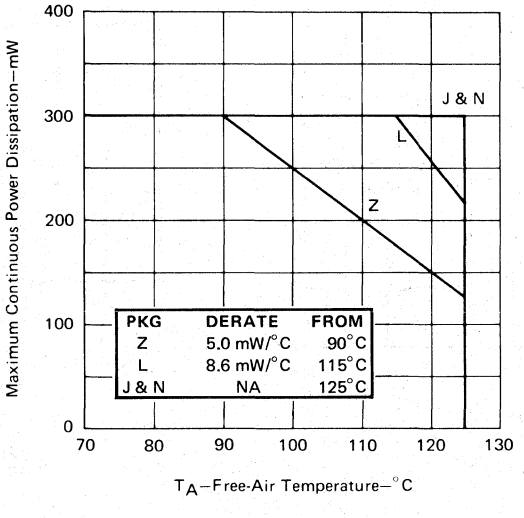


FIGURE 10

TEXAS INSTRUMENTS
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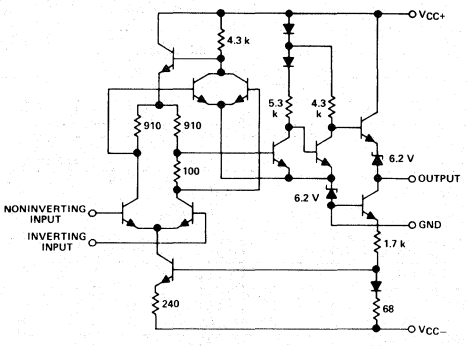
CIRCUIT TYPES SN52820, SN72820
DUAL DIFFERENTIAL COMPARATORS

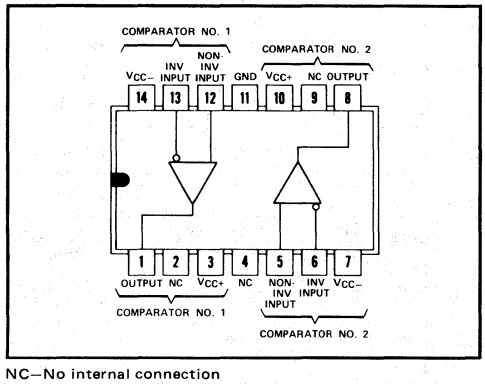
- Fast Response Times
- High Differential Voltage Amplification
- Low Offset Characteristics
- Outputs Compatible with Most TTL and DTL Circuits

schematic (each comparator)



Resistor values are in ohms.
Component values shown are nominal.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



NC—No internal connection

description

The SN52820 and SN72820 are improved versions of the SN72720 dual high-speed voltage comparator. Each comparator has differential inputs and a low-impedance output. When compared with the SN72720, these circuits feature higher amplification (typically 33,000) due to an extra amplification stage and increased accuracy because of lower offset characteristics. They are particularly useful in applications requiring an amplitude discriminator, memory sense amplifier, or a high-speed limit detector. The SN52820 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN72820 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1)	14 V
Supply voltage V_{CC-} (see Note 1)	−7 V
Differential input voltage (see Note 2)	±5 V
Input voltage (either input, see Note 1)	±7 V
Peak output current ($t_w \leq 1$ s)	10 mA
Continuous total power dissipation: each comparator	300 mW
total package, (see Note 3)	600 mW
Operating free-air temperature range: SN52820 Circuits	−55°C to 125°C
SN72820 Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. For SN52820, this rating applies at (or below) 95°C free-air temperature. For operation above this temperature, derate linearly at the rate of 10.9 mW/°C. For SN72820, this rating applies at (or below) 70°C free-air temperature without derating.

electrical characteristics at specified free-air temperature, V_{CC+} = 12 V, V_{CC-} = −6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN52820 MIN	SN52820 TYP	SN52820 MAX	SN72820 MIN	SN72820 TYP	SN72820 MAX	UNIT
V_{IO}	Input offset voltage	$R_S \leq 200\ \Omega$, See Note 4	25°C		0.6	2		1.6	3.5	mV
			Full range			3			4.5	
α_{VIO}	Average temperature coefficient of input offset voltage	R_S = 50 Ω, See Note 4	MIN to 25°C		3	10		3	20	μV/°C
			25°C to MAX		3	10		3	20	
I_{IO}	Input offset current	See Note 4	25°C		0.75	3		1.8	5	μA
			MIN		1.8	7			7.5	
			MAX		0.25	3			7.5	
α_{IIO}	Average temperature coefficient of input offset current	See Note 4	MIN to 25°C		15	75		24	100	nA/°C
			25°C to MAX		5	25		15	50	
I_{IB}	Input bias current	See Note 4	25°C		7	15		7	20	μA
			MIN		12	25		9	30	
V_{ICR}	Common-mode input voltage range	V_{CC-} = −7 V	Full range	±5			±5			V
V_{ID}	Differential input voltage range		Full range	±5			±5			V
A_{VD}	Large-signal differential voltage amplification	No load, V_O = 0 to 2.5 V	25°C	12,500	33,000		10,000	33,000		
			Full range	10,000			8,000			
V_{OH}	High-level output voltage	V_{ID} = 5 mV, I_{OH} = 0	Full range		4§	5		4§	5	V
		V_{ID} = 5 mV, I_{OH} = −5 mA	Full range	2.5	3.6§		2.5	3.6§		
V_{OL}	Low-level output voltage	V_{ID} = −5 mV, I_{OL} = 0	Full range	−1	−0.5§	0‡	−1	−0.5§	0‡	V
I_{OL}	Low-level output current	V_{ID} = −5 mV, V_O = 0	25°C	2	2.4		1.6	2.4		mA
			MIN	1	2.3		0.5	2.4		
			MAX	0.5	2.3		0.5	2.4		
r_o	Output resistance	V_O = 1.4 V	25°C		200			200		Ω
CMRR	Common-mode rejection ratio	$R_S \leq 200\ \Omega$	Full range	80	100§		70	100§		dB
I_{CC+}	Supply current from V_{CC+} (each comparator)	V_{ID} = −5 mV, No load	Full range		5.5§	9		5.5§	9	mA
I_{CC-}	Supply current from V_{CC-} (each comparator)		Full range		−3.5§	−7		−3.5§	−7	mA
P_D	Total power dissipation (each comparator)		Full range		90§	150		90§	150	mW

†Full range (MIN to MAX) for SN52820 is −55°C to 125°C and for the SN72820 is 0°C to 70°C.

‡The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic levels only, e.g., when 0 V is the maximum, the minimum limit is a more-negative voltage.

§These typical values are at T_A = 25°C.

NOTE 4: These characteristics are verified by measurements at the following temperatures and output voltage levels: for SN52820, V_O = 1.8 V at T_A = −55°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1V at T_A = 125°C; for SN72820, V_O = 1.5 V at T_A = 0°C, V_O = 1.4 V at 25°C, and V_O = 1.2 V at T_A = 70°C. These output voltage levels were selected to approximate the logic threshold voltages of the types of digital logic circuits these comparators are intended to drive.

switching characteristics, V_{CC+} = 12 V, V_{CC-} = −6 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Response time	R_L = ∞, C_L = 5 pF, See Note 5		30	80	ns

NOTE 5: The response time specified is for a 100-mV input step with 5-mV overdrive.

For definition of terms and typical characteristic curves, see the SN52810/SN72810 data sheet on page 3-79.

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TYPE	SN52733, SN72733	SN5510, SN7510	SN5511, SN7511	SN5512, SN7512	SN5514, SN7514	UNIT
Differential Voltage Amplification, Typ	10 to 400 (Adjustable)	93	3000	300	300	
Bandwidth (−3 dB), Typ	200 (Gain of 10)	40	3	80	80	MHz
Bandwidth (Unity-Gain), Typ	400	300	100	400	400	MHz
Input Offset Current, Typ	0.4	3	0.6	1	1	μA
Input Offset Voltage, Typ	1.5 (Gain of 400)	5	1	1 (can be nulled)	1	mV
Output Voltage Swing, Typ	4.7	4	5	3.4	3.4	V p-p
Packages	L, N	F, L	F, L, N	L	L	

CIRCUIT TYPES SN52733, SN72733
DIFFERENTIAL VIDEO AMPLIFIERS

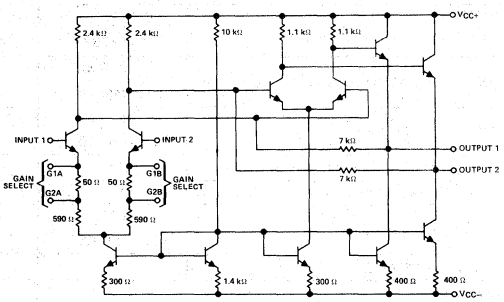
- 200 MHz Bandwidth
- 250 kΩ Input Resistance
- Selectable Nominal Amplification of 10, 100, or 400
- No Frequency Compensation Required

description

The SN52733 and SN72733 are monolithic two-stage video amplifiers with differential inputs and differential outputs.

Internal series-shunt feedback provides wide bandwidth, low phase distortion, and excellent gain stability. Emitter-follower outputs enable the device to drive capacitive loads and all stages are current-source biased to obtain high common-mode and supply-voltage rejection ratios.

schematic



Component values shown are nominal

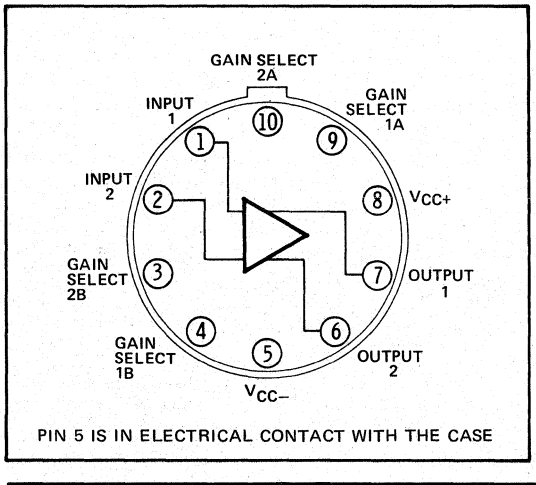
Fixed differential amplification of 10, 100, or 400 may be selected without external components, or amplification may be adjusted from 10 to 400 by the use of a single external resistor connected between G1A and G1B. No external frequency-compensating components are required for any gain option.

The device is particularly useful in magnetic-tape or disc-file systems using phase or NRZ encoding and in high-speed thin-film or plated-wire memories. Other applications include general purpose video and pulse amplifiers where wide bandwidth, low phase shift, and excellent gain stability are required.

The SN52733 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN72733 is characterized for operation from 0°C to 70°C.

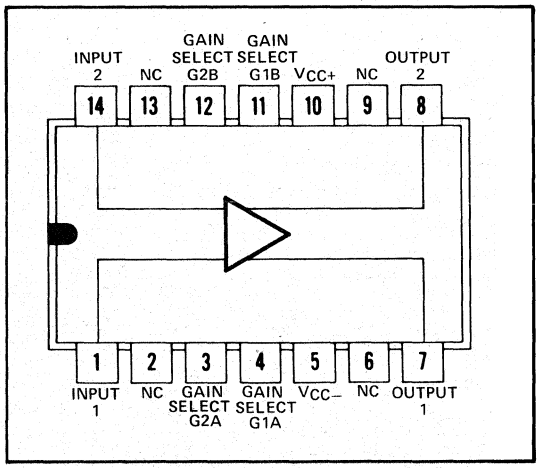
terminal assignments

L PLUG-IN-PACKAGE
(TOP VIEW)



PIN 5 IS IN ELECTRICAL CONTACT WITH THE CASE

N DUAL-IN-LINE PACKAGE
(TOP VIEW)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN52733	SN72733	UNIT
Supply voltage V_{CC+} (See Note 1)		8	8	V
Supply voltage V_{CC-} (See Note 1)		−8	−8	V
Differential input voltage		±5	±5	V
Common-mode input voltage		±6	±6	V
Output current		10	10	mA
Continuous total power dissipation (See Note 2 on the following page)		500	500	mW
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16" from case for 60 seconds	L package	300	300	°C
Lead temperature 1/16" from case for 10 seconds	N package	260	260	°C

NOTE 1: All voltage values, except differential input voltages, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC+} and V_{CC-}.

electrical characteristics, T_A = 25°C, V_{CC+} = 6 V, V_{CC-} = −6 V

PARAMETER		TEST FIGURE	TEST CONDITIONS	GAIN† SELECT	SN52733 MIN	SN52733 TYP	SN52733 MAX	SN72733 MIN	SN72733 TYP	SN72733 MAX	UNIT
A_{VD}	Large-signal differential voltage amplification	1	V_{OD} = 1 V	1	300	400	500	250	400	600	
				2	90	100	110	80	100	120	
				3	9	10	11	8	10	12	
BW	Bandwidth	2	R_S = 50 Ω	1		50			50		MHz
				2		90			90		
				3		200			200		
I_{IO}	Input offset current			Any		0.4	3		0.4	5	μA
I_{IB}	Input bias current			Any		9	20		9	30	μA
V_I	Input voltage range	1		Any	±1			±1			V
V_{OC}	Common-mode output voltage	1		Any	2.4	2.9	3.4	2.4	2.9	3.4	V
V_{OO}	Output offset voltage	1		1		0.6	1.5		0.6	1.5	V
				2 & 3		0.35	1		0.35	1.5	
V_{OPP}	Maximum peak-to-peak output voltage swing	1		Any	3	4.7		3	4.7		V
r_i	Input resistance	3	$V_{OD} \leq$ 1 V	1		4			4		kΩ
				2	20	24		10	24		
				3		250			250		
r_o	Output resistance					20			20		Ω
C_i	Input capacitance	3	$V_{OD} \leq$ 1 V	2		2			2		pF
CMRR	Common-mode rejection ratio	4	V_{IC} = ±1 V, f ≤ 100 kHz	2	60	86		60	86		dB
			V_{IC} = ±1 V, f = 5 MHz	2		70			70		
$\Delta V_{CC}/\Delta V_{IO}$	Supply voltage rejection ratio	1	ΔV_{CC+} = ± 0.5 V, ΔV_{CC-} = ± 0.5 V	2	50	70		50	70		dB
V_n	Broadband equivalent input noise voltage	5	BW = 1 kHz to 10 MHz	Any		12			12		μV
t_{pd}	Propagation delay time	2	R_S = 50 Ω, Output voltage step = 1 V	1		7.5			7.5		ns
				2		6.0	10		6.0	10	
				3		3.6			3.6		
t_r	Rise time	2	R_S = 50 Ω, Output voltage step = 1 V	1		10.5			10.5		ns
				2		4.5	10		4.5	12	
				3		2.5			2.5		
$I_{sink(max)}$	Maximum output sink current			Any	2.5	3.6		2.5	3.6		mA
I_{CC}	Supply current		No load, no signal	Any		16	24		16	24	mA

†The gain selection is made as follows:
Gain 1 . . . Gain Select pin G1A is connected to pin G1B, and pins G2A and G2B are open.
Gain 2 . . . Gain Select pin G1A and pin G1B are open, pin G2A is connected to pin G2B.
Gain 3 . . . All four gain-select pins are open.

DEFINITION OF TERMS

Large-Signal Differential Voltage Amplification (A_{VD}) The ratio of the change in voltage between the output terminals to the change in voltage between the input terminals producing it.

Bandwidth (BW) The range of frequencies within which the differential gain of the amplifier is not more than 3 dB below its low-frequency value.

Input Offset Current (I_{IO}) The difference between the currents into the two input terminals with the inputs grounded.

Input Bias Current (I_{IB}) The average of the currents into the two input terminals with the inputs grounded.

Input Voltage Range (V_I) The range of voltage which if exceeded at either input terminal will cause the amplifier to cease functioning properly.

Common-Mode Output Voltage (V_{OC}) The average of the d-c voltages at the two output terminals.

Output Offset Voltage (V_{OO}) The difference between the d-c voltages at the two output terminals when the input terminals are grounded.

Maximum Peak-to-Peak Output Voltage Swing (V_{OPP}) The maximum peak-to-peak output voltage swing that can be obtained without clipping. This includes the unbalance caused by output offset voltage.

Input Resistance (r_i) The resistance between the input terminals with either input grounded.

Output Resistance (r_o) The resistance between either output terminal and ground.

Input Capacitance (C_i) The capacitance between the input terminals with either input grounded.

Common-Mode Rejection Ratio (CMRR) The ratio of differential voltage amplification to common-mode voltage amplification. This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in output offset voltage referred to the input.

Supply Voltage Rejection Ratio ($\Delta V_{CC}/\Delta V_{IO}$) The ratio of the change in power supply voltages to the change in output offset voltage referred to the input. For these devices, both supply voltages are varied symmetrically.

Propagation Delay Time (t_{pd}) The interval between the application of an input voltage step and its arrival at either output, measured at 50% of the final value.

Rise Time (t_r) The time required for an output voltage step to change from 10% to 90% of its final value.

Maximum Output Sink Current ($I_{sink(max)}$) The maximum available current into either output terminal when that output is at its most negative potential.

Supply Current (I_{CC}) The average of the magnitudes of the two supply currents.

NOTE 2: For SN52733 in the L package, this rating applies at (or below) 90°C free-air temperature with derating above that temperature at the rate of 8.3 mW/°C. For SN52733 in the N package, this rating applies at (or below) 105°C free-air temperature with derating above that temperature at the rate of 11.1 mW/°C. For SN72733 in either package, this rating applies at (or below) 70°C free-air temperature without derating.

TEXAS INSTRUMENTS
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PARAMETER MEASUREMENT INFORMATION

test circuits

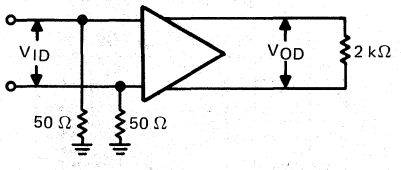


FIGURE 1

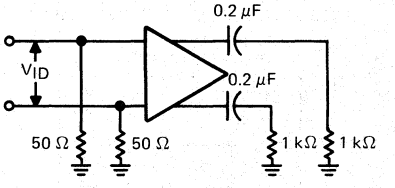


FIGURE 2

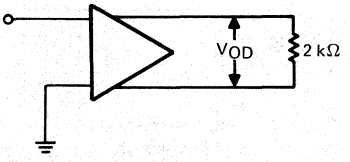


FIGURE 3

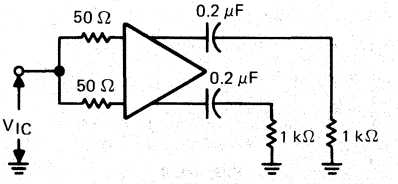


FIGURE 4

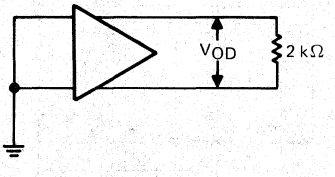
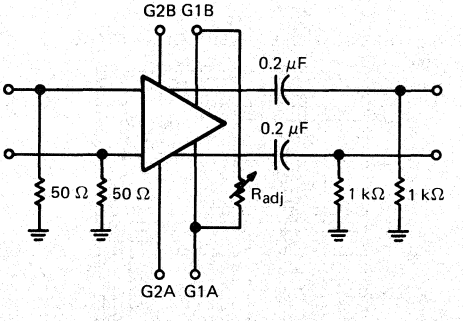


FIGURE 5



VOLTAGE AMPLIFICATION ADJUSTMENT

FIGURE 6

TYPICAL CHARACTERISTICS

PHASE SHIFT
vs
FREQUENCY

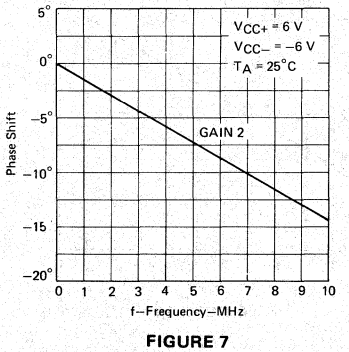


FIGURE 7

PHASE SHIFT
vs
FREQUENCY

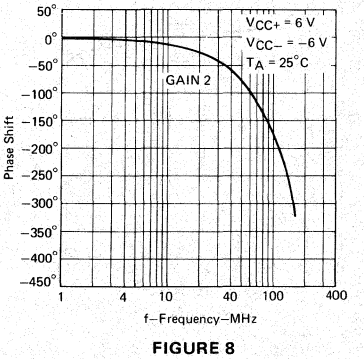


FIGURE 8

TYPICAL CHARACTERISTICS

VOLTAGE AMPLIFICATION
(SINGLE-ENDED OR DIFFERENTIAL)
vs
TEMPERATURE

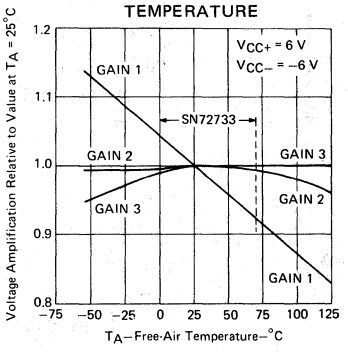


FIGURE 9

VOLTAGE AMPLIFICATION
(SINGLE-ENDED OR DIFFERENTIAL)
vs
SUPPLY VOLTAGE

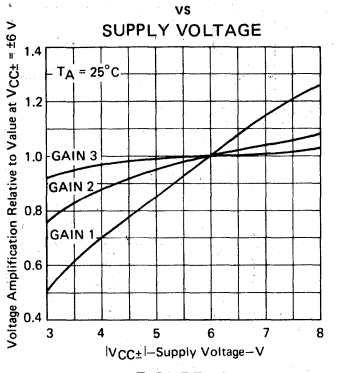


FIGURE 10

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
RESISTANCE BETWEEN G1A AND G1B

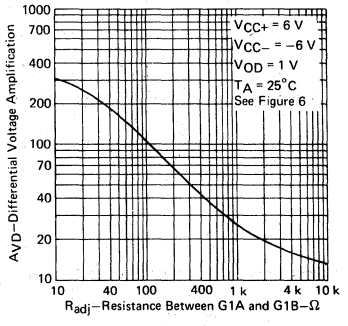


FIGURE 11

SINGLE-ENDED VOLTAGE AMPLIFICATION
vs
FREQUENCY

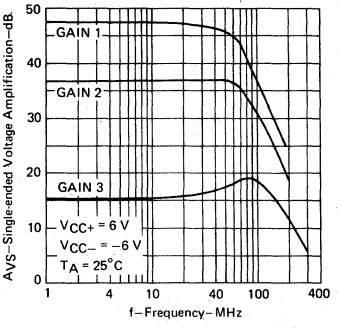


FIGURE 12

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

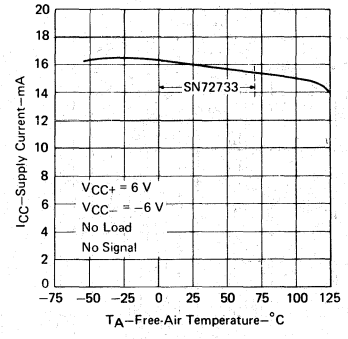


FIGURE 13

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

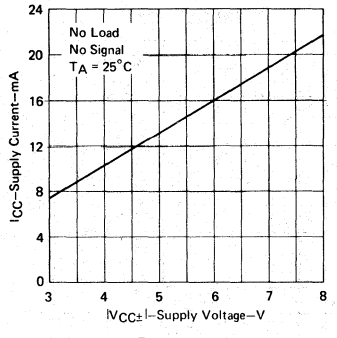


FIGURE 14

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TYPICAL CHARACTERISTICS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
LOAD RESISTANCE

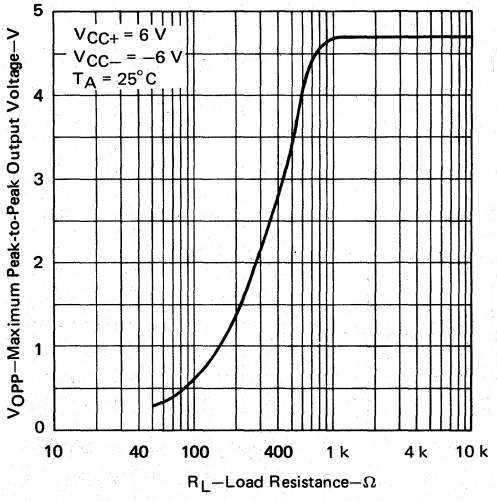

FIGURE 15

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

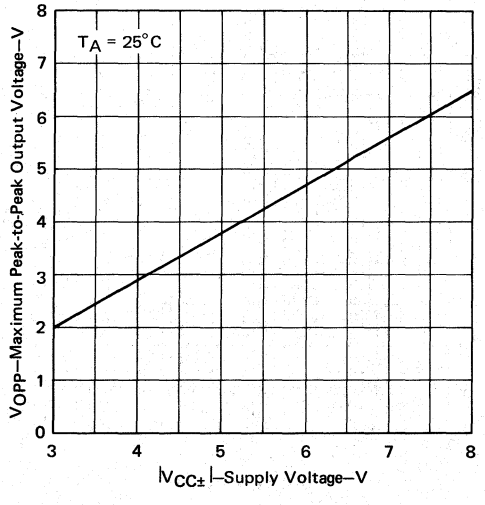

FIGURE 16

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

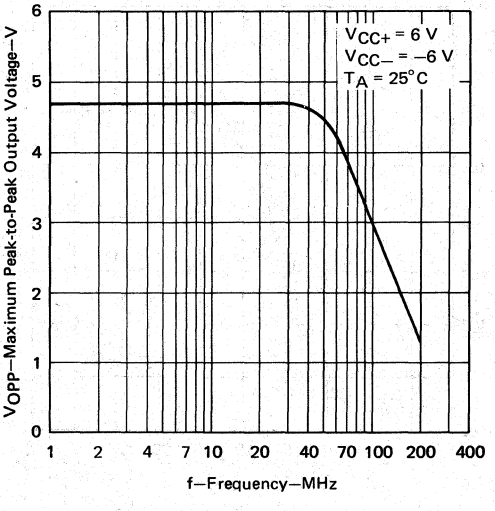

FIGURE 17

INPUT RESISTANCE
vs
FREE-AIR TEMPERATURE

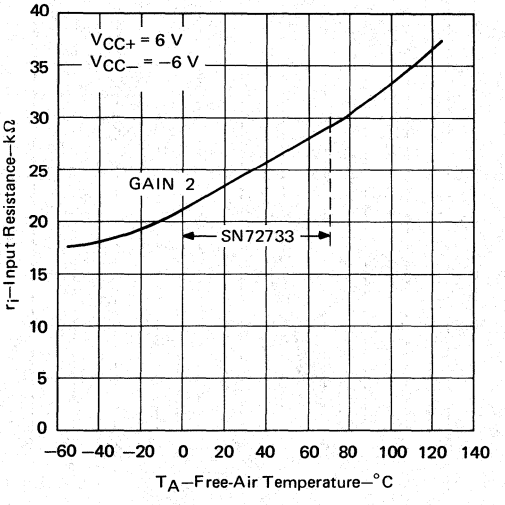

FIGURE 18

TYPICAL CHARACTERISTICS

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

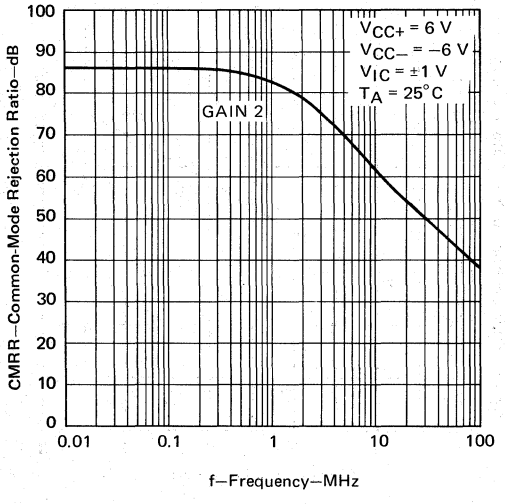

FIGURE 19

DIFFERENTIAL INPUT OVERLOAD RECOVERY TIME
vs
DIFFERENTIAL INPUT VOLTAGE

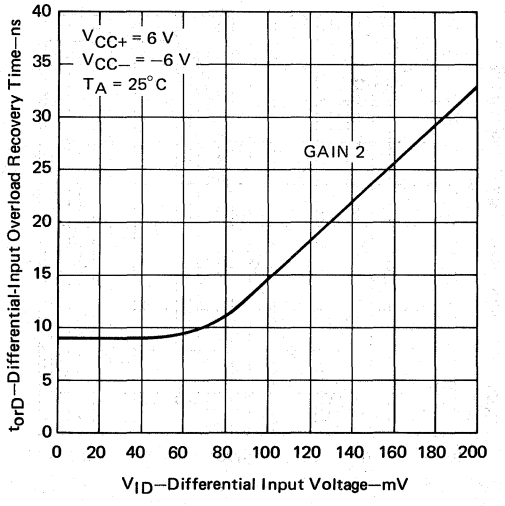

FIGURE 20

PULSE RESPONSE
AS A FUNCTION OF
SUPPLY VOLTAGE

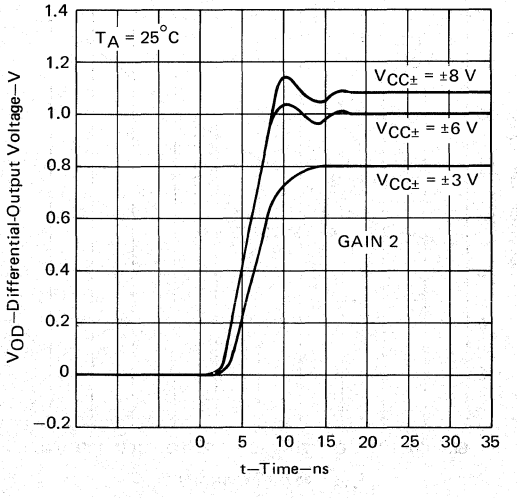

FIGURE 21

PULSE RESPONSE
AS A FUNCTION OF GAIN

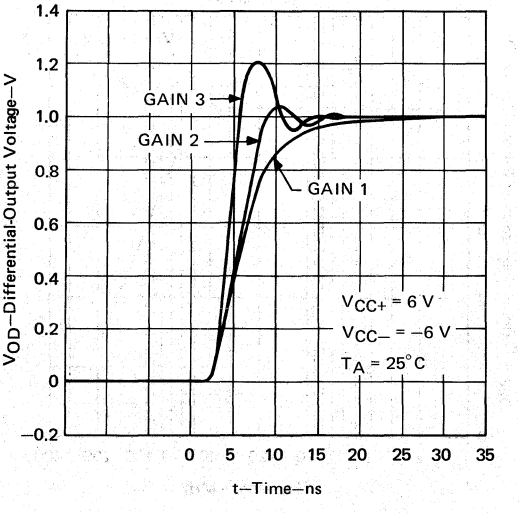

FIGURE 22

TEXAS INSTRUMENTS
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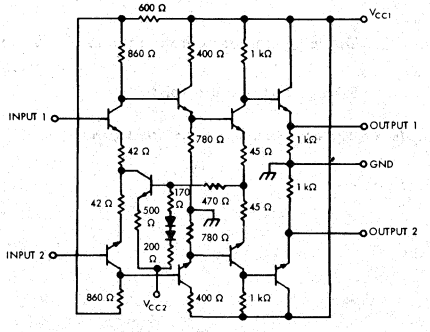
WIDE-BAND VIDEO AMPLIFIER
FEATURING
Flat Frequency Response with Low Phase-Shift from DC to 40 MHz

description

This wide-band video amplifier features a flat frequency response and low phase-shift from dc to 40 MHz. Differential inputs and outputs are provided which permit it to be used as a high-frequency differential amplifier.

Elements of the SN5510 video-amplifier bar include transistors with transition frequency as high as 1.2 GHz under low-current and low-V_{CE} conditions. Circuit frequency response from dc to greater than 100 MHz is possible.

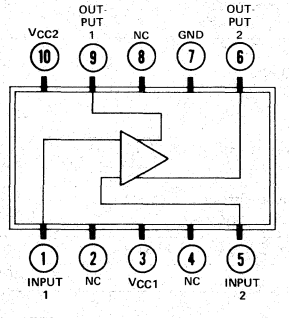
schematic



Component values shown are nominal.

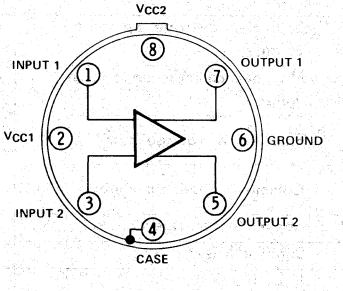
terminal assignments

F
FLAT PACKAGE (TOP VIEW)



THE CIRCUIT IS ELECTRICALLY INSULATED FROM THE CASE

L
PLUG-IN PACKAGE (TOP VIEW)



THE CIRCUIT IS ELECTRICALLY INSULATED FROM THE CASE

NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltages (See Note 1): V_{CC1} . . . . . +8 V
V_{CC2} . . . . . −8 V
Differential input voltage . . . . . 5 V
Positive input voltage (See Note 1) . . . . . V_{CC1}
Negative input voltage (See Note 1) . . . . . V_{CC2}
Operating free-air temperature ranges: SN5510F . . . . . −55°C to 70°C
SN5510L . . . . . −55°C to 100°C
Operating case temperature ranges: SN5510F . . . . . −55°C to 100°C
SN5510L . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These voltage values are with respect to network ground.

3

electrical characteristics, $T_A = 25°C$, $V_{CC1} = +6$ V, $V_{CC2} = -6$ V

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DO}	Differential-output offset voltage	1			0.5	1.3	V
$V_{CMO(av)}$	Average common-mode output offset voltage	1		2.6	3.1	3.5	V
I_{in}	Input current	1			40	80	μA
I_{DI}	Differential-input offset current	1			3	20	μA
D_S	Single-ended output distortion	2	Load resistance = 5 kΩ, input distortion < 0.2%, V_{out} = 1 V rms, f = 10 kHz		1.5	5	%
$V_{N(in)}$	Equivalent average input noise voltage	3	Single-ended, R_S = 0, f = 10 Hz to 500 kHz		5		μV
V_{CMIM}	Maximum common-mode input voltage				±1		V
A_{vs}	Small-signal voltage gain	2	Single-ended, load resistance = 5 kΩ, f = 100 kHz	75	93	110	
A_{vcm}	Common-mode-input voltage gain	4	Single-ended, load resistance = 5 kΩ, V_{in} = 0.3 V rms, f = 100 kHz		−45	−30	dB
CMRR	Common-mode rejection ratio	4	Load resistance = 5 kΩ, f = 100 kHz		85		dB
BW	Bandwidth (−3 dB)	2			40		MHz
r_{in}	Input resistance	5	f = 100 kHz		6		kΩ
C_{in}	Input capacitance	5	f = 100 kHz		7		pF
z_{out}	Output impedance	5	f = 100 kHz		35		Ω
P_T	Total power dissipation	1	No input signal, no external load		165	220	mW
t_r	Rise time	6	Single-ended, V_{in} = 5 mV		9	12	ns
t_f	Fall time	6	Single-ended, V_{in} = 5 mV		9	12	ns

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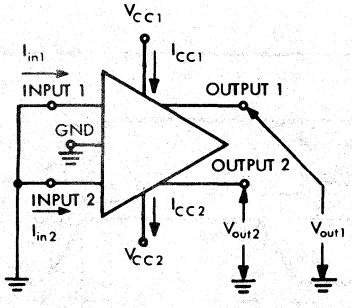
letter symbol and parameter definitions

V_{DO}	The d-c differential voltage that exists between the output terminals when the input terminals are at ground.
$V_{CMO(av)}$	The average of the d-c output voltages with respect to ground when the input terminals are grounded.
I_{DI}	The difference in the currents into the two input terminals.
V_{CMIM}	The maximum common-mode voltage that can be impressed on the input terminals while maintaining differential operation.
CMRR	The ratio of the differential-mode voltage gain to the common-mode voltage gain.
BW	The range of frequencies within which the open-loop voltage gain is within 3 dB of the mid-frequency value.

3

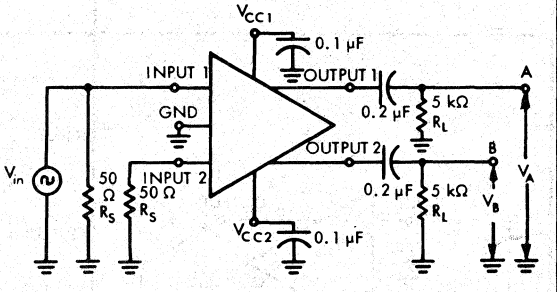
PARAMETER MEASUREMENT INFORMATION

test circuits



1. $V_{DO} = |V_{out1} - V_{out2}|$
2. $V_{CMO(av)} = \dfrac{V_{out1} + V_{out2}}{2}$
3. $I_{DI} = |I_{in1} - I_{in2}|$
4. $P_T = |V_{CC1} \bullet I_{CC1}| + |V_{CC2} \bullet I_{CC2}|$

FIGURE 1



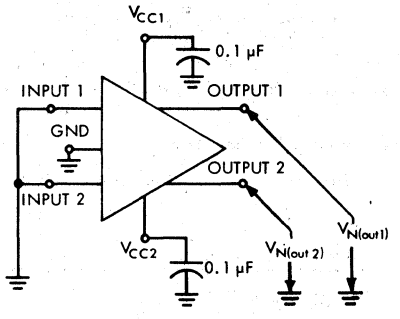
1. Single-ended output distortion is measured at A or B with V_A or V_B = 1 V rms, input distortion < 0.2%, and f = 10 kHz.
2. $A_{VS} = \left|\dfrac{V_A \text{ or } V_B}{V_{in}}\right|$

where: V_{in} = 1 mV rms and f = 100 kHz.

FIGURE 2

PARAMETER MEASUREMENT INFORMATION

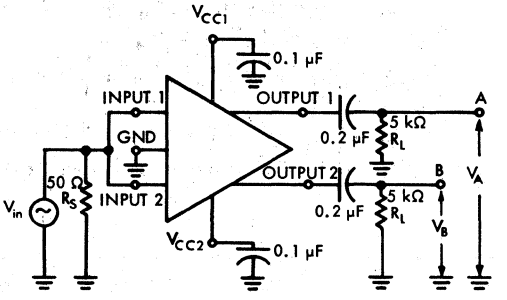
test circuits (continued)



1. $V_{\overline{N(in)}} = \dfrac{V_{\overline{N(out1)}} \text{ or } V_{\overline{N(out2)}}}{A_{VS}}$

where: $V_{\overline{N(out)}}$ = true rms broad-band noise voltage from 10 Hz to 500 kHz.

FIGURE 3



1. $A_{vcm} = 20 \text{ Log} \left| \dfrac{V_A \text{ or } V_B}{V_{in}} \right|$

where: V_{in} = 0.3 V rms and f = 100 kHz.

2. CMRR = 20 Log $A_{VS} - A_{vcm}$

FIGURE 4

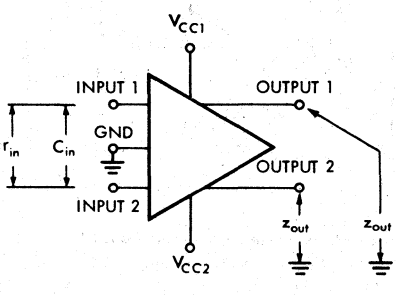
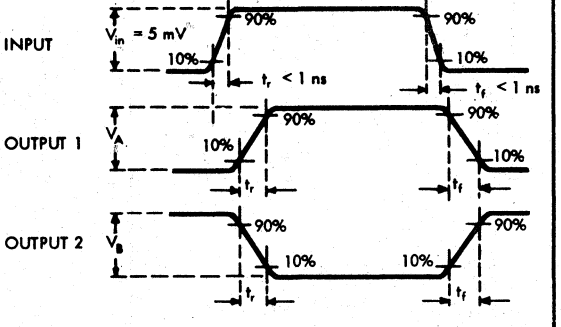


FIGURE 5



1. Test circuit is identical to that shown in Figure 2.

FIGURE 6 — t_r and t_f VOLTAGE WAVEFORMS

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TYPICAL CHARACTERISTICS†

AVERAGE COMMON-MODE OUTPUT OFFSET VOLTAGE
vs
FREE-AIR TEMPERATURE

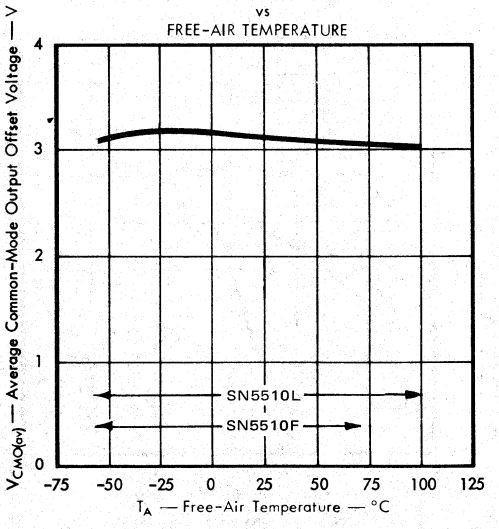

FIGURE 7

INPUT CURRENT
vs
FREE-AIR TEMPERATURE

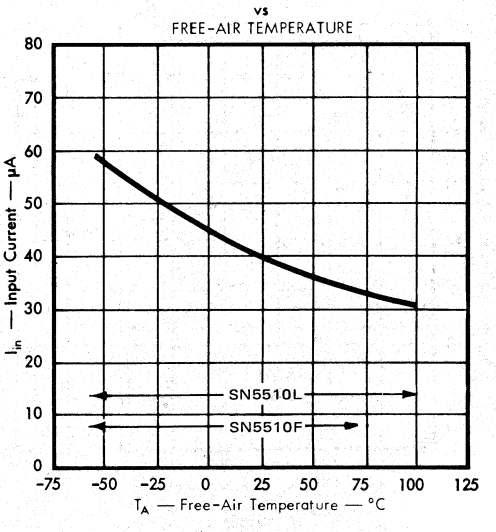

FIGURE 8

PEAK-TO-PEAK OUTPUT VOLTAGE
vs
LOAD RESISTANCE

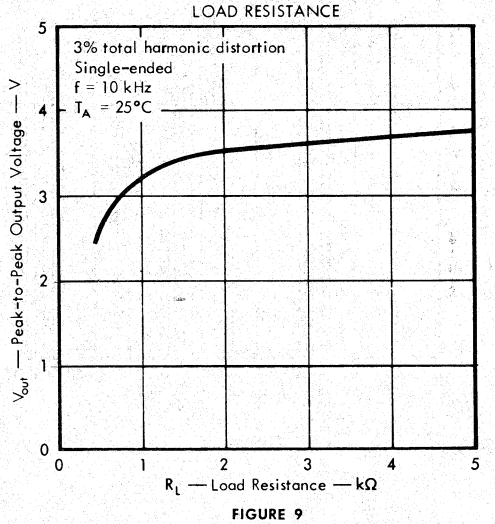

FIGURE 9

PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

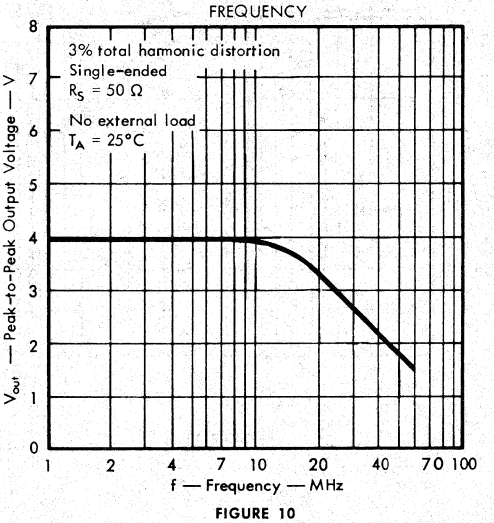

FIGURE 10

†Unless otherwise noted $V_{CC1} = +6$ V, $V_{CC2} = -6$ V.

TYPICAL CHARACTERISTICS†

SMALL-SIGNAL VOLTAGE GAIN
vs
FREE-AIR TEMPERATURE

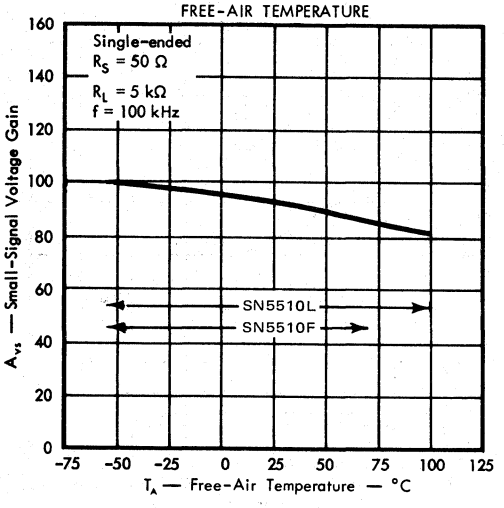

FIGURE 11

SMALL-SIGNAL VOLTAGE GAIN VARIATION
vs
SUPPLY VOLTAGE

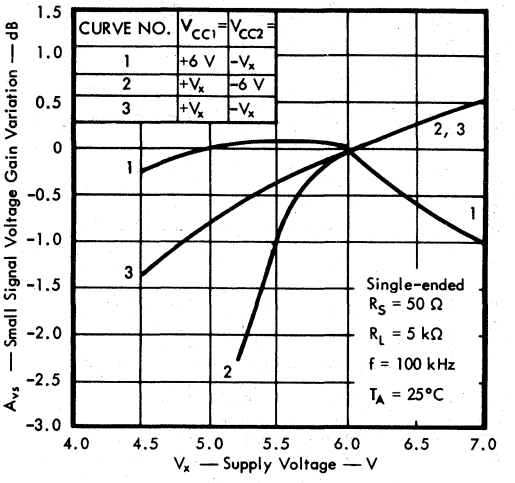

FIGURE 12

SMALL-SIGNAL VOLTAGE GAIN
vs
FREQUENCY

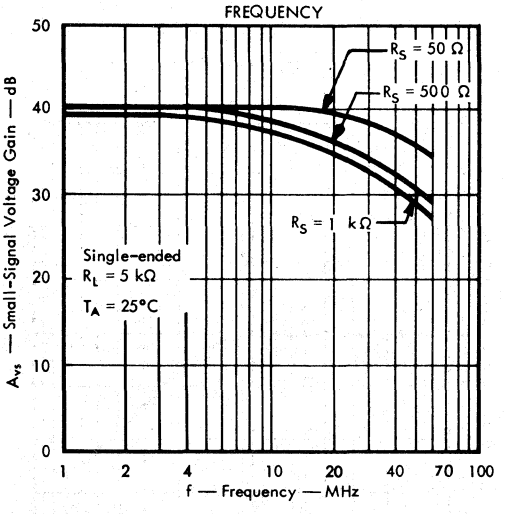

FIGURE 13

SMALL-SIGNAL VOLTAGE GAIN
vs
FREQUENCY

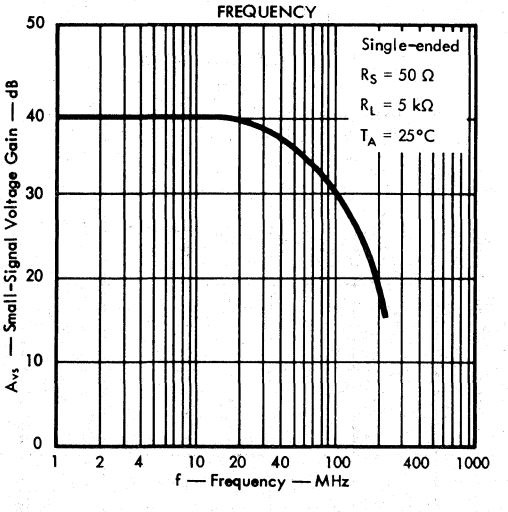

FIGURE 14

†Unless otherwise noted V_{CC1} = +6 V, V_{CC2} = −6 V.

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TYPICAL CHARACTERISTICS†

PHASE SHIFT
vs
FREQUENCY

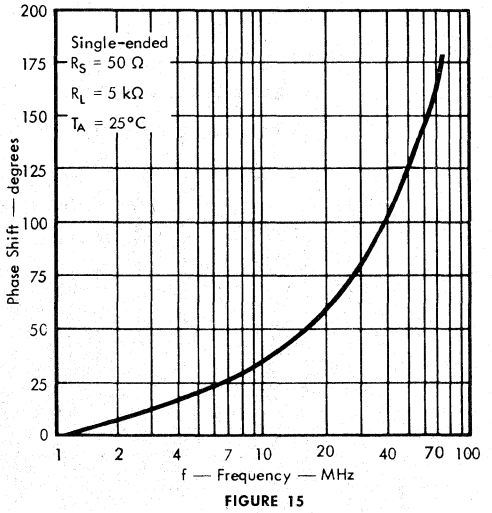


FIGURE 15

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

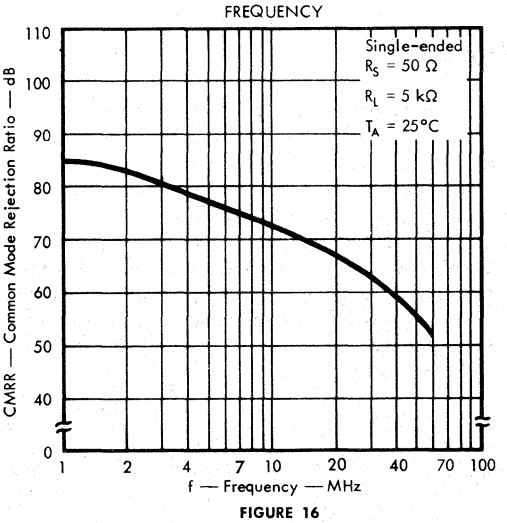
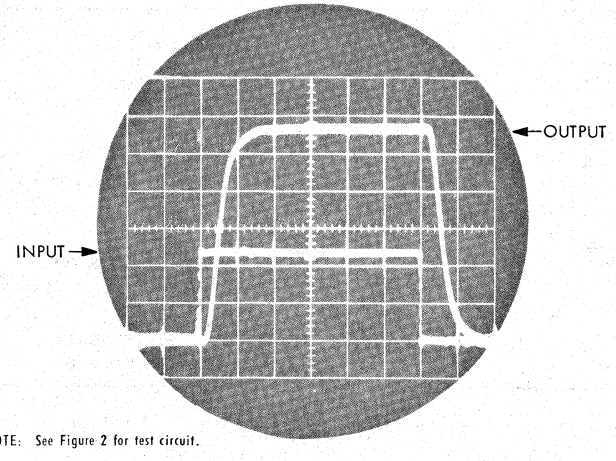


FIGURE 16

†V_{CC1} = +6 V and V_{CC2} = −6 V.



SCALES

Horizontal: 10 ns/division
Vertical: Output = 200 mV/division
Input = 5 mV/division

NOTE: See Figure 2 for test circuit.

FIGURE 17 — OSCILLOSCOPE PRESENTATION OF PULSE RESPONSE

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CIRCUIT TYPE SN7510
DIFFERENTIAL VIDEO AMPLIFIER

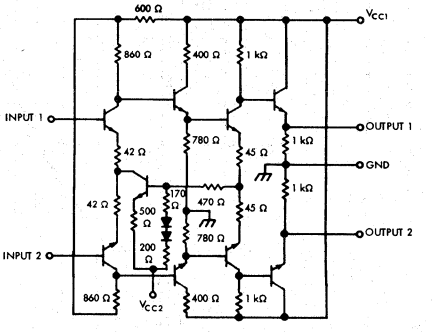
WIDE-BAND VIDEO AMPLIFIER
FEATURING
Flat Frequency Response with Low Phase-Shift from DC to 40 MHz

description

This wide-band video amplifier features a flat frequency response and low phase-shift from dc to 40 MHz. Differential inputs and outputs are provided which permit it to be used as a high-frequency differential amplifier.

Elements of the SN7510 video-amplifier bar include transistors with transition frequency as high as 1.2 GHz under low-current and low-V_{CE} conditions. Circuit frequency response from dc to greater than 100 MHz is possible.

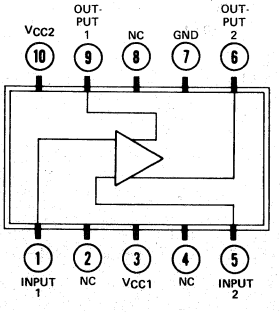
schematic



Component values shown are nominal.

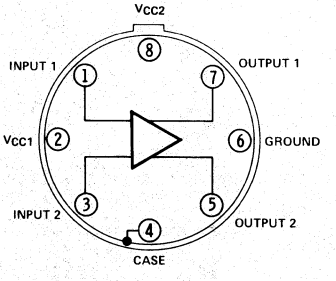
terminal assignments

F
FLAT PACKAGE (TOP VIEW)



THE CIRCUIT IS ELECTRICALLY INSULATED FROM THE CASE

L
PLUG-IN PACKAGE (TOP VIEW)



THE CIRCUIT IS ELECTRICALLY INSULATED FROM THE CASE

NC—No internal connection

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltages (See Note 1): V_{CC1} . . . . . +8 V
V_{CC2} . . . . . −8 V
Differential input voltage . . . . . 5 V
Positive input voltage (See Note 1) . . . . . V_{CC1}
Negative input voltage (See Note 1) . . . . . V_{CC2}
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These voltage values are with respect to network ground.

3

electrical characteristics, $T_A = 25°C$, $V_{CC1} = +6$ V, $V_{CC2} = -6$ V

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DO}	Differential-output offset voltage	1			0.5	2	V
$V_{CMO(av)}$	Average common-mode output offset voltage	1		2	3	4	V
I_{in}	Input current	1			50	100	μA
I_{DI}	Differential-input offset current	1			5	30	μA
V_{OM}	Maximum peak-to-peak output voltage	2	Single-ended, load resistance = 5 kΩ, f = 100 kHz, V_{in} = 20 mV rms		4.5		V
D_S	Single-ended output distortion	2	Load resistance = 5 kΩ, input distortion < 0.2%, V_{out} = 1 V rms, f = 10 kHz		2		%
$V_{N(in)}$	Equivalent average input noise voltage	3	Single-ended, R_S = 0, f = 10 Hz to 500 kHz		5		μV
V_{CMIM}	Maximum common-mode input voltage				±1		V
A_{vs}	Small-signal voltage gain	2	Single-ended, load resistance = 5 kΩ, f = 100 kHz	60	90	120	
A_{vcm}	Common-mode-input voltage gain	4	Single-ended, load resistance = 5 kΩ, V_{in} = 0.3 V rms, f = 100 kHz		−40	−20	dB
CMRR	Common-mode rejection ratio	4	Load resistance = 5 kΩ, f = 100 kHz		85		dB
BW	Bandwidth (−3 dB)	2			40		MHz
r_{in}	Input resistance	5	f = 100 kHz		6		kΩ
C_{in}	Input capacitance	5	f = 100 kHz		7		pF
z_{out}	Output impedance	5	f = 100 kHz		35		Ω
P_T	Total power dissipation	1	No input signal, no external load		165	220	mW
t_r	Rise time	6	Single-ended, V_{in} = 5 mV		10	15	ns
t_f	Fall time	6	Single-ended, V_{in} = 5 mV		10	15	ns

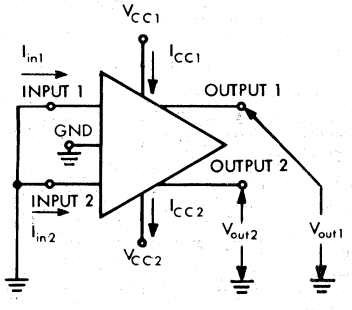
letter symbol and parameter definitions

V_{DO}	The d-c differential voltage that exists between the output terminals when the input terminals are at ground.
$V_{CMO(av)}$	The average of the d-c output voltages with respect to ground when the input terminals are grounded.
I_{DI}	The difference in the currents into the two input terminals.
V_{OM}	The maximum peak-to-peak output voltage swing that can be obtained without clipping.
V_{CMIM}	The maximum common-mode voltage that can be impressed on the input terminals while maintaining differential operation.
CMRR	The ratio of the differential-mode voltage gain to the common-mode voltage gain.
BW	The range of frequencies within which the open-loop voltage gain is within 3 dB of the mid-frequency value.

3

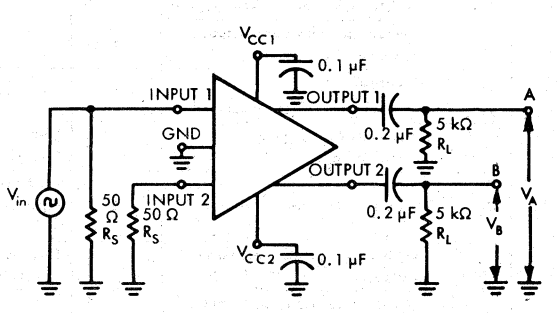
PARAMETER MEASUREMENT INFORMATION

test circuits



1. $V_{DO} = |V_{out1} - V_{out2}|$
2. $V_{CMO(av)} = \dfrac{V_{out1} + V_{out2}}{2}$
3. $I_{DI} = |I_{in1} - I_{in2}|$
4. $P_T = |V_{CC1} \bullet I_{CC1}| + |V_{CC2} \bullet I_{CC2}|$

FIGURE 1



1. Single-ended output distortion is measured at A or B with V_A or V_B = 1 V rms, input distortion < 0.2%, and f = 10 kHz.
2. $A_{VS} = \left|\dfrac{V_A \text{ or } V_B}{V_{in}}\right|$
   where: V_{in} = 1 mV rms and f = 100 kHz.
3. $V_{OM} = V_A$ or V_B

FIGURE 2

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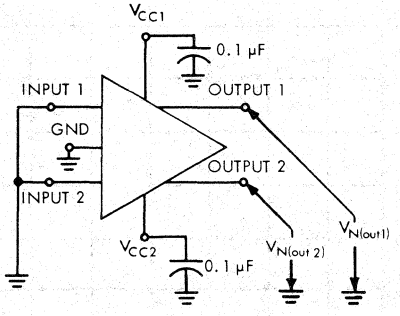
PARAMETER MEASUREMENT INFORMATION

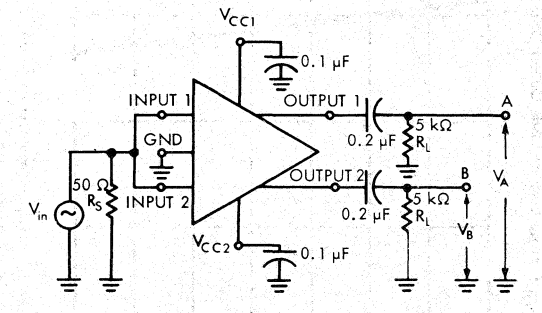
test circuits (continued)



1. $V_{\overline{N(in)}} = \dfrac{V_{\overline{N(out1)}} \text{ or } V_{\overline{N(out2)}}}{A_{VS}}$

where: $V_{\overline{N(out)}}$ = true rms broad-band noise voltage from 10 Hz to 500 kHz.

FIGURE 3



1. $A_{vcm} = 20 \text{ Log} \left| \dfrac{V_A \text{ or } V_B}{V_{in}} \right|$

where: V_{in} = 0.3 V rms and f = 100 kHz.

2. CMRR = 20 Log $A_{VS} - A_{vcm}$

FIGURE 4

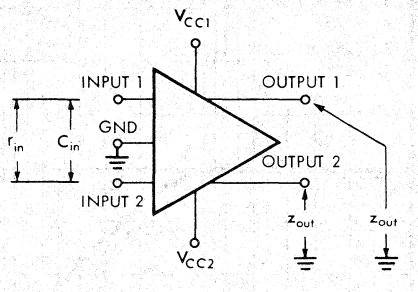
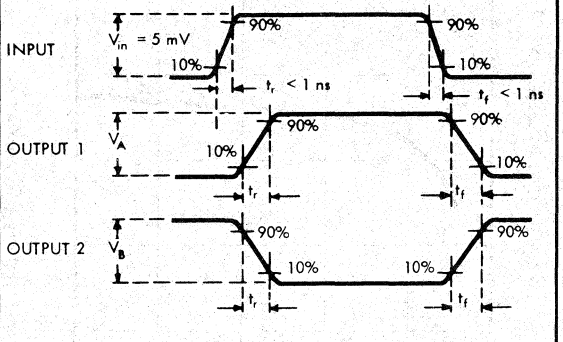


FIGURE 5



1. Test circuit is identical to that shown in Figure 2.

FIGURE 6 — t_r and t_f VOLTAGE WAVEFORMS

TYPICAL CHARACTERISTICS†

AVERAGE COMMON-MODE OUTPUT OFFSET VOLTAGE
vs
FREE-AIR TEMPERATURE

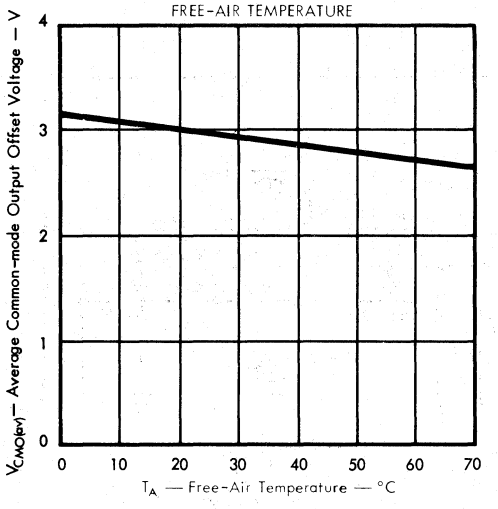


FIGURE 7

INPUT CURRENT
vs
FREE-AIR TEMPERATURE

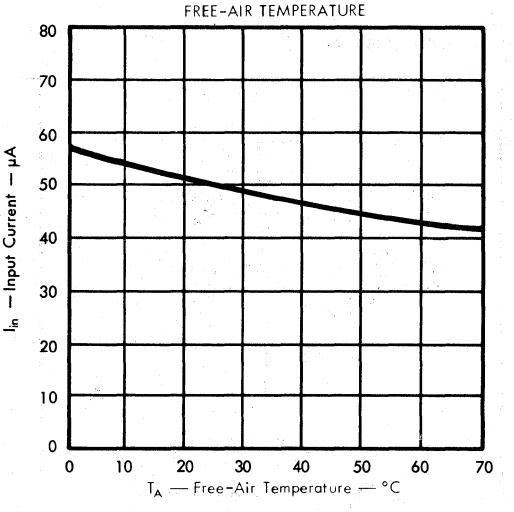


FIGURE 8

PEAK-TO-PEAK OUTPUT VOLTAGE
vs
LOAD RESISTANCE

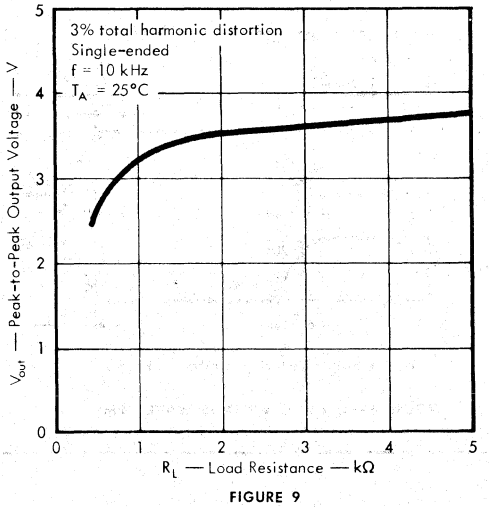


FIGURE 9

PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

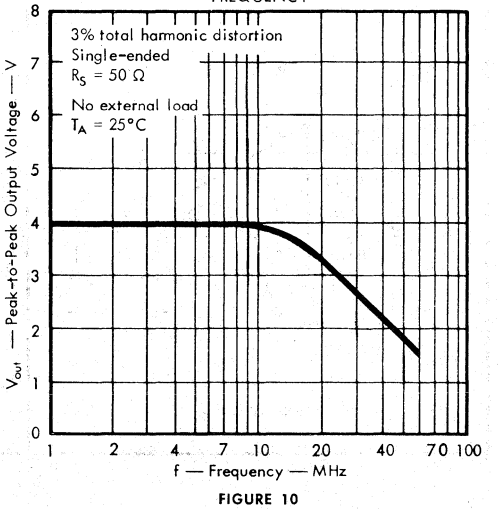


FIGURE 10

† Unless otherwise noted V_{CC1} = +6 V, V_{CC2} = −6 V.

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TYPICAL CHARACTERISTICS†

SMALL-SIGNAL VOLTAGE GAIN
vs
FREE-AIR TEMPERATURE

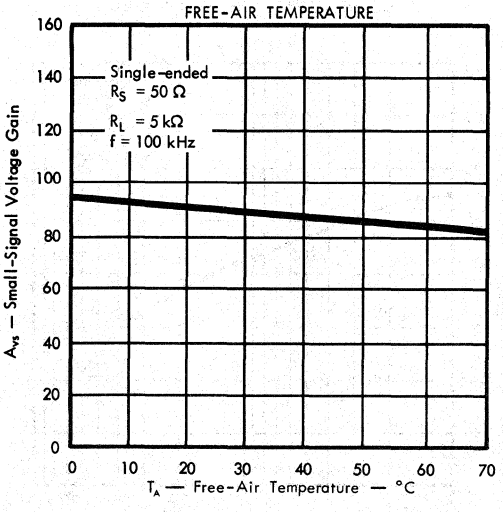


FIGURE 11

SMALL-SIGNAL VOLTAGE GAIN VARIATION
vs
SUPPLY VOLTAGE

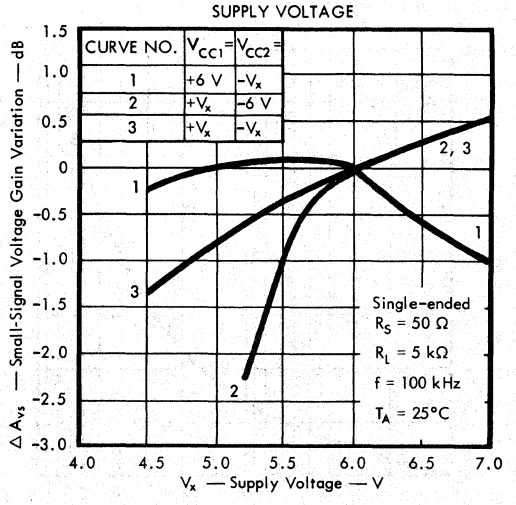


FIGURE 12

SMALL-SIGNAL VOLTAGE GAIN
vs
FREQUENCY

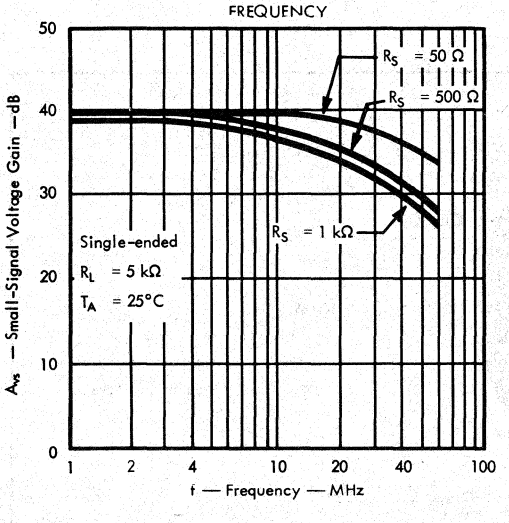


FIGURE 13

SMALL-SIGNAL VOLTAGE GAIN
vs
FREQUENCY

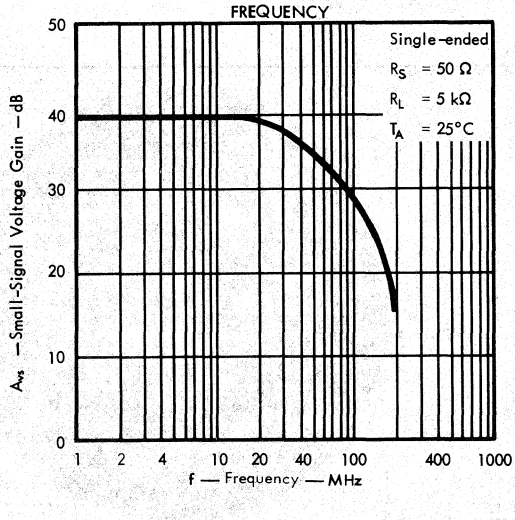


FIGURE 14

† Unless otherwise noted $V_{CC1} = +6$ V, $V_{CC2} = -6$ V.

TYPICAL CHARACTERISTICS†

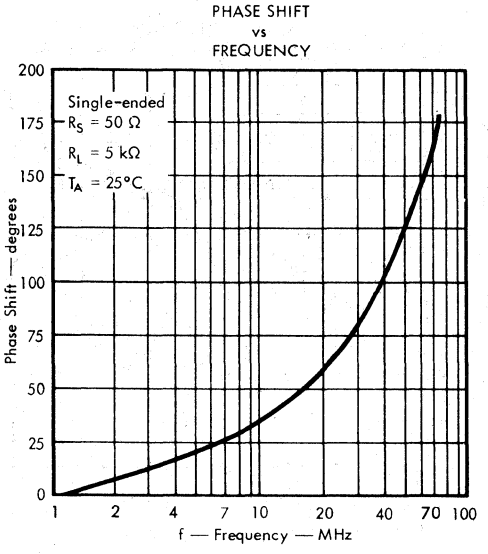


FIGURE 15

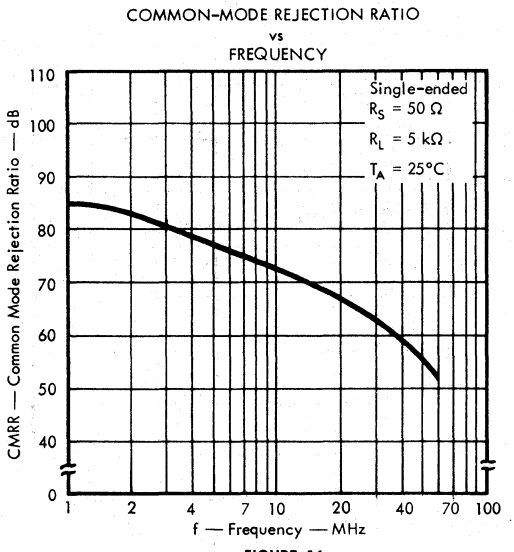
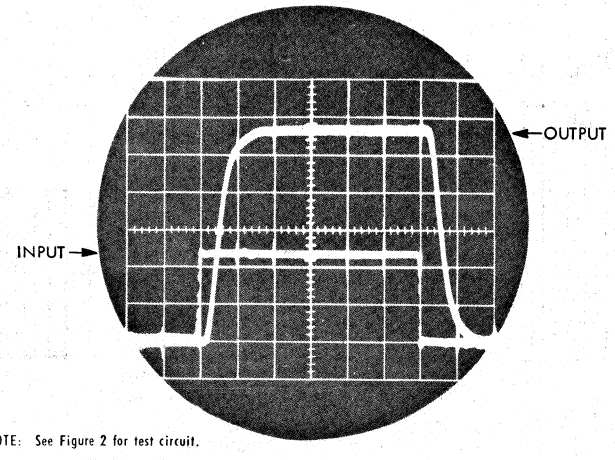


FIGURE 16

† $V_{CC1} = +6$ V and $V_{CC2} = -6$ V.



NOTE: See Figure 2 for test circuit.

FIGURE 17 — OSCILLOSCOPE PRESENTATION OF PULSE RESPONSE

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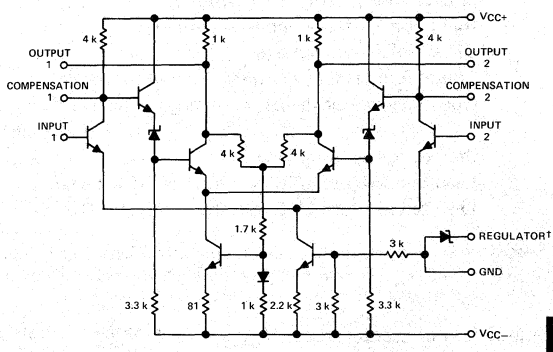
CIRCUIT TYPES SN5511, SN7511
DIFFERENTIAL VIDEO AMPLIFIERS

- Low Common-Mode Offset Voltage
- High Common-Mode Rejection Ratio
- High Gain-Bandwidth Product

schematic



Resistor values are nominal in ohms.

†Regulator terminal is used only with single supply. See description.

description

The SN5511 and SN7511 are wide-band amplifiers with differential inputs and outputs. High gain and low offset voltage permit use in applications requiring feedback. Frequency characteristics are such that a stable closed-loop configuration with 30-dB gain results in a 30-MHz bandwidth.

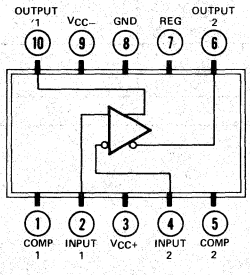
Accessibility to first-stage collectors makes offset balancing and frequency compensation possible with minimal effect on input and frequency characteristics.

The base of the first-stage current-source transistor is made available to permit operation from either a single 12-volt power supply or two 6-volt power supplies. For the latter, leave the regulator terminal open and connect the positive terminal of one supply to V_{CC+}, the negative terminal of the other supply to V_{CC-}, and the remaining terminals of the two supplies to the device ground terminal. For operation from a single 12-volt supply, connect the positive terminal of the supply to both the V_{CC+} and regulator terminals and connect the negative terminal to V_{CC-}. In either case, the device ground terminal is the reference for single-ended input and output voltages.

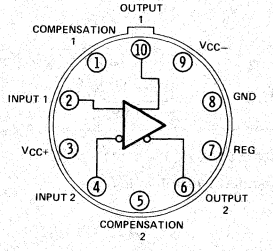
The wide bandwidth and high gain allow this amplifier to be used in a variety of applications where a stable differential video amplifier is required. Low common-mode offset voltage extends possible uses to comparators and direct-coupled amplifiers. The SN5511 is characterized for operation over the full military temperature range of –55°C to 125°C; the SN7511 is characterized for operation from 0°C to 70°C.

terminal assignments

F
FLAT PACKAGE (TOP VIEW)

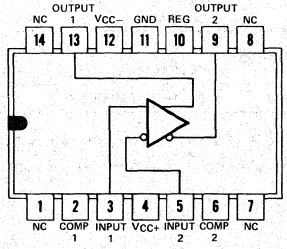


L
PLUG-IN PACKAGE (TOP VIEW)



ALL LEADS ARE ELECTRICALLY INSULATED FROM THE CASE

N
DUAL-IN-LINE PACKAGE (TOP VIEW)



NC – No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1) . . . . . 8 V
Supply voltage V_{CC-} (see Note 1) . . . . . −8 V
Input voltage, either input to ground . . . . . ±6 V
Differential input voltage . . . . . ±6 V
Continuous total power dissipation at (or below) 55°C free-air temperature (see Note 2) . . . . . 500 mW
Operating free-air temperature range: SN5511 Circuits . . . . . −55°C to 125°C
SN7511 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds, F and L packages . . . . . 300°C
Lead temperature 1/16 inch from case for 10 seconds, N package . . . . . 260°C

NOTES: 1. All voltage values, unless otherwise specified, are with respect to the network ground terminal.
2. For operation above 55°C free-air temperature, refer to Dissipation Derating Curve, Figure 1.

3

electrical characteristics, V_{CC+} = 6 V, V_{CC-} = −6 V, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST FIGURE	TEST CONDITIONS†	SN5511 MIN	SN5511 TYP	SN5511 MAX	SN7511 MIN	SN7511 TYP	SN7511 MAX	UNIT
A_{VD}	Large-signal differential voltage amplification		1	f ≤ 1 kHz, No load		3000					
				f ≤ 1 kHz, R_L = 5 kΩ		1200			600		
A_{VS}	Large-signal single-ended voltage amplification		2	f ≤ 1 kHz, R_L = 5 kΩ	400	600		250	300		
BW	Bandwidth	−3 dB		R_S = 500 Ω, No load		3			3		MHz
		Unity gain				100			100		
V_{IO}	Input offset voltage					1	5		1	5	mV
α_{VIO}	Average temperature coefficient of input offset voltage			T_A = −55°C to 25°C		4					μV/°C
				T_A = 25°C to 125°C		2					
				T_A = 0°C to 25°C					4		
				T_A = 25°C to 70°C					2		
I_{IO}	Input offset current					0.6	7		0.6	10	μA
I_{IB}	Input bias current					10	15		15	20	μA
V_I	Input voltage range		3		+2.5 −2			±1			V
V_{OO}	Output offset voltage			No load		0.35			0.35		V
				R_L = 500 Ω		0.17			0.17		
V_{OPP}	Maximum peak-to-peak output voltage swing		2	f ≤ 1 kHz, R_L = 5 kΩ	2.5	5		1.5	3		V
				f ≤ 1 kHz, R_L = 500 Ω		3			2		
z_{id}	Differential input impedance			f = 1 kHz		5			5		kΩ
z_{os}	Single-ended output impedance			f = 1 kHz		800			800		Ω
CMRR	Common-mode rejection ratio		3	f ≤ 100 kHz, No load, See Note 3	59	95		52	90		dB
P_D	Total power dissipation			No load, No signal		180			180		mW

NOTE 3: For SN5511, V_{IC} = +2.5 V to −2 V; for SN7511, V_{IC} = + 1 V to −1 V.

†Unless otherwise specified, V_{IO} is applied and the regulator terminal is open.

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DEFINITION OF TERMS

Large-Signal Differential Voltage Amplification (A_{VD}) The ratio of the change in voltage between the output terminals to the change in voltage between the input terminals producing it.

Large-Signal Single-Ended Voltage Amplification (A_{VS}) The ratio of the change in single-ended output voltage to the change in single-ended input voltage.

Input Offset Voltage (V_{IO}) The d-c voltage which must be applied between the input terminals to force the quiescent d-c differential output voltage to zero.

Average Temperature Coefficient of Input Offset Voltage (α_{VIO}) The ratio of the change in input offset voltage to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{VIO} = \left| \frac{(V_{IO} @ T_{A(1)}) - (V_{IO} @ T_{A(2)})}{T_{A(1)} - T_{A(2)}} \right|$$ where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

Input Offset Current (I_{IO}) The difference between the currents into the two input terminals with the inputs grounded.

Input Bias Current (I_{IB}) The average of the currents into the two input terminals with the inputs grounded.

Input Voltage Range (V_I) The range of voltage which if exceeded at either input terminal will cause the amplifier to cease functioning properly.

3

Output Offset Voltage (V_{OO}) The difference between the d-c voltages at the two output terminals when the input terminals are grounded.

Maximum Peak-to-Peak Output Voltage Swing (V_{OPP}) The maximum peak-to-peak output voltage swing that can be obtained without clipping. This includes the unbalance caused by output offset voltage.

Differential Input Impedance (z_{id}) The small-signal impedance between the two input terminals.

Single-Ended Output Impedance (z_{os}) The small-signal impedance between one output terminal and ground.

Common-Mode Rejection Ratio (CMRR) The ratio of differential voltage amplification to common-mode voltage amplification. This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in output offset voltage referred to the input.

Total Power Dissipation (P_D) The total d-c power supplied to the device less any power delivered from the device to a load. At no load; $P_D = V_{CC+} \cdot I_{CC+} + V_{CC-} \cdot I_{CC-}$.

THERMAL INFORMATION

DISSIPATION DERATING CURVE

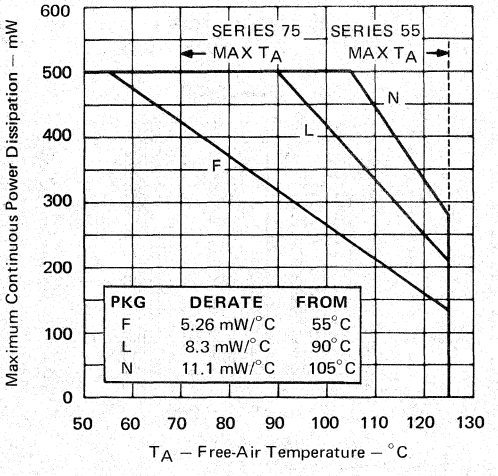


FIGURE 1

PARAMETER MEASUREMENT INFORMATION

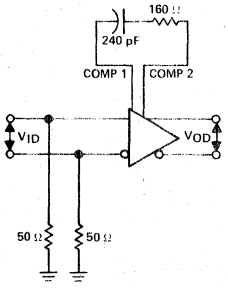


FIGURE 2 – A_{VD}

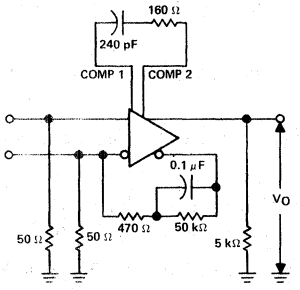


FIGURE 3 – A_{VS}, V_{OPP}

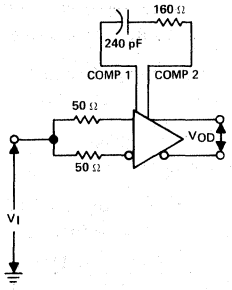


FIGURE 4 – V_I, CMRR

TYPICAL CHARACTERISTICS

3

SN5511
SINGLE-ENDED OPEN-LOOP VOLTAGE AMPLIFICATION
vs
FREQUENCY

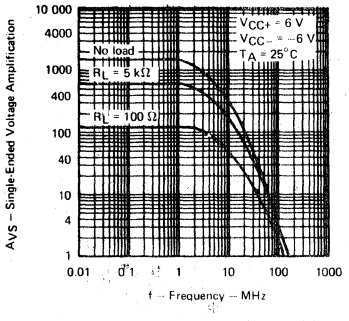


FIGURE 5

SN5511
SINGLE-ENDED OPEN-LOOP VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

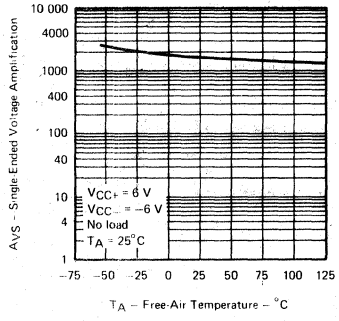


FIGURE 6

SN5511
SINGLE-ENDED OPEN-LOOP VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGES

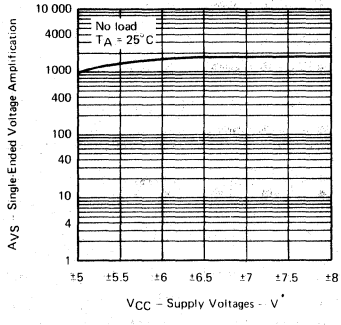


FIGURE 7

SN5511
INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

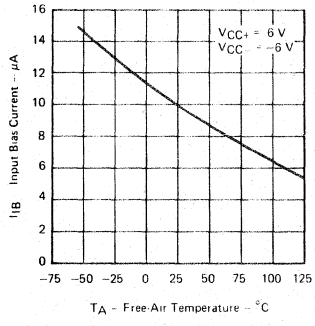


FIGURE 8

SN5511
MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE (OPEN-LOOP)
vs
LOAD RESISTANCE

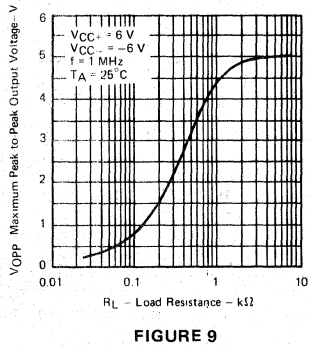


FIGURE 9

SN5511
MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE (OPEN-LOOP)
vs
FREQUENCY

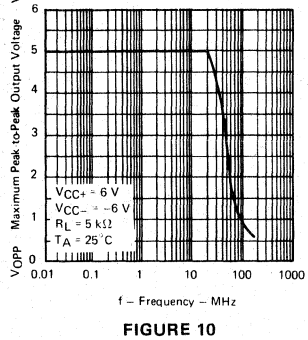


FIGURE 10

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPICAL CHARACTERISTICS

SN5511
SINGLE-ENDED CLOSED-LOOP
VOLTAGE AMPLIFICATION
vs
FREQUENCY

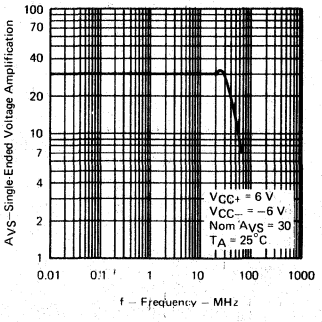
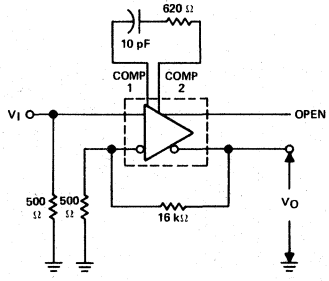


FIGURE 11

NOMINAL AMPLIFICATION OF 30



TEST CIRCUIT
FOR FIGURES 11 AND 12

SN5511
MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE (CLOSED-LOOP)
vs
FREQUENCY

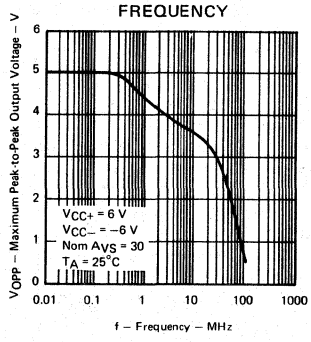


FIGURE 12

3

SN5511
SINGLE-ENDED CLOSED-LOOP
VOLTAGE AMPLIFICATION
vs
FREQUENCY

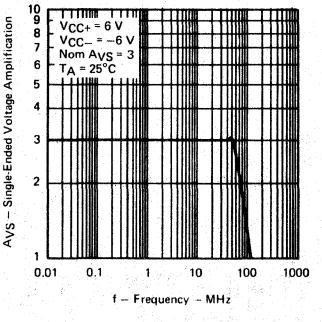
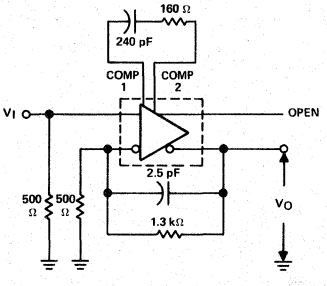


FIGURE 13

NOMINAL AMPLIFICATION OF 3



TEST CIRCUIT
FOR FIGURES 13 AND 14

SN5511
MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE (CLOSED-LOOP)
VS
FREQUENCY

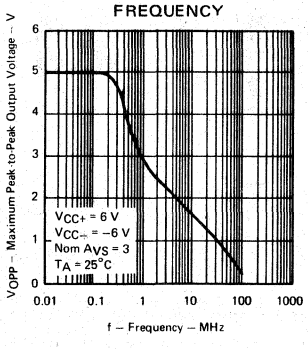


FIGURE 14

SN5511
SINGLE-ENDED CLOSED-LOOP
VOLTAGE AMPLIFICATION
vs
FREQUENCY

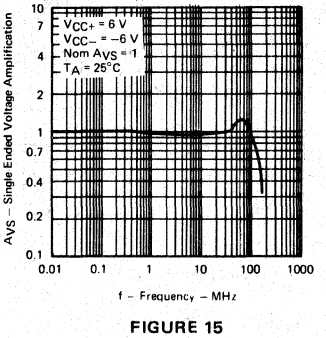
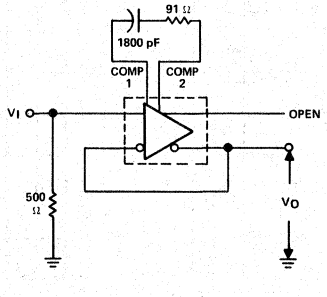


FIGURE 15

NOMINAL AMPLIFICATION OF 1



TEST CIRCUIT
FOR FIGURES 15 AND 16

SN5511
MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE (CLOSED-LOOP)
vs
FREQUENCY

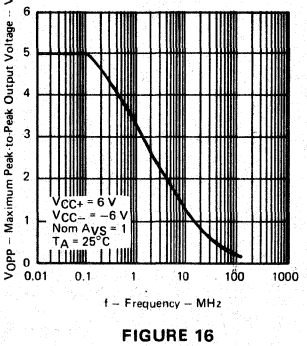


FIGURE 16

TYPICAL CHARACTERISTICS

INPUT IMPEDANCE
vs
FREE-AIR TEMPERATURE

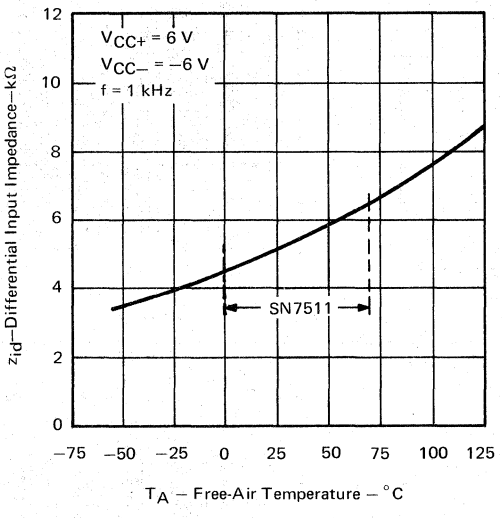


FIGURE 17

SN5511

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

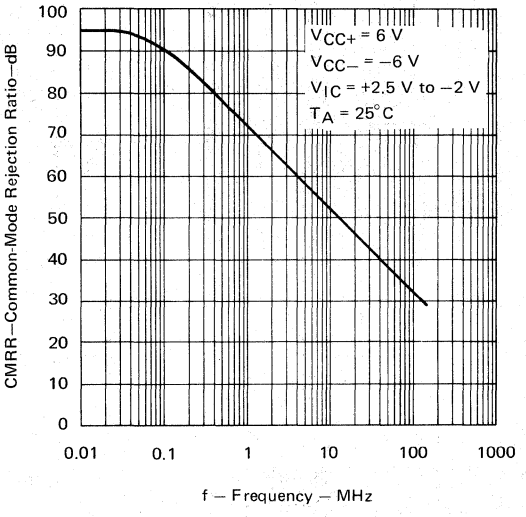


FIGURE 18

TOTAL POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

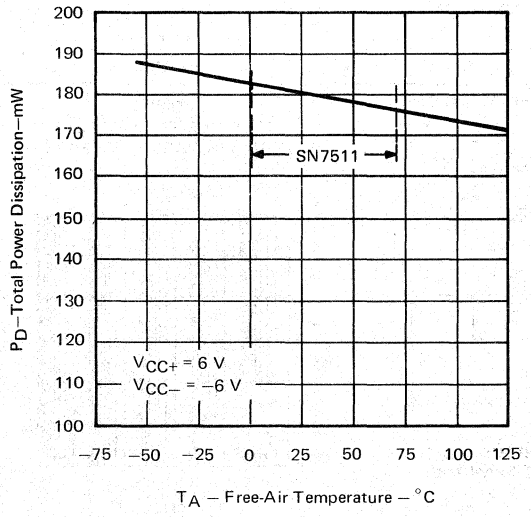


FIGURE 19

SPOT NOISE FIGURE
vs
FREQUENCY

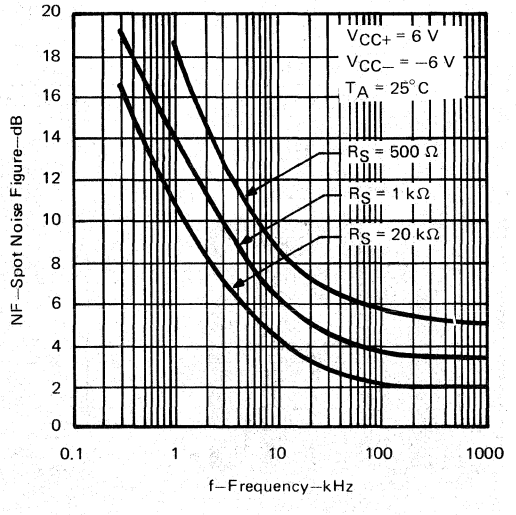


FIGURE 20

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN5512, SN5514, SN7512, SN7514 DIFFERENTIAL VIDEO AMPLIFIERS

- 80-MHz Bandwidth
- No Frequency Compensation Required
- Typical Differential Voltage Amplification of 300
- SN5512 and SN7512 Have Offset-Voltage Null Capability

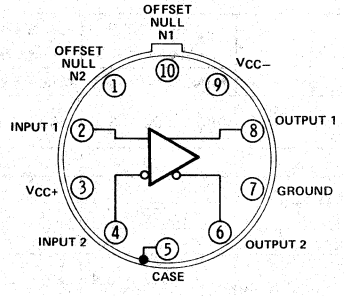
description

Each of these wide-band video amplifiers feature a flat frequency response and low phase distortion from dc to typically 80 MHz. Emitter-follower outputs enable the devices to drive capacitive loads. A low-value potentiometer may be connected between the offset null inputs of the SN5512 and SN7512, as shown in Figure 7, to null out the offset voltage.

These circuits are designed for use as sense amplifiers in high-speed thin-film or plated-wire memories, as magnetic tape-read amplifiers, or as general purpose pulse or video amplifiers.

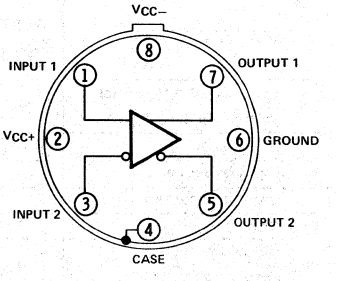
terminal assignments

SN5512, SN7512
L PLUG-IN PACKAGE
(TOP VIEW)



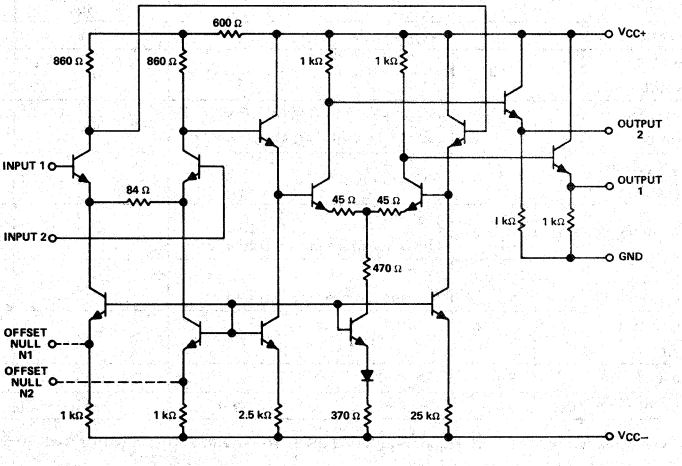
THE CIRCUIT IS ELECTRICALLY INSULATED FROM THE CASE

SN5514, SN7514
L PLUG-IN PACKAGE
(TOP VIEW)



THE CIRCUIT IS ELECTRICALLY INSULATED FROM THE CASE

schematic



NOTES: 1. Component values shown are nominal.
2. Offset null terminals (shown with dashed lines) are provided on the SN5512 and SN7512 only.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	SN5512 SN5514	SN7512 SN7514	UNIT
Supply voltage V_{CC+} (See Note 3)	8	8	V
Supply voltage V_{CC-} (See Note 3)	−8	−8	V
Differential input voltage	±5	±5	V
Common-mode input voltage	±6	±6	V
Voltage between either offset null terminal (N1/N2) and V_{CC-} (SN5512 and SN7512)	±0.5	±0.5	V
Output current	10	10	mA
Continuous total power dissipation at (or below) 65°C free-air temperature (See Note 4)	500	500	mW
Operating free-air temperature range	−55 to 125	0 to 70	°C
Storage temperature range	−65 to 150	−65 to 150	°C
Lead temperature 1/16" from case for 60 seconds	300	300	°C

NOTES: 3. All voltage values, except differential input voltages, are with respect to the network ground terminal.
4. For operation above 65°C free-air temperature, refer to Dissipation Derating Curve, Figure 6.

3

electrical characteristics, T_A = 25°C, V_{CC+} = 6 V, V_{CC-} = −6 V

PARAMETER		TEST FIGURE	TEST CONDITIONS	SN5512 SN5514			SN7512 SN7514			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
A_{VD}	Large-signal differential voltage amplification	1	V_{OD} = 1 V	250	300	350	200	300	400	
BW	Bandwidth	2	R_S = 50 Ω		80			80		MHz
I_{IO}	Input offset current				1	3		1	5	μA
I_{IB}	Input bias current				50	80		50	80	μA
V_I	Input voltage range	1		±1			±1			V
V_{OC}	Common-mode output voltage	1		2.4	2.7	3.4	2.4	2.7	3.4	V
V_{OO}	Output offset voltage	1			0.5	1.3		0.5	1.3	V
V_{OPP}	Maximum peak-to-peak output voltage swing	3		3	5		3	5		V
r_i	Input resistance	3	$V_{OD} \leq 1$ V		6			6		kΩ
r_o	Output resistance				35			35		Ω
C_i	Input capacitance	3	$V_{OD} \leq 1$ V		7			7		pF
CMRR	Common-mode rejection ratio	4	V_{IC} = ± 1 V, f ≤ 100 kHz		84			84		dB
$\Delta V_{CC}/\Delta V_{IO}$	Supply voltage rejection ratio	1	ΔV_{CC+} = from 6 V to 5.5 V ΔV_{CC-} = from −6 V to −5.5 V	50	80		50	80		dB
V_n	Broadband equivalent input noise voltage	5	See Note 5		3			3		μV
t_{pd}	Propagation delay time	2	R_S = 50 Ω, Output voltage step = 0 to 1 V		6			6		ns
t_r	Rise time	2	R_S = 50 Ω, Output voltage step = 0 to 1 V		5			5		ns
$I_{sink(max)}$	Maximum output sink current			2.5	3.2		2.5	3.2		mA
I_{CC+}	Supply current from V_{CC+}		No load, No signal		19	25		19	25	mA
I_{CC-}	Supply current from V_{CC-}		No load, No signal		−13	−20		−13	−20	mA

NOTE 5: This parameter is measured in a system with response down 3 dB at 10 Hz and 500 kHz with a 6-dB/octave rolloff.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

DEFINITION OF TERMS

Large-Signal Differential Voltage Amplification (A_{VD}) The ratio of the change in voltage between the output terminals to the change in voltage between the input terminals producing it.

Bandwidth (BW) The range of frequencies within which the differential gain of the amplifier is not more than 3 dB below its low-frequency value.

Input Offset Current (I_{IO}) The difference between the currents into the two input terminals with the inputs grounded.

Input Bias Current (I_{IB}) The average of the currents into the two input terminals with the inputs grounded.

Input Voltage Range (V_I) The range of voltage which if exceeded at either input terminal will cause the amplifier to cease functioning properly.

Common-Mode Output Voltage (V_{OC}) The average of the d-c voltages at the two output terminals.

Output Offset Voltage (V_{OO}) The difference between the d-c voltages at the two output terminals when the input terminals are grounded.

Maximum Peak-to-Peak Output Voltage Swing (V_{OPP}) The maximum peak-to-peak output voltage swing that can be obtained without clipping. This includes the unbalance caused by output offset voltage.

Input Resistance (r_i) The resistance between the input terminals with either input grounded.

Output Resistance (r_o) The resistance between either output terminal and ground.

Input Capacitance (C_i) The capacitance between the input terminals with either input grounded.

Common-Mode Rejection Ratio (CMRR) The ratio of differential voltage amplification to common-mode voltage amplification. This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in output offset voltage referred to the input.

Supply Voltage Rejection Ratio ($\Delta V_{CC}/\Delta V_{IO}$) The ratio of the change in power supply voltages to the change in output offset voltage referred to the input. For these devices, both supply voltages are varied symmetrically.

Propagation Delay Time (t_{pd}) The interval between the application of an input voltage step and its arrival at either output, measured at 50% of the final value.

Rise Time (t_r) The time required for an output voltage step to change from 10% to 90% of its final value.

Maximum Output Sink Current ($I_{sink(max)}$) The maximum available current into either output terminal when that output is at its most negative potential.

PARAMETER MEASUREMENT INFORMATION

test circuits

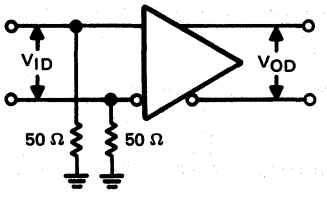


FIGURE 1

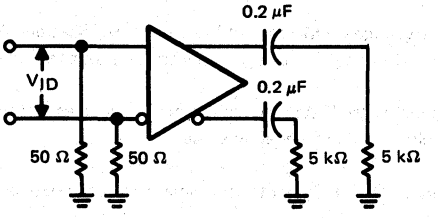


FIGURE 2

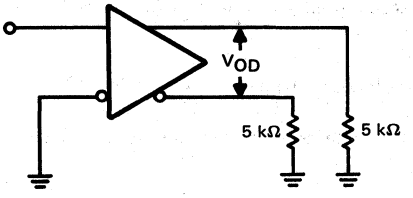


FIGURE 3

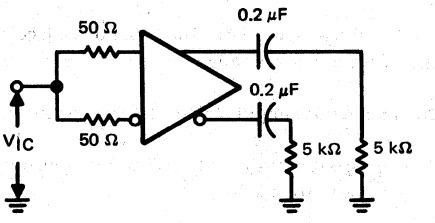


FIGURE 4

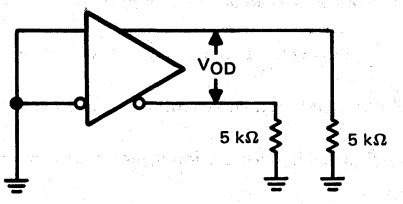


FIGURE 5

THERMAL INFORMATION

DISSIPATION DERATING CURVE

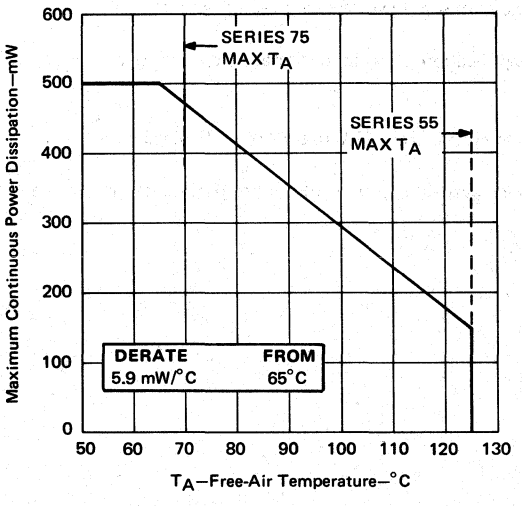


FIGURE 6

TYPICAL APPLICATION DATA

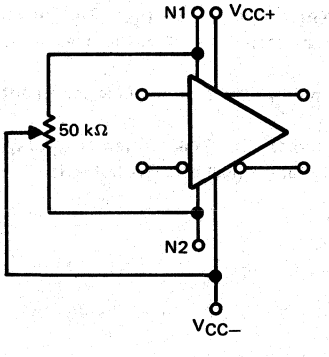


FIGURE 7–SN5512/SN7512
INPUT-OFFSET-VOLTAGE NULL CIRCUIT

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

line drivers

TYPE	SN55109, SN75109	SN55110, SN75110	SN75113*	SN75114*	SN75150†	SN75450A
• Operating Frequency	> 10 MHz	> 10 MHz	> 10 MHz	> 10 MHz	10 kHz at 2500-pF Load	< 1 MHz
• Type of Lines	Balanced or Single-Ended	Balanced or Single-Ended	Balanced or Single-Ended	Balanced or Single-Ended	Single-Ended	Balanced or Single-Ended
• Length of Line	Up to 5,000′	Up to 10,000′	Up to 1,000′	Up to 1,000′	Up to 500′	Up to 500′
• Input	TTL	TTL	TTL	TTL	TTL	TTL
• Output	Current Mode	Current Mode	Voltage Mode	Voltage Mode	Voltage Mode	Current Mode
• Party Line Operation	Yes	Yes	Yes	Yes	No	Yes
• Strobe Control	Yes	Yes	Yes	No	No	
• Power Supply	+5 V and −5 V	+5 V and −5 V	+5 V	+5 V	+12 V and −12 V	+5 V
Packages	J, N	J, N	J, N	J, N	J, N, P	N
Application Notes	CA130: Line Drivers and Receivers CA146: Data Transmission					CA150-Peripheral Interface Circuits

line receivers

TYPE	SN55107A, SN75107A	SN55108A, SN75108A	SN55115,* SN75115*	SN75154*
• Input Sensitivity, Max	25 mV	25 mV	0.5 V	
• Switching Time, Max	25 ns	25 ns	50 ns	50 ns
• Strobe Capability	Yes	Yes	Yes	No
• Output	TTL, Active Pull-Up	TTL, Open-Collector	TTL, Open-Collector With Active Pull-Up Option	TTL, Active Pull-Up
• Fan-Out to Series 54	10	10	10	10
• Power Supply	+5 V and −5 V	+5 V and −5 V	+5 V	+5 V or +12 V
Packages	J, N	J, N	J, N	J, N
Application Notes	CA130: Line Drivers and Receivers CA146: Data Transmission			

*To be announced soon

†Satisfies requirements of EIA standard RS-232-C

TYPE SN75100L
DUAL DIFFERENTIAL LINE RECEIVER

SERIES 75 LINE RECEIVER

featuring

- **High Input Impedance**
- **Fast Switching Speed**
- **Good Small-Signal Sensitivity**
- **TTL and DTL Compatible Outputs**
- **Wire-OR Output Capability**

description

The SN75100L is a monolithic, dual line receiver which consists of two independent discriminator/buffer circuits in a single package. Each line receiver is composed of a voltage-sensitive, differential-input comparator which drives an open-collector, saturated-logic buffer. This device is designed to operate throughout the temperature range of 0°C to 70°C with a maximum switching time of 40 nanoseconds. The buffer output is at a logical 1 voltage level when the voltage at the signal input is at least 100 millivolts more positive than the reference voltage applied at V_{ref}. The output is at a logical 0 level when the voltage at the signal input is at least 100 millivolts more negative than the reference voltage applied at V_{ref}.

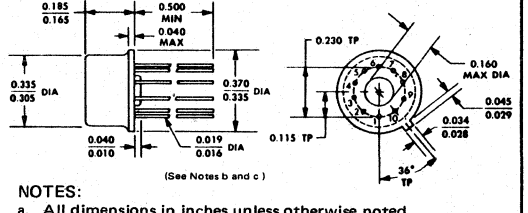
The line receiver has a common-mode input voltage range of -1.5 volts to 1.5 volts which means that both inputs can withstand common voltages of as much as 1.5 volts above or below ground. The buffer output will produce the correct logic-level output for a minimum difference in voltage of 100 millivolts between the differential inputs.

For normal single-ended operation, the data transmission line is connected to the signal input with a fixed d-c voltage between -1.5 volts and 1.5 volts applied at V_{ref}. For maximum noise immunity, the d-c voltage level at V_{ref} should be set midway between the logical 0 and logical 1 voltage levels of the input signal. Alternatively, the functions of the signal and reference-voltage inputs may be interchanged.

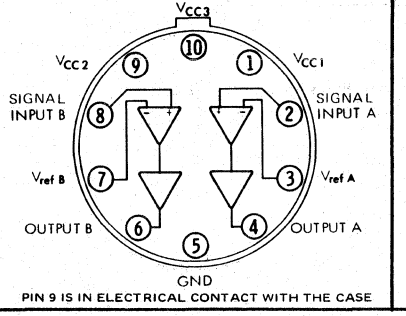
When the line receiver is used in a differential mode with balanced two-wire lines, one wire is connected to the signal input and the other wire is connected to V_{ref}. Since a maximum difference of 100 millivolts between the signal input and V_{ref} will assure a given logical level at the buffer output, a trade-off between input sensitivity and common-mode rejection can be made by using external voltage dividers at the inputs.

mechanical data

The SN75100L package outline is the same as JEDEC TO-100 except for diameter of standoff. Gold-plated leads (-00) require no additional cleaning or processing for use in soldered assembly. Solder-dipped leads (-10) are also available.



NOTES:
a. All dimensions in inches unless otherwise noted.
b. This dimension not applicable for solder-dipped leads.
c. When solder-dipped leads are specified, dipped area of lead extends from lead tip to within 0.050 of lower extremity of metallic case.



PIN 9 IS IN ELECTRICAL CONTACT WITH THE CASE

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltages (See Note 1): V_{CC1} . . . . . 10 V
V_{CC2} . . . . . -10 V
V_{CC3} . . . . . 6 V
Differential input voltage, V_{inD} (See Note 2) . . . . . ± 5 V
Input voltage, V_{in} or V_{ref} (See Note 1) . . . . . ± 5.5 V
Maximum current into the output, I_{sink} . . . . . 60 mA
Continuous power dissipation at (or below) 25°C free-air temperature (See Note 3) . . . . . 680 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . -65°C to 150°C

recommended operating conditions

Supply voltages (See Note 1): V_{CC1} . . . . . 8 V ± 10%
V_{CC2} . . . . . -8 V ± 10%
V_{CC3} . . . . . 4 V ± 10%
Reference voltage, V_{ref} . . . . . -1.5 V to 1.5 V

3

NOTES: 1. These voltage values are with respect to network ground terminal.
2. These voltage values are with respect to the other differential-input terminal.
3. Derate linearly to 435 mW at 70°C free-air temperature at the rate of 5.4 mW/°C.

electrical characteristics (unless otherwise noted, V_{CC1} = 8 V, V_{CC2} = -8 V, V_{CC3} = 4 V, T_A = 0°C to 70°C)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{inD(0)}$	Logical 0 input voltage at the signal input, with respect to V_{ref}, required to ensure logical 0 level at the output	1	V_{ref} = -1.5 V to 1.5 V	-100			mV
$V_{inD(1)}$	Logical 1 input voltage at the signal input, with respect to V_{ref}, required to ensure logical 1 level at the output	1	V_{ref} = -1.5 V to 1.5 V	100			mV
$V_{out(0)}$	Logical 0 output voltage	2	V_{in} = -2 V to 1.4 V, V_{ref} = 1.5 V, I_{sink} = 40 mA		0.25	0.5	V
			V_{in} = -2 V to -1.6 V, V_{ref} = -1.5 V, I_{sink} = 40 mA		0.25	0.5	V
$I_{out(1)}$	Output reverse current	2	V_{in} = -1.4 V to 3.5 V, V_{ref} = -1.5 V, V_{out} = 5.5 V			250	μA
I_{in}	Input current into the signal input	3	V_{ref} = -1.5 V, See Note 4		20	50	μA
$I_{in(ref)}$	Input current into V_{ref}	3	V_{ref} = 1.5 V, See Note 4		20	50	μA
I_{CC1}	V_{CC1} supply current	4	V_{CC1} = 8.8 V		15	22	mA
I_{CC2}	V_{CC2} supply current	4	V_{CC2} = -8.8 V		-13	-17	mA
I_{CC3}	V_{CC3} supply current	4	V_{CC3} = 4.4 V		10	20	mA

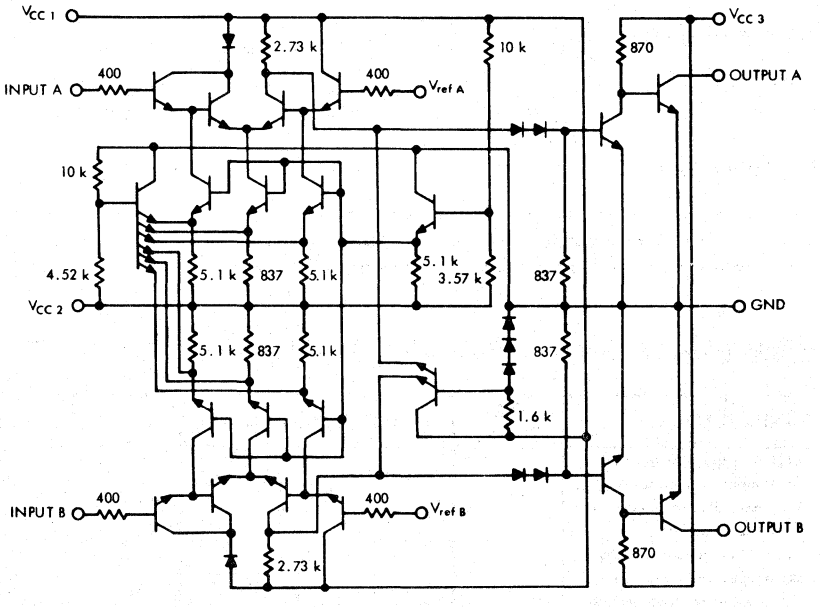
†All typical values are at 25°C.

NOTE: 4. The maximum value specified is also applicable under any combination of the following conditions:
a. V_{CC1} is open, grounded, or at 8 V ± 10%.
b. V_{CC2} is open, grounded, or at -8 V ± 10%.
c. V_{CC3} is open, grounded, or at 4 V.
d. V_{in} = 2 V to 4.4 V.

switching characteristics, V_{CC1} = 8 V, V_{CC2} = -8 V, V_{CC3} = 4 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{pd(1)}$	Propagation delay time to logical 1 level	5	R_L = 100 Ω, C_L = 20 pF, V_L = 4 V, f = 1 MHz		20	40	ns
$t_{pd(0)}$	Propagation delay time to logical 0 level	5			20	40	ns

schematic diagram



NOTE: All resistor values are in ohms.

PARAMETER MEASUREMENT INFORMATION †

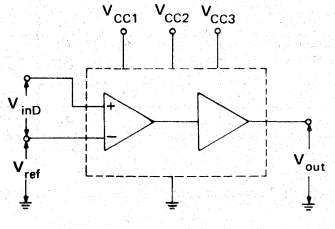


FIGURE 1– $V_{inD(0)}$ and $V_{inD(1)}$

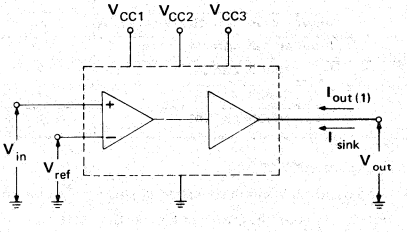


FIGURE 2– $V_{out(0)}$ and $I_{out(1)}$

†Arrows indicate direction of current flow.

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PARAMETER MEASUREMENT INFORMATION †

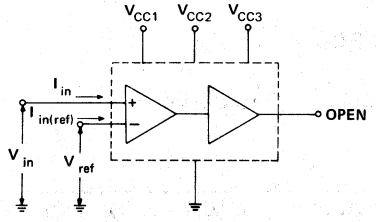


FIGURE 3–I_{in} and $I_{in(ref)}$

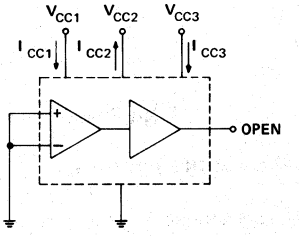
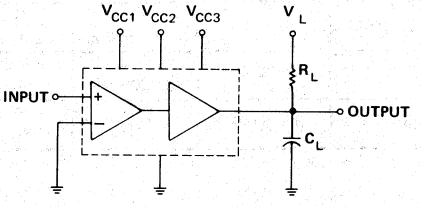
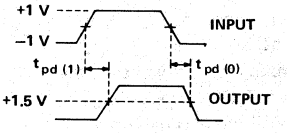


FIGURE 4–I_{CC1}, I_{CC2}, and I_{CC3}



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 5–$t_{pd(1)}$ and $t_{pd(0)}$

†Arrows indicate direction of current flow.

TYPICAL APPLICATION DATA

The SN75100L is ideally suited for use as a differential or single-ended line receiver. Maximum flexibility is ensured by the high-impedance inputs and open-collector outputs. The outputs are compatible for driving TTL or DTL digital circuits and may be combined to perform the wire-OR function.

When used in a single-ended "party line" data-transmission system, transmission lines may be either a twisted pair or coaxial cable. See Figure A.

By terminating the transmission line at each end, a two-way signal path may be utilized. The SN75100L provides very little loading to the transmission line due to its high input impedance. Therefore, transmitter/receiver pairs may be tied into the line anywhere along its length without disturbing the impedance level of the line.

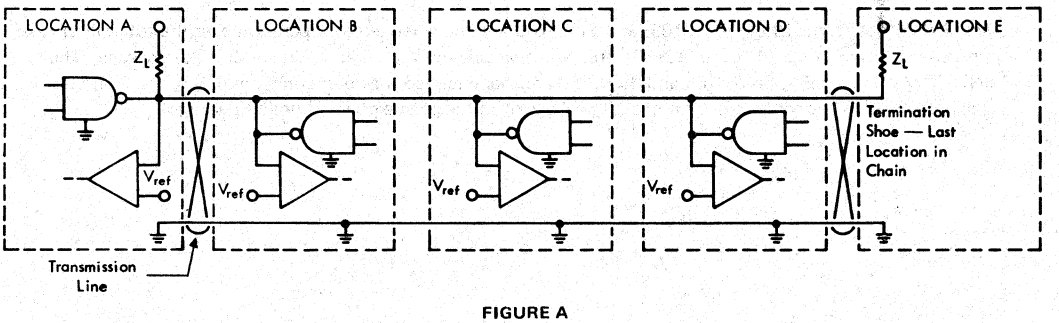


FIGURE A

CIRCUIT TYPES SN55107A, SN55108A, SN55109, SN55110, SN75107A, SN75108A, SN75109, SN75110 DUAL LINE RECEIVERS AND DRIVERS

SERIES 55/75107A LINE CIRCUITS
featuring

• High Speed • Standard Supply Voltages • Dual Channels

additional features of line receivers

- high common-mode rejection ratio
- high input impedance
- high input sensitivity
- differential input common-mode voltage range of ± 3 V
- differential input common-mode voltage range of more than ±15 V using external attenuator
- strobe inputs for receiver selection
- gate inputs for logic versatility
- TTL or DTL drive capability
- high d-c noise margins

–55°C to 125°C J Package	0°C to 70°C J or N Package	CIRCUIT FUNCTION	OUTPUT FUNCTION
SN55107A	SN75107A	Dual Line Receiver	Active Pull-Up
SN55108A	SN55108A	Dual Line Receiver	Open Collector
SN55109	SN75109	Dual Line Driver	6-mA Current Switch
SN55110	SN75110	Dual Line Driver	12-mA Current Switch

additional features of line drivers

- TTL input compatibility
- current-mode output (6 mA or 12 mA typical)
- high output impedance
- high common-mode output voltage range (–3 V to 10 V)
- inhibitor available for driver selection

description

The Series 55/75107 circuits are TTL/DTL compatible high-speed line receivers and drivers. Each is a monolithic dual circuit featuring two independent channels.

The SN55107A, SN55108A, SN75107A, and SN75108A line receivers are designed for general use as well as such specific applications as data comparators and balanced, unbalanced, and party-line transmission systems. These devices are unilaterally interchangeable with and replace SN55107, SN55108, SN75107, and SN75108, respectively, but offer diode-clamped inputs to simplify circuit design.

The SN55109, SN55110, SN75109, and SN75110 line drivers are designed to be used in many categories of applications in balanced, unbalanced, and party-line systems and as level converters.

The SN55107A, SN55108A, SN55109, and SN55110 are characterized for operation over the full military temperature range of –55°C to 125°C, and are available in the ceramic dual-in-line (J) package. The SN75107A, SN75108A, SN75109, and SN75110 are characterized for operation from 0°C to 70°C and are available either in the ceramic dual-in-line (J) package or in the plastic dual-in-line (N) package.

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design characteristics

Series 55/75107A Line Circuits are TTL-compatible dual circuits intended for use in high-speed data-transmission systems. The drivers are designed to drive balanced, terminated transmission lines, such as twisted-pair, at normal line impedances without high power dissipation. The receivers are designed to detect low-level differential signals in the presence of common-mode noise and variations of temperature and supplies. Either driver may be used with either receiver. Specifications reflect worst-case conditions of temperature, supply voltages, and input voltages.

line receivers - SN55/75107A, SN55/75108A

The SN55/75107A and SN55/75108A are dual line receivers featuring independent channels with common voltage supply and ground terminals. The SN55/75107A circuit features a TTL-compatible active pull-up (totem-pole) output. The SN55/75108A circuit is also TTL-compatible, but features an open-collector output configuration that permits the dot-OR logic connection with similar outputs (such as the SN54/74101 TTL gate or other SN55/75108A line receivers). This permits a level of logic to be implemented without extra delay. All other features of the line receivers are identical.

The SN55/75107A and SN55/75108A line circuits are designed to detect input signals of 25 millivolts (or greater) amplitude and convert the polarity of the signal into appropriate TTL-compatible output logic levels.

The SN55/75107A and SN55/75108A feature high input impedance and low input currents which induce very little loading on the transmission line. This makes these devices especially useful in party-line systems. The excellent input sensitivity (3 millivolts typical) is particularly important when data is to be detected at the end of a long transmission line and the amplitude of the data has been deteriorated due to cable losses.

The receiver input common-mode voltage range is ±3 volts. This is adequate for application in most systems. In systems with requirements for greater common-mode voltage range, input attenuators may be used to decrease the noise to an acceptable level at the receiver-input terminals.

The receivers feature individual strobe inputs for each channel and a strobe input common to both channels for logic versatility. The strobe inputs are tested to guarantee 400 millivolts of d-c noise margin when interfaced with Series 54/74 TTL.

line drivers - SN55/75109, SN55/75110

The SN55/75109 and SN55/75110 are dual line drivers featuring independent channels with common voltage supply and ground terminals. The significant difference between the two drivers is in the output-current specification. The driver circuits feature a constant output current that is switched to either of two output terminals by the appropriate logic levels at the input terminals. The output current can be switched off (inhibited) by appropriate logic levels on the inhibit inputs. The output current is nominally 6 milliamperes for the SN55/75109 and 12 milliamperes for the SN55/75110. System design determines which driver is best suited to a particular application.

The inhibit feature is provided so the circuits can be used in party-line or data-bus applications. A strobe or inhibitor, common to both drivers, is included for increased driver-logic versatility. The output current in the inhibited mode, $I_{O(off)}$, is specified so that minimum line loading is induced when the driver is used in a party-line system with other drivers. The output impedance of the driver in the inhibited mode is very high—the output impedance of a transistor biased to cutoff.

The driver outputs have a common-mode voltage range of −3 volts to +10 volts, allowing common-mode voltage on the line without affecting driver performance.

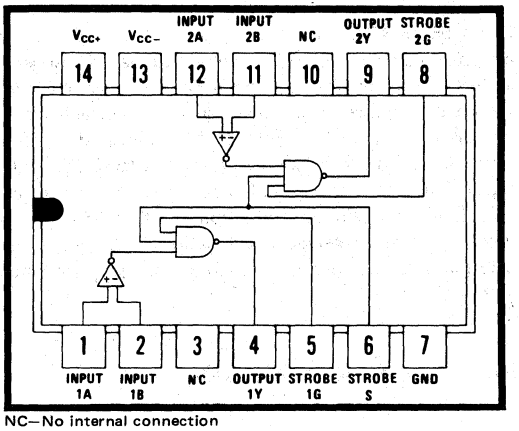
The logic and inhibit inputs of the drivers are designed to satisfy TTL-system requirements. The logic inputs are tested at 2.0 volts for high-logic-level conditions and 0.8 volt for low-logic-level conditions. These tests guarantee 400 millivolts of noise margin when interfaced with Series 54/74 TTL.

logic

TRUTH TABLE

DIFFERENTIAL INPUTS A-B	STROBES G	STROBES S	OUTPUT Y
$V_{ID} \geq 25$ mV	L or H	L or H	H
-25 mV $< V_{ID} < 25$ mV	L or H	L	H
	L	L or H	H
	H	H	INDETERMINATE
$V_{ID} \leq -25$ mV	L or H	L	H
	L	L or H	H
	H	H	L

SN55107A, SN55108A J DUAL-IN-LINE PACKAGE
SN75107A, SN75108A J OR N DUAL-IN-LINE PACKAGE



NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

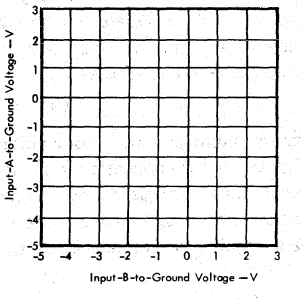
Supply voltage V_{CC+} (See Note 1) . . . . . 7 V
Supply voltage V_{CC-} (See Note 1) . . . . . −7 V
Differential input voltage (See Note 2) . . . . . ±6 V
Common-mode input voltage (See Note 1) . . . . . ±5 V
Strobe input voltage (See Note 1) . . . . . 5.5 V
Operating free-air temperature range, Series 55 . . . . . −55°C to 125°C
Series 75 . . . . . 0°C to 70°C
Storage temperature range, ceramic dual-in-line (J) package . . . . . −65°C to 150°C
plastic dual-in-line (N) package . . . . . −55°C to 150°C

recommended operating conditions (see note 3)

	SN55107A, SN55108A MIN	NOM	MAX	SN75107A, SN75108A MIN	NOM	MAX	UNIT
Supply voltage V_{CC+} (See Note 1)	4.5	5	5.5	4.75	5	5.25	V
Supply voltage V_{CC-} (See Note 1)	−4.5	−5	−5.5	−4.75	−5	−5.25	V
Output sink current			−16			−16	mA
Differential input voltage (See Notes 2 and 4)	−5†		5	−5†		5	V
Common-mode input voltage (See Notes 1 and 4)	−3†		3	−3†		3	V
Input voltage range, any differential input to ground (See Note 4)	−5†		3	−5†		3	V
Operating free-air temperature range	−55		125	0		70	°C

NOTES: 1. These voltage values are with respect to network ground terminal.
2. These voltage values are at the noninverting (+) terminal with respect to the inverting (−) terminal.
3. When using only one channel of the line receiver, the inputs of the other channel should be grounded.
4. The recommended combinations of input voltages fall within the shaded area of the figure at the right.

RECOMMENDED COMBINATIONS OF INPUT VOLTAGES FOR LINE RECEIVERS



†The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic voltage levels only.

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definition of input logic levels†

		TEST FIGURE	MIN	MAX	UNIT
V_{IDH}	High-level input voltage between differential inputs	1	0.025	5	V
V_{IDL}	Low-level input voltage between differential inputs	1	−5	−0.025	V
$V_{IH(S)}$	High-level input voltage at strobe inputs	3	2	5.5	V
$V_{IL(S)}$	Low-level input voltage at strobe inputs	3	0	0.8	V

† The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS‡		SN55107A, SN75107A			SN55108A, SN75108A			UNIT
					MIN	TYP§	MAX	MIN	TYP§	MAX	
I_{IH}	High-level input current into 1A or 2A	2	V_{CC+} = MAX, V_{ID} = 0.5 V,	V_{CC-} = MAX, V_{IC} = −3 V to 3 V		30	75		30	75	μA
I_{IL}	Low-level input current into 1A or 2A	2	V_{CC+} = MAX, V_{ID} = −2 V,	V_{CC-} = MAX, V_{IC} = −3 V to 3 V			−10			−10	μA
I_{IH}	High-level input current into 1G or 2G	4	V_{CC+} = MAX, $V_{IH(S)}$ = 2.4 V	V_{CC-} = MAX,			40			40	μA
			V_{CC+} = MAX, $V_{IH(S)}$ = MAX V_{CC+}	V_{CC-} = MAX,			1			1	mA
I_{IL}	Low-level input current into 1G or 2G	4	V_{CC+} = MAX, $V_{IL(S)}$ = 0.4 V	V_{CC-} = MAX,			−1.6			−1.6	mA
I_{IH}	High-level input current into S	4	V_{CC+} = MAX, $V_{IH(S)}$ = 2.4 V	V_{CC-} = MAX,			80			80	μA
			V_{CC+} = MAX, $V_{IH(S)}$ = MAX V_{CC+}	V_{CC-} = MAX,			2			2	mA
I_{IL}	Low-level input current into S	4	V_{CC+} = MAX, $V_{IL(S)}$ = 0.4 V	V_{CC-} = MAX,			−3.2			−3.2	mA
V_{OH}	High-level output voltage	3	V_{CC+} = MIN, I_{load} = −400 μA,	V_{CC-} = MIN, V_{IC} = −3 V to 3 V	2.4						V
V_{OL}	Low-level output voltage	3	V_{CC+} = MIN, I_{sink} = 16 mA,	V_{CC-} = MIN, V_{IC} = −3 V to 3 V			0.4			0.4	V
I_{OH}	High-level output current	3	V_{CC+} = MIN, V_{OH} = MAX V_{CC+}	V_{CC-} = MIN,						250	μA
I_{OS}	Short-circuit output current	5	V_{CC+} = MAX,	V_{CC-} = MAX	−18		−70				mA
I_{CCH+}	High-logic-level supply current from V_{CC+}	6	V_{CC+} = MAX, V_{ID} = 25 mV,	V_{CC-} = MAX, T_A = 25°C		18	30		18	30	mA
I_{CCH-}	High-logic-level supply current from V_{CC-}	6	V_{CC+} = MAX, V_{ID} = 25 mV,	V_{CC-} = MAX, T_A = 25°C		−8.4	−15		−8.4	−15	mA

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

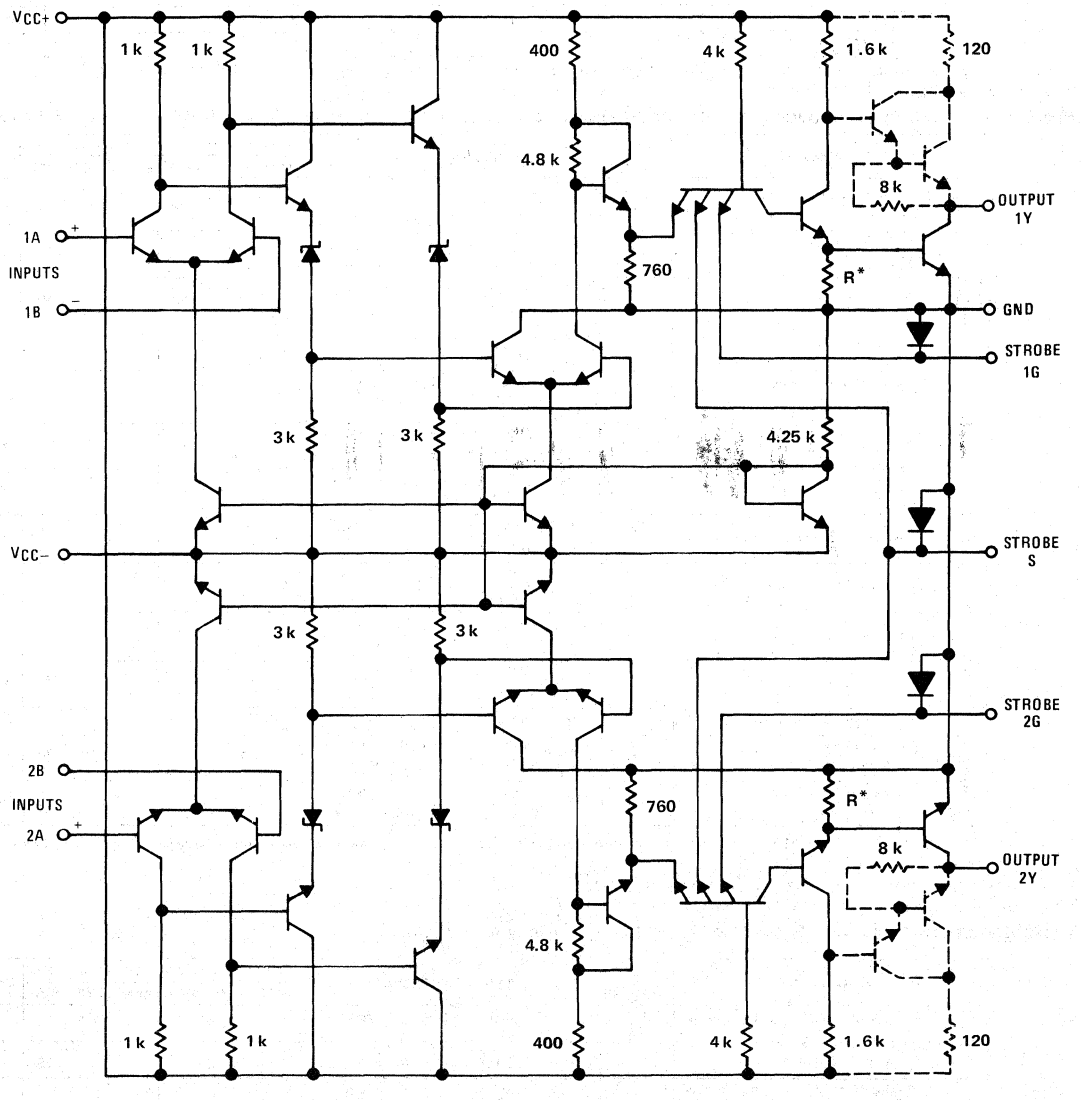
§ All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.

¶ Not more than one output should be shorted at a time.

switching characteristics, V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS		SN55107A, SN75107A			SN55108A, SN75108A			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
$t_{PLH(D)}$	Propagation delay time, low-to-high level, from differential inputs A and B to output	7	R_L = 390 Ω,	C_L = 50 pF		17	25				ns
			R_L = 390 Ω,	C_L = 15 pF					19	25	
$t_{PHL(D)}$	Propagation delay time, high-to-low level, from differential inputs A and B to output	7	R_L = 390 Ω,	C_L = 50 pF		17	25				ns
			R_L = 390 Ω,	C_L = 15 pF					19	25	
$t_{PLH(S)}$	Propagation delay time, low-to-high level, from strobe input G or S to output	7	R_L = 390 Ω,	C_L = 50 pF		10	15				ns
			R_L = 390 Ω,	C_L = 15 pF					13	20	
$t_{PHL(S)}$	Propagation delay time, high-to-low level, from strobe input G or S to output	7	R_L = 390 Ω,	C_L = 50 pF		8	15				ns
			R_L = 390 Ω,	C_L = 15 pF					13	20	

schematic



R* = 1 kΩ for SN55107A and SN75107A, 750 Ω for SN55108A and SN75108A.

NOTES: 1. Component values shown are nominal.
2. Resistance values are in ohms.
3. Components shown with dashed lines are applicable to the SN55107A and SN75107A only.

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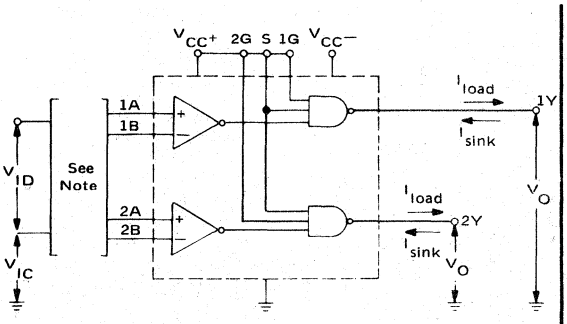
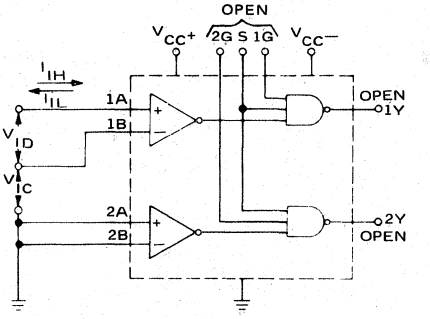
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



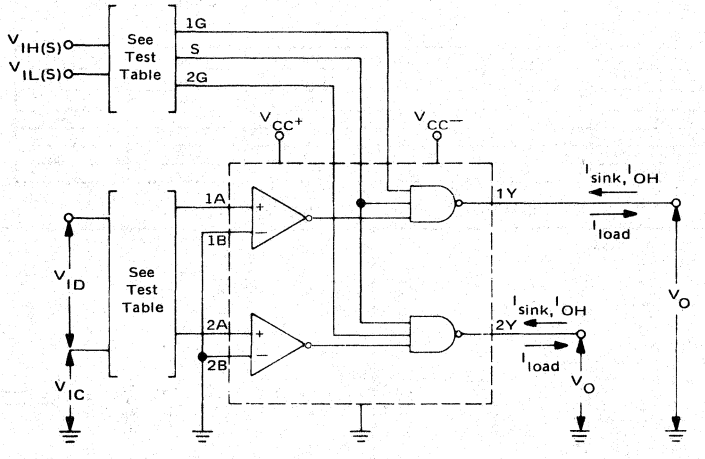
NOTE: When testing one channel, the inputs of the other channel are grounded.

FIGURE 1–V_{IDH} and V_{IDL}



NOTE: Each pair of differential inputs is tested separately. The inputs of the other pair are grounded.

FIGURE 2–I_{IH} and I_{IL}



TEST TABLE

SN55107A SN75107A	SN55108A SN75108A	V_{ID}	STROBE 1G or 2G	STROBE S
TEST		APPLY		
V_{OH}	I_{OH}	+25 mV	$V_{IH(S)}$	$V_{IH(S)}$
V_{OH}	I_{OH}	−25 mV	$V_{IL(S)}$	$V_{IH(S)}$
V_{OH}	I_{OH}	−25 mV	$V_{IH(S)}$	$V_{IL(S)}$
V_{OL}	V_{OL}	−25 mV	$V_{IH(S)}$	$V_{IH(S)}$

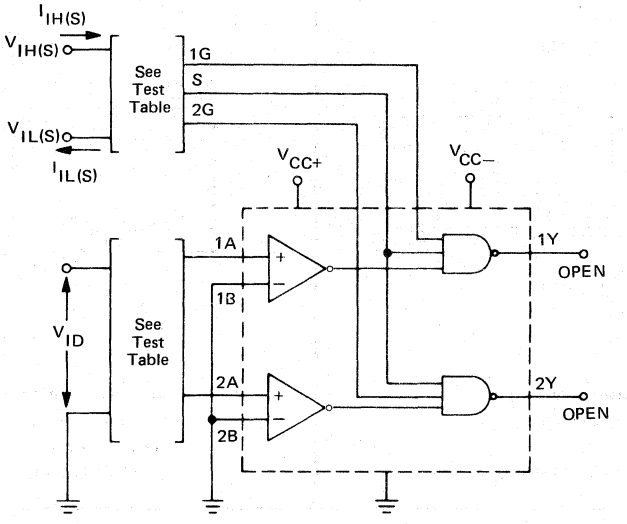
NOTES: 1. V_{IC} = −3 V to 3 V.
2. When testing one channel, the inputs of the other channel should be grounded.

FIGURE 3–$V_{IH(S)}$, $V_{IL(S)}$, V_{OH}, V_{OL}, and I_{OH}

† Arrows indicate actual direction of current flow.

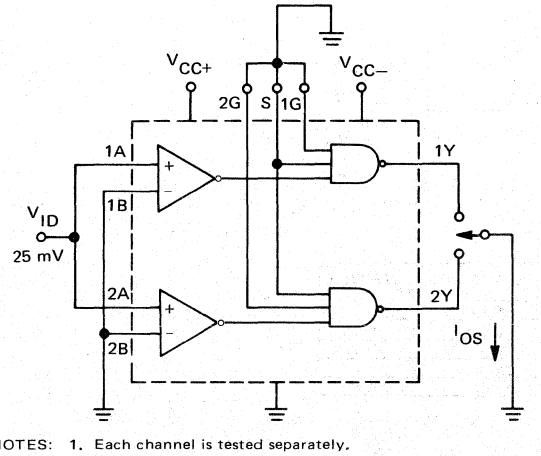
PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



TEST	INPUT 1A	INPUT 2A	STROBE 1G	STROBE S	STROBE 2G
I_{IH} at Strobe 1G	+25 mV	Gnd	$V_{IH(S)}$	Gnd	Gnd
I_{IH} at Strobe 2G	Gnd	+25 mV	Gnd	Gnd	$V_{IH(S)}$
I_{IH} at Strobe S	+25 mV	+25 mV	Gnd	$V_{IH(S)}$	Gnd
I_{IL} at Strobe 1G	−25 mV	Gnd	$V_{IL(S)}$	4.5 V	Gnd
I_{IL} at Strobe 2G	Gnd	−25 mV	Gnd	4.5 V	$V_{IL(S)}$
I_{IL} at Strobe S	−25 mV	−25 mV	4.5 V	$V_{IL(S)}$	4.5 V

FIGURE 4 – $I_{IH(G)}$, $I_{IL(G)}$, $I_{IH(S)}$, and $I_{IL(S)}$



NOTES: 1. Each channel is tested separately.
2. Not more than one output should be grounded at a time.

FIGURE 5–I_{OS}

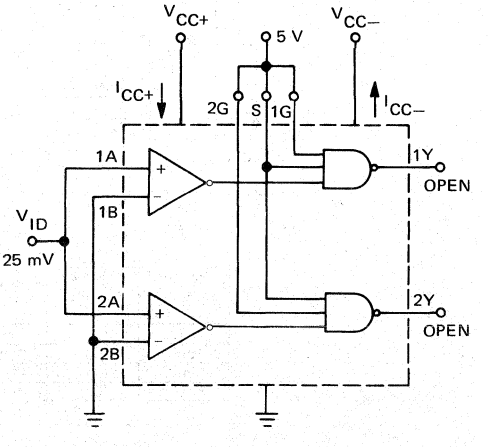


FIGURE 6–I_{CC+} and I_{CC-}

† Arrows indicate actual direction of current flow.

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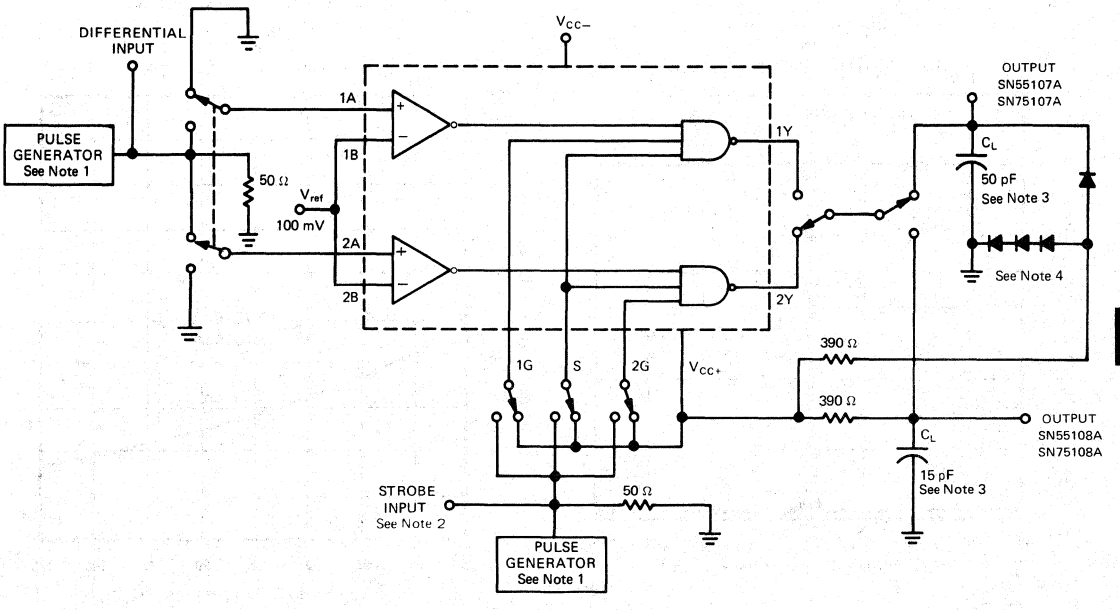
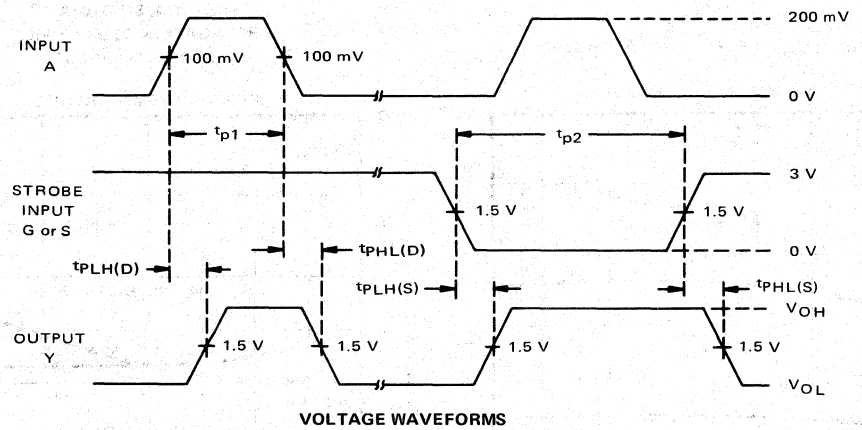
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: 1. The pulse generators have the following characteristics: Z_{out} = 50 Ω, $t_r = t_f = 10 \pm 5$ ns, t_{p1} = 500 ns, PRR = 1 MHz, t_{p2} = 1 ms, PRR = 500 kHz.

2. Strobe input pulse is applied to Strobe 1G when inputs 1A-1B are being tested, to Strobe S when inputs 1A-1B or 2A-2B are being tested, and to Strobe 2G when inputs 2A-2B are being tested.

3. C_L includes probe and jig capacitance.

4. All diodes are 1N916.

FIGURE 7—PROPAGATION DELAY TIMES

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

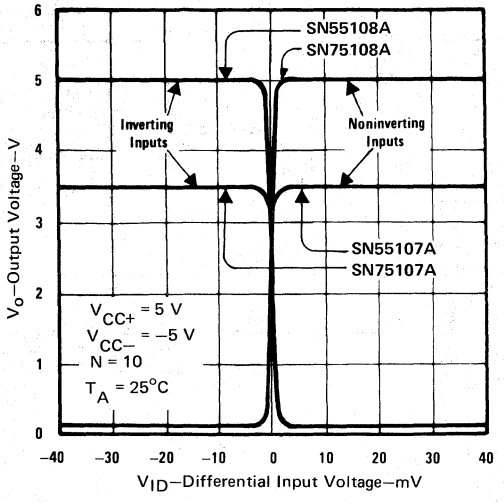


FIGURE 8

HIGH-LEVEL INPUT CURRENT
INTO 1A or 2A
vs
FREE-AIR TEMPERATURE

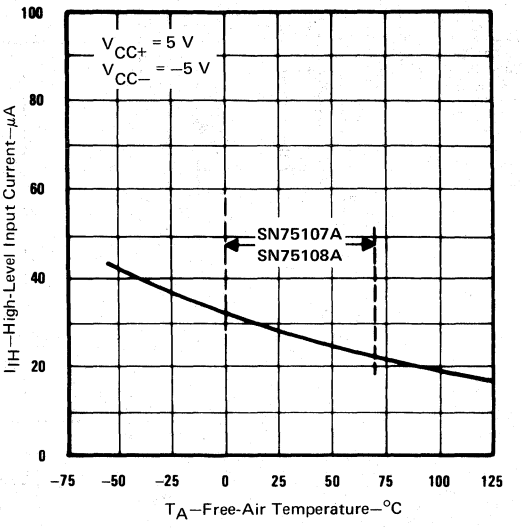


FIGURE 9

HIGH-LOGIC-LEVEL SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

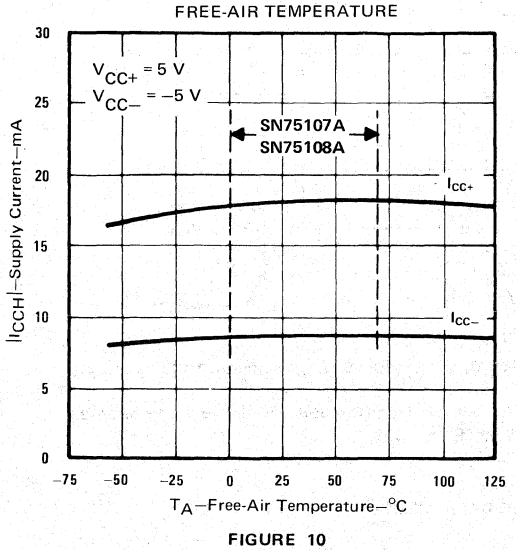


FIGURE 10

SN55107A, SN75107A
PROPAGATION DELAY TIME
(DIFFERENTIAL INPUTS)
vs
FREE-AIR TEMPERATURE

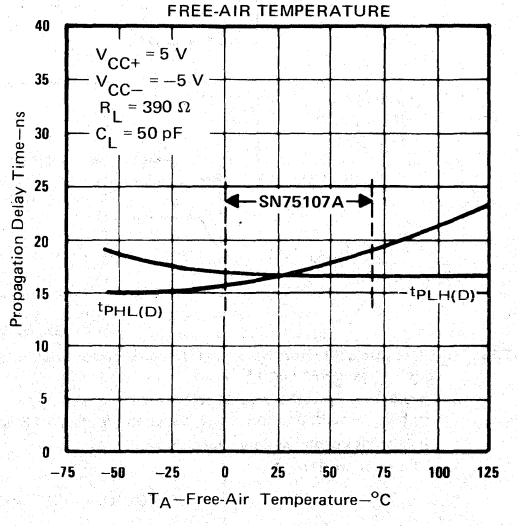


FIGURE 11

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TYPICAL CHARACTERISTICS

SN55108A, SN75108A
PROPAGATION DELAY TIME
LOW-TO-HIGH LEVEL
(DIFFERENTIAL INPUTS)
vs
FREE-AIR TEMPERATURE

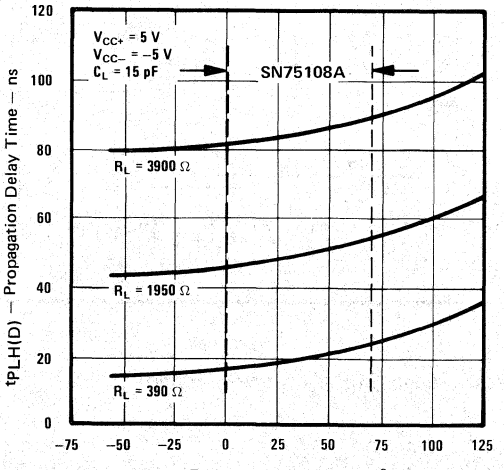


FIGURE 12

SN55108A, SN75108A
PROPAGATION DELAY TIME
HIGH-TO-LOW LEVEL
(DIFFERENTIAL INPUTS)
vs
FREE-AIR TEMPERATURE

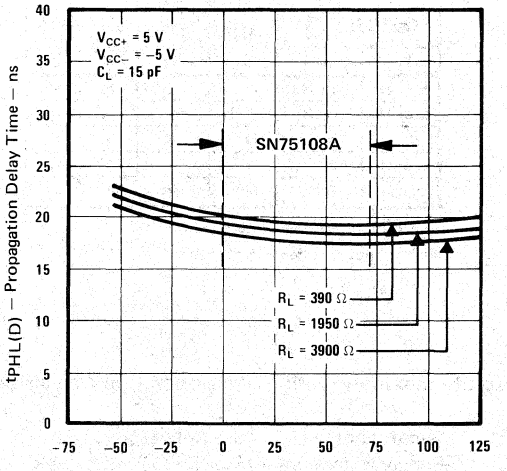


FIGURE 13

SN55107A, SN75107A
PROPAGATION DELAY TIME
(STROBE INPUTS)
vs
FREE-AIR TEMPERATURE

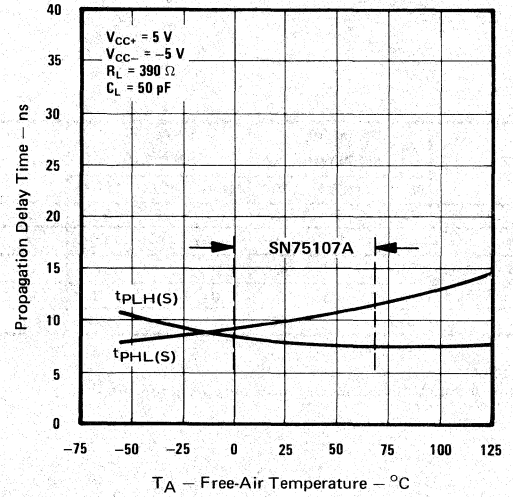


FIGURE 14

SN55108A, SN75108A
PROPAGATION DELAY TIME
(STROBE INPUTS)
vs
FREE-AIR TEMPERATURE

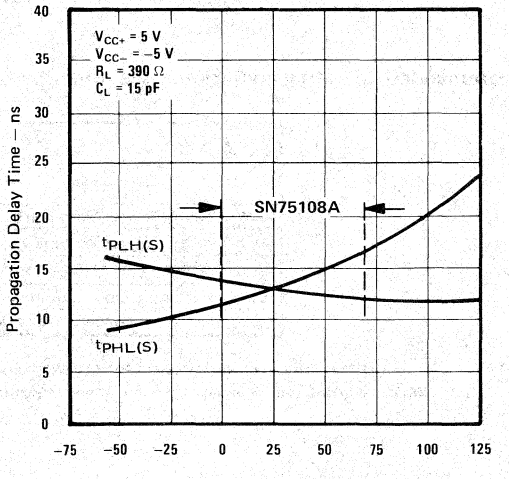
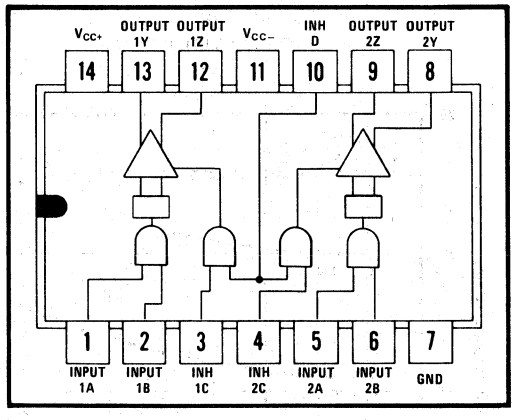


FIGURE 15

3

SN55109, SN55110 J DUAL-IN-LINE PACKAGE
SN75109, SN75110 J OR N DUAL-IN-LINE PACKAGE



logic

TRUTH TABLE

LOGIC INPUTS		INHIBITOR INPUTS		OUTPUTS	
A	B	C	D	Y	Z
L or H	L or H	L	L or H	H	H
L or H	L or H	L or H	L	H	H
L	L or H	H	H	L	H
L or H	L	H	H	L	H
H	H	H	H	H	L

Low output represents the on state

High output represents the off state

3

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (See Note 1) . . . . . 7 V
Supply voltage V_{CC-} (See Note 1) . . . . . –7 V
Logic and inhibitor input voltages (See Note 1) . . . . . 5.5 V
Common-mode output voltage (See Note 1) . . . . . –5 to 12 V
Operating free-air temperature range, Series 55 . . . . . –55°C to 125°C
Series 75 . . . . . 0°C to 70°C
Storage temperature range, ceramic dual-in-line (J) package . . . . . –65°C to 150°C
plastic dual-in-line (N) package . . . . . –55°C to 150°C

recommended operating conditions (see note 2)

	SN55109, SN55110			SN75109, SN75110			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC+} (See Note 1)	4.5	5	5.5	4.75	5	5.25	V
Supply voltage V_{CC-} (See Note 1)	–4.5	–5	–5.5	–4.75	–5	–5.25	V
Positive common-mode output voltage (See Note 1)	0		10	0		10	V
Negative common-mode output voltage (See Note 1)	0		–3	0		–3	V
Operating free-air temperature range	–55		125	0		70	°C

NOTES: 1. These voltage values are with respect to the network ground terminal.
2. When using only one channel of the line drivers, the other channel should be inhibited and/or its outputs grounded.

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definition of input logic levels†

		TEST FIGURE	MIN	MAX	UNIT
V_{IH}	High-level input voltage at any input	16, 17	2	5.5	V
V_{IL}	Low-level input voltage at any input	16, 17	0	0.8	V

†The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS‡		SN55109, SN75109 MIN	SN55109, SN75109 TYP§	SN55109, SN75109 MAX	SN55110, SN75110 MIN	SN55110, SN75110 TYP§	SN55110, SN75110 MAX	UNIT
$I_{IH(L)}$	High-level input current into 1A, 1B, 2A or 2B	16	V_{CC+} = MAX, $V_{IH(L)}$ = 2.4 V	V_{CC-} = MAX,			40			40	μA
			V_{CC+} = MAX, $V_{IH(L)}$ = MAX V_{CC+}	V_{CC-} = MAX,			1			1	mA
$I_{IL(L)}$	Low-level input current into 1A, 1B, 2A or 2B	16	V_{CC+} = MAX, $V_{IL(L)}$ = 0.4 V	V_{CC-} = MAX,			−3			−3	mA
$I_{IH(I)}$	High-level input current into 1C or 2C	17	V_{CC+} = MAX, $V_{IH(I)}$ = 2.4 V	V_{CC-} = MAX,			40			40	μA
			V_{CC+} = MAX, $V_{IH(I)}$ = MAX V_{CC+}	V_{CC-} = MAX,			1			1	mA
$I_{IL(I)}$	Low-level input current into 1C or 2C	17	V_{CC+} = MAX, $V_{IL(I)}$ = 0.4 V	V_{CC-} = MAX,			−3			−3	mA
$I_{IH(I)}$	High-level input current into D	17	V_{CC+} = MAX, $V_{IH(I)}$ = 2.4 V	V_{CC-} = MAX,			80			80	μA
			V_{CC+} = MAX, $V_{IH(I)}$ = MAX V_{CC+}	V_{CC-} = MAX,			2			2	mA
$I_{IL(I)}$	Low-level input current into D	17	V_{CC+} = MAX, $V_{IL(I)}$ = 0.4 V	V_{CC-} = MAX,			−6			−6	mA
$I_{O(on)}$	On-state output current	18	V_{CC+} = MAX,	V_{CC-} = MAX		7			15		mA
			V_{CC+} = MIN,	V_{CC-} = MAX	3.5			6.5			mA
$I_{O(off)}$	Off-state output current	18	V_{CC+} = MIN,	V_{CC-} = MIN		100			100		μA
$I_{CC+(on)}$	Supply current from V_{CC+} with driver enabled	19	$V_{IL(L)}$ = 0.4 V,	$V_{IH(I)}$ = 2 V		18	30		23	35	mA
$I_{CC-(on)}$	Supply current from V_{CC-} with driver enabled	19	$V_{IL(L)}$ = 0.4 V,	$V_{IH(I)}$ = 2 V		−18	−30		−34	−50	mA
$I_{CC+(off)}$	Supply current from V_{CC+} with driver inhibited	19	$V_{IL(L)}$ = 0.4 V,	$V_{IL(I)}$ = 0.4 V		18			21		mA
$I_{CC-(off)}$	Supply current from V_{CC-} with driver inhibited	19	$V_{IL(L)}$ = 0.4 V,	$V_{IL(I)}$ = 0.4 V		−10			−17		mA

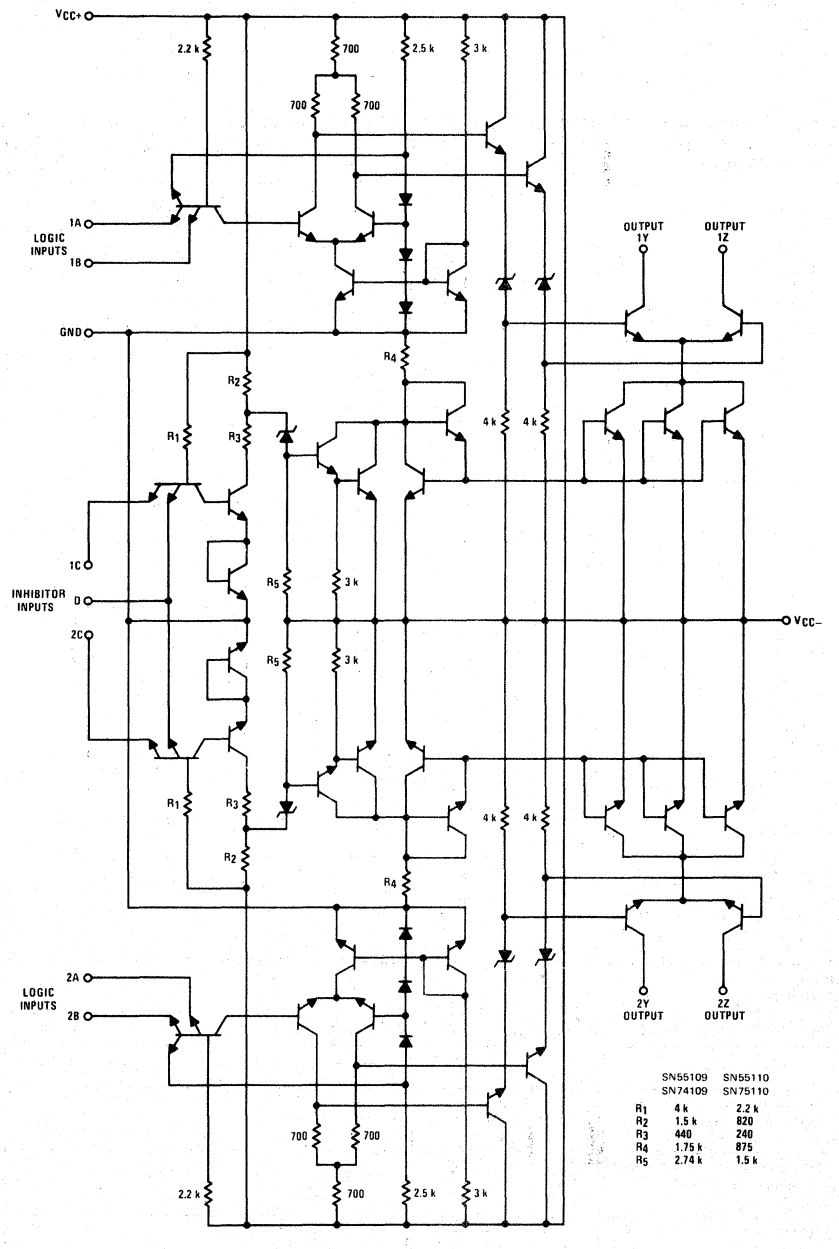
‡For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions for the applicable device type.

§All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.

switching characteristics, V_{CC+} = 5 V, V_{CC-} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{PLH(L)}$	Propagation delay time, low-to-high level, from logic input A or B to output Y or Z	20	R_L = 50 Ω,	C_L = 40 pF		9	15	ns
$t_{PHL(L)}$	Propagation delay time, high-to-low level, from logic input A or B to output Y or Z	20	R_L = 50 Ω,	C_L = 40 pF		9	15	ns
$t_{PLH(I)}$	Propagation delay time, low-to-high level, from inhibitor input C or D to output Y or Z	20	R_L = 50 Ω,	C_L = 40 pF		16	25	ns
$t_{PHL(I)}$	Propagation delay time, high-to-low level, from inhibitor input C or D to output Y or Z	20	R_L = 50 Ω,	C_L = 40 pF		13	25	ns

schematic



	SN55109 SN74109	SN55110 SN75110
R_1	4 k	2.2 k
R_2	1.5 k	820
R_3	440	240
R_4	1.75 k	875
R_5	2.74 k	1.5 k

NOTES: 1. Component values shown are nominal.
2. Resistance values are in ohms.

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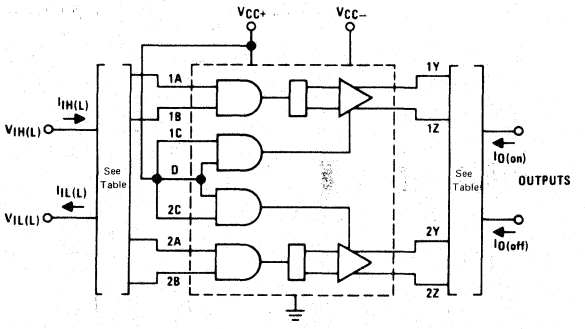
PARAMETER MEASUREMENT INFORMATION

d-c test circuits †

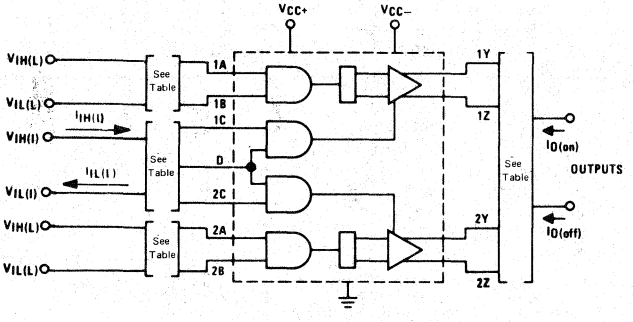


TEST TABLE

TEST AT ANY LOGIC INPUT	LOGIC INPUTS NOT UNDER TEST	ALL INHIBITOR INPUTS	OUTPUT 1Y or 2Y	OUTPUT 1Z or 2Z
$V_{IH(L)}$	Open	$V_{IH(I)}$	H (See Note 1)	L (See Note 1)
$V_{IL(L)}$	V_{CC+}	$V_{IH(I)}$	L (See Note 1)	H (See Note 1)
$I_{IH(L)}$	Gnd	$V_{IH(I)}$	Gnd	Gnd
$I_{IL(L)}$	4.5 V	$V_{IH(I)}$	Gnd	Gnd

NOTES: 1. Low output represents the on state, high output represents the off state.
2. Each input is tested separately.

FIGURE 16 – $V_{IH(L)}$, $V_{IL(L)}$, $I_{IH(L)}$, and $I_{IL(L)}$



TEST TABLE

TEST AT ANY INHIBITOR INPUT	ALL LOGIC INPUTS	INHIBITOR INPUTS NOT UNDER TEST	OUTPUT 1Y or 2Y	OUTPUT 1Z or 2Z
$V_{IH(I)}$	$V_{IH(L)}$	Open	H (See Note 1)	L (See Note 1)
	$V_{IL(L)}$	Open	L (See Note 1)	H (See Note 1)
$V_{IL(I)}$	$V_{IH(L)}$	V_{CC+}	H (See Note 1)	H (See Note 1)
	$V_{IL(L)}$	V_{CC+}	H (See Note 1)	H (See Note 1)
$I_{IH(I)}$	Gnd	Gnd	Gnd	Gnd
$I_{IL(I)}$	Gnd	4.5 V	Gnd	Gnd

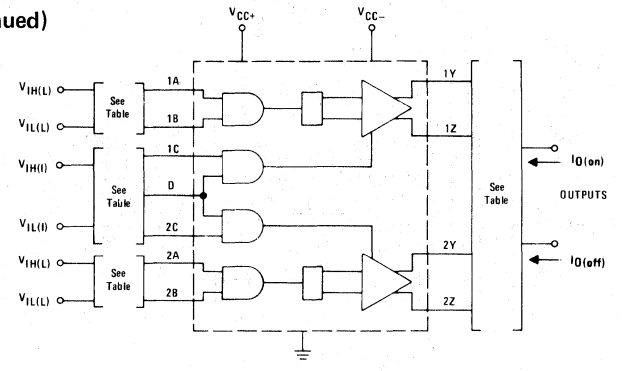
NOTES: 1. Low output represents the on state, high output represents the off state.
2. Each input is tested separately.

FIGURE 17 – $V_{IH(I)}$, $V_{IL(I)}$, $I_{IH(I)}$, $I_{IL(I)}$

† Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

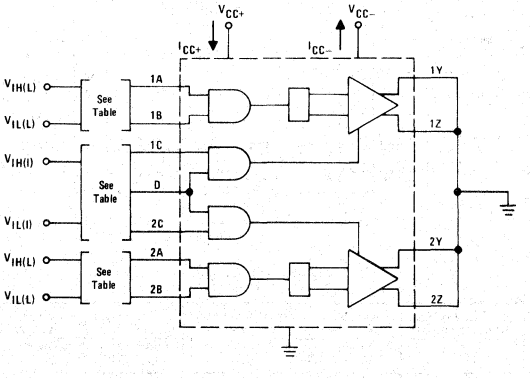
d-c test circuits† (continued)



TEST TABLE

TEST		LOGIC INPUTS		INHIBITOR INPUTS	
		1A or 2A	1B or 2B	1C or 2C	D
$I_{O(on)}$	at output 1Y or 2Y	$V_{IL(L)}$	$V_{IL(L)}$	$V_{IH(I)}$	$V_{IH(I)}$
		$V_{IL(L)}$	$V_{IH(L)}$		
		$V_{IH(L)}$	$V_{IL(L)}$		
$I_{O(on)}$	at output 1Z or 2Z	$V_{IH(L)}$	$V_{IH(L)}$	$V_{IH(I)}$	$V_{IH(I)}$
$I_{O(off)}$	at output 1Y or 2Y	$V_{IH(L)}$	$V_{IH(L)}$	$V_{IH(I)}$	$V_{IH(I)}$
$I_{O(off)}$	at output 1Z or 2Z	$V_{IL(L)}$	$V_{IL(L)}$	$V_{IH(I)}$	$V_{IH(I)}$
		$V_{IL(L)}$	$V_{IH(L)}$		
		$V_{IH(L)}$	$V_{IL(L)}$		
$I_{O(off)}$	at output 1Y, 2Y, 1Z, or 2Z	Either state	Either state	$V_{IL(I)}$	$V_{IL(I)}$
				$V_{IL(I)}$	$V_{IH(I)}$
				$V_{IH(I)}$	$V_{IL(I)}$

FIGURE 18 –$I_{O(on)}$ and $I_{O(off)}$



TEST TABLE

TEST		ALL LOGIC INPUTS	ALL INHIBITOR INPUTS
$I_{CC+(on)}$	Driver enabled	$V_{IL(L)}$	$V_{IH(I)}$
$I_{CC-(on)}$	Driver enabled	$V_{IL(L)}$	$V_{IH(I)}$
$I_{CC+(off)}$	Driver inhibited	$V_{IL(L)}$	$V_{IL(I)}$
$I_{CC-(off)}$	Driver inhibited	$V_{IL(L)}$	$V_{IL(I)}$

FIGURE 19 –I_{CC+} and I_{CC-}

† Arrows indicate actual direction of current flow.

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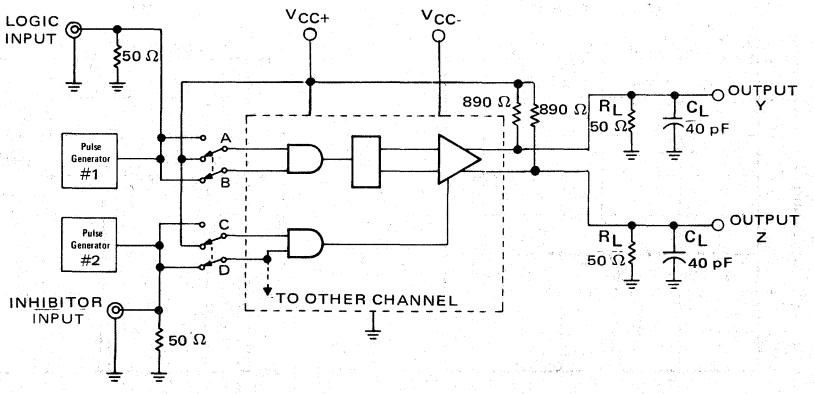
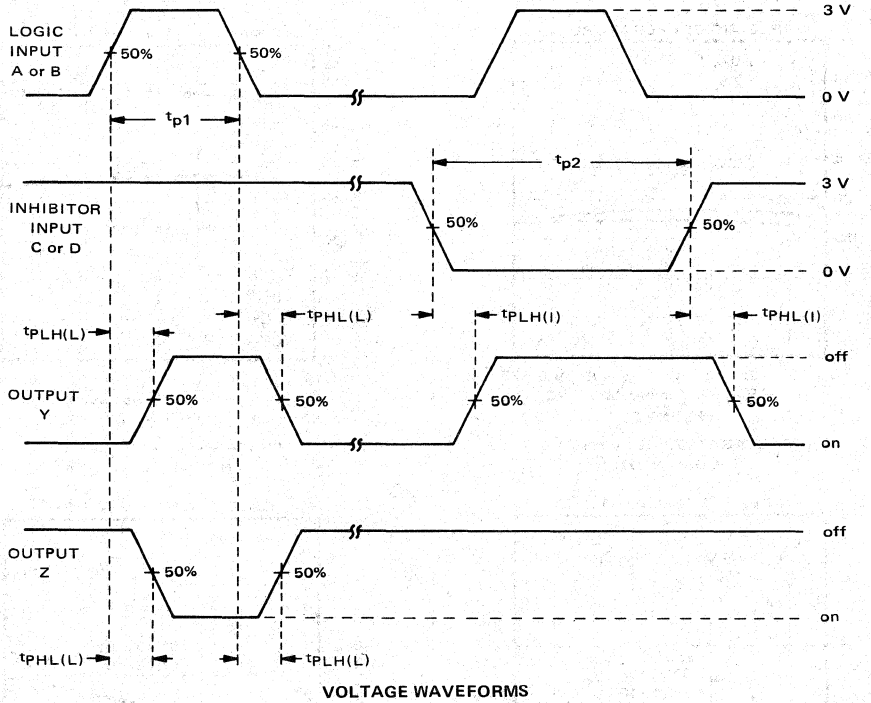
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: 1. The pulse generators have the following characteristics: Z_{out} = 50 Ω, $t_r = t_f = 10 \pm 5$ ns, t_{p1} = 500 ns, PRR = 1 MHz, t_{p2} = 1 ms, PRR = 500 kHz.
2. C_L includes probe and jig capacitance.
3. For simplicity, only one channel and the inhibitor connections are shown.

FIGURE 20–PROPAGATION DELAY TIMES

TYPICAL CHARACTERISTICS

SN55109, SN75109
OUTPUT CURRENT
vs
LOGIC INPUT VOLTAGE

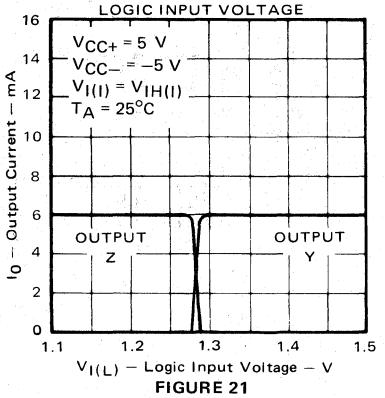


FIGURE 21

SN55110, SN75110
OUTPUT CURRENT
vs
LOGIC INPUT VOLTAGE

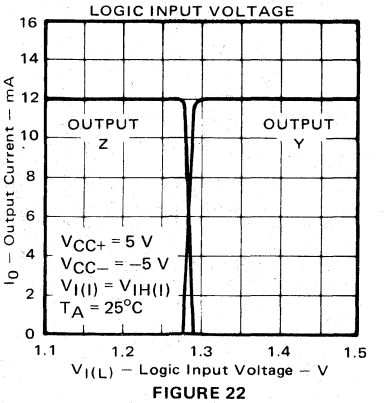


FIGURE 22

SN55109, SN75109
SUPPLY CURRENT WITH DRIVER ENABLED
vs
FREE-AIR TEMPERATURE

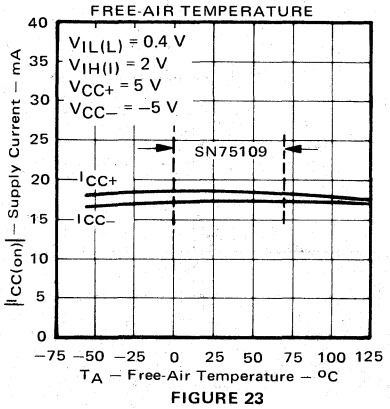


FIGURE 23

SN55110, SN75110
SUPPLY CURRENT WITH DRIVER ENABLED
vs
FREE-AIR TEMPERATURE

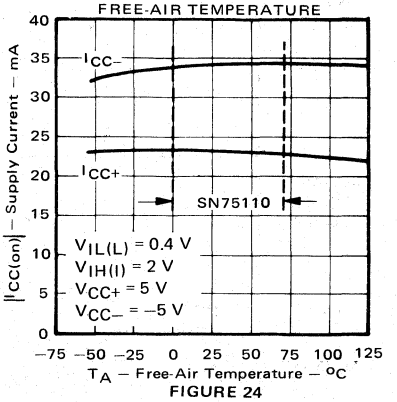


FIGURE 24

PROPAGATION DELAY TIME
(LOGIC INPUTS)
vs
FREE-AIR TEMPERATURE

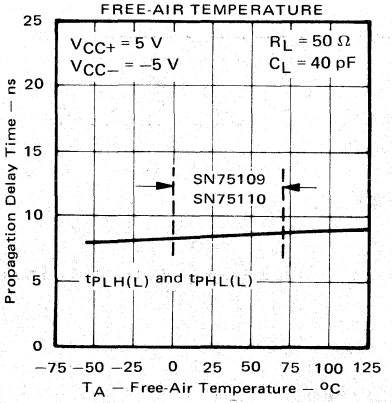


FIGURE 25

PROPAGATION DELAY TIME
(INHIBITOR INPUTS)
vs
FREE-AIR TEMPERATURE

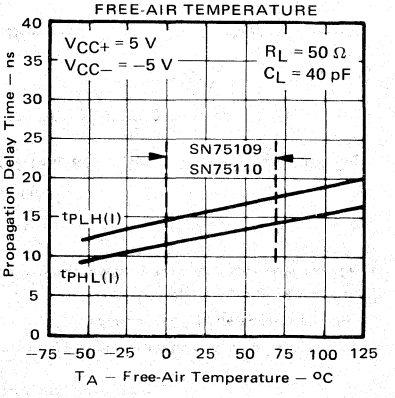


FIGURE 26

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TYPICAL APPLICATION DATA

BASIC BALANCED-LINE TRANSMISSION SYSTEM

Series 55/75107A dual line circuits are designed specifically for use in high-speed data transmission systems that utilize balanced, terminated transmission lines such as twisted-pair lines. The system operates in the balanced mode, so that noise induced on one line is also induced on the other. The noise appears common-mode at the receiver input terminals where it is rejected. The ground connection between the line driver and receiver is not part of the signal circuit so that system performance is not affected by circulating ground currents.

The unique driver-output circuit allows terminated transmission lines to be driven at normal line impedances. High-speed system operation is ensured since line reflections are virtually eliminated when terminated lines are used. Cross-talk is minimized by low signal amplitudes and low line impedances.

The typical data delay in a system is approximately (30 + 1.3 L) nanoseconds, where L is the distance in feet separating the driver and receiver. This delay includes one gate delay in both the driver and receiver.

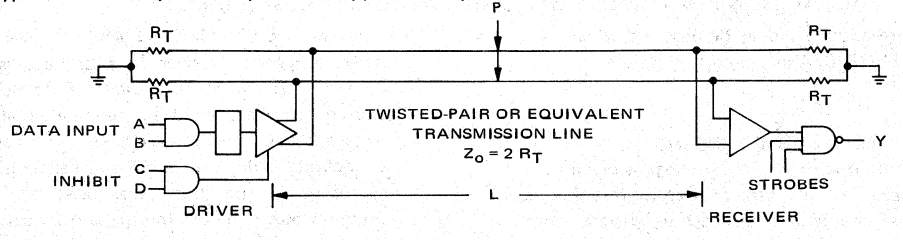
Data is impressed on the balanced-line system by unbalancing the line voltages with the driver output current. The driven line is selected by appropriate driver-input logic levels. The voltage difference is approximately:

$$V_{DIFF} \simeq 1/2\ I_{O(on)} \cdot R_T.$$

High series line resistance will cause degradation of the signal. The receivers, however, will detect signals as low as 25 mV (or less). For normal line resistances, data may be recovered from lines of several thousand feet in length.

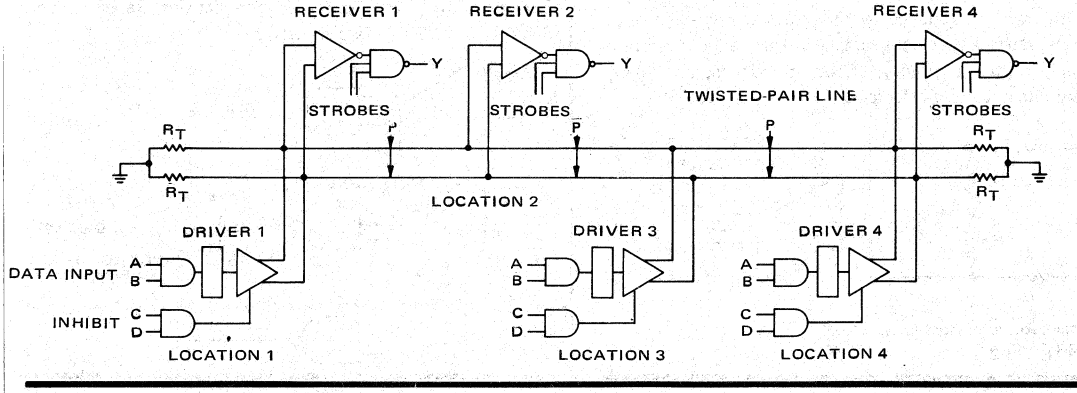
Line-termination resistors (R_T) are required only at the extreme ends of the line. For short lines, termination resistors at the receiver only may prove adequate. The signal amplitude will then be approximately:

$$V_{DIFF} \simeq I_{O(on)} \cdot R_T.$$



DATA-BUS OR PARTY-LINE SYSTEM

The strobe feature of the receivers and the inhibit feature of the drivers allow the Series 55/75107A dual line circuits to be used in data-bus or party-line systems. In these applications, several drivers and receivers may share a common transmission line. An enabled driver transmits data to all enabled receivers on the line while other drivers and receivers are disabled. Data is thus time-multiplexed on the transmission line. Series 55/75107A device specifications allow widely varying thermal and electrical environments at the various driver and receiver locations. The data-bus system offers maximum performance at minimum cost.



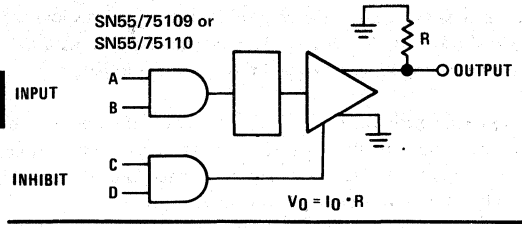
TYPICAL APPLICATION DATA

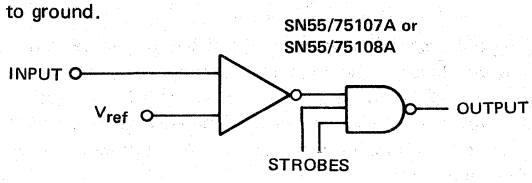
UNBALANCED OR SINGLE-LINE SYSTEMS

Series 55/75107A dual line circuits may also be used in unbalanced or single-line systems. Although these systems do not offer the same performance as balanced systems for long lines, they are adequate for very short lines where environmental noise is not severe.

The receiver threshold level is established by applying a d-c reference voltage to one receiver input terminal. The signal from the transmission line is applied to the remaining input. The reference voltage should be optimized so that signal swing is symmetrical about it for maximum noise margin. The reference voltage should be in the range of −3 volts to +3 volts. It can be provided by a voltage supply or by a voltage divider from an available supply voltage.

A single-ended output from a driver may be used in single-line systems. Coaxial or shielded line is preferred for minimum noise and cross-talk problems. For large signal swings, the high output current (12 mA) of the SN55/75110 is recommended. Drivers may be parallelled for higher current. The unused driver output must be tied to ground.





PRECAUTIONS IN THE USE OF SERIES 55/75107A LINE CIRCUITS

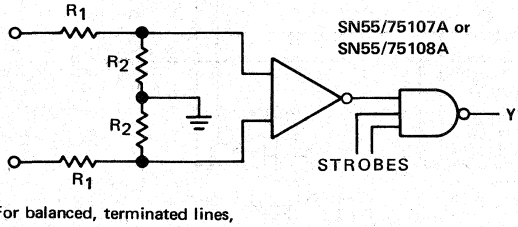
The following precautions should be observed when using or testing Series 55/75107A line circuits:

(1) Drivers, SN55/75109 and SN55/75110
When only one driver in a package is being used, the outputs of the other driver must either be grounded or inhibited in order to prevent excess power dissipation.

(2) Receivers, SN55/75107A and SN55/75108A
When only one receiver in a package is being used, at least one of the differential inputs of the unused receiver should be terminated at some voltage between −3 volts and +3 volts, preferably at ground. Failure to do so will cause improper operation of the unit being used because of common bias circuitry for the current sources of the two receivers.

INCREASING COMMON-MODE INPUT VOLTAGE RANGE OF RECEIVER

The SN55/75107A and SN55/75108A line receivers feature a common-mode input voltage range of ±3 volts. This satisfies the requirements for all but the noisiest system applications. For these severe noise environments, the common-mode range can be extended by the use of external input attenuators. Common-mode input voltages can in this way be reduced to ±3 volts at the receiver input terminals. Differential data signals will be reduced proportionately. Input sensitivity, input impedance, and delay times will be adversely affected.

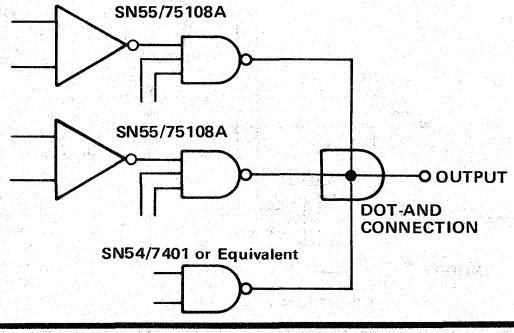


For balanced, terminated lines,
$Z_o = 2R_1 + 2R_2$

SN55/75108A DOT-AND OUTPUT CONNECTIONS

The SN55/75108A line receivers feature an open-collector-output circuit that can be connected in the DOT-AND logic configuration with other SN55/75108A outputs, SN5401/7401 outputs, or other similar outputs. This allows a level of logic to be implemented without additional logic delay.

For rules for such DOT-AND connections, refer to the SN5401 or SN7401 data sheet.



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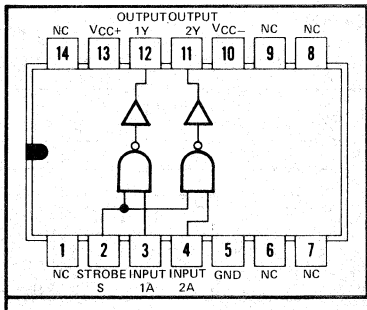
CIRCUIT TYPE SN75150
DUAL LINE DRIVER

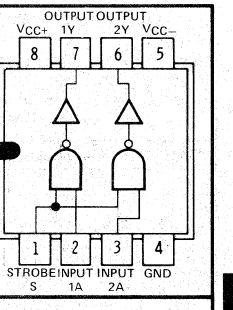
SATISFIES REQUIREMENTS OF EIA STANDARD RS-232-C

- Withstands Sustained Output Short-Circuit to any Low-Impedance Voltage between −25 V and 25 V
- 2 μs Max Transition Time through the +3 V to −3 V Transition Region under Full 2500-pF Load
- Inputs Compatible with Most TTL and DTL Families
- Common Strobe Input
- Inverting Output
- Slew Rate can be Controlled with an External Capacitor at the Output
- Standard Supply Voltages . . . ±12 V

J OR N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



P
DUAL-IN-LINE PACKAGE
(TOP VIEW)



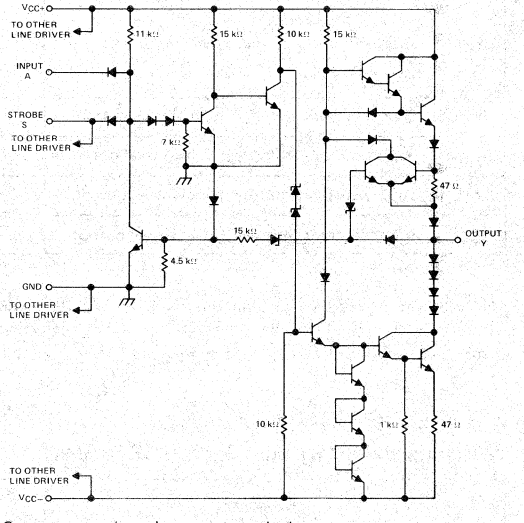
positive logic: $Y = \overline{AS}$

NC—No internal connection

description

The SN75150 is a monolithic dual line driver designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by EIA Standard RS-232-C. A rate of 20,000 bits per second can be transmitted with a full 2500-pF load. Other applications are in data-transmission systems using relatively short single lines, in level translators, and for driving MOS devices. The logic input is compatible with most TTL and DTL families. Operation is from +12-volt and −12-volt power supplies. The SN75150 is characterized for operation from 0°C to 70°C.

schematic (each line driver)



Component values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1)	15 V
Supply voltage V_{CC-} (see Note 1)	−15 V
Input voltage (see Note 1)	15 V
Applied output voltage (see Note 1)	±25 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage V_{CC+}	10.8	12	13.2	V
Supply voltage V_{CC-}	−10.8	−12	−13.2	V
Input voltage, V_I	0		5.5	V
Applied output voltage, V_O			±15	V
Operating free-air temperature, T_A	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP†	MAX (SEE NOTE 2)	UNIT
V_{IH}	High-level input voltage	1			2			V
V_{IL}	Low-level input voltage	2					0.8	V
V_{OH}	High-level output voltage	2	V_{CC+} = 10.8 V, V_{CC-} = −13.2 V, V_{IL} = 0.8 V, R_L = 3 kΩ to 7 kΩ		5	8		V
V_{OL}	Low-level output voltage	1	V_{CC+} = 10.8 V, V_{CC-} = −10.8 V, V_{IH} = 2 V, R_L = 3 kΩ to 7 kΩ			−8	−5	V
I_{IH}	High-level input current	3	V_{CC+} = 13.2 V, V_{CC-} = −13.2 V, V_I = 2.4 V	Data input		1	10	μA
				Strobe input		2	20	
I_{IL}	Low-level input current	3	V_{CC+} = 13.2 V, V_{CC-} = −13.2 V, V_I = 0.4 V	Data input		−1	−1.6	mA
				Strobe input		−2	−3.2	
I_{OS}	Short-circuit output current	4	V_{CC+} = 13.2 V, V_{CC-} = −13.2 V	V_O = 25 V		2		mA
				V_O = −25 V		−3		
				V_O = 0 V, V_I = 3 V		15		
				V_O = 0 V, V_I = 0 V		−15		
I_{CCH+}	Supply current from V_{CC+}, high-level output	5	V_{CC+} = 13.2 V, V_{CC-} = −13.2 V, V_I = 0 V, R_L = 3 kΩ, T_A = 25°C			10	22	mA
I_{CCH-}	Supply current from V_{CC-}, high-level output					−1	−10	mA
I_{CCL+}	Supply current from V_{CC+}, low-level output	5	V_{CC+} = 13.2 V, V_{CC-} = −13.2 V, V_I = 3 V, R_L = 3 kΩ, T_A = 25°C			8	17	mA
I_{CCL-}	Supply current from V_{CC-}, low-level output					−9	−20	mA

NOTE 2: The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic levels only, e.g., when −5 V is the maximum, the typical value is a more-negative voltage.

†All typical values are at V_{CC+} = 12 V, V_{CC-} = −12 V, T_A = 25°C.

switching characteristics, V_{CC+} = 12 V, V_{CC-} = −12 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{TLH}	Transition time, low-to-high-level output	6	C_L = 2500 pF, R_L = 3 kΩ to 7 kΩ	0.2	1.4	2	μs
t_{THL}	Transition time, high-to-low-level output			0.2	1.5	2	μs
t_{TLH}	Transition time, low-to-high-level output	6	C_L = 15 pF, R_L = 7 kΩ		40		ns
t_{THL}	Transition time, high-to-low-level output				20		ns
t_{PLH}	Propagation delay time, low-to-high-level output	6	C_L = 15 pF, R_L = 7 kΩ		60		ns
t_{PHL}	Propagation delay time, high-to-low-level output				45		ns

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PARAMETER MEASUREMENT INFORMATION

d-c test circuits‡

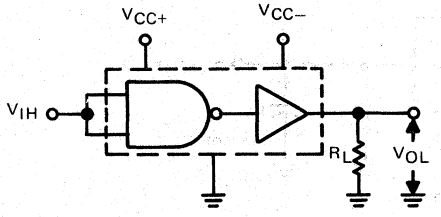
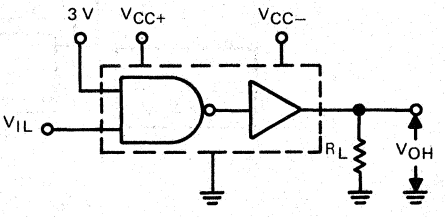
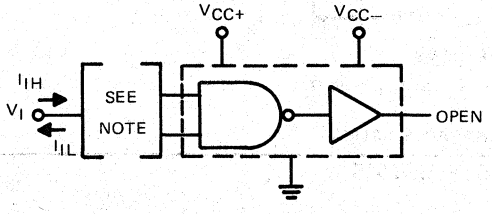


FIGURE 1–V_{IH}, V_{OL}



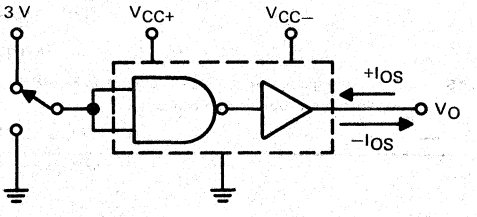
Each input is tested separately.

FIGURE 2–V_{IL}, V_{OH}



NOTE: When testing I_{IH}, the other input is at 3 V; when testing I_{IL}, the other input is open.

FIGURE 3–I_{IH}, I_{IL}



I_{OS} is tested for both input conditions at each of the specified output conditions.

FIGURE 4–I_{OS}

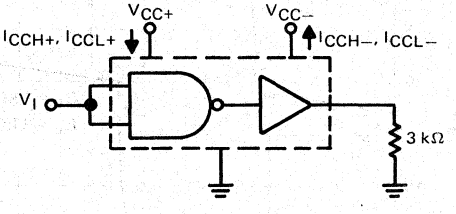
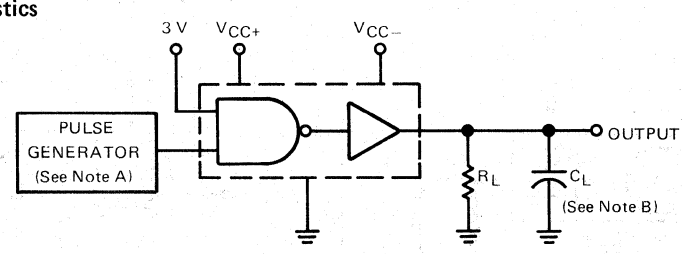


FIGURE 5–I_{CCH+}, I_{CCH-}, I_{CCL+}, I_{CCL-}

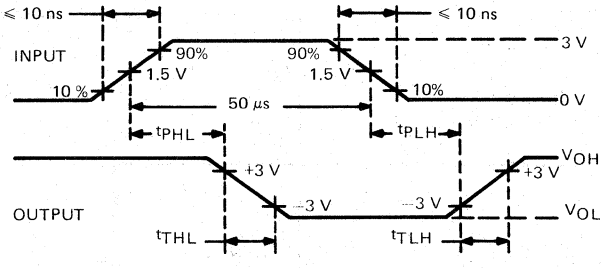
‡Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 6–SWITCHING CHARACTERISTICS

TYPICAL CHARACTERISTICS

OUTPUT CURRENT
vs
APPLIED OUTPUT VOLTAGE

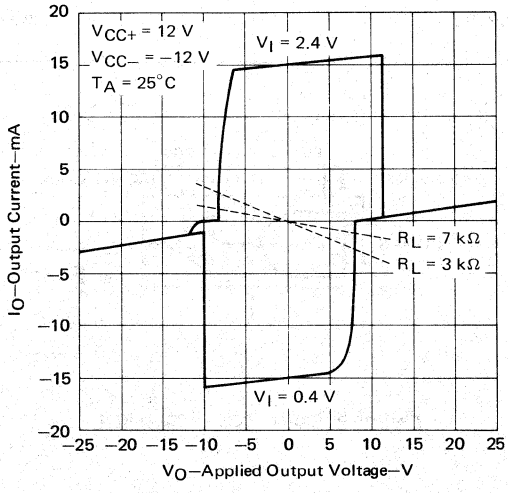


FIGURE 7

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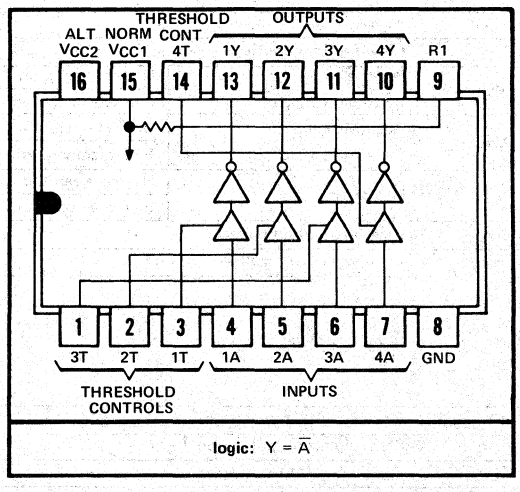
CIRCUIT TYPE SN75154
QUADRUPLE LINE RECEIVER

SATISFIES REQUIREMENTS OF EIA STANDARD RS-232-C

- Input Resistance . . . 3 kΩ to 7 kΩ over Full RS-232-C Voltage Range
- Input Threshold Adjustable to Meet "Fail-Safe" Requirements Without Using External Components
- Built-In Hysteresis for Increased Noise Immunity
- Inverting Output Compatible with DTL or TTL
- Output with Active Pull-Up for Symmetrical Switching Speeds
- Standard Supply Voltages . . . 5 V or 12 V

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



description

The SN75154 is a monolithic quadruple line receiver designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by EIA Standard RS-232C. Other applications are for relatively short, single-line, point-to-point data transmission and for level translators. Operation is normally from a single five-volt supply; however, a built-in option allows operation from a 12-volt supply without the use of additional components. The output is compatible with most TTL and DTL circuits when either supply voltage is used.

In normal operation, the threshold-control terminals are connected to the V_{CC1} terminal, pin 15, even if power is being supplied via the alternate V_{CC2} terminal, pin 16. This provides a wide hysteresis loop which is the difference between the positive-going and negative-going threshold voltages. See typical characteristics. In this mode of operation, if the input voltage goes to zero, the output voltage will remain at the low or high level as determined by the previous input.

For fail-safe operation, the threshold-control terminals are open. This reduces the hysteresis loop by causing the negative-going threshold voltage to be above zero. The positive-going threshold voltage remains above zero as it is unaffected by the disposition of the threshold terminals. In the fail-safe mode, if the input voltage goes to zero or an open-circuit condition, the output will go to the high level regardless of the previous input condition.

The SN75154 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Normal supply voltage (pin 15), V_{CC1} (see Note 1)	7 V
Alternate supply voltage (pin 16), V_{CC2} (see Note 1)	14 V
Input voltage (see Note 1)	±25 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Normal supply voltage (pin 15), V_{CC1}	4.5	5	5.5	V
Alternate supply voltage (pin 16), V_{CC2}	10.8	12	13.2	V
Input voltage			±15	V
Normalized fan-out from each output, N			10	
Operating free-air temperature, T_A	0	25	70	°C

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST FIGURE	TEST CONDITIONS	MIN	TYP‡	MAX (SEE NOTE 2)	UNIT
V_{IH}	High-level input voltage		1		3			V
V_{IL}	Low-level input voltage		1				−3	V
V_{T+}	Positive-going threshold voltage	Normal operation	1		0.8	2.2	3	V
		Fail-safe operation			0.8	2.2	3	
V_{T-}	Negative-going threshold voltage	Normal operation	1		−3	−1.1	0	V
		Fail-safe operation			0.8	1.4	3	
$V_{T+}-V_{T-}$	Hysteresis	Normal operation	1		0.8	3.3	6	V
		Fail-safe operation			0	0.8	2.2	
V_{OH}	High-level output voltage		1	I_{OH} = −400 μA	2.4	3.5		V
V_{OL}	Low-level output voltage		1	I_{OL} = 16 mA		0.23	0.4	V
r_I	Input resistance		2	ΔV_I = −25 V to −14 V	3	5	7	kΩ
				ΔV_I = −14 V to −3 V	3	5	7	
				ΔV_I = −3 V to 3 V	3	6		
				ΔV_I = 3 V to 14 V	3	5	7	
				ΔV_I = 14 V to 25 V	3	5	7	
$V_{I(open)}$	Open-circuit input voltage		3	I_I = 0	0	0.2	2	V
I_{OS}	Short-circuit output current†		4	V_{CC1} = 5.5 V, V_I = −5 V	−10	−20	−40	mA
I_{CC1}	Supply current from V_{CC1}		5	V_{CC1} = 5.5 V, T_A = 25°C		20	35	mA
I_{CC2}	Supply current from V_{CC2}			V_{CC2} = 13.2 V, T_A = 25°C		23	40	

†Not more than one output should be shorted at a time.

‡ All typical values are at V_{CC1} = 5 V, T_A = 25°C.

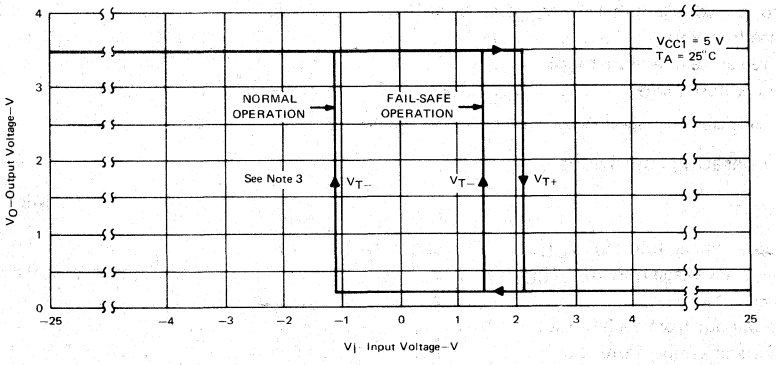
NOTE 2: The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic and threshold levels only, e.g., when −3 V is the maximum, the minimum limit is a more-negative voltage.

switching characteristics, V_{CC1} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	6	C_L = 50 pF, R_L = 390 Ω		22		ns
t_{PHL}	Propagation delay time, high-to-low-level output				20		ns
t_{TLH}	Transition time, low-to-high-level output				9		ns
t_{THL}	Transition time, high-to-low-level output				6		ns

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE vs INPUT VOLTAGE



NOTE 3: For normal operation, the threshold controls are connected to V_{CC1}, pin 15. For fail-safe operation, the threshold controls are open.

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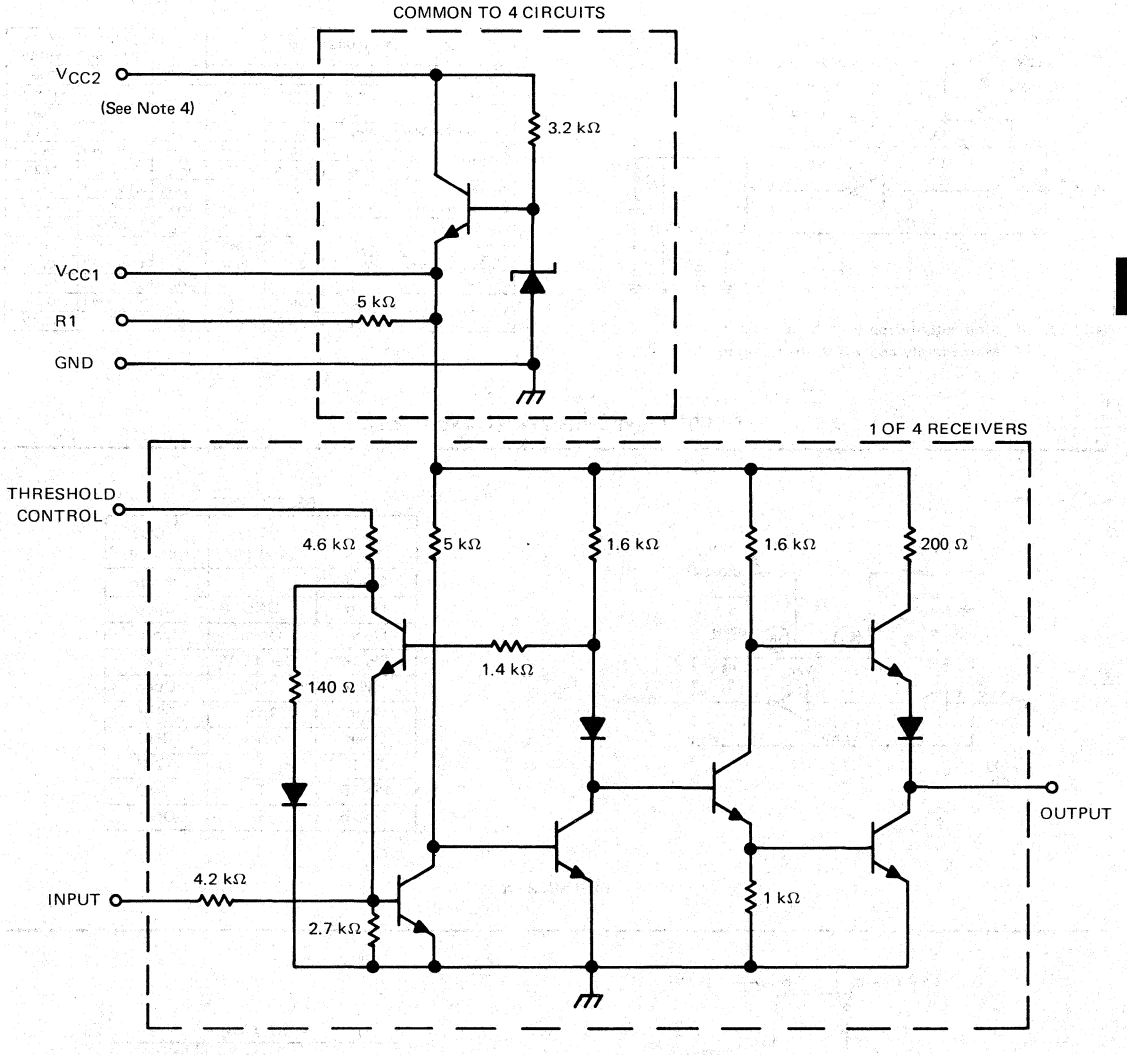
schematic



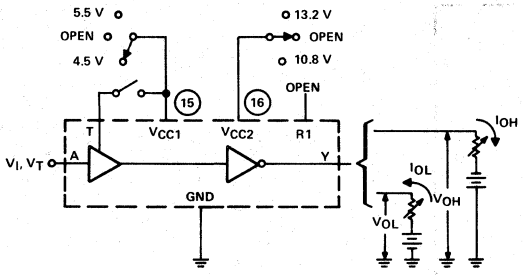
Component values shown are nominal

. . . Substrate

NOTE 4: When using V_{CC1} (pin 15), V_{CC2} (pin 16) may be left open or shorted to V_{CC1}. When using V_{CC2}, V_{CC1} must be left open or connected to the threshold control pins.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits†

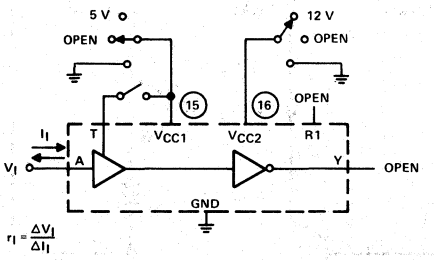


NOTES: A. Momentarily apply −5 V, then 0.8 V.
B. Momentarily apply 5 V, then ground.

TEST TABLE

TEST	MEASURE	A	T	Y	V_{CC1} (PIN 15)	V_{CC2} (PIN 16)
Open-circuit input (fail safe)	V_{OH}	Open	Open	I_{OH}	4.5 V	Open
	V_{OH}	Open	Open	I_{OH}	Open	10.8 V
V_{T+} min, V_{T-} min (fail safe)	V_{OH}	0.8 V	Open	I_{OH}	5.5 V	Open
	V_{OH}	0.8 V	Open	I_{OH}	Open	13.2 V
V_{T+} min (normal)	V_{OH}	Note A	Pin 15	I_{OH}	5.5 V and T	Open
	V_{OH}	Note A	Pin 15	I_{OH}	T	13.2 V
V_{IL} max, V_{T-} min (normal)	V_{OH}	−3 V	Pin 15	I_{OH}	5.5 V and T	Open
	V_{OH}	−3 V	Pin 15	I_{OH}	T	13.2 V
V_{IH} min, V_{T+} max, V_{T-} max (fail safe)	V_{OL}	3 V	Open	I_{OL}	4.5 V	Open
	V_{OL}	3 V	Open	I_{OL}	Open	10.8 V
V_{IH} min, V_{T+} max (normal)	V_{OL}	3 V	Pin 15	I_{OL}	4.5 V and T	Open
	V_{OL}	3 V	Pin 15	I_{OL}	T	10.8 V
V_{T-} max (normal)	V_{OL}	Note B	Pin 15	I_{OL}	5.5 V and T	Open
	V_{OL}	Note B	Pin 15	I_{OL}	T	13.2 V

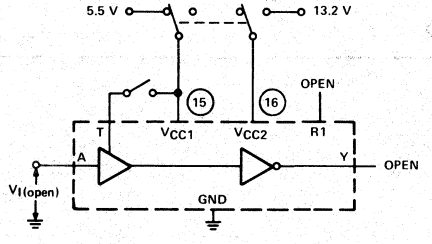
FIGURE 1 – V_{IH}, V_{IL}, V_{T+}, V_{T-}, V_{OH}, V_{OL}



TEST TABLE

T	V_{CC1} (PIN 15)	V_{CC2} (PIN 16)
Open	5 V	Open
Open	GND	Open
Open	Open	Open
Pin 15	T and 5 V	Open
GND	GND	Open
Open	Open	12 V
Open	Open	GND
Pin 15	T	12 V
Pin 15	T	GND
Pin 15	T	Open

FIGURE 2–r_I



TEST TABLE

T	V_{CC1} (PIN 15)	V_{CC2} (PIN 16)
Open	5.5 V	Open
Pin 15	5.5 V	Open
Open	Open	13.2 V
Pin 15	T	13.2 V

FIGURE 3–$V_{I(open)}$

† Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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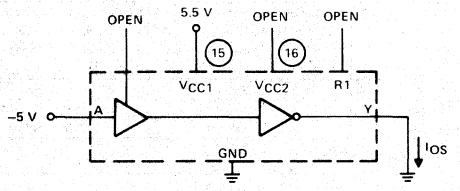
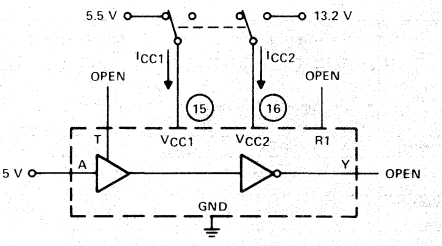
PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



Each output is tested separately.

FIGURE 4–I_{OS}



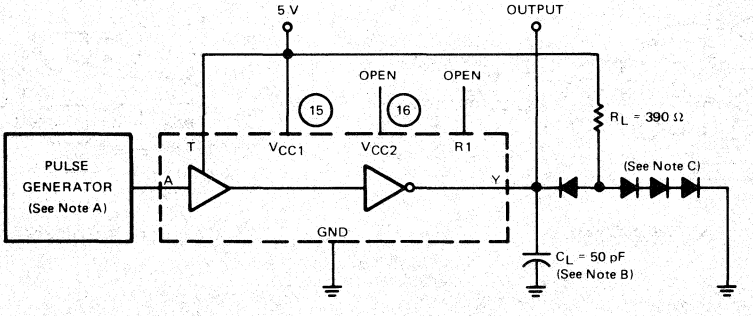
All four line receivers are tested simultaneously.

FIGURE 5–I_{CC}

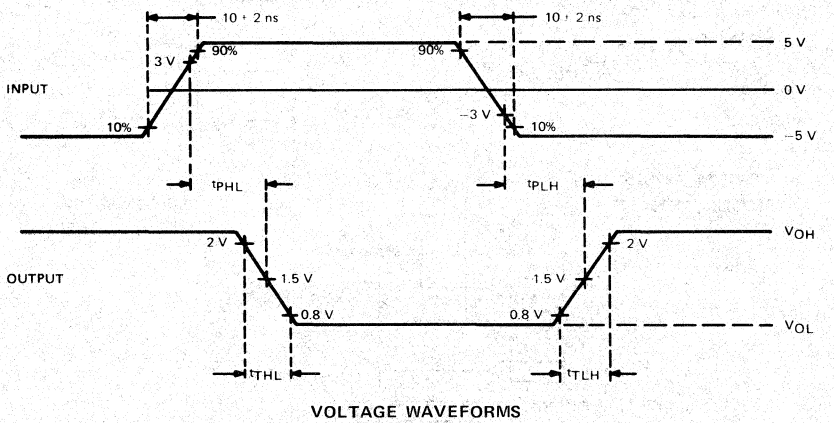
†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

3

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

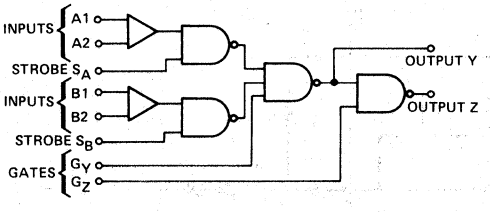
NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, t_w = 200 ns, duty cycle ≤ 20%.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.

FIGURE 6–SWITCHING TIMES

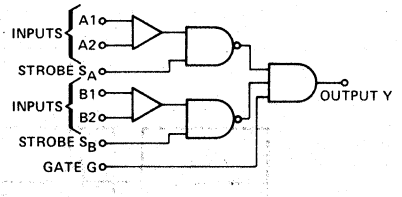
SENSE AMPLIFIER SELECTION GUIDE

TYPE	SN7520, SN7521	SN7522, SN7523	SN7524, SN7525 SN75234, SN75235†	SN7526, SN7527	SN7528, SN7529 SN75238, SN75239†
Features	• Provide Memory Data Register • Complementary Outputs	• Open-Collector Output Stage • High Fan-Out	• Dual Sense Channels • Independent Strobes	• Complete Memory Data Function • Effective Strobe Width of Less than 10 ns	• Test Points for Strobe Timing Adjustment • Dual Sense Channels
Packages	J, N	J, N	J, N	J, N	J, N
Applications	Large Memories	Large Memories	General Purpose Sense Amplifiers	High-Performance Sense Amplifiers	General Purpose Sense Amplifiers
Application Notes	CA-101: Operating and Use of Series 7520N Sense Amplifiers				

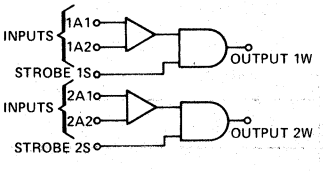
3 block diagrams



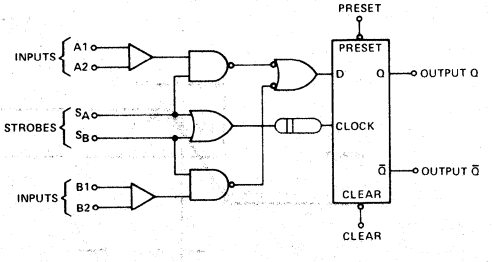
SN7520, SN7521



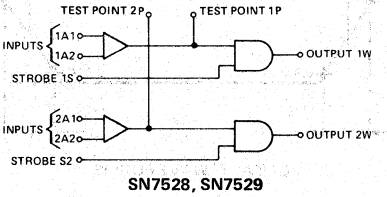
SN7522, SN7523



SN7524, SN7525
SN75234, SN75234†



SN7526, SN7527



SN7528, SN7529
SN75238, SN75239†

†Types SN75234, SN75235, SN75238, and SN75239 are indentical to types SN7524, SN7525, SN7528, and SN7529, respectively, except that an additional stage has been added to the output gate to provide an inverted output.

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HIGH-SPEED SENSE AMPLIFIERS FOR CONVERSION OF COINCIDENT-CURRENT MEMORY READOUT TO SATURATED DIGITAL-LOGIC LEVELS

performance features

- high speed and fast recovery time
- time and amplitude signal discrimination
- adjustable input threshold voltage levels
- narrow region of threshold voltage uncertainty
- multiple differential-input preamplifiers
- high d-c noise margin—typically one volt
- good fan-out capability

ease-of-design features

- choice of output circuit function
- TTL or DTL drive capability
- standard logic supply voltages
- plug-in configuration ideal for flow-soldering techniques
- pins on 100-mil grid spacings for industrial-type circuit boards

description

Series 7520 monolithic sense amplifiers are designed for use with high-speed memory systems. These sense amplifiers detect bipolar differential-input signals from the memory and provide the interface circuitry between the memory and the logic section. Low-level pulses originating in the memory are transformed into logic levels compatible with standard transistor-transistor-logic (TTL) and diode-transistor-logic (DTL) circuits.

These sense amplifiers feature multiple, differential-input preamplifiers and versatile gating and output circuits, permitting a significant reduction in the circuitry required to accomplish the sensing function. A unique circuit design provides inherent stability of the input threshold level over a wide range of power-supply voltage levels and temperature ranges. Independent strobing of each of the dual sense-input channels ensures maximum versatility and permits detection to occur when the signal-to-noise ratio is at a maximum. The gate and strobe inputs and the outputs are compatible with standard TTL and DTL digital logic circuits.

The SN7520 and SN7521 circuits may be used to perform the functions of a flip-flop or register which responds to the sense and strobe input conditions.

The SN7522 and SN7523 circuits feature a high-fan-out, single-ended, open-collector output stage. In addition, they may be used to expand the inputs to an SN7520 or SN7521 circuit, or to perform the wired-AND function.

The SN7524 and SN7525 circuits provide for independent, dual-channel sensing with separate outputs.

The SN7526 and SN7527 circuits have a D-type flip-flop output with external clear and preset inputs.

The SN7528 and SN7529 circuits are similar to the SN7524 and SN7525 except that the output of each preamplifier is available as a test point.

CONTENTS

design characteristics

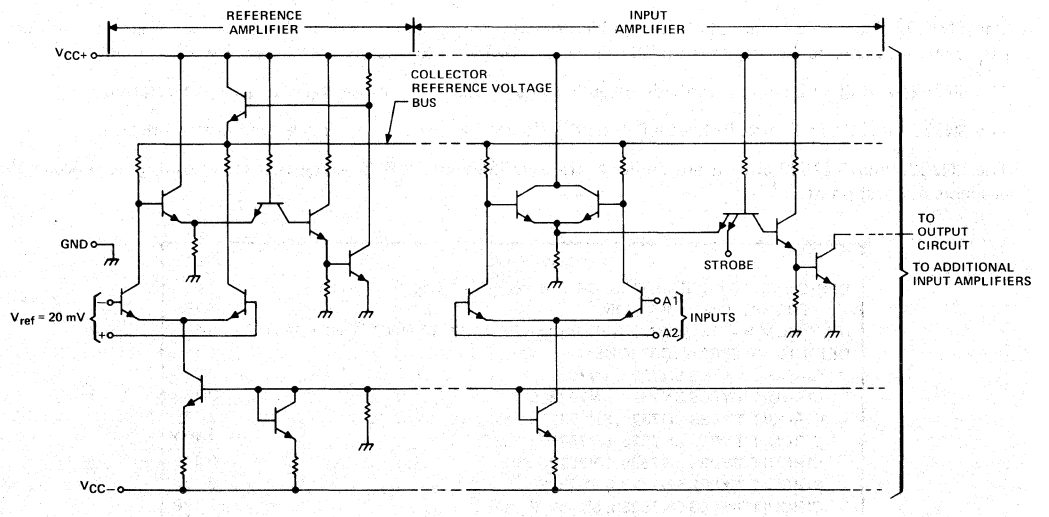
Series 7520 sense amplifiers are completely d-c coupled. Previous designs have resulted in circuits in which the threshold level could not be closely controlled because they were highly sensitive to changes in the d-c levels throughout the amplifier. This was due primarily to the required tolerances on the absolute value of resistors and the resistor temperature coefficients. The "matched-amplifier" design of Series 7520 circuits depends on resistor ratios rather than absolute values. In this design, excellent stability of the threshold level can be maintained despite component variations and changes in bias levels. The capability of multiple-input amplifiers increases the versatility of the design.

The basic circuit is used to implement several sense amplifier designs. Additional logic circuitry is added to the strobe-gate output to provide versatile sensing functions. The outputs of two or more input amplifiers can be combined to implement multiple-input amplifiers, a function not previously available in integrated form. The d-c coupled design eliminates many of the problems associated with overload recovery time and threshold shift (with high input repetition rates) usually encountered in sense amplifier designs that use reactive coupling components.

circuit operation

The basic Series 7520 sense amplifier strobe and threshold circuit is shown in Figure A. The design uses a "matched-amplifier" concept which takes advantage of the inherent excellent component matching and thermal tracking characteristics of monolithic integrated circuits. A reference amplifier is used to generate the collector reference voltage which is distributed to the input amplifiers. Application of an external reference voltage, V_{ref}, establishes the input-amplifier threshold voltage level, V_T. The design is such that there is 1:1 correspondence between the applied reference voltage, V_{ref}, and the nominal threshold voltage level, V_T. The reference and input amplifiers use identical circuit configurations; therefore, changes in bias levels introduced into the input amplifier, through changes in temperature or power-supply voltage levels, are compensated by similar changes in the reference amplifier.

The collector reference voltage, supplied by the reference amplifier, can be used to control the threshold-voltage level of more than one input amplifier, thereby establishing equal threshold levels to all of the input sense channels simultaneously.



Patent pending

FIGURE A—BASIC SERIES 7520 SENSE-AMPLIFIER CIRCUIT

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circuit operation (continued)

The second stage of the input amplifier is a TTL gate. The gate provides the threshold action for the input sense channel and provides a convenient point in the circuit to accomplish the strobe function. The differential-input sense signal switches the output of the TTL gate only when the strobe input voltage is higher than the logic input threshold voltage. The strobe input, therefore, provides the sense amplifier with the capability of time discrimination, allowing the input signal to be detected when the signal-to-noise ratio is at a maximum.

The logic inputs (i.e., gate and strobe) of Series 7520 sense amplifiers are designed to be compatible with Series 74 TTL digital integrated circuits. The multiple-emitter transistors are utilized to provide inherent switching-time advantages over other saturated-logic schemes. The same guaranteed noise margin and logic threshold voltage as for Series 74 are assured each of the gate and strobe inputs. This is accomplished by testing each logic input under standard Series 74 test conditions, i.e., 2 volts for high-level input condition and 0.8 volt for low-level input conditions. Since the guaranteed minimum high-level output voltage is 2.4 volts and the guaranteed maximum low-level output voltage is 0.4 volt, a minimum noise margin of 0.4 volt is assured at each input.

SN7520 and SN7521 circuit

This circuit is a dual-channel sense amplifier with the preamplifiers connected to a common output stage and a complementary output stage. The output circuit is composed of two cascaded NAND gates, each with external gate inputs. External connection of the Z output and the G_Y input results in a flip-flop or register that is set by signals at the differential-input terminals. Reset of the register is performed at the G_Z input. Capacitive coupling from output Z to G_Y results in output pulse stretching. In either connection, complementary output levels are available. The gate and strobe inputs and the outputs are compatible with standard TTL logic. The input function of SN7520/SN7521 can be expanded by connecting the Y output of SN7522/SN7523 to the G_Y input of the circuit being expanded.

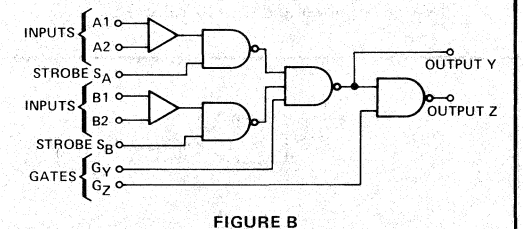

FIGURE B
SN7520/SN7521 LOGIC DIAGRAM

logic: $Y = \overline{G}_Y + A \cdot S_A + B \cdot S_B$
$Z = \overline{G}_Z + \overline{Y}$
$Z = \overline{G}_Z + G_Y (\overline{A} + \overline{S}_A)(\overline{B} + \overline{S}_B)$

SN7520 and SN7521 circuit (continued)

SN7522 and SN7523 circuit

This circuit is a dual-channel sense amplifier with the preamplifiers connected to a common output stage. The output circuit features an open-collector output which permits two or more of these outputs to be connected in the wire-AND configuration. Each package includes a load resistor that may be used as the output pull-up resistor. High sink-current capability is a feature of this design, and a separate ground terminal is used for the output circuitry. These devices can also be used as input expanders for the SN7520/SN7521 circuit.

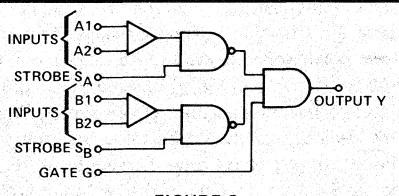

FIGURE C
SN7522/SN7523 LOGIC DIAGRAM

logic: $Y = G(\overline{A} + \overline{S}_A)(\overline{B} + \overline{S}_B)$

SN7524 and SN7525 circuit

This circuit features two completely independent sense amplifiers in a single package. Each channel features high fan-out capability.

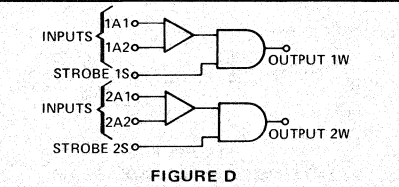

FIGURE D
SN7524/SN7525 LOGIC DIAGRAM
SN75234/SN75235 SAME EXCEPT INVERTED OUTPUT

logic: W = AS for SN7524 and SN7525
W = $\overline{AS}$ for SN75234 and SN75235

SN7526 and SN7527 circuit

This circuit is a dual-channel sense amplifier with the preamplifiers connected to a D-type flip-flop with external clear and preset inputs. A delay between the strobe input terminals and the clock input of the flip-flop ensures that data is set up at the D input of the flip-flop prior to clocking.

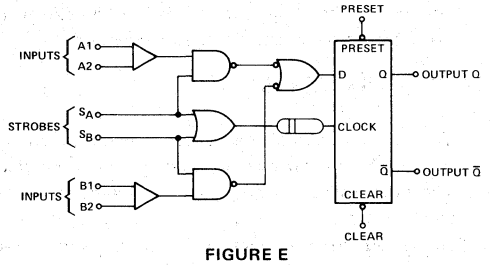

FIGURE E
SN7526/SN7527 LOGIC DIAGRAM

logic: See truth table on page 14.

SN7528 and SN7529 circuit

This circuit features two separate single-preamplifier sense amplifiers in a single package. The output of each preamplifier is available as a test point. These test points can be used to observe the amplified core signal to facilitate accurate strobe timing. When using this device, care should be taken to avoid coupling the strobe signal or other stray signals to the test point. Excessive loading of the test point is also to be avoided. The result of either coupling or loading will be a change in the threshold voltage of the device. The output circuit of each channel features a simple TTL gate configuration with a high fan-out capability.

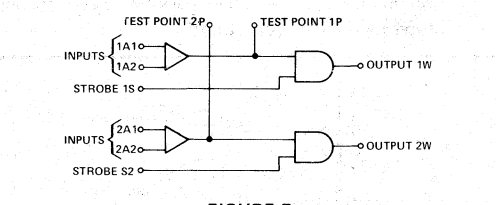

FIGURE F
SN7528/SN7529 LOGIC DIAGRAM
SN75238/SN75239 SAME EXCEPT INVERTED OUTPUT

logic: W = AS for SN7528 and SN7529
W = $\overline{AS}$ for SN75238 and SN75239

SN75234, SN75235, SN75238, SN75239 circuits

These dual sense amplifier circuits are the same as SN7524, SN7525, SN7528, and SN7529, respectively, except that an additional stage has been added to the output gate to provide an inverted output. Compared to using a separate gate for inversion, not only is package count reduced, but less propagation delay is added.

reference voltage considerations

These sense amplifiers feature a variable-threshold voltage level with simultaneous adjustment of both sense channels or both sense amplifiers by a single reference voltage. The operating threshold voltage level of the input amplifiers is established by and is approximately equal to the applied reference input voltage, V_{ref}. Several methods may be used to supply this reference voltage; however, methods given here will be limited to the discussion of fundamental design considerations. These sense amplifiers are recommended for use in systems requiring threshold voltage levels of ±15 to ±40 mV.

A simple method of generating the reference voltage is the use of a resistor voltage divider from either the positive (V_{CC+}) or negative (V_{CC-}) voltage supplies. See Figure G. This type of voltage divider may be used to supply an individual reference amplifier or to supply a number of paralleled reference amplifiers. The bias current required at the reference amplifier input is low (nominally 30 μA); therefore, voltage dividers of this type may normally be operated with very low current requirements. In noisy environments, the use of a filter capacitor across the inputs is recommended. By locating the capacitor as close to the device terminals as possible, noise and stray signals will be presented common-mode to the reference amplifier and thus be rejected.

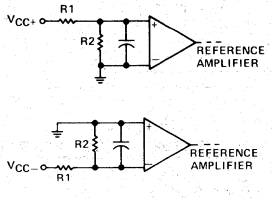

FIGURE G

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input line layout considerations

Input sensitivity and device speed require adequate precautions in the routing of signal input and reference lines to prevent noise pickup. Bypassing of supply and reference inputs at the device with low-inductance disc ceramic capacitors, and use of a good ground plane to separate strobe and output lines from sense and reference input lines, is recommended.

sense-input termination resistor considerations

Termination resistors are intentionally omitted from the sense-input terminals so the designer may select resistor values which will be compatible with the particular application. Matched termination resistors, (R_T, Figure H), normally in the range of 25 Ω to 200 Ω each, are required not only to terminate the sense line in a desired impedance but also to provide a d-c path for the sense-input bias currents. Careful matching of the resistor pairs should be observed or effective common-mode rejection will be reduced.

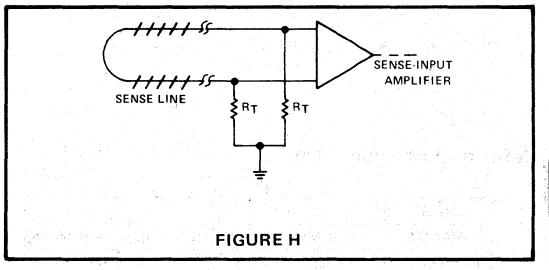


FIGURE H

3

output drive capability

The output circuits of these sense amplifiers feature the ability to sink or supply load current, This capability permits direct use with both TTL- and DTL-type loads. The open-collector output of the SN7522/SN7523 circuit may be connected to similar outputs to perform the wire-AND function. Load currents (out of the output terminal) are specified as negative values. Arrows on the d-c test circuit indicate the actual direction of current flow.

logic input current requirements

Logic input current requirements are specified at worst-case power-supply conditions over the operating free-air temperature range of 0°C to 70°C. The logic input currents are identical to and compatible with Series 74 TTL digital integrated circuits. Each logic input of the multiple-emitter input transistors requires no more than a 1.6-mA flow out of the input at a low logic level. Each input emitter requires current into the input when it is at a high-logic level. This current is 40 μA maximum. Currents into the input terminals are specified as positive values. Arrows on the d-c test circuits indicate the actual direction of current flow.

absolute maximum ratings (over free-air temperature range unless otherwise noted)

Supply voltages (see Note 1)
- V_{CC+} . . . . . 7 V
- V_{CC-} . . . . . −7 V

Differential input voltage, V_{ID} or V_{ref} . . . . . ±5 V
Voltage from any input to ground (see Note 2) . . . . . 5.5 V
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . −55°C to 150°C

recommended operating conditions

	MIN	NOM	MAX	UNIT
V_{CC+} (see Note 1)	4.75	5	5.25	V
V_{CC-} (see Note 1)	−4.75	−5	−5.25	V
V_{ref}	15		40	mV

NOTES: 1. These voltage values are with respect to network ground terminal.
2. Strobe and gate input voltages must be zero or positive with respect to network ground terminal.

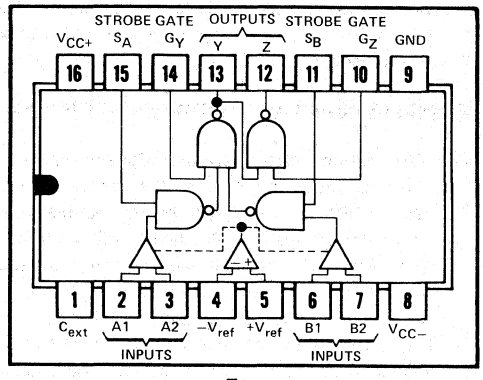
CIRCUIT TYPES SN7520,SN7521
DUAL-CHANNEL SENSE AMPLIFIERS WITH COMPLEMENTARY OUTPUTS

TRUTH TABLE

INPUTS						OUTPUTS	
A	B	G_Y	G_Z	S_A	S_B	Y	Z
X	X	L	X	X	X	H	$\overline{G}_Z$
H	X	X	X	H	X	H	$\overline{G}_Z$
X	H	X	X	X	H	H	$\overline{G}_Z$
L	L	H	X	X	X	L	H
L	X	H	X	X	L	L	H
X	L	H	X	L	X	L	H
X	X	H	X	L	L	L	H
X	X	X	L	X	X	X	H

J OR N

DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{G}_Y + A \cdot S_A + B \cdot S_B$

$Z = \overline{G}_Z + \overline{Y}$

$Z = \overline{G}_Z + G_Y(\overline{A} + \overline{S}_A)(\overline{B} + \overline{S}_B)$

3

definition of logic levels

INPUT	H	L	X
A or B†	$V_{ID} \geqslant V_T$ max	$V_{ID} \leqslant V_T$ min	Irrelevant
Any G or S	$V_I \geqslant V_{IH}$ min	$V_I \leqslant V_{IL}$ max	Irrelevant

†A and B are differential voltages (V_{ID}) between A1 and A2 or B1 and B2, respectively. For these circuits, V_{ID} is considered positive regardless of which terminal of each pair is positive with respect to the other.

electrical characteristics (unless otherwise noted V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 0°C to 70°C)

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_T	Differential input threshold voltage (see Note 3, page 17)	1	V_{ref} = 15 mV	SN7520	11	15	19	mV
				SN7521	8	15	22	
			V_{ref} = 40 mV	SN7520	36	40	44	
				SN7521	33	40	47	
V_{ICF}	Common-mode input firing voltage (see Note 4, page 17)	none	V_{ref} = 40 mV, $V_{I(S)} = V_{IH}$ *Common-mode input pulse:* $t_r \leqslant 15$ ns, $t_f \leqslant 15$ ns, t_w = 50 ns			±2.5		V
I_{IB}	Differential-input bias current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0			30	75	μA
I_{IO}	Differential-input offset current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0			0.5		μA
V_{IH}	High-level input voltage (strobe and gate inputs)	3			2			V
V_{IL}	Low-level input voltage (strobe and gate inputs)	3					0.8	V
V_{OH}	High-level output voltage	3	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, I_{OH} = −400 μA		2.4	4		V
V_{OL}	Low-level output voltage	3	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, I_{OL} = 16 mA			0.25	0.4	V
I_{IH}	High-level input current (strobe and gate inputs)	4	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 2.4 V				40	μA
			V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 5.25 V				1	mA
I_{IL}	Low-level input current (strobe and gate inputs)	4	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IL} = 0.4 V			−1	−1.6	mA
$I_{OS(Y)}$	Short-circuit output current into Y	5	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V		−3		−5	mA
$I_{OS(Z)}$	Short-circuit output current into Z	5	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V		−2.1		−3.5	mA
I_{CC+}	Supply current from V_{CC+}	6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25°C			28	40	mA
I_{CC-}	Supply current from V_{CC-}	6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25°C			−14	−20	mA

‡All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.

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switching characteristics, V_{CC+} = 5 V, V_{CC-} = −5 V, $C_{ext} \geq$ 100 pF, T_A = 25°C

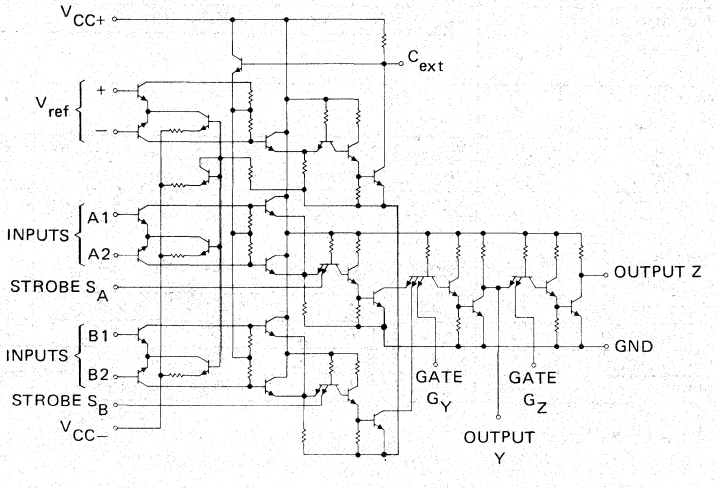
PROPAGATION DELAY TIMES			TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYMBOL	FROM INPUT	TO OUTPUT						
$t_{PLH(DY)}$	A1-A2 OR B1-B2	Y	32	C_L = 15 pF, R_L = 288 Ω		25	40	ns
$t_{PHL(DY)}$						20		
$t_{PLH(DZ)}$	A1-A2 OR B1-B2	Z	32	C_L = 15 pF, R_L = 288 Ω		30		ns
$t_{PHL(DZ)}$						35	55	
$t_{PLH(SY)}$	STROBE A OR B	Y	32	C_L = 15 pF, R_L = 288 Ω		15	30	ns
$t_{PHL(SY)}$						20		
$t_{PLH(SZ)}$	STROBE A OR B	Z	32	C_L = 15 pF, R_L = 288 Ω		30		ns
$t_{PHL(SZ)}$						35	55	
$t_{PLH(GY, Y)}$	GATE G_Y	Y	33	C_L = 15 pF, R_L = 288 Ω		15	25	ns
$t_{PHL(GY, Y)}$						10		
$t_{PLH(GY, Z)}$	GATE G_Y	Z	33	C_L = 15 pF, R_L = 288 Ω		15		ns
$t_{PHL(GY, Z)}$						20	30	
$t_{PLH(GZ, Z)}$	GATE G_Z	Z	34	C_L = 15 pF, R_L = 288 Ω		15		ns
$t_{PHL(GZ, Z)}$						10	20	

typical recovery and cycle times, V_{CC+} = 5 V, V_{CC-} = −5 V, $C_{ext} \geq$ 100 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{orD}	Differential-input overload recovery time (see Note 5)	*Differential Input Pulse:* V_{ID} = 2 V, $t_r = t_f$ = 20 ns		20		ns
t_{orC}	Common-mode-input overload recovery (see Note 6)	*Common-Mode Input Pulse:* V_{IC} = ±2 V, $t_r = t_f$ = 20 ns		20		ns
$t_{cyc(min)}$	Minimum cycle time			200		ns

NOTES: 5. Differential-input overload recovery time is the time necessary for the device to recover from the specified differential-input-overload signal prior to the strobe-enable signal.
6. Common-mode-input overload recovery time is the time necessary for the device to recover from the specified common-mode-input overload signal prior to the strobe-enable signal.

schematic

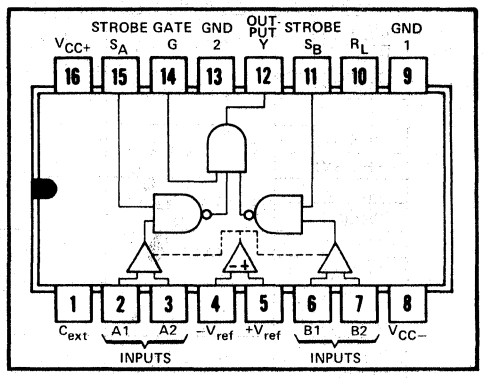


CIRCUIT TYPES SN7522, SN7523
DUAL-CHANNEL SENSE AMPLIFIERS

TRUTH TABLE

INPUTS					OUTPUT
A	B	G	S_A	S_B	Y
L	L	H	X	X	H
L	X	H	X	L	H
X	L	H	L	X	H
X	X	H	L	L	H
X	X	L	X	X	L
H	X	X	H	X	L
X	H	X	X	H	L

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = G(\overline{A} + \overline{S}_A)(\overline{B} + \overline{S}_B)$

definition of logic levels

INPUT	H	L	X
A or B†	$V_{ID} \geq V_T$ max	$V_{ID} \leq V_T$ min	Irrelevant
Any G or S	$V_I \geq V_{IH}$ min	$V_I \leq V_{IL}$ max	Irrelevant

†A and B are differential voltages (V_{ID}) between A1 and A2 or B1 and B2, respectively. For these circuits, V_{ID} is considered positive regardless of which terminal of each pair is positive with respect to the other.

electrical characteristics (unless otherwise noted $V_{CC+} = 5$ V, $V_{CC-} = -5$ V, $T_A = 0°C$ to $70°C$)

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_T	Differential input threshold voltage (see Note 3, page 17)	7	V_{ref} = 15 mV	SN7522	11	15	19	mV
				SN7523	8	15	22	
			V_{ref} = 40 mV	SN7522	36	40	44	
				SN7523	33	40	47	
V_{ICF}	Common-mode input firing voltage (see Note 4, page 17)	none	V_{ref} = 40 mV, $V_{I(S)} = V_{IH}$ *Common-mode input pulse:* $t_r \leq 15$ ns, $t_f \leq 15$ ns, $t_w = 50$ ns			±2.5		V
I_{IB}	Differential-input bias current	2	$V_{CC+} = 5.25$ V, $V_{CC-} = -5.25$ V, $V_{ID} = 0$			30	75	μA
I_{IO}	Differential-input offset current	2	$V_{CC+} = 5.25$ V, $V_{CC-} = -5.25$ V, $V_{ID} = 0$			0.5		μA
V_{IH}	High-level input voltage (strobe and gate inputs)	8			2			V
V_{IL}	Low-level input voltage (strobe and gate inputs)	8					0.8	V
V_{OH}	High-level output voltage	8	$V_{CC+} = 4.75$ V, $V_{CC-} = -4.75$ V, $I_{OH} = -400$ μA		2.4	4		V
V_{OL}	Low-level output voltage	8	$V_{CC+} = 4.75$ V, $V_{CC-} = -4.75$ V, $I_{OL} = 16$ mA			0.25	0.4	V
I_{IH}	High-level input current (strobe and gate inputs)	9	$V_{CC+} = 5.25$ V, $V_{CC-} = -5.25$ V, $V_{IH} = 2.4$ V				40	μA
			$V_{CC+} = 5.25$ V, $V_{CC-} = -5.25$ V, $V_{IH} = 5.25$ V				1	mA
I_{IL}	Low-level input current (strobe and gate inputs)	9	$V_{CC+} = 5.25$ V, $V_{CC-} = -5.25$ V, $V_{IL} = 0.4$ V			−1	−1.6	mA
I_{OH}	High-level output current	10	$V_{CC+} = 4.75$ V, $V_{CC-} = -4.75$ V, $V_O = 5.25$ V				250	μA
I_{OS}	Short-circuit output current	11	$V_{CC+} = 5.25$ V, $V_{CC-} = -5.25$ V		−2.1		−3.5	mA
I_{CC+}	Supply current from V_{CC+}	6	$V_{CC+} = 5.25$ V, $V_{CC-} = -5.25$ V, $T_A = 25°C$			27	40	mA
I_{CC-}	Supply current from V_{CC-}	6	$V_{CC+} = 5.25$ V, $V_{CC-} = -5.25$ V, $T_A = 25°C$			−15	−20	mA

‡All typical values are at $V_{CC+} = 5$ V, $V_{CC-} = -5$ V, $T_A = 25°C$.

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switching characteristics, V_{CC+} = 5 V, V_{CC-} = −5 V, $C_{ext} \geq$ 100 pF, T_A = 25°C

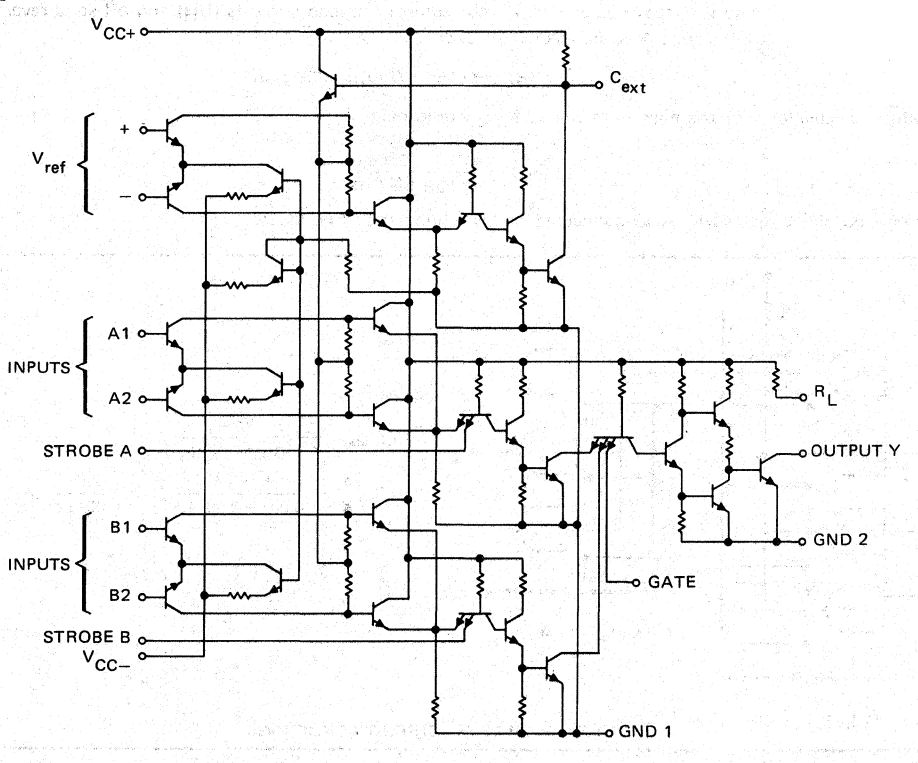
PROPAGATION DELAY TIMES			TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYMBOL	FROM INPUT	TO OUTPUT						
$t_{PLH(D)}$	A1-A2 OR B1-B2	Y	35	C_L = 15 pF, R_L = 288 Ω		20		ns
$t_{PHL(D)}$						30	45	
$t_{PLH(S)}$	STROBE A OR B	Y	35	C_L = 15 pF, R_L = 288 Ω		20		ns
$t_{PHL(S)}$						20	40	
$t_{PLH(G)}$	GATE	Y	36	C_L = 15 pF, R_L = 288 Ω		10		ns
$t_{PHL(G)}$						15	25	

typical recovery and cycle times, V_{CC+} = 5 V, V_{CC-} = −5 V, $C_{ext} \geq$ 100 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{orD}	Differential-input overload recovery time (see Note 5)	*Differential Input Pulse:* V_{ID} = 2 V, $t_r = t_f$ = 20 ns		20		ns
t_{orC}	Common-mode-input overload recovery (see Note 6)	*Common-Mode Input Pulse:* V_{IC} = ±2 V, $t_r = t_f$ = 20 ns		20		ns
$t_{cyc(min)}$	Minimum cycle time			200		ns

NOTES: 5. Differential-input overload recovery time is the time necessary for the device to recover from the specified differential input-overload signal prior to the strobe-enable signal.
6. Common-mode-input overload recovery time is the time necessary for the device to recover from the specified common-mode-input overload signal prior to the strobe-enable signal.

schematic



APPLICATION DATA

combined fan-out and wire-AND capabilities

The open-collector TTL gate, when supplied with a proper load resistor (R_L), may be paralleled with other similar TTL gates to perform the wire-AND function, and simultaneously, will drive from one to nine Series 54/74 loads. When no other open-collector gates are paralleled, this gate may be used to drive ten Series 54/74 loads. For any of these conditions an appropriate load resistor value must be determined for the desired circuit configuration. A maximum resistor value must be determined which will ensure that sufficient load current (to TTL loads) and off current (through paralleled outputs) will be available while the output is high. A minimum resistor value must be determined which will ensure that current through this resistor and sink current from the TTL loads will not cause the output voltage to rise above the low level even if one of the paralleled outputs is sinking all the current.

In both conditions (low and high level) the value of R_L is determined by:

$$R_L = \frac{V_{RL}}{I_{RL}}$$

where V_{RL} is the voltage drop in volts, and I_{RL} is the current in amperes.

high-level (off-state) circuit calculations (see figure I)

The allowable voltage drop across the load resistor (V_{RL}) is the difference between V_{CC} applied and the V_{OH} level required at the load:

$$V_{RL} = V_{CC} - V_{OH\ min}$$

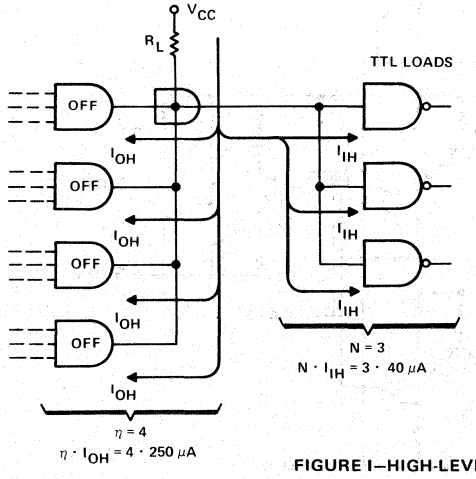
The total current through the load resistor (I_{RL}) is the sum of the load currents (I_{IH}) and off-state reverse currents (I_{OH}) through each of the wire-AND-connected outputs:

$$I_{RL} = \eta \cdot I_{OH} + N \cdot I_{IH} \text{ to TTL loads}$$

Therefore, calculations for the maximum value of R_L would be:

$$R_{L(max)} = \frac{V_{CC} - V_{OH\ min}}{\eta \cdot I_{OH} + N \cdot I_{IH}}$$

where η = number of gates wire-AND-connected, and N = number of TTL loads.



Calculation:

$$R_{L(max)} = \frac{V_{CC} - V_{OH\ min}}{\eta \cdot I_{OH} + N \cdot I_{IH}}$$

$$R_{L(max)} = \frac{5 - 2.4}{0.001 + 0.00012}\ \Omega = \frac{2.6}{0.00112}\ \Omega = 2321\ \Omega$$

FIGURE I—HIGH-LEVEL CIRCUIT CONDITIONS

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APPLICATION DATA

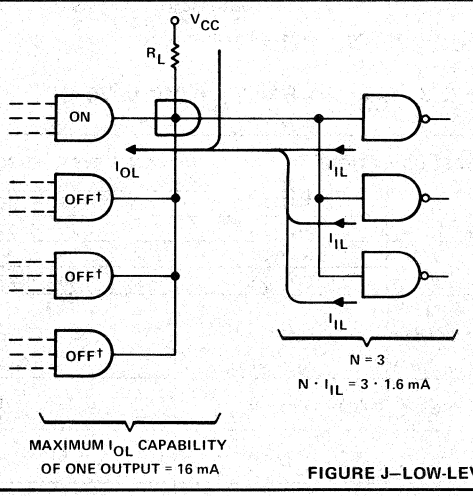
low-level (on-state) circuit calculations (see figure J)

The current through the resistor must be limited to the maximum sink-current of one output transistor. Note that if several output transistors are wire-AND connected, the current through R_L may be shared by those paralleled transistors. However, unless it can be absolutely guaranteed that more than one transistor will be on during low-level periods, the current must be limited to 16 mA, the maximum current which will ensure a low-level maximum of 0.4 volt.

Also, fan-out must be considered. Part of the 16 mA will be supplied from the inputs which are being driven. This reduces the amount of current which can be allowed through R_L.

Therefore, the equation used to determine the minimum value of R_L would be:

$$R_{L(min)} = \frac{V_{CC} - V_{OL\ max}}{I_{OL\ capability} - N \cdot I_{IL}}$$



Calculation:

$$R_{L(min)} = \frac{V_{CC} - V_{OL\ max}}{I_{OL\ capability} - N \cdot I_{OL}}$$

$$R_{L(min)} = \frac{5 - 0.4}{0.016 - 0.0048}\ \Omega = \frac{4.6}{0.0112}\ \Omega = 410\ \Omega$$

†Current into OFF outputs is negligible at the low logic level.

FIGURE J—LOW-LEVEL CIRCUIT CONDITIONS

driving series 54/74 loads and combining outputs

Table 1 provides minimum and maximum resistor values, calculated from equations shown above, for driving one to ten Series 54/74 loads and wire-AND connecting two to seven parallel outputs. Each value shown for one wire-AND output is determined by the fan-out plus the cutoff current of a single output transistor. Extension beyond seven wire-AND connections is permitted with fan-outs of seven or less if a valid minimum and maximum R_L is possible. When fanning-out to ten Series 54/74 loads, the calculation for the minimum value of R_L indicates that an infinite resistance should be used ($V_{RL} \div 0 = \infty$); however, the use of a 4-kΩ resistor in this case will satisfy the high-level condition and limit the low level to less than 0.43 volt.

TABLE 1

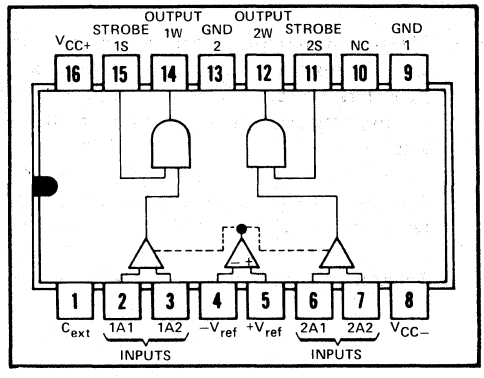
FAN-OUT TO TTL LOADS	WIRE-AND OUTPUTS							
	1	2	3	4	5	6	7	1 to 7
1	8965	4814	3291	2500	2015	1688	1452	319
2	7878	4482	3132	2407	1954	1645	1420	359
3	7027	4193	2988	2321	1897	1604	1390	410
4	6341	3939	2857	2241	1843	1566	1361	479
5	5777	3714	2736	2166	1793	1529	1333	575
6	5306	3513	2626	2096	1744	1494	1306	718
7	4905	3333	2524	2031	1699	1460	1280	958
8	4561	3170	2429	1969	1656	X	X	1437
9	4262	3023	X	X	X	X	X	2875
10	4000	X	X	X	X	X	X	4000§
	MAXIMUM							MIN
	LOAD RESISTOR VALUE IN OHMS							

‡—All values shown in the table are based on:
High-level conditions: $V_{CC} = 5$ V, $V_{OH\ min} = 2.4$ V
Low-level conditions: $V_{CC} = 5$ V, $V_{OL\ max} = 0.4$ V
X—Not recommended or not possible.
§—The theoretical value is ∞. See explanation in text.

TRUTH TABLE

INPUTS A	INPUTS S	OUTPUT W
H	H	H
L	X	L
X	L	L

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: W = AS

NC—No internal connection

definition of logic levels

INPUT	H	L	X
A†	$V_{ID} \geq V_T$ max	$V_{ID} \leq V_T$ min	Irrelevant
S	$V_I \geq V_{IH}$ min	$V_I \leq V_{IL}$ max	Irrelevant

†A is a differential voltage (V_{ID}) between A1 and A2. For these circuits, V_{ID} is considered positive regardless of which terminal is positive with respect to the other.

electrical characteristics (unless otherwise noted $V_{CC+} = 5$ V, $V_{CC-} = -5$ V, $T_A = 0°C$ to $70°C$)

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_T	Differential-input threshold voltage (see Note 3, page 17)	12	V_{ref} = 15 mV	SN7524	11	15	19	mV
				SN7525	8	15	22	
			V_{ref} = 40 mV	SN7524	36	40	44	
				SN7525	33	40	47	
V_{ICF}	Common-mode input firing voltage (see Note 4, page 17)	none	V_{ref} = 40 mV, $V_{I(S)} = V_{IH}$ *Common-Mode Input Pulse:* $t_r \leq 15$ ns, $t_f \leq 15$ ns, $t_w = 50$ ns			±2.5		V
I_{IB}	Differential-input bias current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0			30	75	μA
I_{IO}	Differential-input offset current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0			0.5		μA
V_{IH}	High-level input voltage (strobe inputs)	13			2			V
V_{IL}	Low-level input voltage (strobe inputs)	13					0.8	V
V_{OH}	High-level output voltage	13	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, I_{OH} = −400 μA		2.4	4		V
V_{OL}	Low-level output voltage	13	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, I_{OL} = 16 mA			0.25	0.4	V
I_{IH}	High-level input current (strobe inputs)	14	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 2.4 V				40	μA
			V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 5.25 V				1	mA
I_{IL}	Low-level input current (strobe inputs)	14	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IL} = 0.4 V			−1	−1.6	mA
I_{OS}	Short-circuit output current	15	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V		−2.1		−3.5	mA
I_{CC+}	Supply current from V_{CC+}	6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25°C			25	40	mA
I_{CC-}	Supply current from V_{CC-}	6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25°C			−15	−20	mA

‡All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.

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switching characteristics, V_{CC+} = 5 V, V_{CC-} = −5 V, $C_{ext} \geq$ 100 pF, T_A = 25°C

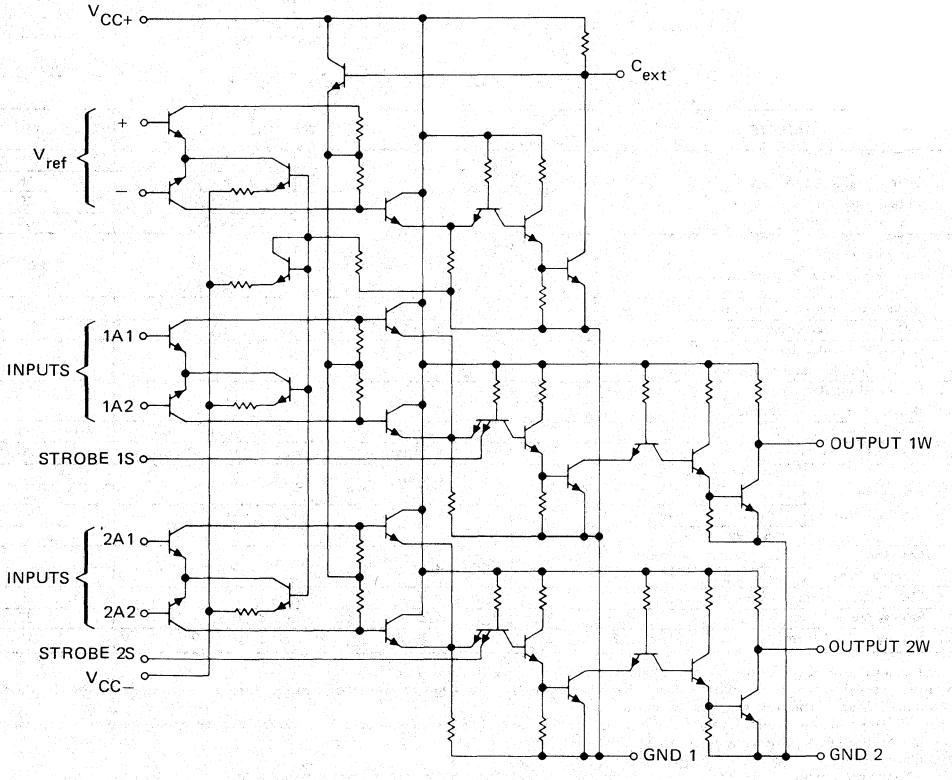
PROPAGATION DELAY TIMES			TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYMBOL	FROM INPUT	TO OUTPUT						
$t_{PLH(D)}$	A1–A2	W	37	C_L = 15 pF, R_L = 288 Ω		25	40	ns
$t_{PHL(D)}$						20		
$t_{PLH(S)}$	STROBE	W	37	C_L = 15 pF, R_L = 288 Ω		15	30	ns
$t_{PHL(S)}$						20		

typical recovery and cycle times, V_{CC+} = 5 V, V_{CC-} = −5 V, $C_{ext} \geq$ 100 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{orD}	Differential-input overload recovery time (see Note 5)	*Differential Input Pulse:* V_{ID} = 2 V, $t_r = t_f$ = 20 ns		20		ns
t_{orC}	Common-mode-input overload recovery time (see Note 6)	*Common-Mode Input Pulse:* V_{IC} = ±2 V, $t_r = t_f$ = 20 ns		20		ns
$t_{cyc(min)}$	Minimum cycle time			200		ns

NOTES: 5. Differential-input overload recovery time is the time necessary for the device to recover from the specified differential-input-overload signal prior to the strobe-enable signal.
6. Common-mode-input overload recovery time is the time necessary for the device to recover from the specified common-mode-input overload signal prior to the strobe-enable signal.

schematic



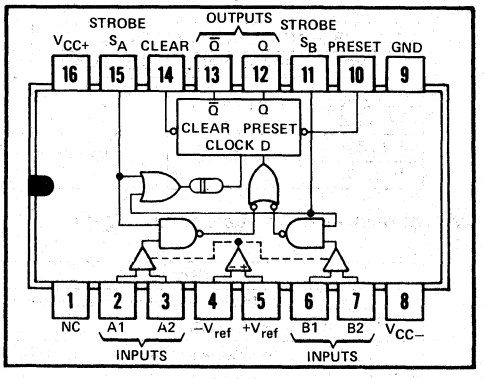
CIRCUIT TYPES SN7526, SN7527
DUAL-CHANNEL SENSE AMPLIFIERS WITH OUTPUT DATA REGISTERS

TRUTH TABLE

INPUTS AT TIME OF STROBE TRANSITION				OUTPUTS	
A	B	S_A	S_B	Q	$\overline{Q}$
H	X	↑	L	H	L
H	X	↑	↑	H	L
X	H	L	↑	H	L
X	H	↑	↑	H	L
L	L	↑	↑	L	H
L	X	↑	L	L	H
X	L	L	↑	L	H
X	X	H	↑	No Change	
X	X	↑	H	No Change	

NOTES: A. H = high level (steady state), L = low level (steady state), ↑ = transition from low level to high level, X = irrelevant.
B. Information at the inputs is transferred to the outputs on the positive-going edge of the strobe pulse.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: Low input to preset sets Q to high level.
Low input to clear resets Q to low level.
Preset and clear dominate all other inputs.

NC—No internal connection

definition of logic levels

INPUT	H	L
A or B†	$V_{ID} \geqslant V_T$ max	$V_{ID} \leqslant V_T$ min
S_A or S_B	$V_I \geqslant V_{IH}$ min	$V_I \leqslant V_{IL}$ max

†A and B are differential voltages (V_{ID}) between A1 and A2 or B1 and B2, respectively. For these circuits, V_{ID} is considered positive regardless of which terminal of each pair is positive with respect to the other.

recommended operating conditions¶

	MIN	MAX	UNIT
Width of clear or preset pulse, t_w	30		ns
Width of strobe pulse, t_w	30		ns
Input setup time, t_{setup}◇	20		ns
Input hold time, t_{hold}□	5		ns

electrical characteristics (unless otherwise noted V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 0°C to 70°C)

PARAMETER			TEST FIGURE	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_T	Differential input threshold voltage (see Note 3, page 17)		16	V_{ref} = 15 mV	SN7526	11	15	19	mV
					SN7527	8	15	22	
				V_{ref} = 40 mV	SN7526	36	40	44	
					SN7527	33	40	47	
V_{ICF}	Common-mode input firing voltage (see Note 4, page 17)		none	V_{ref} = 40 mV, $V_{I(S)} = V_{IH}$ *Common-Mode Input Pulse:* $t_r \leqslant 15$ ns, $t_f \leqslant 15$ ns, t_w = 50 ns			±2.5		V
I_{IB}	Differential input bias current		2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0			30	75	μA
I_{IO}	Differential-input offset current		2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0			0.5		μA
V_{IH}	High-level input voltage at strobe, preset, and clear inputs		17			2			V
V_{IL}	Low-level input voltage at strobe, preset, and clear inputs		17					0.8	V
V_{OH}	High-level output voltage		17	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, I_{OH} = −400 μA		2.4	3.6		V
V_{OL}	Low-level output voltage		17	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, I_{OL} = 16 mA			0.26	0.4	V
I_{IH}	High-level input current	clear and strobe inputs	19	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 2.4 V				80	μA
		preset input						120	
		clear and strobe inputs	19	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 5.25 V				2	mA
		preset input						3	
I_{IL}	Low-level input current	clear and strobe inputs	19	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IL} = 0.4 V			−2	−3.2	mA
		preset input					−3	−4.8	
I_{OS}	Short-circuit output current§		18	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V		−18		−57	mA
I_{CC+}	Supply current from V_{CC+}		6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25°C			27	40	mA
I_{CC-}	Supply current from V_{CC-}		6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25°C			−10	−20	mA

¶These are in addition to the conditions on Page 5. See waveforms in Figure 30.
◇Setup time is the interval immediately preceding the positive-going edge of the strobe pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.
□Hold time is the interval immediately following the positive-going edge of the strobe pulse during which interval the data to be recognized must be maintained at the input to ensure its continued recognition.
‡All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

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switching characteristics, V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C

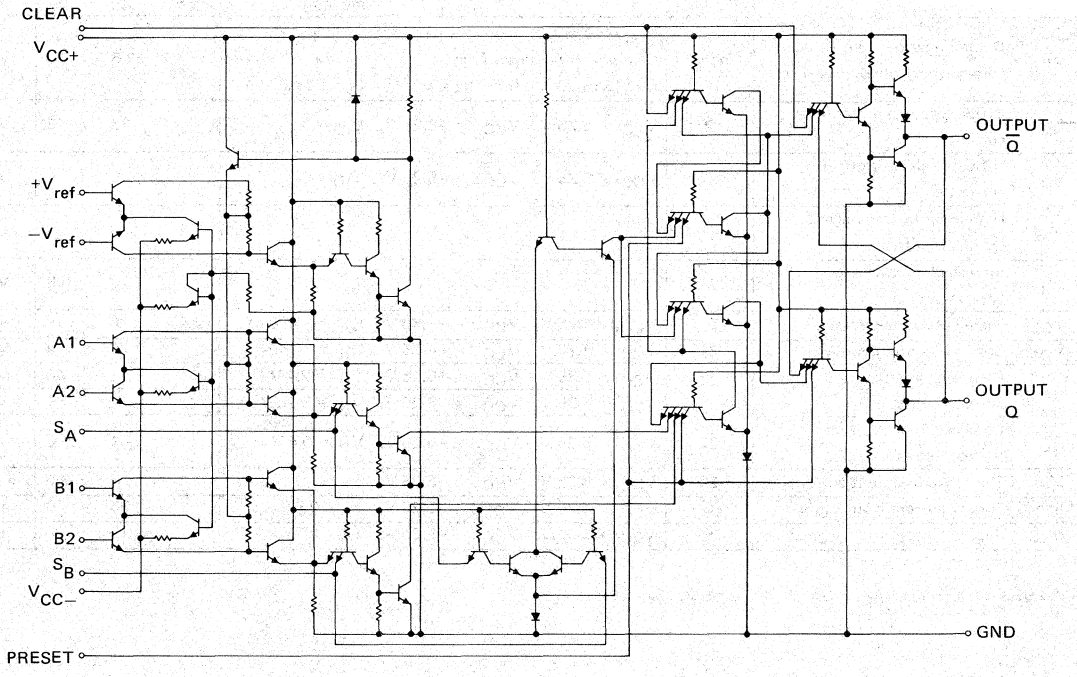
PROPAGATION DELAY TIMES			TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYMBOL	FROM INPUT	TO OUTPUT						
$t_{PLH}(SQ)$	STROBE S_A or S_B	Q	38	C_L = 15 pF, R_L = 288 Ω		25	45	ns
$t_{PHL}(SQ)$						30	45	
$t_{PLH}(S\bar{Q})$	STROBE S_A or S_B	$\bar{Q}$	38	C_L = 15 pF, R_L = 288 Ω		25	45	ns
$t_{PHL}(S\bar{Q})$						30	45	
$t_{PLH}(CQ)$	CLEAR	$\bar{Q}$	38	C_L = 15 pF, R_L = 288 Ω		15	25	ns
$t_{PHL}(CQ)$		Q				20	40	
$t_{PLH}(PQ)$	PRESET	Q	38	C_L = 15 pF, R_L = 288 Ω		15	25	ns
$t_{PHL}(P\bar{Q})$		$\bar{Q}$				20	40	

typical recovery and cycle times, V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{orD}	Differential-input overload recovery time (see Note 5)	*Differential Input Pulse:* V_{ID} = 2 V, $t_r = t_f$ = 20 ns		20		ns
t_{orC}	Common-mode-input overload recovery time (see Note 6)	*Common-Mode Input Pulse:* V_{IC} = ±2 V, $t_r = t_f$ = 20 ns		20		ns
$t_{cyc(min)}$	Minimum cycle time			200		ns

NOTES: 5. Differential-input overload recovery time is the time necessary for the device to recover from the specified differential-input-overload signal prior to the strobe-enable signal.
6. Common-mode-input overload recovery time is the time necessary for the device to recover from the specified common mode input overload signal prior to the strobe-enable signal.

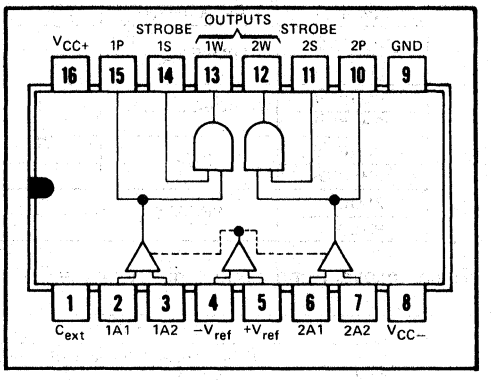
schematic



TRUTH TABLE

INPUTS A	INPUTS S	OUTPUT W
H	H	H
L	X	L
X	L	L

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: W = AS

definition of logic levels

INPUT	H	L	X
A†	$V_{ID} \geq V_{T\ max}$	$V_{ID} \leq V_{T\ min}$	Irrelevant
S	$V_I \geq V_{IH\ min}$	$V_I \leq V_{IL\ max}$	Irrelevant

†A is a differential voltage (V_{ID}) between A1 and A2. For these circuits, V_{ID} is considered positive regardless of which terminal is positive with respect to the other.

3

electrical characteristics (unless otherwise noted V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 0°C to 70°C)

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_T	Differential-input threshold voltage (see Note 3, page 17)	20	V_{ref} = 15 mV	SN7528	11	15	19	mV
				SN7529	8	15	22	
			V_{ref} = 40 mV	SN7528	36	40	44	
				SN7529	33	40	47	
V_{ICF}	Common-mode input firing voltage (see Note 4, page 17)	none	V_{ref} = 40 mV, $V_{I(S)} = V_{IH}$ *Common-Mode Input Pulse:* $t_r \leq 15$ ns, $t_f \leq 15$ ns, t_w = 50 ns			±2.5		V
I_{IB}	Differential-input bias current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0			30	75	μA
I_{IO}	Differential-input offset current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0			0.5		μA
V_{IH}	High-level input voltage (strobe inputs)	21			2			V
V_{IL}	Low-level input voltage (strobe inputs)	21					0.8	V
V_{OH}	High-level output voltage	21	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, I_{OH} = −400 μA		2.4	4		V
V_{OL}	Low-level output voltage	21	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, I_{OL} = 16 mA			0.25	0.4	V
I_{IH}	High-level input current (strobe inputs)	22	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 2.4 V				40	μA
			V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 5.25 V				1	mA
I_{IL}	Low-level input current (strobe inputs)	22	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IL} = 0.4 V			−1	−1.6	mA
I_{OS}	Short-circuit output current	23	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V		−2.1		−3.5	mA
I_{CC+}	Supply current from V_{CC+}	6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25°C			25	40	mA
I_{CC-}	Supply current from V_{CC-}	6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25°C			−15	−20	mA

‡All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.

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switching characteristics, V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C

PROPAGATION DELAY TIMES			TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYMBOL	FROM INPUT	TO OUTPUT						
$t_{PLH(D)}$	A1–A2	W	39	C_L = 15 pF, R_L = 288 Ω		25	40	ns
$t_{PHL(D)}$						20		ns
$t_{PLH(S)}$	STROBE	W	39	C_L = 15 pF, R_L = 288 Ω		15	30	ns
$t_{PHL(S)}$						20		ns

typical recovery and cycle times, V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{orD}	Differential-input overload recovery time (see Note 5)	*Differential Input Pulse:* V_{ID} = 2 V, t_f = 20 ns		20		ns
t_{orC}	Common-mode-input overload recovery time (see Note 6)	*Common-Mode Input Pulse:* V_{IC} = ±2 V, $t_r = t_f$ = 20 ns		20		ns
$t_{cyc(min)}$	Minimum cycle time			200		ns

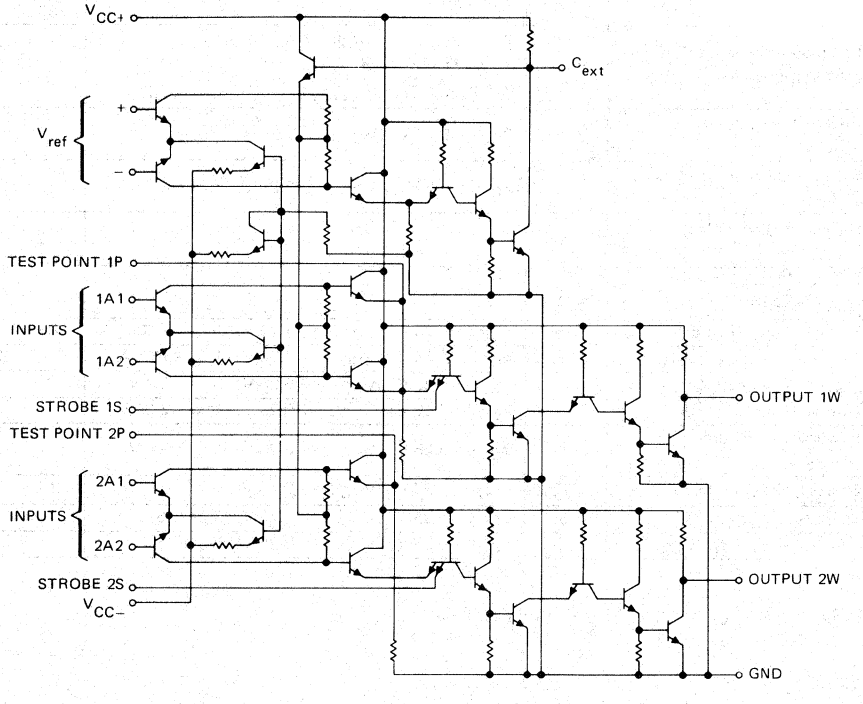
NOTES: 3. The differential-input threshold voltage (V_T) is defined as the d-c differential-input voltage (V_{ID}) required to force the output of the sense amplifier to the logic gate threshold voltage level.

4. Common-mode input firing voltage is the minimum common-mode voltage that will exceed the dynamic range of the input at the specified conditions and cause the logic output to switch. The specified common-mode input signal is applied with a strobe-enable present.

5. Differential-input overload recovery time is the time necessary for the device to recover from the specified differential-input overload signal prior to the strobe-enable signal.

6. Common-mode-input overload recovery time is the time necessary for the device to recover from the specified common-mode-input overload signal prior to the strobe-enable signal.

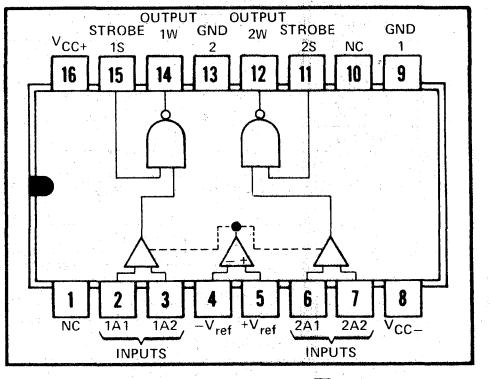
schematic



TRUTH TABLE

INPUTS		OUTPUT
A	S	W
H	H	L
L	X	H
X	L	H

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $W = \overline{AS}$

NC—No internal connection

definition of logic levels

INPUT	H	L	X
A†	$V_{ID} \geq V_{T\ max}$	$V_{ID} \leq V_{T\ min}$	Irrelevant
S	$V_I \geq V_{IH\ min}$	$V_I \leq V_{IL\ max}$	Irrelevant

†A is a differential voltage (V_{ID}) between A1 and A2. For these circuits, V_{ID} is considered positive regardless of which terminal is positive with respect to the other.

3

electrical characteristics (unless otherwise noted $V_{CC+} = 5$ V, $V_{CC-} = -5$ V, $T_A = 0°C$ to $70°C$)

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_T	Differential-input threshold voltage (see Note 3, page 17)	24	V_{ref} = 15 mV	SN75234	11	15	19	mV
				SN75235	8	15	22	
			V_{ref} = 40 mV	SN75234	36	40	44	
				SN75235	33	40	47	
V_{ICF}	Common-mode input firing voltage (see Note 4, page 17)	none	V_{ref} = 40 mV, $V_{I(S)} = V_{IH}$ *Common-Mode Input Pulse:* $t_r \leq 15$ ns, $t_f \leq 15$ ns, $t_w = 50$ ns			±2.5		V
I_{IB}	Differential-input bias current	2	$V_{CC+} = 5.25$ V, $V_{CC-} = -5.25$ V, $V_{ID} = 0$			30	75	μA
I_{IO}	Differential-input offset current	2	$V_{CC+} = 5.25$ V, $V_{CC-} = -5.25$ V, $V_{ID} = 0$			0.5		μA
V_{IH}	High-level input voltage (strobe inputs)	25			2			V
V_{IL}	Low-level input voltage (strobe inputs)	25					0.8	V
V_{OH}	High-level output voltage	25	$V_{CC+} = 4.75$ V, $V_{CC-} = -4.75$ V, $I_{OH} = -400$ μA		2.4	4		V
V_{OL}	Low-level output voltage	25	$V_{CC+} = 4.75$ V, $V_{CC-} = -4.75$ V, $I_{OL} = 16$ mA			0.25	0.4	V
I_{IH}	High-level input current (strobe inputs)	26	$V_{CC+} = 5.25$ V, $V_{CC-} = -5.25$ V, $V_{IH} = 2.4$ V				40	μA
			$V_{CC+} = 5.25$ V, $V_{CC-} = -5.25$ V, $V_{IH} = 5.25$ V				1	mA
I_{IL}	Low-level input current (strobe inputs)	26	$V_{CC+} = 5.25$ V, $V_{CC-} = -5.25$ V, $V_{IL} = 0.4$ V			−1	−1.6	mA
I_{OS}	Short-circuit output current	27	$V_{CC+} = 5.25$ V, $V_{CC-} = -5.25$ V		−2.1		−3.5	mA
I_{CC+}	Supply current from V_{CC+}	6	$V_{CC+} = 5.25$ V, $V_{CC-} = -5.25$ V, $T_A = 25°C$			25	40	mA
I_{CC-}	Supply current from V_{CC-}	6	$V_{CC+} = 5.25$ V, $V_{CC-} = -5.25$ V, $T_A = 25°C$			−15	−20	mA

‡All typical values are at $V_{CC+} = 5$ V, $V_{CC-} = -5$ V, $T_A = 25°C$.

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switching characteristics, V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C

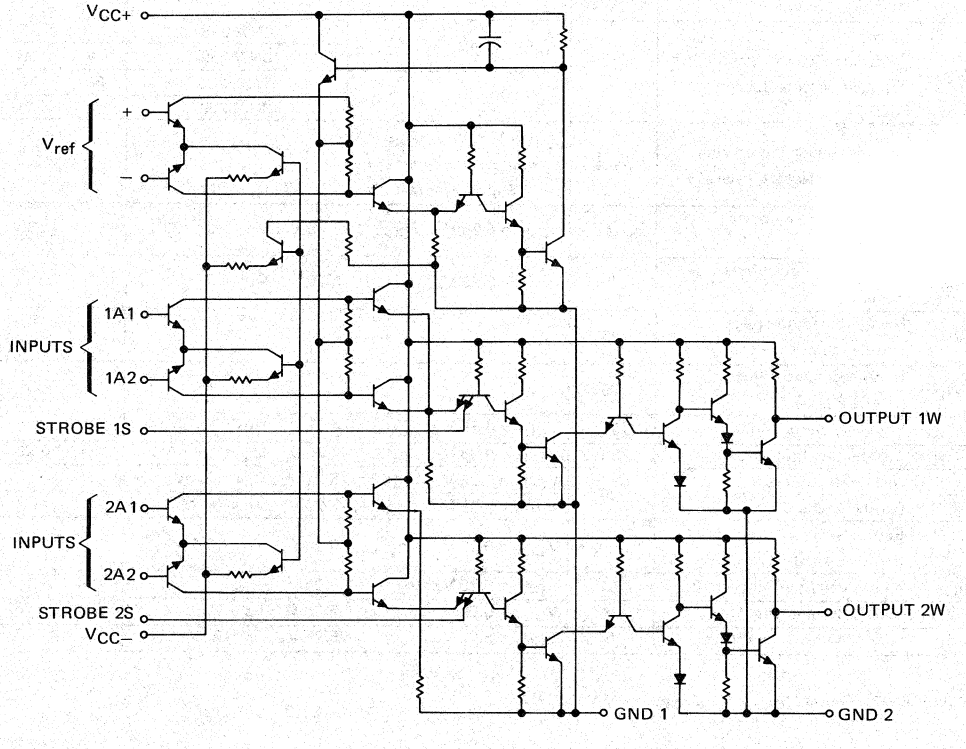
PROPAGATION DELAY TIMES			TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYMBOL	FROM INPUT	TO OUTPUT						
$t_{PLH(D)}$	A1–A2	W	40	C_L = 15 pF, R_L = 288 Ω		25		ns
$t_{PHL(D)}$						25	40	
$t_{PLH(S)}$	STROBE	W	40	C_L = 15 pF, R_L = 288 Ω		25		ns
$t_{PHL(S)}$						15	30	

typical recovery and cycle times, V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{orD}	Differential-input overload recovery time (see Note 5)	*Differential Input Pulse:* V_{ID} = 2 V, $t_r = t_f$ = 20 ns		20		ns
t_{orC}	Common-mode-input overload recovery time (see Note 6)	*Common-Mode Input Pulse:* V_{IC} = ±2 V, $t_r = t_f$ = 20 ns		20		ns
$t_{cyc(min)}$	Minimum cycle time			200		ns

NOTES: 5. Differential-input overload recovery time is the time necessary for the device to recover from the specified differential-input-overload signal prior to the strobe-enable signal.
6. Common-mode-input overload recovery time is the time necessary for the device to recover from the specified common-mode-input overload signal prior to the strobe-enable signal.

schematic

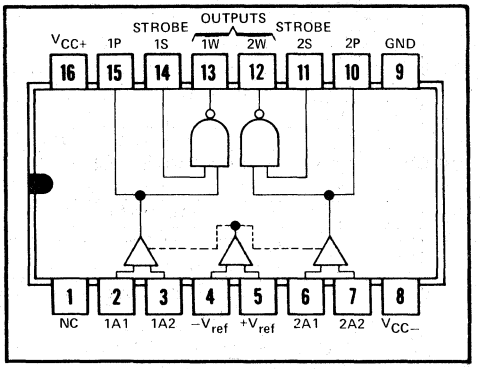


CIRCUIT TYPES SN75238, SN75239
DUAL SENSE AMPLIFIERS WITH PREAMPLIFIER TEST POINTS

TRUTH TABLE

INPUTS A	INPUTS S	OUTPUT W
H	H	L
L	X	H
X	L	H

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $W = \overline{AS}$

NC—No internal connection

definition of logic levels

INPUT	H	L	X
A†	$V_{ID} \geq V_{T\ max}$	$V_{ID} \leq V_{T\ min}$	Irrelevant
S	$V_I \geq V_{IH\ min}$	$V_I \leq V_{IL\ max}$	Irrelevant

†A is a differential voltage (V_{ID}) between A1 and A2. For these circuits, V_{ID} is considered positive regardless of which terminal is positive with respect to the other.

3

electrical characteristics (unless otherwise noted $V_{CC+} = 5$ V, $V_{CC-} = -5$ V, $T_A =$ 0°C to 70°C)

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_T	Differential-input threshold voltage (see Note 3, page 17)	28	V_{ref} = 15 mV	SN75238	11	15	19	mV
				SN75239	8	15	22	
			V_{ref} = 40 mV	SN75238	36	40	44	
				SN75239	33	40	47	
V_{ICF}	Common-mode input firing voltage (see Note 4, page 17)	none	V_{ref} = 40 mV, $V_{I(S)} = V_{IH}$ *Common-Mode Input Pulse:* $t_r \leq 15$ ns, $t_f \leq 15$ ns, $t_w = 50$ ns			±2.5		V
I_{IB}	Differential-input bias current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0			30	75	μA
I_{IO}	Differential-input offset current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0			0.5		μA
V_{IH}	High-level input voltage (strobe inputs)	29			2			V
V_{IL}	Low-level input voltage (strobe inputs)	29					0.8	V
V_{OH}	High-level output voltage	29	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, I_{OH} = −400 μA		2.4	4		V
V_{OL}	Low-level output voltage	29	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, I_{OL} = 16 mA			0.25	0.4	V
I_{IH}	High-level input current (strobe inputs)	30	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 2.4 V				40	μA
			V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 5.25 V				1	mA
I_{IL}	Low-level input current (strobe inputs)	30	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IL} = 0.4 V			−1	−1.6	mA
I_{OS}	Short-circuit output current	31	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V		−2.1		−3.5	mA
I_{CC+}	Supply current from V_{CC+}	6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25°C			25	40	mA
I_{CC-}	Supply current from V_{CC-}	6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25°C			−15	−20	mA

‡All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.

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switching characteristics, V_{CC+} = 5 V, V_{CC-} = –5 V, T_A = 25°C

PROPAGATION DELAY TIMES			TEST	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYMBOL	FROM INPUT	TO OUTPUT	FIGURE					
$t_{PLH(D)}$	A1–A2	W	41	C_L = 15 pF, R_L = 288 Ω		25		ns
$t_{PHL(D)}$						25	40	ns
$t_{PLH(S)}$	STROBE	W	41	C_L = 15 pF, R_L = 288 Ω		25		ns
$t_{PHL(S)}$						15	30	ns

typical recovery and cycle times, V_{CC+} = 5 V, V_{CC-} = –5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{orD}	Differential-input overload recovery time (see Note 5)	*Differential Input Pulse:* V_{ID} = 2 V, t_f = 20 ns		20		ns
t_{orC}	Common-mode-input overload recovery time (see Note 6)	*Common-Mode Input Pulse:* V_{IC} = ±2 V, $t_r = t_f$ = 20 ns		20		ns
$t_{cyc(min)}$	Minimum cycle time			200		ns

3

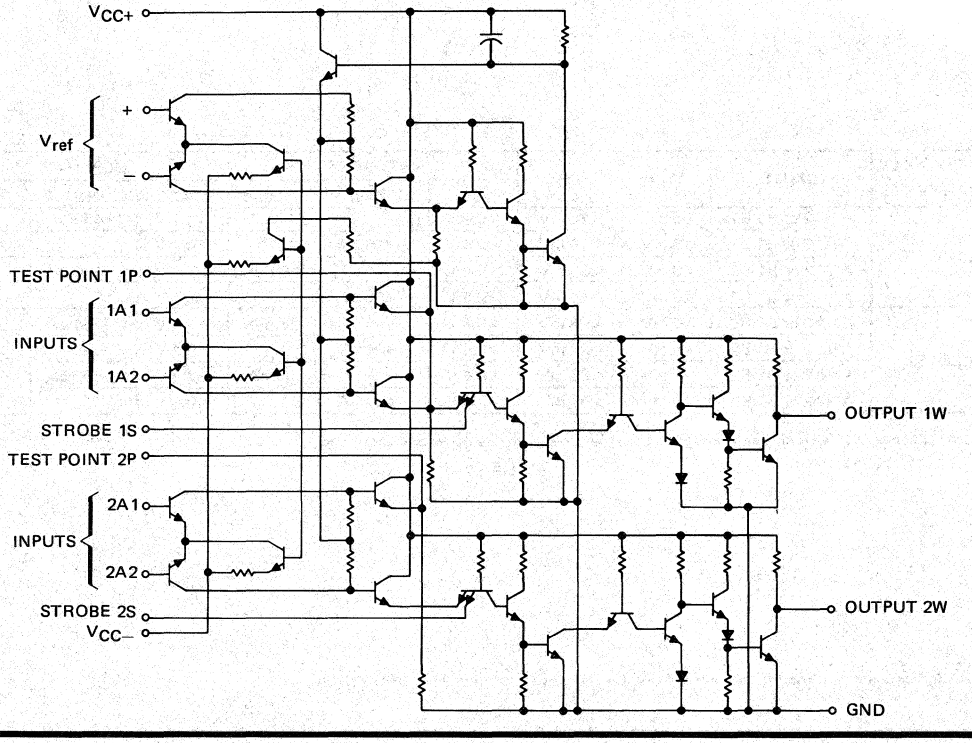
NOTES: 3. The differential-input threshold voltage (V_T) is defined as the d-c differential-input voltage (V_{ID}) required to force the output of the sense amplifier to the logic gate threshold voltage level.

4. Common-mode input firing voltage is the minimum common-mode voltage that will exceed the dynamic range of the input at the specified conditions and cause the logic output to switch. The specified common-mode input signal is applied with a strobe-enable present.

5. Differential-input overload recovery time is the time necessary for the device to recover from the specified differential-input overload signal prior to the strobe-enable signal.

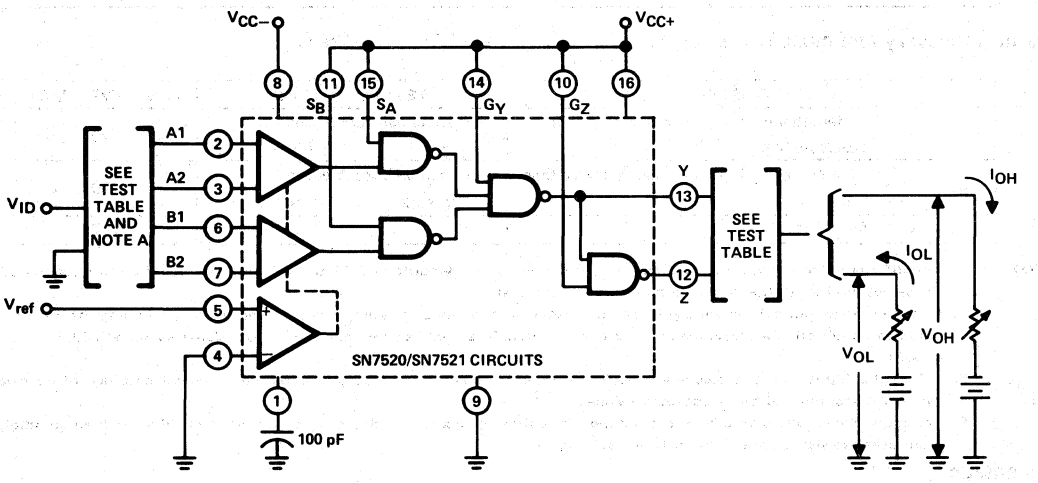
6. Common-mode-input overload recovery time is the time necessary for the device to recover from the specified common-mode-input overload signal prior to the strobe-enable signal.

schematic



PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



TEST TABLE

CIRCUIT TYPE	INPUTS	V_{ref}	V_{ID}	OUTPUT Y			OUTPUT Z		
				V_O	I_{OH}	I_{OL}	V_O	I_{OH}	I_{OL}
SN7520	A1-A2 or B1-B2	15 mV	≤11 mV	≤0.4 V		16 mA	≥2.4 V	–400 μA	
	A1-A2 or B1-B2	15 mV	≥19 mV	≥2.4 V	–400 μA		≤0.4 V		16 mA
	A1-A2 or B1-B2	40 mV	≤36 mV	≤0.4 V		16 mA	≥2.4 V	–400 μA	
	A1-A2 or B1-B2	40 mV	≥44 mV	≥2.4 V	–400 μA		≤0.4 V		16 mA
SN7521	A1-A2 or B1-B2	15 mV	≤ 8 mV	≤0.4 V		16 mA	≥2.4 V	–400 μA	
	A1-A2 or B1-B2	15 mV	≥22 mV	≥2.4 V	–400 μA		≤0.4 V		16 mA
	A1-A2 or B1-B2	40 mV	≤33 mV	≤0.4 V		16 mA	≥2.4 V	–400 μA	
	A1-A2 or B1-B2	40 mV	≥47 mV	≥2.4 V	–400 μA		≤0.4 V		16 mA

NOTE A: Each pair of differential inputs is tested separately with the other pair grounded.

FIGURE 1–V_T

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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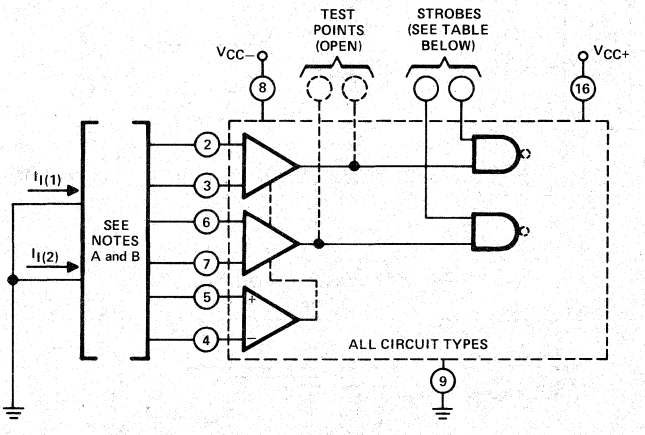
PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



NOTES: A. Each preamplifier is tested separately. Inputs not under test are grounded.
B. $I_{IB} = I_{I(1)}$ and/or $I_{I(2)}$; $I_{IO} = I_{I(1)} - I_{I(2)}$; $I_{I(1)}$ and $I_{I(2)}$ are the currents into the two inputs of the pair under test.

PIN CONNECTIONS (OTHER THAN THOSE SHOWN ABOVE)

CIRCUIT TYPES	100 pF to GND	APPLY V_{CC+}	APPLY GND	LEAVE OPEN	OTHER
SN7520, SN7521	C_{ext} (1)	G_Y, G_Z, S_A, S_B (14) (10) (15) (11)		Y, Z (13) (12)	
SN7522, SN7523	C_{ext} (1)	G, S_A, S_B (14) (15) (11)	GND 2 (13)		R_L, Y (10) (12)
SN7524, SN7525	C_{ext} (1)	1S, 2S (15) (11)	GND 2 (13)	1W, 2W (14) (12)	
SN7526, SN7527		PRESET, CLEAR, S_A, S_B (10) (14) (15) (11)		Q, $\overline{Q}$ (12) (13)	
SN7528, SN7529	C_{ext} (1)	1S, 2S (14) (11)		1P, 2P, 1W, 2W (15) (10) (13) (12)	
SN75234, SN75235		1S, 2S (15) (11)	GND 2 (13)	1W, 2W (14) (12)	
SN75238, SN75239		1S, 2S (14) (11)		1P, 2P, 1W, 2W (15) (10) (13) (12)	

FIGURE 2–I_{IB}, I_{IO}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

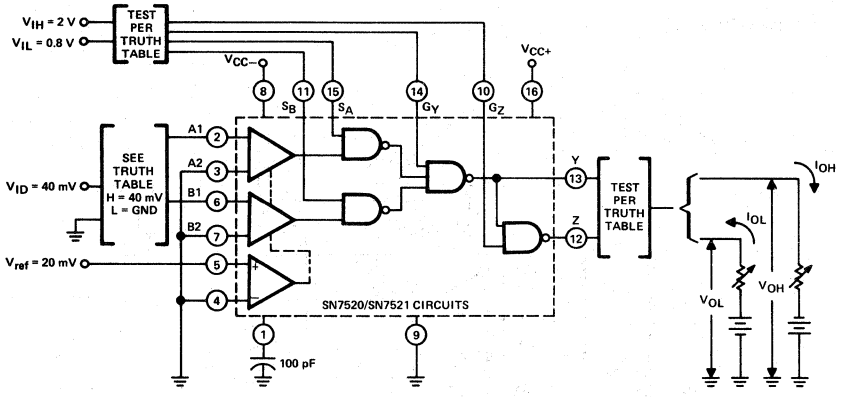
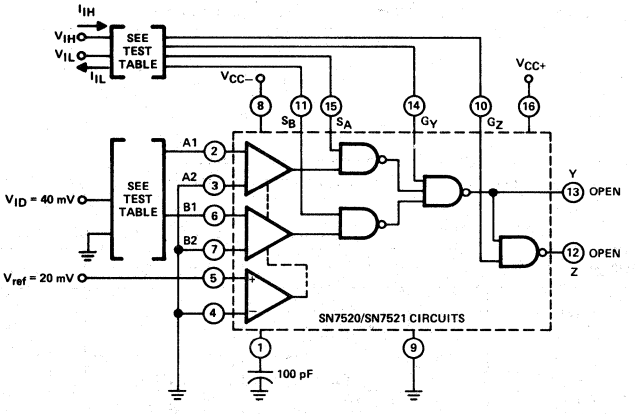


FIGURE 3–V_{IH}, V_{IL}, V_{OH}, V_{OL}



TEST TABLE

TEST	INPUT A1	INPUT B1	STROBE S_A	STROBE S_B	GATE G_Y	GATE G_Z
I_{IH} at STROBE S_A	GND	GND	V_{IH}	V_{IL}	V_{IL}	V_{IL}
I_{IH} at STROBE S_B	GND	GND	V_{IL}	V_{IH}	V_{IL}	V_{IL}
I_{IH} at GATE G_Y	V_{ID}	V_{ID}	V_{IH}	V_{IH}	V_{IH}	V_{IL}
I_{IH} at GATE G_Z	GND	GND	V_{IL}	V_{IL}	V_{IH}	V_{IH}
I_{IL} at STROBE S_A	V_{ID}	GND	V_{IL}	V_{IL}	V_{IL}	V_{IL}
I_{IL} at STROBE S_B	GND	V_{ID}	V_{IL}	V_{IL}	V_{IL}	V_{IL}
I_{IL} at GATE G_Y	GND	GND	V_{IL}	V_{IL}	V_{IL}	V_{IL}
I_{IL} at GATE G_Z	GND	GND	V_{IL}	V_{IL}	V_{IL}	V_{IL}

FIGURE 4–I_{IH}, I_{IL}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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d-c test circuits† (continued)

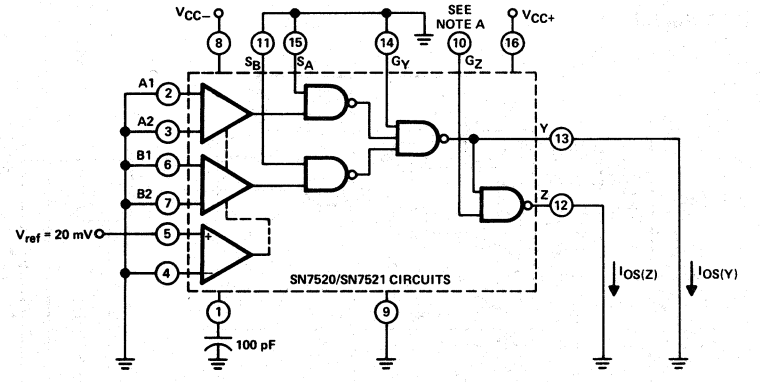
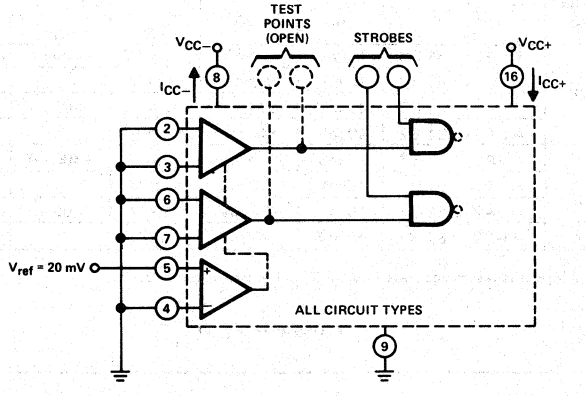


FIGURE 5–I_{OS}

NOTE A: When testing $I_{OS(Y)}$, Pin 10 is open; when testing $I_{OS(Z)}$, Pin 10 is grounded.



PIN CONNECTIONS (OTHER THAN THOSE SHOWN ABOVE)

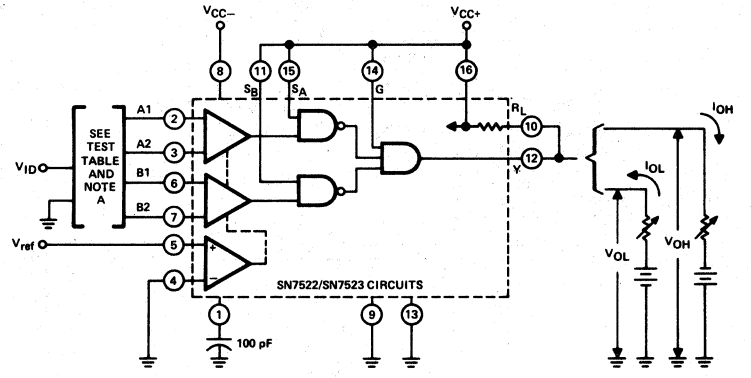
CIRCUIT TYPES	100 pF to GND	APPLY GND	LEAVE OPEN
SN7520, SN7521	C_{ext} (1)	G_Y, G_Z, S_A, S_B (14) (10) (15) (11)	Y, Z (13) (12)
SN7522, SN7523	C_{ext} (1)	G, S_A, S_B, GND 2 (14) (15) (11) (13)	R_L, Y (10) (12)
SN7524, SN7525	C_{ext} (1)	1S, 2S, GND 2 (15) (11) (13)	1W, 2W (14) (12)
SN7526, SN7527		S_A, S_B (15) (11)	PRESET, CLEAR, Q, $\overline{Q}$ (10) (14) (12) (13)
SN7528, SN7529	C_{ext} (1)	1S, 2S (14) (11)	1P, 2P, 1W, 2W (15) (10) (13) (12)
SN75234, SN75235		1S, 2S, GND 2 (15) (11) (13)	1W, 2W (14) (12)
SN75238, SN75239		1S, 2S (14) (11)	1P, 2P, 1W, 2W (15) (10) (13) (12)

FIGURE 6–I_{CC+}, I_{CC-}

† Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



TEST TABLE

CIRCUIT TYPE	INPUTS	V_{ref}	V_{ID}	OUTPUT		
				V_O	I_{OH}	I_{OL}
SN7522	A1-A2 or B1-B2	15 mV	≤11 mV	≥2.4 V	–400 μA	
	A1-A2 or B1-B2	15 mV	≥19 mV	≤0.4 V		16 mA
	A1-A2 or B1-B2	40 mV	≤36 mV	≥2.4 V	–400 μA	
	A1-A2 or B1-B2	40 mV	≥44 mV	≤0.4 V		16 mA
SN7523	A1-A2 or B1-B2	15 mV	≤ 8 mV	≥2.4 V	–400 μA	
	A1-A2 or B1-B2	15 mV	≥22 mV	≤0.4 V		16 mA
	A1-A2 or B1-B2	40 mV	≤33 mV	≥2.4 V	–400 μA	
	A1-A2 or B1-B2	40 mV	≥47 mV	≤0.4 V		16 mA

NOTE A: Each pair of differential inputs is tested separately with the other pair grounded.

FIGURE 7–V_T

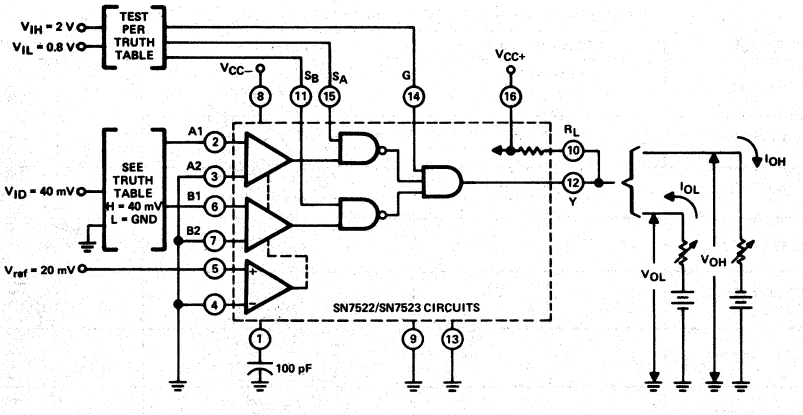


FIGURE 8–V_{IH}, V_{IL}, V_{OH}, V_{OL}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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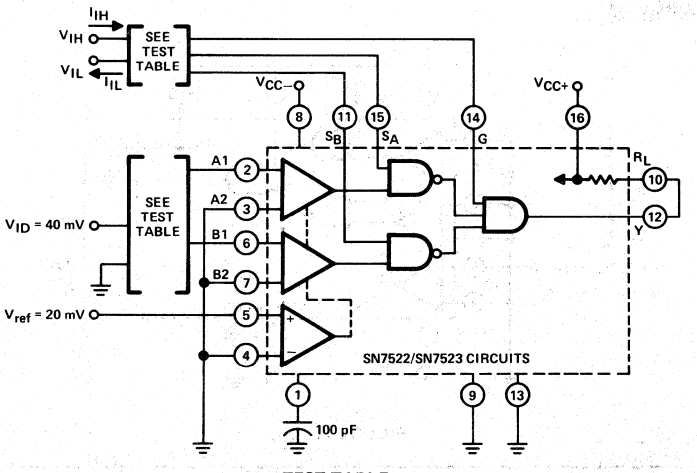
PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



TEST TABLE

TEST	INPUT A1	INPUT B1	STROBE S_A	STROBE S_B	GATE G
I_{IH} at STROBE S_A	GND	GND	V_{IH}	V_{IL}	V_{IH}
I_{IH} at STROBE S_B	GND	GND	V_{IL}	V_{IH}	V_{IH}
I_{IH} at GATE	V_{ID}	V_{ID}	V_{IH}	V_{IH}	V_{IH}
I_{IL} at STROBE S_A	V_{ID}	GND	V_{IL}	V_{IL}	V_{IH}
I_{IL} at STROBE S_B	GND	V_{ID}	V_{IL}	V_{IL}	V_{IH}
I_{IL} at GATE	GND	GND	V_{IL}	V_{IL}	V_{IL}

FIGURE 9–I_{IH}, I_{IL}

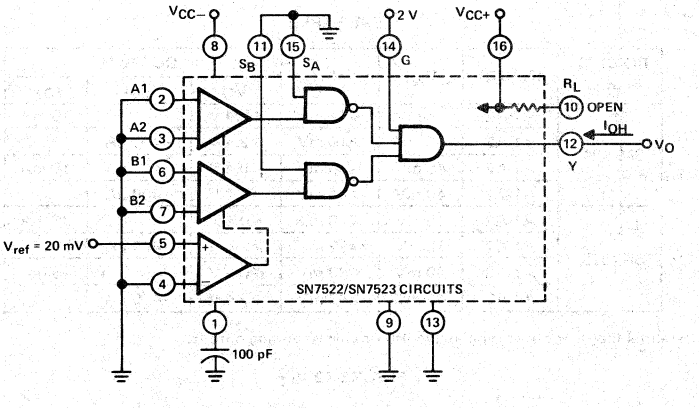


FIGURE 10–I_{OH}

† Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

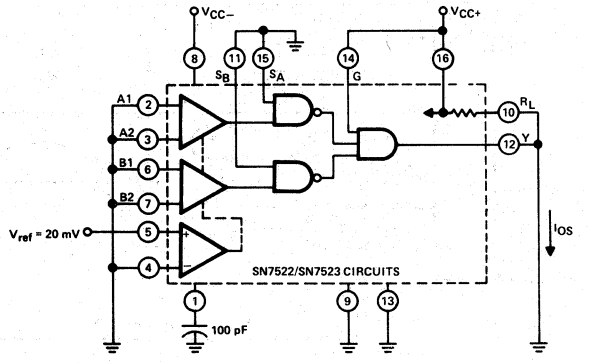
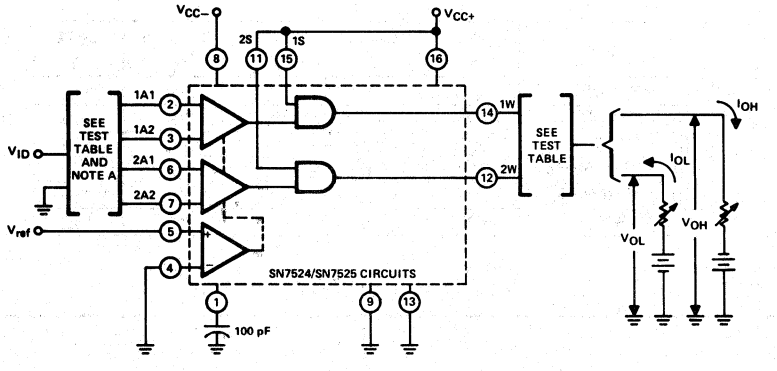


FIGURE 11–I_{OS}



TEST TABLE

CIRCUIT TYPE	INPUTS	V_{ref}	V_{ID}	OUTPUT		
				V_O	I_{OH}	I_{OL}
SN7524	A1-A2	15 mV	≤11 mV	≤0.4 V		16 mA
	A1-A2	15 mV	≥19 mV	≥2.4 V	−400 μA	
	A1-A2	40 mV	≤36 mV	≤0.4 V		16 mA
	A1-A2	40 mV	≥44 mV	≥2.4 V	−400 μA	
SN7525	A1-A2	15 mV	≤ 8 mV	≤0.4 V		16 mA
	A1-A2	15 mV	≥22 mV	≥2.4 V	−400 μA	
	A1-A2	40 mV	≤33 mV	≤0.4 V		16 mA
	A1-A2	40 mV	≥47 mV	≥2.4 V	−400 μA	

NOTE A: Each pair of differential inputs is tested separately with its corresponding output.

FIGURE 12–V_T

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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d-c test circuits† (continued)

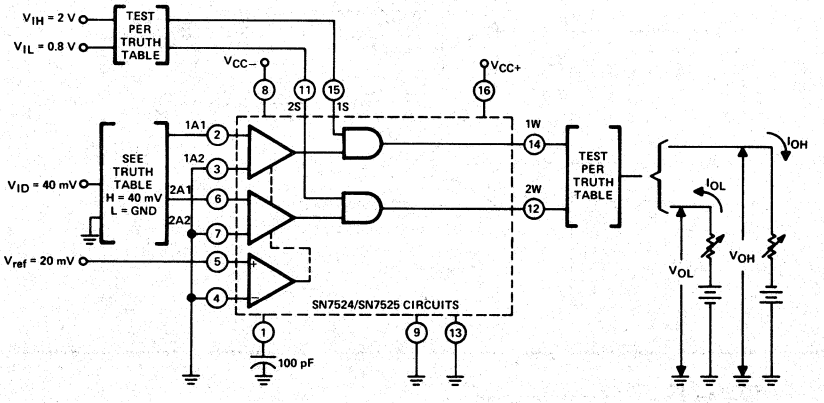
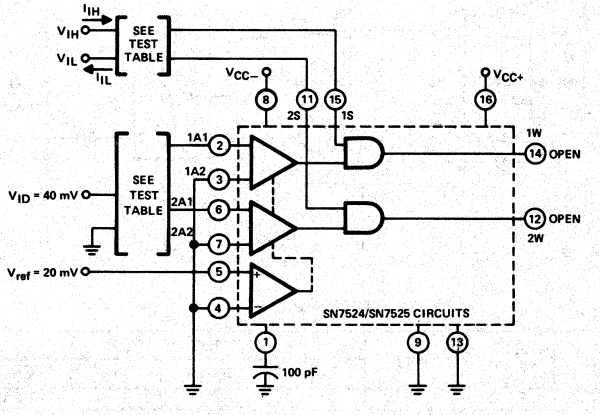


FIGURE 13–V_{IH}, V_{IL}, V_{OH}, V_{OL}



TEST TABLE

TEST	INPUT 1A1	INPUT 2A1	STROBE 1S	STROBE 2S
I_{IH} at STROBE 1S	GND	GND	V_{IH}	V_{IL}
I_{IH} at STROBE 2S	GND	GND	V_{IL}	V_{IH}
I_{IL} at STROBE 1S	V_{ID}	GND	V_{IL}	V_{IL}
I_{IL} at STROBE 2S	GND	V_{ID}	V_{IL}	V_{IL}

FIGURE 14–I_{IH}, I_{IL}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

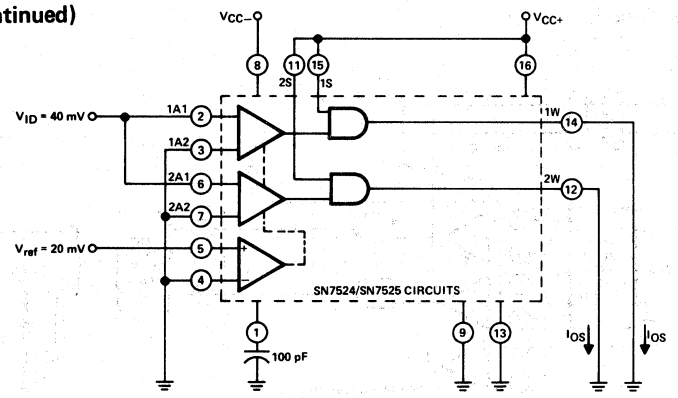
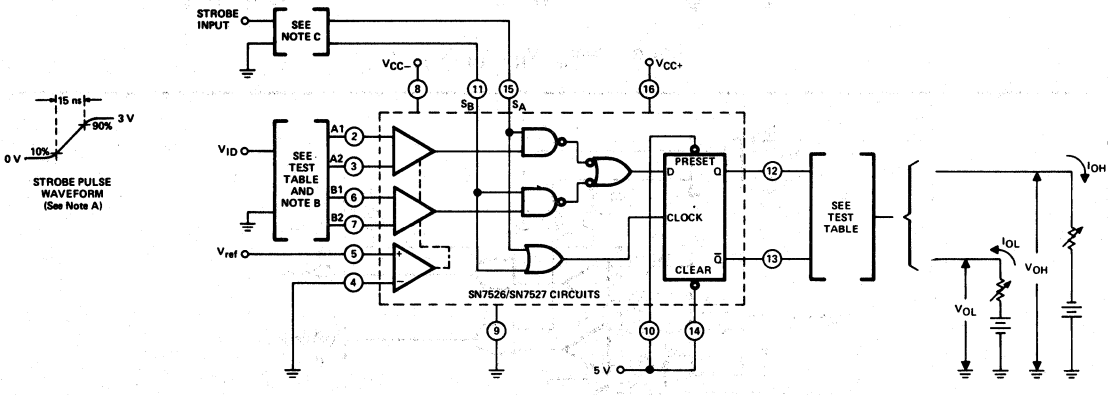


FIGURE 15–I_{OS}



TEST TABLE

CIRCUIT TYPE	INPUTS	V_{ref}	V_{ID}	OUTPUT Q			OUTPUT $\overline{Q}$		
				V_O	I_{OH}	I_{OL}	V_O	I_{OH}	I_{OL}
SN7526	A1-A2 or B1-B2	15 mV	≤11 mV	≤0.4 V		16 mA	≥2.4 V		16 mA
	A1-A2 or B1-B2	15 mV	≥19 mV	≥2.4 V	−400 μA		≤0.4 V	−400 μA	
	A1-A2 or B1-B2	40 mV	≤36 mV	≤0.4 V		16 mA	≥2.4 V		16 mA
	A1-A2 or B1-B2	40 mV	≥44 mV	≥2.4 V	−400 μA		≤0.4 V	−400 μA	
SN7527	A1-A2 or B1-B2	15 mV	≤ 8 mV	≤0.4 V		16 mA	≥2.4 V		16 mA
	A1-A2 or B1-B2	15 mV	≥22 mV	≥2.4 V	−400 μA		≤0.4 V	−400 μA	
	A1-A2 or B1-B2	40 mV	≤33 mV	≤0.4 V		16 mA	≥2.4 V		16 mA
	A1-A2 or B1-B2	40 mV	≥47 mV	≥2.4 V	−400 μA		≤0.4 V	−400 μA	

NOTES: A. The strobe input pulse is supplied by a generator with the following characteristics: Z_O = 50 Ω, $t_r = t_f$ = 15 ± 5 ns, t_w = 500 ns, PRR = 1 MHz.

B. Each pair of differential inputs is tested separately with the other pair grounded.

C. Strobe input pulse is applied to Strobe A when inputs A1-A2 are being tested and to Strobe B when inputs B1-B2 are being tested. In each case, the other strobe input is grounded.

FIGURE 16–V_T

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

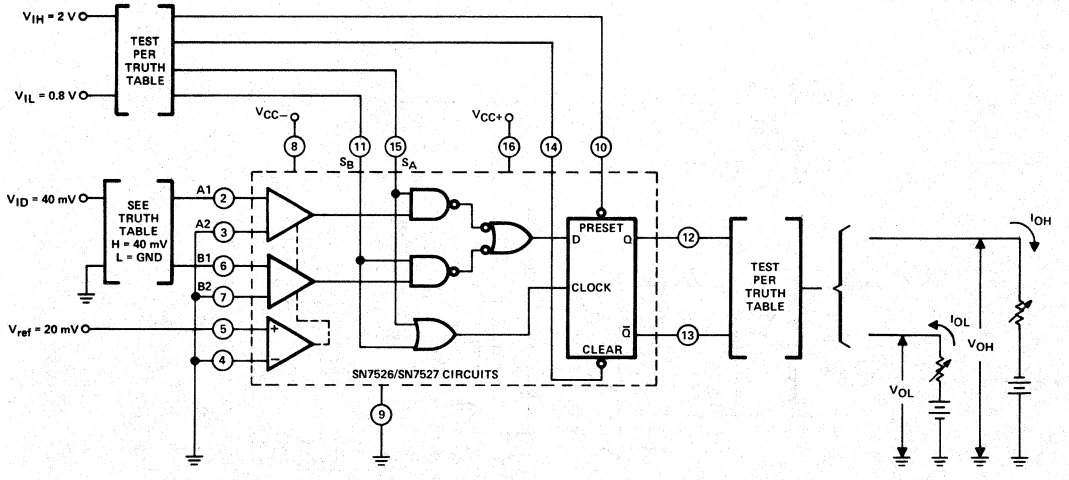
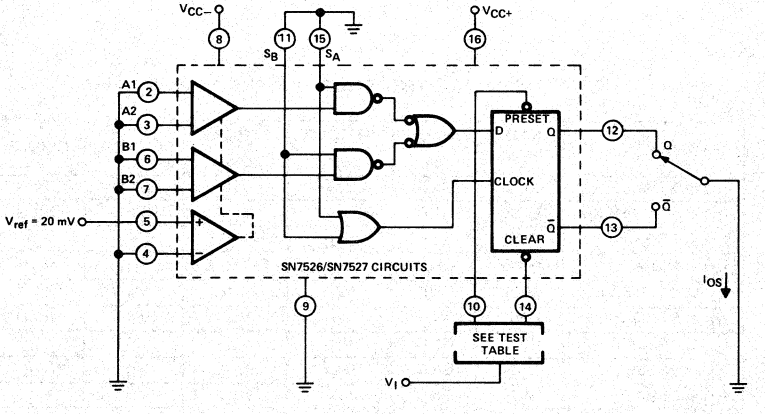


FIGURE 17–V_{IH}, V_{IL}, V_{OH}, V_{OL}



TEST TABLE

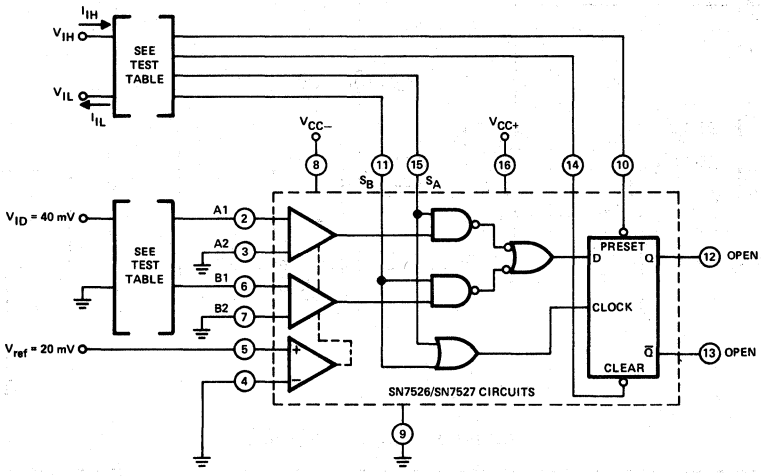
PARAMETER	PRESET	CLEAR
I_{OS} at OUTPUT Q	V_{IL}	V_{IH}
I_{OS} at OUTPUT $\overline{Q}$	V_{IH}	V_{IL}

FIGURE 18–I_{OS}

Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



TEST TABLE

PARAMETER	INPUT A1	INPUT B1	STROBE S_A	STROBE S_B	PRESET	CLEAR
I_{IH} at STROBE S_A	GND	GND	V_{IH}	V_{IL}	OPEN	OPEN
I_{IH} at STROBE S_B	GND	GND	V_{IL}	V_{IH}	OPEN	OPEN
I_{IH} at PRESET	GND	V_{ID}	V_{IL}	NOTE B	V_{IH}	V_{IH}
I_{IH} at CLEAR	GND	GND	V_{IL}	NOTE B	V_{IH}	V_{IH}
I_{IL} at STROBE S_A	V_{ID}	GND	V_{IL}	V_{IH}	OPEN	OPEN
I_{IL} at STROBE S_B	GND	V_{ID}	V_{IH}	V_{IL}	OPEN	OPEN
I_{IL} at PRESET	GND	GND	V_{IL}	V_{IL}	V_{IL}	V_{IL}
I_{IL} at PRESET	V_{ID}	GND	V_{IH}	V_{IL}	V_{IL}	V_{IL}
I_{IL} at CLEAR	V_{ID}	GND	V_{IL}	V_{IL}	V_{IL}	V_{IL}

NOTES: A. Each input is tested separately.
B. Momentary ground, then V_{IH}.

FIGURE 19–I_{IH}, I_{IL}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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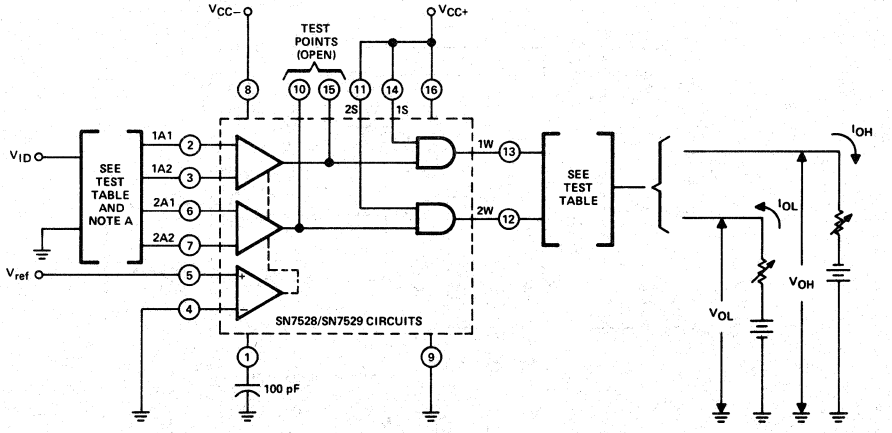
d-c test circuits† (continued)



TEST TABLE

CIRCUIT TYPE	INPUTS	V_{ref}	V_{ID}	OUTPUT		
				V_O	I_{OH}	I_{OL}
SN7528	A1-A2	15 mV	≤11 mV	≤0.4 V		16 mA
	A1-A2	15 mV	≥19 mV	≥2.4 V	−400 μA	
	A1-A2	40 mV	≤36 mV	≤0.4 V		16 mA
	A1-A2	40 mV	≥44 mV	≥2.4 V	−400 μA	
SN7529	A1-A2	15 mV	≤ 8 mV	≤0.4 V		16 mA
	A1-A2	15 mV	≥22 mV	≥2.4 V	−400 μA	
	A1-A2	40 mV	≤33 mV	≤0.4 V		16 mA
	A1-A2	40 mV	≥47 mV	≥2.4 V	−400 μA	

NOTE A: Each pair of inputs is tested separately with its corresponding output.

FIGURE 20–V_T

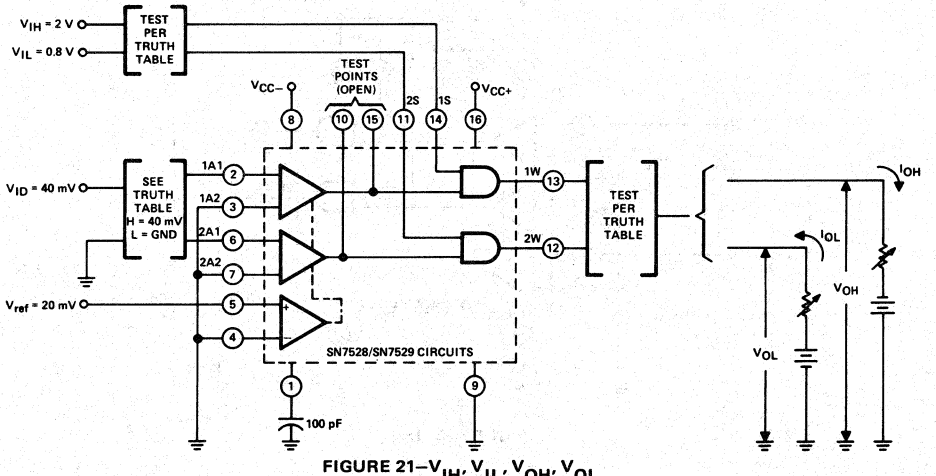
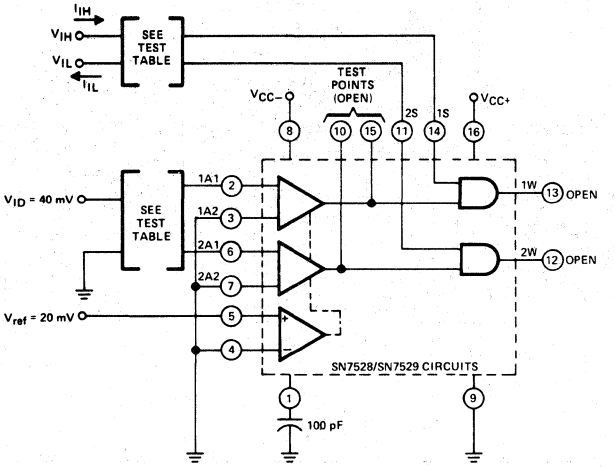


FIGURE 21–V_{IH}, V_{IL}, V_{OH}, V_{OL}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



TEST TABLE

TEST	INPUT 1A1	INPUT 2A1	STROBE 1S	STROBE 2S
I_{IH} at STROBE 1S	GND	GND	V_{IH}	V_{IL}
I_{IH} at STROBE 2S	GND	GND	V_{IL}	V_{IH}
I_{IL} at STROBE 1S	V_{ID}	GND	V_{IL}	V_{IL}
I_{IL} at STROBE 2S	GND	V_{ID}	V_{IL}	V_{IL}

FIGURE 22–I_{IH}, I_{IL}

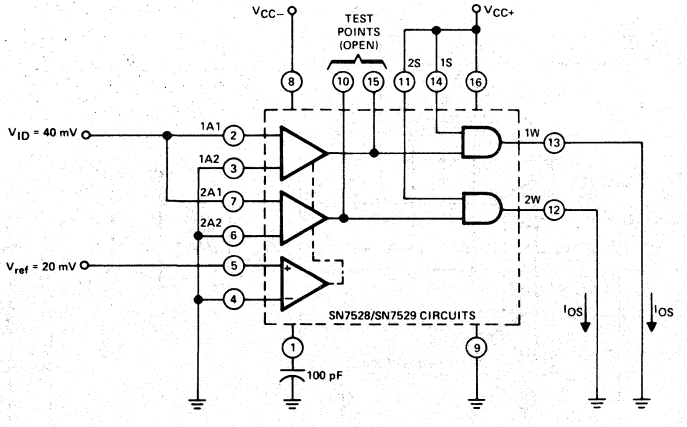


FIGURE 23–I_{OS}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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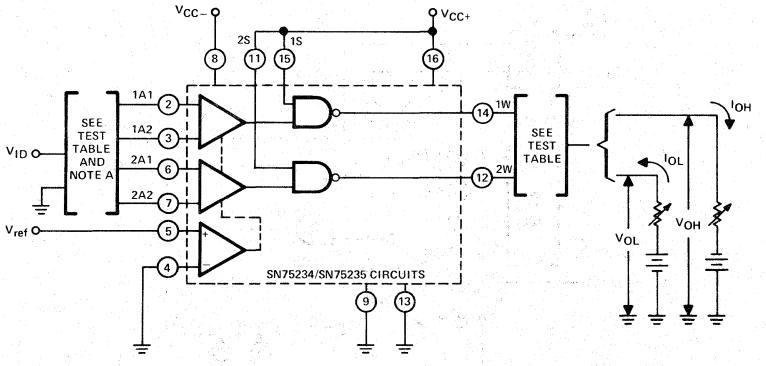
PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



TEST TABLE

CIRCUIT TYPE	INPUTS	V_{ref}	V_{ID}	OUTPUT		
				V_O	I_{OH}	I_{OL}
SN75234	A1-A2	15 mV	≤11 mV	≥2.4 V	−400 μA	
	A1-A2	15 mV	≥19 mV	≤0.4 V		16 mA
	A1-A2	40 mV	≤36 mV	≥2.4 V	−400 μA	
	A1-A2	40 mV	≥44 mV	≤0.4 V		16 mA
SN75235	A1-A2	15 mV	≤ 8 mV	≥2.4 V	−400 μA	
	A1-A2	15 mV	≥22 mV	≤0.4 V		16 mA
	A1-A2	40 mV	≤33 mV	≥2.4 V	−400 μA	
	A1-A2	40 mV	≥47 mV	≤0.4 V		16 mA

NOTE A: Each pair of differential inputs is tested separately with its corresponding output.

FIGURE 24–V_T

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

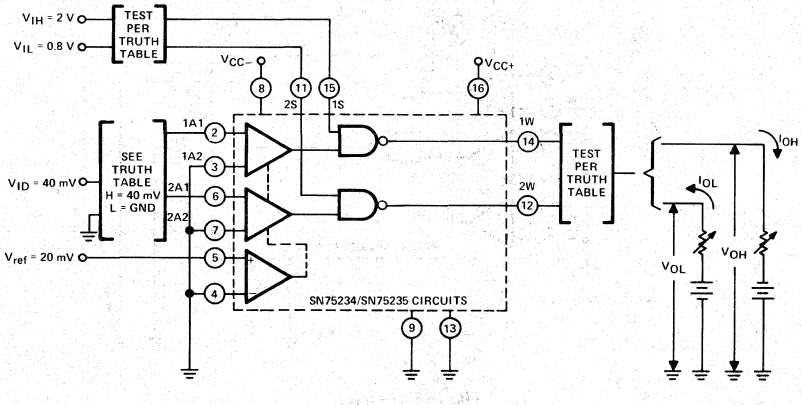
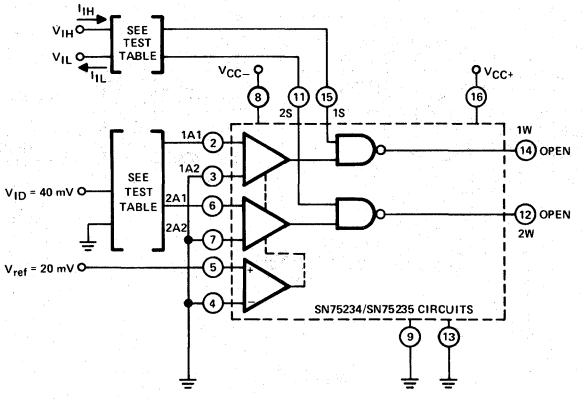


FIGURE 25–V_{IH}, V_{IL}, V_{OH}, V_{OL}

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



TEST TABLE

TEST	INPUT 1A1	INPUT 2A1	STROBE 1S	STROBE 2S
I_{IH} at STROBE 1S	GND	GND	V_{IH}	V_{IL}
I_{IH} at STROBE 2S	GND	GND	V_{IL}	V_{IH}
I_{IL} at STROBE 1S	V_{ID}	GND	V_{IL}	V_{IL}
I_{IL} at STROBE 2S	GND	V_{ID}	V_{IL}	V_{IL}

FIGURE 26–I_{IH}, I_{IL}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

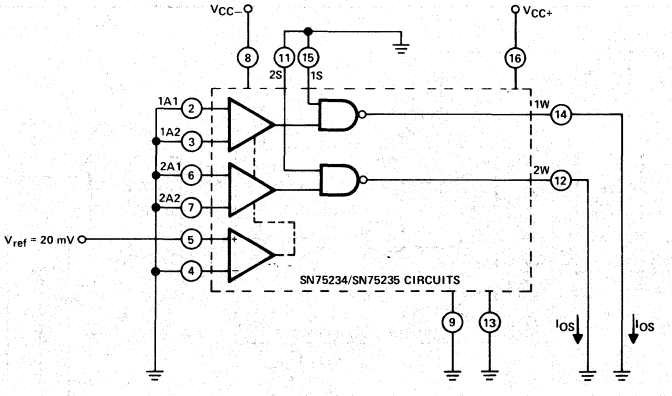


FIGURE 27–I_{OS}

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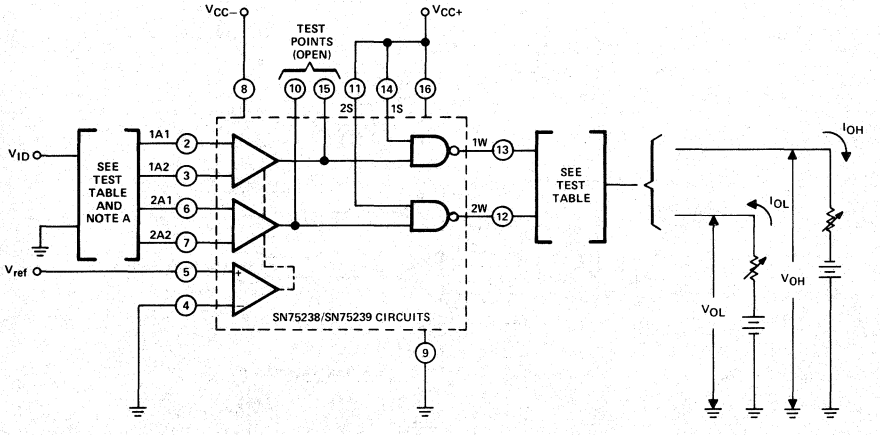
PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



TEST TABLE

CIRCUIT TYPE	INPUTS	V_{ref}	V_{ID}	OUTPUT		
				V_O	I_{OH}	I_{OL}
SN75238	A1-A2	15 mV	≤11 mV	≥2.4 V	−400 μA	
	A1-A2	15 mV	≥19 mV	≤0.4 V		16 mA
	A1-A2	40 mV	≤36 mV	≥2.4 V	−400 μA	
	A1-A2	40 mV	≥44 mV	≤0.4 V		16 mA
SN75239	A1-A2	15 mV	≤ 8 mV	≥2.4 V	−400 μA	
	A1-A2	15 mV	≥22 mV	≤0.4 V		16 mA
	A1-A2	40 mV	≤33 mV	≥2.4 V	−400 μA	
	A1-A2	40 mV	≥47 mV	≤0.4 V		16 mA

NOTE A: Each pair of inputs is tested separately with its corresponding output.

FIGURE 28–V_T

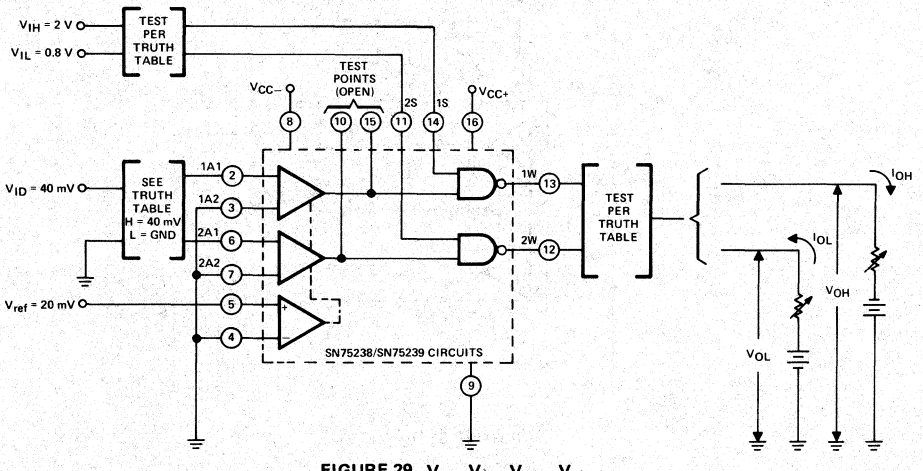
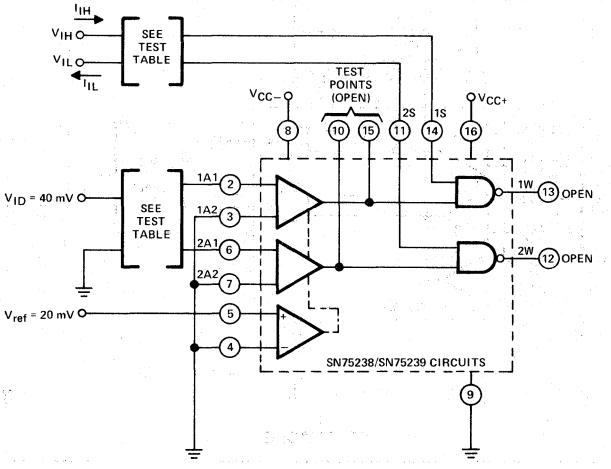


FIGURE 29–V_{IH}, V_{IL}, V_{OH}, V_{OL}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



TEST TABLE

TEST	INPUT 1A1	INPUT 2A1	STROBE 1S	STROBE 2S
I_{IH} at STROBE 1S	GND	GND	V_{IH}	V_{IL}
I_{IH} at STROBE 2S	GND	GND	V_{IL}	V_{IH}
I_{IL} at STROBE 1S	V_{ID}	GND	V_{IL}	V_{IL}
I_{IL} at STROBE 2S	GND	V_{ID}	V_{IL}	V_{IL}

FIGURE 30–I_{IH}, I_{IL}

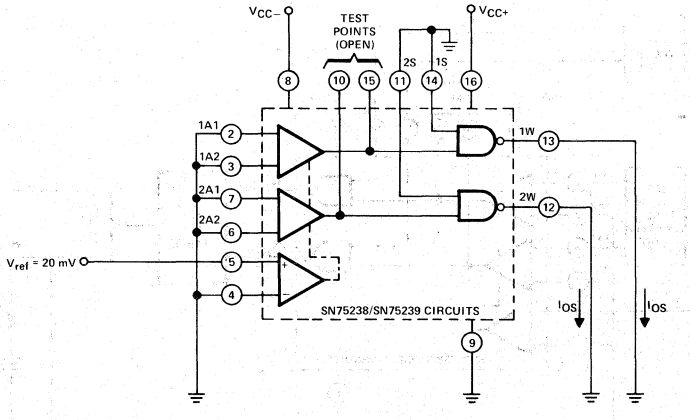


FIGURE 31–I_{OS}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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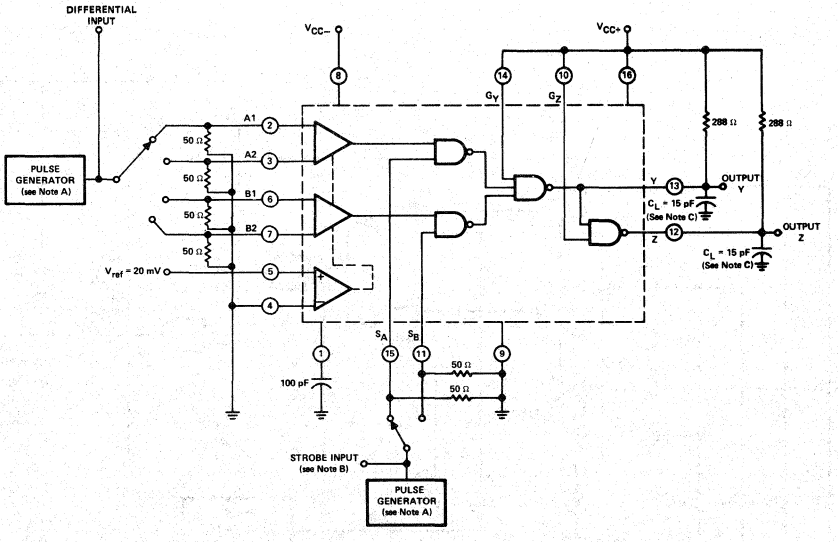
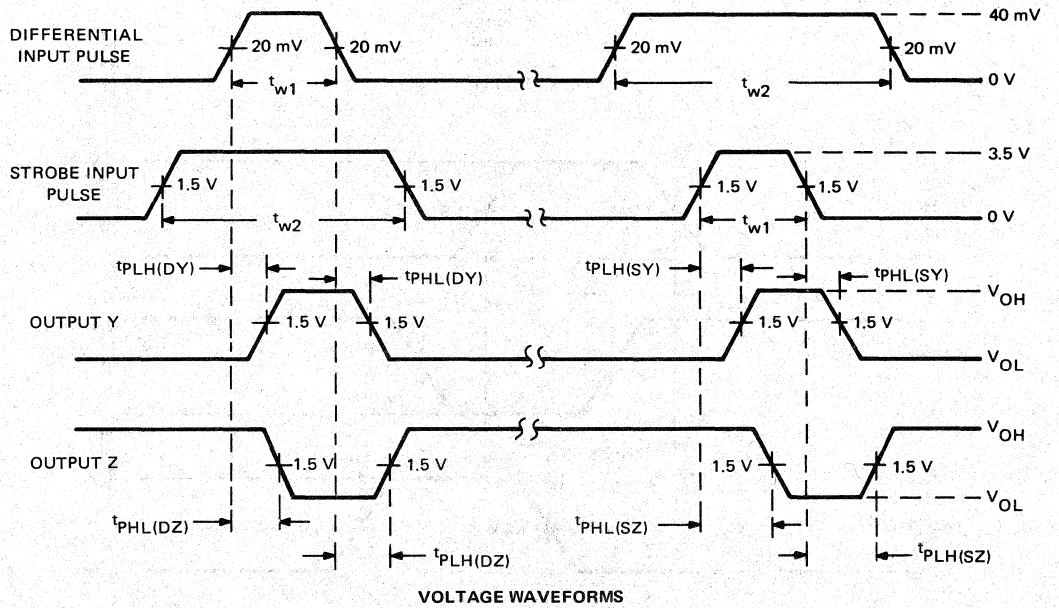
PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_O = 50 Ω, $t_r = t_f$ = 15 ± 5 ns, t_{w1} = 100 ns, t_{w2} = 300 ns, and PRR = 1 MHz.

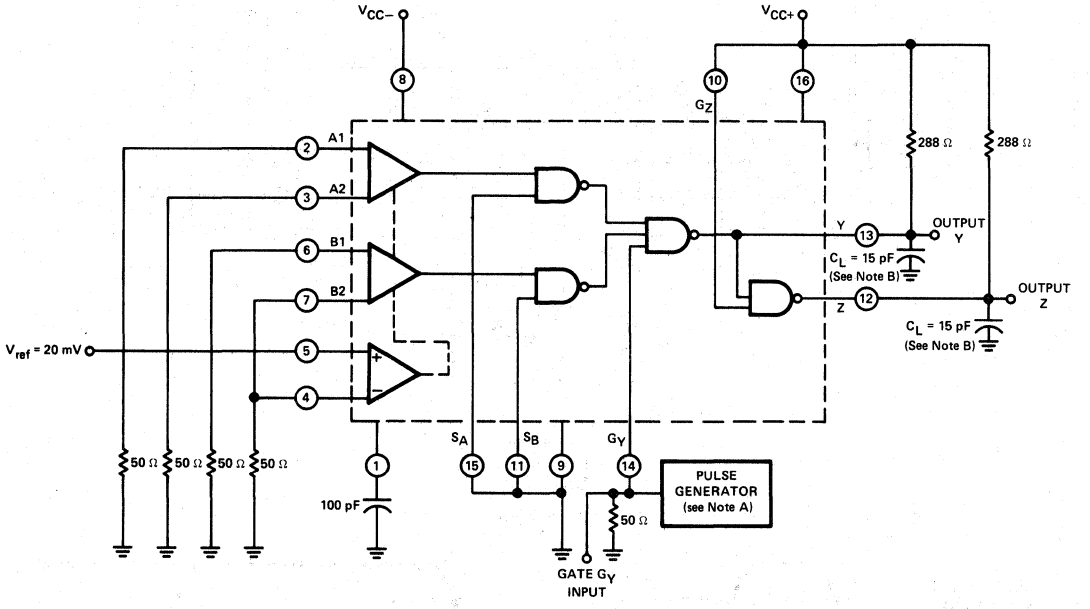
B. The strobe input pulse is applied to Strobe S_A when inputs A1-A2 are being tested and to Strobe S_B when inputs B1-B2 are being tested.

C. C_L includes probe and jig capacitance.

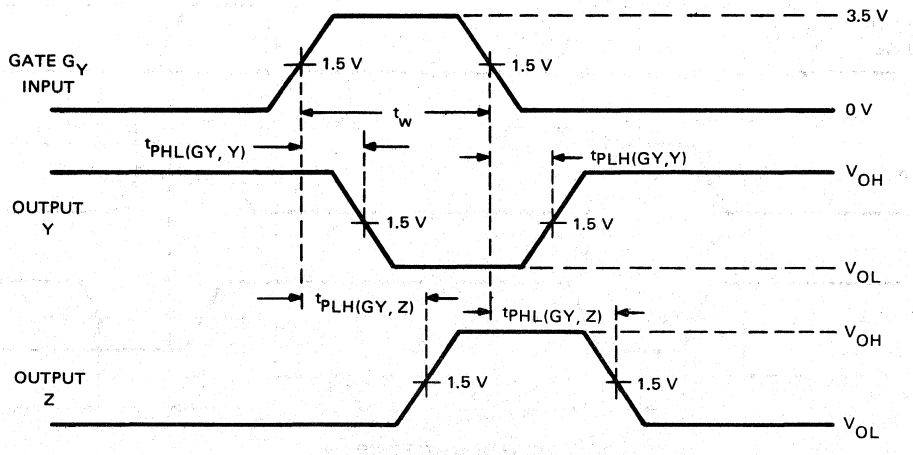
FIGURE 32–SN7520/SN7521 PROPAGATION DELAY TIMES FROM DIFFERENTIAL AND STROBE INPUTS

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, $t_r = t_f$ = 15 ± 5 ns, t_w = 100 ns, and PRR = 1 MHz.
B. C_L includes probe and jig capacitance.

FIGURE 33–SN7520/SN7521 PROPAGATION DELAY TIMES FROM GATE G_Y

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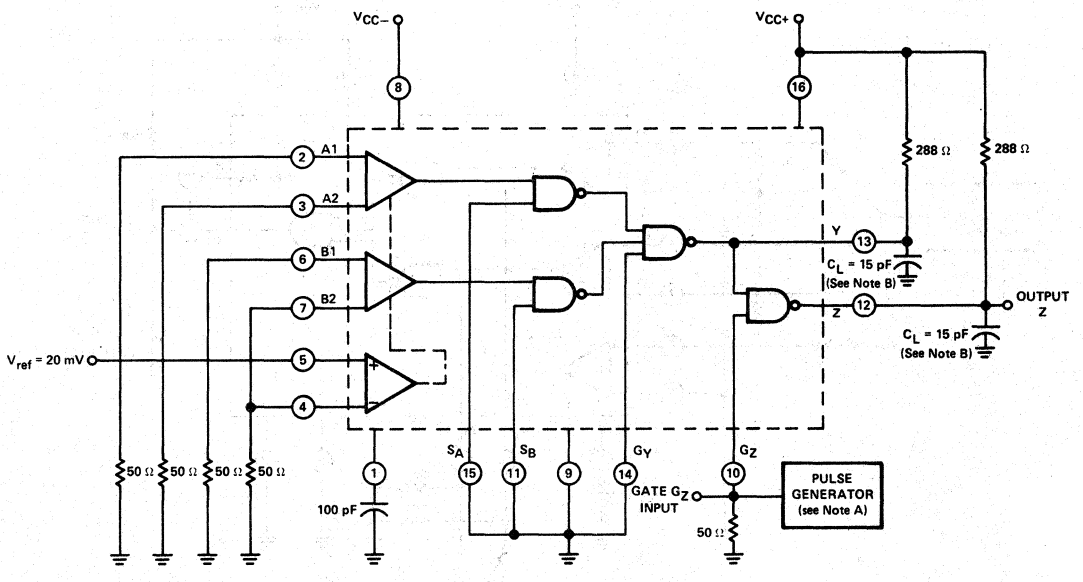
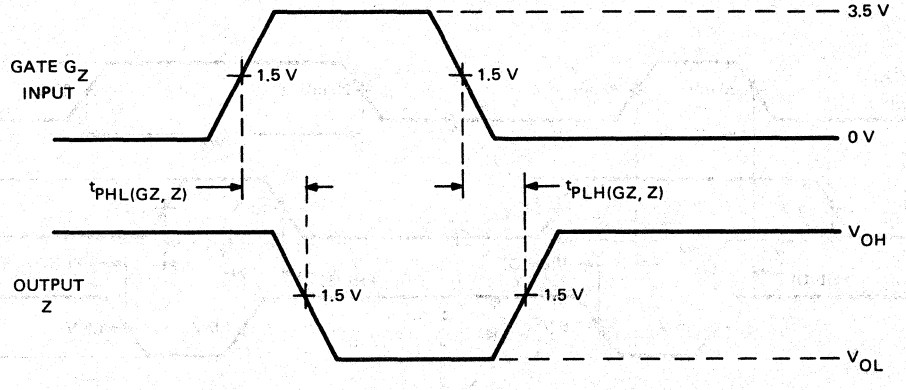
PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



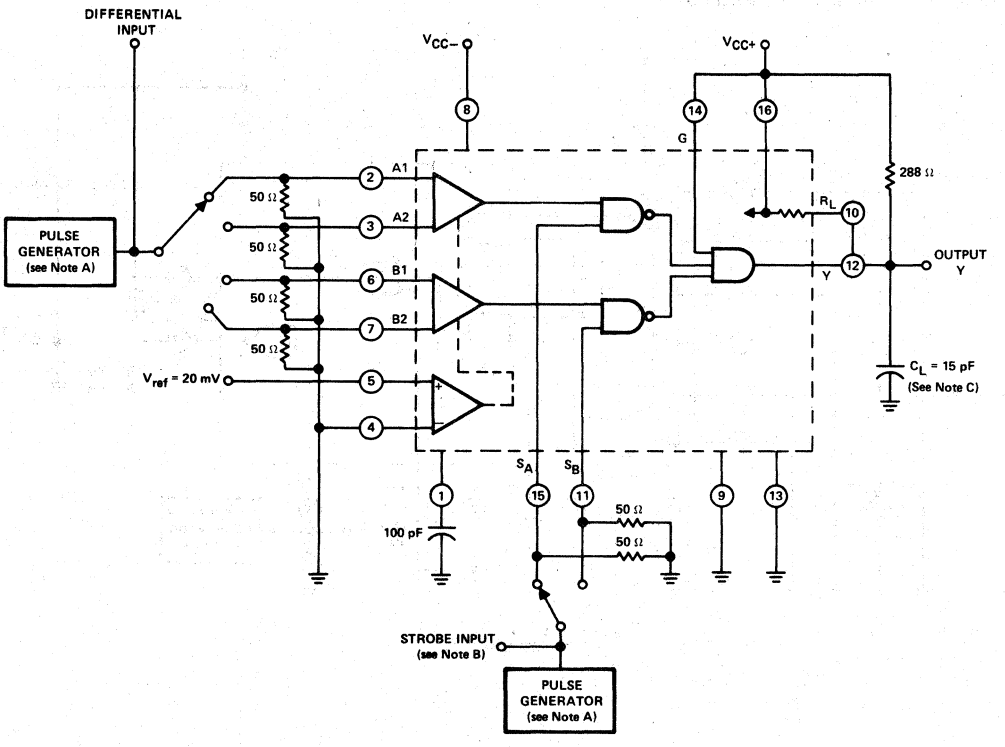
VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, $t_r = t_f$ = 15 ± 5 ns, t_w = 100 ns, and PRR = 1 MHz.
B. C_L includes probe and jig capacitance.

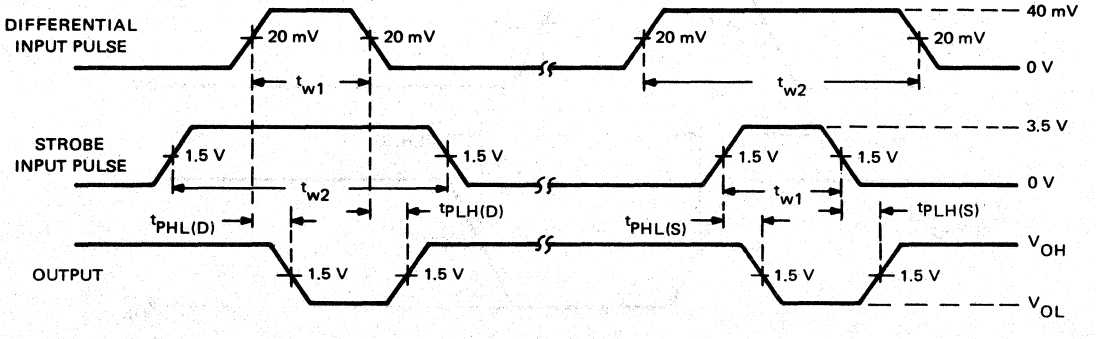
FIGURE 34–SN7520/SN7521 PROPAGATION DELAY TIMES FROM GATE G_Z

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: $Z_{out} \approx 50\ \Omega$, $t_r = t_f = 15 \pm 5$ ns, $t_{w1} = 100$ ns, $t_{w2} = 300$ ns, PRR = 1 MHz.

B. The strobe input pulse is applied to Strobe S_A when testing inputs A1-A2 and to Strobe S_B when testing inputs B1-B2.

C. C_L includes probe and jig capacitance.

FIGURE 35–SN7522/SN7523 PROPAGATION DELAY TIMES FROM DIFFERENTIAL AND STROBE INPUTS

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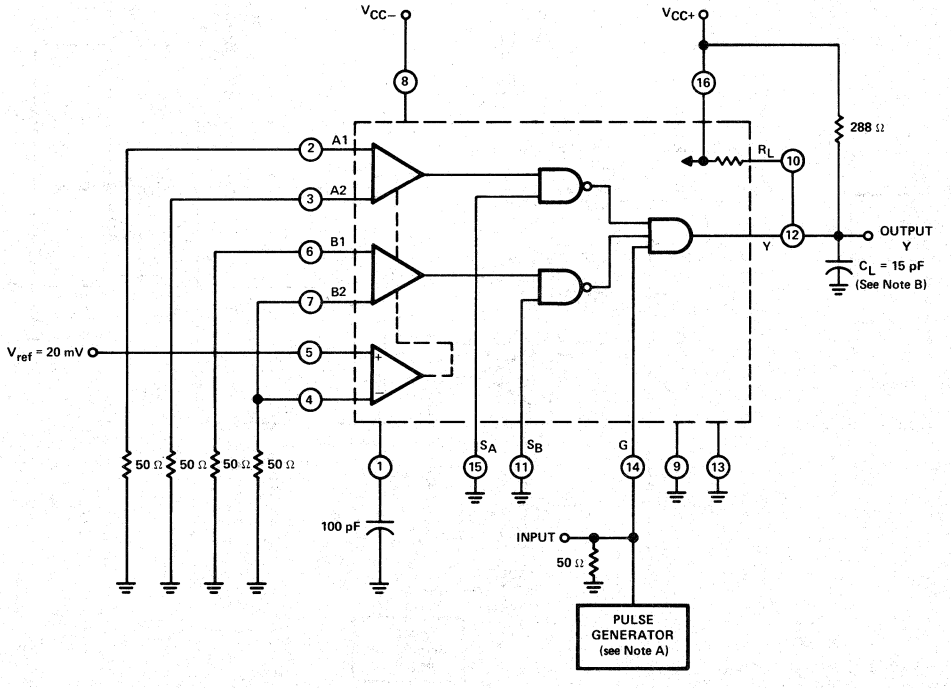
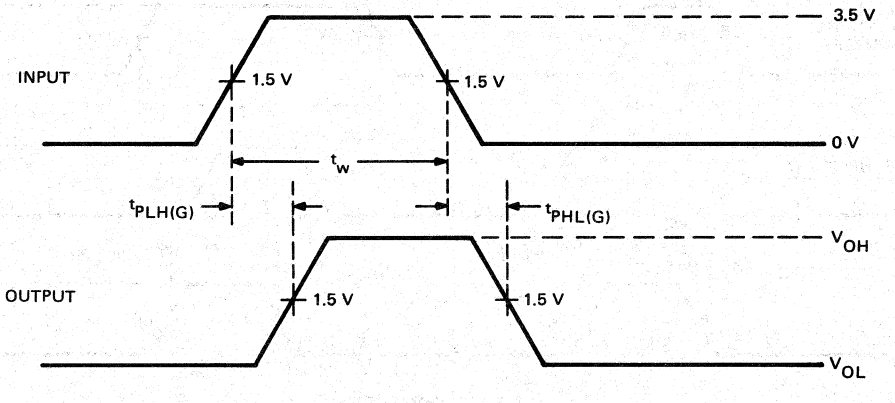
switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

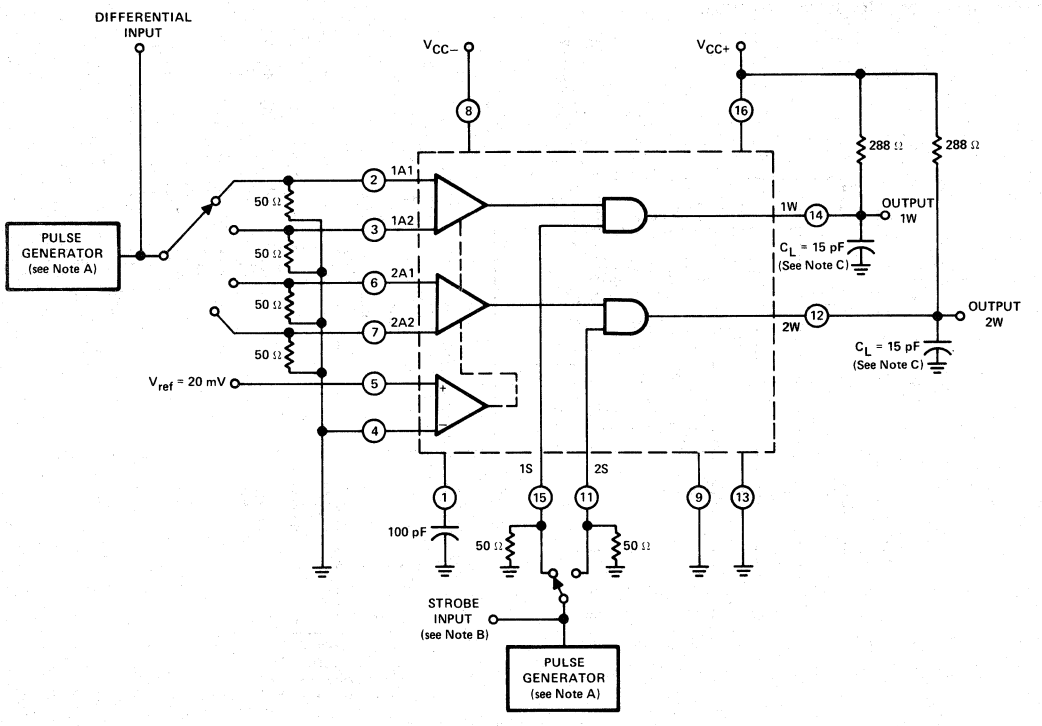
NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, $t_r = t_f$ = 15 ± 5 ns, t_{p1} = 100 ns, t_{p2} = 300 ns, t_{p3} = 0.8 μs, PRR = 1 MHz.

B. C_L includes probe and jig capacitance.

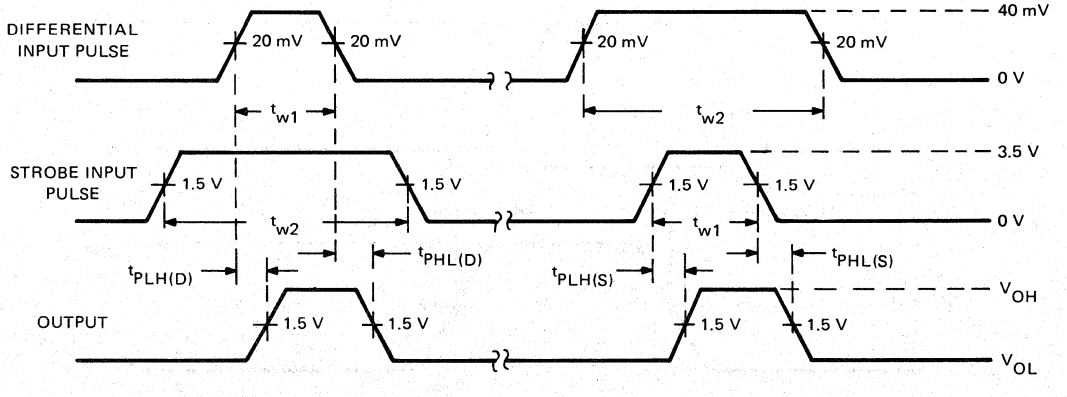
FIGURE 36–SN7522/SN7523 PROPAGATION DELAY TIMES FROM GATE INPUT

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_{out} = 50 Ω, $t_r = t_f$ = 15 ± 5 ns, t_{w1} = 100 ns, t_{w2} = 300 ns, and PRR = 1 MHz.

B. The strobe input pulse is applied to Strobe 1S when inputs 1A1-1A2 are being tested and to Strobe 2S when inputs 2A1-2A2 are being tested.

C. C_L includes probe and jig capacitance.

FIGURE 37–SN7524/SN7525 PROPAGATION DELAY TIMES

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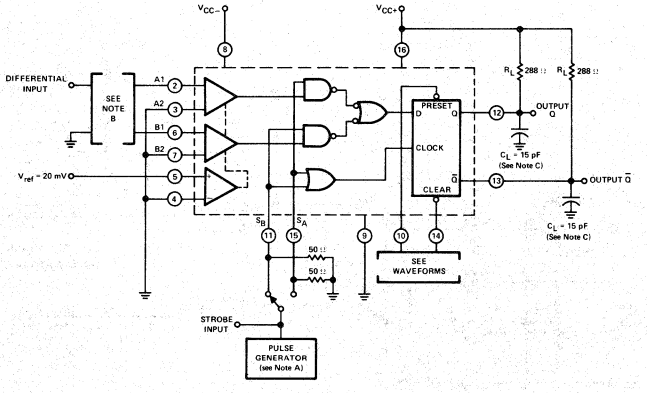
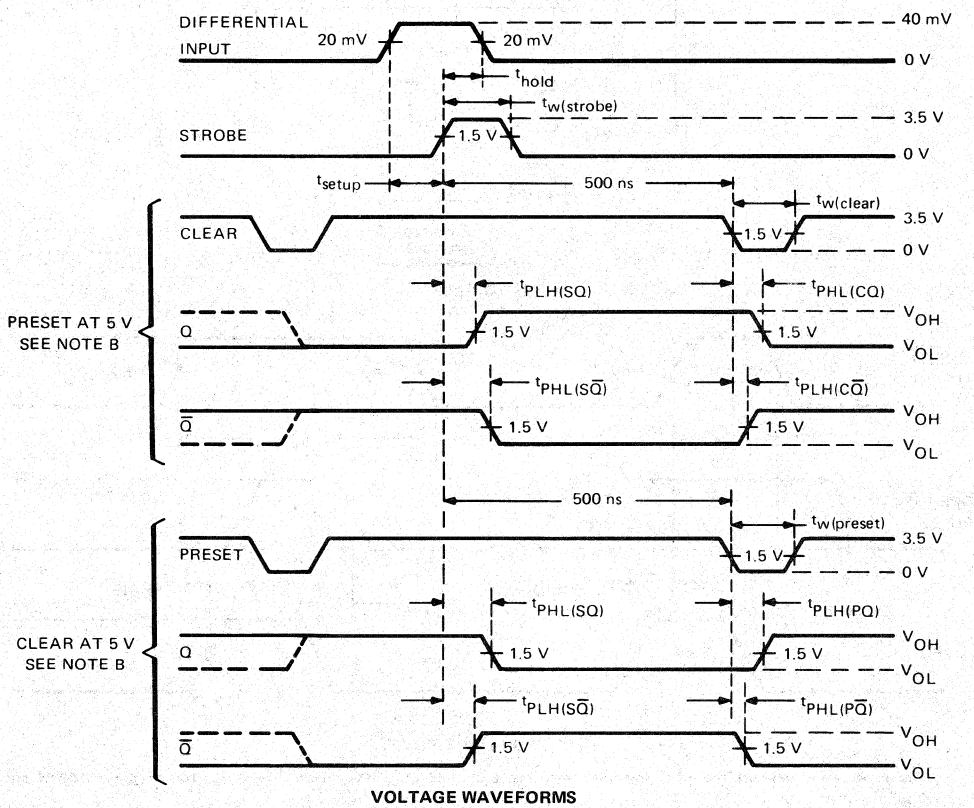
PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



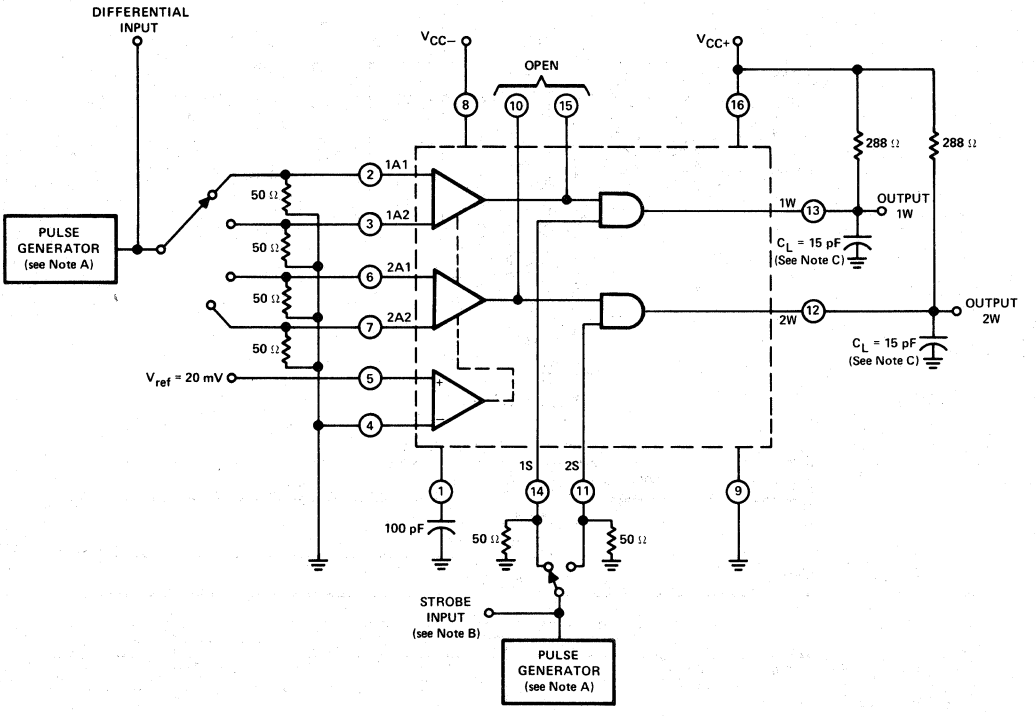
VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_{out} = 50 Ω, $t_r = t_f$ = 15 ± 5 ns, t_w = 50 ns, and PRR = 1 MHz.
B. Each preamplifier is tested separately. Apply 40-mV pulse to input A1 when testing Strobe S_A and to B1 when testing Strobe S_B.
C. C_L includes probe and jig capacitance.

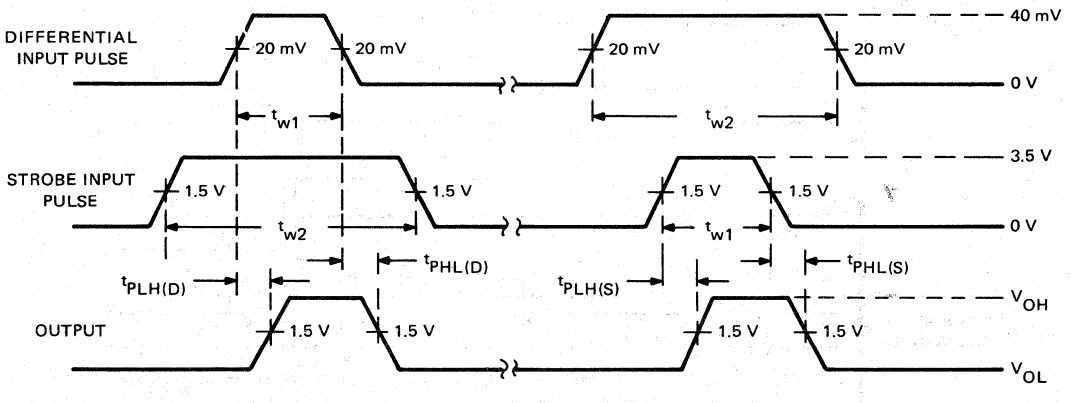
FIGURE 38–SN7526/SN7527 PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_{out} = 50 Ω, $t_r = t_f$ = 15 ± 5 ns, t_{w1} = 100 ns, t_{w2} = 300 ns, and PRR = 1 MHz.

B. The strobe input pulse is applied to Strobe 1S when inputs 1A1-1A2 are being tested and to Strobe 2S when inputs 2A1-2S2 are being tested.

C. C_L includes probe and jig capacitance.

FIGURE 39—SN7528/SN7529 PROPAGATION DELAY TIMES

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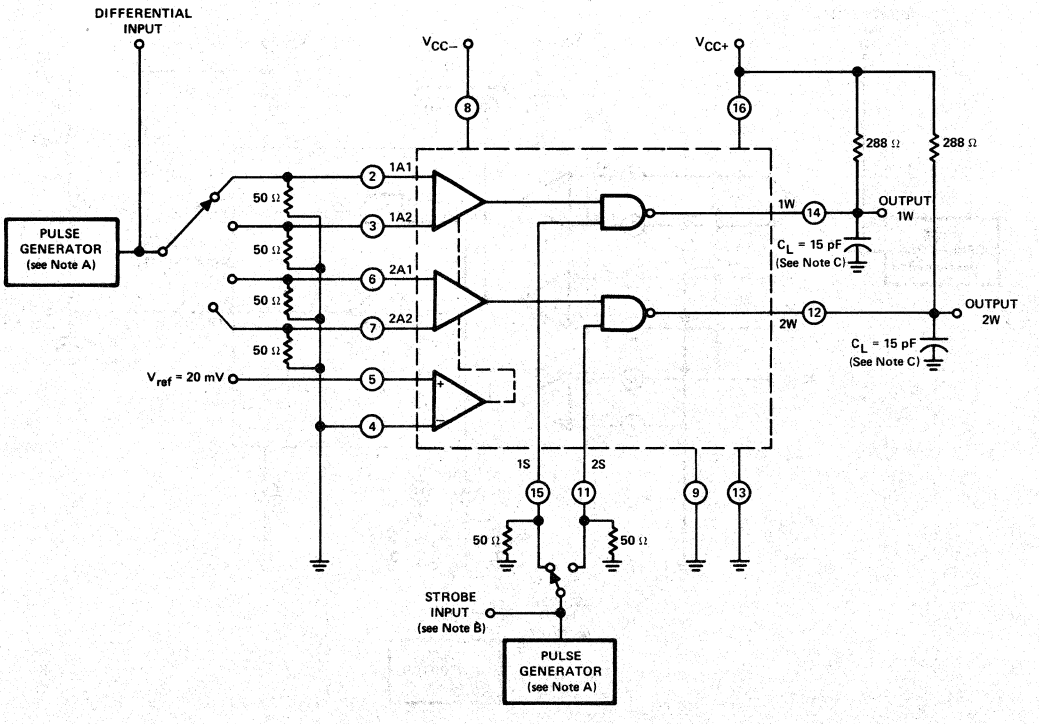
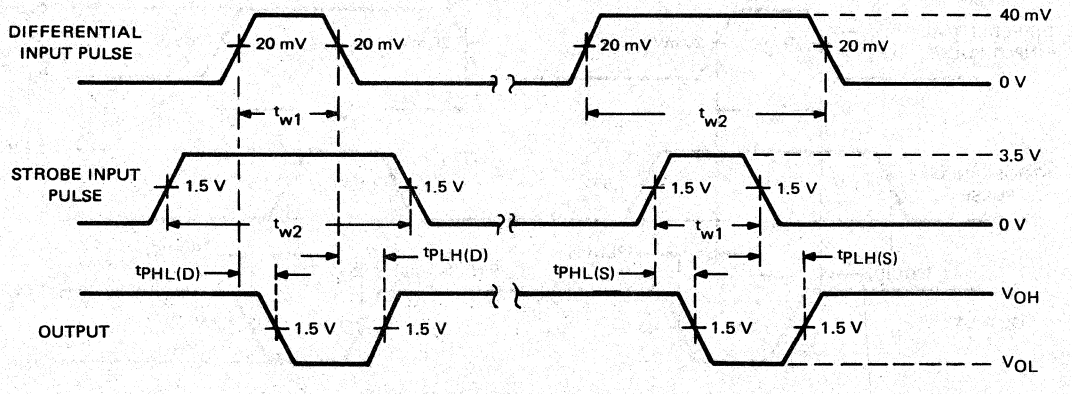
PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_{out} = 50 Ω, $t_r = t_f$ = 15 ± 5 ns, t_{w1} = 100 ns, t_{w2} = 300 ns, and PRR = 1 MHz.

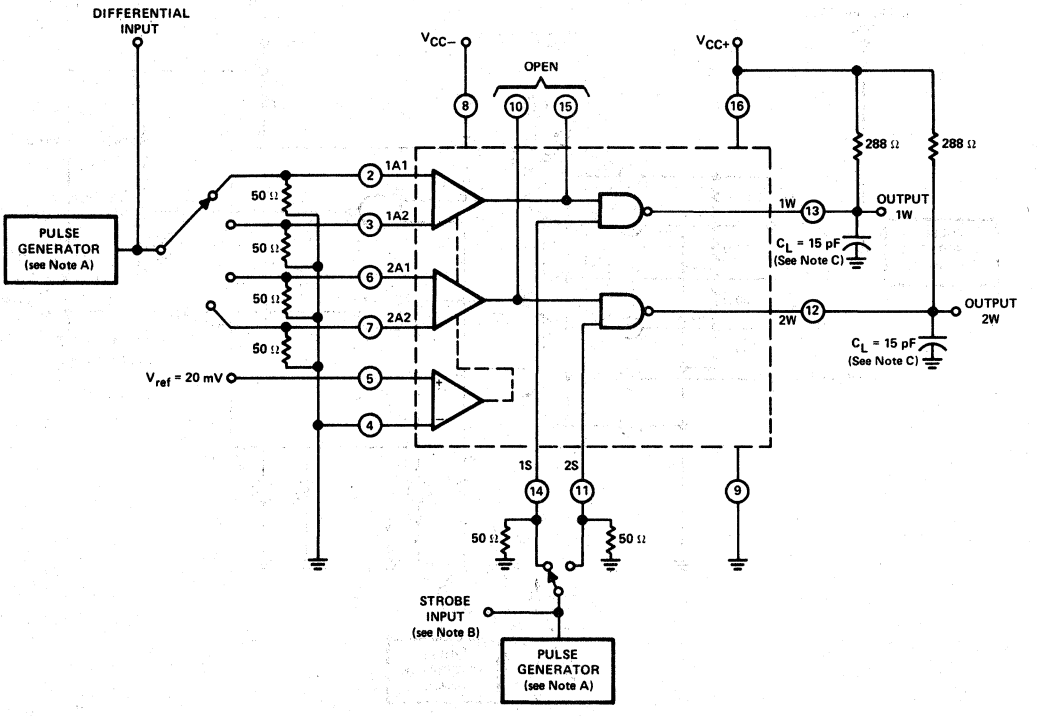
B. The strobe input pulse is applied to Strobe 1S when inputs 1A1-1A2 are being tested and to Strobe 2S when inputs 2A1-2A2 are being tested.

C. C_L includes probe and jig capacitance.

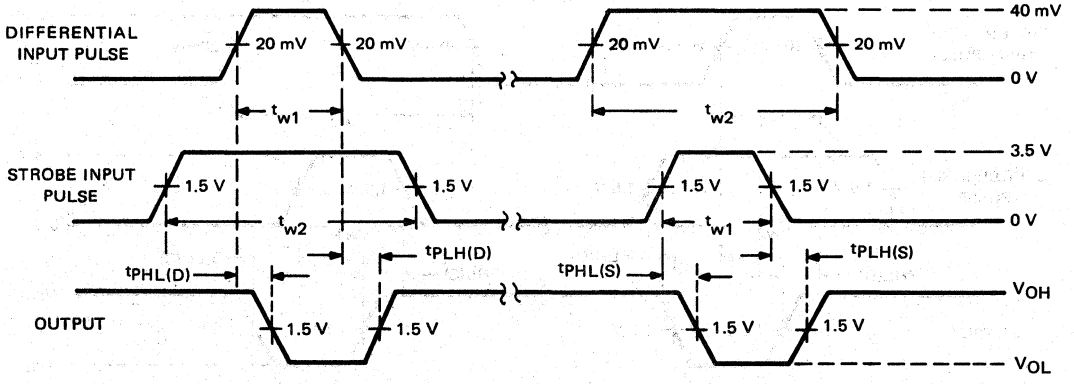
FIGURE 40–SN75234/SN75235 PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_{out} = 50 Ω, $t_r = t_f$ = 15 ± 5 ns, t_{w1} = 100 ns, t_{w2} = 300 ns, and PRR = 1 MHz.

B. The strobe input pulse is applied to Strobe 1S when inputs 1A1-1A2 are being tested and to Strobe 2S when inputs 2A1-2S2 are being tested.

C. C_L includes probe and jig capacitance.

FIGURE 41–SN75238/SN75239 PROPAGATION DELAY TIMES

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TYPICAL CHARACTERISTICS

THRESHOLD VOLTAGE
vs
REFERENCE VOLTAGE

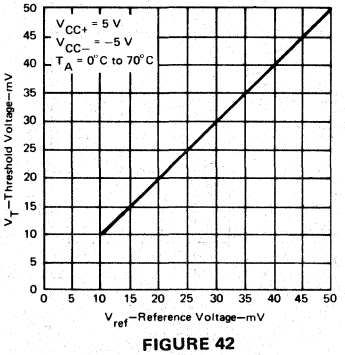

FIGURE 42

THRESHOLD VOLTAGE
vs
SUPPLY VOLTAGE

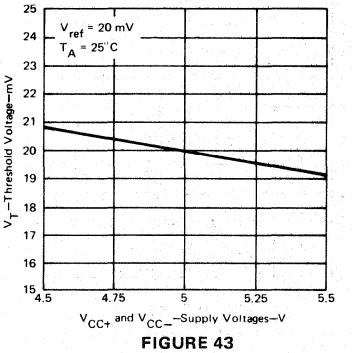

FIGURE 43

NORMALIZED THRESHOLD VOLTAGE
vs
PULSE REPETITION RATE

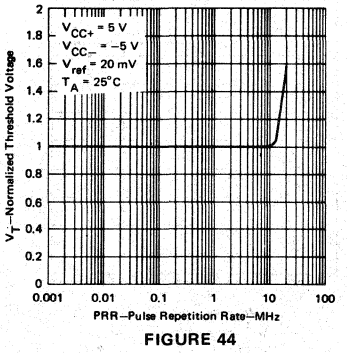

FIGURE 44

COMMON-MODE FIRING VOLTAGE
vs
FREE-AIR TEMPERATURE

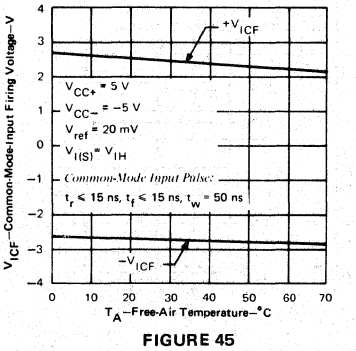

FIGURE 45

DIFFERENTIAL-INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

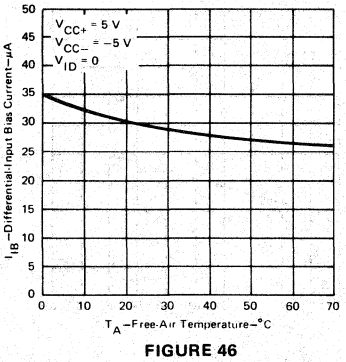

FIGURE 46

DIFFERENTIAL-INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

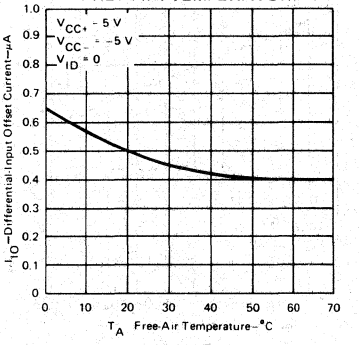

FIGURE 47

TYPICAL CHARACTERISTICS

HIGH-LEVEL INPUT CURRENT
vs
INPUT VOLTAGE

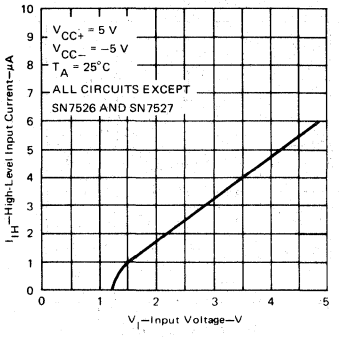

FIGURE 48

LOW-LEVEL INPUT CURRENT
vs
INPUT VOLTAGE

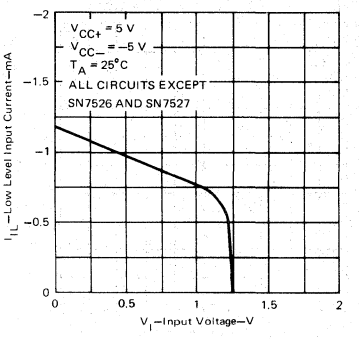

FIGURE 49

OUTPUT VOLTAGE
vs
DIFFERENTIAL-INPUT VOLTAGE

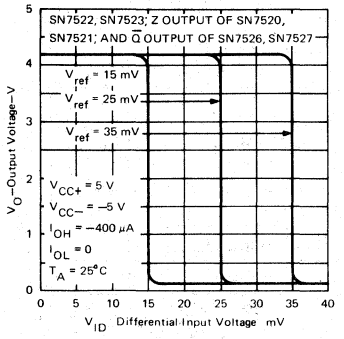

FIGURE 50

OUTPUT VOLTAGE
vs
DIFFERENTIAL-INPUT VOLTAGE

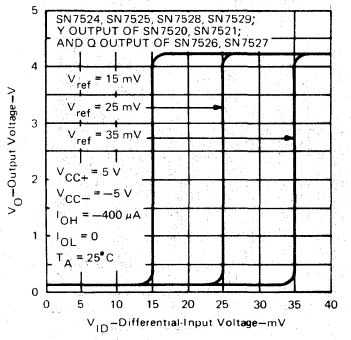

FIGURE 51

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

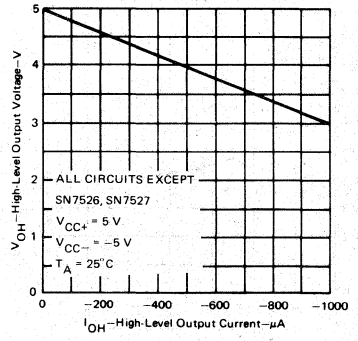

FIGURE 52

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

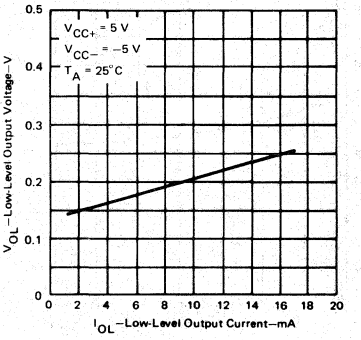

FIGURE 53

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TYPICAL APPLICATIONS

small memory systems

This application demonstrates an improved method of sensing data from relatively small memory systems. Two individual core planes, usually consisting of 4096 cores each, can be interfaced by each of the dual-channel SN7524 or SN7525 sense amplifiers, see Figure K. Standard TTL or DTL integrated circuits, driven directly from the compatible sense-amplifier outputs, may be selected to serve as the memory data register (MDR).

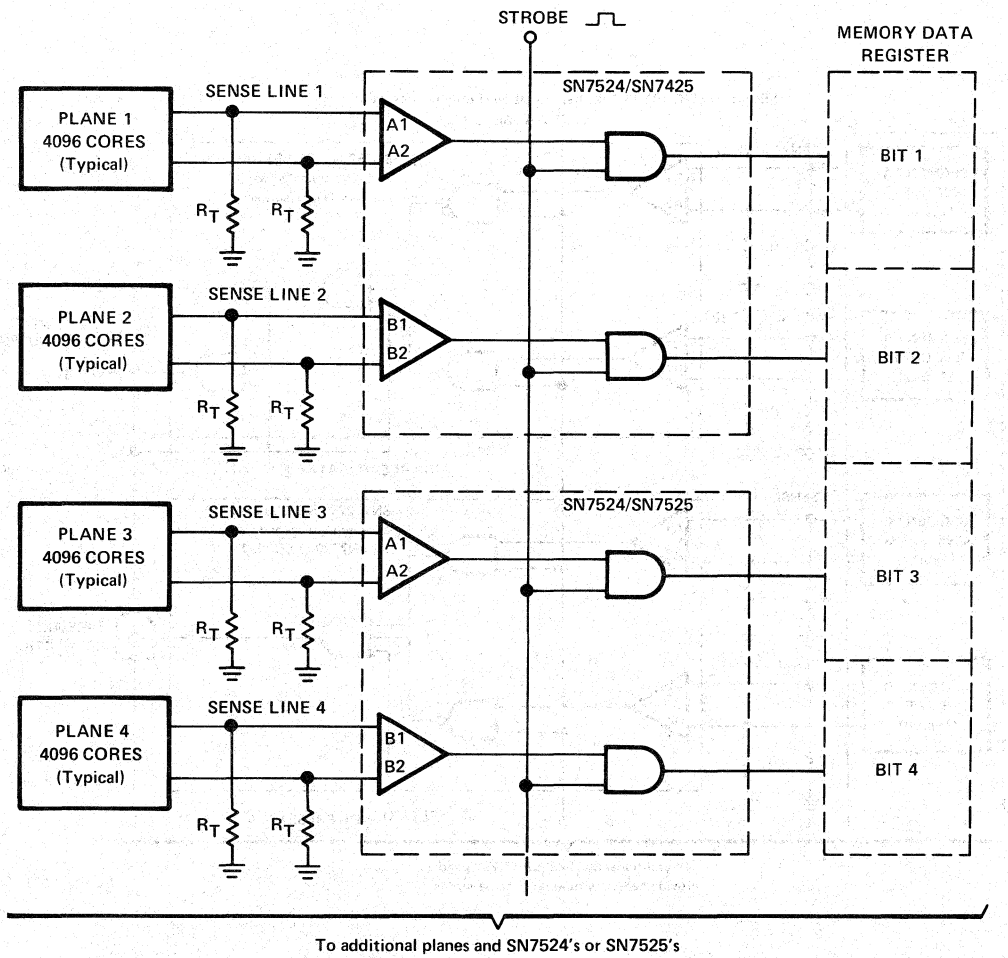

FIGURE K–SENSING SMALL MEMORY SYSTEMS

TYPICAL APPLICATIONS (continued)

large memory systems

This application demonstrates an improved method of sensing data from large memory systems. The signal-to-noise ratio can be increased by sectioning the large core planes as illustrated in Figure L. Two segments, usually consisting of 4096 cores each, can be interfaced by each of the dual-input channels of the SN7420/SN7421 or SN7422/SN7423 sense amplifiers. The cascaded output gates of the SN7520/SN7521 circuits may be connected to serve as the memory data register (MDR). A number of SN7522/SN7523 sense amplifiers may be wire-AND connected to expand the input function of the MDR to interface all the segments of the plane. Complementary outputs, clear, and preset functions are provided for the MDR. Rules for combined fan-out and wire-AND capabilities must be observed.

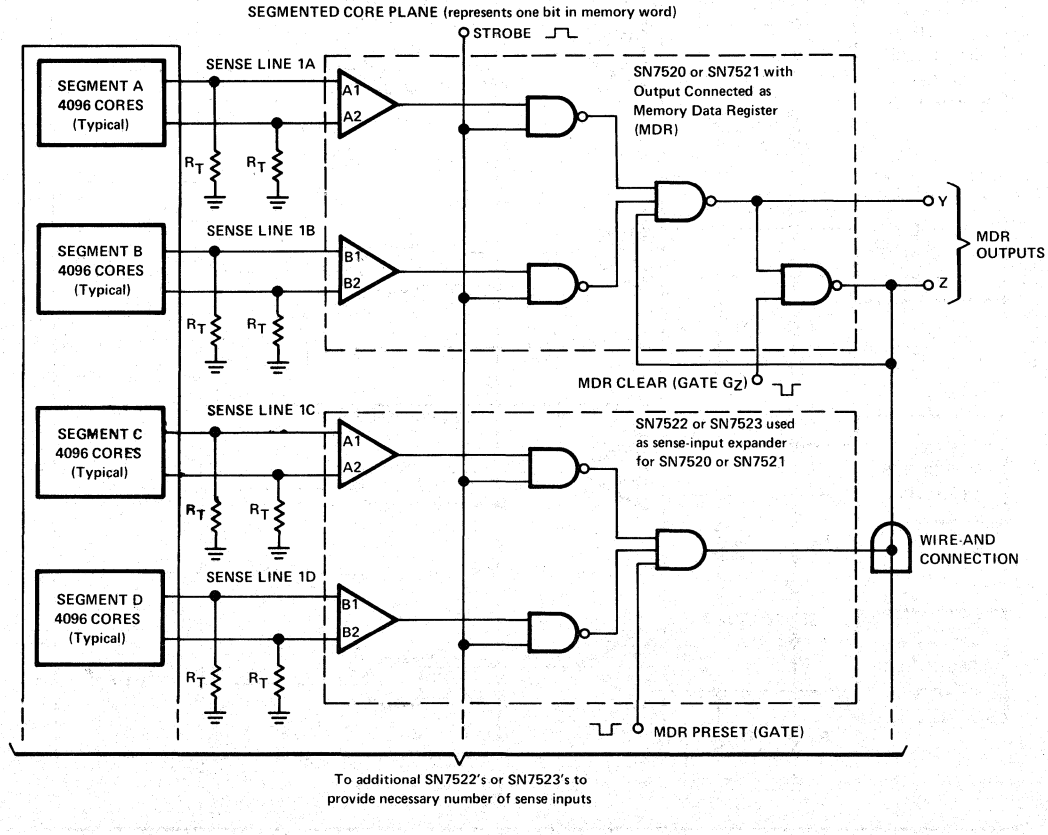

FIGURE L–SENSING LARGE MEMORY SYSTEMS

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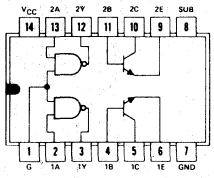
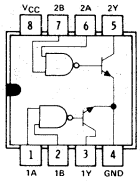
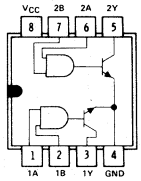
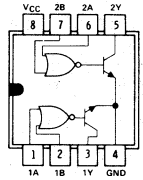
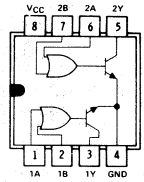
peripheral drivers

TYPE	SN75450A	SN75451A	SN75452	SN75453	SN75454
Block Diagrams		 Y = AB	 Y = $\overline{AB}$	 Y = A+B	 Y = $\overline{A+B}$
Features	Two TTL gates and two high current transistors on one chip. Each transistor sinks 300 mA of current and has a minimum collector-emitter breakdown voltage of 30 V.				
	• Two Uncommitted Transistors	• 8-pin Package	• AND Gates	• NOR Gates	• OR Gates
Applications	• Lamp Driver • Relay Driver • MOS Driver • Line Driver	• Lamp Driver • Relay Driver	• Lamp Driver • Relay Driver	• Lamp Driver • Relay Driver	• Lamp Driver • Relay Driver
Package	N	P	P	P	P

3

memory drivers

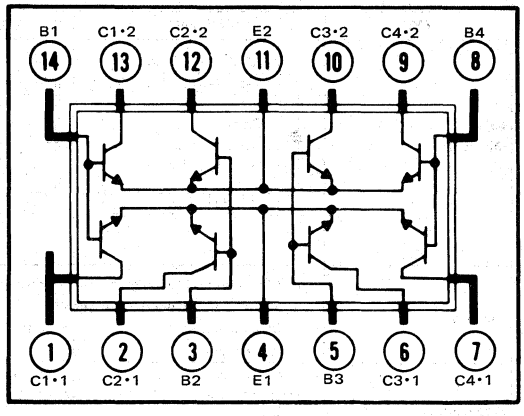
TYPE	SN75303 4 X 2 TRANSISTOR ARRAY	SN75308 2 X 4 TRANSISTOR ARRAY	SN75324 DRIVER WITH DECODE INPUTS	SN75325 DRIVER WITH DECODE INPUT
Features	• Eight 150-mA Monolithic Transistors • $V_{(BR)CBO}$ = 25 V Min • $V_{(BR)CEO}$ = 18 V Min • $V_{CE(sat)}$ = 0.75 V Max at I_C = 150 mA • t_{PHL} = 14 ns Typ • t_{PLH} = 18 ns Typ	• Eight 600-mA Monolithic Transistors • $V_{(BR)CBO}$ = 25 V Min • $V_{(BR)CEO}$ = 10 V Min • $V_{CE(sat)}$ = 0.55 V Typ at I_C = 500 mA • t_{on} = 36 ns Typ • t_{off} = 23 ns Typ	• Four 400-mA Transistors • TTL-Compatible Inputs • Internal Decoding and Timing Gates • Single 14-V Supply	• Four 600-mA Transistors • TTL-Compatible Inputs • Internal Decoding • 5-V Supply
Application	• Core Memories • Read-Only Memories	• Core Memories • Read-Only Memories • Plated-Wire Memories	• Core Memories	• Core Memories • Plated-Wire Memories • Hammer Driver
Package	N, S	J, N	N, S	J, N
Application Notes			CA-107: SN75324 Monolithic Memory Driver	

CIRCUIT TYPE SN75303
2 X 4 TRANSISTOR ARRAY

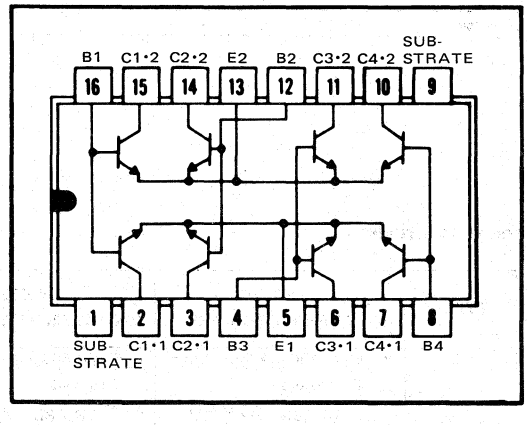
150-mA MEMORY DRIVER

- Maximum $V_{CE(sat)}$ of 750 mV at 150 mA I_C
- Maximum V_{BE} of 1.1 V at 150 mA I_C
- Minimum h_{FE} of 15 at 150 mA I_C

S FLAT PACKAGE (TOP VIEW)



N DUAL-IN-LINE PACKAGE (TOP VIEW)



3 **description**

Each SN75303 is a monolithic array of eight n-p-n transistors designed for use in core, thin-film, and plated-wire memories as a medium-current word-line driver. Selection is by base-emitter activation. The SN75303 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Collector-base voltage	25 V
Collector-emitter voltage (see Note 1)	18 V
Emitter-base voltage	5 V
Continuous collector current	200 mA
Continuous total package dissipation	250 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: This value applies when the base-emitter diode is open-circuited.

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electrical characteristics at 25°C free-air temperature (unless otherwise noted)†

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$V_{(BR)CBO}$	Collector-base breakdown voltage	I_C = 10 μA,	I_E = 0		25			V
$V_{(BR)CEO}$	Collector-emitter breakdown voltage	I_C = 10 mA,	I_B = 0,	See Note 2	18			V
$V_{(BR)CES}$	Collector-emitter breakdown voltage	I_C = 1 mA,	V_{BE} = 0		25			V
$V_{(BR)EBO}$	Emitter-base breakdown voltage	I_E = 10 μA,	I_C = 0		5			V
h_{FE}	Static forward current transfer ratio	V_{CE} = 2 V,	I_C = 30 mA	See Note 2	20	35		
		V_{CE} = 2 V, T_A = 0°C	I_C = 30 mA,		15			
		V_{CE} = 2 V,	I_C = 150 mA		15	25		
V_{BE}	Base-emitter voltage	I_B = 3 mA,	I_C = 30 mA	See Note 2	0.7	0.8	0.9	V
		I_B = 3 mA, T_A = 0°C to 70°C	I_C = 30 mA,		0.65		0.95	
		I_B = 15 mA,	I_C = 150 mA		0.8	1	1.1	
$V_{CE(sat)}$	Collector-emitter saturation voltage	I_B = 3 mA,	I_C = 30 mA	See Note 2		0.2	0.4	V
		I_B = 3 mA, T_A = 70°C	I_C = 30 mA,				0.45	
		I_B = 15 mA,	I_C = 150 mA			0.5	0.75	
C_{obo}	Common-base open-circuit output capacitance (1 transistor)	V_{CB} = 5 V, See Note 3	I_E = 0,	f = 140 kHz,		5		pF
C_{ibo}	Common-base open-circuit input capacitance (4 transistors in parallel)	V_{EB} = 0.5 V, See Note 4	I_C = 0,	f = 140 kHz,		40		pF

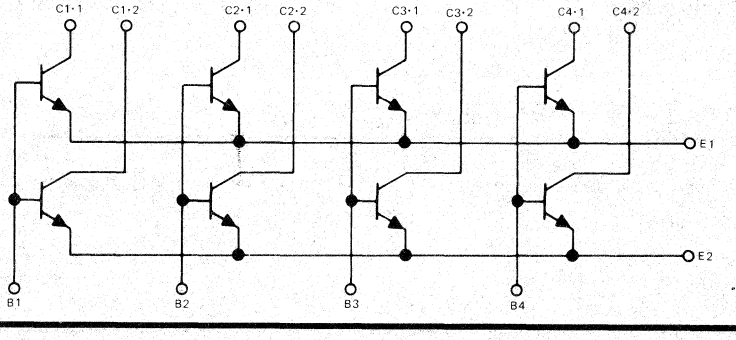
NOTES: 2. These parameters must be measured using pulse techniques, t_w = 300 μs, duty cycle ≤ 2%.
3. For measuring C_{obo}, the emitter of the transistor under test and all terminals of the other transistors are open.
4. For measuring C_{ibo}, the four base terminals are connected in parallel. The emitter terminal of the transistors not under test and all the collector terminals are open.

switching characteristics at 25°C free-air temperature†

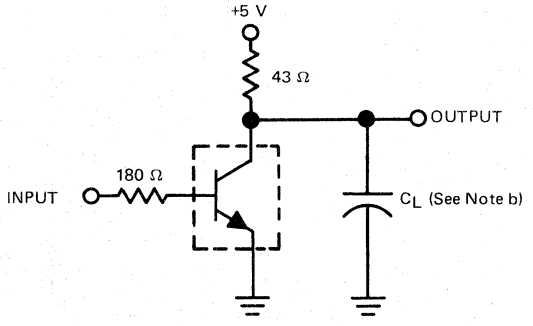
PARAMETER		TEST CONDITIONS‡			MIN	TYP	MAX	UNIT
t_{THL}	Transition time, high-to-low-level output	I_C = 100 mA,	$I_{B(1)}$ = 10 mA,			8	12	ns
t_{PHL}	Propagation delay time, high-to-low-level output	$V_{BE(off)}$ = 0, C_L ≤ 15 pF,	R_L = 43 Ω, See Figure 1			14	22	
t_{TLH}	Transition time, low-to-high-level output	I_C = 100 mA,	$I_{B(1)}$ = 10 mA,			6	12	ns
t_{PLH}	Propagation delay time, low-to-high-level output	$I_{B(2)}$ = −10 mA, C_L ≤ 15 pF,	R_L = 43 Ω, See Figure 2			18	30	

†Test conditions and limits apply separately to each transistor unless otherwise noted. The terminals of the transistors not under test are open during the measurement of these characteristics.
‡Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

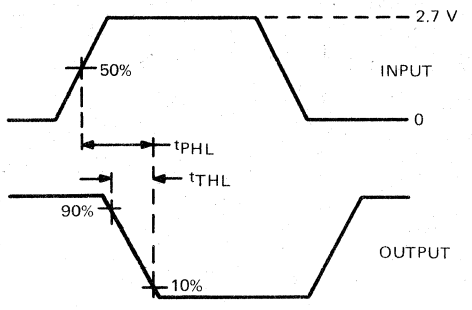
schematic



PARAMETER MEASUREMENT INFORMATION

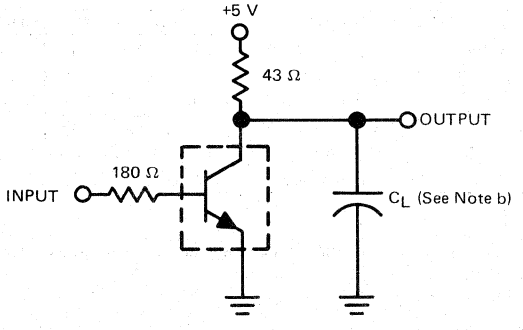


TEST CIRCUIT

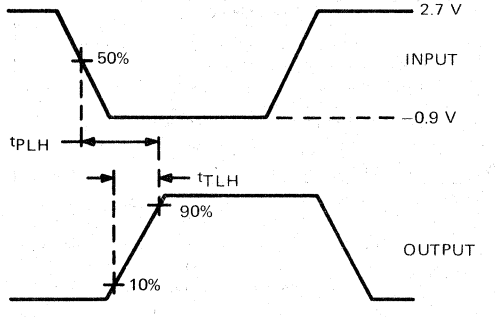


VOLTAGE WAVEFORMS

FIGURE 1–t_{THL} and t_{PHL}



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 2–t_{TLH} and t_{PLH}

NOTES: a. The input waveforms are supplied by a generator with the following characteristics: $Z_{out} = 50\ \Omega$, $t_r \leq 2$ ns, $t_w \approx 70$ ns, duty cycle ≤ 2%.
b. C_L includes probe and jig capacitance.

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TYPICAL CHARACTERISTICS

BASE-EMITTER VOLTAGE
vs
COLLECTOR CURRENT

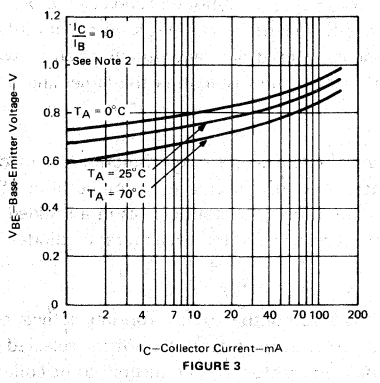

FIGURE 3

COLLECTOR-EMITTER SATURATION VOLTAGE
vs
COLLECTOR CURRENT

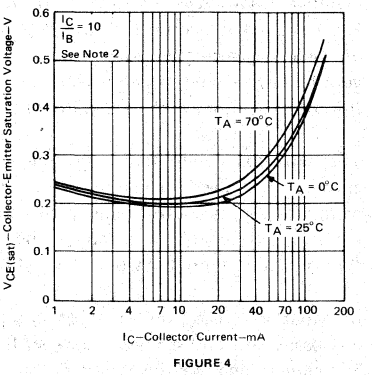

FIGURE 4

STATIC FORWARD
CURRENT TRANSFER RATIO
vs
COLLECTOR CURRENT

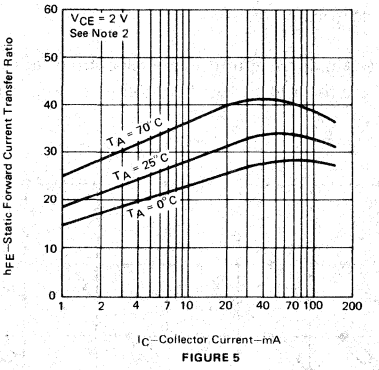

FIGURE 5

TURN-ON TIME
vs
FREE-AIR TEMPERATURE

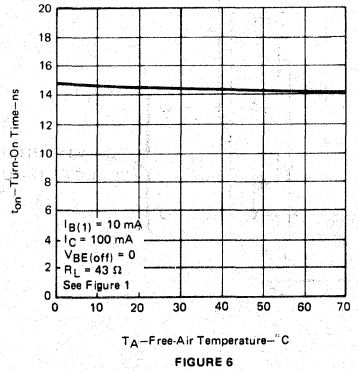

FIGURE 6

TURN-OFF TIME
vs
FREE-AIR TEMPERATURE

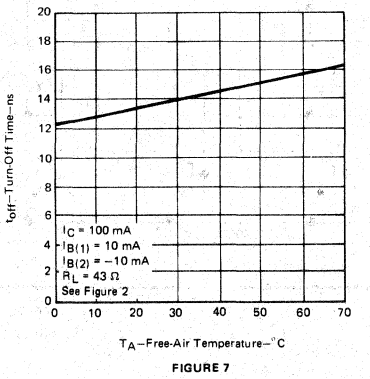

FIGURE 7

NOTE 2: These parameters must be measured using pulse techniques, t_w = 300 μs, duty cycle ≤ 2%.

TYPICAL APPLICATION DATA

Use of the SN75303 in High-Speed Read-Only Memories

Significant advantages result from the use of a high-speed, read-only memory (ROM) in computers and calculators. This ROM is used for control, as a function generator, or for performing highly repetitive routines such as multiplying, dividing , or calculating square roots. The read-only memory has permanently stored data and usually operates with a very fast cycle time. It can perform repetitive operations much more efficiently and faster than the larger and slower read-write memory in the computer or calculator.

The SN75303 two-by-four transistor array is designed to perform the word-line drive or select function for medium current, high-speed, read-only memories organized in the word-oriented (2D) or linear-select configuration. Such memories use magnetic memory elements such as plated wires, planar thin-films, transformers (as in a braided-wire memory), or ferrite switch cores. They also may utilize passive elements such as resistors, capacitors, or diodes. The typical organization of a word-oriented ROM is shown in the figure below.

Information is read from the ROM by selecting the desired word line. This is accomplished by appropriate activiation of one base-select and one emitter-select line. The transistor in the SN75303 array at the intersection of the selected base and emitter lines will be activated, thus sinking current from the word-line load resistor, R_L, connected to its collector. Energy is coupled from the selected word line to the sense lines by the memory elements (ME) located at the intersections of the word line and the sense lines. The presence of an ME can represent a stored logic 1 bit of information while the absence of an ME represents a stored logic 0 bit. (The desired information is stored in such a memory during fabrication and is not electrically alterable.)

The stored word is read out at the sense-amplifier outputs. The selection of a sense amplifier will depend on the type of ME used in the memory and may take the form of a special amplifier, a comparator, or a logic gate.

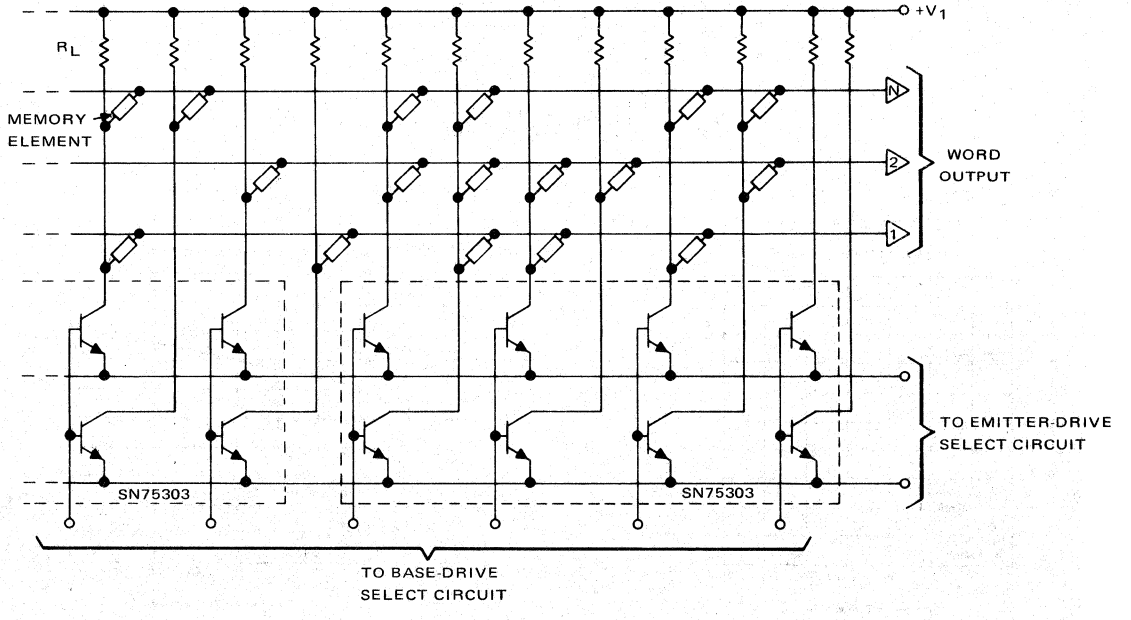

FIGURE 8

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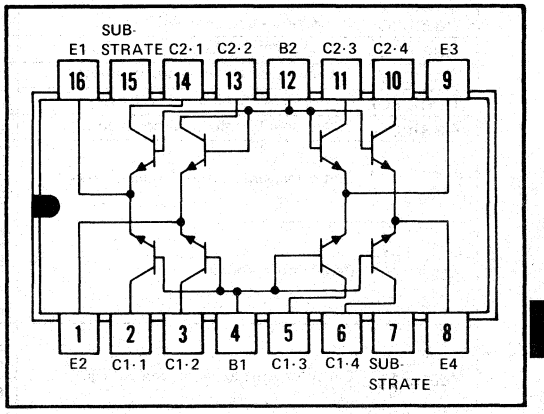
CIRCUIT TYPE SN75308
2 X 4 TRANSISTOR ARRAY

- For High-Current Switching . . . to 600 mA Rated Collector Current
- Low Storage Time . . . 13 ns Typical
- Cross-Coupled Bases and Emitters Arranged for Selection

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



description

The SN75308 is an array of eight high-current (600 mA max) n-p-n transistors designed for use in linear select (2D) memory designs utilizing ferrite cores, plated wire, planar film, diodes, resistors, or other memory elements. One of eight transistors can be switched by selection of the appropriate base and emitter inputs. Drive of the base and emitter inputs can be provided by available circuits such as the SN7440, SN75450, and SN75451. The SN75308 transistors feature fast switching times.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Collector-base voltage	25 V
Collector-emitter voltage (see Note 1)	25 V
Collector-emitter voltage (see Note 2)	10 V
Emitter-base voltage	4.5 V
Continuous current, each collector	600 mA
Continuous total package dissipation (see Note 3)	800 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTES: 1. This value applies when the base-emitter diode is short-circuited.
2. This value applies between 100 μA and 10 mA collector current when the base-emitter diode is open-circuited.
3. This value applies for any combination provided the ratings of single transistors are not exceeded.

electrical characteristics for each transistor at 25°C free-air temperature †

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$V_{(BR)CBO}$	Collector-base breakdown voltage	I_C = 100 μA,	I_E = 0		25			V
$V_{(BR)CEO}$	Collector-emitter breakdown voltage	I_C = 10 mA,	I_B = 0,	See Note 4	10			V
$V_{(BR)CES}$	Collector-emitter breakdown voltage	I_C = 100 μA,	V_{BE} = 0		25			V
$V_{(BR)EBO}$	Emitter-base breakdown voltage	I_E = 100 μA,	I_C = 0		5			V
$V_{(BR)CU}$	Collector-substrate breakdown voltage	I_C = 100 μA,	I_B = 0,	I_E = 0	25			V
h_{FE}	Static forward current transfer ratio	V_{CB} = 1 V,	I_E = 30 mA	See Note 4	15			
		V_{CB} = 1 V,	I_E = 100 mA		20			
		V_{CB} = 1 V,	I_E = 500 mA		20			
V_{BE}	Base-emitter voltage	I_B = 3 mA,	I_C = 30 mA	See Note 4		0.73	1	V
		I_B = 10 mA,	I_C = 100 mA			0.82	1.1	
		I_B = 30 mA,	I_C = 300 mA			1.0	1.2	
		I_B = 50 mA,	I_C = 500 mA			1.1	1.3	
$V_{CE(sat)}$	Collector-emitter saturation voltage	I_B = 3 mA,	I_C = 30 mA	See Note 4		0.15	0.3	V
		I_B = 10 mA,	I_C = 100 mA			0.2	0.4	
		I_B = 30 mA,	I_C = 300 mA			0.36	0.6	
		I_B = 50 mA,	I_C = 500 mA			0.55	0.8	
$\lvert h_{fe} \rvert$	Small-signal common-emitter forward current transfer ratio	V_{CE} = 10 V,	I_C = 100 mA,	f = 100 MHz		2		
C_{obo}	Common-base open-circuit output capacitance (1 transistor)	V_{CB} = 10 V,	I_E = 0,	f = 140 kHz, See Note 5		18		pF
C_{ibo}	Common-base open-circuit input capacitance (2 transistors in parallel)	V_{EB} = 0.5 V,	I_C = 0,	f = 140 kHz, See Note 6		65		pF

NOTES: 4. These parameters must be measured using pulse techniques. t_w = 200 μs, duty cycle ⩽ 2%.
5. For measuring C_{obo}, the emitter terminal of the transistor under test and all terminals of the other transistors are open.
6. For measuring C_{ibo}, the base terminals are connected in parallel. The emitter terminals of the transistors not under test and all the collector terminals are open.

switching characteristics at 25°C free-air temperature†

PARAMETER		TEST CONDITIONS‡			TYP	UNIT
t_d	Delay time	I_C = 500 mA,	$I_{B(1)}$ = 50 mA,		16	ns
t_r	Rise time	$V_{BE(off)}$ = −0.9 V,	R_L = 28.7 Ω,		20	
t_{on}	Turn-on time	C_L = 15 pF,	See Figure 1		36	
t_s	Storage time	I_C = 500 mA,	$I_{B(1)}$ = 50 mA,		13	
t_f	Fall time	$I_{B(2)}$ = −50 mA,	R_L = 28.7 Ω,		10	
t_{off}	Turn-off time	C_L = 15 pF,	See Figure 1		23	

†Test conditions and limits apply separately to each transistor unless otherwise noted. The terminals of the transistors not under test are open during the measurement of these characteristics.

‡Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

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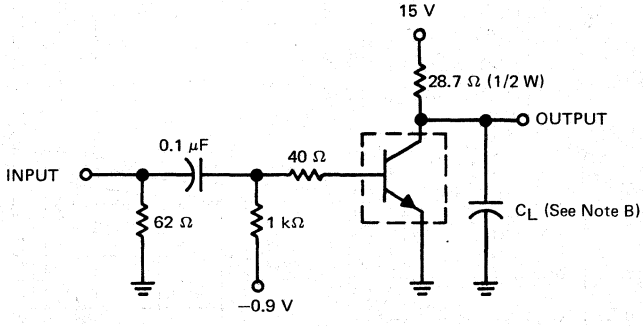
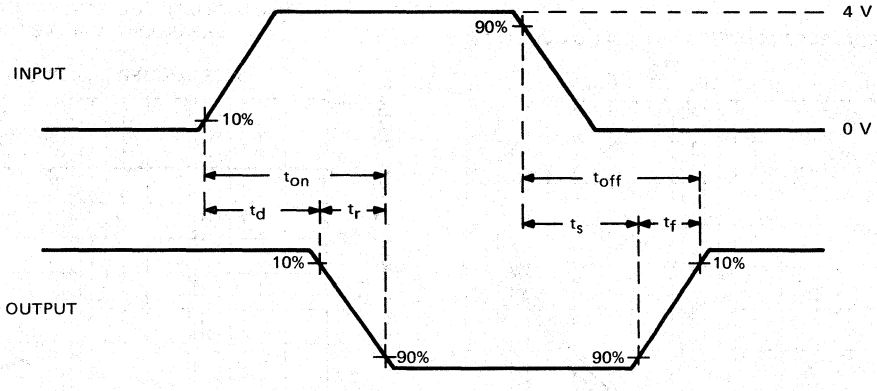
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The input waveform is supplied by a generator with the following characteristics: Z_{out} = 50 Ω, $t_r \leq$ 10 ns, $t_f \leq$ 10 ns, $t_w \approx$ 100 ns, duty cycle ≤ 2%.
B. C_L includes probe and jig capacitance.

FIGURE 1—SWITCHING CHARACTERISTICS

TYPICAL CHARACTERISTICS

STATIC FORWARD CURRENT TRANSFER RATIO
vs
EMITTER CURRENT

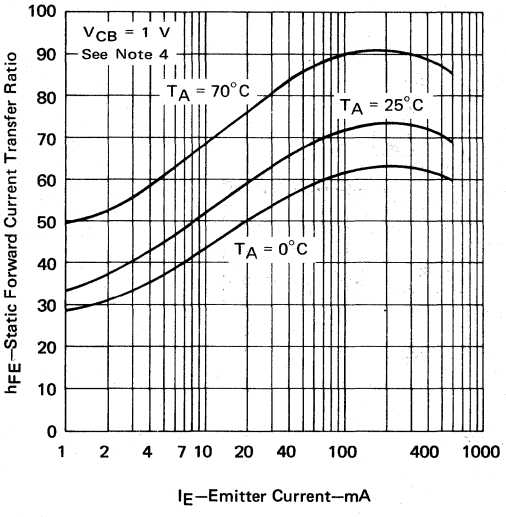


FIGURE 2

BASE-EMITTER VOLTAGE
vs
COLLECTOR CURRENT

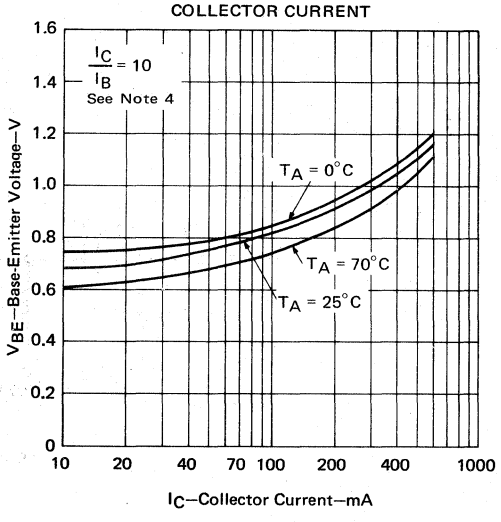


FIGURE 3

COLLECTOR-EMITTER SATURATION VOLTAGE
vs
COLLECTOR CURRENT

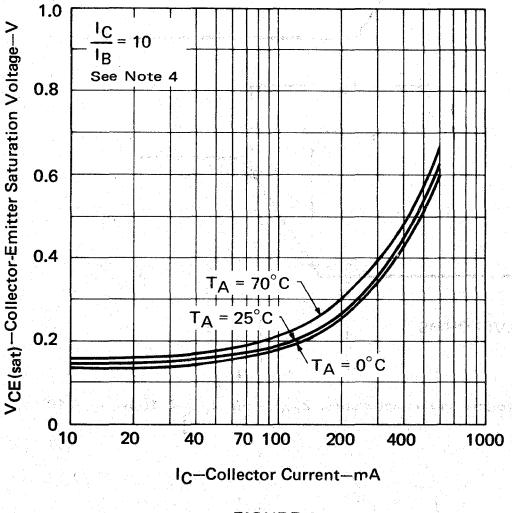


FIGURE 4

NORMALIZED COLLECTOR-EMITTER
BREAKDOWN VOLTAGE
vs
BASE-EMITTER RESISTANCE

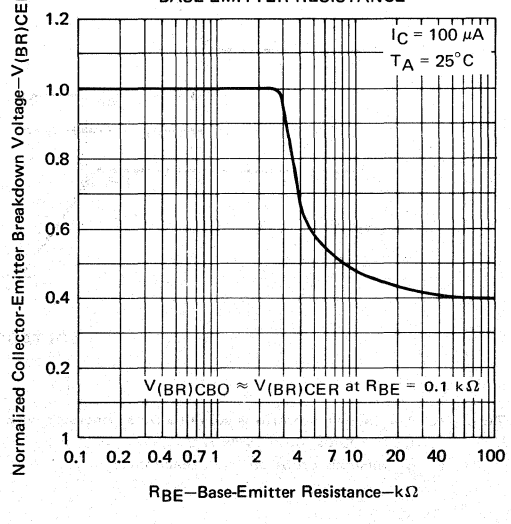


FIGURE 5

NOTE 4: These parameters must be measured using pulse techniques. t_w = 200 μs, duty cycle ≤ 2%.

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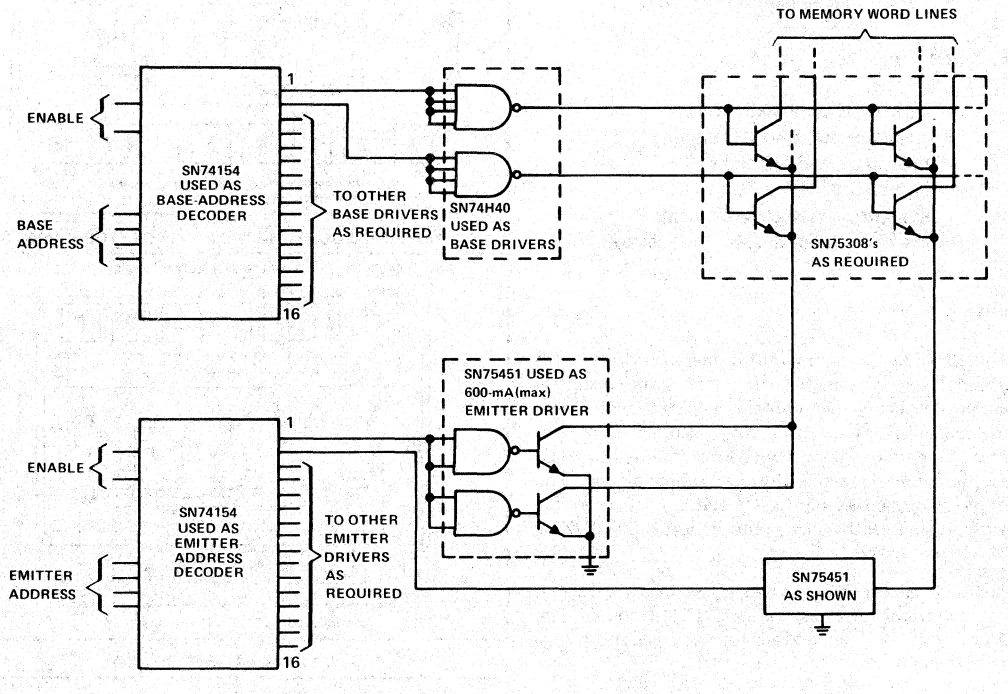
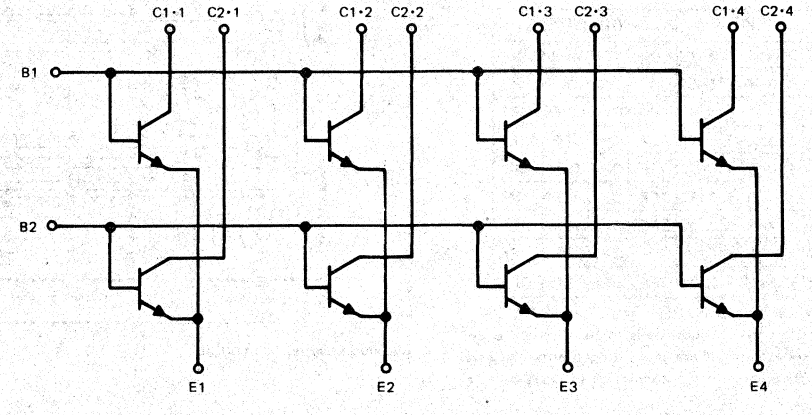
TYPICAL APPLICATION DATA

The SN75308 two-by-four transistor array is designed to perform the word-line drive or select function for medium current, high-speed, read-only memories organized in the word-oriented (2D) or linear-select configuration. Such memories use magnetic memory elements such as plated wires, planar thin-films, transformers (as in a braided-wire memory), or ferrite switch cores. They also may utilize passive elements such as resistors, capacitors, or diodes. The typical organization of a word-oriented ROM is shown on the SN75303 data sheet; a base and emitter selection technique is shown below. A similar selection circuit can be used with the SN75303 although with it the SN75451's need not be paralleled.



3

schematic



CIRCUIT TYPE SN75324
MEMORY DRIVER WITH DECODE INPUTS

SERIES 75 MEMORY DRIVER

PERFORMANCE

- fast switching times
- 400-mA output capability
- internal decoding and timing circuitry
- dual sink/source outputs
- output short-circuit protection

EASE OF DESIGN

- TTL or DTL compatibility
- eliminates transformer coupling
- reduces drive-line lengths
- increases reliability
- minimizes external components
- choice of flat or dual-in-line packages

description

The SN75324 is a monolithic memory driver with decode inputs designed for use with magnetic memories. The device contains two 400-milliampere (source/sink) switch pairs, with decoding capability from four address lines. Two address inputs (B and C) are used for mode selection, i.e., source or sink. The other two address inputs (A and D) are used for switch-pair selection, i.e., output switch-pair Y/Z or W/X respectively.

The sink circuit is composed of an inverting switch with a transistor-transistor-logic (TTL) input. The source circuit is an emitter-follower driven from a TTL input stage.

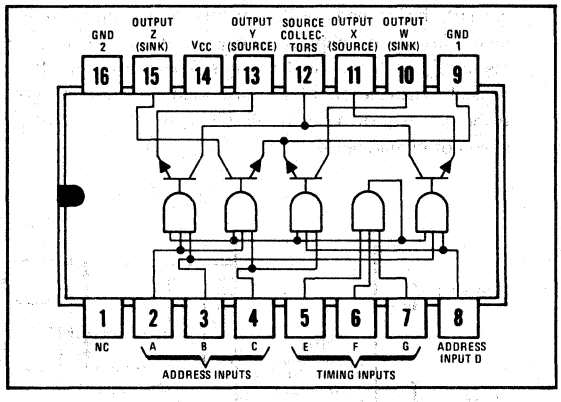
The SN75324 is characterized for operation from 0°C to 70°C.

TRUTH TABLE

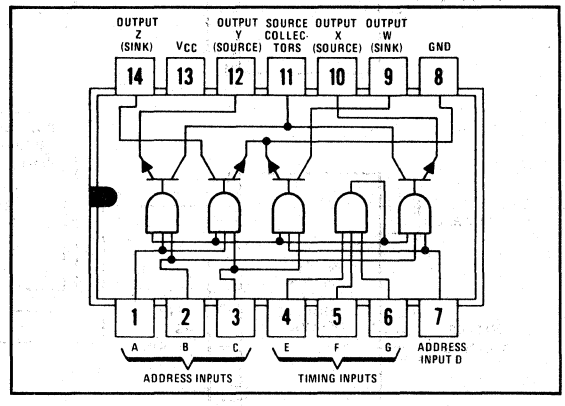
INPUTS							OUTPUTS			
ADDRESS				TIMING			SINK	SOURCES		SINK
A	B	C	D	E	F	G	W	X	Y	Z
0	0	1	1	1	1	1	ON	OFF	OFF	OFF
0	1	0	1	1	1	1	OFF	ON	OFF	OFF
1	1	0	0	1	1	1	OFF	OFF	ON	OFF
1	0	1	0	1	1	1	OFF	OFF	OFF	ON
X	X	X	X	0	X	X	OFF	OFF	OFF	OFF
X	X	X	X	X	0	X	OFF	OFF	OFF	OFF
X	X	X	X	X	X	0	OFF	OFF	OFF	OFF

NOTES: 1. X = Logical 1 or logical 0.
2. Not more than one output is to be allowed to be ON at one time: When all timing inputs are at a logical 1, two of the address inputs must be at a logical 0.

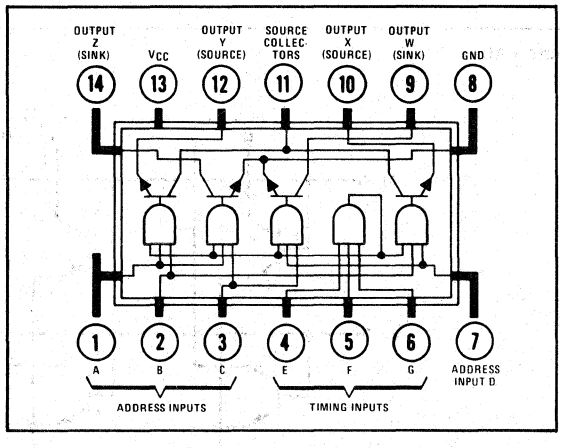
J CERAMIC DUAL-IN-LINE PACKAGE (TOP VIEW)



N PLASTIC DUAL-IN-LINE PACKAGE (TOP VIEW)



S FLAT PACKAGE (TOP VIEW)



NC—No internal connection
GND 1 and GND 2 are to be used in parallel

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logic definition

Standard positive logic applies with the following definitions used for specifying digital-level signals:

LOW VOLTAGE = LOGICAL 0
HIGH VOLTAGE = LOGICAL 1

absolute maximum ratings over operating case temperature range (unless otherwise noted)

Supply voltage V_{CC} (See Note 1) . . . . . 17 V
Input voltage (See Note 2) . . . . . 5.5 V
Operating case temperature range . . . . . 0°C to 70°C
Continuous total power dissipation at (or below) 70°C case temperature . . . . . 800 mW
Storage temperature range . . . . . -65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

electrical characteristics (unless otherwise noted, V_{CC} = 14 V, T_C = 0°C to 70°C)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input	1		3.5			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input	1				0.8	V
$I_{in(1)}$	Logical 1 level address input current	1	V_{in} = 5 V			200	μA
$I_{in(1)}$	Logical 1 level timing input current	1	V_{in} = 5 V			100	μA
$I_{in(0)}$	Logical 0 level address input current	1	V_{in} = 0 V			-6	mA
$I_{in(0)}$	Logical 0 level timing input current	1	V_{in} = 0 V			-12	mA
$V_{(sat)}$	Sink saturation voltage	2	$I_{sink} \simeq$ 420 mA, R_L = 53 Ω		0.75	0.85	V
$V_{(sat)}$	Source saturation voltage	2	$I_{source} \simeq$ -420 mA, R_L = 47.5 Ω		0.75	0.85	V
I_{off}	Output reverse current (off state)	1	V_{in} = 0 V		125	200	μA
I_{CC}	Supply current, all sources and sinks off	3	V_{in} = 0 V		12.5	15	mA
I_{CC}	Supply current, either sink selected	4			30	40	mA
I_{CC}	Supply current, either source selected	4			25	35	mA

†These typical values are at T_C = 25°C.

switching characteristics, V_{CC} = 14 V, T_C = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{pd(1)}$	Propagation delay time to logical 1 level, source output	5	R_{L1} = 53 Ω, R_{L2} = 500 Ω, C_L = 20 pF			90	ns
$t_{pd(0)}$	Propagation delay time to logical 0 level, source output	5				50	ns
$t_{pd(1)}$	Propagation delay time to logical 1 level, sink output	6	R_L = 53 Ω, C_L = 20 pF			110	ns
$t_{pd(0)}$	Propagation delay time to logical 0 level, sink output	6				40	ns
t_s	Sink storage time	6				70	ns

3

thermal information

The SN75324 is designed to be used at a case temperature not to exceed 70°C. Under this condition, infrared microradiometer and X-ray studies indicate that a safe junction temperature is maintained under specified worst-case conditions.

SN75324 circuits should be mounted so that minimum thermal resistance is achieved. A thermal compound should be used between the bottom of the flat S package and a heat sink. This, in conjunction with unrestricted forced-air flow across the heat sink and package, has been found to adequately satisfy thermal requirements. No thermal compound is required with the dual-in-line package. Air flow should be across the short dimension of either package.

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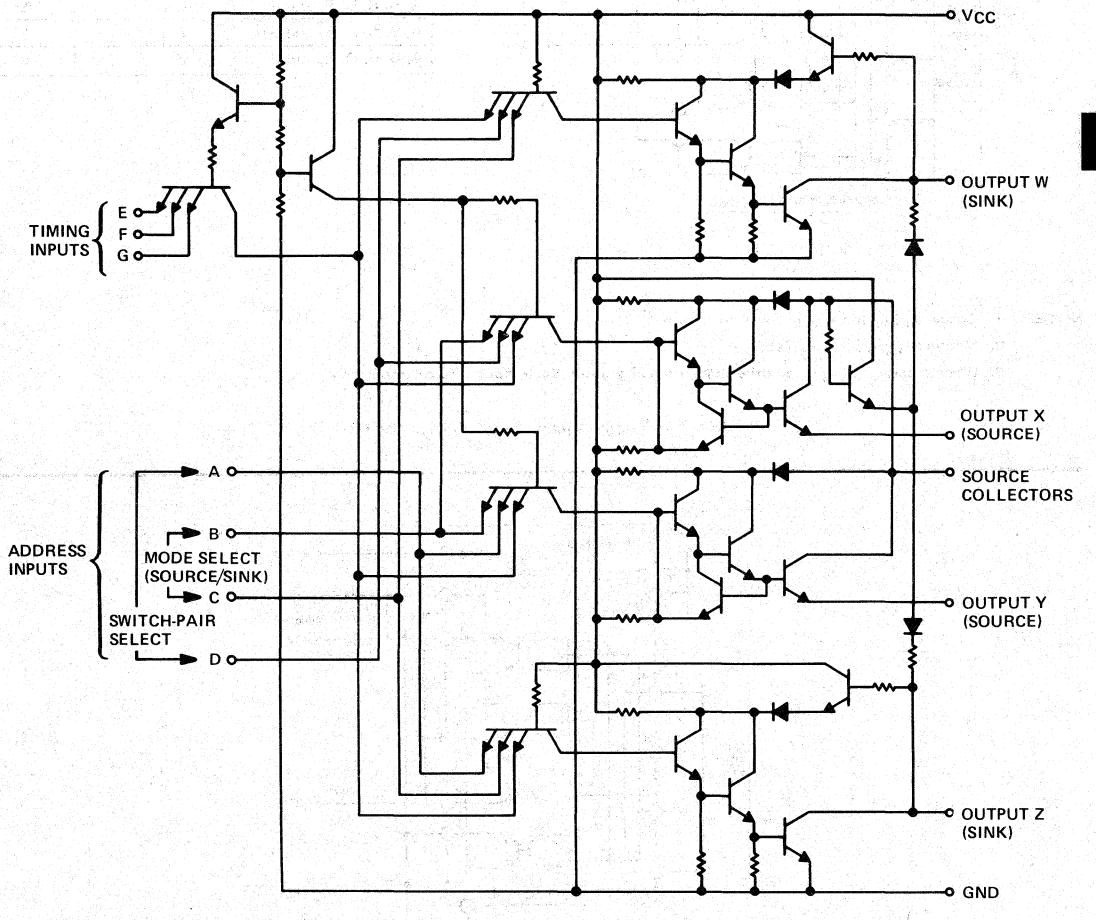
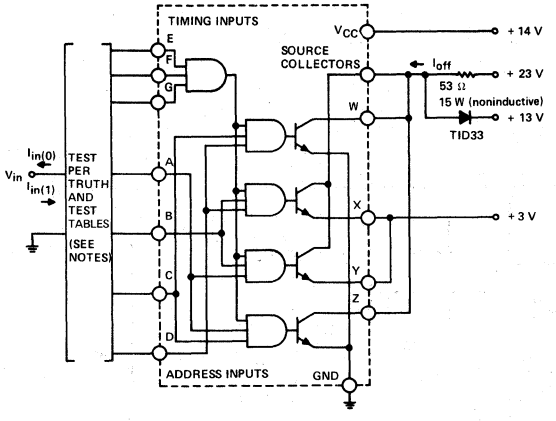
schematic


VCC
OUTPUT W
(SINK)
TIMING
INPUTS
E
F
G
OUTPUT X
(SOURCE)
SOURCE
COLLECTORS
A
B
C
D
ADDRESS
INPUTS
MODE SELECT
(SOURCE/SINK)
SWITCH-PAIR
SELECT
OUTPUT Y
(SOURCE)
OUTPUT Z
(SINK)
GND

PARAMETER MEASUREMENT INFORMATION

d-c test circuits†

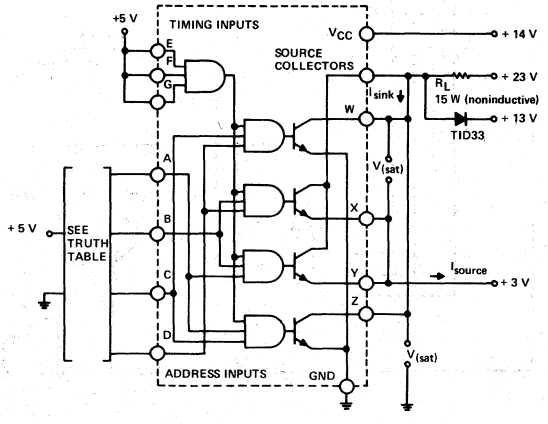


TEST TABLE FOR $I_{in(0)}$

APPLY 3.5 V	GROUND	TEST $I_{in(0)}$
B, C, E, F, and G	A and D	A
B, C, E, F, and G	A and D	D
A, D, E, F, and G	B and C	B
A, D, E, F, and G	B and C	C
A, B, C, D, F, and G	E	E
A, B, C, D, E, and G	F	F
A, B, C, D, E, and F	G	G

NOTES: 1. Check $V_{in(1)}$ and $V_{in(0)}$ per Truth Table.
2. Measure $I_{in(0)}$ per Test Table.
3. When measuring $I_{in(1)}$, all other inputs are at ground. Each input is tested separately.

FIGURE 1 – $V_{in(0)}$, $V_{in(1)}$, $I_{in(0)}$, $I_{in(1)}$, and I_{off}



NOTE: This parameter must be measured using pulse techniques. t_p = 500 ns, duty cycle ⩽ 1%.

FIGURE 2 – $V_{(sat)}$

† Arrows indicate actual direction of current flow.

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PARAMETER MEASUREMENT INFORMATION

d-c test circuits † (continued)

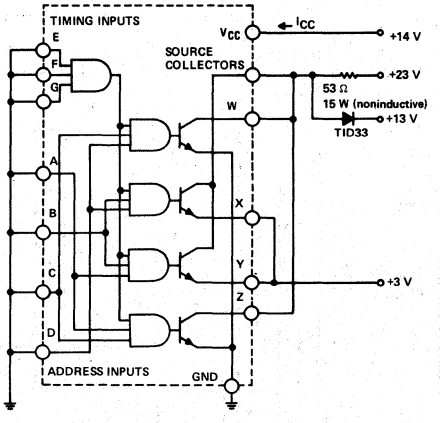
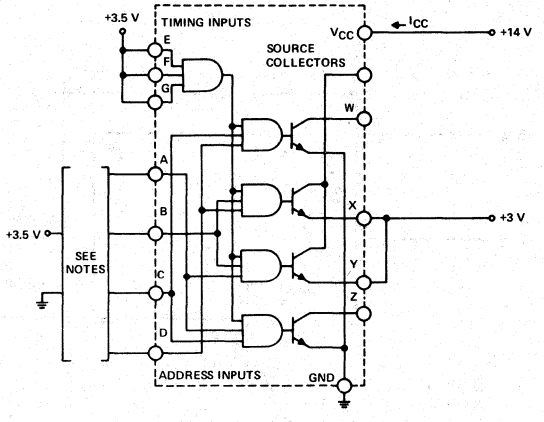


FIGURE 3 – I_{CC} (ALL OUTPUTS OFF)



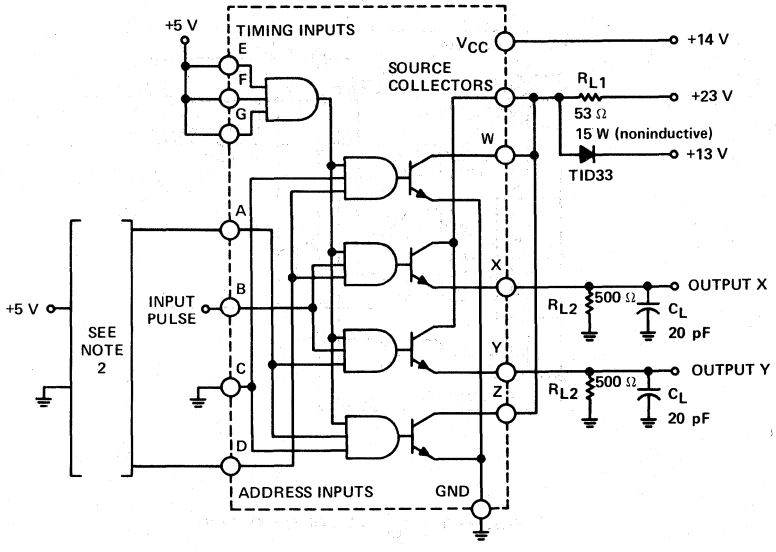
NOTES: 1. Ground A and B, apply 3.5 V to C and D, and measure I_{CC} (output W is on).
2. Ground B and D, apply 3.5 V to A and C, and measure I_{CC} (output Z is on).
3. Ground A and C, apply 3.5 V to B and D, and measure I_{CC} (output X is on).
4. Ground C and D, apply 3.5 V to A and B, and measure I_{CC} (output Y is on).

FIGURE 4 – I_{CC} (ONE OUTPUT ON)

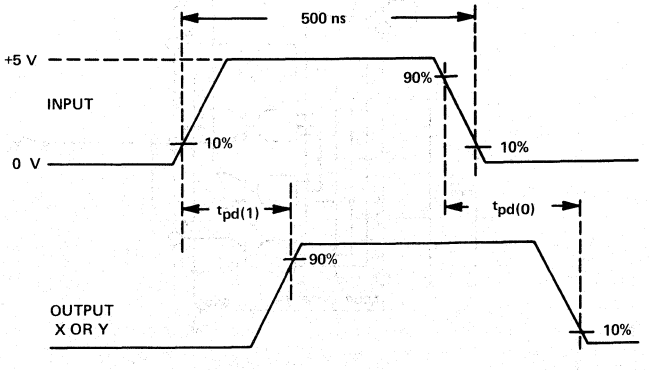
† Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST TABLE



VOLTAGE WAVEFORMS

NOTES: 1. The input waveform is supplied by a generator with the following characteristics: $t_r = t_f = 10$ ns, duty cycle $\leqslant 1\%$, and $Z_{out} \approx 50\ \Omega$.

2. When measuring delay times at output X, apply +5 V to input D, and ground A. When measuring delay times at output Y, apply +5 V to input A, and ground D.

3. C_L includes probe and jig capacitance.

4. Unless otherwise noted all resistors are 0.5 W.

FIGURE 5 – SOURCE-OUTPUT SWITCHING TIMES

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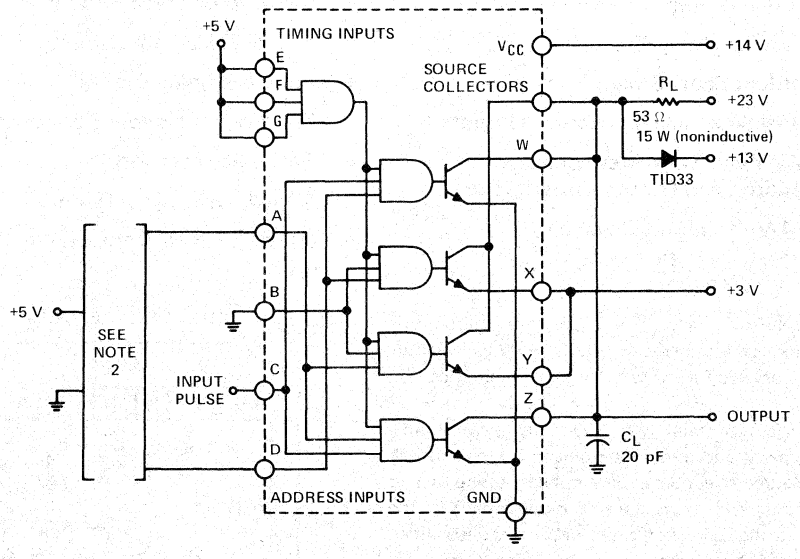
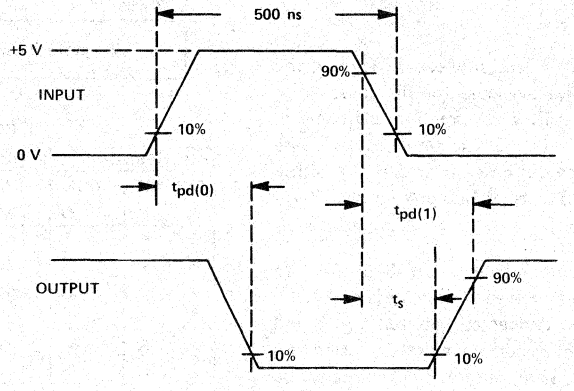
PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: 1. The input waveform is supplied by a generator with the following characteristics: $t_r = t_f = 10$ ns, duty cycle $\leqslant 1\%$, $Z_{out} \approx 50\ \Omega$.
2. When measuring delay times at output W, apply +5 V to input D, and ground A. When measuring delay times at output Z, apply +5 V to input A, and ground D.
3. C_L includes probe and jig capacitance.

FIGURE 6 – SINK-OUTPUT SWITCHING TIMES

CIRCUIT TYPES SN55325, SN75325
MEMORY DRIVERS

SERIES 55/75 MEMORY DRIVER
featuring

PERFORMANCE

- 600-mA Output Capability
- Fast Switching Times
- Output Short-Circuit Protection
- Dual Sink and Dual Source Outputs
- Minimum Time Skew between Address and Output Current Rise
- 24-Volt Output Capability

EASE OF DESIGN

- Source Base Drive Externally Adjustable
- TTL or DTL Compatibility
- Input Clamping Diodes
- Transformer Coupling Eliminated
- Reliability Increased
- Drive-Line Lengths Reduced
- Use of External Components Minimized

3

description

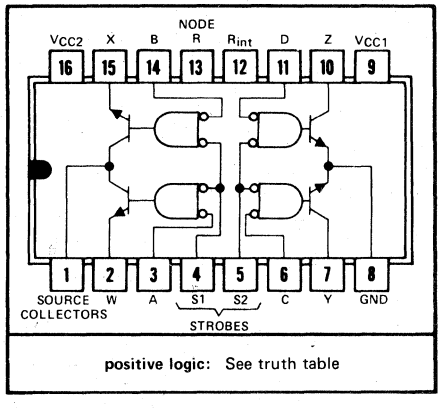
The SN55325 and SN75325 are monolithic integrated circuit memory drivers with logic inputs and are designed for use with magnetic memories.

The devices contain two 600-milliampere source-switch pairs and two 600-milliampere sink-switch pairs. Source selection is determined by one of two logic inputs, and source turn-on is determined by the source strobe. Likewise, sink selection is determined by one of two logic inputs, and sink turn-on is determined by the sink strobe. This arrangement allows selection of one of the four switches and its subsequent turn-on with minimum time skew of the output current rise.

When R_{int} and node R are connected together, the amount of base drive available for the source-1 or source-2 output transistor is set internally by a 575-ohm resistor. This method provides adequate base drive for source currents up to 375 mA with a V_{CC2} voltage of 15 volts or 600 mA with a V_{CC2} voltage of 24 volts.

When source currents greater than 375 mA are required, it is recommended that a resistor of the appropriate value be connected between V_{CC2} and node R and R_{int} must remain open. By using this method the source base current may usually be regulated within ±5%. An advantage of this method of setting the base drive is that the power dissipated by this resistor is external to the package and allows the integrated circuit to operate at higher source currents for a given junction temperature.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: See truth table

TRUTH TABLE

ADDRESS INPUTS				STROBE INPUTS		OUTPUTS			
SOURCE		SINK		SOURCE	SINK	SOURCE		SINK	
A	B	C	D	S1	S2	W	X	Y	Z
L	H	X	X	L	H	ON	OFF	OFF	OFF
H	L	X	X	L	H	OFF	ON	OFF	OFF
X	X	L	H	H	L	OFF	OFF	ON	OFF
X	X	H	L	H	L	OFF	OFF	OFF	ON
X	X	X	X	H	H	OFF	OFF	OFF	OFF
H	H	H	H	X	X	OFF	OFF	OFF	OFF

H = high level, L = low level, X = irrelevant
NOTE: Not more than one output is to be on at any one time.

Each sink-output collector has an internal pull-up resistor in parallel with a clamping diode connected to V_{CC2}. This arrangement provides protection from voltage surges associated with switching inductive loads.

The SN55325 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN75325 is characterized for operation from 0°C to 70°C.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN55325	SN75325	UNIT
Supply voltage V_{CC1} (see Note 1)		7	7	V
Supply voltage V_{CC2} (see Note 1)		25	25	V
Input voltage (any address or strobe input)		5.5	5.5	V
Continuous total dissipation at (or below) 70°C free-air temperature (see Note 2)		800	800	mW
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J Package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N Package	260	260	°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For operation of SN55325 above 70°C free-air temperature, refer to Dissipation Derating Curve, Figure 20.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

3

PARAMETER			TEST FIGURE	TEST CONDITIONS		SN55325 MIN	SN55325 TYP†	SN55325 MAX	SN75325 MIN	SN75325 TYP†	SN75325 MAX	UNIT
V_{IH}	High-level input voltage		1 & 2			2			2			V
V_{IL}	Low-level input voltage		3 & 4					0.8			0.8	V
V_I	Input clamp voltage		5	V_{CC1} = 4.5 V, I_I = −10 mA,	V_{CC2} = 24 V, T_A = 25°C		−1.3	−1.7		−1.3	−1.7	V
$I_{(off)}$	Source-collectors terminal off-state current		1	V_{CC1} = 4.5 V, V_{CC2} = 24 V	Full range			500			200	μA
					T_A = 25°C		3	150		3	200	
V_{OH}	High-level sink output voltage		2	V_{CC1} = 4.5 V, I_O = 0	V_{CC2} = 24 V,	19	23		19	23		V
$V_{(sat)}$	Saturation voltage‡	Source outputs	3	V_{CC1} = 4.5 V, V_{CC2} = 15 V, R_L = 24 Ω, $I_{(source)}$ ≈ −600 mA, See Note 3	Full range			0.9			0.9	V
					T_A = 25°C		0.43	0.7		0.43	0.75	
		Sink outputs	4	V_{CC1} = 4.5 V, V_{CC2} = 15 V, R_L = 24 Ω, $I_{(sink)}$ ≈ 600 mA, See Note 3	Full range			0.9			0.9	
					T_A = 25°C		0.43	0.7		0.43	0.75	
I_I	Input current at maximum input voltage	address inputs	5	V_{CC1} = 5.5 V, V_I = 5.5 V	V_{CC2} = 24 V,			1			1	mA
		strobe inputs						2			2	
I_{IH}	High-level input current	address inputs	5	V_{CC1} = 5.5 V, V_I = 2.4 V	V_{CC2} = 24 V,		3	40		3	40	μA
		strobe inputs					6	80		6	80	
I_{IL}	Low-level input current	address inputs	5	V_{CC1} = 5.5 V, V_I = 0.4 V	V_{CC2} = 24 V,		−1	−1.6		−1	−1.6	mA
		strobe inputs					−2	−3.2		−2	−3.2	
$I_{CC(off)}$	Supply current, all sources and sinks off	from V_{CC1}	6	V_{CC1} = 5.5 V, T_A = 25°C	V_{CC2} = 24 V,		14	22		14	22	mA
		from V_{CC2}					7.5	20		7.5	20	
I_{CC1}	Supply current from V_{CC1}, either sink on		7	V_{CC1} = 5.5 V, $I_{(sink)}$ = 50 mA,	V_{CC2} = 24 V, T_A = 25°C		55	70		55	70	mA
I_{CC2}	Supply current from V_{CC2}, either source on		8	V_{CC1} = 5.5 V, $I_{(source)}$ = −50 mA,	V_{CC2} = 24 V, T_A = 25°C		32	50		32	50	mA

†All typical values are at T_A = 25°C.
‡Not more than one output is to be on at any one time.
NOTE 3: These parameters must be measured using pulse techniques. t_w = 200 μs, duty cycle ≤ 2%.

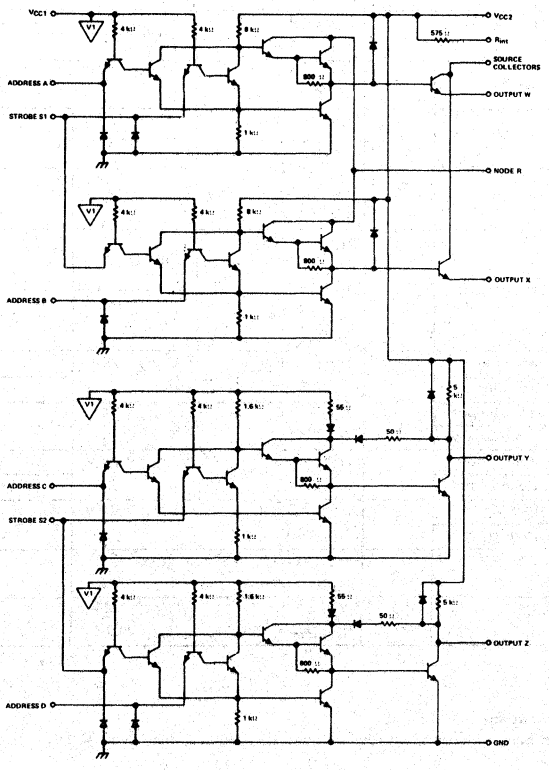
switching characteristics, V_{CC1} = 5 V, T_A = 25°C

PARAMETER¶	TO (OUTPUT)	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Source collectors	9	V_{CC2} = 15 V, R_L = 24 Ω, C_L = 25 pF		25	50	ns
t_{PHL}					25	50	
t_{TLH}	Source outputs	10	V_{CC2} = 20 V, R_L = 1 kΩ, C_L = 25 pF		55		ns
t_{THL}					7		
t_{PLH}	Sink outputs	9	V_{CC2} = 15 V, R_L = 24 Ω, C_L = 25 pF		20	45	ns
t_{PHL}					20	45	
t_{TLH}	Sink outputs	9	V_{CC2} = 15 V, R_L = 24 Ω, C_L = 25 pF		7	15	ns
t_{THL}					9	20	
t_s	Sink outputs	9	V_{CC2} = 15 V, R_L = 24 Ω, C_L = 25 pF		15	30	ns

3

¶ t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
t_{TLH} = transition time, low-to-high-level output
t_{THL} = transition time, high-to-low-level output
t_s = storage time

schematic

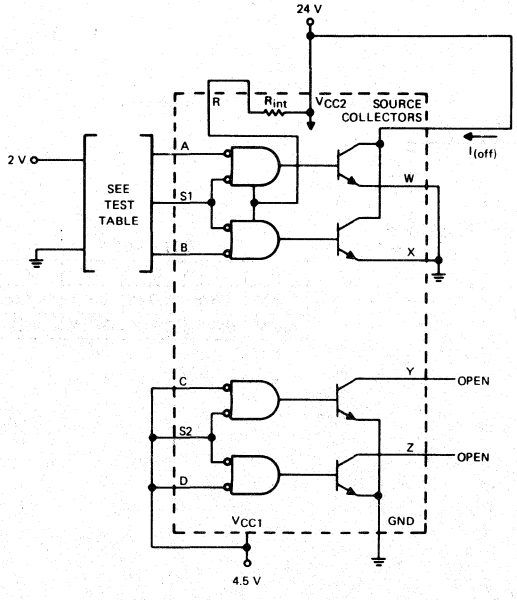


Component values shown are nominal.

V1 . . . V_{CC} bus

PARAMETER MEASUREMENT INFORMATION

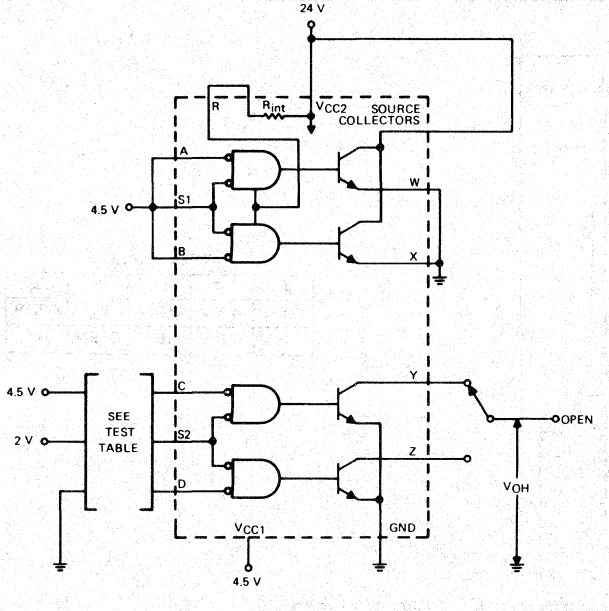
d-c test circuits†



TEST TABLE

A	B	S1
GND	GND	2 V
2 V	2 V	GND

FIGURE 1–$I_{(off)}$



TEST TABLE

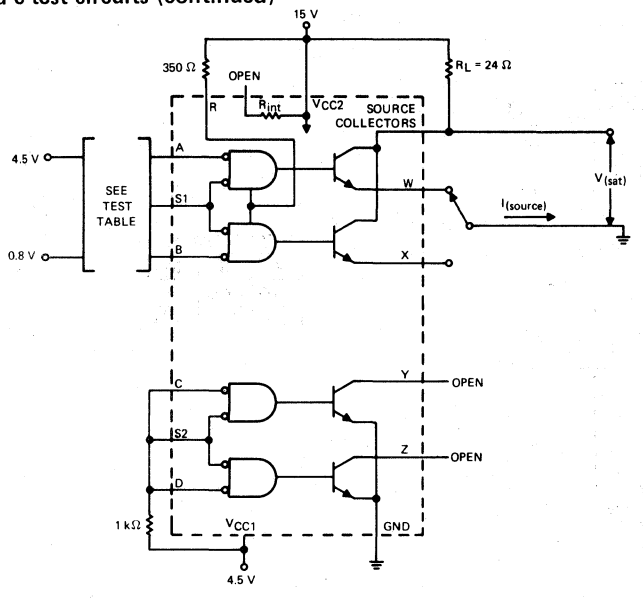
C	D	S2	Y	Z
2 V	4.5 V	GND	V_{OH}	OPEN
GND	4.5 V	2 V	V_{OH}	OPEN
4.5 V	2 V	GND	OPEN	V_{OH}
4.5 V	GND	2 V	OPEN	V_{OH}

FIGURE 2–V_{IH} AND V_{OH}

† Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits (continued)†

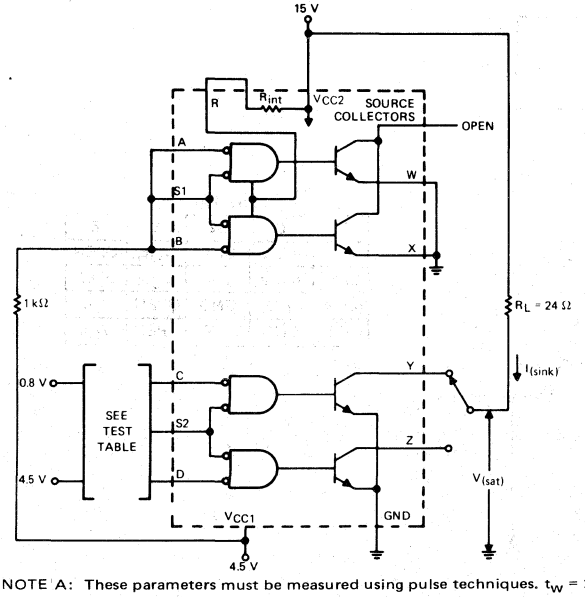


TEST TABLE

A	B	S1	W	X
0.8 V	4.5 V	0.8 V	GND	OPEN
4.5 V	0.8 V	0.8 V	OPEN	GND

NOTE A: These parameters must be measured using pulse techniques. t_w = 200 μs, duty cycle ≤ 2%.

FIGURE 3–V_{IL} AND SOURCE $V_{(sat)}$



TEST TABLE

C	D	S2	Y	Z
0.8 V	4.5 V	0.8 V	R_L	OPEN
4.5 V	0.8 V	0.8 V	OPEN	R_L

NOTE A: These parameters must be measured using pulse techniques. t_w = 200 μs, duty cycle ≤ 2%.

FIGURE 4–V_{IL} AND SINK $V_{(sat)}$

† Arrows indicate actual direction of current flow.

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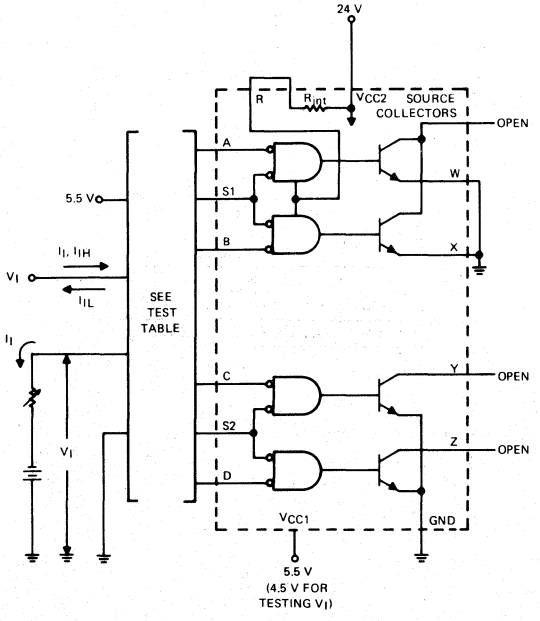
PARAMETER MEASUREMENT INFORMATION

d-c test circuits (continued)†



TEST TABLES

I_I, I_{IH}

APPLY V_I = 5.5 V, MEASURE I_I APPLY V_I = 2.4 V, MEASURE I_{IH}	GROUND	APPLY 5.5 V
A	S1	B, C, S2, D
S1	A, B	C, S2, D
B	S1	A, C, S2, D
C	S2	A, S1, B, D
S2	C, D	A, S1, B
D	S2	A, S1, B, C

V_I, I_{IL}

APPLY V_I = 0.4 V, MEASURE I_{IL} APPLY I_I = −10 mA MEASURE V_I	APPLY 5.5 V
A	S1, B, C, S2, D
S1	A, B, C, S2, D
B	A, S1, C, S2, D
C	A, S1, B, S2, D
S2	A, S1, B, C, D
D	A, S1, B, C, S2

FIGURE 5–V_I, I_I, I_{IH}, AND I_{IL}

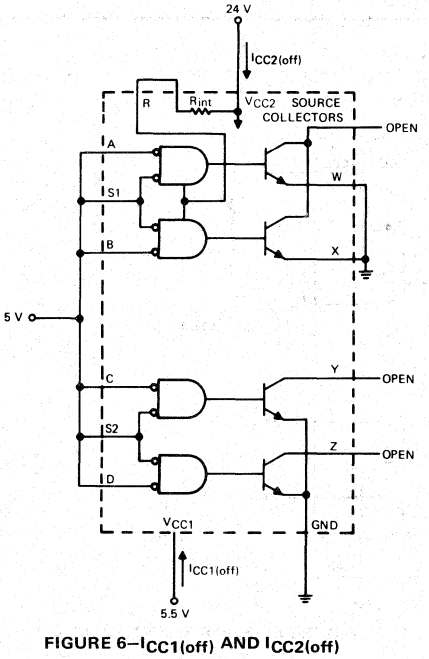
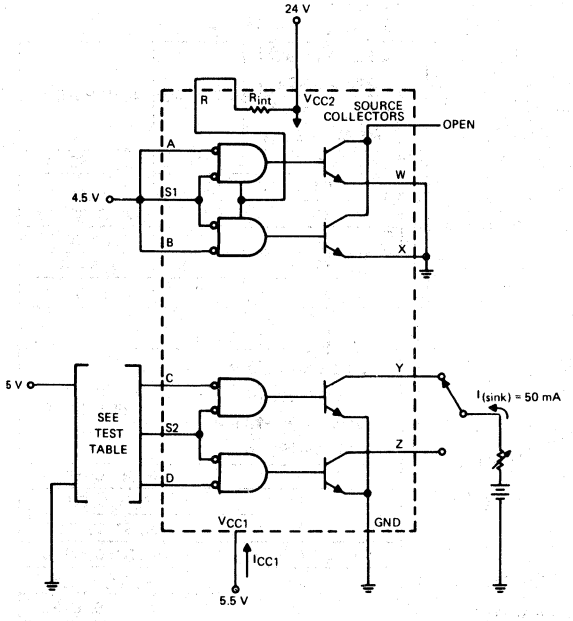


FIGURE 6–$I_{CC1(off)}$ AND $I_{CC2(off)}$

† Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

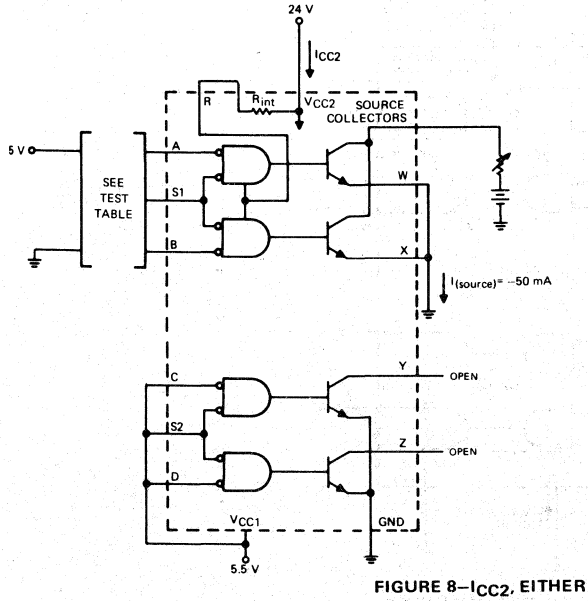
d-c test circuits (continued)†



TEST TABLE

C	D	S2	Y	Z
GND	5 V	GND	$I_{(sink)}$	OPEN
5 V	GND	GND	OPEN	$I_{(sink)}$

FIGURE 7–I_{CC1}, EITHER SINK ON



TEST TABLE

A	B	S1
GND	5 V	GND
5 V	GND	GND

FIGURE 8–I_{CC2}, EITHER SOURCE ON

† Arrows indicate actual direction of current flow.

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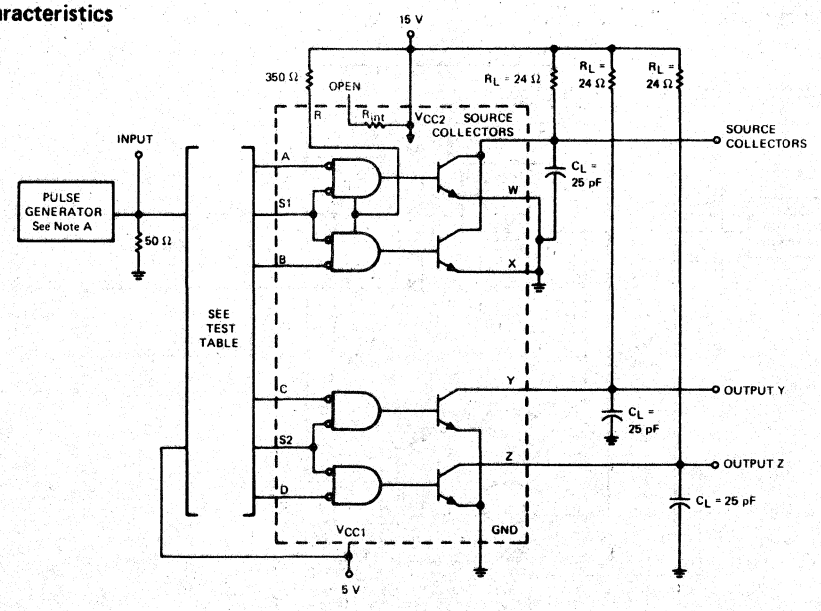
PARAMETER MEASUREMENT INFORMATION

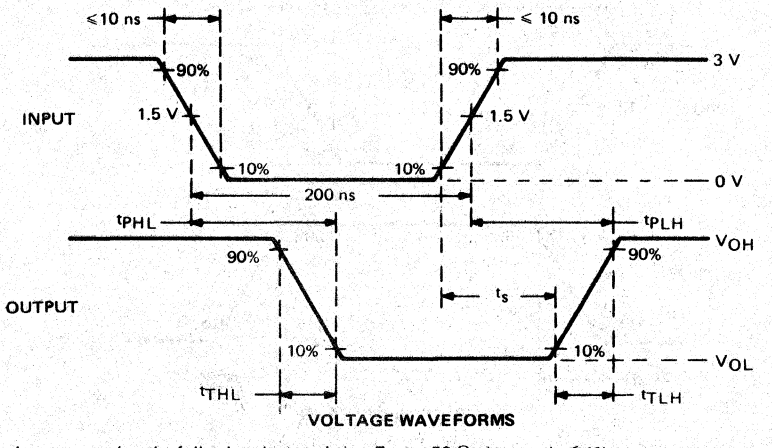
switching characteristics



TEST CIRCUIT

TEST TABLE

PARAMETER	OUTPUT UNDER TEST	INPUT	CONNECT TO 5 V
t_{PLH} and t_{PHL}	Source collectors	A and S1	B, C, D and S2
		B and S1	A, C, D and S2
t_{PLH}, t_{PHL}, t_{TLH}, t_{THL}, and t_s	Sink output Y	C and S2	A, B, D and S1
	Sink output Z	D and S2	A, B, C and S1



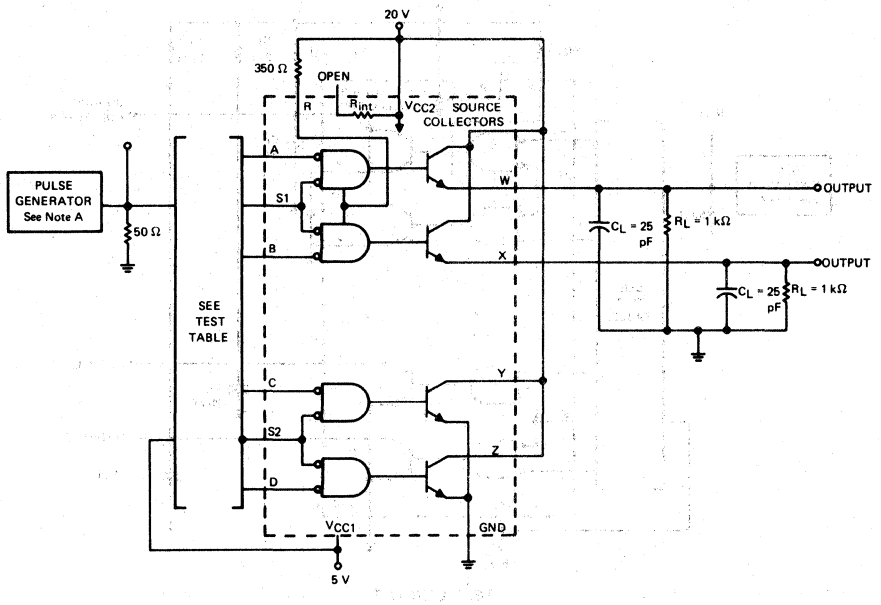
VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, duty cycle ≤ 1%.
B. C_L includes probe and jig capacitance.

FIGURE 9–SWITCHING TIMES

PARAMETER MEASUREMENT INFORMATION

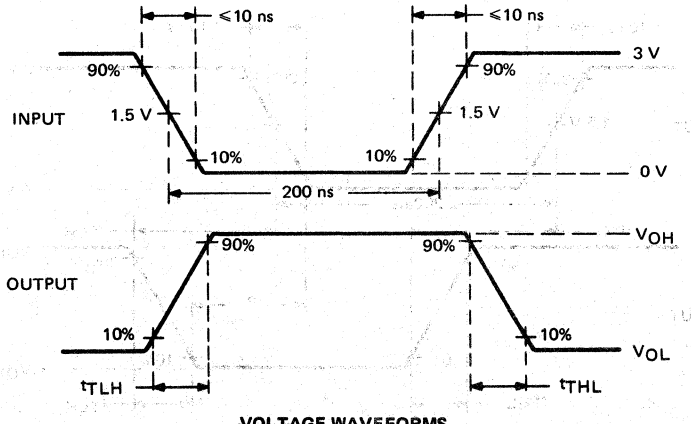
switching characteristics



TEST CIRCUIT

TEST TABLE

PARAMETER	OUTPUT UNDER TEST	INPUT	CONNECT TO 5 V
t_{TLH} and t_{THL}	Source output W	A and S1	B, C, D, and S2
	Source output X	B and S1	A, C, D, and S2



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, duty cycle ≤ 1%.
B. C_L includes probe and jig capacitance.

FIGURE 10–TRANSITION TIMES OF SOURCE OUTPUTS

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TYPICAL CHARACTERISTICS

OFF-STATE CURRENT INTO SOURCE COLLECTORS
vs
FREE-AIR TEMPERATURE

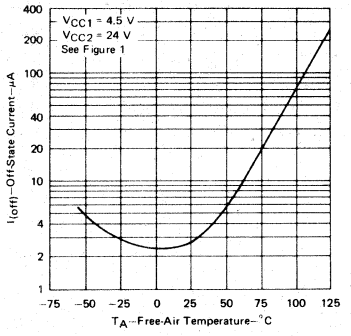


FIGURE 11

HIGH-LEVEL SINK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

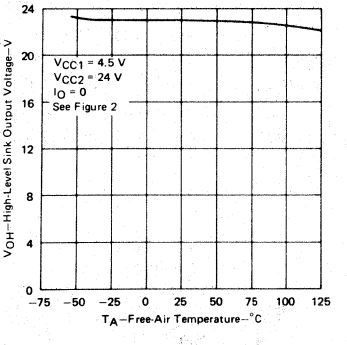


FIGURE 12

SOURCE OR SINK SATURATION VOLTAGE
vs
SOURCE CURRENT OR SINK CURRENT

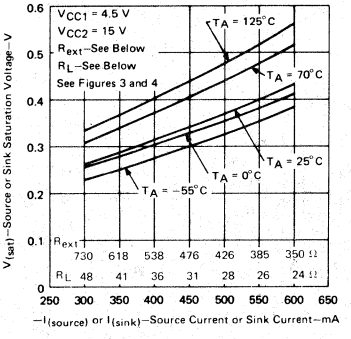


FIGURE 13

SOURCE OR SINK SATURATION VOLTAGE
vs
FREE-AIR TEMPERATURE

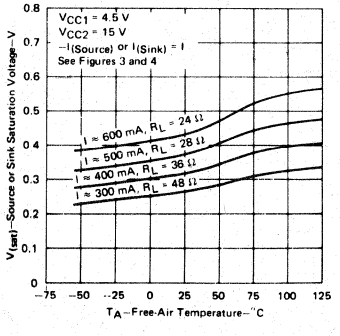


FIGURE 14

SUPPLY CURRENT, ALL SOURCES AND SINKS OFF
vs
FREE-AIR TEMPERATURE

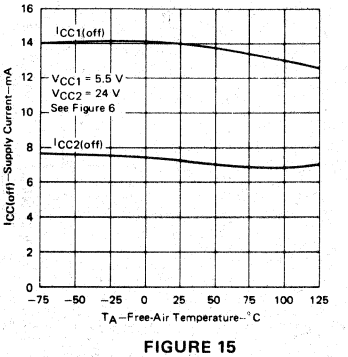
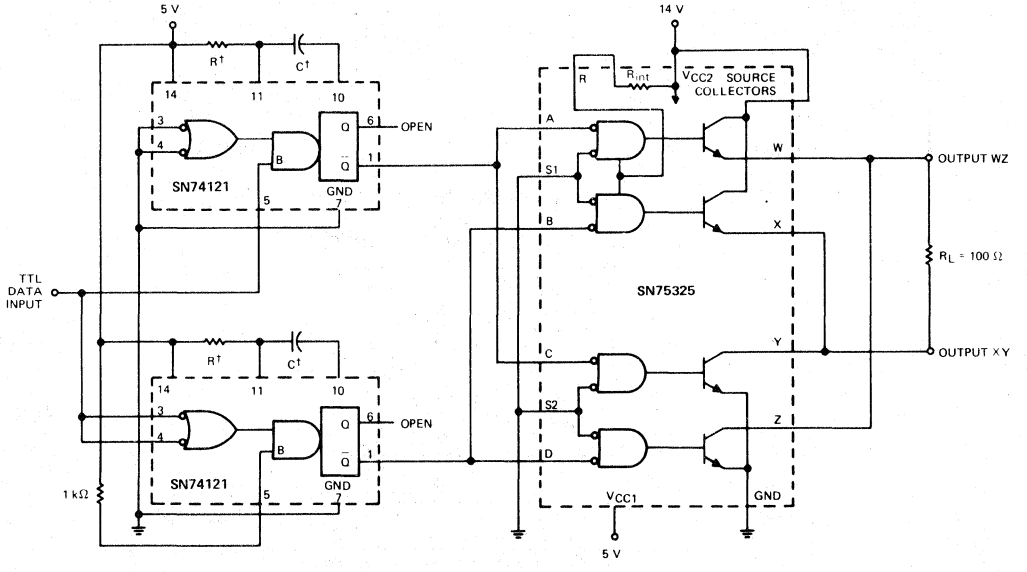


FIGURE 15

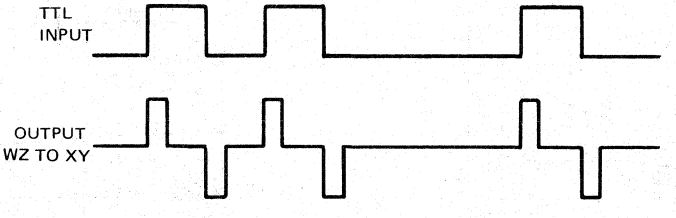
TYPICAL APPLICATION DATA

balanced bipolar logic-line driver

The circuit shown in Figure 16 converts standard TTL logic to bipolar logic. Bipolar logic is primarily used in transmitting data or clock pulses over long lines. This line-driver may be operated from a single 5-volt supply; however, the output drive may be increased by raising the supply voltage to the source collectors. The circuit features a tri-state output which is off during the absence of data, thus not dissipating high power. It provides a balanced drive circuit giving maximum noise immunity when used with the proper line receiver. Large drive levels can be used to further increase noise immunity. The circuit is capable of driving twisted-pair lines of several miles in length or low-impedance coaxial lines.



TEST CIRCUIT



VOLTAGE WAVEFORMS

†R and C are adjusted to give the desired bipolar output pulse width.

FIGURE 16–BALANCED BIPOLAR LOGIC–LINE DRIVER

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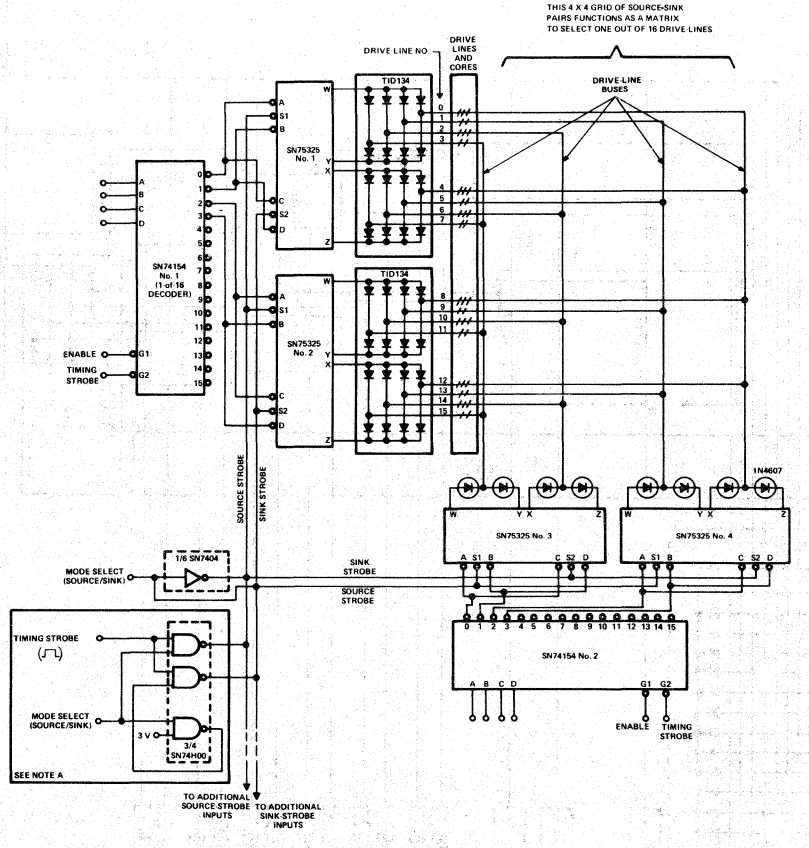
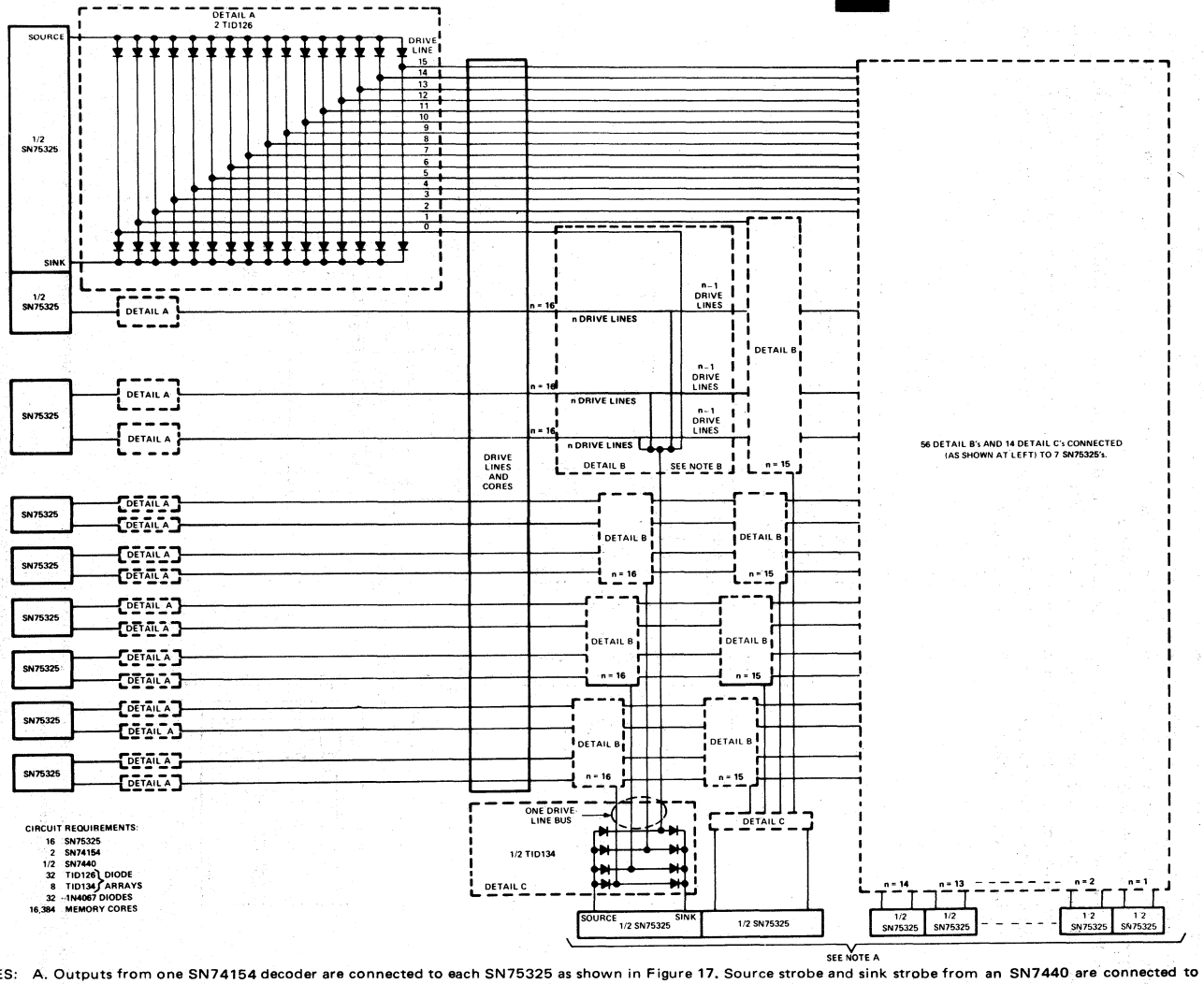
TYPICAL APPLICATION DATA

In memory-drive applications the SN75325 (or for full-temperature operation, the SN55325) can be connected in any of several ways. Typically, however, sources and sinks are arranged in pairs from which many drive-lines branch off as shown in Figure 17. Here each drive-line is served by a unique combination of two source/sink pairs so that a selection matrix is formed. To select drive-line 13, SN74154 No. 1 must be set to 3 (with mode select high), enabling source X of SN75325 No. 2 to drive lines 12 through 15, and SN74154 No. 2 must be set to 2, providing a sink at Y of SN75325 No. 4 for drive-line 13 only. Alternatively, to drive current in drive-line 13 in the opposite direction, only the mode-select voltage would be changed from high to low. The size of such a matrix is limited only by the number of drive-lines that a source/sink pair can serve. This number in turn depends on the capacitive and inductive load that each drive-line of the particular system imposes on the driver. A 256-drive-line selection matrix is shown in Figure 18. These 256 drive-lines are sufficient to serve $(256/2)^2 = 16{,}384$ individual cores.



NOTE A: This optional mode-select and timing-strobe technique can be used in place of the SN7440 mode-select and SN74154 timing-strobe when minimum time skew is desired.

FIGURE 17–SN75325 USED AS A MEMORY DRIVER TO SELECT ONE OF SIXTEEN DRIVE LINES



NOTES: A. Outputs from one SN74154 decoder are connected to each SN75325 as shown in Figure 17. Source strobe and sink strobe from an SN7440 are connected to each SN75325 as shown in Figure 17.

B. The division of the drive-line bus into four segments reduces the capacitive load on the SN75325 driver.

FIGURE 18—SN75325 SERVING 256 DRIVE LINES IN A MAGNETIC MEMORY

TYPICAL APPLICATION DATA

external resistor calculation

A typical magnetic-memory word-drive requirement is shown in Figure 19. A source-output transistor of one SN75325 delivers load current (I_L). The sink-output transistor of another SN75325 sinks this current.

The value of the external pull-up resistor (R_{ext}) for a particular memory application may be determined using the following equation:

$$R_{ext} = \frac{16\,[V_{CC2(min)} - V_S - 2.2]}{I_L - 1.6\,[V_{CC2(min)} - V_S - 2.9]} \qquad \text{(Equation 1)}$$

where: R_{ext} is in kΩ,
$V_{CC2(min)}$ is the lowest expected value of V_{CC2} in volts,
V_S is the source output voltage in volts with respect to ground,
I_L is in mA.

3

The power dissipated in resistor R_{ext} during the load current pulse duration is calculated using Equation 2,

$$P_{Rext} \approx \frac{I_L}{16}\,[V_{CC2(min)} - V_S - 2] \qquad \text{(Equation 2)}$$

where: P_{Rext} is in mW.

After solving for R_{ext}, the magnitude of the source collector current (I_{CS}) is determined from Equation 3,

$$I_{CS} \approx 0.94\, I_L \qquad \text{(Equation 3)}$$

where: I_{CS} is in mA.

As an example, let $V_{CC2(min)}$ = 20 V and V_L = 3 V while I_L of 500 mA flows.

Using Equation 1,

$$R_{ext} = \frac{16\ (20 - 3 - 2.2)}{500 - 1.6\ (20 - 3 - 2.9)} = 0.5\ k\Omega$$

and from Equation 2,

$$P_{Rext} \approx \frac{500}{16}\,[20 - 3 - 2] \approx 470\ mW$$

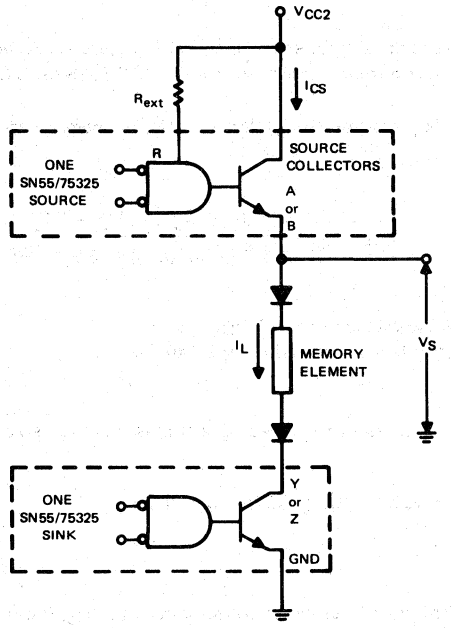
The amount of the memory system current source (I_{CS}) from Equation 3 is:

$$I_{CS} \approx 0.94\ (500) \approx 470\ mA$$

In this example the regulated source-output transistor base current through the external pull-up resistor (R_{ext}) and the source gate is approximately 30 mA. This current and I_{CS} comprise I_L.

TYPICAL APPLICATION DATA

external resistor calculation (continued)



NOTES: A. For clarity, partial logic diagrams of two SN75325's are shown.
B. Source and sink shown are in different packages.

FIGURE 19

THERMAL INFORMATION

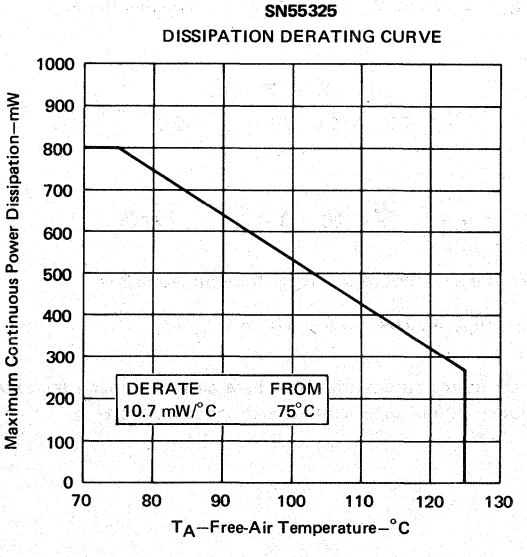


FIGURE 20

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PERIPHERAL DRIVERS FOR HIGH-CURRENT SWITCHING AT HIGH SPEEDS

ɔerformance

- 300-mA Output Current Capability
- High-Voltage Outputs
- High-Speed Switching

ɜase-of-design

- Circuit Flexibility for Varied Applications and Choice of Logic Function
- TTL or DTL Compatible Diode-Clamped Inputs
- Standard Supply Voltages

SUMMARY OF DUAL DRIVERS

DEVICE	LOGIC OF COMPLETE CIRCUIT	PACKAGE
SN75450A	AND†	N
SN75451A	AND	P
SN75452	NAND	P
SN75453	OR	P
SN75454	NOR	P

†With transistor base connected directly to output of gate.

3

ɪescription

Series 75450 dual peripheral drivers are a family of versatile devices designed for use in systems that employ TTL or DTL logic. Typical applications include high-speed logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, and memory drivers. Additionally, the SN75450A may be used as a line driver. The SN75450A and SN75451A are functionally interchangeable with and are recommended for replacement of SN75450 and SN75451, respectively, in most applications which do not require the very high speed of the prototypes. The A-versions offer improved freedom from latch-up and diode-clamped inputs to simplify system design. They can drive lamps, relays, and memories to rated levels of voltage and current without external loading capacitors. Series 75450 drivers are monolithic circuits designed for operation over the temperature range of 0°C to 70°C.

The SN75450A is a unique general-purpose device featuring two standard Series 74 TTL gates and two uncommitted, high-current, high-voltage n-p-n transistors. The SN75450A offers the system designer the flexibility of tailoring the circuit to the application.

The SN75451A, SN75452, SN75453, and SN75454 are dual peripheral AND, NAND, OR, and NOR drivers respectively, (assuming positive logic) with the output of the logic gates internally connected to the bases of the n-p-n output transistors.

CONTENTS

RELIMINARY DATA SHEET:
ɹpplementary data will be
ɹblished at a later date.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	SN75450A	SN75451A SN75452 SN75453 SN75454	UNIT
Supply voltage, V_{CC}	7	7	V
Input voltage (see Note 1)	5.5	5.5	V
Interemitter voltage (see Note 2)	5.5	5.5	V
V_{CC}-to-substrate voltage	35		V
Collector-to-substrate voltage	35		V
Collector-base voltage	35		V
Collector-emitter voltage (see Note 3)	30		V
Emitter-base voltage	5		V
Output voltage (see Notes 1 and 4)		30	V
Continuous collector current (see Note 5)	300		mA
Continuous output current (see Note 5)		300	mA
Continuous total power dissipation	800	800	mW
Operating free-air temperature range	0 to 70	0 to 70	°C
Storage temperature range	−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 10 seconds	260	260	°C

NOTES: 1. Voltage values are with respect to network ground terminal unless otherwise specified.
2. This is the voltage between two emitters of a multiple-emitter transistor.
3. This value applies when the base-emitter resistance (R_{BE}) is equal to or less than 500 Ω.
4. This is the maximum voltage which should be applied to any output when it is in the off state.
5. Both halves of these dual circuits may conduct rated current simultaneously.

recommended operating conditions (see note 6)

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Operating free-air temperature range, T_A	0	25	70	°C

NOTE 6: For the SN75450A only, the substrate (pin 8), must always be at the most-negative device voltage for proper operation.

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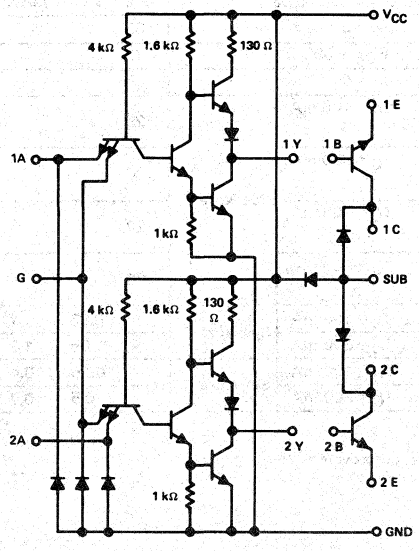
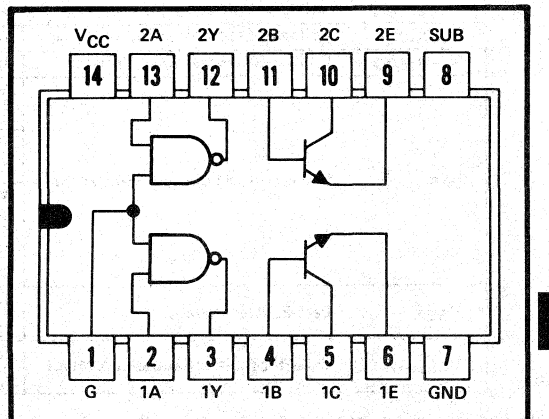
schematic



Component values shown are nominal

N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{AG}$ (gate only)
$C = AG$ (gate and transistor)

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

TTL gates

PARAMETER			TEST FIGURE	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage		1		2			V
V_{IL}	Low-level input voltage		2				0.8	V
V_I	Input clamp voltage		3	V_{CC} = 4.75 V, I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage		2	V_{CC} = 4.75 V, V_{IL} = 0.8 V, I_{OH} = −400 μA	2.4	3.3		V
V_{OL}	Low-level output voltage		1	V_{CC} = 4.75 V, V_{IH} = 2 V, I_{OL} = 16 mA		0.22	0.4	V
I_I	Input current at maximum input voltage	input A	4	V_{CC} = 5.25 V, V_I = 5.5 V			1	mA
		input G					2	
I_{IH}	High-level input current	input A	4	V_{CC} = 5.25 V, V_I = 2.4 V			40	μA
		input G					80	
I_{IL}	Low-level input current	input A	3	V_{CC} = 5.25 V, V_I = 0.4 V			−1.6	mA
		input G					−3.2	
I_{OS}	Short-circuit output current‡		5	V_{CC} = 5.25 V	−18		−55	mA
I_{CCH}	Supply current, high-level output		6	V_{CC} = 5.25 V, V_I = 0		2	4	mA
I_{CCL}	Supply current, low-level output			V_{CC} = 5.25 V, V_I = 5 V		6	11	mA

†All typical values at V_{CC} = 5 V, T_A = 25°C.
‡Not more than one output should be shorted at a time.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

output transistors

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	I_C = 100 μA, I_E = 0		35			V
$V_{(BR)CER}$	Collector-Emitter Breakdown Voltage	I_C = 100 μA, R_{BE} = 500 Ω		30			V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	I_E = 100 μA, I_C = 0		5			V
h_{FE}	Static Forward Current Transfer Ratio	V_{CE} = 3 V, I_C = 100 mA, T_A = 25°C	See Note 7	25			
		V_{CE} = 3 V, I_C = 300 mA, T_A = 25°C		30			
		V_{CE} = 3 V, I_C = 100 mA, T_A = 0°C		20			
		V_{CE} = 3 V, I_C = 300 mA, T_A = 0°C		25			
V_{BE}	Base-Emitter Voltage	I_B = 10 mA, I_C = 100 mA	See Note 7		0.85	1	V
		I_B = 30 mA, I_C = 300 mA			1.05	1.2	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	I_B = 10 mA, I_C = 100 mA	See Note 7		0.25	0.4	V
		I_B = 30 mA, I_C = 300 mA			0.5	0.7	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 7: These parameters must be measured using pulse techniques, t_w = 300 μs, duty cycle ≤ 2%.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

TTL gates

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	12	C_L = 15 pF, R_L = 400 Ω		20		ns
t_{PHL}	Propagation delay time, high-to-low-level output				8		ns

output transistors

PARAMETER		TEST FIGURE	TEST CONDITIONS‡	MIN	TYP	MAX	UNIT
t_d	Delay time	13	I_C = 200 mA, $I_{B(1)}$ = 20 mA, $I_{B(2)}$ = −40 mA, $V_{BE(off)}$ = −1 V, C_L = 15 pF, R_L = 50 Ω		8		ns
t_r	Rise time				12		ns
t_s	Storage time				7		ns
t_f	Fall time				6		ns

gates and transistors combined

PARAMETER		TEST FIGURE	TEST CONDITIONS‡	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	14	I_C = 200 mA, C_L = 15 pF, R_L = 50 Ω		40		ns
t_{PHL}	Propagation delay time, high-to-low-level output				25		ns
t_{TLH}	Transition time, low-to-high-level output				10		ns
t_{THL}	Transition time, high-to-low-level output				12		ns

‡Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

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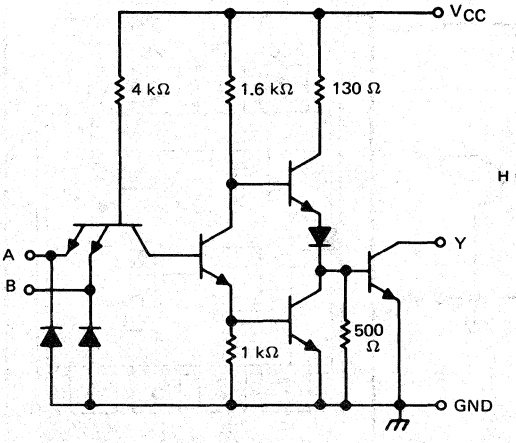
schematic (each driver)



Component values shown are nominal

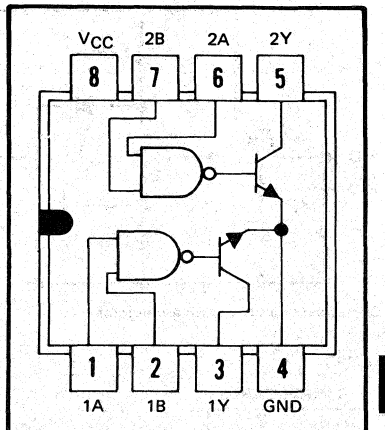
logic

TRUTH TABLE

A	B	Y
L	L	L (on state)
L	H	L (on state)
H	L	L (on state)
H	H	H (off state)

H = high level, L = low level

P
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: Y = AB

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage	7		2			V
V_{IL}	Low-level input voltage	7				0.8	V
V_I	Input clamp voltage	8	V_{CC} = 4.75 V, I_I = −12 mA			−1.5	V
I_{OH}	High-level output current	7	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{OH} = 30 V			100	μA
V_{OL}	Low-level output voltage	7	V_{CC} = 4.75 V, V_{IL} = 0.8 V, I_{OL} = 100 mA		0.25	0.4	V
			V_{CC} = 4.75 V, V_{IL} = 0.8 V, I_{OL} = 300 mA		0.5	0.7	
I_I	Input current at maximum input voltage	9	V_{CC} = 5.25 V, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	9	V_{CC} = 5.25 V, V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	8	V_{CC} = 5.25 V, V_I = 0.4 V		−1	−1.6	mA
I_{CCH}	Supply current, high-level output	10	V_{CC} = 5.25 V, V_I = 5 V		7	11	mA
I_{CCL}	Supply current, low-level output		V_{CC} = 5.25 V, V_I = 0		52	65	mA

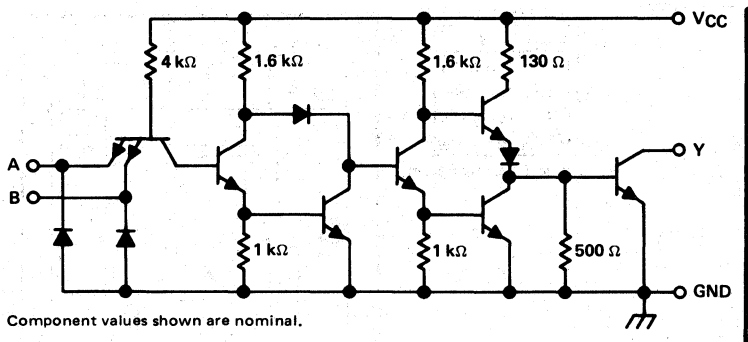
†All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		45		ns
t_{PHL}	Propagation delay time, high-to-low-level output				25		ns
t_{TLH}	Transition time, low-to-high-level output				10		ns
t_{THL}	Transition time, high-to-low-level output				12		ns

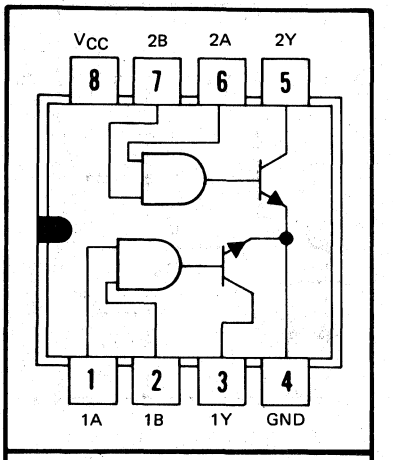
CIRCUIT TYPE SN75452
DUAL PERIPHERAL POSITIVE-NAND DRIVER

schematic (each driver)



Component values shown are nominal.

P
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{AB}$

logic

TRUTH TABLE

A	B	Y
L	L	H (off state)
L	H	H (off state)
H	L	H (off state)
H	H	L (on state)

H = high level L = low level

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage	7		2			V
V_{IL}	Low-level input voltage	7				0.8	V
V_I	Input clamp voltage	8	V_{CC} = 4.75 V, I_I = −12 mA			−1.5	V
I_{OH}	High-level output current	7	V_{CC} = 4.75 V, V_{IL} = 0.8 V, V_{OH} = 30 V			100	μA
V_{OL}	Low-level output voltage	7	V_{CC} = 4.75 V, V_{IH} = 2 V, I_{OL} = 100 mA		0.25	0.4	V
			V_{CC} = 4.75 V, V_{IH} = 2 V, I_{OL} = 300 mA		0.5	0.7	
I_I	Input current at maximum input voltage	9	V_{CC} = 5.25 V, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	9	V_{CC} = 5.25 V, V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	8	V_{CC} = 5.25 V, V_I = 0.4 V		−1	−1.6	mA
I_{CCH}	Supply current, high-level output	10	V_{CC} = 5.25 V, V_I = 0 V		11	14	mA
I_{CCL}	Supply current, low-level output		V_{CC} = 5.25 V, V_I = 5 V		56	71	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		50		ns
t_{PHL}	Propagation delay time, high-to-low-level output				35		ns
t_{TLH}	Transition time, low-to-high-level output				10		ns
t_{THL}	Transition time, high-to-low-level output				12		ns

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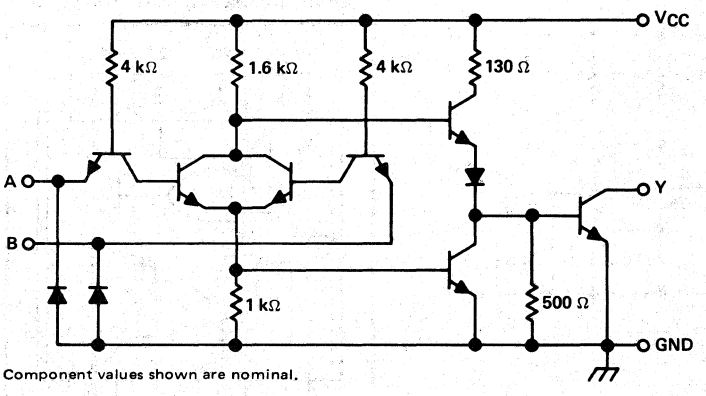
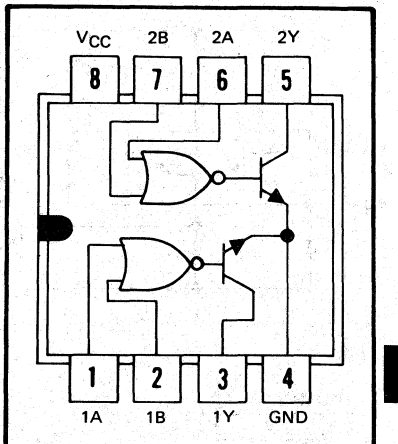
schematic (each driver)



Component values shown are nominal.

P
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: Y = A + B

logic

TRUTH TABLE

A	B	Y
L	L	L (on state)
L	H	H (off state)
H	L	H (off state)
H	H	H (off state)

H = high level, L = low level

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage	7		2			V
V_{IL}	Low-level input voltage	7				0.8	V
V_I	Input clamp voltage	8	V_{CC} = 4.75 V, I_I = −12 mA			−1.5	V
I_{OH}	High-level output current	7	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{OH} = 30 V			100	μA
V_{OL}	Low-level output voltage	7	V_{CC} = 4.75 V, V_{IL} = 0.8 V, I_{OL} = 100 mA		0.25	0.4	V
			V_{CC} = 4.75 V, V_{IL} = 0.8 V, I_{OL} = 300 mA		0.5	0.7	
I_I	Input current at maximum input voltage	9	V_{CC} = 5.25 V, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	9	V_{CC} = 5.25 V, V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	8	V_{CC} = 5.25 V, V_I = 0.4 V		−1	−1.6	mA
I_{CCH}	Supply current, high-level output	11	V_{CC} = 5.25 V, V_I = 5 V		8	11	mA
I_{CCL}	Supply current, low-level output		V_{CC} = 5.25 V, V_I = 0		54	68	mA

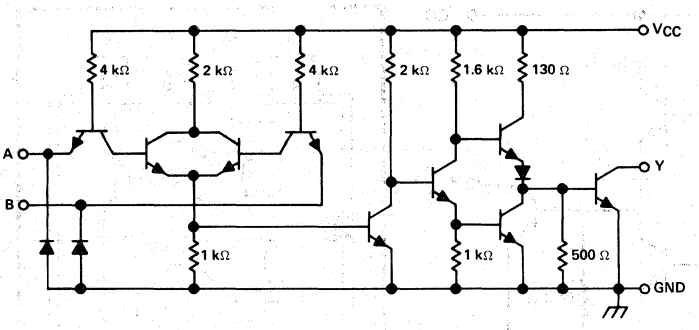
†All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		35		ns
t_{PHL}	Propagation delay time, high-to-low-level output				25		ns
t_{TLH}	Transition time, low-to-high-level output				10		ns
t_{THL}	Transition time, high-to-low-level output				12		ns

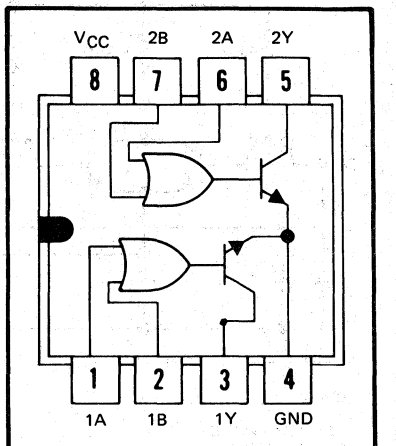
CIRCUIT TYPE SN75454
DUAL PERIPHERAL POSITIVE-NOR DRIVER

schematic (each driver)



P

DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{A + B}$

logic

TRUTH TABLE

A	B	Y
L	L	H (off state)
L	H	L (on state)
H	L	L (on state)
H	H	L (on state)

H = high level, L = low level

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage	7		2			V
V_{IL}	Low-level input voltage	7				0.8	V
V_I	Input clamp voltage	8	V_{CC} = 4.75 V, I_I = −12 mA			−1.5	V
I_{OH}	High-level output voltage	7	V_{CC} = 4.75 V, V_{IL} = 0.8 V, V_{OH} = 30 V			100	μA
V_{OL}	Low-level output voltage	7	V_{CC} = 4.75 V, V_{IH} = 2 V, I_{OL} = 100 mA		0.25	0.4	V
			V_{CC} = 4.75 V, V_{IH} = 2 V, I_{OL} = 300 mA		0.5	0.7	
I_I	Input current at maximum input voltage	9	V_{CC} = 5.25 V, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	9	V_{CC} = 5.25 V, V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	8	V_{CC} = 5.25 V, V_I = 0.4 V			−1.6	mA
I_{CCH}	Supply current, high-level output	11	V_{CC} = 5.25 V, V_I = 0 V		13	17	mA
I_{CCL}	Supply current, low-level output		V_{CC} = 5.25 V, V_I = 5 V		61	79	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		50		ns
t_{PHL}	Propagation delay time, high-to-low-level output				25		ns
t_{TLH}	Transition time, low-to-high-level output				10		ns
t_{THL}	Transition time, high-to-low-level output				12		ns

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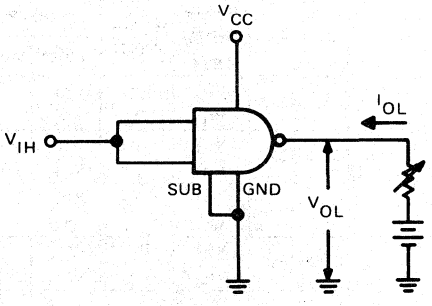
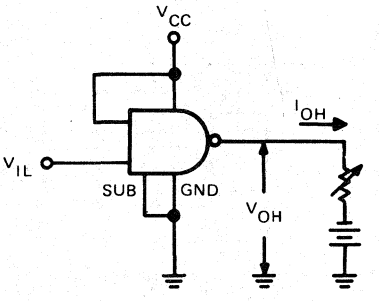
PARAMETER MEASUREMENT INFORMATION

d-c test circuits †



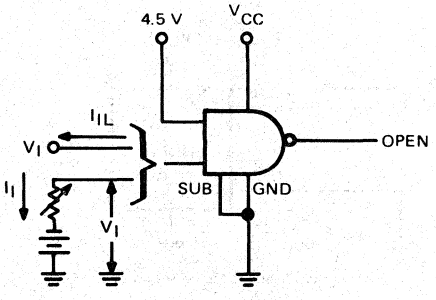
Both inputs are tested simultaneously.

FIGURE 1–V_{IH}, V_{OL}



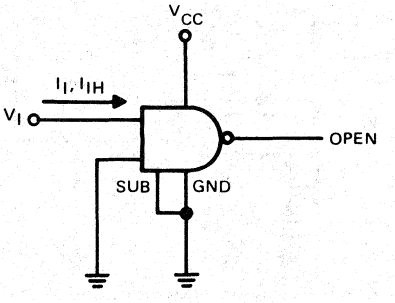
Each input is tested separately.

FIGURE 2–V_{IL}, V_{OH}



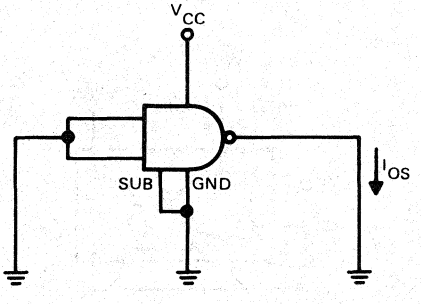
Each input is tested separately.

FIGURE 3–V_I, I_{IL}



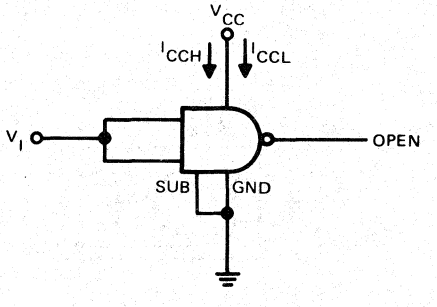
Each input is tested separately.

FIGURE 4–I_I, I_{IH}



Each gate is tested separately.

FIGURE 5–I_{OS}



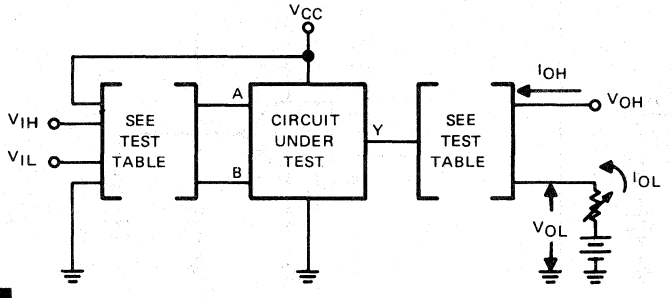
Both gates are tested simultaneously.

FIGURE 6–I_{CCH}, I_{CCL}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

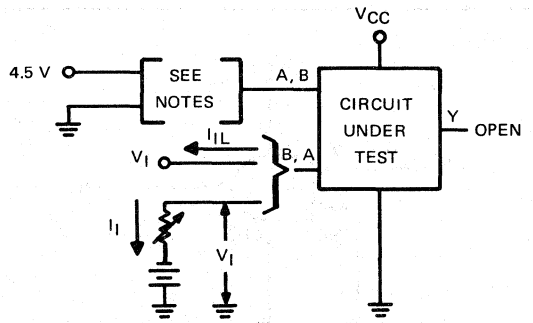


TEST TABLE

CIRCUIT	INPUT UNDER TEST	OTHER INPUT	OUTPUT	
			APPLY	MEASURE
SN75451A	V_{IH} V_{IL}	V_{IH} V_{CC}	V_{OH} I_{OL}	I_{OH} V_{OL}
SN75452	V_{IH} V_{IL}	V_{IH} V_{CC}	I_{OL} V_{OH}	V_{OL} I_{OH}
SN75453	V_{IH} V_{IL}	GND V_{IL}	V_{OH} I_{OL}	I_{OH} V_{OL}
SN75454	V_{IH} V_{IL}	GND V_{IL}	I_{OL} V_{OH}	V_{OL} I_{OH}

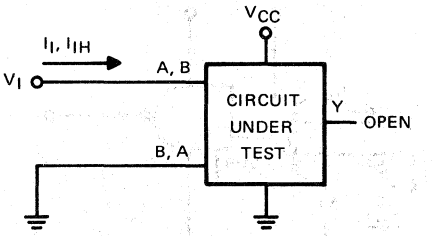
NOTE: Each input is tested separately.

FIGURE 7–V_{IH}, V_{IL}, I_{OH}, V_{OL}



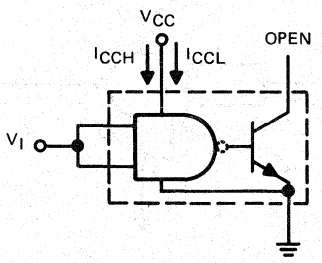
NOTES: A. Each input is tested separately.
B. When testing SN75453 and SN75454, input not under test is grounded. For all other circuits it is at 4.5 V.

FIGURE 8–V_I, I_{IL}



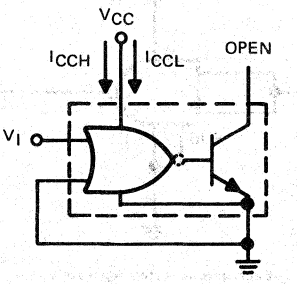
Each input is tested separately.

FIGURE 9–I_I, I_{IH}



Both gates are tested simultaneously.

FIGURE 10–I_{CCH}, I_{CCL} FOR AND, NAND CIRCUITS



Both gates are tested simultaneously.

FIGURE 11–I_{CCH}, I_{CCL} FOR OR, NOR CIRCUITS

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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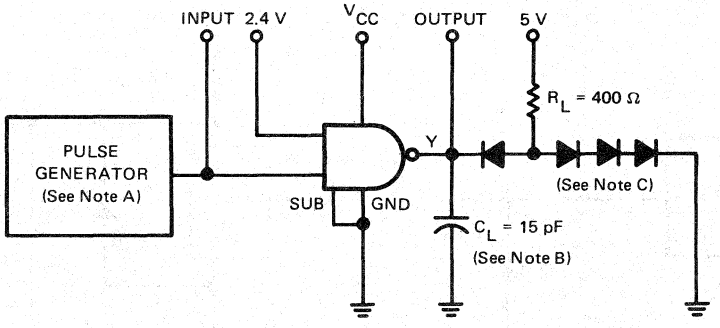
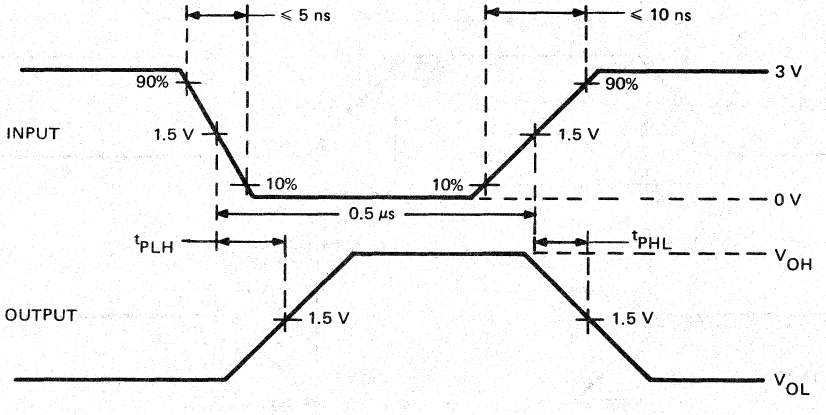
PARAMETER MEASUREMENT INFORMATION

witching characteristics



TEST CIRCUIT



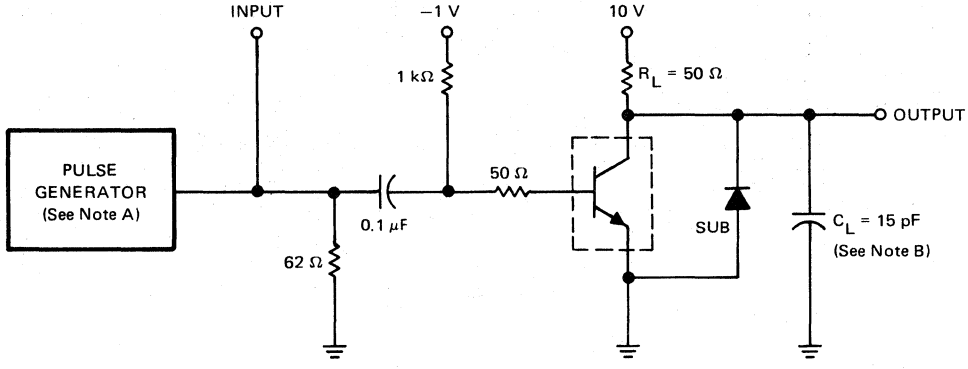
VOLTAGE WAVEFORMS

)TES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L include probe and jig capacitance.
C. All diodes are 1N3064.

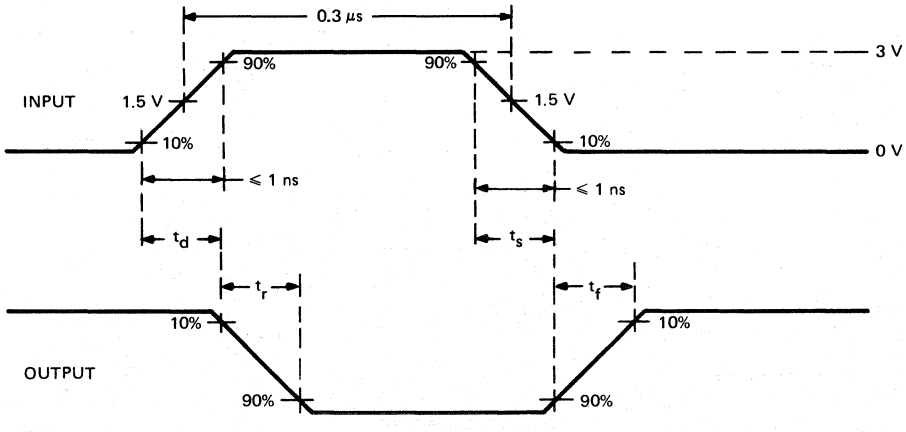
FIGURE 12–PROPAGATION DELAY TIMES, EACH GATE (SN75450A ONLY)

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: duty cycle ≤ 1%, Z_{out} ≈ 50 Ω.
B. C_L includes probe and jig capacitance.

FIGURE 13–SWITCHING TIMES, EACH TRANSISTOR (SN75450A ONLY)

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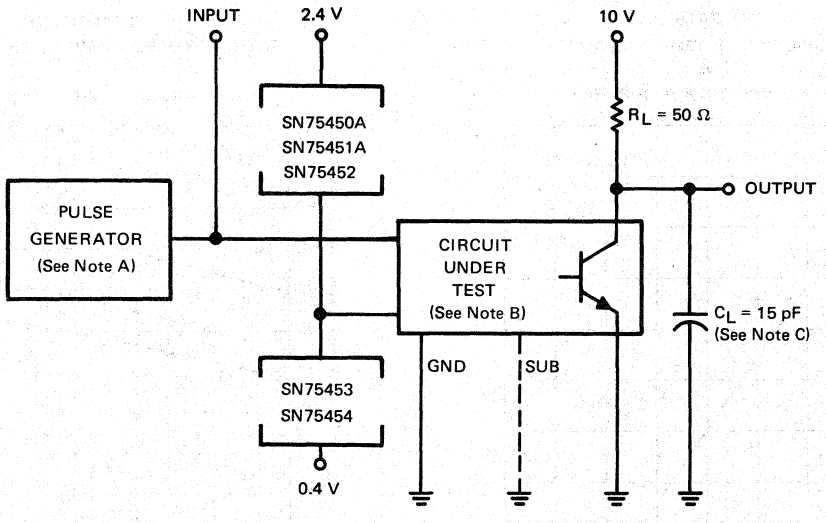
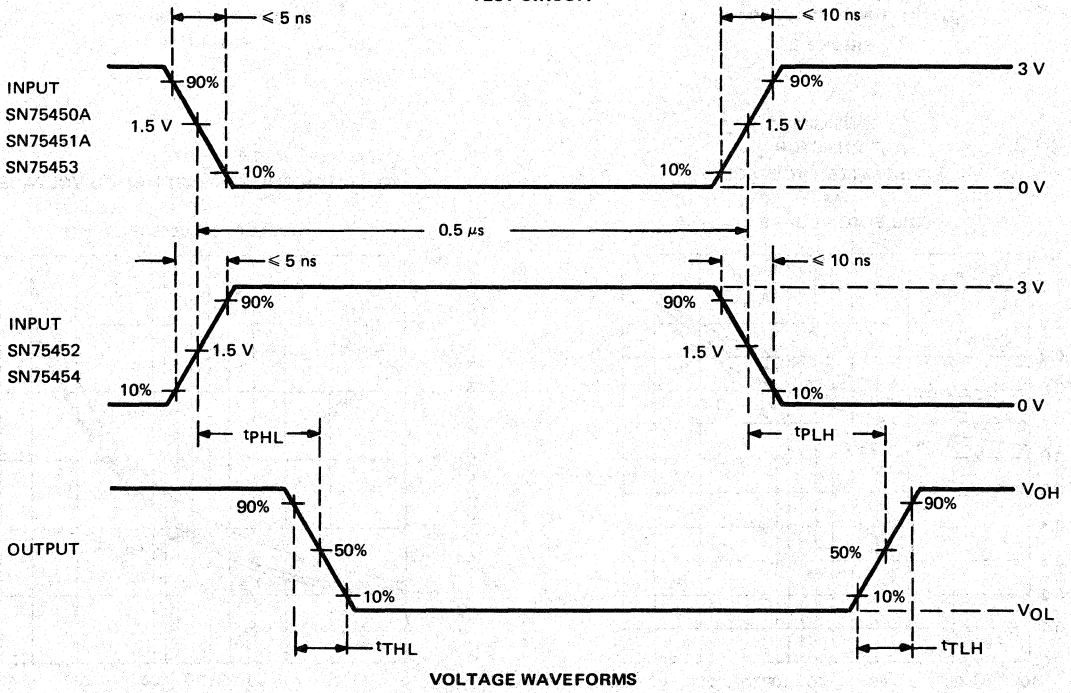
PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. When testing SN75450A, connect output Y to transistor base and ground the substrate terminal.
C. C_L includes probe and jig capacitance.

FIGURE 14–SWITCHING TIMES OF COMPLETE DRIVERS

TYPICAL CHARACTERISTICS

SN75450A
TTL GATE
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

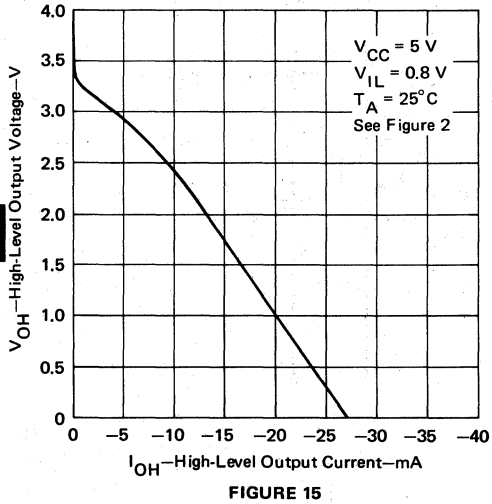


FIGURE 15

SN75450A
TRANSISTOR
STATIC FORWARD CURRENT TRANSFER RATIO
vs
COLLECTOR CURRENT

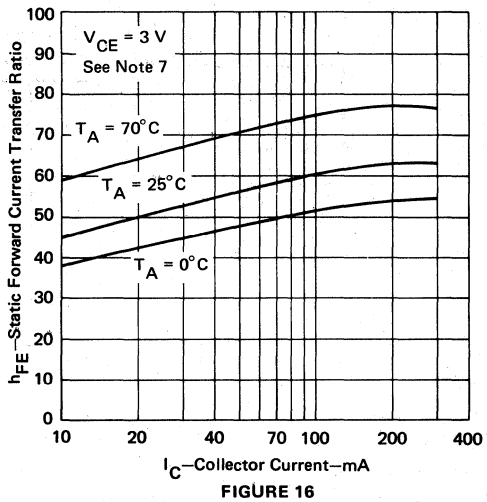


FIGURE 16

SN75450A
TRANSISTOR
BASE-EMITTER VOLTAGE
vs
COLLECTOR CURRENT

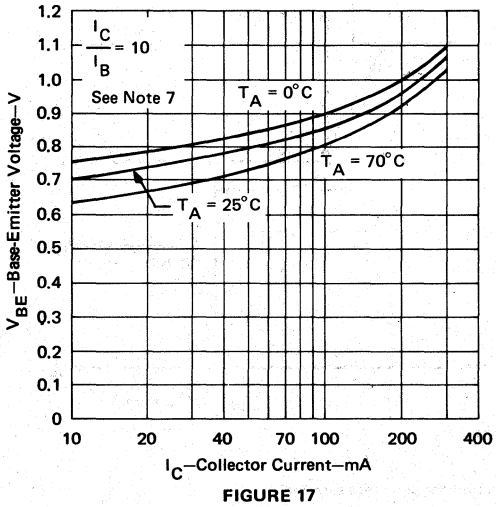


FIGURE 17

TRANSISTOR
COLLECTOR-EMITTER SATURATION VOLTAGE
vs
COLLECTOR CURRENT

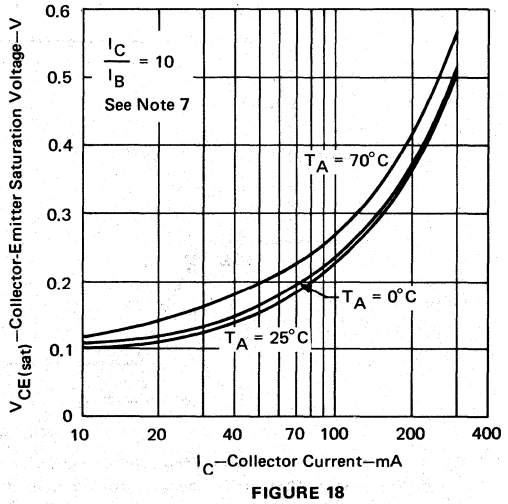


FIGURE 18

NOTE 7: These parameters must be measured using pulse techniques. t_w = 300 μs, duty cycle ≤ 2%.

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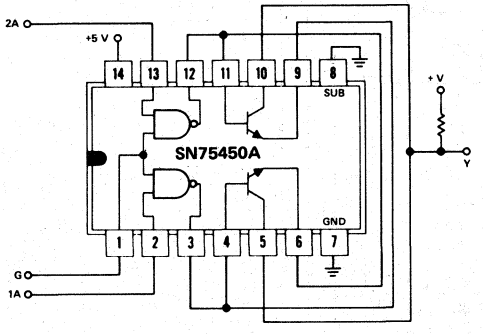
TYPICAL APPLICATION DATA



$Y = \overline{G} + 1A \cdot 2A + 1\overline{A} \cdot 2\overline{A}$

FIGURE 19–GATED COMPARATOR

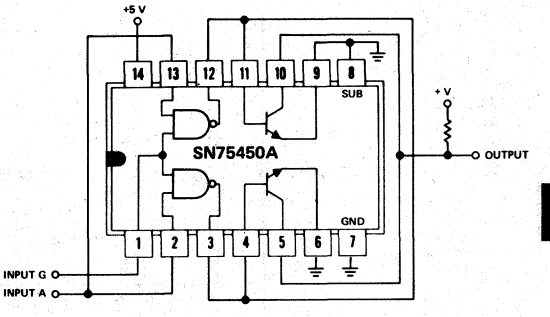


FIGURE 20–500-mA SINK

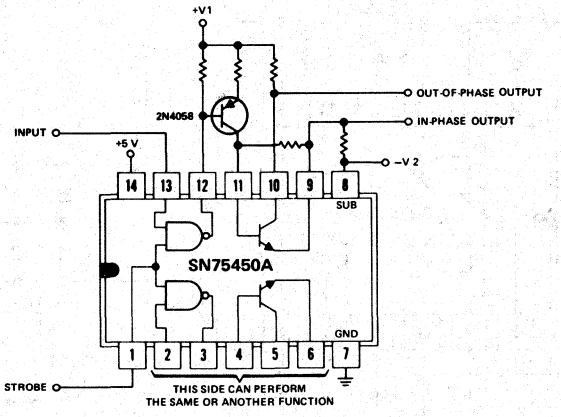


FIGURE 21–FLOATING SWITCH

TYPICAL APPLICATION DATA

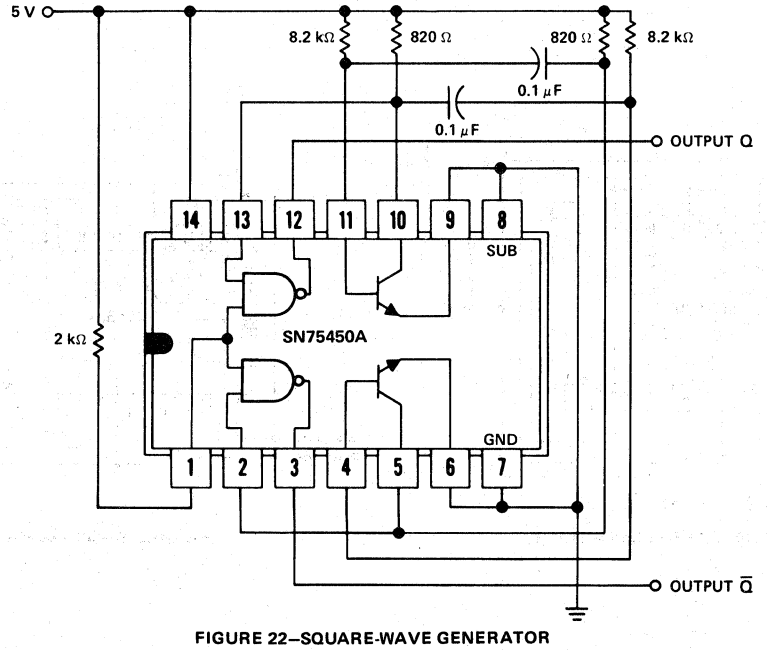
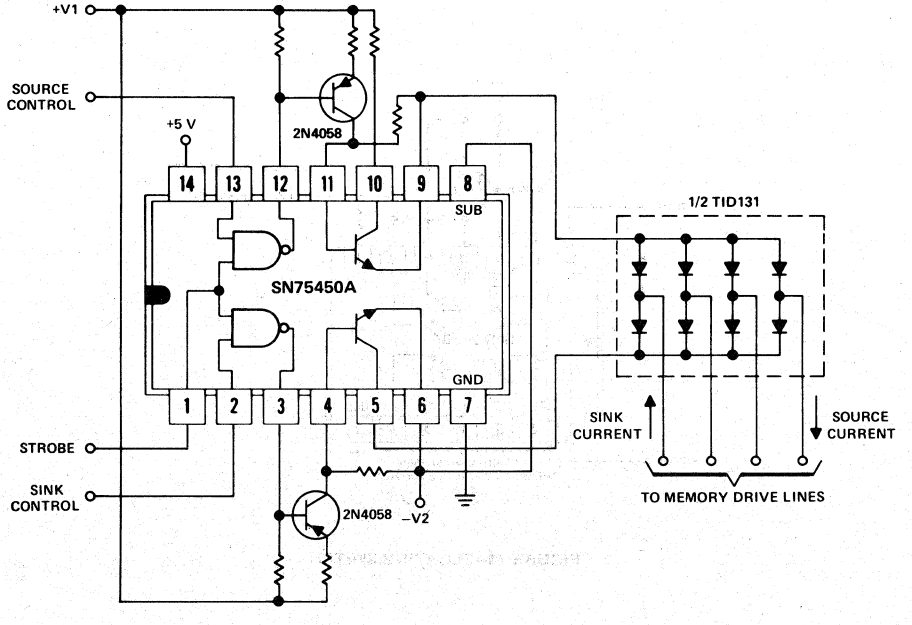


FIGURE 22–SQUARE-WAVE GENERATOR



Source and sink controls are activated by high-level input voltages ($V_{IH} \geq 2V$).

FIGURE 23–CORE MEMORY DRIVER

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TYPICAL APPLICATION DATA

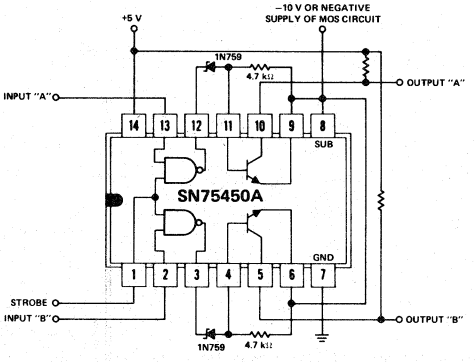


FIGURE 24—DUAL TTL-TO-MOS DRIVER

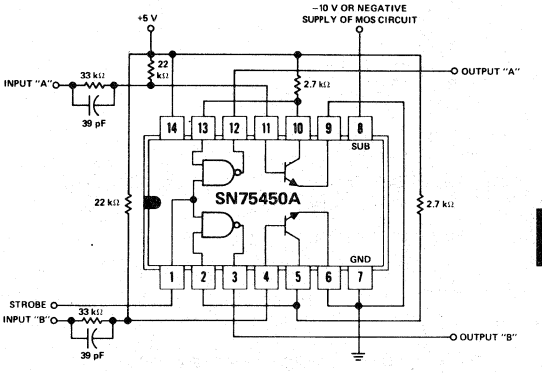
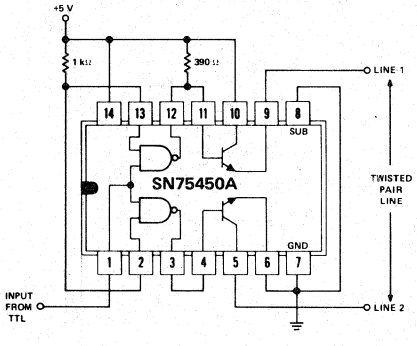
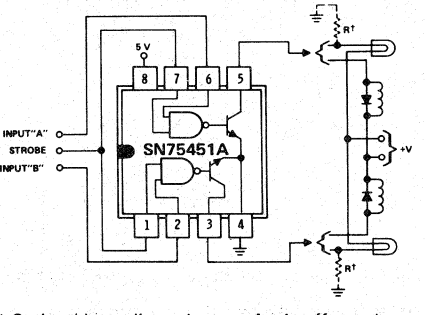


FIGURE 25—DUAL MOS-TO-TTL DRIVER



Termination is made at the receiving end as follows:
Line 1 is terminated to ground through $Z_o/2$;
Line 2 is terminated to +5 volts through $Z_o/2$;
where Z_o is the line impedence.

FIGURE 26—BALANCED LINE DRIVER



† Optional keep-alive resistors maintain off-state lamp current at ≈ 10% to reduce surge current.

FIGURE 27—DUAL LAMP OR RELAY DRIVER

TYPICAL APPLICATION DATA

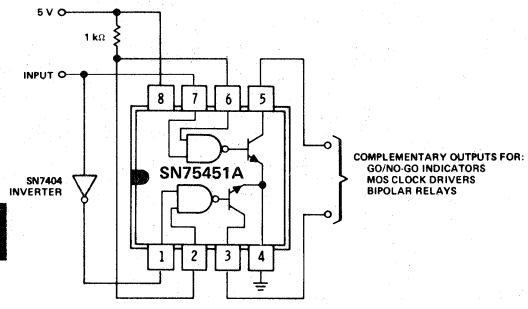


FIGURE 28–COMPLEMENTARY DRIVER

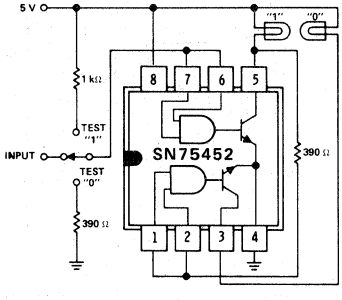
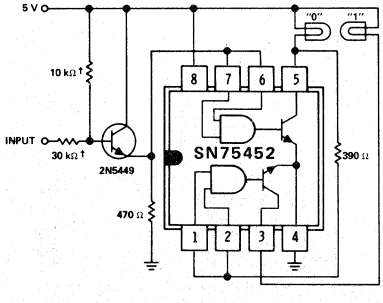


FIGURE 29–TTL OR DTL POSITIVE LOGIC-LEVEL DETECTOR



† The two input resistors must be adjusted for the level of MOS input.

FIGURE 30–MOS NEGATIVE-LOGIC-LEVEL DETECTOR

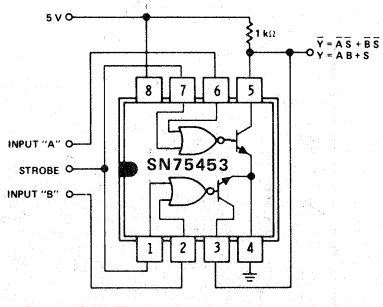


FIGURE 31–LOGIC SIGNAL COMPARATOR

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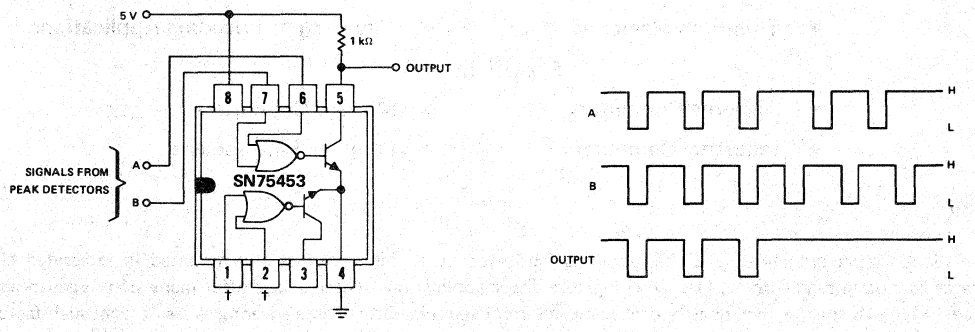
TYPICAL APPLICATION DATA



Low output occurs only when inputs are low simultaneously.

†If inputs are unused, they should be connected to +5 V through a 1 kΩ resistor.

FIGURE 32–IN-PHASE DETECTOR

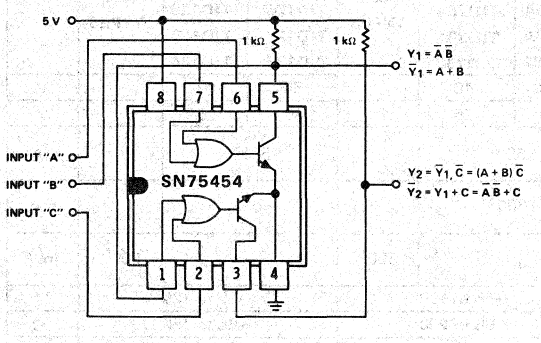


FIGURE 33–MULTIFUNCTION LOGIC-SIGNAL COMPARATOR

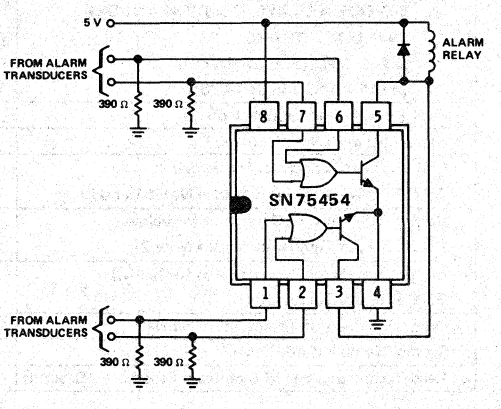


FIGURE 34–ALARM DETECTOR

CORE-DRIVER DIODE ARRAYS

For Application With

- Magnetic Cores
- Plated-Wire Memories
- Thin-Film Memories
- Decoding or Encoding Applications

For Use In

- Airborne Computers
- Military Computers
- Industrial Computers
- Peripheral Equipment

description

3

These diode arrays are multiple diode junctions fabricated by a planar process and mounted in integrated circuit packages for use in high-current, fast-switching core-driver applications. These arrays offer many of the advantages of integrated circuits such as high-density packaging and improved reliability. These advantages result from such factors as fewer connections, more uniform device parameters, smaller size, less weight, fewer glass-to-metal seals, and the elimination of pressure contacts and whiskers.

The arrays are available in hermetically sealed, welded flat packages or in dual-in-line plastic packages.

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

	FLAT PACKAGE			DUAL-IN-LINE PACKAGE			
	EACH DIODE		TOTAL DEVICE	EACH DIODE		TOTAL DEVICE	UNIT
8-DIODE ARRAYS (COMMON CATHODE) 8-DIODE ARRAYS (COMMON ANODE) 16-DIODE ARRAYS DUAL 10-DIODE ARRAYS DUAL 8-DIODE ARRAYS	TID21A TID23A TID25A TID29A TID131	TID22A TID24A TID26A TID30A TID132	ALL TYPES	TID121 TID123 TID125 TID129 TID133	TID122 TID124 TID126 TID130 TID134	ALL TYPES	
Peak Reverse Voltage (See Note 1)	60	40		60	40		V
Steady-State Reverse Voltage, V_R	40	25		40	25		V
Peak Forward Current at (or below) 25°C Free-Air Temperature (See Notes 1 and 2)	500†			500‡			mA
Continuous Forward Current at (or below) 25°C Free-Air Temperature (See Note 2)	300§			400¶			mA
Continuous Power Dissipation at (or below) 25°C Free-Air Temperature			500◇			600□	mW
Operating Free-Air Temperature Range	−65 to 150			−65 to 125			°C
Storage Temperature Range	−65 to 200			−65 to 150			°C
Lead Temperature 1/16 Inch from Case for 10 Seconds	300			260			°C

NOTES: 1. These values apply for 100-μs pulses, duty cycle ⩽ 20%.
2. The values shown for total device apply for any combination provided the ratings of individual diodes are not exceeded.

†Derate linearly to 150°C free-air temperature at the rate of 4 mA/°C.
‡Derate linearly to 125°C free-air temperature at the rate of 5 mA/°C.
§Derate linearly to 150°C free-air temperature at the rate of 2.4 mA/°C.
¶Derate linearly to 125°C free-air temperature at the rate of 4 mA/°C.
◇Derate linearly to 150°C free-air temperature at the rate of 4 mW/°C.
□Derate linearly to 125°C free-air temperature at the rate of 6 mW/°C.

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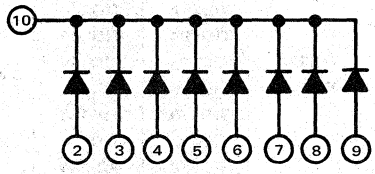
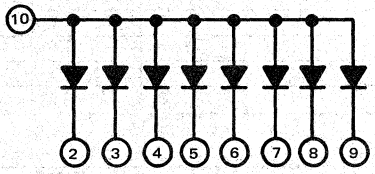
FLAT PACKAGES

TID21A, TID22A
8-DIODE ARRAY (COMMON CATHODE)
10-PIN PACKAGE



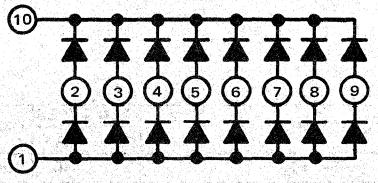
(1) No internal connection

TID23A, TID24A
8-DIODE ARRAY (COMMON ANODE)
10-PIN PACKAGE

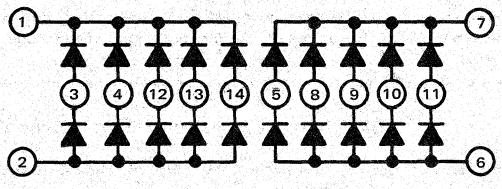


(1) No internal connection

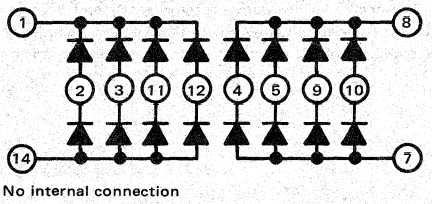
TID25A, TID26A
16-DIODE ARRAY
10-PIN PACKAGE



TID29A, TID30A
DUAL 10-DIODE ARRAY
14-PIN PACKAGE



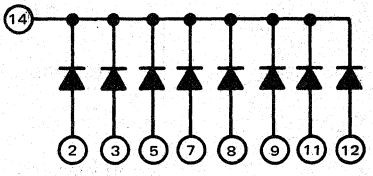
TID131, TID132
DUAL 8-DIODE ARRAY
14-PIN PACKAGE



(6) (13) No internal connection

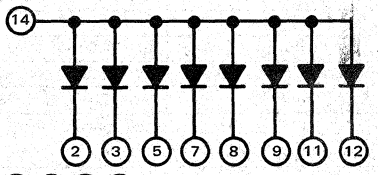
14-PIN PLASTIC DUAL-IN-LINE PACKAGES

TID121, TID122
8-DIODE ARRAY (COMMON CATHODE)
14-PIN PACKAGE



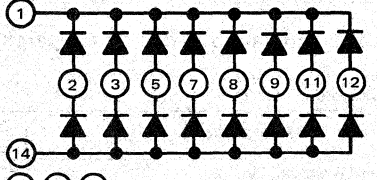
(1) (4) (6) (10) (13) No internal connection

TID123, TID124
8-DIODE ARRAY (COMMON ANODE)
14-PIN PACKAGE



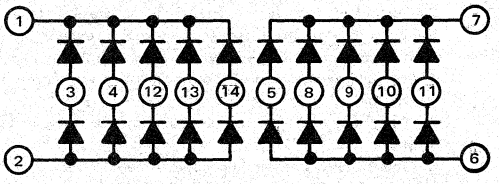
(1) (4) (6) (10) (13) No internal connection

TID125, TID126
16-DIODE ARRAY
14-PIN PACKAGE

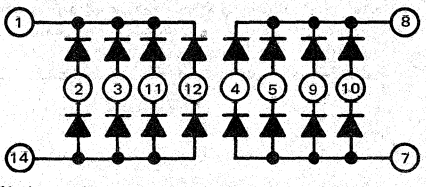


(4) (6) (10) (13) No internal connection

TID129, TID130
DUAL 10-DIODE ARRAY
14-PIN PACKAGE



TID133, TID134
DUAL 8-DIODE ARRAY
14-PIN PACKAGE



(6) (13) No internal connection

3

electrical characteristics at 25°C free-air temperature

single-diode operation (see note 3)

PARAMETER		TEST CONDITIONS		TID21A TID121		TID22A TID122		TID23A TID25A TID29A TID123 TID125 TID129 TID131 TID133		TID24A TID26A TID30A TID124 TID126 TID130 TID132 TID134		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$V_{(BR)}$	Reverse Breakdown Voltage	I_R = 10 μA		60		40		60		40		V
I_R	Static Reverse Current	V_R = 40 V,	See Note 4		0.1				0.1			μA
		V_R = 25 V,	See Note 4				0.1				0.1	μA
V_F	Static Forward Voltage	I_F = 100 mA			1		1.1		1		1.1	V
v_F	Instantaneous Forward Voltage	I_F = 500 mA,	See Note 5		1.3		1.5		1.3		1.5	V
V_{FM}	Peak Forward Voltage	I_F = 500 mA,	See Note 6		5		5		5		5	V
C_T	Total Capacitance†	V_R = 0,	f = 1 MHz		4		4		8		8	pF

multiple-diode operation (see note 7)

PARAMETER		TEST CONDITIONS		ALL TYPES		UNIT
				MIN	MAX	
I_{R1}	Static Reverse Current	V_{R1} = rated V_R,	I_{FN} = 25 mA		10	μA
V_{F1}	Static Forward Voltage	$I_{F1} = I_{FN}$ = 25 mA			1	V

switching characteristics at 25°C free-air temperature

single-diode operation (see note 3)

PARAMETER		TEST CONDITIONS		ALL TYPES		UNIT
				MIN	MAX	
t_{fr}	Forward Recovery Time	I_F = 500 mA,	See Figure 3		40	ns
t_{rr}	Reverse Recovery Time	I_F = 200 mA, R_L = 100 Ω, See Figure 4	I_{RM} = 200 mA, i_{rr} = 20 mA,		20	ns

NOTES: 3. Test conditions and limits apply separately to each of the diodes. The diodes not under test are open-circuited during the measurement of these characteristics except for the measurement of I_R on arrays having both common-cathode and common-anode diodes (see Figures 1 and 2).

4. For arrays having both common-anode and common-cathode diodes see Figures 1 and 2, Parameter Measurement Information section.

5. This parameter is measured using pulse techniques. t_w = 300 μs, duty cycle = 2 %. Read time is 90 μs from the leading edge of the pulse.

6. The initial instantaneous value is measured using pulse techniques. t_w = 150 ns, duty cycle ⩽ 2%, pulse rise time ⩽ 10 ns. The total diode shunt capacitance is 19 pF maximum and the equipment bandwidth is 80 MHz.

7. Subscript numeral 1 refers to the diode under test; subscript N refers simultaneously to each of the other diodes in the section. Each diode is individually tested after the device reaches operating thermal equilibrium. Test conditions apply separately to common-anode and common-cathode sections.

†C_T is the total pin-to-pin capacitance measured across any of the diodes. For arrays having both common-anode and common-cathode sections, the interaction of the other diodes cannot easily be separated out unless three-terminal guarded measurement techniques are used. The actual capacitance of a single isolated diode will typically be 30% of the measured pin-to-pin value for the common-cathode diodes, and 75% of the measured value for the common-anode diodes.

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PARAMETER MEASUREMENT INFORMATION

When measuring the reverse current of an individual diode of a device having both common-anode and common-cathode sections, the current meter must be placed so that the shunt current through the other diodes is bypassed around the meter to obtain accurate readings, the voltage drop across the current meter must be less than 10 mV.

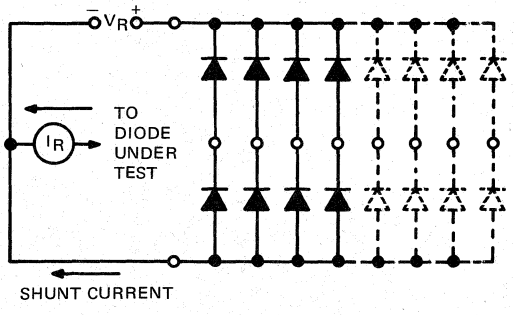


FIGURE 1–TEST CIRCUIT FOR COMMON-CATHODE DIODES

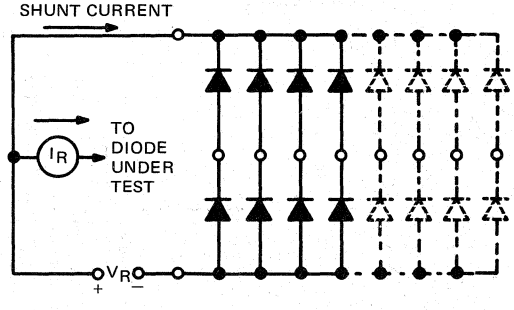
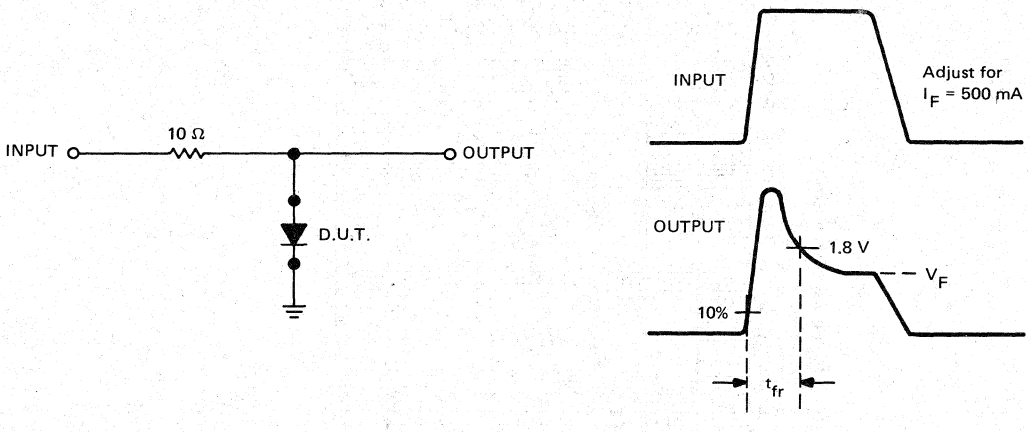


FIGURE 2–TEST CIRCUIT FOR COMMON-ANODE DIODES



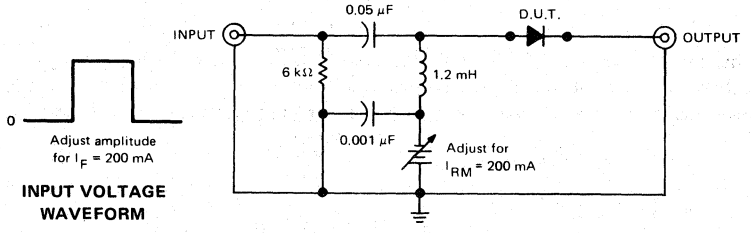
TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 3–FORWARD RECOVERY TIME

NOTES: a. The input pulse is supplied by a generator with the following characteristics: $t_r \leq 15$ ns, $Z_{out} = 50\ \Omega$, $t_w = 150$ ns, duty cycle $\leq$ 2%.

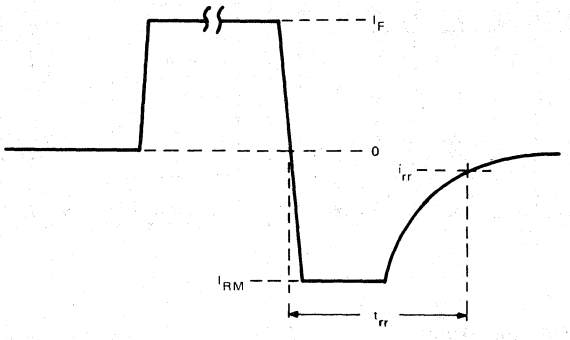
b. The output waveform is monitored on an oscilloscope with the following characteristics: $t_r \leq 4.5$ ns, $R_{in} \geq 1\ M\Omega$, $C_{in} \leq 5$ pF.

PARAMETER MEASUREMENT INFORMATION



INPUT VOLTAGE WAVEFORM

TEST CIRCUIT



OUTPUT CURRENT WAVEFORM

FIGURE 4–REVERSE RECOVERY TIME

NOTES: c. The input pulse is supplied by a generator with the following characteristics: $t_f \leq 1$ ns, $Z_{out} = 50\ \Omega$, $t_w = 200$ ns, duty cycle ≤ 1%.

d. The output waveform is monitored on an oscilloscope with the following characteristics: $t_r \leq 0.4$ ns, $R_{in} = 50\ \Omega$.

TYPICAL CHARACTERISTICS

FORWARD CONDUCTION CHARACTERISTICS

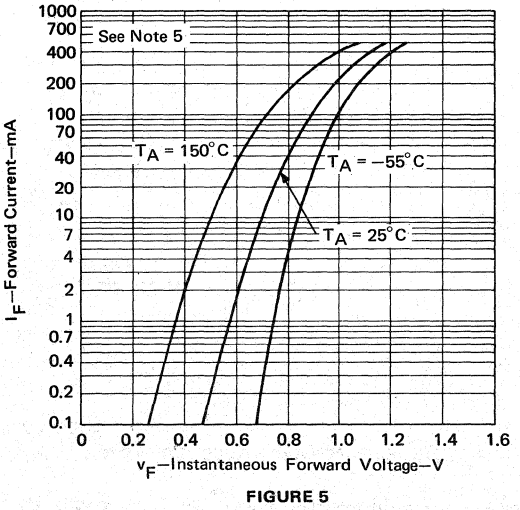


FIGURE 5

NOTE 5: This parameter is measured using pulse techniques. $t_w = 300\ \mu s$, duty cycle = 2%. Read time is 90 μs from the leading edge of the pulse.

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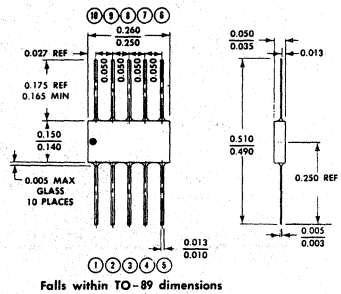
MECHANICAL DATA

flat packages

These hermetic packages feature glass-to-metal seals and welded construction in 10-pin and 14-pin configurations. Package body and leads are gold-plated F-15‡ glass-sealing alloy. Approximate weight is 0.1 gram. All external surfaces are metallic.

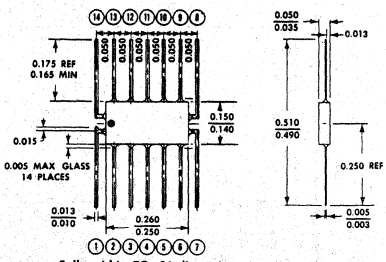
TID21A, TID22A, TID23A, TID24A, TID25A, TID26A



Falls within TO-89 dimensions

NOTES: a. All dimensions in inches.
b. All decimals ±0.005 except as noted.
c. Lead centerlines are located within ±0.005 of their true positions relative to body centerlines. This is measured along lines located within 0.030 from (and parallel to) the sides of the package.

TID29A, TID30A, TID131, TID132



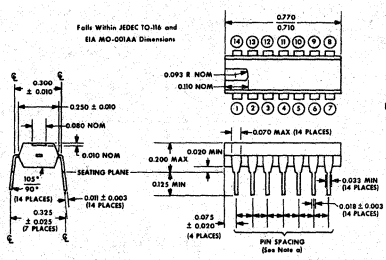
Falls within TO-84 dimensions

NOTES: a. All dimensions in inches.
b. All decimals ±0.005 except as noted.
c. Lead centerlines are located within ±0.005 of their true positions relative to body centerlines. This is measured along lines located within 0.030 from (and parallel to) the sides of the package.

plastic dual-in-line package

The compound used to mold the dual-in-line package will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. These packages are intended for insertion in mounting-hole rows on 0.300-inch centers. Once the leads are compressed to 0.300-inch separation and inserted, sufficient tension is provided to secure the package in the board during soldering. The silver-plated leads require no additional cleaning or processing when used in soldered assembly.

TID121, TID122, TID123, TID124, TID125, TID126, TID129, TID130, TID133, TID134



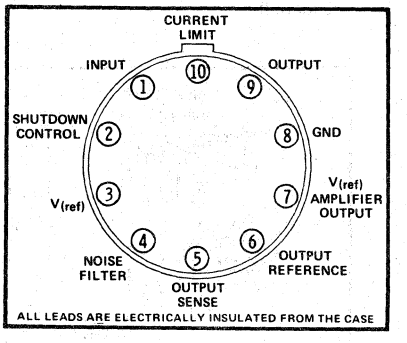
NOTES: a. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins 4 and 11.
b. All dimensions are in inches unless otherwise noted.

‡F-15 is the ASTM designation for an iron-nickel-cobalt alloy containing nominally 53% iron, 29% nickel, and 17% cobalt.

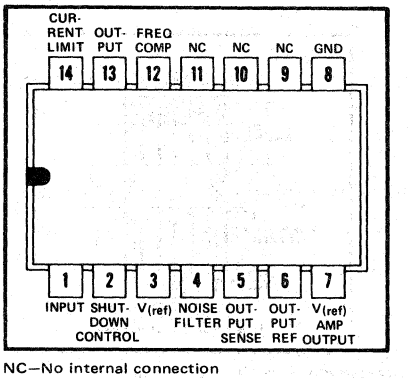
CIRCUIT TYPE SN72400
VOLTAGE REGULATOR

- 200-mA Load Current without External Power Transistor
- Remote Shutdown Control
- Adjustable Short-Circuit Current Limiter
- Input Voltages to 40 Volts
- Output Adjustable from 2 to 37 Volts

L
PLUG-IN PACKAGE (TOP VIEW)



N
DUAL-IN-LINE PACKAGE (TOP VIEW)



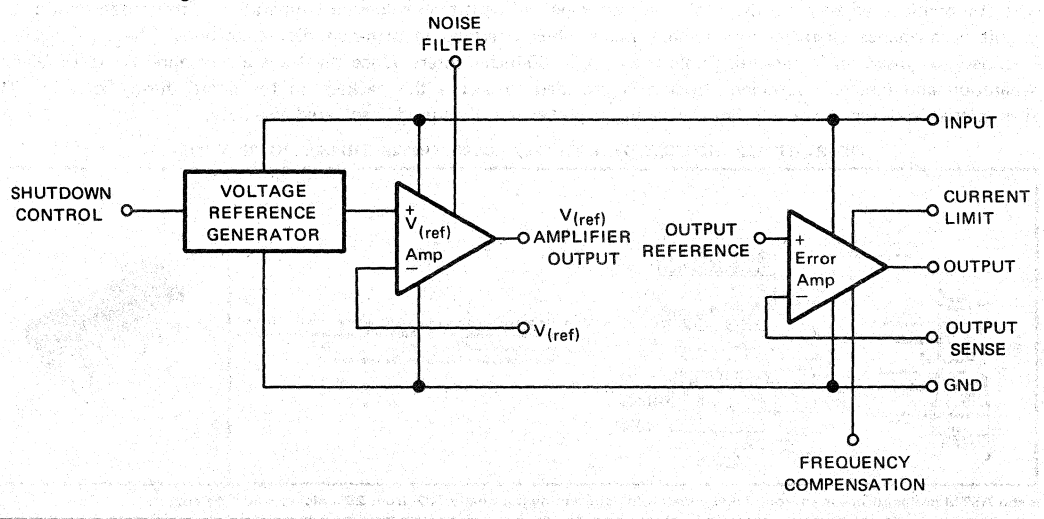
NC—No internal connection

description

The SN72400 voltage regulator is a monolithic integrated circuit featuring a versatile circuit configuration and excellent performance specifications. A temperature-compensated power supply may be constructed by the addition of only two resistors to set the desired output voltage and two capacitors.

The circuit consists of a temperature-compensated reference voltage generator, a reference voltage amplifier, an error amplifier, a 200-milliampere output transistor, a remote shutdown circuit, and an adjustable output current limiter. The device features high ripple rejection, excellent input and load regulation, low temperature sensitivity, and low standby current. The SN72400 is designed for use in positive or negative power supplies as a series, shunt, switching, or floating regulator.

functional block diagram



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Input voltage (see Note 1)	40 V
Input-output voltage differential	40 V
Load current	200 mA
$V_{(ref)}$ amplifier output current	5 mA
Shutdown control voltage (see Notes 1 and 2)	V_I or 10 V
Power dissipation at (or below) 50°C free-air temperature (see Note 3)	800 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds, L package	300°C
Lead temperature 1/16 inch from case for 10 seconds, N package	260°C

NOTES: 1. Voltage values, except input-output voltage differential, are with respect to the network ground terminal.
2. The shutdown control voltage must never exceed the amount of the input voltage or 10 volts, whichever is less.
3. Power dissipation = $(I_I - I_O)\ V_I + (V_I - V_O)\ I_O$. For devices in the L package operating above 50°C free-air temperature, derate linearly at the rate of 8 mW/°C. No derating is required for devices in the N package.

3

recommended operating conditions

	MIN	MAX	UNIT
Input voltage, V_I	8.5	40	V
Output voltage, V_O	2	37	V
Input-to-output voltage differential, $V_I - V_O$	3		V
Output current, I_O	1	200	mA
Operating free-air temperature, T_A	0	70	°C

electrical characteristics (unless otherwise noted, T_A = 25°C, see Note 4)

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input regulation	1	$V_O \approx 5$ V, I_O = 1 mA, V_I = 12 V to 15 V		0.03%	0.1%	
Ripple rejection	3	Ripple frequency = 50 Hz to 10 kHz		60		dB
Load regulation	4	V_I = 15 V, $V_O \approx 10$ V, I_O = 1 mA to 50 mA, T_A = 0°C to 70°C, See Note 5		−0.03%	−0.1%	
Reference voltage, $V_{(ref)}$	1 or 2		2.1	2.3	2.5	V
Standby current	1	V_I = 40 V, I_O = 0		3	8	mA
Temperature coefficient of output voltage	1	T_A = 0°C to 70°C		±0.002		%/°C
Short-circuit output current	1 or 2	R_L = 0, R_{SC} = 7 Ω		91		mA
Output impedance	5	V_I = 14 V, f = 10 kHz		0.02		Ω
Output noise voltage	1	R1 = 0 Ω ($V_O \approx V_{(ref)}$), BW = 10 Hz to 5 MHz		0.1		mV
Minimum shutdown control voltage	6	V_I = 40 V, $I_O \leq 150\ \mu$A			2.4	V
Shutdown control current	6	V_I = 40 V, Shutdown control at 2.4 V		0.8	1.5	mA

NOTES: 4. Unless otherwise specified, V_I = 12 V, V_O = 8 V, I_O = 10 mA, C_N = 0.1 μF.
5. Load regulation is measured using pulsed techniques (t_w = 150 μs, duty cycle = 5%) to limit changes in internal power dissipation. Output voltage drift due to large changes in internal power dissipation must be taken into account separately.

DEFINITION OF TERMS

Input Regulation The percentage change in the output voltage for a specified change in the input voltage.

$$\text{Input Regulation} = \left[\frac{\Delta V_O}{V_O \text{ at } V_I = 12\text{ V}}\right] 100\%$$

Ripple Rejection The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.

Load Regulation The percentage change in the output voltage for a specified change in output current.

$$\text{Load Regulation} = \left(\frac{V_O \text{ at } I_{O(2)} - V_O \text{ at } I_{O(1)}}{V_O \text{ at } I_{O(1)}}\right) 100\%$$

where $I_{O(1)}$ and $I_{O(2)}$ are the specified low and high current extremes, respectively.

Standby Current The input current to the regulator with no load current.

3

Temperature Coefficient of Output Voltage (α_{VO}) The ratio of the difference between the highest and lowest values of output voltage for the full temperature range to the output voltage at 25°C, expressed as a percentage and averaged over the full temperature range.

$$\alpha_{VO} = \pm\left[\frac{V_O \text{ max} - V_O \text{ min}}{V_O \text{ at } 25°C}\right] \frac{100\%}{70°C}$$

Short-Circuit Output Current The output current of the regulator with the output shorted to ground.

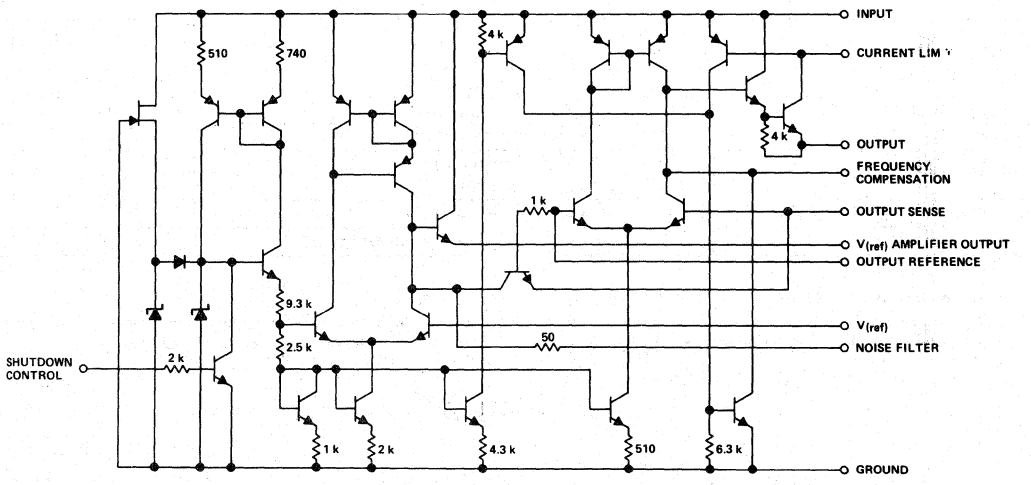
Output Impedance The ratio of a-c rms output voltage to the a-c rms output current.

Output Noise Voltage The rms output noise voltage with a constant load and no input ripple.

Minimum Shutdown Control Voltage The lowest voltage at the shutdown control terminal which will cause the regulator output current to decrease to below a specified value.

Shutdown Control Current The current into the shutdown control terminal.

schematic



All resistor values are nominal in ohms.

NOTE: The frequency compensation terminal is not available on devices in the 10-pin plug-in package (outline L).

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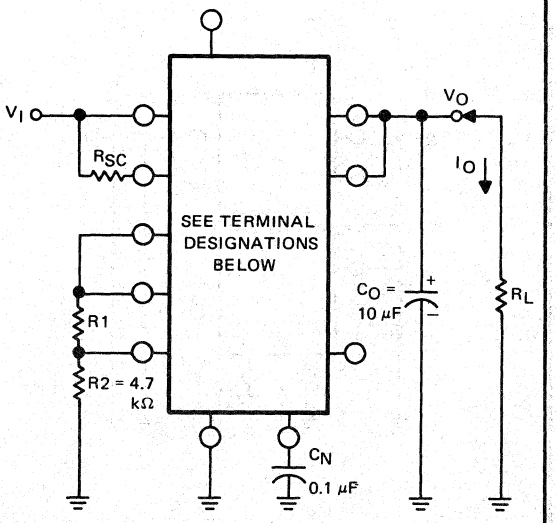
PARAMETER MEASUREMENT INFORMATION

BASIC REGULATOR CONFIGURATION FOR $V_{(ref)} \leq V_O \leq 37$ V



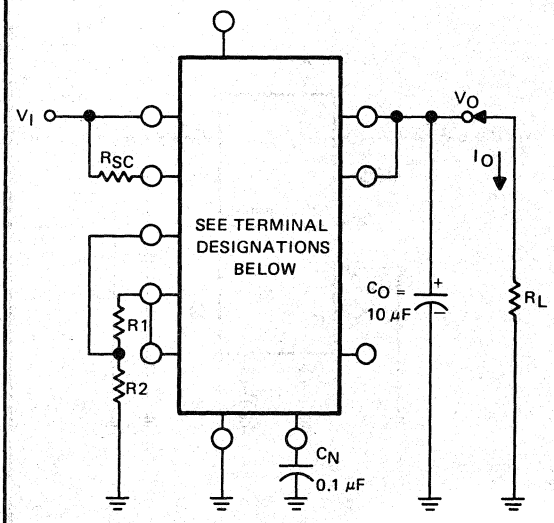
$$V_O = \frac{R1 + R2}{R2} V_{(ref)}$$

For $V_{(ref)} = 2.35$ V and R2 = 4.7 kΩ:

$$R1 = \left(2 \frac{k\Omega}{V}\right) V_O - 4.7\ k\Omega$$

FIGURE 1

BASIC REGULATOR CONFIGURATION FOR $2\ V \leq V_O \leq V_{(ref)}$



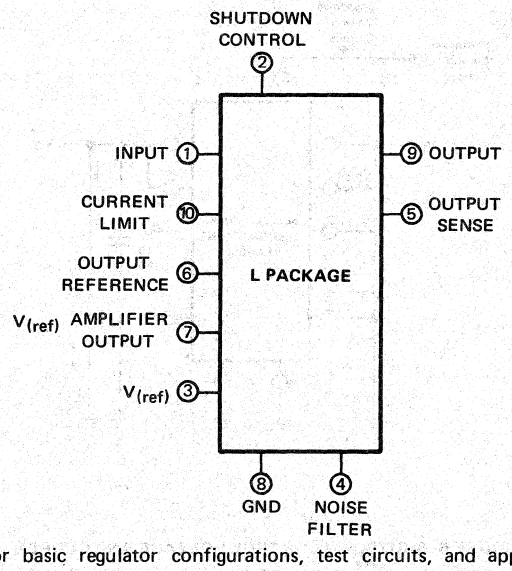
$$V_O = \frac{R2}{R1 + R2} V_{(ref)}$$

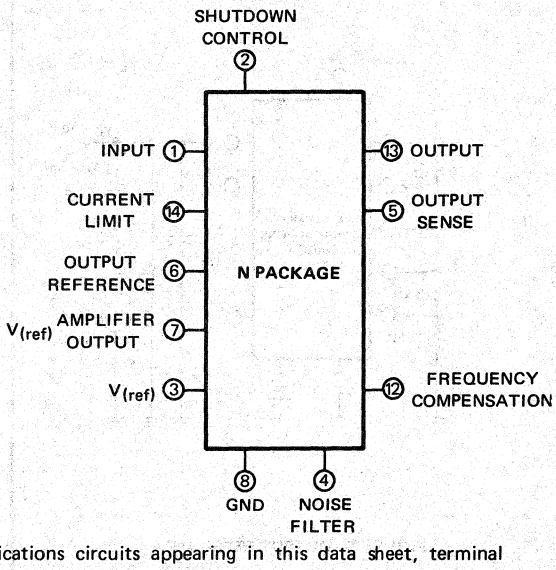
For $V_{(ref)} = 2.35$ V:

$$R2 \approx (2\ V_O)\ k\Omega;\ R1 \approx 4.7\ k\Omega - R2$$

FIGURE 2

TERMINAL DESIGNATIONS





For basic regulator configurations, test circuits, and applications circuits appearing in this data sheet, terminal functions are defined by their relative positions as shown in the drawings above.

PARAMETER MEASUREMENT INFORMATION

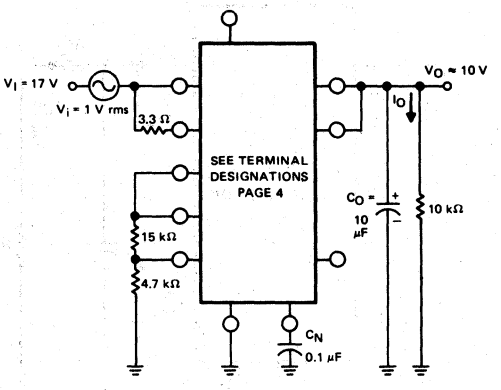


FIGURE 3–RIPPLE REJECTION

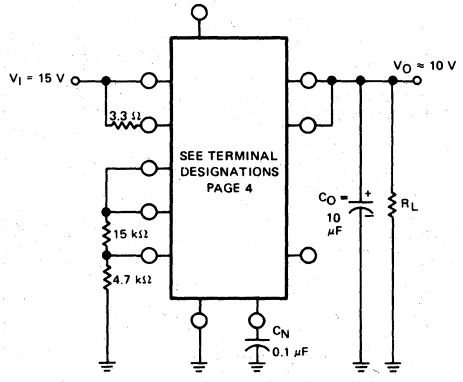


FIGURE 4–LOAD REGULATION

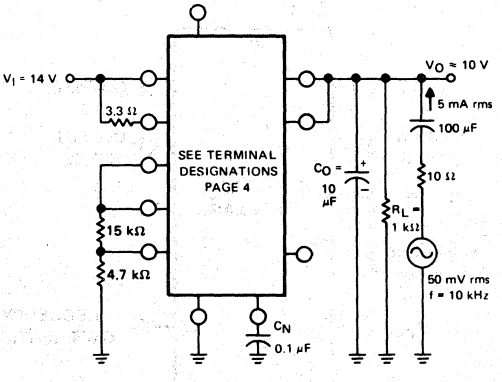


FIGURE 5–OUTPUT IMPEDANCE

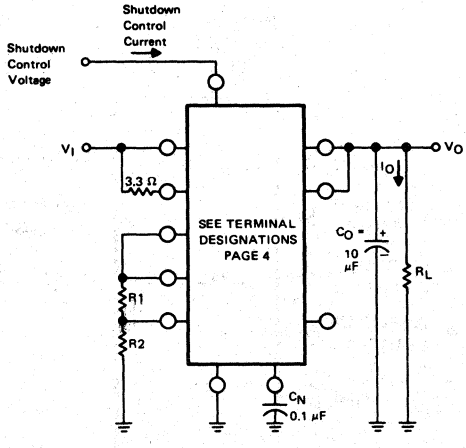


FIGURE 6–SHUTDOWN CONTROL VOLTAGE AND CURRENT

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TYPICAL CHARACTERISTICS

INPUT REGULATION
vs
INPUT-TO-OUTPUT
VOLTAGE DIFFERENTIAL

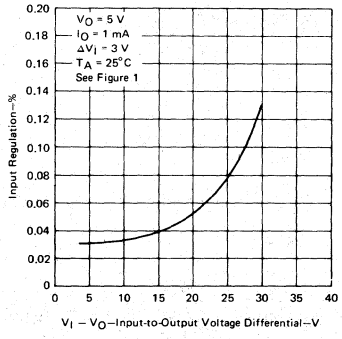

FIGURE 7

LOAD REGULATION
vs
INPUT-TO-OUTPUT
VOLTAGE DIFFERENTIAL

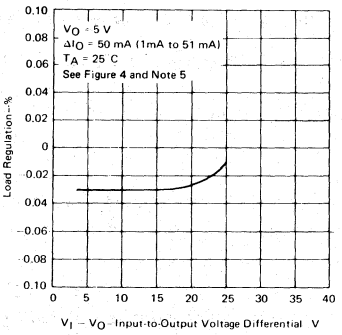

FIGURE 8

STANDBY CURRENT
vs
INPUT VOLTAGE

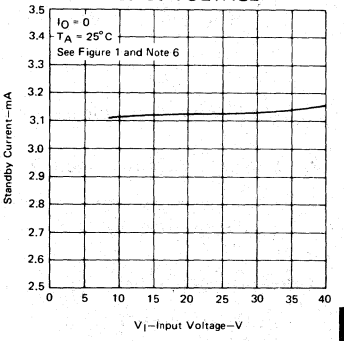

FIGURE 9

CURRENT LIMITING
CHARACTERISTICS

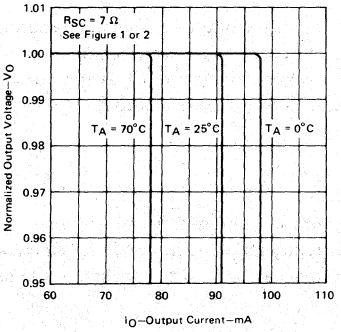

FIGURE 10

OUTPUT IMPEDANCE
vs
FREQUENCY

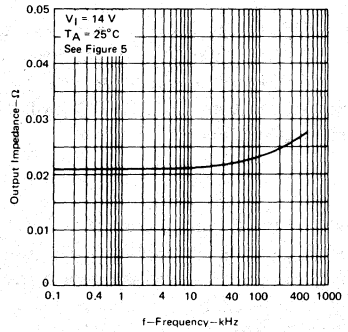

FIGURE 11

TRANSIENT RESPONSE
for
CHANGE IN INPUT VOLTAGE

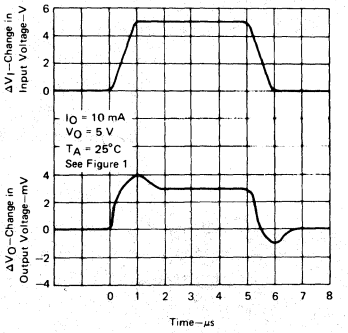

FIGURE 12

TRANSIENT RESPONSE
for
CHANGE IN OUTPUT CURRENT

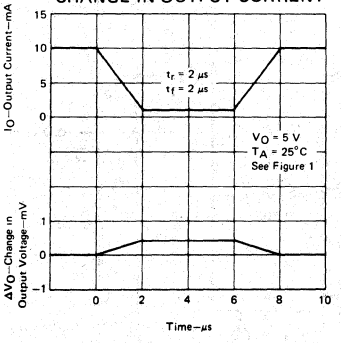

FIGURE 13

TRANSIENT RESPONSE
for
CHANGE IN OUTPUT CURRENT

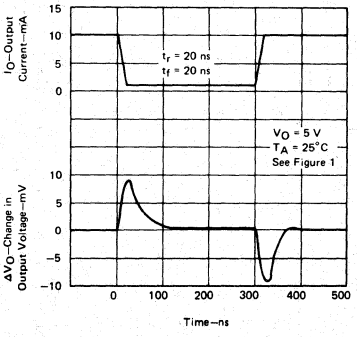

FIGURE 14

THERMAL CHARACTERISTICS

MAXIMUM OUTPUT CURRENT
vs
INPUT-TO-OUTPUT
VOLTAGE DIFFERENTIAL

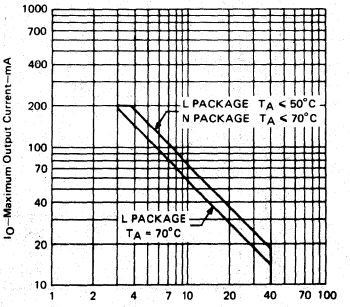

FIGURE 15

NOTES:

5. Load regulation is measured using pulsed techniques (t_W = 150 μs, duty cycle = 5%) to limit changes in internal power dissipation. Output voltage drift due to large changes in internal power dissipation must be taken into account separately.
6. $V_{(ref)}$ amplifier output current is 0.5 mA.

TYPICAL APPLICATION DATA

output voltage

Figures 1 and 2 show basic positive voltage regulator configurations for output voltages from 2 volts to 37 volts. For an adjustable output voltage, make R1 in Figure 1 a potentiometer with a maximum resistance of:

$$R1\ (max) \geqslant \left(2\frac{k\Omega}{V}\right)(V_O\ max) - 4.7\ k\Omega$$

See Figure 16 for the basic negative voltage regulator connections.

short-circuit output current limiting

The maximum output current, I_{OS}, is determined by the magnitude of resistor R_{SC} which is connected between the input and current limit terminals. Select $R_{SC} \approx 0.63$ volts/I_{OS} in amperes.

noise filter capacitor, C_N

A 0.1-μF capacitor from the noise filter terminal to ground will reduce the output noise voltage to typically below 100 μV (rms). The capacitance value can be increased or decreased depending on the application requirements, but a minimum value of 0.001 μF is recommended.

frequency compensation

The compensation technique shown in Figures 1 through 6 (10-μF capacitor, C_O, from the output terminal to ground) is used for optimum transient response. The 14-pin N plastic package provides a separate frequency compensation terminal and, for most applications, a 0.001-μF capacitor from the frequency compensation terminal to the output sense terminal (C_C) is adequate compensation. Larger values of C_C will degrade pulse response and output impedance characteristics and smaller values will reduce stability.

shutdown control

A d-c voltage (2.4 V minimum) applied to the shutdown control terminal will effectively turn off the regulated output voltage, thereby eliminating power consumption by output loading circuitry and greatly reducing the regulator standby current. Standard TTL or DTL IC logic circuits driving the shutdown control terminal can be used to turn the regulator on and off.

CONNECTION FOR A NEGATIVE OUTPUT VOLTAGE

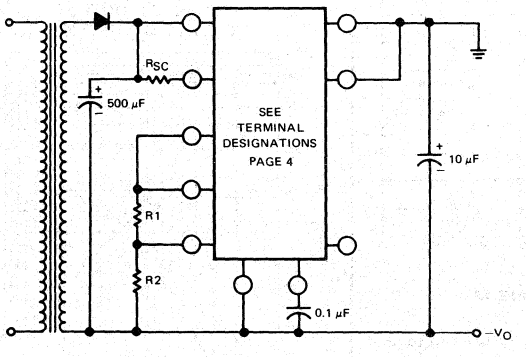

FIGURE 16

POSITIVE VOLTAGE REGULATOR WITH EXTERNAL N-P-N OUTPUT TRANSISTOR

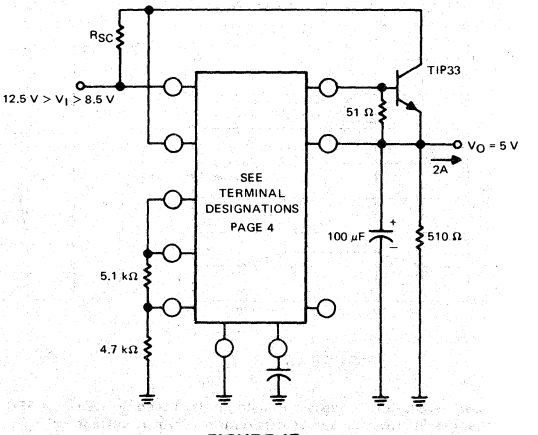

FIGURE 17

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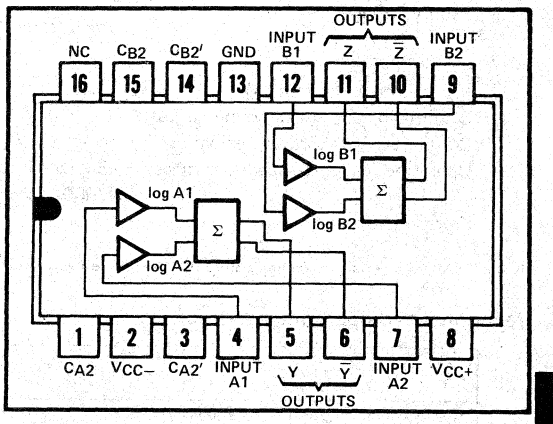
- Excellent Dynamic Range
- Wide Bandwidth
- Built-In Temperature Compensation
- Log Linearity (30 dBV Sections) . . . 1 dBV
- Wide Input Voltage Range

J OR N
DUAL-IN-LINE PACKAGES (TOP VIEW)



3

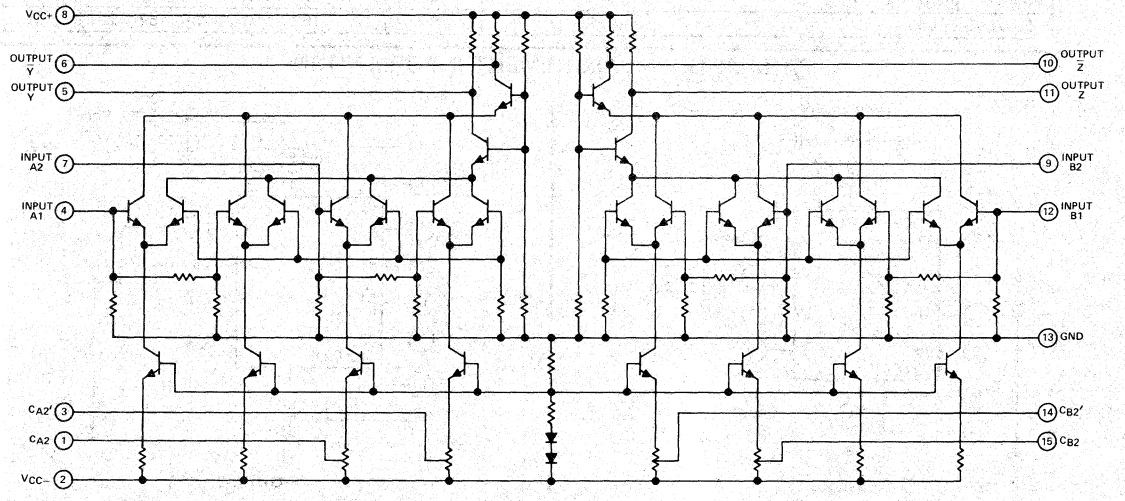
Y∝ log A1 + log A2; Z∝ log B1 + B2
where: A1, A2, B1, and B2 are in dBV, 0 dBV = 1 V.
C_{A2}, $C_{A2'}$, C_{B2}, and $C_{B2'}$, are detector compensation inputs.
NC—No internal connection

description

This monolithic logarithmic amplifier circuit contains four 30-dBV log stages. Gain in each stage is such that the output of each stage is proportional to the logarithm of the input voltage over the 30-dBV input voltage range. Each half of the circuit contains two of these 30-dBV stages summed together in one differential output which is proportional to the sum of the logs of the input voltages of the two stages. The four stages may be interconnected to obtain a theoretical input voltage range of 120 dBV. In practice, this permits the input voltage range to be typically greater than 80 dBV with log linearity of ±0.5 dBV (see application data). Bandwidth is from dc to 40 megahertz.

These circuits are useful in military weapons systems, broadband radar, and infrared reconnaissance systems. They serve for data compression and analog compensation. The logarithmic amplifiers are used in log IF circuitry as well as video and log amplifiers. The SN56502 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN76502 is characterized for operation from 0°C to 70°C.

schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltages (see Note 1):
- V_{CC+} 8V
- V_{CC-} . . . . . −8V

Input voltage (see Note 1) 6V
Output sink current (any one output) . . . . . 30 mA
Continuous total power dissipation . . . . . 500 mW
Operating free-air temperature range: SN56502 Circuits . . . . . −55°C to 125°C
SN76502 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

Note 1: All voltage values, except differential output voltages, are with respect to network ground terminal.

recommended operating conditions

	SN56502			SN76502			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Input voltage for each 30-dBV stage	0.01		1	0.01		1	V_{p-p}
Operating free-air temperature, T_A	−55	25	125	0	25	70	°C

electrical characteristics, V_{CC+} = 6 V, V_{CC-} = −6 V, T_A = 25°C

PARAMETER	TEST FIGURE	SN56502			SN76502			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Differential output offset voltage	1		±25	±60		±40		mV
Quiescent output voltage	2	5.45	5.6	5.85	5.45	5.6	5.85	V
D-c scale factor (differential output), each 30-dBV stage, −35 dBV to −5 dBV	3	7	8	10	6	8	12	mV/dBV
A-c scale factor (differential output)			8			8		mV/dBV
D-c error at −20 dBV (midpoint of −35 dBV to −5 dBV range)	3		1	2		1		dBV
Input impedance			500			500		Ω
Output impedance			200			200		Ω
Rise time, 10% to 90% points, C_L = 24 pF	4		20	25		20	25	ns
Supply current from V_{CC+}	2	14.5	18.5	23	14.5	18.5	23	mA
Supply current from V_{CC-}	2	−6	−8.5	−10.5	−6	−8.5	−10.5	mA
Power dissipation	2	123	162	201	123	162	201	mW

PARAMETER MEASUREMENT INFORMATION

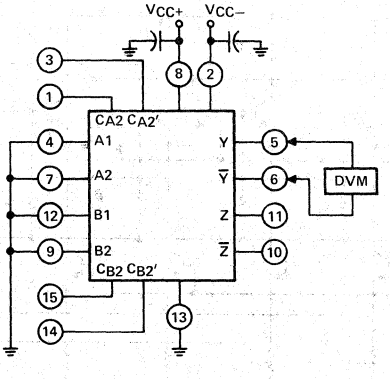


FIGURE 1

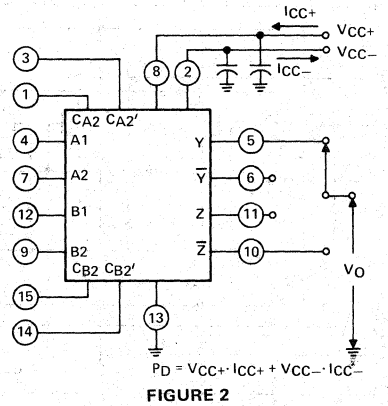


FIGURE 2

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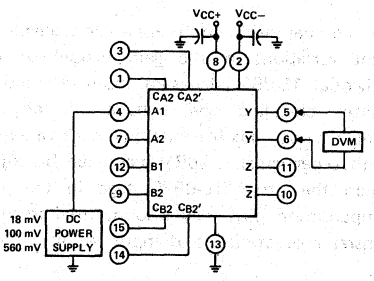
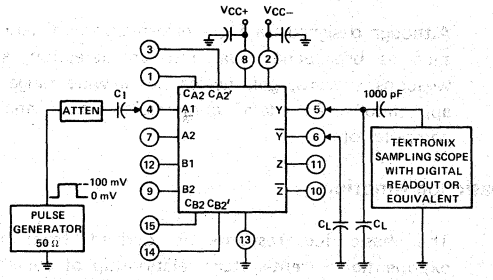
PARAMETER MEASUREMENT INFORMATION



$$\text{Scale Factor} = \frac{[V_{out(560\ mV)} - V_{out(18\ mV)}]\ mV}{30\ dBV}$$

$$\text{Error} = \frac{|V_{out(100\ mV)} - 0.5\ V_{out(560\ mV)} - 0.5\ V_{out(18\ mV)}|}{\text{Scale Factor}}$$

FIGURE 3



NOTES: A. The input pulse has the following characteristics: t_w = 50 ns, $t_r \leq 2$ ns, $t_f \leq 2$ ns, PRR = 10 MHz.

B. Capacitor C_I consists of three capacitors in parallel: 1 μF, 0.1 μF, and 0.01 μF.

C. C_L includes probe and jig capacitance.

FIGURE 4

3

TYPICAL CHARACTERISTICS

SN56502
DIFFERENTIAL OUTPUT OFFSET VOLTAGE
vs
FREE-AIR TEMPERATURE

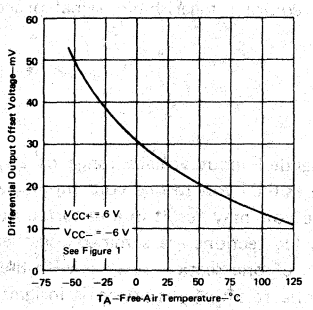


FIGURE 5

QUIESCENT OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

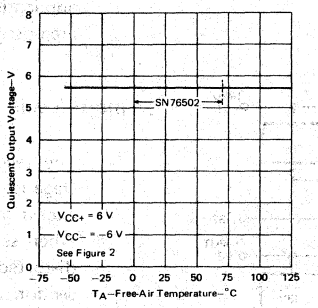


FIGURE 6

SN56502
D-C SCALE FACTOR
vs
FREE-AIR TEMPERATURE

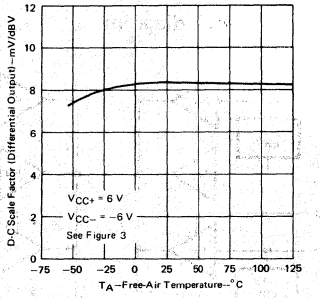


FIGURE 7

SN56502
D-C ERROR
vs
FREE-AIR TEMPERATURE

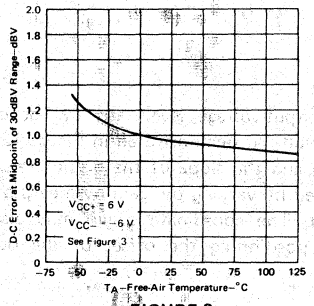


FIGURE 8

OUTPUT RISE TIME
vs
LOAD CAPACITANCE

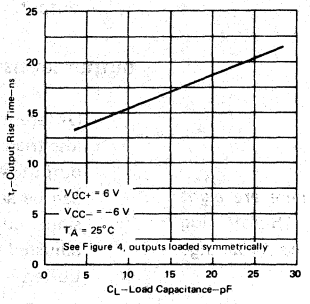


FIGURE 9

POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

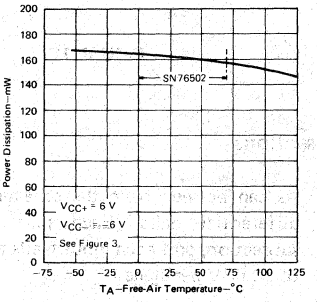


FIGURE 10

TYPICAL APPLICATION DATA

Although designed for high-performance applications such as broadband radar infrared detection, and weapons systems, this device has a wide range of applications in data compression and analog computation.

basic log function

The basic log response is derived from the exponential current-voltage relationship of collector current and base-emitter voltage. This relationship is given in the equation:

$$m \cdot V_{BE} = \ln [(I_C + I_{CES})/I_{CES}]$$

where: I_C = collector current
I_{CES} = collector current at $V_{BE} = 0$
$m = q/kT$ (in V^{-1})
V_{BE} = base-emitter voltage

The differential input amplifier allows dual-polarity inputs, is self-compensating for temperature variations, and is relatively insensitive to noise.

functional block diagram

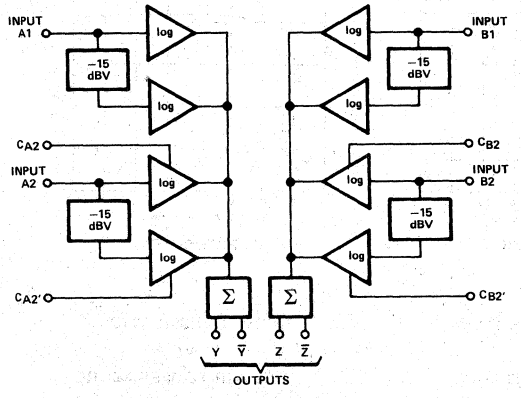


FIGURE 11

log sections

As can be seen from the schematic, there are eight differential pairs. Each pair is a 15-dBV log subsection, and each input feeds two pairs for a range of 30 dBV per stage.

Four compensation points are made available to allow slight variations in the gain (slope) of the two individual 15-dBV stages of input A2 and B2. By slightly changing the voltage on any of the compensation pins from its quiescent value, the gain of that particular 15-dBV stage can be adjusted to match the other 15-dBV stage in the pair. The compensation pins may also be used to match the transfer characteristics of input A2 to A1 or B2 to B1.

The log stages in each half of the circuit are summed by directly connecting their collectors together and summing through a common-base output stage. The two sets of output collectors are used to give two log outputs, Y and $\overline{Y}$ (or Z and $\overline{Z}$) which are equal in amplitude but opposite in polarity. This increases the versatility of the device.

By proper choice of external connections, linear amplification, linear attentuation, and many different applications requiring logarithmic signal processing are possible.

input levels

The recommended input voltage range of any one stage is given as 0.01 volt to one volt. Input levels in excess of one volt may result in a distorted output. When several log sections are summed together, the distorted area of one section overlaps with the next section and the resulting distortion is insignificant. However, there is a limit to the amount of overdrive that may be applied. As the input drive reaches ±3.5 volts, saturation occurs, clamping the collector-summing line and severely distorting the output. Therefore, the signal to any input must be limited to approximately ±3 volts to ensure a clean output.

output levels

Differential-output-voltage levels are low, generally less than 0.6 volt. As demonstrated in Figure 12, the output swing and the slope of the output response can be adjusted by varying the gain by means of the slope control. The coordinate origin may also be adjusted by positioning the offset of the output buffer.

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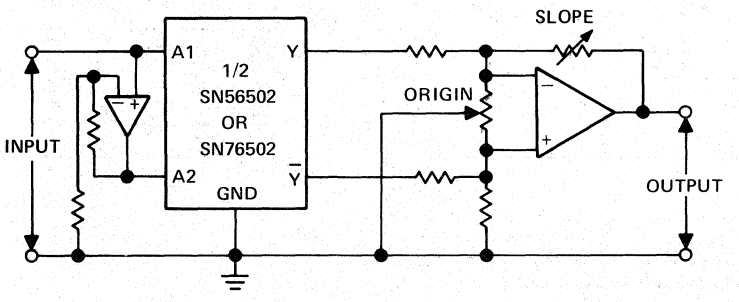
TYPICAL APPLICATION DATA

circuits

Figures 12 through 19 show typical circuits using these logarithmic amplifiers. Operational amplifiers not otherwise designated are SN52741 or SN72741. For operation at higher frequency, use of SN52733/SN72733 is recommended instead of SN52741/SN72741, with the differential outputs connected as in Figure 14. The SN5510/SN7510 or SN5511/SN7511 wideband amplifiers may also be used.



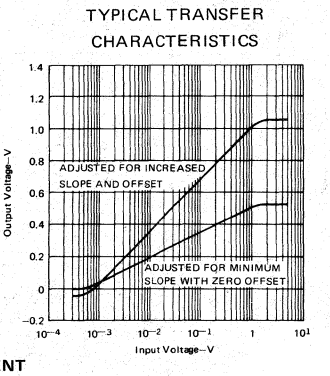
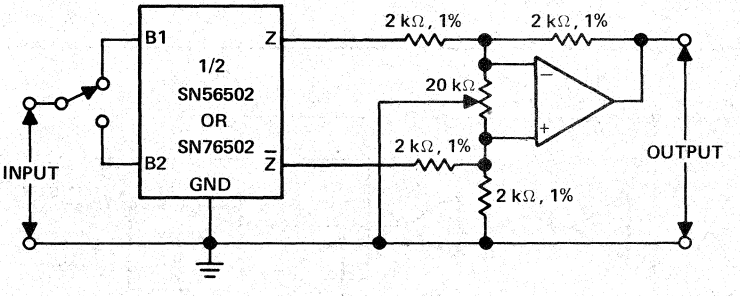


FIGURE 12–OUTPUT SLOPE AND ORIGIN ADJUSTMENT



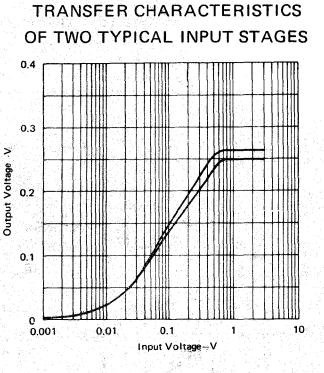
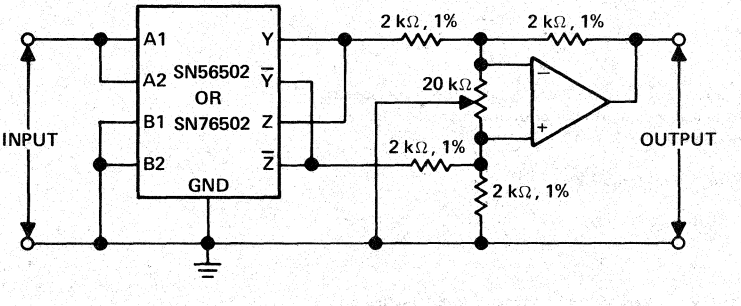


FIGURE 13–UTILIZATION OF SEPARATE STAGES



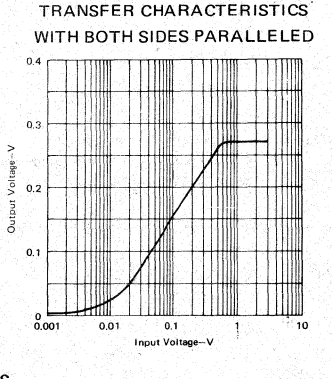
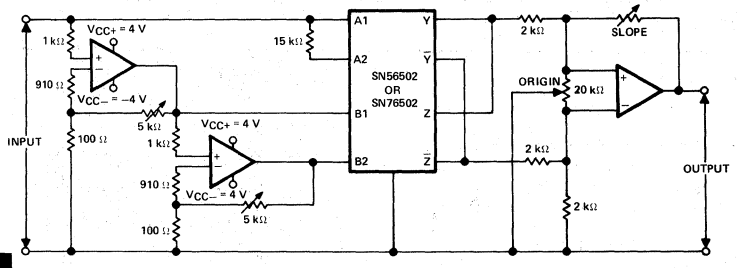
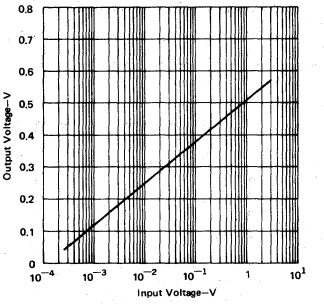


FIGURE 14–UTILIZATION OF PARALLELED INPUTS

TYPICAL APPLICATION DATA



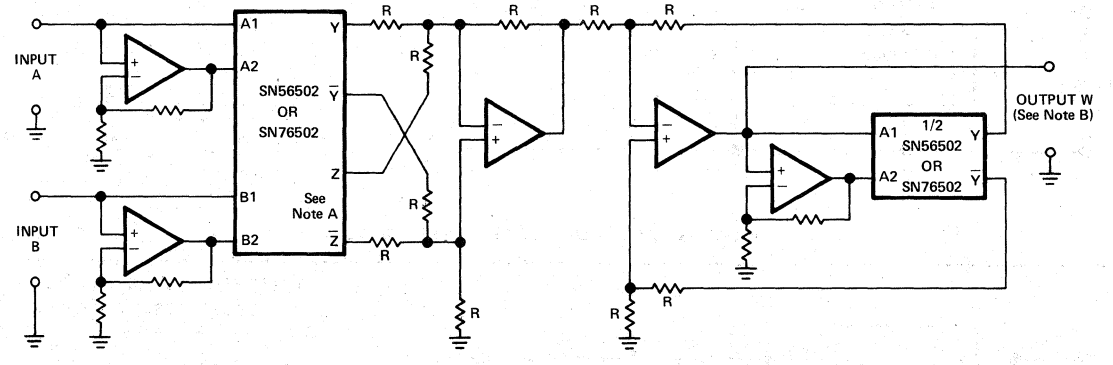
TRANSFER CHARACTERISTICS



3

NOTES: A. Inputs are limited by reducing the supply voltages for the input amplifiers to ±4 V.
B. The gains of the input amplifiers are adjusted to achieve smooth transitions.

FIGURE 15–LOGARITHMIC AMPLIFIER WITH INPUT VOLTAGE RANGE GREATER THAN 80 dBV



NOTES: A. Connections shown are for multiplication. For division, Z and $\overline{Z}$ connections are reversed.
B. Output W may need to be amplified to give actual product or quotient of A and B.
C. R designates resistors of equal value, typically 2 kΩ to 10 kΩ.

Multiplication: $W = A \cdot B \Rightarrow \log W = \log A + \log B$, or $W = a^{(\log_a A + \log_a B)}$

Division: $W = A/B \Rightarrow \log W = \log A - \log B$, or $W = a^{(\log_a A - \log_a B)}$

FIGURE 16–MULTIPLICATION OR DIVISION

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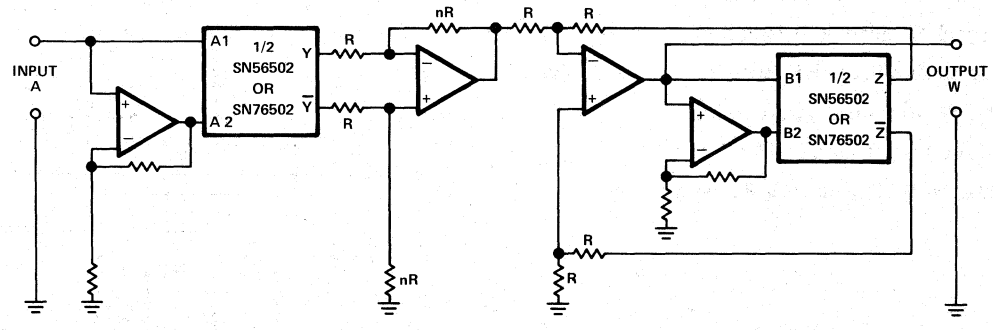
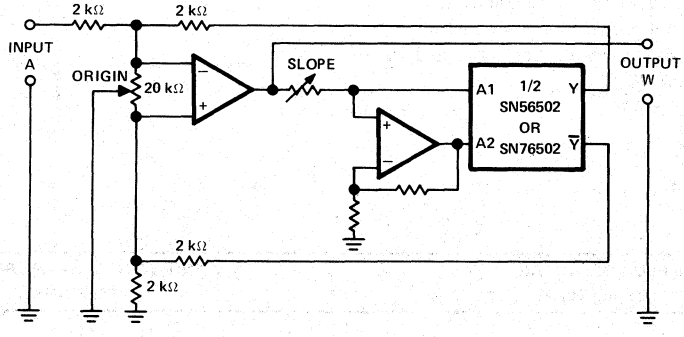
TYPICAL APPLICATION DATA



NOTE: R designates resistors of equal value, typically 2 kΩ to 10 kΩ. The power to which the input variable is raised is fixed by setting nR. Output W may need to be amplified to give the correct value.

Exponential: $W = A^n \Rightarrow \log W = n \log A$, or $W = a^{(n \log_a A)}$

FIGURE 17–RAISING A VARIABLE TO A FIXED POWER



NOTE: Adjust the slope to correspond to the base "a".

Exponential to any base: W = a

FIGURE 18–RAISING A FIXED NUMBER TO A VARIABLE POWER

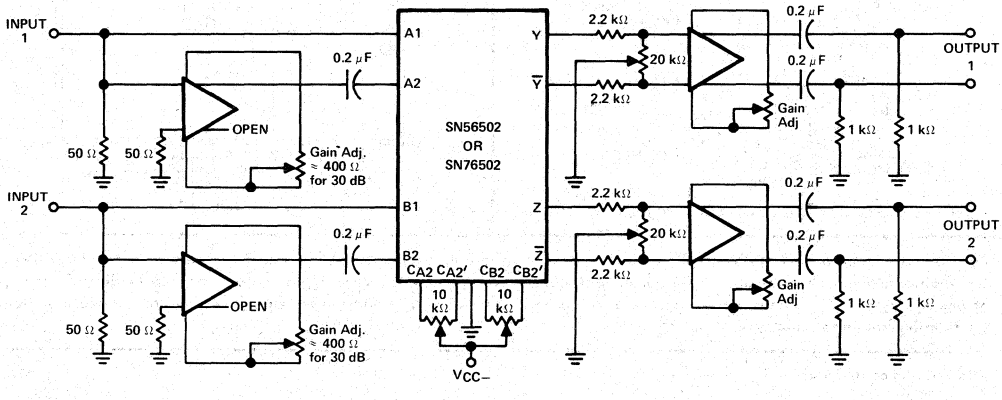
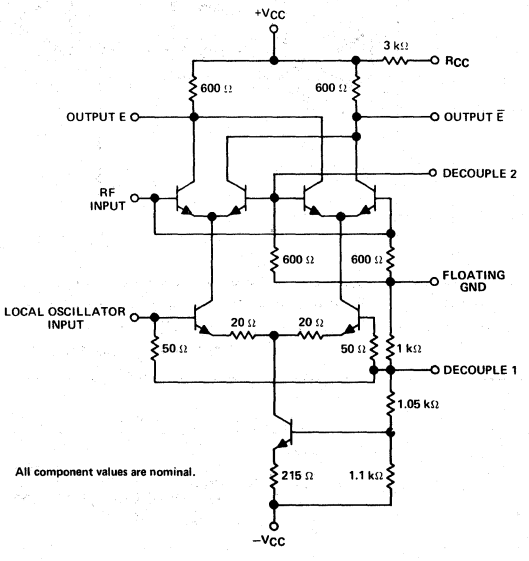


FIGURE 19–DUAL-CHANNEL RF LOGARITHMIC AMPLIFIER WITH 50-dB INPUT RANGE PER CHANNEL AT 10 MHz

CIRCUIT TYPES SN56514, SN76514
BALANCED MIXERS

- Flat Response to 100 MHz
- Local Oscillator IF Isolation . . . 30 dB Typ
- Local Oscillator RF Isolation . . . 60 dB Typ
- RF-IF Isolation . . . 30 dB Typ
- Conversion Gain . . . 14 dB Typ
- Use with 12-V or ±6-V Power Supplies

schematic



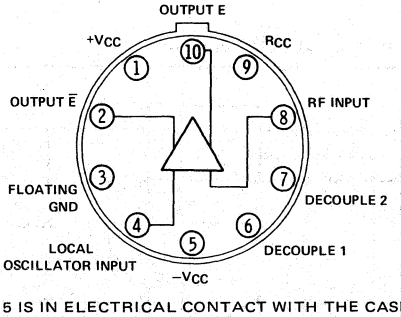
description

3

The SN56514 and SN76514 are doubly balanced mixers which utilize two cross-coupled, differential transistor pairs driven by a third balanced pair. The circuit features a flat response over a wide band of frequencies. The SN56514 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN76514 is characterized for operation from 0°C to 70°C.

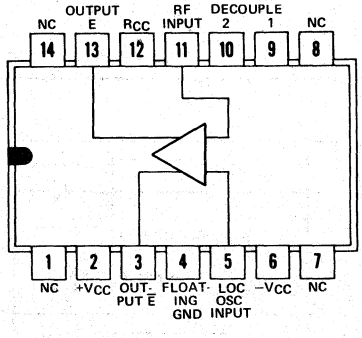
terminal assignments

L PLUG-IN PACKAGE
(TOP VIEW)



PIN 5 IS IN ELECTRICAL CONTACT WITH THE CASE

J AND N DUAL-IN-LINE PACKAGES
(TOP VIEW)



For operation from a single 12-V supply, connect the positive terminal of the supply to $+V_{CC}$, the negative terminal to $-V_{CC}$, and the floating-ground terminal to R_{CC}. For operation from two 6-V supplies, leave R_{CC} open and connect the positive terminal of one supply to $+V_{CC}$, the negative terminal of the other supply to $-V_{CC}$, and the remaining terminals of the two supplies to the floating-ground terminal. See Figure 19.

NC—No internal connection

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	18 V
Input voltage (see Notes 1 and 2)	7 V
Continuous output current (see Note 3)	10 mA
Continuous total power dissipation at (or below) 70°C free-air temperature (see Note 4)	500 mW
Operating free-air temperature range: SN56514 Circuits	−55°C to 125°C
SN76514 Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		12		V
Local oscillator input voltage (see Note 5)		250	300	mV p-p
RF input voltage (see Note 5)		10	30	mV p-p
Operating free-air temperature range: SN56514 Circuits	−55	25	125	°C
SN76514 Circuits	0	25	70	°C

electrical characteristics at 25°C free-air temperature, V_{CC} = 12 V

PARAMETER		TEST FIGURE	TEST CONDITIONS	SN56514			SN76514			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_O	Quiescent output voltage	1		9.6	10.5	11.3	9.6	10.5	11.3	V
I_{CC}	Supply current	1		5.5	7.4	10.9	5.5	7.4	10.9	mA
G_C	Conversion gain (single-ended output)	2	f_{RF} and f_{LO} = 100 kHz thru 40 MHz	11	14	17	11	14	17	dB
LOIFI	Local oscillator to IF isolation	3	f_{LO} = 100 kHz thru 40 MHz	15	29†			29†		dB
LORFI	Local oscillator to RF isolation	3	f_{LO} = 100 kHz thru 40 MHz	40	52†			52†		dB
RFIFI	RF to IF isolation	4	f_{RF} = 100 kHz thru 40 MHz	15	28†			28†		dB

†The typical values are at 40 MHz.

NOTES: 1. All d-c voltage values are with respect to $-V_{CC}$ terminal.
2. This rating applies to the local-oscillator input, RF input, and Decouple 2.
3. This value applies for both outputs simultaneously.
4. For operation of SN56514 above 70°C free-air temperature, refer to Dissipation Derating Curve, Figure 18.
5. All signal voltages are with respect to the floating-ground terminal. Alternatively, the RF input may be applied differentially between the RF input terminal and Decouple 2.

PARAMETER MEASUREMENT INFORMATION

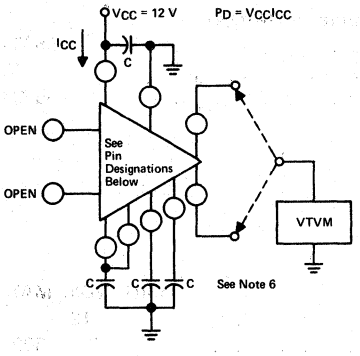


FIGURE 1–V_O, I_{CC}, and P_D

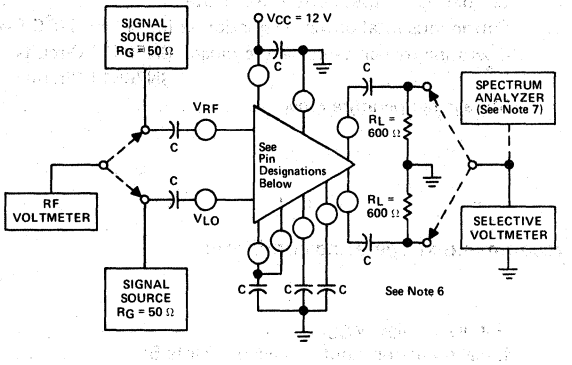


FIGURE 2–G_C

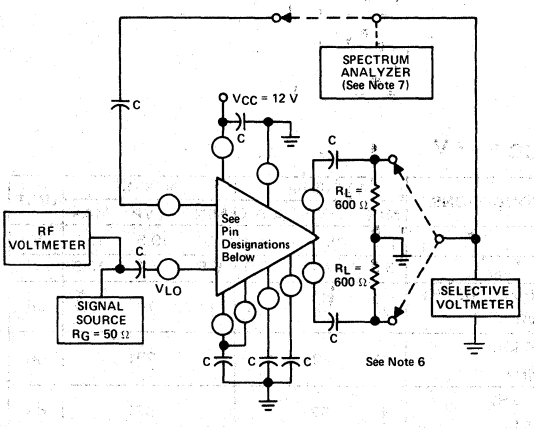


FIGURE 3–LOIFI and LORFI

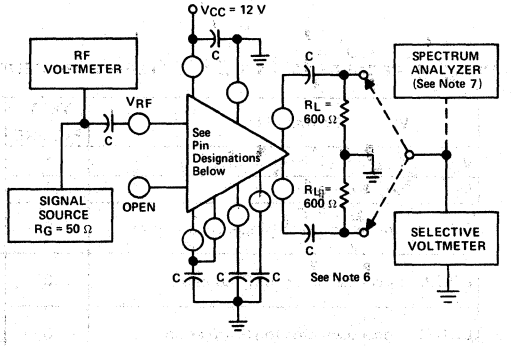
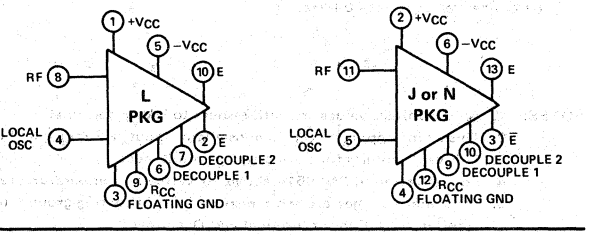


FIGURE 4–RFIFI

Pin Designations: For all test circuits appearing in this data sheet, terminal functions are defined by their relative positions as shown in the drawings in this block.



NOTES: 6. Capacitor C comprises the following capacitors in parallel: 1 μF, 0.1 μF, and 0.0015 μF.
7. The spectrum analyzer is used for frequencies above the normal range of the selective voltmeter.

TEXAS INSTRUMENTS
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TYPICAL CHARACTERISTICS

QUIESCENT OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

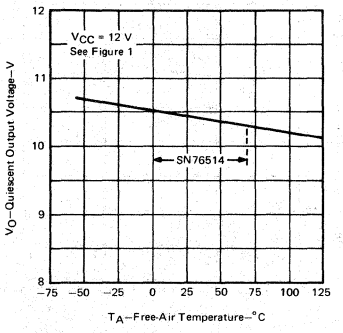

FIGURE 5

TOTAL POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

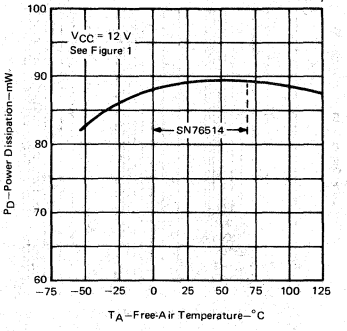

FIGURE 6

CONVERSION GAIN
vs
SUPPLY VOLTAGES

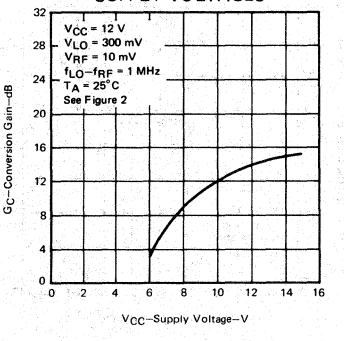

FIGURE 7

CONVERSION GAIN
vs
LOCAL OSCILLATOR VOLTAGE

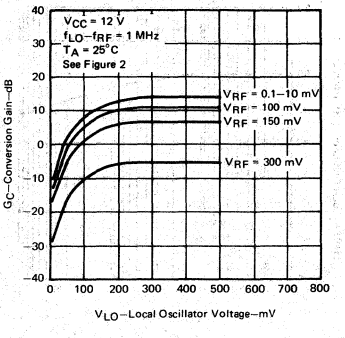

FIGURE 8

CONVERSION GAIN
vs
FREQUENCY

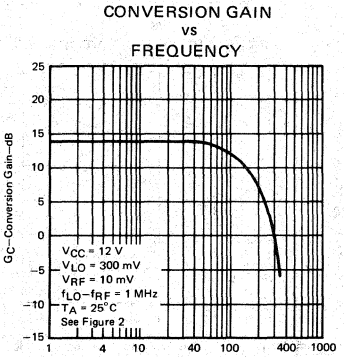

FIGURE 9

CONVERSION GAIN
vs
FREE-AIR TEMPERATURE

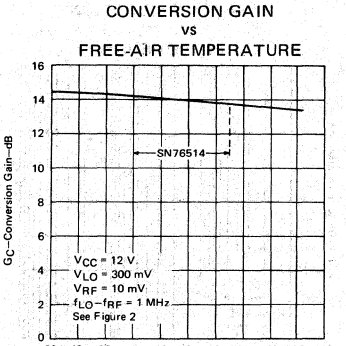

FIGURE 10

TYPICAL CHARACTERISTICS

LOCAL OSCILLATOR TO IF ISOLATION
vs
FREQUENCY

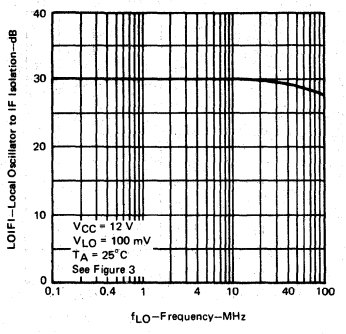

FIGURE 11

LOCAL OSCILLATOR TO IF ISOLATION
vs
FREE-AIR TEMPERATURE

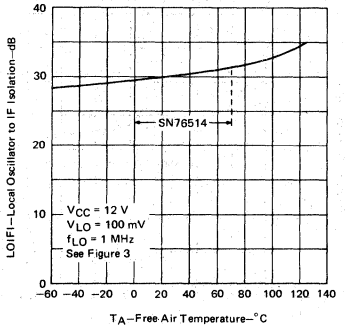

FIGURE 12

LOCAL OSCILLATOR TO RF ISOLATION
vs
FREQUENCY

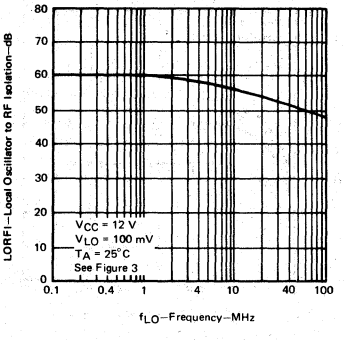

FIGURE 13

LOCAL OSCILLATOR TO RF ISOLATION
vs
FREE-AIR TEMPERATURE

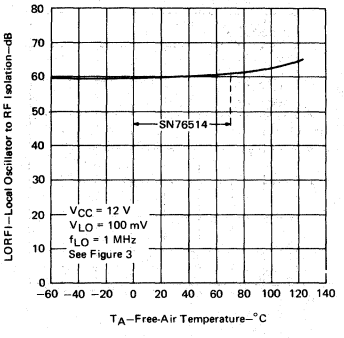

FIGURE 14

RF TO IF ISOLATION
vs
FREQUENCY

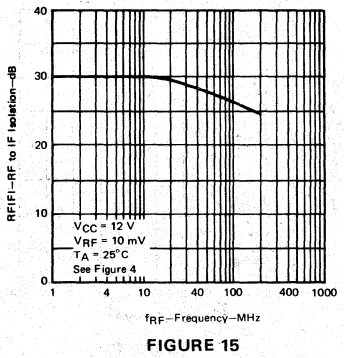

FIGURE 15

RF TO IF ISOLATION
vs
FREE-AIR TEMPERATURE

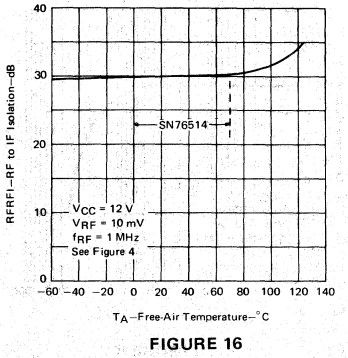

FIGURE 16

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TYPICAL CHARACTERISTICS

SIDEBAND HARMONIC SUPPRESSION
vs
LOCAL OSCILLATOR FREQUENCY

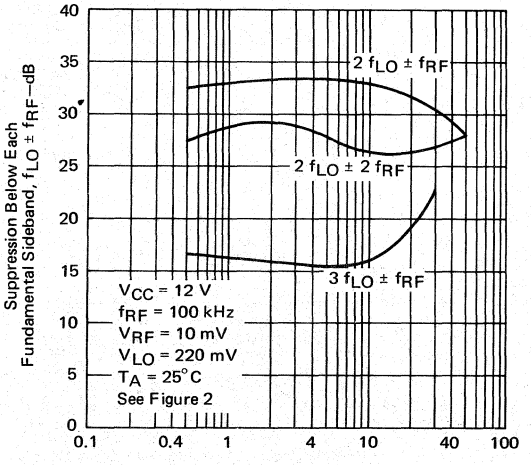


FIGURE 17

THERMAL INFORMATION

DISSIPATION DERATING CURVE

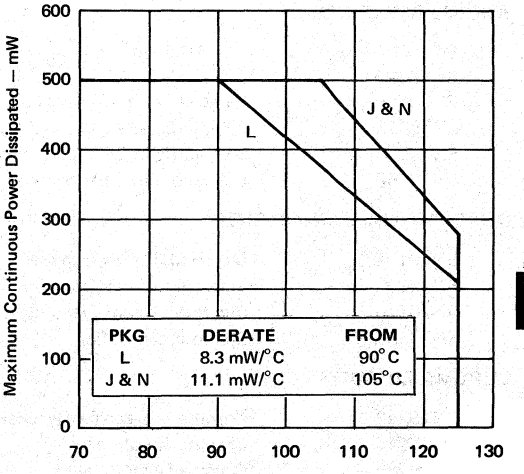


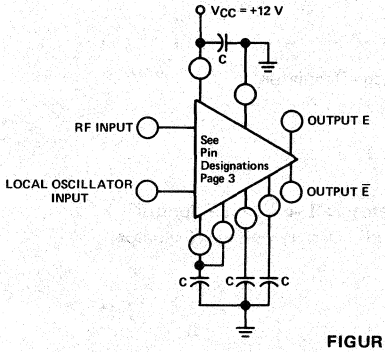
FIGURE 18

TYPICAL APPLICATION DATA

The SN55514 and SN75514 balanced mixers are designed to have considerable circuit flexibility which results in a wide range of applications. Typical applications include use as balanced modulators for sideband-suppressed-carrier generation, product detectors for demodulation, frequency converters, and frequency or phase modulators. In addition, the SN55514 and SN75514 may be used in control systems and analog computers as low-level multipliers or squaring circuits.

The circuits are designed to operate from either a single 12-V supply or two 6-V supplies. Electrical characteristics will be unchanged with the use of either power supply option. External bypass capacitors, as shown in Figure 19, should be used for optimum performance.

The mixer's electrical performance and the inherent IC advantages of size, reliability, and component matching make it very desirable for use in communication and control systems.



NOTE: Capacitor C comprises the following capacitors in parallel: 1 μF, 0.1 μF, and 0.0015 μF.

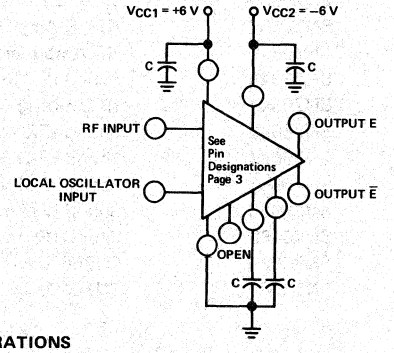


FIGURE 19—EXTERNAL CAPACITOR CONFIGURATIONS

CONSUMER CIRCUITS SUMMARY

Following is a listing of Consumer Circuits presently available from Texas Instruments. Should you desire additional information, application engineering advice, or sales assistance, please contact your nearest TI Sales office.

AUDIO AMPLIFIERS

SN76001	1 W Audio at 9 V and 8 Ω
SN76003	3 W Audio at 30 V and 16 Ω
SN76010	Same as SN76001 except for different pin arrangement
SN76013	3 W Audio at 24 V and 8 Ω
SN76005	5 W Audio at 34 V and 16 Ω
SN76050	5 W Audio at 14 V and 4 Ω

DUAL CHANNEL AND STEREO

SN76104	Stereo Multiplex Decoder
SN76105	Stereo Multiplex Decoder
SN76110	Stereo Multiplex Decoder
SN76131	Stereo Preamplifier

CHROMA CIRCUITS

SN76242	Chroma Sub-carrier Regenerator
SN76243	Chroma Amplifier
SN76246	Chroma Demodulator
SN76630	PAL Chroma Demodulator

COMPLEX TV FUNCTIONS

SN76530	Video Detector
SN76532	TV Jungle (suitable for horizontal deflection with tubes)
SN76533	TV Jungle (suitable for horizontal deflection with semiconductors)
SN76540	TV Jungle for N-P-N Tuners and Ge Diode Detection
SN76541	TV Jungle for N-P-N Tuners and Low Level Detection
SN76542	TV Jungle for P-N-P Tuners and Ge Diode Detection
SN76564	Automatic Fine Tuning

REGULATORS FOR VARACTOR TUNERS

SN76550	33 V at 5 mA
SN76552	22 V at 5 mA
SN76553	12 V at 5 mA

IF CIRCUITS FOR RADIO AND TV

SN76600	1st and 2nd Video IF Stages
SN76603	RF/IF Amplifier
SN76619	RF Amplifier/FM Detector
SN76640	Sound IF/Limiter, Slope Detector, Audio Driver, Voltage Regulator
SN76641	IF Limiting Amplifier
SN76642	Sound IF/Detector
SN76643	Sound IF/Detector
SN76650	1st and 2nd Video IF with Keyed AGC
SN76660	Sound IF/Amplifier Limiter, Balanced Coincidence Detector, D-c Volume Control
SN76665	Sound IF/Amplifier Limiter, Detector, Attenuator, Audio Driver, Voltage Regulator
SN76670	SN76660 with Open-Collector Output
SN76680	SN76660 with Audio Driver and Voltage Regulator

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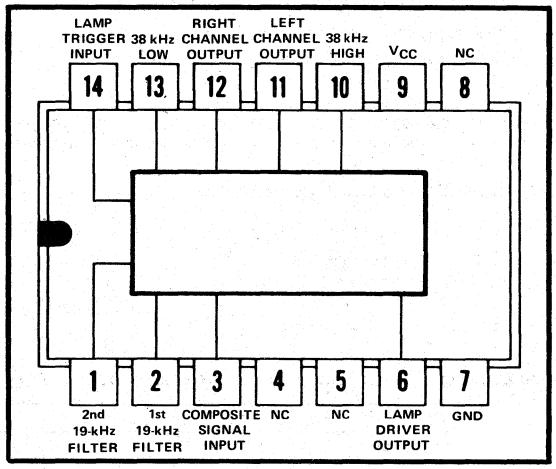
FOR USE IN FM MULTIPLEX SYSTEMS

- Designed to be Interchangeable with Motorola MC1307P
- Power Supply Range . . . 8 to 14 V
- Low Harmonic Distortion
- Stereo-Indicator Lamp Driver
- Monaural Squelch Capability

N
DUAL-IN-LINE PACKAGE (TOP VIEW)

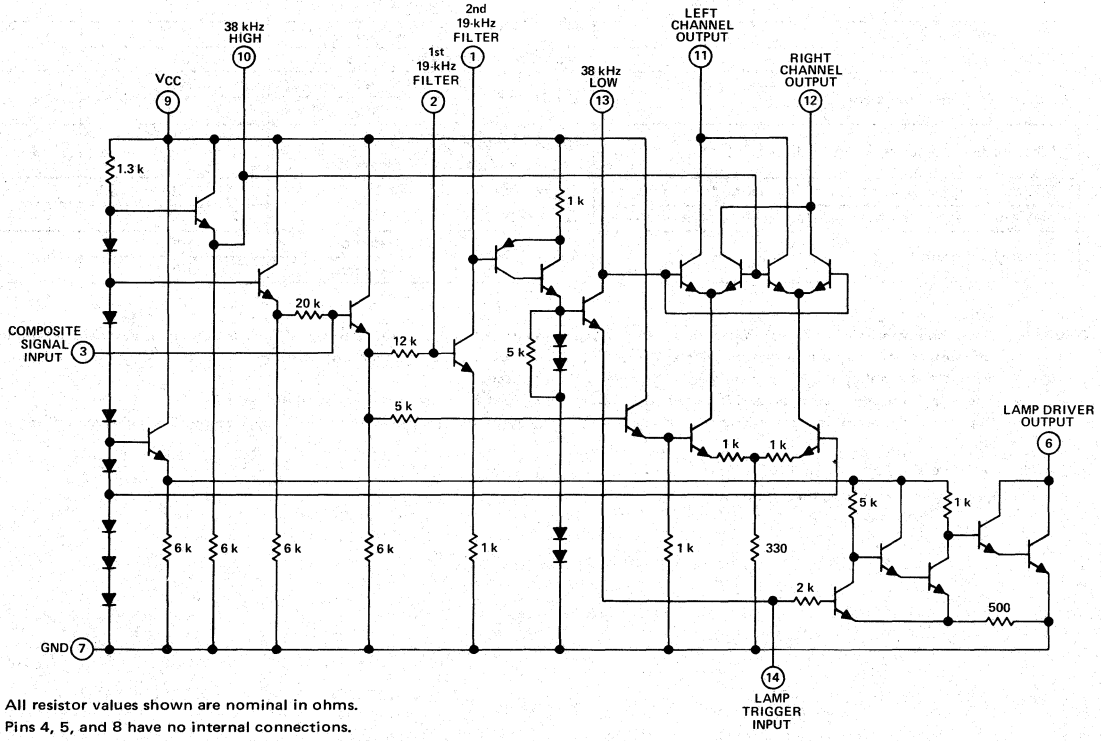


NC—No internal connection

description

The SN76110 is a monolithic integrated circuit designed to process the detected composite multiplex signal. The circuit provides left-channel and right-channel separation and balance, and also has a driver output for a stereo-indicator lamp.

schematic



All resistor values shown are nominal in ohms.
Pins 4, 5, and 8 have no internal connections.

CIRCUIT TYPE SN76110
STEREO DEMODULATOR

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 22 V
Lamp driver current . . . . . 40 mA
Power dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 625 mW
Operating free-air temperature range . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Derate linearly to 375 mW at 75°C free-air temperature at the rate of 5 mW/°C.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	8	12	14	V
Operating free-air temperature, T_A	0	25	75	°C

3

electrical characteristics (unless otherwise noted V_{CC} = 8 V to 14 V, T_A = 25°C, see figure 1)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
Input impedance	f = 1 kHz			20		kΩ
Stereo channel separation	See Note 3	f_{mod} = 100 Hz		40		dB
		f_{mod} = 1 kHz	30	45		
		f_{mod} = 10 kHz		35		
Total harmonic distortion	f_{mod} = 1 kHz, See Notes 3 and 4			0.3%		
Channel balance	Monaural input = 200 mV rms			0.5	1	dB
Ultrasonic frequency rejection	See Note 5	f = 19 kHz		25		dB
		f = 38 kHz		20		
Inherent SCA rejection (without filter)	f_{mod} = 60 kHz to 74 kHz, See Notes 4 and 5 and Figure 2			55‡		dB
Minimum trigger input for on state at lamp-driver output	Trigger frequency = 19 kHz,			10	20	mV rms
Maximum trigger input for off state at lamp-driver output	R1 = 180 Ω		2	6		
Power dissipation	V_{CC} = 12 V	lamp off		140		mW
		lamp on		170		

NOTES: 3. These characteristics are measured with a 564-mV p-p standard multiplex composite signal. This is defined as a signal containing left and/or right audio modulation with a 10-percent, 19-kHz pilot signal in accordance with FCC regulations. For stereo testing, both left-channel-only and right-channel-only modulation are used.
4. The total harmonic distortion and SCA rejection values apply for both stereo and monaural operation.
5. Rejection is referenced to a 1-kHz output signal produced by a 364-mV p-p standard multiplex composite signal as defined in Note 3.

†All typical values are at V_{CC} = 12 V.

‡This is the lowest value for the specified frequency range.

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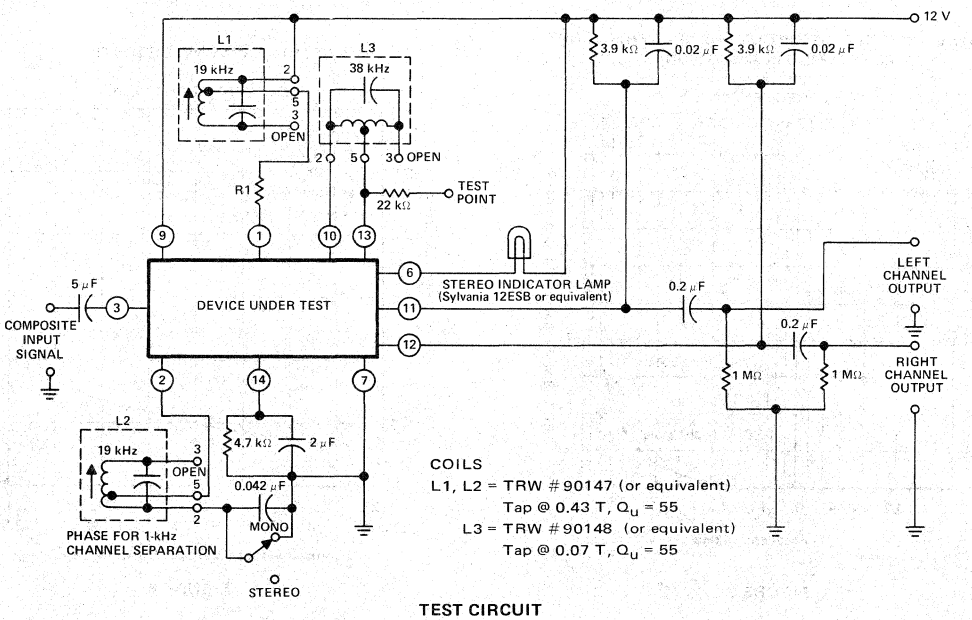
PARAMETER MEASUREMENT INFORMATION



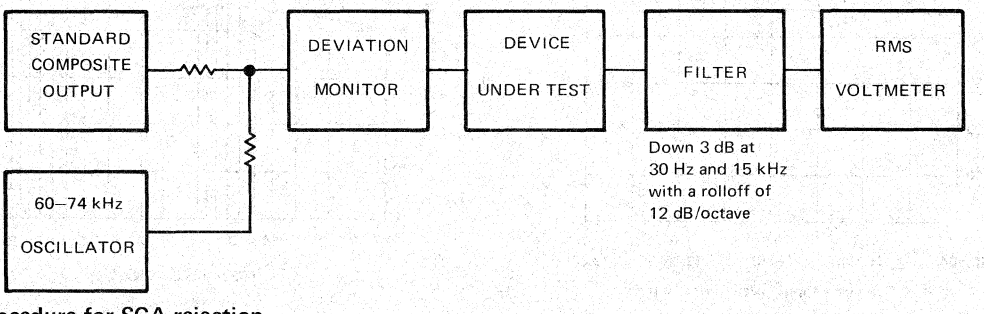
TEST CIRCUIT

typical voltages with respect to pin 7, V_{CC} = 12 V, R1 = 180 Ω, lamp on, measured using a VTVM

Pin Number	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Volts	11.8	3.2	3.9	NC	NC	0.9	0	NC	12	4.8	8.8	8.8	4.8	1.7

NC—No internal connection

FIGURE 1



test procedure for SCA rejection

1. Modulate the stereo generator with a 1-kHz reference signal.
2. Adjust output for 67.5 kHz deviation.
3. Remove the 1-kHz reference signal.
4. Alternately adjust a 19-kHz pilot signal and a 60-kHz to 74-kHz external signal to deviate 6.7-kHz.
5. Rejection is defined as the difference in dB between the magnitude of the 1-kHz reference signal and the audio components present due to the interaction of the 19-kHz and 38-kHz components with the 60-kHz to 74-kHz signal.

FIGURE 2

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION AND BEAT FREQUENCY COMPONENTS IN AUDIO SIGNAL vs FREQUENCY

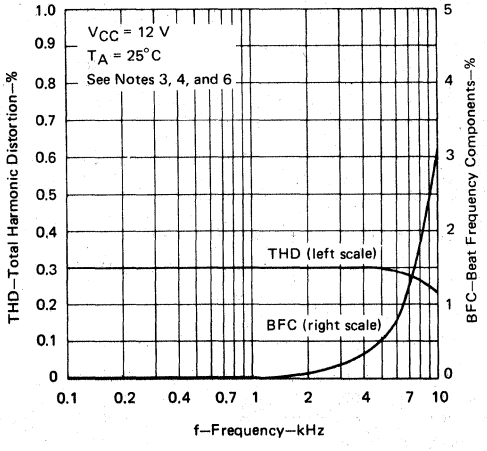


FIGURE 3

TOTAL HARMONIC DISTORTION vs COMPOSITE INPUT LEVEL

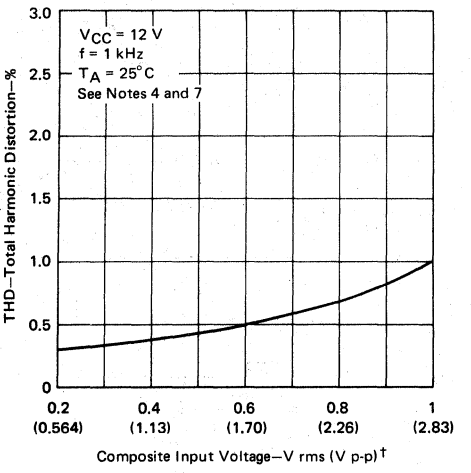


FIGURE 4

CHANNEL SEPARATION vs COMPOSITE INPUT LEVEL

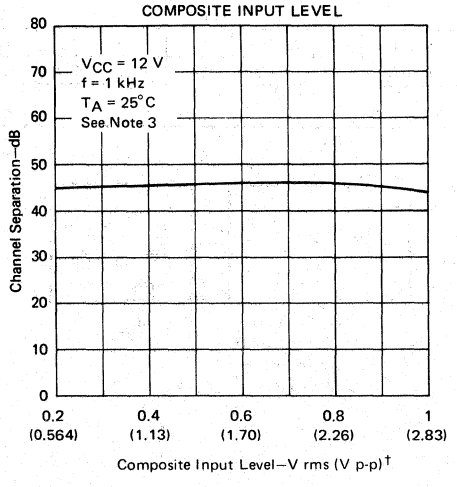


FIGURE 5

CHANNEL SEPARATION vs FREQUENCY

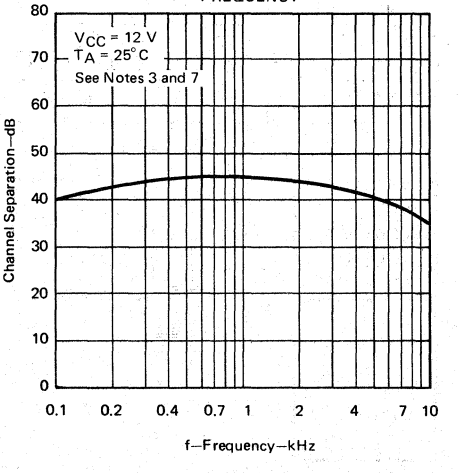


FIGURE 6

NOTES: 3. These characteristics are measured with a 564-mV p-p standard multiplex composite signal. This is defined as a signal containing left and/or right audio modulation with a 10-percent, 19-kHz pilot signal in accordance with FCC regulations. For stereo testing, both left-channel-only and right-channel-only modulation are used.
4. The total harmonic distortion and SCA rejection values apply for both stereo and monaural operation.
6. Beat frequency components (BFC) result from the presence of the 19-kHz pilot signal in stereo broadcasts.
7. Input signal is a 1-kHz composite signal, 846 mV p-p.

†The rms scale is valid for monaural modulation (L=R) only. The peak-to-peak scale is valid for monaural or stereo modulation.

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TYPICAL CHARACTERISTICS

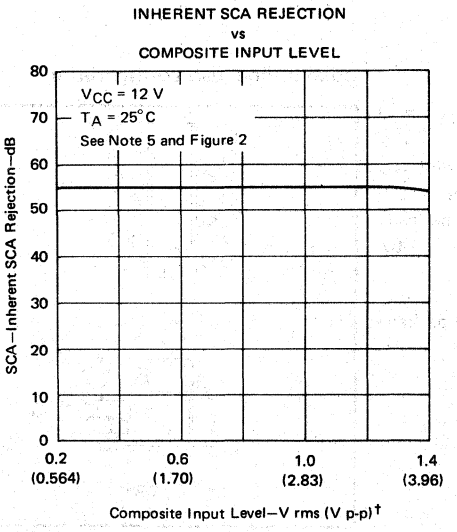


FIGURE 7

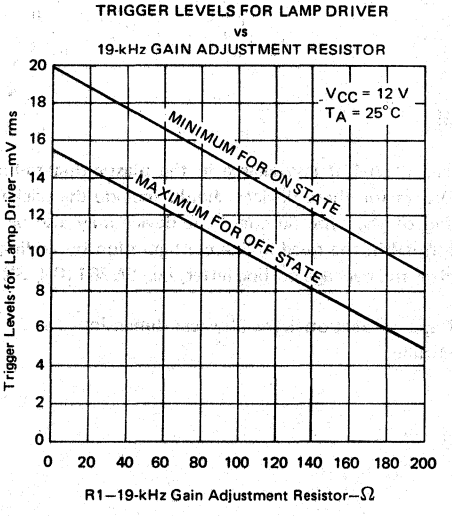


FIGURE 8

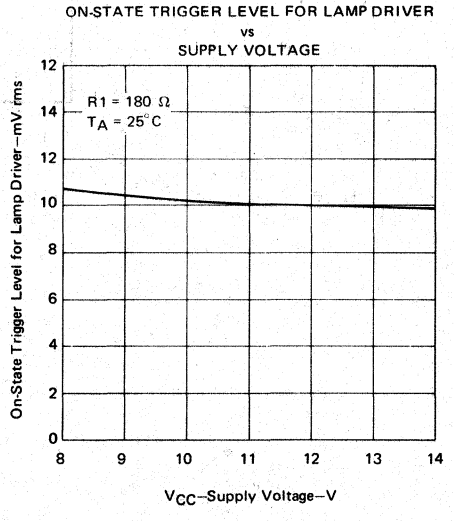


FIGURE 9

NOTE 5: Rejection is referenced to a 1-kHz output signal produced by a 364-mV p-p standard multiplex composite signal as defined in Note 3.

† The rms scale is valid for monaural modulation (L=R) only. The peak-to-peak scale is valid for monaural or stereo modulation.

CIRCUIT TYPE SN76110
STEREO DEMODULATOR

ORDERING INSTRUCTIONS AND MECHANICAL DATA

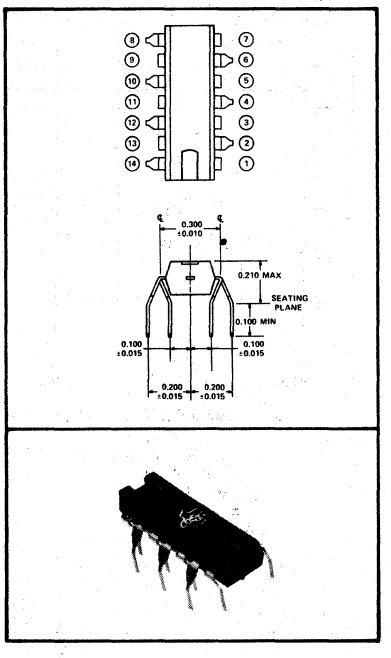
general

The SN76110 is available in the plastic dual-in-line package (outline N). Orders for these devices should include the package outline letter at the end of the type number. The device may also be ordered with the leads formed in the quad-in-line configuration by adding the dash number –07 after the package outline letter, i.e., SN76110N, SN76110N–07.

Refer to Section 1 for physical dimensions for the dual-in-line N-package outline.

3

quad-in-line lead configuration



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4

ECL Circuits

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ultra-high speed: 2-3 ns

The ECL2500 Series is a compatible catalog family of ultra-high-speed (2-3 ns) ECL functions designed to fulfill the integrated-circuit requirements of next-generation computer systems. Twenty-eight device types perform both multifunction and complex logic, storage, and interface functions (up to 13 gates/package), all of which are offered in the economical industry-standard 16-pin plastic dual-in-line package.

summary of functions

	Gates/Pkg	Number of Types	Remarks
Logic			
Basic Gates and Multifunction Gates	1-6	18	Complementary Outputs High Fan-in High Fan-out Dotted Inputs/Outputs Multi-Output
Arithmetic and Decoder	5-12	3	Full Adder 3-Bit Decoder 5-Bit Group Carry
Interface			
Line Driver	2	1	Drives Two 50-Ω Lines
Line Receiver	2	1	High CMRR
High-Level-to-ECL Converter	2	1	Compatible with TTL, DTL, RTL
ECL-to-High-Level Converter	2	1	
Storage			
Multifunction Latch	4	1	Single-input gated
Complex Latch	9-13	2	2-input gated
Total Compatible Functions		28	

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absolute maximum ratings

Power Supply Voltage (V_{CC} to V_{EE})	6 V
Input Voltage (V_{in} @ V_{BB} = 0.0 V)	± 2 V
Output Source Current	40 mA d-c
Storage Temperature Range	−40°C to 150°C

recommended operating conditions

V_{CC} (Pin ③ and/or Pin ⑥)	1.32 V
V_{BB} (Pin ⑮)	OV (Gnd)
V_{EE} (Pin ⑩)	−3.2 V
Operating Temperature Range	0° to 75° C
System Impedance	50 Ω

4

electrical characteristics of basic ECL gate

Test Conditions: V_{CC} = 1.32 V, V_{BB} = 0,
V_{EE} = −3.2 V, T_A = 25°C

			Typical
Fan-out			1-10
Speed	Fan-out = 1	t_t (10% – 90% pts)	2.8 ns
		t_p (50% pts)*	2.3 ns
	Fan-out = 10	t_t *	4.3 ns
		t_p *	3.5 ns
Power Dissipation/Gate		Unterminated, P_{DU}	30 mW
		Terminated, P_{DT} **	60 mW
Logic Levels:			
	Logical "1"		400 mV
	Logical "0"		−400 mV
Noise Margin			200 mV

*See switching waveforms in figure 6.
**Complementary outputs driving 50 Ω to Gnd and 270 Ω to −3.2 V.

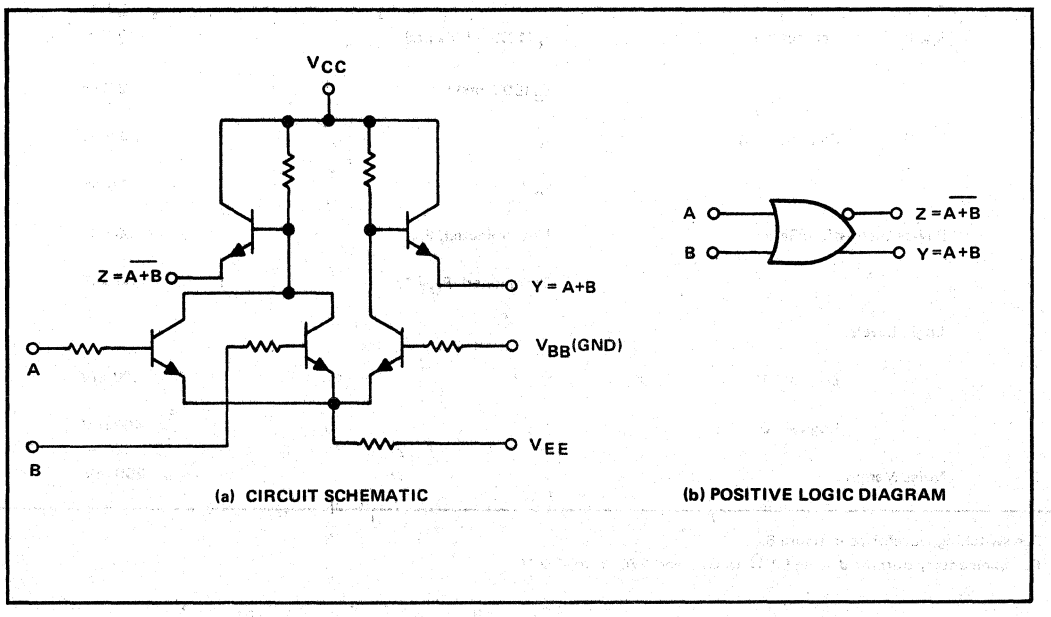
basic ECL gate

The basic ECL gate configuration is shown in figure 1. The high-speed performance results from the nonsaturating operation of the high-f_T transistor current switches. The high impedance of the load (input to differential amplifier) coupled with the low impedance of the driving source (emitter-follower output) allows high d-c fan-out. High-speed operation and high a-c fan-out are possible because all circuits are designed to operate in a 50-Ω system. When high-speed operation is a requirement, it is recommended that terminated 50-Ω transmission lines be utilized to interconnect circuits.

The basic ECL gate design of the ECL2500 Series provides both the output function Y and its complement Z; however, to maximize logic capability, some modules have only one output.

To minimize the number of packages to implement a system, and to reduce external connections, many units in the ECL2500 Series include logical connections between gates within the package. In-phase collector dotting (positive AND logic), out-of-phase emitter dotting (positive OR logic), and multiple inputs common to one package pin have been utilized to provide a very comprehensive logic family. An example of output dotting within the package is shown in figure 2. The positive logic WIRED-AND function is achieved by connecting in-phase collectors and the incorporation of an up-level clamp transistor. The positive logic WIRED-OR function within the package is accomplished by connecting out-of-phase-emitter-follower outputs. This inherent logic flexibility provides the system designer with a logic family with 1.6 times the logic/module density of conventional digital logic families.

figure 1. ECL gate



(a) CIRCUIT SCHEMATIC

(b) POSITIVE LOGIC DIAGRAM

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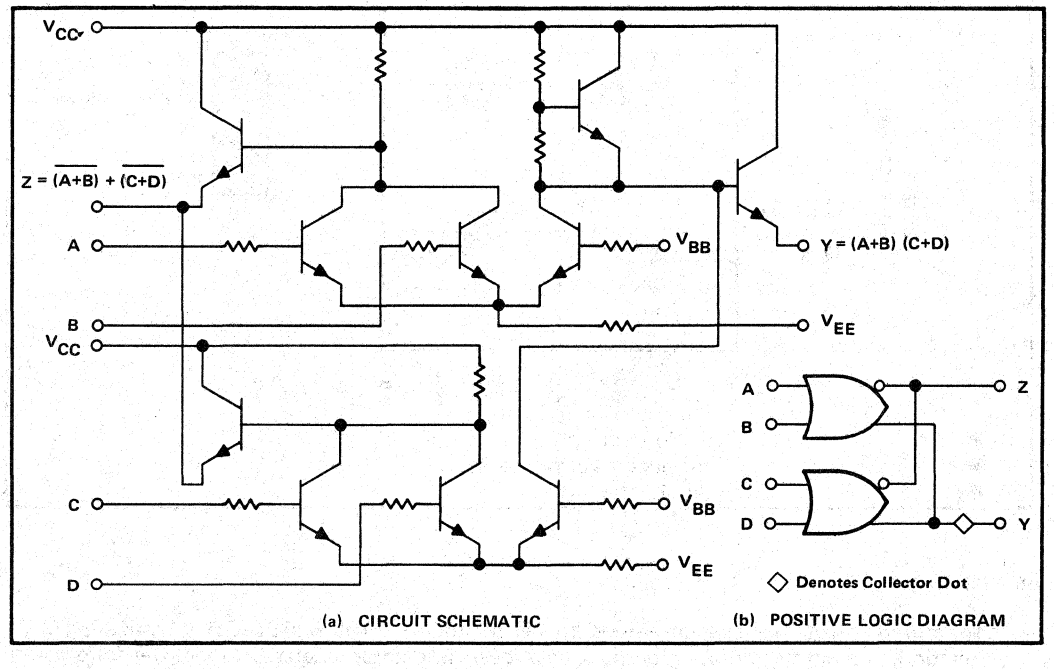
figure 2. ECL output dotting



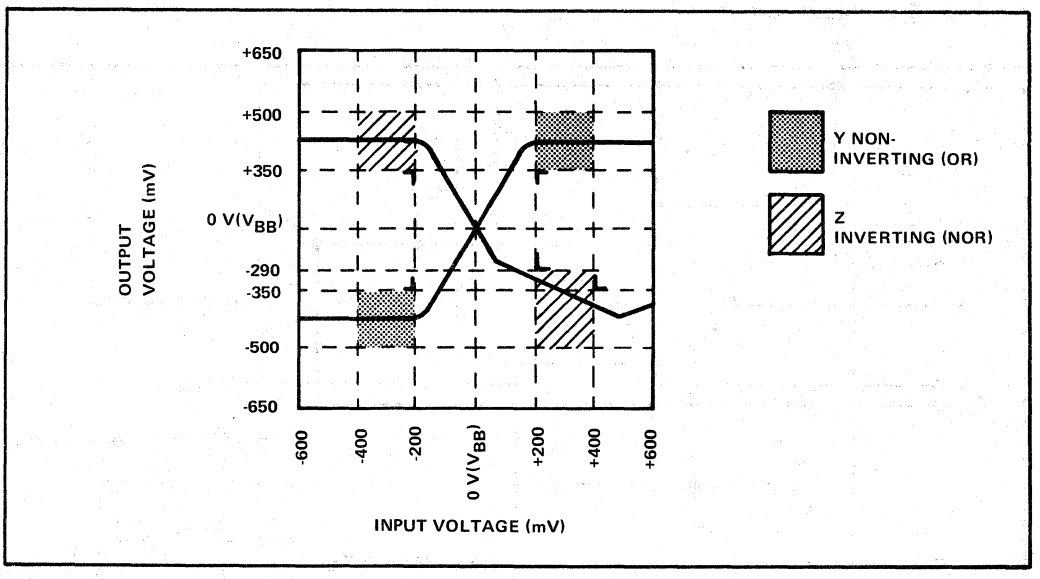
4

logic levels

Typical logic levels for the basic gate are 400 mV for a logical "1" and -400 mV for a logical "0" when operating with V_{CC}= 1.32 V, V_{EE}= −3.2 V, and V_{REF}= 0 V. Minimum levels when operating at 25° C free-air temperature and loaded with 50 Ω to ground and 270 Ω pulldown to −3.2 V are ± 350 mV. These logic levels are ensured with inputs at ±200 mV which provide 150 mV of d-c noise margin. Since the actual threshold is approximately 150 mV and typical output levels are 400 mV, typical d-c noise margin in excess of 200 mV can be expected. Transfer characteristics for the basic gate are shown in figure 3.

For gating functions which have emitter dots or parallel emitter followers, up levels will be increased by 50 mV to 450 mV. Likewise, down levels will increase by a similar amount to -350 mV.

figure 3. transfer characteristics-basic ECL gate



4

loading

To minimize package dissipation and to permit the external WIRED-OR (positive logic) function, the emitter-follower outputs have been left unterminated. The emitter-follower output is capable of driving a load of up to 25 mA d-c, but requires an externally provided negative voltage source and termination. The recommended termination includes a 270-Ω resistive load (pulldown) to V_{EE} (−3.2 V) and 50 Ω to V_{BB} (GND). To utilize the high-speed characteristics (≈ 2-ns switching speeds) of the ECL2500 Series, transmission lines or other controlled-impedance systems should be utilized to accomplish interconnections. The 50 Ω to ground provide proper termination when a 50-Ω transmission line is used.

When operating in a controlled-impedance interconnection system, two general classes of fan-out loading are permitted. The first (cluster loading) involves loads which can be connected within two inches from any source (output). The measurement is made between package pins. (Seating plane is used as a reference point.) These loads, called source stubs, are treated as lumped-capacitance loads which increase switching times but cause no reflection problems.

Since ECL circuit outputs may be directly wired together (emitter "dotted") to provide an OR (positive logic) function, cluster loading constraints apply to each of the sources making up the WIRED-OR. Up to ten such outputs may be "dotted" provided no two are more than two inches apart.

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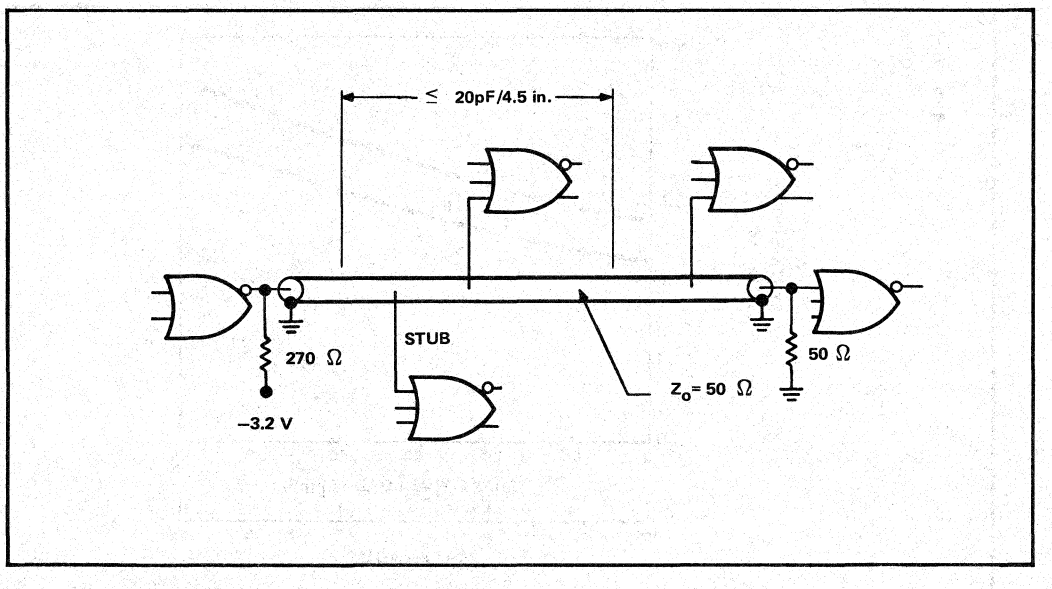
A second class of fan-out loading is commonly referred to as distributive loading. Such loads are greater than two inches from any source as measured between package pins (seating plane is used as reference point). These loads must be treated as lumped loads along a transmission line. The logic levels and switching speeds of the ECL2500 Series permit a maximum lumped load of 20 pF with less than a 20 per cent reflection coefficient for a 50-Ω printed-circuit line (e_r = 4.5). However, these loads must be 4.5 inches or more apart. Smaller lumped loads may be spaced closer together provided no more than 20 pF exists along any 4.5 inches of line measured outside the two-inch source stub.

Lumped loads may consist of circuit (gate) input capacitance and stub capacitance if used. Capacitances due to circuit inputs are ≈ 5.0 pF per input, while that attributed to stubs is dependent on the type of transmission line used. Figure 4 shows a typical distributive-loading arrangement.

Both cluster and distributive loads may be employed separately or in combination. Termination resistors for a load configuration involving only a cluster may be placed where convenient, but any other configuration requires termination at the end of the transmission line.

4

figure 4. typical distributive loading



unused inputs

To ensure high-speed operation all unused inputs should be tied to -1.0 ± 0.5 V.

power dissipation

Basic gate power drain with outputs unterminated is between 22 mW and 34 mW under the following conditions:

V_{CC} = 1.32 V
V_{EE} = -3.2 V
V_{BB} = 0 V

All inputs at 400 mV

When terminated into 50 Ω to ground and 270 Ω to −3.2 V, each emitter-follower output will dissipate an additional 22 mW in the up-level state and approximately 8 mW in the down-level state. Therefore, a basic gate with terminated complementary outputs will dissipate approximately 60 mW.

4

switching times

Switching-time performance at 25° C with various capacitive loadings is described in figure 5. This capacitive loading is directly relatable to a-c fan-out assuming 4-5 pF per gate input. Delay-time degradation with increasing fan-out approximates 75 ps per additional load. Switching-time waveform definitions and output terminations used for testing are shown in figure 6.

figure 5. switching time vs loading

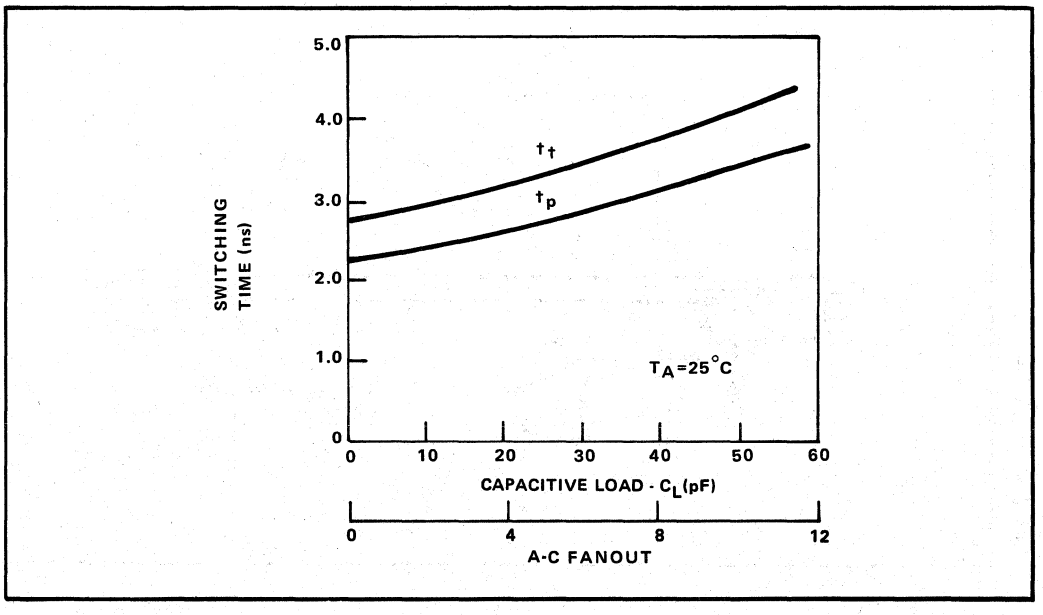


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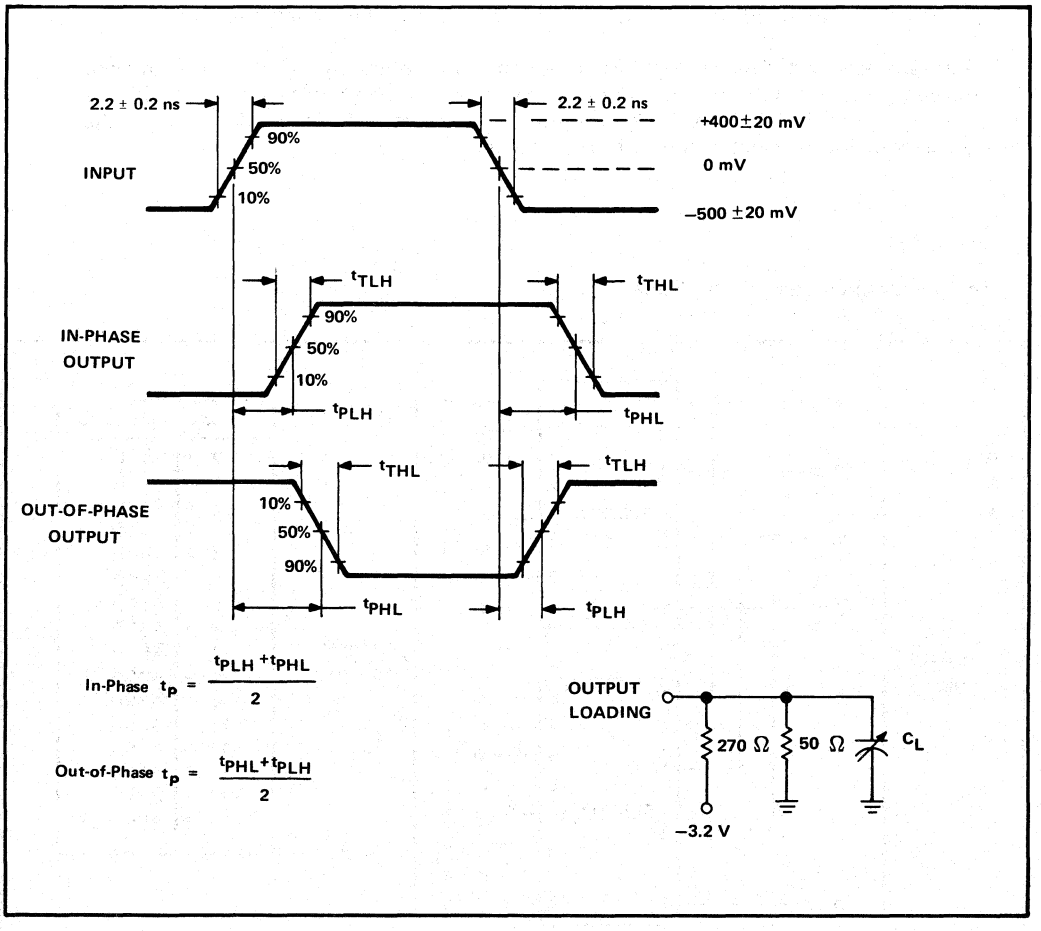
figure 6. switching time waveforms



arithmetic and decoder

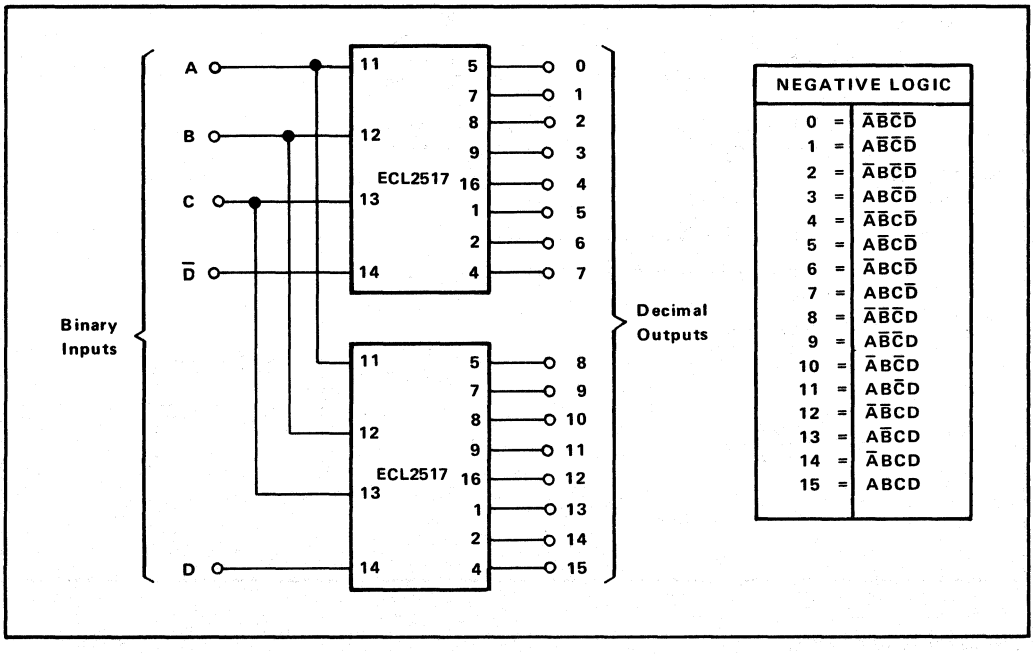
In addition to multifunction logic, more complex gating functions such as a 5-Bit Group Carry, Full Sum/Carry Adder, and 3-Bit Decoder have been included in the ECL2500 Series. Each of these modules will implement logic functions found in most large systems.

The 5-Bit Group Carry (ECL2515) is designed to provide the "look-ahead" carry feature required in high-speed adder applications. By utilizing this device and implementing the add function, significant reduction in addition delay time can be achieved as compared to ripple-through-carry addition.

The Full Sum-Carry Adder (ECL2516) produces the sum and carry outputs along with their complements for 1-bit additions. This addition can be accomplished in less than 3 ns.

The 3-Bit Decoder with Enable (ECL2517) generates a negative logical "1" on one of eight outputs dependent on the 3-bit binary input. The enable or 4th-bit input permits 4-bit binary decoding when two ECL2517 packages are utilized as shown in figure 7. Also shown is the binary decoding for the eight outputs of the ECL2517.

figure 7. 4-bit binary decode application



line driver

Each of the line drivers in the ECL2531 (2 per package) is designed to drive two 50-Ω transmission lines from both its in-phase and out-of-phase outputs. This permits fanning-out in two directions from each output.

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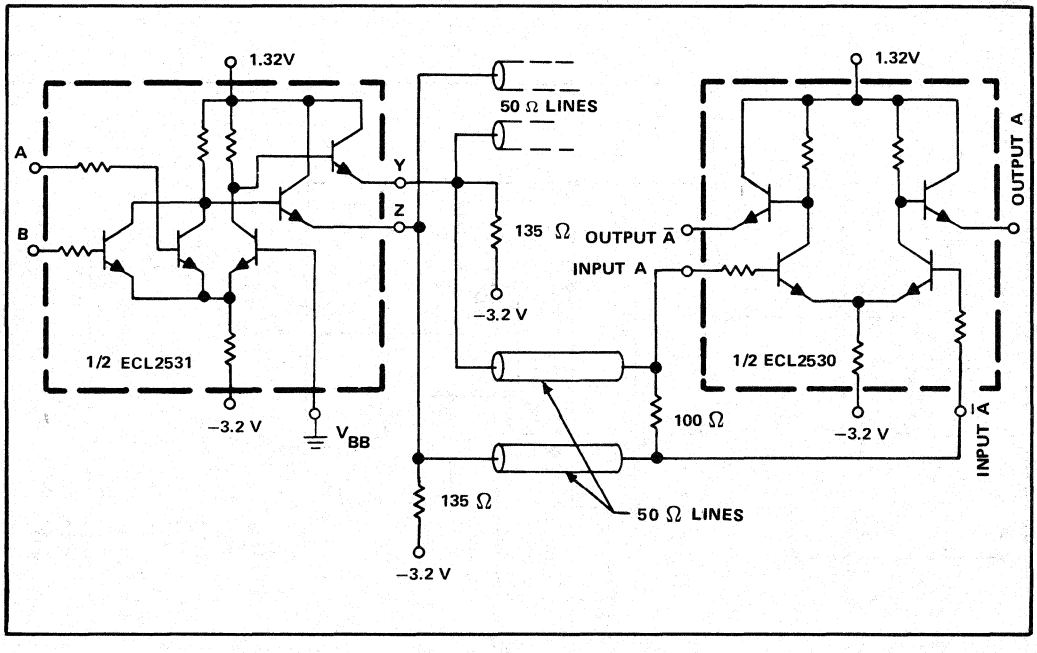
line receiver

The Dual Line Receiver (ECL2530) is designed to provide compatibility with the dual-line driver; however, it can be driven by any of the functions in the family. Its unique characteristics stem from optimization of the basic gate differential amplifier allowing input of a differential signal. Common-mode noise rejection of the Line Receiver permits transmission of logic signals over paths which are exposed to rather large noise transients and between areas in a machine which have devices operating at significantly different junction temperatures.

A typical connection arrangement is shown in figure 8.

figure 8. line driver/line receiver application



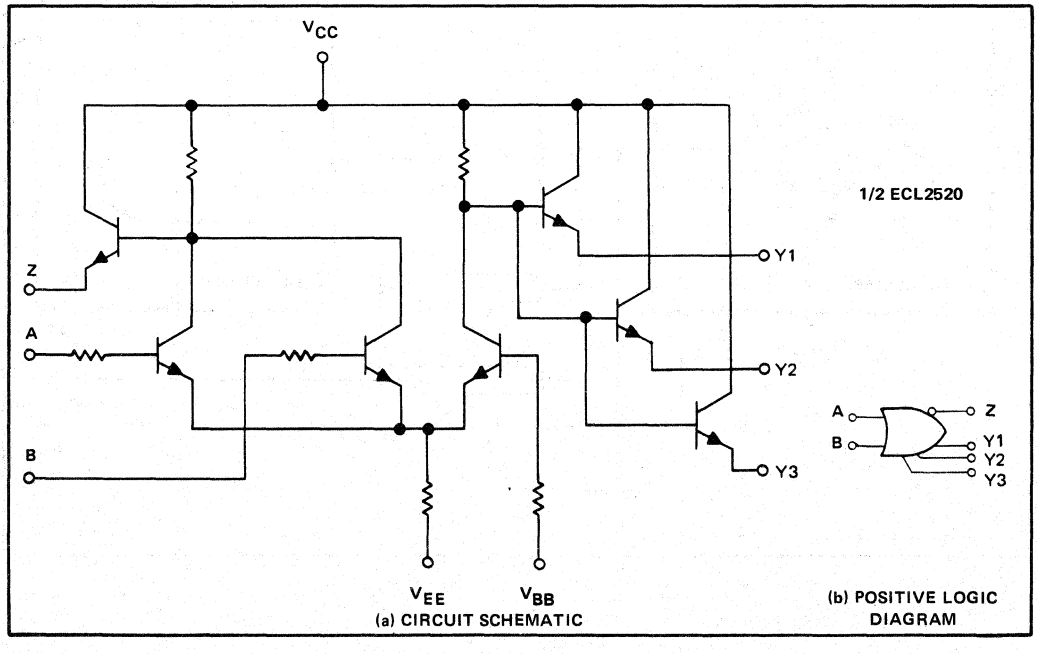
multi-output gates (drivers)

Additional fan-out or drive capability is provided in the ECL2500 Series through the use of gates with multiple emitter-follower outputs on either the in-phase or out-of-phase side of a basic gate. Additional logic flexibility can be obtained via external WIRED-OR connections of emitter-followers from these gates.

There are four dual-gate packages in the family which have gates with as many as four inputs or as many as four emitter-followers. Refer to the ECL2520 through ECL2523 for input/output combinations available.

The multiple emitter-follower circuit diagram and logic diagram is shown in figure 9.

figure 9. multi-output emitter-followers



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logic-level converters

Two Dual Logic-Level Converters are offered in the ECL2500 Series.

ECL2536	High-Level Logic to ECL
ECL2537	ECL to High-Level Logic (HLL)

The level converters are so designed that the High-Level-Logic inputs or outputs are compatible with standard saturated logic such as TTL, DTL and RTL.

The ECL2536 contains two HLL-to-ECL converters, each having an HLL input and an ECL input. The ECL input is most often used to inhibit the converter. Worst-case HLL-input levels must be $\geq$ 1.2 V and $\leq$ 0.5 V when operating with a V_{CC} of 5.0 V for the input stage.

The ECL2537 contains two ECL-to-HLL converters, each having two ECL inputs. When operating with a V_{CC} = 5.0 V and an external pulldown resistor, the output levels are:

Logical "1"	$\geq$ 3.4 V
Logical "0"	$\leq$ 0.4 V

The external pulldown resistor may be varied to satisfy the current-sinking requirement when driving TTL or DTL. Figure 10(b) shows a typical connection.

storage functions

Storage elements in the ECL2500 Series consist of three Dual "D" type flip-flops, commonly referred to as latches.

The ECL2540 is a dual latch which requires both a negative-going clock and its complement to store data presented at the data (D) input. Each latch has complementary outputs and dissipates the least amount of power ($\approx$ 60 mW) of the latches. Refer to the ECL2540 logic diagram for associated switching-time waveforms.

The ECL2541 and ECL2542 provide single-phase clock operation in addition to built-in gating features. Each latch in the ECL2541 has a single gated input, complementary outputs, plus multi-output emitter followers on one side of the latch. Multiple emitter-followers permit fan-out in two directions. Each latch in the ECL2542 has two gated inputs and a single output.

The ECL2541 and ECL2542 are defined for negative-logic inputs and upon application of a logical "1" (low level) clock the complement of the data presented at the $\overline{D}$ input will appear as output Q. Also, both devices have set and reset inputs which operate independent of the clock. The truth tables and switching waveforms applicable to these devices are shown on the data sheet.

figure 10 (a). TTL to ECL logic-level converter

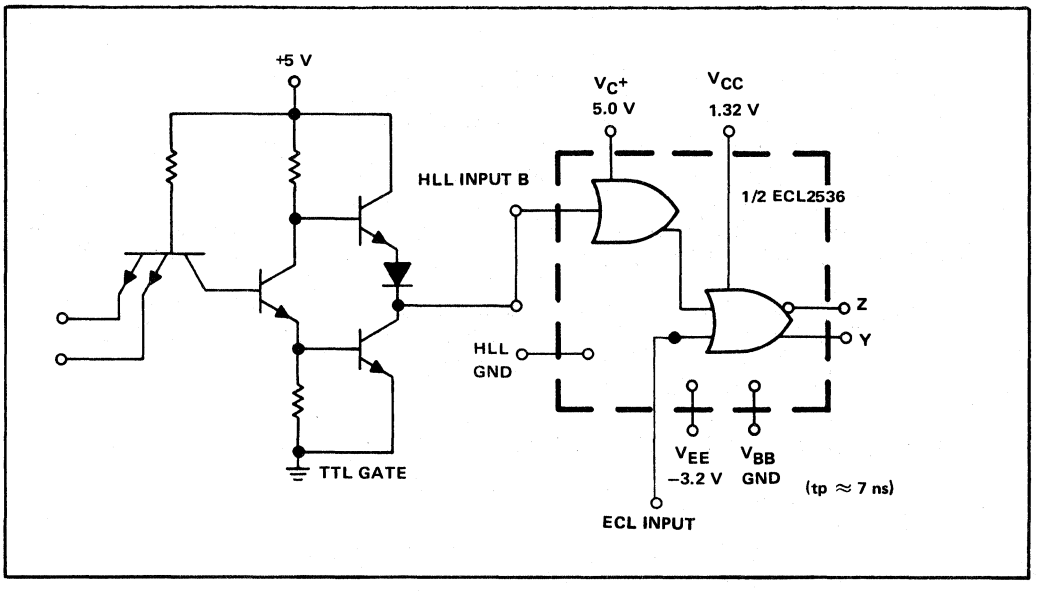
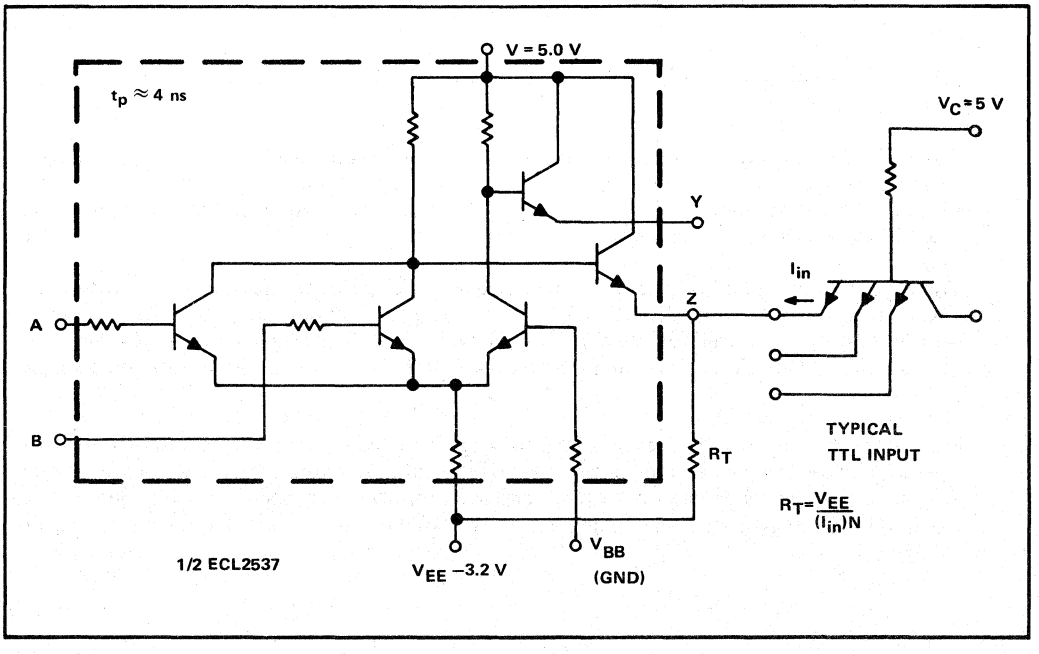


figure 10 (b). ECL to TTL logic-level converter



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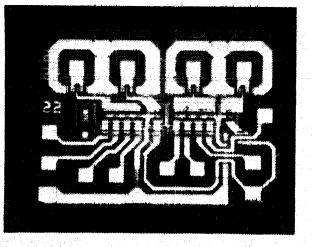
ECL2500 SERIES EMITTER-COUPLED-LOGIC (ECL) BASIC GATES FOR APPLICATION IN ULTRA-HIGH-SPEED DIGITAL SYSTEMS

description



The ECL2500 series is a compatible family of ECL functions with basic gate delays of 2 to 3 ns per stage. The family is specifically designed for operation from 0°C to 75°C.

The ECL2500 family includes:

- **Basic Gate Modules**
- Multifunction Gate Modules
- Bistable Modules
- Arithmetic Modules
- Interface Modules
- Memory Module

family features

- High speed. . .typical gate propagation delay time of 2.5 ns
- Complementary OR/NOR outputs with capability for wired-OR connections
- Designed for use with transmission lines to ensure maximum signal transmission without noise. Characterized for 50-ohm lines
- High noise immunity: ±225 mV typical at 25°C

This data sheet covers the basic gate modules. Separate data sheets cover the balance of the ECL2500 modules.

ECL2500 series basic gates

The seven ECL2500 series modules that form the basic gate group are shown in the table below. These modules contain various combinations of the basic ECL gate shown in the schematic of Figure A and the logic diagrams of Figure B.

SUMMARY OF MODULES IN BASIC GATE GROUP

MODULE	GATES PER MODULE	INPUTS PER GATE	POSITIVE LOGIC	OUTPUTS PER GATE	
				Y (OR)	Z (NOR)
ECL2500	2	4	OR/NOR	1	1
ECL2501	1	9	OR/NOR	1	1
ECL2502	3	2	OR/NOR	1	1
ECL2503	4	2	NOR		1
ECL2504	4	1	OR/NOR	1	1
ECL2505	3	3	NOR		1
ECL2511	4	2 (1 common to each gate)	OR	1	

schematic

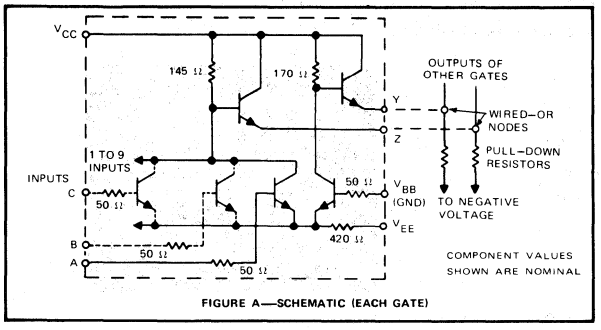


FIGURE A—SCHEMATIC (EACH GATE)

logic

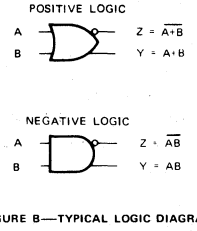


FIGURE B—TYPICAL LOGIC DIAGRAMS

Positive logic OR/NOR functions or negative logic AND/NAND functions are provided at the Y (OR) and Z (NOR) outputs, as shown.

Emitter-follower outputs require external pull-down resistors. The wired-OR function can be obtained by connecting emitter-follower outputs of separate gates together. Only one pull-down resistor is required for each wired-OR node.

4

absolute maximum ratings (see note 1)

Terminal voltages and currents . . . . . See table below
Storage temperature range . . . . . −40°C to 150°C
Temperature range with supply and bias voltages applied . . . . . −40°C to 100°C

TERMINAL VOLTAGE AND/OR CURRENT, T_A = 0°C TO 75°C (SEE NOTES 2 AND 3)

TERMINAL	REMARKS	VOLTAGE		CURRENT
		CONTINUOUS	20-μs SURGE	
V_{CC}		2 V	4.5 V	
V_{EE}		−4 V	−7 V	
Each Input	All other inputs open	−3.5 V	−4 V	
		2 V	2 V	
Output Y	All inputs high			−40 mA
Output Z	All inputs low			−40 mA

recommended operating conditions

Supply voltage V_{CC} . . . . . 1.32 V ± 2%
Supply voltage V_{EE} . . . . . −3.2 V ± 2%
Reference voltage V_{BB} . . . . . 0 V (GND)
Reverse bias on unused inputs . . . . . −1 V ± 0.5 V
Normalized d-c fan-out . . . . . 0 to 35
Load on each output . . . . . characterized at 270 Ω to V_{EE}, 50 Ω to GND
Operating free-air temperature range . . . . . 0°C to 75°C

NOTES: 1. Absolute maximum ratings are limits beyond which the life of individual devices may be impaired and are never to be exceeded in service or testing.
2. Maximum terminal conditions must be considered as mutually exclusive.
3. All voltages are referenced to V_{BB}, which is at GND.

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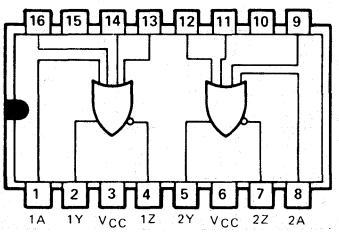
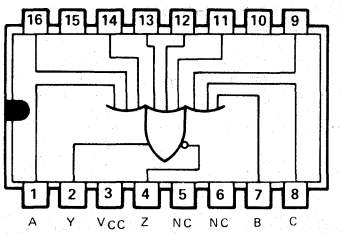
logic

ECL2500



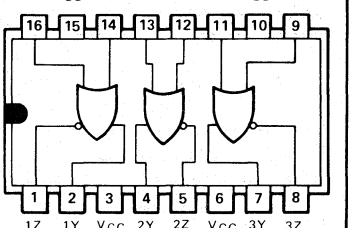
DUAL 4-INPUT OR/NOR GATE

ECL2501



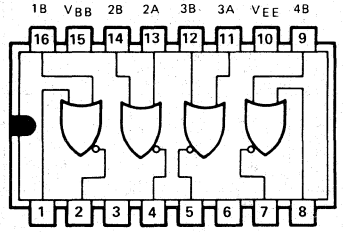
9-INPUT OR/NOR GATE

ECL2502



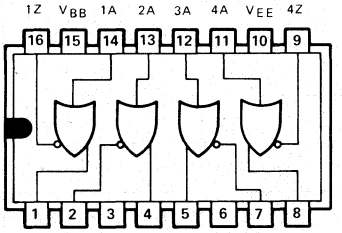
TRIPLE 2-INPUT OR/NOR GATE

ECL2503



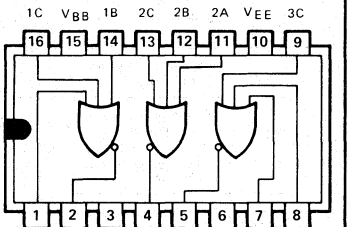
QUADRUPLE 2-INPUT NOR GATE

ECL2504



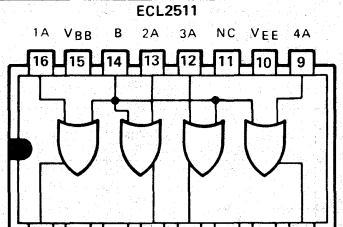
QUADRUPLE DELAY/INVERTER GATE

ECL2505



TRIPLE 3-INPUT NOR GATE

ECL2511



QUADRUPLE 2-INPUT OR GATE

MODULE	POSITIVE LOGIC		NEGATIVE LOGIC	
	Y(OR)	Z(NOR)	Y(AND)	Z(NAND)
ECL2500	A+B+C+D	$\overline{A+B+C+D}$	ABCD	$\overline{ABCD}$
ECL2501	A+B+C+D+E+F+G+H+I	$\overline{A+B+C+D+E+F+G+H+I}$	ABCDEFGHI	$\overline{ABCDEFGHI}$
ECL2502	A+B	$\overline{A+B}$	AB	$\overline{AB}$
ECL2503		$\overline{A+B}$		$\overline{AB}$
ECL2504	A	$\overline{A}$	A	$\overline{A}$
ECL2505		$\overline{A+B+C}$		$\overline{ABC}$
ECL2511	1A+B, 2A+B, 3A+B, 4A+B		1A•B, 2A•B, 3A•B, 4A•B	

NC—No internal connection

truth tables (for this series, H = positive voltage, L = negative voltage, X = irrelevant)

ECL2500

A	B	C	D	Y	Z
L	L	L	L	L	H
H	X	X	X	H	L
X	H	X	X	H	L
X	X	H	X	H	L
X	X	X	H	H	L
H	H	H	H	H	L

ECL2501

A	B	C	D	E	F	G	H	I	Y	Z
L	L	L	L	L	L	L	L	L	L	H
H	X	X	X	X	X	X	X	X	H	L
X	H	X	X	X	X	X	X	X	H	L
X	X	H	X	X	X	X	X	X	H	L
X	X	X	H	X	X	X	X	X	H	L
X	X	X	X	H	X	X	X	X	H	L
X	X	X	X	X	H	X	X	X	H	L
X	X	X	X	X	X	H	X	X	H	L
X	X	X	X	X	X	X	H	X	H	L
X	X	X	X	X	X	X	X	H	H	L
H	H	H	H	H	H	H	H	H	H	L

ECL2502

A	B	Y	Z
L	L	L	H
H	X	H	L
X	H	H	L
H	H	H	L

ECL2503

A	B	Z
L	L	H
H	X	L
X	H	L
H	H	L

ECL2504

A	Y	Z
L	L	H
H	H	L

ECL2505

A	B	C	Z
L	L	L	H
H	X	X	L
X	H	X	L
X	X	H	L
H	H	H	L

ECL2511

A	B	Y
L	L	L
H	X	H
X	H	H
H	H	H

electrical characteristics at specified free-air temperature

PARAMETER		TEST FIGURE	TEST CONDITIONS*		MODULE							SEE NOTE 4			UNIT
					ECL2500	ECL2501	ECL2502	ECL2503	ECL2504	ECL2505	ECL2511	MIN	TYP	MAX	
V_{IH}	High-level input voltage			0°C 25°C 75°C	• • •	• • •	• • •	• • •	• • •	• • •	• • •	150 150 150		720 720 720	mV
V_{IL}	Low-level input voltage			0°C 25°C 75°C	• • •	• • •	• • •	• • •	• • •	• • •	• • •	−1500 −1500 −1500		−150 −150 −150	mV
$V_{OH(Y)}$	High-level output voltage at OR output	2	V_I = 0.2 V	0°C 25°C 75°C	• • •	• • •	• • •		• • •		• • •	315 350	390 425 495	500 580	mV
$V_{OL(Y)}$	Low-level output voltage at OR output	2	V_I = −0.2 V	0°C 25°C 75°C	• • •	• • •	• • •		• • •		• • •	−505 −490	−445 −425 −385	−350 −310	mV
$V_{OH(Z)}$	High-level output voltage at NOR output	2	V_I = −0.2 V	0°C 25°C 75°C	• • •	• • •	• • •	• • •	• • •	• • •		315 350	390 425 495	500 580	mV
$V_{OL(Z)}$	Low-level output voltage at NOR output	2	V_I = 0.2 V	0°C 25°C 75°C	• • •	• • •	• • •	• • •	• • •	• • •		−420	−385 −365 −325	−310 −280	mV
$V_{OL(Z)}$	Low-level output voltage at NOR output	2	V_I = 0.4 V	0°C 25°C 75°C	• • •	• • •	• • •	• • •	• • •	• • •		−505 −490	−455 −425 −380	−315	mV
$V_{OH(Y)}$	High-level output voltage at OR output	2	V_I = 0.15 V	0°C 25°C 75°C	• • •	• • •	• • •		• • •		• • •	290 325			mV
$V_{OL(Y)}$	Low-level output voltage at OR output	2	V_I = −0.15 V	0°C 25°C 75°C	• • •	• • •	• • •		• • •		• • •			−325 −290	mV
$V_{OH(Z)}$	High-level output voltage at NOR output	2	V_I = −0.15 V	0°C 25°C 75°C				• • •		• • •		290 325			mV
$V_{OL(Z)}$	Low-level output voltage at NOR output	2	V_I = 0.15 V	0°C 25°C 75°C				• • •		• • •				−290 −260	mV
I_{IH}	High-level input current (each input)	3	V_I = 0.5 V	0°C 25°C 75°C	• • •	• • •	• • •	• • •	• • •	• • •	• • •			255 235 200	μA
I_{IL}	Low-level input current	4	V_I = −3.2 V	0°C 25°C 75°C	• • •	• • •	• • •	• • •	• • •	• • •	• • •			−0.5† −0.6† −0.9†	μA
I_{CC} or $-I_{EE}$	Supply current	5	V_I = −0.5 V	25°C	• •	 • 	 • 	 • 	 • 	 • 	 •	8 4 13 18 18 13 18		15 8 21 28 28 21 28	mA
C_{in}	Input capacitance (each input)		See Note 5	25°C	•	•	•	•	•	•	•		5		pF
z_{out}	Output impedance		See Note 6	25°C	•	•	•	•	•	•	•		5		Ω

* V_{BB} = GND, V_{CC} = 1.32 V ±1%, V_{EE} = −3.20 V ±1%.

† These are worst-case values for nine inputs in parallel. See Supplementary Parameter Measurement Information for each gate.

NOTES: 4. The algebraic convention where the most positive limit is designated as maximum is used in this data sheet for logic voltage levels only, e.g., if −350 mV is a maximum, the typical and minimum limits are more negative voltages.

5. C_{in} is measured using peak-current techniques. A square-wave input pulse is applied, and the input current waveform is integrated with respect to time to determine Q. C_{in} = Q/V.

6. Constant-current loads are used to determine the output impedance which is derived from the slope of a V_O vs I_O curve.

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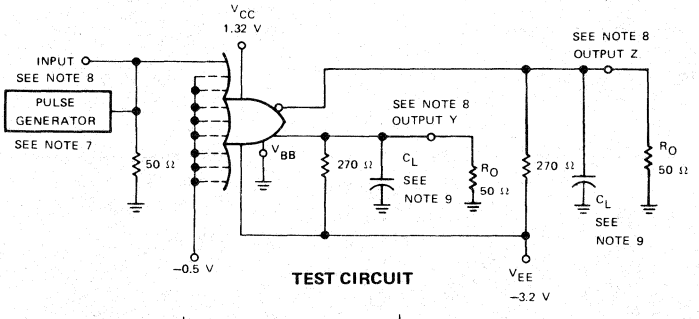
typical operating characteristics at specified free-air temperature (see figure 1)

PARAMETER		C_L	T_A	ECL2500 ECL2502 ECL2504	ECL2501		ECL2503 ECL2505	ECL2511		UNIT
				ANY OUTPUT	Y OUTPUT	Z OUTPUT	ANY OUTPUT	A INPUTS	B INPUT	
				TYP†	TYP†	TYP†	TYP†	TYP†	TYP†	
t_{PHL}	Propagation delay time, high-to-low-level output	4 pF	0°C	2.4	2.4	2.6	2.6	2.4	2.7	ns
			25°C	2.3	2.3	2.4	2.5	2.5	2.8	
	and/or		75°C	2.4	2.4	2.6	2.6	2.4	2.7	
t_{PLH}	Propagation delay time, low-to-high-level output	50 pF	0°C	3.5	3.5	3.8	3.8	3.4	3.4	ns
			25°C	3.3	3.3	3.5	3.5	3.6	3.7	
			75°C	3.5	3.5	3.8	3.8	3.4	3.4	
t_{THL}	Transition time, high-to-low-level output	4 pF	0°C	3.3	3.3	5.1	4.3	4.0	4.2	ns
			25°C	3.0	3.0	4.8	4.0	3.8	4.0	
	and/or		75°C	3.3	3.3	5.1	4.3	4.0	4.2	
t_{TLH}	Transition time, low-to-high-level output	50 pF	0°C	4.2	4.2	4.7	4.4	4.5	4.7	ns
			25°C	3.9	3.9	4.4	4.1	4.3	4.5	
			75°C	4.2	4.2	4.7	4.4	4.5	4.7	

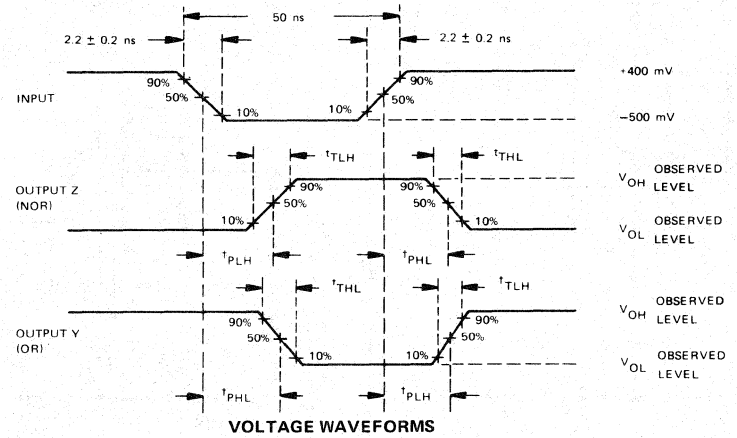
†See Supplementary Parameter Measurement Information for MIN and MAX values at T_A = 25°C.

4

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

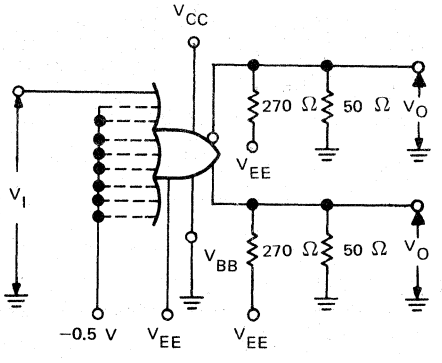
FIGURE 1—PROPAGATION DELAY AND TRANSITION TIMES

NOTES: 7. The generator has the following characteristics: Z_{out} = 50 Ω, PRR = 1 MHz.

8. The waveforms are monitored on an oscilloscope with a rise time of less than or equal to 350 ps. Either a high-impedance probe with an input impedance of 100 kΩ paralleled by 2 pF, or a 50-Ω impedance system can be used. The 50-Ω resistors designated R_O are the oscilloscope input resistance in the 50-Ω system or discrete resistors with a high-impedance probe.

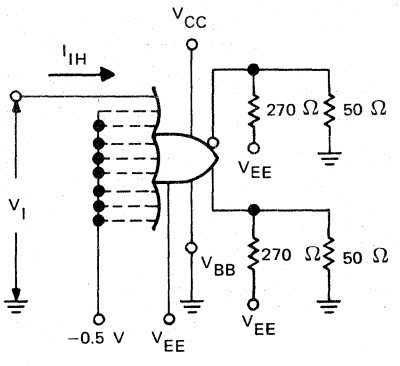
9. C_L includes probe and fixture capacitance. A capacitance of 50 pF can be used to approximate an a-c fan-out of 10.

PARAMETER MEASUREMENT INFORMATION†



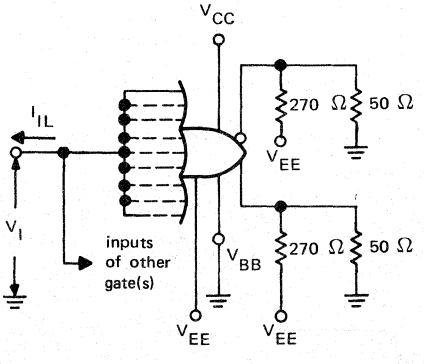
A. V_I is applied to each input separately.
B. Each output is tested separately.

FIGURE 2—V_{OH} AND V_{OL}



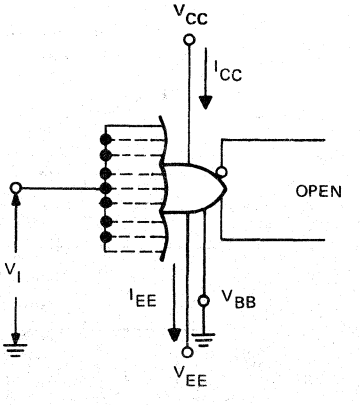
Each input is tested separately.

FIGURE 3—I_{IH}



All inputs of all gates are connected in parallel.

FIGURE 4—I_{IL}



A. All gates are tested simultaneously.
B. I_{CC} is the total current into all V_{CC} terminals.

FIGURE 5–I_{CC} OR I_{EE}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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SUPPLEMENTARY PARAMETER MEASUREMENT INFORMATION

electrical characteristics at specified free-air temperature

PARAMETER (SEE NOTE 10)	TERMINALS TO BE TESTED (SEE NOTE 11)		TEST FIGURE	INPUT CONDITIONS			T_A	MIN	TYP	MAX	UNIT
	INPUTS	OUTPUTS Y	OUTPUTS Z	INPUT UNDER TEST	OTHER INPUT(S) OF SAME GATE	INPUTS OF OTHER GATE(S)					
ECL2500	V_{BB} (pin 15) = GND, V_{CC} (pin 3 and pin 6) = 1.32 V, V_{EE} (pin 10) = −3.2 V										
$V_{OH(Y)}$	1,13,14,16	2		2	0.2 V	−0.5 V	−0.5 V	0°C	315	390		mV
								25°C	350	425	500	
	8,9,11,12	5						75°C		495	580	
$V_{OL(Y)}$	1,13,14,16	2		2	−0.2 V	−0.5 V	−0.5 V	0°C	−505	−445		mV
								25°C	−490	−425	−350	
	8,9,11,12	5						75°C		−385	−310	
$V_{OH(Z)}$	1,13,14,16		4	2	−0.2 V	−0.5 V	−0.5 V	0°C	315	390		mV
								25°C	350	425	500	
	8,9,11,12		7					75°C		495	580	
$V_{OL(Z)}$	1,13,14,16		4	2	0.2 V	−0.5 V	−0.5 V	0°C		−385		mV
								25°C	−420	−365	−310	
	8,9,11,12		7					75°C		−325	−280	
$V_{OL(Z)}$	1, 13, 14, 16		4	2	0.4 V	−0.5 V	−0.5 V	0°C	−505	−455		mV
								25°C	−490	−425		
	8, 9, 11, 12		7					75°C		−380	−315	
$V_{OH(Y)}$	12	5		2	0.15 V	−0.5 V	−0.5 V	0°C	290			mV
								25°C	325			
								75°C				
$V_{OL(Y)}$	12	5		2	−0.15 V	−0.5 V	−0.5 V	0°C				mV
								25°C			−325	
								75°C			−290	
I_{IH}	1,13,14,16			3	0.5 V	−0.5 V	−0.5 V	0°C			255	μA
								25°C			235	
	8,9,11,12							75°C			200	
I_{IL}	1,13,14,16			4	All inputs of both gates in parallel at −3.2 V			0°C			−0.5	μA
								25°C			−0.5	
	8,9,11,12							75°C			−0.8	
ECL2501	V_{BB} (pin 15) = GND, V_{CC} (pin 3) = 1.32 V, V_{EE} (pin 10) = −3.2 V										
$V_{OH(Y)}$	1,7,8,9,11, 12,13,14,16	2		2	0.2 V	−0.5 V		0°C	315	390		mV
								25°C	350	425	500	
								75°C		495	580	
$V_{OL(Y)}$	1,7,8,9,11, 12,13,14,16	2		2	−0.2 V	−0.5 V		0°C	−505	−455		mV
								25°C	−490	−425	−350	
								75°C		−385	−310	
$V_{OH(Z)}$	1,7,8,9,11, 12,13,14,16		4	2	−0.2 V	−0.5 V		0°C	315	390		mV
								25°C	350	425	500	
								75°C		495	580	
$V_{OL(Z)}$	1,7,8,9,11, 12,13,14,16		4	2	0.2 V	−0.5 V		0°C		−385		mV
								25°C	−420	−365	−310	
								75°C		−325	−280	
$V_{OL(Z)}$	1,7,8,9,11, 12,13,14,16		4	2	0.4 V	−0.5 V		0°C	−505	−455		mV
								25°C	−490	−425		
								75°C		−380	−315	
$V_{OH(Y)}$	1	2		2	0.15 V	−0.5 V		0°C	290			mV
								25°C	325			
								75°C				
$V_{OL(Y)}$	1	2		2	−0.15 V	−0.5 V		0°C				mV
								25°C			−325	
								75°C			−290	
I_{IH}	1,7,8,9,11, 12,13,14,16			3	0.5 V	−0.5 V		0°C			255	μA
								25°C			235	
								75°C			200	
I_{IL}	1,7,8,9,11, 12,13,14,16			4	All inputs in parallel at −3.2 V			0°C			−0.5	μA
								25°C			−0.6	
								75°C			−0.9	

NOTES: 10. See page 4 for defining term associated with each symbol.
11. Each gate is tested separately unless otherwise noted. See referenced test figure for output termination. Gates not under test have their outputs terminated in the same manner, and power applied.

SUPPLEMENTARY PARAMETER MEASUREMENT INFORMATION

electrical characteristics at specified free-air temperature

PARAMETER (SEE NOTE 10)	TERMINALS TO BE TESTED (SEE NOTE 11)		TEST FIGURE	INPUT CONDITIONS			T_A	MIN	TYP	MAX	UNIT
	INPUTS	OUTPUTS Y Z		INPUT UNDER TEST	OTHER INPUT(S) OF SAME GATE	INPUTS OF OTHER GATES					
ECL2502	V_{BB} (pin 15) = GND, V_{CC} (pin 3 and pin 6) = 1.32 V, V_{EE} (pin 10) = −3.2 V										
$V_{OH(Y)}$	14,16	2	2	0.2 V	−0.5 V	−0.5 V	0°C	315	390		mV
	12,13	4					25°C	350	425	500	
	9,11	7					75°C		495	580	
$V_{OL(Y)}$	14,16	2	2	−0.2 V	−0.5 V	−0.5 V	0°C	−505	−445		mV
	12,13	4					25°C	−490	−425	−350	
	9,11	7					75°C		−385	−310	
$V_{OH(Z)}$	14,16	1	2	−0.2 V	−0.5 V	−0.5 V	0°C	315	390		mV
	12,13	5					25°C	350	425	500	
	9,11	8					75°C		495	580	
$V_{OL(Z)}$	14,16	1	2	0.2 V	−0.5 V	−0.5 V	0°C		−385		mV
	12,13	5					25°C	−420	−365	−310	
	9,11	8					75°C		−325	−280	
$V_{OL(Z)}$	14,16	1	2	0.4 V	−0.5 V	−0.5 V	0°C	−505	−455		mV
	12,13	5					25°C	−490	−425		
	9,11	8					75°C		−380	−315	
$V_{OH(Y)}$	11	7	2	0.15 V	−0.5 V	−0.5 V	0°C	290			mV
							25°C	325			
							75°C				
$V_{OL(Y)}$	11	7	2	−0.15 V	−0.5 V	−0.5 V	0°C				mV
							25°C			−325	
							75°C			−290	
I_{IH}	14,16		3	0.5 V	−0.5 V	−0.5 V	0°C			255	μA
	12,13						25°C			235	
	9,11						75°C			200	
I_{IL}	14,16		4	All inputs of all gates in parallel at −3.2 V			0°C			−0.5	μA
	12,13						25°C			−0.5	
	9,11						75°C			−0.6	
ECL2503	V_{BB} (pin 15) = GND, V_{CC} (pin 3 and pin 6) = 1.32 V, V_{EE} (pin 10) = −3.2 V										
$V_{OH(Z)}$	1,16	2	2	−0.2 V	−0.5 V	−0.5 V	0°C	315	390		mV
	13,14	4					25°C	350	425	500	
	11,12	5					75°C		495	580	
	8,9	7									
$V_{OL(Z)}$	1,16	2	2	0.2 V	−0.5 V	−0.5 V	0°C		−385		mV
	13,14	4					25°C	−420	−365	−310	
	11,12	5					75°C		−325	−280	
	8,9	7									
$V_{OL(Z)}$	1,16	2	2	0.4 V	−0.5 V	−0.5 V	0°C	−505	−455		mV
	13,14	4					25°C	−490	−425		
	11,12	5					75°C		−380	−315	
	8,9	7									
$V_{OH(Z)}$	9	7	2	−0.15 V	−0.5 V	−0.5 V	0°C	290			mV
							25°C	325			
							75°C				
$V_{OL(Z)}$	9	7	2	0.15 V	−0.5 V	−0.5 V	0°C				mV
							25°C			−290	
							75°C			−260	
I_{IH}	1,16		3	0.5 V	−0.5 V	−0.5 V	0°C			255	μA
	13,14						25°C			235	
	11,12						75°C			200	
	8,9										
I_{IL}	1,16		4	All inputs of all gates in parallel at −3.2 V			0°C			−0.5	μA
	13,14						25°C			−0.5	
	11,12						75°C			−0.8	
	8,9										

NOTES: 10. See page 4 for defining term associated with each symbol.

11. Each gate is tested separately unless otherwise noted. See referenced test figure for output termination. Gates not under test have their outputs terminated in the same manner, and power applied.

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SUPPLEMENTARY PARAMETER MEASUREMENT INFORMATION

electrical characteristics at specified free-air temperature

PARAMETER (SEE NOTE 10)	TERMINALS TO BE TESTED (SEE NOTE 11)		TEST FIGURE	INPUT CONDITIONS			T_A	MIN	TYP	MAX	UNIT
	INPUTS	OUTPUTS Y Z		INPUT UNDER TEST	OTHER INPUT(S) OF SAME GATE	INPUTS OF OTHER GATES					
ECL2504	V_{BB} (pin 15) = GND, V_{CC} (pin 3 and pin 6) = 1.32 V, V_{EE} (pin 10) = −3.2 V										
$V_{OH(Y)}$	14	1	2	0.2 V		−0.5 V	0°C 25°C 75°C	315 350	390 425 495	500 580	mV
	13	4									
	12	5									
	11	8									
$V_{OL(Y)}$	14	1	2	−0.2 V		−0.5 V	0°C 25°C 75°C	−505 −490	−445 −425 −385	−350 −310	mV
	13	4									
	12	5									
	11	8									
$V_{OH(Z)}$	14	16	2	−0.2 V		−0.5 V	0°C 25°C 75°C	315 350	390 425 495	500 580	mV
	13	2									
	12	7									
	11	9									
$V_{OL(Z)}$	14	16	2	0.2 V		−0.5 V	0°C 25°C 75°C	−420	−385 −365 −325	−310 −280	mV
	13	2									
	12	7									
	11	9									
$V_{OL(Z)}$	14	16	2	0.4 V		−0.5 V	0°C 25°C 75°C	−505 −490	−455 −425 −380	−315	mV
	13	2									
	12	7									
	11	9									
$V_{OH(Y)}$	13	4	2	0.15 V		−0.5 V	0°C 25°C 75°C	290 325			mV
$V_{OL(Y)}$	13	4	2	−0.15 V		−0.5 V	0°C 25°C 75°C			325 290	mV
I_{IH}	14		3	0.5 V		−0.5 V	0°C 25°C 75°C			255 235 200	μA
	13										
	12										
	11										
I_{IL}	14		4	Inputs of all gates in parallel at −3.2 V			0°C 25°C 75°C			−0.5 −0.5 −0.5	μA
	13										
	12										
	11										
ECL2505	V_{BB} (pin 15) = GND, V_{CC} (pin 3 and pin 6) = 1.32 V, V_{EE} (pin 10) = −3.2 V										
$V_{OH(Z)}$	1,14,16	2	2	−0.2 V	−0.5 V	−0.5 V	0°C 25°C 75°C	315 350	390 425 495	500 580	mV
	11,12,13	4									
	7,8,9	5									
$V_{OL(Z)}$	1,14,16	2	2	0.2 V	−0.5 V	−0.5 V	0°C 25°C 75°C	−420	−385 −365 −325	−310 −280	mV
	11,12,13	4									
	7,8,9	5									
$V_{OL(Z)}$	1,14,16	2	2	0.4 V	−0.5 V	−0.5 V	0°C 25°C 75°C	−505 −490	−455 −425 −380	−315	mV
	11,12,13	4									
	7,8,9	5									
$V_{OH(Z)}$	9	5	2	−0.15 V	−0.5 V	−0.5 V	0°C 25°C 75°C	290 325			mV
$V_{OL(Z)}$	9	5	2	0.15 V	−0.5 V	−0.5 V	0°C 25°C 75°C			−290 −260	mV
I_{IH}	1,14,16		3	0.5 V	−0.5 V	−0.5 V	0°C 25°C 75°C			255 235 200	μA
	11,12,13										
	7,8,9										
I_{IL}	1,14,16		4	All inputs of all gates in parallel at −3.2 V			0°C 25°C 75°C			−0.5 −0.6 −0.9	μA
	11,12,13										
	7,8,9										

NOTES: 10. See page 4 for defining term associated with each symbol.

11. Each gate is tested separately unless otherwise noted. See referenced test figure for output termination. Gates not under test have their outputs terminated in the same manner, and power applied.

SUPPLEMENTARY PARAMETER MEASUREMENT INFORMATION

electrical characteristics at specified free-air temperature

PARAMETER (SEE NOTE 10)	TERMINALS TO BE TESTED (SEE NOTE 11)		TEST FIGURE	INPUT CONDITIONS			T_A	MIN	TYP	MAX	UNIT
	INPUTS	OUTPUTS Y Z		INPUT UNDER TEST	OTHER INPUT(S) OF SAME GATE	INPUTS OF OTHER GATES					
ECL2511	V_{BB} (pin 15) = GND, V_{CC} (pin 2, pin 3, pin 6, and pin 7) = 1.32 V, V_{EE} (pin 10) = −3.2 V										
$V_{OH(Y)}$	16,14	1	2	0.2 V	−0.5 V	−0.5 V	0°C 25°C 75°C	315 350	390 425 495	500 580	mV
	13,14	4									
	12,14	5									
	9,14	8									
$V_{OL(Y)}$	16,14	1	2	−0.2 V	−0.5 V	−0.5 V	0°C 25°C 75°C	−505 −490	−445 −425 −385	−350 −310	mV
	13,14	4									
	12,14	5									
	9,14	8									
$V_{OH(Y)}$	16	1	2	0.15 V	−0.5 V	−0.5 V	0°C 25°C 75°C	290 325			mV
$V_{OL(Y)}$	16	1	2	−0.15 V	−0.5 V	−0.5 V	0°C 25°C 75°C			−325 −290	mV
I_{IH}	16		3	0.5 V	−0.5 V	−0.5 V	0°C 25°C 75°C			255 235 200	mV
	13										
	12										
	9										
	14		3	0.5 V	−0.5 V		0°C 25°C 75°C			1020 940 800	μA
I_{IL}	16		4	All inputs of all gates in parallel at −3.2 V			0°C 25°C 75°C			−0.5 −0.5 −0.8	μA
	13										
	12										
	9										
	14										

NOTES: 10. See page 4 for defining term associated with each symbol.

11. Each gate is tested separately unless otherwise noted. See referenced test figure for output termination. Gates not under test have their outputs terminated in the same manner, and power applied.

GENERAL APPLICATION INFORMATION

Multiple V_{CC} terminals have been supplied to reduce crosstalk noise. All V_{CC} terminals should be connected even if all gates in a module are not used.

Applications of the ECL2500 basic gates at other than data sheet conditions are covered in a separate family application document.

General loading for fan-out may be divided into two classes:

CLASS I — **Short-Line or Cluster Loading.**
Loads which can be connected within two inches of any source can be treated as lumped capacitive loads which include the gate inputs and stub-line capacitances. Switching times can be interpolated accordingly. No two dotted outputs can be more than two inches apart for this case.

CLASS II — **Long-Line or Distributive Loading.**
These loads must be treated as lumped loads along a transmission line and termination should be at the end of the transmission chain. No more than 20 pF of load is recommended per 4.5 inches of 50-ohm printed line (with dielectric constant of 4.5) in order that the reflection coefficient be no greater than 20%. If the loads are lumped loads of 20 pF, they must be 4.5 inches apart. If individual gates and CLASS I loads are distributed, they must not exceed the 20 pF per 4.5 inches of line.

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SUPPLEMENTARY PARAMETER MEASUREMENT INFORMATION

operating characteristics at specified free-air temperature (see figure 1)

TERMINALS TO BE TESTED (SEE NOTES 12, 13, AND 14)				C_L	t_{PHL} and/or t_{PLH} PROPAGATION TIMES—ns						t_{THL} and/or t_{TLH} TRANSITION TIMES—ns					
					$T_A = 0°C$			$T_A = 25°C$			$T_A = 75°C$			$T_A = 0°C$			$T_A = 25°C$			$T_A = 75°C$		
INPUT	OUTPUT	INPUT	OUTPUT	INPUT	OUTPUT	INPUT	OUTPUT	pF	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
ECL2500																										
1, 13, 14, 16	2, 4	8, 9, 11, 12	5, 7				4		2.4			1.5	2.3	3.3		2.4			3.3			1.7	3.0	4.7		3.3	
							50		3.5			2.4	3.3	4.4		3.5			4.2			2.5	3.9	6.5		4.2	
ECL2501																										
1,7,8, 9,11, 12,13, 14,16	2						4		2.4			1.5	2.3	3.3		2.4			3.3			1.7	3.0	4.7		3.3	
							50		3.5			2.4	3.3	4.4		3.5			4.2			2.5	3.9	6.5		4.2	
1,7,8, 9,11, 12,13, 14,16	4						4		2.6			1.6	2.4	3.4		2.6			5.1			2.8	4.8	6.5		5.1	
							50		3.8			2.4	3.5	4.5		3.8			4.7			2.8	4.4	6.5		4.7	
ECL2502																										
2, 14,16	1	4, 12,13	5	7, 9,11	8		4		2.4			1.5	2.3	3.3		2.4			3.3			1.7	3.0	4.7		3.3	
							50		3.5			2.4	3.3	4.4		3.5			4.2			2.5	3.9	6.5		4.2	
ECL2503																										
1, 16	2	13, 14	4	11, 12	5	8, 9	7	4	2.6			1.7	2.5	3.5		2.6			4.3			2.8	4.0	5.6		4.3	
								50	3.8			2.4	3.5	4.5		3.8			4.4			2.8	4.1	6.5		4.4	
ECL2504																										
14	1, 16	13	4, 2	12	5, 7	11	8, 9	4	2.4			1.5	2.3	3.3		2.4			3.3			1.7	3.0	4.7		3.3	
								50	3.5			2.4	3.3	4.4		3.5			4.2			2.5	3.9	6.5		4.2	
ECL2505																										
1, 14, 16	2	11, 12, 13	4	7, 8, 9	5			4	2.6			1.7	2.5	3.5		2.6			4.3			2.8	4.0	5.6		4.3	
								50	3.8			2.4	3.5	4.5		3.8			4.4			2.8	4.1	6.5		4.4	
ECL2511																										
16	1	13	4	12	5	9	8	4	2.4			1.7	2.5	3.5		2.4			4.0			2.6	3.8	5.2		4.0	
								50	3.4			2.4	3.6	4.5		3.4			4.5			2.6	4.3	6.5		4.5	
14	1	14	4	14	5	14	8	4	2.7			1.9	2.8	3.7		2.7			4.2			2.6	4.0	5.4		4.2	
								50	3.4			2.7	3.7	4.9		3.4			4.7			2.6	4.5	6.5		4.7	

NOTES: 12. Each gate is tested separately.

13. The input pulse is measured as it is applied sequentially to each input of the gate under test and a waveform measurement is made at each of the outputs of that gate. Times are as defined in Figure 1.

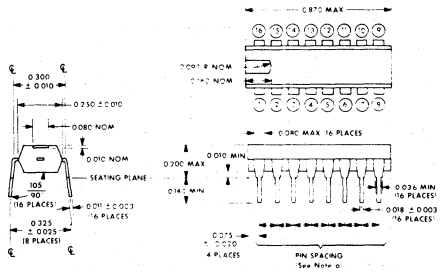
14. Bias voltages and loads for the gate under test are shown in Figure 1. Unused gates have inputs biased to −0.5 V, outputs under load, and power applied.

mechanical data

The circuit bars are mounted on a 16-lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperatures with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. This package is intended for insertion in mounting-hole rows on 0.300-inch centers. Once the leads are compressed to 0.300-inch separation and inserted, sufficient tension is provided to secure the package in the board during soldering. Silver-plated leads require no additional cleaning or processing when used in soldered assembly.

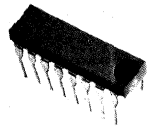
The plastic case is electrically nonconductive.

16-PIN PLASTIC DUAL-IN-LINE PACKAGE OUTLINE



NOTES a. The true position pin spacing is 0.100 between center lines. Each pin centerline is located within 0.010 of its true longitudinal position relative to pins 1 and 16.

b. All dimensions are in inches unless otherwise noted.



terminal designations

Pin assignments are shown in the table below and correspond to the logic diagrams on page 3.
Outputs are denoted Y or Z. Inputs are denoted A, B, C, etc.
Respective inputs and outputs are identified by a gate number preceding the pin symbol.
Power is supplied via the V_{CC}, V_{EE}, and V_{BB} terminals.
V_{BB} is a reference voltage.
NC indicates no internal connection.

PIN ASSIGNMENTS

PIN	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
ECL2500	1A	1Y	V_{CC}	1Z	2Y	V_{CC}	2Z	2A	2B	V_{EE}	2C	2D	1B	1C	V_{BB}	1D
ECL2501	A	Y	V_{CC}	Z	NC	NC	B	C	D	V_{EE}	E	F	G	H	V_{BB}	I
ECL2502	1Z	1Y	V_{CC}	2Y	2Z	V_{CC}	3Y	3Z	3A	V_{EE}	3B	2A	2B	1A	V_{BB}	1B
ECL2503	1A	1Z	V_{CC}	2Z	3Z	V_{CC}	4Z	4A	4B	V_{EE}	3A	3B	2A	2B	V_{BB}	1B
ECL2504	1Y	2Z	V_{CC}	2Y	3Y	V_{CC}	3Z	4Y	4Z	V_{EE}	4A	3A	2A	1A	V_{BB}	1Z
ECL2505	1A	1Z	V_{CC}	2Z	3Z	V_{CC}	3A	3B	3C	V_{EE}	2A	2B	2C	1B	V_{BB}	1C
ECL2511	1Y	V_{CC}	V_{CC}	2Y	3Y	V_{CC}	V_{CC}	4Y	4A	V_{EE}	NC	3A	2A	B	V_{BB}	1A

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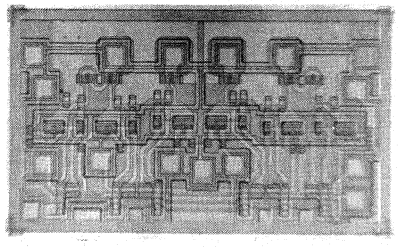
ECL2500 SERIES EMITTER-COUPLED-LOGIC (ECL) MULTIFUNCTION GATES FOR APPLICATION IN ULTRA-HIGH-SPEED DIGITAL SYSTEMS



description

The ECL2500 series is a compatible family of ECL functions with basic gate delays of 2 to 3 ns per stage. The family is specifically designed for operation from 0°C to 75°C.

The ECL2500 family includes:

- Basic Gate Modules
- **Multifunction Gate Modules**
- Bistable Modules
- Arithmetic Modules
- Interface Modules
- Memory Module

family features

- High speed . . . typical gate propagation delay time of 2.5 ns
- Complementary OR/NOR outputs with capability for wired-OR connections
- Designed for use with transmission lines to ensure maximum signal transmission without noise. Characterized for 50-ohm lines
- High noise immunity: ±225 mV typical at 25°C

This data sheet covers the multifunction-gate modules. Separate data sheets cover the balance of the ECL2500 modules.

ECL2500 series multifunction gates

The seven ECL2500 series modules that form the multifunction gate group are shown in the table below. These modules contain various combinations of the multifunction ECL circuit shown in the schematic of Figure A and the logic diagrams of Figure B.

SUMMARY OF MODULES IN MULTIFUNCTION GATE GROUP

MODULE	GATES PER MODULE	INPUTS PER GATE	POSITIVE LOGIC	OUTPUTS PER MODULE	
				Y	Z
ECL2506	4	3	NOR-OR		1
ECL2507	5	2	NOR-OR		1
ECL2508	6	2	NOR-OR		1
ECL2509	4	2	OR-AND/NOR-OR	1	1
ECL2510	4	3,3,3,2	OR-AND/NOR-OR	1	1
ECL2512	6	2 (1 common to each 2 gates)	NOR-OR		2
ECL2513	4	2 (1 common to 2 gates)	OR-AND/NOR-OR	2	2

schematic

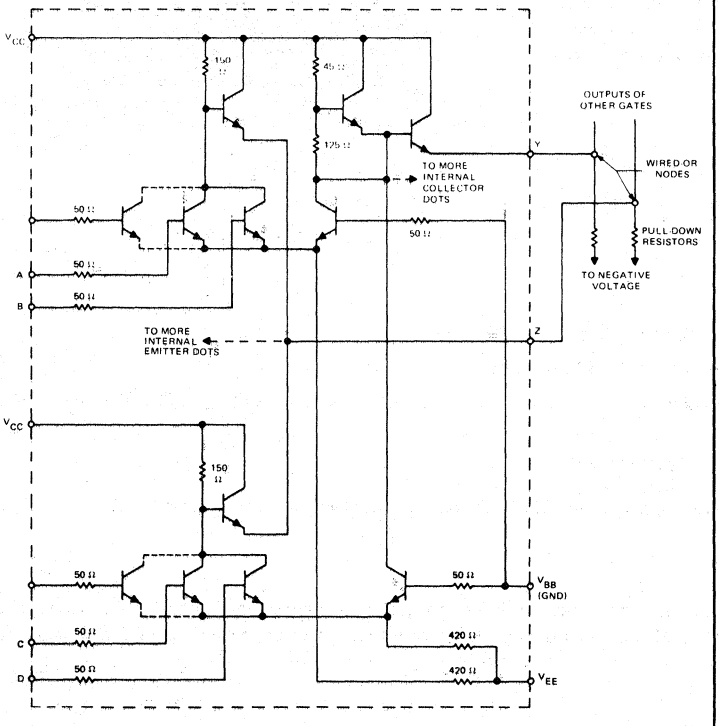


FIGURE A – TYPICAL SCHEMATIC

logic

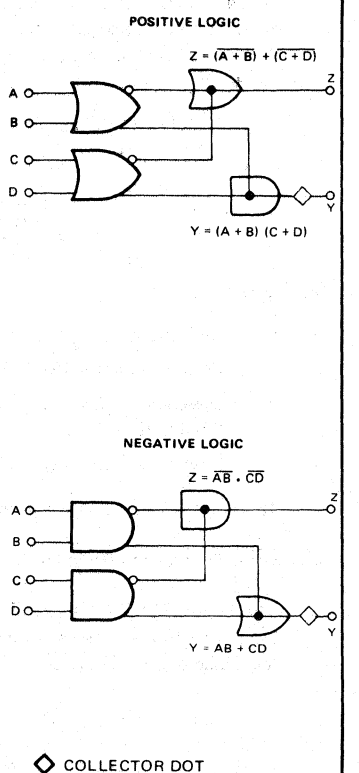


FIGURE B – TYPICAL LOGIC DIAGRAMS

Positive logic OR-AND/NOR-OR functions or negative logic AND-OR/NAND-AND functions are provided at the Y and Z outputs, as shown.

Emitter-follower outputs require an external pull-down resistor. The wired-OR function can be obtained by connecting emitter-follower outputs of separate gates together. Only one pull-down resistor is required for each wired-OR node.

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truth tables (for this series, H = positive voltage, L = negative voltage, X = irrelevant)

ECL2506

INPUTS											OUTPUT
A	B	C	D	E	F	G	H	I	J	K	L	Z
L	L	L	X	X	X	X	X	X	X	X	X	H
X	X	X	L	L	L	X	X	X	X	X	X	H
X	X	X	X	X	X	L	L	L	X	X	X	H
X	X	X	X	X	X	X	X	X	L	L	L	H
For a LOW output, at least one input of each gate must be HIGH												
H	X	X	H	X	X	H	X	X	H	X	X	L
X	H	X	X	H	X	X	H	X	X	H	X	L
X	X	H	X	X	H	X	X	H	X	X	H	L

ECL2507

INPUTS									OUTPUT
A	B	C	D	E	F	G	H	I	J	Z
L	L	X	X	X	X	X	X	X	X	H
X	X	L	L	X	X	X	X	X	X	H
X	X	X	X	L	L	X	X	X	X	H
X	X	X	X	X	X	L	L	X	X	H
X	X	X	X	X	X	X	X	L	L	H
For a LOW output, at least one input of each gate must be HIGH										
H	X	H	X	H	X	H	X	H	X	L
X	H	X	H	X	H	X	H	X	H	L

ECL2508

INPUTS										OUTPUT
A	B	C	D	E	F	G	H	I	J	K	L	Z
L	L	X	X	X	X	X	X	X	X	X	X	H
X	X	L	L	X	X	X	X	X	X	X	X	H
X	X	X	X	L	L	X	X	X	X	X	X	H
X	X	X	X	X	X	L	L	X	X	X	X	H
X	X	X	X	X	X	X	X	L	L	X	X	H
X	X	X	X	X	X	X	X	X	X	L	L	H
For a LOW output, at least one input of each gate must be HIGH												
H	X	H	X	H	X	H	X	H	X	H	X	L
X	H	X	H	X	H	X	H	X	H	X	H	L

ECL2509

INPUTS								OUTPUTS	
A	B	C	D	E	F	G	H	Y	Z
L	L	X	X	X	X	X	X	L	H
X	X	L	L	X	X	X	X	L	H
X	X	X	X	L	L	X	X	L	H
X	X	X	X	X	X	L	L	L	H
For a HIGH Y and LOW Z, at least one input of each gate must be HIGH									
H	X	H	X	H	X	H	X	H	L
X	H	X	H	X	H	X	H	H	L

ECL2510

INPUTS										OUTPUTS	
A	B	C	D	E	F	G	H	I	J	K	Y	Z
L	L	X	X	X	X	X	X	X	X	X	L	H
X	X	L	L	L	X	X	X	X	X	X	L	H
X	X	X	X	X	L	L	L	X	X	X	L	H
X	X	X	X	X	X	X	X	L	L	L	L	H
For a HIGH Y and LOW Z, at least one input of each gate must be HIGH												
H	X	H	X	X	H	X	X	H	X	X	H	L
X	H	X	H	X	X	H	X	X	H	X	H	L
X	H	X	X	H	X	X	H	X	X	H	H	L

ECL2512

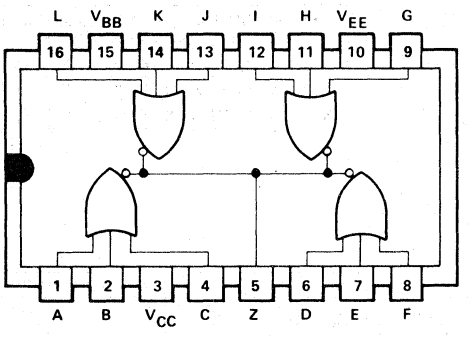
INPUTS												OUTPUTS	
1A	D	1B	E	1C	F	2A	D	2B	E	2C	F	1Z	2Z
L	L	X	X	X	X		L					H	Determined
X	X	L	L	X	X				L			H	by inputs
X	X	X	X	L	L						L	H	2A,2B,2C,
H	X	H	X	H	X							L	D,E, and F.
X	H	X	H	X	H		H		H		H	L	(See below)
	L					L	L	X	X	X	X	Determined	H
		L				X	X	L	L	X	X	by inputs	H
				L		X	X	X	X	L	L	1A,1B,1C,	H
						H	X	H	X	H	X	D,E, and F.	L
	H		H		H	X	H	X	H	X	H	(See above)	L
For a LOW output from either section, at least one input of each gate in that section must be HIGH													

ECL2513

INPUTS								OUTPUTS	
1A	1B	1C	D	2A	2B	2C	D	1Y 1Z	2Y 2Z
L	L	X	X					L H	Determined
X	X	L	L				L	L H	by inputs
H	X	H	X					H L	2A,2B,2C, and D.
X	H	X	H				H	H L	(See below)
				L	L	X	X	Determined	L H
			L	X	X	L	L	by inputs	L H
				H	X	H	X	1A,1B,1C, and D.	H L
			H	X	H	X	H	(See above)	H L
For a HIGH Y and LOW Z from either section, at least one input of each gate in that section must be HIGH									

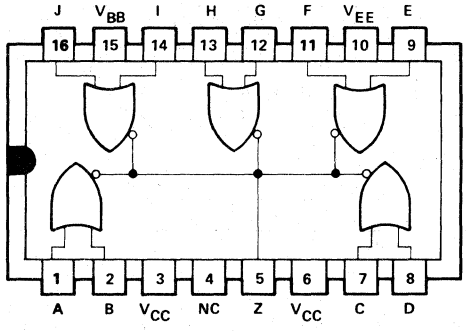
logic

ECL2506



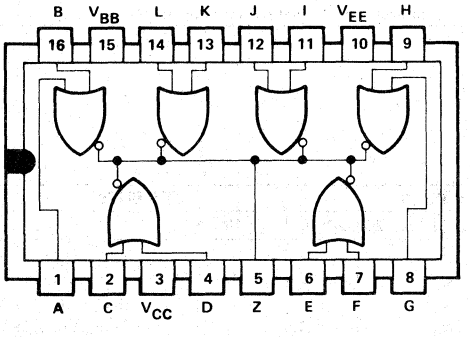
4-WIDE 3-INPUT NOR-OR GATE

ECL2507



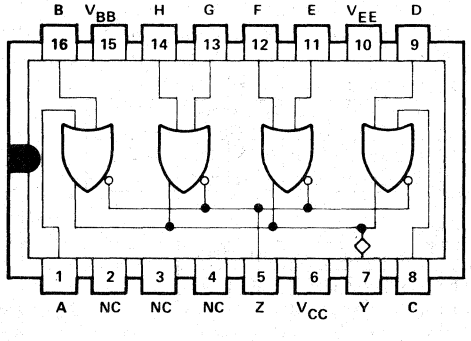
5-WIDE 2-INPUT NOR-OR GATE

ECL2508



6-WIDE 2-INPUT NOR-OR GATE

ECL2509



4-WIDE 2-INPUT
OR-AND/NOR-OR GATE

NC—No internal connection

◇ — Collector Dot

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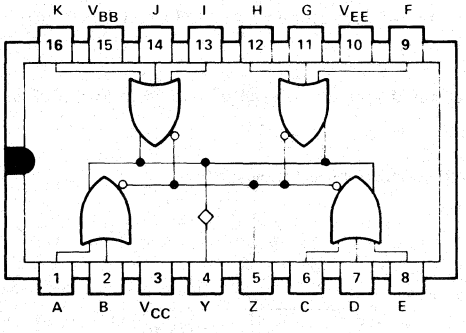
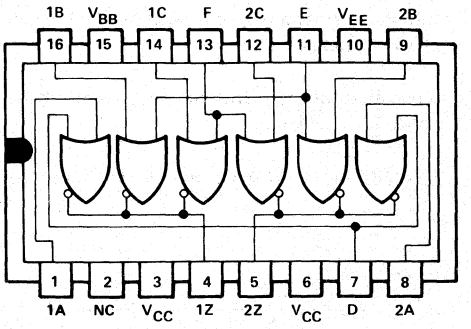
ECL2510



4-WIDE 3-3-3-2 INPUT
OR-AND/NOR-OR GATE

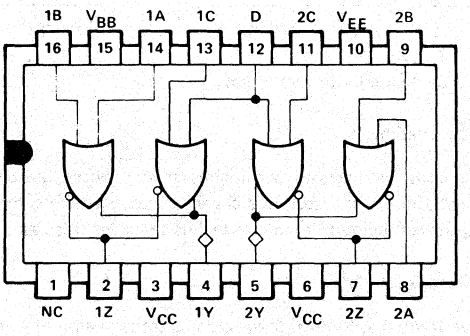
ECL2512



DUAL 3-WIDE 2-INPUT NOR-OR GATE
WITH COMMON INPUTS

4

ECL2513



DUAL 2-WIDE 2-INPUT OR-AND/NOR-OR GATE
WITH COMMON INPUT

MODULE	POSITIVE LOGIC		NEGATIVE LOGIC	
	Y	Z	Y	Z
ECL2506		$\overline{A+B+C} + \overline{D+E+F} + \overline{G+H+I} + \overline{J+K+L}$		$\overline{ABC} \cdot \overline{DEF} \cdot \overline{GHI} \cdot \overline{JKL}$
ECL2507		$\overline{A+B} + \overline{C+D} + \overline{E+F} + \overline{G+H} + \overline{I+J}$		$\overline{AB} \cdot \overline{CD} \cdot \overline{EF} \cdot \overline{GH} \cdot \overline{IJ}$
ECL2508		$\overline{A+B} + \overline{C+D} + \overline{E+F} + \overline{G+H} + \overline{I+J} + \overline{K+L}$		$\overline{AB} \cdot \overline{CD} \cdot \overline{EF} \cdot \overline{GH} \cdot \overline{IJ} \cdot \overline{KL}$
ECL2509	(A+B) (C+D) (E+F) (G+H)	$\overline{A+B} + \overline{C+D} + \overline{E+F} + \overline{G+H}$	AB + CD + EF + GH	$\overline{AB} \cdot \overline{CD} \cdot \overline{EF} \cdot \overline{GH}$
ECL2510	(A+B) (C+D+E) (F+G+H) (I+J+K)	$\overline{A+B} + \overline{C+D+E} + \overline{F+G+H} + \overline{I+J+K}$	AB + CDE + FGH + IJK	$\overline{AB} \cdot \overline{CDE} \cdot \overline{FGH} \cdot \overline{IJK}$
ECL2512		$\overline{A+D} + \overline{B+E} + \overline{C+F}$		$\overline{AD} \cdot \overline{BE} \cdot \overline{CF}$
ECL2513	(A+B) (C+D)	$\overline{A+B} + \overline{C+D}$	AB + CD	$\overline{AB} \cdot \overline{CD}$

NC—No internal connection ◇— Collector Dot

GENERAL APPLICATION INFORMATION

Multiple V_{CC} terminals have been supplied to reduce crosstalk noise. All V_{CC} terminals should be connected even if all gates in a module are not used.

Applications of the multifunction gates at other than data sheet conditions are covered in a separate ECL2500 series application document.

The multifunction gates divide into two groups with internal wired connections as follows:

MODULE	COLLECTOR DOTS	EMITTER DOTS
ECL2513†	2	2
ECL2509	4	4
ECL2510	4	4

†Each half

MODULE	EMITTER DOTS
ECL2512†	3
ECL2506	4
ECL2507	5
ECL2508	6

†Each half

General loading for fan-out may be divided into two classes:

CLASS I Short-Line or Cluster Loading.

Loads which can be connected within two inches of any source can be treated as lumped capacitive loads which include the gate inputs and stub-line capacitances. Switching times can be interpolated accordingly. No two dotted outputs can be more than two inches apart for this case.

CLASS II Long-Line or Distributive Loading.

These loads must be treated as lumped loads along a transmission line and termination should be at the end of the transmission chain. No more than 20 pF of load is recommended per 4.5 inches of 50-ohm printed line (with dielectric constant of 4.5) in order that the reflection coefficient be no greater than 20%. If the loads are lumped loads of 20 pF, they must be 4.5 inches apart. If individual gates and CLASS I loads are distributed, they must not exceed the 20 pF per 4.5 inches of line.

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absolute maximum ratings (see note 1)

Terminal voltages and currents . . . . . See table below
Storage temperature range . . . . . −40°C to 150°C
Temperature range with supply and bias voltages applied . . . . . −40°C to 100°C

TERMINAL VOLTAGE AND/OR CURRENT, T_A = 0°C TO 75°C (SEE NOTES 2 AND 3)

TERMINAL	REMARKS	VOLTAGE		CURRENT
		CONTINUOUS	20-μs SURGE	
V_{CC}		2 V	4.5 V	
V_{EE}		−4 V	−7 V	
Each Input	All other inputs open	−3.5 V	−4 V	
		2 V	2 V	
Output Y	All inputs high			−40 mA
Output Z	All inputs low			−40 mA

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recommended operating conditions

Supply voltage V_{CC} . . . . . 1.32 V ± 2%
Supply voltage V_{EE} . . . . . −3.2 V ± 2%
Reference voltage V_{BB} . . . . . 0 V (GND)
Reverse bias on unused inputs . . . . . −1 V ± 0.5 V
Normalized d-c fan-out . . . . . 0 to 35
Load on each output . . . . . characterized at 270 Ω to V_{EE}, 50 Ω to GND
Operating free-air temperature range . . . . . 0°C to 75°C

NOTES: 1. Absolute maximum ratings are limits beyond which the life of individual devices may be impaired and are never to be exceeded in service or testing.
2. Maximum terminal conditions must be considered as mutually exclusive.
3. All voltages are referenced to V_{BB}, which is at GND.

electrical characteristics at specified free-air temperature

PARAMETER		TEST FIGURE	TEST CONDITIONS*		MODULE							SEE NOTE 4			UNIT
					ECL2506	ECL2507	ECL2508	ECL2509	ECL2510	ECL2512	ECL2513	MIN	TYP	MAX	
V_{IH}	High-level input voltage			0°C 25°C 75°C	•	•	•	•	•	•	•	150 150 150		720 720 720	mV
V_{IL}	Low-level input voltage			0°C 25°C 75°C	•	•	•	•	•	•	•	−1500 −1500 −1500		−150 −150 −150	mV
$V_{OH(Y)}$	High-level output voltage at Y output	2	V_I = 0.2 V	0°C 25°C 75°C				•	•		•	315 350	390 425 495	 500 580	mV
$V_{OL(Y)}$	Low-level output voltage at Y output	2	V_I = −0.2 V	0°C 25°C 75°C				•	•		•	−505 −490	**−450** **−410** **−290**	 −350 **−230**	mV
$V_{OH(Z)}$	High-level output voltage at Z output	2	V_I = −0.2 V	0°C 25°C 75°C	•	•	•	•	•	•	•	315 350	390 425 495	 500 580	mV
$V_{OL(Z)}$	Low-level output voltage at Z output	2	V_I = 0.2 V	0°C 25°C 75°C	•	•	•	•	•	•	•	−440	−385 −365 −325	 −310 −280	mV
$V_{OL(Z)}$	Low-level output voltage at Z output	2	V_I = 0.4 V	0°C 25°C 75°C	•	•	•	•	•	•	•	−505 −490	−455 −425 −380	 −315	mV
$V_{OH(Z)}$	High-level output voltage at Z output	2	V_I = −0.5 V	0°C 25°C 75°C	•	•	•	•	•	•	•			630† 700†	mV
$V_{OH(Y)}$	High-level output voltage at Y output	2	V_I = 0.15 V	0°C 25°C 75°C				•	•		•	290 325			mV
$V_{OL(Y)}$	Low-level output voltage at Y output	2	V_I = −0.15 V	0°C 25°C 75°C				•	•		•			−335 −215	mV
$V_{OH(Z)}$	High-level output voltage at Z output	2	V_I = −0.15 V	0°C 25°C 75°C	•	•	•			•		290 325			mV
$V_{OL(Z)}$	Low-level output voltage at Z output	2	V_I = 0.15 V	0°C 25°C 75°C	•	•	•			•				−290 −260	mV
I_{IH}	High-level input current (each input)	3	V_I = 0.5 V	0°C 25°C 75°C	•	•	•	•	•	•	•			255 235 200	μA
I_{IL}	Low-level input current	4	V_I = −3.2 V	0°C 25°C 75°C	•	•	•	•	•	•	•			−0.6‡ −0.8‡ −1.2‡	μA
I_{CC} or $-I_{EE}$	Supply current	5	V_I = −0.5 V	25°C	• 	 • 	 • 	 • 	 • 	 • 	 •	17 23 27 17 17 27 17		28 35 42 28 28 42 28	mA
C_{in}	Input capacitance (each input)		See Note 5	25°C	•	•	•	•	•	•	•		5		pF
z_{out}	Output impedance		See Note 6	25°C	•	•	•	•	•	•	•		5		Ω

*V_{BB} = GND, V_{CC} = 1.32 V ± 1%, V_{EE} = −3.20 V ± 1%.

†These are worst case values for ECL2508 which has six emitters dotted. See Supplementary Parameter Measurement Information for each module.

‡These are worst-case values for twelve inputs in parallel. See Supplementary Parameter Measurement Information for each module.

NOTES: 4. The algebraic convention where the most positive limit is designated as maximum is used in this data sheet for logic voltage levels only, e.g., if −350 mV is a maximum, the typical and minimum limits are more negative voltages.

5. C_{in} is measured using peak current techniques. A square-wave input pulse is applied, and the input current waveform is integrated with respect to time to determine Q. C_{in} = Q/V.

6. Constant-current loads are used to determine the output impedance which is derived from the slope of a V_O vs I_O curve.

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operating characteristics at specified free-air temperature (see figure 1)

PARAMETER		C_L	T_A	ECL2506 THRU ECL2508, ECL2512			ECL2509, ECL2510, ECL2513			UNIT
				Z OUTPUTS			ANY OUTPUT			
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Propagation delay time, high-to-low-level output and/or Propagation delay time, low-to-high-level output	4 pF	0°C		2.6			2.6		ns
			25°C	1.7	2.6	3.5	1.6	2.6	4.1	
			75°C		2.6			2.6		
t_{PLH}		50 pF	0°C		3.6			3.5		ns
			25°C	2.4	3.6	4.5	2.5	3.5	4.6	
			75°C		3.6			3.6		
t_{THL}	Transition time, high-to-low-level output and/or Transistion time, low-to-high-level output	4 pF	0°C		4.0			3.4		ns
			25°C	2.8	4.0	5.6	2.0	3.4	6.3	
			75°C		4.1			3.5		
t_{TLH}		50 pF	0°C		4.5			4.4		ns
			25°C	2.8	4.5	6.5	2.5	4.3	6.5	
			75°C		4.4			4.1		

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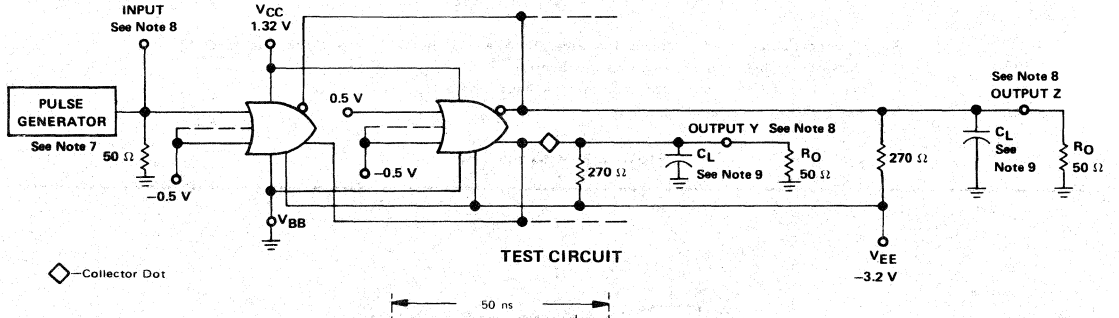
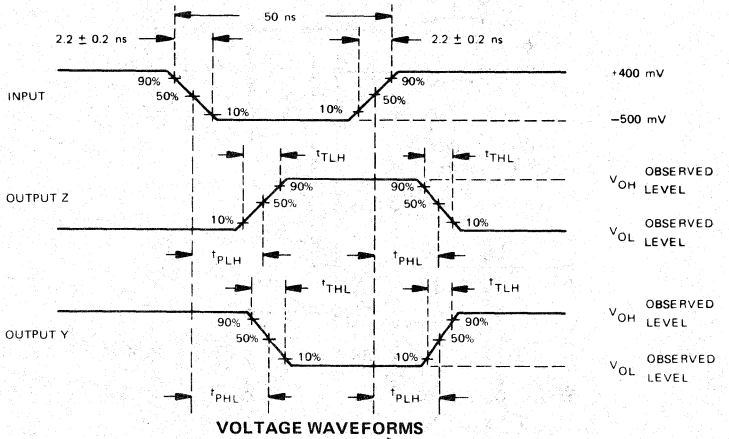
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

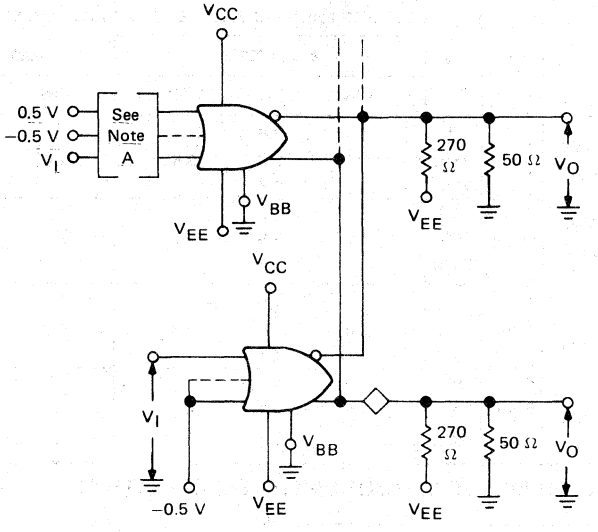


VOLTAGE WAVEFORMS

FIGURE 1—PROPAGATION DELAY AND TRANSITION TIMES

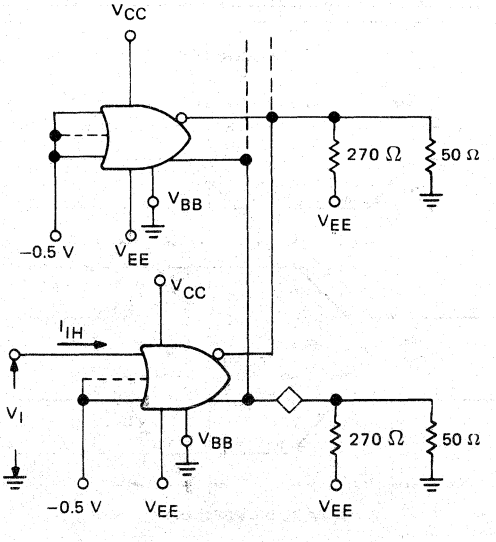
NOTES: 7. The generator has the following characteristics: Z_{out} = 50 Ω, PRR = 1 MHz.
8. The waveforms are monitored on an oscilloscope with a rise time of less than or equal to 350 ps. Either a high-impedance probe with an input impedance of 100 kΩ paralleled by 2 pF, or a 50-Ω impedance system can be used. The 50-Ω resistors designated R_O are the oscilloscope input resistance in the 50-Ω system or discrete resistors with a high-impedance probe.
9. C_L includes probe and fixture capacitance. A capacitance of 50 pF can be used to approximate an a-c fan-out of 10.

PARAMETER MEASUREMENT INFORMATION†



A. The particular input voltages for each module are shown in the Supplementary Parameter Measurement Information Section.
B. V_I is applied to each input separately except where Note 13 applies.
C. Each output is tested separately.

FIGURE 2–V_{OH} and V_{OL}



Each input is tested separately.

FIGURE 3–I_{IH}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.
◇ – Collector Dot

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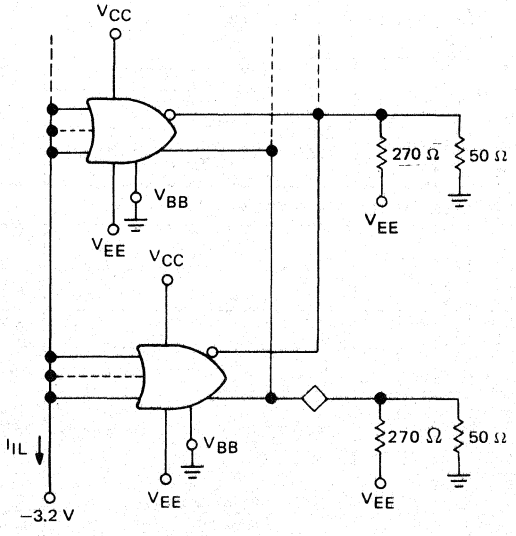
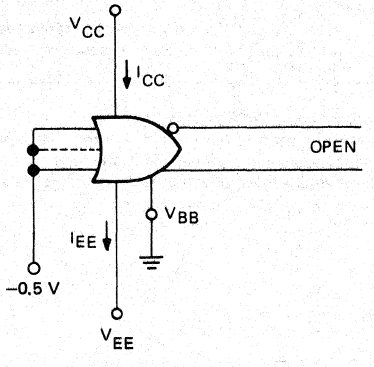
PARAMETER MEASUREMENT INFORMATION†



All inputs of all gates are connected in parallel.

FIGURE 4–I_{IL}



A. All gates are tested simultaneously.
B. I_{CC} is the total current into all V_{CC} terminals.

FIGURE 5–I_{CC} or I_{EE}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

◇ – Collector Dot

SUPPLEMENTARY PARAMETER MEASUREMENT INFORMATION

electrical characteristics at specified free-air temperature

PARAMETER (SEE NOTE 10)	TERMINALS TO TO BE TESTED (SEE NOTE 11)		TEST FIGURE	INPUT CONDITIONS			T_A	MIN	TYP	MAX	UNIT
	INPUTS	OUTPUTS Y Z		INPUT UNDER TEST	OTHER INPUT(S) OF SAME GATE	INPUTS OF OTHER GATE(S)					
ECL2506	**V_{BB} (pin 15) = GND, V_{CC} (pin 3) = 1.32 V, V_{EE} (pin 10) = −3.2 V**										
$V_{OH(Z)}$	1, 2, 4 6, 7, 8 9, 11, 12 13, 14, 16	5	2	−0.2 V	−0.5 V	See Note 12	0°C 25°C 75°C	315 350	390 425 495	500 580	mV
$V_{OL(Z)}$	1, 2, 4 6, 7, 8 9, 11, 12 13, 14, 16	5	2	0.2 V	−0.5 V	See Note 13	0°C 25°C 75°C	−440	−385 −365 −325	−310 −280	mV
$V_{OL(Z)}$	1, 2, 4 6, 7, 8 9, 11, 12 13, 14, 16	5	2	0.4 V	−0.5 V	See Note 13	0°C 25°C 75°C	−505 −490	−455 −425 −380	 −315	mV
$V_{OH(Z)}$	1, 2, 4 6, 7, 8 9, 11, 12 13, 14, 16	5	2	All inputs of all gates in parallel at −0.5 V			0°C 25°C 75°C			615 685	mV
$V_{OH(Z)}$	4	5	2	−0.15 V	−0.5 V	See Note 12	0°C 25°C 75°C	290 325			mV
$V_{OL(Z)}$	4	5	2	0.15 V	−0.5 V	See Note 13	0°C 25°C 75°C			−290 −260	mV
I_{IH}	1, 2, 4 6, 7, 8 9, 11, 12 13, 14, 16		3	0.5 V	−0.5 V	−0.5 V	0°C 25°C 75°C			255 235 200	μA
I_{IL}	1, 2, 4, 6, 7, 8, 9, 11, 12, 13, 14, 16		4	All inputs of all gates in parallel at −3.2 V			0°C 25°C 75°C			−0.6 −0.8 −1.2	μA

NOTES: 10. See page 8 for defining term associated with each symbol.
11. Each gate is tested separately unless otherwise noted. See referenced test figure for output termination. Gates not under test have their outputs terminated in the same manner, and power applied.
12. At least one input of each other gate must be at 0.5 V. Other inputs are biased to −0.5 V.
13. One input of each gate must be at V_I. Other inputs are biased to −0.5 V.

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SUPPLEMENTARY PARAMETER MEASUREMENT INFORMATION

electrical characteristics at specified free-air temperature

PARAMETER (SEE NOTE 10)	TERMINALS TO BE TESTED (SEE NOTE 11)		TEST FIGURE	INPUT CONDITIONS			T_A	MIN	TYP	MAX	UNIT
	INPUTS	OUTPUTS Y Z		INPUT UNDER TEST	OTHER INPUT(S) OF SAME GATE	INPUTS OF OTHER GATE(S)					
ECL2507	**V_{BB} (pin 15) = GND, V_{CC} (pin 3 and pin 6) = 1.32 V, V_{EE} (pin 10) = −3.2 V**										
$V_{OH(Z)}$	1, 2 7, 8 9, 11 12, 13 14, 16	5	2	−0.2 V	−0.5 V	See Note 12	0°C 25°C 75°C	315 350	390 425 495	500 580	mV
$V_{OL(Z)}$	1, 2 7, 8 9, 11 12, 13 14, 16	5	2	0.2 V	−0.5 V	See Note 13	0°C 25°C 75°C	−440	−385 −365 −325	−310 −280	mV
$V_{OL(Z)}$	1, 2 7, 8 9, 11 12, 13 14, 16	5	2	0.4 V	−0.5 V	See Note 13	0°C 25°C 75°C	−505 −490	−455 −425 −380	 −315	mV
$V_{OH(Z)}$	1, 2 7, 8 9, 11 12, 13 14, 16	5	2	All inputs of all gates in parallel at −0.5 V			0°C 25°C 75°C			 625 695	mV
$V_{OH(Z)}$	2	5	2	−0.15 V	−0.5 V	See Note 12	0°C 25°C 75°C	290 325			mV
$V_{OL(Z)}$	2	5	2	0.15 V	−0.5 V	See Note 13	0°C 25°C 75°C			−290 −260	mV
I_{IH}	1, 2 7, 8 9, 11 12, 13 14, 16		3	0.5 V	−0.5 V	−0.5 V	0°C 25°C 75°C			255 235 200	μA
I_{IL}	1, 2, 7, 8, 9, 11, 12, 13, 14, 16		4	All inputs of all gates in parallel at −3.2 V			0°C 25°C 75°C			−0.5 −0.7 −1.0	μA

NOTES: 10. See page 8 for defining term associated with each symbol.
11. Each gate is tested separately unless otherwise noted. See referenced test figure for output termination. Gates not under test have their outputs terminated in the same manner, and power applied.
12. At least one input of each other gate must be at 0.5 V. Other inputs are biased to −0.5 V.
13. One input of each gate must be at V_I. Other inputs are biased to −0.5 V.

SUPPLEMENTARY PARAMETER MEASUREMENT INFORMATION

electrical characteristics at specified free-air temperature

PARAMETER (SEE NOTE 10)	TERMINALS TO BE TESTED (SEE NOTE 11)		TEST FIGURE	INPUT CONDITIONS			T_A	MIN	TYP	MAX	UNIT
	INPUTS	OUTPUTS Y Z		INPUT UNDER TEST	OTHER INPUT(S) OF SAME GATE	INPUTS OF OTHER GATE(S)					
ECL2508	V_{BB} (pin 15) = GND, V_{CC} (pin 3) = 1.32 V, V_{EE} (pin 10) = −3.2 V										
$V_{OH(Z)}$	1, 16 2, 4 6, 7 8, 9 11, 12 13, 14		5	2	−0.2 V	−0.5 V	See Note 12	0°C 25°C 75°C	315 350	390 425 495	500 580	mV
$V_{OL(Z)}$	1, 16 2, 4 6, 7 8, 9 11, 12 13, 14		5	2	0.2 V	−0.5 V	See Note 13	0°C 25°C 75°C	−440	−385 −365 −325	−310 −280	mV
$V_{OL(Z)}$	1, 16 2, 4 6, 7 8, 9 11, 12 13, 14		5	2	0.4 V	−0.5 V	See Note 13	0°C 25°C 75°C	−505 −490	−455 −425 −380	 −315	mV
$V_{OH(Z)}$	1, 16 2, 4 6, 7 8, 9 11, 12 13, 14		5	2	All inputs of all gates in parallel at −0.5 V			0°C 25°C 75°C			630 700	mV
$V_{OH(Z)}$	11		5	2	−0.15 V	−0.5 V	See Note 12	0°C 25°C 75°C	290 325			mV
$V_{OL(Z)}$	11		5	2	0.15 V	−0.5 V	See Note 13	0°C 25°C 75°C			−290 −260	mV
I_{IH}	1, 16 2, 4 6, 7 8, 9 11, 12 13, 14			3	0.5 V	−0.5 V	−0.5 V	0°C 25°C 75°C			255 235 200	μA
I_{IL}	1, 2, 4, 6, 7, 8, 9, 11, 12, 13, 14, 16			4	All inputs of all gates in parallel at −3.2 V			0°C 25°C 75°C			−0.6 −0.8 −1.2	μA

NOTES: 10. See page 8 for defining term associated with each symbol.
11. Each gate is tested separately unless otherwise noted. See referenced test figure for output termination. Gates not under test have their outputs terminated in the same manner, and power applied.
12. At least one input of each other gate must be at 0.5 V. Other inputs are biased to −0.5 V.
13. One input of each gate must be at V_I. Other inputs are biased to −0.5 V.

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SUPPLEMENTARY PARAMETER MEASUREMENT INFORMATION

electrical characteristics at specified free-air temperature

PARAMETER (SEE NOTE 10)	TERMINALS TO BE TESTED (SEE NOTE 11)		TEST FIGURE	INPUT CONDITIONS			T_A	MIN	TYP	MAX	UNIT
	INPUTS	OUTPUTS Y Z		INPUT UNDER TEST	OTHER INPUT(S) OF SAME GATE	INPUTS OF OTHER GATE(S)					
ECL2509	V_{BB} (pin 15) = GND, V_{CC} (pin 6) = 1.32 V, V_{EE} (pin 10) = −3.2 V										
$V_{OH(Y)}$	1, 16 8, 9 11, 12 13, 14	7	2	0.2 V	−0.5 V	0.5 V	0°C 25°C 75°C	315 350	390 425 495	500 580	mV
$V_{OL(Y)}$	1, 16 8, 9 11, 12 13, 14	7	2	−0.2 V	−0.5 V	See Note 12	0°C 25°C 75°C	−505 −490	−450 −410 −290	−350 −230	mV
$V_{OH(Z)}$	1, 16 8, 9 11, 12 13, 14	5	2	−0.2 V	−0.5 V	See Note 12	0°C 25°C 75°C	315 350	390 425 495	500 580	mV
$V_{OL(Z)}$	1, 16 8, 9 11, 12 13, 14	5	2	0.2 V	−0.5 V	See Note 13	0°C 25°C 75°C	−440	−385 −365 −325	−310 −280	mV
$V_{OL(Z)}$	1, 16 8, 9 11, 12 13, 14	5	2	0.4 V	−0.5 V	See Note 13	0°C 25°C 75°C	−505 −490	−455 −425 −380	 −315	mV
$V_{OH(Z)}$	1, 16 8, 9 11, 12 13, 14	5	2	All inputs of all gates in parallel at −0.5 V			0°C 25°C 75°C			615 685	mV
$V_{OH(Y)}$	8	7	2	0.15 V	−0.5 V	See Note 13	0°C 25°C 75°C	290 325			mV
$V_{OL(Y)}$	8	7	2	−0.15 V	−0.5 V	See Note 12	0°C 25°C 75°C			−335 −215	mV
I_{IH}	1, 16 8, 9 11, 12 13, 14		3	0.5 V	−0.5 V	−0.5 V	0°C 25°C 75°C			255 235 200	μA
I_{IL}	1, 8, 9, 11, 12, 13, 14, 16		4	All inputs of all gates in parallel at −3.2 V			0°C 25°C 75°C			−0.5 −0.6 −0.8	μA

NOTES: 10. See page 8 for defining term associated with each symbol.
11. Each gate is tested separately unless otherwise noted. See referenced test figure for output termination. Gates not under test have their outputs terminated in the same manner, and power applied.
12. At least one input of each other gate must be at 0.5 V. Other inputs are biased to −0.5 V.
13. One input of each gate must be at V_I. Other inputs are biased to −0.5 V.

SUPPLEMENTARY PARAMETER MEASUREMENT INFORMATION

electrical characteristics at specified free-air temperature

PARAMETER (SEE NOTE 10)	TERMINALS TO TO BE TESTED (SEE NOTE 11)		TEST FIGURE	INPUT CONDITIONS			T_A	MIN	TYP	MAX	UNIT
	INPUTS	OUTPUTS Y Z		INPUT UNDER TEST	OTHER INPUT(S) OF SAME GATE	INPUTS OF OTHER GATE(S)					
ECL2510	**V_{BB} (pin 15) = GND, V_{CC} (pin 3) = 1.32 V, V_{EE} (pin 10) = −3.2 V**										
$V_{OH(Y)}$	1, 2 6, 7, 8 9, 11, 12 13, 14, 16	4	2	0.2 V	−0.5 V	0.5 V	0°C 25°C 75°C	315 350	390 425 495	 500 580	mV
$V_{OL(Y)}$	1, 2 6, 7, 8 9, 11, 12 13, 14, 16	4	2	−0.2 V	−0.5 V	See Note 12	0°C 25°C 75°C	−505 −490	−450 −410 −290	 −350 −230	mV
$V_{OH(Z)}$	1, 2 6, 7, 8 9, 11, 12 13, 14, 16	5	2	−0.2 V	−0.5 V	See Note 12	0°C 25°C 75°C	315 350	390 425 495	 500 580	mV
$V_{OL(Z)}$	1, 2 6, 7, 8 9, 11, 12 13, 14, 16	5	2	0.2 V	−0.5 V	See Note 13	0°C 25°C 75°C	 −440	−385 −365 −325	 −310 −280	mV
$V_{OL(Z)}$	1, 2 6, 7, 8 9, 11, 12 13, 14, 16	5	2	0.4 V	−0.5 V	See Note 13	0°C 25°C 75°C	−505 −490	−455 −425 −380	 −315	mV
$V_{OH(Z)}$	1, 2 6, 7, 8 9, 11, 12 13, 14, 16	5	2	All inputs of all gates in parallel at −0.5 V			0°C 25°C 75°C			 615 685	mV
$V_{OH(Y)}$	2	4	2	0.15 V	−0.5 V	See Note 13	0°C 25°C 75°C	290 325			mV
$V_{OL(Y)}$	2	4	2	−0.15 V	−0.5 V	See Note 12	0°C 25°C 75°C			 −335 −215	mV
I_{IH}	1, 2 6, 7, 8 9, 11, 12 13, 14, 16		3	0.5 V	−0.5 V	−0.5 V	0°C 25°C 75°C			 255 235 200	μA
I_{IL}	1, 2, 6, 7, 8, 9, 11, 12, 13, 14, 16		4	All inputs of all gates in parallel at −3.2 V			0°C 25°C 75°C			 −0.6 −0.8 −1.1	μA

NOTES: 10. See page 8 for defining term associated with each symbol.
11. Each gate is tested separately unless otherwise noted. See referenced test figure for output termination. Gates not under test have their outputs terminated in the same manner, and power applied.
12. At least one input of each other gate must be at 0.5 V. Other inputs are biased to −0.5 V.
13. One input of each gate must be at V_I. Other inputs are biased to −0.5 V.

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SUPPLEMENTARY PARAMETER MEASUREMENT INFORMATION

electrical characteristics at specified free-air temperature

PARAMETER (SEE NOTE 10)	TERMINALS TO BE TESTED (SEE NOTE 11)		TEST FIGURE	INPUT CONDITIONS			T_A	MIN	TYP	MAX	UNIT
	INPUTS	OUTPUTS Y Z		INPUT UNDER TEST	OTHER INPUT(S) OF SAME GATE	REMAINING INPUTS OF OTHER GATE(S)					
ECL2512	V_{BB} (pin 15) = GND, V_{CC} (pin 3 and pin 6) = 1.32 V, V_{EE} (pin 10) = −3.2 V										
$V_{OH(Z)}$	1, 7 11, 16 13, 14	4	2	−0.2 V	−0.5 V	0.5 V	0°C 25°C 75°C	315 350	390 425 495	500 580	mV
	7, 8 9, 11 12, 13	5									
$V_{OL(Z)}$	1, 7 11, 16 13, 14	4	2	0.2 V	−0.5 V	See Note 13	0°C 25°C 75°C	 −440	−385 −365 −325	 −310 −280	mV
	7, 8 9, 11 12, 13	5									
$V_{OL(Z)}$	1, 7 11, 16 13, 14	4	2	0.4 V	−0.5 V	See Note 13	0°C 25°C 75°C	−505 −490	−455 −425 −380	 −315	mV
	7, 8 9, 11 12, 13	5									
$V_{OH(Z)}$	1, 7 11, 16 13, 14	4	2	All inputs of all gates in parallel at −0.5 V			0°C 25°C 75°C			 600 670	mV
	7, 8 9, 11 12, 13	5									
$V_{OH(Z)}$	8	5	2	−0.15 V	−0.5 V	0.5 V	0°C 25°C 75°C	290 325			mV
$V_{OL(Z)}$	8	5	2	0.15 V	−0.5 V	See Note 13	0°C 25°C 75°C			−290 −260	mV
I_{IH}	1 16 14 8 9 12		3	0.5 V	−0.5 V	−0.5 V	0°C 25°C 75°C			255 235 200	μA
	7, 11, 13		3	0.5 V	−0.5 V	−0.5 V	0°C 25°C 75°C			510 470 400	μA
I_{IL}	1, 7, 8, 9, 11, 12, 13, 14, 16		4	All inputs of all gates in parallel at −3.2 V			0°C 25°C 75°C			−0.6 −0.8 −1.2	μA

NOTES: 10. See page 8 for defining term associated with each symbol.
11. Each gate is tested separately unless otherwise noted. See referenced test figure for output termination. Gates not under test have their outputs terminated in the same manner, and power applied.
13. One input of each gate must be at V_I. Other inputs are biased to −0.5 V.

SUPPLEMENTARY PARAMETER MEASUREMENT INFORMATION

electrical characteristics at specified free-air temperature

PARAMETER (SEE NOTE 10)	TERMINALS TO BE TESTED (SEE NOTE 11)		TEST FIGURE	INPUT CONDITIONS			T_A	MIN	TYP	MAX	UNIT
	INPUTS	OUTPUTS Y Z		INPUT UNDER TEST	OTHER INPUT(S) OF SAME GATE	REMAINING INPUTS OF OTHER GATE(S)					
ECL2513	V_{BB} (pin 15) = GND, V_{CC} (pin 3 and pin 6) = 1.32 V, V_{EE} (pin 10) = −3.2 V										
$V_{OH(Y)}$	14, 16 12, 13 8, 9 11, 12	4 5	2	0.2 V	−0.5 V	0.5 V	0°C 25°C 75°C	315 350	390 425 495	500 580	mV
$V_{OL(Y)}$	14, 16 12, 13 8, 9 11, 12	4 5	2	−0.2 V	−0.5 V	0.5 V	0°C 25°C 75°C	−505 −490	−450 −410 −290	−350 −230	mV
$V_{OH(Z)}$	14, 16 12, 13 8, 9 11, 12	2 7	2	−0.2 V	−0.5 V	0.5 V	0°C 25°C 75°C	315 350	390 425 495	500 580	mV
$V_{OL(Z)}$	14, 16 12, 13 8, 9 11, 12	2 7	2	0.2 V	−0.5 V	See Note 13	0°C 25°C 75°C	−440	−385 −365 −325	−310 −280	mV
$V_{OL(Z)}$	14, 16 12, 13 8, 9 11, 12	2 7	2	0.4 V	−0.5 V	See Note 13	0°C 25°C 75°C	−505 −490	−455 −425 −380	−315	mV
$V_{OH(Z)}$	14, 16 12, 13 8, 9 11, 12	2 7	2	All inputs of all gates in parallel at −0.5 V			0°C 25°C 75°C			580 650	mV
$V_{OH(Y)}$	13	4	2	0.15 V	−0.5 V	0.5 V	0°C 25°C 75°C	290 325			mV
$V_{OL(Y)}$	13	4	2	−0.15 V	−0.5 V	0.5 V	0°C 25°C 75°C			−335 −215	mV
I_{IH}	14, 16 13 8, 9 11		3	0.5 V	−0.5 V	−0.5 V	0°C 25°C 75°C			255 235 200	μA
I_{IH}	12		3	0.5 V	−0.5 V	−0.5 V	0°C 25°C 75°C			510 470 400	μA
I_{IL}	8, 9, 11, 12, 13, 14, 16		4	All inputs of all gates in parallel at −3.2 V			0°C 25°C 75°C			−0.5 −0.6 −0.8	μA

NOTES: 10. See page 8 for defining term associated with each symbol.
11. Each gate is tested separately unless otherwise noted. See referenced test figure for output termination. Gates not under test have their outputs terminated in the same manner, and power applied.
13. One input of each gate must be at V_I. Other inputs are biased to −0.5 V.

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SUPPLEMENTARY PARAMETER MEASUREMENT INFORMATION

operating characteristics at specified free-air temperature (see figure 1)

TERMINALS TO BE TESTED (SEE NOTES 16, 17, 18, AND 19)						C_L	t_{PHL} and/or t_{PLH} PROPAGATION TIMES—ns									t_{THL} and/or t_{TLH} TRANSITION TIMES—ns								
							T_A = 0°C			T_A = 25°C			T_A = 75°C			T_A = 0°C			T_A = 25°C			T_A = 75°C		
INPUT	OUTPUT	INPUT	OUTPUT	INPUT	OUTPUT	INPUT	OUTPUT	pF	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
ECL2506																										
1		6		9		13		4		2.6			1.7	2.6	3.5		2.6			4.0			2.8	4.0	5.6		4.1	
2	5	7	5	11	5	14	5																			
4		8		12		16		50		3.6			2.4	3.6	4.5		3.6			4.5			2.8	4.5	6.5		4.4	
ECL2507																										
1		7		9		12		4		2.6			1.7	2.6	3.5		2.6			4.0			2.8	4.0	5.6		4.1	
2	5	8	5	11	5	13	5																			
4		8		12		16		50		3.6			2.4	3.6	4.5		3.6			4.5			2.8	4.5	6.5		4.4	
14								4		2.6			1.7	2.6	3.5		2.6			4.0			2.8	4.0	5.6		4.1	
16	5							50		3.6			2.4	3.6	4.5		3.6			4.5			2.8	4.5	6.5		4.4	
ECL2508																										
1		2		6		8		4		2.6			1.7	2.6	3.5		2.6			4.0			2.8	4.0	5.6		4.1	
16	5	4	5	7	5	9	5																			
11		13						50		3.6			2.4	3.6	4.5		3.6			4.5			2.8	4.5	6.5		4.4	
12	5	14	5					4		2.6			1.7	2.6	3.5		2.6			4.0			2.8	4.0	5.6		4.1	
ECL2509																										
1	7	8	7	11	7	13	7	4		2.6			1.6	2.6	4.1		2.6			3.4			2.0	3.4	6.3		3.5	
16	5	9	5	12	5	14	5	50		3.5			2.5	3.5	4.6		3.6			4.4			2.5	4.3	6.5		4.1	
ECL2510																										
1	4	6	4	9	4	13	4	4		2.6			1.6	2.6	4.1		2.6			3.4			2.0	3.4	6.3		3.5	
		7		11		14																				
2	5	8	5	12	5	16	5	50		3.5			2.5	3.5	4.6		3.6			4.4			2.5	4.3	6.5		4.1	
ECL2512																										
1		11		13		7		4		2.6			1.7	2.6	3.5		2.6			4.0			2.8	4.0	5.6		4.1	
7	4	16	4	14	4	8	5	50		3.6			2.4	3.6	4.5		3.6			4.5			2.8	4.5	6.5		4.4	
9		12						4		2.6			1.7	2.6	3.5		2.6			4.0			2.8	4.0	5.6		4.1	
11	5	13	5					50		3.6			2.4	3.6	4.5		3.6			4.5			2.8	4.5	6.5		4.4	
ECL2513																										
14	4	12	4	8	5	11	5	4		2.6			1.6	2.6	4.1		2.6			3.4			2.0	3.4	6.3		3.5	
16	2	13	2	9	7	12	7	50		3.5			2.5	3.5	4.6		3.6			4.4			2.5	4.3	6.5		4.1	

NOTES: 16. Each gate is tested separately. At least one input of each of the other gates (excluding the inactive half of the ECL2512 or ECL2513) must be at 0.5 V with the other inputs at −0.5 V.

17. The input pulse is measured as it is applied sequentially to each input of the gate under test, and a waveform measurement is made at each of the outputs of that gate. Times are as defined in Figure 1.

18. Other inputs of the same gate as input under test are at −0.5 V.

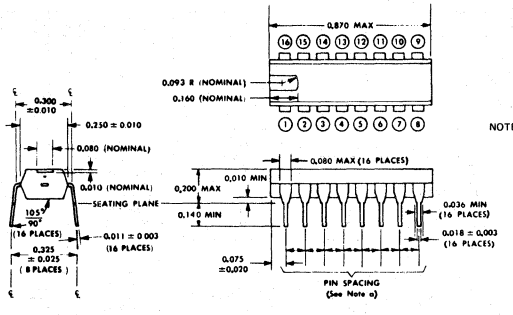
19. Bias voltages and loads for the half of the ECL2512 and ECL2513 under test are shown in Figure 1. The inactive half has remaining inputs biased to −0.5 V, outputs under load, and power applied.

mechanical data

The circuit bars are mounted on a 16-lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperatures with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. This package is intended for insertion in mounting-hole rows on 0.300-inch centers. Once the leads are compressed to 0.300-inch separation and inserted, sufficient tension is provided to secure the package in the board during soldering. Silver-plated leads require no additional cleaning or processing when used in soldered assembly.

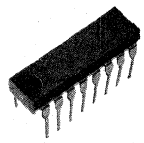
The plastic case is electrically nonconductive.

16-PIN PLASTIC DUAL-IN-LINE PACKAGE OUTLINE



NOTES: a. The true-position pin spacing is 0.100 between center-lines. Each pin centerline is located within 0.010 of its true longitudinal position relative to pins 1 and 16.

b. All dimensions are in inches unless otherwise noted.



terminal designations

Pin assignments are shown in the table below and correspond to the logic diagrams on pages 4 and 5.

Outputs are denoted by Y or Z. Inputs are denoted by A, B, C, etc.

Respective inputs and outputs are identified by a gate number preceding the pin symbol.

Power is supplied via the V_{CC}, V_{EE}, and V_{BB} terminals.

V_{BB} is a reference voltage.

NC indicates no internal connection.

PIN ASSIGNMENTS

PIN	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
ECL2506	A	B	V_{CC}	C	Z	D	E	F	G	V_{EE}	H	I	J	K	V_{BB}	L
ECL2507	A	B	V_{CC}	NC	Z	V_{CC}	C	D	E	V_{EE}	F	G	H	I	V_{BB}	J
ECL2508	A	C	V_{CC}	D	Z	E	F	G	H	V_{EE}	I	J	K	L	V_{BB}	B
ECL2509	A	NC	NC	NC	Z	V_{CC}	Y	C	D	V_{EE}	E	F	G	H	V_{BB}	B
ECL2510	A	B	V_{CC}	Y	Z	C	D	E	F	V_{EE}	G	H	I	J	V_{BB}	K
ECL2512	1A	NC	V_{CC}	1Z	2Z	V_{CC}	D	2A	2B	V_{EE}	E	2C	F	1C	V_{BB}	1B
ECL2513	NC	1Z	V_{CC}	1Y	2Y	V_{CC}	2Z	2A	2B	V_{EE}	2C	D	1C	1A	V_{BB}	1B

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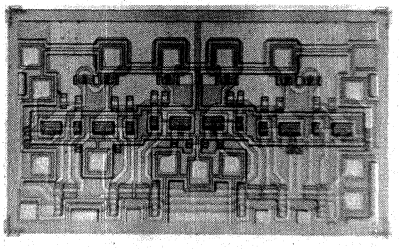
ECL2500 SERIES EMITTER-COUPLED-LOGIC (ECL) ARITHMETIC MODULES FOR APPLICATION IN ULTRA-HIGH-SPEED DIGITAL SYSTEMS

description

The ECL2500 series is a compatible family of ECL functions with basic gate delays of 2 to 3 ns per stage. The family is specifically designed for operation from 0°C to 75°C.



The ECL2500 family includes:

- Basic Gate Modules
- Multifunction Gate Modules
- Bistable Modules
- **Arithmetic Modules**
- Interface Modules
- Memory Module

family features

- High speed. . .typical gate propagation delay time of 2.5 ns
- Complementary OR/NOR outputs with capability for wired-OR connections
- Designed for use with transmission lines to ensure maximum signal transmission without noise. Characterized for 50-ohm lines
- High noise immunity: ±225 mV typical at 25°C

This data sheet covers the arithmetic modules.
Separate data sheets cover the balance of the ECL2500 modules.

ECL2500 series arithmetic modules

The ECL2500 series arithmetic modules are summarized in the table below. These modules contain the multifunction ECL circuits shown in the schematics of Figures A and B. The basic principle of collector dotting and emitter dotting, used in both modules, is the shown in Figure C. Logic diagrams of ECL2515 and ECL2516 are shown on page 4.

SUMMARY OF ARITHMETIC MODULES

MODULE	GATES PER MODULE	INPUTS PER GATE	POSITIVE LOGIC	OUTPUTS OF MODULE
ECL2515 GROUP CARRY	5	1, 2, 3, 4, 5	OR-AND/NOR-OR	Y and Z
ECL2516 FULL SUM-CARRY ADDER	7	2, 2, 2, 3, 3, 3, 3	OR-AND/NOR-OR	Σ, $\overline{\Sigma}$, C_O, and $\overline{C}_O$

schematic

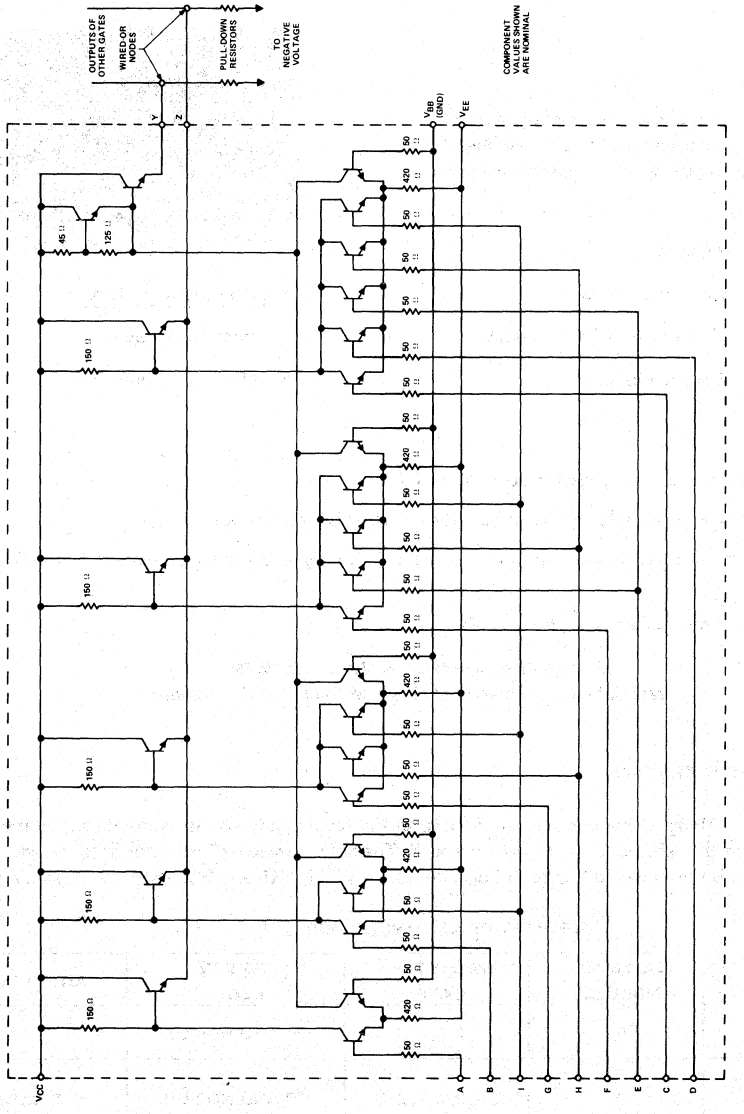


FIGURE A—SCHEMATIC OF ECL2515

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logic

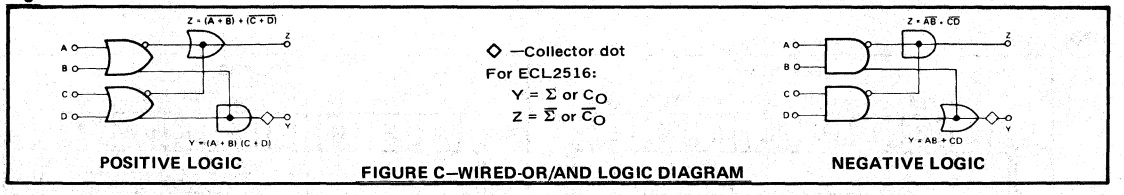


FIGURE C—WIRED-OR/AND LOGIC DIAGRAM

schematic

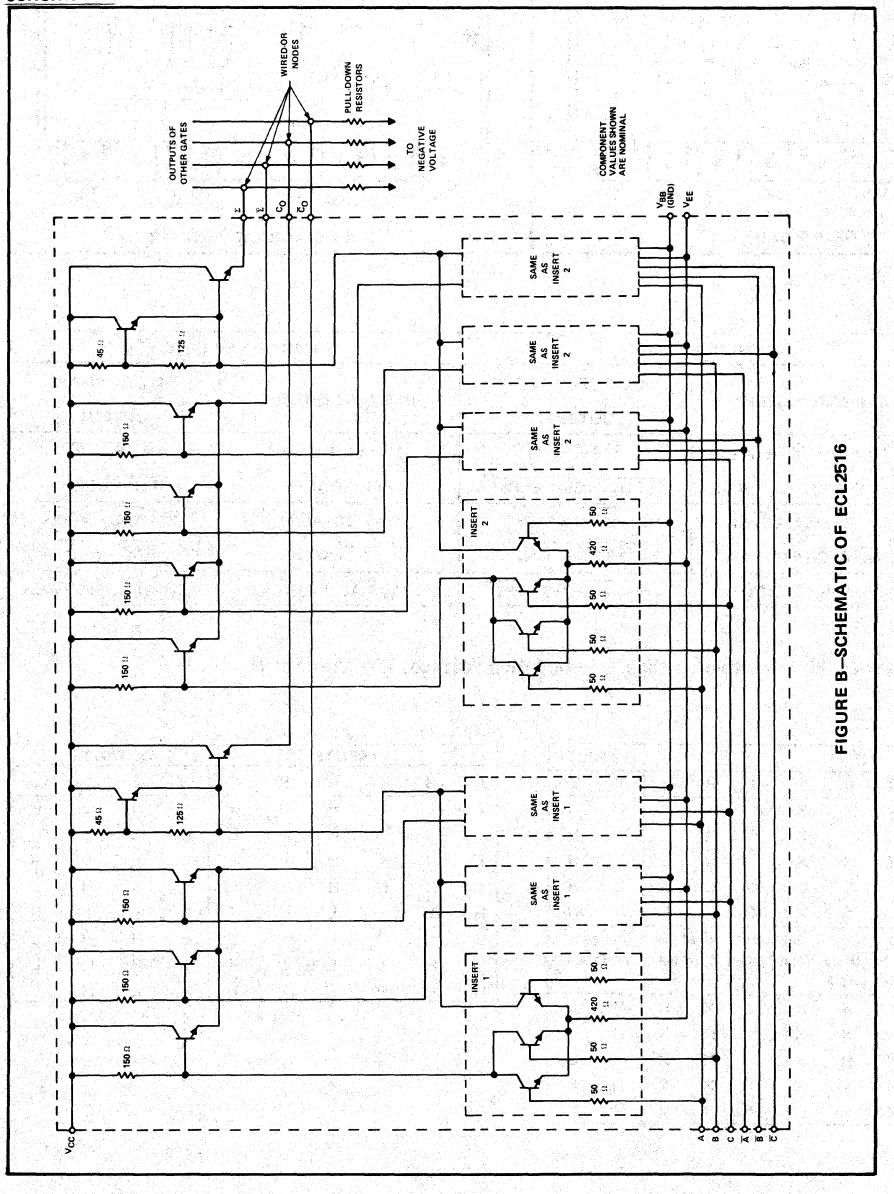


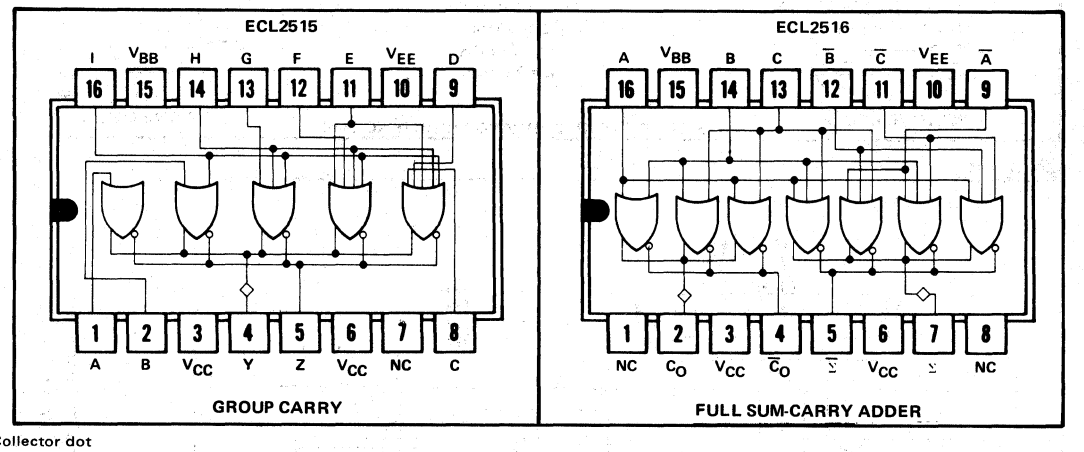
FIGURE B—SCHEMATIC OF ECL2516

Positive logic OR-AND/NOR-OR functions or negative logic AND-OR/NAND-AND functions are provided at the various outputs of ECL2515 and ECL2516 as shown in the logic table.

Emitter-follower outputs require an external pull-down resistor. The wired-OR function can be obtained by connecting emitter-follower outputs of other modules together. Only one pull-down resistor is required for each wired-OR node. Each output of a module can be wired-OR connected independently of the other outputs of the module.

4

logic



◇—Collector dot
NC—No internal connection

MODULE	POSITIVE LOGIC		NEGATIVE LOGIC	
	IN-PHASE OUTPUT	OUT-OF-PHASE OUTPUT	IN-PHASE OUTPUT	OUT-OF-PHASE OUTPUT
ECL2515	$Y = A(B+I)(G+H+I) \cdot (E+F+H+I)(C+D+E+H+I)$	$Z = \bar{A}+\overline{B+I}+\overline{G+H+I}+\overline{E+F+H+I}+\overline{C+D+E+H+I}$	$Y = A+BI+GHI+EFHI+CDEHI$	$Z = \bar{A} \cdot \overline{BI} \cdot \overline{GHI} \cdot \overline{EFHI} \cdot \overline{CDEHI}$
ECL2516	$\Sigma = (A+B+C)(\bar{A}+\bar{B}+C) \cdot (\bar{A}+B+\bar{C})(A+\bar{B}+\bar{C})$	$\bar{\Sigma} = \overline{A+B+C}+\overline{\bar{A}+\bar{B}+C}+\bar{A}+B+\bar{C}+A+\bar{B}+\bar{C}$	$\Sigma = ABC+\bar{A}\bar{B}C+\bar{A}B\bar{C}+A\bar{B}\bar{C}$	$\bar{\Sigma} = \overline{ABC} \cdot \overline{\bar{A}\bar{B}C} \cdot \overline{\bar{A}B\bar{C}} \cdot \overline{A\bar{B}\bar{C}}$
	$C_O = (A+B)(B+C)(A+C)$	$\bar{C}_O = \overline{A+B}+\overline{B+C}+\overline{A+C}$	$C_O = AB+BC+AC$	$\bar{C}_O = \overline{AB} \cdot \overline{BC} \cdot \overline{AC}$

truth tables (for this series, H = positive voltage, L = negative voltage, X = irrelevant)

ECL2515

INPUTS									OUTPUTS	
A	B	C	D	E	F	G	H	I	Y	Z
L	X	X	X	X	X	X	X	X	L	H
X	L	X	X	X	X	X	X	L	L	H
X	X	X	X	X	X	L	L	L	L	H
X	X	X	X	L	L	X	L	L	L	H
X	X	L	L	L	X	X	L	L	L	H
For a LOW Y and HIGH Z, all inputs to at least one gate must be LOW. For a HIGH Y and LOW Z, at least one input of each gate must be HIGH.										
H	X	X	X	X	X	X	X	H	H	L
H	H	X	X	X	X	X	H	X	H	L
H	H	X	X	H	X	H	X	X	H	L
H	H	X	H	X	H	H	X	X	H	L
H	H	H	X	X	H	H	X	X	H	L

ECL2516

INPUTS						OUTPUTS			
A	B	C	Ā	B̄	C̄	Σ	Σ̄	C_O	$\bar{C}_O$
L	L	L	H	H	H	L	H	L	H
L	L	H	H	H	L	H	L	L	H
L	H	L	H	L	H	H	L	L	H
L	H	H	H	L	L	L	H	H	L
H	L	L	L	H	H	H	L	L	H
H	L	H	L	H	L	L	H	H	L
H	H	L	L	L	H	L	H	H	L
H	H	H	L	L	L	H	L	H	L

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absolute maximum ratings (see note 1)

Terminal voltages and currents . . . . . See table below
Storage temperature range . . . . . −40°C to 150°C
Temperature range with supply and bias voltages applied . . . . . −40°C to 100°C

TERMINAL VOLTAGE AND/OR CURRENT, T_A = 0°C TO 75°C (SEE NOTES 2 AND 3)

TERMINAL	REMARKS	VOLTAGE		CURRENT
		CONTINUOUS	20-μs SURGE	
V_{CC}		2 V	4.5 V	
V_{EE}		−4 V	−7 V	
Each Input	All other inputs open	−3.5 V	−4 V	
		2 V	2 V	
Output Y†	All inputs high			−40 mA
Output Z†	All inputs low			−40 mA

†For ECL2516: Y = Σ or C_o, Z = $\overline{\Sigma}$ or $\overline{C}_o$

recommended operating conditions

Supply voltage V_{CC} . . . . . 1.32 V ± 2%
Supply voltage V_{EE} . . . . . −3.2 V ± 2%
Reference voltage V_{BB} . . . . . 0 V (GND)
Reverse bias on unused inputs . . . . . −1 V ± 0.5 V
Normalized d-c fan-out . . . . . 0 to 35
Load on each output . . . . . characterized at 270 Ω to V_{EE}, 50 Ω to GND
Operating free-air temperature range . . . . . 0°C to 75°C

NOTES: 1. Absolute maximum ratings are limits beyond which the life of individual devices may be impaired and are never to be exceeded in service or testing.
2. Maximum terminal conditions must be considered as mutually exclusive.
3. All voltages are referenced to V_{BB}, which is at GND.

ECL2515 electrical characteristics at specified free-air temperature

PARAMETER		TEST FIGURE	TEST CONDITIONS*						MIN	TYP	MAX	UNIT
			TERMINALS (SEE NOTE 4)		INPUT CONDITIONS			T_A	(SEE NOTE 5)			
			INPUTS	OUTPUTS Y Z	INPUT UNDER TEST, V_I	OTHER INPUT(S) OF SAME GATE	REMAINING INPUTS OF OTHER GATES					
V_{IH}	High-level input voltage							0°C	150		720	mV
								25°C	150		720	
								75°C	150		720	
V_{IL}	Low-level input voltage							0°C	−1500		−150	mV
								25°C	−1500		−150	
								75°C	−1500		−150	
$V_{OH(Y)}$	High-level output voltage at Y output	2	1 2, 16 13, 14, 16 11, 12, 14, 16 8, 9, 11, 14, 16	4	0.2 V	−0.5 V	0.5 V	0°C	315	390		mV
								25°C	350	425	500	
								75°C		495	580	
$V_{OL(Y)}$	Low-level output voltage at Y output	2	Same as for $V_{OH(Y)}$ above		−0.2 V	−0.5 V	0.5 V	0°C	−505	−450		mV
								25°C	−490	−410	−350	
								75°C		−290	−230	
$V_{OH(Z)}$	High-level output voltage at Z output	2	1 2, 16 13, 14, 16 11, 12, 14, 16 8, 9, 11, 14, 16	5	−0.2 V	−0.5 V	0.5 V	0°C	315	390		mV
								25°C	350	425	500	
								75°C		495	580	
$V_{OL(Z)}$	Low-level output voltage at Z output	2	Same as for $V_{OH(Z)}$ above		0.2 V	−0.5 V	See Note 6	0°C		−385		mV
								25°C	−440	−365	−310	
								75°C		−325	−280	
$V_{OL(Z)}$	Low-level output voltage at Z output	2	Same as for $V_{OH(Z)}$ above		0.4 V	−0.5 V	See Note 6	0°C	−505	−455		mV
								25°C	−490	−425		
								75°C		−380	−315	
$V_{OH(Z)}$	High-level output voltage at Z output	2	Same as for $V_{OH(Z)}$ above		All inputs of all gates in parallel at −0.5 V			0°C				mV
								25°C			625	
								75°C			695	
$V_{OH(Y)}$	High-level output voltage at Y output	2	1	4	0.15 V	−0.5 V	0.5 V	0°C	290			mV
								25°C	325			
								75°C				
$V_{OL(Y)}$	Low-level output voltage at Y output	2	1	4	−0.15 V	−0.5 V	0.5 V	0°C				mV
								25°C			−335	
								75°C			−215	
I_{IH}	High-level input current (each input)	3	1, 2, 8, 9, 12, 13 11, 14, 16 See Note 7		0.5 V	−0.5 V	−0.5 V	0°C			255	μA
								25°C			235	
								75°C			200	
I_{IL}	Low-level input current (all inputs)	4	1, 2, 8, 9, 11, 12, 13, 14, 16		All inputs of all gates in parallel at −3.2 V			0°C			−0.8	μA
								25°C			−1	
								75°C			−1.5	
I_{CC} or $-I_{EE}$	Supply current	5			All inputs of all gates in parallel at −0.5 V			25°C	20		36	mA
C_{in}	Input capacitance (see Note 8)							25°C		5		pF
z_{out}	Output impedance (see Note 9)			4 5				25°C		5		Ω

*V_{BB} (pin 15) = GND, V_{CC} (pins 3 and 6) = 1.32 V ±1%, V_{EE} (pin 10) = −3.20 V ±1%.

NOTES:
4. Each gate is tested separately unless otherwise noted. See referenced test figure for output termination. Gates not under test have their outputs terminated in the same manner, and power applied.
5. The algebraic convention where the most positive limit is designated as maximum is used in this data sheet for logic voltage levels only, e.g., if −350 mV is a maximum, the typical and minimum limits are more negative voltages.
6. One input of each gate must be at V_I. Other inputs are biased to −0.5 V.
7. Terminals 11, 14, and 16 are internally connected to 2, 3, and 4 gates respectively, and maximum I_{IH} for these terminals at each temperature can be determined by multiplying the value given for I_{IH} by 2, 3, or 4 respectively.
8. C_{in} is measured using peak-current techniques. A square-wave input pulse is applied, and the input current waveform is integrated with respect to time to determine Q. C_{in} = Q/V. When a terminal is an input to more than one gate, multiply the value given by the number of gates to which this terminal is an input.
9. Constant-current loads are used to determine the output impedance which is derived from the slope of a V_O vs I_O curve.

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ECL2516 electrical characteristics at specified free-air temperature†

PARAMETER		TEST FIGURE	TEST CONDITIONS* TERMINALS (SEE NOTE 4) INPUTS	OUTPUTS Y	OUTPUTS Z	INPUT CONDITIONS: INPUT UNDER TEST, V_I	OTHER INPUT(S) OF SAME GATE	REMAINING INPUTS OF OTHER GATES	T_A	MIN (SEE NOTE 5)	TYP (SEE NOTE 5)	MAX (SEE NOTE 5)	UNIT
V_{IH}	High-level input voltage								0°C 25°C 75°C	150 150 150		720 720 720	mV
V_{IL}	Low-level input voltage								0°C 25°C 75°C	−1500 −1500 −1500		−150 −150 −150	mV
$V_{OH(Y)}$	High-level output voltage at Y output	2	16, 14 14, 13 16, 13 16, 14, 13 9, 12, 13 9, 14, 11 16, 12, 11	2 7 		0.2 V	−0.5 V	0.5 V	0°C 25°C 75°C	315 350	390 425 495	 500 580	mV
$V_{OL(Y)}$	Low-level output voltage at Y output	2	Same as for $V_{OH(Y)}$ above			−0.2 V	−0.5 V	0.5 V	0°C 25°C 75°C	−505 −490	−450 −410 −290	 −350 −230	mV
$V_{OH(Z)}$	High-level output voltage at Z output	2	16, 14 14, 13 16, 13 16, 14, 13 9, 12, 13 9, 14, 11 16, 12, 11		4 5 	−0.2 V	−0.5 V	0.5 V	0°C 25°C 75°C	315 350	390 425 495	 500 580	mV
$V_{OL(Z)}$	Low-level output voltage at Z output	2	Same as for $V_{OH(Z)}$ above			0.2 V	−0.5 V	See Note 6	0°C 25°C 75°C	 −440	−385 −365 −325	 −310 −280	mV
$V_{OL(Z)}$	Low-level output voltage at Z output	2	Same as for $V_{OH(Z)}$ above			0.4 V	−0.5 V	See Note 6	0°C 25°C 75°C	−505 −490	−455 −425 −380	 −315	mV
$V_{OH(Z)}$	High-level output voltage at Z output	2	16, 14 14, 13 16, 13 16, 14, 13 9, 12, 13 9, 14, 11 16, 12, 11		4 5 	All inputs of all gates in parallel at −0.5 V			0°C 25°C 75°C 0°C 25°C 75°C			600 670 615 685	mV
$V_{OH(Y)}$	High-level output voltage at Y output	2	13	7		0.15 V	−0.5 V	0.5 V	0°C 25°C 75°C	290 325		 	mV
$V_{OL(Y)}$	Low-level output voltage at Y output	2	13	7		−0.15 V	−0.5 V	0.5 V	0°C 25°C 75°C			 −335 −215	mV
I_{IH}	High-level input current (each input)	3	9 11 12 13 14 16			0.5 V	−0.5 V	−0.5 V	0°C 25°C 75°C 0°C 25°C 75°C			510 470 400 1020 940 800	μA μA
I_{IL}	Low-level input current (all inputs)	4	9, 11, 12, 13, 14, 16			All inputs of all gates in parallel at −3.2 V			0°C 25°C 75°C			−0.9 −1.2 −1.8	μA
I_{CC} or $-I_{EE}$	Supply current	5				All inputs of all gates in parallel at −0.5 V			25°C	30		45	mA
C_{in}	Input capacitance (see Note 8)								25°C		5		pF
z_{out}	Output impedance (see Note 9)								25°C		5		Ω

*V_{BB} (pin 15) = GND, V_{CC} (pins 3 and 6) = 1.32 V ± 1%, V_{EE} (pin 10) = −3.20 V ± 1%.
†Y = Σ or C_O; Z = $\overline{\Sigma}$ or $\overline{C}_O$.

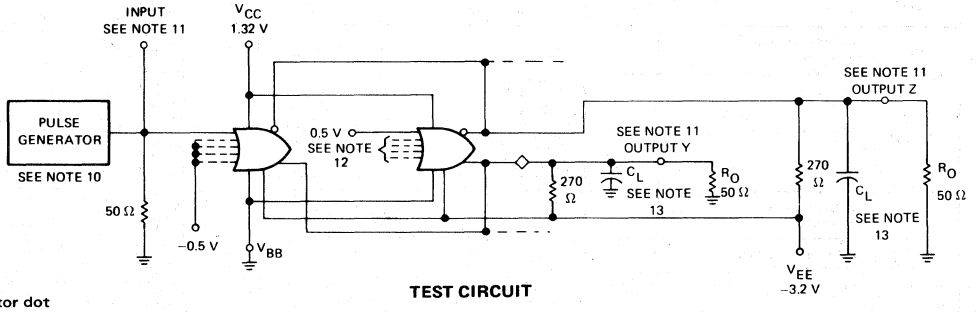
NOTES:
4. Each gate is tested separately unless otherwise noted. See referenced test figure for output termination. Gates not under test have their outputs terminated in the same manner, and power applied.
5. The algebraic convention where the most positive limit is designated as maximum is used in this data sheet for logic voltage levels only, e.g., if −350 mV is a maximum, the typical and minimum limits are more negative voltages.
6. One input of each gate must be at V_I. Other inputs are biased to −0.5 V.
8. C_{in} is measured using peak-current techniques. A square-wave input pulse is applied, and the input current waveform is integrated with respect to time to determine Q. C_{in} = Q/V. When a terminal is an input to more than one gate, multiply the value given by the number of gates to which this terminal is an input.
9. Constant-current loads are used to determine the output impedance which is derived from the slope of a V_O vs I_O curve.

operating characteristics at specified free-air temperature (see figure 1)

PARAMETER		C_L	T_A	ECL2515 EITHER OUTPUT			ECL2516 ANY OUTPUT			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Propagation delay time, high-to-low level output and/or	4 pF	0°C		2.6			2.6		
			25°C	1.5	2.6	4.1	1.5	2.6	4.1	ns
			75°C		2.6			2.6		
t_{PLH}	Propagation delay time low-to-high-level output	50 pF	0°C		3.5			3.5		
			25°C	2.4	3.5	4.8	2.4	3.5	4.8	ns
			75°C		3.5			3.5		
t_{THL}	Transition time, high-to-low-level output and/or	4 pF	0°C		4.0			4.0		
			25°C	1.6	4.0	6.6	1.6	4.0	6.6	ns
			75°C		4.1			4.1		
t_{TLH}	Transition time, low-to-high-level output	50 pF	0°C		4.7			4.7		
			25°C	1.9	4.6	6.9	1.9	4.6	6.9	ns
			75°C		4.4			4.4		

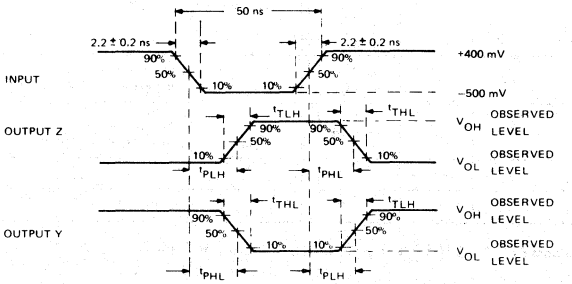
4

PARAMETER MEASUREMENT INFORMATION†



◇—Collector dot

TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 1–PROPAGATION DELAY AND TRANSITION TIMES

†For ECL2516: Y = Σ or C_O; Z = $\overline{\Sigma}$ or $\overline{C}_O$.

NOTES: 10. The generator has the following characteristics: Z_{out} = 50 Ω, PRR = 1 MHz.

11. The waveforms are monitored on an oscilloscope with a rise time of less than or equal to 350 ps. Either a high-impedance probe with an input impedance of 100 kΩ paralleled by 2 pF, or a 50-Ω impedance system can be used. The 50-Ω resistors designated R_O are the oscilloscope input resistance in the 50-Ω system or discrete resistors with a high-impedance probe.

12. This test circuit shows only the principle of measuring propagation delay times and transition times; i.e., no internal connection of the input terminals is shown. See Table I for ECL2515 or Table II for ECL2516 for voltages to be applied to input terminals for each test.

13. C_L includes probe and fixture capacitance. A capacitance of 50 pF can be used to approximate an a-c fan-out of 10.

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PARAMETER MEASUREMENT INFORMATION

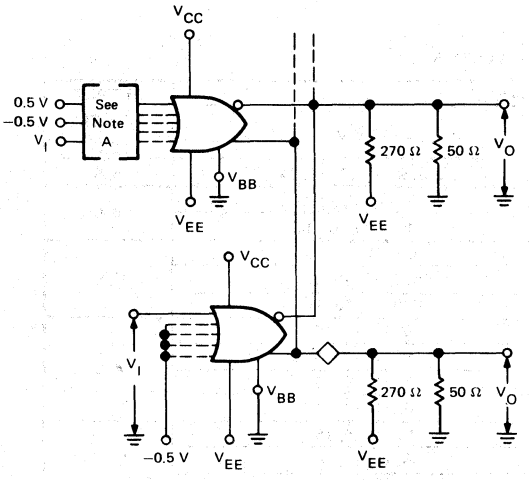
TEST TABLE I—ECL2515

INPUT TERMINAL CONDITIONS			OUTPUT UNDER TEST
PULSE GENERATOR	0.5 V	–0.5 V	
1	16	2, 8, 9, 11, 12, 13, 14	4, 5
2	1, 14	8, 9, 11, 12, 13, 16	4, 5
16		2, 8, 9, 11, 12, 13	
13	1, 2, 11	8, 9, 12, 14, 16	4, 5
14		8, 9, 12, 13, 16	
16		8, 9, 12, 13, 14	
11	1, 2, 9, 13	8, 12, 14, 16	4, 5
12		8, 11, 14, 16	
14		8, 11, 12, 16	
16		8, 11, 12, 14	
8	1, 2, 12, 13	9, 11, 14, 16	4, 5
9		8, 11, 14, 16	
11		8, 9, 14, 16	
14		8, 9, 11, 16	
16		8, 9, 11, 14	

TEST TABLE II—ECL2516

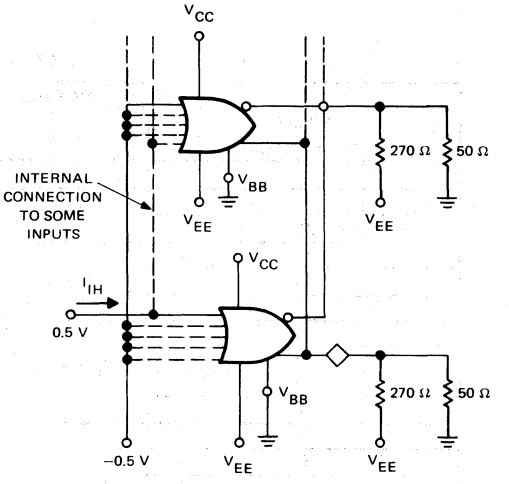
INPUT TERMINAL CONDITIONS			OUTPUT UNDER TEST
PULSE GENERATOR	0.5 V	–0.5 V	
16	11, 13	9, 12, 14	2, 4
14		9, 12, 16	
14	9, 16	11, 12, 13	2, 4
13		11, 12, 14	
16	12, 14	9, 11, 13	2, 4
13		9, 11, 16	
16	9, 11	12, 13, 14	7, 5
14		12, 13, 16	
13		12, 14, 16	
9	14, 16	11, 12, 13	7, 5
12		9, 11, 13	
13		9, 11, 12	
9	12, 13	11, 14, 16	7, 5
14		9, 11, 16	
11		9, 14, 16	
16	9, 14	11, 12, 13	7, 5
12		11, 13, 16	
11		12, 13, 16	

PARAMETER MEASUREMENT INFORMATION†



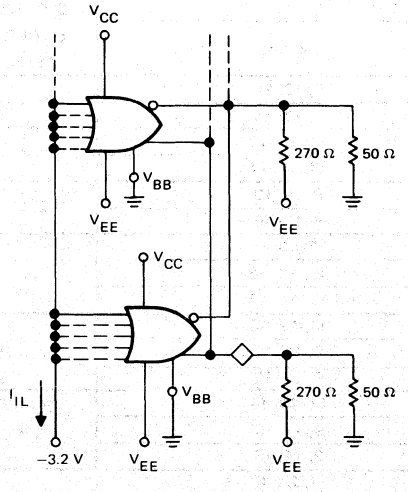
A. The particular input voltages for each module are shown in the electrical characteristics tables.
B. V_I is applied to each input separately except where Note 6 applies.
C. Each output is tested separately.

FIGURE 2–V_{OH} and V_{OL}



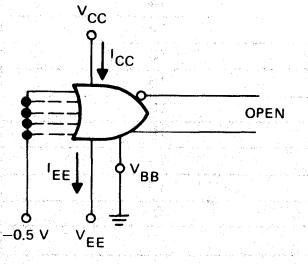
Each input is tested separately.

FIGURE 3–I_{IH}



All inputs of all gates are connected in parallel.

FIGURE 4–I_{IL}



A. All gates are tested simultaneously.
B. I_{CC} is the total current into all V_{CC} terminals.

FIGURE 5–I_{CC} or I_{EE}

◇—Collector dot

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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APPLICATION INFORMATION

ECL2515

The ECL2515 module is designed to provide the logic function for carry look-ahead in high-speed binary adders. In carry look-ahead, bit positions for binary numbers added together produce "generate" terms and "propagate" terms for the carry and sum logic equations.

The ECL2515 produces a "generate" term for 5 bits in one level of logic with a typical propagation delay of 3.0 nanoseconds with a fan-out of 4.

ECL2516

The ECL2516 is a full adder for two binary bits and carry-in that produces a sum and carry-out. The binary bits and their complements, along with carry-in and its complement, are required as inputs.

The sum and its complement and the carry-out and its complement are both produced in one level of logic with a typical propagation delay of 3.0 nanoseconds with a fan-out of 4.

general

Multiple V_{CC} terminals have been supplied to reduce crosstalk noise. All V_{CC} terminals should be connected even if all gates in a module are not used.

Applications of the arithmetic modules at other than data sheet conditions are covered in a separate ECL2500 series application document.

General loading for fan-out may be divided into two classes:

CLASS I **Short-Line or Cluster Loading.**
Loads which can be connected within two inches of any source can be treated as lumped capacitive loads which include the gate inputs and stub-line capacitances. Switching times can be interpolated accordingly. No two dotted outputs can be more than two inches apart for this case.

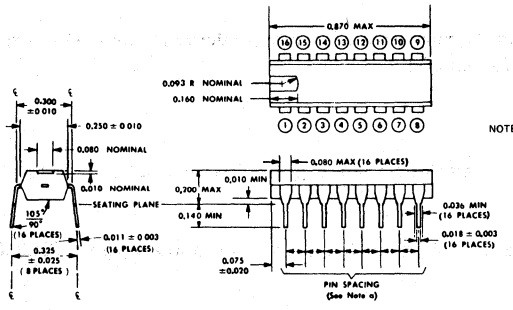
CLASS II **Long-Line or Distributive Loading.**
These loads must be treated as lumped loads along a transmission line and termination should be at the end of the transmission chain. No more than 20 pF of load is recommended per 4.5 inches of 50-ohm printed line (with dielectric constant of 4.5) in order that the reflection coefficient be no greater than 20%. If the loads are lumped loads of 20 pF, they must be 4.5 inches apart. If individual gates and **CLASS I** loads are distributed, they must not exceed the 20 pF per 4.5 inches of line.

mechanical data

The circuit bars are mounted on a 16-lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperatures with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. This package is intended for insertion in mounting-hole rows on 0.300-inch centers. Once the leads are compressed to 0.300-inch separation and inserted, sufficient tension is provided to secure the package in the board during soldering. Silver-plated leads require no additional cleaning or processing when used in soldered assembly.

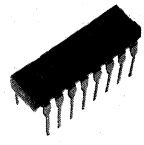
The plastic case is electrically nonconductive.

16-PIN PLASTIC DUAL-IN-LINE PACKAGE OUTLINE



NOTES: a. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within 0.010 of its true longitudinal position relative to pins 1 and 16.

b. All dimensions are in inches unless otherwise noted.



terminal designations

Pin assignments are shown in the table below and correspond to logic diagrams on page 4.
Outputs are denoted by Y and Z for ECL2515 and by Σ, $\overline{\Sigma}$, C_O, and $\overline{C}_O$ for ECL2516.
Inputs are denoted by A through I for ECL2515 and by A, B, C, $\overline{A}$, $\overline{B}$, and $\overline{C}$ for ECL2516.
Power is supplied via the V_{CC}, V_{EE}, and V_{BB} terminals.
V_{BB} is a reference voltage.
NC indicates no internal connection.

PIN ASSIGNMENTS

PIN	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
ECL2515	A	B	V_{CC}	Y	Z	V_{CC}	NC	C	D	V_{EE}	E	F	G	H	V_{BB}	I
ECL2516	NC	C_O	V_{CC}	$\overline{C}_O$	$\overline{\Sigma}$	V_{CC}	Σ	NC	$\overline{A}$	V_{EE}	$\overline{C}$	$\overline{B}$	C	B	V_{BB}	A

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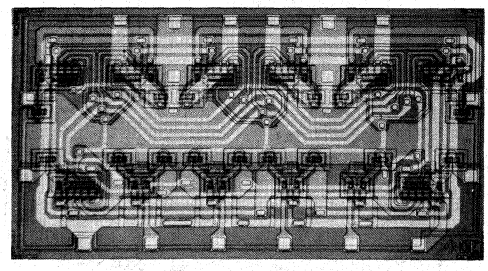
ECL2500 SERIES EMITTER-COUPLED-LOGIC (ECL) DECODER MODULE FOR APPLICATION IN ULTRA-HIGH-SPEED DIGITAL SYSTEMS



description

The ECL2500 series is a compatible family of ECL functions with basic gate delays of 2 to 3 ns per stage. The family is specifically designed for operation from 0°C to 75°C.

The ECL2500 family includes:

- Basic Gate Modules
- **Multifunction Gate Modules**
- Bistable Modules
- Arithmetic Modules
- Interface Modules
- Memory Module

family features

- High speed. . .typical gate propagation delay time of 2.5 ns
- Complementary OR/NOR outputs with capability for wired-OR connections
- Designed for use with transmission lines to ensure maximum signal transmission without noise. Characterized for 50-ohm lines
- High noise immunity: ± 225 mV typical at 25°C

This data sheet covers the decoder module. Separate data sheets cover the balance of the ECL2500 modules.

ECL2500 series 3-bit-to-8-line decoder with enable

The ECL2500 series decoder module is summarized in the table below. The schematic diagram of this module is shown in Figure A.

SUMMARY OF DECODER MODULE

MODULE	GATES PER MODULE	INPUTS PER MODULE	OUTPUTS PER MODULE
ECL2517	12 (4 input, 8 output)	4 (3 bits plus enable)	8 (1 per output gate)

CIRCUIT TYPE ECL2517
EMITTER-COUPLED-LOGIC DECODER

schematic

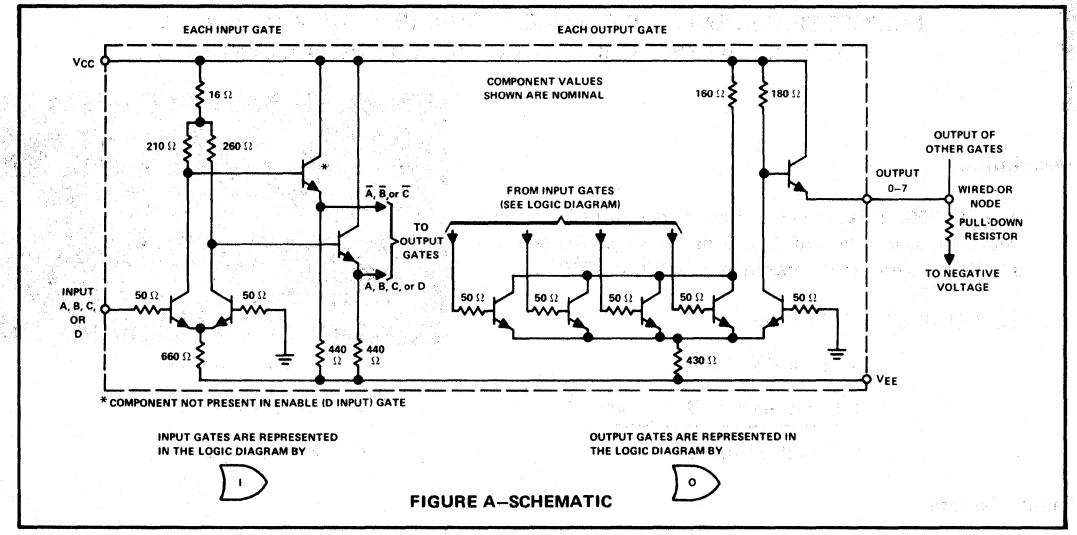


FIGURE A–SCHEMATIC

Emitter-follower outputs require external pull-down resistors. The wired-OR function can be obtained by connecting emitter-follower outputs of other gates to any of the outputs. Only one pull-down resistor is required for each wired-OR node.

absolute maximum ratings (see note 1)

Terminal voltages and currents	See table below
Storage temperature range	−40°C to 150°C
Temperature range with supply and bias voltage applied	−40°C to 100°C

TERMINAL VOLTAGE AND/OR CURRENT, T_A = 0°C TO 75°C (SEE NOTES 2 AND 3)

TERMINAL	REMARKS	VOLTAGE		CURRENT
		CONTINUOUS	20-μs SURGE	
V_{CC}		2 V	4.5 V	
V_{EE}		−4 V	−7 V	
Each Input	All other inputs open	−3.5 V	−4 V	
		2 V	2 V	
Any output	All inputs high			−40 mA

recommended operating conditions

Supply voltage V_{CC}	1.32 V ± 2%
Supply voltage V_{EE}	−3.2 V ± 2%
Reference voltage V_{BB}	0 V (GND)
Reverse bias on unused inputs	−1 V ± 0.5 V
Normalized d-c fan-out	0 to 35
Load on each output	characterized at 270 Ω to V_{EE}, 50 Ω to GND
Operating free-air temperature range	0°C to 75°C

NOTES: 1. Absolute maximum ratings are limits beyond which the life of individual devices may be impaired and are never to be exceeded in service or testing.
2. Maximum terminal conditions must be considered as mutually exclusive.
3. All voltages are referenced to V_{BB}, which is at GND.

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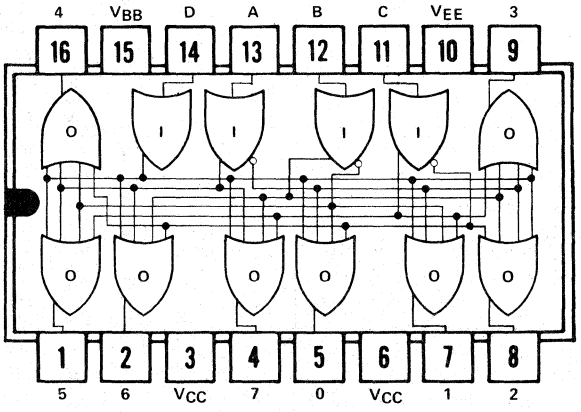
logic



OUTPUT LINE	POSITIVE LOGIC	NEGATIVE LOGIC
0	$\bar{A}+\bar{B}+\bar{C}+D$	$\bar{A}\bar{B}\bar{C}D$
1	$\bar{A}+\bar{B}+C+D$	$\bar{A}\bar{B}CD$
2	$\bar{A}+B+\bar{C}+D$	$\bar{A}B\bar{C}D$
3	$\bar{A}+B+C+D$	$\bar{A}BCD$
4	$A+\bar{B}+\bar{C}+D$	$A\bar{B}\bar{C}D$
5	$A+\bar{B}+C+D$	$A\bar{B}CD$
6	$A+B+\bar{C}+D$	$AB\bar{C}D$
7	$A+B+C+D$	$ABCD$

INPUT GATE

OUTPUT GATE

truth table (for this module, H = positive voltage, L = negative voltage, X = irrelevant)

INPUTS				OUTPUT LINES							
A	B	C	D	0	1	2	3	4	5	6	7
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	H	H	L
L	L	H	L	H	H	H	H	H	H	L	H
L	H	L	L	H	H	H	H	H	L	H	H
L	H	H	L	H	H	H	H	L	H	H	H
H	L	L	L	H	H	H	L	H	H	H	H
H	L	H	L	H	H	L	H	H	H	H	H
H	H	L	L	H	L	H	H	H	H	H	H
H	H	H	L	L	H	H	H	H	H	H	H

CIRCUIT TYPE ECL2517
EMITTER-COUPLED-LOGIC DECODER

electrical characteristics at specified free-air temperature*

PARAMETER		TEST FIGURE	INPUT CONDITIONS TERMINAL 13 $V_{I(A)}$	12 $V_{I(B)}$	11 $V_{I(C)}$	14 $V_{I(D)}$	OUTPUT TERMINAL	T_A	MIN (SEE NOTE 4)	TYP (SEE NOTE 4)	MAX (SEE NOTE 4)	UNIT
V_{IH}	High-level input voltage							0°C	150		720	mV
								25°C	150		720	
								75°C	150		720	
V_{IL}	Low-level input voltage							0°C	−1500		−150	mV
								25°C	−1500		−150	
								75°C	−1500		−150	
$V_{OH(0)}$	High-level output voltage at line 0	1	0.5 V	0.5 V	0.5 V	0.2 V	5	0°C	290	365		mV
								25°C	325	400	500	
								75°C		470	570	
$V_{OL(0)}$	Low-level output voltage at line 0	1	0.5 V	0.5 V	0.5 V	−0.2 V	5	0°C	−505	−445		mV
								25°C	−490	−425	−350	
								75°C		−385	−310	
$V_{OH(1)}$	High-level output voltage at line 1	1	0.5 V	−0.2 V	−0.5 V	−0.5 V	7	0°C	290	365		mV
								25°C	325	400	500	
								75°C		470	570	
$V_{OL(1)}$	Low-level output voltage at line 1	1	0.5 V	0.2 V	−0.5 V	−0.5 V	7	0°C	−505	−445		mV
								25°C	−490	−425	−350	
								75°C		−385	−310	
$V_{OH(2)}$	High-level output voltage at line 2	1	0.5 V	0.2 V	0.5 V	−0.5 V	8	0°C	290	365		mV
								25°C	325	400	500	
								75°C		470	570	
$V_{OL(2)}$	Low-level output voltage at line 2	1	0.5 V	−0.2 V	0.5 V	−0.5 V	8	0°C	−505	−445		mV
								25°C	−490	−425	−350	
								75°C		−385	−310	
$V_{OH(3)}$	High-level output voltage at line 3	1	−0.2 V	−0.5 V	−0.5 V	−0.5 V	9	0°C	290	365		mV
								25°C	325	400	500	
								75°C		470	570	
$V_{OL(3)}$	Low-level output voltage at line 3	1	0.2 V	−0.5 V	−0.5 V	−0.5 V	9	0°C	−505	−445		mV
								25°C	−490	−425	−350	
								75°C		−385	−310	
$V_{OH(4)}$	High-level output voltage at line 4	1	0.2 V	0.5 V	0.5 V	−0.5 V	16	0°C	290	365		mV
								25°C	325	400	500	
								75°C		470	570	
$V_{OL(4)}$	Low-level output voltage at line 4	1	−0.2 V	0.5 V	0.5 V	−0.5 V	16	0°C	−505	−445		mV
								25°C	−490	−425	−350	
								75°C		−385	−310	
$V_{OH(5)}$	High-level output voltage at line 5	1	−0.5 V	0.5 V	0.2 V	−0.5 V	1	0°C	290	365		mV
								25°C	325	400	500	
								75°C		470	570	
$V_{OL(5)}$	Low-level output voltage at line 5	1	−0.5 V	0.5 V	−0.2 V	−0.5 V	1	0°C	−505	−445		mV
								25°C	−490	−425	−350	
								75°C		−385	−310	
$V_{OH(6)}$	High-level output voltage at line 6	1	−0.5 V	−0.5 V	−0.2 V	−0.5 V	2	0°C	290	365		mV
								25°C	325	400	500	
								75°C		470	570	
$V_{OL(6)}$	Low-level output voltage at line 6	1	−0.5 V	−0.5 V	0.2 V	−0.5 V	2	0°C	−505	−445		mV
								25°C	−490	−425	−350	
								75°C		−385	−310	
V_{OH}	High-level output voltage at all lines	1	−0.5 V	−0.5 V	−0.5 V	0.15 V	1, 2, 4, 5, 7, 8, 9, 16	0°C	290	365		mV
								25°C	325	400	500	
								75°C		470	570	
$V_{OL(7)}$	Low-level output voltage at line 7	1	−0.5 V	−0.5 V	−0.5 V	−0.15 V	4	0°C	−505	−445		mV
								25°C	−490	−425	−350	
								75°C		−385	−310	
I_{IH}	High-level input current	2	Input under test at 0.5 V, other inputs at −0.5 V					0°C			165	μA
								25°C			150	
								75°C			125	
I_{IL}	Low-level input current (all inputs)	3	All inputs in parallel at −3.2 V					0°C			−0.5	μA
								25°C			−0.5	
								75°C			−0.5	
I_{CC} or $-I_{EE}$	Supply current	4	All inputs in parallel at −0.5 V					25°C	84		133	mA
C_{in}	Input capacitance (see Note 5)							25°C		5		pF
z_{out}	Output impedance (see Note 6)							25°C		5		Ω

*V_{BB} (pin 15) = GND, V_{CC} (pin 3 and pin 6) = 1.32 V ± 1%, V_{EE} (pin 10) = −3.20 V ± 1%.

NOTES: 4. The algebraic convention where the most positive limit is designated as maximum is used in this data sheet for logic voltage levels only, e.g., if −350 mV is a maximum, the typical and minimum limits are more negative voltages.

5. C_{in} is measured using peak-current techniques. A square-wave input pulse is applied, and the input current waveform is integrated with respect to time to determine Q. $C_{in} = Q/V$.

6. Constant-current loads are used to determine the output impedance which is derived from the slope of a V_O vs I_O curve.

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operating characteristics at specified free-air temperature (see figure 5)

TERMINALS TO BE TESTED (SEE NOTE 7)		C_L	t_{PHL} and/or t_{PLH} PROPAGATION TIMES–ns									t_{THL} and/or t_{TLH} TRANSITION TIMES–ns								
			$T_A = 0°C$			$T_A = 25°C$			$T_A = 75°C$			$T_A = 0°C$			$T_A = 25°C$			$T_A = 75°C$		
INPUT	OUTPUT	pF	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
14	5	4		4.8		3	4.8	6.6		5.0			3.6		2.3	3.7	5.5		3.6	
14	7																			
14	8																			
14	9																			
14	16																			
14	1																			
14	2																			
14	4																			
14	5	50		5.9		3.9	5.8	7.7		5.8			4.5		2.5	4.3	6.5		4.2	
14	7																			
14	8																			
14	9																			
14	16																			
14	1																			
14	2																			
14	4																			

NOTE: 7. The eight combinations of voltages at input terminals A, B, and C shown in the table of Figure 5, are applied sequentially. With each combination of input voltages, the enable input, D, is pulsed from the high level to the low level to give a low-level output at the particular output line shown in the table. The input pulse is measured as it is applied with each combination of input voltages and a waveform measurement is made at the corresponding output.

GENERAL APPLICATION INFORMATION

Multiple V_{CC} terminals have been supplied to reduce crosstalk noise. All V_{CC} terminals should be connected.

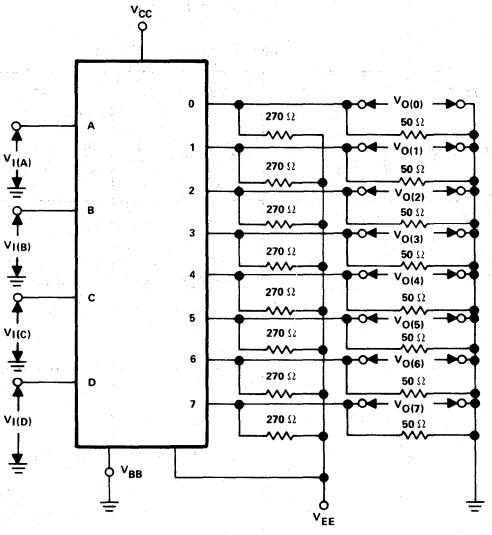
Applications of the ECL2517 decoder module at other than data sheet conditions are covered in a separate ECL2500 series application document.

General loading for fan-out may be divided into two classes:

CLASS I **Short-Line or Cluster Loading.**
Loads which can be connected within two inches of any source can be treated as lumped capacitive loads which include the gate inputs and stub-line capacitances. Switching times can be interpolated accordingly. No two dotted outputs can be more than two inches apart for this case.

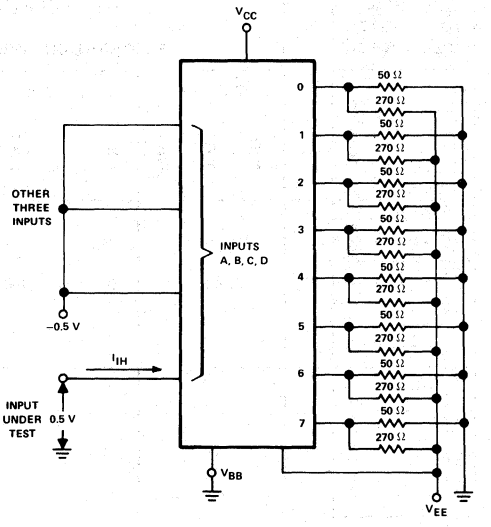
CLASS II **Long-Line or Distributive Loading.**
These loads must be treated as lumped loads along a transmission line and termination should be at the end of the transmission chain. No more than 20 pF of load is recommended per 4.5 inches of 50-ohm printed line (with dielectric constant of 4.5) in order that the reflection coefficient be no greater than 20%. If the loads are lumped loads of 20 pF, they must be 4.5 inches apart. If individual gates and **CLASS I** loads are distributed, they must not exceed the 20 pF per 4.5 inches of line.

PARAMETER MEASUREMENT INFORMATION†



V_I is applied to each input as specified in the electrical characteristics table.

FIGURE 1–V_{OH} AND V_{OL}



Each input is tested separately.

FIGURE 2–I_{IH}

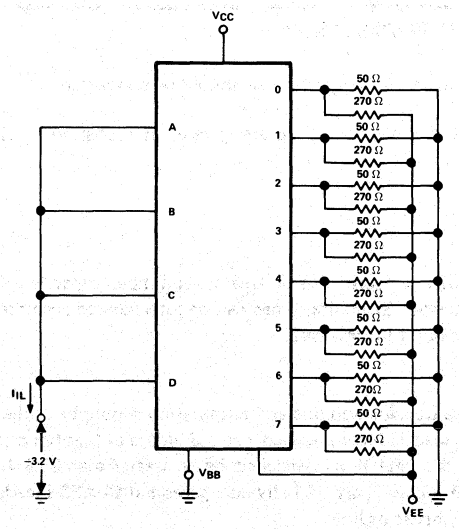
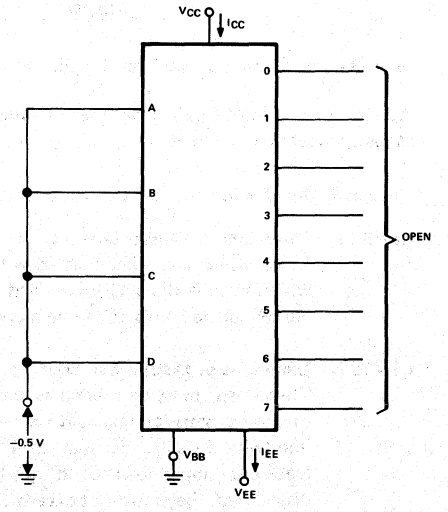


FIGURE 3–I_{IL}



I_{CC} is the total current into both V_{CC} terminals.

FIGURE 4–I_{CC} OR I_{EE}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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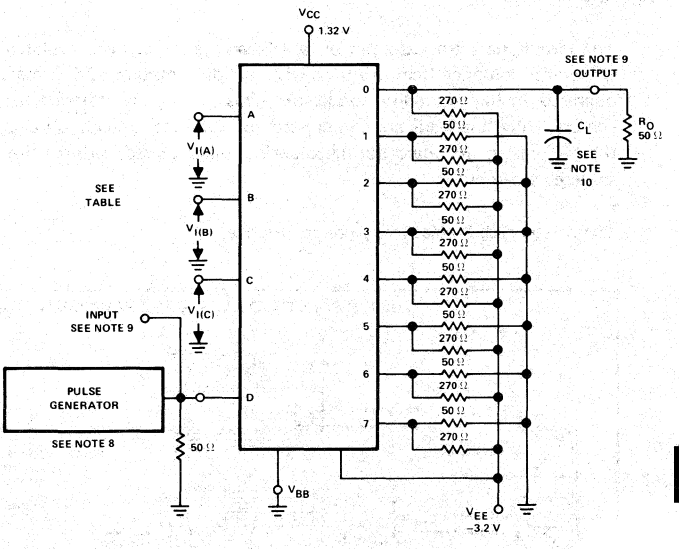
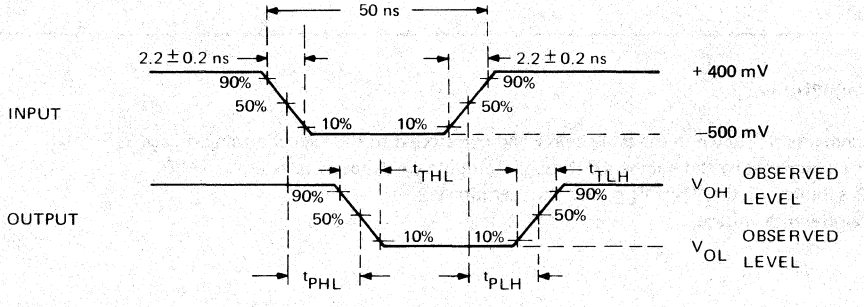
PARAMETER MEASUREMENT INFORMATION

INPUT TERMINAL			OUTPUT UNDER TEST	
13	12	11		
$V_{I(A)}$	$V_{I(B)}$	$V_{I(C)}$	LINE	TERMINAL
0.5 V	0.5 V	0.5 V	0	5
0.5 V	0.5 V	−0.5 V	1	7
0.5 V	−0.5 V	0.5 V	2	8
0.5 V	−0.5 V	−0.5 V	3	9
−0.5 V	0.5 V	0.5 V	4	16
−0.5 V	0.5 V	−0.5 V	5	1
−0.5 V	−0.5 V	0.5 V	6	2
−0.5 V	−0.5 V	−0.5 V	7	4

SEE NOTE 7



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 5–PROPAGATION DELAY AND TRANSITION TIMES

NOTES:
7. The eight combinations of voltages at input terminals A, B, and C shown in the table of Figure 5, are applied sequentially. With each combination of input voltages, the enable input, D, is pulsed from the high level to the low level to give a low-level output at the particular output line shown in the table. The input pulse is measured as it is applied with each combination of input voltages and a waveform measurement is made at the corresponding output.
8. The generator has the following characteristics: Z_{out} = 50 Ω, PRR = 1 MHz.
9. The waveforms are monitored on an oscilloscope with a rise time of less than or equal to 350 ps. Either a high-impedance probe with an input impedance of 100 kΩ paralleled by 2 pF, or a 50-Ω impedance system can be used. The 50-Ω resistor designated R_O is the oscilloscope input resistance in the 50-Ω system or a discrete resistor with a high-impedance probe.
10. C_L includes probe and fixture capacitance. A capacitance of 50 pF can be used to approximate an a-c fan-out of 10.

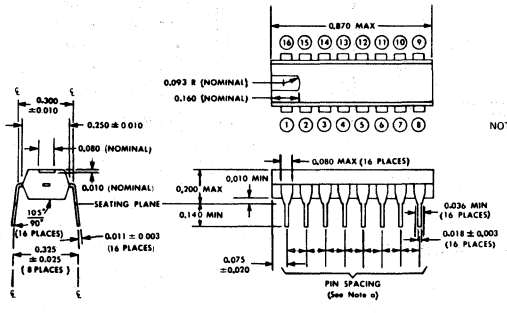
CIRCUIT TYPE ECL2517
EMITTER-COUPLED-LOGIC DECODER

mechanical data

The circuit bars are mounted on a 16-lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperatures with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. This package is intended for insertion in mounting-hole rows on 0.300-inch centers. Once the leads are compressed to 0.300-inch separation and inserted, sufficient tension is provided to secure the package in the board during soldering. Silver-plated leads require no additional cleaning or processing when used in soldered assembly.

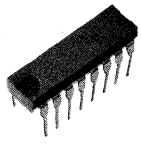
The plastic case is electrically nonconductive.

16-PIN PLASTIC DUAL-IN-LINE PACKAGE OUTLINE



NOTES: a. The true-position pin spacing is 0.100 between center lines. Each pin centerline is located within 0.010 of its true longitudinal position relative to pins 1 and 16.

b. All dimensions are in inches unless otherwise noted.



terminal designations

Pin assignments are shown in the table below and correspond to the logic diagram on page 3.
Outputs are denoted by the numbers 0 through 7. Inputs are denoted by A, B, C, and D.
Power is supplied via the V_{CC}, V_{EE}, and V_{BB} terminals.
V_{BB} is a reference voltage.

PIN ASSIGNMENTS

PIN	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
ECL2517	5	6	V_{CC}	7	0	V_{CC}	1	2	3	V_{EE}	C	B	A	D	V_{BB}	4

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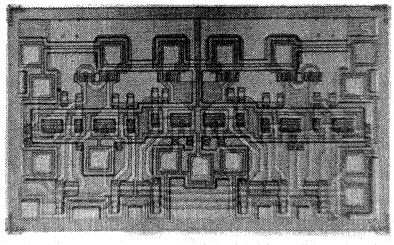
ECL2500 SERIES DUAL EMITTER-COUPLED-LOGIC (ECL) PARALLEL EMITTER-FOLLOWER GATES FOR APPLICATION IN ULTRA-HIGH-SPEED DIGITAL SYSTEMS



description

The ECL2500 series is a compatible family of ECL functions with basic gate delays of 2 to 3 ns per stage. The family is specifically designed for operation from 0°C to 75°C.

The ECL2500 family includes:

- Basic Gate Modules
- **Multifunction Gate Modules**
- Bistable Modules
- Arithmetic Modules
- Interface Modules
- Memory Modules

family features

- High speed . . . typical gate propagation delay time of 2.5 ns
- Complementary OR/NOR outputs with capability for wired-OR connections
- Designed for use with transmission lines to ensure maximum signal transmission without noise. Characterized for 50-ohm lines
- High noise immunity: ± 225 mV typical at 25°C

This data sheet covers the parallel emitter-follower modules.
Separate data sheets cover the balance of the ECL2500 modules.

ECL2500 series parallel emitter-follower gates

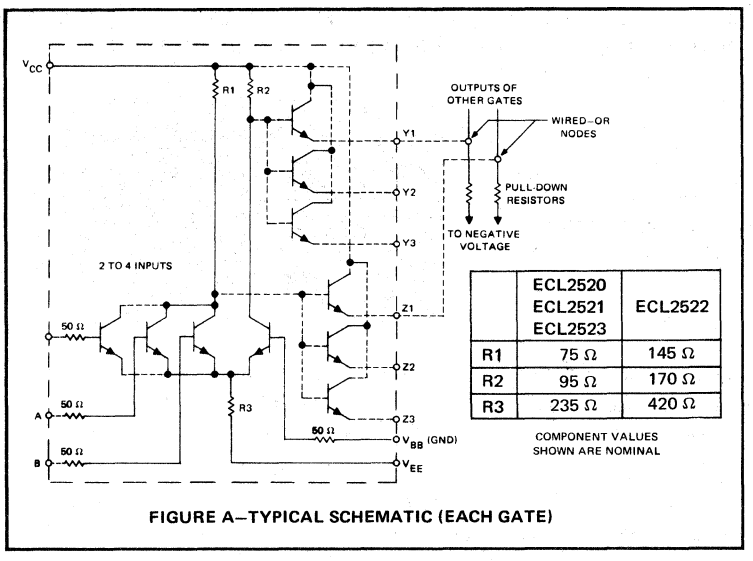
The four ECL2500 series modules that form the dual parallel emitter-follower gate group are shown in the table below. These modules contain various combinations of the ECL circuit shown in the schematic of Figure A and the logic diagrams of Figure B.

SUMMARY OF MODULES IN PARALLEL EMITTER-FOLLOWER GATE GROUP

MODULE	GATES PER MODULE	INPUTS PER GATE	POSITIVE LOGIC	OUTPUTS PER GATE	
				Y(OR)	Z(NOR)
ECL2520	2	2	OR/NOR	3	1
ECL2521	2	3	OR	3	
ECL2522	2	4	NOR		2
ECL2523	2	3	NOR		3

TYPES ECL2520 THRU ECL2523
DUAL PARALLEL EMITTER-FOLLOWER GATES

schematic



	ECL2520 ECL2521 ECL2523	ECL2522
R1	75 Ω	145 Ω
R2	95 Ω	170 Ω
R3	235 Ω	420 Ω

COMPONENT VALUES SHOWN ARE NOMINAL

FIGURE A—TYPICAL SCHEMATIC (EACH GATE)

logic

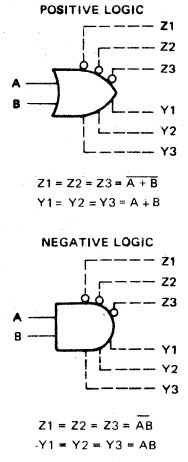


FIGURE B
TYPICAL LOGIC DIAGRAMS

Positive logic OR/NOR functions or negative logic AND/NAND functions are provided at the Y (OR) and Z (NOR) outputs, as shown.

Emitter-follower outputs require an external pull-down resistor. The wired-OR function can be obtained by connecting emitter-follower outputs of separate gates together. Only one pull-down resistor is required for each wire-OR node. Each output of a gate can be wire-OR connected independently of the other outputs of that gate.

absolute maximum ratings (see note 1)

Terminal voltages and currents . . . . . See table below
Storage temperature range . . . . . −40°C to 150°C
Temperature range with supply and bias voltages applied . . . . . −40°C to 100°C

TERMINAL VOLTAGE AND/OR CURRENT, T_A = 0°C TO 75°C (SEE NOTES 2 AND 3)

TERMINAL	REMARKS	VOLTAGE		CURRENT
		CONTINUOUS	20-μs SURGE	
V_{CC}		2 V	4.5 V	
V_{EE}		−4 V	−7 V	
Each Input	All other inputs open	−3.5 V	−4 V	
		2 V	2 V	
Output Y	All inputs high			−40 mA
Output Z	All inputs low			−40 mA

NOTES: 1. Absolute maximum ratings are limits beyond which the life of individual devices may be impaired and are never to be exceeded in service or testing.
2. Maximum terminal conditions must be considered as mutually exclusive.
3. All voltages are referenced to V_{BB}, which is at GND.

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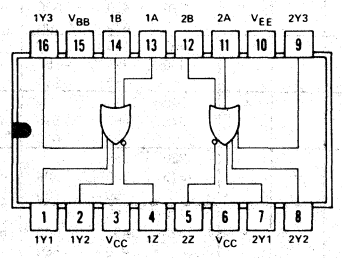
recommended operating conditions

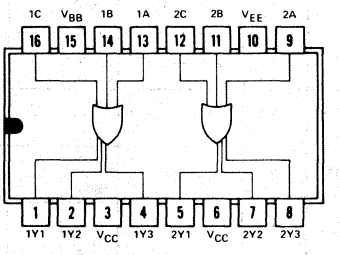
Supply voltage V_{CC}	1.32 V ± 2%
Supply voltage V_{EE}	−3.2 V ± 2%
Reference voltage V_{BB}	0 V (GND)
Reverse bias on unused inputs	−1 V ± 0.5 V
Normalized d-c fan-out	0 to 35
Load on each output	characterized at 270 Ω to V_{EE}, 50 Ω to GND
Operating free-air temperature range	0°C to 75°C

ECL2520



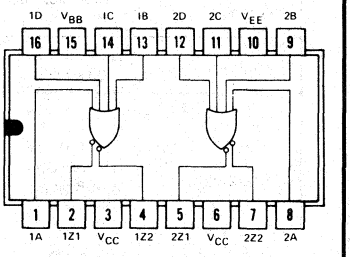
DUAL 2-INPUT OR/NOR GATE
(1 NOR, 3 OR OUTPUTS PER GATE)

ECL2521



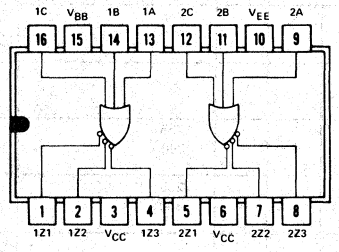
DUAL 3-INPUT OR GATE
(3 OR OUTPUTS PER GATE)

ECL2522



DUAL 4-INPUT NOR GATE
(2 NOR OUTPUTS PER GATE)

ECL2523



DUAL 3-INPUT NOR GATE
(3 NOR OUTPUTS PER GATE)

MODULE	POSITIVE LOGIC OUTPUT		NEGATIVE LOGIC OUTPUT	
	Y(OR)	Z(NOR)	Y (AND)	Z (NAND)
ECL2520	A+B	$\overline{A+B}$	AB	$\overline{AB}$
ECL2521	A+B+C		ABC	
ECL2522		$\overline{A+B+C+D}$		$\overline{ABCD}$
ECL2523		$\overline{A+B+C}$		$\overline{ABC}$

truth tables (for this series, H = positive voltage, L = negative voltage, X = irrelevant)

ECL2520

INPUTS		OUTPUTS			
A	B	Y1	Y2	Y3	Z
L	L	L	L	L	H
X	H	H	H	H	L
H	X	H	H	H	L
H	H	H	H	H	L

ECL2521

INPUTS			OUTPUTS		
A	B	C	Y1	Y2	Y3
L	L	L	L	L	L
H	X	X	H	H	H
X	H	X	H	H	H
X	X	H	H	H	H
H	H	H	H	H	H

ECL2522

INPUTS				OUTPUTS	
A	B	C	D	Z1	Z2
L	L	L	L	H	H
H	L	L	L	L	L
X	H	X	X	L	L
X	X	H	X	L	L
X	X	X	H	L	L
H	H	H	H	L	L

ECL2523

INPUTS			OUTPUTS		
A	B	C	Z1	Z2	Z3
L	L	L	H	H	H
H	X	X	L	L	L
X	H	X	L	L	L
X	X	H	L	L	L
H	H	H	L	L	L

electrical characteristics at specified free-air temperature

PARAMETER		TEST FIGURE	TEST CONDITIONS*		MODULE ECL2520	MODULE ECL2521	MODULE ECL2522	MODULE ECL2523	MIN (SEE NOTE 4)	TYP (SEE NOTE 4)	MAX (SEE NOTE 4)	UNIT
V_{IH}	High-level input voltage			0°C					150		720	
				25°C	•	•	•	•	150		720	mV
				75°C					150		720	
V_{IL}	Low-level input voltage			0°C					−1500		−150	
				25°C	•	•	•	•	−1500		−150	mV
				75°C					−1500		−150	
$V_{OH(Y)}$	High-level output voltage at OR output	2	V_I = 0.2 V	0°C					290	365		
				25°C	•	•			325	400	500	mV
				75°C						470	580	
$V_{OL(Y)}$	Low-level output voltage at OR output	2	V_I = −0.2 V	0°C					−505	−445		
				25°C	•	•			−490	−425	−350	mV
				75°C						−385	−310	
$V_{OH(Z)}$	High-level output voltage at NOR output	2	V_I = −0.2 V	0°C					340	415		
				25°C	•				375	450	525	mV
				75°C						520	605	
				0°C					280	355		
				25°C			•		315	390	500	mV
				75°C						460	580	
				0°C					290	365		
				25°C				•	325	400	500	mV
				75°C						470	580	
$V_{OL(Z)}$	Low-level output voltage at NOR output	2	V_I = 0.2 V	0°C						−385		
				25°C	•		•	•	−420	−365	−310	mV
				75°C						−325	−280	
$V_{OL(Z)}$	Low-level output voltage at NOR output	2	V_I = 0.4 V	0°C					−505	−455		
				25°C	•		•	•	−490	−425		mV
				75°C						−380	−315	
$V_{OH(Y)}$	High-level output voltage at OR output	2	V_I = 0.15 V	0°C					265			
				25°C	•	•			300			mV
				75°C								
$V_{OL(Y)}$	Low-level output voltage at OR output	2	V_I = −0.15 V	0°C								
				25°C	•	•					−325	mV
				75°C							−290	
$V_{OH(Z)}$	High-level output voltage at NOR output	2	V_I = −0.15 V	0°C					255			
				25°C			•		290			mV
				75°C								
				0°C					265			
				25°C				•	300			mV
				75°C								
$V_{OL(Z)}$	Low-level output voltage at NOR output	2	V_I = 0.15 V	0°C								
				25°C			•	•			−290	mV
				75°C							−260	
I_{IH}	High-level input current	3	V_I = 0.5 V	0°C							510†	
				25°C	•	•	•	•			470†	μA
				75°C							400†	
I_{IL}	Low-level input current	4	V_I = −3.2 V	0°C							−0.5‡	
				25°C	•	•	•	•			−0.6‡	μA
				75°C							−0.8‡	
I_{CC}					•				15		27	
or	Supply current	5	V_I = −0.5 V	25°C		•			15		27	mA
$-I_{EE}$							•		8		15	
								•	15		27	
C_{in}	Input capacitance		See Note 5	25°C	•	•	•	•		6		pF
z_{out}	Output impedance		See Note 6	25°C	•	•	•	•		5		Ω

*V_{BB} = GND, V_{CC} = 1.32 V ± 1%, V_{EE} = −3.20 V ± 1%.
†These are worst-case values. See Supplementary Parameter Measurement Information for each gate.
‡These are worst-case values for eight inputs in parallel. See Supplementary Parameter Measurement Information for each gate.

NOTES: 4. The algebraic convention where the most positive limit is designated as maximum is used in this data sheet for logic voltage levels only, e.g., if −350 mV is a maximum, the typical and minimum limits are more negative voltages.
5. C_{in} is measured using peak-current techniques. A square-wave input pulse is applied, and the input current waveform is integrated with respect to time to determine Q. C_{in} = Q/V.
6. Constant-current loads are used to determine the output impedance which is derived from the slope of a V_O vs I_O curve.

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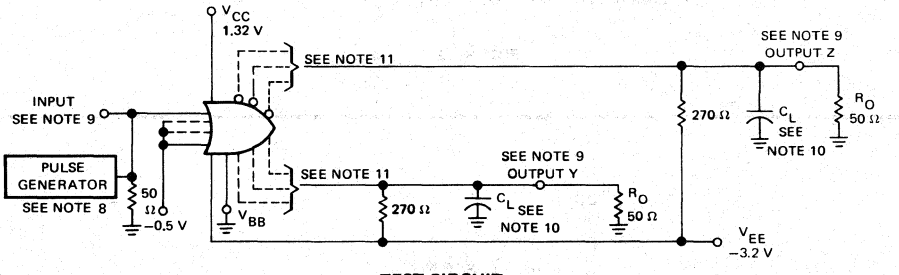
operating characteristics at specified free-air temperature (see figure 1)

PARAMETER		C_L	T_A	ECL2520						ECL2521			ECL2522 ECL2523			UNIT
				Y OUTPUTS			Z OUTPUTS			Y OUTPUTS			Z OUTPUTS			
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Propagation delay time, high-to-low-level output and/or	4 pF	0°C		3.2			2.1			3.2			3.3		
			25°C	2.2	3.2	4.3	1.3	2.1	3.1	2.2	3.2	4.3	2.2	3.2	4.3	ns
			75°C		3.2			2.1			3.2			3.3		
t_{PLH}	Propagation delay time, low-to-high-level output	50 pF	0°C		4.3			3.1			4.3			4.5		
			25°C	3.2	4.3	5.6	2.1	3.1	4.2	3.2	4.3	5.6	3.2	4.3	5.6	ns
			75°C		4.3			3.1			4.3			4.5		
t_{THL}	Transition time high-to-low-level output and/or	4 pF	0°C		5.1			2.6			5.1			5.3		
			25°C	2.8	5.2	6.5	1.7	2.6	3.9	2.8	5.2	6.5	2.8	5.2	6.5	ns
			75°C		5.1			2.6			5.1			5.1		
t_{TLH}	Transition time, low-to-high-level output	50 pF	0°C		4.9						4.9			4.9		
			25°C	2.8	4.8	6.5	See Note 7			2.8	4.8	6.5	2.8	4.8	6.5	ns
			75°C		4.7						4.7			4.7		

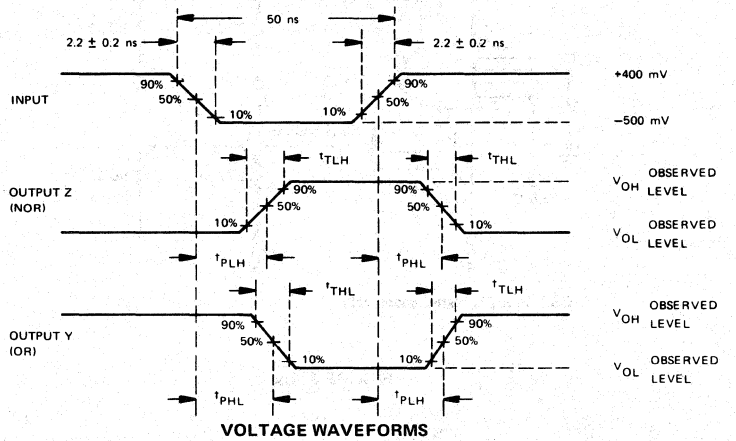
NOTE: 7. The transition times for the Z output at C_L = 50 pF are:
t_{THL} values are the same as for the Y output at 50 pF;
t_{TLH} values are the same as for the Z output at 4 pF.

4

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

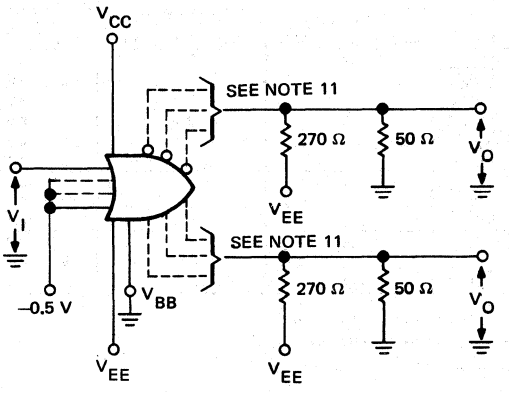


VOLTAGE WAVEFORMS

FIGURE 1—PROPAGATION DELAY AND TRANSITION TIMES

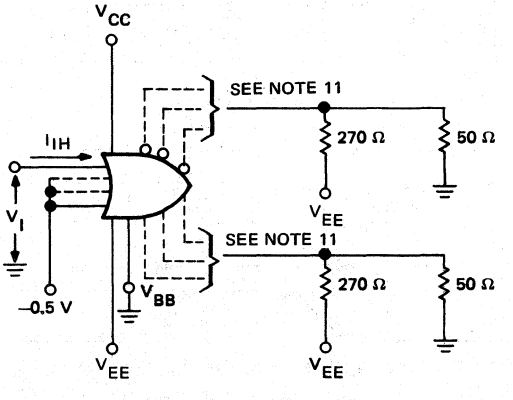
NOTES: 8. The generator has the following characteristics: Z_{out} = 50 Ω, PRR = 1 MHz.
9. The waveforms are monitored on an oscilloscope with a rise time of less than or equal to 350 ps. Either a high-impedance probe with an input impedance of 100 kΩ paralleled by 2 pF, or a 50-Ω impedance system can be used. The 50-Ω resistors designated R_O are the oscilloscope input resistance in the 50-Ω system or discrete resistors with a high-impedance probe.
10. C_L includes probe and fixture capacitance. A capacitance of 50 pF can be used to approximate an a-c fan-out of 10.
11. Each of the output terminals is loaded as shown.

PARAMETER MEASUREMENT INFORMATION†



A. V_I is applied to each input separately.
B. Each output is tested separately.

FIGURE 2–V_{OH} and V_{OL}



Each input is tested separately.

FIGURE 3–I_{IH}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

NOTE: 11. Each of the output terminals is loaded as shown.

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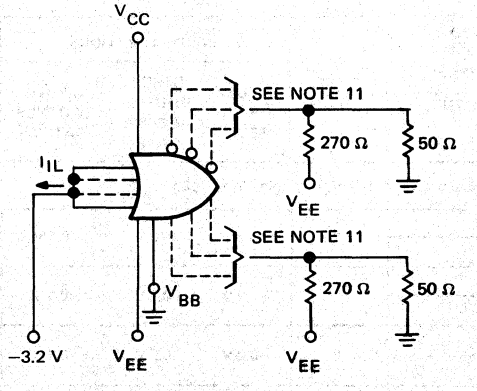
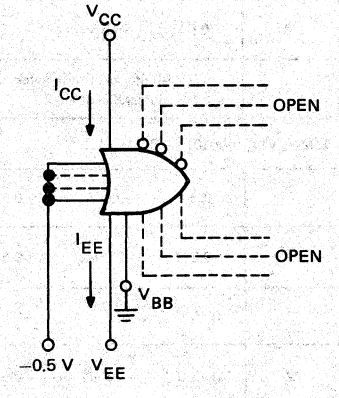
PARAMETER MEASUREMENT INFORMATION†



All inputs of both gates are connected in parallel.

FIGURE 4–I_{IL}



A. Both gates are tested simultaneously.
B. I_{CC} is the total current into both V_{CC} terminals.

FIGURE 5–I_{CC} or I_{EE}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

NOTE: 11. Each of the output terminals is loaded as shown.

SUPPLEMENTARY PARAMETER MEASUREMENT INFORMATION

electrical characteristics at specified free-air temperature

PARAMETER (SEE NOTE 12)	TERMINALS TO BE TESTED (SEE NOTE 13)		TEST FIGURE	INPUT CONDITIONS			T_A	MIN	TYP	MAX	UNIT
	INPUTS	OUTPUTS Y Z		INPUT UNDER TEST	OTHER INPUT(S) OF SAME GATE	INPUTS OF OTHER GATE(S)					
ECL2520 V_{BB} (pin 15) = GND, V_{CC} (pin 3 and pin 6) = 1.32 V, V_{EE} (pin 10) = −3.2 V											
$V_{OH(Y)}$	13, 14	1, 2, 16	2	0.2 V	−0.5 V	−0.5 V	0°C	290	365		mV
	11, 12	7, 8, 9					25°C	325	400	500	
							75°C		470	580	
$V_{OL(Y)}$	13, 14	1, 2, 16	2	−0.2 V	−0.5 V	−0.5 V	0°C	−505	−445		mV
	11, 12	7, 8, 9					25°C	−490	−425	−350	
							75°C		−385	−310	
$V_{OH(Z)}$	13, 14	4	2	−0.2 V	−0.5 V	−0.5 V	0°C	340	415		mV
	11, 12	5					25°C	375	450	525	
							75°C		520	605	
$V_{OL(Z)}$	13, 14	4	2	0.2 V	−0.5 V	−0.5 V	0°C		−385		mV
	11, 12	5					25°C	−440	−365	−310	
							75°C		−325	−280	
$V_{OL(Z)}$	13, 14	4	2	0.4 V	−0.5 V	−0.5 V	0°C	−505	−455		mV
	11, 12	5					25°C	−490	−425		
							75°C		−380	−315	
$V_{OH(Y)}$	11, 12	7	2	0.15 V	−0.5 V	−0.5 V	0°C	265			mV
							25°C	300			
							75°C				
$V_{OL(Y)}$	11, 12	7	2	−0.15 V	−0.5 V	−0.5 V	0°C				mV
							25°C			−325	
							75°C			−290	
I_{IH}	13, 14		3	0.5 V	−0.5 V	−0.5 V	0°C			510	μA
	11, 12						25°C			470	
							75°C			400	
I_{IL}	11, 12, 13, 14		4	All inputs of both gates in parallel at −3.2 V			0°C			−0.5	μA
							25°C			−0.5	
							75°C			−0.5	
ECL2521 V_{BB} (pin 15) = GND, V_{CC} (pin 3 and pin 6) = 1.32 V, V_{EE} (pin 10) = −3.2 V											
$V_{OH(Y)}$	9, 11, 12	5, 7, 8	2	0.2 V	−0.5 V	−0.5 V	0°C	290	365		mV
	13, 14, 16	1, 2, 4					25°C	325	400	500	
							75°C		470	580	
$V_{OL(Y)}$	9, 11, 12	5, 7, 8	2	−0.2 V	−0.5 V	−0.5 V	0°C	−505	−445		mV
	13, 14, 16	1, 2, 4					25°C	−490	−425	−350	
							75°C		−385	−310	
$V_{OH(Y)}$	13, 14, 16	1	2	0.15 V	−0.5 V	−0.5 V	0°C	265			mV
							25°C	300			
							75°C				
$V_{OL(Y)}$	13, 14, 16	1	2	−0.15 V	−0.5 V	−0.5 V	0°C				mV
							25°C			−325	
							75°C			−290	
I_{IH}	9, 11, 12		3	0.5 V	−0.5 V	−0.5 V	0°C			510	μA
	13, 14, 16						25°C			470	
							75°C			400	
I_{IL}	9, 11, 12, 13, 14, 16		4	All inputs of both gates in parallel at −3.2 V			0°C			−0.5	μA
							25°C			−0.5	
							75°C			−0.6	

NOTES: 12. See page 4 for defining term associated with each symbol.

13. Each gate is tested separately unless otherwise noted. See referenced test figure for output termination. Gates not under test have their outputs terminated in the same manner, and power applied.

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SUPPLEMENTARY PARAMETER MEASUREMENT INFORMATION

electrical characteristics at specified free-air temperature

PARAMETER (SEE NOTE 12)	TERMINALS TO BE TESTED (SEE NOTE 13)		TEST FIGURE	INPUT CONDITIONS			T_A	MIN	TYP	MAX	UNIT
	INPUTS	OUTPUTS Y Z		INPUT UNDER TEST	OTHER INPUT(S) OF SAME GATE	INPUTS OF OTHER GATE(S)					
ECL2522 V_{BB} (pin 15) = GND, V_{CC} (pin 3 and pin 6) = 1.32 V, V_{EE} (pin 10) = −3.2 V											
$V_{OH(Z)}$	1, 13, 14, 16	2, 4	2	−0.2 V	−0.5 V	−0.5V	0°C	280	355		mV
	8, 9, 11, 12	5, 7					25°C	315	390	500	
							75°C		460	580	
$V_{OL(Z)}$	1, 13, 14, 16	2, 4	2	0.2 V	−0.5 V	−0.5 V	0°C		−385		mV
	8, 9, 11, 12	5, 7					25°C	−440	−365	−310	
							75°C		−325	−280	
$V_{OL(Z)}$	1, 13, 14, 16	2, 4	2	0.4 V	−0.5 V	−0.5 V	0°C	−505	−455		mV
	8, 9, 11, 12	5, 7					25°C	−490	−425		
							75°C		−380	−315	
$V_{OH(Z)}$	1, 13, 14, 16	2	2	−0.15 V	−0.5 V	−0.5 V	0°C	255			mV
							25°C	290			
							75°C				
$V_{OL(Z)}$	1, 13, 14, 16	2	2	0.15 V	−0.5 V	−0.5 V	0°C				mV
							25°C			−290	
							75°C			−260	
I_{IH}	1, 13, 14, 16		3	0.5 V	−0.5 V	−0.5 V	0°C			255	μA
	8, 9, 11, 12						25°C			235	
							75°C			200	
I_{IL}	1, 8, 9, 11, 12, 13, 14, 16		4	All inputs of both gates in parallel at −3.2 V			0°C			−0.5	μA
							25°C			−0.6	
							75°C			−0.8	
ECL2523 V_{BB} (pin 15) = GND, V_{CC} (pin 3 and pin 6) = 1.32 V, V_{EE} (pin 10) = −3.2 V											
$V_{OH(Z)}$	13, 14, 16	1, 2, 4	2	−0.2 V	−0.5 V	−0.5 V	0°C	290	365		mV
	9, 11, 12	5, 7, 8					25°C	325	400	500	
							75°C		470	580	
$V_{OL(Z)}$	13, 14, 16	1, 2, 4	2	0.2 V	−0.5 V	−0.5 V	0°C		−385		mV
	9, 11, 12	5, 7, 8					25°C	−440	−365	−310	
							75°C		−325	−280	
$V_{OL(Z)}$	9, 11, 12	5	2	0.4 V	−0.5 V	−0.5 V	0°C	−505	−455		mV
							25°C	−490	−425		
							75°C		−380	−315	
$V_{OH(Z)}$	9, 11, 12	5	2	−0.15 V	−0.5 V	−0.5 V	0°C	265			mV
							25°C	300			
							75°C				
$V_{OL(Z)}$	9, 11, 12	5	2	0.15 V	−0.5 V	−0.5 V	0°C				mV
							25°C			−290	
							75°C			−260	
I_{IH}	13, 14, 16		3	0.5 V	−0.5 V	−0.5 V	0°C			510	μA
	9, 11, 12						25°C			470	
							75°C			400	
I_{IL}	9, 11, 12, 13, 14, 16		4	All inputs of both gates in parallel at −3.2 V			0°C			−0.5	μA
							25°C			−0.5	
							75°C			−0.6	

NOTES: 12. See page 4 for defining term associated with each symbol.
13. Each gate is tested separately unless otherwise noted. See referenced test figure for output termination. Gates not under test have their outputs terminated in the same manner, and power applied.

SUPPLEMENTARY PARAMETER MEASUREMENT INFORMATION

operating characteristics at specified free-air temperature (see figure 1)

TERMINALS TO BE TESTED (SEE NOTES 14, 15, 16)				C_L	t_{PHL} and/or t_{PLH} PROPAGATION TIMES–ns									t_{THL} and/or t_{TLH} TRANSITION TIMES–ns								
					T_A = 0°C			T_A = 25°C			T_A = 75°C			T_A = 0°C			T_A = 25°C			T_A = 75°C		
INPUT	OUTPUT	INPUT	OUTPUT	pF	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
ECL2520																						
13, 14	1, 2, 16	11, 12	7, 8, 9	4		3.2			2.2	3.2	4.3		3.2		5.1			2.8	5.2	6.5		5.1
				50		4.3			3.2	4.3	5.6		4.3		4.9			2.8	4.8	6.5		4.7
13, 14	4	11, 12	5	4		2.1			1.3	2.1	3.1		2.1		2.6			1.7	2.6	3.9		2.6
				50		3.1			2.1	3.1	4.2		3.1		2.6† 4.9‡			1.7† 2.8‡	2.6† 4.8‡	3.9† 6.5‡		2.6† 4.7‡
ECL2521																						
13, 14, 16	1, 2, 4	9, 11, 12	5, 7, 8	4		3.2			2.2	3.2	4.3		3.2		5.1			2.8	5.2	6.5		5.1
				50		4.3			3.2	4.3	5.6		4.3		4.9			2.8	4.8	6.5		4.7
ECL2522																						
1, 13, 14, 16	2, 4	8, 9, 11, 12	5, 7	4		3.3			2.2	3.2	4.3		3.3		5.3			2.8	5.2	6.5		5.1
				50		4.5			3.2	4.3	5.6		4.5		4.9			2.8	4.8	6.5		4.7
ECL2523																						
13, 14, 16	1, 2, 4	9, 11, 12	5, 7, 8	4		3.3			2.2	3.2	4.3		3.3		5.3			2.8	5.2	6.5		5.1
				50		4.5			3.2	4.3	5.6		4.5		4.9			2.8	4.8	6.5		4.7

† For t_{TLH} only.
‡ For t_{THL} only.

NOTES: 14. Each gate is tested separately.
15. The input pulse is measured as it is applied sequentially to each input of the gate under test, and a waveform measurement is made at each of the outputs of that gate. Times are as defined in Figure 1.
16. Bias voltages and loads for the gate under test are shown in Figure 1. The unused gate has inputs biased to −0.5 V, outputs under load, and power applied.

GENERAL APPLICATION INFORMATION

Multiple V_{CC} terminals have been supplied to reduce crosstalk noise. All V_{CC} terminals should be connected even if all gates in a module are not used.

Applications of the parallel emitter-follower gates at other than data sheet conditions are covered in a separate ECL2500 Series application document.

General loading for fan-out may be divided into two classes:

CLASS I Short-Line or Cluster Loading.

Loads which can be connected within two inches of any source can be treated as lumped capacitive loads which include the gate inputs and stub-line capacitances. Switching times can be interpolated accordingly. No two dotted outputs can be more than two inches apart for this case.

CLASS II Long-Line or Distributive Loading.

These loads must be treated as lumped loads along a transmission line and termination should be at the end of the transmission chain. No more than 20 pF of load is recommended per 4.5 inches of 50-ohm printed line (with dielectric constant of 4.5) in order that the reflection coefficient be no greater than 20%. If the loads are lumped loads of 20 pF, they must be 4.5 inches apart. If individual gates and **CLASS I** loads are distributed, they must not exceed the 20 pF per 4.5 inches of line.

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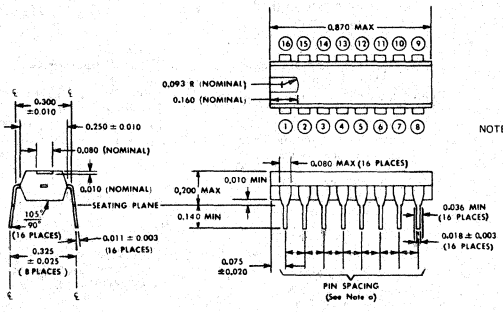
mechanical data

The circuit bars are mounted on a 16-lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperatures with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. This package is intended for insertion in mounting-hole rows on 0.300-inch centers. Once the leads are compressed to 0.300-inch separation and inserted, sufficient tension is provided to secure the package in the board during soldering. Silver-plated leads require no additional cleaning or processing when used in soldered assembly.

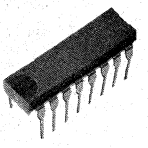
The plastic case is electrically nonconductive.

16-PIN PLASTIC DUAL-IN-LINE PACKAGE OUTLINE



NOTES: a. The true-position pin spacing is 0.100 between center-lines. Each pin centerline is located within 0.010 of its true longitudinal position relative to pins 1 and 16.

b. All dimensions are in inches unless otherwise noted.



4

terminal designations

Pin assignments are shown in the table below and correspond to the logic diagrams on page 3.
Outputs are denoted by Y or Z. Inputs are denoted by A, B, C, etc.
Respective inputs and outputs are identified by a gate number preceding the pin symbol.
Power is supplied via the V_{CC}, V_{EE}, and V_{BB} terminals.
V_{BB} is a reference voltage.

PIN ASSIGNMENTS

PIN	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
ECL2520	1Y1	1Y2	V_{CC}	1Z	2Z	V_{CC}	2Y1	2Y2	2Y3	V_{EE}	2A	2B	1A	1B	V_{BB}	1Y3
ECL2521	1Y1	1Y2	V_{CC}	1Y3	2Y1	V_{CC}	2Y2	2Y3	2A	V_{EE}	2B	2C	1A	1B	V_{BB}	1C
ECL2522	1A	1Z1	V_{CC}	1Z2	2Z1	V_{CC}	2Z2	2A	2B	V_{EE}	2C	2D	1B	1C	V_{BB}	1D
ECL2523	1Z1	1Z2	V_{CC}	1Z3	2Z1	V_{CC}	2Z2	2Z3	2A	V_{EE}	2B	2C	1A	1B	V_{BB}	1C

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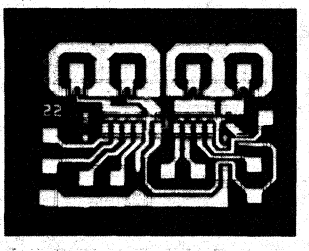
ECL2500 SERIES EMITTER-COUPLED-LOGIC (ECL) DUAL LINE RECEIVER AND DUAL LINE DRIVER FOR APPLICATION IN ULTRA-HIGH-SPEED DIGITAL SYSTEMS

description

The ECL2500 series is a compatible family of ECL functions with basic gate delays of 2 to 3 ns per stage. The family is specifically designed for operation from 0°C to 75°C.



The ECL2500 family includes:

- Basic Gate Modules
- Multifunction Gate Modules
- Bistable Modules
- Arithmetic Modules
- **Interface Modules**
- Memory Module

family features

- High speed . . . typical gate propagation delay time of 2.5 ns
- Complementary OR/NOR outputs with capability for wired-OR connections
- Designed for use with transmission lines to ensure maximum signal transmission without noise. Characterized for 50-ohm lines
- High noise immunity: ± 225 mV typical at 25°C

This data sheet covers the line receiver and the line driver modules.
Separate data sheets cover the balance of the ECL2500 modules.

ECL2500 series line receiver and line driver

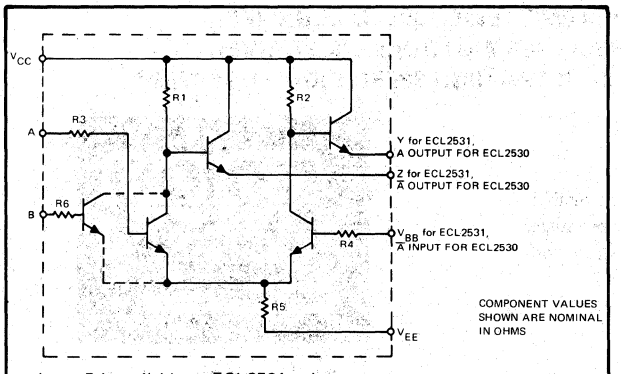
The ECL2500 series dual line receiver and dual line driver modules are shown in the tables below. These modules contain various combinations of the ECL circuit shown in the schematic of Figure A and the logic diagrams of Figure B.

SUMMARY OF LINE RECEIVER AND LINE DRIVER MODULES

MODULE	DIFFERENTIAL AMPLIFIERS PER MODULE	DIFFERENTIAL INPUTS PER AMPLIFIER	POSITIVE LOGIC	DIFFERENTIAL OUTPUTS PER AMPLIFIER	
				A	$\overline{A}$
ECL2530 Line Receiver	2	2	NOR/OR	1	1

MODULE	GATES PER MODULE	INPUTS PER GATE	POSITIVE LOGIC	OUTPUTS PER GATE	
				Y (OR)	Z (NOR)
ECL2531 Line Driver	2	2	NOR/OR	1	1

schematic



Input B is available on ECL2531 only

	R1	R2	R3	R4	R5	R6
ECL2530	145	145	50	50	420	–
ECL2531	100	120	50	50	290	50

FIGURE A–SCHEMATIC (each gate)

logic

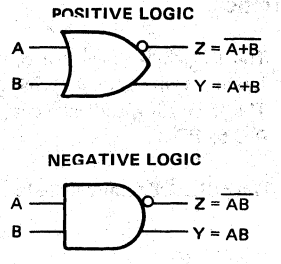


FIGURE B–ECL2531 LOGIC DIAGRAMS

Positive logic OR/NOR functions or negative logic AND/NAND functions are provided at the Y (OR) and Z (NOR) outputs, as shown. When the $\overline{A}$ input of the ECL2530 is connected to V_{BB}, the A and $\overline{A}$ outputs function as OR (Y) and NOR (Z) outputs respectively; and vice versa when the A input is connected to V_{BB}.

Emitter-follower outputs require an external pull-down resistor. The wired-OR function can be obtained by connecting emitter-follower outputs of separate gates together. Only one pull-down resistor is required for each wired-OR node.

absolute maximum ratings (see note 1)

Terminal voltages and currents	See table below
Storage temperature range	–40°C to 150°C
Temperature range with supply and bias voltage applied	–40°C to 100°C

TERMINAL VOLTAGE AND/OR CURRENT, T_A = 0°C to 75°C (SEE NOTES 2 AND 3)

TERMINAL	REMARKS	VOLTAGE		CURRENT	
		CONTINUOUS	20-μs SURGE	ECL2530	ECL2531
V_{CC}		2 V	4.5 V		
V_{EE}		–4 V	–7 V		
Each Input	Other input of ECL2530 at V_{BB}, all other inputs of ECL2531 open	–3.5 V	–4 V		
		2 V	2 V		
Output Y	All inputs (input A of ECL2530) high			–40 mA	–50 mA
Output Z	All inputs (input A of ECL2530) low			–40 mA	–50 mA

NOTES: 1. Absolute maximum ratings are limits beyond which the life of individual devices may be impaired and are never to be exceeded in service or testing.
2. Maximum terminal conditions must be considered as mutually exclusive.
3. All voltages are referenced to V_{BB}, which is at GND.

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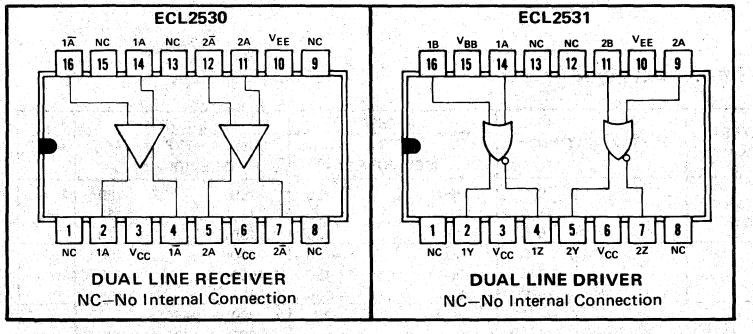
logic



ECL2530†

POSITIVE LOGIC		NEGATIVE LOGIC	
A (OR)	$\overline{A}$ (NOR)	A (AND)	$\overline{A}$ (NAND)
A	$\overline{A}$	A	$\overline{A}$

†With $\overline{A}$ input at V_{BB}

ECL2531

POSITIVE LOGIC		NEGATIVE LOGIC	
Y (OR)	Z (NOR)	Y (AND)	Z (NAND)
A + B	$\overline{A + B}$	AB	$\overline{AB}$

truth tables (for this series, H = positive voltage, L = negative voltage, X = irrelevant)

ECL2530			
INPUTS		OUTPUTS	
A	$\overline{A}$	A	$\overline{A}$
L	V_{BB}	L	H
H	V_{BB}	H	L
V_{BB}	L	H	L
V_{BB}	H	L	H

ECL2531			
INPUTS		OUTPUTS	
A	B	Y	Z
L	L	L	H
H	X	H	L
X	H	H	L
H	H	H	L

recommended operating conditions

Supply voltage V_{CC}	1.32 V ± 2%
Supply voltage V_{EE}	−3.2 V ± 2%
Reference voltage V_{BB}	0 V (GND)
Reverse bias on unused inputs	−1 V ± 0.5 V
Normalized d-c fan-out	0 to 35
Load on each output	ECL2530 characterized at 270 Ω to V_{EE}, 50 Ω to GND ECL2531 characterized at 135 Ω to V_{EE}, 25 Ω to GND
Operating free-air temperature range	0°C to 75°C

GENERAL APPLICATION INFORMATION

Multiple V_{CC} terminals have been supplied to reduce crosstalk noise. All V_{CC} terminals should be connected even if all gates in a module are not used.

Applications of the line receiver and the line driver modules at other than data sheet conditions are covered in a separate ECL2500 series application document.

General loading for fan-out may be divided into two classes:

CLASS I **Short-Line or Cluster Loading.**
Loads which can be connected within two inches of any source can be treated as lumped capacitive loads which include the gate inputs and stub-line capacitances. Switching times can be interpolated accordingly. No two dotted outputs can be more than two inches apart for this case.

CLASS II **Long-Line or Distributive Loading.**
These loads must be treated as lumped loads along a transmission line and termination should be at the end of the transmission chain. No more than 20 pF of load is recommended per 4.5 inches of 50-ohm printed line (with dielectric constant of 4.5) in order that the reflection coefficient be no greater than 20%. If the loads are lumped loads of 20 pF, they must be 4.5 inches apart. If individual gates and **CLASS I** loads are distributed, they must not exceed the 20 pF per 4.5 inches of line.

electrical characteristics at specified free-air temperature

PARAMETER (SEE NOTE 4)		TEST FIGURE	TEST CONDITIONS*		ECL2530 MIN	ECL2530 TYP	ECL2530 MAX	ECL2531 MIN	ECL2531 TYP	ECL2531 MAX	UNIT
					(SEE NOTE 5)			(SEE NOTE 5)			
V_{IH}	High-level input voltage			0°C	150		720	150		720	mV
				25°C	150		720	150		720	
				75°C	150		720	150		720	
V_{IL}	Low-level input voltage			0°C	−1500		−150	−1500		−150	mV
				25°C	−1500		−150	−1500		−150	
				75°C	−1500		−150	−1500		−150	
$V_{OH(Y)}$	High-level output voltage at OR output	2	V_I = 0.2 V	0°C				290	365		mV
				25°C				325	400	475	
				75°C					470	560	
$V_{OL(Y)}$	Low-level output voltage at OR output	2	V_I = −0.2 V	0°C				−505	−450		mV
				25°C				−495	−430	−355	
				75°C					−390	−310	
$V_{OH(Z)}$	High-level output voltage at NOR output	2	V_I = −0.2 V	0°C	315	390		290	365		mV
				25°C	350	425	500	325	400	475	
				75°C		495	580		470	560	
$V_{OL(Z)}$	Low-level output voltage at NOR output	2	V_I = 0.2 V	0°C		−385			−400		mV
				25°C	−440	−365	−310	−450	−380	−310	
				75°C		−325	−280		−340	−280	
$V_{OL(Z)}$	Low-level output voltage at NOR output	2	V_I = 0.4 V	0°C	−505	−455		−505	−460		mV
				25°C	−490	−425		−495	−430		
				75°C		−380	−315		−385	−315	
$V_{OH(Y)}$	High-level output voltage at OR output	2	V_I = 0.15 V	0°C				270			mV
				25°C				305			
				75°C							
$V_{OL(Y)}$	Low-level output voltage at OR output	2	V_I = −0.15 V	0°C							mV
				25°C						−330	
				75°C						−290	
$V_{OH(Z)}$	High-level output voltage at NOR output	2	V_I = −0.15 V	0°C	290						mV
				25°C	325						
				75°C							
$V_{OL(Z)}$	Low-level output voltage at NOR output	2	V_I = 0.15 V	0°C							mV
				25°C			−290				
				75°C			−260				
I_{IH}	High-level input current	3	V_I = 0.5 V	0°C			255			385	μA
				25°C			235			350	
				75°C			200			300	
I_{IL}	Low-level input current	4	V_I = −3.2 V	0°C			−0.5			−0.5	μA
				25°C			−0.5			−0.5	
				75°C			−0.5			−0.5	
I_{CC} or I_{EE}	Supply current	5	V_I = −0.5 V	25°C	8		15	12		22	mA
C_{in}	Input capacitance		See Note 6	25°C		5			5		pF
z_{out}	Output impedance		See Note 7	25°C		5			5		Ω

*V_{BB} = GND, V_{CC} = 1.32 V ± 1%, V_{EE} = −3.20 V ± 1%.

NOTES: 4. When the $\overline{A}$ input of the ECL2530 is connected to V_{BB}, the A and $\overline{A}$ outputs function as OR (Y) and NOR (Z) outputs respectively; and vice versa when the A input is connected to V_{BB}.

5. The algebraic convention where the most positive limit is designated as maximum is used in this data sheet for logic voltage levels only, e. g., if −350 mV is a maximum, the typical and minimum limits are more negative voltages.

6. C_{in} is measured using peak-current techniques. A square-wave input pulse is applied and the input current waveform is integrated with respect to time to determine Q. C_{in} = Q/V.

7. Constant-current loads are used to determine the output impedance which is derived from the slope of a V_O vs I_O curve.

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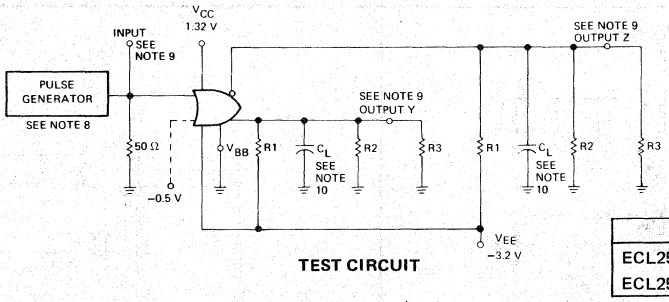
operating characteristics at specified free-air temperature (see figure 1)

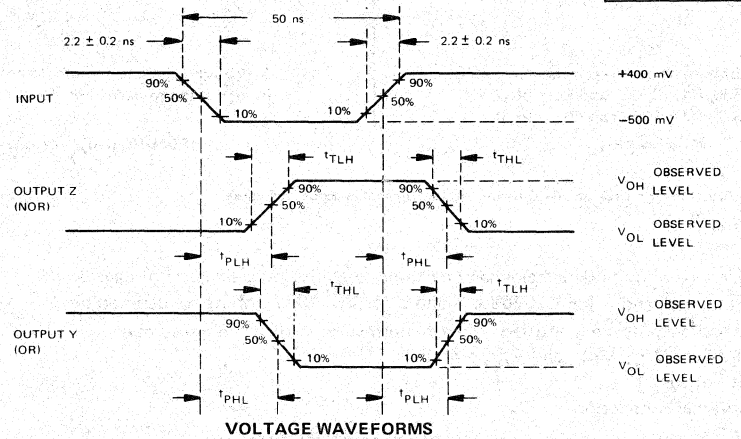
PARAMETER		C_L	T_A	ECL2530 ANY OUTPUT			ECL2531 ANY OUTPUT			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Propagation delay time, high-to-low-level output and/or	4 pF	0°C		2.1			2.7		ns
			25°C	1.3	2.1	3	1.8	2.7	3.7	
			75°C		2.2			2.8		
t_{PLH}	Propagation delay time, low-to-high-level output	50 pF	0°C		3.1			3.5		ns
			25°C	2.3	3.1	4.2	2.6	3.5	4.6	
			75°C		3.1			3.5		
t_{THL}	Transition time, high-to-low-level output and/or	4 pF	0°C		2.7			3.8		ns
			25°C	1.6	2.9	4.2	2.5	3.8	5	
			75°C		2.8			3.9		
t_{TLH}	Transition time, low-to-high-level output	50 pF	0°C		3.6			3.7		ns
			25°C	2.2	3.6	6	2.5	3.7	5	
			75°C		3.6			3.7		

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

	R1	R2	R3
ECL2530	270 Ω	Not Used	50 Ω
ECL2531	135 Ω	50 Ω	50 Ω

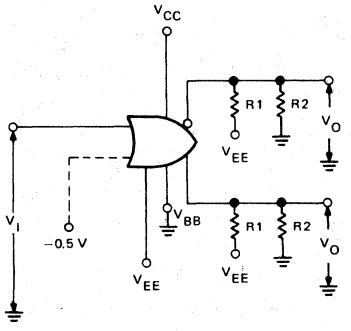


VOLTAGE WAVEFORMS

FIGURE 1—PROPAGATION DELAY AND TRANSITION TIMES

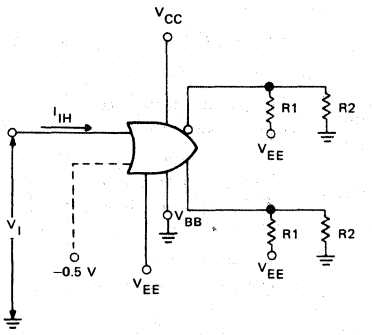
NOTES:
8. The generator has the following characteristics: Z_{out} = 50 Ω, PRR = 1 MHz.
9. The waveforms are monitored on an oscilloscope with a rise time of less than or equal to 350 ps. Either a high-impedance probe with an input impedance of 100 kΩ paralleled by 2 pF or a 50-Ω impedance system can be used. Resistors R3 are the oscilloscope input resistance in the 50-Ω system or discrete resistors with a high-impedance probe.
10. C_L includes probe and fixture capacitance. A capacitance of 50 pF can be used to approximate an a-c fan-out of 10.

PARAMETER MEASUREMENT INFORMATION†



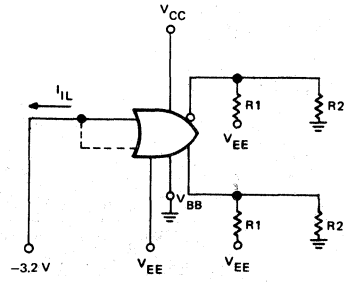
A. V_I is applied to each input separately.
B. Each output is tested separately.
C. For ECL2530, R1 = 270 Ω and R2 = 50 Ω.
For ECL2531, R1 = 135 Ω and R2 = 25 Ω.

FIGURE 2–V_{OH} AND V_{OL}



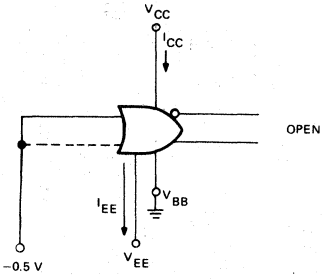
A. Each input is tested separately.
B. For ECL2530, R1 = 270 Ω and R2 = 50 Ω.
For ECL2531, R1 = 135 Ω and R2 = 25 Ω.

FIGURE 3–I_{IH}



A. All inputs of both gates are connected in parallel.
B. For ECL2530, R1 = 270 Ω and R2 = 50 Ω.
For ECL2531, R1 = 135 Ω and R2 = 25 Ω.

FIGURE 4–I_{IL}



A. Both gates are tested simultaneously.
B. I_{CC} is the total current into both V_{CC} terminals.

FIGURE 5–I_{CC} or I_{EE}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

terminal designations

Pin assignments are shown in the table below and correspond to the logic diagrams of page 3.
Outputs are denoted by A and $\overline{A}$ for ECL2530, Y and Z for ECL2531. Inputs are denoted by A, $\overline{A}$, or B.
Respective inputs and outputs are identified by a gate number preceding the pin symbol.
Power is supplied via the V_{CC}, V_{EE}, and V_{BB} terminals.
V_{BB} is a reference voltage.
NC indicates no internal connection.

PIN ASSIGNMENTS

PIN	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
ECL2530	NC	1A (OUT)	V_{CC}	1$\overline{A}$ (OUT)	2A (OUT)	V_{CC}	2$\overline{A}$ (OUT)	NC	NC	V_{EE}	2A (IN)	2$\overline{A}$ (IN)	NC	1A (IN)	NC	1$\overline{A}$ (IN)
ECL2531	NC	1Y	V_{CC}	1Z	2Y	V_{CC}	2Z	NC	2A	V_{EE}	2B	NC	NC	1A	V_{BB}	1B

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SUPPLEMENTARY PARAMETER MEASUREMENT INFORMATION

electrical characteristics at specified free-air temperature

PARAMETER (SEE NOTES 4 AND 11)	TERMINALS TO BE TESTED (SEE NOTE 12)		TEST FIGURE	INPUT CONDITIONS			T_A	MIN (SEE NOTE 5)	TYP (SEE NOTE 5)	MAX (SEE NOTE 5)	UNIT
	INPUTS	OUTPUTS Y Z		INPUT UNDER TEST	OTHER INPUT(S) OF SAME GATE	INPUTS OF OTHER GATE(S)					
ECL2530 V_{CC} (pin 3 and pin 6) = 1.32 V, V_{EE} (pin 10) = −3.2 V											
$V_{OH(Z)}$	14	4	2	−0.2 V	GND	OPEN	0°C	315	390		mV
	16	2					25°C	350	425	500	
	11	7					75°C		495	580	
	12	5									
$V_{OL(Z)}$	14	4	2	0.2 V	GND	OPEN	0°C		−385		mV
	16	2					25°C	−440	−365	−310	
	11	7					75°C		−325	−280	
	12	5									
$V_{OL(Z)}$	14	4	2	0.4 V	GND	OPEN	0°C	−505	−455		mV
	16	2					25°C	−490	−425		
	11	7					75°C		−380	−315	
	12	5									
$V_{OH(Z)}$	11	7	2	−0.15 V	GND	OPEN	0°C	290			mV
							25°C	325			
							75°C				
$V_{OL(Z)}$	11	7	2	0.15 V	GND	OPEN	0°C				mV
							25°C			−290	
							75°C			−260	
I_{IH}	14		3	0.5 V	GND	OPEN	0°C			255	μA
	16						25°C			235	
	11						75°C			200	
	12										
I_{IL}	11, 12, 14, 16		4	All inputs of both gates in parallel at −3.2 V			0°C			−0.5	μA
							25°C			−0.5	
							75°C			−0.5	
ECL2531 V_{BB} (pin 15) = GND, V_{CC} (pin 3 and pin 6) = 1.32 V, V_{EE} (pin 10) = −3.2 V											
$V_{OH(Y)}$	14, 16	2	2	0.2 V	−0.5 V	−0.5 V	0°C	290	365		mV
	9, 11	5					25°C	325	400	475	
							75°C		470	560	
$V_{OL(Y)}$	14, 16	2	2	−0.2 V	−0.5 V	−0.5 V	0°C	−505	−450		mV
	9, 11	5					25°C	−495	−430	−355	
							75°C		−390	−310	
$V_{OH(Z)}$	14, 16	4	2	−0.2 V	−0.5 V	−0.5 V	0°C	290	365		mV
	9, 11	7					25°C	325	400	475	
							75°C		470	560	
$V_{OL(Z)}$	14, 16	4	2	0.2 V	−0.5 V	−0.5 V	0°C		−400		mV
	9, 11	7					25°C	−450	−380	−310	
							75°C		−340	−280	
$V_{OL(Z)}$	14, 16	4	2	0.4 V	−0.5 V	−0.5 V	0°C	−505	−460		mV
	9, 11	7					25°C	−495	−430		
							75°C		−385	−315	
$V_{OH(Y)}$	9	5	2	0.15 V	−0.5 V	−0.5 V	0°C	270			mV
							25°C	305			
							75°C				
$V_{OL(Y)}$	9	5	2	−0.15 V	−0.5 V	−0.5 V	0°C				mV
							25°C			−330	
							75°C			−290	
I_{IH}	14, 16		3	0.5 V	−0.5 V	−0.5 V	0°C			385	μA
	9, 11						25°C			350	
							75°C			300	
I_{IL}	9, 11, 14, 16		4	All inputs of both gates in parallel at −3.2 V			0°C			−0.5	μA
							25°C			−0.5	
							75°C			−0.5	

NOTES: 4. When the $\overline{A}$ input of the ECL2530 is connected to V_{BB}, the A and $\overline{A}$ outputs function as OR (Y) and NOR (Z) outputs respectively; and vice versa when the A input is connected to V_{BB}.

5. The algebraic convention where the most positive limit is designated as maximum is used in this data sheet for logic voltage levels only, e.g., if −350 mV is a maximum, the typical and minimum limits are more negative voltages.

11. See page 4 for defining term associated with each symbol.

12. Each gate is tested separately unless otherwise noted. See referenced test figure for output termination. Gates not under test have their outputs terminated in the same manner, and power applied.

SUPPLEMENTARY PARAMETER MEASUREMENT INFORMATION

operating characteristics at specified free-air temperature (see figure 1)

TERMINALS TO BE TESTED (SEE NOTES 13, 14, 15)				C_L	t_{PHL} and/or t_{PLH} PROPAGATION TIMES—ns									t_{THL} and/or t_{TLH} TRANSITION TIMES—ns								
					T_A = 0°C			T_A = 25°C			T_A = 75°C			T_A = 0°C			T_A = 25°C			T_A = 75°C		
INPUT	OUTPUT	INPUT	OUTPUT	pF	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
ECL2530 (See Note 16)																						
14	2	16	4	4		2.1		1.3	2.1	3		2.2			2.7		1.6	2.9	4.2		2.8	
	4		2	50		3.1		2.3	3.1	4.2		3.1			3.6		2.2	3.6	6		3.6	
11	5	12	7	4		2.1		1.3	2.1	3		2.2			2.7		1.6	2.9	4.2		2.8	
	7		5	50		3.1		2.3	3.1	4.2		3.1			3.6		2.2	3.6	6		3.6	
ECL2531																						
14, 16	2, 4	9, 11	5, 7	4		2.7		1.8	2.7	3.7		2.8			3.8		2.5	3.8	5		3.9	
				50		3.5		2.6	3.5	4.6		3.5			3.7		2.5	3.7	5		3.7	

4

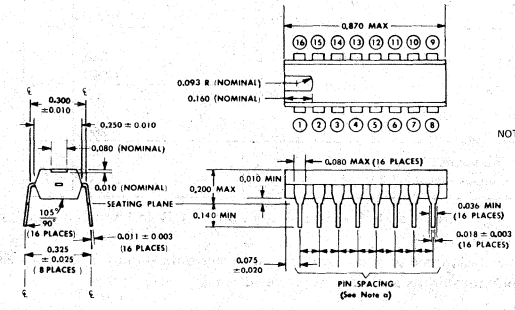
NOTES: 13. Each gate is tested separately.
14. The input pulse is measured as it is applied sequentially to each input of the gate under test and a waveform measurement is made at each of the outputs of that gate. Times are as defined in Figure 1.
15. Bias voltages and loads for the gate under test are shown in Figure 1. The unused gate has inputs biased to −0,5 V, outputs under load, and power applied.
16. When an input pulse is applied to pin 11, pin 12 is at GND, and vice versa. The same relationship holds true between pins 14 and 16.

mechanical data

The circuit bars are mounted on a 16-lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperatures with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. This package is intended for insertion in mounting-hole rows on 0.300-inch centers. Once the leads are compressed to 0.300-inch separation and inserted, sufficient tension is provided to secure the package in the board during soldering. Silver-plated leads require no additional cleaning or processing when used in soldered assembly.

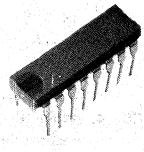
The plastic case is electrically nonconductive.

16-PIN PLASTIC DUAL-IN-LINE PACKAGE OUTLINE



NOTES: a. The true-position pin spacing is 0.100 between center-lines. Each pin centerline is located within 0.010 of its true longitudinal position relative to pins 1 and 16.

b. All dimensions are in inches unless otherwise noted.



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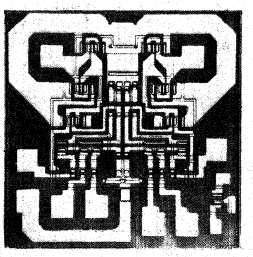
ECL2500 SERIES EMITTER-COUPLED-LOGIC (ECL) LEVEL CONVERTERS FOR APPLICATION IN ULTRA-HIGH-SPEED DIGITAL SYSTEMS



description

The ECL2500 series is a compatible family of ECL functions with basic gate delays of 2 to 3 ns per stage. The family is specifically designed for operation from 0°C to 75°C.

The ECL2500 family includes:

- Basic Gate Modules
- Multifunction Gate Modules
- Bistable Modules
- Arithmetic Modules
- **Interface Modules**
- Memory Module

family features

- High speed . . . typical gate propagation delay time of 2.5 ns
- Complementary OR/NOR outputs with capability for wired-OR connections
- Designed for use with transmission lines to ensure maximum signal transmission without noise. Characterized for 50-ohm lines
- High noise immunity: ± 225 mV typical at 25°C

This data sheet covers the ECL-to-HLL and HLL-to-ECL converter modules. Separate data sheets cover the balance of the ECL2500 modules.

ECL2500 series ECL-to-HLL and HLL-to-ECL converters

The ECL2536 contains two high-level-logic-to-emitter-coupled-logic converters each having an HLL input (B*) and an ECL input (A). Each converter has complementary ECL outputs. The ECL input (A) is provided to be used as an INHIBIT/ENABLE control. When input A is low, the converter is enabled and the output state is determined by input B*. When input A is high, output Y is high and output Z is low regardless of the state of input B*.

The ECL2537 contains two emitter-coupled-logic-to-high-level-logic converters. Each converter has two ECL inputs and complementary HLL outputs.

The ECL2536 and ECL2537 are summarized in the table below, shown schematically in Figure A, and shown logically in Figure B.

SUMMARY OF HLL-TO-ECL AND ECL-TO-HLL CONVERTERS

MODULE	GATES PER MODULE	INPUTS PER GATE	POSITIVE LOGIC	OUTPUTS PER GATE	
				Y (OR)	Z (NOR)
ECL2536 DUAL HLL-TO-ECL CONVERTER	2	1 HLL input 1 ECL inhibit input	OR/NOR	1	1
ECL2537 DUAL ECL-TO-HLL CONVERTER	2	2	OR/NOR	1	1

TYPES ECL2536, ECL2537
HLL-TO-ECL AND ECL-TO-HLL CONVERTERS

schematic

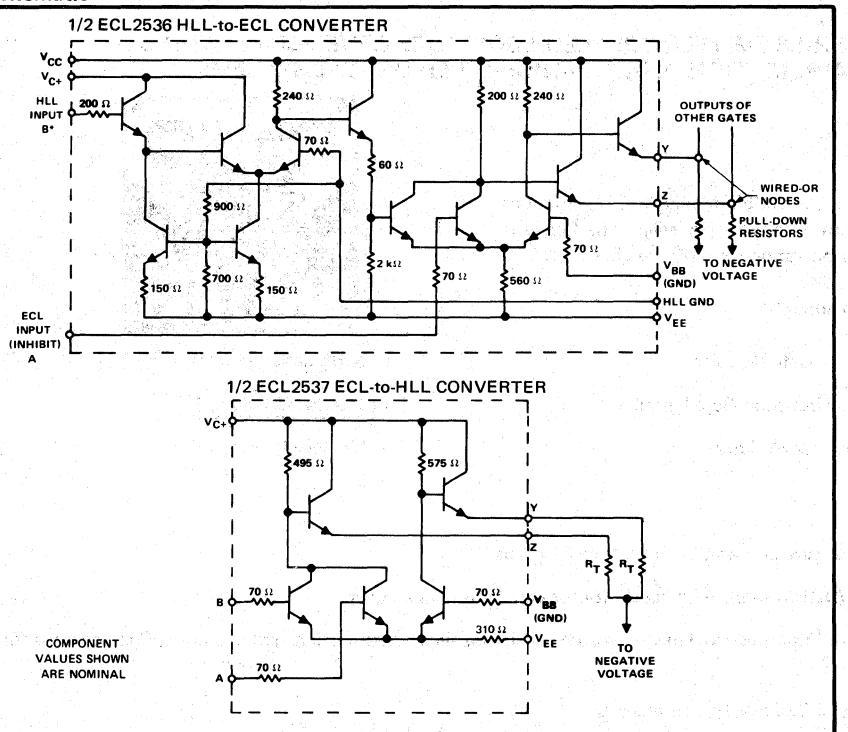


FIGURE A—SCHEMATIC

logic

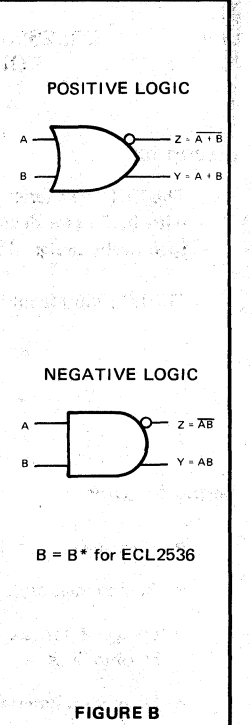
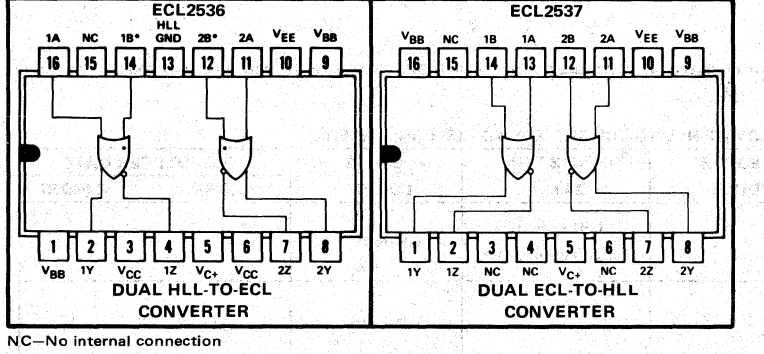


FIGURE B
LOGIC DIAGRAMS

Positive logic OR/NOR functions or negative logic AND/NAND functions are provided at the Y (OR) and Z (NOR) outputs, as shown.

Emitter-follower outputs require an external pull-down resistor. For ECL2536 only, the wired-OR function can be obtained by connecting emitter-follower outputs of separate gates together. Only one pull-down resistor is required for each wired-OR node. ECL2537 outputs require pull-down resistors (R_T in schematic above) to sink the low-level input current of the driven HLL inputs. ECL2537 cannot have wired-OR connections.

logic



NC—No internal connection

MODULE	POSITIVE LOGIC		NEGATIVE LOGIC	
	Y (OR)	Z (NOR)	Y (AND)	Z (NAND)
ECL2536	A+B*	$\overline{A+B^*}$	AB*	$\overline{AB^*}$
ECL2537	A+B	$\overline{A+B}$	AB	$\overline{AB}$

B* is the HLL input of the ECL2536.

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truth tables

(For HLL inputs, H = high-level positive voltage, L = low-level positive voltage. For ECL inputs, H = positive voltage, L = negative voltage)

ECL2536

INPUTS		OUTPUTS	
A	B*	Y (OR)	Z (NOR)
L	L	L	H
L	H	H	L
H	L	H	L
H	H	H	L

B* is the HLL input of the ECL2536.

ECL2537

INPUTS		OUTPUTS	
A	B	Y (OR)	Z (NOR)
L	L	L	H
L	H	H	L
H	L	H	L
H	H	H	L

absolute maximum ratings (see note 1)

Terminal voltages and currents . . . . . See table below
Storage temperature range . . . . . −40°C to 150°C
Temperature range with supply and bias voltages applied . . . . . −40°C to 100°C

4

TERMINAL VOLTAGE AND/OR CURRENT, T_A = 0°C to 75°C (SEE NOTES 2 AND 3)

TERMINAL	REMARKS	VOLTAGE		CURRENT
		CONTINUOUS	20-μs SURGE	
V_{C+}		6 V	7 V	
V_{CC} (ECL2536)		2 V	4.5 V	
V_{EE}		−4 V	−7 V	
Each ECL input (ECL2536 and ECL2537)	All other inputs open	−3.5 V	−4 V	
		2 V	2 V	
Each HLL input (ECL2536 only)		−1.25 V	−1.5 V	
		4.5 V	5 V	
Output Y (ECL2536)	A input low, B* input high			−40 mA
Output Y (ECL2537)	All inputs high			−40 mA
Output Z	All inputs low			−40 mA

recommended operating conditions

Supply voltage V_{C+} . . . . . 4.8 V ± 1%
Supply voltage V_{CC} (ECL2536 only) . . . . . 1.32 V ± 2%
Supply voltage V_{EE} . . . . . −3.2 V ± 2%
Reference voltage V_{BB} . . . . . 0 V (GND)
Reverse bias on unused ECL inputs . . . . . −1 V ± 0.5 V
Low-level bias on unused HLL inputs . . . . . 0 V (GND)
Normalized d-c fan-out: ECL2536 . . . . . 0 to 35
ECL2537 . . . . . 0 to 8 loads, each requiring 1.6 mA
Load on each output: ECL2536 . . . . . characterized at 270 Ω to V_{EE}, 50 Ω to GND
ECL2537 . . . . . characterized at 300 Ω to V_{EE}
Operating free-air temperature range . . . . . 0°C to 75°C

NOTES: 1. Absolute maximum ratings are limits beyond which the life of individual devices may be impaired and are never to be exceeded in service or testing.
2. Maximum terminal conditions must be considered as mutually exclusive.
3. All voltages are referenced to V_{BB}, which is at GND.

ECL2536 electrical characteristics using HLL inputs

PARAMETER		TEST FIGURE	TEST CONDITIONS* TERMINALS (SEE NOTE 4) INPUTS	OUTPUTS Y	OUTPUTS Z	INPUT CONDITIONS: INPUT UNDER TEST, V_I	INPUT CONDITIONS: HLL INPUT OF OTHER GATE	T_A	MIN (SEE NOTE 5)	TYP (SEE NOTE 5)	MAX (SEE NOTE 5)	UNIT
V_{IH}	High-level input voltage		14					0°C	1.05		4.5	V
								25°C	1.05		4.5	
			12					75°C	1.05		4.5	
V_{IL}	Low-level input voltage		14					0°C	−1		0.65	V
								25°C	−1		0.65	
			12					75°C	−1		0.65	
$V_{OH(Y)}$	High-level output voltage at OR output	2	14	2		1.2 V	0 V	0°C	315	410		mV
								25°C	350	450	525	
			12	8				75°C		520	600	
$V_{OL(Y)}$	Low-level output voltage at OR output	2	14	2		0.5 V	0 V	0°C	−505	−470		mV
								25°C	−505	−450	−350	
			12	8				75°C		−410	−310	
$V_{OH(Z)}$	High-level output voltage at NOR output	2	14		4	0.5 V	0 V	0°C	315	410		mV
								25°C	350	450	525	
			12		7			75°C		520	600	
$V_{OL(Z)}$	Low-level output voltage at NOR output	2	14		4	1.2 V	0 V	0°C	−505	−470		mV
								25°C	−505	−450	−350	
			12		7			75°C		−410	−315	
$V_{OH(Y)}$	High-level output voltage at OR output	2	14	2		1.05 V	0 V	0°C	315	410		mV
								25°C	350	450	525	
			12	8				75°C		520	600	
$V_{OL(Y)}$	Low-level output voltage at OR output	2	14	2		0.65 V	0 V	0°C	−505	−470		mV
								25°C	−505	−450	−350	
			12	8				75°C		−410	−310	
$V_{OH(Z)}$	High-level output voltage at NOR output	2	14		4	0.65 V	0 V	0°C	315	410		mV
								25°C	350	450	525	
			12		7			75°C		520	600	
$V_{OL(Z)}$	Low-level output voltage at NOR output	2	14		4	1.05 V	0 V	0°C	−505	−470		mV
								25°C	−505	−450	−350	
			12		7			75°C		−410	−315	
I_{IH}	High-level input current	3	14			2.8 V	0 V	0°C			220	μA
								25°C			200	
			12					75°C			170	
I_{IL}	Low-level input current	3	12, 14			0 V	0 V	0°C			220	μA
								25°C			200	
								75°C			170	
I_{C+}	Supply current from V_{C+}	4				Both HLL inputs at 2.4 V		25°C	10		17.5	mA
I_{CC}	Supply current from V_{CC}	4				Both HLL inputs at 2.4 V		25°C	9		16	mA
I_{EE}	Supply current from V_{EE}	4				Both HLL inputs at 2.4 V		25°C	−22		−38	mA
C_{in}	Input capacitance (see Note 6)		14					25°C		2		pF
			12									
z_{out}	Output impedance (see Note 7)			2	4			25°C		5		Ω
				8	7							

*ECL inputs (pins 11 and 16) biased to −0.5 V, V_{BB} (pins 1 and 9) = GND, V_{CC} (pins 3 and 6) = 1.32 V ± 1%, V_{EE} (pin 10) = −3.2 V ±1%, V_{C+} (pin 5) = 4.8 V ± 1%.

NOTES: 4. Each gate is tested separately unless otherwise noted. See referenced test figure for output terminations.

5. The algebraic convention where the most positive limit is designated as maximum is used in this data sheet for logic voltage levels only, e.g., if −350 mV is a maximum, the typical and minimum limits are more negative voltages.

6. C_{in} is measured using peak-current techniques. A square-wave input pulse is applied, and the input current waveform is integrated with respect to time to determine Q. C_{in} = Q/V.

7. Constant-current loads are used to determine the output impedance which is derived from the slope of a V_O vs I_O curve.

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ECL2536 electrical characteristics using ECL inputs

PARAMETER		TEST FIGURE	TEST CONDITIONS* TERMINALS (SEE NOTE 4) INPUTS	TERMINALS (SEE NOTE 4) OUTPUTS Y	TERMINALS (SEE NOTE 4) OUTPUTS Z	INPUT CONDITIONS: INPUT UNDER TEST, V_I	INPUT CONDITIONS: ECL INPUT OF OTHER GATE	T_A	MIN (SEE NOTE 5)	TYP (SEE NOTE 5)	MAX (SEE NOTE 5)	UNIT
V_{IH}	High-level input voltage		16					0°C	150		720	mV
								25°C	150		720	
			11					75°C	150		720	
V_{IL}	Low-level input voltage		16					0°C	−1500		−150	mV
								25°C	−1500		−150	
			11					75°C	−1500		−150	
$V_{OH(Y)}$	High-level output voltage at OR output	2	16	2		0.2 V	−0.5 V	0°C	315	410		mV
								25°C	350	450	525	
			11	8				75°C		520	600	
$V_{OL(Y)}$	Low-level output voltage at OR output	2	16	2		−0.2 V	−0.5 V	0°C	−505	−470		mV
								25°C	−505	−450	−350	
			11	8				75°C		−410	−310	
$V_{OH(Z)}$	High-level output voltage at NOR output	2	16		4	−0.2 V	−0.5 V	0°C	315	410		mV
								25°C	350	450	525	
			11		7			75°C		520	600	
$V_{OL(Z)}$	Low-level output voltage at NOR output	2	16		4	0.2 V	−0.5 V	0°C		−410		mV
								25°C		−390	−310	
			11		7			75°C		−350	−280	
$V_{OL(Z)}$	Low-level output voltage at NOR output	2	16		4	0.4 V	−0.5 V	0°C	−505	−470		mV
								25°C	−505	−450		
			11		7			75°C		−410	−315	
$V_{OH(Y)}$	High-level output voltage at OR output	2	11	8		0.15 V	−0.5 V	0°C	290			mV
								25°C	325			
								75°C				
$V_{OL(Y)}$	Low-level output voltage at OR output	2	11	8		−0.15 V	−0.5 V	0°C				mV
								25°C			−325	
								75°C			−290	
I_{IH}	High-level input current	3	16			0.5 V	−0.5 V	0°C			255	μA
								25°C			235	
			11					75°C			200	
I_{IL}	Low-level input current (both ECL inputs)	5	11, 16			Both ECL inputs at −3.2 V		0°C			−0.5	μA
								25°C			−0.5	
								75°C			−0.5	
I_{C+}	Supply current from V_{C+}	4				Both ECL inputs at −0.5 V		25°C	5		8.5	mA
I_{CC}	Supply current from V_{CC}	4				Both ECL inputs at −0.5 V		25°C	13		22	mA
I_{EE}	Supply current from V_{EE}	4				Both ECL inputs at −0.5 V		25°C	−20		−35	mA
C_{in}	Input capacitance (see Note 6)		16					25°C		5		pF
			11									
z_{out}	Output impedance (see Note 7)			2	4			25°C		5		Ω
				8	7							

*HLL inputs (pins 12 and 14) grounded, V_{BB} (pins 1 and 9) = GND, V_{CC} (pins 3 and 6) = 1.32 V ± 1%, V_{EE} (pin 10) = −3.2 V ± 1%, V_{C+} (pin 5) = 4.8 V ± 1%.

NOTES: 4. Each gate is tested separately unless otherwise noted. See referenced test figure for output termination.

5. The algebraic convention where the most positive limit is designated as maximum is used in this data sheet for logic voltage levels only, e.g., if −350 mV is a maximum, the typical and minimum limits are more negative voltages.

6. C_{in} is measured using peak-current techniques. A square-wave input pulse is applied, and the input current waveform is integrated with respect to time to determine Q. C_{in} = Q/V.

7. Constant-current loads are used to determine the output impedance which is derived from the slope of a V_O vs I_O curve.

ECL2537 electrical characteristics

PARAMETER (SEE NOTE 8)	TEST CONDITIONS*							MIN	TYP	MAX	UNIT
	TEST FIGURE	TERMINALS (SEE NOTE 4)		INPUT CONDITIONS			T_A	(SEE NOTE 5)			
		INPUTS	OUTPUTS Y Z	INPUT UNDER TEST, V_I	OTHER INPUT OF SAME GATE	INPUTS OF OTHER GATE					
V_{IH}		13, 14					0°C	150		720	mV
		11, 12					25°C	150		720	
							75°C	150		720	
V_{IL}		13, 14					0°C	−1500		−150	mV
		11, 12					25°C	−1500		−150	
							75°C	−1500		−150	
$V_{OH(Y)}$	6	13, 14	1	0.2 V	−0.5 V	−0.5 V	0°C	3	3.4		V
		11, 12	8				25°C	3.2	3.6		
							75°C		3.8		
$V_{OL(Y)}$	6	13, 14	1	−0.2 V	−0.5 V	−0.5 V	0°C	−0.8	−0.35		V
		11, 12	8				25°C	−0.7	−0.25	0.2	
							75°C		−0.15	0.3	
$V_{OH(Z)}$	6	13, 14	2	−0.2 V	−0.5 V	−0.5 V	0°C	3	3.4		V
		11, 12	7				25°C	3.2	3.6		
							75°C		3.8		
$V_{OL(Z)}$	6	13, 14	2	0.2 V	−0.5 V	−0.5 V	0°C	−0.7	−0.2		V
		11, 12	7				25°C	−0.6	−0.1	0.2	
							75°C		0.0	0.3	
$V_{OL(Z)}$	6	13, 14	2	0.4 V	−0.5 V	−0.5 V	0°C	−1	−0.35		V
		11, 12	7				25°C	−0.9	−0.25	0.2	
							75°C		−0.15	0.3	
$V_{OH(Y)}$	6	13, 14	1	0.15 V	−0.5 V	−0.5 V	0°C	2.9			V
		11, 12	8				25°C	3.1			
							75°C				
$V_{OL(Y)}$	6	13, 14	1	−0.15 V	−0.5 V	−0.5 V	0°C				V
		11, 12	8				25°C			0.3	
							75°C			0.4	
I_{IH}	7	13, 14		0.5 V	−0.5 V	−0.5 V	0°C			510	μA
		11, 12					25°C			470	
							75°C			400	
I_{IL} (all inputs)	8	11, 12, 13, 14		Both inputs of both gates in parallel at −3.2 V			0°C			−0.5	μA
							25°C			−0.5	
							75°C			−0.5	
I_{C+}	9			All inputs at −0.5 V			25°C	8		17	mA
I_{EE}	9			All inputs at −0.5 V			25°C	−8		−17	mA
C_{in} (see Note 6)		13, 14					25°C		5		pF
		11, 12									
z_{out} (see Note 7)			1 2				25°C		10		Ω
			8 7								

*V_{BB} (pins 9 and 16) = GND, V_{C+} (pin 5) = 4.8 V ± 1%, V_{EE} (pin 10) = −3.2 V ± 1%.

NOTES: 4. Each gate is tested separately unless otherwise noted. See referenced test figure for output termination.

5. The algebraic convention where the most positive limit is designated at maximum is used in this data sheet for logic voltage levels only, e.g., if −350 mV is a maximum, the typical and minimum limits are more negative voltages.

6. C_{in} is measured using peak-current techniques. A square-wave input pulse is applied, and the input current waveform is integrated with respect to time to determine Q. $C_{in} = Q/V$.

7. Constant-current loads are used to determine the output impedance which is derived from the slope of a V_O vs I_O curve.

8. See pages 4 or 5 for defining term associated with each symbol.

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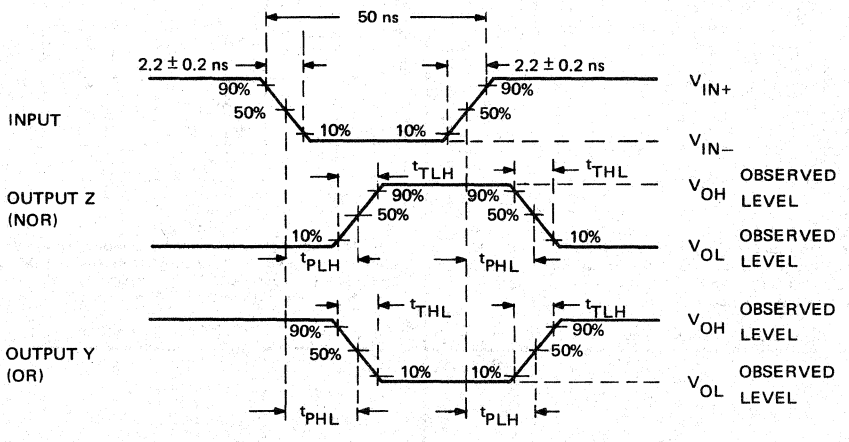
operating characteristics at specified free-air temperature (see figure 1)

TERMINALS TO BE TESTED (SEE NOTES 9, 10, and 11)				C_L	t_{PHL} and/or t_{PLH} PROPAGATION TIMES—ns									t_{THL} and/or t_{TLH} TRANSITION TIMES—ns								
					T_A = 0°C			T_A = 25°C			T_A = 75°C			T_A = 0°C			T_A = 25°C			T_A = 75°C		
INPUT	OUTPUT	INPUT	OUTPUT	pF	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
ECL2536 using HLL inputs (see figure 10)																						
14	2, 4	12	8, 7	4		4.0			2.8	3.9	5.5		4.0		3.9			2.5	4.0	6.5		4.2
				50		5.0			3.7	5.0	6.5		5.2		4.3			2.5	4.4	7		4.3
ECL2536 using ECL inputs (see figure 11)																						
16	2, 4	11	8, 7	4		2.5			1.3	2.4	3.7		2.5		4.1			2.5	4.0	6.5		4.1
				50		3.4			2.2	3.5	4.8		3.4		4.4			2.5	4.4	7		4.3
ECL2537 (see figure 12)																						
13 14	1, 2	11 12	8, 7	15		3.4			2.2	3.5	5		3.6		3.7			2.2	3.7	6.5		3.8



VOLTAGE WAVEFORMS

MODULE	V_{IN+} (V)	V_{IN-} (V)
ECL2536 (HLL)	1.40 ± 0.05	0 ± 0.05
ECL2536 (ECL)	0.40 ± 0.02	−0.50 ± 0.02
ECL2537	0.40 ± 0.05	−0.50 ± 0.05

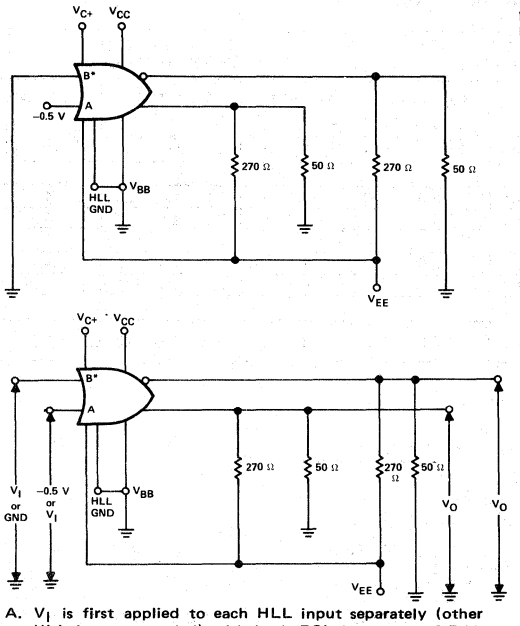
FIGURE 1—PROPAGATION DELAY AND TRANSITION TIMES

NOTES: 9. Each gate is tested separately.

10. The input pulse is measured as it is applied sequentially to each input of the gate under test and a waveform measurement is made at each of the outputs of that gate.

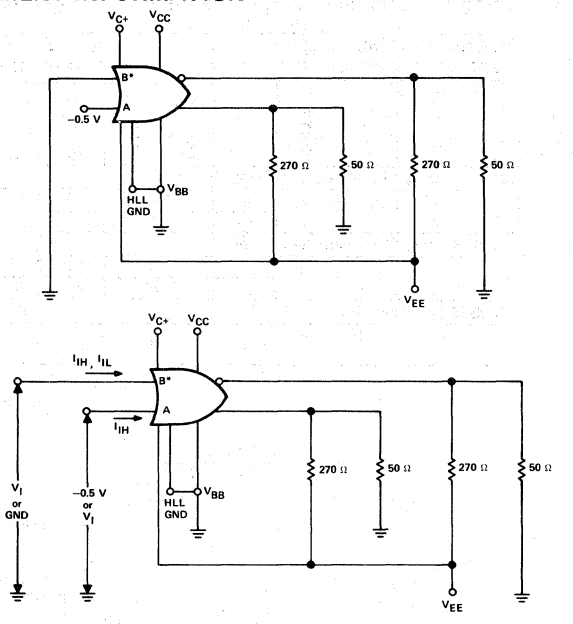
11. Bias voltages and loads for the gate under test are shown in Figures 10 through 12. Unused gates have inputs biased as shown in Figure 2 for the ECL2536 or Figure 6 for the ECL2537, outputs under load, and power applied.

PARAMETER MEASUREMENT INFORMATION†



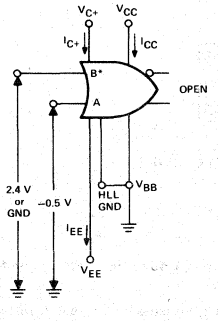
A. V_I is first applied to each HLL input separately (other HLL input grounded) with both ECL inputs at −0.5 V; then V_I is applied to each ECL input separately (other ECL input at −0.5 V) with both HLL inputs at ground.
B. Each output is tested separately.

FIGURE 2–V_{OH} AND V_{OL}



V_I is first applied to each HLL input separately (other HLL input grounded) with both ECL inputs at −0.5 V; then V_I is applied to each ECL input separately (other ECL input at −0.5 V) with both HLL inputs at ground.

FIGURE 3–I_{IH} AND I_{IL}



A. The supply currents are measured with both the HLL inputs first at 2.4 V, then at GND.
B. Both gates are tested simultaneously. I_{CC} is the total current into the two V_{CC} terminals.

FIGURE 4–I_{C+}, I_{CC}, AND I_{EE}

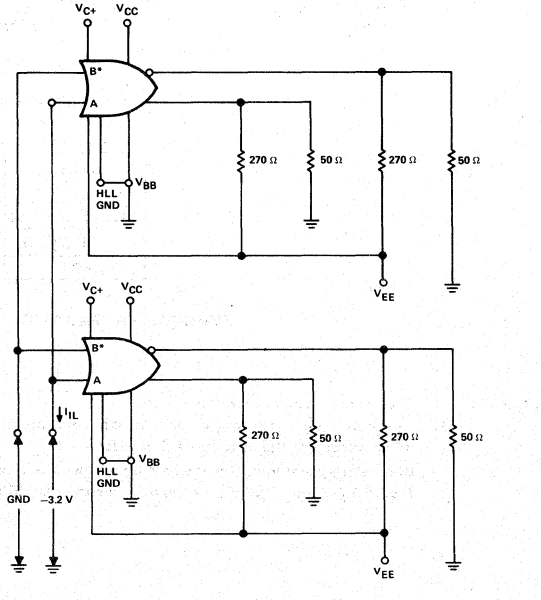


FIGURE 5–I_{IL}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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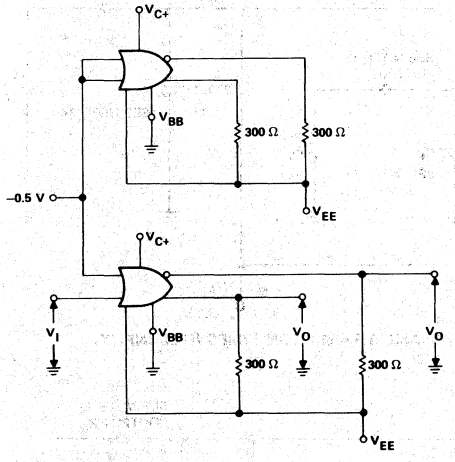
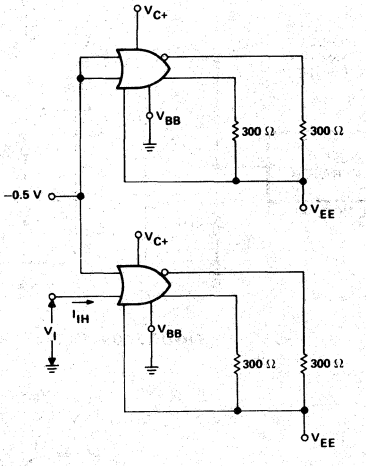
PARAMETER MEASUREMENT INFORMATION†



A. V_I is applied to each input separately.
B. Each output is tested separately.

FIGURE 6–V_{OH} AND V_{OL}



Each input is tested separately.

FIGURE 7–I_{IH}

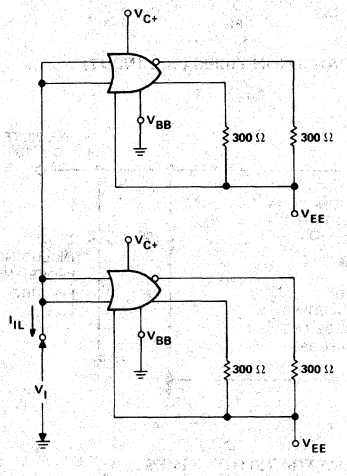
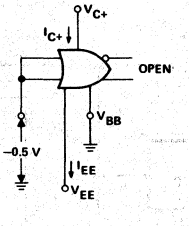


FIGURE 8–I_{IL}



Both gates are tested simultaneously.

FIGURE 9–I_{C+} OR I_{EE}

† Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

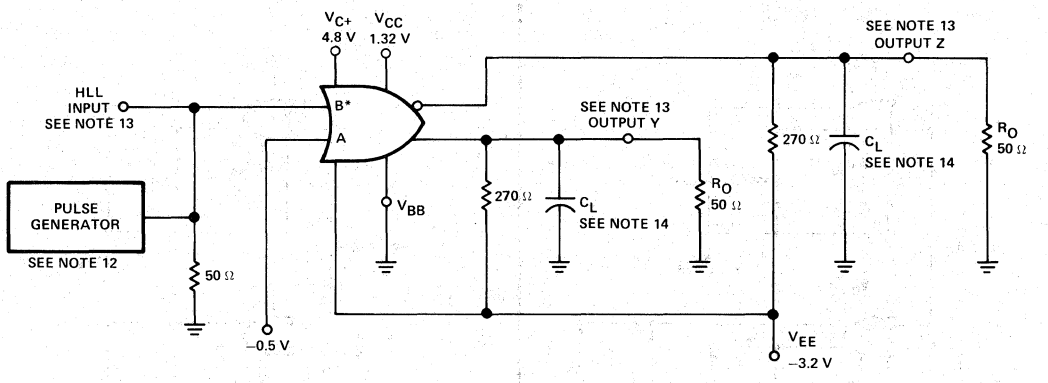


FIGURE 10—ECL2536 PROPAGATION DELAY AND TRANSITION TIMES (HLL INPUT)

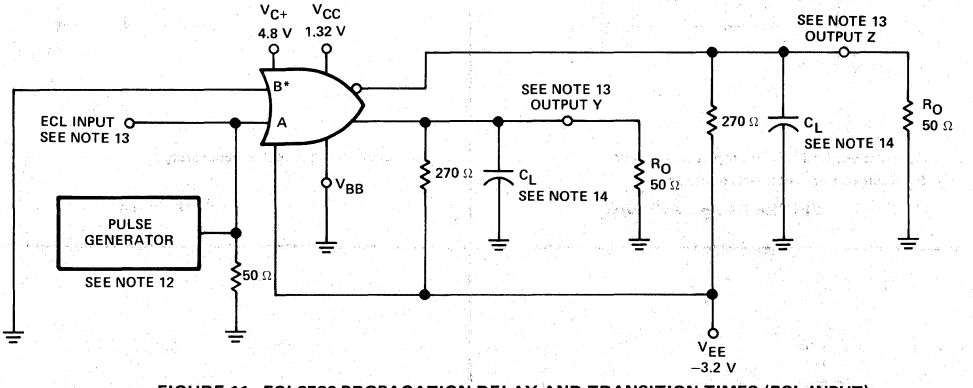


FIGURE 11—ECL2536 PROPAGATION DELAY AND TRANSITION TIMES (ECL INPUT)

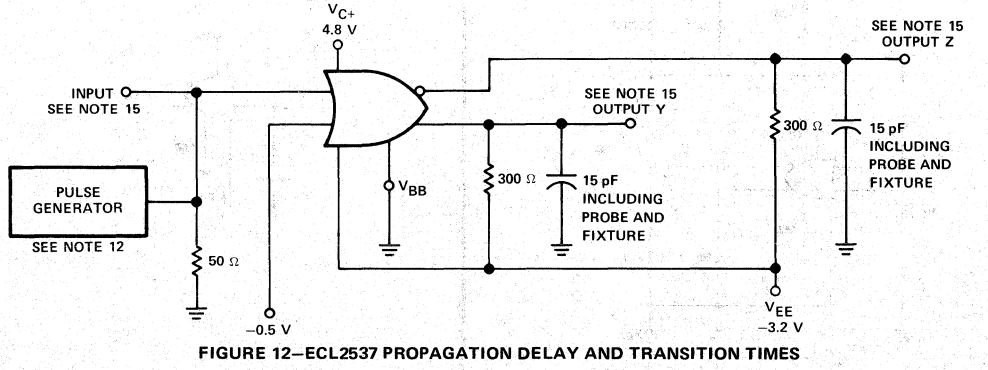


FIGURE 12—ECL2537 PROPAGATION DELAY AND TRANSITION TIMES

NOTES: 12. The generator has the following characteristics: Z_{out} = 50 Ω, PRR = 1 MHz. See waveform details in Figure 1.
13. The waveforms for ECL2536 are monitored on an oscilloscope with a rise time of less than or equal to 350 ps. Either a high-impedance probe with an input impedance of 100 kΩ paralleled by 2 pF, or a 50-Ω impedance system can be used. The 50-Ω resistors designated R_O are the oscilloscope input resistance in the 50-Ω system or discrete resistors with a high-impedance probe.
14. C_L includes probe and fixture capacitance. A capacitance of 50 pF can be used to approximate an a-c fan-out of 10.
15. The waveforms for ECL2537 are monitored on an oscilloscope with a rise time of less than or equal to 350 ps. A high-impedance probe with an input impedance of 100 kΩ paralleled by 2 pF is used.

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GENERAL APPLICATION INFORMATION

ECL2536

input conditions

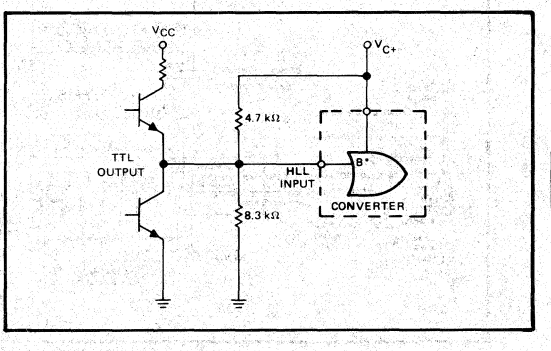
The ECL2536 converts high-level-logic inputs to ECL2500-logic-level outputs.

A control INHIBIT/ENABLE ECL input is provided to lock out data presented at the HLL input. A high-level (H) input voltage inhibits the converter outputs in a stable state such that signals on the HLL input are not transmitted through the converter. A low-level (L) input voltage enables the converter and the output levels are determined by the logic level of the HLL input.

The output feeding the HLL input should have an H level $\geq$ 1.2 V and an L level $\leq$ 0.5 V in order to maintain at least a 150-mV noise margin.

driving by TTL

The HLL input requires up to 220 μA of current to be supplied with both H-level and L-level voltage inputs. TTL outputs are designed to sink current in the low state, not to supply current. To assure reliable performance with all types of TTL circuits, it is recommended that a resistor divider be placed at the HLL input external to the package. The divider has 4.7 kΩ from the HLL input to V_{C+} and 8.3 kΩ to ground, as shown.



ECL output loading

General loading for fan-out from the ECL outputs may be divided into two classes:

CLASS I **Short-Line or Cluster Loading**
Loads which can be connected within two inches of any source can be treated as lumped capacitive loads which include the gate inputs and stub-line capacitances. Switching times can be interpolated accordingly. No two dotted outputs can be more than two inches apart for this case.

CLASS II **Long-Line or Distributive Loading**
These loads must be treated as lumped loads along a transmission line and termination should be at the end of the transmission chain. No more than 20 pF of load is recommended per 4.5 inches of 50-ohm printed line (with dielectric constant of 4.5) in order that the reflection coefficient be no greater than 20%. If the loads are lumped loads of 20 pF, they must be 4.5 inches apart. If individual gates and **CLASS I** loads are distributed, they must not exceed the 20 pF per 4.5 inches of line.

ECL2537

The ECL2537 converts ECL2500-logic-level inputs to high-level-logic outputs.

An external pull-down resistor to a negative voltage must be provided on the HLL output terminals. The size of the resistor is determined by the current it must sink in order to maintain the correct low-level voltage with the DTL or TTL fan-out being driven.

Characterization is with a pull-down resistor of 300 Ω to -3.2 V which represents a fan-out of five Texas Instruments Series 54/74 TTL logic gates.

No wired-OR connection is allowed on the HLL outputs because an emitter-follower junction breakdown may occur if one converter output is high and this forces another output to be high which would otherwise be low.

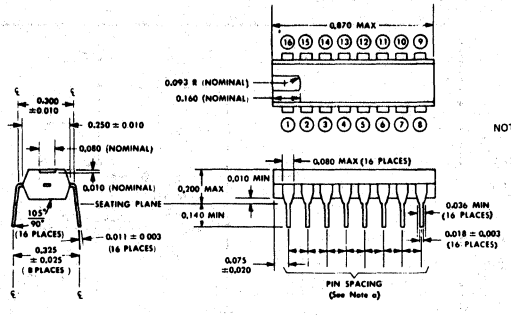
The V_{C+} power supply must be held at 4.8 V $\pm$ 1%. Otherwise, the output voltage specifications for maximum V_{OL} or minimum V_{OH} may be exceeded.

mechanical data

The circuit bars are mounted on a 16-lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperatures with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. This package is intended for insertion in mounting-hole rows on 0.300-inch centers. Once the leads are compressed to 0.300-inch separation and inserted, sufficient tension is provided to secure the package in the board during soldering. Silver-plated leads require no additional cleaning or processing when used in soldered assembly.

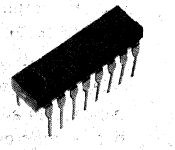
The plastic case is electrically nonconductive.

16-PIN PLASTIC DUAL-IN-LINE PACKAGE OUTLINE



NOTES: a. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within 0.010 of its true longitudinal position relative to pins 1 and 16.

b. All dimensions are in inches unless otherwise noted.



terminal designations

Pin assignments are shown in the table below and correspond to the logic diagrams on page 2.
Outputs are denoted Y or Z. Inputs are denoted A, B, or B*.
Respective inputs and outputs are identified by a gate number preceding the pin symbol.
Power is supplied via the V_{C+}, V_{CC}, V_{EE}, and V_{BB} terminals.
V_{BB} is a reference voltage.
NC indicates no internal connection.

PIN ASSIGNMENTS

PIN	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
ECL2536	V_{BB}	1Y	V_{CC}	1Z	V_{C+}	V_{CC}	2Z	2Y	V_{BB}	V_{EE}	2A	2B*	HLL GND	1B*	NC	1A
ECL2537	1Y	1Z	NC	NC	V_{C+}	NC	2Z	2Y	V_{BB}	V_{EE}	2A	2B	1A	1B	NC	V_{BB}

*HLL input

Multiple V_{CC} terminals have been supplied to reduce cross-talk noise. Multiple V_{BB} terminals are also provided. All V_{BB} and V_{CC} terminals should be connected even if all gates in the module are not used.

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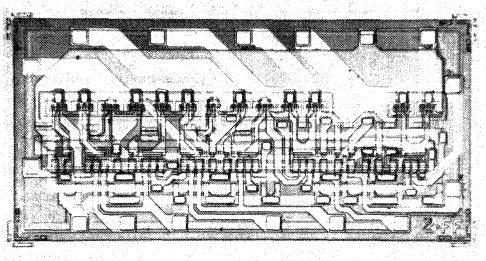
ECL2500 SERIES EMITTER-COUPLED-LOGIC (ECL) BISTABLE MODULES FOR APPLICATION IN ULTRA-HIGH-SPEED DIGITAL SYSTEMS

description



The ECL2500 series is a compatible family of ECL functions with basic gate delays of 2 to 3 ns per stage. The family is specifically designed for operation from 0°C to 70°C.

The ECL2500 family includes:

- Basic Gate Modules
- Multifunction Gate Modules
- **Bistable Modules**
- Arithmetic Modules
- Interface Modules
- Memory Module

family features

- High speed . . . typical gate propagation delay time of 2.5 ns
- Complementary OR/NOR outputs with capability for wired-OR connections
- Designed for use with transmission lines to ensure maximum signal transmission without noise. Characterized for 50-ohm lines
- High noise immunity: ±225 mV typical at 25°C

This data sheet covers the bistable modules.
Separate data sheets cover the balance of the ECL2500 modules.

ECL2500 series bistable modules

The ECL2500 series bistable modules are summarized in the table below. These modules contain the ECL circuits shown in the schematics of Figures A, B, and C on pages 6 and 7. Logic diagrams of ECL2540 through ECL2542 are shown on page 4.

SUMMARY OF BISTABLE MODULES

MODULE	GATES PER MODULE	LATCHES PER MODULE	OUTPUTS PER BISTABLE CIRCUIT	
			Q (LATCH)	$\overline{Q}$ (LATCH COMPLEMENT)
ECL2540	4	2	1	1
ECL2541	9	2	1	2
ECL2542	13	2		1

APPLICATION INFORMATION

general

The bistable modules specified in this data sheet contain dual latches. Each half of the ECL2540 is a latch with a separate data input. Two clock inputs, C and C′, feed both latches. Q and $\overline{Q}$ outputs are provided from each latch. Each half of the ECL2541 is a latch with additional circuitry which provides a data input and a gate input to control the input data. Common clock, set, and reset inputs are included. One Q and two $\overline{Q}$ outputs are provided for each latch. Each half of the ECL2542 is a latch with additional circuitry which provides two data inputs each with a gate input to control the input data. Common clock, set, and reset inputs serve both latches. Only $\overline{Q}$ outputs are provided.

Each latch has the possibility to operate in the following modes:

Register — The mode in which the data input controls the state of the latch. Q is high when data is high.

Storage — The mode in which the latch stores data received during the register mode. Input data is locked out from changing the latch state.

Set — The mode whereby Q is set high (or $\overline{Q}$ low) which is normally done when the clock is high.

Reset — The mode whereby Q is set low (or $\overline{Q}$ high) which is normally done when the clock is high (low for ECL2540).

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The ECL2541 and ECL2542 have the register mode subdivided:

Register Mode/Clock Control — The mode whereby the gate input is low, allowing the data to set the latch when the clock goes low.

Register Mode/Gate Control — The mode whereby the clock input is low, allowing the data to set the latch when the gate is low.

Each Q and $\overline{Q}$ output must be terminated in a pull-down resistor.

The Q terminal of the ECL2541 must have a termination resistor (in addition to the pull-down resistor) on the output at all times (whether the output is used for fan-out or not), because internal feedback occurs from this point.

For full-temperature-range operation of all devices, data must be present before the clock pulse and the minimum width of the clock pulse is 4.5 ns. For the ECL2541 and ECL2542, the data pulse must extend beyond the clock pulse to allow for the delay associated with the clock-buffering gate.

For the ECL2540, latching occurs on either the leading or trailing edge of the C or C′ pulse. For the ECL2541 and ECL2542, latching occurs on the leading edge of the clock pulse.

Multiple V_{CC} terminals have been supplied to reduce crosstalk noise. All V_{CC} terminals should be connected even if all gates in a module are not used.

General loading for fan-out may be divided into two classes:

CLASS I **Short-Line or Cluster Loading.**
Loads which can be connected within two inches of any source can be treated as lumped capacitive loads which include the gate inputs and stub-line capacitances. Switching times can be interpolated accordingly. No two dotted outputs can be more than two inches apart for this case.

CLASS II **Long-Line or Distributive Loading.**
These loads must be treated as lumped loads along a transmission line and termination should be at the end of the transmission chain. No more than 20 pF of load is recommended per 4.5 inches of 50-ohm printed line (with dielectric constant of 4.5) in order that the reflection coefficient be no greater than 20%. If the loads are lumped loads of 20 pF, they must be 4.5 inches apart. If individual gates and **CLASS I** loads are distributed, they must not exceed the 20 pF per 4.5 inches of line.

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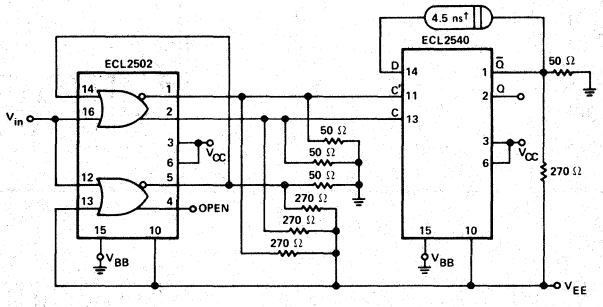
APPLICATION INFORMATION

ECL2540

The ECL2540 requires two clock inputs. Faulty operation occurs if the C′ input lags behind C by more than 0.5 ns. The interval between the transition of the two clocks is referred to as skew. C′ can be skewed ahead of C by as much as 1.5 ns.

The ECL2540 can be used as a toggle as shown in Figure 1. However, the delay from $\overline{Q}$ to D must be greater than the clock pulse width. Thus, when pulse widths are very long, this becomes impractical unless a technique such as that shown in Figure 1 is used. This technique uses two gates of an ECL2502 as a pulse-shaping network to allow operation of a toggle from 100 megacycles per second down to cycles per second.



†Delay between $\overline{Q}$ and D must be greater than 4.5 ns based on the propagation delay characteristics of the ECL2502 and its feedback loop.

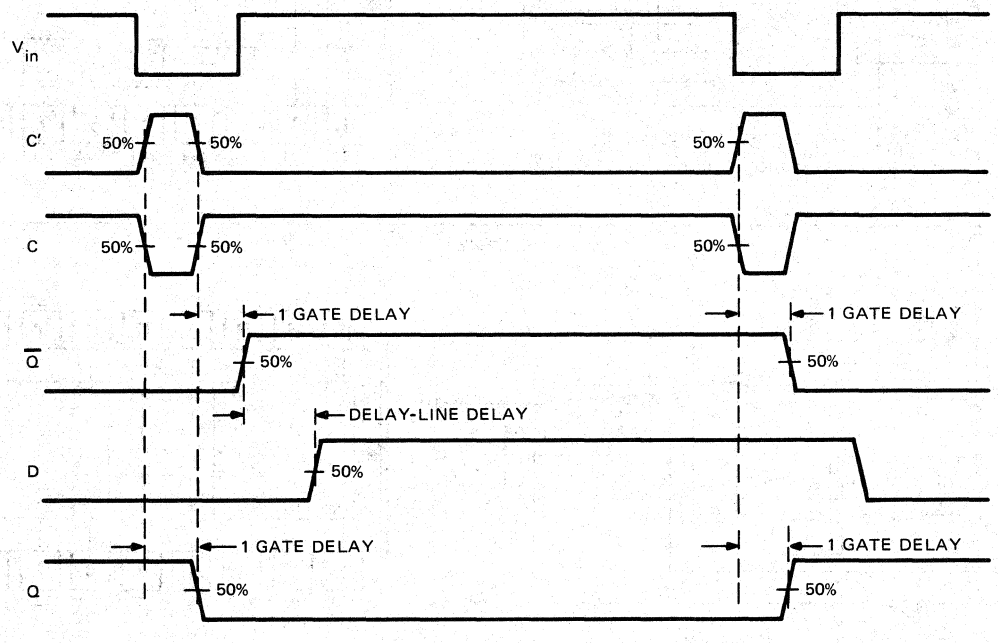
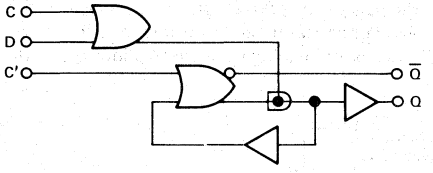


FIGURE 1—ECL2540 USED AS A TOGGLE (WITHOUT SKEW)

TYPES ECL2540 THRU ECL2542
EMITTER-COUPLED-LOGIC BISTABLE MODULES

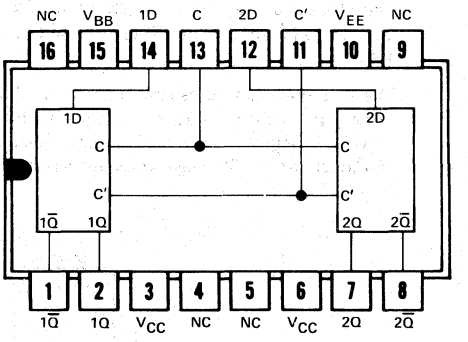
logic†

ECL2540

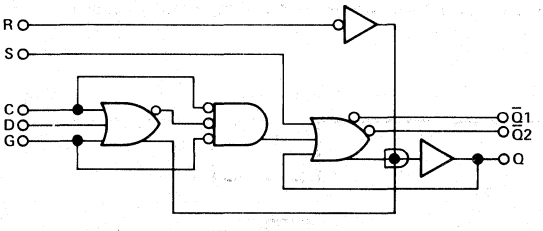


$$Q_{n+1} = (C+D)(Q_n+C')$$
$$\overline{Q}_{n+1} = (\overline{C}\,\overline{D}+\overline{Q}_n)\overline{C'}$$

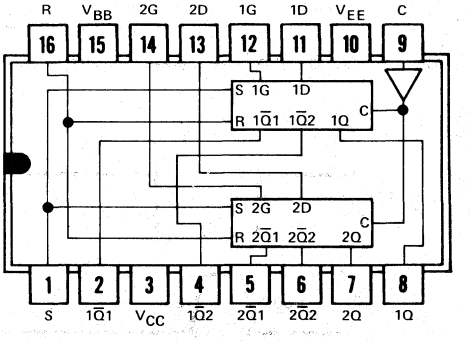
NC—No internal connection



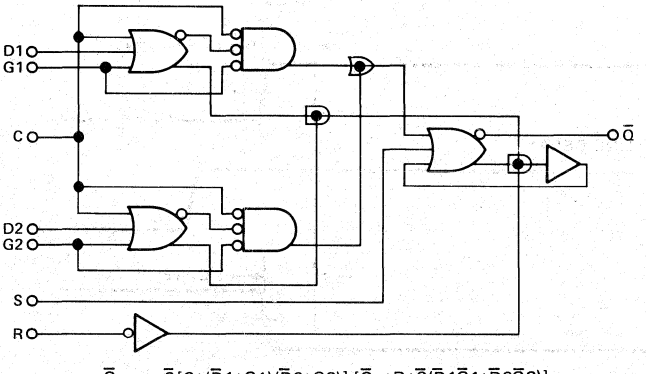
ECL2541



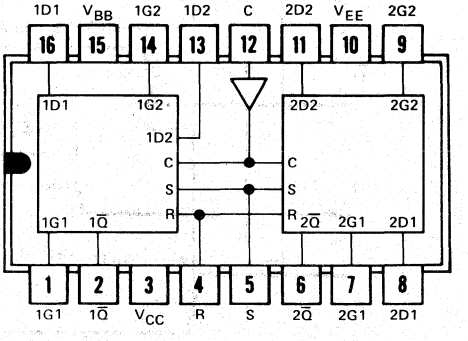
$$Q_{n+1} = \overline{R}[(C+D+G)(Q_n+S)+\overline{C}D\overline{G}]$$
$$\overline{Q}_{n+1} = \overline{S}(C+\overline{D}+G)(\overline{Q}_n+R+\overline{C}\overline{D}\overline{G})$$



ECL2542



$$\overline{Q}_{n+1} = \overline{S}[C+(\overline{D}1+G1)(\overline{D}2+G2)]\,[\overline{Q}_n+R+\overline{C}(\overline{D}1\overline{G}1+\overline{D}2\overline{G}2)]$$



†One half of each bistable module is shown in the logic diagrams.

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truth tables (for this series, H = positive voltage, L = negative voltage, X = irrelevant)

ECL2540

MODE	INPUTS			OUTPUTS	
	CLOCK		DATA	LATCH	LATCH COMPLEMENT
	C	C′	D	Q_{n+1}	$\overline{Q}_{n+1}$
Register	L	H	H	H	L
	L	H	L	L	(L)†
Clock-controlled storage	H	L	X	Q_n	$\overline{Q}_n$
Set	H	H	X	H	L
Reset	L	L	L	L	H
Forbidden (see Note 1)	L	L	H	Q_n	$\overline{Q}_n$

ECL2541

MODE	INPUTS					OUTPUTS	
	SET	RESET	CLOCK	GATE	DATA	LATCH	LATCH COMPLEMENT
	S	R	C	G	D	Q_{n+1}	$\overline{Q}_{n+1}$
Register	L	L	L	L	H	H	L
	L	L	L	L	L	L	H
Clock-controlled storage	L	L	H	X	X	Q_n	$\overline{Q}_n$
Gate-controlled storage	L	L	X	H	X	Q_n	$\overline{Q}_n$
Set	H	L	H	X	X	H	L
	H	L	X	H	X	H	L
Reset	L	H	H	X	X	L	H
	L	H	X	H	X	L	H
Forbidden	H	L	L	L	H	H	L
	H	L	L	L	L	L	L
	L	H	L	L	H	L	L
	L	H	L	L	L	L	H
	H	H	X	X	X	L	L

ECL2542

MODE	INPUTS							OUTPUT
	SET	RESET	CLOCK	GATE		DATA		LATCH COMPLEMENT
	S	R	C	G1	G2	D1	D2	$\overline{Q}_{n+1}$
Register	L	L	L	H	L	X	D2	$\overline{D2}$
	L	L	L	L	H	D1	X	$\overline{D1}$
	L	L	L	L	L	D1	D2	$\overline{D1 + D2}$
Clock-controlled storage	L	L	H	X	X	X	X	$\overline{Q}_n$
Gate-controlled storage	L	L	X	H	H	X	X	$\overline{Q}_n$
Set	H	L	H	X	X	X	X	L
	H	L	X	H	H	X	X	L
Reset	L	H	H	X	X	X	X	H
	L	H	X	H	H	X	X	H
Forbidden	H	L	L	L	X	X	X	See Note 2
	H	L	L	X	L	X	X	
	L	H	L	L	X	X	X	
	L	H	L	X	L	X	X	
	H	H	X	X	X	X	X	

†$\overline{Q}$ is made low by C′ being high. When C′ returns to its normal state (low) following the clock pulse, $\overline{Q}$ goes high (the complement of data).

NOTES: 1. This condition is data-controlled storage, whereas only clock-controlled storage is desired in the ECL2540. Hence, this condition is placed in the forbidden category.

2. The forbidden input combinations for ECL2542 may produce pseudo-stable output states which do not persist when a storage mode is subsequently selected or may produce outputs not in harmony with the normally used input patterns.

schematics

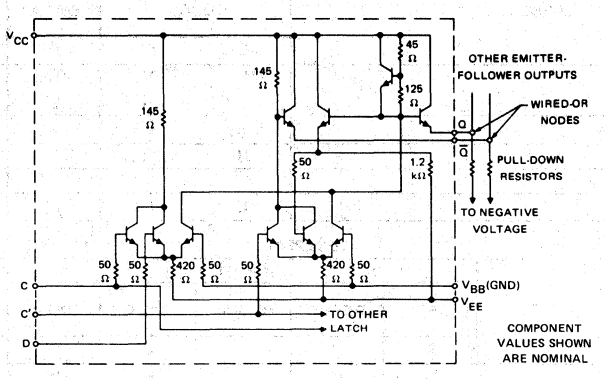

FIGURE A–SCHEMATIC OF HALF OF ECL2540

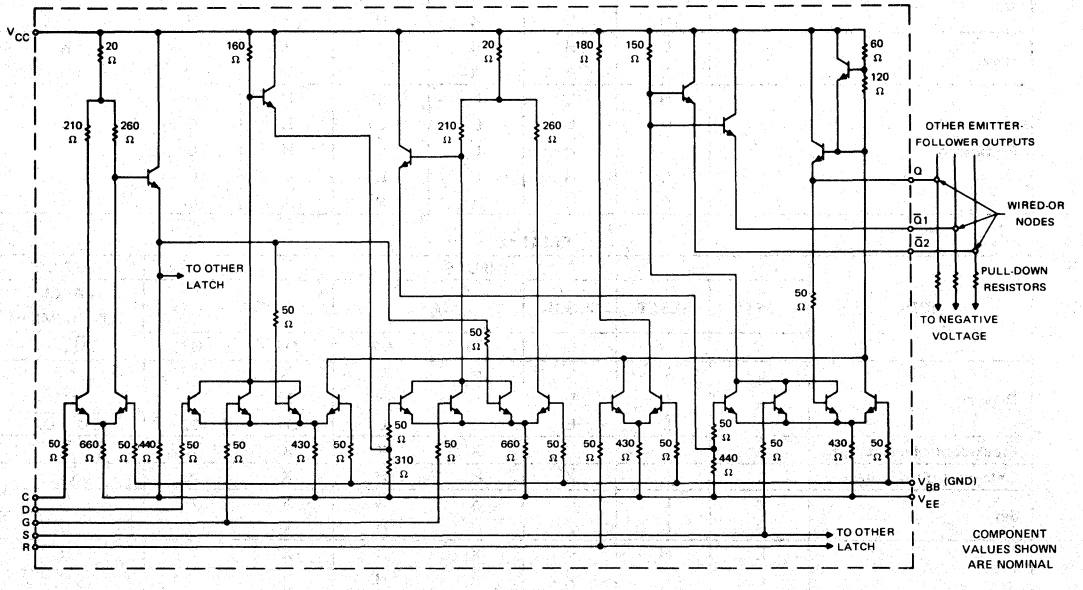

FIGURE B–SCHEMATIC OF HALF OF ECL2541

Emitter-follower outputs require an external pull-down resistor. The wired-OR function can be obtained by connecting the emitter-follower outputs of a bistable module to the emitter-follower outputs of other gates or other bistable modules. Only one pull-down resistor is required for each wire-OR node.

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schematic

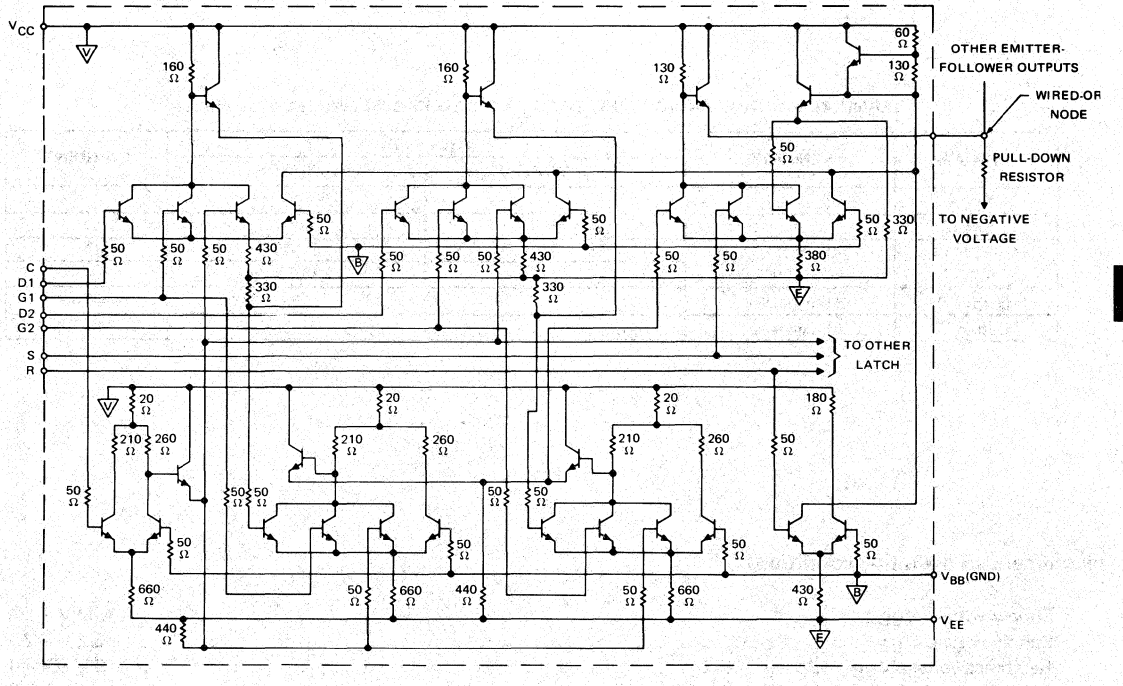

FIGURE C–SCHEMATIC OF HALF OF ECL2542

COMPONENT VALUES SHOWN ARE NOMINAL

▽ –V_{CC} bus
▽ –V_{BB} bus
▽ –V_{EE} bus (substrate)

4

absolute maximum ratings (see note 3)

Terminal voltages and currents . . . . . See table below
Storage temperature range . . . . . −40°C to 150°C
Free-air temperature range with supply and bias voltages applied . . . . . −40°C to 100°C

TERMINAL VOLTAGE AND/OR CURRENT, T_A = 0°C TO 75°C (SEE NOTES 4 AND 5)

TERMINAL	REMARKS	VOLTAGE		CURRENT
		CONTINUOUS	20-μs SURGE	
V_{CC}		2 V	4.5 V	
V_{EE}		−4 V	−7 V	
Each Input	All other inputs open	−3.5 V	−4 V	
		2 V	2 V	
Output Q	At high level			−40 mA
Output $\overline{Q}$	At high level			−40 mA

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recommended operating conditions

Supply voltage V_{CC} . . . . . 1.32 V ± 2%
Supply voltage V_{EE} . . . . . −3.2 V ± 2%
Reference voltage V_{BB} . . . . . 0 V (GND)
Reverse bias on unused inputs . . . . . −1 V ± 0.5 V
Normalized d-c fan-out . . . . . 0 to 35
Load on each output . . . . . characterized at 270 Ω to V_{EE}, 50 Ω to GND
Operating free-air temperature range . . . . . 0°C to 75°C

NOTES: 3. Absolute maximum ratings are limits beyond which the life of individual devices may be impaired and are never to be exceeded in service or testing.
4. Maximum terminal conditions must be considered as mutually exclusive.
5. All voltages are referenced to V_{BB}, which is at GND.

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ECL2540 electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS*										UNIT
		TEST FIGURE	INITIAL CONDITIONS (SEE TABLE I)	VOLTAGE AT INPUT UNDER TEST	INPUT(S) UNDER TEST	OTHER INPUT TERMINALS 0.5 V	OTHER INPUT TERMINALS −0.5 V	OUTPUT TERMINAL Q	OUTPUT TERMINAL $\bar{Q}$	T_A	MIN TYP MAX (SEE NOTE 6)	
V_{IH}	High-level input voltage									0°C 25°C 75°C	150 720 150 720 150 720	mV
V_{IL}	Low-level input voltage									0°C 25°C 75°C	−1500 −150 −1500 −150 −1500 −150	mV
$V_{OH(Q)}$	High-level output voltage at Q output, register mode	4	X	0.2 V	14 12	11 11	13 13	2 7		0°C 25°C 75°C	280 315	mV
$V_{OL(Q)}$	Low-level output voltage at Q output, register mode	4	X	−0.2 V	14 12	11 11	13 13	2 7		0°C 25°C 75°C	−330 −210	mV
$V_{OH(Q)}$	High-level output voltage at Q output, storage mode	4	S	0.2 V	13 13		11, 14 11, 12	2 7		0°C 25°C 75°C	280 365 315 400 500 470 580	mV
$V_{OL(Q)}$	Low-level output voltage at Q output, storage mode	4	R	−0.2 V	11 11	13, 14 13, 12		2 7		0°C 25°C 75°C	−505 −440 −480 −400 −330 −280 −210	mV
$V_{OH(\bar{Q})}$	High-level output voltage at $\bar{Q}$ output, storage mode	4	R	−0.2 V	11 11	13, 14 13, 12			1 8	0°C 25°C 75°C	280 365 315 400 500 470 580	mV
$V_{OL(\bar{Q})}$	Low-level output voltage at $\bar{Q}$ output, storage mode	4	S	0.2 V	13 13		11, 14 11, 12		1 8	0°C 25°C 75°C	−505 −440 −490 −425 −350 −390 −315	mV
$V_{OH(Q)}$	High-level output voltage at Q output, set mode	4	R	0.2 V	11, 13 11, 13		14 12	2 7		0°C 25°C 75°C	280 315	mV
$V_{OL(Q)}$	Low-level output voltage at Q output, reset mode	4	S	−0.2 V	11, 13 11, 13		14 12	2 7		0°C 25°C 75°C	−330 −210	mV
I_{IH}	High-level input current	5	X	0.5 V	14 12		11, 12, 13 11, 13, 14			0°C 25°C 75°C	255 235 200	μA
			X	0.5 V	11 13		12, 13, 14 11, 12, 14			0°C 25°C 75°C	510 470 400	μA
I_{IL}	Low-level input current	6	X	All inputs in parallel at −3.2 V						0°C 25°C 75°C	−0.5 −0.5 −0.6	μA
I_{CC} or $-I_{EE}$	Supply current	7	X	All inputs in parallel at −0.5 V						25°C	20 34	mA
C_{in}	Input capacitance (see Note 7)		X		Each					25°C	5	pF
Z_{out}	Output impedance (see Note 8)		X					2, 7	1, 8	25°C	5	Ω

NOTES: 6. The algebraic convention where the most-positive limit is designated as maximum is used in this data sheet for logic voltage levels only, e.g., if −350 mV is a maximum, the typical and minimum limits are more-negative voltages.

7. C_{in} is measured using peak-current techniques. A square-wave input pulse is applied, and the input current waveform is integrated with respect to time to determine Q. C_{in} = Q/V. When a terminal is an input to more than one gate, multiply the value given by the number of gates to which this terminal is an input.

8. Constant-current loads are used to determine the output impedance which is derived from the slope of a V_O vs I_O curve.

TABLE I—INITIAL CONDITIONS

Several of the parameters require the application of conditions which cause the outputs to assume definite states prior to applying test conditions specified above.

SYMBOL	DESCRIPTION	INPUT TERMINALS* 0.5 V	INPUT TERMINALS* −0.5 V
X	Irrelevant		
S	Set 1Q and 2Q high, $1\bar{Q}$ and $2\bar{Q}$ low	11, 13	14, 12
R	Reset 1Q and 2Q low, $1\bar{Q}$ and $2\bar{Q}$ high		11, 12, 13, 14

*V_{BB} (pin 15) = GND, V_{CC} (pins 3 and 6) = 1.32 V, V_{EE} (pin 10) = −3.2 V. Input and output terminals are open except as specified in these tables and in the d-c test figures.

ECL2541 electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS*								MIN	TYP	MAX	UNIT
		TEST FIGURE	INITIAL CONDITIONS (SEE TABLE II)	VOLTAGE AT INPUT UNDER TEST	INPUT(S) UNDER TEST	OTHER INPUT TERMINALS 0.5 V	OTHER INPUT TERMINALS −0.5 V	OUTPUT TERMINAL Q	OUTPUT TERMINAL $\overline{Q}$	T_A	(SEE NOTE 6)			
V_{IH}	High-level input voltage									0°C 25°C 75°C	150 150 150		720 720 720	mV
V_{IL}	Low-level input voltage									0°C 25°C 75°C	−1500 −1500 −1500		−150 −150 −150	mV
$V_{OH(Q)}$	High-level output voltage at Q output, register mode	4	X	0.2 V	11		1, 9, 12, 16	8		0°C 25°C 75°C	280 315			mV
					13		1, 9, 14, 16	7						
				−0.2 V	12	11	1, 9, 16	8						
					14	13	1, 9, 16	7						
				−0.2 V	9	11	1, 12, 16	8						
					9	13	1, 14, 16	7						
$V_{OL(Q)}$	Low-level output voltage at Q output, register mode	4	X	−0.2 V	11		1, 9, 12, 16	8		0°C 25°C 75°C			−330 −210	mV
					13		1, 9, 14, 16	7						
				−0.2 V	12		1, 9, 11, 16	8						
					14		1, 9, 13, 16	7						
				−0.2 V	9		1, 11, 12, 16	8						
					9		1, 13, 14, 16	7						
$V_{OH(Q)}$	High-level output voltage at Q output, storage mode	4	S	0.2 V	12		1, 9, 11, 16	8		0°C 25°C 75°C	280 315	365 400 470	500 580	mV
					14		1, 9, 13, 16	7						
				0.2 V	9		1, 11, 12, 16	8						
					9		1, 13, 14, 16	7						
$V_{OL(Q)}$	Low-level output voltage at Q output, storage mode	4	R	0.2 V	12	11	1, 9, 16	8		0°C 25°C 75°C	−505 −480	−440 −400 −280	−330 −210	mV
					14	13	1, 9, 16	7						
				0.2 V	9	11	1, 12, 16	8						
					9	13	1, 14, 16	7						
$V_{OH(\overline{Q})}$	High-level output voltage at $\overline{Q}$ output, storage mode	4	R	0.2 V	12	11	1, 9, 16		2, 4	0°C 25°C 75°C	280 315	365 400 470	500 580	mV
					14	13	1, 9, 16		5, 6					
				0.2 V	9	11	1, 12, 16		2, 4					
					9	13	1, 14, 16		5, 6					
$V_{OL(\overline{Q})}$	Low-level output voltage at $\overline{Q}$ output, storage mode	4	S	0.2 V	12		1, 9, 11, 16		2, 4	0°C 25°C 75°C	−505 −490	−440 −425 −390	−350 −315	mV
					14		1, 9, 13, 16		5, 6					
				0.2 V	9		1, 11, 12, 16		2, 4					
					9		1, 13, 14, 16		5, 6					
$V_{OH(Q)}$	High-level output voltage at Q output, set mode	4	R	0.2 V	1	9	16	8		0°C 25°C 75°C	280 315			mV
					1	9	16	7						
$V_{OL(Q)}$	Low-level output voltage at Q output, reset mode	4	S	0.2 V	16	9	1	8		0°C 25°C 75°C			−330 −210	mV
					16	9	1	7						

(Continued on page 11)

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ECL2541 electrical characteristics at specified free-air temperature (continued)

PARAMETER		TEST CONDITIONS*								MIN	TYP	MAX (SEE NOTE 6)	UNIT
		TEST FIGURE	INITIAL CONDITIONS (SEE TABLE II)	VOLTAGE AT INPUT UNDER TEST	INPUT(S) UNDER TEST	OTHER INPUT TERMINALS 0.5 V	OTHER INPUT TERMINALS −0.5 V	OUTPUT TERMINAL Q	OUTPUT TERMINAL $\overline{Q}$	T_A			
I_{IH}	High-level input current	5	X	0.5 V	9		1, 11, 12 13,14,16			0°C		255	μA
					11		1, 9, 12, 13, 14, 16			25°C		235	
					13		1, 9, 11, 12, 14, 16			75°C		200	
					1		9, 11, 12 13, 14, 16			0°C		510	μA
					12		1, 9, 11 13, 14, 16			25°C		470	
					14		1, 9, 11 12, 13, 16			75°C		400	
					16		1, 9, 11 12, 13, 14						
I_{IL}	Low-level input current	6	X	All inputs in parallel at −3.2 V						0°C		−0.6	μA
										25°C		−0.8	
										75°C		−1.1	
I_{CC} or $-I_{EE}$	Supply current	7	X	All inputs in parallel at −0.5 V						25°C	60	124	mA
C_{in}	Input capacitance (see Note 7)		X		Each					25°C		5	pF
Z_{out}	Output impedance (see Note 8)		X					7, 8	2, 4, 5, 6	25°C		5	Ω

*V_{BB} (pin 15) = GND, V_{CC} (pin 3) = 1.32 V, V_{EE} (pin 10) = −3.2 V. Input and output terminals are open except as specified in these tables and in the d-c test figures.

NOTES:
6. The algebraic convention where the most-positive limit is designated as maximum is used in this data sheet for logic voltage levels only, e.g., if −350 mV is a maximum, the typical and minimum limits are more-negative voltages.
7. C_{in} is measured using peak-current techniques. A square-wave input pulse is applied, and the input current waveform is integrated with respect to time to determine Z. C_{in} = Q/V. When a terminal is an input to more than one gate, multiply the value given by the number of gates to which this terminal is an input.
8. Constant-current loads are used to determine the output impedance which is derived from the slope of a V_O vs I_O curve.

TABLE II—INITIAL CONDITIONS

Several of the parameters require the application of conditions which cause the outputs to assume definite states prior to applying test conditions specified above.

SYMBOL	DESCRIPTION	INPUT TERMINALS* 0.5 V	INPUT TERMINALS* −0.5 V
X	Irrelevant		
S	Set 1Q and 2Q high, 1$\overline{Q}$1, 1$\overline{Q}$2, 2$\overline{Q}$1, and 2$\overline{Q}$2 low	1, 9	16
R	Reset 1Q and 2Q low, 1$\overline{Q}$1, 1$\overline{Q}$2, 2$\overline{Q}$1, and 2$\overline{Q}$2 high	9, 16	1

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ECL2542 electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS*							T_A	MIN	TYP	MAX	UNIT
		TEST FIGURE	INITIAL CONDITIONS (SEE TABLE III)	VOLTAGE AT INPUT UNDER TEST	INPUT(S) UNDER TEST	OTHER INPUT TERMINALS 0.5 V	OTHER INPUT TERMINALS −0.5 V	OUTPUT TERMINAL $\overline{Q}$		(SEE NOTE 6)			
V_{IH}	High-level input voltage								0°C 25°C 75°C	150 150 150		720 720 720	mV
V_{IL}	Low-level input voltage								0°C 25°C 75°C	−1500 −1500 −1500		−150 −150 −150	mV
V_{OH}	High-level output voltage, register mode	4	X	−0.2 V	13	1, 16	4, 5, 12, 14	2	0°C 25°C 75°C	280 315			mV
					11	7, 8	4, 5, 9, 12	6					
					14	1, 16	4, 5, 12, 13	2					
					9	7, 8	4, 5, 11, 12	6					
					12	1, 16	4, 5, 13, 14	2					
					12	7, 8	4, 5, 9, 11	6					
					16	13, 14	1, 4, 5, 12	2					
					8	9, 11	4, 5, 7, 12	6					
					1	13, 14	4, 5, 12, 16	2					
					7	9, 11	4, 5, 8, 12	6					
					12	13, 14	1, 4, 5, 16	2					
					12	9, 11	4, 5, 7, 8	6					
V_{OL}	Low-level output voltage, register mode	4	X	0.2 V	13	1	4, 5, 12, 14, 16	2	0°C 25°C 75°C			−350 −315	mV
					11	7	4, 5, 8, 9, 12	6					
				−0.2 V	14	1, 13	4, 5, 12, 16	2					
					9	7, 11	4, 5, 8, 12	6					
				−0.2 V	12	1, 13	4, 5, 14, 16	2					
					12	7, 11	4, 5, 8, 9	6					
				0.2 V	16	14	1, 4, 5, 12, 13	2					
					8	9	4, 5, 7, 11, 12	6					
				−0.2 V	1	14, 16	4, 5, 12, 13	2					
					7	8, 9	4, 5, 11, 12	6					
				−0.2 V	12	14, 16	1, 4, 5, 13	2					
					12	8, 9	4, 5, 7, 11	6					
V_{OH}	High-level output voltage, storage mode	4	R	0.2 V	14	1, 13	4, 5, 12, 16	2	0°C 25°C 75°C	280 315	365 400 470	500 580	mV
					9	7, 11	4, 5, 8, 12	6					
					1	14, 16	4, 5, 12, 13	2					
					7	8, 9	4, 5, 11, 12	6					
					12		1, 4, 5, 13, 14, 16	2					
					12		4, 5, 7, 8, 9, 11	6					
V_{OL}	Low-level output voltage, storage mode	4	S	0.2 V	14	1	4, 5, 12, 13, 16	2	0°C 25°C 75°C	−505 −490	−440 −425 −390	−350 −315	mV
					9	7	4, 5, 8, 11, 12	6					
					1	14	4, 5, 12, 13, 16	2					
					7	9	4, 5, 8, 11, 12	6					
					12		1, 4, 5, 13, 14, 16	2					
					12		4, 5, 7, 8, 9, 11	6					
V_{OL}	Low-level output voltage, set mode	4	R	0.2 V	5	12	4	2	0°C 25°C 75°C			−350 −315	mV
					5	12	4	6					
V_{OH}	High-level output voltage, reset mode	4	S	0.2 V	4	12	5	2	0°C 25°C 75°C	280 315			mV
					4	12	5	6					

(Continued on page 13)

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ECL2542 electrical characteristics at specified free-air temperature (continued)

PARAMETER		TEST CONDITIONS*								MIN	TYP	MAX (SEE NOTE 6)	UNIT
		TEST FIGURE	INITIAL CONDITIONS (SEE TABLE III)	VOLTAGE AT INPUT UNDER TEST	INPUT(S) UNDER TEST	OTHER INPUT TERMINALS 0.5 V	OTHER INPUT TERMINALS −0.5 V	OUTPUT TERMINAL $\overline{Q}$	T_A				
I_{IH}	High level input current	5	X	0.5 V	8		1, 4, 5, 7, 9 11, 12, 13, 14, 16		0°C 25°C 75°C			255 235 200	μA
					11		1, 4, 5, 7, 8 9, 12, 13, 14, 16						
					12		1, 4, 5, 7, 8 9, 11, 13, 14, 16						
					13		1, 4, 5, 7, 8 9, 11, 12, 14, 16						
					16		1, 4, 5, 7, 8 9, 11, 12, 13, 14						
					1		4, 5, 7, 8, 9 11, 12, 13, 14, 16		0°C 25°C 75°C			510 470 400	μA
					4		1, 5, 7, 8, 9 11, 12, 13, 14, 16						
					5		1, 4, 7, 8, 9 11, 12, 13, 14, 16						
					7		1, 4, 5, 8, 9 11, 12, 13, 14, 16						
					9		1, 4, 5, 7, 8 11, 12, 13, 14, 16						
					14		1, 4, 5, 7, 8 9, 11, 12, 13, 16						
I_{IL}	Low-level input current	6	X	All inputs in parallel at −3.2 V					0°C 25°C 75°C			−0.9 −1.2 −1.7	μA
I_{CC} or $-I_{EE}$	Supply current	7	X	All inputs in parallel at −0.5 V					25°C	81		165	mA
C_{in}	Input capacitance (see Note 7)		X		Each				25°C		5		pF
Z_{out}	Output impedance (see Note 8)		X					2, 6	25°C		5		Ω

NOTES: 6. The algebraic convention where the most-positive limit is designated as maximum is used in this data sheet for logic voltage levels only, e.g., if −350 mV is a maximum, the typical and minimum limits are more-negative voltages.

7. C_{in} is measured using peak-current techniques. A square-wave input pulse is applied, and the input current waveform is integrated with respect to time to determine Q. C_{in} = Q/V. When a terminal is an input to more than one gate, multiply the value given by the number of gates to which this terminal is an input.

8. Constant-current loads are used to determine the output impedance which is derived from the slope of a V_O vs I_O curve.

TABLE III—INITIAL CONDITIONS

Several of the parameters require the application of conditions which cause the outputs to assume definite states prior to applying test conditions specified above.

SYMBOL	DESCRIPTION	INPUT TERMINALS* 0.5 V	INPUT TERMINALS* −0.5 V
X	Irrelevant		
S	Set $1\overline{Q}$ and $2\overline{Q}$ low	5, 12	4
R	Reset $1\overline{Q}$ and $2\overline{Q}$ high	4, 12	5

*V_{BB} (pin 15) = GND, V_{CC} (pin 3) = −1.3 V, V_{EE} (pin 10) = −3.2 V. Input and output terminals are open except as specified in these tables and in the d-c test figures.

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operating characteristics at specified free-air temperature

MODE	C_L	t_{PHL} and/or t_{PLH} PROPAGATION TIMES—ns									t_{THL} and/or t_{TLH} TRANSITION TIMES—ns								
		T_A = 0°C			T_A = 25°C			T_A = 75°C			T_A = 0°C			T_A = 25°C			T_A = 75°C		
	pF	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
ECL2540 (see Figure 2 and Table IV)																			
Register	4		2.5		1.6	2.4	3.5		2.5			3.8		2	3.7	5.2		3.9	
	50		3.6		2.4	3.6	4.5		3.6			4.7		2.5	4.6	6.7		4.4	
ECL2541 (see Figure 3 and Table V)																			
Register (Clock Controlled)	4		6.3		4.2	6.2	7.7		6.5			4.6		2	4.7	6.9		4.7	
	50		7.7		5.5	7.8	10.8		8.0			5.9		2.7	5.8	8.6		5.5	
Register (Gate Controlled)	4		4.3		2.3	4.2	5.8		4.3			4.6		2.3	4.6	6.5		4.6	
	50		5.6		3.4	5.7	8.5		5.7			5.6		2.7	5.4	7.8		5.1	
Set	4		2.7		1.9	2.7	3.5		2.8			4.5		2.9	4.5	6		4.6	
	50		3.8		2.7	3.8	4.7		3.8			4.7		2.7	4.6	7		4.5	
Reset	4		3.8		2.3	3.8	5.8		4.1			4.4		2.3	4.3	6.5		4.6	
	50		6.0		3.4	5.9	8.5		6.0			7.1		4.6	7.0	8.6		6.4	
ECL2542 (see Figure 3 and Table VI)																			
Register (Clock Controlled)	4		7.0		5.5	7.0	8.1		7.1			4.6		3	4.5	5.7		4.5	
	50		8.2		6.7	8.1	9.4		8.3			4.8		3	4.8	6.9		4.7	
Register (Gate Controlled)	4		4.5		3.3	4.4	5.7		4.4			4.2		3	4.1	5.7		4.1	
	50		5.7		4.5	5.6	6.8		5.5			4.7		3	4.7	6.9		4.6	
Set	4		2.9		1.7	2.7	3.1		2.6			4.6		3	4.5	5.7		4.6	
	50		4.0		3.2	4.0	4.7		3.9			5.4		4	5.6	6.9		5.5	
Reset	4		4.4		3.3	4.3	5.8		4.6			4.2		3	4.2	5.7		4.4	
	50		5.4		4.5	5.4	6.8		5.4			3.9		3	4.0	5		4.0	

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PARAMETER MEASUREMENT INFORMATION

TABLE IV—ECL2540

INPUT TERMINALS		OUTPUT UNDER TEST		PARAMETER MEASURED
DATA GENERATOR	−0.5 V			
14	12	2	Q	t_{PLH}, t_{TLH}, t_{PHL}, and t_{THL}
14	12	1	$\overline{Q}$	
12	14	7	Q	
12	14	8	$\overline{Q}$	

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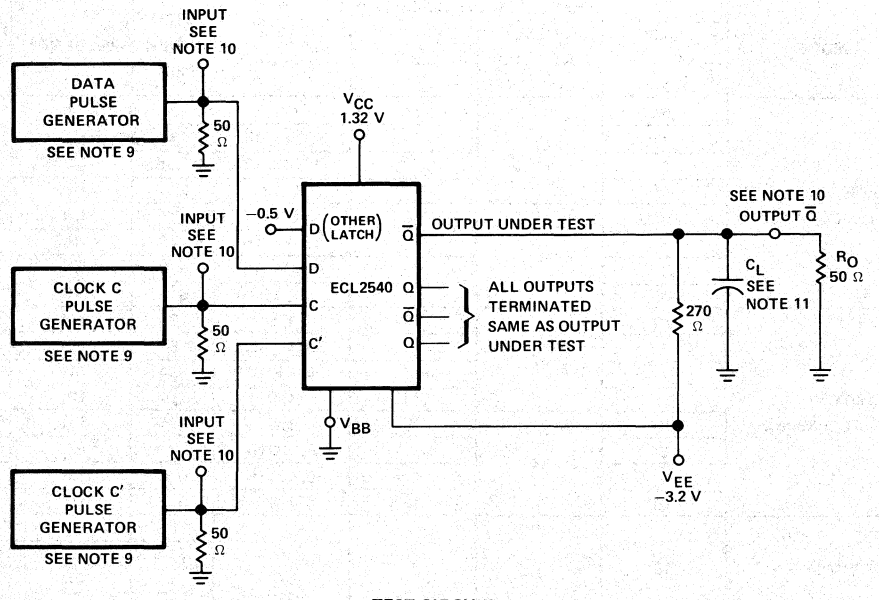
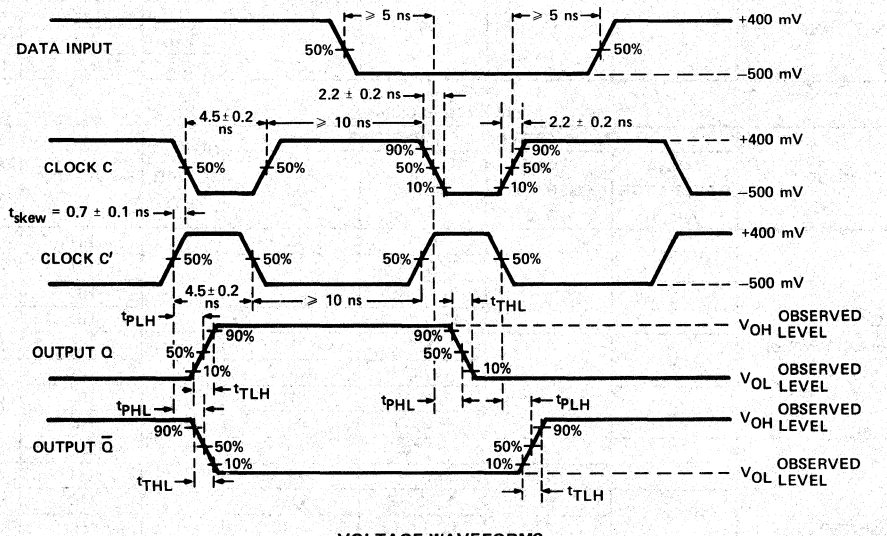
PARAMETER MEASUREMENT INFORMATION
ECL2540



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 2–ECL2540 PROPAGATION DELAY AND TRANSITION TIMES (WITH SKEW)

NOTES:
9. Each generator has a 50-Ω output impedance.
10. The waveforms are monitored on an oscilloscope with a rise time of less than or equal to 350 ps. Either a high-impedance probe with an input impedance of 100 kΩ paralleled by 2 pF, or a 50-Ω impedance system can be used. The 50-Ω resistor designated R_O is the oscilloscope input resistance in the 50-Ω system or a discrete resistor with a high-impedance probe.
11. C_L includes probe and fixture capacitance. A capacitance of 50 pF can be used to approximate an a-c fan-out of 10.

PARAMETER MEASUREMENT INFORMATION

TABLE V–ECL2541

MODE	INPUT TERMINAL CONDITIONS				OUTPUT UNDER TEST	WAVEFORM	PARAMETER MEASURED
	PULSE GENERATOR NO. 1	PULSE GENERATOR NO. 2	0.5 V	−0.5 V			
REGISTER (Clock Controlled)	16	9	11	1, 12	8	LH	t_{PLH}, t_{TLH}
	1			11, 12, 16	8	HL	t_{PHL}, t_{THL}
	1			11, 12, 16	2, 4	LH	t_{PLH}, t_{TLH}
	16		11	1, 12	2, 4	HL	t_{PHL}, t_{THL}
	16	9	13	1, 14	7	LH	t_{PLH}, t_{TLH}
	1			13, 14, 16	7	HL	t_{PHL}, t_{THL}
	1			13, 14, 16	5, 6	LH	t_{PLH}, t_{TLH}
	16		13	1, 14	5, 6	HL	t_{PHL}, t_{THL}
REGISTER (Gate Controlled)	16	12	11	1, 9	8	LH	t_{PLH}, t_{TLH}
	1			9, 11, 16	8	HL	t_{PHL}, t_{THL}
	1			9, 11, 16	2, 4	LH	t_{PLH}, t_{TLH}
	16		11	1, 9	2, 4	HL	t_{PHL}, t_{THL}
	16	14	13	1, 9	7	LH	t_{PLH}, t_{TLH}
	1			9, 13, 16	7	HL	t_{PHL}, t_{THL}
	1			9, 13, 16	5, 6	LH	t_{PLH}, t_{TLH}
	16		13	1, 9	5, 6	HL	t_{PHL}, t_{THL}
SET TIME	16	1	9	All other input terminals open	8	LH	t_{PLH}, t_{TLH}
					2, 4	HL	t_{PHL}, t_{THL}
					7	LH	t_{PLH}, t_{TLH}
					5, 6	HL	t_{PHL}, t_{THL}
RESET TIME	1	16	9		2, 4	LH	t_{PLH}, t_{TLH}
					8	HL	t_{PHL}, t_{THL}
					5, 6	LH	t_{PLH}, t_{TLH}
					7	HL	t_{PHL}, t_{THL}

TABLE VI–ECL2542

MODE	INPUT TERMINAL CONDITIONS				OUTPUT UNDER TEST	WAVEFORM	PARAMETER MEASURED
	PULSE GENERATOR NO. 1	PULSE GENERATOR NO. 2	0.5 V	−0.5 V			
REGISTER (Clock Controlled)	5	12	1, 16	4, 13, 14	2	LH	t_{PLH}, t_{TLH}
			13, 14	1, 4, 16		LH	t_{PLH}, t_{TLH}
	4		1, 13, 16	5, 14		HL	t_{PHL}, t_{THL}
			13, 14, 16	1, 5		HL	t_{PHL}, t_{THL}
	5	12	7, 8	4, 9, 11	6	LH	t_{PLH}, t_{TLH}
			9, 11	4, 7, 8		LH	t_{PLH}, t_{TLH}
	4		7, 8, 11	5, 9		HL	t_{PHL}, t_{THL}
			8, 9, 11	5, 7		HL	t_{PHL}, t_{THL}
REGISTER (Gate Controlled)	5	14	1, 16	4, 12, 13	2	LH	t_{PLH}, t_{TLH}
		1	13, 14	4, 12, 16		LH	t_{PLH}, t_{TLH}
	4	14	1, 13, 16	5, 12		HL	t_{PHL}, t_{THL}
		1	13, 14, 16	5, 12		HL	t_{PHL}, t_{THL}
	5	9	7, 8	4, 11, 12	6	LH	t_{PLH}, t_{TLH}
		7	9, 11	4, 8, 12		LH	t_{PLH}, t_{TLH}
	4	9	7, 8, 11	5, 12		HL	t_{PHL}, t_{THL}
		7	8, 9, 11	5, 12		HL	t_{PHL}, t_{THL}
SET TIME	4	5	12	All other input terminals open	2, 6	HL	t_{PHL}, t_{THL}
RESET TIME	5	4	12		2, 6	LH	t_{PLH}, t_{TLH}

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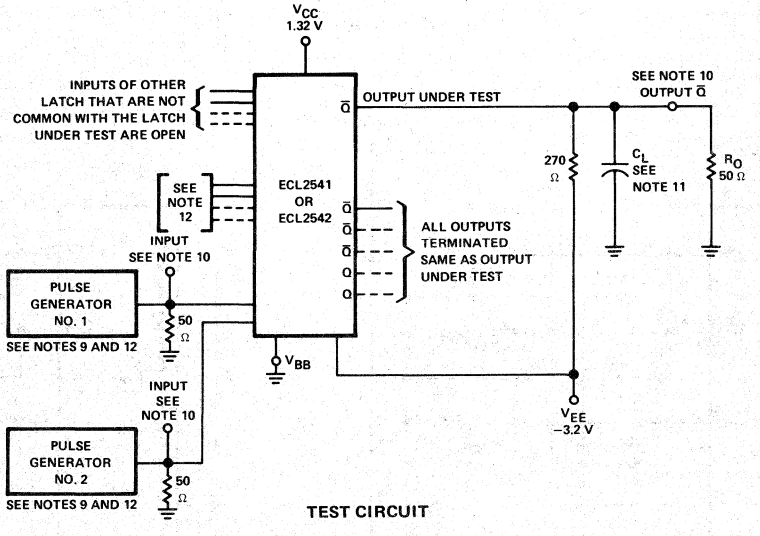
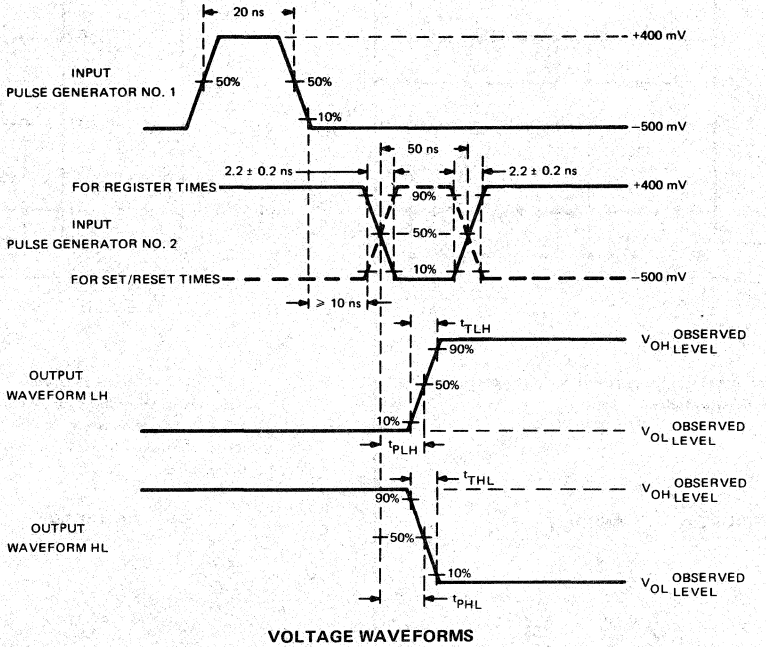
PARAMETER MEASUREMENT INFORMATION
ECL2541 AND ECL2542



TEST CIRCUIT

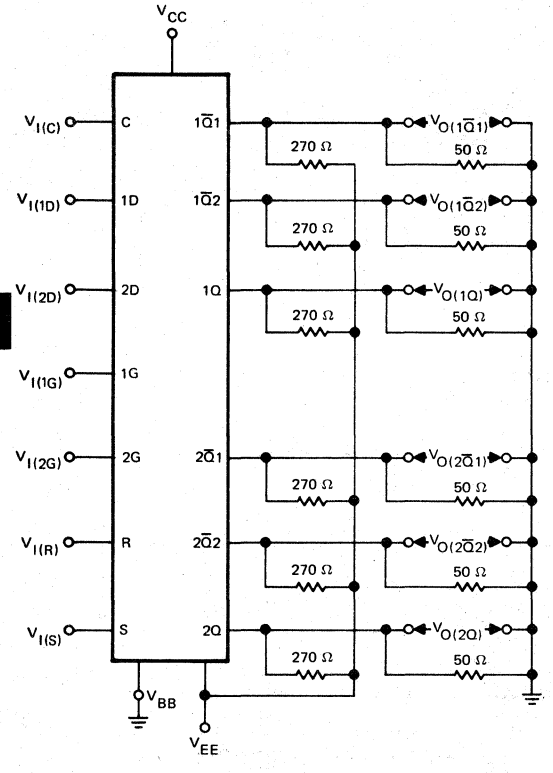


VOLTAGE WAVEFORMS

FIGURE 3–ECL2541 AND ECL2542 PROPAGATION DELAY AND TRANSITION TIMES

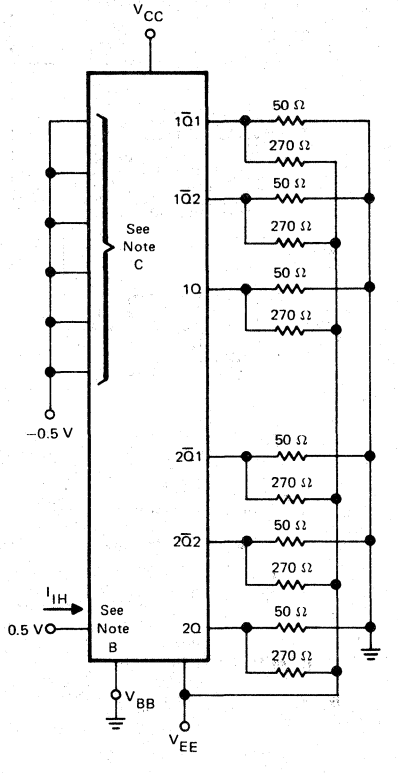
NOTES:
9. Each generator has a 50-Ω output impedance.
10. The waveforms are monitored on an oscilloscope with a rise time of less than or equal to 350 ps. Either a high-impedance probe with an input impedance of 100 kΩ paralleled by 2 pF, or a 50-Ω impedance system can be used. The 50-Ω resistor designated R_O is the oscilloscope input resistance in the 50-Ω system or a discrete resistor with a high-impedance probe.
11. C_L includes probe and fixture capacitance. A capacitance of 50 pF can be used to approximate an a-c fan-out of 10.
12. See Table V (ECL2541) or Table VI (ECL2542) for voltages to be applied to input terminals for each test.

PARAMETER MEASUREMENT INFORMATION†
ECL2541
(See Note 13)



V_I is applied to each input as specified in the electrical characteristics table.

FIGURE 4–V_{OH} AND V_{OL}



A. Each input is tested separately.
B. Any one of the following seven inputs: C, 1D, 1G, 2D, 2G, R, and S.
C. Other six inputs listed in note B that are not under test.

FIGURE 5–I_{IH}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.
NOTE 13: ECL2540 and ECL2542 are tested in a manner similar to that shown for ECL2541.

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PARAMETER MEASUREMENT INFORMATION†
ECL2541
(See Note 13)

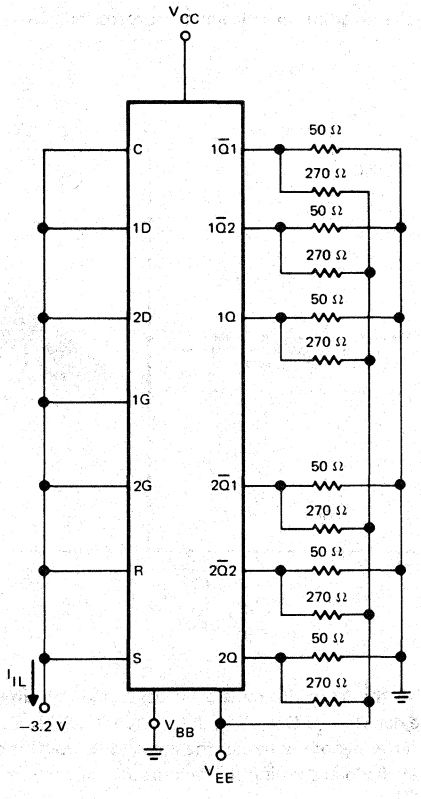


FIGURE 6–I_{IL}

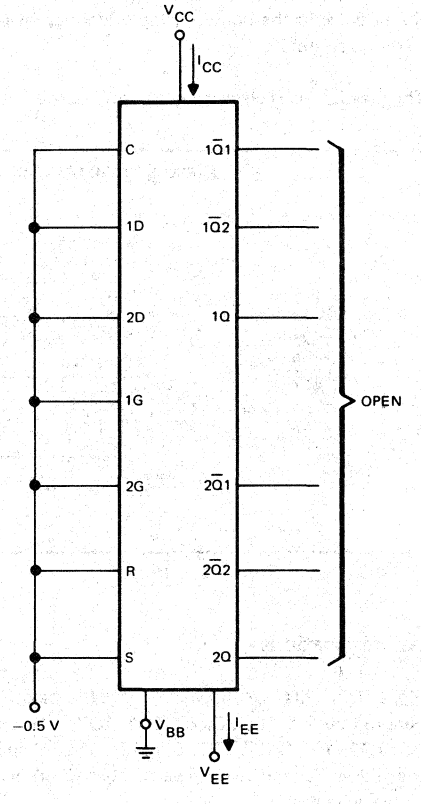


FIGURE 7–I_{CC} OR I_{EE}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

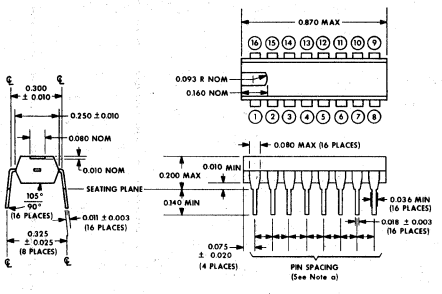
NOTE 13: ECL2540 and ECL2542 are tested in a manner similar to that shown for ECL2541.

mechanical data

The circuit bars are mounted on a 16-lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperatures with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. This package is intended for insertion in mounting-hole rows on 0.300-inch centers. Once the leads are compressed to 0.300-inch separation and inserted, sufficient tension is provided to secure the package in the board during soldering. Silver-plated leads require no additional cleaning or processing when used in soldered assembly.

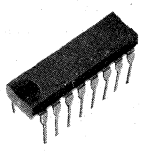
The plastic case is electrically nonconductive.

16-PIN PLASTIC DUAL-IN-LINE PACKAGE OUTLINE



NOTES: a. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within 0.010 of its true longitudinal position relative to pins 1 and 16.

b. All dimensions are in inches unless otherwise noted.



terminal designations

Pin assignments are shown in the table below and correspond to the logic diagrams on pages 2 and 3. Outputs are denoted by 1Q, $1\overline{Q}$, 2Q, $2\overline{Q}$, 1Q1, $1\overline{Q}2$, $1\overline{Q}1$, $1\overline{Q}2$, $2\overline{Q}1$, and $2\overline{Q}2$. Inputs are denoted by C, C′, 1D, 2D, 1D1, 1D2, 2D1, 2D2, 1G, 2G, 1G1, 1G2, 2G1, 2G2, S and R. The number preceding the letter denotes whether the input (or output) is part of the first or second latch. The number (if any) following the letter distinguishes inputs (or outputs) of the same latch from each other.

Power is supplied via the V_{CC}, V_{EE}, and V_{BB} terminals.

V_{BB} is a reference voltage.

NC indicates no internal connection.

PIN ASSIGNMENTS

PIN	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
ECL2540	$1\overline{Q}$	1Q	V_{CC}	NC	NC	V_{CC}	2Q	$2\overline{Q}$	NC	V_{EE}	C′	2D	C	1D	V_{BB}	NC
ECL2541	S	$1\overline{Q}1$	V_{CC}	$1\overline{Q}2$	$2\overline{Q}1$	$2\overline{Q}2$	2Q	1Q	C	V_{EE}	1D	1G	2D	2G	V_{BB}	R
ECL2542	1G1	$1\overline{Q}$	V_{CC}	R	S	$2\overline{Q}$	2G1	2D1	2G2	V_{EE}	2D2	C	1D2	1G2	V_{BB}	1D1

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Series 54S/74S Circuits

Schottky TTL
Previewing Three Series 54S/74S MSI Functions*

SN54S/74S181 Arithmetic/Logic Units

- Fastest and most versatile IC adder
- 20 ns typical add time for 16 bit words
- Performs all arithmetic/logic functions of a CPU
- Cascadable to N-bits
- Pin-for-pin functional equivalent of SN54/74181 ALU

SN54S/74S194 Universal Bidirectional Shift-Registers

- Industry's first fully universal 100-MHz TTL shift registers
  - Parallel broadside load
  - Shift right
  - Shift left
  - Inhibit clock (do nothing)
- Cascadable to N-bits
- Designed specifically for performing all shift functions required of high-speed accumulators employing SN74S181 ALU's

SN54S/74S157 Quad 2-Input Multiplexers

- Typical propagation delays of 2.25 ns per level at 13 mW per gate
- May be used with SN74S181 and SN74S194 to implement high-speed CPU accumulator
- Selects bused data from one of two sources
- Generates four functions of two variables (one variable is common)

* Available Mid-1971

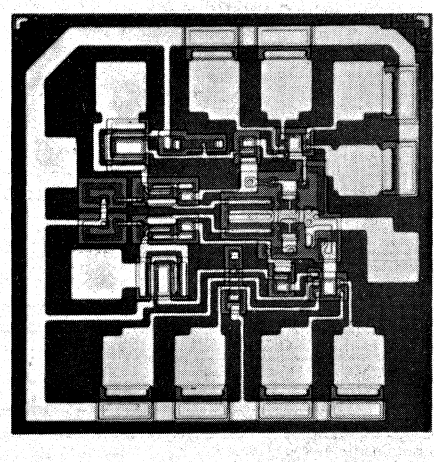
For the Full Line of Series 54S/74S Schottky SSI, See Page 5

SERIES 54S/74S
SCHOTTKY-CLAMPED† TRANSISTOR-TRANSISTOR LOGIC

FOR HIGH-SPEED, HIGH-PERFORMANCE DIGITAL SYSTEMS

description

Series 54S/74S Schottky TTL circuits are implemented with full Schottky-barrier-diode clamping to achieve ultra-high speeds previously obtainable only with emitter-coupled logic, yet they retain the desirable features of, and are completely compatible with, most of the popular saturated logic circuits. Schottky TTL circuits currently offer the best speed-power product of any high-speed logic family.



Schottky-barrier-diode clamping prevents transistors from achieving classic saturation and thereby effectively eliminates excess charge storage and subsequent recovery times. These recovery times contribute significantly to overall propagation delays experienced with saturated digital-logic circuits.

Series 54S/74S circuits are completely compatible with the Series 54/74, Series 54H/74H, and Series 54L/74L TTL logic families. Ease of use and compatibility with other TTL families result in flexibility of choice within the four speed-power ranges offered (Series 54/74, 54H/74H, 54L/74L, 54S/74S) to achieve highly efficient system grading to specific performance requirements.

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Definitive specifications are provided for operating characteristics over the full military temperature range of −55°C to 125°C for Series 54S circuits and over the temperature range of 0°C to 70°C for Series 74S circuits.

features

VERY-HIGH-SPEED, LOW-POWER OPERATION

- **3-ns typical gate propagation delay time**
- **19-mW-per-gate power dissipation at 50% duty cycle — speed-power product = 57 pJ**
- **125-MHz typical J-K flip-flop maximum input clock frequency (d-c coupled)**

EASE OF SYSTEM DESIGN

- **fully compatible with Series 54/74, 54H/74H, and 54L/74L TTL (including MSI/LSI), and most DTL**
- **Schottky-diode-clamped inputs simplify system design**
- **terminated, controlled-impedance lines not normally required**
- **low output impedance: provides low a-c noise susceptability**
  drives highly capacitive loads

IMPROVED CIRCUIT PERFORMANCE

- **switching times virtually insensitive to power supply and/or temperature variations**
- **power dissipation remains relatively low at operating frequencies up to 100 MHz**
- **high fan-out: 20 54S/74S loads at the high logic level**
  10 54S/74S loads at the low logic level
- **high d-c noise margin—typically 1 volt**

CONTENTS

†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U. S. Patent Number 3,463,975.

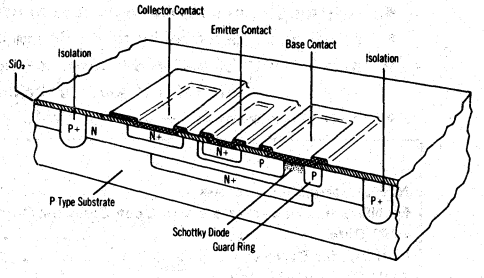
SERIES 54S/74S
FEATURING 3-ns SPEED AND 20-mW-PER-GATE PERFORMANCE
SMALL SCALE INTEGRATION (SSI)

FUNCTION	OPERATING TEMPERATURE RANGE		PACKAGES*			
	−55°C to 125°C	0°C to 70°C	Dual-In-Line		Flat	PAGE
NAND/NOR GATES						
Quadruple 2-Input Positive-NAND Gates	SN54S00	SN74S00	J	N	W	5-4
Quadruple 2-Input Positive-NAND Gates (with Open-Collector Output)	SN54S03	SN74S03	J	N	W	5-8
Hex Inverters	SN54S04	SN74S04	J	N	W	5-4
Hex Inverters (with Open-Collector Output)	SN54S05	SN74S05	J	N	W	5-8
Triple 3-Input Positive-NAND Gates	SN54S10	SN74S10	J	N	W	5-4
Triple 3-Input Positive-AND Gates	SN54S11	SN74S11	J	N	W	5-10
Triple 3-Input Position-AND Gates (with Open-Collector Output)	SN54S15	SN74S15	J	N	W	5-10
Dual 4-Input Positive-NAND Gates	SN54S20	SN74S20	J	N	W	5-4
Dual 4-Input Positive-NAND Gates (with Open-Collector Output)	SN54S22	SN74S22	J	N	W	5-8
Dual 4-Input Positive-NAND Buffers	SN54S40	SN74S40	J	N	W	5-12
Dual 4-Input Positive-NAND Line Drivers	SN54S140	SN74S140	J	N	W	5-12
AND-OR-INVERT GATES						
4-2-3-2-Input AND-OR-INVERT Gates	SN54S64	SN74S64	J	N	W	5-13
4-2-3-2-Input AND-OR-INVERT Gates (with Open-Collector Output)	SN54S65	SN74S65	J	N	W	5-13
FLIP-FLOPS						
Dual D-Type Edge-Triggered Flip-Flops	SN54S74	SN74S74	J	N	W	5-15
Dual J-K Negative Edge-Triggered Flip-Flops (80 MHz) with Preset and Clear	SN54S112	SN74S112	J	N	W	5-17
Dual J-K Negative Edge-Triggered Flip-Flops (80 MHz) with Preset	SN54S113	SN74S113	J	N	W	5-21
Dual J-K Negative Edge-Triggered Flip-Flops (80 MHz) Common Clock and Common Clear	SN54S114	SN74S114	J	N	W	5-21

*For outline drawings of all packages, see Section 1.

The Schottky TTL Technology

The Schottky-clamped transistor is produced utilizing conventional diffusions. The base contact opening is extended beyond the base diffusion and over the collector region. Metallization is deposited over both the base and collector regions and simultaneously serves as the transistor base contact and the SBD anode contact. The collector n-type material and the metallization then form the metal-silicon SBD structure (refer to cross-section at right).



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The Schottky TTL Technology (Continued)

The SBD is connected in parallel to the base-collector junction of the normal TTL n-p-n transistor. As the SBD has a lower forward voltage than the base-collector junction, it clamps the transistor as base drive increases, diverting most excess base current from the base-collector junction, and prevents the transistor from reaching classic saturation. Excess stored charge, which exists in usual transistor structures and which must be removed before switching occurs, does not exist in the SBD-clamped transistor.

In addition to incorporation of the SBD into popular 54/74 TTL, the Series 54S/74S Schottky TTL family employs shallower diffusion and smaller geometries which lower internal capacitances and further reduces overall propagation delays. Elimination of gold-doping simplifies processing and stabilizes switching speeds over the operating temperature range.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Output voltage (see Notes 1 and 3) . . . . . 7 V
Operating free-air temperature range: Series 54S Circuits . . . . . −55°C to 125°C
Series 74S Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor.
3. This is the maximum voltage which should be applied to any open-collector output when it is in the off state.

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recommended operating conditions

	SERIES 54S CIRCUITS			SERIES 74S CIRCUITS			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Operating free-air temperature, T_A	−55		125	0		70	°C

unused inputs of positive-AND/NAND gates

For optimum switching times and minimum noise susceptibility, unused inputs of AND or NAND gates should be maintained at a voltage greater than 2.7 V, but not to exceed the absolute maximum rating of 5.5 V. This eliminates the distributed capacitance associated with the floating input emitter, bond wire, and package lead, and ensures that no degradation will occur in the propagation delay times. Some possible ways of handling input emitters are:

a. Connect unused inputs to an independent supply voltage. Preferably, this voltage should be between 2.7 V and 3.5 V.
b. Connect unused inputs to a used input if maximum fan-out of the driving output will not be exceeded. Each additional input presents a full load to the driving output at a high-level voltage but adds no loading at a low-level voltage.
c. Connect unused inputs to V_{CC} through a 1-kΩ resistor so that if a transient which exceeds the 5.5-V maximum rating should occur, the impedance will be high enough to protect the input. One to 25 unused inputs may be connected to each 1-kΩ resistor.

input-current requirements

Input-current requirements reflect worst-case V_{CC} and temperature conditions. Each input of the multiple-emitter input transistors requires a maximum of 2 mA out of the input at a low logic level which is defined as 1 normalized load. Each input requires current into the input at a high logic level. This current is 50 μA maximum for each emitter. Currents into the input terminals are specified as positive values.

fan-out capability

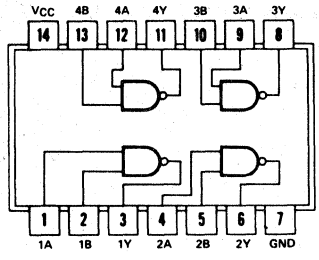
Fan-out (N) reflects the ability of an output to supply current to a number of normalized loads at a high logic level and to sink current at the low logic level. At the high logic level, each standard output is capable of supplying current to drive 20 Series 54H, 74H, 54S, or 74S loads (N_H = 20). Currents out of the output are specified as negative values. At the low logic level, each standard output is capable of sinking current from 10 Series 54H, 74H, 54S, or 74S loads (N_L = 10).

CIRCUIT TYPES SN54S00, SN54S04, SN54S10, SN54S20, SN74S00, SN74S04, SN74S10, SN74S20
POSITIVE-NAND GATES/HEX INVERTERS

Typical Propagation Time . . . 3 ns at C_L = 15 pF
Typical Power Dissipation . . . 19 mW per Gate at 50% Duty Cycle

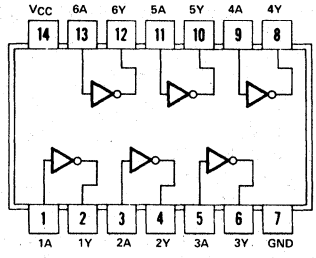
J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)

SN54S00, SN74S00
QUADRUPLE 2-INPUT NAND GATES



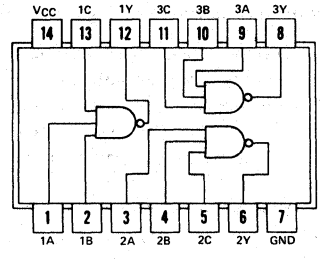
positive logic: $Y = \overline{AB}$

SN54S04, SN74S04
HEX INVERTERS



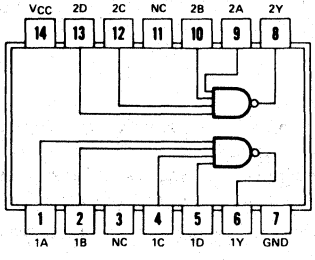
positive logic: $Y = \overline{A}$

SN54S10, SN74S10
TRIPLE 3-INPUT NAND GATES



positive logic: $Y = \overline{ABC}$

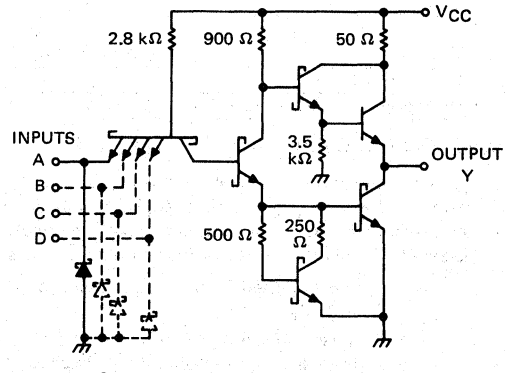
SN54S20, SN74S20
DUAL 4-INPUT NAND GATES



positive logic: $Y = \overline{ABCD}$

NC - No internal connection

schematic (each gate)



Component values shown are nominal.

recommended operating conditions

		SN54S00, SN54S04, SN54S10, SN54S20			SN74S00, SN74S04, SN74S10, SN74S20			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Operating free-air temperature, T_A		−55		125	0		70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, I_{OH} = −1 mA	V_{IL} = 0.8 V,	Series 54S	2.5	3.4		V
				Series 74S	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 20 mA	V_{IH} = 2 V,				0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V				1	mA
I_{IH}	High-level input current (each input)	V_{CC} = MAX,	V_I = 2.7 V				50	μA
I_{IL}	Low-level input current (each input)	V_{CC} = MAX,	V_I = 0.5 V				−2	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX			−40		−100	mA
I_{CCH}	Supply current, high-level output (average per gate)	V_{CC} = MAX,	All inputs at 0 V			2.5	4	mA
I_{CCL}	Supply current, low-level output (average per gate)	V_{CC} = MAX,	All inputs at 5 V			5	9	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

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switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS¶		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF,	R_L = 280 Ω	2	3	4.5	ns
		C_L = 50 pF,	R_L = 280 Ω		4.5		
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15 pF,	R_L = 280 Ω	2	3	5	ns
		C_L = 50 pF,	R_L = 280 Ω		5		

¶Switching characteristic measurements are made utilizing the same test circuits as illustrated for Darlington outputs in Figure 74 of the Series 54H/74H section. The inverting-output waveform is applicable for these three circuits. In lieu of Notes 1 through 4, the following notes are applicable:

NOTES: A. The pulse generator has the following characteristics: $V_{in(1)}$ = 3 V, $V_{in(0)}$ = 0 V, $t_1 = t_0$ = 2.5 ns, PRR = 1 MHz, duty cycle = 50%, and $Z_{out} \approx 50\ \Omega$.

B. Inputs not under test are at 2.7 V.

C. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE
vs
INPUT VOLTAGE

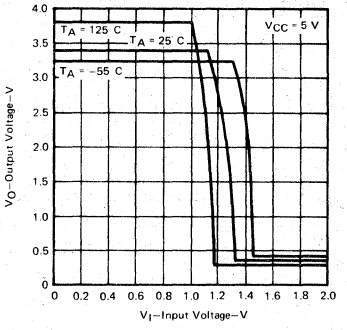

FIGURE 1

INPUT-CLAMPING-DIODE
FORWARD VOLTAGE
vs
FREE-AIR TEMPERATURE

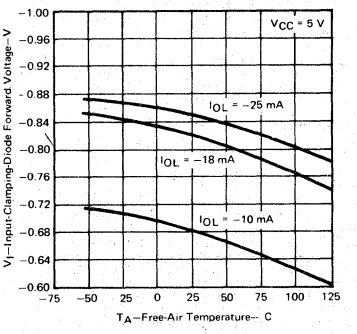

FIGURE 2

INPUT CURRENT
vs
INPUT VOLTAGE

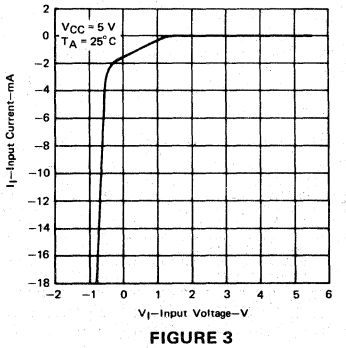

FIGURE 3

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

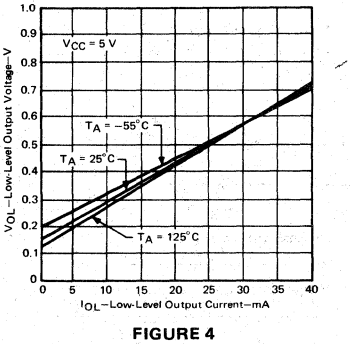

FIGURE 4

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

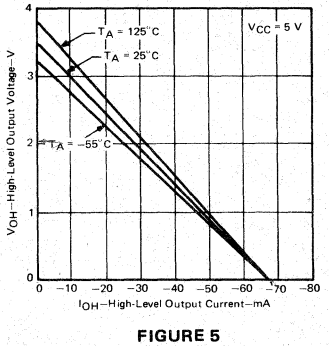

FIGURE 5

HIGH-LEVEL INPUT CURRENT
vs
FREE-AIR TEMPERATURE

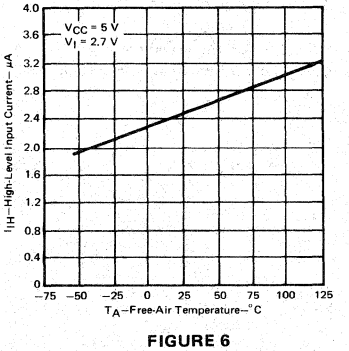

FIGURE 6

†Data for temperatures below 0°C and above 70°C is applicable to Series 54S circuits only.

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TYPICAL CHARACTERISTICS†

PROPAGATION DELAY TIME,
LOW-TO-HIGH-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

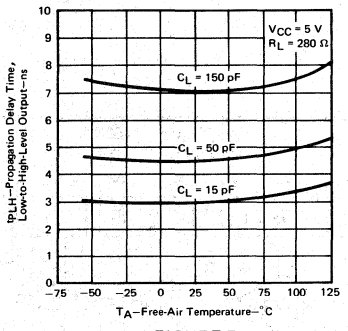


FIGURE 7

PROPAGATION DELAY TIME,
LOW-TO-HIGH-LEVEL OUTPUT
vs
SUPPLY VOLTAGE

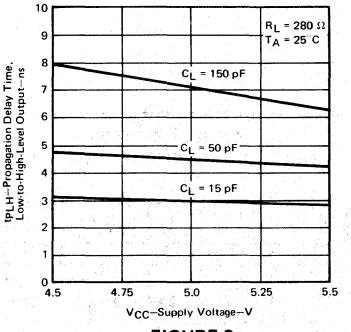


FIGURE 8

PROPAGATION DELAY TIME,
HIGH-TO-LOW-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

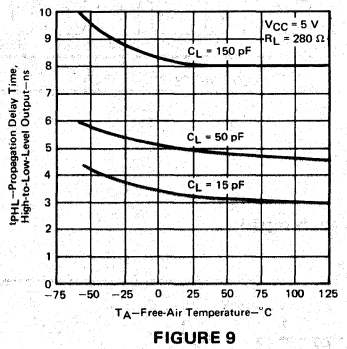


FIGURE 9

PROPAGATION DELAY TIME,
HIGH-TO-LOW-LEVEL OUTPUT
vs
SUPPLY VOLTAGE

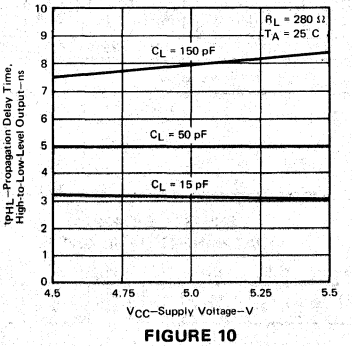


FIGURE 10

AVERAGE PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

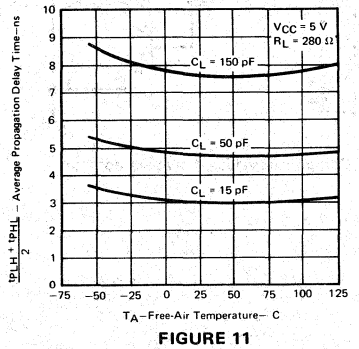


FIGURE 11

POWER DISSIPATION PER GATE
vs
FREQUENCY

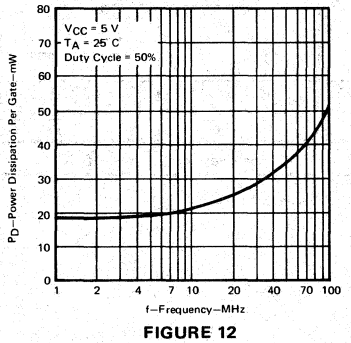


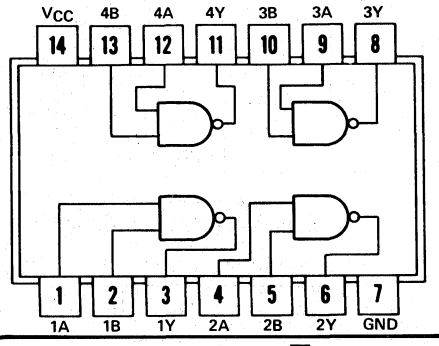
FIGURE 12

†Data for temperatures below 0°C and above 70°C is applicable to Series 54S circuits only.

Typical Propagation Time . . . 5 ns at C_L = 15 pF
Typical Power Dissipation . . . 17 mW per Gate at 50% Duty Cycle

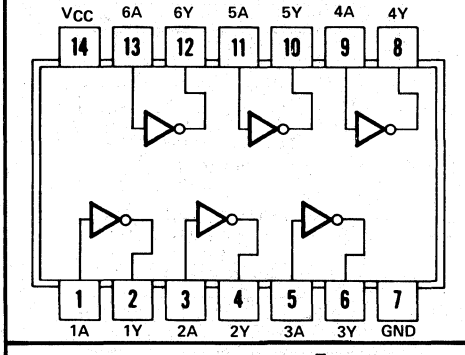
J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)

SN54S03, SN74S03
QUADRUPLE 2-INPUT NAND GATES



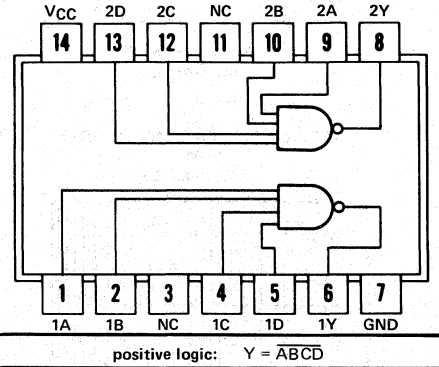
positive logic: $Y = \overline{AB}$

SN54S05, SN74S05
HEX INVERTERS



positive logic: $Y = \overline{A}$

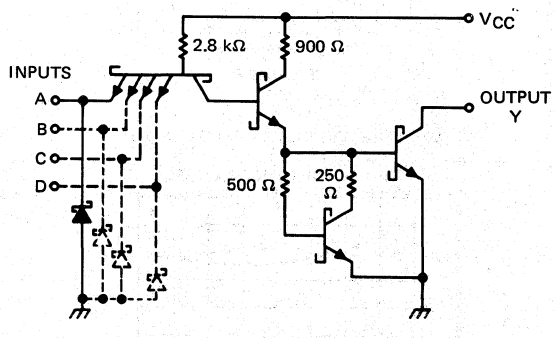
SN54S22, SN74S22
DUAL 4-INPUT NAND GATES



positive logic: $Y = \overline{ABCD}$

NC—No internal connection

schematic (each gate)



Component values shown are nominal.

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recommended operating conditions

	SN54S03, SN54S05, SN54S22			SN74S03, SN74S05, SN74S22			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from any output, N			10			10	
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.2	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{OH} = 5.5 V	V_{IL} = 0.8 V,			250	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 20 mA	V_{IH} = 2 V,			0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current (each input)	V_{CC} = MAX,	V_I = 2.7 V			50	μA
I_{IL}	Low-level input current (each input)	V_{CC} = MAX,	V_I = 0.5 V			−2	mA
I_{CCH}	Supply current, high-level output (average per gate)	V_{CC} = MAX,	All inputs at 0 V		1.5	3.3	mA
I_{CCL}	Supply current, low-level output (average per gate)	V_{CC} = MAX,	All inputs at 5 V		5	9	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

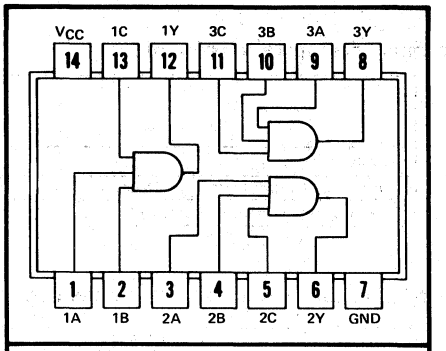
PARAMETER		TEST CONDITIONS¶		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF,	R_L = 280 Ω	2	5	7.5	ns
		C_L = 50 pF,	R_L = 280 Ω		7.5		
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15 pF,	R_L = 280 Ω	2	4.5	7	ns
		C_L = 50 pF,	R_L = 280 Ω		7		

¶ Switching characteristic measurements are made utilizing the same test circuit as illustrated for open-collector outputs in Figure 74 of the Series 54H/74H section. The inverting-output waveform is applicable for these circuits. In lieu of Notes 1 through 4, the following notes are applicable:

NOTES: A. The pulse generator has the following characteristics: $V_{in(1)}$ = 3 V, $V_{in(0)}$ = 0 V, $t_1 = t_0$ = 2.5 ns, PRR = 1 MHz, duty cycle = 50%, and $Z_{out} \approx 50\ \Omega$.
B. Inputs not under test are at 2.7 V.
C. C_L includes probe and jig capacitance.

CIRCUIT TYPES SN54S11, SN54S15, SN74S11, SN74S15
TRIPLE 3-INPUT POSITIVE-AND GATES

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)



positive logic: Y = ABC

SN54S11, SN74S11 ACTIVE PULL-UP

- Typical Propagation Time . . . 5 ns at C_L = 15 pF
- Typical Power Dissipation . . . 32 mW per Gate at 50% Duty Cycle

SN54S15, SN74S15 OPEN-COLLECTOR

- Typical Propagation Time . . . 6 ns at C_L = 15 pF
- Typical Power Dissipation . . . 29 mW per Gate at 50% Duty Cycle

5

recommended maximum fan-out from each output

	SN54S11 SN74S11	SN54S15 SN74S15
Loads at a high logic level	20	
Loads at a low logic level	10	10

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS †		SN54S11 SN74S11 MIN	SN54S11 SN74S11 TYP‡	SN54S11 SN74S11 MAX	SN54S15 SN74S15 MIN	SN54S15 SN74S15 TYP‡	SN54S15 SN74S15 MAX	UNIT
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, I_{OH} = −1 mA	SN54S11	2.5	3.4					V
			SN74S11	2.7	3.4					
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{OH} = 5.5 V							250	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 20 mA				0.5			0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current (each input)	V_{CC} = MAX, V_I = 2.7 V				50			50	μA
I_{IL}	Low-level input current (each input)	V_{CC} = MAX, V_I = 0.5 V				−2			−2	mA
I_{OS}	Short-circuit output current §	V_{CC} = MAX		−40		−100				mA
I_{CCH}	Supply current, high-level output (average per gate)	V_{CC} = MAX, All inputs at 5 V			4.5	8		3.5	6.5	mA
I_{CCL}	Supply current, low-level output (average per gate)	V_{CC} = MAX, All inputs at 0 V			8	14		8	14	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable series on the second page of this section.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

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switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER	TEST CONDITIONS¶	SN54S11 SN74S11			SN54S15 SN74S15			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH} Propagation delay time, low-to-high-level output	C_L = 15 pF, R_L = 280 Ω	2.5	4.5	7	2.5	5.5	8.5	ns
	C_L = 50 pF, R_L = 280 Ω		6			8.5		ns
t_{PHL} Propagation delay time, high-to-low-level output	C_L = 15 pF, R_L = 280 Ω	2.5	5	7.5	2.5	6	9	ns
	C_L = 50 pF, R_L = 280 Ω		7.5			8		ns

¶Switching characteristic measurements are made utilizing the same test circuits as illustrated in Figure 74 of the Series 54H/74H section. The noninverting-output waveform is applicable for these circuits. In lieu of Notes 1 through 4, the following notes are applicable:

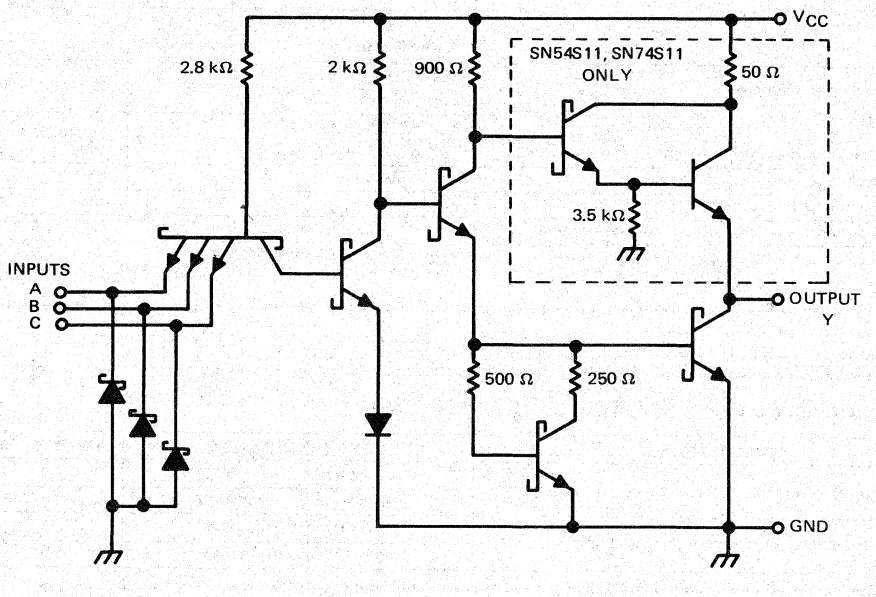
NOTES: A. The pulse generator has the following characteristics: $V_{in(1)}$ = 3 V, $V_{in(0)}$ = 0 V, $t_1 = t_0$ = 2.5 ns, PRR = 1 MHz, duty cycle = 50%, and $Z_{out} \approx 50\ \Omega$.

B. Inputs not under test are at 2.7 V.

C. C_L includes probe and jig capacitance.

5

schematic (each gate)

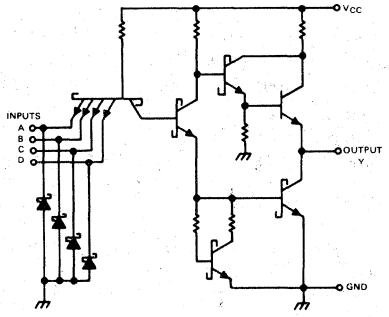


Component values shown are nominal.

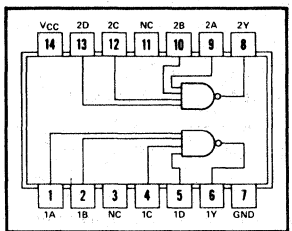
CIRCUIT TYPES SN54S40, SN54S140, SN74S40, SN74S140
DUAL 4-INPUT POSITIVE-NAND BUFFERS/LINE DRIVERS

Typical Propagation Time . . . 4 ns at C_L = 50 pF

schematic (each gate)



J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)



positive logic: $Y = \overline{ABCD}$

NC - No internal connection

recommended maximum fan-out from each output

Loads at a high logic level 60
Load at a low logic level 30

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OH} = −3 mA	Series 54S	2.5	3.4		V
			Series 74S	2.7	3.4		
		V_{CC} = MIN, V_I = 0.5 V, R_O = 50 Ω to GND	SN54S140	2			V
			SN74S140				
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 60 mA				0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current (each input)	V_{CC} = MAX, V_I = 2.7 V				100	μA
I_{IL}	Low-level input current (each input)	V_{CC} = MAX, V_I = 0.5 V				−4	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−50		−225	mA
I_{CCH}	Supply current, high-level output (average per gate)	V_{CC} = MAX, All inputs at 0 V			5	9	mA
I_{CCL}	Supply current, low-level output (average per gate)	V_{CC} = MAX, All inputs at 5 V			12.5	22	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable series on the second page of this section.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed 100 milliseconds.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 30

PARAMETER		TEST CONDITIONS ¶	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF, R_L = 93 Ω	2	4	6.5	ns
		C_L = 150 pF, R_L = 93 Ω		6		ns
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 50 pF, R_L = 93 Ω	2	4	6.5	ns
		C_L = 150 pF, R_L = 93 Ω		6		ns

¶Switching characteristic measurements are made utilizing the same test circuits as illustrated for Darlington outputs in Figure 74 of the Series 54H/74H section. The inverting waveform is applicable for these circuits. In lieu of Notes 1 through 4, the following notes are applicable:

NOTES: A. The pulse generator has the following characteristics: $V_{in(1)}$ = 3 V, $V_{in(0)}$ = 0 V, $t_1 = t_0$ = 2.5 ns, PRR = 1 MHz, duty cycle = 50%, and $Z_{out} \approx 50\ \Omega$.
B. Inputs not under test are at 2.7 V.
C. C_L includes probe and jig capacitance.

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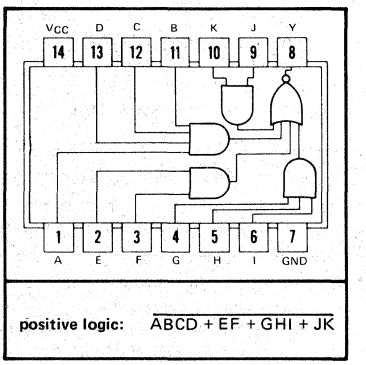
SN54S64, SN74S64 ACTIVE PULL-UP

- Typical Propagation Time . . . 3.5 ns at C_L = 15 pF
- Typical Power Dissipation . . . 39 mW at 50% Duty Cycle

SN54S65, SN74S65 OPEN-COLLECTOR

- Typical Propagation Time . . . 5 ns at C_L = 15 pF
- Typical Power Dissipation . . . 36 mW at 50% Duty Cycle

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)



positive logic: $\overline{ABCD + EF + GHI + JK}$

recommended maximum fan-out from each output

	SN54S64 SN74S64	SN54S65 SN74S65
Loads at a high logic level	20	
Loads at a low logic level	10	10

5

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54S64 SN74S64 MIN	SN54S64 SN74S64 TYP‡	SN54S64 SN74S64 MAX	SN54S65 SN74S65 MIN	SN54S65 SN74S65 TYP‡	SN54S65 SN74S65 MAX	UNIT
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 0.8 V, I_{OH} = −1 mA	SN54S64	2.5	3.4					V
			SN74S64	2.7	3.4					
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 0.8 V, V_{OH} = 5.5 V							250	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 2 V, I_{OL} = 20 mA				0.5			0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current (each input)	V_{CC} = MAX, V_I = 2.7 V				50			50	μA
I_{IL}	Low-level input current (each input)	V_{CC} = MAX, V_I = 0.5 V				−2			−2	mA
I_{OS}	Short-circuit output current §	V_{CC} = MAX		−40		−100				mA
I_{CCH}	Supply current, high-level output	V_{CC} = MAX, See Note 1			7	12.5		6	11	mA
I_{CCL}	Supply current, low-level output	V_{CC} = MAX, See Note 2			8.5	16		8.5	16	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable Series on the second page of this section.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

NOTES: 1. I_{CCH} is measured with all inputs grounded, and the outputs open.
2. I_{CCL} is measured with all inputs of one gate at 5 V, the remaining inputs grounded, and the outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER	TEST CONDITIONS¶	SN54S64 SN74S64			SN54S65 SN74S65			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH} Propagation delay time, low-to-high-level output	C_L = 15 pF, R_L = 280 Ω	2	3.5	5.5	2	5	7.5	ns
	C_L = 50 pF, R_L = 280 Ω		5			8		ns
t_{PHL} Propagation delay time, high-to-low-level output	C_L = 15 pF, R_L = 280 Ω	2	3.5	5.5	2	5.5	8.5	ns
	C_L = 50 pF, R_L = 280 Ω		5.5			6.5		ns

¶Switching characteristic measurements are made utilizing the same test circuits as illustrated in Figure 74 of the Series 54H/74H section. The inverting-output waveform is applicable for these circuits. In lieu of Notes 1 through 4, the following notes are applicable:

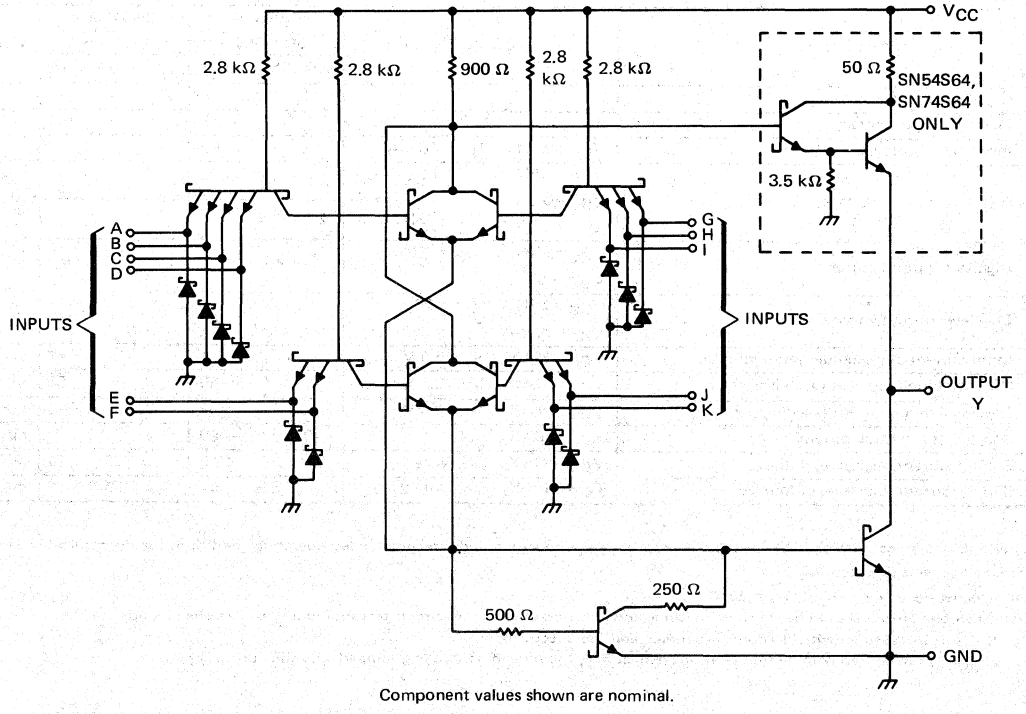
NOTES: A. The pulse generator has the following characteristics: $V_{in(1)}$ = 3 V, $V_{in(0)}$ = 0 V, $t_1 = t_0$ = 2.5 ns, PRR = 1 MHz, duty cycle = 50%, and $Z_{out} \approx 50\ \Omega$.

B. Input pulse is applied to one input of one AND section, 2.7 V is applied to all unused inputs of that AND section, and all inputs of unused AND sections are grounded.

C. C_L includes probe and jig capacitance.

5

schematic



Component values shown are nominal.

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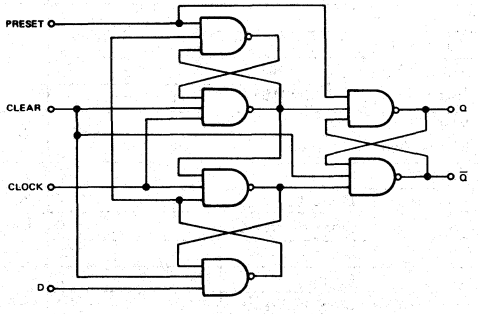
Typical Maximum Input Clock Frequency . . . 90 MHz
Typical Power Dissipation . . . 75 mW per Flip-Flop

functional block diagram (each flip-flop)



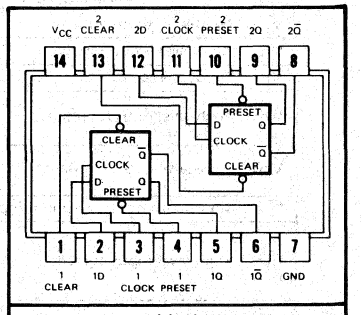
TRUTH TABLE
(Each Flip-Flop)

t_n		t_{n+1}
INPUT		OUTPUT
D	Q	Q̄
L	L	H
H	H	L

H = high level, L = low level

NOTES: A. t_n = bit time before clock pulse
B. t_{n+1} = bit time after clock pulse

J OR N DUAL-IN-LINE OR W FLAT PACKAGE (TOP VIEW)



positive logic:
Low input to preset sets Q to high level
Low input to clear resets Q to low level
Preset and clear are independent of clock

description

These monolithic dual edge-triggered flip-flops utilize Schottky TTL circuitry to produce very-high-speed D-type flip-flops. Each flip-flop has individual clear and preset inputs, and also complementary Q and Q̄ outputs.

Information at input D is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D-input signal has no effect.

These circuits are fully compatible for use with most TTL or DTL circuits. A full fan-out to 10 normalized Series 54S/74S loads is available from each of the outputs at a low logic level. At a high logic level, a fan-out of 20 is available to facilitate tying unused inputs to used inputs. Maximum clock frequency is 75 megahertz, with a typical power dissipation of 75 milliwatts per flip-flop.

The SN54S74 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74S74 is characterized for operation from 0°C to 70°C.

recommended operating conditions

		SN54S74			SN74S74			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Clock frequency, f_{clock}			70			70		MHz
Width of clock pulse, $t_{w(clock)}$			7			7		ns
Width of preset pulse, $t_{w(preset)}$			7			7		ns
Width of clear pulse, $t_{w(clear)}$			7			7		ns
Input setup time, t_{setup}	High-level data		10			10		ns
	Low-level data		12			12		ns
Input hold time, t_{hold}		0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA					−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8, I_{OH} = −1 mA		SN54S74	2.5	3.4		V
				SN74S74	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8, I_{OL} = 20 mA					0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V					1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V	D input				50	μA
			Clock or Preset				100	
			Clear				150	
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V	D input				−2	mA
			Clock or Preset				−4	
			Clear				−6	
I_{OS}	Short-circuit output current§	V_{CC} = MAX			−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 1				30		mA

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†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type. See Figures 1 through 5 of the Series 54H/74H section for test circuits.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

NOTE 1: I_{CC} is measured with outputs open, clock grounded, and J, K, preset, and clear at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS¶	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 280 Ω		90		MHz
t_{PLH}	Propagation delay time, low-to-high-level output, from clear or preset			5		ns
t_{PHL}	Propagation delay time, high-to-low-level output, from clear or preset			8		ns
t_{PLH}	Propagation delay time, low-to-high-level output, from clock			7		ns
t_{PHL}	Propagation delay time, high-to-low-level output, from clock			7		ns

¶Switching characteristic measurements are made utilizing the same test circuits as illustrated in Figures 6, 7, and 8 of the Series 54H/74H section, except that the input pulse rise and fall times (shown as ⩽ 7 ns) are ⩽ 2.5 ns. Information in the notes of these figures is applicable except as follows:

In Figures 7 and 8: $t_{w(clock)}$ = 10 ns.
In Figure 7: t_{setup} = 8 ns and t_w = 30 ns.
In Figure 8: t_{setup} = 8 ns and t_w = 30 ns.

PRELIMINARY DATA SHEET:
Supplementary data will be published at a later date.

TEXAS INSTRUMENTS
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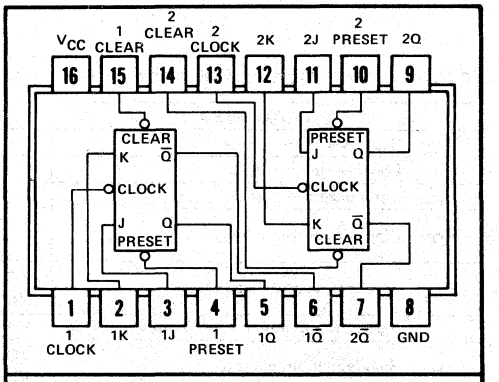
- Typical Maximum Input Clock Frequency . . . 125 MHz
- Fully D-C Coupled
- Typical Power Dissipation . . . 75 mW per Flip-Flop

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)



positive logic: Low input to preset sets Q to high level.
Low input to clear resets Q to low level.
Clear and preset are independent of clock.

TRUTH TABLE

t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\bar{Q}_n$

NOTES: A. t_n = Bit time before clock pulse.
B. t_{n+1} = Bit time after clock pulse.

5

description

These monolithic dual J-K flip-flops feature individual J, K, clock, and asynchronous preset and clear inputs to each flip-flop. When the clock goes high, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is high and the bistable will perform according to the truth table as long as minimum setup and hold times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

recommended operating conditions

		SN54S112			SN74S112			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Input clock frequency, f_{clock}		0		80	0		80	MHz
Width of clock pulse, $t_{w(clock)}$		6			6			ns
Width of preset pulse, $t_{w(preset)}$		8			8			ns
Width of clear pulse, $t_{w(clear)}$		8			8			ns
Input setup time, t_{setup} (see Note 1)		3			3			ns
Input hold time, t_{hold} (see Note 2)		0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

NOTES: 1. Setup time is the interval immediately preceding the negative-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.
2. Hold time is the interval immediately following the negative-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its continued recognition.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = −1 mA	SN54S112	2.5	3.4		V
				SN74S112	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 20 mA				0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V		J or K input			50	μA
				Clock, preset, or clear			100	
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V		J or K input			−1.6	mA
				Clock			−4	
				Preset or clear			−7	
I_{OS}	Short-circuit output current§	V_{CC} = MAX,			−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 3			30	50	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

NOTE 3: I_{CC} is measured with outputs open, clock grounded, and J, K, preset, and clear at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS¶		MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF,	R_L = 280 Ω	80	125		MHz
t_{PLH}	Propagation delay time, low-to-high-level output, from clear or preset			2	4	7	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from clear or preset			2	5	7	ns
t_{PLH}	Propagation delay time, low-to-high-level output, from clock			2	4	7	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from clock			2	5	7	ns

¶Switching characteristic measurements are made utilizing the same test circuits as illustrated for Darlington outputs in Figures 77 and 78 of the Series 54H/74H section. Information in the notes of these figures pertaining to the SN74H108 is applicable for the SN74S112, except $t_1 = t_0$ = 2.5 ns for all input pulse characteristics and the steady-state J and K input voltages are 2.7 V instead of 2.4 V.

TEXAS INSTRUMENTS
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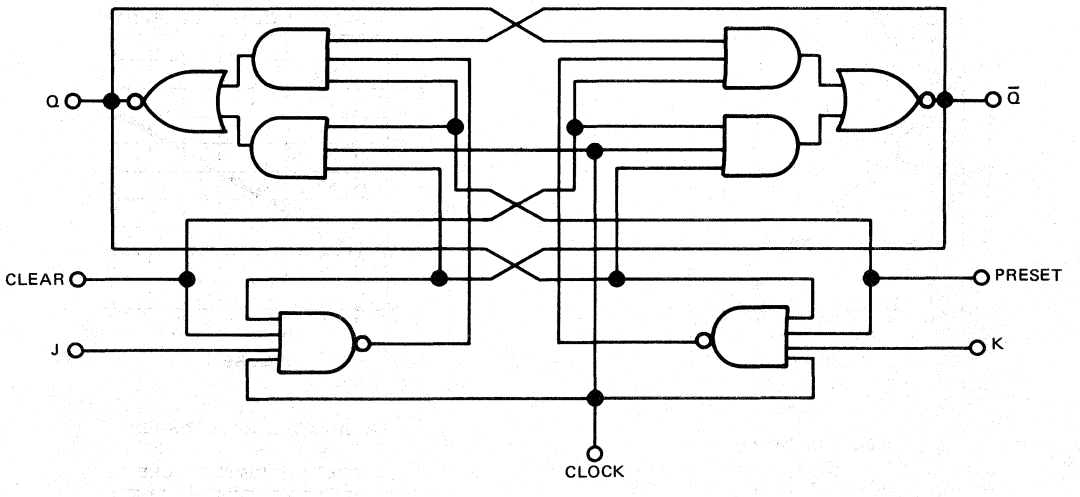
functional block diagram (each flip-flop)



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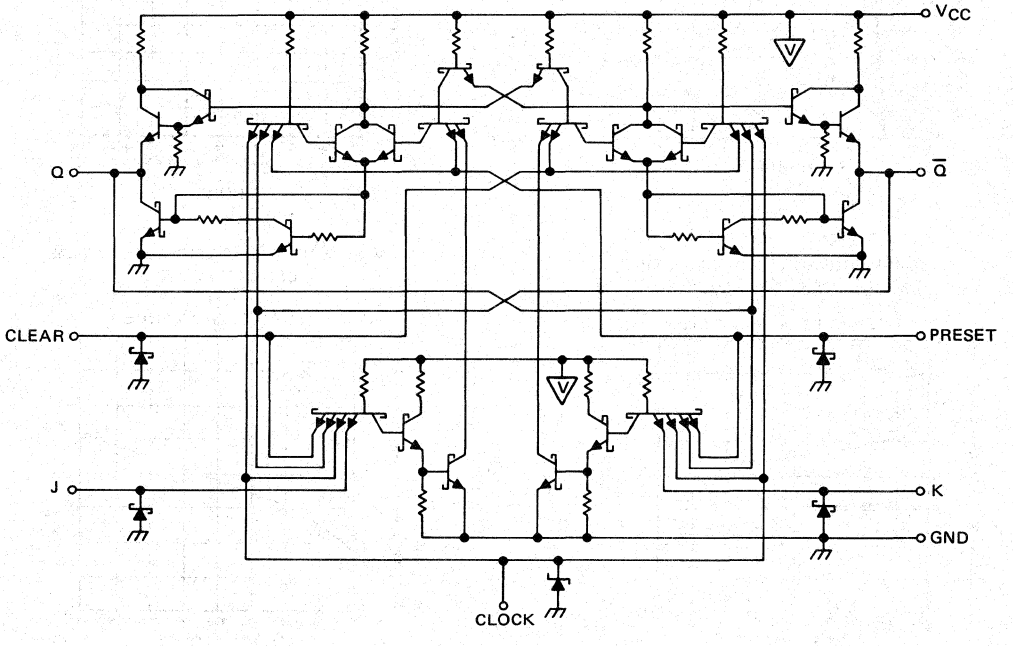
schematic (each flip-flop)



▽ . . . V_{CC} bus

TYPICAL CHARACTERISTICS†

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

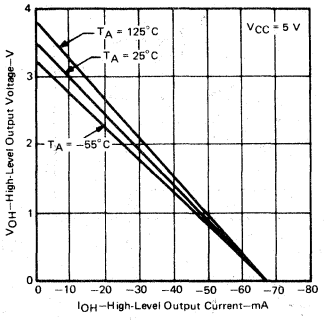


FIGURE 1

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

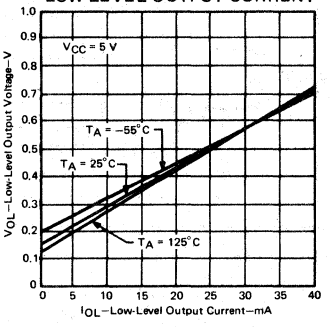


FIGURE 2

INPUT CURRENT
vs
INPUT VOLTAGE

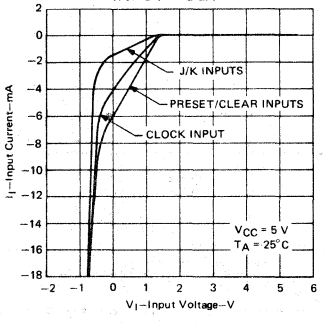


FIGURE 3

HIGH-LEVEL INPUT CURRENT
vs
FREE-AIR TEMPERATURE

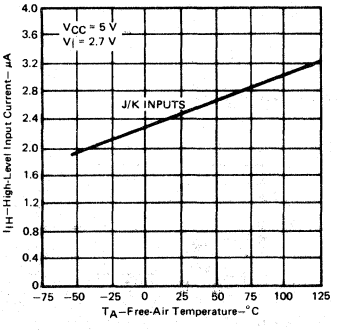


FIGURE 4

AVERAGE PROPAGATION DELAY TIME,
CLOCK TO OUTPUT
vs
FREE-AIR TEMPERATURE

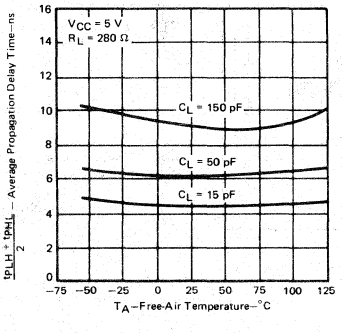


FIGURE 5

AVERAGE PROPAGATION DELAY TIME,
CLOCK TO OUTPUT
vs
LOAD CAPACITANCE

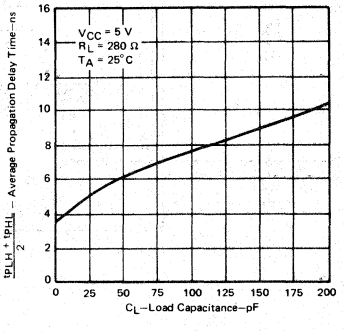


FIGURE 6

†Data for temperatures below 0°C and above 70°C is applicable to Series 54S circuits only.

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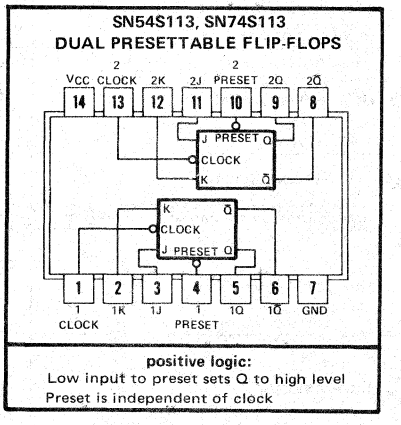
Typical Maximum Input Clock Frequency . . . 125 MHz
Typical Power Dissipation . . . 75 mW per Flip-Flop

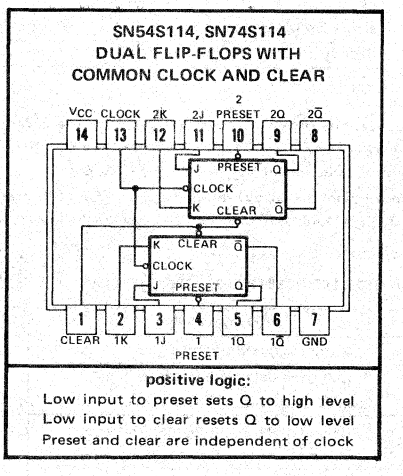
TRUTH TABLE

t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

NOTES: A. t_n = Bit time before clock pulse.
B. t_{n+1} = Bit time after clock pulse.

J OR N DUAL-IN-LINE OR W FLAT PACKAGE (TOP VIEW)





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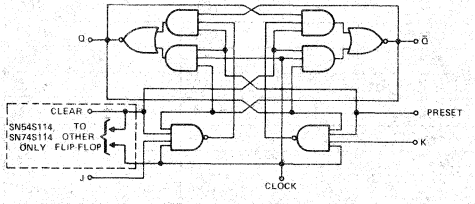
functional block diagram (each flip-flop)



description

The SN54S113 and SN74S113 offer individual J, K, preset, and clock inputs. The SN54S114 and SN74S114 offer common clock and common clear inputs and individual J, K, and preset inputs.

These monolithic dual flip-flops are designed so that when the clock goes high, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is high and the bistable will perform according to the truth table as long as minimum setup times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

recommended operating conditions

		SN54S113 SN54S114			SN74S113 SN74S114			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Input clock frequency, f_{clock}		0		80	0		80	MHz
Width of clock pulse, $t_{w(clock)}$		6			6			ns
Width of preset pulse, $t_{w(preset)}$		8			8			ns
Width of clear pulse, $t_{w(clear)}$	SN54S114, SN74S114	8			8			ns
Input setup time, t_{setup}		3			3			ns
Input hold time, t_{hold}		0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN545113 SN74S113			SN54S114 SN74S114			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1 mA	Series 54S	2.5	3.4		2.5	3.4		V
			Series 74S	2.7	3.4		2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 20 mA			0.5			0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V	J or K input			50			50	μA
			Clock			100			200	
			Preset			100			100	
			Clear						200	
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V	J or K input			−1.6			−1.6	mA
			Clock			−4			−8	
			Preset			−7			−7	
			Clear						−14	
I_{OS}	Short circuit output current§	V_{CC} = MAX		−40		−100	−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 3		30	50		30	50	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type. See Figures 64 through 69 of the Series 54H/74H section for test circuits.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

NOTE 3: I_{CC} is measured with outputs open, clock grounded, and J, K, preset, and clear at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS¶	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 280 Ω	80	125		MHz
t_{PLH}	Propagation delay time, low-to-high-level output, from clear or preset		2	4	7	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from clear or preset		2	5	7	ns
t_{PLH}	Propagation delay time, low-to-high-level output, from clock		2	4	7	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from clock		2	5	7	ns

¶ Switching characteristic measurements are made utilizing the same test circuits as illustrated for Darlington outputs in Figures 77 and 78 of the Series 54H/74H section. Information in the notes of these figures pertaining to the SN74H108 is applicable except $t_1 = t_0 = 2.5$ ns for all input pulse characteristics and the steady-state J and K input voltages are 2.7 V instead of 2.4 V.

TEXAS INSTRUMENTS
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Series 54/74 Circuits

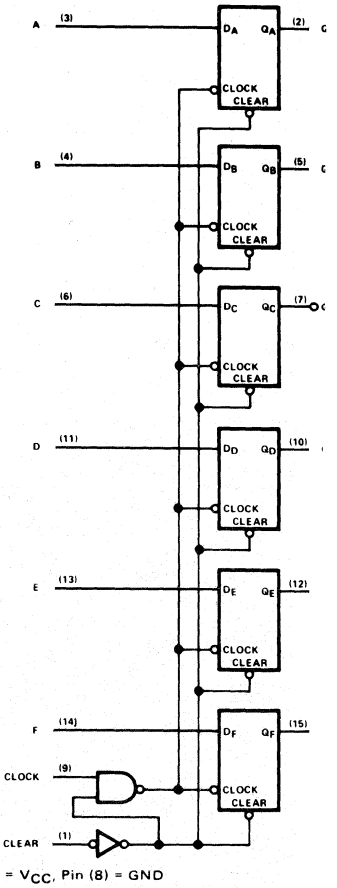
New TTL/MSI Now Available

SN54/74175 Quad and SN54/74174 HEX D-Type Flip-Flops With Direct Clear

- Replace latch circuits with clocked operation
- Reduce F-F Package count by 50 to 66
- Fully buffered inputs/outputs
- Economical for use as:
  - Buffer registers
  - Shift registers
  - Shift-register generators
  - Pattern generators
  - Scratch-pad memories

LOGIC

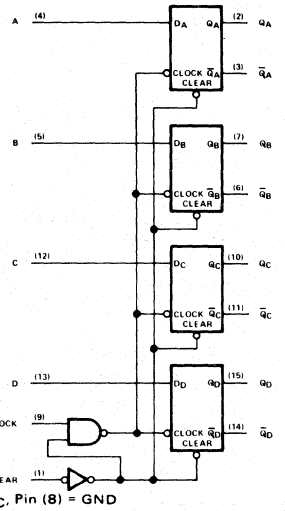
SN54174, SN74174



Pin (16) = V_{CC}, Pin (8) = GND

LOGIC

SN54175, SN74175



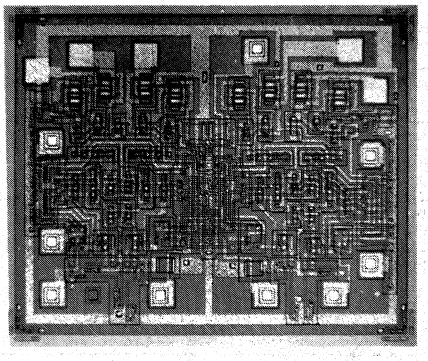
Pin (16) = V_{CC}, Pin (8) = GND

Available in 16-pin
J, N, and W packages

HIGH-SPEED SATURATED TRANSISTOR-TRANSISTOR LOGIC CIRCUITS FOR GENERAL-PURPOSE DIGITAL SYSTEM APPLICATIONS

description

TYPICAL DUAL FLIP-FLOP CIRCUIT BAR



Series 54/74 integrated circuits are designed and characterized for high-speed, general-purpose digital applications where high d-c noise margin and relatively low power dissipation are important system considerations. This logic series includes the basic gates, flip-flop elements, and complex logic and storage elements needed to perform all functions of general-purpose digital systems. Series 54 and 74 are completely compatible with Series 54H/74H, 54L/74L, and 54S/74S TTL logic families. Compatibility of these four TTL families permits improved systems design as the logician is permitted the flexibility of selecting component switching speed or circuit power dissipation with respect to system requirements. Series 54H/74H or 54S/74S high-speed TTL circuits can be selectively used to perform those functions requiring minimal propagation delay times. Series 54L/74L low-power TTL circuits can be used to reduce total power requirements. All four TTL families are designed to operate at the same supply voltages and compatible logic levels. In addition, high d-c noise margins characteristic of TTL circuits are maintained.

6

Definitive specifications are provided for operating characteristics over the full military temperature range of −55°C to 125°C for Series 54 circuits, and over the temperature range of 0°C to 70°C for Series 74 circuits.

features

LOW SYSTEM COST

- **choice of packages — ceramic flat package**
  — economical dual-in-line plastic package
  — ceramic dual-in-line package
- **broad selection of SSI and MSI functions — reduces package count**

OPTIMUM CIRCUIT PERFORMANCE

- **high speed — typical gate propagation delay time of 10 ns**
- **high d-c noise margin — typically one volt**
- **low output impedance provides low a-c noise susceptibility**
- **diode-clamped inputs simplify system design**
- **low power dissipation — 10 mW per gate at 50% duty cycle**
- **full fan-out —10 Series 54/74L loads**
  — 40 Series 54L/74L loads
  — 8 Series 54S/74S or 54H/74H loads
- **compatible for use with other current-sinking logic families — DTL, other TTL**
- **all inputs are diode clamped to minimize transmission-line effects**

SERIES 54/74
FEATURING 10 ns SPEED AND 10 mW PER GATE PERFORMANCE
SMALL SCALE INTEGRATION (SSI)

FUNCTION	OPERATING TEMPERATURE RANGES		PACKAGES*			SEC.-PAGE
	–55°C to 125°C	0°C to 70°C	Dual-In-Line		Flat	
NAND/NOR/AND/OR GATES AND BUFFERS						
Quadruple 2-Input Positive NAND Gates	SN5400	SN7400	J	N	W	6-5
Quadruple 2-Input Positive NAND Gates (with Open-Collector Output)	SN5401	SN7401	J	N	W	6-6
Quadruple 2-Input Positive NOR Gates	SN5402	SN7402	J	N	W	6-9
Quadruple 2-Input Positive NAND Gates (with Open-Collector Output)	SN5403	SN7403	J	N		6-10
Hex Inverters	SN5404	SN7404	J	N	W	6-11
Hex Inverters (with Open-Collector Output)	SN5405	SN7405	J	N	W	6-12
Hex Inverter Buffers/Drivers (with Open-Collector High-Voltage Output)	SN5406	SN7406	J	N	W	6-13
Hex Buffers/Drivers (with Open-Collector High-Voltage Output)	SN5407	SN7407	J	N	W	6-15
Quadruple 2-Input Positive AND Gates	SN5408	SN7408	J	N	W	6-17
Quadruple 2-Input Positive AND Gates	SN5409	SN7409	J	N	W	6-17
Triple 3-Input Positive NAND Gates	SN5410	SN7410	J	N	W	6-20
Triple 3-Input Positive NAND Gates (with Open-Collector Output)	SN5412	SN7412	J	N	W	6-21
Dual NAND Schmitt Triggers	SN5413	SN7413	J	N	W	6-22
Hex Inverter Buffers/Drivers (with Open-Collector High-Voltage Output)	SN5416	SN7416	J	N	W	6-13
Hex Buffers/Drivers (with Open-Collector High-Voltage Output)	SN5417	SN7417	J	N	W	6-15
Dual 4-Input Positive NAND Gates	SN5420	SN7420	J	N	W	6-26
Expandable Dual 4-Input Positive NOR Gates (with Strobe)	SN5423	SN7423	J	N	W	6-27
Dual 4-Input Positive NOR Gates	SN5425	SN7425	J	N	W	6-27
Quadruple 2-Input High-Voltage Interface NAND Gates	SN5426	SN7426	J	N		6-30
Triple 3-Input Positive NOR Gates	SN5427	SN7427	J	N	W	6-32
8-Input Positive NAND Gates	SN5430	SN7430	J	N	W	6-34
Quadruple 2-Input Positive OR Gates	SN5432	SN7432	J	N	W	6-35
Quadruple 2-Input Positive NAND Buffers	SN5437	SN7437	J	N	W	6-37
Quadruple 2-Input Positive NAND Buffers (with Open-Collector Output)	SN5438	SN7438	J	N	W	6-37
Dual 4-Input Positive NAND Buffers	SN5440	SN7440	J	N	W	6-39

SEE PAGES 9-1, 9-2, AND 9-3 FOR LISTING OF TTL MSI CIRCUITS

*For outline drawings of all packages, see Section 1.

–SEE ORDERING INSTRUCTIONS PAGE 1-1–

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

SERIES 54/74
FEATURING 10 ns SPEED AND 10 mW PER GATE PERFORMANCE
SMALL SCALE INTEGRATION (SSI)

FUNCTION	OPERATING TEMPERATURE RANGES		PACKAGES*			SEC.-PAGE
	−55°C to 125°C	0°C to 70°C	Dual-In-Line		Flat	
AND-OR-INVERT GATES						
Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gates	SN5450	SN7450	J	N	W	6-40
Dual 2-Wide 2-Input AND-OR-INVERT Gates	SN5451	SN7451	J	N	W	6-40
Expandable 4-Wide 2-Input AND-OR-INVERT Gates	SN5453	SN7453	J	N	W	6-42
4-Wide 2-Input AND-OR-INVERT Gates	SN5454	SN7454	J	N	W	6-42
EXPANDERS						
Dual 4-Input Expander	SN5460		J	N	W	6-44
Dual 4-Input Expander		SN7460	J	N	W	6-45
FLIP-FLOPS						
Positive Edge-Triggered J-K Flip-Flops (AND Inputs)	SN5470	SN7470	J	N	W	6-46
J-K Master-Slave Flip-Flops (AND Inputs)	SN5472	SN7472	J	N	W	6-49
Dual J-K Master-Slave Flip-Flops	SN5473	SN7473	J	N	W	6-52
Dual D-Type Edge-Triggered Flip-Flops	SN5474	SN7474	J	N	W	6-55
Dual-J-K Master-Slave Flip-Flops with Preset and Clear	SN5476	SN7476	J	N	W	6-58
Gated J-K Master-Slave Flip-Flops	SN54104	SN74104	J	N	W	6-61
Gated J-K Master-Slave Flip-Flops	SN54105	SN74105	J	N	W	6-61
Dual J-K Master-Slave Flip-Flops (V_{CC}-14, Gnd-7)	SN54107	SN74107	J	N		6-52
Gated J-K Master-Slave Flip-Flops with Data Lockout	SN54110	SN74110	J	N	W	6-66
Dual J-K Master-Slave Flip-Flops with Data Lockout	SN54111	SN74111	J	N	W	6-69
Monostable Multivibrators	SN54121	SN74121	J	N	W	6-72
Retriggerable Monostable Multivibrators with Clear	SN54122	SN74122	J	N	W	6-79
Dual Retriggerable Monostable Multivibrators with Clear	SN54123	SN74123	J	N	W	6-79

SEE PAGES 9-1, 9-2, AND 9-3 FOR LISTING OF TTL MSI CIRCUITS

*For outline drawings of all packages, see Section 1.

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1)	7 V
Input Voltage, V_{in} (See Note 1)	5.5 V
Interemitter Voltage (See Note 2)	5.5 V
Resistor Node Voltage, SN54121, SN74121 (See Note 1)	−5.5 V to 7 V
Operating Free-Air Temperature Range: Series 54 Circuits	−55°C to 125°C
Series 74 Circuits	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor.

logic definition

Series 54/74 logic is defined in terms of standard POSITIVE LOGIC using the following definitions:

HIGH VOLTAGE = LOGICAL 1

LOW VOLTAGE = LOGICAL 0

input clamping diodes

Although not shown on all schematic diagrams, all of these SSI circuits incorporate input diodes. Each clamping diode is capable of limiting negative excursions at the input to a maximum of 1.5 volts below ground, even if −12 mA of current is drawn.

unused inputs of NAND/AND gates

6

For optimum switching times and minimum noise susceptibility, unused inputs should be maintained at a positive voltage greater than 2.4 V but not exceed the absolute maximum rating of 5.5 V. This eliminates the distributed capacitance associated with the floating input-transistor emitter, bond wire, and package lead, and ensures that no degradation will occur in the propagation delay times. Some possible ways of handling input emitters are:

a. Connect unused inputs to an independent supply voltage. Preferably, this voltage should be between 2.4 V and 3.5 V.
b. Connect unused inputs to a used input if maximum fan-out of the driving output will not be exceeded. Each input presents a full load in the logical 1 state to the driving output.
c. Connect unused inputs to V_{CC} through a 1-kΩ resistor so that if a transient which exceeds the 5.5-V maximum rating should occur, the impedance will be high enough to protect the input. One to 25 unused inputs may be connected to each 1-kΩ resistor.

input-current requirements

Input-current requirements reflect worst-case conditions over the specified recommended operating free-air temperature and V_{CC} ranges. Each input, of the multiple emitter input transistors which have a 4-kΩ base resistor, requires that no more than −1.6 mA flow out of the input at a logical 0 voltage level; therefore, one load (N = 1) is −1.6 mA maximum. Each input requires current into the input at a logical 1 voltage level. This current is 40 μA maximum for each emitter of input transistors with the 4-kΩ base resistor. Currents into the input terminals are specified as positive values. Arrows on the d-c test circuits indicate the actual direction of current flow.

fan-out capability

Fan-out reflects the ability of an output to sink current from a number of loads (N) at a logical 0 voltage level and to supply current at a logical 1 voltage level. Each standard output is capable of sinking current or supplying current to 10 loads (N = 10). The buffer gate is capable of sinking current or supplying current to 30 loads (N = 30). Load currents (out of the output terminal) are specified as negative values. Arrows on the d-c test circuits indicate the actual direction of current flow.

Series 54/74 circuits are well suited for driving Series 54H/74H and 54S/74S high-speed TTL and Series 54L/74L low-power TTL circuits. As examples, a Series 54/74 output, rated for a fan-out of ten (N=10), will drive eight 54H/74H loads or forty 54/74L loads.

TEXAS INSTRUMENTS
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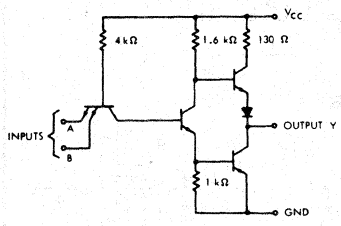
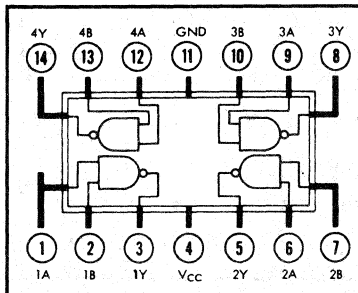
schematic (each gate)

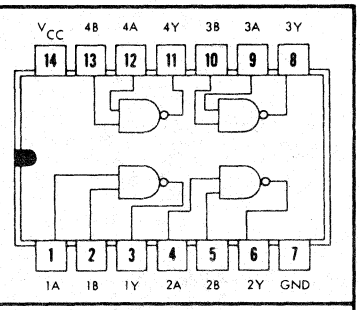


NOTE: Component values shown are nominal.

W FLAT PACKAGE
(TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: $Y = \overline{AB}$

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	SN5400 Circuits	4.5	5	5.5	V
	SN7400 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N				10	
Operating Free-Air Temperature Range, T_A:	SN5400 Circuits	−55	25	125	°C
	SN7400 Circuits	0	25	70	°C

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals to ensure logical 0 level at output	1			2			V
$V_{in(0)}$	Logical 0 input voltage required at either input terminal to ensure logical 1 level at output	2					0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −400 μA		2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 16 mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current§	5	V_{CC} = MAX	SN5400	−20		−55	mA
				SN7400	−18		−55	
$I_{CC(0)}$	Logical 0 level supply current	6	V_{CC} = MAX, V_{in} = 5 V			12	22	mA
$I_{CC(1)}$	Logical 1 level supply current	6	V_{CC} = MAX, V_{in} = 0			4	8	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	65	C_L = 15 pF, R_L = 400 Ω		7	15	ns
t_{pd1}	Propagation delay time to logical 1 level	65	C_L = 15 pF, R_L = 400 Ω		11	22	ns

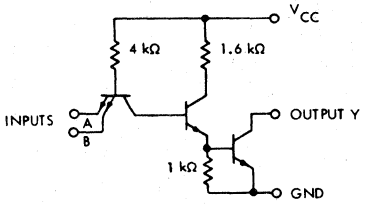
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

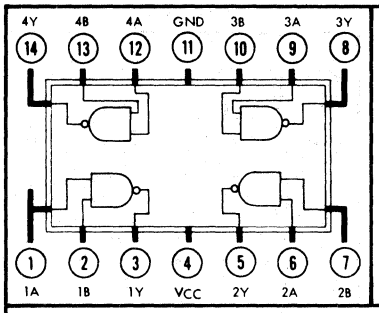
CIRCUIT TYPES SN5401, SN7401
QUADRUPLE 2-INPUT POSITIVE NAND GATES
(WITH OPEN-COLLECTOR OUTPUT)

schematic (each gate)

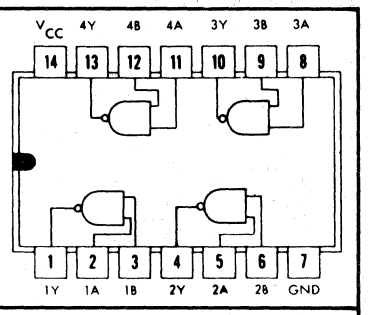


NOTE: Component values shown are nominal.

W FLAT PACKAGE (TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{AB}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN5401 Circuits	4.5	5	5.5	V
SN7401 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN5401 Circuits	−55	25	125	°C
SN7401 Circuits	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals to ensure logical 0 (on) level at output	1			2			V
$V_{in(0)}$	Logical 0 input voltage required at either input terminal to ensure logical 1 (off) level at output	7					0.8	V
$I_{out(1)}$	Output reverse current	7	V_{CC} = MIN, $V_{out(1)}$ = 5.5 V	V_{in} = 0.8 V,			250	μA
$V_{out(0)}$	Logical 0 output voltage (on level)	1	V_{CC} = MIN, I_{sink} = 16 mA	V_{in} = 2 V,			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX,	V_{in} = 0.4 V			−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX,	V_{in} = 2.4 V			40	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
$I_{CC(0)}$	Logical 0 level supply current	6	V_{CC} = MAX,	V_{in} = 5 V		12	22	mA
$I_{CC(1)}$	Logical 1 level supply current	6	V_{CC} = MAX,	V_{in} = 0		4	8	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	65	C_L = 15 pF,	R_L = 400 Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	65	C_L = 15 pF,	R_L = 4 kΩ		35	45	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

APPLICATION DATA

combined fan-out and wire-AND capabilities

The open-collector TTL gate, when supplied with a proper load resistor (R_L), can be paralleled with other similar TTL gates to perform the wire-AND function, and simultaneously, will drive from one to nine Series 54 TTL loads. When no other open-collector gates are paralleled, this gate can be used to drive ten TTL loads. For any of these conditions an appropriate load resistor value must be determined for the desired circuit configuration. A maximum resistor value must be determined which will ensure that sufficient load current (to TTL loads) and off current (through paralleled outputs) will be available during a logical 1 level at output. A minimum resistor value must be determined which will ensure that current through this resistor and sink current from the TTL loads will not cause the output voltage to rise above the logical 0 level even if one of the paralleled outputs is sinking all the current.

In both conditions (logical 0 and logical 1) the value of R_L is determined by:

$$R_L = \frac{V_{RL}}{I_{RL}}$$

where: V_{RL} is the voltage drop in volts, and I_{RL} is the current in amperes.

logical 1 (off level) circuit calculations (see figure F)

The allowable voltage drop across the load resistor (V_{RL}) is the difference between V_{CC} applied and the $V_{out(1)}$ level required at the load:

$$V_{RL} = V_{CC} - V_{out(1)\ required}$$

The total current through the load resistor (I_{RL} is the sum of the load currents ($I_{in(1)}$) and off-level reverse currents ($I_{out(1)}$ through each of the wire-AND connected outputs:

$$I_{RL} = \eta \cdot I_{out(1)} + N \cdot I_{in(1)} \text{ to TTL loads}$$

Therefore, calculations for the maximum value of R_L would be:

$$R_{L(max)} = \frac{V_{CC} - V_{out(1)\ required}}{\eta \cdot I_{out(1)} + N \cdot I_{in(1)}}$$

where: η = number of gates wire-AND connected, and N = number of TTL loads.

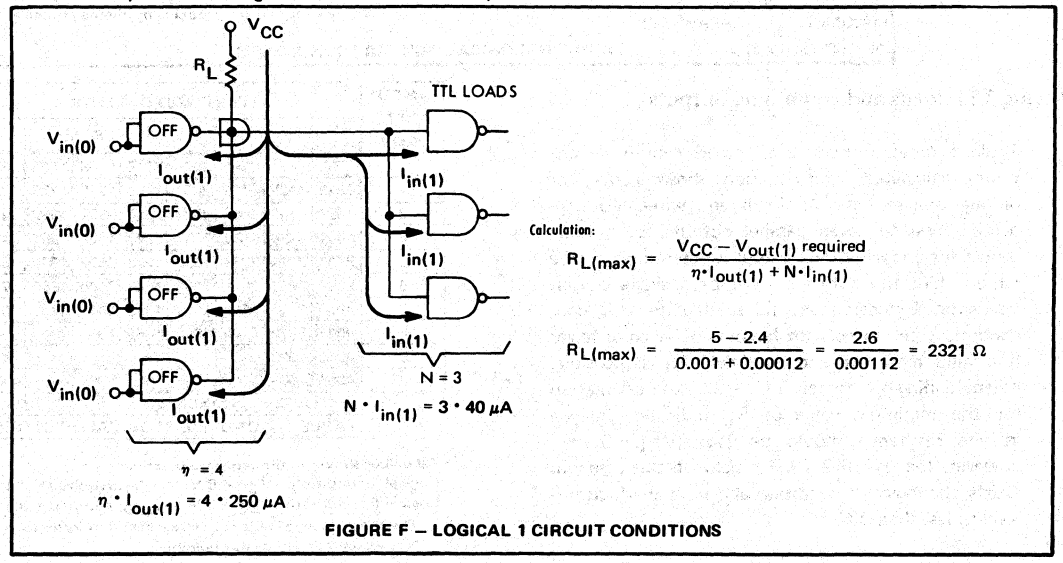


FIGURE F – LOGICAL 1 CIRCUIT CONDITIONS

APPLICATION DATA

logical 0 (on level) circuit calculations (see figure G)

The current through the resistor must be limited to the maximum sink-current capability of one output transistor. Note that if several output transistors are wire-AND connected, the current through R_L may be shared by those paralleled transistors. However, unless it can be absolutely guaranteed that more than one transistor will be on during logical 0 periods, the current must be limited to 16 mA, the maximum current which will ensure a logical 0 maximum of 0.4 volts.

Also, fan-out must be considered. Part of the 16 mA will be supplied from the inputs which are being driven. This reduces the amount of current allowed through R_L.

Therefore, the equation used to determine the minimum value of R_L is:

$$R_{L(min)} = \frac{V_{CC} - V_{out(0)\ required}}{I_{sink\ capability} - I_{sink\ from\ TTL\ loads}}$$

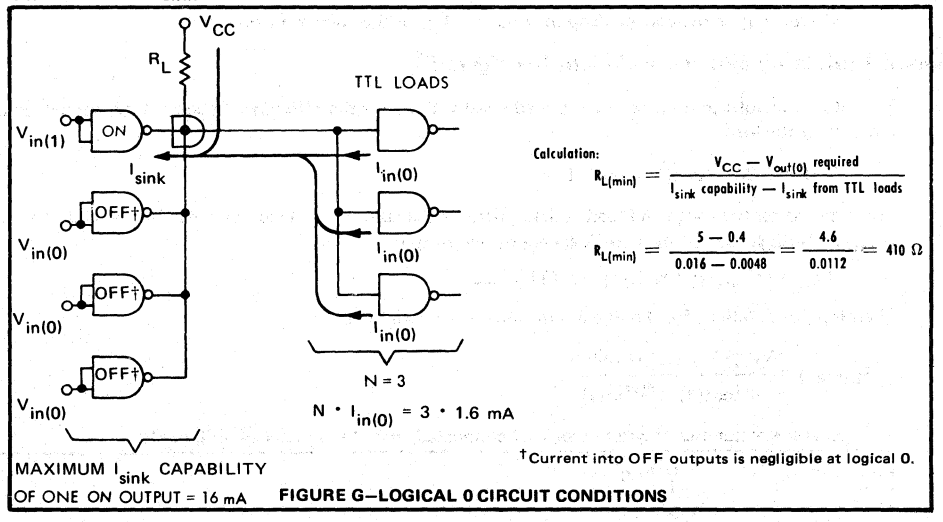


FIGURE G–LOGICAL 0 CIRCUIT CONDITIONS

driving TTL loads and combining outputs

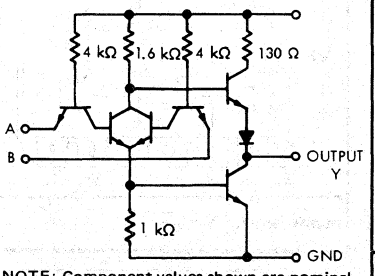
Table I provides minimum and maximum resistor values, calculated from equations shown above, for driving one to ten TTL loads and wire-AND connecting two to seven parallel outputs. Each value shown for one wire-AND output is determined by the fan-out plus the cutoff current of a single output transistor. Extension beyond seven wire-AND connections is permitted with fan-outs of seven or fewer if a valid minimum and maximum R_L is possible. When fanning-out to ten TTL loads, the calculation for the minimum value of R_L indicates that an infinite resistance should be used ($V_{RL} \div 0 = \infty$); however, the use of a 4 kΩ resistor in this case will satisfy the logical 1 condition and limit the logical 0 level to less than 0.43 V.

FAN-OUT TO TTL LOADS	WIRE-AND OUTPUTS							
	1	2	3	4	5	6	7	1 to 7
1	8965	4814	3291	2500	2015	1688	1452	319
2	7878	4482	3132	2407	1954	1645	1420	359
3	7027	4193	2988	2321	1897	1604	1390	410
4	6341	3939	2857	2241	1843	1566	1361	479
5	5777	3714	2736	2166	1793	1529	1333	575
6	5306	3513	2626	2096	1744	1494	1306	718
7	4905	3333	2524	2031	1699	1460	1280	958
8	4561	3170	2429	1969	1656	X	X	1437
9	4262	3023	X	X	X	X	X	2875
10	4000	X	X	X	X	X	X	4000§
	MAXIMUM							MIN

TABLE 1–LOAD RESISTOR VALUE IN OHMS

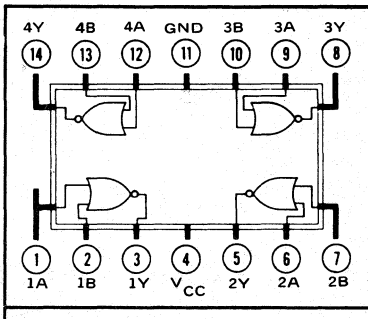
‡ All values shown in the table are based on:
Logical 1 conditions: V_{CC} = 5 V, $V_{out(1)}$ required = 2.4 V
Logical 0 conditions: V_{CC} = 5 V, $V_{out(0)}$ required = 0.4 V
§ – The theoretical value is ∞. See explanation in text.
X – Not recommended or not possible.

schematic (each gate)

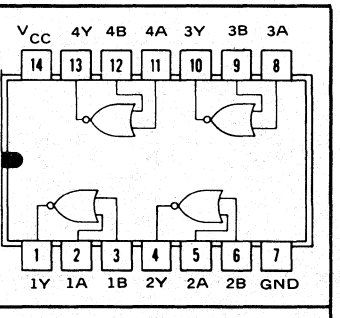


NOTE: Component values shown are nominal.

W FLAT PACKAGE
(TOP VIEW)



J OR N-DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: $Y = \overline{A + B}$

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	SN5402 Circuits	4.5	5	5.5	V
	SN7402 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N				10	
Operating Free-Air Temperature Range, T_A:	SN5402 Circuits	−55	25	125	°C
	SN7402 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at either input terminal to ensure logical 0 level at output	8			2			V
$V_{in(0)}$	Logical 0 input voltage required at both input terminals to ensure logical 1 level at output	9					0.8	V
$V_{out(1)}$	Logical 1 output voltage	9	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −400 μA		2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	10	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 16 mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	11	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	12	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current§	13	V_{CC} = MAX	SN5402	−20		−55	mA
				SN7402	−18		−55	
$I_{CC(0)}$	Logical 0 level supply current	14	V_{CC} = MAX, V_{in} = 5 V			14	27	mA
$I_{CC(1)}$	Logical 1 level supply current	14	V_{CC} = MAX, V_{in} = 0			8	16	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	65	C_L = 15 pF, R_L = 400 Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	65	C_L = 15 pF, R_L = 400 Ω		12	22	ns

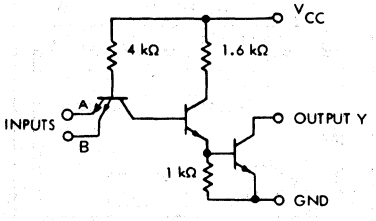
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

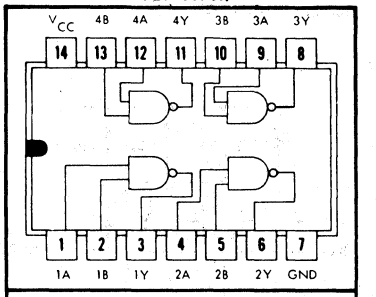
CIRCUIT TYPES SN5403, SN7403
QUADRUPLE 2-INPUT POSITIVE NAND GATES
(WITH OPEN-COLLECTOR OUTPUT)

schematic (each gate)



NOTE: Component values shown are nominal.

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: $Y = \overline{AB}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN5403 Circuits	4.5	5	5.5	V
SN7403 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N (and see pages 2-7 and 2-8)			10	
Operating Free-Air Temperature Range, T_A: SN5403 Circuits	−55	25	125	°C
SN7403 Circuits	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals to ensure logical 0 (on) level at output)	1		2			V
$V_{in(0)}$	Logical 0 input voltage required at either input terminal to ensure logical 1 (off) level at output	7				0.8	V
$I_{out(1)}$	Output reverse current	7	V_{CC} = MIN, V_{in} = 0.8 V, $V_{out(1)}$ = 5.5 V			250	μA
$V_{out(0)}$	Logical 0 output voltage (on level)	1	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 16 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.4 V			−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX, V_{in} = 2.4 V			40	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{CC(0)}$	Logical 0 level supply current	6	V_{CC} = MAX, V_{in} = 5 V		12	22	mA
$I_{CC(1)}$	Logical 1 level supply current	6	V_{CC} = MAX, V_{in} = 0		4	8	mA

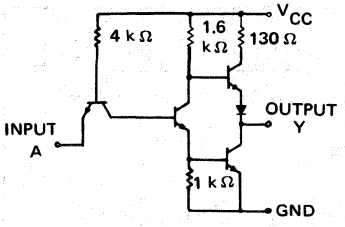
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	65	C_L = 15 pF, R_L = 400 Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	65	C_L = 15 pF, R_L = 4 kΩ		35	45	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

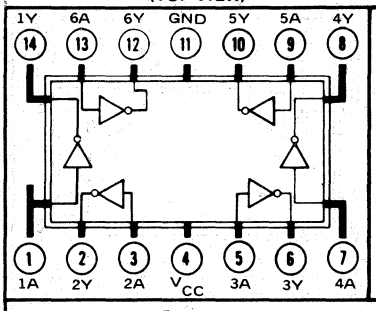
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

schematic (each inverter)

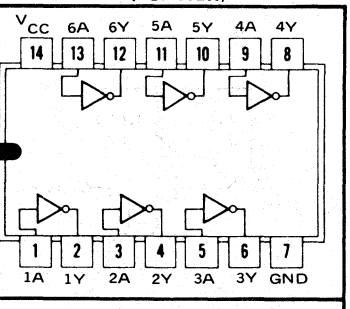


NOTE: Component values shown are nominal.

W FLAT PACKAGE
(TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: $Y = \bar{A}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN5404 Circuits	4.5	5	5.5	V
SN7404 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN5404 Circuits	−55	25	125	°C
SN7404 Circuits	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at input terminal to ensure logical 0 level at output	15			2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	16					0.8	V
$V_{out(1)}$	Logical 1 output voltage	16	V_{CC} = MIN, I_{load} = −400 μA	V_{in} = 0.8 V,	2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	15	V_{CC} = MIN, I_{sink} = 16 mA	V_{in} = 2 V,		0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current	18	V_{CC} = MAX,	V_{in} = 0.4 V			−1.6	mA
$I_{in(1)}$	Logical 1 level input current	18	V_{CC} = MAX,	V_{in} = 2.4 V			40	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current§	19	V_{CC} = MAX	SN5404	−20		−55	mA
				SN7404	−18		−55	
$I_{CC(0)}$	Logical 0 level supply current	20	V_{CC} = MAX,	V_{in} = 5 V		18	33	mA
$I_{CC(1)}$	Logical 1 level supply current	20	V_{CC} = MAX,	V_{in} = 0		6	12	mA

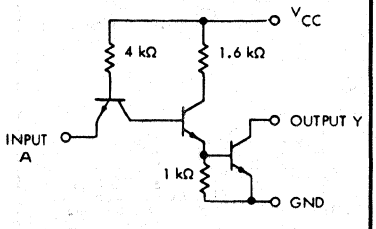
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	65	C_L = 15 pF,	R_L = 400 Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	65	C_L = 15 pF,	R_L = 400 Ω		12	22	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

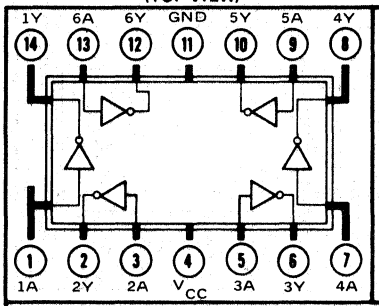
CIRCUIT TYPES SN5405, SN7405
HEX INVERTERS (WITH OPEN-COLLECTOR OUTPUT)

schematic (each inverter)

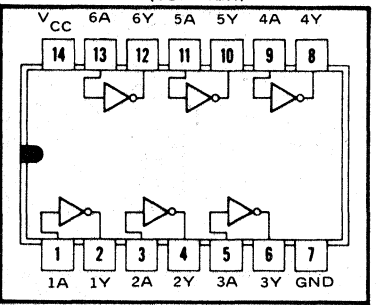


NOTE: Component values shown are nominal.

W FLAT PACKAGE
(TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic $Y = \overline{A}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN5405 Circuits	4.5	5	5.5	V
SN7405 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N (and see pages 2-7 and 2-8)			10	
Operating Free-Air Temperature Range, T_A: SN5405 Circuits	−55	25	125	°C
SN7405 Circuits	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at input terminal to ensure logical 0 (on) level at output	15			2			V
$V_{in(0)}$	Logical 0 input voltage required at input terminal to ensure logical 1 (off) level at output	17					0.8	V
$I_{out(1)}$	Output reverse current	17	V_{CC} = MIN, $V_{out(1)}$ = 5.5 V	V_{in} = 0.8 V,			250	μA
$V_{out(0)}$	Logical 0 output voltage (on level)	15	V_{CC} = MIN, I_{sink} = 16 mA	V_{in} = 2 V,			0.4	V
$I_{in(0)}$	Logical 0 level input current	18	V_{CC} = MAX,	V_{in} = 0.4 V			−1.6	mA
$I_{in(1)}$	Logical 1 level input current	18	V_{CC} = MAX,	V_{in} = 2.4 V			40	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
$I_{CC(0)}$	Logical 0 level supply current	20	V_{CC} = MAX, T_A = 25°C	V_{in} = 5 V,		18	33	mA
$I_{CC(1)}$	Logical 1 level supply current	20	V_{CC} = MAX, T_A = 25°C	V_{in} = 0,		6	12	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C

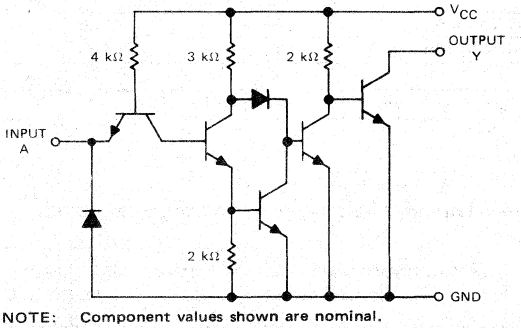
PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	65	C_L = 15 pF,	R_L = 400 Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	65	C_L = 15 pF,	R_L = 4 kΩ		40	55	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ These typical values are at V_{CC} = 5 V, T_A = 25°C.

FOR INTERFACING WITH HIGH-LEVEL CIRCUITS OR FOR DRIVING HIGH-CURRENT LOADS

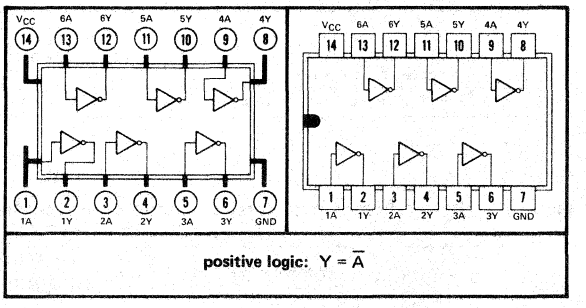
schematic (each inverter)



NOTE: Component values shown are nominal.

W FLAT PACKAGE (TOP VIEW)

J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)



- Converts TTL voltage levels to MOS levels
- High sink-current capability
- Input clamping diodes simplify system design
- Typical propagation delay time: 15 ns
- Open-collector driver for indicator lamps and relays
- Inputs fully compatible with most TTL and DTL circuits
- Typical power dissipation: 105 mW

6

description

These monolithic TTL hex inverter buffers/drivers feature high-voltage open-collector outputs for interfacing with high-level circuits (such as MOS), or for driving high-current loads (such as lamps or relays), and are also characterized for use as inverter buffers for driving TTL inputs. For increased fan-out, several inverters in a single package may be paralleled. The SN5406 and SN7406 have minimum breakdown voltages of 30 volts and the SN5416 and SN7416 have minimum breakdown voltages of 15 volts. The maximum sink current is 30 milliamperes for the SN5406 and SN5416, and 40 milliamperes for the SN7406 and SN7416.

These circuits are completely compatible with most TTL or DTL families. Inputs are diode-clamped to minimize transmission-line effects which simplifies design. Typical power dissipation is 150 milliwatts and average propagation delay time is 15 nanoseconds. The SN5406 and SN5416 are characterized for operation over the full military temperature range of −55°C to 125°C; the SN7406 and SN7416 are characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1)		7 V
Input voltage (see Note 1)		5.5 V
Output voltage (see Notes 1 and 2):	SN5406, SN7406 Circuits	30 V
	SN5416, SN7416 Circuits	15 V
Operating free-air temperature range:	SN5406, SN5416 Circuits	−55°C to 125°C
	SN7406, SN7416 Circuits	0°C to 70°C
Storage temperature range		−65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the maximum voltage which should be applied to any output when it is in the off state.

recommended operating conditions

		SN5406, SN5416			SN7406, SN7416			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Output voltage, V_{OH}	SN5406, SN7406			30			30	V
	SN5416, SN7416			15			15	
Low-level output current, I_{OL}				30			40	mA
Operating free-air temperature range, T_A		−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage	74		2			V
V_{IL}	Low-level input voltage	75				0.8	V
I_{OH}	High-level output current	75	V_{CC} = MIN, V_I = 0.8 V, V_{OH} = MAX			250	μA
V_{OL}	Low-level output voltage	74	V_{CC} = MIN, V_I = 2 V, I_{OL} = MAX			0.7	V
			V_{CC} = MIN, V_I = 2 V, I_{OL} = 16 mA			0.4	
I_{IH}	High-level input current (each input)	76	V_{CC} = MAX, V_I = 2.4 V			40	μA
			V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IL}	Low-level input current (each input)	77	V_{CC} = MAX, V_I = 0.4 V			−1.6	mA
I_{CCH}	Supply current, high-level output	78	V_{CC} = MAX, V_I = 0		30	42	mA
I_{CCL}	Supply current, low-level output	78	V_{CC} = MAX, V_I = 5 V		27	38	mA

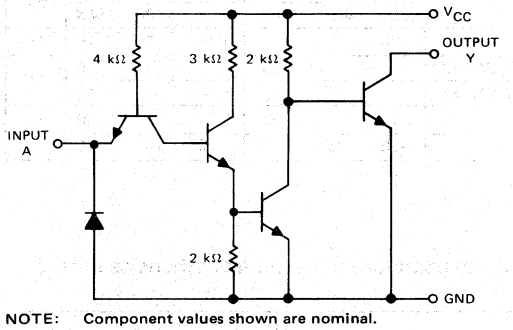
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	79	C_L = 15 pF, R_L = 110 Ω		10	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output	79	C_L = 15 pF, R_L = 110 Ω		15	23	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

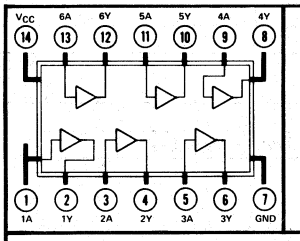
FOR INTERFACING WITH HIGH-LEVEL CIRCUITS OR FOR DRIVING HIGH-CURRENT LOADS

schematic (each buffer/driver)

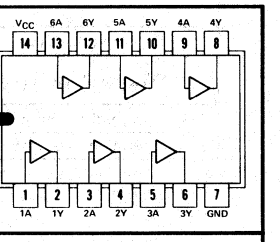


NOTE: Component values shown are nominal.

W
FLAT PACKAGE
(TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: Y = A

- **Converts TTL voltage levels to MOS levels**
- **High sink-current capability**
- **Input clamping diodes simplify system design**
- **Typical propagation delay time: 14 ns**
- **Open-collector driver for indicator lamps and relays**
- **Inputs fully compatible with most TTL and DTL circuits**
- **Typical power dissipation: 145 mW**

6

description

These monolithic TTL hex buffers/drivers feature high-voltage open-collector outputs for interfacing with high-level circuits (such as MOS), or for driving high-current loads (such as lamps or relays), and are also characterized for use as buffers for driving TTL inputs. For increased fan-out, several buffers in a single package may be paralleled. The SN5407 and SN7407 have minimum breakdown voltages of 30 volts and the SN5417 and SN7417 have minimum breakdown voltages of 15 volts. The maximum sink current is 30 milliamperes for the SN5407 and SN5417, and 40 milliamperes for the SN7407 and SN7417.

These circuits are completely compatible with most TTL and DTL families. Inputs are diode-clamped to minimize transmission-line effects which simplifies design. Typical power dissipation is 145 milliwatts and average propagation delay time is 14 nanoseconds. The SN5407 and SN5417 are characterized for operation over the full military temperature range of −55°C to 125°C; the SN7407 and SN7417 are characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1)		7 V
Input voltage (see Note 1)		5.5 V
Output voltage (see Notes 1 and 2):	SN5407, SN7407 Circuits	30 V
	SN5417, SN7417 Circuits	15 V
Operating free-air temperature range:	SN5407, SN5417 Circuits	−55°C to 125°C
	SN7407, SN7417 Circuits	0°C to 70°C
Storage temperature range		−65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the maximum voltage which should be applied to any output when it is in the off state.

recommended operating conditions

		SN5407, SN5417			SN7407, SN7417			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Output voltage, V_{OH}	SN5407, SN7407			30			30	V
	SN5417, SN7417			15			15	
Low-level output current, I_{OL}				30			40	mA
Operating free-air temperature range, T_A		−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage	80		2			V
V_{IL}	Low-level input voltage	81				0.8	V
I_{OH}	High-level output current	80	V_{CC} = MIN, V_I = 2 V, V_{OH} = MAX			250	μA
V_{OL}	Low-level output voltage	81	V_{CC} = MIN, V_I = 0.8 V, I_{OL} = MAX			0.7	V
			V_{CC} = MIN, V_I = 0.8 V, I_{OL} = 16 mA			0.4	
I_{IH}	High-level input current (each input)	82	V_{CC} = MAX, V_I = 2.4 V			40	μA
			V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IL}	Low-level input current (each input)	83	V_{CC} = MAX, V_I = 0.4 V			−1.6	mA
I_{CCH}	Supply current, high-level output	84	V_{CC} = MAX, V_I = 5 V		29	41	mA
I_{CCL}	Supply current, low-level output	84	V_{CC} = MAX, V_I = 0		21	30	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C

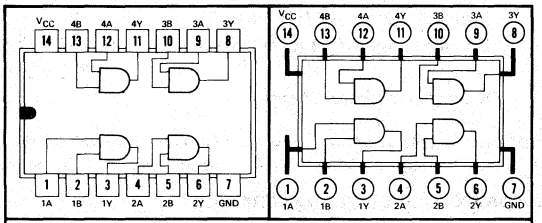
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	85	C_L = 15 pF, R_L = 110 Ω		6	10	ns
t_{PHL}	Propagation delay time, high-to-low-level output	85	C_L = 15 pF, R_L = 110 Ω		20	30	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

Choice of Totem-Pole Outputs (SN5408/SN7408) or Open-Collector Outputs (SN5409/SN7409)

J OR N
DUAL-IN-LINE PACKAGE
(TOP VIEW)

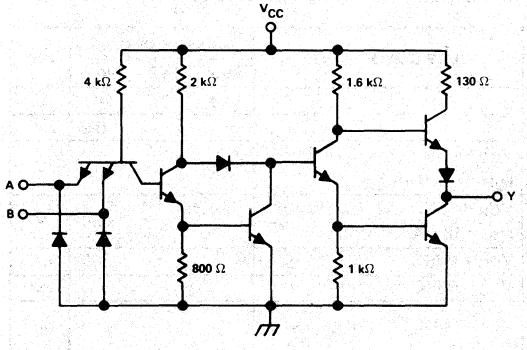
W
FLAT PACKAGE
(TOP VIEW)



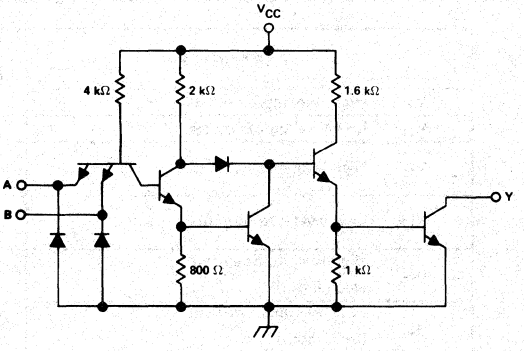
positive logic: Y = AB

schematics (each gate)

SN5408, SN7408



SN5409, SN7409



Component values shown are nominal.

description

These Series 54/74 TTL gates provide the system designer with direct implementation of the positive AND or negative OR functions.

The SN5408/SN7408, with totem-pole outputs, drives 10 normalized Series 54/74 loads at the low output level and 20 loads at the high output level. The SN5409/SN7409, with open-collector output, provides additional logic flexibility, as the outputs may be wire-AND connected to extend the AND function. The SN5409/SN7409 will sink sufficient current to drive 10 normalized Series 54/74 loads at the low output level.

The SN5408 and SN5409 are characterized for operation over the full military temperature range of −55°C to 125°C; the SN7408 and SN7409 are characterized for operation from 0°C to 70°C.

CIRCUIT TYPES SN5408, SN5409, SN7408, SN7409
QUADRUPLE 2-INPUT POSITIVE AND GATES

SN5408, SN7408

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range, T_A: SN5408 Circuits . . . . . −55°C to 125°C
SN7408 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor.

recommended operating conditions

	SN5408			SN7408			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N			10			10	
Operating free-air temperature range, T_A	−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		SN5408, SN7408			UNIT
					MIN	TYP‡	MAX	
V_{IH}	High-level input voltage	86			2			V
V_{IL}	Low-level input voltage	88					0.8	V
V_{OH}	High-level output voltage	86	V_{CC} = MIN, I_{OH} = −800 μA	V_{IH} = 2 V,	2.4			V
V_{OL}	Low-level output voltage	88	V_{CC} = MIN, I_{OL} = 16 mA	V_{IL} = 0.8 V,			0.4	V
I_{IH}	High-level input current (each input)	89	V_{CC} = MAX,	V_I = 2.4 V			40	μA
			V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IL}	Low-level input current (each input)	90	V_{CC} = MAX,	V_I = 0.4 V			−1.6	mA
I_{OS}	Short-circuit output current§	91	V_{CC} = MAX	SN5408	−20		−55	mA
				SN7408	−18		−55	
I_{CCH}	Supply current, high-level output	92	V_{CC} = MAX,	V_I = 5 V		11	21	mA
I_{CCL}	Supply current, low-level output	92	V_{CC} = MAX,	V_I = 0		20	33	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	SN5408, SN7408			UNIT
				MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	93	C_L = 15 pF, R_L = 400 Ω		17.5	27	ns
t_{PHL}	Propagation delay time, high-to-low-level output				12	19	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

SN5409, SN7409

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Output voltage (see Notes 1 and 3) . . . . . 5.5 V
Operating free-air temperature range: SN5409 Circuits . . . . . −55°C to 125°C
SN7409 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor.
3. This is the maximum voltage which should be applied to any output when it is in the off state.

recommended operating conditions

	SN5409			SN7409			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N			10			10	
Operating free-air temperature range, T_A	−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	SN5409, SN7409			UNIT
				MIN	TYP‡	MAX	
V_{IH}	High-level input voltage	87		2			V
V_{IL}	Low-level input voltage	88				0.8	V
I_{OH}	High-level output current	87	V_{CC} = MIN, V_{IH} = 2 V, V_{OH} = 5.5 V			250	μA
V_{OL}	Low-level output voltage	88	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.4	V
I_{IH}	High-level input current (each input)	89	V_{CC} = MAX, V_I = 2.4 V			40	μA
			V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IL}	Low-level input current (each input)	90	V_{CC} = MAX, V_I = 0.4 V			−1.6	mA
I_{CCH}	Supply current, high-level output	92	V_{CC} = MAX, V_I = 5 V		11	21	mA
I_{CCL}	Supply current, low-level output	92	V_{CC} = MAX, V_I = 0		20	33	mA

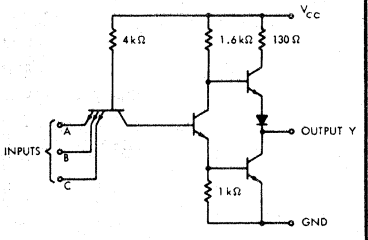
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	SN5409, SN7409			UNIT
				MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	93	C_L = 15 pF, R_L = 400 Ω		21	32	ns
t_{PHL}	Propagation delay time, high-to-low-level output				16	24	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

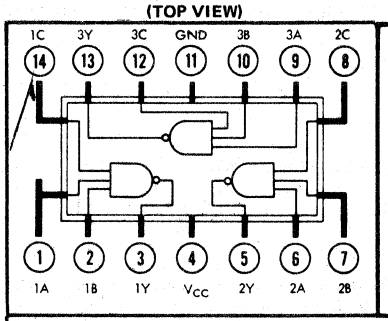
CIRCUIT TYPES SN5410, SN7410
TRIPLE 3-INPUT POSITIVE NAND GATES

schematic (each gate)

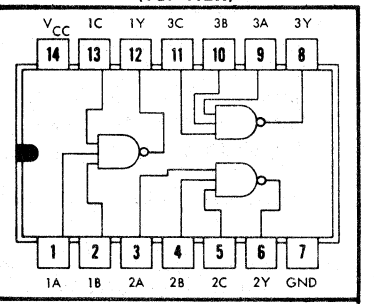


NOTE: Component values shown are nominal.

W FLAT PACKAGE
(TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: $Y = \overline{ABC}$

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	SN5410 Circuits	4.5	5	5.5	V
	SN7410 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N				10	
Operating Free-Air Temperature Range, T_A:	SN5410 Circuits	−55	25	125	°C
	SN7410 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1			2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2					0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −400 μA		2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 16 mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
I_{OS}	Short circuit output current§	5	V_{CC} = 5.5 V	SN5410	−20		−55	mA
				SN7410	−18		−55	
$I_{CC(0)}$	Logical 0 level supply current	6	V_{CC} = MAX, V_{in} = 5 V			9	16.5	mA
$I_{CC(1)}$	Logical 1 level supply current	6	V_{CC} = MAX, V_{in} = 0			3	6	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

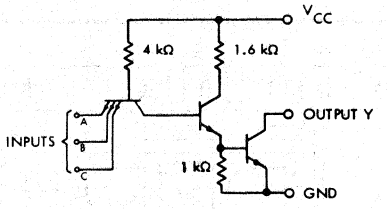
PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	65	C_L = 15 pF, R_L = 400 Ω			7	15	ns
t_{pd1}	Propagation delay time to logical 1 level	65	C_L = 15 pF, R_L = 400 Ω			11	22	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

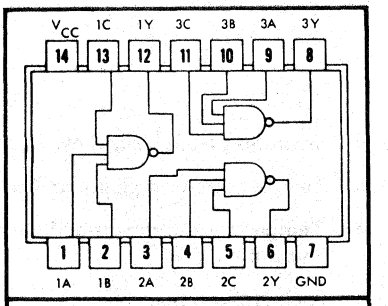
§ Not more than one output should be shorted at a time.

schematic (each gate)



NOTE: Component values shown are nominal.

J OR N DUAL-IN-LINE OR
W FLAT PACKAGES (TOP VIEW)



positive logic: $Y = \overline{ABC}$

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	SN5412 Circuits	4.5	5	5.5	V
	SN7412 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N				10	
Operating Free-Air Temperature Range, T_A:	SN5412 Circuits	−55	25	125	°C
	SN7412 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals to ensure logical 0 (on) level at output	1			2			V
$V_{in(0)}$	Logical 0 input voltage required at either input terminal to ensure logical 1 (off) level at output	7					0.8	V
$I_{out(1)}$	Output reverse current	7	V_{CC} = MIN, $V_{out(1)}$ = 5.5 V	$V_{in(0)}$ = 0.8 V,			250	μA
$V_{out(0)}$	Logical 0 output voltage (on level)	1	V_{CC} = MIN, I_{sink} = 16 mA	V_{in} = 2 V,			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX,	V_{in} = 0.4 V			−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX,	V_{in} = 2.4 V			40	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
$I_{CC(0)}$	Logical 0 level supply current	6	V_{CC} = MAX,	V_{in} = 5 V		9	16.5	mA
$I_{CC(1)}$	Logical 1 level supply current	6	V_{CC} = MAX,	V_{in} = 0		3	6	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C

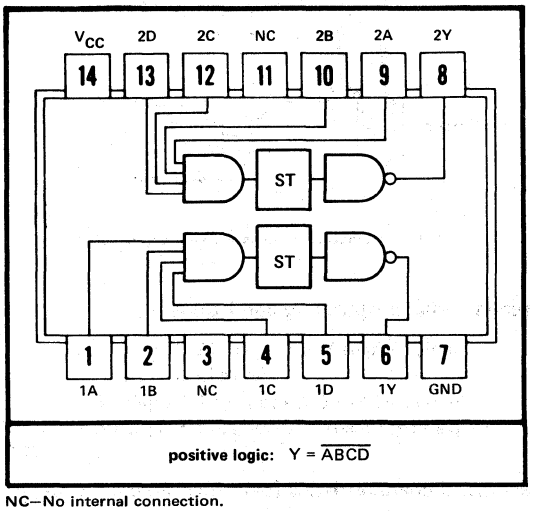
PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	65	C_L = 15 pF,	R_L = 400 Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	65	C_L = 15 pF,	R_L = 4 kΩ		35	45	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating condionts for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

CIRCUIT TYPES SN5413,SN7413
DUAL NAND SCHMITT TRIGGERS

- Operation from Very Slow Edges
- Temperature-Compensated Threshold Levels
- Temperature-Compensated Hysteresis, Typically 0.8 V
- High Noise Immunity

J OR N DUAL-IN-LINE OR
W FLAT PACKAGES (TOP VIEW)†



NC—No internal connection.
†Pin assignments for these circuits are the same for all packages.

description

6

The SN5413 and SN7413 dual Schmitt triggers consist of two identical Schmitt-trigger circuits in monolithic integrated circuit form. Logically, each circuit functions as a four-input NAND gate, but because of the Schmitt action, the gate has different input threshold levels for positive- and negative-going signals. The hysteresis, or backlash, which is the difference between the two threshold levels, is typically 800 mV.

An important design feature is the built-in temperature compensation which ensures very high stability of the threshold levels and the hysteresis over a very wide temperature range. Typically, the hysteresis changes by 3% over the temperature range of −55°C to 125°C and the upper threshold changes by 1% over the same range. The SN5413/SN7413 can be triggered from the slowest of input ramps and still give clean, jitter-free output signals. It can also be triggered from straight d-c levels.

These circuits are fully compatible with most other TTL, DTL, or MSI circuits. The SN5413 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN7413 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1)		7 V
Input voltage (see Note 1)		5.5 V
Interemitter voltage (see Note 2)		5.5 V
Operating free-air temperature range:	SN5413 Circuits	−55°C to 125°C
	SN7413 Circuits	0°C to 70°C
Storage temperature range		−65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor.

recommended operating conditions

		SN5413			SN7413			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Operating free-air temperature range, T_A		−55	0	125	0	25	70	°C
Maximum input rise and fall times		No restriction			No restriction			

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{T+}	Positive-going threshold voltage	94	V_{CC} = 5 V	1.5	1.7	2	V
V_{T-}	Negative-going threshold voltage	95	V_{CC} = 5 V	0.6	0.9	1.1	V
$V_{T+}-V_{T-}$	Hysteresis	94 & 95	V_{CC} = 5 V	0.4	0.8		V
V_I	Input clamp voltage	97	V_{CC} = MIN, I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage	95	V_{CC} = MIN, V_I = 0.6 V, I_{OH} = −800 μA	2.4	3.3		V
V_{OL}	Low-level output voltage	94	V_{CC} = MIN, V_I = 2 V, I_{OL} = 16 mA		0.22	0.4	V
I_{T+}	Input current at positive-going threshold	94	V_{CC} = 5 V, V_I = V_{T+}		−0.65		mA
I_{T-}	Input current at negative-going threshold	95	V_{CC} = 5 V, V_I = V_{T-}		−0.85		mA
I_I	Input current at maximum input voltage	96	V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	96	V_{CC} = MAX, V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	97	V_{CC} = MAX, V_I = 0.4 V		−1	−1.6	mA
I_{OS}	Short-circuit output current§	98	V_{CC} = MAX	−18		−55	mA
I_{CCH}	Supply current, high-level output	99	V_{CC} = MAX, V_I = 0		14	23	mA
I_{CCL}	Supply current, low-level output	99	V_{CC} = MAX, V_I = 4.5 V		20	32	mA

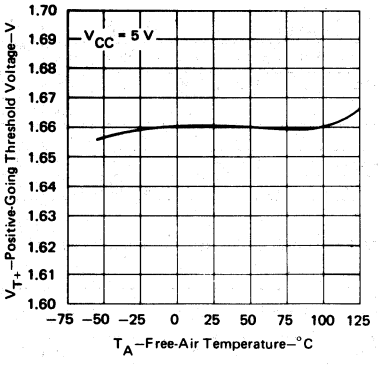
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

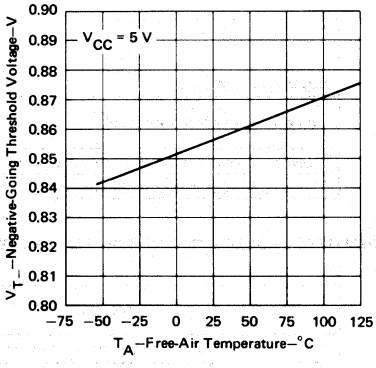
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	100	C_L = 15 pF, R_L = 400 Ω		18	27	ns
t_{PHL}	Propagation delay time, high-to-low-level output	100	C_L = 15 pF, R_L = 400 Ω		15	22	ns

TYPICAL CHARACTERISTICS

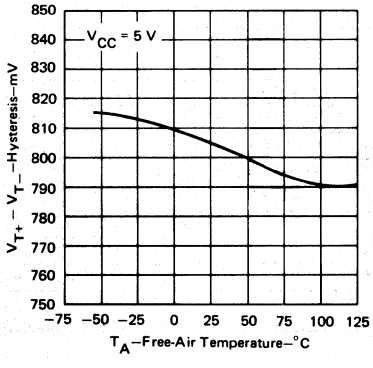
POSITIVE-GOING THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE



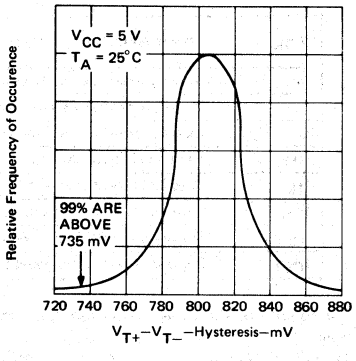
NEGATIVE-GOING THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE



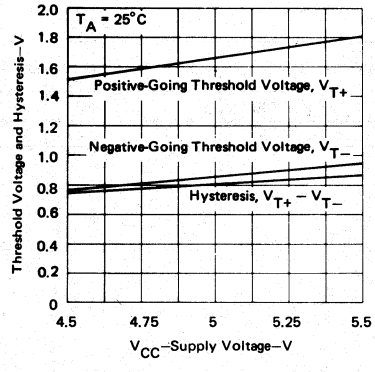
HYSTERESIS
vs
FREE-AIR TEMPERATURE



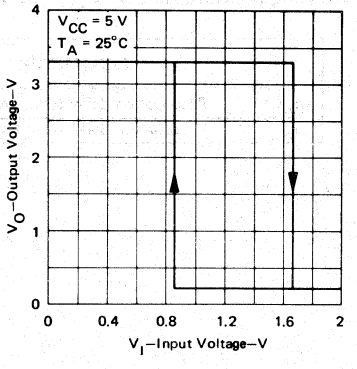
DISTRIBUTION OF UNITS
FOR HYSTERESIS



THRESHOLD VOLTAGES AND HYSTERESIS
vs
SUPPLY VOLTAGE



OUTPUT VOLTAGE
vs
INPUT VOLTAGE



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