The Engineering Staff of
TEXAS INSTRUMENTS INCORPORATED
Semiconductor Group

The Semiconductor Memory Data Book for Design Engineers

TEXAS INSTRUMENTS
INCORPORATED

TI worldwide sales offices

ALABAMA

P.O. Box 2237, 304 Wynn Drive
Huntsville, Alabama 35804
205-837-7530

ARIZONA

4820 N. Black Canyon Hwy.
Suite 202
Phoenix, Arizona 85017
602-248-8028

CALIFORNIA

831 S. Douglass St.
El Segundo, California 90245
213-973-2571

Balboa Towers Bldg., Suite 805
5252 Balboa Avenue
San Diego, California 92117
714-279-2622

1505 East 17th St., Suite 201
Santa Ana, California 92701
714-835-9031

776 Palomar Avenue
Sunnyvale, California 94086
408-732-1840

COLORADO

9725 E. Hampden St., Suite 301
Denver, Colorado 80231
303-751-1780

CONNECTICUT

35 Worth Avenue
Hamden, Connecticut 06518
203-281-0074

FLORIDA

601 W. Oakland Park Blvd.
Fort Lauderdale, Florida 33311
305-566-3294

2221 Lee Road, Suite 108
Winter Park, Florida 32789
305-644-3535

GEORGIA

Route 1, Creekwood Pass
Dallas, Georgia 30132
404-445-4908

ILLINOIS

1701 Lake Avenue, Suite 300
Glenview, Illinois 60025
312-729-5710

INDIANA

3705 Rupp Drive
Arch Bldg.
Fort Wayne, Indiana 46805
219-484-0606

2346 S. Lynhurst Dr., Suite 101
Indianapolis, Indiana 46241
317-248-8555

MASSACHUSETTS

504 Totten Pond Road
Waltham, Mass. 02154
617-890-7400

MICHIGAN

Central Park Plaza
26211 Central Park Blvd., Suite 215
Southfield, Michigan 48076
313-353-0830

MINNESOTA

A.I.C. Bldg., Suite 202
7615 Metro Blvd.
Edina, Minn. 55435
612-835-2900

NEW JERSEY

1245 Westfield Ave.
Clark, New Jersey 07066
201-574-9800

NEW MEXICO

1101 Cardenas Drive, N.E.,
Room 215
Albuquerque, New Mexico 87110
505-265-8491

NEW YORK

144 Metro Pk.
Rochester, New York 14623
716-461-1800

6700 Old Collamer Rd.
East Syracuse, New York 13057
315-463-9291

P.O. Box 618, 112 Nanticoke Ave.
Endicott, New York 13760
607-785-9987

167 Main Street
Fishkill, New York 12524
914-896-6793

2 Huntington Quadrangle, Suite 2N04
Huntington Station, New York 11746
516-293-2560

NORTH CAROLINA

3631 Westfield
High Point, N.C. 27260
919-869-3651

OHIO

28790 Chagrin Blvd., Suite 120
Cleveland, Ohio 44122
216-464-2990

Hawley Bldg., Suite 101
4140 Linden Avenue
Dayton, Ohio 45432
513-253-3121

OREGON

10700 S.W. Beaverton Hwy., Suite 111
Beaverton, Oregon 97005
503-643-1182

PENNSYLVANIA

275 Commerce Drive
Fort Washington, Pa. 19034
215-643-6450

TEXAS

Headquarters — Gen. Offices
Dallas, Texas 75222
214-238-2011

MS366—P.O. Box 5012
Dallas, Texas 75222
214-238-6805

3939 Ann Arbor
Houston, Texas 77042
713-785-6906

VIRGINIA

8512 Trabue Road
Richmond, Virginia 23235
804-320-3830

WASHINGTON

700 112th N.E., Suite 101
Bellevue, Washington 98004
206-455-3480

WASHINGTON, D.C.

1500 Wilson Blvd., Suite 1100
Arlington, Virginia 22209
703-525-0336

ARGENTINA

Texas Instruments Argentina S.A.I.C.F.

C.C. Box 2296—Correo Central
Buenos Aires, Argentina
748-1141

ASIA

Texas Instruments Asia Limited

5F Aoyama Tower Bldg.
24-15 Minami Aoyama Chome
Minato-ku, Tokyo 107, Japan
402-6171

11A-15 Chatham Road
First Floor, Kowloon
Hong Kong
3-670061

Texas Instruments Singapore (PTE) Ltd.
27 Kallang Place
Singapore 1, Rep. of Singapore
258-1122

Texas Instruments Taiwan Limited
P.O. Box 3999
Taipei, Chung Ho, Taiwan
921 623

Texas Instruments Malaysia SDN. BHD.
Number 1 Lorong Enggang 33
Kuala Lampur 15-07, Malaysia
647 911

AUSTRALIA

Texas Instruments Australia Ltd.

Suite 205, 118 Great North Road
Five Dock N.S.W. 2046 Australia
831-2555

Box 63, Post Office
171-175 Philip Highway
Elizabeth 5112 South Australia
255-2066

BRAZIL

Texas Instrumentos Electronicos
do Brasil Ltda.

Rua Joao Annes, 153-Lapa
Caixa Postal 30.103, CEP 01.000
Sao Paulo, SP, Brasil
260-2956

CANADA

Texas Instruments Incorporated

935 Montee De Liesse
St. Laurent H4T 1R2
Quebec, Canada
514-341-3232

5F Caesar Avenue
Ottawa 12
Ontario, Canada
613-825-3716

280 Centre Str. East
Richmond Hill (Toronto)
Ontario, Canada
716-856-4453

DENMARK

Texas Instruments Denmark

46D, Marielundvej
2730 Herlev, Denmark
(01) 91 74 00

FINLAND

Texas Instruments Finland OY

Fredrikinkatu 75, A7
Helsinki 10, Finland
44 71 71

FRANCE

Texas Instruments France

Boite Postale 5
06 Villeneuve-Loubet, France
31 03 64

La Boursidiere, Bloc A
R.N. 186, 92350 Le Plessis Robinson
630.23.43

30-31 Quai Rambaud
69 Lyon, France
42 78 50

GERMANY

Texas Instruments Deutschland GmbH

Haggerty Str. 1
8050 Freising, Germany
08161/80-1

Frankfurter Ring 243
8000 Munich 40, Germany
089/325011-15

Lazarettstrasse, 19
4300 Essen, Germany
02141/20916

Krugerstrasse 24
1000 Berlin 49, Germany
0311/74 44 041

Akazlenstrasse 22-26
6230 Frankfurt-Griesheim
Germany
0611/39 90 61

Steimbker Hof 8A
3000 Hannover, Germany
0511/55 60 41

Krefelderstrasse 11-15
7000 Stuttgart 50, Germany
0711/54 70 01

ITALY

Texas Instruments Italia SpA

Via Della Giustizia 9
20125 Milan, Italy
02-688 31 41

Via L. Mancinella 65
00199 Roma, Italy
06-83 77 45

Via Montebello 27
10124 Torino, Italy
011-83 22 76

MEXICO

Texas Instruments de Mexico S.A.

Poniente 116 #489
Col. Industrial Vallejo
Mexico City, D.F., Mexico
567-92-00

NETHERLANDS

Texas Instruments Holland N.V.

Entrepot Gebouw-Kamer 225
P.O. Box 7603
Schiphol-Centrum
020-17 36 36

NORWAY

Texas Instruments Norway A/S
Sentrumskontorene
Brugaten 1
Oslo 1, Norway
33 18 80

SWEDEN

Texas Instruments Sweden AB

S-104 40 Stockholm 14
Skeppargatan 26
67 98 35

UNITED KINGDOM

Texas Instruments Limited

Manton Lane
Bedford, England
0234-67466

$2.95
(In U.S.A.)

The Semiconductor Memory Data Book

for Design Engineers

First Edition

TEXAS INSTRUMENTS
INCORPORATED

CC-420
43037-65-GI

Printed in U.S.A.

IMPORTANT NOTICES

Texas Instruments reserves the right to make changes at any time in order to improve design and to supply the best product possible.

TI cannot assume any responsibility for any circuits shown or represent that they are free from patent infringement.

Information contained herein supercedes previously published data on these devices from TI.

INTRODUCTION

This book contains detailed specifications for 111 semiconductor memory integrated circuits manufactured and supplied worldwide by Texas Instruments. A continuous upgrading of process and design technology has resulted in a wide spectrum of memory products with information retrieval times from a few nanoseconds to a few microseconds. They cover the basic memory functions of serial storage, random-access mass storage, permanent read-only storage and programmable read-only storage of binary information. These LSI high-technology products include:

- 59 MOS Memory products to provide system economy and large storage capacity from:
  - 11 state-of-the-art high-density single transistor cell 4096-bit RAM's designed specifically for mass storage systems
  - 12 economical industry-standard 1024-bit static RAM's for simplified application in small or medium size systems
  - 24 different shift registers featuring highly efficient organizations for implementing serial and recirculating memories in data communications and display systems
- 43 TTL high-performance memories, 38 with Schottky clamping, including:
  - 256-bit and 1024-bit RAM's featuring modified I^2L cell design and single-level metalization to enhance reliability
  - PROM's featuring Titanium-Tungsten fuse links for fast and reliable programming
  - New high density 20-pin 2048-bit and 4096-bit PROM's for reduced board area and system cost
- 7 ECL ultra-high performance memories including:
  - 5 RAM's with access times from 10 ns to 15 ns typically
  - 1 256-bit PROM using Titanium-Tungsten fuse links with a typical access time of 15 ns

Also included are brief product descriptions of 4 microprocessor products from Texas Instruments, 3 manufactured with MOS technology and the other with Integrated Injection Logic (I^2L), a revolutionary new semiconductor technology. These new microprocessor products are directly compatible with most of the semiconductor memory products included in this book.

An eight-page glossary defines symbols and terms used with memory integrated circuits in accordance with current deliberations by the EIA/JEDEC (Electronic Industries Association) and IEC (International Electrotechnical Commission).

Ordering instructions and mechanical data for the package types available are given at the end of the section for each technology (MOS, TTL, and ECL).

The 38510/MACH IV Procurement Specification is included in its entirety and has been updated to include provisions for memory circuits and for the CMOS technology. A current listing of JAN MIL-M-38510 integrated circuits provideds cross-reference from circuit type number to 38510 slash sheet and from 38510 slash sheet to circuit type number. Also covered are the 4096-bit RAMs processed to level III of the MACH IV specification.

The final section in the book is on IC sockets and interconnection panels. TI produces a complete line of these products, and their inclusion here provides a handy reference for the design engineer.

General Information

1

TABLE OF CONTENTS

1

1

ALPHANUMERIC INDEX

*Extended Temperature Range and Hi-Rel (SMC) versions start on page 101.

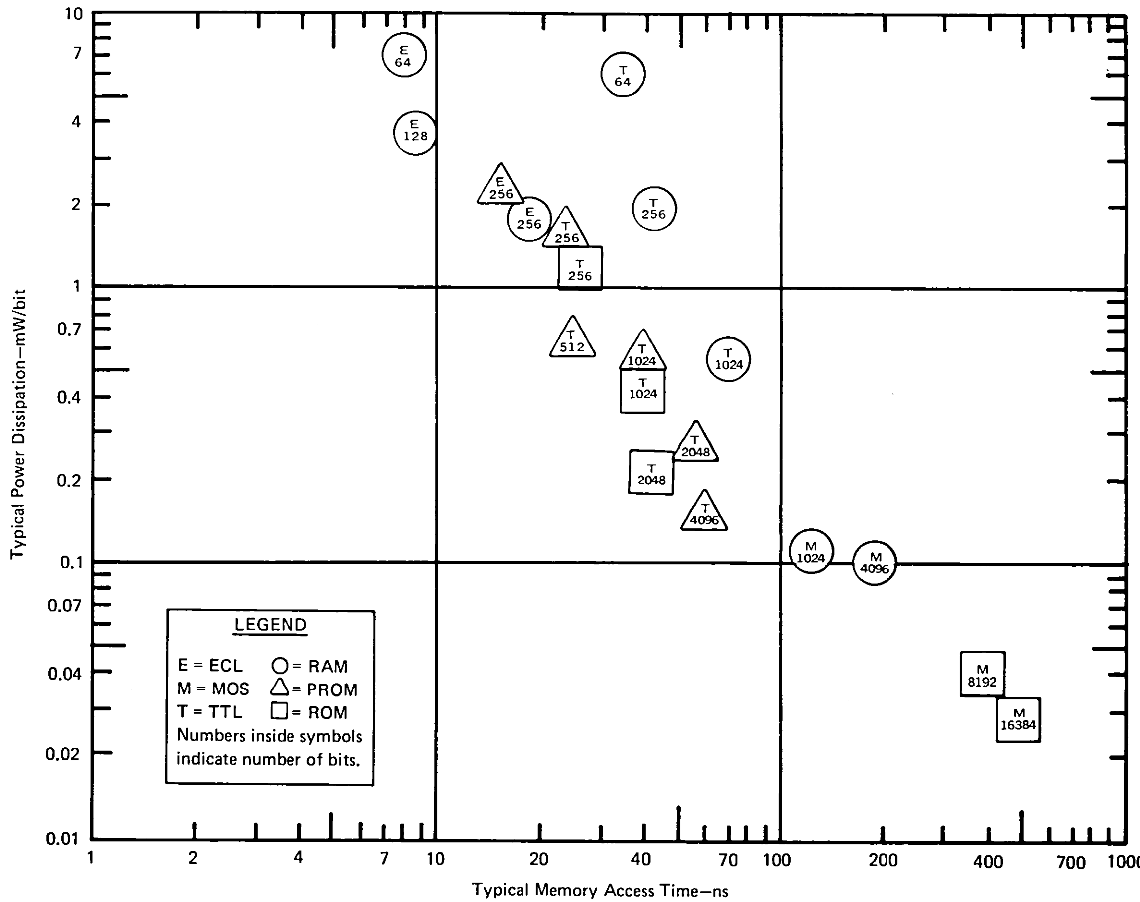
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

WORDS	BITS PER WORD 1	2	4	8
16	16		RAMs SN10145 SN54S189/SN74S189 SN54S289/SN74S289 SN7489	
32	32	64		ROMs SN5488A/SN7488A PROMS SN54188A/SN74188A SN54S188/SN74S188 SN54S288/SN74S288
64	RAMs SN10140 SN10142 SN10148	128		RAMs TMS 4036 PROMs SN54186/SN74186
128	RAMs SN10147	256		
256	RAMs SN10144 SN54S201/SN74S201 SN54S301/SN74S301	512	RAMs TMS 4039, TMS 4042, TMS 4043 ROMs SN54187/SN74187 PROMs SN54S287/SN74S287 SN54S387/SN74S387	ROMs SN54S271/SN74S271 SN54S371/SN74S371 PROMs SN54S470/SN74S470 SN54S471/SN74S471
512		1024	ROMs SN54S270/SN74S270 SN54S370/SN74S370	PROMs SN74S472 SN74S473
1024	RAMs TMS 1103 TMS 4033 TMS 4034 TMS 4035 TMS 4062 TMS 4063 SN74S209 SN74S309	2048		ROMs TMS 4700
2048		4096	8192	ROMs TMS 4800
4096	RAMs TMS 4030 TMS 4050 TMS 4051 TMS 4060		16384 ROMs TMS 4800	32768

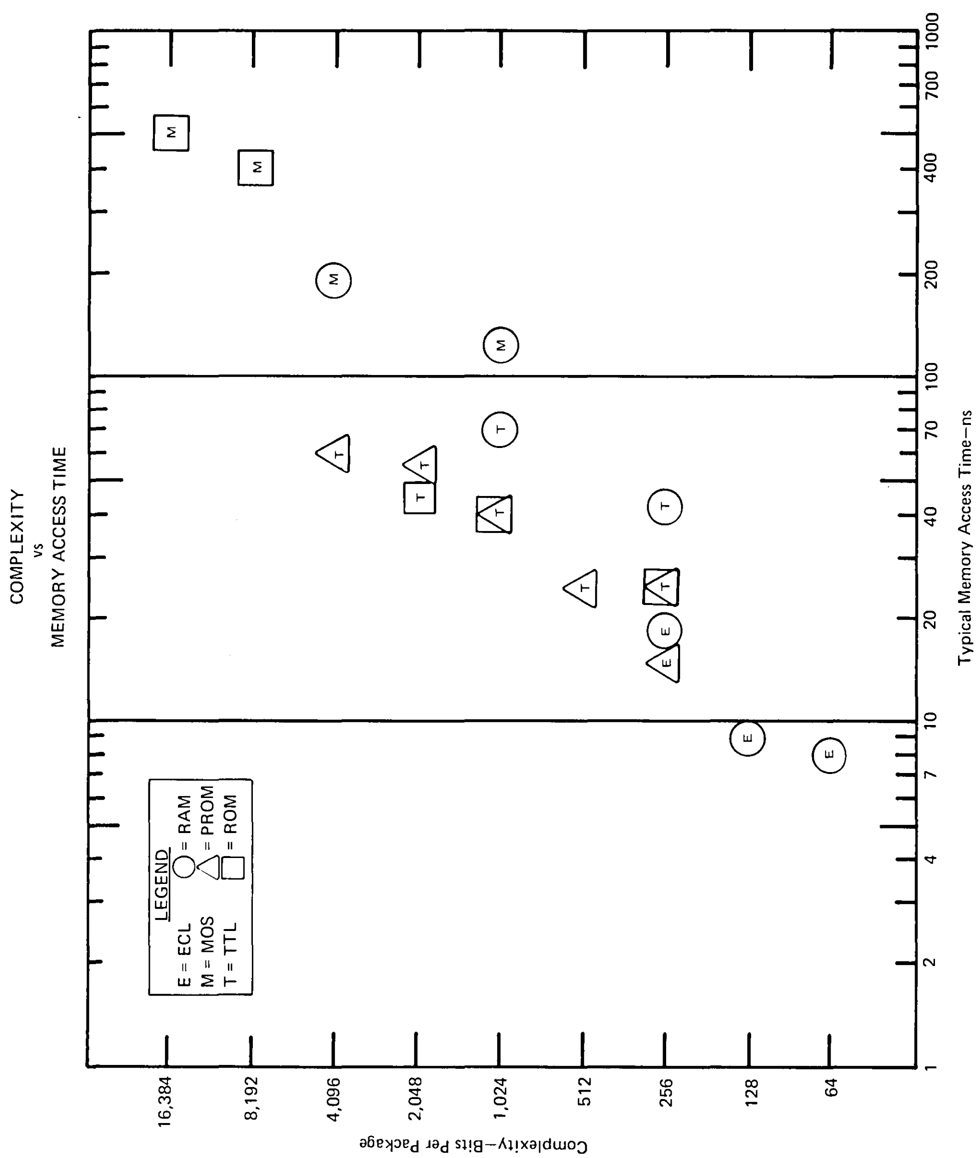
Numbers on shaded lines indicate overall complexity

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

POWER DISSIPATION PER BIT
vs
MEMORY ACCESS TIME



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222


COMPLEXITY
vs
MEMORY ACCESS TIME
LEGEND
E = ECL
M = MOS
T = TTL
= RAM
= PROM
= ROM
Complexity—Bits Per Package
16,384
8,192
4,096
2,048
1,024
512
256
128
64
Typical Memory Access Time—ns
1
2
4
7
10
20
40
70
100
200
400
700
1000

SHIFT REGISTERS
SELECTION GUIDE

1

SHIFT REGISTERS

BITS PER REGISTER	REGISTERS PER PACKAGE				
	1	2	4	6	9
32				TMS 3112 TMS 3122 TMS 3123	
64			TMS 3121 TMS 3417		
80			TMS 3120 TMS 3409		TMS 3135
96		TMS 3126			
100		TMS 3101 TMS 3127			TMS 3137
128		TMS 3114 TMS 3128			TMS 3138
132		TMS 3129			TMS 3139
133		TMS 3113 TMS 3130			TMS 3140
136		TMS 3131			
144		TMS 3132			
512	TMS 3401				
1024	TMS 3133				

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

GLOSSARY
MEMORY INTEGRATED CIRCUIT TERMS AND DEFINITIONS

INTRODUCTION

This glossary consists of three parts: (1) general concepts and types of memories, (2) operating conditions and characteristics (including letter symbols), and (3) graphic symbols and logic conventions. The terms, symbols, abbreviations, and definitions used with memory integrated circuits have not, as yet, been standardized. All are currently under consideration by the EIA/JEDEC (Electronic Industries Association) and the IEC (International Electrotechnical Commission). The following are as consistent with the past and future works of these organizations as is possible to anticipate at this time.

PART I—GENERAL CONCEPTS AND TYPES OF MEMORIES

Chip-Enable Input

A control input to an integrated circuit that, depending on the logic level applied to it, will either permit or prevent operation of the device for input, internal transfer, manipulation, refreshing, and output of data.

NOTES: 1. Retention of data by a static memory is not affected by the logic level of the chip-enable input.
2. See "Chip-Select Input."

Chip-Select Input, Output-Enable Input

A control input to an integrated circuit that, depending on the logic level applied to it, will either permit or prevent the output of data from the device.

NOTES: 1. A chip-select input usually differs from a chip-enable input in that the chip-select input does not necessarily prevent input and internal manipulation of data when it disables the output, while the chip-enable input has that broader function.
2. When disabled by a chip-enable or chip-select signal, the outputs will assume a low level, a high level, or a floating (high-impedance) state, depending on the design of the particular circuit.

Dynamic (Read/Write) Memory

A read/write memory in which the cells require the repetitive application of control signals in order to retain the data stored.

NOTES: 1. The words "read/write" may be omitted from the term when no misunderstanding will result.
2. Such repetitive application of the control signals is normally called a refresh operation.
3. A dynamic memory may use static addressing or sensing circuits.
4. This definition applies whether the control signals are generated inside or outside the integrated circuit.

First-In, First-Out (FIFO) Memory; Digital Storage Buffer

A memory from which data bytes or words can be read in the same order, but not necessarily at the same rate, as that of the data entry.

Last-In, First-Out (LIFO) Memory

A memory from which data bytes or words can be read with the order reversed from that of data entry.

Mask-Programmed Read-Only Memory

A read-only memory in which the data content of each cell is determined during manufacture by the use of a mask, the data content thereafter being unalterable.

Memory Cell

The smallest subdivision of a memory into which data has been or can be entered, in which it is or can be stored, and from which it can be retrieved.

GLOSSARY
MEMORY INTEGRATED CIRCUIT TERMS AND DEFINITIONS

Memory Integrated Circuit

An integrated circuit consisting of memory cells and usually including associated circuits such as those for address selection, amplifiers, etc.

Parallel Access

A feature of a memory by which all the bits of a byte or word are entered simultaneously at several inputs or retrieved simultaneously from several outputs.

1

Programmable Read-Only Memory (PROM)

A read-only memory that after being manufactured can have the data content of each memory cell altered once only.

Random-Access Memory (RAM)

A memory that provides access to any of its address locations in any desired sequence with similar nominal access time for each location.
NOTE: Although this term can be used with either read/write or read-only memories, it is often used by itself in referring to a read/write memory.

Read-Only Memory (ROM)

A memory intended to be read only.
NOTE: Unless otherwise qualified, the term "read-only memory" implies that the content is unalterable and defined by construction.

Read/Write Memory

A memory in which each cell may be selected by applying appropriate electronic input signals and the stored data may be either (a) sensed at appropriate output terminals, or (b) changed in response to other similar electronic input signals.

Reprogrammable Read-Only Memory

A read-only memory that after being manufactured can have the data content of each memory cell altered more than once.

Serial Access

A feature of a memory by which all the bits of a byte or word are entered sequentially at a single input or retrieved sequentially from a single output.

Static (Read/Write) Memory

A read/write memory in which the data is retained in the absence of control signals.
NOTES: 1. The words "read/write" may be omitted from the term when no misunderstanding will result.
2. A static memory may use dynamic addressing or sensing circuits.

Volatile Memory

A memory the data content of which is lost when power is removed.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PART II—OPERATING CONDITIONS AND CHARACTERISTICS (INCLUDING LETTER SYMBOLS)

The symbols for quantities involving time use upper and lower case letters according to the following historically evolved principles:

a. Time itself, is always represented by a lower case t.

b. Subscripts are lower case when one or more letters represent single words, e.g. d for delay, su for setup, rd for read, wr for write.

c. Multiple subscripts are upper case when each letter stands for a different word, e.g. CS for chip select, PLH for propagation delay from low to high, RMW for read, modify write.

1

Access Time

The time between the application of a specified input pulse during a read cycle and the availability of valid data signals at an output.

Example symbology:

$t_{a(ad,LH)}$	Access time from address, low-to-high-level output
$t_{a(ad,HL)}$	Access time from address, high-to-low-level output
$t_{a(CE)}$	Access time from chip enable
$t_{a(CS)}$	Access time from chip select

Current

High-level input current, I_{IH}
The current into* an input when a high-level voltage is applied to that input.

High-level output current, I_{OH}
The current into* an output with input conditions applied that according to the product specification will establish a high level at the output.

Low-level input current, I_{IL}
The current into* an input when a low-level voltage is applied to that input.

Low-level output current, I_{OL}
The current into* an output with input conditions applied that according to the product specification will establish a low level at the output.

Off-state (high-impedance-state) output current (of a three-state output), I_{OZ}
The current into* an output having three-state capability with input conditions applied that according to the product specification will establish the high-impedance state at the output.

Short-circuit output current, I_{OS}
The current into* an output when the output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potential).

Supply current, I_{CC}, I_{DD}, I_{EE}, I_{GG}, I_{SS}
The current into*, respectively, the V_{CC}, V_{DD}, V_{EE}, V_{GG}, or V_{SS} supply terminal of an integrated circuit.

*Current out of a terminal is given as a negative value.

GLOSSARY
MEMORY INTEGRATED CIRCUIT TERMS AND DEFINITIONS

Cycle Time

Read cycle time, $t_{c(rd)}$ (see note)
The time interval between the start of a read cycle and the start of the next cycle.

Read, modify write cycle time, $t_{c(RMW)}$ (see note)
The time interval between the start of a cycle in which the memory is read and new data is entered and the start of the next cycle.

1

Write cycle time, $t_{c(wr)}$ (see note)
The time interval between the start of a write cycle and the start of the next cycle.
NOTE: The read, write, or read, modify write cycle time is the actual interval between two impulses and may be insufficient for the completion of operations within the memory. A minimum value is specified that is the shortest time in which the memory will perform its read and/or write function correctly.

Data Valid Time

Data valid time with respect to chip select, $t_{DV(CS)}$
The interval following chip deselection during which output data continues to be valid.

Data valid time with respect to address, $t_{DV(ad)}$
The interval following an initial change of address during which data stored at the initial address continues to be valid at the output.

Delay Time

The time between the specified reference points on two waveforms.

Example symbology:

$t_{d(\phi1\text{-}\phi2)}$	Delay time, clock 1 to clock 2
$t_{d(PH\text{-}CEH)}$	Delay time, precharge high to chip enable high

Hold Time

Hold time, t_h
The interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.
NOTES: 1. The hold time is the actual time between two events and may be insufficient to accomplish the intended result. A minimum value is specified that is the shortest interval for which correct operation of the logic element is guaranteed.
2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of data and the active transition) for which correct operation of the logic element is guaranteed.

Example symbology:

$t_{h(ad)}$	Address hold time
$t_{h(da)}$	Data hold time
$t_{h(rd)}$	Read hold time
$t_{h(wr)}$	Write hold time
$t_{h(rs)}$	Reset hold time

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

Output Enable and Disable Time

Output enable time (of a three-state output) to high level, t_{PZH} (or low level, t_{PZL})
The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined high (or low) level.

Output enable time (of a three-state output) to high or low level, t_{PZX}
The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to either of the defined active levels (high or low).

Output disable time (of a three-state output) from high level, t_{PHZ} (or low level, t_{PLZ})
The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined high (or low) level to a high-impedance (off) state.

Output disable time (of a three-state output) from high or low level, t_{PXZ}
The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from either of the defined active levels (high or low) to a high-impedance (off) state.

Propagation Time

Propagation delay time, t_{PD}
The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level.

Propagation delay time, low-to-high-level output, t_{PLH}
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.

Propagation delay time, high-to-low-level output, t_{PHL}
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

Pulse Width

Pulse width, t_w
The time interval between specified reference points on the leading and trailing edges of the pulse waveform.

Example symbology:

$t_{w(CEH)}$	Pulse width, chip enable high
$t_{w(CEL)}$	Pulse width, chip enable low
$t_{w(clr)}$	Clear pulse width
$t_{w(CS)}$	Chip-select pulse width
$t_{w(\phi)}$	Clock pulse width
$t_{w(rs)}$	Reset pulse width
$t_{w(wr)}$	Write pulse width

GLOSSARY
MEMORY INTEGRATED CIRCUIT TERMS AND DEFINITIONS

Recovery Time

Sense recovery time, t_{SR}
The time interval needed to switch a memory from a write mode to a read mode and to obtain valid data signals at the output.

Write recovery time
The time interval between the termination of a write pulse and the initiation of a new cycle.

1

Refresh Time

Refresh time, $t_{refresh}$ (see note)
The time interval between successive signals that are intended to restore the level in a dynamic memory cell to its original level.
NOTE: The refresh time is the actual time between two refresh operations and may be insufficient to protect the stored data. A maximum value is specified that is the longest interval for which correct operation is guaranteed.

Setup Time

Setup time, t_{su}
The time interval between the application of a signal that is maintained at a specified input terminal and a consecutive active transition at another specified input terminal.
NOTES: 1. The setup time is the actual time between two events and may be insufficient to accomplish the setup. A minimum value is specified that is the shortest interval for which correct operation of the logic element is guaranteed.
2. The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the logic element is guaranteed.

Example symbology:

$t_{su(ad)}$	Address setup time
$t_{su(da)}$	Data setup time
$t_{su(rd)}$	Read setup time
$t_{su(wr)}$	Write setup time

Transition Time

Transition time, low-to-high-level, t_{TLH}
The time between a specified low-level voltage and a specified high-level voltage on a waveform that is changing from the defined low level to the defined high level.

Transition time, high-to-low-level, t_{THL}
The time between a specified high-level voltage and a specified low-level voltage on a waveform that is changing from the defined high level to the defined low level.

Voltage

High-level input voltage, V_{IH}
An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.
NOTE: A minimum or B-limit value (V_{IHB}, $V_{IH'B}$) is specified that is the least positive (most negative) value of high-level input voltage for which operation of the logic element within specification limits is guaranteed. For ECL circuits, a least-negative-limit value (V_{IHA}) is also specified.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

High-level output voltage, V_{OH}
The voltage at an output terminal with input conditions applied that according to the product specification will establish a high level at the output.

Input clamp voltage, V_{IK}
An input voltage in a region of relatively low differential resistance that serves to limit the input voltage swing.

Low-level input voltage, V_{IL}
An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables.
NOTE: A maximum or A-limit value (V_{ILA} or $V_{IL'A}$) is specified that is the most positive (least negative) value of low-level input voltage for which operation of the logic element within specification limits is guaranteed. For ECL circuits, a most-negative-limit value (V_{ILB}) is also specified.

Low-level output voltage, V_{OL}
The voltage at an output terminal with input conditions applied that according to the product specification will establish a low level at the output.

PART III—GRAPHIC SYMBOLS AND LOGIC CONVENTIONS

All graphic symbols shown in this section are standard in the USA (ANSI and IEEE) and internationally (IEC).

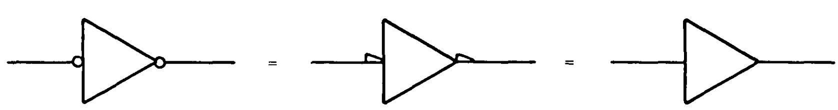
Negation and Polarity Indication, Use of Bars

In this book, the logic negation symbol O and the polarity indicator ⊳ are used interchangeably to indicate:

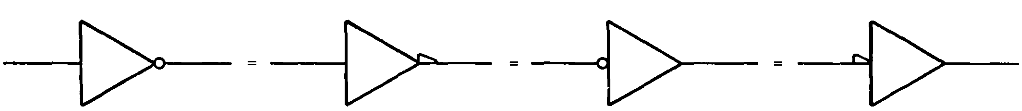
a. A control input (e.g. chip select) that is active when it is at its low logic level.
b. A dynamic input (e.g. clock) that is active on its high-to-low transition.
c. A data input that is out of phase with a data output that is not marked with a negation symbol or polarity indicator.
d. A data output that is out of phase with a data input that is not marked with a negation symbol or polarity indicator.

NOTE: If both data input and output are marked with a negation symbol or polarity indicator, they are in phase with each other. When used with a memory, the terms "in phase," "out of phase," and "inverted" refer to the relationship between the level at the input when a particular data bit is entered and the level at the output when that same bit is retrieved, not to the input and output levels at a given instant.

These three symbols are equivalent and represent a noninverting function:



These four symbols are equivalent and represent an inverting function:



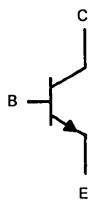
GLOSSARY
MEMORY INTEGRATED CIRCUIT TERMS AND DEFINITIONS

1

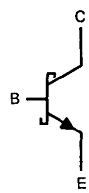
Letter abbreviations that represent inputs or outputs meeting criteria a, b, c, or d above are usually used with a bar.

Examples: $\overline{\text{CS}}$ and $\overline{\text{E}}$ represent chip-select and enable inputs that select and enable when low and do not select and enable when high. $\overline{\text{DO}}$ represents a data output the signal levels of which are inverted (out of phase) with respect to data input DI.

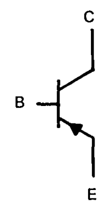
Transistor Graphic Symbols



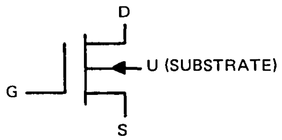
N-P-N BIPOLAR TRANSISTOR



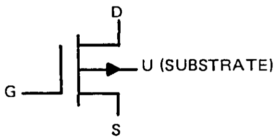
SCHOTTKY-CLAMPED N-P-N BIPOLAR TRANSISTOR



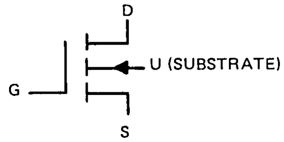
P-N-P BIPOLAR TRANSISTOR



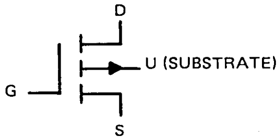
N-CHANNEL MOS DEPLETION-TYPE FIELD-EFFECT TRANSISTOR



P-CHANNEL MOS DEPLETION-TYPE FIELD-EFFECT TRANSISTOR



N-CHANNEL MOS ENHANCEMENT-TYPE FIELD-EFFECT TRANSISTOR



P-CHANNEL MOS ENHANCEMENT-TYPE FIELD-EFFECT TRANSISTOR

Interchangeability Guide

2

INTERCHANGEABILITY GUIDE

Direct replacements were based on similarity of electrical and mechanical characteristics as shown in currently published data. Interchangeability in particular applications is not guaranteed. Before using a device as a substitute, the user should compare the specifications of the substitute device with the specifications of the original.

Texas Instruments makes no warranty as to the information furnished and buyer assumes all risk in the use thereof. No liability is assumed for damages resulting from the use of the information contained in this list.

ECL CIRCUITS
(alphabetically by manufacturers)

ECL package cross-reference:

2

	TI	Fairchild	Motorola	Signetics
Ceramic dual-in-line	J	D	L	F
Ceramic and metal dual-in-line	JE		AL	

FAIRCHILD SEMICONDUCTOR

FSC TYPE	TI DIRECT REPLACEMENT
F10405	SN10147
F10410	SN10144

MOTOROLA

MOTOROLA TYPE	TI DIRECT REPLACEMENT
MMC10140	SN10140
MMC10142	SN10142
MMC10144	SN10144
MMC10145	SN10145
MMC10147	SN10147
MMC10148	SN10148

SIGNETICS

SIGNETICS TYPE	TI DIRECT REPLACEMENT
S10139	SN10139
S10140	SN10140
S10144	SN10144
S10145	SN10145
S10148	SN10148

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

MOS CIRCUITS
(alphabetically by manufacturers)

ADVANCED MICRO DEVICES

AMD TYPE	DESCRIPTION	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGN	DESCRIPTION
AM 1002	2 x 128 SSR		TMS 3128/3138	2 x 128 SSR/9 x 128 SSR
AM 1402A	4 x 256 DSR		TMS 3133	1 x 1024 SSR
AM 1403A	2 x 512 DSR		TMS 3133	1 x 1024 SSR
AM 1404A	1 x 1024 DSR		TMS 3133	1 x 1024 SSR
AM 1406	2 x 100 DSR		TMS 3127/3137	2 x 100/9 x 100 SSR
AM 1407	2 x 100 DSR		TMS 3127/3137	2 x 100/9 x 100 SSR
AM 2505	1 x 512 DSR		TMS 3133	1 x 1024 SSR
AM 2512	1 x 1024 DSR		TMS 3133	1 x 1024 SSR
AM 2521	2 x 128 SSR		TMS 3128/3138	2 x 128 SSR/9 x 128 SSR
AM 2524	1 x 512 DSR		TMS 3133	1 x 1024 SSR
AM 2525	1 x 1024 DSR		TMS 3133	1 x 1024 SSR
AM 2533	1 x 1024 SSR	TMS 3133	TMS 3133	1 x 1024 SSR
AM 2803	2 x 512 DSR		TMS 3133	1 x 1024 SSR
AM 2804	1 x 1024 DSR		TMS 3133	1 x 1024 SSR
AM 2805	1 x 512 DSR		TMS 3133	1 x 1024 SSR
AM 2806	1 x 1024 DSR		TMS 3133	1 x 1024 SSR
AM 2807	1 x 512 DSR		TMS 3133	1 x 1024 SSR
AM 2808	1 x 1024 DSR		TMS 3133	1 x 1024 SSR
AM 2809	2 x 128 SSR		TMS 3128/3138	2 x 128 SSR/9 x 128 SSR
AM 2810	2 x 128 SSR		TMS 3128/3138	2 x 128 SSR/9 x 128 SSR
AM 2814	2 x 128 SSR	TMS 3114	TMS 3128	2 x 128 SSR
AM 2833	1 x 1024 SSR	TMS 3133	TMS 3133	1 x 1024 SSR
AM 2841	64 x 4 FIFO		TMS 4024	64 x 9 FIFO
AM 3114	2 x 128 SSR	TMS 3114	TMS 3128/3138	2 x 128 SSR/9 x 128 SSR
AM 3341	64 x 4 FIFO		TMS 4024	64 x 9 FIFO
AM 4057	1 x 512 SSR		TMS 3133	1 x 1024 SSR
AM 5057	1 x 512 SSR		TMS 3133	1 x 1024 SSR
AM 9102	1 x 1024 SRAM	TMS 4034	TMS 4051	1 x 4096 DRAM
AM 9102A	1 x 1024 SRAM	TMS 4033	TMS 4051	1 x 4096 DRAM

AMERICAN MICROSYSTEMS INCORPORATED

AMI TYPE	DESCRIPTION	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGN	DESCRIPTION
S 1463	2 x 64 SSR		TMS 3121	4 x 64 SSR
S 1670	2 x 100 SSR		TMS 3127/3137	2 x 100/9 x 100 SSR
S 1687	1 x 1024 DSR		TMS 3133	1 x 1024 SSR
S 1701	2 x 512 DSR		TMS 3133	1 x 1024 SSR
S 1709	8 x 13 FIFO		TMS 4024	64 x 9 FIFO
S 2103	1 x 1024 DRAM		TMS 4062/4063	1 x 1024 DRAM
			TMS 4030	1 x 4096 DRAM
S 2146	1 x 1024 DRAM		TMS 4062/4063	1 x 1024 DRAM
			TMS 4030	1 x 4096 DRAM
S 3102	1 x 1024 SRAM	TMS 4035	TMS 4051	1 x 4096 DRAM
S 3102A	1 x 1024 SRAM	TMS 4033	TMS 4051	1 x 4096 DRAM
S 3102B	1 x 1024 SRAM	TMS 4034	TMS 4051	1 x 4096 DRAM
S 3103	1 x 1024 DRAM		TMS 4062/4063	1 x 1024 DRAM
			TMS 4050	1 x 4096 DRAM

AMERICAN MICROSYSTEMS INCORPORATED

AMI TYPE	DESCRIPTION	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGN	DESCRIPTION
S 4006	1 x 1024 DRAM		TMS 4062/4063	1 x 1024 DRAM
			TMS 4050	1 x 4096 DRAM
S 4008	1 x 1024 DRAM		TMS 4062/4063	1 x 1024 DRAM
			TMS 4050	1 x 4096 DRAM

ELECTRONIC ARRAYS

EA TYPE	DESCRIPTION	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGN	DESCRIPTION
EA 1004	2 x 100 SSR		TMS 3127/3137	2 x 100/9 x 100 SSR
EA 1005	2 x 100 SSR		TMS 3127/3137	2 x 100/9 x 100 SSR
EA 1008	2 x 80 SSR		TMS 3120/3135	4 x 80/9 x 80 SSR
EA 1009	2 x 80 SSR		TMS 3120/3135	4 x 80/9 x 80 SSR
EA 1012	2 x 50 SSR		TMS 3002	2 x 50 SSR
EA 1200	4 x 32 DSR		TMS 3122/23	6 x 32 SSR
EA 1201	4 x 32 DSR		TMS 3122/23	6 x 32 SSR
EA 1206	1 x 512 DSR		TMS 3133	1 x 1024 SSR
EA 1212	1 x 512 DSR		TMS 3133	1 x 1024 SSR
EA 1213	4 x 80 DSR		TMS 3120/3135	4 x 80/9 x 80 SSR
EA 1214	4 x 80 DSR		TMS 3120/3135	4 x 80/9 x 80 SSR
EA 2102	1 x 1024 SRAM	TMS 4035	TMS 4035	1 x 1024 SRAM
EA 3501	ASCII GEN		TMS 2501	ASCII GEN
EA 3701	ASCII GEN		TMS 4103	ASCII GEN
EA 4501	ASCII GEN		TMS 2501	ASCII GEN
EA 4800	8 x 2048 ROM	TMS 4800	TMS 4800	8 x 2048 ROM
				4 x 4096 ROM
EA 4900	8 x 2048 ROM	TMS 4800	TMS 4800	8 x 2048 ROM
				4 x 4096 ROM

FAIRCHILD SEMICONDUCTOR

FSC TYPE	DESCRIPTION	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGN	DESCRIPTION
3325	4 x 64 DSR		TMS 3121	4 x 64 DSR
3329	1 x 512 DSR		TMS 3133	1 x 1024 SSR
3341	4 x 64 FIFO		TMS 4024	64 x 9 FIFO
3342	4 x 64 SSR	TMS 3121	TMS 3121	4 x 64 SSR
3343	2 x 128 SSR		TMS 3128/3138	2 x 128 SSR/9 x 128 SSR
3344	2 x 132 SSR		TMS 3129/3138	2 x 132 SSR/9 x 128 SSR
3345	2 x 136 SSR		TMS 3131	8 x 136 SSR
3346	2 x 144 SSR		TMS 3132	8 x 144 SSR
3347	4 x 80 SSR	TMS 3120	TMS 3120/3135	4 x 80/9 x 80 SSR
3348/9	6 x 32 SSR	TMS 3112/22	TMS 3112/22	6 x 32 SSR
3355	1 x 1024 SSR	TMS 3133	TMS 3133	1 x 1024 SSR
3383	1 x 256 DSR		TMS 3417	4 x 64 DSR
3524-5	1 x 1024 DRAM		TMS 4062/63	1 x 1024 DRAM
			TMS 4050	1 x 4096 DRAM

GENERAL INSTRUMENT

GI TYPE	DESCRIPTION	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGN	DESCRIPTION
SL-5-2100	2 x 128 SSR		TMS 3128/3138	2 x 128 SSR/9 x 128 SSR
SL-5-C2100	2 x 100 SSR		TMS 3127/3137	2 x 100/9 x 100 SSR
SL-5-4032	4 x 32 SSR		TMS 3122	6 x 32 SSR
SL-6-2064	2 x 64 SSR		TMS 3121	4 x 64 SSR
SL-9-1512	1 x 512 SSR		TMS 3133	1 x 1024 SSR
SL-9-4080	4 x 80 SSR		TMS 3120/3135	4 x 80 SSR/9 x 80 SSR
DL-9-1402A	4 x 256 DSR		TMS 3133	1 x 1024 SSR
DL-9-1403A	2 x 512 DSR		TMS 3133	1 x 1024 SSR
DL-9-1404A	1 x 1024 DSR		TMS 3133	1 x 1024 SSR
DL-6-2100	2 x 100 DSR		TMS 3127/3137	2 x 100/9 x 100 SSR
DL-6-2128	2 x 128 DSR		TMS 3128/3138	2 x 128 SSR/9 x 128 SSR
RA-9-1103	1 x 1024 DRAM		TMS 4062/63 TMS 4050	1 x 1024 DRAM 1 x 4096 DRAM
AY-5-1012	UART	TMS 6011	TMS 6011	UART

INTEL

INTEL TYPE	DESCRIPTION	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGN	DESCRIPTION
1103	1 x 1024 DRAM	TMS 1103	TMS 4050/4051 TMS4060	1 x 4096 DRAM 1 x 4096 DRAM
1311/12/13	ASCII GEN		TMS 2501	ASCII GEN
C1402A	4 x 256 DSR		TMS 3133	1 x 1024 SSR
C1403A	2 x 512 DSR		TMS 3133	1 x 1024 SSR
C1404A	1 x 1024 DSR		TMS 3133	1 x 1024 SSR
C1405A	1 x 512 DSR		TMS 3133	1 x 1024 SSR
1406/1506	8 x 100 DSR		TMS 3127/3137	2 x 100/9 x 100 SSR
1407/1507	2 x 100 SDR		TMS 3127/3137	2 x 100/9 x 100 SSR
2101	4 x 256 SRAM	TMS 4039	TMS 4039	4 x 256 SRAM
2101-1	4 x 256 SRAM	TMS 4039-2	TMS 4039-2	4 x 256 SRAM
2101-2	4 x 256 SRAM	TMS 4039-1	TMS 4039-1	4 x 256 SRAM
2102-1	1 x 1024 SRAM	TMS 4033	TMS 4033	1 x 1024 SRAM
2102-2	1 x 1024 SRAM	TMS 4034	TMS 4034	1 x 1024 SRAM
2102	1 x 1024 SRAM	TMS 4035	TMS 4035	1 x 1024 SRAM
2111	4 x 256 SRAM	TMS 4042	TMS 4042	4 x 256 SRAM
2111-1	4 x 256 SRAM	TMS 4042-2	TMS 4042-2	4 x 256 SRAM
2111-2	4 x 256 SRAM	TMS 4042-1	TMS 4043-1	4 x 256 SRAM
2112	4 x 256 SRAM	TMS 4043	TMS 4043	4 x 256 SRAM
2112-2	4 x 256 SRAM	TMS 4043-1	TMS 4043-1 TMS 4043-2	4 x 256 SRAM
P2405	1 x 1024 DSR		TMS 3133	1 x 1024 SSR
2107A	1 x 4096 DRAM	TMS 4030/4060	TMS 4030/4060	1 x 4096 DRAM
8308	8 x 1024 ROM	TMS 4700	TMS 4700	8 x 1024 ROM

2

INTERCHANGEABILITY GUIDE

INTERSIL

INTERSIL TYPE	DESCRIPTION	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGN	DESCRIPTION
IM 7552	1 x 1024 SRAM	TMS 4035	TMS 4035/4051	1 x 1024 SRAM
IM 7552-2	1 x 1024 SRAM	TMS 4034	TMS 4034/4051	1 x 1024 SRAM
IM 7552-1	1 x 1024 SRAM	TMS 4033	TMS 4033/4051	1 x 1024 SRAM
IM 7702	4 x 256 DSR		TMS 3133	1 x 1024 SSR
IM 7703	2 x 512 DSR		TMS 3133	1 x 1024 SSR
IM 7704	1 x 1024 DSR		TMS 3133	1 x 1024 SSR
IM 7712	1 x 1024 DSR		TMS 3133	1 x 1024 SSR
IM 7722	1 x 1024 DSR		TMS 3133	1 x 1024 SSR
IM 7780	4 x 80 DSR	TMS 3409	TMS 3120/3135	4 x 80 DSR/SSR/9 x 80 SSR

MOSTEK

MOSTEK TYPE	DESCRIPTION	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGN	DESCRIPTION
1002	2 x 128 SSR		TMS 3128/3138	2 x 128 SSR/9 x 128 SSR
1007	4 x 80 DSR	TMS 3409	TMS 3120/3135	4 x 80 DSR/SSR/9 x 80 SSR
4096	1 x 4096 DRAM		TMS 4050/4060	1 x 4096 DRAM
4102P	1 x 1024-SRAM	TMS 4035	TMS 4051	1 x 1024 SRAM
4102P-1	1 x 1024 SRAM	TMS 4033	TMS 4051	1 x 1024 SRAM

NATIONAL SEMICONDUCTOR

NATIONAL TYPE	DESCRIPTION	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGN	DESCRIPTION
MM 402/3	2 x 50 DSR		TMS 3002	8 x 50 SSR
MM 406/7	2 x 100 DSR		TMS 3127/3137	2 x 100/9 x 100 SSR
MM 1103	1 x 1024 DRAM	TMS 1103	TMS 4050	1 x 1024 DRAM
MM 1402A	4 x 256 DSR		TMS 3133	1 x 1024 SSR
MM 1403A	2 x 512 DSR		TMS 3133	1 x 1024 SSR
MM 1404A	1 x 1024 DSR		TMS 3133	1 x 1024 SSR
MM 2102	1 x 1024 SRAM	TMS 4035	TMS 4035	1 x 1024 SRAM
MM 4006A	2 x 100 DSR		TMS 3127/3137	2 x 100/9 x 100 SSR
MM 4013	1 x 1024 DSR		TMS 3133	1 x 1024 SSR
MM 4016	1 x 512 DSR		TMS 3133	1 x 1024 SSR
MM 4020	4 x 80 DSR		TMS 3120/3135	4 x 80/9 x 80 SSR
MM 4105	4 x 64 DSR		TMS 3121	4 x 64 SSR
MM 4052	2 x 80 SSR		TMS 3120/3135	2 x 80/9 x 80 SSR
MM 4053	8 x 100 SSR		TMS 3127/3137	2 x 100/9 x 100 SSR
MM 4056	2 x 256 SSR		TMS 3133	1 x 1024 SSR
MM 4057	1 x 512 SSR		TMS 3133	1 x 1024 SSR
MM 4060	2 x 128 SSR	TMS 3128	TMS 3128/3138	2 x 128 SSR/9 x 128 SSR
MM 5058	1 x 1024 SSR	TMS 3133	TMS 3133	1 x 1024 SSR
MM 5260	1 x 1024 DRAM		TMS 4062/63 TMS 4050/4060	1 x 1024 DRAM 1 x 4096 DRAM

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

SIGNETICS

SIGNETICS TYPE	DESCRIPTION	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGN	DESCRIPTION
1103	1 x 1024 DRAM	TMS 1103	TMS 4062/63 TMS 4050/4060	1 x 1024 DRAM 1 x 4096 DRAM
2502	4 x 256 DSR		TMS 3133	1 x 1024 SSR
2503	2 x 512 DSR		TMS 3133	1 x 1024 SSR
2504	1 x 1024 DSR		TMS 3133	1 x 1024 SSR
2505	1 x 512 DSR		TMS 3133	1 x 1024 SSR
2506	2 x 100 DSR		TMS 3127/3137	2 x 100/9 x 100 SSR
2507	2 x 100 DSR		TMS 3127/3137	2 x 100/9 x 100 SSR
2510	2 x 100 SSR		TMS 3127/3137	2 x 100/9 x 100 SSR
2512	1 x 1024 DSR		TMS 3133	1 x 1024 SSR
2513	2560 ROM		TMS 2501	2560 ASCII GEN
2517	2 x 100 DSR		TMS 3127/3137	2 x 100/9 x 100 SSR
2518	6 x 32 SSR	TMS 3122	TMS 3122	6 x 32 SSR
2521	2 x 128 SSR	TMS 3128	TMS 3128/3138	2 x 128 SSR/9 x 128 SSR
2522	2 x 132 SSR	TMS 3129	TMS 3129/3139	2 x 132 SSR/9 x 132 SSR
2524	1 x 512 DSR		TMS 3133	1 x 1024 SSR
2525	1 x 1024 DSR		TMS 3133	1 x 1024 SSR
2532	4 x 80 SSR	TMS 3120	TMS 3120/3135	4 x 80/9 x 80 SSR
2533	1 x 1024 SSR	TMS 3133	TMS 3133	1 x 1024 SSR
2535	32 x 8 FIFO		TMS 4024	64 x 9 FIFO
2602	1 x 1024 SRAM	TMS 4035	TMS 4051	1 x 1024 SRAM
2602-1	1 x 1024 SRAM	TMS 4033	TMS 4051	1 x 1024 SRAM

WESTERN DIGITAL

WD TYPE	DESCRIPTION	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGN	DESCRIPTION
TR 1602	UART	TMS 6011	TMS 6011	UART
FR 1502E	40 x 9 FIFO		TMS 4024	64 x 9 FIFO

TTL MEMORIES
(alphabetically by manufacturers)

ADVANCED MICRO DEVICES

Example of AMD order code:

Prefix: AM — Type: 27S03 (Bipolar Memory) — Suffix: D M

Package: D = DIP, P = Molded

Temperature Range: C = 0°C to 70°C, M = –55°C to 125°C

AMD TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS	AMD TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS
2700	SN74S201	SN74S201	27S08M	SN54S188	SN54S188
2701	SN74S301	SN74S301	27S09C	SN74S288	SN74S288
27S02C	SN74S289	SN74S289	27S09M	SN54S288	SN54S288
27S02M	SN54S289	SN54S289	27S10C	SN74S387	SN74S387
27S03C	SN74S189	SN74S189	27S10M	SN54S387	SN54S387
27S03M	SN54S189	SN54S189	27S11C	SN74S287	SN74S287
27S08C	SN74S188	SN74S188	27S11M	SN54S287	SN54S287

FAIRCHILD SEMICONDUCTOR

Example of Fairchild order code:

Prefix: F — Type: 93410 — Suffix: D M

Package: D = Ceramic DIP, P = Plastic DIP

Temperature Range: C = 0°C to 70°C or 75°C, M = –55°C to 125°C

FSC TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS	FSC TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGN
93403	SN74S289	SN74S289	93421C	SN74S201	SN74S201
93406C	SN74187	SN74187	93421M	SN54S201	SN54S201
93410AC	SN74S301	SN74S301	93425AC	SN74S209	SN74S209
93410C	SN74S301	SN74S301	93425C	SN74S209	SN74S209
93410M	SN54S301	SN54S301	93426C	SN74S287	SN74S287
93411C	SN74S201	SN74S201	93426M	SN54S287	SN54S287
93411M	SN54S201	SN54S201	93434	SN7488A	SN74S188
93415AC	SN74S309	SN74S309	93436C	SN74S270	SN74S270
93415C	SN74S309	SN74S309	93436M	SN54S270	SN54S270
93416C	SN74S387	SN74S387	93446C	(SN74S370 ROM)	SN74S472
93417M	SN54S387	SN54S387	93446M	(SN54S370 ROM)	SN54S472

HARRIS SEMICONDUCTOR

Example of Harris order code:

Memory	Prefix	Package	Type	Suffix	Temperature Range
	HM1	1 = DIP 9 = Flat Pack	7620	5	2 = −55°C to 125°C 5 = 0°C to 75°C

HARRIS TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS
H0512-38510	SNJ54186	SNJ54S287/SNJ54S387
HM_7602-2	SN54S188	SN54S188
HM_7602-5	SN74S188	SN74S188
HM_7603-2	SN54S288	SN54S288
HM_7603-5	SN74S288	SN74S288
HM_7610-2	SN54S387	SN54S387
HM_7610-5	SN74S387	SN74S387
HM_7611-2	SN54S287	SN54S287
HM_7611-5	SN74S287	SN74S287
HM_7620-2	(SN54S270 ROM)	SN54S387
HM_7620-5	(SN74S270 ROM)	SN74S387/SN74S473
HM_7621-2	(SN54S370 ROM)	SN54S287
HM_7621-5	(SN74S370 ROM)	SN74S287/SN74S472
HM_7640-2		SN54S287/SN54S471
HM_7640-5		SN74S287/SN74S472
HM_7641-2		SN54S387/SN54S470
HM_7641-5		SN74S387/SN74S473
HM_7642-2		SN54S287/SN54S471
HM_7642-5		SN74S472
HM_7643-2		SN54S387/SN54S470
HM_7643-5		SN74S473
HM_7644-2		SN54S287/SN54S471
HM_7644-5		SN74S472
HPROM0512-2	SN54186	SN54S470/SN54S471
HPROM0512-5	SN74186	SN74S470
HPROM1024-2	SN54S287	SN54S287
HPROM1024-5	SN74S287	SN74S287
HPROM1024A-2	SN54S387	SN54S387
HPROM1024A-5	SN74S387	SN74S387
HRPOM8256-2	SN54S188	SN54S188
HRPOM8256-2	SN54S188	SN74S188

INTEL

Example of Intel order code:

Package	Prefix	Type	Suffix
C = CDIP (Metal lid) D = CDIP P = Plastic DIP	P	3101	(None)

INTEL TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS
3101	SN54S289/SN74S289	SN54S289/SN74S289
3101A	SN54S289/SN74S289	SN54S289/SN74S289
3106	SN54S201/SN74S201	SN54S201/SN74S201
3106A	SN54S201/SN74S201	SN54S201/SN74S201
3107	SN54S301/SN74S301	SN54S301/SN74S301
3107A	SN54S301/SN74S301	SN54S301/SN74S301
3110	SN74S309	SN74S209
3301A	SN54187/SN74187	SN54187/SN74187
3304		SN54S473/SN74S473
3601	SN54S387/SN74S387	SN54S387/SN74S387
3604		SN54S473/SN74S473
3624		SN54S472/SN74S472

INTERCHANGEABILITY GUIDE

INTERSIL

Example of Intersil order code:

Prefix
IM — Memory

Type
5601
Bipolar
5 = RAM
6 = ROM

Suffix
C D E
16 Pins
Package
D = Ceramic DIP
P = Plastic DIP
Temperature Range
C = 0°C to 75°C
M = –55°C to 125°C

INTERSIL TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS
IM5501C	SN74S289	SN74S289
IM5501M	SN54S289	SN54S289
IM5503AC	SN74S301	SN74S301
IM5503AM	SN54S301	SN54S301
IM5503C	SN74S301	SN74S301
IM5503M	SN54S301	SN54S301
IM5523AC	SN74S201	SN74S201
IM5523AM	SN54S201	SN54S201
IM5523C	SN74S201	SN74S201
IM5523M	SN54S201	SN54S201
IM5533AC	SN74S301	SN74S301
IM5533AM	SN54S301	SN54S301
IM5533C	SN74S301	SN74S301
IM5533M	SN54S301	SN54S301

INTERSIL TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS
IM5600C	SN74S188	SN74S188
IM5600CF	SN74S188	SN74S188
IM5600M	SN54S188	SN54S188
IM5603AC	SN74S387	SN74S387
IM5603AM	SN54S387	SN54S387
IM5604C	(SN74S270 ROM)	SN74S470
IM5604M	(SN54S270 ROM)	SN54S470
IM5610C	SN74S288	SN74S288
IM5610F	SN74S288	SN74S288
IM5610M	SN54S288	SN54S288
IM5623C	SN74S287	SN74S287
IM5623M	SN54S287	SN54S287
IM5624C	(SN74S370 ROM)	SN74S471
IM5624	(SN54S370 ROM)	SN54S471

MONOLITHIC MEMORIES, INC.

Prefix
H 5 2
Performance
A = AND Enable
H = High Speed
Function
2 = ROM
3 = PROM
5 = RAM
Temperature Range
5 = –55°C to 125°C
6 = 0°C to 70°C

Type
40

Suffix
D
Package
D = CDIP
N = EPOXY

MMI TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS
A5200		SN54S473
A5241		SN54S472
A6240		SN74S473
A6241		SN74S472
H5200	SN54187	SN54187
H5201	(SN54S287 PROM)	SN54S370
H5240		SN54S473
H5241		SN54S472
H6201	(SN74S287 PROM)	SN74S370
H6240		SN74S473
H6241		SN74S472
5200	SN54187	SN54187
5201	(SN54S387 PROM)	SN54S270
5205	SN54S270	SN54S270

MMI TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS
5206	SN54S370	SN54S370
5210		SN54S470
5225		SN54S470
5230	SN5488A	SN5488A
5231	(SN54S188 PROM)	SN54S371
5235		SN54S470
5300	SN54S387	SN54S387
5301	SN54S287	SN54S287
5305	(SN54S270 ROM)	SN54S470
5306	(SN54S370 ROM)	SN54S471
5330	SN54S188	SN54S188
5331	SN54S288	SN54S288
5335		SN54S470
5340		SN54S473

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

MONOLITHIC MEMORIES, INC. (continued)

MMI TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS	MMI TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS
5530	SN54S301	SN54S301	6235		SN74S470
5531	SN54S201	SN54S201	6300	SN74S387	SN74S387
5560	SN54S289	SN54S289	6301	SN74S287	SN74S287
5561	SN54S189	SN54S189	6305	(SN74S270 ROM)	SN74S470
6200	SN74187	SN74187	6306	(SN74S370 ROM)	SN74S471
6201	(SN74S387 PROM)	SN74S270	6330	SN74S188	SN74S188
6205	SN74S270	SN74S270	6331	SN74S288	SN74S288
6206	SN74S370	SN74S370	6335		SN74S470
6210		SN74S470	6340		SN74S473
6225		SN74S473	6530	SN74S301	SN74S301
6230	SN7488A	SN7488A	6531	SN74S201	SN74S201
6231	(SN74S188 PROM)	SN74S371	6560	SN74S289	SN74S289
			6561	SN74S189	SN74S189

2

NATIONAL SEMICONDUCTOR

Prefix	Type	Suffix
DM	7599	N
Digital Monolithic	Temperature Range	Package
	7 = –55°C to 125°C	D = Glass/Metal DIP
	8 = 0°C to 70°C	F = Flat Package
		N = Molded DIP

NSC TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS	NSC TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS
DM7573	SN54S387	SN54S387	DM8574	SN74S287	SN74S287
DM7574	SN54S287	SN54S287	DM8577	SN74S188	SN74S188
DM7577	SN54S188	SN54S188	DM8578	SN74S288	SN74S288
DM7578	SN54S288	SN54S288	DM8582	SN74S301	SN74S301
DM7595		SN54S473	DM8595		SN74S473
DM7596		SN54S472	DM8596		SN74S472
DM7597	SN54S370	SN54S370	DM8597	SN74S370	SN74S370
DM7598		SN54S471	DM8598		SN74S471
DM7599	SN54S189	SN54S189	DM8599	SN74S189	SN74S189
DM7795		SN54S473	DM85S99	SN74S189	SN74S189
DM7796		SN54S472	DM8795		SN74S473
DM8573	SN74S387	SN74S387	DM8796		SN74S472

INTERCHANGEABILITY GUIDE

SIGNETICS

Example of Signetics order code:

Prefix	Type	Suffix
N	8204	B

Temperature Range
N = 0°C to 75°C
S = −55°C to 125°C

Package
B = 16-Pin Plastic DIP
F = Ceramic DIP
N = 24-Pin Plastic DIP
Q = Ceramic Flat Pack

SIGNETICS TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS	SIGNETICS TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS
N8204		SN74S471	N82S130		SN74S473
N8205		SN74S472	N82S131		SN74S472
N82S06	SN74S201	SN74S201	N82S226	SN74187	SN74187
N82S07	SN74S301	SN74S301	N82S229	(SN74S287 PROM)	SN74S370
N82S08	SN74S309	SN74S309	N82S230	SN74S270	SN74S270
N82S10	SN74S309	SN74S309	N82S231	SN74S370	SN74S370
N82S11	SN74S209	SN74S209	S82S07	SN54S301	SN54S301
N82S16	SN74S201	SN74S201	S82S16	SN54S201	SN54S201
N82S17	SN74S301	SN74S301	S82S17	SN54S301	SN54S301
N8223	SN74S188	SN74S188	S82S23	SN54S188	SN54S188
N82S23	SN74S188	SN74S188	S82S25	SN54S301	SN54S301
N8225	SN74S189	SN74S189	S82S114		SN54S471
N82S25	SN74S301	SN74S301	S82S115		SN54S472
N82S110	SN74S309	SN74S309	S82S123	SN54S288	SN54S288
N82S111	SN74S209	SN74S209	S82S126	SN54S387	SN54S387
N82S114		SN74S471	S82S129	SN54S287	SN54S287
N82S115		SN74S472	S82S130		SN54S473
N82S116	SN74S201	SN74S201	S82S131		SN54S472
N82S117	SN74S301	SN74S301	S82S226	SN54187	SN54187
N82S123	SN74S288	SN74S288	S82S229	(SN54S287 PROM)	SN54S370
N82S126	SN74S387	SN74S387	S82S230	SN54S270	SN54S270
N82S129	SN74S287	SN74S287	S72S231	SN54S370	SN54S370

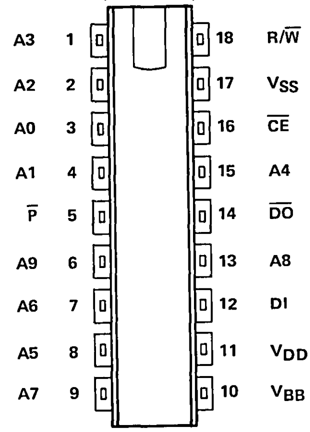
MOS Memories

TMS 1103 JL, NL; TMS 1103-1 JL, NL
1024-BIT DYNAMIC RANDOM-ACCESS MEMORIES

BULLETIN NO. DL-S 7512234, JANUARY 1975

- 1024 x 1-Bit Organization
- Low Power Dissipation
- Input Interface
  - Fully Decoded, On-Chip Address Decode
  - Static Charge Protection
- Output Interface
  - OR-Tie Capability
- Address Access Time
  - TMS 1103 JL, NL . . . 300 ns
  - TMS 1103-1 JL, NL . . . 150 ns
- P-Channel Silicon-Gate Technology
- 18-Pin 300-Mil Dual-In-Line Packages

18-PIN CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGES
(TOP VIEW)



description

The TMS 1103 JL, NL and TMS 1103-1 JL, NL are monolithic random-access memory devices organized as 1024 one-bit words. Outputs may be OR-tied for simple memory expansion since a particular device can be activated by a chip-enable signal. Stored information is read nondestructively and all cells in any row are refreshed by addressing that row at least once every 2-milliseconds for the TMS 1103, 1-millisecond for the TMS 1103-1. These RAMs are fabricated with P-channel silicon-gate enhancement-type technology. Two power supplies and three control clock signals are required with address inputs decoded on the chip. The TMS 1103-1 is a faster-access version of the TMS 1103 with improved cycle times. The TMS 1103 and TMS 1103-1 are offered in both 18-pin ceramic (JL suffix) and plastic (NL suffix) dual-in-line packages.

operation

addresses (A0-A9)

Address terminals are used to activate a particular cell in a 32 x 32 array. Each row address (A0—A4) and each column address (A5—A9) of 5 bits uniquely specify a 10-bit address for a single memory cell. All address signals must be stable during transitions of the chip-enable, read/write, or data-in control signals.

chip enable ($\overline{CE}$)

The chip-enable terminal enables one particular device of an array whose outputs are connected to a common data bus. Chip enable must be low during any read or write interval to allow data to enter or exit.

precharge ($\overline{P}$)

The precharge terminal must be low at the start of any read or write cycle and remain low for a specified time interval after chip enable drops to a low. This overlap interval must be maintained between a specified minimum and maximum time in order to maintain the integrity of stored data.

read/write (R/$\overline{W}$)

The read/write input terminal gates data out of or into the addressed memory cell. Read/write is low when data is written and high during a read interval.

data in (DI)

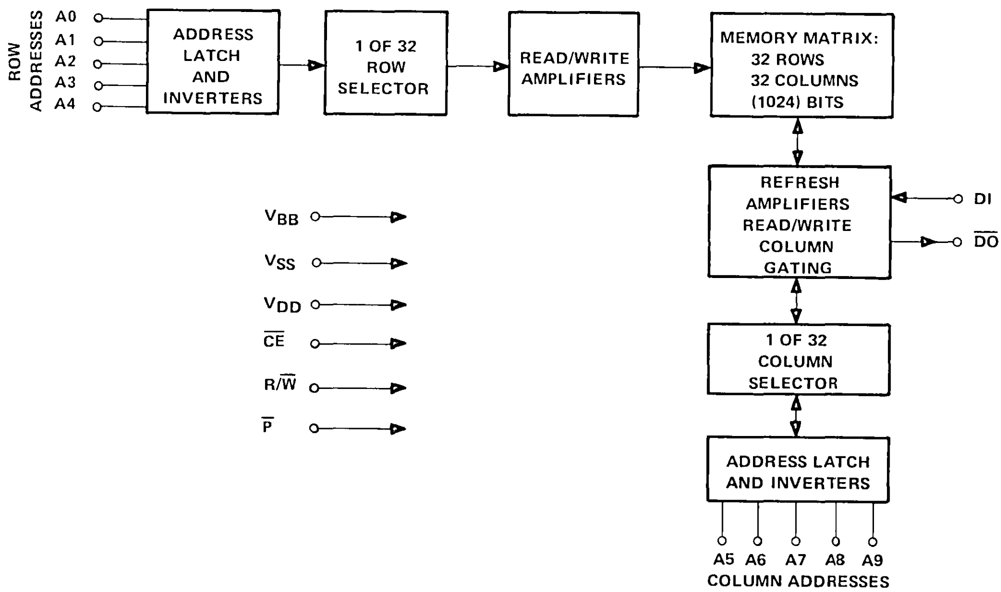
The data-in terminal connects the incoming data bus to the addressed cell for a write operation.

data out ($\overline{DO}$)

Stored data appears at the data-out terminal as the complement of the data-in logic level. Information on the data-out terminal is sensed just prior to the rise of chip enable in a read-only cycle and prior to the fall of read/write in a read, modify write cycle.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1)	−25 to 0.3 V
Supply voltage, V_{SS} (see Note 1)	−25 to 0.3 V
Input voltage (any input)	−25 to 0.3 V
Continuous power dissipation	1 W
Operating free-air temperature range: TMS 1103	0°C to 70°C
TMS 1103-1	0°C to 55°C
Storage temperature range	−65°C to 150°C

NOTE 1: Under absolute maximum ratings, voltage values are with respect to the most-positive supply voltage, V_{BB} (substrate). Throughout the remainder of this data sheet, voltage values are with respect to V_{DD}.

recommended operating conditions

PARAMETER	TMS 1103			TMS 1103-1			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		0			0		V
Supply voltage, V_{SS}	15.2	16	16.8	18	19	20	V
Supply voltage, $V_{BB}-V_{SS}$ (see Note 2)	3		4	3		4	V
Operating free-air temperature, T_A	0		70	0		55	°C

NOTE 2. $V_{BB}-V_{SS}$ supply should be applied at the same time as or before V_{SS}.

electrical characteristics at specified free-air temperatures
V_{SS} = 16.8 V, (V_{BB}–V_{SS}) = 3 V, V_{DD} = 0 V (TMS 1103 JL, NL)
V_{SS} = 20 V, (V_{BB}–V_{SS}) = 3 V, V_{DD} = 0 V (TMS 1103-1 JL, NL)

PARAMETER		TEST CONDITIONS†		TMS 1103 MIN	TMS 1103 TYP‡	TMS 1103 MAX	TMS 1103-1 MIN	TMS 1103-1 TYP‡	TMS 1103-1 MAX	UNIT
V_{IH}	High-level input voltage	T_A = MIN		V_{SS} −1		V_{SS} +1	V_{SS} −1		V_{SS} +1	V
		T_A = MAX		V_{SS} −0.7		V_{SS} +1	V_{SS} −1		V_{SS} +1	
V_{IL}	Low-level input voltage (all addresses and data-in lines)	T_A = MIN		V_{SS} −17		V_{SS} −14.2	V_{SS} −20		V_{SS} −18	V
		T_A = MAX		V_{SS} −17		V_{SS} −14.5	V_{SS} −20		V_{SS} −18	
V_{IL}	Low-level input voltage (precharge, chip-enable, and read/write inputs) (see Note 3)	T_A = MIN		V_{SS} −17		V_{SS} −14.7	V_{SS} −20		V_{SS} −18	V
		T_A = MAX		V_{SS} −17		V_{SS} −15	V_{SS} −20		V_{SS} −18	
V_{OH}	High-level output voltage	R_L = 100 Ω,	T_A = 25°C	60	90	500	115	130	900	mV
		R_L = 100 Ω,	T_A = MAX	50	80	500	90	115	900	
I_I	Input current	V_I = 0 V,	T_A = MIN to MAX			1			10	μA
I_{OH}	High-level output current	R_L = 100 Ω,	T_A = 25°C	600	900	5000	1150	1130	9000	μA
		R_L = 100 Ω,	T_A = MAX	500	800	5000	900	1150	9000	
$I_{O(off)}$	Off-state output current	V_O = 0 V,	T_A = MIN to MAX			1			10	μA
I_{BB}	Supply current from V_{BB}	T_A = MIN to MAX				100			100	μA
$I_{DD(1)}$	Supply current from V_{DD} during precharge pulse width	All addresses = 0 V, $\overline{CE}$ at V_{SS}, V_I = V_{SS}, Precharge = 0 V,	T_A = 25°C		37	56		45	60	mA
$I_{DD(2)}$	Supply current from V_{DD} during precharge and chip-enable overlap	All addresses = 0 V, $\overline{CE}$ at 0 V, V_I = V_{SS}, Precharge = 0 V,	T_A = 25°C		38	59		50	68	mA
$I_{DD(3)}$	Supply current from V_{DD} during precharge to end of chip enable	Precharge = V_{SS}, $\overline{CE}$ at 0 V, V_I = V_{SS}, T_A = 25°C			5.5	11		8.5	11	μA
$I_{DD(4)}$	Supply current from V_{DD} during chip enable to precharge delay	Precharge = V_{SS}, $\overline{CE}$ at V_{SS}, V_I = V_{SS}, T_A = 25°C			3	4		3	4	mA
$I_{DD(av)}$	Average supply current from V_{DD} — TMS 1103	$t_{w(\overline{P})}$ = 190 ns, T_A = 25°C	t_c = 580 ns,		17	25		20	23	mA
	Average supply current from V_{DD} — TMS 1103-1	$t_{w(\overline{P})}$ = 105 ns, T_A = 25°C	t_c = 340 ns							

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at T_A = 25°C.

NOTE 3. The maximum values for V_{IL} for precharge, chip-enable, and read/write of the TMS 1103 may be increased to V_{SS} − 14.2 V at 0°C and V_{SS} − 14.5 V at 70°C (same values as those specified for the address and data-in lines) with a 40-ns degradation (worst case) in $t_{su(ad\text{-}\overline{CE})}$, $t_{d(\overline{PL}\text{-}\overline{CEL})}$, $t_{c(rd)}$, $t_{c(RW)}$, $t_{a(ad)}$, and $t_{a(\overline{P})}$.

dynamic electrical characteristics over operating free-air temperature range (unless otherwise noted)

T_A = 0°C to 70°C, V_{SS} = 16 V ± 5%, ($V_{BB} - V_{SS}$) = 3 V to 4 V, V_{DD} = 0 V (TMS 1103 JL, NL)
T_A = 0°C to 55°C, V_{SS} = 19 V ± 5%, ($V_{BB} - V_{SS}$) = 3 V to 4 V, V_{DD} = 0 V (TMS 1103-1 JL, NL)

capacitance at 25°C free-air temperature

CHARACTERISTICS		TEST CONDITIONS†	PLASTIC PKG		CERAMIC PKG		UNIT
			TYP	MAX	TYP	MAX	
$C_{i(ad)}$	Address input capacitance	$V_I = V_{SS}$	5	7	10	12	pF
$C_{i(\overline{P})}$	Precharge input capacitance	$V_I = V_{SS}$	15	18	16.5	19.5	pF
$C_{i(\overline{CE})}$	Chip-enable input capacitance	$V_I = V_{SS}$	15	18	18	21	pF
$C_{i(R/\overline{W})}$	Read/write input capacitance	$V_I = V_{SS}$	11	15	15.5	19.5	pF
$C_{i(da)}$	Data input capacitance	$\overline{CE}$ at 0 V, $V_I = V_{SS}$	4	5	6.5	7.5	pF
		$\overline{CE}$ at V_{SS}, $V_I = V_{SS}$	2	4	5.6	6.5	
C_o	Data output capacitance	V_O = 0 V	2	3	6	7	pF

†f = 1 MHz, and all unused pins are at ac ground.

read, write, and read, modify write cycle

PARAMETER		TEST CONDITIONS	TMS 1103		TMS 1103-1		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(rfsh)}$	Refresh cycle time	$t_r = t_f$ = 20 ns, C_L = 100 pF (1103), C_L = 50 pF (1103-1), R_L = 100 Ω, V_{ref} = 40 mV (1103), V_{ref} = 80 mV (1103-1)		2		1	ms
$t_{su(ad-\overline{CE})}$	Address-to-chip-enable setup time		115		30		ns
$t_{h(\overline{CE}-ad)}$	Chip-enable-to-address hold time		20		10		ns
$t_{d(\overline{P}L-\overline{CE}L)}$	Precharge low to chip-enable low delay time		125		60		ns
$t_{d(\overline{CE}H-\overline{P}L)}$	Chip-enable high to precharge low delay time		85		40		ns
$t_{d(\overline{CE}L-\overline{P}H)1}$	Chip-enable low to precharge high delay time between low reference points		25	75	5	30	ns
$t_{d(\overline{CE}L-\overline{P}H)2}$	Chip-enable low to precharge high delay time between high reference points			140		85	ns

read cycle

PARAMETER		TEST CONDITIONS	TMS 1103		TMS 1103-1		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time	$t_r = t_f$ = 20 ns,	480		300		ns
$t_{d(\overline{P}H-\overline{CE}H)}$	Precharge high to chip-enable high delay time	C_L = 100 pF (1103),	165	500	115	500	ns
$t_{p(\overline{P}H)}$	Precharge high to output propagation delay time	C_L = 50 pF (1103-1), R_L = 100 Ω,		120		75	ns
$t_{a(ad)}$	Access time from address (see Note 4)	V_{ref} = 40 mV (1103),	300		150		ns
$t_{a(\overline{P})}$	Access time from precharge (see Note 5)	V_{ref} = 80 mV (1103-1)	310		180		ns

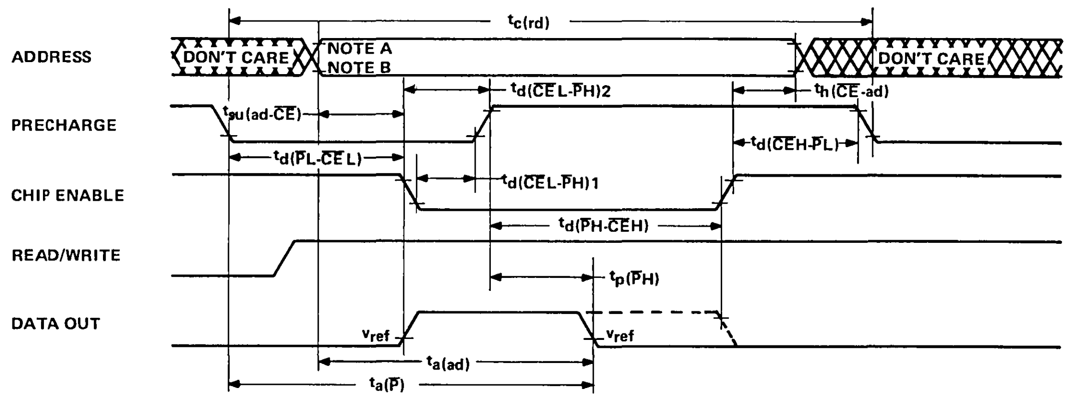
NOTES:

4. $t_{a(ad)} = t_{su(ad-\overline{CE})} + t_{f(\overline{CE})} + t_{d(\overline{CE}L-\overline{P}H)1} + t_{r(\overline{P})} + t_{p(\overline{P}H)}$.
5. $t_{a(\overline{P})} = t_{d(\overline{P}L-\overline{CE}L)} + t_{f(\overline{CE})} + t_{d(\overline{CE}L-\overline{P}H)1} + t_{r(\overline{P})} + t_{p(\overline{P}H)}$.

write or read, modify write cycle

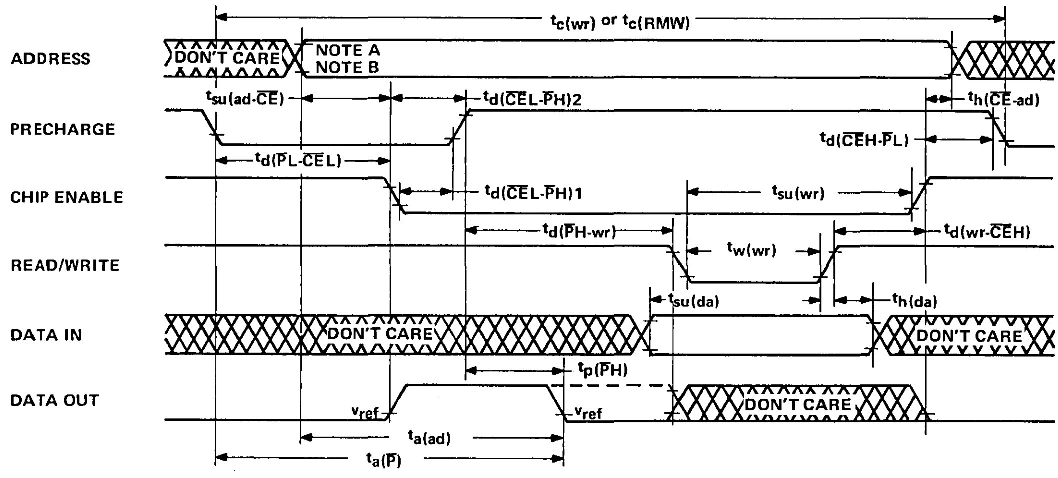
PARAMETER		TEST CONDITIONS	TMS 1103		TMS 1103-1		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(wr)}$	Write cycle time	$t_r = t_f$ = 20 ns, C_L = 100 pF (1103), C_L = 50 pF (1103-1), R_L = 100 Ω, V_{ref} = 40 mV (1103), V_{ref} = 80 mV (1103-1)	580		340		ns
$t_{c(RMW)}$	Read, modify write cycle time		580		340		ns
$t_{d(\overline{P}H-wr)}$	Precharge high to write delay time		165	500	115	500	ns
$t_{w(wr)}$	Write pulse width		50		20		ns
$t_{su(wr)}$	Write setup time		80		20		ns
$t_{su(da)}$	Data setup time		105		40		ns
$t_{h(da)}$	Data hold time		10		10		ns
$t_{p(\overline{P}H)}$	Precharge high to output propagation delay time			120		75	ns
$t_{d(wr-\overline{CE}H)}$	Write to chip-enable high delay time		0		0		ns

PARAMETER MEASUREMENT INFORMATION



NOTES:
A. The high-level time reference on each waveform except data out is V_{SS} −2 V.
B. The low-level time reference on each waveform except data out is V_{DD} +2 V.

FIGURE 1—READ CYCLE



NOTES:
A. The high-level time reference on each waveform except data out is V_{SS} −2 V.
B. The low-level time reference on each waveform except data out is V_{DD} +2 V.

FIGURE 2 – WRITE OR READ, MODIFY WRITE CYCLE

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

MOS LSI

TMS 4030 JL, NL; TMS 4030-1 JL, NL; TMS 4030-2 JL, NL
4096-BIT DYNAMIC RANDOM-ACCESS MEMORIES

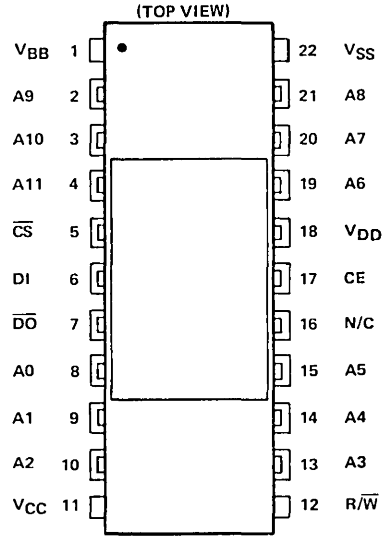
BULLETIN NO. DL-S 7512240, FEBRUARY 1975

- 4096 x 1 Organization
- 3 Performance Ranges:

	ACCESS TIME (MAX)	READ OR WRITE CYCLE (MIN)	READ, MODIFY WRITE CYCLE (MIN)
TMS 4030	300 ns	470 ns	710 ns
TMS 4030-1	250 ns	430 ns	640 ns
TMS 4030-2	200 ns	400 ns	580 ns

- Full TTL Compatibility on All Inputs (No Pull-up Resistors Needed)
- Low Power Dissipation
  - 400 mW Operating (Typical)
  - 0.2 mW Standby (Typical)
- Single Low-Capacitance Clock
- N-Channel Silicon-Gate Technology
- 22-Pin 400-Mil Dual-in-Line Package

22-PIN CERAMIC AND PLASTIC DUAL-IN-LINE PACKAGES (TOP VIEW)



3

description

The TMS 4030 series is composed of high-speed dynamic 4096-bit MOS random-access memories, organized as 4096 one-bit words. N-channel silicon-gate technology is employed to optimize the speed/power/density trade-off. Three performance options are offered: 300 ns access for the TMS 4030, 250 ns access for the TMS 4030-1, and 200 ns for TMS 4030-2. These options allow the system designer to more closely match the memory performance to the capability of the arithmetic processor.

All inputs except the chip enable are fully TTL-compatible and require no pull-up resistors. The low capacitance of the address and control inputs precludes the need for specialized drivers. When driven by a Series 74 device, the guaranteed dc input noise immunity is 200 mV. The TTL-compatible buffer is guaranteed to drive two Series 74 TTL gates. The TMS 4030 series uses only one clock (chip enable) to simplify system design. The low-capacitance chip-enable input requires a positive voltage swing (12 volts), which can be driven by a variety of widely available drivers.

The typical power dissipation of these RAM's is 400 mW active and 0.2 mW standby. To retain data only 6 mW average power is required, which includes the power consumed to refresh the contents of the memory.

The TMS 4030 series is offered in both 22-pin ceramic (JL suffix) and plastic (NL suffix) dual-in-line packages. The series is guarantted for operation from 0°C to 70°C. These packages are designed for insertion in mounting-hole rows on 0.400-mil centers.

operation

chip select ($\overline{CS}$)

The chip-select terminal, which can be driven from standard TTL circuits without an external pull-up resistor, affects the data-in, data-out and read/write inputs. The data input and data output terminals are enabled when chip select is low. Therefore, the read, write, and read, modify write operations are performed only when chip select is low. If the chip is to be selected for a given cycle, the chip-select input must be low on or before the rising edge of the chip enable. If the chip is not to be selected for a given cycle, chip select must be held high as long as chip enable is high. A register for the chip-select input is provided on the chip to reduce overhead and simplify system design.

chip enable (CE)

A single external clock input is required. All read, write, and read, modify write operations take place when the chip enable input is high. When the chip enable is low, the memory is in the low-power standby mode. No read/write operations can take place because the chip is automatically precharging.

PRELIMINARY DATA SHEET: Supplementary data may be published at a later date.

operation (continued)

mode select (R/$\overline{W}$)

The read or write mode is selected through the read/write (R/$\overline{W}$) input. A logic high on the R/$\overline{W}$ input selects the read mode and a logic low selects the write mode. The read/write terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected.

address (A0–A11)

All addresses must be stable on or before the rising edge of the chip-enable pulse. All address inputs can be driven from standard TTL circuits without pull-up resistors. Address registers are provided on chip to reduce overhead and simplify system design.

data-in (DI)

Data is written during a write or read, modify write cycle while the chip enable is high. The data-in terminal can be driven from standard TTL circuits without a pull-up resistor. There is no register on the data-in terminal.

data-out ($\overline{DO}$)

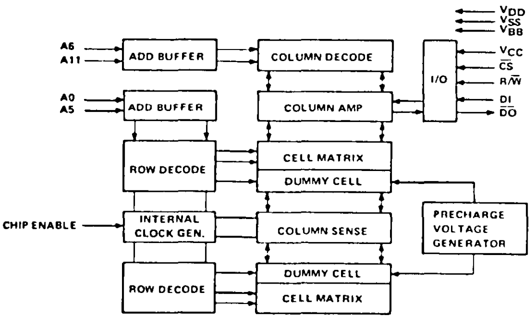
3

The three-state output buffer provides direct TTL compatibility with a fan-out of two Series 74 TTL gates. The output is in the high-impedance (floating) state when the chip enable is low. It remains in the high-impedance state if the chip-select input is high when chip enable goes high and provided that chip select remains high as long as chip enable is high. If the chip select is set up low prior to the rise of chip enable and held low an interval after that rise, the output will be enabled as long as chip enable stays high regardless of subsequent changes in the level of chip select. A data-valid mode is always preceded by a low output state. Data-out is inverted from data-in.

refresh

Refresh must be performed every two milliseconds by cycling through the 64 addresses of the lower-order-address inputs, A0 through A5 (pins 8, 9, 10, 13, 14, 15), or by addressing every row within any 2-millisecond period. Addressing any row refreshes all 64 bits in that row. The chip does not need to be selected during the refresh. If the chip is refreshed during a write mode, then chip select must be high. The column addresses (A6 through A11) can be indeterminate during refresh.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note)	−0.3 to 20 V
Supply voltage, V_{DD} (see Note)	−0.3 to 20 V
Supply voltage, V_{SS} (see Note)	−0.3 to 20 V
All input voltages (see Note)	−0.3 to 20 V
Chip-enable voltage (see Note)	−0.3 to 20 V
Output voltage (operating, with respect to V_{SS})	−2 to 7 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−55°C to 150°C

NOTE: Under absolute maximum ratings, voltage values are with respect to the most-negative supply voltage, V_{BB} (substrate), unless otherwise noted. Throughout the remainder of this data sheet, voltage values are with respect to V_{SS}.

recommended operating conditions (see Note)

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Supply voltage, V_{DD}	11.4	12	12.6	V
Supply voltage, V_{SS}		0		V
Supply voltage, V_{BB}	−2.7	−3	−3.3	V
High-level input voltage, V_{IH} (all inputs except chip enable)	2.2		5.25	V
High-level chip enable input voltage, $V_{IH(CE)}$	V_{DD} −0.6		V_{DD} +1.0	V
Low-level input voltage, V_{IL} (all inputs except chip enable) (see Note)	−0.6		0.6	V
Low-level chip enable input voltage, $V_{IL(CE)}$ (see Note)	−1		0.6	V
Refresh time, $t_{refresh}$			2	ms
Operating free-air temperature, T_A	0		70	°C

NOTE: The algebraic convention where the most negative limit is designated as minimum is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions, T_A = 0°C to 70°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	$I_O = -2$ mA		2.4		V_{CC}	V
V_{OL}	Low-level output voltage	$I_O = 3.2$ mA		V_{SS}		0.4	V
I_I	Input current (all inputs except chip enable)	V_I = 0 to 5.25 V				10	μA
$I_{I(CE)}$	Chip enable input current	V_I = 0 to 13.2 V				2	μA
I_{OZ}	High-impedance-state (off-state output current	V_O = 0 to 5.25 V				10	μA
I_{CC}	Supply current from V_{CC}	2 Series 74 TTL loads				1	mA
I_{DD}	Supply current from V_{DD}	$V_{IH(CE)}$ = 12.6 V			30	60	mA
I_{DD}	Supply current from V_{DD}, standby	$V_{IL(CE)}$ = 0.6 V			20	200	μA
$I_{DD(av)}$	Average supply current from V_{DD} during read or write cycle	Minimum cycle time	TMS 4030		32		mA
			TMS 4030-1		35		
			TMS 4030-2		38		
$I_{DD(av)}$	Average supply current from V_{DD} during read, modify write cycle		TMS 4030		32		mA
			TMS 4030-1		35		
			TMS 4030-2		38		
I_{BB}	Supply current from V_{BB}	V_{BB} = −3.3 V, V_{DD} = 12.6 V,	V_{CC} = 5.25 V, V_{SS} = 0 V		−5	−100	μA

†All typical values are at T_A = 25°C

capacitance at V_{DD} = 12 V, V_{SS} = 0 V, V_{BB} = −3 V, V_{CC} = 5 V, $V_{I(CE)}$ = 0 V, V_I = 0 V, f = 1 MHz, T_A = 0°C to 70°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$C_{i(ad)}$	Input capacitance address inputs			5	7	pF
$C_{i(CE)}$	Input capacitance clock input	$V_{I(CE)}$ = 10.8 V		18	22	pF
		$V_{I(CE)}$ = −1.0 V		23	27	
$C_{i(\overline{CS})}$	Input capacitance chip select input			4	6	pF
$C_{i(data)}$	Input capacitance data input			4	6	pF
$C_{i(R/\overline{W})}$	Input capacitance read/write input			5	7	pF
C_o	Output capacitance			5	7	pF

†All typical values are at T_A = 25°C.

read cycle timing requirements over recommended supply voltage range, T_A = 0°C to 70°C

PARAMETER		TMS 4030		TMS 4030-1		TMS 4030-2		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time	470		430		400		ns
$t_{w(CEH)}$	Pulse width, chip enable high	300	4000	260	4000	230	4000	ns
$t_{w(CEL)}$	Pulse width, chip enable low	130		130		130		ns
$t_{r(CE)}$	Chip-enable rise time		40		40		40	ns
$t_{f(CE)}$	Chip-enable fall time		40		40		40	ns
$t_{su(ad)}$	Address setup time	0↑		0↑		0↑		ns
$t_{su(\overline{CS})}$	Chip-select setup time	0↑		0↑		0↑		ns
$t_{su(rd)}$	Read setup time	0↑		0↑		0↑		ns
$t_{h(ad)}$	Address hold time	150↑		150↑		150↑		ns
$t_{h(\overline{CS})}$	Chip-select hold time	150↑		150↑		150↑		ns
$t_{h(rd)}$	Read hold time	40↓		40↓		40↓		ns

↑↓ The arrow indicates the edge of the chip enable pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

3

read cycle switching characteristics over recommended supply voltage range, T_A = 0°C to 70°C

PARAMETER		TMS 4030		TMS 4030-1		TMS 4030-2		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(CE)}$	Access time from chip enable†		280		230		180	ns
$t_{a(ad)}$	Access time from address†		300		250		200	ns
t_{PHZ} or t_{PLZ}	Output disable time from high or low level‡	30		30		30		ns
t_{PZL}	Output enable time to low level‡		250		200		150	ns

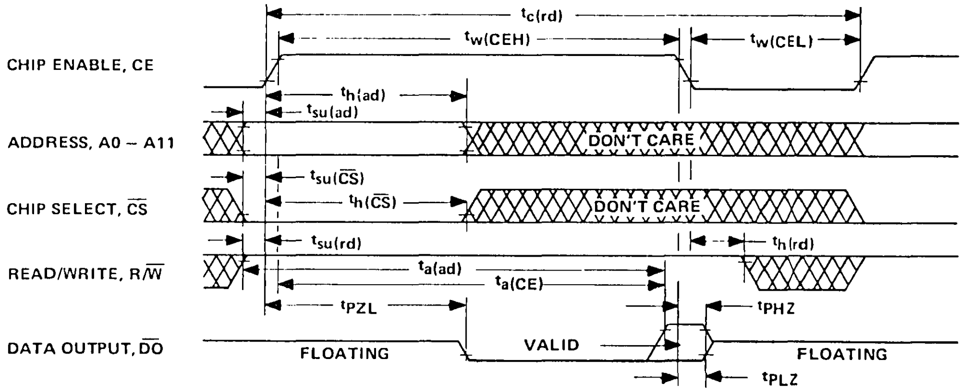
†Test conditions: C_L = 50 pF, $t_{r(CE)}$ = 20 ns, Load = 1 Series 74 TTL gate.
‡Test conditions: C_L = 50 pF, Load = 1 Series 74 TTL gate.

write cycle timing requirements over recommended supply voltage range, T_A = 0°C to 70°C

PARAMETER		TMS 4030		TMS 4030-1		TMS 4030-2		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(wr)}$	Write cycle time	470		430		400		ns
$t_{w(CEH)}$	Pulse width, chip enable high	300	4000	260	4000	230	4000	ns
$t_{w(CEL)}$	Pulse width, chip enable low	130		130		130		ns
$t_{w(wr)}$	Write pulse width	200		190		180		ns
$t_{r(CE)}$	Chip-enable rise time		40		40		40	ns
$t_{f(CE)}$	Chip-enable fall time		40		40		40	ns
$t_{su(ad)}$	Address setup time	0↑		0↑		0↑		ns
$t_{su(\overline{CS})}$	Chip-select setup time	0↑		0↑		0↑		ns
$t_{su(da\text{-}wr)}$	Data-to-write setup time*	0		0		0		ns
$t_{su(wr)}$	Write-pulse setup time	240↓		220↓		210↓		ns
$t_{h(ad)}$	Address hold time	150↑		150↑		150↑		ns
$t_{h(\overline{CS})}$	Chip-select hold time	150↑		150↑		150↑		ns
$t_{h(da)}$	Data hold time	40↓		40↓		40↓		ns

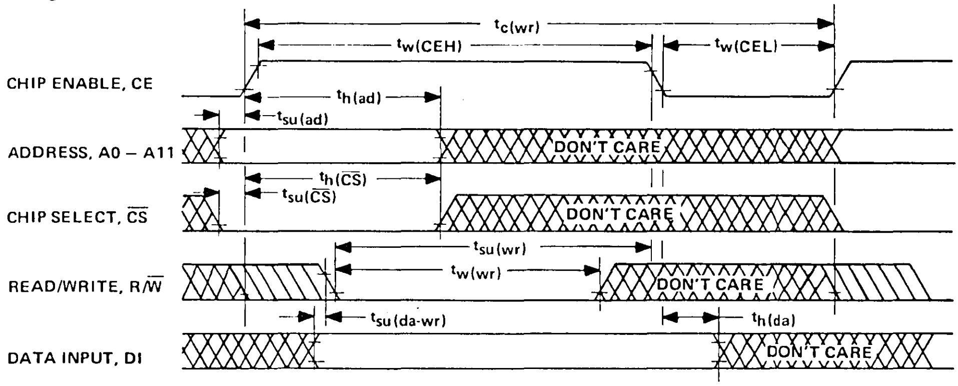
↑↓ The arrow indicates the edge of the chip enable pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.
*If R/$\overline{W}$ is low before CE goes high then DI must be valid when CE goes high.

read cycle timing



NOTE: For the chip-enable input, high and low timing points are 90% and 10% of $V_{IH(CE)}$. Other input timing points are 0.6 V (low) and 2.2 V (high). Output timing points are 0.4 V (low) and 2.4 V (high).

write cycle timing



NOTE: For the chip-enable input, high and low timing points are 90% and 10% of $V_{IH(CE)}$. Other input timing points are 0.6 V (low) and 2.2 V (high). Output timing points are 0.4 V (low) and 2.4 V (high). During the time from the rise of CE to the fall of R/$\overline{W}$, R/$\overline{W}$ is permitted to change from high to low only.

read, modify write cycle timing requirements over recommended supply voltage range, T_A = 0°C to 70°C

PARAMETER		TMS 4030		TMS 4030-1		TMS 4030-2		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(RMW)}$	Read, modify write cycle time*	710		640		580		ns
$t_{w(CEH)}$	Pulse width, chip enable high*	540	4000	470	4000	410	4000	ns
$t_{w(CEL)}$	Pulse width, chip enable low	130		130		130		ns
$t_{w(wr)}$	Write-pulse width	200		190		180		ns
$t_{r(CE)}$	Chip-enable rise time		40		40		40	ns
$t_{f(CE)}$	Chip-enable fall time		40		40		40	ns
$t_{su(ad)}$	Address setup time	0↑		0↑		0↑		ns
$t_{su(\overline{CS})}$	Chip-select setup time	0↑		0↑		0↑		ns
$t_{su(da\text{-}wr)}$	Data-to-write setup time	0		0		0		ns
$t_{su(rd)}$	Read pulse setup time	0↑		0↑		0↑		ns
$t_{su(wr)}$	Write pulse setup time	240↓		220↓		210↓		ns
$t_{h(ad)}$	Address hold time	150↑		150↑		150↑		ns
$t_{h(\overline{CS})}$	Chip-select hold time	150↑		150↑		150↑		ns
$t_{h(rd)}$	Read hold time	280↑		230↑		180↑		ns
$t_{h(da)}$	Data hold time	40↓		40↓		40↓		ns

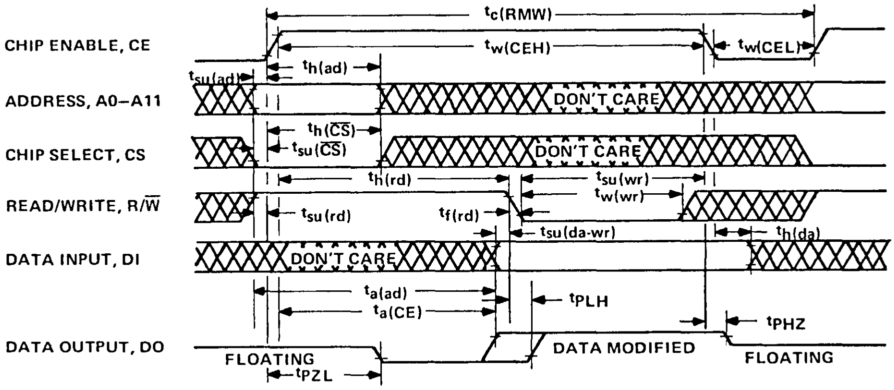
↑↓ The arrow indicates the edge of the chip-enable pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.
*Test conditions: $t_{f(rd)}$ = 20 ns.

read, modify write cycle switching characteristics over recommended supply voltage range, T_A = 0°C to 70°C

PARAMETER		TMS 4030		TMS 4030-1		TMS 4030-2		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(CE)}$	Access time from chip enable†		280		230		180	ns
$t_{a(ad)}$	Access time from address†		300		250		200	ns
t_{PLH}	Propagation delay time, low-to-high level output from write pulse‡	30		30		30		ns
t_{PHZ}	Output disable time from high level‡	30		30		30		ns
t_{PZL}	Output enable time to low level‡		250		200		150	ns

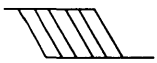
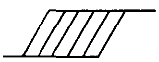
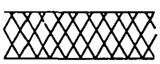
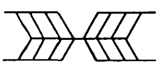
†Test conditions: C_L = 50 pF, $t_{r(CE)}$ = 20 ns, Load = 1 Series 74 TTL gate.
‡Test Conditions: C_L = 50 pF, Load = 1 Series 74 TTL gate.

read, modify write cycle timing

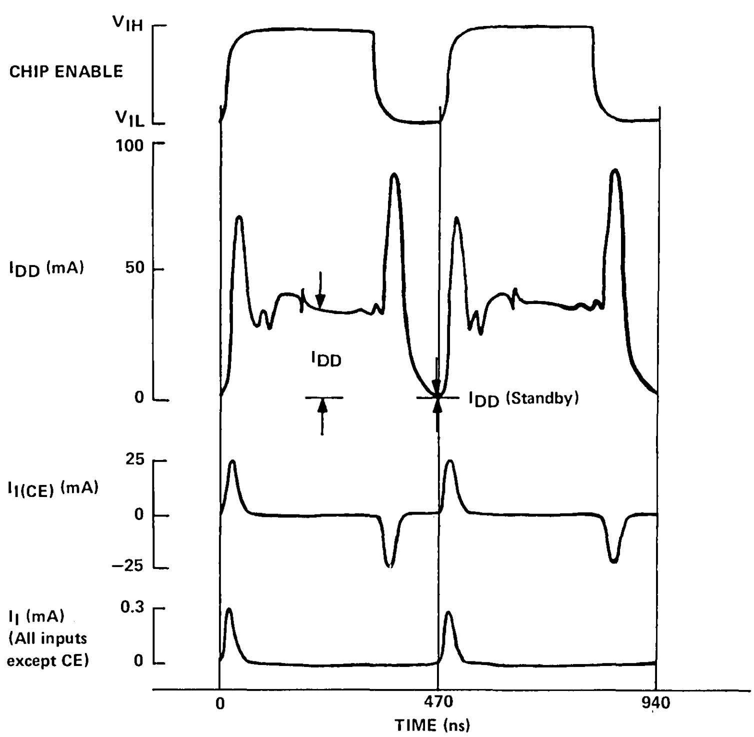


NOTE: For the chip enable input, high and low timing points are 90% and 10% of $V_{IH(CE)}$. Other input timing points are 0.6 V (low) and 2.2 V (high). Output timing points are 0.4 V (low) and 2.4 V (high).

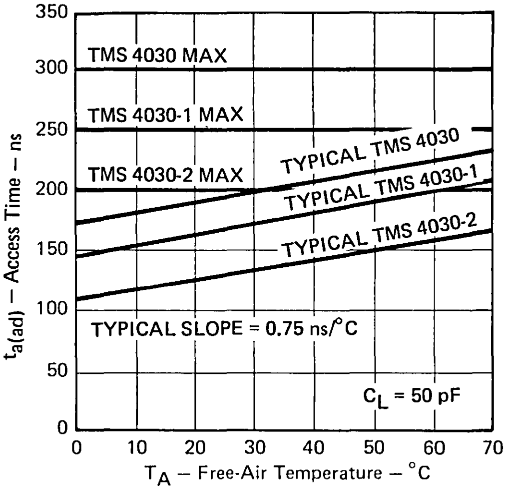
timing diagram conventions

TIMING DIAGRAM SYMBOL	MEANING: INPUT FORCING FUNCTIONS	MEANING: OUTPUT RESPONSE FUNCTIONS
	Must be steady high or low	Will be steady high or low
	High-to-low changes permitted	Will be changing from high to low sometime during designated interval
	Low-to-high changes permitted	Will be changing from low to high sometime during designated interval
	Don't Care	State unknown or changing
	(Does not apply)	Center line is high-impedance off-state

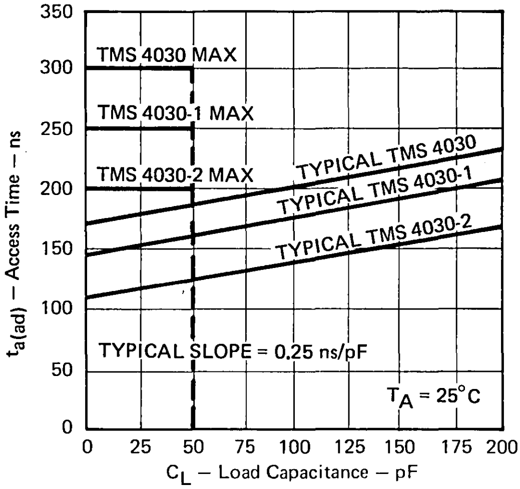
TYPICAL WAVEFORMS



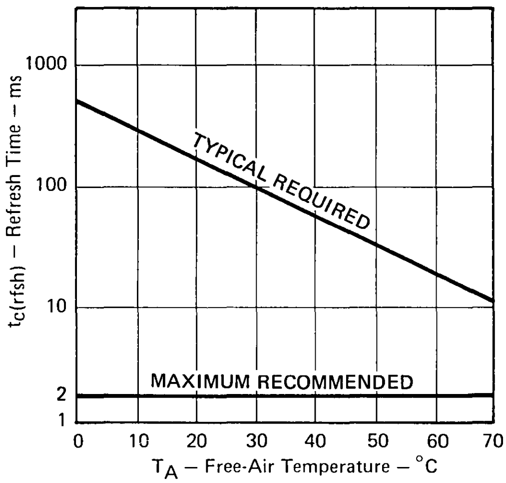
ACCESS TIMES vs TEMPERATURE



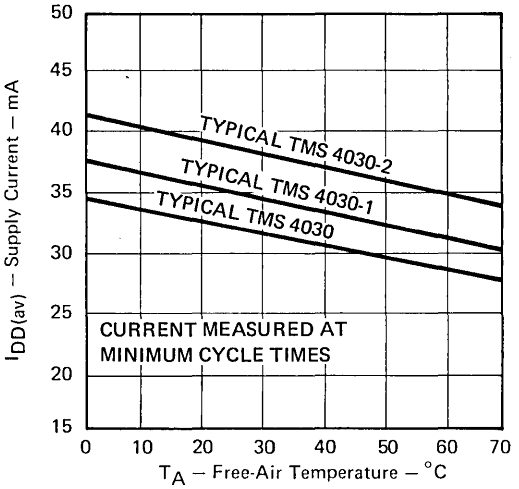
ACCESS TIMES vs LOAD CAPACITANCE



REFRESH TIME vs TEMPERATURE



AVERAGE CURRENT vs TEMPERATURE



PRINTED IN U.S.A. 27!

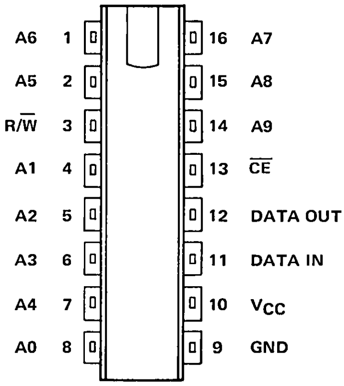
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TMS 4033 JL, NL; TMS 4034 JL, NL; TMS 4035 JL, NL
1024-WORD BY 1-BIT STATIC RANDOM-ACCESS MEMORIES

BULLETIN NO. DL-S 7512189, OCTOBER 1974—REVISED MAY 1975

- 1024 x 1-Bit Organization
- Static Operation (No Clocks, No Refresh)
- Input Interface
  - Fully Decoded
  - TTL Compatible
  - Static Charge Protection
- Output Interface
  - 3-State
  - Fan-out 1 Series 74 TTL Load
  - OR-Tie Capability
- Access Time
  - TMS 4033 JL, NL . . . 450 ns Max
  - TMS 4034 JL, NL . . . 650 ns Max
  - TMS 4035 JL, NL . . . 1000 ns Max
- Interchangeable with Intel 2102-1, 2102-2, and 2102 Respectively
- N-Channel Silicon-Gate Technology

16-PIN CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGES
(TOP VIEW)



3

description

This series is a family of static random-access memories, each organized as 1024 one-bit words. Due to their static design, system overhead costs are minimized by elimination of refresh-clocking circuitry and by simplification of the timing requirements. In addition all inputs and outputs are fully compatible with Series 74 TTL, including the single 5-volt power supply. These memories are fabricated by means of the same technology employed with the TMS 4030 JL, NL 4K RAM — N-channel silicon-gate. This technology provides optimum chip density and performance when cost is considered. Three performance ranges allow the designer to better match the memory to the specific system requirements, thereby maximizing the cost/performance trade-off.

The TMS 4033, TMS 4034, and TMS 4035 are offered in 16-pin dual-in-line ceramic (JL suffix) and plastic (NL suffix) packages designed for insertion in mounting-hole rows on 300-mil centers. These devices are characterized for operation from 0°C to 70°C.

operation

Addresses (A0-A9)

Address inputs are used to select individual storage locations within the RAM. Since the addresses are not latched, the address-valid time determines the cycle time during both the read and write cycle. Therefore, the address-valid time must be a minimum of 450 nanoseconds for the TMS 4033, 650 nanoseconds for the TMS 4034, and 1000 nanoseconds for the TMS 4035. The address inputs can be driven from standard Series 54/74 TTL with no external pull-up resistors.

operation (continued)

Chip Enable ($\overline{CE}$)

The $\overline{CE}$ input is used to enable the memory chip for a reading or writing operation. In a single-chip system, this pin can be hardwired to ground so that the chip is continuously enabled. For the read cycle, chip-enable low must extend past the address to ensure valid data for that address. Once the chip-enable goes high, the output buffer will immediately return to the high-impedance state. For the write cycle, chip-enable low must occur before the read/write input goes to the write state ensuring no ambiguity in the chip enabled for a particular write cycle. This input can be driven from Series 54/74 TTL with no external pull-up resistors.

Read/Write (R/$\overline{W}$)

In the write mode prior to an address change, R/$\overline{W}$ must be in the read state (high level) and must remain in that state for a minimum period to eliminate the possibility of data being written into an unwanted location. The read/write input is TTL compatible without external pull-up resistors.

3

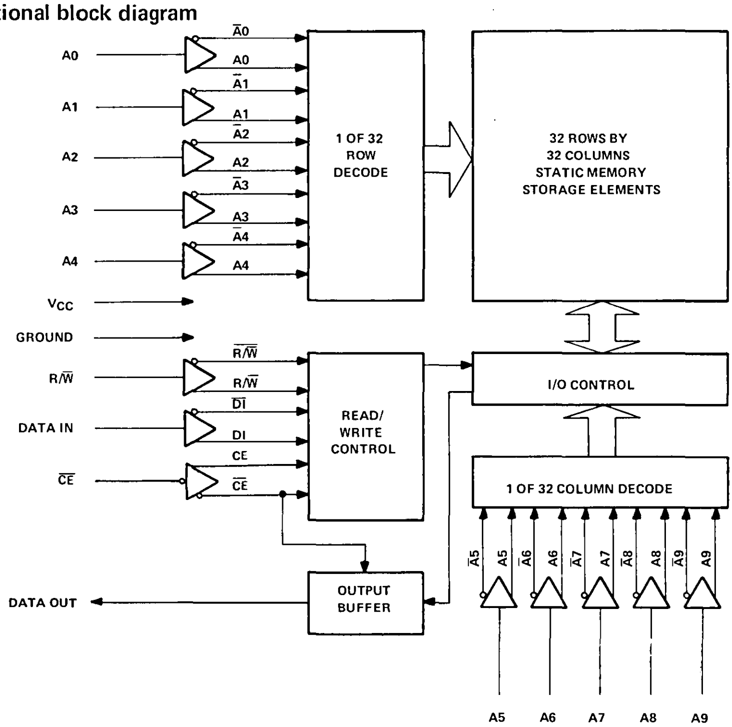
Data In (DI)

The DI input accepts the input data during the write mode. During a write cycle, data must be valid for a minimum time period before the read/write input is brought to the read state ensuring that proper data will enter the location selected. To eliminate any data ambiguity, data must be held valid past the end of the write pulse.

Data Out (DO)

Data out is a three-state terminal controlled by the chip-enable input, which supplies output data during a read cycle. A high level on chip enable places the data-out terminal in the high-impedance state.

functional block diagram



FUNCTION TABLE

$\overline{CE}$	R/$\overline{W}$	I/O
L	L	WRITE
L	H	READ
H	X	HIGH Z

H = HIGH LEVEL
L = LOW LEVEL

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{CC} (see Note 1) . . . . −0.5 to 7 V
Input voltage (any input) (see Note 1) . . . . −0.5 to 7 V
Continuous power dissipation . . . . 1 W
Operating free-air temperature range . . . . 0°C to 70°C
Storage temperature range . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to the ground terminal.

*COMMENT: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2.2		V_{CC}	V
Low-level input voltage, V_{IL} (see Note 2)	−0.3		0.65	V
Operating free-air temperature, T_A	0		70	°C

NOTE 2: The algebraic convention where the most negative limit is designated as minimum is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -100\ \mu A$,	$V_{CC} = 4.75$ V	2.2			V
V_{OL}	Low-level output voltage	$I_{OL} = 1.9$ mA,	$V_{CC} = 5.25$ V			0.45	V
I_I	Input current	$V_I = 0$ to 5.25 V				±10	μA
I_{OZH}	Off-state output current, high-level voltage applied	$\overline{CE}$ at 2.2 V,	$V_O = 4$ V			10	μA
I_{OZL}	Off-state output current, low-level voltage applied	$\overline{CE}$ at 2.2 V,	$V_O = 0.45$ V		−10	−100	μA
I_{CC}	Supply current from V_{CC}	$V_{CC} = 5.25$ V, All inputs at 5.25 V	Data out open,		45	70	mA
C_i	Input capacitance	$T_A = 25°C$,	f = 1 MHz		3	5	pF
C_o	Output capacitance	$T_A = 25°C$,	f = 1 MHz		7	10	pF

†All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

conditions for testing timing requirements

Input high levels . . . . 2.2 V
Input low levels . . . . 0.65 V
Input rise and fall times . . . . 20 ns
Output load . . . . 1 Series 74 TTL load, $C_L = 100$ pF
All timing requirements . . . . 50% point of waveform

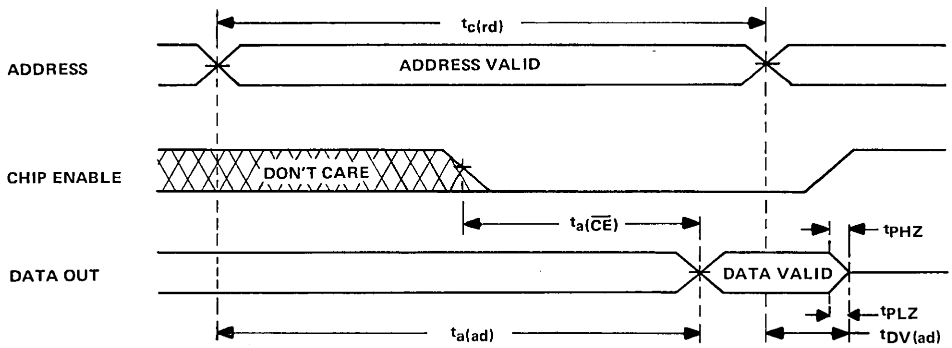
3

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

read cycle timing requirements over recommended supply voltage range, T_A = 0°C to 70°C (unless otherwise noted)

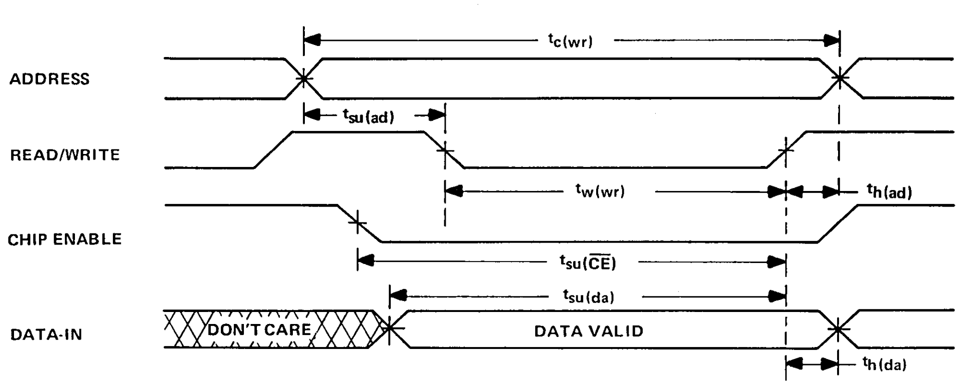
PARAMETER		TMS 4033			TMS 4034			TMS 4035			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	MIN	TYP†	MAX	
$t_{c(rd)}$	Read cycle time	450			650			1000			ns
$t_{a(ad)}$	Access time from address		300	450		450	650		500	1000	ns
$t_{a(\overline{CE})}$	Access time from chip enable			200			300			500	ns
$t_{DV(ad)}$	Previous output data valid from address	50			50			50			ns
t_{PHZ} or t_{PLZ}	Output disable time from chip enable	0		200	0		200	0		200	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.



write cycle timing requirements over recommended supply voltage range, T_A = 0°C to 70°C

PARAMETER		TMS 4033		TMS 4034		TMS 4035		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(wr)}$	Write cycle time	450		650		1000		ns
$t_{w(wr)}$	Write pulse width	250		400		750		ns
$t_{su(ad)}$	Address setup time	150		200		200		ns
$t_{su(\overline{CE})}$	Chip enable to write setup time	350		550		850		ns
$t_{su(da)}$	Data-in to write setup time	300		450		800		ns
$t_{h(ad)}$	Address hold time	50		50		50		ns
$t_{h(da)}$	Data hold time	50		50		50		ns



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

MOS LSI

TMS 4036 JL, NL; TMS 4036-1 JL, NL; TMS 4036-2 JL, NL
64-WORD BY 8-BIT STATIC RANDOM-ACCESS MEMORIES

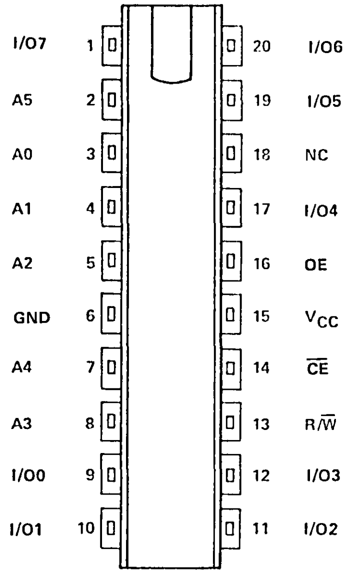
BULLETIN NO. DL-S 7512277, MAY 1975

- 64 x 8 Organization
- Static Operation (No Clocks, No Refresh)
- Compact 20-Pin 300-Mil Dual-in-Line Package
- 3 Performance Ranges:

	ACCESS TIME (MAX)	READ OR WRITE CYCLE (MIN)
TMS 4036	1000 ns	1000 ns
TMS 4036-1	650 ns	650 ns
TMS 4036-2	450 ns	450 ns

- Multiplexed Common Bus I/O
- Input Interface
  - Fully Decoded
  - TTL Compatible
  - Static Charge Protection
- Output Interface
  - 3-State
  - Fan-Out 1 Series 74 TTL Load
  - OR-Tie Capability
- Power Dissipation . . . 450 mW Maximum
- N-Channel Silicon-Gate Technology
- 8-Bit Word Length Ideal for Microprocessor-Based Systems

20-PIN CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGES
(TOP VIEW)



3

description

This series of static random-access memories is organized as 64 words of 8 bits. Data inputs and outputs are multiplexed on an 8-bit, bidirectional bus controlled by the combination of chip enable and output enable. Static design results in reduced overhead costs by elimination of refresh-clocking circuitry and by simplification of the timing requirements. In addition, all inputs and outputs are fully compatible with Series 74 TTL, including the single 5-volt power supply. The TMS 4036 series is manufactured using TI's reliable N-channel silicon-gate technology to optimize the cost/performance relationship. Readout is nondestructive and the output data polarity is not inverted from data-in.

The TMS 4036 is offered in compact 20-pin ceramic (JL suffix) and plastic (NL suffix) dual-in-line packages designed for insertion in mounting-hole rows on 300-mil centers. The series is guaranteed for operation from 0°C to 70°C.

operation

addresses (A0-A5)

The 6-bit address selects one of 64 8-bit words. The address-valid time determines cycle time during both the read and write cycles. The address inputs can be driven directly from standard Series 54/74 TTL with no external pull-up resistors required.

75

PRELIMINARY DATA SHEET:
Supplementary data may be published at a later date.

operation (continued)

chip enable ($\overline{CE}$)

The $\overline{CE}$ terminal is used to enable a specific memory device. If $\overline{CE}$ is low, the device is enabled for either a read or write cycle, depending on the state of the read/write and output-enable terminals. When $\overline{CE}$ is high, the I/O buffers are in the high-impedance state. $\overline{CE}$ may be driven from Series 74 TTL. For a more complete understanding of $\overline{CE}$, see the section on output enable.

read/write (R/$\overline{W}$)

The R/$\overline{W}$ input must be high during read and low during write operations. Prior to an address change, R/$\overline{W}$ must be in the read state and must remain in that state for a minimum period to eliminate the possibility of data being written into an unwanted position. The R/$\overline{W}$ input is TTL-compatible and does not require external resistors.

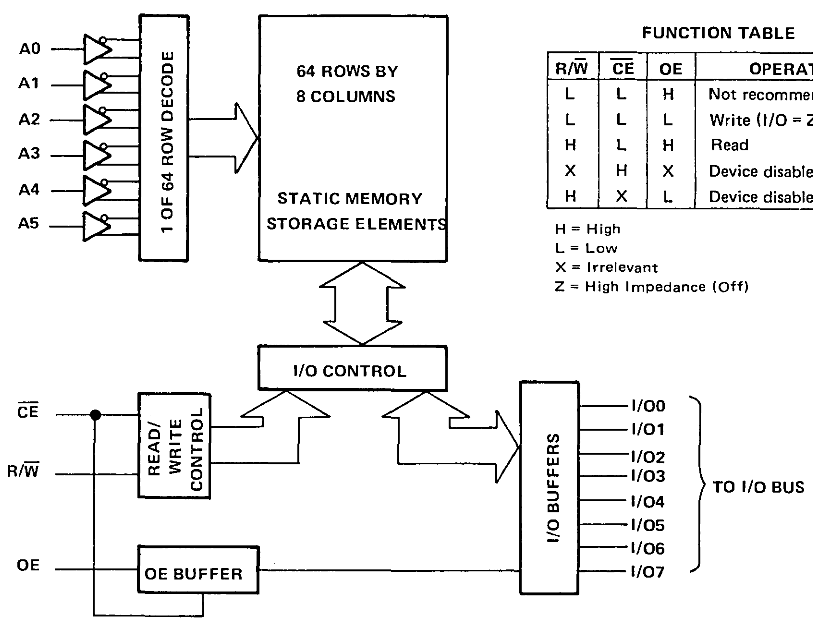
output enable (OE)

The output enable terminal controls the I/O buffer and determines whether the bus is in an input or output mode. When OE is low, the I/O terminals are in the input configuration; when OE is high, the I/O terminals are in the output configuration. The read cycle and write cycle timing diagrams show in detail the relation between $\overline{CE}$, OE, and the other signals (refer to the function table). This input is also compatible with Series 74 TTL circuits.

input/output buffer (I/O0-I/O7)

Each of these terminals interface directly with the external data bus and have the capability of being both an input and an output buffer. These buffers are controlled by a combination of $\overline{CE}$ and OE as described in the output enable section. Each buffer is three-state and fully TTL compatible, both as an input and an output.

functional block diagram



FUNCTION TABLE

R/$\overline{W}$	$\overline{CE}$	OE	OPERATION
L	L	H	Not recommended
L	L	L	Write (I/O = Z)
H	L	H	Read
X	H	X	Device disabled (I/O = Z)
H	X	L	Device disabled (I/O = Z)

H = High
L = Low
X = Irrelevant
Z = High Impedance (Off)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{CC} (see Notes 1 and 2)	−0.5 to 7 V
Input voltage (any input) (see Notes 1 and 2)	−0.5 to 7 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTES:
1. Voltage values are with respect to the ground terminal.
2. For all combinations of inputs, the I/O lines may be shorted to V_{SS} or V_{CC} for a period not to exceed five milliseconds.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

PARAMETER	TMS 4036			TMS 4036-1			TMS 4036-2			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	V
Supply voltage, V_{SS}		0			0			0		V
High-level input voltage, V_{IH}	2.2		V_{CC}	2.2		V_{CC}	2.2		V_{CC}	V
Low-level input voltage, V_{IL} (see Note 3)	−0.3		0.8	−0.3		0.8	−0.3		0.8	V
Read cycle time, $t_{c(rd)}$	1000			650			450			ns
Write cycle time, $t_{c(wr)}$	1000			650			450			ns
Write pulse width, $t_{w(wr)}$	500			300			200			ns
Address setup time, $t_{su(ad)}$	450			300			200			ns
Chip-enable setup time, $t_{su(\overline{CE})}$	700			500			400			ns
Data setup time, $t_{su(da)}$	600			400			300			ns
Address hold time, $t_{h(ad)}$	50			50			50			ns
Data hold time, $t_{h(da)}$	50			50			50			ns
Operating free-air temperature, T_A	0		70	0		70	0		70	°C

NOTE 3: The albegraic convention where the most negative limit is designated as minimum is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

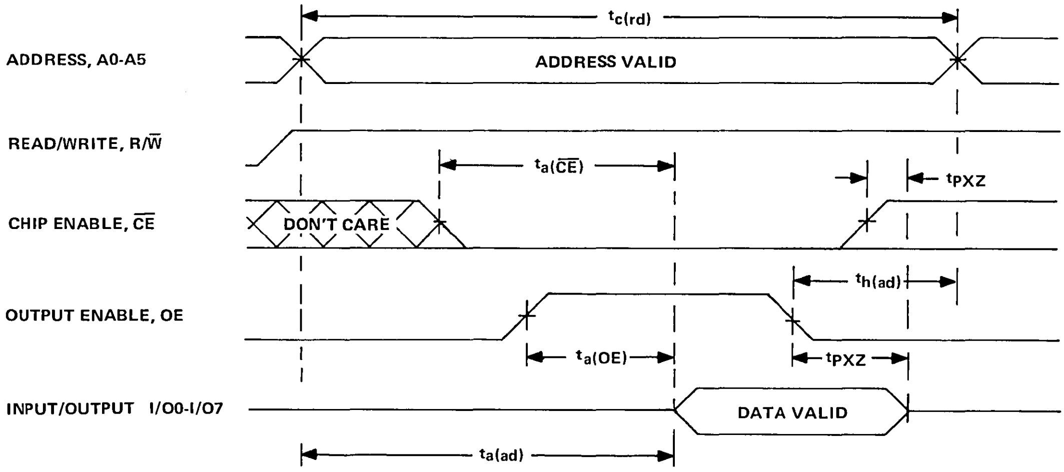
PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -100\ \mu A$,	$V_{CC} = 4.75$ V	2.4		V
V_{OL}	Low-level output voltage	$I_{OL} = 1.9$ mA,	$V_{CC} = 4.75$ V		0.4	V
I_{IH}	High-level input current into address, R/$\overline{W}$, $\overline{CE}$, or OE	$V_I = 5.25$ V			10	µA
I_{OZH}	Off-state output current, high-level voltage applied at I/O terminal	$V_O = 5.25$ V, $\overline{CE}$ at 5.25 V	OE at 0 V,		10	µA
		$V_O = 5.25$ V, $\overline{CE}$ at 2.2 V	OE at 5.25 V,		10	
		$V_O = 5.25$ V, $\overline{CE}$ at 0 V	OE at 0.8 V,		10	
I_{OZL}	Off-state output current, low-level voltage applied at I/O terminal	$V_O = 0$ V, $\overline{CE}$ at 2.2 V	OE at 5.25 V,		−100	µA
		$V_O = 0$ V, $\overline{CE}$ at 0 V	OE at 0.8 V,		−100	
I_{CC}	Supply current from V_{CC}				85	mA
C_i	Input capacitance	f = 1 MHz,	$T_A = 25°C$		10	pF
$C_{i/o}$	I/O terminal capacitance	f = 1 MHz,	$T_A = 25°C$		20	pF

switching characteristics over recommended supply voltage ranges, T_A = 0°C to 70°C

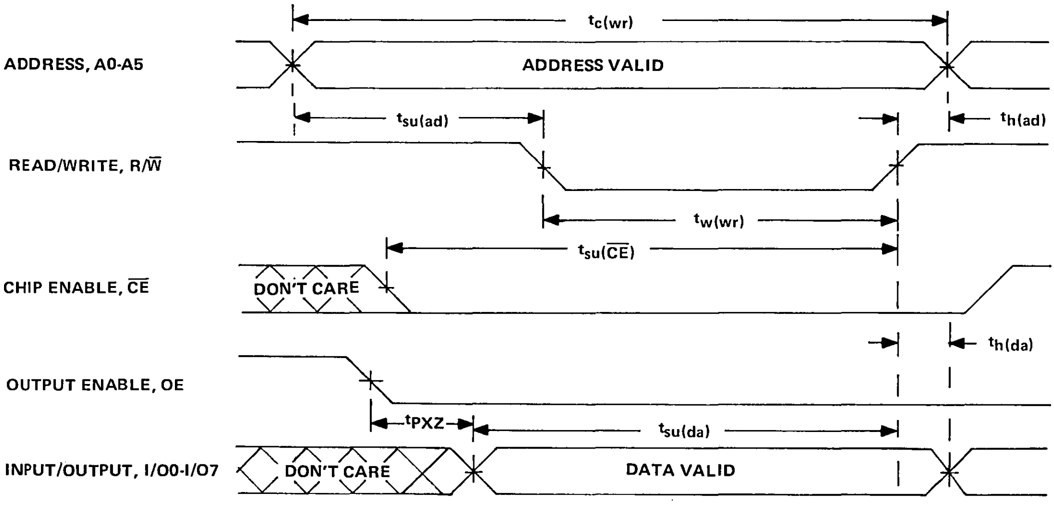
PARAMETER		TMS 4036			TMS 4036-1			TMS 4036-2			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	MIN	TYP†	MAX	
$t_{a(ad)}$	Access time from address			1000			650			450	ns
$t_{a(\overline{CE})}$	Access time from chip enable			200			190			180	ns
$t_{a(OE)}$	Access time from output enable			200			190			180	ns
t_{PXZ}	Output disable time from chip enable	0	60	200	0	60	200	0	60	200	ns
t_{PXZ}	Output disable time from output enable (see Note 4)	0	60	200	0	60	200	0	60	200	ns

NOTE 4: This parameter defines the delay for the I/O bus to enter the input mode.
†All typical values are at T_A = 25°C.

read cycle timing



write cycle timing



NOTE: For measuring timing requirements and characteristics, V_{IH} = 2.2 V, V_{IL} = 0.65 V, t_r = t_f = 20 ns and all timing points are 50% points.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TMS 4039 JL, NL; TMS 4039-1 JL, NL; TMS 4039-2 JL, NL
256-WORD BY 4-BIT STATIC RANDOM-ACCESS MEMORIES

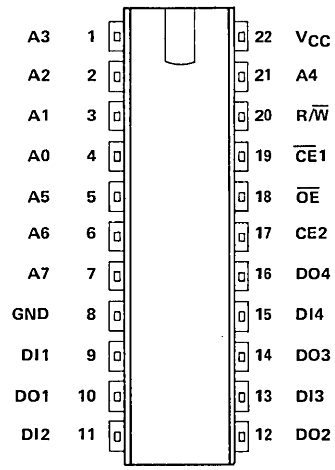
BULLETIN NO. DL-S 7512271, MAY 1975

- 256 x 4 Organization
- Static Operation (No Clocks, No Refresh)
- 3 Performance Ranges:

	ACCESS TIME (MAX)	READ OR WRITE CYCLE (MIN)
TMS 4039	1000 ns	1000 ns
TMS 4039-1	650 ns	650 ns
TMS 4039-2	450 ns	450 ns

- Input Interface
  - Fully Decoded
  - TTL-Compatible
  - Static Charge Protection
- Output Interface
  - Two Chip-Enable Inputs for OR-Tie Capability
  - Fan-out to 1 Series 74 TTL Load
  - 3-State Outputs and Output Enable Control for Common I/O Data Bus Systems
- Power Dissipation . . . 175 mW Typical
- Organized for Microprocessor-Based Systems
- Interchangeable with Intel 2101, 2101-2, and 2101-1, Respectively

22-PIN CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGES
(TOP VIEW)



description

This series of static random-access memories is organized as 256 words of 4 bits. Static design results in reduced overhead costs by elimination of refresh-clocking circuitry and by simplification of timing requirements. All inputs and outputs are fully compatible with Series 74 TTL, including the single 5-volt power supply. The TMS 4039 series is manufactured using TI's reliable N-channel enhancement-type silicon-gate technology to optimize the cost/performance relationship. Readout is nondestructive and output data is not inverted from data in.

The TMS 4039 series is offered in 22-pin dual-in-line ceramic (JL suffix) and plastic (NL suffix) packages designed for insertion in mounting-hole rows on 400-mil centers. The series is characterized for operation from 0°C to 70°C.

operation

addresses (A0-A7)

The eight address inputs select one of 256 4-bit words. The address inputs can be driven directly from standard Series 54/74 TTL with no external pull-up resistors.

chip enable ($\overline{CE}1$ and CE2)

To enable the device, $\overline{CE}1$ must be low and CE2 must be high. The two chip-enable terminals can be driven from a common source with an inverter or either terminal can be hard wired to its enabled level. When the memory is disabled, data cannot be entered and the outputs are in the high-impedance state.

PRELIMINARY DATA SHEET:
Supplementary data may be published at a later date.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

operation (continued)

read/write (R/$\overline{W}$)

The R/$\overline{W}$ input must be high during read and low during write operations. Prior to an address change, R/$\overline{W}$ must be in the read state and must remain in that state for a minimum period to eliminate the possibility of data being written into an unwanted position. The R/$\overline{W}$ input is TTL-compatible and does not require external resistors.

output enable ($\overline{OE}$)

The output enable must be low to read for when it is high the outputs are in the high-impedance state useful for OR-ties or common input/output operation. When the device is not used in the common-input/output configuration, the output enable terminal can be hard wired low.

data in (DI1-DI4)

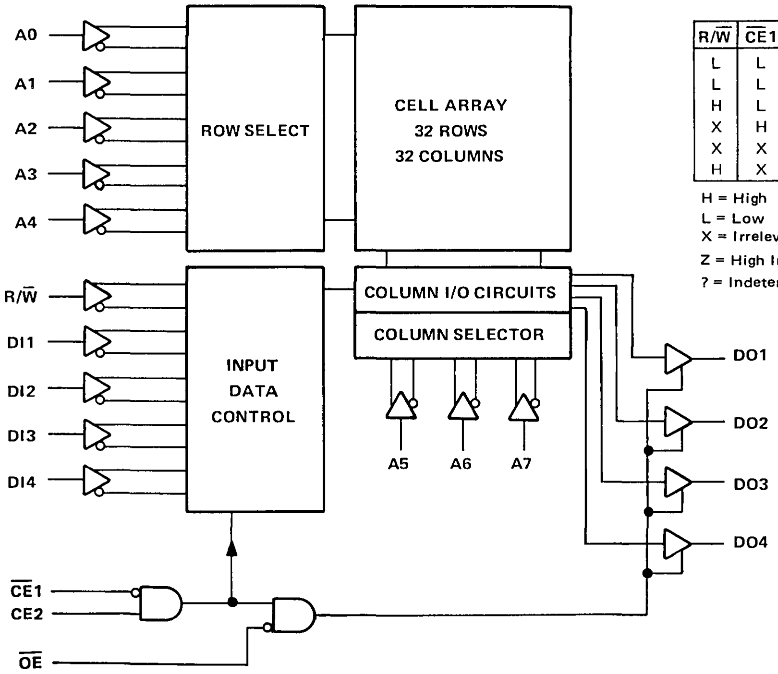
The DI inputs accept input data during a write operation. During a write cycle, data must be set up a minimum time before R/$\overline{W}$ goes to the read state (high) to ensure that correct data will enter the addressed memory cell. Also, input data must be held valid a minimum time after the rise of R/$\overline{W}$.

3

data out (DO1-DO4)

Data out is a three-state terminal controlled by $\overline{OE}$, $\overline{CE}$1, and CE2. To read data, $\overline{CE}$1 and $\overline{OE}$ must be low with CE2 high. When $\overline{OE}$ or $\overline{CE}$1 goes high or CE2 goes low, the output terminals are forced to the high-impedance state.

functional block diagram



FUNCTION TABLE

R/$\overline{W}$	$\overline{CE}$1	CE2	$\overline{OE}$	OPERATION
L	L	H	L	Write (DO = ?)
L	L	H	H	Write (DO = Z)
H	L	H	L	Read
X	H	X	X	Device Disabled (DO = Z)
X	X	L	X	Device Disabled (DO = Z)
H	X	X	H	Device Disabled (DO = Z)

H = High
L = Low
X = Irrelevent
Z = High Impedance
? = Indeterminate

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{CC} (see Note 1)	−0.5 to 7 V
Input voltage (any input) (see Note 1)	−0.5 to 7 V
Continuous power dissipation	1 W
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: Voltage values are with respect to the ground terminal.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

PARAMETER	TMS 4039			TMS 4039-1			TMS 4039-2			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	V
High-level input voltage, V_{IH}	2.2		V_{CC}	2.2		V_{CC}	2.2		V_{CC}	V
Low-level input voltage, V_{IL} (see Note 2)	−0.5		0.65	−0.5		0.65	−0.5		0.65	V
Read cycle time, $t_{c(rd)}$	1000			650			450			ns
Write cycle time, $t_{c(wr)}$	1000			650			450			ns
Write pulse width, $t_{w(wr)}$	800			450			300			ns
Address setup time, $t_{su(ad)}$	150			150			100			ns
Chip-enable setup time, $t_{su(CE)}$	900			550			400			ns
Data setup time, $t_{su(da)}$	700			400			280			ns
Address hold time, $t_{h(ad)}$	50			50			50			ns
Data hold time, $t_{h(da)}$	100			100			100			ns
Operating free-air temperature, T_A	0		70	0		70	0		70	°C

NOTE 2: The algebraic convention where the most negative limit is designated as minimum is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -150\ \mu A$,	$V_{CC} = 4.75$ V	2.2			V
V_{OL}	Low-level output voltage	$I_{OL} = 2$ mA,	$V_{CC} = 5.25$ V			0.45	V
I_I	Input current	$V_I = 0$ to 5.25 V				±10	µA
I_{OZH}	Off-state output current, high-level voltage applied	$\overline{CE}$ at 2.2 V,	$V_O = 4$ V			15	µA
I_{OZL}	Off-state output current, low-level voltage applied	$\overline{CE}$ at 2.2 V,	$V_O = 0.45$ V			−50	µA
I_{CC}	Supply current from V_{CC}	$V_{CC} = 5.25$ V, $I_O = 0$ mA	$T_A = 25°C$			60	mA
			$T_A = 0°C$			70	
C_i	Input capacitance	$V_I = 0$ V, f = 1 MHz	$T_A = 25°C$,		4	8	pF
C_o	Output capacitance	$V_O = 0$ V, f = 1 MHz	$T_A = 25°C$,		8	12	pF

†All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

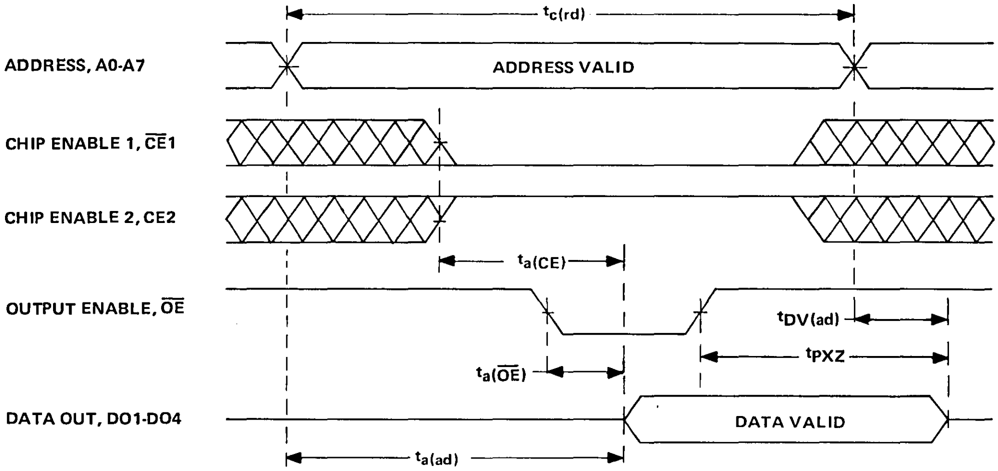
switching characteristics over recommended supply voltage range, $T_A = 0°C$ to $70°C$, 1 Series 74 TTL load, $C_L = 100$ pF

PARAMETER		TMS 4039		TMS 4039-1		TMS 4039-2		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(ad)}$	Access time from address		1000		650		450	ns
$t_{a(CE)}$	Access time from chip enable $\overline{CE1}$ or CE2		800		400		350	ns
$t_{a(\overline{OE})}$	Access time from output enable		700		350		300	ns
$t_{DV(ad)}$	Previous output data valid after address change	40		40		40		ns
t_{PXZ}	Output disable time from output enable (see Note 3)	0	200	0	150	0	150	ns

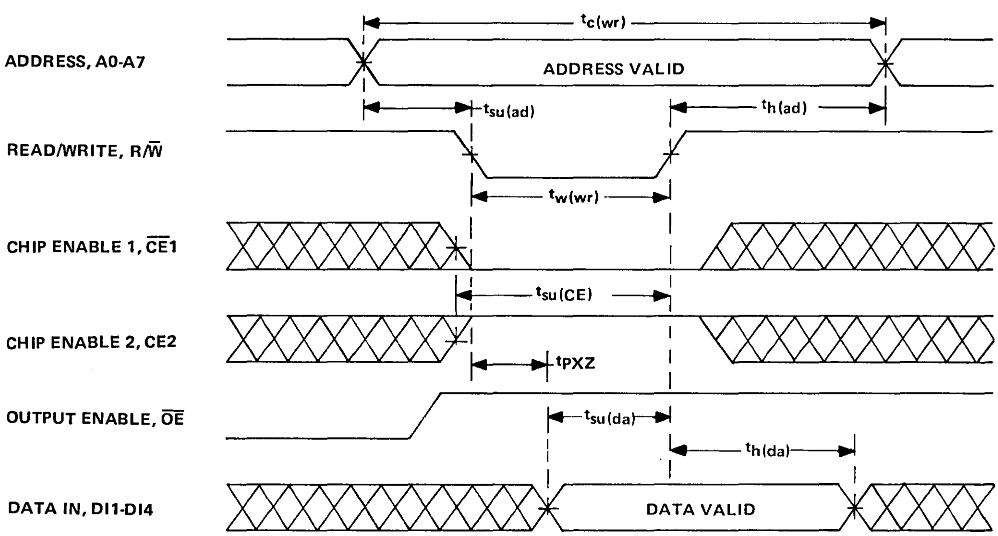
NOTE 3: With the outputs OR-tied to the inputs, this parameter defines the delay for the I/O bus to enter the input mode.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

read cycle timing



write cycle timing



NOTE: For measuring timing requirements and characteristics, V_{IH} = 2.2 V, V_{IL} = 0.65 V, t_r = t_f = 20 ns and all timing points are 50% points.

PRINTED IN U.S.A 575

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TMS 4042 JL, NL; TMS 4042-1 JL, NL; TMS 4042-2 JL, NL
256-WORD BY 4-BIT STATIC RANDOM-ACCESS MEMORIES

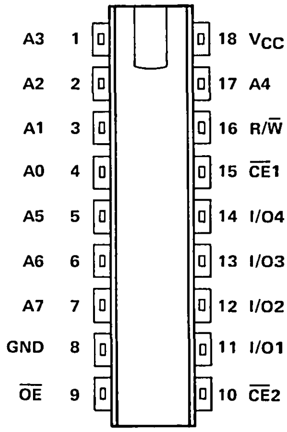
BULLETIN NO. DL-S 7512269, MAY 1975

- 256 x 4 Organization
- Common I/O
- 18-Pin Package
- Static Operation (No Clocks, No Refresh)
- 3 Performance Ranges:

	ACCESS TIME (MAX)	READ OR WRITE CYCLE (MIN)
TMS 4042	1000 ns	1000 ns
TMS 4042-1	650 ns	650 ns
TMS 4042-2	450 ns	450 ns

- Input Interface
  - Fully Decoded
  - TTL-Compatible
  - Static Charge Protection
- Output Interface
  - Two Chip-Enable Inputs for OR-Tie Capability
  - Fan-out to 1 Series 74 TTL Load
  - 3-State Outputs and Output Enable Control for Common I/O Data Bus Systems
- Power Dissipation . . . 175 mW Typical
- Organized for Microprocessor-Based Systems
- Interchangeable with Intel 2111, 2111-2, and 2111-1, Respectively

18-PIN CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGES
(TOP VIEW)



description

This series of static random-access memories is organized as 256 words of 4 bits. Static design results in reduced overhead costs by elimination of refresh-clocking circuitry and by simplification of timing requirements. The use of common input/output terminals, controlled by the chip enable and output enable terminals, allows the use of an 18-pin package and saves board space in comparison to the TMS 4039. The common input/outputs are fully compatible with Series 74 TTL. The device requires a single 5-volt power supply. The TMS 4042 series is manufactured using TI's reliable N-channel enhancement-type silicon-gate technology to optimize the cost/performance relationship. Readout is nondestructive and output data is not inverted from data in.

The TMS 4042 series is offered in 18-pin dual-in-line ceramic (JL suffix) and plastic (NL suffix) packages designed for insertion in mounting-hole rows on 300-mil centers. The series is characterized for operation from 0°C to 70°C.

operation

addresses (A0-A7)

The eight address inputs select one of 256 4-bit words. The address inputs can be driven directly from standard Series 54/74 TTL with no external pull-up resistors.

chip enable 1 and chip enable 2 ($\overline{CE}$1 and $\overline{CE}$2)

To enable the device, $\overline{CE}$1 and $\overline{CE}$2 must be low. The two chip-enable terminals can be driven from a common source or either terminal can be hard wired low. When the memory is disabled, data cannot be entered and the outputs are in the high-impedance state.

PRELIMINARY DATA SHEET:
Supplementary data may be published at a later date.

operation (continued)

read/write (R/$\overline{\text{W}}$)

The R/$\overline{\text{W}}$ input must be high during read and low during write operations. Prior to an address change, R/$\overline{\text{W}}$ must be in the read state and must remain in that state for a minimum period to eliminate the possibility of data being written into an unwanted position. The R/$\overline{\text{W}}$ input is TTL-compatible and does not require external resistors.

output enable ($\overline{\text{OE}}$)

The output enable must be low to read for when it is high the outputs are in the high-impedance state.

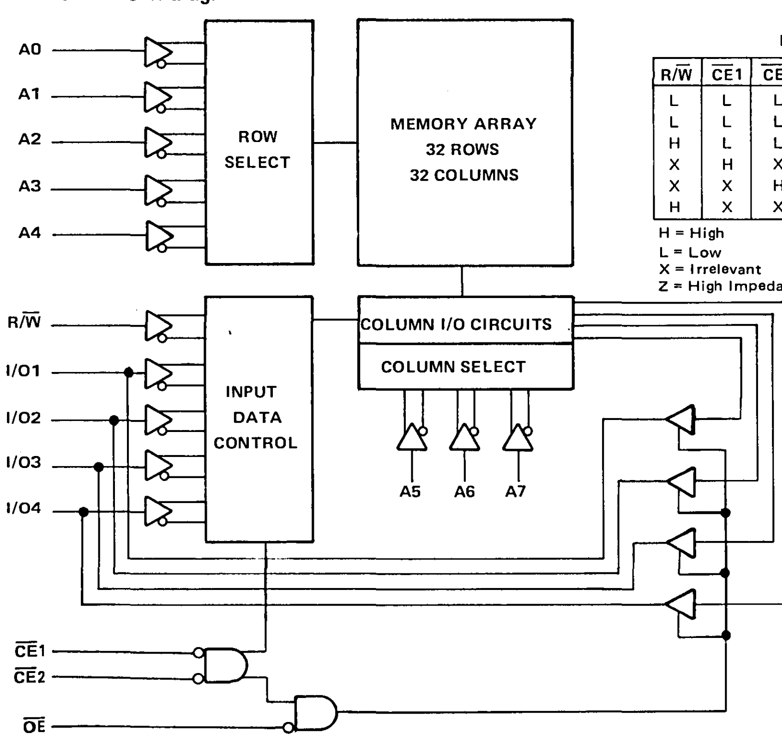
input/output (I/O1-I/O4)

The common input/output terminals are used for both read and write operations. During a write cycle, data must be set up a minimum time before R/$\overline{\text{W}}$ goes to the read state (high) to ensure that correct data will enter the addressed memory cell. Also, input data must be held valid a minimum time after the rise of R/$\overline{\text{W}}$.

3

The output buffers are three-state and are controlled by $\overline{\text{OE}}$, $\overline{\text{CE1}}$, and $\overline{\text{CE2}}$. The input buffers are controlled by R/$\overline{\text{W}}$, $\overline{\text{CE1}}$, and $\overline{\text{CE2}}$. To read data, $\overline{\text{CE1}}$, $\overline{\text{CE2}}$, and $\overline{\text{OE}}$ must be low. If any one of these three inputs goes to the high level, the output terminals are forced to the high-impedance state. The common I/O terminals can be driven directly by Series 74 TTL and the buffers can drive Series 74 TTL circuits without external resistors.

functional block diagram



FUNCTION TABLE

R/$\overline{\text{W}}$	$\overline{\text{CE1}}$	$\overline{\text{CE2}}$	$\overline{\text{OE}}$	OPERATION
L	L	L	L	Not recommended
L	L	L	H	Write (I/O = Z)
H	L	L	L	Read
X	H	X	X	Device Disabled (I/O = Z)
X	X	H	X	Device Disabled (I/O = Z)
H	X	X	H	Device Disabled (I/O = Z)

H = High
L = Low
X = Irrelevant
Z = High Impedance

575

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{CC} (see Note 1)	−0.5 to 7 V
Input voltage (any input) (see Note 1)	−0.5 to 7 V
Continuous power dissipation	1 W
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: Voltage values are with respect to the ground terminal.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

PARAMETER	TMS 4042 MIN	TMS 4042 NOM	TMS 4042 MAX	TMS 4042-1 MIN	TMS 4042-1 NOM	TMS 4042-1 MAX	TMS 4042-2 MIN	TMS 4042-2 NOM	TMS 4042-2 MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	V
High-level input voltage, V_{IH}	2.2		V_{CC}	2.2		V_{CC}	2.2		V_{CC}	V
Low-level input voltage, V_{IL} (see Note 2)	−0.5		0.65	−0.5		0.65	−0.5		0.65	V
Read cycle time, $t_{c(rd)}$	1000			650			450			ns
Write cycle time, $t_{c(wr)}$	1000			650			450			ns
Write pulse width, $t_{w(wr)}$	800			450			300			ns
Address setup time, $t_{su(ad)}$	150			150			100			ns
Chip enable setup time, $t_{su(\overline{CE})}$	900			550			400			ns
Data setup time, $t_{su(da)}$	700			400			280			ns
Address hold time, $t_{h(ad)}$	50			50			50			ns
Data hold time, $t_{h(da)}$	100			100			100			ns
Operating free-air temperature, T_A	0		70	0		70	0		70	°C

NOTE 2: The algebraic convention where the most negative limit is designated as minimum is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -150\ \mu A$,	$V_{CC} = 4.75$ V	2.2			V
V_{OL}	Low-level output voltage	$I_{OL} = 2$ mA,	$V_{CC} = 5.25$ V			0.45	V
I_I	Input current	$V_I = 0$ to 5.25 V				±10	μA
I_{OZH}	Off-state output current, high-level voltage applied	$\overline{CE}$ at 2.2 V,	$V_O = 4$ V			15	μA
I_{OZL}	Off-state output current, low-level voltage applied	$\overline{CE}$ at 2.2 V,	$V_O = 0.45$ V			−50	μA
I_{CC}	Supply current from V_{CC}	$V_{CC} = 5.25$ V, $I_O = 0$ mA	$T_A = 25°C$			60	mA
			$T_A = 0°C$			70	mA
C_i	Input capacitance	$V_I = 0$ V, f = 1 MHz	$T_A = 25°C$,		4	8	pF
C_o	Output capacitance	$V_O = 0$ V, f = 1 MHz	$T_A = 25°C$,		10	15	pF

†All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

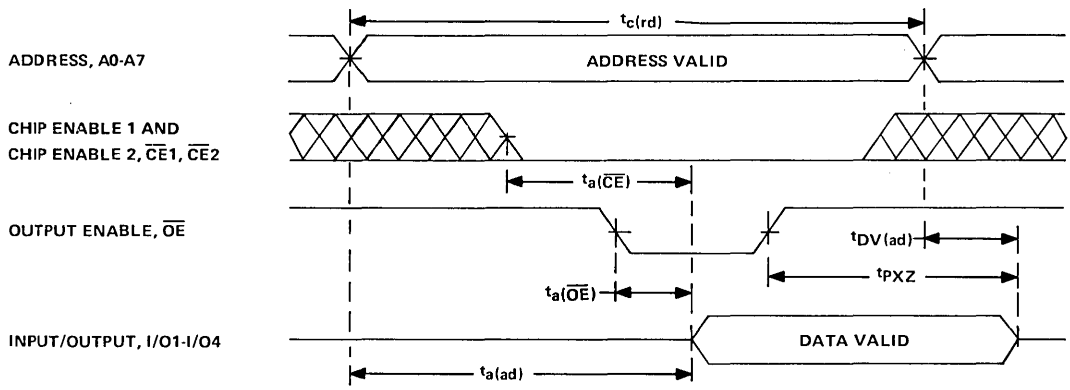
3

switching characteristics over recommended supply voltage range, T_A = 0°C to 70°C, 1 Series 74 TTL load, C_L = 100 pF

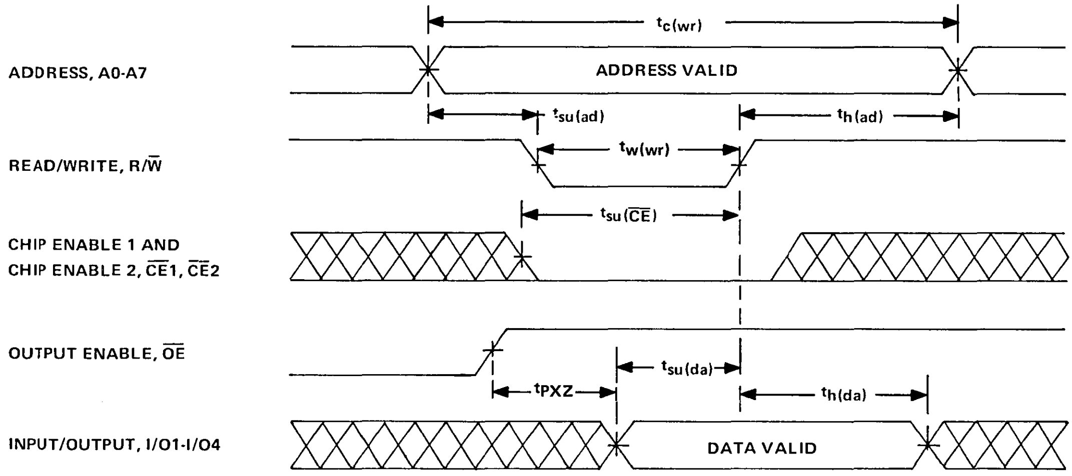
PARAMETER		TMS 4042		TMS 4042-1		TMS 4042-2		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(ad)}$	Access time from address		1000		650		450	ns
$t_{a(\overline{CE})}$	Access time from chip enable $\overline{CE}1$ or $\overline{CE}2$		800		400		350	ns
$t_{a(\overline{OE})}$	Access time from output enable		700		350		300	ns
$t_{DV(ad)}$	Previous output data valid after address change	40		40		40		ns
t_{PXZ}	Output disable time from output enable (see Note 3)	0	200	0	150	0	150	ns

NOTE 3: This parameter defines the delay for the I/O bus to enter the input mode.

read cycle timing



write cycle timing



NOTE: For measuring timing requirements and characteristics, V_{IH} = 2.2 V, V_{IL} = 0.65 V, $t_r = t_f$ = 20 ns and all timing points are 50% points.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TMS 4043 JL, NL; TMS 4043-1 JL, NL; TMS 4043-2 JL, NL
256-WORD BY 4-BIT STATIC RANDOM-ACCESS MEMORIES

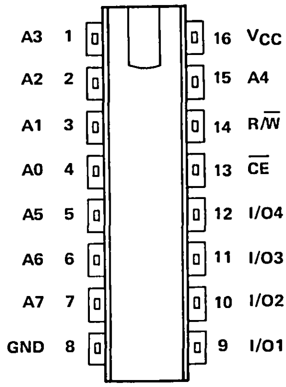
BULLETIN NO. DL-S 7512270, MAY 1975

- 256 x 4 Organization
- Common I/O
- 16-Pin Package
- Static Operation (No Clocks, No Refresh)
- 3 Performance Ranges:

	ACCESS TIME (MAX)	READ OR WRITE CYCLE (MIN)
TMS 4043	1000 ns	1000 ns
TMS 4043-1	650 ns	650 ns
TMS 4043-2	450 ns	450 ns

- Input Interface
  - Fully Decoded
  - TTL-Compatible
  - Static Charge Protection
- Output Interface
  - Chip-Enable Input and 3-State Outputs for OR-Tie Capability in Common I/O Data Bus Systems
  - Fan-out to 1 Series 74 TTL Load
- Power Dissipation . . . 175 mW Typical
- Organized for Microprocessor-Based Systems
- TMS 4043 and TMS 4043-1 Are Interchangeable with Intel 2112 and 2112-2, Respectively

16-PIN CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGES
(TOP VIEW)



3

description

This series of static random-access memories is organized as 256 words of 4 bits. Static design results in reduced overhead costs by elimination of refresh-clocking circuitry and by simplification of timing requirements. The use of common input/output terminals, controlled by the chip enable and read/write terminals, allows the use of a 16-pin package and saves board space in comparison to the TMS 4039 or TMS 4042. The common input/outputs are fully compatible with Series 74 TTL. The device requires a single 5-volt power supply. The TMS 4043 series is manufactured using TI's reliable N-channel enhancement-type silicon-gate technology to optimize the cost/performance relationship. Readout is nondestructive and output data is not inverted from data in.

The TMS 4043 series is offered in 16-pin dual-in-line ceramic (JL suffix) and plastic (NL suffix) packages designed for insertion in mounting-hole rows on 300-mil centers. The series is characterized for operation from 0°C to 70°C.

operation

addresses (A0-A7)

The eight address inputs select one of 256 4-bit words. The address inputs can be driven directly from standard Series 54/74 TTL with no external pull-up resistors.

chip enable ($\overline{CE}$)

To enable the device, $\overline{CE}$ must be low. When the memory is disabled, data cannot be entered and the outputs are in the high-impedance state.

PRELIMINARY DATA SHEET:
Supplementary data may be published at a later date.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

operation (continued)

read/write (R/$\overline{W}$)

The R/$\overline{W}$ input must be high during read and low during write operations. Prior to an address change, R/$\overline{W}$ must be in the read state and must remain in that state for a minimum period to eliminate the possibility of data being written into an unwanted position. The R/$\overline{W}$ input is TTL-compatible and does not require external resistors.

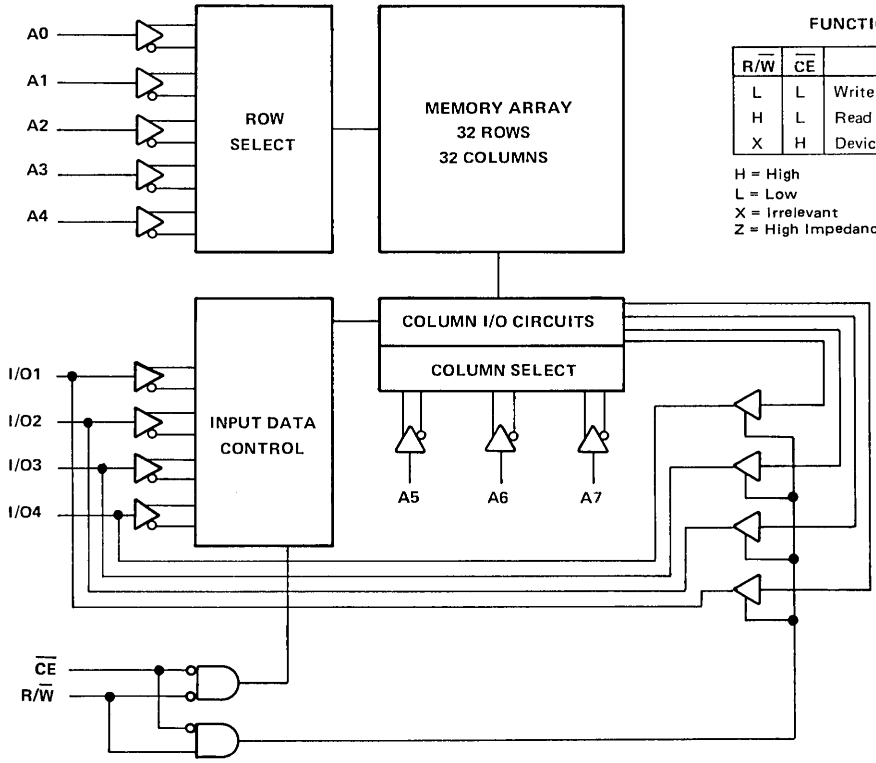
input/output (I/O1-I/O4)

The common input/output terminals are used for both read and write operations. During a write cycle, data must be set up a minimum time before R/$\overline{W}$ goes to the read state (high) to ensure that correct data will enter the addressed memory cell. Also, input data must be held valid a minimum time after the rise of R/$\overline{W}$.

The output buffers are three-state and they are controlled by $\overline{CE}$ and R/$\overline{W}$. If $\overline{CE}$ goes high or R/$\overline{W}$ goes low, the output terminals are forced to the high-impedance state. The input buffers are also controlled by $\overline{CE}$ and R/$\overline{W}$. To read data, $\overline{CE}$ must be low and R/$\overline{W}$ high. The common I/O terminals can be driven directly by Series 74 TTL and the buffers can drive Series 74 TTL circuits without external resistors.

3

functional block diagram



FUNCTION TABLE

R/$\overline{W}$	$\overline{CE}$	OPERATION
L	L	Write (I/O = Z)
H	L	Read
X	H	Device disabled (I/O = Z)

H = High
L = Low
X = Irrelevant
Z = High Impedance

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{CC} (see Note 1)	−0.5 to 7 V
Input voltage (any input) (see Note 1)	−0.5 to 7 V
Continuous power dissipation	1 W
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: Voltage values are with respect to the ground terminal.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

PARAMETER	TMS 4043			TMS 4043-1			TMS 4043-2			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	V
High-level input voltage, V_{IH}	2.2		V_{CC}	2.2		V_{CC}	2.2		V_{CC}	V
Low-level input voltage, V_{IL} (see Note 2)	−0.5		0.65	−0.5		0.65	−0.5		0.65	V
Read cycle time, $t_{c(rd)}$	1000			650			450			ns
Write cycle time, $t_{c(wr)}$	1000			650			450			ns
Address setup time, $t_{su(ad)}$	150			100			50			ns
Chip-enable setup time, $t_{su(\overline{CE})}$	0			0			0			ns
Data setup time, $t_{su(da)}$	600			300			150			ns
Address hold time, $t_{h(ad)}$	50			50			50			ns
Chip-enable hold time, $t_{h(\overline{CE})}$	0			0			0			ns
Data hold time, $t_{h(da)}$	100			50			50			ns
Operating free-air temperature, T_A	0		70	0		70	0		70	°C

NOTE 2: The algebraic convention where the most negative limit is designated as minimum is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −150 µA,	V_{CC} = 4.75 V	2.2			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA,	V_{CC} = 5.25 V			0.45	V
I_I	Input current	V_I = 0 to 5.25 V				±10	µA
I_{OZH}	Off-state output current, high-level voltage applied	$\overline{CE}$ at 2.2 V,	V_O = 4 V			15	µA
I_{OZL}	Off-state output current, low-level voltage applied	$\overline{CE}$ at 2.2 V,	V_O = 0.45 V			−50	µA
I_{CC}	Supply current from V_{CC}	V_{CC} = 5.25 V,	T_A = 25°C			60	mA
		I_O = 0 mA	T_A = 0°C			70	mA
C_i	Input capacitance	V_I = 0 V, f = 1 MHz	T_A = 25°C,		4	8	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		10	15	pF

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

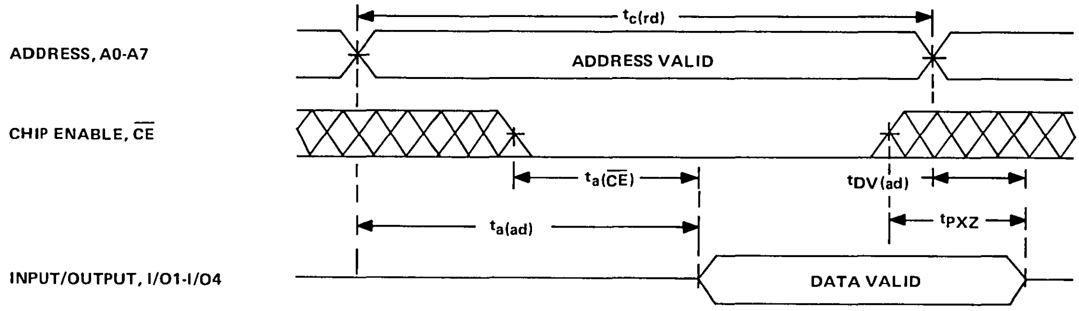
3

switching characteristics over recommended supply voltage range, $T_A = 0°C$ to $70°C$, 1 Series 74 TTL load, $C_L = 100$ pF

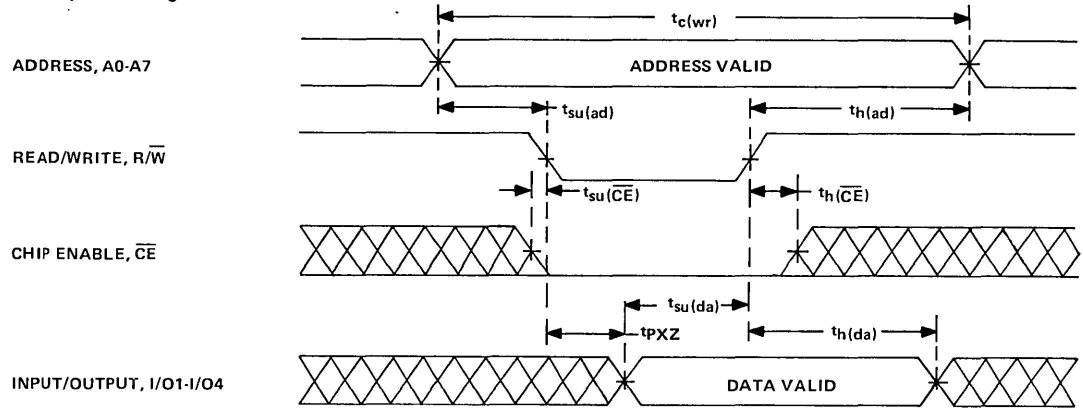
PARAMETER		TMS 4043		TMS 4043-1		TMS 4043-2		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(ad)}$	Access time from address		1000		650		450	ns
$t_{a(\overline{CE})}$	Access time from chip enable		800		500		350	ns
$t_{DV(ad)}$	Previous output data valid after address change	40		40		40		ns
t_{PXZ}	Output disable time from chip enable (see Note 3)	0	200	0	150	0	150	ns
t_{PXZ}	Output disable time from read/write (see Note 3)		200		200		200	ns

NOTE 3: This parameter defines the delay for the I/O bus to enter the input mode.

read cycle timing



write cycle timing



NOTE: For measuring timing requirements and characteristics, $V_{IH} = 2.2$ V, $V_{IL} = 0.65$ V, $t_r = t_f = 20$ ns and all timing points are 50% points.

PRINTED IN U.S.A. 575

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TMS 4050 JL, NL; TMS 4050-1 JL, NL; TMS 4050-2 JL, NL
4096-BIT DYNAMIC RANDOM-ACCESS MEMORIES

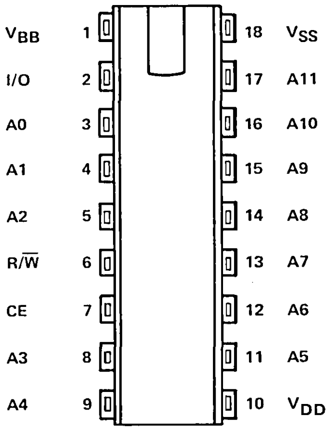
BULLETIN NO. DL-S 7512242, FEBRUARY 1975—REVISED MAY 1975

- 4096 x 1 Organization
- 18-Pin 300-Mil Package Configuration
- Multiplexed Data Input/Output
- 3 Performance Ranges:

	ACCESS TIME (MAX)	READ OR WRITE CYCLE (MIN)	READ, MODIFY WRITE CYCLE (MIN)
TMS 4050	300 ns	470 ns	730 ns
TMS 4050-1	250 ns	430 ns	660 ns
TMS 4050-2	200 ns	400 ns	600 ns

- Full TTL Compatibility on All Inputs (No Pull-up Resistors Needed)
- Registers for Addresses Provided on Chip
- Open-Drain Output Buffer
- Single Low-Capacitance Clock
- Low-Power Dissipation
  - 420 mW Operating (Typical)
  - 0.1 mW Standby (Typical)
- N-Channel Silicon-Gate Technology

18-PIN CERAMIC AND PLASTIC DUAL-IN-LINE PACKAGES (TOP VIEW)



3

description

The TMS 4050 series is composed of high-speed dynamic 4096-bit MOS random-access memories, organized as 4096 one-bit words. N-channel silicon-gate technology is employed to optimize the speed/power/density trade-off. Three performance options are offered: 300 ns access for the TMS 4050, 250 ns access for the TMS 4050-1, and 200 ns for TMS 4050-2. These options allow the system designer to more closely match the memory performance to the capability of the arithmetic processor.

All inputs except the chip enable are fully TTL-compatible and require no pull-up resistors. The input buffers allow a minimum 200 mV noise margin when driven by a series 74 TTL device. The TTL-compatible open-drain buffer is guaranteed to drive 1 series 74 TTL gate. The low capacitance of the address and control inputs precludes the need for specialized drivers. The TMS 4050 series uses only one clock (chip enable) to simplify system design. The low-capacitance chip-enable input requires a positive voltage swing (12 volts), which can be driven by a variety of widely available drivers. The data input and output are multiplexed to facilitate compatibility with a common bus system. A 12 line address is available, which minimizes external control logic and optimizes system performance.

The typical power dissipation of these RAM's is 420 mW active and 0.1 mW standby. To retain data only 6 mW average power is required, which includes the power consumed to refresh the contents of the memory.

The TMS 4050 series is offered in both 18-pin ceramic (JL suffix) and plastic (NL suffix) dual-in-line packages. The series is guaranteed for operation from 0°C to 70°C. Packages are designed for insertion in mounting hole rows on 300-mil centers.

operation

chip enable (CE)

A single external clock input is required. All read, write, and read, modify write operations take place when the chip enable input is high. When the chip enable is low, the memory is in the low-power standby mode and is not selected. No read/write operations can take place during the standby mode because the chip is deselected and is automatically precharging.

operation (continued)

mode select (R/$\overline{W}$)

The read or write mode is selected through the read/write (R/$\overline{W}$) input. A logic high on the R/$\overline{W}$ input selects the read mode and a logic low selects the write mode. The read/write terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected and the data output is disabled when the write mode is selected.

address (A0–A11)

All addresses must be stable on or before the rising edge of the chip-enable pulse. All address inputs can be driven from standard TTL circuits without pull-up resistors. Address registers are provided on chip to reduce overhead and simplify system design.

data input/output (I/O)

Data input and output are multiplexed on a common input/output terminal, which is controlled by the R/$\overline{W}$ input. Data is written during a write or read, modify write cycle while the chip enable is high. The I/O terminal requires connection to an external pull-up resistor since the output buffer has an open-drain configuration. The open-drain output buffer provides direct TTL sink compatibility with a fan-out of one Series 74 TTL gate. A low logic level results from conduction in the open-drain output buffer while a high level occurs with the buffer in its high-impedance state. Data written into the memory is read out in its true form.

3

refresh

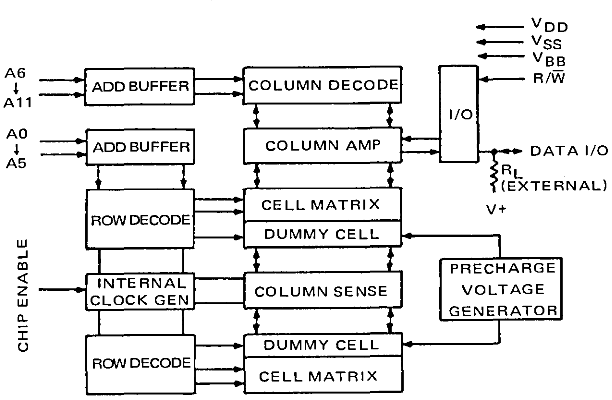
Refresh of the cell matrix is accomplished by performing a memory cycle at each of the 64 row addresses (A0 through A5) every 2 milliseconds or less. Addressing any row refreshes all 64 bits in that row. The column addresses (A6 through A11) can be indeterminate during refresh.

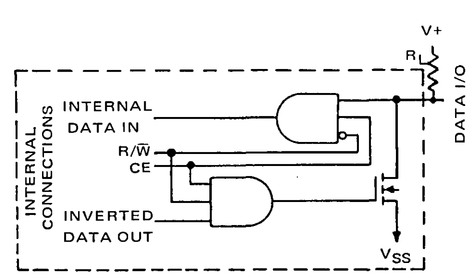
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1)	–0.3 to 20 V
Supply voltage, V_{SS} (see Note 1)	–0.3 to 20 V
All input voltages (see Note 1)	–0.3 to 20 V
Chip-enable voltage (see Note 1)	–0.3 to 20 V
Output voltage (operating, with respect to V_{SS})	–2 to 7 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	–55°C to 150°C

NOTE: 1. Under absolute maximum ratings, voltage values are with respect to the most-negative supply voltage, V_{BB} (substrate), unless otherwise noted. Throughout the remainder of this data sheet, voltage values are with respect to V_{SS}.

functional block diagram





I/O LOGIC

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	11.4	12	12.6	V
Supply voltage, V_{SS}		0		V
Supply voltage, V_{BB}	–4.5	–5	–5.5	V
High-level input voltage, V_{IH} (all inputs except chip enable)	2.2		5.5	V
High-level chip enable input voltage, $V_{IH(CE)}$	V_{DD} –0.6		V_{DD}+1	V
Low-level input voltage, V_{IL} (all inputs except chip enable) (see Note 2)	–0.6		0.6	V
Low-level chip enable input voltage, $V_{IL(CE)}$ (see Note 2)	–1		0.6	V
Refresh time, $t_{refresh}$			2	ms
Operating free-air temperature, T_A	0		70	°C

NOTE 2: The algebraic convention where the most negative limit is designated as minimum is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions, T_A = 0°C to 70°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	t_a = guaranteed maximum access time, R_L = 2.2 kΩ to 5.5 V, C_L = 50 pF, Load = 1 Series 74 TTL gate		2.4			V
V_{OL}	Low-level output voltage			V_{SS}		0.4	V
I_{OL}	Low-level output current	t_a = guaranteed maximum access time, C_L = 50 pF, V_{OL} = 0.4 V		5			mA
I_I	Input current (all inputs including I/O except chip enable)	V_I = –0.6 to 5.5 V				10	µA
$I_{I(CE)}$	Chip enable input current	V_I = –1 to 13.2 V				10	µA
I_{DD}	Supply current from V_{DD}	$V_{IH(CE)}$ = 13.2 V	TMS4050		35	60	mA
			TMS4050-1				
			TMS4050-2		35	70	
I_{DD}	Supply current from V_{DD}, standby	$V_{IL(CE)}$ = 0.6 V			10	200	µA
$I_{DD(av)}$	Average supply current from V_{DD} during read or write cycle	Minimum cycle timing	TMS 4050		32		mA
			TMS 4050-1		35		
			TMS 4050-2		38		
$I_{DD(av)}$	Average supply current from V_{DD} during read, modify write cycle		TMS 4050		32		mA
			TMS 4050-1		35		
			TMS 4050-2		38		
I_{BB}	Supply current from V_{BB}	V_{BB} = –5.5 V, V_{DD} = 12.6 V, V_{SS} = 0 V			5	100	µA

†All typical values are at T_A = 25°C.

capacitance at V_{DD} = 12 V, V_{SS} = 0 V, V_{BB} = –5 V, $V_{I(CE)}$ = 0 V, V_I = 0 V, f = 1 MHz, T_A = 0°C to 70°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$C_{i(ad)}$	Input capacitance address inputs			5	7	pF
$C_{i(CE)}$	Input capacitance clock input	$V_{I(CE)}$ = 12 V		24	28	pF
		$V_{I(CE)}$ = 0 V		29	33	
$C_{i(R/\overline{W})}$	Input capacitance read/write input			5	7	pF
$C_{(I/O)}$	I/O terminal capacitance			7	9	pF

†All typical values are at T_A = 25°C.

3

read cycle timing requirements over recommended supply voltage range, T_A = 0°C to 70°C

PARAMETER		TMS 4050		TMS 4050-1		TMS 4050-2		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time	470		430		400		ns
$t_{w(CEH)}$	Pulse width, chip enable high	300	4000	260	4000	230	4000	ns
$t_{w(CEL)}$	Pulse width, chip enable low	130		130		130		ns
$t_{r(CE)}$	Chip-enable rise time		40		40		40	ns
$t_{f(CE)}$	Chip-enable fall time		40		40		40	ns
$t_{su(ad)}$	Address setup time	0↑		0↑		0↑		ns
$t_{su(rd)}$	Read setup time	0↑		0↑		0↑		ns
$t_{h(ad)}$	Address hold time	150↑		150↑		150↑		ns
$t_{h(rd)}$	Read hold time	40↓		40↓		40↓		ns

↑↓ The arrow indicates the edge of the chip-enable pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

read cycle switching characteristics over recommended supply voltage range, T_A = 0°C to 70°C

PARAMETER		TMS 4050		TMS 4050-1		TMS 4050-2		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(CE)}$	Access time from chip enable*		280		230		180	ns
$t_{a(ad)}$	Access time from addresses†		300		250		200	ns
t_{PLH}	Propagation delay time, low-to-high level output from chip enable*	40		40		40		ns

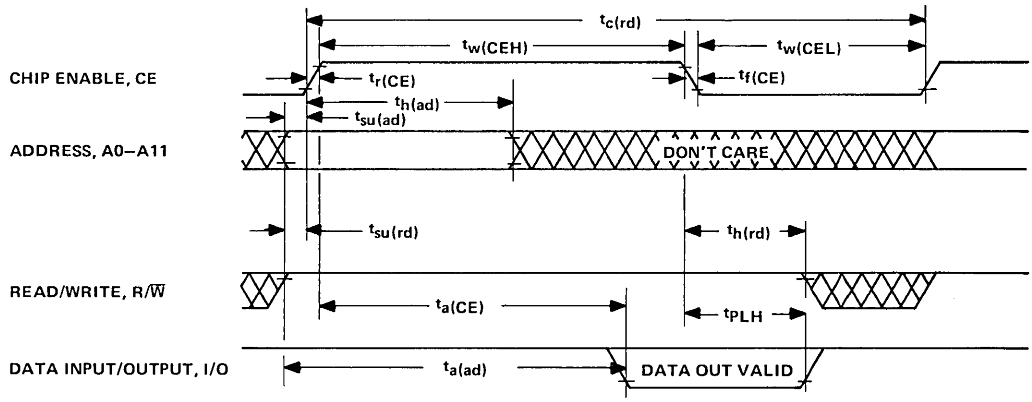
*Test conditions: C_L = 50 pF, R_L = 2.2 kΩ to 5.5 V, Load = 1 Series 74 TTL gate.
†Test conditions: C_L = 50 pF, R_L = 2.2 kΩ to 5.5 V, Load = 1 Series 74 TTL gate, $t_{r(CE)}$ = 20 ns.

write cycle timing requirements over recommended supply voltage range, T_A = 0°C to 70°C

PARAMETER		TMS 4050		TMS 4050-1		TMS 4050-2		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(wr)}$	Write cycle time	470		430		400		ns
$t_{w(CEH)}$	Pulse width, chip enable high	300	4000	260	4000	230	4000	ns
$t_{w(CEL)}$	Pulse width, chip enable low	130		130		130		ns
$t_{w(wr)}$	Write pulse width	200		190		180		ns
$t_{r(CE)}$	Chip-enable rise time		40		40		40	ns
$t_{f(CE)}$	Chip-enable fall time		40		40		40	ns
$t_{su(ad)}$	Address setup time	0↑		0↑		0↑		ns
$t_{su(da\text{-}wr)}$	Data-to-write setup time*	0		0		0		ns
$t_{su(wr)}$	Write-pulse setup time	240↓		220↓		210↓		ns
$t_{d(CEH\text{-}wr)}$	Chip-enable-high-to-write delay time†		40↑		40↑		40↑	ns
$t_{h(ad)}$	Address hold time	150↑		150↑		150↑		ns
$t_{h(da)}$	Data hold time	40↓		40↓		40↓		ns

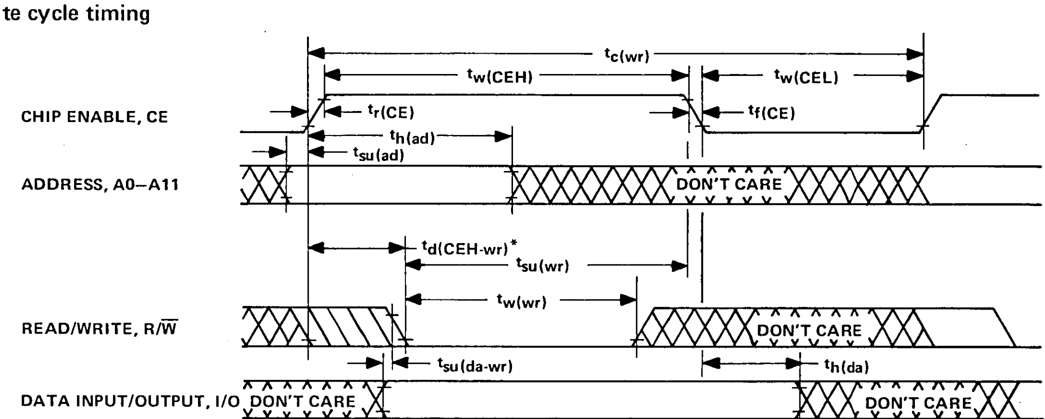
↑↓ The arrow indicates the edge of the chip-enable pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.
*If $R/\overline{W}$ is low before CE goes high, then I/O (data in) must be valid when CE goes high.
†The write pulse must go low at least $t_{su(wr)}$ minimum before CE goes low. If $R/\overline{W}$ remains high more than $t_{d(CEH\text{-}wr)}$ maximum (40 ns) after CE goes high, the data-in driver must be disabled until $R/\overline{W}$ goes low since additional power to overcome the output buffer may be required when writing in a high with some of the faster devices (see comments on Region 1 under read, modify write timing diagram).

read or refresh cycle timing



NOTE: For the chip-enable input, high and low timing points are 3.0 V (high) and 1.0 V (low). Other input timing points are 0.6 V (low) and 2.2 V (high). Output timing points are 0.4 V (low) and 2.4 V (high).
For minimum cycle, $t_{r(\overline{CE})}$ and $t_{f(\overline{CE})}$ are equal to 20 ns.

write cycle timing



NOTE: For the chip-enable input, high and low timing points are 3.0 V (high) and 1.0 V (low). Other timing points are 0.6 V (low) and 2.2 V (high). Output timing points are 0.4 V (low) and 2.4 V (high).
*The write pulse must go low at least $t_{su(wr)}$ minimum before $\overline{CE}$ goes high. If R/$\overline{W}$ remains high more than $t_{d(\overline{CE}L\text{-}wr)}$ maximum (60 ns) after $\overline{CE}$ goes low, the data-in driver must be disabled until R/$\overline{W}$ goes low since additional power to overcome the output buffer may be required when writing in a high with some of the faster devices. During $t_{d(CEH\text{-}wr)}$, R/$\overline{W}$ is permitted to change from high to low only.

read, modify write cycle timing requirements over recommended supply voltage range, $T_A = 0°C$ to $70°C$

PARAMETER		TMS 4050 MIN	TMS 4050 MAX	TMS 4050-1 MIN	TMS 4050-1 MAX	TMS 4050-2 MIN	TMS 4050-2 MAX	UNIT
$t_{c(RMW)}$	Read, modify write cycle time†	730		660		600		ns
$t_{w(CEH)}$	Pulse width, chip enable high†	560	4000	490	4000	430	4000	ns
$t_{w(CEL)}$	Pulse width, chip enable low	130		130		130		ns
$t_{w(wr)}$	Write pulse width	200		190		180		ns
$t_{r(CE)}$	Chip-enable rise time		40		40		40	ns
$t_{f(CE)}$	Chip-enable fall time		40		40		40	ns
$t_{d(wr-daL)}$	Write to data-in-low delay time		20		20		20	ns
$t_{su(ad)}$	Address setup time	0↑		0↑		0↑		ns
$t_{su(daH)}$	Data-in-high setup time	240↓		220↓		210↓		ns
$t_{su(rd)}$	Read-pulse setup time	0↑		0↑		0↑		ns
$t_{su(wr)}$	Write-pulse setup time	240↓		220↓		210↓		ns
$t_{h(ad)}$	Address hold time	150↑		150↑		150↑		ns
$t_{h(rd)}$	Read hold time	300↑		250↑		200↑		ns
$t_{h(da)}$	Data hold time	40↓		40↓		40↓		ns

3

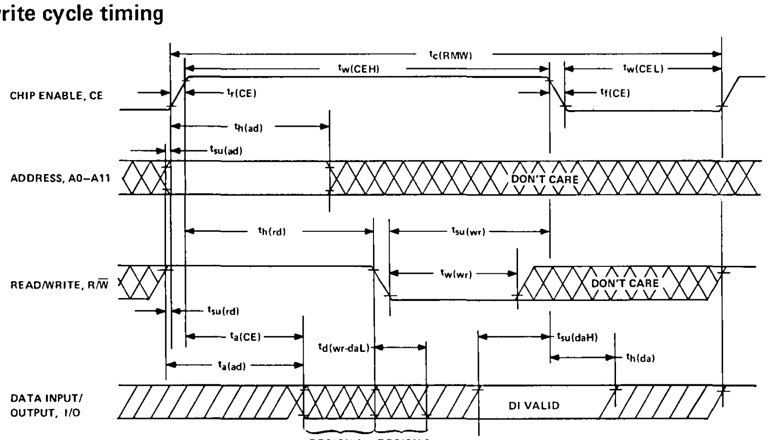
↑↓ The arrow indicates the edge of the chip-enable pulse for reference: ↑ for the rising edge; ↓ for the falling edge.
†Test conditions: $t_{f(rd)} = 20$ ns.

read, modify write cycle switching characteristics over recommended supply voltage range, $T_A = 0°C$ to $70°C$

PARAMETER		TMS 4050 MIN	TMS 4050 MAX	TMS 4050-1 MIN	TMS 4050-1 MAX	TMS 4050-2 MIN	TMS 4050-2 MAX	UNIT
$t_{a(CE)}$	Access time from chip enable*		280		230		180	ns
$t_{a(ad)}$	Access Time from addresses†		300		250		200	ns

*Test conditions: $C_L = 50$ pF, $R_L = 2.2$ kΩ, Load = 1 Series 74 TTL gate.
†Test conditions: $C_L = 50$ pF, $R_L = 2.2$ kΩ, Load = 1 Series 74 TTL gate. $t_{r(CE)} = 20$ ns.

read, modify write cycle timing

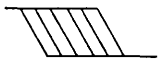
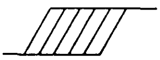
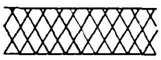
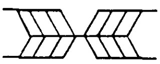


REGION 1 – In region 1, data-out is valid until the I/O terminal is forced high or low by the data-in driver. A transition from low to high is persmissible but additional power to overcome the output buffer will be required. A transition from high to low is permitted without power penalty.

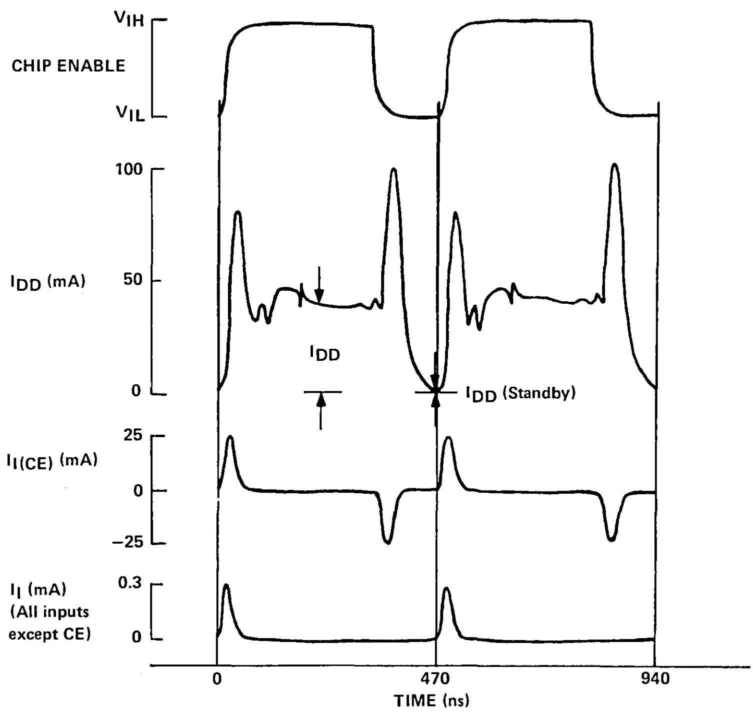
REGION 2 – In region 2 a single transition is permitted. It is NOT a true "Don't Care" region. If a low is to be written it must be valid by the end of region 2.

NOTE: For the chip enable input high and low timing points are 90% and 10% of $V_{IH(CE)}$. Other input timing points are 0.6 V (low) and 2.2 V (high). Output timing points are 0.4 V (low) and 2.4 V (high).
For minimum cycle, $t_{r(CE)}$ and $t_{f(CE)}$ are equal to 20 ns.

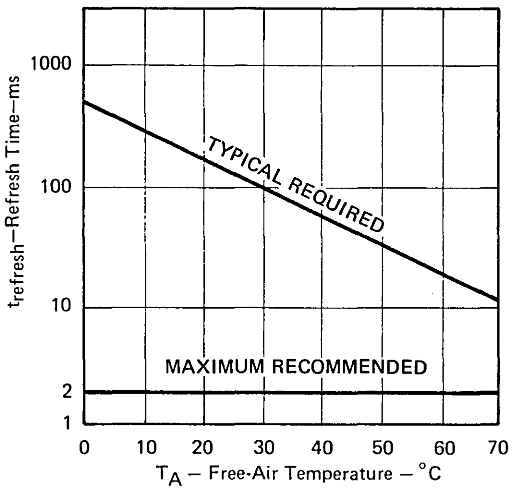
timing diagram conventions

TIMING DIAGRAM SYMBOL	MEANING: INPUT FORCING FUNCTIONS	MEANING: OUTPUT RESPONSE FUNCTIONS
	Must be steady high or low	Will be steady high or low
	High-to-low changes permitted	Will be changing from high to low sometime during designated interval
	Low-to-high changes permitted	Will be changing from low to high sometime during designated interval
	Don't care	State unknown or changing
	(Does not apply)	Center line is high-impedance off-state

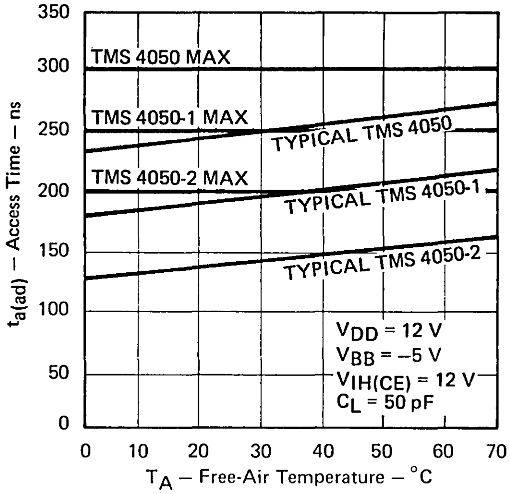
TYPICAL WAVEFORMS



REFRESH TIME vs TEMPERATURE



ACCESS TIMES vs TEMPERATURE



3

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TMS 4051 JL, NL; TMS 4051-1 JL, NL
4096-BIT DYNAMIC RANDOM-ACCESS MEMORIES

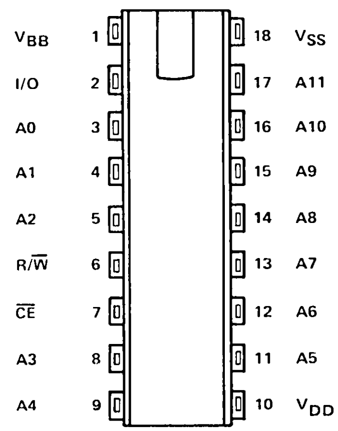
BULLETIN NO. DL-S 7512256, MAY 1975

- 4096 x 1 Organization
- 18-Pin 300-Mil Package Configuration
- Single Low-Capacitance TTL-Compatible Clock
- Multiplexed Data Input/Output
- 2 Performance Ranges:

	ACCESS TIME (MAX)	READ OR WRITE CYCLE (MIN)	READ, MODIFY WRITE CYCLE (MIN)
TMS 4051	300 ns	470 ns	730 ns
TMS 4051-1	250 ns	430 ns	660 ns

- Full TTL Compatibility on All Inputs (No Pull-up Resistors Needed Except with $\overline{CE}$)
- Registers for Addresses Provided on Chip
- Open-Drain Output Buffer
- Low-Power Dissipation
  - 460 mW Operating (Typical)
  - 60 mW Standby (Typical)
- N-Channel Silicon-Gate Technology

18-PIN CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGES
(TOP VIEW)



3

description

The TMS 4051 series is composed of high-speed dynamic 4096-bit MOS random-access memories, organized as 4096 one-bit words. N-channel silicon-gate technology is employed to optimize the speed/power/density trade-off. Two performance options are offered: 300 ns access for the TMS 4051 and 250 ns access for the TMS 4051-1. These options allow the system designer to more closely match the memory performance to the capability of the arithmetic processor.

The address, data input/output, and read/write inputs can be driven directly from Series 74 TTL circuits. A 200-mV noise margin is guaranteed in this configuration, which eliminates the need for specialized drivers. The chip-enable input is TTL-compatible and can interface with a Series 74 TTL circuit as long as a pull-up resistor to V_{CC} is employed in order to provide a high-level input voltage of 3 V minimum. The data input and output are multiplexed to facilitate compatibility with a common bus system. A 12-line address is available, which minimizes external control logic and optimizes system performance.

The typical power dissipation of these RAM's is 460 mW active and 60 mW standby. To retain data only 70 mW average power is required, which includes the power consumed to refresh the contents of the memory.

The TMS 4051 series is offered in both 18-pin ceramic (JL suffix) and plastic (NL suffix) dual-in-line packages. The series is guaranteed for operation from 0°C to 70°C. Packages are designed for insertion in mounting-hole rows on 300-mil centers.

operation

chip enable ($\overline{CE}$)

A single external clock input is required. All read, write, and read, modify write operations take place when the chip enable input is low. When the chip enable is high, the memory is in the low-power standby mode and is not selected. No read/write operations can take place during the standby mode because the chip is deselected and is automatically precharging. The $\overline{CE}$ input can be driven by a standard TTL circuit with a pull-up resistor.

PRELIMINARY DATA SHEET: Supplementary data may be published at a later date.

operation (continued)

mode select (R/$\overline{W}$)

The read or write mode is selected through the read/write (R/$\overline{W}$) input. A logic high on the R/$\overline{W}$ input selects the read mode and a logic low selects the write mode. The read/write terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected and the data output is disabled when the write mode is selected.

address (A0–A11)

All addresses must be stable on or before the falling edge of the chip-enable pulse. All address inputs can be driven from standard TTL circuits without pull-up resistors. Address registers are provided on chip to reduce overhead and simplify system design.

data input/output (I/O)

Data input and output are multiplexed on a common input/output terminal, which is controlled by the R/$\overline{W}$ input. Data is written during a write or read, modify write cycle while the chip enable is low. The I/O terminal requires connection to an external pull-up resistor since the output buffer has an open-drain configuration. The open-drain output buffer provides direct TTL sink compatibility with a fan-out of one Series 74 TTL gate. A low logic level results from conduction in the open-drain output buffer while a high level occurs with the buffer in its high-impedance state. Data written into the memory is read out in its true form.

refresh

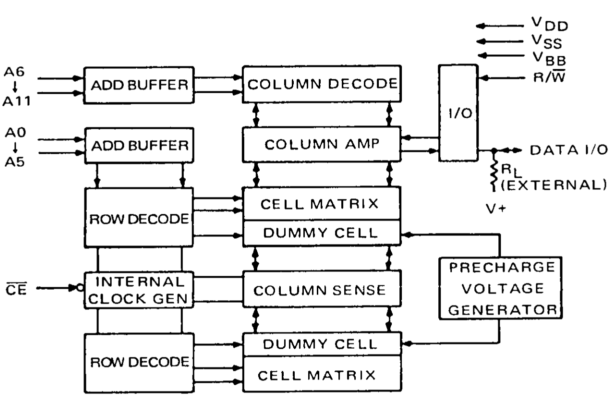
Refresh of the cell matrix is accomplished by performing a memory cycle at each of the 64 row addresses (A0 through A5) every 2 milliseconds or less. Addressing any row refreshes all 64 bits in that row. The column addresses (A6 through A11) can be indeterminate during refresh.

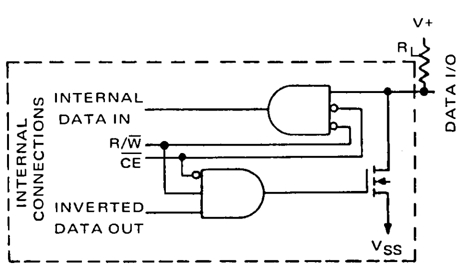
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1)	−0.3 to 20 V
Supply voltage, V_{SS} (see Note 1)	−0.3 to 20 V
All input voltages (see Note 1)	−0.3 to 20 V
Chip-enable voltage (see Note 1)	−0.3 to 20 V
Output voltage (operating, with respect to V_{SS})	−2 to 7 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−55°C to 150°C

NOTE: 1. Under absolute maximum ratings, voltage values are with respect to the most-negative supply voltage, V_{BB} (substrate), unless otherwise noted. Throughout the remainder of this data sheet, voltage values are with respect to V_{SS}.

functional block diagram





I/O LOGIC

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

3

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	11.4	12	12.6	V
Supply voltage, V_{SS}		0		V
Supply voltage, V_{BB}	−4.5	−5	−5.5	V
High-level input voltage, V_{IH} (all inputs except chip enable)	2.2		5.5	V
High-level chip enable input voltage, $V_{IH(\overline{CE})}$	3		5.5	V
Low-level input voltage, V_{IL} (all inputs except chip enable) (see Note 2)	−0.6		0.6	V
Low-level chip enable input voltage, $V_{IL(\overline{CE})}$ (see Note 2)	−0.6		0.6	V
Refresh time, $t_{refresh}$			2	ms
Operating free-air temperature, T_A	0		70	°C

NOTE 2: The algebraic convention where the most negative limit is designated as minimum is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions, T_A = 0°C to 70°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	t_a = guaranteed maximum access time, R_L = 2.2 kΩ to 5.5 V, C_L = 50 pF, Load = 1 Series 74 TTL gate		2.4			V
V_{OL}	Low-level output voltage			V_{SS}		0.4	V
I_{OL}	Low-level output current	t_a = guaranteed maximum access time, C_L = 50 pF, V_{OL} = 0.4 V		5			mA
I_I	Input current (all inputs including I/O except chip enable)	V_I = −0.6 to 5.5 V				10	μA
$I_{I(\overline{CE})}$	Chip enable input current	V_I = −0.6 to 5.5 V				10	μA
I_{DD}	Supply current from V_{DD}	$V_{IL(\overline{CE})}$ = 0.6 V			37	70	mA
I_{DD}	Supply current from V_{DD}, standby	$V_{IH(\overline{CE})}$ = 3.5 V			5	8	mA
$I_{DD(av)}$	Average supply current from V_{DD} during read or write cycle	Minimum cycle timing	TMS 4051		45		mA
			TMS 4051-1		47		
$I_{DD(av)}$	Average supply current from V_{DD} during read, modify write cycle		TMS 4051		50		mA
			TMS 4051-1		54		
I_{BB}	Supply current from V_{BB}	V_{BB} = −5.5 V, V_{DD} = 12.6 V, V_{SS} = 0 V			5	100	μA

†All typical values are at T_A = 25°C.

capacitance at V_{DD} = 12 V, V_{SS} = 0 V, V_{BB} = −5 V, $V_{I(\overline{CE})}$ = 0 V, V_I = 0 V, f = 1 MHz, T_A = 0°C to 70°C (unless otherwise noted)

	PARAMETER	MIN	TYP†	MAX	UNIT
$C_{i(ad)}$	Input capacitance address inputs		5	7	pF
$C_{i(\overline{CE})}$	Input capacitance clock input		5	7	pF
$C_{i(R/\overline{W})}$	Input capacitance read/write input		5	7	pF
$C_{(I/O)}$	I/O terminal capacitance		7	9	pF

†All typical values are at T_A = 25°C.

read cycle timing requirements over recommended supply voltage range, T_A = 0°C to 70°C

PARAMETER		TMS 4051		TMS 4051-1		UNIT
		MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time	470		430		ns
$t_{w(\overline{CE}H)}$	Pulse width, chip enable high	130		130		ns
$t_{w(\overline{CE}L)}$	Pulse width, chip enable low	300	4000	260	4000	ns
$t_{r(\overline{CE})}$	Chip-enable rise time		40		40	ns
$t_{f(\overline{CE})}$	Chip-enable fall time		40		40	ns
$t_{su(ad)}$	Address setup time	0↓		0↓		ns
$t_{su(rd)}$	Read setup time	0↓		0↓		ns
$t_{h(ad)}$	Address hold time	180↓		165↓		ns
$t_{h(rd)}$	Read hold time	80↑		80↑		

↑↓The arrow indicates the edge of the chip-enable pulse used for reference: ↑for the rising edge, ↓for the falling edge.

3

read cycle switching characteristics over recommended supply voltage range, T_A = 0°C to 70°C

PARAMETER		TMS 4051		TMS 4051-1		UNIT
		TYP†	MAX	TYP†	MAX	
$t_{a(\overline{CE})}$	Access time from chip enable‡		280		230	ns
$t_{a(ad)}$	Access time from addresses*		300		250	ns
t_{PLH}	Propagation delay time, low-to-high level output from chip enable‡	60		60		ns

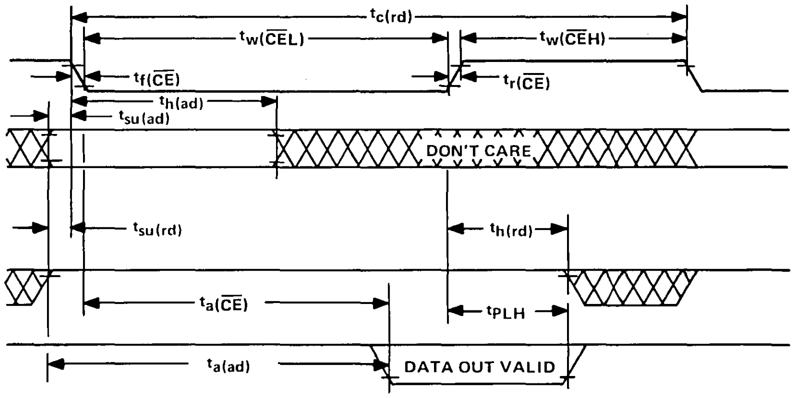
†All typical values are at T_A = 25°C.
‡Test conditions: C_L = 50 pF, R_L = 2.2 kΩ to 5.5 V, Load = 1 Series 74 TTL gate.
*Test conditions: C_L = 50 pF, R_L = 2.2 kΩ to 5.5 V, Load = 1 Series 74 TTL gate, $t_{f(\overline{CE})}$ = 20 ns.

write cycle timing requirements over recommended supply voltage range, T_A = 0°C to 70°C

PARAMETER		TMS 4051		TMS 4051-1		UNIT
		MIN	MAX	MIN	MAX	
$t_{c(wr)}$	Write cycle time	470		430		ns
$t_{w(\overline{CE}H)}$	Pulse width, chip enable high	130		130		ns
$t_{w(\overline{CE}L)}$	Pulse width, chip enable low	300	4000	260	4000	ns
$t_{w(wr)}$	Write pulse width	200		190		ns
$t_{r(\overline{CE})}$	Chip-enable rise time		40		40	ns
$t_{f(\overline{CE})}$	Chip-enable fall time		40		40	ns
$t_{su(ad)}$	Address setup time	0↓		0↓		ns
$t_{su(da\text{-}wr)}$	Data-to-write setup time*	0		0		ns
$t_{su(wr)}$	Write-pulse setup time	240↑		220↑		ns
$t_{d(\overline{CE}L\text{-}wr)}$	Chip-enable-low-to-write delay time†		60↓		60↓	ns
$t_{h(ad)}$	Address hold time	180↓		165↓		ns
$t_{h(da)}$	Data hold time	80↑		80↑		ns

↑↓The arrow indicates the edge of the chip-enable pulse used for reference: ↑for the rising edge, ↓for the falling edge.
*If R/$\overline{W}$ is low before $\overline{CE}$ goes low, then I/O (data in) must be valid when $\overline{CE}$ goes low.
†The write pulse must go low at least $t_{su(wr)}$ minimum before $\overline{CE}$ goes high. If R/$\overline{W}$ remains high more than $t_{d(\overline{CE}L\text{-}wr)}$ maximum (60 ns) after $\overline{CE}$ goes low, the data-in driver must be disabled until R/$\overline{W}$ goes low since additional power to overcome the output buffer may be required when writing in a high with some of the faster devices (see comments on Region 1 under read, modify write timing diagram).

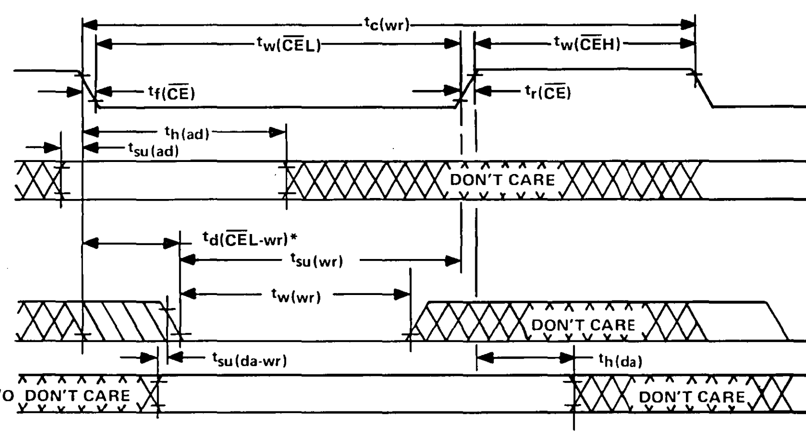
read or refresh cycle timing



NOTE: For the chip-enable input, high and low timing points are 3.0 V (high) and 1.0 V (low). Other input timing points are 0.6 V (low) and 2.2 V (high). Output timing points are 0.4 V (low) and 2.4 V (high).
For minimum cycle, $t_{r(\overline{CE})}$ and $t_{f(\overline{CE})}$ are equal to 20 ns.

3

write cycle timing



NOTE: For the chip-enable input, high and low timing points are 3.0 V (high) and 1.0 V (low). Other timing points are 0.6 V (low) and 2.2 V (high). Output timing points are 0.4 V (low) and 2.4 V (high).
*The write pulse must go low at least $t_{su(wr)}$ minimum before $\overline{CE}$ goes high. If R/$\overline{W}$ remains high more than $t_{d(\overline{CE}L\text{-}wr)}$ maximum (60 ns) after $\overline{CE}$ goes low, the data-in driver must be disabled until R/$\overline{W}$ goes low since additional power to overcome the output buffer may be required when writing in a high with some of the faster devices. During $t_{d(\overline{CE}L\text{-}wr)}$, R/$\overline{W}$ is permitted to change from high to low only.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

read, modify write cycle timing requirements over recommended supply voltage range, T_A = 0°C to 70°C

PARAMETER		TMS 4051		TMS 4051-1		UNIT
		MIN	MAX	MIN	MAX	
$t_{c(RMW)}$	Read, modify write cycle time†	730		660		ns
$t_{w(\overline{CE}H)}$	Pulse width, chip enable high†	130		130		ns
$t_{w(\overline{CE}L)}$	Pulse width, chip enable low	560	4000	490	4000	ns
$t_{w(wr)}$	Write pulse width	200		190		ns
$t_{r(\overline{CE})}$	Chip-enable rise time		40		40	ns
$t_{f(\overline{CE})}$	Chip-enable fall time		40		40	ns
$t_{d(wr\text{-}daL)}$	Write to data-in-low delay time		20		20	ns
$t_{su(ad)}$	Address setup time	0↓		0↓		ns
$t_{su(daH)}$	Data-in-high setup time	240↑		220↑		ns
$t_{su(rd)}$	Read-pulse setup time	0↓		0↓		ns
$t_{su(wr)}$	Write-pulse setup time	240↑		220↑		ns
$t_{h(ad)}$	Address hold time	180↓		165↓		ns
$t_{h(rd)}$	Read hold time	320↓		270↓		ns
$t_{h(da)}$	Data hold time	80↑		80↑		ns

↑↓The arrow indicates the edge of the chip-enable pulse for reference: ↑for the rising edge; ↓for the falling edge.
†Test conditions: $t_{f(rd)}$ = 20 ns.

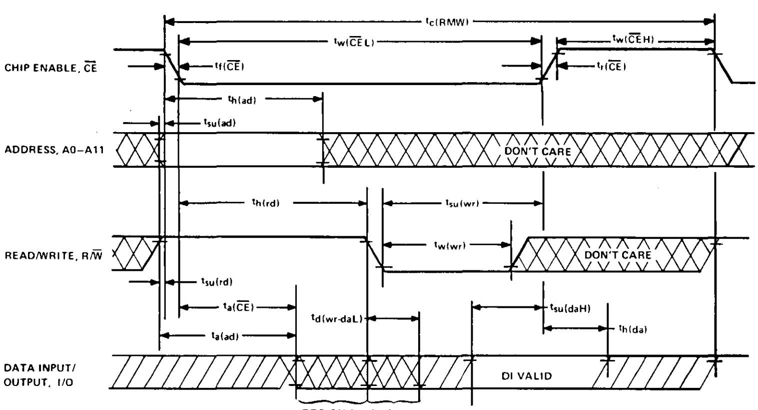
3

read, modify write cycle swithcing characteristics over recommended supply voltage range, T_A = 0°C to 70°C

PARAMETER		TMS 4051		TMS 4051-1		UNIT
		MIN	MAX	MIN	MAX	
$t_{a(\overline{CE})}$	Access time from chip enable*		280		230	ns
$t_{a(ad)}$	Access time from addresses†		300		250	ns

*Test conditions: C_L = 50 pF, R_L = 2.2 kΩ, Load = 1 Series 74 TTL gate.
†Test conditions: C_L = 50 pF, R_L = 2 2 kΩ, Load = 1 Series 74 TTL gate. $t_{f(\overline{CE})}$ = 20 ns.

read, modify write cycle timing



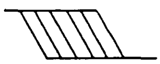
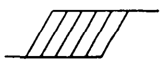
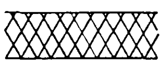
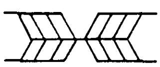
REGION 1 – In region 1, data-out is valid until the I/O terminal is forced high or low by the data-in driver. A transition from low to high is permissible but additional power to overcome the output buffer will be required. A transition from high to low is permitted without power penalty.

REGION 2 – In region 2 a single transition is permitted. It is NOT a true "Don't Care" region. If a low is to be written it must be valid by the end of region 2.

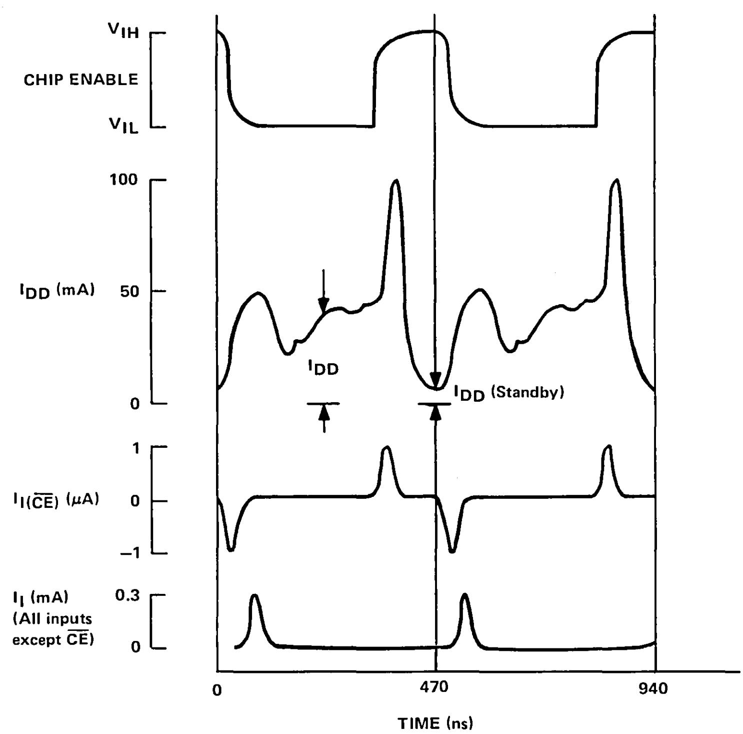
NOTE: For the chip enable input high and low timing points are 3.0 V (high) and 1.0 V (low). Other input timing points are 0.6 V (low) and 2.2 V (high). Output timing points are 0.4 V (low) and 2.4 V (high).
For minimum cycle, $t_{r(\overline{CE})}$ and $t_{f(\overline{CE})}$ are equal to 20 ns.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

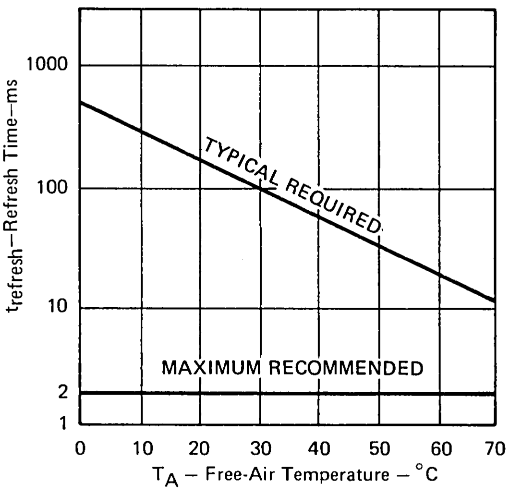
timing diagram conventions

TIMING DIAGRAM SYMBOL	MEANING: INPUT FORCING FUNCTIONS	MEANING: OUTPUT RESPONSE FUNCTIONS
	Must be steady high or low	Will be steady high or low
	High-to-low changes permitted	Will be changing from high to low sometime during designated interval
	Low-to-high changes permitted	Will be changing from low to high sometime during designated interval
	Don't Care	State unknown or changing
	(Does not apply)	Center line is high-impedance off-state

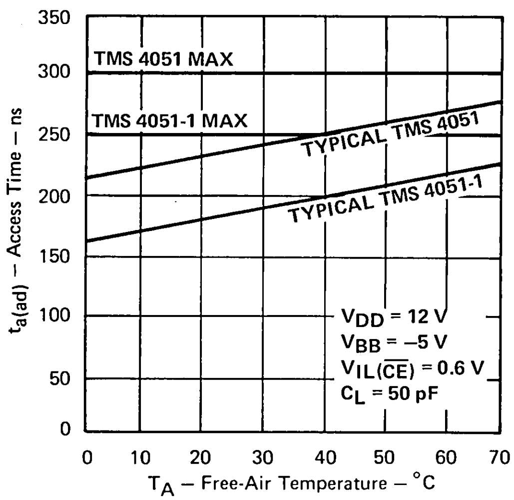
TYPICAL WAVEFORMS



REFRESH TIME vs TEMPERATURE



ACCESS TIMES vs TEMPERATURE



3

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TMS 4060 JL, NL; TMS 4060-1 JL, NL; TMS 4060-2 JL, NL
4096-BIT DYNAMIC RANDOM-ACCESS MEMORIES

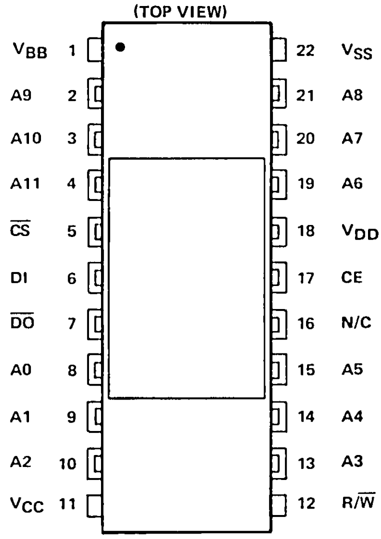
BULLETIN NO. DL-S 7512241, FEBRUARY 1975

- 4096 x 1 Organization
- 3 Performance Ranges:

	ACCESS TIME (MAX)	READ OR WRITE CYCLE (MIN)	READ, MODIFY WRITE CYCLE (MIN)
TMS 4060	300 ns	470 ns	710 ns
TMS 4060-1	250 ns	430 ns	640 ns
TMS 4060-2	200 ns	400 ns	580 ns

- Full TTL Compatibility on All Inputs (No Pull-up Resistors Needed)
- Low Power Dissipation
  - 400 mW Operating (Typical)
  - 0.2 mW Standby (Typical)
- Single Low-Capacitance Clock
- N-Channel Silicon-Gate Technology
- 22-Pin 400-Mil Dual-in-Line Package

22-PIN CERAMIC AND PLASTIC DUAL-IN-LINE PACKAGES (TOP VIEW)



3

description

The TMS 4060 series is composed of high-speed dynamic 4096-bit MOS random-access memories, organized as 4096 one-bit words. N-channel silicon-gate technology is employed to optimize the speed/power/density trade-off. Three performance options are offered: 300 ns access for the TMS 4060, 250 ns access for the TMS 4060-1, and 200 ns for TMS 4060-2. These options allow the system designer to more closely match the memory performance to the capability of the arithmetic processor.

All inputs except the chip enable are fully TTL-compatible and require no pull-up resistors. The low capacitance of the address and control inputs precludes the need for specialized drivers. When driven by a Series 74 device, the guaranteed dc input noise immunity is 200 mV. The TTL-compatible buffer is guaranteed to drive two Series 74 TTL gates. The TMS 4060 series uses only one clock (chip enable) to simplify system design. The low-capacitance chip-enable input requires a positive voltage swing (12 volts), which can be driven by a variety of widely available drivers.

The typical power dissipation of these RAM's is 400 mW active and 0.3 mW standby. To retain data only 6 mW average power is required, which includes the power consumed to refresh the contents of the memory.

The TMS 4060 series is offered in both 22-pin ceramic (JL suffix) and plastic (NL suffix) dual-in-line packages. The series is guaranteed for operation from 0°C to 70°C. These packages are designed for insertion in mounting-hole rows on 0.400-mil centers.

operation

chip select ($\overline{CS}$)

The chip-select terminal, which can be driven from standard TTL circuits without an external pull-up resistor, affects the data-in, data-out and read/write inputs. The data input and data output terminals are enabled when chip select is low. Therefore, the read, write, and read, modify write operations are performed only when chip select is low. If the chip is to be selected for a given cycle, the chip-select input must be low on or before the rising edge of the chip enable. If the chip is not to be selected for a given cycle, chip select must be held high as long as chip enable is high. A register for the chip-select input is provided on the chip to reduce overhead and simplify system design.

chip enable (CE)

A single external clock input is required. All read, write, and read, modify write operations take place when the chip enable input is high. When the chip enable is low, the memory is in the low-power standby mode. No read/write operations can take place because the chip is automatically precharging.

operation (continued)

mode select (R/$\overline{W}$)

The read or write mode is selected through the read/write (R/$\overline{W}$) input. A logic high on the R/$\overline{W}$ input selects the read mode and a logic low selects the write mode. The read/write terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected.

address (A0–A11)

All addresses must be stable on or before the rising edge of the chip-enable pulse. All address inputs can be driven from standard TTL circuits without pull-up resistors. Address registers are provided on chip to reduce overhead and simplify system design.

data-in (DI)

Data is written during a write or read, modify write cycle while the chip enable is high. The data-in terminal can be driven from standard TTL circuits without a pull-up resistor. There is no register on the data-in terminal.

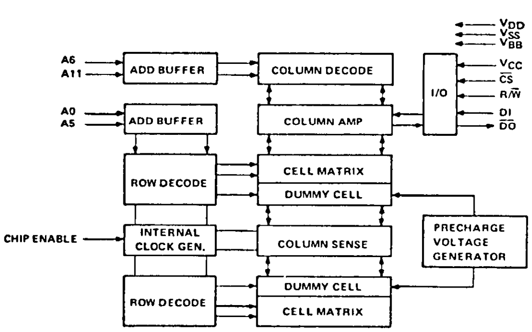
data-out ($\overline{DO}$)

The three-state output buffer provides direct TTL compatibility with a fan-out of two Series 74 TTL gates. The output is in the high-impedance (floating) state when the chip enable is low. It remains in the high-impedance state if the chip-select input is high when chip enable goes high and provided that chip select remains high as long as chip enable is high. If the chip select is set up low prior to the rise of chip enable and held low an interval after that rise, the output will be enabled as long as chip enable stays high regardless of subsequent changes in the level of chip select. A data-valid mode is always preceded by a low output state. Data-out is inverted from data-in.

refresh

Refresh must be performed every two milliseconds by cycling through the 64 addresses of the lower-order-address inputs, A0 through A5 (pins 8, 9, 10, 13, 14, 15), or by addressing every row within any 2-millisecond period. Addressing any row refreshes all 64 bits in that row. The chip does not need to be selected during the refresh. If the chip is refreshed during a write mode, then chip select must be high. The column addresses (A6 through A11) can be indeterminate during refresh.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note)	−0.3 to 20 V
Supply voltage, V_{DD} (see Note)	−0.3 to 20 V
Supply voltage, V_{SS} (see Note)	−0.3 to 20 V
All input voltages (see Note)	−0.3 to 20 V
Chip-enable voltage (see Note)	−0.3 to 20 V
Output voltage (operating, with respect to V_{SS})	−2 to 7 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−55°C to 150°C

NOTE: Under absolute maximum ratings, voltage values are with respect to the most-negative supply voltage, V_{BB} (substrate), unless otherwise noted. Throughout the remainder of this data sheet, voltage values are with respect to V_{SS}.

recommended operating conditions (see Note)

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Supply voltage, V_{DD}	11.4	12	12.6	V
Supply voltage, V_{SS}		0		V
Supply voltage, V_{BB}	−4.5	−5	−5.5	V
High-level input voltage, V_{IH} (all inputs except chip enable)	2.2		5.25	V
High-level chip enable input voltage, $V_{IH(CE)}$	V_{DD} −0.6		V_{DD} +1.0	V
Low-level input voltage, V_{IL} (all inputs except chip enable) (see Note)	−0.6		0.6	V
Low-level chip enable input voltage, $V_{IL(CE)}$ (see Note)	−1		0.6	V
Refresh time, $t_{refresh}$			2	ms
Operating free-air temperature, T_A	0		70	°C

NOTE: The algebraic convention where the most negative limit is designated as minimum is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions, T_A = 0°C to 70°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_O = −2 mA		2.4		V_{CC}	V
V_{OL}	Low-level output voltage	I_O = 3.2 mA		V_{SS}		0.4	V
I_I	Input current (all inputs except chip enable)	V_I = 0 to 5.25 V				10	μA
$I_{I(CE)}$	Chip enable input current	V_I = 0 to 13.2 V				2	μA
I_{OZ}	High-impedance-state (off-state) output current	V_O = 0 to 5.25 V				10	μA
I_{CC}	Supply current from V_{CC}	2 Series 74 TTL loads				1	mA
I_{DD}	Supply current from V_{DD}	$V_{IH(CE)}$ = 12.6 V			30	60	mA
I_{DD}	Supply current from V_{DD}, standby	$V_{IL(CE)}$ = 0.6 V			20	200	μA
$I_{DD(av)}$	Average supply current from V_{DD} during read or write cycle	Minimum cycle time	TMS 4060		32		mA
			TMS 4060-1		35		
			TMS 4060-2		38		
$I_{DD(av)}$	Average supply current from V_{DD} during read, modify write cycle		TMS 4060		32		mA
			TMS 4060-1		35		
			TMS 4060-2		38		
I_{BB}	Supply current from V_{BB}	V_{BB} = −5.5 V, V_{DD} = 12.6 V,	V_{CC} = 5.25 V, V_{SS} = 0 V		−5	−100	μA

†All typical values are at T_A = 25°C.

capacitance at V_{DD} = 12 V, V_{SS} = 0 V, V_{BB} = −5 V, V_{CC} = 5 V, $V_{I(CE)}$ = 0 V, V_I = 0 V, f = 1 MHz, T_A = 0°C to 70°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$C_{i(ad)}$	Input capacitance address inputs			5	7	pF
$C_{i(CE)}$	Input capacitance clock input	$V_{I(CE)}$ = 10.8 V		18	22	pF
		$V_{I(CE)}$ = −1.0 V		23	27	
$C_{i(\overline{CS})}$	Input capacitance chip select input			4	6	pF
$C_{i(data)}$	Input capacitance data input			4	6	pF
$C_{i(R/\overline{W})}$	Input capacitance read/write input			5	7	pF
C_o	Output capacitance			5	7	pF

†All typical values are at T_A = 25°C.

read cycle timing requirements over recommended supply voltage range, $T_A = 0°C$ to $70°C$

PARAMETER		TMS 4060 MIN	TMS 4060 MAX	TMS 4060-1 MIN	TMS 4060-1 MAX	TMS 4060-2 MIN	TMS 4060-2 MAX	UNIT
$t_{c(rd)}$	Read cycle time	470		430		400		ns
$t_{w(CEH)}$	Pulse width, chip enable high	300	4000	260	4000	230	4000	ns
$t_{w(CEL)}$	Pulse width, chip enable low	130		130		130		ns
$t_{r(CE)}$	Chip-enable rise time		40		40		40	ns
$t_{f(CE)}$	Chip-enable fall time		40		40		40	ns
$t_{su(ad)}$	Address setup time	0↑		0↑		0↑		ns
$t_{su(\overline{CS})}$	Chip-select setup time	0↑		0↑		0↑		ns
$t_{su(rd)}$	Read setup time	0↑		0↑		0↑		ns
$t_{h(ad)}$	Address hold time	150↑		150↑		150↑		ns
$t_{h(\overline{CS})}$	Chip-select hold time	150↑		150↑		150↑		ns
$t_{h(rd)}$	Read hold time	40↓		40↓		40↓		ns

↑↓ The arrow indicates the edge of the chip enable pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

3

read cycle switching characteristics over recommended supply voltage range, $T_A = 0°C$ to $70°C$

PARAMETER		TMS 4060 MIN	TMS 4060 MAX	TMS 4060-1 MIN	TMS 4060-1 MAX	TMS 4060-2 MIN	TMS 4060-2 MAX	UNIT
$t_{a(CE)}$	Access time from chip enable†		280		230		180	ns
$t_{a(ad)}$	Access time from address†		300		250		200	ns
t_{PHZ} or t_{PLZ}	Output disable time from high or low level‡	30		30		30		ns
t_{PZL}	Output enable time to low level‡		250		200		150	ns

†Test conditions: $C_L = 50$ pF, $t_{r(CE)} = 20$ ns, Load = 1 Series 74 TTL gate.
‡Test conditions: $C_L = 50$ pF, Load = 1 Series 74 TTL gate.

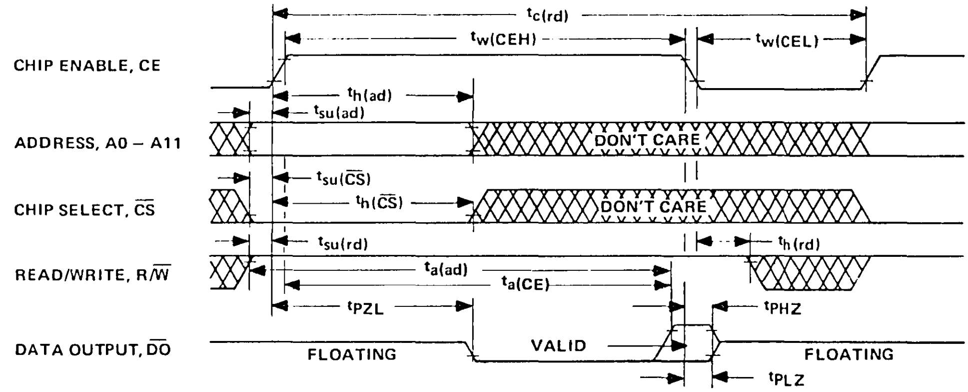
write cycle timing requirements over recommended supply voltage range, $T_A = 0°C$ to $70°C$

PARAMETER		TMS 4060 MIN	TMS 4060 MAX	TMS 4060-1 MIN	TMS 4060-1 MAX	TMS 4060-2 MIN	TMS 4060-2 MAX	UNIT
$t_{c(wr)}$	Write cycle time	470		430		400		ns
$t_{w(CEH)}$	Pulse width, chip enable high	300	4000	260	4000	230	4000	ns
$t_{w(CEL)}$	Pulse width, chip enable low	130		130		130		ns
$t_{w(wr)}$	Write pulse width	200		190		180		ns
$t_{r(CE)}$	Chip-enable rise time		40		40		40	ns
$t_{f(CE)}$	Chip-enable fall time		40		40		40	ns
$t_{su(ad)}$	Address setup time	0↑		0↑		0↑		ns
$t_{su(\overline{CS})}$	Chip-select setup time	0↑		0↑		0↑		ns
$t_{su(da-wr)}$	Data-to-write setup time*	0		0		0		ns
$t_{su(wr)}$	Write-pulse setup time	240↓		220↓		210↓		ns
$t_{h(ad)}$	Address hold time	150↑		150↑		150↑		ns
$t_{h(\overline{CS})}$	Chip-select hold time	150↑		150↑		150↑		ns
$t_{h(da)}$	Data hold time	40↓		40↓		40↓		ns

↑↓ The arrow indicates the edge of the chip enable pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.
*If R/$\overline{W}$ is low before CE goes high then DI must be valid when CE goes high.

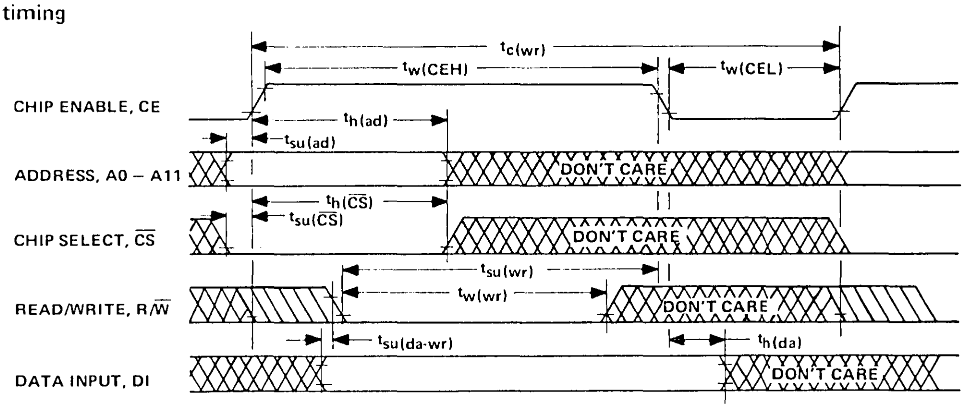
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

read cycle timing



NOTE: For the chip-enable input, high and low timing points are 90% and 10% of $V_{IH(CE)}$. Other input timing points are 0.6 V (low) and 2.2 V (high). Output timing points are 0.4 V (low) and 2.4 V (high).

write cycle timing



NOTE: For the chip-enable input, high and low timing points are 90% and 10% of $V_{IH(CE)}$. Other input timing points are 0.6 V (low) and 2.2 V (high). Output timing points are 0.4 V (low) and 2.4 V (high). During the time from the rise of CE to the fall of R/$\overline{W}$, R/$\overline{W}$ is permitted to change from high to low only.

read, modify write cycle timing requirements over recommended supply voltage range, T_A = 0°C to 70°C

PARAMETER		TMS 4060		TMS 4060-1		TMS 4060-2		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(RMW)}$	Read, modify write cycle time*	710		640		580		ns
$t_{w(CEH)}$	Pulse width, chip enable high*	540	4000	470	4000	410	4000	ns
$t_{w(CEL)}$	Pulse width, chip enable low	130		130		130		ns
$t_{w(wr)}$	Write-pulse width	200		190		180		ns
$t_{r(CE)}$	Chip-enable rise time		40		40		40	ns
$t_{f(CE)}$	Chip-enable fall time		40		40		40	ns
$t_{su(ad)}$	Address setup time	0↑		0↑		0↑		ns
$t_{su(\overline{CS})}$	Chip-select setup time	0↑		0↑		0↑		ns
$t_{su(da-wr)}$	Data-to-write setup time	0		0		0		ns
$t_{su(rd)}$	Read pulse setup time	0↑		0↑		0↑		ns
$t_{su(wr)}$	Write pulse setup time	240↓		220↓		210↓		ns
$t_{h(ad)}$	Address hold time	150↑		150↑		150↑		ns
$t_{h(\overline{CS})}$	Chip-select hold time	150↑		150↑		150↑		ns
$t_{h(rd)}$	Read hold time	280↑		230↑		180↑		ns
$t_{h(da)}$	Data hold time	40↓		40↓		40↓		ns

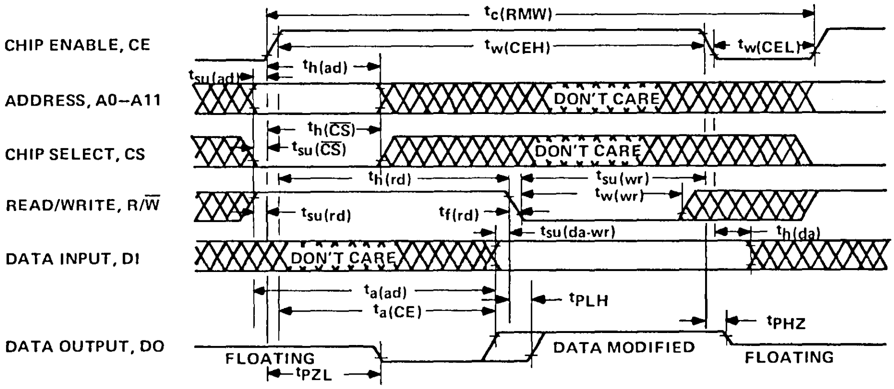
↑↓ The arrow indicates the edge of the chip-enable pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.
*Test conditions: $t_{f(rd)}$ = 20 ns.

read, modify write cycle switching characteristics over recommended supply voltage range, T_A = 0°C to 70°C

PARAMETER		TMS 4060		TMS 4060-1		TMS 4060-2		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(CE)}$	Access time from chip enable†		280		230		180	ns
$t_{a(ad)}$	Access time from address†		300		250		200	ns
t_{PLH}	Propagation delay time, low-to-high level output from write pulse‡	30		30		30		ns
t_{PHZ}	Output disable time from high level‡	30		30		30		ns
t_{PZL}	Output enable time to low level‡		250		200		150	ns

†Test conditions: C_L = 50 pF, $t_{r(CE)}$ = 20 ns, Load = 1 Series 74 TTL gate.
‡Test conditions: C_L = 50 pF, Load = 1 Series 74 TTL gate.

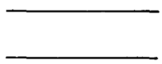
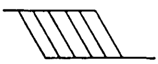
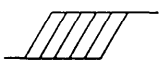
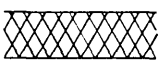
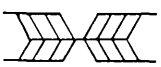
read, modify write cycle timing



NOTE: For the chip enable input, high and low timing points are 90% and 10% of $V_{IH(CE)}$. Other input timing points are 0.6 V (low) and 2.2 V (high). Output timing points are 0.4 V (low) and 2.4 V (high).

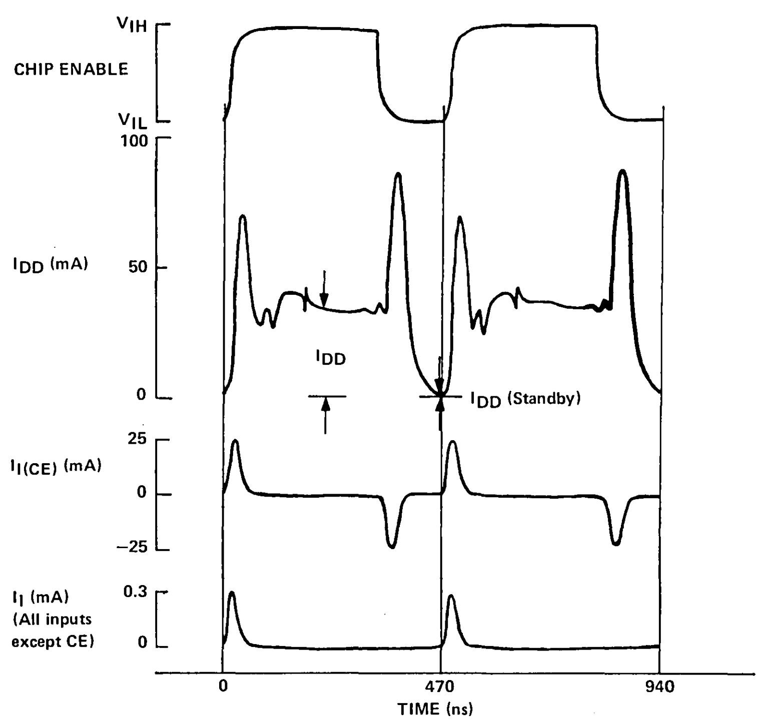
3

timing diagram conventions

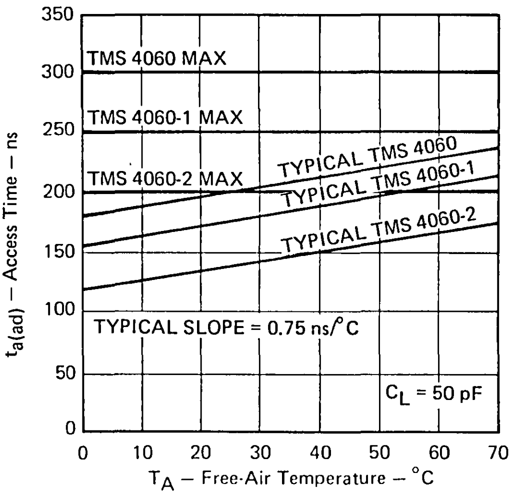
TIMING DIAGRAM SYMBOL	MEANING INPUT FORCING FUNCTIONS	MEANING OUTPUT RESPONSE FUNCTIONS
	Must be steady high or low	Will be steady high or low
	High-to-low changes permitted	Will be changing from high to low sometime during designated interval
	Low-to-high changes permitted	Will be changing from low to high sometime during designated interval
	Don't care	State unknown or changing
	(Does not apply)	Center line is high-impedance off-state

3

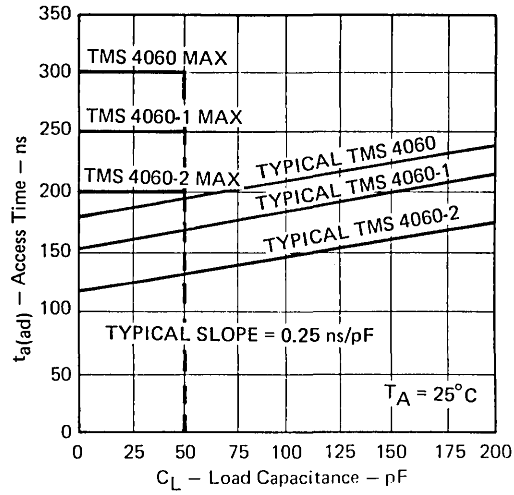
TYPICAL WAVEFORMS



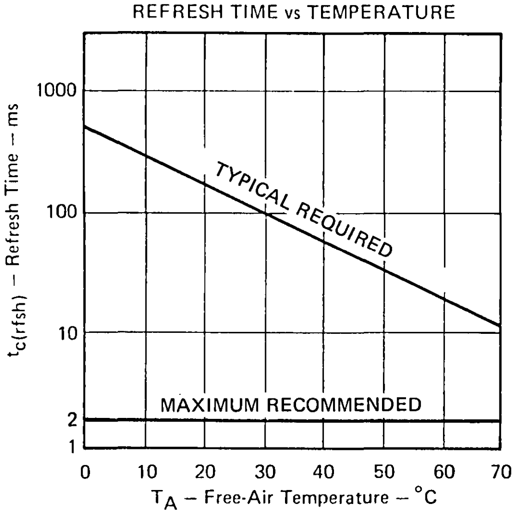
ACCESS TIMES vs TEMPERATURE



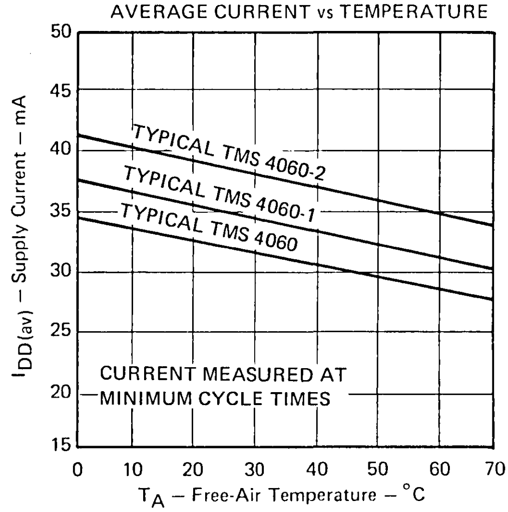
ACCESS TIMES vs LOAD CAPACITANCE



REFRESH TIME vs TEMPERATURE



AVERAGE CURRENT vs TEMPERATURE



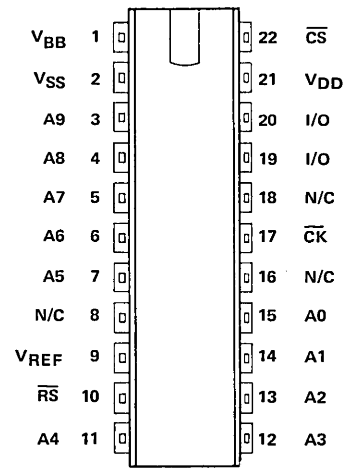
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

MOS LSI — TMS 4062 JL, NL; TMS 4063 JL, NL
1024-WORD BY 1-BIT DYNAMIC RANDOM-ACCESS MEMORIES

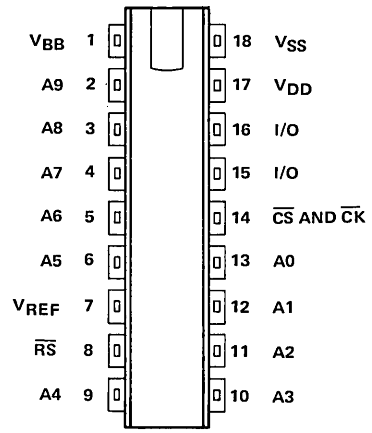
BULLETIN NO. DL-S 7512272, MAY 1975

- 1024 x 1 Organization
- Access Time . . . 130 ns Maximum
- Cycle Time . . . 200 ns Maximum
- Low Power Dissipation:
  Operating . . . 120 mW Typical
  Standby . . . 2 mW Typical
- Differential Output
- Wire-OR Capability
- Chip Select For Simplified Memory Expansion
- 22-Pin or 18-Pin Dual-In-Line Package

TMS 4062 JL, NL
22-PIN CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGES
(TOP VIEW)



TMS 4063 JL, NL
18-PIN CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGES
(TOP VIEW)



description

The TMS 4062 JL, NL and TMS 4063 JL, NL are high-speed, 1024-word by 1-bit, dynamic random-access memories fabricated on a single monolithic chip with P-channel enhancement-type MOS processing. The devices are designed for use in low-cost, high-performance memory applications. High performance and low power dissipation are achieved with a four-transistor storage cell and unique support circuitry. Low-capacitance inputs minimize driver-circuit power requirements, simplify TTL-to-MOS conversion, and reduce overall system costs.

The memory is fully decoded and its differential outputs can be OR-tied. The chip-select input allows the selection of individual components in large memory arrays. Stored information is nondestructively read and the differential output voltage is of the same polarity as the differential input voltage during the write operation. Since the memory is dynamic, it must be refreshed periodically.

The TMS 4062 is offered in 22-pin dual-in-line ceramic (JL suffix) and plastic (NL suffix) packages designed for insertion in mounting-hole rows on 400-mil centers. The TMS 4063 is offered in 18-pin ceramic (JL suffix) and plastic (NL suffix) dual-in-line packages designed for insertion in mounting-hole rows on 300-mil centers.

3

operation

Reset ($\overline{RS}$)

Every device cycle begins with the reset pulse. When the reset input is low, the internal circuits are precharged and the address inverters are turned off. Address inputs must be valid and stable before reset goes high and must be held stable a minimum time after reset goes high to allow the row and column decoders to function.

operation (continued)

Clock and Chip-Select Clock ($\overline{CK}$, $\overline{CS}$)

The clock input is gated by the row decoders to activate a row the address of which is specified by A0-A4. The chip-select clock input is gated by the column decoders to select a column of address A5-A9. Thus, the clock and chip-select clock pulses, at the low level and along with a 10-bit address, isolate a single memory cell and allow transfer of information to or from the input/output lines, which are also gated by the chip-select clock. After output data is read, the clock and chip-select clock must return to the high level before the start of the next cycle.

Address (A0-A9)

Addresses must be valid before reset goes high. The address inputs exhibit small input capacitances since these inputs are connected to the drains of MOS transistors that are turned off during the reset and clock pulses.

Data Input/Output (I/O)

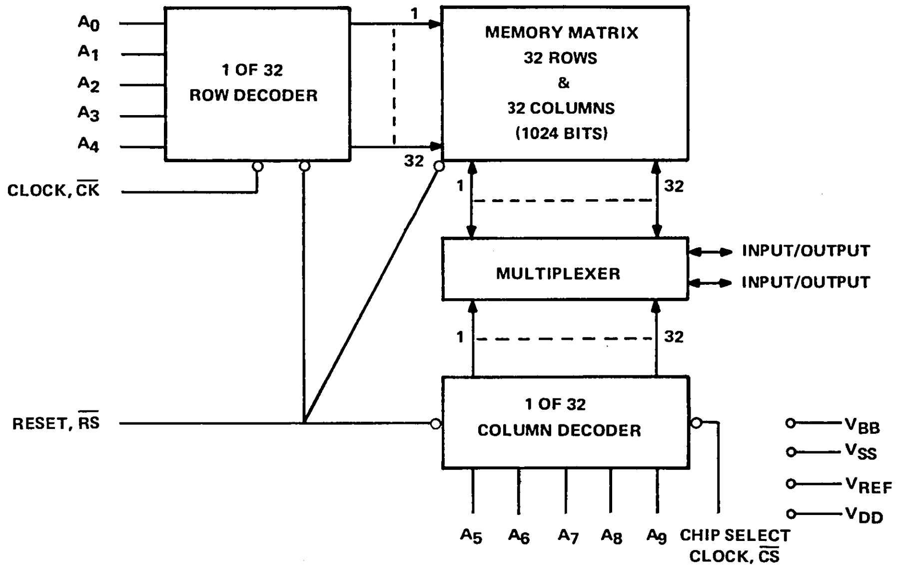
Data is read or written through two input/output terminals that operate in a differential mode. To write, one I/O input is taken high while the other remains at V_{REF}. During a later read cycle, the input that was taken high will source current while the other will not. The I/O terminals may be connected by resistors to V_{REF} for voltage sensing or directly to a current sense amplifier such as the SN75370. The I/O terminals are gated by chip select.

3

Refresh

Each cell must be refreshed at least once in every 2-millisecond period by cycling through the lower order row addresses (A0-A4) or by addressing each row at least once in that period. Addressing any row refreshes all 32 cells in that row. The chip-select clock need not be activated during refresh; however, the clock input must be cycled from high to low to high.

functional block diagram



3

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltages:
- V_{DD} and V_{REF}, with respect to V_{SS} . . . . −27 V to 0.5 V
- V_{DD} and V_{REF}, with respect to V_{BB} . . . . −30 V to 0.5 V
- V_{BB}, with respect to V_{SS} . . . . −0.5 V to 10 V

All input voltages, with respect to V_{SS} . . . . −30 V to 0.5 V
Operating free-air temperature range . . . . −0°C to 70°C
Storage temperature range . . . . −55°C to 125°C

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, $V_{BB}-V_{SS}$ (see Notes 1 and 2)	2.3	2.5	2.7	V
Supply voltage, V_{DD}		0		V
Supply voltage, V_{SS}	19	20	21	V
Supply voltage, V_{REF}	6.6	7	7.4	V
High-level input voltage, all inputs, V_{IH}	V_{SS} −2		V_{SS}	V
Low-level address input voltage, $V_{IL(ad)}$ (see Note 3)	−2	0	1	V
Low-level input voltage at reset and both clocks, $V_{IL(rs,\ \phi)}$ (see Note 3)	−5	0	0.4	V
Low-level input voltage at I/O, $V_{IL(I/O)}$	V_{REF} −1	V_{REF}	V_{REF} +1	V
Refresh time, $t_{refresh}$			2	ms
Operating free-air temperature, T_A	0		70	°C

NOTES: 1. Throughout this data sheet supply voltage values are with respect to V_{DD}, unless otherwise noted.
2. V_{BB} must be applied prior to V_{SS}.
3. The algebraic convention where the most positive limit is designated as maximum is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_{ODH}	High-level differential output current		100			μA
$I_{I(ad)}$	Address input current	$V_I = V_{DD}$ (0 V)			1	μA
$I_{I(rs,\ \phi)}$	Reset or either clock input current	$V_I = V_{DD}$ (0 V)			10	μA
$I_{I(I/O)}$	I/O input current	$V_I = V_{REF}$			2	μA
I_{BB}	Supply current from V_{BB}	All inputs at V_{SS}			10	μA
I_{REF}	Supply current from V_{REF}	All inputs at V_{SS}			10	μA
$I_{SS(1)}$	Supply current from V_{SS}	All address and reset inputs at V_{SS}, (see Figure 1)			100	μA
$I_{SS(2)}$	Supply current from V_{SS}	Reset at V_{DD} (0 V), Clocks at V_{SS}, T_A = 25°C		9	15	mA
$I_{SS(3)}$	Peak supply current from V_{SS} (see Note 4)	Reset and both clocks at V_{SS}, All addresses at V_{DD} (0 V), T_A = 25°C		18	30	mA
$I_{SS(4)}$	Supply current from V_{SS}	Reset at V_{SS}, All other inputs at V_{DD} (0 V)			100	μA
$I_{SS(av)}$	Average supply current from V_{SS}	All supply voltages nominal, t_c = 290 ns		6		mA

†All typical values are at T_A = 25°C.
NOTE 4: The steady-state value of $I_{SS(3)}$ is less than 100 μA.

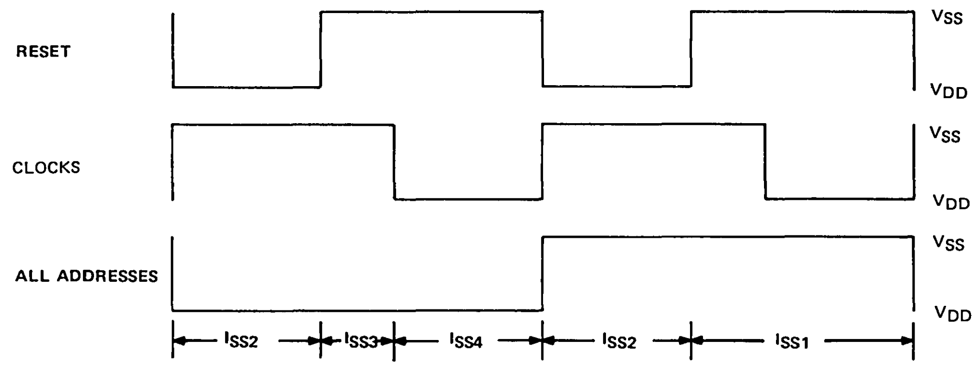


FIGURE 1—TIME INTERVALS FOR MEASURING SUPPLY CURRENTS

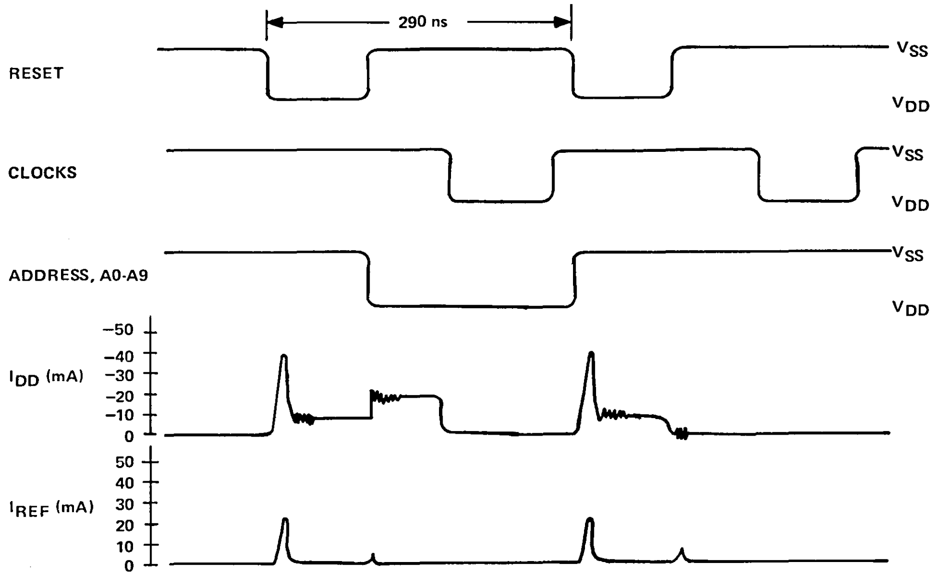
3

capacitances over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP†	MAX	UNIT
$C_{i(ad)}$	Input capacitance, address inputs	$V_I = V_{SS}$, f = 1 MHz	2.5	3.5	pF
$C_{i(rs)}$	Input capacitance, reset inputs	$V_I = V_{SS}$, f = 1 MHz	30	40	pF
$C_{i(\phi)}$	Input capacitance, both clock inputs	$V_I = V_{SS}$, f = 1 MHz	15	18	pF
$C_{(I/O)}$	I/O terminal capacitance	$V_I = V_{SS}$, f = 1 MHz	2.5	3.5	pF

†All typical values are at $T_A = 25°C$.

TYPICAL DYNAMIC CURRENT WAVEFORMS



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

57!

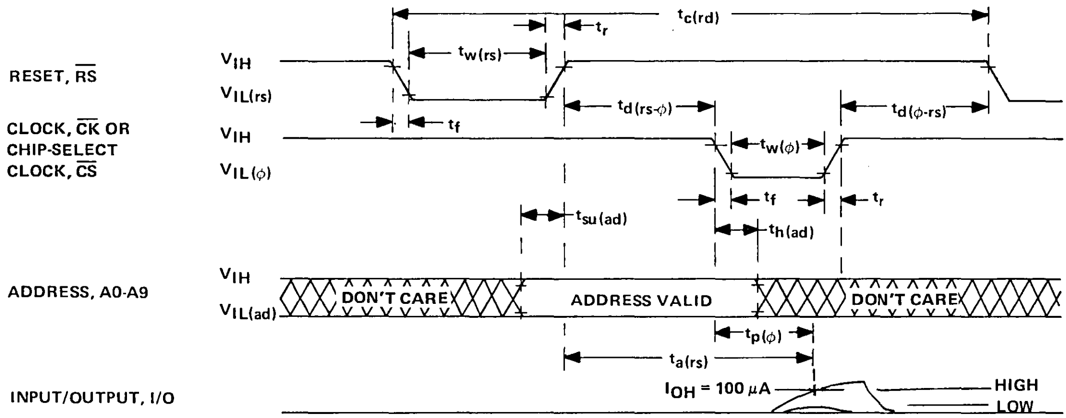
read cycle timing requirements over recommended supply voltage ranges, T_A = 0°C to 70°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{c(rd)}$	Read cycle time	$V_{IL(rs,\phi)} = 0$ V	290		ns
		$V_{IL(rs,\phi)} = -5$ V	200		
$t_{w(rs)}$	Pulse width, reset low	$V_{IL(rs,\phi)} = 0$ V	90	2000	ns
		$V_{IL(rs,\phi)} = -5$ V	20	2000	
$t_{w(\phi)}$	Pulse width, either clock low	$V_{IL(rs,\phi)} = 0$ V	60	2000	ns
		$V_{IL(rs,\phi)} = -5$ V	40	2000	
t_r	Rise time of reset or either clock			20	ns
t_f	Fall time of reset or either clock			20	ns
$t_{d(rs\text{-}\phi)}$	Delay time, reset high to either clock		60	2000	ns
$t_{d(\phi\text{-}rs)}$	Delay time, either clock high to reset		0		ns
$t_{su(ad)}$	Address setup time		0		ns
$t_{h(ad)}$	Address hold time		50		ns

read cycle switching characteristics over recommended supply voltage ranges, T_A = 0°C to 70°C, $R_L = 400\ \Omega$, $C_L = 10$ pF

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{a(rs)}$	Access time from reset	$V_{IL(rs,\phi)} = 0$ V		150	ns
		$V_{IL(rs,\phi)} = -5$ V		130	
$t_{p(\phi)}$	Propagation delay time to output	$V_{IL(rs,\phi)} = 0$ V		90	ns
		$V_{IL(rs,\phi)} = -5$ V		70	

read cycle timing diagram



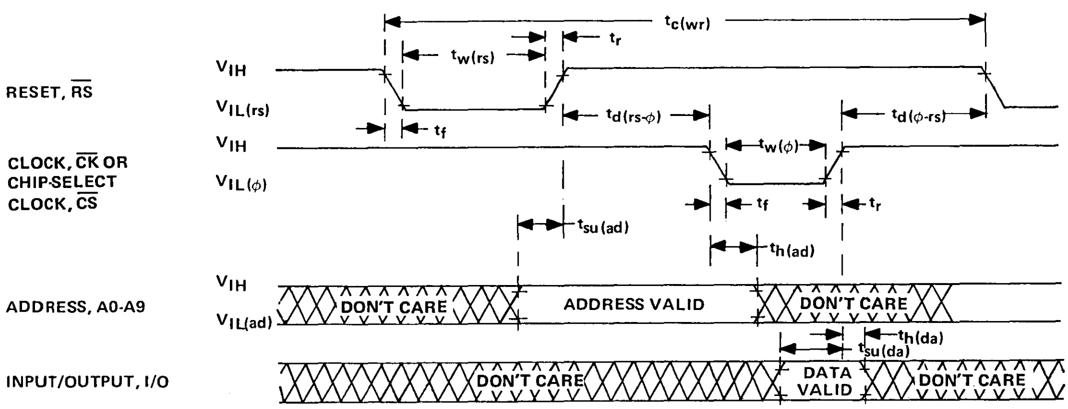
NOTE: All reference points on inputs are 90% and 10% points.

write cycle timing requirements over recommended supply voltage ranges, T_A = 0°C to 70°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{c(wr)}$	Write cycle time	$V_{IL(rs,\phi)}$ = 0 V	290		ns
		$V_{IL(rs,\phi)}$ = −5 V	200		
$t_{w(rs)}$	Pulse width, reset low	$V_{IL(rs,\phi)}$ = 0 V	90	2000	ns
		$V_{IL(rs,\phi)}$ = −5 V	20	2000	
$t_{w(\phi)}$	Pulse width, either clock low	$V_{IL(rs,\phi)}$ = 0 V	60	2000	ns
		$V_{IL(rs,\phi)}$ = −5 V	40	2000	
t_r	Rise time of reset or either clock			20	ns
t_f	Fall time of reset or either clock			20	ns
$t_{d(rs\text{-}\phi)}$	Delay time, reset high to either clock		60	2000	ns
$t_{d(\phi\text{-}rs)}$	Delay time, either clock high to reset		0		ns
$t_{su(ad)}$	Address setup time		0		ns
$t_{su(da)}$	Data setup time	$V_{IL(rs,\phi)}$ = 0 V	70		ns
		$V_{IL(rs,\phi)}$ = −5 V	60		
$t_{h(ad)}$	Address hold time		50		ns
$t_{h(da)}$	Data hold time		0		ns

3

write cycle timing diagram



NOTE: All reference points on inputs are 90% and 10% points.

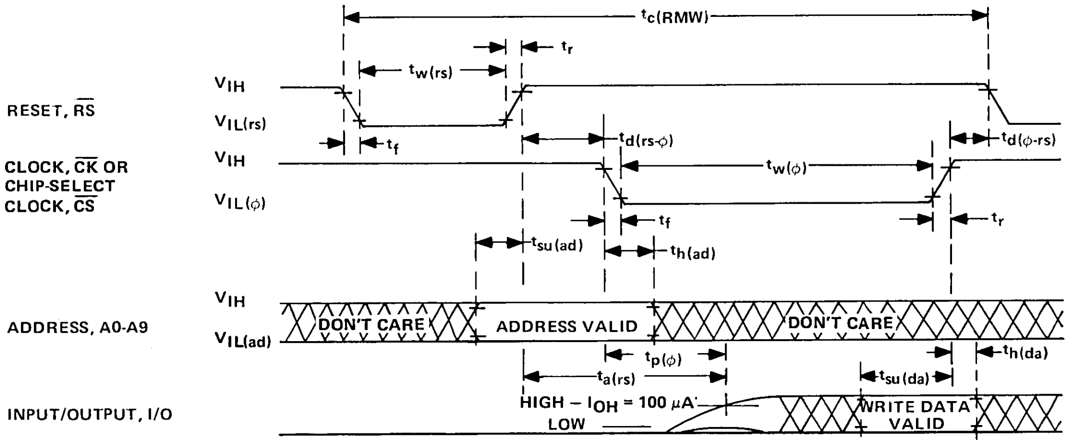
read, modify write cycle timing requirements over recommended supply voltage ranges, T_A = 0°C to 70°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{c(RMW)}$	Read, modify write cycle time	$V_{IL(rs,\phi)}$ = 0 V	370		ns
		$V_{IL(rs,\phi)}$ = −5 V	290		
$t_{w(rs)}$	Pulse width, reset low	$V_{IL(rs,\phi)}$ = 0 V	90	2000	ns
		$V_{IL(rs,\phi)}$ = −5 V	20	2000	
$t_{w(\phi)}$	Pulse width, either clock low	$V_{IL(rs,\phi)}$ = 0 V	180	2000	ns
		$V_{IL(rs,\phi)}$ = −5 V	140	2000	
t_r	Rise time of reset or either clock			20	ns
t_f	Fall time of reset or either clock			20	ns
$t_{d(rs\text{-}\phi)}$	Delay time, reset high to either clock		60	2000	ns
$t_{d(\phi\text{-}rs)}$	Delay time, either clock high to reset		0		ns
$t_{su(ad)}$	Address setup time		0		ns
$t_{su(da)}$	Data setup time	$V_{IL(rs,\phi)}$ = 0 V	70		ns
		$V_{IL(rs,\phi)}$ = −5 V	60		
$t_{h(ad)}$	Address hold time		50		ns
$t_{h(da)}$	Data hold time		0		ns

read, modify write cycle switching characteristics over recommended supply voltage ranges, T_A = 0°C to 70°C, R_L = 400 Ω, C_L = 10 pF

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{a(rs)}$	Access time from reset	$V_{IL(rs,\phi)}$ = 0 V	150		ns
		$V_{IL(rs,\phi)}$ = −5 V	130		
$t_{p(\phi)}$	Propagation delay time to output	$V_{IL(rs,\phi)}$ = 0 V	90		ns
		$V_{IL(rs,\phi)}$ = −5 V	70		

read, modify write cycle timing diagram



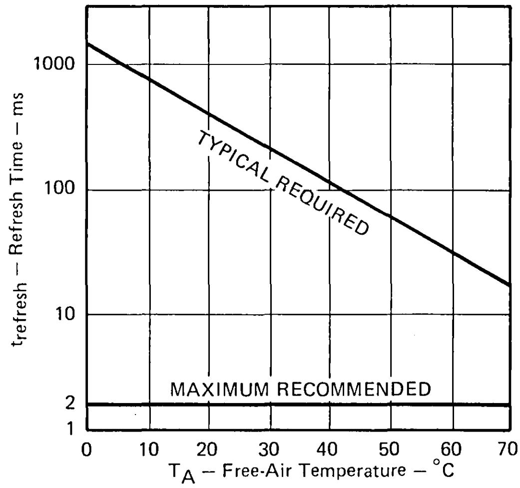
NOTE: All reference points on inputs are 90% and 10% points.

3

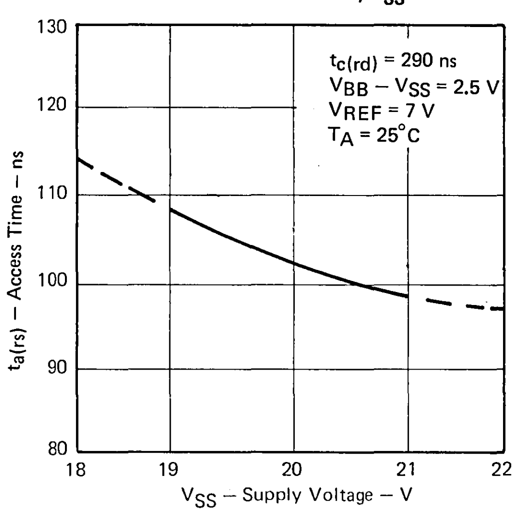
3

TYPICAL CHARACTERISTICS

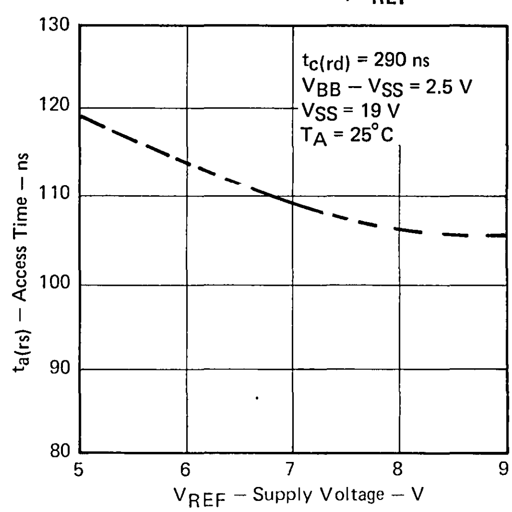
REFRESH vs FREE-AIR TEMPERATURE



ACCESS TIME FROM RESET vs SUPPLY VOLTAGE, V_{SS}



ACCESS TIME FROM RESET vs SUPPLY VOLTAGE, V_{REF}



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

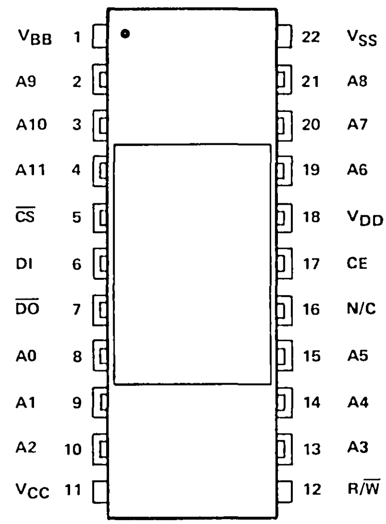
TMS 4030 JR, TMS 4050 JR, TMS 4060 JR SMC 4030 JR, SMC 4050 JR, SMC 4060 JR 4096-BIT RANDOM-ACCESS MEMORIES

BULLETIN NO. DL-S 7512276, MAY 1975

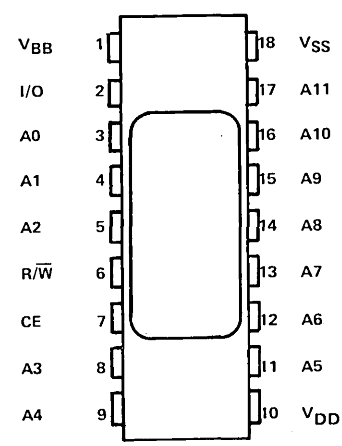
EXTENDED TEMPERATURE RANGE AND HI-REL DEVICES

- 4096 x 1 Organization
- Extended Temperature Range (−55°C to 85°C)
- SMC Type Processed to Class B of MIL-STD-883 per Level III of TI 38510/MACH-IV Program
- Maximum Access Time . . . 300 ns
- Minimum Read or Write Cycle . . . 470 ns
- Minimum Read, Modify Write Cycle: 710 ns (730 ns for TMS 4050)
- Full TTL Compatibility on All Inputs (No Pull-Up Resistors Needed)
- Single Low-Capacitance Clock

TMS 4030 JR, TMS 4060 JR
SMC 4030 JR, SMC 4060 JR
22-PIN CERAMIC DUAL-IN-LINE PACKAGE
(TOP VIEW)



TMS 4050 JR, SMC 4050 JR
18-PIN CERAMIC DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

The TMS 4030 JR, TMS 4050 JR, and TMS 4060 JR are extended temperature range (−55°C to 85°C) versions of the TMS 4030 JL, TMS 4050 JL, and TMS 4060 JL. These devices are ideal for critical equipment applications in aerospace, industrial, and military environments.

The SMC 4030 JR, SMC 4050 JR, and SMC 4060 JR are also rated to operate from −55°C to 85°C. These SMC devices are specifically processed and 100% screened to the requirements of Class B of MIL-STD-883 per level III of the Texas Instruments 38510/MACH-IV program.

The SMC series of 4096-bit RAMs receive the following special screening tests:

Precap visual	method 2010.2
Stabilization bake	method 1006.1
Temperature cycling . . .	method 1010.1
Centrifuge	method 2001.1
Fine and gross leak	method 1014.1
Burn-in for 168 hours at 125°C	method 1015.1
Final electrical testing at 25°C and high temperatures	

These two series of devices are offered only in ceramic (JR suffix) dual-in-line packages. The 22-pin package (TMS 4030, TMS 4060, SMC 4030, and SMC 4060) inserts in mounting-hole rows on 400-mil centers. The 18-pin package (TMS 4050, SMC 4050) is designed for insertion in mounting-hole rows on 300-mil centers and is ideal for high-density applications.

PRELIMINARY DATA SHEET:
Supplementary data may be published at a later date.

TMS 4030 JR, TMS 4050 JR, TMS 4060 JR
SMC 4030 JR, SMC 4050 JR, SMC 4060 JR
4096-BIT RANDOM-ACCESS MEMORIES

operation

For a complete description of the device operation see the appropriate data sheets on the commercial temperature range (0°C to 70°C, JL, NL suffix) 4K RAM products. All timing parameters on these extended-temperature range and high-reliability devices are identical with the associated 300-ns-access-time commercial device types.

For detailed information on processing, refer to TI's MACH IV program and High-Reliability Microelectronics Procurement Specifications, MIL-STD-883.

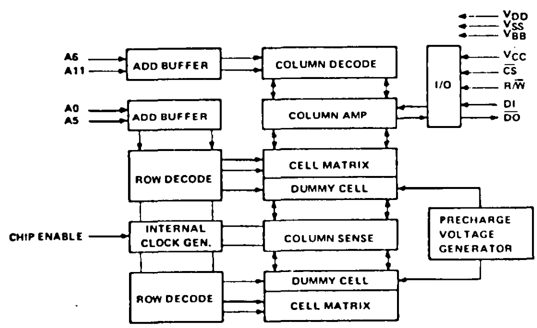
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1)	−0.3 to 20 V
Supply voltage, V_{SS} (see Note 1)	−0.3 to 20 V
All input voltages (see Note 1)	−0.3 to 20 V
Chip-enable voltage (see Note 1)	−0.3 to 20 V
Output voltage (operating, with respect to V_{SS})	−2 to 7 V
Operating free-air temperature range	−55°C to 85°C
Storage temperature range	−55°C to 150°C

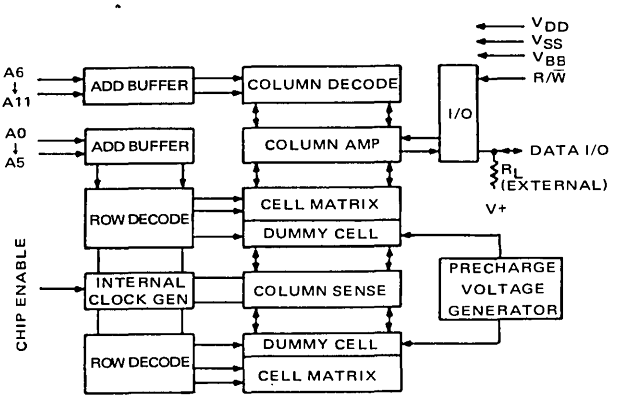
3

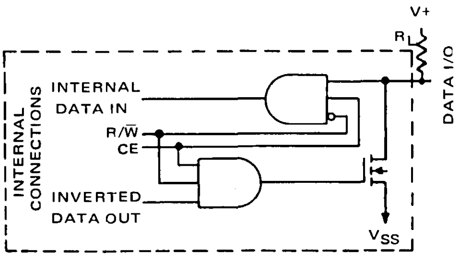
NOTE: 1. Under absolute maximum ratings, voltage values are with respect to the most negative supply voltage, V_{BB} (substrate), unless otherwise noted. Throughout the remainder of this data sheet voltage values are with respect to V_{SS}.

functional block diagram



TMS 4030/SMC 4030, TMS 4060/SMC 4060





I/O LOGIC

TMS 4050/SMC 4050

recommended operating conditions

PARAMETER	TMS 4030 JR SMC 4030 JR			TMS 4060 JR SMC 4060 JR			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.75	5	5.25	4.75	5	5.25	V
Supply voltage, V_{DD}	11.4	12	12.6	11.4	12	12.6	V
Supply voltage, V_{SS}		0			0		V
Supply voltage, V_{BB}	−2.7	−3	−3.3	−4.5	−5	−5.5	V
High-level input voltage, V_{IH} (all inputs except chip enable)	2.2		5.25	2.2		5.25	V
High-level chip enable input voltage, $V_{IH(CE)}$	V_{DD} −0.6		V_{DD} +1	V_{DD} −0.6		V_{DD} +1	V
Low-level input voltage, V_{IL} (all inputs except chip enable)	−0.6†		0.6	−0.6†		0.6	V
Low-level chip enable input voltage, $V_{IL(CE)}$	−1†		0.6	−1†		0.6	V
Refresh time, $t_{refresh}$			1			1	ms
Operating free-air temperature, T_A	−55		85	−55		85	°C

†The algebraic convention where the most negative limit is designated as minimum is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions, T_A = −55°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_O = −2 mA	2.4		V_{CC}	V
V_{OL}	Low-level output voltage	I_O = 3.2 mA	V_{SS}		0.4	V
I_I	Input current (all inputs except chip enable)	V_I = 0 to 5.25 V			10	μA
$I_{I(CE)}$	Chip-enable input current	V_I = 0 to 13.2 V			2	μA
I_{OZ}	High-impedance-state (off-state) output current	V_O = 0 to 5.25 V			10	μA
I_{CC}	Supply current from V_{CC}	2 Series 74 TTL loads			1	mA
I_{DD}	Supply current from V_{DD}	$V_{IH(CE)}$ = 12.6 V		30	80	mA
I_{DD}	Supply current from V_{DD}, standby	$V_{IL(CE)}$ = 0.6 V		20	200	μA
$I_{DD(av)}$	Average supply current from V_{DD} during read or write cycle	Minimum cycle time		32		mA
$I_{DD(av)}$	Average supply current from V_{DD} during read, modify write cycle	Minimum cycle time		32		mA
I_{BB}	Supply current from V_{BB}	V_{BB} = MAX‡, V_{CC} = 5.25 V, V_{DD} = 12.6 V, V_{SS} = 0 V		−5	−100	μA

†All typical values are at T_A = 25°C.
‡MAX = −3.3 V for TMS 4030; −5.5 V for TMS 4060.

capacitance at V_{DD} = 12 V, V_{SS} = 0 V, V_{BB} = NOM, V_{CC} = 5 V, $V_{I(CE)}$ = 0 V, V_I = 0 V, f = 1 MHz, T_A = −55°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$C_{i(ad)}$	Input capacitance address inputs			5	7	pF
$C_{i(CE)}$	Input capacitance clock input	$V_{I(CE)}$ = 10.8 V		18	22	pF
		$V_{I(CE)}$ = −1 V		23	27	
$C_{i(\overline{CS})}$	Input capacitance chip-select input			4	6	pF
$C_{i(data)}$	Input capacitance data input			4	6	pF
$C_{i(R/\overline{W})}$	Input capacitance read/write input			5	7	pF
C_o	Output capacitance			5	7	pF

†All typical values are at T_A = 25°C.

3

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	11.4	12	12.6	V
Supply voltage, V_{SS}		0		V
Supply voltage, V_{BB}	−4.5	−5	−5.5	V
High-level input voltage, V_{IH} (all inputs except chip enable)	2.2		5.5	V
High-level chip-enable input voltage, $V_{IH(CE)}$	V_{DD} −0.6		V_{DD} +1	V
Low-level input voltage, V_{IL} (all inputs except chip enable)	−0.6†		0.6	V
Low-level chip-enable input voltage, $V_{IL(CE)}$	−1†		0.6	V
Refresh time, $t_{refresh}$			1	ms
Operating free-air temperature, T_A	−55		85	°C

†The algebraic convention where the most negative limit is designated as minimum is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions, T_A = −55°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	t_a = guaranteed maximum access time, R_L = 2.2 kΩ to 5.5 V, C_L = 50 pF, Load = 1 Series 74 TTL gate	2.4			V
V_{OL}	Low-level output voltage		V_{SS}		0.4	V
I_{OL}	Low-level output current	t_a = guaranteed maximum access time, C_L = 50 pF, V_{OL} = 0.4 V	5			mA
I_I	Input current (all inputs including I/O except chip enable)	V_I = −0.6 to 5.5 V			10	μA
$I_{I(CE)}$	Chip-enable input current	V_I = −1 to 13.2 V			10	μA
I_{DD}	Supply current from V_{DD}	$V_{IH(CE)}$ = 13.2 V		35	80	mA
I_{DD}	Supply current from V_{DD}, standby	$V_{IL(CE)}$ = 0.6 V		10	200	μA
$I_{DD(av)}$	Average supply current from V_{DD} during read or write cycle	Minimum cycle timing		32		mA
$I_{DD(av)}$	Average supply current from V_{DD} during read, modify write cycle	Minimum cycle timing		32		mA
I_{BB}	Supply current from V_{BB}	V_{BB} = −5.5 V, V_{DD} = 12.6 V, V_{SS} = 0 V		5	100	μA

†All typical values are at T_A = 25°C.

capacitance at V_{DD} = 12 V, V_{SS} = 0 V, V_{BB} = −5 V, $V_{I(CE)}$ = 0 V, V_I = 0 V, f = 1 MHz, T_A = −55°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$C_{i(ad)}$	Input capacitance address inputs			5	7	pF
$C_{i(CE)}$	Input capacitance clock input	$V_{I(CE)}$ = 12 V		24	28	pF
		$V_{I(CE)}$ = 0 V		29	33	
$C_{i(R/\overline{W})}$	Input capacitance read/write input			5	7	pF
$C_{(I/O)}$	I/O terminal capacitance			7	9	pF

†All typical values are at T_A = 25°C.

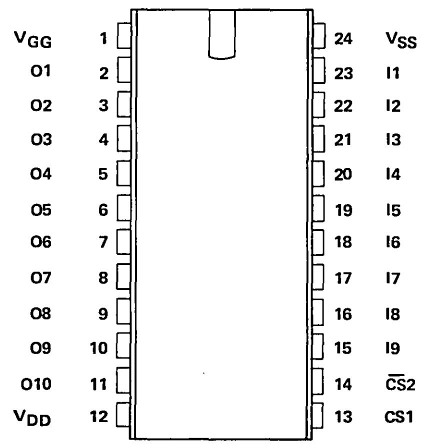
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TMS 2501 JC, NC
64 x 5 x 7 STATIC USASCII CHARACTER GENERATOR

MAY 1975

- Organization . . . 64 Characters of 35 Bits in a 5 x 7 Matrix
- Access Time . . . 250 ns Typical
- Inputs and Outputs Fully TTL-Compatible
- Two Chip-Select Inputs
- 3-State Output Buffers for OR-Ties
- Row Output (Seven 5-Bit Rows in Sequence)

24-PIN CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGES
(TOP VIEW)

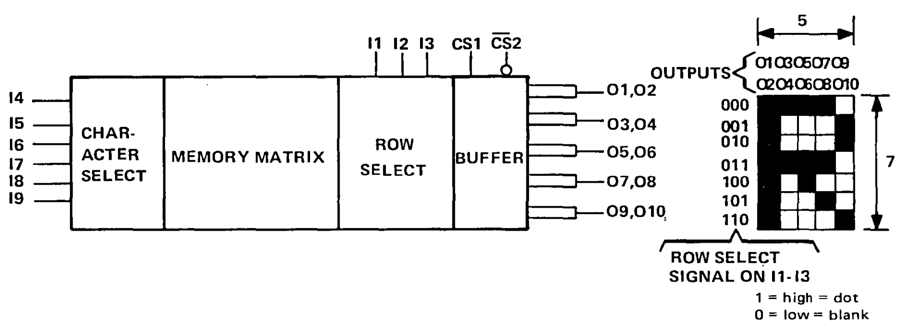


description

The TMS 2501 generates 64 USASCII characters for driving a 5 x 7 matrix display. All inputs can be driven directly from Series 74 TTL circuits and the 3-state push-pull output buffers can drive Series 74 TTL circuits without external resistors. The 5-bit row words appear on the odd-numbered outputs with I9 low and on the even-numbered outputs with I9 high. Outputs O1 and O2, O3 and O4, . . . O9 and O10 must be externally OR-tied in pairs. CS1 must be high and $\overline{\text{CS2}}$ low to enable the device.

The TMS 2501 is offered in 24-pin ceramic (JC suffix) or plastic (NC suffix) packages designed for insertion in mounting-hole rows on 600-mil centers. The devices are characterized for operation from –25°C to 85°C.

functional block diagram



A complete data sheet for the TMS 2500 Series may be obtained by writing directly to:

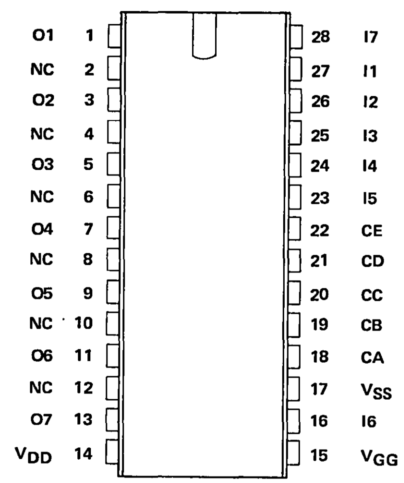
Marketing and Information Services
Texas Instruments Incorporated
P.O. Box 5012 MS 308
Dallas, Texas 75222

TMS 4103 JC, NC
64 x 5 x 7 STATIC USASCII CHARACTER GENERATOR

MAY 1975

- Organization . . . 64 Characters of 35 Bits in a 5 x 7 Matrix
- Access Time . . . 500 ns Typical
- Inputs and Outputs Fully TTL-Compatible
- 7-Bit Input Address
- Open-Drain Output Buffers
- Column Output (Five 7-Bit Columns in Sequence)

28-PIN CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGES
(TOP VIEW)



NC — No Connection

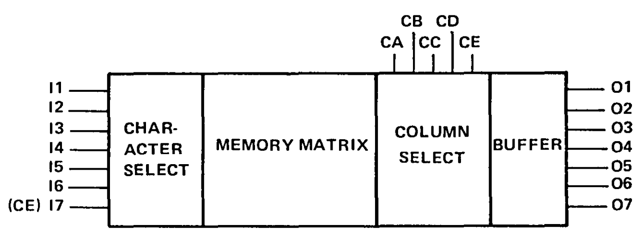
description

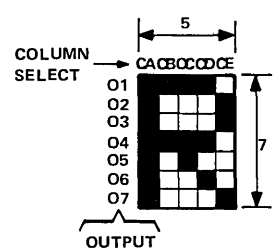
The TMS 4103 generates 64 USASCII characters for driving a 5 x 7 matrix display. Output buffers are open-drain and are capable of driving Series 74 TTL circuits without external resistors. All inputs can be driven directly from Series 74 TTL circuits.

The five 7-bit column words appear on O1 through O7 as column select inputs CA through CE are strobed in sequence with a high level pulse. The device is enabled with a high level on I7.

The TMS 4103 is offered in 28-pin ceramic (JC suffix) or plastic (NC suffix) packages designed for insertion in mounting-hole rows on 600-mil centers. The devices are characterized for operation from −25°C to 85°C.

functional block diagram





A complete data sheet for the TMS 4100 Series may be obtained by writing directly to:

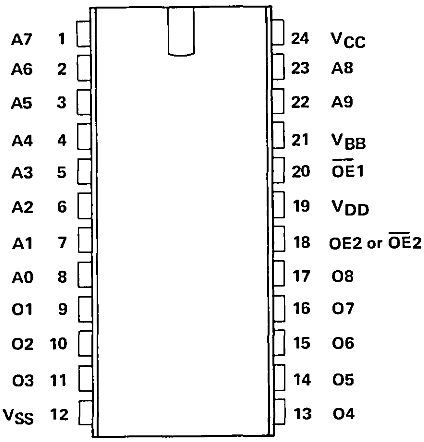
Marketing and Information Services
Texas Instruments Incorporated
P.O. Box 5012 MS 308
Dallas, Texas 75222

TMS 4700 JL, NL
1024-WORD BY 8-BIT READ-ONLY MEMORY

BULLETIN NO. DL-S 7512273, MAY 1975

- 1024 x 8 Organization
- All Inputs and Outputs TTL-Compatible
- Maximum Access Time . . . 450 ns
- Minimum Cycle Time . . . 450 ns
- Typical Power Dissipation . . . 310 mW
- 3-State Outputs for OR-Ties
- Output Enable Control
- Silicon-Gate Technology
- 8-Bit Output for use in Microprocessor Based Systems

24-PIN CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGES
(TOP VIEW)



description

The TMS 4700 JL, NL is an 8,192-bit read-only memory organized as 1024 words of 8-bit length. The device is fabricated using N-channel silicon-gate technology for high speed and simple interface with bipolar circuits. All inputs can be driven by Series 74 TTL circuits with the use of external pull-up resistors and each output can drive one Series 74 TTL circuit without external resistors. The data outputs are three-state for OR-tieing multiple devices on a common bus. Two output-enable controls, one customer programmable, allow data to be read. The option on output enable 2 is explained in the section "Software Package".

The TMS 4700 is designed for high-density fixed-memory applications such as logic-function generation and microprogramming. This ROM is supplied in 24-pin dual-in-line ceramic (JL suffix) and plastic (NL suffix) packages designed for insertion in mounting-hole rows on 600-mil centers. The device is characterized for operation from 0°C to 70°C.

operation

address (A0-A9)

The address-valid interval determines the device cycle time. The 10-bit positive-logic address is decoded on-chip to select one of 1024 words of 8-bit length in the memory array. A0 is the least-significant bit and A9 the most-significant bit of the word address.

output enable ($\overline{OE}1$ and OE2†)

$\overline{OE}1$ is active when it is low. OE2 can be programmed, during mask fabrication, to be active with a high or a low level input. When both output enables are active, all eight outputs are enabled and the eight-bit addressed word can be read. When either output enable is not active, all eight outputs are in a high-impedance state.

data out (O1-O8)

The eight outputs must be enabled by both output enable controls before the output word can be read. Data will remain valid until the address is changed or the outputs are disabled. When disabled, the three-state outputs are in a high-impedance state. The outputs will drive TTL circuits without external components.

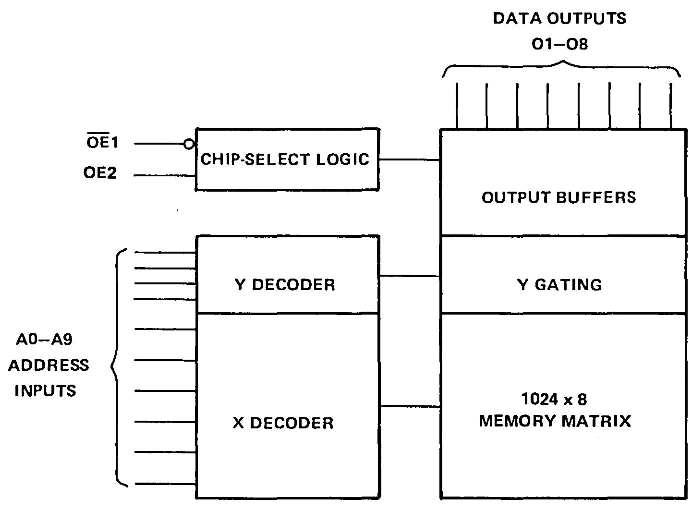
†Symbol OE2 assumes output enable 2 is programmed active high. If active low, the symbol would be $\overline{OE}2$.

PRELIMINARY DATA SHEET:
Supplementary data may be published at a later date.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TMS 4700 JL, NL
1024-WORD BY 8-BIT READ-ONLY MEMORY

functional block diagram



3

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{CC} (see Note 1)	−0.3 V to 20 V
Supply voltage, V_{DD} (see Note 1)	−0.3 V to 20 V
Supply voltage, V_{SS} (see Note 1)	−0.3 V to 20 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−55°C to 125°C

NOTE 1: Under absolute maximum ratings, voltage values are with respect to the normally most positive supply, V_{BB} (substrate). Throughout the remainder of this data sheet voltage values are with respect to V_{SS}.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{BB}	−4.75	−5	−5.25	V
Supply voltage, V_{CC}	4.75	5	5.25	V
Supply voltage, V_{DD}	11.4	12	12.6	V
Supply voltage, V_{SS}		0		V
High-level input voltage, V_{IH}	3.3		V_{CC}	V
Low-level input voltage, V_{IL}	V_{SS}		0.8	V
Read cycle time, $t_{c(rd)}$	430			ns
Output-enable rise time, $t_{r(\overline{OE}1)}$ and $t_{r(OE2)}$		10	20	ns
Output-enable fall time, $t_{f(\overline{OE}1)}$ and $t_{f(OE2)}$		10	20	ns
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended supply voltage ranges, T_A = 0°C to 70°C (unless otherwise noted)

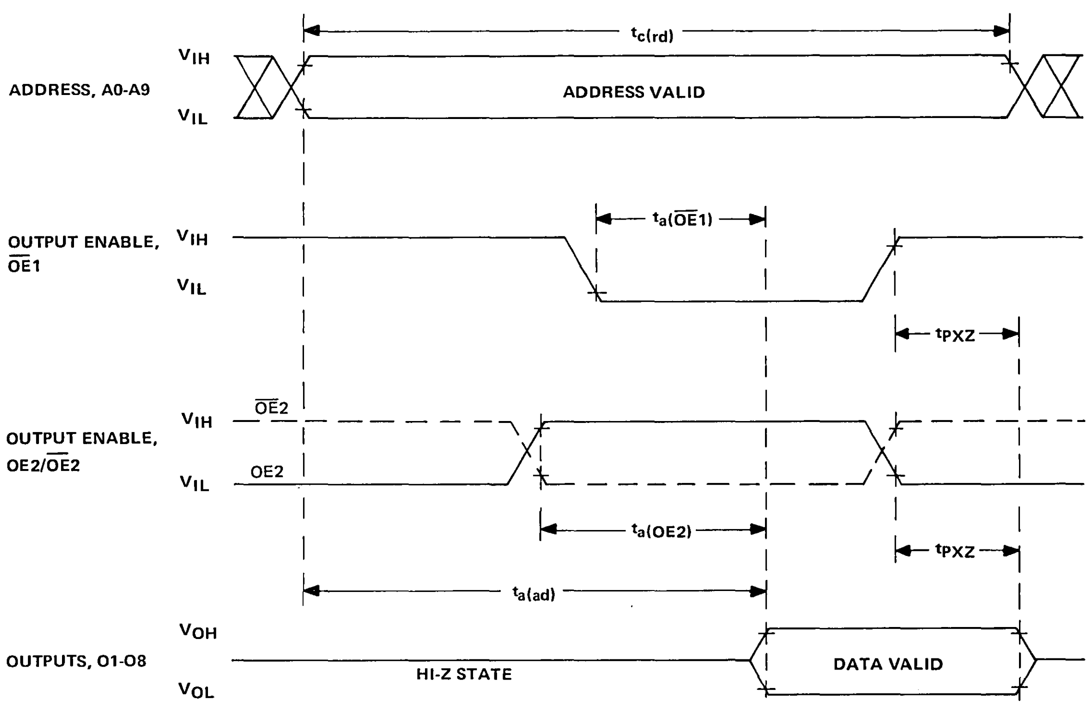
PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −1 mA	3.7			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.45	V
I_I	Input current	V_I = 0 to 6.5 V			±10	μA
I_{BB}	Supply current from V_{BB}	Both output enables active		−0.1		mA
I_{CC}	Supply current from V_{CC}	Both output enables active		2		mA
I_{DD}	Supply current from V_{DD}	Both output enables active		25		mA
P_D	Power dissipation			310		mW

†All typical values are at T_A = 25°C and nominal voltages.

switching characteristics over recommended supply voltage ranges, T_A = 0°C to 70°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{a(ad)}$	Access time from address	C_L = 50 pF, 1 Series 74 TTL load		430	ns
$t_{a(\overline{OE}1)}$	Access time from output enable 1	C_L = 50 pF, 1 Series 74 TTL load		90	ns
$t_{a(OE2)}$	Access time from output enable 2	C_L = 50 pF, 1 Series 74 TTL load		130	ns
t_{PXZ}	Output disable time from either chip enable	C_L = 50 pF, 1 Series 74 TTL load		90	ns

voltage waveforms



NOTE: Timing points are 90% (high) and 10% (low).

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TMS 4700 JL, NL
1024-WORD BY 8-BIT READ-ONLY MEMORY

SOFTWARE PACKAGE

The TMS 4700 JL, NL is a fixed-program memory in which the programming is performed by TI at the factory during the manufacturing cycle to the specific customer inputs supplied in the format shown. The device is organized as 1024 8-bit words with address locations numbered 0 to 1023. Any 8-bit word can be coded as a 2-digit hexadecimal number between 00 and FF. All stored words and addresses in the following format are coded in hexadecimal numbers. In coding, all binary words must be in positive logic before conversion to hexadecimal. O1 is considered the least-significant bit and O8 the most-significant bit. For addresses A0 is least significant and A9 is most significant.

Every card should include the TI Custom Device Number in the form ZAXXXX (4-digit number to be assigned by TI) in columns 75 through 80.

Output enable 2 is customer programmable. Every card should include in column 74 a 1 if the output is to be enabled with a high-level input at $\overline{OE}2$ or a 0 for enabling with a low-level input.

The 1024 coded words must be supplied on 64 cards with 16 2-digit hex numbers per card.

3

CARD	COLUMN	HEXADECIMAL INFORMATION
1	1–9	BLANK
	10	: (ASCII character colon)
	11–12	10 (specifies 16 words per card)
	13	BLANK
	14–16	Hex address of 1st word on 1st card (0th word, address normally 000)
	17–18	BLANK
	19–20	0th word in Hex
	•	
	•	
	•	
	49–50	15th word in Hex
	51–73	BLANK
64	1–9	BLANK
	10	: (ASCII character colon)
	11–12	10
	13	BLANK
	14–16	Hex address of 1st word on 64th card (1008th word, address normally 3F0)
	17–18	BLANK
	19–20	1008th word in Hex
	•	
	•	
	•	
	49–50	1023rd word in Hex
	51–73	BLANK

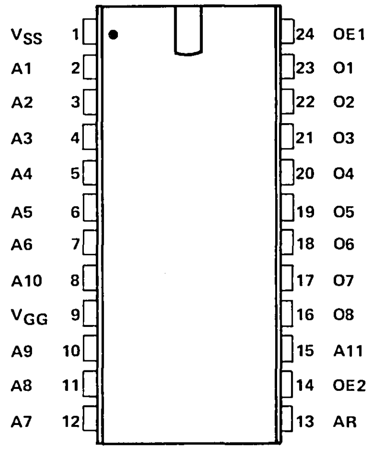
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TMS 4800 JL, NL
16384-BIT READ-ONLY MEMORY

BULLETIN NO. DL-S 7512260, MAY 1975

- 2048 x 8 or 4096 x 4 Organization
- Total TTL-Compatibility
- Maximum Access Time . . . 700 ns
- Minimum Cycle Time . . . 1000 ns
- Typical Power Dissipation . . . 450 mW
- Open-Drain Output for Wire-OR Configurations
- 24-Pin 600-Mil Dual-in-Line Packages
- Two Chip-Enable Controls

24-PIN CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGES
(TOP VIEW)



3

description

The TMS 4800 JL, NL is a 16384-bit read-only memory, organized as either 2048 words of 8-bits or 4096 words of 4-bits. All inputs are TTL-compatible. The eight open-drain outputs must be connected by pull-down resistors to an external negative supply to drive standard TTL circuits. Two output-enable terminals allow each 2048 x 4-bit array to be read independently as 4-bit words or simultaneously as 8-bit words.

Two devices can be OR-tied, with proper choice of programming on the output-enable terminals to be specified by the customer. Addresses may change up to 50 ns after the clock cycle begins. This allows TTL address-decoding circuits to synchronize on the rise of the clock and stabilize during this interval effectively shortening the device read-access time. The TMS 4800 is designed with P-channel enhancement-type technology for high-density, fixed-memory applications such as logic function generation and microprogramming. This ROM is supplied in a ceramic (JL suffix) or plastic (NL suffix) 24-pin package designed for insertion in mounting-hole rows on 600-mil centers.

operation

address read (AR)

Address read constitutes the master timing signal of the device. After AR goes high, address and output enable inputs latch. The address-read clock is high during the address-valid and output-enable-valid intervals. Data out is valid both before and after AR goes low, since enabled outputs latch during the cycle.

address (A1-A11)

Any of the 2048-word addresses are selected by an 11-bit positive-logic binary word, A1 being the least-significant bit progressing through to A11, which is the most-significant bit. Address inputs can change up to 50 ns after the AR clock goes high and must remain valid 250 ns after AR goes high. This input latching feature allows the user to change address while data is being read. These system advantages result from latching of the internal address register during a short address-valid interval.

output enable (OE1 and OE2)

The ROM consists of two side-by-side 2048-word-by-4-bit arrays. OE1 enables output terminals O1 through O4 and OE2 outputs O5 through O8 with the two arrays being enabled independently. The user may choose any of four combinations by enabling with either a low or high level on OE1 or OE2. To read 8-bit words with a single address, both OE1 and OE2 must be enabled. For 8-bit readout, two devices may be OR-tied to increase the effective size of the ROM system by programming complementary enable levels on corresponding device terminals.

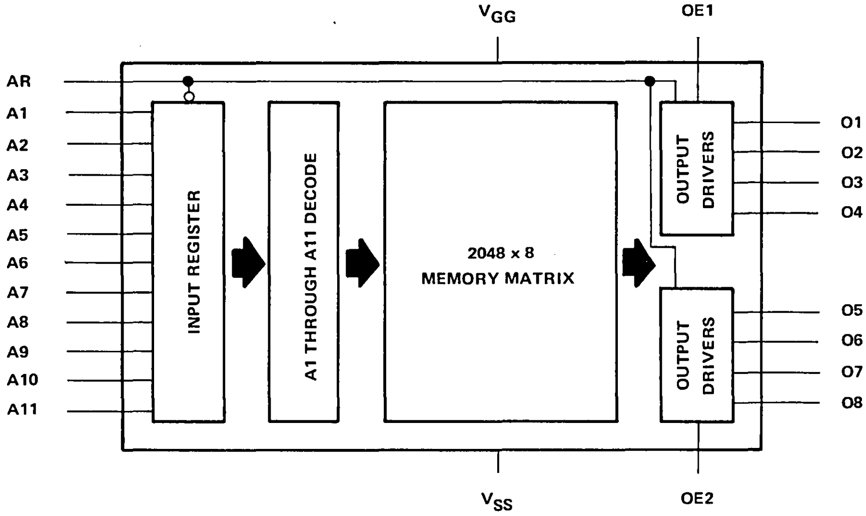
operation (continued)

Output terminals on a single device are OR-tied for a 4096-word x 4-bit organization as follows: O1 to O5; O2 to O6; O3 to O7; and O4 to O8. Since the OE1 and OE2 inputs latch internally, the enable signals may change before or during the output data-valid interval. For additional information on OR-ties, see the section on Expanded Memory Configurations.

data out (O1-O8)

Outputs O1 through O4 are enabled by OE1 with outputs O5 through O8 enabled by OE2. Output transistors are open-drain and compatible with TTL circuits when connected to an external negative supply through a pull-down resistor. All outputs go low immediately after the rise of AR. A disabled output rises to a high level after a propagation delay following the fall of the AR clock if a high logic level was stored. If devices are OR-tied, an enabled output should be read before AR goes low in order to distinguish a stored high from a high coming from the OR-tied disabled output. Because the outputs latch, data on an enabled output remains valid until the next rise of the AR clock.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{GG} (see Note 1)	−20 to 0.3 V
All input voltages (see Note 1)	−20 to 0.3 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−55°C to 150°C

NOTE: 1. Under absolute maximum ratings, voltage values are with respect to V_{SS}(substrate). Throughout the remainder of this data sheet voltage values are with respect to a floating ground.

*COMMENT: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{SS}	4.75	5	5.25	V
Supply voltage, V_{GG}	−11	−12	−13	V
High-level input voltage, V_{IH} (all inputs)	V_{SS} −1.5		V_{SS}	V
Low-level input voltage, V_{IL} (all inputs) (see Note 2)	−4		0.6	V
Read cycle time, $t_{c(rd)}$	1000			ns
Pulse width, address read high, $t_{w(ARH)}$	500		100000	ns
Pulse width, address read low, $t_{w(ARL)}$	450			ns
Address-read rise time, $t_{r(AR)}$			40	ns
Address-read fall time, $t_{f(AR)}$			40	ns
Address-read-high-to-address delay time, $t_{d(ARH\text{-}ad)}$			50	ns
Address-read-high-to-output-enable delay time, $t_{d(ARH\text{-}OE)}$			50	ns
Address hold time, $t_{h(ad)}$	250			ns
Output-enable hold time, $t_{h(OE)}$	250			ns
Operating free-air temperature, T_A	0		70	°C

NOTE 2. The algebraic convention where the most positive limit is designated as maximum is used in this data sheet for logic voltage levels only.

3

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = 2.4 mA	2.5			V
I_{OL}	Low-level output current	V_{OL} = 0.4 V			50	μA
I_I	Input current (all inputs)	V_I = V_{SS}			1	μA
I_{SS}	Supply current from V_{SS}			29	40	mA
I_{GG}	Supply current from V_{GG}			−29	−40	mA

‡All typical values are at T_A = 25°C.

switching characteristics over recommended supply voltage range, T_A = 0°C to 70°C (unless otherwise noted)

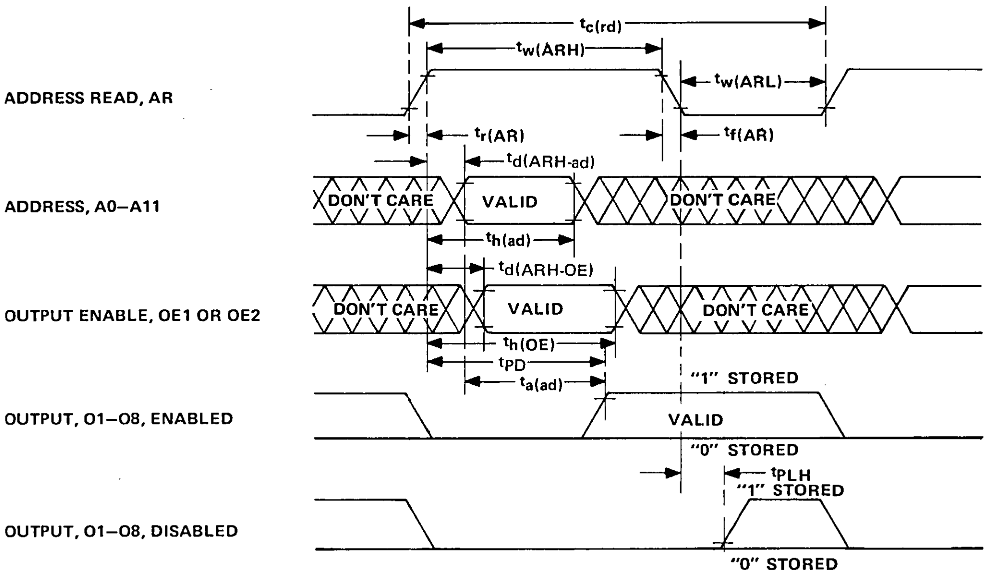
PARAMETER		MIN	TYP‡	MAX	UNIT
$t_{a(ad)}$	Access time from address		550	700	ns
t_{PLH}	Propagation delay time, low-to-high level output from address read (output disabled)	200			ns
t_{PD}	Propagation delay time from address read to data valid		600	750	ns

‡Typical values are measured at V_{SS} = 5 V, V_{GG} = −12 V, and T_A = 25°C.

NOTES: 3. Enabled outputs remain valid until next AR pulse. Disabled outputs may be considered valid until 200 ns after the high-to-low transition of AR.

4. All rise and fall times are ≤20 ns.

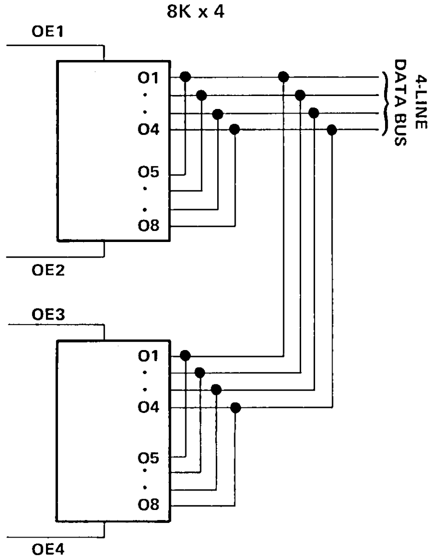
voltage waveforms



3

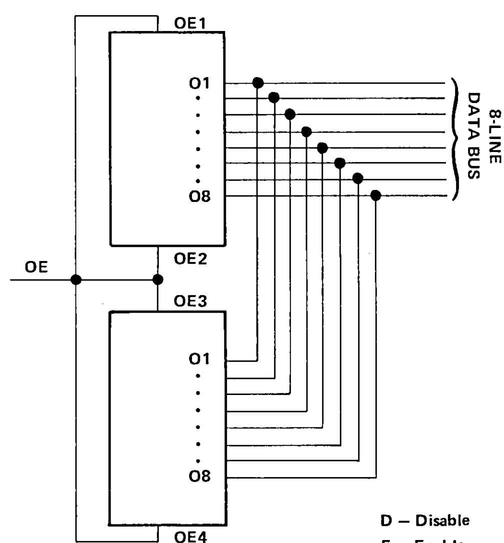
EXPANDED READ-ONLY MEMORY CONFIGURATIONS

8K x 4



WORDS	OE1	OE2	OE3	OE4
0–2048	E	D	D	D
2049–4096	D	E	D	D
4097–6144	D	D	E	D
6145–8192	D	D	D	E

4K x 8



D – Disable
E – Enable

WORDS	OE
0–2048	E
2049–4096	D

NOTE: One device programmed to enable with OE1 = OE2 = 1
Other device programmed to enable with OE1 = OE2 = 0

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

SOFTWARE PACKAGE

The TMS 4800 JL, NL is a fixed program memory in which the programming is performed by TI, at the factory during the manufacturing cycle, to the specific customer inputs supplied in the format shown. The device is organized so that it can be used for storing either 2048 words of 8 bits or 4096 words of 4 bits. Words of 8- or 4-bit lengths are read by proper enable levels on OE1 and OE2. Output O1 is the least-significant bit in an 8-bit word, O5 and O1 in 4-bit words. All addresses and stored words in either organization are coded in octal. Any address up to 2048 can be written as a 4-digit octal number. Any 8-bit binary word can be converted to a 3-bit octal number. In coding, all binary words must be in positive logic and right justified before conversion to octal.

Every card must include the following coded information.
Column 73—OE1 enable code
Column 74—OE2 enable code
Columns 75–80 – TI CUSTOM DEVICE NUMBER ZAXXXX (4-DIGIT NUMBER ASSIGNED BY TI)

The output enable (OE) option is programmed on the chip with the customer pattern. A high voltage level enable is specified by a "1" in columns 73 or 74, a low voltage level enable by a "0".

2048-word by 8-bits

Code deck format –

Card	Column	Octal Information
1	1–4	Octal address (N) of 1st output word on 1st card
	5–7	1st stored 8-bit word (in octal)
	8–10	2nd stored 8-bit word (in octal)
	• • •	
	50–52	16th stored 8-bit word (in octal)
2	1–4	Octal address (N + 16) of 1st output word on 2nd card
	5–7	17th stored 8-bit word
	• • •	
	50–52	32nd stored 8-bit word
128	1–4	Octal address (N + 2032) of 1st output word on 128th card
	5–7	2033rd stored 8-bit word
	• • •	
	50–52	2048th stored 8-bit word

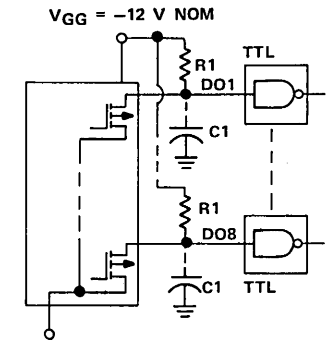
4096-word by 4-bits

Terminals OE1 and OE2 independently enable outputs O1-O4 and O5-O8. Each enable terminal can be programmed to enable with a high or low level input.

To read only 4 bits simultaneously from either set of output terminals, the stored information *must* be coded as an 8-bit positive logic binary word converted to octal. Each 4-bit binary word is right justified before forming the 8-bit word. In coding, words 1 and 2049, 2 and 2050, . . . and 2048 and 4096 are combined (O8-O5 on the left of O4-O1) as 8-bit words and converted to octal as in the case of the 2048 by 8 coding instructions. This coding format also requires 128 cards with 16 octal words (32 4-bit binary words) per card.

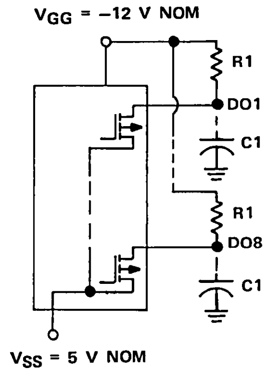
OUTPUT INTERFACE

single resistor TTL interface



R1 = 6.8 kΩ
C1 = 15 pF
MAX TTL FAN-OUT = 1

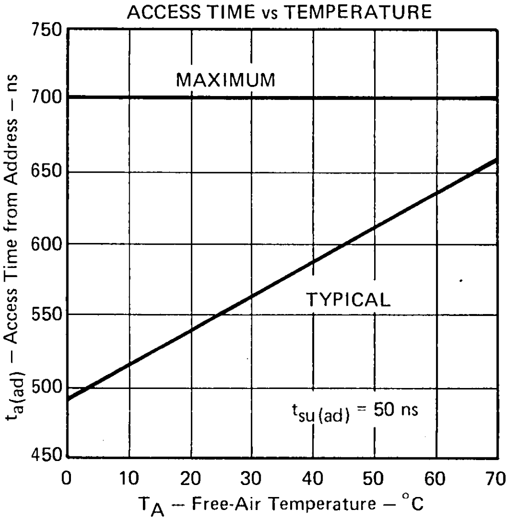
MOS interface



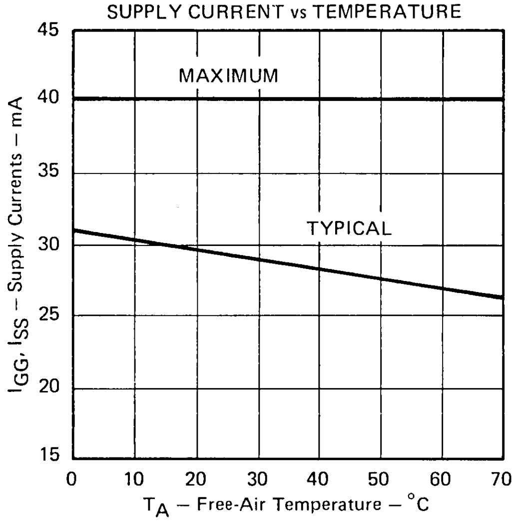
R1 = 12 kΩ
C1 = 10 pF

TYPICAL CHARACTERISTICS

ACCESS TIME vs TEMPERATURE



SUPPLY CURRENT vs TEMPERATURE



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

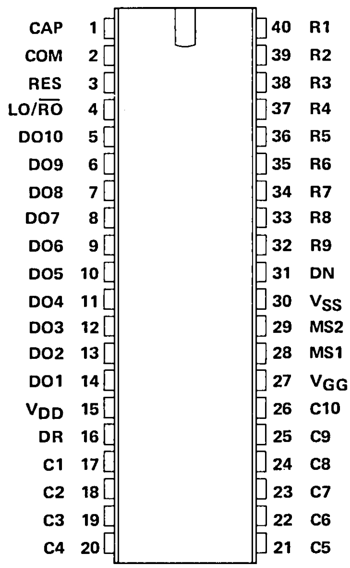
PRINTED IN U.S.A.

TMS 5001 NL
4-MODE DYNAMIC 90-KEY KEYBOARD ENCODER

BULLETIN NO. DL-S 7512274, MAY 1975

- ASCII Logical Bit-Pairing and Typewriter Codes
- ASR33 Teletype Code
- Baudot Paper Tape Punch Code
- N-Key Roll-Over or Lockout Mode
- Data-Ready Pulsed Output
- Internal Oscillator
- Latched Data Outputs
- Adjustable Key-Noise Protection
- Keyboard Column Leakage Compensation
- Compatible with Reed and Mechanical Switches
- TTL-Compatible Inputs and Outputs
- 10-Bit Output Words

40-PIN PLASTIC
DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

The TMS 5001 NL is an MOS LSI dynamic encoder for use with standard keyboards having up to 90 keys. The encoder is pre-programmed to generate in positive logic two ANSI-standard codes – the logical bit pairing and the typewriter codes – the ASR33 teletype code, and the Baudot paper tape code. The device utilizes a 3600-bit ROM (40 x 90 organization), a 9-row by 10-column key-scanning matrix, driver and sense amplifier interface circuits, a control circuit, a shift-register memory, and an on-chip oscillator with frequency determined by an external resistor and capacitor.

The circuit can operate in the N-key roll-over or N-key lockout mode with external logic control. Key-make and key-break noise is ignored after initial key identification because scanning is terminated for a time interval that can be adjusted with another external capacitor at the delay-node terminal.

One of four key modes is selected by proper input levels at two mode-select terminals. A data-ready pulse is generated to indicate that a key is depressed, the binary word has been encoded, and that word is available at the I/O terminals.

The control inputs are compatible with Series 74 TTL circuits using pull-up resistors. Each data output can drive one Series 74 TTL circuit without external resistors.

The TMS 5001 NL is offered in a 40-pin dual-in-line plastic (NL suffix) package designed for insertion in mounting-hole rows on 600-mil centers. The device is characterized for operation from 0°C to 70°C.

operation

The TMS 5001 subsystem consists basically of an oscillator, row and column matrix scanners, a control section with memory, and a ROM with buffered outputs.

oscillator

The internal oscillator generates two internal clock signals at the oscillator frequency that control the precharge of the column inputs and drive the row and column scanning counters. The oscillator frequency is set by an external resistor connected between the **resistor** (RES) and **common** (COM) terminals and an external capacitor connected between the **capacitor** (CAP) and **common** (COM) terminals.

PRELIMINARY DATA SHEET:
Supplementary data may be published at a later date.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

operation (continued)

row and column matrix scanners

The keyboard is connected to the **column** (C1-C10) inputs and the **row** (R1-R9) outputs. During one half of an oscillator cycle, the column inputs and row outputs are precharged to a negative voltage. In the next half-cycle, the modulo-10-counter column scanner enables one of the ten column-input gates and the modulo-9-counter row scanner allows one row to be connected to V_{SS} (nominally 5 V) through an MOS transistor having an impedance of about 600 ohms. If the keyboard switch for that row and column is closed, the column input line capacitance discharges through the MOS load to V_{SS}. At a voltage V_{SH} (near V_{SS}) the key closure is detected and scanning immediately stops. The row and column position is uniquely identified and stored as a single bit in a 90-bit shift register (see control section). Any single key depression is detected within one keyboard scan cycle, which is 90 oscillator or clock cycles. Within one-half clock cycle after detection, the output word becomes valid at the **data out** (DO1-DO10) terminals.

In the roll-over mode, two clock cycles plus one delay-node interval after detection of a depressed key the scanning operation resumes and the next depressed-key location is detected and stored in the memory. Any new output word becomes valid one-half clock cycle after detection. If multiple keys are depressed simultaneously, the scanners will ultimately locate and store all locations in the memory and each output word will become valid in rapid sequence.

In the lockout mode as the delay node voltage drops through V_{SL}, scanning does not resume until the first key is released and the first output remains valid until the second depressed key is detected. Thus the second and subsequent depressed keys are ignored until the first key is released.

In either mode when a key is released, scanning in the next cycle is halted when that key location is reached. The halt signal is obtained from the information in the memory identifying that key location. Key-release noise is therefore ignored until the delay node again precharges to V_{SL}. Then scanning resumes and the next depressed key is identified and its location stored in the memory.

control section

The **delay node** (DN) terminal voltage controls the time during which scanning stops after key detection. An external capacitor may be connected between DN and V_{DD} to lengthen this delay. Key-noise immunity can therefore be adjusted according to the key-switch characteristics.

A high-level **data ready** (DR) output pulse having a length of one clock cycle appears one-half clock cycle after the output data becomes valid to indicate that the encoded output word is available at the ten outputs.

The **lockout/roll-over** (LO/$\overline{\text{RO}}$) terminal places the device in the lockout operating mode when the LO/$\overline{\text{RO}}$ input is high or in the roll-over mode when LO/$\overline{\text{RO}}$ is low.

ROM and output buffers

The row counter output addresses the ROM to generate a unique 10-bit binary word for each of the four modes and each of the 90 key positions. One of the four modes is selected by combinations of high- and low-level inputs at the **mode select** terminals (MS1 and MS2) as shown in the Character Output Charts.

The **data outputs** (DO1-DO8) can drive Series 74 TTL circuits without external resistors. Output data becomes valid within one-half clock cycle after a key is detected.

In the lockout mode, output words are latched and data remains valid until all three of the following events occur: 1) the key is released, 2) the delay node precharges to V_{SL} and scanning starts, and 3) a new key is depressed and detected.

In the roll-over mode, output data remains valid only until the delay node charges to V_{SL} and another key is detected. The DR pulse is generated within one cycle after key detection.

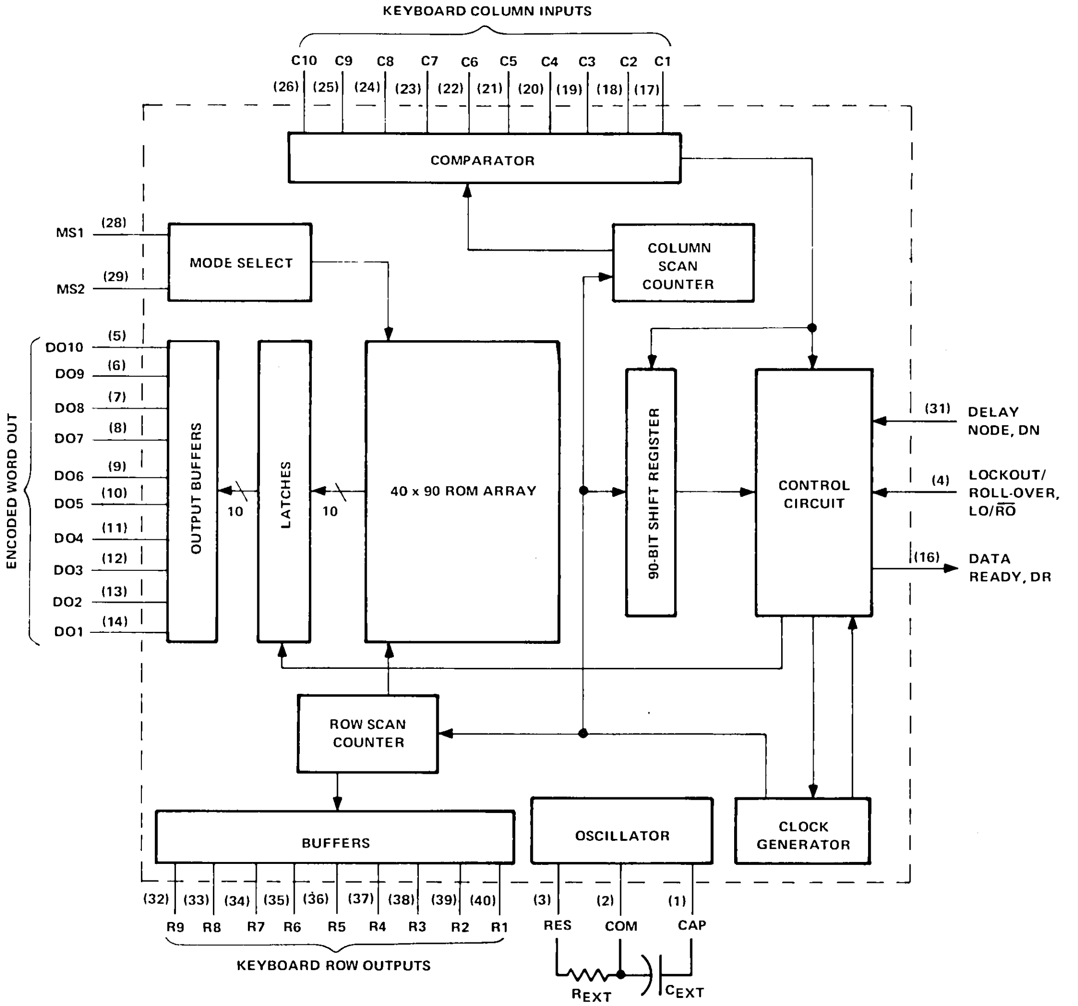
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{DD} (see Note 1)	−20 V to 0.3 V
Supply voltage, V_{GG} (see Note 1)	−20 V to 0.3 V
Input voltages (all inputs) (see Note 1)	−20 V to 0.3 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−55°C to 150°C

NOTE 1: Under absolute maximum ratings, voltage values are with respect to the normally most positive supply, V_{SS} (substrate). Throughout the remainder of this data sheet voltage values are with respect to V_{DD}.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

functional block diagram



TMS 5001 NL
4-MODE DYNAMIC 90-KEY KEYBOARD ENCODER

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		0		V
Supply voltage, V_{GG}	−11	−12	−13	V
Supply voltage, V_{SS}	4.75	5	5.25	V
High-level input voltage (MS and LO/$\overline{\text{RO}}$ inputs), V_{IH}	V_{SS} −1.6		V_{SS}	V
Low-level input voltage (MS and LO/$\overline{\text{RO}}$ inputs), V_{IL}			V_{SS} −3.9	V
Oscillator frequency, f_{osc}	10		100	kHz
Operating free-air temperature, T_A	0		70	°C

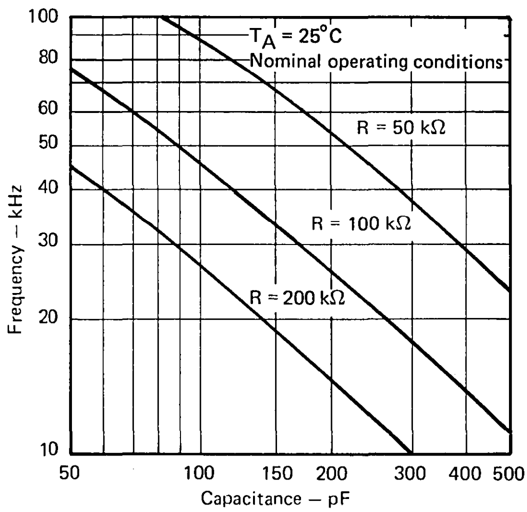
electrical characteristics over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
High-level sense voltage, V_{SH}		V_{SS} −2.2	V_{SS}	V
Low-level sense voltage (see Note 2), V_{SL}			V_{SS} −7.8	V
High-level output voltage, data ready and DO outputs, V_{OH}	I_{OH} = 100 μA	V_{SS} −1	V_{SS}	V
Low-level output voltage, data ready and DO outputs, V_{OL}	I_{OL} = 1.6 mA	0	0.5	V
Precharge voltage at column inputs (see Note 2)			V_{GG} +7.5	V
Supply current from V_{GG}, I_{GG}			−42	mA
Row or column line capacitance	f = 100 kHz		1000	pF

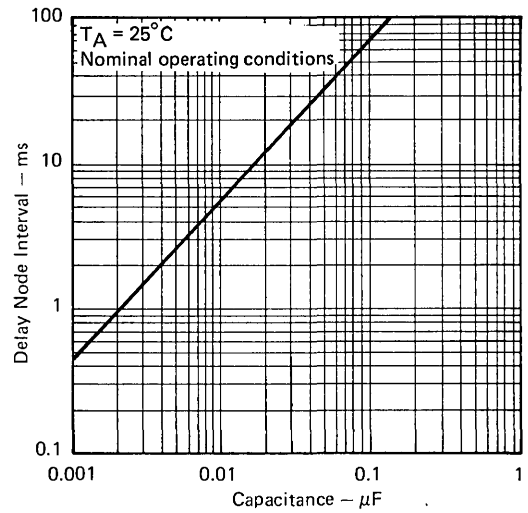
NOTE 2: The algebraic convention where the most positive (least negative) limit is designated as maximum is used in this data sheet for sense and precharge voltage levels only.

TYPICAL OPERATING CHARACTERISTICS

OSCILLATOR FREQUENCY vs EXTERNAL RESISTANCE AND CAPACITANCE



DELAY NODE INTERVAL vs EXTERNAL CAPACITANCE



3

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

character output charts

TYPEWRITER PAIRING

	C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	MODE†
R1	ESC	2	ETX	4	NUL	6	7	8	9	0	0
	ESC	@	ETX	$	NUL	^	&	*	(	)	1
	ESC		ETX		NUL						2
	ESC	2	ETX	4	NUL	6	7	8	9	0	3
R2	1		3	R	5						0
	!		#	R	%						1
				DC2							2
	1		3	r	5						3
R3	Q	W	E	F	T	Y	U	I	O	P	0
	Q	W	E	F	T	Y	U	I	O	P	1
	DC1	ETB	ENQ	ACK	DC4	EM	NAK	HT	SI	DLE	2
	q	w	e	f	t	y	u	i	o	p	3
R4	A	S	D	V	G	H	J	K	L		0
	A	S	D	V	G	H	J	K	L		1
	SOH	DC3	EOT	SYN	BEL	BS	LF	VT	FF		2
	a	s	d	v	g	h	j	k	l		3
R5	Z	X	C	SP	B	N	M				0
	Z	X	C	SP	B	N	M				1
	SUB	CAN	ETX	SP	STX	SO	CR				2
	z	x	c	SP	b	n	m				3
R6	/	9	8	7	LF	{	'	/	.	,	0
	/	9	8	7	LF	}	"	?	>	<	1
					LF						2
	/	9	8	7	LF	{	'	/	.	,	3
R7	#	6	5	4	CR		[			;	0
	#	6	5	4	CR		]			:	1
					CR						2
	#	6	5	4	CR		[			;	3
R8	+	3	2	1	DEL						0
	+	3	2	1	DEL						1
					DEL						2
	+	3	2	1	DEL						3
R9	-	.	0	,	\			'	=	-	0
	-	.	0	,	!			~	+	—	1
					FS						2
	-	.	0	,	\			'	=	-	3

†MODE	MS1	MS2
0	L	L
1	L	H
2	H	L
3	H	H

LOGICAL BIT PAIRING

	C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	MODE†
R1	ESC		ETX	4	NUL						0
	ESC		ETX	$	NUL						1
	ESC		ETX		NUL						2
	ESC		ETX	4	NUL						3
R2	1	2	3	R	5	6	7	8	9	0	0
	!	"	#	R	%	&	'	(	)		1
				DC2							2
	1	2	3	r	5	6	7	8	9	0	3
R3	Q	W	E	F	T	Y	U	I	O	P	0
	Q	W	E	F	T	Y	U	I	O	P	1
	DC1	ETB	ENQ	ACK	DC4	EM	NAK	HT	SI	DLE	2
	q	w	e	f	t	y	u	i	o	p	3
R4	A	S	D	V	G	H	J	K	L		0
	A	S	D	V	G	H	J	K	L		1
	SOH	DC3	EOT	SYN	BEL	BS	LF	VT	FF		2
	a	s	d	v	g	h	j	k	l		3
R5	Z	X	C	SP	B	N	M				0
	Z	X	C	SP	B	N	M				1
	SUB	CAN	ETX	SP	STX	SO	CR				2
	z	x	c	SP	b	n	m				3
R6	/	9	8	7	LF			/	.	'	0
	/	9	8	7	LF			?	>	<	1
					LF						2
	/	9	8	7	LF			/	.	,	3
R7	#	6	5	4	CR	]		:	;		0
	#	6	5	4	CR	}		*	+		1
					CR	GS					2
	#	6	5	4	CR	]		:	;		3
R8	+	3	2	1	DEL	_	[	@			0
	+	3	2	1	DEL	_	{	'			1
					DEL	US	ESC	NUL			2
	+	3	2	1	DEL	_	[	@			3
R9	-	.	0	,	\	^	-				0
	-	.	0	,	!	~	=				1
					FS	RS					2
	-	.	0	,	\	^	-				3

†MODE	MS1	MS2
0	L	L
1	L	H
2	H	L
3	H	H

3

TMS 5001 NL
4-MODE DYNAMIC 90-KEY KEYBOARD ENCODER

character output charts

BAUDOT

	C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	MODE†
R1		LF		FIGS		SP	LTRS	LF	CR	P	0, 1, 2, 3
R2	Q	W	E		R	T	Y	U	I	O	0, 1, 2, 3
R3											0, 1, 2, 3
R4											0, 1, 2, 3
R5											0, 1, 2, 3
R6	A	S	D	F		G	H	J	K	L	0, 1, 2, 3
R7	FIGS	Z	X	C			V	B	N	M	0, 1, 2, 3
R8	LTRS	LF	CR	P							0, 1, 2, 3
R9	CR	LF	LTRS	SP			P	CR	LF	LTRS	0, 1, 2, 3

†MODE	MS1	MS2
0	L	L
1	L	H
2	H	L
3	H	H

ASR33

	C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	MODE†
R1	ESC		ETX	4	NUL						0
	ESC		ETX	$	NUL						1
	ESC		ETX		NUL						2
	ESC		ETX		NUL						3
R2	1	2	3	R	5	6	7	8	9	0	0
	!	"	#		%	&	'	(	)		1
				DC2							2
											3
R3	Q	W	E	F	T	Y	U	I			0
											1
	DC1	ETB	ENQ	ACK	DC4	EM	NAK	HT			2
											3
R4	A	S	D	V	G	H	J			K	0
										[	1
	SOH	DC3	EOT	SYN	BEL	BS	LF			VT	2
										ESC	3
R5	Z	X	C	SP	B			N	M	L	0
				SP				^	]	\	1
	SUB	CAN	ETX	SP	STX			SO	CR	FF	2
				SP				RS	GS	FS	3
R6	/	9	8	7	LF			/	.	,	0
	/	9	8	7	LF			?	>	<	1
					LF						2
	/	9	8	7	LF						3
R7	#	6	5	4	CR			:	;		0
	#	6	5	4	CR			*	+		1
					CR						2
	#	6	5	4	CR						3
R8	+	3	2	1	DEL				P	O	0
	+	3	2	1	DEL				@	_	1
					DEL				DLE	SI	2
	+	3	2	1	DEL				NUL	US	3
R9	-	.	0	,			-				0
	-	.	0	,			=				1
											2
	-	.	0	,							3

†MODE	MS1	MS2
0	L	L
1	L	H
2	H	L
3	H	H

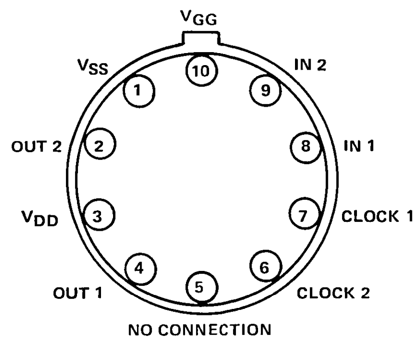
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TMS 3101 LC, NC
DUAL 100-BIT STATIC SHIFT REGISTER

MAY 1975

- DC to 2.5-MHz Operation
- Static Configuration
- Inputs and Outputs Fully TTL-Compatible
- Push-Pull Output Buffers
- Power Supplies . . . 5 V, −12 V
- Low-Threshold Technology

TO-100 HERMETICALLY SEALED PACKAGE
(TOP VIEW)

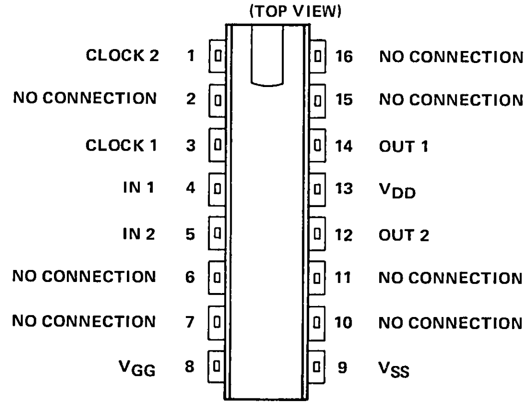


description

The TMS 3101 LC, NC is a dual 100-bit static shift register with independent inputs and outputs for each register. Two external clocks are common to both registers. All inputs and outputs are fully compatible with Series 74 TTL and require no external resistors.

The TMS 3101 is offered in 10-pin TO-100 (LC suffix) and 16-pin dual-in-line plastic (NL suffix) packages. The 16-pin package is designed for insertion in mounting-hole rows on 300-mil centers.

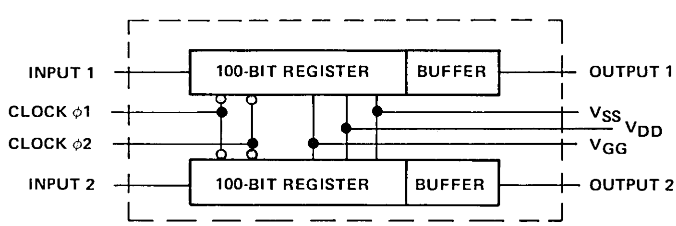
16-PIN PLASTIC DUAL-IN-LINE PACKAGE
(TOP VIEW)



applications

The TMS 3101 can be used in display, terminal, and card read/punch equipment.

functional block diagram



A complete data sheet may be obtained by writing directly to:

Marketing and Information Services
Texas Instruments Incorporated
P.O. Box 5012 MS 308
Dallas, Texas 75222

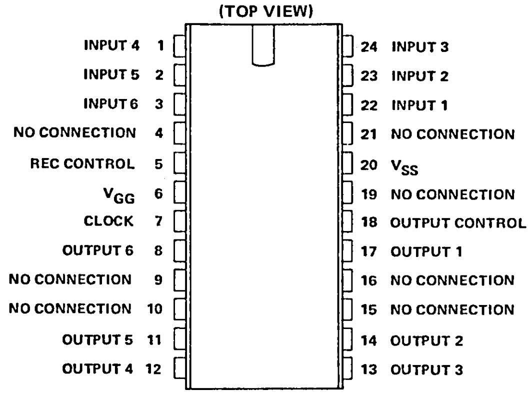
TMS 3112 JC, NC; TMS 3122 JC, NC; TMS 3123 JC, NC
HEX 32-BIT STATIC SHIFT REGISTERS

BULLETIN NO. DL-S 7512261, MAY 1975

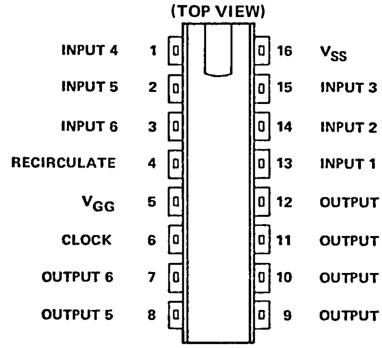
- DC to 2-MHz Operation
- Static Configuration
- Single TTL-Compatible Clock
- Inputs and Outputs are Fully TTL-Compatible
- Single-Ended (Open-Drain) Buffers
- On-Chip Recirculate Logic
- Gated-Output Control (TMS 3112, TMS 3123)
- Power Supplies . . . 5 V, −12 V
- MOS Low-Threshold P-Channel Technology

CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGES

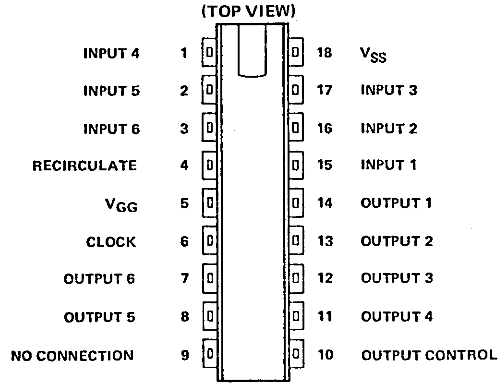
TMS 3112
(TOP VIEW)



TMS 3122
(TOP VIEW)



TMS 3123
(TOP VIEW)



NOTE: The TMS 3122 and TMS 3123 are compatible pin for pin except for output gate control, which necessitates one extra pin.

description

The TMS 3112, TMS 3122, and TMS 3123 JC, NC are 6-channel by 32-bit shift registers on a single monolithic chip with separate inputs and outputs and a common recirculate control. The TMS 3112 and TMS 3123 feature a common output gating control. The clock and all inputs can be driven directly from Series 74 TTL circuits and all outputs are capable of driving one Series 74 TTL circuit.

Cross-coupled inverters (flip-flops) are employed to implement each bit storage location. This static design allows input data rates from dc to 2 MHz and long-term data storage.

P-channel enhancement-type low-threshold processing has been employed to reduce power dissipation and provide simple interfaces with bipolar circuits.

The TMS 3122 and TMS 3123 are offered in 16-pin and 18-pin dual-in-line packages, respectively. The TMS 3112 is offered in a 24-pin dual-in-line package. All three devices are available in ceramic (JC suffix) or plastic (NC suffix) packages. The 16- and 18-pin packages are designed for insertion in mounting-hole rows on 300-mil centers. These devices are characterized for operation from −25°C to 85°C.

applications

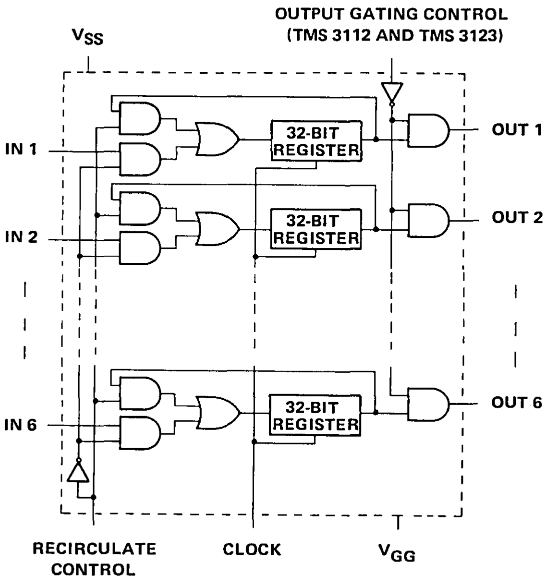
The TMS 3112, TMS 3122 and TMS 3123 can be used in printers, terminals, and peripheral (IBM System 3) applications where 32, 64, or 96 bits of serial storage are needed.

operation

Transfer of data into and out of the shift register occurs on the low-to-high transition of the clock. Input data must be set up a minimum time before the low-to-high transition and must be held for a minimum time after that transition. For long-term data storage, the clock must be maintained high, and in this mode the recirculate and data input levels may change without affecting the data output levels.

Recirculate occurs on the low-to-high clock transition with the recirculate control high. The recirculate control level must be set up a minimum time before this transition and held a minimum time after the transition. Data is entered with the recirculate control low. During recirculation, data is continuously available at the outputs when the output gate control is low. A high level on the output gate control forces all outputs low. Data inputs are inhibited during recirculation.

functional block diagram



NOTE: TMS 3122 does not have output gating.

FUNCTION TABLE

RECIRCULATE	INPUT	FUNCTION
H	L	Recirculate
H	H	Recirculate
L	L	L is written
L	H	H is written

H = high level
L = low level

3

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{GG} (see Note 1)	−20 V to 0.3 V
Clock input voltage (see Note 1)	−20 V to 0.3 V
Data input voltage (see Note 1)	−20 V to 0.3 V
Operating free-air temperature range	−25°C to 85°C
Storage temperature range	−55°C to 150°C

NOTE 1: Under absolute maximum ratings, voltage values are with respect to the normally most-positive supply, V_{SS} (substrate). Throughout the remainder of this data sheet voltage values are with respect to a floating ground.

*Comment: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{GG}	−11	−12	−13	V
Supply voltage, V_{SS}	4.75	5	5.25	V
High-level input voltage, V_{IH}	V_{SS} −1.3		V_{SS}	V
High-level clock voltage, $V_{IH(\phi)}$	V_{SS} −1.3		V_{SS}	V
Low-level input voltage, V_{IL}			V_{SS} −4	V
Low-level clock voltage, $V_{IL(\phi)}$			V_{SS} −4	V
Clock pulse transition time, low-to-high-level, $t_{TLH(\phi)}$			5000	ns
Clock pulse transition time, high-to-low-level, $t_{THL(\phi)}$			5000	ns
Pulse width, clock high, $t_{w(\phi H)}$	300		∞	ns
Pulse width, clock low, $t_{w(\phi L)}$	150		50000	ns
Recirculate pulse width, $t_{w(rec)}$	250			ns
Data setup time, $t_{su(da)}$	60			ns
Recirculate setup time, $t_{su(rec)}$	120			ns
Data hold time, $t_{h(da)}$	60			ns
Recirculate hold time, $t_{h(rec)}$	100			ns
Clock frequency, f_{ϕ}	0		2	MHz
Operating free-air temperature, T_A	−25		85	°C

3

electrical characteristics under nominal operating conditions, T_A = −25°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	R_L = 7.5 kΩ to V_{GG}	V_{SS} −1			V
V_{OL}	Low-level output voltage	R_L = 7.5 kΩ to V_{GG}, $I_{OL} \approx$ −1.6 mA			0.6	V
I_I	Input current (all inputs)	V_I = 0 V			−500	nA
I_{GG}	Supply current from V_{GG}	Load = 1 TTL gate (see Note 2), f = 1 MHz, T_A = 25°C		−15	−25	mA
I_{SS}	Supply current from V_{SS}	Load = 1 TTL gate (see Note 2), f = 1 MHz, T_A = 25°C		25	30	mA
P_D	Power dissipation	Load = 1 TTL gate (see Note 2), f = 1 MHz, T_A = 25°C		425	500	mW
C_i	Input capacitance, all inputs except clock	V_I = V_{SS}, f = 1 MHz		5	7	pF
$C_{i(\phi)}$	Clock input capacitance	$V_{I(\phi)}$ = V_{SS}, f = 1 MHz		6	7	pF

†All typical values are at T_A = 25°C.

NOTE 2: For final test purposes, a worst-case TTL load is simulated by a load of 2.7 kΩ and a capacitance of 10 pF.

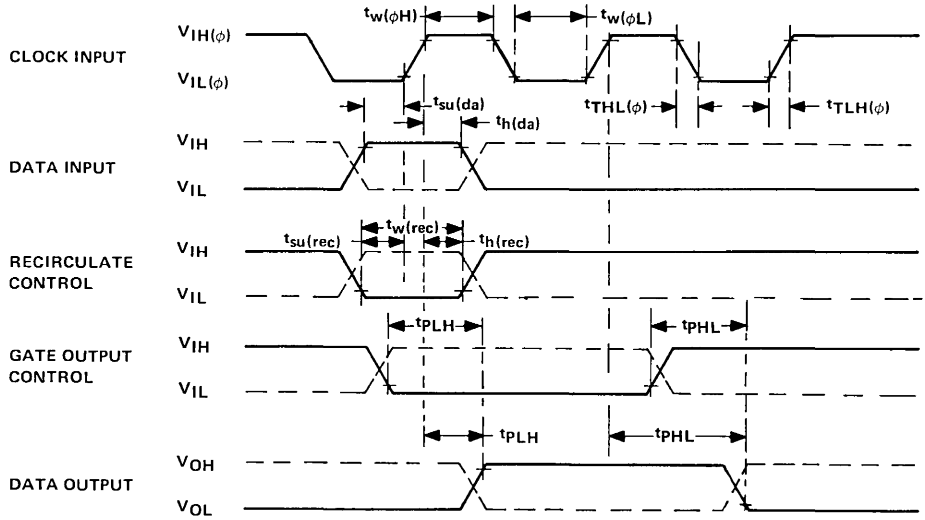
switching characteristics under nominal operating conditions, T_A = −25°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from clock	R_L = 7.5 kΩ to V_{GG}, C_L = 70 pF		350	440	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			350	440	ns
t_{PLH}	Propagation delay time, low-to-high-level output from output control	R_L = 7.5 kΩ to V_{GG}, C_L = 70 pF		180	250	ns
t_{PHL}	Propagation delay time, high-to-low-level output from output control			180	250	ns

†All typical values are at T_A = 25°C.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

voltage waveforms



NOTE: Measurements are made at 90% (high) and 10% (low) timing points.

'75 PRINTED IN U.S.A.

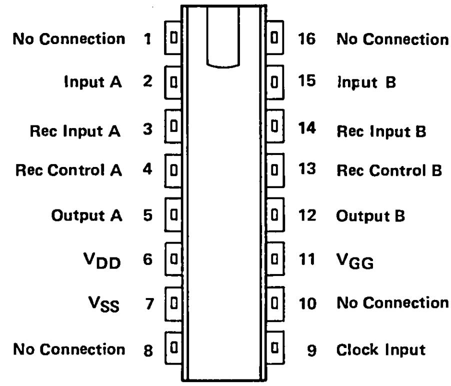
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TMS 3113 JC, NC; TMS 3114 JC, NC
DUAL 133-, 128-BIT STATIC SHIFT REGISTERS

BULLETIN NO. DL-S 7512262, MAY 1975

- DC to 2-MHz Operation
- Static Configuration
- Single TTL-Compatible Clock
- Inputs and Outputs Fully TTL-Compatible
- On-Chip Recirculate Logic
- Power Supplies . . . 5 V, −12 V
- Low-Threshold Technology

16-PIN CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGES
(TOP VIEW)



description

The TMS 3113 JC, NC and TMS 3114 JC, NC are dual static shift registers with independent input, output, and recirculate controls for each register. A single-phase clock is common to both registers. The clock and all inputs can be driven from Series 74 TTL circuits and each output can drive one Series 74 TTL circuit.

Three clocks are generated internally. Cross-coupled inverters (flip-flops) are employed to implement each bit storage location. This static design allows data rates from dc to 2 MHz and long-term data storage.

P-channel enhancement-type low-threshold processing has been employed to reduce power dissipation and provide simple interfaces with bipolar circuits.

The TMS 3113 and TMS 3114 are offered in 16-pin dual-in-line ceramic (JC suffix) or plastic (NC suffix) packages designed for insertion in mounting-hole rows on 300-mil centers. These devices are characterized for operation from −25°C to 85°C.

applications

The TMS 3113 and TMS 3114 can be used in printers, peripherals, and display equipment.

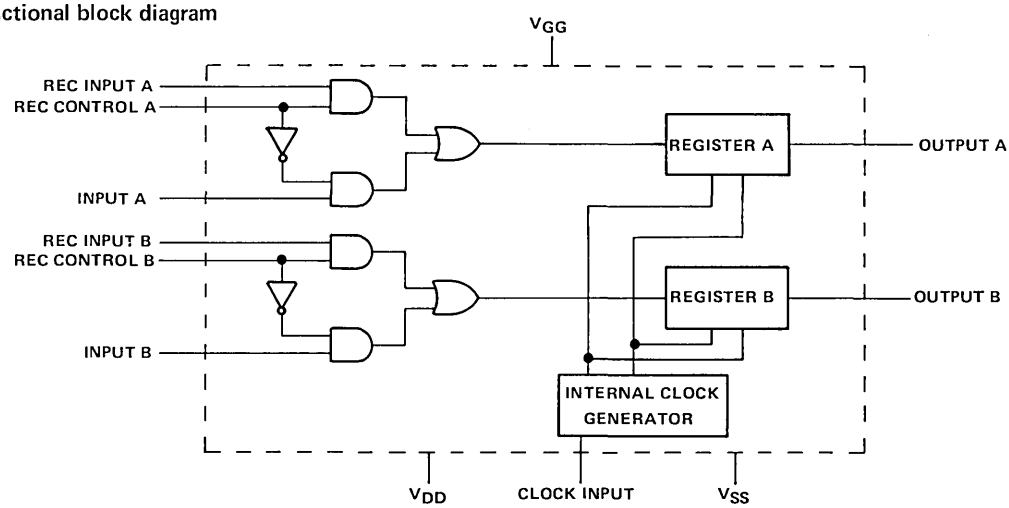
operation

Transfer of data into and out of the shift register occurs on the low-to-high transition of the clock. Input data must be set up a minimum time before the low-to-high transition and must be held for a minimum time after that transition. For long-term data storage, the clock must be maintained high, and in this mode the recirculate and data input levels may change without affecting the data output levels.

Data recirculation is accomplished by externally connecting each output to the corresponding input. Recirculate occurs on the low-to-high clock transition with the recirculate control high. The recirculate control level must be set up a minimum time before this transition and held a minimum time after the transition. Data is entered with the recirculate control low. During recirculation, data is continuously available at the outputs and data inputs are inhibited.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage V_{DD} (see Note 1)	−6 V to 0.3 V
Supply voltage V_{GG} (see Note 1)	−20 V to 0.3 V
Clock input voltage (see Note 1)	−15 V to 0.3 V
Data input voltage (see Note 1)	−15 V to 0.3 V
Operating free-air temperature range	−25°C to 85°C
Storage temperature range	−55°C to 150°C

NOTE 1: Under absolute maximum ratings, voltage values are with respect to the normally most-positive supply, V_{SS} (substrate). Throughout the remainder of this data sheet voltage values are with respect to V_{DD}.

*Comment: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		0		V
Supply voltage, V_{GG}	−11	−12	−13	V
Supply voltage, V_{SS}	4.75	5	5.25	V
High-level input voltage, V_{IH}	3.5			V
High-level clock input voltage, $V_{IH(\phi)}$	3.5			V
Low-level input voltage, V_{IL}			0.6	V
Low-level clock input voltage, $V_{IL(\phi)}$			0.6	V
Clock pulse transition time, low-to-high-level, $t_{TLH(\phi)}$		0.02	5	μs
Clock pulse transition time, high-to-low-level, $t_{THL(\phi)}$		0.02	5	μs
Pulse width, clock high, $t_{w(\phi H)}$	330		∞	ns
Pulse width, clock low, $t_{w(\phi L)}$	130		50000	ns
Data setup time, $t_{su(da)}$	100			ns
Recirculate setup time, $t_{su(rec)}$	100			ns
Data hold time, $t_{h(da)}$	100			ns
Recirculate hold time, $t_{h(rec)}$	150			ns
Clock frequency, f_{ϕ}	0		2	MHz
Operating free-air temperature, T_A	−25		85	°C

electrical characteristics under nominal operating conditions, T_A = −25°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = 0.2 mA	4			V
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA			0.5	V
I_I	Input current (all inputs)	V_I = 0.6 V			−500	nA
I_{GG}	Supply current from V_{GG}	Load = 1 TTL gate (see Note 2)		−17		mA
I_{SS}	Supply current from V_{SS}	Load = 1 TTL gate (see Note 2)		32		mA
P_D	Power dissipation	Load = 1 TTL gate (see Note 2)		360		mW
C_i	Input capacitance, all inputs except clock	V_I = 5 V, f = 1 MHz		8	12	pF
$C_{i(\phi)}$	Clock input capacitance	$V_{I(\phi)}$ = 5 V, f = 1 MHz		9	13	pF

†All typical values are at T_A = 25°C.

NOTE 2: For final test purposes, a worst-case TTL load is simulated by a load of 2.7 kΩ and a capacitance of 10 pF.

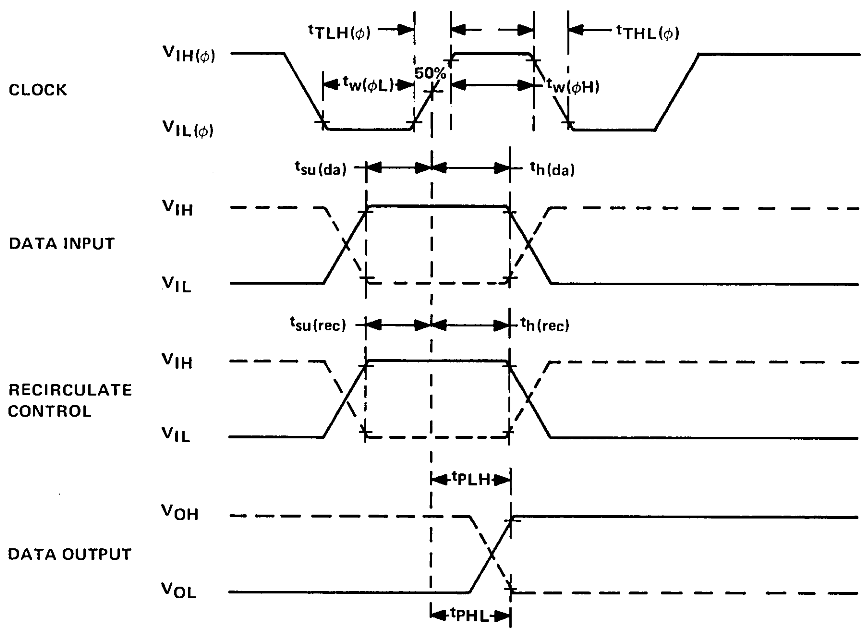
switching characteristics under nominal operating conditions, T_A = −25°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from clock	1 Series 74 TTL Load + 10 pF OR		300	350	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock	10 MΩ + 10 pF (MOS Load) (see Note 3)		300	350	ns

†All typical values are at T_A = 25°C.

NOTE 3: For final test purposes, a worst-case TTL load is simulated by a load of 2.7 kΩ and a capacitance of 10 pF. A worst-case MOS load is simulated by a load of 10 MΩ and 10 pF. All loads are connected between output and V_{SS}.

voltage waveforms



NOTE: Timing points are at 90% (high) and 10% (low) unless otherwise noted.

3

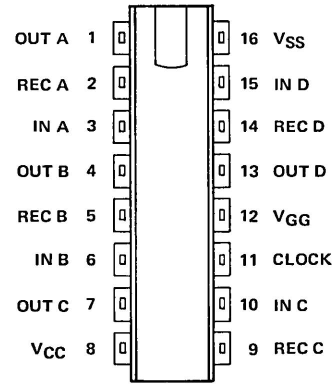
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TMS 3120 JC, NC; TMS 3121 JC, NC
QUADRUPLE 80-, 64-BIT STATIC SHIFT REGISTERS

BULLETIN NO. DL-S 7512267, MAY 1975

- DC to 2.5-MHz Operation
- Static Configuration
- Single TTL-Compatible Clock
- Inputs and Outputs Fully TTL-Compatible
- Push-Pull Output Buffers
- On-Chip Recirculate Logic
- Power Supplies . . . 5 V, −12 V
- Low-Threshold MOS Technology

16-PIN CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGES
(TOP VIEW)



description

The TMS 3120 and TMS 3121 are quad 80-bit and quad 64-bit shift registers with independent inputs, outputs, and recirculate controls for each register. A single-phase clock is common to all registers. The clock and data inputs can be driven from Series 74 TTL circuits and the push-pull output buffers can drive one TTL load or low-level MOS loads without external pull-up resistors.

Cross-coupled inverters (flip-flops) are employed to implement each bit storage location. This static design allows input data rates from dc to 2.5 MHz and long-term data storage.

P-channel enhancement-type low-threshold processing has been employed to reduce power dissipation and provide simple interface with bipolar circuits.

The TMS 3120 and TMS 3121 are offered in 16-pin dual-in-line ceramic (JC suffix) or plastic (NC suffix) packages designed for insertion in mounting-hole rows on 300-mil centers. These devices are characterized for operation from −25°C to 85°C.

applications

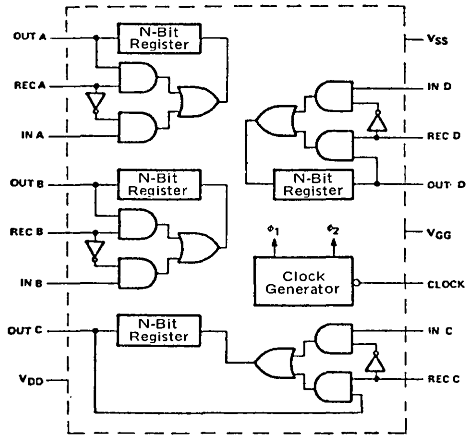
The TMS 3120 can be used in card punch, key-to-tape, key-to-disk, printer, and CRT display equipment for both 40- and 80-column applications. The TMS 3121 is used in general purpose buffer memories.

operation

Transfer of data into and out of the shift register occurs on the high-to-low transition of the clock. Input data must be set up a minimum time before the high-to-low clock transition and must be held for a minimum time after that transition. For long term data storage, the clock must be maintained low, and in this mode the recirculate and data input levels may change without affecting the data output levels.

Recirculate occurs on the high-to-low clock transition with the recirculate control high. The recirculate control must be set up a minimum time before this transition and held a minimum time after the transition. Data is entered with the recirculate control low. During recirculation, data is continuously available at the output and the data input is inhibited.

functional block diagram



3

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{DD} (see Note 1)	−20 V to 0.3 V
Supply voltage, V_{GG} (see Note 1)	−20 V to 0.3 V
Clock input voltage (see Note 1)	−20 V to 0.3 V
Data input voltage (see Note 1)	−20 V to 0.3 V
Operating free-air temperature range	−25°C to 85°C
Storage temperature range	−55°C to 150°C

NOTE 1: Under absolute maximum ratings, voltage values are with respect to the normally most-positive supply, V_{SS} (substrate). Throughout the remainder of this data sheet voltage values are with respect to V_{DD}.

*Comment: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		0		V
Supply voltage, V_{GG}	−11	−12	−13	V
Supply voltage, V_{SS}	4.75	5	5.25	V
High-level input voltage, V_{IH}	V_{SS} −1.6			V
High-level clock input voltage, $V_{IH(\phi)}$	V_{SS} −1.6			V
Low-level input voltage, V_{IL}			0.8	V
Low-level clock input voltage, $V_{IL(\phi)}$			0.8	V
Clock pulse transition time, low-to-high-level, $t_{TLH(\phi)}$			10	μs
Clock pulse transition time, high-to-low-level, $t_{THL(\phi)}$			10	μs
Pulse width, clock high, $t_{w(\phi H)}$	200		100000	ns
Pulse width, clock low, $t_{w(\phi L)}$	200		∞	ns
Data setup time, $t_{su(da)}$	190			ns
Recirculate setup time, $t_{su(rec)}$	190			ns
Data hold time, $t_{h(da)}$	90			ns
Recirculate hold time, $t_{h(rec)}$	90			ns
Clock frequency, f_{ϕ} (see Note 2)	0		2.5	MHz
Operating free-air temperature, T_A	−25		85	°C

NOTE 2: For cascading, data input frequency = 2 MHz maximum.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

electrical characteristics under nominal operating conditions, T_A = –25°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = 100 μA	V_{SS} –1	V_{SS} –0.5		V
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA		0.2	0.4	V
I_I	Input current (all inputs)	V_I = 0			–0.1	μA
I_{GG}	Supply current from V_{GG}	Load = 1 TTL gate (see Note 3) f = 1 MHz, T_A = 25°C		–10	–15	mA
I_{SS}	Supply current from V_{SS}	Load = 1 TTL gate (see Note 3) f = 1 MHz, T_A = 25°C		30	35	mA
P_D	Power dissipation	Load = 1 TTL gate (see Note 3) f = 1 MHz, T_A = 25°C			355	mW
C_i	Input capacitance, all inputs except clock	$V_I = V_{SS}$, f = 1 MHz		3.5	5	pF
$C_{i(\phi)}$	Clock input capacitance	$V_{I(\phi)} = V_{SS}$, f = 1 MHz		3.5	5	pF

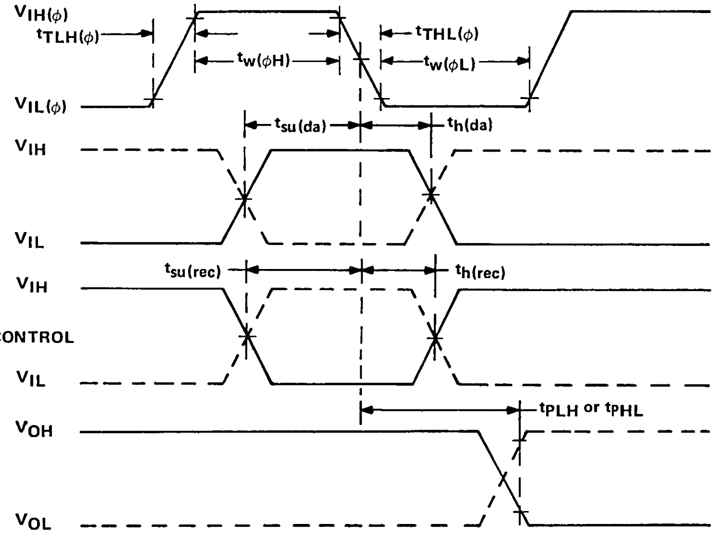
†All typical values are at T_A = 25°C.
NOTE 3: For test purposes, a TTL load is simulated by a load of 2.7 kΩ and 20 pF between the output and V_{SS}.

switching characteristics under nominal operating conditions, T_A = –25°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from clock	1 Series 74 TTL Load + 10 pF (see Note 4)	100	400	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock	1 Series 74 TTL Load + 10 pF (see Note 4)	100	400	ns
t_{PLH}	Propagation delay time, high-to-low-level output from clock	R_L = 10 MΩ, C_L = 10 pF (MOS Load), (see Note 4)	100	300	ns
t_{PHL}	Propagation delay time, low-to-high-level output from clock	R_L = 10 MΩ, C_L = 10 pF (MOS Load), (see Note 4)	100	300	ns

NOTE 4: For final test purposes, a worst-case TTL load is simulated by a load of 2.7 kΩ and a capacitance of 10 pF. A worst-case MOS load is simulated by a load of 10 MΩ and 10 pF. All loads are connected between output and V_{SS}.

voltage waveforms



NOTE: For the clock input and output data, timing points are 90% (high) and 10% (low). All other timing points are at 50%.

3

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

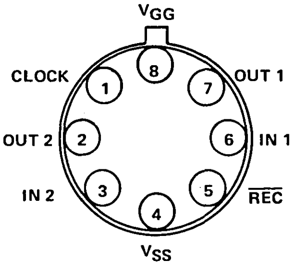
MOS
LSI

TMS 3126, 3127, 3128, 3129, 3130, 3131, 3132 LC, NC
DUAL 96-, 100-, 128-, 132-, 133-, 136-, 144-BIT
STATIC SHIFT REGISTERS

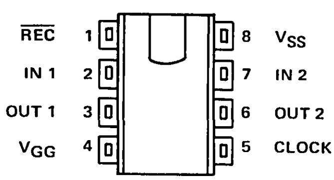
BULLETIN NO. DL-S 7512263, MAY 1975

- DC to 2.5-MHz Operation
- Static Configuration
- Single TTL-Compatible Clock
- Inputs and Outputs Fully TTL-Compatible
- Push-Pull Output Buffers
- On-Chip Recirculate Logic
- Power Supplies . . . 5 V, −12 V
- Seven Standard Bit Lengths

TO-99 HERMETICALLY SEALED PACKAGE
(TOP VIEW)



8-PIN PLASTIC DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

This series is a family of MOS dual static shift registers. These circuits are monolithically constructed by use of thick-oxide techniques and P-channel enhancement-type transistors, which allow TTL-compatibility for ease of system design.

An on-chip clock generator provides three internal phases from a single external TTL-level clock. All inputs including the low-capacitance clock can be driven directly from Series 74 TTL circuits without the need for pull-up resistors. The push-pull outputs are compatible with Series 74 TTL and have a fan-out capability of one TTL load. A current limiter has been incorporated in the output buffers to reduce power dissipation when driving bipolar logic. No external components are needed for TTL interface.

Cross-coupled inverters (flip-flops) are employed to implement each bit storage location. This static design allows input data rates from dc to 2.5 MHz and long-term data storage. Recirculate logic has been incorporated on the chip to simplify system design.

These devices are offered in the TO-99 hermetically sealed package (suffix LC) and in the 8-pin dual-in-line plastic package (suffix NC). The 8-pin dual-in-line package is designed for insertion in mounting-hole rows on 300-mil centers. These devices are characterized for operation from −25°C to 85°C.

applications

Various bit lengths are offered to cover most computer peripheral applications such as printers, buffer memories, and CRT refresh memories.

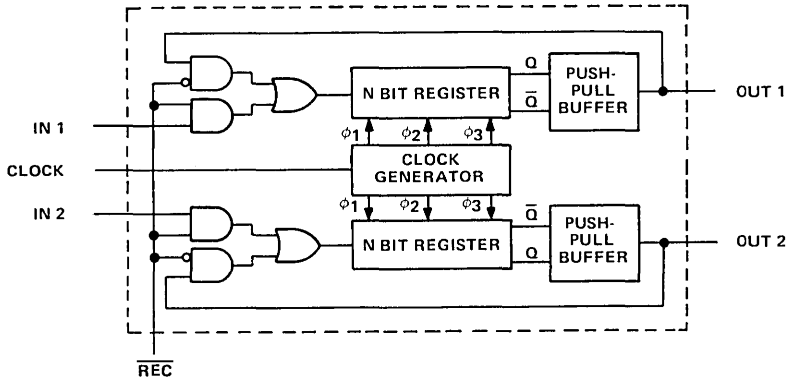
operation

Transfer of data into and out of the shift registers occurs on the low-to-high transition of the clock. Input data must be set up a minimum time before the low-to-high clock transition and must be held for a minimum time after that transition. For long-term data storage, the clock must be maintained high, and in this mode the recirculate and data input levels may change without affecting the data output levels.

Recirculate occurs on the low-to-high clock transition with the recirculate control low. The recirculate control must be set up a minimum time before this transition and held a minimum time after the transition. Data is entered with the recirculate control high. During recirculation, data is continuously available at the output and the data input is inhibited.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{GG} (see Note 1)	−20 V to 0.3 V
Clock input voltage (see Note 1)	−20 V to 0.3 V
Data input voltage (see Note 1)	−20 V to 0.3 V
Operating free-air temperature range	−25°C to 85°C
Storage temperature range	−55°C to 150°C

NOTE 1: Under absolute maximum ratings, voltage values are with respect to the normally most-positive supply, V_{SS} (substrate). Throughout the remainder of this data sheet voltage values are with respect to a floating ground.

*Comment: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{GG}	−11	−12	−13	V
Supply voltage, V_{SS}	4.5	5	5.5	V
High-level input voltage, V_{IH}	V_{SS} −1.8			V
Low-level input voltage, V_{IL}			V_{SS} −3.9	V
Clock pulse transition time, low-to-high level, $t_{TLH(\phi)}$		0.02	5	μs
Clock pulse transition time, high-to-low level, $t_{THL(\phi)}$		0.02	5	μs
Pulse width, clock high, $t_{w(\phi H)}$	300		∞	ns
Pulse width, clock low, $t_{w(\phi L)}$	100		1000000	ns
Recirculate pulse width, $t_{w(rec)}$	125			ns
Data setup time, $t_{su(da)}$	80			ns
Recirculate setup time, $t_{su(rec)}$	100			ns
Data hold time, $t_{h(da)}$	80			ns
Recirculate hold time, $t_{h(rec)}$	25			ns
Clock frequency, f_{ϕ}	0		2.5	MHz
Operating free-air temperature, T_A	−25		85	°C

electrical characteristics under nominal operating conditions, T_A = –25°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = 0.2 mA		4			V
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA				0.4	V
I_I	Input current (all inputs)	V_I = 0.8 V				–500	nA
I_{OS}	Short-circuit output current	V_O = 0 V,	V_{GG} = –11 V			–10	mA
I_{GG}	Supply current from V_{GG}	f = 2.5 MHz,	1 TTL load (see Note 2)		–22	–30	mA
P_D	Power dissipation	f = 2.5 MHz,	1 TTL load (see Note 2)		374	510	mW
C_i	Input capacitance, all inputs except clock	V_I = 5 V,	f = 1 MHz		3.5	5	pF
$C_{i(\phi)}$	Clock input capacitance	$V_{I(\phi)}$ = 5 V,	f = 1 MHz		3.5	5	pF

†All typical values are at T_A = 25°C.
NOTE 2: For test purposes, a TTL load is simulated by a load of 2.7 kΩ and 20 pF between the output and V_{SS}.

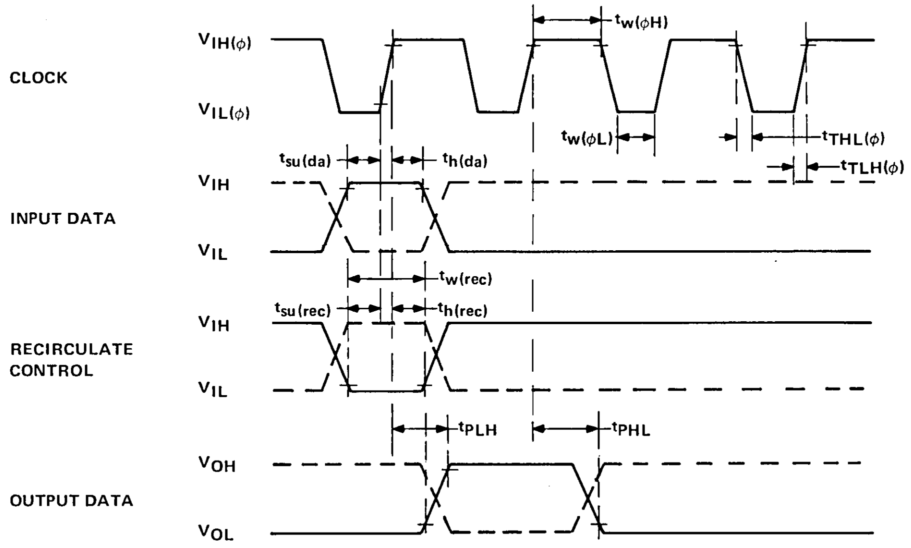
3

switching characteristics under nominal operating conditions, T_A = –25°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from clock	Load = 1 TTL gate (see Note 3)		250	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			250	ns

NOTE 3: For test purposes, a TTL load is simulated by a load of 2.7 kΩ and 20 pF between the output and V_{SS}.

voltage waveforms



NOTE: All timing measurements are made at 10% or 90% points.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PRINTED IN U.S.A. 575

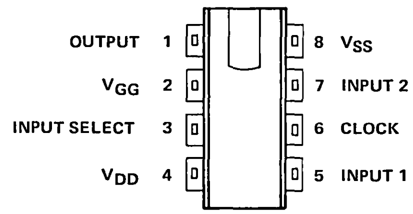
MOS
LSI

TMS 3133 NC
1024-BIT STATIC SHIFT REGISTER

BULLETIN NO. DL-S 7512264, MAY 1975

- DC to 2-MHz Operation
- Static Configuration
- Single TTL-Compatible Clock
- Inputs and Outputs Fully TTL-Compatible
- Push-Pull Output Buffers
- Power Supplies . . . 5 V, −12 V
- MOS Low-Threshold P-Channel Technology

8-PIN PLASTIC
DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

The TMS 3133 NC is a 1024-bit static shift register designed with on-chip pull-up resistors on the inputs and the low-capacitance clock. The input can be driven directly from Series 74 TTL circuits without the use of external components. The push-pull output buffer will drive a TTL or MOS load without external components.

Two input terminals are provided. Data can be entered in either input depending on the state of the input select control. Cross-coupled inverters (flip-flops) are employed to implement each bit storage location. This static design allows input data rates from dc to 2 MHz and long-term data storage.

Ion-implant depletion-type P-channel low-threshold processing has been employed to reduce power dissipation and provide simple interfaces with bipolar circuits.

The TMS 3133 NC is offered in an 8-pin plastic (NC suffix) package designed for insertion in mounting-hole rows on 300-mil centers. The device is characterized for operation from −25°C to 85°C.

applications

The TMS 3133 NC is ideally suited for applications requiring a long serial memory where ease of use and low overhead circuitry are required. These applications include low-cost sequential-access memories, CRT refresh memories, drum memory replacements, and delay lines.

operation

Transfer of data into and out of the shift register occurs on the high-to-low transition of the clock. Input data must be set up a minimum time before the high-to-low transition and must be held for a minimum time after that transition. For long-term data storage, the clock must be maintained low, and in this mode the input select and data input levels may change without affecting the data output levels.

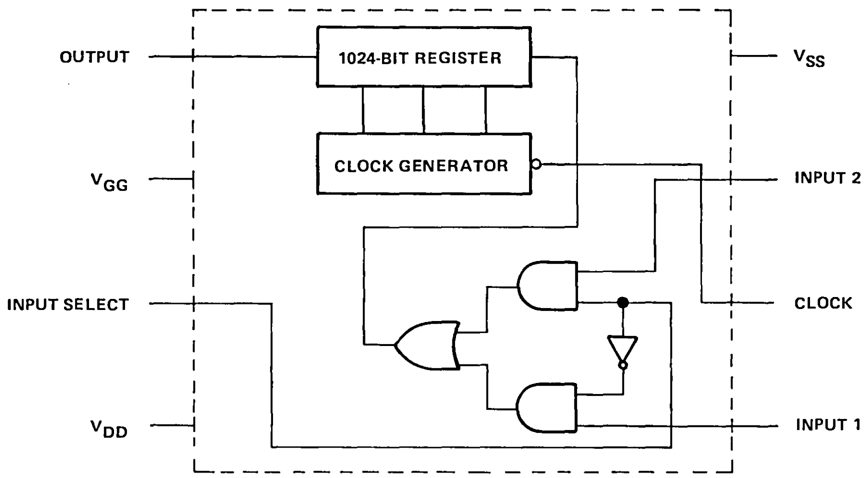
Data recirculation is accomplished by externally connecting the output to either input. Recirculate occurs on the high-to-low clock transition with the input select control set to enter data at the input connected to the output. The input select control level must be set up a minimum time before this transition and held a minimum time after the transition. During recirculation, data is continuously available at the output and the unselected data input is inhibited.

PRELIMINARY DATA SHEET:
Supplementary data may be published at a later date.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TMS 3133 NC
1024-BIT STATIC SHIFT REGISTER

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{DD} (see Note 1)	−20 V to 0.3 V
Supply voltage, V_{GG} (see Note 1)	−20 V to 0.3 V
Clock input voltage (see Note 1)	−20 V to 0.3 V
Data input voltage (see Note 1)	−20 V to 0.3 V
Operating free-air temperature range	−25°C to 85°C
Storage temperature range	−55°C to 150°C

NOTE 1: Under absolute maximum ratings, voltage values are with respect to the normally most-positive supply, V_{SS} (substrate). Throughout the remainder of this data sheet voltage values are with respect to V_{DD}.

*Comment: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		0		V
Supply voltage, V_{GG}	−11	−12	−13	V
Supply voltage, V_{SS}	4.75	5	5.25	V
High-level input voltage, V_{IH} (see Note 2)	V_{SS} −1.4			V
Low-level input voltage, V_{IL}			0.8	V
Clock pulse transition time, low-to-high-level, $t_{TLH(\phi)}$			10	μs
Clock pulse transition time, high-to-low-level, $t_{TLH(\phi)}$			10	μs
Pulse width, clock high, $t_{w(\phi H)}$	200		100000	ns
Pulse width, clock low, $t_{w(\phi L)}$	200		∞	ns
Data setup time, $t_{su(da)}$	100			ns
Input select setup time, $t_{su(sel)}$	100			ns
Data hold time, $t_{h(da)}$	100			ns
Input select hold time, $t_{h(sel)}$	100			ns
Clock frequency, f_{ϕ}	0		2	MHz
Operating free-air temperature, T_A	−25		85	°C

NOTE 2: TTL compatibility of all inputs is ensured by incorporation of internal pull-up resistors on the chip.

electrical characteristics under nominal operating conditions, T_A = –25°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = 100 µA	V_{SS} –1	V_{SS} –0.5		V
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA		0.2	0.4	V
I_I	Input current (all inputs)	V_I = 0 V, V_{SS} = 5 V, T_A = 25°C			–0.8	mA
I_{GG}	Supply current from V_{GG}	f = 1 MHz, Duty cycle = 50%,		–10	–14	mA
I_{SS}	Supply current from V_{SS}	1 Series 74 TTL Load (see Note 3)		35	50	mA
P_D	Power dissipation	T_A = 25°C		250	420	mW
C_i	Input capacitance	V_I = V_{SS}, f = 1 MHz		5	7	pF

†All typical values are at T_A = 25°C.

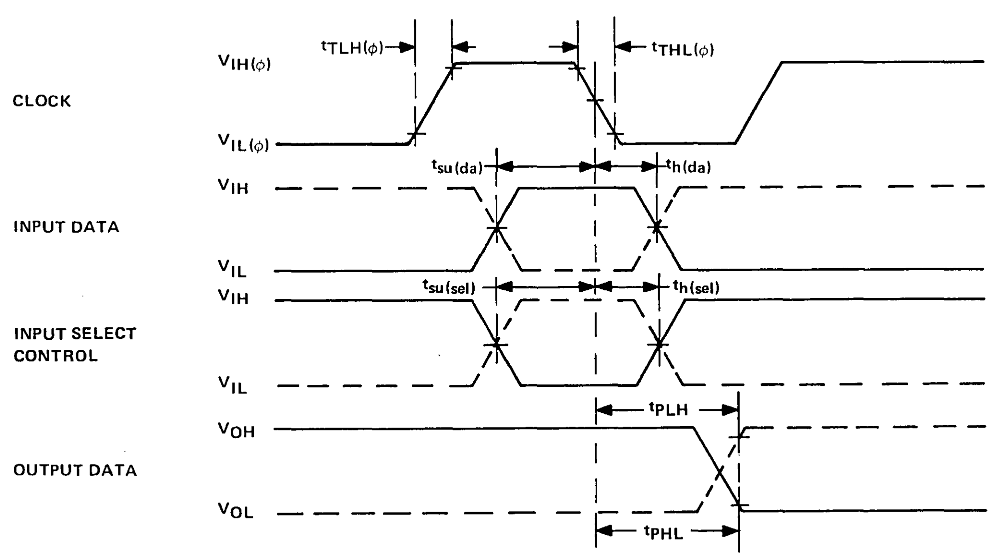
NOTE 3: For final test purposes, a worst-case TTL load is simulated by a load of 2.7 kΩ and a capacitance of 10 pF.

switching characteristics under nominal operating conditions, T_A = –25°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from clock	1 Series 74 TTL Load + 10 pF, OR	110	350	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock	10 MΩ + 10 pF (MOS Load), (see Note 4)	110	350	ns

NOTE 4: For final test purposes, a worst-case TTL load is simulated by a load of 2.7 kΩ and a capacitance of 10 pF. A worst-case MOS load is simulated by a load of 10 MΩ and 10 pF. All loads are connected between output and V_{SS}.

voltage waveforms



3

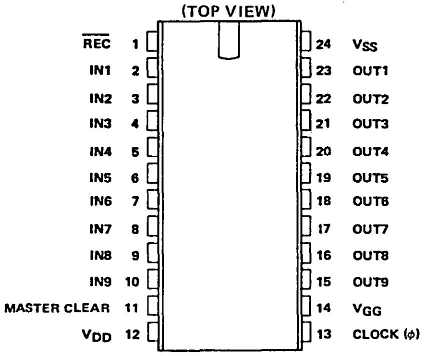
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TMS 3135, 3137, 3138, 3139, 3140 JC, NC
9- BY 80-, 100-, 128-, 132-, 133-BIT STATIC SHIFT REGISTERS

BULLETIN NO. DL-S 7512265, MAY 1975

- DC to 1.5-MHz Operation
- Static Configuration
- Single TTL-Compatible Clock
- Inputs and Outputs Fully TTL-Compatible
- Push-Pull Output Buffers
- On-Chip Recirculate Logic
- Master-Clear Pin
- Power Supplies . . . 5 V, −12 V
- MOS P-Channel Depletion-Type Technology

24-PIN CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGES
(TOP VIEW)



description

3

The TMS 3135, 3137, 3138, 3139, 3140 JC, NC series is a family of MOS 9 x N static shift registers fabricated by means of P-channel ion-implant depletion-load technology. The nine registers permit the use of eight-bit storage plus a marker or parity bit. The design incorporates on-chip pull-up resistors on all inputs including the low-capacitance clock, allowing all inputs to be driven directly from Series 74 TTL without the use of external components. The push-pull output buffer, tied between V_{DD} and V_{SS}, will drive TTL or MOS loads without the use of external components.

An on-chip generator provides three internal phases from the single external TTL clock. Cross-coupled inverters (flip-flops) are employed to implement each bit, providing for static operation as well as dynamic operation from dc to 1.5 MHz. Recirculate logic has been incorporated on the chip to simplify system design. A master-clear pin permits simultaneous clearing of all registers to a low logic level, again simplifying system design.

The TMS 3135, 3137, 3138, 3139, 3140 series is offered in a dual-in-line 24-pin ceramic (JC suffix) or plastic (NC suffix) package designed for insertion in mounting-hole rows on 600-mil centers. These devices are characterized for operation from −25°C to 85°C.

applications

The TMS 3135, 3137, 3138, 3139, and 3140 can be used in printer, terminal, peripheral, CRT display, card punch, key-to-tape, key-to-disk, and general purpose buffer memory applications as replacements for two, four, or nine quad, dual, or single shift registers. Both component and board space cost savings result from higher replication of the serial storage function in a single package.

operation

Transfer of data into and out of the shift registers occurs on the high-to-low transition of the clock. Input data must be set up a minimum time before the high-to-low clock transition and must be held for a minimum time after that transition. For long-term data storage, the clock must be maintained low, and in this mode the recirculate and data input levels may change without affecting the data output levels.

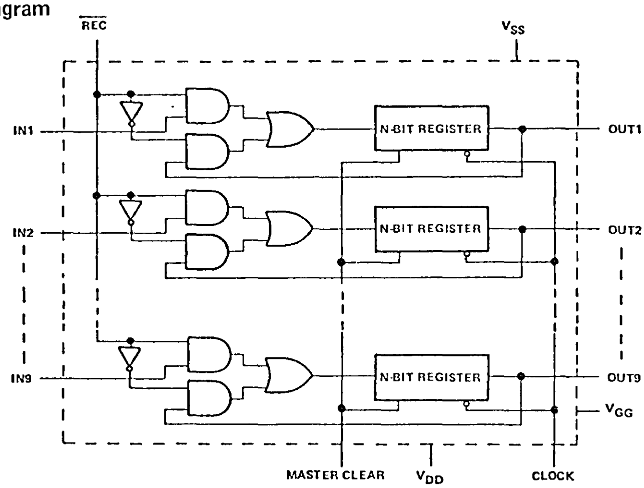
Recirculate occurs on the high-to-low transition with the recirculate control low. The recirculate control must be set up a minimum time before this transition and held a minimum time after the transition. Data is entered with the recirculate control high. During recirculation, data is continuously available at the output and the data input is inhibited.

All nine registers are cleared simultaneously by a high-level pulse on the master-clear pin with the clock in either state. The master-clear input must be inactive (low) at least 250 ns prior to a low-to-high transition of the clock on which transfer of new data is to occur.

PRELIMINARY DATA SHEET:
Supplementary data may be published at a later date.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{DD} (see Note 1)	−20 V to 0.3 V
Supply voltage, V_{GG} (see Note 1)	−20 V to 0.3 V
Clock input voltage (see Note 1)	−20 V to 0.3 V
Data input voltage (see Note 1)	−20 V to 0.3 V
Operating free-air temperature range	−25°C to 85°C
Storage temperature range	−55°C to 150°C

NOTE 1: Under absolute maximum ratings, voltage values are with respect to the normally most-positive supply, V_{SS} (substrate). Throughout the remainder of this data sheet voltage values are with respect to V_{DD}.

*Comment: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		0		V
Supply voltage, V_{GG}	−11	−12	−13	V
Supply voltage, V_{SS}	4.75	5	5.25	V
High-level input voltage, V_{IH} (see Note 2)	V_{SS} −1.4			V
Low-level input voltage, V_{IL} (see Note 2)			0.8	V
Clock pulse transition time, low-to-high level, $t_{THL(\phi)}$			10	μs
Clock pulse transition time, high-to-low level, $t_{TLH(\phi)}$			10	μs
Pulse width, clock high, $t_{w(\phi H)}$	300		100000	ns
Pulse width, clock low, $t_{w(\phi L)}$	300		∞	ns
Width of clear pulse, $t_{w(clr)}$	40			μs
Clear inactive-state setup time, $t_{su(clrL)}$	250			ns
Data setup time, $t_{su(da)}$	100			ns
Recirculate setup time, $t_{su(rec)}$	120			ns
Data hold time, $t_{h(da)}$	100			ns
Recirculate hold time, $t_{h(rec)}$	120			ns
Clock frequency, f_{ϕ}	0		1.5	MHz
Operating free-air temperature, T_A	−25		85	°C

NOTE 2: TTL compatibility of all inputs is ensured by the incorporation of internal pull-up resistors on the chip.

3

electrical characteristics under nominal operating conditions, T_A = –25°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = 100 μA	V_{SS} –1	V_{SS} –0.5		V
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA		0.4	0.6	V
I_I	Input current (all inputs)	V_I = 0		–0.5	–0.8	mA
I_{GG}	Supply current from V_{GG}	Load = 1 TTL gate (see Note 3), f = 1 MHz, T_A = 25°C, Duty cycle = 50%		–9	–12	mA
I_{SS}	Supply current from V_{SS}	Load = 1 TTL gate (see Note 3), f = 1 MHz, T_A = 25°C, Duty cycle = 50%		45	60	mA
P_D	Power dissipation	Load = 1 TTL gate (see Note 3), f = 1 MHz, T_A = 25°C, Duty cycle = 50%		330	450	mW
C_i	Input capacitance, all inputs except clock	V_I = V_{SS}, f = 1 MHz		5	7	pF
$C_{i(\phi)}$	Clock input capacitance	$V_{I(\phi)}$ = V_{SS}, f = 1 MHz		5	7	pF

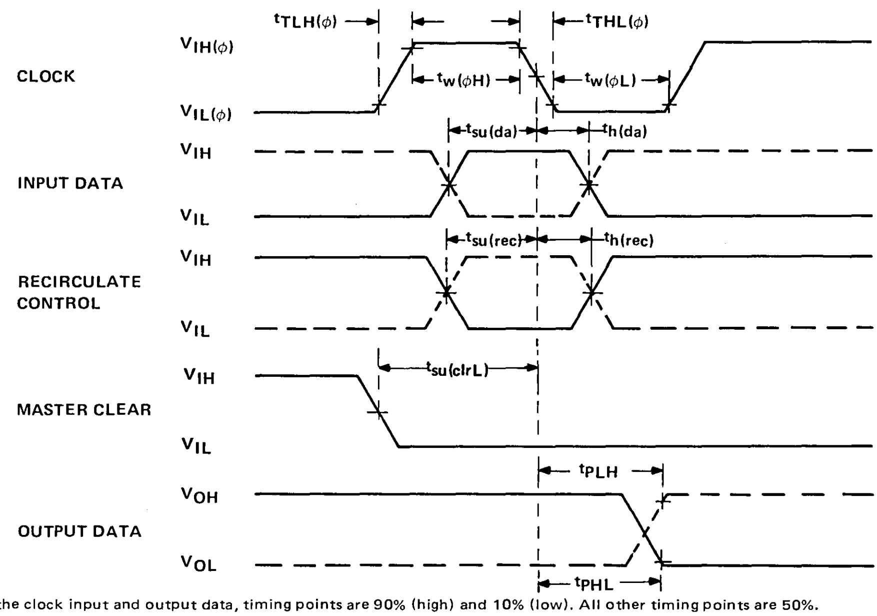
†All typical values are at T_A = 25°C and nominal operating conditions.
NOTE 3: For test purposes, a TTL load is simulated by a load of 2.7 kΩ and 20 pF between the output and V_{SS}.

3

switching characteristics under nominal operating conditions, T_A = –25°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from clock	1 Series 74 TTL load + 10 pF or R_L = 10 MΩ, C_L = 10 pF (MOS load)	110	550	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock		110	550	ns

voltage waveforms



NOTE: For the clock input and output data, timing points are 90% (high) and 10% (low). All other timing points are 50%.

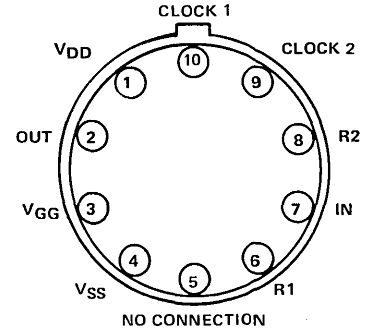
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TMS 3401 LC, NC
512-BIT DYNAMIC SHIFT REGISTER

MAY 1975

- 1-kHz to 5-MHz Operation
- Dynamic Configuration
- Inputs and Outputs Fully TTL-Compatible
- Push-Pull Output Buffers
- Power Supplies . . . 5 V, −12 V
- Low-Threshold Technology

TO-100 HERMETICALLY-SEALED PACKAGE
(TOP VIEW)

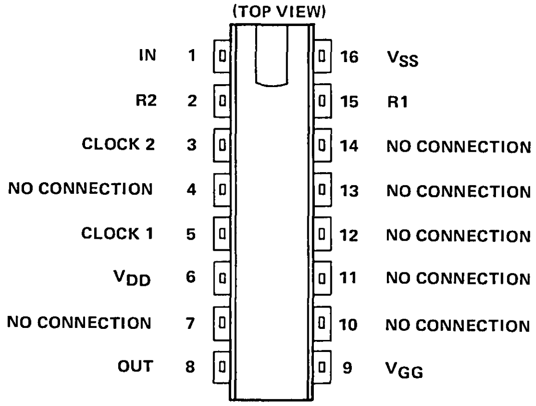


description

The TMS 3401 LC, NC is a single 512-bit dynamic shift register designed for high speed and low power dissipation. The input and output are fully compatible with Series 74 TTL and require no external resistors.

The TMS 3401 is offered in 10-pin TO-100 (LC suffix) and 16-pin dual-in-line plastic (NC suffix) packages. The 16-pin package is designed for insertion in mounting-hole rows on 300-mil centers.

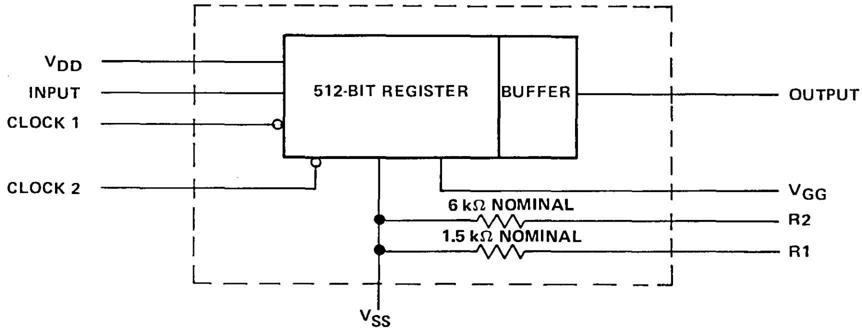
16-PIN PLASTIC DUAL-IN-LINE PACKAGE
(TOP VIEW)



applications

The TMS 3401 can be used in display, delay line, and long serial storage applications.

functional block diagram



A complete data sheet may be obtained by writing directly to:

Marketing and Information Services
Texas Instruments Incorporated
P.O. Box 5012 MS 308
Dallas, Texas 75222

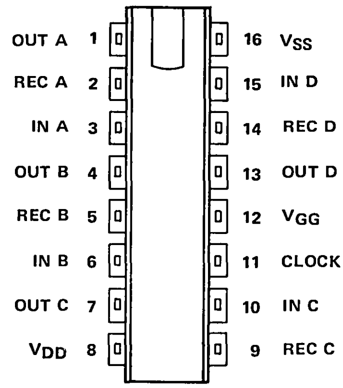
MOS
LSI

TMS 3409 JC, NC; TMS 3417 JC, NC
QUADRUPLE 80-, 64-BIT DYNAMIC SHIFT REGISTERS

BULLETIN NO. DL-S 7512266, MAY 1975

- 10-kHz to 5-MHz Operation
- Dynamic Configuration
- Single TTL-Compatible Clock
- Inputs and Outputs Fully TTL-Compatible
- On-Chip Recirculate Logic
- Power Supplies . . . 5 V, −12 V
- MOS Low-Threshold Self-Aligned-Gate Technology

16-PIN CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGES
(TOP VIEW)



description

The TMS 3409 and TMS 3417 are quad 80-bit and quad 64-bit shift registers, respectively, with independent inputs, outputs, and recirculate controls for each register. A single external clock signal generates two internal clock phases to each register. The clock and all inputs can be driven from Series 74 TTL circuits and all outputs can drive TTL circuits without the use of external resistors.

P-channel enhancement-type low-threshold processing with self-aligned gates has been employed to reduce power dissipation and provide simple interfaces with bipolar circuits.

The TMS 3409 and TMS 3417 are offered in 16-pin dual-in-line ceramic (JC suffix) or plastic (NC suffix) packages designed for insertion in mounting-hole rows on 300-mil centers. These devices are characterized for operation from −25°C to 85°C.

applications

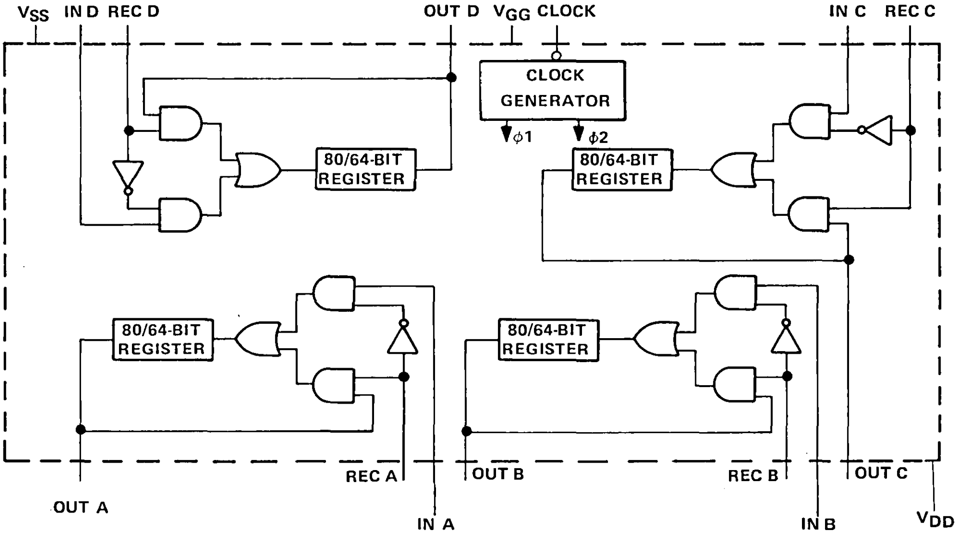
The TMS 3409 and TMS 3417 can be used in terminals, CRT displays, key-to-tape, key-to-disk, and card-punch applications.

operation

Transfer of data into and out of the shift register occurs on the high-to-low transition of the clock with output data becoming valid after a specified propagation delay following that transition. Input data must be set up a minimum time before the high-to-low transition and must be held for a minimum time after that transition.

Recirculate occurs on the high-to-low clock transition with the recirculate control high. The recirculate control level must be set up a minimum time before this transition and held a minimum time after the transition. Data is entered with the recirculate control low. During recirculation, data is continuously available at the outputs and data inputs are inhibited.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{DD} (see Note 1)	−20 V to 0.3 V
Supply voltage, V_{GG} (see Note 1)	−20 V to 0.3 V
Clock input voltage (see Note 1)	−20 V to 0.3 V
Data input voltage (see Note 1)	−20 V to 0.3 V
Operating free-air temperature range	−25°C to 85°C
Storage temperature range	−55°C to 150°C

NOTE 1: Under absolute maximum ratings, voltage values are with respect to the normally most-positive supply, V_{SS} (substrate). Throughout the remainder of this data sheet voltage values are with respect to V_{DD}.

*Comment: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		0		V
Supply voltage, V_{GG}	−11	−12	−13	V
Supply voltage, V_{SS}	4.75	5	5.25	V
High-level input voltage, V_{IH}	$V_{SS}-2$		V_{SS}	V
High-level clock input voltage, $V_{IH(\phi)}$	$V_{SS}-2$		V_{SS}	V
Low-level input voltage, V_{IL}	0		0.8	V
Low-level clock input voltage, $V_{IL(\phi)}$	0		0.4	V
Pulse width, clock high, $t_{w(\phi H)}$	75		50000	ns
Pulse width, clock low, $t_{w(\phi L)}$	125		50000	ns
Data setup time, $t_{su(da)}$	50			ns
Recirculate setup time, $t_{su(rec)}$	200			ns
Data hold time, $t_{h(da)}$	50			ns
Recirculate hold time, $t_{h(rec)}$	100			ns
Clock frequency, f_{ϕ}	0.01		5	MHz
Operating free-air temperature, T_A	−25		85	°C

3

electrical characteristics under nominal operating conditions, T_A = –25°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = 0.5 mA	V_{SS} –1	V_{SS} –0.5	V_{SS}	V
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA		0.3	0.4	V
I_I	Input current (all inputs)	V_I = 0			–100	nA
I_{GG}	Supply current from V_{GG}	Load = 1 TTL gate (see Note 2), f = 1 MHz		–10	–12	mA
I_{SS}	Supply current from V_{SS}	Load = 1 TTL gate (see Note 2), f = 1 MHz		33	47	mA
P_D	Power dissipation	Load = 1 TTL gate (see Note 2), f = 1 MHz		285	400	mW
C_i	Input capacitance, all inputs except clock	V_I = V_{SS}, f = 1 MHz			10	pF
$C_{i(\phi)}$	Clock input capacitance	$V_{I(\phi)}$ = V_{SS}, f = 1 MHz			25	pF

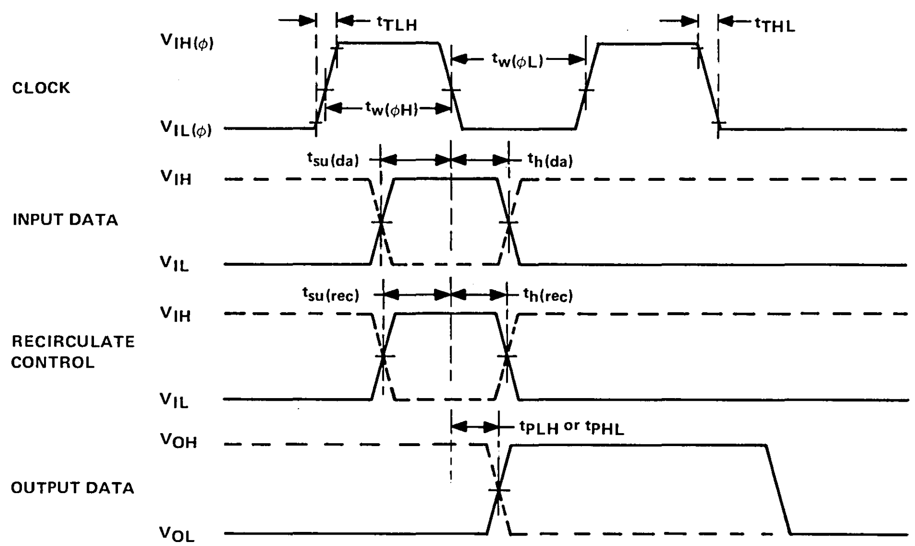
†All typical values are at T_A = 25°C.
NOTE 2: For final test purposes, a worst-case TTL load is simulated by a load of 2.7 kΩ and a capacitance of 10 pF.

switching characteristics under nominal operating conditions, T_A = –25°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from clock	1 Series 74 TTL Load + 10 pF OR		100	160	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock	10 MΩ + 10 pF (MOS Load) (see Note 3)		100	160	ns
t_{TLH}	Transition time, low-to-high-level output	1 Series 74 TTL Load + 10 pF			60	ns
t_{THL}	Transition time, high-to-low-level output	(see Note 3)			50	ns

†All typical values are at T_A = 25°C.
NOTE 3: For final test purposes a worst-case TTL load is simulated by a load of 2.7 kΩ and a capacitance of 10 pF. A worst-case MOS load is simulated by a load of 10 MΩ and 10 pF. All loads are connected between output and V_{SS}.

voltage waveforms



NOTE 3. All timings are with respect to 50% points of transitions with the exception of clock transition times, which are measured at 90% (high) and 10% (low).

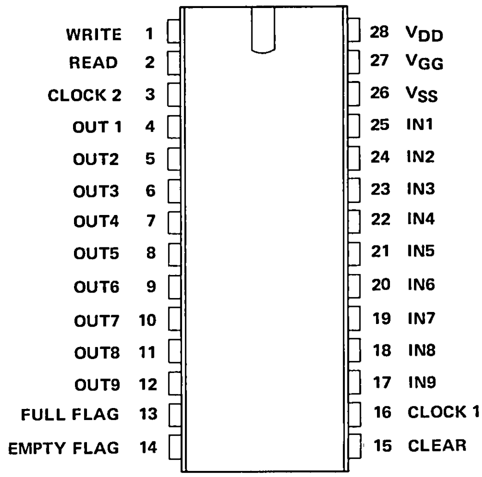
PRINTED IN U.S.A. 57?
TEXAS INSTRUMENTS INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TMS 4024 JC, NC
9 X 64 DIGITAL STORAGE BUFFER (FIFO)

BULLETIN NO. DL-S 7512268, MAY 1975

- 64 Words of 9 Bits of Elastic Storage
- TTL-Compatibility on All Inputs Including Clocks
- 3-State Output Buffers
- 3 Control Inputs (Read, Write, Clear)
- DC to 250-kHz Data Rate
- Status Outputs (Full, Empty)
- Synchronous and Asynchronous Operation
- 2-Cycle (4-μs) Throughput
- Long-Term Data Retention
- Output Pins Directly Opposite Corresponding Inputs

28-PIN CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGES
(TOP VIEW)



3

description

The TMS 4024 JC, NC is a first-in, first-out digital storage buffer that will store up to 64 nine-bit words. The major components of the device include a 9 x 64 dynamic RAM, three shift counters, and comparison and control logic. A RAM-type organization results in minimal ripple-through time. Data written at the input when the RAM is empty is available at the output two clock cycles later. The input and output are completely independent of each other. Input and output timing can be dependent on the clock timing (synchronous mode) or can be operated independently (asynchronous mode). The dynamic RAM requires two-phase continuous clocking at a specified minimum frequency. The clocks can be driven directly from TTL logic.

Low-threshold, thick-oxide, MOS p-channel enhancement-type technology is employed to allow interfacing with TTL circuits without external components.

The TMS 4024 is suitable for many applications as an interface between systems clocked at different speeds and in keyboard buffers, data concentrators, etc.

This device is offered in 28-pin dual-in-line ceramic (JC suffix) and plastic (NC suffix) packages designed for insertion in mounting-hole rows on 600-mil centers. The TMS 4024 is characterized for operation from −25°C to 85°C.

operation (refer to diagram "basic internal operation")

The TMS 4024 will process data at any desired rate from dc to one-half the continuous clock frequency with every other cycle used for automatic refresh. At a nominal 500-kHz clock rate the maximum data rate is 250 kHz. Data is processed in parallel format, word by word.

Writing and reading may be done either synchronously or asynchronously in relation to the clocks. Asynchronous operation is limited to data rates of less than one-third of the clock frequency. Read and write commands must have a minimum separation of one clock cycle.

A positive-going transition at the read or write input is recognized as a command and must occur a minimum time before the rise of clock 2.

A write command causes the data present at the input to be transferred into the buffer. Data-in must be valid for the period during which clock 2 is low. For asynchronous operation, data-in must be valid for two periods after a write command is given because a write command may be given at any time in relation to the clock.

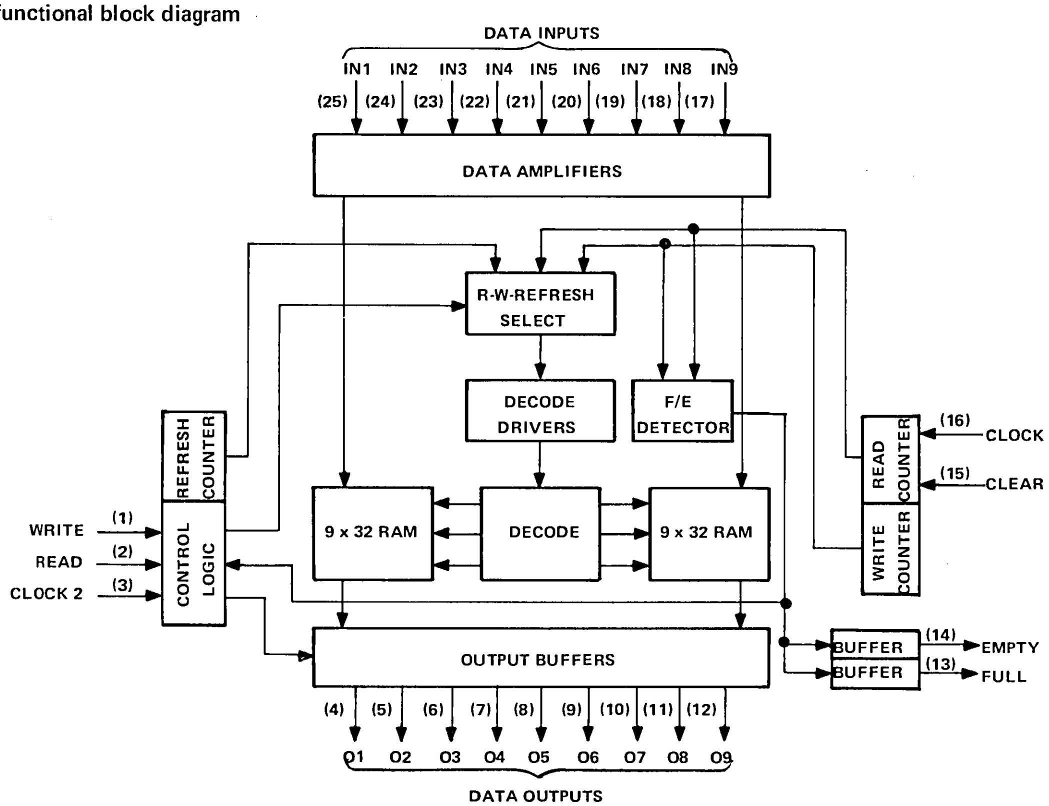
operation (continued)

If both read and write inputs are brought to a high logic level, the read and write operations are disabled and the data outputs float. The data present in the RAM is retained while the read and write operations are disabled.

A clear command will clear all contents of the digital storage buffer, except for the output latches. When the clear input is brought to a high level, it invalidates all other commands. Completion of a clear operation is detected by a high level at the empty status output. The clear command should be synchronized with clock 2.

Status outputs (empty and full) are provided to avoid invalid operation and to facilitate cascading of the device. A high level at the full status output invalidates write commands and a high level at the empty status output invalidates read commands.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1)	−15 V to 0.3 V
Supply voltage, V_{GG} (see Note 1)	−20 V to 0.3 V
Clock input voltage range (see Note 1)	−15 V to 0.3 V
Data input voltage range (see Note 1)	−15 V to 0.3 V
Operating free-air temperature range	−25°C to 85°C
Storage temperature range	−55°C to 150°C

NOTE 1: Under absolute maximum ratings voltage values are with respect to V_{SS} (substrate). Throughout the remainder of this data sheet voltage values are with respect to a floating ground.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD} (see Note 2)	−4.75	−5	−5.25	V
Supply voltage, V_{GG} (see Note 2)	−10.8	−12	−13.2	V
Supply voltage, V_{SS} (see Note 2)	4.75	5	5.25	V
High-level input voltage, all inputs including clocks, V_{IH} (see Note 3)	V_{SS} −1.5	3.5	V_{SS}	V
Low-level input voltage, all inputs including clocks, V_{IL} (see Note 3)	−5.5	0	0.3	V
Clock pulse rise time, $t_{r(\phi)}$		25	50	ns
Clock pulse fall time, $t_{f(\phi)}$		25	50	ns
Clock-1 pulse width, $t_{w(\phi1)}$	400	700		ns
Clock-2 pulse width, $t_{w(\phi2)}$	700	1000		ns
Read pulse width, $t_{w(rd)}$	300	2000		ns
Write pulse width, $t_{w(wr)}$	300	2000		ns
Clear pulse width, $t_{w(clr)}$	1			ck cyc
Delay time, clock 1 to clock 2, $t_{d(\phi1\text{-}\phi2)}$	300			ns
Delay time, clock 2 to clock 1, $t_{d(\phi2\text{-}\phi1)}$	0	300		ns
Delay time, clock 2 to clock 1, plus clock-1 pulse width, $t_{d(\phi2\text{-}\phi1)} + t_{w(\phi1)}$	1000			ns
Delay time, read to clock 2, $t_{d(rd\text{-}\phi2)}$	400	600		ns
Delay time, write to clock 2, $t_{d(wr\text{-}\phi2)}$	400	600		ns
Data setup time, $t_{su(da)}$	350			ns
Data hold time, $t_{h(da)}$		350		ns
Data input frequency, f_{data}	0		250	kHz
Clock frequency, f_{ϕ}	120		500	kHz
Operating free-air temperature, T_A	−25		85	°C

NOTES:
2. Voltage values are with respect to a floating ground.
3. The algebraic convention where the most negative limit is designated as minimum is used in this data sheet for logic voltage levels only.
4. Nominal timing is given for 500-kHz operation.

electrical characteristics under nominal operating conditions, T_A = −25°C to 85°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −0.5 mA	V_{SS} −1	V_{SS} −0.5	V_{SS}	V
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA (see Note 5)		0	0.4	V
I_I	Input current, all inputs including clocks				1000	nA
$I_{DD(avg)}$	Average supply current from V_{DD} (see Note 6)	MOS load		−8		mA
$I_{GG(avg)}$	Average supply current from V_{GG} (see Note 6)	MOS load		−6		mA
P_D	Power dissipation	MOS load		182		mW
C_i	Input capacitance, all inputs including clock	f = 100 kHz		7		pF

†All typical values are at T_A = 25°C.

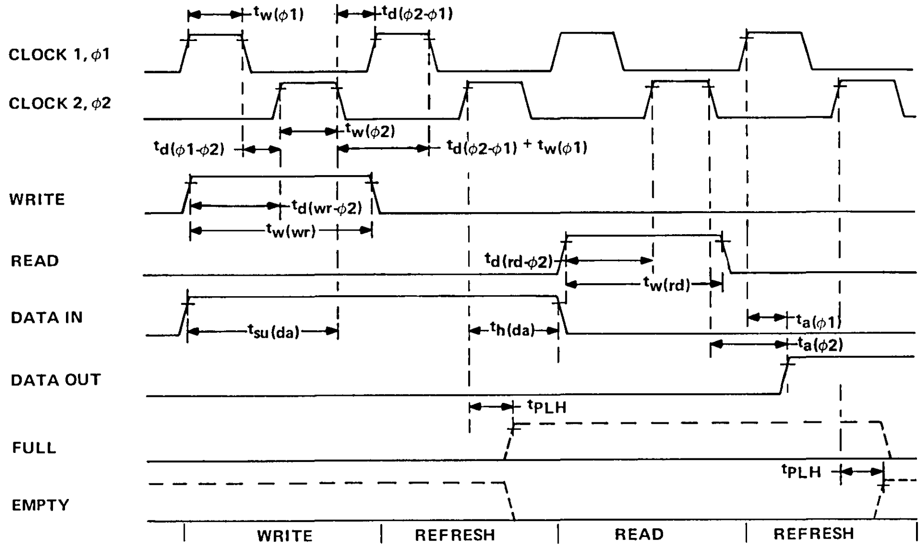
NOTES:
5. V_{OL} is measured with a 1.5-kΩ resistor in series with the output and includes the drop across the resistor.
6. Typical values of $I_{DD(avg)}$ and $I_{GG(avg)}$ are −25 mA and −8 mA at 85°C, each output driving a Series 74 TTL load with a 1.5-kΩ resistor in series, a 25% clock duty cycle (% of time clock is high) and a 75% output current duty cycle (% of time outputs are low).
Typical values of $I_{DD(avg)}$ and $I_{GG(avg)}$ are −60 mA and −8 mA at 85°C, each output driving a Series 74 TTL load with no resistor in series, a 25% clock duty cycle and all outputs low continuously.

switching characteristics under nominal operating conditions, T_A = –25°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$t_{a(\phi1)}$	Access time from clock 1	1 Series 74 TTL load, 25 pF in parallel, 1.5 kΩ in series		400		ns
$t_{a(\phi2)}$	Access time from clock 2		950	1000	1200	ns
t_{PLH}	Propagation delay time, low-to-high level flag outputs from clock 2			400		ns

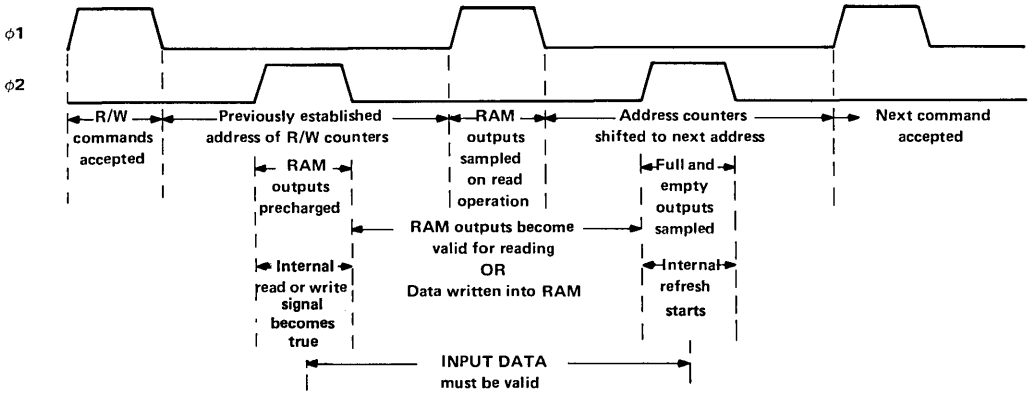
†All typical values are at T_A = 25°C.

timing diagram and voltage waveforms



NOTE: Timing points are 90% (high) and 10% (low).

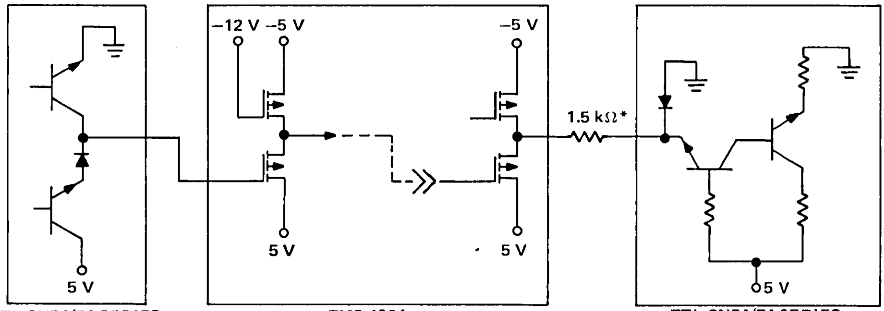
basic internal operation



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

interface circuits

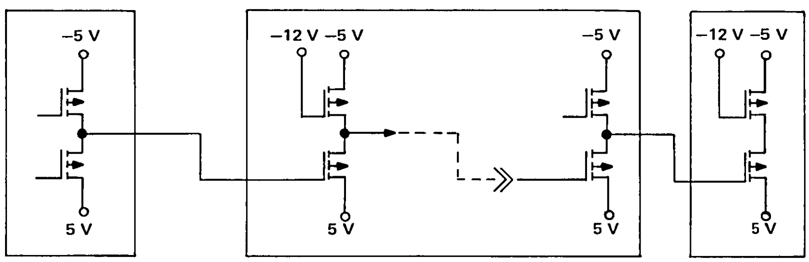
a) TTL



TTL SN54/74 SERIES — TMS 4024 — TTL SN54/74 SERIES

*1.5 kΩ resistor optional — the presence of this resistor helps to reduce power dissipation in the TMS 4024 while driving TTL.

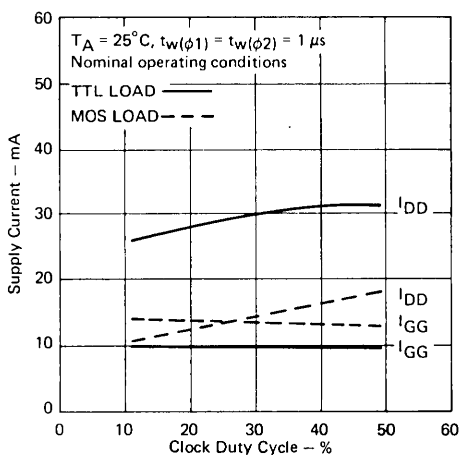
b) MOS



MOS DRIVE — TMS 4024 — MOS LOAD

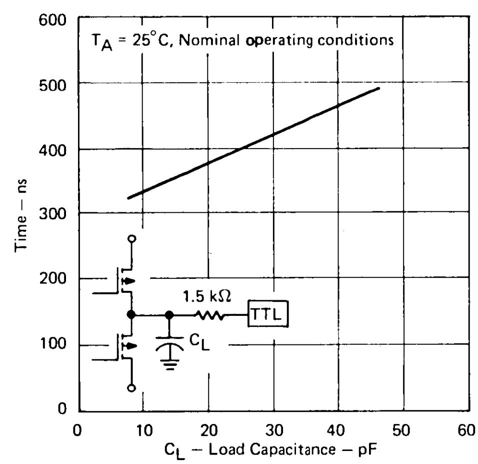
TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs DUTY CYCLE



NOTE: TTL load, 1.5 kΩ series resistor, all outputs low; MOS load, all outputs high.

PROPAGATION DELAY TIMES FOR FULL OR EMPTY FLAGS FROM CLOCK 2 OR ACCESS TIME FROM CLOCK 1 vs LOAD CAPACITANCE



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

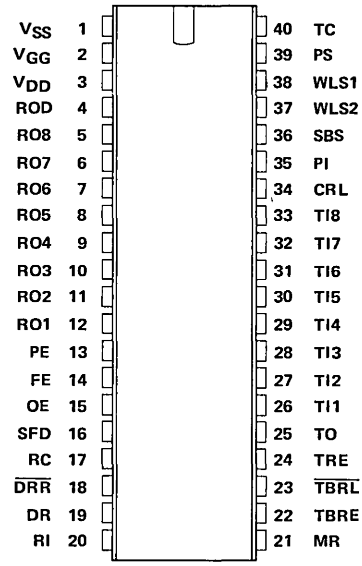
MOS
LSI

TMS 6011 JC, NC
ASYNCHRONOUS DATA INTERFACE (UART)

BULLETIN NO. DL-S 7512275, MAY 1975

- Transmits, Receives, and Formats Data
- Full-Duplex or Half-Duplex Operation
- Operation from DC to 200 kHz
- Static Logic
- Buffered Parallel Inputs and Outputs
- Programmable Word Lengths . . . 5, 6, 7, 8 Bits
- Programmable Information Rate
- Programmable Parity Generation/Verification
- Programmable Parity Inhibit
- Automatic Data Formatting
- Automatic Status Generation
- 3-State Push-Pull Buffers
- Low-Threshold Technology
- Standard Power Supplies . . . 5 V, −12 V
- Full TTL Compatibility . . . No External Components

40-PIN CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGES
(TOP VIEW)



description

The TMS 6011 JC, NC is an MOS/LSI subsystem designed to provide the data interface between a serial communications link and data processing equipment such as a peripheral or a computer. The device is often referred to as an asynchronous data interface or as a universal asynchronous receiver/transmitter (UART).

The receiver section of the TMS 6011 will accept serial data from the transmission line and convert it to parallel data. The serial word will have start, data, and stop bits. Parity may be generated and verified. The receiver section will validate the received data transmission by checking proper start, parity, and stop bits, and will convert the data to parallel.

The transmitter section will accept parallel data, convert it to serial form, and generate the start, parity, and stop bits.

The TMS 6011 is a fully programmable circuit allowing maximum flexibility of operation, defined as follows:

- The receiver and transmitter sections are separate and can operate either in full-duplex (simultaneous transmission and reception) or in half-duplex mode (alternate transmission and reception).
- The data word may be externally selected to be 5, 6, 7, or 8 bits long.
- Baud rate is externally selected by the clock frequency. Clock frequency can vary between 0 and 200 kHz.
- Parity, which is generated in the transmit mode and verified in the receive mode, can be selected as either odd or even. It is also possible to disable the parity bit by inhibiting the parity generation and verification.
- The stop bit can be selected as either a single- or a double-bit stop.
- Static logic is used to maximize flexibility of operation and to simplify the task of the user. The data holding registers are static and will hold a data word until it is replaced by another word.
- Asynchronous operation allows the use of a single transmission line. The clock period has to be within ±4% of 1/16 of the time for one bit for the transmitter and/or receiver but no phase relationship is required.

To allow for a wide range of possible configurations, three-state push-pull buffers have been used on all outputs except **Transmitter Output (TO)** and **Transmitter Register Empty (TRE)**. They allow the wire-OR configuration.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

description (continued)

The TMS 6011 can be used in a wide range of data handling equipment such as modems, peripherals, printers, data displays, and minicomputers. By taking full advantage of the latest MOS/LSI design and processing techniques, it has been possible to implement the entire transmit, receive, and format function necessary for digital data communication in a single package, avoiding the cumbersome circuitry previously necessary.

P-channel enhancement-type low-threshold technology permits the use of standard power supplies (5 V, −12 V) as well as direct TTL interface. No external components are needed.

The TMS 6011 is offered in both 40-pin dual-in-line ceramic (JC suffix) and plastic (NC suffix) packages designed for insertion in mounting-hole rows on 600-mil centers. The device is characterized for operation from −25°C to 85°C.

operation

The operation can be best understood by visualizing the TMS 6011 as three separate sections: 1) common control, 2) transmitter, and 3) receiver. The transmitter and receiver sections are independent while the control section directs both receive and transmit.

common control section

3

The common control section will direct both the receiver and the transmitter sections.

The initialization of the TMS 6011 is performed through the **Master Reset (MR)** terminal. The **MR** terminal is strobed to a high level after power turn-on to reset all status and transmitter registers and to reset **Transmitter Output (TO)** to a high level. The **Receiver Outputs (RO1-RO8)** are not controlled by the **MR** terminal.

Status flags **Parity Error, Framing Error, Overrun Error, Data Ready,** and **Transmitter Buffer Register Empty** are disabled when the **Status Flags Disable (SFD)** is at a high level. When disabled, the status flags float (three-state buffers are in the high-impedance state). The **Transmitter Register Empty (TRE)** status flag is not a three-state output.

The number of bits per word is controlled by the **Word Length Select 1 (WLS1)** and **Word Length Select 2 (WLS2)** inputs. The word length may be 5, 6, 7, or 8 bits. Selection is as follows:

WORD LENGTH	WLS1	WLS2
5	Low	Low
6	High	Low
7	Low	High
8	High	High

The parity to be checked by the receiver and generated by the transmitter is determined by the **Parity Select (PS)** input. A high level on the **PS** input selects even parity and a low level selects odd parity.

The parity will not be checked or generated if a high level is applied to **Parity Inhibit (PI)**; in this case the stop bit or bits will immediately follow the data bit.

When a high level is applied to **PI**, the **Parity Error (PE)** status flag is brought to a low level indicating a no-parity error because parity is disregarded in this mode.

To select either one or two stop bits, the **Stop Bit(s) Select (SBS)** terminal is used. A high level at this terminal will result in two stop bits while a low level will produce only one.

To load the control bits (**WLS1, WLS2, PS, PI,** and **SBS**) a high level is applied to the **Control Register Load (CRL)** terminal. This terminal may be strobed or hard wired to a high level.

operation (continued)

transmitter section

The transmitter section will accept data in parallel form, then serialize, format, and transmit the data in serial form.

Parallel input data is received through the **Transmitter Inputs (TI1-TI8).**

Serial output data is transmitted from the **Transmitter Output (TO)** terminal.

Input data is stored in the transmitter-buffer register. A low level at the **Transmitter Buffer Register Load ($\overline{\text{TBRL}}$)** command terminal will load a word in the transmitter-buffer register. The length of this word is determined by **Word Length Select 1 (WLS1)** and **Word Length Select 2 (WLS2).** If a word of length greater than this appears at **TI8** through **TI1**, only the least significant bits are accepted. The word is justified into the least significant bit, **TI1.**

The data is transferred to the transmitter register when the $\overline{\text{TBRL}}$ terminal goes from low to high. The loading of the transmitter register is delayed if the transmitter section is presently transmitting data. In this case the loading of the transmitter register is delayed until the transmission has been performed.

3

Output serial data (transmitted from the **TO** terminal) is clocked out by **Transmitter Clock (TC).** The clock rate is 16 times faster than the data rate.

The data is formatted as follows: start bit, data, parity bit, stop bits (1 or 2). Start bits, parity bits, and stop bits are generated by the TMS 6011. When no data is transmitted the output **TO** remains at a high level.

The start of transmission is defined as the transition of **TO** from a high to a low logic level.

Two flags are provided. A high level at the **Transmitter Buffer Register Empty (TBRE)** flag indicates that a word has been transferred to the transmitter/receiver and that the transmitter buffer register is now ready to accept a new word. A high level at the **Transmitter Register Empty (TRE)** flag indicates that the transmitter section has completed the transmission of a complete word including stop bits. The **TRE** flag will remain at a high level until the start of transmission of a new word.

Both the transmitter buffer register and the transmitter register are static and will perform long-term storage of data.

receiver section

The data is received in serial form at the **Receiver Input (RI).** The data from **RI** enters the receiver register at a point determined by the character length, the parity, and the number of stop bits. **RI** must be maintained high when no data is being received. The data is clocked by the **Receiver Clock (RC).** The clock rate is 16 times faster than the data rate.

Data is transferred from the receiver register to the receiver buffer register. The output data is then presented in parallel form at the eight **Receiver Outputs (RO1** through **RO8).** The MOS output buffers used for the eight **RO** terminals are three-state push-pull output buffers that permit the wire-OR configuration through use of the **Receiver Output Disable (ROD)** terminal. When a high level is applied to **ROD** the **RO** outputs are floating. If the word length is less than 8 bits, the most significant bits will be at a low level. The output word is right justified. **RO1** is the least significant bit and **RO8** is the most significant bit.

A low level applied to the **Data Ready Reset ($\overline{\text{DRR}}$)** terminal resets the **Data Ready (DR)** output to a low level.

Several flags are provided in the receiver section. There are three error flags (**Parity Error, Framing Error,** and **Overrun Error**) and a **DR** flag. These status flags may be disabled by a high level at the **Status Flags Disable (SFD)** terminal.

A high level at the **Parity Error (PE)** terminal indicates an error in parity.

A high level at the **Framing Error (FE)** terminal indicates a framing error that is an invalid or nonexistent stop bit in the received word.

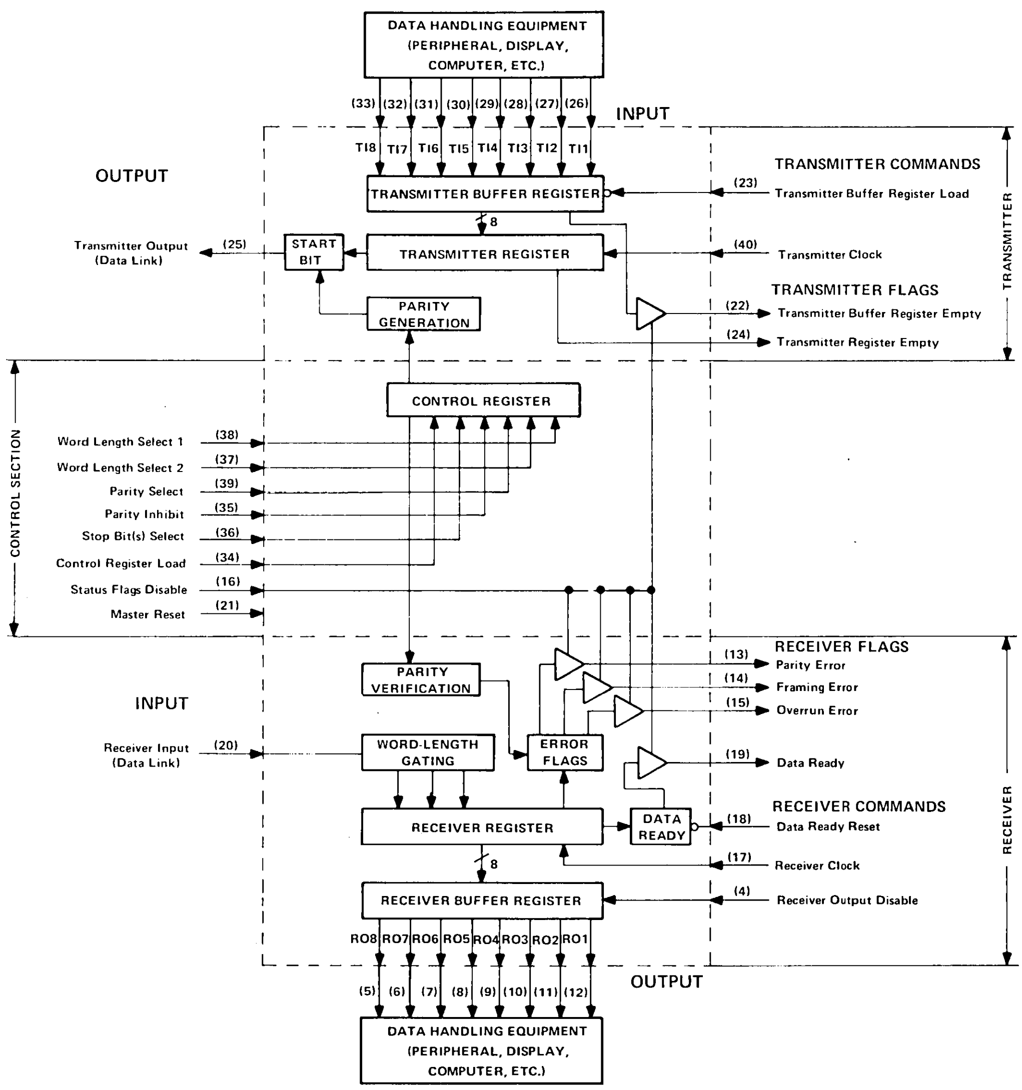
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

operation (continued)

A high level at the **Overrun Error (OE)** terminal indicates an overrun. An overrun occurs when the previous word has not been read, i.e., when the **DR** output has not been reset before the present data was transferred to the receiver buffer register.

A high level at the **DR** terminal indicates that a word has been received, stored in the receiver-buffer register and that the data is available at outputs **RO1** through **RO8.** The **DR** terminal can be reset through the **$\overline{\text{DRR}}$** terminal.

functional block diagram



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{DD} (see Note 1)	−20 V to 0.3 V
Supply voltage, V_{GG} (see Note 1)	−20 V to 0.3 V
Input voltage (any input) (see Note 1)	−20 V to 0.3 V
Operating free-air temperature range	−25°C to 85°C
Storage temperature range	−55°C to 150°C

NOTE 1: Under absolute maximum ratings, voltage values are with respect to the normally most positive supply, V_{SS} (substrate). Throughout the remainder of this data sheet voltage values are with respect to V_{DD}.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

PARAMETER		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}			0		V
Supply voltage, V_{GG}		−11.5	−12	−12.5	V
Supply voltage, V_{SS}		4.75	5	5.25	V
High-level input voltage, all inputs, V_{IH} (see Notes 2 and 3)		V_{SS} −1.5		V_{SS} +0.3	V
Low-level input voltage, all inputs, V_{IL} (see Notes 2 and 3)		−12		0.8	V
Pulse width, t_w	Clock	2.5			μs
	Transmitter buffer register load	400			ns
	Control register load	250			ns
	Parity inhibit (see Notes 4 and 5)	400			ns
	Parity select (see Notes 4 and 5)	300			ns
	Word length select and stop bit select (see Notes 4 and 5)	300			ns
	Master reset	1.5			μs
	Data ready reset	250			ns
Data setup time, $t_{su(da)}$		10↓			ns
Data hold time, $t_{h(da)}$		20↑			ns
Clock frequency, f_ϕ (see Note 6)		0		200	kHz
Operating free-air temperature, T_A		−25		85	°C

NOTES: 2. All data, clock, and command inputs have internal pull-up resistors to allow direct clocking by any TTL circuit.
3. The algebraic convention where the most negative limit is designated as minimum is used in this data sheet for logic voltage levels only.
4. Inputs to PI, PS, WLS1, WLS2, and SBS are normally static signals. A minimum pulse width has been indicated for possible pulsed operation.
5. All control signal pulses should be centered with respect to CRL to ensure maximum setup and hold time.
6. Clock frequency is 16 times the baud rate.

↑↓The arrow indicates the edge of the $\overline{TBRL}$ pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −200 μA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA			0.6	V
I_{IH}	High-level input current, all inputs	V_I = 5 V			10	μA
I_{IL}	Low-level input current, all inputs	V_I = 0 V			−1.6	mA
I_{GG}	Supply current from V_{GG}	All inputs at a high level		−7	−12	mA
I_{SS}	Supply current from V_{SS}	All inputs at a high level		20	30	mA
P_D	Power dissipation	All inputs at a high level		190	300	mW
C_i	Input capacitance, all inputs	V_I = V_{SS}, f = 1 MHz		10	20	pF

†All typical values are at T_A = 25°C and nominal voltages.

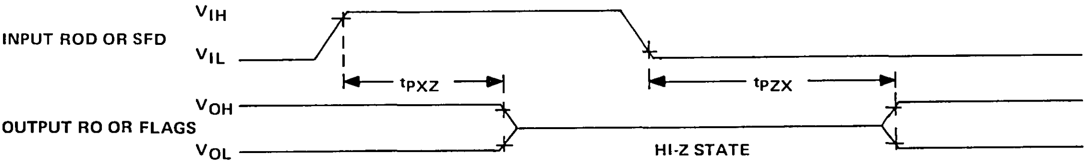
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

switching characteristics over full ranges of recommended operating conditions (unless otherwise noted)

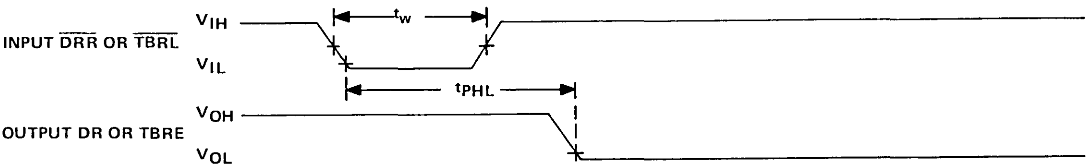
PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low level DR output from $\overline{DRR}$	1 Series 74 TTL load		800	1000	ns
t_{PHL}	Propagation delay time, high-to-low level TBRE output from $\overline{TBRL}$			800	1000	ns
t_{PZX}	Enable time, receiver output from ROD			300	500	ns
t_{PXZ}	Disable time, receiver output from ROD			300	500	ns
t_{PZX}	Enable time, outputs PE, FE, OE, DR, or TBRE from SFD			300	500	ns
t_{PXZ}	Disable time, outputs PE, FE, OE, DR, or TBRE from SFD			300	500	ns

†All typical values are at $T_A = 25°C$ and nominal voltages.

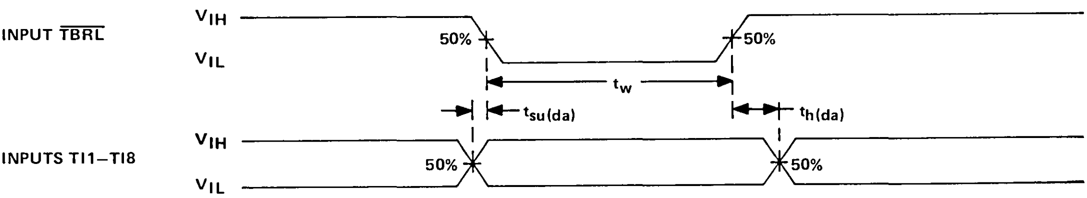
voltage waveforms



ENABLE AND DISABLE TIMES



PROPAGATION DELAY TIMES

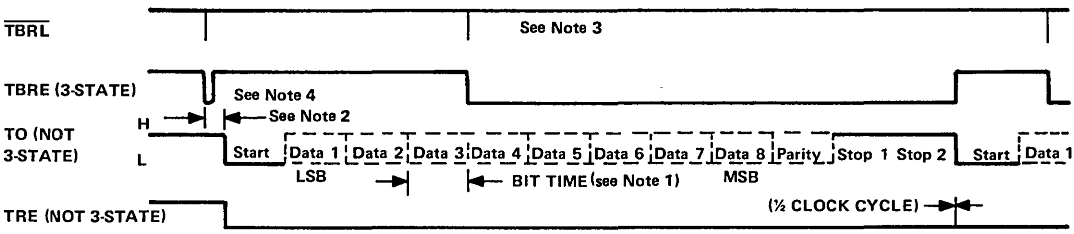


DATA SETUP AND HOLD TIMES

NOTE: All enable, disable, and propagation delay times are referenced to the 90% or 10% points. All pulse widths are referenced to the 50% points.

operation timing diagram

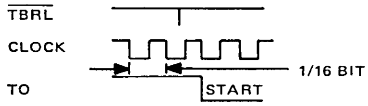
TRANSMITTER TIMING†



† Transmitter initially assumed inactive at start of diagram, shown for 8 level code and parity and 2 stops.

NOTES: 1. Bit time is 16 clock cycles.

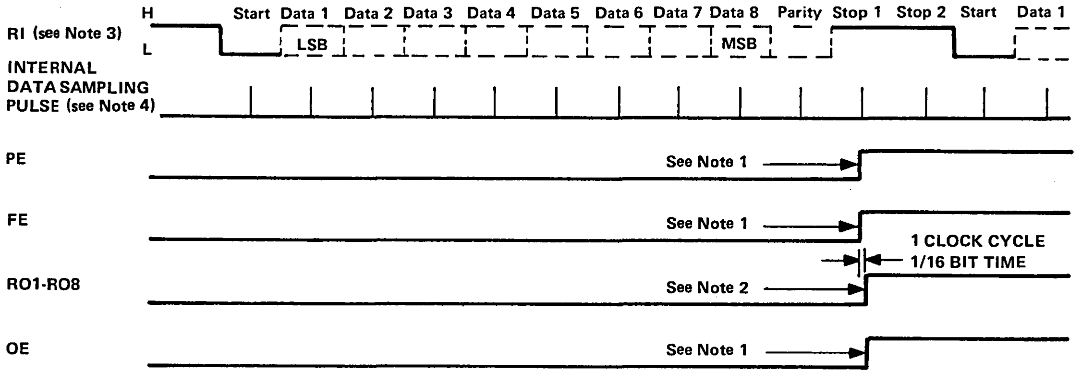
2. If transmitter is inactive the start pulse will appear on line within one clock cycle of time data strobe occurs (see detail below).



3. Because transmitter is double buffered, another data strobe can occur anywhere during transmission of character 1.

4. TBRE goes to a low for a period of approximately one clock cycle following a TBRL pulse.

RECEIVER TIMING



NOTES: 1. This is the point at which the error condition is detected, if error occurs.

2. A high-to-low transition on the DR pin indicates that the contents of the receiver register has been transferred to the receiver buffer register and that the three error-flag signals are valid. Output data remains valid until the next word is transferred into the receiver buffer register.

3. The RI waveform illustrates an eight-bit word with parity and two stop bits. If parity is inhibited, the stop bits immediately follow the last data bit. For all word lengths, the data in the buffer register must be right justified, i.e., RO1 (pin 12) is the least significant bit.

4. Data sampling occurs at the center of each data bit (8 clock cycles after the beginning of the bit).

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

MOS MEMORY SYSTEM COMPATIBILITY

1) POWER SUPPLIES

In P-channel MOS Memories the substrate is normally biased positive with respect to the drain or source nodes. The substrate bias is normally negative for N-channel devices. In order to provide compatible interfaces with bipolar integrated circuits, power supply voltages are translated for most MOS Memory devices of recent design to maintain the recommended substrate bias conditions and to provide input and output voltage levels between ground (0 volts) and V_{CC} (+5 volts), the standard system supply voltage in equipment using TTL integrated circuits.

The chart below shows the recommended supply voltages for the MOS Memory devices in this catalog along with the symbols used for the various supply terminals.

MOS MEMORY NOMINAL POWER SUPPLY VOLTAGES AND TERMINAL SYMBOLOGY

TECHNOLOGY	P-CHANNEL			N-CHANNEL		
	METAL GATE		SILICON GATE			
SUPPLY VOLTAGE						
22.5 V		V_{BB}				
20 V		V_{SS}				
19 V			V_{BB}			
16 V			V_{SS}			
12 V					V_{DD}	V_{DD}
7 V		V_{REF}				
5 V	V_{SS}			V_{CC}		V_{CC}
0	V_{DD}	V_{DD}	V_{DD}	GND	V_{SS}	V_{SS}
−3 V						
−5 V					V_{BB}	V_{BB}
−12 V	V_{GG}					
PRODUCT TYPE	Static and dynamic shift registers, ROM's, keyboard encoder, UART	Dynamic RAM's	Dynamic RAM	Static RAM's	4K Dynamic RAM's	ROM
TYPE NUMBERS	TMS 3101 thru TMS 3409 (all S/R's) TMS 4800 TMS 2501 TMS 4103 TMS 5001 TMS 6011	TMS 4062 TMS 4063	TMS 1103	TMS 4033 TMS 4034 TMS 4035 TMS 4036 series TMS 4039 series TMS 4042 series TMS 4043 series	TMS 4030 series TMS 4050 series TMS 4051 series TMS 4060 series	TMS 5400

MOS MEMORY SYSTEM COMPATIBILITY

3

2) INPUT COMPATIBILITY

Figure 1 illustrates how Series 74 TTL circuits are specified to guarantee that any Series 74 circuit will drive or can be driven by any other Series 74 circuit. The 0.4-volt difference in output and input specifications is called the noise margin. These margins guarantee that any Series 74 circuit is compatible with any other Series 74 circuit and that the probability of false data inputs from spurious switching transients or induced voltage levels is minimized.

SERIES 74 TTL INPUT AND OUTPUT SPECIFICATIONS

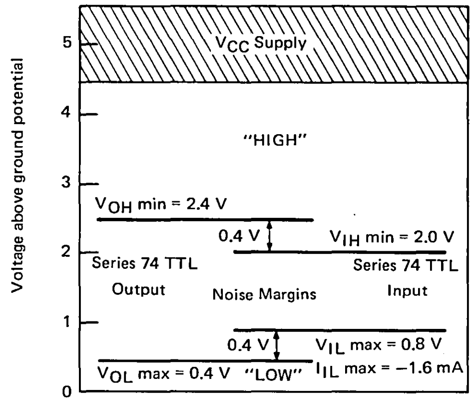
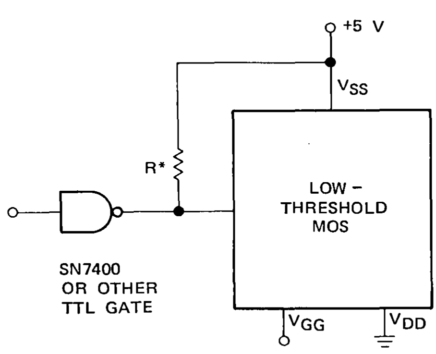


FIGURE 1

All TI shift registers and most ROM's and RAM's are designed with inputs that can be driven directly without level-shifter or amplifier circuits. The phrase "fully TTL-compatible" has been used to indicate that a MOS Memory device will drive or be driven by Series 74 circuits with adequate noise margins without the use of external pull-up or pull-down components. Some P-channel MOS Memories require a pull-up resistor on the input to meet the minimum input voltage high level, V_{IH} min. Figure 2 illustrates the interface with TTL. In all cases, the input of the MOS circuit has a very high impedance. Therefore, TTL input compatibility is easily achieved.



*The value of the R resistor varies depending on speed-power requirements. In many cases this resistor is diffused on the MOS chip. For low-threshold MOS the resistor assures that the worst-case TTL output is pulled up to at least 3.5 V for proper MOS circuit operation.

FIGURE 2

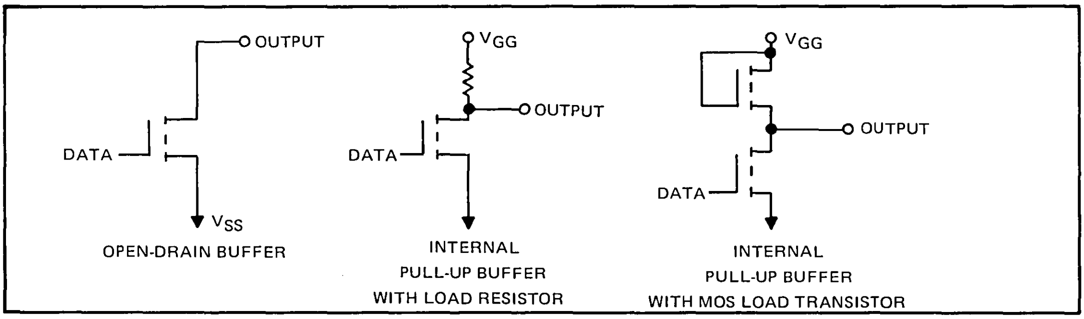
3) OUTPUT COMPATIBILITY

Three types of buffers are commonly used on MOS devices:

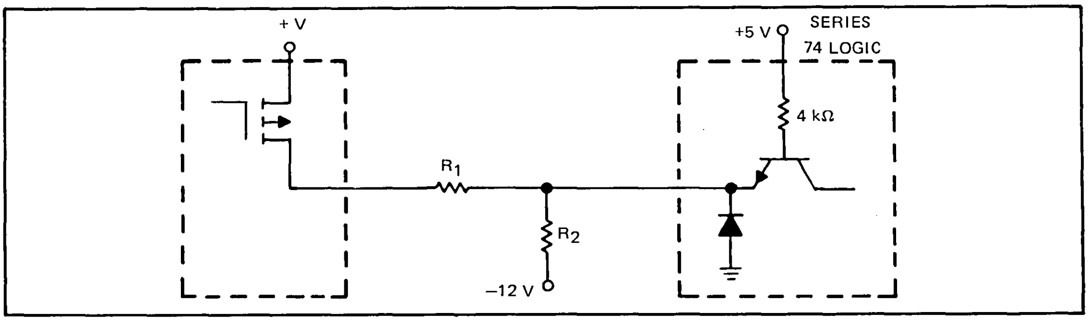
- Open-drain
- Internal pull-up
- Push-pull

a) Open-drain and internal pull-up

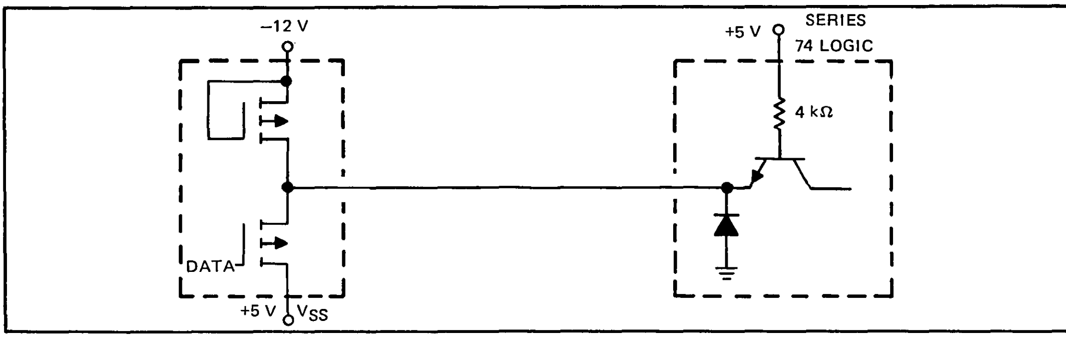
The buffer is simply a current switch. In the "off" state the impedance of the buffer is extremely large, while in the "on" state it is typically under 1 kΩ. A discrete resistor or an MOS transistor may be used as a load with an open-drain buffer. This resistor or transistor may be internal to the MOS circuit.



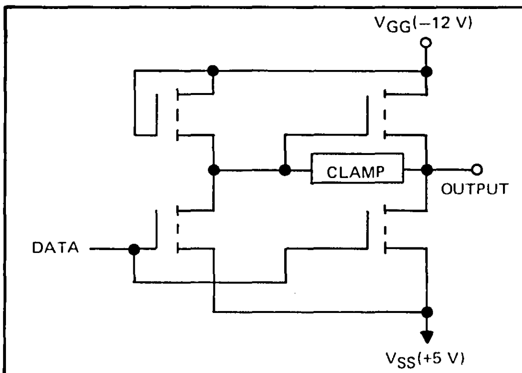
In every case compatibility with MOS is easily achieved. For instance, for an open-drain buffer with MOS:



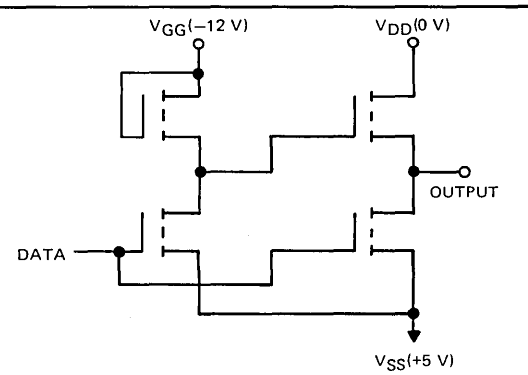
R_2 provides the necessary current sink for the TTL input; R_1 is sometimes used to limit power dissipation or the positive excursion of the TTL input to +5 V. If R_2 is on the chip, no external components may be necessary.



Two types are common. The unsaturated push-pull buffer is the most commonly used for low-threshold circuits since the smaller drain-source voltage permits the upper output transistor to operate in the unsaturated or low-resistance region of the I_D vs V_{DS} characteristic curve. As a result, the output voltage swings near V_{DD} without going negative and permits direct TTL compatibility without external components.



SATURATED PUSH-PULL BUFFER



UNSATURATED PUSH-PULL BUFFER

4) CLOCKS

Depending on the circuit type, there are different clock requirements:

No clocks – Static RAMs, ROMs, etc.
1 clock – with other clocks generated internally
2 clocks – most dynamic shift registers

a) One external clock

An internal circuit generates the clocks from a single outside clock signal. The outside clock signal has the same swing as the data input signal and the compatibility is identical (see preceeding paragraph 3).

Single-clock low-threshold MOS circuits will accept a TTL clock without adding components.

b) Two or four clocks

The clock signals must swing between V_{SS} and V_{GG}. To go from a single-TTL-level clock to a multiple-MOS-level clock, two circuits are required: 1) a clock generator to generate the necessary clock pulses, and 2) a clock driver to bring the clock levels to the required values. In most cases only one clock circuit is needed for an entire MOS LSI system.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

general

Electrical characteristics presented in this catalog, unless otherwise noted, apply for circuit type(s) listed in the page heading, regardless of package. Factory orders for circuits described should include the complete part-type numbers listed on each page.

MOS NUMBERING SYSTEM

EXAMPLE: TM S 4030 N L

1. TI MOS Prefix (TM)

2. Product Status (S)
   - S Standard devices
   - X Prototype or experimental
   - C Custom design
   - T High reliability

3. Unique Product Identification Number (4030)

4. Package (N)
   - F Flat
   - J Ceramic dual-in-line
   - N Plastic dual-in-line
   - L Metal can
   - U Unencapsulated (beam lead, etc.)

5. Temperature Range (L)
   - C −25°C to 85°C
   - L 0°C to 70°C
   - M −55°C to 125°C
   - R −55°C to 85°C
   - S Special range

manufacturing information

Alloying is performed in an inert atmosphere. A silicon gold eutectic is formed during the alloying operation.

Thermal compression bonding is used. Typical bond strength is 5 grams. Bond strength is monitored on a lot-to-lot basis. Any bond strength of less than 2 grams causes rejection of the entire lot of devices.

TI uses a low-temperature alloy brazing to seal ceramic packages. Metal-can packages are welded. Glass leaks are eliminated by testing in a fluorocarbon solution heated to 150°C. Fine-leak elimination is performed through mass spectrometer techniques. All MOS LSI devices produced by TI are capable of withstanding 5×10^{-7} ppm fine-leak inspection, and may be screened to 5×10^{-8} ppm fine leak, if desired by the customer, for special applications.

All packages are capable of withstanding a shock of 3,000 G. All packages are capable of passing a 20,000-G acceleration (centrifuge) test in the Y axis. Pin strength is measured by a pin-shearing test. All pins are able to withstand the application of a force of 6 pounds at 45° in the peel-off direction.

dual-in-line packages

A pin-to-pin spacing of 100 mils has been selected for all dual-in-line packages.

TI uses several hermetically sealed ceramic dual-in-line packages, each of which consist of a ceramic base, plated metal cap, and tin-plated leads.

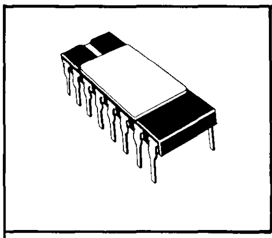
The following dual-in-line packages are available in plastic or ceramic:

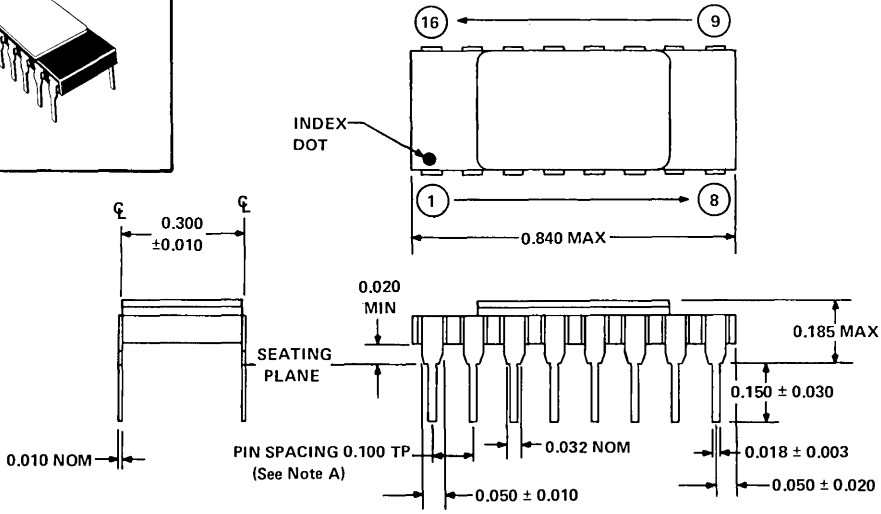
	8 PIN	10 PIN	16 PIN	18 PIN	22 PIN	24 PIN	28 PIN	40 PIN
300 mils between rows	X†	X†	X	X				
400 mils between rows					X	X†		
600 mils between rows						X	X	X

†There are no products shown in this data book in the 8-pin ceramic package or the ceramic or plastic 10-pin or 24-pin, 400-mil package.

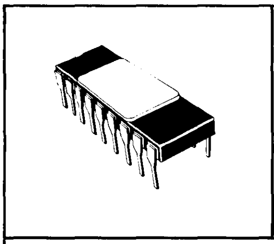
MOS LSI MECHANICAL DATA

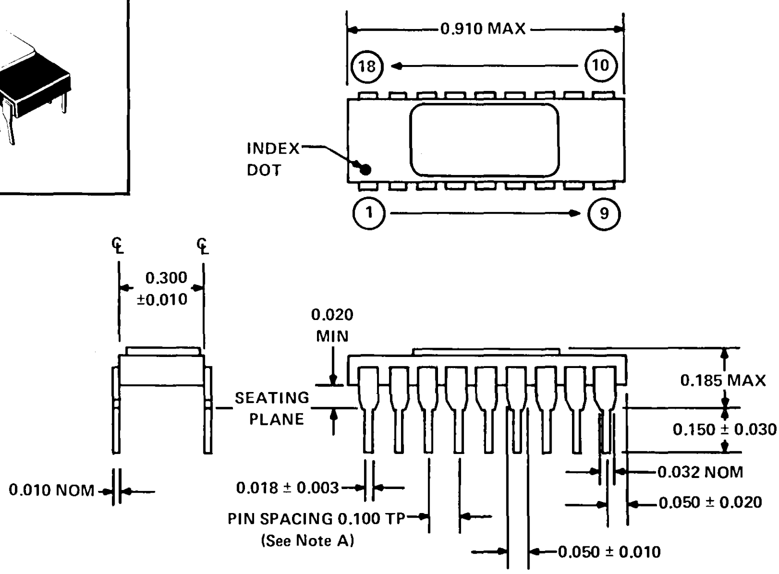
16-PIN CERAMIC DUAL-IN-LINE PACKAGE





18-PIN CERAMIC DUAL-IN-LINE PACKAGE

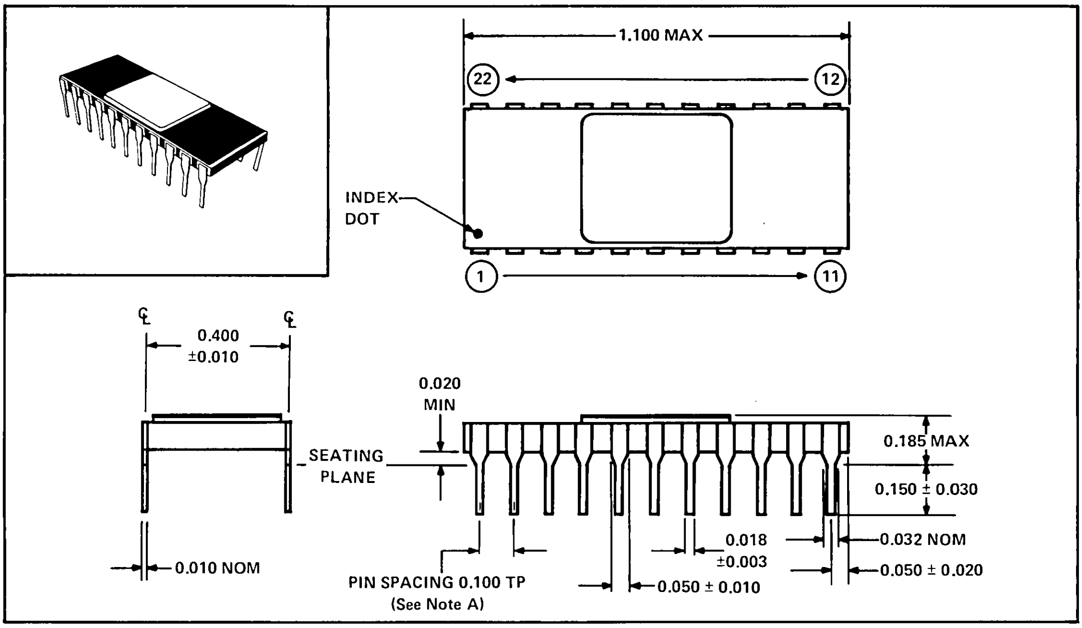




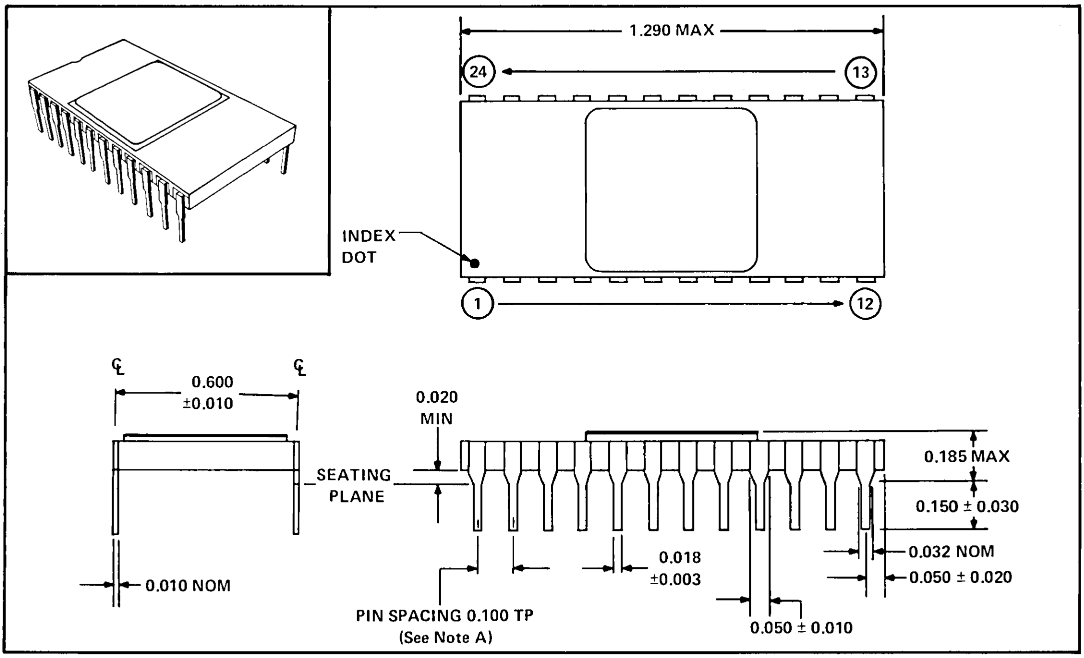
NOTES: A. Each pin centerline is located within 0.010 of its true longitudinal position.
B. All linear dimensions are in inches.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

22-PIN CERAMIC DUAL-IN-LINE PACKAGE



24-PIN CERAMIC DUAL-IN-LINE PACKAGE

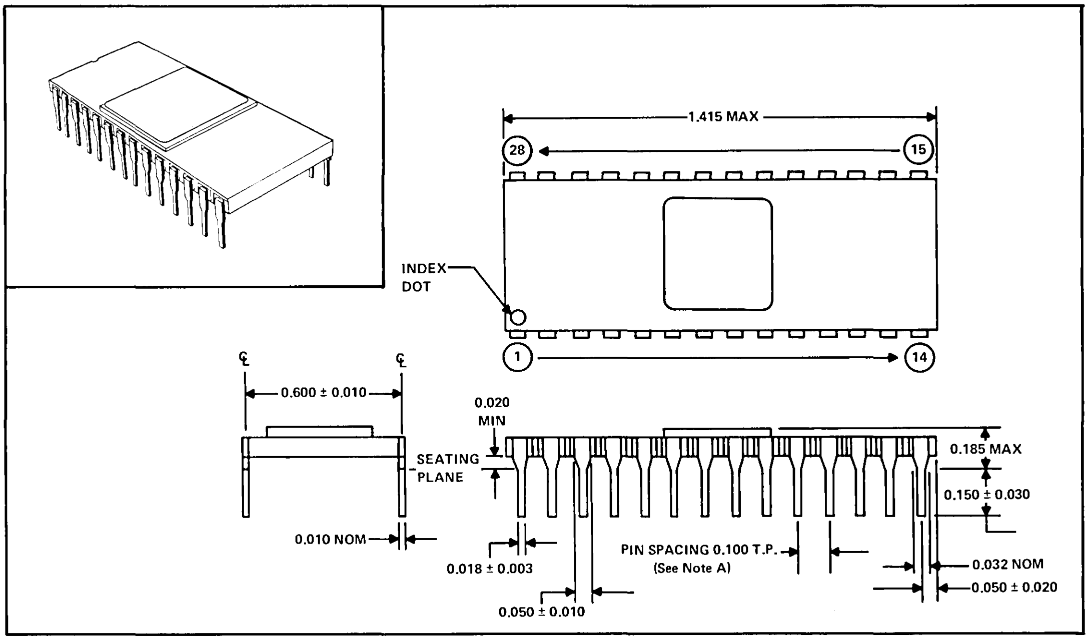


NOTES: A. Each pin centerline is located within 0.010 of its true longitudinal position.
B. All linear dimensions are in inches.

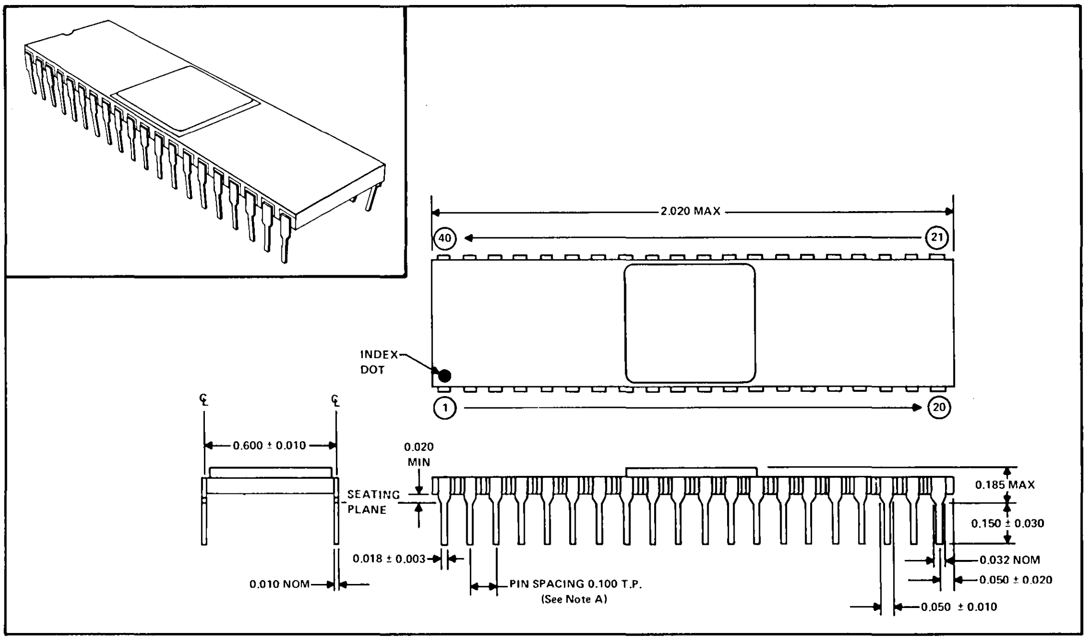
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

MOS LSI MECHANICAL DATA

28-PIN CERAMIC DUAL-IN-LINE PACKAGE



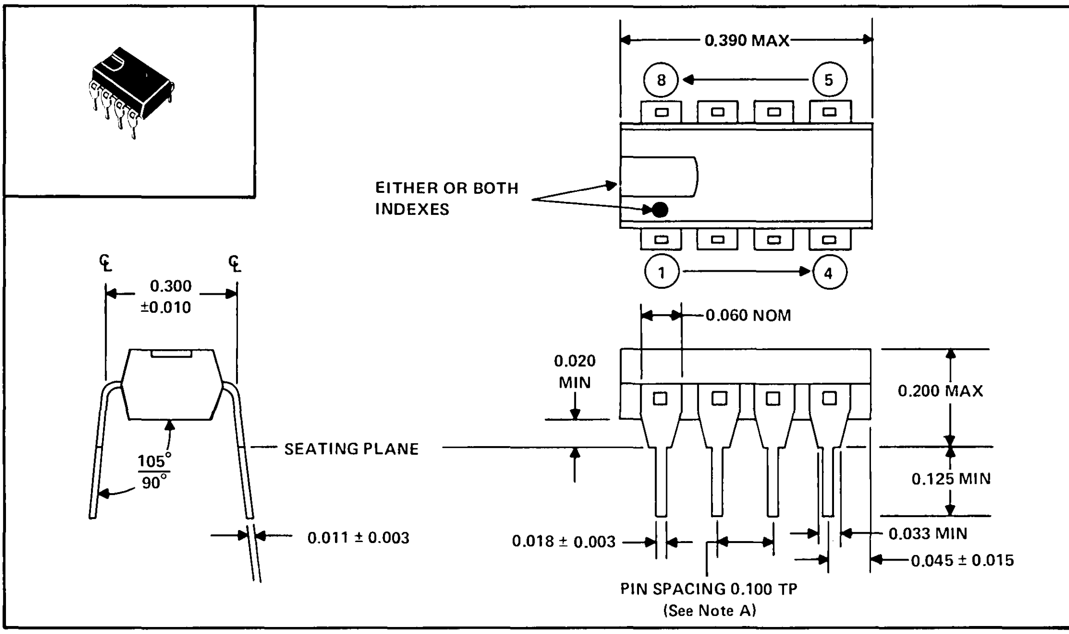
40-PIN CERAMIC DUAL-IN-LINE PACKAGE



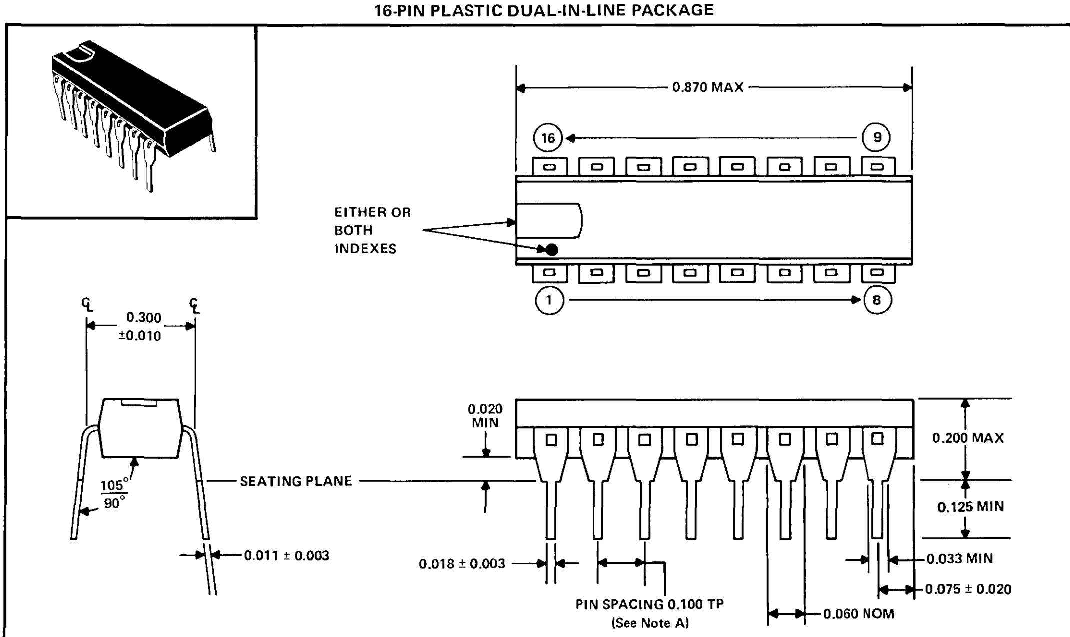
NOTES: A. Each pin centerline is located within 0.010 of its true longitudinal position.
B. All linear dimensions are in inches.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

8-PIN PLASTIC DUAL-IN-LINE PACKAGE



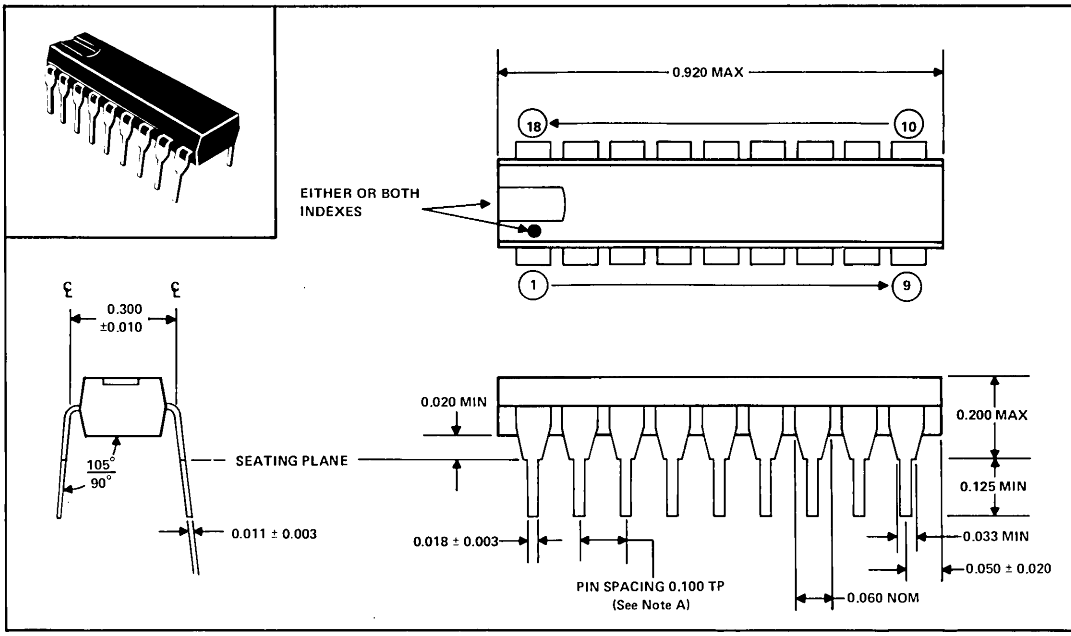
16-PIN PLASTIC DUAL-IN-LINE PACKAGE



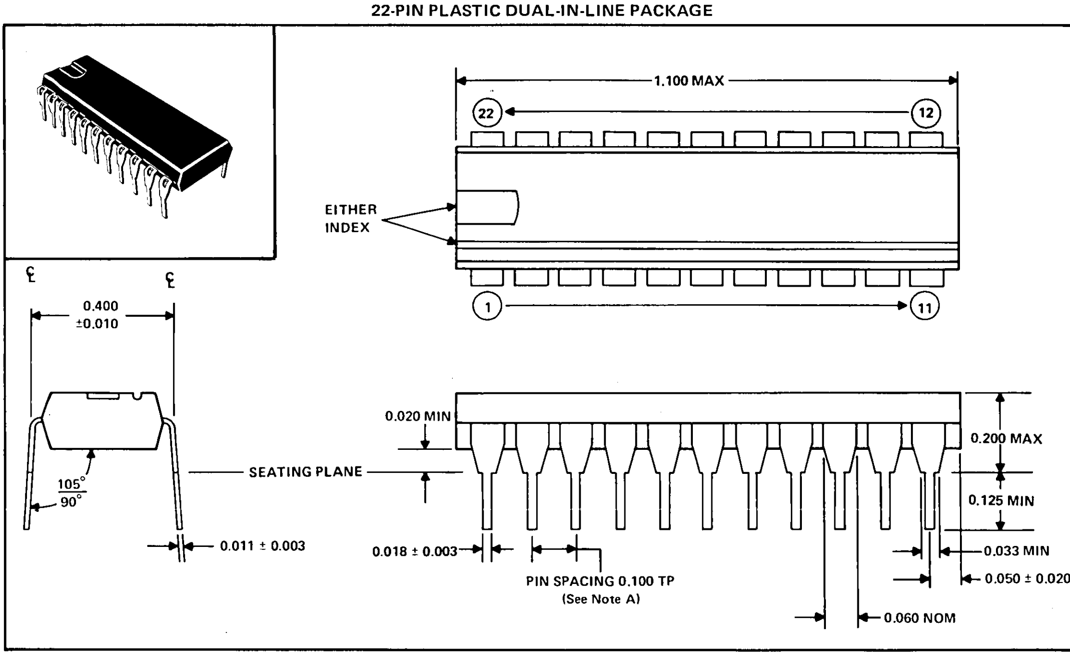
NOTES: A. Each pin centerline is located within 0.010 of its true longitudinal position.
B. All linear dimensions are in inches.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

18-PIN PLASTIC DUAL-IN-LINE PACKAGE



22-PIN PLASTIC DUAL-IN-LINE PACKAGE

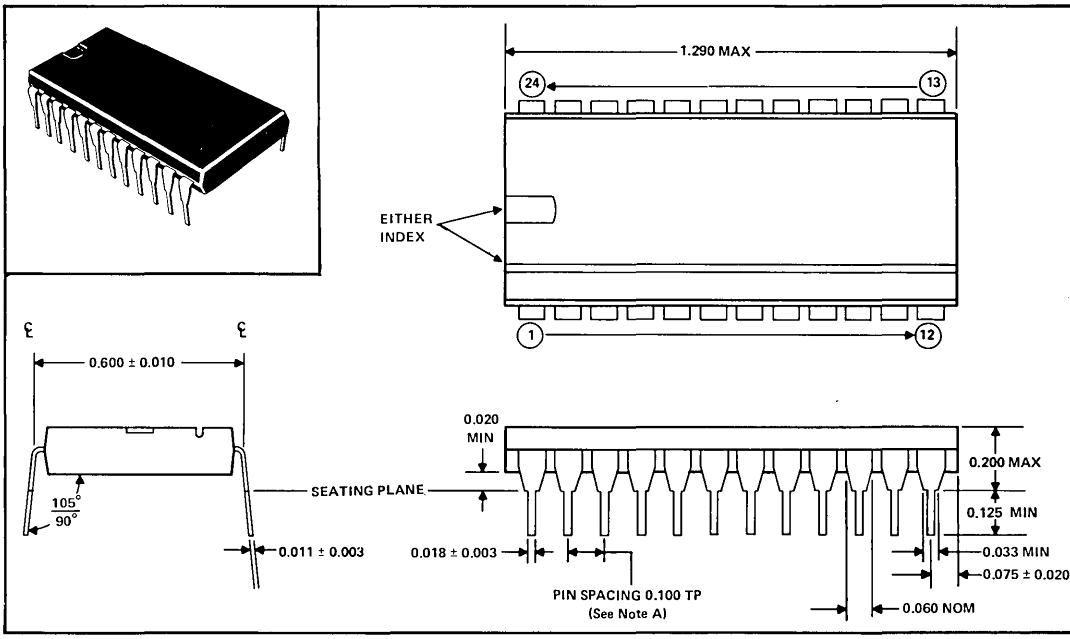


NOTES: A. Each pin centerline is located within 0.010 of its true longitudinal position.
B. All linear dimensions are in inches.

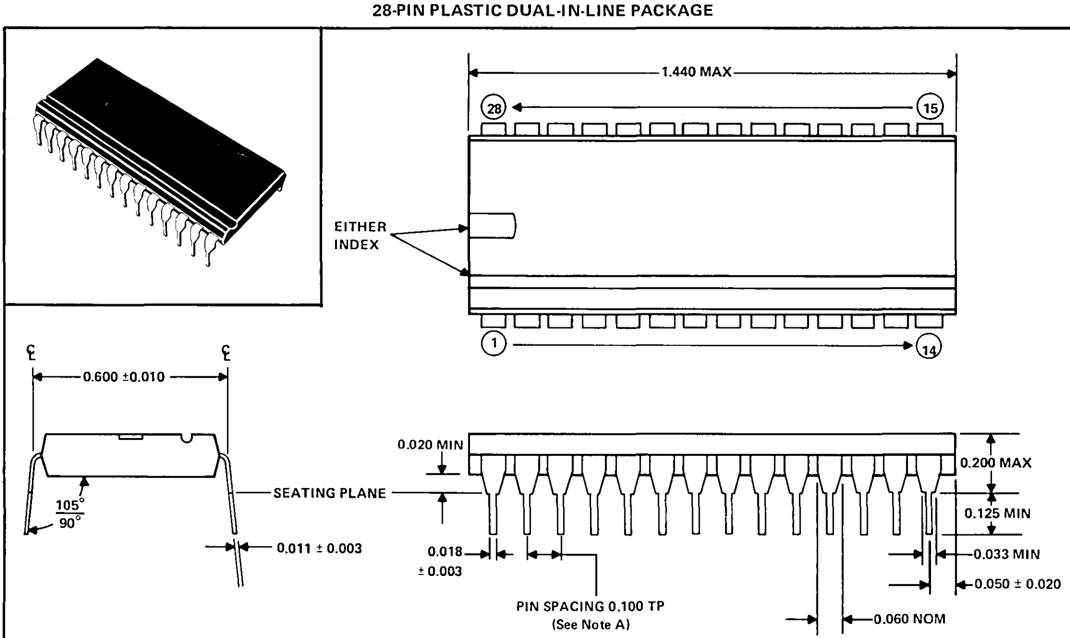
3

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

24-PIN PLASTIC DUAL-IN-LINE PACKAGE

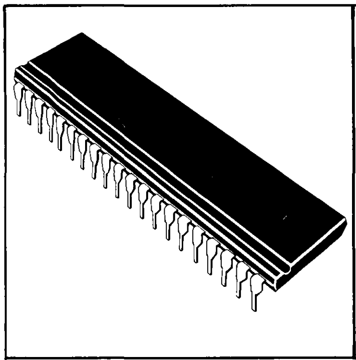


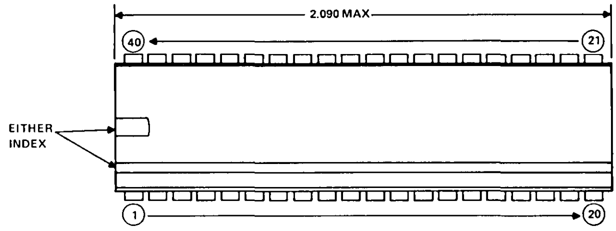
28-PIN PLASTIC DUAL-IN-LINE PACKAGE

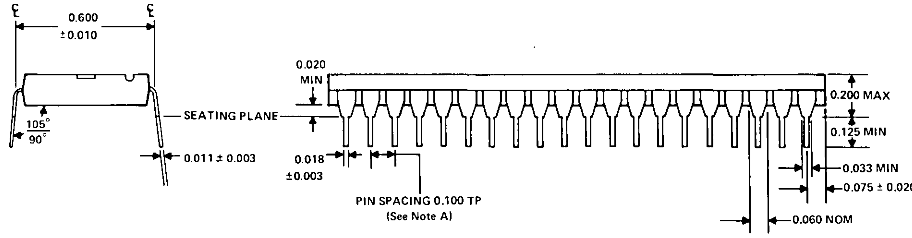


NOTES: A. Each pin centerline is located within 0.010 of its true longitudinal position.
B. All linear dimensions are in inches.

40-PIN PLASTIC DUAL-IN-LINE PACKAGE







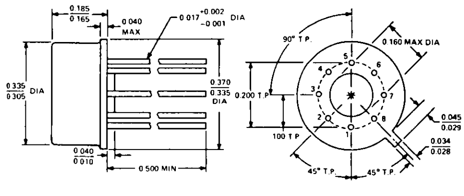
NOTES: A. Each pin centerline is located within 0.010 of its true longitudinal position.

B. All linear dimensions are in inches.

metal-can

For devices such as shift registers requiring few inputs and outputs, TI uses two metal-can packages.

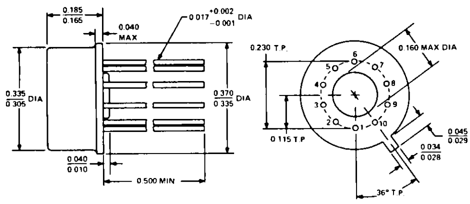
8-PIN METAL CAN



ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED

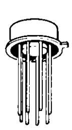
Same as JEDEC TO-99 and MO-002AK except for diameter of standoff

10-PIN METAL CAN



ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED

Same as JEDEC TO-100 and MO-006AD except for diameter of standoff

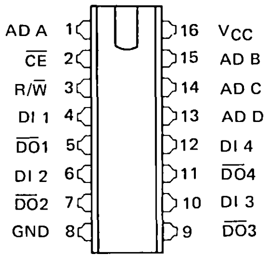


575

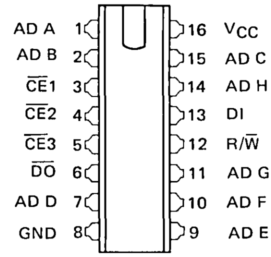
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TTL
Memories

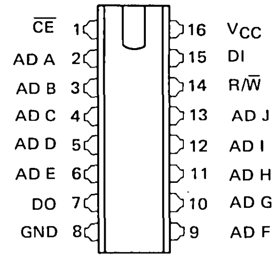
64 BITS (16 WORDS BY 4 BITS)
'S189, 'S289



256 BITS (256 WORDS BY 1 BIT)
'S201, 'S301



1024 BITS (1024 WORDS BY 1 BIT)
SN74S209, SN74S309



Pin assignments for all of these memories are the same for all packages.

- **Schottky-Clamped for High Performance**
- **Full On-Chip Decoding and Fast Chip-Enable Simplify System Decoding**
- **P-N-P Inputs Reduce Loading on System Buffers/Drivers**
- **Choice of 3-State or Open-Collector Outputs**

TYPE NUMBER (PACKAGES)		TYPE OF	BIT SIZE	TYPICAL ACCESS TIMES		WRITE CYCLE TIME	
−55°C to 125°C	0°C to 70°C	OUTPUT(S)	(ORGANIZATIONS)	CHIP-SELECT	ADDRESS	SN54S'	SN74S'
SN54S189(J, W)	SN74S189(J, N)	3-State	64 Bits	12 ns	25 ns	25 ns	25 ns
SN54S289(J, W)	SN74S289(J, N)	Open-Collector	(16 W x 4 B)				
SN54S201(J, W)	SN74S201(J, N)	3-State	256 Bits	13 ns	42 ns	100 ns	65 ns
SN54S301(J, W)	SN74S301(J, N)	Open-Collector	(256 W x 1 B)				
	SN74S209(J, N)	3-State	1024 Bits	20 ns	70 ns		150 ns
	SN74S309(J, N)	Open-Collector	(1024 W x 1 B)				

description

These monolithic TTL memories feature Schottky clamping for high performance, a fast chip-select access time to enhance decoding at the system level, and the 'S201 and 'S209 RAMs utilize inverted-cell memory elements to achieve high densities. The memories feature p-n-p input transistors that reduce the low-level input current requirement to a maximum of −0.25 milliamperes, only one-eighth that of a Series 54S/74S standard load factor.

A three-state-output version and an open-collector-output version are offered for each of the three organizations. A three-state output offers the convenience of an open-collector output with the speed of a totem-pole output; it can be bus-connected to other similar outputs, yet it retains the fast rise time characteristic of the TTL totem-pole output. An open-collector output offers the capability of direct interface with a data line having a passive pull-up.

write cycle

Information to be stored in the memory is written into the selected address (AD) location when the chip-enable ($\overline{CE}$) and the read/write (R/$\overline{W}$) inputs are low. While the read/write input is low, the memory output(s) is(are) off (three-state = Hi-Z, open-collector = high). When a number of outputs are bus-connected, this off state neither loads nor drives the data bus; however, it permits the bus line to be driven by other active outputs or a passive pull-up.

read cycle

Information stored in the memory (see function table for input/output phase relationship) is available at the output(s) when the read/write input is high and the chip-enable input(s) is(are) low. When one(or more) chip-enable input is(are) high, the output(s) will be off.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

FUNCTION TABLE

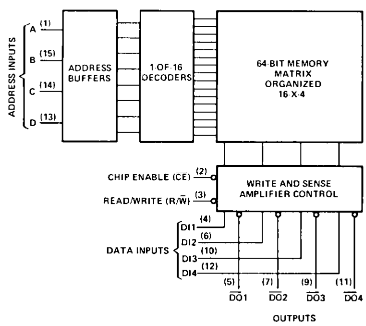
FUNCTION	INPUTS		OUTPUTS			
	CHIP ENABLE†	READ/ WRITE	'S189 'S201	'S289 'S301	SN74S209	SN74S309
Write	L	L	High Impedance	H	High Impedance	H
Read	L	H	Complement of Data Entered	Complement of Data Entered	Data Entered	Data Entered
Inhibit	H	X	High Impedance	H	High Impedance	H

H = high level, L = low level, X = irrelevant

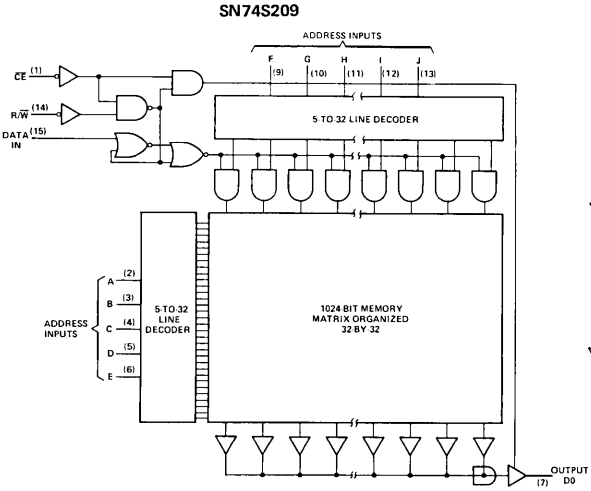
†For chip-enable of 'S201 and 'S301: L = all $\overline{CE}$ inputs low, H = one or more $\overline{CE}$ inputs high.

functional block diagrams

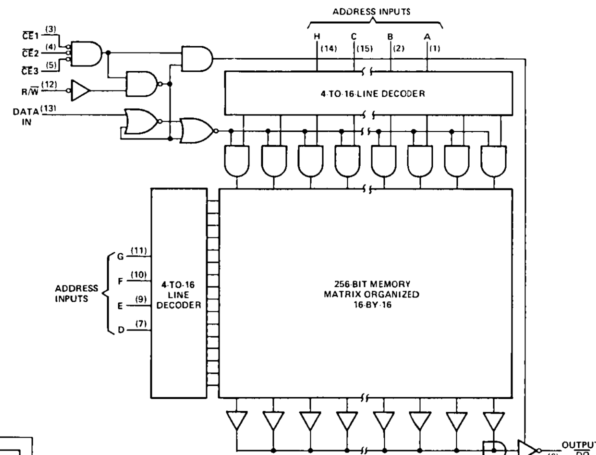
'S189, 'S289



SN74S209

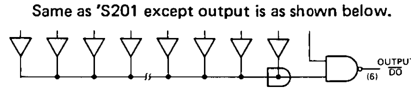


'S201



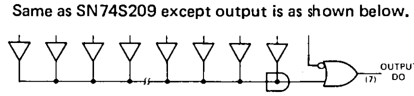
'S301

Same as 'S201 except output is as shown below.



SN74S309

Same as SN74S209 except output is as shown below.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)		7 V
Input voltage		5.5 V
Off-state output voltage		5.5 V
Operating free-air temperature range:	SN54S' Circuits	−55°C to 125°C
	SN74S' Circuits	0°C to 70°C
Storage temperature range		−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

recommended operating conditions

		SN54S189			SN74S189			SN54S201			SN74S201			SN74S209			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	4.5	5	5.5	4.75	5	5.25	4.75	5	5.25	V
High-level output current, I_{OH}				−2			−6.5			−2			−10.3			−10.3	mA
Low-level output current, I_{OL}				16			16			16			16			16	mA
Width of write pulse, $t_{w(wr)}$ (see Figure 1)		25			25			100			65			130			ns
Setup time (see Figure 1)	Address before write pulse, $t_{su(ad)}$	0↓			0↓			0↓			0↓			10↓			ns
	Chip enable before write pulse, $t_{su(\overline{CE})}$	0↓			0↓			0↓			0↓			10↓			
	Data before end of write pulse, $t_{su(da)}$	25↑			25↑			100↑			65↑			140↑			
Hold time (see Figure 1)	Address after write pulse, $t_{h(ad)}$	0↑			0↑			0↑			0↑			10↑			ns
	Chip enable after write pulse, $t_{h(\overline{CE})}$	0↑			0↑			0↑			0↑			10↑			
	Data after write pulse, $t_{h(da)}$	0↑			0↑			0↑			0↑			10↑			
Operating free-air temperature, T_A		−55		125	0		70	−55		125	0		70	0		70	°C

↑↓The arrow indicates the transition of the read/write input used for reference: ↑for the low-to-high-transition, ↓for the high-to-low transition.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			'S189			'S201			SN74S209			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			2			V
V_{IL}	Low-level input voltage						0.8			0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = ◆					−1.2			−1.2			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX		Series 54S'	2.4	3.4		2.4	3.3					V
				Series 74S'	2.4	3.2		2.4	2.9		2.4	2.9		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		Series 54S'		0.35	0.5		0.38	0.5				V
				Series 74S'		0.35	0.45		0.38	0.45		0.38	0.45	
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V, V_O = 2.4 V					50			40			100	μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V, V_O = 0.4 V					−50			−40			−100	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V					1			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V					25			25			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V					−250			−250			−250	μA
I_{OS}	Short-circuit output current§	V_{CC} = MAX			−30		−100	−30		−100	−30		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2	Series 54S'	T_A = MAX			110			115				mA
				T_A = 25°C		75	110		100	140				
				T_A = MIN			110			155				
			Series 74S'	Full range		75	110		100	140		110	140	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Duration of the short circuit should not exceed one second.
◆I_I = −18 mA for 'S189 and 'S201, −12 mA for 'S209.

NOTE 2: For the 'S189 I_{CC} is measured with the read/write and chip-enable inputs grounded, all other inputs at 4.5 V, and the outputs open.
For the 'S201 and SN74S209 I_{CC} is measured with all chip-enable inputs grounded, all other inputs at 4.5 V, and the output open.

recommended operating conditions

		SN54S289			SN74S289			SN54S301			SN74S301			SN74S309			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	4.5	5	5.5	4.75	5	5.25	4.75	5	5.25	V
High-level output voltage, V_{OH}				5.5			5.5			5.5			5.5			5.5	V
Low-level output current, I_{OL}				16			16			16			16			16	mA
Width of write pulse, $t_{w(wr)}$ (see Figure 1)		25			25			100			65			130			ns
Setup time (see Figure 2)	Address before write pulse, $t_{su(ad)}$	0↓			0↓			0↓			0↓			10↓			ns
	Chip enable before write pulse, $t_{su(\overline{CE})}$	0↓			0↓			0↓			0↓			10↓			
	Data before end of write pulse, $t_{su(da)}$	25↑			25↑			100↑			65↑			140↑			
Hold time (see Figure 2)	Address after write pulse, $t_{h(ad)}$	0↑			0↑			0↑			0↑			10↑			ns
	Chip enable after write pulse, $t_{h(\overline{CE})}$	0↑			0↑			0↑			0↑			10↑			
	Data after write pulse, $t_{h(da)}$	0↑			0↑			0↑			0↑			10↑			
Operating free-air temperature, T_A		−55		125	0		70	−55		125	0		70	0		70	°C

↑↓The arrow indicates the transition of the read/write input used for reference: ↑for the low-to-high-transition, ↓for the high-to-low transition.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			'S289			'S301			SN74S309			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			2			V
V_{IL}	Low-level input voltage						0.8			0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = ♦					−1.2			−1.2			−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V		V_O = 2.4 V			40			40			100	µA
				V_O = 5.5 V			100			100			250	
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		Series 54S'			0.5		0.38	0.5				V
				Series 74S'			0.45		0.38	0.45		0.38	0.45	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V					1			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V					25			25			25	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V					−250			−250			−250	µA
I_{CC}	Supply current	V_{CC} = MAX, See Note 3	Series 54S'	T_A = MAX			105			110				mA
				T_A = 25°C		75	105		100	140				
				T_A = MIN			105			155				
			Series 74S'	Full range		75	105		100	140		110	140	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
♦I_I = −18 mA for 'S289 and 'S301, −12 mA for 'S309.
NOTE 3: For the 'S289 I_{CC} is measured with the read/write and chip-enable inputs grounded, all other inputs at 4.5 V, and the outputs open.
For the 'S301 and SN74S309 I_{CC} is measured with all chip-enable inputs grounded, all other inputs at 4.5 V, and the output open.

switching characteristics over recommended operating ranges of T_A and V_{CC} (unless otherwise noted)

random-access memories with three-state outputs

PARAMETER			TEST CONDITIONS	SN54S189		SN74S189		SN54S201		SN74S201		SN74S209		UNIT
				TYP‡	MAX	TYP‡	MAX	TYP‡	MAX	TYP‡	MAX	TYP‡	MAX	
$t_{w(wr,min)}$	Minimum width of write pulse		C_L = 30 pF, R_L = 300 Ω, See Figure 1	15	25	15	25	40	100	40	65	65	85	ns
$t_{a(ad)}$	Access time from address			25	50	25	35	42	85	42	65	70	100	ns
$t_{a(\overline{CE})}$	Access time from chip enable (enable time)			12	25	12	17	13	40	13	30	20	40	ns
t_{SR}	Sense recovery time			22	40	22	35	20	50	20	40	20	40	ns
t_{PXZ}	Disable time from high or low level	from $\overline{CE}$	C_L = 5 pF, R_{L1} = 300 Ω, See Figure 1	12	25	12	17	9	30	9	20	15	30	ns
		from R/$\overline{W}$		12		12		13	45	13	35	25	40	

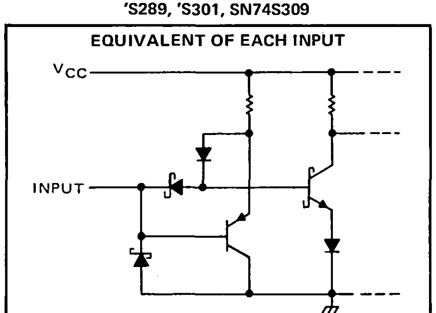
random-access memories with open-collector outputs

PARAMETER			TEST CONDITIONS	SN54S289		SN74S289		SN54S301		SN74S301		SN74S309		UNIT
				TYP‡	MAX	TYP‡	MAX	TYP‡	MAX	TYP‡	MAX	TYP‡	MAX	
$t_{w(wr,min)}$	Minimum width of write pulse		C_L = 30 pF, R_{L1} = 300 Ω, R_{L2} = 600 Ω, See Figure 2	15	25	15	25	40	100	40	65	65	85	ns
$t_{a(ad)}$	Access time from address			25	50	25	35	42	85	42	65	70	100	ns
$t_{a(\overline{CE})}$	Access time from chip enable (enable time)			12	25	12	17	13	40	13	30	20	40	ns
t_{SR}	Sense recovery time			22	40	22	35	20	50	20	40	20	40	ns
t_{PLH}	Propagation delay time, low-to-high-level output (disable time)	from $\overline{CE}$		12	25	12	17	8	30	8	20	15	30	ns
		from R/$\overline{W}$		12		12		15	45	15	35	25	40	

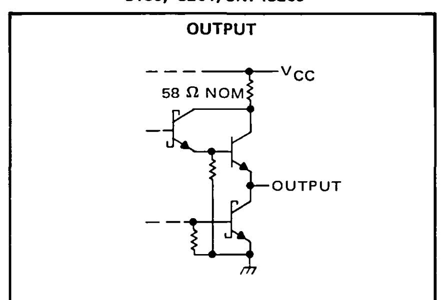
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

schematics of inputs and outputs

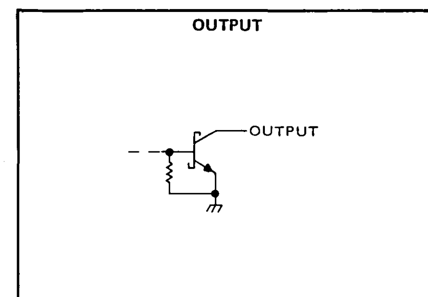
'S189, 'S201, SN74S209,
'S289, 'S301, SN74S309



'S189, 'S201, SN74S209

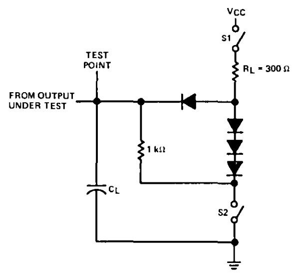


'S289, 'S301, SN74S309

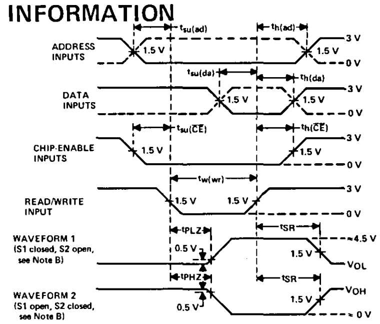


TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

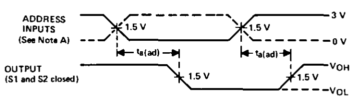
PARAMETER MEASUREMENT INFORMATION



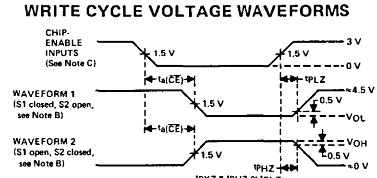
LOAD CIRCUIT



WRITE CYCLE VOLTAGE WAVEFORMS



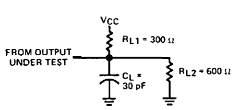
ACCESS TIME FROM ADDRESS INPUTS VOLTAGE WAVEFORMS



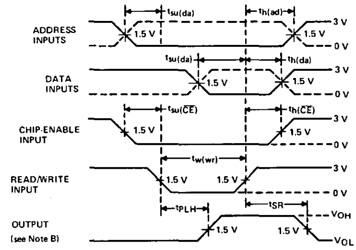
ACCESS (ENABLE) TIME AND DISABLE TIME FROM CHIP ENABLE VOLTAGE WAVEFORMS

NOTES:
- A. When measuring access times from address inputs, the chip enable input(s) is(are) low and the read/write is high.
- B. Waveform 1 is for the output with internal conditions such that the output is low except when disabled. Waveform 2 is for the output with internal conditions such that the output is high except when disabled.
- C. When measuring access and disable times from chip enable input(s), the address inputs are steady-state and the read/write input is high.
- D. Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leqslant 2.5$ ns, $t_f \leqslant 2.5$ ns, PRR $\leqslant 1$ MHz, and $Z_{out} \approx 50\ \Omega$.

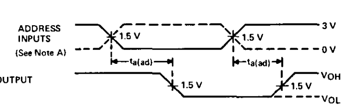
FIGURE 1–TESTING RAM's WITH 3-STATE OUTPUTS

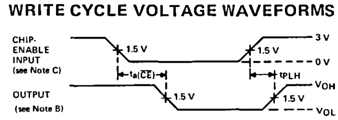


LOAD CIRCUIT



WRITE CYCLE VOLTAGE WAVEFORMS





ACCESS TIME FROM ADDRESS INPUTS VOLTAGE WAVEFORMS

ACCESS (ENABLE) TIME AND DISABLE TIME FROM CHIP ENABLE VOLTAGE WAVEFORMS

NOTES:
- A. When measuring access times from address inputs, the chip-enable input(s) is(are) low and the read/write input is high.
- B. Waveform shown is for the output with internal conditions such that the output is low except when disabled.
- C. When measuring access and disable times from chip-enable input(s), the address inputs are steady-state and the read/write input is high.
- D. Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leqslant 2.5$ ns, $t_f \leqslant 2.5$ ns, PRR $\leqslant 1$ MHz, and $Z_{out} \approx 50\ \Omega$.

FIGURE 2–TESTING RAM's WITH OPEN-COLLECTOR OUTPUTS

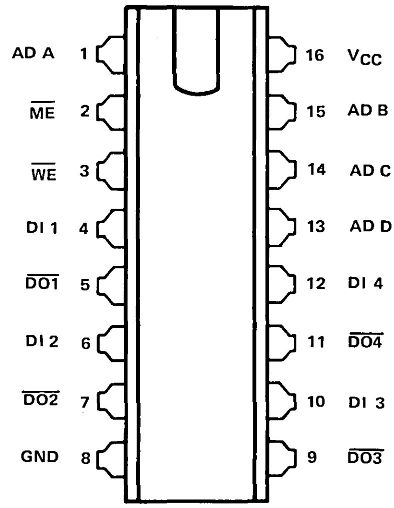
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPE SN7489
64-BIT RANDOM-ACCESS READ/WRITE MEMORY

BULLETIN NO. DL-S 7511386, DECEMBER 1972—REVISED MAY 1975

- For Application as a "Scratch Pad" Memory with Nondestructive Read-Out
- Fully Decoded Memory Organized as 16 Words of Four Bits Each
- Fast Access Time . . . 33 ns Typical
- Diode-Clamped, Buffered Inputs
- Open-Collector Outputs Provide Wire-AND Capability
- Typical Power Dissipation . . . 375 mW
- Compatible with Most TTL and DTL Circuits

J OR N PACKAGE



description

This 64-bit active-element memory is a monolithic, high-speed, transistor-transistor logic (TTL) array of 64 flip-flop memory cells organized in a matrix to provide 16 words of four bits each. Each of the 16 words is addressed in straight binary with full on-chip decoding.

The buffered memory inputs consist of four address lines, four data inputs, a write enable, and a memory enable for controlling the entry and access of data. The memory has open-collector outputs which may be wire-AND connected to permit expansion up to 4704 words of N-bit length without additional output buffering. Access time is typically 33 nanoseconds; power dissipation is typically 375 milliwatts.

$\overline{ME}$	$\overline{WE}$	OPERATION	CONDITION OF OUTPUTS
L	L	Write	Complement of Data Inputs
L	H	Read	Complement of Selected Word
H	L	Inhibit Storage	Complement of Data Inputs
H	H	Do Nothing	High

write operation

Information present at the data inputs is written into the memory by addressing the desired word and holding both the memory enable and write enable low. Since the internal output of the data input gate is common to the input of the sense amplifier, the sense output will assume the opposite state of the information at the data inputs when the write enable is low.

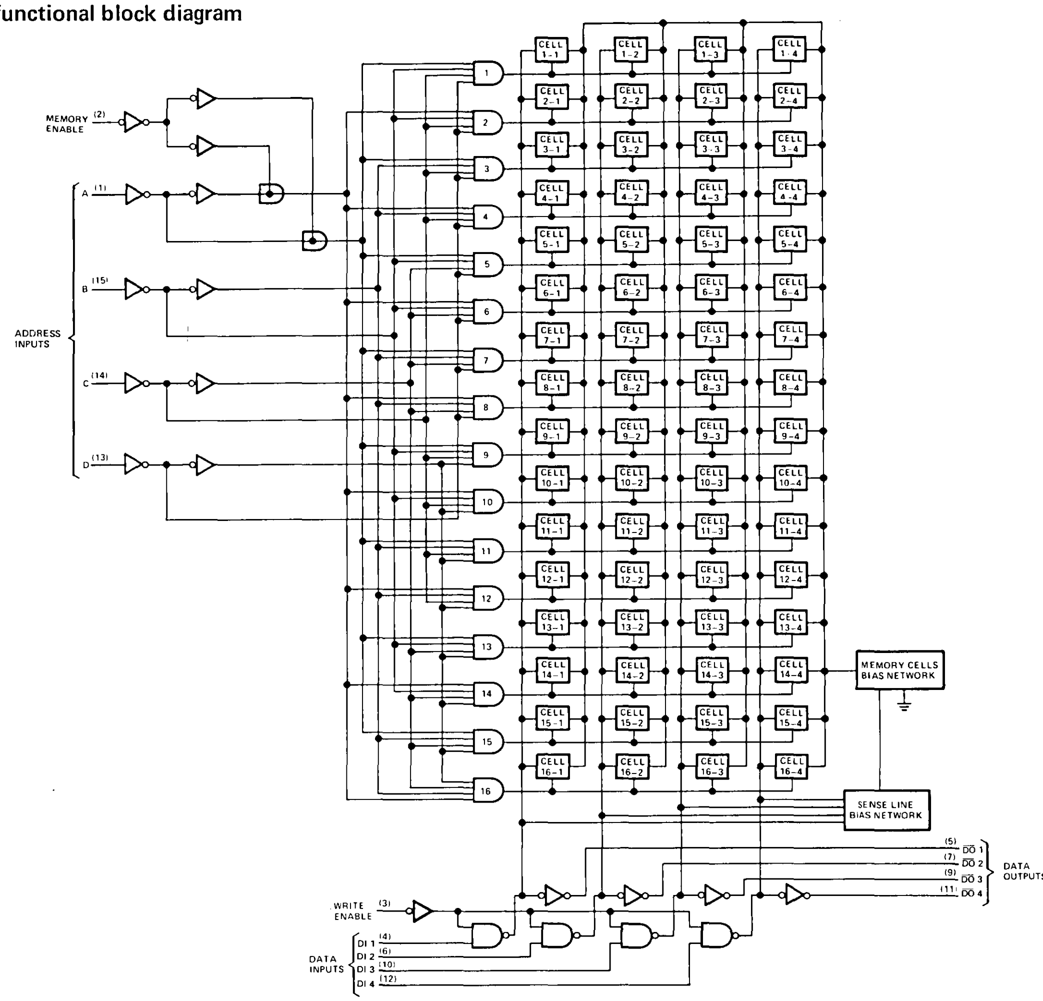
read operation

The complement of the information which has been written into the memory is nondestructively read out at the four sense outputs. This is accomplished by holding the memory enable low, the write enable high, and selecting the desired address.

4

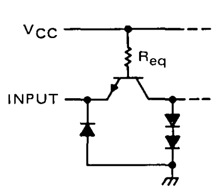
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

functional block diagram



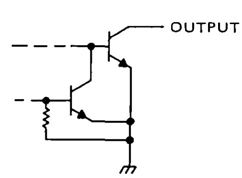
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



Data Inputs: R_{eq} = 6 kΩ NOM
All others: R_{eq} = 4 kΩ NOM

TYPICAL OF ALL OUTPUTS



575

4

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
High-level output voltage, V_{OH} (see Notes 1 and 2)	5.5 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the maximum voltage that should be applied to any output when it is in the off state.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Width of write-enable pulse, t_w	40			ns
Setup time, data input with respect to write enable, t_{su} (see Figure 1)	40			ns
Hold time, data input with respect to write enable, t_h (see Figure 1)	5			ns
Select input setup time with respect to write enable, t_{su}	0			ns
Select input hold time after writing, t_h (see Figure 1)	5			ns
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

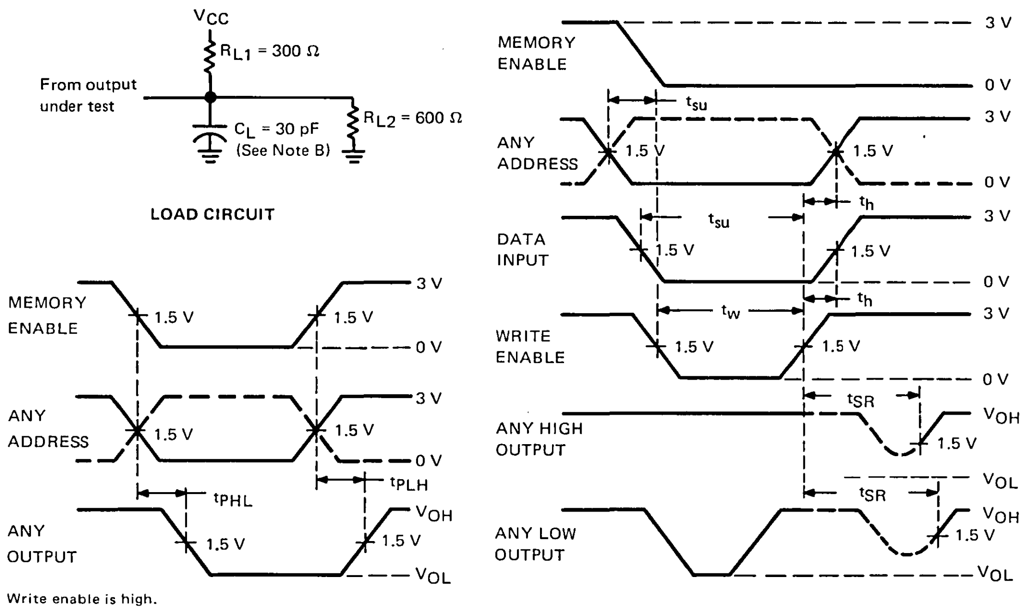
PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	$I_I = -12$ mA			−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, V_{OH} = 5.5 V			20	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V,	I_{OL} = 12 mA			0.4	V
			I_{OL} = 16 mA			0.45	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−1.6	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 3		75	105	mA
C_o	Off-state output capacitance	V_{CC} = 5 V, f = 1 MHz	V_O = 2.4 V,		6.5		pF

NOTE 3: I_{CC} is measured with the memory enable grounded, all other inputs at 4.5 V, and all outputs open.
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from memory enable		C_L = 30 pF, R_{L1} = 300 Ω, R_{L2} = 600 Ω, See Figure 1		26	50	ns
t_{PHL}	Propagation delay time, high-to-low-level output from memory enable				33	50	ns
t_{PLH}	Propagation delay time, low-to-high-level output from any address input				30	60	ns
t_{PHL}	Propagation delay time, high-to-low-level output from any address input				35	60	ns
t_{SR}	Sense recovery time after writing	output initially high			39	70	ns
		output initially low			48	70	ns

PARAMETER MEASUREMENT INFORMATION



READ CYCLE **WRITE CYCLE FROM WRITE ENABLE**

NOTES: A. The input pulse generators have the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 1—SWITCHING CHARACTERISTICS

TYPICAL CHARACTERISTICS

INPUT CURRENT vs INPUT VOLTAGE

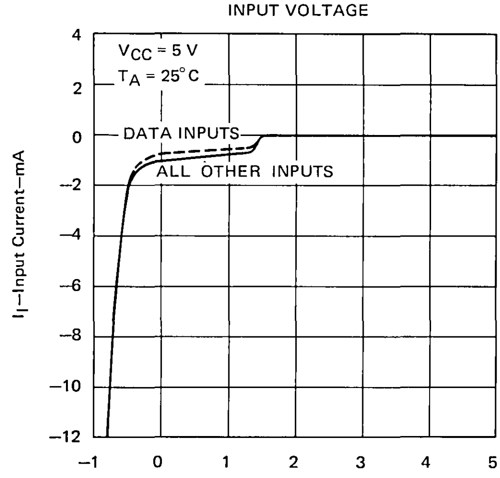


FIGURE 2

PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

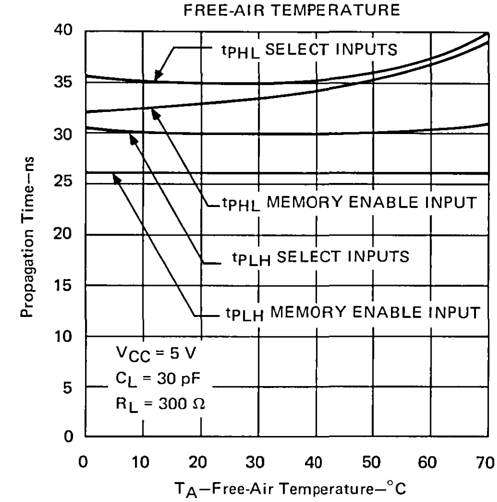


FIGURE 3

4

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

SERIES 54/74, 54S/74S
PROGRAMMABLE READ-ONLY MEMORIES

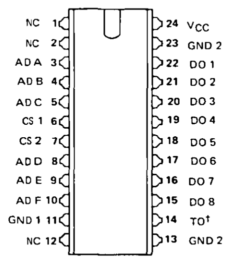
BULLETIN NO. DL-S 7512258, MAY 1975

- Titanium-Tungsten (Ti-W) Fuse Links for Fast, Low-Voltage, Reliable Programming
- All Schottky-Clamped PROM's Offer:
  - Fast Chip Select to Simplify System Decode
  - Choice of Three-State or Open-Collector Outputs
  - P-N-P Inputs for Reduced Loading on System Buffers/Drivers
- Full Decoding and Chip Select Simplify System Design
- Applications Include:
  - Microprogramming/Firmware Loaders
  - Code Converters/Character Generators
  - Translators/Emulators
  - Address Mapping/Look-Up Tables

TYPE NUMBER (PACKAGES)		BIT SIZE	OUTPUT	TYPICAL ACCESS TIME (ns)	
−55°C to 125°C	0°C to 70°C	(ORGANIZATION)	CONFIGURATION	FROM ADDRESS	FROM CHIP SELECT
SN54186(J, W)	SN74186(J, N)	512 bits (64 W x 8 B)	open-collector	50	55
SN54188A(J, W)	SN74188A(J,N)	256 bits (32 W x 8 B)	open-collector	30	34
SN54S188(J, W)	SN74S188(J, N)		open-collector	25	12
SN54S288(J, W)	SN74S288(J, N)		three-state	25	12
SN54S287(J, W)	SN74S287(J, N)	1024 bits (256 W x 4 B)	three-state	42	15
SN54S387(J, W)	SN74S387(J, N)		open-collector	42	15
SN54S470(J)	SN74S470(J, N)	2048 bits (256 W x 8 B)	open-collector	50	20
SN54S471(J)	SN74S471(J, N)		three-state	50	20
SN54S472(J)	SN74S472(J, N)	4096 bits (512 W x 8 B)	three-state	55	20
SN54S473(J)	SN74S473(J, N)		open-collector	55	20

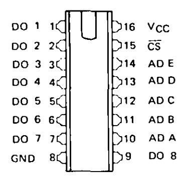
4

512 BITS
(64 WORDS BY 8 BITS)
'186

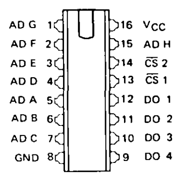


NC—No internal connection
†TO is used for testing purposes. The logic at TO is undefined.

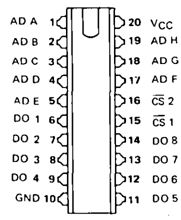
256 BITS
(32 WORDS BY 8 BITS)
'188A, 'S188, 'S288



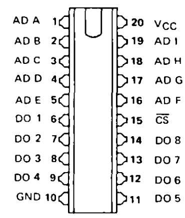
1024 BITS
(256 WORDS BY 4 BITS)
'S287, 'S387



2048 BITS
(256 WORDS BY 8 BITS)
'S470, 'S471



4096 BITS
(512 WORDS BY 8 BITS)
'S472, 'S473



Pin assignments for all of these memories are the same for all packages.

description

These monolithic TTL programmable read-only memories (PROM's) feature titanium-tungsten (Ti-W) fuse links with each link designed to program in one millisecond or less. The Schottky-clamped versions of these PROM's offer considerable flexibility for upgrading existing designs or improving new designs as they feature full Schottky clamping for improved performance, low-current MOS-compatible p-n-p inputs, choice of bus-driving three-state or open-collector outputs, and improved chip-select access times.

The high-complexity 2048- and 4096-bit PROM's can be used to significantly improve system density for fixed memories as all are offered in the 20-pin dual-in-line package having pin-row spacings of 0.300 inch.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

description (continued)

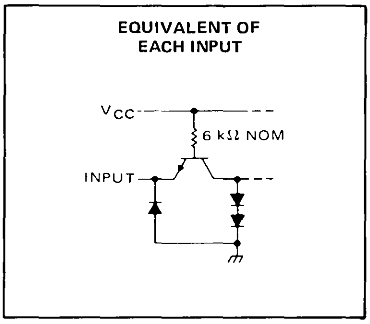
Data can be electronically programmed, as desired, at any bit location in accordance with the programming procedure specified. All PROM's, except the 'S287 and 'S387, are supplied with a low-logic-level output condition stored at each bit location. The programming procedure open-circuits Ti-W metal links, which reverses the stored logic level at selected locations. The procedure is irreversible; once altered, the output for that bit location is permanently programmed. Outputs never having been altered may later be programmed to supply the opposite output level. Operation of the unit within the recommended operating conditions will not alter the memory content.

A low level at the chip-select input(s) enables each PROM except the '186, which is enabled by a high level at both chip-select inputs. The opposite level at any chip-select input causes the outputs to be off.

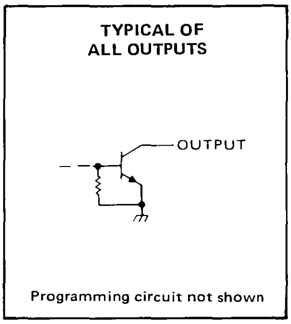
The three-state output offers the convenience of an open-collector output with the speed of a totem-pole output; it can be bus-connected to other similar outputs yet it retains the fast rise time characteristic of the TTL totem-pole output. The open-collector output offers the capability of direct interface with a data line having a passive pull-up.

schematics of inputs and outputs

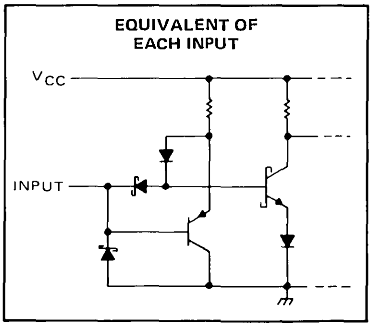
'186, '188A



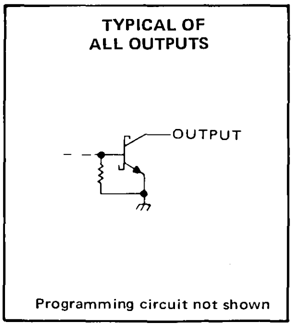
'186, '188A



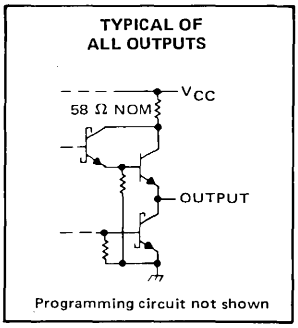
'S188, 'S287, 'S288, 'S387
'S470, 'S471, 'S472, 'S473



'S188, 'S387,
'S470, 'S473



'S287, 'S288
'S471, 'S472



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage (see Note 1)		7 V
Input voltage		5.5 V
Off-state output voltage		5.5 V
Operating free-air temperature range:	SN54', SN54S' Circuits	−55°C to 125°C
	SN74', SN74S' Circuits	0°C to 70°C
Storage temperature range		−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal (GND 2 of '186),. For '186 GND 1 and both GND 2 terminals are all connected to system ground except during programming. The supply-voltage rating does not apply during programming of the '188, '188A, or the 54S/74S PROM's.

4

recommended conditions for programming

		MIN	NOM	MAX	UNIT
Supply voltages (see Note 2)	V_{CC}	4.75	5	5.25	V
	GND 1	−5		−6†	V
Input conditions (see Note 3 and 4)	High level	Open circuit or equivalent			
	Low level	−5		−6†	V
Output voltage				−6.5†‡	V
Output current, output being programmed		−95	−120	−130	mA
Duration of programming pulse (see Note 5)		1		20	ms
Programming duty cycle			25	35	%
Free-air temperature		0		55	°C

†Absolute maximum ratings. ‡Clamp to ensure output does not exceed −0.5 V with respect to GND 1.

NOTES: 2. Voltage values are with respect to the GND 2 terminals.
3. The high-level (off) output of a Series 54/74 or 54S/74S open-collector gate with no pull-up resistor meets the requirements for a high-level input condition.
4. The low-level input voltage must be within ±0.5 volts of the applied voltage at GND 1.
5. Programming is guaranteed if the pulse is applied to the output for 10 ms. Typically, programming occurs in less than 1 ms.

step-by-step programming procedure

Programming the SN54186 or SN74186 is performed individually for each of the 512 bit locations and consists basically of applying a current pulse to each output terminal where a low logic level is to be changed to a high (off) level. The power supply and ground connections described below are designed to ensure that alteration of the memory content occurs during the programming procedure only.

1. Connect the memory as shown in Figure 1. To address a particular word in the memory, set the input switches to the binary equivalent of that word where a low logic level is as specified under "recommended conditions for programming" and a high logic level is either an open circuit or connection to an open-collector TTL gate with no pull-up resistor.
2. Apply a programming current pulse as specified to the pin associated with the first bit to be changed from a low-level to a high-level output.
3. Repeat Step 2 for each high-level output desired in the word addressed (program only one bit at a time). Any bit that is to remain at a low level should have its respective output open-circuited during the entire programming cycle for the addressed word.
4. Set the next input address and repeat steps 2 and 3 at a programming duty cycle of 35% maximum. This procedure is repeated for each input address for which a specific output word pattern is desired. A low logic level can always be changed to a high logic level simply by repeating Steps 1 and 2. Once programmed to provide a high logic level, the output cannot be changed to supply a low logic level.

NOTE: When verification indicates that a bit did not program, repeat steps 2 through 4. If the bit did not program after the second application of a 1-millisecond programming pulse, repeat steps 2 through 4 using programming pulse time of 10 to 20 milliseconds. Regardless of the programming pulse duration, its total average pulse time should be no more than 35% of the programming cycle.

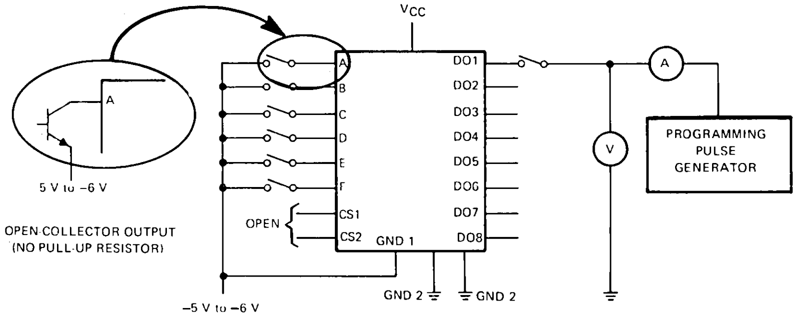


FIGURE 1—PROGRAMMING CONNECTIONS

recommended conditions for programming

		'188A			SN54S', SN74S'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 6)	Steady state	4.75	5	5.75	4.75	5	5.75	V
	Program pulse	10	10.5	11†	10	10.5	11†	V
Input voltage	High level, V_{IH}	2.4		5	2.4		5	V
	Low level, V_{IL}	0		0.5	0		0.5	V
Termination of all outputs except the one to be programmed		See load circuit (Figure 2)			See load circuit (Figure 2)			
Voltage applied to output to be programmed, $V_{O(pr)}$ (see Note 7)			0.25	+0.3 −0.8	0	0.25	0.3	V
Duration of V_{CC} programming pulse Y (see Figure 3 and Note 8)		1		20	1		20	ms
Programming duty cycle			25	35		25	35	%
Free-air temperature		0		55	0		55	°C

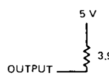
† Absolute maximum ratings.

NOTES: 6. Voltage values are with respect to the GND 2 terminals.
7. The '188A, 'S188, 'S288, 'S470, 'S471, 'S472, and 'S473 are supplied with all bit locations containing a low logic level, and programming a bit changes the output of the bit to high logic level. The 'S287 and 'S387 are supplied with all bit outputs at a high logic level, and programming a bit changes it to a low logic level.
8. Programming is guaranteed if the pulse applied is 10 ms long. Typically, programming occurs in 1 ms.

step-by-step programming procedure

1. Apply steady-state supply voltage (V_{CC} = 5 V) and address the word to be programmed.
2. Verify that the bit location needs to be programmed. If not, proceed to the next bit.
3. If the bit requires programming, disable the outputs by applying a high-logic-level voltage to the chip-select input(s).
4. Only one bit location is programmed at a time. Connect each output not being programmed to 5 V through 3.9 kΩ and apply the voltage specified in the table to the output to be programmed. Maximum current out of the programming output supply during programming is 150 mA.
5. Step V_{CC} to 10.5 V nominal. Maximum supply current required during programming is 750 mA.
6. Apply a low-logic-level voltage to the chip-select input(s). This should occur between 10 μs and 1 ms after V_{CC} has reached its 10.5-V level. See programming sequence of Figure 3.
7. After the X pulse time (1 ms) is reached, a high logic level is applied to the chip-select inputs to disable the outputs.
8. Within 10 μs to 1 ms after the chip-select input(s) reach a high logic level, V_{CC} should be stepped down to 5 V at which level verification can be accomplished.
9. The chip-select input(s) may be taken to a low logic level (to permit program verification) 10 μs or more after V_{CC} reaches its steady-state value of 5 V.
10. At a Y pulse duty cycle of 35% or less, repeat steps 1 through 8 for each output where it is desired to program a bit.

NOTES: A) V_{CC} should be removed between program pulses to reduce dissipation and chip temperatures. See Figure 3.
B) When verification indicates that a bit did not program, repeat steps 3 through 9. If the bit did not program after the second application of a 1-ms X pulse, repeat steps 3 through 9 using an X pulse time of 10 to 20 ms. Regardless of the X duration, the total average pulse time of Y should be no more than 35% of the programming cycle.



LOAD CIRCUIT FOR EACH OUTPUT NOT BEING PROGRAMMED OR FOR PROGRAM VERIFICATION
FIGURE 2

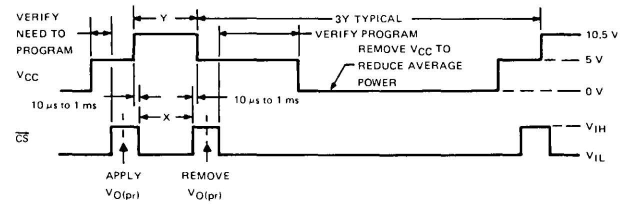


FIGURE 3—VOLTAGE WAVEFORMS FOR PROGRAMMING

recommended operating conditions

	SN54186 SN54188A			SN74186 SN74188A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			12			12	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		'186			'188A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−1.5			−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	V_{OH} = 2.4 V			100				μA
			V_{OH} = 5.5 V			200			100	
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 12 mA				0.4			0.45	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V				40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−1			−1	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 9	Both CS at 0 V		47	95				mA
			Both CS at 4.5 V		80	120				
I_{CCH}	Supply current, all outputs high	V_{CC} = MAX	See Note 10					50	80	mA
I_{CCL}	Supply current, all outputs low		See Note 11					82	110	
C_o	Off-state output capacitance	V_{CC} = 5 V, V_O = 2 V,	f = 1 MHz		6.5			6.5		pF

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTES: 9. I_{CC} of '186 is measured with all outputs open and the address inputs at 4.5 V. Typical values are for 50% of the bits programmed.
10. I_{CCH} of '188A is measured with all inputs at 4.5 V, all outputs open.
11. I_{CCL} of '188A is measured with the chip-select input grounded, all other inputs at 4.5 V, and all outputs open. The typical value shown is for the worst-case condition of all eight outputs low at one time. This condition may not be possible after the device has been programmed.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

TYPE	TEST CONDITIONS	$t_{a(ad)}$ (ns) Access time from address		$t_{a(CS/\overline{CS})}$ (ns) Access time from chip select (enable time)		t_{PLH} (ns) Propagation delay time, low-to-high-level output from chip select (disable time)	
		TYP	MAX	TYP	MAX	TYP	MAX
'186	C_L = 30 pF, R_{L1} = 400 Ω,	50	75	55	75	40	75
'188A	R_{L2} = 600 Ω, See Figure 4	30	50	34	50	23	50

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

recommended operating conditions

		'S188			'S387, 'S470, 'S473			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	Series 54S	4.5	5	5.5	4.5	5	5.5	V
	Series 74S	4.75	5	5.25	4.75	5	5.25	
High-level output voltage, V_{OH}				5.5			5.5	V
Low-level output current, I_{OL}				20			16	mA
Operating free-air temperature, T_A	Series 54S	−55		125	−55		125♦	°C
	Series 74S	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.2	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	V_{OH} = 2.4 V			50	µA
			V_{OH} = 5.5 V			100	
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = MAX			0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V			25	µA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.5 V			−250	µA
I_{CC}	Supply current	V_{CC} = MAX,	'S188		80	110	mA
		Chip select(s) at 0 V,	'S387		100	135	
		Outputs open,	'S470		110	155	
		See Note 12	'S473		120		

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

TYPE	TEST CONDITIONS	$t_{a(ad)}$ (ns) Access time from address		$t_{a(\overline{CS})}$ (ns) Access time from chip select (enable time)		t_{PLH} (ns) Propagation delay time, low-to-high-level output from chip select (disable time)	
		TYP‡	MAX	TYP‡	MAX	TYP‡	MAX
SN54S188	C_L = 30 pF, R_{L1} = 300 Ω, R_{L2} = 600 Ω, See Figure 4	25	50	12	30	12	30
SN74S188		25	40	12	25	12	25
SN54S387		42	75	15	40∮	15	40∮
SN74S387		42	65	15	35	15	35
SN54S470		50	80	20	40	15	35
SN74S470		50	70	20	35	15	30
SN54S473		55		20		15	
SN74S473		55		20		15	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
♦An SN54S387 in the W package operating at free-air temperatures above 108°C requires a heat sink that provides a thermal resistance from case to free air, $R_{\theta CA}$, of not more than 42 °C/W.
∮Tentative specifications.
NOTE 12: The typical values of I_{CC} shown are with all outputs low.

4

recommended operating conditions

		'S287 'S471, 'S472			'S288			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	Series 54S	4.5	5	5.5	4.5	5	5.5	V
	Series 74S	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}	Series 54S			−2			−2	mA
	Series 74S			−6.5			−6.5	
Low-level output current, I_{OL}				16			20	mA
Operating free-air temperature, T_A	Series 54S	−55		125	−55		125♦	°C
	Series 74S	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54S'			SN74S'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = MAX	2.4	3.4		2.4	3.2		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = MAX			0.5			0.5	V
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_O = 2.4 V	V_{IH} = 2 V,			50			50	μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_O = 0.5 V	V_{IH} = 2 V,			−50			−50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V			25			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.5 V			−250			−250	μA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−30		−100	−30		−100	mA
I_{CC}	Supply current	V_{CC} = MAX,	'S287		100	135		100	135	mA
		Chip select(s) at 0 V,	'S288		80	110		80	110	
		Outputs open,	'S471		110	155		110	155	
		See Note 12	'S472		120			120		

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

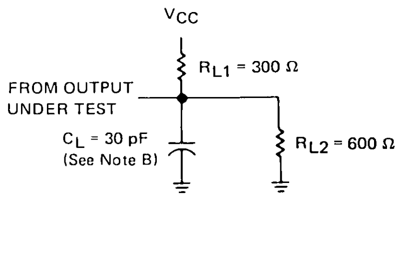
TYPE	TEST CONDITIONS	$t_{a(ad)}$ (ns) Access time from address		$t_{a(\overline{CS})}$ (ns) Access time from chip select (enable time)		t_{PXZ} (ns) Disable time from high or low level	
		TYP‡	MAX	TYP‡	MAX	TYP‡	MAX
SN54S287	C_L = 30 pF for $t_{a(ad)}$ and $t_{a(\overline{CS})}$, 5 pF for t_{PXZ}; R_L = 300 Ω; See Figure 5	42	75∮	15	40∮	12	
SN74S287		42	65	15	35	12	
SN54S288		25	50	12	30	8	30
SN74S288		25	40	12	25	8	20
SN54S471		50	80	20	40	15	35
SN74S471		50	70	20	35	15	30
SN54S472		55		20		15	
SN74S472		55		20		15	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
♦An SN54S287 in the W package operating at free-air temperatures above 108°C requires a heat sink that provides a thermal resistance from case-to-free-air, $R_{\theta CA}$, of not more than 42°C/W.
NOTE 12: The typical values of I_{CC} shown are with all outputs low.
∮Tentative specifications

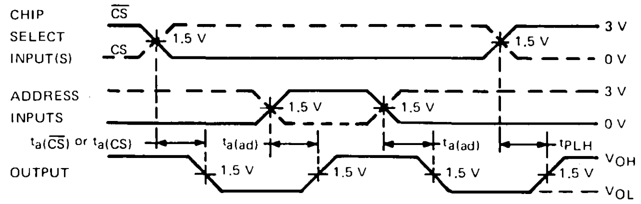
4

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION



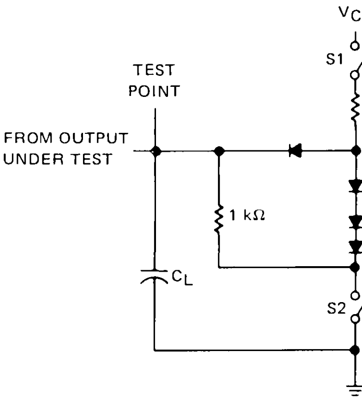
LOAD CIRCUIT



VOLTAGE WAVEFORMS

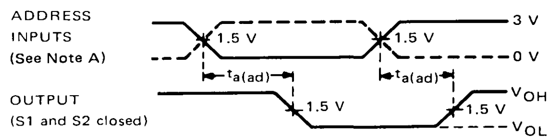
NOTES: A. The input pulse generator has the following characteristics: $Z_{out} \approx 50\ \Omega$ and PRR $\leqslant$ 1 MHz. For Series 54/74, $t_r \leqslant 7$ ns, $t_f \leqslant 7$ ns. For Series 54S/74S, $t_r \leqslant 2.5$ ns, $t_f \leqslant 2.5$ ns.
B. C_L includes probe and jig capacitance.
C. The pulse generator is connected to the input under test. The other inputs, memory content permitting, are connected so that the input will switch the output under test.

FIGURE 4—SWITCHING TIMES OF '186, '188A, 'S188, 'S470, 'S387, AND 'S473

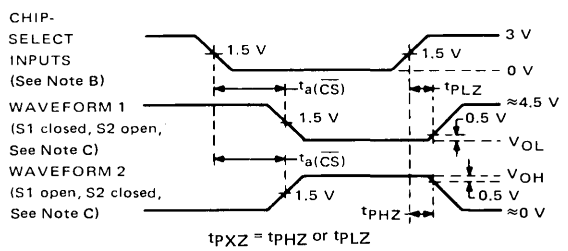


C_L includes probe and jig capacitance.
All diodes are 1N3064.

LOAD CIRCUIT



ACCESS TIME FROM ADDRESS INPUTS VOLTAGE WAVEFORMS



ACCESS (ENABLE) TIME AND DISABLE TIME FROM CHIP SELECT VOLTAGE WAVEFORMS

NOTES: A. When measuring access times from address inputs, the chip-select input(s) is(are) low.
B. When measuring access and disable times from chip-select input(s), the address inputs are steady-state.
C. Waveform 1 is for the output with internal conditions such that the output is low except when disabled. Waveform 2 is for the output with internal conditions such that the output is high except when disabled.
D. Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leqslant 2.5$ ns, $t_f \leqslant 2.5$ ns, PRR $\leqslant$ 1 MHz, and $Z_{out} \approx 50\ \Omega$.

FIGURE 5—SWITCHING TIMES OF 'S287, 'S288, 'S471, AND 'S472

PRINTED IN U.S.A.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

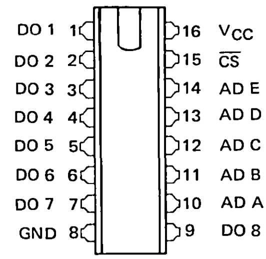
SERIES 54/74, 54S/74S READ-ONLY MEMORIES

BULLETIN NO. DL-S 7512259, MAY 1975

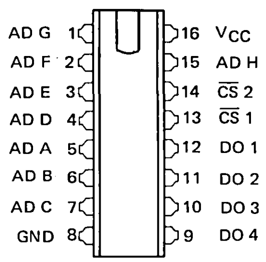
- Mask-Programmed Memories That Can Replace PROMs
- Full On-Chip Decoding and Fast Chip Select(s) Simplify System Decoding
- All Schottky-Clamped ROMs Offer
  - —Choice of 3-State or Open-Collector Outputs
  - —P-N-P Inputs for Reduced Loading on System Buffers/Drivers
- Applications Include:
  - —Microprogramming Firmware/Firmware Loaders
  - —Code Converters/Character Generators
  - —Translators/Emulators
  - —Address Mapping/Look-Up Tables

TYPE NUMBER (PACKAGES)		TYPE OF	BIT SIZE	TYPICAL ACCESS TIMES	
−55°C to 125°C	0°C to 70°C	OUTPUT(S)	(ORGANIZATION)	CHIP-SELECT	ADDRESS
SN5488A(J, W)	SN7488A(J, N)	Open-Collector	256 Bits (32 W x 8 B)	22 ns	26 ns
SN54187(J, W)	SN74187(J, N)	Open-Collector	1024 Bits (256 W x 4 B)	20 ns	40 ns
SN54S270(J)	SN74S270(J, N)	Open-Collector	2048 Bits (512 W x 4 B)	15 ns	45 ns
SN54S370(J)	SN74S370(J, N)	3-State			
SN54S271(J)	SN74S271(J, N)	Open-Collector	2048 Bits (256 W x 8 B)	15 ns	45 ns
SN54S371(J)	SN74S371(J, N)	3-State			

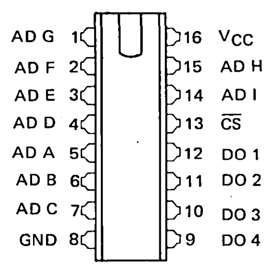
256 BITS (32 WORDS BY 8 BITS)
'88A



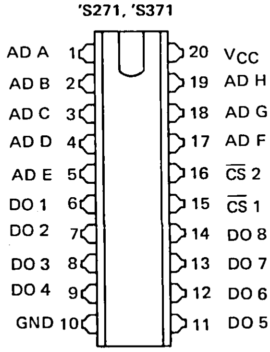
1024 BITS (256 WORDS BY 4 BITS)
'187



2048 BITS (512 WORDS BY 4 BITS)
'S270, 'S370



2048 BITS (256 WORDS BY 8 BITS)
'S271, 'S371



Pin assignments for all of these memories are the same for all packages.

description

These monolithic TTL custom-programmed read-only memories (ROMs) are particularly attractive for applications requiring medium to large quantities of the same bit pattern. Plug-in replacements can be obtained for most of the popular TTL PROMs.

The high-complexity 2048-bit ROMs can be used to significantly improve system bit density for fixed memory as all are offered in compact 16- or 20-pin dual-in-line packages having pin-row spacings of 0.300-inch.

The Schottky-clamped versions offer considerable flexibility for upgrading existing designs or improving new designs as they feature improved performance; plus, they offer low-current MOS-compatible p-n-p inputs, choice of bus-driving three-state or open-collector outputs, and improved chip-select access times.

Data from a sequenced deck of data cards punched according to the specified format are permanently programmed by the factory into the monolithic structure for all bit locations. Upon receipt of the order, Texas Instruments will assign a special identifying number for each pattern programmed according to the order. The completed devices will be marked with the appropriate TI special device number. It is important that the customer specify not only the output levels desired at all bit locations, but also the other information requested under ordering instructions.

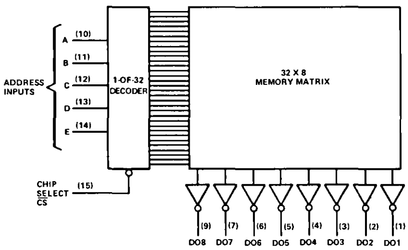
The three-state outputs offer the convenience of an open-collector output with the speed of a totem-pole output: they can be bus-connected to other similar outputs yet they retain the fast rise time characteristic of the TTL totem-pole output. The open-collector outputs offer the capability of direct interface with a data line having a passive pull-up.

Word-addressing is accomplished in straight positive-logic binary and the memory may be read when all $\overline{CS}$ inputs are low. A high at any $\overline{CS}$ input causes the outputs to be off.

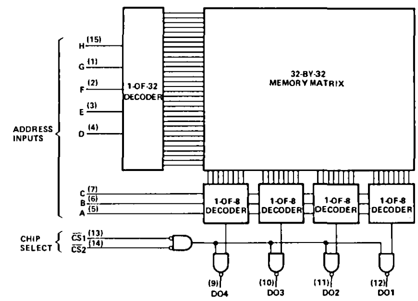
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

functional block diagrams

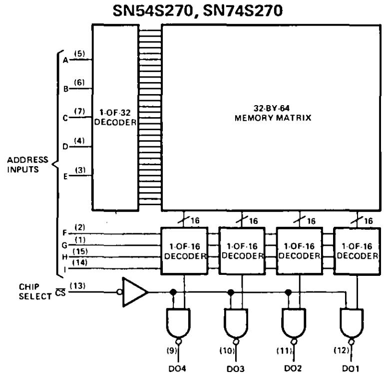
SN5488A, SN7488A



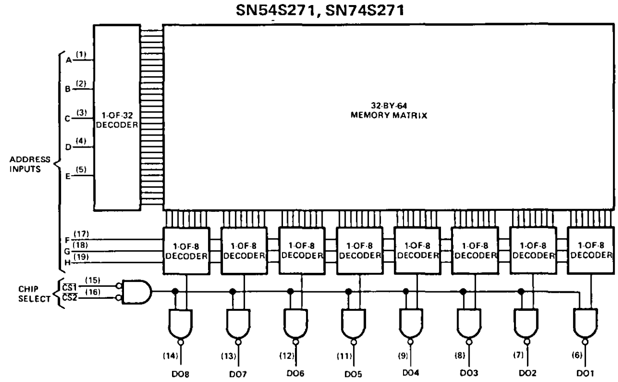
SN54187, SN74187



SN54S270, SN74S270

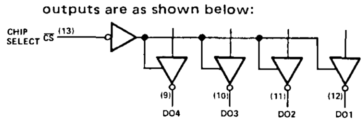


SN54S271, SN74S271



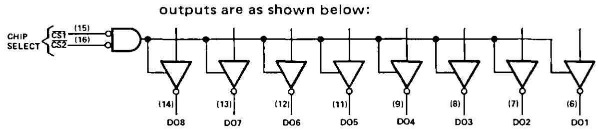
SN54S370, SN74S730

Same as SN54S270, SN74S270 except outputs are as shown below:



SN54S371, SN74S371

Same as SN54S271, SN74S271 except outputs are as shown below:



word addressing

'88A

WORD ADDRESS TABLE

WORD	INPUTS				
	E	D	C	B	A
0	L	L	L	L	L
1	L	L	L	L	H
2	L	L	L	H	L
3	L	L	L	H	H
4	L	L	H	L	L
5	L	L	H	L	H
6	L	L	H	H	L
7	L	L	H	H	H
8	L	H	L	L	L
	Words 9 thru 26 omitted				
27	H	H	L	H	H
28	H	H	H	L	L
29	H	H	H	L	H
30	H	H	H	H	L
31	H	H	H	H	H

'187, 'S271, 'S371

WORD ADDRESS TABLE

WORD	INPUTS							
	H	G	F	E	D	C	B	A
0	L	L	L	L	L	L	L	L
1	L	L	L	L	L	L	L	H
2	L	L	L	L	L	L	H	L
3	L	L	L	L	L	L	H	H
4	L	L	L	L	L	H	L	L
5	L	L	L	L	L	H	L	H
6	L	L	L	L	L	H	H	L
7	L	L	L	L	L	H	H	H
8	L	L	L	L	H	L	L	L
	Words 9 thru 250 omitted							
251	H	H	H	H	H	L	H	H
252	H	H	H	H	H	H	L	L
253	H	H	H	H	H	H	L	H
254	H	H	H	H	H	H	H	L
255	H	H	H	H	H	H	H	H

'S270, 'S370

WORD ADDRESS TABLE

WORD	INPUTS								
	I	H	G	F	E	D	C	B	A
0	L	L	L	L	L	L	L	L	L
1	L	L	L	L	L	L	L	L	H
2	L	L	L	L	L	L	L	H	L
3	L	L	L	L	L	L	L	H	H
4	L	L	L	L	L	L	H	L	L
5	L	L	L	L	L	L	H	L	H
6	L	L	L	L	L	L	H	H	L
7	L	L	L	L	L	L	H	H	H
8	L	L	L	L	L	H	L	L	L
	Words 9 thru 506 omitted								
507	H	H	H	H	H	H	L	H	H
508	H	H	H	H	H	H	H	L	L
509	H	H	H	H	H	H	H	L	H
510	H	H	H	H	H	H	H	H	L
511	H	H	H	H	H	H	H	H	H

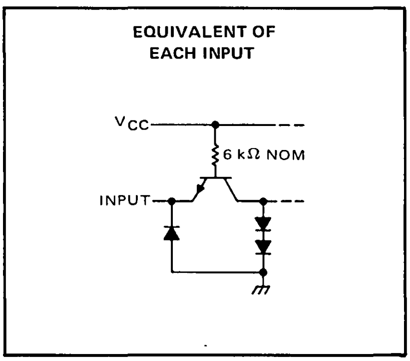
Word selection is accomplished in a conventional positive-logic binary code with the A address input being the least-significant bit progressing alphabetically through the address inputs to the most-significant bit.

SERIES 54/74, 54S/74S
READ-ONLY MEMORIES

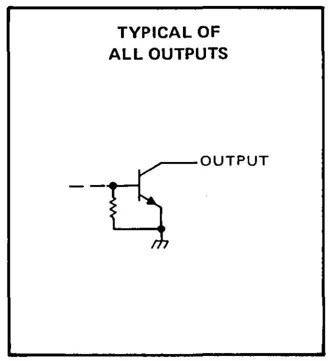
4

schematics of inputs and outputs

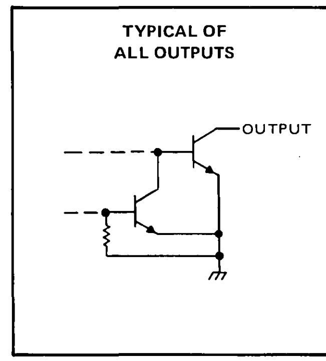
'88A, '187



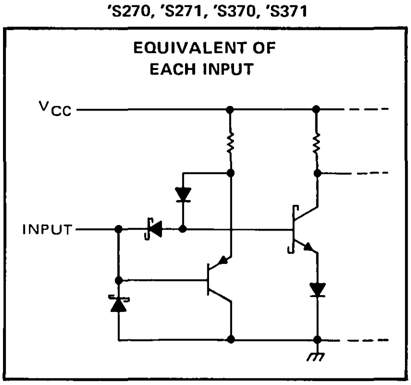
'88A



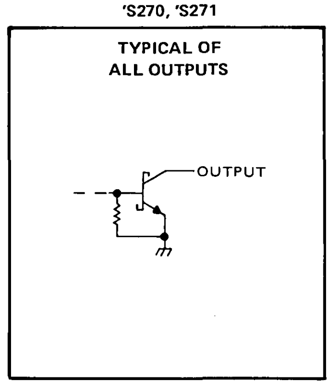
'187



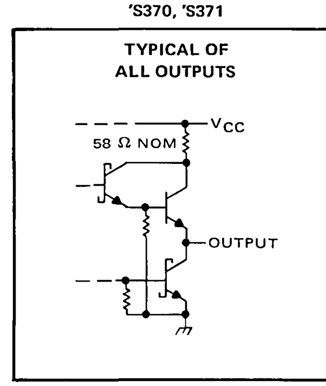
'S270, 'S271, 'S370, 'S371



'S270, 'S271



'S370, 'S371



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)		7 V
Input voltage		5.5 V
Off-state output voltage		5.5 V
Operating free-air temperature range:	SN54', SN54S' Circuits (see Note 2)	−55°C to 125°C
	SN74', SN74S' Circuits	0°C to 70°C
Storage temperature range		−65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. An SN54187 in the W package operating at free-air temperatures above 111°C requires a heat sink that provides a thermal resistance from case-to-free-air, $R_{\theta CA}$, of not more than 46°C/W.

recommended operating conditions

	SN5488A			SN7488A			SN54187			SN74187			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5			5.5			5.5	V
Low-level output current, I_{OL}			12			12			16			16	mA
Operating free-air temperature, T_A (see Note 2)	−55		125	0		70	−55		125	0		70	°C

NOTE 2: An SN54187 in the W package operating at free-air temperatures above 111°C requires a heat sink that provides a thermal resistance from case-to-free-air, $R_{\theta CA}$, of not more than 46°C/W.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		'88A			'187			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA			−1.5			−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, V_{OH} = 5.5 V			40			40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	I_{OL} = 12 mA		0.2	0.4			0.4	V
			I_{OL} = 16 mA						0.45	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			25			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−1			−1	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 3		64	80		92	130	mA
C_o	Off-state output capacitance	V_{CC} = 5 V, f = 1 MHz	V_O = 5 V,		6.5			6.5		pF

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 3: With outputs open and $\overline{CS}$ input(s) grounded, I_{CC} is measured first by selecting a word that contains the maximum number of programmed high-level outputs, then by selecting a word that contains the maximumnumber of programmed low-level outputs.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	'88A		'187		UNIT
			TYP	MAX	TYP	MAX	
$t_{a(ad)}$	Access time from address	C_L = 30 pF,	26	45	40	60	ns
$t_{a(\overline{CS})}$	Access time from chip select (enable time)	R_{L1} = 400 Ω ('88A) 300 Ω ('187)	22	35	20	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from chip select (disable time)	R_{L2} = 600 Ω, See Figure 1	22	35	20	30	ns

4

575

recommended operating conditions

	SN54S270 SN54S271			SN74S270 SN74S271			SN54S370 SN54S371			SN74S370 SN74S371			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5							V
High-level output current, I_{OH}									−2			−6.5	mA
Low-level output current, I_{OL}			16			16			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		'S270, 'S271			'S370, 'S371			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = MAX				2.4			V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	V_{OH} = 2.4 V			50				µA
			V_{OH} = 5.5 V			100				µA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = MAX			0.5			0.5	V
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_O = 2.4 V	V_{IH} = 2 V,						50	µA
I_{OZL}	Off-state output current low-level voltage applied	V_{CC} = MAX, V_O = 0.5 V	V_{IH} = 2 V,						−50	µA
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V			25			25	µA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.5 V			−0.25			−0.25	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX					−30		−100	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 4		105	155		105	155	mA
C_o	Off-state output capacitance	V_{CC} = 5 V, f = 1 MHz	V_O = 5 V,		6.5			6.5		pF

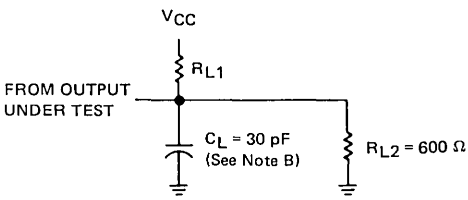
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
NOTE 4: With outputs open and $\overline{CS}$ input(s) grounded, I_{CC} is measured first by selecting a word that contains the maximum number of programmed high-level outputs; then by selecting a word that contains the maximum number of programmed low-level outputs.

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

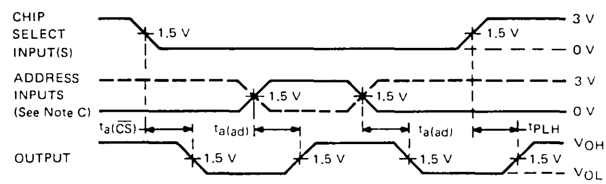
PARAMETER		TEST CONDITIONS	SN54270 SN54271		SN74270 SN74271		SN54370 SN54370		SN74370 SN74370		UNIT
			TYP‡	MAX	TYP‡	MAX	TYP‡	MAX	TYP‡	MAX	
$t_{a(ad)}$	Access time from address	R_{L2} = 600 Ω, See Figure 1	45	95	45	70					ns
$t_{a(\overline{CS})}$	Access time from chip select (enable time)		15	45	15	30					ns
t_{PLH}	Propagation delay time, low-to-high-level output from chip select (disable time)		15	40	15	25					ns
$t_{a(ad)}$	Access time from address	C_L = 30 pF, See Figure 2					45	95	45	70	ns
$t_{a(\overline{CS})}$	Access time from chip select (enable time)						15	45	15	30	ns
t_{PXZ}	Disable time from high or low level	C_L = 5 pF, See Figure 2					10	40	10	25	ns

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

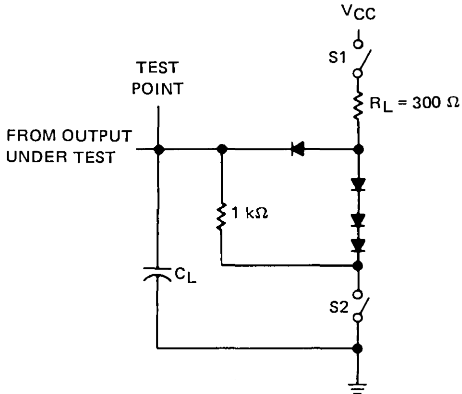


VOLTAGE WAVEFORMS

NOTES: A. The input pulse generator has the following characteristics: PRR ⩽ 1 MHz, Z_{out} ≈ 50 Ω. For Series 54/74, t_r ⩽ 7 ns, t_f ⩽ 7 ns, for Series 54S/74S, t_r ⩽ 2.5 ns, t_f ⩽ 2.5 ns.
B. C_L includes probe and jig capacitance.
C. The pulse generator is connected to the input under test. The other inputs, memory content permitting, are connected so that the input will switch the output under test.

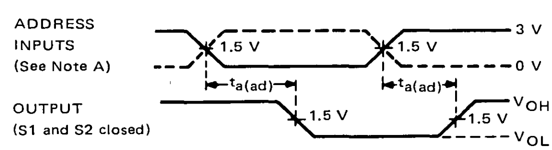
FIGURE 1—SWITCHING TIMES OF '88A, '187, 'S270, AND 'S271 (OPEN-COLLECTOR OUTPUTS)

4

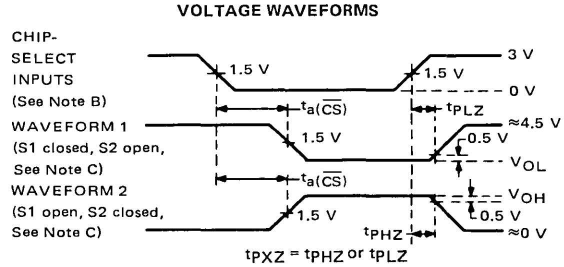


C_L includes probe and jig capacitance.
All diodes are 1N3064.

LOAD CIRCUIT



ACCESS TIME FROM ADDRESS INPUTS VOLTAGE WAVEFORMS



ACCESS (ENABLE) TIME AND DISABLE TIME FROM CHIP SELECT VOLTAGE WAVEFORMS

NOTES: A. When measuring access times from address inputs, the chip-select input(s) is(are) low.
B. When measuring access and disable times from chip-select input(s) the address inputs are steady-state.
C. Waveform 1 is for the output with internal conditions such that the output is low except when disabled. Waveform 2 is for the output with internal conditions such that the output is high except when disabled.
D. Input waveforms are supplied by pulse generators having the following characteristics: t_r ⩽ 2.5 ns, t_f ⩽ 2.5 ns, PRR ⩽ 1 MHz, and Z_{out} ≈ 50 Ω.

FIGURE 2—SWITCHING TIMES OF 'S370 AND 'S371 (3-STATE OUTPUTS)

ORDERING INSTRUCTIONS

Programming instructions for these read-only memories are solicited in the form of a sequenced deck of standard 80-column data cards providing the information requested under "data card format," accompanied by a properly sequenced listing of these cards, and the supplementary ordering data. Upon receipt of these items, a computer run will be made from the deck of cards which will produce a complete function table for the requested part. This function table, showing output conditions for each of the words, will be forwarded to the purchaser as verification of the input data as interpreted by the computer-automated design (CAD) program. This single run also generates mask and test program data; therefore, verification of the function table should be completed promptly.

Each card in the data deck prepared by the purchaser identifies the words specified and describes the levels at the outputs for each of those words. All addresses must have all outputs defined and columns designated as "blank" must not be punched. Cards should be punched according to the data card format shown.

SUPPLEMENTARY ORDERING DATA

Submit the following information with the data cards:

a) Customer's name and address
b) Customer's purchase order number
c) Customer's drawing number.

The following information will be furnished to the customer by Texas Instruments:

a) TI part number
b) TI sales order number
c) Date received.

'88A DATA CARD FORMAT (32 CARDS)

Column	
1-2	Punch a right-justified integer representing the positive-logic binary input address (00-31) for the word described on the card.
3-4	Blank
5	Punch "H" or "L" for output Y8. H = high-voltage-level output, L = low-voltage-level output
6-9	Blank
10	Punch "H" or "L" for output DO 7.
11-14	Blank
15	Punch "H" or "L" for output DO 6.
16-19	Blank
20	Punch "H" or "L" for output DO 5.
21-24	Blank
25	Punch "H" or "L" for output DO 4.
26-29	Blank
30	Punch "H" or "L" for output DO 3.
31-34	Blank
35	Punch "H" or "L" for output DO 2.
36-39	Blank
40	Punch "H" or "L" for output DO 1.
41-49	Blank
50-51	Punch a right-justified integer representing the current calendar day of the month.
52	Blank
53-55	Punch an alphabetic abbreviation representing the current month.
56	Blank
57-58	Punch the last two digits of the current year.
59	Blank
60-61	Punch "SN"
62-66	Punch a left-justified integer representing the Texas Instruments part number. This is supplied by the factory through a TI sales representative.
67-68	Blank
69-80	Preferably these columns should be punched to reflect the customer's part or specification-control number. This information is not essential.

'187 DATA CARD FORMAT (32 CARDS)

Column	
1- 3	Punch a right-justified integer representing the binary input address (000-248) for the first set of outputs described on the card.
4	Punch a "–" (Minus sign)
5- 7	Punch a right-justified integer representing the binary input address (007-255) for the last set of outputs described on the card.
8- 9	Blank

4

575

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

ORDERING INSTRUCTIONS

10-13	Punch "H", "L", or "X" for bits four, three, two, and one (outputs DO 4, DO 3, DO 2 and DO 1 in that order) for the first set of outputs specified on the card. H = high-voltage-level output, L = low-voltage-level output, X = output level irrelevant.
14	Blank
15-18	Punch "H", "L", or "X" for the second set of outputs.
19	Blank
20-23	Punch "H", "L", or "X" for the third set of outputs.
24	Blank
25-28	Punch "H" "L", or "X" for the fourth set of outputs.
29	Blank
30-33	Punch "H", "L", or "X" for the fifth set of outputs.
34	Blank
35-38	Punch "H", "L", or "X" for the sixth set of outputs.
39	Blank
40-43	Punch "H", "L", or "X" for the seventh set of outputs.
44	Blank
45-48	Punch "H", "L", or "X" for the eighth set of outputs.
49	Blank
50-51	Punch a right-justified integer representing the current calendar day of the month.
52	Blank
53-55	Punch an alphabetic abbreviation representing the current month.
56	Blank
57-58	Punch the last two digits of the current year.
59	Blank
60-61	Punch "SN"
62-66	Punch a left-justified integer representing the Texas Instruments part number. This is supplied by the factory through a TI sales representative.
67-68	Blank
69-80	Preferably these columns should be punched to reflect the customer's part or specification-control number. This information is not essential.

'S270, 'S370 DATA CARD FORMAT (64 CARDS)

Column	
1-3	Punch a right-justified integer representing the binary input address (000-504) for the first set of outputs described on the card.
4	Punch a "—" (Minus sign)
5-7	Punch a right-justified integer representing the binary input address (007-511) for the last set of outputs described on the card.
8-80	Same as the '187 data card format.

'S271, 'S371 DATA CARD FORMAT (64 CARDS)

Column	
1- 3	Punch a right-justified integer representing the binary input address (000-252) for the first set of outputs described on the card.
4	Punch a "—" (Minus sign)
5- 7	Punch a right-justified integer representing the binary input address (003-255) for the last set of outputs described on the card.
8- 9	Blank
10-17	Punch "H", "L", or "X" for bits eight, seven, six, five, four, three, two, and one (outputs DO 8, DO 7, DO 6, DO 5, DO 4, DO 3, DO 2, and DO 1 in that order) for the first set of outputs specified on the card. H = high-voltage-level output, L = low-voltage-level output, X = output level irrelevant.
18	Blank
19-26	Punch "H", "L", or "X" for the second set of outputs.
27	Blank
28-35	Punch "H", "L", or "X" for the third set of outputs.
36	Blank
37-44	Punch "H", "L", or "X" for the fourth set of outputs.
45-49	Blank
50-80	Same as the '187 data card format.

4

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TTL MEMORIES MECHANICAL DATA

general

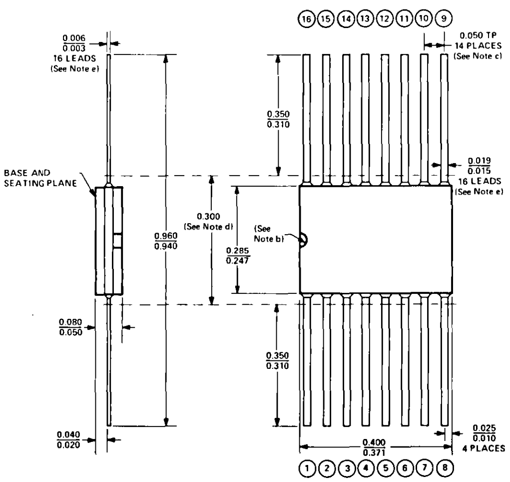
The availability of a particular TTL memory in a particular package is denoted by an alphabetical reference in a table on the data sheet for that type of memory, or above the pin-connection diagram. These letters refer to mechanical outline drawings shown in this section. Orders for these memories should include the package outline letter at the end of the circuit type number; e.g., SN54S287W, SN74S470J

W ceramic flat packages

These hermetically sealed flat packages consist of an electrically nonconductive ceramic base and cap, and a 16- or 24-lead frame. Hermetic sealing is accomplished with glass. Tin-plated ("bright-dipped") leads (—00) require no additional cleaning or processing when used in soldered assembly.

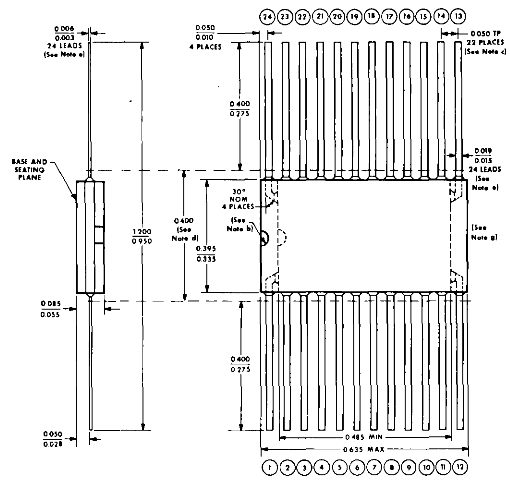
4

16-PIN W CERAMIC



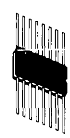
Falls Within
JEDEC MO-004AG Dimensions

24-PIN W CERAMIC

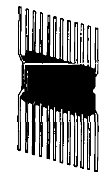


Falls Within
JEDEC MO-019AA Dimensions

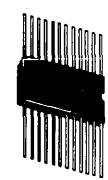
NOTES: a. All dimensions are in inches.
b. Index point is provided on cap for terminal identification only.
c. Leads are within 0.005 radius of true position (TP) at maximum material condition.
d. This dimension determines a zone within which all body and lead irregularities lie.
e. Not applicable for solder-dipped leads.
f. When solder-dipped leads are specified, dipped area extends from lead tip to within 0.050 of package body.
g. End configuration of 24-pin package is at the option of TI.



16 PIN



24 PIN



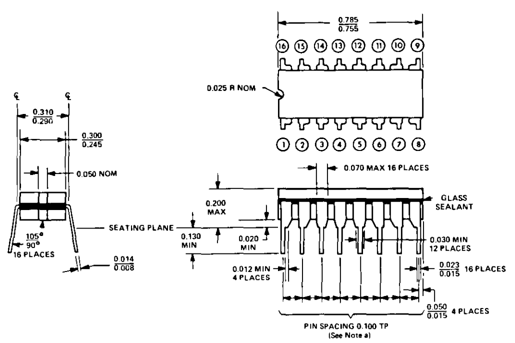
24 PIN

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

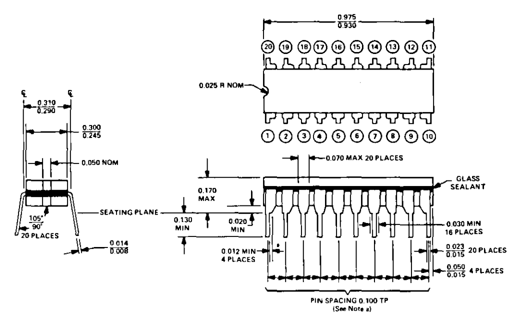
J ceramic dual-in-line packages

These hermetically sealed dual-in-line packages consist of a ceramic base, ceramic cap, and a 16-, 20-, or 24-lead frame. The packages are intended for insertion in mounting-hole rows on 0.300-inch or 0.600-inch centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads (—00) require no additional cleaning or processing when used in soldered assembly.

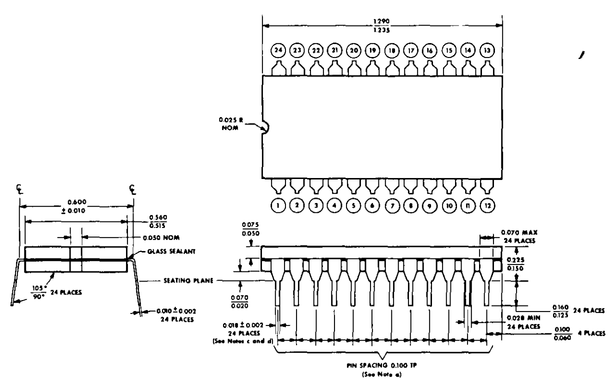
16-PIN J CERAMIC



20-PIN J CERAMIC

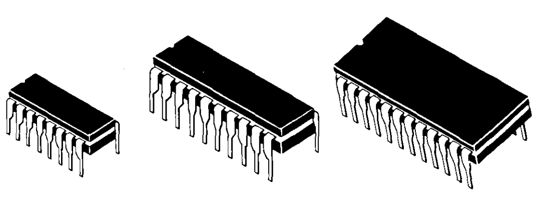


24-PIN J CERAMIC



Falls Within
JEDEC MO-015AA Dimensions

NOTES: a. Each pin centerline is located within 0.010 of its true longitudinal position.
b. All dimensions are in inches unless otherwise noted.



16-PIN 20-PIN 24-PIN

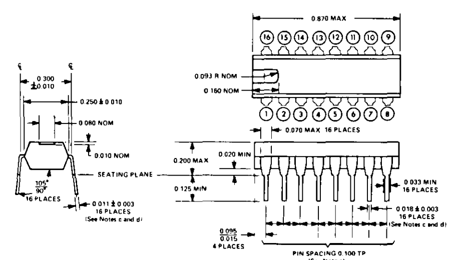
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TTL MEMORIES MECHANICAL DATA

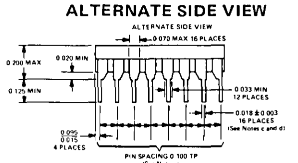
N plastic dual-in-line packages

These dual-in-line packages consist of a circuit mounted on a 16-, 20-, or 24-lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. These packages are intended for insertion in mounting-hole rows on 0.300-inch or 0.600-inch centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

16-PIN N PLASTIC

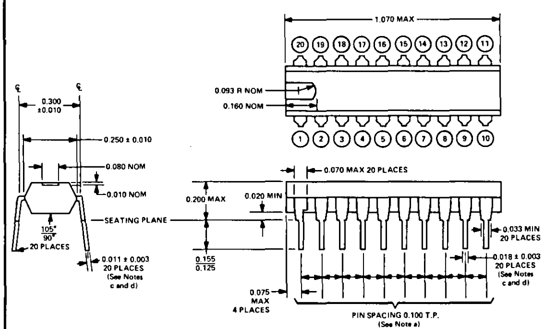


ALTERNATE SIDE VIEW

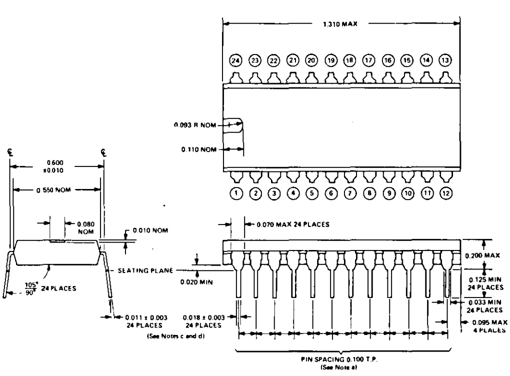


Package configuration of 16-pin N package (see alternative sideviews) is at the option of TI.

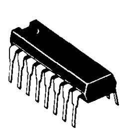
20-PIN N PLASTIC



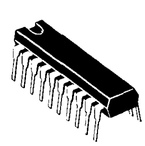
24-PIN N PLASTIC



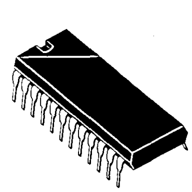
NOTES:
- a. Each pin centerline is located within 0.010 of its true longitudinal position.
- b. All dimensions are in inches unless otherwise noted.
- c. This dimension does not apply for solder-dipped leads.
- d. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0.020 above the seating plane.



16-PIN



20-PIN



24-PIN

4

575

ECL
Memories

5

SERIES SN10000 MEMORIES

BULLETIN NO. DL-S 7512255, MAY 1975

- **Full On-Chip Address Decoding and Output-Sense Amplification**
- **Constant Current Drain Over a Wide Supply Voltage Range**
- **Logic Levels Compatible with Series SN10000 Logic Levels**
- **Compatible for Wired-OR Word Expansion**

5

absolute maximum ratings over operating ambient temperature range† (unless otherwise noted)

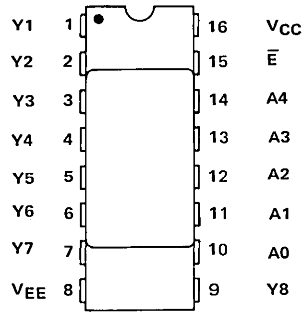
Supply voltage V_{EE} (see Note 1)	−7 V
Input voltage range	0 V to V_{EE}
Output current	−50 mA
Operating ambient temperature range	0°C to 85°C
Storage temperature range	−55°C to 125°C
Lead temperature 1/16 inch from case for 10 seconds	300°C

NOTE 1: Unless otherwise noted all voltage values are with respect to the V_{CC} terminals and all V_{CC} terminals must be connected in parallel.

†The ambient temperature conditions assume air moving perpendicular to the longitudinal axis and parallel to the seating plane of the device at a velocity of 500 feet per minute with the device under test soldered to a 4 x 6 x 0.062-inch double-sided 2-oz copper-clad circuit board.

- 32-Word-by-Eight-Bit Organization
- Full On-Chip Address Decoding and Output-Sensing Amplification
- Capability for Wired-OR Connections
- Easy Programming

J OR JE
DUAL-IN-LINE PACKAGE (TOP VIEW)

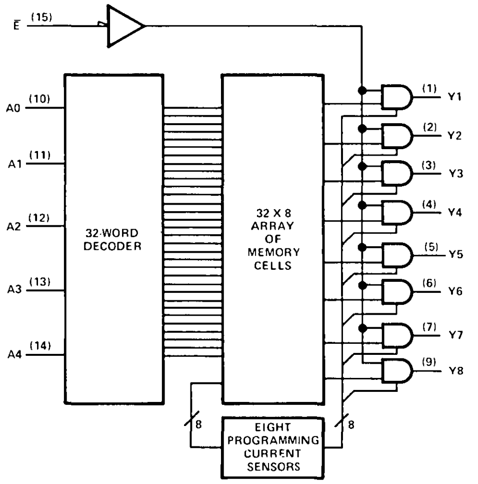


description

The SN10139 is a field-programmable, 256-bit read-only memory organized as 32 words of eight bits each. Full address decoding and output sense amplification are included on the chip. Each of the 32 words is addressed by the binary address inputs A0 through A4. The outputs Y1 through Y8 can be connected to other emitter-follower outputs to achieve wired-OR word expansion. An enable input, Ē, is provided for ease in expansion. The device is enabled when the enable input is low. When the enable input is high, all outputs are forced low.

Data can be electronically programmed, as desired, at any of the 256 bit locations in accordance with the programming procedure specified. Prior to programming, the memory contains a low-logic-level output condition at all bit locations. The programming procedure open-circuits metal links, which results in a high-logic-level output at the selected locations. The procedure is irreversible; once altered, the output for that bit is permanently programmed to provide a high logic level. Outputs never having been altered may later be programmed to supply a high-level output. Operation of the device within the recommended operating conditions will not alter the memory content.

functional block diagram



5

recommended operating conditions

	B	NOM	A (SEE NOTE 3)	UNIT
Supply voltage, V_{EE}	−5.72	−5.2	−4.68	V
Operating ambient temperature, T_A	0		85	°C

electrical characteristics at specified ambient temperature†

PARAMETER		TEST CONDITIONS (SEE NOTES 1 AND 2)		B	TYP	A (SEE NOTE 3)	UNIT
V_{IH}	High-level input voltage		0°C	−1020		−840	mV
			25°C	−980		−810	
			85°C	−910		−700	
V_{IH}'	High-level input voltage		0°C	−1145			mV
			25°C	−1105			
			85°C	−1035			
V_{IL}	Low-level input voltage		0°C	V_{EE}		−1645	mV
			25°C	V_{EE}		−1630	
			85°C	V_{EE}		−1595	
V_{IL}'	Low-level input voltage		0°C			−1490	mV
			25°C			−1475	
			85°C			−1440	
V_{OH}	High-level output voltage	$V_{IH} = V_{IHB}$, $V_{IL} = V_{ILA}$	0°C	−1000		−840	mV
			25°C	−960		−810	
			85°C	−890		−700	
V_{OL}	Low-level output voltage	$V_{IH} = V_{IHB}$, $V_{IL} = V_{ILA}$	0°C	−1870		−1665	mV
			25°C	−1850		−1650	
			85°C	−1825		−1615	
V_{OH}'	High-level output voltage	$V_{IH} = V_{IH'B}$, $V_{IL} = V_{IL'A}$	0°C	−1020		−840	mV
			25°C	−980		−810	
			85°C	−910		−700	
V_{OL}'	Low-level output voltage	$V_{IH} = V_{IH'B}$, $V_{IL} = V_{IL'A}$	0°C	−1870		−1645	mV
			25°C	−1850		−1630	
			85°C	−1825		−1595	
I_{IH}	High-level input current	V_I = −810 mV, Other inputs open	25°C			265	µA
I_{IL}	Low-level input current	V_I = −1850 mV, Other inputs open	25°C	0.5			µA
I_{EE}	Supply current	All inputs and outputs open	25°C	−145	−107		mA
		All inputs at −810 mV, All outputs open	25°C	−145	−110		mA

switching characteristics at 25°C free-air temperature

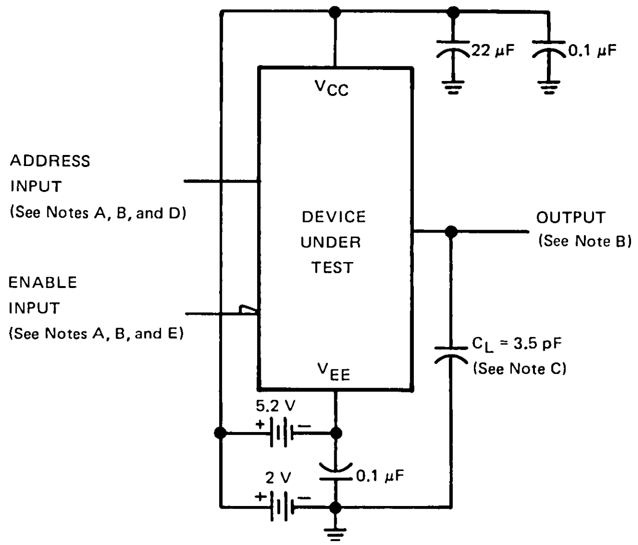
PARAMETER		TEST CONDITIONS	B	A (SEE NOTE 3)	UNIT
$t_{a(ad)}$	Access time from address	C_L = 3.5 pF, R_L = 50 Ω, See Figures 1 and 2		20	ns
t_{PLH}	Propagation delay time, low-to-high-level output from $\overline{E}$ (enable time)			15	ns
t_{PHL}	Propagation delay time, high-to-low-level output from $\overline{E}$ (disable time)			15	ns

NOTES: 1. All parameters are measured with V_{EE} = −5.200 V, V_{CC} = 0 V, and (unless otherwise noted) the output is connected to −2.000 V through 50 Ω.
2. Test conditions stating $V_{IH} = V_{IHB}$ (or $V_{IH'B}$) and/or $V_{IL} = V_{ILA}$ (or $V_{IL'A}$) mean that the high-level input voltages are equal to the B limit of V_{IH} (or V_{IH}') specified for the particular temperature (see note 3) and/or the low-level input voltages are equal to the appropriate A limit of V_{IL} (or V_{IL}'). The output voltage limits are guaranteed for any appropriate combination of input conditions for the desired output.
3. This data sheet uses the algebraic-limit system that has been adopted by the International Electrotechnical Commission. The A limit is the more positive (less negative) limit; the B limit is the less positive (more negative) limit.

†The ambient temperature conditions assume air moving perpendicular to the longitudinal axis and parallel to the seating plane of the device at a velocity of 500 feet per minute with the device under test soldered to a 4 x 6 x 0.062-inch double-sided 2-oz copper-clad circuit board.

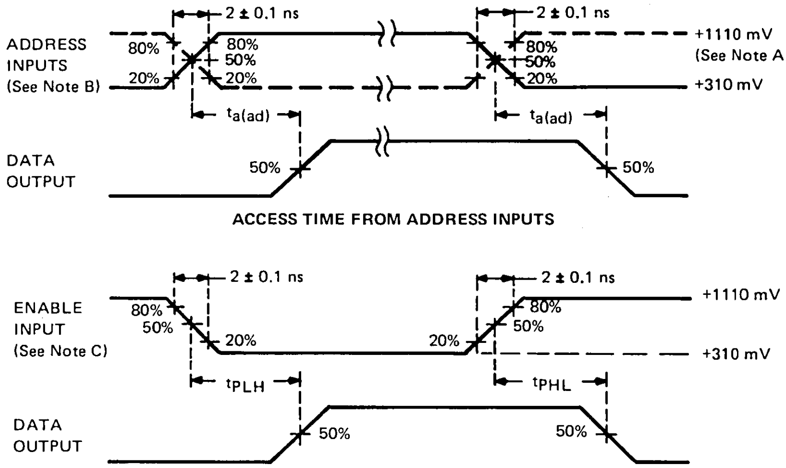
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input waveforms are supplied by generators having the following characteristics: Z_{out} = 50 Ω, PRR = 2 MHz. Transition times of input waveforms are 2 ± 0.1 ns between the 20% and 80% levels and are determined with no device in the socket.
B. The waveforms are monitored on an oscilloscope having the following characteristics: $t_r \leqslant$ 0.35 ns, R_{in} = 50 Ω. Input and output cables are equal lengths of 50-Ω coaxial cable.
C. C_L includes jig capacitance.
D. All address lines not under test must be biased to select a memory cell.
E. If the enable line is not under test, it must be at a low logic level.

FIGURE 1—TEST CIRCUIT



ENABLE AND DISABLE TIMES

NOTES: A. Voltage values on input waveforms are with respect to ground.
B. The enable input is low.
C. The bit location addressed contains high-level data.

FIGURE 2—VOLTAGE WAVEFORMS

5

step-by-step programming procedure

manual

1. Connect V_{EE} (Pin 8) to ground and V_{CC} (Pin 16) to 5.2 V. See Figure 3. Address the word to be programmed by applying to the appropriate address inputs 4 to 4.6 V for a high level and 0 to 1 V for a low level.
2. Raise V_{CC} (Pin 16) to 12 V. This level must not be maintained longer than 1 second. Maximum supply current during programming is 250 mA.
3. After V_{CC} has stabilized at 12 V (including any ringing that may be present on the V_{CC} line), apply a current pulse of 2.5 mA to the output corresponding to the bit to be programmed to a high.
4. Return V_{CC} to 5.2 V.
   CAUTION: To prevent excessive chip temperature rise, V_{CC} should not be allowed to remain at 12 V for more than 1 second.
5. Verify that the selected bit has programmed by connecting a 460-Ω resistor to ground and measuring the voltage at the output. If a high level ($V_O \geqslant 4.2$ V) is not detected at the output, the programming procedure should be repeated once.
6. If verification is positive, proceed to next bit to be programmed.

automatic

1. Connect V_{EE} (Pin 8) to ground and V_{CC} (Pin 16) to 5.2 V. See Figure 3. Address the word to be programmed by applying to the appropriate address inputs 4 to 4.6 V for a high level and 0 to 1 V for a low level.
2. Raise V_{CC} (Pin 16) to 12 V. This level must not be maintained longer than 1 second. Maximum supply current during programming is 250 mA.
3. After a delay of 100 μs minimum, 1 ms maximum, apply a 2.5-mA current pulse to the output corresponding to the first bit to be programmed to a high. This output pulse is maintained between 0.5 and 1 ms. See Figure 4.
4. Repeat step 3 for each bit of the selected word specified as a high. (Program only one bit at a time; the delay between output programming pulses should not be greater than 1 ms.)
5. After all the desired bits of the selected word have been programmed, change address data and repeat the preceeding two paragraphs.
   NOTE: If all the maximum times listed above are maintained, the entire memory will program in less than 1 second. Therefore, it would be permissable for V_{CC} to remain at 12 V during the entire programming time.
6. After stepping through all address words, return V_{CC} to 5.2 V and verify that each bit has programmed. If one or more bits have not programmed, repeat the entire programming procedure once.

recommended conditions for programming

		B (SEE NOTE 3)	NOM	A	UNIT
Supply voltage, V_{CC}	To program	11.5	12	12.5	V
	To verify	5	5.2	5.4	
Input voltage	High level	4		4.6	V
	Low level	0		1	
Output current during programming		2	2.5	3	mA
Programming pulse width, $t_{w(p)}$ (See Note 4)		0.5		1	ms
Programming pulse rise time				10	μs
Programming pulse delay (See Note 4)	Following V_{CC} change, $t_{d(1)}$	0.1		1	ms
	Between output pulses, $t_{d(2)}$	0.01		1	

NOTES: 3. This data sheet uses the algebraic-limit system that has been adopted by the International Electrotechnical Commission. The A limit is the more positive (less negative) limit; the B limit is the less positive (more negative) limit.
4. These maximum times are specified to minimize the amount of time V_{CC} is at 12 V.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PROGRAMMING INFORMATION

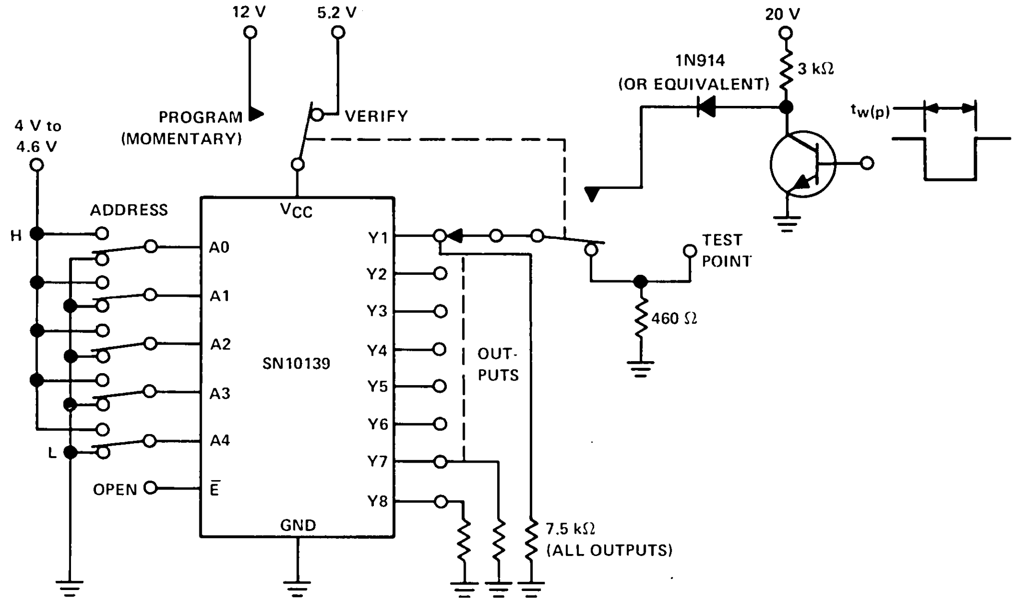


FIGURE 3—PROGRAMMING CIRCUIT

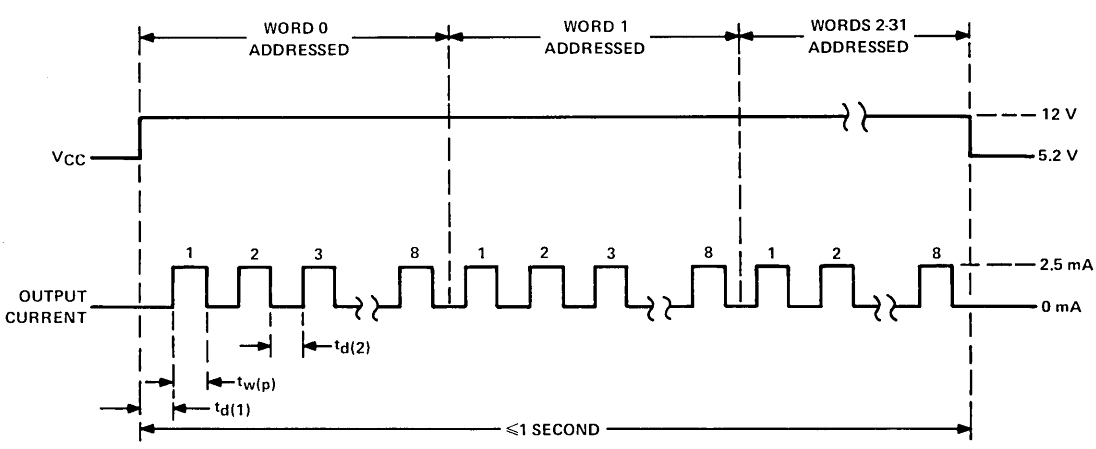


FIGURE 4—TIMING DIAGRAM FOR AUTOMATIC PROGRAMMING

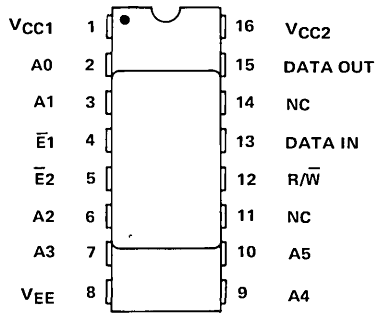
5

TYPES SN10140, SN10142, SN10148
64-BIT RANDOM-ACCESS MEMORIES

MAY 1975

- SN10140 Drives 90-Ohm Loads
- SN10142 and SN10148 Drive 50-Ohm Loads
- Fast Access Times:
  10 ns Max (SN10142)
  15 ns Max (SN10140, SN10148)
- 64-Word-by-One-Bit Organization
- Full On-Chip Address Decoding and Output-Sense Amplification
- Capability for Wired-OR Connections
- Low Sensitivity to Supply Voltage Variation

J OR JE
DUAL-IN-LINE PACKAGE (TOP VIEW)



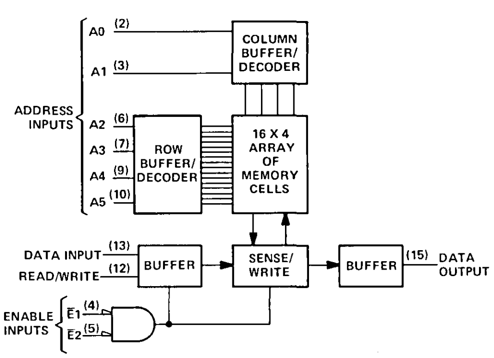
description

These 64-bit active-element memories are monolithic, high-speed, emitter-coupled-logic (ECL) arrays of 64 storage cells organized to provide 64 words of one bit each. Full address decoding and output sense amplification are included on the chip. An additional level of decoding is provided for memory systems by the two enable inputs. Each of the 64 words is addressed by the binary address inputs A0 through A5. The output can be connected to other emitter-follower outputs to achieve wired-OR word expansion. The SN10140, SN10142, and SN10148 are fully compatible with the SN10000 logic family. The SN10148 and SN10142 are specified to meet SN10000 levels when driving 50-ohm loads and the SN10140 is specified to drive a 90-ohm load.

Information at the data input is written into the memory by addressing the desired word with the address lines and taking the read/write input low while both enable inputs are held low. The output is forced low while the memory is in the write mode.

Information stored in the memory is read out by holding the read/write line high, selecting the desired address, and taking both enable inputs low.

functional block diagram



FUNCTION TABLE

READ/WRITE	ENABLE Ē1	ENABLE Ē2	OPERATION
L	L	L	Write (output low)
H	L	L	Read
X	H	X	Chip disabled (output low)
X	X	H	Chip disabled (output low)

H = high level, L = low level, X = irrelevant

5

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

recommended operating conditions

		B (SEE NOTE 3)	NOM (SEE NOTE 3)	A (SEE NOTE 3)	UNIT
Supply voltage, V_{EE}		−5.72	−5.2	−4.68	V
Width of write pulse, $t_{w(wr)}$ (see Figure 9)		10			ns
Setup time, t_{su} (see Figure 9)	Address before write pulse	5			ns
	Enable before write pulse	3			
	Data before end of write pulse	10			
Hold time, t_h (see Figure 9)	Address after write pulse	3			ns
	Enable after write pulse	0			
	Data after write pulse	3			
Operating ambient temperature, T_A		0		85	°C

electrical characteristics at specified ambient temperature†

PARAMETER			TEST CONDITIONS (SEE NOTES 1 AND 2)		B (SEE NOTE 3)	TYP (SEE NOTE 3)	A (SEE NOTE 3)	UNIT
V_{IH}	High-level input voltage			0°C	−1020		−840	mV
				25°C	−980		−810	
				85°C	−910		−700	
$V_{IH'}$	High-level input voltage			0°C	−1145			mV
				25°C	−1105			
				85°C	−1035			
V_{IL}	Low-level input voltage			0°C	V_{EE}		−1645	mV
				25°C	V_{EE}		−1630	
				85°C	V_{EE}		−1595	
$V_{IL'}$	Low-level input voltage			0°C			−1490	mV
				25°C			−1475	
				85°C			−1440	
V_{OH}	High-level output voltage		$V_{IH} = V_{IHB}$, $V_{IL} = V_{ILA}$	0°C	−1000		−840	mV
				25°C	−960		−810	
				85°C	−890		−700	
V_{OL}	Low-level output voltage		$V_{IH} = V_{IHB}$, $V_{IL} = V_{ILA}$	0°C	−2000		−1665	mV
				25°C	−1990		−1650	
				85°C	−1920		−1615	
$V_{OH'}$	High-level output voltage		$V_{IH} = V_{IH'B}$, $V_{IL} = V_{IL'A}$	0°C	−1020		−840	mV
				25°C	−980		−810	
				85°C	−910		−700	
$V_{OL'}$	Low-level output voltage		$V_{IH} = V_{IH'B}$, $V_{IL} = V_{IL'A}$	0°C	−2000		−1645	mV
				25°C	−1990		−1630	
				85°C	−1920		−1595	
I_{IH}	High-level input current	Read/Write	$V_I = -810$ mV, Other inputs open	25°C			355	µA
		Other inputs					265	
I_{IL}	Low-level input current		$V_I = -1990$ mV, Other inputs open	25°C	0.5			µA
I_{EE}	Supply current		All inputs and the output open	25°C	−103	−85		mA

NOTES: 1. All parameters are measured with $V_{EE} = -5.200$ V, $V_{CC1} = V_{CC2} = 0$ V, and (unless otherwise noted) the output is connected to −2.000 V through 50 Ω for SN10142 and SN10148, or 90 Ω for SN10140.

2. Test conditions stating $V_{IH} = V_{IHB}$ (or $V_{IH'B}$) and/or $V_{IL} = V_{ILA}$ (or $V_{IL'A}$) mean that the high-level input voltages are equal to the B limit of V_{IH} (or $V_{IH'}$) specified for the particular temperature (see note 3) and/or the low-level input voltages are equal to the appropriate A limit of V_{IL} (or $V_{IL'}$). The output voltage limits are guaranteed for any appropriate combination of input conditions specified by the function table for the desired output.

3. This data sheet uses the algebraic-limit system that has been adopted by the International Electrotechnical Commission. The A limit is the more positive (less negative) limit; the B limit is the less positive (more negative) limit.

†The ambient temperature conditions assume air moving perpendicular to the longitudinal axis and parallel to the seating plane of the device at a velocity of 500 feet per minute with the device under test soldered to a 4 x 6 x 0.062-inch double-sided 2-oz copper-clad circuit board.

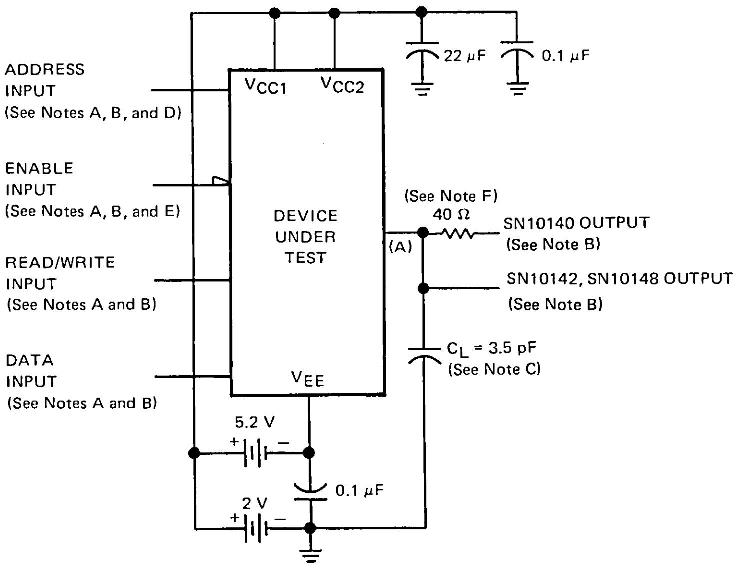
5

switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	SN10140 SN10148 B	SN10140 SN10148 TYP	SN10140 SN10148 A	SN10142 B	SN10142 TYP	SN10142 A	UNIT
			(SEE NOTE 3)			(SEE NOTE 3)			
$t_{a(ad)}$	Access time from address	C_L = 3.5 pF, R_L = 90 Ω (SN10140) 50 Ω (SN10142, SN10148), See Figures 5 and 9		10	15		8	10	ns
t_{PLH}	Propagation delay time, low-to-high-level output from $\overline{E}$ (enable time)			7	12		7	12	ns
t_{PHL}	Propagation delay time, high-to-low-level output from $\overline{E}$ (disable time)			7	12		7	12	ns
t_{TLH}	Transition time, low-to-high-level output (20% to 80%)				2.5			2.5	ns
t_{THL}	Transition time, high-to-low-level output (80% to 20%)				2.5			2.5	ns
t_{SR}	Sense recovery time				10			10	ns

NOTE 3: This data sheet uses the algebraic-limit system that has been adopted by the International Electrotechnical Commission. The A limit is the more positive (less neagtive) limit; the B limit is the less positive (more negative) limit.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input waveforms are supplied by generators having the following characteristics: Z_{out} = 50 Ω, PRR = 2 MHz. Transition times of input waveforms are 2 ± 0.1 ns between the 20% and 80% levels and are determined with no device in the socket.

B. The waveforms are monitored on an oscilloscope having the following characteristics: $t_r \leqslant 0.35$ ns, R_{in} = 50 Ω. Input and output cables are equal lengths of 50-Ω coaxial cable.

C. C_L includes jig capacitance.

D. All address lines not under test must be biased to select a memory cell.

E. Enable line(s) not under test must be at a low logic level.

F. 40-Ω external resistor shown is used for SN10140 only. When testing SN10142 or SN10148, connect point (A) directly to 50-Ω output cable.

FIGURE 5—TEST CIRCUIT

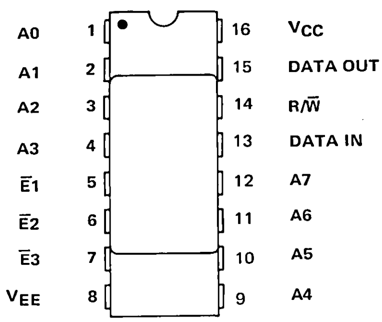
5

TYPE SN10144
256-BIT RANDOM-ACCESS MEMORY

MAY 1975

- Fast Access Time . . . 18 ns Typical
- 256-Word-by-One-Bit Organization
- Drives 50-Ohm Loads
- Full On-Chip Address Decoding and Output-Sense Amplification
- Capability for Wired-OR Connections
- Low Sensitivity to Supply Voltage Variation

J OR JE
DUAL-IN-LINE PACKAGE (TOP VIEW)



description

This 256-bit active-element memory is a monolithic high-speed, emitter-coupled-logic (ECL) array of 256 storage cells organized to provide 256 words of one bit each. Full address decoding and output sense amplification are included on the chip. An additional level of decoding is provided for memory systems by the three enable inputs. Each of the 256 words is addressed by the binary address inputs A0 through A7. The output can be connected to other emitter-follower outputs to achieve wired-OR word expansion.

Information at the data input is written into the memory by addressing the desired word with the address lines and taking the read/write input low while all enable inputs are held low. The output is forced low while the memory is in the write mode.

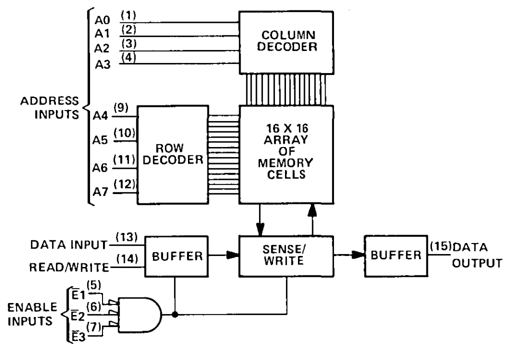
Information stored in the memory is read out by holding the read/write line high, selecting the desired address, and taking all enable inputs low.

FUNCTION TABLE

READ/ WRITE	ENABLE Ē1	Ē2	Ē3	OPERATION
L	L	L	L	Write (output low)
H	L	L	L	Read
X	H	X	X	Chip disabled (output low)
X	X	H	X	Chip disabled (output low)
X	X	X	H	Chip disabled (output low)

H = high level, L = low level, X = irrelevant

functional block diagram



recommended operating conditions

		B	NOM	A	UNIT
		(SEE NOTE 3)			
Supply voltage, V_{EE}		−5.72	−5.2	−4.68	V
Width of write pulse, $t_{w(wr)}$ (see Figure 9)		25			ns
Setup time, t_{su} (see Figure 9)	Address before write pulse	8			ns
	Enable before write pulse	2			
	Data before end of write pulse	27†			
Hold time, t_h (see Figure 9)	Address after write pulse	2			ns
	Enable after write pulse	2			
	Data after write pulse	2			
Operating ambient temperature, T_A		0		85	°C

†Note that this setup time is referenced to the end of the write pulse. With a minimum-width (25-ns) write pulse, this limit is equivalent to a 2-ns setup time referenced to the start of the write pulse. The setup-time requirement is thus made independent of write pulse width.

electrical characteristics at specified ambient temperature‡

PARAMETER			TEST CONDITIONS (SEE NOTES 1 AND 2)		B	TYP	A	UNIT
V_{IH}	High-level input voltage			0°C	−1020		−840	mV
				25°C	−980		−810	
				85°C	−910		−700	
V_{IH}'	High-level input voltage			0°C	−1145			mV
				25°C	−1105			
				85°C	−1035			
V_{IL}	Low-level input voltage			0°C	V_{EE}		−1645	mV
				25°C	V_{EE}		−1630	
				85°C	V_{EE}		−1595	
V_{IL}'	Low-level input voltage			0°C			−1490	mV
				25°C			−1475	
				85°C			−1440	
V_{OH}	High-level output voltage		$V_{IH} = V_{IHB}$, $V_{IL} = V_{ILA}$	0°C	−1000		−840	mV
				25°C	−960		−810	
				85°C	−890		−700	
V_{OL}	Low-level output voltage		$V_{IH} = V_{IHB}$, $V_{IL} = V_{ILA}$	0°C	−1870		−1665	mV
				25°C	−1850		−1650	
				85°C	−1825		−1615	
V_{OH}'	High-level output voltage		$V_{IH} = V_{IH'B}$, $V_{IL} = V_{IL'A}$	0°C	−1020		−840	mV
				25°C	−980		−810	
				85°C	−910		−700	
V_{OL}'	Low-level output voltage		$V_{IH} = V_{IH'B}$, $V_{IL} = V_{IL'A}$	0°C	−1870		−1645	mV
				25°C	−1850		−1630	
				85°C	−1825		−1595	
I_{IH}	High-level input current	$\overline{E}$ inputs	$V_I = -810$ mV,	25°C			265	μA
		Other inputs	Other inputs open				50	
I_{IL}	Low-level input current	$\overline{E}$ inputs	$V_I = -1850$ mV,	25°C	0.5			μA
		Other inputs	Other inputs open		−50			
I_{EE}	Supply current		All inputs and the output open	25°C	−125	−90		mA

NOTES: 1. All parameters are measured with $V_{EE} = -5.200$ V, $V_{CC} = 0$ V, and (unless otherwise noted) the output is connected to −2.000 V through 50 Ω.

2. Test conditions stating $V_{IH} = V_{IHB}$ (or $V_{IH'B}$) and/or $V_{IL} = V_{ILA}$ (or $V_{IL'A}$) mean that the high-level input voltages are equal to the B limit of V_{IH} (or V_{IH}') specified for the particular temperature (see note 3) and/or the low-level input voltages are equal to the appropriate A limit of V_{IL} (or V_{IL}'). The output voltage limits are guaranteed for any appropriate combination of input conditions specified by the function table for the desired output.

3. This data sheet uses the algebraic-limit system that has been adopted by the International Electrotechnical Commission. The A limit is the more positive (less negative) limit; the B limit is the less positive (more negative) limit.

‡The ambient temperature conditions assume air moving perpendicular to the longitudinal axis and parallel to the seating plane of the device at a velocity of 500 feet per minute with the device under test soldered to a 4 x 6 x 0.062-inch double-sided 2-oz copper-clad circuit board.

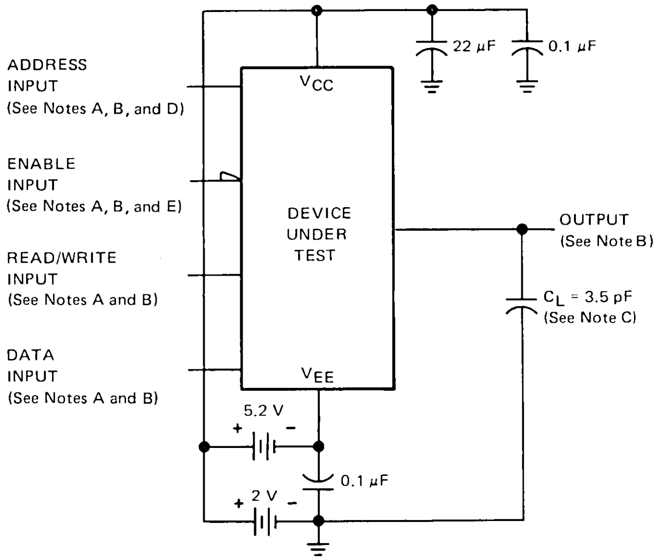
5

switching characteristics at 25°C free-air temperature

PARAMETER			TEST CONDITIONS	B TYP (SEE NOTE 3)	A	UNIT
$t_{a(ad)}$	Access time from address		C_L = 3.5 pF, R_L = 50 Ω, See Figures 6 and 9 and Note 4	18	35	ns
t_{PLH}	Propagation delay time, low-to-high-level output from $\overline{E}$ (enable time)			8	12	ns
t_{PHL}	Propagation delay time, high-to-low-level output from $\overline{E}$ (disable time)			8	12	ns
t_{PHL}	Propagation delay time, high-to-low-level output from read/write			8	17	ns
t_{TLH}	Transition time, low-to-high-level output (20% to 80%)			2.5		ns
t_{THL}	Transition time, high-to-low-level output (80% to 20%)			2.5		ns
t_{SR}	Sense recovery time			8	17	ns
$t_{w(wr,min)}$	Minimum width of write pulse			15	25	ns
$t_{su(min)}$	Minimum setup time	Address before write pulse		−15	8	ns
		Enable before write pulse		−8	2	
		Data before end of write pulse		8	27	
$t_{h(min)}$	Minimum hold time	Address after write pulse		−3	2	ns
		Enable after write pulse		−8	2	
		Data after write pulse		−7	2	

NOTES: 3. This data sheet uses the algebraic limit system that has been adopted by the International Electrotechnical Commission. The A limit is the more positive (less negative) limit; the B limit is the less positive (more negative) limit.
4. Actual values for the minimum width of write pulse, the three minimum setup times, and the three minimum hold times can each be determined separately by setting the other six intervals at their A-limit values.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input waveforms are supplied by generators having the following characteristics: Z_{out} = 50 Ω, PRR = 2 MHz. Transition times of input waveforms are 2 ± 0.1 ns between the 20% and 80% levels and are determined with no device in the socket.
B. The waveforms are monitored on an oscilloscope having the following characteristics: $t_r \leqslant 0.35$ ns, R_{in} = 50 Ω. Input and output cables are equal lengths of 50-Ω coaxial cable.
C. C_L includes jig capacitance.
D. All address lines not under test must be biased to select a memory cell.
E. Enable lines not under test must be at a low logic level.

FIGURE 6—TEST CIRCUIT

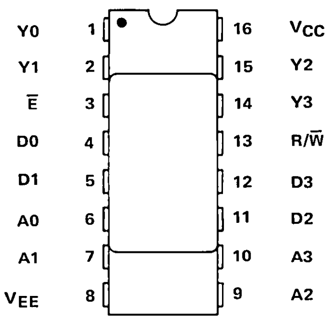
5

TYPE SN10145
64-BIT RANDOM-ACCESS MEMORY

MAY 1975

- Fast Access Time . . . 9 ns Typical
- 16-Word-by-Four-Bit Organization
- Drives 50-Ohm Loads
- Full On-Chip Address Decoding and Output-Sense Amplification
- Capability for Wired-OR Connections
- Low Sensitivity to Supply Voltage Variation

J OR JE
DUAL-IN-LINE PACKAGE (TOP VIEW)



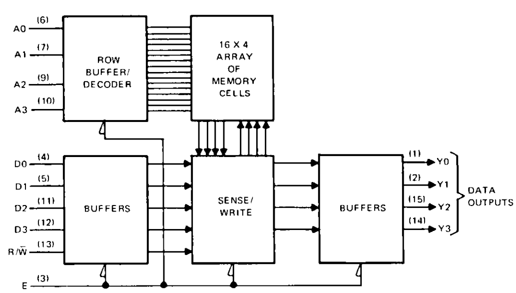
description

This 64-bit active-element memory is a monolithic high-speed, emitter-coupled-logic (ECL) array of 64 storage cells organized to provide 16 words of four bits each. This organization and the high speed makes the SN10145 particularly useful in register file or small scratch-pad applications. Full address decoding and output sense amplification are included on the chip. Each of the 16 words is addressed by the binary address inputs A0 through A3. The output can be connected to other emitter-follower outputs to achieve wired-OR word expansion. The SN10145 is fully compatible with the SN10000 logic family.

Information at the data input is written into the memory by addressing the desired word with the address lines and taking the read/write input low while the enable input is held low. The output is forced low while the memory is in the write mode.

Information stored in the memory is read out by holding the read/write line high, selecting the desired address, and taking the enable input low.

functional block diagram



FUNCTION TABLE

READ/WRITE R/W̅	ENABLE E̅	OPERATION
L	L	Write (output low)
H	L	Read
X	H	Chip disabled (output low)

H = high level, L = low level, X = irrelevant

5

recommended operating conditions

		B	NOM	A	UNIT
		(SEE NOTE 3)			
Supply voltage, V_{EE}		−5.72	−5.2	−4.68	V
Width of write pulse, $t_{w(wr)}$ (see Figure 9)			7.5		ns
Setup time, t_{su} (see Figure 9)	Address before write pulse		3.5		ns
	Enable before write pulse		3		
	Data before end of write pulse		7.5		
Hold time, t_h (see Figure 9)	Address after write pulse		3.5		ns
	Enable after write pulse		3		
	Data after write pulse		3		
Operating ambient temperature, T_A		0		85	°C

electrical characteristics at specified ambient temperature†

PARAMETER		TEST CONDITIONS (SEE NOTES 1 AND 2)		B (SEE NOTE 3)	A	UNIT
V_{IH}	High-level input voltage		0°C	−1020	−840	mV
			25°C	−980	−810	
			85°C	−910	−700	
$V_{IH'}$	High-level input voltage		0°C	−1145		mV
			25°C	−1105		
			85°C	−1035		
V_{IL}	Low-level input voltage		0°C	V_{EE}	−1645	mV
			25°C	V_{EE}	−1630	
			85°C	V_{EE}	−1595	
$V_{IL'}$	Low-level input voltage		0°C		−1490	mV
			25°C		−1475	
			85°C		−1440	
V_{OH}	High-level output voltage	$V_{IH} = V_{IHB}$, $V_{IL} = V_{ILA}$	0°C	−1000	−840	mV
			25°C	−960	−810	
			85°C	−890	−700	
V_{OL}	Low-level output voltage	$V_{IH} = V_{IHB}$, $V_{IL} = V_{ILA}$	0°C	−1870	−1665	mV
			25°C	−1850	−1650	
			85°C	−1825	−1615	
$V_{OH'}$	High-level output voltage	$V_{IH} = V_{IH'B}$, $V_{IL} = V_{IL'A}$	0°C	−1020	−840	mV
			25°C	−980	−810	
			85°C	−910	−700	
$V_{OL'}$	Low-level output voltage	$V_{IH} = V_{IH'B}$, $V_{IL} = V_{IL'A}$	0°C	−1870	−1645	mV
			25°C	−1850	−1630	
			85°C	−1825	−1595	
I_{IH} High-level input current	Any Data input	$V_I = -810$ mV, Other inputs open	25°C		220	µA
	Read/Write input				470	
	Any Address or $\overline{E}$ input				200	
I_{IL}	Low-level input current	$V_I = -1850$ mV, Other inputs open	25°C	0.5		µA
I_{EE}	Supply current	All inputs and outputs open	25°C	−150		mA

NOTES: 1. All parameters are measured with $V_{EE} = -5.200$ V, $V_{CC} = 0$ V, and (unless otherwise noted) the output is connected to −2.000 V through 50 Ω.

2. Test conditions stating $V_{IH} = V_{IHB}$ (or $V_{IH'B}$) and/or $V_{IL} = V_{ILA}$ (or $V_{IL'A}$) mean that the high-level input voltages are equal to the B limit of V_{IH} (or $V_{IH'}$) specified for the particular temperature (see note 3) and/or the low-level input voltages are equal to the appropriate A limit of V_{IL} (or $V_{IL'}$). The output voltage limits are guaranteed for any appropriate combination of input conditions specified by the function table for the desired output.

3. This data sheet uses the algebraic-limit system that has been adopted by the International Electrotechnical Commission. The A limit is the more positive (less negative) limit; the B limit is the less positive (more negative) limit.

†The ambient temperature conditions assume air moving perpendicular to the longitudinal axis and parallel to the seating plane of the device at a velocity of 500 feet per minute with the device under test soldered to a 4 x 6 x 0.062-inch double-sided 2-oz copper-clad circuit board.

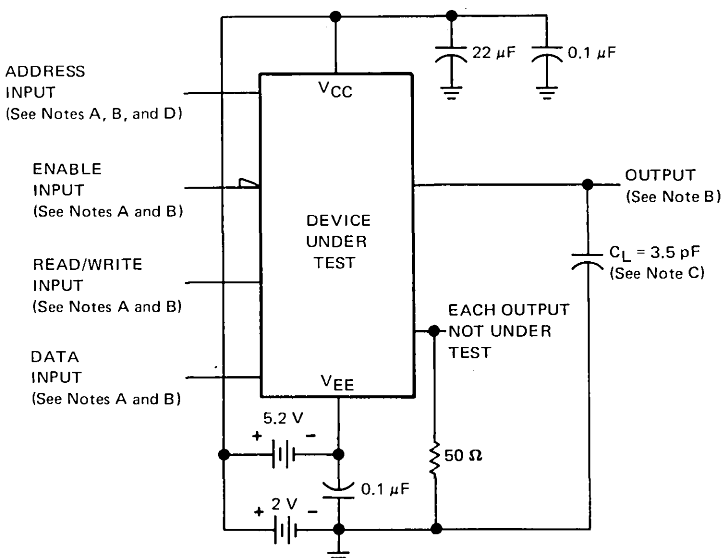
5

switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	B TYP A (SEE NOTE 3)	UNIT
$t_{a(ad)}$	Access time from address	C_L = 3.5 pF, R_L = 50 Ω, See Figures 7 and 9	6	ns
t_{PLH}	Propagation delay time, low-to-high-level output from $\overline{E}$ (enable time)		6	ns
t_{PHL}	Propagation delay time, high-to-low-level output from $\overline{E}$ (disable time)		9	
t_{TLH}	Transition time, low-to-high-level output (20% to 80%)		2.5	ns
t_{THL}	Transition time, high-to-low-level output (80% to 20%)		2.5	
t_{SR}	Sense recovery time		7.5	ns

NOTE 3: This data sheet uses the algebraic-limit system that has been adopted by the International Electrotechnical Commission. The A limit is the more positive (less negative) limit; the B limit is the less positive (more negative) limit.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input waveforms are supplied by generators having the following characteristics: Z_{out} = 50 Ω, PRR = 2 MHz. Transition times of input waveforms are 2 ± 0.1 ns between the 20% and 80% levels and are determined with no device in the socket.

B. The waveforms are monitored on an oscilloscope having the following characteristics: $t_r \leq 0.35$ ns, R_{in} = 50 Ω. Input and output cables are equal lengths of 50-Ω coaxial cable.

C. C_L includes jig capacitance.

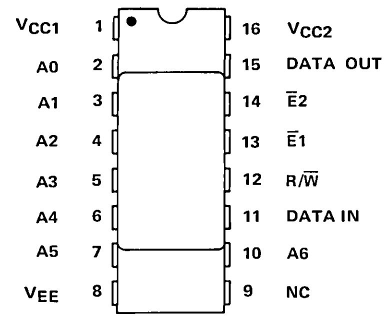
D. All address lines not under test must be biased to select a memory cell.

FIGURE 7—TEST CIRCUIT

5

- Fast Access Time . . . 15 ns Maximum
- 128-Word-by-One-Bit Organization
- Full On-Chip Address Decoding and Output-Sense Amplification
- Capability for Wired-OR Connections
- Low Sensitivity to Supply Voltage Variation

J OR JE
DUAL-IN-LINE PACKAGE (TOP VIEW)



NC—No internal connection

description

This 128-bit active-element memory is a monolithic, high-speed, emitter-coupled-logic (ECL) array of 128 storage cells organized to provide 128 words of one bit each. Full address decoding and output sense amplification are included on the chip. An additional level of decoding is provided for memory systems by the two enable inputs. Each of the 128 words is addressed by the binary address inputs A0 through A6. The output can be connected to other emitter-follower outputs to achieve wired-OR word expansion.

Information at the data input is written into the memory by addressing the desired word with the address lines and taking the read/write input low while both enable inputs are held low. The output is forced low while the memory is in the write mode.

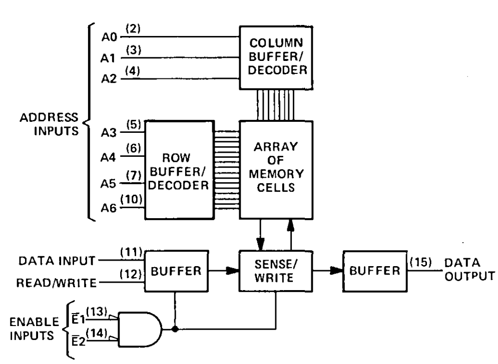
Information stored in the memory is read out by holding the read/write line high, selecting the desired address, and taking both enable inputs low.

FUNCTION TABLE

READ/ WRITE	ENABLE $\overline{E}$1	$\overline{E}$2	OPERATION
L	L	L	Write (output low)
H	L	L	Read
X	H	X	Chip disabled (output low)
X	X	H	Chip disabled (output low)

H = high level, L = low level, X = irrelevant

functional block diagram



5

recommended operating conditions

		B	NOM	A	UNIT
		(SEE NOTE 3)			
Supply voltage, V_{EE}		−5.72	−5.2	−4.68	V
Width of write pulse, $t_{w(wr)}$ (see Figure 9)		8			ns
Setup time, t_{su} (see Figure 9)	Address before write pulse	4			ns
	Enable before write pulse	1			
	Data before end of write pulse	8			
Hold time, t_h (see Figure 9)	Address after write pulse	3			ns
	Enable after write pulse	1			
	Data after write pulse	1			
Operating ambient temperature, T_A		0		85	°C

electrical characteristics at specified ambient temperature†

PARAMETER			TEST CONDITIONS (SEE NOTES 1 AND 2)		B	TYP	A	UNIT
					(SEE NOTE 3)			
V_{IH}	High-level input voltage			0°C	−1020		−840	mV
				25°C	−980		−810	
				85°C	−910		−700	
V_{IH}'	High-level input voltage			0°C	−1145			mV
				25°C	−1105			
				85°C	−1035			
V_{IL}	Low-level input voltage			0°C	V_{EE}		−1645	mV
				25°C	V_{EE}		−1630	
				85°C	V_{EE}		−1595	
V_{IL}'	Low-level input voltage			0°C			−1490	mV
				25°C			−1475	
				85°C			−1440	
V_{OH}	High-level output voltage		$V_{IH} = V_{IHB}$, $V_{IL} = V_{ILA}$	0°C	−1000		−840	mV
				25°C	−960		−810	
				85°C	−890		−700	
V_{OL}	Low-level output voltage		$V_{IH} = V_{IHB}$, $V_{IL} = V_{ILA}$	0°C	−2000		−1665	mV
				25°C	−1990		−1650	
				85°C	−1920		−1615	
V_{OH}'	High-level output voltage		$V_{IH} = V_{IH'B}$, $V_{IL} = V_{IL'A}$	0°C	−1020		−840	mV
				25°C	−980		−810	
				85°C	−910		−700	
V_{OL}'	Low-level output voltage		$V_{IH} = V_{IH'B}$, $V_{IL} = V_{IL'A}$	0°C	−2000		−1645	mV
				25°C	−1990		−1630	
				85°C	−1920		−1595	
I_{IH}	High-level input current	Read/Write	$V_I = -810$ mV, Other inputs open	25°C			355	μA
		Other inputs					265	
I_{IL}	Low-level input current		$V_I = -1990$ mV, Other inputs open	25°C	0.5			μA
I_{EE}	Supply current		All inputs and the output open	25°C	−100	−85	−50	mA

NOTES: 1. All parameters are measured with $V_{EE} = -5.200$ V, $V_{CC1} = V_{CC2} = 0$ V, and (unless otherwise noted) the output is connected to −2.000 V through 50 Ω.
2. Test conditions stating $V_{IH} = V_{IHB}$ (or $V_{IH'B}$) and/or $V_{IL} = V_{ILA}$ (or $V_{IL'A}$) mean that the high-level input voltages are equal to the B limit of V_{IH} (or V_{IH}') specified for the particular temperature (see note 3) and/or the low-level input voltages are equal to the appropriate A limit of V_{IL} (or V_{IL}'). The output voltage limits are guaranteed for any appropriate combination of input conditions specified by the function table for the desired output.
3. This data sheet uses the algebraic-limit system that has been adopted by the International Electrotechnical Commission. The A limit is the more positive (less negative) limit; the B limit is the less positive (more negative) limit.

†The ambient temperature conditions assume air moving perpendicular to the longitudinal axis and parallel to the seating plane of the device at a velocity of 500 feet per minute with the device under test soldered to a 4 x 6 x 0.062-inch double-sided 2-oz copper-clad circuit board.

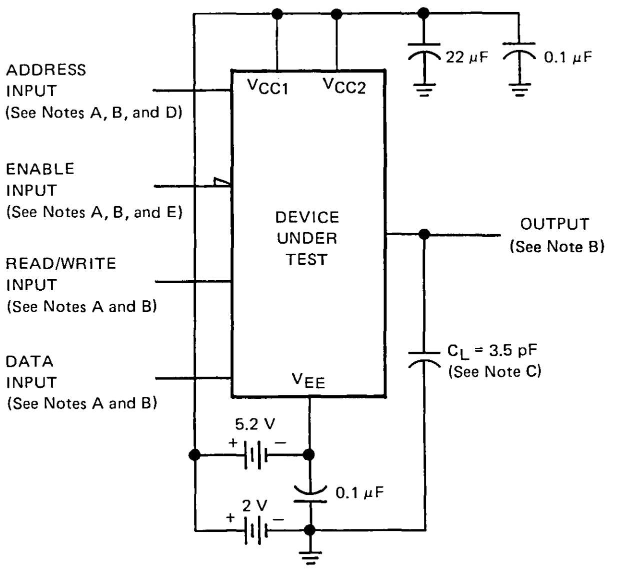
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	B (SEE NOTE 3)	A (SEE NOTE 3)	UNIT
$t_{a(ad)}$	Access time from address	C_L = 3.5 pF, R_L = 50 Ω, See Figures 8 and 9		15	ns
t_{PLH}	Propagation delay time, low-to-high-level output from $\bar{E}$ (enable time)		3	8.5	ns
t_{PHL}	Propagation delay time, high-to-low-level output from E (disable time)		3	8.5	ns
t_{TLH}	Transition time, low-to-high-level output (20% to 80%)		1	2.5	ns
t_{THL}	Transition time, high-to-low-level output (80% to 20%)		1	2.5	ns
t_{SR}	Sense recovery time			10	ns

NOTE 3: This data sheet uses the algebraic-limit system that has been adopted by the International Electrotechnical Commission. The A limit is the more positive (less negative) limit; the B limit is the less positive (more negative) limit.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input waveforms are supplied by generators having the following characteristics: Z_{out} = 50 Ω, PRR = 2 MHz. Transition times of input waveforms are 2 ± 0.1 ns between the 20% and 80% levels and are determined with no device in the socket.

B. The waveforms are monitored on an oscilloscope having the following characteristics: $t_r \leqslant 0.35$ ns, R_{in} = 50 Ω. Input and output cables are equal lengths of 50-Ω coaxial cable.

C. C_L includes jig capacitance.

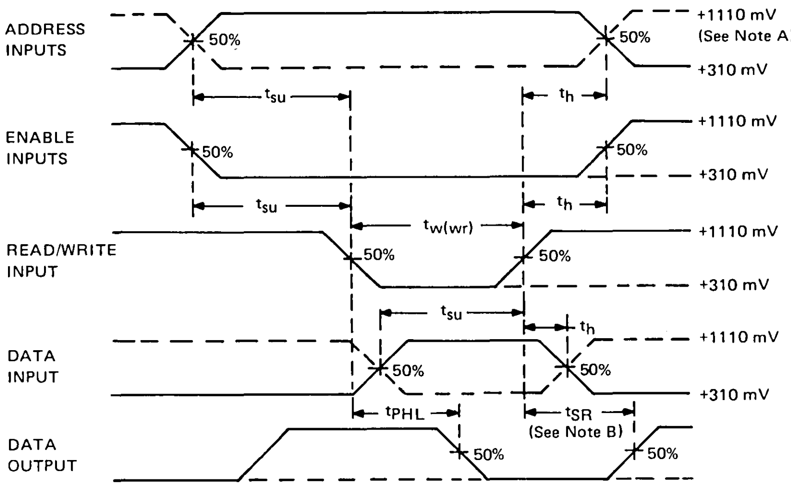
D. All address lines not under test must be biased to select a memory cell.

E. Enable line(s) not under test must be at a low logic level.

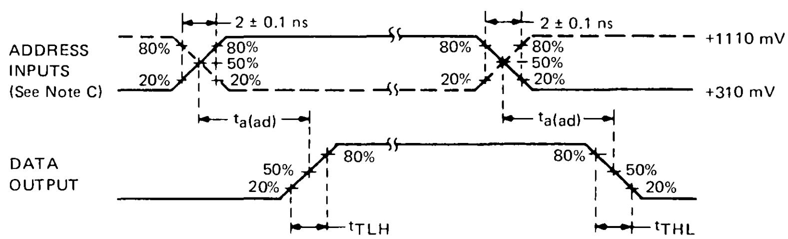
FIGURE 8—TEST CIRCUIT

5

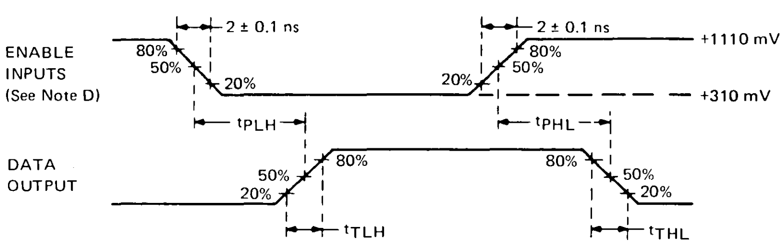
PARAMETER MEASUREMENT INFORMATION



WRITE CYCLE VOLTAGE WAVEFORMS



ACCESS TIME FROM ADDRESS INPUTS



ENABLE AND DISABLE TIMES

NOTES: A. Voltage values on input waveforms are with respect to ground.
B. Sense recovery time can only be measured following the writing of a high-level input.
C. All enable inputs are low, read/write input is high.
D. Read/write input is high, other enable input(s) is(are) low, bit location addressed contains high-level data.

FIGURE 9—VOLTAGE WAVEFORMS

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPICAL CHARACTERISTICS†

HIGH-LEVEL AND LOW-LEVEL
OUTPUT VOLTAGES
vs
AMBIENT TEMPERATURE

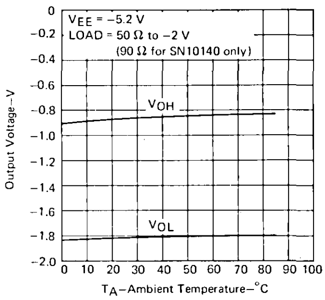


FIGURE 10

HIGH-LEVEL and LOW-LEVEL OUTPUT VOLTAGES
vs
SUPPLY VOLTAGE

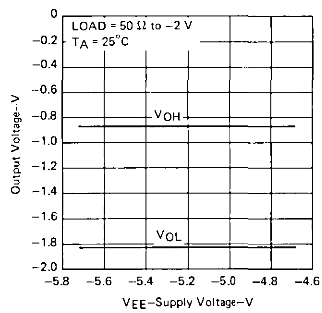


FIGURE 11

OUTPUT VOLTAGE
vs
OUTPUT CURRENT

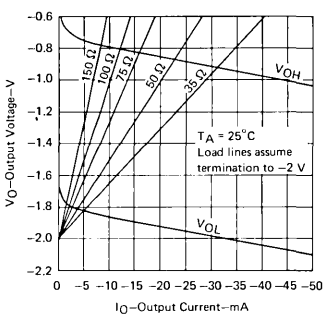


FIGURE 12

INPUT CURRENT
vs
INPUT VOLTAGE

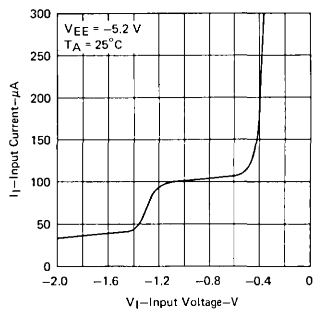


FIGURE 13

TRANSITION TIME,
LOW-TO-HIGH-LEVEL OUTPUT
vs
SUPPLY VOLTAGE

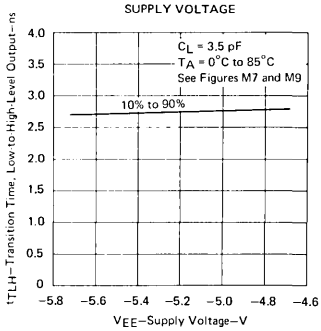


FIGURE 14

TRANSITION TIME,
HIGH-TO-LOW-LEVEL OUTPUT
vs
SUPPLY VOLTAGE

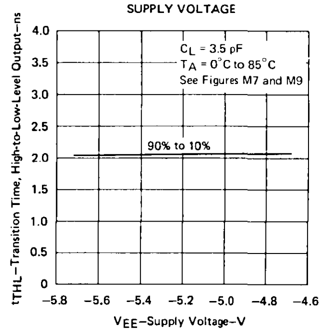


FIGURE 15

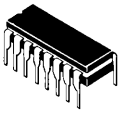
†The ambient temperature conditions assume air moving perpendicular to the longitudinal axis and parallel to the seating plane of the device at a velocity of 500 feet per minute with the device under test soldered to a 4 x 6 x 0.062-inch double-sided 2-oz copper-clad circuit board.

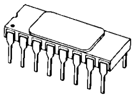
ECL MEMORIES MECHANICAL DATA

MECHANICAL DATA AND ORDERING INSTRUCTIONS

general

The availability of a particular Series SN10000 part in a particular package is denoted by an alphabetical reference above the pin-connection diagrams. Series SN10000 memories are available in the J and JE ceramic packages. Orders for these circuits should include the package outline letter(s) (J or JE) at the end of the circuit type number; e.g., SN10139J, SN10145JE.

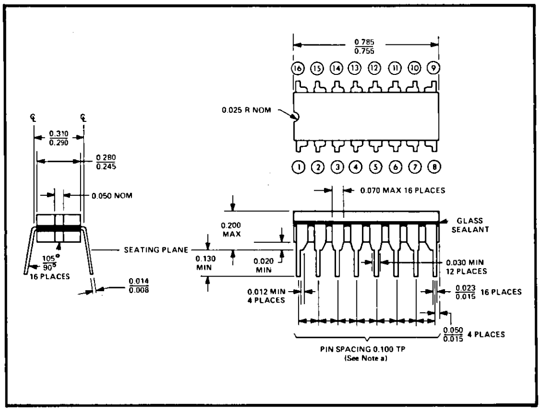




J ceramic dual-in-line package

This hermetically sealed, dual-in-line package consists of a ceramic base, ceramic cap, and 16-lead frame. The package is intended for insertion in mounting-hole rows on 0.300-inch centers. Once the leads are compressed to 0.300-inch separation, sufficient tension is provided to secure the package in the board during soldering. Tin-plated (bright-dipped) leads require no additional cleaning or processing when used in soldered assembly.

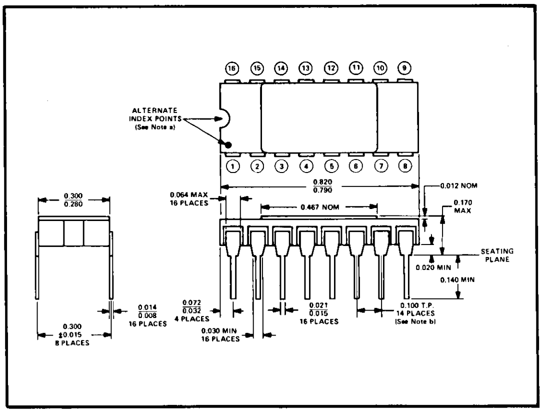
5



NOTES: a. Each pin centerline is located within 0.010 inch of its true longitudinal position.
b. All dimensions are in inches unless otherwise noted.

JE ceramic dual-in-line package

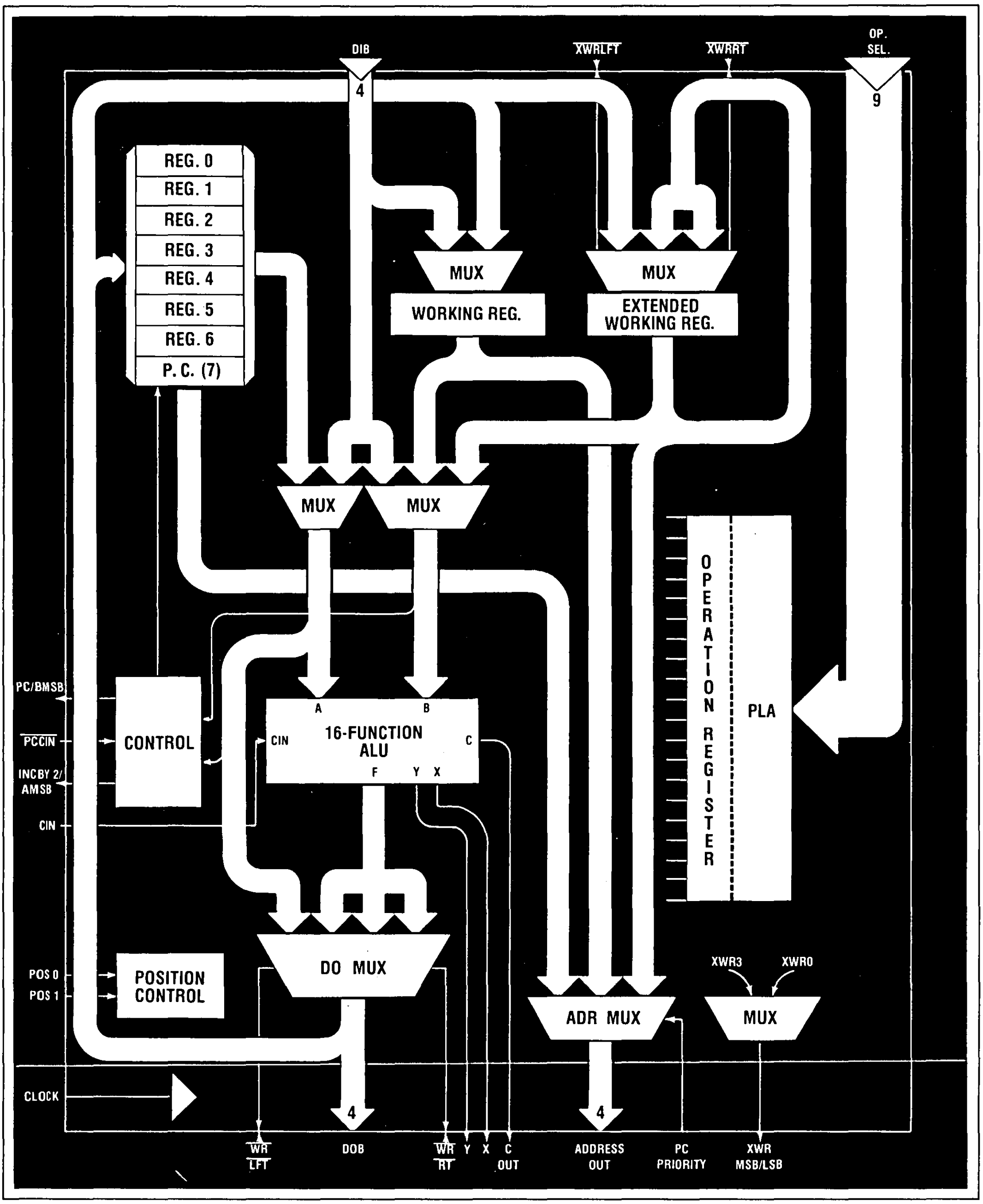
This ceramic dual-in-line package has 16 leads attached by brazing and a gold-plated lid hermetically sealed to the header at relatively low temperature using a solder preform. The package is intended for insertion in mounting-hole rows on 0.300-inch centers. The gold-plated leads require no additional cleaning or processing when used in soldered or welded assembly.



NOTES: a. Terminal identification is provided by either a notch with a nominal radius of 0.032 inch or a dot on the body near the number-one terminal.
b. Each pin centerline is located within 0.010 inch of its true longitudinal position.
c. All dimensions are in inches.

Microprocessor Summary

6


DIB
XWRLFT
XWRRT
OP. SEL.
4
9
REG. 0
REG. 1
REG. 2
REG. 3
REG. 4
REG. 5
REG. 6
P. C. (7)
MUX
WORKING REG.
MUX
EXTENDED WORKING REG.
MUX
MUX
OPERATION REGISTER
PLA
PC/BMSB
PCCIN
INCBY 2/ AMSB
CIN
CONTROL
A
B
CIN
16-FUNCTION ALU
C
F
Y
X
DO MUX
POS 0
POS 1
POSITION CONTROL
XWR3
XWR0
ADR MUX
MUX
CLOCK
4
4
WR LFT
DOB
WR RT
Y
X
C OUT
ADDRESS OUT
PC PRIORITY
XWR MSB/LSB

SBP0400

4-bit slice microprogrammable microprocessor element. Integrated Injection Logic. ....from Texas Instruments.

The SBP0400 is a digital processor building block and the first of the standard Integrated Injection Logic (I^2L) ICs from TI.

The 0400 combines the unique properties of I^2L technology with an expandable 4-bit slice architecture to offer an unmatched level of performance and design flexibility.

It's microprogrammable. You build instructions by externally sequencing the 0400's factory-programmed micro-operations. Emulate existing designs, at either the micro or macro level, with software compatibility. Or create highly efficient new designs with tailored instructions.

With over 1,600 gates, monolithically integrated into a 40-pin package, the 0400 offers the basis for efficient, low cost design solutions to a host of applications in both industrial (0° to 70°C) and military (−55° to 125°C) environments.

The SBP0400 is also directly expandable to any word size which is a multiple of 4-bits.

Some examples: One SBP0400 can make a basic 4-bit intelligent controller. Two, in parallel, makes an 8-bit dedicated processor. Three makes a 12-bit controller. And, with four—the CPU of a general purpose 16-bit "mini".

SBP0400 is characterized by the ability to perform any one of its 512 preprogrammed micro-operations within a single clock cycle.

Basic Architecture

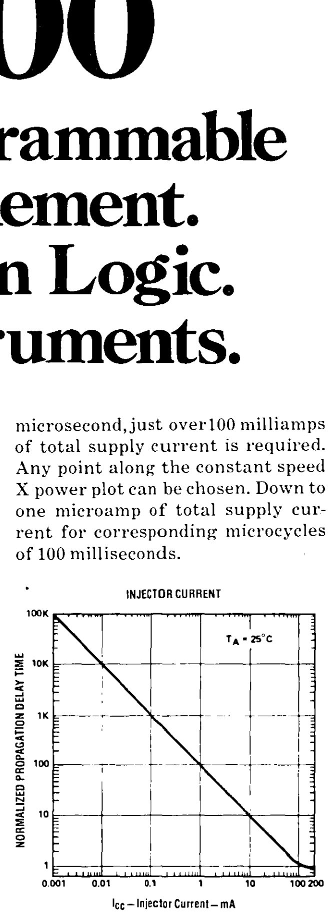
- Microprogrammable, bit-slice design expandable in 4-bit multiples.
- Parallel access to all control, data and address functions.
- 16-function ALU with full-carry look ahead capability.
- 8-word general register file including independent program counter with incrementor.
- Dual 4-bit working registers with full shifting capability.
- On-chip factory programmable logic array (PLA) contains a repertoire of 512 micro-operations.

Functional Power

- Static edge-triggered operation with full TTL compatibility.
- ALU operand modifications/combination via 8 arithmetic or 8 Boolean functions.
- Bidirectional logic/arithmetic shift/circulate of single/double signed, single/double precision binary words.
- Single clock ALU-shift combinations simplify implementation of iterative multiply and non-restore divide algorithms.
- Internal operation register and independent program counter provide pipelining capability.

Performance: The SBP0400 operates at a constant speed X power product over a 10^5 performance range. Virtually any single DC power source, voltage or current, can be used.

Speed is a direct function of supply current. As the graph shows: For typical microcycle times of one microsecond, just over 100 milliamps of total supply current is required. Any point along the constant speed X power plot can be chosen. Down to one microamp of total supply current for corresponding microcycles of 100 milliseconds.



Design with the 0400 and the choice is yours: Word size. Instruction set. Power and speed. Use your imagination. The SBP0400 is just the beginning.

Engineering evaluation devices are available now. Designated X0400N, they are $90.00 each (1-24). Order directly from your nearest TI Sales Office. A product manual accompanies purchase. For a "Mini-Spec" write Texas Instruments Incorporated, P.O. Box 5012 M/S 308, Dallas, Texas 75222.

6

TMS 1000 NC, TMS 1200 NC
MICROCOMPUTERS

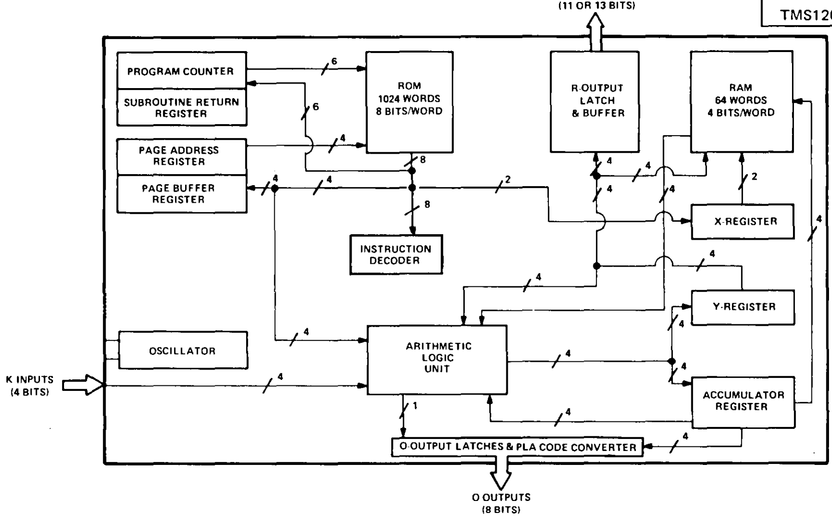
DESCRIPTION

The TMS1000 series is a family of P-channel MOS four-bit microcomputers with a ROM, a RAM, and an arithmetic logic unit on a single semiconductor chip. The TMS1000 family is unique in the field of microprocessors because this device is a single-chip binary computer. A customer's specification determines the software that is reproduced during wafer processing by a single-level mask technique that defines a fixed ROM pattern. This versatile one-chip computer is very cost effective and capable of performing a variety of complex functions.

Key features of the TMS1000 series are:

- 8192-bit Read-Only Memory (ROM) on chip
- 256-bit Random-Access Memory (RAM) on chip
- 11 latched control/data-strobe outputs in a 28-pin package
- 13 latched control/data-strobe outputs in a 40-pin package
- 8 parallel data outputs and output programmable logic array (PLA)
- Arithmetic Logic Unit (ALU) and 2 four-bit working registers on chip
- On-chip oscillator, or external synchronization if desired
- Conditional branching and subroutines
- Four-bit parallel data input
- Programmable instruction decoder
- Single-power-supply operation
- TTL compatible

TMS1000 SERIES	
DEVICE	PACKAGE
TMS1000NC	28-Pin DIP
TMS1200NC	40-Pin DIP



TMS1000-SERIES LOGIC BLOCKS

One major advantage of the TMS1000 series is flexibility. The TMS1000 series is effective in applications such as printer controllers, data terminals, remote sensing systems, cash registers, appliance controls, and automotive applications. Through the TMS1000 series versatility, a wide range of systems realize reduced costs, fewer parts, and high reliability.

The microcomputer's ROM program controls data input, storage, processing, and output. Data processing takes place in the arithmetic logic unit. K input data goes into the ALU, as shown in the figure above, and is stored in the four-bit accumulator. The accumulator output accesses the output latches, the RAM storage cells, and the adder input. Data storage in the 256-bit RAM is organized into 64 words, four bits per word. The four-bit words are conveniently grouped into four 16-word files addressed by a two-bit register. A four-bit register addresses one of the 16 words in a file by ROM control.

The O outputs and the R outputs are the output channels. The eight parallel O outputs are decoded from five data latches. The O outputs serve many applications because the decoder is a programmable logic array (PLA) that is modified by changing the gate-level mask tooling. Each of the thirteen R outputs of the TMS1200NC and the eleven R

6

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

outputs on the TMS1000NC has an individual storage element that can be set or reset by program control. The R outputs send status or enable signals to external devices. The R outputs strobe the O outputs to displays, to other TMS1000 series chips, or to TTL and other interface circuits. The same R outputs multiplex data into the K inputs whenever necessary.

There are 43 basic instructions that handle I/O, constant data from the ROM, bit control, internal data transfer, arithmetic processing, branching, looping, and subroutines. The eight-bit instruction word performs 256 unique operations for maximum efficiency.

DESIGN SUPPORT

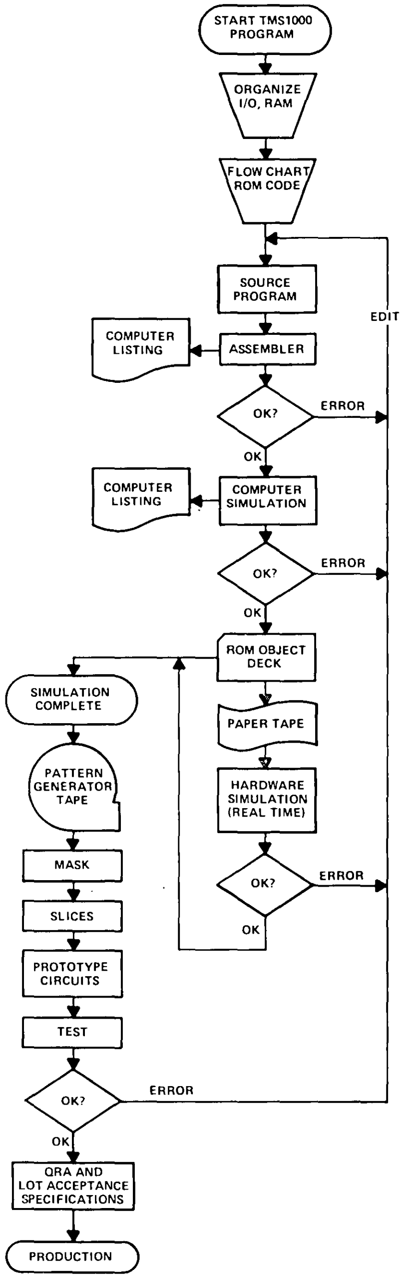
Through a staff of experienced application programmers, Texas Instruments will, upon request, assist customers in evaluating applications, in training designers to program the TMS1000 series and in simulating programs. TI will also contract to write programs to customer's specifications.

TI has developed an assembler and simulator for aiding software designs. These programs are available on nationwide time-sharing systems and at TI computer facilities.

A TMS1000 series program (see flowchart) is written in assembly language using standard mnemonics. The assembler converts the source code (assembly language program) into machine code, which is transferred to a software simulation program. Also the assembler produces a machine code object deck. The object deck is used to produce a tape for hardware simulation or a tape for generating prototype tooling.

The TMS1000 series programs are checked by software and hardware simulation. The software simulation offers the advantages of printed outputs for instruction traces or periodic outputs. The hardware simulation offers the designer the advantages of real-time simulation and testing asynchronous inputs. A software user's guide is available.

After the algorithms have been checked and approved by the customer, the final object code and machine option statements are supplied to TI. A gate mask is generated and slices produced. After assembly and testing, the prototypes are shipped to the customer for approval. Upon receiving final approval, the part is released for volume production at the required rate as one unique version of the TMS1000 family.



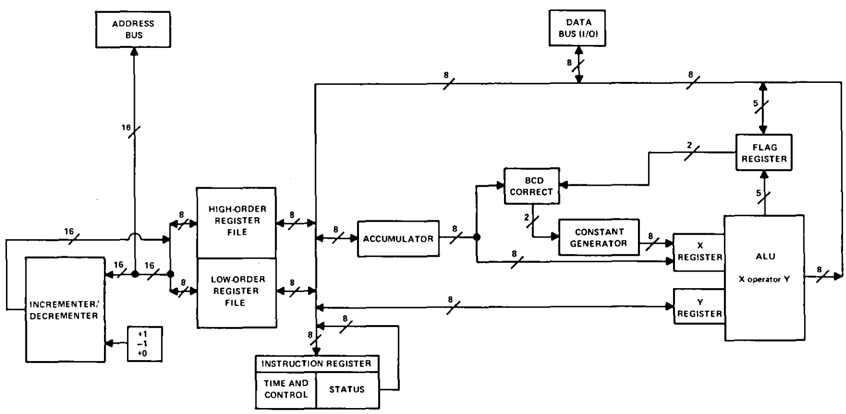
TMS1000-SERIES ALGORITHM DEVELOPMENT

6

TMS 8080, TMS 5501
8-BIT MOS MICROPROCESSOR SYSTEM

TMS 8080
An Eight-Bit Central Process Unit

- 2-μs Instruction Cycle Time
- Addresses up to 65,536 Words of Memory
- 8-Bit Bidirectional I/O Bus
- Serves up to 256 Input and 256 Output Ports
- Uses a Memory Stack for Subroutine Saves
- 8 Vectored Interrupts
- 9 Internal Registers
- 78 Instructions
- Power Supplies: 12 V, 5 V, 0 V, –5 V
- TTL-Compatible

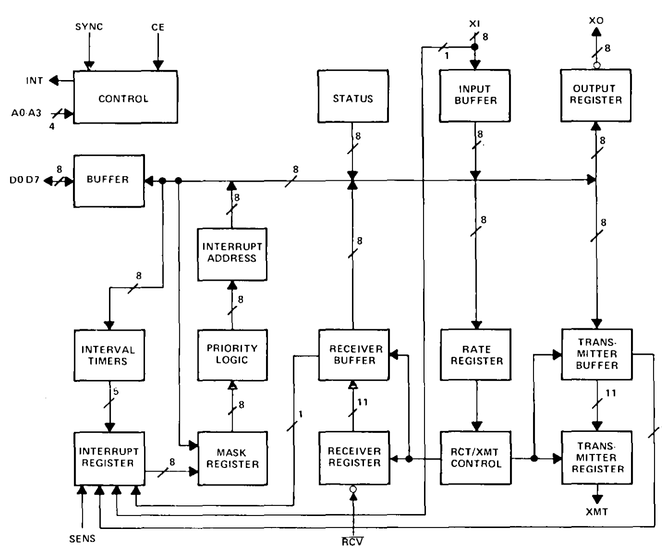


6

TMS 5501

A multifunction input/output circuit that is controlled by the TMS 8080 through memory referencing instructions. The TMS 5501 provides a TMS 8080 microprocessor system with a synchronous data interface, data I/O buffers, interrupt control logic, and interval timers. The TMS 8080 causes data to be transferred by the TMS 5501 by issuing commands via the system address bus. These commands include:

- read the serial receive register
- read the external data input lines
- read the interrupt address
- read TMS 5501 status information
- issue discrete commands
- load baud-rate register
- load the serial transmiter register
- load the output register
- load the interrupt mask
- load an interval timer



38510/MACH IV

High-Reliability Microelectronics Procurement Specifications

MIL-STD-883

7

CONTENTS

7

REVISIONS

CLASSIFICATION (MAJOR/MINOR)	DATE CODE EFFECTIVITY	LTR	DESCRIPTION	DATE	APPROVED
Major	7040	A	Incorporate MIL-M-38510 and Revision Notice 2 of MIL-STD-883	8/15/70	J Adams
Major	7239	B	Incorporate Revision Notice 3 and 4 of MIL-STD-883 and Revision A of MIL-STD-38510	9/1/72	JDA
Major	7401	C	Incorporate revised Level IV (SNH) processing with inclusion of recorded electrical data with delta requirements; incorporate technological criteria in Table III for precap of complex circuits.	1/1/74	JAK
Minor	7518	D	Incorporate Revision A of MIL-STD-883 and provisions for MOS LSI and CMOS devices	4/15/75	D.S.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES: ANGLES ± 1° 3 PLACE DECIMAL ±.010 2 PLACE DECIMAL ±.02	DR C. E. Smith DATE 9/22/69	TEXAS INSTRUMENTS INCORPORATED SEMICONDUCTOR CIRCUITS DIVISION DALLAS, TEXAS
INTERPRET DWG. IN ACCORDANCE WITH STD. DESCRIBED IN MIL-STD-100	CHK 10/17/69	TITLE MICROELECTRONICS, HIGH RELIABILITY PROCUREMENT SPECIFICATION (MIL-STD 38510/883)
MATERIAL:	ENGR 10/20/69	
	QUALITY CONTROL 10/29/69	
	QRA MGR. JD Adams 10/31/69	
	DESIGN ACTIVITY RELEASE DEPARTMENT MANAGER, TTL	SIZE A — CODE IDENT NO. 01295 — DRAWING NO. 38510/MACH IV PROGRAM
	CIRCUITS DIVISION MANAGER	SCALE — REV D — SHEET

7

7

38510/MACH IV PROGRAM

1.0 **SCOPE**

1.1 This specification establishes standards for materials, workmanship, performance capabilities, identification, and processing of high-reliability monolithic integrated circuits.

1.2 Intent

The intent of this document is such as to recognize that quality and reliability are *built* into, not *tested* into, a product. There is no specification or screening procedure that can substitute for inherent, built-in reliability. However, it must be realized that irrespective of lot quality, there will always be some small percentage of devices that are subject to early failure (infant mortality). A well engineered screening procedure will eliminate most, if not all, of these early failures. Secondly, the screening and acceptance testing described herein will also serve to demonstrate, with a high degree of statistical confidence, that the required levels of quality and reliability have, in fact, been built into the product.

2.0 **APPLICABLE DOCUMENTS**

2.1 The following specifications and standards, of the issue in effect on the date of invitation for bids or request for proposal, form a part of this specification to the extent specified herein:

2.2 Specifications

Military

MIL-M-55565	Microcircuits, Packaging of
MIL-M-38510	Microcircuits devices, general specification for

2.3 Standards

Military

MIL-STD-105	Sampling Procedures and Tables for Inspection by Attributes
MIL-STD-883	Test Methods and Procedures for Microelectronics
MIL-STD-790	Reliability Assurance Program for Electronic Parts Specification
MIL-STD-1276	Leads, Weldable, for Electronic Components Parts
MIL-STD-1313	Microelectronics Terms and Definitions

Detail Specifications

SNXXXX (Bipolar) TMSXXXX (MOS LSI) TFXXXX (CMOS)	Detail Specification for a Particular Part Type (e.g., Manufacturer's Data Sheet)

2.4 Precedence of Documents

For the purpose of interpretation, in case of any conflicts, the following order of precedence shall apply:

a) Purchase Order	—The purchase order shall have precedence over any referenced specification.
b) Detail Specification	—The detail specification shall have precedence over this specification and other referenced specifications.
c) This Specification	—This specification shall have precedence over all referenced specifications.
d) Referenced Specifications	—Referenced Specifications shall apply to the extent specified herein.

2.5 Federal and/or military specifications and standards required shall be obtained from the usual government sources.

3.0 GENERAL REQUIREMENTS

The individual item requirements shall be as specified herein and in accordance with the applicable detail specification. In the event of any conflict between the requirements of this specification and the detail specification, the latter shall govern. The static and dynamic electrical performance requirements of the integrated circuits plus absolute maximum ratings and test methods shall be as specified in the detail specifications.

3.1.1 Definitions

a)	LTPD	Lot Tolerance Percent Defective shall be as defined by MIL-M-38510.
b)	λ	Lambda, stated in percent per 1000 hours as defined by MIL-M-38510.
c)	MRN	Minimum reject number as defined by MIL-M-38510.
d)	Production Lot	For the purpose of this specification, a production lot shall be defined per MIL-M-38510.
e)	Inspection Lot	An inspection lot shall be as defined in MIL-M-38510.
f)	C	Acceptance number as defined by MIL-M-38510.

3.1.2 Terms and Definitions

Terms and definitions shall be as defined in MIL-STD-1313.

3.1.3 Classification of Requirements

The requirements for the integrated circuits are classified herein as follows:

Requirement	Paragraph
Process Conditioning, Testing and Screening	3.2
Qualification	3.3
Design and Construction	3.4

3.2 Process Conditioning, Testing and Screening

Three levels of screening and quality assurance for integrated circuits are provided for in this specification. Process conditioning, testing and screening shall be as specified in 4.3 and the applicable figure for the appropriate quality assurance level stated on the purchase order and defined as follows:

SCREENING LEVEL	PART NUMBER PREFIX			APPLICABLE FLOW CHART
	BIPOLAR	CMOS	MOS LSI	
38510/883 Class A (Level IV)	SNH	TFH	Not Avail.	Figure 4
38510/883 Class B (Level III)	SNC	TFC		Figure 3
			SMC	Figure 2
38510/883 Class C (Level I)	SNM	TFM	Not Avail.	Figure 1

3.3 Qualification

Vendor qualification for delivery of integrated circuits to this specification shall be as specified in paragraph 4.2.

3.4 Design and Construction

7

Integrated circuit design and construction shall be in accordance with the requirements specified herein and in the applicable detail specification.

3.4.1 Topography

Integrated circuits furnished under this specification shall have topography information available for review by procuring activity. The information made available shall provide sufficient data for thorough circuit design, application, performance, and failure analysis studies.

3.4.1.1 Monolithic Die Topography

An enlarged photograph or drawing (to scale) with a minimum magnification of 80 times the die (chip) size showing the topography of elements formed on the silicon monolithic die shall be available for review. This shall be identified with the specific detail integrated circuit part-type in which it is used and the applicable detail specification.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

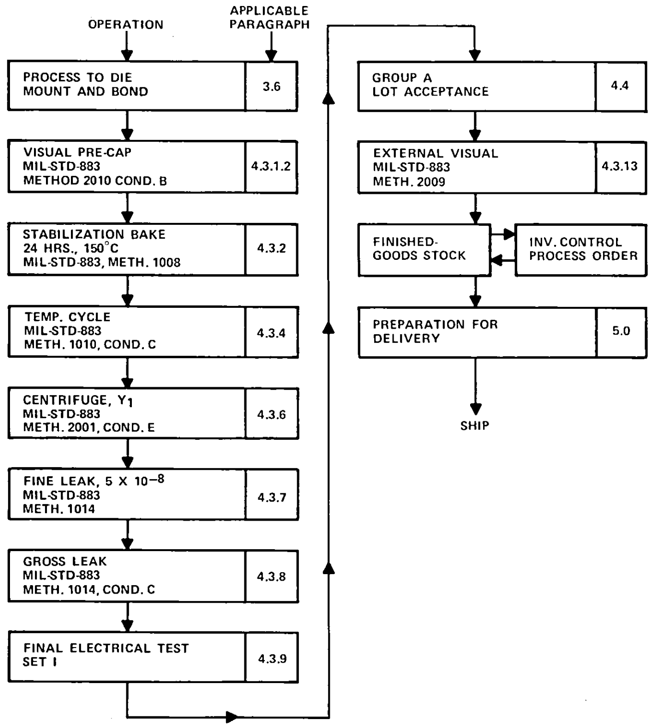


FIGURE 1—FLOW CHART FOR 38510 CLASS C LEVEL I

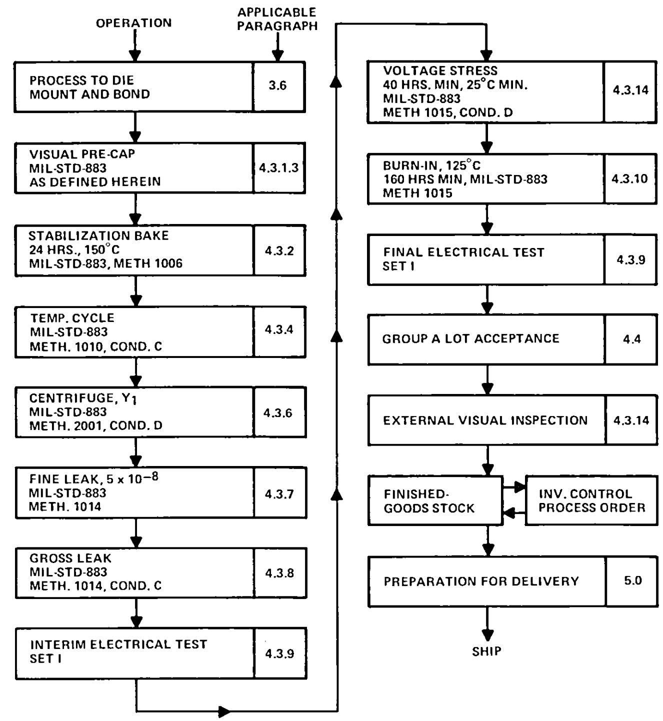


FIGURE 2—FLOW CHART FOR MOS LSI 38510 CLASS B (LEVEL III SMC)

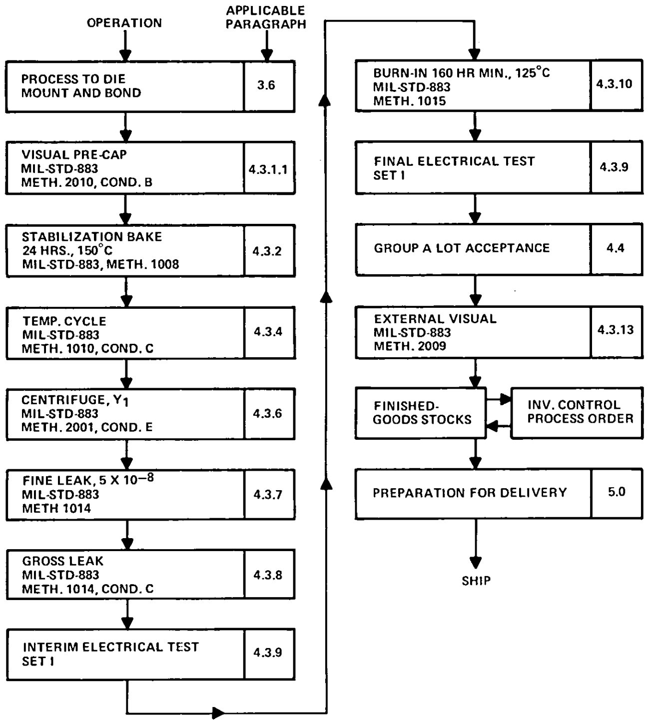


FIGURE 3—FLOW CHART FOR 38510 CLASS B LEVEL III

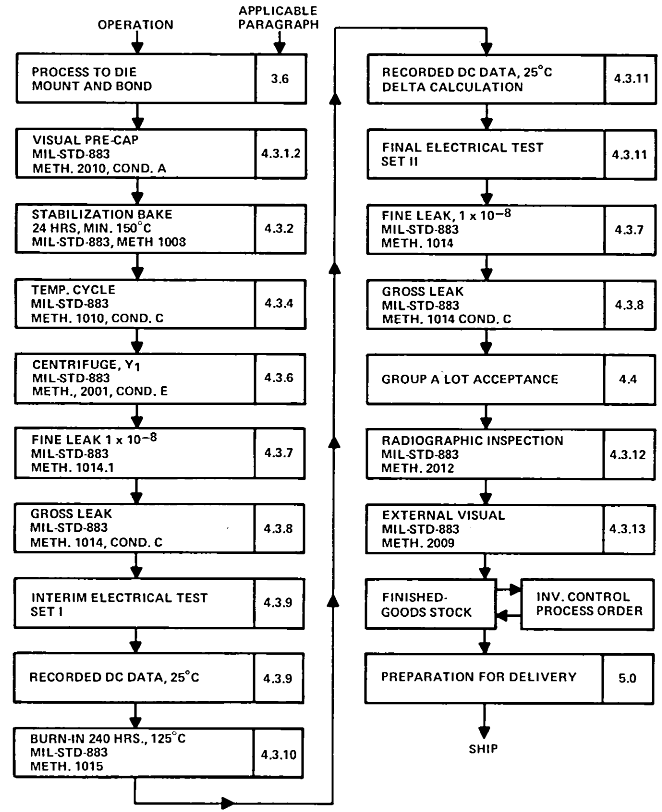


FIGURE 4—FLOW CHART FOR 38510 CLASS A LEVEL IV

3.4.1.2 Die Intraconnection Pattern

An enlarged photograph or drawing (to scale) with a minimum magnification of 80 times the die (chip) size showing the specific intraconnection pattern utilized to intraconnect the elements in the circuit. This shall be in the same scale as the die topography 3.4.1.1 so that the elements utilized and those not being used can easily be determined.

3.4.2 Materials

Materials shall be inherently non-nutrient to fungus and shall not blister, crack, outgas, soften, flow or exhibit other immediate or latent defects that adversely affect storage, operation or environmental capabilities of integrated circuits.

3.4.2.1 Material Selection

Materials selected for use in the construction of the integrated circuits shall be chosen for maximum suitability for the application. This shall include consideration of the best balance for:

a) Electrical performance

b) Thermal compatibility and conductivity

c) Chemical stability including resistance to deleterious interactions with other materials

d) Metallurgical stability with respect to adjacent materials and change in crystal configuration

e) Maximum stability with regard to continued uniform performance through the specified environmental conditions and life.

3.4.2.2 Foreign Materials

No lacquer, grease, paste, desiccant or other similar foreign encapsulant or coating material shall be included in the circuit enclosure nor applied to any part of the internal circuit assembly.

3.4.3 Mechanical

3.4.3.1 Case

Each integrated circuit shall be securely mounted and hermetically sealed within a case designed and constructed to conform to the outline and physical dimensions shown in the detailed specification.

3.4.3.2 Interconnections

Interconnections within the integrated circuit case shall be minimized and there shall be no wire crossovers. Circuit intraconnections by means of wire jumpers shall not be used. (See Note 6.2)

3.4.3.3 Leads

Lead material, construction, and outline shall be as specified on the detail specification and shall be capable of meeting the solderability test of MIL-STD-883, Method 2003. (See note 6.4).

3.4.3.3.1 Lead Size

Lead outline and dimensions shall be as specified in the detail specification.

3.4.3.3.2 Lead Surface Condition

Leads shall be free of the following defects over their entire length when inspected under a minimum of 4X magnification:

a) Foreign materials adhering to the leads such as paint, film, deposits and dust. Where adherence of such foreign materials is in question, leads may be subjected to a clean, contaminant-free (e.g., oil, dust, etc.), filtered air stream (suction or expulsion) of 88 feet per second maximum, or a wash/rinse as necessary and reinspected.

b) Nicks, cuts, scratches or other surface defacing defects which expose the base metal.

3.4.3.3.3 Lead Straightness

Leads shall be aligned within a 0.050-inch diameter, 0.050-inch length cylinder concentric to the point of lead emergence from the case and the X-axis (the axis parallel to the lead axis). Along the remaining lead length, there shall be no unspecified bend whose radius is less than 0.10 inch and no twist whose angle is greater than 30° (ribbon leads, only).

3.4.3.3.4 Preformed Leads

Preformed leads, when specified, shall be in accordance with the detail specification. The part number of the integrated circuit shall remain as specified in the applicable detail specification or purchase order, the applicable suffix designation shall appear on the purchase order but shall not be marked on the device.

3.4.3.3.5 Carriers (Mech-Pak Carrier)

Carrier-matrix assemblies consisting of individually mounted integrated circuits shall be furnished when so specified by purchase order. The individual carriers shall have provisions for use with automatic test equipment contacts. Devices supplied "clipped-out" of the Mech-Pak Carrier shall be supplied in the Barnes Carrier type 029-188 or equivalent. (Applicable to Flat Packs only.)

3.5 Marking of Integrated Circuits

3.5.1 Legibility

All marking shall be permanent in nature and remain legible when subjected to specified operating, storage, and environmental requirements. All markings shall be insoluble in standard solvents such as trichlorethylene, water and xylene.

3.5.2 Marking Details

Marking of the integrated circuits shall be located as follows unless otherwise specified in the detail specification:

a) TO-99, TO-100, and similar "can" cases shall be marked on the top of the case. Where space limitations exist, the side of the case may be used.

b) Flat Packs shall be marked on the top of the case. Where space limitation exists, the bottom of the package may be utilized as necessary. As a minimum the top of the package shall show the manufacturer's identification mark or symbol, the device part number, date code, and pin 1 orientation mark (where applicable).

c) Dual-in-line plug-in packages shall be marked in the same manner as flat packs.

3.5.3 Required Device Marking

a) Index point indicating the starting point for numbering of leads shall be as indicated in the detail specification. The indexing point may be a tab, color dot, or other suitable indicator.

b) Manufacturer's identification mark or symbol.

c) An alpha-numeric lot date code indicating the week of initial submission for screening or inspection. The date code shall be as follows:

   1) EIA four-digit date code, the first two numbers shall be the last two digits of the year, the last two numbers shall indicate the calendar week.

2) A Gothic letter which identifies separate lots of the same device type processed within the same calendar week. (If no more than one lot is processed through screening or inspection in a given calendar week, the Gothic letter may be omitted.)

d) Manufacturer's part number defining circuit type and applicable MIL-STD-883 screening level and MIL-M-38510 product assurance level as defined in paragraph 3.2.

e) Individual device serial number is required for Class A (SNH).

f) A dot to indicate acceptance by Radiographic inspection

NOTE:

When a color dot is used to identify pin one, the radiographic inspection acceptance dot shall be placed on the bottom of the package.

g) Gothic letter per U.S. Customs code preceding data code identifies assembly location.

3.6 Product Assurance

The manufacturer shall establish and maintain a reliability assurance program that complies with the basic intent of MIL-STD-790. Furthermore, it is intended that each integrated circuit delivered shall be free of any defect in design, material, manufacturing process, testing and handling, which would degrade or otherwise limit its performance when used within the specified limits.

3.6.1 Visual and Mechanical Examination

Integrated circuits shall be examined to verify that material, design, construction, physical dimensions, marking and workmanship are in accordance with the specified acceptance criteria.

3.6.2 Test Equipment

The manufacturer shall prepare and maintain a current list, by name and drawing number or other unique identification, of test equipment used in the manufacturing and testing of devices submitted for acceptance inspection under this specification. This list shall be made available to the procuring activity representative upon request.

3.6.3 Process Controls

Each integrated circuit shall be constructed by manufacturing processes which are under the surveillance of the manufacturer's Quality Control department. The processes shall be monitored and controlled by use of statistical techniques in accordance with published specifications and procedures. The manufacturer shall prepare and maintain suitable documentation (such as quality control manuals, inspection instructions, control charts, etc.) covering all phases of incoming part and material inspection and in-process inspections required to assure that product quality meets the requirements of this specification. The

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

procuring activity may verify, with the permission of and in the company of the manufacturer's designated representative, that suitable documentation exists and is being applied. Information designated as proprietary by the manufacturer will be made available to the procuring activity or its representative only with the written permission of the manufacturer.

Process control is recognized as being vital to the concept of "built-in" quality. The process control program shall include a scanning electron microscope (SEM) monitor program for evaluating the metal integrity over oxide step and oxide step contour. The SEM analysis will be defined in a Quality & Reliability Assurance document.

3.6.4 Production Changes

The manufacturer shall advise the procuring activity of the time at which any major change(s) in production or QC methods or documentation become effective during the period of device production for delivery against any given purchase order referencing this specification.

3.7 Workmanship

Integrated circuits shall be manufactured and processed in a careful and workmanlike manner, in accordance with the production processes, workmanship instructions, inspection and test procedures, and training aids prepared by the manufacturer in fulfillment of the reliability assurance program established by paragraph 3.6.

3.7.1 Personnel Certification

The manufacturer shall be responsible for training, testing and certification of personnel involved in producing integrated circuits. Training shall be commensurate and consistent with the requirements of this specification and in conformance to the basic intent of MIL-STD-790. Training aids in the form of satisfactory criteria shall be available for operator and inspector review at any time.

3.7.2 Personnel Evaluation

The supplier shall maintain a continuous evaluation of the proficiency of personnel concerned with production and inspection. Retraining of an operator or inspector shall be required when this evaluation establishes that a degree of proficiency necessary to meet the requirements of this specification is not being exercised.

3.7.3 Rework provisions

3.7.3.1 Rework

All rework on micorcircuits manufactured under this specification shall be accomplished in accordance with paragraph 3.7.1 of MIL-M-38510 as defined herein.

3.7.3.2 Rebonding

Rebonding shall be in accordance with MIL-M-38510, as defined herein (see Note 6.5)

3.8 Performance Capabilities

The integrated circuits delivered to this specification shall be designed to be capable of meeting the environmental requirements specified in Table II. The manufacturer need not perform these tests specifically for the contract or specification, but shall provide data which demonstrates the ability of the integrated circuits to pass the environmental tests. The data shall have been generated on devices from the same generic family as the circuits being supplied to this specification, and the package configuration shall be the same as for the delivered parts (i.e., Flat Pack, TO-100, etc.).

3.9 Quality and Reliability Assurance Program Plan

The manufacturer shall establish and implement a Quality and Reliability Assurance Program Plan that meets the intent of MIL-M-38510, Appendix A. Submission of the program plan to the procuring activity shall not be a requirement of this specification; however, the program plan shall be maintained by the manufacturer and shall be available for review by the procuring activity.

4.0 QUALITY ASSURANCE PROVISIONS

4.1 Responsibility for Inspection

Unless otherwise specified in the contract or purchase order, the manufacturer is responsible for the performance of all inspection requirements specified herein. Except as otherwise specified, the manufacturer may utilize his own facilities or any commercial laboratory acceptable to the procuring activity. The procuring activity may, at its discretion, perform any of the inspections set forth in the specification where such inspections are deemed necessary to assure supplies and services conform to prescribed requirements.

4.1.1 Inspection and Testing Procedures Coverage

Inspection and testing processes and procedures prepared in fulfillment of the reliability assurance program established per paragraph 3.6 shall be prescribed by clear, complete and current instructions. These instructions shall assure inspection and test of materials, work in process and completed integrated circuits as required by this specification. In addition, criteria for approval and rejection of materials and integrated circuits shall be included.

4.1.2 Inspection at Point of Delivery

The procuring activity may, at its discretion, reinspect any or all of the delivered parts excluding Group B and C destructive samples as defined by MIL-STD-883. All parts found to be defective, excluding devices exhibiting damage from use, may be returned to the manufacturer at the manufacturer's expense.

4.1.3 Inspection Records

The manufacturer shall maintain a reliability data and records library. This library shall have on file, for review by the procuring activity, records of examination, qualification test results, variables data (when required) and all other pertinent data generated on devices manufactured to this specification.

4.1.4 Control of Procurement Sources

The manufacturer shall be responsible for assuring that all supplies and services conform to this specification, the detail specification and the manufacturer's procurement requirements.

4.1.4.1 Manufacturer's Receiving Inspection

Purchased supplies shall be subjected to inspection after receipt as necessary to ensure conformance to contract requirements. In selecting sampling plans, consideration shall be given to the controls exercised by the procurement source and evidence of sustained quality conformance.

4.1.4.2 The manufacturer shall provide procedures for withholding from use all incoming supplies pending completion of required tests or receipt of necessary certification or test records and their evaluation.

4.1.4.3 The manufacturer shall initiate corrective action with the procurement source depending upon the nature and frequency of receipt of nonconforming supplies.

4.1.5 Procuring Activity Quality Assurance Representative

The procuring activity, may, at its discretion, place quality assurance representatives in the manufacturer's plant as deemed necessary to assure conformance to contract requirements in any non-proprietary phase of design, fabrication, processing, inspection, and testing of the integrated circuits being produced. The manufacturer shall provide reasonable facilities and assistance for the safety and convenience of such personnel in the performance of their duties. Inspection and test procedures shall be made available for review by the quality assurance representative.

4.2 Qualification and Quality Conformance Inspection

4.2.1 Qualification

Manufacturer's specific device qualification shall be based on compliance with the quality conformance test per Table III for MOS LSI devices. Qualification for other technologies shall be per Table 1 except that the testing will be to one LTPD level tighter than as defined in Table B-I of MIL-M-38510.

4.2.1.2 Procedures and Definitions

4.2.1.2.1 Sampling Procedure

Device selection for the qualification procedure of 4.2.1 shall be based on a random sampling technique and will be selected from a generic family.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

4.2.1.2.2 Generic Family

Electrically and structurally similar devices shall be said to comprise a generic family (e.g., TTL) if they meet the following criteria:

a) Are designed with the same basic circuit-element configuration such as TTL, TTL Schottky, DTL, CMOS, MOS metal-gate, or MOS silicon-gate, and differ only in the number or complexity of specified circuits which they contain. Generic family for linear circuits is defined by circuit function (e.g. op amp, comparator, etc.).

b) Are designed for the same supply, bias and signal voltage, and for input/output capability with each other under an established set of loading rules.

c) Are enclosed in housings (packages) of the same basic construction (e.g., hermetically sealed flat packages, dual-in-line ceramic, dual-in-line plastic) and outline, differing only in the number of active housing terminals included and/or utilized.

4.2.2 Quality Conformance Inspection

Quality conformance inspection group B and C requirements are per Tables I and II, Table II shall apply to MOS LSI and Table I to other technologies.

a) When specifically called out and funded on the purchase order or contract, the manufacturer shall perform the quality conformance inspections (Group B and/or Group C) on a lot-by-lot basis.

b) The manufacturer shall, upon request, make available for review generic quality conformance inspection and data. Data on Group B shall be by package type, number of pins, and assembly location for all subgroups.

Data on Group C, subgroups 1, 2, and 3, shall be by package type, number of pins, and assembly location. Subgroups 4 and 5 by chip generic family in hermetic packages.

4.2.2.1 Lot Acceptance Sampling

Statistical sampling for quality conformance inspections shall be in accordance with MIL-M-38510 Table B-I.

Group B samples, except bond strength samples, shall be selected from sublots that have successfully completed all of the 100% processing steps specified on the applicable process flow chart.

4.2.2.2 Resubmission of Failed Lots

When any lot submitted for quality conformance inspection fails any subgroup requirement, it may be resubmitted a maximum of one time for that particular subgroup. One additional submission is permitted, provided an analysis is performed to determine the failure mechanism for each reject device in the subgroup, and that it is determined that the failures are due to one of the following:

a) Testing error resulting in electrical damage to devices

7

b) A defect that can effectively be removed by rescreening the lot

c) Random defects which do not reflect poor basic device designs or poor workmanship.

4.2.2.3 Early Shipments

When quality conformance inspection is being performed for a specific contract or purchase order, the accepted Group A devices that are awaiting shipment pending successful completion of Group B and/or Group C, shall be stored in the Quality Assurance test area. Under no circumstances shall such parts be shipped prior to the successful completion of the Group B tests.

4.2.2.4 Groups B and C Test Data

All lot-by-lot data generated by Group B and/or Group C testing when specifically called out and funded on the purchase order, shall accompany the initial shipment of devices. This data shall consist, at a minimum, of the following:

a) Attributes data for Group B. Endpoints for the subgroups are visual per the applicable MIL-STD-883 test method.

b) Attributes data for Group C subgroups 1, 2, 4 and 5. Endpoints for these subgroups shall be per Table I and II.

4.2.2.5 Precedure in Case of Test Equipment Failure or Operator Error

Where an integrated circuit is believed to have failed as a result of faulty test equipment or operator error, the failure shall be entered in the test record which shall be retained for review along with a complete explanation verifying why the failure is believed to be invalid. If it is determined that the failure is invalid, a replacement integrated circuit from the same inspection lot may be added to the sample. The replacement integrated circuit shall be subjected to all those tests to which the discarded integrated circuit was submitted prior to its failure, and any remaining specified test to which the discarded integrated circuit was not subjected prior to its failure.

4.3 Quality Assurance Processing, Methods and Procedures

This section establishes the test methods and conditions to be used for the 100% processing (screening) requirements specified by the applicable process flow chart.

4.3.1 Precap Visual Inspection

Each microcircuit shall be required to pass the appropriate precap visual inspection defined as follows. Precap Lot Acceptance shall be per paragraph 4.6.

4.3.1.1 38510 Class C (Level I) and 38510 Class (Level III) devices shall be visually inspected in accordance with MIL-STD-883, Method 2010, Condition B.

4.3.1.2 38510A (Level IV) devices (designated for NASA type applications) shall be visually inspected in accordance with MIL-STD-883, Method 2010, Condition A. (See notes 6.1.1.1 and 6.1.1.2).

4.3.1.3 Complex MSI and LSI circuits as defined in MIL-STD-883, Method 5004, paragraph 3.3 may be precap inspected per MIL-STD-883, Method 5004, paragraph 3.3.1 for 38510 Class B (Level III) and paragraph 3.3.2 for 38510 Class C (Level I).

4.3.2 Stabilization Bake

The purpose of this test is to determine the effect on microelectronic devices of baking at elevated temperatures without electrical stress applied. Test shall be performed in accordance with MIL-STD-883, Method 1008, Condition C.

4.3.3 Thermal Shock

The purpose of this test is to determine the resistance of the device to sudden exposure to extreme changes in temperature. Test shall be performed in accordance with MIL-STD-883, Method 1011.1, Condition A.

4.3.4 Temperature Cycle

This test is conducted for the purpose of determining the resistance of a part to exposures to extremes of high and low temperatures, and to the effect of alternate exposures to these extremes, such as would be experienced when equipment or parts are transferred to and from heated shelters in arctic areas. Test shall be performed in accordance with MIL-STD-883, Method 1010, Condition C, minimum of 10 cycles. For MSI and LSI complex devices as defined in MIL-STD-883, Method 5004, paragraph 3.3, 50 cycles may be used in lieu of alternate pre-cap visual inspection criteria.

4.3.5 Mechanical Shock

The shock test is intended to determine the suitability of the devices for use in electronic equipment which may be subjected to moderately severe shocks as a result of suddenly applied forces or abrupt changes in motion produced by rough handling, transportation, or field operation. Test shall be performed in accordance with MIL-STD-883, Method 2002, Condition B, five blows minimum.

4.3.6 Centrifuge (Constant Acceleration)

The centrifuge test is used to determine the effects on microelectronics devices of a centrifugal force. This test is designed to indicate structural and mechanical weaknesses not necessarily detected in shock and vibration tests. Test shall be performed in accordance with MIL-STD-883, Method 2002, Condition E for devices having less than 20 pins and Condition D for those having more than 20 pins.

4.3.7 Fine Leak Test

Each integrated circuit for 38510 Class C (Level I), 38510 Class B (Level III), and 38510 Class A (Level IV) screens shall be subject to a fine leak test in accordance with paragraph 4.3.7.1 or 4.3.7.2. The method shall be optional providing it is consistent with and capable of detecting the specified leak rate of the applicable process flow chart.

4.3.7.1 Helium Leak Test

Helium leak test shall be performed in accordance with MIL-STD-883, Method 1014, Condition A.

4.3.7.2 Radiflo Leak Test

Radiflo leak test shall be performed in accordance with MIL-STD-883, Method 1014, Condition B. Krypton 85 bomb pressure and dwell time are a function of the radioactivity level and shall be selected so as to conform to the equations given in Condition B.

4.3.8 Gross-Leak Test

Each integrated circuit for 38510 Class C (Level I), 38510 Class B, (Level III) and 38510 Class A (Level IV) screens shall be subjected to the appropriate gross-leak test of paragraph 4.3.8.1 or 4.3.8.2, or an approved equivalent. The manufacturer may, at his option, perform gross-leak testing after the Set I Electrical Tests of paragraph 4.3.9.

4.3.8.1 When specifically called out and funded on the purchase order or contract, units will be bombed 2 hours minimum at 30 psig in FC-78, or equivalent. Units will then be immersed in FC-40 or equivalent at +125°C ±5°C for 30 seconds minimum and observed for for a definite stream of bubbles, more than two large bubbles, or an attached bubble that grows in size, per MIL-STD-883, Method 1014, Condition C2.

7

4.3.8.2 Units will be immersed in FC-40 or equivalent at +25°C ± 5°C for 30 seconds minimum and observed for a definite stream of bubbles, more than two large bubbles or an attached bubble that grows in size, per MIL-STD-883, Method 1015, Condition C1,.

4.3.9 Final Electrical Test (Set I)

Each integrated circuit shall be required to pass the electrical requirements of the data sheet. The manufacturer shall also perform such additional testing necessary to assure the parts will meet the temperature extreme limits. MOS LSI memory devices will be 100% dc and ac tested both at 25°C and at high temperature.

When specifically called out and funded on the purchase order or contract, the manufacturer shall perform subgroups 2, 3, and 4 of paragraph 4.4 in accordance with Method 5004 of MIL-STD-883.

4.3.10 Burn-In

The burn-in screen is performed for the purpose of eliminating marginal devices and early-life failures evidenced as time and stress dependent. Test shall be in accordance with MIL-STD-883, Method 1015, Condition A, D, or E at 125 ± 5°C for digital circuits and Conditions A, B, C, or D for linear circuits. 38510 Class B (Level III) MSI and LSI complex devices, as defined in MIL-STD-883, paragraph 3.3.1, may receive a 240-hour-minimum burn-in in lieu of alternate precap visual inspection criteria per MIL-STD-883, Method 5004, paragraph 3.3.1.

4.3.11 Final Electrical Test (Set II)

Each 38510 Class A (Level IV) integrated circuit shall be required to pass the electrical requirements of the detail specifications. The following tests shall be performed as a minimum: dc parameters at maximum and minimum rated temperatures, and switching parameters at 25°C. In addition, each bipolar device shall have critical 25°C dc electrical parameters read and recorded by serial number and shall pass the following delta requirements:

PARAMETER	DELTA LIMIT
V_{OL}	±10% of detail specification limit
V_{OH}	±10% of detail specification limit
I_{IL}	±10% of detail specification limit
I_{IH}	±10% of detail specification limit

CMOS recorded parameters and delta limits will be defined by the manufacturer as required.

One copy of the pre-burn-in and post-burn-in recorded data with delta calculations shall be shipped with each lot. Data will not be available for the metal flat pack (T). See MIL-M-38510, Class S. The manufacturer may, when deemed necessary, elect to perform additional electrical testing over and above the requirements stated herein.

4.3.12 Radiographic Inspection (X-ray)

Test shall be performed in accordance with MIL-STD-883, Method 2012. X-ray may be performed at any point after serialization at the manufacturer's option. (see note 6.3).

4.3.13 External Visual Inspection

The purpose of this examination is to verify that materials, construction, marking, and general workmanship are as specified. Examination shall be in accordance with MIL-STD-883, Method 2009.

4.3.14 Voltage Stress

Selected n-channel MOS LSI devices will be voltage stressed for 40 hours minimum at 25°C min per MIL-STD-883 Method 10155, Condition D.

4.4 Group A Conformance

Group A conformance shall consist of the electrical parameters in the manufacturer's data sheet. If an inspection lot is made up of a collection of sublots, each sublot shall conform to Group A, as specified.

SUBGROUP	LTPD (%)			
	LEVEL I 38510C	LEVEL II	LEVEL III 38510B	LEVEL IV 38510A
Subgroup 1 25°C, dc	5	7	5	5
Subgroup 2 High Temperature, dc	10	10	7	5
Subgroup 3 Low Temperature, dc	10	10	7	5
Subgroup 4 Dynamic and Switching Tests @ 25°C	10	10	7	5

NOTE: Functional tests included in dc tests.

4.5 Certification

The manufacturer shall include a certificate of compliance with each shipment of parts if requested on the purchase order. This certificate shall indicate that all specified tests and requirements of this specification have been made or met, and that the lot of devices (identified by lot and/or batch number) is acceptable. The certificate shall bear the name and signature of the manufacturer's Quality Control representative, the date of acceptance or signing, and any pertinent notes as applicable.

7

4.6 Precap Lot Acceptance

After each precap inspection the lot of devices shall be sampled by quality control and inspected for the specified visual criteria.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TABLE I
QUALITY CONFORMANCE TEST (GROUP B/GROUP C)

TEST	MIL-STD-883 METHOD	CONDITIONS	LTPD LEVEL IV 38510A	LTPD LEVEL III 38510B	LTPD LEVEL I 38510C
Subgroup 1[2]					
Physical Dimensions	2016		19	15	20
Subgroup 2[2]					
Marking Permanency	2015				
Visual and Mechanical	2014				
Bond Strength[1]	2011	Condition C or D 2 grams for Au bonds 1.5 grams for Al bonds	10	15	20
Subgroup 3[2]					
Solderability	2003	Omit Aging	10	15	15
Subgroup 4[2]					
Lead Fatigue	2004	Conditions B_2			
Fine Leak	1014	Conditions A or B, per para. 4.3.7 of this spec.			
Gross Leak	1014	Condition C, per para. 4.3.8 of this spec.	10	15	15
		GROUP C			
Subgroup 1					
Thermal Shock	1011	Condition B			
Temp. Cycle	1010	Condition C			
Moisture Resistance	1004	Omit Initial Cond.			
Fine Leak	1014	Conditions A or B, per para 4.3.7 herein			
Gross Leak	1014	Condition C, per para. 4.3.8 herein	10	15	15
Electrical End Points	5005	Subgroups 1, 2, 3, and 7			
Subgroup 2					
Mechanical Shock	2002	Condition B			
Vibration Variable Freq.	2007	Condition A			
Constant Acceleration	2001	Condition E[3]			
Fine Leak	1014	Conditions A or B, per para. 4.3.7 herein			
Gross Leak	1014	Condition C, per para. 4.3.8 herein	10	15	15
Electrical End Points	5005	Subgroups 1, 2, 3, and 7			
Subgroup 3					
Salt Atmosphere	1009	Condition A Omit Initial Conditioning	10	15	15
Subgroup 4					
High Temp Storage	1008	150°C, 1000 Hrs.			
Electrical End Points	5005	Subgroups 1, 2, 3, and 7	7	7	7
Subgroup 6					
Operating Life Test	1005	125°C, 1000 Hrs. Minimum			
Electrical End Points	5005	Subgroups 1, 2, 3, and 7	5	5	5

1. Bond strength test may be performed on samples randomly selected immediately following internal visual prior to sealing.
2. Visual and/or hermetic end points; hence, electrical or visual rejects may be used. Reference MIL-STD-883, Method 5005.2, para. 3.4.
3. Condition D for packages with 20 pins or more. Condition E for packages with less than 20 pins.

7

TABLE II
QUALITY CONFORMANCE TEST
MOS LSI CIRCUIT

TEST	MIL-STD-883 METHOD	CONDITIONS	LTPD
Subgroup 1			
Temperature Cycle	1001	Condition C	
Constant Acceleration	2001	Condition D[1], Y_1 Plane	
Electrical End Points	5005	Subgroup 1	15
Subgroup 2			
Operating Life	1005	Condition D, 500 Hrs. Minimum	
Electrical End Points	5005	Subgroup 1	10

1. Condition D for packages with 20 pins or more. Condition E for packages with less than 20 pins.

TABLE III
MANUFACTURERS QUALIFICATION PROCEDURE
MOS LSI CIRCUITS

TEST	MIL-STD-883 METHOD	CONDITIONS	LTPD
Subgroup 1[1]			
Physical Dimensions	2016		15
Visual and Mechanical	2014		
Subgroup 2[1]			
Solderability	2003	Omit Aging	15
Subgroup 3[2]			
Thermal Shock	1011	Condition B	
Temperature Cycling	1010	Condition C	
Moisture Resistance	1004	Omit Initial Conditioning	
Electrical End Points	5005	Subgroup 1	15
Subgroup 4[2]			
Mechanical Shock	2002	Condition B	
Vibration Variable Freq.	2007	Condition A	
Constant Acceleration	2001	Condition E[3]	
Electrical End Points	5005	Subgroup 1	15
Subgroup 5[1]			
Lead Fatigue	2004	Condition B2	
Fine Leak	1014	Condition A or B Per Para. 4.3.7 Herein	
Gross Leak	1014	Condition C2 Per Para. 4.3.7 Herein	15
Subgroup 6[1]			
Salt Atmosphere	1009	Condition A, Omit Initial Conditioning	15
Subgroup 7[2]			
Storage Life	1008	150°C, 1000 Hrs. Minimum	
Electrical End Points	5005	Subgroup 1	7
Subgroup 8[2]			
Operating LIfe	1005	85°C, 1000 Hrs. Minimum	
Electrical End Points	5005	Subgroup 1	10
Subgroup 9[1]			
Bond Strength	2011	Condition B, D	10 devices not greater than 1% defective

1. Visual and/or hermetic end points; hence, electrical rejects may be used. Reference MIL-STD-883, Method 5005.2, Para. 3.4.
2. Electrical end points only.
3. Condition D for packages with 20 pins or more. Condition E for packages with less than 20 pins.

7

5.0 PREPARATION FOR DELIVERY

5.1 Final Visual Shipping Inspection

Each lot of microcircuits and its associated documentation shall be sampled by Quality Control and visually inspected for the following:

a) Scratched, nicked or bent leads

b) Damaged header (packages)

c) All test data specified in section 4.0

d) Certificate of Compliance as specified in section 4.0

e) All other pertinent documentation required and specified by this specification.

5.2 Packing Requirements

Parts shall be packed in containers of the type, size, and kind commonly used which will ensure acceptance by common carriers and safe delivery at the destination and in accordance with MIL-M-55565, Level C, bulk pack. The containers shall be clearly marked with manufacturer's name or symbol.

5.3 Preservation and Package Identification

The package shall be marked with the following:

The country of origin if other than U.S.A.

Procuring activity parts number

Purchase order number

Material nomenclature

Quantity

Lot number

Date code

This information shall appear on the label or shall be directly marked on each container. Method is optional.

6.0 NOTES

6.1 Precap Visual Method 2010

The following criteria may be in conflict with the circuit design topology and construction techniques of some microcircuit manufacturers. Where such a conflict does exist, the inspection criteria listed herein may be waived. (Reference paragraph 3.0 of MIL-STD-883, Method 2010).

6.1.1 Preseat Visual Inspection, Test Condition B [38510 Class B (Level III) and 38510 Class C (Level I)].

6.1.1.1 Paragraph 3.2: a 20-PSI minimum blow-off prior to seal will be performed to meet the intent of a controlled environment.

6.1.1.2 For titanium-tungsten, gold, titanium-tungsten multilayered systems, the underlying metal is defined as the bottom titanium tungsten and the top layer is defined as gold.

6.2 Interconnections

Circuit interconnections (metallization pattern) shall be designed so that no properly fabricated connection shall experience a current density greater than 5 X 10^5 amperes/cm^2, including allowances for worst-case conductor composition, normal production tolerances on design dimensions, and nominal thickness at critical areas such as contact windows.

6.3 X-Ray Method 2012

Paragraph 3.9.2.2a(2) and (3) delete and replace with: "Cause for rejection shall be a single void in the bar attachment material opening two adjacent sides and exceeding 50% of the length of one side and 100% of the length of the other side."

6.4 Salt Atmosphere Test, Method 1009

Where package design considerations necessitate (such as 0.75-inch tip-to-tip metal flat packs), there may be a conformal coating applied prior to the salt atmosphere test.

6.5 Rebonding

Attempts to bond where only impressions have been made in the metal and where the bond did not make a physical attachment to the pad or post shall not be considered evidence of rebonding.

JAN MIL-M-38510 Integrated Circuits

8

JAN MIL-M-38510 INTEGRATED CIRCUITS

The MIL-M-38510 JAN Program implemented by Texas Instruments provides a standardized qualification and specification system for high-reliability military applications. The program covers a wide range of monolithic integrated circuits including digital and linear device types in both dual-in-line and flat pack configurations. For device types not yet covered by MIL-M-38510 JAN slash sheets or for cost-effectivity and improved availability, the Texas Instruments 38510/MACH IV Program is recommended. It includes all the significant and practical controls, lot acceptances, and screenings included in the MIL-M-38510 JAN Program and is available at approximately one-third of the cost. The 38510/MACH IV Program includes a controlled procurement document encompassing general specifications MIL-M-38510A and MIL-STD-883A dated 15 November 1974. Revision D of the TI 38510/MACH IV specification is included in Tab Section 7 of this book.

The TI 38510/MACH IV Program also offers an aid to specification writing by providing a cost-effective 38510 and 883 base document, whereby special device program specifications may be written invoking any additional testing options unique to a specific program. The TI 38510/MACH IV specification is organized and written per MIL-STD-100 to allow its use as a program specification by merely adding the user's company name and drawing number, as well as any required additions or deletions necessary to meet the specific program goals.

Table I provides a convenient cross-reference from the JAN part numbers to the corresponding standard catalog part numbers. The cross reference from the catalog numbers to the JAN slash sheet numbers is provided in Table II.

The complete JAN part number with the tables of class, case, and lead finish codes is given in Table III, along with a cross reference to the TI 38510/MACH IV part number. A table of standard TI cases and lead finishes is also provided to assist in specifying the proper JAN part number. It is imperative that the proper case and lead finish shown in the table be specified on the parts list and procurement documentation. The specific package for each device is determined by referring to the proper data sheet.

The following figure defines the reliability classes of MIL-M-38510 JAN and TI 38510/MACH IV ICs, and the intended areas of application. MIL-M-38510 recommends that for original equipment complements, the device class appropriate to the need be used, while Class B is recommended for spare parts for logistic support.

RECOMMENDED USE	TYPICAL SYSTEM APPLICATIONS	MIL-STD-883 MIL-M-38510 CLASS	38510/MACH IV LEVEL
Where repair or replacement is readily accomplished and "down time" is not critical	Prototype, noncritical support or ground systems	Class C	I (SNM)
Where repair or replacement is difficult or impossible and reliability is vital	Avionics and tactical missile systems	Class B	III (SNC)
Where repair or replacement is difficult or impossible and reliability is imperative	Critical avionics, space and strategic missile systems	Class A/S	IV (SNH)

Wide acceptance of TI 38510/MACH IV Class B "SNC" level devices has made possible improved availability thru distributor and factory stocking programs. The following military documents (see Note 1) establish the processing, quality, and reliability assurance requirements for JAN integrated circuits. The detail requirements of each individual JAN device are specified in the slash sheets.

MIL-M-38510/XXX, Microcircuits, Digital, TTL, . . ., . . ., Monolithic Silicon (Slash Sheets)
MIL-M-38510A, Microcircuits, General Specification for
MIL-STD-883A, Test Methods and Procedures for Microelectronics
QPL-38510, Qualified Products List for MIL-M-38510

NOTE 1: Copies of these documents may be requested from the Naval Pulbications and Forms Center, 5801 Tabor Avenue, Philadelphia, Pa. 19120.

TABLE I. JAN INTEGRATED CIRCUITS AND CIRCUIT-TYPE CROSS-REFERENCE

JAN /NO.	CKT TYPE	JAN /NO.	CKT TYPE	JAN /NO.	CKT TYPE	JAN /NO.	CKT TYPE
00101	5430	01401	54150	04001	54H50	07501†	54S86
00102	5420	01402	9312‡	04002	54H51	07502†	54S135
00103	5410	01403	54153	04003	54H53	07601†	54S194
00104	5400	01404	9309	04004	54H54	07602†	54S195
00105	5404	01405	54157	04005	54H55	07701†	54S138
00106	5412	01406†	54151	04101	54L51	07702†	54S139
00107	5401	01501	5475	04102	54L54	07703†	54S280
00108	5405	01502	5477	04103	54L55	07801†	54S181
00109	5403	01503	54116	04104♦	54L54	07802†	54S182
00201	5472	01504	9314‡	04201	54L121	07901†	54S151
00202	5473	01601	5408	04202	54L122	07902†	54S153
00203	54107	01602	5409	05001	4011A	07903†	54S157
00204	5476	01701	54174	05002	4012A	07904†	54S158
00205	5474	01702	54175	05003	4023A	07905†	54S251
00206	5470	01703†	54173	05101	4013A	07906†	54S257
00207	5479‡	01801†	54170	05102	4027A	07907†	54S258
00301	5440	01901†	54180	05201	4000A	08001†	54S11
00302	5437	02001	54L30	05202	4001A	08002†	54S15
00303	5438	02002	54L20	05203	4002A	08101†	54S140
00401	5402	02003	54L10	05204	4025A	08201†	54S85
00402	5423	02004	54L00	05301	4007A	10101	52741
00403	5425	02005	54L04	05302	4019A	10102	52747
00404	5427	02006	54L01/54L03	05303	4030A	10103	52101A
00501	5450	02101	54L71	05401	4008A	10104	52108A
00502	5451	02102	54L72	05501	4009A	10105†	LH2101A
00503	5453	02103	54L73	05502	4010A	10106†	LH2108A
00504	5454	02104	54L78	05503	4049A	10201	52723
00601	5482	02105	54L74	05504	4050A	10202†	52104
00602	5483	02201	54H72	05601	4017A	10203†	52105
00603	9304‡	02202	54H73	05602	4018A	10301	52710
00701	5486	02203	54H74	05603	4020A	10302	52711
00801	5406	02204	54H76	05604	4022A	10303	52106
00802	5416	02205	54H101	05605	4024A	10304	52111
00803	5407	02206	54H103	05701	4006A	10401	55107
00804	5417	02301	54H30	05702	4014A	10402	55108
00805	5426	02302	54H20	05703	4015A	10403	55114
00901	5495	02303	54H10	05704	4021A	10404	55115
00902	5496	02304	54H00	05705	4031A	10405	55113
00903	54164	02305	54H04	05706†	4035A	10406†	7831
00904	54165	02306	54H01	05707†	4034A	10501†	52733
00905	54194	02307	54H22	05801†	4016A	10601	LM102‡
00906	54195	02401	54H40	06001	10501‡	10602	52110
00907†	9300‡	02501	54L90	06002	10502‡	10701	52109
00908†	9328	02502	54L93	06003	10505‡	10801†	3018A
00909†	54198	02503†	54L193	06004	10506‡	10802†	3045
00910†	54166	02504†	93L10	06005	10507‡	15001	5485
01001	5442	02505†	93L16	06006	10509‡	15101	5413
01002	5443	02601	54L86	06101†	10531‡	15102	5414
01003	5444	02701	54L02	06102†	10631‡	15103	54132
01004	5445	02801	54L95	06103†	10576‡	15201†	54154
01005	54145	02802	54L164	06104†	10535‡	15202†	54155
01006	5446	02803	93L28‡	07001	54S00	15203†	54156
01007	5447	02804	93L00	07002	54S03	15204†	8250
01008	5448	02805	76L70	07003	54S04	15205†	8251
01009	5449	02806♦	54L91	07004	54S05	15206†	8252
01101	54181	02901	54L42	07005	54S10	15301†	54125
01102	54182	02902	54L43	07006	54S20	15302†	54126
01201	54121	02903	54L44	07007	54S22	15501†	54H08
01202	54122	02904	54L46	07008	54S30	15502†	54H11
01203	54123	02905	54L47	07009	54S133	15601†	54147
01301	5492	02906	76L42A	07010	54S134	15602†	54148
01302	5493	03001	15930	07101	54S74	15801†	9321
01303	54160	03002	15935	07102	54S112	15802†	9301
01304	54163	03003	15936	07103	54S113	15803†	9311
01305	54162	03004	15946	07104	54S114	15804†	9317
01306	54161	03005	15962	07105	54S174	20101	54186 (PROM 512)
01307	5490	03101	15932	07106	54S175	20102	MCM5304‡
01308	54192	03102	15944	07201	54S40	20103†	IM5603A
01309	54193	03103	15957	07301	54S02	20201†	54S387 (PROM 1024)
01310†	54196	03104	15958	07401	54S51	20202†	IM5623
01311†	54197	03105	15933	07402	54S64	23001†	5531 (256 RAM)
01312†	54177	03501	MH0026	07403	54S65	23002†	93410 (256 RAM)

NOTE: Only the basic JAN and SN numbers are shown. Complete the numbers as shown in Table III.
†Slash sheets not released as of date of this publication.
‡Not recommended for new designs.
♦Class S only.

JAN MIL-M-38510 INTEGRATED CIRCUITS

TABLE I. JAN INTEGRATED CIRCUITS AND CIRCUIT-TYPE CROSS-REFERENCE

JAN /NO.	CKT TYPE	JAN /NO.	CKT TYPE	JAN /NO.	CKT TYPE	JAN /NO.	CKT TYPE
23501†	TMS4060 (4K RAM)	30109†	54LS109	30701†	54LS138	31202†	54LS283
23502†	TMS4050 (4K RAM)	30201†	54LS40	30702†	54LS139	31301†	54LS13
30001†	54LS00	30202†	54LS37	30703†	54LS42	31302†	54LS14
30002†	54LS03	30203†	54LS38	30704†	54LS47	31303†	54LS132
30003†	54LS04	30301†	54LS02	30801†	54LS181	31401†	54LS123
30004†	54LS05	30302†	54LS27	30901†	54LS151	31402†	54LS221
30005†	54LS10	30303†	54LS266	30902†	54LS153	31501†	54LS90
30006†	54LS12	30401†	54LS51	30903†	54LS157	31502†	54LS93
30007†	54LS20	30402†	54LS54	30904†	54LS158	31503†	54LS160
30008†	54LS22	30501†	54LS32	30905†	54LS251	31504†	54LS161
30009†	54LS30	30502†	54LS86	30906†	54LS257	31505†	54LS168
30101†	54LS73	30601†	54LS194	30907†	54LS258	31506†	54LS169
30102†	54LS74	30602†	54LS195	30908†	54LS253	31507†	54LS192
30103†	54LS112	30603†	54LS95	31001†	54LS11	31508†	54LS193
30104†	54LS113	30604†	54LS96	31002†	54LS15	31601†	54LS75
30105†	54LS114	30605†	54LS164	31003†	54LS21	31602†	54LS279
30106†	54LS174	30606†	54LS298	31004†	54LS08	31701†	54LS124
30107†	54LS175	30607†	54LS395	31101†	54LS85	31702†	54LS324
30108†	54LS107	30608†	54LS670	31201†	54LS83A	31801†	54LS261

TABLE II. CIRCUIT-TYPE AND JAN INTEGRATED CIRCUITS CROSS-REFERENCE

CKT TYPE	JAN /NO.	CKT TYPE	JAN /NO.	CKT TYPE	JAN /NO.	CKT TYPE	JAN /NO.
LH2101A	10105†	4016A	05801†	54H72	02201	54LS114	30105†
LH2108A	10106†	4017A	05601	54H73	02202	54LS123	31401†
LM102	10601	4018A	05602	54H74	02203	54LS124	31701†
MCM5304‡	20102	4019A	05302	54H76	02204	54LS132	31303†
MH0026	03501	4020A	05603	54H101	02205	54LS138	30701†
TMS4050	23502 (4K RAM)	4021A	05704	54H103	02206	54LS139	30702†
TMS4060	23501 (4K RAM)	4022A	05604	54LS00	30001†	54LS151	30901†
1M5600	20103	4023A	05003	54LS02	30301†	54LS153	30902†
1M5603A	20103†	4024A	05605	54LS03	30002†	54LS157	30903†
1M5623	20202†	4025A	05204	54LS04	30003†	54LS158	30904†
10501‡	06001	4027A	05102	54LS05	30004†	54LS160	31503†
10502‡	06002	4030A	05303	54LS08	31004†	54LS161	31504†
10505‡	06003	4031A	05705	54LS10	30005†	54LS164	30605†
10506‡	06004	4034A	05706†	54LS11	31001†	54LS168	31505†
10507‡	06005	4035A	05707†	54LS12	30006†	54LS169	31506†
10509‡	06006	4049A	05503	54LS13	31301†	54LS174	30106†
10531‡	06101†	4050A	05504	54LS14	31302†	54LS175	30107†
10535‡	06104†	52101A	10103	54LS15	31002†	54LS181	30801†
10576‡	06103†	52104	10202†	54LS20	30007†	54LS192	31507†
10631‡	06102†	52105	10203†	54LS21	31003†	54LS193	31508†
15930	03001	52106	10303	54LS22	31008†	54LS194	30601†
15932	03101	52108A	10104	54LS27	30302†	54LS195	30602†
15933	03105	52109	10701	54LS30	30009†	54LS221	31402†
15935	03002	52110	10602	54LS32	30501†	54LS251	30905†
15936	03003	52111	10304	54LS37	30202†	54LS253	30908†
15944	03102	52710	10301	54LS38	30203†	54LS257	30906†
15946	03004	52711	10302	54LS40	30201†	54LS258	30907†
15957	03103	52723	10201	54LS42	30703†	54LS261	31801†
15958	03104	52733	10501†	54LS47	30704†	54LS266	30303†
15962	03005	52741	10101	54LS51	30401†	54LS279	31602†
3018A	10801†	54H00	02304	54LS54	30402†	54LS283	31202†
3045	10802†	54H01	02306	54LS73	30101†	54LS298	30606†
4000A	05201	54H04	02305	54LS74	30102†	54LS324	31702†
4001A	05202	54H08	15501†	54LS75	31601†	54LS395	30607†
4002A	05203	54H10	02303	54LS83A	31201†	54LS670	30608†
4006A	05701	54H11	15502†	54LS85	31101†	54L00	02004
4007A	05301	54H20	02302	54LS86	30502†	54L01	02006
4008A	05401	54H22	02307	54LS90	31501†	54L02	02701
4009A	05501	54H30	02301	54LS93	31502†	54L03	02006
4010A	05502	54H40	02401	54LS95	30603†	54L04	02005
4011A	05001	54H50	04001	54LS96	30604†	54L10	02003
4012A	05002	54H51	04002	54LS107	30108†	54L20	02002
4013A	05101	54H53	04003	54LS109	30109†	54L30	02001
4014A	05702	54H54	04004	54LS112	30103†	54L42	02901
4015A	05703	54H55	04005	54LS113	30104†	54L43	02902

NOTE: Only the basic JAN and SN numbers are shown. Complete the numbers as shown in Table III.
†Slash sheets not released as of date of this publication.
‡Not recommended for new designs.

TABLE II. CIRCUIT-TYPE AND JAN INTEGRATED CIRCUITS CROSS-REFERENCE

CKT TYPE	JAN /NO.	CKT TYPE	JAN /NO.	CKT TYPE	JAN /NO.	CKT TYPE	JAN /NO.
54L44	02903	54S140	08101†	5447	01007	54164	00903
54L46	02904	54S151	07901†	5448	01008	54165	00904
54L47	02905	54S153	07902†	5449	01009	54166	00910†
54L51	04101	54S157	07903†	5450	00501	54173	01703†
54L54	04102, 04104♦	54S158	07904†	5451	00502	54174	01701
54L55	04103	54S174	07105	5453	00503	54175	01702
54L71	02101	54S175	07106	5454	00504	53177	01312†
54L72	02102	54S181	07801†	5470	00206	54180	01901†
54L73	02103	54S182	07802†	5472	00201	54181	01101
54L74	02105	54S194	07601†	5473	00202	54182	01102
54L78	02104	54S195	07602†	5474	00205	54186	20101
54L86	02601	54S251	07905†	5475	01501	54192	01308
54L90	02501	54S257	07906†	5476	00204	54193	01309
54L91	02806♦	54S258	07907†	5477	01502	54194	00905
54L93	02502	54S280	07703†	5479‡	00207	54195	00906
54L95	02801	54S387	20201†	5482	00601	54196	01310
54L121	04201	5400	00104	5483	00602	54197	01311†
54L122	04202	5401	00107	5485	15001	54198	00909†
54L164	02802	5402	00401	5486	00701	5531	23001† (256 RAM)
54L193	02503†	5403	00109	5490	01307	55107	10401
54S00	07001	5404	00105	5492	01301	55108	10402
54S02	07301†	5405	00108	5493	01302	55113	10405
54S03	07002	5406	00801	5495	00901	55114	10403
54S04	07003	5407	00803	5496	00902	55115	10404
54S05	07004	5408	01601	54107	00203	76L42A	02906
54S10	07005	5409	01602	54116	01503	76L70	02805
54S11	08001†	5410	00103	54121	01201	7831	10406†
54S15	08002†	5412	00106	54122	01202	8250	15204†
54S20	07006	5413	15101	54123	01203	8251	15205†
54S22	07007	5414	15102	54125	15301†	8252	15206†
54S30	07008	5416	00802	54126	15302†	93L00	02804
54S40	07201	5417	00804	54132	15103	93L10	02504†
54S51	07401	5420	00102	54145	01005	93L16	02505†
54S64	07402	5423	00402	54147	15601†	93L28‡	02803
54S65	07403	5425	00403	54148	15602†	9300‡	00907†
54S74	07101	5426	00805	54150	01401	9301‡	15802†
54S85	08201	5427	00404	54151	01406†	9304‡	00603
54S86	07501†	5430	00101	54153	01403	9308	01503
54S112	07102	5437	00302	54154	15201†	9309	01404
54S113	07103	5438	00303	54155	15202†	9311	15803†
54S114	07104	5440	00301	54156	15203†	9312‡	01402
54S133	07009	5442	01001	54157	01405	9314‡	01504
54S134	07010	5443	01002	54160	01303	9317	15804†
54S135	07502†	5444	01003	54161	01306	9322	01405
54S138	07701†	5445	01004	54162	01305	9328	00908
54S139	07702†	5446	01006	54163	01304	93410	23002 (266 RAM)

NOTE: Only the basic JAN and SN numbers are shown. Complete the numbers as shown in Table III.
†Slash sheets not released as of date of this publication.
‡Not recommended for new designs.
♦Class S only.

8

TABLE III. TI JAN AND 38510/MACH IV INTEGRATED CIRCUITS

JAN P/N → JAN M38510 / 001 01 B C B

38510/MACH IV P/N → †SN C 5430 J 00

CLASS	
JAN	†38510/ MACH IV
A/S*	H
B	C
C	M

CIRCUIT TYPE
See Cross Reference Tables I & II

CASE OUTLINE (SEE BLOCK A)			
JAN	PACKAGE	38510 (APP.C)	38510/ MACH IV
A	1/4" X 1/4" FLAT-14	F-1	FA
B/T*	1/4" X 1/8" FLAT-14	F-3	T
C	DIP-14	D-1	J
D	1/4" X 3/8" FLAT-14	F-2	W
E	DIP-16	D-2	J
F	1/4" X 3/8" FLAT-16	F-5	W/SB
G	TO-99	A-1	L
H	1/4" X 1/4" FLAT-10	F-4	U
I	TO-100	A-2	L
J	DIP-24	D-3	J
K	3/8" X 5/8" FLAT-24	F-6	W
L	3/8" X 1/2" FLAT-24	F-7	W
‡	DIP-22	‡	J
‡	DIP-18	‡	J
X	TO-5	–	–
Y	TO-3	–	–
Z	1/4" X 3/8" FLAT-24	F-8	–

LEAD FINISH (SEE BLOCK A)		
JAN	TYPE	38510/ MACH IV
A	SOLDER DIP	10
B	TIN-PLATE	00
C	GOLD-PLATE	00

BLOCK A												
JAN CASE OUTLINE & FINISH FOR TI FAMILIES												
PRODUCT	A	B	C	D	E	F	G	I	J	L		
SERIES 54			X	X	X	X			X	X		
SERIES 54H			X	X	X	X						
SERIES 54L		X										
SERIES 54LS			X	X	X	X			X	X		
SERIES 54S			X	X	X	X			X	X		
SERIES 52	X		X				X	X				
SERIES 55	X		X		X	X						
†SERIES 4000 (CMOS)			X	X	X	X						
†MOS LSI											X	X
LEAD FINISH A												
LEAD FINISH B			X	X	X	X			X	X	X	X
LEAD FINISH C	X	X					X	X				

NOTES:

1. Complete the 38510/MACH IV number by adding prefix for class, and suffixes for case outline and lead finish to the basic circuit type number as shown above.

   Example:
   SNC5430J-00

2. Complete the JAN number by adding a three letter suffix for class, case outline, and lead finish as shown above.

   Example:
   JAN M38510/00101BCB

†Prefix designation for Class B 38510/MACH-IV for CMOS is "TFC" and for MOS LSI is "SMC".
‡Unassigned.
*Per MIL-M-0038510B.

8

IC Sockets and Interconnection Panels

9

IC SOCKETS AND INTERCONNECTION PANELS

Texas Instruments lines of off-the-shelf interconnection products are designed specifically to meet the performance needs of volume commercial applications. They provide both the economy of a standard product line and performance features developed after many year's experience with custom designs. Foremost among these is our ability to selectively bond a wrought gold stripe at the contact point. No waste. Reduced cost. Reliable contacts.

Wrought Gold Contact

Plate a contact with gold and you get a better contact. More reliable, longer lasting. Increase the gold, you improve the contact. But gold is precious, so improved performance has to be costly – right? Wrong. Because now you can get the gold only where it is needed – at the point of contact.

How? With selective metallurgical bonding; a gold stripe inlay. Not porous plating, but durable wrought gold bonded to the contact by the same technology used to produce clad coins and thermostat metals.

Texas Instruments, Attleboro, Massachusetts, is the world's largest producer of these multimetal systems. We also know our way around electronics. The result? A full line of reliable, low cost, interconnection systems featuring an extra measure of gold where it's needed. Premium performance at no premium in price.

IC Sockets

Texas Instruments family of IC sockets includes every type and size in common use today, and as wide a choice of contact materials as you'll find anywhere. Choose from open or closed entry *wire-wrapped*† sockets, standard or low profile solder tail sockets, cable plugs, and component platforms. Sizes from 8 to 40 pins.

IC Panels

To match the industry's broadest line of IC sockets TI offers one of the industry's widest selections of off-the-shelf socket panel products. Logic panels. Logic cards. Accessories. Add TI's custom design capability and wire wrapping for full service.

Additional information including pricing and delivery quotations may be obtained from your nearest TI Distributor, TI Representative, or:

Texas Instruments Incorporated
Connector Systems Department
MS 2-16
Attleboro, Massachusetts 02703
Telephone: (617) 222-2800
TELEX: ABORA927708

†Registered trademark of Gardner-Denver

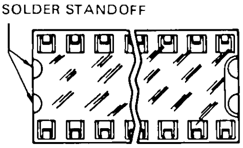
LOW PROFILE SOCKETS

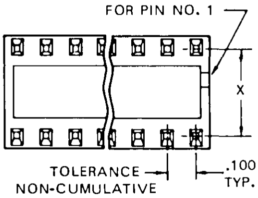
SOLDER TAIL

C-93 SERIES GOLD-CLAD CONTACTS

C-83 SERIES TIN-PLATED CONTACTS

- **Universal mounting and packaging**
- **Anti-wicking wafer**
- **Stand-off tabs on base for solder flush**
- **Redundant contact points for low contact resistance, high reliability and repetitive insertion**
- **Closed entry construction**





MATERIAL:

A. Body-glass filled nylon (GFN)

B. Contact-copper nickel alloy

C. Finish-see part number schedule

NOTES:

A. Sockets meet requirements of Texas Instruments test specification TS-0005 and test report TR-0003

B. Operating temperature −65°C to ±150°C

C. Contacts have redundant spring elements

D. Accommodates standard-IC leads up to .024" square, rectangular, or .024" diameter

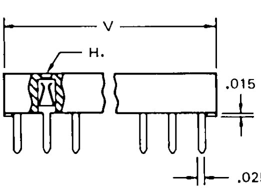
E. Contact is designed and oriented in the plastic body to generate maximum possible contact pressure

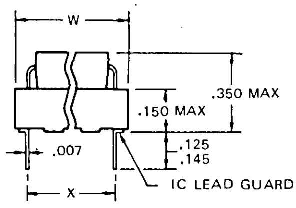
F. Socket is designed to achieve maximum density on boards

G. Sockets may be mounted end to end on .100" centers continuous line or on .400" centers row to row

H. Socket is designed to prevent IC leads from contacting P.C. board

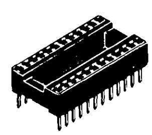
I. Closed entry feature provided to facilitate automatic IC insertion and protects the IC leads against damage





	8 Pin	14 Pin	16 Pin	18 Pin	20 Pin	22 Pin	24 Pin	28 Pin	40 Pin
Dimension X ±.005	.300	.300	.300	.300	.300	.400	.600	.600	.600
Dimension V ±.010	.400	.700	.800	.900	1.000	1.100	1.200	1.400	2.000
Dimension W (max)	.400	.400	.400	.400	.400	.500	.700	.700	.700

PART NO. SCHEDULE



BLACK BODY

NOMEX ANTI-WICKING WAFER		
Pins	**C-93 SERIES**	**C-83 SERIES**
8	C930810	C830810
14	C931410	C831410
16	C931610	C831610
18	C931810	C831810
20	C932010	C832010
22	C932210	C832210
24	C932410	C832410
28	C932810	C832810
40	C934010	C834010

CONTACT FINISH

C-93 SERIES:

100 microinch minimum gold stripe inlay

C-83 SERIES:

200 microinch minimum bright tin plate

9

STANDARD PROFILE SOCKET

SOLDER TAIL

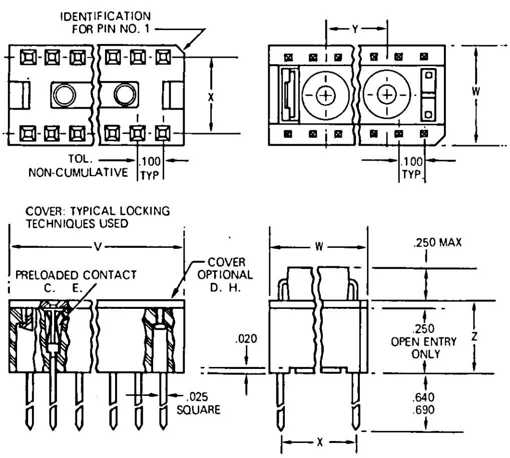
C-82 SERIES PLATED CONTACTS • C-92 SERIES GOLD CLAD CONTACTS

WIRE WRAP

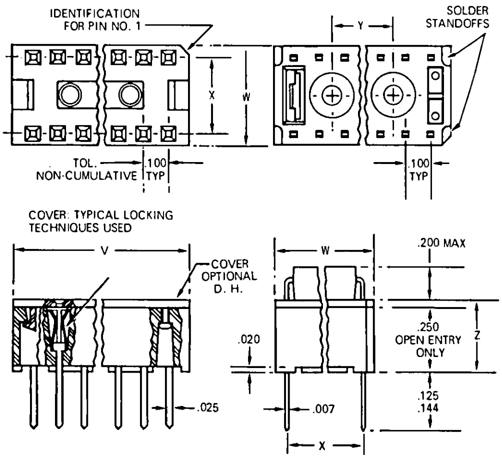
C-81 SERIES PLATED CONTACTS • C-91 SERIES GOLD CLAD CONTACTS

- **Designed for low cost, reliable, high density production packaging**
- **Universal mounting and packaging capabilities**
- **8 to 40 pin lead configurations**
- **Contacts accommodate .015" through .024" rectangular or round dual-in-line leads**
- **Wire wrap posts held to true position of .015" providing a true position of .020" on boards for efficient automatic wire wrapping**

WIRE WRAP



SOLDER TAIL



MATERIAL:

A. Body-glass filled nylon (GFN)

B. Contact-phosphor bronze per QQ-B-750 (C-81) copper nickel alloy (C-91)

C. Finish-see part number schedule

NOTES:

A. Sockets meet requirements of Texas Instruments test specification TS-0003 and test report TR-0001

B. Contacts are replaceable

C. Contacts have redundant spring elements

D. Cover is removeable

E. Contact is designed and oriented in the plastic body to generate maximum possible contact pressure

F. Operating temperature −65°C to +150°C

G. Sockets are designed to achieve maximum density on boards and may be mounted .400" row to row centers

H. Closed entry cover is provided to facilitate automatic insertion and protect IC leads against damage

I. Accommodates standard IC leads up to .024" square, rectangular or .024" dia.

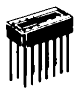
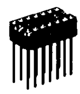
J. Contact retention — 7 lbs. min.

K. Sockets are capable of being automatically or semiautomatically wire wrapped

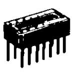
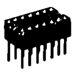
	8 Pin	14 Pin	16 Pin	18 Pin	20 Pin	24 Pin	28 Pin	36 Pin	40 Pin
Dimension V ±0.10	.465	.765	.865	.965	1.065	1.280	1.480	1.845	2.045
Dimension W (max)	.400	.400	.400	.400	.400	.700	.700	.700	.700
Dimension X ±.005	.300	.300	.300	.300	.300	.600	.600	.600	.600
Dimension Y ±0.10	NA	.400	.400	.400	.400	.500	.500	.800	1.000
Dimension Z ±.005	.280	.280	.280	.280	.280	.280	.280	.325	.325

9

WIRE WRAP

PART NUMBER SCHEDULE		OPEN ENTRY	CLOSED ENTRY
			
Contact Finish	Pins	Black Body	Black Cover
Series **C-81** 200-400 microinch min tin per MIL-T-10727	8	C810854	C810804
	14	C811454	C811404
	16	C811654	C811604
	18	C811854	C811804
	20	C812054	C812004
	24	C812454	C812404
	28	C812854	C812804
	36		C813604
	40		C814004
Series **C-91** 50 microinch min gold stripe inlay	8	C910850	C910800
	14	C911450	C911400
	16	C911650	C911600
	18	C911450	C911400
	20	C912050	C911800
	24	C912450	C912000
	28	C912850	C912800
	36		C913600
	40		C914000

SOLDER TAIL

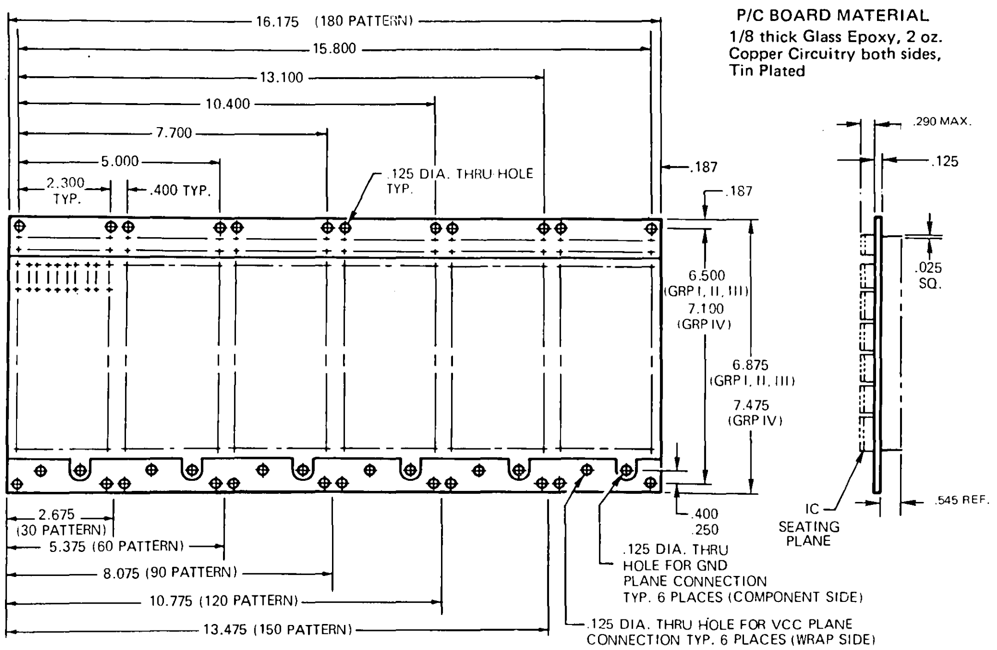
PART NUMBER SCHEDULE		OPEN ENTRY	CLOSED ENTRY
			
Contact Finish	Pins	Black Body	Black Cover
Series **C-82** 30 microinch min gold per MIL-G-45204 over 50 microinch min nickel per QQ-N-290	8	C820850	C820800
	14	C821450	C821400
	16	C821650	C821600
	18	C821850	C821800
	24	C822450	C822400
	28	C822850	C822800
	36		C823600
	40		C824000
Series **C-82** 50 microinch min gold per MIL-G-45204 over 100 microinch min nickel per QQ-N-290	8	C820852	C820802
	14	C821452	C821402
	16	C821652	C821602
	18	C821852	C821802
	24	C822452	C822402
	28	C822852	C822802
	36		C823602
	40		C824002
Series **C-82** 200-400 microinch min tin per MIL-T-10727	8	C820854	C820804
	14	C821454	C821404
	16	C821654	C821604
	18	C821854	C821604
	24	C822454	C822404
	28	C822854	C822804
	36		C823604
	40		C824004
Series **C-92** 100-microinch min gold stripe inlay	8	C920850	C920800
	14	C921450	C921400
	16	C921650	C921600
	18	C921850	C921800
	24	C922450	C922400
	28	C922850	C922800
	36		C923600
	40		C924000

SOCKET PANELS

STANDARD

D4 SERIES

- 180 position panel or multiples of 30 position with 14 or 16 position socket pattern
- I/O — 4 rows with 13 pins per row or 3 - 14 pin sockets
- Low cost standard hardware
- Available in 98 standard series
- Off-the-shelf availability



P/C BOARD MATERIAL
1/8 thick Glass Epoxy, 2 oz. Copper Circuitry both sides, Tin Plated

NOTE: Dimensions shown are nominal. Detail information and tolerances available on request (indicate series and group number).

STANDARD SOCKETS

C-81 or C-91 series, 14 pin or 16 pin, closed entry sockets as designated in the Part No. Schedule at right. See pages 7 and 8 for complete socket information.

C-81 SERIES SOCKETS

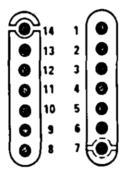
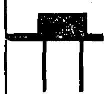
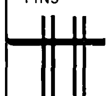
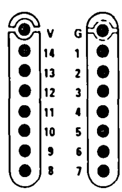
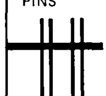
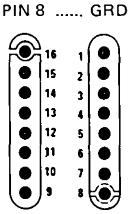
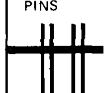
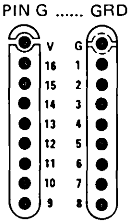
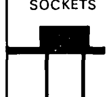
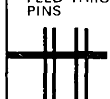
Body......... Glass filled nylon
Contact .... Phosphor bronze per QQ-B-750
Finish .... **30** microinch min. gold per MIL-G-45204 *over* **50** microinch min. nickel per QQ-N-290

C-91 SERIES SOCKETS

Body......... Glass filled nylon
Contact .... Copper nickel alloy
Finish .... **50** microinch min. gold stripe inlay

9

STANDARD PANEL PART NO. SCHEDULE —D4 Series

Group No.	I/O Option	Sockets Per Panel	C-81 Sockets	C-91 Sockets
Group I **14 Pin** PIN 14 .... VCC PIN 7 ...... GRD 	SOCKETS 	30	D411211	D411231
		60	D411212	D411232
		90	D411213	D411233
		120	D411214	D411234
		150	D411215	D411235
		180	D411216	D411236
	FEED-THRU PINS 	30	D411411	D411431
		60	D411412	D411432
		90	D411413	D411433
		120	D411414	D411434
		150	D411415	D411435
		180	D411416	D411436
Group II **14 Pin** PIN V ...... VCC PIN G ...... GRD 	SOCKETS 	30	D434211	D434231
		60	D434212	D434232
		90	D434213	D434233
		120	D434214	D434234
		150	D434215	D434235
		180	D434216	D434236
	FEED-THRU PINS 	30	D434411	D434431
		60	D434412	D434432
		90	D434413	D434433
		120	D434414	D434434
		150	D434415	D434435
		180	D434416	D434436
Group III **16 Pin** PIN 16 .... VCC PIN 8 ...... GRD 	SOCKETS 	30	D423211	D423231
		60	D423212	D423232
		90	D423213	D423233
		120	D423214	D423234
		150	D423215	D423235
		180	D423216	D423236
	FEED-THRU PINS 	30	D423411	D423431
		60	D423412	D423432
		90	D423413	D423433
		120	D423414	D423434
		150	D423415	D423435
		180	D423416	D423436
Group IV **16 Pin** PIN V ...... VCC PIN G ...... GRD 	SOCKETS 	30	D444211	D444231
		60	D444212	D444232
		90	D444213	D444233
		120	D444214	D444234
		150	D444215	D444235
		180	D444216	D444236
	FEED-THRU PINS 	30	D444411	D444431
		60	D444412	D444432
		90	D444413	D444433
		120	D444414	D444434
		150	D444415	D444435
		180	D444416	D444436

9

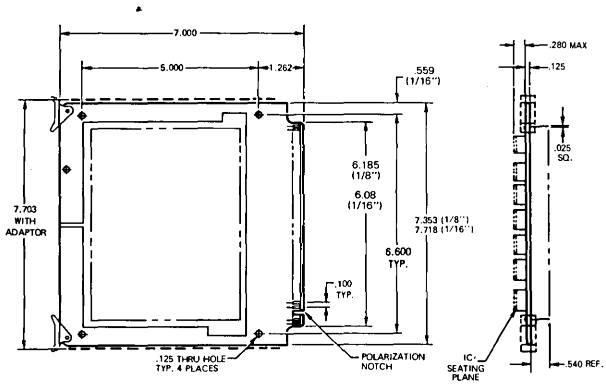
SOCKET CARDS

STANDARD

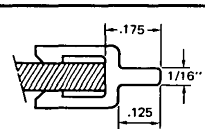
DO2 SERIES

- **Low Cost**
- **14 - 16 pin socket pattern – 60 position**
- **Standard ground and power pin commitment**
- **8 standard designs**
- **Mates with dual 60 position edge connector**

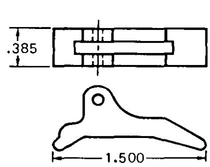
P/C BOARD MATERIAL
1/16 and 1/8 thick Glass Epoxy, 2 oz. Copper Circuitry both sides, Tin Plated



NOTE: Dimensions shown are nominal. Detail information and tolerances available on request (indicate series and group number).



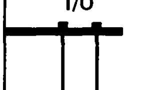
ADAPTER
Part no. Z501300



EJECTOR KEYS
Material: Nylon
Part no. Z501200 (1/8")
Z501201 (1/16")

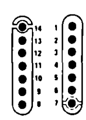
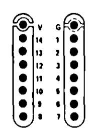
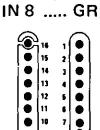
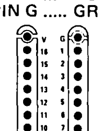
DO Series
MULTIPURPOSE CARD PART NO. SCHEDULE

I/O



Board Thk.	Part No.
1/16"	Z012510
1/8"	Z011510

DO2 Series
STANDARD CARD PART NO. SCHEDULE

Group No.	Board Thk.	C-81 Sockets	C-91 Sockets
Group I 14 Pin PIN 14 .... VCC PIN 7 ..... GRD 	1/16"	D022110	D022130
	1/8"	D021110	D021130
Group II 14 Pin PIN V ..... VCC PIN G ..... GRD 	1/16"	D022310	D022330
	1/8"	D021310	D021330
Group III 16 Pin PIN 16 .... VCC PIN 8 ..... GRD 	1/16"	D022210	D022230
	1/8"	D021210	D021230
Group IV 16 Pin PIN V ..... VCC PIN G ..... GRD 	1/16"	D022410	D022430
	1/8"	D021410	D021430

9