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TEXAS INSTRUMENTS INCORPORATED
Semiconductor Group

1981 Supplement to The TTL Data Book

for

Design Engineers

Second Edition

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INCORPORATED

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for

Design Engineers

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Index and Mechanical Data

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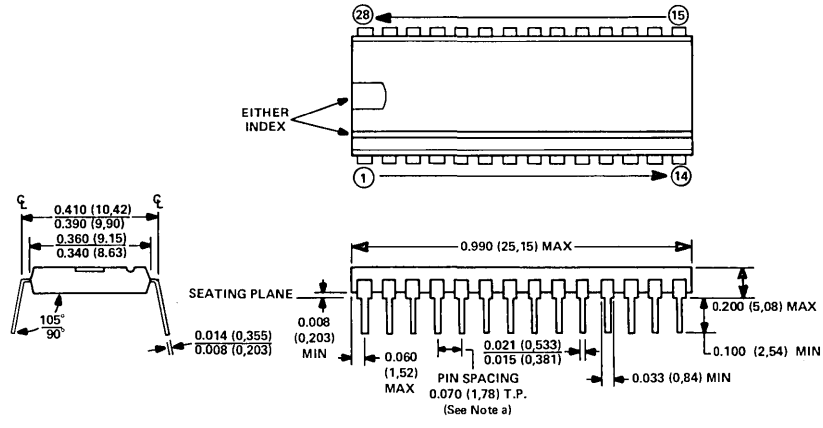
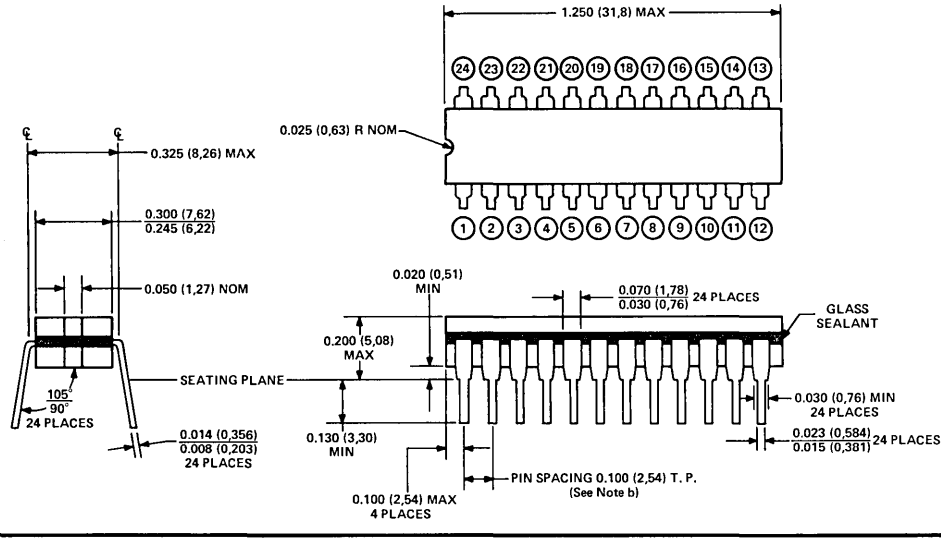
J and JT ceramic dual-in-line package

These hermetically sealed dual-in-line packages consist of a ceramic base, ceramic cap, and a 24- or 28-lead frame. Hermetic sealing is accomplished with glass. The packages are intended for insertion in mounting-hole rows on 0.300 (7,62) or 0.600 (15,24) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads (–00) require no additional cleaning or processing when used in soldered assembly.

28 PIN J CERAMIC

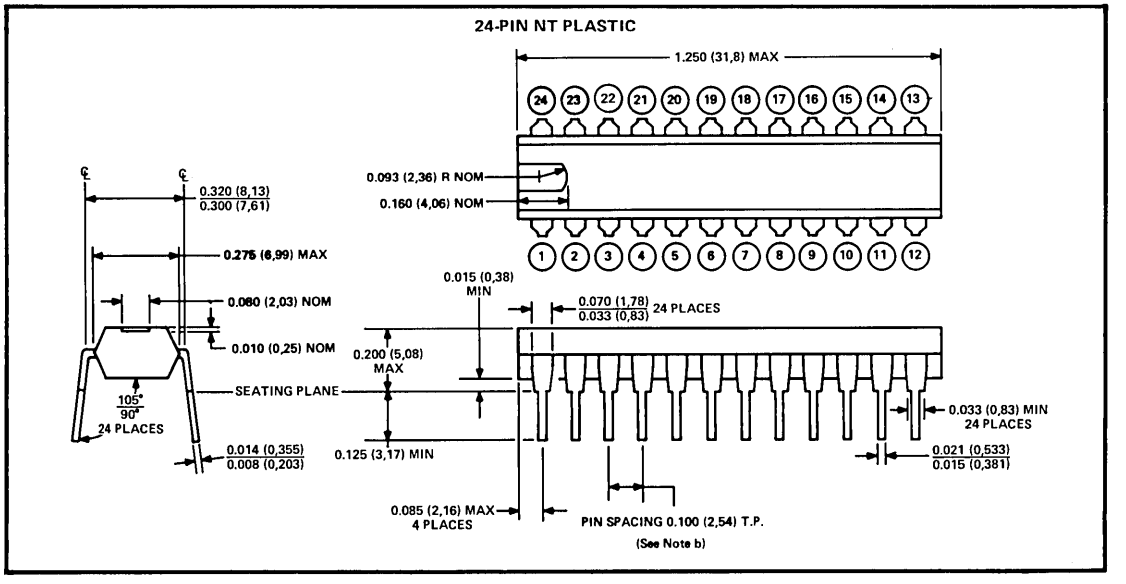


24 PIN JT CERAMIC



NT plastic dual-in-line packages

This dual-in-line package consists of a circuit mounted on a 24-lead frame and encapsulated within an electrically non-conductive plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. The packages are intended for insertion in mounting hole rows on 0.300 (7,62) or 0.600 (15,24) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.



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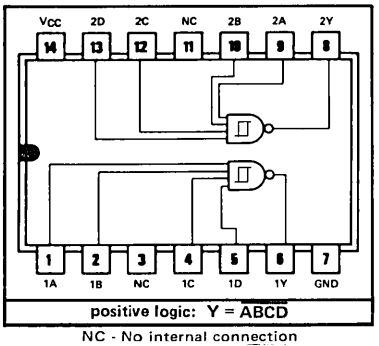
Low-Power Schottky and Schottky Circuits

TYPES SN54LS18, SN54LS19, SN54LS24, SN74LS18, SN74LS19, SN74LS24
SCHMITT-TRIGGER POSITIVE-NAND GATES AND INVERTERS WITH TOTEM-POLE OUTPUTS

D2627, JANUARY 1981

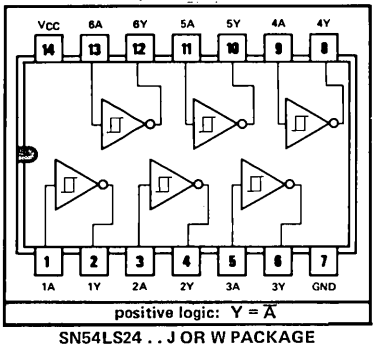
- Functionally and Mechanically Identical To 'LS13, 'LS14, and 'LS132, Respectively
- Improved Line-Receiving Characteristics
- P-N-P Inputs Reduce System Loading
- Excellent Noise Immunity With Typical Hysteresis of 0.7 V

SN54LS18 . . J OR W PACKAGE
SN74LS18 . . J OR N PACKAGE
(TOP VIEW)

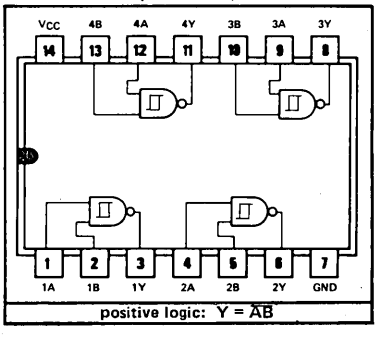


NC - No internal connection

SN54LS19 . . J OR W PACKAGE
SN74LS19 . . J OR N PACKAGE
(TOP VIEW)



SN54LS24 . . J OR W PACKAGE
SN74LS24 . . J OR N PACKAGE
(TOP VIEW)

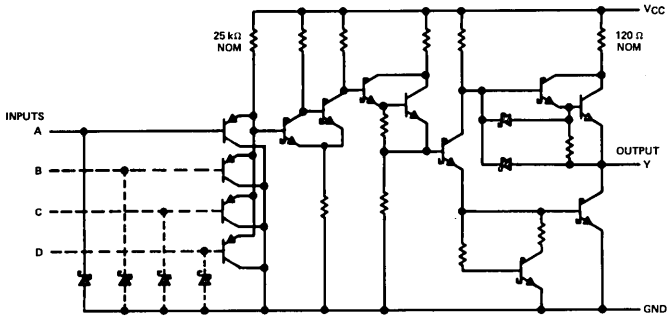


description

Each circuit functions as a NAND gate or inverter, but because of the Schmitt action, it has different input threshold levels for positive (V_{T+}) and for negative going (V_{T-}) signals. The hysteresis or backlash, which is the difference between the two threshold levels ($V_{T+} - V_{T-}$), is typically 700 millivolts.

These circuits are temperature-compensated and can be triggered from the slowest of input ramps and still give clean, jitter-free output signals.

schematic (each gate)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS'	−55°C to 125°C
SN74LS'	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

PRODUCT PREVIEW
This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

recommended operating conditions

	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{T+}	Positive-going threshold voltage	V_{CC} = 5 V			1.8			1.8		V
V_{T-}	Negative-going threshold voltage	V_{CC} = 5 V			1.1			1.1		V
	Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = 5 V		0.4	0.7		0.4	0.7		V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_I = V_{T-min}, I_{OH} = −400 μA		2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_I = V_{T+max}	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
I_{T+}	Input current at positive-going threshold	V_{CC} = 5 V, V_I = V_{T+}			−2			−2		μA
I_{T-}	Input current at negative-going threshold	V_{CC} = 5 V, V_I = V_{T-}			−5			−5		μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−0.2			−0.2	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX, V_I = V_O = 0 V		−20		−100	−20		−100	mA
I_{CCH}	Supply current, outputs high	V_{CC} = MAX, V_I = 0 V	'LS18		3.3			3.3		mA
			'LS19		9.9			9.9		
			'LS24		6.6			6.6		
I_{CCL}	Supply current, outputs low	V_{CC} = MAX, V_I = 4.5 V	'LS18		5.7			5.7		mA
			'LS19		17			17		
			'LS24		11			11		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, see note 2

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS18			'LS19			'LS24			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Any	Y	R_L = 2 kΩ, C_L = 15 pF		13			13			13		ns
t_{PHL}	Any	Y			37			18			25		ns

NOTE 2: Load circuit and voltage waveforms are shown on page 3-11 of *The TTL Data Book for Design Engineers*, Second Edition, LCC4112.

t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output

TEXAS INSTRUMENTS
INCORPORATED
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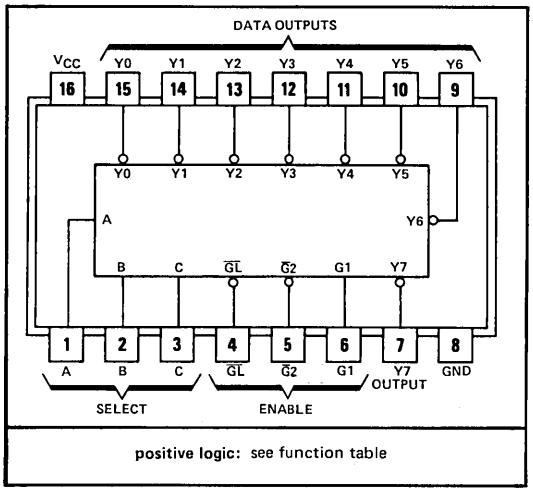
TYPES SN54LS137, SN74LS137
3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS WITH ADDRESS LATCHES

D2416, JUNE 1978

- Combines Decoder and 3-Bit Address Latch
- Incorporates 3 Enable Inputs to Simplify Cascading
- Low Power Dissipation . . . 65 mW Typ

SN54LS137 . . . J OR W PACKAGE
SN74LS137 . . . J OR N PACKAGE
(TOP VIEW)

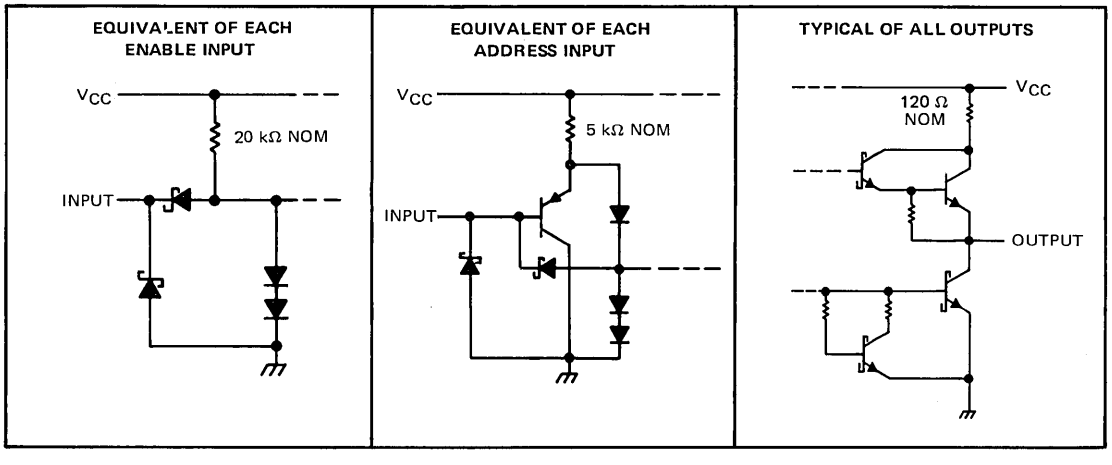


positive logic: see function table

description

The 'LS137 is a three-line to eight-line decoder/demultiplexer with latches on the three address inputs. When the latch-enable input ($\overline{GL}$) is low, the 'LS137 acts as a decoder/demultiplexer. When $\overline{GL}$ goes from low to high, the address present at the select inputs (A, B, and C) is stored in the latches. Further address changes are ignored as long as $\overline{GL}$ remains high. The output enable controls, G1 and $\overline{G2}$, control the state of the outputs independently of the select or latch-enable inputs. All of the outputs are high unless G1 is high and $\overline{G2}$ is low. The 'LS137 is ideally suited for implementing glitch-free decoders in strobed (stored-address) applications in bus-oriented systems.

schematics of inputs and outputs



TEXAS INSTRUMENTS
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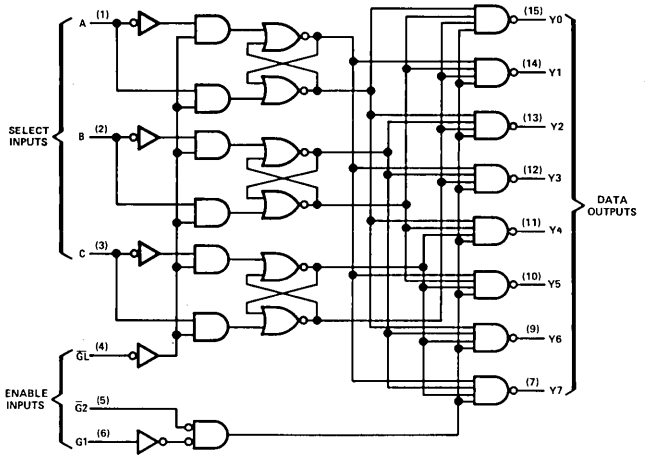
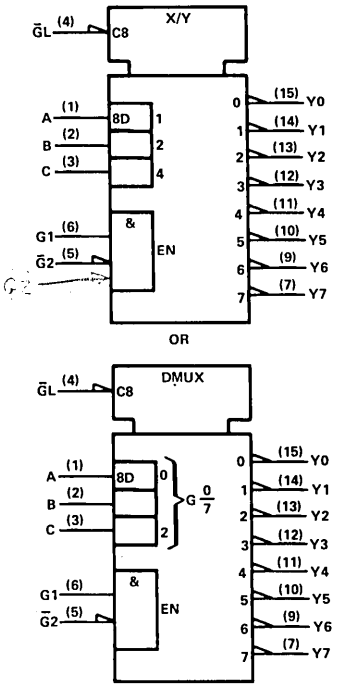
functional block diagram (positive logic)



logic symbol



FUNCTION TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT										
$\overline{GL}$	G1	$\overline{G2}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	H	H	L
H	H	L	X	X	X	Output corresponding to stored address, L; all others, H							

H = high level, L = low level, X = irrelevant

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (See Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS137 . . . . . −55°C to 125°C
SN74LS137 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

TEXAS INSTRUMENTS
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recommended operating conditions

	SN54LS137			SN74LS137			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Width of enabling pulse at $\overline{G1}$, t_w	15			15			ns
Setup time at A, B, and C inputs, t_{su}	10			10			ns
Hold time at A, B, and C inputs, t_h	10			10			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN54LS137			SN74LS137			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, I_{OH} = −400 μA		2.5	3.5		2.7	3.5		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL} max	V_{IH} = 2 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V	Enable			−0.4			−0.4	mA
				A, B, C			−0.2			−0.2	
I_{OS}	Short-circuit output current§	V_{CC} = MAX			−20		−100	−20		−100	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 2			11	18		11	18	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 2: I_{CC} is tested with all inputs grounded and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, see note 3

PARAMETER◇	FROM (INPUT)	TO (OUTPUT)	LEVELS OF DELAY	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A, B, C	Y	2	C_L = 15 pF, R_L = 2 kΩ, See Note 3		11	17	ns
t_{PHL}			4			25	38	
t_{PLH}	A, B, C	Y	3			16	24	ns
t_{PHL}			3			19	29	
t_{PLH}	Enable $\overline{G2}$	Y	2			13	21	ns
t_{PHL}			2			16	27	
t_{PLH}	Enable G1	Y	3			14	21	ns
t_{PHL}			3			18	27	
t_{PLH}	Enable $\overline{G1}$	Y	3			18	27	ns
t_{PHL}			4			25	38	

◇t_{PLH} ≡ propagation delay time, low-to-high-level output.
t_{PHL} ≡ propagation delay time, high-to-low-level output.

NOTE 3: For load circuit and voltage waveforms, see page 3-11 of *The TTL Data Book for Design Engineers,* second edition.

TYPICAL APPLICATION DATA

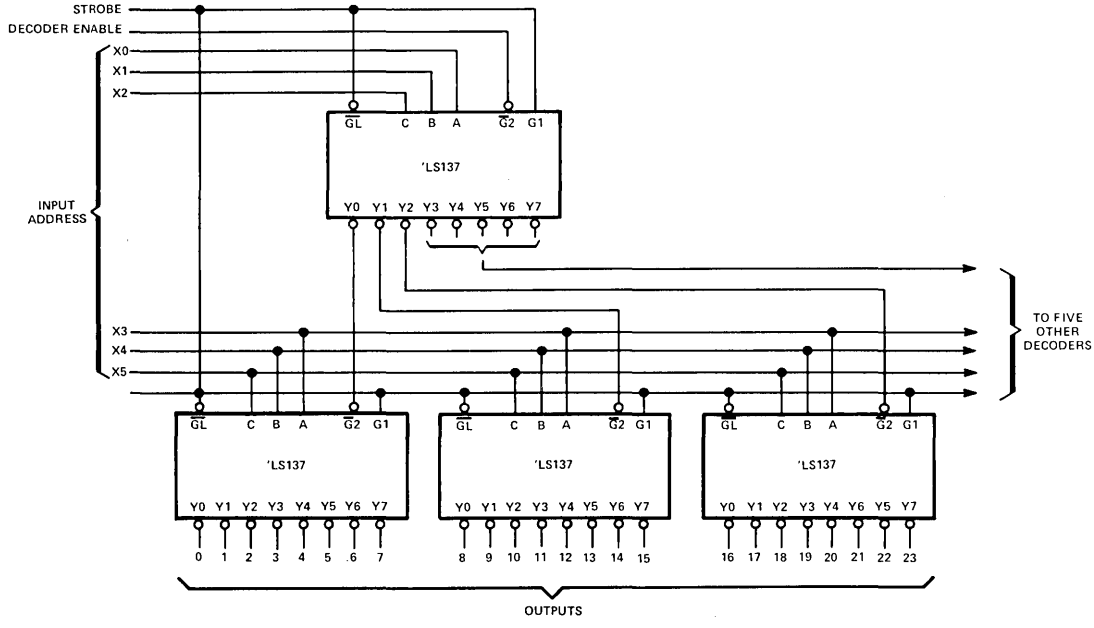


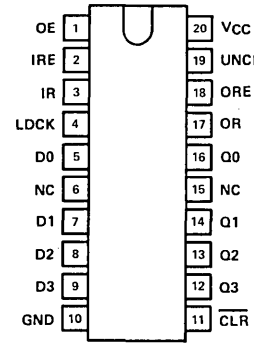
FIGURE 1–6-LINE TO 64-LINE DECODER WITH INPUT ADDRESS STORAGE

TYPES SN54LS222, SN54LS224, SN54LS227, SN54LS228, SN74LS222, SN74LS224, SN74LS227, SN74LS228
16 X 4 ASYNCHRONOUS FIRST-IN FIRST-OUT MEMORIES

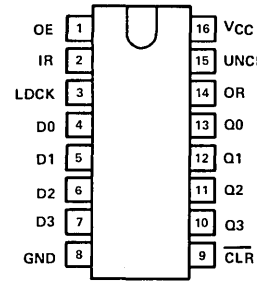
D2616, JANUARY 1981

- Independent Asynchronous Inputs and Outputs
- 16 Words of 4 Bits Each
- 3-State Outputs Drive Bus Lines Directly
- Data Rates from 0 to 10 MHz
- Fall-Through Time . . . 50 ns Typ
- Data Terminals Arranged for Optimum PC Board Layout
- Expandable Using External Gating

SN54LS222, SN54LS227 . . . J PACKAGE
SN74LS222, SN74LS227 . . . J OR N PACKAGE
(TOP VIEW)



SN54LS224, SN54LS228 . . . J PACKAGE
SN74LS224, SN74LS228 . . . J OR N PACKAGE
(TOP VIEW)



NC = No internal connection

description

These 64-bit memories are Low-Power Schottky memory arrays organized as 16 words of 4 bits each. They can be expanded in multiples of 15m+1 words or 4n bits, or both, (where n is the number of packages in the vertical array and m is the number of packages in the horizontal array) but some external gating is required (see Figure 1). For longer words using the 'LS224 or 'LS228, the IR signals of the first-rank packages and OR signals of the last-rank packages must be ANDed for proper synchronization.

TYPE	INPUT-READY ENABLE AND OUTPUT-READY ENABLE	OUTPUT
'LS222	Yes	3-State
'LS224	No	3-State
'LS227	Yes	Open-collector
'LS228	No	Open-collector

operation

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. These FIFO's are designed to process data at rates from 0 to 10 MHz in a bit-parallel format, word by word. Data is written into the memory on a high-to-low transition at the load clock input (LDCK) and read out on a low-to-high transition at the unload clock input (UNCK).

The memory is full when the number of words clocked in exceeds the number of words clocked out by 16. When the memory is full, LDCK signals have no effect. When the memory is empty, UNCK signals have no effect.

Status of the FIFO memory (see timing diagram) is monitored by the input ready (IR) and output ready (OR) flags that indicate "not full" and "not empty" conditions. The IR output will be high only when the memory is not full and the LDCK input is low. The OR output will be high only when the memory is not empty and UNCK is high.

A high-to-low transition at the clear ($\overline{CLR}$) input resets the internal stack control counters and also sets IR high and OR low to indicate that old data remaining at the data outputs is invalid. Data outputs are noninverting with respect to the data inputs and are at high impedance when output enable (OE) is low. OE does not affect the IR and OR outputs.

PRODUCT PREVIEW

TEXAS INSTRUMENTS
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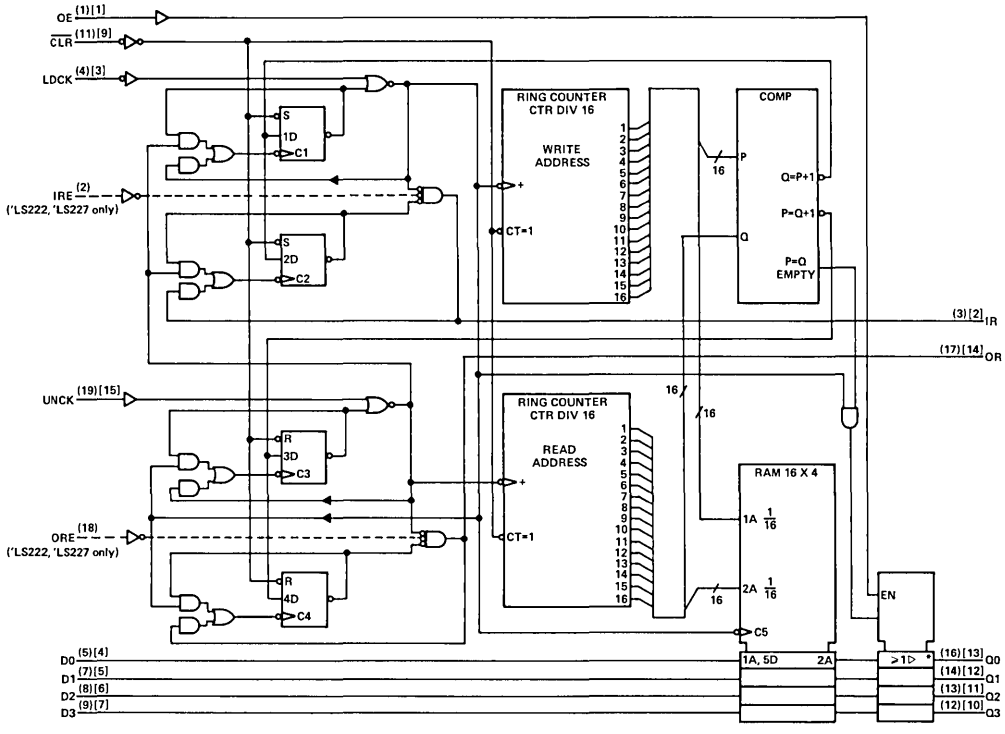
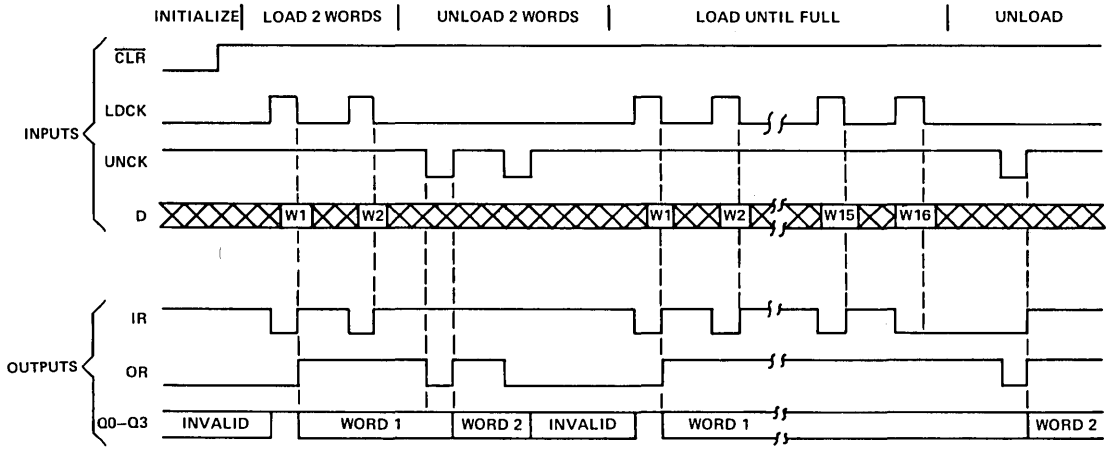
functional block diagram (positive logic)



•'LS222 and 'LS224 have 3-state (▽) outputs.
'LS227 and 'LS228 have open-collector (◇) outputs.

('LS222 and 'LS227 pin numbers)
['LS224 and 'LS228 pin numbers]

timing diagram



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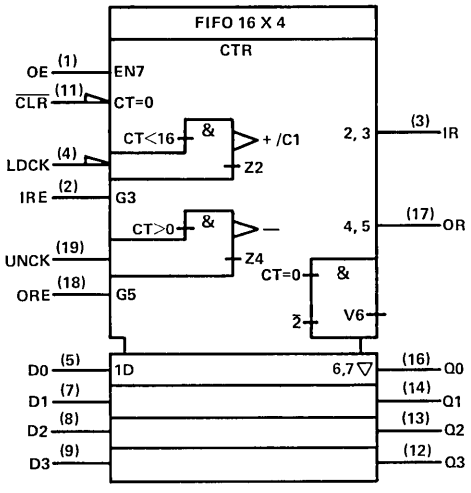
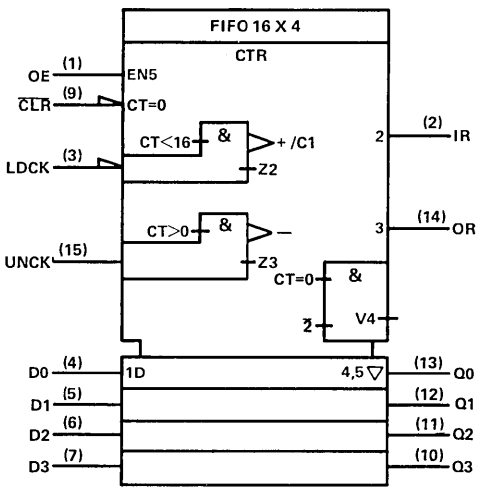
logic symbols

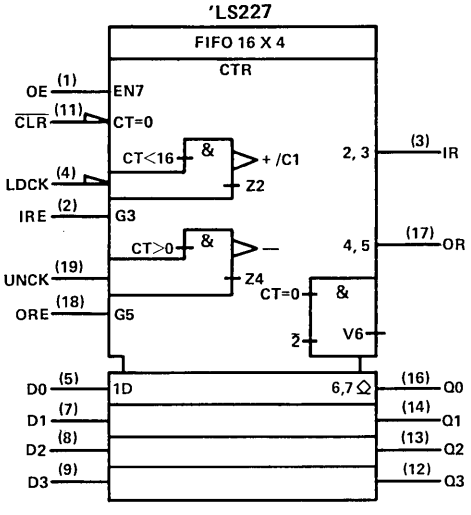
'LS222



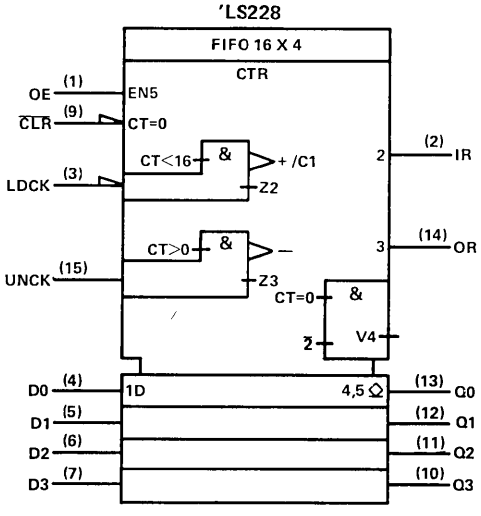
'LS224



'LS227



'LS228



These symbols are functionally accurate but do not show the details of implementation; for these, see the functional block diagram. The symbol represents the memory as if it were controlled by a single counter whose content is the number of words stored at that time. Output data is invalid when the counter content is 0.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (See Note 1)		7 V
Input voltage:		7 V
Off-state output voltage		5.5 V
Operating free-air temperature range:	SN54LS222, SN54LS224, SN54LS227, SN54LS228	−55°C to 125°C
	SN74LS222, SN74LS224, SN74LS227, SN74LS228	0°C to 70°C
Storage temperature range		−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	Q			−1			−2.6	mA
	IR, OR			−400			−400	μA
Low-level output current, I_{OL}	Q			12			24	mA
	IR, OR			4			8	
Setup time, t_{su}	D to LDCK ↓	50			50			ns
Hold time, t_h	D from LDCK↓	0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	Q	V_{CC} = MIN, V_{IH} = 2 V,	I_{OH} = MAX	2.4	3.3		2.4	3.2		V
		IR, OR	V_{IL} = V_{IL} max,	I_{OH} = −400 μA	2.5	3.4		2.7	3.4		
V_{OL}	Low-level output voltage	Q	V_{CC} = MIN, V_{IH} = 2 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
		IR, OR	V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
				I_{OL} = 8 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	Q	V_{CC} = MAX, V_{IH} = 2 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied	Q	V_{IL} = V_{IL} max	V_O = 0.4 V			−20			−20	μA
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7 V				100			100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit current§	Q	V_{CC} = MAX		−30		−130	−30		−130	mA
		IR, OR			−20		−100	−20		−100	
I_{CC}	Supply current		V_{CC} = MAX	Outputs high		84			84		mA
				Outputs low		87			87		
				Outputs disabled		89			89		

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

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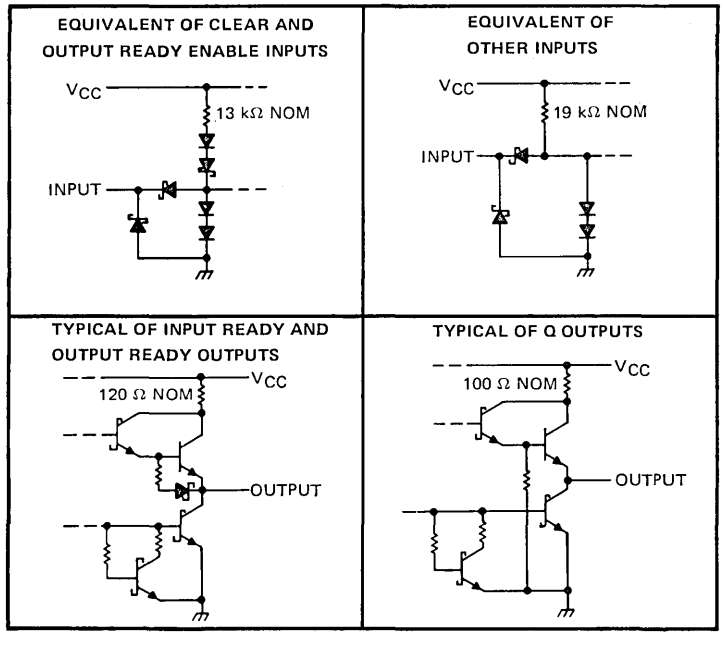
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM	TO	TEST CONDITIONS	'LS222			'LS224			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	IRE↑	IR	R_L = 2 kΩ, C_L = 15 pF, See Note 2		21					ns
t_{PHL}	IRE↓	IR			10					ns
t_{PLH}	ORE↑	OR			21					ns
t_{PHL}	ORE↓	OR			10					ns
t_{PLH}	LDCK↓	IR			25			25		ns
t_{PHL}	LDCK↑	IR			31			31		ns
t_{PLH}	LDCK↓	OR			45			45		ns
t_{PLH}	UNCK↑	OR			28			28		ns
t_{PHL}	UNCK↓	OR			26			26		ns
t_{PLH}	UNCK↑	IR			45			45		ns
t_{PLH}	$\overline{CLR}$↓	IR			33			33		ns
t_{PHL}	$\overline{CLR}$↓	OR			23			23		ns
t_{PLH}	LDCK↓	Q	R_L = 667 Ω, C_L = 45 pF, See Note 2		45			45		ns
t_{PHL}	LDCK↓	Q			34			34		ns
t_{PLH}	UNCK↑	Q			48			48		ns
t_{PHL}	UNCK↑	Q			46			46		ns
t_{PZL}	OE↑	Q			23			23		ns
t_{PZH}	OE↑	Q			21			21		ns
t_{PLZ}	OE↓	Q	R_L = 667 Ω, C_L = 5 pF, See Note 2		15			15		ns
t_{PHZ}	OE↓	Q			22			22		ns

NOTE 2: For load circuits and voltage waveforms, see page 3-11 of *The TTL Data Book for Design Engineers*, second edition.

schematics of inputs and outputs



recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}	Q			5.5			5.5	V
High-level output current, I_{OH}	IR, OR			−400			−400	μA
Low-level output current, I_{OL}	Q			12			24	mA
	IR, OR			4			8	
Setup time, t_{su}	D to LDCK ↓	50			50			ns
Hold time, t_h	D from LDCK↓	0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	IR, OR	V_{CC} = MIN, V_{IH} = 2 V, I_{OH} = −400 μA, V_{IL} = V_{IL} max		2.5	3.4		2.7	3.4		V
I_{OH}	High-level output current	Q	V_{CC} = MIN, V_{IH} = 2 V, V_{OH} = 5.5 V, V_{IL} = V_{IL} max				100			100	μA
V_{OL}	Low-level output voltage	Q	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
		IR, OR		I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
				I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7 V				100			100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	IR, OR	V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current		V_{CC} = MAX	Outputs high		84			84		mA
				Outputs low		87			87		
				Outputs disabled		89			89		

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

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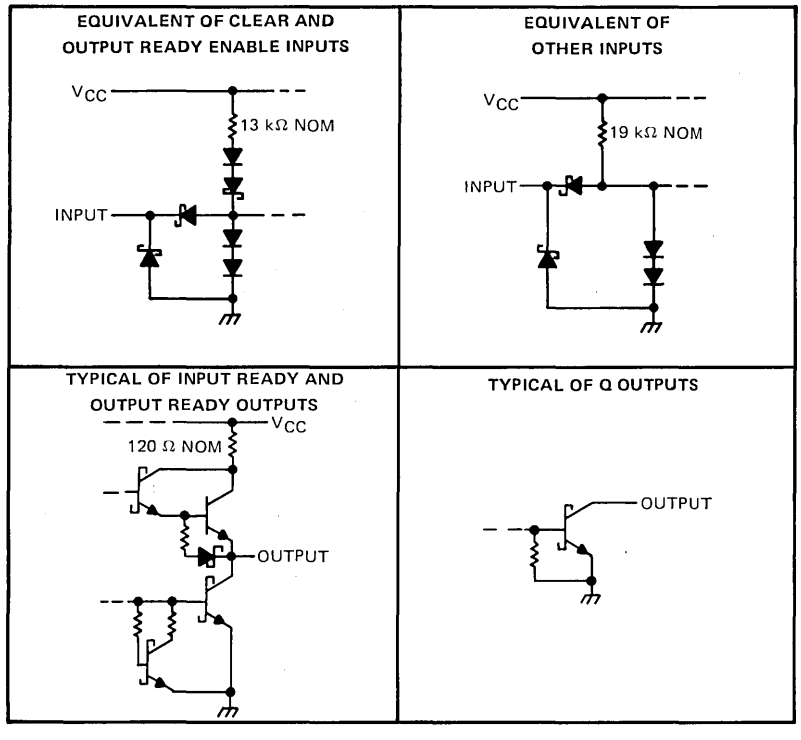
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM	TO	TEST CONDITIONS	'LS227			'LS228			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	IRE ↑	IR			23					ns
t_{PHL}	IRE ↓	IR			10					ns
t_{PLH}	ORE ↑	OR			23					ns
t_{PHL}	ORE ↓	OR			10					ns
t_{PLH}	LDCK ↓	IR	R_L = 2 kΩ,		27			27		ns
t_{PHL}	LDCK ↑	IR	C_L = 15 pF,		32			32		ns
t_{PLH}	LDCK ↓	OR	See Note 2		52			52		ns
t_{PLH}	UNCK ↑	OR			31			31		ns
t_{PHL}	UNCK ↓	OR			26			26		ns
t_{PLH}	UNCK ↑	IR			49			49		ns
t_{PLH}	$\overline{CLR}$ ↓	IR			36			36		ns
t_{PHL}	$\overline{CLR}$ ↓	OR			24			24		ns
t_{PLH}	LDCK ↓	Q			54			54		ns
t_{PHL}	LDCK ↓	Q			41			41		ns
t_{PLH}	UNCK ↑	Q	R_L = 667 Ω,		62			62		ns
t_{PHL}	UNCK ↑	Q	C_L = 45 pF,		53			53		ns
t_{PLH}	OE ↓	Q	See Note 2		23			23		ns
t_{PHL}	OE ↑	Q			25			25		ns

NOTE 2: For load circuits and voltage waveforms, see page 3-11 of *The TTL Data Book for Design Engineers*, second edition.

schematics of inputs and outputs



TYPICAL APPLICATIONS INFORMATION

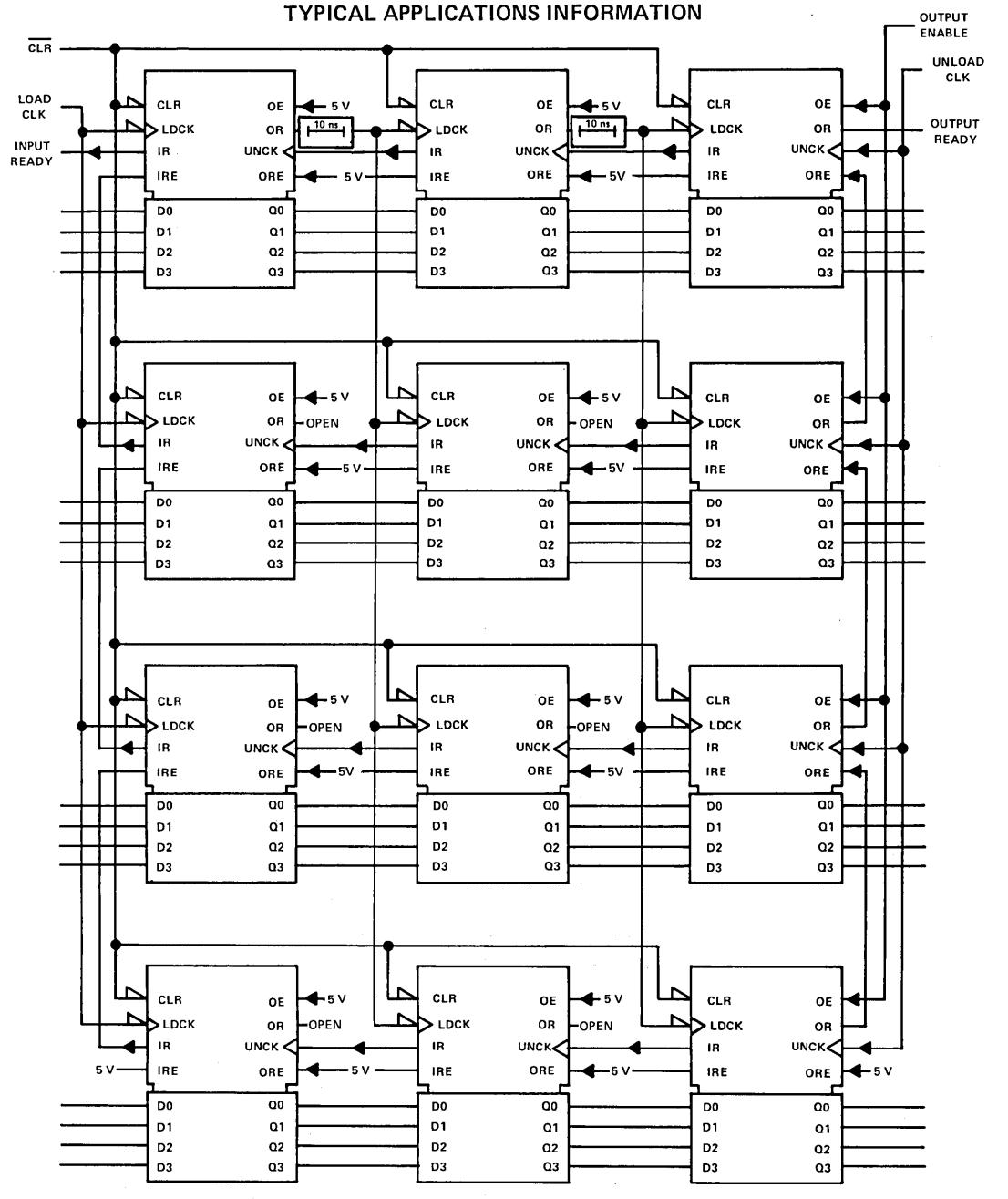


FIGURE 1–46-WORD BY 16-BIT EXPANSION USING 'LS222

10 ns ≡ Noninverting delay ⩾ 10 ns (e.g., 2 stages of 'LS04), 2 places.

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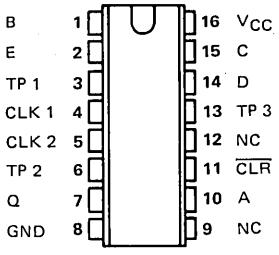
TYPES SN54LS292, SN54LS294, SN74LS292, SN74LS294
PROGRAMMABLE FREQUENCY DIVIDERS/DIGITAL TIMERS

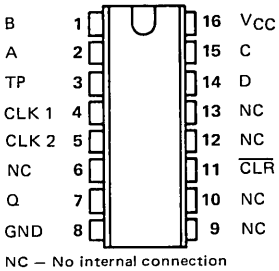
D2628, JANUARY 1981

- Count Divider Chain
- Digitally Programmable from 2^2 to 2^n (n = 31 for 'LS292, n = 15 for 'LS294)
- Useable Frequency Range from DC to 30 MHz
- Easily Expandable
- Applications
  - Frequency Division
  - Digital Timing

SN54LS292 . . J OR W PACKAGE
SN74LS292 . . J OR N PACKAGE
(TOP VIEW)



SN54LS294 . . J OR W PACKAGE
SN74LS294 . . J OR N PACKAGE
(TOP VIEW)



NC – No internal connection

description

These programmable frequency dividers/digital timers contain 31 flip-flops ('LS292) or 15 flip-flops ('LS294) plus 30 gates on a single chip. The count modulo is under digital control of the inputs provided.

Both types feature an active-low clear input to initialize the state of all flip-flops. To facilitate incoming inspection, test points are provided (TP1, TP2, and TP3 on the 'LS292 and TP on the 'LS294). These test points are not intended to drive system loads. Both types feature two clock inputs; either one may be used for clock gating. (See the function table below.)

'LS292, 'LS294 FUNCTION TABLE

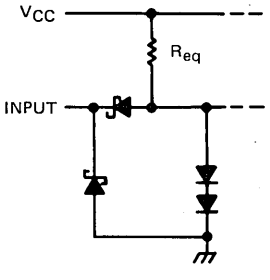
CLEAR	CLK 1	CLK 2	Q OUTPUT MODE
L	X	X	Cleared to L
H	↑	L	Count
H	L	↑	Count
H	H	X	Inhibit
H	X	H	Inhibit

A brief look at the digital timing capabilities of the 'LS292 will show that with a 1-MHz input frequency, programming for 2^{10} will give a period of 1.024 ms, and 2^{20} will give a period of 1.05 sec, 2^{26} will give a period of 1.12 min, and 2^{31} will give a period of 35.79 min.

These devices are easily cascadable giving limitless possibilities to timing delays that can be achieved.

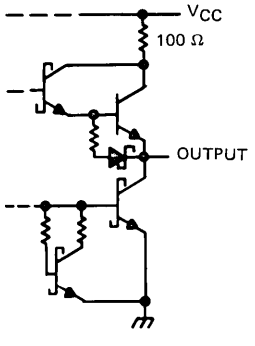
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT

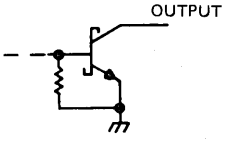


CLK: R_{eq} = 10 kΩ NOM
All others: R_{eq} = 20 kΩ NOM

TYPICAL OF Q OUTPUTS



TYPICAL OF TP OUTPUTS



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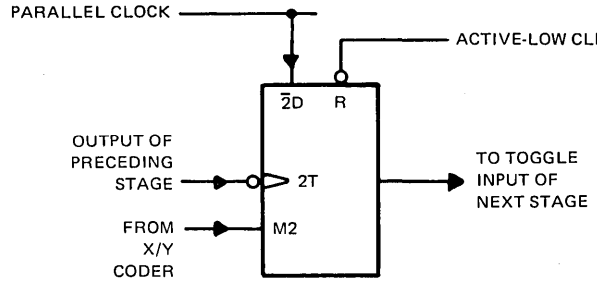
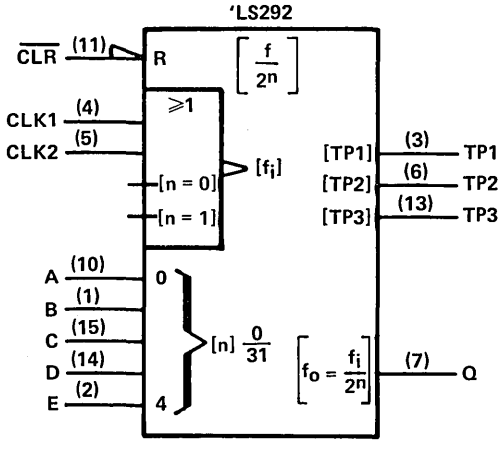
operation

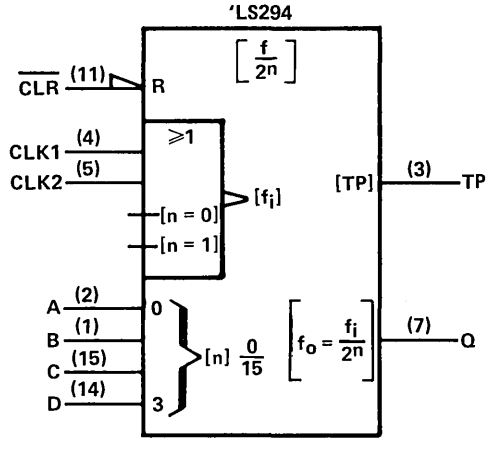
The functional block diagram shows that the count modulo is controlled by an X/Y decoder connected to the mode-control inputs of several flip-flops. These flip flops with mode controls each have a "D" input connected to the parallel clock line and a "T" input driven by the preceding stage. The parallel clock frequency is always the input frequency divided by four.

The X/Y decoder output selected by the programming inputs goes low. While a mode control is low, the "D" input of that flip-flop is enabled, and the signal from the parallel clock line ($f_{in} \div 4$) is passed to the "T" input of the following stage. All the other mode controls are high enabling the "T" inputs and causing each flip-flop in turn to divide by two.



logic symbols





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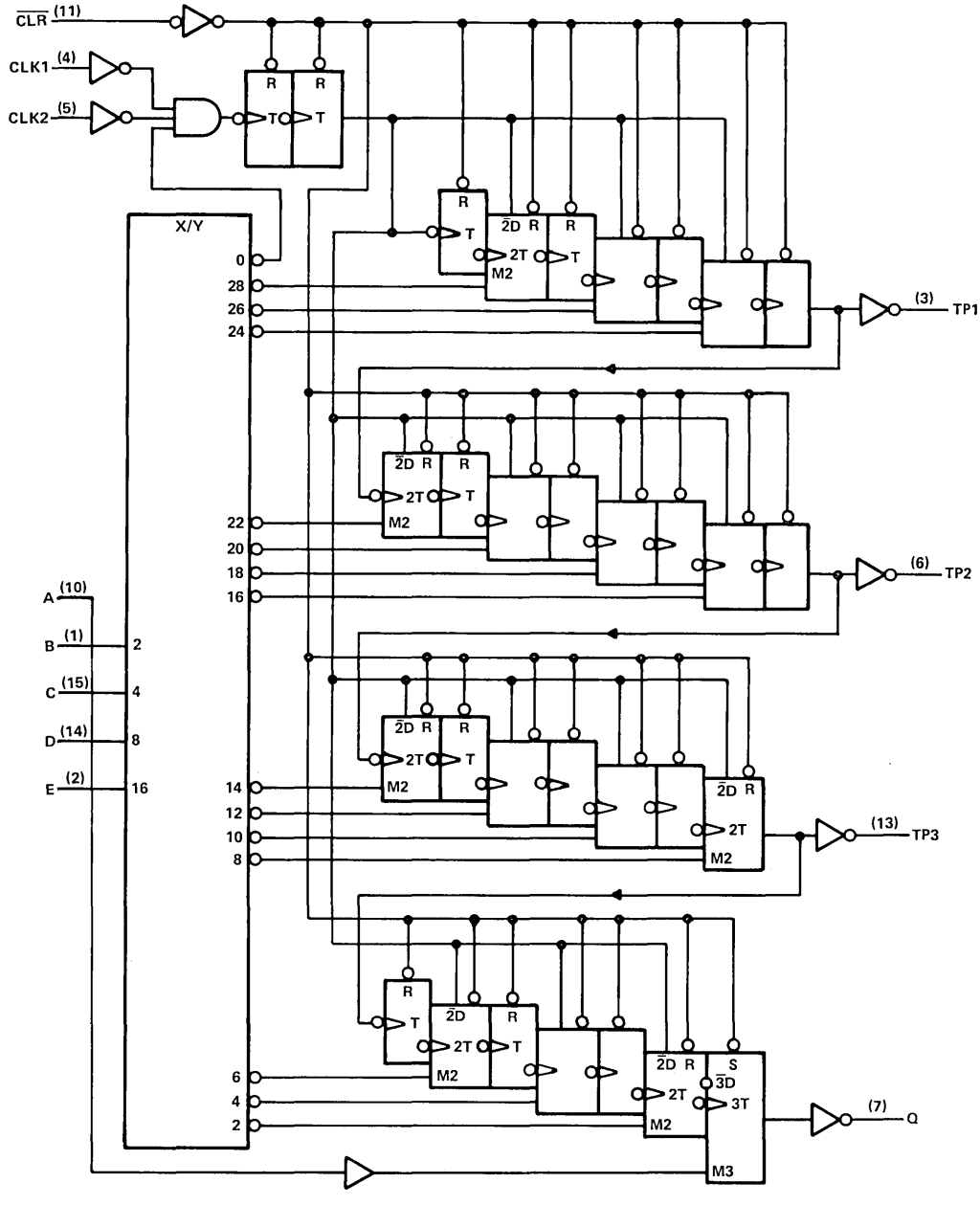
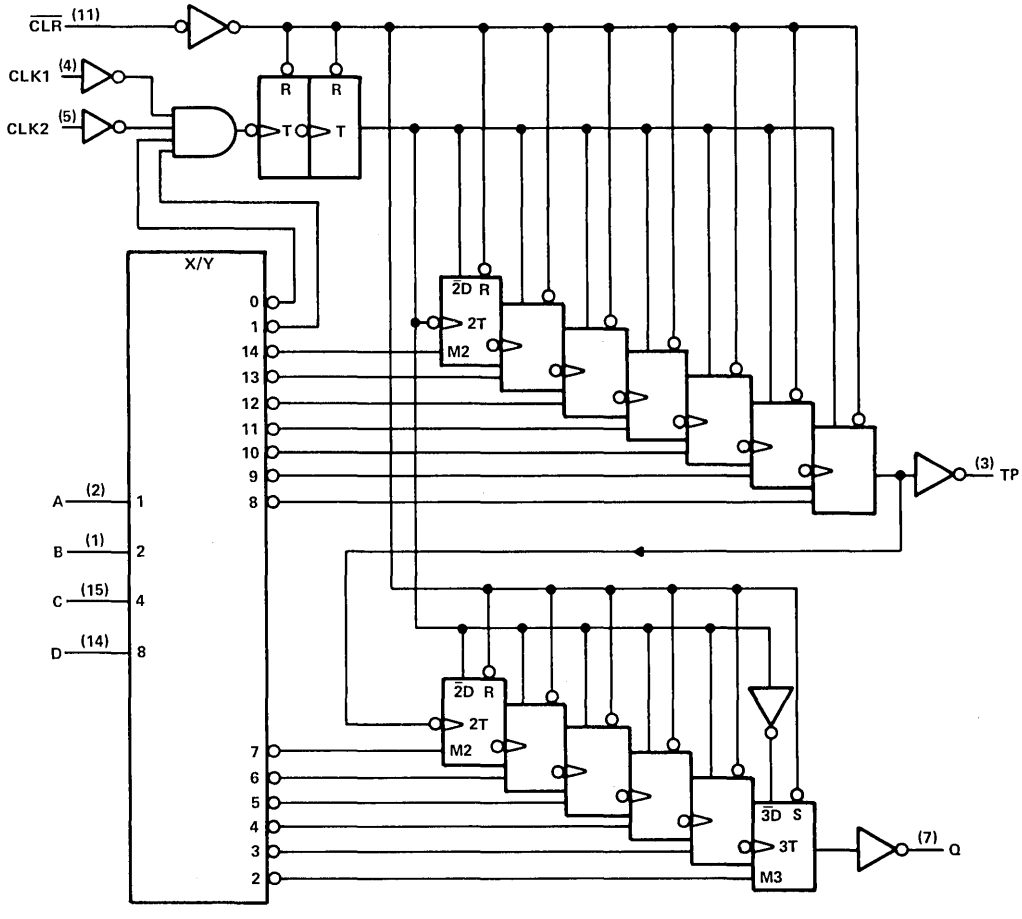
functional block diagram (positive logic)

'LS292



functional block diagram (positive logic)

'LS294



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS292, SN54LS294 . . . . . −55°C to 125°C
SN74LS292, SN74LS294 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

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recommended operating conditions

	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH} (Q only)			−1.2			−1.2	mA
Low-level output current, I_{OL} (Q only)			12			24	mA
Clock frequency, f_{clock}	0		30	0		30	MHz
Width of clock input pulse, t_w	16			16			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	Q	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = $V_{IL\ max}$	I_{OH} = −1.2 mA,	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	Q	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = $V_{IL\ max}$	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
		TP♦		I_{OL} = 1 mA					0.25	0.4	
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	CLK1, CLK2	V_{CC} = MAX, V_I = 0.4 V				−0.8			−0.8	mA
		All others					−0.4			−0.4	
I_{OS}	Short-circuit output current§	Q	V_{CC} = MAX		−30		−130	−30		−130	mA
I_{CC}	Supply current	'LS292	V_{CC} = MAX, All inputs grounded, All outputs open			40	75		40	75	mA
		'LS294				30	50		30	50	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ The duration of the short-circuit should not exceed one second.
♦ The TP output or outputs are not intended to drive external loads but are solely provided for test points.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, R_L = 667 Ω, C_L = 45 pF, see note 2

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS292			'LS294			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	CLK 1 or 2			30	50		30	50		MHz
t_{PLH}	CLK1 or 2	Q	Modulo set at 2^2, A thru E = LLLHL ('LS292), A thru D = LLHL ('LS294)		55	90		55	90	ns
t_{PHL}	CLK 1 or 2	Q			80	120		80	120	ns

NOTE 2: Voltage waveforms are shown on page 3-11 of *The TTL Data Book for Design Engineers*, Second Edition, LCC4112. See load circuit in Figure 1.

f_{max} ≡ maximum clock frequency
t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output

switching loads

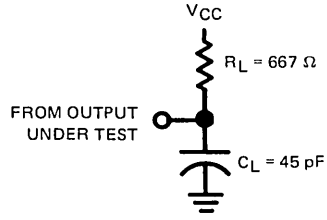

FIGURE 1

'LS292 FUNCTION TABLE

PROGRAMMING INPUTS					FREQUENCY DIVISION							
					Q		TP1		TP2		TP3	
E	D	C	B	A	BINARY	DECIMAL	BINARY	DECIMAL	BINARY	DECIMAL	BINARY	DECIMAL
L	L	L	L	L	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit
L	L	L	L	H	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit
L	L	L	H	L	2^2	4	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	L	L	H	H	2^3	8	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	L	H	L	L	2^4	16	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	L	H	L	H	2^5	32	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	L	H	H	L	2^6	64	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	L	H	H	H	2^7	128	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	H	L	L	L	2^8	256	2^9	512	2^{17}	131,072	2^2	4
L	H	L	L	H	2^9	512	2^9	512	2^{17}	131,072	2^2	4
L	H	L	H	L	2^{10}	1,024	2^9	512	2^{17}	131,072	2^4	16
L	H	L	H	H	2^{11}	2,048	2^9	512	2^{17}	131,072	2^4	16
L	H	H	L	L	2^{12}	4,096	2^9	512	2^{17}	131,072	2^6	64
L	H	H	L	H	2^{13}	8,192	2^9	512	2^{17}	131,072	2^6	64
L	H	H	H	L	2^{14}	16,384	2^9	512	Disabled Low		2^8	256
L	H	H	H	H	2^{15}	32,768	2^9	512	Disabled Low		2^8	256
H	L	L	L	L	2^{16}	65,536	2^9	512	2^3	8	2^{10}	1,024
H	L	L	L	H	2^{17}	131,072	2^9	512	2^3	8	2^{10}	1,024
H	L	L	H	L	2^{18}	262,144	2^9	512	2^5	32	2^{12}	4,096
H	L	L	H	H	2^{19}	524,288	2^9	512	2^5	32	2^{12}	4,096
H	L	H	L	L	2^{20}	1,048,576	2^9	512	2^7	128	2^{14}	16,384
H	L	H	L	H	2^{21}	2,097,152	2^9	512	2^7	128	2^{14}	16,384
H	L	H	H	L	2^{22}	4,194,304	Disabled Low		2^9	512	2^{16}	65,536
H	L	H	H	H	2^{23}	8,388,608	Disabled Low		2^9	512	2^{16}	65,536
H	H	L	L	L	2^{24}	16,777,216	2^3	8	2^{11}	2,048	2^{18}	262,144
H	H	L	L	H	2^{25}	33,554,432	2^3	8	2^{11}	2,048	2^{18}	262,144
H	H	L	H	L	2^{26}	67,108,864	2^5	32	2^{13}	8,192	2^{20}	1,048,576
H	H	L	H	H	2^{27}	134,217,728	2^5	32	2^{13}	8,192	2^{20}	1,048,576
H	H	H	L	L	2^{28}	268,435,456	2^7	128	2^{15}	32,768	2^{22}	4,194,304
H	H	H	L	H	2^{29}	536,870,912	2^7	128	2^{15}	32,768	2^{22}	4,194,304
H	H	H	H	L	2^{30}	1,073,741,824	2^9	512	2^{17}	131,072	2^{24}	16,777,216
H	H	H	H	H	2^{31}	2,147,483,648	2^9	512	2^{17}	131,072	2^{24}	16,777,216

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'LS294 FUNCTION TABLE

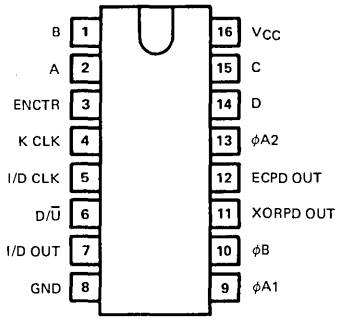
PROGRAMMING INPUTS				FREQUENCY DIVISION			
				Q		TP	
D	C	B	A	BINARY	DECIMAL	BINARY	DECIMAL
L	L	L	L	Inhibit	Inhibit	Inhibit	Inhibit
L	L	L	H	Inhibit	Inhibit	Inhibit	Inhibit
L	L	H	L	2^2	4	2^9	512
L	L	H	H	2^3	8	2^9	512
L	H	L	L	2^4	16	2^9	512
L	H	L	H	2^5	32	2^9	512
L	H	H	L	2^6	64	2^9	512
L	H	H	H	2^7	128	Disabled Low	
H	L	L	L	2^8	256	2^2	4
H	L	L	H	2^9	512	2^3	8
H	L	H	L	2^{10}	1,024	2^4	16
H	L	H	H	2^{11}	2,048	2^5	32
H	H	L	L	2^{12}	4,096	2^6	64
H	H	L	H	2^{13}	8,192	2^7	128
H	H	H	L	2^{14}	16,384	2^8	256
H	H	H	H	2^{15}	32,768	2^9	512

TYPES SN54LS297, SN74LS297
DIGITAL PHASE-LOCKED-LOOP FILTERS

D2629, JANUARY 1981

- Digital Design Avoids Analog Compensation Errors
- Easily Cascadable for Higher Order Loops
- Useful Frequency from DC to:
  50 MHz Typical (K Clock)
  35 MHz Typical (I/D Clock)

SN54LS297 . . . J OR W PACKAGE
SN74LS297 . . . J OR N PACKAGE



description

The SN54LS297 and SN74LS297 devices are designed to provide a simple, cost-effective solution to high-accuracy, digital, phase-locked-loop applications. These devices contain all the necessary circuits, with the exception of the divide-by-N counter, to build first order phase-locked loops as described in Figure 1 in the operations section.

Both exclusive-OR (XORPD) and edge-controlled (ECPD) phase detectors are provided for maximum flexibility.

Proper partitioning of the loop function, with many of the building blocks external to the package, makes it easy for the designer to incorporate ripple cancellation or to cascade to higher order phase-locked loops.

The length of the up/down K counter is digitally programmable according to the K counter function table. With A, B, C, and D all low, the K counter is disabled. With A high and B, C, and D low, the K counter is only three stages long, which widens the bandwidth or capture range and shortens the lock time of the loop. When A, B, C, and D are all programmed high, the K counter becomes seventeen stages long, which narrows the bandwidth or capture range and lengthens the lock time. Real-time control of loop bandwidth by manipulating the A through D inputs can maximize the overall performance of the digital phase-locked loop.

The 'LS297 can perform the classic first-order phase-locked loop function without using analog components. The accuracy of the digital phase-locked loop (DPLL) is not affected by V_{CC} and temperature variations, but depends solely on accuracies of the K clock, I/D clock, and loop propagation delays.

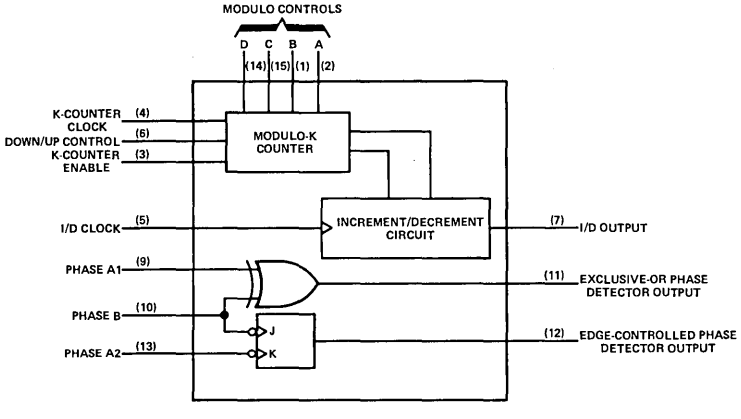


FIGURE 1—SIMPLIFIED BLOCK DIAGRAM

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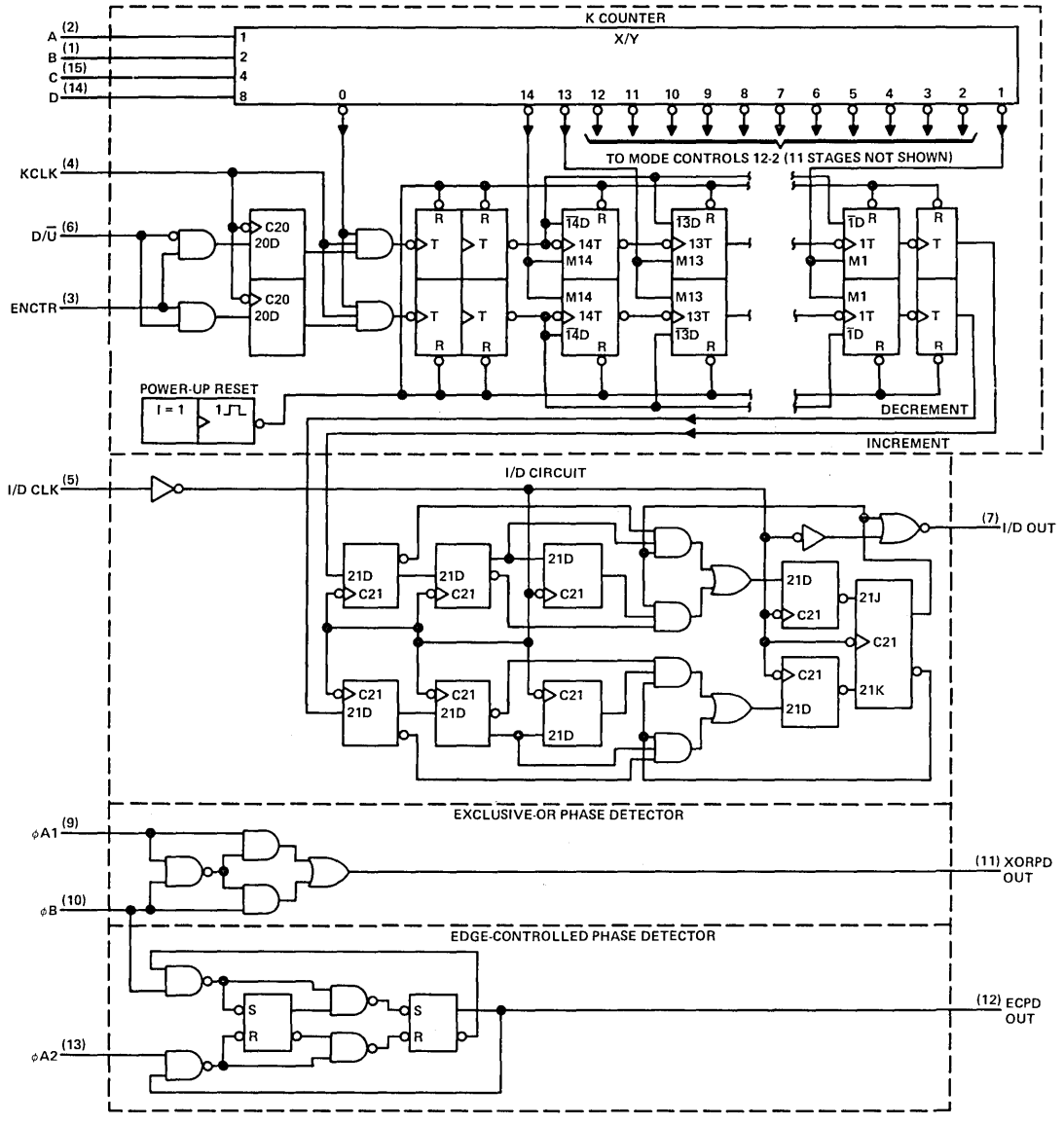
functional block diagram



K COUNTER FUNCTION TABLE
(DIGITAL CONTROL)

D	C	B	A	MODULO (K)
L	L	L	L	Inhibited
L	L	L	H	2^3
L	L	H	L	2^4
L	L	H	H	2^5
L	H	L	L	2^6
L	H	L	H	2^7
L	H	H	L	2^8
L	H	H	H	2^9
H	L	L	L	2^{10}
H	L	L	H	2^{11}
H	L	H	L	2^{12}
H	L	H	H	2^{13}
H	H	L	L	2^{14}
H	H	L	H	2^{15}
H	H	H	L	2^{16}
H	H	H	H	2^{17}

FUNCTION TABLE
EXCLUSIVE-OR PHASE DETECTOR

ϕA1	ϕB	XORPD OUT
L	L	L
L	H	H
H	L	H
H	H	L

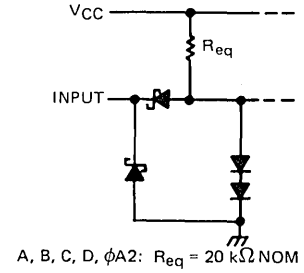
FUNCTION TABLE
EDGE-CONTROLLED PHASE DETECTOR

ϕA2	ϕB	ECPD OUT
H or L	↓	H
↓	H or L	L
H or L	↑	No change
↑	H or L	No change

H = steady-state high level
L = steady-state low level
↓ = transition from high to low
↑ = transition from low to high

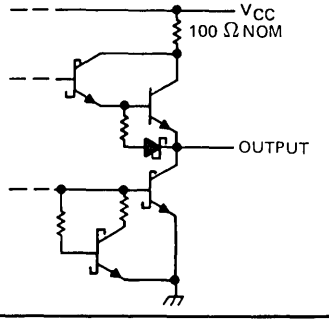
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT

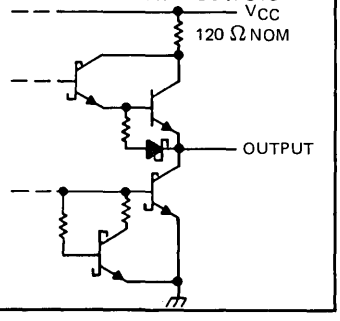


A, B, C, D, ϕA2: R_{eq} = 20 kΩ NOM
ϕB: R_{eq} = 6 kΩ NOM
All others: R_{eq} = 10 kΩ NOM

TYPICAL OF I/D OUTPUT



TYPICAL OF
ECPD AND XORPD OUTPUTS



operation

The phase detector generates an error signal waveform that, at zero phase error, is a 50% duty cycle square wave. At the limits of linear operation, the phase detector output will be either high or low all of the time, depending on the direction of the phase error ($\phi_{in} - \phi_{out}$). Within these limits, the phase detector output varies linearly with the input phase error according to the gain k_d, which is expressed in terms of phase detector output per cycle of phase error. The phase detector output can be defined to vary between ±1 according to the relation:

$$\text{PD Output} = \frac{\%\ \text{high} - \%\ \text{low}}{100} \qquad (1)$$

The output of the phase detector will be $k_d\ \phi_e$, where the phase error $\phi_e = \phi_{in} - \phi_{out}$.

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Exclusive-OR phase detectors (XORPD) and edge-controlled phase detectors (ECPD) are commonly used digital types. The ECPD is more complex than the XORPD logic function, but can be described generally as a circuit that changes states on one of the transitions of its inputs. k_d for an XORPD is 4 because its output remains high (PD output = 1) for a phase error of 1/4 cycle. Similarly, k_d for the ECPD is 2 since its output remains high for a phase error of 1/2 cycle. The type of phase detector will determine the zero-phase-error point, i.e., the phase separation of the phase detector inputs for ϕ_e defined to be zero. For the basic DPLL system of Figure 2, $\phi_e = 0$ when the phase detector output is a square wave. The XORPD inputs are 1/4 cycle out of phase for zero phase error. For the ECPD, $\phi_e = 0$ when the inputs are 1/2 cycle out of phase.

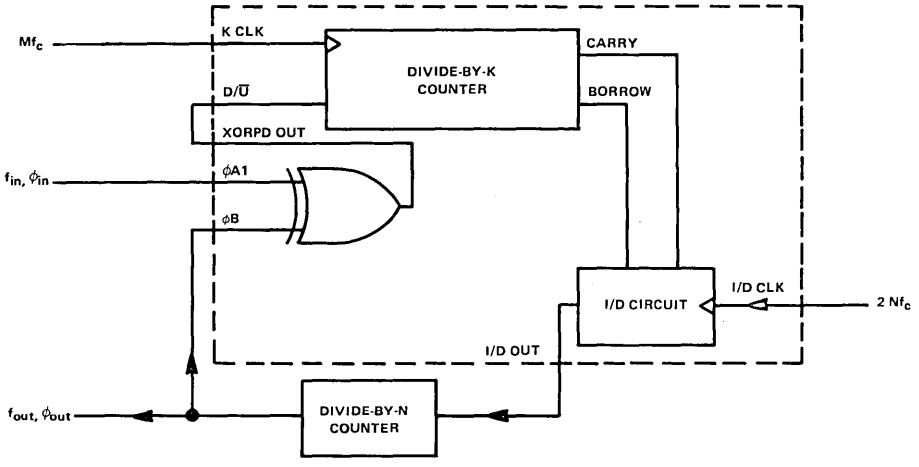

FIGURE 2–DPLL USING EXCLUSIVE-OR PHASE DETECTION

The phase detector output controls the up/down input to the K counter. The counter is clocked by input frequency Mf_c, which is a multiple M of the loop center frequency f_c. When the K counter recycles up, it generates a carry pulse. Recycling while counting down generates a borrow pulse. If the carry and borrow outputs are conceptually combined into one output that is positive for a carry and negative for a borrow, and if the K counter is considered as a frequency divider with the ratio Mf_c/K, the output of the K counter will equal the input frequency multiplied by the division ratio. Thus the output from the K counter is $(k_d\,\phi_e Mf_c)/K$.

The carry and borrow pulses go to the increment/decrement (I/D) circuit, which, in the absence of any carry or borrow pulse, has an output that is 1/2 of the input clock I/D CLK. The input clock is just a multiple, 2N, of the loop center frequency. In response to a carry or borrow pulse, the I/D circuit will either add or delete a pulse at I/D OUT. Thus the output of the I/D circuit will be $Nf_c + (k_d\phi_e Mf_c)/2K$.

The output of the N counter (or the output of the phase-locked loop) is thus:

$$f_o = f_c + (k_d\,\phi_e Mf_c)/2KN$$

If this result is compared to the equation for a first-order analog phase-locked loop, the digital equivalent of the gain of the VCO is just $Mf_c/2KN$ or f_c/K for $M = 2N$.

Thus the simple first-order phase-locked loop with an adjustable K counter is the equivalent of an analog phase-locked loop with a programmable VCO gain.

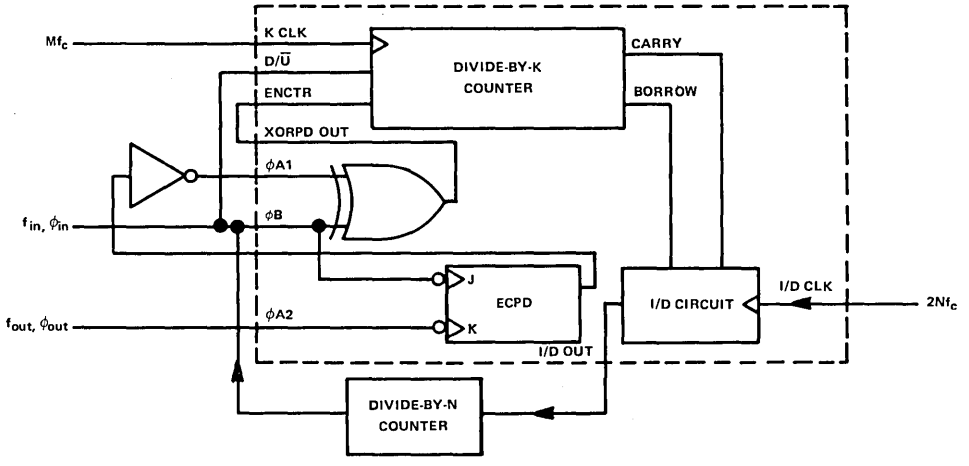

FIGURE 3–DPLL USING BOTH PHASE DETECTORS IN A RIPPLE-CANCELLATION SCHEME

absolute maximum rating over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS297 . . . . . −55°C to 125°C
SN74LS297 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS297			SN74LS297			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	I/D OUT			−1.2			−1.2	mA
	EXOR, ECPD			−400			−400	μA
Low-level output current, I_{OH}	I/D OUT			12			24	mA
	XOR, ECPD			4			8	mA
Clock frequency, f_{clock}	K Clock	0		30	0		30	MHz
	I/D Clock	0		15	0		15	MHz
Width of clock input pulse, t_w	K Clock	16			16			ns
	I/D Clock	33			33			ns
Setup time, t_{su}, to K Clock ↑	U/D̄, ENCTR	30			30			ns
Hold time, t_h, from K Clock ↑	U/D̄, ENCTR	0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS297 MIN	SN54LS297 TYP‡	SN54LS297 MAX	SN74LS297 MIN	SN74LS297 TYP‡	SN74LS297 MAX	UNIT
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	I/D OUT	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OH} = MAX	2.4			2.4			V
		Others		I_{OH} = MAX	2.5			2.7			
V_{OL}	Low-level output voltage	I/D OUT	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
		Others		I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
				I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current	U/$\overline{D}$, EN, ϕA1	V_{CC} = MAX, V_I = 2.7 V				40			40	μA
		ϕB					60			60	
		All others					20			20	
I_{IL}	Low-level input current	A,B,C,D,ϕA1	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
		ϕB	V_I = 0.4 V				−1.2			−1.2	
		All others					−0.8			−0.8	
I_{OS}	Short-circuit output current §	I/D OUT	V_{CC} = MAX		−30		−130	−30		−130	mA
		Others			−20		−100	−20		−100	
I_{CC}	Supply current		V_{CC} = MAX, All inputs grounded, All outputs open			75	120		75	120	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are of V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)		TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	KCLK		I/D OUT	R_L = 667 Ω, C_L = 45 pF, See Note 2	30	50		MHz
	I/D CLK		I/D OUT		15	35		
t_{PLH}	I/D CLK ↑		I/D OUT			15	25	ns
t_{PHL}	I/D CLK ↑		I/D OUT			22	35	ns
t_{PLH}	ϕA1 or ϕB	Other input low	XOR OUT	R_L = 2 kΩ, C_L = 45 pF, See Note 2		10	15	ns
	ϕA1 or ϕB	Other input high	XOR OUT			17	25	
t_{PHL}	ϕA1 or ϕB	Other input low	XOR OUT			15	25	ns
	ϕA1 or ϕB	Other input high	XOR OUT			17	25	
t_{PLH}	ϕB ↓		ECPD OUT			20	30	ns
t_{PHL}	ϕA2↓		ECPD OUT			20	30	ns

¶t_{PLH} = propagation delay time, low-to-high level output
t_{PHL} = propagation delay time, high-to-low level output

NOTE 2: Load circuit and voltage waveforms are shown on page 3-11 of *The TTL Data Book for Design Engineers*, Second Edition, LCC4112.

TYPES SN54LS320, SN54LS321, SN74LS320, SN74LS321
CRYSTAL-CONTROLLED OSCILLATORS

D2418, DECEMBER 1978 – REVISED JANUARY 1981

'LS320

- Crystal-Controlled Oscillator Operation from 1 MHz to 20 MHz
- 2-Phase Driver Outputs

'LS321

- Similar to 'LS320 But Includes f/2 and f/4 Count-Down Outputs

description

The 'LS320 is a crystal-controlled oscillator/clock driver. It features complementary standard and high-current driver outputs. A synchronization flip-flop is included.

The driver outputs, F′ and $\overline{F}$′ have very-low impedance and can be used to drive highly capacitive TTL-level lines. If the driver outputs are not used, then the V_{CC}' terminal can be left open.

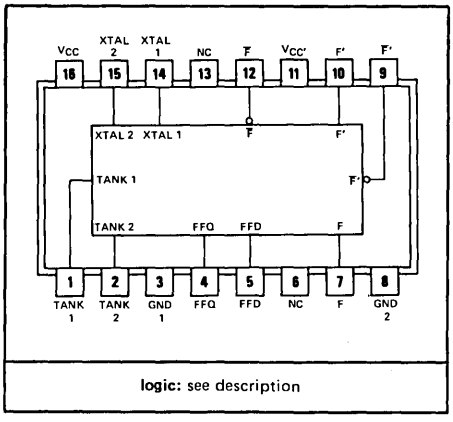
The 'LS321 is identical to the 'LS320 except it additionally features two count-down outputs, F/2 and F/4.

These circuits were designed for crystal control of frequency and capacitive control is not recommended. If a fundamental crystal is used, an inductor of 5 to 160 μH is required to be connected between the tank 1 and tank 2 inputs. If a third-overtone crystal is used, a tuned tank is necessary.

Interaction of the driver outputs with the other outputs limits useful frequencies as shown in the frequency-limits table.

The SN54LS320 and SN54LS321 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LS320 and SN74LS321 are characterized for operation from 0°C to 70°C.

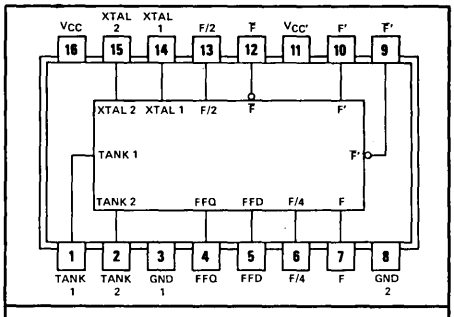
SN54LS320 . . . J OR W PACKAGE
SN74LS320 . . . J OR N PACKAGE
(TOP VIEW)



logic: see description

NC—No internal connection

SN54LS321 . . . J OR W PACKAGE
SN74LS321 . . . J OR N PACKAGE
(TOP VIEW)



logic: see description

FREQUENCY LIMITS

OUTPUTS IN USE	V_{CC}	V_{CC}'	f_{max}
Driver outputs only	5 V	5 V	20 MHz
Other outputs only	5 V	Open	20 MHz
Driver and any other outputs	5 V	5 V	10 MHz

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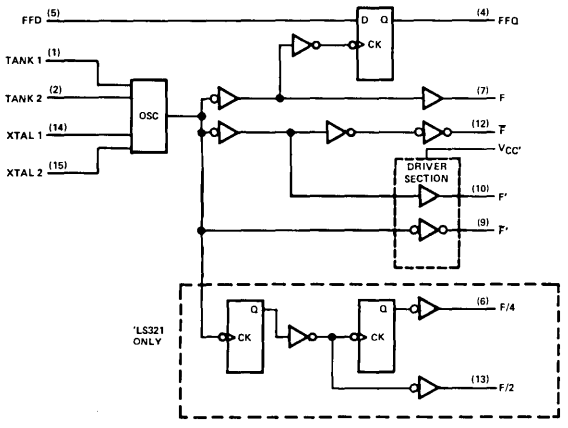
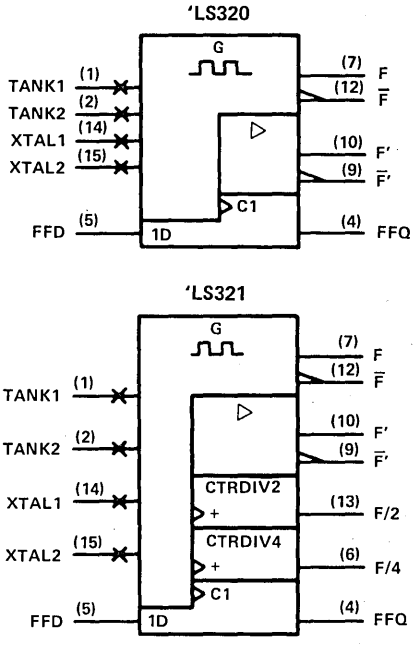
functional block diagram (positive logic)



logic symbols



2

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Supply voltage, V_{CC}' . . . . . 7 V
Input voltage to FFD terminal . . . . . −0.5 V to 7 V
Operating free-air temperature range: SN54LS320, SN54LS321 . . . . . −55°C to 125°C
SN74LS320, SN74LS321 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminals.

recommended operating conditions

		SN54LS320 SN54LS321			SN74LS320 SN74LS321			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Supply voltage, V_{CC}'		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	F' or F̄'			−12			−24	mA
	F, F̄, F/2, F/4			−0.4			−0.4	
Low-level output current, I_{OL}	F' or F̄'			12			24	mA
	F, F̄, F/2, F/4			4			8	
Output frequency, f_{out}	F/2 ('LS321)	0.5		10	0.5		10	MHz
	F/4 ('LS321)	0.25		5	0.25		5	
	F or F̄	1		20	1		20	
Operating free-air temperature, T_A		−55		125	0		70	°C

Input and output schematics are similar to those shown for SN74LS326 on page 7-462 of *The TTL Data Book for Design Engineers*, second edition, LCC4112.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†			SN54LS320 SN54LS321			SN74LS320 SN74LS321			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage					2			2			V
V_{IL}	Low-level input voltage							0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	V_{CC}' = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	F′, $\overline{F}$′	V_{CC} = 4.5 V,	V_{CC}' = 4.5 V,	I_{OH} = −12 mA	2.5	3.3					V
			V_{CC} = 4.75 V,	V_{CC}' = 4.75 V,	I_{OH} = −24 mA				2.7	3.3		
		Others	V_{CC} = MIN,	V_{IH} = 2 V,	I_{OH} = −400 μA	2.5	3.4		2.7	3.4		
V_{OL}	Low-level output voltage	F′, $\overline{F}$′	V_{CC} = MIN,	V_{CC}' = MIN	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
					I_{OL} = 24 mA					0.35	0.5	
		Others	V_{CC} = MIN,	V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
					I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current§		V_{CC} = MAX			−20		−100	−20		−100	mA
I_{CC}	Supply current from V_{CC}		V_{CC} = MAX,	FFD at GND	'LS320		42	70		42	70	mA
					'LS321		47	75		47	75	
I_{CC}'	Supply current from V_{CC}'		V_{CC} = MAX,	V_{CC}' = MAX,	FFD at GND		4	8		4	8	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, V_{CC}' = 5 V, and T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second. Outputs F′ and $\overline{F}$′ do not have short-circuit protection and these limits do not apply.

switching characteristics, V_{CC} = 5 V, V_{CC}' = 5 V, T_A = 25°C

PARAMETER		OUTPUTS	TEST CONDITIONS¶	'LS320			'LS321			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	Maximum operating frequency	F/2	C_L = 100 pF				10	15		MHz
		F/4					5	7.5		
		All others		20	30		20	30		
t_r	Rise time, 1 V to 3 V	F′, $\overline{F}$′	C_L = 50 pF		6	12		6	12	ns
			C_L = 100 pF		7	14		7	14	
			C_L = 200 pF		7	14		7	14	
		Others	C_L = 50 pF		11	22		11	22	
			C_L = 100 pF		25	40		25	40	
			C_L = 200 pF		45	70		45	70	
t_f	Fall time, 3 V to 1 V	F′, $\overline{F}$′	C_L = 50 pF		5	10		5	10	ns
			C_L = 100 pF		5	10		5	10	
			C_L = 200 pF		6	12		6	12	
		Others	C_L = 50 pF		6	12		6	12	
			C_L = 100 pF		10	20		10	20	
			C_L = 200 pF		17	30		17	30	

¶ Load circuit and voltage waveforms are shown on page 3-11 of *The TTL Data Book for Design Engineers*, Second Edition, LCC4112.

TEXAS INSTRUMENTS
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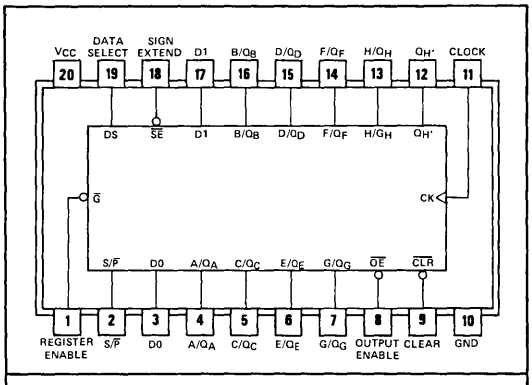
TYPES SN54LS322A, SN74LS322A
8-BIT SHIFT REGISTERS WITH SIGN EXTEND

D2411, OCTOBER 1977 – REVISED JANUARY 1981

- Multiplexed Inputs/Outputs Provide Improved Bit Density
- 3-State Outputs Drive Bus Lines Directly
- Sign Extend Function
- Direct Overriding Clear

SN54LS322A . . . J PACKAGE
SN74LS322A . . . J OR N PACKAGE
(TOP VIEW)



logic: see description and function table

description

These low-power Schottky eight-bit shift registers feature multiplexed input/output data ports to achieve full eight-bit data handling in a single 20-pin package. Serial data may be entered into the shift-right register through either the D0 or the D1 input as selected by the data select input. A serial output (Q_H') is also provided to facilitate expansion. Synchronous parallel loading is accomplished by taking both the register enable and the $S/\overline{P}$ inputs low. This places the three-state input/output ports in the data input mode. Data are entered on the low-to-high transition of the clock. The data extend function repeats the sign in the Q_A flip-flop during shifting. A direct overriding clear input clears the internal registers when taken low whether the outputs are enabled or off. The output enable does not interfere with synchronous operation of the register.

FUNCTION TABLE

OPERATION	INPUTS							INPUTS/OUTPUTS				OUTPUT
	CLEAR	REGISTER ENABLE	$S/\overline{P}$	SIGN EXTEND	DATA SELECT	OUTPUT ENABLE	CLOCK	A/Q_A	B/Q_B	C/Q_C . . . H/Q_H		Q_H'
Clear	L	H	X	X	X	L	X	L	L	L	L	L
	L	X	H	X	X	L	X	L	L	L	L	L
Hold	H	H	X	X	X	L	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{H0}	Q_{H0}
Shift Right	H	L	H	H	L	L	↑	D0	Q_{An}	Q_{Bn}	Q_{Gn}	Q_{Gn}
	H	L	H	H	H	L	↑	D1	Q_{An}	Q_{Bn}	Q_{Gn}	Q_{Gn}
Sign Extend	H	L	H	L	X	L	↑	Q_{An}	Q_{An}	Q_{Bn}	Q_{Gn}	Q_{Gn}
Load	H	L	L	X	X	X	↑	a	b	c	h	h

When the output enable is high, the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected. If both the register enable input and the $S/\overline{P}$ input are low while the clear input is low, the register is cleared while the eight input/output terminals are disabled to the high-impedance state.

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
Q_{A0} . . . Q_{H0} = the level of Q_A through Q_H, respectively, before the indicated steady-state conditions were established
Q_{An} . . . Q_{Hn} = the level of Q_A through Q_H, respectively, before the most recent ↑ transition of the clock
D0, D1 = the level of steady-state inputs at inputs D0 and D1 respectively
a . . . h = the level of steady-state inputs at inputs A through H respectively

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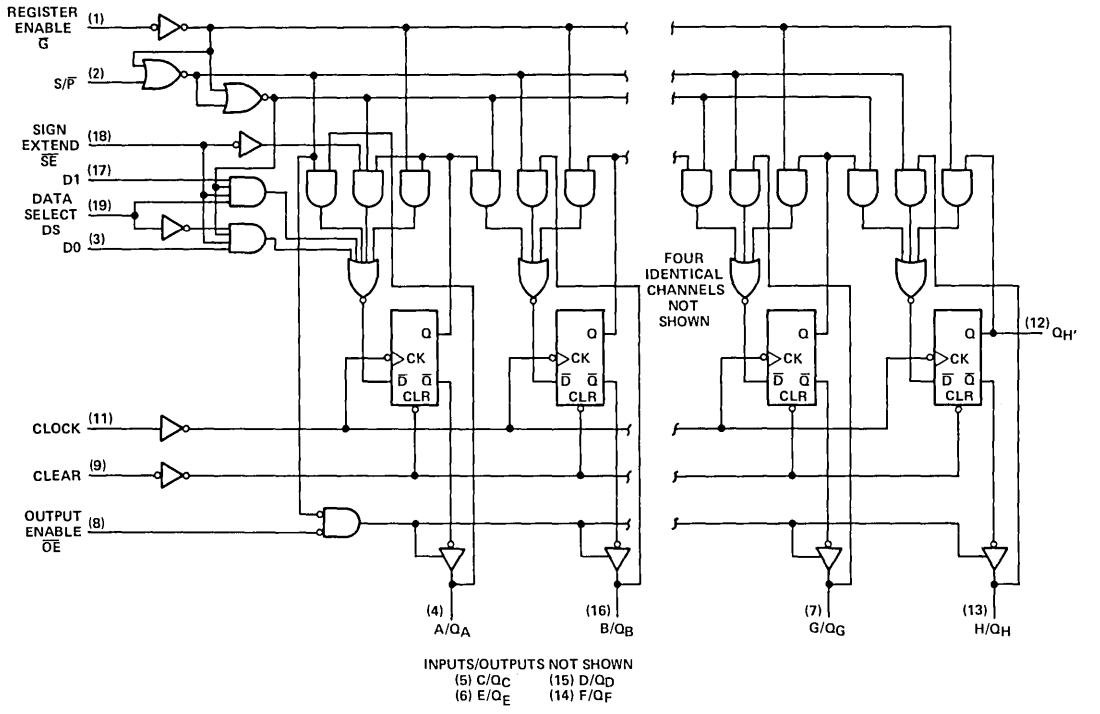
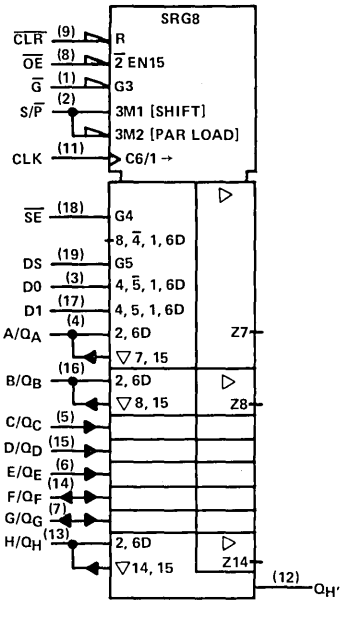
functional block diagram (positive logic)



logic symbol



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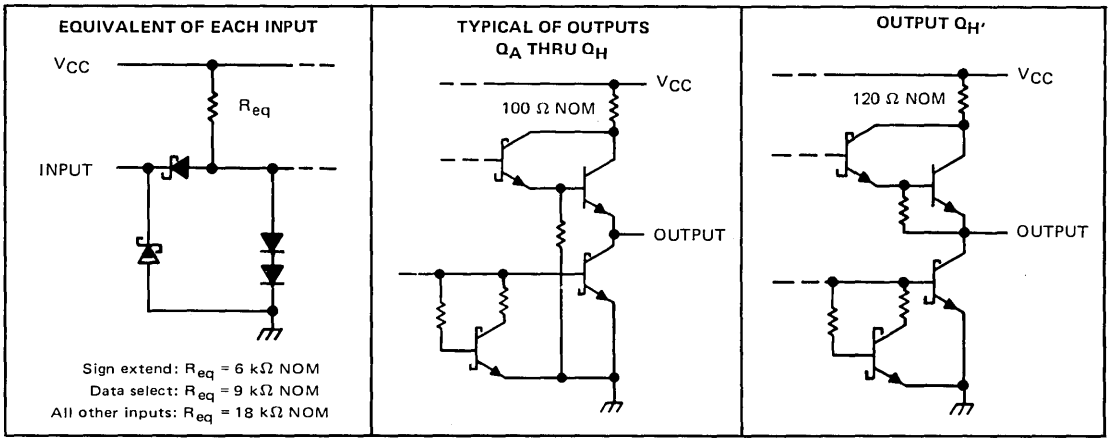
schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54LS322A . . . . . −55°C to 125°C
SN74LS322A . . . . . 0°C to 70°C
Storage temperature . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS322A			SN74LS322A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	Q_A thru Q_H			−1			−2.6	mA
	Q_H'			−0.4			−0.4	
Low-level output current, I_{OL}	Q_A thru Q_H			12			24	mA
	Q_H'			4			8	
Clock frequency, f_{clock}		0		25	0		25	MHz
Width of clock pulse, $t_{w(clock)}$	Clock high	30			30			ns
	Clock low	10			10			
Width of clear pulse, $t_{w(clear)}$	Clear low	20			20			ns
Setup time, t_{su}	Data select	10↑			10↑			ns
	High-level data◇	20↑			20↑			
	Low-level data◇	20↑			20↑			
	Clear inactive-state	20↑			20↑			
Hold time, t_h	Data select	10↑			10↑			ns
	Data◇	0↑			0↑			
Operating free-air temperature, T_A		−55		125	0		70	°C

◇Data includes the two serial inputs and the eight input/output data lines.
↑The arrow indicates that the rising edge of the clock pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS322A MIN	SN54LS322A TYP‡	SN54LS322A MAX	SN74LS322A MIN	SN74LS322A TYP‡	SN74LS322A MAX	UNIT
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	Q_A thru Q_H	V_{CC} = MIN,	V_{IH} = 2 V,	2.4	3.2		2.4	3.1		V
		Q_H'	V_{IL} = V_{IL}max,	I_{OH} = MAX	2.5	3.4		2.7	3.4		
V_{OL}	Low-level output voltage	Q_A thru Q_H	V_{CC} = MIN,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			V_{IH} = 2 V,	I_{OL} = 24 mA					0.35	0.5	
		Q_H'	V_{IL} = V_{IL}max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
				I_{OL} = 8 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	Q_A thru Q_H	V_{CC} = MAX, V_O = 2.7 V	V_{IH} = 2 V,			40			40	μA
I_{OZL}	Off-state output current, low-level voltage applied	Q_A thru Q_H	V_{CC} = MAX, V_O = 0.4 V	V_{IH} = 2 V,			−400			−400	μA
I_I	Input current at maximum input voltage	A thru H	V_{CC} = MAX	V_I = 5.5 V			0.1			0.1	mA
		Data select		V_I = 7 V			0.2			0.2	
		Sign extend		V_I = 7 V			0.3			0.3	
		Any other		V_I = 7 V			0.1			0.1	
I_{IH}	High-level input current	A thru H, DS	V_{CC} = MAX,	V_I = 2.7 V			40			40	μA
		Sign extend					60			60	
		Any other					20			20	
I_{IL}	Low-level input current	Data select	V_{CC} = MAX,	V_I = 0.4 V			−0.8			−0.8	mA
		Sign extend					−1.2			−1.2	
		Any other					−0.4			−0.4	
I_{OS}	Short-circuit output current§	Q_A thru Q_H	V_{CC} = MAX		−30		−130	−30		−130	mA
		Q_H'			−20		−100	−20		−100	
I_{CC}	Supply current		V_{CC} = MAX			35	60		35	60	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			See Note 2	25	35		MHz
t_{PLH}	Clock	Q_H'	C_L = 15 pF, R_L = 2 kΩ, See Note 2		22	33	ns
t_{PHL}					26	35	
t_{PHL}	Clear	Q_H'			27	35	ns
t_{PLH}	Clock	Q_A thru Q_H	C_L = 45 pF, R_L = 665 Ω, See Note 2		16	25	ns
t_{PHL}					22	33	
t_{PHL}	Clear	Q_A thru Q_H			22	35	ns
t_{PZH}	Output enable	Q_A thru Q_H			15	35	ns
t_{PZL}					15	35	
t_{PHZ}	Output enable	Q_A thru Q_H	C_L = 5 pF, R_L = 665 Ω, See Note 2		15	25	ns
t_{PLZ}					15	25	

¶ f_{max} ≡ maximum clock frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
t_{PHZ} ≡ output disable time from high level
t_{PLZ} ≡ output disable time from low level

NOTE 2: For testing f_{max}, all outputs are loaded simultaneously, each with C_L and R_L as specified for the propagation times. See load circuits and waveforms on page 3-11 of *The TTL Data Book For Design Engineers*, Second Edition, LCC4112.

TEXAS INSTRUMENTS
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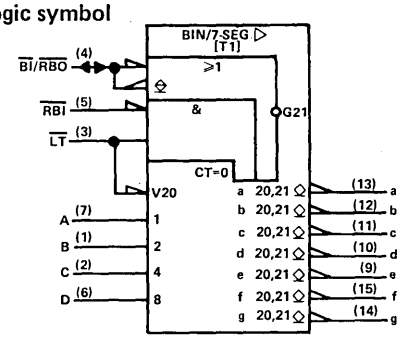
TYPES SN54LS347, SN74LS347
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

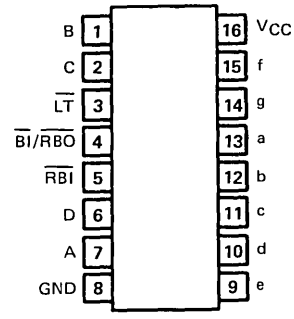
D2426, NOVEMBER 1977

- Low-Voltage Version of SN54LS47/SN74LS47
- Open-Collector Outputs Drive Indicators Directly
- Lamp-Test Provision
- Leading/Trailing Zero Suppression
- Lamp Intensity Modulation Capability

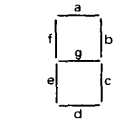
logic symbol



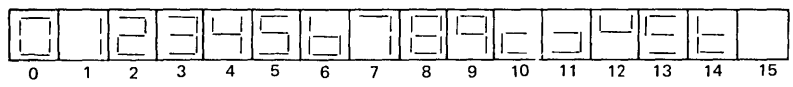
(TOP VIEW)



TYPE	DRIVER OUTPUTS				TYPICAL POWER DISSIPATION	PACKAGES
	ACTIVE LEVEL	OUTPUT CONFIGURATION	SINK CURRENT	MAX VOLTAGE		
SN54LS347	low	open-collector	12 mA	7 V	35 mW	J, W
SN74LS347	low	open-collector	24 mA	7 V	35 mW	J, N



SEGMENT IDENTIFICATION



FONT TABLE T1 – NUMERICAL DESIGNATIONS AND RESULTANT DISPLAYS

FUNCTION TABLE

DECIMAL OR FUNCTION	INPUTS						BI/RBO†	OUTPUTS							NOTE
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	ON	ON	ON	ON	ON	ON	OFF	1
1	H	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF	
2	H	X	L	L	H	L	H	ON	ON	OFF	ON	ON	OFF	ON	
3	H	X	L	L	H	H	H	ON	ON	ON	ON	OFF	OFF	ON	
4	H	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON	
5	H	X	L	H	L	H	H	ON	OFF	ON	ON	OFF	ON	ON	
6	H	X	L	H	H	L	H	OFF	OFF	ON	ON	ON	ON	ON	
7	H	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF	
8	H	X	H	L	L	L	H	ON	ON	ON	ON	ON	ON	ON	
9	H	X	H	L	L	H	H	ON	ON	ON	OFF	OFF	ON	ON	
10	H	X	H	L	H	L	H	OFF	OFF	OFF	ON	ON	OFF	ON	
11	H	X	H	L	H	H	H	OFF	OFF	ON	ON	OFF	OFF	ON	
12	H	X	H	H	L	L	H	OFF	ON	OFF	OFF	OFF	ON	ON	
13	H	X	H	H	L	H	H	ON	OFF	OFF	ON	OFF	ON	ON	
14	H	X	H	H	H	L	H	OFF	OFF	OFF	ON	ON	ON	ON	
15	H	X	H	H	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
BI	X	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	2
RBI	H	L	L	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	3
LT	L	X	X	X	X	X	H	ON	ON	ON	ON	ON	ON	ON	4

H = high level, L = low level, X = irrelevant

NOTES: 1. The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple blanking input (RBI) must be open or high if blanking of a decimal zero is not desired.
2. When a low logic level is applied directly to the blanking input (BI), all segment outputs are off regardless of the level of any other input.
3. When ripple-blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go off and the ripple blanking output (RBO) goes to a low level (response condition).
4. When the blanking input/ripple blanking output (BI/RBO) is open or held high and a low is applied to the lamp-test input, all segment outputs are on.

†BI/RBO is wire AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Peak output current ($t_w \leq 1$ ms, duty cycle $\leq 10\%$) . . . . . 200 mA
Current forced into any output in the off state . . . . . 1 mA
Operating free-air temperature range: SN54LS347 . . . . . −55°C to 125°C
SN74LS347 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS347			SN74LS347			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Off-state output voltage, $V_{O(off)}$	a thru g			7			7	V
On-state output current, $I_{O(on)}$	a thru g			12			24	mA
High-level output current, I_{OH}	BI/RBO			−50			−50	μA
Low-level output current, I_{OL}	BI/RBO			1.6			3.2	mA
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS347			SN74LS347			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	BI/RBO	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, I_{OH} = −50 μA	2.4	4.2		2.4	4.2		V
V_{OL}	Low-level output voltage	BI/RBO	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 1.6 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 3.2 mA					0.35	0.5	
$I_{O(off)}$	Off-state output current	a thru g	V_{CC} = MAX, V_{IL} = V_{IL} max,	V_{IH} = 2 V, $V_{O(off)}$ = 7 V			250			250	μA
$V_{O(on)}$	On-state output voltage	a thru g	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = V_{IL} max	$I_{O(on)}$ = 12 mA		0.25	0.4		0.25	0.4	V
				$I_{O(on)}$ = 24 mA					0.35	0.5	
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current	Any input except BI/RBO	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
		BI/RBO					−1.2			−1.2	
I_{OS}	Short-circuit output current	BI/RBO	V_{CC} = MAX		−0.3		−2	−0.3		−2	mA
I_{CC}	Supply current		V_{CC} = MAX,	See Note 2		7	13		7	13	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: I_{CC} is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{off}	Turn-off time from A input	C_L = 15 pF, R_L = 665 Ω, See Note 4			100	ns
t_{on}	Turn-on time from A input				100	
t_{off}	Turn-off time from RBI input				100	ns
t_{on}	Turn-on time from RBI input				100	

NOTE 4: Load circuit and voltage waveforms are shown on page 3-11 of *The TTL Data Book for Design Engineers*, Second Edition, LCC4112; t_{off} corresponds to t_{PLH} and t_{on} corresponds to t_{PHL}.

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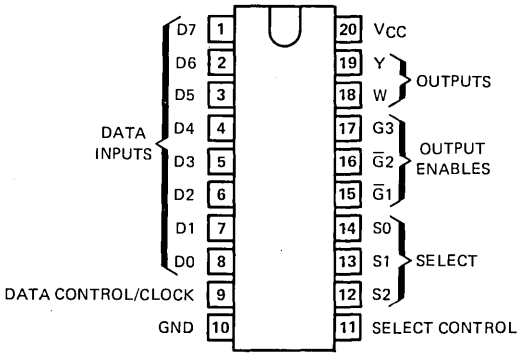
TYPES SN54LS354, SN54LS355, SN54LS356, SN54LS357, SN74LS354, SN74LS355, SN74LS356, SN74LS357
8-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS/REGISTERS

D2544, JULY 1979

- Transparent Latches on Data Select Inputs
- Choice of Data Registers:
  Transparent ('LS354, 'LS355)
  Edge-Triggered ('LS356, 'LS357)
- Choice of Outputs:
  Three-State ('LS354, 'LS356)
  Open-Collector ('LS355, 'LS357)
- Complementary Outputs
- Easily Expandable
- High-Density 20-Pin Package

SN54LS' . . . J PACKAGE
SN74LS' . . . J OR N PACKAGE
(TOP VIEW)



description

These monolithic data selectors/multiplexers contain full on-chip binary decoding to select one of eight data sources. The data-select address is stored in transparent latches that are enabled by a low level on pin 11, $\overline{SC}$. On the 'LS354 and 'LS355 a similar enable for data is obtained by a low level on pin 9, $\overline{DC}$. The edge-triggered data registers of the 'LS356 and 'LS357 are clocked by a low-to-high transition on pin 9, CLK. Complementary outputs are available in either three-state versions ('LS354 and 'LS356) or open-collector versions ('LS355 and 'LS357).

The SN54LS354 through SN54LS357 are characterized for operation over the full military temperature range of −55°C to 125°C; the SN74LS354 through SN74LS357 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS								OUTPUTS	
SELECT†			DATA CONTROL ('LS354, 'LS355)	CLOCK ('LS356, 'LS357)	OUTPUT ENABLES				
S2	S1	S0			$\overline{G1}$	$\overline{G2}$	G3	W	Y
X	X	X	X	X	H	X	X	Z	Z
X	X	X	X	X	X	H	X	Z	Z
X	X	X	X	X	X	X	L	Z	Z
L	L	L	L	↑	L	L	H	$\overline{D0}$	D0
L	L	L	H	H or L	L	L	H	$\overline{D0}_n$	$D0_n$
L	L	H	L	↑	L	L	H	$\overline{D1}$	D1
L	L	H	H	H or L	L	L	H	$\overline{D1}_n$	$D1_n$
L	H	L	L	↑	L	L	H	$\overline{D2}$	D2
L	H	L	H	H or L	L	L	H	$\overline{D2}_n$	$D2_n$
L	H	H	L	↑	L	L	H	$\overline{D3}$	D3
L	H	H	H	H or L	L	L	H	$\overline{D3}_n$	$D3_n$
H	L	L	L	↑	L	L	H	$\overline{D4}$	D4
H	L	L	H	H or L	L	L	H	$\overline{D4}_n$	$D4_n$
H	L	H	L	↑	L	L	H	$\overline{D5}$	D5
H	L	H	H	H or L	L	L	H	$\overline{D5}_n$	$D5_n$
H	H	L	L	↑	L	L	H	$\overline{D6}$	D6
H	H	L	H	H or L	L	L	H	$\overline{D6}_n$	$D6_n$
H	H	H	L	↑	L	L	H	$\overline{D7}$	D7
H	H	H	H	H or L	L	L	H	$\overline{D7}_n$	$D7_n$

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
Z = high-impedance state (off state)
↑ = transition from low to high level
D0 . . . D7 = the level of steady-state inputs at inputs D0 through D7, respectively, at the time of the low-to-high clock transition in the case of 'LS356 and 'LS357
$D0_n$ . . . $D7_n$ = the level of steady state inputs at inputs D0 through D7, respectively, before the most recent low-to-high transition of data control or clock
† This column shows the input address setup with $\overline{SC}$ low.

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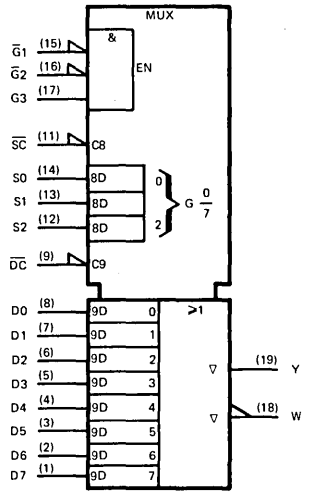
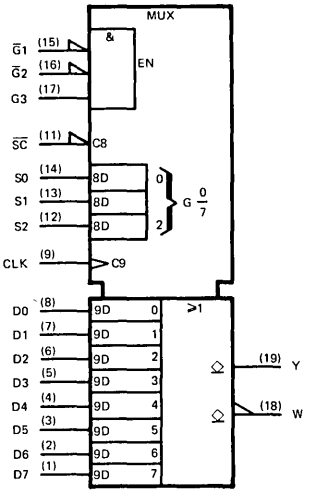
logic symbols†

'LS354
('LS355 is open-collector version)

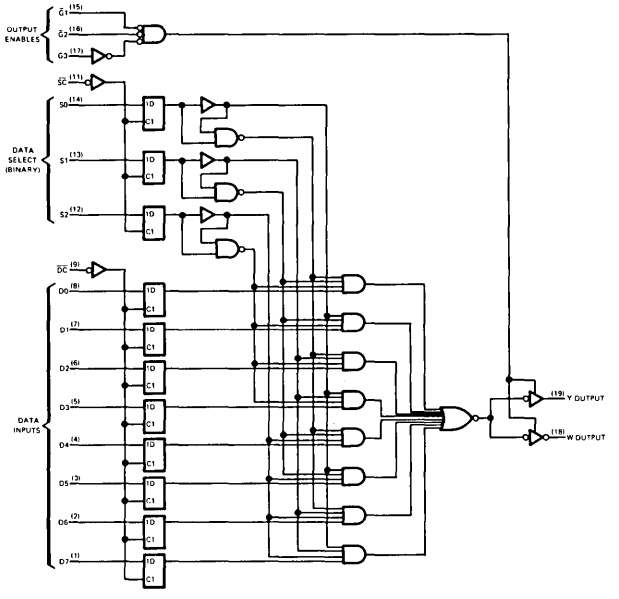


'LS357
('LS356 is 3-state version)

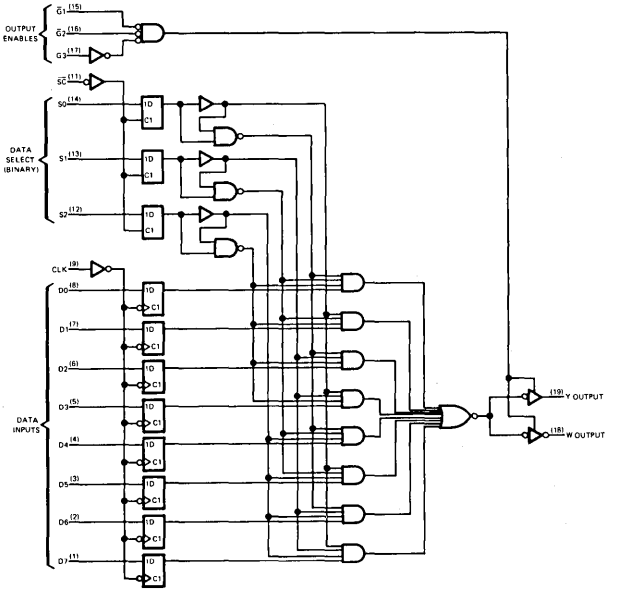


functional block diagrams (positive logic)

'LS354, 'LS355



'LS356, 'LS357



†These symbols are in accordance with IEEE Std 91/ANSI Y32.14 and current discussions in IEC and IEEE.

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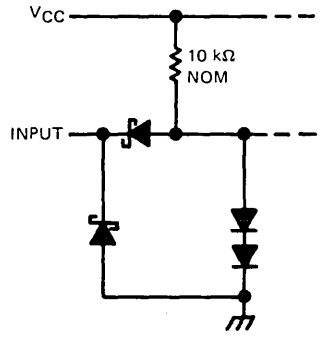
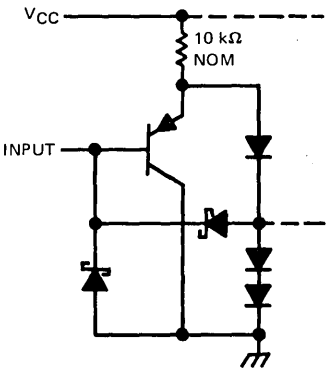
schematics of inputs and outputs

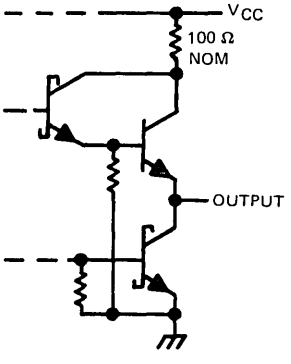
EQUIVALENT OF EACH DATA OR SELECT INPUT



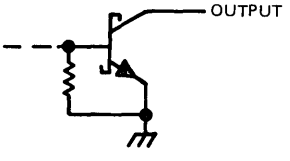
EQUIVALENT OF ALL OTHER INPUTS



TYPICAL OF BOTH OUTPUTS ON 'LS354 AND 'LS356



TYPICAL OF BOTH OUTPUTS ON 'LS355 AND 'LS357



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage (see Note 1)		7 V
Input voltage		7 V
Operating free-air temperature range:	SN54LS'	−55°C to 125°C
	SN74LS'	0°C to 70°C
Storage temperature range		−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS354, SN54LS356			SN74LS354, SN74LS356			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}				5.5			5.5	V
High-level output current, I_{OH}				−1			−2.6	mA
Low-level output current, I_{OL}				12			24	mA
Setup times, high- or low-level data, t_{su} (with respect to ↑ at pin 9)	'LS354	15			15			ns
	'LS356	15			15			
Hold times, high- or low-level data, t_h (with respect to ↑ at pin 9)	'LS354	15			15			ns
	'LS356	0			0			
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†			SN54LS354, SN54LS356			SN74LS354, SN74LS356			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage					2			2			V
V_{IL}	Low-level input voltage							0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, I_{OH} = MAX	V_{IH} = 2 V,	V_{IL} = V_{IL} max,	2.4			2.4			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = V_{IL} max	V_{IH} = 2 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
					I_{OL} = 24 mA					0.35	0.5	
I_{OZ}	Off-state (high-impedance state) output current		V_{CC} = MAX		V_O = 2.7 V			20			20	μA
					V_O = 0.4 V			−20			−20	
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	$\overline{DC}$ or CLK, $\overline{G1}$, $\overline{G2}$, G3	V_{CC} = MAX,	V_I = 0.4 V				−0.2			−0.2	mA
		All others						−0.4			−0.4	
I_{OS}	Short-circuit output current§		V_{CC} = MAX			−30		−130	−30		−130	mA
I_{CC}	Supply current		V_{CC} = MAX,	See Note 2			29	46		29	46	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 2: I_{CC} is measured with the inputs grounded and the outputs open.

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switching characteristics, V_{CC} = 5 V, T_A = 25°C, R_L = 667 Ω

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS354			'LS356			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	D0-D7	Y	C_L = 45 pF, See Note 3		24	36				ns
t_{PHL}					23	35				
t_{PLH}		W			18	27				ns
t_{PHL}					29	44				
t_{PLH}	$\overline{DC}$ or CLK	Y			28	42		18	27	ns
t_{PHL}					26	39		33	50	
t_{PLH}		W			22	33		24	36	ns
t_{PHL}					33	50		18	27	
t_{PLH}	S0, S1, S2	Y			29	44		30	45	ns
t_{PHL}					24	36		28	42	
t_{PLH}		W			28	42		36	54	ns
t_{PHL}					34	51		30	45	
t_{PLH}	$\overline{SC}$	Y			34	51		36	54	ns
t_{PHL}					31	47		40	60	
t_{PLH}		W			27	41		32	48	ns
t_{PHL}					40	60		36	54	
t_{PZH}	$\overline{G1}$, $\overline{G2}$	Y			14	27		14	25	ns
t_{PZL}					18	27		17	25	
t_{PHZ}			C_L = 5 pF, See Note 3		15	23		16	24	ns
t_{PLZ}					15	23		16	24	
t_{PZH}		W	C_L = 45 pF, See Note 3		12	24		14	23	ns
t_{PZL}					16	24		16	23	
t_{PHZ}			C_L = 5 pF, See Note 3		15	23		16	23	ns
t_{PLZ}					15	23		16	23	
t_{PZH}	G3	Y	C_L = 45 pF, See Note 3		15	29		15	27	ns
t_{PZL}					19	29		18	27	
t_{PHZ}			C_L = 5 pF, See Note 3		15	23		16	25	ns
t_{PLZ}					15	23		16	25	
t_{PZH}		W	C_L = 45 pF, See Note 3		13	25		14	25	ns
t_{PZL}					17	25		16	25	
t_{PHZ}			C_L = 5 pF, See Note 3		15	23		16	25	ns
t_{PLZ}					15	23		16	25	

¶ t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
t_{PHZ} ≡ output disable time from high level
t_{PLZ} ≡ output disable time from low level

NOTE 3: Load circuit and waveforms are shown on page 3-11 of *The TTL Data Book for Design Engineers*, second edition.

recommended operating conditions

		SN54LS355 SN54LS357			SN74LS355 SN74LS357			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}				5.5			5.5	V
Low-level output current, I_{OL}				12			24	mA
Setup times, high- or low-level data, t_{su} (with respect to ↑ at pin 9)	'LS355	15			15			ns
	'LS357	15			15			
Hold times, high- or low-level data, t_h (with respect to ↑ at pin 9)	'LS355	15			15			ns
	'LS357	0			0			
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS355 SN54LS357			SN74LS355 SN74LS357			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max, V_{OH} = 5.5 V				100			100	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current, $\overline{DC}$ or CLK, $\overline{G}1$, $\overline{G}2$, G3	V_{CC} = MAX, V_I = 0.4 V				−0.2			−0.2	mA
	Low-level input current, All others					−0.4			−0.4	
I_{CC}	Supply current	V_{CC}= MAX, See Note 2			29	46		29	46	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: I_{CC} is measured with the inputs grounded and the outputs open.

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switching characteristics, V_{CC} = 5 V, T_A = 25°C, R_L = 667 Ω

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS355			'LS357			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	D0-D7	Y	C_L = 45 pF, See Note 3		34	41				ns
t_{PHL}					26	39				
t_{PLH}		W			30	45				ns
t_{PHL}					33	50				
t_{PLH}	$\overline{DC}$ or CLK	Y			38	57		27	41	ns
t_{PHL}					31	47		34	51	
t_{PLH}		W			33	50		32	48	ns
t_{PHL}					39	59		23	35	
t_{PLH}	S0, S1, S2	Y			39	59		38	57	ns
t_{PHL}					36	49		40	60	
t_{PLH}		W			32	48		38	57	ns
t_{PHL}					39	58		35	53	
t_{PLH}	$\overline{SC}$	Y			45	68		44	66	ns
t_{PHL}					42	63		41	62	
t_{PLH}		W			44	66		41	62	ns
t_{PHL}					45	68		41	62	
t_{PLH}	$\overline{G}1$, $\overline{G}2$	Y			21	32		18	27	ns
t_{PHL}					22	33		18	27	
t_{PLH}		W			18	27		20	30	ns
t_{PHL}					19	29		21	32	
t_{PZH}	G3	Y			24	36		24	36	ns
t_{PHL}					25	40		24	36	
t_{PLH}		W			19	29		19	29	ns
t_{PHL}					19	29		19	29	

¶ t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output

NOTE 3: Load circuit and waveforms are shown on page 3-11 of *The TTL Data Book for Design Engineers*, second edition.

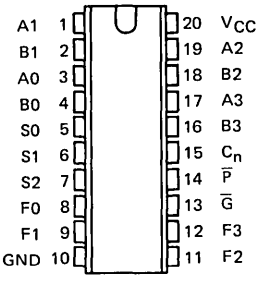
TYPES SN54LS381, SN54LS382, SN74LS381, SN74LS382
ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

D2430, JANUARY 1981

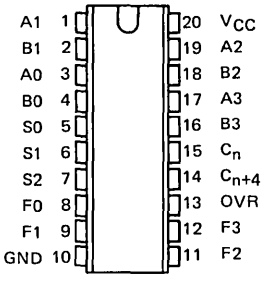
PIN DESIGNATIONS

DESIGNATION	PIN NOS.	FUNCTION
A3, A2, A1, A0	17, 19, 1, 3	WORD A INPUTS
B3, B2, B1, B0	16, 18, 2, 4	WORD B INPUTS
S2, S1, S0	7, 6, 5	FUNCTION-SELECT INPUTS
C_n	15	CARRY INPUT FOR ADDITION, INVERTED CARRY INPUT FOR SUBTRACTION
F3, F2, F1, F0	12, 11, 9, 8	FUNCTION OUTPUTS
$\overline{P}$ ('LS381 ONLY)	14	ACTIVE-LOW CARRY PROPAGATE OUTPUT
$\overline{G}$ ('LS381 ONLY)	13	ACTIVE-LOW CARRY GENERATE OUTPUT
C_{n+4} ('LS382 ONLY)	14	RIPPLE-CARRY OUTPUT
OVR ('LS382 ONLY)	13	OVERFLOW OUTPUT
V_{CC}	20	SUPPLY VOLTAGE
GND	10	GROUND

SN54LS381 . . J PACKAGE
SN74LS381 . . J OR N PACKAGE
(TOP VIEW)



SN54LS382 . . J PACKAGE
SN74LS382 . . J OR N PACKAGE
(TOP VIEW)



- **Fully Parallel 4-Bit ALU's in 20-Pin Package for 0.300-Inch Row Spacing**
- **Ideally Suited for High-Density Economical Processors**
- **'LS381 Features $\overline{G}$ and $\overline{P}$ Outputs for Look-Ahead Carry Cascading**
- **'LS382 Features Ripple Carry ($C_n + 4$) and Overflow (OVR) Outputs**
- **Arithmetic and Logic Operations Selected Specifically to Simplify System Implementation:**
  - **A Minus B**
  - **B Minus A**
  - **A Plus B**
  - **and Five Other Functions**

FUNCTION TABLE

SELECTION			ARITHMETIC/LOGIC
S2	S1	S0	OPERATION
L	L	L	CLEAR
L	L	H	B MINUS A
L	H	L	A MINUS B
L	H	H	A PLUS B
H	L	L	A ⊕ B
H	L	H	A + B
H	H	L	AB
H	H	H	PRESET

H = high level, L = low level

description

The 'LS381 and 'LS382 are low-power Schottky TTL arithmetic logic units (ALUs)/function generators that perform eight binary arithmetic/logic operations on two 4-bit words as shown in the function table. The exclusive-OR, AND, or OR function of the two Boolean variables is provided without the use of external circuitry. Also, the outputs can be cleared (low) or preset (high) as desired. The 'LS381 provides two cascade outputs ($\overline{P}$ and $\overline{G}$) for expansion utilizing SN54S182/SN74S182 look-ahead carry generators. The 'LS382 provides a $C_n + 4$ output to ripple the carry to the C_n input of the next stage. The 'LS382 detects and indicates two's complement overflow condition via the OVR output. The overflow output is logically equivalent to $C_n + 3 \oplus C_n + 4$. When the 'LS382 is cascaded to handle word lengths longer than four bits in length, only the most significant overflow (OVR) output is used.

The SN54LS381 and SN54LS382 will be characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LS381 and SN74LS382 will be characterized for operation from 0°C to 70°C.

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function table

Certain differences exist in the $\overline{G}$, $\overline{P}$ ('LS381) and OVR, C_{n+4} ('LS382) function table compared with similar parts from other vendors. No differences exist in the arithmetic modes (B minus A, A minus B, and A plus B), where these outputs perform valuable cascade functions.

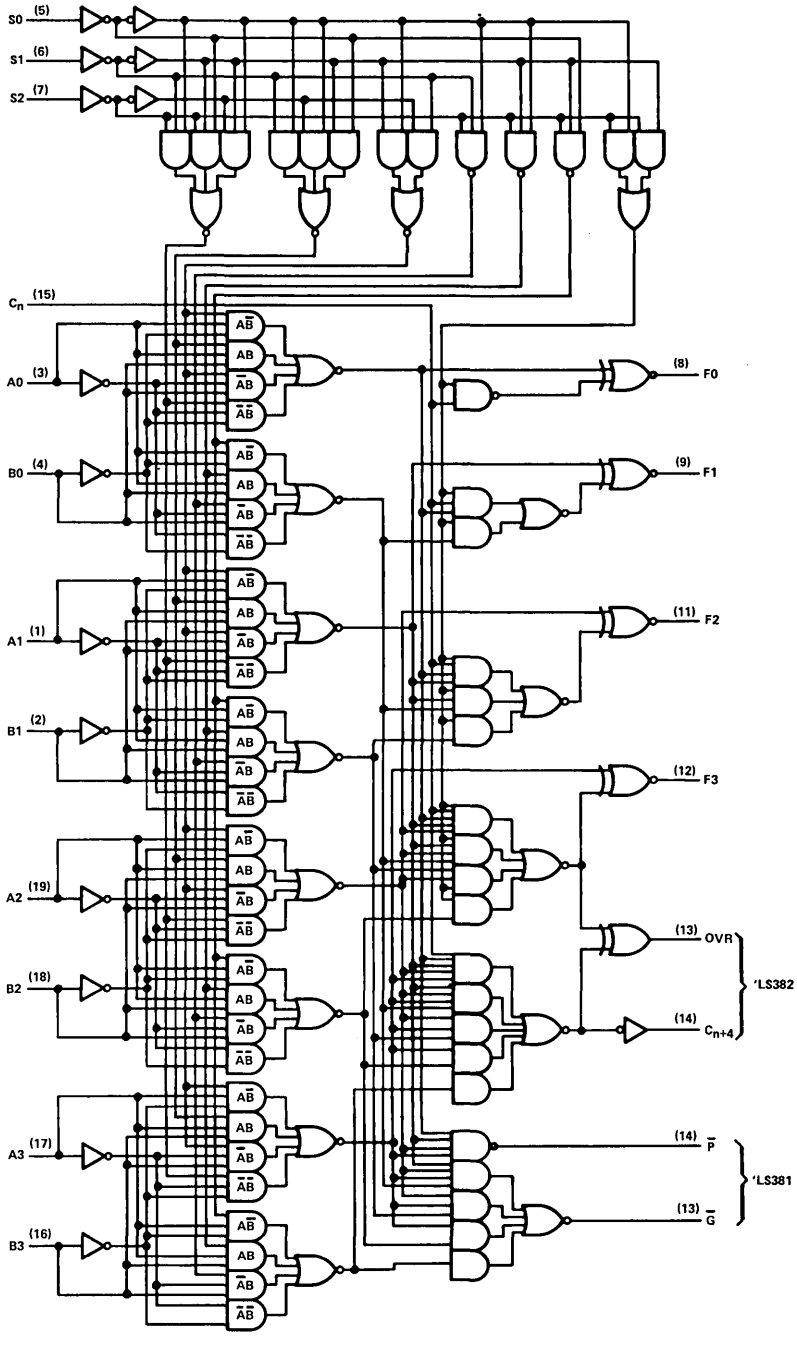
There are slight differences in the other modes (CLEAR, A + B, A ⊕ B, AB, and PRESET), where these outputs are strictly "don't care."

This function table is a condensed version and assumes for A_n that A0, A1, A2, and A3 inputs all agree and for B_n that B0, B1, B2, and B3 inputs all agree. This table is intended to point out the response of these $\overline{G}$, $\overline{P}$ ('LS381) and OVR, C_{n+4} ('LS382) outputs in all modes of operation to facilitate incoming inspection.

FUNCTION TABLE

ARITHMETIC/LOGIC OPERATION	INPUTS						OUTPUTS				('LS381)		('LS382)	
	S2	S1	S0	C_n	A_n	B_n	F3	F2	F1	F0	$\overline{G}$	$\overline{P}$	OVR	C_{n+4}
CLEAR	L	L	L	X	X	X	L	L	L	L	H	H	L	L
B MINUS A	L	L	H	L	L	L	H	H	H	H	H	L	L	L
				L	L	H	H	H	H	L	L	H	L	H
				L	H	L	L	L	L	L	H	H	L	L
				L	H	H	H	H	H	H	H	L	L	L
				H	L	L	L	L	L	L	H	L	L	H
				H	L	H	H	H	H	H	L	H	L	H
				H	H	L	L	L	L	H	H	H	L	L
				H	H	H	L	L	L	L	H	L	L	H
A MINUS B	L	H	L	L	L	L	H	H	H	H	H	L	L	L
				L	L	H	L	L	L	L	H	H	L	L
				L	H	L	H	H	H	L	L	H	L	H
				L	H	H	H	H	H	H	H	L	L	L
				H	L	L	L	L	L	L	H	L	L	H
				H	L	H	L	L	L	H	H	H	L	L
				H	H	L	H	H	H	H	L	H	L	H
				H	H	H	L	L	L	L	H	L	L	H
A PLUS B	L	H	H	L	L	L	L	L	L	L	H	H	L	L
				L	L	H	H	H	H	H	H	L	L	L
				L	H	L	H	H	H	H	H	L	L	L
				L	H	H	H	H	H	L	L	H	L	H
				H	L	L	L	L	L	H	H	H	L	L
				H	L	H	L	L	L	L	H	L	L	H
				H	H	L	L	L	L	L	H	L	L	H
				H	H	H	H	H	H	H	L	H	L	H
A ⊕ B	H	L	L	X	L	L	L	L	L	L	H	H	L	L
				L	L	H	H	H	H	H	H	L	L	L
				H	L	H	H	H	H	H	H	L	H	H
				L	H	L	H	H	H	H	H	L	L	L
				H	H	L	H	H	H	H	H	L	H	H
				X	H	H	L	L	L	L	H	H	L	L
A + B	H	L	H	X	L	L	L	L	L	L	H	H	L	L
				L	L	H	H	H	H	H	H	L	L	L
				H	L	H	H	H	H	H	H	L	H	H
				L	H	L	H	H	H	H	H	L	L	L
				H	H	L	H	H	H	H	H	L	H	H
				L	H	H	H	H	H	H	H	L	L	L
				H	H	H	H	H	H	H	H	L	H	H
AB	H	H	L	X	L	L	L	L	L	L	H	H	L	L
				X	L	H	L	L	L	L	H	H	L	L
				X	H	L	L	L	L	L	H	H	L	L
				L	H	H	H	H	H	H	H	L	L	L
				H	H	H	H	H	H	H	H	L	H	H
PRESET	H	H	H	L	X	X	H	H	H	H	H	L	L	L
				H	X	X	H	H	H	H	H	L	H	H

functional block diagram (positive logic)



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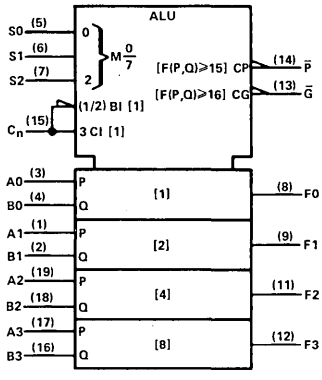
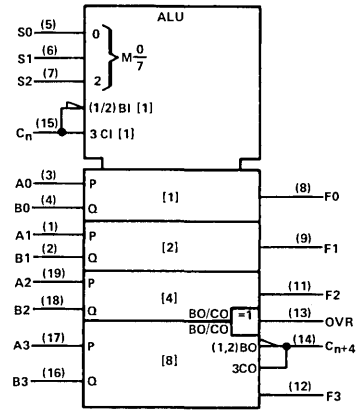
logic symbols

'LS381

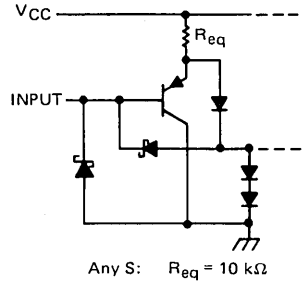


'LS382



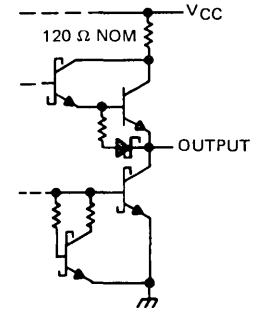
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



Any S: R_{eq} = 10 kΩ
C_n ('LS381): R_{eq} = 2.5 kΩ
All others: R_{eq} = 2 kΩ

TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS381, SN54LS382 . . . . . −55°C to 125°C
SN74LS381, SN74LS382 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−400			−400	μA
Low-level output current, I_{OL}	$\overline{G}$ output of 'LS381			16			16	mA
	All other outputs			4			8	
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, I_{OH} = −400 μA	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	$\overline{G}$ ('LS381)	V_{CC} = MIN,	I_{OL} = 16 mA		0.47	0.7		0.47	0.7	V
		Other outputs	V_{IH} = 2 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
			V_{IL} = V_{IL} max	I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
I_{IH}	High-level input current	Any S	V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
		Any A or B					100			100	
		C_n ('LS381)					80			80	
		C_n ('LS382)					100			100	
I_{IL}	Low-level input current	Any S	V_{CC} = MAX,	V_I = 0.4 V			−0.2			−0.2	mA
		Any A or B					−1			−1	
		C_n ('LS381)					−0.8			−0.8	
		C_n ('LS382)					−0.8			−0.8	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current		V_{CC} = MAX, All inputs grounded, Outputs open			35	65		35	65	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS381			'LS382			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	C_n	Any F	R_L = 2 kΩ, C_L = 15 pF		18	27		18	27	ns
t_{PHL}					14	21		14	21	
t_{PLH}	Any A or B	$\overline{G}$			20	30				ns
t_{PHL}					21	33				
t_{PLH}	Any A or B	$\overline{P}$			21	33				ns
t_{PHL}					23	33				
t_{PLH}	A_i or B_i	F_i			20	30		20	30	ns
t_{PHL}					15	23		15	23	
t_{PLH}	S_i	F_i			35	53		35	53	ns
t_{PHL}					34	51		34	51	
t_{PLH}	S_i	$\overline{G}$ or $\overline{P}$			31	47				ns
t_{PHL}					32	48				
t_{PLH}	Any A or B	C_{n+4}						28	42	ns
t_{PHL}								26	39	
t_{PLH}	Any A or B	OVR						23	35	ns
t_{PHL}								27	41	
t_{PLH}	S_i	C_{n+4} or OVR						38	57	ns
t_{PHL}								36	54	
t_{PLH}	C_n	OVR						10	15	ns
t_{PHL}								13	23	
t_{PLH}	C_n	C_{n+4}						13	21	ns
t_{PHL}								11	20	

TEXAS INSTRUMENTS
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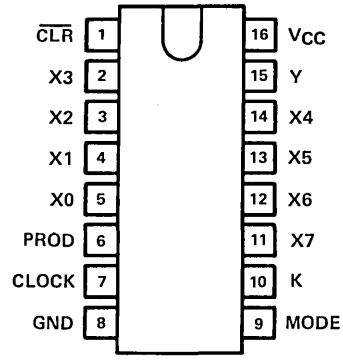
TYPES SN54LS384, SN74LS384
8-BIT BY 1-BIT TWO'S-COMPLEMENT MULTIPLIERS

D2419, JANUARY 1981

- Two's-Complement Multiplication
- Magnitude Only Multiplication
- Cascadable for Any Number of Bits
- 8-Bit Parallel Multiplicand Data Input
- Serial Multiplier Data Input
- Serial Data Output for Multiplication Product
- 40 MHz Typical Maximum Clock Frequency

SN54LS384 . . . J OR W PACKAGE
SN74LS384 . . . J OR N PACKAGE
(TOP VIEW)

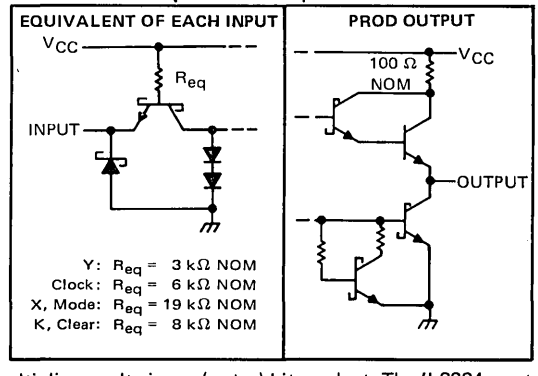


description

The 'LS384 is an 8-bit by 1-bit sequential logic element that performs digital multiplication of two numbers represented in two's-complement form to produce a two's-complement product without external correction by using Booth's algorithm internally. The device accepts an 8-bit multiplicand (X input) and stores this data in eight internal latches. These X latches are controlled via the clear input. When the clear input is low, all internal flip-flops are cleared and the X latches are opened to accept new multiplicand data. When the clear input is high, the latches are closed and are insensitive to X input changes.

The multiplier word data is passed by the Y input in a serial bit stream, least significant bit first. The product is clocked out the PROD output, least significant bit first.

schematics of inputs and outputs



The multiplication of an m-bit multiplicand by an n-bit multiplier results in an (m + n)-bit product. The 'LS384 must be clocked for m + n clock cycles to produce this two's complement product. The n-bit multiplier (Y-input) sign bit data must be extended for the remaining m bits to complete the multiplication cycle.

The device also contains a K input so that devices can be cascaded for longer length X words. The PROD output of one device is connected to the K input of the succeeding device when cascading. The mode input is used to indicate which device contains the most significant bit. The mode input is wired high or low depending on the position of the 8-bit slice in the total X word length. The device with the most significant bit is wired low and all lower order bit packages are wired high.

The SN54LS384 will be characterized for operation over the full military temperature range from −55°C to 125°C. The SN74LS384 will be characterized for operation from 0°C to 70°C.

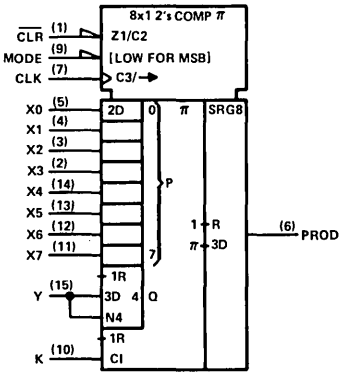
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

FUNCTION TABLE

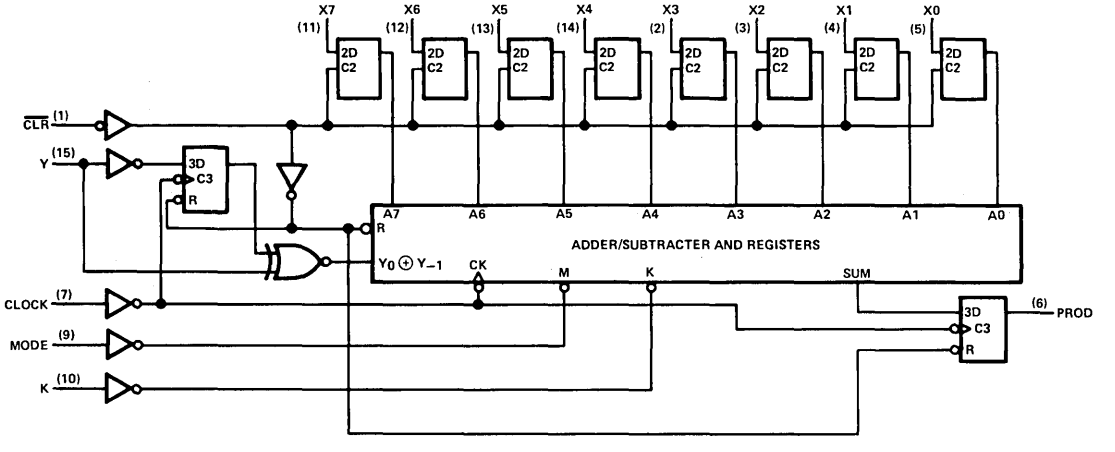
INPUTS				INTERNAL	OUTPUT	FUNCTION
$\overline{CLR}$	CLK	X_i	Y	Y_{-1}	PROD	
L	X	Data	X	L	L	Load new multiplicand and clear internal sum and carry registers
H	↑	X	L	L	Output	Shift sum register
H	↑	X	L	H	per	Add multiplicand to sum register and shift
H	↑	X	H	L	Booth's	Subtract multiplicand from sum register and shift
H	↑	X	H	H	algorithm	Shift sum register

H = high-level, L = low-level, X = irrevelant, ↑ = low-to-high-level transition

logic symbol



functional block diagram (positive logic)



TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54LS384 . . . . . −55°C to 125°C
SN74LS384 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input voltages must be zero or positive with respect to network ground terminal.

recommended operating conditions

		SN54LS384			SN74LS384			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−400			−400	μA
Low-level output current, I_{OL}				4			8	mA
Clock frequency, f_{clock}		0		25	0		25	MHz
Setup time, t_{su}	Y before Clock ↑	45			38			ns
	K before Clock ↑	30			24			
	X before Clear ↓	23			19			
Clear inactive-state set up time before Clock ↑		30			20			ns
Hold time, t_h	Y after Clock ↑	0			0			ns
	K after Clock ↑	0			0			
	X after Clear ↓	2			2			
Pulse width, t_w	Clock high	20			20			ns
	Clock low	20			20			
	Clear low	38			33			
Operating free-air temperature, t_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†			SN54LS384			SN74LS384			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage					2			2			V
V_{IL}	Low-level input voltage							0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, V_{OH} = −400 μA		2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = V_{IL} max	V_{IH} = 2 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
					I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current	X, Mode	V_{CC} = MAX,	V_I = 2.7 V				20			20	μA
		K, Clear						30			30	
		Clock						40			40	
		Y						80			80	
I_{IL}	Low-level input current	X, Mode	V_{CC} = MAX,	V_I = 0.4 V				−0.48			−0.48	mA
		K, Clear						−1.2			−1.2	
		Clock						−1.6			−1.6	
		Y						−3.2			−3.2	
I_{OS}	Short-circuit output current§		V_{CC} = MAX			−20		−100	−20		−100	mA
I_{CC}	Supply current		V_{CC} = MAX,	See Note 3			91	155		91	155	mA

†For conditions shown at MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 3: I_{CC} is measured with the clear input grounded and all other inputs and outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency		25	40		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from clock	C_L = 15 pF,		15	23	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock	R_L = 2 kΩ,		15	23	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear	See Note 4		17	25	ns

NOTE 4: Load circuit and waveforms are shown on page 3-11 of the *TTL Data Book for Design Engineers,* second edition, LCC 4112.

TYPICAL APPLICATION DATA

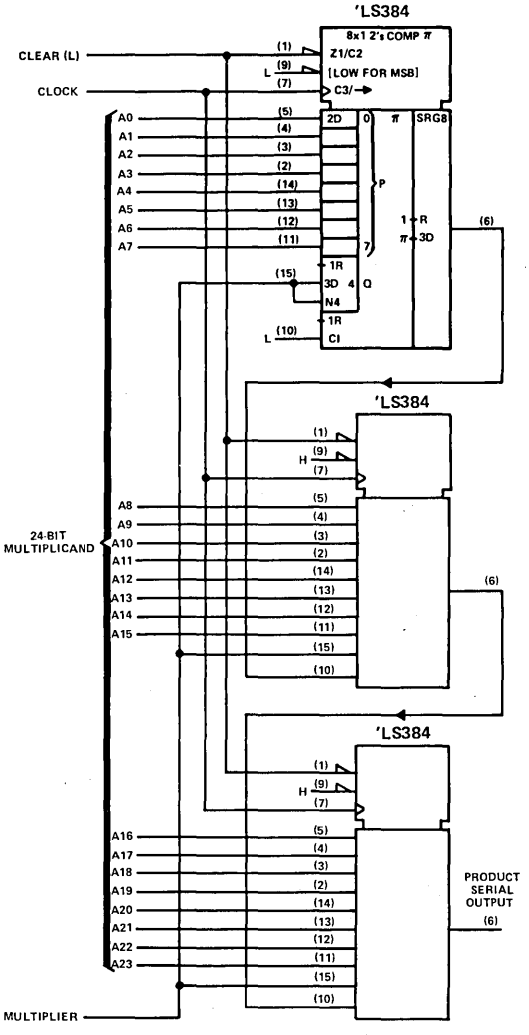

FIGURE 1–BASIC 24-BIT SERIAL/PARALLEL CONNECTION

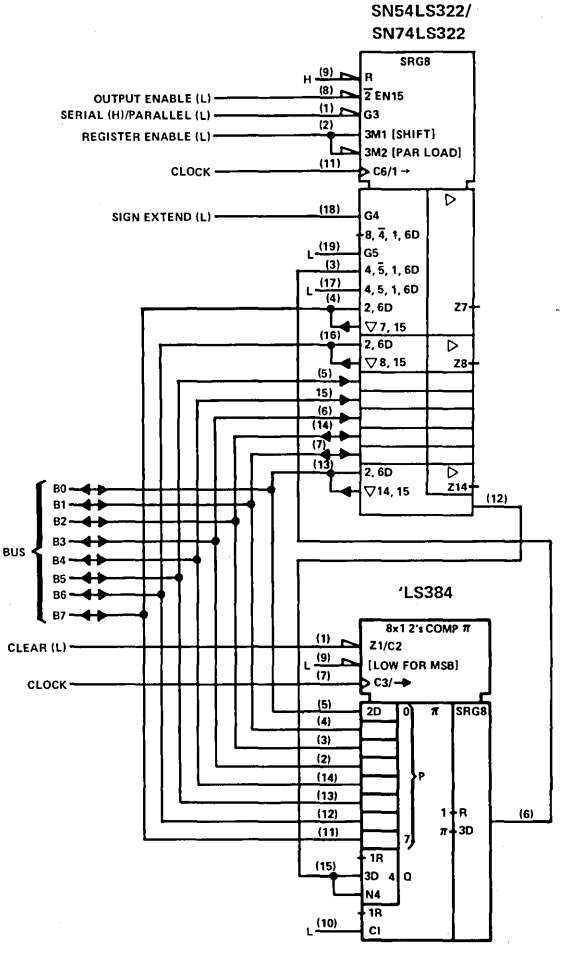

FIGURE 2–8-BIT BY 8-BIT MULTIPLIER, BUS ORGANIZED WITH 8-BIT TRUNCATED PRODUCT

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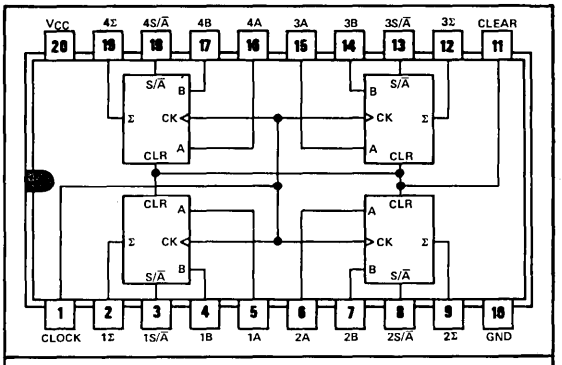
TYPES SN54LS385, SN74LS385
QUADRUPLE SERIAL ADDERS/SUBTRACTORS

D2412, NOVEMBER 1977

- Four Synchronous Elements in a Single 20-Pin Package
- Buffered Clock and Direct Clear Inputs
- Independent Two's-Complement Addition/Subtraction

SN54LS385 . . . J PACKAGE
SN74LS385 . . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

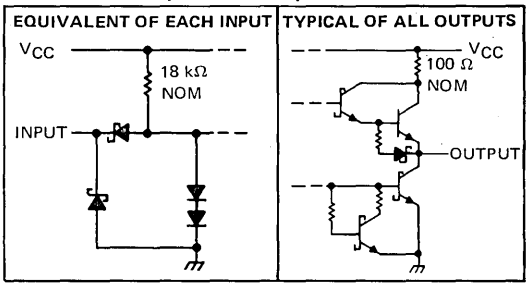
description

The 'LS385 is a general purpose adder/subtractor and is particularly useful as a companion part to the SN54LS384/SN74LS384 serial/parallel two's-complement multiplier. The 'LS385 contains four independent adder/subtractor elements with common clock and clear.

Each of the four independent sum (Σ) outputs reflects its respective A and B input as controlled by the S/Ā control. When S/Ā is high the Σ function is A minus B. When S/Ā is low the Σ function is A plus B.

When low, the clear input asynchronously resets the sum flip-flop low and the carry flip-flop either high in the subtract mode or low in the add mode. The clock is positive-edge triggered and controls the sum and carry flip-flops according to the function table.

schematics of inputs and outputs

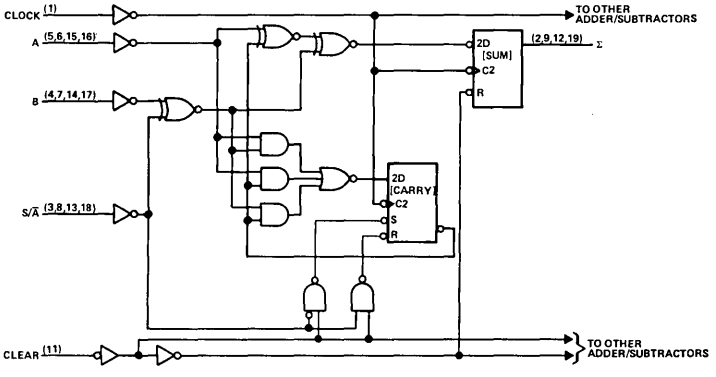


FUNCTION TABLE

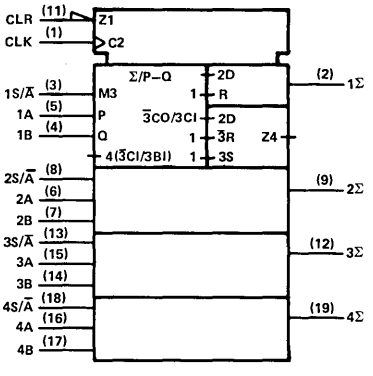
SELECTED FUNCTION	INPUTS CLEAR	S/Ā	A	B	CLOCK	DATA IN CARRY FLIP-FLOP BEFORE ↑	DATA IN CARRY FLIP-FLOP AFTER ↑	Σ OUTPUT AFTER ↑
Clear	L	L	X	X	X	L	L	L
	L	H	X	X	X	H	H	L
Add	H	L	L	L	↑	L	L	L
	H	L	L	L	↑	H	L	H
	H	L	L	H	↑	L	L	H
	H	L	L	H	↑	H	H	L
	H	L	H	L	↑	L	L	H
	H	L	H	L	↑	H	H	L
	H	L	H	H	↑	L	H	L
	H	L	H	H	↑	H	H	H
Subtract	H	H	L	L	↑	L	L	H
	H	H	L	L	↑	H	H	L
	H	H	L	H	↑	L	L	L
	H	H	L	H	↑	H	L	H
	H	H	H	L	↑	L	H	L
	H	H	H	L	↑	H	H	H
	H	H	H	H	↑	L	L	H
	H	H	H	H	↑	H	H	L

H = high level, L = low level, X = irrelevant,
↑ = transition from low to high level at the clock input

functional block diagram (each adder/subtractor, positive logic)



logic symbol



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recommended operating conditions

	SN54LS385			SN74LS385			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Clock frequency, f_{clock}	0		30	0		30	MHz
Width of clock pulse, t_w	16			16			ns
Setup time, t_{su}	10			10			ns
Hold time, t_h	0			0			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS385			SN74LS385			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max, I_{OH} = −400 μA		2.5	3.5		2.7	3.5		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2			48	75		48	75	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with all inputs grounded and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER◇	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			C_L = 15 pF, R_L = 2 kΩ, See Note 3	30	40		MHz
t_{PLH}	Clock	Σ			14	22	ns
t_{PHL}					18	27	
t_{PHL}	Clear	Σ			18	30	ns

◇f_{max} ≡ maximum clock frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 3: Load circuit and voltage waveforms are shown on page 3-11 of *The TTL Data Book for Design Engineers*, Second Edition, LCC4112.

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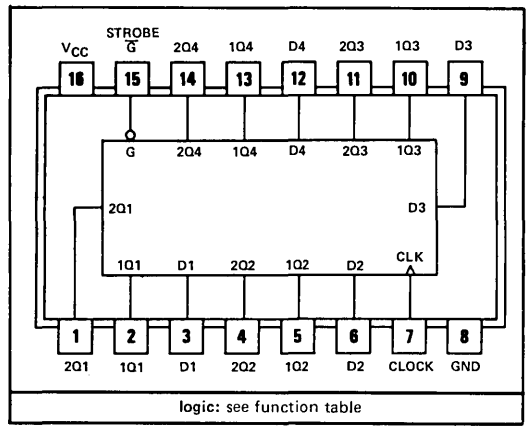
TYPES SN54LS396, SN74LS396
OCTAL STORAGE REGISTERS

D2329, MARCH 1977

- Parallel Access
- Typical Propagation Delay Time . . . 20 ns
- Typical Power Dissipation . . . 120 mW
- Applications:
  N-Bit Storage Files
  Hex/BCD Serial-To-Parallel Converters

SN54LS396 . . . J OR W PACKAGE
SN74LS396 . . . J OR N PACKAGE
(TOP VIEW)



logic: see function table

description

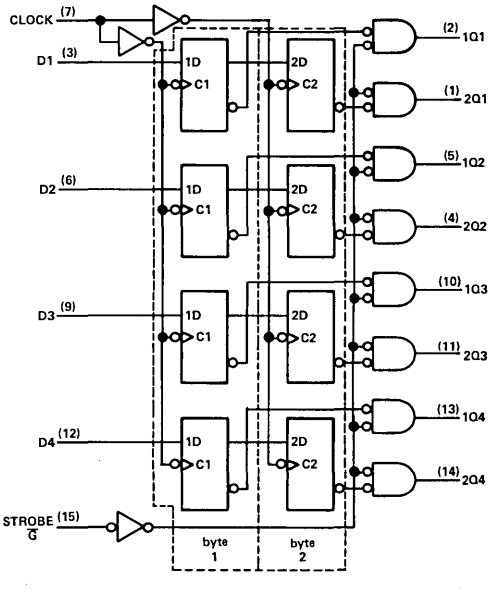
These octal registers are organized as two 4-bit bytes of storage. Upon application of a positive-going clock signal, the information stored in byte 1 is transferred into byte 2 as a new 4-bit byte is loaded into the byte 1 location via the four data lines. The full 8-bit word is available at the outputs after two clock cycles. Both the clock and the strobe lines are fully buffered.

FUNCTION TABLE

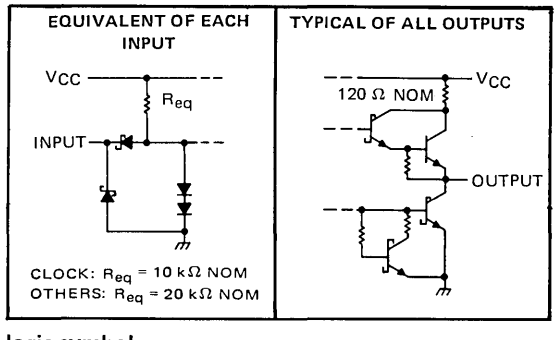
INPUTS						OUTPUTS							
STROBE $\overline{G}$	CLOCK	DATA				BYTE 1				BYTE 2			
		D1	D2	D3	D4	1Q1	1Q2	1Q3	1Q4	2Q1	2Q2	2Q3	2Q4
H	X	X	X	X	X	L	L	L	L	L	L	L	L
L	↑	a	b	c	d	a	b	c	d	$1Q1_n$	$1Q2_n$	$1Q3_n$	$1Q4_n$

H = high level (steady state), L = low level (steady state), X = irrelevant (any input, including transitions)
↑ = transition from low to high level
$1Q1_n$, $1Q2_n$, $1Q3_n$, $1Q4_n$ = the level of 1Q1, 1Q2, 1Q3, and 1Q4, respectively, before the most recent ↑ transition of the clock.

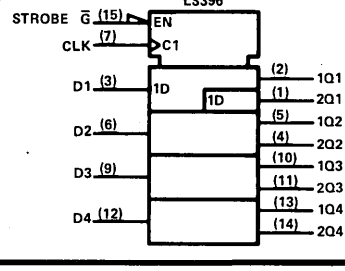
functional block diagram



schematics of inputs and outputs



logic symbol



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS396 . . . . . −55°C to 125°C
SN74LS396 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS396			SN74LS396			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Clock frequency, f_{clock}	0		30	0		30	MHz
Width of clock pulse, t_w	20			20			ns
Setup time, t_{su}	20			20			ns
Hold time, t_h	5			5			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS396			SN74LS396			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX,	V_{IH} = 2 V, I_{OH} = −400 μA	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	Clock input	V_{CC} = MAX,	V_I = 7 V			0.2			0.2	mA
		Other inputs					0.1			0.1	
I_{IH}	High-level input current	Clock input	V_{CC} = MAX,	V_I = 2.7 V			40			40	μA
		Other inputs					20			20	
I_{IL}	Low-level input current	Clock input	V_{CC} = MAX,	V_I = 0.4 V			−0.8			−0.8	mA
		Other inputs					−0.4			−0.4	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current		V_{CC} = MAX,	See Note 2		24	40		24	40	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
NOTE 2: I_{CC} is measured with 4.5 V applied to all inputs and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from clock	C_L = 15 pF, R_L = 2 kΩ, See Note 3		20	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			20	30	
t_{PLH}	Propagation delay time, low-to-high-level output from strobe			20	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output from strobe			20	30	

NOTE 3: Load circuit and voltage waveforms are shown on page 3-11 of *The TTL Data Book for Design Engineers*, Second Edition, LCC4112.

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- Will Not Trigger from Clear
- D-C Triggered from Active-High or Active-Low Gated Logic Inputs
- Retriggerable for Very Long Output Pulses, Up to 100% Duty Cycle
- Overriding Clear Terminates Output Pulse
- Compensated for V_{CC} and Temperature Variations
- 'LS422 Has Internal Timing Resistor

description

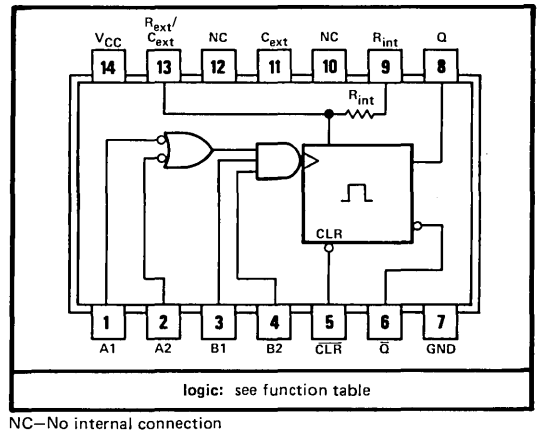
The 'LS422 and 'LS423 are identical to 'LS122 and 'LS123 except they cannot be triggered via clear.

These d-c triggered multivibrators feature output-pulse-width control by three methods. The basic pulse time is programmed by selection of external resistance and capacitance values (see typical application data). The 'LS422 contains an internal timing resistor that allows the circuits to be used with only an external capacitor, if so desired. Once triggered, the basic pulse width may be extended by retriggering the gated low-level-active (A) or high-level-active (B) inputs, or be reduced by use of the overriding clear. Figure 1 illustrates pulse control by retriggering and early clear.

The 'LS422 and 'LS423 have enough Schmitt hysteresis to ensure jitter-free triggering from the B input with transition rates as slow as 0.1 millivolt per nanosecond.

The SN54LS422 and SN54LS423 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LS422 and SN74LS423 are characterized for operation from 0°C to 70°C.

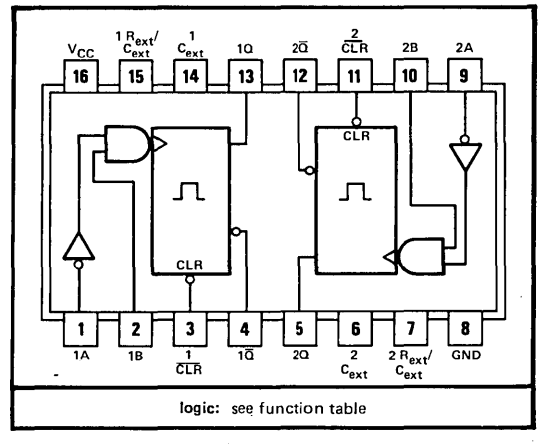
SN54LS422 . . . J OR W PACKAGE
SN74LS422 . . . J OR N PACKAGE
(TOP VIEW) (SEE NOTES 1 THRU 4)



logic: see function table

NC—No internal connection

SN54LS423 . . . J OR W PACKAGE
SN74LS423 . . . J OR N PACKAGE
(TOP VIEW) (SEE NOTES 1 THRU 4)



logic: see function table

NOTES: 1. An external timing capacitor may be connected between C_{ext} and R_{ext}/C_{ext} (positive).
2. To use the internal timing resistor of 'LS422, connect R_{int} to V_{CC}.
3. For improved pulse width accuracy and repeatability, connect an external resistor between R_{ext}/C_{ext} and V_{CC} with R_{int} open-circuited.
4. To obtain variable pulse widths, connect an external variable resistance between R_{int} or R_{ext}/C_{ext} and V_{CC}.

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description (continued)

'LS422
FUNCTION TABLE

INPUTS					OUTPUTS	
CLEAR	A1	A2	B1	B2	Q	$\overline{Q}$
L	X	X	X	X	L	H
X	H	H	X	X	L	H
X	X	X	L	X	L	H
X	X	X	X	L	L	H
H	L	X	↑	H	⎍	⎎
H	L	X	H	↑	⎍	⎎
H	X	L	↑	H	⎍	⎎
H	X	L	H	↑	⎍	⎎
H	H	↓	H	H	⎍	⎎
H	↓	↓	H	H	⎍	⎎
H	↓	H	H	H	⎍	⎎

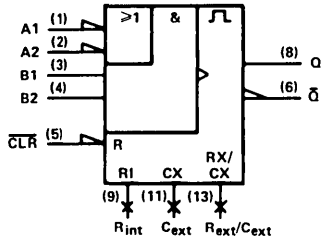
'LS423
FUNCTION TABLE

INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎

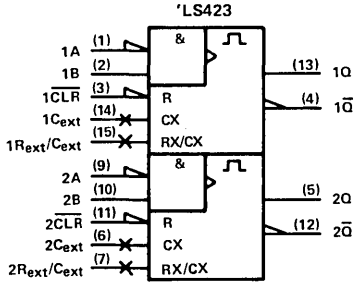
H = high level (steady state)
L = low level (steady state)
↑ = transition from low to high level
↓ = transition from high to low level
X = irrelevant (any input, including transitions)
⎍ = one high-level pulse
⎎ = one low-level pulse

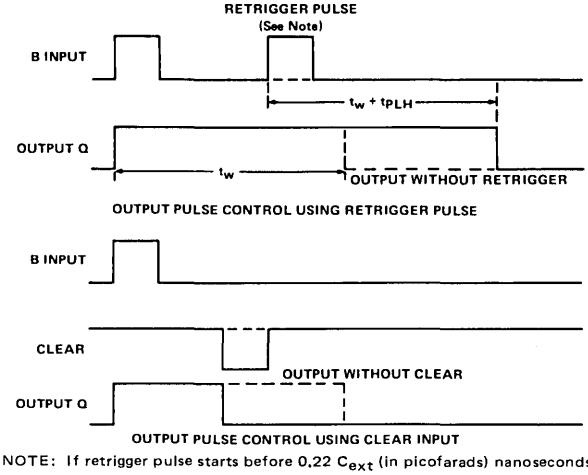
logic symbols

'LS422



'LS423

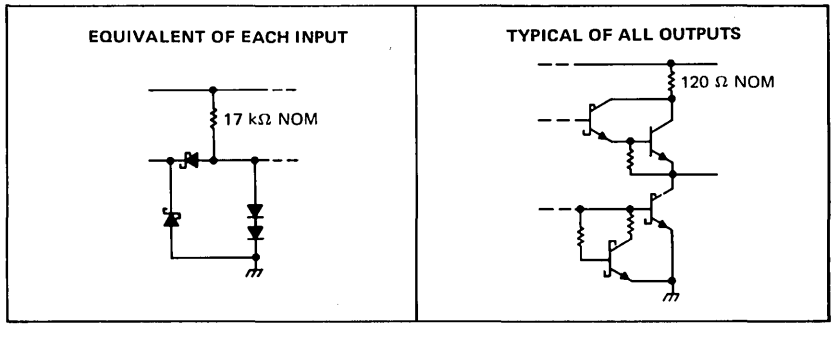




NOTE: If retrigger pulse starts before 0.22 C_{ext} (in picofarads) nanoseconds after previous trigger pulse, output pulse extension may be shorter than $t_w + t_{PLH}$.

FIGURE 1–TYPICAL INPUT/OUTPUT PULSES

schematics of inputs and outputs



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recommended operating conditions

	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Pulse width, t_w	40			40			ns
External timing resistance, R_{ext}	5		180	5		260	kΩ
External capacitance, C_{ext}	No restriction			No restriction			
Wiring capacitance at R_{ext}/C_{ext} terminal			50			50	pF
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN54LS'			SN74LS'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL}max	V_{IH} = 2 V, I_{OH} = −400 μA		2.5	3.5		2.7	3.5		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL}max	V_{IH} = 2 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current♦	V_{CC} = MAX			−20		−100	−20		−100	mA
I_{CC}	Supply current (quiescent or triggered)	V_{CC} = MAX,	See Note 6	'LS422		6	11		6	11	mA
				'LS423		12	20		12	20	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
♦Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
NOTES: 5. To measure V_{OH} at Q, V_{OL} at $\overline{Q}$, or I_{OS} at Q, ground R_{ext}/C_{ext}, apply 2 V to B and clear, and pulse A from 2 V to 0 V.
6. With all outputs open and 4.5 V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5 V, is applied to clock.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, see note 7

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A	Q	C_{ext} = 0, C_L = 15 pF,	R_{ext} = 5 kΩ, R_L = 2 kΩ		23	33	ns
	B					23	44	
t_{PHL}	A	$\overline{Q}$				32	45	ns
	B					34	56	
t_{PHL}	Clear	Q				20	27	ns
t_{PLH}		$\overline{Q}$				28	45	
t_{wQ} (min)	A or B	Q				116	200	ns
t_{wQ}	A or B	Q	C_{ext} = 1000 pF, C_L = 15 pF,	R_{ext} = 10 kΩ, R_L = 2 kΩ	4	4.5	5	μs

¶ t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{wQ} ≡ width of pulse at output Q
NOTE 7: Load circuit and voltage waveforms are shown on page 3-11 of "The TTL Data Book for Design Engineers", second edition.

TYPICAL APPLICATION DATA

The basic output pulse width is determined by the value of external capacitance and timing resistance.

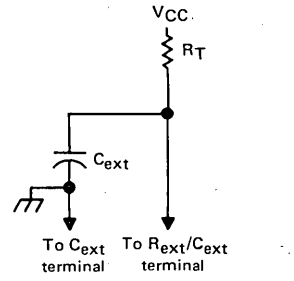
Figure 3 gives curves for output pulse widths ranging from 0.1 μs to 100 μs for several R_T and C_{ext} values. For output pulse widths greater than 100 μs or external capacitance greater than 1000 pF the following equation should be used.

$$t_w = K \cdot R_T \cdot C_{ext}$$

where

t_w is in ns
K is the multiplying factor and is approximately 0.45 for $C_{ext} \geq 1000$ pF.
C_{ext} is in pF

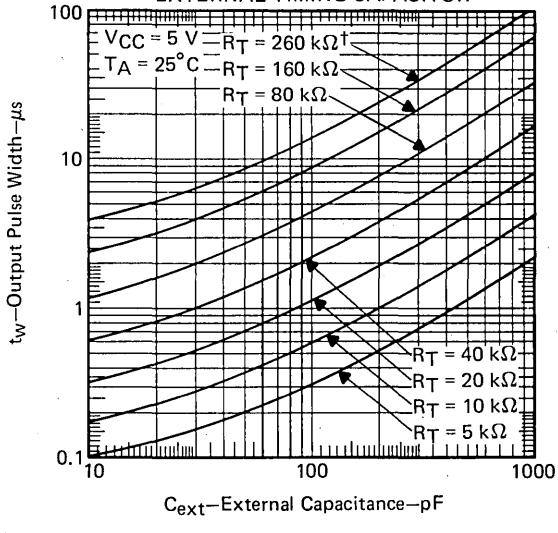
For best results, system ground should be applied to the C_{ext} terminal. These devices do not require a switching diode in series with the R_{ext}/C_{ext} terminal (as required by some other monostable multivibrators).



TIMING COMPONENT CONNECTIONS

FIGURE 2

TYPICAL OUTPUT PULSE WIDTH
vs
EXTERNAL TIMING CAPACITOR



†This value of resistance exceeds the maximum recommended for use over the full temperature range of the SN54LS circuits.

FIGURE 3

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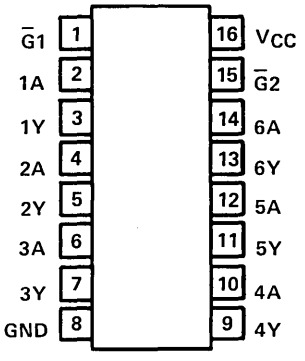
TYPES SN54S436, SN54S437, SN74S436, SN74S437
LINE DRIVER/MEMORY DRIVER CIRCUITS

D2630, JANUARY 1981

MOS MEMORY INTERFACE

- Can Drive High-Impedance Loads
- Interchangeable with National DS16149, DS16179 Drivers
- High-Speed Switching
- Minimum Input Current Required
- Damping Output Resistor Reduces Transients

SN54S436, SN54S437 . . . J OR W PACKAGE
SN74S436, SN74S437 . . . J OR N PACKAGE
(TOP VIEW)

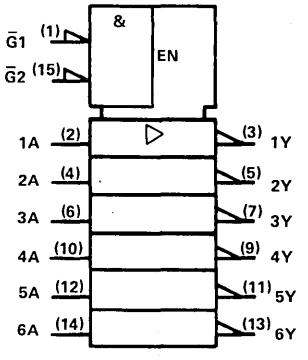


description

The SN54S436, SN54S437, SN74S436 and SN74S437 are monolithic integrated TTL-to-MOS drivers and interface circuits. The devices accept standard TTL and DTL input signals. The p-n-p input transistors use minimum current allowing increased fan-out to these drivers. Schottky-clamped transistor logic permits high-speed operation, minimum propagation time.

A small series damping resistor has been included in the design of the 'S436 to eliminate undersired output transient overshoot. Either enable, G, when high, sets the outputs to the high level for MOS RAM refresh applications.

logic symbol



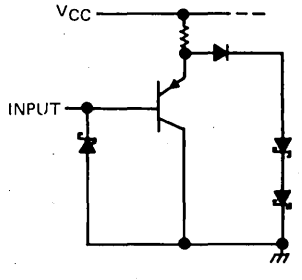
FUNCTION TABLE

ENABLE INPUTS		INPUT	OUTPUT
$\overline{G1}$	$\overline{G2}$		
L	L	L	H
L	L	H	L
X	H	X	H
H	X	X	H

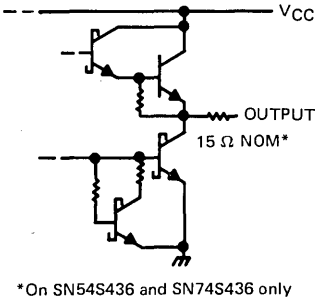
H = high level, L = low level, X = irrelevant

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



*On SN54S436 and SN74S436 only

ADVANCE INFORMATION
This document contains information on a new product. Specifications are subject to change without notice.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage range . . . . . −1.5 V to 7 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)
J package . . . . . 1375 mW
N package . . . . . 1150 mW
W package . . . . . 1000 mW
Operating free-air temperature range: SN54S436, SN54S437 . . . . . −55°C to 125°C
SN74S436, SN74S437 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: All voltage values are with respect to network ground terminal.
2: For operation above 25°C free-air temperature, derate as follows: J package, 11.0 mW/°C, N package, 9.2 mW/°C, W package, 8.0 mW/°C.

recommended operating conditions

	SN54S'			SN74S'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54S'			SN74S'			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = 4.5 V, I_I = −18 mA			−0.75	−1.2		−0.75	−1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5 V, I_{OH} = −10 μA		3.4	4.3		3.5	4.3		V
		V_{CC} = 4.5 V, I_{OH} = −1 mA	'S436	2.4	3.5		2.6	3.5		
			'S437	2.5	3.5		2.7	3.5		
V_{OL}	Low-level output voltage	V_{CC} = 4.5 V, I_{OL} = 10 μA			0.25	0.4		0.25	0.35	V
		V_{CC} = 4.5 V, I_{OL} = 20 mA	'S436		0.6	1.1		0.6	1	
			'S437		0.4	0.5		0.4	0.5	
I_{OL}	Low-level output current	V_{CC} = 4.5 V, V_I = 2 V,	V_O = 4.5 V, See Note 3		150			150		mA
I_{OS}	Short-circuit output current	V_{CC} = 4.5 V, See Note 3	V_O = 0 V,		−250			−250		mA
I_{IH}	High-level input current	V_{CC} = 5.5 V,	V_{IH} = 5.5 V		0.1	40		0.1	40	μA
I_{IL}	Low-level input current	V_{CC} = 5.5 V,	V_{IL} = 0.5 V		−50	−250		−50	−250	μA
I_{CC}	Supply current	V_{CC} = 5.5 V, All other inputs at 3 V	$\overline{G}$ inputs at 0 V,		33	60		33	60	mA
		V_{CC} = 5.5 V,	All inputs at 0 V		14	20		14	20	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 3: When measuring output current on the SN54S437/SN74S437, a 15-Ω resistor should be placed in series with each output.

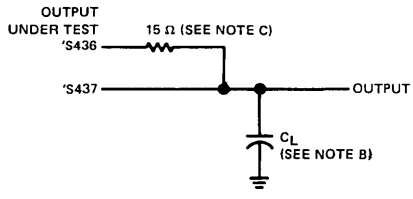
switching characteristics, V_{CC} = 5 V, T_A = 25°C, see note 3

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{AHYL}	Delay time from A high to Y starting low	See Figure 1	C_L = 50 pF		4.5	7	ns
			C_L = 500 pF		7.5	12	
t_{ALYH}	Delay time from A low to Y starting high	See Figure 1	C_L = 50 pF		5	8	ns
			C_L = 500 pF		8	13	
t_{GHYH}	Delay time from $\overline{G}$ high to Y starting high	R_L = 2 kΩ to Gnd, See Figure 2	C_L = 50 pF,		10	18	ns
t_{GLYL}	Delay time from $\overline{G}$ low to Y starting low	R_L = 2 kΩ to V_{CC}, See Figure 3	C_L = 50 pF,		11	18	ns
t_{THL}	Transition time, high-to-low-level output	See Figure 1	C_L = 50 pF		5	8	ns
			C_L = 500 pF		22	35	
t_{TLH}	Transition time, low-to-high-level output	See Figure 1	C_L = 50 pF		6	9	ns
			C_L = 500 pF		26	35	

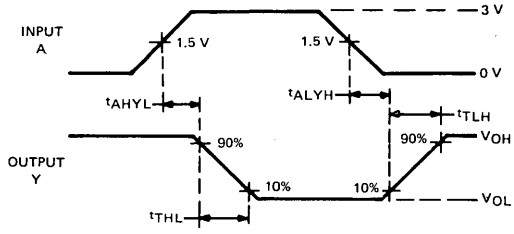
NOTE 3: When measuring switching times on the SN54S437/SN74S437, a 15-Ω resistor should be placed in series with each output.

2

PARAMETER MEASUREMENT INFORMATION

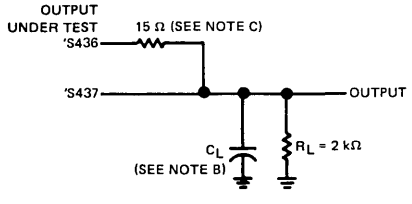


LOAD CIRCUIT

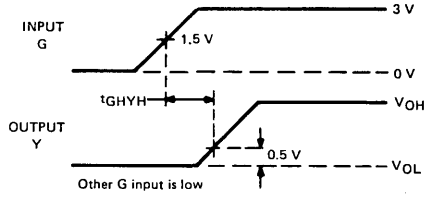


VOLTAGE WAVEFORMS

FIGURE 1

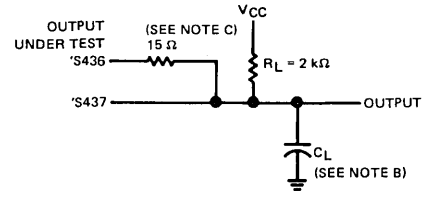


LOAD CIRCUIT

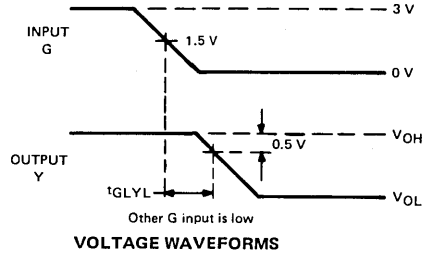


VOLTAGE WAVEFORMS

FIGURE 2



LOAD CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 3

NOTES: A. Input pulses are supplied by a generator having the following characteristics: PRR ≤ 1 MHz, $Z_{out} \approx 50\ \Omega$, $t_r \leq 5$ ns.
B. C_L includes probe and jig capacitance.
C. This 15-Ω resistor is required for testing the SN54S437/SN74S437, but it is internal to the SN54S436/SN74S436 and therefore an external resistor is not used for testing these devices.

TYPICAL APPLICATION DATA

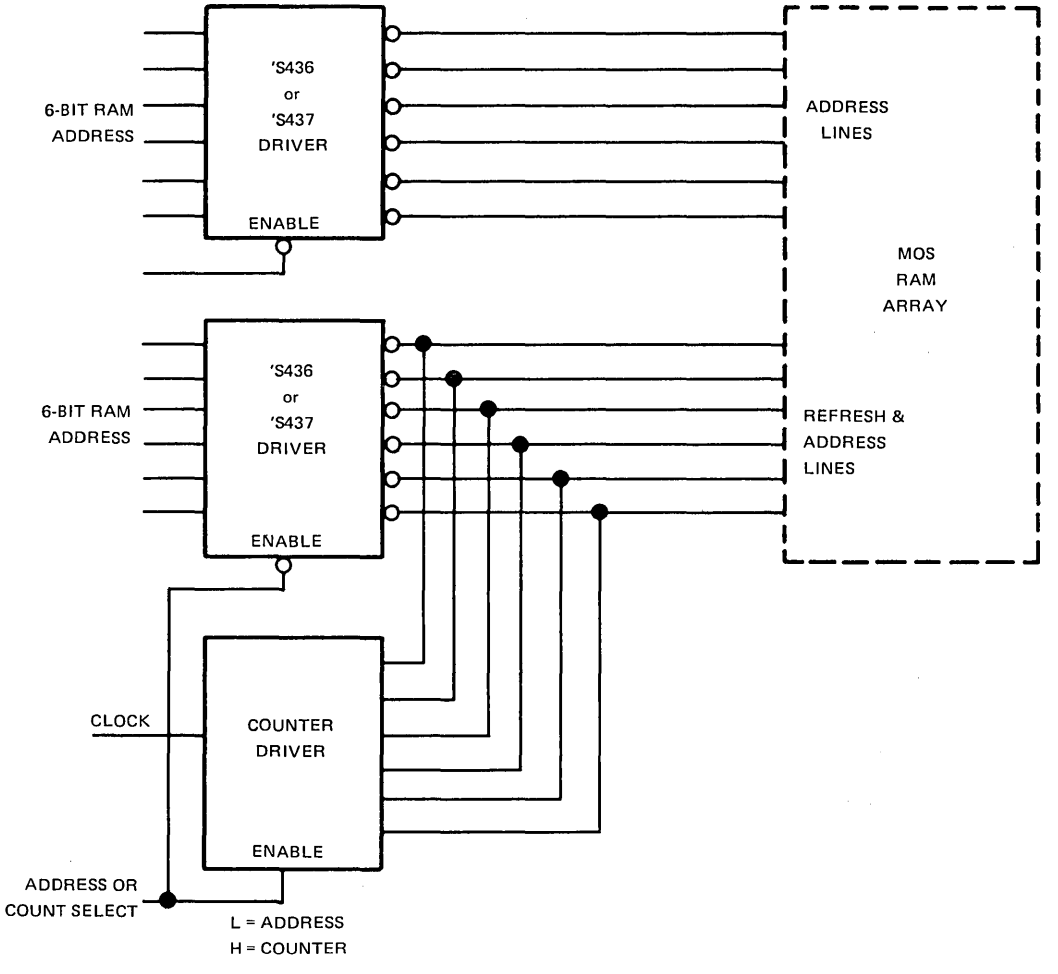


FIGURE 4

TEXAS INSTRUMENTS
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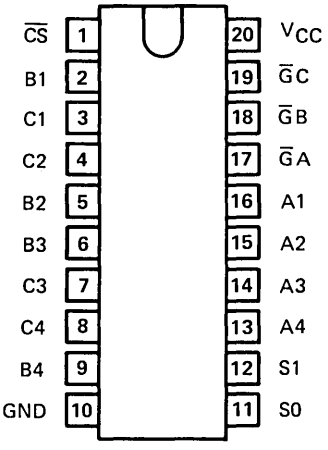
TYPES SN54LS440 THRU SN54LS444, SN54LS448, SN74LS440 THRU SN74LS444, SN74LS448 QUADRUPLE TRIDIRECTIONAL BUS TRANSCEIVERS

D2425, AUGUST 1979

- 3-Way Asynchronous Communication
- On-Chip Bus Selection Decoding
- Input Hysteresis Improves Noise Margin
- Choice of Open-Collector or 3-State Outputs

SN54LS'.....J PACKAGE
SN74LS'.....J OR N PACKAGE
(TOP VIEW)



description

These bus transceivers are designed for asynchronous three-way communication between four-line data buses. They give the designer a choice of selecting inverting, noninverting, or a combination of inverting and noninverting data paths with either 3-state or open-collector outputs.

The S0 and S1 inputs select the bus from which data are to be transferred. The $\overline{G}$ inputs enable the bus or buses to which data are to be transferred. The port for any bus selected for input and any other bus not enabled for output will be at high impedance including those of the open-collector devices.

The SN54LS440 through SN54LS444 and SN54LS448 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LS440 through SN74LS444 and SN74LS448 are characterized for operation from 0°C to 70°C.

DEVICE	OUTPUT	LOGIC
'LS440	Open-Collector	True
'LS441	Open-Collector	Inverting
'LS442	3-State	True
'LS443	3-State	Inverting
'LS444	3-State	True/Inverting
'LS448	Open-Collector	True/Inverting

FUNCTION TABLE

INPUTS						TRANSFERS BETWEEN BUSES		
$\overline{CS}$	S1	S0	$\overline{G}A$	$\overline{G}B$	$\overline{G}C$	'LS440 'LS442	'LS441 'LS443	'LS444 'LS448
H	X	X	X	X	X	None	None	None
X	H	H	X	X	X	None	None	None
X	X	X	H	H	H	None	None	None
X	L	L	X	H	H	None	None	None
X	L	H	H	X	H	None	None	None
X	H	L	H	H	X	None	None	None
L	L	L	X	L	L	A → B, A → C	$\overline{A}$ → B, $\overline{A}$ → C	$\overline{A}$ → B, $\overline{A}$ → C
L	L	H	L	X	L	B → C, B → A	$\overline{B}$ → C, $\overline{B}$ → A	B → C, $\overline{B}$ → A
L	H	L	L	L	X	C → A, C → B	$\overline{C}$ → A, $\overline{C}$ → B	$\overline{C}$ → A, C → B
L	L	L	X	L	H	A → B	$\overline{A}$ → B	$\overline{A}$ → B
L	L	H	H	X	L	B → C	$\overline{B}$ → C	B → C
L	H	L	L	H	X	C → A	$\overline{C}$ → A	$\overline{C}$ → A
L	L	L	X	H	L	A → C	$\overline{A}$ → C	$\overline{A}$ → C
L	L	H	L	X	H	B → A	$\overline{B}$ → A	$\overline{B}$ → A
L	H	L	H	L	X	C → B	$\overline{C}$ → B	C → B

TEXAS INSTRUMENTS
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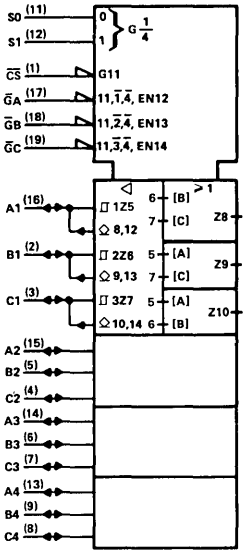
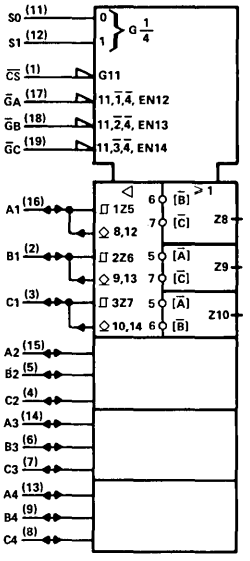
logic symbols

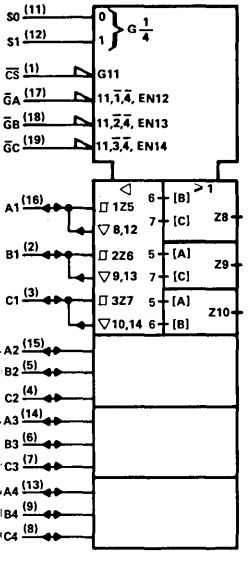
'LS440



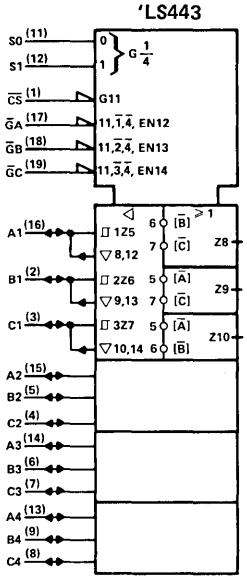
'LS441



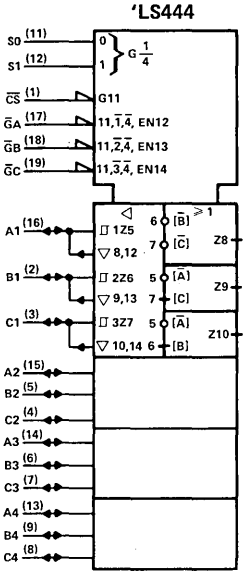
'LS442



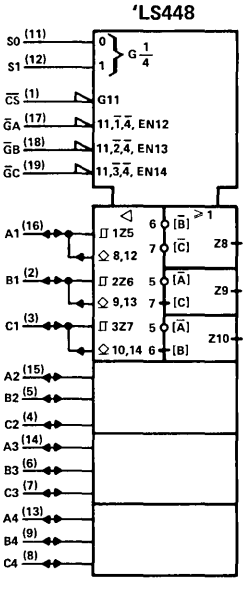
'LS443



'LS444



'LS448



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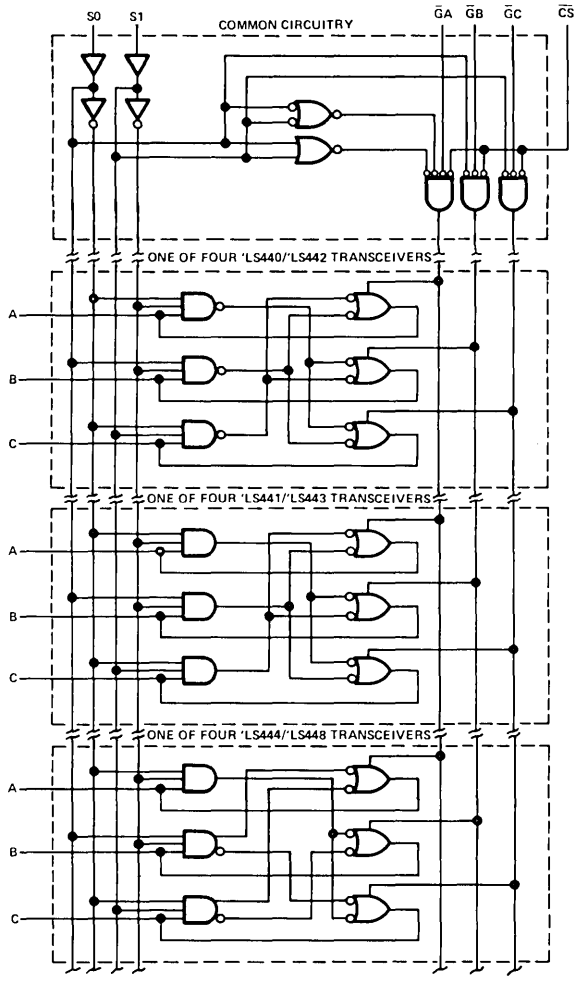
functional block diagram (composite showing one of four transceivers from each type, positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS'	−55°C to 125°C
SN74LS'	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS440 SN54LS441 SN54LS448			SN74LS440 SN74LS441 SN74LS448			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	−55		125	0		70	C

NOTE 1: Voltage values are with respect to the network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.5			0.6	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
	Hysteresis ($V_{T+} - V_{T-}$)	A,B,C input	V_{CC} = MIN		0.1	0.4		0.2	0.4		V
I_{OH}	High-level output current		V_{CC} = MIN, V_{IH} = 2 V,	V_{OH} = 5.5 V, V_{IL} = V_{IL}max			100			100	uA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	V
I_I	Input current at maximum input voltage	A,B,C input	V_{CC} = MAX	V_I = 5.5 V			0.1			0.1	mA
		All others		V_I = 7 V			0.1			0.1	
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
I_{CC}	Supply current	Outputs low	V_{CC} = MAX,	Outputs open		62	90		62	90	mA
		Outputs disabled				64	95		64	95	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics at V_{CC} = 5 V, R_L = 667 Ω, C_L = 45 pF, T_A = 25°C, see Note 2

PARAMETER		FROM (INPUT)	TO (OUTPUT)	'LS440			'LS441			'LS448			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high level output	A	B		24	35		21	30		21	30	ns
		A	C		24	35		21	30		21	30	
		B	A		24	35		21	30		21	30	
		B	C		24	35		21	30		24	35	
		C	A		24	35		21	30		21	30	
		C	B		24	35		21	30		24	35	
t_{PHL}	Propagation delay time, high-to-low level output	A	B		20	30		9	15		9	15	ns
		A	C		20	30		9	15		9	15	
		B	A		20	30		9	15		9	15	
		B	C		20	30		9	15		20	30	
		C	A		20	30		9	15		9	15	
		C	B		20	30		9	15		20	30	
t_{PLH}	Propagation delay time, low-to-high level output	any $\overline{G}$	A, B, C		29	45		23	35		25	40	ns
		S0, S1	A, B, C		33	50		27	40		26	40	
		$\overline{CS}$	A, B, C		31	45		26	40		25	40	
t_{PHL}	Propagation delay time, high-to-low level output	any $\overline{G}$	A, B, C		27	40		20	30		22	35	ns
		S0, S1	A, B, C		32	50		26	40		27	40	
		$\overline{CS}$	A, B, C		28	45		21	30		22	35	

NOTE 2: Load circuit and voltage waveforms are shown on page 3-11 of *The TTL Data Book for Design Engineers*, Second Edition, LCC4112.

recommended operating conditions

	SN54LS442 SN54LS443 SN54LS444			SN74LS442 SN74LS443 SN74LS444			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−12			−15	mA
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

NOTE 1: Voltage values are with respect to the network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.5			0.6	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
	Hysteresis ($V_{T+} - V_{T-}$)	A,B,C input	V_{CC} = MIN		0.1	0.4		0.2	0.4		V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max	I_{OH} = −3 mA	2.4	3.4		2.4	3.4		V
				I_{OH} = MAX	2			2			
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied		V_{CC} = MAX, $\overline{CS}$ at 2 V	V_O = 2.7 V			20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied			V_O = 0.4 V			−400			−400	
I_I	Input current at maximum input voltage	A, B, C	V_{CC} = MAX	V_I = 5.5 V			0.1			0.1	mA
		Others		V_I = 7 V			0.1			0.1	
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
I_{OS}	Short circuit output current¶		V_{CC} = MAX		−40		−225	−40		−225	mA
I_{CC}	Supply current	Outputs low	V_{CC} = MAX,	Outputs open		62	90		62	90	mA
		Outputs at Hi-Z				64	95		64	95	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
¶Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

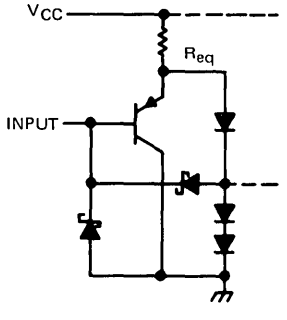
switching characteristics, V_{CC} = 5 V, T_A = 25°C, see Note 2

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS442 MIN	'LS442 TYP	'LS442 MAX	'LS443 MIN	'LS443 TYP	'LS443 MAX	'LS444 MIN	'LS444 TYP	'LS444 MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	A	B	C_L = 45 pF, R_L = 667 Ω		10	14		9	14		9	14	ns
		A	C			10	14		9	14		9	14	
		B	A			10	14		9	14		9	14	
		B	C			10	14		9	14		10	14	
		C	A			10	14		9	14		9	14	
		C	B			10	14		9	14		10	14	
t_{PHL}	Propagation delay time, high-to-low level output	A	B			13	20		7	13		7	13	ns
		A	C			13	20		7	13		7	13	
		B	A			13	20		7	13		7	13	
		B	C			13	20		7	13		13	20	
		C	A			13	20		7	13		7	13	
		C	B			13	20		7	13		13	20	
t_{PZL}	Output enable time to low level	Any $\overline{G}$	A, B, C			22	33		22	33		22	33	ns
		S0 or S1	A, B, C			28	42		28	42		28	42	
		$\overline{CS}$	A, B, C			23	36		24	36		23	36	
t_{PZH}	Output enable time to high level	$\overline{G}$, S, $\overline{CS}$	A, B, C			21	32		20	32		24	32	ns
t_{PLZ}	Output disable time from low level	$\overline{G}$, S, $\overline{CS}$	A, B, C	C_L = 5 pF, R_L = 667 Ω		14	25		15	25		14	25	ns
t_{PHZ}	Output disable time from high level	$\overline{G}$, S, $\overline{CS}$	A, B, C			14	25		15	25		14	25	ns

NOTE 2: Load circuit and voltage waveforms are shown on page 3-11 of *The TTL Data Book for Design Engineers*, Second Edition, LCC4112.

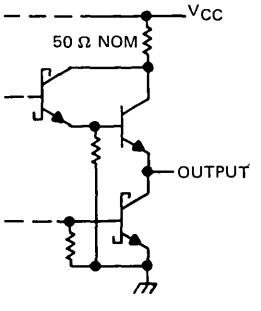
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT

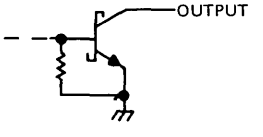


R_{eq}: $\overline{G}$A, $\overline{G}$B, $\overline{G}$C = 9 kΩ NOM
All others = 5 kΩ NOM

TYPICAL OF 3-STATE OUTPUTS



TYPICAL OF OPEN-COLLECTOR OUTPUTS



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

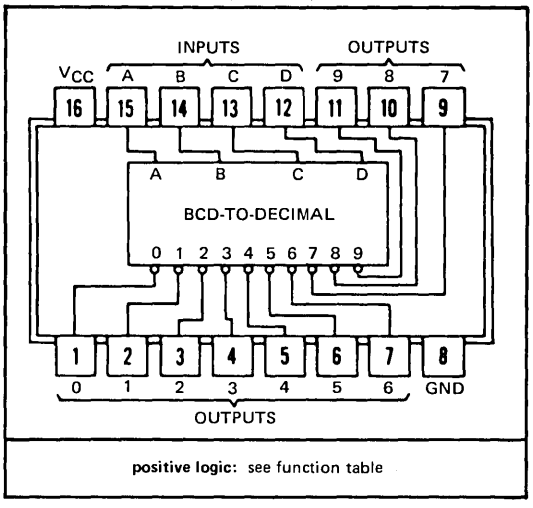
TYPES SN54LS445, SN74LS445
BCD-TO-DECIMAL DECODERS/DRIVERS

D2427, NOVEMBER 1977

FOR USE AS LAMP, RELAY, OR MOS DRIVERS

- Low-Voltage Version of SN54LS145/ SN74LS145
- Full Decoding of Input Logic
- SN74LS445 Has 80-mA Sink-Current Capability
- All Outputs Are Off for Invalid BCD Input Conditions
- Low Power Dissipation . . . 35 mW Typical

SN54LS445 . . . J OR W PACKAGE
SN74LS445 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

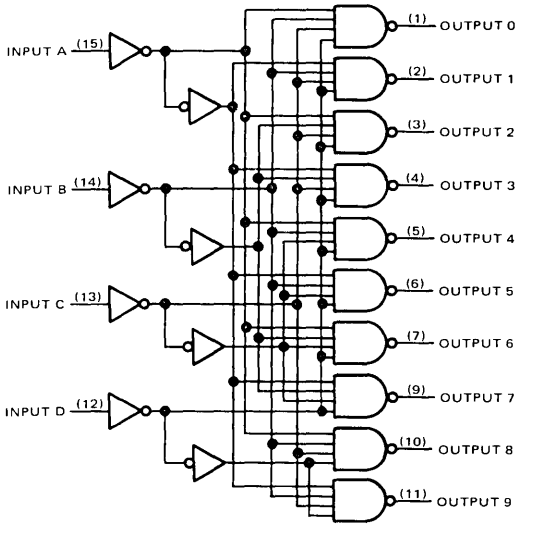
logic

FUNCTION TABLE

NO.	INPUTS				OUTPUTS									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = high level (off), L = low level (on)

functional block diagram



description

These monilithic BCD-to-decimal decoder/drivers consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid BCD input logic ensures that all outputs remain off for all invalid binary input conditions. These decoders feature high-performance, n-p-n output transistors designed for use as indicator/ relay drivers or as open-collector logic-circuit drivers. Each of the output transistors will sink up to 80 milli-amperes of current. Each input is one Series 54LS/ 74LS standard load. Inputs and outputs are entirely compatible for use with TTL or DTL logic circuits, and the outputs are compatible for interfacing with most MOS integrated circuits. Power dissipation is typically 35 milliwatts.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS445 . . . . . −55°C to 125°C
SN74LS445 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS445			SN74LS445			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Off-state output voltage, $V_{O(off)}$			7			7	V
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS445			SN74LS445			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
$I_{O(off)}$	Off-state output current	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, V_{OH} = 7 V			250			250	μA
$V_{O(on)}$	On-state output voltage	V_{CC} = MIN,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{IH} = 2 V,	I_{OL} = 24 mA					0.35	0.5	
		V_{IL} = V_{IL} max	I_{OL} = 80 mA					2.3	3	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 2		7	13		7	13	mA

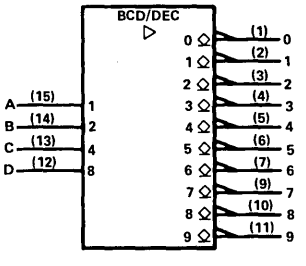
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: I_{CC} is measured with all inputs grounded and outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

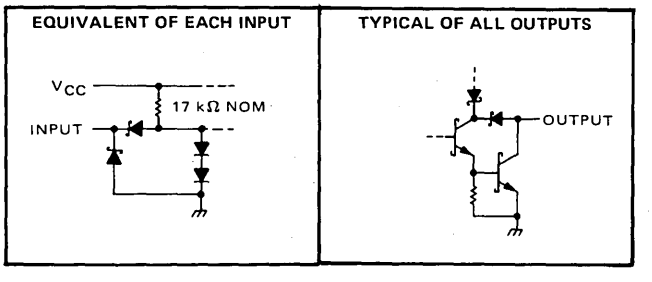
PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 45 pF, R_L = 665 Ω, See Note 3		50	ns
t_{PHL}	Propagation delay time, high-to-low-level output			50	ns

NOTE 3: Load circuit and waveforms are shown on page 3-11 of *The TTL Data Book for Design Engineers,* second edition, LCC 4112.

logic symbol



schematic of inputs and outputs



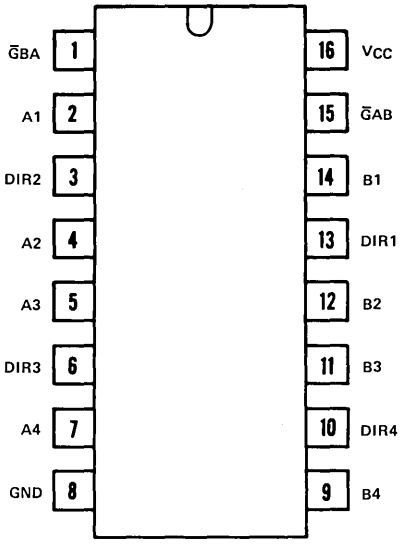
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TYPES SN54LS446, SN54LS449, SN74LS446, SN74LS449
QUADRUPLE BUS TRANSCEIVERS WITH INDIVIDUAL DIRECTION CONTROLS

D2613, OCTOBER 1980

- 3-State Outputs Drive Bus Lines Directly
- P-N-P Inputs Reduce DC Loading on Bus Line
- Hysteresis at Bus Inputs Improves Noise Margins
- Flow-Thru Data Pinout (B Bus Opposite A Bus)
- Choice of True ('LS449) and Inverting ('LS446)

SN54LS . . . J PACKAGE
SN74LS' . . . J or N PACKAGE
(TOP VIEW)



description

These quadruple bus transceivers are designed for data transmission from individual lines of the A bus to individual lines of the B bus or the reverse, depending on the logic levels at the direction-control pins DIR1 through DIR4. These direction controls (one for each channel) allow maximum flexibility in timing. The enable inputs $\overline{G}BA$ and $\overline{G}AB$ can be used to disable the A or B outputs respectively, or to disable both buses for effective isolation.

The SN54LS446 and SN54LS449 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LS446 and SN74LS449 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

ENABLE $\overline{G}BA$	ENABLE $\overline{G}AB$	DIRECTION DIR	OPERATION 'LS446	OPERATION 'LS449
H	H	X	Isolation	Isolation
X	L	H	$\overline{A}$ data to B Bus	A data to B Bus
L	X	L	$\overline{B}$ data to A Bus	B data to A Bus
X	H	H	Isolation	Isolation
H	X	L	Isolation	Isolation

H = high level, L = low level, X = irrelevant

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

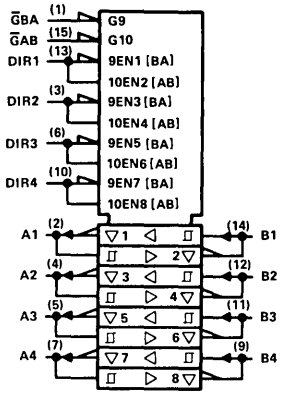
Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54LS' . . . . . −55°C to 125°C
SN74LS' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

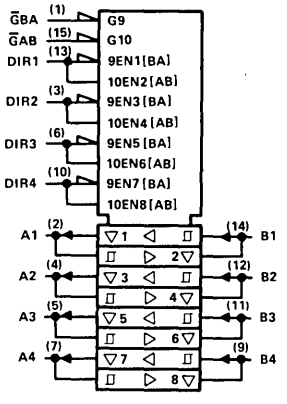
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

logic symbols†

'LS446

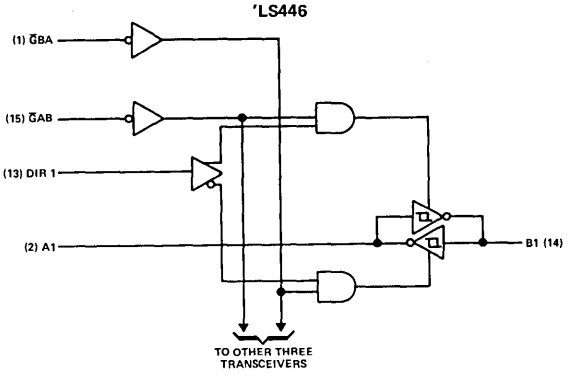


'LS449

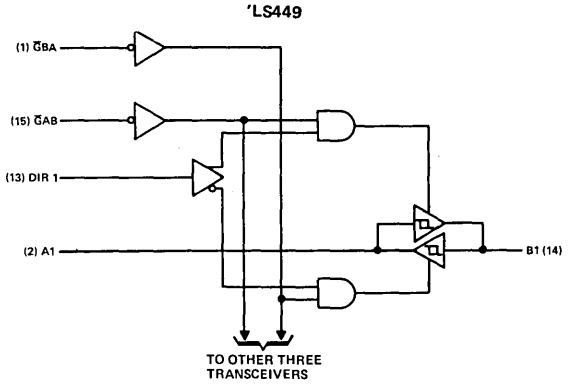


functional block diagrams (positive logic)

'LS446

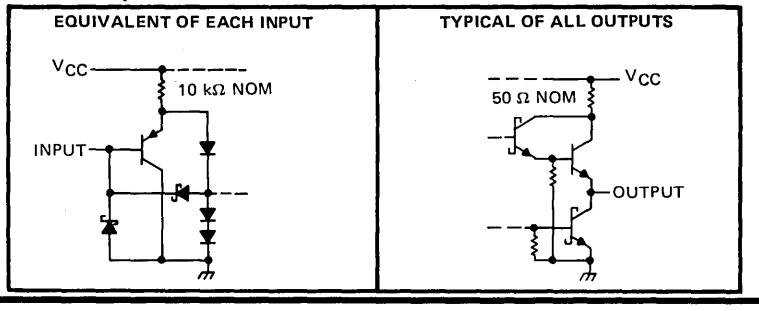


'LS449



†These symbols are in accordance with IEEE Std 91/ANSI Y32 and current discussions IEC and IEEE.

schematics of inputs and outputs



recommended operating conditions

PARAMETER	SN54LS446 SN54LS449			SN74LS446 SN74LS449			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−12			−15	mA
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS446 SN54LS449			SN74LS446 SN74LS449			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.6			0.7	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
	Hysteresis ($V_{T+} - V_{T-}$), A or B input		V_{CC} = MIN		0.1	0.4		0.2	0.4		V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OH} = −3 mA	2.4	3.4		2.4	3.4		V
				I_{OH} = MAX	2			2			
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied		V_{CC} = MAX, V_O = 2.7 V	$\overline{G}$ at 2 V,			20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied		V_{CC} = MAX, V_O = 0.4 V	$\overline{G}$ at 2 V,			−400			−400	μA
I_I	Input current at maximum input voltage	A or B	V_{CC} = MAX,	V_I = 5.5 V			0.1			0.1	mA
		$\overline{G}$AB or $\overline{G}$BA		V_I = 7 V			0.1			0.1	
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
I_{OS}	Short-circuit output current¶		V_{CC} = MAX		−40		−225	−40		−225	mA
I_{CC}	Total supply current	'LS446	V_{CC} = MAX, Outputs open	Outputs high		35	56		35	56	mA
				Outputs low		39	63		39	63	
				Outputs at Hi-Z		42	68		42	68	
		'LS449		Outputs high		42	68		42	68	
				Outputs low		47	75		47	75	
				Outputs at Hi-Z		50	80		50	80	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
¶Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics at V_{CC} = 5 V, T_A = 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS446			'LS449			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	A	B	C_L = 45 pF, R_L = 667 Ω, See Note 2		8	13		10	15	ns
		B	A			8	13		10	15	
t_{PHL}	Propagation delay time, high-to-low-level output	A	B			7	12		11	17	ns
		B	A			7	12		11	17	
t_{PZL}	Output enable time to low level	$\overline{G}$BA	A			24	40		21	35	ns
		$\overline{G}$AB	B			24	40		21	35	
t_{PZH}	Output enable time to high level	$\overline{G}$BA	A			15	25		18	30	ns
		$\overline{G}$AB	B			15	25		18	30	
t_{PLZ}	Output disable time from low level	$\overline{G}$BA	A	C_L = 5 pF, R_L = 667 Ω, See Note 2		14	25		14	25	ns
		$\overline{G}$AB	B			14	25		14	25	
t_{PHZ}	Output disable time from high level	$\overline{G}$BA	A			10	15		10	15	ns
		$\overline{G}$AB	B			10	15		10	15	

NOTE 2: For load circuits and voltage waveforms, see page 3-10 of "The TTL Data Book for Design Engineers," second edition.

TEXAS INSTRUMENTS
INCORPORATED
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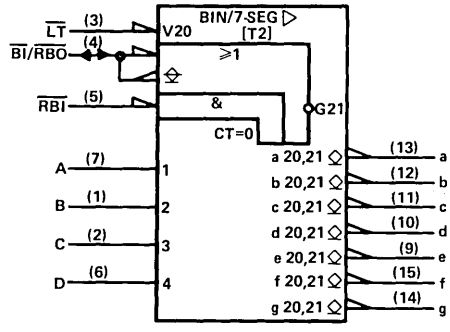
TYPES SN54LS447, SN74LS447
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

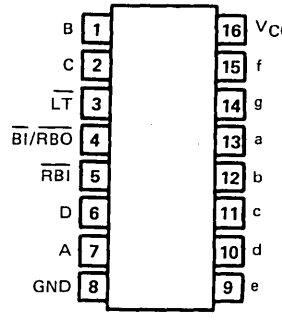
D2428, NOVEMBER 1977

- Low-Voltage Version of SN54LS247/SN74LS247
- Open-Collector Outputs Drive Indicators Directly
- Lamp-Test Provision
- Leading/Trailing Zero Suppression
- Lamp Intensity Modulation Capability

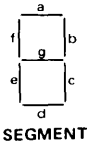
logic symbol



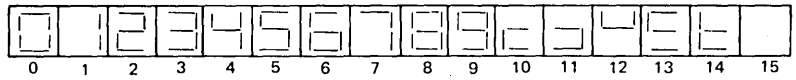
(TOP VIEW)



TYPE	DRIVER OUTPUTS				TYPICAL POWER DISSIPATION	PACKAGES
	ACTIVE LEVEL	OUTPUT CONFIGURATION	SINK CURRENT	MAX VOLTAGE		
SN54LS247	low	open-collector	12 mA	7 V	35 mW	J, W
SN74LS247	low	open-collector	24 mA	7 V	35 mW	J, N



SEGMENT IDENTIFICATION



FONT TABLE T2 – NUMERICAL DESIGNATIONS AND RESULTANT DISPLAYS

FUNCTION TABLE

DECIMAL OR FUNCTION	INPUTS						BI/RBO†	OUTPUTS							NOTE
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	ON	ON	ON	ON	ON	ON	OFF	1
1	H	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF	
2	H	X	L	L	H	L	H	ON	ON	OFF	ON	ON	OFF	ON	
3	H	X	L	L	H	H	H	ON	ON	ON	ON	OFF	OFF	ON	
4	H	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON	
5	H	X	L	H	L	H	H	ON	OFF	ON	ON	OFF	ON	ON	
6	H	X	L	H	H	L	H	ON	OFF	ON	ON	ON	ON	ON	
7	H	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF	
8	H	X	H	L	L	L	H	ON	ON	ON	ON	ON	ON	ON	
9	H	X	H	L	L	H	H	ON	ON	ON	ON	OFF	ON	ON	
10	H	X	H	L	H	L	H	OFF	OFF	OFF	ON	ON	OFF	ON	
11	H	X	H	L	H	H	H	OFF	OFF	ON	ON	OFF	OFF	ON	
12	H	X	H	H	L	L	H	OFF	ON	OFF	OFF	OFF	ON	ON	
13	H	X	H	H	L	H	H	ON	OFF	OFF	ON	OFF	ON	ON	
14	H	X	H	H	H	L	H	OFF	OFF	OFF	ON	ON	ON	ON	
15	H	X	H	H	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
BI	X	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	2
RBI	H	L	L	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	3
LT	L	X	X	X	X	X	H	ON	ON	ON	ON	ON	ON	ON	4

H = high level, L = low level, X = irrelevant

NOTES: 1. The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input (RBI) must be open or high if blanking of a decimal zero is not desired.

2. When a low logic level is applied directly to the blanking input (BI), all segment outputs are off regardless of the level of any other input.

3. When ripple-blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go off and the ripple-blanking output (RBO) goes to a low level (response condition).

4. When the blanking input/ripple blanking output (BI/RBO) is open or held high and a low is applied to the lamp-test input, all segment outputs are on.

†BI/RBO is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Peak output current ($t_w \leq 1$ ms, duty cycle $\leq 10\%$) . . . . . 200 mA
Current forced into any output in the off state . . . . . 1 mA
Operating free-air temperature range: SN54LS447 . . . . . −55°C to 125°C
SN74LS447 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS447			SN74LS447			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Off-state output voltage, $V_{O(off)}$	a thru g			7			7	V
On-state output current, $I_{O(on)}$	a thru g			12			24	mA
High-level output current, I_{OH}	BI/RBO			−50			−50	μA
Low-level output current, I_{OL}	BI/RBO			1.6			3.2	mA
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS447			SN74LS447			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	BI/RBO	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, I_{OH} = −50 μA	2.4	4.2		2.4	4.2		V
V_{OL}	Low-level output voltage	BI/RBO	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 1.6 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 3.2 mA					0.35	0.5	
$I_{O(off)}$	Off-state output current	a thru g	V_{CC} = MAX, V_{IL} = V_{IL} max,	V_{IH} = 2 V, $V_{O(off)}$ = 7 V			250			250	μA
$V_{O(on)}$	On-state output voltage	a thru g	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = V_{IL} max	$I_{O(on)}$ = 12 mA		0.25	0.4		0.25	0.4	V
				$I_{O(on)}$ = 24 mA					0.35	0.5	
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current	Any input except BI/RBO	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
		BI/RBO					−1.2			−1.2	
I_{OS}	Short-circuit output current	BI/RBO	V_{CC} = MAX		−0.3		−2	−0.3		−2	mA
I_{CC}	Supply current		V_{CC} = MAX,	See Note 2		7	13		7	13	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: I_{CC} is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{off}	Turn-off time from A input	C_L = 15 pF, R_L = 665 Ω, See Note 4			100	ns
t_{on}	Turn-on time from A input				100	
t_{off}	Turn-off time from RBI input				100	ns
t_{on}	Turn-on time from RBI input				100	

NOTE 4: Load circuit and voltage waveforms are shown on page 3-11 of *The TTL Data Book for Design Engineers*, Second Edition, LCC4112; t_{off} corresponds to t_{PLH} and t_{on} corresponds to t_{PHL}.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

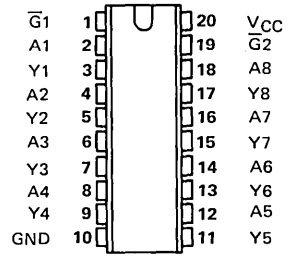
TYPES SN54LS465 THRU SN54LS468, SN74LS465 THRU SN74LS468
OCTAL BUFFERS WITH 3-STATE OUTPUTS

D2631, JANUARY 1981

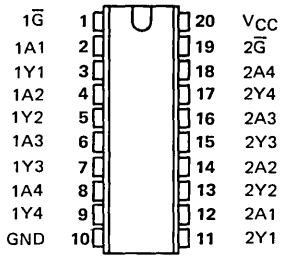
- Mechanically and Functionally Interchangeable With DM71/81LS95 thru DM71/81LS98
- P-N-P Inputs Reduce Bus Loading
- 3-State Outputs Rated at I_{OL} of 12 mA and 24 mA for 54LS and 74LS, Respectively

DEVICE	DATA PATH
'LS465	True
'LS466	Inverting
'LS467	True
'LS468	Inverting

SN54LS465 AND SN54LS466 . . J PACKAGE
SN74LS465 AND SN74LS466 . . J OR N PACKAGE
(TOP VIEW)



SN54LS467 AND SN54LS468 . . J PACKAGE
SN74LS467 AND SN74LS468 . . J OR N PACKAGE
(TOP VIEW)

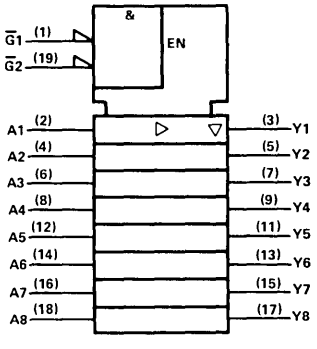


description

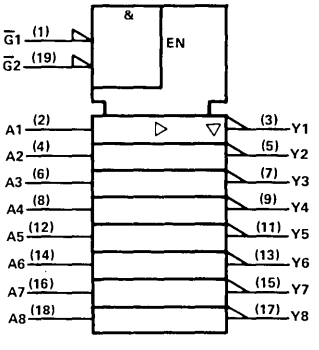
These octal buffers utilize the latest low-power Schottky technology. The 'LS465 and 'LS466 have a two-input active-low AND enable gate controlling all eight data buffers. The 'LS467 and 'LS468 have two separate active-low enable inputs each controlling four data buffers. In either case, a high level on any $\overline{G}$ places the affected outputs at high impedance.

logic symbols

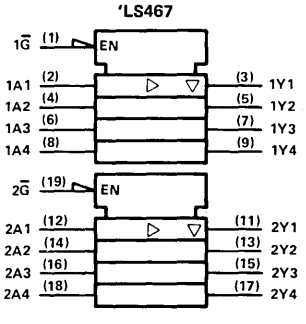
'LS465



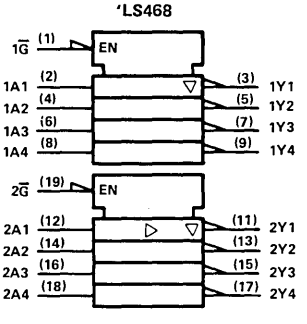
'LS466



'LS467



'LS468



PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54LS465 thru SN54LS468 . . . . . −55°C to 125°C
SN74LS465 thru SN74LS468 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−1			−2.6	mA
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OH} = −1 mA	2.4	3.3					V
				I_{OH} = −2.6 mA				2.4	3.1		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied		V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = V_{IL} max, V_O = 2.7 V				20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied		V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = V_{IL} max, V_O = 0.4 V				−20			−20	μA
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.4 V				−0.2			−0.2	mA
I_{OS}	Short-circuit output current§		V_{CC} = MAX, V_O = 0 V		−30		−130	−30		−130	mA
I_{CC}	Supply current	'LS465, 'LS467	V_{CC} = MAX	Outputs low		14			14		mA
				Outputs high		7			7		
				Output Hi-Z		17			17		
		'LS466, 'LS468		Outputs low		10			10		
				Outputs high		4			4		
				Outputs Hi-Z		13			13		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, see note 2

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS465, 'LS467			'LS466, 'LS468			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Ai	Yi	R_L = 667 Ω, C_L = 45 pF		11			8		ns
t_{PHL}	Ai	Yi			11			8		ns
t_{PZH}	$\overline{G}$ ↓	Y			21			23		ns
t_{PZL}	$\overline{G}$ ↓	Y			24			28		ns
t_{PHZ}	$\overline{G}$ ↑	Y	R_L = 667 Ω, C_L = 5 pF		18			18		ns
t_{PLZ}	$\overline{G}$ ↑	Y			13			13		ns

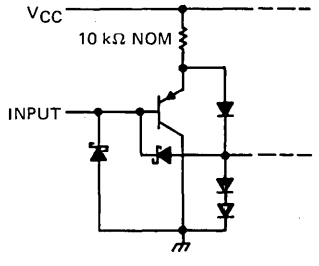
NOTE 2: Load circuit and voltage waveforms are shown on page 3-11 of *The TTL Data Book for Design Engineers*, Second Edition, LCC4112.

t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
t_{PZH} ≡ Output enable time to high level
t_{PZL} ≡ Output enable time to low level
t_{PHZ} ≡ Output disable time from high level
t_{PLZ} ≡ Output disable time from low level

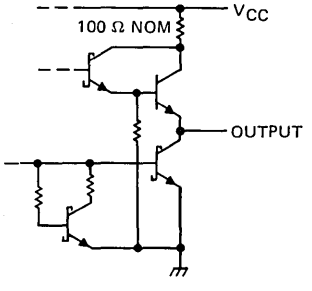
2

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS

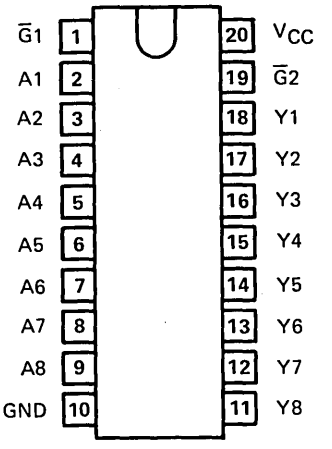


TYPES SN54LS540, SN54LS541, SN74LS540, SN74LS541 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

D2546, AUGUST 1979 – REVISED JUNE 1980

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- P-N-P Inputs Reduce D-C Loading
- Hysteresis at Inputs Improves Noise Margins
- Data Flow-thru Pinout (All Inputs on Opposite Side from Outputs)

SN54LS' . . . J PACKAGE
SN74LS' . . . J OR N PACKAGE
(TOP VIEW)



description

These octal buffers and line drivers are designed to have the performance of the popular SN54LS240/SN74LS240 series and, at the same time, offer a pinout having the inputs and outputs on opposite sides of the package. This arrangement greatly enhances printed circuit board layout.

The three-state control gate is a 2-input NOR such that if either $\overline{G}1$ or $\overline{G}2$ are high, all eight outputs are in the high-impedance state.

The 'LS540 offers inverting data and the 'LS541 offers true data at the outputs.

The SN54LS540 and SN54LS541 are characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LS540 and SN74LS541 are characterized for operation from 0°C to 70°C.

TYPE	RATED I_{OL} (SINK CURRENT)	RATED I_{OH} (SOURCE CURRENT)	TYPICAL POWER DISSIPATION (ENABLED) 'LS540	'LS541
SN54LS'	12 mA	–12 mA	92.5 mW	120 mW
SN74LS'	24 mA	–15 mA	92.5 mW	120 mW

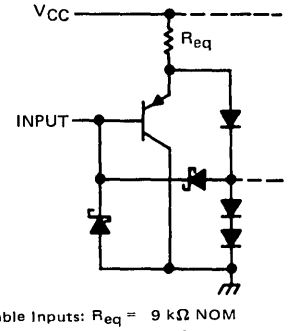
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS540, SN54LS541 . . . . . –55°C to 125°C
SN74LS540, SN74LS541 . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

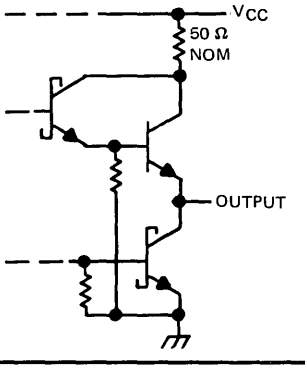
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



Enable Inputs: R_{eq} = 9 kΩ NOM
All Other Inputs: R_{eq} = 10 kΩ NOM

TYPICAL OF ALL OUTPUTS



TEXAS INSTRUMENTS
INCORPORATED
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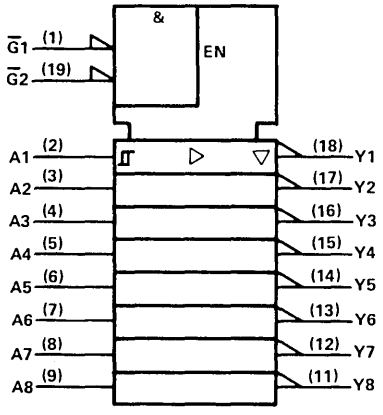
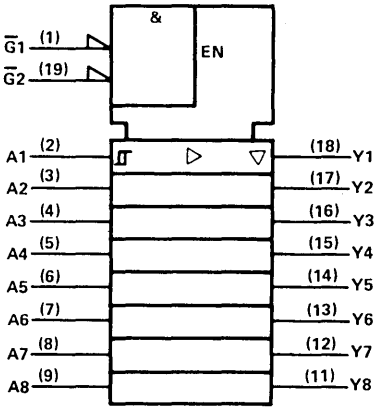
logic symbols

'LS540

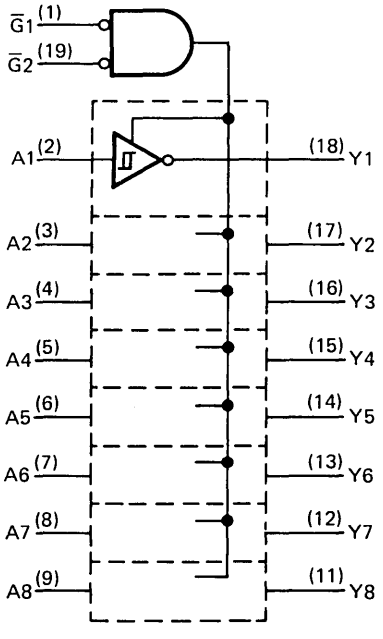


'LS541

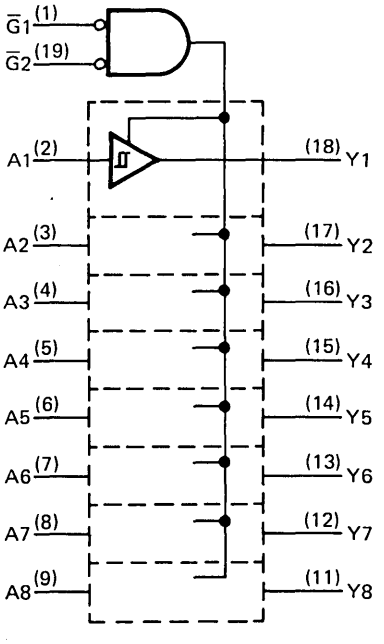


functional block diagram (positive logic)

'LS540



'LS541



recommended operating conditions

PARAMETER	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−12			−15	mA
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
	Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = MIN		0.2	0.4		0.2	0.4		V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, I_{OH} = −3 mA	2.4	3.4		2.4	3.4		V
		V_{CC} = MIN, V_{IL} = 0.5 V,	V_{IH} = 2 V, I_{OH} = MAX	2			2			
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = V_{IL}max	V_O = 2.7 V			20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied		V_O = 0.4 V			−20			−20	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
I_{IH}	High-level input current, any input	V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−0.2			−0.2	mA
I_{OS}	Short-circuit output current♦	V_{CC} = MAX		−40		−225	−40		−225	mA
I_{CC}	Supply current	Outputs high	'LS540		13	25		13	25	mA
			'LS541		18	32		18	32	
		Outputs low	'LS540		24	45		24	45	
			'LS541		30	52		30	52	
		All outputs disabled	'LS540		30	52		30	52	
			'LS541		32	55		32	55	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
♦Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		'LS540			'LS541			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 45 pF, See Note 2	R_L = 667 Ω,		9	15		9	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output				9	15		10	18	ns
t_{PZL}	Output enable time to low level				25	38		25	38	ns
t_{PZH}	Output enable time to high level				15	25		20	32	ns
t_{PLZ}	Output disable time from low level	C_L = 5 pF, See Note 2	R_L = 667 Ω,		15	25		18	29	ns
t_{PHZ}	Output disable time from high level				10	18		10	18	ns

NOTE 2: Load circuit and voltage waveforms are shown on page 3-11 of *The TTL Data Book for Design Engineers*, Second Edition, LCC4112.

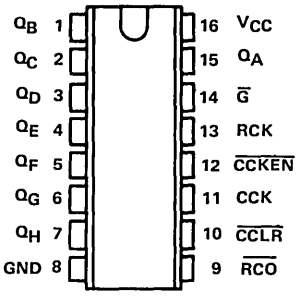
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TYPES SN54LS590, SN54LS591, SN74LS590, SN74LS591
8-BIT BINARY COUNTERS WITH OUTPUT REGISTERS

D2632, JANUARY 1981

- 8-Bit Counter with Register
- Parallel Register Outputs
- Counter has Direct Clear
- Choice of 3-State ('LS590) or Open-Collector ('LS591) Register Outputs
- Guaranteed Counter Frequency . . . . DC to 20 MHz

SN54LS590, SN54LS591 . . J OR W PACKAGE
SN74LS590, SN74LS591 . . J OR N PACKAGE
(TOP VIEW)



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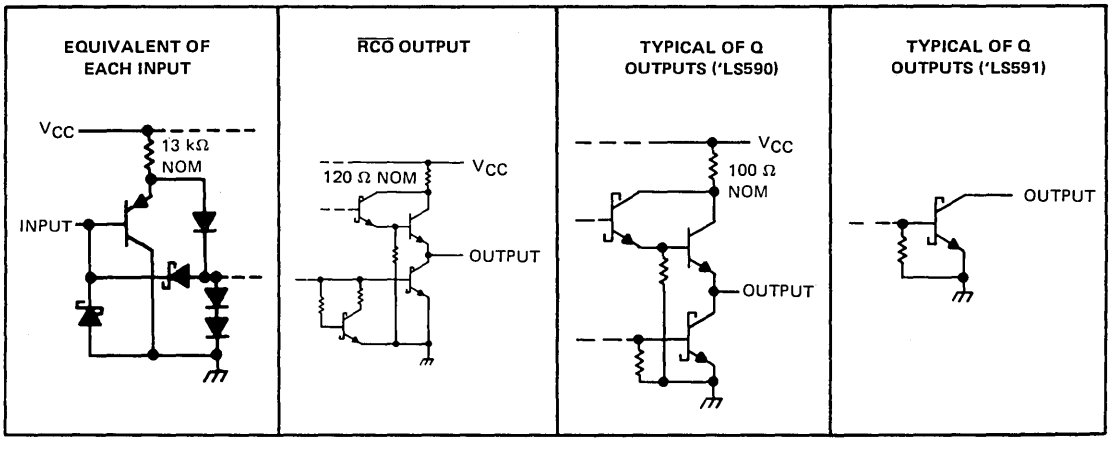
description

These devices contain an 8-bit binary counter that feeds an 8-bit storage register. The storage register has parallel outputs. Separate clocks are provided for both the binary counter and storage register. The binary counter features a direct clear input $\overline{CCLR}$ and a count enable input $\overline{CCKEN}$. For cascading a ripple carry output $\overline{RCO}$ is provided. Expansion is easily accomplished by tying $\overline{RCO}$ of the first stage to $\overline{CCKEN}$ of the second stage, etc.

Both the counter and register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the counter state will always be one count ahead of the register. Internal circuitry prevents clocking from the clock enable.

schematics of inputs and outputs



PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS INSTRUMENTS
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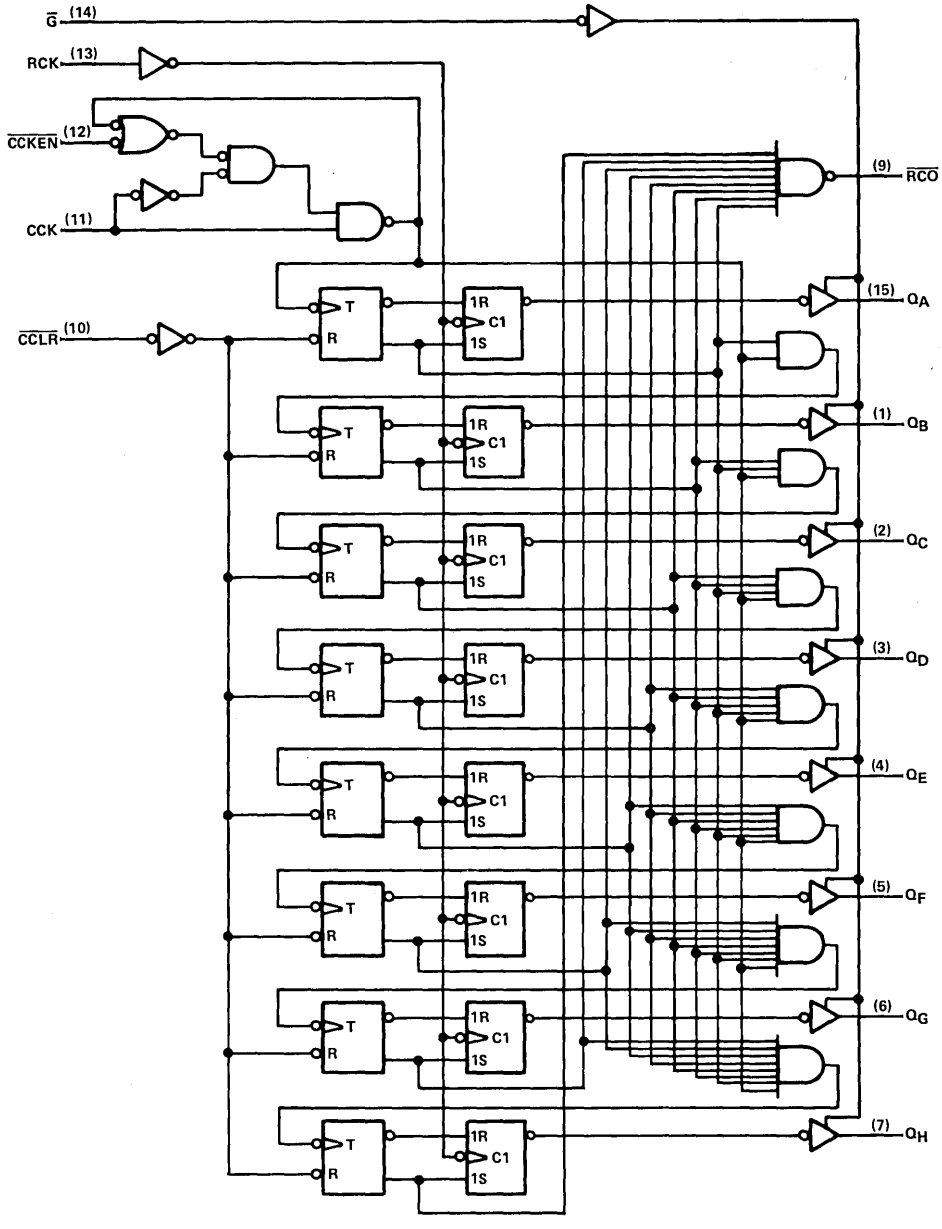
functional block diagram (positive logic)



TEXAS INSTRUMENTS
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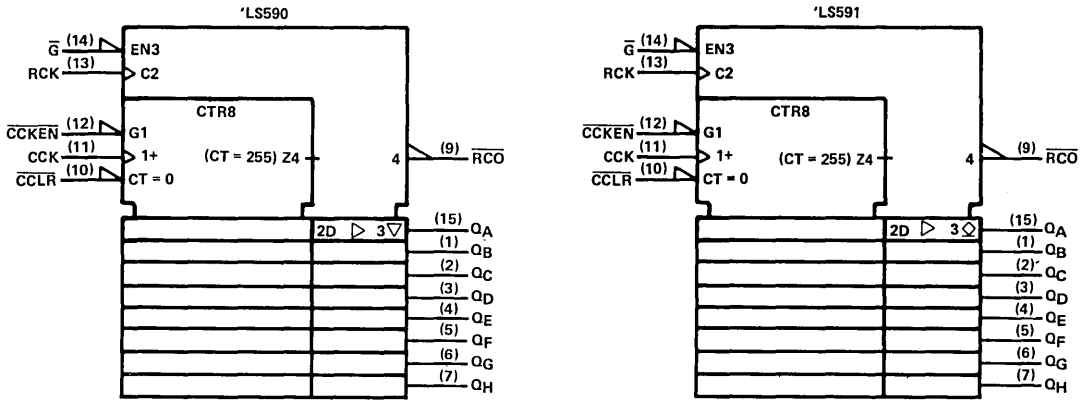
logic symbols



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54LS590, SN54LS591 . . . . . −55°C to 125°C
SN74LS590, SN74LS591 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}	Q, 'LS591 only			5.5			5.5	V
High-level output current, I_{OH}	$\overline{RCO}$			−400			−400	μA
	Q, 'LS590 only			−1			−2.6	mA
Low-level output current, I_{OL}	$\overline{RCO}$			4			8	mA
	Q			12			24	
Counter clock frequency, f_{CCK}		0		20	0		20	MHz
Width of counter clock pulse, $t_{w(CCK)}$		25			25			ns
Width of counter clear pulse, $t_{w(CCLR)}$		20			20			ns
Width of register clock pulse, $t_{w(RCK)}$		20			20			ns
Count enable time, t_{enable}	$\overline{CCKEN}$↓ to CCK↑	20			20			ns
Clear inactive-state setup time, t_{su}	$\overline{CCLR}$↑ to CCK↑	20			20			ns
Setup time, t_{su} (see Note 1)	CCK↑ to RCK↑	40			40			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

NOTE 1: This setup time ensures the register will see stable data from the counter outputs. The clocks may be tied together in which case the register state will be one clock pulse behind the counter.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS' MIN	SN54LS' TYP‡	SN54LS' MAX	SN74LS' MIN	SN74LS' TYP‡	SN74LS' MAX	UNIT
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC}=MIN, I_I=−18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	'LS590 Q	V_{CC}=MIN, V_{IH}=2 V, V_{IL}=V_{IL} max	I_{OH}=−1 mA	2.4	3.2					V
				I_{OH}=−2.6 mA				2.4	3.1		
		$\overline{RCO}$		I_{OH}=−400 μA	2.5	3.4		2.7	3.4		
I_{OH}	High-level output current	'LS591 Q	V_{CC}=MIN, V_{IH}=2 V, V_{IL}=V_{IL} max	V_{OH}=5.5V			100			100	μA
V_{OL}	Low-level output voltage	Q	V_{CC}=MIN, V_{IH}=2 V, V_{IL}=V_{IL} max	I_{OL}=12 mA		0.25	0.4		0.25	0.4	V
				I_{OL}=24 mA					0.35	0.5	
		$\overline{RCO}$		I_{OL}=4 mA		0.25	0.4		0.25	0.4	
				I_{OL}=8 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	'LS590 Q	V_{CC}=MAX, V_{IH}=2 V, V_{IL}=V_{IL} max	V_O=2.7 V			20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied	'LS590 Q	V_{CC}=MAX, V_{IH}=2 V, V_{IL}=V_{IL} max	V_O=0.4 V			−20			−20	μA
I_I	Input current at maximum input voltage		V_{CC}=MAX, V_I=7 V				0.1			0.1	mA
I_{IH}	High-level input current		V_{CC}=MAX, V_I=2.7 V				20			20	μA
I_{IL}	Low-level input current		V_{CC}=MAX, V_I=0.4 V				−0.2			−0.2	mA
I_{OS}	Short-circuit output current§	'LS590 Q	V_{CC}=MAX, V_O=0 V		−30		−130	−30		−130	mA
		$\overline{RCO}$			−20		−100	−20		−100	
I_{CC}	Supply current	'LS590	V_{CC}=MAX, All possible inputs grounded, All outputs open	ICCH		26			26		mA
				ICCL		36			36		
				ICCZ		38			38		
		'LS591		ICCH		26			26		
				ICCL		36			36		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, see note 2

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS590 MIN	'LS590 TYP	'LS590 MAX	'LS591 MIN	'LS591 TYP	'LS591 MAX	UNIT
f_{max}	CCK	$\overline{RCO}$	R_L = 2 kΩ, C_L = 15 pF	20	35		20	35		MHz
t_{PLH}	CCK↑	$\overline{RCO}$			15			15		ns
t_{PHL}	CCK↑	$\overline{RCO}$			20			20		ns
t_{PLH}	$\overline{CCLR}$↓	$\overline{RCO}$			25			25		ns
t_{PLH}	RCK↑	Q	R_L = 667 Ω, C_L = 45 pF		15			30		ns
t_{PHL}	RCK↑	Q			20			20		ns
t_{PZH}	$\overline{G}$↓	Q			15					ns
t_{PZL}	$\overline{G}$↓	Q			20					ns
t_{PHZ}	$\overline{G}$↑	Q	R_L = 667 Ω, C_L = 5 pF		15					ns
t_{PLZ}	$\overline{G}$↑	Q			15					ns
t_{PLH}	$\overline{G}$↑	Q	R_L = 667 Ω, C_L = 45 pF					30		ns
t_{PHL}	$\overline{G}$↓	Q						20		ns

NOTE 2: Load circuit and voltage waveforms are shown on page 3-11 of *The TTL Data Book for Design Engineers*, Second Edition, LCC4112.

TEXAS INSTRUMENTS
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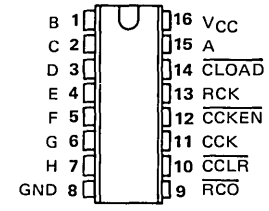
TYPES SN54LS592, SN54LS593, SN74LS592, SN74LS593
8-BIT BINARY COUNTERS WITH INPUT REGISTERS

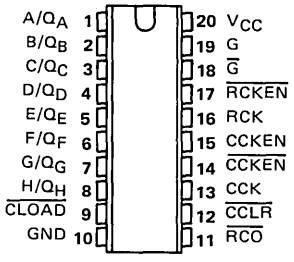
D2633, JANUARY 1981

- Parallel Register Inputs ('LS592)
- Parallel 3-State I/O: Register Inputs/Counter Outputs ('LS593)
- Counter has Direct Overriding Load and Clear
- Guaranteed Counter Frequency . . . DC to 20 MHz

SN54LS592 . . J OR W PACKAGE
SN74LS592 . . J OR N PACKAGE
(TOP VIEW)



SN54LS593 . . J PACKAGE
SN74LS593 . . J OR N PACKAGE
(TOP VIEW)



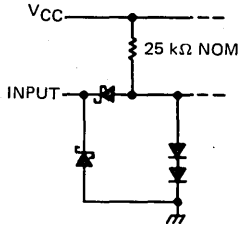
description

The 'LS592 comes in a 16-pin package and consists of a parallel input, 8-bit storage register feeding an 8-bit binary counter. Both the register and the counter have individual positive edge-triggered clocks. In addition, the counter has direct load and clear functions. Expansion is easily accomplished by connecting $\overline{RCO}$ of the first stage to the count enable of the second stage, etc.

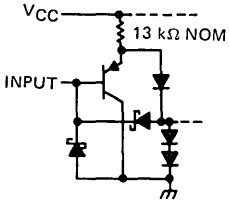
The 'LS593 comes in a 20-pin package and has all the features of the 'LS592 plus 3-state I/O, which provides parallel counter outputs.

schematics of inputs and outputs

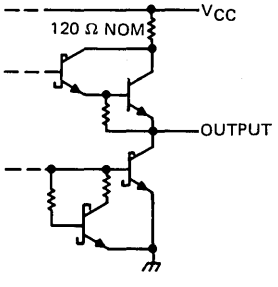
EQUIVALENT OF A THRU H INPUTS



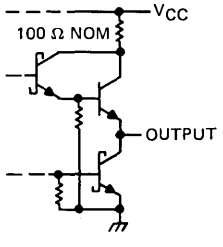
EQUIVALENT OF ALL OTHER INPUTS



$\overline{RCO}$ OUTPUT



TYPICAL OF Q OUTPUTS
('LS593 ONLY)



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PRODUCT PREVIEW

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TEXAS INSTRUMENTS
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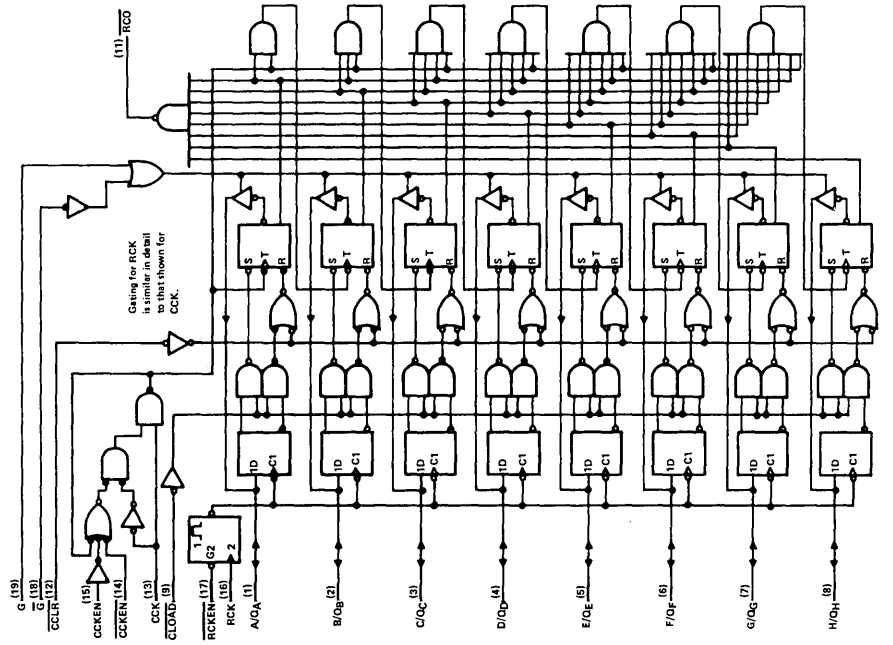
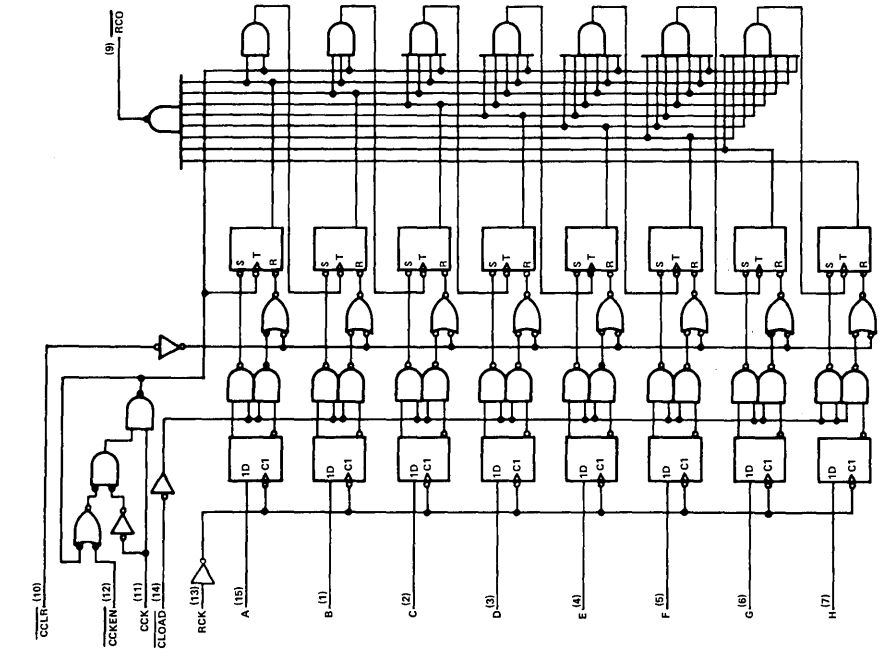
functional block diagrams (positive logic)

'LS593



'LS592



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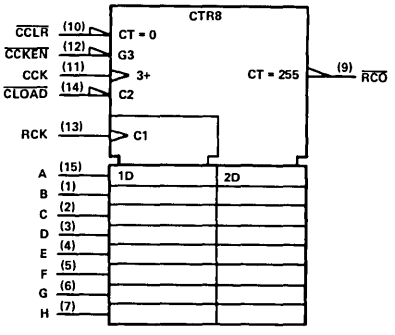
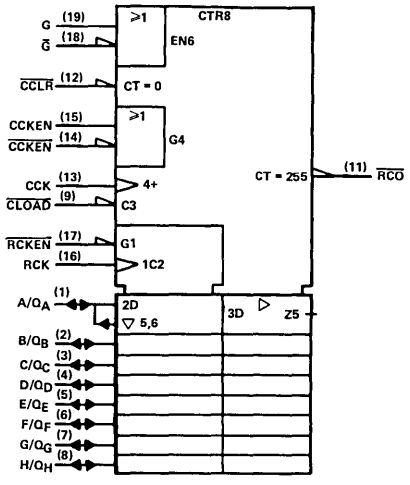
logic symbols

'LS592



'LS593



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (excluding I/O ports) . . . . . 7 V
Off-state output voltage (including I/O ports) . . . . . 5.5 V
Operating free-air temperature range: SN54LS592, SN54LS593 . . . . . −55°C to 125°C
SN74LS592, SN74LS593 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	$\overline{RCO}$			−400			−400	μA
	Q 'LS593 only			−1			−2.6	mA
Low-level output current, I_{OL}	$\overline{RCO}$			4			8	mA
	Q 'LS593 only			12			24	
Counter clock frequency, f_{CCK}		0		20	0		20	MHz
Width of counter clock pulse, t_{wCCK}		25			25			ns
Width of counter clear pulse, $t_{w\overline{CCLR}}$		20			20			ns
Width of register clock pulse, t_{wRCK}		20			20			ns
Width of counter load pulse, $t_{w\overline{CLOAD}}$		20			20			ns
Count enable time, t_{enable}	$\overline{CCKEN}$↓ to CCK↑	20			20			ns
Register enable time, t_{enable}	$\overline{RCKEN}$↓ to RCK↑ 'LS593 only	20			20			ns
Setup time, t_{su} (see Note 2)	$\overline{CCLR}$↑ to CCK↑	20			20			ns
	RCK↑ to CCK↑	40			40			
	Data A thru H to RCK↑	20			20			
Hold time, t_h		0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

NOTE 2: The RCK↑ to CCK↑ setup time ensures the counter will see stable data from the register outputs.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER				TEST CONDITIONS†		SN54LS' MIN	SN54LS' TYP‡	SN54LS' MAX	SN74LS' MIN	SN74LS' TYP‡	SN74LS' MAX	UNIT
V_{IH}	High-level input voltage					2			2			V
V_{IL}	Low-level input voltage							0.7			0.8	V
V_{IK}	Input clamp voltage			V_{CC}=MIN, I_I=−18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	'LS593 Q		V_{CC}=MIN, V_{IH}=2 V, V_{IL}=V_{IL} max	I_{OH}=−1 mA	2.4	3.2					V
					I_{OH}=−2.6 mA				2.4	3.1		
		$\overline{RCO}$			I_{OH}=−400 μA	2.5	3.4		2.7	3.4		
V_{OL}	Low-level output voltage	'LS593 Q		V_{CC}=MIN, V_{IH}=2 V, V_{IL}=V_{IL} max	I_{OL}=12 mA		0.25	0.4		0.25	0.4	V
					I_{OL}=24 mA					0.35	0.5	
		$\overline{RCO}$			I_{OL}=4 mA		0.25	0.4		0.25	0.4	
					I_{OL}=8 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	'LS593 Q		V_{CC}=MAX, V_{IH}=2 V, V_{IL}=V_{IL} max	V_O=2.7 V,			20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied	'LS593 Q		V_{CC}=MAX, V_{IH}=2 V, V_{IL}=V_{IL} max	V_O=0.4 V,			−200			−200	μA
I_I	Input current at maximum input voltage	'LS593 Q		V_{CC}=MAX,	V_I=5.5 V			0.1			0.1	mA
		Others			V_I=7 V			0.1			0.1	
I_{IH}	High-level input current			V_{CC}=MAX, V_I=2.7 V				20			20	μA
I_{IL}	Low-level input current			V_{CC}=MAX, V_I=0.4 V				−0.2			−0.2	mA
I_{OS}	Short-circuit output current§	'LS593 Q		V_{CC}=MAX, V_O=0 V		−30		−130	−30		−130	mA
		$\overline{RCO}$				−20		−100	−20		−100	
I_{CC}	Supply current	'LS592	ICCH	V_{CC}=MAX, All possible inputs grounded, All outputs open			26			26		mA
			ICCL				26			26		
		'LS593	ICCH				28			28		
			ICCL				38			38		
			ICCZ				40			40		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

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switching characteristics, V_{CC} = 5 V, T_A = 25°C, see note 3

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS592			'LS593			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	CCK	$\overline{RCO}$	R_L = 2 kΩ, C_L = 15 pF	20	35		20	35		MHz
t_{PLH}	CCK↑	Q	R_L = 667 Ω, C_L = 45 pF					15		ns
t_{PHL}	CCK↑	Q						20		ns
t_{PLH}	$\overline{CLOAD}$↓	Q						15		ns
t_{PHL}	$\overline{CLOAD}$↓	Q						20		ns
t_{PHL}	$\overline{CCLR}$↓	Q						25		ns
t_{PZH}	G↑	Q						12		ns
t_{PZL}	G↑	Q						17		ns
t_{PZH}	$\overline{G}$↓	Q						15		ns
t_{PZL}	$\overline{G}$↓	Q						20		ns
t_{PHZ}	G↓	Q	R_L = 667 Ω, C_L = 5 pF					12		ns
t_{PLZ}	G↓	Q						13		ns
t_{PHZ}	$\overline{G}$↑	Q						15		ns
t_{PLZ}	$\overline{G}$↑	Q						15		ns
t_{PLH}	CCK↑	$\overline{RCO}$	R_L = 2 kΩ, C_L = 15 pF		15			15		ns
t_{PHL}	CCK↑	$\overline{RCO}$			20			20		ns
t_{PLH}	$\overline{CLOAD}$↓	$\overline{RCO}$			15			15		ns
t_{PHL}	$\overline{CLOAD}$↓	$\overline{RCO}$			20			20		ns
t_{PLH}	$\overline{CCLR}$↓	$\overline{RCO}$			25			25		ns
t_{PLH}	RCK↑	$\overline{RCO}$	R_L = 2 kΩ, C_L = 15 pF, $\overline{CLOAD}$ = L		30			30		ns
t_{PHL}	RCK↑	$\overline{RCO}$			35			35		ns

NOTE 3: For load circuit and voltage waveforms see page 3-11 of *"The TTL Data Book for Design Engineers"*, second edition.

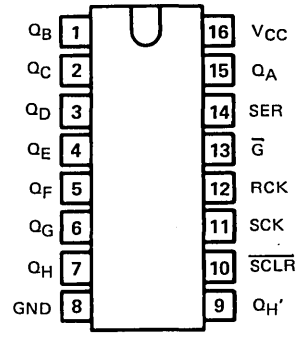
f_{max} ≡ maximum clock frequency
t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
t_{PZH} ≡ Output enable time to high level
t_{PZL} ≡ Output enable time to low level
t_{PHZ} ≡ Output disable time from high level
t_{PLZ} ≡ Output disable time from low level

TYPES SN54LS595, SN54LS596, SN74LS595, SN74LS596
8-BIT SHIFT REGISTERS WITH OUTPUT LATCHES

D2634, JANUARY 1981

- 8-Bit Serial-In, Parallel-Out Shift Registers With Storage
- Choice of 3-State ('LS595) or Open-Collector ('LS596) Parallel Outputs
- Shift Register Has Direct Clear
- Guaranteed Shift Frequency: DC to 20 MHz

SN54LS595, SN54LS596 . . J OR W PACKAGE
SN74LS595, SN74LS596 . . J OR N PACKAGE
(TOP VIEW)

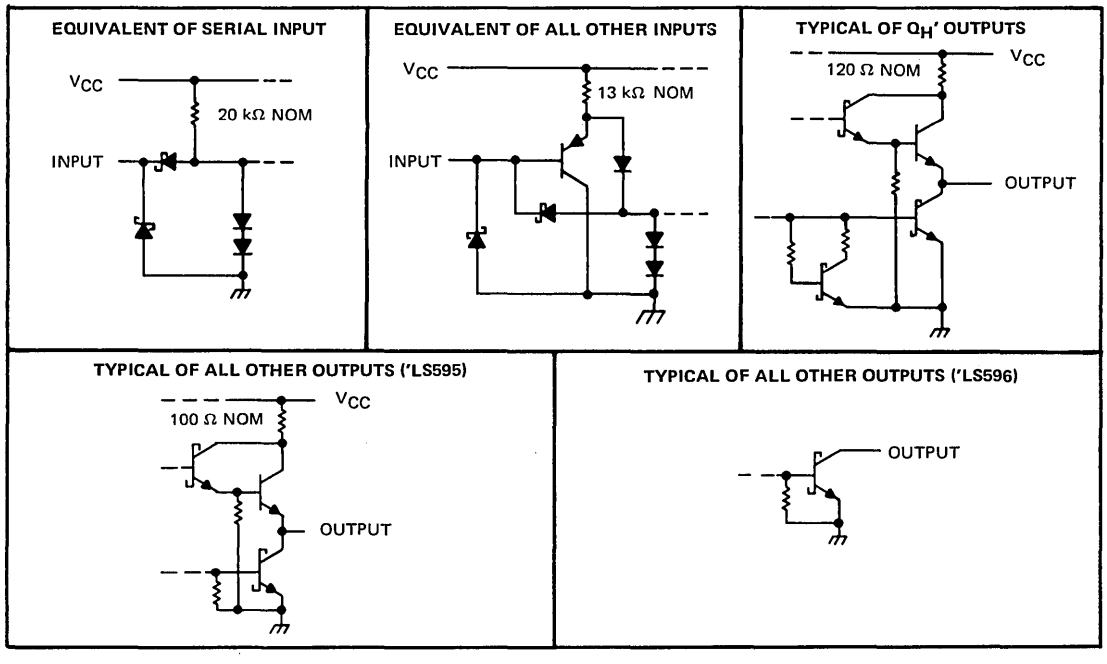


description

These devices each contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state ('LS595) or open-collector ('LS596) outputs. Separate clocks are provided for both the shift register and the storage register. The shift register has a direct-overriding clear, serial input, and serial output pins for cascading.

Both the shift register and storage register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the shift register state will always be one clock pulse ahead of the storage register.

schematics of inputs and outputs



PRODUCT PREVIEW

This draft contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

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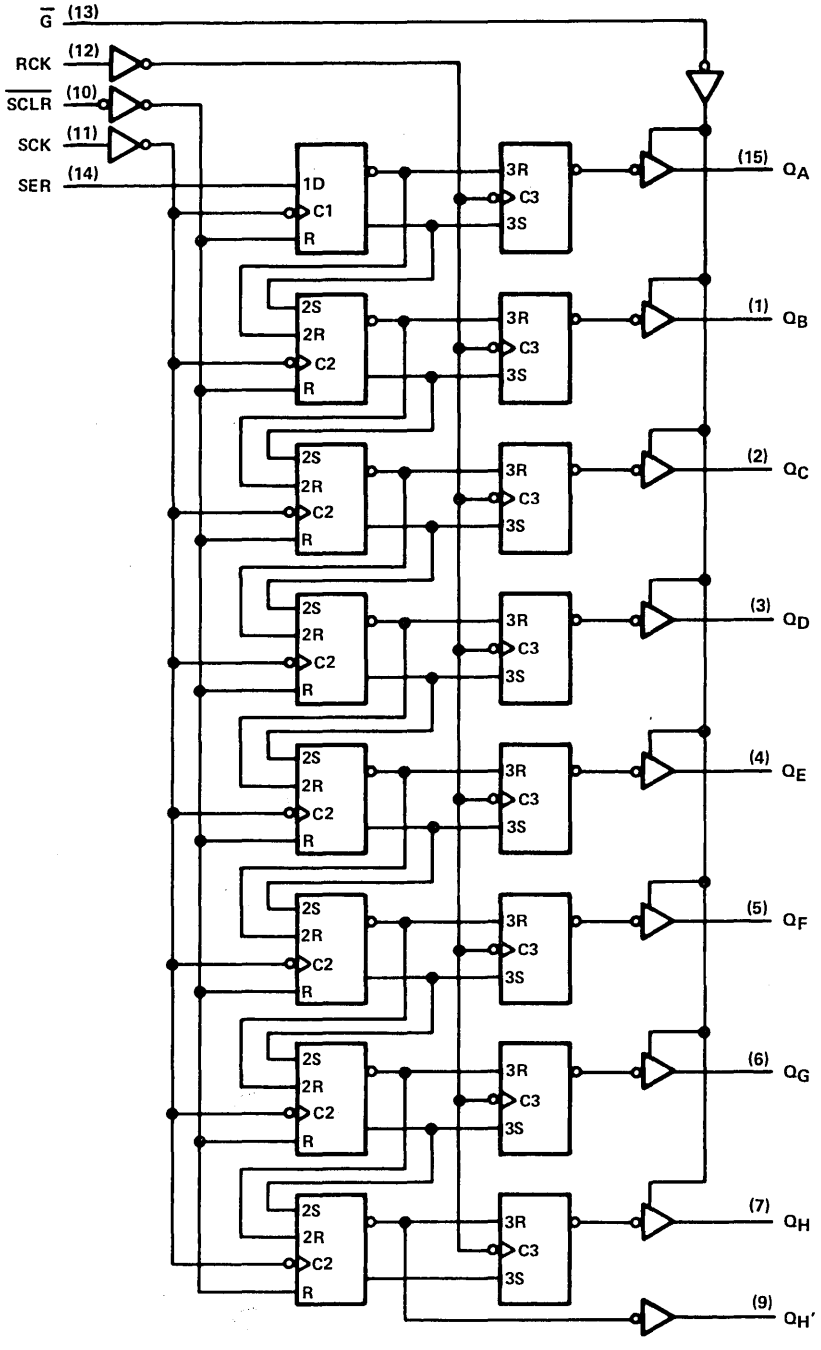
functional block diagram (positive logic)



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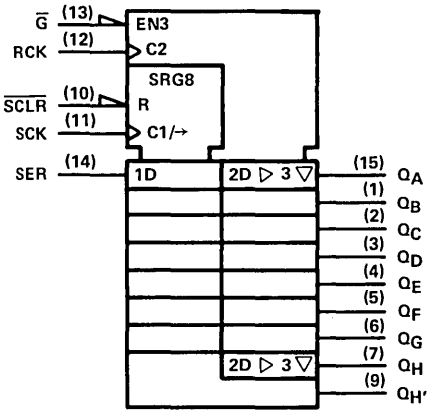
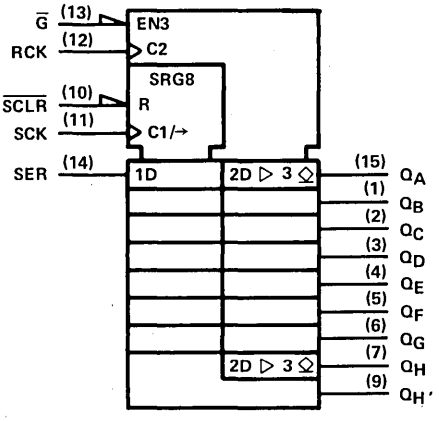
logic symbols

'LS595



'LS596



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54LS595, SN54LS596 . . . . . −55°C to 125°C
SN74LS595, SN74LS596 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}	Q_A thru Q_H, 'LS596 only			5.5			5.5	V
High-level output current, I_{OH}	$Q_{H'}$			−0.4			−0.4	mA
	Q_A thru Q_H			−1			−1	
Low-level output current, I_{OL}	$Q_{H'}$			4			8	mA
	Q			12			24	
Shift clock frequency, $f_{(SCK)}$		0		20	0		20	MHz
Width of shift clock pulse, $t_{w(SCK)}$		25			25			ns
Width of register clock pulse, $t_{w(RCK)}$		20			20			ns
Setup time, t_{su}	$\overline{SCLR}$↑ to SCK↑	20			20			ns
	SER to SCK↑	20			20			
	SCK↑ to RCK↑ (see Note 2)	40			40			
Hold time, t_h	SER from SCK↑	0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

NOTE 2: This setup time ensures the register will see stable data from the shift-register outputs. The clocks may be connected together in which case the storage register state will be one clock pulse behind the shift register.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	'LS595 Q	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max,	I_{OH} = −1 mA	2.4	3.2					V
				I_{OH} = −2.6 mA				2.4	3.1		
		Q_H'		I_{OH} = −0.4 mA	2.5	3.4		2	3.4		
I_{OH}	High-level output current	'LS596 Q	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max, V_{OH} = 5.5 V				100			100	μA
V_{OL}	Low-level output voltage	Q	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
		Q_H'		I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
				I_{OL} = 8 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	'LS595 Q	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = V_{IL} max, V_O = 2.7 V				20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied	'LS595 Q	V_{CC} MAX, V_{IH} = 2 V, V_{IL} = V_{IL} max, V_O = 0.4 V				−20			−20	μA
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	SER	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
		All others					−0.2			−0.2	
I_{OS}	Short-circuit output current§	'LS595 Q	V_{CC} = MAX, V_O = 0		−30		−130	−30		−130	mA
		Q_H'			−20		−100	−20		−100	
I_{CCH}	Supply current, outputs high	'LS595	V_{CC} = MAX, All possible inputs grounded, All outputs open			26			26		mA
		'LS596				26			26		
I_{CCL}	Supply current, outputs low	'LS595				36			36		mA
		'LS596				38			38		
I_{CCZ}	Supply current, outputs off	'LS595				38			38		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, see note 3

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS595			'LS596			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	SCK↑	Q_H'	R_L = 2 kΩ, C_L = 15 pF		10			10		ns
t_{PHL}					15			15		
t_{PLH}	RCK↑	Q_A thru Q_H	R_L = 667 Ω, C_L = 45 pF		15			30		ns
t_{PHL}					20			20		
t_{PZH}	$\overline{G}$↓	Q_A thru Q_H			15					ns
t_{PZL}					20					
t_{PHZ}	$\overline{G}$↑	Q_A thru Q_H	R_L = 667 Ω, C_L = 5 pF		15					ns
t_{PLZ}					15					
t_{PLH}	$\overline{G}$↑	Q_A thru Q_H	R_L = 667 Ω, C_L = 45 pF					30		ns
t_{PHL}	$\overline{G}$↓	Q_A thru Q_H						20		

NOTE 3: Load circuit and voltage waveforms are shown on page 3-11 of *The TTL Data Book for Design Engineers*, Second Edition, LCC4112.

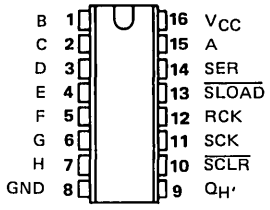
¶ t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
t_{PHZ} ≡ output disable time from high level
t_{PLZ} ≡ output disable time from low level

TYPES SN54LS597, SN54LS598, SN74LS597, SN74LS598
8-BIT SHIFT REGISTERS WITH INPUT LATCHES

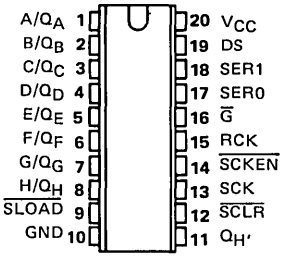
D2635, JANUARY 1981

- 8-Bit Parallel Storage Register Inputs ('LS597)
- Parallel 3-State I/O, Storage Register Inputs, Shift Register Outputs ('LS598)
- Shift Register has Direct Overriding Load and Clear
- Guaranteed Shift Frequency . . . DC to 20 MHz

SN54LS597 . . J OR W PACKAGE
SN74LS597 . . J OR N PACKAGE
(TOP VIEW)



SN54LS598 . . J PACKAGE
SN74LS598 . . J OR N PACKAGE
(TOP VIEW)



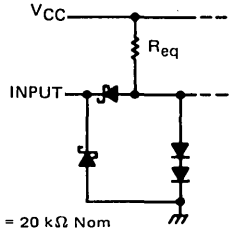
description

The 'LS597 comes in a 16-pin package and consists of an 8-bit storage latch feeding a parallel-in, serial-out 8-bit shift register. Both the storage register and shift register have positive-edge triggered clocks. The shift register also has direct load (from storage) and clear inputs.

The 'LS598 comes in a 20-pin package and has all the features of the 'LS597 plus 3-state I/O ports that provide parallel shift register outputs and also has multiplexed serial data inputs.

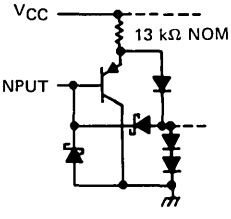
schematics of inputs and outputs

EQUIVALENT OF ALL DATA INPUTS

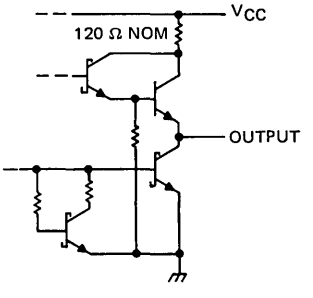


Serial A,B: R_{eq} = 20 kΩ Nom
A thru H: R_{eq} = 25 kΩ Nom

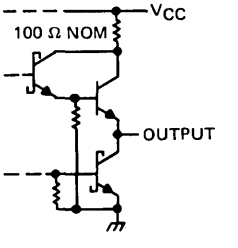
EQUIVALENT OF ALL OTHER INPUTS



Q_H' OUTPUT



TYPICAL OF Q_A THRU Q_H OUTPUTS ('LS598 ONLY)



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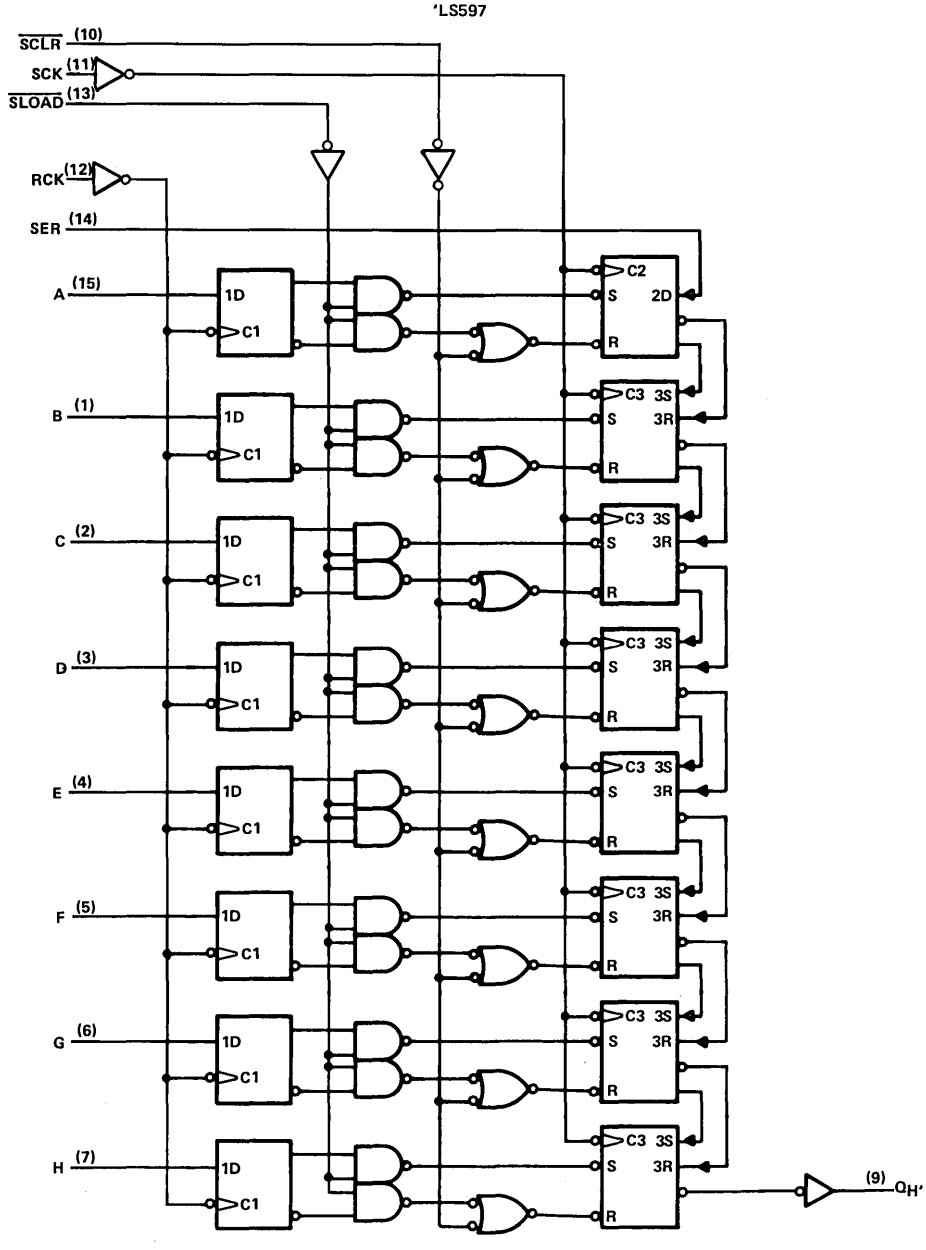
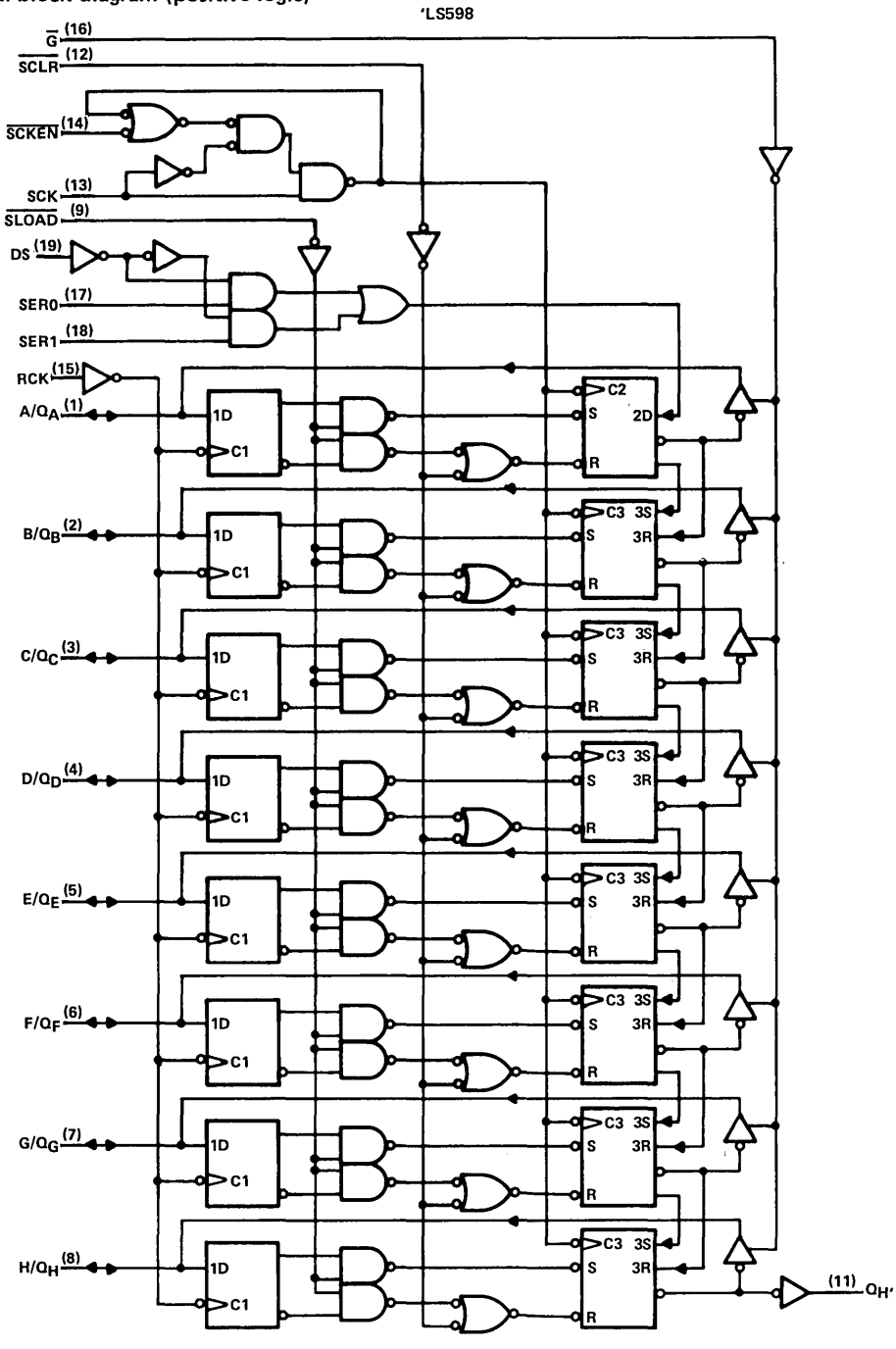
functional block diagram (positive logic)



functional block diagram (positive logic)



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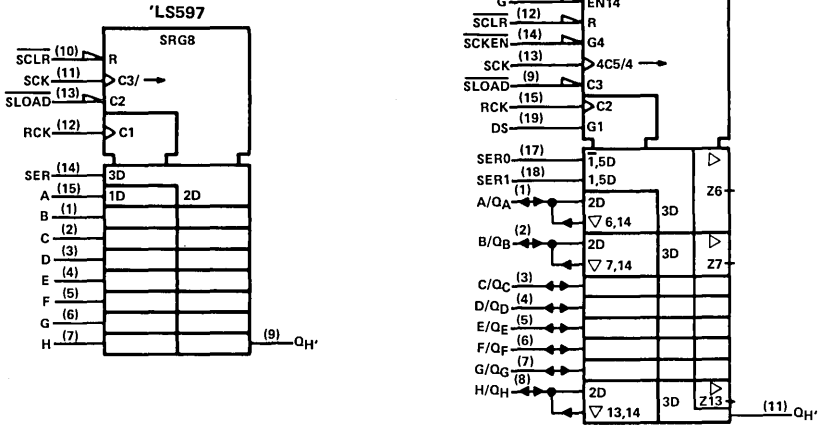
logic symbols



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (excluding I/O ports) . . . . . 7 V
Off-state output voltage (including I/O ports) . . . . . 5.5 V
Operating free-air temperature range: SN54LS597, SN54LS598 . . . . . −55°C to 125°C
SN74LS597, SN74LS598 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

		SN54LS'			SN74LS			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	$Q_{H'}$			−400			−400	μA
	Q_A thru Q_H ('LS598 only)			−1			−2.6	mA
Low-level output current, I_{OL}	$Q_{H'}$			4			8	mA
	Q_A thru Q_H ('LS598 only)			12			24	
Shift clock frequency, f_{SCK}		0		20	0		20	MHz
Pulse width, t_w	SCK	25			25			ns
	RCK	20			20			
	$\overline{SCLR}$	20			20			
	$\overline{SLOAD}$	20			20			
Shift enable time, t_{enable} ('LS598 only)	SCKEN↓ to SCK↑	20			20			ns
Setup time, t_{su} (see Note 2)	$\overline{SCLR}$↑ to SCK↑	20			20			ns
	RCK↑ to SCK↑	40			40			
	SER to SCK↑	20			20			
Hold time, t_h		0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

NOTE 2: The RCK↑ to SCK↑ setup time ensures that the shift register will see stable data coming from the input register.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS' MIN	SN54LS' TYP‡	SN54LS' MAX	SN74LS' MIN	SN74LS' TYP‡	SN74LS' MAX	UNIT
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC}=MIN, I_I=−18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	'LS598 Q	V_{CC}=MIN, V_{IH}=2 V, V_{IL}=V_{IL} max	I_{OH}=−1 mA	2.4	3.2					V
		Q_H'		I_{OH}=−2.6 mA				2.4	3.1		
				I_{OH}=−400 μA	2.5	3.4		2.7	3.4		
V_{OL}	Low-level output voltage	'LS598 Q	V_{CC}=MIN, V_{IH}=2 V, V_{IL}=V_{IL} max	I_{OL}=12 mA		0.25	0.4		0.25	0.4	V
				I_{OL}=24 mA					0.35	0.5	
		Q_H'		I_{OL}=4 mA		0.25	0.4		0.25	0.4	
				I_{OL}=8 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	'LS598 Q	V_{CC}=MAX, V_{IH}=2 V, V_{IL}=V_{IL} max	V_O=2.7 V			20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied	'LS598 Q	V_{CC}=MAX, V_{IH}=2 V, V_{IL}=V_{IL} max	V_O=0.4 V			−200			−200	μA
I_I	Input current at maximum input voltage	'LS598 Q	V_{CC}=MAX,	V_I=5.5 V			0.1			0.1	mA
		Others		V_I=7 V			0.1			0.1	
I_{IH}	High-level input current		V_{CC}=MAX, V_I=2.7 V				20			20	μA
I_{IL}	Low-level input current		V_{CC}=MAX, V_I=0.4 V				−0.2			−0.2	mA
I_{OS}	Short-circuit output current§	'LS598 Q	V_{CC}=MAX, V_O=0 V		−30		−130	−30		−130	mA
		Q_H'			−20		−100	−20		−100	
I_{CC}	Supply current	'LS597	V_{CC}=MAX, All possible inputs grounded, All outputs open	ICCH		26			26		mA
				ICCL		26			26		
		'LS598		ICCH		28			28		
				ICCL		38			38		
				ICCZ		40			40		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, see note 2

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS597 MIN	'LS597 TYP	'LS597 MAX	'LS598 MIN	'LS598 TYP	'LS598 MAX	UNIT
f_{max}	SCK		R_L = 2 kΩ, C_L = 15 pF	20	35		20	35		MHz
t_{PLH}	SCK↑	Q_H'			15			15		ns
t_{PHL}	SCK↑	Q_H'			20			20		ns
t_{PLH}	$\overline{SLOAD}$↓	Q_H'			15			15		ns
t_{PHL}	$\overline{SLOAD}$↓	Q_H'			20			20		ns
t_{PHL}	$\overline{SCLR}$↓	Q_H'			25			25		ns
t_{PLH}	RCK↑	Q_H'	R_L = 2 kΩ, C_L = 15 pF, $\overline{SLOAD}$ = L		30					ns
t_{PHL}	RCK↑	Q_H'			35					ns
t_{PLH}	SCK↑	Q	R_L = 667 Ω, C_L = 45 pF					15		ns
t_{PHL}	SCK↑	Q						20		ns
t_{PLH}	$\overline{SLOAD}$↓	Q						15		ns
t_{PHL}	$\overline{SLOAD}$↓	Q						20		ns
t_{PHL}	$\overline{SCLR}$↓	Q						25		ns
t_{PZH}	$\overline{G}$↓	Q						15		ns
t_{PZL}	$\overline{G}$↓	Q						20		ns
t_{PHZ}	$\overline{G}$↑	Q	R_L = 667 Ω, C_L = 5 pF					15		ns
t_{PLZ}	$\overline{G}$↑	Q						15		ns

NOTE 2: Load circuit and voltage waveforms are shown on page 3-11 of *The TTL Data Book for Design Engineers*, Second Edition, LCC4112.

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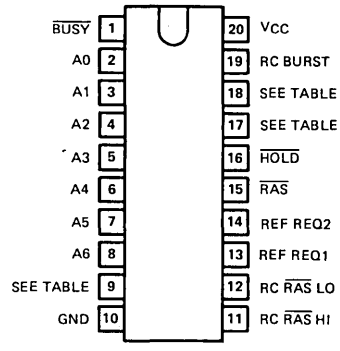
TYPES SN54LS600 THRU SN54LS603, SN74LS600 THRU SN74LS603 MEMORY REFRESH CONTROLLERS

D2547, JANUARY 1981

- Controls Refresh Cycle of 4K, 16K, and 64K Dynamic RAMs
- Creates Static RAM Appearance
- Choice of Transparent, Cycle Steal, or Burst Refresh Modes
- 3-State Outputs Drive Bus Lines Directly
- Critical Times Are User RC-Programmable to Optimize System Performance

SN54LS' . . . J PACKAGE
SN74LS' . . . J OR N PACKAGE
(TOP VIEW)



SELECTION TABLE

DEVICE	REFRESH MODES	MEMORY SIZE	PIN ASSIGNMENTS		
			PIN 9	PIN 17	PIN 18
'LS600	Transparent, Burst	4K or 16K	4K/16K	NC	NC
'LS601	Transparent, Burst	64K	A7	NC	NC
'LS602	Cycle Steal, Burst	4K or 16K	4K/16K	READY	RC CYCLE STEAL
'LS603	Cycle Steal, Burst	64K	A7	READY	RC CYCLE STEAL

NC = No internal connection.

description

The 'LS600 thru 'LS603 memory refresh controllers contain one 8-bit synchronous counter, nine 3-state buffer drivers, four RC-controlled multivibrators, and other control circuitry on a monolithic chip. They are intended for use with RAS-only-refresh dynamic RAMs. These controllers have 3-state RAS and address outputs that are in the high-impedance state when no refresh is in progress. They become active approximately 30 nanoseconds after the REF REQ pins are taken high and remain active until about 30 nanoseconds after the refresh is complete.

operating modes

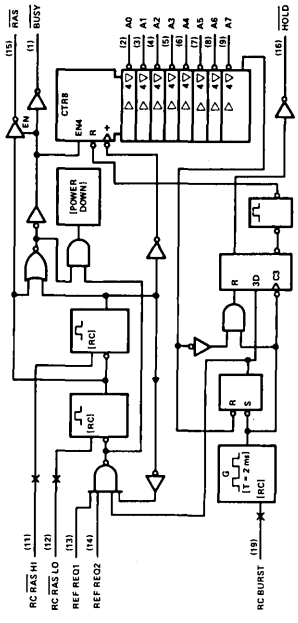
In the transparent refresh mode, row refresh cycles occur during inactive CPU-memory times so that, in most cases, the entire memory refresh sequence can be done "transparently" (without interrupting CPU operations). When the REF REQ pins are taken high to indicate an idle CPU/memory period, as many rows as possible are refreshed. A low level on BUSY signals the CPU to wait until the end of the current row refresh cycle before reinstating operations. When the RC time constant programmed at RC BURST indicates that the safe refresh time of the memory has been exceeded, the memory refresh controller will automatically signal the CPU for an emergency burst-mode refresh by taking HOLD low. The CPU must then take the REF REQ pins high and keep them at the level until HOLD goes high after all rows have been refreshed. The automatic burst refresh will be initiated by the refresh controller even when transparent or cycle-steal refresh operations are already in progress.

Cycle-steal refresh is implemented by dividing the safe refresh time into equal segments and refreshing one row in each of those segments. The safe refresh time is programmed by the time constant at RC BURST and the segment time by the time constant at RC CYCLE STEAL. A low level at READY on the 'LS602 and 'LS603 indicates to the CPU to suspend operations for one memory cycle for a row refresh. In effect it "steals" one memory cycle from the CPU.

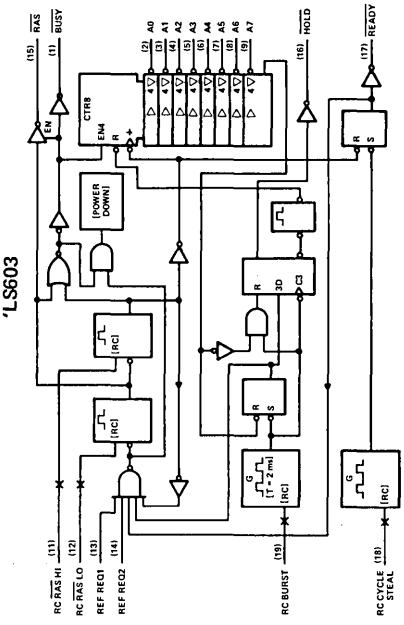
In all operating modes, the latch on the automatic burst mode circuit is reset at the end of every complete memory refresh cycle.

functional block diagrams (positive logic)

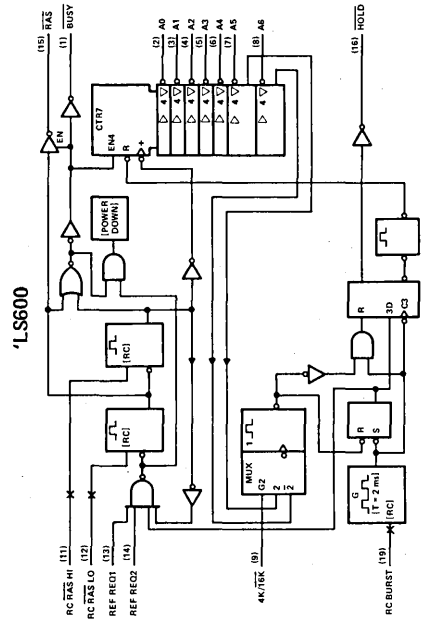
'LS601



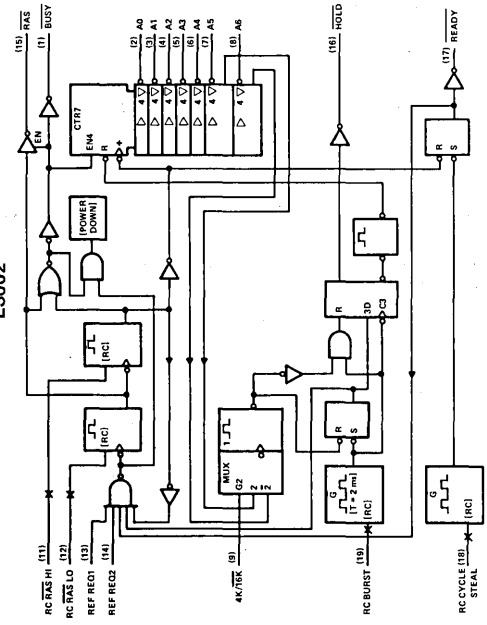
'LS603



'LS600



'LS602



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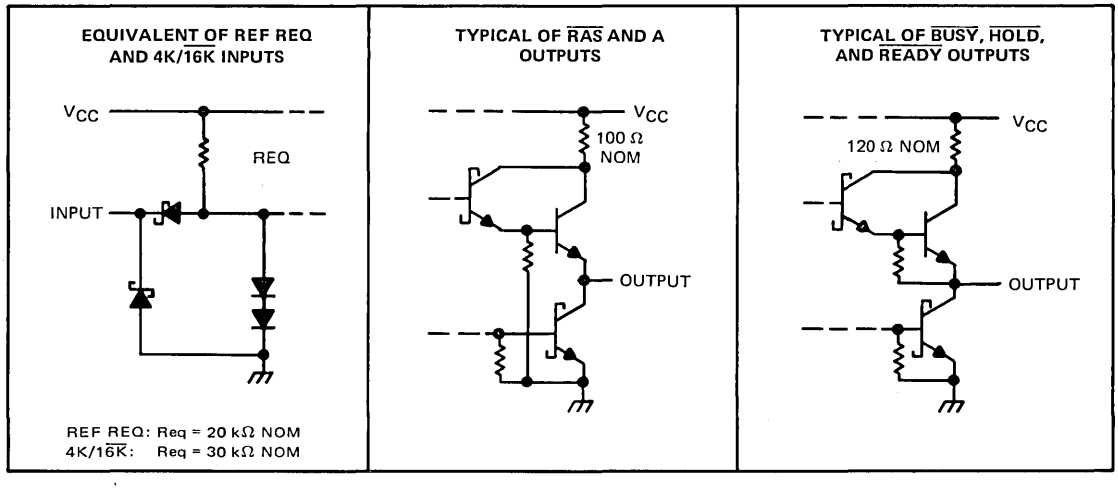
PIN FUNCTION TABLE

PIN	PIN NAME	FUNCTIONAL DESCRIPTION	
1	$\overline{\text{BUSY}}$	Active output indicates to the CPU that a refresh cycle is in progress.	
16	$\overline{\text{HOLD}}$	Active output should be a priority interrupt to the CPU for emergency burst refresh.	
15	$\overline{\text{RAS}}$	3 state output row address strobe.	
11	RC $\overline{\text{RAS}}$ HI	Timing node for high-level portion of $\overline{\text{RAS}}$. See Note 1.	
12	RC $\overline{\text{RAS}}$ LO	Timing node for low-level portion of $\overline{\text{RAS}}$. See Note 1.	
2–8	A0 thru A6	3 state output row address lines.	
9	A7	MSB row address line for 'LS601 and 'LS603 (64K-bit memory controllers).	
9	4K/$\overline{\text{16K}}$	A high input level disables the A5 row address line for 'LS600 and 'LS602. (The high level input makes the count chain 5 bits long while the low level makes the count chain 6 bits long.)	
17	$\overline{\text{READY}}$	Interrupt to CPU for cycle steal refresh ('LS602 and 'LS603).	No internal connection on 'LS600 and 'LS601.
18	RC CYCLE STEAL	Timing node that controls the $\overline{\text{READY}}$ output. See Note 1.	
19	RC BURST	Timing node for burst refresh. See Note 1.	
13, 14	REF REQ1, REF REQ2	High level on both pins starts and continues row refresh. Low on either pin inhibits refresh.	
20, 10	V_{CC}, GND	5-V power supply and network ground pins.	

NOTE 1: All timing nodes require a resistor to V_{CC} and a capacitor to GND. Programmed time is approximately equal to 0.29 RC.

2

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 2) . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54LS600 thru SN54LS603 . . . . . −55°C to 125°C
SN74LS600 thru SN74LS603 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 2: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	A, $\overline{RAS}$			−1			−2.6	mA
	All others			−400			−400	μA
Low-level output current, I_{OL}	A, $\overline{RAS}$			12			24	mA
	All others			4			8	
Width of RAS output pulse, $t_{w(RAS)}$†	High	100			100			ns
	Low	100			100			
External timing resistor, R_{ext}	RC $\overline{RAS}$ LO, RC $\overline{RAS}$ HI	1		6	1		6	kΩ
	RC BURST, RC CYCLE STEAL	1		1000	1		1000	
Operating free-air temperature, T_A		−55		125	0		70	°C

†Maximum operating frequency for the address counter corresponds to its minimum period, which is the sum of $t_{w(RAS-H)}$ min and $t_{w(RAS-L)}$ min.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −1.8 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	A, $\overline{RAS}$	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OH} = −1 mA	2.4	2.9					V
				I_{OH} = −2.6 mA				2.4	2.9		
		All others		I_{OH} = −400 μA	2.5	3.1		2.7	3.1		
V_{OL}	Low-level output voltage	A, $\overline{RAS}$	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
		All others		I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
				I_{OL} = 8 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	A, $\overline{RAS}$	V_{CC} = MAX, REF REQ at V_{IL} max	V_O = 2.7 V			20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied			V_O = 0.4 V			−20			−20	μA
I_I	Input current at maximum input voltage	REF REQ, 4K/$\overline{16K}$	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current	REF REQ, 4K/$\overline{16K}$	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	REF REQ, 4K/$\overline{16K}$	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current¶	A, $\overline{RAS}$	V_{CC} = MAX		−30		−130	−30		−130	mA
		All others			−20		−100	−20		−100	
I_{CC}	Supply current		V_{CC} = MAX, RC $\overline{RAS}$ LO & REF REQ at 0 V			50	85		50	85	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
¶Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

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switching characteristics, V_{CC} = 5 V, T_A = 25°C, see note 3

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}†	REF REQ ↑	$\overline{HOLD}$	R_L = 2 kΩ, C_L = 15 pF	311	370	437	ns
t_{PLH}†	REF REQ ↑	$\overline{BUSY}$		436	525	607	ns
t_{PHL}	REF REQ ↑	$\overline{BUSY}$			25	40	ns
t_{PLH}‡	REF REQ ↑	$\overline{RAS}$	R_L = 667 Ω, C_L = 45 pF	227	270	313	ns
t_{PZL}	REF REQ ↑	$\overline{RAS}$			28	50	ns
$t_{w(H)}$‡		$\overline{RAS}$		238	290	336	ns
$t_{w(L)}$§		$\overline{RAS}$		205	245	282	ns
t_{PHZ}†	REF REQ ↑	$\overline{RAS}$	R_L = 667 Ω, C_L = 5 pF	464	560	649	ns
t_{PLH}‡	REF REQ ↑	A	R_L = 667 Ω, C_L = 45 pF	258	310	358	ns
t_{PHL}‡	REF REQ ↑	A		243	290	340	ns
t_{PZH}	REF REQ ↑	A			24	40	ns
t_{PZL}	REF REQ ↑	A			30	50	ns
t_{PHZ}‡	REF REQ ↑	A	R_L = 667 Ω, C_L = 5 pF	460	560	656	ns
t_{PLZ}‡	REF REQ ↑	A		447	535	619	ns

†Depends on RC network at pin 11 (5 kΩ, 180 pF used for testing) and pin 12 (5 kΩ, 180 pF).

‡Depends on RC network at pin 12 (5 kΩ, 180 pF).

§Depends on RC network at pin 11 (5 kΩ, 180 pF).

NOTE 3: Load circuit and voltage waveforms are shown on page 3-11 of *The TTL Data Book for Design Engineers*, Second Edition, LCC4112.

t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
t_{PZH} ≡ Output enable time to high level
t_{PZL} ≡ Output enable time to low level
t_{PHZ} ≡ Output disable time from high level
t_{PLZ} ≡ Output disable time from low level
$t_{w(H)}$ ≡ Output pulse width, high level
$t_{w(L)}$ ≡ Output pulse width, low level

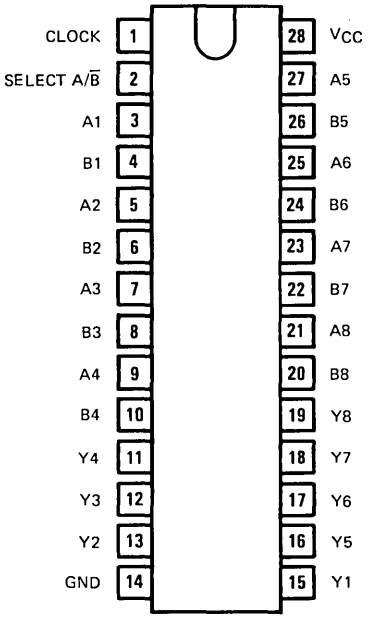
TYPES SN54LS604 THRU SN54LS607, SN74LS604 THRU SN74LS607
OCTAL 2-INPUT MULTIPLEXED LATCHES

D2545, JULY 1979

(TIM99604 THRU TIM99607)

- Choice of Outputs:
  Three-State ('LS604, 'LS606)
  Open-Collector ('LS605, 'LS607)
- 16 D-Type Registers, One for each Data Input
- Multiplexer Selects Stored Data from Either A Bus or B Bus
- Application Oriented:
  Maximum Speed ('LS604, 'LS605)
  Glitch-Free Operation ('LS606, 'LS607)

SN54LS604 thru SN54LS607 . . . J PACKAGE
SN74LS604 thru SN74LS607 . . . J OR N PACKAGE
(TOP VIEW)



description

The 'LS604 through 'LS607 multiplexed latches are ideal for storing data from two input buses, A and B, and providing the output bus with stored data from either the A or B register.

The clock loads data on the positive-going (low-level to high-level) transition. The clock pin also controls the active and high-impedance states of the outputs. When the clock pin is low, the outputs are in the high-impedance or off state. When the clock pin is high, the outputs are enabled.

The 'LS604 and 'LS605 are optimized for high-speed operation. The 'LS606 and 'LS607 are especially designed to eliminate decoding voltage spikes.

These functions are ideal for interface from a 16-bit microprocessor to a 64K RAM board. The row and column addresses can be loaded as one word from the microprocessor and then multiplexed sequentially to the RAM during the time that RAS and CAS are active.

The SN54LS604 through SN54LS607 are characterized for operation over the full military temperature range of −55°C to 125°C; the SN74LS604 through SN74LS607 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS				OUTPUTS
A1-A8	B1-B8	SELECT A/$\overline{B}$	CLOCK	Y1-Y8
A data	B data	L	↑	B data
A data	B data	H	↑	A data
X	X	X	L	Z or Off
X	X	L	H	B register stored data
X	X	H	H	A register stored data

H = high level (steady state)
L = low level (steady state)
X = irrelevant
Z = high-impedance state
Off = H if pull-up resistor is connected to open-collector output
↑ = transistion from low to high level

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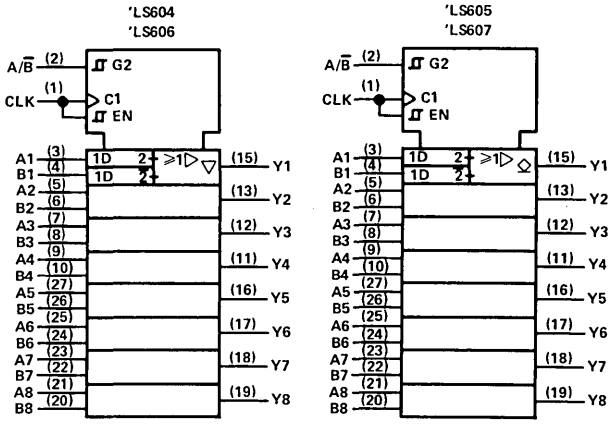
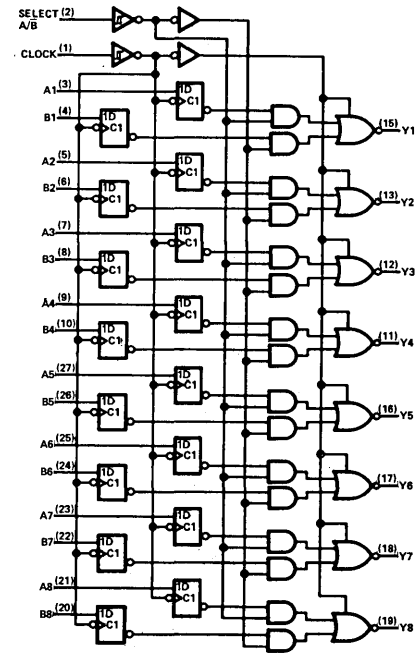
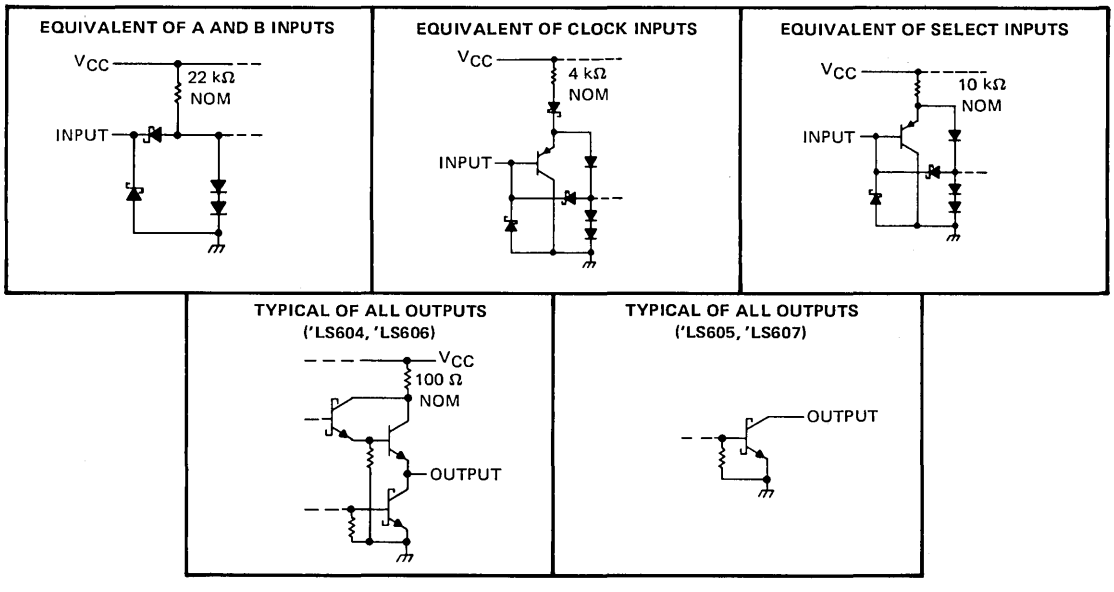
logic symbols



functional block diagram (positive logic)



schematics of inputs and outputs



recommended operating conditions

	SN54LS604 SN54LS606			SN74LS604 SN74LS606			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−1			−2.6	mA
Low-level output current, I_{OL}			12			24	mA
Width of clock pulse, t_w	20			20			ns
Setup time, t_{su}	20↑			20↑			ns
Hold time, t_h	0↑			0↑			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN54LS604 SN54LS606			SN74LS604 SN74LS606			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, I_{OH} = MAX		2.4	3.1		2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_{IL} = V_{IL} max,	V_{IH} = 2 V, V_O = 2.7 V				20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_{IL} = V_{IL} max,	V_{IH} = 2 V, V_O = 0.4				−20			−20	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 7 V	A, B			0.1			0.1	mA
				CLK, SELECT			0.1			0.1	
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V	A, B			20			20	μA
				CLK, SELECT			20			20	
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V	A, B			−0.4			−0.4	mA
				CLK, SELECT			−0.2			−0.2	
I_{OS}	Short-circuit output current§	V_{CC} = MAX			−30		−130	−30		−130	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 2			55	70		55	70	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Note more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 2: I_{CC} is tested with all inputs grounded and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TEST CONDITIONS	'LS604			'LS606			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Select $A/\overline{B}$ (Data: A = H, B = L)	C_L = 45 pF, R_L = 667 Ω, See Note 3		15	25		36	50	ns
t_{PHL}				23	35		16	30	
t_{PLH}	Select $A/\overline{B}$ (Data: A = L, B = H)			31	45		22	35	ns
t_{PHL}				19	30		22	35	
t_{PZH}	Clock			19	30		27	40	ns
t_{PZL}				28	40		35	50	
t_{PHZ}	Clock	C_L = 5 pF, R_L = 667 Ω, See Note 3		20	30		20	30	ns
t_{PLZ}				15	25		15	25	

t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, low-to-high-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
t_{PHZ} ≡ output disable time from high level
t_{PLZ} ≡ output disable time from low level
NOTE 3: Load circuits and voltage waveforms are shown on page 3-11 of *The TTL Data Book for Design Engineers*, second edition.

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recommended operating conditions

	SN54LS605 SN54LS607			SN74LS605 SN74LS607			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			12			24	mA
Width of clock pulse, t_w	20			20			ns
Setup time, t_{su}	20↑			20↑			ns
Hold time, t_h	0↑			0↑			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN54LS605 SN54LS607			SN74LS605 SN74LS607			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, V_{OH} = 5.5 V				250			250	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL} max	V_{IH} = 2 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 7 V	A, B			0.1			0.1	mA
				CLK, SELECT			0.1			0.1	
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V	A, B			20			20	μA
				CLK, SELECT			20			20	
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V	A, B			−0.4			−0.4	mA
				CLK, SELECT			−0.2			−0.2	
I_{CC}	Supply current	V_{CC} = MAX,	See Note 2			40	60		40	60	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: I_{CC} is tested with all inputs grounded and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TEST CONDITIONS	'LS605			'LS607			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Select A/$\overline{B}$ (Data: A = H, B = L)	C_L = 45 pF, R_L = 667 Ω, See Note 3		28	40		51	70	ns
t_{PHL}				28	40		21	30	
t_{PLH}	Select A/$\overline{B}$ (Data: A = L, B = H)			39	60		28	40	ns
t_{PHL}				25	40		28	40	
t_{PLH}	Clock			27	40		30	45	ns
t_{PHL}				25	40		32	45	

t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, low-to-high-level output
NOTE 3: Load circuits and voltage waveforms are shown on page 3-11 of *The TTL Data Book for Design Engineers*, second edition.

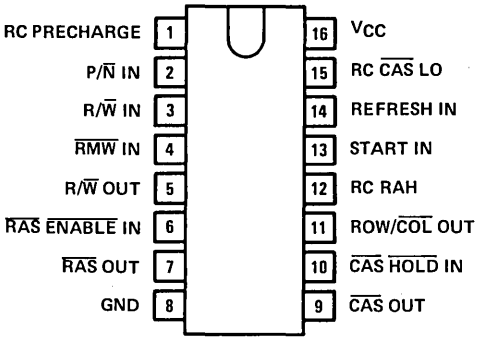
TYPES SN54LS608, SN74LS608
MEMORY CYCLE CONTROLLERS

D2548, JANUARY 1981

(TIM99608)

- Provides Correct Timing for Memory Cycles
  - Read Cycle
  - Write Cycle
  - Read-Modify-Write Cycle
  - RAS-Only Refresh Cycle
- Page or Normal Modes
- Stand-Alone Controller for CPU-to-Memory Interface
- Also Designed to be Part of a Three-Chip Set Consisting of 'LS600 thru 'LS603, 'LS604 thru 'LS607, and 'LS608
- $\overline{RAS}$ Output is 3-State to Share Bus With 'LS600 thru 'LS603
- Critical Times Are User RC-Programmable to Optimize System Performance

SN54LS608 . . . J PACKAGE
SN74LS608 . . . J OR N PACKAGE
(TOP VIEW)



description

The 'LS608 memory cycle controller is designed to interface between a microprocessor and dynamic RAM memories. It contains six RS latches, five D-type flip-flops, and more than 50 miscellaneous gates on a single chip. The 'LS608 combines maximum flexibility and ease of programming via RC nodes to allow optimum memory cycle performance.

The 'LS608 can operate as a stand-alone interface but is also designed to be part of a three-chip memory controller set. The user must select one of the 'LS600 thru 'LS603 refresh controllers and one of the 'LS604 thru 'LS607 multiplexers to use along with the 'LS608 memory cycle controller for complete dynamic RAM control.

After the user has selected and attached RC networks to pins 1, 12, and 15, the 'LS608 will deliver proper $\overline{RAS}$, $\overline{CAS}$, and READ/$\overline{WRITE}$ output signals to execute one memory cycle as the start input is switched from low to high. The actual cycle executed will depend upon steady-state input conditions of the 'LS608 as indicated in the table below.

MEMORY CYCLE	MODE	INPUT CONDITIONS						
		P/$\overline{N}$ IN	R/$\overline{W}$ IN	$\overline{RMW}$ IN	$\overline{RAS}$ $\overline{ENABLE}$ IN	$\overline{CAS}$ $\overline{HOLD}$ IN	START IN	REFRESH IN
READ	PAGE	H	H	H	L	H	↑	L
WRITE		H	L	H	L	H	↑	L
READ-MODIFY-WRITE		H	H	L	L	H	↑	L
READ	NORMAL	L	H	H	L	H	↑	L
WRITE		L	L	H	L	H	↑	L
READ-MODIFY-WRITE		L	H	L	L	H	↑	L
REFRESH	REFRESH	x	x	x	L	H	↑	H
EXTERNAL REFRESH		x	x	x	H	H	x	L

H = High, L= Low, x = Irrelevant, ↑ = low-to-high transition

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

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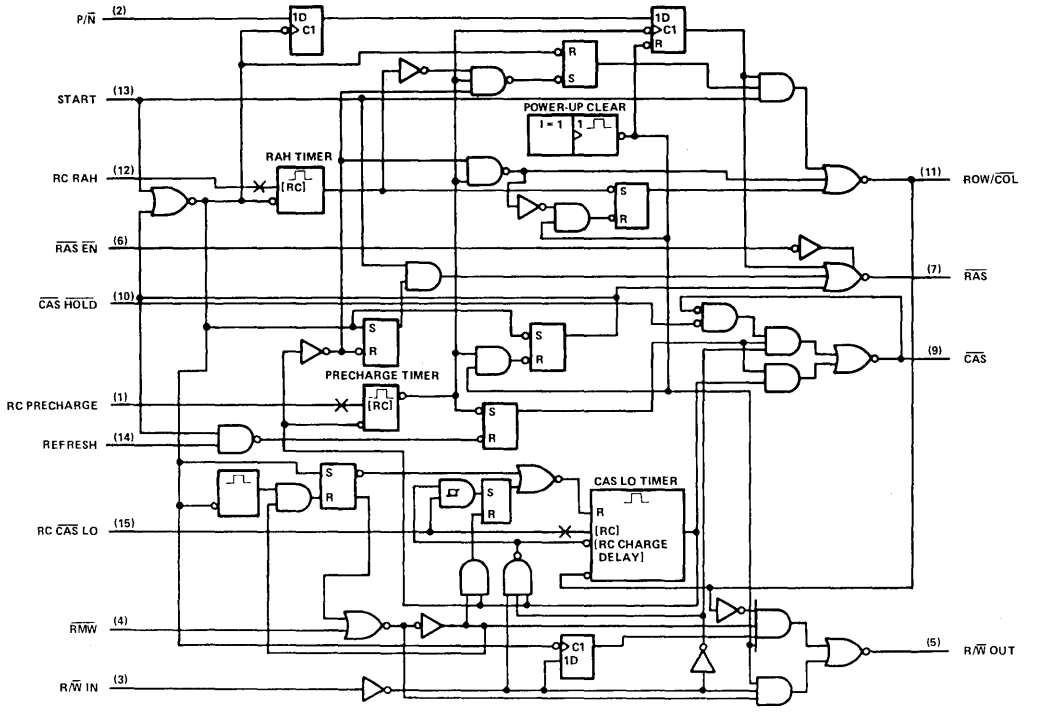
PIN FUNCTION TABLE

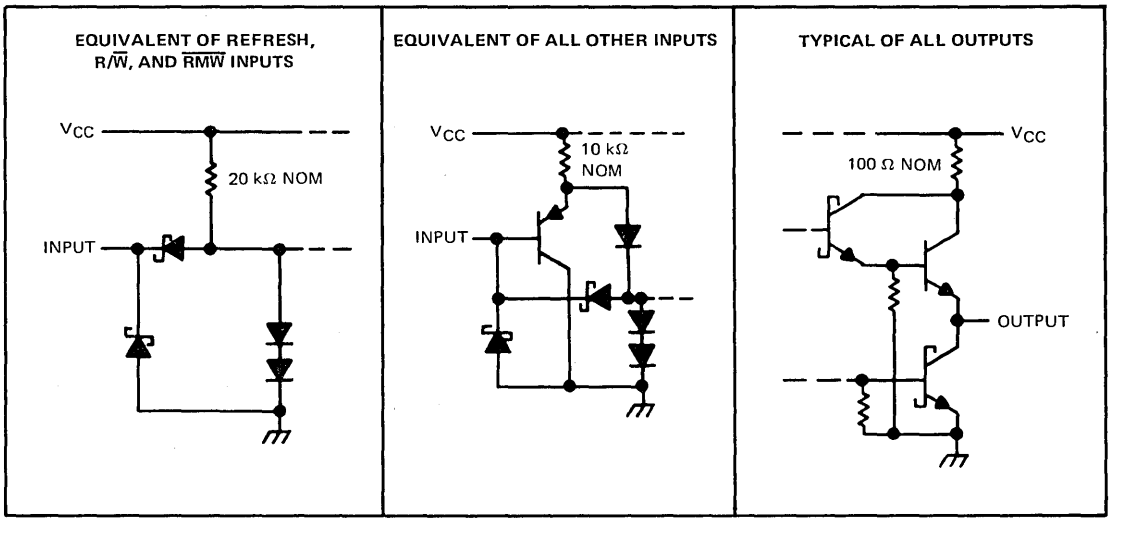
PIN	PIN NAME	FUNCTIONAL DESCRIPTION
1	RC PRECHARGE	User-programmable timing node* for precharge ($\overline{CAS}$ high and $\overline{RAS}$ high).
2	P/$\overline{N}$ IN	When high, initiates a ready cycle (holds R/W OUT high) and, when low, page mode read or write cycle holds $\overline{RAS}$ continuously low while $\overline{CAS}$ and column addresses are sequenced.
3	R/$\overline{W}$ IN	When high, initiates a ready cycle (holds R/$\overline{W}$ OUT high) and, when low, initiates a write cycle (holds R/$\overline{W}$ OUT low) if pin 4 is high and pin 14 is low.
4	$\overline{RMW}$ IN	When low, enables read-modify-write cycle. R/$\overline{W}$ IN must be high at the start of the RMW cycle.
5	R/$\overline{W}$ OUT	When high, indicates a read cycle is in progress. When low, indicates a write cycle is in progress. Normally ties to a $\overline{W}$ memory input in a system.
6	$\overline{RAS}$ $\overline{ENABLE}$ IN	When low, enables $\overline{RAS}$ output. When high, $\overline{RAS}$ is in the high-impedance or third state.
7	$\overline{RAS}$ OUT	3-state row-address-strobe output controlled by $\overline{RAS}$ $\overline{ENABLE}$ IN. In the three-chip controller set, the $\overline{RAS}$ output of the 'LS608 ties to the $\overline{RAS}$ output of the refresh controller ('LS600 thru 'LS603).
8	GND	Device and substrate ground.
9	$\overline{CAS}$ OUT	Column-address-strobe output.
10	$\overline{CAS}$ $\overline{HOLD}$ IN	When low, allows $\overline{CAS}$ to latch in low state. When high, latch is removed. Can be used to improve data retrieval during read cycle.
11	ROW/$\overline{COL}$ (or $\overline{MEMBSY}$) OUT	In a system where the 'LS608 is a stand-alone controller, this output indicates a memory-busy condition to the microprocessor. When the 'LS608 is used as a part of a three-chip controller set, this pin ties to the SELECT A/$\overline{B}$ input of the multiplexer ('LS604 thru 'LS607) for selecting row and column in addition to indicating a memory-busy condition to the microprocessor.
12	RC RAH	User-programmable timing node* for row address hold time. (high level at ROW/$\overline{COL}$ OUT).
13	START IN	When changed from low to high, initiates a memory cycle.
14	REFRESH IN	When high, enables $\overline{RAS}$-only refresh cycle.
15	RC $\overline{CAS}$ LO	User-programmable timing node* for column-address-strobe low time.
16	V_{CC}	5-volt power supply terminal.

*All timing nodes require a resistor to V_{CC} and a capacitor to ground. Programmed time is approximately 0.29 RC.

functional block diagram (positive logic)



schematics of inputs and outputs



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54LS608 . . . . . −55°C to 125°C
SN74LS608 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

		SN54LS608			SN74LS608			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	ROW/$\overline{\text{COL}}$			−0.4			−0.4	mA
	$\overline{\text{RAS}}$			−1			−2.6	
	All others			−1.2			−1.2	
Low-level output current, I_{OL}	ROW/$\overline{\text{COL}}$			4			8	mA
	All others			12			24	
Setup time, t_{su}	R/$\overline{\text{W}}$, $\overline{\text{RMW}}$, P/$\overline{\text{N}}$, or REFRESH to START↑	20			20			ns
	$\overline{\text{CAS}}$ $\overline{\text{HOLD}}$ to $\overline{\text{CAS}}$↓	20			20			
Hold time, t_h		0			0			ns
External timing resistor, R_{ext}	RC RAH	0.1		2	0.1		2	kΩ
	RC $\overline{\text{CAS}}$ LO, RC PRECHARGE	1		6	1		6	
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS608			SN74LS608			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	ROW/$\overline{\text{COL}}$	V_{CC} = MIN,	I_{OH} = −400 μA	2.5	3.4		2.7	3.4		V
		$\overline{\text{RAS}}$	V_{IH} = 2 V,	I_{OH} = MAX	2.4	3.2		2.4	3.1		
		Others	V_{IL} = V_{IL} max	I_{OH} = −1.2 mA	2.4	3.2		2.4	3.2		
V_{OL}	Low-level output voltage	ROW/$\overline{\text{COL}}$	V_{CC} = MIN,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			V_{IH} = 2 V,	I_{OL} = 8 mA					0.35	0.5	
		Others	V_{IL} = V_{IL} max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	
				I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	$\overline{\text{RAS}}$	V_{CC} = MAX, V_{IL} = V_{IL} max,	V_{IH} = 2 V, V_O = 2.7 V			20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied	$\overline{\text{RAS}}$	V_{CC} = MAX, V_{IL} = V_{IL} max,	V_{IH} = 2 V, V_O = 0.4 V			−20			−20	μA
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current	REFRESH, R/$\overline{\text{W}}$, $\overline{\text{RMW}}$	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
		Others					−0.2			−0.2	
I_{OS}	Short-circuit output current§	ROW/$\overline{\text{COL}}$	V_{CC} = MAX,	V_O = 0 V	−20		−100	−20		−100	mA
		Others			−30		−130	−30		−130	
I_{CC}	Supply current		V_{CC} = MAX, All inputs at GND	Outputs open,		45			45		mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, C_L = 45 pF to GND (see waveforms for more detail)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MODE	MIN	TYP	MAX	UNIT
t_{PHL}	START ↑	$\overline{RAS}$	R_L = 667 Ω to V_{CC}	NORMAL READ		12		ns
t_{PLH}†	START ↑	$\overline{RAS}$				425		ns
t_{PHL}‡	START ↑	$\overline{CAS}$				140		ns
t_{PLH}†	START ↑	$\overline{CAS}$				405		ns
t_{PHL}‡	START ↑	R/$\overline{W}$		NORMAL WRITE		115		ns
t_{PLH}†	START ↑	R/$\overline{W}$				440		ns
t_{PLH}	$\overline{CAS}$ HOLD ↑	$\overline{CAS}$		NORMAL READ		10		ns
t_{PHL}‡	START ↑	ROW/$\overline{COL}$	R_L = 2 kΩ to V_{CC}			125		ns
t_{PLH}§	START ↑	ROW/$\overline{COL}$				670		ns
t_{PHL}	R/$\overline{W}$ ↓	R/$\overline{W}$	R_L = 667 Ω to V_{CC}	NORMAL RMW		14		ns
t_{PLH}¶	R/$\overline{W}$ ↓	R/$\overline{W}$				355		ns
t_{PLH}	$\overline{RMW}$ ↑	$\overline{CAS}$				40		ns
t_{PLH}♦	$\overline{RMW}$ ↑	ROW/$\overline{COL}$				320		ns
t_{PZH}	$\overline{RAS}$ EN ↓	$\overline{RAS}$	R_L = 667 Ω to GND	NORMAL READ		15		ns
t_{PZL}	$\overline{RAS}$ EN ↓	$\overline{RAS}$	R_L = 667 Ω to V_{CC}			17		ns
t_{PHZ}	$\overline{RAS}$ EN ↑	$\overline{RAS}$	R_L = 667 Ω to GND			10		ns
t_{PLZ}	$\overline{RAS}$ EN ↑	$\overline{RAS}$	R_L = 667 Ω to V_{CC}			17		ns

† Depends on RC network at pin 12 (2 kΩ, 180 pF used for testing) and the RC network at pin 15 (5 kΩ, 180 pF).

‡ Depends on RC network at pin 12 (2 kΩ, 180 pF).

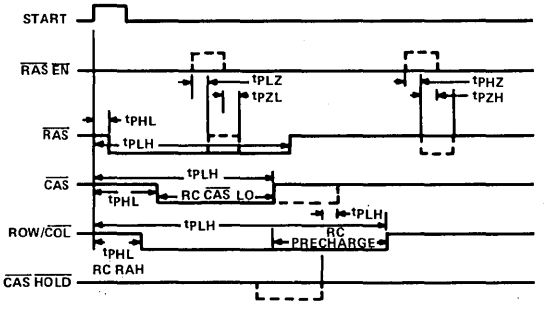
§ Depends on RC networks at pin 12 (2 kΩ, 180 pF), pin 15 (5 kΩ, 180 pF), and pin 1 (5 kΩ, 180 pF).

¶ Depends on RC network at pin 15 (5 kΩ, 180 pF).

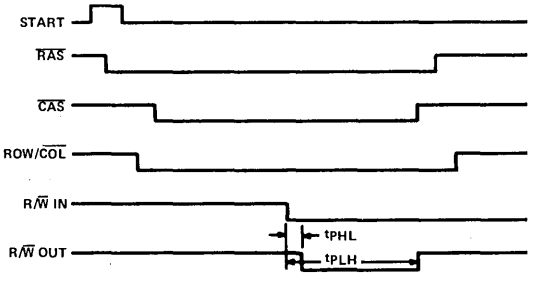
♦ Depends on RC network at pin 1 (5 kΩ, 180 pF).

NOTE 2: Measurement point for all t_{PHZ} output pulses is 2.9 V. Measurement point for all t_{PLZ} output pulses is 0.8 V. All other measurement points are 1.3 V.

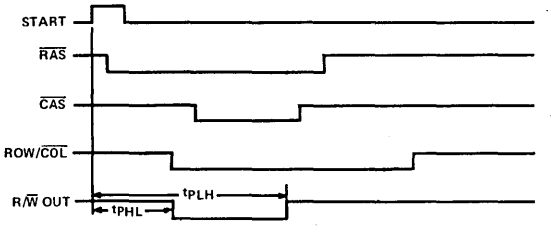
PARAMETER MEASUREMENT INFORMATION



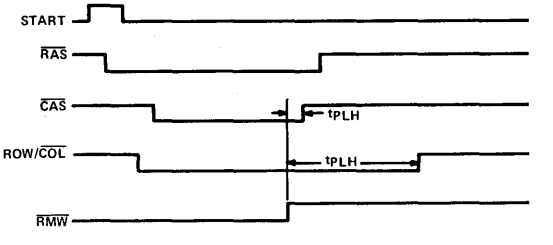
NORMAL READ MODE (R/$\overline{W}$ IN = H)



NORMAL READ-MODIFY-WRITE MODE ($\overline{RMW}$ = L)



NORMAL WRITE MODE (R/$\overline{W}$ IN = L)



NORMAL READ-MODIFY-WRITE ABORT AFTER READ (R/$\overline{W}$ = H)

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TYPES SN54LS610 THRU SN54LS613, SN74LS610 THRU SN74LS613 MEMORY MAPPERS

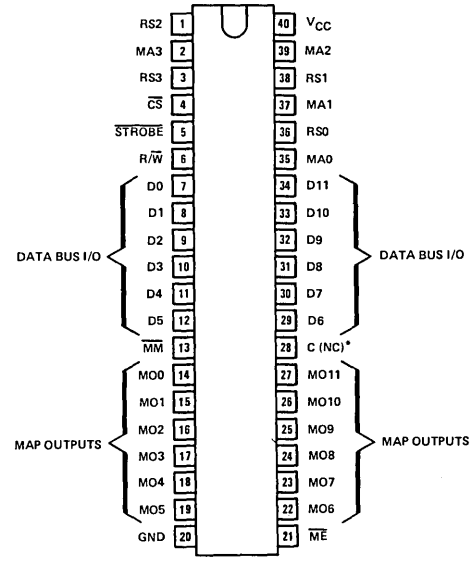
D2549, JANUARY 1981

(TIM99610 THRU TIM99613)

- Expands 4 Address Lines to 12 Address Lines
- Designed for Paged Memory Mapping
- Output Latches Provided on 'LS610 and 'LS611
- Choice of 3-State or Open-Collector Map Outputs
- Compatible with TMS 9900 and Other Microprocessors

DEVICE	OUTPUTS LATCHED	MAP OUTPUT TYPE
'LS610	Yes	3-State
'LS611	Yes	Open-Collector
'LS612	No	3-State
'LS613	No	Open-Collector

SN54LS' . . . J PACKAGE
SN74LS' . . . J OR N PACKAGE
(TOP VIEW)



*NOTE: Pin 28 has no internal connection on 'LS612 and 'LS613

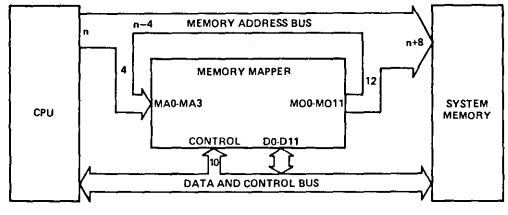
description

These memory-mapper integrated circuits contain a 4-line to 16-line decoder, a 16-word by 12-bit RAM, 16 channels of 2-line to 1-line multiplexers, and other miscellaneous circuitry on a monolithic chip. The 'LS610 and 'LS611 also contain 12 latches with an enable control.

The memory mappers are designed to expand a microprocessor's memory address capability by eight bits. Four bits of the memory address bus (see the figure below) can be used to select one of 16 map registers that contain 12 bits each. These 12 bits are presented to the system memory address bus through the map output buffers along with the unused memory address bits from the CPU. However, addressable memory space without reloading the map registers is the same as would be available with the memory mapper left out. The addressable memory space is increased only by periodically reloading the map registers from the data bus.

This configuration lends itself to memory utilization of 16 pages of $2^{(n-4)}$ registers each without reloading (n = number of address bits available from CPU).

These devices have four modes of operation (read, write, map, and pass). Data may be read from or loaded into the map register selected by the register select inputs (RS0 thru RS3) under control of R/$\overline{W}$ whenever chip select ($\overline{CS}$) is low. The data I/O takes place on the data bus D0 thru D7. The map operation will output the contents of the map register selected by the map address inputs (MA0 thru MA3) when $\overline{CS}$ is high and $\overline{MM}$ (map mode control) is low. The 'LS612 and 'LS613 output stages are transparent in this mode, while the 'LS610 and 'LS611 outputs may be transparent or latched. When $\overline{CS}$ and $\overline{MM}$ are both high (pass mode), the address bits on MA0 thru MA3 appear at MO8–MO11, respectively, (assuming appropriate latch control) with low levels in the other bit positions of the map outputs.



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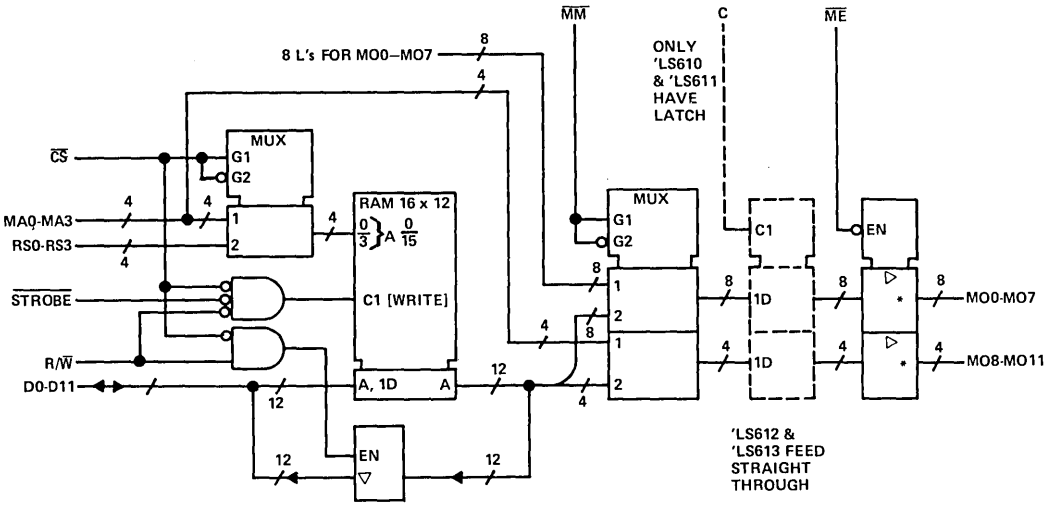
functional block diagram (positive logic)



*'LS610 and 'LS612 have 3-state (▽) map outputs.
'LS611 and 'LS613 have open-collector (◇) map outputs.

PIN FUNCTION TABLE

PIN	PIN NAME	FUNCTIONAL DESCRIPTION
7–12, 29–34	D0 thru D11	I/O connections to data and control bus used for reading from and writing to the map register selected by RS0–RS3 when $\overline{CS}$ is low. Mode controlled by R/$\overline{W}$.
36, 38, 1, 3	RS0 thru RS3	Register select inputs for I/O operations.
6	R/$\overline{W}$	Read or write control used in I/O operations to select the condition of the data bus. When high, the data bus outputs are active for reading the map register. When low, the data bus is used to write into the register.
5	$\overline{STROBE}$	Strobe input used to enter data into the selected map register during I/O operations.
4	$\overline{CS}$	Chip select input. A low input level selects the memory mapper (assuming more than one used) for an I/O operation.
35, 37, 39, 2	MA0 thru MA3	Map address inputs to select one of 16 map registers when in map mode ($\overline{MM}$ low and $\overline{CS}$ high).
14–19, 22–27	MO0 thru MO11	Map outputs. Present the map register contents to the system memory address bus in the map mode. In the pass mode, these outputs provide the map address data on MO8–MO11 and low levels on MO0–MO7.
13	$\overline{MM}$	Map mode input. When low, 12 bits of data are transferred from the selected map register to the map outputs. When high (pass mode), the 4 bits present on the map address inputs MA0-MA3 are passed to the map outputs MO8-MO11, respectively, while MO0-MO7 are set low.
21	$\overline{ME}$	Map enable for the map outputs. A low level allows the outputs to be active while a high input level puts the outputs at high impedance.
28	C	Latch enable input for the 'LS610 and 'LS611 (no internal connection for 'LS612 and 'LS613). A high level will transparently pass data to the map outputs. A low level will latch the outputs.
40, 20	V_{CC}, GND	5-V power supply and network ground (substrate) pins.

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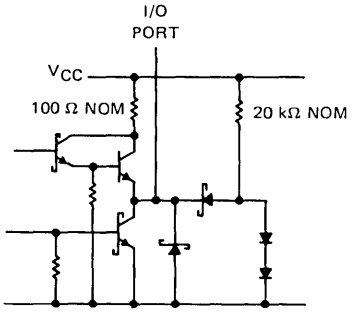
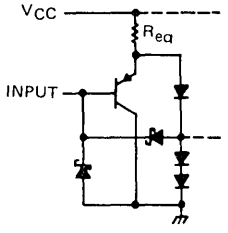
schematics of inputs and outputs

INPUT/OUTPUT PORTS, D0-D11

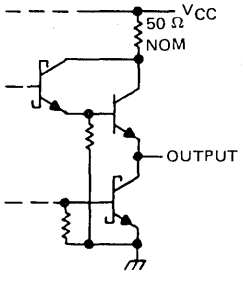


EQUIVALENT OF OTHER INPUTS

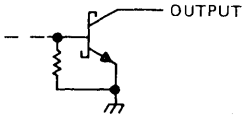


$\overline{MM}$: R_{eq} = 7 kΩ NOM
RS, $\overline{STROBE}$: R_{eq} = 9 kΩ NOM
$\overline{CS}$, R/$\overline{W}$, MA: R_{eq} = 6 kΩ nom

TYPICAL OF MAP OUTPUTS ('LS610, 'LS612)



TYPICAL OF MAP OUTPUTS ('LS611, 'LS613)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)		7 V
Input voltage:	Data Bus I/O	5.5 V
	All other inputs	7 V
Operating free-air temperature range:	SN54LS610 through SN54LS613	−55°C to 125°C
	SN74LS610 through SN74LS613	0°C to 70°C
Storage temperature range		−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS610 SN54LS612			SN74LS610 SN74LS612			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	MO			−12			−15	mA
	D			−1			−2.6	
Low-level output current, I_{OL}	MO			12			24	mA
	D			4			8	
Width of strobe input pulse, t_{SLSH}	See Figure 1	75			75			ns
$\overline{CS}$ setup time ($\overline{CS}$ low to strobe low), t_{CSLSL}		20			20			ns
R/$\overline{W}$ setup time (R/$\overline{W}$ low to strobe low), t_{WLSL}		20			20			ns
RS setup time (RS valid to strobe low), t_{RVSL}		20			20			ns
Data setup time (D0-D11 valid to strobe high), t_{DVSH}		75			75			ns
$\overline{CS}$ hold time (Strobe high to $\overline{CS}$ high), t_{SHCSH}		20			20			ns
R/$\overline{W}$ hold time (Strobe high to R/$\overline{W}$ high), t_{SHWH}		20			20			ns
RS hold time (Strobe high to RS invalid), t_{SHRX}		20			20			ns
Data hold time (Strobe high to D0-D11 invalid), t_{SHDX}		20			20			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS610 SN54LS612			SN74LS610 SN74LS612			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input calmp voltage		V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	MO	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OH} = −3 mA	2.4			2.4			V
				I_{OH} = MAX	2			2			
		D		I_{OH} = MAX	2.4			2.4			
V_{OL}	Low-level output voltage	MO	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
		D		I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
				I_{OL} = 8 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied		V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = V_{IL} max, V_O = 2.7 V				20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied	MO	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = V_{IL} max, V_O = 0.4 V				−20			−20	μA
		D					−400			−400	
I_I	Input current at maximum input voltage	D	V_{CC} = MAX	V_I = 5.5 V			100			100	μA
		All others		V_I = 7 V			100			100	
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	MO	V_{CC} = MAX		−40		−225	−40		−225	mA
		D			−30		−130	−30		−130	
I_{CC}	Supply current		V_{CC} = MAX	Outputs high		112	180		112	180	mA
				Outputs low		112	180		112	180	
				Outputs at high impedance		150	230		180	230	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Note more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

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switching characteristics, V_{CC} = 5 V, T_A = 25°C, C_L = 45 pF to GND

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS610			'LS612			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
t_{CSLDV}	Access (enable) time	$\overline{CS}$↓	D 0-11	R_L = 2 kΩ, See Figure 1, See Note 2		28	50		26	50	ns
t_{WHDV}	Access (enable) time	R/$\overline{W}$↑	D 0-11			20	35		20	35	ns
t_{RVDV}	Access time	RS	D 0-11			49	75		39	75	ns
t_{WLDZ}	Disable time	R/$\overline{W}$↓	D 0-11			32	50		30	50	ns
t_{CSHDZ}	Disable time	$\overline{CS}$↑	D 0-11			42	65		38	65	ns
t_{ELQV}	Access (enable) time	$\overline{ME}$↓	MO 0-11	R_L = 667 Ω, See Figure 2, See Note 2		19	30		17	30	ns
t_{CSHQV}	Access time	$\overline{CS}$↑	MO 0-11			56	85		48	85	ns
t_{MLQV}	Access time	$\overline{MM}$↓	MO 0-11			25	40		22	40	ns
t_{CHQV}	Access time	C↑	MO 0-11			24	40				ns
t_{AVQV1}	Access time ($\overline{MM}$ low)	MA	MO 0-11			46	70		39	70	ns
t_{MHQV}	Access time	$\overline{MM}$↑	MO 0-11			24	40		22	40	ns
t_{AVQV2}	Propagation time ($\overline{MM}$ high)	MA	MO 8-11			19	30		13	30	ns
t_{EHQZ}	Disable time	$\overline{ME}$↑	MO 0-11			14	25		14	25	ns

NOTE 2 For load circuits and measurement points, see page 3-11 of *The TTL Data Book* for *Design Engineers*, second edition, LCC 4112. Access times are tested as t_{PLH} and t_{PHL} or t_{PZH} or t_{PZL}. Disable times are tested as t_{PHZ} and t_{PLZ}.

2

explanation of letter symbols

This data sheet uses a new type of letter symbol to describe time intervals. The format is:

$$t_{AB\text{-}CD}$$

where: subscripts A and C indicate the names of the signals for which changes of state or level or establishment of state or level constitute signal events assumed to occur first and last, respectively, that is, at the beginning and end of the time interval.

Subscripts B and D indicate the direction of the transitions and/or the final states or levels of the signals represented by A and C, respectively. One or two of the following is used:

H = high or transition to high
L = low or transition to low
V = a valid steady-state level
X = unknown, changing, or "don't care" level
Z = high-impedance (off) state.

The hyphen between the B and C subscripts is omitted when no confusion is likely to occur. For these letter symbols on this data sheet, the signal names are further abbreviated as follows:

SIGNAL NAME	B or D SUBSCRIPT
C	C
$\overline{CS}$	CS
D0–11	D
MA0–MA3	A
MO0–MO11	Q
$\overline{ME}$	E
$\overline{MM}$	M
R/$\overline{W}$	W
RS0–RS3	R
$\overline{STROBE}$	S

recommended operating conditions

		SN54LS611 SN54LS613			SN74LS611 SN74LS613			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}	MO			5.5			5.5	V
High-level output current, I_{OH}	D			−1			−2.6	mA
Low-level output current, I_{OL}	MO			12			24	mA
	D			4			8	
Width of strobe input pulse, t_{SLSH}	See Figure 1	75			75			ns
$\overline{CS}$ setup time ($\overline{CS}$ low to strobe low), t_{CSLSL}		20			20			ns
R/$\overline{W}$ setup time (R/$\overline{W}$ low to strobe low), t_{WLSL}		20			20			ns
RS setup time (RS valid to strobe low), t_{RVSL}		20			20			ns
Data setup time (D0-D11 valid to strobe high), t_{DVSH}		75			75			ns
$\overline{CS}$ hold time (Strobe high to $\overline{CS}$ high), t_{SHCSH}		20			20			ns
R/$\overline{W}$ hold time (Strobe high to R/$\overline{W}$ high), t_{SHWH}		20			20			ns
RS hold time (Strobe high to RS invalid), t_{SHRX}		20			20			ns
Data hold time (Strobe high to D0-D11 invalid), t_{SHDX}		20			20			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

NOTE 2: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS611 SN54LS613			SN74LS611 SN74LS613			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	D	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max, I_{OH} = MAX		2.4			2.4			
I_{OH}	High-level output current	MO	V_{CC} = MIN, V_{IH} = 2 V, V_{OH} = 5.5 V				100			100	µA
V_{OL}	Low-level output voltage	MO	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
		D		I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
				I_{OL} = 8 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	D	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = V_{IL} max, V_O = 2.7 V				20			20	µA
I_{OZL}	Off-state output current, low-level voltage applied	D	V_{CC} = MAX, V_{IH} = 2 V, V_O = 0.4 V				−400			−400	
I_I	Input current at maximum input voltage	D	V_{CC} = MAX	V_I = 5.5 V			100			100	
		All others		V_I = 7 V			100			100	
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7 V				20			20	
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	D	V_{CC} = MAX		−30		−130	−30		−130	mA
I_{CC}	Supply current		V_{CC} = MAX	Outputs high		100	170		100	170	mA
				Outputs low		100	170		100	170	
				Outputs at high impedance		110	200		110	200	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

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switching characteristics, V_{CC} = 5 V, T_A = 25°C, C_L = 45 pF to GND

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS611			'LS613			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
t_{CSLDV}	Access (enable) time	$\overline{CS}$↓	D 0-11			31	50		28	50	ns
t_{WHDV}	Access (enable) time	R/$\overline{W}$↑	D 0-11	R_L = 2 kΩ,		23	35		21	35	ns
t_{RVDV}	Access time	RS	D 0-11	See Figure 1,		51	75		47	75	ns
t_{WLDZ}	Disable time	R/$\overline{W}$↓	D 0-11	See Note 2		32	50		31	50	ns
t_{CSHDZ}	Disable time	$\overline{CS}$↑	D 0-11			41	65		40	65	ns
t_{ELQV}	Access (enable) time	$\overline{ME}$↓	MO 0-11			21	30		19	30	ns
t_{CSHQV}	Access time	$\overline{CS}$↑	MO 0-11			57	90		53	90	ns
t_{MLQV}	Access time	MM↓	MO 0-11	R_L = 667 Ω,		25	40		25	40	ns
t_{CHQV}	Access time	C↑	MO 0-11	See Figure 2,		30	45				ns
t_{AVQV1}	Access time ($\overline{MM}$ low)	MA	MO 0-11	See Note 2		47	70		44	70	ns
t_{MHQV}	Access time	MM↑	MO 0-11			31	50		31	50	ns
t_{AVQV2}	Propagation time ($\overline{MM}$ high)	MA	MO 8-11			21	30		20	30	ns
t_{EHQZ}	Disable time	$\overline{ME}$↑	MO 0-11			15	25		15	25	ns

NOTE 2 For load circuits and measurement points, see page 3-11 of *The TTL Data Book* for *Design Engineers,* second edition, LCC 4112. Access times are tested as t_{PLH} and t_{PHL} or t_{PZH} or t_{PZL}. Disable times are tested as t_{PHZ} and t_{PLZ}.

2

TIMING DIAGRAMS

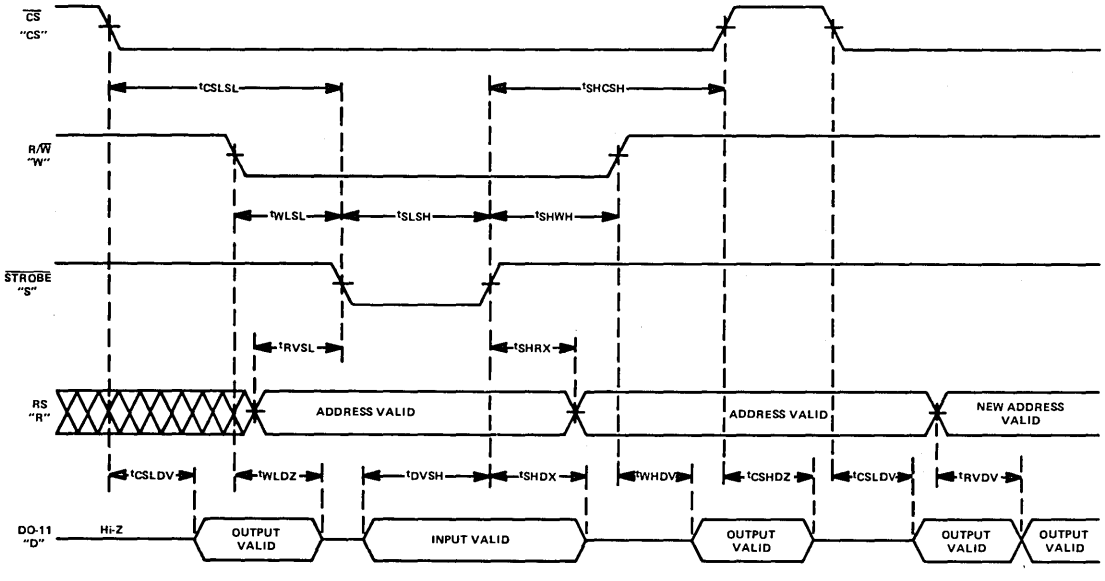

FIGURE 1–WRITE AND READ MODES

TIMING DIAGRAMS

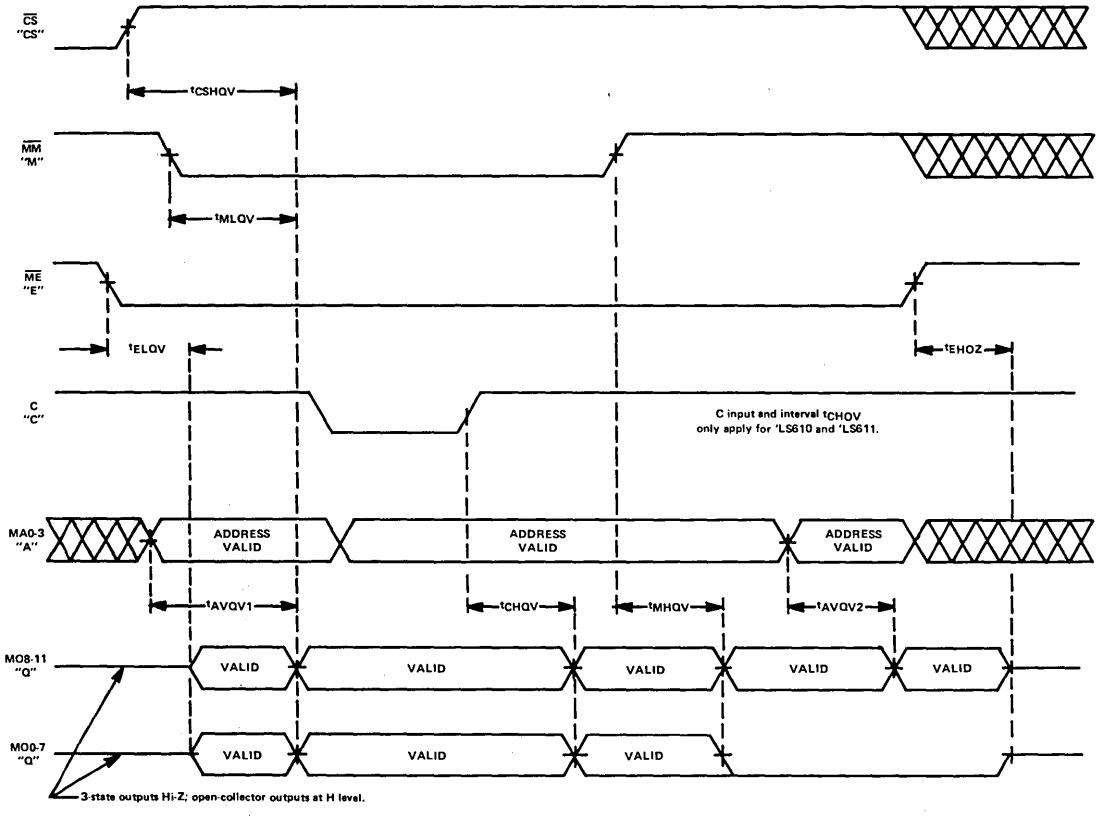

FIGURE 2–MAP AND PASS MODES

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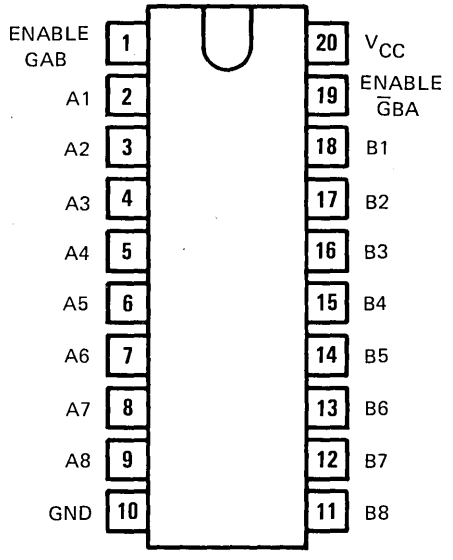
TYPES SN54LS620 THRU SN54LS623, SN74LS620 THRU SN74LS623 OCTAL BUS TRANSCEIVERS

D2537, AUGUST 1979

- Bidirectional Bus Transceivers in High-Density 20-Pin Packages
- Local Bus-Latch Capability
- Hysteresis at Bus Inputs Improves Noise Margins
- Choice of True or Inverting Logic
- Choice of 3-State or Open-Collector Outputs

DEVICE	OUTPUT	LOGIC
'LS620	3-State	Inverting
'LS621	Open-Collector	True
'LS622	Open-Collector	Inverting
'LS623	3-State	True

SN54LS' . . . J PACKAGE
SN74LS' . . . J OR N PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs ($\overline{G}$BA and GAB).

The enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives the 'LS620 thru 'LS623 the capability to store data by simultaneous enabling of $\overline{G}$BA and GAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states. The 8-bit codes appearing on the two sets of buses will be identical for the 'LS621 and 'LS623 devices or complementary for the 'LS620 and 'LS622.

FUNCTION TABLE

ENABLE INPUTS		OPERATION	
$\overline{G}$BA	GAB	'LS620, 'LS622	'LS621, 'LS623
L	L	$\overline{B}$ data to A bus	B data to A bus
H	H	$\overline{A}$ data to B bus	A data to B bus
H	L	Isolation	Isolation
L	H	$\overline{B}$ data to A bus, $\overline{A}$ data to B bus	B data to A bus, A data to B bus

H = high level, L = low level

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54LS' . . . . . −55°C to 125°C
SN74LS' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

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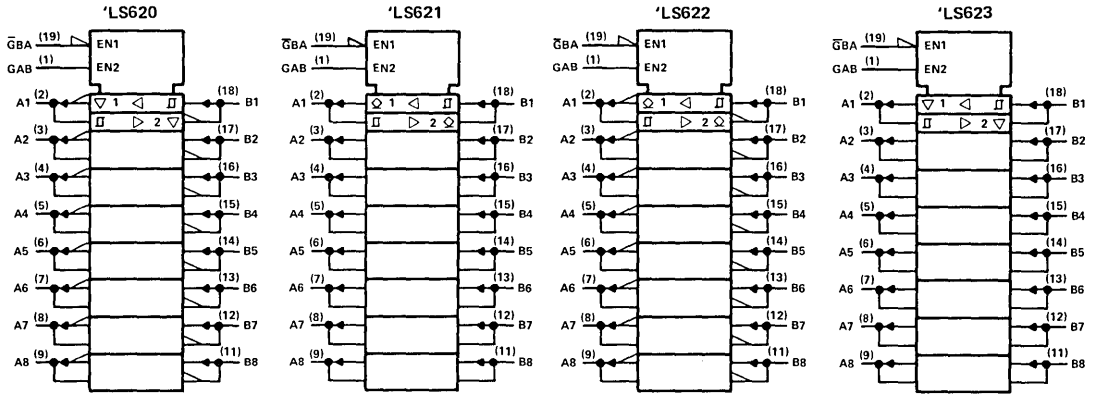
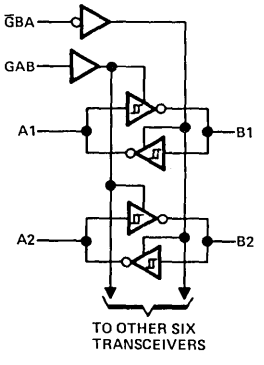
logic symbols

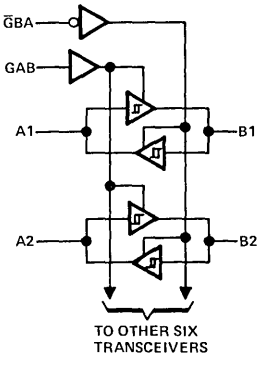


functional block diagrams (positive logic)

¼ 'LS620, ¼ 'LS622

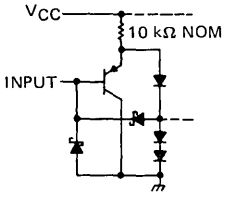


¼ 'LS621, ¼ 'LS623

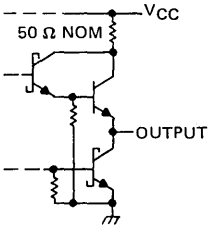


schematics of inputs and outputs

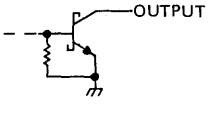
EQUIVALENT OF EACH INPUT



TYPICAL OF OUTPUTS OF 'LS620, 'LS623



TYPICAL OF OUTPUTS OF 'LS621, 'LS622



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recommended operating conditions

PARAMETER	SN54LS620 SN54LS623			SN74LS620 SN74LS623			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−12			−15	mA
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS620 SN54LS623			SN74LS620 SN74LS623			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.5			0.6	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
	Hysteresis ($V_{T+} - V_{T-}$) A or B input		V_{CC} = MIN		0.1	0.4		0.2	0.4		V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OH} = −3 mA	2.4	3.4		2.4	3.4		V
				I_{OH} = MAX	2			2			
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied		V_{CC} = MAX, V_O = 2.7 V	$\overline{G}$ at 2 V,			20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied		V_{CC} = MAX, V_O = 0.4 V	$\overline{G}$ at 2 V,			−400			−400	μA
I_I	Input current at maximum input voltage	A or B	V_{CC} = MAX,	V_I = 5.5 V			0.1			0.1	mA
		$\overline{G}$BA or GAB		V_I = 7 V			0.1			0.1	
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
I_{OS}	Short-circuit output current¶		V_{CC} = MAX		−40		−225	−40		−225	mA
I_{CC}	Total supply current	Outputs high	V_{CC} = MAX,	Outputs open		48	70		48	70	mA
		Outputs low				62	90		62	90	
		Outputs at Hi-Z				64	95		64	95	

†For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
¶Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics at V_{CC} = 5 V, T_A = 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS620			'LS623			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	A	B	C_L = 45 pF, R_L = 667 Ω, See Note 2		6	10		8	15	ns
		B	A			6	10		8	15	
t_{PHL}	Propagation delay time, high-to-low-level output	A	B			8	15		11	15	ns
		B	A			8	15		11	15	
t_{PZL}	Output enable time to low level	$\overline{G}$BA	A			31	40		31	40	ns
		GAB	B			31	40		31	40	
t_{PZH}	Output enable time to high level	$\overline{G}$BA	A			23	40		26	40	ns
		GAB	B			23	40		26	40	
t_{PLZ}	Output disable time from low level	$\overline{G}$BA	A	C_L = 5 pF, R_L = 667 Ω, See Note 2		15	25		15	25	ns
		GAB	B			15	25		15	25	
t_{PHZ}	Output disable time from high level	$\overline{G}$BA	A			15	25		15	25	ns
		GAB	B			15	25		15	25	

NOTE 2: For load circuit and voltage waveforms see page 3-11 of *"The TTL Data Book for Design Engineers"*, second edition.
t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
t_{PZH} ≡ Output enable time to high level
t_{PZL} ≡ Output enable time to low level
t_{PHZ} ≡ Output disable time from high level
t_{PLZ} ≡ Output disable time from low level

recommended operating conditions

PARAMETER	SN54LS621 SN54LS622			SN74LS621 SN74LS622			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS621 SN54LS622			SN74LS621 SN74LS622			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.5			0.6	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
	Hysteresis ($V_{T+} - V_{T-}$) A or B input		V_{CC} = MIN		0.1	0.4		0.2	0.4		V
I_{OH}	High-level output current		V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, V_{OH} = 5.5 V			100			100	μA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
I_{CC}	Total supply current	Outputs high	V_{CC} = MAX,	Outputs open		48	70		48	70	mA
		Outputs low				62	90		62	90	

†For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics at V_{CC} = 5 V, T_A = 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS621			'LS622			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	A	B	C_L = 45 pF, R_L = 667 Ω, See Note 2		17	25		19	25	ns
		B	A			17	25		19	25	
t_{PHL}	Propagation delay time, high-to-low-level output	A	B			16	25		14	25	ns
		B	A			16	25		14	25	
t_{PLH}	Output disable time from low level	$\overline{G}$BA	A			23	40		26	40	ns
		GAB	B			25	40		28	40	
t_{PHL}	Output disable time from high level	$\overline{G}$BA	A			34	50		43	60	ns
		GAB	B			37	50		39	60	

NOTE 2: Load circuit and voltage waveforms are shown on page 3-11 of *The TTL Data Book for Design Engineers*, Second Edition, LCC4112.
t_{PLH} ≡ Propagation delay time, low-to-high-level input.
t_{PHL} ≡ Propagation delay time, high-to-low-level input.

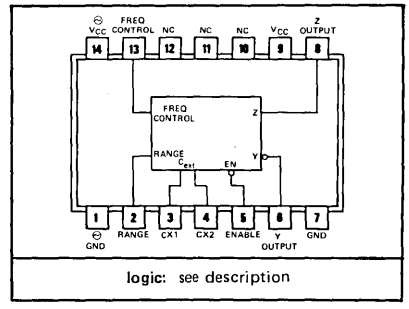
TYPES SN54LS624 THRU SN54LS629, SN74LS624 THRU SN74LS629 VOLTAGE-CONTROLLED OSCILLATORS

D2501, JANUARY 1980 – REVISED OCTOBER 1980

- Separate Supply Voltage Pins for Isolation of Frequency Control Inputs and Oscillators from Output Circuitry
- Highly Stable Operation over Specified Temperature and/or Supply Voltage Ranges

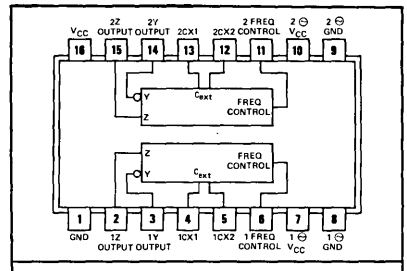
DEVICE TYPE	SIMILAR TO	NUMBER VCO's	COMP'L Z OUT	ENABLE	RANGE INPUT	R_{ext}
'LS624	'LS324	single	yes	yes	yes	no
'LS625	'LS325	dual	yes	no	no	no
'LS626	'LS326	dual	yes	yes	no	no
'LS627	'LS327	dual	no	no	no	no
'LS628	'LS324	single	yes	yes	yes	yes
'LS629	'LS124	dual	no	yes	yes	no

SN54LS'. . . J OR W PACKAGE
SN74LS'. . . J OR N PACKAGE
'LS624 (TOP VIEW)



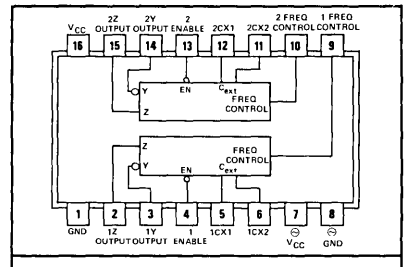
logic: see description

'LS625 (TOP VIEW)



logic: see description

'LS626 (TOP VIEW)



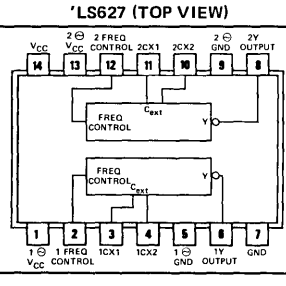
logic: see description

description

These voltage-controlled oscillators (VCO's) are improved versions of the original VCO family: SN54LS124, SN54LS324 thru SN54LS327, SN74LS124, and SN74LS324 thru SN74LS327. These new devices feature improved voltage-to-frequency linearity, range, and compensation. With the exception of the 'LS624 and 'LS628, all of these devices feature two independent VCO's in a single monolithic chip. The 'LS624, 'LS625, 'LS626 and 'LS628 have complementary Z outputs. The output frequency for each VCO is established by a single external component (either a capacitor or a crystal), in combination with voltage-sensitive inputs used for frequency control and frequency range. Each device has a voltage-sensitive input for frequency control; however, the 'LS624, 'LS628, and 'LS629 devices also have one for frequency range. (See Figures 1 thru 6).

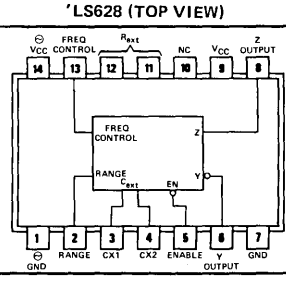
The 'LS628 features two $R_{external}$ pins that can offer more precise temperature compensation than its 'LS624 counterpart.

'LS627 (TOP VIEW)



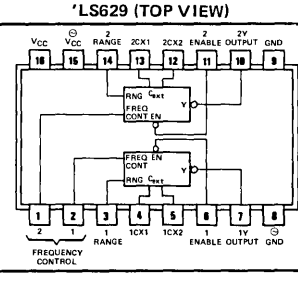
logic: see description

'LS628 (TOP VIEW)



logic: see description

'LS629 (TOP VIEW)



logic: see description

NC—No internal connection

Figure 3 and Figure 6 contain the necessary information to choose the proper capacitor value to obtain the desired operating frequency.

The devices can also be operated from a crystal by connecting a fundamental series resonant crystal across the C_{ext} pins. (Fundamental frequency ≤20 MHz.) The frequency control should be connected to 5 volts and, where applicable, the range control should also be connected to 5 volts.

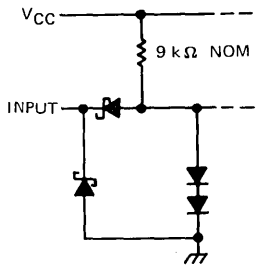
A single 5-volt supply can be used; however, one set of supply voltage and ground pins (V_{CC} and Gnd) is provided for the enable, synchronization-gating, and output sections, and a separate set ($\ominus V_{CC}$ and $\ominus$Gnd) is provided for the oscillator and associated frequency-control circuits so that effective isolation can be accomplished in the system. For operation of frequencies greater than 10 MHz, it is recommended that two independent supplies be used. Disabling either VCO of the 'LS625 and 'LS627 can be achieved by removing the appropriate $\ominus V_{CC}$. An enable input is provided on the 'LS624, 'LS626, 'LS628 and 'LS629. When the enable input is low the output is enabled: when the enable input is high, the internal oscillator is disabled, Y is high, and Z is low. Caution! Crosstalk may occur in the dual devices ('LS625, 'LS626, 'LS627, and 'LS629) when both VCO's are operated simultaneously.

The pulse-synchronization-gating section ensures that the first output pulse is neither clipped nor extended. The duty cycle of the square-wave output is fixed at approximately 50 percent.

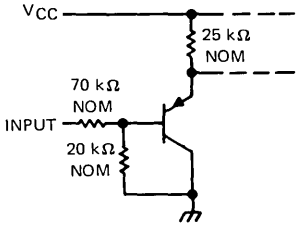
The SN54LS624 thru SN54LS629 are characterized for operation over the full military temperature range of −55°C to 125°C; the SN74LS624 thru SN74LS629 are characterized for operation from 0°C to 70°C.

schematics of inputs and outputs

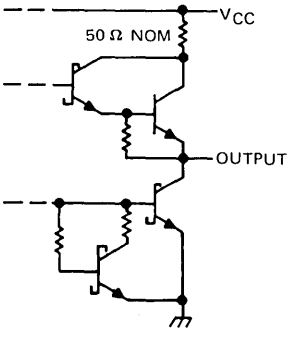
EQUIVALENT OF EACH ENABLE INPUT ('LS624, 'LS626, 'LS628, AND 'LS629)



EQUIVALENT OF EACH FREQUENCY CONTROL OR ('LS624, 'LS628, AND 'LS629) RANGE INPUT



TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Notes 1 and 2) . . . . . 7 V
Input voltage: Enable input♦ . . . . . 7 V
Frequency control or range input▲ . . . . . V_{CC}
Operating free-air temperature range: SN54LS' Circuits . . . . . −55°C to 125°C
SN74LS' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

♦The enable input is provided only on the 'LS624, 'LS626, 'LS628, and 'LS629.
▲The range input is provided only on 'LS624, 'LS628, and 'LS629.

NOTES: 1. Voltage values are with respect to the appropriate ground terminal.
2. Throughout this data sheet, the symbol V_{CC} is used for the voltage applied to both the V_{CC} and $\ominus V_{CC}$ terminals, unless otherwise noted.

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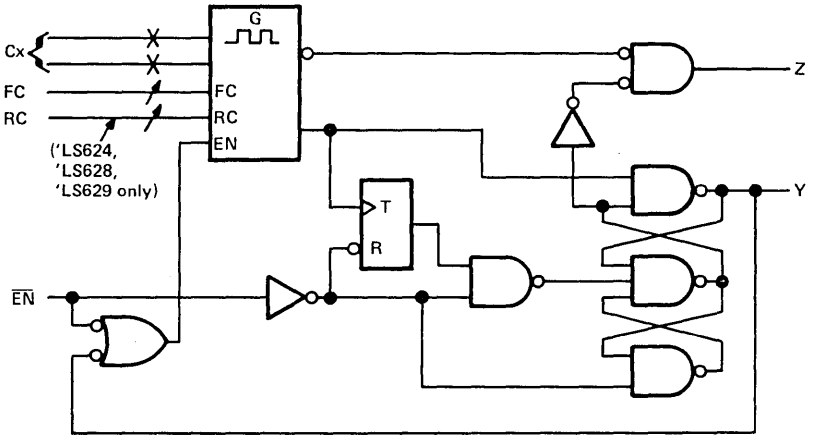
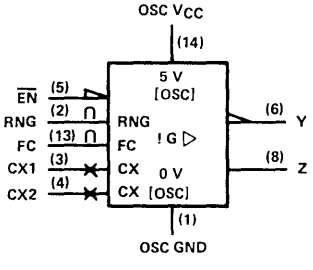
functional block diagram (positive logic)

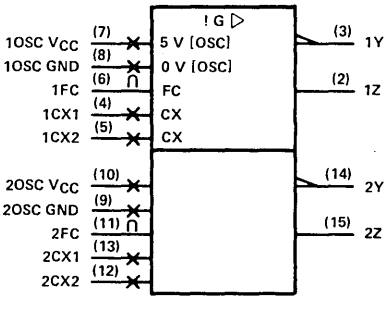


logic symbols¶

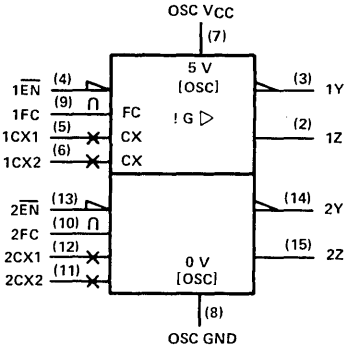
'LS624



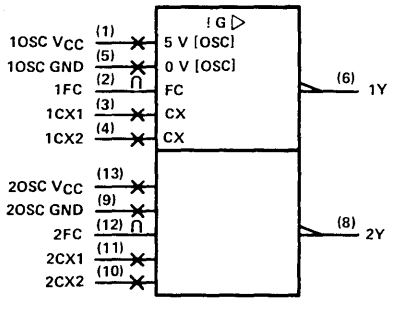
'LS625



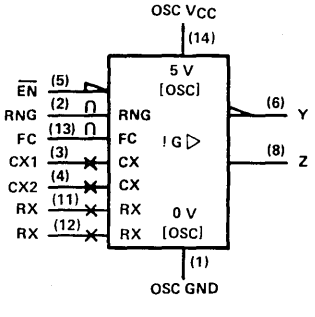
'LS626



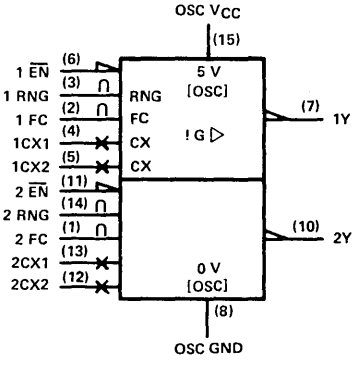
'LS627



'LS628



'LS629



recommended operating conditions

	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Input voltage at frequency control or range input, $V_{I(freq)}$ or $V_{I(rng)}$▲	0		5	0		5	V
High-level output current, I_{OH}			−1.2			−1.2	mA
Low-level output current, I_{OL}			12			24	mA
Output frequency, f_o	1			1			Hz
			20			20	MHz
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†			SN54LS'			SN74LS'			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage at enable◆					2			2			V
V_{IL}	Low-level input voltage at enable◆							0.7			0.8	V
V_{IK}	Input clamp voltage at enable◆		V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, I_{OH} = −1.2 mA,	$\overline{EN}$ at V_{IL} max, See Note 3		2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, $\overline{EN}$ at V_{IL} max,	See Note 3	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
					I_{OL} = 24 mA					0.35	0.5	
I_I	Input current	Freq control or range ▲	V_{CC} = MAX		V_I = 5 V		50	250		50	250	μA
					V_I = 1 V		10	50		10	50	
I_I	Input current at maximum input voltage	Enable◆	V_{CC} = MAX,	V_I = 7 V				0.2			0.2	mA
I_{IH}	High-level input current	Enable◆	V_{CC} = MAX,	V_I = 2.7 V				40			40	μA
I_{IL}	Low-level input current	Enable◆	V_{CC} = MAX,	V_I = 0.4 V				−0.8			−0.8	mA
I_{OS}	Short-circuit output current§		V_{CC} = MAX			−40		−225	−40		−225	mA
I_{CC}	Supply current, total into V_{CC} and ⊖ V_{CC} pins		V_{CC} = MAX, Enable◆ = 4.5 V See Note 4		'LS624		20	35		20	35	mA
					'LS625		35	55		35	55	
					'LS626		35	55		35	55	
					'LS627		35	55		35	55	
					'LS628		20	35		20	35	
					'LS629		35	55		35	55	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

▲ The range input is provided only on the 'LS624, 'LS628, and 'LS629.

◆ The enable input is provided only on the 'LS624, 'LS626, 'LS628, and 'LS629.

NOTES: 3. V_{OH} for Y outputs and V_{OL} for Z outputs are measured while enable inputs are connected to ground, with individual 1-kΩ resistors connected from CX1 to V_{CC} and from CX2 to ground. The resistor connections are reversed for testing V_{OH} for Z outputs and V_{OL} for Y inputs.

4. For 'LS624, 'LS626, 'LS628, and 'LS629, I_{CC} is measured with the outputs disabled and open. For 'LS625 and 'LS627, I_{CC} is measured with one ⊖ V_{CC} = MAX, and with the other ⊖ V_{CC} and outputs open.

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switching characteristics, V_{CC} = 5 V (unless otherwise noted), R_L = 667 Ω, C_L = 45 pF, T_A = 25 °C

PARAMETER		TEST CONDITIONS		'LS624, 'LS628, 'LS629			'LS625, 'LS626, 'LS627			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_O	Output frequency	C_{ext} = 50 pF	$V_{I(freq)}$ = 5 V, $V_{I(rng)}$ = 0 V	15	20	25				MHz
			$V_{I(freq)}$ = 0 V, $V_{I(rng)}$ = 5 V	0.7	1	1.3				
			$V_{I(freq)}$ = 5 V				7	9.5	12	
			$V_{I(freq)}$ = 0 V				0.9	1.2	1.5	

TYPICAL CHARACTERISTICS

'LS624, 'LS628, 'LS629
OUTPUT FREQUENCY
vs
FREQUENCY-CONTROL INPUT VOLTAGE

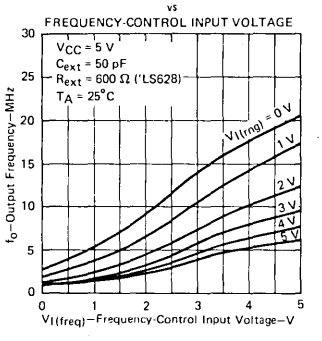


FIGURE 1

'LS624, 'LS628, 'LS629
OUTPUT FREQUENCY
vs
FREQUENCY-CONTROL INPUT VOLTAGE

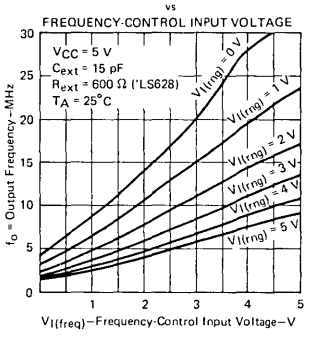


FIGURE 2

'LS624, 'LS628, 'LS629
OUTPUT FREQUENCY
vs
EXTERNAL CAPACITANCE

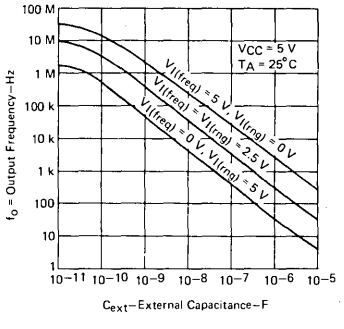


FIGURE 3

TYPICAL CHARACTERISTICS

'LS625, 'LS626, 'LS627
OUTPUT FREQUENCY
vs
FREQUENCY-CONTROL INPUT VOLTAGE

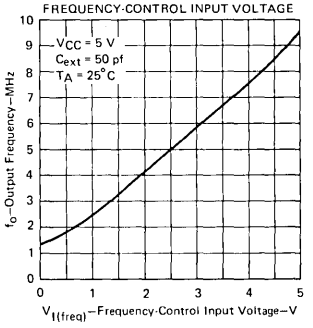


FIGURE 4

'LS625, 'LS626, 'LS627
OUTPUT FREQUENCY
vs
FREQUENCY-CONTROL INPUT VOLTAGE

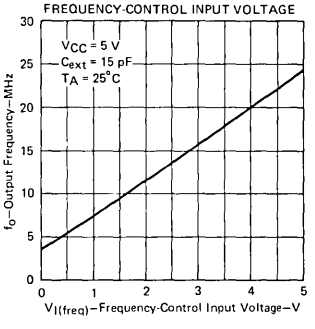


FIGURE 5

'LS625, 'LS626, 'LS627
OUTPUT FREQUENCY
vs
EXTERNAL CAPACITANCE

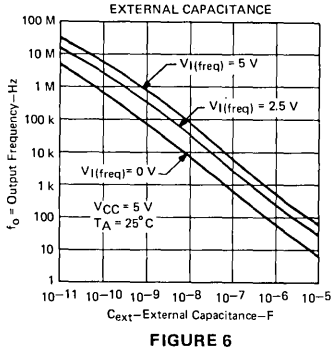


FIGURE 6

ENABLE TIME
vs
FREQUENCY

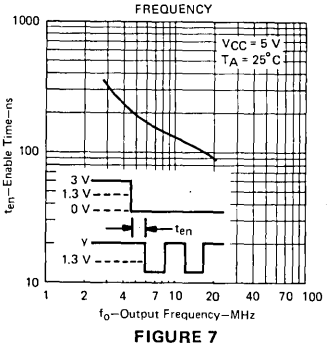
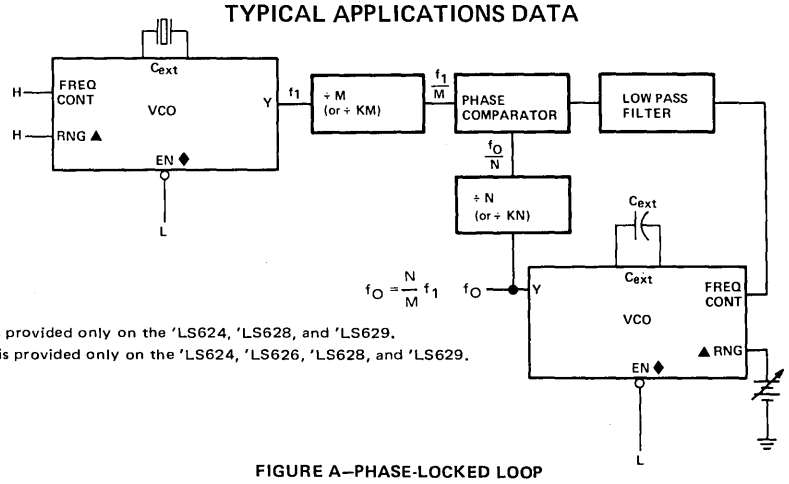


FIGURE 7

TYPICAL APPLICATIONS DATA



▲The range input is provided only on the 'LS624, 'LS628, and 'LS629.
♦The enable input is provided only on the 'LS624, 'LS626, 'LS628, and 'LS629.

FIGURE A—PHASE-LOCKED LOOP

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INCORPORATED
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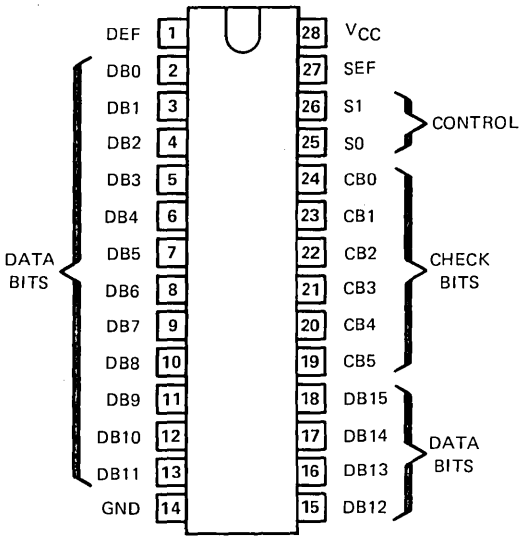
TYPES SN54LS630,SN54LS631,SN74LS630,SN74LS631
16-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

D2550, MARCH 1980

(TIM99630, TIM99631)

- Detects and Corrects Single-Bit Errors
- Detects and Flags Dual-Bit Errors
- Fast Processing Times:
  - Write Cycle: Generates Check Word in 45 ns Typical
  - Read Cycle: Flags Errors in 27 ns Typical
- Power Dissipation 600 mW Typical
- Choice of Output Configurations:
  - 'LS630 . . . 3-State
  - 'LS631 . . . Open-Collector

SN54LS' . . . J PACKAGE
SN74LS' . . . N PACKAGE
(TOP VIEW)



description

The 'LS630 and 'LS631 devices are 16-bit parallel error detection and correction circuits (EDACs) in 28-pin, 600-mil packages. They use a modified Hamming code to generate a 6-bit check word from a 16-bit data word. This check word is stored along with the data word during the memory write cycle. During the memory read cycle, the 22-bit words from memory are processed by the EDACs to determine if errors have occurred in memory.

Single-bit errors in the 16-bit data word are flagged and corrected.

Single-bit errors in the 6-bit check word are flagged, and the CPU sends the EDAC through the correction cycle even though the 16-bit word is not in error. The correction cycle will simply pass along the original 16-bit word in this case and produce error syndrome bits to pinpoint the error-generating location.

Dual-bit errors are flagged but not corrected. These dual errors may occur in any two bits of the 22-bit word from memory (two errors in the 16-bit data word, two errors in the 6-bit check word, or one error in each word).

The gross-error condition of all lows or all highs from memory will be detected. Otherwise, errors in three or more bits of the 22-bit word are beyond the capabilities of these devices to detect.

CONTROL FUNCTION TABLE

Memory Cycle	Control S1	Control S0	EDAC Function	Data I/O	Check Word I/O	Error Flags SEF	Error Flags DEF
WRITE	L	L	Generate Check Word	Input Data	Output Check Word	L	L
READ	L	H	Read Data & Check Word	Input Data	Input Check Word	L	L
READ	H	H	Latch & Flag Errors	Latch Data	Latch Check Word	Enabled	
READ	H	L	Correct Data Word & Generate Syndrome Bits	Output Corrected Data	Output Syndrome Bits	Enabled	

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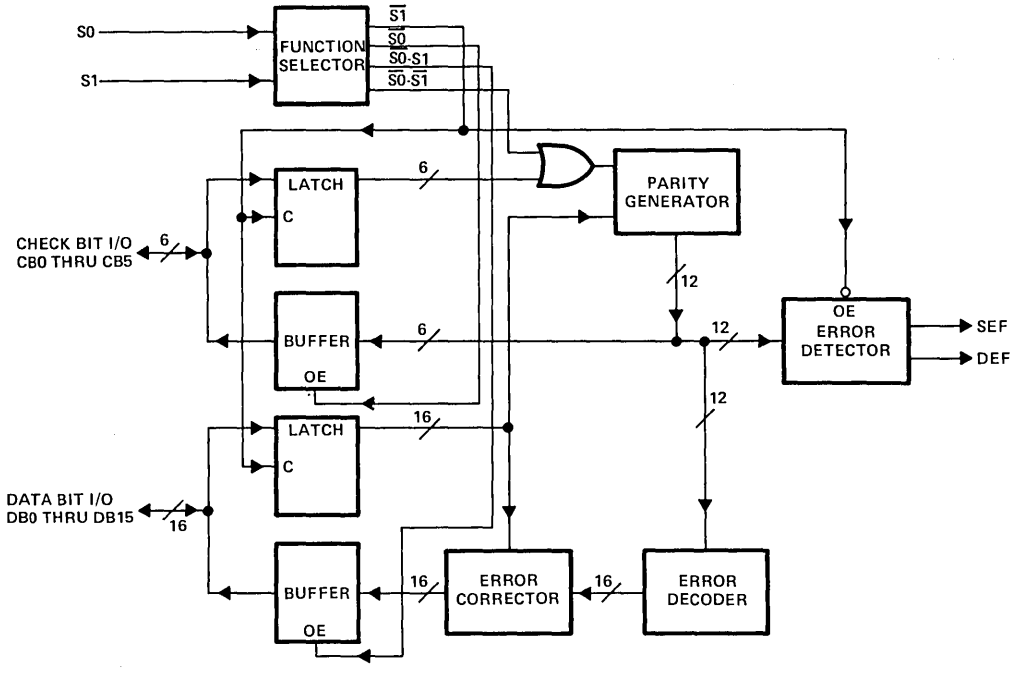
functional block diagram



ERROR FUNCTION TABLE

Total Number of Errors		Error Flags		Data Correction
16-Bit Data	6-Bit Checkword	SEF	DEF	
0	0	L	L	Not Applicable
1	0	H	L	Correction
0	1	H	L	Correction
1	1	H	H	Interrupt
2	0	H	H	Interrupt
0	2	H	H	Interrupt

In order to be able to determine whether the data from the memory is acceptable to use as presented to the bus, the EDAC must be strobed to enable the error flags and the flags will have to be tested for the zero condition.

The first case in the error function table represents the normal, no-error condition. The CPU sees lows on both flags. The next two cases of single-bit errors require data correction. Although the EDAC can discern the single check bit error and ignore it, the error flags are identical to the single error in the 16-bit data word. The CPU will ask for data correction in both cases. An interrupt condition to the CPU results in each of the last three cases, where dual errors occur.

error detection and correction details

During a memory write cycle, six check bits (CB0-CB5) are generated by eight-input parity generators using the data bits as defined below. During a memory read cycle, the 6-bit check word is retrieved along with the actual data.

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CHECKWORD	16-BIT DATA WORD															
BIT	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CB0	x	x		x	x				x	x	x			x		
CB1	x		x	x		x	x		x			x			x	
CB2		x	x		x	x		x		x			x			x
CB3	x	x	x				x	x			x	x	x			
CB4				x	x	x	x	x						x	x	x
CB5									x	x	x	x	x	x	x	x

The six check bits are parity bits derived from the matrix of data bits as indicated by "x" for each bit.

Error detection is accomplished as the 6-bit check word and the 16-bit data word from memory are applied to internal parity generators/checkers. If the parity of all six groupings of data and check bits are correct, it is assumed that no error has occurred and both error flags will be low. (It should be noted that the sense of two of the check bits, bits CB0 and CB1, is inverted to ensure that the gross-error condition of all lows and all highs is detected.)

If the parity of one or more of the check groups is incorrect, an error has occurred and the proper error flag or flags will be set high. Any single error in the 16-bit data word will change the sense of exactly three bits of the 6-bit check word. Any single error in the 6-bit check word changes the sense of only that one bit. In either case, the single error flag will be set high while the dual error flag will remain low.

Any two-bit error will change the sense of an even number of check bits. The two-bit error is not correctable since the parity tree can only identify single-bit errors. Both error flags are set high when any two-bit error is detected.

Three or more simultaneous bit errors can fool the EDAC into believing that no error, a correctable error, or an uncorrectable error has occurred and produce erroneous results in all three cases.

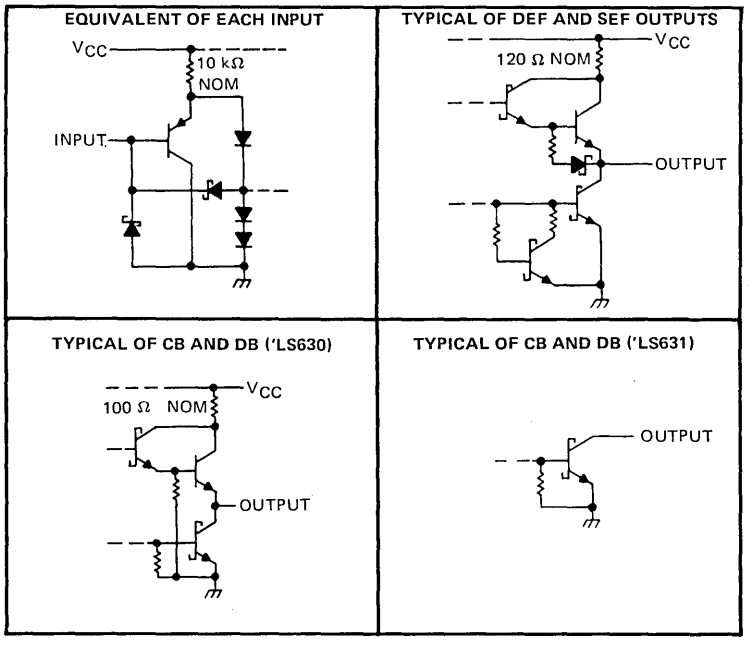
Error correction is accomplished by identifying the bad bit and inverting it. Identification of the erroneous bit is achieved by comparing the 16-bit data word and 6-bit check word from memory with the new check word with one (check word error) or three (data word error) inverted bits.

As the corrected word is made available on the data word I/O port, the check word I/O port presents a 6-bit syndrome error code. This syndrome code can be used to identify the bad memory chip.

ERROR SYNDROME TABLE

	SYNDROME ERROR CODE					
ERROR LOCATION	CB0	CB1	CB2	CB3	CB4	CB5
DB0	L	L	H	L	H	H
DB1	L	H	L	L	H	H
DB2	H	L	L	L	H	H
DB3	L	L	H	H	L	H
DB4	L	H	L	H	L	H
DB5	H	L	L	H	L	H
DB6	H	L	H	L	L	H
DB7	H	H	L	L	L	H
DB8	L	L	H	H	H	L
DB9	L	H	L	H	H	L
DB10	L	H	H	L	H	L
DB11	H	L	H	L	H	L
DB12	H	H	L	L	H	L
DB13	L	H	H	H	L	L
DB14	H	L	H	H	L	L
DB15	H	H	L	H	L	L
CB0	L	H	H	H	H	H
CB1	H	L	H	H	H	H
CB2	H	H	L	H	H	H
CB3	H	H	H	L	H	H
CB4	H	H	H	H	L	H
CB5	H	H	H	H	H	L
NO ERROR	H	H	H	H	H	H

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: S0 and S1 . . . . . 7 V
CB and DB . . . . . 5.5 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54LS630, SN54LS631 . . . . . −55°C to 125°C
SN74LS630, SN74LS631 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage Values are with respect to network ground terminal.

recommended operating conditions

		SN54LS630 SN54LS631			SN74LS630 SN74LS631			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	CB or DB, 'LS630 only			−1			−1	mA
	DEF or SEF			−0.4			−0.4	
High-level output voltage, V_{OH}	CB or DB, 'LS631 only			5.5			5.5	V
Low-level output current, I_{OL}	CB or DB			12			24	mA
	DEF or SEF			4			8	
Setup time, t_{su}	CB or DB to S1↑	30			30			ns
Hold time, t_h	CB or DB after S1↑	15			15			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

↑The upward-pointing arrow indicates a transition from low to high.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETERS			TEST CONDITIONS†		SN54LS630 MIN	SN54LS630 TYP‡	SN54LS630 MAX	SN74LS630 MIN	SN74LS630 TYP‡	SN74LS630 MAX	UNIT
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	CB or DB	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} min	I_{OH} = MAX	2.4	3.3		2.4	3.2		V
		DEF or SEF		I_{OH} = −400 μA	2.5	3.4		2.7	3.4		
V_{OL}	Low-level output voltage	CB or DB	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
		DEF or SEF		I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
				I_{OL} = 8 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	CB or DB	V_{CC} = MAX, S0 and S1 at 2 V	V_O = 2.7 V,			20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied	CB or DB	V_{CC} = MAX, S0 and S1 at 2 V	V_O = 0.4 V,			−200			−200	μA
I_I	Input current at maximum input voltage	CB or DB	V_{CC} = MAX, V_{IH} = 4.5 V	V_I = 5.5 V			0.1			0.1	mA
		S0 or S1		V_I = 7 V			0.1			0.1	
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.4 V			−0.2			−0.2	mA
I_{OS}	Short-circuit output current¶	CB or DB	V_{CC} = MAX,		−30		−130	−30		−130	mA
		DEF or SEF			−20		−100	−20		−100	
I_{CC}	Supply current		V_{CC} = MAX, S0 and S1 at 4.5 V, All CB and DB pins grounded, DEF and SEF open			143	230		143	230	mA

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS631 MIN	SN54LS631 TYP‡	SN54LS631 MAX	SN74LS631 MIN	SN74LS631 TYP‡	SN74LS631 MAX	UNIT
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	DEF or SEF	V_{CC} = MIN, V_{IH} = 2 V,	I_{OH} = −400 μA, V_{IL} = V_{IL} max	2.5	3.4		2.7	3.4		V
I_{OH}	High-level output current	CB or DB	V_{CC} = MIN, V_{IH} = 2 V,	V_{OH} = 5.5 V, V_{IL} = V_{IL} max			100			100	μA
V_{OL}	Low-level output voltage	CB or DB	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
		DEF or SEF		I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
				I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	CB or DB	V_{CC} = MAX, V_{IH} = 4.5 V	V_I = 5.5 V			100			100	μA
		S0 or S1		V_I = 7 V			100			100	
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.4 V			−0.2			−0.2	mA
I_{OS}	Short-circuit output current¶	DEF or SEF	V_{CC} = MAX,		−20		−100	−20		−100	mA
I_{CC}	Supply current		V_{CC} = MAX, S0 and S1 at 4.5 V, All CB and DB grounded, SEF and DEF open			113	180		113	180	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
¶Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, C_L = 45 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS630 MIN	'LS630 TYP	'LS630 MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output◇	DB	CB	S0 at 0 V, S1 at 0 V, R_L = 667 Ω, See Figure 1		31	45	ns
t_{PHL} Propagation delay time, high-to-low-level output◇					45	65	ns
t_{PLH} Propagation delay time, low-to-high-level output★	S1↑	DEF	S0 at 3 V, R_L = 2 kΩ, See Figure 1		27	40	ns
		SEF			20	30	
t_{PZH} Output enable time tc high level#	S0↓	CB, DB	S1 at 3 V, R_L = 667 Ω, See Figure 2		24	40	ns
t_{PZL} Output enable time to low level#	S0↓	CB, DB	S1 at 3 V, R_L = 667 Ω, See Figure 1		30	45	ns
t_{PHZ} Output disable time from high level▲	S0↑	CB, DB	S1 at 3 V, R_L = 667 Ω, See Figure 2		43	65	ns
t_{PLZ} Output disable time from low level▲	S0↑	CB, DB	S1 at 3 V, R_L = 667 Ω, See Figure 1		31	45	ns

switching characteristics, V_{CC} = 5 V, T_A = 25°C, C_L = 45 pF, see Figure 1

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS631 MIN	'LS631 TYP	'LS631 MAX	UNIT
t_{PLH} Propagation delay time, low-to-high level output◇	DB	CB	S0 at 0 V, S1 at 0V, R_L = 667 Ω		38	55	ns
t_{PHL} Propagation delay time, high-to-low-level output◇					45	65	ns
t_{PLH} Propagation delay time, low-to-high-level output★	S1↑	DEF	S0 at 3 V, R_L = 2 kΩ		27	40	ns
		SEF			20	30	ns
t_{PHL} Propagation delay time, high-to-low-level output#	S0↓	CB, DB	S1 at 3 V, R_L = 667 kΩ		28	45	ns
t_{PLH} Propagation delay time, low-to-high-level output▲	S0↑	CB, DB	S1 at 3 V, R_L = 667 kΩ		33	50	ns

◇These parameters describe the time intervals taken to generate the check word during the memory write cycle.
★These parameters describe the time intervals taken to flag errors during the memory read cycle.
#These parameters describe the time intervals taken to correct and output the data word and to generate and output the syndrome error code during the memory read cycle.
▲These parameters describe the time intervals taken to disable the CB and DB buses in preparation for a new data word during the memory read cycle.

PARAMETER MEASUREMENT INFORMATION

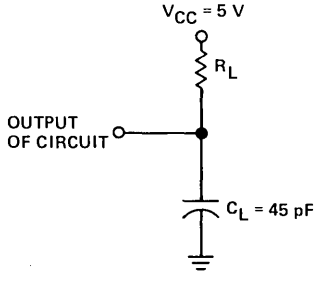

FIGURE 1–OUTPUT LOAD CIRCUIT

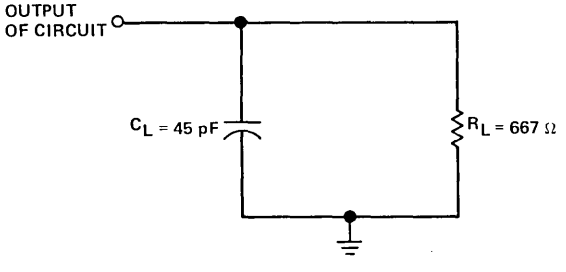

FIGURE 2–OUTPUT LOAD CIRCUIT

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TYPES SN54LS638, SN54LS639, SN74LS638, SN74LS639
OCTAL BUS TRANSCEIVERS

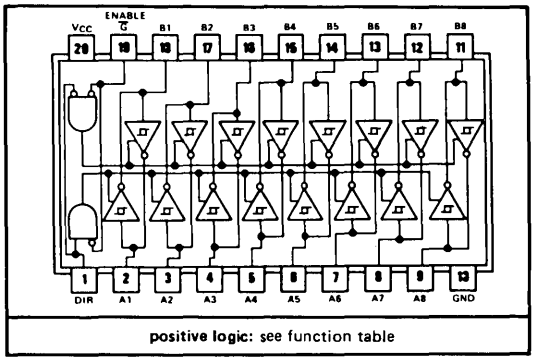
D2636, JANUARY 1981

- Bidirectional Bus Transceivers in High-Density 20-Pin Packages
- Hysteresis at Bus Inputs Improves Noise Margins
- Choice of True or Inverting Logic
- A Bus Outputs are Open-Collector, B Bus Outputs are 3-State

description

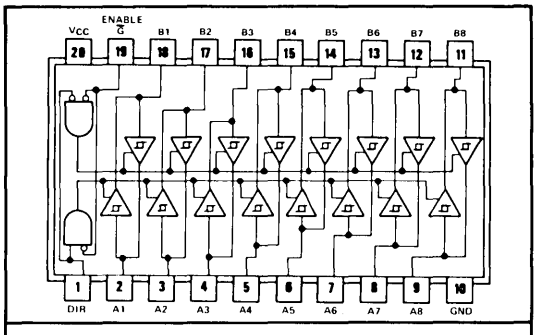
These octal bus transceivers are designed for asynchronous two-way communication between open-collector and 3-state buses. The devices transmit data from the A bus (open-collector) to the B bus (3-state) or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so the buses are isolated.

SN54LS638 . . J PACKAGE
SN74LS638 . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

SN54LS639 . . J PACKAGE
SN74LS639 . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

FUNCTION TABLE

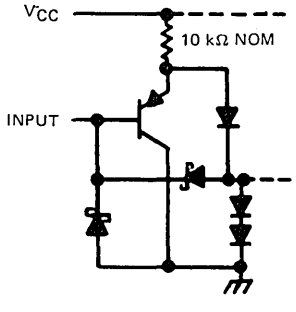
CONTROL INPUTS		OPERATION	
		'LS638	'LS639
$\overline{G}$	DIR		
L	L	$\overline{B}$ data to A bus	B data to A bus
L	H	$\overline{A}$ data to B bus	A data to B bus
H	X	Isolation	Isolation

H = high level, L = low level, X = irrelevant

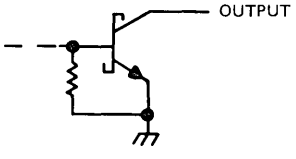
DEVICE	A OUTPUT	B OUTPUT	LOGIC
'LS638	Open-Collector	3-State	Inverting
'LS639	Open-Collector	3-State	True

schematics of inputs and outputs

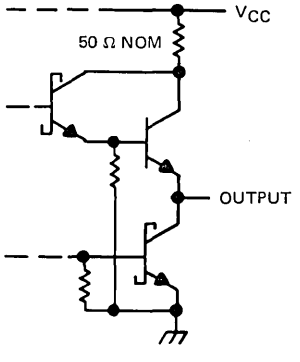
EQUIVALENT OF EACH INPUT



TYPICAL OF A OUTPUTS



TYPICAL OF B OUTPUTS



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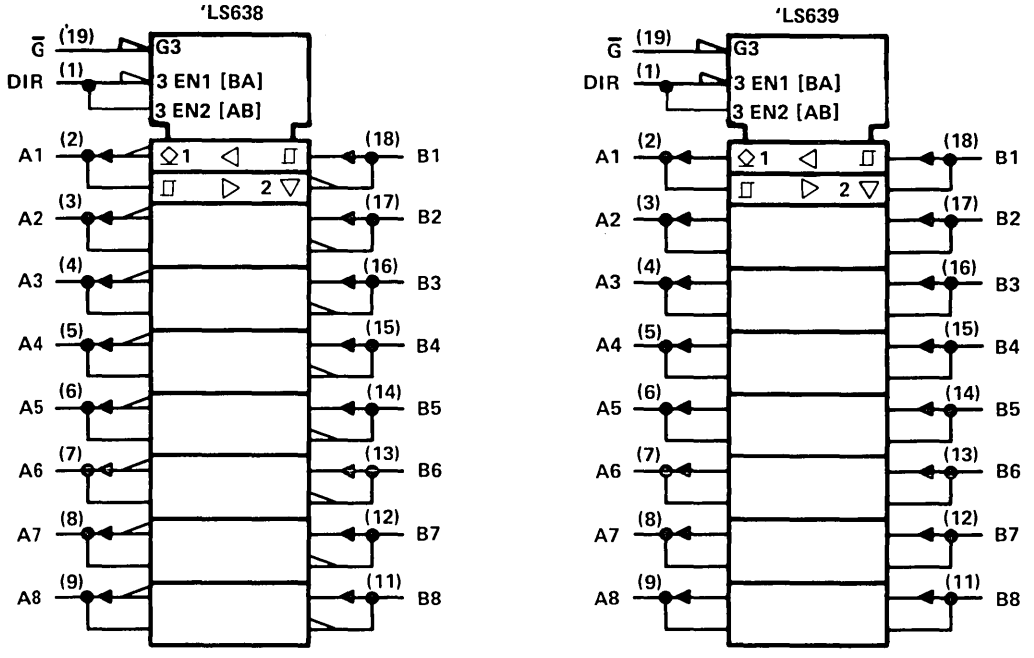
logic symbols



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (DIR or $\overline{G}$) . . . . . 7 V
Off-state output voltage (A or B) . . . . . 5.5 V
Operating free-air temperature range: SN54LS638, SN54LS639 . . . . . −55°C to 125°C
SN74LS638, SN74LS639 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH} (A bus)			5.5			5.5	V
High-level output current, I_{OH} (B bus)			−12			−15	mA
Low-level output current, I_{OL} (A or B bus)			12			24	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.5			0.6	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
	Hysteresis ($V_{T+}-V_{T-}$)		V_{CC} = MIN		0.1	0.4		0.2	0.4		V
I_{OH}	High-level output current	A	V_{CC} = MIN, V_{IH} = 2 V, $V_{IL}=V_{IL}$ max, V_{OH} = 5.5 V				100			100	μA
V_{OH}	High-level output voltage	B	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OH} = −3 mA	2.4			2.4			V
				I_{OH} = MAX	2			2			
V_{OL}	Low-level output voltage	A or B	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	B	V_{CC} = MIN, $\overline{G}$ at 2 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	Off-state output current low-level voltage applied	A or B	V_{CC} = MIN, $\overline{G}$ at 2 V,	V_O = 0.4 V			−400			−400	μA
I_I	Input current at maximum input voltage	A or B	V_{CC} = MAX	V_I = 5.5 V			0.1			0.1	mA
		DIR or $\overline{G}$		V_I = 7 V			0.1			0.1	
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	B	V_{CC} = MAX		−40		−225	−40		−225	mA
I_{CCH}	Supply current, outputs high		V_{CC} = MAX, Outputs open			48	70		48	70	mA
I_{CCL}	Supply current, outputs low		V_{CC} = MAX, Outputs open			62	90		62	90	mA
I_{CCZ}	Supply current, outputs off		V_{CC} = MAX, Outputs open			64	95		64	95	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, see note 2

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS638			'LS639			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	A	B	C_L = 45 pF, R_L = 667 Ω		6	10		8	15	ns
	B	A			17	25		19	25	
t_{PHL}	A	B			8	15		11	15	ns
	B	A			14	25		16	25	
t_{PLH}	$\overline{G}$, DIR	A			26	40		23	40	ns
t_{PHL}	$\overline{G}$, DIR	A			43	60		34	50	ns
t_{PZH}	$\overline{G}$, DIR	B			23	40		26	40	ns
t_{PZL}	$\overline{G}$, DIR	B			31	40		31	40	ns
t_{PHZ}	$\overline{G}$, DIR	B	C_L = 5 pF, R_L = 667 Ω		15	25		15	25	ns
t_{PLZ}	$\overline{G}$, DIR	B			15	25		15	25	ns

NOTE 2: Load circuit and voltage waveforms are shown on page 3-11 of "The TTL Data Book for Design Engineers", second edition.
t_{PLH} ≡ Propagation delay time, low-to-high-level input.
t_{PHL} ≡ Propagation delay time, high-to-low-level input.
t_{PZL} ≡ Output enable time to low level
t_{PZH} ≡ Output enable time to high level
t_{PLZ} ≡ Output disable time from low level
t_{PHZ} ≡ Output disable time from high level

TYPICAL CHARACTERISTICS

SN54LS'
INVERTING OUTPUT VOLTAGE
vs
INPUT VOLTAGE

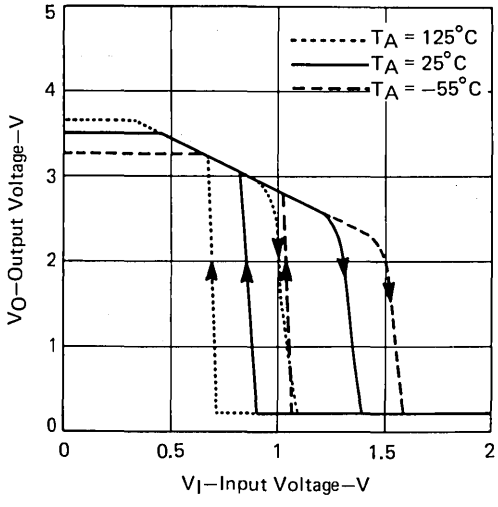


FIGURE 1

SN74LS'
INVERTING OUTPUT VOLTAGE
vs
INPUT VOLTAGE

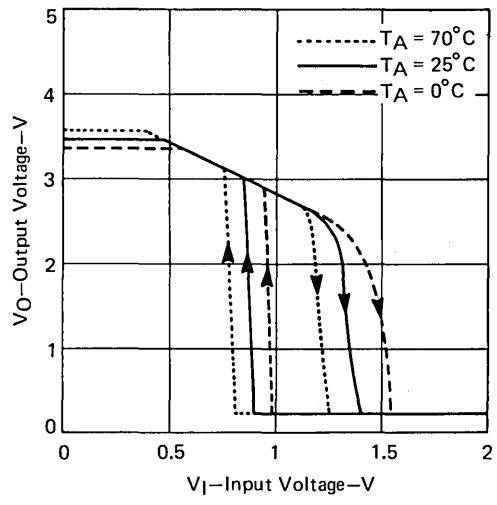


FIGURE 2

SN54LS'
NONINVERTING OUTPUT VOLTAGE
vs
INPUT VOLTAGE

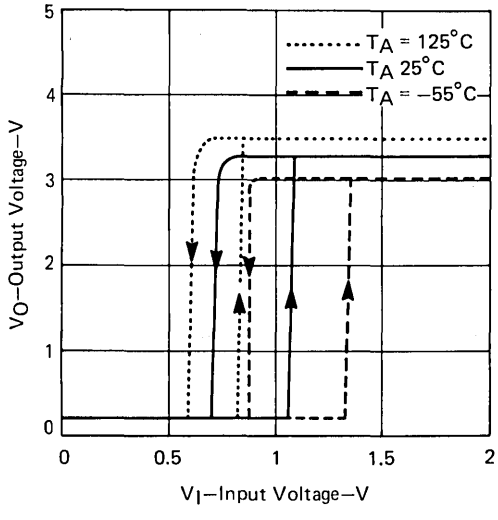


FIGURE 3

SN74LS'
NONINVERTING OUTPUT VOLTAGE
vs
INPUT VOLTAGE

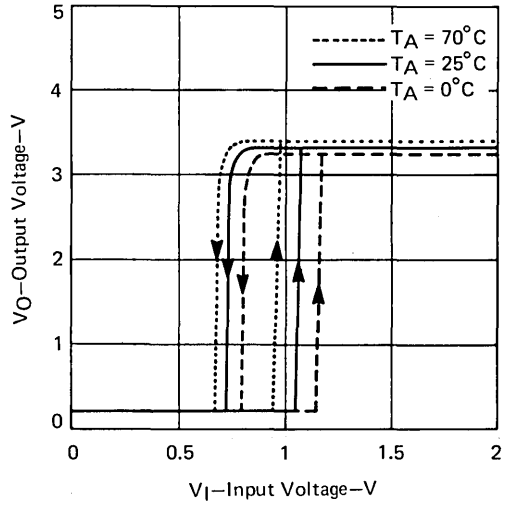


FIGURE 4

TEXAS INSTRUMENTS
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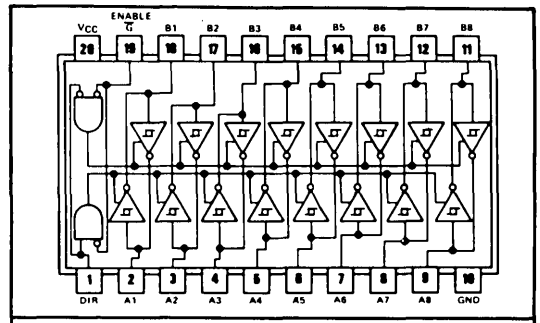
TYPES SN54LS640 THRU SN54LS645, SN74LS640 THRU SN74LS645 OCTAL BUS TRANSCEIVERS

D2420, APRIL 1979

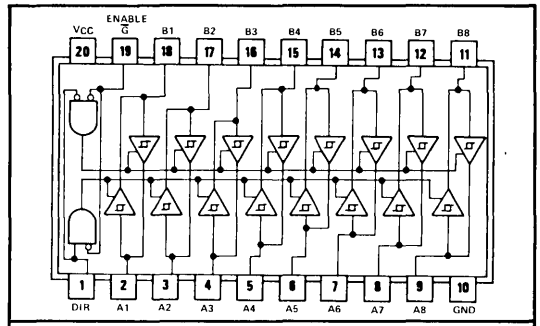
- SN74LS64X-1 Versions Rated at I_{OL} of 48 mA
- Bi-directional Bus Transceivers in High-Density 20-Pin Packages
- Hysteresis at Bus Inputs Improves Noise Margins
- Choice of True or Inverting Logic
- Choice of 3-State or Open-Collector Outputs

SN54LS640, SN54LS642 . . . J PACKAGE
SN74LS640, SN74LS642 . . . J OR N PACKAGE
(TOP VIEW)



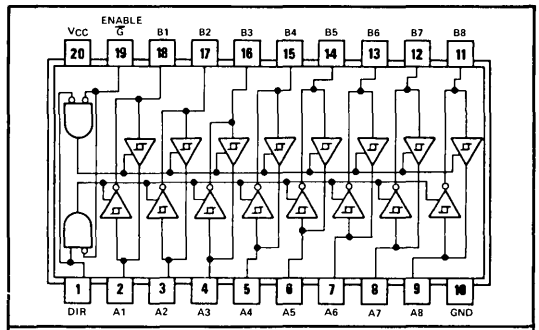
positive logic: see function table

SN54LS641, SN54LS645 . . . J PACKAGE
SN74LS641, SN74LS645 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

SN54LS643, SN54LS644 . . . J PACKAGE
SN74LS643, SN74LS644 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated.

DEVICE	OUTPUT	LOGIC
'LS640	3-State	Inverting
'LS641	Open-Collector	True
'LS642	Open-Collector	Inverting
'LS643	3-State	True and inverting
'LS644	Open-Collector	True and inverting
'LS645	3-State	True

FUNCTION TABLE

CONTROL INPUTS		OPERATION		
$\overline{G}$	DIR	'LS640 'LS642	'LS641 'LS645	'LS643 'LS644
L	L	$\overline{B}$ data to A bus	B data to A bus	B data to A bus
L	H	$\overline{A}$ data to B bus	A data to B bus	$\overline{A}$ data to B bus
H	X	Isolation	Isolation	Isolation

H = high level, L= low level, X = irrelevant

absolute maximum ratings

Same as SN54LS245 and SN74LS245 maximum ratings on page 7-349 of *The TTL Data Book for Design Engineers*, Second Edition.

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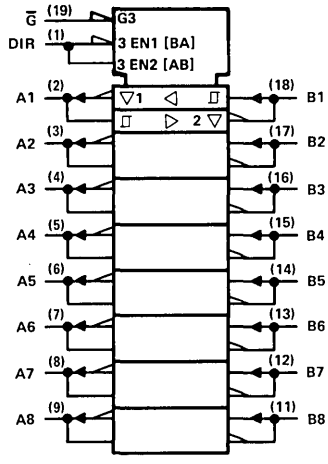
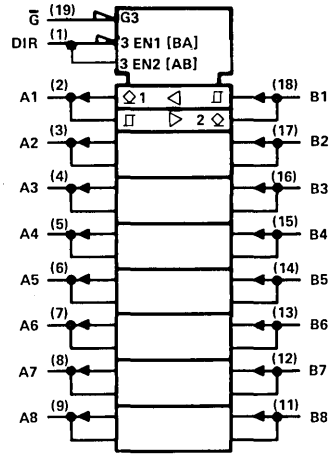
logic symbols

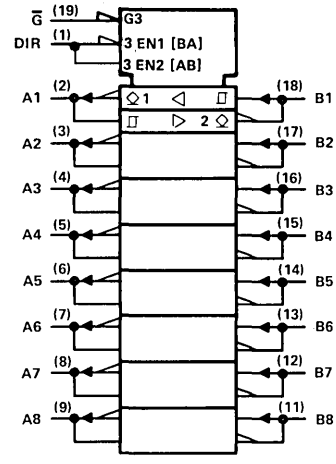
'LS640



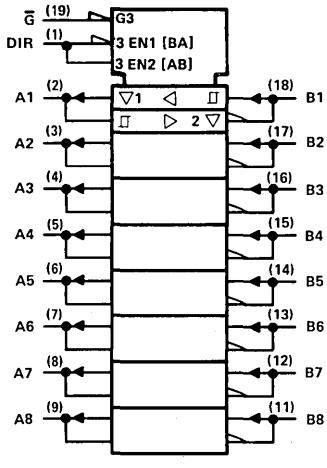
'LS641



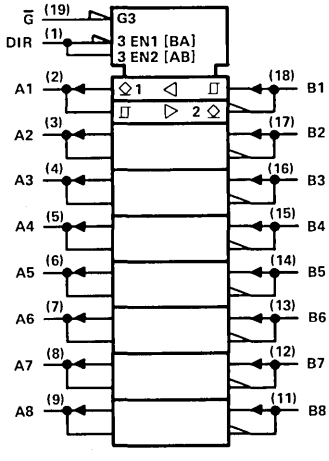
'LS642



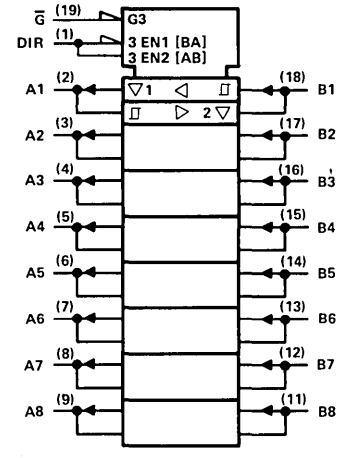
'LS643



'LS644



'LS645



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recommended operating conditions

PARAMETER	SN54LS640 SN54LS643 SN54LS645			SN74LS640 SN74LS643 SN74LS645			SN74LS640–1 SN74LS643–1 SN74LS645–1			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	4.75	5	5.25	V
High-level output current, I_{OH}			−12			−15			−15	mA
Low-level output current, I_{OL}			12			24			48	mA
Operating free-air temperature, T_A	−55		125	0		70	0		70	°C

NOTE 1: Voltage values are with respect to the network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS640 SN54LS643 SN54LS645			SN74LS640 SN74LS643 SN74LS645			SN74LS640–1 SN74LS643–1 SN74LS645–1			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			2			V
V_{IL}	Low-level input voltage						0.5			0.6			0.6	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5			−1.5	V
	Hysteresis ($V_{T+} - V_{T-}$) A or B input		V_{CC} = MIN		0.1	0.4		0.2	0.4		0.2	0.4		V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OH} = −3 mA	2.4	3.4		2.4	3.4		2.4	3.4		V
				I_{OH} = MAX	2			2			2			
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5		0.35	0.5	
				I_{OL} = 48 mA								0.4	0.5	
I_{OZH}	Off-state output current, high-level voltage applied		V_{CC} = MAX, V_O = 2.7 V	$\overline{G}$ at 2 V,			20			20			20	µA
I_{OZL}	Off-state output current, low-level voltage applied		V_{CC} = MAX, V_O = 0.4 V	$\overline{G}$ at 2 V,			−400			−400			−400	µA
I_I	Input current at maximum input voltage	A or B	V_{CC} = MAX	V_I = 5.5 V			0.1			0.1			0.1	mA
		DIR or $\overline{G}$		V_I = 7 V			0.1			0.1			0.1	
I_{IH}	High-level input current		V_{CC} = MAX,	V_{IH} = 2.7 V			20			20			20	µA
I_{IL}	Low-level input current		V_{CC} = MAX,	V_{IL} = 0.4 V			−0.4			−0.4			−0.4	mA
I_{OS}	Short-circuit output current¶		V_{CC} = MAX		−40		−225	−40		−225	−40		−225	mA
I_{CC}	Total supply current	Outputs high	V_{CC} = MAX,	Outputs open		48	70		48	70		48	70	mA
		Outputs low				62	90		62	90		62	90	
		Outputs at Hi-Z				64	95		64	95		64	95	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
¶Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics at V_{CC} = 5 V, T_A = 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS640, 'LS640–1			'LS643, 'LS643–1			'LS645, 'LS645–1			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	A	B	C_L = 45 pF, R_L = 667 Ω, See Note 2		6	10		6	10		8	15	ns
		B	A			6	10		8	15		8	15	
t_{PHL}	Propagation delay time, high-to-low-level output	A	B			8	15		9	15		11	15	ns
		B	A			8	15		11	15		11	15	
t_{PZL}	Output enable time to low level	$\overline{G}$, DIR	A			31	40		32	45		31	40	ns
		$\overline{G}$, DIR	B			31	40		32	45		31	40	
t_{PZH}	Output enable time to high level	$\overline{G}$, DIR	A			23	40		27	40		26	40	ns
		$\overline{G}$, DIR	B			23	40		23	40		26	40	
t_{PLZ}	Output disable time from low level	$\overline{G}$, DIR	A	C_L = 5 pF, R_L = 667 Ω, See Note 2		15	25		15	25		15	25	ns
		$\overline{G}$, DIR	B			15	25		15	25		15	25	
t_{PHZ}	Output disable time from high level	$\overline{G}$, DIR	A			15	25		15	25		15	25	ns
		$\overline{G}$, DIR	B			15	25		15	25		15	25	

NOTE 2: For load circuits and voltage waveforms, see page 3-11 of *The TTL Data Book for Design Engineers,* Second Edition.

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT

TYPICAL OF OUTPUTS

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TYPICAL CHARACTERISTICS

SN54LS'
INVERTING OUTPUT VOLTAGE
vs
INPUT VOLTAGE

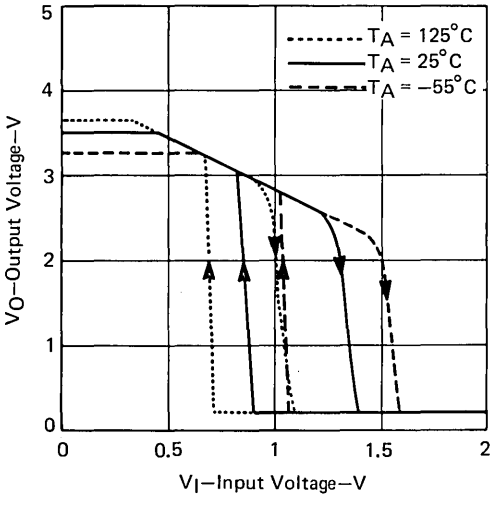


FIGURE 1

SN74LS'
INVERTING OUTPUT VOLTAGE
vs
INPUT VOLTAGE

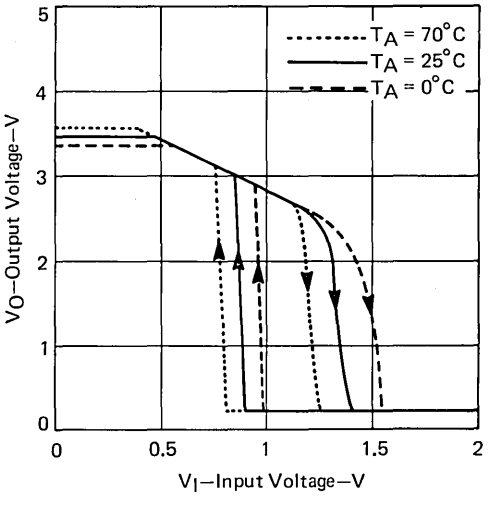


FIGURE 2

SN54LS'
NONINVERTING OUTPUT VOLTAGE
vs
INPUT VOLTAGE

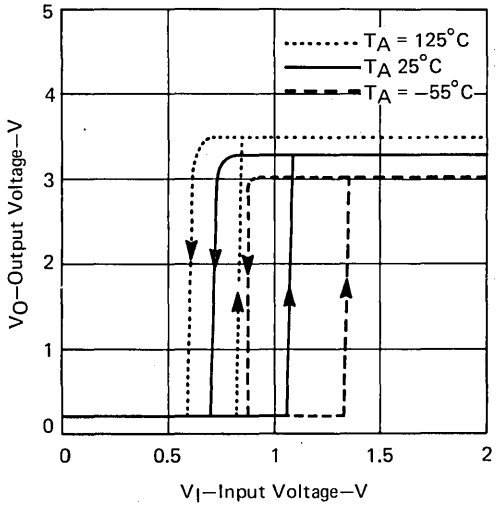


FIGURE 3

SN74LS'
NONINVERTING OUTPUT VOLTAGE
vs
INPUT VOLTAGE

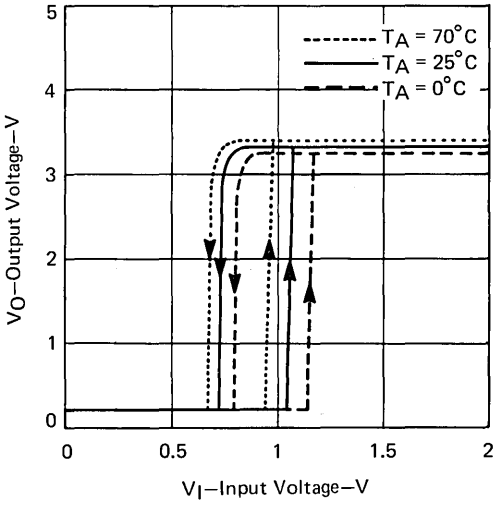


FIGURE 4

recommended operating conditions

PARAMETER	SN54LS641 SN54LS642 SN54LS644			SN74LS641 SN74LS642 SN74LS644			SN74LS641–1 SN74LS642–1 SN74LS644–1			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5			5.5	V
Low-level output current, I_{OL}			12			24			48	mA
Operating free-air temperature, T_A	−55		125	0		70	0		70	°C

NOTE 1 : Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS641 SN54LS642 SN54LS644			SN74LS641 SN74LS642 SN74LS644			SN74LS641–1 SN74LS642–1 SN74LS644–1			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			2			V
V_{IL}	Low-level input voltage						0.5			0.6			0.6	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5			−1.5	V
	Hysteresis ($V_{T+} - V_{T-}$) A or B input		V_{CC} = MIN		0.1	0.4		0.2	0.4		0.2	0.4		V
I_{OH}	High-level output current		V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, V_{OH} = 5.5 V			100			100			100	μA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5		0.35	0.5	
				I_{OL} = 48 mA								0.4	0.5	
I_I	Input current at maximum input voltage	A or B	V_{CC} = MAX	V_I = 5.5 V			0.1			0.1			0.1	mA
		DIR or $\overline{G}$		V_I = 7 V			0.1			0.1			0.1	
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V			20			20			20	μA
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4			−0.4	mA
I_{CC}	Total Supply Current	Outputs high	V_{CC} = MAX,	Outputs open		48	70		48	70		48	70	mA
		Outputs low				62	90		62	90		62	90	
		Outputs at Hi-Z				64	95		64	95		64	95	

†For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions.
‡All Typical values are at V_{CC} = 5 V, T_A = 25°C.

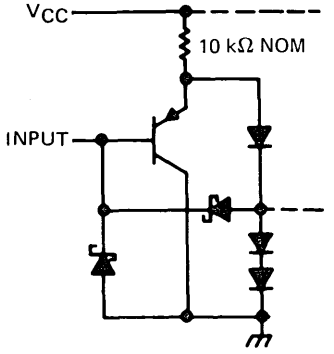
switching characteristics at V_{CC} = 5 V, T_A = 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS641, 'LS641–1			'LS642, 'LS642–1			'LS644, 'LS644–1			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	A	B	C_L = 45 pF, R_L = 667 Ω, See Note 2		17	25		19	25		17	25	ns
		B	A			17	25		19	25		19	25	
t_{PHL}	Propagation delay time, high-to-low-level output	A	B			16	25		14	25		14	25	ns
		B	A			16	25		14	25		16	25	
t_{PLH}	Output disable time from low level	$\overline{G}$, DIR	A			23	40		26	40		26	40	ns
		$\overline{G}$, DIR	B			25	40		28	40		25	40	
t_{PHL}	Output enable time from high level	$\overline{G}$, DIR	A			34	50		43	60		43	60	ns
		$\overline{G}$, DIR	B			37	50		39	60		37	50	

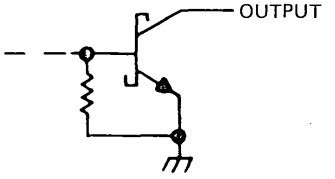
NOTE 2: For load circuits and voltage waveforms, see page 3-11 of *The TTL Data Book for Design Engineers,* Second Edition.

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF OUTPUTS



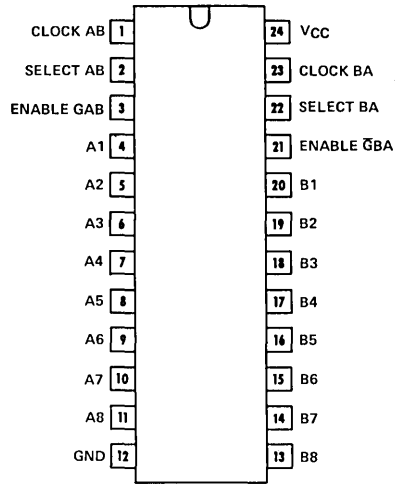
TYPES SN54LS646 THRU SN54LS649
SN74LS646 THRU SN74LS649
OCTAL BUS TRANSCEIVERS AND REGISTERS

D2581, JANUARY 1981

- Bidirectional Bus Transceivers/Registers in the New JT and NT 24-pin 300-mil Packages
- Independent Registers for A and B Buses
- Multiplexed Real-Time and Stored Data
- Choice of True and Inverting Data Paths
- Choice of 3-State or Open-Collector Outputs

DEVICE	OUTPUT	LOGIC
'LS646	3-State	True
'LS647	Open-Collector	True
'LS648	3-State	Inverting
'LS649	Open-Collector	Inverting

SN54LS'. . . JT PACKAGE
SN74LS'. . . JT OR NT PACKAGE
(TOP VIEW)

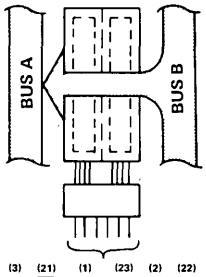


description

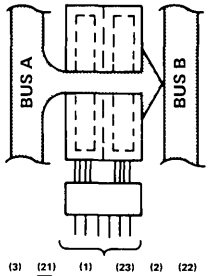
These devices consist of bus transceiver circuits with 3-state or open-collector outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a high logic level. Control $\overline{G}$ and direction pins are provided to control the transceiver function. In the transceiver mode, data present at the high-impedance port may be stored in either the A or the B register or in both. The select controls can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when the enable control $\overline{G}$ is active (low). In the isolation mode (control $\overline{G}$ high), A data may be stored in the B register and/or B data may be stored in the A register.

When an output function is disabled, the input function is still enabled, and may be used to store and transmit data. Only one of the two buses, A or B may be driven at a time.

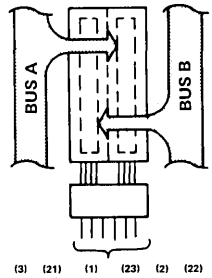
The following examples demonstrate the four fundamental bus-management functions that can be performed with the 'LS646, 'LS647, 'LS648, or 'LS649.



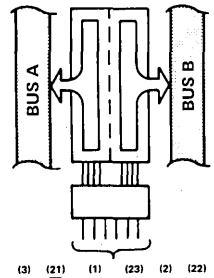
REAL-TIME TRANSFER
BUS B TO BUS A



REAL-TIME TRANSFER
BUS A TO BUS B



STORAGE



TRANSFER
STORED DATA
TO A OR B

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS INSTRUMENTS
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FUNCTION TABLE

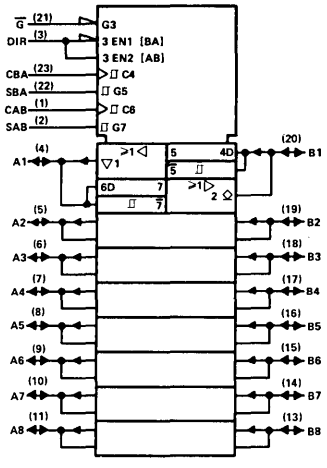
INPUTS						DATA I/O*		OPERATION OR FUNCTION	
$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	'LS646, 'LS647	'LS648, 'LS649
H	X	H or L	H or L	X	X	Input	Input	Isolation	Isolation
H	X	↑	↑	X	X			Store A and B Data	Store A and B Data
L	L	X	X	X	L	Output	Input	Real Time B Data to A Bus	Real Time $\overline{B}$ Data to A Bus
L	L	X	X	X	H			Stored B Data to A Bus	Stored $\overline{B}$ Data to A Bus
L	H	X	X	L	X	Input	Output	Real Time A Data to B Bus	Real Time $\overline{A}$ Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus	Stored $\overline{A}$ Data to B Bus

H = high level L = low level X = irrelevant ↑ = low-to-high-level transition

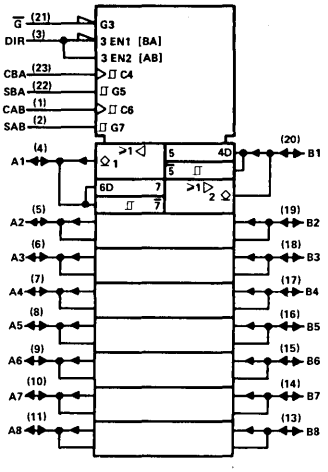
*The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

logic symbols

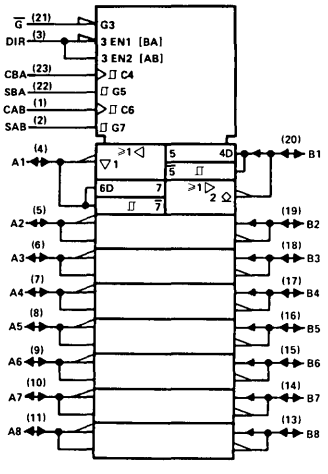
'LS646



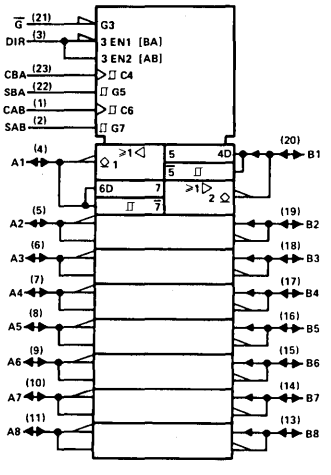
'LS647



'LS648

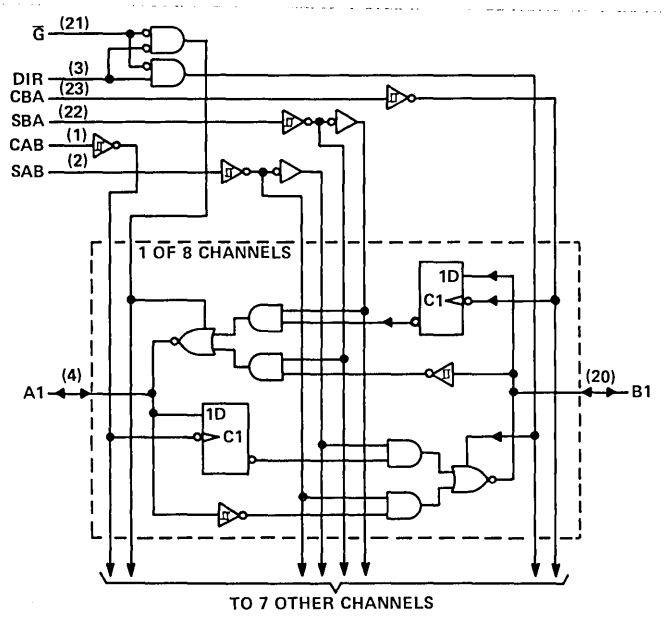


'LS649

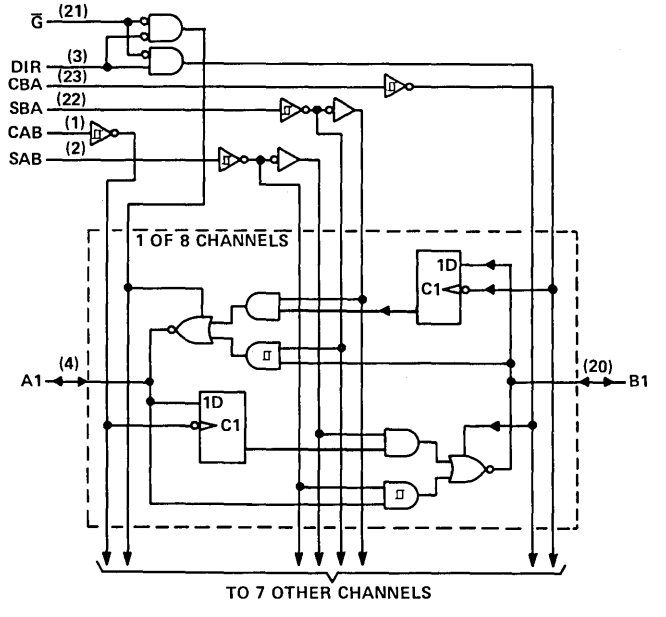


functional block diagram (positive logic)

'LS646, 'LS647

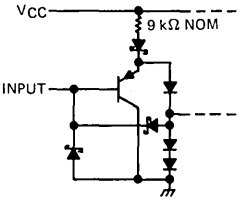


'LS648, 'LS649

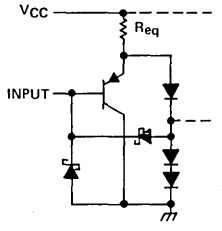


schematics of inputs and outputs

EQUIVALENT OF DIRECTION INPUTS

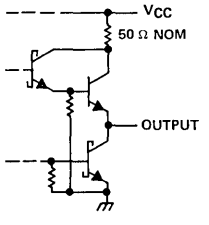


EQUIVALENT OF ALL OTHER INPUTS

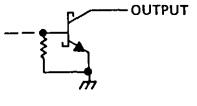


A and B: R_{eq} = 15 kΩ NOM
CAB and CBA: R_{eq} = 10 kΩ NOM
SAB and SBA: R_{eq} = 6 kΩ NOM

TYPICAL OF ALL 'LS646, 'LS648 OUTPUTS



TYPICAL OF ALL 'LS647, 'LS649 OUTPUTS



TEXAS INSTRUMENTS
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absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (control inputs) . . . . . 7 V
Off-state output voltage (A and B ports) . . . . . 5.5 V
Operating free-air temperature: SN54LS646, SN54LS648 . . . . . −55°C to 125°C
SN74LS646, SN74LS648 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54LS646 SN54LS648			SN74LS646 SN74LS648			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−12			−15	mA
Low-level output current, I_{OL}				12			24	mA
Width of clock pulse, t_w		20			20			ns
Setup time, t_{su}	Bus to clock	20			20			ns
Hold time, t_h	Bus from clock	0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

NOTE 1: All voltage values are with respect to the network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS646 SN54LS648			SN74LS646 SN74LS648			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.5			0.6	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
	Hysteresis ($V_{t+} - V_{T-}$), A or B input		V_{CC} = MIN		0.1	0.4		0.2	0.4		V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OH} = −3 mA	2.4	3.4		2.4	3.4		V
				I_{OH} = MAX	2			2			
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied		V_{CC} = MAX,	V_O = 2.7 V			20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied		V_{CC} = MAX,	V_O = 0.4 V			−400			−400	μA
I_I	Input current at maximum input voltage	A or B	V_{CC} = MAX	V_I = 5.5 V			0.1			0.1	mA
		All others		V_I = 7 V			0.1			0.1	
I_{IH}	High-level input current		V_{CC} = MAX,	V_{IH} = 2.7 V			20			20	μA
I_{IL}	Low-level input current		V_{CC} = MAX,	V_{IL} = 0.4 V			−0.4			−0.4	mA
I_{OS}	Short-circuit output current¶		V_{CC} = MAX,	V_O = 0	−40		−225	−40		−225	mA
I_{CC}	Total supply current	'LS646	V_{CC} = MAX, Outputs open	Outputs high		91	145		91	145	mA
				Outputs low		103	165		103	165	
				Outputs at Hi-Z		103	165		103	165	
		'LS648	V_{CC} = MAX, Outputs open	Outputs high		78			78		
				Outputs low		86			86		
				Outputs at Hi-Z		88			88		

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
¶Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER◇	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS646			'LS648			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Clock	Bus	R_L = 667 Ω, C_L = 45 pF, See Note 2		15	25		15		ns
t_{PHL}					23	35		26		ns
t_{PLH}	Bus	Bus			12	18		25		ns
t_{PHL}					13	20		23		ns
t_{PLH}	Select, with bus input high†	Bus			33	50		36		ns
t_{PHL}					14	25		36		ns
t_{PLH}	Select, with bus input low†				26	40		27		ns
t_{PHL}					21	35		27		ns
t_{PZH}	Enable	Bus			33	55		30		ns
t_{PZL}					42	65		38		ns
t_{PZH}	Direction				28	45		24		ns
t_{PZL}					39	60		35		ns
t_{PHZ}	Enable	Bus	R_L = 667 Ω, C_L = 5 pF, See Note 2		23	35		23		ns
t_{PLZ}					22	35		22		ns
t_{PHZ}	Direction				20	30		23		ns
t_{PLZ}					19	30		19		ns

t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
t_{PHZ} ≡ output disable time from high level
t_{PLZ} ≡ output disable time from low level

†These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

NOTE 2: Load circuits and voltage waveforms are shown on page 3-11 of *The TTL Data Book for Design Engineers*, second edition.

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (control inputs) . . . . . 7 V
Off-state output voltage (A and B ports) . . . . . 5.5 V
Operating free-air temperature range: SN54LS647, SN54LS649 . . . . . −55°C to 125°C
SN74LS647, SN74LS649 . . . . . −0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54LS647 SN54LS649			SN74LS647 SN74LS649			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)		4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}				5.5			5.5	V
Low-level output current, I_{OL}				12			24	mA
Width of clock pulse, t_w		20			20			ns
Setup time, t_{su}	Bus to clock	20			20			ns
Hold time, t_h	Bus from clock	0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

NOTE 1: All voltage values are with respect to the network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS647 SN54LS649			SN74LS647 SN74LS649			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.5			0.6	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
	Hysteresis ($V_{t+} - V_{T-}$), A or B input		V_{CC} = MIN		0.1	0.4		0.2	0.4		V
I_{OH}	High-level output current		V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, V_{OH} = 5.5 V			100			100	μA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
I_I	Input current at maximum input voltage	A or B	V_{CC} = MAX,	V_I = 5.5 V			0.1			0.1	mA
		All others		V_I = 7 V			0.1			0.1	
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.5 V			20			20	μA
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
I_{CC}	Total Supply Current	'LS647	V_{CC} = MAX, Outputs open	Outputs high		79	130		79	130	mA
				Outputs low		94	150		94	150	
		'LS649	V_{CC} = MAX, Outputs open	Outputs high		76			76		
				Outputs low		90			90		

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS647			'LS649			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Clock	Bus	R_L = 667 Ω, C_L = 45 pF, See Note 2		22	35		24		ns
t_{PHL}					28	45		26		ns
t_{PLH}	Bus	Bus			17	26		23		ns
t_{PHL}					18	27		23		ns
t_{PLH}	Select, with bus input high†	Bus			39	60		42		ns
t_{PHL}					19	30		36		ns
t_{PLH}	Select, with bus input low†				33	50		36		ns
t_{PHL}					29	45		27		ns
t_{PLH}	Enable	Bus			25	40		25		ns
t_{PHL}					33	50		35		ns
t_{PLH}	Direction				23	35		32		ns
t_{PHL}					25	40		29		ns

t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output

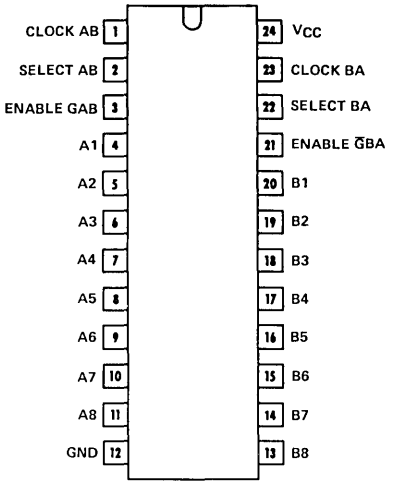
†These parameters are measured with the internal outputs state of the storage register opposite to that of the bus input.

NOTE 2: Load circuits and voltage waveforms are shown on page 3-11 of *The TTL Data Book for Design Engineers*, second edition.

D2637, JANUARY 1981

- Bidirectional Bus Transceivers/Registers in the New JT and NT 24-pin 300-mil Packages
- Independent Registers and Enables for A and B Buses
- Multiplexed Real-Time and Stored Data
- Choice of True and Inverting Data Paths
- 3-State Outputs Drive Bus Lines Directly

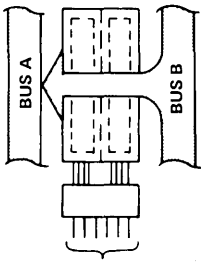
SN54LS'. . . JT PACKAGE
SN74LS'. . . JT OR NT PACKAGE
(TOP VIEW)



description

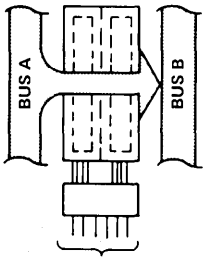
These devices consist of bus transceiver circuits with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a high logic level. Independent enable pins are provided to control the transceiver function. In the transceiver mode, data present at the high-impedance port may be stored in either the A or the B register or in both. The select controls can multiplex stored and real-time (transparent mode) data. The enable pins can control the direction of data in the transceiver modes, disable all bus outputs (leaving the inputs active) for isolation, or enable the bus outputs in a data swap operation. Data can still be stored in the isolation mode. The buses may be driven simultaneously from storage.

The following examples demonstrate the four fundamental bus-management functions that can be performed with the 'LS651 or 'LS652.



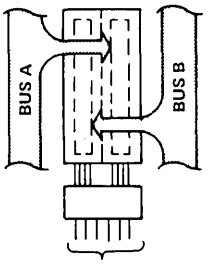
(3) GAB	(21) $\overline{GBA}$	(1) CAB	(23) CBA	(2) SAB	(22) SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



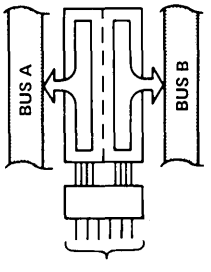
(3) GAB	(21) $\overline{GBA}$	(1) CAB	(23) CBA	(2) SAB	(22) SBA
H	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



(3) GAB	(21) $\overline{GBA}$	(1) CAB	(23) CBA	(2) SAB	(22) SBA
L	H	↑	↑	X	X

STORAGE



(3) GAB	(21) $\overline{GBA}$	(1) CAB	(23) CBA	(2) SAB	(22) SBA
H	L	H or L	H or L	H	H

TRANSFER
STORED DATA
TO A AND/OR B

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

FUNCTION TABLE

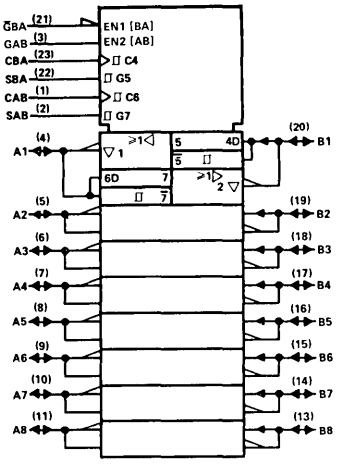
INPUTS						DATA I/O*		OPERATION OR FUNCTION	
GAB	$\overline{G}$BA	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	'LS651	'LS652
L	H	H or L	H or L	X	X	Input	Input	Isolation	Isolation
L	H	↑	↑	X	X			Store A and B Data	Store A and B Data
L	L	X	X	X	L	Output	Input	Real Time $\overline{B}$ Data to A Bus	Real Time B Data to A Bus
L	L	X	H or L	X	H			Stored $\overline{B}$ Data to A Bus	Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real Time $\overline{A}$ Data to B Bus	Real Time A Data to B Bus
H	H	H or L	X	H	X			Stored $\overline{A}$ Data to B Bus	Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{A}$ Data to B Bus and Stored $\overline{B}$ Data to A Bus	Stored A Data to B Bus and Stored B Data to A Bus

H = high level L = low level X = irrelevant ↑ = low-to-high-level transition

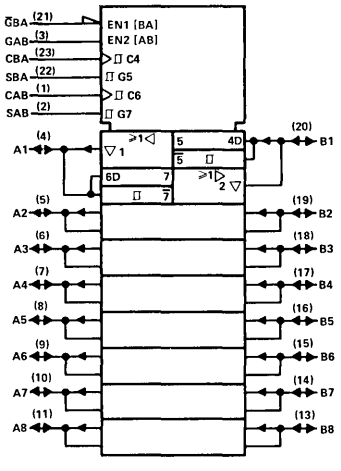
*The data output functions may be enabled or disabled by various signals at the GAB and $\overline{G}$BA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

logic symbols

'LS651

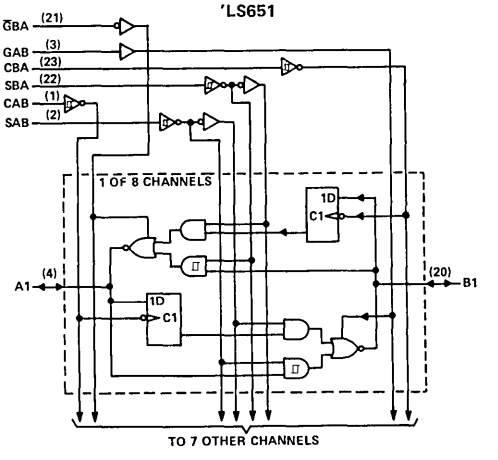


'LS652

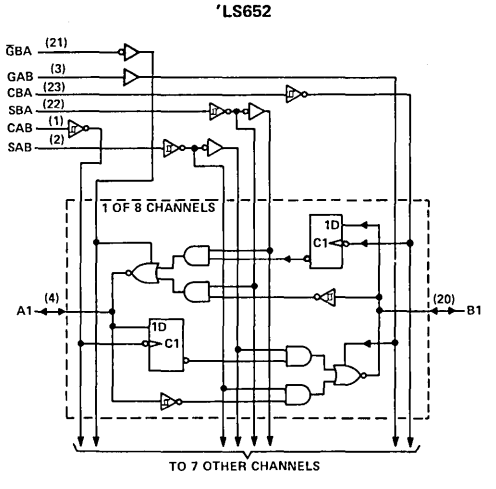


functional block diagram (positive logic)

'LS651



'LS652



TEXAS INSTRUMENTS
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absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (control inputs) . . . . . 7 V
Off-state output voltage (A and B ports) . . . . . 5.5 V
Operating free-air temperature: SN54LS651, SN54LS652 . . . . . −55°C to 125°C
SN74LS651, SN74LS652 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54LS651 SN54LS652			SN74LS651 SN74LS652			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−12			−15	mA
Low-level output current, I_{OL}				12			24	mA
Width of clock pulse, t_w		20			20			ns
Setup time, t_{su}	Bus to clock	20			20			ns
Hold time, t_h	Bus from clock	0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

NOTE 1: All voltage values are with respect to the network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS651 SN54LS652			SN74LS651 SN74LS652			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.5			0.6	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
	Hysteresis ($V_{t+} - V_{T-}$), A or B input		V_{CC} = MIN		0.1	0.4		0.2	0.4		V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OH} = −3 mA	2.4	3.4		2.4	3.4		V
				I_{OH} = MAX	2			2			
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied		V_{CC} = MAX,	V_O = 2.7 V			20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied		V_{CC} = MAX,	V_O = 0.4 V			−400			−400	μA
I_I	Input current at maximum input voltage	A or B	V_{CC} = MAX	V_I = 5.5 V			0.1			0.1	mA
		All others		V_I = 7 V			0.1			0.1	
I_{IH}	High-level input current		V_{CC} = MAX,	V_{IH} = 2.7 V			20			20	μA
I_{IL}	Low-level input current		V_{CC} = MAX,	V_{IL} = 0.4 V			−0.4			−0.4	mA
I_{OS}	Short-circuit output current¶		V_{CC} = MAX,	V_O = 0	−40		−225	−40		−225	mA
I_{CC}	Total supply current	'LS651	V_{CC} = MAX, Outputs open	Outputs high		78			78		mA
				Outputs low		86			86		
				Outputs at Hi-Z		88			88		
		'LS652	V_{CC} = MAX, Outputs open	Outputs high		91			91		
				Outputs low		103			103		
				Outputs at Hi-Z		103			103		

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
¶Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

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switching characteristics, V_{CC} = 5 V, T_A = 25°C

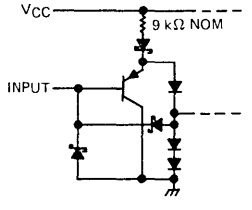
PARAMETER◇	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS651			'LS652			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Clock	Bus	R_L = 667 Ω, C_L = 45 pF, See Note 2		15			15		ns
t_{PHL}					26			23		ns
t_{PLH}	Bus	Bus			15			15		ns
t_{PHL}					23			15		ns
t_{PLH}	Select, with bus input high†	Bus			36			33		ns
t_{PHL}					36			15		ns
t_{PLH}	Select, with bus input low†				27			26		ns
t_{PHL}					27			21		ns
t_{PZH}	Enable $\overline{G}$BA	A Bus			24			28		ns
t_{PZL}					35			39		ns
t_{PZH}	Enable GAB	B Bus			30			33		ns
t_{PZL}					38			42		ns
t_{PHZ}	Enable $\overline{G}$BA	A Bus	R_L = 667 Ω, C_L = 5 pF, See Note 2		23			23		ns
t_{PLZ}					19			19		ns
t_{PHZ}	Enable GAB	B Bus			23			23		ns
t_{PLZ}					22			22		ns

t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
t_{PHZ} ≡ output disable time from high level
t_{PLZ} ≡ output disable time from low level

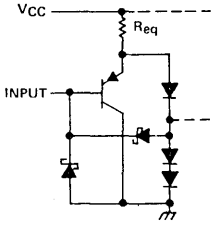
†These parameters are measured with the internal output state of the storage register opposite to that of the bus input.
NOTE 2: Load circuits and voltage waveforms are shown on page 3-11 of *The TTL Data Book for Design Engineers*, second edition.

schematics of inputs and outputs

EQUIVALENT OF GAB INPUTS

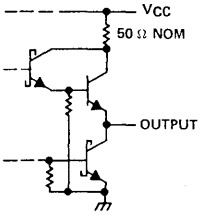


EQUIVALENT OF ALL OTHER INPUTS



A and B: R_{eq} = 15 kΩ NOM
$\overline{G}$BA, CAB and CBA: R_{eq} = 10 kΩ NOM
SAB and SBA: R_{eq} = 6 kΩ NOM

TYPICAL OF ALL OUTPUTS



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TYPES SN54LS668, SN54LS669, SN74LS668, SN74LS669
SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

D2351, APRIL 1977 – REVISED JANUARY 1981

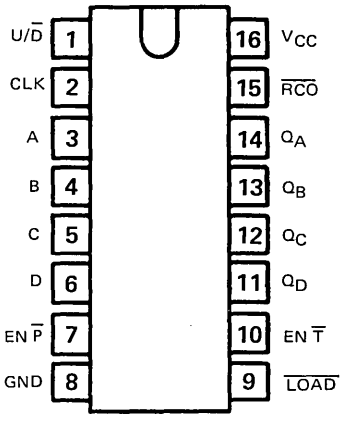
'LS668 . . . SYNCHRONOUS UP/DOWN DECADE COUNTERS
'LS669 . . . SYNCHRONOUS UP/DOWN BINARY COUNTERS

Programmable Look-Ahead Up/Down Binary/Decade Counters

- Fully Synchronous Operation for Counting and Programming
- Internal Look-Ahead for Fast Counting
- Carry Output for n-Bit Cascading
- Fully Independent Clock Circuit
- Buffered Outputs

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY		TYPICAL POWER DISSIPATION
	COUNTING UP	COUNTING DOWN	
'LS668, 'LS669	35 MHz	35 MHz	100 mW

SERIES SN54LS' . . . J OR W PACKAGE
SERIES SN74LS' . . . J OR N PACKAGE
(TOP VIEW)



2

description

These synchronous presettable counters feature an internal carry look-ahead for cascading in high-speed counting applications. The 'LS668 are decade counters and the 'LS669 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple-clock) counters. A buffered clock input triggers the four master-slave flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; that is, the outputs may each be preset to either level. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count enable inputs ($\overline{P}$ and $\overline{T}$) must be low to count. The direction of the count is determined by the level of the up/down input. When the input is high, the counter counts up; when low, it counts down. Input $\overline{T}$ is fed forward to enable the carry output. The carry output thus enabled will produce a low-level output pulse with a duration approximately equal to the high portion of the Q_A output when counting up and approximately equal to the low portion of the Q_A output when counting down. This low-level overflow carry pulse can be used to enable successive cascaded stages. Transitions at the enable $\overline{P}$ or $\overline{T}$ inputs are allowed regardless of the level of the clock input. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design.

These counters feature a fully independent clock circuit. Changes at control inputs (enable $\overline{P}$, enable $\overline{T}$, load, up/down) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

The 'LS668 and 'LS669 are completely new designs. Compared to the original 'LS168 and 'LS169, they feature 0-nanosecond minimum hold time, reduced input currents I_{IH} and I_{IL}, and all buffered outputs.

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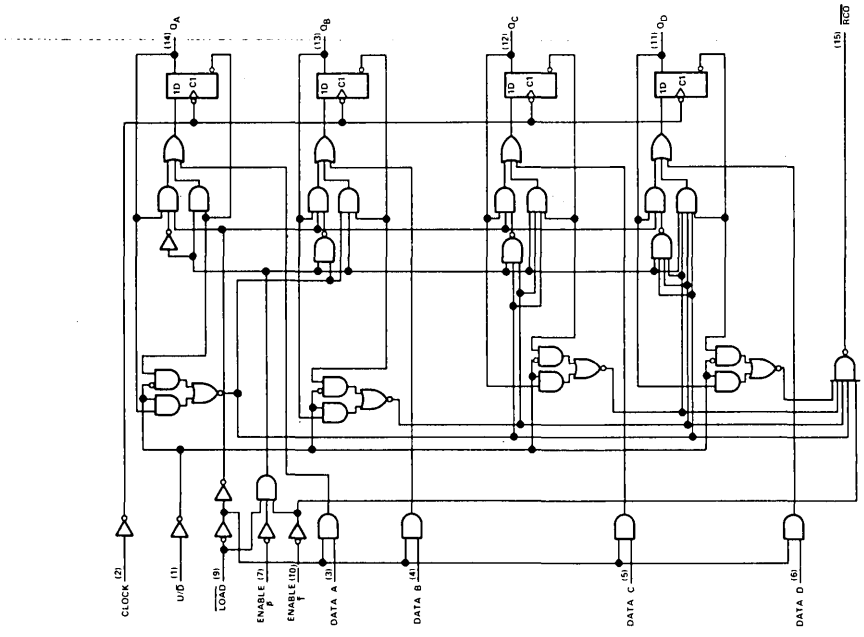
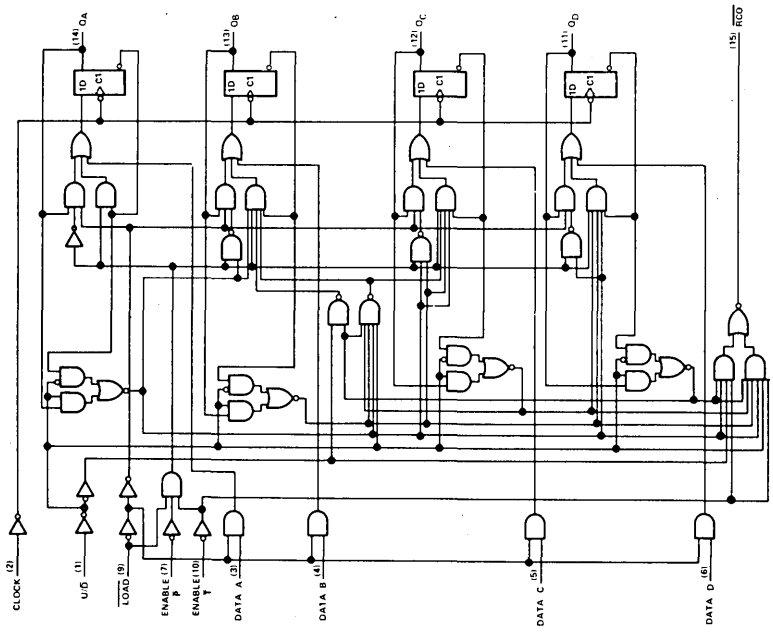
functional block diagrams

SN54LS669, SN74LS669, BINARY COUNTERS



SN54LS668, SN74LS668, DECADE COUNTERS



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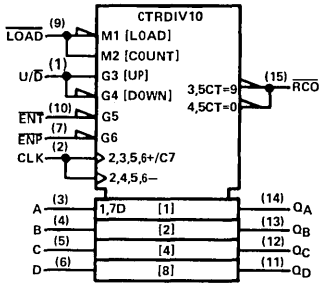
'LS668 DECADE COUNTERS

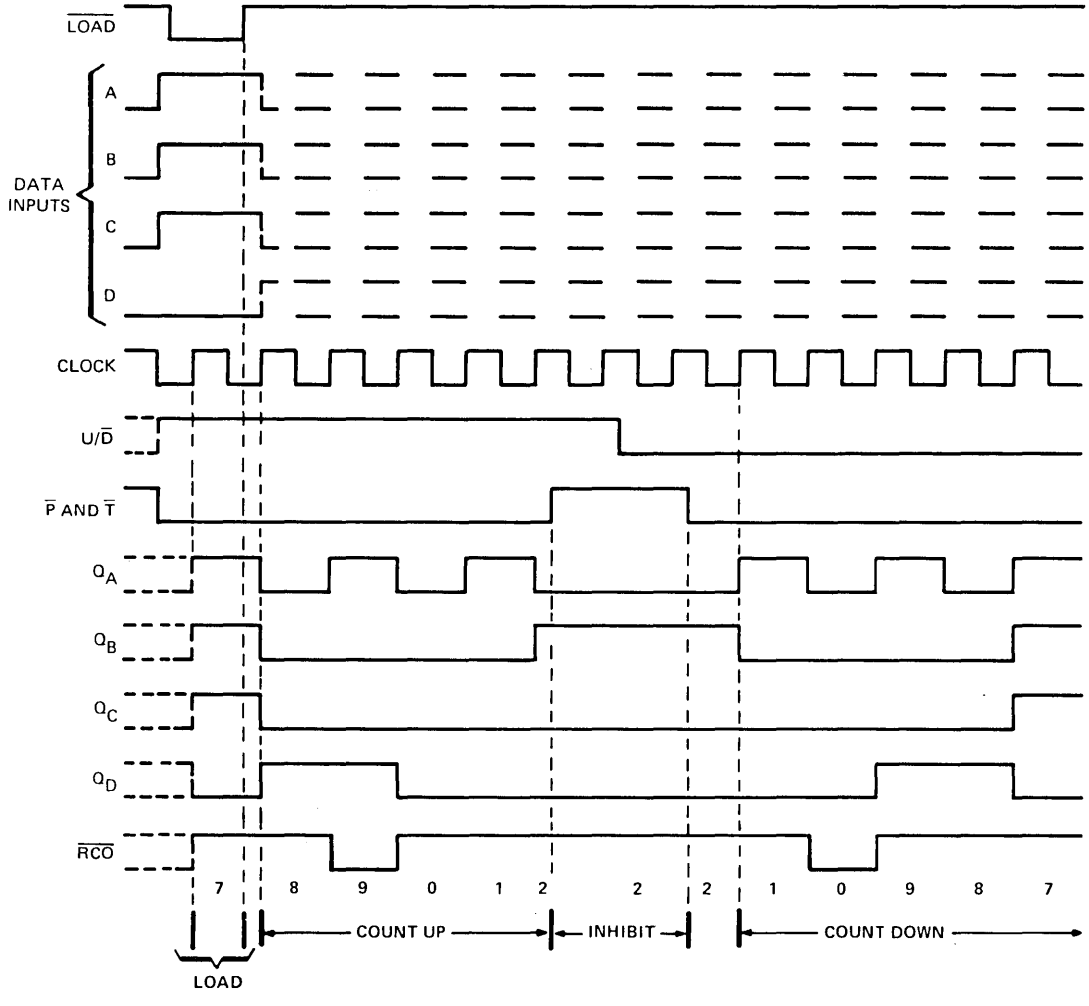
logic symbol



typical load, count, and inhibit sequences

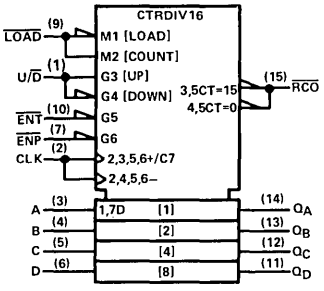
Illustrated below is the following sequence:

1. Load (preset) to BCD seven
2. Count up to eight, nine (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), nine, eight, and seven



'LS669 BINARY COUNTERS

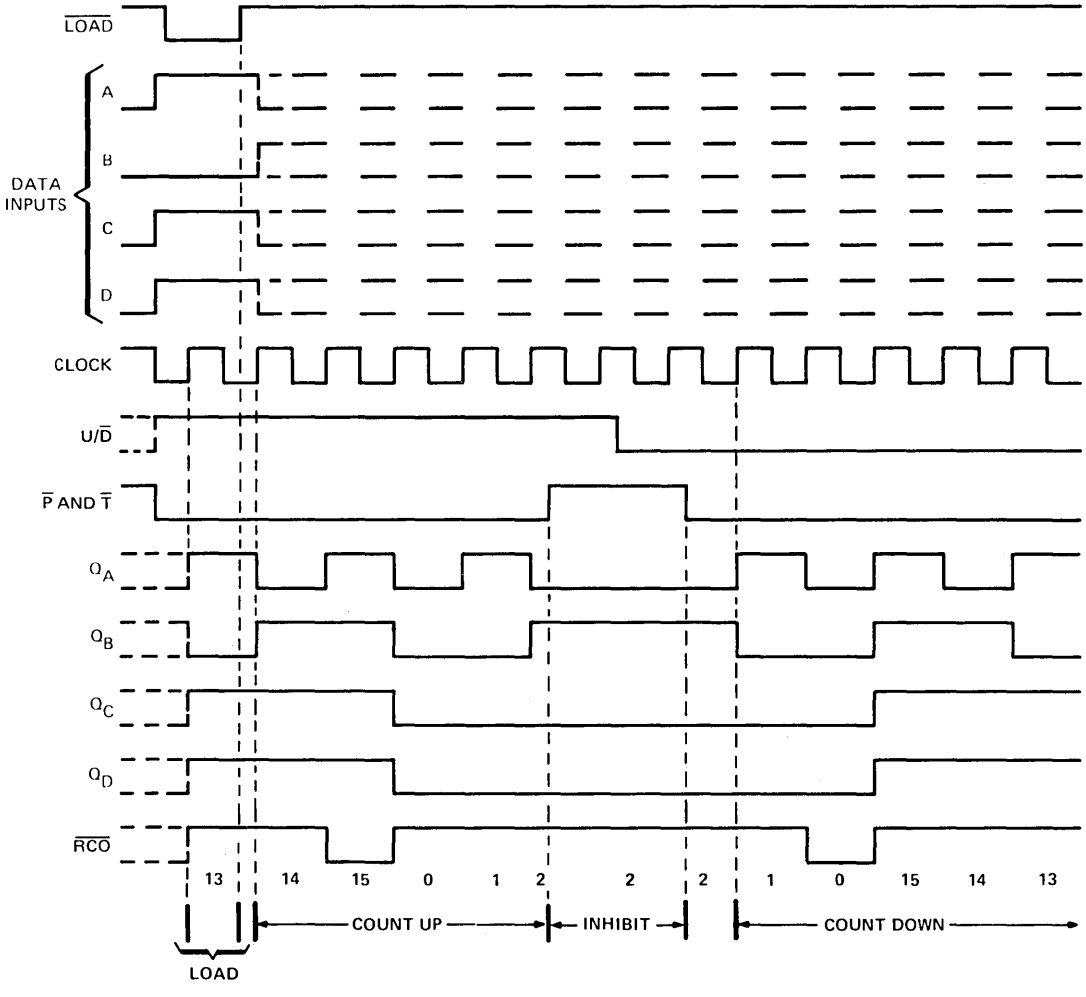
logic symbol



typical load, count, and inhibit sequences

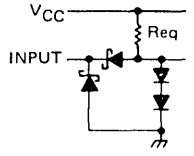
Illustrated below is the following sequence:

1. Load (preset) to binary thirteen
2. Count up to fourteen, fifteen (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen



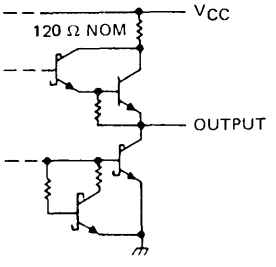
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



Load: R_{eq} = 10 kΩ NOM
Data: R_{eq} = 25 kΩ NOM
Clock, Enable $\overline{P}$, $\overline{T}$, U/$\overline{D}$: R_{eq} = 20 kΩ NOM

TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS668, SN54LS669 . . . . . −55°C to 125°C
SN74LS668, SN74LS669 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS668 SN54LS669			SN74LS668 SN74LS669			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−400			−400	μA
Low-level output current, I_{OL}				4			8	mA
Clock frequency, f_{clock}		0		25	0		25	MHz
Width of clock pulse, $t_{w(clock)}$ (high or low) (see Figure 1)		20			20			ns
Setup time, t_{su} (see Figure 1)	Data inputs A, B, C, D	20			20			ns
	Enable $\overline{P}$ or $\overline{T}$	35			35			
	$\overline{LOAD}$	25			25			
	U/$\overline{D}$	30			30			
Hold time at any input with respect to clock, t_h (see Figure 1)		0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS668 SN54LS669			SN74LS668 SN74LS669			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, I_{OH} = −400 μA	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	A, B, C, D, $\overline{P}$, U/$\overline{D}$	V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
		Clock, $\overline{T}$					0.1			0.1	
		$\overline{LOAD}$					0.2			0.2	
I_{IH}	High-level input current	A, B, C, D, $\overline{P}$, U/$\overline{D}$	V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
		Clock, $\overline{T}$					20			20	
		$\overline{LOAD}$					40			40	
I_{IL}	Low-level input current	A, B, C, D, $\overline{P}$, U/$\overline{D}$	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
		Clock, $\overline{T}$					−0.4			−0.4	
		$\overline{LOAD}$					−0.8			−0.8	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current		V_{CC} = MAX,	See Note 2		20	34		20	34	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 2: I_{CC} is measured after applying a momentary 4.5 V, then ground, to the clock input with all other inputs grounded and the outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			C_L = 15 pF, R_L = 2 kΩ, See Figures 2 and 3	25	32		MHz
t_{PLH}	Clock	$\overline{RCO}$			26	40	ns
t_{PHL}					40	60	
t_{PLH}	Clock	Any Q			18	27	ns
t_{PHL}					18	27	
t_{PLH}	Enable $\overline{T}$	$\overline{RCO}$			11	17	ns
t_{PHL}					29	45	
t_{PLH}◇	U/$\overline{D}$	$\overline{RCO}$			22	35	ns
t_{PHL}◇					26	40	

¶f_{max} ≡ Maximum clock frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output.
t_{PHL} ≡ propagation delay time, high-to-low-level output.
◇Propagation delay time from up/down to ripple carry must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum (0), the ripple carry output transition will be in phase. If the count is maximum (9 for 'LS668 or 15 for 'LS669), the ripple carry output will be out of phase.

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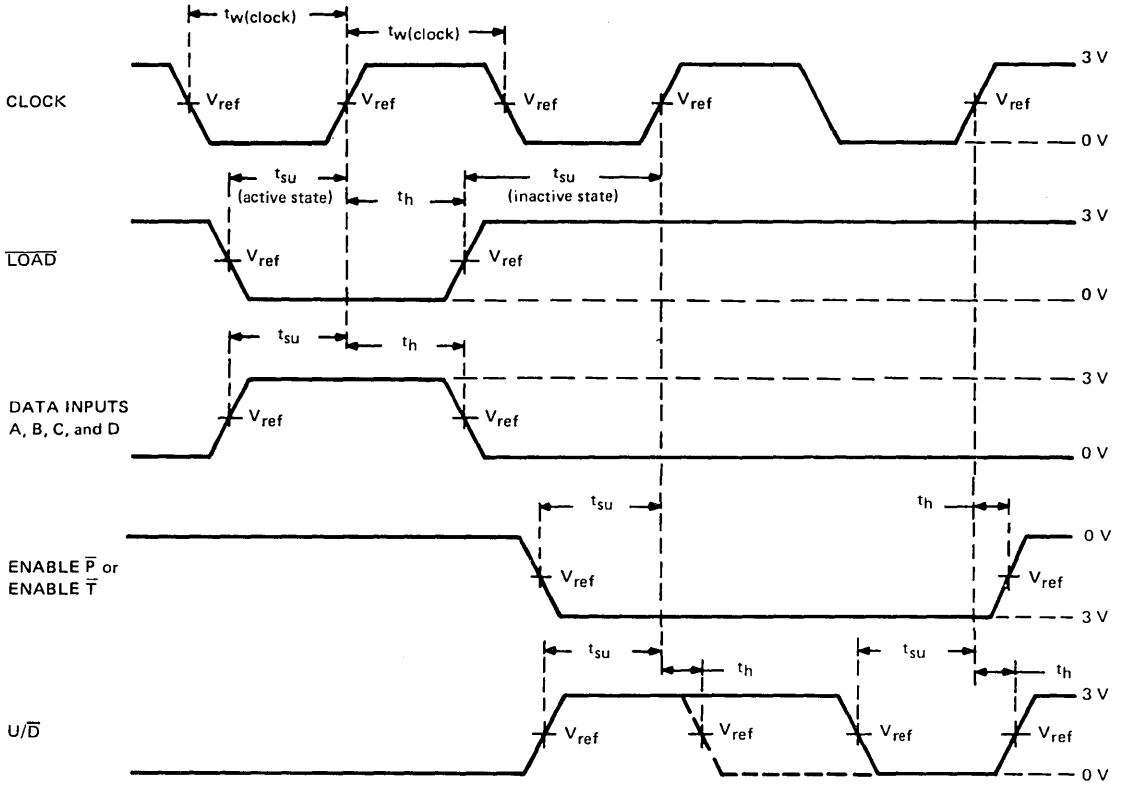
PARAMETER MEASUREMENT INFORMATION

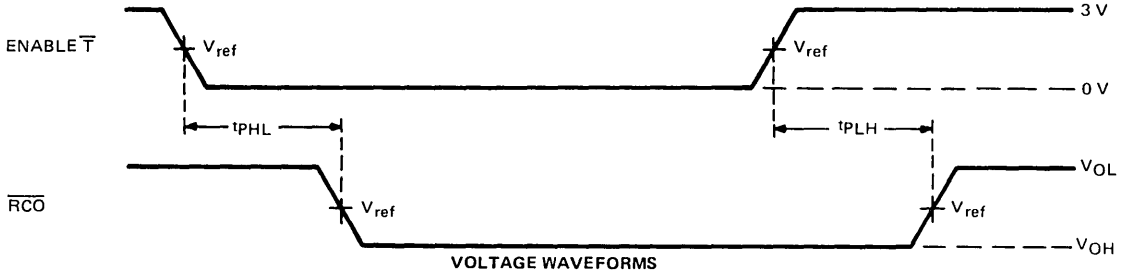


VOLTAGE WAVEFORMS

NOTES: A. The input pulses are supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$; $t_r \leq 15$ ns, $t_f \leq 6$ ns.

B. $V_{ref} = 1.3$ V.

FIGURE 1–PULSE WIDTHS, SETUP TIMES, HOLD TIMES



VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$; $t_r \leq 15$ ns, $t_f \leq 6$ ns.

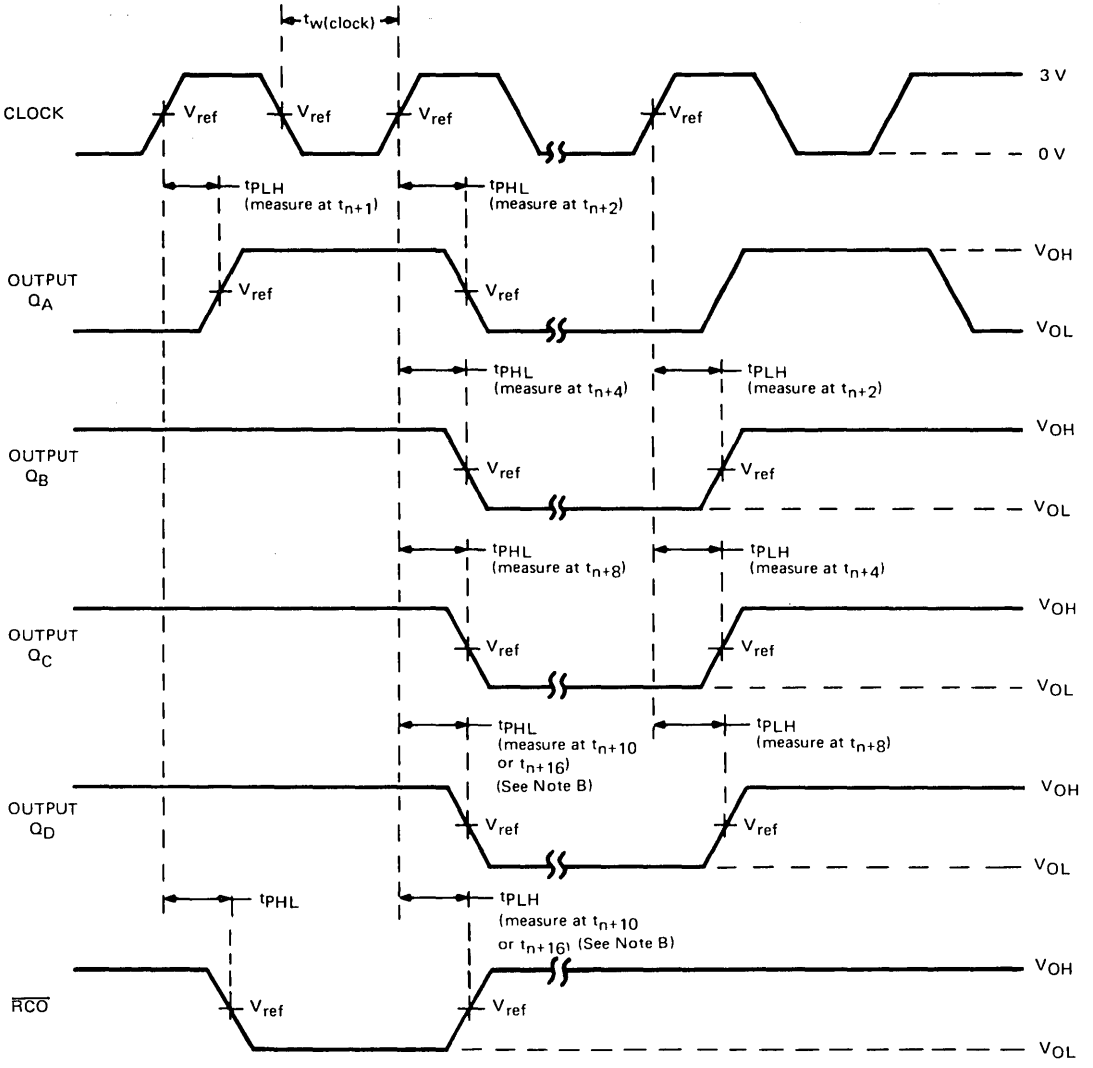
B. t_{PLH} and t_{PHL} from enable $\overline{T}$ input to ripple carry output assume that the counter is at the maximum count (Q_A and Q_D high for 'LS668, all Q outputs high for 'LS669).

C. $V_{ref} = 1.3$ V.

D. Propagation delay time from up/down to ripple carry must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum (0) the ripple carry output transition will be in phase. If the count is maximum (9 for 'LS668, or 15 for 'LS669) the ripple carry output will be out of phase.

FIGURE 2–PROPAGATION DELAY TIMES TO CARRY OUTPUT

PARAMETER MEASUREMENT INFORMATION



UP-COUNT VOLTAGE WAVEFORMS

NOTES: A. The input pulses are supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$, $t_r \leq 15$ ns, $t_f \leq 6$ ns. Vary PRR to measure f_{max}.
B. Outputs Q_D and carry are tested at t_{n+10} for the 'LS668, and at t_{n+16} for the 'LS669, where t_n is the bit-time when all outputs are low.
C. $V_{ref} = 1.3$ V.

FIGURE 3–PROPAGATION DELAY TIMES FROM CLOCK

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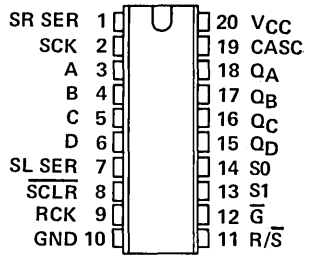
TYPES SN54LS671, SN54LS672, SN74LS671, SN74LS672
4-BIT UNIVERSAL SHIFT REGISTERS/LATCHES WITH 3-STATE OUTPUTS

D2638, JANUARY 1981

- 4-Bit Universal Shift Registers/Latches
- Multiplexed Outputs for Shift Register or Latched Data
- Choice of Direct SR Clear ('LS671) or Synchronous SR Clear ('LS672)
- 3-State Outputs Drive Bus Lines Directly
- Expandable to Any Word Length

SN54LS671, SN54LS672 . . J PACKAGE
SN74LS671, SN74LS672 . . J OR N PACKAGE



description

The 'LS671 and 'LS672 each contain a 4-bit universal shift register (similar to the 'LS194A) and a 4-bit storage register (similar to the 'LS175) multiplexed to a 3-state output stage (similar to the 'LS258). The user has the option of selecting the shift or storage register via the register/shift select input R/$\overline{S}$. The 'LS671 has a direct-overriding shift register clear while the 'LS672 features a synchronous shift register clear. The shift register has four distinct modes of operation, namely:

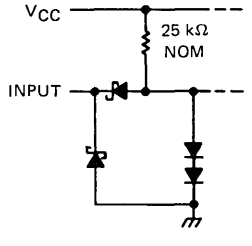
Inhibit clock (do nothing)
Shift right (in the direction Q_A toward Q_D)
Shift left (in the direction Q_D toward Q_A)
Parallel (broadside) load

A cascade output for the shift register is provided so that full shift register functionality is provided even while the outputs are in the high-impedance mode. The cascade output presents Q_A data in the shift-left mode, Q_D data in the shift-right mode.

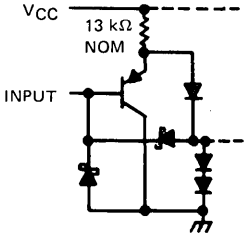
Both the shift register clock and the latch clock are triggered on the positive transition. The output control ($\overline{G}$) activates Q_A thru Q_D when low, it places Q_A thru Q_D into the high-impedance state when high.

schematics of inputs and outputs

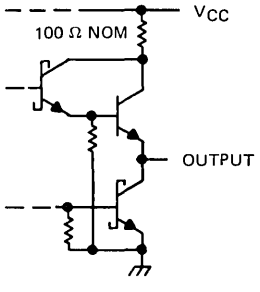
EQUIVALENT OF A THRU D, SL SER, AND SR SER INPUTS



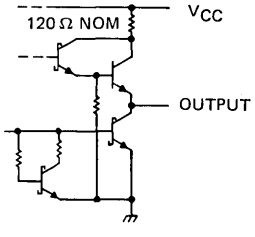
EQUIVALENT OF ALL OTHER INPUTS



TYPICAL OF Q_A THRU Q_D OUTPUTS



TYPICAL OF CASCADE OUTPUT



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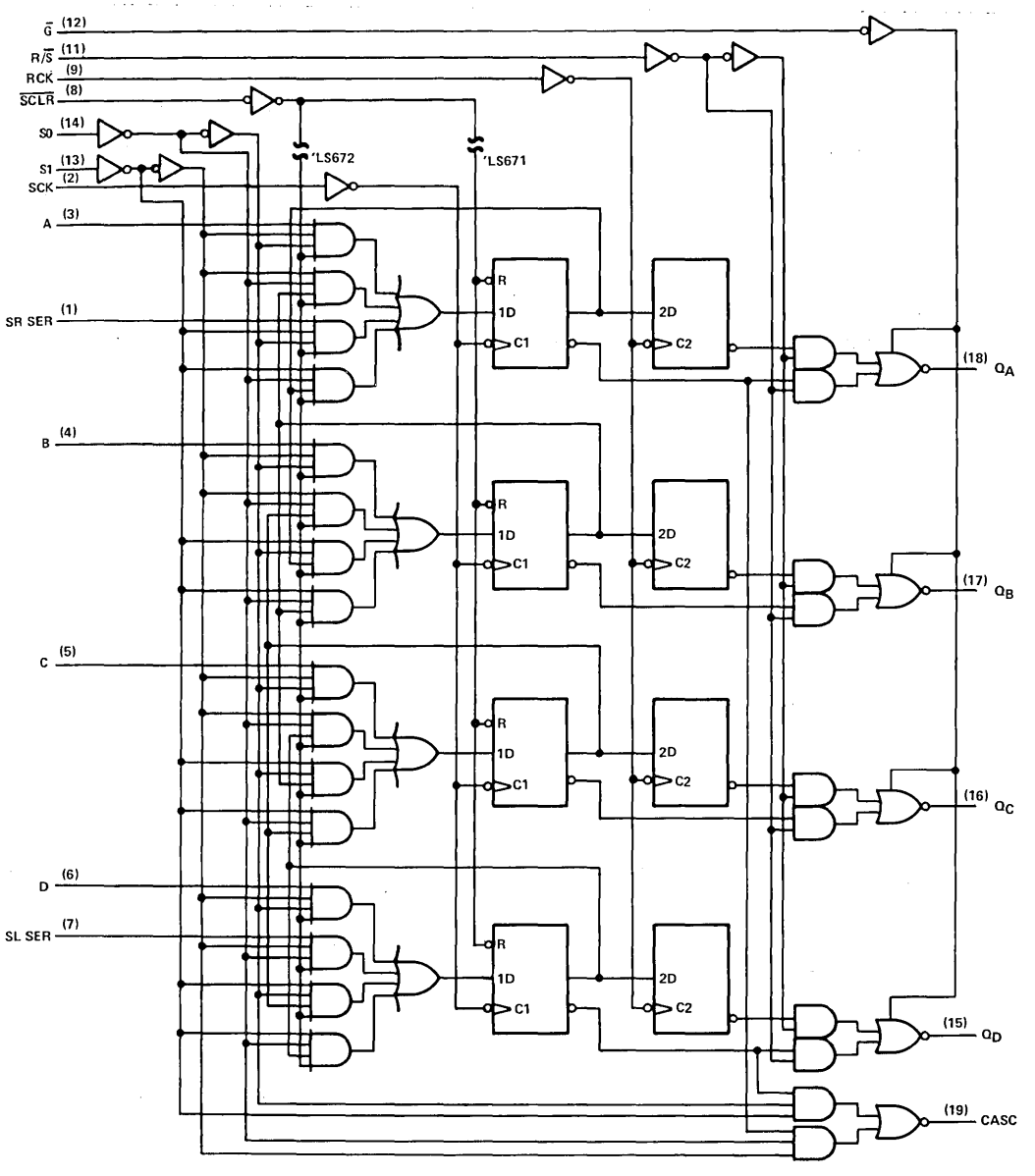
functional block diagram (positive logic)



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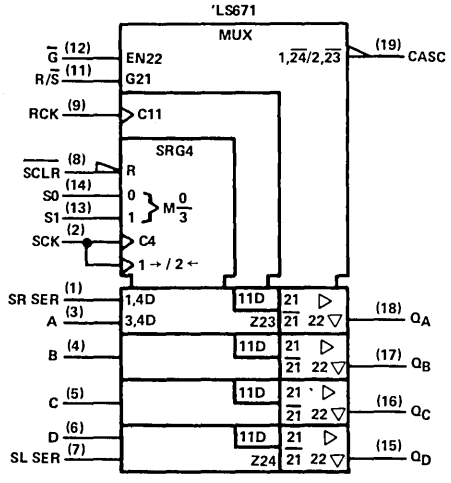
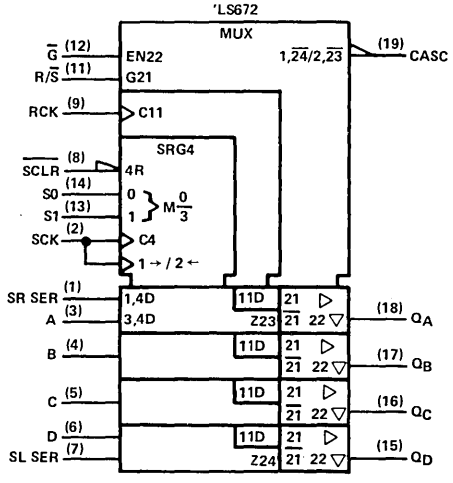
logic symbols





FUNCTION TABLE

			SR MODE		SCK		SERIAL INPUTS		PARALLEL INPUTS				PARALLEL OUTPUTS				
$\overline{G}$	R/$\overline{S}$	$\overline{SCLR}$	S1	S0	'LS671	'LS672	SL	SR	A	B	C	D	Q_A	Q_B	Q_C	Q_D	CASC*
L	L	L	X	X	X	↑	X	X	X	X	X	X	L	L	L	L	(*)
L	L	H	X	X	L	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	(*)
L	L	H	L	L	X	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	H
L	L	H	L	H	↑	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Cn}
L	L	H	L	H	↑	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Cn}
L	L	H	H	L	↑	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H	Q_{Bn}
L	L	H	H	L	↑	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L	Q_{Bn}
L	L	H	H	H	↑	↑	X	X	a	b	c	d	a	b	c	d	H
H	X	X	L	H	↑	↑	X	X	X	X	X	X	Z	Z	Z	Z	Q_{Cn}
H	X	X	H	L	↑	↑	X	X	X	X	X	X	Z	Z	Z	Z	Q_{Bn}
L	H	X	X	X	X	X	X	X	X	X	X	X	Internal register contents				(*)

When the output control $\overline{G}$ is high, the 3-state outputs are disabled to the high-impedance state; however, sequential operation of the shift register and the output at CASC are not affected.

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a, b, c, d = the level of steady-state input at A, B, C, or D, respectively
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established
Q_{An}, Q_{Bn}, Q_{Cn} = the level of Q_A, Q_B, or Q_C, respectively, before the most-recent transition of the clock
Z = high-impedance state
*The cascade output displays the D bit of the shift register in mode 1 (S1, S0 = L, H), the A bit in mode 2 (S1, S0 = HL), and is inactive (H) in modes 0 and 3 (S1, S0 = LL and HH).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54LS671, SN54LS672 . . . . . −55°C to 125°C
SN74LS671, SN74LS672 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	Cascade out			−0.4			−0.4	mA
	Q_A, Q_B, Q_C, Q_D			−1			−2.6	
Low-level output current, I_{OL}	Cascade out			4			8	mA
	Q_A, Q_B, Q_C, Q_D			12			24	
Width of SCK, RCK, or $\overline{SCLR}$ ('LS671 only) input pulse, t_w		30			30			ns
Setup time, t_{su}	S0 or S1 to SCK ↑	45			45			ns
	$\overline{SCLR}$ ↓ ('LS672 only) to SCK ↑	45			45			
	A, B, C, D to SCK ↑	30			30			
	SCK ↑ to RCK ↑	30			30			
	SER to SCK ↑	35			35			
Hold time, t_h	Any input from RCK ↑ or SCK ↑	0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	$Q_A - Q_D$	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OH} = −1 mA	2.4	3.1					V
		$Q_A - Q_D$		I_{OH} = −2.6 mA				2.4	3.1		
		CASC		I_{OH} = −400 μA	2.5	3.2		2.7	3.2		
V_{OL}	Low-level output voltage	$Q_A - Q_D$	V_{CC} = MIN, V_{IH} = 2 V	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		$Q_A - Q_D$		I_{OL} = 24 mA					0.35	0.5	
		CASC		I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
		CASC		I_{OL} = 8 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	$Q_A - Q_D$	V_{CC} = MAX, V_{IH} = 2 V,	V_O = 2.7 V, V_{IL} = V_{IL} max			20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied	$Q_A - Q_D$	V_{CC} = MAX, V_{IH} = 2 V,	V_O = 0.4 V, V_{IL} = V_{IL} max			−20			−20	μA
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current	A, B, C, D	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
		All others					−0.2			−0.2	
I_{OS}	Short-circuit output current§	$Q_A - Q_D$	V_{CC} = MAX,	V_O = 0 V	−30		−130	−30		−130	mA
		CASC			−20		−100	−20		−100	
I_{CC}	Supply current	All outputs low	V_{CC} = MAX, All outputs open	See Note 2		35	70		35	70	mA
		All outputs high		See Note 3		30	65		30	65	
		Q_A thru Q_D, at Hi-Z		See Note 4		37	70		37	70	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

NOTES: 2. I_{CCL} is tested after two 0-V to 4.5-V to 0-V pulses have been applied to SCK and RCK while S0 is at 4.5 V and all other inputs are grounded.

3. I_{CCH} is tested after two 4.5-V to 0-V to 4.5-V pulses have been applied to SCK and RCK while all other inputs are at 4.5 V.

4. I_{CCZ} is tested after two 0-V to 4.5-V to 0-V pulses have been applied to SCK and RCK while S0 and $\overline{G}$ are at 4.5 V and all other inputs are grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, see note 5

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS MODE	TEST CONDITIONS LOAD	'LS671 MIN	'LS671 TYP	'LS671 MAX	'LS672 MIN	'LS672 TYP	'LS672 MAX	UNIT
t_{PLH}	SCK ↑	CASCADE	SHIFT LEFT OR RIGHT	R_L = 2 kΩ, C_L = 15 pF		31	45		31	45	ns
t_{PHL}						14	25		14	25	
t_{PLH}	S0, S1					11	20		12	20	ns
t_{PHL}						11	20		12	20	
t_{PHL}	SCK ↑		SR CLEAR						19	30	ns
t_{PHL}	$\overline{SCLR}$ ↓					19	30				ns
t_{PLH}	SCK ↑	$Q_A - Q_D$	SHIFT LEFT OR RIGHT	R_L = 667 Ω, C_L = 45 pF		10	20		10	20	ns
t_{PHL}						16	25		16	25	
t_{PLH}			SR LOAD			10	20		10	20	ns
t_{PHL}						15	25		15	25	
t_{PHL}			SR CLEAR						17	30	ns
t_{PHL}	$\overline{SCLR}$ ↓					21	30				ns
t_{PLH}	RCK ↑		LATCH			10	20		10	20	ns
t_{PHL}						15	25		15	25	
t_{PLH}	R/$\overline{S}$ ↑		MUX			12	25		13	25	ns
t_{PHL}						15	25		15	25	
t_{PLH}	R/$\overline{S}$ ↓					17	25		17	25	ns
t_{PHL}						16	25		16	25	
t_{PZH}	$\overline{G}$ ↓		3-STATE ENABLE			16	25		16	25	ns
t_{PZL}						19	30		19	30	
t_{PHZ}	$\overline{G}$ ↑		3-STATE DISABLE	R_L = 667 Ω, C_L = 5 pF		16	25		16	25	ns
t_{PLZ}						16	25		16	25	

NOTE 5: Load circuit and voltage waveforms are shown on page 3-11 of *The TTL Data Book for Design Engineers*, Second Edition, LCC4112.

t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
t_{PZH} ≡ Output enable time to high level
t_{PZL} ≡ Output enable time to low level
t_{PHZ} ≡ Output disable time from high level
t_{PLZ} ≡ Output disable time from low level

TYPICAL APPLICATION DATA

The 'LS671 or 'LS672 can easily be expanded utilizing the cascade output and the SL SER and SR SER inputs. A typical expansion is shown below.

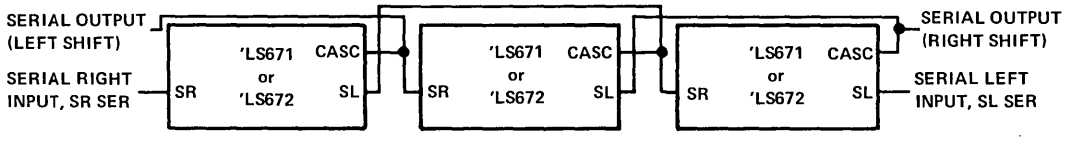

FIGURE 1 – 'LS671, 'LS672 EXPANDED TO 12 BITS, (3 PACKAGES)

Any desired word length may be obtained using the scheme shown. Corresponding control pins of all the packages are tied in common, i.e., all S0 pins are connected together, all S1 pins are connected together, etc.

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TYPES SN54LS673, SN54LS674, SN74LS673, SN74LS674
16-BIT SHIFT REGISTERS

D2421, JUNE 1978

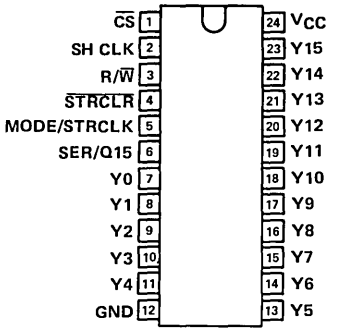
'LS673

- 16-Bit Serial-In, Serial-Out Shift Register with 16-Bit Parallel-Out Storage Register
- Performs Serial-to-Parallel Conversion

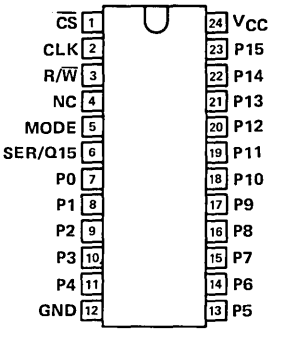
'LS674

- 16-Bit Parallel-In, Serial-Out Shift Register
- Performs Parallel-to-Serial Conversion

SN54LS673 . . . J OR W PACKAGE
SN74LS673 . . . J OR N PACKAGE
(TOP VIEW)



SN54LS674 . . . J OR W PACKAGE
SN74LS674 . . . J OR N PACKAGE
(TOP VIEW)



NC — No internal connection

description

SN54LS673, SN74LS673

The 'LS673 is a 16-bit shift register and a 16-bit storage register in a single 24-pin package. A three-state input/output (SER/Q15) port to the shift register allows serial entry and/or reading of data. The storage register is connected in a parallel data loop with the shift register and may be asynchronously cleared by taking the store-clear input low. The storage register may be parallel loaded with shift-register data to provide shift-register status via the parallel outputs. The shift register can be parallel loaded with the storage-register data upon command.

A high logic level at the chip-select ($\overline{CS}$) input disables both the shift-register clock and the storage-register clock and places SER/Q15 in the high-impedance state. The store-clear function is not disabled by the chip select.

Caution must be exercised to prevent false clocking of either the shift register or the storage register via the chip-select input. The shift clock should be low during the low-to-high transition of chip select and the store clock should be low during the high-to-low transition of chip select.

SN54LS674, SN74LS674

The 'LS674 is a 16-bit parallel-in, serial-out shift register. A three-state input/output (SER/Q15) port provides access for entering serial data or reading the shift-register word in a recirculating loop.

The device has four basic modes of operation:

1) Hold (do nothing)
2) Write (serially via input/output)
3) Read (serially)
4) Load (parallel via data inputs)

Low-to-high-level changes at the chip select input should be made only when the clock input is low to prevent false clocking.

'LS673

FUNCTION TABLE

INPUTS					SER/ Q15	SHIFT REGISTER FUNCTIONS				STORAGE REGISTER FUNCTIONS	
$\overline{CS}$	R/$\overline{W}$	SH CLK	$\overline{STRCLR}$	MODE/ STRCLK		SHIFT	READ FROM SERIAL OUTPUT	WRITE INTO SERIAL INPUT	PARALLEL LOAD	CLEAR	LOAD
H	X	X	X	X	Z	NO	NO	NO	NO		NO
X	X	X	L	X						YES	
L	L	↓	X	X	Z	YES	NO	YES	NO		
L	H	X	X	X	Q15		YES	NO			NO
L	H	↓	X	L	Q14n	YES	YES	NO	NO		NO
L	H	↓	L	H	L	NO	YES		YES	YES	NO
L	H	↓	H	H	Y15n	NO	YES		YES	NO	NO
L	L	X	H	↑	Z		NO		NO	NO	YES

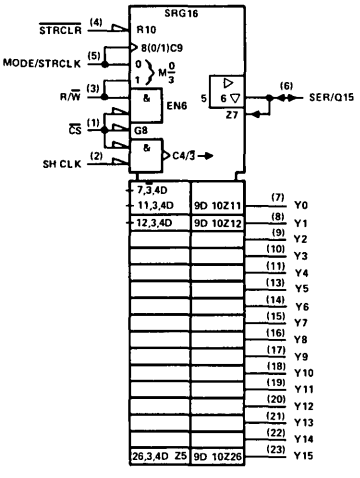
logic symbols

'LS674 FUNCTION TABLE

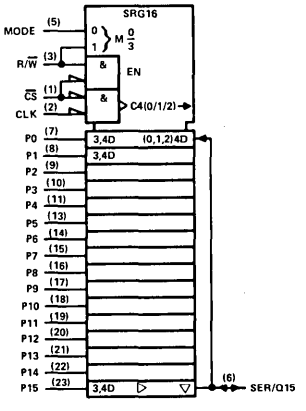
INPUTS				SER/ Q15	OPERATION
$\overline{CS}$	R/$\overline{W}$	MODE	CLK		
H	X	X	X	Z	Do nothing
L	L	X	↓	Z	Shift and write (serial load)
L	H	L	↓	Q14n	Shift and read
L	H	H	↓	P15	Parallel load

H = high level (steady state)
L = low level (steady state)
↑ = transition from low to high level
↓ = transition from high to low level
X = irrelevant (any input including transitions)
Z = high impedance, input mode
Q14n = content of 14th bit of the shift register before the most recent ↓ transition of the clock.
Q15 = present content of 15th bit of the shift register
Y15n = content of the 15th bit of the storage register before the most recent ↓ transition of the clock.
P15 = level of input P15

'LS673

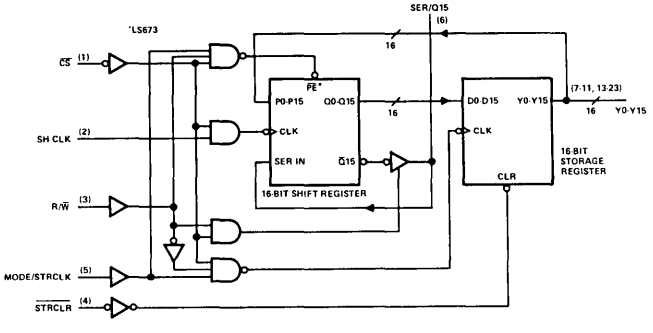


'LS674

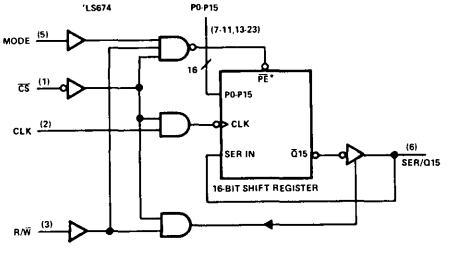


functional block diagrams

SN54LS673, SN74LS673



SN54LS674, SN74LS674



*When $\overline{PE}$ is low, data is synchronously parallel loaded into the shift registers from the 16 P inputs and no shifting takes place.

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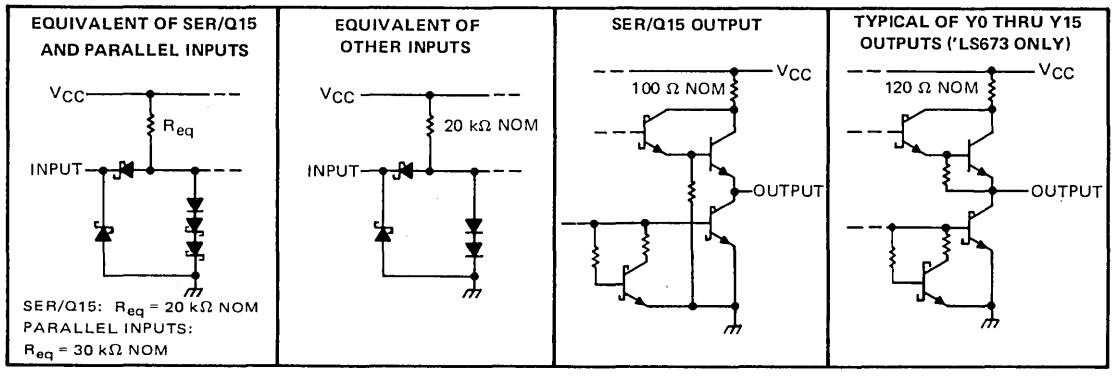
schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

2

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: SER/Q15 . . . . . 5.5 V
All others . . . . . 7 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54LS673, SN54LS674 . . . . . −55°C to 125°C
SN74LS673, SN74LS674 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1. Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	SER/Q15			−1			−2.6	mA
	Y0 thru Y15			−0.4			−0.4	
Low-level output current, I_{OL}	SER/Q15			12			24	mA
	Y0 thru Y15			4			8	
Clock frequency, f_{clock}		0		20	0		20	MHz
Width of clock input pulse, $t_{w(clock)}$		20			20			ns
Width of clear input pulse, $t_{w(clear)}$		20			20			ns
Setup time, t_{su}	SER/Q15	20			20			ns
	P0 thru P15	20			20			
	Mode	35			35			
	R/$\overline{W}$, $\overline{CS}$	35			35			
Hold time, t_h	SER/Q15	0			0			ns
	P0 thru P15	0			0			
	Mode	0			0			
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS' MIN	SN54LS' TYP‡	SN54LS' MAX	SN74LS' MIN	SN74LS' TYP‡	SN74LS' MAX	UNIT
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	SER/Q15	V_{CC} = MIN,	V_{IH} = 2 V,	2.4	3.2		2.4	3.1		V
		Y0 thru Y15¶	V_{IL} = V_{IL}max,	I_{OH} = MAX	2.5	3.4		2.7	3.4		
V_{OL}	Low-level output voltage	SER/Q15	V_{CC} = MIN, V_{IH} = 2 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
		Y0 thru Y15¶	V_{IL} = V_{IL}max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
				I_{OL} = 8 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	SER/Q15	V_{CC} = MAX, V_{IL} = V_{IL}max,	V_{IH} = 2 V, V_O = 2.7 V			40			40	μA
I_{OZL}	Off-state output current, low-level voltage applied	SER/Q15	V_{CC} = MAX, V_{IL} = V_{IL}max,	V_{IH} = 2 V, V_O = 0.4 V			−400			−400	μA
I_I	Input current at maximum input voltage	SER/Q15	V_{CC} = MAX	V_I = 5.5 V			0.1			0.1	mA
		Others		V_I = 7 V			0.1			0.1	
I_{IH}	High-level input current	SER/Q15	V_{CC} = MAX,	V_I = 2.7 V			40			40	μA
		Others					20			20	
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	SER/Q15	V_{CC} = MAX		−30		−130	−30		−130	mA
		Y0 thru Y15¶			−20		−100	−20		−100	
I_{CC}	Supply current	'LS673	V_{CC} = MAX			50	80		52	80	mA
		'LS674				25	40		25	40	

†For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.
¶'LS673 only.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, see note 2

PARAMETER	'LS673 FROM	'LS673 TO	'LS674 FROM	'LS674 TO	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	SH CLK	SER/Q15	CLK	SER/Q15	R_L = 667 Ω, C_L = 45 pF	20	28		MHz
t_{PHL}	$\overline{STRCLR}$	Y0 thru Y15			R_L = 2 kΩ, C_L = 15 pF		25	40	ns
t_{PLH}	MODE/ STRCLK	Y0 thru Y15					28	45	
t_{PHL}							30	45	
t_{PLH}	SH CLK	SER/Q15	CLK	SER/Q15	R_L = 667 Ω, C_L = 45 pF		21	33	ns
t_{PHL}							26	40	
t_{PZH}	$\overline{CS}$, R/$\overline{W}$	SER/Q15	$\overline{CS}$, R/$\overline{W}$	SER/Q15	R_L = 667 Ω, C_L = 45 pF		30	45	ns
t_{PZL}							30	45	
t_{PHZ}	$\overline{CS}$, R/$\overline{W}$	SER/Q15	$\overline{CS}$, R/$\overline{W}$	SER/Q15	R_L = 667 Ω, C_L = 5 pF		25	40	ns
t_{PLZ}							25	40	

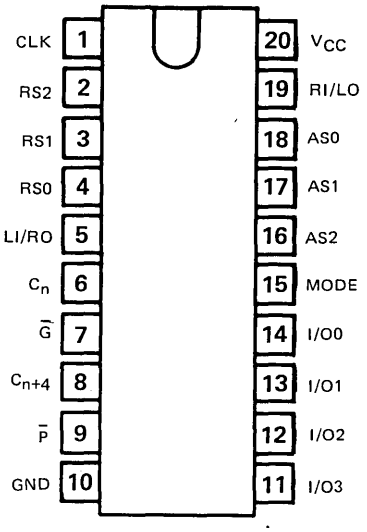
NOTE 2: For load circuit and voltage waveforms see page 3-11 of *"The TTL Data Book for Design Engineers"*, second edition.
f_{max} ≡ maximum clock frequency
t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
t_{PZH} ≡ Output enable time to high level
t_{PZL} ≡ Output enable time to low level
t_{PHZ} ≡ Output disable time from low level
t_{PLZ} ≡ Output disable time from high level

TYPES SN54LS681, SN74LS681
4-BIT PARALLEL BINARY ACCUMULATORS

D2422, JANUARY 1981

- Full 4-Bit Binary Accumulator in a Single 20-Pin Package
- Contains Two Synchronous Registers:
  Word A
  Word B Shift/Accumulator
- 16 Arithmetic Operations Including B Minus A and A Minus B
- 16 Logic-Mode Operations
- Expandable to Handle N-Bit Words with Full Carry Look-Ahead
- Bus Driving I/O Ports

SN54LS681 . . . J PACKAGE
SN74LS681 . . . J OR N PACKAGE
(TOP VIEW)



description

These low-power Schottky IC's integrate a high-speed arithmetic logic unit (ALU) complete with word A and word B registers on a single chip. The ALU performs 16 arithmetic and 16 logic functions (see Tables 1 and 2). Full carry look-ahead is provided for fast carry of four-bit words. The carry input (C_n) and propagate and generate outputs ($\overline{P}$ and $\overline{G}$) are provided for direct use with SN54S182/SN74S182 carry look-ahead generators for optimum performance with longer words.

The A and B registers are controlled by three inputs (RS0, RS1, and RS2). These pins define eight distinct register modes (see Table 3). The A register is a simple storage register while the B register is a combination storage/shift/accumulator register. The contents of the A and B registers provide the A and B words for the ALU.

Four I/O ports (I/O 0 thru I/O 3) are provided for parallel loading of word A and/or word B into their respective registers. These same ports also serve as bus driving outputs for the ALU/accumulator results (F_j). Two additional I/O ports (RI/LO and LI/RO) are provided to allow expansion of the accumulator for words greater than four bits in length.

The A or B register can be parallel loaded from the four I/O ports. The B register can also be parallel loaded from the ALU as an accumulator register and in addition, the B register can be serially loaded from either the RI/LO or the LI/RO ports.

The SN54LS681 is characterized for operation over the full military temperature range from −55°C to 125°C. The SN74LS681 is characterized for operation from 0°C to 70°C.

PRODUCT PREVIEW
This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

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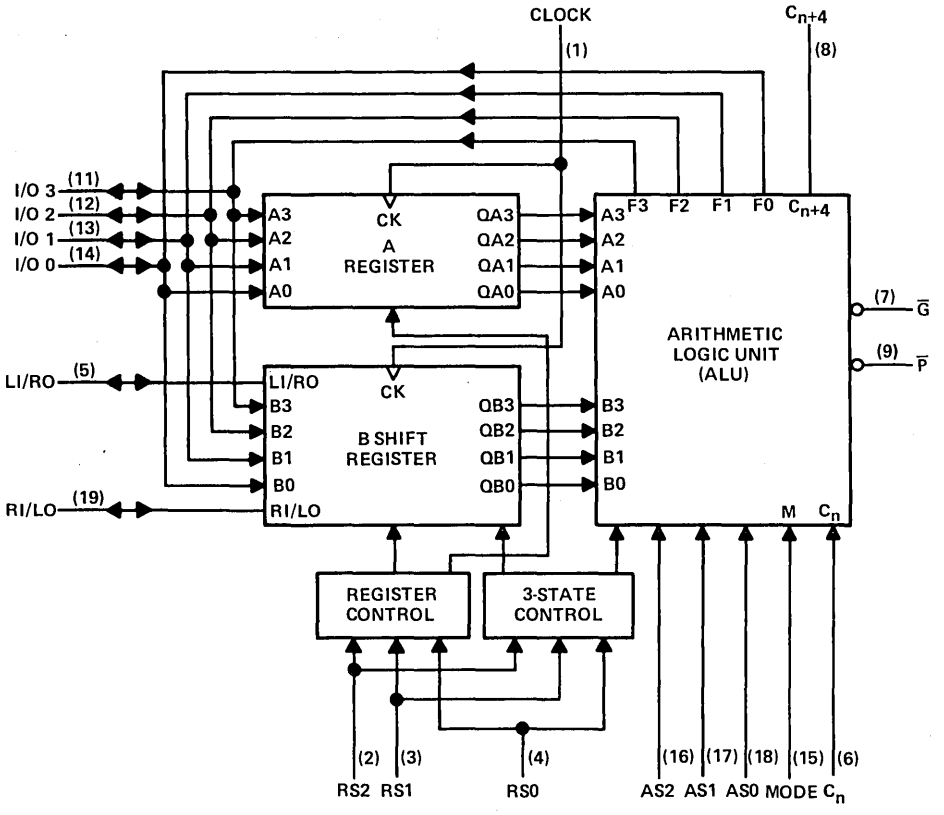
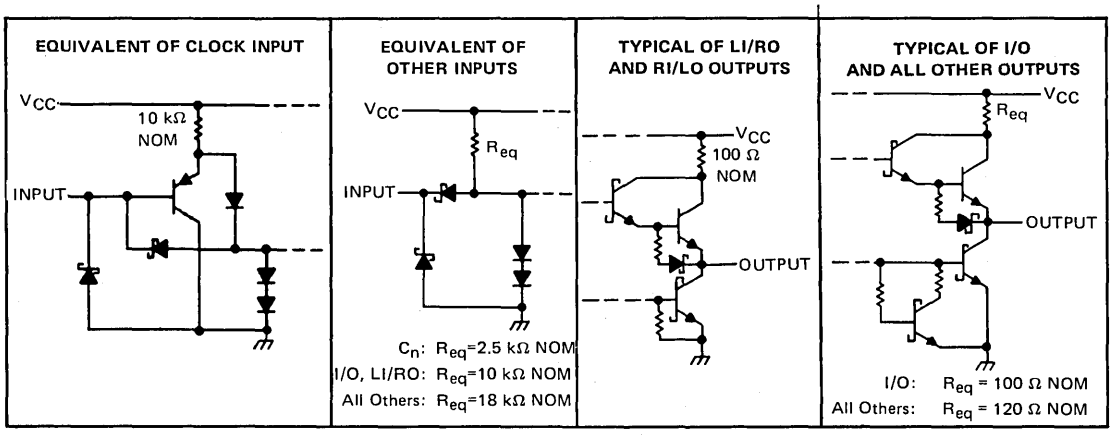
functional block diagram



schematics of inputs and outputs



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FUNCTION TABLES

TABLE 1 – ARITHMETIC FUNCTIONS

Mode Control (M) = Low

ALU SELECTION			ACTIVE-HIGH DATA	
			C_n = H	C_n = L
AS2	AS1	AS0	(with carry)	(no carry)
L	L	L	F_j = L	F_j = H
L	L	H	F = B MINUS A	F = B MINUS A MINUS 1
L	H	L	F = A MINUS B	F = A MINUS B MINUS 1
L	H	H	F = A PLUS B PLUS 1	F = A PLUS B
H	L	L	F = B PLUS 1	$F_j = B_j$
H	L	H	F = $\overline{B}$ PLUS 1	$F_j = \overline{B_j}$
H	H	L	F = A PLUS 1	$F_j = A_j$
H	H	H	F = $\overline{A}$ PLUS 1	$F_j = \overline{A_j}$

TABLE 2 – LOGIC FUNCTIONS

Mode Control (M) = High

ALU SELECTION			ACTIVE-HIGH DATA	
			C_n = H	C_n = L
AS2	AS1	AS0	(with carry)	(no carry)
L	L	L	F_0 = H, $F_1 = F_2 = F_3$ = L	F_j = L
L	L	H	$F_j = A_j \oplus B_j$ PLUS 1	$F_j = A_j \oplus B_j$
L	H	L	$F_j = \overline{A_j \oplus B_j}$ PLUS 1	$F_j = \overline{A_j \oplus B_j}$
L	H	H	F_j = L	F_j = H
H	L	L	$F_j = A_jB_j$ PLUS 1	$F_j = A_jB_j$
H	L	H	$F_j = \overline{A_j + B_j}$ PLUS 1	$F_j = \overline{A_j + B_j}$
H	H	L	$F_j = \overline{A_jB_j}$ PLUS 1	$F_j = \overline{A_jB_j}$
H	H	H	$F_j = A_j + B_j$ PLUS 1	$F_j = A_j + B_j$

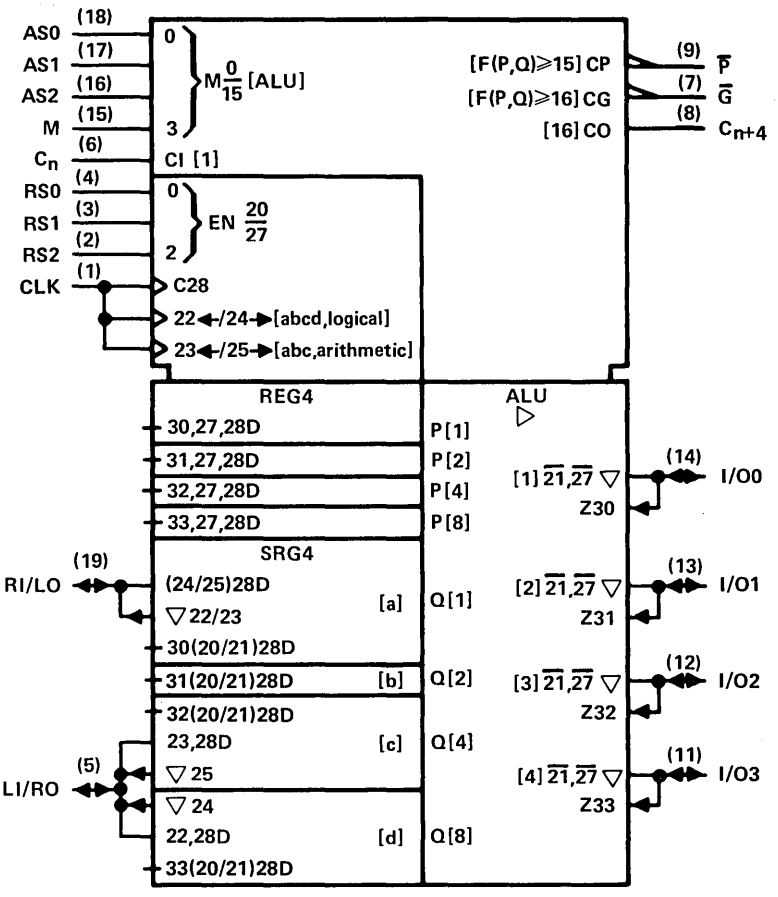
2

TABLE 3 – REGISTER FUNCTIONS

FUNCTION	INPUTS BEFORE L TO H CLOCK TRANSITION								INTERNAL OUTPUTS AFTER L TO H CLOCK TRANSITION											
	REGISTER SELECTION			DATA INPUTS						A REGISTER				B SHIFT REGISTER						ALU			
	RS2	RS1	RS0	LI/RO	I/O 3	I/O 2	I/O 1	I/O 0	RI/LO	QA3	QA2	QA1	QA0	LI/RO	QB3	QB2	QB1	QB0	RI/LO	F3	F2	F1	F0
ACCUM	L	L	L	Z	F3	F2	F1	F0	Z	$QA3_0$	$QA2_0$	$QA1_0$	$QA0_0$	Z	$F3_n$	$F2_n$	$F1_n$	$F0_n$	Z	F3	F2	F1	F0
LOAD B	L	L	H	Z	b3	b2	b1	b0	Z	$QA3_0$	$QA2_0$	$QA1_0$	$QA0_0$	Z	b3	b2	b1	b0	Z	Z	Z	Z	Z
LEFT SHIFT LOGICAL	L	H	L	li	F3	F2	F1	F0	QB0	$QA3_0$	$QA2_0$	$QA1_0$	$QA0_0$	li	li	$QB3_n$	$QB2_n$	$QB1_n$	$QB1_n$	F3	F2	F1	F0
LEFT SHIFT ARITH	L	H	H	li	F3	F2	F1	F0	QB0	$QA3_0$	$QA2_0$	$QA1_0$	$QA0_0$	li	$QB3_n$	li	$QB2_n$	$QB1_n$	$QB1_n$	F3	F2	F1	F0
RIGHT SHIFT LOGICAL	H	L	L	QB3	F3	F2	F1	F0	ri	$QA3_0$	$QA2_0$	$QA1_0$	$QA0_0$	$QB2_n$	$QB2_n$	$QB1_n$	$QB0_n$	ri	ri	F3	F2	F1	F0
RIGHT SHIFT ARITH	H	L	H	QB2	F3	F2	F1	F0	ri	$QA3_0$	$QA2_0$	$QA1_0$	$QA0_0$	$QB1_n$	$QB3_n$	$QB1_n$	$QB0_n$	ri	ri	F3	F2	F1	F0
HOLD	H	H	L	Z	F3	F2	F1	F0	Z	$QA3_0$	$QA2_0$	$QA1_0$	$QA0_0$	Z	$QB3_0$	$QB2_0$	$QB1_0$	$QB0_0$	Z	$F3_0$	$F2_0$	$F1_0$	$F0_0$
LOAD A	H	H	H	Z	a3	a2	a1	a0	Z	a3	a2	a1	a0	Z	$QB3_0$	$QB2_0$	$QB1_0$	$QB0_0$	Z	Z	Z	Z	Z

H = high level (steady state)
L = low level (steady state)
Z = high impedance (output off)
a0 . . . a3, b0 . . . b3 = the level of steady-state condition at I/O 0 thru I/O 3, respectively and intended as A or B input data
F0 . . . F3 = internal ALU results
$QA0_0 \ldots QB0_0$, $F0_0 \ldots F3_0$ = the level of QA0 thru QB3 and F0 thru F3, respectively, before the indicated steady-state input conditions were established
$QA0_n \ldots QB3_n$ = the level of QA0 thru QB3 before the most recent ↑ transition of the clock
ri, li = the level of steady-state conditions at RI/LO or LI/RO, respectively

logic symbol



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS681	−55°C to 125°C
SN74LS681	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

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recommended operating conditions

		SN54LS681			SN74LS681			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	LI/RO, I/O, RI/LO			−1			−2.6	mA
	$\overline{P}$, $\overline{G}$, C_{n+4}			−400			−400	μA
Low-level output current, I_{OL}	I/O			12			24	mA
	C_{n+4}, LI/RO, RI/LO			4			8	
	$\overline{P}$			8			8	
	$\overline{G}$			16			16	
Clock frequency, f_{clock}		0		20	0		20	MHz
Width of clock pulse, $t_{w(clock)}$		25			25			ns
Setup time, t_{su}	RS0-RS2 to CLK↑	30			30			ns
	Data I/O to CLK↑	25			25			
Hold time, t_h		0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS681			SN74LS681			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage	C_n					0.7			0.7	V
		All others					0.7			0.8	
V_{IK}	Input clamp voltage		V_{CC}=MIN, I_I=−18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	All I/O	V_{CC}=MIN, V_{IH}=2 V, V_{IL}=V_{IL} max, I_{OH}=MAX		2.4	3.1		2.4	3.2		V
		$\overline{P}$, $\overline{G}$, C_{n+4}			2.5	3.4		2.7	3.4		
V_{OL}	Low-level output voltage	I/O	V_{CC}=MAX, V_{IH}=2 V, V_{IL}=V_{IL} max	I_{OL}=12 mA		0.25	0.4		0.25	0.4	V
				I_{OL}=24 mA					0.35	0.5	
		LI/RO, RI/LO, C_{n+4}		I_{OL}=4 mA		0.25	0.4		0.25	0.4	
				I_{OL}=8 mA					0.35	0.5	
		$\overline{P}$		I_{OL}=8 mA		0.35	0.5		0.35	0.5	
		$\overline{G}$		I_{OL}=16 mA		0.35	0.5		0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	I/O, LI/RO, RI/LO	V_{CC}=MAX, V_{IH}=2 V, V_{IL}=V_{IL} max, V_O=2.7 V				40			40	μA
I_{OZL}	Off-state output current, low-level voltage applied	I/O, LI/RO	V_{CC}=MAX, V_{IH}=2 V, V_{IL}=V_{IL} max, V_O=0.4 V				−800			−800	μA
		RI/LO					−400			−400	
I_I	Input current at maximim input voltage	All I/O	V_{CC}=MAX	V_I=5.5 V			0.1			0.1	mA
		C_n		V_I=7 V			0.5			0.5	
		All others					0.1			0.1	
I_{IH}	High-level input current	C_n	V_{CC}=MAX, V_I=2.7 V				100			100	μA
		All I/O					40			40	
		All others					20			20	
I_{IL}	Low-level input current	C_n	V_{CC}=MAX, V_I=0.4 V				−4			−4	mA
		I/O, LI/RO					−0.8			−0.8	
		CLK					−0.2			−0.2	
		All others					−0.4			−0.4	
I_{OS}	Short-circuit output current§	I/O	V_{CC}=MAX		−30		−130	−30		−130	mA
		LI/RO, RI/LO, $\overline{P}$, $\overline{G}$, C_{n+4}			−20		−100	−20		−100	
I_{CC}	Supply current		V_{CC}=MAX, RS0 at 4.5 V, All other I/O at 0 V			100			100		mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operations.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	CLOCK↑	$\overline{P}$	R_L = 667 Ω,	C_L = 45 pF		23		ns
t_{PHL}						30		
t_{PLH}		$\overline{G}$				25		ns
t_{PHL}						26		
t_{PLH}		I/O				24		ns
t_{PHL}						27		
t_{PLH}		C_{n+4}	R_L = 2 kΩ,	C_L = 15 pF		36		ns
t_{PHL}						34		
t_{PLH}		LI/RO				25		ns
t_{PHL}						24		
t_{PLH}		RI/LO				19		ns
t_{PHL}						19		
t_{PLH}	AS0-AS2	$\overline{P}$	R_L = 667 Ω,	C_L = 45 pF		27		ns
t_{PHL}						28		
t_{PLH}		$\overline{G}$				25		ns
t_{PHL}						27		
t_{PLH}		I/O				28		ns
t_{PHL}						27		
t_{PLH}		C_{n+4}	R_L = 2 kΩ,	C_L = 15 pF		41		ns
t_{PHL}						36		
t_{PLH}	C_n	$\overline{P}$	R_L = 667 Ω,	C_L = 45 pF		9		ns
t_{PHL}						9		
t_{PLH}		I/O				15		ns
t_{PHL}						13		
t_{PLH}		C_{n+4}	R_L = 2 kΩ,	C_L = 15 pF		21		ns
t_{PHL}						19		
t_{PLH}	MODE	$\overline{P}$	R_L = 667 Ω,	C_L = 45 pF		25		ns
t_{PHL}						27		
t_{PLH}		$\overline{G}$				20		ns
t_{PHL}						22		
t_{PLH}		I/O				27		ns
t_{PHL}						26		
t_{PLH}		C_{n+4}	R_L = 2 kΩ,	C_L = 15 pF		39		ns
t_{PHL}						37		
t_{PZH}	RS0-RS2	I/O	R_L = 667 Ω	C_L = 45 pF		31		ns
t_{PZL}						31		
t_{PHZ}				C_L = 5 pF		30		ns
t_{PLZ}						30		
t_{PZH}		LI/RO	R_L = 2 kΩ	C_L = 15 pF		25		ns
t_{PZL}						29		
t_{PHZ}				C_L = 5 pF		25		ns
t_{PLZ}						25		
t_{PZH}		RI/LO	R_L = 2 kΩ	C_L = 15 pF		25		ns
t_{PZL}						31		
t_{PZH}				C_L = 5 pF		25		ns
t_{PZL}						25		

NOTE 2: For load circuit and voltage waveforms see page 3-11 of *"The TTL Data Book for Design Engineers"*, second edition.

t_{PLH} ≡ Propagation delay time, low-to-high-level input
t_{PHL} ≡ Propagation delay time, high-to-low-level input
t_{PZL} ≡ Output enable time to low level
t_{PZH} ≡ Output enable time to high level
t_{PLZ} ≡ Output disable time from low level
t_{PHZ} ≡ Output disable time from high level

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TYPES SN54LS682 THRU SN54LS689, SN74LS682 THRU SN74LS689 8-BIT MAGNITUDE COMPARATORS

D2617, JANUARY 1981

- Compares Two 8-Bit Words
- Choice of Totem-Pole or Open-Collector Outputs
- Hysteresis at P and Q Inputs
- 'LS682 and 'LS683 have 20-kΩ Pullup Resistors on the Q Inputs
- 'LS686 and 'LS687 . . . New JT and NT 24-Pin, 300-Mil Packages

TYPE	$\overline{P=Q}$	$\overline{P>Q}$	OUTPUT ENABLE	OUTPUT CONFIGURATION	20-kΩ PULLUP
'LS682	yes	yes	no	totem-pole	yes
'LS683	yes	yes	no	open-collector	yes
'LS684	yes	yes	no	totem-pole	no
'LS685	yes	yes	no	open-collector	no
'LS686	yes	yes	yes	totem-pole	no
'LS687	yes	yes	yes	open-collector	no
'LS688	yes	no	yes	totem-pole	no
'LS689	yes	no	yes	open-collector	no

description

These magnitude comparators perform comparisons of two eight-bit binary or BCD words. All types provide $\overline{P=Q}$ outputs and the 'LS682 thru 'LS687 provide $\overline{P>Q}$ outputs as well. The 'LS682, 'LS684, 'LS686, and 'LS688 have totem-pole outputs, while the 'LS683, 'LS685, 'LS687, and 'LS689 have open-collector outputs. The 'LS682 and 'LS683 feature 20-kΩ pullup termination resistors on the Q inputs for analog or switch data.

FUNCTION TABLE

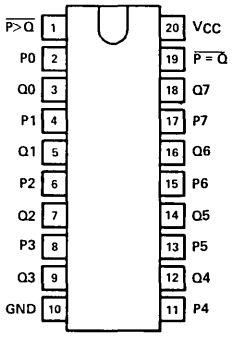
INPUTS			OUTPUTS	
DATA	ENABLES			
P, Q	$\overline{G}$, $\overline{G1}$	$\overline{G2}$	$\overline{P=Q}$	$\overline{P>Q}$
P = Q	L	L	L	H
P > Q	L	L	H	L
P < Q	L	L	H	H
X	H	H	H	H

H = high level, L = low level, X = irrelevant

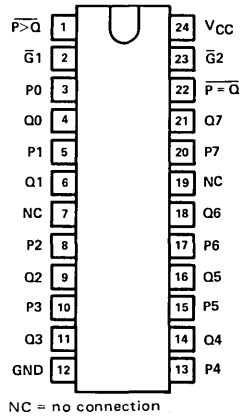
NOTES: 1. The last line of function table applies only to those devices having enable inputs, i.e., 'LS686 thru 'LS689.

2. The $\overline{P<Q}$ function can be generated by applying the $\overline{P=Q}$ and $\overline{P>Q}$ outputs to a 2-input NAND gate.

SN54LS682 THRU SN54LS685 . . . J PACKAGE
SN74LS682 THRU SN74LS685 . . . J OR N PACKAGE
(TOP VIEW)

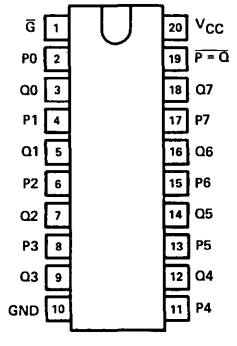


SN54LS686, SN54LS687 . . . JT PACKAGE
SN74LS686, SN74LS687 . . . JT OR NT PACKAGE
(TOP VIEW)



NC = no connection

SN54LS688, SN54LS689 . . . J PACKAGE
SN74LS688, SN74LS689 . . . J OR N PACKAGE
(TOP VIEW)



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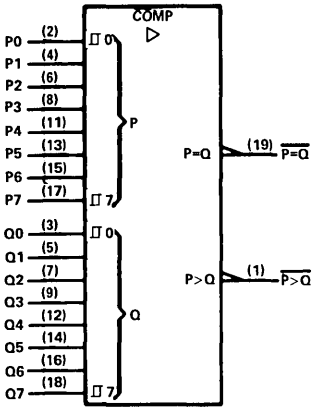
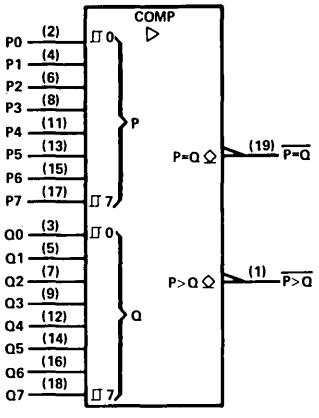
logic symbols

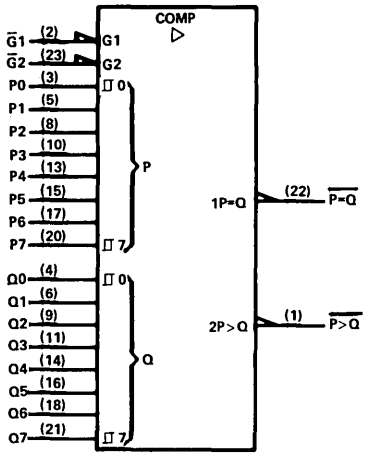
'LS682, 'LS684



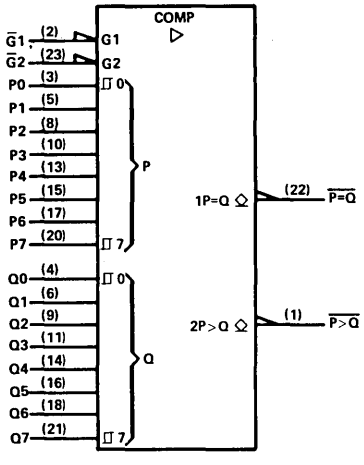
'LS683, 'LS685



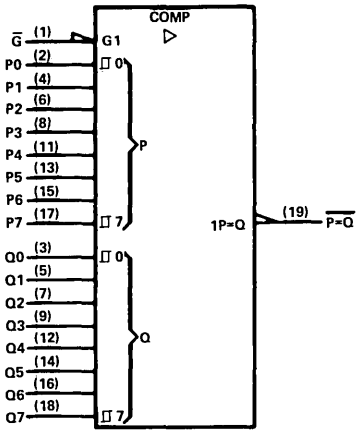
'LS686



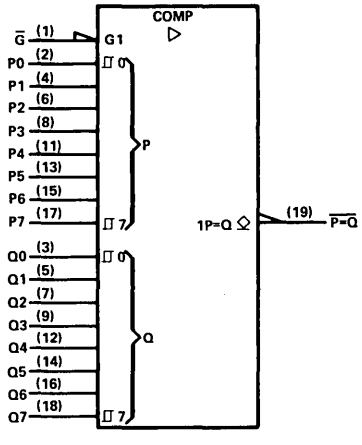
'LS687



'LS688



'LS689



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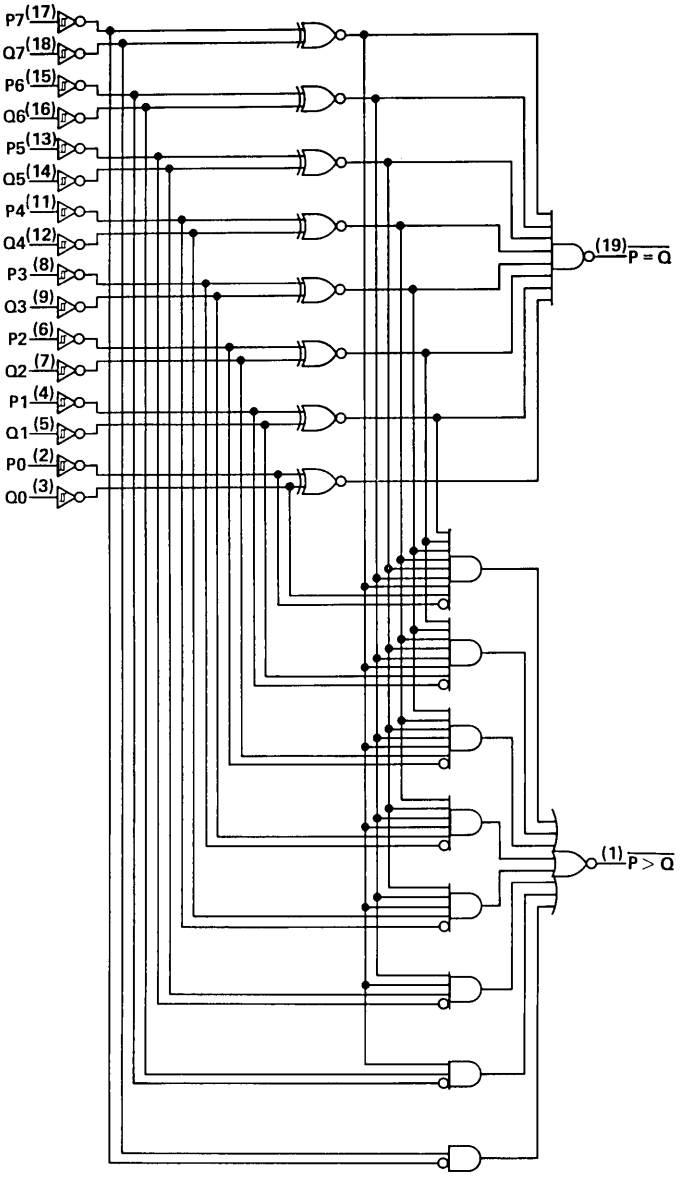
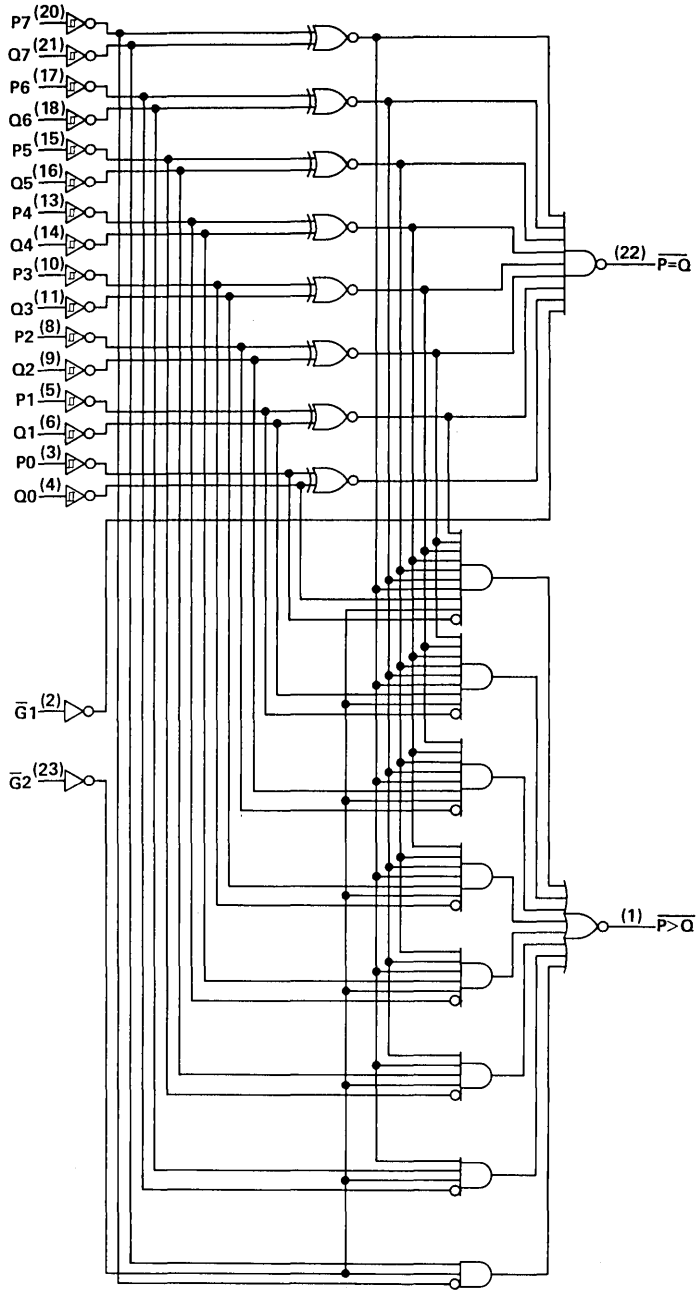
'LS682 thru 'LS685 functional block diagram (positive logic)



'LS686, 'LS687 functional block diagram (positive logic)



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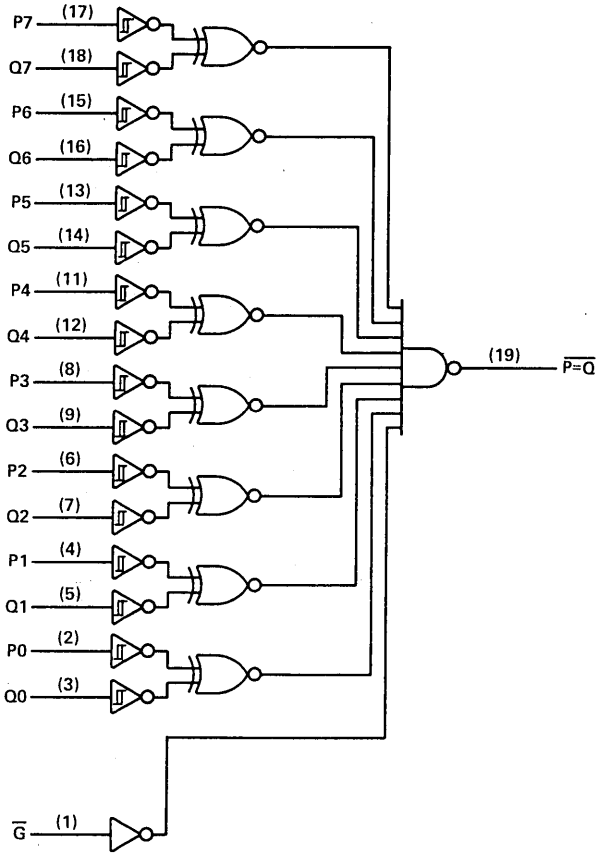
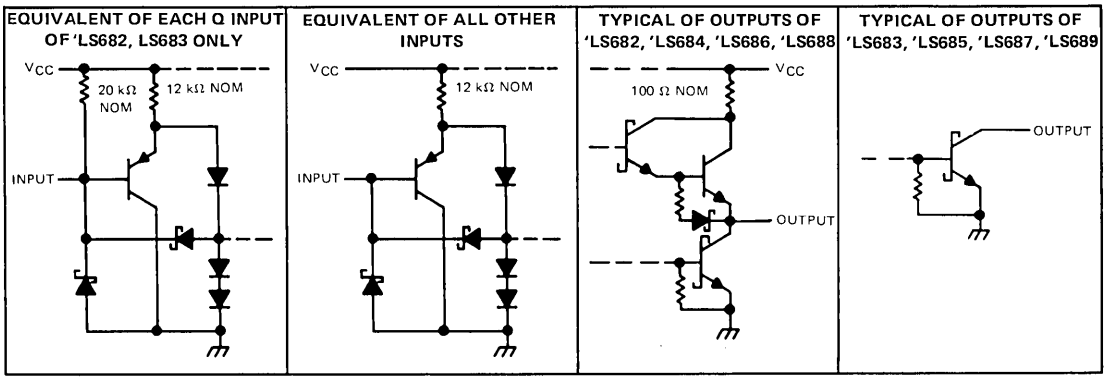
'LS688, 'LS689 functional block diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage (see Note 1)	7 V
Input voltage: Q inputs of 'LS682 and 'LS683	5.5 V
All other inputs	7 V
Off-state output voltage: 'LS683, 'LS685, 'LS687, 'LS689	5.5 V
Operating free-air temperature range: SN54LS682 thru SN54LS689	−55°C to 125°C
SN74LS682 thru SN74LS689	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

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'LS682, 'LS684, 'LS686, 'LS688

recommended operating conditions

PARAMETER	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
$V_{T+} - V_{T-}$	Hysteresis	P or Q inputs	V_{CC} = MIN			0.4			0.4		V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = V_{IL}max,	V_{IH} = 2 V, I_{OH} = −400 μA	2.5			2.7			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
I_I	Input current at maximum input voltage	Q inputs, 'LS682	V_{CC} = MAX,	V_I = 5.5 V			0.1			0.1	mA
		All other inputs	V_{CC} = MAX,	V_I = 7 V							
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current	Q inputs, 'LS682	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
		All other inputs					−0.2			−0.2	
I_{OS}	Short-circuit output current¶		V_{CC} = MAX,	V_O = 0	−20		−100	−20		−100	mA
I_{CC}	Supply current	'LS682	V_{CC} = MAX,	See Note 2		42	70		42	70	mA
		'LS684				40	65		40	65	
		'LS686				44	75		44	75	
		'LS688				40	65		40	65	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

¶Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: I_{CC} is measured with any $\overline{G}$ inputs grounded, all other inputs at 4.5 V, and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER#	FROM (INPUTS)	TO (OUTPUT)	TEST CONDITIONS	'LS682			'LS684			'LS686			'LS688			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	P	$\overline{P=Q}$	R_L = 667 Ω, C_L = 45 pF, All other inputs low, See Note 3		13	25		15	25		13	25		12	18	ns
t_{PHL}					15	25		17	25		20	30		17	23	
t_{PLH}	Q	$\overline{P=Q}$			14	25		16	25		13	25		12	18	ns
t_{PHL}					15	25		15	25		21	30		17	23	
t_{PLH}	$\overline{G}$, $\overline{G1}$	$\overline{P=Q}$									11	20		12	18	ns
t_{PHL}											19	30		13	20	
t_{PLH}	P	$\overline{P>Q}$			20	30		22	30		19	30				ns
t_{PHL}					15	30		17	30		15	30				
t_{PLH}	Q	$\overline{P>Q}$			21	30		24	30		18	30				ns
t_{PHL}					19	30		20	30		19	30				
t_{PLH}	$\overline{G2}$	$\overline{P>Q}$									21	30				ns
t_{PHL}											16	25				

#t_{PLH} ≡ propagation delay time, low-to-high-level outputs; t_{PHL} ≡ propagation delay time, high-to-low-level output.

NOTE 3: Load circuit and waveforms are shown on page 3-11 of *The TTL Data Book for Design Engineers*, second edition, LCC4112.

recommended operating conditions 'LS683, 'LS685, 'LS687, 'LS689

PARAMETER	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
$V_{T+} - V_{T-}$	Hysteresis	P or Q inputs	V_{CC} = MIN			0.4			0.4		V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = V_{IL}max,	V_{IH} = 2 V, V_{OH} = 5.5 V			250			100	μA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
I_I	Input current at maximum input voltage	Q inputs, 'LS683	V_{CC} = MAX,	V_I = 5.5 V			0.1			0.1	mA
		All other inputs	V_{CC} = MAX,	V_I = 7 V							
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current	Q inputs, 'LS683	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
		All other inputs					−0.2			−0.2	
I_{CC}	Supply current	'LS683	V_{CC} = MAX,	See Note 2		42	70		42	70	mA
		'LS685				40	65		40	65	
		'LS687				44	75		44	75	
		'LS689				40	65		40	65	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: I_{CC} is measured with any G inputs grounded, all other inputs at 4.5 V, and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUTS)	TO (OUTPUT)	TEST CONDITIONS	'LS683			'LS685			'LS687			'LS689			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	P	$\overline{P=Q}$	R_L = 667 Ω, C_L = 45 pF, All other inputs low, See Note 3		30	45		30	45		24	35		24	40	ns
t_{PHL}					20	30		19	35		20	30		22	35	
t_{PLH}	Q	$\overline{P=Q}$			24	35		24	45		24	35		24	40	ns
t_{PHL}					23	35		23	35		20	30		22	35	
t_{PLH}	$\overline{G}$, $\overline{G}1$	$\overline{P=Q}$									21	35		22	35	ns
t_{PHL}											18	30		19	30	
t_{PLH}	P	$\overline{P>Q}$			31	45		32	45		24	35				ns
t_{PHL}					17	30		16	35		16	30				
t_{PLH}	Q	$\overline{P>Q}$			30	45		30	45		24	35				ns
t_{PHL}					21	30		20	35		16	30				
t_{PLH}	$\overline{G}2$	$\overline{P>Q}$									24	35				ns
t_{PHL}											15	30				

¶t_{PLH} ≡ propagation delay time, low-to-high-level output; t_{PHL} ≡ propagation delay time, high-to-low-level output.
NOTE 3: Load circuit and waveforms are shown on page 3-11 of *The TTL Data Book for Design Engineers,* second edition, LCC4112.

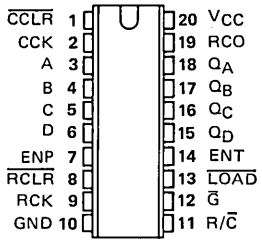
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TYPES SN54LS690 THRU SN54LS693, SN74LS690 THRU SN74LS693 SYNCHRONOUS COUNTERS WITH OUTPUT REGISTERS AND MULTIPLEXED 3-STATE OUTPUTS

D2423, JANUARY 1981

- 4-Bit Counters/Registers
- Multiplexed Outputs for Counter or Latched Data
- 3-State Outputs Drive Bus Lines Directly
- 'LS690 . . Decade Counter, Direct Clear
  'LS691 . . Binary Counter, Direct Clear
  'LS692 . . Decade Counter, Synchronous Clear
  'LS693 . . Binary Counter, Synchronous Clear

SN54LS690 THRU SN54LS693 . . . J PACKAGE
SN74LS690 THRU SN74LS693 . . . J OR N PACKAGE
(TOP VIEW)



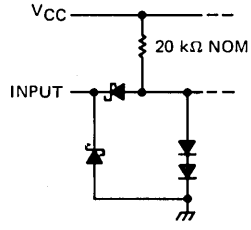
description

These low-power Schottky LSI devices incorporate synchronous counters, four-bit D-type registers, and quadruple two-line to one-line multiplexers with three-state outputs in a single 20-pin package. The counters can be programmed from the data inputs and have enable P and enable T inputs and a ripple-carry output for easy expansion. The register/counter select input, R/$\overline{C}$, selects the counter when low or the register when high for the three-state outputs, Q_A, Q_B, Q_C, and Q_D. These outputs are rated at 12 and 24 milliamperes (54LS/74LS) for good bus-driving performance.

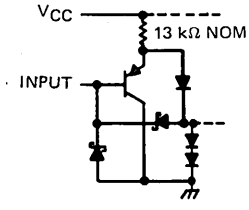
Individual clock and clear inputs are provided for both the counter and the register. Both clock inputs are positive-edge triggered. The clear line is active low and is asynchronous on the 'LS690 and 'LS691, synchronous on the 'LS692 and 'LS693.

schematics of inputs and outputs

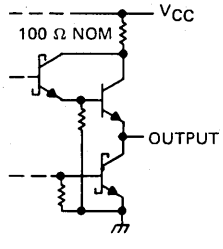
EQUIVALENT OF A, B, C, D INPUTS



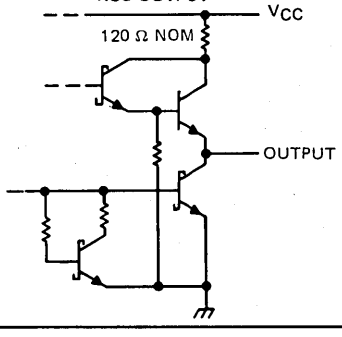
EQUIVALENT OF ALL OTHER INPUTS



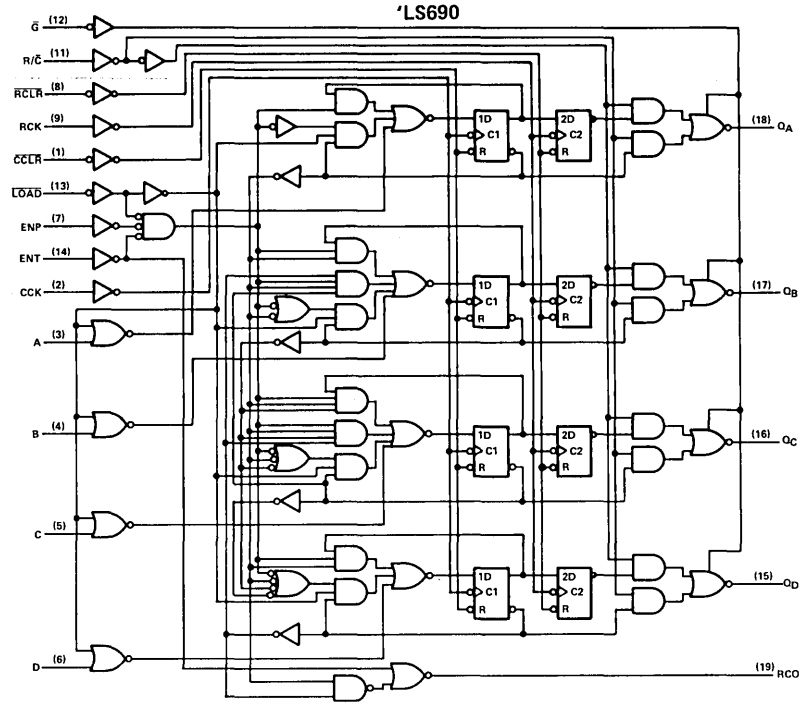
TYPICAL OF ALL Q OUTPUTS



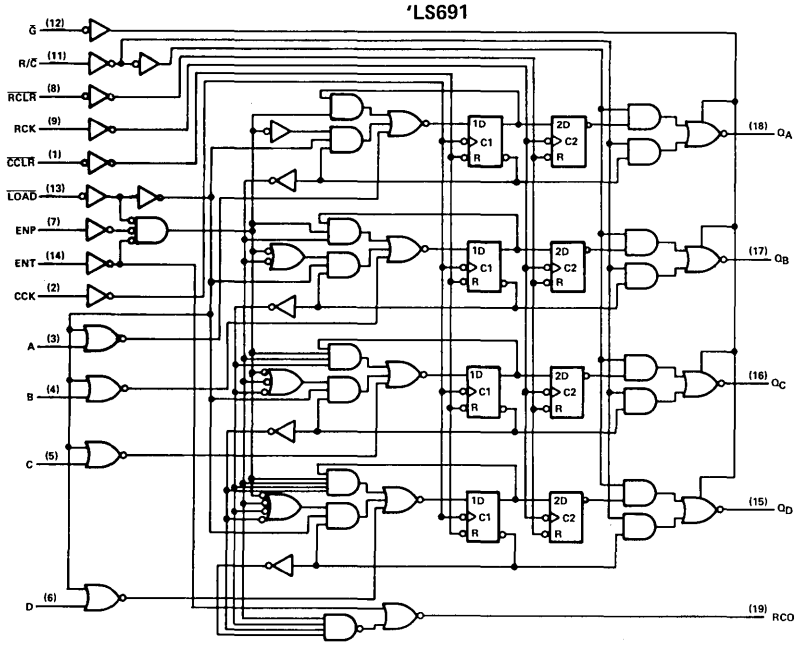
RCO OUTPUT



'LS690



'LS691



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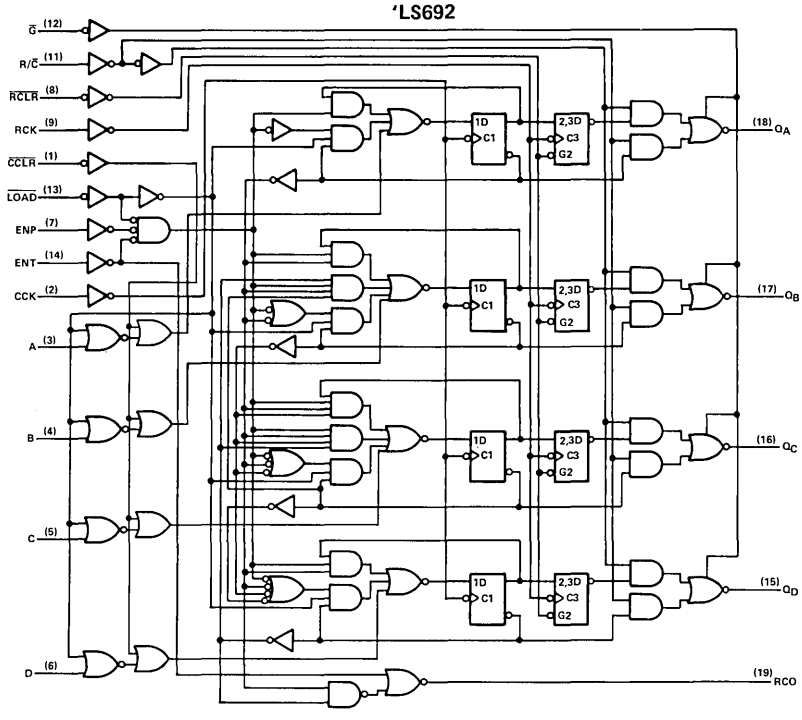
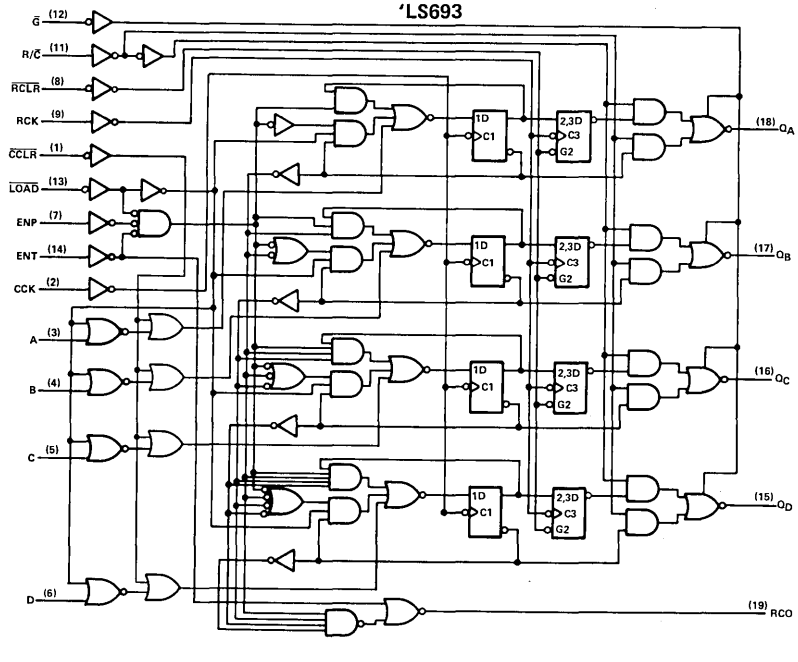
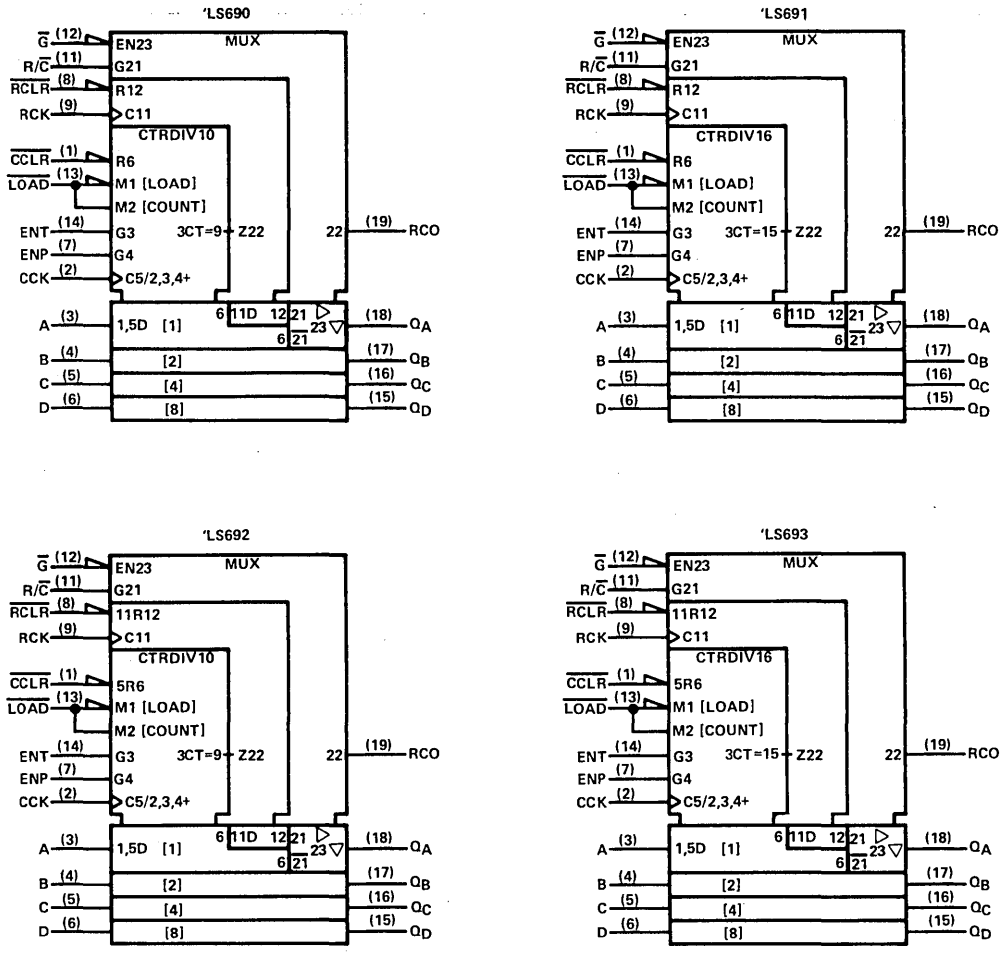
'LS692


G (12)
R/C (11)
RCLR (8)
RCK (9)
CCLR (1)
LOAD (13)
ENP (7)
ENT (14)
CCK (2)
A (3)
B (4)
C (5)
D (6)
1D
C1
2,3D
C3
G2
(18) QA
(17) QB
(16) QC
(15) QD
(19) RCO

'LS693


G (12)
R/C (11)
RCLR (8)
RCK (9)
CCLR (1)
LOAD (13)
ENP (7)
ENT (14)
CCK (2)
A (3)
B (4)
C (5)
D (6)
1D
C1
2,3D
C3
G2
(18) QA
(17) QB
(16) QC
(15) QD
(19) RCO

logic symbols



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS690 thru SN54LS693	−55°C to 125°C
SN74LS690 thru SN74LS693	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

recommended operating conditions

			SN54LS'			SN74LS'			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}			4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}		Q			−1			−2.6	mA
		RCO			−400			−400	μA
Low-level output current, I_{OL}		Q			12			24	mA
		RCO			4			8	mA
Clock frequency, f_{clock}		CCK	0		20	0		20	MHz
		RCK	0		20	0		20	MHz
Width of clock pulse, t_w (high or low)		CCK	25			25			ns
		RCK	25			25			ns
Setup time, t_{su}		A-D to CCK↑	30			30			ns
		Enable P or T to CCK↑	30			30			ns
	'LS692, 'LS693 only	$\overline{CCLR}$↓ to CCK↑	20			20			ns
	'LS692, 'LS693 only	$\overline{RCLR}$↓ to RCK↑	20			20			ns
Hold time, t_h	Any input from CCK↑ or RCK↑		0			0			ns
Operating free-air temperature, T_A			−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC}=MIN, I_I=−18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	Any Q	V_{CC}=MIN, V_{IH}=2 V, V_{IL}=V_{IL} max	I_{OH}=−1 mA	2.4	3.1					V
		Any Q		I_{OH}=−2.6 mA				2.4	3.1		
		RCO		I_{OH}=−400 μA	2.5	3.2		2.7	3.2		
V_{OL}	Low-level output voltage	Any Q	V_{CC}=MIN, V_{IH}=2 V, V_{IL}=V_{IL} max	I_{OL}=12 mA		0.25	0.4		0.25	0.4	V
		Any Q		I_{OL}=24 mA					0.35	0.5	
		RCO		I_{OL}=4 mA		0.25	0.4		0.25	0.4	
		RCO		I_{OL}=8 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	Any Q	V_{CC}=MAX, V_{IH}=2 V, V_{IL}=V_{IL} max, V_O=2.7 V				20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied	Any Q	V_{CC}=MAX, V_{IH}=2 V, V_{IL}=V_{IL} max, V_O=0.4 V				−20			−20	μA
I_I	Input current at maximum input voltage		V_{CC}=MAX, V_I=7 V				0.1			0.1	mA
I_{IH}	High-level input current		V_{CC}=MAX, V_I=2.7 V				20			20	μA
I_{IL}	Low-level input current	A thru D	V_{CC}=MAX, V_I=0.4 V				−0.4			−0.4	mA
		All others					−0.2			−0.2	
I_{OS}	Short-circuit output current§	Any Q	V_{CC}=MAX, V_O=0 V		−30		−130	−30		−130	mA
		RCO			−20		−100	−20		−100	
I_{CCH}	Supply current, outputs high		V_{CC}=MAX, All outputs open	See Note 2		46	65		46	65	mA
I_{CCL}	Supply current, outputs low			See Note 3		48	70		48	70	
I_{CCZ}	Supply current, outputs off			See Note 4		48	70		48	70	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and duration of short-circuit should not exceed one second.

NOTES: 2. I_{CCH} is measured after two 4.5-V to 0-V to 4.5-V pulses have been applied to CCK and RCK while $\overline{G}$ is grounded and all other inputs are at 4.5 V.
3. I_{CCL} is measured after two 0-V to 4.5-V to 0-V pulses have been applied to CCK and RCK while all other inputs are grounded.
4. I_{CCZ} is measured after two 0-V to 4.5-V to 0-V pulses have been applied to CCK and RCK while $\overline{G}$ is at 4.5 V and all other inputs are grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, see note 5

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS690, 'LS691			'LS692, 'LS693			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	CCK↑	RCO	R_L = 2 kΩ, C_L = 15 pF		23	40		23	40	ns
t_{PHL}					23	40		23	40	
t_{PLH}	ENT	RCO			13	20		13	20	ns
t_{PHL}					13	20		13	20	
t_{PLH}	CCK↑	Q	R_L = 667 Ω, C_L = 45 pF		12	20		12	20	ns
t_{PHL}					17	25		17	25	
t_{PLH}	RCK↑	Q			12	20		12	20	ns
t_{PHL}					17	25		17	25	
t_{PHL}	$\overline{CCLR}$↓	Q			23	40				ns
t_{PHL}	$\overline{RCLR}$↓	Q			20	30				ns
t_{PHL}	CCK↑	Q (CLEAR)						23	40	ns
t_{PHL}	RCK↑	Q (CLEAR)						20	30	ns
t_{PLH}	R/$\overline{C}$	Q			16	25		16	25	ns
t_{PHL}					16	25		16	25	
t_{PZH}	$\overline{G}$↓	Q			19	30		19	30	ns
t_{PZL}					19	30		19	30	
t_{PHZ}	$\overline{G}$↑	Q	R_L = 667 Ω, C_L = 5 pF		17	30		17	30	ns
t_{PLZ}					17	30		17	30	

NOTE 5: Load circuit and voltage waveforms are shown on page 3-11 of *The TTL Data Book for Design Engineers*, Second Edition, LCC4112.

t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
t_{PZH} ≡ Output enable time to high level
t_{PZL} ≡ Output enable time to low level
t_{PHZ} ≡ Output disable time from high level
t_{PLZ} ≡ Output disable time from low level

TEXAS INSTRUMENTS
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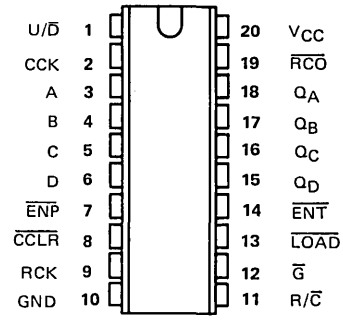
TYPES SN54LS696 THRU SN54LS699, SN74LS696 THRU SN74LS699 SYNCHRONOUS UP/DOWN COUNTERS WITH OUTPUT REGISTERS AND MULTIPLEXED 3-STATE OUTPUTS

D2424, JANUARY 1981

- 4-Bit Counters/Registers
- Multiplexed Outputs for Counter or Latched Data
- 3-State Outputs Drive Bus Lines Directly
- 'LS696 . . Decade Counter, Direct Clear
  'LS697 . . Binary Counter, Direct Clear
  'LS698 . . Decade Counter, Synchronous Clear
  'LS699 . . Binary Counter, Synchronous Clear

SN54LS696 THRU SN54LS699 . . J PACKAGE
SN74LS696 THRU SN74LS699 . . J OR N PACKAGE
(TOP VIEW)



2

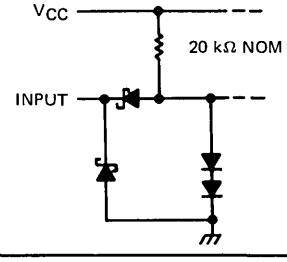
description

These low-power Schottky LSI devices incorporate synchronous up/down counters, four-bit D-type registers, and quadruple two-line to one-line multiplexers with three-state outputs in a single 20-pin package. The up/down counters are programmable from the data inputs and feature enable $\overline{P}$ and enable $\overline{T}$ and a ripple-carry output for easy expansion. The register/counter select input R/$\overline{C}$, selects the counter when low and the register when high for the three-state outputs, Q_A, Q_B, Q_C, and Q_D. These outputs are rated at 12 and 24 milliamperes (54LS/74LS) for good bus driving performance.

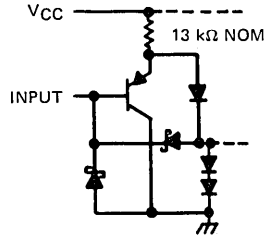
Both the counter clock CCK and register clock RCK are positive-edge triggered. The counter clear $\overline{CCLR}$ is active low and is asynchronous on the 'LS696 and 'LS697, synchronous on the 'LS698 and 'LS699.

schematics of inputs and outputs

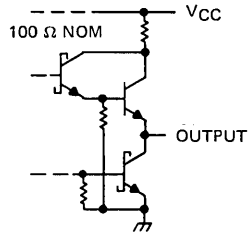
EQUIVALENT OF A, B, C, D INPUTS



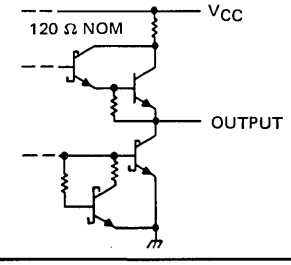
EQUIVALENT OF ALL OTHER INPUTS



TYPICAL OF ALL Q OUTPUTS

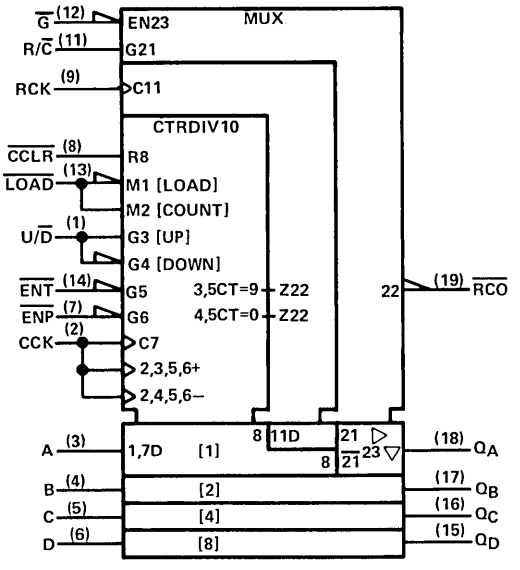


$\overline{RCO}$ OUTPUT

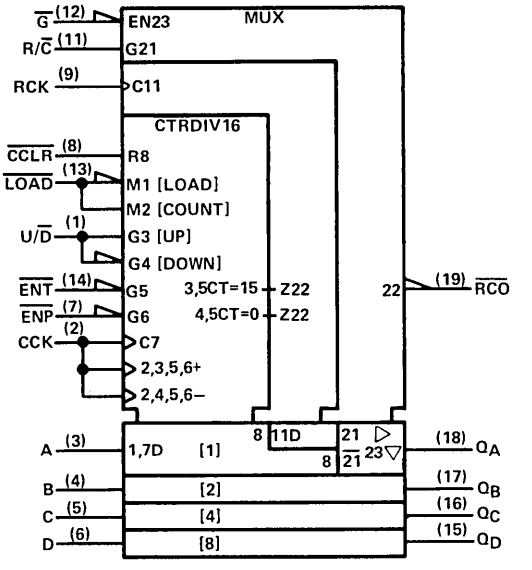


logic symbols

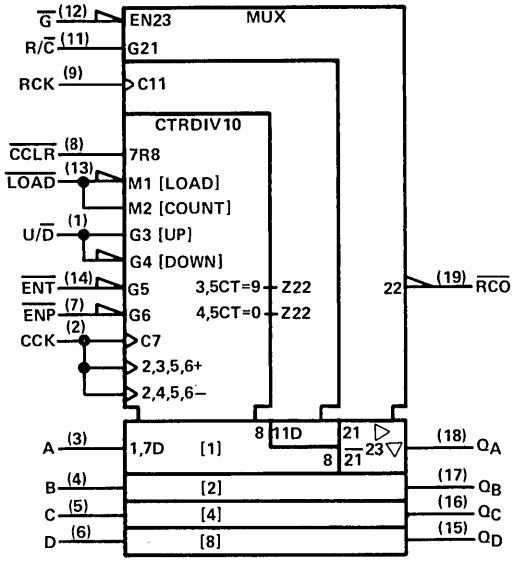
'LS696



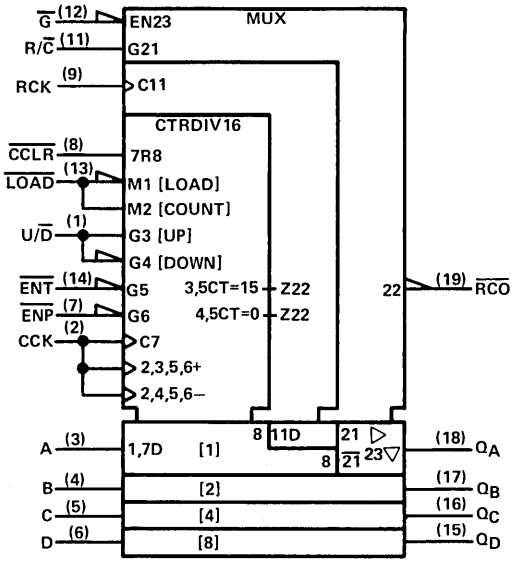
'LS697



'LS698



'LS699



TEXAS INSTRUMENTS
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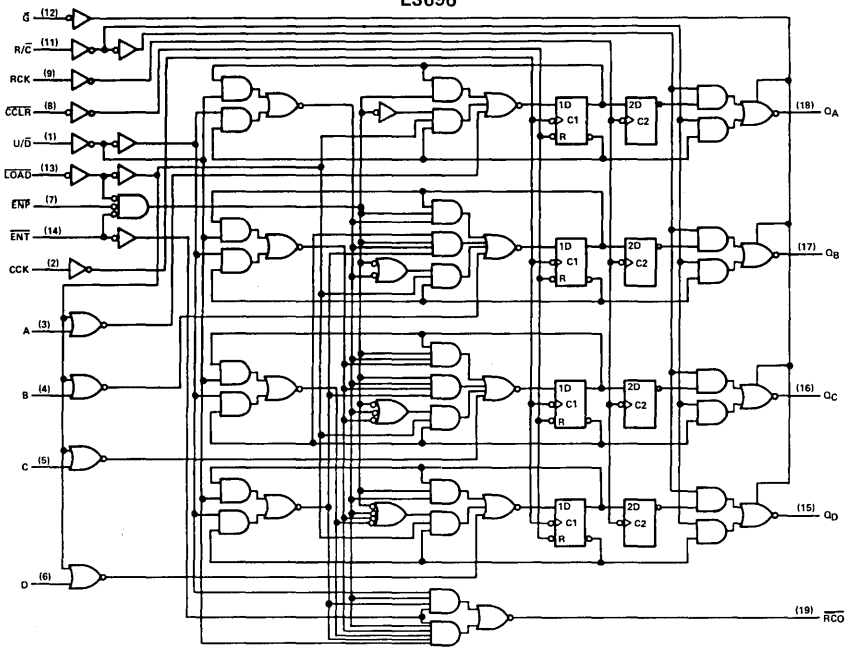
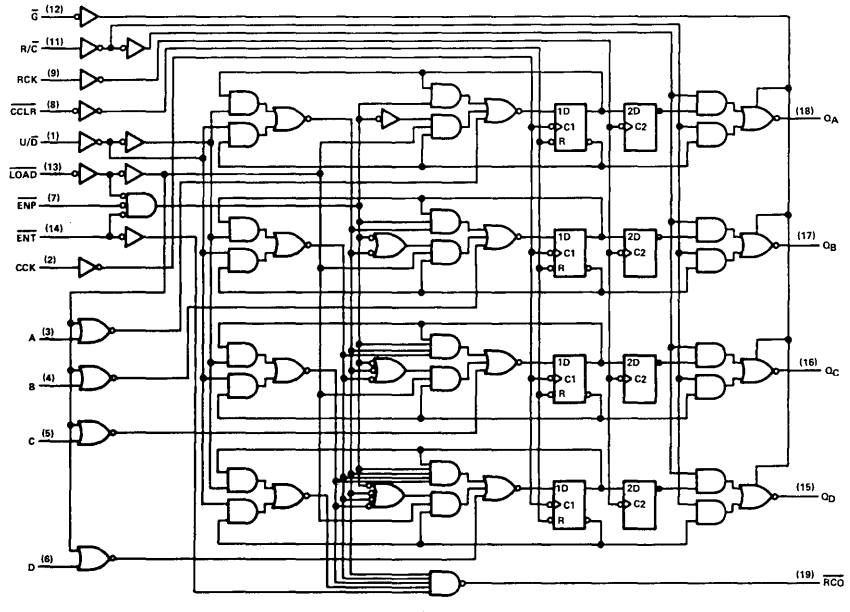
functional block diagrams

'LS696

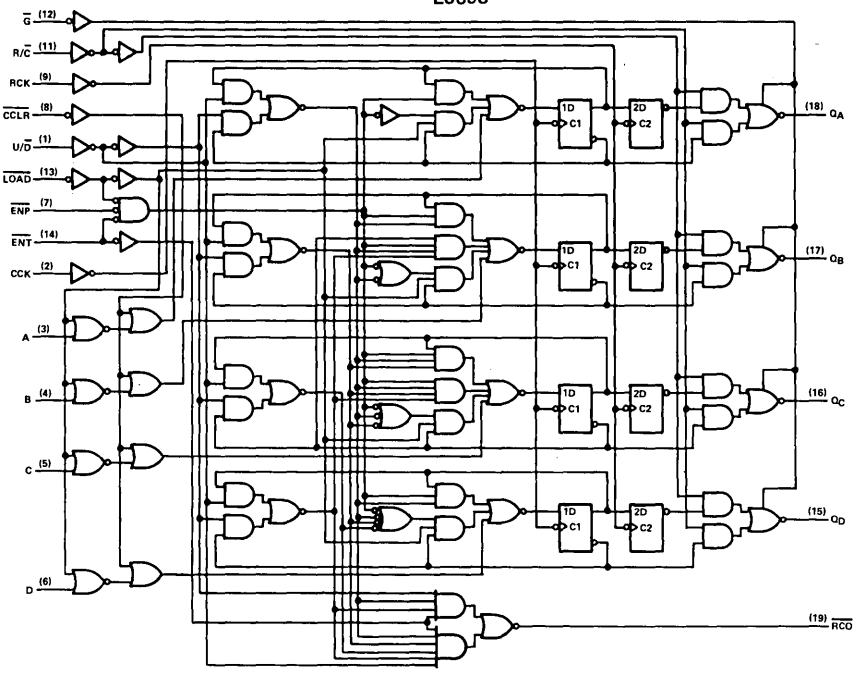


'LS697

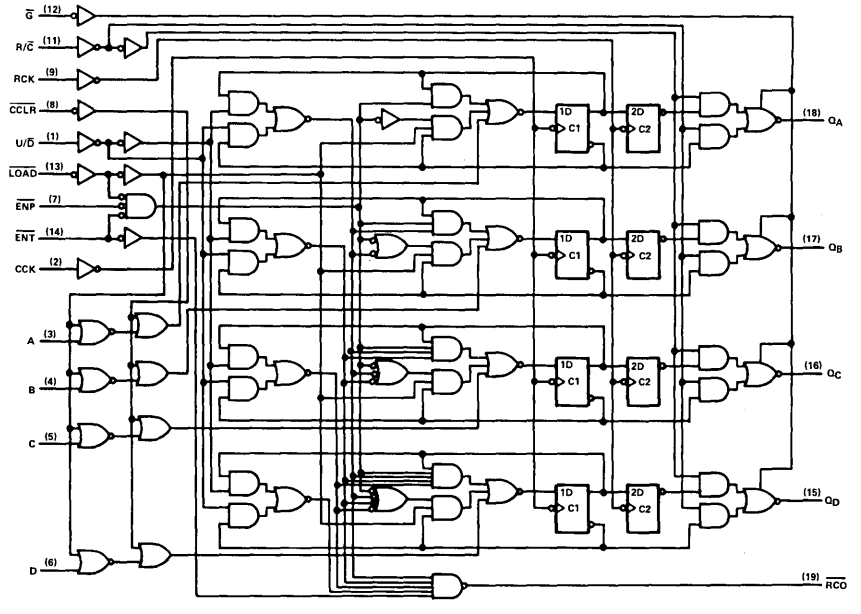


functional block diagrams

'LS698



'LS699



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54LS696 thru SN54LS699 . . . . . −55°C to 125°C
SN74LS696 thru SN74LS699 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	Q			−1			−2.6	mA
	$\overline{RCO}$			−400			−400	μA
Low-level output current, I_{OL}	Q			12			24	mA
	$\overline{RCO}$			4			8	
Clock frequency, f_{clock}	CCK	0		20	0		20	MHz
	RCK	0		20	0		20	
Width of clock pulse, t_w (high or low)	CCK	25			25			ns
	RCK	25			25			
Setup time, t_{su}	A-D to CCK↑	30			30			ns
	Enable $\overline{P}$ or $\overline{T}$ to CCK↑	30			30			
	U/$\overline{D}$ to CCK↑	35			35			
	'LS698, 'LS699, $\overline{CCLR}$ to CCK↑	20			20			
Hold time, t_h		0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC}=MIN, I_I=−18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	Any Q	V_{CC}=MIN, V_{IH}=2 V, V_{IL}=V_{IL} max	I_{OH}=−1 mA	2.4	3.1					V
		Any Q		I_{OH}=−2.6 mA				2.4	3.1		
		$\overline{RCO}$		I_{OH}=−400 μA	2.5	3.2		2.7	3.2		
V_{OL}	Low-level output voltage	Any Q	V_{CC}=MIN, V_{IH}=2 V, V_{IL}=V_{IL} max	I_{OL}=12 mA		0.25	0.4		0.25	0.4	V
		Any Q		I_{OL}=24 mA					0.35	0.5	
		$\overline{RCO}$		I_{OL}=4 mA		0.25	0.4		0.25	0.4	
		$\overline{RCO}$		I_{OL}=8 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	Any Q	V_{CC}=MAX, $\overline{G}$ at 2 V,	V_O=2.7 V			20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied	Any Q	V_{CC}=MAX, $\overline{G}$ at 2 V,	V_O=0.4 V			−20			−20	μA
I_I	Input current at maximum input voltage		V_{CC}=MAX, V_I=7 V				0.1			0.1	mA
I_{IH}	High-level input current		V_{CC}=MAX, V_I=2.7 V				20			20	μA
I_{IL}	Low-level input current	A thru D	V_{CC}=MAX, V_I=0.4 V				−0.4			−0.4	mA
		All others					−0.2			−0.2	
I_{OS}	Short-circuit output current§	Any Q	V_{CC}=MAX, V_O=0 V		−30		−130	−30		−130	mA
		$\overline{RCO}$			−20		−100	−20		−100	
I_{CCH}	Supply current, outputs high		V_{CC}=MAX, All outputs open	See Note 2		46	65		46	65	mA
I_{CCL}	Supply current, outputs low			See Note 3		48	70		48	70	
I_{CCZ}	Supply current, outputs off			See Note 4		48	70		48	70	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTES: 2. I_{CCH} is measured after two 4.5 V to 0 V to 4.5 V pulses have been applied to CCK and RCK while $\overline{G}$ is grounded and all other inputs are at 4.5 V.

3. I_{CCL} is measured after two 0 V to 4.5 V to 0 V pulses have been applied to CCK and RCK while all other inputs are grounded.

4. I_{CCZ} is measured after two 0 V to 4.5 V to 0 V pulses have been applied to CCK and RCK while $\overline{G}$ is at 4.5 V and all other inputs are grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS696, 'LS697			'LS698, 'LS699			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	CCK↑	$\overline{RCO}$	R_L = 2 kΩ, C_L = 15 pF		23	40		23	40	ns
t_{PHL}					23	40		23	40	ns
t_{PLH}	$\overline{ENT}$	$\overline{RCO}$			13	20		13	20	ns
t_{PHL}					13	20		13	20	ns
t_{PLH}	CCK↑	Q	R_L = 667 Ω, C_L = 45 pF		12	20		12	20	ns
t_{PHL}					17	25		17	25	ns
t_{PLH}	RCK↑	Q			12	20		12	20	ns
t_{PHL}					17	25		17	25	ns
t_{PHL}	$\overline{CCLR}$↓	Q			23	40				ns
t_{PHL}	CCK↑	Q (CLEAR)						23	40	ns
t_{PLH}	R/$\overline{C}$	Q			16	25		16	25	ns
t_{PHL}					16	25		16	25	ns
t_{PZH}	$\overline{G}$↓	Q			19	30		19	30	ns
t_{PZL}					19	30		19	30	ns
t_{PHZ}	$\overline{G}$↑	Q	R_L = 667 Ω, C_L = 5 pF		17	30		17	30	ns
t_{PLZ}					17	30		17	30	ns

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Advanced Low-Power Schottky and Advanced Schottky Circuits

INTRODUCTION

The development by Texas Instruments of an advanced Schottky TTL process has enabled TI to offer two new high-performance bipolar logic families. Both of these product lines, Advanced Low-Power Schottky (ALS) and Advanced Schottky (AS), are constructed with an advanced oxide-isolated, ion-implanted process employing composed masks. This process, compared to previous process technologies, allows for smaller and shallower geometries, which means a substantial reduction in parasitic and side-wall capacitances and decreased transistor switching times. The end result is an improvement in the speed-power performance. The ALS family will offer both lower power and faster speeds than LS, while the AS family will offer speeds up to twice as fast as Schottky TTL at approximately the same power.

The ALS family features a reduction in power dissipation per gate, improved AC performance, higher input threshold, schottky clamping diodes on each input and output, protection against negative input voltage, full TTL compatibility, and (like the LS family) three categories of output drive capability (that is standard, buffer, and bus-driver type outputs). While the ALS product line does include SSI and MSI devices that are functionally and pin-for-pin compatible with already existing popular TTL, S, and LS devices, the major design emphasis will be on the introduction of new state-of-the-art LSI type devices. All ALS DC parameters, with the exception of I_{CC} and one or two other parameters, will have the same specification as LS devices.

The AS family features a 30- to 40-percent improvement in AC performance, full TTL compatibility, and sink and source capability equal to or greater than Schottky TTL. The AS product line will consist mainly of new high-density 20- or 24-pin functions. The 24-pin functions will be offered in a new 300-mil slim-line package. Again, most AS DC parameters will have the same specifications as Schottky TTL.

All ALS and AS devices will be offered in both plastic and ceramic chip carriers. Pin assignments for ALS and AS devices in plastic chip carriers (FN) are given in Section 7 of this supplement.

This section (Section 5) is divided into the ALS portion and the AS portion. Both have the following format: A two-page comprehensive listing is given of the DC parameters (that is, absolute maximum ratings, recommended operating conditions, and electrical characteristics) of that family. An important item to note is that the 74 series, as well as the 54 series, will be specified at plus or minus ten-percent power-supply tolerance. Each family will offer outputs with three different drive capabilities.

These two pages are followed by individual data sheets that contain the following device information; pinout, functional description, function table, and I_{CC} and switching parameters, when available. Another important item to note is the change in AC specifications. All ALS devices will be specified over the full recommended ranges of temperature and V_{CC} with a 50-pF load for both the 54 and 74 series as well as the usual 15-pF, 25°C, 5-V specifications. AS devices will also be specified with a 50-pF load over the full recommended ranges of temperature and V_{CC} and at 25°C and 5 V.

ABSOLUTE MAXIMUM RATINGS OVER FREE-AIR TEMPERATURE RANGE

Supply voltage, V_{CC} (See Note 1)		7V
Input voltage, V_I: All inputs		7V
I/O ports		5.5V
Off state (High-level) voltage apllied to open-collector outputs		7V
High-level voltage applied to 3-state outputs		5.5V
Operating free-air temperature range:	SN54ALS	-55°C to 125°C
	SN74ALS	0°C to 70°C
Storage temperature range		-65°C to 150°C

NOTE: 1. Voltage values are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		STANDARD OUTPUT			BUFFER OUTPUT			BUS DRIVER OUTPUT			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage	54/74ALS	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
High-level output current, I_{OH} †	54/74ALS			-0.4			-1			-12	mA
	74ALS*			-0.4			-2.6			-15	mA
High-level output voltage, V_{OH} ¶	54/74ALS			5.5			5.5			5.5	V
Low-level output current, I_{OL}	54/74ALS			4			12			12	mA
	74ALS*			8			24			24/48§	mA
Operating free-air temperature, T_A	54ALS	-55		125	-55		125	-55		125	°C
	74ALS	0		70	0		70	0		70	°C

† Does not apply to open-collector outputs.
¶ Applies only to open-collector outputs.
§ Indicates a dash one(-1) spec.
* The extended conditions apply if V_{CC} is maintained between 4.75V and 5.25V.

ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)

PARAMETER		TEST CONDITIONS		STANDARD OUTPUT MIN	STANDARD OUTPUT TYP†	STANDARD OUTPUT MAX	BUFFER OUTPUT MIN	BUFFER OUTPUT TYP†	BUFFER OUTPUT MAX	BUS DRIVER OUTPUT MIN	BUS DRIVER OUTPUT TYP†	BUS DRIVER OUTPUT MAX	UNIT
V_{IH}	HIGH-LEVEL INPUT VOLTAGE			2			2			2			V
V_{IL}	LOW-LEVEL INPUT VOLTAGE					0.8			0.8			0.8	V
V_{IK}	INPUT CLAMP VOLTAGE	V_{CC}=MIN, I_I=-18mA				-1.5			-1.5			-1.5	V
V_{OH}	HIGH-LEVEL OUTPUT VOLTAGE (SEE NOTE 1)	I_{OH}=-3mA	54/74ALS V_{CC}=MIN							2.4	3.2		V
		I_{OH}=MAX	54/74ALS V_{CC}=MIN	2.5	3.4		2.4	3.2		2			V
			74ALS V_{CC}=4.75V	2.7	3.4		2.4	3.3		2			V
I_{OH}	HIGH-LEVEL OUTPUT CURRENT (SEE NOTE 2)	V_{CC}=MIN, V_{OH}=MAX				0.1			0.1			0.1	mA
V_{OL}	LOW-LEVEL OUTPUT VOLTAGE	I_{OL}=MAX	54/74ALS V_{CC}=MIN		0.25	0.4		0.25	0.4		0.25	0.4	V
			74ALS V_{CC}=4.75V		0.35	0.5		0.35	0.5		0.35	0.5	V
I_I	INPUT CURRENT AT MAXIMUM INPUT VOLTGE	V_{CC}=MAX, V_I=7V				0.1			0.1			0.1	mA
I_{IH}	HIGH-LEVEL INPUT CURRENT	V_{CC}=MAX, V_I=2.7V				20			20			20	uA
I_{IL}	LOW-LEVEL INPUT CURRENT	V_{CC}=MAX, V_{IL}=0.4V				-0.2			-0.2			-0.2	mA
I_O	OUTPUT CURRENT ¶	V_{CC}=MAX, V_O=2.25V		-10		-60	-15		-70	-20		-120	mA
I_{OZH}	OFF-STATE OUTPUT CURRENT, HIGH-LEVEL VOLTAGE APPLIED (SEE NOTE 3)	V_{CC}=MAX, V_O=2.7V	I/O PORTS						40			40	uA
			NON-I/O						20			20	uA
I_{OZL}	OFF-STATE OUTPUT CURRENT, LOW-LEVEL VOLTAGE APPLIED (SEE NOTE 3)	V_{CC}=MAX, V_O=0.4V	I/O PORTS						-0.2			-0.2	mA
			NON-I/O						-20			-20	uA
I_{CC}	SUPPLY CURRENT (SEE NOTE 4)												mA

† ALL TYPICAL NUMBERS ARE AT V_{CC}=5V, T_A=25°C.

¶ THE OUTPUT CONDITIONS HAVE BEEN CHOSEN TO PRODUCE A CURRENT THAT CLOSELY APPROXIMATES ONE-HALF THE TRUE SHORT-CIRCUIT CURRENT, I_{OS}.

NOTES 1. DOES NOT APPLY TO OPEN-COLLECTOR OUTPUTS.
2. APPLIES ONLY TO OPEN-COLLECTOR OUTPUTS.
3. APPLIES ONLY TO 3-STATE OUTPUTS.
4. REFER TO INDIVIDUAL DATA SHEET FOR I_{CC} LIMITS.

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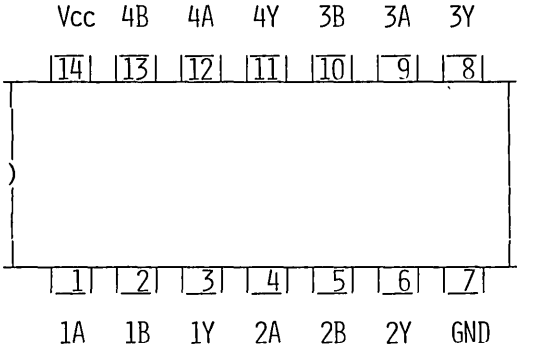
* QUAD 2-INPUT NAND GATES
* ADVANCED OXIDE-ISOLATED, ION-IMPLANTED SCHOTTKY TTL PROCESS
* FUNCTIONALLY AND PIN-FOR-PIN COMPATIBLE WITH TTL COUNTERPART
* IMPROVED AC PERFORMANCE OVER LS COUNTERPART AT HALF THE POWER
* SWITCHING SPECIFICATIONS AT 50 pF
* IMPROVED INPUT THRESHOLD VOLTAGE
* IMPROVED LINE RECEIVING CHARACTERISTICS

J OR N PACKAGE

POSITIVE LOGIC: $Y=\overline{AB}$



THIS ADVANCED LOW-POWER SCHOTTKY DEVICE HAS BEEN FABRICATED BY AN ADVANCED OXIDE-ISOLATED, ION-IMPLANTED SCHOTTKY TTL PROCESS DEVELOPED BY TI. THE MAJOR BENEFIT OF THIS PROCESS IS THE IMPROVEMENT OF THE SPEED-POWER PRODUCT BY THE REDUCTION OF PARASITIC AND SIDE-WALL CAPACITANCE AND ENHANCED f_T. THE ALS FAMILY FEATURES THE SAME OUTPUT DRIVE CHARACTERISTICS AS THE LS FAMILY.

FOR ABSOLUTE MAXIMUM RATINGS, RECOMMENDED OPERATING CONDITIONS, AND DC ELECTRICAL CHARACTERISTICS, SEE PAGES 226 AND 227, STANDARD OUTPUT.

SWITCHING CHARACTERISTICS OVER RECOMMENDED T_A RANGE, V_{CC}=4.5V TO 5.5V, R_L=500 OHMS, C_L=50pF (UNLESS OTHERWISE NOTED). REFER TO PAGE 267 FOR LOAD CIRCUITS & WAVEFORMS.

PARAMETER	SN54ALS/74ALS00* MIN	TYP	MAX	SN54ALS00 MIN	TYP	MAX	SN74ALS00 MIN	TYP	MAX	UNIT
TPLH		4		3		14	3		11	NS
TPHL		5		3		14	3		11	NS

* SN54ALS/74ALS00 VALUES ARE AT V_{CC} = 5V, T_A = 25°C, C_L = 15pF, R_L = 500 OHMS

SUPPLY CURRENT OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (SEE NOTE)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CCH}	SUPPLY CURRENT, OUTPUTS HIGH	V_{CC}=MAX, V_I=0V		0.43	0.85	mA
I_{CCL}	SUPPLY CURRENT, OUTPUTS LOW	V_{CC}=MAX, V_I=4.5V		1.62	3	mA

NOTE: TYPICAL VALUES ARE AT V_{CC} = 5V, T_A = 25°C

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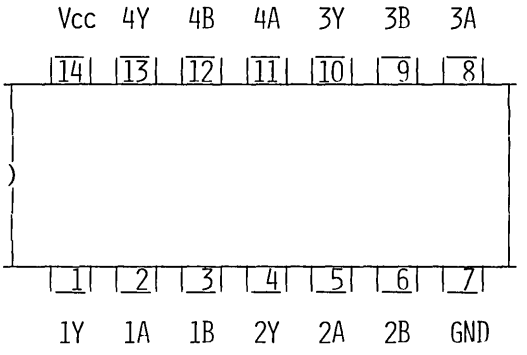
* QUAD 2-INPUT NAND GATES WITH OPEN-COLLECTOR OUTPUTS
* ADVANCED OXIDE-ISOLATED, ION-IMPLANTED SCHOTTKY TTL PROCESS
* FUNCTIONALLY AND PIN-FOR-PIN COMPATIBLE WITH TTL COUNTERPART
* IMPROVED AC PERFORMANCE OVER LS COUNTERPART AT HALF THE POWER
* SWITCHING SPECIFICATIONS AT 50 pF
* IMPROVED INPUT THRESHOLD VOLTAGE
* IMPROVED LINE RECEIVING CHARACTERISTICS

J OR N PACKAGE

POSITIVE LOGIC: $Y=\overline{AB}$



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FOR ABSOLUTE MAXIMUM RATINGS, RECOMMENDED OPERATING CONDITIONS AND DC ELECTRICAL CHARACTERISTICS SEE PAGES 226 AND 227, STANDARD OUTPUT:

SWITCHING CHARACTERISTICS OVER RECOMMENDED T_A RANGE, V_{CC}=4.5V TO 5.5V, R_L=500 OHMS, C_L=50pF (UNLESS OTHERWISE NOTED). REFER TO PAGE 267 FOR LOAD CIRCUITS & WAVEFORMS.

PARAMETER	SN54ALS/74ALS01* MIN	TYP	MAX	SN54ALS01 MIN	TYP	MAX	SN74ALS01 MIN	TYP	MAX	UNIT
TPLH		20		23		59	23		54	NS
TPHL		12		8		29	8		28	NS

* SN54ALS/74ALS01 VALUES ARE AT V_{CC} = 5V, T_A = 25°C, C_L = 15pF, R_L = 500 OHMS

SUPPLY CURRENT OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (SEE NOTE)

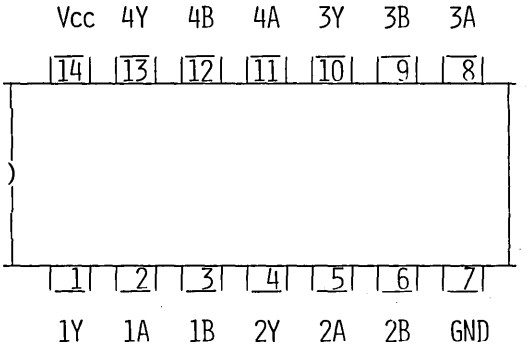
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CCH} SUPPLY CURRENT, OUTPUTS HIGH	V_{CC}=MAX, V_I=0V		0.43	0.85	mA
I_{CCL} SUPPLY CURRENT, OUTPUTS LOW	V_{CC}=MAX, V_I=4.5V		1.62	3	mA

NOTE: TYPICAL VALUES ARE AT V_{CC} = 5V, T_A = 25°C

* QUAD 2-INPUT NOR GATES
* ADVANCED OXIDE-ISOLATED, ION-IMPLANTED SCHOTTKY TTL PROCESS
* FUNCTIONALLY AND PIN-FOR-PIN COMPATIBLE WITH TTL COUNTERPART
* IMPROVED AC PERFORMANCE OVER LS COUNTERPART AT HALF THE POWER
* SWITCHING SPECIFICATIONS AT 50 pF
* IMPROVED INPUT THRESHOLD VOLTAGE
* IMPROVED LINE RECEIVING CHARACTERISTICS

J OR N PACKAGE

POSITIVE LOGIC: $Y=\overline{A+B}$



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FOR ABSOLUTE MAXIMUM RATINGS, RECOMMENDED OPERATING CONDITIONS AND DC ELECTRICAL CHARACTERISTICS SEE PAGE 226 AND 227, STANDARD OUTPUT.

SWITCHING CHARACTERISTICS OVER RECOMMENDED T_A RANGE, V_{CC}=4.5V TO 5.5V, R_L=500 OHMS, C_L=50pF (UNLESS OTHERWISE NOTED). REFER TO PAGE 267 FOR LOAD CIRCUITS & WAVEFORMS.

PARAMETER	SN54ALS/74ALS02* MIN	TYP	MAX	SN54ALS02 MIN	TYP	MAX	SN74ALS02 MIN	TYP	MAX	UNIT
TPLH		6		3		14	3		12	NS
TPHL		5		3		11	3		10	NS

* SN54ALS/74ALS02 VALUES ARE AT V_{CC} = 5V, T_A = 25°C, C_L = 15pF, R_L = 500 OHMS

SUPPLY CURRENT OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (SEE NOTE)

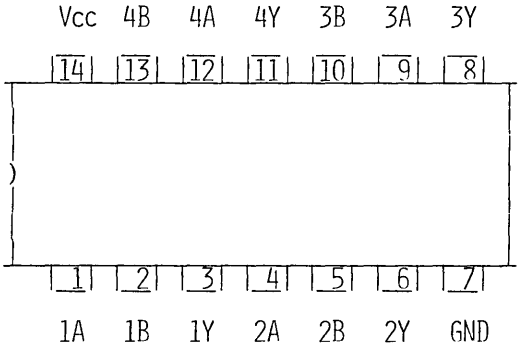
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CCH} SUPPLY CURRENT, OUTPUTS HIGH	V_{CC}=MAX, V_I=0V		0.86	2.2	mA
I_{CCL} SUPPLY CURRENT, OUTPUTS LOW	V_{CC}=MAX, V_I=4.5V		2.16	4	mA

NOTE: TYPICAL VALUES ARE AT V_{CC} = 5V, T_A = 25°C

* QUAD 2-INPUT NAND GATES WITH OPEN-COLLECTOR OUTPUTS
* ADVANCED OXIDE-ISOLATED, ION-IMPLANTED SCHOTTKY TTL PROCESS
* FUNCTIONALLY AND PIN-FOR-PIN COMPATIBLE WITH TTL COUNTERPART
* IMPROVED AC PERFORMANCE OVER LS COUNTERPART AT HALF THE POWER
* SWITCHING SPECIFICATIONS AT 50 pF
* IMPROVED INPUT THRESHOLD VOLTAGE
* IMPROVED LINE RECEIVING CHARACTERISTICS

J OR N PACKAGE

POSITIVE LOGIC: $Y=\overline{AB}$



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FOR ABSOLUTE MAXIMUM RATINGS, RECOMMENDED OPERATING CONDITIONS, AND DC ELECTRICAL CHARACTERISTICS, SEE PAGES 226 AND 227, STANDARD OUTPUT.

SWITCHING CHARACTERISTICS OVER RECOMMENDED T_A RANGE, V_{CC}=4.5V TO 5.5V, R_L=500 OHMS, C_L=50pF (UNLESS OTHERWISE NOTED). REFER TO PAGE 267 FOR LOAD CIRCUITS & WAVEFORMS.

PARAMETER	SN54ALS/74ALS03*			SN54ALS03			SN74ALS03			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TPLH		20		23		59	23		54	NS
TPHL		12		8		29	8		28	NS

* SN54ALS/74ALS03 VALUES ARE AT V_{CC} = 5V, T_A = 25°C, C_L = 15pF, R_L = 500 OHMS

SUPPLY CURRENT OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (SEE NOTE)

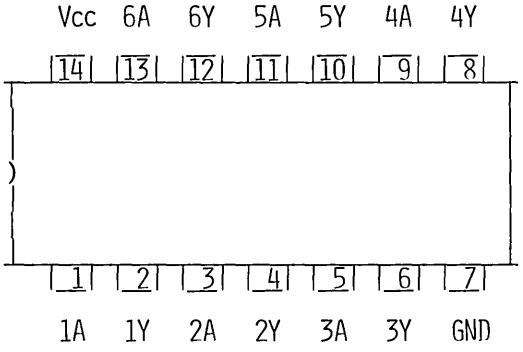
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CCH}	SUPPLY CURRENT, OUTPUTS HIGH	V_{CC}=MAX, V_I=0V		0.43	0.85	mA
I_{CCL}	SUPPLY CURRENT, OUTPUTS LOW	V_{CC}=MAX, V_I=4.5V		1.62	3	mA

NOTE: TYPICAL VALUES ARE AT V_{CC} = 5V, T_A = 25°C

* HEX INVERTERS
* ADVANCED OXIDE-ISOLATED, ION-IMPLANTED SCHOTTKY TTL PROCESS
* FUNCTIONALLY AND PIN-FOR-PIN COMPATIBLE WITH TTL COUNTERPART
* IMPROVED AC PERFORMANCE OVER LS COUNTERPART AT HALF THE POWER
* SWITCHING SPECIFICATIONS AT **50 pF**
* IMPROVED INPUT THRESHOLD VOLTAGE
* IMPROVED LINE RECEIVING CHARACTERISTICS

J OR N PACKAGE

POSITIVE LOGIC: $Y=\overline{A}$



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FOR ABSOLUTE MAXIMUM RATINGS, RECOMMENDED OPERATING CONDITIONS, AND DC ELECTRICAL CHARACTERISTICS, SEE PAGES 226 AND 227, STANDARD OUTPUT.

SWITCHING CHARACTERISTICS OVER RECOMMENDED T_A RANGE, V_{CC}=4.5V TO 5.5V, R_L=500 OHMS, C_L=50pF (UNLESS OTHERWISE NOTED). REFER TO PAGE 267 FOR LOAD CIRCUITS & WAVEFORMS.

PARAMETER	SN54ALS/74ALS04*			SN54ALS04			SN74ALS04			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TPLH		4		3		14	3		11	NS
TPHL		3		2		12	2		9	NS

* SN54ALS/74ALS04 VALUES ARE AT V_{CC} = 5V, T_A = 25°C, C_L = 15pF, R_L = 500 OHMS

SUPPLY CURRENT OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (SEE NOTE)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CCH} SUPPLY CURRENT, OUTPUTS HIGH	V_{CC}=MAX, V_I=0V		0.65	1.1	mA
I_{CCL} SUPPLY CURRENT, OUTPUTS LOW	V_{CC}=MAX, V_I=4.5V		2.4	3.8	mA

NOTE: TYPICAL VALUES ARE AT V_{CC} = 5V, T_A = 25°C

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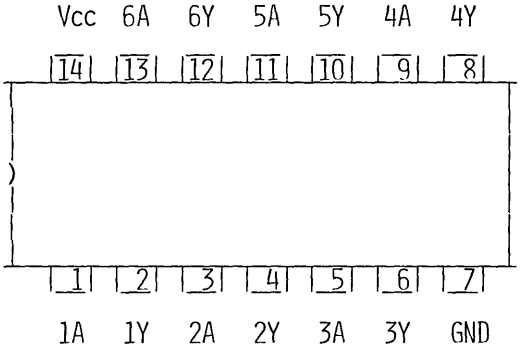
* HEX INVERTERS WITH OPEN-COLLECTOR OUTPUTS
* ADVANCED OXIDE-ISOLATED, ION-IMPLANTED SCHOTTKY TTL PROCESS
* FUNCTIONALLY AND PIN-FOR-PIN COMPATIBLE WITH TTL COUNTERPART
* IMPROVED AC PERFORMANCE OVER LS COUNTERPART AT HALF THE POWER
* SWITCHING SPECIFICATIONS AT 50 pF
* IMPROVED INPUT THRESHOLD VOLTAGE
* IMPROVED LINE RECEIVING CHARACTERISTICS

J OR N PACKAGE

POSITIVE LOGIC: $Y=\overline{A}$



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THIS ADVANCED LOW-POWER SCHOTTKY DEVICE HAS BEEN FABRICATED BY AN ADVANCED OXIDE-ISOLATED, ION-IMPLANTED SCHOTTKY TTL PROCESS DEVELOPED BY TI. THE MAJOR BENEFIT OF THIS PROCESS IS THE IMPROVEMENT OF THE SPEED-POWER PRODUCT BY THE REDUCTION OF PARASITIC AND SIDE-WALL CAPACITANCE AND ENHANCED F_T. THE ALS FAMILY FEATURES THE SAME OUTPUT DRIVE CHARACTERISTICS AS THE LS FAMILY.

FOR ABSOLUTE MAXIMUM RATINGS, RECOMMENDED OPERATING CONDITIONS, AND DC ELECTRICAL CHARACTERISTICS, SEE PAGES 226 AND 227, STANDARD OUTPUT.

SWITCHING CHARACTERISTICS OVER RECOMMENDED T_A RANGE, V_{CC}=4.5V TO 5.5V, R_L=500 OHMS, C_L=50pF (UNLESS OTHERWISE NOTED). REFER TO PAGE 267 FOR LOAD CIRCUITS & WAVEFORMS.

PARAMETER	SN54ALS/74ALS05*			SN54ALS05			SN74ALS05			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TPLH		20		23		59	23		54	NS
TPHL		7		7		29	7		23	NS

* SN54ALS/74ALS05 VALUES ARE AT V_{CC} = 5V, T_A = 25°C, C_L = 15pF, R_L = 500 OHMS

SUPPLY CURRENT OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (SEE NOTE)

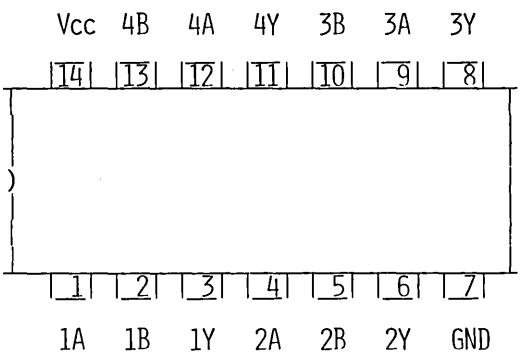
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CCH}	SUPPLY CURRENT, OUTPUTS HIGH	V_{CC}=MAX, V_I=0V		0.65	1.1	mA
I_{CCL}	SUPPLY CURRENT, OUTPUTS LOW	V_{CC}=MAX, V_I=4.5V		2.4	3.8	mA

NOTE: TYPICAL VALUES ARE AT V_{CC} = 5V, T_A = 25°C

* QUAD 2-INPUT AND GATES
* ADVANCED OXIDE-ISOLATED, ION-IMPLANTED SCHOTTKY TTL PROCESS
* FUNCTIONALLY AND PIN-FOR-PIN COMPATIBLE WITH TTL COUNTERPART
* IMPROVED AC PERFORMANCE OVER LS COUNTERPART AT HALF THE POWER
* SWITCHING SPECIFICATIONS AT 50 pF
* IMPROVED INPUT THRESHOLD VOLTAGE
* IMPROVED LINE RECEIVING CHARACTERISTICS

J OR N PACKAGE

POSITIVE LOGIC: Y=AB



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FOR ABSOLUTE MAXIMUM RATINGS, RECOMMENDED OPERATING CONDITIONS, AND DC ELECTRICAL CHARACTERISTICS, SEE PAGES 226 AND 227, STANDARD OUTPUT.

SWITCHING CHARACTERISTICS OVER RECOMMENDED T_A RANGE, V_{CC}=4.5V TO 5.5V, R_L=500 OHMS, C_L=50pF (UNLESS OTHERWISE NOTED). REFER TO PAGE 267 FOR LOAD CIRCUITS & WAVEFORMS.

PARAMETER	SN54ALS/74ALS08*			SN54ALS08			SN74ALS08			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TPLH		8		4		16	4		14	NS
TPHL		5		3		12	3		10	NS

* SN54ALS/74ALS08 VALUES ARE AT V_{CC} = 5V, T_A = 25°C, C_L = 15pF, R_L = 500 OHMS

SUPPLY CURRENT OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (SEE NOTE)

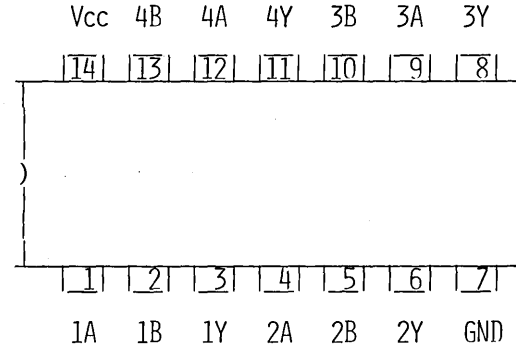
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CCH}	SUPPLY CURRENT, OUTPUTS HIGH	V_{CC}=MAX, V_I=4.5V		1.3	2.4	mA
I_{CCL}	SUPPLY CURRENT, OUTPUTS LOW	V_{CC}=MAX, V_I=0V		2.2	4	mA

NOTE: TYPICAL VALUES ARE AT V_{CC} = 5V, T_A = 25°C

* QUAD 2-INPUT AND GATES WITH OPEN-COLLECTOR OUTPUTS
* ADVANCED OXIDE-ISOLATED, ION-IMPLANTED SCHOTTKY TTL PROCESS
* FUNCTIONALLY AND PIN-FOR-PIN COMPATIBLE WITH TTL COUNTERPART
* IMPROVED AC PERFORMANCE OVER LS COUNTERPART AT HALF THE POWER
* SWITCHING SPECIFICATIONS AT 50 pF
* IMPROVED INPUT THRESHOLD VOLTAGE
* IMPROVED LINE RECEIVING CHARACTERISTICS

J OR N PACKAGE

POSITIVE LOGIC: Y=AB



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FOR ABSOLUTE MAXIMUM RATINGS, RECOMMENDED OPERATING CONDITIONS, AND DC ELECTRICAL CHARACTERISTICS, SEE PAGES 226 AND 227, STANDARD OUTPUT.

SWITCHING CHARACTERISTICS OVER RECOMMENDED T_A RANGE, V_{CC}=4.5V TO 5.5V, R_L=500 OHMS, C_L=50pF (UNLESS OTHERWISE NOTED). REFER TO PAGE 267 FOR LOAD CIRCUITS & WAVEFORMS.

PARAMETER	SN54ALS/74ALS09*			SN54ALS09			SN74ALS09			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TPLH		20		23		59	23		54	NS
TPHL		10		5		17	5		15	NS

* SN54ALS/74ALS09 VALUES ARE AT V_{CC} = 5V, T_A = 25°C, C_L = 15pF, R_L = 500 OHMS

SUPPLY CURRENT OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (SEE NOTE)

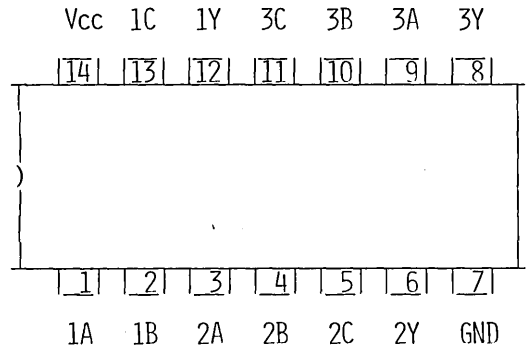
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CCH} SUPPLY CURRENT, OUTPUTS HIGH	V_{CC}=MAX, V_I=4.5V		1.35	2.4	mA
I_{CCL} SUPPLY CURRENT, OUTPUTS LOW	V_{CC}=MAX, V_I=0V		2.2	4	mA

NOTE: TYPICAL VALUES ARE AT V_{CC} = 5V, T_A = 25°C

* TRIPLE 3-INPUT NAND GATES
* ADVANCED OXIDE-ISOLATED, ION-IMPLANTED SCHOTTKY TTL PROCESS
* FUNCTIONALLY AND PIN-FOR-PIN COMPATIBLE WITH TTL COUNTERPART
* IMPROVED AC PERFORMANCE OVER LS COUNTERPART AT HALF THE POWER
* SWITCHING SPECIFICATIONS AT 50 pF
* IMPROVED INPUT THRESHOLD VOLTAGE
* IMPROVED LINE RECEIVING CHARACTERISTICS

J OR N PACKAGE

POSITIVE LOGIC: $Y=\overline{ABC}$



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FOR ABSOLUTE MAXIMUM RATINGS, RECOMMENDED OPERATING CONDITIONS, AND DC ELECTRICAL CHARACTERISTICS, SEE PAGES 226 AND 227, STANDARD OUTPUT.

SWITCHING CHARACTERISTICS OVER RECOMMENDED T_A RANGE, V_{CC}=4.5V TO 5.5V, R_L=500 OHMS, C_L=50pF (UNLESS OTHERWISE NOTED). REFER TO PAGE 267 FOR LOAD CIRCUITS & WAVEFORMS.

PARAMETER	SN54ALS/74ALS10*			SN54ALS10			SN74ALS10			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TPLH		4		3		14	3		11	NS
TPHL		10		4		21	4		18	NS

* SN54ALS/74ALS10 VALUES ARE AT V_{CC} = 5V, T_A = 25°C, C_L = 15pF, R_L = 500 OHMS

SUPPLY CURRENT OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (SEE NOTE)

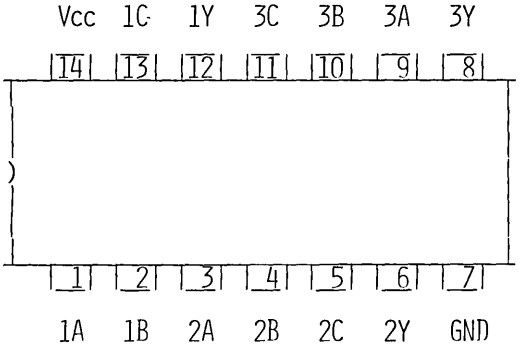
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CCH}	SUPPLY CURRENT, OUTPUTS HIGH	V_{CC}=MAX, V_I=0V		0.32	0.6	mA
I_{CCL}	SUPPLY CURRENT, OUTPUTS LOW	V_{CC}=MAX, V_I=4.5V		1.2	2.2	mA

NOTE: TYPICAL VALUES ARE AT V_{CC} = 5V, T_A = 25°C

* TRIPLE 3-INPUT AND GATES
* ADVANCED OXIDE-ISOLATED, ION-IMPLANTED SCHOTTKY TTL PROCESS
* FUNCTIONALLY AND PIN-FOR-PIN COMPATIBLE WITH TTL COUNTERPART
* IMPROVED AC PERFORMANCE OVER LS COUNTERPART AT HALF THE POWER
* SWITCHING SPECIFICATIONS AT 50 pF
* IMPROVED INPUT THRESHOLD VOLTAGE
* IMPROVED LINE RECEIVING CHARACTERISTICS

J OR N PACKAGE

POSITIVE LOGIC: Y=ABC



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FOR ABSOLUTE MAXIMUM RATINGS, RECOMMENDED OPERATING CONDITIONS, AND DC ELECTRICAL CHARACTERISTICS, SEE PAGES 226 AND 227, STANDARD OUTPUT.

SWITCHING CHARACTERISTICS OVER RECOMMENDED T_A RANGE, V_{CC}=4.5V TO 5.5V, R_L=500 OHMS, C_L=50pF (UNLESS OTHERWISE NOTED). REFER TO PAGE 267 FOR LOAD CIRCUITS & WAVEFORMS.

PARAMETER	SN54ALS/74ALS11*			SN54ALS11			SN74ALS11			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TPLH		12		5		23	5		20	NS
TPHL		6		3		12	3		10	NS

* SN54ALS/74ALS11 VALUES ARE AT V_{CC} = 5V, T_A = 25°C, C_L = 15pF, R_L = 500 OHMS

SUPPLY CURRENT OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (SEE NOTE)

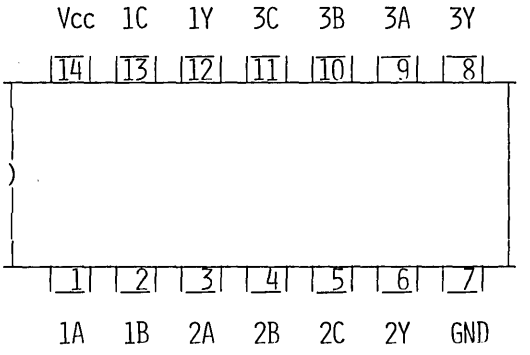
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CCH} SUPPLY CURRENT, OUTPUTS HIGH	V_{CC}=MAX, V_I=4.5V		1	1.8	mA
I_{CCL} SUPPLY CURRENT, OUTPUTS LOW	V_{CC}=MAX, V_I=0V		1.6	3	mA

NOTE: TYPICAL VALUES ARE AT V_{CC} = 5V, T_A = 25°C

* TRIPLE 3-INPUT NAND GATES WITH OPEN-COLLECTOR OUTPUTS
* ADVANCED OXIDE-ISOLATED, ION-IMPLANTED SCHOTTKY TTL PROCESS
* FUNCTIONALLY AND PIN-FOR-PIN COMPATIBLE WITH TTL COUNTERPART
* IMPROVED AC PERFORMANCE OVER LS COUNTERPART AT HALF THE POWER
* SWITCHING SPECIFICATIONS AT 50 pF
* IMPROVED INPUT THRESHOLD VOLTAGE
* IMPROVED LINE RECEIVING CHARACTERISTICS

J OR N PACKAGE

POSITIVE LOGIC: $Y=\overline{ABC}$



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FOR ABSOLUTE MAXIMUM RATINGS, RECOMMENDED OPERATING CONDITIONS, AND DC ELECTRICAL CHARACTERISTICS, SEE PAGES 226 AND 227, STANDARD OUTPUT.

SWITCHING CHARACTERISTICS OVER RECOMMENDED T_A RANGE, V_{CC}=4.5V TO 5.5V, R_L=500 OHMS, C_L=50pF (UNLESS OTHERWISE NOTED). REFER TO PAGE 267 FOR LOAD CIRCUITS & WAVEFORMS.

PARAMETER	SN54ALS/74ALS12*			SN54ALS12			SN74ALS12			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TPLH		20		23		59	23		54	NS
TPHL		15		9		37	9		30	NS

* SN54ALS/74ALS12 VALUES ARE AT V_{CC} = 5V, T_A = 25°C, C_L = 15pF, R_L = 500 OHMS

SUPPLY CURRENT OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (SEE NOTE)

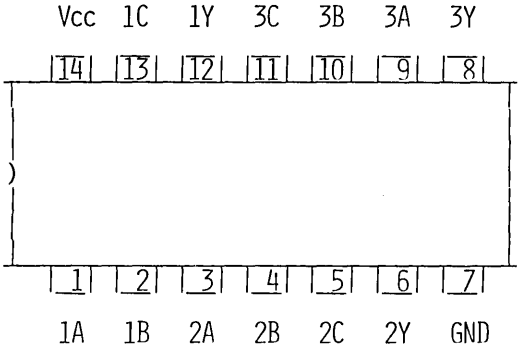
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CCH}	SUPPLY CURRENT, OUTPUTS HIGH	V_{CC}=MAX, V_I=0V		0.32	0.6	mA
I_{CCL}	SUPPLY CURRENT, OUTPUTS LOW	V_{CC}=MAX, V_I=4.5V		1.2	2.2	mA

NOTE: TYPICAL VALUES ARE AT V_{CC} = 5V, T_A = 25°C

* TRIPLE 3-INPUT AND GATES WITH OPEN-COLLECTOR OUTPUTS
* ADVANCED OXIDE-ISOLATED, ION-IMPLANTED SCHOTTKY TTL PROCESS
* FUNCTIONALLY AND PIN-FOR-PIN COMPATIBLE WITH TTL COUNTERPART
* IMPROVED AC PERFORMANCE OVER LS COUNTERPART AT HALF THE POWER
* SWITCHING SPECIFICATIONS AT 50 pF
* IMPROVED INPUT THRESHOLD VOLTAGE
* IMPROVED LINE RECEIVING CHARACTERISTICS

J OR N PACKAGE

POSITIVE LOGIC: Y=ABC



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FOR ABSOLUTE MAXIMUM RATINGS, RECOMMENDED OPERATING CONDITIONS, AND DC ELECTRICAL CHARACTERISTICS, SEE PAGES 226 AND 227, STANDARD OUTPUT.

SWITCHING CHARACTERISTICS OVER RECOMMENDED T_A RANGE, V_{CC}=4.5V TO 5.5V, R_L=500 OHMS, C_L=50pF (UNLESS OTHERWISE NOTED). REFER TO PAGE 267 FOR LOAD CIRCUITS & WAVEFORMS.

PARAMETER	SN54ALS/74ALS15*			SN54ALS15			SN74ALS15			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TPLH		20		23		59	23		54	NS
TPHL		10		6		14	6		13	NS

* SN54ALS/74ALS15 VALUES ARE AT V_{CC} = 5V, T_A = 25°C, C_L = 15pF, R_L = 500 OHMS

SUPPLY CURRENT OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (SEE NOTE)

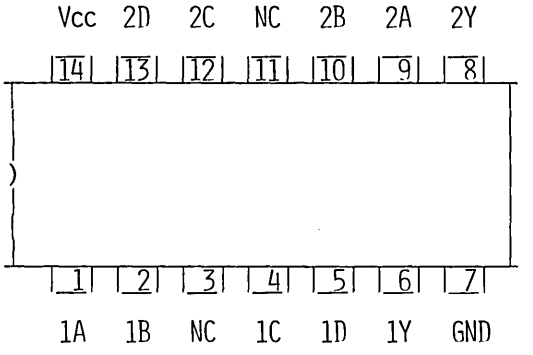
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CCH} SUPPLY CURRENT, OUTPUTS HIGH	V_{CC}=MAX, V_I=4.5V		1	1.8	mA
I_{CCL} SUPPLY CURRENT, OUTPUTS LOW	V_{CC}=MAX, V_I=0V		1.66	3	mA

NOTE: TYPICAL VALUES ARE AT V_{CC} = 5V, T_A = 25°C

* DUAL 4-INPUT NAND GATES
* ADVANCED OXIDE-ISOLATED, ION-IMPLANTED SCHOTTKY TTL PROCESS
* FUNCTIONALLY AND PIN-FOR-PIN COMPATIBLE WITH TTL COUNTERPART
* IMPROVED AC PERFORMANCE OVER LS COUNTERPART AT HALF THE POWER
* SWITCHING SPECIFICATIONS AT 50 pF
* IMPROVED INPUT THRESHOLD VOLTAGE
* IMPROVED LINE RECEIVING CHARACTERISTICS

J OR N PACKAGE

POSITIVE LOGIC: $Y=\overline{ABCD}$



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FOR ABSOLUTE MAXIMUM RATINGS, RECOMMENDED OPERATING CONDITIONS, AND DC ELECTRICAL CHARACTERISTICS, SEE PAGES 226 AND 227, STANDARD OUTPUT.

SWITCHING CHARACTERISTICS OVER RECOMMENDED T_A RANGE, V_{CC}=4.5V TO 5.5V, R_L=500 OHMS, C_L=50pF (UNLESS OTHERWISE NOTED). REFER TO PAGE 267 FOR LOAD CIRCUITS & WAVEFORMS.

PARAMETER	SN54ALS/74ALS20* MIN	TYP	MAX	SN54ALS20 MIN	TYP	MAX	SN74ALS20 MIN	TYP	MAX	UNIT
TPLH		4		3		14	3		11	NS
TPHL		15		5		28	5		25	NS

* SN54ALS/74ALS20 VALUES ARE AT V_{CC} = 5V, T_A = 25°C, C_L = 15pF, R_L = 500 OHMS

SUPPLY CURRENT OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (SEE NOTE)

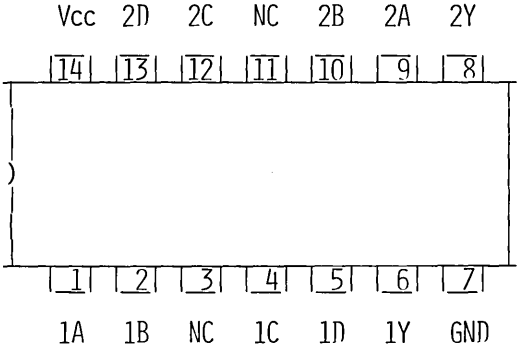
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CCH}	SUPPLY CURRENT, OUTPUTS HIGH	V_{CC}=MAX, V_I=0V		0.22	0.4	mA
I_{CCL}	SUPPLY CURRENT, OUTPUTS LOW	V_{CC}=MAX, V_I=4.5V		0.81	1.5	mA

NOTE: TYPICAL VALUES ARE AT V_{CC} = 5V, T_A = 25°C

* DUAL 4-INPUT AND GATES
* ADVANCED OXIDE-ISOLATED, ION-IMPLANTED SCHOTTKY TTL PROCESS
* FUNCTIONALLY AND PIN-FOR-PIN COMPATIBLE WITH TTL COUNTERPART
* IMPROVED AC PERFORMANCE OVER LS COUNTERPART AT HALF THE POWER
* SWITCHING SPECIFICATIONS AT **50 pF**
* IMPROVED INPUT THRESHOLD VOLTAGE
* IMPROVED LINE RECEIVING CHARACTERISTICS

J OR N PACKAGE

POSITIVE LOGIC: Y=ABCD



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SWITCHING CHARACTERISTICS OVER RECOMMENDED T_A RANGE, V_{CC}=4.5V TO 5.5V, R_L=500 OHMS, C_L=50pF (UNLESS OTHERWISE NOTED). REFER TO PAGE 267 FOR LOAD CIRCUITS & WAVEFORMS.

PARAMETER	SN54ALS/74ALS21* MIN	TYP	MAX	SN54ALS21 MIN	TYP	MAX	SN74ALS21 MIN	TYP	MAX	UNIT
TPLH		12		6		30	6		26	NS
TPHL		5		3		12	3		10	NS

* SN54ALS/74ALS21 VALUES ARE AT V_{CC} = 5V, T_A = 25°C, C_L = 15pF, R_L = 500 OHMS

SUPPLY CURRENT OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (SEE NOTE)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CCH} SUPPLY CURRENT, OUTPUTS HIGH	V_{CC}=MAX, V_I=4.5V		0.67	1.2	mA
I_{CCL} SUPPLY CURRENT, OUTPUTS LOW	V_{CC}=MAX, V_I=0V		1.1	2	mA

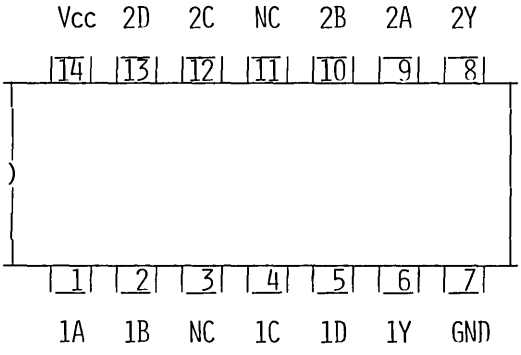
NOTE: TYPICAL VALUES ARE AT V_{CC} = 5V, T_A = 25°C

* DUAL 4-INPUT NAND GATES WITH OPEN-COLLECTOR OUTPUTS
* ADVANCED OXIDE-ISOLATED, ION-IMPLANTED SCHOTTKY TTL PROCESS
* FUNCTIONALLY AND PIN-FOR-PIN COMPATIBLE WITH TTL COUNTERPART

  IMPROVED AC PERFORMANCE OVER LS COUNTERPART AT HALF THE POWER
* SWITCHING SPECIFICATIONS AT **50 pF**
* IMPROVED INPUT THRESHOLD VOLTAGE
* IMPROVED LINE RECEIVING CHARACTERISTICS

J OR N PACKAGE

POSITIVE LOGIC: $Y=\overline{ABCD}$



THIS ADVANCED LOW-POWER SCHOTTKY DEVICE HAS BEEN FABRICATED BY AN ADVANCED OXIDE-ISOLATED, ION-IMPLANTED SCHOTTKY TTL PROCESS DEVELOPED BY TI. THE MAJOR BENEFIT OF THIS PROCESS IS THE IMPROVEMENT OF THE SPEED-POWER PRODUCT BY THE REDUCTION OF PARASITIC AND SIDE-WALL CAPACITANCE AND ENHANCED f_T. THE ALS FAMILY FEATURES THE SAME OUTPUT DRIVE CHARACTERISTICS AS THE LS FAMILY.

FOR ABSOLUTE MAXIMUM RATINGS, RECOMMENDED OPERATING CONDITIONS, AND DC ELECTRICAL CHARACTERISTICS, SEE PAGES 226 AND 227, STANDARD OUTPUT.

SWITCHING CHARACTERISTICS OVER RECOMMENDED T_A RANGE, V_{CC}=4.5V TO 5.5V, R_L=500 OHMS, C_L=50pF (UNLESS OTHERWISE NOTED). REFER TO PAGE 267 FOR LOAD CIRCUITS & WAVEFORMS.

PARAMETER	SN54ALS/74ALS22*			SN54ALS22			SN74ALS22			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TPLH		20		23		59	23		54	NS
TPHL		19		13		42	13		37	NS

* SN54ALS/74ALS22 VALUES ARE AT V_{CC} = 5V, T_A = 25°C, C_L = 15pF, R_L = 500 OHMS

SUPPLY CURRENT OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (SEE NOTE)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CCH}	SUPPLY CURRENT, OUTPUTS HIGH	V_{CC}=MAX, V_I=0V		0.22	0.4	mA
I_{CCL}	SUPPLY CURRENT, OUTPUTS LOW	V_{CC}=MAX, V_I=4.5V		0.8	1.5	mA

NOTE: TYPICAL VALUES ARE AT V_{CC} = 5V, T_A = 25°C

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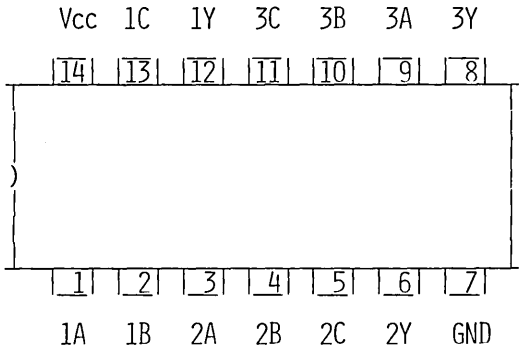
* TRIPLE 3-INPUT NOR GATES
* ADVANCED OXIDE-ISOLATED, ION-IMPLANTED SCHOTTKY TTL PROCESS
* FUNCTIONALLY AND PIN-FOR-PIN COMPATIBLE WITH TTL COUNTERPART
* IMPROVED AC PERFORMANCE OVER LS COUNTERPART AT HALF THE POWER
* SWITCHING SPECIFICATIONS AT **50 pF**
* IMPROVED INPUT THRESHOLD VOLTAGE
* IMPROVED LINE RECEIVING CHARACTERISTICS

J OR N PACKAGE

POSITIVE LOGIC: $Y=\overline{A+B+C}$



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FOR ABSOLUTE MAXIMUM RATINGS, RECOMMENDED OPERATING CONDITIONS, AND DC ELECTRICAL CHARACTERISTICS, SEE PAGES 226 AND 227, STANDARD OUTPUT.

SWITCHING CHARACTERISTICS OVER RECOMMENDED T_A RANGE, V_{CC}=4.5V TO 5.5V, R_L=500 OHMS, C_L=50pF (UNLESS OTHERWISE NOTED). REFER TO PAGE 267 FOR LOAD CIRCUITS & WAVEFORMS.

PARAMETER	SN54ALS/74ALS27* MIN	TYP	MAX	SN54ALS27 MIN	TYP	MAX	SN74ALS27 MIN	TYP	MAX	UNIT
TPLH		9		4		22	4		15	NS
TPHL		3		3		10	3		9	NS

* SN54ALS/74ALS27 VALUES ARE AT V_{CC} = 5V, T_A = 25°C, C_L = 15pF, R_L = 500 OHMS

SUPPLY CURRENT OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (SEE NOTE)

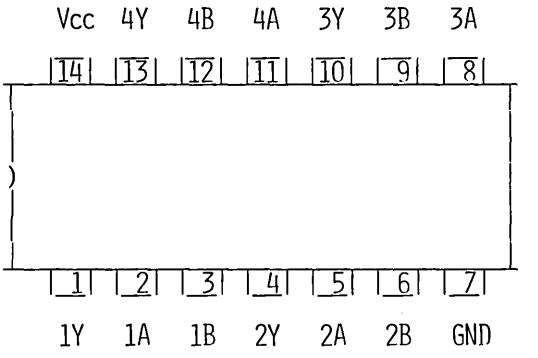
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CCH} SUPPLY CURRENT, OUTPUTS HIGH	V_{CC}=MAX, V_I=0V		0.97	1.8	mA
I_{CCL} SUPPLY CURRENT, OUTPUTS LOW	V_{CC}=MAX, V_I=4.5V		2	4	mA

NOTE: TYPICAL VALUES ARE AT V_{CC} = 5V, T_A = 25°C

* QUAD 2-INPUT NOR BUFFERS
* ADVANCED OXIDE-ISOLATED, ION-IMPLANTED SCHOTTKY TTL PROCESS
* FUNCTIONALLY AND PIN-FOR-PIN COMPATIBLE WITH TTL COUNTERPART
* IMPROVED AC PERFORMANCE OVER LS COUNTERPART AT HALF THE POWER
* SWITCHING SPECIFICATIONS AT 50 pF
* IMPROVED INPUT THRESHOLD VOLTAGE
* IMPROVED LINE RECEIVING CHARACTERISTICS

J OR N PACKAGE

POSITIVE LOGIC: $Y=\overline{A+B}$



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FOR ABSOLUTE MAXIMUM RATINGS, RECOMMENDED OPERATING CONDITIONS, AND DC ELECTRICAL CHARACTERISTICS, SEE PAGES 226 AND 227, BUFFER OUTPUT.

SWITCHING CHARACTERISTICS OVER RECOMMENDED T_A RANGE, V_{CC}=4.5V TO 5.5V, R_L=500 OHMS, C_L=50pF (UNLESS OTHERWISE NOTED). REFER TO PAGE 267 FOR LOAD CIRCUITS & WAVEFORMS.

PARAMETER	SN54ALS/74ALS28*			SN54ALS28			SN74ALS28			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TPLH		4		2		10	2		8	NS
TPHL		4		3		10	3		8	NS

* SN54ALS/74ALS28 VALUES ARE AT V_{CC} = 5V, T_A = 25°C, C_L = 15pF, R_L = 500 OHMS

SUPPLY CURRENT OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (SEE NOTE)

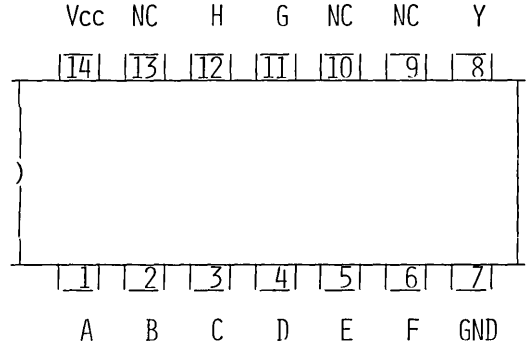
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CCH}	SUPPLY CURRENT, OUTPUTS HIGH	V_{CC}=MAX, V_I=0V		1.7	2.8	mA
I_{CCL}	SUPPLY CURRENT, OUTPUTS LOW	V_{CC}=MAX, V_I=4.5V		4.8	8	mA

NOTE: TYPICAL VALUES ARE AT V_{CC} = 5V, T_A = 25°C

* 8-INPUT NAND GATES
* ADVANCED OXIDE-ISOLATED, ION-IMPLANTED SCHOTTKY TTL PROCESS
* FUNCTIONALLY AND PIN-FOR-PIN COMPATIBLE WITH TTL COUNTERPART
* IMPROVED AC PERFORMANCE OVER LS COUNTERPART AT HALF THE POWER
* SWITCHING SPECIFICATIONS AT **50 pF**
* IMPROVED INPUT THRESHOLD VOLTAGE
* IMPROVED LINE RECEIVING CHARACTERISTICS

J OR N PACKAGE

POSITIVE LOGIC: $Y=\overline{ABCDEFGH}$



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THIS ADVANCED LOW-POWER SCHOTTKY DEVICE HAS BEEN FABRICATED BY AN ADVANCED OXIDE-ISOLATED, ION-IMPLANTED SCHOTTKY TTL PROCESS DEVELOPED BY TI. THE MAJOR BENEFIT OF THIS PROCESS IS THE IMPROVEMENT OF THE SPEED-POWER PRODUCT BY THE REDUCTION OF PARASITIC AND SIDE-WALL CAPACITANCE AND ENHANCED f_T. THE ALS FAMILY FEATURES THE SAME OUTPUT DRIVE CHARACTERISTICS AS THE LS FAMILY.

FOR ABSOLUTE MAXIMUM RATINGS, RECOMMENDED OPERATING CONDITIONS, AND DC ELECTRICAL CHARACTERISTICS, SEE PAGES 226 AND 227, STANDARD OUTPUT.

SWITCHING CHARACTERISTICS OVER RECOMMENDED T_A RANGE, V_{CC}=4.5V TO 5.5V, R_L=500 OHMS, C_L=50pF (UNLESS OTHERWISE NOTED). REFER TO PAGE 267 FOR LOAD CIRCUITS & WAVEFORMS.

PARAMETER	SN54ALS/74ALS30*			SN54ALS30			SN74ALS30			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TPLH		4		3		14	3		11	NS
TPHL		10		5		28	5		25	NS

* SN54ALS/74ALS30 VALUES ARE AT V_{CC} = 5V, T_A = 25°C, C_L = 15pF, R_L = 500 OHMS

SUPPLY CURRENT OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (SEE NOTE)

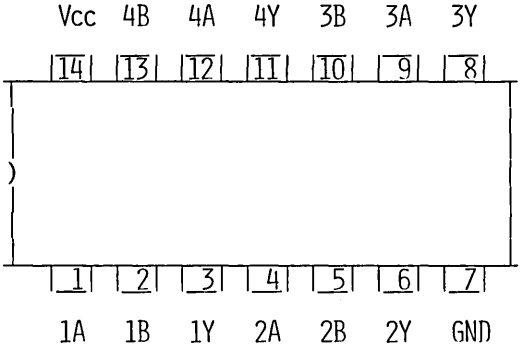
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CCH}	SUPPLY CURRENT, OUTPUTS HIGH	V_{CC}=MAX, V_I=0V		0.22	0.36	mA
I_{CCL}	SUPPLY CURRENT, OUTPUTS LOW	V_{CC}=MAX, V_I=4.5V		0.54	0.9	mA

NOTE: TYPICAL VALUES ARE AT V_{CC} = 5V, T_A = 25°C

* QUAD 2-INPUT OR GATES
* ADVANCED OXIDE-ISOLATED, ION-IMPLANTED SCHOTTKY TTL PROCESS
* FUNCTIONALLY AND PIN-FOR-PIN COMPATIBLE WITH TTL COUNTERPART
* IMPROVED AC PERFORMANCE OVER LS COUNTERPART AT HALF THE POWER
* SWITCHING SPECIFICATIONS AT 50 pF
* IMPROVED INPUT THRESHOLD VOLTAGE
* IMPROVED LINE RECEIVING CHARACTERISTICS

J OR N PACKAGE

POSITIVE LOGIC: Y=A+B



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FOR ABSOLUTE MAXIMUM RATINGS, RECOMMENDED OPERATING CONDITIONS, AND DC ELECTRICAL CHARACTERISTICS, SEE PAGES 226 AND 227, STANDARD OUTPUT.

SWITCHING CHARACTERISTICS OVER RECOMMENDED T_A RANGE, V_{CC}=4.5V TO 5.5V, R_L=500 OHMS, C_L=50pF (UNLESS OTHERWISE NOTED). REFER TO PAGE 267 FOR LOAD CIRCUITS & WAVEFORMS.

PARAMETER	SN54ALS/74ALS32*			SN54ALS32			SN74ALS32			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TPLH		6		3		16	3		14	NS
TPHL		5		3		13	3		12	NS

* SN54ALS/74ALS32 VALUES ARE AT V_{CC} = 5V, T_A = 25°C, C_L = 15pF, R_L = 500 OHMS

SUPPLY CURRENT OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (SEE NOTE)

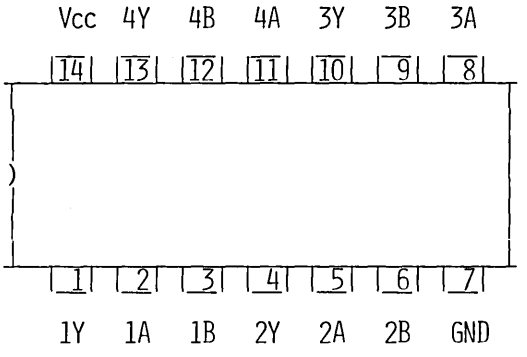
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CCH} SUPPLY CURRENT, OUTPUTS HIGH	V_{CC}=MAX, V_I=4.5V		1.9	4	mA
I_{CCL} SUPPLY CURRENT, OUTPUTS LOW	V_{CC}=MAX, V_I=0V		2.6	4.9	mA

NOTE: TYPICAL VALUES ARE AT V_{CC} = 5V, T_A = 25°C

* QUAD 2-INPUT NOR BUFFERS WITH OPEN-COLLECTOR OUTPUTS
* ADVANCED OXIDE-ISOLATED, ION-IMPLANTED SCHOTTKY TTL PROCESS
* FUNCTIONALLY AND PIN-FOR-PIN COMPATIBLE WITH TTL COUNTERPART
* IMPROVED AC PERFORMANCE OVER LS COUNTERPART AT HALF THE POWER
* SWITCHING SPECIFICATIONS AT 50 pF
* IMPROVED INPUT THRESHOLD VOLTAGE
* IMPROVED LINE RECEIVING CHARACTERISTICS

J OR N PACKAGE

POSITIVE LOGIC: $Y=\overline{A+B}$



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FOR ABSOLUTE MAXIMUM RATINGS, RECOMMENDED OPERATING CONDITIONS, AND DC ELECTRICAL CHARACTERISTICS, SEE PAGES 226 AND 227, BUFFER OUTPUT.

SWITCHING CHARACTERISTICS OVER RECOMMENDED T_A RANGE, V_{CC}=4.5V TO 5.5V, R_L=500 OHMS, C_L=50pF (UNLESS OTHERWISE NOTED). REFER TO PAGE 267 FOR LOAD CIRCUITS & WAVEFORMS.

PARAMETER	SN54ALS/74ALS33*			SN54ALS33			SN74ALS33			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TPLH		20		10		40	10		30	NS
TPHL		9		7		18	7		15	NS

* SN54ALS/74ALS33 VALUES ARE AT V_{CC} = 5V, T_A = 25°C, C_L = 15pF, R_L = 500 OHMS

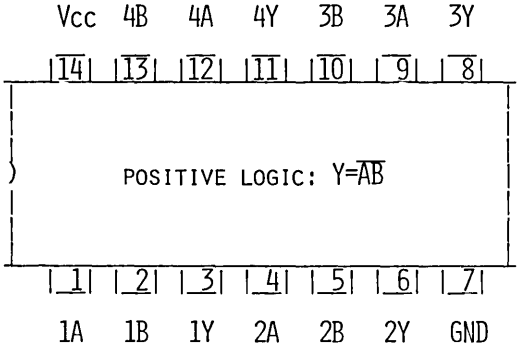
SUPPLY CURRENT OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (SEE NOTE)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CCH} SUPPLY CURRENT, OUTPUTS HIGH	V_{CC}=MAX, V_I=0V		1.7	2.8	mA
I_{CCL} SUPPLY CURRENT, OUTPUTS LOW	V_{CC}=MAX, V_I=4.5V		4.8	8	mA

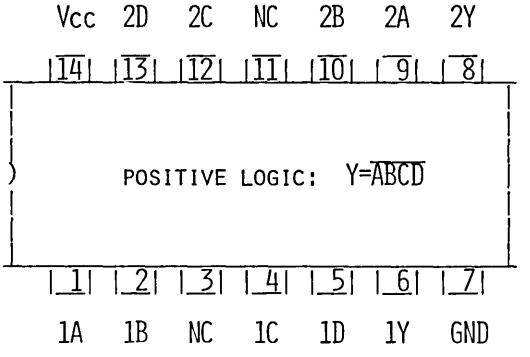
NOTE: TYPICAL VALUES ARE AT V_{CC} = 5V, T_A = 25°C

* 'ALS37 QUAD 2-INPUT NAND BUFFERS
* ADVANCED OXIDE-ISOLATED, ION-IMPLANTED SCHOTTKY TTL PROCESS
* IMPROVED AC PERFORMANCE OVER LS COUNTERPART AT HALF THE POWER
* SWITCHING SPECIFICATIONS AT 50 pF
* 'ALS40 DUAL 4-INPUT NAND BUFFERS
* FUNCTIONALLY AND PIN-FOR-PIN COMPATIBLE WITH TTL COUNTERPARTS
* IMPROVED LINE RECEIVING CHARACTERISTICS
* IMPROVED INPUT THRESHOLD VOLTAGE

'ALS37 . . . J OR N PACKAGE



'ALS40 . . . J OR N PACKAGE



FOR ABSOLUTE MAXIMUM RATINGS, RECOMMENDED OPERATING CONDITIONS, AND DC ELECTRICAL CHARACTERISTICS SEE PAGES 226 AND 227, BUFFER OUTPUT.

SWITCHING CHARACTERISTICS OVER RECOMMENDED T_A RANGE, V_{CC}=4.5V TO 5.5V, R_L=500 OHMS, C_L=50pF (UNLESS OTHERWISE NOTED). REFER TO PAGE 267 FOR LOAD CIRCUITS & WAVEFORMS.

PARAMETER	SN54ALS/74ALS37* MIN	TYP	MAX	SN54ALS37 MIN	TYP	MAX	SN74ALS37 MIN	TYP	MAX	UNIT
TPLH		4		2		10	2		8	NS
TPHL		4		3		10	3		8	NS

PARAMETER	SN54ALS/74ALS40* MIN	TYP	MAX	SN54ALS40 MIN	TYP	MAX	SN74ALS40 MIN	TYP	MAX	UNIT
TPLH		4		2		10	2		8	NS
TPHL		4		3		10	3		8	NS

* SN54ALS/74ALS37 AND SN54ALS/74ALS40 VALUES ARE AT V_{CC} = 5V, T_A = 25°C, C_L = 15pF, R_L = 500 OHMS

SUPPLY CURRENT OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (SEE NOTE)

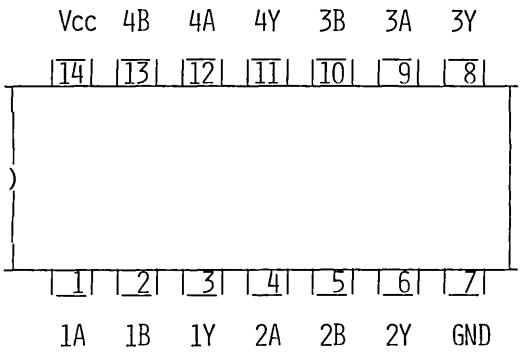
PARAMETER	TEST CONDITIONS	SN54ALS/74ALS37 MIN	TYP	MAX	SN54ALS/74ALS40 MIN	TYP	MAX	UNIT
I_{CCH} SUPPLY CURRENT, OUTPUTS HIGH	V_{CC}=MAX, V_I=0V		0.86	1.6		0.43	0.8	mA
I_{CCL} SUPPLY CURRENT, OUTPUTS LOW	V_{CC}=MAX, V_I=4.5V		4	6.4		2	3.2	mA

NOTE: TYPICAL VALUES ARE AT V_{CC} = 5V, T_A = 25°C

* QUAD 2-INPUT NAND BUFFERS WITH OPEN-COLLECTOR OUTPUTS
* ADVANCED OXIDE-ISOLATED, ION-IMPLANTED SCHOTTKY TTL PROCESS
* FUNCTIONALLY AND PIN-FOR-PIN COMPATIBLE WITH TTL COUNTERPART
* IMPROVED AC PERFORMANCE OVER LS COUNTERPART AT HALF THE POWER
* SWITCHING SPECIFICATIONS AT 50 pF
* IMPROVED INPUT THRESHOLD VOLTAGE
* IMPROVED LINE RECEIVING CHARACTERISTICS

J OR N PACKAGE

POSITIVE LOGIC: $Y=\overline{AB}$



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FOR ABSOLUTE MAXIMUM RATINGS, RECOMMENDED OPERATING CONDITIONS, AND DC ELECTRICAL CHARACTERISTICS, SEE PAGES 226 AND 227, BUFFER OUTPUT.

SWITCHING CHARACTERISTICS OVER RECOMMENDED T_A RANGE, V_{CC}=4.5V TO 5.5V, R_L=500 OHMS, C_L=50pF (UNLESS OTHERWISE NOTED). REFER TO PAGE 267 FOR LOAD CIRCUITS & WAVEFORMS.

PARAMETER	SN54ALS/74ALS38*			SN54ALS38			SN74ALS38			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TPLH		20		10		40	10		30	NS
TPHL		9		7		18	7		15	NS

* SN54ALS/74ALS38 VALUES ARE AT V_{CC} = 5V, T_A = 25°C, C_L = 15pF, R_L = 500 OHMS

SUPPLY CURRENT OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (SEE NOTE)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CCH}	SUPPLY CURRENT, OUTPUTS HIGH	V_{CC}=MAX, V_I=0V		0.86	1.6	mA
I_{CCL}	SUPPLY CURRENT, OUTPUTS LOW	V_{CC}=MAX, V_I=4.5V		4	6.4	mA

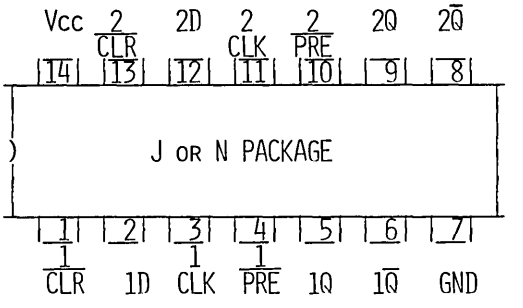
NOTE: TYPICAL VALUES ARE AT V_{CC} = 5V, T_A = 25°C

* DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS
* ADVANCED OXIDE-ISOLATED, ION-IMPLANTED SCHOTTKY TTL PROCESS
* SWITCHING SPECIFICATIONS AT 50 pF
* FUNCTIONALLY AND PIN-FOR-PIN COMPATIBLE WITH TTL COUNTERPART
* IMPROVED AC PERFORMANCE OVER LS COUNTERPART AT HALF THE POWER
* IMPROVED INPUT THTRESHOLD VOLTAGE

FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	L	L	H
H	H	↑	H	H	L
H	H	L	X	Q_0	$\overline{Q}_0$

* THIS CONFIGURATION IS NONSTABLE



FOR ABSOLUTE MAXIMUM RATINGS, RECOMMENDED OPERATING CONDITIONS, AND DC ELECTRICAL CHARACTERISTICS SEE PAGES 226 AND 227, STANDARD OUTPUT.

TIMING REQUIREMENTS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE

		SN54ALS74			SN74ALS74			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
DATA SETUP TIME, t_{su}		15			15			NS
DATA HOLD TIME, t_h		0			0			NS
CLEAR OR PRESET INACTIVE STATE SETUP TIME, t_{su}		10			10			NS
PULSE WIDTH, t_w	CLOCK HIGH	14			12			NS
	CLOCK LOW	19			17			NS
	PRESET OR CLEAR LOW	15			15			NS

SETUP AND HOLD TIMES ARE WITH RESPECT TO LOW-TO-HIGH TRANSITION OF CLOCK

SWITCHING CHARACTERISTICS OVER RECOMMENDED T_A RANGE, V_{CC}=4.5 TO 5.5V, R_L=500 OHMS, C_L=50pF (UNLESS OTHERWISE NOTED). REFER TO PAGE 267 FOR LOAD CIRCUITS & WAVEFORMS.

PARAMETER	FROM	SN54ALS/74ALS74*			SN54ALS74			SN74ALS74			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
FMAX		40	50		30			34			MHZ
TPLH	PRESET OR		6		3		15	3		13	NS
TPHL	CLEAR		10		5		17	5		15	NS
TPLH			8		5		18	5		16	NS
TPHL	CLOCK		12		7		20	7		18	NS

* SN54ALS/74ALS74 VALUES ARE AT V_{CC} = 5V, T_A = 25°C, C_L = 15pF, R_L = 500 OHMS

SUPPLY CURRENT OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (SEE NOTE)

PARAMETER		TEST CONDITIONS	SN54ALS74			SN74ALS74			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	SUPPLY CURRENT	V_{CC}=MAX ¶		2.4	4		2.4	4	MA

NOTE: TYPICAL VALUES ARE AT V_{CC}=5V, T_A=25°C

¶ I_{CC} IS MEASURED WITH OUTPUTS OPEN AND D, CLK, AND $\overline{PRE}$ GROUNDED, THEN WITH D, CLK, AND $\overline{CLR}$ GROUNDED.

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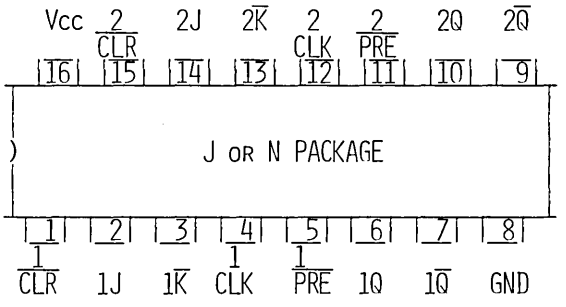
* DUAL J-$\overline{K}$ POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET
* ADVANCED OXIDE-ISOLATED, ION-IMPLANTED SCHOTTKY TTL PROCESS
* SWITCHING SPECIFICATIONS AT 50 pF
* FUNCTIONALLY AND PIN-FOR-PIN COMPATIBLE WITH TTL COUNTERPART
* IMPROVED AC PERFORMANCE OVER LS COUNTERPART
* IMPROVED LINE RECEIVING CHARACTERISTICS AND INPUT THRESHOLD VOLTAGE

FUNCTION TABLE

INPUTS					OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q_0	$\overline{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$

* THIS CONFIGURATION IS NONSTABLE



FOR ABSOLUTE MAXIMUM RATINGS, RECOMMENDED OPERATING CONDITIONS, AND DC ELECTRICAL CHARACTERISTICS SEE PAGES 226 AND 227, STANDARD OUTPUT.

TIMING REQUIREMENTS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE

		SN54ALS109 MIN	SN54ALS109 TYP	SN54ALS109 MAX	SN74ALS109 MIN	SN74ALS109 TYP	SN74ALS109 MAX	UNIT
DATA SETUP TIME, t_{su}		15			15			NS
DATA HOLD TIME, t_h		0			0			NS
CLEAR OR PRESET INACTIVE STATE SETUP TIME, t_{su}		10			10			NS
PULSE WIDTH, t_w	CLOCK HIGH	14			12			NS
	CLOCK LOW	19			17			NS
	PRESET OR CLEAR LOW	15			15			NS

SETUP AND HOLD TIMES ARE WITH RESPECT TO LOW-TO-HIGH TRANSITION OF CLOCK

SWITCHING CHARACTERISTICS OVER RECOMMENDED T_A RANGE, V_{CC}=4.5 TO 5.5V, R_L=500 OHMS, C_L=50pF (UNLESS OTHERWISE NOTED). REFER TO PAGE 267 FOR LOAD CIRCUITS & WAVEFORMS.

PARAMETER	FROM	SN54ALS/74ALS109* MIN	SN54ALS/74ALS109* TYP	SN54ALS/74ALS109* MAX	SN54ALS109 MIN	SN54ALS109 TYP	SN54ALS109 MAX	SN74ALS109 MIN	SN74ALS109 TYP	SN74ALS109 MAX	UNIT
f_{max}		40	50		30			34			MHZ
t_{PLH}	PRESET OR		6		3		15	3		13	NS
t_{PHL}	CLEAR		10		5		17	5		15	NS
t_{PLH}			8		5		18	5		16	NS
t_{PHL}	CLOCK		12		7		20	7		18	NS

* SN54ALS/74ALS109 VALUES ARE AT V_{CC} = 5V, T_A = 25°C, C_L = 15pF, R_L = 500 OHMS

SUPPLY CURRENT OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (SEE NOTE)

PARAMETER		TEST CONDITIONS	SN54ALS109 MIN	SN54ALS109 TYP	SN54ALS109 MAX	SN74ALS109 MIN	SN74ALS109 TYP	SN74ALS109 MAX	UNIT
I_{CC}	SUPPLY CURRENT	V_{CC}=MAX ¶		2.4	4		2.4	4	mA

NOTE: TYPICAL VALUES ARE AT V_{CC}=5V, T_A=25°C

¶ I_{CC} IS MEASURED WITH OUTPUTS OPEN WITH J, $\overline{K}$, CLK, AND $\overline{PRE}$ GROUNDED, THEN WITH J, $\overline{K}$, CLK, AND $\overline{CLR}$ GROUNDED.

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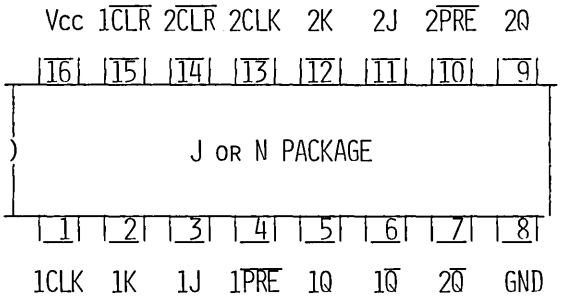
TYPES SN54ALS112 AND SN74ALS112 DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

* DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET
* ADVANCED OXIDE-ISOLATED, ION-IMPLANTED SCHOTTKY TTL PROCESS
* IMPROVED INPUT THRESHOLD VOLTAGE
* FUNCTIONALLY AND PIN-FOR-PIN COMPATIBLE WITH TTL COUNTERPART
* IMPROVED LINE RECEIVING CHARACTERISTICS
* SWITCHING SPECIFICATIONS AT 50 pF

FUNCTION TABLE

INPUTS					OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q}_0$

* THIS CONFIGURATION IS NONSTABLE



FOR ABSOLUTE MAXIMUM RATINGS, RECOMMENDED OPERATING CONDITIONS, AND DC ELECTRICAL CHARACTERISTICS SEE PAGES 226 AND 227, STANDARD OUTPUT.

TIMING REQUIREMENTS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE

		SN54ALS112			SN74ALS112			
		MIN	TYP	MAX	MIN	TYP	MAX	UNIT
DATA SETUP TIME, TSU		25			25			NS
CLR OR PRE INACTIVE STATE SETUP TIME, TSU		20			20			NS
DATA HOLD TIME, TH		0			0			NS
PULSE WIDTH, TW	CLOCK HIGH	30			25			NS
	CLOCK LOW	10			5			NS
	PRESET OR CLEAR LOW	15			15			NS

SETUP AND HOLD TIMES ARE WITH RESPECT TO HIGH-TO-LOW TRANSITION OF CLOCK

SWITCHING CHARACTERISTICS OVER RECOMMENDED T_A RANGE, V_{CC}=4.5 TO 5.5V, R_L=500 OHMS, C_L=50pF (UNLESS OTHERWISE NOTED). REFER TO PAGE 267 FOR LOAD CIRCUITS & WAVEFORMS.

		SN54ALS/74ALS112*			SN54ALS112			SN74ALS112			
PARAMETER	FROM	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
FMAX		35	40		25			30			MHZ
TPLH	CLOCK		10		5		20	5		18	NS
TPHL			15		7		24	7		22	NS
TPLH	PRESET OR CLEAR		10		5		20	5		20	NS
TPHL			15		7		24	7		22	NS

* SN54ALS/74ALS112 VALUES ARE AT V_{CC} = 5V, T_A = 25°C, C_L = 15pF, R_L = 500 OHMS

SUPPLY CURRENT OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (SEE NOTE)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	SUPPLY CURRENT	V_{CC}=MAX ¶		2.4	4.5	MA

NOTE: TYPICAL VALUES ARE AT V_{CC} = 5V, T_A = 25°C

¶ I_{CC} IS MEASURED WITH OUTPUTS OPEN WITH J,K,CLK AND $\overline{PRE}$ GROUNDED, THEN WITH J,K, CLK, AND $\overline{CLR}$ GROUNDED.

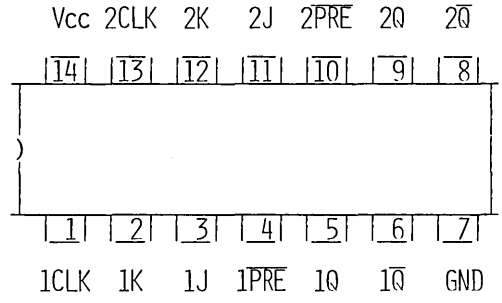
* DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET
* ADVANCED OXIDE-ISOLATED, ION-IMPLANTED SCHOTTKY TTL PROCESS
* IMPROVED INPUT THRESHOLD VOLTAGE
* FUNCTIONALLY AND PIN-FOR-PIN COMPATIBLE WITH TTL COUNTERPART
* IMPROVED LINE RECEIVING CHARACTERISTICS
* SWITCHING SPECIFICATIONS AT 50 pF

FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{PRE}$	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	H	L
H	↓	L	L	Q_0	$\overline{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\overline{Q}_0$

* THIS CONFIGURATION IS NONSTABLE

J OR N PACKAGE



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FOR ABSOLUTE MAXIMUM RATINGS, RECOMMENDED OPERATING CONDITIONS, AND DC ELECTRICAL CHARACTERISTICS SEE PAGES 226 AND 227, STANDARD OUTPUT.

TIMING REQUIREMENTS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE

		SN54ALS113			SN74ALS113			
		MIN	TYP	MAX	MIN	TYP	MAX	UNIT
DATA SETUP TIME, t_{su}		25			25			NS
PRESET INACTIVE STATE SETUP TIME, t_{su}		20			20			NS
DATA HOLD TIME, t_h		0			0			NS
PULSE WIDTH, t_w	CLOCK HIGH	30			25			NS
	CLOCK LOW	10			5			NS
	PRESET LOW	15			15			NS

SETUP AND HOLD TIMES ARE WITH RESPECT TO HIGH-TO-LOW TRANSITION OF CLOCK

SWITCHING CHARACTERISTICS OVER RECOMMENDED T_A RANGE, V_{CC}=4.5 TO 5.5V, R_L=500 OHMS, C_L=50pF (UNLESS OTHERWISE NOTED). REFER TO PAGE 267 FOR LOAD CIRCUITS & WAVEFORMS.

		SN54ALS/74ALS113*			SN54ALS113			SN74ALS113			
PARAMETER	FROM	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
f_{max}		35	40		25			30			MHZ
t_{PLH}	CLOCK		10		5		20	5		18	NS
t_{PHL}			15		7		24	7		22	NS
t_{PLH}	PRESET		10		5		20	5		20	NS
t_{PHL}			15		7		24	7		24	NS

* SN54ALS/74ALS113 VALUES ARE AT V_{CC} = 5V, T_A = 25°C, C_L = 15pF, R_L = 500 OHMS

SUPPLY CURRENT OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (SEE NOTE)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	SUPPLY CURRENT	V_{CC}=MAX ¶		2.4	4.5	MA

NOTE: TYPICAL VALUES ARE AT V_{CC} = 5V, T_A = 25°C

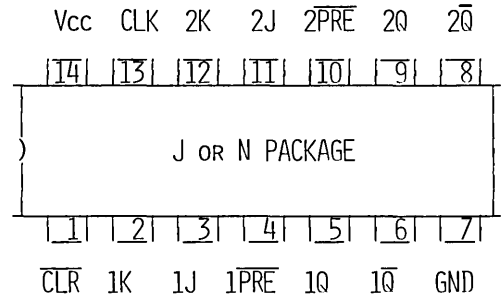
¶ I_{CC} IS MEASURED WITH OUTPUTS OPEN WITH J,K,CLK, AND $\overline{PRE}$ GROUNDED.

* DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET, COMMON CLEAR AND COMMON CLOCK
* ADVANCED OXIDE-ISOLATED, ION-IMPLANTED SCHOTTKY TTL PROCESS
* FUNCTIONALLY AND PIN-FOR-PIN COMPATIBLE WITH TTL COUNTERPART
* IMPROVED LINE RECEIVING CHARACTERISTICS AND INPUT THRESHOLD VOLTAGE
* SWITCHING SPECIFICATIONS AT 50 pF

FUNCTION TABLE

INPUTS					OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q}_0$

* THIS CONFIGURATION IS NONSTABLE



FOR ABSOLUTE MAXIMUM RATINGS, RECOMMENDED OPERATING CONDITIONS, AND DC ELECTRICAL CHARACTERISTICS SEE PAGES 226 AND 227, STANDARD OUTPUT.

TIMING REQUIREMENTS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE

		SN54ALS114			SN74ALS114			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
DATA SETUP TIME, TSU		25			25			NS
CLR OR PRE INACTIVE STATE SETUP TIME, TSU		20			20			NS
DATA HOLD TIME, TH		0			0			NS
PULSE WIDTH, TW	CLOCK HIGH	30			25			NS
	CLOCK LOW	10			5			NS
	PRESET OR CLEAR LOW	15			15			NS

SETUP AND HOLD TIMES ARE WITH RESPECT TO HIGH-TO-LOW TRANSITION OF CLOCK

SWITCHING CHARACTERISTICS OVER RECOMMENDED T_A RANGE, V_{CC}=4.5 TO 5.5V, R_L=500 OHMS, C_L=50pF (UNLESS OTHERWISE NOTED). REFER TO PAGE 267 FOR LOAD CIRCUITS & WAVEFORMS.

PARAMETER	FROM	SN54ALS/74ALS114*			SN54ALS114			SN74ALS114			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
FMAX		35	40		25			30			MHZ
TPLH	CLOCK		10		5		20	5		18	NS
TPHL			15		7		24	7		22	NS
TPLH	PRESET OR CLEAR		10		5		20	5		18	NS
TPHL			15		7		24	7		22	NS

* SN54ALS/74ALS114 VALUES ARE AT V_{CC} = 5V, T_A = 25°C, C_L = 15pF, R_L = 500 OHMS

SUPPLY CURRENT OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (SEE NOTE)

PARAMETER		TEST CONDITIONS	SN54ALS114			SN74ALS114			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	SUPPLY CURRENT	V_{CC}=MAX ¶		2.4	4.5		2.4	4.5	mA

NOTE: TYPICAL VALUES ARE AT V_{CC} = 5V, T_A = 25°C

¶ I_{CC} IS MEASURED WITH OUTPUTS OPEN WITH J,K,CLK AND $\overline{PRE}$ GROUNDED, THEN WITH J,K, CLK, AND $\overline{CLR}$ GROUNDED.

* 13-INPUT NAND GATE
* ADVANCED OXIDE-ISOLATED, ION-IMPLANTED SCHOTTKY TTL PROCESS
* FUNCTIONALLY AND PIN-FOR-PIN COMPATIBLE WITH TTL COUNTERPART
* IMPROVED INPUT THRESHOLD VOLTAGE
* IMPROVED LINE RECEIVING CHARACTERISTICS
* SWITCHING SPECIFICATIONS AT **50 pF**

J OR N PACKAGE

POSITIVE LOGIC: $Y=\overline{ABCDEFGHIJKLM}$

THIS ADVANCED LOW-POWER SCHOTTKY DEVICE HAS BEEN FABRICATED BY AN ADVANCED OXIDE-ISOLATED, ION-IMPLANTED SCHOTTKY TTL PROCESS DEVELOPED BY TI. THE MAJOR BENEFIT OF THIS PROCESS IS THE IMPROVEMENT OF THE SPEED-POWER PRODUCT BY THE REDUCTION OF PARASITIC AND SIDE-WALL CAPACITANCE AND ENHANCED F_T. THE ALS FAMILY FEATURES THE SAME OUTPUT DRIVE CHARACTERISTICS AS THE LS FAMILY.

FOR ABSOLUTE MAXIMUM RATINGS, RECOMMENDED OPERATING CONDITIONS, AND DC ELECTRICAL CHARACTERISTICS, SEE PAGES 226 AND 227, STANDARD OUTPUT.

SWITCHING CHARACTERISTICS OVER RECOMMENDED T_A RANGE, V_{CC}=4.5V TO 5.5V, R_L=500 OHMS, C_L=50pF (UNLESS OTHERWISE NOTED). REFER TO PAGE 267 FOR LOAD CIRCUITS & WAVEFORMS.

PARAMETER	SN54ALS/74ALS133*			SN54ALS133			SN74ALS133			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TPLH		6		3		14	3		11	NS
TPHL		10		5		28	5		25	NS

* SN54ALS/74ALS133 VALUES ARE AT V_{CC} = 5V, T_A = 25°C, C_L = 15pF, R_L = 500 OHMS

SUPPLY CURRENT OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (SEE NOTE)

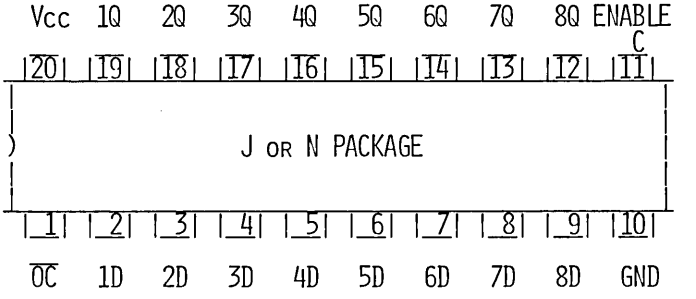
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CCH}	SUPPLY CURRENT, OUTPUTS HIGH	V_{CC}=MAX, V_I=0V		0.24	0.34	mA
I_{CCL}	SUPPLY CURRENT, OUTPUTS LOW	V_{CC}=MAX, V_I=4.5V		0.56	0.8	mA

NOTE: TYPICAL VALUES ARE AT V_{CC} = 5V, T_A = 25°C

* OCTAL D-TYPE TRANSPARENT LATCHES
* ADVANCED OXIDE-ISOLATED, ION-IMPLANTED SCHOTTKY TTL PROCESS
* FUNCTIONALLY EQUIVALENT TO THE 'LS373 AND 'S373
* SWITCHING SPECIFICATIONS AT 50 pF
* BUS-STRUCTURED PINOUTS
* IMPROVED AC PERFORMANCE OVER 'LS373 AT APPROXIMATELY HALF THE POWER
* 3-STATE BUFFER-TYPE OUTPUTS DRIVE BUS LINES DIRECTLY

FUNCTION TABLE

OUTPUT CONTROL	ENABLE C	D	OUTPUT Q
L	H	H	H
L	H	L	L
L	L	X	Q0
H	X	X	Z



FOR ABSOLUTE MAXIMUM RATINGS, RECOMMENDED OPERATING CONDITIONS, AND DC ELECTRICAL CHARACTERISTICS SEE PAGES 226 AND 227, BUFFER OUTPUT.

TIMING REQUIREMENTS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE

	MIN	TYP	MAX	UNIT
DATA SETUP TIME, TSU	10			NS
DATA HOLD TIME, TH	7			NS
WIDTH OF ENABLE PULSE, TW	10			NS

SETUP AND HOLD TIMES ARE WITH RESPECT TO HIGH-TO-LOW TRANSITION OF ENABLE

SWITCHING CHARACTERISTICS OVER RECOMMENDED TA RANGE, Vcc=4.5 TO 5.5V, RL=500 OHMS, CL=50pF (UNLESS OTHERWISE NOTED). REFER TO PAGE 267 FOR LOAD CIRCUITS & WAVEFORMS.

PARAMETER	FROM	SN54ALS/74ALS573* MIN	TYP	MAX	SN54ALS573 MIN	TYP	MAX	SN74ALS573 MIN	TYP	MAX	UNIT
TPLH	DATA	5			2		15	2		12	NS
TPHL	DATA	5			2		15	2		12	NS
TPLH	ENABLE	11			8		27	8		20	NS
TPHL	ENABLE	11			8		20	8		19	NS
TPZH	OUTPUT CONTROL	8			4		21	5		18	NS
TPZL	OUTPUT CONTROL	8			4		21	5		18	NS
TPHZ	OUTPUT CONTROL	3			2		10	2		8	NS
TPLZ	OUTPUT CONTROL	5			3		15	3		13	NS

* SN54ALS/74ALS573 VALUES ARE AT Vcc = 5V, TA = 25°C, CL = 15pF, RL = 500 OHMS

SUPPLY CURRENT OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (SEE NOTE)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ICCH SUPPLY CURRENT, OUTPUTS HIGH	Vcc = MAX, OUTPUTS OPEN		10	14	mA
ICCL SUPPLY CURRENT, OUTPUTS LOW			15	22	mA
ICCZ SUPPLY CURRENT, OUTPUTS DISABLED			15.5	24	mA

NOTE: TYPICAL VALUES ARE AT Vcc = 5V, TA = 25°C

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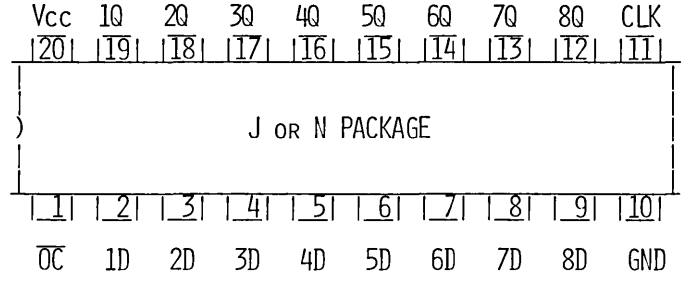
TYPES SN54ALS574 AND SN74ALS574
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS

* OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS
* ADVANCED OXIDE-ISOLATED, ION-IMPLANTED SCHOTTKY TTL PROCESS
* FUNCTIONALLY EQUIVALENT TO THE 'LS374 AND 'S374
* BUS-STRUCTURED PINOUT
* IMPROVED AC PERFORMANCE OVER 'LS374 AT APPROXIMATELY HALF THE POWER
* 3-STATE BUFFER-TYPE OUTPUTS DRIVE BUS LINES DIRECTLY
* SWITCHING SPECIFICATIONS AT 50 pF

FUNCTION TABLE

OUTPUT CONTROL	CLOCK	D	OUTPUT Q
L	↑	H	H
L	↑	L	L
L	L	X	Q0
H	X	X	Z



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FOR ABSOLUTE MAXIMUM RATINGS, RECOMMENDED OPERATING CONDITIONS, AND DC ELECTRICAL CHARACTERISTICS SEE PAGES 226 AND 227, BUFFER OUTPUT.

TIMING REQUIREMENTS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE

		SN54ALS574			SN74ALS574			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
DATA SETUP TIME, TSU		10			10			NS
DATA HOLD TIME, TH		4			0			NS
WIDTH OF CLOCK PULSE, TW	HIGH	10			10			NS
	LOW	17			15			NS

SETUP AND HOLD TIMES ARE WITH RESPECT TO LOW-TO-HIGH TRANSITION OF CLOCK

SWITCHING CHARACTERISTICS OVER RECOMMENDED T_A RANGE, V_{CC}=4.5 TO 5.5V, R_L=500 OHMS, C_L=50pF (UNLESS OTHERWISE NOTED). REFER TO PAGE 267 FOR LOAD CIRCUITS & WAVEFORMS.

PARAMETER	FROM	SN54ALS/74ALS574*			SN54ALS574			SN74ALS574			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
FMAX		45	50		30			35			MHz
TPLH	CLOCK		7		4		15	4		12	NS
TPHL			7		4		15	4		12	NS
TPZH	OUTPUT CONTROL		8		4		21	5		18	NS
TPZL			8		4		21	5		18	NS
TPHZ	OUTPUT CONTROL		3		2		10	2		8	NS
TPLZ			5		3		15	3		13	NS

* SN54ALS/74ALS574 VALUES ARE AT V_{CC} = 5V, T_A = 25°C, C_L = 15pF, R_L = 500 OHMS

SUPPLY CURRENT OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (SEE NOTE)

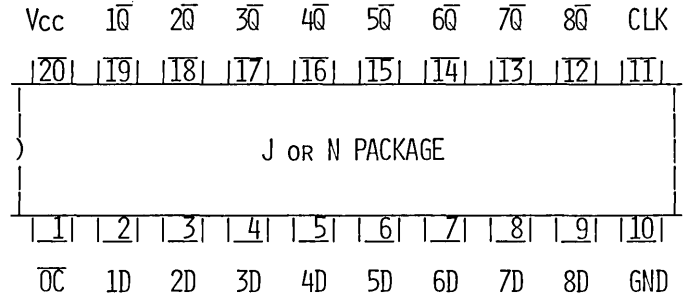
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CCH} SUPPLY CURRENT, OUTPUTS HIGH	V_{CC} = MAX, OUTPUTS OPEN		10.5	15	mA
I_{CCL} SUPPLY CURRENT, OUTPUTS LOW			14.5	21	mA
I_{CCZ} SUPPLY CURRENT, OUTPUTS DISABLED			15.5	27	mA

NOTE: TYPICAL VALUES ARE AT V_{CC} = 5V, T_A = 25°C

* OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH INVERTED OUTPUTS
* ADVANCED OXIDE-ISOLATED, ION IMPLANTED SCHOTTKY TTL PROCESS
* BUS-STRUCTURED PINOUT
* BUFFER-TYPE OUTPUTS DRIVE BUS LINES DIRECTLY
* SWITCHING SPECIFICATIONS AT 50 pF

FUNCTION TABLE

OUTPUT CONTROL	CLOCK	D	OUTPUT $\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z



FOR ABSOLUTE MAXIMUM RATINGS, RECOMMENDED OPERATING CONDITIONS, AND DC ELECTRICAL CHARACTERISTICS SEE PAGES 226 AND 227, BUFFER OUTPUT.

TIMING REQUIREMENTS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE

		SN54ALS576			SN74ALS576			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
DATA SETUP TIME, TSU		10			10			NS
DATA HOLD TIME, TH		4			0			NS
WIDTH OF CLOCK PULSE, TW	HIGH	10			10			NS
	LOW	17			15			NS

SETUP AND HOLD TIMES ARE WITH RESPECT TO LOW-TO-HIGH TRANSITION OF CLOCK

SWITCHING CHARACTERISTICS OVER RECOMMENDED T_A RANGE, V_{CC}=4.5 TO 5.5V, R_L=500 OHMS, C_L=50pF (UNLESS OTHERWISE NOTED). REFER TO PAGE 267 FOR LOAD CIRCUITS & WAVEFORMS.

PARAMETER	FROM	SN54ALS/74ALS576*			SN54ALS576			SN74ALS576			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
FMAX		45	50		30			35			MHz
TPLH	CLOCK		7		4		15	4		12	NS
TPHL	CLOCK		7		4		15	4		12	NS
TPZH	OUTPUT CONTROL		8		4		21	4		18	NS
TPZL	OUTPUT CONTROL		8		4		21	4		18	NS
TPHZ	OUTPUT CONTROL		3		2		10	2		8	NS
TPLZ	OUTPUT CONTROL		5		3		15	3		13	NS

* SN54ALS/74ALS576 VALUES ARE AT V_{CC} = 5V, T_A = 25°C, C_L = 15pF, R_L = 500 OHMS

SUPPLY CURRENT OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (SEE NOTE)

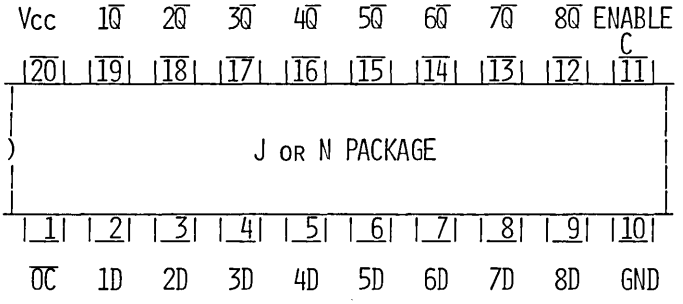
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CCH} SUPPLY CURRENT, OUTPUTS HIGH	V_{CC} = MAX, OUTPUTS OPEN		10.5	15	mA
I_{CCL} SUPPLY CURRENT, OUTPUTS LOW			14.5	21	mA
I_{CCZ} SUPPLY CURRENT, OUTPUTS DISABLED			15.5	27	mA

NOTE: TYPICAL VALUES ARE AT V_{CC} = 5V, T_A = 25°C

* OCTAL D-TYPE TRANSPARENT LATCHES WITH INVERTED OUTPUTS
* ADVANCED OXIDE-ISOLATED, ION-IMPLANTED SCHOTTKY TTL PROCESS
* BUS-STRUCTURED PINOUT
* 3-STATE BUFFER-TYPE OUTPUTS DRIVE BUS LINES DIRECTLY
* SWITCHING SPECIFICATIONS AT 50 pF

FUNCTION TABLE

OUTPUT CONTROL	ENABLE C	D	OUTPUT $\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z



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FOR ABSOLUTE MAXIMUM RATINGS, RECOMMENDED OPERATING CONDITIONS, AND DC ELECTRICAL CHARACTERISTICS SEE PAGES 226 AND 227, BUFFER OUTPUT.

TIMING REQUIREMENTS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE

	MIN	TYP	MAX	UNIT
DATA SETUP TIME, TSU	10			NS
DATA HOLD TIME, TH	0			NS
WIDTH OF ENABLE PULSE, TW	15			NS

SETUP AND HOLD TIMES ARE WITH RESPECT TO HIGH-TO-LOW TRANSITION OF ENABLE

SWITCHING CHARACTERISTICS OVER RECOMMENDED T_A RANGE, V_{CC}=4.5 TO 5.5V, R_L=500 OHMS, C_L=50pF (UNLESS OTHERWISE NOTED). REFER TO PAGE 267 FOR LOAD CIRCIUTS & WAVEFORMS.

		SN54ALS/74ALS580*			SN54ALS580			SN74ALS580			
PARAMETER	FROM	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
TPLH	DATA		9		3		21	3		18	NS
TPHL	DATA		5		3		15	3		12	NS
TPLH	ENABLE		11		8		29	8		22	NS
TPHL	ENABLE		11		8		22	8		21	NS
TPZH	OUTPUT CONTROL		8		4		21	4		18	NS
TPZL	OUTPUT CONTROL		8		4		21	4		18	NS
TPHZ	OUTPUT CONTROL		3		2		10	2		8	NS
TPLZ	OUTPUT CONTROL		5		3		15	3		13	NS

* SN54ALS/74ALS580 VALUES ARE AT V_{CC} = 5V, T_A = 25°C, C_L = 15pF, R_L = 500 OHMS

SUPPLY CURRENT OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (SEE NOTE)

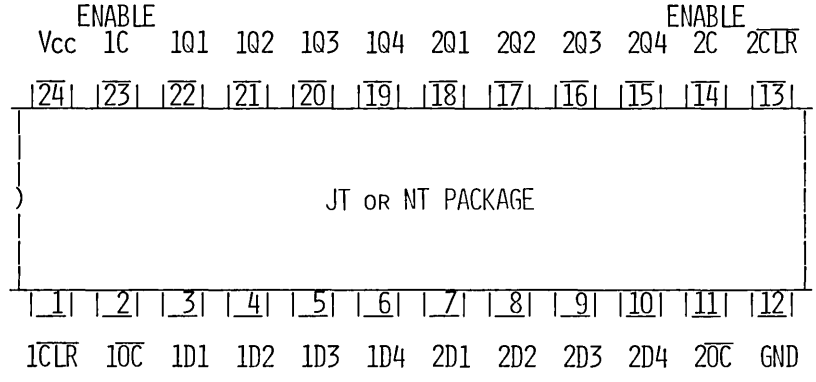
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CCH}	SUPPLY CURRENT, OUTPUTS HIGH	V_{CC} = MAX, OUTPUTS OPEN		10	16	mA
I_{CCL}	SUPPLY CURRENT, OUTPUTS LOW			15	24	mA
I_{CCZ}	SUPPLY CURRENT, OUTPUTS DISABLED			15.5	26	mA

NOTE: TYPICAL VALUES ARE AT V_{CC} = 5V, T_A = 25°C

* DUAL 4-BIT D-TYPE LATCHES
* BUS-STRUCTURED PINOUT
* ADVANCED OXIDE-ISOLATED, ION-IMPLANTED TTL SCHOTTKY PROCESS
* 3-STATE BUFFER-TYPE OUTPUTS DRIVE BUS LINES DIRECTLY
* SWITCHING SPECIFICATIONS AT 50 pF

FUNCTION TABLE

$\overline{CLR}$	D	EN C	$\overline{OC}$	Q
X	X	X	H	Z
L	X	X	L	L
H	H	H	L	H
H	L	H	L	L
H	X	L	L	Q_0



FOR ABSOLUTE MAXIMUM RATINGS, RECOMMENDED OPERATING CONDITIONS, AND DC ELECTRICAL CHARACTERISTICS SEE PAGES 226 AND 227, BUFFER OUTPUT.

TIMING REQUIREMENTS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE

		MIN	TYP	MAX	UNIT
DATA SETUP TIMES, TSU		10			NS
DATA HOLD TIMES, TH		7			NS
PULSE WIDTH, TW	ENABLE HIGH	10			NS
	CLEAR LOW	15			NS

SETUP AND HOLD TIMES ARE WITH RESPECT TO HIGH-TO-LOW TRANSITION OF ENABLE

SWITCHING CHARACTERISTICS OVER RECOMMENDED T_A RANGE, V_{CC}=4.5 TO 5.5V, R_L=500 OHMS, C_L=50pF (UNLESS OTHERWISE NOTED). REFER TO PAGE 267 FOR LOAD CIRCIUTS & WAVEFORMS.

PARAMETER	FROM	SN54ALS/74ALS873* MIN	TYP	MAX	SN54ALS873 MIN	TYP	MAX	SN74ALS873 MIN	TYP	MAX	UNIT
TPLH	DATA		5		2		15	2		12	NS
TPHL			5		2		15	2		12	NS
TPLH	ENABLE		11		8		29	8		22	NS
TPHL			11		8		22	8		21	NS
TPZH	OUTPUT CONTROL		8		4		21	4		18	NS
TPZL			8		4		21	4		18	NS
TPHZ	OUTPUT CONTROL		3		2		10	2		8	NS
TPLZ			5		2		15	2		13	NS
TPHL	CLEAR		11		6		24	6		24	NS

* SN54ALS/74ALS873 VALUES ARE AT V_{CC} = 5V, T_A = 25°C, C_L = 15pF, R_L = 500 OHMS

SUPPLY CURRENT OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (SEE NOTE)

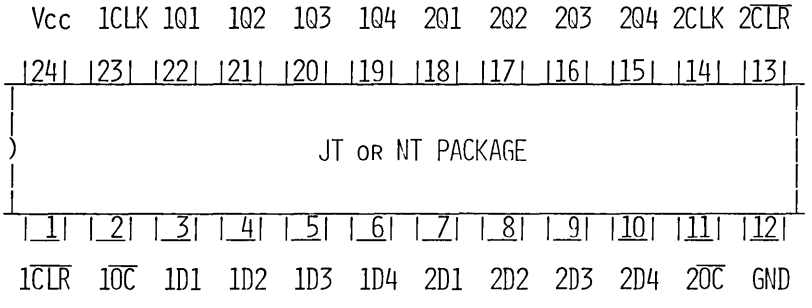
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CCH}	SUPPLY CURRENT, OUTPUTS HIGH	V_{CC} = MAX, OUTPUTS OPEN		10	21	mA
I_{CCL}	SUPPLY CURRENT, OUTPUTS LOW			15	29	mA
I_{CCZ}	SUPPLY CURRENT, OUTPUTS DISABLED			15.5	31	mA

NOTE: TYPICAL VALUES ARE AT V_{CC} = 5V, T_A = 25°C

* DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS
* ADVANCED OXIDE-ISOLATED, ION-IMPLANTED TTL SCHOTTKY PROCESS
* BUS-STRUCTURED PINOUT
* 3-STATE BUFFER-TYPE OUTPUTS DRIVE BUS LINES DIRECTLY
* SWITCHING SPECIFICATIONS AT 50 pF

FUNCTION TABLE

$\overline{CLR}$	D	CLK	$\overline{OC}$	Q
X	X	X	H	Z
L	X	X	L	L
H	H	↑	L	H
H	L	↑	L	L
H	X	L	L	Q_0



FOR ABSOLUTE MAXIMUM RATINGS, RECOMMENDED OPERATING CONDITIONS, AND DC ELECTRICAL CHARACTERISTICS SEE PAGES 226 AND 227, BUFFER OUTPUT.

3

TIMING REQUIREMENTS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE

		SN54ALS874			SN74ALS874			
		MIN	TYP	MAX	MIN	TYP	MAX	UNIT
DATA SETUP TIMES, TSU		10			10			NS
DATA HOLD TIMES, TH		4			0			NS
CLEAR INACTIVE STATE SETUP TIME, TSU		10			10			NS
PULSE WIDTH, TW	CLOCK HIGH	10			10			NS
	CLOCK LOW	17			15			NS
	CLEAR LOW	10			10			NS

SETUP AND HOLD TIMES ARE WITH RESPECT TO LOW-TO-HIGH TRANSITION OF CLOCK

SWITCHING CHARACTERISTICS OVER RECOMMENDED T_A RANGE, V_{CC}=4.5 TO 5.5V, R_L=500 OHMS, C_L=50pF (UNLESS OTHERWISE NOTED). REFER TO PAGE 267 FOR LOAD CIRCIUTS & WAVEFORMS.

PARAMETER	FROM	SN54ALS/74ALS874*			SN54ALS874			SN74ALS874			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
FMAX		45	50		30			35			MHz
TPLH	CLOCK		7		4		15	4		12	NS
TPHL			7		4		15	4		12	NS
TPZH	OUTPUT CONTROL		8		4		21	4		18	NS
TPZL			8		4		21	4		18	NS
TPHZ	OUTPUT CONTROL		3		2		10	2		8	NS
TPLZ			5		3		15	3		13	NS
TPHL	CLEAR		11		6		22	6		19	NS

* SN54ALS/74ALS874 VALUES ARE AT V_{CC} = 5V, T_A = 25°C, C_L = 15pF, R_L = 500 OHMS

SUPPLY CURRENT OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (SEE NOTE)

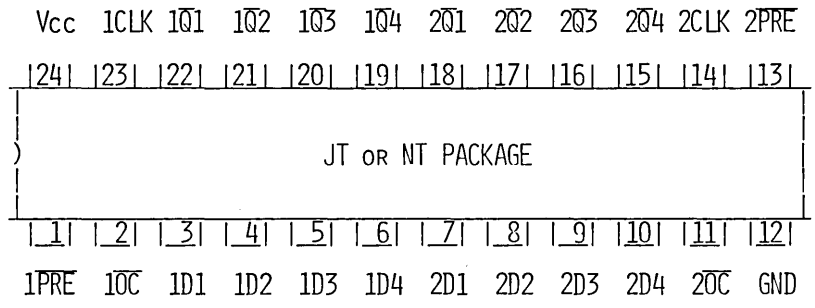
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CCH}	SUPPLY CURRENT, OUTPUTS HIGH	V_{CC}=MAX, OUTPUTS OPEN		14	21	mA
I_{CCL}	SUPPLY CURRENT, OUTPUTS LOW			18	29	mA
I_{CCZ}	SUPPLY CURRENT, OUTPUTS DISABLED			20	31	mA

NOTE: TYPICAL VALUES ARE AT V_{CC} = 5V, T_A = 25°C

* DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH INVERTED OUTPUTS
* ADVANCED OXIDE-ISOLATED, ION-IMPLANTED TTL SCHOTTKY PROCESS
* BUS-STRUCTURED PINOUT
* 3-STATE BUFFER-TYPE OUTPUTS DRIVE BUS LINES DIRECTLY
* SWITCHING SPECIFICATIONS AT 50 pF

FUNCTION TABLE

PRE	D	CLK	$\overline{OC}$	Q
X	X	X	H	Z
L	X	X	L	L
H	H	↑	L	L
H	L	↑	L	H
H	X	L	L	Q_0



FOR ABSOLUTE MAXIMUM RATINGS, RECOMMENDED OPERATING CONDITIONS, AND DC ELECTRICAL CHARACTERISTICS SEE PAGES 226 AND 227, BUFFER OUTPUT.

TIMING REQUIREMENTS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE

		SN54ALS876			SN74ALS876			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
DATA SETUP TIMES, t_{su}		10			10			NS
DATA HOLD TIMES, t_h		4			0			NS
PRESET INACTIVE STATE SETUP TIME, t_{su}		10			10			NS
PULSE WIDTH, t_w	CLOCK HIGH	10			10			NS
	CLOCK LOW	17			15			NS
	PRESET LOW	10			10			NS

SETUP AND HOLD TIMES ARE WITH RESPECT TO LOW-TO-HIGH TRANSITION OF CLOCK

SWITCHING CHARACTERISTICS OVER RECOMMENDED T_A RANGE, V_{CC}=4.5 TO 5.5V, R_L=500 OHMS, C_L=50pF (UNLESS OTHERWISE NOTED). REFER TO PAGE 267 FOR LOAD CIRCIUTS & WAVEFORMS.

PARAMETER	FROM	SN54ALS/74ALS876*			SN54ALS876			SN74ALS876			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}		45	50		30			35			MHz
t_{PLH}	CLOCK		7		4		15	4		12	NS
t_{PHL}			7		4		15	4		12	NS
t_{PZH}	OUTPUT		8		4		21	4		18	NS
t_{PZL}	CONTROL		8		4		21	4		18	NS
t_{PHZ}	OUTPUT		3		2		10	2		8	NS
t_{PLZ}	CONTROL		5		3		15	3		13	NS
t_{PHL}	PRESET		11		6		22	6		19	NS

* SN54ALS/74ALS876 VALUES ARE AT V_{CC} = 5V, T_A = 25°C, C_L = 15pF, R_L = 500 OHMS

SUPPLY CURRENT OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (SEE NOTE)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CCH} SUPPLY CURRENT, OUTPUTS HIGH	V_{CC} = MAX, OUTPUTS OPEN		14	21	mA
I_{CCL} SUPPLY CURRENT, OUTPUTS LOW			18	29	mA
I_{CCZ} SUPPLY CURRENT, OUTPUTS DISABLED			20	31	mA

NOTE: TYPICAL VALUES ARE AT V_{CC} = 5V, T_A = 25°C

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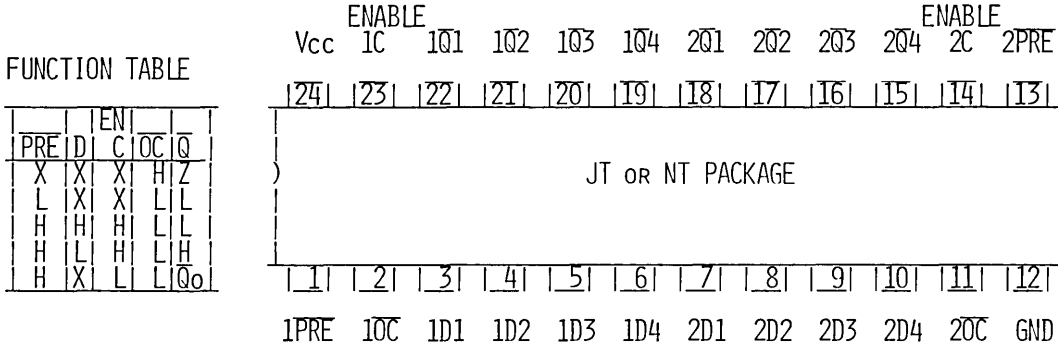
* DUAL 4-BIT D-TYPE LATCHES WITH INVERTED OUTPUTS
* ADVANCED OXIDE-ISOLATED, ION-IMPLANTED TTL SCHOTTKY PROCESS
* BUS-STRUCTURED PINOUT
* 3-STATE BUFFER-TYPE OUTPUTS DRIVE BUS LINES DIRECTLY
* SWITCHING SPECIFICATIONS AT 50 pF

FUNCTION TABLE

		EN		
PRE	D	C	OC	Q
X	X	X	H	Z
L	X	X	L	L
H	H	H	L	L
H	L	H	L	H
H	X	L	L	Q_0



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FOR ABSOLUTE MAXIMUM RATINGS, RECOMMENDED OPERATING CONDITIONS, AND DC ELECTRICAL CHARACTERISTICS SEE PAGES 226 AND 227, BUFFER OUTPUT.

TIMING REQUIREMENTS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE

		MIN	TYP	MAX	UNIT
DATA SETUP TIMES, t_{su}		15			NS
DATA HOLD TIMES, t_h		0			NS
PULSE WIDTH, t_w	ENABLE HIGH	15			NS
	PRESET LOW	15			NS

SETUP AND HOLD TIMES ARE WITH RESPECT TO HIGH-TO-LOW TRANSITION OF ENABLE

SWITCHING CHARACTERISTICS OVER RECOMMENDED T_A RANGE, V_{CC}=4.5 TO 5.5V, R_L=500 OHMS, C_L=50pF (UNLESS OTHERWISE NOTED). REFER TO PAGE 267 FOR LOAD CIRCUITS & WAVEFORMS.

		SN54ALS/74ALS880*			SN54ALS880			SN74ALS880			
PARAMETER	FROM	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
t_{PLH}	DATA		10		3		23	3		20	NS
t_{PHL}			5		3		15	3		12	NS
t_{PLH}	ENABLE		12		8		31	8		24	NS
t_{PHL}			11		8		22	8		21	NS
t_{PZH}	OUTPUT CONTROL		8		4		21	5		18	NS
t_{PZL}			8		4		21	5		18	NS
t_{PHZ}	OUTPUT CONTROL		3		2		10	2		8	NS
t_{PLZ}			5		3		15	3		13	NS
t_{PHL}	PRESET		11		6		24	6		21	NS

* SN54ALS/74ALS873 VALUES ARE AT V_{CC} = 5V, T_A = 25°C, C_L = 15pF, R_L = 500 OHMS

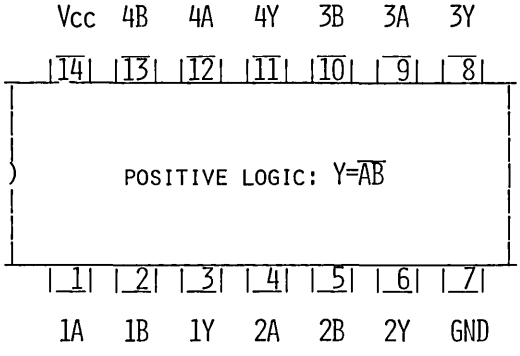
SUPPLY CURRENT OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (SEE NOTE)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CCH}	SUPPLY CURRENT, OUTPUTS HIGH	V_{CC} = MAX, OUTPUTS OPEN		14	21	mA
I_{CCL}	SUPPLY CURRENT, OUTPUTS LOW			19	29	mA
I_{CCZ}	SUPPLY CURRENT, OUTPUTS DISABLED			20	31	mA

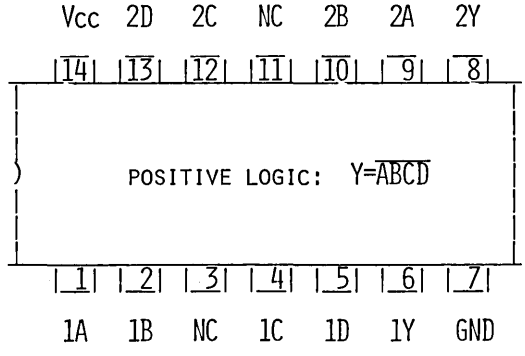
NOTE: TYPICAL VALUES ARE AT V_{CC} = 5V, T_A = 25°C

* 'ALS1000 QUAD 2-INPUT NAND GATES
* ADVANCED OXIDE-ISOLATED, ION-IMPLANTED SCHOTTKY TTL PROCESS
* IMPROVED AC PERFORMANCE AND INCREASED OUTPUT DRIVE CAPABILITY OVER THE 'LS00 AND 'LS20
* 'ALS1020 DUAL 4-INPUT NAND GATES
* FUNCTIONALLY AND PIN-FOR-PIN COMPATIBLE WITH TTL COUNTERPARTS
* IMPROVED INPUT THRESHOLD VOLTAGE AND LINE RECEIVING CHARACTERISTICS
* SWITCHING SPECIFICATIONS AT 50 pF

'ALS1000. . . J OR N PACKAGE



'ALS1020. . . J OR N PACKAGE



FOR ABSOLUTE MAXIMUM RATINGS, RECOMMENDED OPERATING CONDITIONS, AND DC ELECTRICAL CHARACTERISTICS SEE PAGES 226 AND 227, BUFFER OUTPUT.

SWITCHING CHARACTERISTICS OVER RECOMMENDED T_A RANGE, V_{CC}=4.5V TO 5.5V, R_L=500 OHMS, C_L=50pF (UNLESS OTHERWISE NOTED). REFER TO PAGE 267 FOR LOAD CIRCUITS & WAVEFORMS.

PARAMETER	SN54ALS/74ALS1000*			SN54ALS1000			SN74ALS1000			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TPLH		4		2		10	2		8	NS
TPHL		4		3		10	3		8	NS

PARAMETER	SN54ALS/74ALS1020*			SN54ALS1020			SN74ALS1020			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TPLH		4		2		10	2		8	NS
TPHL		4		3		10	3		8	NS

* SN54ALS/74ALS1000 AND SN54ALS/74ALS1020 VALUES ARE AT V_{CC} = 5V, T_A = 25°C, C_L = 15pF, R_L = 500 OHMS

SUPPLY CURRENT OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (SEE NOTE)

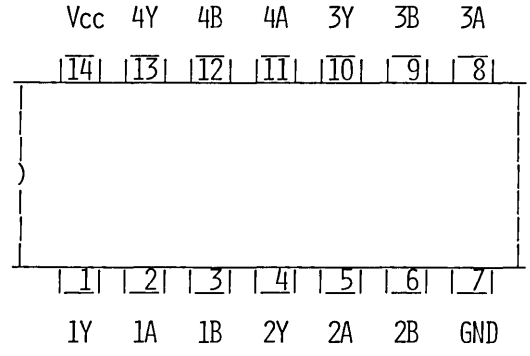
PARAMETER	TEST CONDITIONS	SN54ALS/74ALS1000			SN54ALS/74ALS1020			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
I_{CCH} SUPPLY CURRENT, OUTPUTS HIGH	V_{CC}=MAX, V_I=0V		0.86	1.6		0.43	0.8	mA
I_{CCL} SUPPLY CURRENT, OUTPUTS LOW	V_{CC}=MAX, V_I=4.5V		4	6.4		2	3.2	mA

NOTE: TYPICAL VALUES ARE AT V_{CC} = 5V, T_A = 25°C

* QUAD 2-INPUT NOR GATES
* ADVANCED OXIDE-ISOLATED, ION-IMPLANTED SCHOTTKY TTL PROCESS
* IMPROVED AC PERFORMANCE AND INCREASED OUTPUT DRIVE CAPABILITY OVER THE 'LS02
* FUNCTIONALLY AND PIN-FOR-PIN COMPATIBLE WITH TTL COUNTERPARTS
* IMPROVED INPUT THRESHOLD VOLTAGE
* IMPROVED LINE RECEIVING CHARACTERISTICS
* SWITCHING SPECIFICATIONS AT 50 pF

J OR N PACKAGE

POSITIVE LOGIC: $Y=\overline{A+B}$



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THIS ADVANCED LOW-POWER SCHOTTKY DEVICE HAS BEEN FABRICATED BY AN ADVANCED OXIDE-ISOLATED, ION-IMPLANTED SCHOTTKY TTL PROCESS DEVELOPED BY TI. THE MAJOR BENEFIT OF THIS PROCESS IS THE IMPROVEMENT OF THE SPEED-POWER PRODUCT BY THE REDUCTION OF PARASITIC AND SIDE-WALL CAPACITANCE AND ENHANCED F_T. THE ALS FAMILY FEATURES THE SAME OUTPUT DRIVE CHARACTERISTICS AS THE LS FAMILY.

FOR ABSOLUTE MAXIMUM RATINGS, RECOMMENDED OPERATING CONDITIONS, AND DC ELECTRICAL CHARACTERISTICS SEE PAGES 226 AND 227, BUFFER OUTPUT.

SWITCHING CHARACTERISTICS OVER RECOMMENDED T_A RANGE, V_{CC}=4.5V TO 5.5V, R_L=500 OHMS, C_L=50pF (UNLESS OTHERWISE NOTED). REFER TO PAGE 267 FOR LOAD CIRCUITS & WAVEFORMS.

PARAMETER	SN54ALS/74ALS1002*			SN54ALS1002			SN74ALS1002			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TPLH		4		2		10	2		8	NS
TPHL		4		3		10	3		8	NS

* SN54ALS/74ALS1002 VALUES ARE AT V_{CC} = 5V, T_A = 25°C, C_L = 15pF, R_L = 500 OHMS

SUPPLY CURRENT OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (SEE NOTE)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CCH}	SUPPLY CURRENT, OUTPUTS HIGH	V_{CC}=MAX, V_I=0V		1.7	2.8	mA
I_{CCL}	SUPPLY CURRENT, OUTPUTS LOW	V_{CC}=MAX, V_I=4.5V		4.8	8	mA

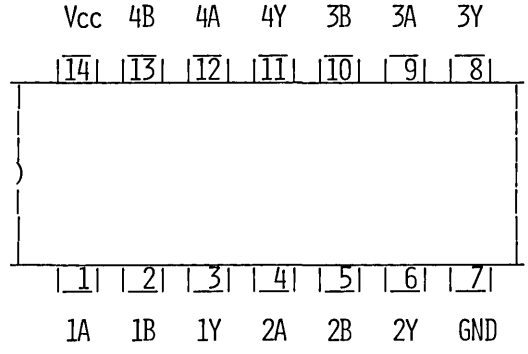
NOTE: TYPICAL VALUES ARE AT V_{CC} = 5V, T_A = 25°C

TYPES SN54ALS1003 AND SN74ALS1003 QUAD 2-INPUT NAND GATES WITH OPEN-COLLECTOR OUTPUTS

* QUAD 2-INPUT NAND GATES WITH OPEN-COLLECTOR OUTPUTS
* ADVANCED OXIDE-ISOLATED, ION-IMPLANTED SCHOTTKY TTL PROCESS
* IMPROVED AC PERFORMANCE AND INCREASED OUTPUT DRIVE CAPABILITY OVER THE 'LS03
* FUNCTIONALLY AND PIN-FOR-PIN COMPATIBLE WITH TTL COUNTERPARTS
* IMPROVED INPUT THRESHOLD VOLTAGE
* IMPROVED LINE RECEIVING CHARACTERISTICS
* SWITCHING SPECIFICATIONS AT 50 pF

J OR N PACKAGE

POSITIVE LOGIC: $Y=\overline{AB}$



THIS ADVANCED LOW-POWER SCHOTTKY DEVICE HAS BEEN FABRICATED BY AN ADVANCED OXIDE-ISOLATED, ION-IMPLANTED SCHOTTKY TTL PROCESS DEVELOPED BY TI. THE MAJOR BENEFIT OF THIS PROCESS IS THE IMPROVEMENT OF THE SPEED-POWER PRODUCT BY THE REDUCTION OF PARASITIC AND SIDE-WALL CAPACITANCE AND ENHANCED F_T. THE ALS FAMILY FEATURES THE SAME OUTPUT DRIVE CHARACTERISTICS AS THE LS FAMILY.

FOR ABSOLUTE MAXIMUM RATINGS, RECOMMENDED OPERATING CONDITIONS, AND DC ELECTRICAL CHARACTERISTICS SEE PAGES 226 AND 227, BUFFER OUTPUT.

SWITCHING CHARACTERISTICS OVER RECOMMENDED T_A RANGE, V_{CC}=4.5V TO 5.5V, R_L=500 OHMS, C_L=50pF (UNLESS OTHERWISE NOTED). REFER TO PAGE 267 FOR LOAD CIRCUITS & WAVEFORMS.

PARAMETER	SN54ALS/74ALS1003* MIN	TYP	MAX	SN54ALS1003 MIN	TYP	MAX	SN74ALS1003 MIN	TYP	MAX	UNIT
TPLH		20		10		40	10		30	NS
TPHL		9		7		18	7		15	NS

* SN54ALS/74ALS1003 VALUES ARE AT V_{CC} = 5V, T_A = 25°C, C_L = 15pF, R_L = 500 OHMS

SUPPLY CURRENT OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (SEE NOTE)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CCH}	SUPPLY CURRENT, OUTPUTS HIGH	V_{CC}=MAX, V_I=0V		0.86	1.6	mA
I_{CCL}	SUPPLY CURRENT, OUTPUTS LOW	V_{CC}=MAX, V_I=4.5V		4	6.4	mA

NOTE: TYPICAL VALUES ARE AT V_{CC} = 5V, T_A = 25°C

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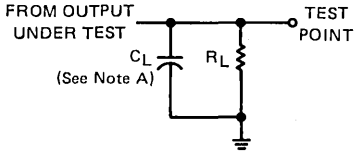
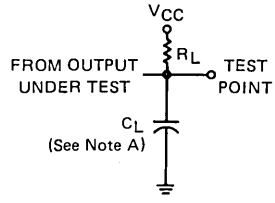
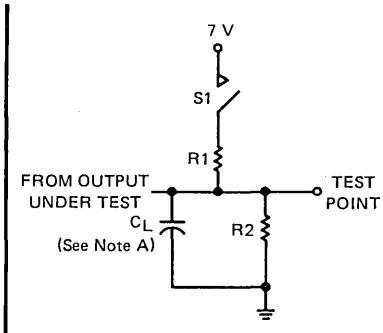
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS

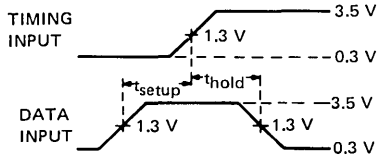


LOAD CIRCUIT FOR OPEN-COLLECTOR OUTPUTS

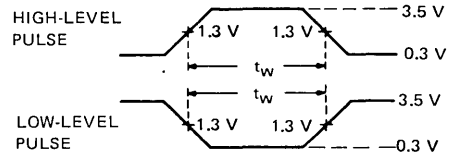


LOAD CIRCUIT FOR THREE-STATE OUTPUTS

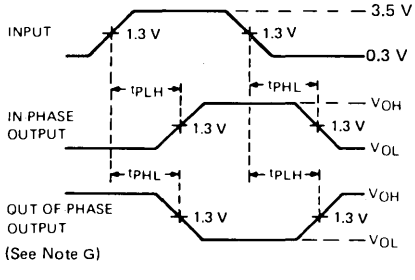
NOTE A. C_L includes probe and jig capacitance.



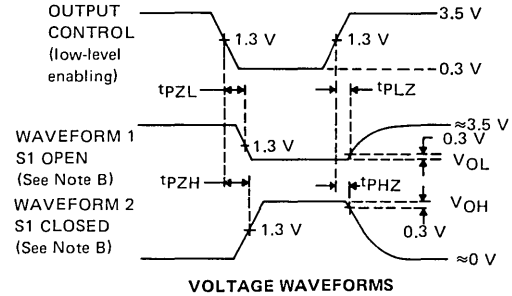
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE WIDTHS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cyle = 50%.

D. When measuring propagation delay times of 3-state outputs, switch S1 is open.

ABSOLUTE MAXIMUM RATINGS OVER FREE-AIR TEMPERATURE RANGE

SUPPLY VOLTAGE, V_{CC} (SEE NOTE 1)		7V
INPUT VOLTAGE, V_I: ALL INPUTS		7V
I/O PORTS		5.5V
OFF STATE (HIGH-LEVEL) VOLTAGE APLLIED TO OPEN-COLLECTOR OUTPUTS		7V
HIGH-LEVEL VOLTAGE APPLIED TO 3-STATE OUTPUTS		5.5V
OPERATING FREE-AIR TEMPERATURE RANGE:	SN54AS	-55°C TO 125°C
	SN74AS	0°C TO 70°C
STORAGE TEMPERATURE RANGE		-65°C TO 150°C

NOTE: 1. VOLTAGE VALUES ARE WITH RESPECT TO NETWORK GROUND TERMINAL.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		STANDARD OUTPUT			BUFFER OUTPUT			BUS DRIVER OUTPUT			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
SUPPLY VOLTAGE	54/74AS	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
HIGH-LEVEL OUTPUT CURRENT, I_{OH} †	54/74AS			-2			-12			-40	mA
	74AS*			-2			-15			-48	mA
HIGH-LEVEL OUTPUT VOLTAGE, V_{OH} ¶	54/74AS			5.5			5.5			5.5	V
LOW-LEVEL OUTPUT CURRENT, I_{OL}	54/74AS			20			32			48	mA
	74AS*			20			48			48	mA
OPERATING FREE-AIR TEMPERATURE, T_A	54AS	-55		125	-55		125	-55		125	°C
	74AS	0		70	0		70	0		70	°C

† DOES NOT APPLY TO OPEN-COLLECTOR OUTPUTS.
¶ APPLIES ONLY TO OPEN-COLLECTOR OUTPUTS.
* THE EXTENDED CONDITIONS APPLY IF V_{CC} IS MAINTAINED BETWEEN 4.75V AND 5.25V.

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ELECTRICAL CHARACTERISTICS OVER RECOMMDENED OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)

PARAMETER		TEST CONDITION		STANDARD OUTPUT MIN	STANDARD OUTPUT TYP†	STANDARD OUTPUT MAX	BUFFER OUTPUT MIN	BUFFER OUTPUT TYP†	BUFFER OUTPUT MAX	BUS DRIVER OUTPUT MIN	BUS DRIVER OUTPUT TYP†	BUS DRIVER OUTPUT MAX	UNIT
V_{IH}	HIGH-LEVEL INPUT VOLTAGE			2			2			2			V
V_{IL}	LOW-LEVEL INPUT VOLTAGE					0.8			0.8			0.8	V
V_{IK}	INPUT CLAMP VOLTAGE	V_{CC}=MIN, I_I=-18mA				-1.2			-1.2			-1.2	V
V_{OH}	HIGH-LEVEL OUTPUT VOLTAGE (SEE NOTE 1)	I_{OH}=-3mA	54/74AS V_{CC}=MIN							2.4	3.2		
		I_{OH}=MAX	54/74AS V_{CC}=MIN	2.5	3.4		2.4	3.2		2.0			V
			74AS V_{CC}=4.75V	2.7	3.4		2.4	3.3		2.0			V
I_{OH}	HIGH-LEVEL OUTPUT CURRENT (SEE NOTE 2)	V_{CC}=MIN, V_{OH}=MAX				0.1			0.1			0.1	mA
V_{OL}	LOW-LEVEL OUTPUT VOLTAGE	V_{CC}=MIN	54/74AS V_{CC}=MIN		.25	0.5		.25	0.5		.25	0.5	V
		I_{OL}=MAX	74AS V_{CC}=4.75V		.35	0.5		.35	0.5		.35	0.5	V
I_I	INPUT CURRENT AT MAXIMUM INPUT VOLTGE	V_{CC}=MAX, V_I=7V	54AS			0.5			0.5			0.5	mA
			74AS			0.3			0.3			0.3	mA
I_{IH}	HIGH-LEVEL INPUT CURRENT	V_{CC}=MAX, V_I=2.7V	54AS			0.4			0.4			0.4	mA
			74AS			0.2			0.2			0.2	mA
I_{IL}	LOW-LEVEL INPUT CURRENT	V_{CC}=MAX, V_{IL}=0.5V				-2			-2			-2.4	mA
I_O	OUTPUT CURRENT ¶	V_{CC}=MAX, V_O=2.25V		-20		-75	-50		-165	-150			mA
I_{OZH}	OFF-STATE OUTPUT CURRENT, HIGH-LEVEL VOLTAGE APPLIED (SEE NOTE 3)	V_{CC}=MAX, V_O=2.7V	I/O PORTS 54AS						.45			.45	mA
			I/O PORTS 74AS						.25			.25	mA
			NON-I/O						50			50	uA
I_{OZL}	OFF STATE OUTPUT CURRENT, LOW-LEVEL VOLTAGE APPLIED (SEE NOTE 3)	V_{CC}=MAX, V_O=0.5V	I/O PORTS						-2			-2.4	mA
			NON-I/O						-50			-50	uA
I_{CC}	SUPPLY CURRENT (SEE NOTE 4)												mA

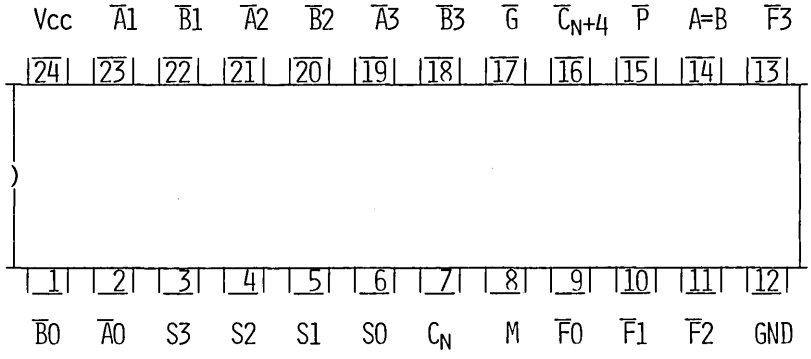
† ALL TYPICAL NUMBERS ARE AT V_{CC}=5V, T_A=25°C.

¶ THE OUTPUT CONDITIONS HAVE BEEN CHOSEN TO PRODUCE A CURRENT THAT CLOSELY APPROXIMATES ONE-HALF THE TRUE SHORT-CIRCUIT CURRENT, I_{OS}.

NOTES 1. DOES NOT APPLY TO OPEN-COLLECTOR OUTPUTS.
2. APPLIES ONLY TO OPEN-COLLECTOR OUTPUTS.
3. APPLIES ONLY TO 3-STATE OUTPUTS.
4. REFER TO INDIVIDUAL DATA SHEETS FOR I_{CC} LIMITS.

* 4-BIT ALU's/FUNCTION GENERATORS IN A 24-PIN, 600-MIL PACKAGE
* FUNCTIONALLY AND PIN-FOR-PIN COMPATIBLE WITH 'S181
* TYPICAL ADD TIMES:
  32-BIT WORDS...18NS
  16-BIT WORDS...15NS
* APPROXIMATELY 40% FASTER THAN SCHOTTKY 'S181 ALU
* ADVANCED OXIDE-ISOLATED, ION-IMPLANTED SCHOTTKY TTL PROCESS
* SWITCHING SPECIFICATIONS AT 50 pF

J OR N PACKAGE



THIS ADVANCED SCHOTTKY DEVICE HAS BEEN FABRICATED BY AN ADVANCED OXIDE-ISOLATED, ION-IMPLANTED TTL PROCESS DEVELOPED BY TI. THE MAJOR BENEFIT OF THIS PROCESS IS THE IMPROVEMENT OF THE SPEED-POWER PRODUCT BY THE REDUCTION OF PARASITIC AND SIDE-WALL CAPACITANCE AND ENHANCED F_T.

THE 'AS181 IS FUNCTIONALLY EQUIVALENT TO AND PIN-FOR-PIN COMPATIBLE WITH THE 'S181.

ALL FUNCTIONS ARE GIVEN BY TABLE 1. TABLE 2 GIVES THE RESULTS IF ACTIVE-HIGH DATA IS USED.

ABSOLUTE MAXIMUM RATINGS ARE SHOWN ON PAGE 268.

TABLE 1

SELECTION				ACTIVE-LOW DATA		
				M = H	M = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC FUNCTIONS	C_n = L (no carry)	C_n = H (with carry)
L	L	L	L	F = $\overline{A}$	F = A MINUS 1	F = A
L	L	L	H	F = $\overline{AB}$	F = AB MINUS 1	F = AB
L	L	H	L	F = $\overline{A}$ + B	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
L	L	H	H	F = 1	F = MINUS 1 (2's COMP)	F = ZERO
L	H	L	L	F = $\overline{A + B}$	F = A PLUS (A + $\overline{B}$)	F = A PLUS (A + $\overline{B}$) PLUS 1
L	H	L	H	F = $\overline{B}$	F = AB PLUS (A + $\overline{B}$)	F = AB PLUS (A + $\overline{B}$) PLUS 1
L	H	H	L	F = A $\oplus$ B	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	F = A + $\overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
H	L	L	L	F = A$\overline{B}$	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1
H	L	L	H	F = A $\oplus$ B	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = A$\overline{B}$ PLUS (A + B)	F = A$\overline{B}$ PLUS (A + B) PLUS 1
H	L	H	H	F = A + B	F = (A + B)	F = (A + B) PLUS 1
H	H	L	L	F = 0	F = A PLUS A*	F = A PLUS A PLUS 1
H	H	L	H	F = A$\overline{B}$	F = AB PLUS A	F = AB PLUS A PLUS 1
H	H	H	L	F = AB	F = A$\overline{B}$ PLUS A	F = A$\overline{B}$ PLUS A PLUS 1
H	H	H	H	F = A	F = A PLUS 1	F = A PLUS 1

TABLE 2

SELECTION				ACTIVE-HIGH DATA		
				M = H	M = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC FUNCTIONS	$\overline{C_n}$ = H (no carry)	$\overline{C_n}$ = L (with carry)
L	L	L	L	F = $\overline{A}$	F = A	F = A PLUS 1
L	L	L	H	F = $\overline{A + B}$	F = A + B	F = (A + B) PLUS 1
L	L	H	L	F = $\overline{A}$B	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
L	L	H	H	F = 0	F = MINUS 1 (2's COMPL)	F = ZERO
L	H	L	L	F = $\overline{AB}$	F = A PLUS A$\overline{B}$	F = A PLUS A$\overline{B}$ PLUS 1
L	H	L	H	F = $\overline{B}$	F = (A + B) PLUS A$\overline{B}$	F = (A + B) PLUS A$\overline{B}$ PLUS 1
L	H	H	L	F = A $\oplus$ B	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	F = A$\overline{B}$	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
H	L	L	L	F = $\overline{A}$ + B	F = A PLUS AB	F = A PLUS AB PLUS 1
H	L	L	H	F = A $\oplus$ B	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = (A + $\overline{B}$) PLUS AB	F = (A + $\overline{B}$) PLUS AB PLUS 1
H	L	H	H	F = AB	F = AB MINUS 1	F = AB
H	H	L	L	F = 1	F = A PLUS A*	F = A PLUS A PLUS 1
H	H	L	H	F = A + $\overline{B}$	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1
H	H	H	L	F = A + B	F = (A + $\overline{B}$) PLUS A	F = (A + $\overline{B}$) PLUS A PLUS 1
H	H	H	H	F = A	F = A MINUS 1	F = A

*Each bit is shifted to the next more significant position.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
SUPPLY VOLTAGE, V_{CC}	54/74AS	4.5	5	5.5	V
HIGH-LEVEL OUTPUT VOLTAGE, V_{OH} A=B OUTPUT ONLY	54/74AS			5.5	V
HIGH-LEVEL OUTPUT CURRENT, I_{OH} FOR ALL OTHER OUTPUTS	54/74AS			-2	mA
LOW-LEVEL OUTPUT CURRENT, I_{OL}	54/74AS			20	mA
OPERATING FREE-AIR TEMPERATURE, T_A	54AS	-55		125	°C
	74AS	0		70	°C

ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)

PARAMETER			TEST CONDITIONS		MIN	TYP*	MAX	UNIT
V_{IH}	HIGH-LEVEL INPUT VOLTAGE				2			V
V_{IL}	LOW-LEVEL INPUT VOLTAGE						0.8	V
V_{IK}	INPUT CLAMP VOLTAGE		V_{CC}=MIN, I_I=-18mA				-1.2	V
I_{IH}	HIGH-LEVEL INPUT CURRENT	M INPUT					20	uA
		ANY A OR B INPUT					60	uA
		ANY S INPUT					80	uA
		CARRY INPUT	V_{CC}=MAX, V_I=2.7V				120	uA
I_{IL}	LOW-LEVEL INPUT CURRENT	M INPUT					-2	mA
		ANY A OR B INPUT					-6	mA
		ANY S INPUT					-8	mA
		CARRY INPUT	V_{CC}=MAX, V_I=0.5V				-12	mA
I_I	INPUT CURRENT AT MAX. INPUT VOLTAGE	M INPUT					0.1	mA
		ANY A OR B INPUT					0.3	mA
		ANY S INPUT					0.4	mA
		CARRY INPUT	V_{CC}=MAX, V_I=7V				0.6	mA
V_{OH}	HIGH-LEVEL OUTPUT VOLTAGE, ANY OUTPUT EXCEPT A=B		V_{IH}=2V, V_{IL}=.8V, I_{OH}=MAX	54/74AS V_{CC}=MIN	2.5	3.2		V
				74AS V_{CC}=4.75V	2.7	3.2		V
V_{OL}	LOW-LEVEL OUTPUT VOLTAGE		V_{IH}=2V, V_{IL}=.8V, I_{OL}=MAX	54/74AS V_{CC}=MIN		0.3	0.5	V
				74AS V_{CC}=4.75V		0.3	0.5	V
I_{OH}	HIGH-LEVEL OUTPUT CURRENT, A=B OUTPUT ONLY		V_{CC}=MIN, V_{IH}=2V, V_{IL}=0.8V, V_{OH}=5.5V				250	uA
I_{CCL}	SUPPLY CURRENT, OUTPUTS LOW		V_{CC}=MAX			100	167	mA
I_{CCH}	SUPPLY CURRENT, OUTPUTS HIGH		V_{CC}=MAX			124	207	mA

* ALL TYPICAL VALUES ARE AT V_{CC} = 5V, T_A =25°C

SWITCHING CHARACTERISTICS OVER RECOMMENDED T_A RANGE, V_{CC} = 4.5 TO 5.5V, C_L= 50pF, R_L=500 OHMS (UNLESS OTHERWISE NOTED). REFER TO PAGE 276 FOR LOAD CIRCUITS AND WAVEFORMS.

PARAMETER	INPUT	OUTPUT	TEST CONDITIONS	SN54/74AS181* MIN	TYP	MAX	SN54AS181 MIN	TYP	MAX	SN74AS181 MIN	TYP	MAX	UNIT
TPLH	C_N	C_{N+4}		7			3		11	3		10	
TPHL				5			2		9	2		7	NS
TPLH	ANY $\overline{A}$ OR $\overline{B}$	C_{N+4}	M=S1=S2=0V S0=S3=4.5V ($\overline{SUM}$ MODE)	8			4		14	4		12	
TPHL				7			2		10	2		8	NS
TPLH	ANY $\overline{A}$ OR $\overline{B}$	C_{N+4}	M=S0=S3=0V S1=S2=4.5V($\overline{DIFF}$ MODE)	9			4		15	4		13	
TPHL				8			2		10	2		9	NS
TPLH	C_N	ANY $\overline{F}$	M=0V($\overline{SUM}$ OR $\overline{DIFF}$ MODE)	6			3		10	3		8	
TPHL				6			3		10	3		8	NS
TPLH	ANY $\overline{A}$ OR $\overline{B}$	$\overline{G}$	M=S1=S2=0V S0=S3=4.5V ($\overline{SUM}$ MODE)	5			2		9	2		7	
TPHL				5			2		9	2		7	NS
TPLH	ANY $\overline{A}$ OR $\overline{B}$	$\overline{G}$	M=S0=S3=0V S1=S2=4.5V($\overline{DIFF}$ MODE)	6			2		10	2		8	
TPHL				6			2		10	2		8	NS
TPLH	ANY $\overline{A}$ OR $\overline{B}$	$\overline{P}$	M=S1=S2=0V S0=S3=4.5V ($\overline{SUM}$ MODE)	6			2		9	2		7	
TPHL				6			2		9	2		7	NS
TPLH	ANY $\overline{A}$ OR $\overline{B}$	$\overline{P}$	M=S0=S3=0V S1=S2=4.5V($\overline{DIFF}$ MODE)	6			2		10	2		8	
TPHL				6			2		10	2		8	NS
TPLH	$\overline{A}_I$ OR $\overline{B}_I$	$\overline{F}_I$	M=S1=S2=0V S0=S3=4.5V ($\overline{SUM}$ MODE)	5			2		9	2		7	
TPHL				5			2		9	2		7	NS
TPLH	$\overline{A}_I$ OR $\overline{B}_I$	$\overline{F}_I$	M=S0=S3=0V S1=S2=4.5V($\overline{DIFF}$ MODE)	6			2		10	2		8	
TPHL				6			2		10	2		8	NS
TPLH	$\overline{A}_I$ OR $\overline{B}_I$	$\overline{F}_I$	M=4.5V(LOGIC MODE)	6			2		10	2		8	
TPHL				6			2		10	2		8	NS
TPHL	ANY $\overline{A}$ OR $\overline{B}$	A=B	C_L=15pF, R_L=280OHMS M=S0=S3=0V, S1=S2=4.5V ($\overline{DIFF}$ MODE)	11			4		16	4		14	
TPHL				9			4		14	4		12	NS

* SN54/74AS181 SPECIFICATIONS VALID ONLY AT 25°C.

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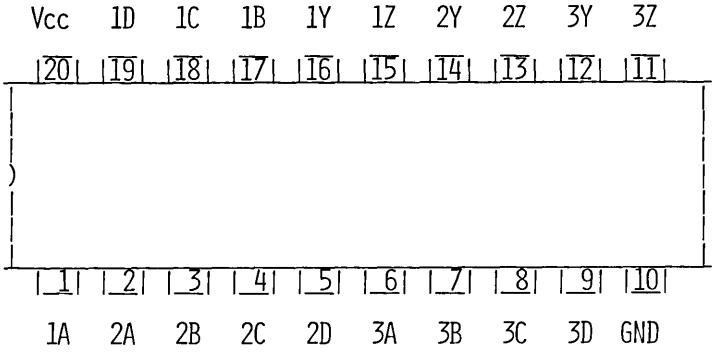
* TRIPLE 4-INPUT AND/NAND DRIVER
* HIGH CAPACITIVE DRIVE CAPABILITY
* ADVANCED OXIDE-ISOLATION, ION-IMPLANTED TTL SCHOTTKY PROCESS
* APPROXIMATELY TWICE THE AC PERFORMANCE OF SCHOTTKY TTL

J OR N PACKAGE

POSITIVE LOGIC: $Y=\overline{ABCD}$
$Z=\overline{ABCD}$



THIS ADVANCED SCHOTTKY DEVICE HAS BEEN FABRICATED BY AN ADVANCED OXIDE-ISOLATED, ION-IMPLANTED TTL PROCESS DEVELOPED BY TI. THE MAJOR BENEFIT OF THIS PROCESS IS THE IMPROVEMENT OF THE SPEED-POWER PRODUCT BY THE REDUCTION OF PARASITIC AND SIDE-WALL CAPACITANCE AND ENHANCED F_T.

FOR ABSOLUTE MAXIMUM RATINGS, RECOMMENDED OPERATING CONDITIONS, AND DC ELECTRICAL CHARACTERISTICS SEE PAGES 268 AND 269, BUS DRIVER OUTPUT.

SUPPLY CURRENT OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (SEE NOTE)

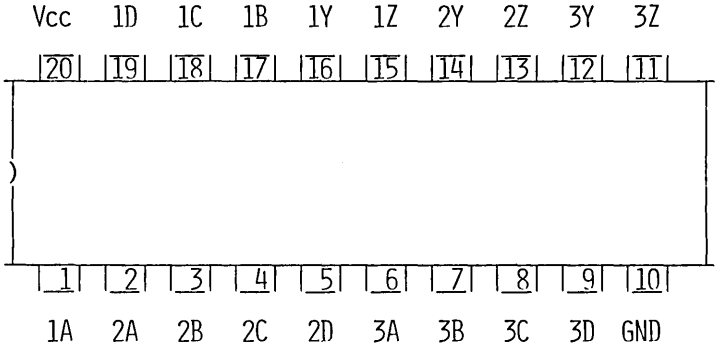
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC} SUPPLY CURRENT, OUTPUTS LOW	V_{CC}=MAX		15		mA

NOTE: TYPICAL VALUES ARE AT V_{CC} = 5V, T_A = 25°C

* TRIPLE 4-INPUT OR/NOR LINE DRIVERS
* ADVANCED OXIDE-ISOLATION, ION-IMPLANTED TTL SCHOTTKY PROCESS
* HIGH CAPACITIVE DRIVE CAPABILITY
* APPROXIMATELY TWICE THE AC PERFORMANCE OF SCHOTTKY TTL

J OR N PACKAGE

POSITIVE LOGIC: $Y=\overline{A+B+C+D}$
$Z=\overline{A+B+C+D}$



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FOR ABSOLUTE MAXIMUM RATINGS, RECOMMENDED OPERATING CONDITIONS, AND DC ELECTRICAL CHARACTERISTICS SEE PAGES 268 AND 269, BUS DRIVER OUTPUT.

SUPPLY CURRENT OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (SEE NOTE)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC} SUPPLY CURRENT, OUTPUTS LOW	V_{CC}=MAX		15		mA

NOTE: TYPICAL VALUES ARE AT V_{CC} = 5V, T_A = 25°C

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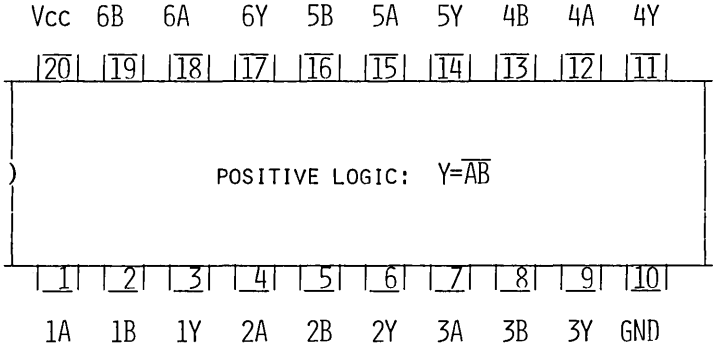
* HEX 2-INPUT NAND DRIVERS
* ADVANCED OXIDE-ISOLATED, ION-IMPLANTED TTL SCHOTTKY PROCESS
* SWITCHING SPECIFICATIONS AT 50 pF
* HIGH CAPACITIVE DRIVE CAPABILITY
* APPROXIMATELY TWICE THE AC PERFORMANCE OF SCHOTTKY TTL

J OR N PACKAGE



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FOR ABSOLUTE MAXIMUM RATINGS, RECOMMENDED OPERATING CONDITIONS, AND DC ELECTRICAL CHARACTERISTICS SEE PAGES 268 AND 269, BUS DRIVER OUTPUT.

SWITCHING CHARACTERISTICS OVER RECOMMENDED T_A RANGE, V_{CC}=4.5 TO 5.5V, R_L=500 OHMS, C_L=50pF (UNLESS OTHERWISE NOTED). REFER TO PAGE 267 FOR LOAD CIRCIUTS & WAVEFORMS.

PARAMETER	54AS/74AS804*			54AS804			74AS804			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TPLH		2		1		4	1		3	NS
TPHL		2		1		4	1		3	NS

* 54AS/74AS804 VALUES ARE AT V_{CC} = 5V, T_A = 25°C, C_L = 50pF, R_L = 500 OHMS

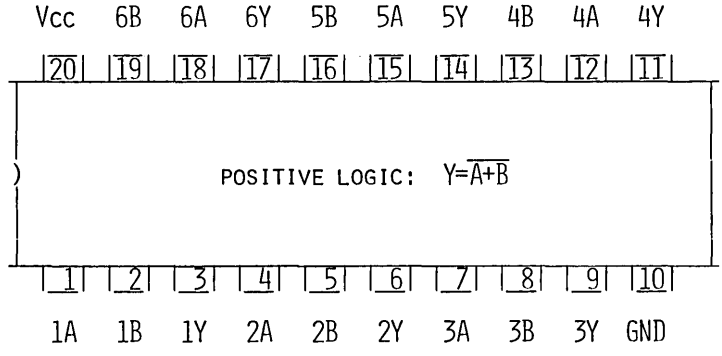
SUPPLY CURRENT OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (SEE NOTE)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CCL} SUPPLY CURRENT, OUTPUTS LOW	V_{CC}=MAX		36	50	mA
I_{CCH} SUPPLY CURRENT, OUTPUTS HIGH	V_{CC}=MAX		17	27	mA

NOTE: TYPICAL VALUES ARE AT V_{CC} = 5V, T_A = 25°C

* HEX 2-INPUT NOR DRIVERS
* ADVANCED OXIDE-ISOLATED, ION-IMPLANTED TTL SCHOTTKY PROCESS
* SWITCHING SPECIFICATIONS AT 50 pF
* HIGH CAPACITIVE DRIVE CAPABILITY
* APPROXIMATELY TWICE THE AC PERFORMANCE OF SCHOTTKY TTL

J OR N PACKAGE



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FOR ABSOLUTE MAXIMUM RATINGS, RECOMMENDED OPERATING CONDITIONS, AND DC ELECTRICAL CHARACTERISTICS SEE PAGES 268 AND 269, BUS DRIVER OUTPUT.

SWITCHING CHARACTERISTICS OVER RECOMMENDED T_A RANGE, V_{CC}=4.5 TO 5.5V, R_L=500 OHMS, C_L=50pF (UNLESS OTHERWISE NOTED). REFER TO PAGE 267 FOR LOAD CIRCIUTS & WAVEFORMS.

PARAMETER	54AS/74AS805*			54AS805			74AS805			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TPLH		2		1		4	1		3	NS
TPHL		2		1		4	1		3	NS

* 54AS/74AS805 VALUES ARE AT V_{CC} = 5V, T_A = 25°C, C_L = 50pF, R_L = 500 OHMS

SUPPLY CURRENT OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (SEE NOTE)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CCL} SUPPLY CURRENT, OUTPUTS LOW	V_{CC}=MAX		42	66	mA
I_{CCH} SUPPLY CURRENT, OUTPUTS HIGH	V_{CC}=MAX		29	45	mA

NOTE: TYPICAL VALUES ARE AT V_{CC} = 5V, T_A = 25°C

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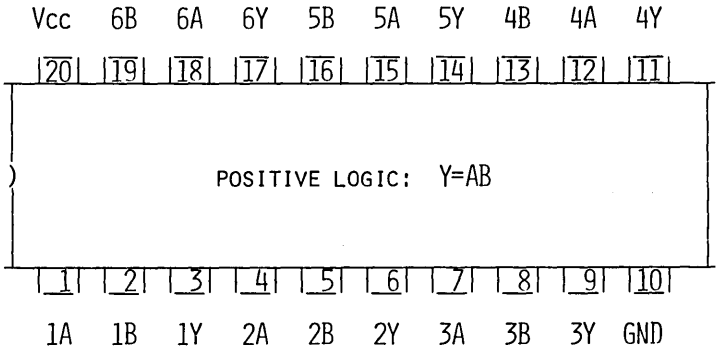
* HEX 2-INPUT AND DRIVERS
* ADVANCED OXIDE-ISOLATED, ION-IMPLANTED TTL SCHOTTKY PROCESS
* SWITCHING SPECIFICATIONS AT **50 pF**
* HIGH CAPACITIVE DRIVE CAPABILITY
* APPROXIMATELY TWICE THE AC PERFORMANCE OF SCHOTTKY TTL

J OR N PACKAGE



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FOR ABSOLUTE MAXIMUM RATINGS, RECOMMENDED OPERATING CONDITIONS, AND DC ELECTRICAL CHARACTERISTICS SEE PAGES 268 AND 269, BUS DRIVER OUTPUT.

SWITCHING CHARACTERISTICS OVER RECOMMENDED T_A RANGE, V_{CC}=4.5 TO 5.5V, R_L=500 OHMS, C_L=50pF (UNLESS OTHERWISE NOTED). REFER TO PAGE 267 FOR LOAD CIRCIUTS & WAVEFORMS.

PARAMETER	54AS/74AS808*			54AS808			74AS808			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TPLH		3		1		6	1		5	NS
TPHL		3		1		5	1		4	NS

* 54AS/74AS808 VALUES ARE AT V_{CC} = 5V, T_A = 25°C, C_L = 50pF, R_L = 500 OHMS

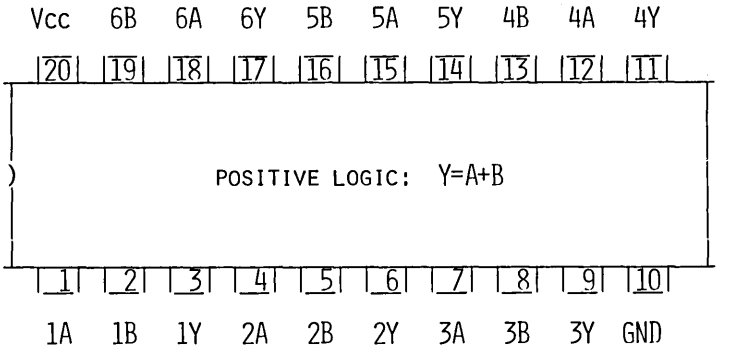
SUPPLY CURRENT OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (SEE NOTE)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CCL} SUPPLY CURRENT, OUTPUTS LOW	V_{CC}=MAX		52	75	mA
I_{CCH} SUPPLY CURRENT, OUTPUTS HIGH	V_{CC}=MAX		30	48	mA

NOTE: TYPICAL VALUES ARE AT V_{CC} = 5V, T_A = 25°C

* HEX 2-INPUT OR DRIVERS
* ADVANCED OXIDE-ISOLATED, ION-IMPLANTED TTL SCHOTTKY PROCESS
* SWITCHING SPECIFICATIONS AT **50 pF**
* HIGH CAPACITIVE DRIVE CAPABILITY
* APPROXIMATELY TWICE THE AC PERFORMANCE OF SCHOTTKY TTL

J OR N PACKAGE



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FOR ABSOLUTE MAXIMUM RATINGS, RECOMMENDED OPERATING CONDITIONS, AND DC ELECTRICAL CHARACTERISTICS SEE PAGES 268 AND 269, BUS DRIVER OUTPUT.

SWITCHING CHARACTERISTICS OVER RECOMMENDED T_A RANGE, V_{CC}=4.5 TO 5.5V, R_L=500 OHMS, C_L=50pF (UNLESS OTHERWISE NOTED). REFER TO PAGE 267 FOR LOAD CIRCIUTS & WAVEFORMS.

PARAMETER	54AS/74AS832*			54AS832			74AS832			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TPLH		3		1		6	1		5	NS
TPHL		3		1		5	1		4	NS

* 54AS/74AS832 VALUES ARE AT V_{CC} = 5V, T_A = 25°C, C_L = 50pF, R_L = 500 OHMS

SUPPLY CURRENT OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (SEE NOTE)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CCL} SUPPLY CURRENT, OUTPUTS LOW	V_{CC}=MAX		64	92	mA
I_{CCH} SUPPLY CURRENT, OUTPUTS HIGH	V_{CC}=MAX		40	65	mA

NOTE: TYPICAL VALUES ARE AT V_{CC} = 5V, T_A = 25°C

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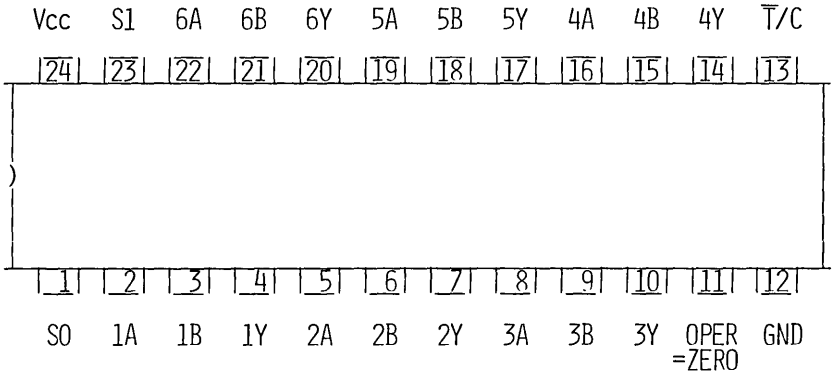
* HEX 2-TO-1 UNIVERSAL MULTIPLEXER IN A 24-PIN, 300-MIL PACKAGE
* ADVANCED OXIDE-ISOLATION, ION-IMPLANTED TTL SCHOTTKY PROCESS
* CHOICE OF TRUE OR COMPLEMENT DATA
* 3-STATE BUFFER TYPE OUTPUTS
* APPROXIMATELY TWICE THE AC PERFORMANCE OF SCHOTTKY TTL

JT OR NT PACKAGE



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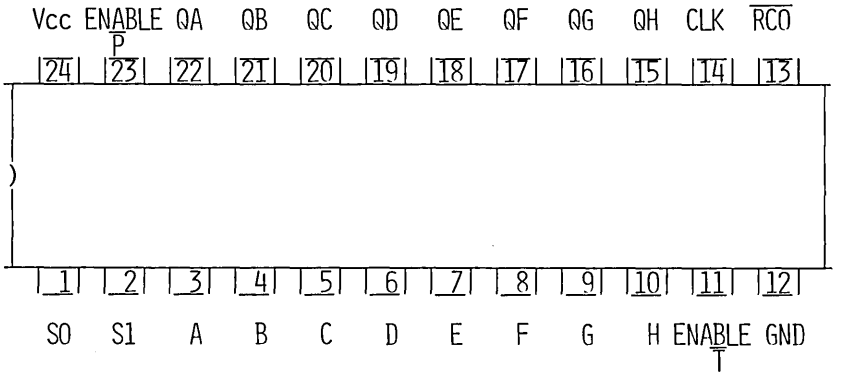
FUNCTION TABLE

$\overline{T}$/C	S1	S0	Y OUTPUTS	OPERAND=ZERO
L	L	L	A	H=ALL A INPUTS LOW
L	L	H	B	H=ALL B INPUTS LOW
L	H	L	AB	HI-Z
L	H	H	L	L
H	L	L	$\overline{A}$	H=ALL A INPUTS LOW
H	L	H	$\overline{B}$	H=ALL B INPUTS LOW
H	H	L	$\overline{AB}$	HI-Z
H	H	H	HI-Z	HI-Z

* 8-BIT SYNCHRONOUS BIDIRECTIONAL COUNTERS IN A 24-PIN, 300-MIL PACKAGE
* FULLY PROGRAMMABLE WITH SYNCHRONOUS COUNTING AND LOADING
* '$AS867$ ASYNCHRONOUS CLEAR
  '$AS869$ SYNCHRONOUS CLEAR
* RIPPLE CARRY OUTPUT FOR N-BIT CASCADING
* ADVANCED OXIDE-ISOLATION, ION-IMPLANTED TTL SCHOTTKY PROCESS
* APPROXIMATELY TWICE THE AC PERFORMANCE OF SCHOTTKY TTL
* BUFFER TYPE OUTPUTS
* 115 MHz TYPICAL CLOCK FREQUENCY

JT OR NT PACKAGE



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THE SYNCHRONOUS OPERATION OF THESE 8-BIT BINARY COUNTERS IS PERFORMED BY SIMULTANEOUSLY CLOCKING ALL FLIP-FLOPS, SO THAT THE OUTPUTS CHANGE COINCIDENT WITH EACH OTHER, THUS ALLEVIATING COUNTING SPIKES ASSOCIATED WITH ASYNCHONOUS COUNTERS. COUNTING AND LOADING OF THESE COUNTERS IS ACCOMPLISHED ON THE POSITIVE TRANSITION OF THE CLOCK. THE '$AS867$ FEATURES AN ASYNCHONOUS CLEAR, WHILE THE '$AS869$ FEATURES A SYNCHONOUS CLEAR. AN INTERNAL LOOK-AHEAD CARRY OUTPUT($\overline{RCO}$) AND TWO ENABLES($\overline{P}$ AND $\overline{T}$) ARE PROVIDED TO PERFORM FAST CASCADABLE COUNTING SCHEMES.

FUNCTION TABLE

S1	S0	FUNCTION
L	L	LOAD
L	H	COUNT UP
H	L	COUNT DOWN
H	H	CLEAR

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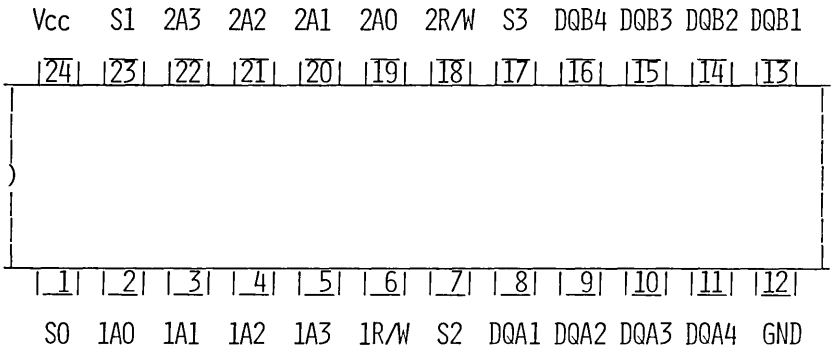
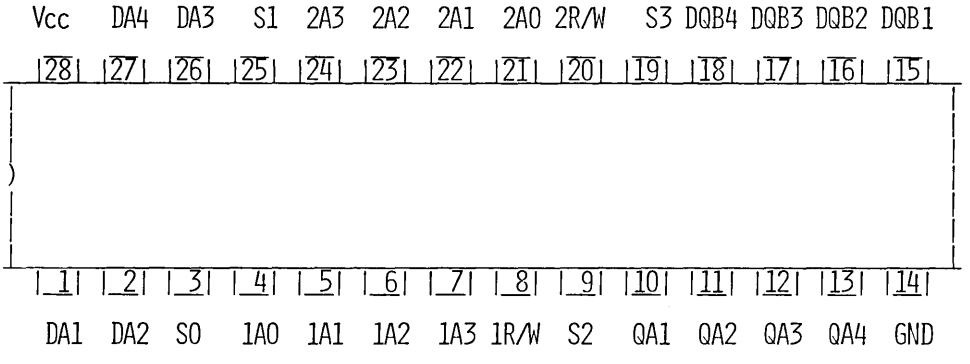
* DUAL 16-BY-4 REGISTER FILE
* ADVANCED OXIDE-ISOLATION, ION-IMPLANTED TTL SCHOTTKY PROCESS
* 3-STATE BUFFER-TYPE OUTPUTS DRIVE BUS LINES DIRECTLY
* 'AS870 24-PIN, 300-MIL PACKAGE
  'AS871 28-PIN, 600-MIL PACKAGE
* APPROXIMATELY TWICE THE AC PERFORMANCE OF SCHOTTKY TTL
* INDIVIDUAL READ/WRITE AND ADDRESS CONTROLS
* DESIGNED SPECIFICALLY FOR MULTIBUS ARCHITECTURE AND OVERLAPPING FILE OPERATIONS

'AS870 . . . JT OR NT PACKAGE



'AS871 . . . J OR N PACKAGE



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THESE DEVICES FEATURE TWO 16-BY-4 REGISTER FILES. EACH REGISTER FILE HAS INDIVIDUAL READ/WRITE CONTROLS AND ADDRESS LINES. THE 'AS870 IS A 24-PIN DEVICE AND HAS TWO 4-BIT DATA I/O PORTS (DQA1- DQA4 AND DQB1 - DQB4). THE 'AS871 ON THE OTHER HAND, IS A 28-PIN DEVICE AND HAS ONLY ONE 4-BIT DATA I/O PORT (DQB1 - DQB4), THE OTHER 4-BIT DATA WORD HAS INDIVIDUAL DATA INPUTS (DA1 - DA4), AND DATA OUTPUTS (QA1 - QA4).

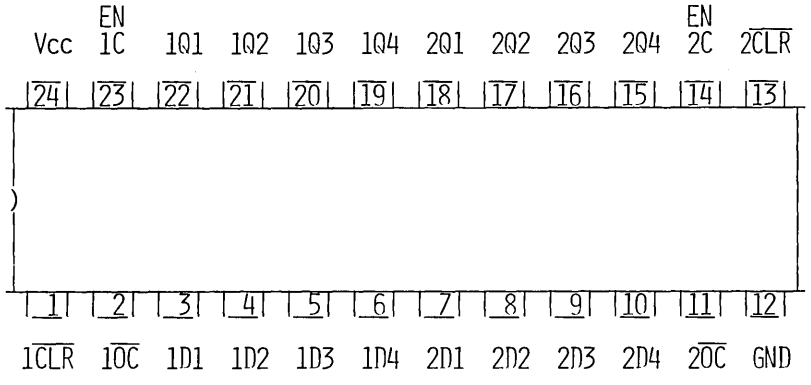
FOR EITHER DEVICE BOTH DATA WORDS (A OR B) HAVE ACCESS TO EITHER REGISTER FILE AND TO PREVENT WRITING CONFLICTS IN THE DUAL-INPUT MODE, THE B INPUT PORT TAKES PRIORITY. THE SELECT LINES S2 AND S3 SELECT THE I/O MODE, MEANING THE MODE OF EACH I/O PORT WHILE THE OTHER TWO SELECT LINES S0 AND S1 CONTROL WHICH PORT HAS ACCESS TO WHICH REGISTER. THE ADDRESS LINES (1A0 - 1A3 OR 2A0 - 2A3) ARE DECODED BY AN INTERNAL 1-OF-16 DECODER TO SELECT WHICH REGISTER IS TO BE ACCESSED. ALL OUTPUTS ARE 3-STATE BUFFER-TYPE OUTPUTS DESIGNED SPECIFICALLY TO DRIVE BUS LINES DIRECTLY.

FUNCTION TABLE

INPUT/OUTPUT			FILE SELECT		
S2	S3	I/O SEL	S0	S1	FILE SEL
L	L	A OUT, B OUT	L	L	1R TO A, 1R TO B
			H	L	2R TO A, 1R TO B
			L	H	1R TO A, 2R TO B
			H	H	2R TO A, 2R TO B
H	L	A IN, B OUT	L	L	A TO 1R, 1R TO B
			H	L	A TO 2R, 1R TO B
			L	H	A TO 1R, 2R TO B
			H	H	A TO 2R, 2R TO B
L	H	A OUT, B IN	L	L	1R TO A, B TO 1R
			H	L	2R TO A, B TO 1R
			L	H	1R TO A, B TO 2R
			H	H	2R TO A, B TO 2R
H	H	A IN, B IN	L	L	B TO 1R
			H	L	A TO 2R, B TO 1R
			L	H	A TO 1R, B TO 2R
			H	H	B TO 2R

* DUAL 4-BIT D-TYPE LATCHES IN A 24-PIN, 300-MIL PACKAGE
* BUS-STRUCTURED PINOUT
* ADVANCED OXIDE-ISOLATED, ION-IMPLANTED TTL SCHOTTKY PROCESS
* 3-STATE BUFFER-TYPE OUTPUTS DRIVE BUS LINES DIRECTLY

JT OR NT PACKAGE



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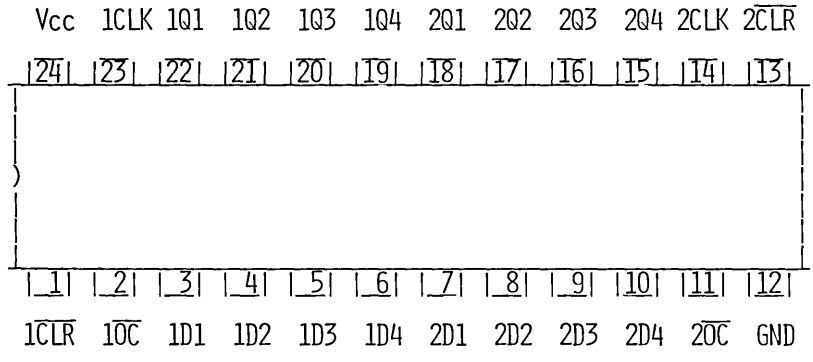
FUNCTION TABLE

$\overline{CLR}$	D	ENABLE C	OUTPUT CONTROL	Q
X	X	X	H	Hi-Z
L	X	X	L	L
H	H	H	L	H
H	L	H	L	L
H	X	L	L	Qo

TYPES SN54AS874 AND SN74AS874
DUAL 4-BIT D-TYPE FLIP-FLOPS

* DUAL 4-BIT D-TYPE FLIP-FLOPS IN A 24-PIN, 300-MIL PACKAGE
* ADVANCED OXIDE-ISOLATED, ION-IMPLANTED TTL SCHOTTKY PROCESS
* BUS-STRUCTURED PINOUT
* 3-STATE BUFFER-TYPE OUTPUTS DRIVE BUS LINES DIRECTLY

JT OR NT PACKAGE



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FUNCTION TABLE

$\overline{CLR}$	D	CLOCK	OUTPUT CONTROL	Q
X	X	X	H	Hi-Z
L	X	X	L	L
H	H	↑	L	H
H	L	↑	L	L
H	X	X	L	Qo

TEXAS INSTRUMENTS
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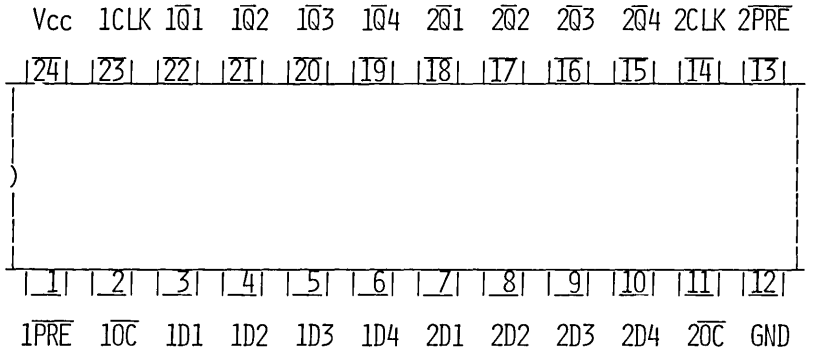
TYPES SN54AS876 AND SN74AS876
DUAL 4-BIT D-TYPE FLIP-FLOPS WITH INVERTED OUTPUTS

* DUAL 4-BIT D-TYPE FLIP-FLOPS WITH INVERTED OUTPUTS
* BUS-STRUCTURED PINOUT
* ADVANCED OXIDE-ISOLATED, ION-IMPLANTED TTL SCHOTTKY PROCESS
* 3-STATE BUFFER-TYPE OUTPUTS DRIVE BUS LINES DIRECTLY

JT OR NT PACKAGE



THIS ADVANCED SCHOTTKY DEVICE HAS BEEN FABRICATED BY AN ADVANCED OXIDE-ISOLATED, ION-IMPLANTED TTL PROCESS DEVELOPED BY TI. THE MAJOR BENEFIT OF THIS PROCESS IS THE IMPROVEMENT OF THE SPEED-POWER PRODUCT BY THE REDUCTION OF PARASITIC AND SIDE-WALL CAPACITANCE AND ENHANCED F_T. THESE 8-BIT REGISTERS ARE DIVIDED INTO TWO 4-BIT WORDS, EACH 4-BIT WORD HAS ITS OWN CLOCK, PRESET, AND OUTPUT CONTROL INPUTS. ON THE POSITIVE TRANSITION OF THE CLOCK, THE Q OUTPUTS WILL BE SET TO THE COMPLEMENT OF THE LOGIC STATES THAT WERE SET UP AT THE D-INPUTS. THESE DEVICES FEATURE 3-STATE BUFFER-TYPE OUTPUTS DESIGNED SPECIFICALLY TO DRIVE BUS LINES DIRECTLY. A HIGH ON THE OUTPUT CONTROL WILL PUT THE OUTPUTS IN THE HIGH-IMPEDANCE STATE. ANOTHER FEATURE OF THESE DEVICES IS THE FLOW-THROUGH ARCHITECTURE; ALL INPUTS ARE ON ONE SIDE OF THE PACKAGE WITH ALL OUTPUTS ON THE OTHER SIDE. THE OUTPUT CONTROL DOES NOT EFFECT THE INTERNAL OPERATION OF THE FLIP-FLOPS.

FUNCTION TABLE

$\overline{PRE}$	D	CLOCK	OUTPUT CONTROL	$\overline{Q}$
X	X	X	H	H_I-Z
L	X	X	L	L
H	H	↑	L	L
H	L	↑	L	H
H	X	X	L	$\overline{Q}_0$

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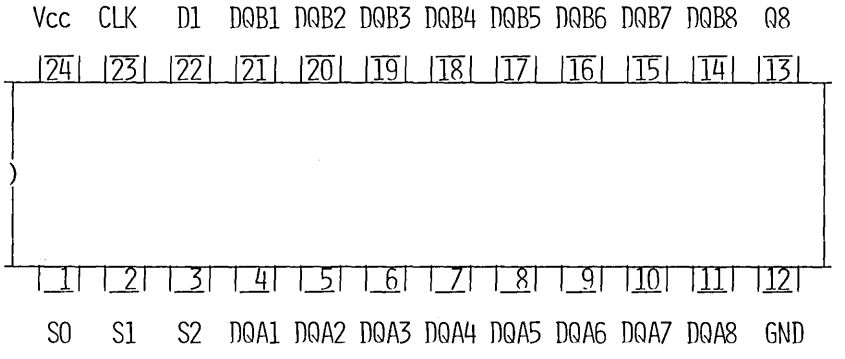
TYPES SN54AS877 AND SN74AS877
8-BIT UNIVERSAL TRANSCIEVER/PORT CONTROLLERS

* 8-BIT UNIVERSAL TRANSCIEVER/PORT CONTROLLERS A 24-PIN, 300-MIL PACKAGE
* EIGHT SELECTABLE TRANSCEIVER/PORT FUNCTIONS
* 3-STATE BUFFER-TYPE OUTPUTS DRIVE BUS LINES DIRECTLY
* ADVANCED OXIDE-ISOLATION, ION-IMPLANTED TTL SCHOTTKY PROCESS
* APPROXIMATELY TWICE THE AC PERFORMANCE OF SCHOTTKY TTL

JT OR NT PACKAGE



THIS ADVANCED SCHOTTKY DEVICE HAS BEEN FABRICATED BY AN ADVANCED OXIDE-ISOLATED, ION-IMPLANTED TTL PROCESS DEVELOPED BY TI. THE MAJOR BENEFIT OF THIS PROCESS IS THE IMPROVEMENT OF THE SPEED-POWER PRODUCT BY THE REDUCTION OF PARASITIC AND SIDE-WALL CAPACITANCE AND ENHANCED F_T.

THE 'AS877 FEATURES TWO 8-BIT I/O PORTS (DQA1 - DQA8 AND DQB1 - DQB8), AN 8-BIT PARALLEL-LOAD, SERIAL-IN, PARALLEL-OUT, AND SERIAL-OUT SHIFT REGISTER AND CONTROL LOGIC. WITH THESE FEATURES, THIS DEVICE IS CAPABLE OF PERFORMING EIGHT SELECTABLE TRANSCEIVER/ PORT FUNCTIONS, DEPENDING ON THE STATE OF THE THREE SELECT LINES S0, S1, AND S2. THESE FUNCTIONS INCLUDE: TRANSFERRING DATA FROM PORT A TO PORT B OR VICE VERSA (I.E., THE TRANSCIEVER FUNCTION), TRANSFERRING DATA FROM THE REGISTER TO EITHER PORT, SERIAL SHIFTING DATA TO EITHER PORT, PERFORMING OFF-LINE SHIFTS (A AND B PORTS IN HIGH-IMPEDANCE STATE), AND CLEARING THE REGISTER. SYNCHRONOUS PARALLEL LOADING OF THE INTERNAL REGISTER CAN BE ACCOMPLISHED BY EITHER PORT ON THE POSITIVE TRANSISTION OF THE CLOCK WHILE SERIALLY SHIFTING DATA IN VIA THE D0 INPUT. ALL SERIAL DATA IS SHIFTED RIGHT, THAT IS, Q1 TO Q2 TO Q3 AND SO FORTH. ALL OUTPUTS ARE BUFFER-TYPE OUTPUTS DESIGNED SPECIFICALLY TO DRIVE BUS LINES DIRECTLY AND ALL ARE 3-STATE EXCEPT FOR Q8.

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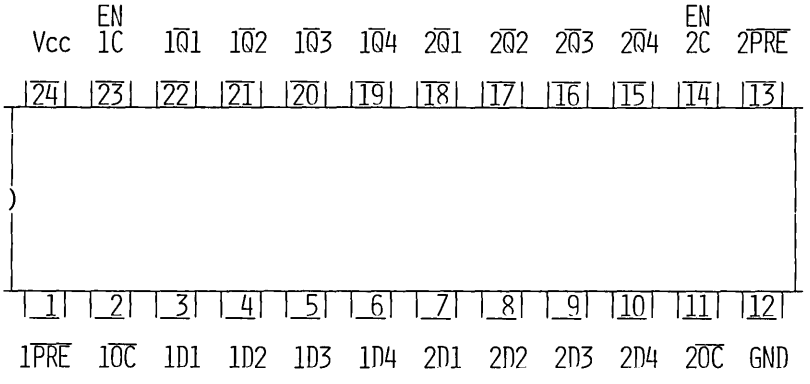
* DUAL 4-BIT D-TYPE LATCHES WITH INVERTED OUTPUTS IN A 24-PIN, 300-MIL PACKAGE
* ADVANCED OXIDE-ISOLATED, ION-IMPLANTED TTL SCHOTTKY PROCESS
* BUS-STRUCTURED PINOUT
* 3-STATE BUFFER-TYPE OUTPUTS DRIVE BUS LINES DIRECTLY

JT OR NT PACKAGE



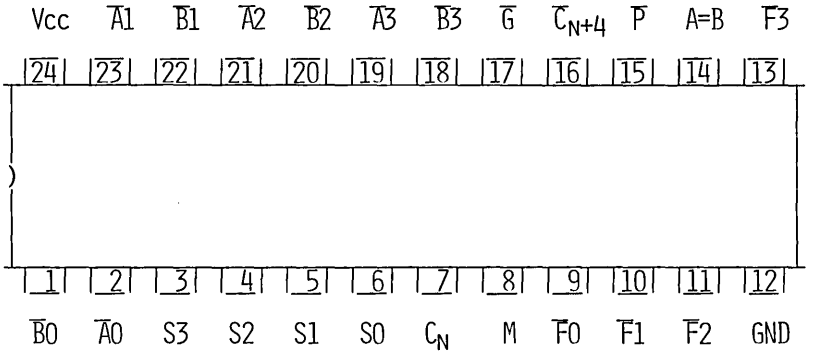
THIS ADVANCED SCHOTTKY DEVICE HAS BEEN FABRICATED BY AN ADVANCED OXIDE-ISOLATED, ION IMPLANTED TTL PROCESS DEVELOPED BY TI. THE MAJOR BENEFIT OF THIS PROCESS IS THE IMPROVEMENT OF THE SPEED-POWER PRODUCT BY THE REDUCTION OF PARASITIC AND SIDE-WALL CAPACITANCE AND ENHANCED F_T. THESE 8-BIT LATCHES ARE DIVIDED INTO TWO 4-BIT WORDS, EACH 4-BIT WORD HAS ITS OWN ENABLE, PRESET, AND OUTPUT CONTROL INPUTS. WITH ENABLE C ACTIVE (HIGH), THE LATCHES ARE TRANSPARENT, THAT IS, $\overline{Q}$ WILL FOLLOW THE COMPLEMENT OF D. THESE DEVICES FEATURE 3-STATE BUFFER-TYPE OUTPUTS DESIGNED SPECIFICALLY TO DRIVE BUS LINES DIRECTLY. A HIGH ON THE OUTPUT CONTROL WILL PUT THE OUTPUTS IN THE HIGH-IMPEDANCE STATE. ANOTHER FEATURE OF THESE DEVICES IS THE FLOW-THROUGH ARCHITECTURE; ALL INPUTS ARE ON ONE SIDE OF THE PACKAGE WITH ALL OUTPUTS ON THE OTHER SIDE. THE OUTPUT CONTROL DOES NOT EFFECT THE INTERNAL OPERATION OF THE LATCHES.

FUNCTION TABLE

$\overline{PRE}$	D	ENABLE C	OUTPUT CONTROL	$\overline{Q}$
X	X	X	H	HI-Z
L	X	X	L	L
H	H	H	L	L
H	L	H	L	$\overline{H}$
H	X	L	L	$\overline{Q_0}$

* 4-BIT ALU's/FUNCTION GENERATORS IN A 24-PIN, 300-MIL PACKAGE
* 'AS881 HAS SAME OPERATING MODES AS BOTH THE 'S181 AND 'AS181 EXPANDED TO INCLUDE STATUS RESIGTER CHECKS
* SWITCHING SPECIFICATIONS AT 50 pF
* APPROXIMATELY 40% FASTER THAN SCHOTTKY 'S181 ALU
* ADVANCED OXIDE-ISOLATED, ION-IMPLANTED SCHOTTKY TTL PROCESS
* TYPICAL ADD TIMES:
  32-BIT WORDS...18NS
  16-BIT WORDS...15NS

JT OR NT PACKAGE



THIS ADVANCED SCHOTTKY DEVICE HAS BEEN FABRICATED BY AN ADVANCED OXIDE-ISOLATED, ION-IMPLANTED TTL PROCESS DEVELOPED BY TI. THE MAJOR BENEFIT OF THIS PROCESS IS THE IMPROVEMENT OF THE SPEED-POWER PRODUCT BY THE REDUCTION OF PARASITIC AND SIDE-WALL CAPACITANCE AND ENHANCED F_T.

THE 'AS881 HAS THE SAME PINOUT AND SAME FUNCTIONALITY AS BOTH THE 'S181 AND THE 'AS181 EXCEPT FOR THE $\overline{P}$, $\overline{G}$, AND C_{N+4} OUTPUTS WHEN THE DEVICE IS IN THE LOGIC MODE (M=H).

IN THE LOGIC MODE THE $\overline{P}$, $\overline{G}$, AND C_{N+4} OUTPUTS OF THE 'AS181 HAVE THE FOLLOWING FUNCTIONS: $\overline{P} = \overline{F}0\overline{F}1\overline{F}2\overline{F}3$, $\overline{G}$ = H, AND $C_{N+4} = \overline{P}\ C_N$. A STATUS CHECK FOR ALL PAIRS BEING EQUAL ($A_I = B_I$), IS PERFORMED WHEN THE SELECT INPUTS (S3, S2, S1, S0) EQUAL HLLH. IN THIS CASE $\overline{P} = \overline{A}0+\overline{B}0+\overline{A}1+\overline{B}1+\overline{A}2+\overline{B}2+\overline{A}3+\overline{B}3$, $\overline{G}$ = H, AND $C_{N+4} = \overline{P}\ C_N$. TO PERFORM A STATUS CHECK FOR ANY PAIR BEING LOW, THE SELECT INPUTS ARE SET TO LHLL THEN $\overline{P} = \overline{A}0\overline{B}0+\overline{A}1\overline{B}1+\overline{A}2\overline{B}2+\overline{A}3\overline{B}3$, $\overline{G}$ = H, AND $C_{N+4} = \overline{P}\ C_N$.

ALL OTHER FUNCTIONS ARE GIVEN BY TABLE 1. TABLE 2 GIVES THE RESULTS IF ACTIVE-HIGH DATA IS USED.

ABSOLUTE MAXIMUM RATINGS ARE SHOWN ON PAGE 268.

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TABLE 1

SELECTION				ACTIVE-LOW DATA		
				M = H	M = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC FUNCTIONS	C_n = L (no carry)	C_n = H (with carry)
L	L	L	L	F = $\overline{A}$	F = A MINUS 1	F = A
L	L	L	H	F = $\overline{AB}$	F = AB MINUS 1	F = AB
L	L	H	L	F = $\overline{A}$ + B	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
L	L	H	H	F = 1	F = MINUS 1 (2's COMP)	F = ZERO
L	H	L	L	F = $\overline{A + B}$	F = A PLUS (A + $\overline{B}$)	F = A PLUS (A + $\overline{B}$) PLUS 1
L	H	L	H	F = $\overline{B}$	F = AB PLUS (A + $\overline{B}$)	F = AB PLUS (A + $\overline{B}$) PLUS 1
L	H	H	L	F = $\overline{A \oplus B}$	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	F = A + $\overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
H	L	L	L	F = $\overline{A}$B	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1
H	L	L	H	F = A $\oplus$ B	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = A$\overline{B}$ PLUS (A + B)	F = A$\overline{B}$ PLUS (A + B) PLUS 1
H	L	H	H	F = A + B	F = (A + B) PLUS 1	F = (A + B) PLUS 1
H	H	L	L	F = 0	F = A PLUS A*	F = A PLUS A PLUS 1
H	H	L	H	F = A$\overline{B}$	F = AB PLUS A	F = AB PLUS A PLUS 1
H	H	H	L	F = AB	F = A$\overline{B}$ PLUS A	F = A$\overline{B}$ PLUS A PLUS 1
H	H	H	H	F = A	F = A	F = A PLUS 1

TABLE 2

SELECTION				ACTIVE-HIGH DATA		
				M = H	M = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC FUNCTIONS	$\overline{C}_n$ = H (no carry)	$\overline{C}_n$ = L (with carry)
L	L	L	L	F = $\overline{A}$	F = A	F = A PLUS 1
L	L	L	H	F = $\overline{A + B}$	F = A + B	F = (A + B) PLUS 1
L	L	H	L	F = $\overline{A}$B	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
L	L	H	H	F = 0	F = MINUS 1 (2's COMPL)	F = ZERO
L	H	L	L	F = $\overline{AB}$	F = A PLUS A$\overline{B}$	F = A PLUS A$\overline{B}$ PLUS 1
L	H	L	H	F = $\overline{B}$	F = (A + B) PLUS A$\overline{B}$	F = (A + B) PLUS A$\overline{B}$ PLUS 1
L	H	H	L	F = A $\oplus$ B	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	F = A$\overline{B}$	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
H	L	L	L	F = $\overline{A}$ + B	F = A PLUS AB	F = A PLUS AB PLUS 1
H	L	L	H	F = $\overline{A \oplus B}$	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = (A + $\overline{B}$) PLUS AB	F = (A + $\overline{B}$) PLUS AB PLUS 1
H	L	H	H	F = AB	F = AB MINUS 1	F = AB
H	H	L	L	F = 1	F = A PLUS A*	F = A PLUS A PLUS 1
H	H	L	H	F = A + $\overline{B}$	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1
H	H	H	L	F = A + B	F = (A + $\overline{B}$) PLUS A	F = (A + $\overline{B}$) PLUS A PLUS 1
H	H	H	H	F = A	F = A MINUS 1	F = A

*Each bit is shifted to the next more significant position.

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE, V_{CC}	54/74AS	4.5	5	5.5	V
HIGH-LEVEL OUTPUT VOLTAGE, V_{OH} FOR A=B OUTPUT ONLY	54/74AS			5.5	V
HIGH-LEVEL OUTPUT CURRENT, I_{OH} FOR ALL OTHER OUTPUTS	54/74AS			-2	mA
LOW-LEVEL OUTPUT CURRENT, I_{OL}	54/74AS			20	mA
	54AS	-55		125	°C
OPERATING FREE-AIR TEMPERATURE, T_A	74AS	0		70	°C

† THE EXTENDED CONDITIONS APPLY IF V_{CC} IS MAINTAINED BETWEEN 4.75V AND 5.25V

ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)

PARAMETER			TEST CONDITIONS		MIN	TYP*	MAX	UNIT
V_{IH}	HIGH-LEVEL INPUT VOLTAGE				2			V
V_{IL}	LOW-LEVEL INPUT VOLTAGE						0.8	V
V_{IK}	INPUT CLAMP VOLTAGE		V_{CC}=MIN, I_I=-18mA				-1.2	V
I_{IH}	HIGH-LEVEL INPUT CURRENT	M INPUT					20	uA
		ANY A OR B INPUT					60	uA
		ANY S INPUT					80	uA
		CARRY INPUT	V_{CC}=MAX, V_I=2.7V				120	uA
I_{IL}	LOW-LEVEL INPUT CURRENT	M INPUT					-2	mA
		ANY A OR B INPUT					-6	mA
		ANY S INPUT					-8	mA
		CARRY INPUT	V_{CC}=MAX, V_I=0.5V				-12	mA
I_I	INPUT CURRENT AT MAX. INPUT VOLTAGE	M INPUT					0.1	mA
		ANY A OR B INPUT					0.3	mA
		ANY S INPUT					0.4	mA
		CARRY INPUT	V_{CC}=MAX, V_I=7V				0.6	mA
V_{OH}	HIGH-LEVEL OUTPUT VOLTAGE, ANY OUTPUT EXCEPT A=B		V_{IH}=2V, V_{IL}=.8V, I_{OH}=MAX	54/74AS V_{CC}=MIN	2.5	3.2		V
				74AS V_{CC}=4.75V	2.7	3.2		V
V_{OL}	LOW-LEVEL OUTPUT VOLTAGE		V_{IH}=2V, V_{IL}=.8V, I_{OL}=MAX	54/74AS V_{CC}=MIN		0.3	0.5	V
				74AS V_{CC}=4.75V		0.3	0.5	V
I_{OH}	HIGH-LEVEL OUTPUT CURRENT, A=B OUTPUT ONLY		V_{CC}=MIN, V_{IH}=2V, V_{IL}=0.8V, V_{OH}=5.5V				250	uA
I_{CCL}	SUPPLY CURRENT, OUTPUTS LOW		V_{CC}=MAX			100	167	mA
I_{CCH}	SUPPLY CURRENT, OUTPUTS HIGH		V_{CC}=MAX			124	207	mA

* ALL TYPICAL VALUES ARE AT V_{CC} = 5V, T_A =25°C

SWITCHING CHARACTERISTICS OVER RECOMMENDED T_A RANGE, V_{CC} = 4.5 TO 5.5V, C_L = 50pF, R_L=500 OHMS (UNLESS OTHERWISE NOTED). REFER TO PAGE 276 FOR LOAD CIRCIUTS AND WAVEFORMS.

PARAMETER	INPUT	OUTPUT	TEST CONDITIONS	SN54/74AS881* MIN	SN54/74AS881* TYP	SN54/74AS881* MAX	SN54AS881 MIN	SN54AS881 TYP	SN54AS881 MAX	SN74AS881 MIN	SN74AS881 TYP	SN74AS881 MAX	UNIT
TPLH					7		3		11	3		10	
TPHL	C_N	C_{N+4}			5		2		9	2		7	NS
TPLH			M=S1=S2=0V		8		4		14	4		12	
TPHL	ANY $\overline{A}$ OR $\overline{B}$	C_{N+4}	S0=S3=4.5V ($\overline{SUM}$ MODE)		7		2		10	2		8	NS
TPLH			M=S0=S3=0V		9		4		15	4		13	
TPHL	ANY $\overline{A}$ OR $\overline{B}$	C_{N+4}	S1=S2=4.5V($\overline{DIFF}$ MODE)		8		2		10	2		9	NS
TPLH					6		3		10	3		8	
TPHL	C_N	ANY $\overline{F}$	M=0V($\overline{SUM}$ OR $\overline{DIFF}$ MODE)		6		3		10	3		8	NS
TPLH			M=S1=S2=0V		5		2		9	2		7	
TPHL	ANY $\overline{A}$ OR $\overline{B}$	$\overline{G}$	S0=S3=4.5V ($\overline{SUM}$ MODE)		5		2		9	2		7	NS
TPLH			M=S0=S3=0V		6		2		10	2		8	
TPHL	ANY $\overline{A}$ OR $\overline{B}$	$\overline{G}$	S1=S2=4.5V($\overline{DIFF}$ MODE)		6		2		10	2		8	NS
TPLH			M=S1=S2=0V		6		2		9	2		7	
TPHL	ANY $\overline{A}$ OR $\overline{B}$	$\overline{P}$	S0=S3=4.5V ($\overline{SUM}$ MODE)		6		2		9	2		7	NS
TPLH			M=S0=S3=0V		6		2		10	2		8	
TPHL	ANY $\overline{A}$ OR $\overline{B}$	$\overline{P}$	S1=S2=4.5V($\overline{DIFF}$ MODE)		6		2		10	2		8	NS
TPLH			M=S1=S2=0V		5		2		9	2		7	
TPHL	$\overline{A}_I$ OR $\overline{B}_I$	$\overline{F}_I$	S0=S3=4.5V ($\overline{SUM}$ MODE)		5		2		9	2		7	NS
TPLH			M=S0=S3=0V		6		2		10	2		8	
TPHL	$\overline{A}_I$ OR $\overline{B}_I$	$\overline{F}_I$	S1=S2=4.5V($\overline{DIFF}$ MODE)		6		2		10	2		8	NS
TPLH					6		2		10	2		8	
TPHL	$\overline{A}_I$ OR $\overline{B}_I$	$\overline{F}_I$	M=4.5V(LOGIC MODE)		6		2		10	2		8	NS
			C_L=15pF, R_L=280OHMS										
TPHL			M=S0=S3=0V, S1=S2=4.5V		11		4		16	4		14	
TPHL	ANY $\overline{A}$ OR $\overline{B}$	A=B	($\overline{DIFF}$ MODE)		9		4		14	4		12	NS

* SN54/74AS881 SPECIFICATIONS VALID ONLY AT 25°C.

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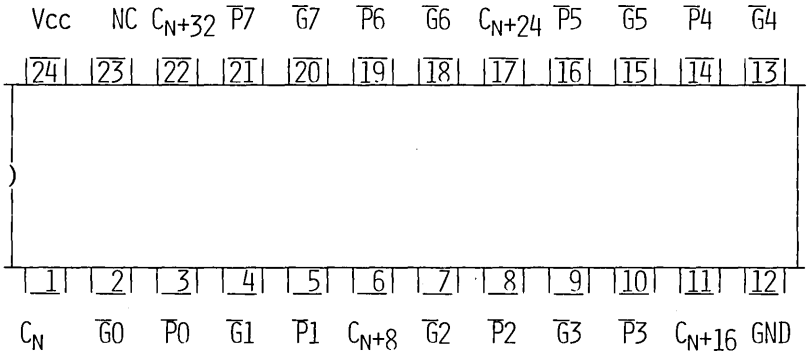
* LOOK-AHEAD CARRY GENERATORS IN A 300-MIL WIDE 24-PIN PACKAGE
* DIRECTLY COMPATIBLE WITH THE NEW 'AS181 & 'AS881 ALU'S AND ALSO THE POPULAR 'S181
* ADVANCED OXIDE-ISOLATED, ION-IMPLANTED TTL SCHOTTKY PROCESS
* SWITCHING SPECIFICATIONS AT 50 pF

JT OR NT PACKAGE



THIS ADVANCED SCHOTTKY DEVICE HAS BEEN FABRICATED BY AN ADVANCED OXIDE-ISOLATED, IONIMPLANTED TTL PROCESS DEVELOPED BY TI. THE MAJOR BENEFIT OF THIS PROCESS IS THE IMPROVEMENT OF THE SPEED-POWER PRODUCT BY THE REDUCTION OF PARASITIC AND SIDE-WALL CAPACITANCE AND ENHANCED F_T.

THE SN54/74AS882 ARE HIGH-SPEED LOOK-AHEAD CARRY GENERATORS CAPABLE OF ANTICIPATING THE CARRY ACROSS A GROUP OF EIGHT 4-BIT BINARY ADDERS. THEY ARE CASCADABLE TO PERFORM LOOK-AHEAD ACROSS N-BIT ADDERS.

'AS882 LOGIC EQUATIONS

$$C_{N+8} = G1+P1G0+P1P0C_N$$

$$C_{N+16} = G3+P3G2+P3P2G1+P3P2P1G0+P3P2P1P0C_N$$

$$C_{N+24} = G5+P5G4+P5P4G3+P5P4P2G2+P5P4P3P2G1+P5P4P3P2P1G0+P5P4P3P2P1P0C_N$$

$$C_{N+32} = G7+P7G6+P7P6G5+P7P6P5G4+P7P6P5P4G3+P7P6P5P4P3G2+P7P6P5P4P3P2G1+ P7P6P5P4P3P2P1G0+P7P6P5P4P3P2P1P0C_N$$

ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING T_A RANGE (UNLESS OTHERWISE NOTED)

PARAMETER			TEST CONDITIONS	MIN	TYP*	MAX	UNIT
V_{IH}	HIGH-LEVEL INPUT VOLTAGE			2			V
V_{IL}	LOW-LEVEL INPUT VOLTAGE					0.8	V
V_{IK}	INPUT CLAMP VOLTAGE		V_{CC}=MIN, I_I=-18mA			-1.2	V
I_I	INPUT CURRENT AT MAXIMUM INPUT VOLTAGE	P0,P1 INPUTS ONLY	V_{CC}=MAX, V_I=7V			2.0	mA
		P2,P3 INPUTS ONLY				1.5	mA
		P4,P5 INPUTS ONLY				1.0	mA
		P6,P7,C_N INPUTS ONLY				0.5	mA
		G0,G6 INPUTS ONLY				4.0	mA
		G1,G2,G4 INPUTS ONLY				6.0	mA
		G3 INPUT ONLY				7.5	mA
		G5 INPUT ONLY				7.0	mA
		G7 INPUT ONLY				4.5	mA
I_{IH}	HIGH-LEVEL INPUT CURRENT	P0,P1 INPUTS ONLY	V_{CC}=MAX, V_I=2.7V			0.8	mA
		P2,P3 INPUTS ONLY				0.6	mA
		P4,P5 INPUTS ONLY				0.4	mA
		P6,P7,C_N INPUTS ONLY				0.2	mA
		G0,G6 INPUTS ONLY				1.6	mA
		G1,G2,G4 INPUTS ONLY				2.4	mA
		G3 INPUT ONLY				3.0	mA
		G5 INPUT ONLY				2.8	mA
		G7 INPUT ONLY				1.8	mA
I_{IL}	LOW-LEVEL INPUT CURRENT	P0 INPUT ONLY	V_{CC}=MAX, V_I=0.5V			13	mA
		P1 INPUT ONLY				11	mA
		P2 INPUT ONLY				8	mA
		P3 INPUT ONLY				7	mA
		P4 INPUT ONLY				5	mA
		C_N,P5 INPUTS ONLY				4	mA
		P6,P7 INPUTS ONLY				2	mA
		G0 INPUT ONLY				25	mA
		G1 INPUT ONLY				36	mA
		G2 INPUT ONLY				39	mA
		G3 INPUT ONLY				46	mA
		G4 INPUT ONLY				40	mA
		G5 INPUT ONLY				44	mA
		G6,G7 INPUTS ONLY				28	mA
V_{OH}	HIGH-LEVEL OUTPUT VOLTAGE		V_{CC}=4.5V, I_{OH}=-2mA	2.5	3.2		V
			V_{CC}=4.75V, I_{OH}=-2mA	2.7	3.2		V
V_{OL}	LOW-LEVEL OUTPUT VOLTAGE		V_{CC}=MIN, I_{OL}=MAX		0.3	0.5	V
I_{CCL}	SUPPLY CURRENT, OUTPUTS LOW		V_I=0V, V_{CC}=MAX		58	84	mA
I_{CCH}	SUPPLY CURRENT, OUTPUTS HIGH		V_I=4.5V, V_{CC}=MAX		72	105	mA

*ALL TYPICAL VALUES ARE AT V_{CC}=5V, T_A=25°C

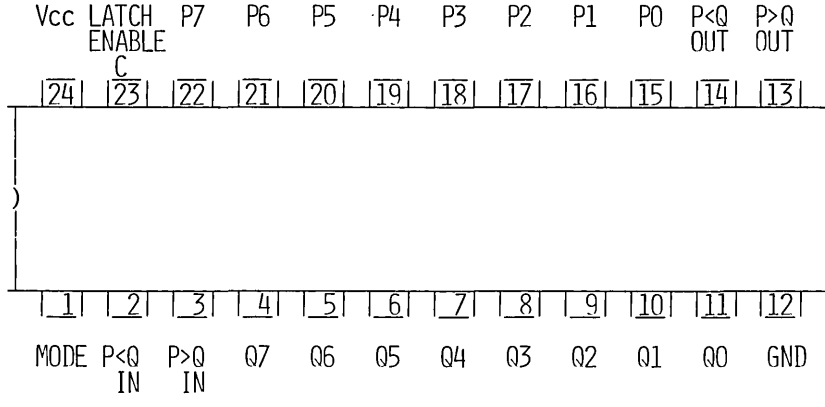
SWITCHING CHARACTERISTICS OVER RECOMMENDED T_A RANGE, V_{CC}=4.5 TO 5.5V, R_L=500 OHMS, C_L=50pF (UNLESS OTHERWISE NOTED). REFER TO PAGE 267 FOR LOAD CIRCUITS & WAVEFORMS.

PARAMETER		54AS/74AS882*			54AS882			74AS882			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
C_N TO ANY OUTPUT	TPLH		8		4		15	4		14	NS
	TPHL		6		4		12	4		10	NS
P OR G TO C_N + 8			4		2		9	2		8	NS
P OR G TO C_N + 16			4		2		9	2		8	NS
P OR G TO C_N + 24			6		2		11	2		10	NS
P OR G TO C_N + 32			8		2		13	2		12	NS

* 54AS/74AS882 VALUES ARE AT V_{CC} = 5V, T_A = 25°C, C_L = 50pF, R_L = 500 OHMS

* 8-BIT MAGNITUDE COMPARATORS IN IN A 24-PIN, 300-MIL PACKAGE
* CHOICE OF LOGICAL OR ARITHMETIC COMPARISON
* BUFFER-TYPE OUTPUTS DRIVE BUS LINES DIRECTLY
* BOTH INPUT PORTS FEATURE HYSTERESIS TO IMPROVE NOISE REJECTION
* ADVANCED OXIDE-ISOLATION, ION-IMPLANTED TTL SCHOTTKY PROCESS
* APPROXIMATELY TWICE THE AC PERFORMANCE OF SCHOTTKY TTL
* LATCHABLE P INPUT PORTS POWER-UP CLEAR

JT OR NT PACKAGE



THIS ADVANCED SCHOTTKY DEVICE HAS BEEN FABRICATED BY AN ADVANCED OXIDE-ISOLATED, ION-IMPLANTED TTL PROCESS DEVELOPED BY TI. THE MAJOR BENEFIT OF THIS PROCESS IS THE IMPROVEMENT OF THE SPEED-POWER PRODUCT BY THE REDUCTION OF PARASITIC AND SIDE-WALL CAPACITANCE AND ENHANCED F_T.

THIS DEVICE IS CAPABLE OF PERFORMING HIGH-SPEED LOGICAL OR ARITHMETIC COMPARISON (WHICH IS PERFORMED ON SIGN PLUS TWO'S COMPLEMENT DATA) ON TWO 8-BIT DATA WORDS. THE SELECTION OF THE TYPE OF COMPARISON IS ACCOMPLISHED BY THE MODE INPUT (REFER TO FUNCTION TABLE). THIS DEVICE HAS TWO CASCADING INPUTS, P>Q AND P<Q, FOR CASCADING PURPOSES. ANOTHER FEATURE OF THIS DEVICE IS THE LATCHING CAPABILITY FOR THE A INPUT WORD.

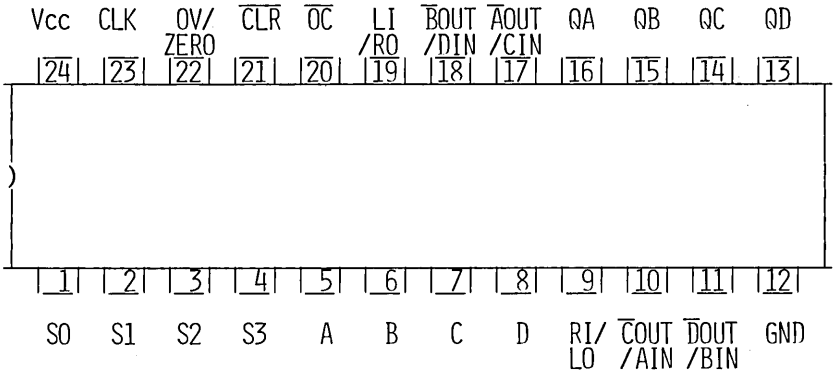
FUNCTION TABLE

COMPARISON	MODE INPUT	DATA INPUTS P0-P7, Q0-Q0	INPUTS P>Q	INPUTS P<Q	OUTPUTS P>Q	OUTPUTS P<Q
LOGICAL	H	P>Q	X	X	H	L
LOGICAL	H	P<Q	X	X	L	H
LOGICAL*	H	P=Q	H OR L	H OR L	H OR L	H OR L
ARITHMETIC	L	P AG Q	X	X	H	L
ARITHMETIC	L	Q AG P	X	X	L	H
ARITHMETIC*	L	P=Q	H OR L	H OR L	H OR L	H OR L

*IN THESE CASES THE P>Q OUTPUT WILL FOLLOW THE P>Q INPUT, AND THE P<Q OUTPUT WILL FOLLOW THE P<Q INPUT.

* EXPANDABLE MULTIFUNCTION BINARY/HEXIDECIMAL SCALERS IN A 24-PIN, 300-MIL PACKAGE
* BUFFER-TYPE OUTPUTS DRIVE BUS LINES DIRECTLY
* 100-MHZ TYP SHIFT RATE
* ADVANCED OXIDE-ISOLATION, ION-IMPLANTED TTL SCHOTTKY PROCESS
* APPROXIMATELY TWICE THE AC PERFORMANCE OF SCHOTTKY TTL

JT OR NT PACKAGE



THIS ADVANCED SCHOTTKY DEVICE HAS BEEN FABRICATED BY AN ADVANCED OXIDE-ISOLATED, ION-IMPLANTED TTL PROCESS DEVELOPED BY TI. THE MAJOR BENEFIT OF THIS PROCESS IS THE IMPROVEMENT OF THE SPEED-POWER PRODUCT BY THE REDUCTION OF PARASITIC AND SIDE-WALL CAPACITANCE AND ENHANCED F_T.

THIS DEVICE FEATURES A 4-BIT SHIFT REGISTER CAPABLE OF BEING USER PROGRAMMABLE (VIA THE FOUR INPUT SELECT LINES S0-S3) TO PERFORM ARITHMETIC AND LOGICAL SHIFTS IN BOTH DIRECTIONS AND TO PERFORM 2- OR 3-PLACE SCALING. THE SIX COMMON I/O PORTS (RI/LO, LI/RO, AND $\overline{\text{AOUT}}$/CIN-$\overline{\text{DOUT}}$/AIN) ENABLE THESE FUNCTIONS TO BE N-BIT CASCADABLE. THE SHIFT REGISTER CAN BE SYNCHRONOUSLY LOADED VIA THE DATA INPUT LINES A-D WITH EITHER TRUE OR COMPLEMENT DATA. IN THE SCALE MODES, DATA ON INPUT LINES A-D WILL BE ASYNCHRONOUSLY AND TRANSPARENTLY SCALED UNTIL A SYNCHRONOUS MODE IS SELECTED AT WHICH TIME THE CURRENT DATA WILL BE LATCHED INTO THE STORAGE ELEMENTS. ONCE DATA IS IN THE REGISTER, IT CAN BE SHIFTED LEFT OR RIGHT SYNCHRONOUSLY (ON THE POSITIVE CLOCK EDGE). THE STORAGE REGISTER CAN ALSO BE CLEARED VIA THE CLEAR INPUT LINE. THE CLOCK INPUT SELECTS CHOICE OF DETECTION OF EITHER OVERFLOW OF $Q_D \oplus Q_C$ OR ALL ZERO'S ON THE STORAGE REGISTER OUTPUTS. THE HIGH-IMPEDANCE STATE OF THE FOUR 3-STATE BUFFER TYPE OUTPUTS QA-QD (WHICH ARE FED DIRECTLY FROM THE STORAGE REGISTER) IS CONTROLLED BY THE OUTPUT CONTROL INPUT $\overline{\text{OC}}$.

Programmable Logic Arrays

TYPES FP54ALS16L8, FP54ALS16R8, FP54ALS16R6, FP54ALS16R4
FP74ALS16L8, FP74ALS16R8, FP74ALS16R6, FP74ALS16R4
FIXED-OR ARRAYS

* 'ALS VERSIONS OF 4 POPULAR PAL®* DEVICES

  TWICE AS FAST, TYPICAL PROPAGATION DELAY . . . 12NS

  IDENTICAL PROGRAMMING PROCEDURE

  PIN FOR PIN COMPATIBLE

DESCRIPTION

THESE FIXED-OR ARRAYS COMBINE THE ADVANCED LOW-POWER SCHOTTKY TECHNOLOGY WITH PROVEN TiW FUSE LINKS TO PROVIDE A RELIABLE, HIGH-PERFORMANCE REPLACEMENT FOR CONVENTIONAL TTL, WITH THE ADVANTAGE OF QUICK DESIGN CHANGES AND MORE COMPACT BOARDS.

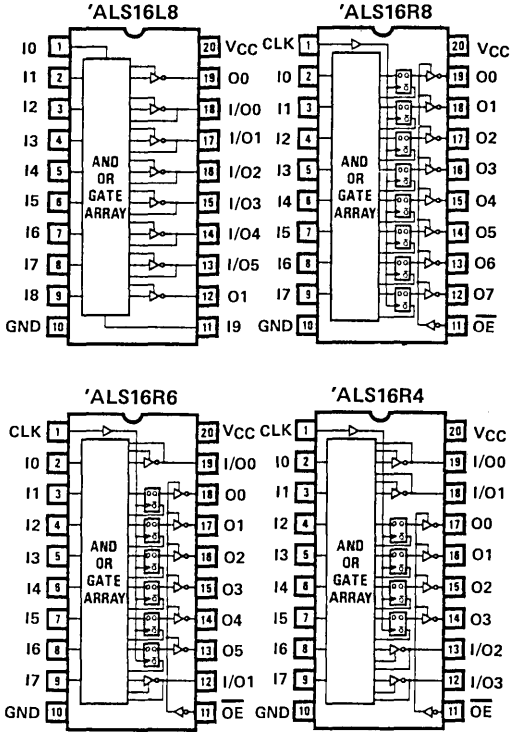
THE DEVICES WITH REGISTERS STORE THE OUTPUT OF THE AND-OR ARRAY ON THE HIGH-TO-LOW TRANSITION OF THE CLOCK.

ORDERING INFORMATION

FP 74ALS 16 R 6 N

* PREFIX
  - FP-STANDARD PREFIX
  - FPM-MACH IV, LEVEL I
  - FPC-MACH IV, LEVEL III
* 74 - 0°C TO 70°C
  54 - -55°C TO 125°C
* ALS - ADVANCED LOW-POWER SCHOTTKY PROCESS
* NUMBER OF ARRAY INPUTS
* OUTPUT TYPES:
  - L - ACTIVE LOW
  - R - REGISTERED
* NUMBER OF SPECIAL OUTPUTS
* PACKAGE TYPE

J OR N PACKAGE (TOP VIEW)



PROGRAMMERS		
MANUFACTURER	PERSONALITY CARD	SOCKET ADAPTOR
STRUCTURED DESIGN	SD-20/24	
DATA I/O CORP.	SYSTEM 19 919-1427	715-1428-2
PRO-LOG CORP.	PM9068	

PART #	DESCRIPTION
'ALS16L8	OCTAL 16-INPUT AND-OR-INVERT GATE ARRAY
'ALS16R8	OCTAL 16-INPUT REGISTERED AND-OR GATE ARRAY
'ALS16R6	HEX 16-INPUT REGISTERED AND-OR GATE ARRAY
'ALS16R4	QUAD 16-INPUT REGISTERED AND-OR GATE ARRAY

*PAL IS THE REGISTERED TRADEMARK OF MONOLITHIC MEMORIES, INC.

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, V_{CC}	7V
INPUT VOLTAGE	5.5V
OFF-STATE OUTPUT VOLTAGE	5.5V
STORAGE TEMPERATURE	-65° TO 150°C

RECOMMENDED OPERATING CONDITIONS

		FP54ALS'			FP74ALS'			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
V_{CC}	SUPPLY VOLTAGE	4.5	5	5.5	4.75	5	5.25	V
I_{OH}	HIGH-LEVEL OUTPUT CURRENT			-1			-2.6	mA
I_{OL}	LOW-LEVEL OUTPUT CURRENT			12			24	mA
T_A	OPERATING FREE-AIR TEMPERATURE	-55		125	0		70	°C

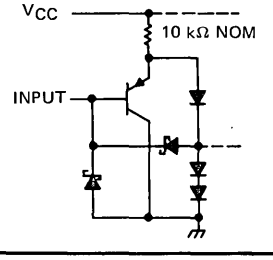
ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)

PARAMETER		TEST CONDITIONS		FP54ALS' MIN	FP54ALS' TYP*	FP54ALS' MAX	FP74ALS' MIN	FP74ALS' TYP*	FP74ALS' MAX	UNIT
V_{IH}	HIGH-LEVEL INPUT VOLTAGE			2			2			V
V_{IL}	LOW-LEVEL INPUT VOLTAGE					0.8			0.8	V
V_{IK}	INPUT CLAMP VOLTAGE	V_{CC} = MIN, I_I = -18mA				-1.5			-1.5	V
V_{OH}	HIGH-LEVEL OUTPUT VOLTAGE	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = 2V		2.4	3.2		2.4	3.3		V
V_{OL}	LOW-LEVEL OUTPUT VOLTAGE	V_{CC} = MIN, V_{IH} = 2V, I_{OL} = MAX, V_{IL} = 0.8V			0.25	0.4		0.35	0.5	V
I_I	INPUT CURRENT AT MAX INPUT VOLTAGE	V_{CC} = MAX, V_{IH} = 5.5V				0.1			0.1	mA
I_{IH}	HIGH-LEVEL INPUT CURRENT	V_{CC} = MAX, V_{IH} = 2.7V				20			20	uA
I_{IL}	LOW-LEVEL INPUT CURRENT	V_{CC} = MAX, V_{IL} = 0.4V				-0.4			-0.4	mA
I_O	OUTPUT CURRENT	V_O = 2.25V		-15	-33	-65	-15	-33	-65	mA
I_{OZH}	OFF-STATE OUTPUT CURRENT, HIGH-LEVEL VOLTAGE APPLIED	V_{CC}=MAX, V_{IH}=2V, V_{IL}=.8V, V_O=2.7V	0 PINS			20			20	uA
			I/O PINS			100			100	
I_{OZL}	OFF-STATE OUTPUT CURRENT, LOW-LEVEL VOLTAGE APPLIED	V_{CC}=MAX, V_{IH}=2V, V_{IL}=.8V, V_O=0.4V	0 PINS			-20			-20	uA
			I/O PINS			-100			-100	
I_{CC}	SUPPLY CURRENT	V_{CC}=MAX, V_I=0V, OUTPUTS OPEN	16L8		110	210		110	180	mA
			16R8,6,4		115	225		115	190	

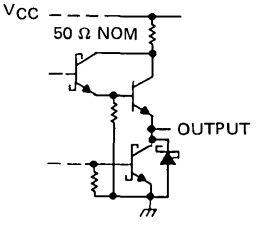
*ALL TYPICAL VALUES ARE AT V_{CC} = 5 V, T_A = 25°C

SCHEMATICS OF INPUTS AND OUTPUTS

EQUIVALENT OF EACH INPUT



TYPICAL OF OUTPUTS



TEXAS INSTRUMENTS
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'ALS16R8, 'ALS16R6, 'ALS16R4 TIMING REQUIREMENTS

		MIN	MAX	UNIT
CLOCK FREQUENCY, FCLOCK		0	35	MHz
WIDTH OF CLOCK PULSE, TW	HIGH	12		NS
	LOW	12		
SETUP TIME FROM INPUT OR FEEDBACK, TSU		15		NS
HOLD TIME, TH		0		NS

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C

	PARAMETER	TEST CONDITIONS	FP54ALS' MIN	FP54ALS' TYP	FP54ALS' MAX	FP74ALS' MIN	FP74ALS' TYP	FP74ALS' MAX	UNIT
FMAX	MAXIMUM CLOCK FREQUENCY		35			35			MHz
TPLH	INPUT OR FEEDBACK TO NON-REGISTERED OUTPUT	R_L = 500 OHM TO GND, C_L = 50pF TO GND		12			12		NS
TPHL				12			12		
TPLH	CLOCK TO OUTPUT OR FEEDBACK NOT APPLICABLE TO '16L8			10			10		NS
TPHL				10			10		
TPZH	OUTPUT ENABLE TIME FROM OE NOT APPLICABLE TO '16L8	R_{L1} = 500 OHM TO 7 V, R_{L2} = 500 OHM TO GND, C_L = 50pF TO GND		8			8		NS
TPZL				8			8		
TPHZ	OUTPUT DISABLE TIME FROM OE NOT APPLICALBE TO '16L8			8			8		NS
TPLZ				8			8		
TPZH	OUTPUT ENABLE TIME FROM I INPUT NOT APPLICABLE TO '16R8			12			12		NS
TPZL				12			12		
TPHZ	OUTPUT DISABLE TIME FROM I INPUT NOT APPLICABLE TO '16R8			12			12		NS
TPLZ				12			12		

PROGRAMMING PARAMETERS, T_A = 25°C

	PARAMETER		MIN	NOM	MAX	UNIT
VIHH	PROGRAM-LEVEL INPUT VOLTAGE		11	11.5	12	V
IIHH	PROGRAM-LEVEL INPUT CURRENT	OUTPUT PROGRAM PULSE			50	mA
		OE, I/R			25	
		ALL OTHER INPUTS			5	
ICCH	PROGRAM SUPPLY CURRENT				400	mA
TP	PROGRAM PULSE WIDTH		10		50	US
TD	DELAY TIME		100			NS
TDV	DELAY TIME TO VERIFY		100			US
	PROGRAM PULSE DUTY CYCLE				25	%
	VERIFY-PROTECT-INPUT VOLTAGE		20	21	22	V
	VERIFY-PROTECT-INPUT CURRENT				400	mA
	VERIFY-PROTECT-PULSE WIDTH		20		50	MS

Programming Procedure

The fuses are programmed using a low-voltage linear-select procedure. The array is divided into two groups, products 0 thru 31 and products 32 thru 63, for which pin identifications are shown in the pin configurations on following page. To program a particular fuse, both an input line and a product line are selected according to the following procedure:

Step 1 Raise Output Enable, $\overline{OE}$, to V_{IHH}.
Step 2 Select an input line by applying voltages to I_0, I_1, I_2, I_3, I_4, I_5, I_6, I_7, and L/R, as shown in Table 1.
Step 3 Select a product line by applying voltages to A_0, A_1, and A_2 as shown in Table 2.
Step 4 Raise V_{CC} (pin 20) to V_{IHH}.
Step 5 Program the fuse by pulsing the output O3, O2, O1, or O0 of the selected product group to V_{IHH} as shown in Table 2.
Step 6 Lower V_{CC} (pin 20) to 6.0 V.
Step 7 Pulse the CLOCK pin and verify the output pin, O3, O2, O1, or O0 to be Low.
Step 8 Lower V_{CC} (pin 20) to 4.5 V and repeat step 7.
Step 9 Should the output not verify, repeat steps 1 thru 8 up to five (5) times.

This procedure is repeated for all fuses to be blown (see Programming Waveforms).

To prevent further verification, two last fuses may be blown by raising pin 1 and pin 11 to V_P. V_{CC} is not required during this operation.

Voltage Legend:
L = Low-level input voltage, V_{IL} HH = High-level program, V_{IHH}
H = High-level input voltage, V_{IH} Z = High impedance (e.g., 10 kilohms to 5 V)

INPUT LINE NUMBER	PIN IDENTIFICATION								
	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	L/R
0	HH	HH	HH	HH	HH	HH	HH	L	Z
1	HH	HH	HH	HH	HH	HH	HH	H	Z
2	HH	HH	HH	HH	HH	HH	HH	L	HH
3	HH	HH	HH	HH	HH	HH	HH	H	HH
4	HH	HH	HH	HH	HH	HH	L	HH	Z
5	HH	HH	HH	HH	HH	HH	H	HH	Z
6	HH	HH	HH	HH	HH	HH	L	HH	HH
7	HH	HH	HH	HH	HH	HH	H	HH	HH
8	HH	HH	HH	HH	HH	L	HH	HH	Z
9	HH	HH	HH	HH	HH	H	HH	HH	Z
10	HH	HH	HH	HH	HH	L	HH	HH	HH
11	HH	HH	HH	HH	HH	H	HH	HH	HH
12	HH	HH	HH	HH	L	HH	HH	HH	Z
13	HH	HH	HH	HH	H	HH	HH	HH	Z
14	HH	HH	HH	HH	L	HH	HH	HH	HH
15	HH	HH	HH	HH	H	HH	HH	HH	HH
16	HH	HH	HH	L	HH	HH	HH	HH	Z
17	HH	HH	HH	H	HH	HH	HH	HH	Z
18	HH	HH	HH	L	HH	HH	HH	HH	HH
19	HH	HH	HH	H	HH	HH	HH	HH	HH
20	HH	HH	L	HH	HH	HH	HH	HH	Z
21	HH	HH	H	HH	HH	HH	HH	HH	Z
22	HH	HH	L	HH	HH	HH	HH	HH	HH
23	HH	HH	H	HH	HH	HH	HH	HH	HH
24	HH	L	HH	HH	HH	HH	HH	HH	Z
25	HH	H	HH	HH	HH	HH	HH	HH	Z
26	HH	L	HH	HH	HH	HH	HH	HH	HH
27	HH	H	HH	HH	HH	HH	HH	HH	HH
28	L	HH	HH	HH	HH	HH	HH	HH	Z
29	H	HH	HH	HH	HH	HH	HH	HH	Z
30	L	HH	HH	HH	HH	HH	HH	HH	HH
31	H	HH	HH	HH	HH	HH	HH	HH	HH

TABLE 1 INPUT LINE SELECT

PRODUCT LINE NUMBER	PIN IDENTIFICATION						
	O_3	O_2	O_1	O_0	A_2	A_1	A_0
0,32	Z	Z	Z	HH	Z	Z	Z
1,33	Z	Z	Z	HH	Z	Z	HH
2,34	Z	Z	Z	HH	Z	HH	Z
3,35	Z	Z	Z	HH	Z	HH	HH
4,36	Z	Z	Z	HH	HH	Z	Z
5,37	Z	Z	Z	HH	HH	Z	HH
6,38	Z	Z	Z	HH	HH	HH	Z
7,39	Z	Z	Z	HH	HH	HH	HH
8,40	Z	Z	HH	Z	Z	Z	Z
9,41	Z	Z	HH	Z	Z	Z	HH
10,42	Z	Z	HH	Z	Z	HH	Z
11,43	Z	Z	HH	Z	Z	HH	HH
12,44	Z	Z	HH	Z	HH	Z	Z
13,45	Z	Z	HH	Z	HH	Z	HH
14,46	Z	Z	HH	Z	HH	HH	Z
15,47	Z	Z	HH	Z	HH	HH	HH
16,48	Z	HH	Z	Z	Z	Z	Z
17,49	Z	HH	Z	Z	Z	Z	HH
18,50	Z	HH	Z	Z	Z	HH	Z
19,51	Z	HH	Z	Z	Z	HH	HH
20,52	Z	HH	Z	Z	HH	Z	Z
21,53	Z	HH	Z	Z	HH	Z	HH
22,54	Z	HH	Z	Z	HH	HH	Z
23,55	Z	HH	Z	Z	HH	HH	HH
24,56	HH	Z	Z	Z	Z	Z	Z
25,57	HH	Z	Z	Z	Z	Z	HH
26,58	HH	Z	Z	Z	Z	HH	Z
27,59	HH	Z	Z	Z	Z	HH	HH
28,60	HH	Z	Z	Z	HH	Z	Z
29,61	HH	Z	Z	Z	HH	Z	HH
30,62	HH	Z	Z	Z	HH	HH	Z
31,63	HH	Z	Z	Z	HH	HH	HH

TABLE 2 PRODUCT LINE SELECT

TEXAS INSTRUMENTS
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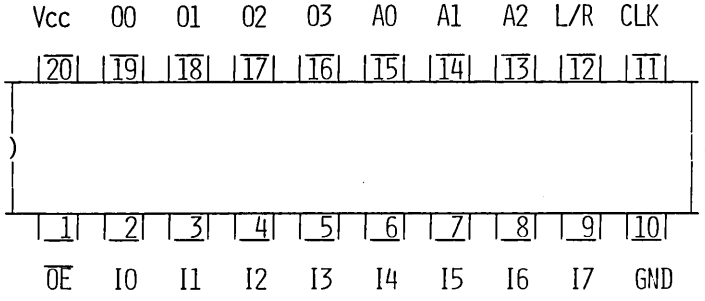
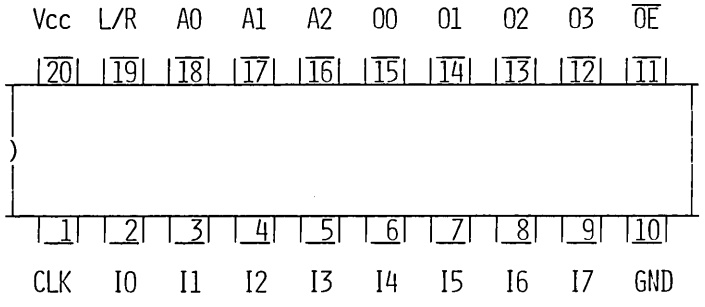
PIN CONFIGURATIONS FOR PROGRAMMING ONLY

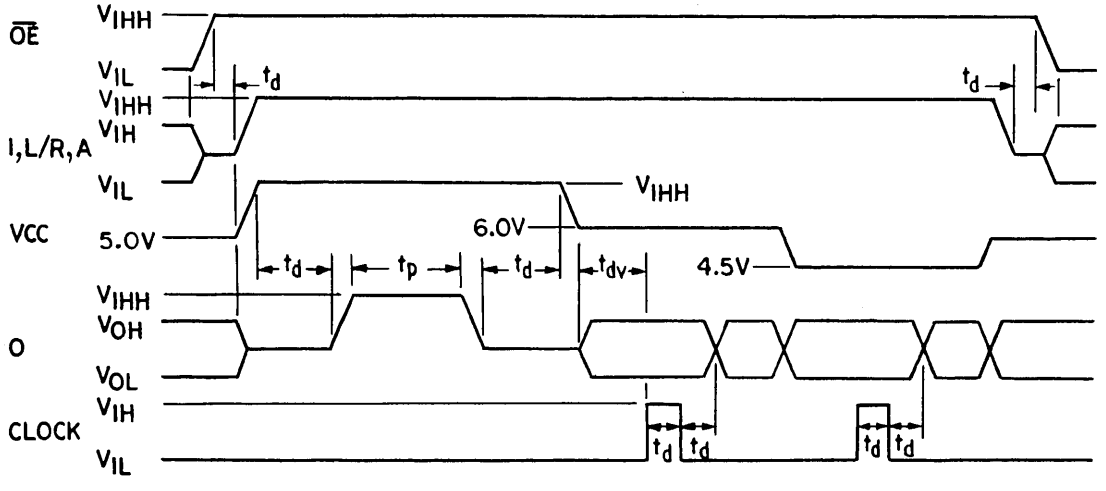
PRODUCTS 0 THRU 31



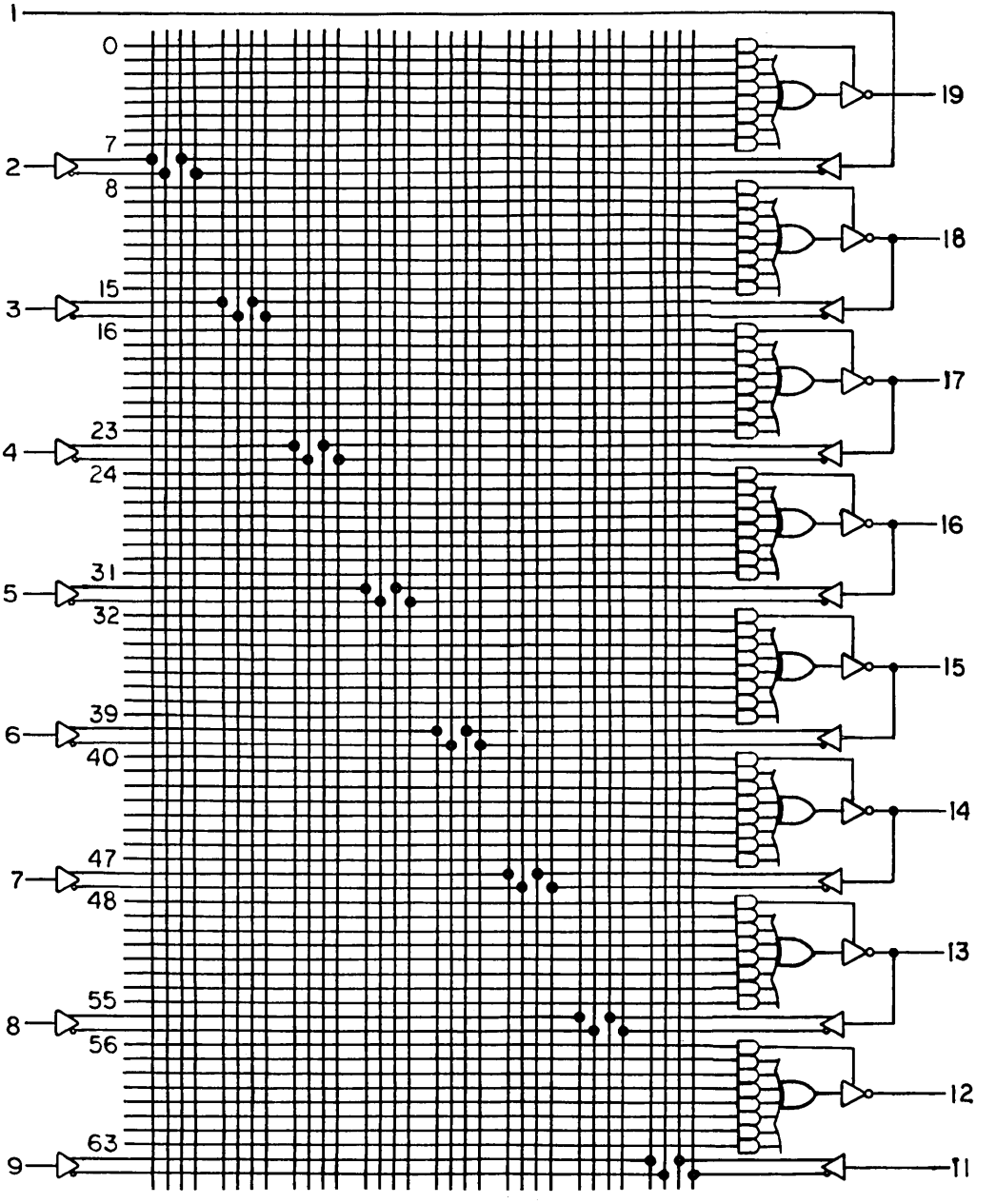
PRODUCTS 32 THRU 63



PROGRAMMING WAVEFORMS



LOGIC DIAGRAM



TEXAS INSTRUMENTS
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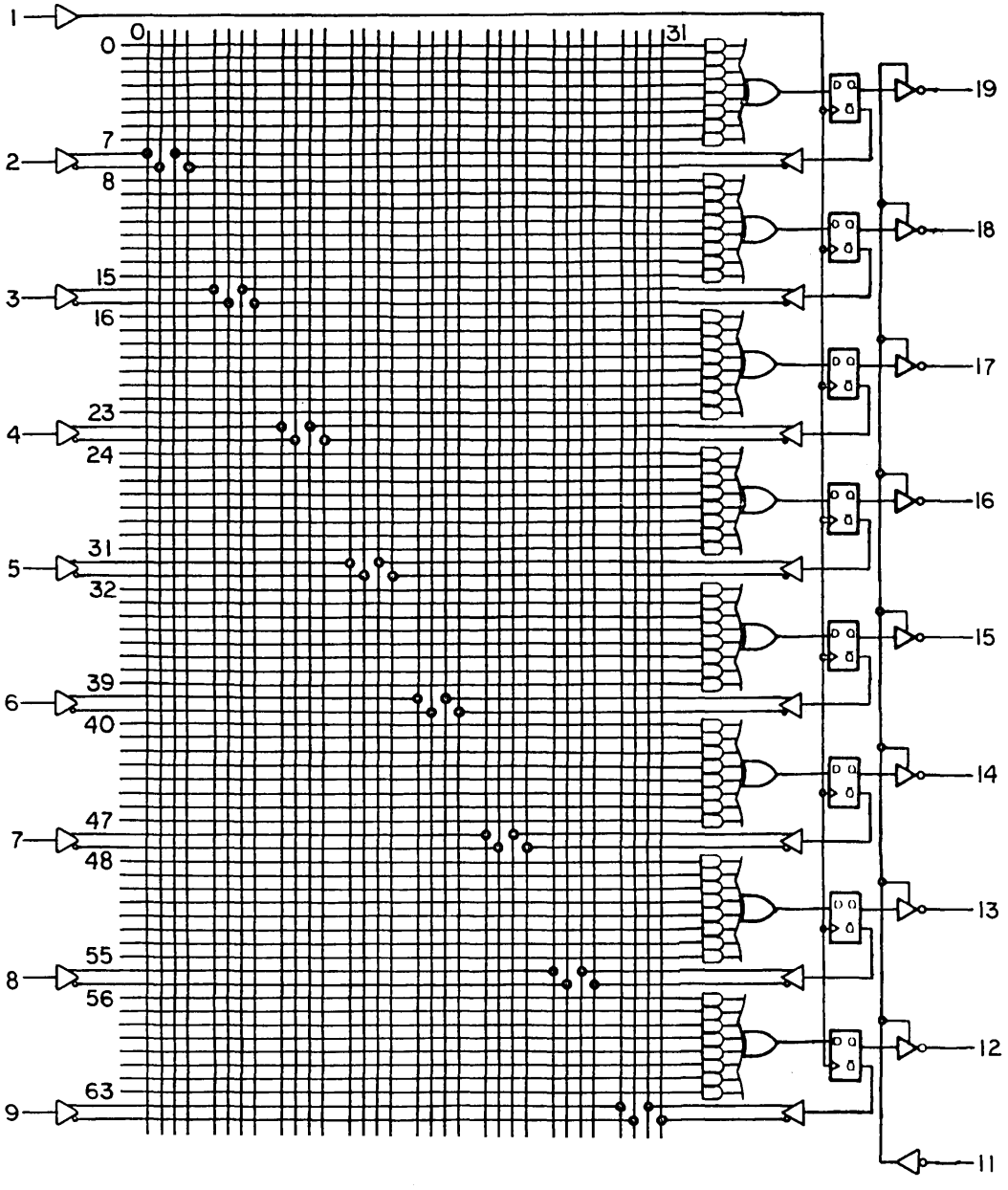
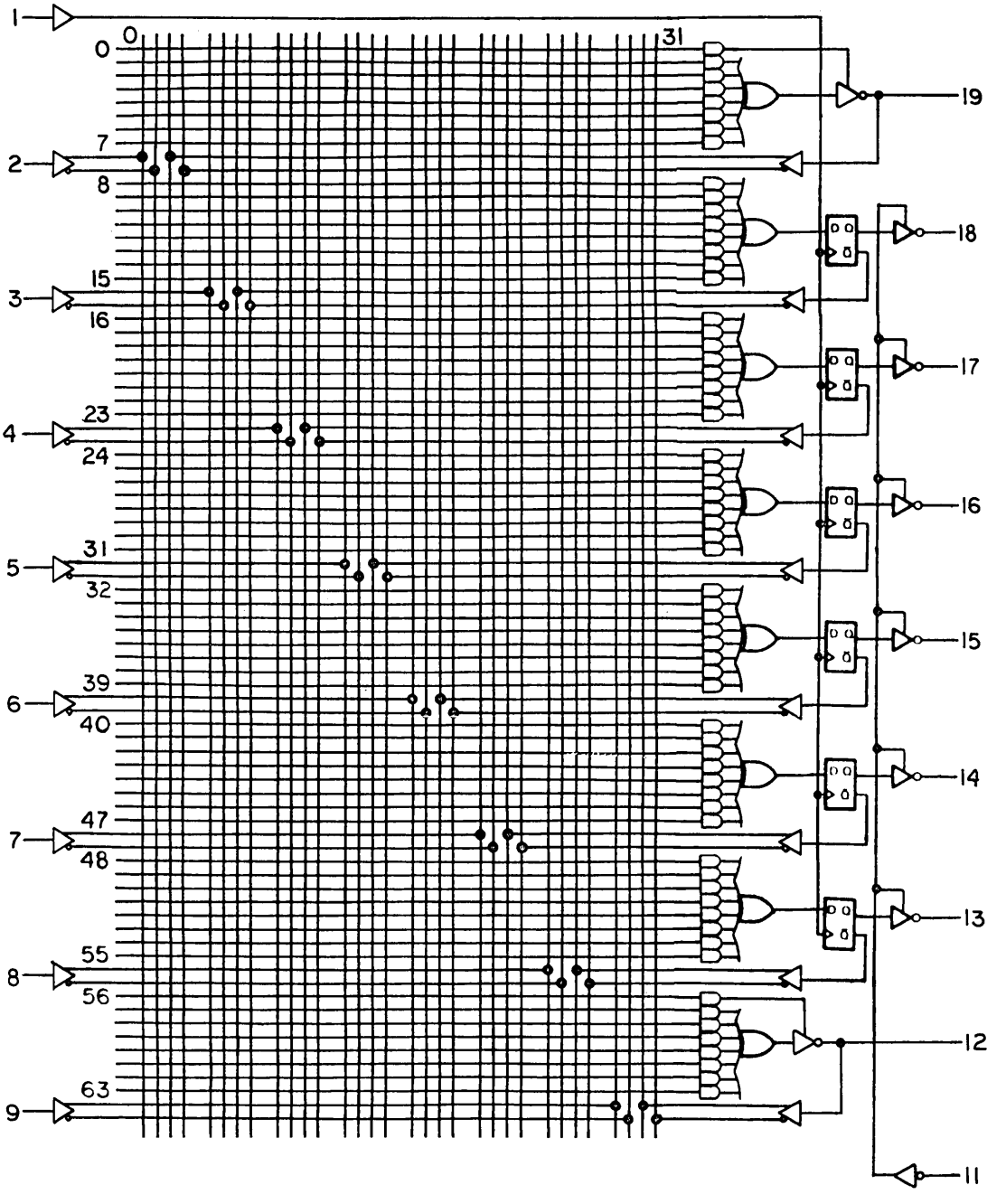
LOGIC DIAGRAM



LOGIC DIAGRAM



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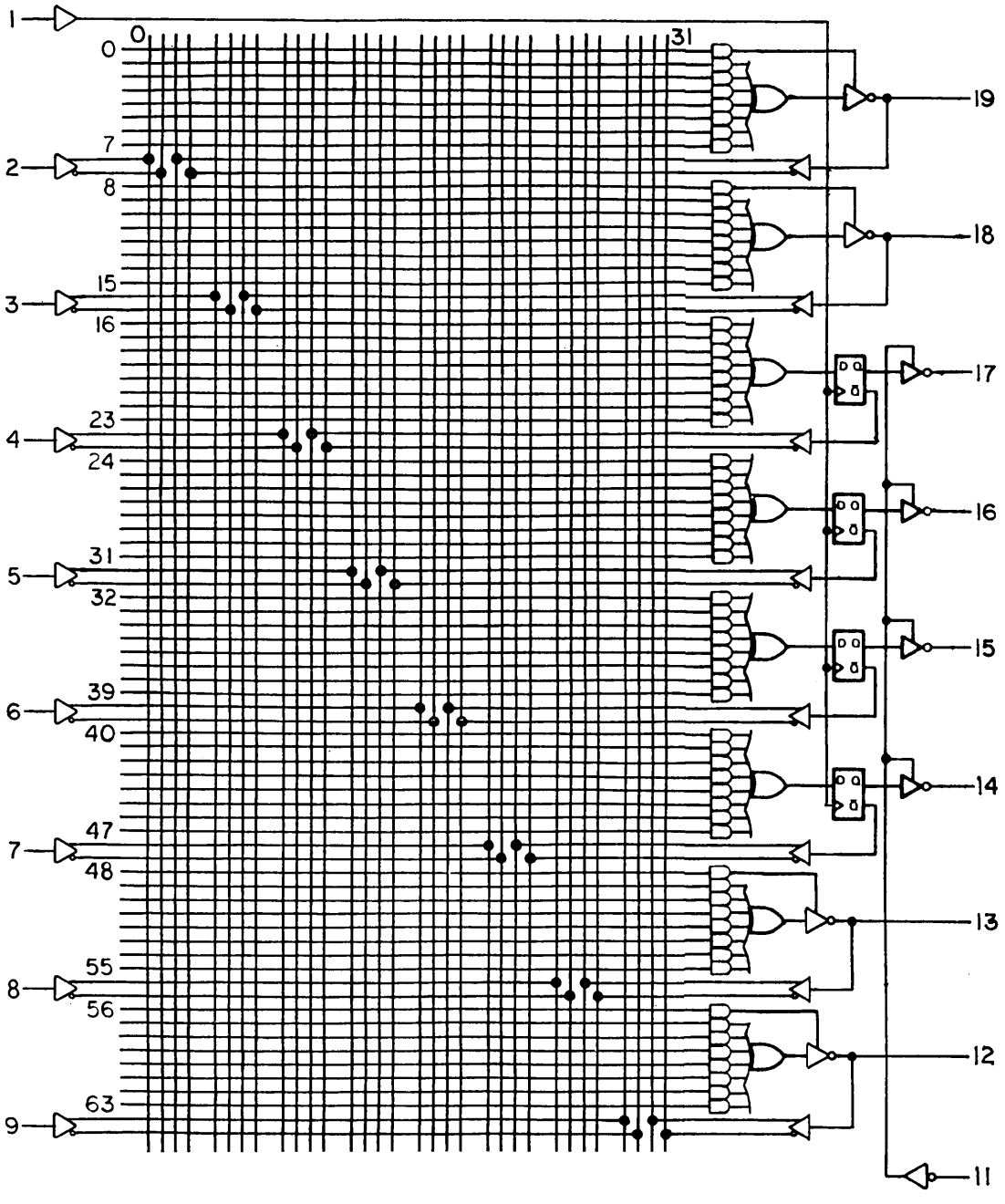
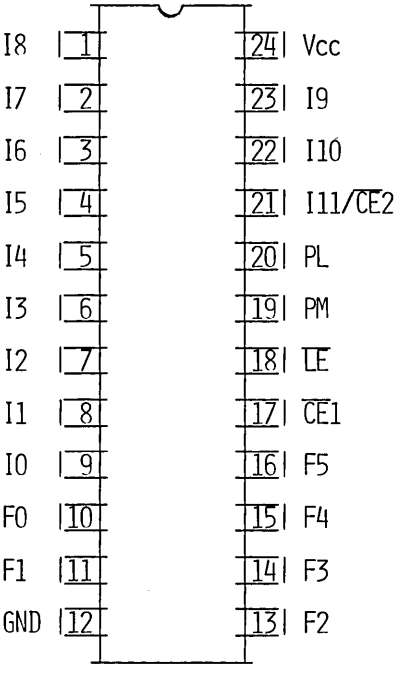
LOGIC DIAGRAM



TYPES FP54LS333, FP54LS335, FP74LS333, FP74LS335
FIELD-PROGRAMMABLE LOGIC SEQUENCERS

- 45 ns TYPICAL INPUT to OUTPUT PROPAGATION DELAY
- 24-PIN, 300-mil SLIM LINE PACKAGES
- LOW-POWER, 350 mW TYPICAL POWER DISSIPATION
- 12 INPUT VARIABLES
- 32 PRODUCT TERMS
- 6-BIT OUTPUT LATCH
- 4-BIT STATE REGISTER

JT or NT PACKAGE
(TOP VIEW)



DESCRIPTION

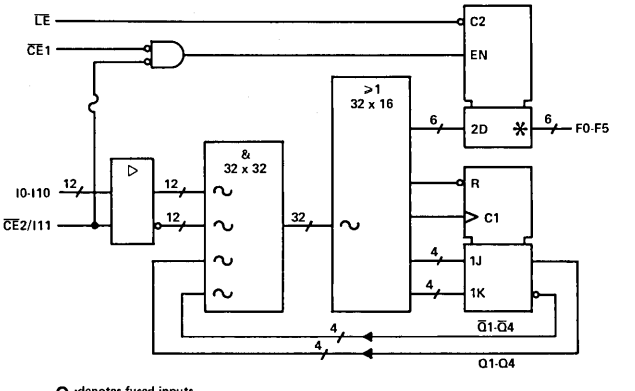
The 'LS333 (three-state outputs) and the 'LS335 (open-collector outputs) are Low-Power Schottky Bipolar TTL field-programmable logic sequencers designed to solve state-machine problems of the Mealy type. They contain four completely buried J-K flip-flops in the feedbath path between the OR and AND matrices. The common clock and clear lines are also programmable by separate OR terms, in addition to the four J inputs and four K inputs.

The output-function levels are stored by a common asynchronous latch enable pin ($\overline{LE}$) that controls the 6-Bit output transparent latches.

Pin 21 is a user programmable option: it must be programmed to function as a 12th input or as a chip enable AND'ed with pin 17 for 3-state control of the outputs. An auto chip-enable option for expansion of terms is available through the manufacturer.

The program mode (PM), and the program latch (PL) pins are unique programming control inputs that simplify the programming procedure as described later. These pins are to be grounded during normal device operation.

FUNCTIONAL BLOCK DIAGRAM
(POSITIVE LOGIC)



denotes fused inputs.
* 'LS333 has 3-state (▽) outputs; 'LS335 has open-collector (Ω) outputs.

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ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, V_{CC}	7V
INPUT VOLTAGE	7V
OFF-STATE OUTPUT VOLTAGE	5.5V
STORAGE TEMPERATURE	-65° TO 150°C

RECOMMENDED OPERATING CONDITIONS

		FP54LS'			FP74LS'			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
V_{CC}	SUPPLY VOLTAGE	4.5	5	5.5	4.75	5	5.25	V
I_{OH}	HIGH-LEVEL OUTPUT CURRENT			-1			-2.6	mA
I_{OL}	LOW-LEVEL OUTPUT CURRENT			12			24	mA
T_A	OPERATING FREE-AIR TEMPERATURE	-55		125	0		70	°C

ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)

PARAMETER		TEST CONDITIONS	FP54LS' MIN	FP54LS' TYP*	FP54LS' MAX	FP74LS' MIN	FP74LS' TYP*	FP74LS' MAX	UNIT
V_{IH}	HIGH-LEVEL INPUT VOLTAGE		2			2			V
V_{IL}	LOW-LEVEL INPUT VOLTAGE				0.7			0.8	V
V_{IK}	INPUT CLAMP VOLTAGE	V_{CC}=MIN, I_I=-18mA			-1.5			-1.5	V
V_{OH}	HIGH-LEVEL OUTPUT VOLTAGE	V_{CC}=MIN, V_{IH}=2V, V_{IL}=MAX, I_{OH}=MAX	2.4	3.1		2.4	3.1		V
V_{OL}	LOW-LEVEL OUTPUT VOLTAGE	V_{CC}=MIN, V_{IH}=2V, V_{IH}=MAX, I_{OL}=MAX		0.25	0.4		0.25	0.4	V
I_I	INPUT CURRENT AT MAXIMUM INPUT VOLTAGE	V_{CC}=MAX, V_{IH}=5.5V			0.1			0.1	mA
I_{IH}	HIGH-LEVEL INPUT CURRENT	V_{CC}=MAX, V_{IH}=2.7V			20			20	uA
I_{IL}	LOW-LEVEL INPUT CURRENT	V_{CC}=MAX, V_{IL}=0.4V, PL			-0.4			-0.4	mA
		V_{CC}=MAX, V_{IL}=0.4V, ALL OTHER			-0.2			-0.2	mA
I_O	OUTPUT CURRENT	V_O=2.25V	-15		-65	-15		-65	mA
I_{OZH}	OFF-STATE OUTPUT CURRENT, HIGH-LEVEL VOLTAGE APPLIED	V_{CC}=MAX, CE1@2V, V_O=2.7V			20			20	uA
I_{OZL}	OFF-STATE OUTPUT CURRENT, LOW-LEVEL VOLTAGE APPLIED	V_{CC}=MAX, CE1@2V, V_O=2.7V			-20			-20	uA
I_{CC}	SUPPLY CURRENT	V_{CC}=MAX, CE1@4.5V, ALL OTHER INPUTS=0V		70			70		mA

*ALL TYPICAL VALUES ARE AT V_{CC} = 5V, T_A = 25°C

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TPLH, TPHL	INPUT TO OUTPUT	R_L = 667 OHMS, C_L = 45 pF			45	NS
TPLH, TPHL	CLOCK TO OUTPUT				65	NS
TPLH, TPHL	CLEAR TO OUTPUT				60	NS
TPXZ, TPZX	CE TO OUTPUT	R_L = 667 OHMS, C_L = 5 pF			20	NS
TPLH, TPHL	LE TO OUTPUT				25	NS
TPXZ, TPZX	AUTO CHIP ENABLE TO OUTPUT				50	NS

PROGRAMMING PARAMETERS, T_A = 25°C

PARAMETER		MIN	NOM	MAX	UNIT
V_{IHH}	PROGRAM-LEVEL INPUT VOLTAGE	10	10.5	11	V
I_{CCH}	PROGRAM SUPPLY CURRENT		300		mA
TP	PROGRAM PULSE WIDTH	100		1000	us
TR	PROGRAM PULSE RISE TIME		100		NS
	PROGRAM PULSE DUTY CYCLE		25	35	%

Programming Procedure

I11/$\overline{CE2}$ INPUT

If pin 21 is to function as $\overline{CE2}$, both AND/$\overline{AND}$ links at each of the 32 product terms must be fused per AND matrix programming procedure creating a don't care for input I11. If it is to become the 12th data input, $\overline{CE2}$ is removed as follows:

Step 1: Set Vcc to 5 V, PM, PL, & GND to 0 V.
Step 2: Apply Vihh to IO-I11.
Step 3: Address product term 45 by applying its binary code to outputs F5 to F0 with F0 as LSB, using TTL logic levels, H=1 & L=0.
Step 4: a) Ramp PL to Vihh.
b) Pulse Vcc to Vihh.
c) Lower Vcc to 5 V.

AND MATRIX, input variables 0 to 11

Step 1: Set Vcc to 5V,PM,PL,& GND to 0 V.
Step 2: Apply the true logic level, either Vih or Vil, to the input to be programmed (only one at a time) and raise all remaining inputs to Vihh.
Step 3: Address the product term to be programmed (0-31). See Step 3 above.
Step 4: a) Ramp program latch (PL) to Vihh.
b) Pulse Vcc to Vihh for a MAX of 1 ms (35% duty cycle).
c) Return PL to 0 V.
Step 5: Disable the programmed input with Vihh.
Step 6: Repeat 2-5 for all other input variables and product terms.

AND MATRIX, Feedback input lines Q/$\overline{Q}$

Step 1: Set Vcc to 5 V, PM, PL, & GND to 0 V.
Step 2: Select the F/F output (to be programmed true) by applying TTL logic levels to inputs IO-I4 using the addresses in Table 1. Apply Vihh to I5-I11.
Step 3: Address the product term.
Step 4: a) Ramp PL to Vihh.
b) Disable inputs IO-I4 with Vihh.
c) Pulse Vcc to Vihh.
d) Return PL to OV.
Step 5: Repeat 2-4 for all other Q/$\overline{Q}$ AND input lines and product terms.

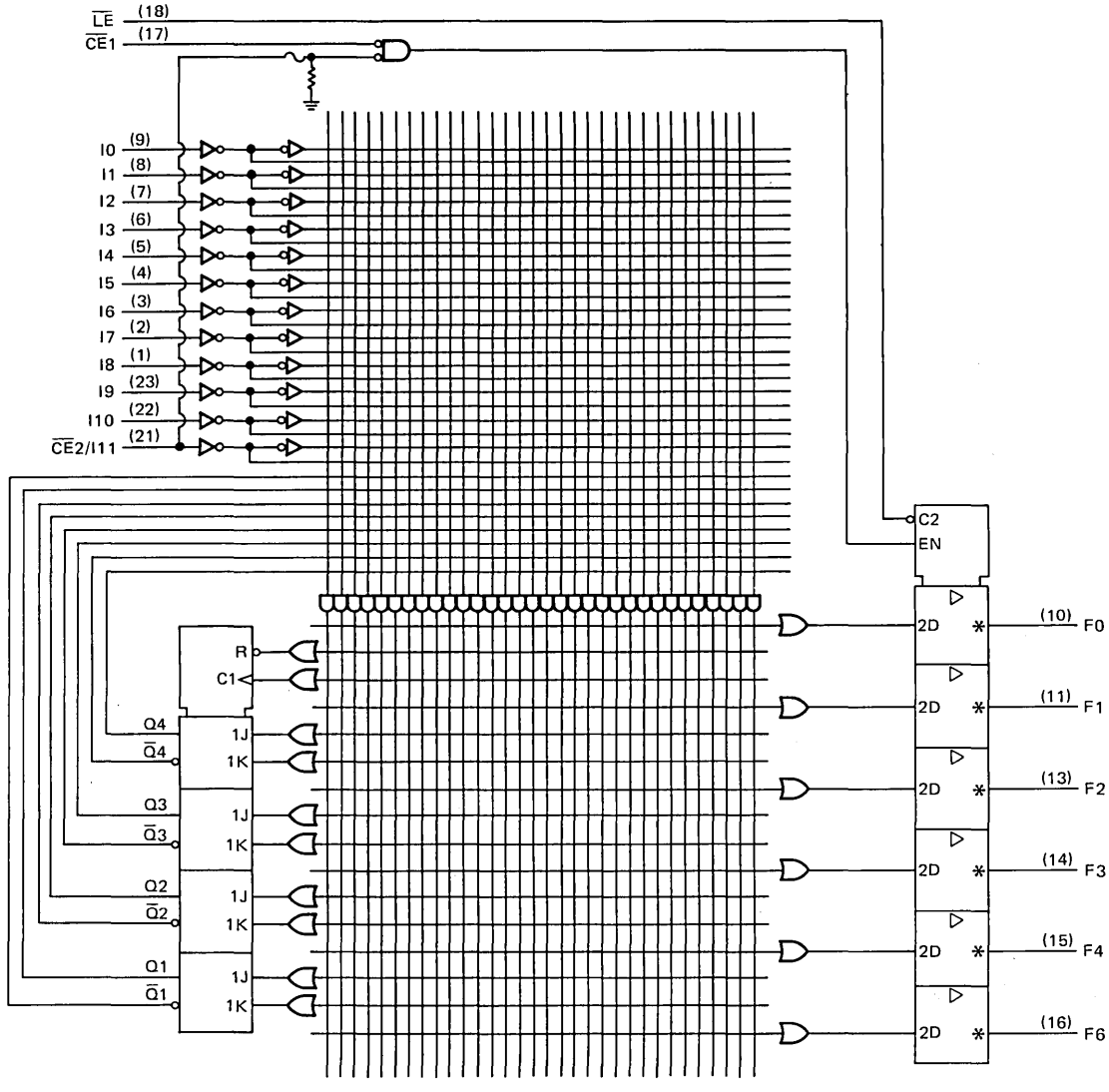
OR MATRIX

Step 1: Set Vcc to 5 V, PM to Vihh, PL and GND to 0 V.
Step 2: Select the output function or f/f input line by applying TTL logic levels to inputs IO to I4 using the addresses in Table 1. Apply Vihh to I5-I11.
Step 3: Ramp PL to 5 V.
Step 4: Disable inputs IO-I4 with Vihh.
Step 5: Address the product term.
Step 6: Pulse Vcc to Vihh.
Step 7: Repeat 5-6 for each of the product terms to be false in the addressed output function or f/f input line.
Step 8: Return PL to 0 V.
Step 9: Repeat 2-8 for each output function and f/f input line.

TABLE 1

ADDRESS APPLIED TO INPUTS I4 I3 I2 I1 I0	AND PROG MODE F/F OUTPUT TO BE TRUE	OR PROG MODE TERM TO BE FALSE IN SUM
L L L L L	Q4	CLK
L L L L H	$\overline{Q4}$	CLR
L L L H L	Q3	J4
L L L H H	$\overline{Q3}$	K4
L L H L L	Q2	J3
L L H L H	$\overline{Q2}$	K3
L L H H L	Q1	J2
L L H H H	$\overline{Q1}$	K2
L H L L L	NONE	J1
L H L L H		K1
L H L H L		F0
L H L H H		F1
L H H L L		F2
L H H L H		F3
L H H H L		F4
L H H H H		F5
H H H H H		NONE

LOGIC DIAGRAM

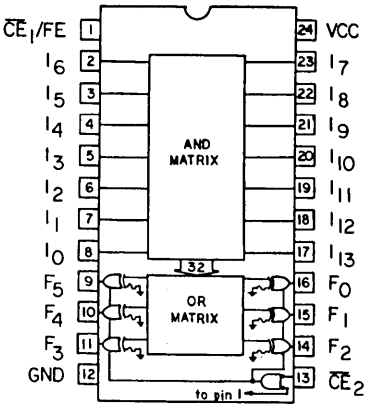


~denotes fused inputs.
*'LS333 has 3-state (▽) outputs; 'LS335 has open-collector (◇) outputs.

TYPES FP54AS839, FP54AS840, FP74AS839, FP74AS840
14 X 32 X 6 FIELD-PROGRAMMABLE LOGIC ARRAYS

JT OR NT PACKAGE

(TOP VIEW)



* 10 NS TYPICAL INPUT TO OUTPUT PROPAGATION DELAY
* 24-PIN, 300-MIL SLIM LINE PACKAGES
* 700 MW TYPICAL POWER DISSIPATION
* PROGRAMMABLE OUTPUT POLARITY

LOGIC FUNCTION

$F = P_0+P_1+\ldots+P_{31}$ FOR POLARITY LINK INTACT

$\overline{F} = P_0*P_1*\ldots*P_{31}$ FOR POLARITY LINK OPEN

WHERE P_0 THRU P_{31} ARE PRODUCT TERMS OF INPUT VARIABLES I_0 THRU I_{13}

DESCRIPTION

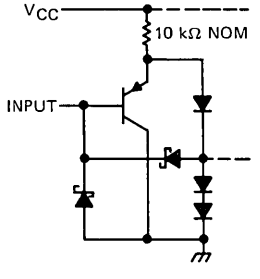
THE 'AS839 (THREE-STATE OUTPUTS) AND THE 'AS840 (OPEN-COLLECTOR OUTPUTS) ARE ADVANCED SCHOTTKY BIPOLAR TTL FIELD-PROGRAMMABLE LOGIC ARRAYS, CONTAINING 32 PRODUCT TERMS (AND TERMS), AND 6 SUM TERMS (OR TERMS). EACH OF THE 6 SUM-OF-PRODUCTS OUTPUT FUNCTIONS CAN BE PROGRAMMED EITHER TRUE ACTIVE-HIGH OR TRUE ACTIVE-LOW. THE TRUE OF EACH OUTPUT FUNCTION IS ACTIVATED BY THE PROGRAMMED LOGICAL MINTERMS OF 14 OR LESS INPUT VARIABLES. THE OUTPUTS ARE CONTROLLED BY TWO CHIP-ENABLE PINS ALLOWING OUTPUT INHIBIT AND EXPANSION OF TERMS.

THESE DEVICES ARE IDEALLY SUITED FOR HIGH-SPEED DATA PATH LOGIC REPLACEMENT, WHERE SEVERAL CONVENTIONAL SSI FUNCTIONS CAN BE DESIGNED INTO A SINGLE PACKAGE.

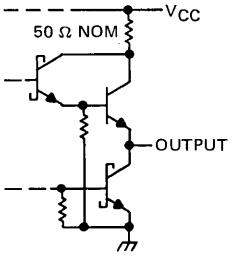
THE FP54AS839 AND FP54AS840 ARE CHARACTERIZED FOR OPERATION OVER THE FULL MILITARY TEMPERATURE RANGE OF -55°C TO 125°C. THE FP74AS839 AND FP74AS840 ARE CHARACTERIZED FOR OPERATION FROM 0°C TO 70°C.

SCHEMATICS OF INPUTS AND OUTPUTS

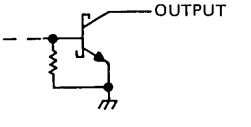
EQUIVALENT OF EACH INPUT



TYPICAL OF OUTPUTS OF 'AS839



TYPICAL OF OUTPUTS OF 'AS840



PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

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ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, V_{CC}	7V
INPUT VOLTAGE	5.5V
OFF-STATE OUTPUT VOLTAGE	5.5V
STORAGE TEMPERATURE	-65° TO 150°C

RECOMMENDED OPERATING CONDITIONS

	PARAMETER	FP54AS' MIN	FP54AS' NOM	FP54AS' MAX	FP74AS' MIN	FP74AS' NOM	FP74AS' MAX	UNIT
V_{CC}	SUPPLY VOLTAGE	4.5	5	5.5	4.75	5	5.25	V
I_{OH}	HIGH-LEVEL OUTPUT CURRENT			-12			-15	mA
I_{OL}	LOW-LEVEL OUTPUT CURRENT			32			48	mA
T_A	OPERATING FREE-AIR TEMPERATURE	-55		125	0		70	°C

ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)

PARAMETER		TEST CONDITION	FP54AS' MIN	FP54AS' TYP*	FP54AS' MAX	FP74AS' MIN	FP74AS' TYP*	FP74AS' MAX	UNIT
V_{IH}	HIGH-LEVEL INPUT VOLTAGE		2			2			V
V_{IL}	LOW-LEVEL INPUT VOLTAGE				0.8			0.8	V
V_{IK}	INPUT CLAMP VOLTAGE	V_{CC} = MIN, I_I = -18mA			-1.2			-1.2	V
V_{OH}	HIGH-LEVEL OUTPUT VOLTAGE	V_{CC} = MIN, V_{IL} =0.4V, I_{OH} = -2.6mA, V_{IH} =2V	2.4	3.2		2.4	3.4		V
V_{OL}	LOW-LEVEL OUTPUT VOLTAGE	V_{CC} = MIN, V_{IL} =0.8V, I_{OL} = 48mA, V_{IH} = 2V		0.25	0.5		0.37	0.5	V
I_I	INPUT CURRENT AT MAX INPUT VOLTAGE	V_{CC} = MAX, V_{IH} = 5.5V			0.1			0.1	mA
I_{IH}	HIGH-LEVEL INPUT CURRENT	V_{CC} = MAX, V_{IH} = 2.7V			20			20	uA
I_{IL}	LOW-LEVEL INPUT CURRENT	V_{CC} = MAX, V_{IL} = 0.4V			-2			-2	mA
I_O	OUTPUT CURRENT	V_O = 2.25V	-15	-33	-65	-15	-33	-65	mA
I_{OZH}	OFF-STATE OUTPUT CURRENT, HIGH-LEVEL VOLTAGE APPLIED	V_{CC} = MAX, V_{IH} = 2V, V_{IL} = 0.8V, V_O = 2.7V			50			50	uA
I_{OZL}	OFF-STATE OUTPUT CURRENT, LOW-LEVEL VOLTAGE APPLIED	V_{CC} = MAX, V_{IH} = 2V, V_{IL} = 0.8V, V_O = 0.4V			-50			-50	uA
I_{CC}	SUPPLY CURRENT	V_{CC} = 5V, V_I = 0V, $\overline{CE}$ INPUTS AT 5V		145			145		mA

*ALL TYPICAL VALUES ARE AT V_{CC} = 5 V, T_A = 25°C

4

SWITCHING CHARACTERISTICS, V_{CC} = +5V, T_A = 25°C

PARAMETER	FROM INPUT	TEST CONDITIONS	FP54AS' MIN	FP54AS' TYP	FP54AS' MAX	FP74AS' MIN	FP74AS' TYP	FP74AS' MAX	UNIT
TPLH		OUTPUT FUSE INTACT, C_L=45pF, R_L=667 OHMS		10			10		NS
TPHL				10			10		
TPLH		OUTPUT FUSE OPEN, C_L=45pF, R_L=667 OHMS		11			11		NS
TPHL				12			12		
TPZH	PIN 1 OR 13	C_L=5pF		6			6		NS
TPZL				6			6		
TPHZ	PIN 1 OR 13	C_L=5pF		6			6		NS
TPLZ				6			6		

PROGRAMMING PARAMETERS, T_A = 25°C

	PARAMETER		MIN	NOM	MAX	UNIT
V_{IHH}	POLARITY AND FUSE ENABLE PROGRAM-LEVEL INPUT VOLTAGE			20		V
I_{IHH}	PROGRAM-LEVEL INPUT CURRENT	POLARITY OUTPUT		325		mA
		$\overline{CE1}$/FE		10		
V_{CCH}	POLARITY VERIFY-LEVEL SUPPLY, 'OR' PROGRAM/VERIFY-LEVEL SUPPLY			8.5		V
V_{CC}	'AND' PROGRAM/VERIFY-LEVEL V_{CC} SUPPLY VOLTAGE			5		
V_{CCL}	POLARITY PROGRAM-LEVEL V_{CC} SUPPLY VOLTAGE			0		
I_{CC}	'AND'/'OR' PROGRAM SUPPLY CURRENT		0.5		1	A
V_{IX}	INPUT DISABLE VOLTAGE, $\overline{CE2}$ PROGRAM ENABLE LEVEL, 'OR' PROGRAM-LEVEL INPUT VOLTAGE			10		V
I_{IX}	INPUT CURRENT	INPUT VARIABLES			2	mA
		$\overline{CE2}$			5	
		'OR' PROGRAM OUTPUT			10	
TP	PROGRAM PULSE WIDTH	$\overline{CE2}$		400		US
TD	DELAY TIME		10			US
TR	RISE TIME			25		US
	PROGRAMMING PULSE DUTY CYCLE				50	%

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PROGRAMMING PROCEDURE

(Load all output pins with a 10-kilohm resistor to 5V, set GND (pin 12) to 0V)

PROGRAM OUTPUT POLARITY

Program the output polarity before programming either the AND matrix or the OR matrix. A virgin device has all of its 6 outputs set to active high. When the polarity link of an output is fused, that output function becomes active low. Note that all outputs of a virgin device are at a low logic level. Program one output at a time as follows:

Step 1: Set $\overline{CE}_1$/FE (pin 1) to 0V.
Step 2: Set V_{CC} (pin 24) to 0V, set $\overline{CE}_2$ (pin 13) and I_0 to I_{13} to V_{IH}.
Step 3: Pulse the appropriate output to V_{IHH} and remove after tp.
Step 4: Repeat step 3 for each output to be programmed active low.

VERIFY OUTPUT POLARITY

Step 1: Set $\overline{CE}_1$/FE (pin 1) to 0V; set V_{CC} (pin 24) to V_{CCH}.
Step 2: Enable the device by applying V_{IL} to $\overline{CE}_2$, (pin 13).
Step 3: Set all inputs I_0 thru I_{13} to V_{IH}.
Step 4: Sense the logic state of all 6 outputs. An output at V_{OH} has been programmed active low, while an output at V_{OL} has remained active high.
Step 5: Remove V_{CC}.

PROGRAM 'AND' MATRIX

Program each input separately for each product term, one fuse at a time. Unused terms do not require fusing, however, all input variables of a selected product term must be programmed either true, complement, or don't care (both links are blown), as follows:

Step 1: Set $\overline{CE}_1$/FE (pin 1) to 0V; set V_{CC} (pin 24) to 5V.
Step 2: Disable all outputs by applying V_{IH} to $\overline{CE}_2$ (pin 13).
Step 3: Disable all inputs by applying V_{IX} to inputs I_0 thru I_{13}.
Step 4: Address the product term to be programmed (0 thru 31) by applying its binary code (V_{IH} for '1', V_{IL} for '0') to outputs F_0 thru F_4 with F_0 as the least significant bit.
Step 5: Lower the voltage on the first input to V_{IH} for a true, or to V_{IL} for the complement.
Step 6: After td, raise $\overline{CE}_1$/FE to V_{IHH}.
Step 7: After additional td, pulse the $\overline{CE}_2$ input to V_{IX} for t_p.
Step 8: After a td delay, lower $\overline{CE}_1$/FE to 0V.
Step 9: Disable programmed input by raising it back to V_{IX}.
Step 10: Repeat steps 5-9 for each input.
Step 11: Repeat steps 4-10 for each product term.

VERIFY 'AND' MATRIX

Step 1: Set $\overline{CE}_1$/FE (pin 1) to 0V; set V_{CC} (pin 24) to 5V.
Step 2: Enable F_5 output by setting $\overline{CE}_2$ to V_{IX}.
Step 3: Disable all inputs by applying V_{IX} to inputs I_0 thru I_{13}.
Step 4: Address the product term to be verified (0-31) by applying its corresponding binary code on outputs F_0 thru F_4.
Step 5: Lower the input voltage on the first input to V_{IH} and check the logic level of output F_5, then lower the same input to V_{IL} and again check the level of

PROGRAMMING PROCEDURE (CONT.)

F_5. The input variable state contained in the product term is determined from the following table: (Note that two tests are required to verify the programmed state of each variable).

I	F5	STATE
L	L	TRUE
H	H	
L	H	COMPLEMENT
H	L	
L	H	DON'T CARE
H	H	
L	L	INACTIVE
H	L	

Step 6: Disable verified input by raising it back to V_{IX}.
Step 7: Repeat steps 5-6 for all other inputs.
Step 8: Repeat steps 4-7 for all other product terms.

PROGRAM 'OR' MATRIX

If the product term is contained in the output function, no fusing is needed. Unwanted terms are deleted by programming one at a time, as follows:

Step 1: Set $\overline{CE}_1$/FE (pin 1) to 0V.
Step 2: Disable the outputs by setting $\overline{CE}_2$ (pin 13) to V_{IH}.
Step 3: Wait td and raise V_{CC} (pin 24) to the program level, V_{CCH}.
Step 4: Use the inputs I_0 thru I_5 to address the product term (0-31) that is to be removed by applying the corresponding binary code with input I_0 as the LSB.
Step 5: Raise the output pin to V_{IX}.
Step 6: Wait td, then raise $\overline{CE}_1$/FE to V_{IHH}.
Step 7: Wait td, then pulse $\overline{CE}_2$ to V_{IX} for a period of t_p.
Step 8: Wait td, then lower $\overline{CE}_1$/FE to 0V
Step 9: Wait td, then remove V_{IX} from output pin.
Step 10: Repeat steps 5-9 for all other output functions.
Step 11: Repeat steps 4-10 for all other product terms.
Step 12: Lower V_{CC} to 5V.

VERIFY 'OR' MATRIX

Step 1: Set $\overline{CE}_1$/FE (pin 1) to 0V.
Step 2: Disable the outputs by setting $\overline{CE}_2$ to V_{IH}.
Step 3: Wait td and set V_{CC} (pin 24) to the verify level, V_{CCH}.
Step 4: Address the product term to be verified (0-31) by applying its binary code to inputs I_0 thru I_5.
Step 5: Wait td, and set $\overline{CE}_2$ (pin 13) to V_{IL}.
Step 6: Sense the state of all 6 outputs F_0 thru F_5 to determine the status of the 'OR' matrix from the following table:

OUTPUT		
ACTIVE HIGH	ACTIVE LOW	'OR' FUSE LINK
L	H	FUSED
H	L	PRESENT

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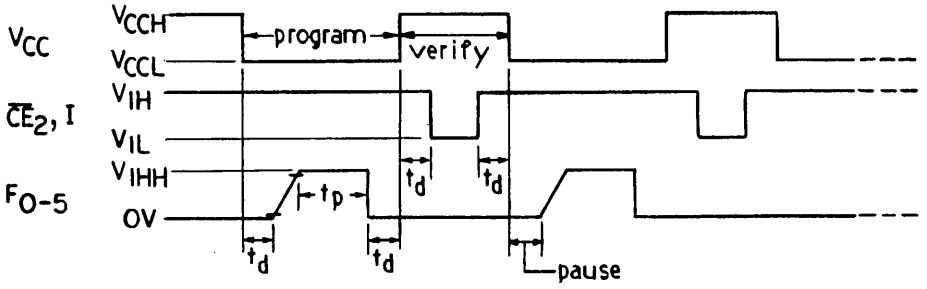
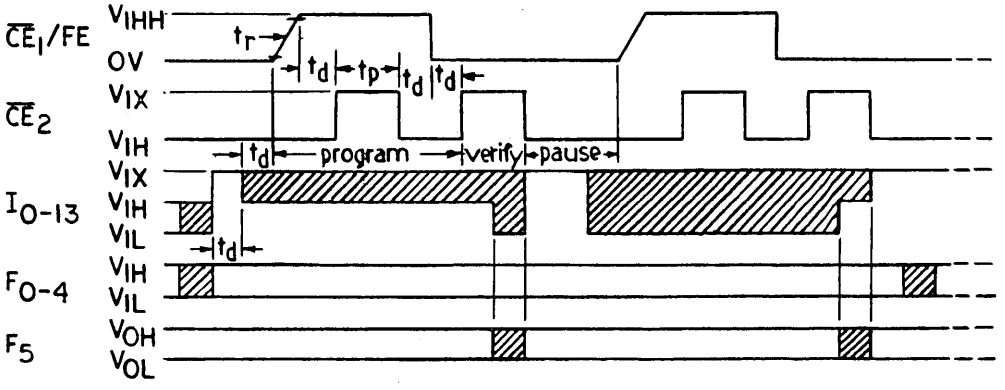
PROGRAMMING WAVEFORMS

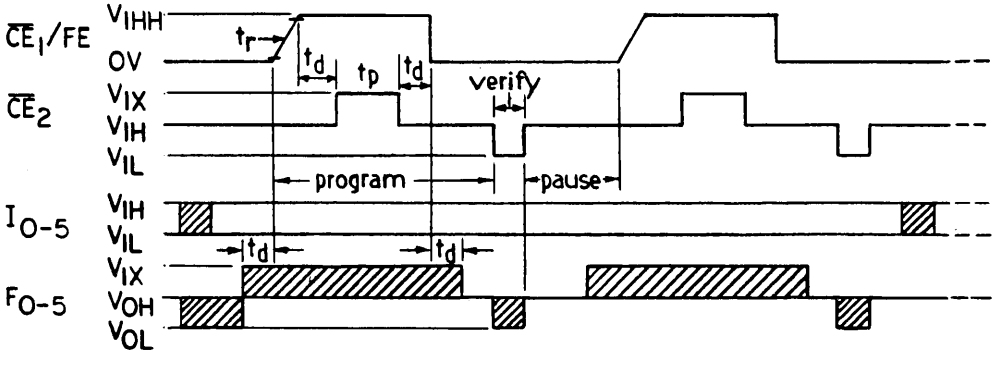
OUTPUT POLARITY



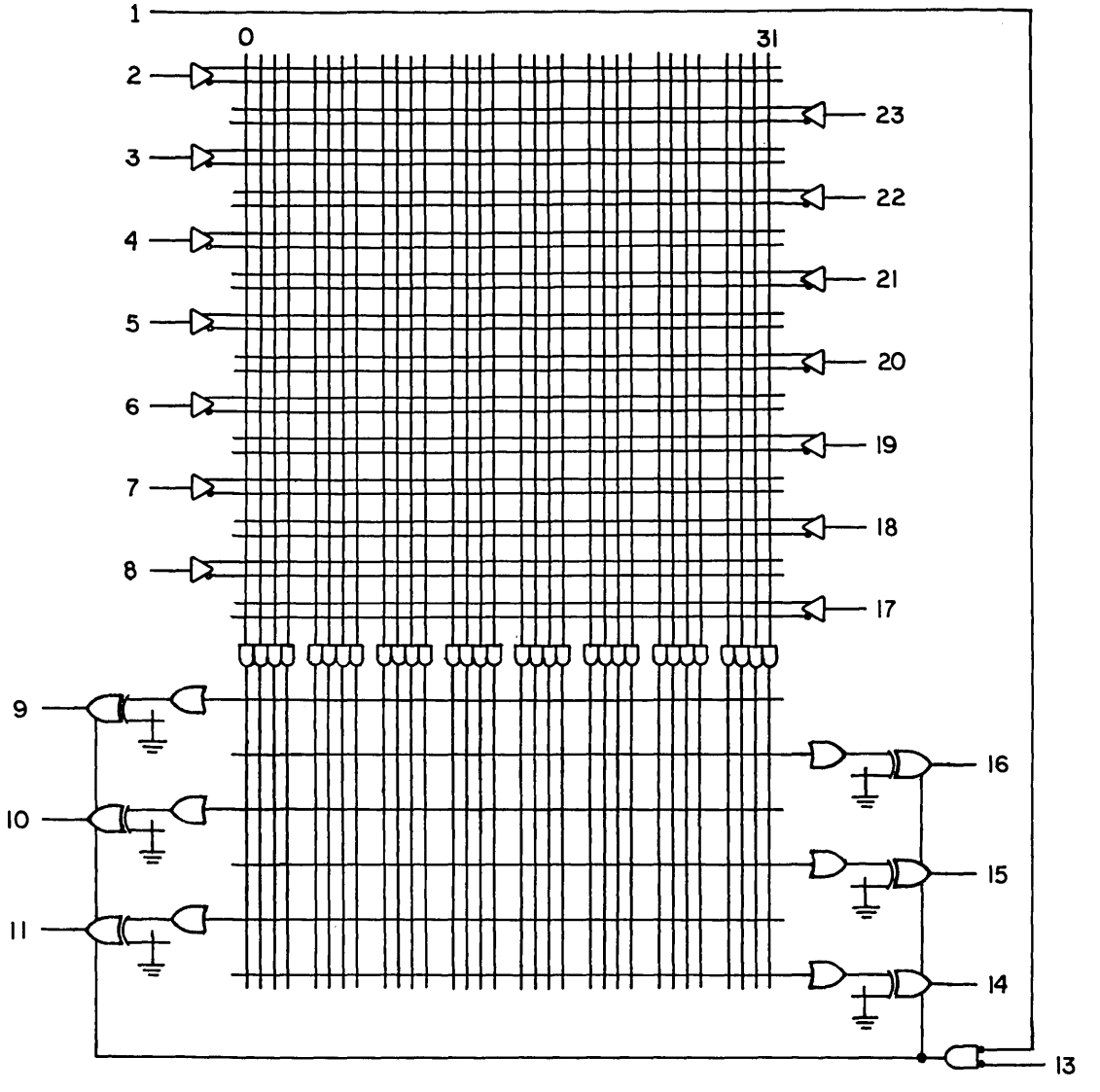
AND MATRIX



OR MATRIX



LOGIC DIAGRAM



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Explanation of New Logic Symbols

EXPLANATION OF NEW LOGIC SYMBOLS

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If you have questions on this Explanation of New Logic Symbols, please contact:

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Telephone (214) 995-3746

IEEE Standards may be purchased from:

Institute of Electrical and Electronics Engineers, Inc.
345 East 47th Street
New York, N.Y. 10017

International Electrotechnical Commission (IEC) publications may be purchased from:

American National Standards Institute, Inc.
1430 Broadway
New York, N.Y. 10018

by F. A. Mann

1 INTRODUCTION

The International Electrotechnical Commission (IEC) has been developing a very powerful symbolic language that can show the relationship of each input of a digital logic circuit to each output without showing explicitly the internal logic. At the heart of the system is dependency notation, which will be explained in Section 4.

The system was introduced in the USA in a rudimentary form in IEEE/ANSI Standard Y32.14-1973. Lacking at that time a complete development of dependency notation, it offered little more than a substitution of rectangular shapes for the familiar distinctive shapes for representing the basic functions of AND, OR, negation, etc. This is no longer the case.

Internationally, Working Group 2 of IEC Technical Committee TC-3 is preparing a new document (Publication 617-12) that will consolidate the original work started in the mid 1960's and published in 1972 (Publication 117-15) and the amendments and supplements that have followed. Similarly for the USA, IEEE Committee SCC 11.9 is revising the publication IEEE Std 91/ANSI Y32.14. Texas Instruments is participating in the work of both organizations and this Supplement to the TTL Data Book introduces new logic symbols in anticipation of the new standards. When changes are made as the standards develop, future editions of the TTL Data Book will take those changes into account.

The following explanation of the new symbolic language is necessarily brief and greatly condensed from what the standards publications will finally contain. This is not intended to be sufficient for those people who will be developing symbols for new devices. It is primarily intended to make possible the understanding of the symbols used in this book; comparing the symbols with functional block diagrams and/or function tables will further help that understanding.

2 SYMBOL COMPOSITION

A symbol comprises an outline or a combination of outlines together with one or more qualifying symbols. The shape of the symbols is not significant. As shown in Figure 1, general qualifying symbols are used to tell exactly what logical operation is performed by the elements. Table I shows the general qualifying symbols used in this data book. Input lines are placed on the left and output lines are placed on the right. When an exception is made to that convention, the direction of signal flow is indicated by an arrow as shown in Figure 11.

All outputs of a single, unsubdivided element always have identical internal logic states determined by the function of the element except when otherwise indicated by an associated qualifying symbol or label inside the element.

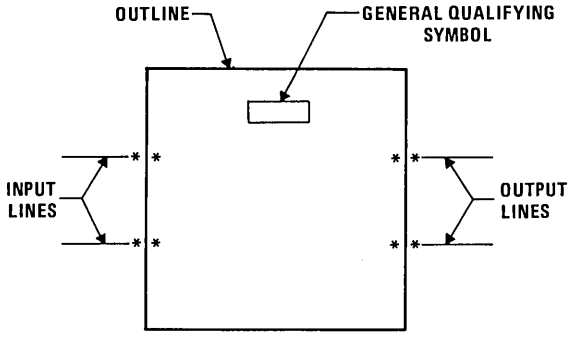

FIGURE 1 – SYMBOL COMPOSITION

The outlines of elements may be abutted or embedded in which case the following conventions apply. There is no logic connection between the elements when the line common to their outlines is in the direction of signal flow. There is at least one logic connection between the elements when the line common to their outlines is perpendicular to the direction of signal flow. The number of logic connections between elements will be clarified by the use of qualifying symbols and this is discussed further under that topic. If no indications are shown on either side of the common line, it is assumed there is only one connection.

When a circuit has one or more inputs that are common to more than one element of the circuit, the common-control block may be used. This is the only distinctively shaped outline used in the IEC system. Figure 2 shows that unless otherwise qualified by dependency notation, an input to the common-control block is an input to each of the elements below the common-control block.

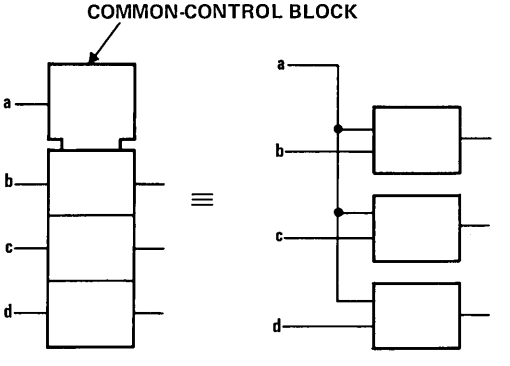

FIGURE 2 – ILLUSTRATION OF COMMON- CONTROL BLOCK

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A common output depending on all elements of the array can be shown as the output of a common-output element. Its distinctive visual feature is the double line at its top. In addition the common-output element may have other inputs as shown in Figure 3. The function of the common-output element must be shown by use of a general qualifying symbol.

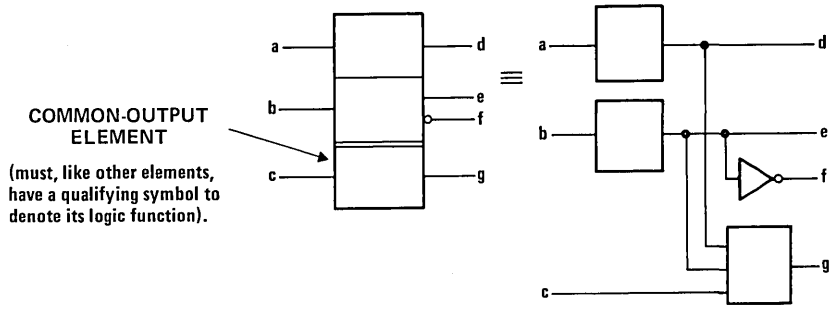

FIGURE 3 – ILLUSTRATION OF COMMON-OUTPUT ELEMENT

3 QUALIFYING SYMBOLS

3.1 General Qualifying Symbols

Table I shows the general qualifying symbols used in this data book. These characters are placed near the top center or the geometric center of a symbol or symbol element to define the basic function of the device represented by the symbol or of the element.

3.2 Qualifying Symbols for Inputs and Outputs

Qualifying symbols for inputs and outputs are shown in Table II and will be familiar to most users with the possible exception of the logic polarity and analog signal indicators. The older logic negation indicator means that the external 0 state produces the internal 1 state. The internal 1 state means the active state. Logic negation may be used in pure logic diagrams; in order to tie the external 1 and 0 logic states to the levels H (high) and L (low), a statement of whether positive logic (1 = H, 0 = L) or negative logic (1 = L, 0 = H) is being used is required or must be assumed. Logic polarity indicators eliminate the need for calling out the logic convention and are used in this data book in the symbology for actual devices. The presence of the triangular polarity indicator indicates that the L logic level will produce the internal 1 state (the active state) or that, in the case of an output, the internal 1 state will produce the external L level. Note how the active direction of transition for a dynamic input is indicated in positive logic, negative logic, and with polarity indication.

EXPLANATION OF NEW LOGIC SYMBOLS

TABLE I – GENERAL QUALIFYING SYMBOLS

SYMBOL	DESCRIPTION	EXAMPLE
&	AND gate or function.	SN7400
≥1	OR gate or function. The symbol was chosen to indicate that at least one active input is needed to activate the output.	SN7402
=1	Exclusive OR. One and only one input must be active to activate the output.	SN7486
=	Logic identity. All inputs must stand at same state.	SN74180
2k	An even number of inputs must be active.	SN74180
2k+1	An odd number of inputs must be active.	*
1	The one input must be active.	SN7404
▷ or ◁	A buffer or element with more-than usual output capability (symbol is oriented in the direction of signal flow).	SN74S436
⎍	Schmitt trigger; element with hysteresis.	SN74LS18
X/Y	Coder, code converter (DEC/BCD, BIN/OUT, BIN/7-SEG, etc.).	SN74LS347
MUX	Multiplexer/data selector.	SN74150
DMUX or DX	Demultiplexer.	SN74138
Σ	Adder.	SN74LS385
P–Q	Subtracter.	SN74LS385
CPG	Look-ahead carry generator.	SN74182
π	Multiplier.	SN74LS384
COMP	Magnitude comparator.	SN74LS682
ALU	Arithmetic logic unit.	SN74LS381
⎍	Retriggerable monostable.	SN74LS422
1⎍	Non-retriggerable monostable (one-shot).	SN74121
G	Astable element. Showing waveform is optional.	SN74LS320
!G	Synchronously starting astable.	SN74LS624
G!	Astable element that stops with a completed pulse.	
SRGm	Shift register. m = number of bits.	SN74LS595
CTRm	Counter. m = number of bits; cycle length = 2^m.	SN54LS590
CTR DIVm	Counter with cycle length = m.	SN74LS668
ROM	Read-only memory.	*
RAM	Random-access read/write memory.	SN74170
FIFO	First-in, first-out memory.	SN74LS222

*Not all of the general qualifying symbols have been used in this book, but they are included here for the sake of completeness.

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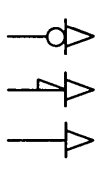
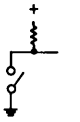
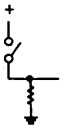
TABLE II – QUALIFYING SYMBOLS FOR INPUTS AND OUTPUTS

	Logic negation at input. External 0 produces internal 1.
	Logic negation at output. Internal 1 produces external 0.
	Active-low input. Equivalent to in positive logic.
	Active-low output. Equivalent to in positive logic.
	Active-low input in the case of right-to-left signal flow.
	Active-low output in the case of right-to-left signal flow.
	Signal flow from right to left. If not otherwise indicated, signal flow is from left to right.
	Bidirectional signal flow.
	Dynamic inputs active on indicated transition POSITIVE LOGIC: 1→0 (not used); 0→1 NEGATIVE LOGIC: 0→1 (not used); 1→0 POLARITY INDICATION: not used; H→L (not used); L→H
	Nonlogic connection. A label inside the symbol will usually define the nature of this pin.
	Input for analog signals.
	Internal connection. 1 state on left produces 1 state on right.
	Negated internal connection. 1 state on left produces 0 state on right.
	Dynamic internal connection. Transition from 0 to 1 on left produces transitory 1 state on right.
	Internal input (virtual input). It always stands at its internal 1 state unless affected by an overriding dependency relationship.
	Internal output (virtual output). Its effect on an internal input to which it is connected is indicated by dependency notation.

The internal connections between logic elements abutted together in a symbol may be indicated by the symbols shown. Each logic connection may be shown by the presence of qualifying symbols at one or both sides of the common line and if confusion can arise about the numbers of connections, use can be made of one of the internal connection symbols.

The internal (virtual) input is an input originating somewhere else in the circuit and is not connected directly to a terminal. The internal (virtual) output is likewise not connected directly to a terminal.

TABLE III – SYMBOLS INSIDE THE OUTLINE

¬	Postponed output (of a pulse-triggered flip-flop). The output changes when input initiating change (e.g., a C input) returns to its initial external state or level. See § 5.
⊓	Bi-threshold input (input with hysteresis)
◇	NPN open-collector or similar output that can supply a relatively low-impedance L level when not turned off. Requires external pull-up. Capable of positive-logic wired-AND connection. 
◈	Passive-pull-up output is similar to NPN open-collector output but is suplemented with a built-in passive pull-up.
◇	NPN open-emitter or similar output that can supply a relatively low-impedance H level when not turned off. Requires external pull-down. Capable of positive-logic wired-OR connection. 
◈	Passive-pull-down output is similar to NPN open-emitter output but is supplemented with a built-in passive pull-down.
▽	3-state output
EN	Enable input When at its internal 1-state, all outputs are enabled. When at its internal 0-state, open-collector and open-emitter outputs are off, three-state outputs are at normally defined internal logic states and at external high-impedance state, and all other outputs (e.g., totem-poles) are at the internal 0-state.
J, K, R, S, T	Usual meanings associated with flip-flops (e.g., R = reset, T = toggle)
D	Data input to a storage element equivalent to: 
→m ←m	Shift right (left) inputs, m = 1, 2, 3 etc. If m = 1, it is usually not shown.
+m −m	Counting up (down) inputs, m = 1, 2, 3 etc. If m = 1, it is usually not shown.
0 m	Binary grouping. m is highest power of 2.
CT = 15	The contents-setting input, when active, causes the content of a register to take on the indicated value.
CT = 9	The content output is active if the content of the register is as indicated.
	Input line grouping . . . . indicates two or more terminals used to implement a single logic input. e.g., The paired expander inputs of SN7450. 
"1"	Fixed-state output always stands at its internal 1 state. For example, see SN74185.

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The application of internal inputs and outputs requires an understanding of dependency notation, which is explained in Section 4.

In an array of elements, if the same general qualifying symbol and the same qualifying symbols associated with inputs and outputs would appear inside each of the elements of the array, these qualifying symbols are usually shown only in the first element. This is done to reduce clutter and to save time in recognition. Similarly, large identical elements that are subdivided into smaller elements may each be represented by an unsubdivided outline. The SN54LS440 symbol illustrates this principle.

3.3 Symbols Inside the Outline

Table III shows some symbols used inside the outline. Note particularly that open-collector, open-emitter, and three-state outputs have distinctive symbols. Also note that an EN input affects all of the outputs of the circuit and has no effect on inputs. When an enable input affects only certain outputs and/or affects one or more inputs, a form of dependency notation will indicate this (see 4.9). The effects of the EN input on the various types of outputs are shown.

It is particularly important to note that a D input is always the data input of a storage element. At its internal 1 state, the D input sets the storage element to its 1 state, and at its internal 0 state it resets the storage element to its 0 state.

The binary grouping symbol will be explained more fully in Section 8. Binary-weighted inputs are arranged in order and the binary weights of the least-significant and the most-significant lines are indicated by numbers. In this data book weights of input and output lines will be represented by powers of two usually only when the binary grouping symbol is used, otherwise, decimal numbers will be used. The grouped inputs generate an internal number on which a mathematical function can be performed or that can be an identifying number for dependency notation. See Figure 28. A frequent use is in addresses for memories.

Reversed in direction, the binary grouping symbol can be used with outputs. The concept is analogous to that for the inputs and the weighted outputs will indicate the internal number assumed to be developed within the circuit.

Other symbols are used inside the outlines in this data book in accordance with the IEC/IEEE standards but are not shown here. Generally these are associated with arithmetic operations and are self-explanatory.

When nonstandardized information is shown inside an outline, it is usually enclosed in square brackets [like these].

4 DEPENDENCY NOTATION

4.1 General Explanation

Dependency notation is the powerful tool that sets the IEC symbols apart from previous systems and makes compact, meaningful, symbols possible. It provides the means of denoting the relationship between inputs, outputs, or inputs and outputs without actually showing all the elements and interconnections involved. The information provided by dependency notation supplements that provided by the qualifying symbols for an element's function.

In the convention for the dependency notation, use will be made of the terms "affecting" and "affected". In cases where it is not evident which inputs must be considered as being the affecting or the affected ones (e.g., if they stand in an AND relationship), the choice may be made in any convenient way.

So far, ten types of dependency have been defined and all of these are used in this data book. They are listed below in the order in which they are presented and are summarized in Table IV following 4.11.

Section	Dependency Type or Other Subject
4.2	G, AND
4.3	General rules for dependency notation
4.4	V, OR
4.5	N, Negate, (Exclusive OR)
4.6	Z, Interconnection
4.7	C, Control
4.8	S, Set and R, Reset
4.9	EN, Enable
4.10	M, Mode
4.11	A, Address

4.2 G (AND) Dependency

A common relationship between two signals is to have them ANDed together. This has traditionally been shown by explicitly drawing an AND gate with the signals connected to the inputs of the gate. The 1972 IEC publication and the 1973 IEEE/ANSI standard showed several ways to show this AND relationship using dependency notation. While nine other forms of dependency have since been defined, the ways to invoke AND dependency are now reduced to one.

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In Figure 4 input **b** is ANDed with input **a** and the complement of **b** is ANDed with **c**. The letter G has been chosen to indicate AND relationships and is placed at input **b**, inside the symbol. A number considered appropriate by the symbol designer (1 has been used here) is placed after the letter G and also at each affected input. Note the bar over the 1 at input **c**.

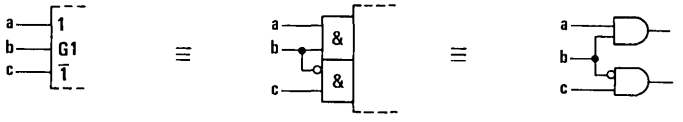

FIGURE 4 – G DEPENDENCY BETWEEN INPUTS

In Figure 5, output **b** affects input **a** with an AND relationship. The lower example shows that it is the internal logic state of **b**, unaffected by the negation sign, that is ANDed. Figure 6 shows input **a** to be ANDed with a dynamic input **b**.

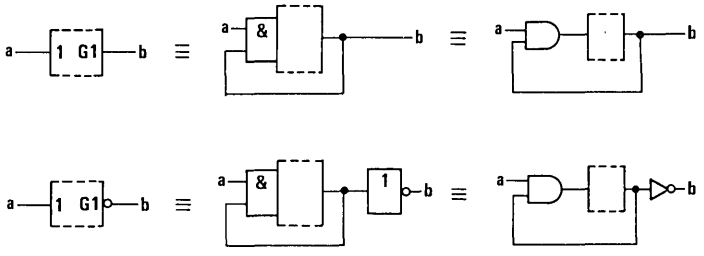

FIGURE 5 – G DEPENDENCY BETWEEN OUTPUTS AND INPUTS

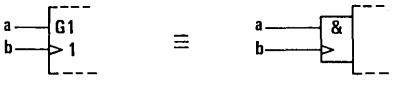

FIGURE 6 – G DEPENDENCY WITH A DYNAMIC INPUT

The rules for G dependency can be summarized thus:

When a G*m* input or output (*m* is a number) stands at its internal 1 state, all inputs and outputs affected by G*m* stand at their normally defined internal logic states. When the G*m* input or output stands at its 0 state, all inputs and outputs affected by G*m* stand at their internal 0 states.

4.3 Conventions for the Application of Dependency Notation in General

The rules for applying dependency relationships in general follow the same pattern as was illustrated for G dependency.

Application of dependency notation is accomplished by:

1) labeling the input (or output) *affecting* other inputs or outputs with the letter symbol indicating the relationship involved (e.g., G for AND) followed by an identifying number, appropriately chosen, and
2) labeling each input or output *affected* by that affecting input (or output) with that same number.

If it is the complement of the internal logic state of the affecting input or output that does the affecting, then a bar is placed over the identifying numbers at the affected inputs or outputs. See Figure 4.

If two affecting inputs or outputs have the same letter and same identifying number, they stand in an OR relationship to each other. See Figure 7.

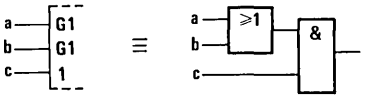

FIGURE 7 – OR'ED AFFECTING INPUTS

If the affected input or output requires a label to denote its function (e.g., "D"), this label will be *prefixed* by the identifying number of the affecting input. See Figure 12.

If an input or output is affected by more than one affecting input, the identifying numbers of each of the affecting inputs will appear in the label of the affected one, separated by commas. The normal reading order of these numbers is the same as the sequence of the affecting relationships. See Figure 12.

If the labels denoting the functions of affected inputs or outputs must be numbers, (e.g., outputs of a coder), the identifying numbers to be associated with both affecting inputs and affected inputs or outputs will be replaced by another character selected to avoid ambiguity, e.g., Greek letters. See Figure 8.

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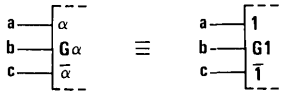


FIGURE 8 – SUBSTITUTION FOR NUMBERS

4.4 V (OR) Dependency

The symbol denoting OR dependency is the letter V. See Figure 9.

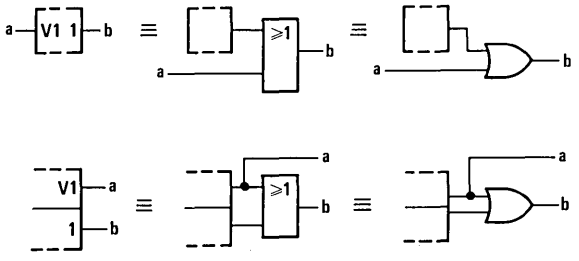
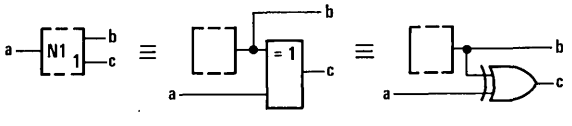


FIGURE 9 – V (OR) DEPENDENCY

When a V*m* input or output stands at its internal 1 state, all inputs and outputs affected by V*m* stand at their internal 1 states. When the V*m* input or output stands at its internal 0 state, all inputs and outputs affected by V*m* stand at their normally defined internal logic states.

4.5 N (Negate) (X-OR) Dependency

The symbol denoting negate dependency is the letter N. See Figure 10. Each input or output affected by an N*m* input or output stands in an exclusive-OR relationship with the N*m* input or output.



If a = 0, then c = b
If a = 1, then c = $\bar{b}$

FIGURE 10 – N (NEGATE) (X-OR) DEPENDENCY

When an N*m* input or output stands at its internal 1 state, the internal logic state of each input and each output affected by N*m* is the complement of what it would otherwise be. When an N*m* input or output stands at its internal 0 state, all inputs and outputs affected by N*m* stand at their normally defined internal logic states.

4.6 Z (Interconnection) Dependency

The symbol denoting interconnection dependency is the letter Z.

Interconnection dependency is used to indicate the existence of internal logic connections between inputs, outputs, internal inputs, and/or internal outputs.

The internal logic state of an input or output affected by a Z*m* input or output will be the same as the internal logic state of the Z*m* input or output, unless modified by additional dependency notation. See Figure 11.

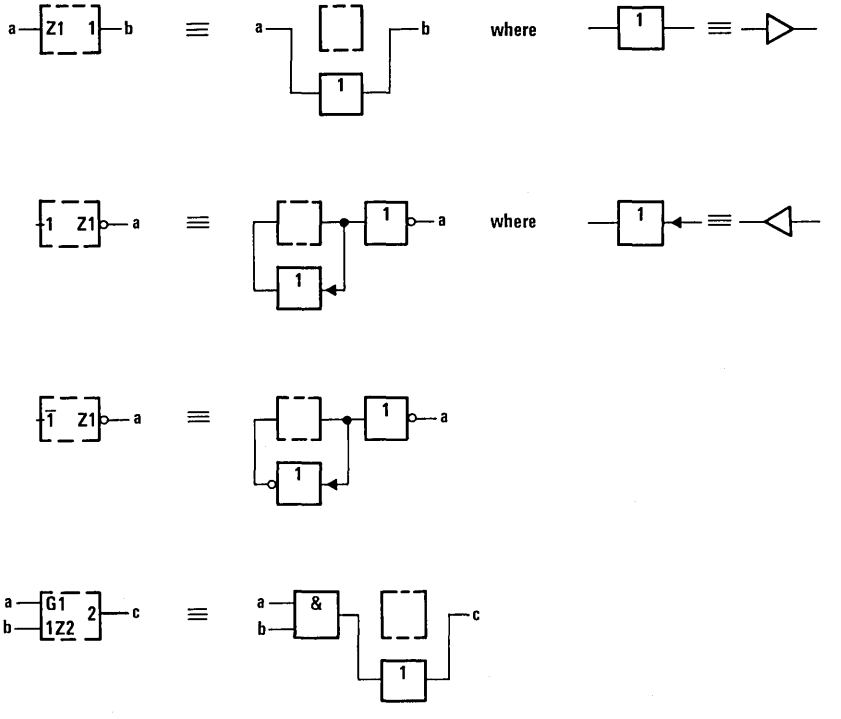


FIGURE 11 – Z (INTERCONNECTION) DEPENDENCY

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4.7 C (Control) Dependency

The symbol denoting control dependency is the letter C.

Control inputs are usually used to enable or disable the data (D, J, K, R, or S) inputs of storage elements. They may take on their internal 1 states (be active) either statically or dynamically. In the latter case the dynamic input symbol is used as shown in the third example of Figure 12.

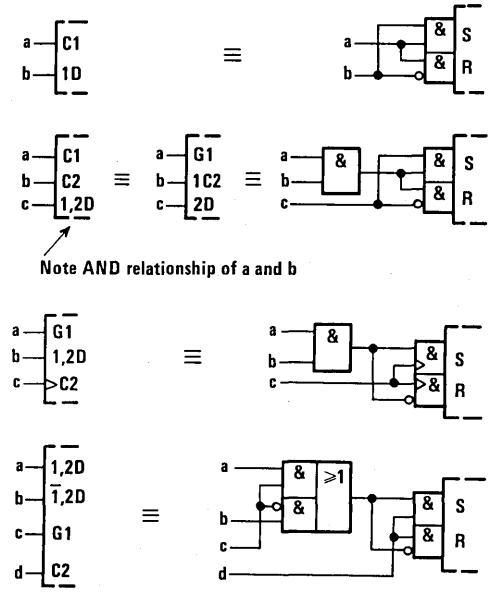


FIGURE 12 – C (CONTROL) DEPENDENCY

When a C*m* input or output stands at its internal 1 state, the inputs affected by C*m* have their normally defined effect on the function of the element, i.e., these inputs are enabled. When a C*m* input or output stands at its internal 0 state, the inputs affected by C*m* are disabled and have no effect on the function of the element.

4.8 S (Set) and R (Reset) Dependencies

The symbol denoting set dependency is the letter S. The symbol denoting reset dependency is the letter R.

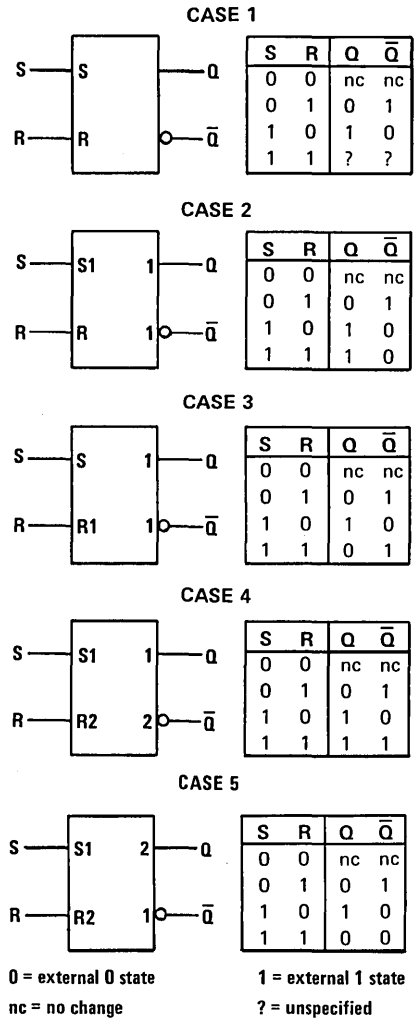
Set and reset dependenies are used if it is necessary to specify the effect of the combination R=S=1 on a bistable element. Case 1 in Figure 13 does not use S or R dependency.

When an S*m* input is at its internal 1 state, outputs affected by the Sm input will react, regardless of the state of an R input, as they normally would react to the combination S=1, R=0. See cases 2, 4, and 5 in Figure 13.

When an R*m* input is at its internal 1 state, outputs affected by the Rm input will react, regardless of the state of an S input, as they normally would react to the combination S=0, R=1. See cases 3, 4, and 5 in Figure 13.

When an S*m* or R*m* input is at its internal 0 state, it has no effect.

Note that the noncomplementary output patterns in cases 4 and 5 are only pseudo stable. The simultaneous return of the inputs to S=R=0 produces an unforeseeable stable and complementary output pattern.



S	R	Q	$\overline{Q}$
0	0	nc	nc
0	1	0	1
1	0	1	0
1	1	?	?

S	R	Q	$\overline{Q}$
0	0	nc	nc
0	1	0	1
1	0	1	0
1	1	1	0

S	R	Q	$\overline{Q}$
0	0	nc	nc
0	1	0	1
1	0	1	0
1	1	0	1

S	R	Q	$\overline{Q}$
0	0	nc	nc
0	1	0	1
1	0	1	0
1	1	1	1

S	R	Q	$\overline{Q}$
0	0	nc	nc
0	1	0	1
1	0	1	0
1	1	0	0

0 = external 0 state **1 = external 1 state**
nc = no change **? = unspecified**

FIGURE 13 – S (SET AND R (RESET) DEPENDENCIES

4.9 EN (Enable) Dependency

The symbol denoting enable dependency is the combination of letters EN.

An EN*m* input has the same effect on outputs as an EN input, see 3.1, but it effects only those outputs labeled with the identifying number *m*. It also affects those inputs labeled with the identifying number *m*. By contrast, an EN input affects all outputs and no inputs. The effect of an EN*m* input on an affected input is identical to that of a C*m* input. See Figure 14.

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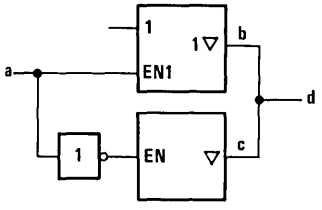
When an EN*m* input stands at its internal 1 state, the inputs affected by EN*m* have their normally defined effect on the function of the element and the outputs affected by this input stand at their normally defined internal logic states, i.e., these inputs and outputs are enabled.



If a = 0, b is disabled and d = c
If a = 1, c is disabled and d = b

FIGURE 14 – EN (ENABLE) DEPENDENCY

When an EN*m* input stands at its internal 0 state, the inputs affected by EN*m* are disabled and have no effect on the function of the element, and the outputs affected by EN*m* are also disabled. Open-collector outputs are turned off, three-state outputs stand at their normally defined internal logic states but externally exhibit high impedance, and all other outputs (e.g., totem-pole outputs) stand at their internal 0 states.

4.10 M (Mode) Dependency

The symbol denoting mode dependency is the letter M.

Mode dependency is used to indicate that the effects of particular inputs and outputs of an element depend on the mode in which the element is operating.

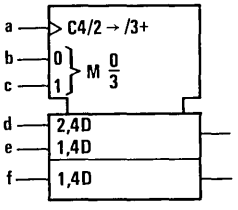
If an input or output has the same effect in different modes of operation, the identifying numbers of the relevant affecting M*m* inputs will appear in the label of that affected input or output between parentheses and separated by solidi. See Figure 19.

4.10.1 M Dependency Affecting Inputs

M dependency affects inputs the same as C dependency. When an M*m* input or M*m* output stands at its internal 1 state, the inputs affected by this M*m* input or M*m* output have their normally defined effect on the function of the element, i.e., the inputs are enabled.

When an M*m* input or M*m* output stands at its internal 0 state, the inputs affected by this M*m* input or M*m* output have no effect on the function of the element. When an affected input has several sets of labels separated by solidi (e.g., C4/2→/3+), any set in which the identifying number of the M*m* input or M*m* output appears has no effect and is to be ignored. This represents disabling of some of the functions of a multifunction input.

The circuit in Figure 15 has two inputs, **b** and **c**, that control which one of four modes (0, 1, 2, or 3) will exist at any time. Inputs **d**, **e**, and **f** are D inputs subject to dynamic control (clocking) by the **a** input. The numbers 1 and 2 are in the series chosen to indicate the modes so inputs **e** and **f** are only enabled in mode 1 (for parallel loading) and input **d** is only enabled in mode 2 (for serial loading). Note that input **a** has three functions. It is the clock for entering data. In mode 2, it causes right shifting of data, which means a shift away from the control block. In mode 3, it causes the contents of the register to be incremented by one count.



Note that all operations are synchronous.

In MODE 0 (b = 0, c = 0), the outputs remain at their existing states as none of the inputs has an effect.

In MODE 1 (b = 1, c = 0), parallel loading takes place thru inputs e and f.

In MODE 2 (b = 0, c = 1), shifting down and serial loading thru input d take place.

In MODE 3 (b = c = 1), counting up by increment of 1 per clock pulse takes place.

FIGURE 15 – M (MODE) DEPENDENCY AFFECTING INPUTS

4.10.2 M Dependency Affecting Outputs

When an M*m* input or M*m* output stands at its internal 1 state, the affected outputs stand at their normally defined internal logic states, i.e., the outputs are enabled.

When an M*m* input or M*m* output stands at its internal 0 state, at each affected output any set of labels containing the identifying number of that M*m* input or M*m* output has no effect and is to be ignored. When an output has several different sets of labels separated by solidi (e.g., 2,4/3,5), only those sets in which the identifying number of this M*m* input or M*m* output appears are to be ignored.

In Figure 16, mode 1 exists when the **a** input stands at its internal 1 state. The delayed output symbol is effective only in mode 1 (when input **a** = 1) in which case the device functions as a pulse-triggered flip-flop. See Section 5. When input **a** = 0, the device is not in mode 1 so the delayed output symbol has no effect and the device functions as a transparent latch.

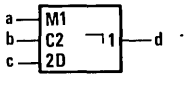


FIGURE 16 – TYPE OF FLIP-FLOP DETERMINED BY MODE

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In Figure 17, if input a stands at its internal 1 state establishing mode 1, output **b** will stand at its internal 1 state only when the content of the register equals 9. Since output **b** is located in the common-control block with no defined function outside of mode 1, this output will stand at its internal 0 state when input **a** stands at its internal 0 state, regardless of the register content.

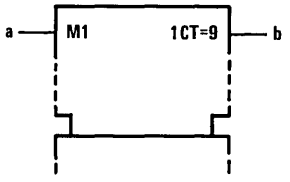

FIGURE 17 – DISABLING AN OUTPUT OF THE COMMON-CONTROL BLOCK

In Figure 18, if input **a** stands at its internal 1 state establishing mode 1, output **b** will stand at its internal 1 state only when the content of the register equals 15. If input **a** stands at its internal 0 state, output **b** will stand at its internal 1 state only when the content of the register equals 0.

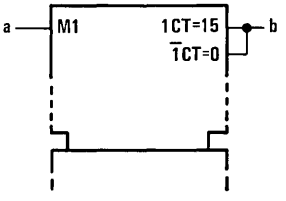

FIGURE 18 – DETERMINING AN OUTPUT'S FUNCTION

In Figure 19 inputs **a** and **b** are binary weighted to generate the numbers 0, 1, 2, or 3. This determines which one of the four modes exists.

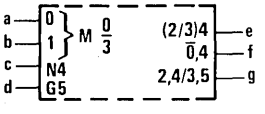

FIGURE 19 – DEPENDENT RELATIONSHIPS AFFECTED BY MODE

At output **e** the label set causing negation (if **c** = 1) is effective only in modes 2 and 3. In modes 0 and 1 this output stands at its normally defined state as if it had no labels. At output **f** the label set has effect when the mode is not 0 so output **e** is negated (if **c** = 1) in modes 1, 2, and 3. In mode 0 the label set has no effect so the output stands at its normally defined state. In this example 0,4 is equivalent to (1/2/3)4. At output **g** there are two label sets. The first set, causing negation (if **c** = 1), is effective only in mode 2. The second set, subjecting **g** to AND dependency on **d**, has effect only in mode 3.

Note that in mode 0 none of the dependency relationships has any effect on the outputs, so **e**, **f**, and **g** will all stand at the same state.

4.11 A (Address) Dependency

The symbol denoting address dependency is the letter A.

Address dependency provides a clear representation of those elements, particularly memories, that use address control inputs to select specified sections of a multidimensional array. Such a section of a memory array is usually called a word. The purpose of address dependency is to allow a symbolic presentation of the entire array. An input of the array shown at a particular element of this general section is common to the corresponding elements of all selected sections of the array. An output of the array shown at a particular element of this general section is the result of the OR function of the outputs of the corresponding elements of selected sections. If the label of an output of the array shown at a particular element of this general section indicates that this output is an open-circuit output or a three-state output, then this indication refers to the output of the array and not to those of the sections of the array.

Inputs that are not affected by any affecting address input have their normally defined effect on all sections of the array, whereas inputs affected by an address input have their normally defined effect only on the section selected by that address input.

An affecting address input is labelled with the letter A followed by an identifying number that corresponds with the address of the particular section of the array selected by this input. Within the general section presented by the symbol, inputs and outputs affected by an A*m* input are labelled with the letter A, which stands for the identifying numbers, i.e., the addresses, of the particular sections.

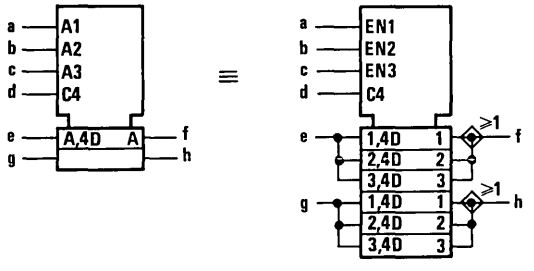

FIGURE 20 – A (ADDRESS) DEPENDENCY

Figure 20 shows a 3-word by 2-bit memory having a separate address line for each word and uses EN dependency to explain the operation. To select word 1, input a is taken to its 1 state, which establishes mode 1. Data can now be clocked into the inputs marked "1,4D". Unless words 2 and 3 are also selected, data cannot be clocked in at the inputs marked "2,4D" and "3,4D". The outputs will be the OR functions of the selected outputs, i.e., only those enabled by the active EN functions.

The identifying numbers of affecting address inputs correspond with the addresses of the sections selected by these inputs. They need not necessarily differ from those of other affecting dependency-inputs (e.g., G, V, N, . . .), because in the general section presented by the symbol they are replaced by the letter A.

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If there are several sets of affecting *Am* inputs for the purpose of independent and possibly simultaneous access to sections of the array, then the letter A is modified to 1A, 2A, . . . Because they have access to the same sections of the array, these sets of A inputs may have the same identifying numbers.

Figure 21 is another illustration of the concept.

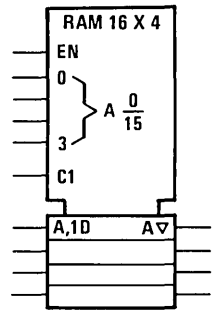

FIGURE 21

FIGURE 21 – ARRAY OF 16 SECTIONS OF FOUR TRANSPARENT LATCHES WITH 3-STATE OUTPUTS COMPRISING A 16-WORD X 4-BIT RANDOM-ACCESS MEMORY

TABLE IV – SUMMARY OF DEPENDENCY NOTATION

TYPE OF DEPENDENCY	LETTER SYMBOL*	AFFECTING INPUT AT ITS 1-STATE	AFFECTING INPUT AT ITS 0-STATE
Address	A	Permits action (address selected)	Prevents action (address not selected)
Control	C	Permits action	Prevents action
Enable	EN	Permits action	Prevents action of inputs. ◇outputs off. ▽outputs at external high impedance, no change in internal logic state. Other outputs at internal 0 state.
AND	G	Permits action	Imposes 0 state
Mode	M	Permits action (mode selected)	Prevents action (mode not selected)
Negate (X-OR)	N	Complements state	No effect
RESET	R	Affected output reacts as it would to S = 0, R = 1	No effect
SET	S	Affected output reacts as it would to S = 1, R = 0	No effect
OR	V	Imposes 1 state	Permits action
Interconnection	Z	Imposes 1 state	Imposes 0 state

*These letter symbols appear at the AFFECTING input (or output) and are followed by a number. Each input (or output) AFFECTED by that input is labeled with that same number. When the labels EN, R, and S appear at inputs without the following numbers, the descriptions above do not apply. The action of these inputs is described under "Symbols Inside The Outline", see 3.1.

5 BISTABLE ELEMENTS

The dynamic input symbol, the postponed output symbol, and dependency notation provide the tools to differentiate four main types of bistable elements and make synchronous and asynchronous inputs easily recognizable. See Figure 22. The first column shows the essential distinguishing features; the other columns show examples.

Transparent latches have a level-operated control input. The D input is active as long as the C input is at its internal 1 state. The outputs respond immediately. Edge-triggered elements accept data from D, J, K, R, or S inputs on the active transition of C. Pulse-triggered elements require the setup of data before the start of the control pulse; the C input is considered static since the data must be maintained as long as C is at its 1 state. The output is postponed until C returns to its 0 state. The data-lock-out element is similar to the pulse-triggered version except that the C input is considered dynamic in that shortly after C goes through its active transition, the data inputs are disabled and data does not have to be held. However, the output is still postponed until the C input returns to its initial external level.

Notice that synchronous inputs can be readily recognized by their dependency labels (1D, 1J, 1K, 1S, 1R) compared to the asynchronous inputs (S, R), which are not dependent on the C inputs.

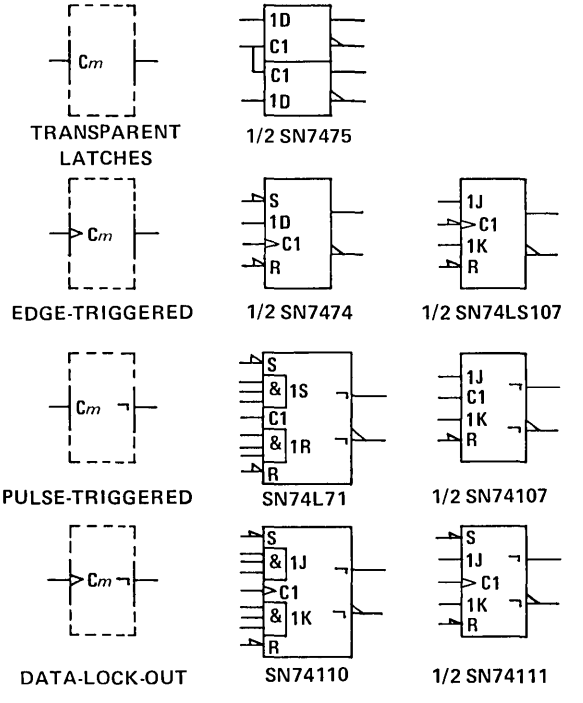

FIGURE 22 – FOUR TYPES OF BISTABLE CIRCUITS

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6 CODERS

The general symbol for a coder or code converter is shown in Figure 23. X and Y may be replaced by appropriate indications of the code used to represent the information at the inputs and at the outputs, respectively.

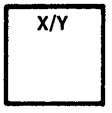


FIGURE 23 – CODER GENERAL SYMBOL

Indication of code conversion is based on the following rule:

> Depending on the input code, the internal logic states of the inputs determine an internal value. This value is reproduced by the internal logic states of the outputs, depending on the output code.

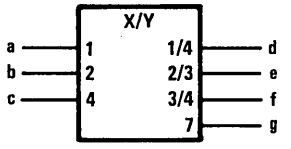
The indication of the relationships between the internal logic states of the inputs and the internal value is accomplished by:

1) labelling the inputs with numbers. In this case the internal value equals the sum of the weights associated with those inputs that stand at their internal 1-state, or by
2) replacing X by an appropriate indication of the input code and labelling the inputs with characters that refer to this code.

The relationships between the internal value and the internal logic states of the outputs are indicated by:

1) labelling each output with a list of numbers representing those internal values that lead to the internal 1-state of that output. These numbers shall be separated by solidi as in Figure 24. This labelling may also be applied when Y is replaced by a letter denoting a type of dependency (see Section 7). If a continuous range of internal values produces the internal 1 state of an output, this can be indicated by two numbers that are inclusively the beginning and the end of the range, with these two numbers separated by three dots, e.g., 4 . . . 9 = 4/5/6/7/8/9, or by
2) replacing Y by an appropriate indication of the output code and labelling the outputs with characters that refer to this code as in Figure 25.

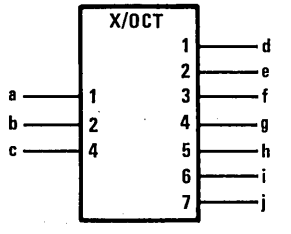
Alternatively, the general symbol may be used together with an appropriate reference to a table in which the relationship between the inputs and outputs is indicated. This is a recommended way to symbolize a PROM after it has been programmed.



TRUTH TABLE

INPUTS			OUTPUTS			
c	b	a	g	f	e	d
0	0	0	0	0	0	0
0	0	1	0	0	0	1
0	1	0	0	0	1	0
0	1	1	0	1	1	0
1	0	0	0	1	0	1
1	0	1	0	0	0	0
1	1	0	0	0	0	0
1	1	1	1	0	0	0

FIGURE 24 – AN X/Y CODE CONVERTER



TRUTH TABLE

INPUTS			OUTPUTS						
c	b	a	j	i	h	g	f	e	d
0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	1
0	1	0	0	0	0	0	0	1	0
0	1	1	0	0	0	0	1	0	0
1	0	0	0	0	0	1	0	0	0
1	0	1	0	0	1	0	0	0	0
1	1	0	0	1	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0

FIGURE 25 – AN X/OCTAL CODE CONVERTER

7 USE OF A CODER TO PRODUCE AFFECTING INPUTS

It often occurs that a set of affecting inputs for dependency notation is produced by decoding the signals on certain inputs to an element. In such a case use can be made of the symbol for a coder as an embedded symbol. See Figure 26.

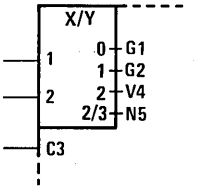


FIGURE 26 – PRODUCING VARIOUS TYPES OF DEPENDENCIES

If all affecting inputs produced by a coder are of the same type and their identifying numbers correspond with the numbers shown at the outputs of the coder, Y (in the qualifying symbol X/Y) may be replaced by the letter denoting the type of dependency. The indications of the affecting inputs should then be omitted. See Figure 27.

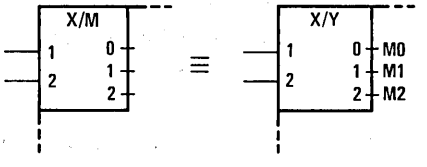


FIGURE 27 – PRODUCING ONE TYPE OF DEPENDENCY

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8 USE OF BINARY GROUPING TO PRODUCE AFFECTING INPUTS

If all affecting inputs produced by a coder are of the same type and have consecutive identifying numbers not necessarily corresponding with the numbers that would have been shown at the outputs of the coder, use can be made of the binary grouping symbol (see 3.1). k external lines effectively generate 2^k internal inputs. The bracket is followed by the letter denoting the type of dependency followed by $\frac{m1}{m2}$. The m1 is to be replaced by the smallest identifying number and the m2 by the largest one, as shown in Figure 28.

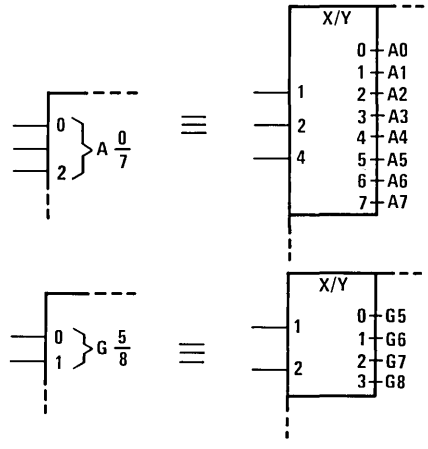

FIGURE 28 – USE OF THE BINARY GROUPING SYMBOL

9 SEQUENCE OF INPUT LABELS

If an input having a single functional effect is affected by other inputs, the qualifying symbol (if there is any) for that functional effect is preceded by the labels corresponding to the affecting inputs. The left-to-right order of these preceding labels is the order in which the effects or modifications must be applied. The affected input has no functional effect on the element if the logic state of any one of the affecting inputs, considered separately, would cause the affected input to have no effect, regardless of the logic states of other affecting inputs.

If an input has several different functional effects or has several different sets of affecting inputs, depending on the mode of action, the input may be shown as often as required. However, there are cases in which this method of presentation is not advantageous. In those cases the input may be shown once with the different sets of labels separated by solidi. See Figure 29. No meaning is attached to the order of these sets of labels. If one of the functional effects of an input is that of an unlabelled input of the element, a solidus will precede the first set of labels shown.

If all inputs of a combinational element are disabled (caused to have no effect on the function of the element), the internal logic states of the outputs of the element are not specified by the symbol. If all inputs of a sequential element are disabled, the content of this element is not changed and the outputs remain at their existing internal logic states.

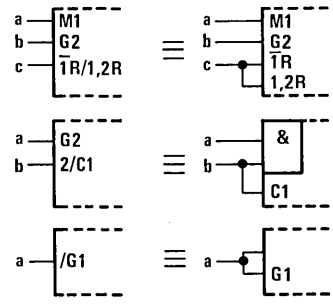

FIGURE 29 – INPUT LABELS

Labels may be factored using algebraic techniques.

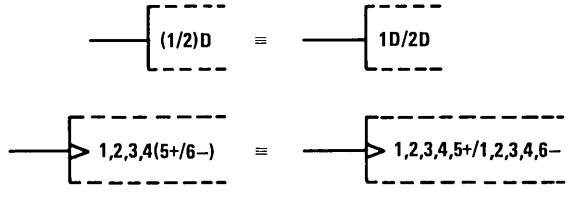

FIGURE 30 – FACTORING INPUT LABELS

10 SEQUENCE OF OUTPUT LABELS

If an output has a number of different labels, regardless of whether they are identifying number of affecting inputs or outputs or not, these labels are shown in the following order:

1) if the postponed output symbol has to be shown, this comes first, if necessary preceded by the indications of the inputs to which it must be applied;

2) followed by the labels indicating modifications of the internal logic state of the output, such that the left-to-right order of these labels corresponds with the order in which their effects must be applied;

3) followed by the label indicating the effect of the output on inputs and other outputs of the element.

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Symbols for open-circuit or three-state outputs, where applicable, are placed just inside the outside boundary of the symbol adjacent to the output line. See Figure 31.

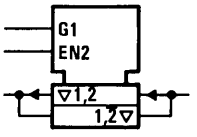

FIGURE 31 – PLACEMENT OF 3-STATE SYMBOLS

If an output needs several different sets of labels that represent alternative functions (e.g., depending on the mode of action), these sets may be shown on different output lines that must be connected outside the outline. However, there are cases in which this method of presentation is not advantageous. In those cases the output may be shown once with the different sets of labels separated by solidi. See Figure 32.

Two adjacent identifying numbers of affecting inputs in a set of labels that are not already separated by a nonnumeric character should be separated by a comma.

If a set of labels of an output not containing a solidus contains the identifying number of an affecting M*m* input standing at its internal 0 state, this set of labels has no effect on that output.

Labels may be factored using algebraic techniques.

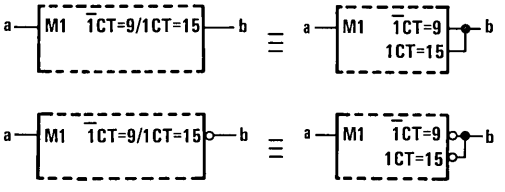

FIGURE 32 – OUTPUT LABELS

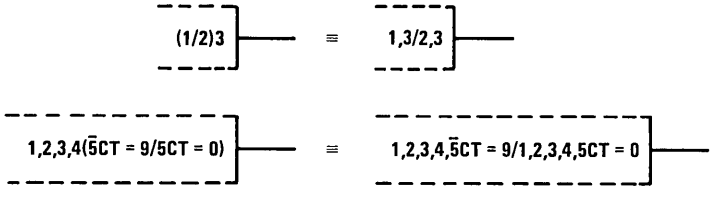

FIGURE 33 – FACTORING OUTPUT LABELS

If you have questions on this Explanation of New Logic Symbols, please contact:

F.A. Mann MS 84
Texas Instruments Incorporated
P.O. Box 225012
Dallas, Texas 75265
Telephone (214) 995-3746

IEEE Standards may be purchased from:

Institute of Electrical and Electronics Engineers, Inc.
345 East 47th Street
New York, N.Y. 10017

International Electrotechnical Commission (IEC) publications may be purchased from:

American National Standards Institute, Inc.
1430 Broadway
New York, N.Y. 10018

Revisions to The TTL Data Book Second Edition

6

Revisions to *The TTL Data Book for Design Engineers,* Second Edition

This section contains new information and corrections for device specifications in the *"Data Book"* divided into two parts as shown below.

The reader should check the Important Notices on the back of the title page to determine the status of his data book. Second printing copies are identified by the statement "Second printing" below the copyright notice. Third printing copies are similarly identified. All others are first printing.

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REVISIONS TO THE FIRST PRINTING

PAGE	LOCATION	CHANGE
1-3 thru 1-8	Alphanumeric Index	1. Several types have updated specifications. Add suffix A to the type numbers listed below. 'LS73 'LS113 'LS365 'LS76 'LS114 'LS366 'LS78 'LS125 'LS367 'LS107 'LS126 'LS368 'LS112 2. Add at the end of the index: TIM9908 7-448 7-448
1-9 thru 1-28 and partially repeated 7-3 thru 7-14	Functional Index and Selection Guide	1. Add suffix A to type numbers listed above. For possible changes in selection data, see individual data sheet revisions. 2. Remove * (indicating new products) from type numbers listed below. These are now standard devices. This also applies to data sheets. 'LS147 'LS245† SN74LS362† 'LS148 'LS275 'LS373 'LS183 'LS295B 'LS374 'S226 'LS348† 'LS395A †Appears twice in index.
5-4	Absolute maximum ratings	Change "High-level voltage applied to a disabled 3-state output" from V_{CC} or 7 V to 5.5 V, for all except Series 54L/74L. Series 54L/74L has no specification.
5-6 thru 5-77	Pin assignment drawings	Add suffix A to same type numbers as in Alphanumeric Index.
5-32	107	Delete "MASTER-SLAVE" from title. Add function table for 'LS107A like that for 'LS73A on page 5-22.
5-45	168 and 170	Change SN74S168 (J, W) to SN74S168 (J, N) and SN74170 (J, W) to SN74170 (J, N)
5-50	192	Change SN74192 (J, N) second line to SN74L192 (J, N)
5-55	241 243	Re-label pin 17 to be 2A4. Change SN54243 (J, W) SN74243 (J, N) to SN54LS243 (J, W) SN74LS243 (J, N)
5-58	266	Re-label pin assignment drawing as shown below. pin 4 2Y pin 8 3A pin 5 2A pin 9 3B pin 6 2B pin 10 3Y
5-62	287 288 289	Change from SN74S287 (J, W) to SN74S287 (J, N) Change from SN74S288 (J, W) to SN74S288 (J, N) Change from SN74S289 (J, W) to SN74S289 (J, N)
5-64	299	1. Re-label pin 9 connection "CLEAR" two places. 2. Re-label pin 12 connection "CLOCK" two places.
6-25	Switching characteristics: '38	Change test condition from R_L = 667 Ω to R_L = 133 Ω

REVISIONS TO THE FIRST PRINTING

PAGE	LOCATION: AFFECTED TYPES	CHANGE
6-33	'LS125, 'LS126	Add suffix A to type numbers two places.
	Recommended operating conditions: 'LS125A, 'LS126A	Change I_{OL} max limits: from to 54 FAMILY 8 mA 12 mA 74 FAMILY 16 mA 24 mA
	Electrical characteristics: 'LS125A, 'LS126A	Change test condition for V_{OL} for Series 74LS from I_{OL} = 8 mA to I_{OL} = 12 mA.
6-34	'LS125, 'LS126	Add suffix A to type numbers three places each.
	Switching characteristics: 'LS125A, 'LS126A	1. Change SN54LS/74LS test conditions to be C_L = 45 pF, R_L = 667 Ω C_L = 5 pF, R_L = 667 Ω 2. Change note to read "# Load circuit and voltage waveforms are shown on pages 3-10 and 3-11."
6-35	Schematic: 'LS125	Add suffix A to type number and add "C INPUT" to unlabeled input at left.
	Schematic: 'LS126	Add suffix A to type number and change "$\overline{G}$ INPUT" to "C INPUT."
6-36	'LS365, 'LS366 'LS367, 'LS368	Add suffix A to type numbers two places.
	Recommended operating conditions: 'LS365A thru 'LS368A	Change I_{OL} maximum limits: from to SN54 FAMILY 8 mA 12 mA SN74 FAMILY 16 mA 24 mA
	Electrical characteristics: 'LS365A thru 'LS368A	Change V_{OL} test conditions to be: V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max; I_{OL} = MAX; I_{OL} = 12 mA
6-37	'LS365, 'LS366 'LS367, 'LS368	Add suffix A to type numbers.
	Schematics: '367A, '368A	†R is 600 Ω for the control section associated with $\overline{G}$1 and 900 Ω for the control section associated with $\overline{G}$2.
	Switching characteristics: 'LS365A thru 'LS368A	Change SN54LS/74LS test conditions: C_L = 45 pF, R_L = 667 Ω C_L = 5 pF, R_L = 667 Ω
6-38	'LS365, 'LS366 'LS367, 'LS368	Add suffix A to type numbers.

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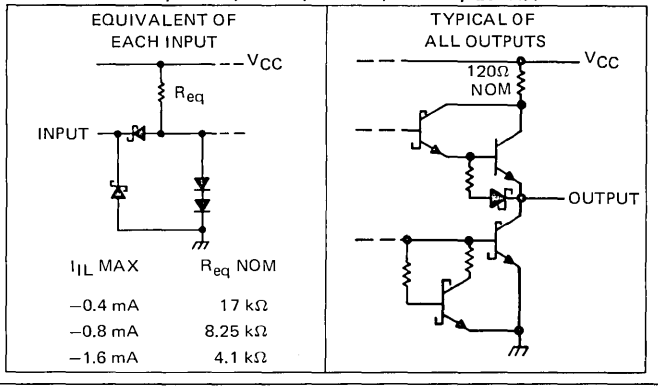
<table>
<tr><th>PAGE</th><th>LOCATION:
AFFECTED TYPES</th><th>CHANGE</th></tr>
<tr><td>6-40</td><td>Electrical characteristics:
'23, '50, '53</td><td>1. Change $I_{\overline{X}}$ maximum limit for SN7423 from −3.5 mA to −3.8 mA.
2. Change V_{OL} test conditions:
from: (SN54'): $R_{\overline{X}X}$ = 138 Ω; (SN74'): $R_{\overline{X}X}$ = 130 Ω
to: (SN54'): $R_{\overline{X}X}$ = ▲; (SN74'): $R_{\overline{X}X}$ = ▲
3. Add note "▲ $R_{\overline{X}X}$ equals 114 Ω for SN5423, 138 Ω for SN5450 and SN5453, 105 Ω for SN7423, and 130 Ω for SN7450 and SN7453."</td></tr>
<tr><td>6-43</td><td>Electrical characteristics:
SN7460</td><td>Change test condition for $V_{\overline{X}X(on)}$ from $I_{\overline{X}}$ = 3.5 mA to $I_{\overline{X}}$ = 3.8 mA.</td></tr>
<tr><td>6-56</td><td>'LS73, 'LS107, 'LS113
'LS76, 'LS112,
'LS78, 'LS114</td><td>1. Add suffix A to type numbers two places.
2. Change I_{CC} maximum limit from 8 mA to 6 mA in first, third, and fourth columns only.</td></tr>
<tr><td>6-57</td><td>'LS73, 'LS76, 'LS78,
'LS107, 'LS112,
'LS113, 'LS114</td><td>1. Add suffix A to the type numbers in the switching characteristics table, the functional block diagram, and the block diagram caption.
2. Change switching characteristics:
t_{PLH} typical: from 11 ns to 15 ns
t_{PHL} maximum: from 30 ns to 20 ns
3. Change schematics as shown below.
'LS73A, 'LS76A, 'LS78A, 'LS112A, 'LS113A, 'LS114A
 
</td></tr>
<tr><td>6-61</td><td>Switching characteristics:
'279, 'LS279</td><td>1. Label existing limits column for '279.
2. Add new column shown:
<table><tr><th colspan="3">'LS279</th></tr><tr><th>MIN</th><th>TYP</th><th>MAX</th></tr><tr><td></td><td>12</td><td>22</td></tr><tr><td></td><td>13</td><td>21</td></tr><tr><td></td><td>15</td><td>27</td></tr></table></td></tr>
<tr><td>6-69</td><td>Equivalent input:
'LS221</td><td>Delete "25 kΩ NOM" and replace with "R_{eq}".</td></tr>
</table>

REVISIONS TO THE FIRST PRINTING

<table>
<tr><th>PAGE</th><th>LOCATION:
AFFECTED TYPES</th><th>CHANGE</th></tr>
<tr><td rowspan="2">6-71</td><td>Recommended operating conditions:
'LS221</td><td>Change "Output duty cycle " maximum limits for R_T = 2 kΩ from 67% to 50%.</td></tr>
<tr><td>Electrical characteristics:
'LS221</td><td>Change I_{IL} maximum limit for Input B from −0.4 mA to −0.8 mA.</td></tr>
<tr><td>6-83</td><td>'LS241, 'S241</td><td>Relabel pin 17 "2A4" in pin assignment drawing.</td></tr>
<tr><td>6-84</td><td>Electrical characteristics:
'LS240, 'LS241,
'LS244</td><td>1. Change V_{OH} test conditions to be:
<table><tr><td>V_{CC} = MIN,</td><td>V_{IH} = 2 V,</td></tr><tr><td>V_{IL} = V_{IL} max,</td><td>I_{OH} = −3 mA</td></tr><tr><td>V_{CC} = MIN,</td><td>V_{IH} = 2 V,</td></tr><tr><td>V_{IL} = 0.5 V,</td><td>I_{OH} = MAX</td></tr></table>2. Change I_{OS} minimum limit from −50 mA to −40 mA two places.</td></tr>
<tr><td>6-85</td><td>Electrical characteristics:
SN74S240, SN74S241</td><td>Add a set of test conditions and limits for V_{OH} and label existing conditions as shown below.
<table><tr><th></th><th></th><th>MIN</th><th>TYP</th><th>MAX</th><th>MIN</th><th>TYP</th><th>MAX</th><th>UNIT</th></tr><tr><td>SN74S'</td><td>V_{CC} = MIN, V_{IH} = 2 V,
V_{IL} = 0.8 V, I_{OH} = −1 mA</td><td>2.7</td><td></td><td></td><td>2.7</td><td></td><td></td><td rowspan="3">V</td></tr><tr><td>SN54S' and SN74S'</td><td>V_{CC} = MIN, V_{IH} = 2 V,
V_{IL} = 0.8 V, I_{OH} = −3 mA</td><td>2.4</td><td>3.4</td><td></td><td>2.4</td><td>3.4</td><td></td></tr><tr><td>SN54S' and SN74S'</td><td>V_{CC} = MIN, V_{IH} = 2 V,
V_{IL} = 0.5 V, I_{OH} = MAX</td><td>2</td><td></td><td></td><td>2</td><td></td><td></td></tr></table></td></tr>
<tr><td>6-88</td><td>Electrical characteristics:
'LS242, 'LS243</td><td>1. Change I_{OZH} maximum limit from 20 μA to 40 μA two places.
2. Add a set of test conditions and limits for I_I as shown below.
<table><tr><th></th><th></th><th></th><th>MIN</th><th>TYP</th><th>MAX</th><th>MIN</th><th>TYP</th><th>MAX</th><th>UNIT</th></tr><tr><td>A or B</td><td rowspan="2">V_{CC} = MAX</td><td>V_I = 5.5 V</td><td></td><td></td><td>0.1</td><td></td><td></td><td>0.1</td><td rowspan="2">mA</td></tr><tr><td>$\overline{G}$AB or GBA</td><td>V_I = 7 V</td><td></td><td></td><td>0.1</td><td></td><td></td><td>0.1</td></tr></table>3. Change I_{OS} minimum limit from −50 mA to −40 mA two places.</td></tr>
<tr><td>6-96</td><td>Figure 10, Note B:
Expandable gates</td><td>Delete the parenthetic statement regarding resistor values and add the table below.
RESISTANCE VALUE TABLE
<table><tr><td>SN5423</td><td>114 Ω</td></tr><tr><td>SN5450, SN5453</td><td>138 Ω</td></tr><tr><td>SN7423</td><td>105 Ω</td></tr><tr><td>SN7450, SN7453</td><td>130 Ω</td></tr></table></td></tr>
</table>

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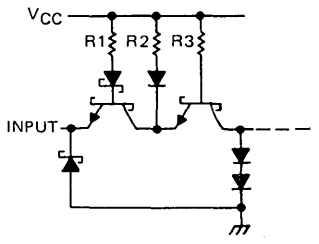
<table>
<tr><th>PAGE</th><th>LOCATION:
AFFECTED TYPES</th><th>CHANGE</th></tr>
<tr><td>7-74</td><td>'LS90, 'LS92, 'LS93</td><td>Delete Schottky diode in parallel with input transistor.
'LS90, 'LS92, 'LS93
EQUIVALENT OF A AND B INPUTS
 

NOMINAL VALUES
<table>
<tr><th>INPUT</th><th>R1</th><th>R2</th><th>R3</th></tr>
<tr><td>A</td><td>10 kΩ</td><td>10 kΩ</td><td>10 kΩ</td></tr>
<tr><td>B ('LS90, 'LS92)</td><td>6.7 kΩ</td><td>6.7 kΩ</td><td>5 kΩ</td></tr>
<tr><td>B ('LS93)</td><td>15 kΩ</td><td>15 kΩ</td><td>10 kΩ</td></tr>
</table></td></tr>
<tr><td>7-78</td><td>Electrical characteristics: 'LS90, 'LS92</td><td>1. Change I_{IL} "output current" to "input current".
2. Change note to be "¶ Q_A outputs are tested . . ."</td></tr>
<tr><td>7-79</td><td>Electrical characteristics: 'LS93</td><td>Change I_{IL} "output current" to "input current".</td></tr>
<tr><td>7-100</td><td>Recommended operating conditions: 'LS96</td><td>Change "width of clock pulse, $t_{w(clock)}$" minimum limit from 35 ns to 20 ns.</td></tr>
<tr><td>7-123</td><td>Description: 'LS124, 'S124</td><td>Delete the last sentence of the fourth paragraph under description, "Simultaneous operation . . . not recommended."</td></tr>
<tr><td rowspan="3">7-155</td><td>Electrical characteristics: 'LS147, 'LS148</td><td>Change SN54LS', SN74LS' maximum V_{OH} limits to minimum limits.</td></tr>
<tr><td>Switching characteristics: 'LS147</td><td>Change 'LS147 limits column to be:
<table>
<tr><th>MIN</th><th>TYP</th><th>MAX</th></tr>
<tr><td></td><td>12</td><td>18</td></tr>
<tr><td></td><td>12</td><td>18</td></tr>
<tr><td></td><td>21</td><td>33</td></tr>
<tr><td></td><td>15</td><td>23</td></tr>
</table></td></tr>
<tr><td>Switching characteristics: 'LS148</td><td>Change 'LS148 limits column to be:
<table>
<tr><th>MIN</th><th>TYP</th><th>MAX</th></tr>
<tr><td></td><td>14</td><td>18</td></tr>
<tr><td></td><td>15</td><td>25</td></tr>
<tr><td></td><td>20</td><td>36</td></tr>
<tr><td></td><td>16</td><td>29</td></tr>
<tr><td></td><td>7</td><td>18</td></tr>
<tr><td></td><td>25</td><td>40</td></tr>
<tr><td></td><td>35</td><td>55</td></tr>
<tr><td></td><td>9</td><td>21</td></tr>
<tr><td></td><td>16</td><td>25</td></tr>
<tr><td></td><td>12</td><td>25</td></tr>
<tr><td></td><td>12</td><td>17</td></tr>
<tr><td></td><td>14</td><td>36</td></tr>
<tr><td></td><td>12</td><td>21</td></tr>
<tr><td></td><td>23</td><td>35</td></tr>
</table></td></tr>
</table>

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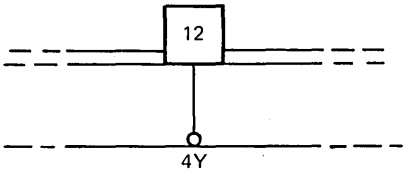
<table>
<tr><th>PAGE</th><th>LOCATION:
AFFECTED TYPES</th><th>CHANGE</th></tr>
<tr><td>7-177</td><td>Electrical characteristics:
'155</td><td>Change V_{IK} test conditions from $I_I = -12$ mA to $I_I = -8$ mA.</td></tr>
<tr><td>7-179</td><td>Electrical characteristics:
'156</td><td>Change V_{IK} test conditions from $I_I = -12$ mA to $I_I = -8$ mA.</td></tr>
<tr><td>7-181</td><td>Pin assignment
drawing:
'LS158, 'S158</td><td>Add inversion indicator for output 4Y.
 
</td></tr>
<tr><td>7-187</td><td>Electrical characteristics:
'S157, 'S158</td><td>1. Change Note 2 to read "I_{CC} is measured with all outputs open".
2. Change I_{CC} test conditions and limits columns to be:
<table>
<tr><th></th><th>MIN</th><th>TYP</th><th>MAX</th><th>MIN</th><th>TYP</th><th>MAX</th><th>UNIT</th></tr>
<tr><td>V_{CC} = MAX, All inputs at 4.5 V, See Note 2</td><td></td><td>50</td><td>78</td><td></td><td>39</td><td>61</td><td rowspan="2">mA</td></tr>
<tr><td>V_{CC} = MAX, A Inputs at 4.5 V, B, G, S Inputs at 0 V, See Note 2</td><td></td><td></td><td></td><td></td><td></td><td>81</td></tr>
</table></td></tr>
<tr><td>7-190</td><td>Description:
'160 thru '163,
'LS160A thru 'LS163A,
'S162, 'S163</td><td>Change third and fourth sentences of second paragraph to read: "Low-to-high transitions at the load input of the '160 thru '163 should be avoided when the clock is low if the enable inputs are high at or before the transition. This restriction is not applicable to the 'LS160A thru 'LS163A or 'S162 or 'S163."</td></tr>
<tr><td>7-200</td><td>Equivalent schematic
of each input:
'S162, 'S163</td><td>Add a 20-kΩ resistor between V_{CC} and Input for all inputs except clock and load.
Clock and load inputs have no such resistor.</td></tr>
<tr><td>7-219</td><td>Notes: '166</td><td>1. Change present Note 2 to Note 3.
2. Add new Note 2: An SN54166 in the W package operating at free-air temperatures above 113°C requires a heat sink that provides a thermal resistance from case to free air, $R_{\theta CA}$, of not more than 48°C/W.</td></tr>
<tr><td></td><td>Absolute maximum
ratings: SN54166</td><td>Add "(see Note 2)" to "Operating free-air temperature range: SN54166."</td></tr>
<tr><td></td><td>Recommended operating
conditions: SN54166</td><td>Add "(see Note 2)" to "Operating free-air temperature range, T_A."</td></tr>
<tr><td></td><td>Electrical characteristics:
'166</td><td>1. Change I_{CC} test condition from "See Note 2" to "See Note 3."
2. Change I_{CC} values as shown:
<table>
<tr><th>MIN</th><th>TYP</th><th>MAX</th><th>MIN</th><th>TYP</th><th>MAX</th></tr>
<tr><td></td><td>90</td><td>127</td><td></td><td>90</td><td>127</td></tr>
</table></td></tr>
</table>

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PAGE	LOCATION: AFFECTED TYPES	CHANGE
7-220	Electrical characteristics: 'LS166	Change "Note 2" to "Note 3" for I_{CC} test conditions and in notes.
7-227	Block Diagram: 'LS169A	Change the AND gate for Ripple Carry output, Pin 15, to a NAND gate.
7-233	Equivalent schematic of each input: 'S168, 'S169	Add a 20-kΩ resistor between V_{CC} and the Input for Load input only. All other inputs have no such resistor.
7-286	Typical application data: '182, 'S182	Change " '181 or 'S182" to " '182 or 'S182".
7-288	Electrical characteristics: 'H183	1. Add I_{CCH} maximum limit of 65 mA. 2. Change Note 4 ". . . and all outputs at 4.5 V" to ". . . and all inputs at 4.5 V".
7-289	Note 4: 'LS183	Change Note 4 ". . .and all outputs at 4.5 V." to ". . . and all inputs at 4.5 V".
	Switching characteristics: 'LS183	Change limits column to be: MIN TYP MAX 9 15 20 33
7-302	Recommended operating conditions: 'LS190, 'LS191	Change minimum limit for "Count enable time, t_{enable}" from 20 ns to 40 ns two places.
7-306	Description: '192, '193, 'L192, 'L193, 'LS192, 'LS193	Change ". . . count-down input" in the next-to-last line to ". . . count-up input".
7-313	Recommended operating conditions: 'LS192, 'LS193	Add parameter "Clear inactive-state setup time, t_{su}" with minimum limit of 40 ns for SN54LS' and SN74LS'.
	Switching characteristics: 'LS142, 'LS143	Change limits column to be: MIN TYP MAX 25 32 17 26 18 24 16 24 15 24 27 38 30 47 24 40 25 40 23 35
7-332	Recommended operating conditions: '196, '197	Change "Pulse width, t_w" Clock-1 input minimum limit from 20 ns to 10 ns two places, and Clock-2 input minimum limit from 30 ns to 20 ns two places.
7-334	Recommended operating conditions: 'LS196, 'LS197	Change "Count enable time, t_{enable}" minimum limit from 20 ns to 30 ns two places.

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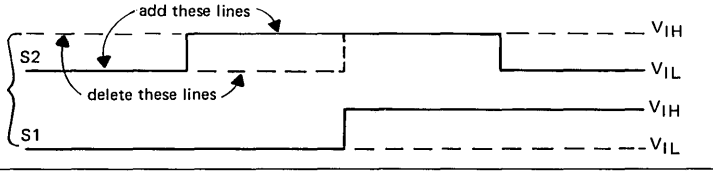
<table>
<tr><th>PAGE</th><th>LOCATION
AFFECTED TYPES</th><th>CHANGE</th></tr>
<tr><td>7-343</td><td>Electrical characteristics:
'198, '199</td><td>Change limits columns for I_{CC} to be:
<table>
<tr><th>MIN</th><th>TYP</th><th>MAX</th><th>MIN</th><th>TYP</th><th>MAX</th><th>UNIT</th></tr>
<tr><td></td><td>90</td><td>127</td><td></td><td>90</td><td>127</td><td>mA</td></tr>
</table></td></tr>
<tr><td rowspan="2">7-346</td><td>Function tables:
'S226</td><td>Modify the first two lines to make the table read:
BUS-MANAGEMENT FUNCTION TABLE
<table>
<tr><th>OPERATION</th><th>S2</th><th>S1</th><th>LATCH FUNCTIONS</th></tr>
<tr><td>DRIVE BUS A</td><td>L</td><td>L</td><td>Pass Bus B Data to Bus A</td></tr>
<tr><td>DRIVE BUS B</td><td>H</td><td>L</td><td>Pass Bus A Data to Bus B</td></tr>
<tr><td>EXCHANGE</td><td>H</td><td>H</td><td>Store Bus A and Bus B Data</td></tr>
<tr><td>BUS A AND B</td><td>L</td><td>H</td><td>Read Out Stored Data</td></tr>
</table></td></tr>
<tr><td>Absolute maximum ratings:
SN54S226</td><td>1. Change operating temperature specification to be:
Operating free-air temperature range: SN54S226 (see Note 2) . . .
2. Add "NOTE 2: An SN54S226 in the J package operating at temperatures above 113°C requires a heat-sink that provides a thermal resistance from case to free air, $R_{\theta CA}$, of not more than 48°C/W."</td></tr>
<tr><td rowspan="2">7-347</td><td>Recommended operating conditions: 'S226</td><td>1. Change minimum limit for "Data setup time, t_{su}" from 5↓ to 0↓ four places.
2. Change minimum limit for "Data hold time, t_h" from 5↓ to 30↓ four places.
3. Add (see Note 2) to "Operating free-air temperature, T_A".</td></tr>
<tr><td>Electrical characteristics:
'S226</td><td>1. Change present Note 2 to Note 3 and add new Note 2 same as page 7-346.
2. Change I_{CC} test conditions from "See Note 2" to "See Note 3" and add a maximum limit of 185 mA.
3. Change I_{IL} maximum limit from −300 μA to −380 μA.</td></tr>
<tr><td rowspan="3">7-348</td><td>Switching characteristics:
'S226</td><td>Change table as shown:
<table>
<tr><th>TEST CONDITIONS</th><th>MIN</th><th>TYP</th><th>MAX</th><th>UNIT</th></tr>
<tr><td rowspan="8">C_L = 50 pF, R_L = 280 Ω,
See Note 4</td><td></td><td>20</td><td>30</td><td rowspan="2">ns</td></tr>
<tr><td></td><td>15</td><td>30</td></tr>
<tr><td></td><td>25</td><td>37</td><td rowspan="2">ns</td></tr>
<tr><td></td><td>19</td><td>30</td></tr>
<tr><td></td><td>25</td><td>37</td><td rowspan="2">ns</td></tr>
<tr><td></td><td>19</td><td>30</td></tr>
<tr><td></td><td>12</td><td>20</td><td rowspan="2">ns</td></tr>
<tr><td></td><td>12</td><td>20</td></tr>
<tr><td rowspan="2">C_L = 5 pF, R_L = 280 Ω,
See Note 4</td><td></td><td>10</td><td>15</td><td rowspan="2">ns</td></tr>
<tr><td></td><td>10</td><td>15</td></tr>
</table></td></tr>
<tr><td>Notes: 'S226</td><td>Change present Note 2 to Note 4.</td></tr>
<tr><td>Applications:
'S226</td><td>Change voltage waveform as shown:
 
</td></tr>
</table>

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<table>
<tr><th>PAGE</th><th>LOCATION:
AFFECTED TYPES</th><th>CHANGE</th></tr>
<tr><td>7-349</td><td>Features: 'LS245</td><td>• Typical Propagation Delay Times, Port-to-Port . . . 8 ns</td></tr>
<tr><td>7-350</td><td>Electrical characteristics:
'LS245</td><td>1. Change limits columns for parameters shown.
<table>
<tr><th></th><th></th><th></th><th>MIN</th><th>TYP</th><th>MAX</th><th>MIN</th><th>TYP</th><th>MAX</th><th>UNIT</th></tr>
<tr><td>I_{OZH}</td><td></td><td></td><td></td><td></td><td>10</td><td></td><td></td><td>10</td><td>μA</td></tr>
<tr><td>I_{OZL}</td><td></td><td></td><td></td><td></td><td>−200</td><td></td><td></td><td>−200</td><td></td></tr>
<tr><td>I_{CC}</td><td></td><td></td><td></td><td>48</td><td>70</td><td></td><td>48</td><td>70</td><td>mA</td></tr>
<tr><td></td><td></td><td></td><td></td><td>62</td><td>90</td><td></td><td>62</td><td>90</td><td></td></tr>
<tr><td></td><td></td><td></td><td></td><td>64</td><td>95</td><td></td><td>64</td><td>95</td><td></td></tr>
</table>
2. Change I_I test conditions and limits as shown below.
<table>
<tr><td>A or B</td><td rowspan="2">V_{CC} = MAX</td><td>V_I = 5.5 V</td><td></td><td>0.1</td><td></td><td>0.1</td><td rowspan="2">mA</td></tr>
<tr><td>DIR or $\overline{G}$</td><td>V_I = 7 V</td><td></td><td>0.1</td><td></td><td>0.1</td></tr>
</table></td></tr>
<tr><td></td><td>Switching characteristics:
'LS245</td><td>Change limits column to be:
<table>
<tr><th>MIN</th><th>TYP</th><th>MAX</th></tr>
<tr><td></td><td>8</td><td>12</td></tr>
<tr><td></td><td>8</td><td>12</td></tr>
<tr><td></td><td>27</td><td>40</td></tr>
<tr><td></td><td>25</td><td>40</td></tr>
<tr><td></td><td>15</td><td>25</td></tr>
<tr><td></td><td>15</td><td>25</td></tr>
</table></td></tr>
<tr><td>7-374</td><td>Electrical characteristics:
'LS257, 'LS258</td><td>Change I_{OZH} test condition from V_O = 2.4 V to V_O = 2.7 V</td></tr>
<tr><td></td><td>Switching characteristics:
'LS257, 'LS258</td><td>Change R_L = 667 kΩ to R_L = 667 Ω</td></tr>
<tr><td>7-375</td><td>Electrical characteristics:
'S257, 'S258</td><td>Add to V_{OH} new test conditions and limits as shown.
<table>
<tr><th></th><th></th><th>MIN</th><th>TYP</th><th>MAX</th><th>MIN</th><th>TYP</th><th>MAX</th><th>UNIT</th></tr>
<tr><td>V_{CC} = MIN, V_{IH} = 2 V,
V_{IL} = 0.8 V, I_{OH} = −1 mA</td><td>SN74S'</td><td>2.7</td><td></td><td></td><td>2.7</td><td></td><td></td><td>V</td></tr>
</table></td></tr>
<tr><td>7-393</td><td>Switching characteristics:
'LS275</td><td>Change test conditions and limits columns as shown.
<table>
<tr><th></th><th></th><th></th><th>MIN</th><th>TYP</th><th>MAX</th></tr>
<tr><td></td><td>Any</td><td>C_L = 45 pF, R_L = 667 Ω,
See Note 2</td><td></td><td>35
42</td><td>62
66</td></tr>
<tr><td rowspan="3">Enable $\overline{G}$</td><td rowspan="3">Any</td><td>C_L = 45 pF, R_L = 667 Ω,
See Note 2</td><td></td><td>8
13</td><td>23
23</td></tr>
<tr><td>C_L = 5 pF, R_L = 667 Ω,
See Note 2</td><td></td><td>10
10</td><td>15
15</td></tr>
</table></td></tr>
<tr><td>7-407</td><td>Electrical characteristics:
SN54LS280</td><td>Change I_{CC} minimum value for SN54LS280 to a typical value (16 mA).</td></tr>
</table>

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<table>
<tr><th>PAGE</th><th>LOCATION:
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<tr><td>7-426</td><td>Electrical characteristics:
'290, '293</td><td>Change I_{IL} "High-level input . . ." to "Low-level input . . ."</td></tr>
<tr><td></td><td>Switching characteristics:
'290</td><td>Change t_{PHL} maximum limit, bottom line, from 24 ns to 40 ns.</td></tr>
<tr><td>7-428</td><td>Electrical characteristics:
'LS290, 'LS293</td><td>Change I_{IL} "Low-level output . . ." to "Low-level input . . ."</td></tr>
<tr><td>7-430</td><td>Electrical characteristics:
'295B</td><td>Change I_{CC} limits columns to be:
<table>
<tr><th>MIN</th><th>TYP</th><th>MAX</th><th>MIN</th><th>TYP</th><th>MAX</th><th>UNIT</th></tr>
<tr><td></td><td>20</td><td>29</td><td></td><td>20</td><td>29</td><td rowspan="2">mA</td></tr>
<tr><td></td><td>22</td><td>33</td><td></td><td>22</td><td>33</td></tr>
</table></td></tr>
<tr><td>7-431</td><td>Switching characteristics:
'LS295B</td><td>Change limits column to be:
<table>
<tr><th>MIN</th><th>TYP</th><th>MAX</th></tr>
<tr><td>30</td><td>45</td><td></td></tr>
<tr><td></td><td>14</td><td>20</td></tr>
<tr><td></td><td>19</td><td>30</td></tr>
<tr><td></td><td>18</td><td>26</td></tr>
<tr><td></td><td>20</td><td>30</td></tr>
<tr><td></td><td>13</td><td>20</td></tr>
<tr><td></td><td>13</td><td>20</td></tr>
</table></td></tr>
<tr><td>7-440</td><td>Electrical characteristics:
'LS299</td><td>1. Change I_I as shown below.
<table>
<tr><th></th><th></th><th></th><th>MIN</th><th>TYP</th><th>MAX</th><th>MIN</th><th>TYP</th><th>MAX</th><th>UNIT</th></tr>
<tr><td>S0, S1</td><td rowspan="3">V_{CC} = MAX</td><td>V_I = 7 V</td><td></td><td></td><td>200</td><td></td><td></td><td>200</td><td rowspan="3">μA</td></tr>
<tr><td>A thru H</td><td>V_I = 5.5 V</td><td></td><td></td><td>100</td><td></td><td></td><td>100</td></tr>
<tr><td>Any other</td><td>V_I = 7 V</td><td></td><td></td><td>100</td><td></td><td></td><td>100</td></tr>
</table>
2. Change I_{IH} maximum limit for "Any other" input from 30 μA to 20 μA two places.
3. Change I_{IL} test condition from V_I = 0.5 V to V_I = 0.4 V.</td></tr>
<tr><td>7-449</td><td>Electrical characteristics:
'LS348</td><td>Add I_{OZ} for A0, A1, and A2 outputs exactly like that for the 'LS353 on page 7-459.</td></tr>
<tr><td>7-450</td><td>Switching characteristics:
'LS348
(TIM9908)</td><td>Change test conditions and limits column as shown below.
<table>
<tr><th>TEST CONDITIONS</th><th>MIN</th><th>TYP</th><th>MAX</th><th>UNIT</th></tr>
<tr><td rowspan="4">C_L = 45 pF,
R_L = 667 Ω,
See Note 3</td><td></td><td>11</td><td>17</td><td rowspan="2">ns</td></tr>
<tr><td></td><td>20</td><td>30</td></tr>
<tr><td></td><td>23</td><td>35</td><td rowspan="2">ns</td></tr>
<tr><td></td><td>23</td><td>35</td></tr>
<tr><td rowspan="8">C_L = 15 pF,
R_L = 2 kΩ,
See Note 3</td><td></td><td>11</td><td>18</td><td rowspan="2">ns</td></tr>
<tr><td></td><td>26</td><td>40</td></tr>
<tr><td></td><td>38</td><td>55</td><td rowspan="2">ns</td></tr>
<tr><td></td><td>9</td><td>21</td></tr>
<tr><td></td><td>11</td><td>17</td><td rowspan="2">ns</td></tr>
<tr><td></td><td>14</td><td>36</td></tr>
<tr><td></td><td>17</td><td>21</td><td rowspan="2">ns</td></tr>
<tr><td></td><td>25</td><td>40</td></tr>
<tr><td rowspan="2">C_L = 45 pF, R_L = 667 Ω,
See Note 3</td><td></td><td>25</td><td>39</td><td rowspan="2">ns</td></tr>
<tr><td></td><td>24</td><td>41</td></tr>
<tr><td rowspan="2">C_L = 5 pF,
R_L = 667 Ω</td><td></td><td>18</td><td>27</td><td rowspan="2">ns</td></tr>
<tr><td></td><td>23</td><td>35</td></tr>
</table></td></tr>
</table>

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<table>
<tr><th>PAGE</th><th>LOCATION:
AFFECTED TYPES</th><th>CHANGE</th></tr>
<tr><td>7-453</td><td>Switching characteristics:
'351</td><td>Add maximum values and change one typical value as shown below.
<table>
<tr><th>MIN</th><th>TYP</th><th>MAX</th><th>UNIT</th></tr>
<tr><td></td><td>20</td><td>30</td><td rowspan="2">ns</td></tr>
<tr><td></td><td>20</td><td>30</td></tr>
<tr><td></td><td>10</td><td>22</td><td rowspan="2">ns</td></tr>
<tr><td></td><td>10</td><td>22</td></tr>
<tr><td></td><td>18</td><td>33</td><td rowspan="2">ns</td></tr>
<tr><td></td><td>20</td><td>33</td></tr>
<tr><td></td><td>6</td><td>20</td><td rowspan="2">ns</td></tr>
<tr><td></td><td>10</td><td>20</td></tr>
</table></td></tr>
<tr><td>7-463</td><td>Switching characteristics:
'LS362 (TIM9904)</td><td>1. Change V_{CC1} to V_{CC} and V_{CC2} to V_{DD}.
2. Change minimum limits for $t_{r(\phi)}$ and $t_{f(\phi)}$ from 10 ns to 5 ns.</td></tr>
<tr><td rowspan="2">7-474</td><td>Electrical characteristics:
'LS374</td><td>Change I_{CC} maximum limit for 'LS374 from 45 mA to 40 mA two places.</td></tr>
<tr><td>Switching characteristics:
'LS373, 'LS374</td><td>Change limits columns to be:
<table>
<tr><th colspan="3">'LS373</th><th colspan="3">'LS374</th></tr>
<tr><th>MIN</th><th>TYP</th><th>MAX</th><th>MIN</th><th>TYP</th><th>MAX</th></tr>
<tr><td></td><td></td><td></td><td>35</td><td>50</td><td></td></tr>
<tr><td></td><td>12</td><td>18</td><td></td><td></td><td></td></tr>
<tr><td></td><td>12</td><td>18</td><td></td><td></td><td></td></tr>
<tr><td></td><td>20</td><td>30</td><td></td><td>15</td><td>28</td></tr>
<tr><td></td><td>18</td><td>30</td><td></td><td>19</td><td>28</td></tr>
<tr><td></td><td>15</td><td>28</td><td></td><td>20</td><td>28</td></tr>
<tr><td></td><td>25</td><td>36</td><td></td><td>21</td><td>28</td></tr>
<tr><td></td><td>12</td><td>20</td><td></td><td>12</td><td>20</td></tr>
<tr><td></td><td>15</td><td>25</td><td></td><td>14</td><td>25</td></tr>
</table></td></tr>
<tr><td>7-497</td><td>Electrical characteristics:
'S395A</td><td>Change limits columns for I_{CC} as shown.
<table>
<tr><th>MIN</th><th>TYP</th><th>MAX</th><th>MIN</th><th>TYP</th><th>MAX</th></tr>
<tr><td></td><td>22</td><td>34</td><td></td><td>22</td><td>34</td></tr>
<tr><td></td><td>21</td><td>31</td><td></td><td>21</td><td>31</td></tr>
</table></td></tr>
<tr><td>7-498</td><td>Switching characteristics:
'LS395</td><td>Change limits column to be:
<table>
<tr><th>MIN</th><th>TYP</th><th>MAX</th></tr>
<tr><td>30</td><td>45</td><td></td></tr>
<tr><td></td><td>22</td><td>35</td></tr>
<tr><td></td><td>15</td><td>30</td></tr>
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<tr><td></td><td>15</td><td>25</td></tr>
<tr><td></td><td>17</td><td>25</td></tr>
<tr><td></td><td>11</td><td>17</td></tr>
<tr><td></td><td>12</td><td>20</td></tr>
</table></td></tr>
</table>

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<table>
<tr><th>PAGE</th><th>LOCATION:
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<tr><td rowspan="2">7-510</td><td>Switching characteristics:
SN74LS424 (TIM8224)</td><td>1. Change minimum limit for $t_{\phi 2L,\phi 1H}$ to be $\frac{2t_c}{9} - 30$ ns.
2. Change minimum limit for $t_{\phi 2H,SSL}$ to be $\frac{6t_c}{9} - 50$ ns.</td></tr>
<tr><td>Example:
SN74LS424 (TIM8224)</td><td>1. Change minimum limit for $t_{\phi 2L,\phi 1H}$ from 86 ns to 70 ns.
2. Change minimum limit for $t_{\phi 2H,SSL}$ from 270 ns to 250 ns.</td></tr>
<tr><td>7-513</td><td>Figure 6:
SN74LS424 (TIM8224)</td><td>Add applications information shown below.
CRYSTAL REQUIREMENTS
Frequency tolerance: ±0.005% for 0°C to 70°C
Resonance Mode: series, fundamental (use 3rd overtone mode with tank circuit
Load capacitance: 20 pF to 35 pF
Equivalent resistance: 20 Ω to 75 Ω
Minimum power dissipation: 4 mW</td></tr>
<tr><td>7-529</td><td>Switching characteristics:
'LS670</td><td>1. Change table as shown below for the bottom four parameters.
<table>
<tr><td>t_{PZH}</td><td rowspan="4">Read enable</td><td rowspan="4">Any Q</td><td>C_L = 15 pF, R_L = 2 kΩ,
See Figures 1 and 4</td></tr>
<tr><td>t_{PZL}</td></tr>
<tr><td>t_{PHZ}</td><td rowspan="2">C_L = 5 pF, R_L = 2 kΩ,
See Figures 1 and 4</td></tr>
<tr><td>t_{PLZ}</td></tr>
</table>
2. Change enable time and disable time symbols shown below for definitions.
<table>
<tr><th>from</th><th>to</th></tr>
<tr><td>t_{ZH}</td><td>t_{PZH}</td></tr>
<tr><td>t_{ZL}</td><td>t_{PZL}</td></tr>
<tr><td>t_{HZ}</td><td>t_{PHZ}</td></tr>
<tr><td>t_{LZ}</td><td>t_{PLZ}</td></tr>
</table></td></tr>
</table>

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PAGE	LOCATION: AFFECTED TYPES	CHANGE
1-3 thru 1-8	Alphanumeric Index	See updated Alphanumeric Index starting on page 6 of this Supplement.
1-9 thru 1-28 and partially repeated 7-3 thru 7-14	Functional Index and Selection Guide	1. Delete the following type numbers and all data peculiar to them: 'LS124, 'LS208, 'LS302, 'LS327 'LS168A, 'S208, 'LS314, SN74LS362 'LS200A, 'LS214, 'S314, 'LS363 'S200A, 'S214, 'LS315, 'LS364 'LS202, 'LS215, 'LS324, SN74LS424 'LS207, 'LS300A, 'LS325, TIM8224 'S207, 'S300A, 'LS326, TIM9904 2. Add suffix A to the 'LS173. 3. For possible changes in selection data, see individual data sheet revisions.
3-6	Negative-going threshold voltage, V_{T-} Positive-going threshold voltage, V_{T+}	Delete "transition-operated" and change "a" to "an." Delete "transition-operated" and change "a" to "an."
4-10 and 4-11	W ceramic flat package drawings and notes	Delete "(see Note e)" twice in each drawing, and delete Notes e and f.
5-17	52	Change SN54H42(W) to SN54H52(W)
5-22	(*) Note	Change note to read, "*This configuration is nonstable; that is, it will not persist when preset or clear input returns to its inactive (high) level. Furthermore, in this configuration the output levels of the 'LS74A are not guaranteed to meet the minimum limits for V_{OH} if the low-level voltages at preset and clear are near V_{IL} maximum."
5-23	75	In the pin assignment drawing, pin 6 should be 3D and pin 10 should be 3Q. Relabel the D and Q inside the block to agree.
5-31	Upper box	This box should be labeled 101 near the upper left corner.
5-35 and 5-36	121, 122, and 123	In the function tables, under Q and $\overline{Q}$, add an asterisk (*) after each L and H on the second, third, and fourth lines (121 and 122), and on the second and third lines (123), and add the following note at the bottom of each page: "*These lines of the function table assume that the indicated steady-state conditions at the A and B inputs have been setup long enough for any pulse started before the setup to have been completed."
5-38	136	Add to the title: WITH OPEN-COLLECTOR OUTPUTS
5-39	138	Change title to read: 3-TO 8-LINE DECODERS/DEMULTIPLEXERS
	139	Change title to read: 2-TO 4-LINE DECODERS/DEMULTIPLEXERS
5-45	168	Delete SN54LS168A (J,W) SN74LS168A (J,N)
5-46	173	Add suffix A to SN54LS173 and SN74LS173.
5-52	200, 202	Delete these blocks and all information contained therein.
5-53	207, 208, 214, 215	
5-55	243	TRANSCEIVERS misspelled
5-60	276	After the words COMMON DIRECT CLEAR add AND PRESET

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PAGE	LOCATION: AFFECTED TYPES	CHANGE
5-61	280	The bracket and the word OUTPUT below pins 4 and 5 in pin assignment drawing should be below pins 5 and 6.
5-64	300, 302	Delete these blocks and all information contained therein.
5-65	314, 315, 324	
5-66	325, 326, 327	
5-67	362	
5-68	363, 364	
5-69	370, 371	Delete "See Bipolar Microcomputer Components Data Book, LCC4270" two places.
5-74	424	Delete this block and all information contained therein.
	425	Change ACTIVE-HIGH ENABLING to ACTIVE-LOW ENABLING
5-75	426	Change ACTIVE-LOW ENABLING to ACTIVE-HIGH ENABLING
5-76	481	Delete "SN54S481 (J)", add "SN74LS481 (J)".
6-5	Supply current: 'H01	Change I_{CCH} typical from 6.8 mA to 10 mA, and I_{CCH} maximum from 10 mA to 16.8 mA.
	Supply current: 'H22	Change I_{CCH} typical from 3.4 mA to 5 mA, and I_{CCH} maximum from 5 mA to 8.4 mA.
6-9	Switching characteristics: '02	Change t_{PLH} from 15 ns to 22 ns maximum.
6-10	Electrical characteristics: 'H11, 'H21	Change I_I maximum from 0.1 mA to 1 mA.
6-14	Electrical characteristics: 'LS13, 'LS14, 'LS132	Change V_{IK} maximum from 1.5 V to −1.5 V.
6-26	Electrical characteristics	In test conditions for V_{IK}, change I_I = § to I_I = @18 mA, and below the table delete § and the note that follows it.
6-28	Recommended operating conditions: 'S32	For the 54 Family, change V_{CC} maximum from 5.25 V to 5.5 V.
6-30	Electrical characteristics	Under test conditions for V_{OH}, swap "54 Family" and "74 Family."
6-33	Electrical characteristics: 'LS125A, 'LS126A	Change V_{IK} maximum from 1.5 V to −1.5 V.
6-34	Schematics: '125, '126	In titles under schematics, delete "A" after '125 and '126.
6-56	Recommended operating conditions: 'LS74A	Change minimum setup time for high-level data from 25 ns to 20 ns.
	Recommended operating conditions: 'LS109	1. Change minimum setup time for high-level data from 20 ns to 35 ns. 2. Change minimum setup time for low-level data from 20 ns to 25 ns.
	Electrical characteristics: 54LS/74LS flip-flops	Under test conditions for I_{OS} refer to the following note and add the note below to the table: For certain devices where state commutation can be caused by the shorting of an output to ground, an equivalent test will be performed with V_O = 2.25 V and 2.125 V for the 54 Family and 74 Family, respectively, with the minimum and maximum limits reduced to one-half of their stated values.
6-57	Schematics of inputs and outputs: 'LS107A	To the type numbers immediately over the boxes labeled EQUIVALENT OF EACH INPUT and TYPICAL OF ALL OUTPUTS, add 'LS107A.
6-60	Recommended operating conditions: 'LS279	Change supply voltage, V_{CC} for the 74 Family from 4.5 V to 4.75 V.
	Electrical characteristics: '279, 'LS279	In the test conditions for V_{IK}, change V_{CC} = MAX to V_{CC} = MIN.

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<table>
<tr><th>PAGE</th><th>LOCATION:
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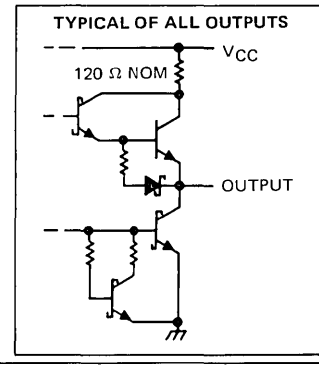
<tr><td>6-84</td><td>Electrical characteristics:
'LS240, 'LS241, 'LS244</td><td>For I_{CC}, outputs high, change the typical values from 13 mA to 17 mA, two places, and the maximum values from 23 mA to 27 mA, two places.</td></tr>
<tr><td>6-85</td><td>Recommended operating conditions: 'S240, 'S241</td><td>Add new parameter: "External resistance between any input or V_{CC} and ground" with a maximum limit of 40 kΩ in two places.</td></tr>
<tr><td>6-88</td><td>Electrical characteristics:
'LS242, 'LS243</td><td>1. Test conditions for A inputs, change "$\overline{G}$AB and GBA at V_{IL} max" to "$\overline{G}$AB and GBA at 0 V.
2. Test conditions for B inputs, change "$\overline{G}$AB and GBA at 2 V" to "$\overline{G}$AB and GBA at 4.5 V.</td></tr>
<tr><td rowspan="2">6-96</td><td>Figure 13</td><td>Five inputs on left side should be tied to 4.5 V (instead of ground).</td></tr>
<tr><td>Figure 14</td><td>Five inputs on left side should be tied to ground (instead of 4.5 V).</td></tr>
<tr><td>7-28</td><td>Electrical characteristics:
'46A, '47A</td><td>Test conditions for $V_{O(on)}$, change V_{CC} = MAX to V_{CC} = MIN.</td></tr>
<tr><td>7-29</td><td>Electrical characteristics:
'L46, 'L47</td><td>Test conditions for $V_{O(on)}$, change V_{CC} = MAX to V_{CC} = MIN.</td></tr>
<tr><td>7-30</td><td>Electrical characteristics:
'LS47</td><td>Test conditions for $V_{O(on)}$, change V_{CC} = MAX to V_{CC} = MIN.</td></tr>
<tr><td>7-39</td><td>Recommended operating conditions: 'LS75, 'LS77</td><td>Change maximum limit for Hold time, t_h from 0 ns to 5 ns two places.</td></tr>
<tr><td>7-62</td><td>Electrical characteristics:
SN74LS85</td><td>Change the V_{IL} maximum limit from 0.8 V to 0.7 V</td></tr>
<tr><td>7-68</td><td>Electrical characteristics:
'LS86</td><td>Test conditions for V_{OL}, "V_{IL} = V_{IL} mas" should be "V_{IL} = V_{IL} max"</td></tr>
<tr><td>7-93</td><td>Recommended operating conditions: 'LS95B</td><td>Change minimum width of clock pulse from 25 ns to 20 ns two places.</td></tr>
<tr><td>7-123 thru 7-128</td><td>'LS124</td><td>Delete all references, specifications, schematics, etc., pertaining to the SN54LS124 and SN74LS124.</td></tr>
<tr><td>7-136</td><td>Electrical characteristics:
'LS138, 'LS139</td><td>For I_{OS}, specify different limits for 'LS138 and 'LS139
<table>
<tr><th colspan="2" rowspan="2"></th><th colspan="3">SN54LS138
SN54LS139</th><th colspan="3">SN74LS138
SN74LS139</th></tr>
<tr><th>MIN</th><th>TYP</th><th>MAX</th><th>MIN</th><th>TYP</th><th>MAX</th></tr>
<tr><td rowspan="2">I_{OS}</td><td>'LS138</td><td>−20</td><td>−100</td><td></td><td>−20</td><td>−100</td><td></td></tr>
<tr><td>'LS139</td><td>−6</td><td>−40</td><td></td><td>−5</td><td>−42</td><td></td></tr>
</table></td></tr>
<tr><td>7-137</td><td>Recommended operating conditions 'S138, 'S139</td><td>Change type number under SN54S138 from "SN74S139" to "SN54S139."</td></tr>
<tr><td>7-153</td><td>Output schematic:
'LS147, 'LS148</td><td>Add a Schottky diode as shown.
 
</td></tr>
</table>

<table>
<tr><th>PAGE</th><th>LOCATION:
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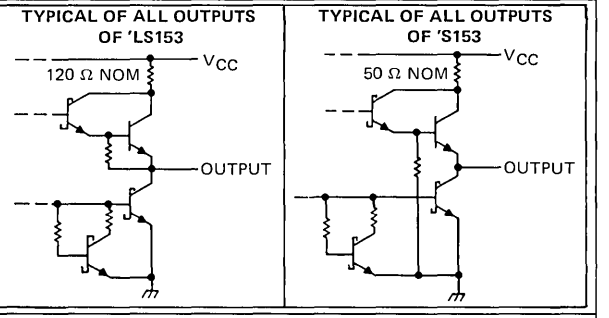
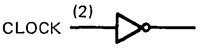
<tr><td>7-154

7-155</td><td>Switching characteristics:
'148

Switching characteristics:
'LS148</td><td>First four parameters (measured to A0,A1, or A2 output), change FROM (INPUT) from "0 thru 7" to "1 thru 7."
<table>
<tr><th>PARAMETER</th><th>FROM (INPUT)</th><th>TO (OUTPUT)</th><th>WAVEFORM</th></tr>
<tr><td>t_{PLH}</td><td rowspan="2">1 to 7</td><td rowspan="2">A0, A1, or A2</td><td rowspan="2">In-phase output</td></tr>
<tr><td>t_{PHL}</td></tr>
<tr><td>t_{PLH}</td><td rowspan="2">1 to 7</td><td rowspan="2">A0, A1, or A2</td><td rowspan="2">Out-of-phase output</td></tr>
<tr><td>t_{PHL}</td></tr>
</table></td></tr>
<tr><td>7-160</td><td>Switching characteristics:
'150</td><td>In the '150 column, the limits on the last line should be swapped with those on the line immediately above it.
<table>
<tr><th>PARAMETER</th><th>FROM (INPUT)</th><th>TO (OUTPUT)</th><th>MIN</th><th>TYP</th><th>MAX</th></tr>
<tr><td>t_{PLH}</td><td rowspan="2">E0 thru E15, or D0 thru D7</td><td rowspan="2">W</td><td></td><td>8.5</td><td>14</td></tr>
<tr><td>t_{PHL}</td><td></td><td>13</td><td>20</td></tr>
</table></td></tr>
<tr><td>7-166</td><td>Output schematic:
'LS153, 'S153</td><td>Replace block entitled "TYPICAL OF OUTPUTS OF 'LS153, 'S153" with two blocks as shown.

</td></tr>
<tr><td>7-176</td><td>Absolute maximum ratings: '155, '156, 'LS155, 'LS156</td><td colspan="2">After the words "Off-state output voltage:", change '155 and LS155 to '156 and 'LS156, respectively.</td></tr>
<tr><td>7-186</td><td>Electrical characteristics:
'LS158</td><td>Add another ICC parameter as shown
<table>
<tr><th colspan="4" rowspan="2">TEST CONDITIONS</th><th colspan="3">SN54LS'</th><th colspan="3">SN74LS'</th></tr>
<tr><th>MIN</th><th>TYP</th><th>MAX</th><th>MIN</th><th>TYP</th><th>MAX</th></tr>
<tr><td rowspan="3">I_{CC}</td><td rowspan="3">V_{CC}=MAX</td><td>See Note 2</td><td>'LS157</td><td></td><td>9.7</td><td>16</td><td></td><td>9.7</td><td>16</td></tr>
<tr><td>See Note 2</td><td>'LS158</td><td></td><td>4.8</td><td>8</td><td></td><td>4.8</td><td>8</td></tr>
<tr><td>All A inputs at 4.5 V, All other inputs at 0 V</td><td>'LS158</td><td></td><td>6.5</td><td>11</td><td></td><td>6.5</td><td>11</td></tr>
</table></td></tr>
<tr><td></td><td>Switching characteristics:
'LS158</td><td>1. t_{PHL} from data inputs, change the typical from 7 ns to 10 ns, and the maximum from 12 ns to 15 ns.
2. t_{PHL} from strobe, change the typical from 12 ns to 18 ns, and the maximum from 18 ns to 24 ns.</td></tr>
<tr><td>7-192</td><td>Functional block diagram: 'LS160A, 'LS162A</td><td>The clock input buffer should have an inversion indicator like the one for the 'LS163A.

</td></tr>
<tr><td>7-200</td><td>Input schematic:
'S162, 'S163</td><td colspan="2">Change (OPEN FOR CLOCK AND LOAD INPUTS) to (OPEN FOR CLOCK AND DATA INPUTS).</td></tr>
<tr><td>7-201</td><td>Electrical characteristics:
'S162, 'S163</td><td>Change I_{IH} as shown
<table>
<tr><th colspan="2" rowspan="2"></th><th colspan="3">SN54S162
SN54S163</th><th colspan="3">SN74S162
SN74S163</th></tr>
<tr><th>MIN</th><th>TYP</th><th>MAX</th><th>MIN</th><th>TYP</th><th>MAX</th></tr>
<tr><td rowspan="2">I_{IH}</td><td>Clock and data</td><td></td><td></td><td>50</td><td></td><td></td><td>50</td></tr>
<tr><td>Other inputs</td><td></td><td>−10</td><td>−200</td><td></td><td>−10</td><td>−200</td></tr>
</table></td></tr>
</table>

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<table>
<tr><th>PAGE</th><th>LOCATION:
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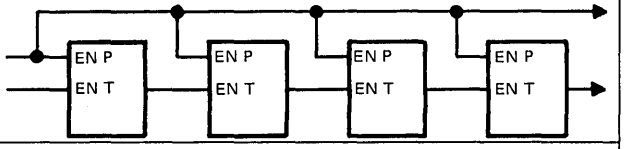
<tr><td>7-205</td><td>Typical application data: '160 thru '163, 'LS160A thru 'LS163A, 'S162, 'S163</td><td>Connections to EN P and EN T inputs of first two counters from the left should be changed as shown.
  </td></tr>
<tr><td>7-220</td><td>Recommended operating conditions: 'LS166</td><td>1. Width of clock or clear pulse, t_w, change minimum from 20 ns to 30 ns two places.
2. Hold time at any input, t_h, change minimum from 0 ns to 15 ns two places.</td></tr>
<tr><td>7-226 thru 7-236</td><td>'LS168A</td><td>Delete all references, specifications, diagrams, etc., pertaining to the SN54LS168A and SN74LS168A.</td></tr>
<tr><td>7-234</td><td>Electrical characteristics: 'S168, 'S169</td><td>Add separate I_{IH} limits for the Load input.
<table>
<tr><th colspan="2" rowspan="2"></th><th colspan="3">SN54S168
SN54S169</th><th colspan="3">SN74S168
SN74S169</th></tr>
<tr><th>MIN</th><th>TYP</th><th>MAX</th><th>MIN</th><th>TYP</th><th>MAX</th></tr>
<tr><td rowspan="3">I_{IH}</td><td>Load</td><td>−10</td><td></td><td>−200</td><td>−10</td><td></td><td>−200</td></tr>
<tr><td>Enable $\overline{T}$</td><td></td><td></td><td>100</td><td></td><td></td><td>100</td></tr>
<tr><td>Other inputs</td><td></td><td></td><td>50</td><td></td><td></td><td>50</td></tr>
</table></td></tr>
<tr><td>7-242</td><td>Electrical characteristics: 'LS170</td><td>Change I_{OH} maximum limit from 20 μA to 100 μA two places.</td></tr>
<tr><td>7-249</td><td>'LS173</td><td>1. Add suffix A to 'LS173 twice in the headliner, twice over the pin assignments drawing, in the small table to the left of the pin assignments drawing, in the first, ninth, and 13th lines of the first paragraph of the description, and on the first line of the second paragraph of the description.
2. In the small table to the left of the pin assignments drawing, change the typical power dissipation from 85 mW to 95 mW.</td></tr>
<tr><td>7-250</td><td>'LS173</td><td>Add suffix A to 'LS173 twice in the headliner, three times in the absolute maximum ratings table, and once between the second and third schematics.</td></tr>
<tr><td>7-252</td><td>'LS173</td><td>1. Add suffix A to 'LS173 twice in the headliner, twice in the recommended operating conditions table, and twice in the electrical characteristics table.
2. In the recommended operating conditions, change the setup time for data enable from 17 ns minimum to 35 ns minimum.
3. In the switching characteristics, change the limits column to be:
4. Delete DESIGN GOAL note at the bottom of the page.
<table>
<tr><th>MIN</th><th>TYP</th><th>MAX</th></tr>
<tr><td>30</td><td>50</td><td></td></tr>
<tr><td></td><td>26</td><td>35</td></tr>
<tr><td></td><td>17</td><td>25</td></tr>
<tr><td></td><td>22</td><td>30</td></tr>
<tr><td></td><td>15</td><td>23</td></tr>
<tr><td></td><td>18</td><td>27</td></tr>
<tr><td></td><td>11</td><td>17</td></tr>
<tr><td></td><td>11</td><td>17</td></tr>
</table></td></tr>
<tr><td>7-257</td><td>Switching characteristics: 'LS174, 'LS175</td><td>Make two columns of limits:
<table>
<tr><th colspan="3">'LS174</th><th colspan="3">'LS175</th></tr>
<tr><th>MIN</th><th>TYP</th><th>MAX</th><th>MIN</th><th>TYP</th><th>MAX</th></tr>
<tr><td>30</td><td>40</td><td></td><td>30</td><td>40</td><td></td></tr>
<tr><td></td><td></td><td></td><td></td><td>20</td><td>30</td></tr>
<tr><td></td><td>23</td><td>35</td><td></td><td>20</td><td>30</td></tr>
<tr><td></td><td>20</td><td>30</td><td></td><td>13</td><td>25</td></tr>
<tr><td></td><td>21</td><td>30</td><td></td><td>16</td><td>25</td></tr>
</table></td></tr>
</table>

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<table>
<tr><th>PAGE</th><th>LOCATION:
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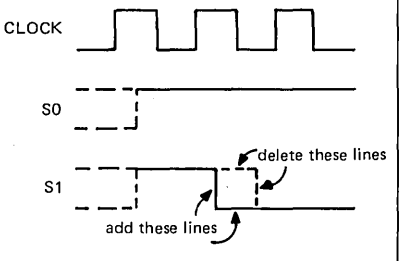
<tr><td>7-293</td><td>Switching characteristics:
'184, '185A</td><td>1. Change C_L = 15 pF to C_L = 30 pF.
2. Change R_{L1} = 400 Ω to R_{L1} = 300 Ω.</td></tr>
<tr><td rowspan="2">7-296</td><td>Pin assignment drawing:
'190, '191, 'LS190,
'LS191</td><td>1. Below ENABLE under pin 4 delete G.
2. Inside the block above pin 4 change G to CTEN.</td></tr>
<tr><td>Description</td><td>Delete the last sentence of the second paragraph, "Level changes at the down/up input . . . when the clock input is high" and replace with the following:
A false clock may occur if the down/up input changes while the clock is low. A false ripple carry may occur if both the clock and enable are low and the down/up input is high during a load pulse.</td></tr>
<tr><td>7-297</td><td>Functional block diagrams</td><td>Delete the G after ENABLE in both block diagrams.</td></tr>
<tr><td>7-302</td><td>Recommended operating conditions: 'LS190, 'LS191</td><td>Change the minimum data hold time from 0 ns to 5 ns two places.</td></tr>
<tr><td>7-313</td><td>Recommended operating conditions: 'LS192, 'LS193</td><td>Change the minimum data hold time from 0 ns to 5 ns two places.</td></tr>
<tr><td>7-322</td><td>Electrical characteristics: 'S194</td><td>Test conditions for I_{IL} change V_I = 0.4 V to V_I = 0.5 V.</td></tr>
<tr><td>7-341</td><td>Typical sequences: '198</td><td>Change waveforms as shown:
 
</td></tr>
<tr><td>7-346</td><td>Bus-management function table: 'S226</td><td>Replace with new table:
<table>
<tr><th colspan="2">MODE CONTROLS</th><th colspan="2">STROBES</th><th colspan="2">A-TO-B LATCHES</th><th colspan="2">B-TO-A LATCHES</th><th>OPERATION</th></tr>
<tr><th>S2</th><th>S1</th><th>GAB</th><th>GBA</th><th>1</th><th>2</th><th>1</th><th>2</th><th></th></tr>
<tr><td rowspan="2">L</td><td rowspan="2">L</td><td rowspan="2">X</td><td>L</td><td rowspan="2">Latch</td><td rowspan="2">Trans</td><td>Trans</td><td>Trans</td><td>Pass B to A</td></tr>
<tr><td>H</td><td>Latch</td><td>Trans</td><td>Read out stored data</td></tr>
<tr><td>L</td><td>H</td><td>X</td><td>X</td><td>Latch</td><td>Trans</td><td>Latch</td><td>Trans</td><td>Read out stored data</td></tr>
<tr><td rowspan="2">H</td><td rowspan="2">L</td><td>L</td><td rowspan="2">X</td><td>Trans</td><td>Trans</td><td rowspan="2">Latch</td><td rowspan="2">Trans</td><td>Pass A to B</td></tr>
<tr><td>H</td><td>Latch</td><td>Trans</td><td>Read out stored data</td></tr>
<tr><td rowspan="2">H</td><td rowspan="2">H</td><td>L</td><td>L</td><td>Trans</td><td>Latch</td><td>Trans</td><td>Latch</td><td>Read in both buses</td></tr>
<tr><td>H</td><td>H</td><td>Latch</td><td>Latch</td><td>Latch</td><td>Latch</td><td>Store bus data</td></tr>
</table>
H=high level L=low level X=irrelevant Latch=latched Trans=transparent</td></tr>
</table>

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<table>
<tr><th>PAGE</th><th>LOCATION:
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<tr><td>7-347</td><td>Recommended operating conditions: 'S226</td><td>Replace data setup time and data hold time with the following:
<table>
<tr><th colspan="2">PARAMETER</th><th>MIN</th><th>TYP</th><th>MAX</th><th>MIN</th><th>TYP</th><th>MAX</th><th>UNIT</th></tr>
<tr><td colspan="2">Width of strobe pulse</td><td></td><td></td><td>30</td><td></td><td></td><td>20</td><td>ns</td></tr>
<tr><td rowspan="2">Setup time, t_{su}</td><td>To Strobe</td><td></td><td></td><td>30↑</td><td></td><td></td><td>20↑</td><td rowspan="2">ns</td></tr>
<tr><td>To Select</td><td></td><td></td><td>30</td><td></td><td></td><td>20</td></tr>
<tr><td rowspan="2">Hold time, t_h</td><td>To Strobe</td><td></td><td></td><td>0↑</td><td></td><td></td><td>0↑</td><td rowspan="2">ns</td></tr>
<tr><td>To Select</td><td></td><td></td><td>0</td><td></td><td></td><td>0</td></tr>
</table></td></tr>
<tr><td></td><td>Electrical characteristics: 'S226</td><td>1. Test conditions for V_{OL} change I_{OL} = 20 mA to I_{OL} = 15 mA.
2. Change I_{OZL} maximum limit from −100 μA to −250 μA.
3. Split I_{IL} into two lines as shown:
<table>
<tr><td rowspan="2">I_{IL} Low-level input current</td><td>OCAB, OCBA</td><td rowspan="2">V_{CC}=MAX, V_I=0.5 V</td><td>−0.38</td><td rowspan="2">mA</td></tr>
<tr><td>All other inputs</td><td>−1.6</td></tr>
</table></td></tr>
<tr><td>7-349</td><td>Absolute maximum ratings: 'LS245</td><td>Add rating "Off-state output voltage . . . 5.5 V"</td></tr>
<tr><td>7-350</td><td>Electrical characteristics: 'LS245</td><td>Change I_{OZH} maximum limit from 10 μA to 20 μA.</td></tr>
<tr><td>7-356</td><td>Electrical characteristics: '246, '247</td><td>Test conditions for $V_{O(on)}$ change V_{CC} = MAX to V_{CC} = MIN.</td></tr>
<tr><td>7-357</td><td>Electrical characteristics: 'LS247</td><td>Test conditions for $V_{O(on)}$ change V_{CC} = MAX to V_{CC} = MIN.</td></tr>
<tr><td>7-360</td><td>Electrical characteristics: '249</td><td>Test conditions for I_I change V_I = 7 V to V_I = 5.5 V.</td></tr>
<tr><td>7-370</td><td>Switching characteristics: 'LS253</td><td>Test conditions for t_{HZ} and t_{LZ} "C_L" missing. Should be "C_L = 5 pF."</td></tr>
<tr><td>7-375</td><td>Electrical characteristics: 'S257, 'S258</td><td>Change I_{OZH} maximum limit from 0.5 μA to 50 μA.</td></tr>
<tr><td>7-379</td><td>Recommended operating conditions: 'LS259 (TIM9906)</td><td>1. Change minimum hold time for data inputs from 0 ns to 5 ns two places.
2. Change minimum hold time for address inputs from 0 ns to 15 ns two places.</td></tr>
<tr><td>7-382</td><td>Electrical characteristics: SN54LS261</td><td>I_{CC} limits delete 22 from the minimum column and enter 20 in the typical column.</td></tr>
<tr><td>7-407</td><td>Switching characteristics: 'LS280</td><td>Test conditions add: Inputs not under test at 0 V.</td></tr>
<tr><td>7-408</td><td>Switching characteristics: 'S280</td><td>Test conditions change R_L = 180 Ω to R_L = 280 Ω.</td></tr>
<tr><td>7-411</td><td>Table 1: 'S281</td><td>For ALU selection HLH and C_n = L, change $\overline{F}_n = \overline{B}_n$ to $F_n = \overline{B}_n$.</td></tr>
<tr><td>7-419</td><td>Recommended operating conditions: SN74S283</td><td>Change maximum low-level output current for output C4 from 0 to 10.</td></tr>
<tr><td>7-430</td><td>Recommended operating conditions: 'LS295B</td><td>1. Change maximum clock frequency from 20 MHz to 30 MHz two places.
2. Change minimum width of clock pulse from 25 ns to 16 ns two places.</td></tr>
<tr><td>7-437</td><td>Features: 'LS299</td><td>Change guaranteed shift (clock) frequency for the 'LS299 from 35 MHz to 25 MHz.</td></tr>
</table>

REVISIONS TO THE FIRST AND SECOND PRINTINGS

<table>
<tr><th>PAGE</th><th>LOCATION:
AFFECTED TYPES</th><th>CHANGE</th></tr>
<tr><td>7-439</td><td>Absolute maximum ratings: 'LS299</td><td>Change the off-state output voltage from 7 V to 5.5 V.</td></tr>
<tr><td></td><td>Recommended operating conditions: 'LS299</td><td>1. Change the maximum clock frequency from 35 MHz to 25 MHz two places.
2. Change the minimum width of clock pulse for clock high from 20 ns to 30 ns two places.
3. Change the minimum width of clock pulse for clock low from 20 ns to 10 ns two places.
4. Change the minimum setup time for the select inputs from 10 ns to 35 ns two places.</td></tr>
<tr><td>7-440</td><td>Electrical characteristics: 'LS299</td><td>1. Change minimum V_{OH} for Q_A or Q_H output from 2.7 V to 2.5 V for SN54LS299 only.
2. Change I_{CC} typical value from 35 mA to 33 mA two places, and the maximum limit from 60 mA to 53 mA two places.</td></tr>
<tr><td></td><td>Switching characteristics: 'LS299</td><td>Change the limits column as shown.
<table>
<tr><th>MIN</th><th>TYP</th><th>MAX</th><th>UNIT</th></tr>
<tr><td>25</td><td>35</td><td></td><td>MHz</td></tr>
<tr><td></td><td>22</td><td>33</td><td rowspan="3">ns</td></tr>
<tr><td></td><td>26</td><td>39</td></tr>
<tr><td></td><td>27</td><td>40</td></tr>
<tr><td></td><td>17</td><td>25</td><td rowspan="2">ns</td></tr>
<tr><td></td><td>26</td><td>39</td></tr>
<tr><td></td><td>26</td><td>40</td><td>ns</td></tr>
<tr><td></td><td>13</td><td>21</td><td rowspan="2">ns</td></tr>
<tr><td></td><td>19</td><td>30</td></tr>
<tr><td></td><td>10</td><td>15</td><td rowspan="2">ns</td></tr>
<tr><td></td><td>10</td><td>15</td></tr>
</table></td></tr>
<tr><td>7-442</td><td>Electrical characteristics: 'S299</td><td>Add an additional line for I_{IL} for S0, S1:
<table>
<tr><td rowspan="3">I_{IL}</td><td>Clock or clear</td><td rowspan="3">V_{CC} = MAX, V_I = 0.5 V</td><td>−2</td><td>mA</td></tr>
<tr><td>S0, S1</td><td>−400</td><td rowspan="2">μA</td></tr>
<tr><td>Any other</td><td>−250</td></tr>
</table></td></tr>
<tr><td>7-443</td><td>'LS323</td><td>1. Seventh feature, change guaranteed shift (clock) frequency from 35 MHz to 25 MHz.
2. Delete DESIGN GOAL note at bottom of page.</td></tr>
<tr><td>7-444</td><td>Switching characteristics: 'LS323</td><td>1. Change limits column to be:
<table>
<tr><th>MIN</th><th>TYP</th><th>MAX</th></tr>
<tr><td>25</td><td>35</td><td></td></tr>
<tr><td></td><td>22</td><td>33</td></tr>
<tr><td></td><td>26</td><td>39</td></tr>
<tr><td></td><td>17</td><td>25</td></tr>
<tr><td></td><td>25</td><td>39</td></tr>
<tr><td></td><td>14</td><td>21</td></tr>
<tr><td></td><td>20</td><td>30</td></tr>
<tr><td></td><td>10</td><td>15</td></tr>
<tr><td></td><td>10</td><td>15</td></tr>
</table></td></tr>
<tr><td></td><td></td><td>2. Delete DESIGN GOAL note at bottom of page.</td></tr>
<tr><td>7-445 thru 7-447</td><td>Entire data sheet: 'LS324 thru 'LS327</td><td>Delete completely.</td></tr>
<tr><td>7-450</td><td>Switching characteristics: 'LS348 (TIM 9908)</td><td>In the "FROM (INPUT)" column, change the first two entries from "0 thru 7" to "1 thru 7".</td></tr>
<tr><td>7-460 thru 7-466</td><td>Entire data sheet: 'LS362 (TIM9904)</td><td>Delete completely. This product now being marketed exclusively by MOS Microprocessor Division.</td></tr>
<tr><td>7-467 thru 7-470</td><td>Entire data sheet: 'LS363, 'LS364</td><td>Delete completely.</td></tr>
</table>

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REVISIONS TO THE FIRST AND SECOND PRINTINGS

<table>
<tr><th>PAGE</th><th>LOCATION:
AFFECTED TYPES</th><th>CHANGE</th></tr>
<tr><td rowspan="3">7-473</td><td>Schematics: 'LS373</td><td>1. Change title first block to EQUIVALENT OF DATA INPUTS.
2. In first block, replace "R_{eq}" with "20 kΩ NOM", and delete the two lines of type below the schematic.
3. Change title of middle block to EQUIVALENT OF ENABLE AND OUTPUT CONTROL INPUTS.</td></tr>
<tr><td>Schematics: 'LS374</td><td>1. Delete entire block labeled EQUIVALENT OF OUTPUT CONTROL INPUT.
2. Change title of block labeled EQUIVALENT OF CLOCK INPUT to EQUIVALENT OF CLOCK AND OUTPUT CONTROL INPUTS.</td></tr>
<tr><td>Recommended operating conditions: 'LS373</td><td>1. Change minimum data setup time from 0 ns to 5 ns two places.
2. Change minimum data hold time from 10 ns to 20 ns two places.</td></tr>
<tr><td>7-475</td><td>'S373, 'S374</td><td>Delete TENTATIVE DATA note at bottom of page.</td></tr>
<tr><td rowspan="2">7-476</td><td>Switching characteristics: 'S373</td><td>1. Change the values for t_{PLH} from data inputs from 5 ns to 7 ns typical, and from 9 ns to 12 ns maximum.
2. Change the values for t_{PHL} from data inputs from 9 ns to 7 ns typical, and from 13 ns to 12 ns maximum.</td></tr>
<tr><td>'S473, 'S474</td><td>Delete the TENTATIVE DATA note at bottom of page.</td></tr>
<tr><td>7-485</td><td>Functional block diagram: 'S381</td><td>The line from C_n input is shown as an input to the NAND gate at the $\overline{P}$ output, but it should not be connected to this gate.</td></tr>
<tr><td rowspan="3">7-494</td><td>Recommended operating conditions: 'LS390, 'LS393</td><td>1. Change count frequency maximum limit for the B input from 20 MHz to 12.5 MHz two places.
2. Change pulse width minimum limit for the B input high or low from 25 ns to 40 ns two places.</td></tr>
<tr><td rowspan="2">Electrical characteristics: 'LS390, 'LS393</td><td>1. Change I_{IH} maximum limit for input A from 40 μA to 100 μA two places.
2. Change I_{IH} maximum limit for input B from 80 μA to 200 μA two places.</td></tr>
<tr><td>Delete TENTATIVE DATA note at bottom of the page.</td></tr>
<tr><td rowspan="2">7-495</td><td rowspan="2">Switching characteristics: 'LS390</td><td>Change f_{max} for B input from 20 MHz to 12.5 MHz minimum, and from 30 MHz to 20 MHz typical.</td></tr>
<tr><td>Delete TENTATIVE DATA note at bottom of the page.</td></tr>
<tr><td>7-497</td><td>Recommended operating conditions: 'LS395A</td><td>1. Change maximum clock frequency from 25 MHz to 30 MHz two places.
2. Change minimum width of clock pulse from 25 ns to 16 ns two places.
3. Replace line for setup time with two lines as shown:
<table>
<tr><th></th><th></th><th>MIN</th><th>NOM</th><th>MAX</th><th>MIN</th><th>NOM</th><th>MAX</th><th>UNIT</th></tr>
<tr><td rowspan="2">Setup time, high-level or low-level data, t_{su}</td><td>Load/shift input</td><td>40</td><td></td><td></td><td>40</td><td></td><td></td><td rowspan="2">ns</td></tr>
<tr><td>All other inputs</td><td>20</td><td></td><td></td><td>20</td><td></td><td></td></tr>
</table></td></tr>
<tr><td>7-501</td><td>Recommended operating conditions: 'LS398, 'LS399</td><td>1. Change minimum setup time (Data) from 20 to 25 ns two places.
2. Change minimum setup time (Word select) from 25 to 45 ns two places.</td></tr>
<tr><td>7-505</td><td>Electrical characteristics: SN54S412</td><td>Change V_{OH} minimum limit from 3.65 V to 3.4 V for SN54S412 only.</td></tr>
<tr><td>7-507 thru 7-513</td><td>Entire data sheet: SN74LS424 (TIM8224)</td><td>Delete completely.</td></tr>
<tr><td>7-514</td><td>SN74S428 (TIM8228), SN74S438 (TIM8238)</td><td>Delete TENTATIVE DATA SHEET note at bottom of page.</td></tr>
<tr><td>7-519</td><td>Typical application data</td><td>1. At the control bus, the bottom label inside the bracket (from pin 27), change I/OR to I/OW.
2. Delete "SN74LS424" from CLOCK GENERATOR DRIVER block. Leave TIM 8224.</td></tr>
</table>

PAGE	LOCATION: AFFECTED TYPES	CHANGE
7-524	Electrical characteristics: 'LS490	1. Test conditions for V_{IK} change I_I = −1 mA to I_I = −18 mA. 2. Change I_{IH} maximum limit for clock input from 40 μA to 100 μA two places.
	'LS490	Delete TENTATIVE DATA note at the bottom of the page.
7-525	'LS490	Delete TENTATIVE DATA note at the bottom of the page.
7-526	Description: 'LS670	Next-to-last sentence of next-to-last paragraph should start, "Up to 128 of these . . .
7-528	Recommended operating conditions: 'LS670	For hold times change $t_{h(W)}$ to $t_{h(D)}$ and $t_{h(D)}$ to $t_{h(W)}$.
7-529	Electrical characteristics: 'LS670	Test conditions for I_{IL} add: V_I = 0.4 V.
8-7		Add an "A" suffix to each circuit type listed as shown below: 54151A 54LS73A 54LS74A 54LS76A 54LS107A 54LS109A 54LS112A 54LS113A 54LS114A 54LS160A 54LS161A 54LS162A 54LS163A 54LS169A 54LS194A 54LS195A 54LS257A 54LS258A
	Right-hand column: SN54LS124, SN54LS168	Delete 54LS124 and SN54LS168
8-8	Center column: 4000A thru 4050A	Delete "CMOS" and the subheadings and thirty type numbers that follow them.

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Chip Carrier Information and Planned New Products

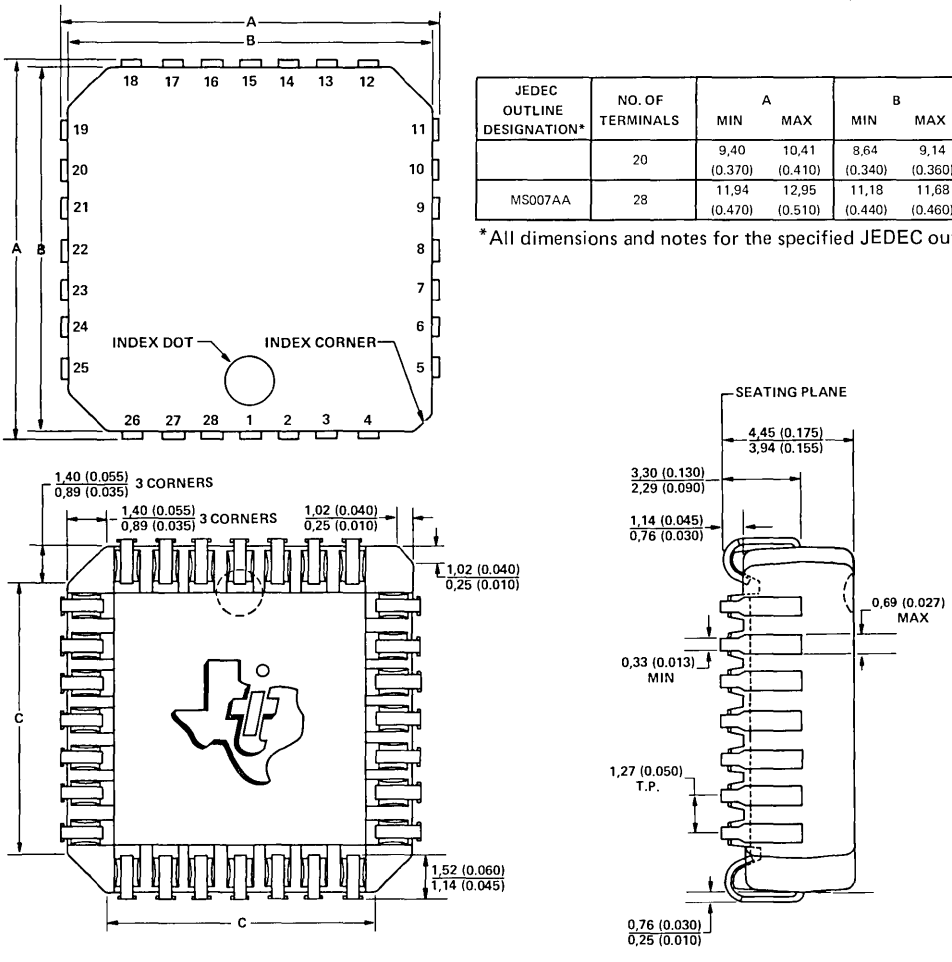
FN plastic chip carrier package

Each of these chip carrier packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound withstands soldering temperatures with no deformation, and circuit performance characteristics remain stable when the devices are operated in high-humidity conditions. The packages are intended for surface mounting on solder lands on 0.050-inch centers. Leads require no additional cleaning or processing when used in soldered assembly.

The following bipolar digital device families will be offered in these plastic chip carrier packages: Advanced Schottky and Advanced Low-Power Schottky, all bipolar PROMS, some Schottky and some Low-Power Schottky.

Products in design will be offered in 44-lead (MS007AB), 52-lead (MS007AC), and 68-lead (MS007AD) packages.

FN PLASTIC CHIP CARRIER PACKAGE
(28-terminal package shown)



JEDEC OUTLINE DESIGNATION*	NO. OF TERMINALS	A MIN	A MAX	B MIN	B MAX	C MIN	C MAX
	20	9,40 (0.370)	10,41 (0.410)	8,64 (0.340)	9,14 (0.360)	6,35 (0.250)	6,48 (0.255)
MS007AA	28	11,94 (0.470)	12,95 (0.510)	11,18 (0.440)	11,68 (0.460)	8,76 (0.345)	9,02 (0.355)

*All dimensions and notes for the specified JEDEC outline apply.

NOTE: Dimensions are in millimeters and (inches).

FC and FD ceramic chip carrier packages

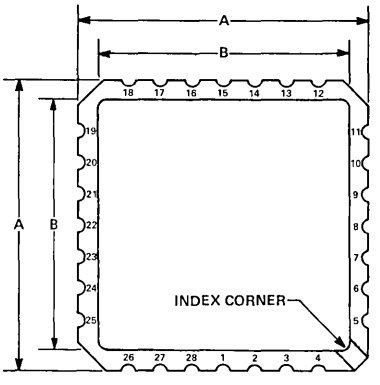
Both versions of these hermetically sealed chip carrier packages have ceramic bases. The FC package has a single-layer base with a ceramic lid and glass seal. The FD package has a three-layer base with either a metal lid and braze seal or a ceramic lid and glass seal, at the option of Texas Instruments.

The packages are intended for surface mounting on solder lands on 0.050-inch centers. Terminals require no additional cleaning or processing when used in soldered assembly.

The full-military-temperature-range versions of the following bipolar digital device families will be offered in these or similar ceramic chip carrier packages: Advanced Low-Power Schottky, PROMs and RAMs, and certain memory support functions (i.e., 'S225, 184A, 185, 284, 285 and 'LS630).

Products in design will be offered in 44-terminal (MS004CD), 52-terminal (MS004CE), 68-terminal (MS004CF), and 84-terminal (MS004CG) packages.

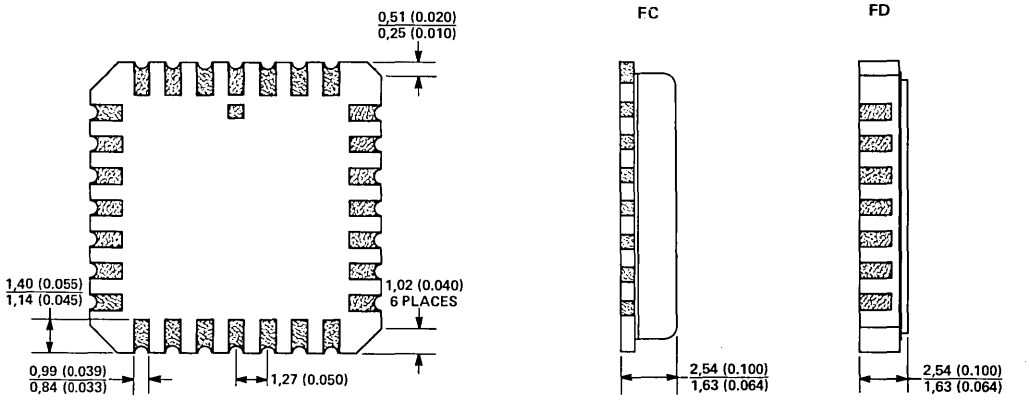
FC AND FD CERAMIC CHIP CARRIER PACKAGE
(28-terminal package shown)



CERAMIC CHIP CARRIERS

JEDEC OUTLINE DESIGNATION*	NUMBER OF TERMINALS	A MIN	A MAX	B MIN	B MAX
MS004CB	20	8,687 (0.342)	9,093 (0.358)	7,798 (0.307)	9,093 (0.358)
MS004CC	28	11,227 (0.442)	11,633 (0.458)	10,312 (0.406)	11,633 (0.458)

*All dimensions and notes for the specified JEDEC outline apply.



All dimensions are in millimeters and parenthetically in inches.

CHIP CARRIER TERMINAL ASSIGNMENT FOR ADVANCED NEW PRODUCTS

'ALS00	'ALS01 'ALS02	'ALS03	'ALS04, 'ALS05	'ALS08, 'ALS09	'ALS10, 'ALS11, 'ALS12, 'ALS15	'ALS20, 'ALS21, 'ALS22
1. nc	1. nc	1. nc	1. 1A	1. nc	1. 1A	1. nc
2. nc	2. 1Y	2. nc	2. nc	2. nc	2. nc	2. nc
3. 1A	3. nc	3. 1A	3. nc	3. 1A	3. nc	3. 1A
4. 1B	4. 1A	4. 1B	4. 1Y	4. 1B	4. 1B	4. nc
5. 1Y	5. 1B	5. 1Y	5. 2A	5. 1Y	5. 2A	5. 1B
6. 2A	6. 2Y	6. 2A	6. 2Y	6. 2A	6. 2B	6. 1C
7. 2B	7. 2A	7. 2B	7. 3A	7. 2B	7. 2C	7. 1D
8. nc	8. nc	8. nc	8. nc	8. nc	8. nc	8. nc
9. 2Y	9. 2B	9. 2Y	9. 3Y	9. 2Y	9. 2Y	9. 1Y
10. GND	10. GND	10. GND	10. GND	10. GND	10. GND	10. GND
11. 3Y	11. 3A	11. 3Y	11. nc	11. 3Y	11. nc	11. nc
12. nc	12. nc	12. nc	12. 4Y	12. nc	12. 3Y	12. 2Y
13. 3A	13. 3B	13. 3A	13. nc	13. 3A	13. nc	13. nc
14. nc	14. nc	14. nc	14. 4A	14. nc	14. nc	14. nc
15. 3B	15. 3Y	15. 3B	15. 5Y	15. 3B	15. 3A	15. 2A
16. 4Y	16. 4A	16. 4Y	16. 5A	16. 4Y	16. 3B	16. 2B
17. nc	17. 4B	17. nc	17. 6Y	17. nc	17. 3C	17. 2C
18. 4A	18. nc	18. 4A	18. nc	18. 4A	18. 1Y	18. nc
19. 4B	19. 4Y	19. 4B	19. 6A	19. 4B	19. 1C	19. 2D
20. V_{CC}	20. V_{CC}	20. V_{CC}	20. V_{CC}	20. V_{CC}	20. V_{CC}	20. V_{CC}

'ALS27	'ALS28	'ALS30	'ALS32	'ALS33	'ALS37, 'ALS38	'ALS40
1. 1A	1. nc	1. A	1. nc	1. nc	1. nc	1. nc
2. nc	2. 1Y	2. B	2. nc	2. 1Y	2. nc	2. nc
3. nc	3. nc	3. nc	3. 1A	3. nc	3. 1A	3. 1A
4. 1B	4. 1A	4. C	4. 1B	4. 1A	4. 1B	4. nc
5. 2A	5. 1B	5. D	5. 1Y	5. 1B	5. 1Y	5. 1B
6. 2B	6. 2Y	6. E	6. 2A	6. 2Y	6. 2A	6. 1C
7. 2C	7. 2A	7. F	7. 2B	7. 2A	7. 2B	7. 1D
8. nc	8. nc	8. nc	8. nc	8. nc	8. nc	8. nc
9. 2Y	9. 2B	9. nc	9. 2Y	9. 2B	9. 2Y	9. 1Y
10. GND	10. GND	10. GND	10. GND	10. GND	10. GND	10. GND
11. nc	11. 3A	11. nc	11. 3Y	11. 3A	11. 3Y	11. nc
12. 3Y	12. nc	12. Y	12. nc	12. nc	12. nc	12. 2Y
13. nc	13. 3B	13. nc	13. 3A	13. 3B	13. 3A	13. nc
14. nc	14. nc	14. nc	14. nc	14. nc	14. nc	14. nc
15. 3A	15. 3Y	15. G	15. 3B	15. 3Y	15. 3B	15. 2A
16. 3B	16. 4A	16. H	16. 4Y	16. 4A	16. 4Y	16. 2B
17. 3C	17. 4B	17. nc	17. nc	17. 4B	17. nc	17. 2C
18. 1Y	18. nc	18. nc	18. 4A	18. nc	18. 4A	18. nc
19. 1C	19. 4Y	19. nc	19. 4B	19. 4Y	19. 4B	19. 2D
20. V_{CC}	20. V_{CC}	20. V_{CC}	20. V_{CC}	20. V_{CC}	20. V_{CC}	20. V_{CC}

nc — no internal connection

CHIP CARRIER TERMINAL ASSIGNMENT FOR ADVANCED NEW PRODUCTS

'ALS74	'ALS109	'ALS112	'ALS113	'ALS114	'ALS133	'ALS573
1. nc	1. nc	1. 1CLK	1. nc	1. nc	1. A	1. $\overline{OC}$
2. $1\overline{CLR}$	2. $1\overline{CLR}$	2. 1K	2. 1CLK	2. $\overline{CLR}$	2. B	2. 1D
3. 1D	3. 1J	3. 1J	3. nc	3. nc	3. nc	3. 2D
4. nc	4. $1\overline{K}$	4. nc	4. 1K	4. 1K	4. C	4. 3D
5. 1CLK	5. 1CLK	5. $1\overline{PRE}$	5. 1J	5. 1J	5. D	5. 4D
6. $1\overline{PRE}$	6. $1\overline{PRE}$	6. 1Q	6. $1\overline{PRE}$	6. $1\overline{PRE}$	6. E	6. 5D
7. 1Q	7. 1Q	7. $1\overline{Q}$	7. 1Q	7. 1Q	7. F	7. 6D
8. nc	8. nc	8. nc	8. nc	8. nc	8. nc	8. 7D
9. $1\overline{Q}$	9. $1\overline{Q}$	9. $2\overline{Q}$	9. $1\overline{Q}$	9. $1\overline{Q}$	9. G	9. 8D
10. GND	10. GND	10. GND	10. GND	10. GND	10. GND	10. GND
11. $2\overline{Q}$	11. $2\overline{Q}$	11. $2\overline{Q}$	11. $2\overline{Q}$	11. $2\overline{Q}$	11. Y	11. ENC
12. 2Q	12. 2Q	12. nc	12. 2Q	12. 2Q	12. H	12. 8Q
13. nc	13. nc	13. $2\overline{PRE}$	13. nc	13. nc	13. nc	13. 7Q
14. nc	14. nc	14. 2J	14. nc	14. nc	14. I	14. 6Q
15. $2\overline{PRE}$	15. $2\overline{PRE}$	15. 2K	15. $2\overline{PRE}$	15. $2\overline{PRE}$	15. J	15. 5Q
16. 2CLK	16. 2CLK	16. 2CLK	16. 2J	16. 2J	16. K	16. 4Q
17. 2D	17. $2\overline{K}$	17. $2\overline{CLR}$	17. 2K	17. 2K	17. L	17. 3Q
18. nc	18. 2J	18. nc	18. nc	18. nc	18. nc	18. 2Q
19. $2\overline{CLR}$	19. $2\overline{CLR}$	19. $1\overline{CLR}$	19. 2CLK	19. CLK	19. M	19. 1Q
20. V_{CC}	20. V_{CC}	20. V_{CC}	20. V_{CC}	20. V_{CC}	20. V_{CC}	20. V_{CC}

'ALS574	'ALS576	'ALS580	'ALS873	'ALS874	'ALS876	'ALS880
1. $\overline{OC}$	1. $\overline{OC}$	1. $\overline{OC}$	1. $1\overline{CLR}$	1. $1\overline{CLR}$	1. $1\overline{PRE}$	1. $1\overline{PRE}$
2. 1D	2. 1D	2. 1D	2. $1\overline{OC}$	2. $1\overline{OC}$	2. $1\overline{OC}$	2. $1\overline{OC}$
3. 2D	3. 2D	3. 2D	3. 1D1	3. 1D1	3. 1D1	3. 1D1
4. 3D	4. 3D	4. 3D	4. 1D2	4. 1D2	4. 1D2	4. 1D2
5. 4D	5. 4D	5. 4D	5. nc	5. nc	5. nc	5. nc
6. 5D	6. 5D	6. 5D	6. nc	6. nc	6. nc	6. nc
7. 6D	7. 6D	7. 6D	7. 1D3	7. 1D3	7. 1D3	7. 1D3
8. 7D	8. 7D	8. 7D	8. 1D4	8. 1D4	8. 1D4	8. 1D4
9. 8D	9. 8D	9. 8D	9. 2D1	9. 2D1	9. 2D1	9. 2D1
10. GND	10. GND	10. GND	10. 2D2	10. 2D2	10. 2D2	10. 2D2
11. CLK	11. CLK	11. ENC	11. 2D3	11. 2D3	11. 2D3	11. 2D3
12. 8Q	12. $8\overline{Q}$	12. $8\overline{Q}$	12. $2\overline{D4}$	12. $2\overline{D4}$	12. $2\overline{D4}$	12. $2\overline{D4}$
13. 7Q	13. $7\overline{Q}$	13. $7\overline{Q}$	13. $2\overline{OC}$	13. $2\overline{OC}$	13. $2\overline{OC}$	13. $2\overline{OC}$
14. 6Q	14. $6\overline{Q}$	14. $6\overline{Q}$	14. GND	14. GND	14. GND	14. GND
15. 5Q	15. $5\overline{Q}$	15. $5\overline{Q}$	15. $2\overline{CLR}$	15. $2\overline{CLR}$	15. $2\overline{PRE}$	15. $2\overline{PRE}$
16. 4Q	16. $4\overline{Q}$	16. $4\overline{Q}$	16. EN2C	16. 2CLK	16. 2CLK	16. EN2C
17. 3Q	17. $3\overline{Q}$	17. $3\overline{Q}$	17. 2Q4	17. 2Q4	17. $2\overline{Q}4$	17. $2\overline{Q}4$
18. 2Q	18. $2\overline{Q}$	18. $2\overline{Q}$	18. 2Q3	18. 2Q3	18. $2\overline{Q}3$	18. $2\overline{Q}3$
19. 1Q	19. $1\overline{Q}$	19. $1\overline{Q}$	19. nc	19. nc	19. nc	19. nc
20. V_{CC}	20. V_{CC}	20. V_{CC}	20. nc	20. nc	20. nc	20. nc
			21. 2Q2	21. 2Q2	21. $2\overline{Q}2$	21. $2\overline{Q}2$
			22. 2Q1	22. 2Q1	22. $2\overline{Q}1$	22. $2\overline{Q}1$
			23. 1Q4	23. 1Q4	23. $1\overline{Q}4$	23. $1\overline{Q}4$
			24. 1Q3	24. 1Q3	24. $1\overline{Q}3$	24. $1\overline{Q}3$
			25. 1Q2	25. 1Q2	25. $1\overline{Q}2$	25. $1\overline{Q}2$
			26. 1Q1	26. 1Q1	26. $1\overline{Q}1$	26. $1\overline{Q}1$
			27. EN1C	27. 1CLK	27. 1CLK	27. EN1C
			28. V_{CC}	28. V_{CC}	28. V_{CC}	28. V_{CC}

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'ALS1000	'ALS1002	'ALS1003	'ALS1020	'AS181	'AS800, 'AS802	'AS804, 'AS805, 'AS808, 'AS832
1. nc	1. nc	1. nc	1. nc	1. $\overline{B}0$	1. 1A	1. 1A
2. nc	2. 1Y	2. nc	2. nc	2. $\overline{A}0$	2. 2A	2. 1B
3. 1A	3. nc	3. 1A	3. 1A	3. S3	3. 2B	3. 1Y
4. 1B	4. 1A	4. 1B	4. nc	4. nc	4. 2C	4. 2A
5. 1Y	5. 1B	5. 1Y	5. 1B	5. nc	5. 2D	5. 2B
6. 2A	6. 1Y	6. 2A	6. 1C	6. S2	6. 3A	6. 2Y
7. 2B	7. 2A	7. 2B	7. 1D	7. S1	7. 3B	7. 3A
8. nc	8. nc	8. nc	8. nc	8. S0	8. 3C	8. 3B
9. 2Y	9. 2B	9. 2Y	9. 1Y	9. Cn	9. 3D	9. 3Y
10. GND	10. GND	10. GND	10. GND	10. M	10. GND	10. GND
11. 3Y	11. 3A	11. 3Y	11. nc	11. $\overline{F}0$	11. 3Z	11. 4Y
12. nc	12. nc	12. nc	12. 2Y	12. $\overline{F}1$	12. 3Y	12. 4A
13. 3A	13. 3B	13. 3A	13. nc	13. $\overline{F}2$	13. 2Z	13. 4B
14. nc	14. nc	14. nc	14. nc	14. GND	14. 2Y	14. 5Y
15. 3B	15. 3Y	15. 3B	15. 2A	15. $\overline{F}3$	15. 1Z	15. 5A
16. 4Y	16. 4A	16. 4Y	16. 2B	16. A=B	16. 1Y	16. 5B
17. nc	17. 4B	17. nc	17. 2C	17. nc	17. 1B	17. 6Y
18. 4A	18. nc	18. 4A	18. nc	18. nc	18. 1C	18. 6A
19. 4B	19. 4Y	19. 4B	19. 2D	19. $\overline{P}$	19. 1D	19. 6B
20. V_{CC}	20. V_{CC}	20. V_{CC}	20. V_{CC}	20. Cn+4	20. V_{CC}	20. V_{CC}
				21. $\overline{G}$		
				22. $\overline{B}3$		
				23. $\overline{A}3$		
				24. $\overline{B}2$		
				25. $\overline{A}2$		
				26. $\overline{B}1$		
				27. $\overline{A}1$		
				28. V_{CC}		

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CHIP CARRIER TERMINAL ASSIGNMENT FOR ADVANCED NEW PRODUCTS

'AS857	'AS867, 'AS869	'AS870	'AS871	'AS873	'AS874	'AS876
1. S0	1. S0	1. S0	1. DA1	1. 1$\overline{CLR}$	1. 1$\overline{CLR}$	1. 1$\overline{PRE}$
2. 1A	2. S1	2. 1A0	2. DA2	2. 1$\overline{OC}$	2. 1$\overline{OC}$	2. 1$\overline{OC}$
3. 1B	3. A	3. 1A1	3. S0	3. 1D1	3. 1D1	3. 1D1
4. 1Y	4. B	4. 1A2	4. 1A0	4. 1D2	4. 1D2	4. 1D2
5. nc	5. nc	5. nc	5. 1A1	5. nc	5. nc	5. nc
6. nc	6. nc	6. nc	6. 1A2	6. nc	6. nc	6. nc
7. 2A	7. C	7. 1A3	7. 1A3	7. 1D3	7. 1D3	7. 1D3
8. 2B	8. D	8. 1R/$\overline{W}$	8. 1R/$\overline{W}$	8. 1D4	8. 1D4	8. 1D4
9. 2Y	9. E	9. S2	9. S2	9. 2D1	9. 2D1	9. 2D1
10. 3A	10. F	10. DQA1	10. QA1	10. 2D2	10. 2D2	10. 2D2
11. 3B	11. G	11. DQA2	11. QA2	11. 2D3	11. 2D3	11. 2D3
12. 3Y	12. H	12. DQA3	12. QA3	12. 2D4	12. 2D4	12. 2D4
13. OPZ	13. EN$\overline{T}$	13. DQA4	13. QA4	13. 2$\overline{OC}$	13. 2$\overline{OC}$	13. 2$\overline{OC}$
14. GND	14. GND	14. GND	14. GND	14. GND	14. GND	14. GND
15. $\overline{T}$/C	15. $\overline{RCO}$	15. DQB1	15. DQB1	15. 2$\overline{CLR}$	15. 2$\overline{CLR}$	15. 2$\overline{PRE}$
16. 4Y	16. CLK	16. DQB2	16. DQB2	16. EN2C	16. 2CLK	16. 2CLK
17. 4B	17. QH	17. DQB3	17. DQB3	17. 2Q4	17. 2Q4	17. 2$\overline{Q}$4
18. 4A	18. QG	18. DQB4	18. DQB4	18. 2Q3	18. 2Q3	18. 2$\overline{Q}$3
19. nc	19. nc	19. nc	19. S3	19. nc	19. nc	19. nc
20. nc	20. nc	20. nc	20. 2R/$\overline{W}$	20. nc	20. nc	20. nc
21. 5Y	21. QF	21. S3	21. 2A0	21. 2Q2	21. 2Q2	21. 2$\overline{Q}$2
22. 5B	22. QE	22. 2R/$\overline{W}$	22. 2A1	22. 2Q1	22. 2Q1	22. 2$\overline{Q}$1
23. 5A	23. QD	23. 2A0	23. 2A2	23. 1Q4	23. 1Q4	23. 1$\overline{Q}$4
24. 6Y	24. QC	24. 2A1	24. 2A3	24. 1Q3	24. 1Q3	24. 1$\overline{Q}$3
25. 6B	25. QB	25. 2A2	25. S1	25. 1Q2	25. 1Q2	25. 1$\overline{Q}$2
26. 6A	26. QA	26. 2A3	26. DA3	26. 1Q1	26. 1Q1	26. 1$\overline{Q}$1
27. S1	27. EN$\overline{P}$	27. S1	27. DA4	27. EN1C	27. 1CLK	27. 1CLK
28. V_{CC}	28. V_{CC}	28. V_{CC}	28. V_{CC}	28. V_{CC}	28. V_{CC}	28. V_{CC}

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CHIP CARRIER TERMINAL ASSIGNMENT FOR ADVANCED NEW PRODUCTS

'AS877	'AS880	'AS881	'AS882	'AS885	'AS894
1. S0	1. 1$\overline{PRE}$	1. $\overline{B}$0	1. Cn	1. M	1. S0
2. S1	2. 1$\overline{OC}$	2. $\overline{A}$0	2. $\overline{G}$0	2. P < Qin	2. S1
3. S2	3. 1D1	3. S3	3. P0	3. P > Qin	3. S2
4. DQA1	4. 1D2	4. nc	4. $\overline{G}$1	4. Q7	4. S3
5. nc	5. nc	5. nc	5. nc	5. nc	5. nc
6. nc	6. nc	6. S2	6. nc	6. nc	6. nc
7. DQA2	7. 1D3	7. S1	7. $\overline{P}$1	7. Q6	7. A
8. DQA3	8. 1D4	8. S0	8. Cn+8	8. Q5	8. B
9. DQA4	9. 2D1	9. Cn	9. $\overline{G}$2	9. Q4	9. C
10. DQA5	10. 2D2	10. M	10. $\overline{P}$2	10. Q3	10. D
11. DQA6	11. 2D3	11. $\overline{F}$0	11. $\overline{G}$3	11. Q2	11. RI/LO
12. DQA7	12. 2D4	12. $\overline{F}$1	12. $\overline{P}$3	12. Q1	12. $\overline{CO}$/AI
13. DQA8	13. 2$\overline{OC}$	13. $\overline{F}$2	13. Cn+16	13. Q0	13. $\overline{DO}$/BI
14. GND	14. GND	14. GND	14. GND	14. GND	14. GND
15. Q8	15. 2$\overline{PRE}$	15. $\overline{F}$3	15. $\overline{G}$4	15. P > Qout	15. QD
16. DQB8	16. EN2C	16. A=B	16. $\overline{P}$4	16. P < Qout	16. QC
17. DQB7	17. 2$\overline{Q}$4	17. nc	17. $\overline{G}$5	17. P0	17. QB
18. DQB6	18. 2$\overline{Q}$3	18. nc	18. $\overline{P}$5	18. P1	18. QA
19. nc	19. nc	19. $\overline{P}$	19. nc	19. nc	19. nc
20. nc	20. nc	20. Cn+4	20. nc	20. nc	20. nc
21. DQB5	21. 2$\overline{Q}$2	21. $\overline{G}$	21. Cn+24	21. P2	21. $\overline{A}$O/CI
22. DQB4	22. 2$\overline{Q}$1	22. $\overline{B}$3	22. $\overline{G}$6	22. P3	22. $\overline{B}$O/DI
23. DQB3	23. 1$\overline{Q}$4	23. $\overline{A}$3	23. $\overline{P}$6	23. P4	23. LI/RO
24. DQB2	24. 1$\overline{Q}$3	24. $\overline{B}$2	24. $\overline{G}$7	24. P5	24. $\overline{OC}$
25. DQB1	25. 1$\overline{Q}$2	25. $\overline{A}$2	25. $\overline{P}$7	25. P6	25. $\overline{CLR}$
26. D1	26. 1$\overline{Q}$1	26. $\overline{B}$1	26. Cn+32	26. P7	26. OV/Z
27. CLK	27. EN1C	27. $\overline{A}$1	27. nc	27. LENC	27. CLK
28. V_{CC}	28. V_{CC}	28. V_{CC}	28. V_{CC}	28. V_{CC}	28. V_{CC}

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PLANNED NEW PRODUCTS

The following is a list of Advanced Low-Power Schottky and Advanced Schottky products that have been identified for introduction in the near future.

'ALS86	Quad 2-input exclusive-OR gates
'ALS138	3- to 8-line decoders/demultiplexers
'ALS139	Dual 2- to 4-line decoders/multiplexers
'ALS151	1- of 8-line data selectors/multiplexers
'ALS153	Dual 1- of 4-line data selectors/multiplexers
'ALS157	Quad 1- of 2-line data selectors/multiplexers
'ALS158	Quad 1- of 2-line data selectors/multiplexers
'ALS160	Synchronous 4-bit counters, decade, direct clear
'ALS161	Synchronous 4-bit counters, binary, direct clear
'ALS162	Fully synchronous 4-bit counters, decade
'ALS163	Fully synchronous 4-bit counters, binary
'ALS168	Synchronous 4-bit up/down counters, decade
'ALS169	Synchronous 4-bit up/down counters, binary
'ALS174	Hex D-type flip-flops
'ALS175	Quad D-type flip-flops
'ALS190	Synchronous 4-bit up/down counters, decade
'ALS191	Synchronous 4-bit up/down counters, binary
'ALS192	Synchronous 4-bit up/down counters, decade
'ALS193	Synchronous 4-bit up/down counters, binary
'ALS240	Octal inverting bus-line drivers
'ALS241	Octal bus-line drivers
'ALS242	Quad inverting bus transceivers
'ALS243	Quad bus transceivers
'ALS244	Octal bus-line drivers
'ALS251	1- of 8-line data selectors/multiplexers, 3-state
'ALS253	Dual 1- of 4-line data selectors/multiplexers, 3-state
'ALS257	Quad 1- of 2-line data selectors/multiplexers, 3-state
'ALS258	Quad 1- of 2-line data selectors/multiplexers, 3-state
'ALS259	8-bit addressable latches
'ALS273	Octal D-type flip-flops
'ALS299	Octal shift/storage registers, 3-state
'ALS323	Octal shift/storage registers, sync. clear, 3-state
'ALS352	Dual 4- to 1-line inverting data selectors/multiplexers
'ALS353	Dual 4- to 1-line data selectors/multiplexers, 3-state, inverting
'ALS465	Octal buffers, 3-state
'ALS466	Octal buffers, inverting, 3-state
'ALS467	Octal buffers, 3-state
'ALS468	Octal buffers, inverting, 3-state
'ALS521	Octal comparators
'ALS538	1- of 8-line decoders, 3-state
'ALS539	Dual 1- of 4-line decoders, 3-state
'ALS540	Octal inverting bus-line drivers, 3-state
'ALS541	Octal bus-line drivers, 3-state
'ALS560	4-bit decade counters, 3-state
'ALS561	4-bit binary counters, 3-state
'ALS568	4-bit decade up/down counters, 3-state
'ALS569	4-bit binary up/down counters, 3-state

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'ALS620	Inverting octal bus transceivers, dual enable, 3-state
'ALS621	Octal bus transceivers, dual enable, open-collector
'ALS622	Inverting octal bus transceivers, dual enable, open-collector
'ALS623	Octal bus transceivers, dual enable, 3-state
'ALS632	32-bit error detection and correction circuits with internal diagnostics
'ALS638	Inverting octal bus transceivers, 3-state and open-collector
'ALS639	Octal bus transceivers, 3-state and open-collector
'ALS640	Inverting octal bus transceivers, 3-state
'ALS641	Octal bus transceivers, open-collector
'ALS642	Inverting octal bus transceivers, open-collector
'ALS643	Inverting/true octal bus transceivers, 3-state
'ALS644	Inverting/true octal bus transceivers, open-collector
'ALS645	Octal bus transceivers, 3-state
'ALS857	6-line universal multiplexers, 3-state
'ALS1008	Quad 2-input AND gates
'ALS1010	Triple 3-input NAND gates
'ALS1011	Triple 3-input NAND gates
'ALS1032	Quad 2-input OR gates
'ALS1240	Low-power 'ALS240
'ALS1241	Low-power 'ALS241
'ALS1242	Low-power 'ALS242
'ALS1243	Low-power 'ALS243
'ALS1244	Low-power 'ALS244
'ALS1616	16-by-16 parallel multipliers
'ALS1620	Low-power 'ALS620
'ALS1621	Low-power 'ALS621
'ALS1622	Low-power 'ALS622
'ALS1623	Low-power 'ALS623
'ALS1638	Low-power 'ALS638
'ALS1639	Low-power 'ALS639
'ALS1640	Low-power 'ALS640
'ALS1641	Low-power 'ALS641
'ALS1642	Low-power 'ALS642
'ALS1643	Low-power 'ALS643
'ALS1644	Low-power 'ALS644
'ALS1645	Low-power 'ALS645
'AS74	Dual D-type flip-flops
'AS109	Dual J-K flip-flops
'AS112	Dual J-K flip-flops
'AS113	Dual J-K flip-flops
'AS114	Dual J-K flip-flops
'AS151	1- of 8-line data selectors/multiplexers
'AS153	Dual 1- of 4-line data selectors/multiplexers
'AS160	Synchronous 4-bit counters, decade, direct clear
'AS161	Synchronous 4-bit counters, binary, direct clear
'AS162	Fully synchronous 4-bit counters, decade
'AS163	Fully synchronous 4-bit counters, binary
'AS168	Synchronous 4-bit up/down counters, decade
'AS169	Synchronous 4-bit up/down counters, binary
'AS174	Hex D-type flip-flops

PLANNED NEW PRODUCTS

'AS175	Quad D-type flip-flops
'AS240	Inverting octal bus-line drivers, 3-state
'AS241	Octal bus-line drivers, 3-state
'AS242	Quad inverting bus transceivers
'AS243	Quad bus transceivers
'AS244	Octal bus-line drivers, 3-state
'AS251	1- of 8-line data selector/multiplexer, 3-state
'AS253	Dual 1- of 4-line data selectors/multiplexers, 3-state
'AS280	9-bit odd/even parity generators/checkers
'AS373	Octal transparent latches, 3-state
'AS374	Octal D-type flip-flops, 3-state
'AS533	Octal inverting transparent latches, 3-state
'AS534	Octal inverting transparent flip-flops, 3-state
'AS573	Octal transparent latches, 3-state
'AS574	Octal D-type edge-triggered flip-flops, 3-state
'AS576	Octal inverting D-type edge-triggered flip-flops, 3-state
'AS580	Octal inverting transparent latches, 3-state

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