The Engineering Staff of
TEXAS INSTRUMENTS INCORPORATED
Semiconductor Group

The Bipolar Microcomputer Components Data Book

for

Design Engineers

Bipolar Memories
Microcomputers
TTL Product Guide

Third Edition

TEXAS INSTRUMENTS
INCORPORATED

TI Sales Offices

ALABAMA: Huntsville, 500 Wynn Drive, Suite 514, Huntsville, AL 35805, (205) 837-7530.

ARIZONA: Phoenix, P.O. Box 35160, 8102 N. 23rd Ave., Suite A, Phoenix, AZ 85069, (602) 249-1313.

CALIFORNIA: El Segundo, 831 S. Douglas St., El Segundo, CA 90245, (213) 973-2571; **Irvine,** 17620 Fitch, Irvine, CA 92714, (714) 545-5210; **Sacramento,** 1900 Point West Way, Suite 171, Sacramento, CA 95815, (916) 929-1521; **San Diego,** 4333 View Ridge Ave., Suite B., San Diego, CA 92123, (714) 278-9600; **Sunnyvale,** P.O. Box 9064, 776 Palomar Ave., Sunnyvale, CA 94086, (408) 732-1840; **Woodland Hills,** 21220 Erwin St., Woodland Hills, CA 91364, (213) 704-7759.

COLORADO: Denver, 9725 E. Hampden St., Suite 301, Denver, CO 80231, (303) 695-2800.

CONNECTICUT: Wallingford, 9 Barnes Industrial Park Rd., Barnes Industrial Park, Wallingford, CT 06492, (203) 269-0074.

FLORIDA: Clearwater, 2280 U.S. Hwy. 19 N., Suite 232, Clearwater, FL 33515, (813) 325-1861; **Ft. Lauderdale,** 2765 N.W. 62nd St., Ft. Lauderdale, FL 33309, (305) 973-8502; **Winter Park,** 1850 Lee Rd., Suite 115, Winter Park, FL 32789, (305) 644-3535.

GEORGIA: Atlanta, 3300 Northeast Expy., Building 9, Atlanta, GA 30341, (404) 452-4600.

ILLINOIS: Arlington Heights, 515 W. Algonquin, Arlington Heights, IL 60005, (312) 640-2934.

INDIANA: Ft. Wayne, 2020 Inwood Dr., Ft. Wayne, IN 46805, (219) 424-5174; **Indianapolis,** 2346 S. Lynhurst, Suite J-400, Indianapolis, IN 46241, (317) 248-8555.

MARYLAND: Baltimore 1 Rutherford Pl., 7133 Rutherford Rd., Baltimore, MD 21207, (301) 944-8600.

MASSACHUSETTS: Waltham, 504 Totten Pond Rd., Waltham, MA 02154, (617) 890-7400.

MICHIGAN: Farmington Hills, 3373 W. 12 Mile Rd., Farmington Hills, MI 48018, (313) 553-1500.

MINNESOTA: Edina, 7625 Parklawn, Edina, MN 55435, (612) 830-1600.

MISSOURI: Kansas City, 8080 Ward Pkwy., Kansas City, MO 64114, (816) 523-2500; **St. Louis,** 11861 Westline, Industrial Line Drive, St. Louis, MO 63141, (314) 569-7600.

NEW JERSEY: Clark, 292 Terminal Ave. West, Clark, NJ 07066, (201) 574-9800.

NEW MEXICO: Albuquerque, 5907 Alice NSE, Suite E, Albuquerque, NM 87110, (505) 265-8491.

NEW YORK: East Syracuse, 6700 Old Collamer Rd., East Syracuse, NY 13057, (315) 463-9291; **Endicott,** 112 Nanticoke Ave., P.O. Box 618, Endicott, NY 13760, (607) 754-3900; **Melville,** 1 Huntington Quadrangle, Suite 3C10, P.O. Box 2936, Melville, NY 11747, (516) 454-6600, **Poughkeepsie,** 201 South Ave., Poughkeepsie, NY 12601, (914) 473-2900; **Rochester,** 1210 Jefferson Rd., Rochester, NY 14623, (716) 424-5400.

NORTH CAROLINA: Charlotte, 8 Woodlawn Green, Woodlawn Rd., Charlotte, NC 28210, (704) 527-0930.

OHIO: Beachwood, 23408 Commerce Park Rd., Beachwood, OH 44122, (216) 464-6100, **Dayton,** Kingsley Bldg., 4124 Linden Ave., Dayton, OH 45432, (513) 258-3877.

OKLAHOMA: Tulsa, 3105 E. Skelly Dr., Suite 512, Tulsa, OK 74105, (918) 749-9547.

OREGON: Beaverton, 6700 SW 105th St., Suite 110, Beaverton, OR 97005, (503) 643-6758.

PENNSYLVANIA: Ft. Washington, 575 Virginia Dr., Ft. Washington, PA 19034, (215) 643-6450.

TENNESSEE: Johnson City, P.O. Drawer 1255, Erwin Hwy., Johnson City, TN 37601, (615) 461-2129.

TEXAS: Austin, 12501 Research Bldg., P.O. Box 2909, Austin, TX 78723, (512) 250-7655; **Dallas,** P.O. Box 225012, Dallas, TX 75265, (214) 995-6531; **Houston,** 9000 Southwest Frwy., Suite 400, Houston, TX 77036, (713) 778-6592.

UTAH: Salt Lake City, 3672 West 2100 South, Salt Lake City UT 84120, (801) 973-6310.

VIRGINIA: Fairfax, 3001 Prosperity, Fairfax, VA 22031, (703) 849-1400; **Midlothian,** 13711 Sutter's Mill Circle, Midlothian, VA 23113, (804) 744-1007.

WASHINGTON: Redmond, 2723 152nd Ave., N.E. Bldg 6, (206) 881-3080, Redmond, WA 98052.

CANADA: Ottawa, 436 McClaren St., Ottawa, Canada, K2P0M8, (613) 233-1177; **Richmond Hill,** 280 Centre St. E., Richmond Hill L4C1B1, Ontario, Canada, (416) 884-9181; **St. Laurent,** Ville St. Laurent Quebec, 9460 Trans Canada Hwy., St. Laurent, Quebec, Canada H4S1R7, (514) 334-3635. L

TI Distributors

ALABAMA: Huntsville, Hall-Mark (205) 837-8700.

ARIZONA: Phoenix, Kierulff (602) 243-4101; R.V. Weatherford (602) 272-7144; **Tempe,** Marshall (602) 968-6181; **Tucson,** Kierulff (602) 624-9986.

CALIFORNIA: Anaheim, R.V. Weatherford (714) 634-9600; **Buena Park,** RPS (213) 744-0355; **Canoga Park,** Marshall (213) 999-5001; **Chatsworth,** JACO (213) 998-2200; **El Monte,** Marshall (213) 686-0141; **Glendale,** R.V. Weatherford (213) 849-3451; **Goleta,** RPS (805) 964-6823; **Irvine,** JACO (714) 540-5600; Marshall (714) 556-6400; **Los Angeles,** Kierulff (213) 725-0325; **Palo Alto,** Kierulff (415) 968-6292; **Pomona,** R.V. Weatherford (714) 623-1261; **Sacramento,** Kierulff (916) 924-8522; **San Diego,** Arrow (714) 565-4800; Kierulff (714) 278-2112; Marshall (714) 578-9600; R.V. Weatherford (714) 695-1700; **Santa Barbara,** R.V. Weatherford (805) 465-8551; **Santa Clara,** United Components (408) 496-6900; **Sunnyvale,** Arrow (408) 745-6600; Marshall (408) 732-1100; Time (408) 734-9888; United Components (408) 496-6900; **Torrance,** Time (213) 320-0880; **Tustin,** Kierulff (714) 731-5711.

COLORADO: Denver, Arrow (303) 758-2100; Diplomat (303) 740-8300; Kierulff (303) 371-6500; **Englewood,** R.V. Weatherford (303) 770-9762.

CONNECTICUT: Orange, Milgray (203) 795-0714; **Wallingford,** Arrow (203) 265-7741; Marshall (203) 265-3822.

FLORIDA: Clearwater, Diplomat (813) 443-4514; **Ft. Lauderdale,** Arrow (305) 973-8502; Diplomat (305) 971-7160; Hall-Mark (305) 971-9280; **Orlando,** Hall-Mark (305) 855-4020; **Palm Bay,** Arrow (305) 725-1480; Diplomat (305) 725-4520; **St. Petersburg,** Kierulff (813) 576-1966; **Winter Park,** Milgray (305) 647-5747.

GEORGIA: Norcross, Arrow (404) 449-8252; Hall-Mark (404) 447-8000; Marshall (404) 923-5750.

ILLINOIS: Bensonville, Diplomat (312) 595-1000; Hall-Mark (312) 860-3800; **Elk Grove Village,** Kierulff (312) 640-0200; **Chicago,** Newark (312) 638-4411; **Schaumburg,** Arrow (312) 893-9420.

INDIANA: Ft. Wayne, Graham (219) 423-3422; **Indianapolis,** Graham (317) 634-8202; Arrow (317) 243-9353.

IOWA: Cedar Rapids, Deeco (319) 365-7551.

KANSAS: Lenexa, Component Specialties (913) 492-3555; **Shawnee Mission,** Hall-Mark (913) 888-4747; **Wichita,** LCOMP (316) 265-9507.

MARYLAND: Baltimore, Arrow (202) 737-1700, (301) 247-5200; Hall-Mark (301) 796-9300; **Columbia,** Diplomat (301) 995-1226; **Rockville,** Milgray (301) 466-6400.

MASSACHUSETTS: Billerica, Kierulff (617) 667-8331; **Burlington,** Marshall (617) 272-8200; **Woburn,** Arrow (617) 933-8130; Time (617) 935-8080.

MICHIGAN: Ann Arbor, Arrow (313) 971-8200; **Oak Park,** Newark (313) 967-0600; **Farmington,** Diplomat (313) 477-3200; **Grand Rapids,** Newark (616) 241-6681.

MINNESOTA: Bloomington, Hall-Mark (612) 854-3223; **Edina,** Arrow (612) 830-1800; Kierulff (612) 835-4388; **Minneapolis,** Diplomat (612) 788-8601.

MISSOURI: Earth City, Hall-Mark (314) 291-5350; **Kansas City,** LCOMP (816) 221-2400; **St. Louis,** Arrow (314) 567-6888; LCOMP (314) 291-6200; Kierulff (314) 569-7630.

NEW HAMPSHIRE: Manchester, Arrow (603) 668-6968.

NEW JERSEY: Camden, General Radio Supply (609) 964-8560; **Cherry Hill,** Hall-Mark (609) 424-0880; **Clifton,** JACO (201) 989-7081; Marshall (201) 340-1900; **Fairfield,** Kierulff (201) 575-6750; **Marlton,** Milgray (609) 424-1300; **Moorestown,** Arrow (609) 235-1900; **Saddlebrook,** Arrow (201) 797-5800; **Totowa,** Diplomat (201) 785-1830.

NEW MEXICO: Albuquerque, Arrow (505) 243-4566; International Electronics (505) 345-8127; United Components (505) 345-9981.

NEW YORK: Endwell, Marshall (607) 754-1570; **Freeport,** Milgray (516) 546-5600, N.J. (800) 645-3986; **Hauppauge,** Arrow (516) 231-1000; JACO (516) 273-5500; **Liverpool,** Arrow (315) 652-1000; Diplomat (315) 652-5000; **Melville,** Diplomat (516) 454-6400; **Rochester,** Arrow (716) 275-0300; Rochester Radio Supply (716) 454-7800; Marshall (716) 235-7620; **Ronkonkoma,** QPL (516) 467-1200.

NORTH CAROLINA: Greensboro, Kierulff (919) 852-6261; **Raleigh,** Arrow (919) 876-3132; Hall-Mark (919) 832-4465; **Winston-Salem,** Arrow (919) 725-8711.

OHIO: Beachwood, Kierulff (216) 464-6100; **Centerville,** Arrow (513) 435-5563; **Cincinnati,** Graham (513) 732-1661; **Columbus,** Hall-Mark (614) 846-1882; **Dayton,** ESCO (513) 226-1133; Marshall (513) 236-8088; **Highland Heights,** Hall-Mark (216) 473-2907; **Solon,** Arrow (216) 248-3990.

OKLAHOMA: Tulsa, Component Specialties (918) 664-2820; Hall-Mark (918) 835-8458; Kierulff (918) 749-9543.

OREGON: Beaverton, Almac/Stroum (503) 641-9070; **Portland,** Kierulff (503) 641-9150.

PENNSYLVANIA: Pittsburgh, Arrow (412) 856-7000.

TEXAS: Austin, Component Specialties (512) 837-8922; Hall-Mark (512) 837-2814; Harrison Equipment (512) 458-3555; Kierulff (512) 250-7037; **Dallas,** Component Specialties (214) 357-6511; Hall-Mark (214) 341-1147; International Electronics (214) 233-9323; Kierulff (214) 343-2400; **El Paso,** International Electronics (915) 778-9761; **Houston,** Component Specialties (713) 771-7237; Hall-Mark (713) 78* 6100; Harrison Equipment (713) 652-4700; Kierulff (713) 778-6530.

UTAH: Salt Lake City, Diplomat (801) 486-4134; Kierulff (801) 973-6913.

WASHINGTON: Redmond, United Components (206) 643-7444; **Seattle,** Almac/Stroum (206) 763-2300; Kierulff (206) 575-4420; **Tukwila,** Arrow (206) 575-0907.

WISCONSIN: Oak Creek, Arrow (414) 764-6600; Hall-Mark (414) 761-3000; **Waukesha,** Kierulff (414) 784-8160.

CANADA: Calgary, Cam Gard Supply (403) 287-0520; Future (403) 259-6408; Varah (403) 230-1235; **Downsview,** CESCO (416) 661-0220; **Edmonton,** Cam Gard Supply (403) 426-1805; **Halifax,** Cam Gard Supply (902) 454-8581; **Hamilton,** Varah (416) 561-9311; **Kamloops,** Cam Gard Supply (604) 372-3338; **Moncton,** Cam Gard Supply (506) 855-2200; **Montreal,** CESCO (514) 735-5511; Future (514) 731-7441; **Ottawa,** CESCO (613) 729-5118; Future (613) 820-8313; **Quebec City,** CESCO (418) 687-4231; **Regina,** Cam Gard Supply (306) 525-1317; **Saskatoon,** Cam Gard Supply (306) 652-6424; **Toronto,** Future (416) 663-5563; **Vancouver,** Cam Gard Supply (604) 291-1441; Future (604) 438-5545; Varah (604) 873-3211; **Winnipeg,** Cam Gard Supply (204) 786-8481; Varah (204) 633-6190. AD

Texas Instruments invented the integrated circuit, microprocessor and microcomputer. Being first is our tradition.

TEXAS INSTRUMENTS
INCORPORATED

The Bipolar Microcomputer Components Data Book

for

Design Engineers

Third Edition

TEXAS INSTRUMENTS
INCORPORATED

LCC5831
72075-081-RS

Printed in U.S.A.

Texas Instruments, the inventor of the integrated circuit, the microprocessor, and the microcomputer, is a leader in semiconductor technology. For information on other semiconductor products, contact:

Marketing and Information Services
Texas Instruments Incorporated
P.O. Box 225012, MS 408
Dallas, Texas 75265

IMPORTANT NOTICES

Texas Instruments reserves the right to make changes at any time in order to improve design and to supply the best product possible.

TI cannot assume any responsibility for any circuits shown or represent that they are free from patent infringement.

Information contained herein supercedes previously published data on these products.

ISBN 0-89512-110-7
Library of Congress Catalog Number: 81-51167

THE BIPOLAR MICROCOMPUTER COMPONENTS DATA BOOK

Third Edition

TI invented the Integrated Circuit, The Microprocessor, and the Microcomputer, which have made TI synonymous with reliability, affordability, and compactness. The products in this book carry on TI's tradition of technology leadership.

This data book describes a series of high-complexity bipolar digital building blocks designed specifically for implementing high-performance computer or controller systems. The series offers the system designer maximum flexibility for achieving cost-effective hardware designs from dedicated, highly specialized unique systems with tailored instructions to general-purpose computers capable of emulating existing machine instructions, or programs, without loss of software investment.

In addition to a choice between a high-performance Schottky-clamped† TTL 4-bit-slice processor element and a 16-bit computer central processing unit (CPU), the system designer can pick from a new expanded family of Schottky TTL memories (RAMs, PROMs, and FIFOs), and state-of-the-art support functions needed to meet all control and interface requirements.

The SN74LS481 and the SN74S481, with typical clock cycle times of 90 ns, feature automatically sequenced iterative multiply, divide, and cyclical-redundancy algorithms to simplify system design. Design is also simplified at a very low package count when the expandable SN54S482/SN74S482 4-bit-slice controller is used to generate next-address functions.

The SBP9900A microprocessor, a ruggedized, monolithic, 16-bit parallel I^2L central processing unit (CPU), combines an advanced memory-to-memory architecture and a powerful minicomputer instruction set with the simplicity of a single power supply and static logic with a single-phase clock to thrust its capabilities beyond those of existing microprocessors.

The SBP9989 microprocessor is the most recent addition to the SBP9900 I^2L family, the military 16-bit solution to meeting the complex tasks of the eighties. With designed-in multiprocessor support, new signal functions and instructions, and increased speed, the SBP9989 extends the 9900 performance level and provides reliability in rugged environments – the key to all SBP9900 family members.

The family of high-performance Schottky TTL memories offers a wide variety of organizations providing efficient solutions for virtually any size micro-control or program memory application. A new expanded family of bipolar PROMs (including standard, low-power, power-down, and registered versions) has dictated a new numbering system to encompass new device types. Redesigned lower density PROMs now offer up to 20% faster maximum address access times and reductions of as much as 35% in power consumption. TI's popular 1K, a Low-Power 2K, two 512 X 8 4K's, and the 1024 X 8 24-Pin 8K PROMs are being followed by a 16K PROM with a typical address access time of 35 ns.

Included in this volume is a Functional Index to all bipolar digital device types available or under development showing the available technologies for each type (Standard TTL, Schottky, Low-Power Schottky, Advanced Low-Power Schottky, Advanced Schottky, etc.). Logic symbols prepared in anticipation of IEEE Std. 91-1982 and pin assignments for all bipolar devices are shown in this data book with typical performance data and chip carrier information where applicable. These additions to the data book should prove helpful to design and component engineers by providing ready access to TI's full line of bipolar digital device types and technologies.

This volume offers design and specification data for bipolar computer components. Complete technical data for any TI semiconductor product is available from your nearest TI field sales office, local authorized TI distributor, or by writing direct to: Marketing and Information Services, Texas Instruments Incorporated, P. O. Box 225012, MS 308, Dallas, Texas 75265.

We sincerely hope you will find the BIPOLAR MICROCOMPUTER COMPONENTS DATA BOOK a meaningful addition to your technical library.

† Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U.S. Patent Number 3,463,975.

TABLE OF CONTENTS

TABLE OF CONTENTS
(Continued)

PAGE

This alphanumeric index includes only those TI products for which data sheet specifications are included in this book. The Functional Index, Section 6, and the Product Guide, Section 8, include some basic information on all current TI bipolar digital-logic products. For detailed specifications on bipolar digital-logic products not contained in this book, see the latest version of The TTL Data Book for Design Engineers.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

GENERAL INFORMATION

INTRODUCTION

This glossary consists of two parts: (1) general concepts for digital circuits including types of bipolar memories and (2) operating conditions and characteristics (including letter symbols). Some of the terms, symbols, abbreviations, and definitions used with memory integrated circuits have not, as yet, been standardized. These are currently under consideration by the EIA/JEDEC (Electronic Industries Association) and the IEC (International Electrotechnical Commission). The following are as consistent with the past and future work of these organizations as is possible to anticipate at this time.

PART I – GENERAL CONCEPTS INCLUDING TYPES OF BIPOLAR MEMORIES

Chip-Enable Input

A control input that when active permits operation of the integrated circuit for input, internal transfer, manipulation, refreshing, and/or output of data and when inactive causes the integrated circuit to be in a reduced-power standby mode.
NOTE: See "chip-select input".

Chip-Select Input

A gating input that when inactive prevents input or output of data to or from an integrated circuit.
NOTE: See "chip-enable input".

Dynamic (Read/Write) Memory

A read/write memory in which the cells require the repetitive application of control signals in order to retain stored data.
NOTES: 1. The words "read/write" may be omitted from the term when no misunderstanding will result.
2. Such repetitive application of the control signals is normally called a refresh operation.
3. A dynamic memory may use static addressing or sensing circuits.
4. This definition applies whether the control signals are generated inside or outside the integrated circuit.

First-In First-Out (FIFO) Memory

A memory from which data bytes or words can be read in the same order, but not necessarily at the same rate, as that of the data entry.

Gate Equivalent Circuit

A basic unit-of-measure of relative digital-circuit complexity. The number of gate equivalent circuits is that number of individual logic gates that would have to be interconnected to perform the same function.

Large-Scale Integration, LSI

A concept whereby a complete major subsystem or system function is fabricated as a single microcircuit. In this context a major subsystem or system, whether digital or linear, is considered to be one that contains 100 or more equivalent gates or circuitry of similar complexity.

Mask-Programmed Read-Only Memory

A read-only memory in which the data content of each cell is determined during manufacture by the use of a mask, the data content thereafter being unalterable.

Medium-Scale Integration, MSI

A concept whereby a complete subsystem or system function is fabricated as a single microcircuit. The subsystem or system is smaller than for LSI, but whether digital or linear, is considered to be one that contains 12 or more equivalent gates or circuitry of similar complexity.

Memory Cell

The smallest subdivision of a memory into which a unit of data has been or can be entered, in which it is or can be stored, and from which it can be retrieved.

Memory Integrated Circuit

An integrated circuit consisting of memory cells and usually including associated circuits such as those for address selection, amplifiers, etc.

Output-Enable Input

A gating input that when active permits the integrated circuit to output data and when inactive causes the integrated circuit output(s) to be at a high impedance (off).

Programmable Read-Only Memory (PROM)

A read-only memory that after being manufactured can have the data content of each memory cell altered once only.

Random-Access Memory (RAM)

A memory that permits access to any of its address locations in any desired sequence with similar access time for each location.
NOTE: The term RAM, as commonly used, denotes a read/write memory.

Read-Only Memory (ROM)

A memory in which the contents are not intended to be altered during normal operation.
NOTE: Unless otherwise qualified, the term "read-only memory" implies that the content is unalterable and defined by construction.

Read/Write Memory

A memory in which each cell may be selected by applying appropriate electronic input signals and the stored data may be either (a) sensed at appropriate output terminals, or (b) changed in response to other similar electronic input signals.

Small-Scale Integration, SSI

Integrated circuits of less complexity than medium-scale integration (MSI).

Very-Large-Scale Integration, VLSI

A concept whereby a complete system function is fabricated as a single microcircuit. In this context, a system, whether digital or linear, is considered to be one that contains 3000 or more gates or circuitry of similar complexity.

Volatile Memory

A memory the data content of which is lost when power is removed.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

PART II – OPERATING CONDITIONS AND CHARACTERISTICS (INCLUDING LETTER SYMBOLS)

The symbols for quantities involving time use upper and lower case letters according to the following historically evolved principles:

a. Time itself, is always represented by a lower case t.

b. Subscripts are lower case when one or more letters represent single words, e.g., d for delay, su for setup, rd for read, wr for write.

c. Multiple subscripts are upper case when each letter stands for a different word, e.g., SR for sense recovery and PLH for propagation delay from low to high.

Access Time (of a memory)

The time between the application of a specified input pulse during a read cycle and the availability of valid data signals at an output.

Example symbology:

$t_{a(ad)}$	Access time from address
$t_{a(E)}$	Access time from chip enable
$t_{a(S)}$	Access time from chip select

Clock Frequency

Maximum clock frequency, f_{max}
The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transistions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.

Current

High-level input current, I_{IH}
The current into* an input when a high-level voltage is applied to that input.

High-level output current, I_{OH}
The current into* an output with input conditions applied that according to the product specification will establish a high level at the output.

Low-level input current, I_{IL}
The current into* an input when a low-level voltage is applied to that input.

Low-level output current, I_{OL}
The current into* an output with input conditions applied that according to the product specification will establish a low level at the output.

Off-state output current, $I_{O(off)}$
The current flowing into* an output with input conditions applied that according to the product specification will cause the output switching element to be in the off state.
Note: This parameter is usually specified for open-collector outputs intended to drive devices other than logic circuits.

*Current out of a terminal is given as a negative value.

Off-state (high-impedance-state) output current (of a three-state output), I_{OZ}
The current into* an output having three-state capability with input conditions applied that according to the product specification will establish the high-impedance state at the output.

Short-circuit output current, I_{OS}
The current into* an output when that output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potential).

Supply current, I_{CC}
The current into* the V_{CC} supply terminal of an integrated circuit.

Cycle Time

Read cycle time, $t_{c(rd)}$ (see note)
The time interval between the start and end of a read cycle.

Read-write cycle time, $t_{c(rd,wr)}$ (see note)
The time interval between the start of a cycle in which the memory is read and new data are entered, and the end of that cycle.

Write cycle time, $t_{c(wr)}$ (see note)
The time interval between the start and end of a write cycle.

NOTE: The read, read-write, or write cycle time is the actual interval between two impulses and may be insufficient for the completion of operations within the memory. A minimum value is specified that is the shortest time in which the memory will perform its read and/or write function correctly.

Hold Time

Hold time, t_h
The interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.

NOTES: 1. The hold time is the actual time between two events and may be insufficient to accomplish the intended result. A minimum value is specified that is the shortest interval for which correct operation of the logic element is guaranteed.
2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of data and the active transition) for which correct operation of the logic element is guaranteed.

Output Enable and Disable Time

Output enable time (of a three-state output) to high level, t_{PZH} (or low level, t_{PZL})
The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined high (or low) level.

Output enable time (of a three-state output) to high or low level, t_{PZX}
The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to either of the defined active levels (high or low).

Output disable time (of a three-state output) from high level, t_{PHZ} (or low level, t_{PLZ})
The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined high (or low) level to a high-impedance (off) state.

*Current out of a terminal is given as a negative value.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

Output disable time (of a three-state output) from high or low level, t_{PXZ}
The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from either of the defined active levels (high or low) to a high-impedance (off) state.

Propagation Time

Propagation delay time, t_{PD}
The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level.

Propagation delay time, low-to-high-level output, t_{PLH}
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.

Propagation delay time, high-to-low-level output, t_{PHL}
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

Pulse Width

Pulse width, t_w
The time interval between specified reference points on the leading and trailing edges of the pulse waveform.

Example symbology:

$t_{w(cl)}$	Clear pulse width
$t_{w(wr)}$	Write pulse width

Recovery Time

Sense Recovery time, t_{SR}
The time interval needed to switch a memory from a write mode to a read mode and to obtain valid data signals at the output.

Release Time

Release time, $t_{release}$
The time interval between the release from a specified input terminal of data intended to be recognized and the occurrence of an active transition at another specified input terminal.
Note: When specified, the interval designated "release time" falls within the setup interval and constitutes, in effect, a negative hold time.

Setup Time

Setup time, t_{su}
The time interval between the application of a signal that is maintained at a specified input terminal and a consecutive active transition at another specified input terminal.
NOTES: 1. The setup time is the actual time between two events and may be insufficient to accomplish the setup. A minimum value is specified that is the shortest interval for which correct operation of the logic element is guaranteed.
2. The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the logic element is guaranteed.

Transition Time

Transition time, low-to-high-level, t_{TLH}
The time between a specified low-level voltage and a specified high-level voltage on a waveform that is changing from the defined low level to the defined high level.

Transition time, high-to-low-level, t_{THL}
The time between a specified high-level voltage and a specified low-level voltage on a waveform that is changing from the defined high level to the defined low level.

Voltage

High-level input voltage, V_{IH}
An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.
NOTE: A minimum is specified that is the least positive value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.

High-level output voltage, V_{OH}
The voltage at an output terminal with input conditions applied that according to the product specification will establish a high level at the output.

Input clamp voltage, V_{IK}
An input voltage in a region of relatively low differential resistance that serves to limit the input voltage swing.

Low-level input voltage, V_{IL}
An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables.
NOTE: A maximum is specified that is the most positive value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

Low-level output voltage, V_{OL}
The voltage at an output terminal with input conditions applied that according to the product specification will establish a low level at the output.

Negative-going threshold voltage, V_{T-}
The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, V_{T+}.

Off-state output voltage, $V_{O(off)}$
The voltage at an output terminal with input conditions applied that according to the product specification will cause the output switching element to be in the off state.
Note: This characteristic is usually specified only for outputs not having internal pull-up elements.

On-state output voltage, $V_{O(on)}$
The voltage at an output terminal with input conditions applied that according to the product specification will cause the output switching element to be in the on state.
Note: This characteristic is usually specified only for outputs not having internal pull-up elements.

Positive-going threshold voltage, V_{T+}
The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, V_{T-}.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

ACRONYMS AND MNEMONICS

AG	arithmetically greater than
AI	address input port
ALU	arithmetic logic unit
AO	address output port
BLWP	branch and load workspace pointer
CCO	counter-carry output
C	clock input (PROMs)
CE	chip enable
CIN	carry in
CL	clock
CLK	clock
CLA	carry look-ahead
CLR	clear
COUT	carry out
CPU	central processing unit
CRC	cyclic redundancy check
CRU	communications register unit
CRUIN	data input to CPU for CRU input operations
CRUOUT	data output from CPU for CRU output operations
CRUCLK	CRU-enable signal from CPU for CRU output operations
DBIN	data bus input
DO	data output port
DMA	direct memory access
DP	double precision
E	asynchronous chip enable
EQ	equal to
FPLA	field-programmable logic array
G	asynchronous output enable
INCMC	increment memory counter
INCPC	increment program counter
INT	interrupt
I/O	input or output
IP	intermediate position
INTREQ	interrupt request
LG	logically greater than
LCIR	left circulate
LD	load
LDCR	load CRU
LSA	left-shift arithmetic
LSB	least-significant bit
LSL	left-shift logical
LSP	least-significant position

MC	memory counter
MEMEN	memory enable
MSB	most-significant bit
MPX	multiplex
MSP	most-significant position
MUX	multiplexer
NC	not connected
OE	output enable
OV	overflow
PC	program counter
PLA	programmable logic array
POS	relative position control (MPS, IP, or LSP)
RCIR	right circulate
RSA	right-shift arithmetic
RSL	right-shift logical
RTWP	return workspace pointer instruction
S	asyncronous chip select
SBZ	set bit to zero
SBO	set bit to one
SP	single precision
ST	status register
STCR	store CRU
TB	test bit
WR	working register
WE	write enable
XOP	extended operation instruction
XWR	extended working register

Additional mnemonics or acronyms specifically relating to SBP 9900A instructions are found on pages 4–24 and 4–26.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

The following symbols are used in function tables on TI data sheets:

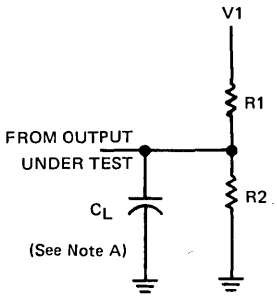
H	=	high level (steady state)
L	=	low level (steady state)
↑	=	transition from low to high level
↓	=	transition from high to low level
→	=	value/level or resulting value/level is routed to indicated destination
↶	=	value/level is re-entered
X	=	irrelevant (any input, including transitions)
Z	=	off (high-impedance) state of a 3-state output
a . . h	=	the level of steady-state inputs at inputs A through H respectively
Q_0	=	level of Q before the indicated steady-state input conditions were established
$\bar{Q}_0$	=	complement of Q_0 or level of $\bar{Q}$ before the indicated steady-state input conditions were established
Q_n	=	level of Q before the most recent active transition indicated by ↓ or ↑
⎍	=	one high-level pulse
⎎	=	one low-level pulse
TOGGLE	=	each output changes to the complement of its previous level on each active transition indicated by ↓ or ↑.

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

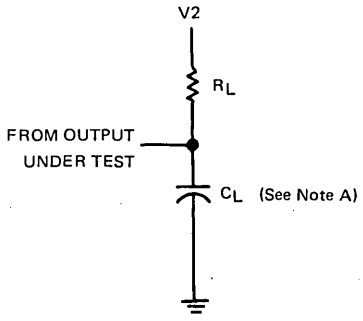
If, in the input columns, a row contains H, L, and/or X together with ↑ and/or ↓, this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, Q_0, or $\bar{Q}_0$), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output. (If the output is shown as a pulse, ⎍ or ⎎, the pulse follows the indicated input transition and persists for an interval dependent on the circuit.)

PARAMETER MEASUREMENT INFORMATION

FOR THREE-STATE OUTPUTS AND BI-STATE TOTEM-POLE OUTPUTS



LOAD CIRCUIT



THEVENIN EQUIVALENT CIRCUIT

VOLTAGE VALUES

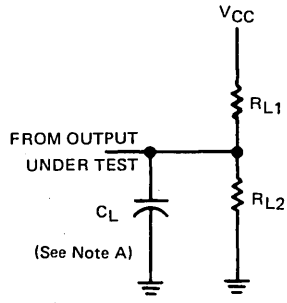
MEASUREMENTS	V_{CC}	V1	V2
t_{PLH} and t_{PHL}	5.5 V	5.5 V	3.7 V
	5.25 V	5.25 V	3.5 V
	4.75 V	4.75 V	3.2 V
	4.5 V	4.5 V	3 V
t_{PHZ} and t_{PZH}	ALL	0 V	0 V
t_{PLZ} and t_{PZL}	ALL	5 V	3.3 V

RESISTOR VALUES

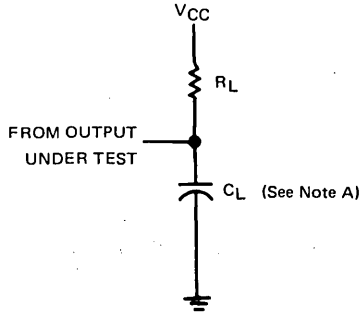
I_{OL} MAX†	R1	R2	R_L
24 mA	200 Ω	400 Ω	133 Ω
20 mA	240 Ω	480 Ω	160 Ω
16 mA	300 Ω	600 Ω	200 Ω
12 mA	400 Ω	800 Ω	267 Ω
8 mA	600 Ω	1.2 kΩ	400 Ω

†See Recommended Operating Conditions.

FOR OPEN-COLLECTOR OUTPUTS

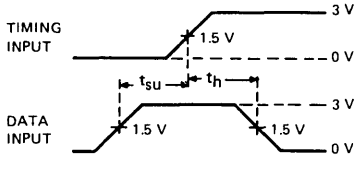


TEST CIRCUIT FOR USE WHEN R_{L1} AND R_{L2} ARE SPECIFIED

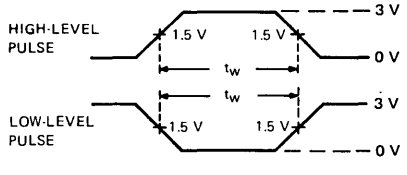


TEST CIRCUIT FOR USE WHEN SINGLE R_L IS SPECIFIED

NOTE A: C_L includes probe and jig capacitance.



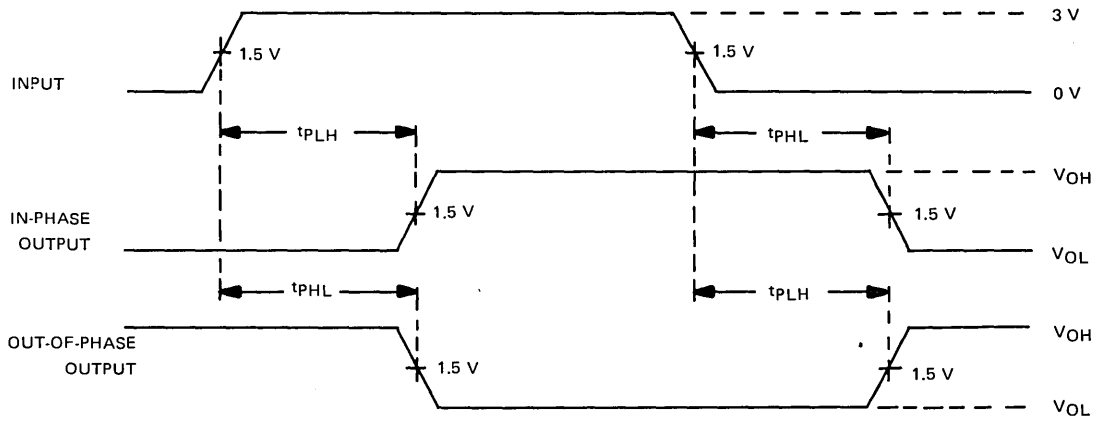
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



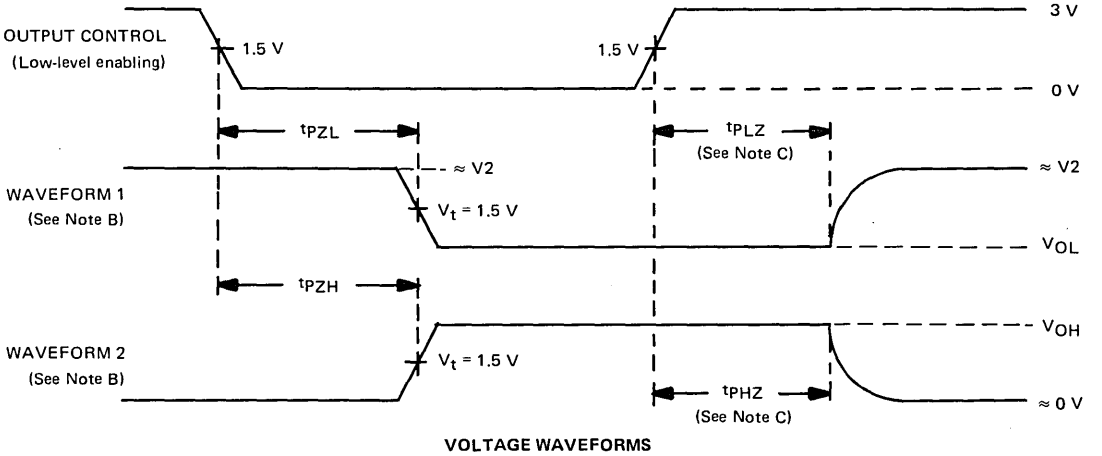
VOLTAGE WAVEFORMS
PULSE WIDTHS

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. TI normally measures t_{PLZ} and t_{PHZ} by reading at the 1.5-volt (V_t) point on the waveform and subtracting the RC time from the reading.
For t_{PLZ}, RCln $\frac{V2 - V_{OLmax}}{V2 - V_t}$ is subtracted from the reading.

For t_{PHZ}, RCln $\frac{V_{OHmin}}{V_t}$ is subtracted from the reading.

D. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

E. All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 1 MHz, $Z_{out} \approx 50\ \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.

Bipolar Memories

BIPOLAR MEMORIES

PAGE

Programmable Read-Only Memories (PROMs)

Random-Access Memories (RAMs)

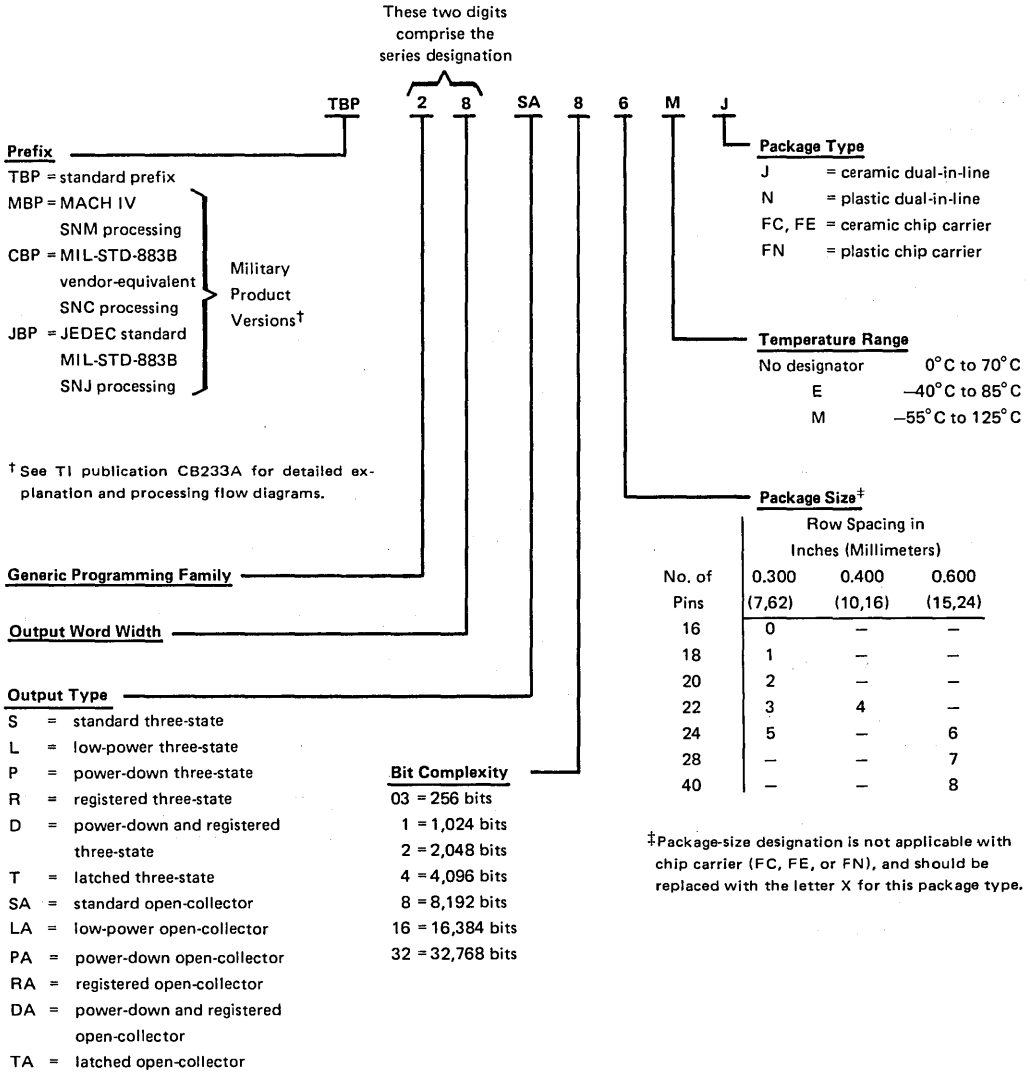
First-In First-Out Memories (FIFOs)

Code Converters

PROM NUMBERING SYSTEM AND ORDERING INSTRUCTIONS

To complement Texas Instruments continually expanding line of bipolar PROMs, a new numbering system is being implemented. This system provides the user with information regarding the generic programming family, bit density, organization, temperature range, and the size and type of package without the necessity of looking up this information in tables. Below is a guide for use of this new numbering system.

Factory orders for PROMs described in this book should include a type number as explained in the following example.



USER-PROGRAMMABLE READ-ONLY MEMORY (PROM) LINE SUMMARIES

STANDARD PROMS

NEW TYPE NUMBER	OLD TYPE NUMBER	OUTPUT TYPE†	BIT SIZE (ORGANIZATION)	TYPICAL PERFORMANCE		SEE PAGE
				ADDRESS ACCESS TIME	POWER DISSIPATION	
TBP18SA030	SN74S188	◇	256 Bits (32W X 8B)	25 ns	400 mW	2-7
TBP18S030	SN74S288	▽				
TBP14S10	SN74S287	▽	1024 Bits (256W X 4B)	42 ns	500 mW	
TBP14SA10	SN74S387	◇				
TBP24S10		▽		35 ns	375 mW	2-13
TBP24SA10		◇				
TBP18SA22	SN74S470	◇	2048 Bits (256W X 8B)	50 ns	550 mW	2-7
TBP18S22	SN74S471	▽				
TBP18S42	SN74S472	▽	4096 Bits (512W X 8B)	55 ns	600 mW	
TBP18SA42	SN74S473	◇				
TBP18S46	SN74S474	▽				
TBP18SA46	SN74S475	◇				
TBP28S42		▽		35 ns	500 mW	2-13
TBP28SA42		◇				
TBP28S45		▽				
TBP28S46		▽				
TBP28SA46		◇				
TBP24S41	SN74S476	▽	4096 Bits (1024W X 4B)	40 ns	475 mW	
TBP24SA41	SN74S477	◇				
TBP24S81	SN74S454	▽	8192 Bits (2048W X 4B)	45 ns	625 mW	
TBP24SA81	SN74S455	◇				
TBP28S86	SN74S478	▽	8192 Bits (1024W X 8B)	45 ns	625 mW	
TBP28SA86	SN74S479	◇				
TBP28S2708	SN74S2708	▽				
TBP28S85		▽		35 ns	550 mW	
TBP28S166		▽	16,384 Bits (2048W X 8B)	35 ns	650 mW	
TBP28SA166		◇				

LOW-POWER PROMS

NEW TYPE NUMBER	OLD TYPE NUMBER	OUTPUT TYPE†	BIT SIZE (ORGANIZATION)	TYPICAL PERFORMANCE		SEE PAGE
				ADDRESS ACCESS TIME	POWER DISSIPATION	
TBP28L22		▽	2048 Bits (256W X 8B)	45 ns	300 mW	2-13
TBP28LA22		◇				
TBP28L42		▽	4096 Bits (512W X 8B)	60 ns	250 mW	
TBP28L45		▽				
TBP28L86	SN74LS478	▽	8192 Bits (1024W X 8B)	80 ns	350 mW	
TBP28L85		▽		65 ns	275 mW	
TBP28L166		▽	16,384 Bits (2048W X 8B)	65 ns	350 mW	

† ◇ = open collector, ▽ = three state.

POWER-DOWN PROMS

NEW TYPE NUMBER	OLD TYPE NUMBER	OUTPUT TYPE†	BIT SIZE (ORGANIZATION)	TYPICAL PERFORMANCE		SEE PAGE
				ADDRESS ACCESS TIME	POWER DISSIPATION	
TBP28P42		▽	4096 Bits (512W X 8B)	35 ns	550/60 mW	2-13
TBP28P45		▽				
TBP28P85		▽	8192 Bits (1024W X 8B)	35 ns	550/60 mW	
TBP28P166		▽	16,384 Bits (2048W X 8B)	35 ns	650/125 mW	

REGISTERED PROMS

NEW TYPE NUMBER	OLD TYPE NUMBER	OUTPUT TYPE†	BIT SIZE (ORGANIZATION)	TYPICAL PERFORMANCE		SEE PAGE
				CLOCK TO OUTPUT	POWER DISSIPATION	
TBP28R45		▽	4096 Bits (512W X 8B)	20 ns	550 mW	2-13
TBP28R85		▽	8192 Bits (1024W X 8B)		600 mW	
TBP28R165 TBP28R166		▽	16,384 Bits (2048W X 8B)		700 mW	

READ/WRITE MEMORY (RAM) LINE SUMMARY

TYPE NUMBER	BIT SIZE (ORGANIZATION)	OUTPUT TYPE†	TYPICAL PERFORMANCE		SEE PAGE
			ADDRESS ACCESS TIME	POWER DISSIPATION	
SN5481A/SN7481A SN5484A/SN7484A	16 Bits X 1	◇	15 ns	224 mW	2-35
SN7489	64 Bits (16W X 4B)	◇	32 ns	378 mW	2-41
SN54LS189A/SN74LS189A		▽	50 ns	173 mW	2-45
SN54S189/SN74S189		▽	25 ns	375 mW	2-49
SN54LS219A/SN74LS219A		▽	50 ns	173 mW	2-45
SN54LS289A/SN74LS289A		◇	50 ns	173 mW	
SN54S289/SN74S289		◇	25 ns	375 mW	2-49
SN54LS319A/SN74LS319A		◇	50 ns	173 mW	2-45
SN74S201	256 Bits (256W X 1B)	▽	42 ns	500 mW	2-53
SN74S301		◇	42 ns	500 mW	

FIRST-IN/FIRST-OUT (FIFO) MEMORIES

TYPE NUMBER	BIT SIZE (ORGANIZATION)	OUTPUT TYPE†	TYPICAL PERFORMANCE				SEE PAGE
			DATA RATES		FALL THROUGH	POWER DISSIPATION	
			INPUT	OUTPUT			
SN54LS222/SN74LS222	64 Bits (16W X 4B)	▽	d-c to 10 MHz	d-c to 10 MHz	50 ns	433 mW	2-57
SN54LS224/SN74LS224		▽					
SN54LS227/SN74LS227		◇					
SN54LS228/SN74LS228		◇					
SN74S225	80 Bits (16W X 5B)	▽			190 ns	400 mW	2-65

† ◇ = open collector, ▽ = three state.

BIPOLAR PROM CROSS REFERENCE

AMD	TI
27S18	TBP18SA030
27S19	TBP18S030
27S20	TBP24SA10
27S21	TBP24S10
27S28	TBP28SA42
27S29	TBP28S42
27S30	TBP28SA46
27S31	TBP28S46
27S32	TBP24SA41
27S33	TBP24S41
27S180	TBP28SA86
27S181	TBP28S86
27S184	TBP24SA81
27S185	TBP24S81

FAIRCHILD	TI
93417	TBP24SA10
93427	TBP24S10
93438	TBP28SA46
93448	TBP28S46
93450	TBP28SA86
96451	TBP28S86
93452	TBP24SA41
93453	TBP24S41
93510	TBP28SA166
93511	TBP28S166

HARRIS	TI
7602	TBP18SA030
7603	TBP18S030
7608	TBP28S2708
7610	TBP24SA10
7611	TBP24S10
7640	TBP28SA46
7641	TBP28S46
7642	TBP24SA41
7643	TBP24S41
7648	TBP28SA42
7649	TBP28S42
7680	TBP28SA86
7681	TBP28S86
7684	TBP24SA81
7685	TBP24S81
76160	TBP28SA166
76161	TBP28S166

INTEL	TI
3601	TBP24SA10
3604	TBP28SA46
3605	TBP24SA41
3608	TBP28SA86
3621	TBP24S10
3624	TBP28S46
3625	TBP24S41
3628	TBP28S86
3636	TBP28S166

INTERSIL	TI
5600	TBP18SA030
5603	TBP24SA10
5605	TBP28SA46
5600	TBP18S030
5623	TBP24S10
5625	TBP28S46
56S06	TBP24SA41
56S26	TBP24S41

MMI	TI
6300-1	TBP24SA10
6301-1	TBP24S10
6308-1	TBP28LA22
6309-1	TBP28L22
6330-1	TBP18SA030
6331-1	TBP18S030
6340-1	TBP28SA46
6341-1	TBP28S46
6348-1	TBP28SA42
6349-1	TBP28S42
6352-1	TBP24SA41
6353-1	TBP24S41
6380-1	TBP28SA86
6381-1	TBP28S86

MOTO-ROLA	TI
7640	TBP28SA46
7641	TBP28S46
7642	TBP24SA41
7643	TBP24S41
7680	TBP28SA86
7681	TBP28S86

NATION-AL	TI
74S188	TBP18SA030
74S287	TBP24S10
74S288	TBP18S030
74S387	TBP24SA10
74S470	TBP28LA22
74S471	TBP28L22
74S472	TBP28S42
74S473	TBP28SA42
74S474	TBP28S46
74S475	TBP28SA46
74S572	TBP24SA41
74S573	TBP24S41
87S180	TBP28SA86
87S181	TBP28S86
87S184	TBP24SA81
87S185	TBP24S81
87S190	TBP28SA166
87S191	TBP28S166

RAY-THEON	TI
29600	TBP28LA22
29601	TBP28L22
29620	TBP28SA42
29621	TBP28S42
29624	TBP28SA46
29625	TBP28S46
29630	TBP28SA86
29631	TBP28S86
29635	TBP28S2708
29650	TBP24SA81
29651	TBP24S81
29660	TBP24SA10
29661	TBP24S10
29680	TBP28SA166
29681	TBP28S166

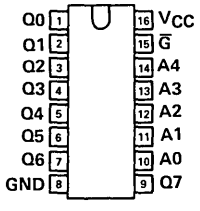
SIG-NETICS	TI
82S23	TBP18SA030
82S123	TBP18S030
82S126	TBP24SA10
82S129	TBP24S10
82S136	TBP24SA41
82S137	TBP24S41
82S140	TBP28SA46
82S141	TBP28S46
82S146	TBP28SA42
82S147	TBP28S42
82S180	TBP28SA86
82S181	TBP28S86
82LS181	TBP28L86
82S184	TBP24SA81
82S185	TBP24S81
82S190	TBP28SA166
82S191	TBP28S166
82S2708	TBP28S2708

- Titanium-Tungsten (Ti-W) Fuse Link For Reliable Low-Voltage Full Family Compatible Programming
- Full Decoding And Fast Chip Select Simplify System Design
- P-N-P Inputs For Reduced Loading On System Buffers/Drivers
- Applications Include:
  Microprogramming/Firmware Loaders
  Code Converters/Character Generators
  Translators/Emulators
  Address Mapping/Look-Up Tables

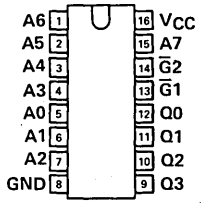
NEW TYPE NUMBER	OLD TYPE NUMBER	BIT SIZE (ORGANIZATION)	OUTPUT CONFIGURATION†	TYPICAL PERFORMANCE	
0°C to 70°C	0°C to 70°C			ADDRESS ACCESS TIME	POWER DISSIPATION
TBP18SA030 (J, N)▲	SN74S188 (J, N)	256 Bits (32W X 8B)	◇	25 ns	400 mW
TBP18S030 (J, N)▲	SN74S288 (J, N)		▽		
TBP14S10 (J, N)▲	SN74S287 (J, N)	1024 Bits (256W X 4B)	▽	42 ns	500 mW
TBP14SA10 (J, N)▲	SN74S387 (J, N)		◇		
TBP18SA22 (J, N)▲	SN74S470 (J, N)	2048 Bits (256W X 8B)	◇	50 ns	550 mW
TBP18S22 (J, N)▲	SN74S471 (J, N)		▽		
TBP18S42 (J, N)▲	SN74S472 (J, N)	4096 Bits (512W X 8B)	▽	55 ns	600 mW
TBP18SA42 (J, N)▲	SN74S473 (J, N)		◇		
TBP18S46 (J, N)▲	SN74S474 (J, N)	4096 Bits (512W X 8B)	▽	55 ns	600 mW
TBP18SA46 (J, N)▲	SN74S475 (J, N)		◇		

▲For full temperature parts (−55°C to +125°C) use suffix MJ. For devices with MIL-STD 883B processing (−55°C to +125°C) see page 2-3.
† ◇ = open collector, ▽ = three state.

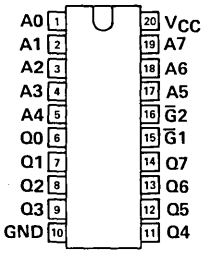
TBP18SA030, TBP18S030
256 BITS
(32 WORDS BY 8 BITS)
(TOP VIEW)



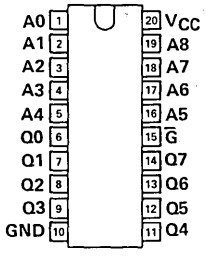
TBP14S10, TBP14SA10
1024 BITS
(256 WORDS BY 4 BITS)
(TOP VIEW)



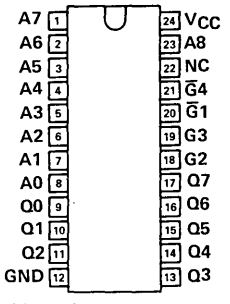
TBP18SA22, TBP18S22
2048 BITS
(256 WORDS BY 8 BITS)
(TOP VIEW)



TBP18S42, TBP18SA42
4096 BITS
(512 WORDS BY 8 BITS)
(TOP VIEW)



TBP18S46, TBP18SA46
4096 BITS
(512 WORDS BY 8 BITS)
(TOP VIEW)



Pin assignments for all of these memories are the same for the J and N packages. See Product Guide, Section 7, for chip carrier pin assignments.

description

These monolithic TTL programmable read-only memories (PROMs) feature titanium-tungsten (Ti-W) fuse links with each link designed to program in 100 microseconds. The Schottky-clamped versions of these PROMs offer considerable flexibility for upgrading existing designs or improving new designs as they feature full Schottky clamping for improved performance, low-current MOS-compatible p-n-p inputs, choice of bus-driving three-state or open-collector outputs, and improved chip-select access times.

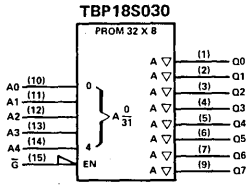
The high-complexity 2048- and 4096-bit PROMs can be used to significantly improve system density for fixed memories as all are offered in the 20-pin dual-in-line package having pin-row spacings of 0.300 inch (7,62 mm).

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

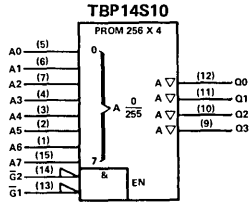
†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U.S. Patent Number 3,463,975.

logic symbols

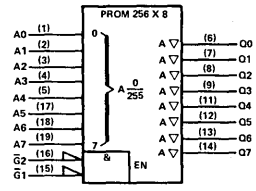
TBP18S030



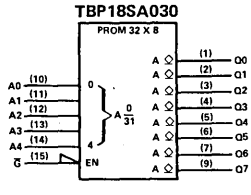
TBP14S10



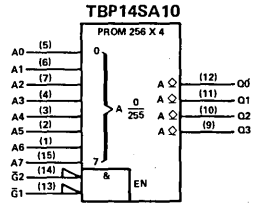
TBP18S22



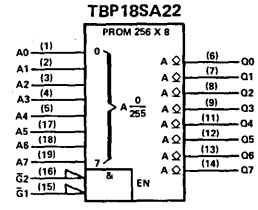
TBP18SA030



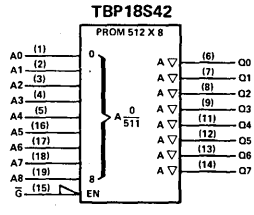
TBP14SA10



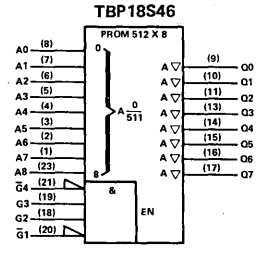
TBP18SA22



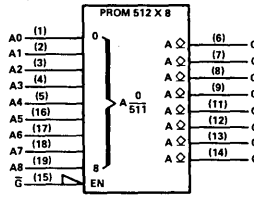
TBP18S42



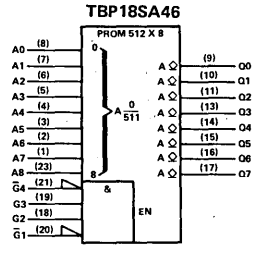
TBP18S46



TBP18SA42



TBP18SA46



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

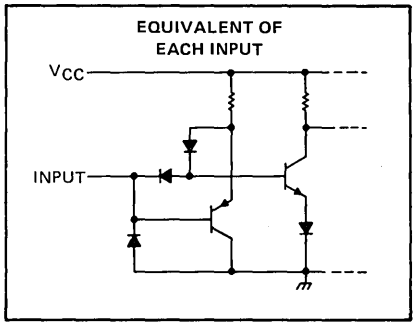
description (continued)

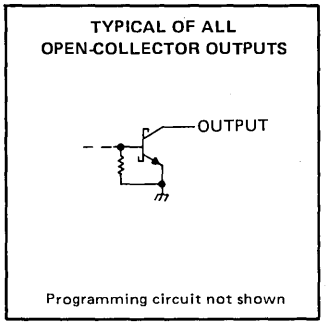
Data can be electronically programmed, as desired, at any bit location in accordance with the programming procedure specified. All PROMs, except the TBP14S10 and TBP14SA10 are supplied with a low-logic-level output condition stored at each bit location. The programming procedure open-circuits Ti-W metal links, which reverses the stored logic level at selected locations. The procedure is irreversible; once altered, the output for that bit location is permanently programmed. Outputs that have never been altered may later be programmed to supply the opposite output level. Operation of the unit within the recommended operating conditions will not alter the memory content.

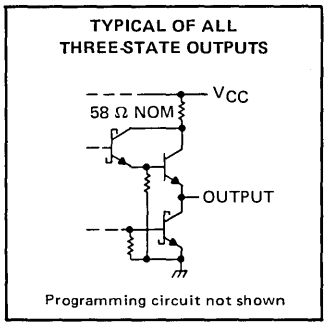
A low level at the chip-select input(s) enables each PROM. The opposite level at any chip-select input causes the outputs to be off.

The three-state output offers the convenience of an open-collector output with the speed of a totem-pole output; it can be bus-connected to other similar outputs yet it retains the fast rise time characteristic of the TTL totem-pole output. The open-collector output offers the capability of direct interface with a data line having a passive pull-up.

schematics of inputs and outputs







absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage (see Note 1) 7V
Input voltage 5.5V
Off-state output voltage 5.5V
Operating free-air temperature range: Full-temperature-range circuits . . . . . −55°C to 125°C
Commercial-temperature-range circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended conditions for programming the TBP18S', TBP18SA', TBP14S', and TBP14SA' PROMs

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC} (see Note 1)	Steady state	4.75	5	5.25	V
	Program pulse	9	9.25	9.5	
Input voltage	High level, V_{IH}	2.4		5	V
	Low level, V_{IL}	0		0.5	
Termination of all outputs except the one to be programmed		See load circuit (Figure 1)			
Voltage applied to output to be programmed, $V_{O(pr)}$ (see Note 2)		0	0.25	0.3	V
Duration of V_{CC} programming pulse X (see Figure 2 and Note 3)		15	25	100	μs
Programming duty cycle for Y pulse			25	35	%
Free-air temperature		20	25	30	°C

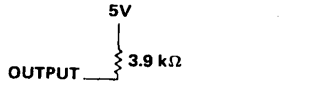
† Absolute maximum ratings.

NOTES: 1. Voltage values are with respect to network ground terminal. The supply voltage rating does not apply during programming.
2. The TBP18S030, TBP18SA030, TBP18SA22, TBP18S22, TBP18S42, TBP18SA42, TBP18S46 and TBP18SA46 are supplied with all bit locations containing a low logic level, and programming a bit changes the output of the bit to high logic level. The TBP14S10, TBP14SA10 are supplied with all bit outputs at a high logic level, and programming a bit changes it to a low logic level.
3. Programming is guaranteed if the pulse applied as 98 μs in duration.

step-by-step programming procedure for the TBP18SA030, TBP18S030, TBP14S10, TBP14SA10, TBP18SA22, TBP18S22, TBP18SA42, TBP18S42, TBP18S46, TBP18SA46

1. Apply steady-state supply voltage (V_{CC} = 5 V) and address the word to be programmed.
2. Verify that the bit location needs to be programmed. If not, proceed to the next bit.
3. If the bit requires programming, disable the outputs by applying a high-logic-level voltage to the chip-select input(s).
4. Only one bit location is programmed at a time. Connect each output not being programmed to 5 V through 3.9 kΩ and apply the voltage specified in the table to the output to be programmed. Maximum current into the programmer output is 150 mA.
5. Step V_{CC} to 9.25 nominal. Maximum supply current required during programming is 750 mA.
6. Apply a low-logic-level voltage to the chip-select input(s). This should occur between 1 μs and 1 ms after V_{CC} has reached its 9.25 level. See programming sequence of Figure 2.
7. After the X pulse time is reached, a high logic level is applied to the chip-select inputs to disable the outputs.
8. Within the range of 1 μs to 1 ms after the chip-select input(s) reach a high logic level, V_{CC} should be stepped down to 5 V at which level verification can be accomplished.
9. The chip-select input(s) may be taken to a low logic level (to permit program verification) 1 μs or more after V_{CC} reaches its steady-state value of 5 V.
10. At a Y pulse duty cycle of 35% or less, repeat steps 1 through 8 for each output where it is desired to program a bit.
11. Verify accurate programming of every word after all words have been programmed using V_{CC} values of 4.5 and 5.5 volts.

NOTE: Only one programming attempt per bit is recommended.



LOAD CIRCUIT FOR EACH OUTPUT NOT BEING PROGRAMMED OR FOR PROGRAM VERIFICATION

FIGURE 1 – LOAD CIRCUIT

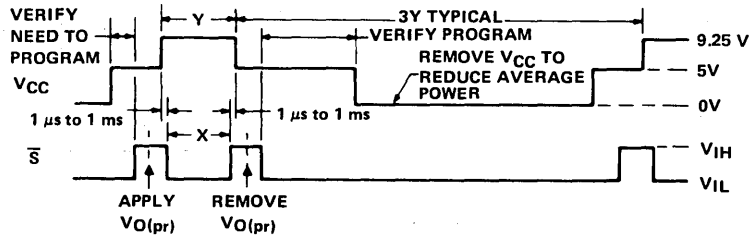


FIGURE 2 – VOLTAGE WAVEFORMS FOR PROGRAMMING

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

recommended operating conditions

PARAMETER		TBP14S10, TBP18S22			TBP18S030			TBP18S42, TBP18S46			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	MJ	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	J, N	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}	MJ			−2			−2			−2	mA
	J, N			−6.5			−6.5			−6.5	
Low-level output current, I_{OL}				16			20			12	mA
Operating free-air temperature, T_A	MJ	−55		125	−55		125	−55		125	°C
	J, N	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		FULL TEMP (MJ)			COMM. TEMP (J, N)			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = MAX	2.4	3.4		2.4	3.2		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = MAX			0.5			0.5	V
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_O = 2.4 V	V_{IH} = 2 V,			50			50	μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_O = 0.5 V	V_{IH} = 2 V,			−50			−50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V			25			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.5 V			−250			−250	μA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−30		−100	−30		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, Chip select(s) at 0 V, Outputs open, See Note 4	TBP14S10		100	135		100	135	mA
			TBP18S030		80	110		80	110	
			TBP18S22		110	155		110	155	
			TBP18S42, TBP18S46		120	155		120	155	

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

TYPE	TEST CONDITIONS	$t_{a(A)}$ (ns) Access time from address			$t_{a(S)}$ (ns) Access time from chip select (enable time)			t_{PXZ} (ns) Disable time from high or low level			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
TBP14S10MJ	C_L = 30 pF for $t_{a(A)}$ and $t_{a(S)}$, 5 pF for t_{PXZ}, See Page 1-12		42	75		15	40		12	40	ns
TBP14S10			42	65		15	35		12	35	ns
TBP18S030MJ			25	50		12	30		8	30	ns
TBP18S030			25	40		12	25		8	20	ns
TBP18S22MJ			50	80		20	40		15	35	ns
TBP18S22			50	70		20	35		15	30	ns
TBP18S42MJ, TBP18S46MJ			55	85		20	45		15	40	ns
TBP18S42, TBP18S46			55	75		20	40		15	35	ns

NOTE: MJ designates full-temperature-range circuits (formerly 54 Family), J and N designate commercial-temperature-range circuits (formerly 74 Family).

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

NOTE 4: The typical values of I_{CC} are with all outputs low.

recommended operating conditions

PARAMETER		TBP14SA10, TBP18SA22			TBP18SA030			TBP18SA42, TBP18SA46			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	MJ	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	J, N	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output voltage, V_{OH}				5.5			5.5			5.5	V
Low-level output current, I_{OL}				16			20			16	mA
Operating free-air temperature, T_A	MJ	−55		125	−55		125	−55		125	°C
	J, N	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.2	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	V_{OH} = 2.4 V			50	μA
			V_{OH} = 5.5 V			100	
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = MAX			0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.5 V			−250	μA
I_{CC}	Supply current	V_{CC} = MAX, Chip select(s) at 0 V, Outputs open, See Note 4	TBP18SA030		80	110	mA
			TBP14SA10		100	135	
			TBP18SA22		110	155	
			TBP18SA42, TBP18SA46		120	155	

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

TYPE	TEST CONDITIONS	$t_{a(A)}$ Access time from address			$t_{a(S)}$ Access time from chip select (enable time)			t_{PLH} Propagation delay time, low-to-high-level output from chip select (disable time)			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
TBP18SA030MJ	C_L = 30 pF, R_{L1} = 300 Ω, R_{L2} = 600 Ω, See Page 1-12		25	50		12	30		12	30	ns
TBP18SA030			25	40		12	25		12	25	ns
TBP14SA10MJ			42	75		15	40		15	40	ns
TBP14SA10			42	65		15	35		15	35	ns
TBP18SA22MJ			50	80		20	40		15	35	ns
TBPSA22			50	70		20	35		15	30	ns
TBP18SA42MJ, TBP18SA46MJ			55	85		20	45		15	40	ns
TBP18SA42, TBP18SA46			55	75		20	40		15	35	ns

NOTE: MJ designates full-temperature-range circuits (formerly 54 Family), J and N designate commercial-temperature-range circuits (formerly 74 Family).

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 4: The typical values of I_{CC} are with all output low.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

SERIES 24 AND 28
STANDARD, LOW-POWER, POWER-DOWN, REGISTERED PROGRAMMABLE READ-ONLY MEMORIES

JUNE 1981

- New, Expanded Family of Standard, Low Power, Power Down, And Registered PROMs
- Titanium-Tungsten (Ti-W) Fuse Links for Reliable Low-Voltage Full-Family-Compatible Programming
- Full Decoding And Fast Chip Select Simplify System Design
- P-N-P Inputs for Reduced Loading On System Buffers/Drivers
- Each PROM Supplied With a High Logic Level Stored At Each Bit Location
- Applications Include:
  Microprogramming/Firm Ware Loaders
  Code Converters/Character Generators
  Translators/Emulators
  Address Mapping/Look-Up Tables

STANDARD PROMS

TYPE NUMBER		OUTPUT CONFIGURATION‡	BIT SIZE (ORGANIZATION)	TYPICAL PERFORMANCE		
				ACCESS TIMES		POWER
NEW TYPE NUMBER	OLD TYPE NUMBER			ADDRESS	SELECT	DISSIPATION
TBP24S10 (J, N)▲		▽	1024 Bits (256W X 4B)	35 ns	20 ns	375 mW
TBP24SA10 (J, N)▲		◇				
TBP28S42 (J, N)▲		▽	4096 Bits (512W X 8B)	35 ns	20 ns	500 mW
TBP28SA42		◇				
TBP28S45 (J, N) †▲		▽				
TBP28S46		▽				
TBP28SA46		◇				
TBP24S41 (J, N)▲	SN74S476 (J, N)	▽	4096 Bits (1024W X 4B)	40 ns	20 ns	475 mW
TBP24SA41 (J, N)▲	SN74S477 (J, N)	◇				
TBP24S81 (J, N) ▲	SN74S454 (J, N)	▽	8192 Bits (2048W X 4B)	45 ns	20 ns	625 mW
TBP24SA81 (J, N) ▲	SN74S455 (J, N)	◇				
TBP28S86 (J, N) ▲	SN74S478 (J, N)	▽	8192 Bits (1024W X 8B)	45 ns	20 ns	625 mW
TBP28SA86 (J, N) ▲	SN74S479 (J, N)	◇				
TBP28S2708 (J, N)	SN74S2708 (J, N)	▽				
TBP28S85 (J, N) †▲		▽		35 ns	15 ns	550 mW
TBP28S166 (J, N) ▲		▽	16,384 Bits (2048W X 8B)	35 ns	15 ns	650 mW
TBP28SA166		◇				

LOW POWER PROMS

TYPE NUMBER		OUTPUT CONFIGURATION‡	BIT SIZE (ORGANIZATION)	TYPICAL PERFORMANCE		
				ACCESS TIMES		POWER
NEW TYPE NUMBER	OLD TYPE NUMBER			ADDRESS	SELECT	DISSIPATION
TBP28L22 (J, N)▲		▽	2048 Bits (256W X 8B)	45 ns	20 ns	375 mW
TBP28LA22		◇				
TBP28L42 (J,N) ▲		▽	4096 Bits (512W X 8B)	60 ns	30 ns	250 mW
TBP28L45 (J, N) †▲		▽				
TBP28L46 (J,N) ▲		▽				
TBP28L86 (J, N)▲	SN74LS478 (J, N)	▽	8192 Bits (1024W X 8B)	80 ns	35 ns	350 mW
TBP28L85 (J, N) †▲		▽		65 ns	30 ns	275 mW
TBP28L166 (J, N) †▲		▽	16,384 Bits (2048W X 8B)	65 ns	30 ns	350 mW

All PROMs are also available in chip carriers.

† NOTE — Electrical parameters for these devices are design goals only.

▲ NOTE — These devices available as full-temperature-range and as high-rel processed devices (use suffix MJ or NJ).

‡ ◇ = open collector, ▽ = three state.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U.S. Patent Number 3,463,975.

POWER DOWN PROMS

TYPE NUMBER		OUTPUT CONFIGURATION‡	BIT SIZE (ORGANIZATION)	TYPICAL PERFORMANCE		
NEW TYPE NUMBER	OLD TYPE NUMBER			ACCESS TIMES		POWER
				ADDRESS	SELECT	DISSIPATION
TBP28P42 (J, N)†		▽	4096 Bits (512W X 8B)	35 ns	55 ns	500/60 mW
TBP28P45 (J, N)†		▽				
TBP28P85 (J, N)†		▽	8192 Bits (1024W X 8B)	35 ns	55 ns	550/60 mW
TBP28P166 (J, N)†		▽	16,384 Bits (2048W X 8B)	35 ns	55 ns	650/125 mW

REGISTERED PROMS

TYPE NUMBER		OUTPUT CONFIGURATION‡	BIT SIZE (ORGANIZATION)	TYPICAL PERFORMANCE		
NEW TYPE NUMBER	OLD TYPE NUMBER			CLOCK TO OUTPUT	ADDRESS SET UP TIME	POWER DISSIPATION
TBP28R45 (J, N)†		▽	4096 Bits (512W X 8B)	20 ns	20 ns	550 mW
TBP28R85 (J, N)†		▽	8192 Bits (1024W X 8B)			600 mW
TBP28R165 (J, N)† TBP28R166 (J, N)†		▽	16,384 Bits (2048W X 8B)			700 mW

All PROMs are also available in chip carriers.

† Electrical parameters for these devices are design goals only.

‡ ▽ = three state.

description

The new 24 and 28 Series of monolithic TTL programmable read-only memories (PROMs) feature an expanded selection of standard, low-power, power-down, and registered PROMs. This expanded PROM family provides the system designer with considerable flexibility in upgrading existing designs or optimizing new designs. Featuring proven titanium-tungsten (Ti-W) fuse links with low-current MOS-compatible p-n-p inputs, all family members utilize a common programming technique designed to program each link with a 100-microsecond pulse.

The new 4096-bit and 8192-bit PROMs are offered in 24-pin 300-mil-wide packages, greatly improving system density for large PROM arrays. For systems requiring even higher levels of complexity and density, the 16,384-bit PROMs provide twice the bit density of the 8192-bit PROMs in 24-pin 600-mil-wide packages. All PROMs are supplied with a logic-high output level stored at each bit location. The programming procedure open-circuits Ti-W metal links, which reverses the stored logic level at selected locations. The procedure is irreversible; once altered, the output for that bit location is permanently programmed. Outputs that have never been altered may later be programmed to supply the opposite output level. Operation of the unit within the recommended operating conditions will not alter the memory content.

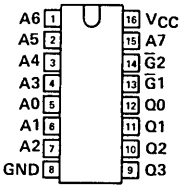
Active level(s) at the chip-select input(s) (S or $\overline{S}$) enables all of the outputs. An inactive level at any chip-select input causes all outputs to be off. On power-down PROMs, active level(s) at the chip-enable input(s) (E or $\overline{E}$) power up the device and enables all of the outputs. An inactive level at any chip-enable input causes all the outputs to be off and the PROM to be in a reduced-power standby mode.

The three-state output offers the convenience of an open-collector output with the speed of a totem-pole output; it can be bus connected to other similar outputs, yet it retains the fast rise time characteristics of the TTL totem-pole output. The open-collector output offers the capability of direct interface with a data line having a passive pull-up.

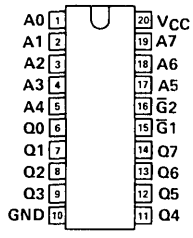
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

PIN ASSIGNMENTS (TOP VIEWS)

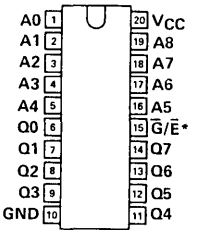
TBP24S10, TBP24SA10
1024 BITS
(256 WORDS BY 4 BITS)



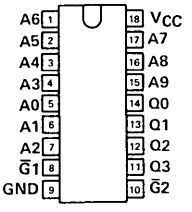
TBP28L22, TBP28LA22
2048 BITS
(256 WORDS BY 8 BITS)



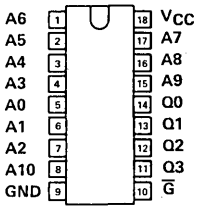
TBP28S42, TBP28SA42
TBP28L42, TBP28P42*
4096 BITS
(512 WORDS BY 8 BITS)



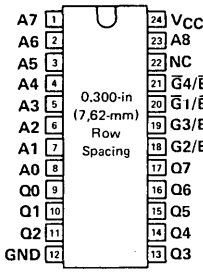
TBP24S41, TBP24SA41
4096 BITS
(1024 WORDS BY 4 BITS)



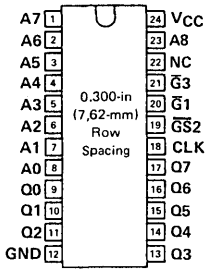
TBP24S81, TBP24SA81
8192 BITS
(2048 WORDS BY 4 BITS)



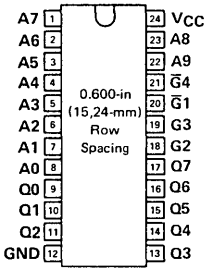
TBP28S45, TBP28L45, TBP28P45*,
TBP28S46, TBP28SA46
4096 BITS
(512 WORDS BY 8 BITS)



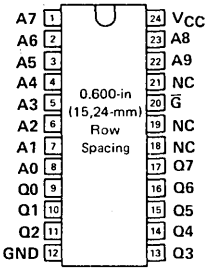
TBP28R45
4096 BITS
(512 WORDS BY 8 BITS)



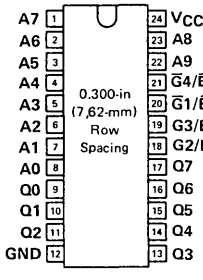
TBP28S86, TBP28SA86, TBP28L86
8192 BITS
(1024 WORDS BY 8 BITS)



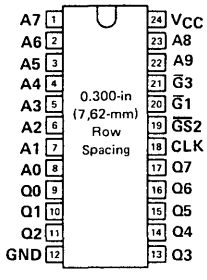
TBP28S2708
8192 BITS
(1024 WORDS BY 8 BITS)



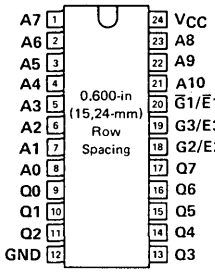
TBP28S85, TBP28L85, TBP28P85*
8192 BITS
(1024 WORDS BY 8 BITS)



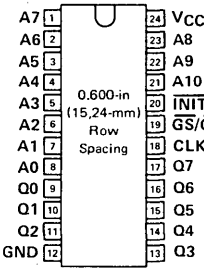
TBP28R85
8192 BITS
(1024 WORDS BY 8 BITS)



TBP28S166, TBP28SA166,
TBP28L166, TBP28P166*
16,384 BITS
(2048 WORDS BY 8 BITS)



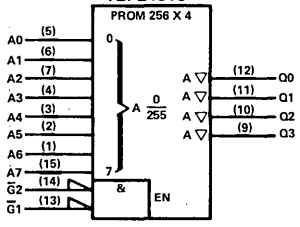
TBP28R165
TBP28R166*
16,384 BITS
(2048 WORDS BY 8 BITS)



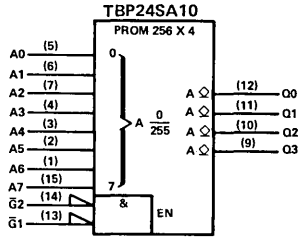
Pin assignments for all of these memories are the same for the J and N packages. See Product Guide, Section 7, for chip carrier pin assignments.
* For those pins having dual designations, the designation to the right of the virgule (/) applies only to the type number(s) immediately followed by an asterisk (*) above the pinout drawing.
nc = no internal connection

logic symbols

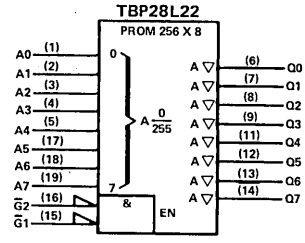
TBP24S10



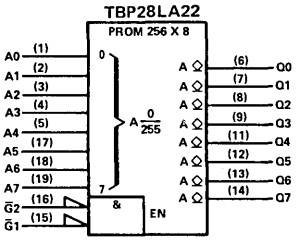
TBP24SA10



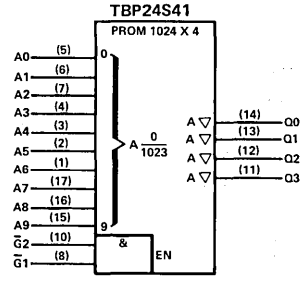
TBP28L22



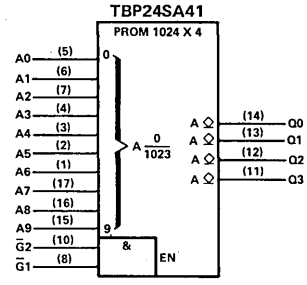
TBP28LA22



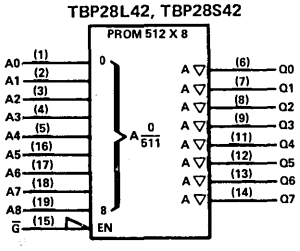
TBP24S41



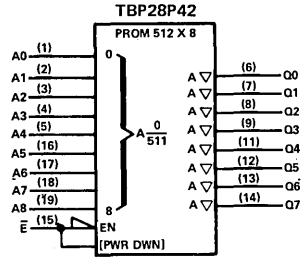
TBP24SA41



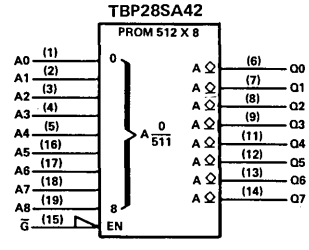
TBP28L42, TBP28S42



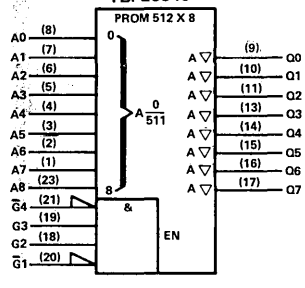
TBP28P42



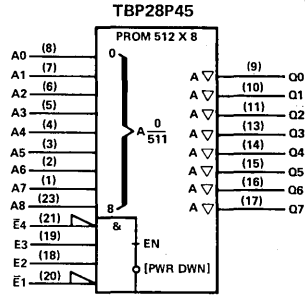
TBP28SA42



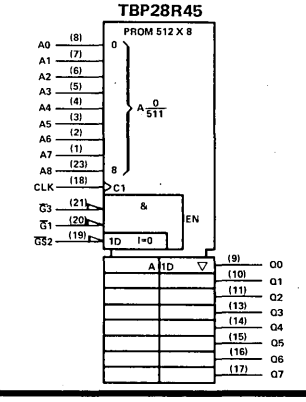
TBP28L45, TBP28S45, TBP28S46



TBP28P45



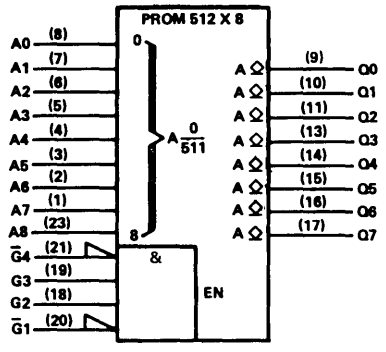
TBP28R45



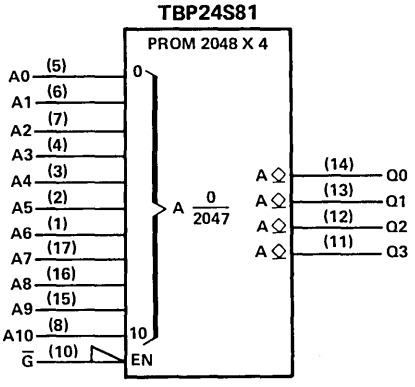
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

logic symbols

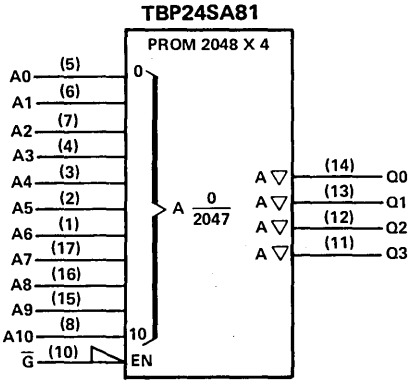
TBP28SA46



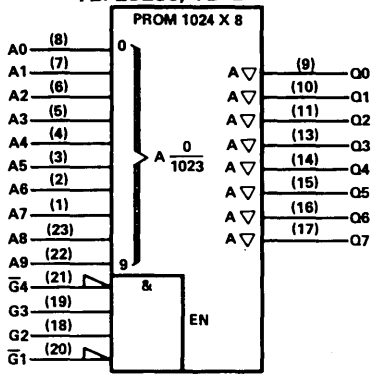
TBP24S81



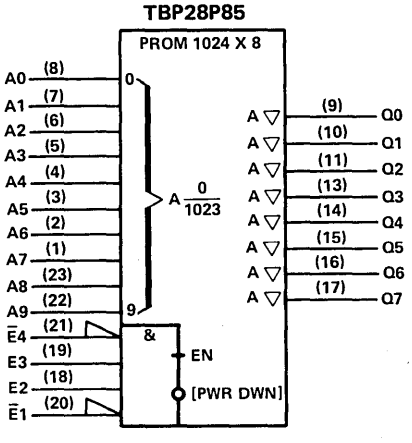
TBP24SA81



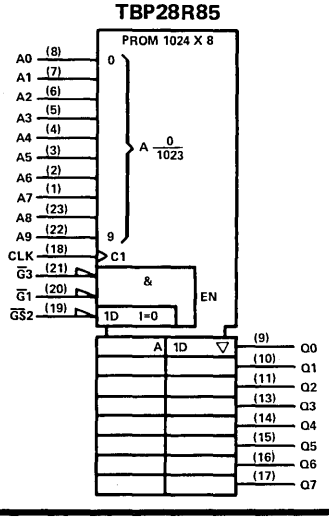
TBP28L85, TBP28S85,
TBP28L86, TBP28S86



TBP28P85



TBP28R85

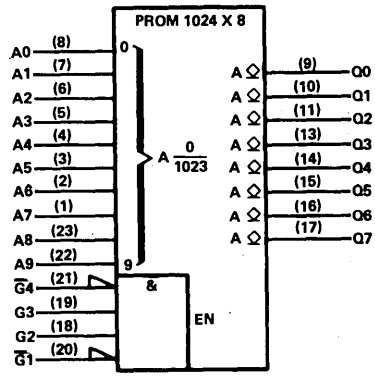


2

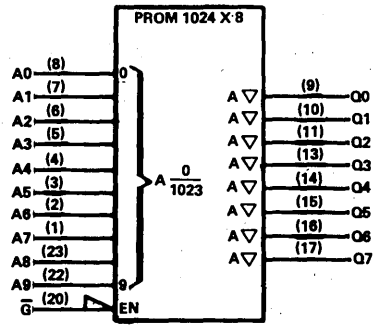
681

logic symbols

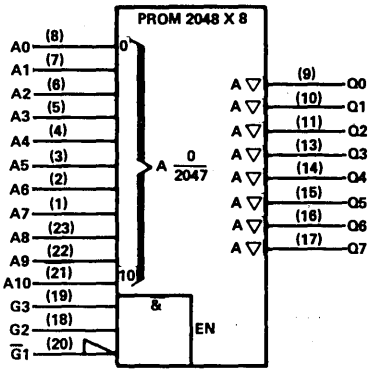
TBP28SA86



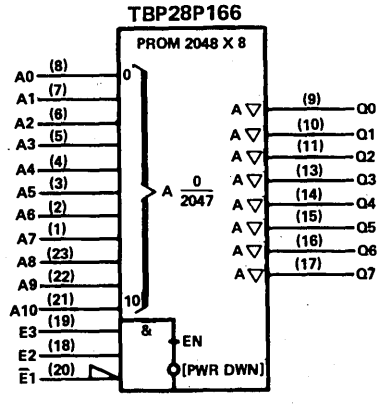
TBP28S2708



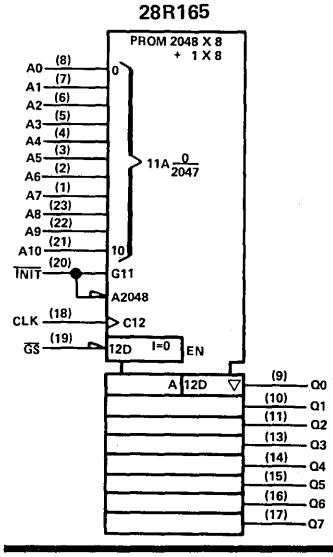
TBP28L166, TBP28S166



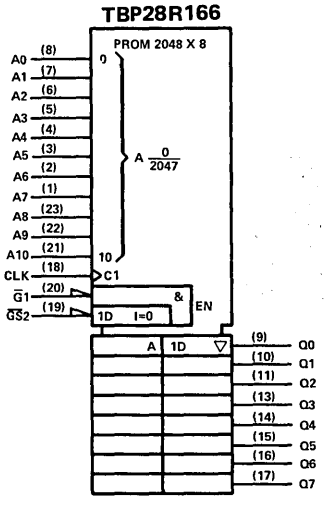
TBP28P166



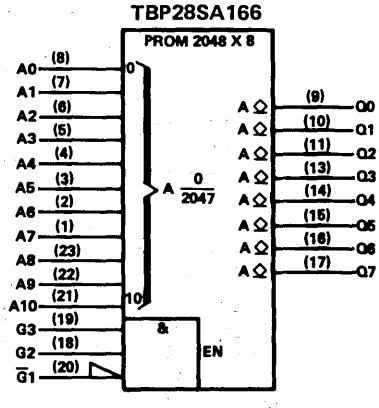
28R165



TBP28R166



TBP28SA166



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

standard PROMs

The standard PROM members of Series 24 and 28 offer the highest performance for applications requiring the uncompromised speed of Schottky technology. The fast chip-select access times allow additional decoding delays to occur without degrading speed performance.

low-power PROMs

To upgrade systems utilizing MOS EPROMs or MOS PROMs, the low-power PROM family offers the increased output drive and speed performance of bipolar technology and the reduced power dissipation necessary to implement effective upgrades. Additionally, low-power PROMs offer substantially reduced power dissipation over standard PROMs with minimal speed penalty.

power-down PROMs

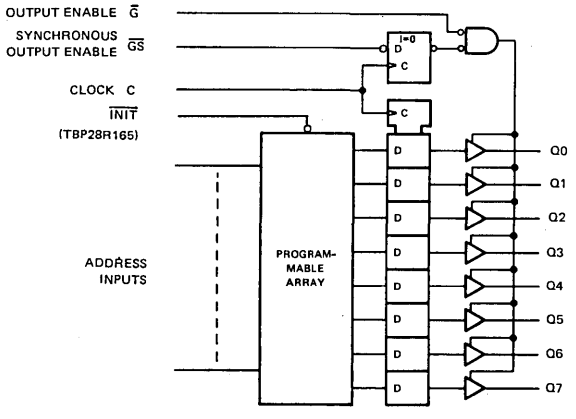
For power-sensitive systems requiring the speed performance of the standard PROM members as well as reduced system power dissipation, the power-down PROM members allow a 75% or better reduction in power dissipation when disabled while providing standard PROM speed performance when enabled. The power-down and power-up functions are sequenced to occur with the outputs at a high-impedance state. The enable (power-up) function provides adequate performance to allow power-up to occur during the normal read access time precluding any degradation in memory speed performance.

registered PROMs

For microprogrammed pipelined systems the Series 24 and 28 registered PROM members offer the system designer reduced package count and improved system performance by incorporating the pipeline register onto the PROM chip. Available in 4096-bit, 8192-bit and 16,384-bit densities, all registered PROMs are provided with synchronous and asynchronous output controls ($\overline{GS}$ and $\overline{G}$) allowing maximum flexibility in data bus control.

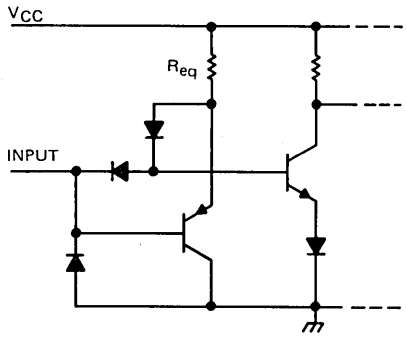
When power is first applied, the edge-triggered latch for the synchronous output control is cleared, and the Q outputs are placed in a high-impedance state. To read data, the address is set up, the synchronous output enable, $\overline{GS}$, is taken low, and a low-to-high transition on the clock (C) input causes the selected data to be stored in the registers. That same transition causes the outputs to be enabled if asynchronous output enable $\overline{G}$ is low. At this time the address may be changed and a new word addressed without a affecting the register contents. If the synchronous output enable is high at the time of a low-to-high clock transition, the outputs will be disabled to the high-impedance state. They may be disabled at any time by taking output enable $\overline{G}$ high. If the initialize control input ($\overline{INIT}$) is low at the time of a low-to-high clock transition, a user-defined code, including all "zeros", all "ones", or a combination of "zeros" and "ones", will be stored in the register.

block diagram (positive logic)



schematics of inputs and outputs

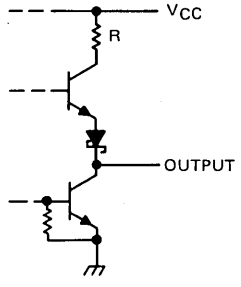
EQUIVALENT OF EACH INPUT



	R_{eq}
LOW-POWER PROMS	20 kΩ NOM
ALL OTHERS	8 kΩ NOM

Programming circuits not shown

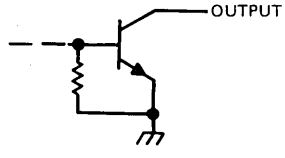
EQUIVALENT OF 3-STATE OUTPUTS



	R
LOW-POWER PROMS	130 Ω NOM
ALL OTHERS	58 Ω NOM

Programming circuit not shown

EQUIVALENT OF OPEN-COLLECTOR OUTPUTS



Programming circuit not shown

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage (see Note 1)	7 V
Input voltage	5.5 V
Chip-select peak input voltage (S, S1, S2) (see Note 2)	11 V
Off-state output voltage	5.5 V
Off-state peak output voltage (see Note 2)	17.25 V
Operating free-air temperature range: Full-temperature-range circuits (MJ)	−55°C to 125°C
Commercial-temperature-range circuits (J, N)	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. These ratings apply only under the conditions described in the programming procedure.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

recommended operating conditions

PARAMETER		TBP24SA10			TBP24SA41			TBP24SA81			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	MJ	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	J, N	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output voltage, V_{OH}				5.5			5.5			5.5	V
Low-level output current, I_{OL}	MJ			16			16			16	mA
	J, N			16			16			16	
Operating free-air temperature range	MJ	−55		125	−55		125	−55		125	°C
	J, N	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TBP24SA10			TBP24SA41			TBP24SA81			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.2			−1.2			−1.2	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	V_O = 2.4 V			50			50			50	μA
			V_O = 5.5 V			100			100			100	
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{CL} = MAX	MJ			0.5			0.5			0.5	V
			J, N			0.45			0.5			0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				25			25			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V				−250			−250			−250	μA
I_{CC}	Supply current	V_{CC} = MAX	MJ		75	100		95	140		125	175	mA
			J, N		75	100		95	140		125	175	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

TYPE		TEST CONDITIONS	$t_{a(A)}$ Access time from address			$t_{a(S)}$ Access time from chip select (enable time)			t_{PLH} Propagation delay time, low-to-high-level output from chip select			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TBP24SA10	MJ	C_L = 30 pF, R_{L1} = 300 Ω, R_{L2} = 600 Ω, See Page 1-12		35	75		20	40		15	40	ns
	J, N			35	65		20	35		15	35	
TBP24SA41	MJ			40	75		20	40		20	40	ns
	J, N			40	60		20	30		20	30	
TBP24SA81	MJ			45	95		20	50		20	50	ns
	J, N			45	70		20	40		20	40	
TBP24SA81-55				43	55		20	40		20	40	ns

NOTE: MJ designates full-temperature-range circuits (formerly 54 Family), J and N designate commercial-temperature-range circuits (formerly 74 Family).

recommended operating conditions

PARAMETER		TBP28SA42			TBP28SA46			TBP28SA86			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	MJ	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	J, N	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output voltage, V_{OH}				5.5			5.5			5.5	V
Low-level output current, I_{OL}	MJ			16			16			12	mA
	J, N			16			16			12	
Operating free-air temperature range	MJ	−55		125	−55		125	−55		125	°C
	J, N	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TBP28SA42			TBP28SA46			TBP28SA86			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.2			−1.2			−1.2	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	V_O = 2.4 V			50			50			50	μA
			V_O = 5.5 V			100			100			100	
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{CL} = MAX				0.5			0.5			0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				25			25			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V				−250			−250			−250	μA
I_{CC}	Supply current	V_{CC} = MAX	MJ		105	135		100	135		125	175	mA
			J, N		105	135		100	135		125	175	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

TYPE	TEST CONDITIONS	$t_{a(A)}$ Access time from address			$t_{a(S)}$ Access time from chip select (enable time)			t_{PLH} Propagation delay time, low-to-high-level output from chip select			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TBP28SA42	C_L = 30 pF,		35	65		20	35		15	35	ns
TBP28SA46	R_{L1} = 300 Ω,		35	65		20	35		15	35	ns
TBP28SA86	R_{L2} = 600 Ω,		45	70		20	40		20	40	ns
TBP28SA86-60	See Page 1-12		43	60		20	40		20	40	ns

NOTE: MJ designates full-temperature-range circuits (formerly 54 Family), J and N designate commercial-temperature-range circuits (formerly 74 Family).

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

recommended operating conditions

PARAMETER		TBP28SA166 MIN	TBP28SA166 NOM	TBP28SA166 MAX	UNIT
Supply voltage, V_{CC}	MJ	4.5	5	5.5	V
	J, N	4.75	5	5.25	
High-level output voltage, V_{OH}				5.5	V
Low-level output current, I_{OL}	MJ			16	mA
	J, N			16	
Operating free-air temperature range	MJ	−55		125	°C
	J, N	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TBP28SA166 MIN	TBP28SA166 TYP‡	TBP28SA166 MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.2	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	V_O = 2.4 V			50	μA
			V_O = 5.5 V			100	
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = MAX				0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				25	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V				−250	μA
I_{CC}	Supply current	V_{CC} = MAX	MJ		130	175	mA
			J, N		130	175	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

TYPE	TEST CONDITIONS	$t_{a(A)}$ Access time from address MIN	TYP	MAX	$t_{a(S)}$ Access time from chip select (enable time) MIN	TYP	MAX	t_{PLH} Propagation delay time, low-to-high-level output from chip select MIN	TYP	MAX	UNIT
TBP28SA166	C_L = 30 pF, R_{L1} = 300 Ω, R_{L2} = 600 Ω, See Page 1-12		35	80		15	40		12	40	ns

NOTE: MJ designates full-temperature-range circuits (formerly 54 Family), J and N designate commercial-temperature-range circuits (formerly 74 Family).

recommended operating conditions

PARAMETER		TBP24S10			TBP24S41			TBP24S81			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	MJ	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	J, N	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}	MJ			−2			−2			−2	mA
	J, N			−6.5			−3.2			−3.2	
Low-level output current, I_{OL}	MJ			16			16			16	mA
	J, N			16			16			16	
Operating free-air temperature range	MJ	−55		125	−55		125	−55		125	°C
	J, N	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TBP24S10			TBP24S41			TBP24S81			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.2			−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX		2.4	3.1		2.4	3.1		2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = MAX				0.5			0.5			0.5	V
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 2.4 V				50			50			50	μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 0.5 V				−50			−50			−50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				25			25			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V				−250			−250			−250	μA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	MJ	−30		−100	−15		−100	−15		−100	mA
			J, N	−30		−100	−20		−100	−20		−100	
I_{CC}	Supply current	V_{CC} = MAX	MJ		75	100		95	140		125	175	mA
			J, N		75	100		95	140		125	175	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

TYPE		TEST CONDITIONS		$t_{a(A)}$ Access time from address			$t_{a(S)}$ Access time from chip select (enable time)			t_{PXZ} Disable time			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TBP24S10	MJ	C_L = 30 pF for $t_{a(A)}$ and $t_{a(S)}$, C_L = 5 pF for t_{PXZ}	See Page 1-12		35	75		20	40		15	40	ns
	J, N				35	55		20	25		15	25	
TBP24S41	MJ				40	75		20	40		20	40	ns
	J, N				40	60		20	30		20	30	
TBP24S81	MJ				45	85		20	50		20	50	ns
	J, N				45	70		20	40		20	40	
TBP24S81-55					43	55		20	40		20	40	ns

NOTE: MJ designates full-temperature-range circuits (formerly 54 Family), J and N designate commercial-temperature-range circuits (formerly 74 Family).

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

recommended operating conditions

PARAMETER		TBP28S42, TBP28S45*			TBP28S46			TBP28S85*			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	MJ	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	J, N	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}	MJ			−2			−2			−2	mA
	J, N			−6.5			−6.5			−3.2	
Low-level output current, I_{OL}	MJ			16			16			16	mA
	J, N			16			16			16	
Operating free-air temperature range	MJ	−55		125	−55		125	−55		125	°C
	J, N	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TBP28S42 TBP28S45*			TBP28S46			TBP28S85*			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.2			−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX		2.4	3.1		2.4	3.1		2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = MAX				0.5			0.5			0.5	V
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 2.4 V				50			50			50	μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 0.5 V				−50			−50			−50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				25			25			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V				−250			−250			−250	μA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	MJ	−30		−100	−15		−100	−15		−100	mA
			J, N	−30		−100	−20		−100	−20		−100	
I_{CC}	Supply current	V_{CC} = MAX	MJ		100	135		100	135		110		mA
			J, N		100	135		100	135		110		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

TYPE		TEST CONDITIONS		$t_{a(A)}$ Access time from address			$t_{a(S)}$ Access time from chip select (enable time)			t_{PXZ} Disable time			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TBP28S42 TBP28S45*		C_L = 30 pF for $t_{a(A)}$ and $t_{a(S)}$, C_L = 5 pF for t_{PXZ}	See Page 1-12		35	60		20	45		15	40	ns
TBP28S46	MJ				35	70		20	45		15	40	ns
	J, N				35	60		20	35		15	35	ns
TBP28S85*					35			15			12		ns

*Electrical parameters for these devices are design goals only.
NOTE: MJ designates full-temperature-range circuits (formerly 54 Family), J and N designate commercial-temperature-range circuits (formerly 74 Family).

recommended operating conditions

PARAMETER		TBP28S86			TBP28S166			TBP28S2708			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	MJ	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	J, N	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}	MJ			−2			−2			−2	mA
	J, N			−3.2			−3.2			−3.2	
Low-level output current, I_{OL}	MJ			12			16			12	mA
	J, N			12			16			12	
Operating free-air temperature range	MJ	−55		125	−55		125	−55		125	°C
	J, N	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TBP28S86			TBP28S166			TBP28S2708			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.2			−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX		2.4	3.1		2.4	3.1		2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = MAX				0.5			0.5			0.5	V
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 2.4 V				50			50			50	μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 0.5 V				−50			−50			−50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				25			25			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V				−250			−250			−250	μA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	MJ	−15		−100	−15		−100	−15		−100	mA
			J, N	−20		−100	−20		−100	−20		−100	
I_{CC}	Supply current	V_{CC} = MAX	MJ		125	175		130			125	175	mA
			J, N		125	175		130			125	175	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

TYPE	TEST CONDITIONS		$t_{a(A)}$ Access time from address			$t_{a(S)}$ Access time from chip select (enable time)			t_{PXZ} Disable time			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TBP28S86	C_L = 30 pF for $t_{a(A)}$ and $t_{a(S)}$, C_L = 5 pF for t_{PXZ}	See Page 1-12		45	70		20	40		20	40	ns
TBP28S86-60				43	60		20	40		20	40	ns
TBP28S166				35	75		15	40		15	40	ns
TBP28S166-55				33	55		15	40		15	40	ns
TBP28S2708				45	70		20	40		20	40	ns

NOTE: MJ designates full-temperature-range circuits (formerly 54 Family), J and N designate commercial-temperature-range circuits (formerly 74 Family).

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

recommended operating conditions

PARAMETER		TBP28LA22			UNIT
		MIN	NOM	MAX	
Supply voltage, V_{CC}	MJ	4.5	5	5.5	V
	J, N	4.75	5	5.25	
High-level output voltage, V_{OH}				5.5	V
Low-level output current, I_{OL}	MJ			16	mA
	J, N			16	
Operating free-air temperature range	MJ	−55		125	°C
	J, N	0		70	

2

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TBP28LA22			UNIT
				MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.2	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	V_O = 2.4 V			50	μA
			V_O = 5.5 V			100	
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = MAX				0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				25	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V				−250	μA
I_{CC}	Supply current	V_{CC} = MAX	MJ		75	100	mA
			J, N		75	100	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

TYPE		TEST CONDITIONS	$t_{a(A)}$ Access time from address			$t_{a(S)}$ Access time from chip select (enable time)			t_{PLH} Propagation delay time, low-to-high-level output from chip select			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TBP28LA22	MJ	C_L = 30 pF, R_{L1} = 300 Ω, R_{L2} = 600 Ω, See Page 1-12		45	80		20	40		15	35	ns
	J, N			45	75		20	35		15	30	

NOTE: MJ designates full-temperature-range circuits (formerly 54 Family), J and N designate commercial-temperature-range circuits (formerly 74 Family).

recommended operating conditions

PARAMETER		TBP28L22			TBP28L42 , TBP28L46			TBP28L85*			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	MJ	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	J, N	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}	MJ			−2			−1			−1	mA
	J, N			−6.5			−1.6			−1.6	
Low-level output current, I_{OL}	MJ			16			8			8	mA
	J, N			16			8			8	
Operating free-air temperature range	MJ	−55		125	−55		125	−55		125	°C
	J, N	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TBP28L22			TBP28L42 TBP28L46			TBP28L85*			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.2			−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX		2.4	3.1		2.4	3.1		2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = MAX				0.5			0.5			0.5	V
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 2.4 V				50			50			50	μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 0.5 V				−50			−50			−50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				25			25			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V				−250			−250			−250	μA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	MJ	−30		−100	−10		−100	−10		−100	mA
			J, N	−30		−100	−10		−100	−10		−100	
I_{CC}	Supply current	V_{CC} = MAX	MJ		75	100		50			55		mA
			J, N		75	100		50			55		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

TYPE		TEST CONDITIONS		$t_{a(A)}$ Access time from address			$t_{a(S)}$ Access time from chip select (enable time)			t_{PXZ} Disable time			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TBP28L22	MJ	C_L = 30 pF for $t_{a(A)}$ and $t_{a(S)}$, C_L = 5 pF for t_{PXZ}	See Page 1-12		45	75		20	40		15	35	ns
	J, N				45	70		20	35		15	30	ns
TBP28L42 TBP28L46	MJ				55	110		25	60		25	50	ns
	J, N				55	95		25	60		25	40	
TBP28L85*					65			30			25		ns

* Electrical parameters for these devices are design goals only.
NOTE: MJ designates full-temperature-range circuits (formerly 54 Family), J and N designate commercial-temperature-range circuits (formerly 74 Family).

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

recommended operating conditions

PARAMETER		TBP28L86			TBP28L166*			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	MJ	4.5	5	5.5	4.5	5	5.5	V
	J, N	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}	MJ			−1			−1	mA
	J, N			−1.6			−1.6	
Low-level output current, I_{OL}	MJ			4			8	mA
	J, N			8			8	
Operating free-air temperature range	MJ	−55		125	−55		125	°C
	J, N	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TBP28L86			TBP28L166*			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX		2.4	3.1		2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = MAX				0.5			0.5	V
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 2.4 V				50			50	μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 0.5 V				−50			−50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				25			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V				−250			−250	μA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	MJ	−10		−100	−10		−100	mA
			J, N	−10		−100	−10		−100	
I_{CC}	Supply current	V_{CC} = MAX	MJ		55			70		mA
			J, N		55			70		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

TYPE		TEST CONDITIONS		$t_{a(A)}$ Access time from address			$t_{a(S)}$ Access time from chip select (enable time)			t_{PXZ} Disable time			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TBP28L86	MJ	C_L = 30 pF for $t_{a(A)}$ and $t_{a(S)}$	See Page 1-12		85	175		55	135		50	90	ns
	J, N				85	130		55	90		50	75	
TBP28L166*		C_L = 5 pF for t_{PXZ}			65			30			25		ns

*Electrical parameters for these devices are design goals only.

NOTE: MJ designates full-temperature-range circuits (formerly 54 family), J and N designate commercial-temperature-range circuits (formerly 74 Family).

recommended operating conditions

PARAMETER		TBP28P42*, TBP28P46*			TBP28P85*			TBP28P166*			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	MJ	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	J, N	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}	MJ			−2			−2			−2	mA
	J, N			−3.2			−3.2			−3.2	
Low-level output current, I_{OL}	MJ			16			16			16	mA
	J, N			16			16			16	
Operating free-air temperature range	MJ	−55		125	−55		125	−55		125	°C
	J, N	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TBP28P42* TBP28P46*			TBP28P85*			TBP28P166*			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.2			−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX		2.4	3.1		2.4	3.1		2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = MAX				0.5			0.5			0.5	V
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 2.4 V				50			50			50	μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 0.5 V				−50			−50			−50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				25			25			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V				−250			−250			−250	μA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	MJ	−15		−100	−15		−100	−15		−100	mA
			J, N	−20		−100	−20		−100	−20		−100	
I_{CC}	Supply current, Power Up	V_{CC} = MAX			100			110			130		mA
	Supply current, Power Down				12			12			25		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

TYPE	TEST CONDITIONS		$t_{a(A)}$ Access time from address			$t_{a(E)}$ Access time from chip enable (enable time)			t_{PXZ} Disable time			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TBP28P42* TBP28P46*	C_L = 30 pF for $t_{a(A)}$ and $t_{a(E)}$, C_L = 5 pF for t_{PXZ}	See Page 1-12		35			55			12		ns
TBP28P85*				35			55			12		ns
TBP28P166*				35			55			12		ns

*Electrical parameters for these devices are design goals only.

NOTE: MJ designates full-temperature-range circuits (formerly 54 Family), J and N designate commercial-temperature-range circuits (formerly 74 Family).

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

recommended operating conditions

PARAMETER		TBP28R46*			TBP28R85*			TBP28R165* TBP28R166*			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	MJ	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	J, N	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}	MJ			−2			−2			−2	mA
	J, N			−3.2			−3.2			−3.2	
Low-level output current, I_{OL}	MJ			16			16			16	mA
	J, N			16			16			16	
Clock pulse width high, $t_{w(CH)}$		20			20			20			ns
Clock pulse width low, $t_{w(CL)}$		20			20			20			ns
$\overline{INIT}$ pulse width low, $t_{w(IL)}$ ('R165 only)								20			ns
Address setup time, $t_{su(A)}$		20			20			20			ns
Chip select setup time, $t_{su(S)}$		0			0			0			ns
Address hold time, $t_{h(A)}$		0			0			0			ns
Chip select hold time, $t_{h(S)}$		5			5			5			ns
Operating free-air temperature range	MJ	−55		125	−55		125	−55		125	°C
	J, N	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TBP28R46*			TBP28R85*			TBP28R165* TBP28R166*			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.2			−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX		2.4	3.1		2.4	3.1		2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = MAX	MJ			0.5			0.5			0.5	V
			J, N			0.5			0.5			0.5	
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 2.4 V				50			50			50	μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 0.5 V				−50			−50			−50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				25			25			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V				−250			−250			−250	μA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	MJ	−15		−100	−15		−100	−15		−100	mA
			J, N	−20		−100	−20		−100	−20		−100	
I_{CC}	Supply current	V_{CC} = MAX	MJ		110			120			140		mA
			J, N		110			120			140		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.
* Electrical and switching parameters for these devices are design goals only.
NOTE: MJ designates full-temperature-range circuits (formerly 54 Family), J and N designate commercial-temperature-range circuits (formerly 74 Family).

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

types TBP28R46*, TBP28R85*, TBP28R165*, TBP28R166*

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{a(C)}$	Access time from clock	C_L = 30 pF, See Page 1-12		20		ns
$t_{PXZ(C)}$	Output disable time from clock			20		ns
$t_{PZX(C)}$	Output enable time from clock			20		ns
$t_{PXZ(G)}$	Output disable time from $\overline{G}$			12		ns
$t_{PZX(G)}$	Output enable time from $\overline{G}$			15		ns

* Electrical and switching parameters for these devices are design goals only.

PARAMETER MEASUREMENT INFORMATION

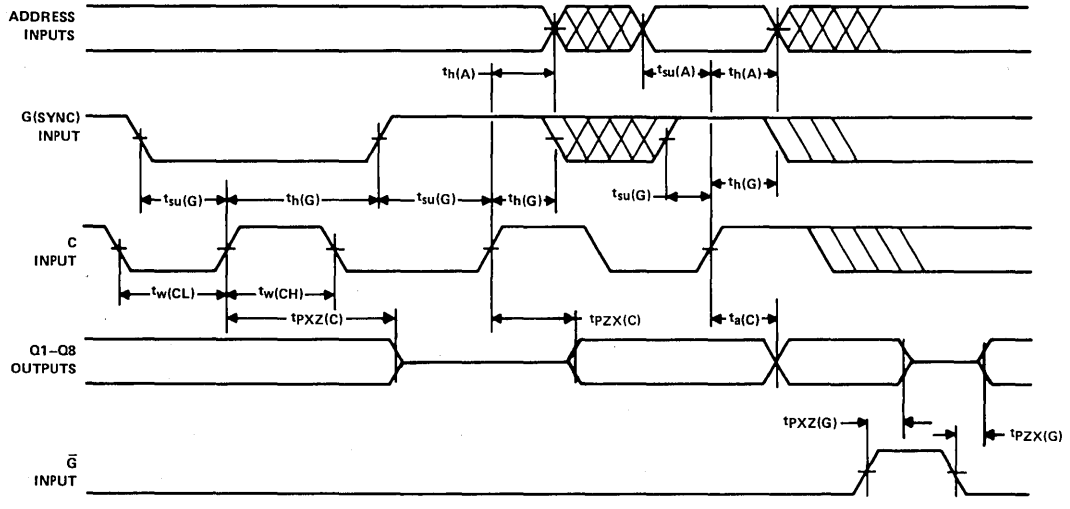


FIGURE 1 – SWITCHING WAVEFORMS FOR TYPES TBP28R45, TBP28R85, TBP28R165, AND TBP28R166

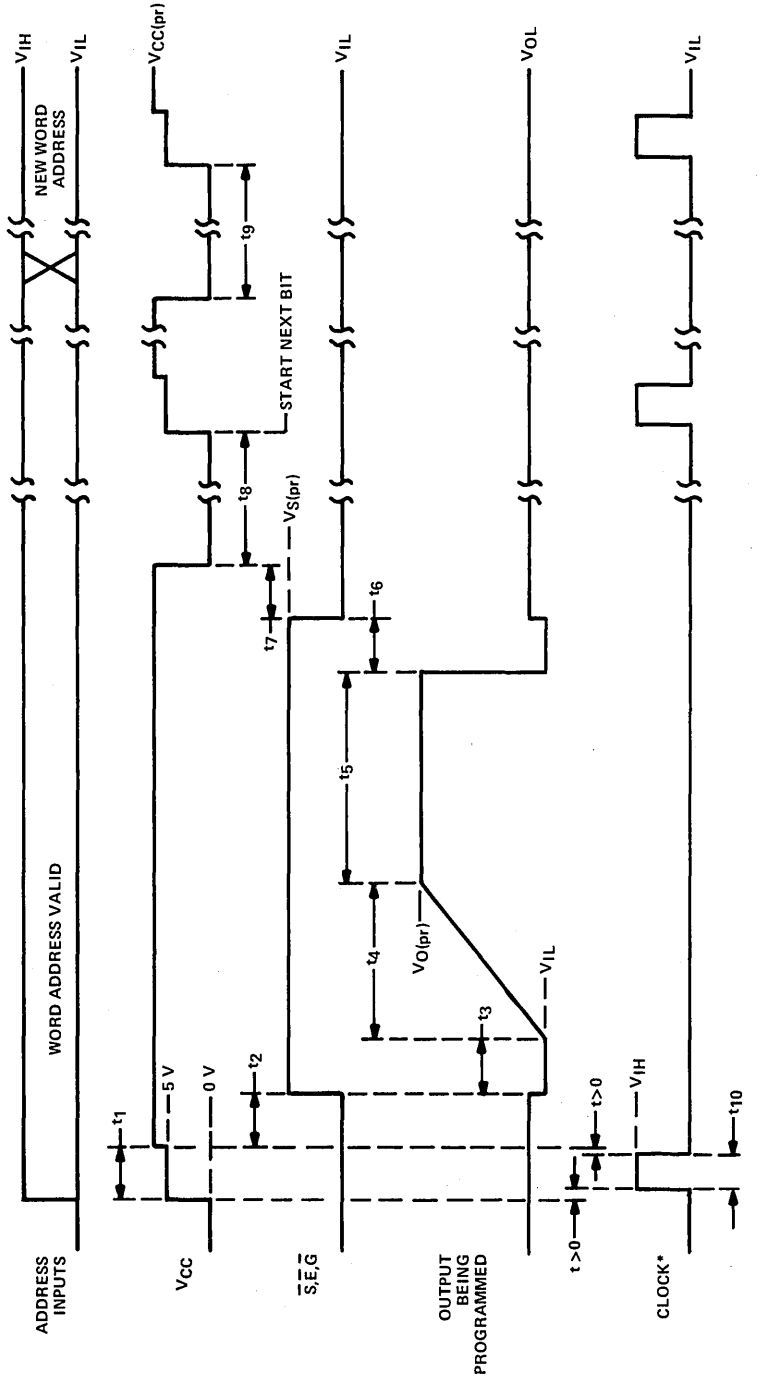
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

recommended conditions for programming (see Figure 2)

		MIN	NOM	MAX	UNIT
Steady-state supply voltage	V_{CC}	4.75	5	5.25	V
Input voltage	V_{IH}	3	4	5	V
	V_{IL}	0	0	0.5	
Voltage at all outputs except the one to be programmed		0	0	0.5	V
Supply voltage level to program a bit	$V_{CC(pr)}$	5.75	6	6.25	V
Select or enable level to program a bit	$V_{S(pr)}$	9.75	10	11	V
Output level during interval t_5	$V_{O(pr)}$	15.75	16	16.25	V
Supply voltage during verification (see step 14)	Low	4.4	4.5	4.6	V
	High	5.4	5.5	5.6	
Time for V_{CC} to settle and to verify need to program	t_1	0	5	10	μs
Time from V_{CC} = 6 V until chip select (enable) is at 10 V	t_2	5	5	10	μs
Time from chip select (enable) high to start of program ramp	t_3	0.1	5	10	μs
Ramp time, output program pulse	t_4	10	15	20	μs
Duration of output program pulse	t_5	15	20	20	μs
Time from end of program pulse to chip select (enable) low	t_6	5	5	10	μs
Time from chip select (enable) low to V_{CC} = 0 V	t_7	0.1	5	5	μs
Time for cooling between bits	t_8	30	50	100	μs
Time for cooling between words	t_9	30	50		μs
Clock pulse duration (registered PROMs)	t_{10}	1	2	3	μs
Free-air temperature	T_A	20	25	30	°C

step-by-step programming instruction (see Figure 2)

1. Address the word to be programmed, apply 5 volts to V_{CC} and active levels to all chip select (S and $\overline{S}$) or chip enable (E and $\overline{E}$) inputs.
2. Verify the status of a bit location by checking the output level. For registered PROMs a clock must be applied to the clock pin to verify the output level.
3. Decrease V_{CC} to 0 volts.
4. For bit locations that do not require programming, skip steps 5 through 11.
5. Increase V_{CC} to $V_{CC(pr)}$ with a minimum current capability of 250 milliamperes.
6. Apply $V_{S(pr)}$ to all the $\overline{S}$, $\overline{E}$ or $\overline{G}$ inputs. $I_I \leqslant 25$ milliamperes. Active-high enables may be left high.
7. Connect all outputs, except the one to be programmed, to V_{IL}. Only one bit is to be programmed at a time.
8. Apply the output programming pulse for 20 microseconds. Minimum current capability of the programming supply should be 250 milliamperes.
9. After terminating the output pulse, disconnect all outputs from V_{IL} conditions.
10. Reduce the voltage at $\overline{S}$, $\overline{E}$, or $\overline{G}$ inputs to V_{IL}.
11. Decrease V_{CC} to 0 volts.
12. Return to step 4 until all outputs in the word have been programmed.
13. Repeat steps 2 through 11 for each word in memory.
14. Verify programming of every word after all words have been programmed using V_{CC} values of 4.5 and 5.5 volts. Note that registered PROMs must be clocked to verify the output condition.



*Registered PROMs only. Rise and fall times should be ≤ 1 μs.

FIGURE 2 – TIMING DIAGRAM AND VOLTAGE WAVEFORMS FOR PROGRAMMING SEQUENCE

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TYPES SN5481A, SN5484A, SN7481A, SN7484A
16-BIT RANDOM-ACCESS MEMORIES

D1332, DECEMBER 1972

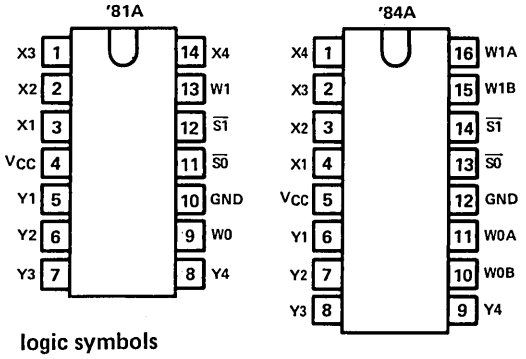
description

Each of these 16-bit active-element memories is a high-speed, monolithic, transistor-transistor-logic (TTL) array of 16 flip-flops and two write amplifiers interconnected to form a scratch-pad memory with direct-address and nondestructive read-out. These devices are interchangeable with and replace SN5481, SN7481, SN5484, and SN7484, but feature diode-clamped inputs, improved switching speeds, and lower supply current requirements.

The flip-flops are arranged in a four-by-four matrix with each flip-flop representing one bit of 16 words. Four X-address lines and four Y-address lines permit the address of one bit at a time. Each flip-flop, composed of two cross-coupled three-emitter transistors, is used to store one bit. To determine if a logic 1 or logic 0 has been stored, it is necessary to know which one of the two flip-flop transistors is conducting. One emitter of each of these transistors serves as the sensing output. All 16 of the logic 1 sensing outputs are connected to the sense 1 (S_1) amplifier input and all 16 of the logic 0 sensing outputs are connected to the sense 0 (S_0) amplifier input. The two remaining emitters of each transistor are used to complete the matrix connections necessary for the X- and Y-address lines. Address line inputs are normally held low and currents from all conducting flip-flop transistors flow out of these address lines.

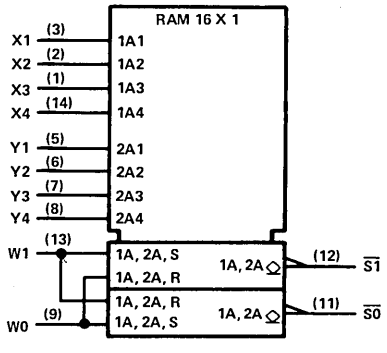
To address a flip-flop both the X- and Y-address lines associated with that flip-flop are taken to a high level. Due to the matrix nature of the circuit, at least one address line of all flip-flops except the one being addressed will continue to remain at a low level and no change will occur in those flip-flops. But, in the addressed flip-flop, the current in the conducting transistor diverts from the address lines to the appropriate sense line and then to one of the sense amplifiers. Thus, either the sense 1 amplifier or the sense 0 amplifier is activated. When this occurs, the output of the activated sense amplifier drops from a high logic level to a low logic level. The memory is nondestructive as the states of the flip-flops are not disturbed during sensing. The memory is volatile and information will be lost if the supply voltage is removed.

SN54'. . . J PACKAGE
SN74'. . . J OR N PACKAGE
(TOP VIEWS)

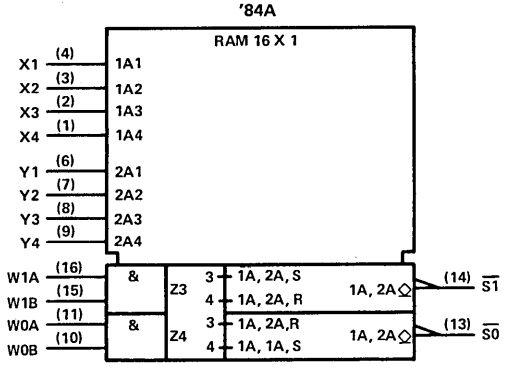


logic symbols

'81A



'84A



To store new information in a flip-flop, it is necessary to address it and apply a high-level voltage to the appropriate write amplifier. (The SN5484A and SN7484A have gated write-amplifier inputs). The output of the write amplifier responds by dropping to a low logic level. Since all Sense 0 lines are connected to the output of the write 0 amplifier and all sense 1 lines are connected to the output of the write 1 amplifier, a low level at the output of a write amplifier

781

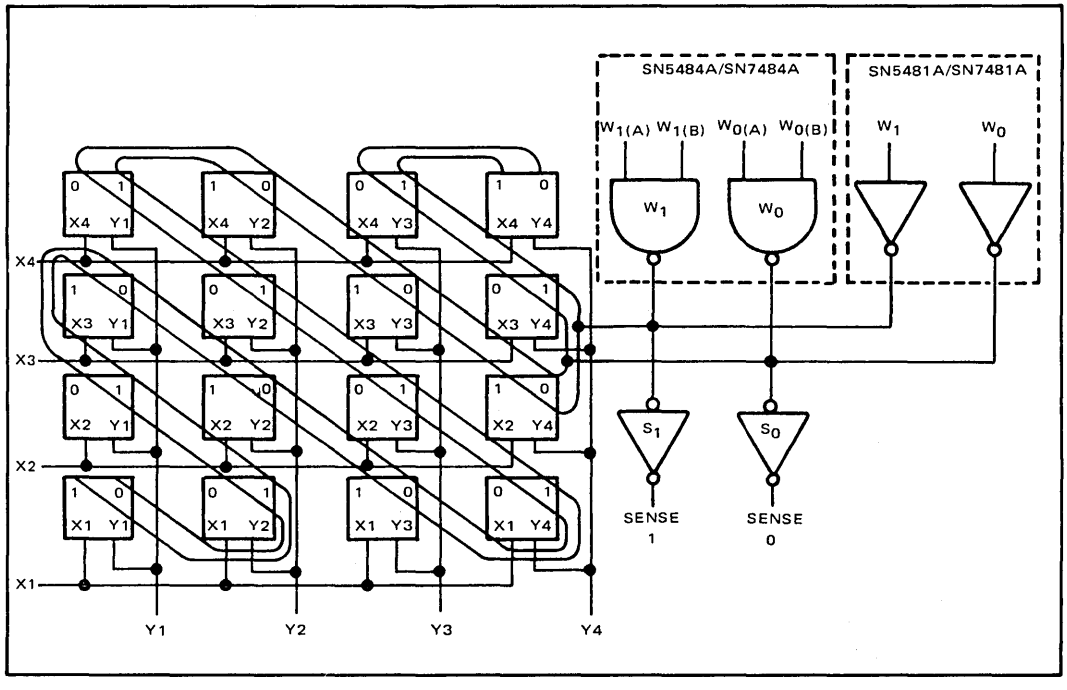
description (continued)

will cause the emitters of all flip-flop transistors connected to that amplifier to go low. In all the flip-flops except the one being addressed, this low voltage has no effect since at least one other emitter on each of the flip-flop transistors is held low by the address lines. Two possibilities exist with the flip-flop that is addressed. The flip-flop may already be in the desired state, in which case no change occurs. If the flip-flop must be changed from one state to the other, the low voltage applied to the emitter of the transistor which is not conducting turns that transistor on causing the other transistor to turn off.

Since the connection between the output of the write amplifier and the sense line is common to the input of the sense amplifier, the memory cannot be used to provide information on the state of a bit while the write amplifiers are activated.

A number of active-element memories may be paralleled to form the desired matrix size (number of words) and to form the desired word length (number of bits). All inputs and outputs are compatible with most DTL and TTL circuits. Average power dissipation is typically 225 milliwatts, and the open-collector outputs may be wire-AND connected to similar outputs. Internal circuitry of the write and sense amplifiers are operated within their linear range to improve speed. Sensing propagation delay times are typically 12 nanoseconds when operated at full fan-out and 30 picofarads of circuit capacitance. The SN5481A and SN5484A circuits are designed for operation over the full military temperature range of −55°C to 125°C; the SN7481A circuits are designed for operation from 0°C to 70°C.

logic diagram



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
High-level output voltage . . . . . 5.5 V
Operating free-air temperature range: SN5481A, SN5484A Circuits . . . . . −55°C to 125°C
SN7481A, SN7484A Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies to any X input in conjunction with any Y input.

2

recommended operating conditions

	SN5481A, SN5484A			SN7481A, SN7484A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			20			40	mA
Width of write pulse, $t_{w(write)}$ (see Figure 1)	20			20			ns
Address input setup time, t_{su} (see Figure 1)	0			0			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	SN5481A, SN5484A			SN7481A, SN7484A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level voltage at any input			2			2			V
V_{IL}	Low-level voltage at address inputs	to prevent writing				0.8			0.8	V
		to prevent sensing				1			1	
V_{IL}	Low-level voltage at write inputs					0.8			1	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
I_{OH}	High-level output current		V_{CC} = MIN, V_{OH} = 5.5 V			250			250	μA
V_{OL}	Low-level output voltage		V_{CC} = MIN, I_{OL} = MAX			0.4			0.4	V
I_I	Input current at maximum input voltage	Write	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
		Address				3			3	
I_{IH}	High-level input current	Write	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
		Address	V_{CC} = MAX, V_I = 4.5 V			400			400	
I_{IL}	Low-level input current	Write	V_{CC} MAX, V_I = 0.4 V			−1.6			−1.6	mA
		Address				−11			−11	
I_{CC}	Supply current		V_{CC} = MAX, All inputs at 0 V			70			65	mA
			V_{CC} = 5 V, All inputs at 0 V		45	60		45	60	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

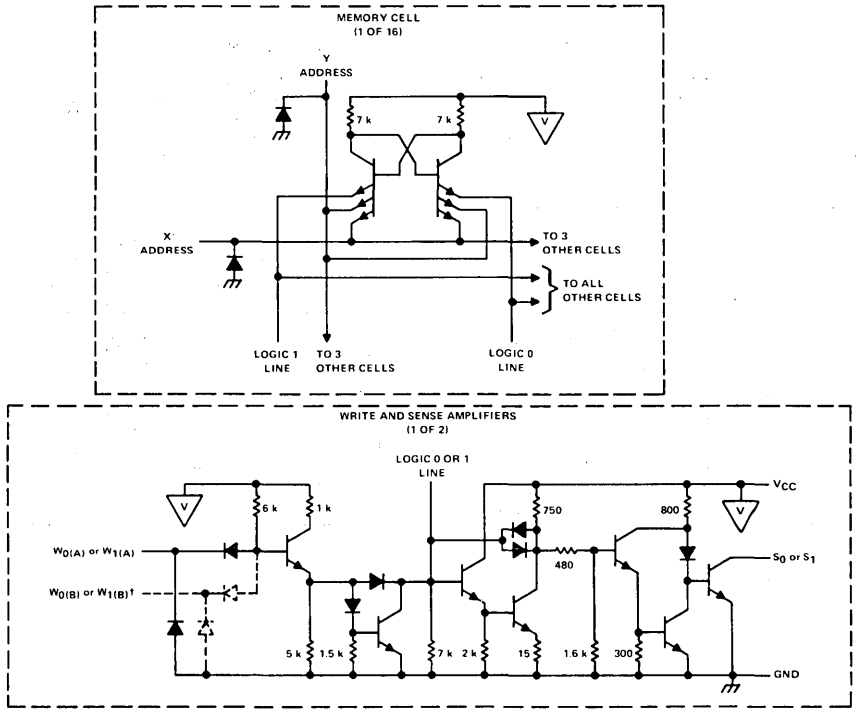
switching characteristics, V_{CC} = 5 V, I_{OL} = MAX†, T_A = 25°C, see figure 1

PARAMETER§	LOCATION ADDRESSED	TEST CONDITIONS	SN5481A, SN5484A			SN7481A, SN7484A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{SR}	X1 – Y1	C_L = 30 pF		13			13		ns
		C_L = 200 pF		18	30		18	30	
t_{PHL}	X1 – Y1	C_L = 30 pF		11	19		12	20	ns
		C_L = 200 pF		17	26		18	27	
t_{PLH}		C_L = 30 pF		13	20		12	19	
		C_L = 200 pF		27	40		18	27	
t_{PHL}	X1 thru X4 and Y1	C_L = 30 pF		10	18		11	19	ns
		C_L = 200 pF		16	25		17	26	
t_{PLH}		C_L = 30 pF		13	20		13	20	
		C_L = 200 pF		27	40		19	28	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

§ t_{SR} ≡ Sense recovery time after writing
t_{PHL} ≡ Propagation delay time, high-to-low-level output
t_{PLH} ≡ Propagation delay time, low-to-high-level output

schematic



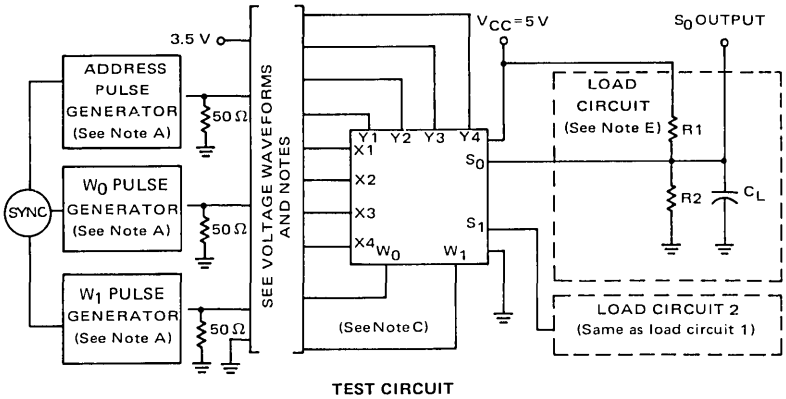
† $W_{0(B)}$ and $W_{1(B)}$ inputs (indicated with dashed lines) are applicable for the SN5484A, SN7484A only.

▽ . . . V_{CC} bus

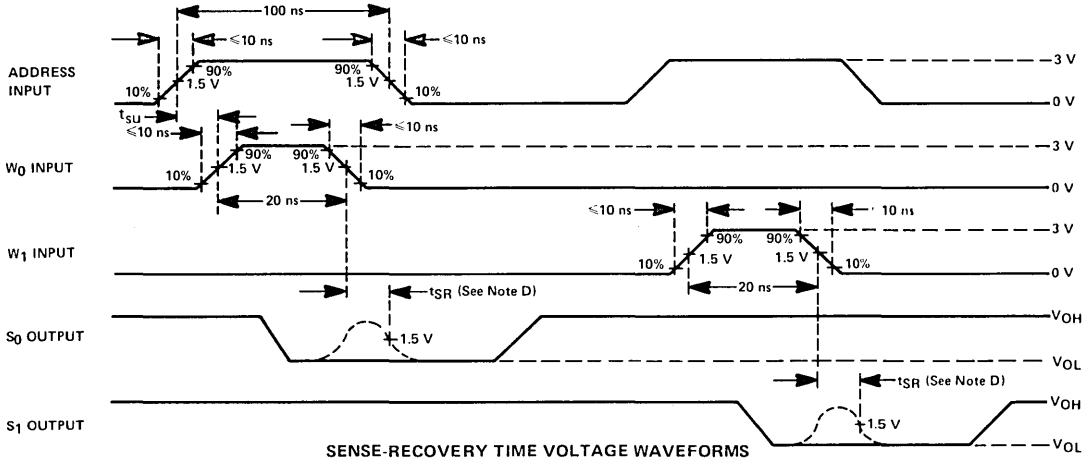
Resistor values shown are nominal and in ohms.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

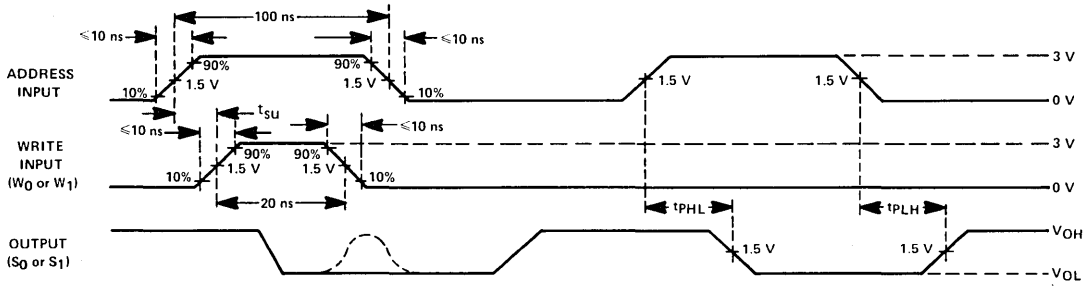
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



SENSE-RECOVERY TIME VOLTAGE WAVEFORMS



PROPAGATION DELAY TIME VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: for the address pulse generator, PRR = 2 MHz; for the W_0 and W_1 pulse generators, PRR = 1 MHz.
B. C_L includes probe and jig capacitance.
C. For the SN5484A and SN7484A, unused W_0 and W_1 inputs are at 3.5 V.
D. t_{SR} ≡ sense-recovery time
E. For the SN5481A and SN5484A: R1 = 240 Ω and R2 = 560 Ω. For the SN7481A and SN7484A: R1 = 120 Ω and R2 = 330 Ω.

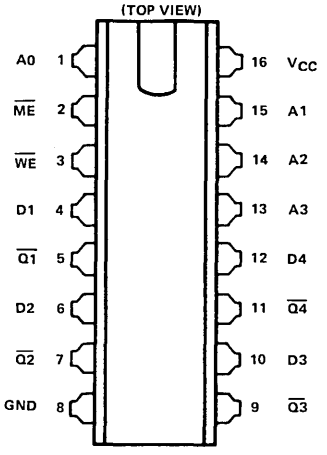
FIGURE 1–SWITCHING CHARACTERISTICS

TYPE SN7489
64-BIT RANDOM-ACCESS READ/WRITE MEMORY

D1416, DECEMBER 1972 – REVISED MAY 1975

- For Application as a "Scratch Pad" Memory with Nondestructive Read-Out
- Fully Decoded Memory Organized as 16 Words of Four Bits Each
- Fast Access Time . . . 33 ns Typical
- Diode-Clamped, Buffered Inputs
- Open-Collector Outputs Provide Wire-AND Capability
- Typical Power Dissipation . . . 375 mW
- Compatible with Most TTL and DTL Circuits

J OR N PACKAGE
(TOP VIEW)

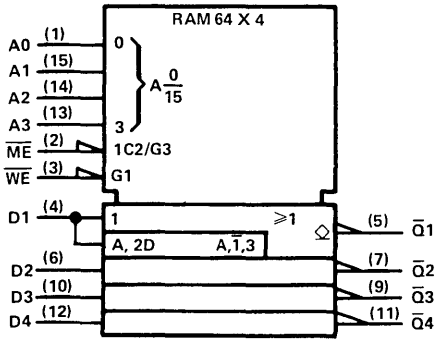


description

This 64-bit active-element memory is a monolithic, high-speed, transistor-transistor logic (TTL) array of 64 flip-flop memory cells organized in a matrix to provide 16 words of four bits each. Each of the 16 words is addressed in straight binary with full on-chip decoding.

The buffered memory inputs consist of four address lines, four data inputs, a write enable, and a memory enable for controlling the entry and access of data. The memory has open-collector outputs which may be wire-AND connected to permit expansion up to 4704 words of N-bit length without additional output buffering. Access time is typically 33 nanoseconds; power dissipation is typically 375 milliwatts.

logic symbol



FUNCTION TABLE

$\overline{ME}$	$\overline{WE}$	OPERATION	CONDITION OF OUTPUTS
L	L	Write	Complement of Data Inputs
L	H	Read	Complement of Selected Word
H	L	Inhibit Storage	Complement of Data Inputs
H	H	Do Nothing	High

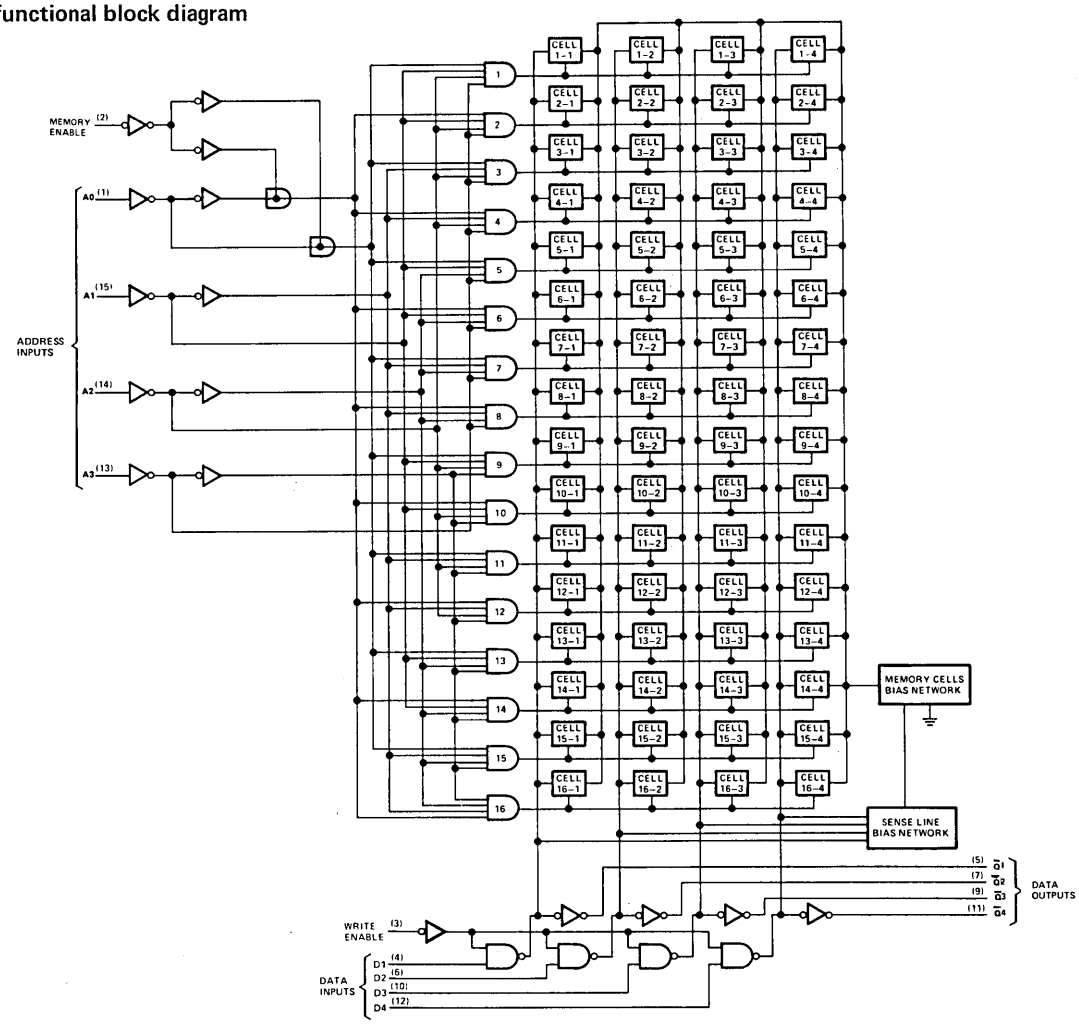
write operation

Information present at the data inputs is written into the memory by addressing the desired word and holding both the memory enable and write enable low. Since the internal output of the data input gate is common to the input of the sense amplifier, the sense output will assume the opposite state of the information at the data inputs when the write enable is low.

read operation

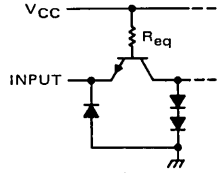
The complement of the information which has been written into the memory is nondestructively read out at the four sense outputs. This is accomplished by holding the memory enable low, the write enable high, and selecting the desired address.

functional block diagram



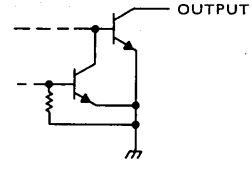
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



Data Inputs: R_{eq} = 6 kΩ NOM
All others: R_{eq} = 4 kΩ NOM

TYPICAL OF ALL OUTPUTS



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
High-level output voltage, V_{OH} (see Notes 1 and 2) . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the maximum voltage that should be applied to any output when it is in the off state.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Width of write-enable pulse, t_w	40			ns
Setup time, data input with respect to write enable, t_{su} (see Figure 1)	40			ns
Hold time, data input with respect to write enable, t_h (see Figure 1)	5			ns
Select input setup time with respect to write enable, t_{su}	0			ns
Select input hold time after writing, t_h (see Figure 1)	5			ns
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA			−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, V_{OH} = 5.5 V			20	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V,	I_{OL} = 12 mA			0.4	V
			I_{OL} = 16 mA			0.45	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−1.6	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 3		75	105	mA
C_o	Off-state output capacitance	V_{CC} = 5 V, f = 1 MHz	V_O = 2.4 V,		6.5		pF

NOTE 3: I_{CC} is measured with the memory enable grounded, all other inputs at 4.5 V, and all outputs open.

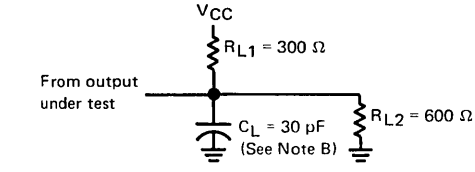
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

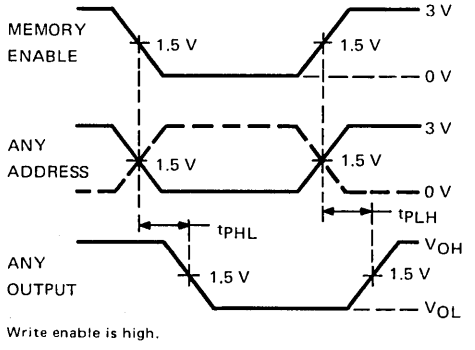
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from memory enable		C_L = 30 pF, R_{L1} = 300 Ω, R_{L2} = 600 Ω, See Figure 1		26	50	ns
t_{PHL}	Propagation delay time, high-to-low-level output from memory enable				33	50	
t_{PLH}	Propagation delay time, low-to-high-level output from any address input				30	60	ns
t_{PHL}	Propagation delay time, high-to-low-level output from any address input				35	60	
t_{SR}	Sense recovery time after writing	output initially high			39	70	ns
		output initially low			48	70	

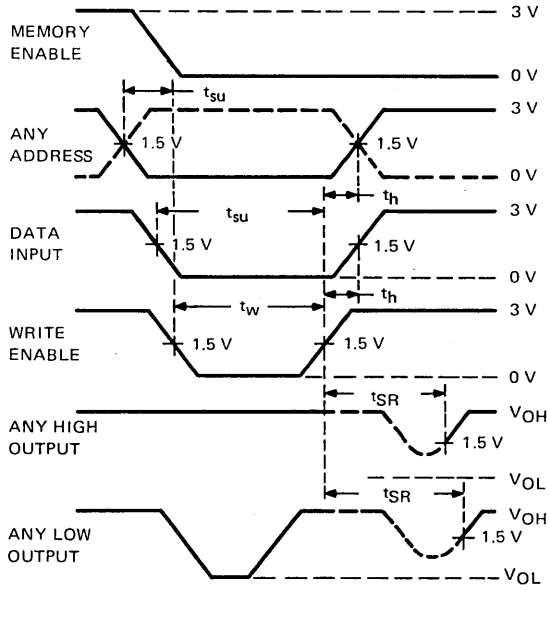
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



READ CYCLE



WRITE CYCLE FROM WRITE ENABLE

NOTES: A. The input pulse generators have the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 1–SWITCHING CHARACTERISTICS

TYPICAL CHARACTERISTICS

INPUT CURRENT vs INPUT VOLTAGE

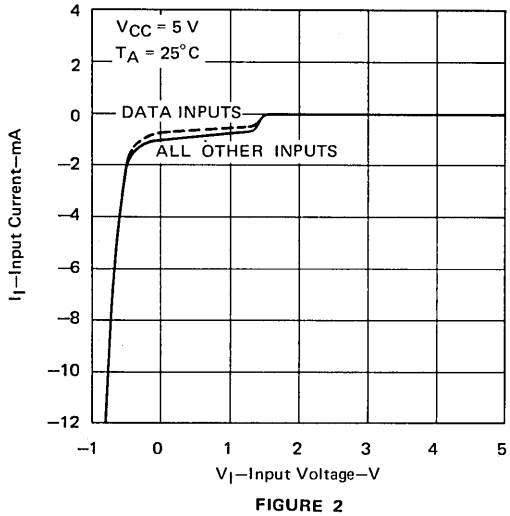


FIGURE 2

PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

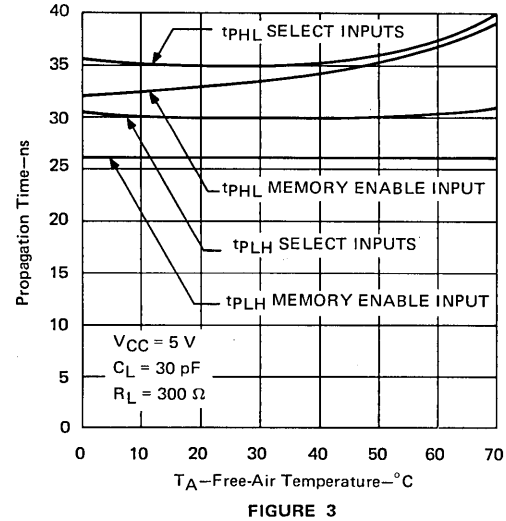


FIGURE 3

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TYPES SN54LS189A, SN54LS219A, SN54LS289A, SN54LS319A, SN74LS189A, SN74LS219A, SN74LS289A, SN74LS319A 64-BIT RANDOM-ACCESS MEMORIES

D2417, SEPTEMBER 1980

- Organized as 16 Words of Four Bits Each
- Choice of Buffered 3-State or Open-Collector Outputs
- Choice of Noninverted or Inverted Outputs
- Typical Access Time . . . 50 ns

description

These monolithic TTL memories feature Schottky clamping for high performance and a fast chip-select access time to enhance decoding at the system level. A three-state-output version and an open-collector-output version are offered for both of the logic choices. A three-state output offers the convenience of an open-collector output with the speed of a totem-pole output; it can be bus-connected to other similar outputs, yet it retains the fast rise time characteristic of the TTL totem-pole output. An open-collector output offers the capability of direct interface with a data line having a passive pull-up.

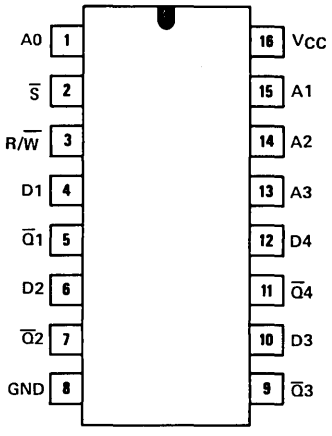
write cycle

Information to be stored in the memory is written into the selected address location when the chip-select ($\overline{S}$) and the write-enable ($R/\overline{W}$) inputs are low. While the write-enable input is low, the memory outputs are off (three-state = Hi-Z, open-collector = high). When a number of outputs are bus-connected, this off state neither loads nor drives the data bus; however, it permits the bus line to be driven by other active outputs or a passive pull-up.

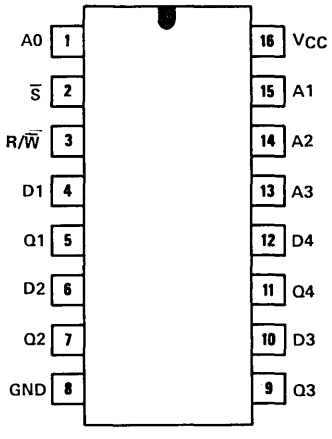
read cycle

Information stored in the memory (see function table for input/output phase relationship) is available at the outputs when the write-enable input is high and the chip-select input is low. When the chip-select input is high, the outputs will be off.

SN54LS189A, SN54LS289A . . . J PACKAGE
SN74LS189A, SN74LS289A . . . J OR N PACKAGE
(TOP VIEW)



SN54LS219A, SN54LS319A . . . J PACKAGE
SN74LS219A, SN74LS319A . . . J OR N PACKAGE
(TOP VIEW)



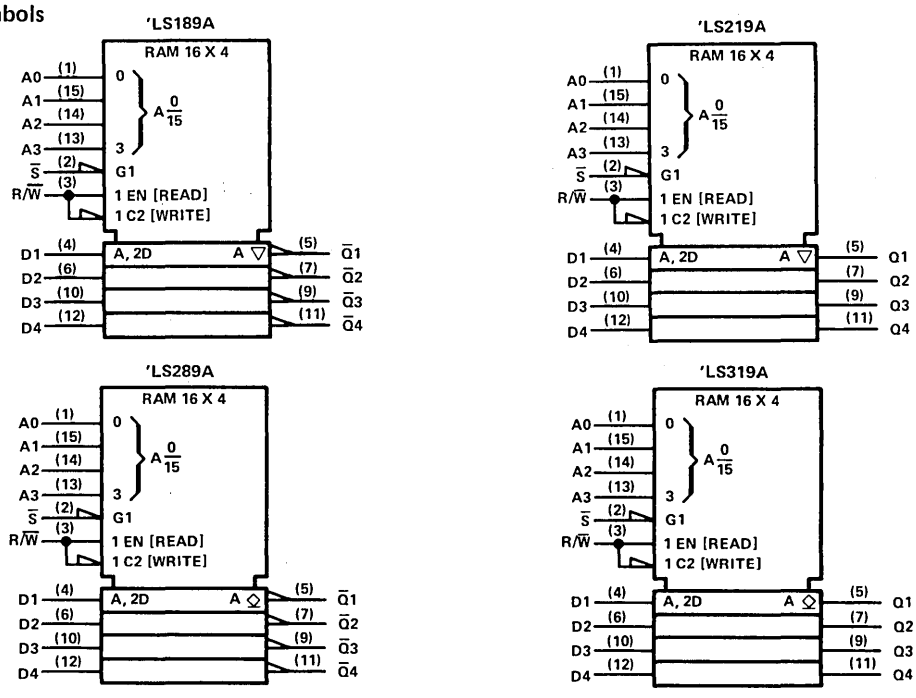
SN54LS' versions are available in chip carriers. See Product Guide, Section 7, for pin assignments.

FUNCTION TABLE

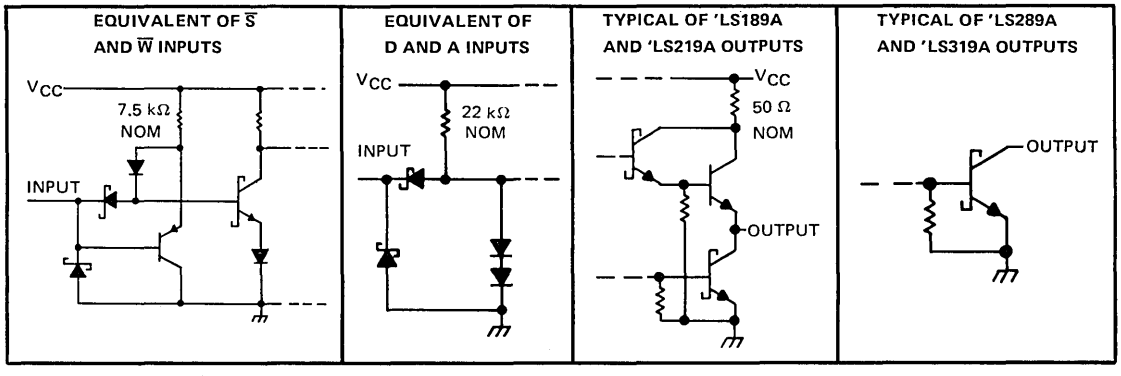
FUNCTION	INPUTS		OUTPUTS			
	CHIP SELECT	WRITE ENABLE	'LS189A	'LS289A	'LS219A	'LS319A
Write	L	L	Z	Off	Z	Off
Read	L	H	Complement of Data Entered	Complement of Data Entered	Data Entered	Data Entered
Inhibit	H	X	Z	Off	Z	Off

H = high level, L = low level, X = irrelevant, Z = high impedance

logic symbols



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Off-state output voltage: 'LS189A, 'LS219A	5.5 V
'LS289A, 'LS319A	7 V
Operating free-air temperature range: SN54LS' Circuits	−55°C to 125°C
SN74LS' Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

recommended operating conditions

		SN54LS189A, SN54LS219A			SN74LS189A, SN74LS219A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−1			−2.6	mA
Low-level output current, I_{OL}				12			24	mA
Width of write pulse (write enable low), $t_{w(wr)}$		80			70			ns
Setup time	Address before write pulse, $t_{su(ad)}$	0↓			0↓			ns
	Data before end of write pulse, $t_{su(da)}$	80↑			60↑			
	Chip-select before end of write pulse, $t_{su(S)}$	80↑			60↑			
Hold time	Address after write pulse, $t_{h(ad)}$	0↑			0↑			ns
	Data after write pulse, $t_{h(da)}$	0↑			0↑			
	Chip-select after write pulse, $t_{h(S)}$	0↑			0↑			
Operating free-air temperature, T_A		−55		125	0		70	°C

↑↓The arrow indicates the transition of the write-enable input used for reference: ↑ for the low-to-high transition, ↓ for the high-to-low transition.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS189A SN54LS219A			SN74LS189A SN74LS219A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max, I_{OH} = MAX		2.4	3.1		2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = V_{IL} max, V_O = 2.7 V				20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = V_{IL} max, V_O = 0.4 V				−20			−20	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				100			100	μA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−30		−130	−30		−130	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2			35	60		35	60	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

NOTE 2: I_{CC} is measured with the write-enable and chip-select inputs grounded, all other inputs at 4.5 V, and all outputs open.

switching characteristics over recommended operating ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER			TEST CONDITIONS	SN54LS189A, SN54LS219A		SN74LS189A, SN74LS219A		UNIT
				TYP‡	MAX	TYP‡	MAX	
$t_{a(ad)}$	Access time from address		C_L = 45 pF, See Note 3	50	90	50	80	ns
$t_{a(S)}$	Access time from chip select (enable time)			35	70	35	60	ns
t_{SR}	Sense recovery time			55	100	55	90	ns
t_{PXZ}	Disable time from high or low level	from $\overline{S}$	C_L = 5 pF, See Note 3	30	60	30	50	ns
		from R/$\overline{W}$		40	70	40	60	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 3: Load circuit and voltage waveforms are shown on page 1-12.

recommended operating conditions

		SN54SL289A, SN54LS319A			SN74LS289A, SN74LS319A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}				5.5			5.5	V
Low-level output current, I_{OL}				12			24	mA
Width of write pulse (write enable low), $t_{w(wr)}$		80			70			ns
Setup time	Address before write pulse, $t_{su(ad)}$	0↓			0↓			ns
	Data before end of write pulse, $t_{su(da)}$	80↑			60↑			
	Chip-select before end of write pulse, $t_{su(S)}$	80↑			60↑			
Hold time	Address after write pulse, $t_{h(ad)}$	0↑			0↑			ns
	Data after write pulse, $t_{h(da)}$	0↑			0↑			
	Chip-select after write pulse, $t_{h(S)}$	0↑			0↑			
Operating free-air temperature, T_A		−55		125	0		70	°C

↑↓The arrow indicates the transition of the write-enable input used for reference: ↑ for the low-to-high transition, ↓ for the high-to-low transition.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS289A, SN54LS319A			SN74LS289A, SN74LS319A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max,	V_O = 2.4 V			20			20	μA
			V_O = 5.5 V			100			100	
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				100			100	μA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2			35	60		35	60	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: I_{CC} is measured with the write-enable and chip-select inputs grounded, all other inputs at 4.5 V, and all outputs open.

switching characteristics over recommended operating ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER			TEST CONDITIONS	SN54LS289A, SN54LS319A		SN74LS289A, SN74LS319A		UNIT
				TYP‡	MAX	TYP‡	MAX	
$t_{a(ad)}$	Access time from address		C_L = 45 pF, R_L = 667 Ω, See Note 3	50	90	50	80	ns
$t_{a(S)}$	Access time from chip select (enable time)			35	70	35	60	ns
t_{SR}	Sense recovery time			55	100	55	90	ns
t_{PLH}	Propagation delay time, low-to-high-level output (disable time)	from $\overline{S}$		30	60	30	50	ns
		from R/$\overline{W}$		40	70	40	60	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 3: Load circuit and voltage waveforms are shown on page 1-12.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

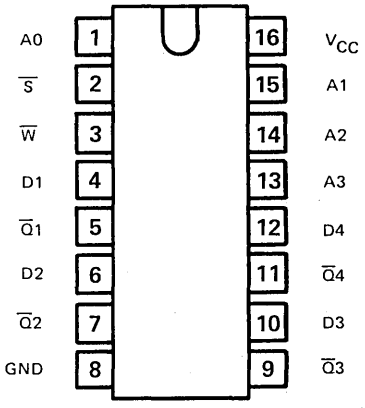
TYPES SN54S189A, SN54S289A, SN74S189A, SN74S289A 64-BIT HIGH-PERFORMANCE RANDOM-ACCESS MEMORIES

SEPTEMBER 1976 – REVISED JUNE 1981

STATIC RANDOM-ACCESS MEMORIES

- Fully Decoded RAM's Organized as 16 Words of Four Bits Each
- Schottky-Clamped for High Speed:
  - Read Cycle Time . . . 25 ns Typical
  - Write Cycle Time . . . 25 ns Typical
- Choice of Three-State or Open-Collector Outputs
- Compatible with Most TTL and I^2L Circuits
- Chip-Select Input Simplifies External Decoding

SN54S189A, SN54S289A . . . . J OR W PACKAGE
SN74S189A, SN74S289A . . . . J OR N PACKAGE
(TOP VIEW)



These devices are also available in chip carriers. See Product Guide Section 7, for pin assignments.

2

description

These 64-bit active-element memories are monolithic Schottky-clamped transistor-transistor logic (TTL) arrays organized as 16 words of four bits each. They are fully decoded and feature a chip-select input to simplify decoding required to achieve expanded system organization. The memories feature p-n-p input transistors that reduce the low-level input current requirement to a maximum of −0.25 milliamperes, only one-eighth that of a Series 54S/74S standard load factor. The chip-select circuitry is implemented with minimal delay times to compensate for added system decoding.

write cycle

The information applied at the data input is written into the selected location when the chip-select input and the write-enable input are low. While the write-enable input is low, the 'S189A output is in the high-impedance state and the 'S289A output is off. When a number of outputs are bus-connected, this high-impedance or off state will neither load nor drive the bus line, but it will allow the bus line to be driven by another active output or a passive pull-up.

read cycle

The stored information (complement of information applied at the data input during the write cycle) is available at the output when the write-enable input is high and the chip-select input is low. When the chip-select input is high, the 'S189A output will be in the high-impedance state and the 'S289A output will be off.

FUNCTION TABLE

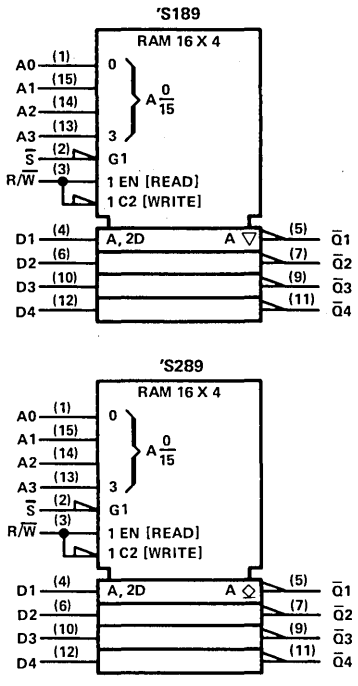
FUNCTION	INPUTS		'S189A OUTPUT	'S289A OUTPUT
	CHIP SELECT	WRITE ENABLE		
Write	L	L	High Impedance	Off
Read	L	H	Complement of Data Entered	Complement of Data Entered
Inhibit	H	X	High Impedance	Off

H = high level, L = low level, X = irrelevant

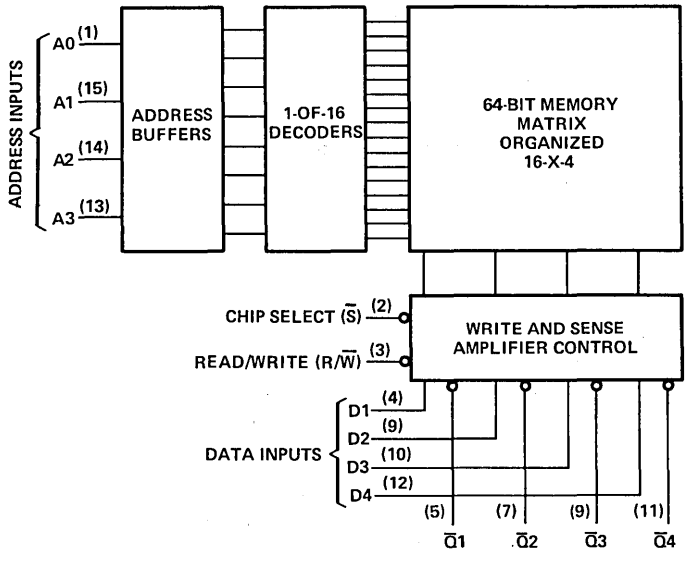
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U. S. Patent Number 3,463,975.

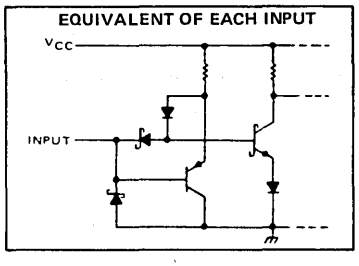
logic symbols

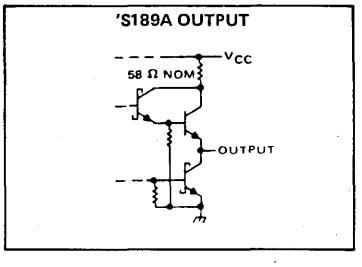


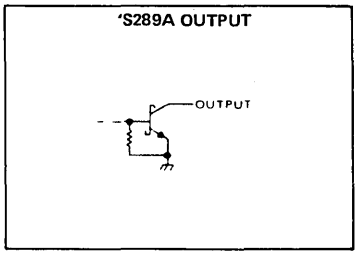
functional block diagram



schematics of inputs and outputs







absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Off-State output voltage	5.5 V
Operating free-air temperature range: SN54S' Circuits	−55°C to 125°C
SN74S' Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

recommended operating conditions

		SN54S189A			SN54S289A			SN74S189A			SN74S289A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	4.75	5	5.25	4.75	5	5.25	V
High-level output voltage, V_{OH}							5.5						5.5	V
High-level output current, I_{OH}				−2						−6.5				mA
Low-level output current, I_{OL}				12			12			12			12	mA
Width of write pulse (write enable low), $t_{w(wr)}$		25			25			25			25			ns
Setup time	Address before write pulse, $t_{su(da)}$	0↓			0↓			0↓			0↓			ns
	Data before end of write pulse, $t_{su(da)}$	25↑			25↑			25↑			25↑			
	Chip-select before end of write pulse, $t_{su(S)}$	25↑			25↑			25↑			25↑			
Hold time	Address after write pulse, $t_{h(ad)}$	3↑			3↑			0↑			0↑			ns
	Data after write pulse, $t_{h(da)}$	0↑			0↑			0↑			0↑			
	Chip-select after write pulse, $t_{h(\overline{S})}$	0↑			0↑			0↑			0↑			
Operating free-air temperature, T_A		−55		125	−55		125	0		70	0		70	°C

↑↓The arrow indicates the transition of the write-enable input used for reference: ↑ for the low-to-high transition, ↓ for the high-to-low transition.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			'S189A			'S289A			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18mA					−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX		SN54S'	2.4	3.4					V
				SN74S'	2.4	3.2					
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	V_O=2.4 V							40	μA
			V_O=5.5 V							100	
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 12 mA				0.35	0.5		0.35	0.5	V
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V, V_{OH} = 2.4 V					50				μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V, V_{OL} = 0.4 V					−50				μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V					1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V					25			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V					−250			−250	μA
I_{OS}	Short-circuit output current§	V_{CC} = MAX			−30		−100				mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2				75	110		75	105	mA

†For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Duration of the short circuit should not exceed one second.

NOTE 2: I_{CC} is measured with the read/write and chip-select inputs grounded. All other inputs at 4.5V, and the outputs open.

'S189A switching characteristics over recommended operating ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER			TEST CONDITIONS	SN54S189A		SN74S189A		UNIT
				TYP‡	MAX	TYP‡	MAX	
$t_{a(ad)}$	Access time from address		C_L = 30 pF, See Note 3	25	50	25	35	ns
$t_{a(S)}$	Access time from chip select (enable time)			18	25	18	22	ns
t_{SR}	Sense recovery time			22	40	22	35	ns
t_{PXZ}	Disable time from high or low level	from $\overline{S}$	C_L = 5 pF, See Note 3	12	25	12	17	ns
		from $\overline{W}$		12	30	12	25	

'S289A switching characteristics over recommended operating ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER			TEST CONDITIONS	SN54S289A		SN74S289A		UNIT
				TYP‡	MAX	TYP‡	MAX	
$t_{a(ad)}$	Access time from address		C_L = 30 pF, R_{L1} = 300 Ω, R_{L2} = 600 Ω, See Note 3	25	50	25	35	ns
$t_{a(S)}$	Access time from chip select (enable time)			18	25	18	22	ns
t_{SR}	Sense recovery time			22	40	22	35	ns
t_{PLH}	Propagation delay time, low-to-high-level output (disable time)	from $\overline{S}$		12	25	12	17	ns
		from $\overline{W}$		12	30	12	25	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C

NOTE: 3. Load circuit and voltage waveforms are shown on page 1-12.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

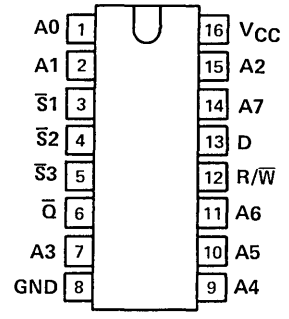
TYPES SN74S201, SN74S301
256-BIT HIGH-PERFORMANCE RANDOM-ACCESS MEMORIES

D2007, SEPTEMBER 1977 – REVISED JUNE 1979

STATIC RANDOM-ACCESS MEMORIES

- Static Fully Decoded RAM's Organized as 256 Words of One Bit Each
- Schottky-Clamped for High Performance
- Choice of Three-State or Open-Collector Outputs
- Compatible with Most TTL and I^2L Circuits
- Chip-Select Inputs Simplify External Decoding
- Typical Performance:
  - Read Access Time . . . . . 42 ns
  - Power Dissipation . . . . . 500 mW

SN74S201, SN74S301 . . J OR N PACKAGE
(TOP VIEW)



2

description

These 256-bit active-element memories are monolithic transistor-transistor logic (TTL) arrays organized as 256 words of one bit. They are fully decoded and have three chip-select inputs to simplify decoding required to achieve expanded system organizations.

write cycle

The information applied at the data input is written into the selected location when the three chip-select inputs and the write-enable input are low. While the write-enable input is low, the 'S201 outputs are in the high-impedance state and the 'S301 outputs are off. When a number of outputs are bus-connected, this high-impedance or off state will neither load nor drive the bus line, but it will allow the bus line to be driven by another active output or a passive pull-up.

read cycle

The stored information (complement of information applied at the data input during the write cycle) is available at the output when the write-enable input is high and the three chip-select inputs are low. When any one of the chip-select inputs are high, the 'S201 outputs will be in the high-impedance state and the 'S301 outputs will be off.

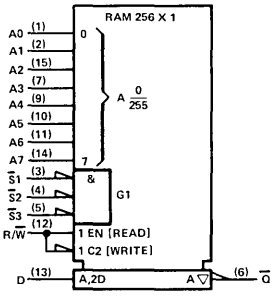
FUNCTION TABLE

FUNCTION	INPUTS		'S201 OUTPUT ($\overline{Q}$)	'S301 OUTPUT ($\overline{Q}$)
	CHIP SELECT ($\overline{S}$)	WRITE ENABLE R/$\overline{W}$		
Write	L	L	High Impedance	Off
Read	L	H	Complement of Data Entered	Complement of Data Entered
Inhibit	H	X	High Impedance	Off

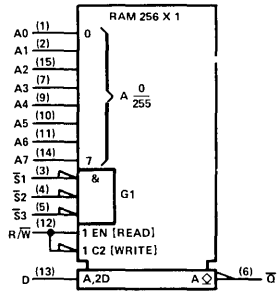
H ≡ high level, L ≡ low level, X ≡ irrelevant
For chip-select: L ≡ all $\overline{S}i$ inputs low, H ≡ one or more $\overline{S}i$ inputs high

logic symbols

SN74S201



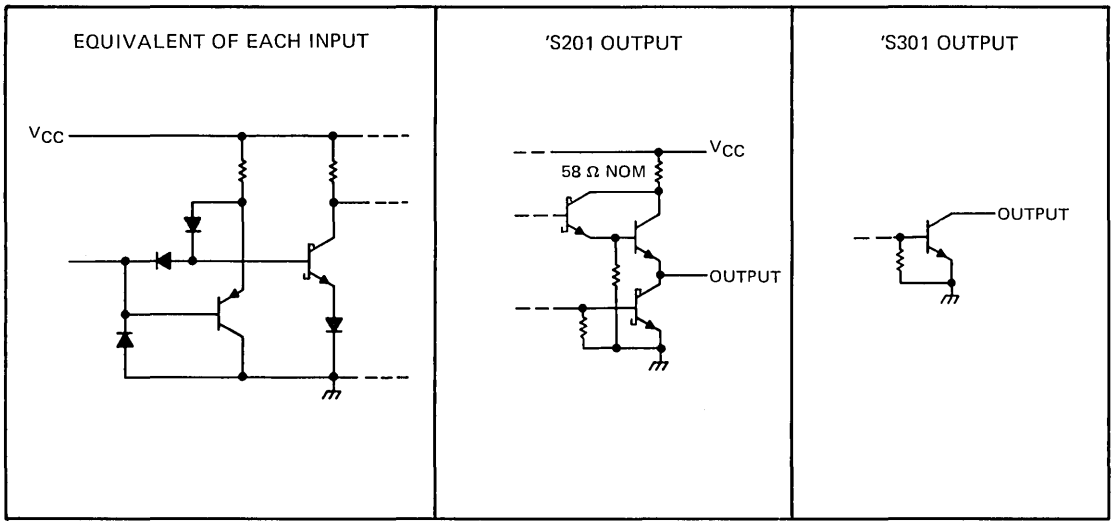
SN74S301



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U. S. Patent Number 3,463,975.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Off-State output voltage . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN74S201			SN74S301			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage, V_{CC} (see Note 1)		4.75	5	5.25	4.75	5	5.25	V
High-level output voltage, V_{OH}							5.5	V
High-level output current, I_{OH}				−10.3				mA
Low-level output current, I_{OL}				16			16	mA
Width of write pulse (write enable low), $t_{w(wr)}$		65			65			ns
Setup time	Address before write pulse, $t_{su(ad)}$	0↓			0↓			ns
	Data before end of write pulse, $t_{su(da)}$	65↑			65↑			
	Chip-select before end of write pulse, $t_{su(\overline{S})}$	65↑			65↑			
Hold time	Address after write pulse, $t_{h(ad)}$	0↑			0↑			ns
	Data after write pulse, $t_{h(da)}$	0↑			0↑			
	Chip-select after write pulse, $t_{h(\overline{S})}$	0↑			0↑			
Operating free-air temperature, T_A		0		70	0		70	°C

↑↓ The arrow indicates the transition of the write input used for references: ↑ for the low to high transistion, ↓ for the high to low transistion.

NOTE 1: Voltage values are with respect to network ground terminal.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		'S201			'S301			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18mA				−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 08 V, I_{OH} = MAX		2.4						V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V,				0.45			0.45	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	V_O=2.4 V						40	μA
			V_O=5.5 V						100	
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V, V_{OH} = 2.4 V				40				μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V, V_{OL} = 0.5 V				−40				μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				25			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V				−250			−250	μA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−30		−100				mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2			100	140		100	140	mA

†For conditions shown as MIN or MAX use the appropriate value specified under recommended operation conditions.
‡These typical values are at V_{CC} = 5 V, T_A = 25°C.
§Duration of the short circuit should not exceed one second.
NOTE: 2. I_{CC} is measured with all chip-select inputs grounded, all other inputs at 4.5 V, and the output open

'S201 switching characteristics over recommended operating ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
$t_{a(ad)}$	Access time from address		C_L = 30 pF, See Note 3		42	65	ns
$t_{a(S)}$	Access time from chip select (select time)				13	30	ns
t_{SR}	Sense recovery time				20	40	ns
t_{PXZ}	Disable time from high or low level	From $\overline{S}$	C_L = 5 pF, See Note 3		9	20	ns
		From R/$\overline{W}$					

'S301 switching characteristics over recommended operating ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
$t_{a(ad)}$	Access time from address		C_L = 30 pF, R_{L1} = 300 Ω, R_{L2} = 600 Ω, See Note 3		42	65	ns
$t_{a(S)}$	Access time from chip enable (enable time)				13	30	ns
t_{SR}	Sense recovery time				20	40	ns
t_{PLH}	Propagation delay time, low-to-high-level output (disable time)	From $\overline{S}$			8	20	ns
		From R/$\overline{W}$			15	35	

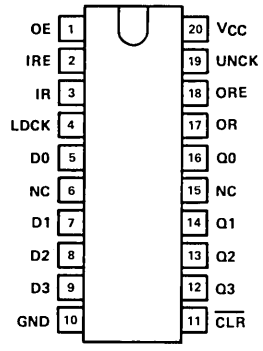
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE: 3. Load circuit and voltage waveforms are shown on page 1-12.

TYPES SN54LS222, SN54LS224, SN54LS227, SN54LS228, SN74LS222, SN74LS224, SN74LS227, SN74LS228
16 X 4 ASYNCHRONOUS FIRST-IN FIRST-OUT MEMORIES

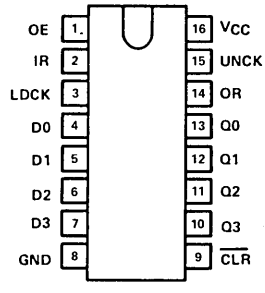
D2616, JANUARY 1981

- Independent Asynchronous Inputs and Outputs
- 16 Words of 4 Bits Each
- 3-State Outputs Drive Bus Lines Directly
- Data Rates from 0 to 10 MHz
- Fall-Through Time . . . 50 ns Typ
- Data Terminals Arranged for Optimum PC Board Layout
- Expandable Using External Gating

SN54LS222, SN54LS227 . . . J PACKAGE
SN74LS222, SN74LS227 . . . J OR N PACKAGE
(TOP VIEW)



SN54LS224, SN54LS228 . . . J PACKAGE
SN74LS224, SN74LS228 . . . J OR N PACKAGE
(TOP VIEW)



NC = No internal connection

SN54LS222, SN54LS224, SN54LS227 and SN54LS228 are also available in chip carriers. See Product Guide, Section 7, for pin assignments.

description

These 64-bit memories are Low-Power Schottky memory arrays organized as 16 words of 4 bits each. They can be expanded in multiples of 15m+1 words or 4n bits, or both, (where n is the number of packages in the vertical array and m is the number of packages in the horizontal array) but some external gating is required (see Figure 1). For longer words using the 'LS224 or 'LS228, the IR signals of the first-rank packages and OR signals of the last-rank packages must be ANDed for proper synchronization.

TYPE	INPUT-READY ENABLE AND OUTPUT-READY ENABLE	OUTPUT
'LS222	Yes	3-State
'LS224	No	3-State
'LS227	Yes	Open-collector
'LS228	No	Open-collector

operation

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. These FIFO's are designed to process data at rates from 0 to 10 MHz in a bit-parallel format, word by word. Data is written into the memory on a high-to-low transition at the load clock input (LDCK) and read out on a low-to-high transition at the unload clock input (UNCK).

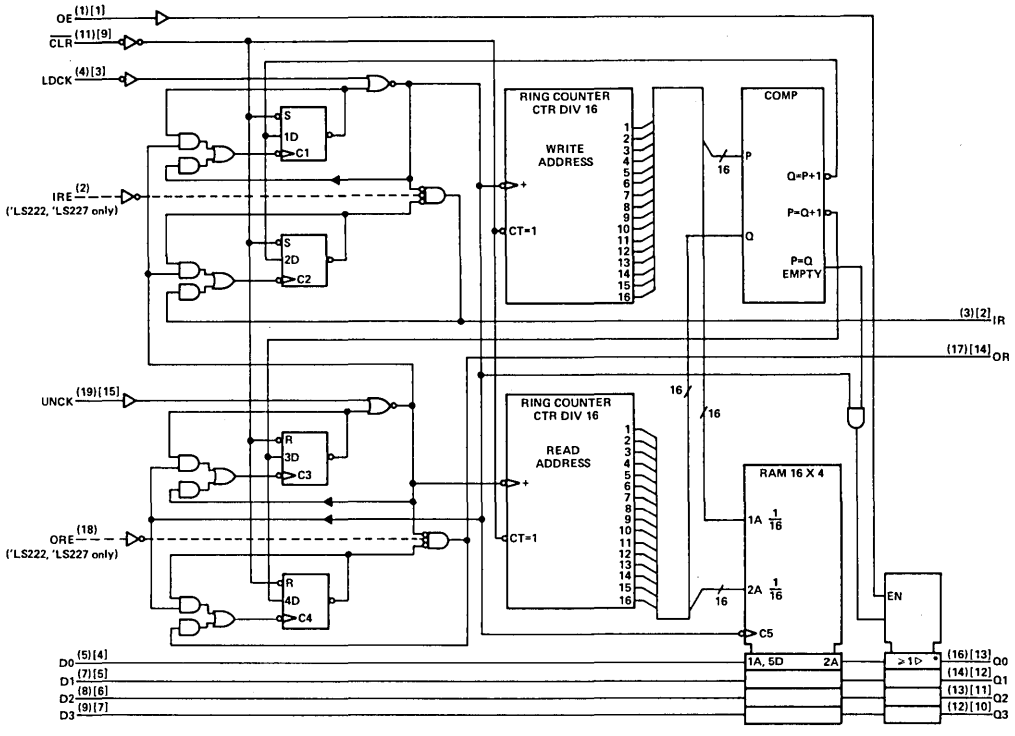
The memory is full when the number of words clocked in exceeds the number of words clocked out by 16. When the memory is full, LDCK signals have no effect. When the memory is empty, UNCK signals have no effect.

Status of the FIFO memory (see timing diagram) is monitored by the input ready (IR) and output ready (OR) flags that indicate "not full" and "not empty" conditions. The IR output will be high only when the memory is not full and the LDCK input is low. The OR output will be high only when the memory is not empty and UNCK is high.

A high-to-low transition at the clear ($\overline{CLR}$) input resets the internal stack control counters and also sets IR high and OR low to indicate that old data remaining at the data outputs is invalid. Data outputs are noninverting with respect to the data inputs and are at high impedance when output enable (OE) is low. OE does not affect the IR and OR outputs.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

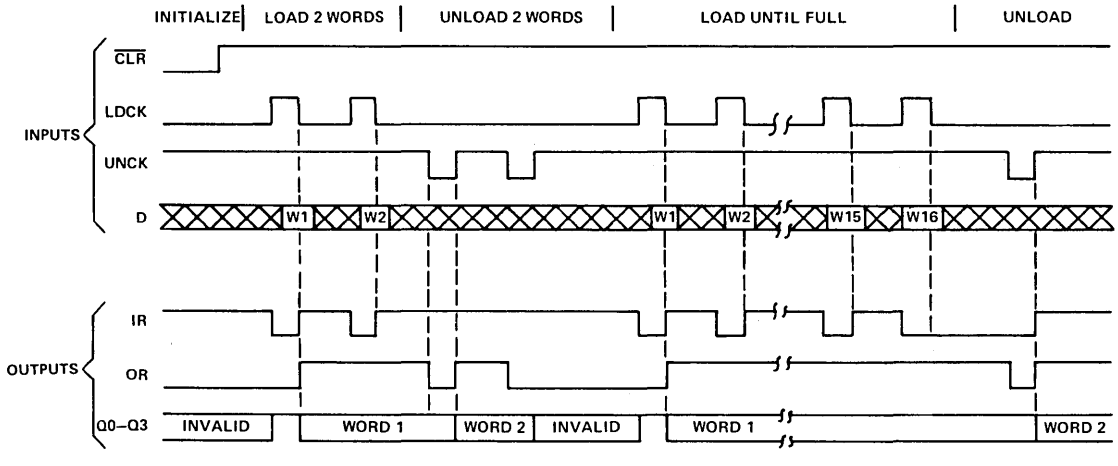
functional block diagram (positive logic)



*'LS222 and 'LS224 have 3-state (▽) outputs.
'LS227 and 'LS228 have open-collector (◇) outputs.

('LS222 and 'LS227 pin numbers)
['LS224 and 'LS228 pin numbers]

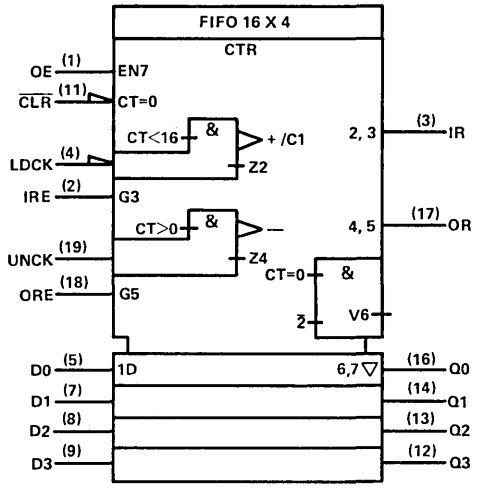
timing diagram



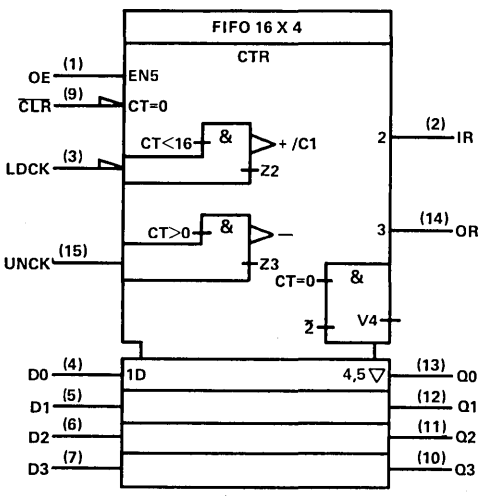
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

logic symbols

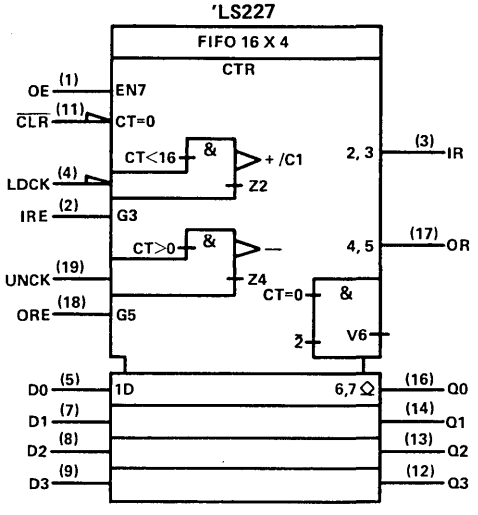
'LS222



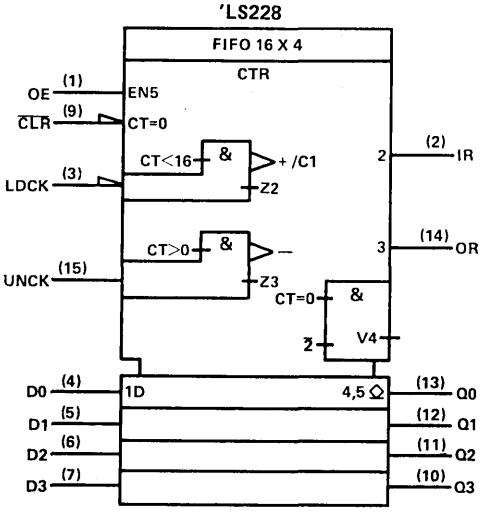
'LS224



'LS227



'LS228



These symbols are functionally accurate but do not show the details of implementation; for these, see the functional block diagram. The symbol represents the memory as if it were controlled by a single counter whose content is the number of words stored at that time. Output data is invalid when the counter content is 0.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (See Note 1) . . . . . 7 V
Input voltage: . . . . . 7 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54LS222, SN54LS224, SN54LS227, SN54LS228 . . . . . −55°C to 125°C
SN74LS222, SN74LS224, SN74LS227, SN74LS228 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	Q			−1			−2.6	mA
	IR, OR			−400			−400	μA
Low-level output current, I_{OL}	Q			12			24	mA
	IR, OR			4			8	
Setup time, t_{su}	D to LDCK ↓	50			50			ns
Hold time, t_h	D from LDCK↓	0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	Q	V_{CC} = MIN, V_{IH} = 2 V,	I_{OH} = MAX	2.4	3.3		2.4	3.2		V
		IR, OR	V_{IL} = V_{IL} max,	I_{OH} = −400 μA	2.5	3.4		2.7	3.4		
V_{OL}	Low-level output voltage	Q	V_{CC} = MIN, V_{IH} = 2 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			V_{IL} = V_{IL} max	I_{OL} = 24 mA					0.35	0.5	
		IR, OR		I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
				I_{OL} = 8 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	Q	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = V_{IL} max	V_O = 2.7 V			20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied	Q		V_O = 0.4 V			−20			−20	μA
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7 V				100			100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit current§	Q	V_{CC} = MAX		−30		−130	−30		−130	mA
		IR, OR			−20		−100	−20		−100	
I_{CC}	Supply current		V_{CC} = MAX	Outputs high		84			84		mA
				Outputs low		87			87		
				Outputs disabled		89			89		

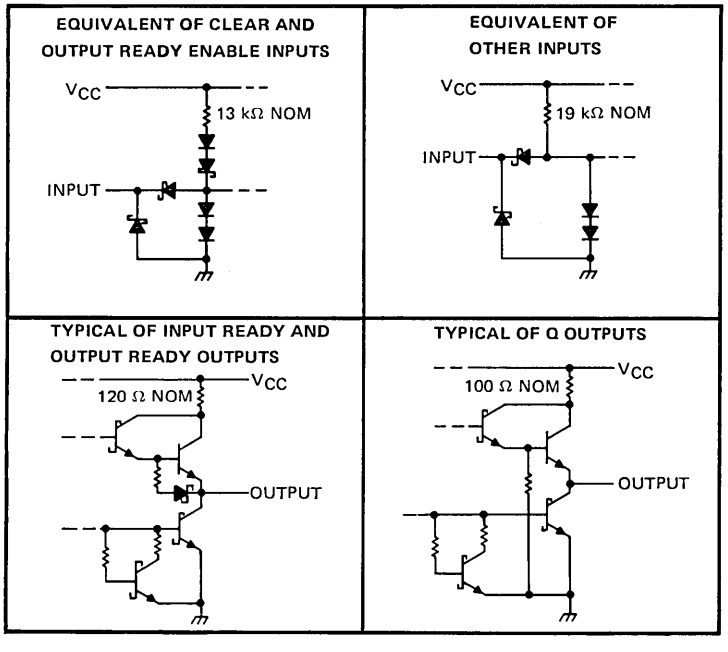
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM	TO	TEST CONDITIONS	'LS222			'LS224			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	IRE↑	IR	C_L = 15 pF, See Note 2		21					ns
t_{PHL}	IRE↓	IR			10					ns
t_{PLH}	ORE↑	OR			21					ns
t_{PHL}	ORE↓	OR			10					ns
t_{PLH}	LDCK↓	IR			25			25		ns
t_{PHL}	LDCK↑	IR			31			31		ns
t_{PLH}	LDCK↓	OR			45			45		ns
t_{PLH}	UNCK↑	OR			28			28		ns
t_{PHL}	UNCK↓	OR			26			26		ns
t_{PLH}	UNCK↑	IR			45			45		ns
t_{PLH}	$\overline{CLR}$↓	IR			33			33		ns
t_{PHL}	$\overline{CLR}$↓	OR			23			23		ns
t_{PLH}	LDCK↓	Q	C_L = 45 pF, See Note 2		45			45		ns
t_{PHL}	LDCK↓	Q			34			34		ns
t_{PLH}	UNCK↑	Q			48			48		ns
t_{PHL}	UNCK↑	Q			46			46		ns
t_{PZL}	OE↑	Q			23			23		ns
t_{PZH}	OE↑	Q			21			21		ns
t_{PLZ}	OE↓	Q	C_L = 5 pF, See Note 2		15			15		ns
t_{PHZ}	OE↓	Q			22			22		ns

NOTE 2: For load circuits and voltage waveforms, see page 1-12.

schematics of inputs and outputs



recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}	Q			5.5			5.5	V
High-level output current, I_{OH}	IR, OR			−400			−400	μA
Low-level output current, I_{OL}	Q			12			24	mA
	IR, OR			4			8	
Setup time, t_{su}	D to LDCK ↓	50			50			ns
Hold time, t_h	D from LDCK↓	0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	IR, OR	V_{CC} = MIN, V_{IH} = 2 V, I_{OH} = −400 μA, V_{IL} = V_{IL} max		2.5	3.4		2.7	3.4		V
I_{OH}	High-level output current	Q	V_{CC} = MIN, V_{IH} = 2 V, V_{OH} = 5.5 V, V_{IL} = V_{IL} max				100			100	μA
V_{OL}	Low-level output voltage	Q	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
		IR, OR		I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
				I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7 V				100			100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	IR, OR	V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current		V_{CC} = MAX	Outputs high		84			84		mA
				Outputs low		87			87		
				Outputs disabled		89			89		

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

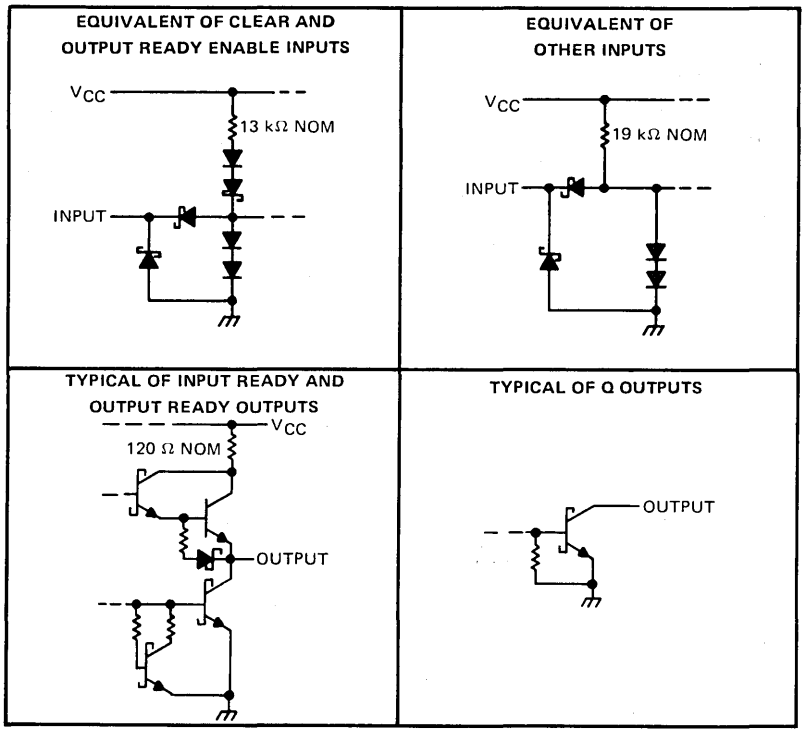
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM	TO	TEST CONDITIONS	'LS227			'LS228			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	IRE ↑	IR	C_L = 15 pF, See Note 2		23					ns
t_{PHL}	IRE ↓	IR			10					ns
t_{PLH}	ORE ↑	OR			23					ns
t_{PHL}	ORE ↓	OR			10					ns
t_{PLH}	LDCK ↓	IR			27			27		ns
t_{PHL}	LDCK ↑	IR			32			32		ns
t_{PLH}	LDCK ↓	OR			52			52		ns
t_{PLH}	UNCK ↑	OR			31			31		ns
t_{PHL}	UNCK ↓	OR			26			26		ns
t_{PLH}	UNCK ↑	IR			49			49		ns
t_{PLH}	$\overline{CLR}$ ↓	IR •			36			36		ns
t_{PHL}	$\overline{CLR}$ ↓	OR			24			24		ns
t_{PLH}	LDCK ↓	Q	R_L = 667 Ω, C_L = 45 pF, See Note 2		54			54		ns
t_{PHL}	LDCK ↓	Q			41			41		ns
t_{PLH}	UNCK ↑	Q			62			62		ns
t_{PHL}	UNCK ↑	Q			53			53		ns
t_{PLH}	OE ↓	Q			23			23		ns
t_{PHL}	OE ↑	Q			25			25		ns

NOTE 2: For load circuits and voltage waveforms, see page 1-12.

schematics of inputs and outputs



TYPICAL APPLICATIONS INFORMATION

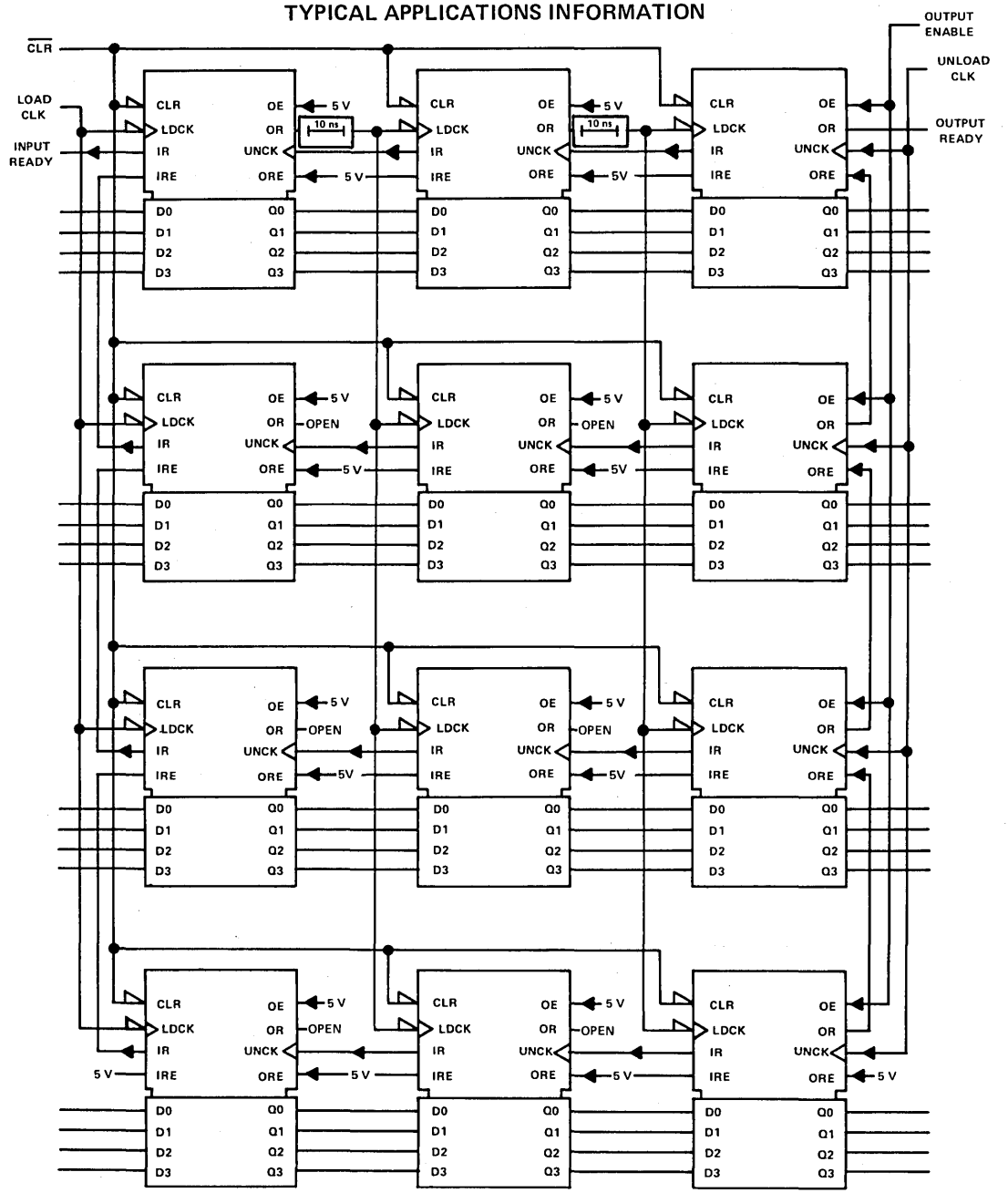


FIGURE 1–46-WORD BY 16-BIT EXPANSION USING 'LS222

10 ns ≡ Noninverting delay ⩾ 10 ns (e.g., 2 stages of 'LS04), 2 places.

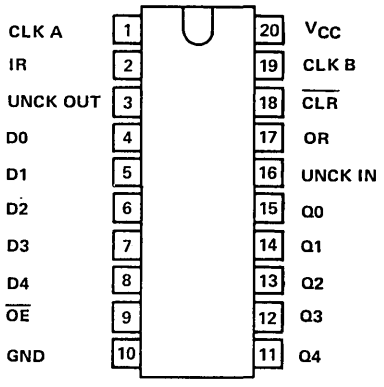
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TYPE SN74S225
16 x 5 ASYNCHRONOUS FIRST-IN FIRST-OUT MEMORY

D1733, SEPTEMBER 1976 – REVISED JUNE 1979

- Independent Synchronous Inputs and Outputs
- Organized as 16-Words of 5 Bits
- DC to 10-MHz Data Rate
- 3-State Data Outputs
- 20-Pin, 300-mil, High-Density Package

SN74S225 . . . J OR N PACKAGE
(TOP VIEW)



This device is also available in a chip carrier. See Product Guide, Section 7, for pin assignments.

description

This 80-bit active-element memory is a monolithic Schottky-clamped transistor-transistor logic (STTL) array organized as 16 words of five-bits each. A memory system using the SN74S225 can easily be expanded in multiples of 16 words or of 5 bits as shown in Figure 2. The three-state outputs controlled by a single enable, OE, make bus connection and multiplexing easy.

operation

A FIFO is a memory storage device which allows data to be written into and/or read from its array at independent data rates. The 'S225 is FIFO which will process data at any desired clock rate from DC to 10 MHz. The data is processed in a parallel format, word by word.

Reading or writing is done independently utilizing separate synchronous data clocks. Data may be written into the array on the low-to-high transition of either load clock input. Data may be read out of the array on the low-to-high transition of the unload clock input (normally high). Writing data into the FIFO may be accomplished in one of two manners: 1) In applications not requiring a clock control (gated), the clock input may be applied to both clock A and B inputs, 2) In applications needing a gated clock, the load clock (gate control) must be high in order for the FIFO to load on the next clock pulse. The clock A and B inputs can be used interchangeably for either clock gate control or clock input.

Status of the 'S225 is provided by three outputs. Input ready monitors the status of the last word location and signifies when the memory is full. This output is high whenever the memory is available to accept any data. The unload clock output also monitors the last word location. This output generates a low-logic-level pulse (synchronized to the internal clock pulse) when the location is vacant. The third status output, output ready, is high when the first word location contains valid data and unload clock input is high. When unload clock input goes low, output ready will go low and stay low until new valid data is in the first word position. The first word location is defined as the location from which data is provided to the outputs.

The data outputs are noninverted with respect to the data inputs and are three-state with a common control input, output enable. When output enable is low, the data outputs are enabled to function as totem-pole outputs. A high-logic-level forces each data output to a high-impedance state while all other inputs and outputs remain active.

The clear input invalidates all data stored in the memory array by clearing the control logic and setting output ready to a low-logic-level on the high-to-low transition of a low-active pulse.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U. S. Patent Number 3,463,975.

FUNCTION TABLES

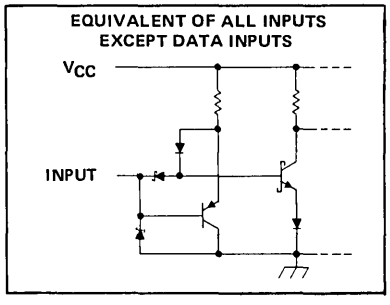
Table 1 – Input Functions

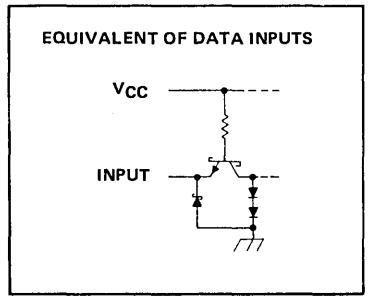
Input	Pin	Description
CLK A	1	Load Clock A
D0-D4	4-8	Data Inputs
$\overline{OE}$	9	Output Enable
UNCK IN	16	Unload Clock
$\overline{CLR}$	18	Clear
CLK B	19	Load Clock B
GND	10	Ground pin
V_{CC}	20	Supply Voltage

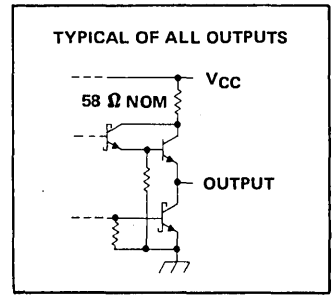
Table 2 – Output Functions

Output	Pin	Description
IR	2	Input Ready
UNCK OUT	3	Unload Clock
Q4-D0	11 - 15	Data Outputs
OR	17	Output Ready

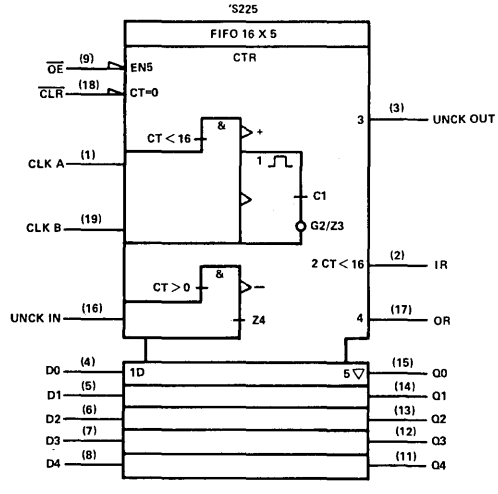
schematics of inputs and outputs







logic symbol



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltage, V_{CC} (see Note 1) 7V
Input Voltage 5.5V
Off-State Output Voltage 5.5V
Operating Free-Air Temperature Range . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

NOTE 1: All voltage values are with respect to network ground terminal.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply Voltage, V_{CC}		4.75	5	5.25	V
High-level output current, I_{OH}	All Outputs Except Data			−3.2	mA
	Data Outputs			−6.5	
Low-level output current, I_{OL}	All Outputs Except Data			8	mA
	Data Outputs			16	
Pulse Width	Load Clock A or B, t_w (high)	25			ns
	Unload Clock Input, t_w (low)	7			
	Clear, t_w (low)	40			
Setup Time	Data to Load Clock, t_{su} (Dli) See Note 2	−20↑			ns
	Clear Release to Load Clock, t_{su}	25↑			
Hold Time, Data from Load Clock, t_h(Dli)		70↑			ns
Operating free-air temperature, T_A		0		70	°C

NOTE 2: Data must be setup within 20 ns after the load clock positive transition.

↑ ≡ The arrow indicates that the low-to-high transition of the load clock is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.2	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = MAX	2.4	2.9		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = MAX		0.35	0.50	V
I_{OZH}	Off-state output current, high-level voltage applied		V_{CC} = MAX, V_{IL} = 0.8 V,	V_{IH} = 2 V, V_O = 2.4 V			50	μA
I_{OZL}	Off-state output current, low-level voltage applied		V_{CC} = MAX, V_{IL} = 0.8 V,	V_{IH} = 2 V, V_O = 0.5 V			-50	μA
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	Data In	V_{CC} = MAX,	V_I = 2.7 V			40	μA
		All Inputs Except Data In					25	
I_{IL}	Low-level input current	Data In	V_{CC} = MAX,	V_I = 0.5 V			−1	mA
		All Inputs Except Data In					−250	μA
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−30		−100	mA
I_{CC}	Supply Current		V_{CC} = MAX,	See Note 3		80	120	mA

†For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} −5 V, T_A = 25°C.
§Duration of the short circuit should not exceed one second.
NOTE 3: I_{CC} is measured with all inputs grounded and the output open.

switching characteristics over recommended operating ranges of T_A and V_{CC} (unless otherwise noted)

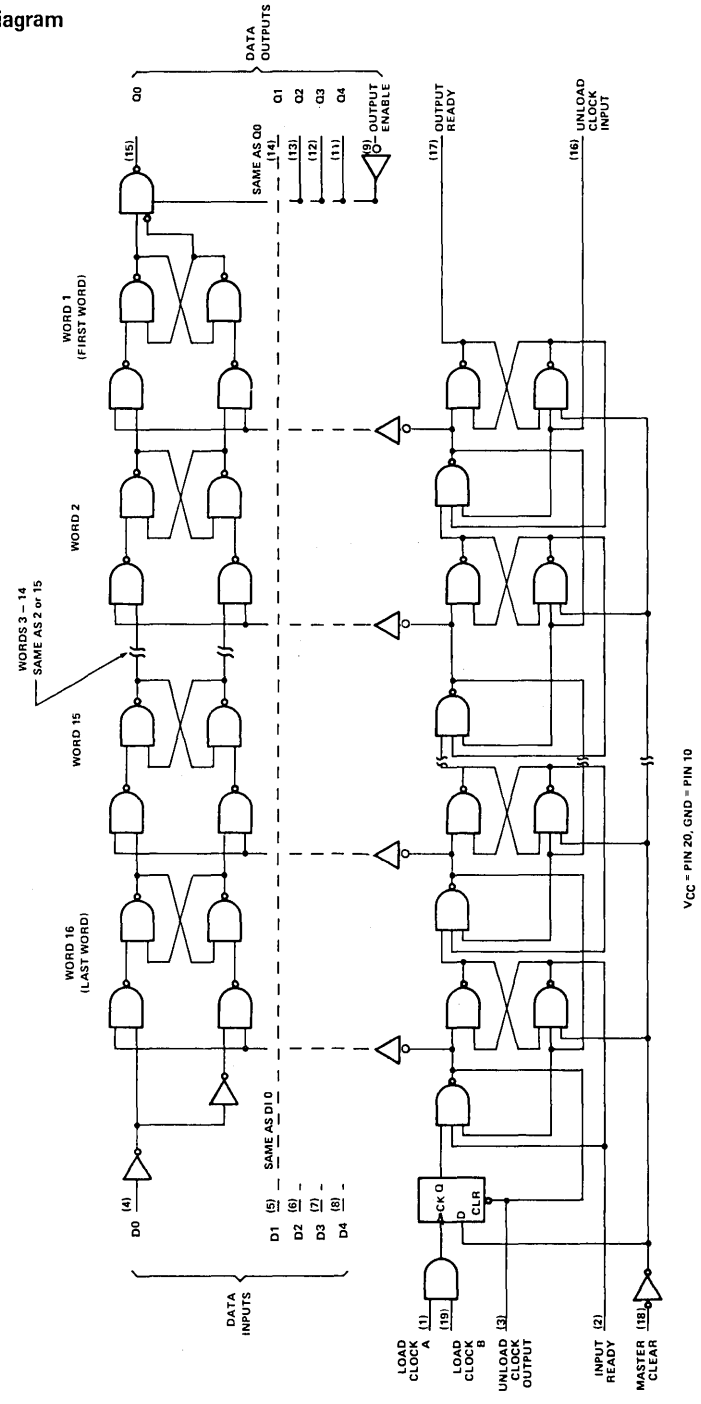
PARAMETERS¶	FROM	TO	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
f_{max}	CLK A		C_L = 30 pF, See Note 4	10	20		MHz
f_{max}	CLK B			10	20		MHz
f_{max}	UNCK IN			10	20		MHz
t_w	UNCK OUT			7	14		ns
t_{PXZ}	$\overline{OE}$	Qi	C_L = 5 pF		10	25	ns
t_{PZX}			C_L = 30 pF, See Note 4		25	40	
t_{PLH}	UNCK IN	Qi			50	75	ns
t_{PHL}					50	75	
t_{PLH}	CLK A or CLK B	OR			190	300	ns
t_{PLH}	UNCK IN	OR			40	60	ns
t_{PHL}					30	45	
t_{PHL}	$\overline{CLR}$	OR			35	60	ns
t_{PHL}	CLK A or CLK B	UNCK OUT			25	45	ns
t_{PHL}	UNCK IN	UNCK OUT			270	400	ns
t_{PHL}	CLK A or CLK B	IR			55	75	ns
t_{PLH}	UNCK IN	IR			255	400	ns
t_{PLH}	$\overline{CLR}$	IR			16	35	ns
t_{PLH}	OR↑	Qi			10	20	ns

¶ f_{max} ≡ maximum clock frequency.
t_w ≡ pulse width (output)
↑↓ ≡ The arrow indicates that the low-to-high (↑) or high-to-low (↓) transition of the output ready (OR) output is used for reference.
t_{PLH} ≡ propagation delay time, low-to-high level output.
t_{PHL} ≡ propagation delay time, high-to-low-level output.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 4: Load circuit and voltage waveforms are shown on page 1-12.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

functional block diagram



TYPICAL WAVEFORMS FOR A 16-WORD FIFO

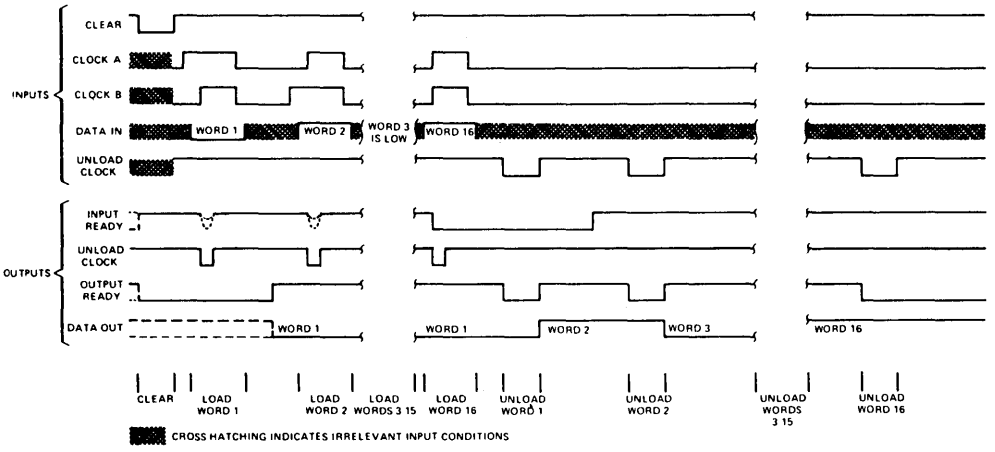


FIGURE 1 – TYPICAL WAVEFORMS FOR A 16-WORD FIFO

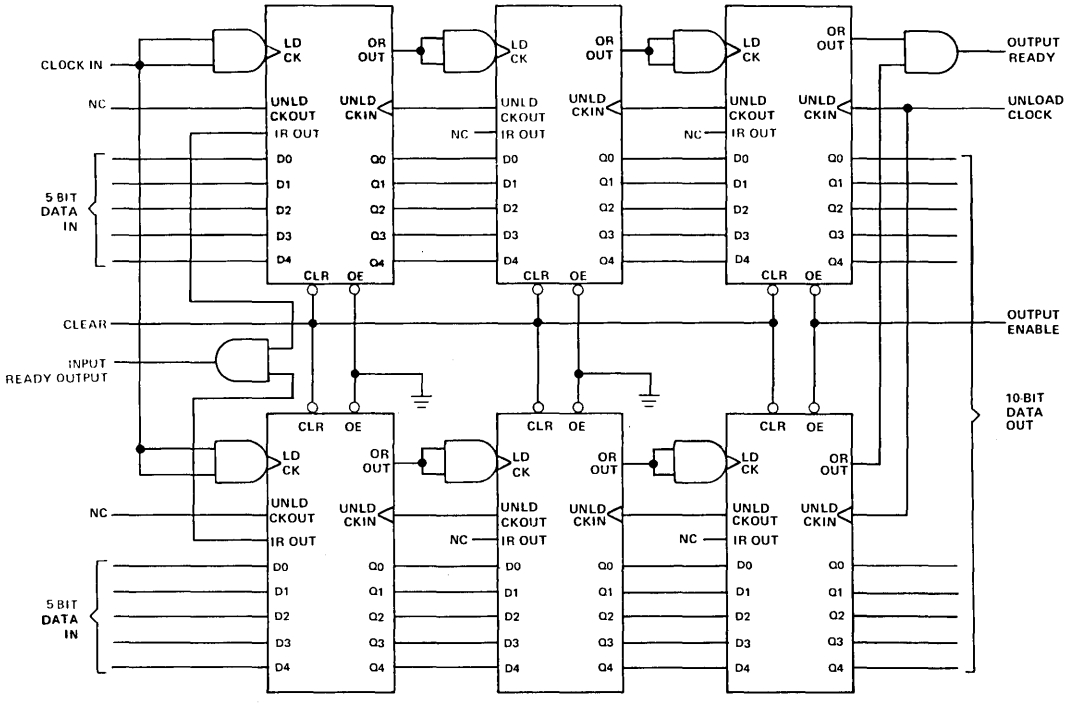


FIGURE 2 – EXPANDING THE 'S225 FIFO (48 WORDS OF 10 BITS SHOWN)

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

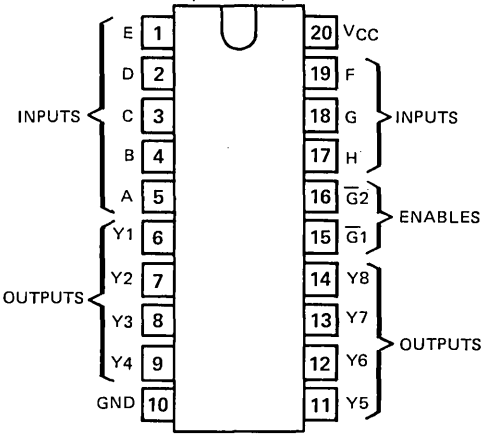
TYPES SN54S484, SN54S485, SN74S484, SN74S485
BCD-TO-BINARY AND BINARY-TO-BCD CONVERTERS

D2534, JUNE 1979

SN54S484, SN74S484 BCD-TO-BINARY CONVERTERS
SN54S485, SN74S485 BINARY-TO-BCD CONVERTERS

- Significant Savings in Package Count Compared with SN54184, SN54185A, SN74184, or SN74185A (Over Half in Many Applications)
- Three-State Outputs

SN54S484, SN54S485 . . . J PACKAGE
SN54S484, SN54S485 . . . J OR N PACKAGE
(TOP VIEW)



description

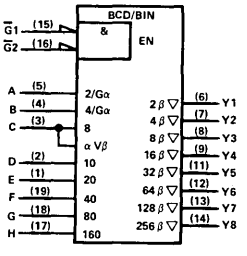
These monolithic converters are derived from the SN54S371/SN74S371 custom-programmed read-only memories. Both of these converters comprehend that the least-significant bits (LSB) of the binary and BCD are logically equal, and in each case the LSB bypasses the converter as shown in the typical applications. This means that a nine-bit converter is produced in each case. The devices are cascadable to N bits.

The three-state outputs offer the convenience of open-collector outputs with the speed of totem-pole outputs: they can be bus-connected to other similar outputs yet they retain the fast rise-time characteristic of totem-pole outputs. A high logic level at either enable ($\overline{G}$) input causes the outputs to be in a high-impedance state.

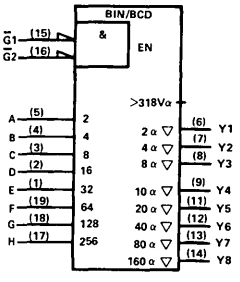
In many applications these converters can, by including 3 more bits than the SN54184/SN74184 or SN54185/SN74185, reduce power consumption significantly and package count by more than half as shown in the tables below.

logic symbols

SN54S484
SN74S484



SN54S485,
SN74S485



SN54S484/SN74S484 vs SN54184/SN74184

DECADES	PACKAGE COUNT		MAXIMUM SUPPLY CURRENT (A)		TYPICAL ACCESS TIME @ T_A = 25°C (ns)	
	'S484	'184	'S484	'184	'S484	'184
3	3	6	0.41	0.59	117	135
4	5	11	0.72	1.09	180	189
5	8	18	1.18	1.78	270	270
6	12	27	1.75	2.67	342	351
7	16	38	2.37	3.76	405	405
8	21	49	3.14	4.85	495	485
9	27	62	4.02	6.14	567	540

These devices are also available in chip carriers. See Product Guide, Section 7, for pin assignments.

SN54S485/SN74S485 vs SN54185/SN74185

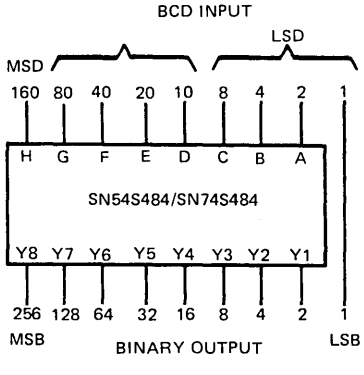
BINARY BITS	PACKAGE COUNT		MAXIMUM SUPPLY CURRENT (A)		TYPICAL ACCESS TIME @ T_A = 25°C (ns)	
	'S485	'185	'S485	'185	'S485	'185
8	2	3	0.25	0.30	72	81
16	8	16	1.12	1.58	252	216
24	19	40	2.67	3.96	459	351
32	33	74	4.78	5.45	612	486

TYPES SN54S484, SN54S485, SN74S484, SN74S485
BCD-TO-BINARY AND BINARY-TO-BCD CONVERTERS

SN54S484, SN74S484
BCD-TO-BINARY CONVERTER
FUNCTION TABLE

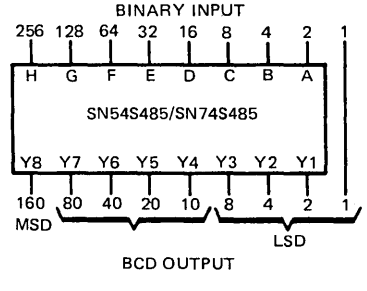
INPUTS								OUTPUTS							
H	G	F	E	D	C	B	A	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1
160	80	40	20	10	8	4	2	256	128	64	32	16	8	4	2
L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	H
L	L	L	L	L	L	H	L	L	L	L	L	L	L	H	L
L	L	L	L	L	L	H	H	L	L	L	L	L	L	H	H
L	L	L	L	L	H	L	L	L	L	L	L	L	H	L	L
L	L	L	L	L	H	L	H	Invalid BCD code (All outputs are high)							
L	L	L	L	L	H	H	L								
L	L	L	L	L	H	H	H								
L	L	L	L	H	L	L	L	L	L	L	L	L	H	L	H
L	L	L	L	H	L	L	H	L	L	L	L	L	H	H	L
L	L	L	L	H	L	H	L	L	L	L	L	L	H	H	H
H	H	H	H	L	L	H	L	H	L	L	H	H	L	L	L
H	H	H	H	L	L	H	H	H	L	L	H	H	L	L	H
H	H	H	H	L	H	L	L	H	L	L	H	H	L	H	L
H	H	H	H	L	H	L	H								
H	H	H	H	L	H	H	L								
H	H	H	H	L	H	H	H								
H	H	H	H	H	L	L	L	H	L	L	H	H	L	H	H
H	H	H	H	H	L	L	H	H	L	L	H	H	H	L	L
H	H	H	H	H	L	H	L	H	L	L	H	H	H	L	H
H	H	H	H	H	L	H	H	H	L	L	H	H	H	H	L
H	H	H	H	H	H	L	L	H	L	L	H	H	H	H	H
H	H	H	H	H	H	L	H								
H	H	H	H	H	H	H	L								
H	H	H	H	H	H	H	H								
X	X	X	X	X	H	X	H	H	H	H	H	H	H	H	H
X	X	X	X	X	H	H	X	H	H	H	H	H	H	H	H

H = high level L = low level X = irrelevant



SN54S485, SN74S485
BINARY-TO-BCD CONVERTER
FUNCTION TABLE

INPUTS								OUTPUTS							
H	G	F	E	D	C	B	A	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1
256	128	64	32	16	8	4	2	160	80	40	20	10	8	4	2
L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	H
L	L	L	L	L	L	H	L	L	L	L	L	L	L	H	L
L	L	L	L	L	L	H	H	L	L	L	L	L	L	H	H
L	L	L	L	L	H	L	L	L	L	L	L	L	H	L	L
L	L	L	L	L	H	L	H	L	L	L	L	L	H	L	H
L	L	L	L	L	H	H	L	L	L	L	L	L	H	H	L
L	L	L	L	L	H	H	H	L	L	L	L	L	H	H	H
L	L	L	L	H	L	L	L	L	L	L	L	H	L	L	L
L	L	L	L	H	L	L	H	L	L	L	L	H	L	L	H
L	L	L	L	H	L	H	L	L	L	L	L	H	L	H	L
L	L	L	L	H	L	H	H	L	L	L	L	H	L	H	H
L	L	L	H	L	L	L	L	L	L	L	H	L	H	L	L
L	L	L	H	L	L	L	H	L	L	L	H	L	H	L	H
L	L	L	H	L	L	H	L	L	L	L	H	L	H	H	L
L	L	L	H	L	L	H	H	L	L	L	H	L	H	H	H
L	L	L	H	L	H	L	L	L	L	L	H	H	L	L	L
L	L	L	H	L	H	L	H	L	L	L	H	H	L	L	H
L	L	L	H	L	H	H	L	L	L	L	H	H	L	H	L
L	L	L	H	L	H	H	H	L	L	L	H	H	L	H	H
L	L	L	H	H	L	L	L	L	L	L	H	H	H	L	L
L	L	L	H	H	L	L	H	L	L	L	H	H	H	L	H
L	L	L	H	H	L	H	L	L	L	L	H	H	H	H	L
L	L	L	H	H	L	H	H	L	L	L	H	H	H	H	H
L	L	L	H	H	H	L	L	L	L	L	H	H	H	H	L
L	L	L	H	H	H	L	H	L	L	L	H	H	H	H	H
L	L	L	H	H	H	H	L	L	L	L	H	H	H	H	L
L	L	L	H	H	H	H	H	L	L	L	H	H	H	H	H
H	L	H	L	L	L	L	L								
thru								H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H								



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) 7V
Input voltage 5.5V
Off-state output voltage 5.5V
Operating free-air temperature range: SN54S484, SN54S485 . . . . . −55°C to 125°C
SN74S484, SN74S485 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

	SN54S'			SN74S'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Off-state output voltage			5.5			5.5	V
High-level output current, I_{OH}			−2			−6.5	mA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

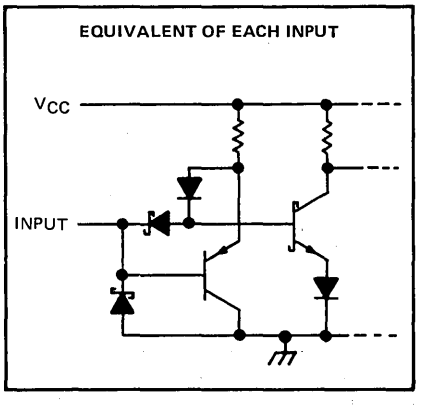
PARAMETER		TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = -18 mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, I_{OH} = MAX	V_{IH} = 2 V,	V_{IL} = 0.8 V,	2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = MAX	V_{IH} = 2 V,	V_{IL} = 0.8 V,			0.5	V
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX,	V_{IH} = 2 V,	V_O = 2.7 V			50	μA
I_{OZL}	Off-state output current low-level voltage applied	V_{CC} = MAX,	V_{IH} = 2 V,	V_O = 0.4 V			−50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V				25	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.5 V				−0.25	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX,			−30		−100	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 2			105	155	mA
C_O	Off-state output capacitance	V_{CC} = 5 V,	V_O = 5 V,	f = 1 MHz		6.5		pF

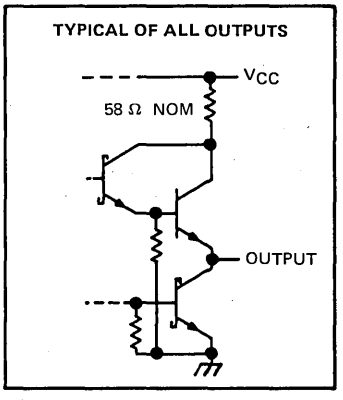
switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54S'			SN74S'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$t_{a(ad)}$	Access time from address	C_L = 30 pF,	See Note 3		45	95		45	70	ns
t_{PZX}	Output enable time	C_L = 30 pF,	See Note 3		15	45		15	30	ns
t_{PXZ}	Output disable time	C_L = 5 pF,	See Note 3		10	40		10	25	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
NOTES: 1. Voltage values are with respect to network ground terminal.
2. With outputs open and enable ($\overline{G}$) inputs grounded, I_{CC} is measured first by selecting a word that contains the maximum number of high-level outputs, then be selecting a word that contains the maximum number of low-level inputs.
3. Load circuit and voltage waveforms are shown on page 1-12.

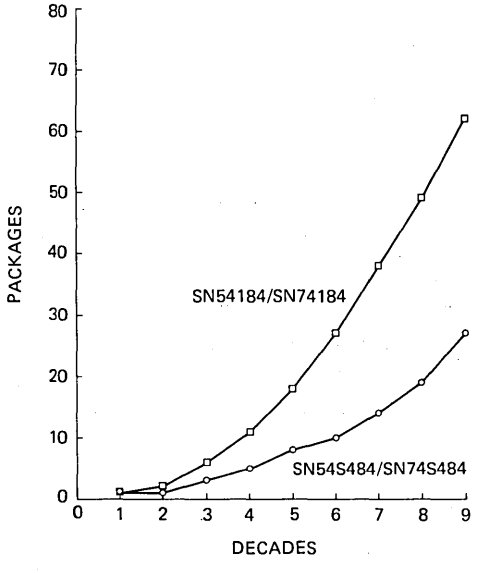
schematics of inputs and outputs



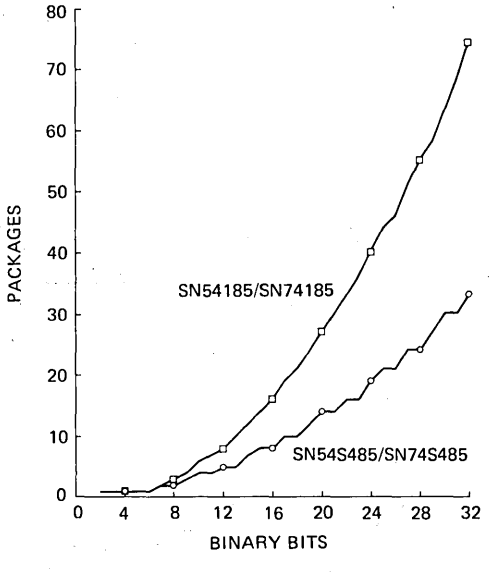


TYPICAL APPLICATION DATA

PACKAGES REQUIRED
vs
DECADES OF CONVERSION

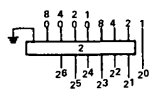


PACKAGES REQUIRED
vs
BINARY BITS OF CONVERSION

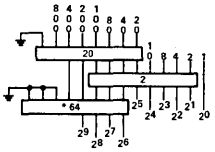


TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

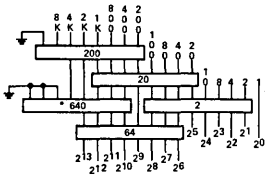
TYPICAL APPLICATION DATA
SN54S484, SN74S484



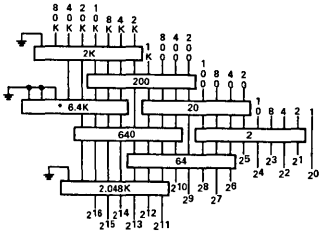
2-DECADE-BCD-TO-BINARY CONVERTER



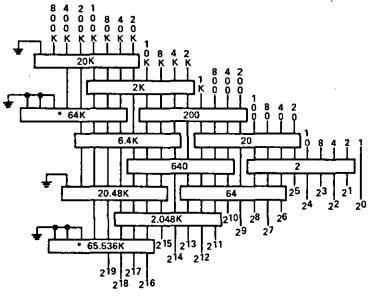
3-DECADE-BCD-TO-BINARY CONVERTER



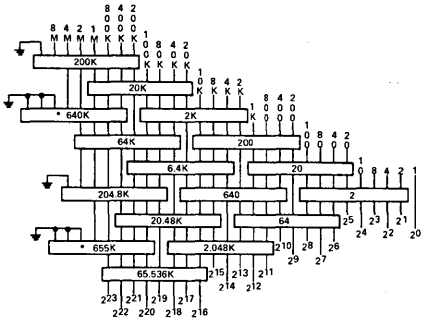
4-DECADE-BCD-TO-BINARY CONVERTER



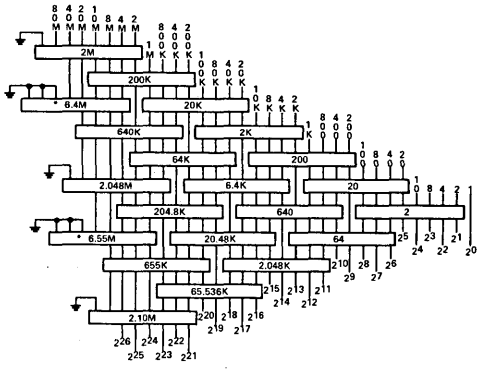
5-DECADE-BCD-TO-BINARY CONVERTER



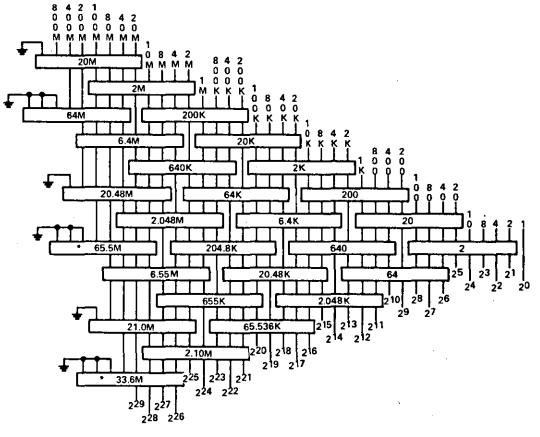
6-DECADE-BCD-TO-BINARY CONVERTER



7-DECADE-BCD-TO-BINARY CONVERTER



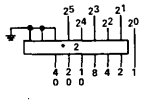
8-DECADE-BCD-TO-BINARY CONVERTER



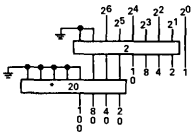
9-DECADE-BCD-TO-BINARY CONVERTER

*SN54184/SN74184 can be used.
K = 10^3, M = 10^6

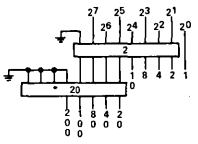
TYPICAL APPLICATION DATA
SN54S485, SN74S485



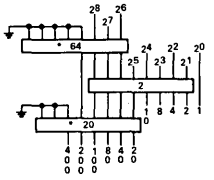
6-BIT-BINARY-TO-BCD CONVERTER



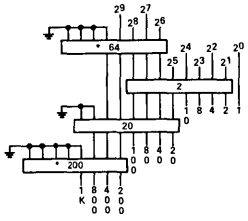
7-BIT-BINARY-TO-BCD CONVERTER



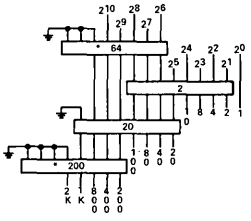
8-BIT-BINARY-TO-BCD CONVERTER



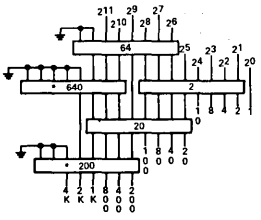
9-BIT-BINARY-TO-BCD CONVERTER



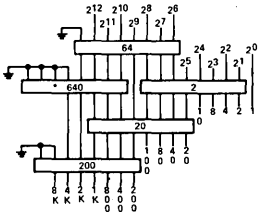
10-BIT-BINARY-TO-BCD CONVERTER



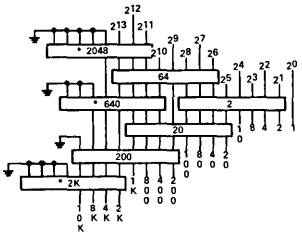
11-BIT-BINARY-TO-BCD CONVERTER



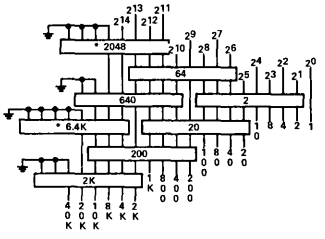
12-BIT-BINARY-TO-BCD CONVERTER



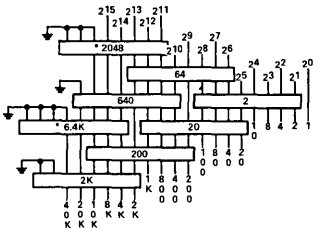
13-BIT-BINARY-TO-BCD CONVERTER



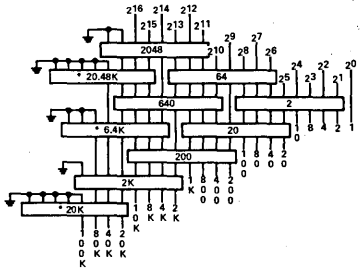
14-BIT-BINARY-TO-BCD CONVERTER



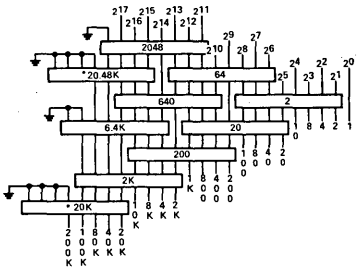
15-BIT-BINARY-TO-BCD CONVERTER



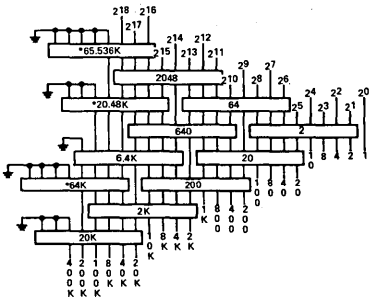
16-BIT-BINARY-TO-BCD CONVERTER



17-BIT-BINARY-TO-BCD CONVERTER



18-BIT-BINARY-TO-BCD CONVERTER

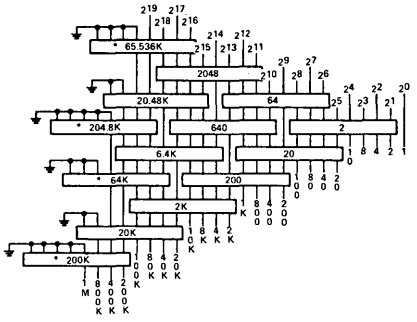


19-BIT-BINARY-TO-BCD CONVERTER

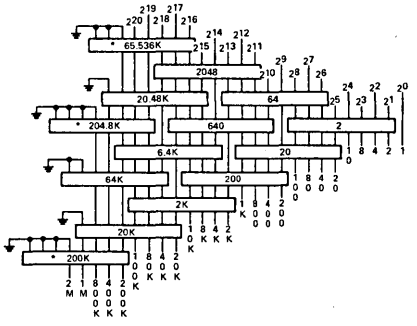
*SN54185/SN74185 can be used.
K = 10^3, M = 10^6

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

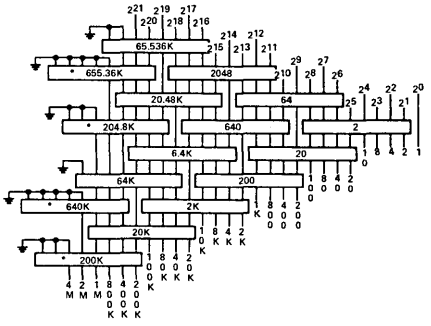
TYPICAL APPLICATION DATA
SN54S485/SN74S485



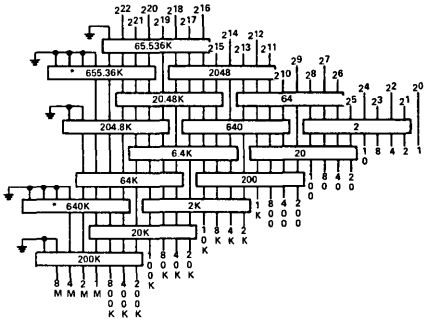
20-BIT-BINARY-TO-BCD CONVERTER



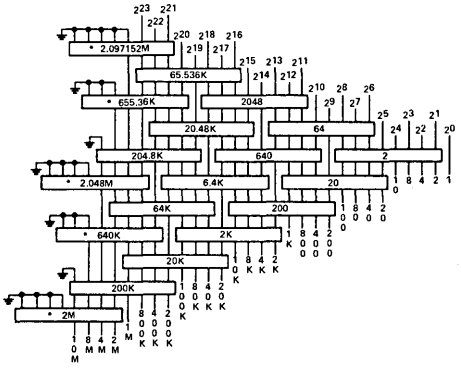
21-BIT-BINARY-TO-BCD CONVERTER



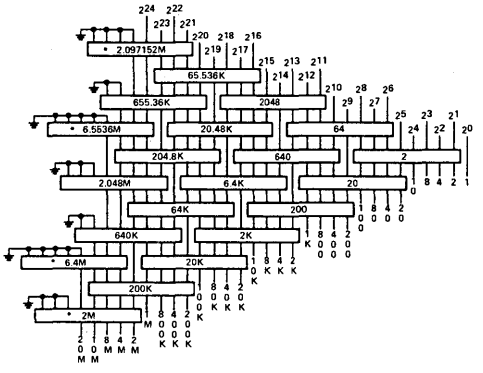
22-BIT-BINARY-TO-BCD CONVERTER



23-BIT-BINARY-TO-BCD CONVERTER



24-BIT-BINARY-TO-BCD CONVERTER

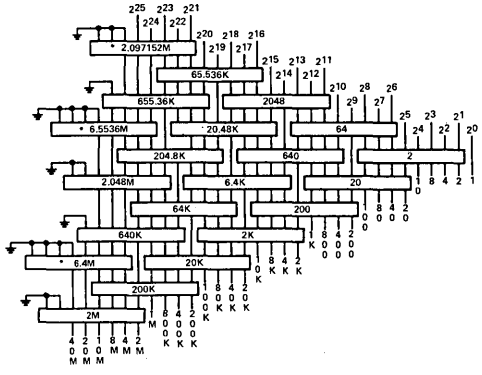


25-BIT-BINARY-TO-BCD CONVERTER

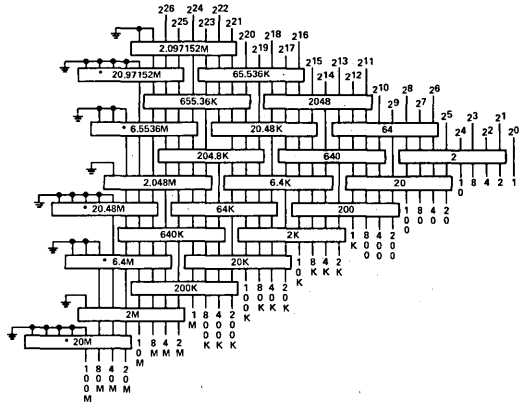
*SN54185/SN74185 can be used.

$K = 10^3$, $M = 10^6$

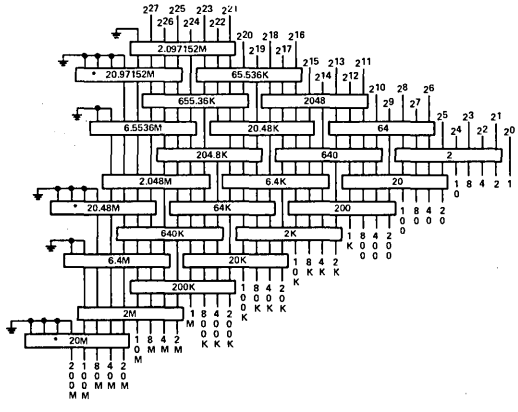
TYPICAL APPLICATION DATA
SN54S485, SN74S485



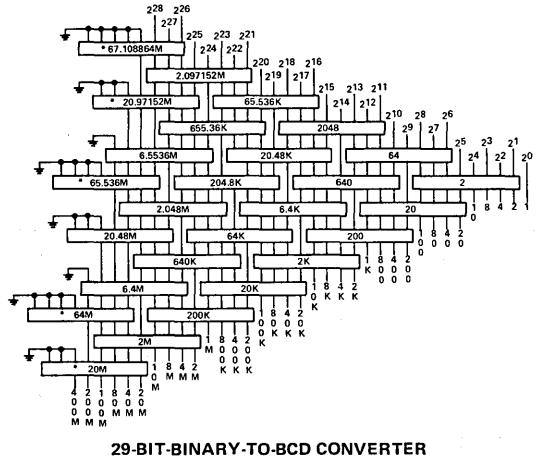
26-BIT-BINARY-TO-BCD CONVERTER



27-BIT-BINARY-TO-BCD CONVERTER



28-BIT-BINARY-TO-BCD CONVERTER

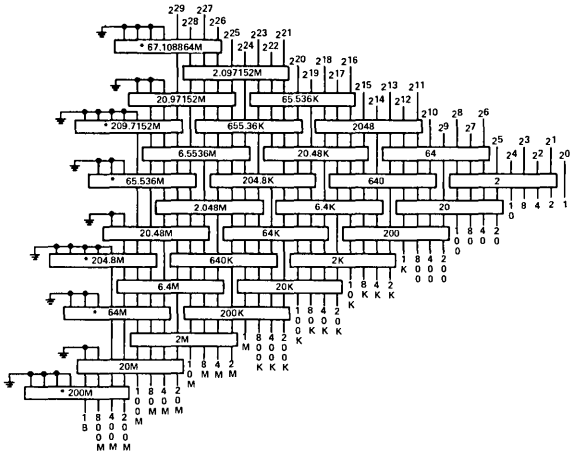


29-BIT-BINARY-TO-BCD CONVERTER

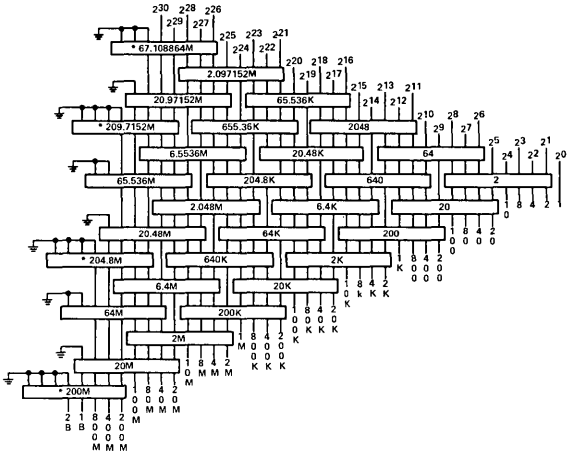
*SN54185/SN74185 can be used.
K = 10^3, M = 10^6

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

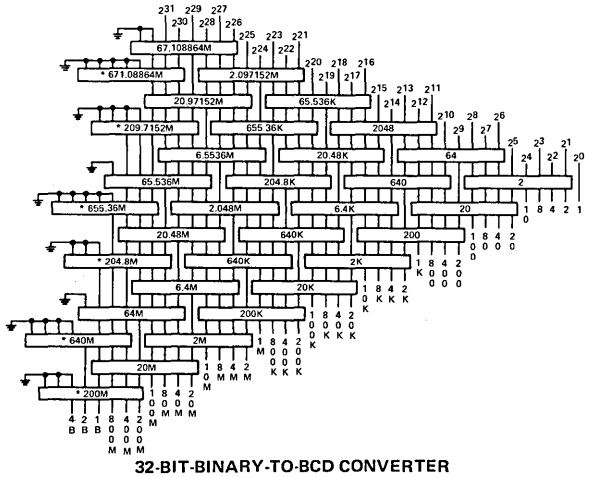
TYPICAL APPLICATION DATA
SN54S485, SN74S485



30-BIT-BINARY-TO-BCD CONVERTER



31-BIT-BINARY-TO-BCD CONVERTER



32-BIT-BINARY-TO-BCD CONVERTER

*SN54185/SN74185 can be used.

K = 10^3, M = 10^6

4-Bit-Slice Schottky Processor Components

Texas Instruments invented the integrated circuit, microprocessor, and microcomputer — technology milestones that made today's SN74LS481 and SN74S481 4-bit-slice Schottky processor components a reality. TI is a world leader in producing reliable, affordable advanced electronics. Being first is our tradition.

4-BIT-SLICE PROCESSOR COMPONENTS

TABLE OF CONTENTS

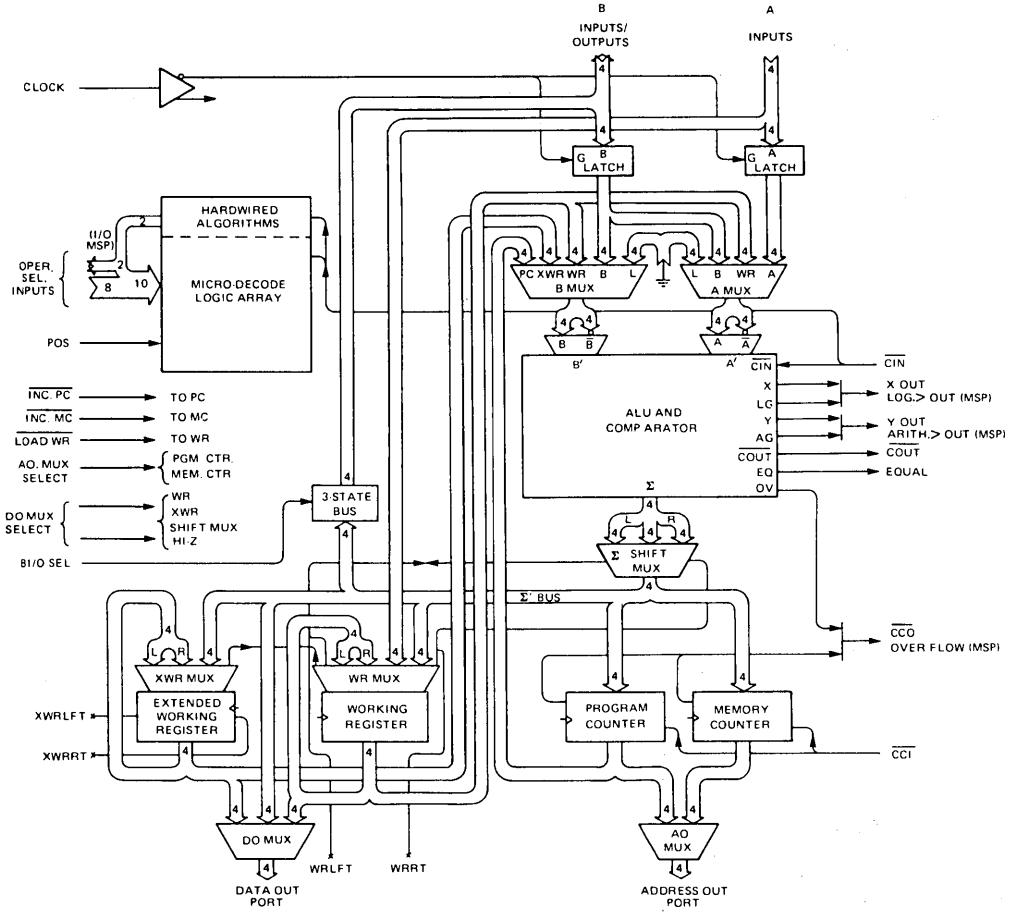
TABLE OF CONTENTS (Continued)

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Continued)

3

LIST OF TABLES



FUNCTIONAL BLOCK DIAGRAM FOR 'LS481/'S481

1 INTRODUCTION

These Schottky TTL 4-bit expandable parallel binary micro/macroprogrammable processor element building blocks are designed specifically for implementing high-performance digital computer/controllers. With the ability to efficiently emulate existing systems, they can be used to upgrade hardware performance with full compatibility to protect software investments.

Two performance ranges are available:

a. The SN74S481, Schottky TTL performs typically at a clock cycle time of 90 nanoseconds at 345 milliamperes of supply current.
b. The SN74LS481, low-power Schottky TTL performs typically at a clock cycle time of 120 nanoseconds at 220 milliamperes of supply current.

1.1 ARCHITECTURAL FEATURES

Designed with full parallel dual input/output ports, the memory-to-memory architecture provides a new dimension in interrupt processing or program context switching flexibilities. Static bipolar logic performs each microinstruction within a single clock cycle.

Primary among the architectural features are:

- Microprogrammable, bit-slice design is expandable in 4-bit multiples
- Full parallel dual input/output ports for use in advanced memory-to-memory architecture
- Full-function ALU with carry look-ahead, magnitude, and overflow decision capabilities
- Double-length accumulator with full shifting capability and sign-bit handling
- Dual memory address generators on-chip.

1.2 OPERATIONAL FEATURES

The functional capabilities, characterized by the 24,780 unique operations, coupled with the macroprogrammable multiply and divide algorithms, make these processor elements particularly attractive for implementing advanced high performance computers and controllers.

In addition to the full parallel data bus structure, the 'LS481/'S481 architecture also features asynchronous access to data routing and counter updating controls which, when combined with the most versatile instruction set available (see operational description) maximizes flexibility, efficiency, and performance. Simultaneous compound operations in the form of an ALU function with shift, plus destination selection with address/iteration updating, plus address *and* present data to memory can be accomplished in a single microcycle. Some other operational features are:

- Simultaneous one-clock compound operations, with status, can reduce microcycles and improve throughput
- Pre-programmed CRG and double-precision multiply/divide algorithms
- Double length accumulator with full bidirectional single/double precision arithmetic/logical/circulate shift capabilities include sign protection
- Full micro-operational control is provided for programming: address updating, data and address source selection, and direct transfer of data to working register or working memory
- Relative position control defines bit-slice rank and sign handling in N-bit applications.

1.3 MECHANICAL FEATURES

These processor elements are supplied in either a high-density quad-in-line ceramic package or a plastic dual-in-line package. The high-density 48-pin ceramic package has quad pin rows formed on 600- and 800-mil centers. Within each of the four rows, the pin spacing is 100 mils, center-to-center. The plastic dual-in-line package has standard 100-mil spacing on 600-mil centers. The outline drawing is provided on page 9-9 of this book.

TABLE 1
FUNCTIONAL DESCRIPTIONS

PIN NUMBER	PIN NAME	PIN FUNCTION	INPUT, OUTPUT, OR INPUT/OUTPUT
46, 47 1, 2	BI/O0, BI/O1 BI/O2, BI/O3	4-bit parallel data input port to the B latch, or 4-bit parallel data output for the Σ-bus when not being used as an input.	Inputs/Outputs
6, 5 4, 3	AI0, AI1 AI2, AI3	4-bit parallel data input port to the A latch and WR.	Inputs
7, 8 9, 10 17, 14 13, 11 15, 16	OP0, OP1 OP2, OP3 OP4, OP5 OP6, OP7 OP8, OP9	OP0 through OP9 serve as a 10-bit parallel operation-select input to the micro-decode logic array. In the most-significant position, OP8 and OP9 additionally serve as open-collector outputs during multiply and divide algorithms. In the least-significant position, OP9 serves as an open-collector output during the CRC algorithm.	Inputs
12	V_{CC}	Single 5-volt power-supply terminal.	Supply Voltage Pin
18	$\overline{CIN}$	Receives low-active ripple carry input data.	Input
19	POS	Directs internal and input/output end-conditions required to define the relative position of each bit-slice when N-SN74S481's are cascaded to implement Nx4-bit word lengths. When biased at 2.4 volts, the package operates as the least-significant (LSP) slice; when grounded, it functions as an intermediate (IP) slice; and when high, 5 volts, it functions as the most-significant (MSP) slice.	Input
20	Y/AG	In least-significant and intermediate positions outputs arithmetic carry generate (Y) for use with look-ahead. In most-significant position outputs true arithmetically-greater-than signal.	Output
21	X/LG	In least-significant and intermediate positions outputs arithmetic carry propagate (X) for use with look-ahead. In most-significant position outputs true logically-greater-than signal.	Output
22	$\overline{COUT}$	Outputs low-active ripple carry data.	Output
23	EQ	Outputs true (active-high) equality of Σ' bus equals zero for each 4-bit slice. The open-collector output permits wire-AND to achieve Nx4-bit equality output.	Open-Collector Output
24	$\overline{LD\,WR}$	When low, data applied at the AI port coincident with the ↑ clock transition is loaded into the WR.	Input
26 25	WRRT, WRLFT	Working register and Σ-bus shift interconnectivity pins. WRRT receives left-shift and outputs right-shift (true) data. WRLFT receives right-shift and outputs left-shift (true) data. Shift can be single-precision, double-precision, signed or unsigned.	Bidirectional I/O
28 27	XWRRT, XWRLFT	Extended working register shift interconnectivity pins. XWRRT receives left-shift and outputs right-shift (true) data. XWRLFT receives right-shift and outputs left-shift (true) data. Shift can be single-precision, double-precision, signed or unsigned.	Bidirectional I/O
29 30	D0 D1	Selects one of three DOP sources (WR, XWR, or Σ-bus) or places the DOP outputs in a high-impedance state.	Inputs
34 33 32 31	DOP0 DOP1 DOP2 DOP3	4-bit parallel, data-out port. DOP0 is LSB.	3-state outputs
35	$\overline{INCMC}$	When low, enables the MC to increment as directed by $\overline{CCI}$ on the next ↑ clock transition. When high, inhibits MC to hold mode. As $\overline{CCO}$ is common to MC and PC, the MC should be inhibited when PC is enabled.	Input
36	GND	Common or ground terminal for the supply voltage.	
37	$\overline{CCO}$/OV	In least-significant and intermediate positions a low-level output indicates that either the PC or MC is at maximum count. As $\overline{CCO}$ is common for both PC and MC ambiguous carry can be avoided if one or both counters is/are disabled by the $\overline{INCPC}$ and/or $\overline{INCMC}$ inputs. In the most-significant position, a high-level output, depending on the operation selected, indicates that the WR, XWR, or ALU will overflow (OV) on the next clock.	Output

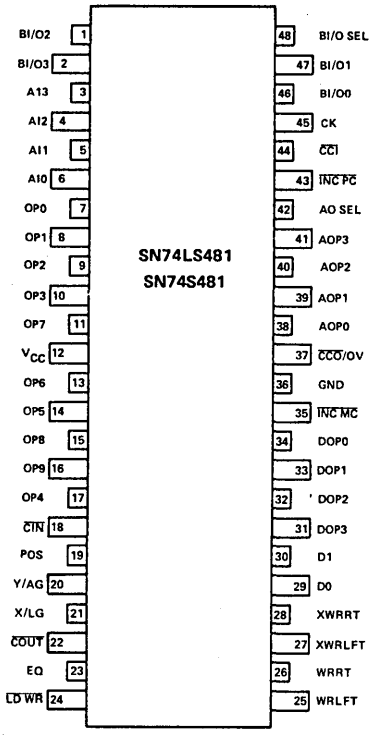


FIGURE 1—PIN ASSIGNMENTS

TABLE 1 (Continued)

PIN NUMBER	PIN NAME	PIN FUNCTION	INPUT, OUTPUT, OR INPUT/OUTPUT
38, 39 40, 41	AOP0, AOP1 AOP2, AOP3	4-bit parallel address-out port.	Outputs
42	A0	Selects one of two AOP sources (PC or MC).	Input
43	$\overline{\text{INCPC}}$	When low, enables the PC to increment as directed by $\overline{\text{CCI}}$ on the next ↑ clock transition. When high, inhibits PC to hold mode. As $\overline{\text{CCO}}$ is common to PC and MC, the PC should be inhibited when MC is enabled.	Input
44	$\overline{\text{CCI}}$	In least-significant position, a low input directs enabled PC or enabled MC to increment by one on next ↑ clock transition. In the LSP, a high directs enabled PC or enabled MC to increment by 2. In other positions, a low is a carry input and a high inhibits the counter.	Input
45	CK	When high, enables the transparency of A and B input latches. When low, latches A and B input data. Clocks synchronous registers and counters on the positive transition.	Input
48	BI/O SEL	When low, enables BI/O to output Σ-bus data. When high, the BI/O output drivers are placed in a high-impedance state permitting BI/O to be used as data inputs.	Input

2. DETAILED FUNCTIONAL DESCRIPTIONS

2.1 MICRO-DECODING LOGIC ARRAY

The micro-decoding logic array is a dedicated 11-input PLA decoding 73 product terms to generate 24 control lines needed to implement the 14 operation forms. The eleven inputs consist of the ten operation select lines (OP0 through OP9) and the ALU carry input. The carry input, utilized as an additional operation select line during operation forms not performing arithmetic functions, maximizes system pin efficiency and functional density.

In an expanded word length system (two or more 'LS481/'S481's), operation select inputs 8 (OP8) and 9 (OP9) assume an input/output capability in the most-significant or least-significant package as a result of the position control and the type of operation being performed. During microprogrammable operation forms I through IX, OP8 and OP9 function simply as another input; but, during the macroprogrammable operations of forms X through XIV one or both become an output during iterations. Table 2 summarizes by operation form the control (output) package and the operation lines which are used as an output.

TABLE 2
MSP OP8 and OP9 ITERATIVE FUNCTION SUMMARY

OP. FORM	ALGORITHM	CONTROL PACKAGE	OPERATION SELECT I/O	
			OP8	OP9
I thru IX	All	None	INPUT	INPUT
X	CRC ACCUMULATION	LSP	INPUT	OUTPUT
XI	SIGNED DIVIDE	MSP	OUTPUT	OUTPUT
XII	UNSIGNED DIVIDE	MSP	INPUT	OUTPUT
XIII	UNSIGNED MULTIPLY	MSP	INPUT	OUTPUT
XIV	SIGNED MULTIPLY	MSP	OUTPUT	OUTPUT

If the macroinstructions are to be used in an expanded word length, OP8 and OP9 select lines of the MSP and the OP9 line of the LSP should be driven from either a 3-state output (which can be placed in high-impedance state) or an open-collector output (which can be wire-OR'ed with the OP select I/O lines). During an iterative function for which the OP line is designated as an open-collector output, the OP line driver should be placed in a high-impedance or off state permitting the output function to drive similar OP lines in the remaining packages.

The output state of OP8 or OP9 is a function of on-chip status decoder as enumerated in the flow diagrams illustrating the five algorithms.

2.2 RELATIVE POSITION CONTROL (POS)

The single line position control, with the ability of decoding one of three input logic states, provides each 'S481 in an expanded word length system with the capability of identifying its relative position. The relative positions, with the corresponding input logic levels are enumerated in Table 3.

TABLE 3
POSITION CONTROL FUNCTIONS

POS INPUT LOGIC LEVEL	RELATIVE POSITION
$\geq$ 3.6 V	MOST-SIGNIFICANT POSITION (MSP)
1.8 V to 3 V	LEAST-SIGNIFICANT POSITION (LSP)
$\leq$ 0.8 V	INTERMEDIATE POSITION (IP)

The relative position identification dictates how each 'LS481/'S481 in the system handles the multi-purpose I/O accommodations and ALU sign and magnitude functions. See Table 4. Shift/Circulate interconnectivity bit transfers are explained in detail under shift/circulate transfer multiplexers.

TABLE 4
DUAL-FUNCTION LOGIC I/O PINS

PIN	MSP	IP	LSP
X/LG	LG (OUT)	X (IN)	X (IN)
Y/LG	AG (OUT)	Y (IN)	Y (IN)
$\overline{CCO}$/OV	OVERFLOW (OUT)	$\overline{CCO}$ (OUT)	$\overline{CCO}$ (OUT)

X AND Y ARE CARRY LOOK-AHEAD FUNCTIONS

2.3 CLOCK

The clock synchronizes the entry or change of data in the 'LS481/'S481 registers and counters, and it controls the status of the A and B input latches. A typical clock cycle is illustrated in Figure 1. The low-to-high transition of the clock input is the clocking edge for any combination of either the working register, extended working register, flag flip-flops, and the program counter or the memory counter activated by the resident operation. During the low-level portion of the clock input, both input latches are latched ensuring data stability at the positive clock transition. After the clock has gone to a high level, the input latches are placed in a transparent mode to accept the next set of input data.

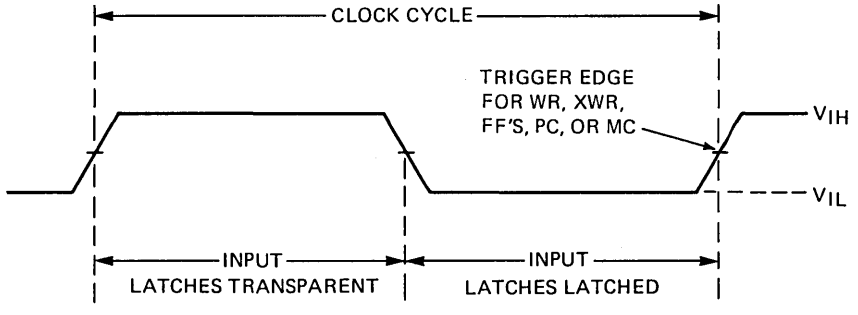


FIGURE 2 – CLOCK CYCLE

2.4 LATCHED DATA INPUT PORTS

The SN74LS481/SN74S481 features dual input ports combined with data flow paths which are designed specifically to reduce the number of system clock cycles needed to enter operands and/or data. Both the A and B input ports are latched, eliminating the need for external registers, to simplify interfacing directly with system data bus paths.

The A input port data is made available to both the input latch and the working register which allows A data to be loaded into the working register directly.

The B port is configured to serve as an input/output data path providing the capability to:

a. Input data to the B latch
b. Output sum-bus data.

This I/O port is designed specifically to simplify implementation of data transfers to the external working memory.

Both the A and B latches are transparent when the 'LS481/'S481 clock input is high. Data applied at the A and B inputs should be stable anytime prior to or at least coincident with the falling edge of the clock input (see Figure 3). After the clock falling edge, the data inputs should be held steady for $t_{hold(data)}$ or longer to facilitate the on-chip clock buffers to latch the data.

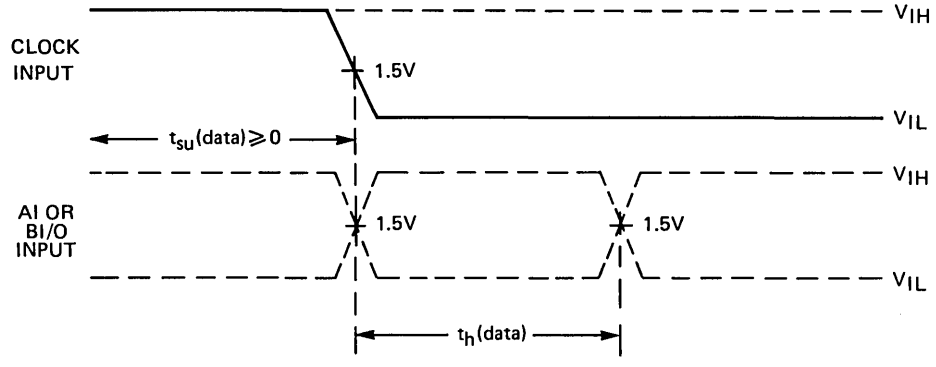


FIGURE 3 – INPUT LATCHES SETUP/HOLD TIMES

The A input port latch data is routed to the A input multiplexers, and the B input port latch data is sourced to both the A and B input multiplexers.

2.5 A AND B OPERAND SOURCES

The A and B input multiplexers source the ALU A' and B' ports through true/complement conditional inverter circuits. Data routing for each, illustrated and listed in Figure 4, provides the ALU with access to the true or complement of:

ALU A' PORT

1. A input latch
2. B input latch
3. Working Register
4. Low logic level inputs (force zeros)

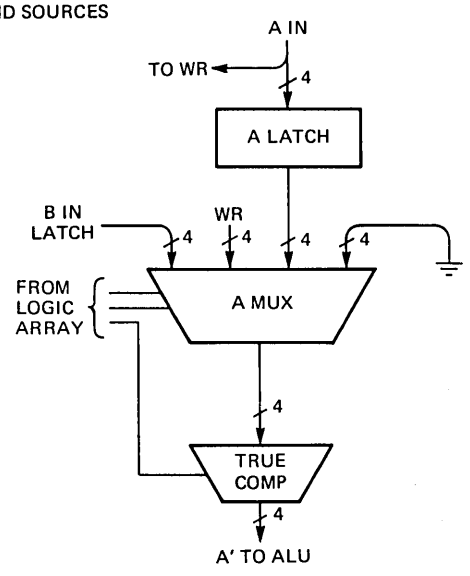
ALU B' PORT

1. B input latch
2. Sum bus
3. Working register
4. Extended working register
5. Program counter
6. Low logic level inputs (force zeros)

The A and B multiplexers and true complement circuits, under control of the resident operation code, are selectable at the microprogram level. The number of A or B multiplexer sources available depend upon the specific operation being performed by the 'LS481/'S481. Operation form descriptions contain detailed microprogramming.

The A and B input multiplexers, with selectable true and complement operand sources, maximizes the processing power of the 'LS481/'S481 by minimizing the active components needed to achieve both the simple but highly flexible data routing tasks and full ALU capabilities.

A OPERAND SOURCES

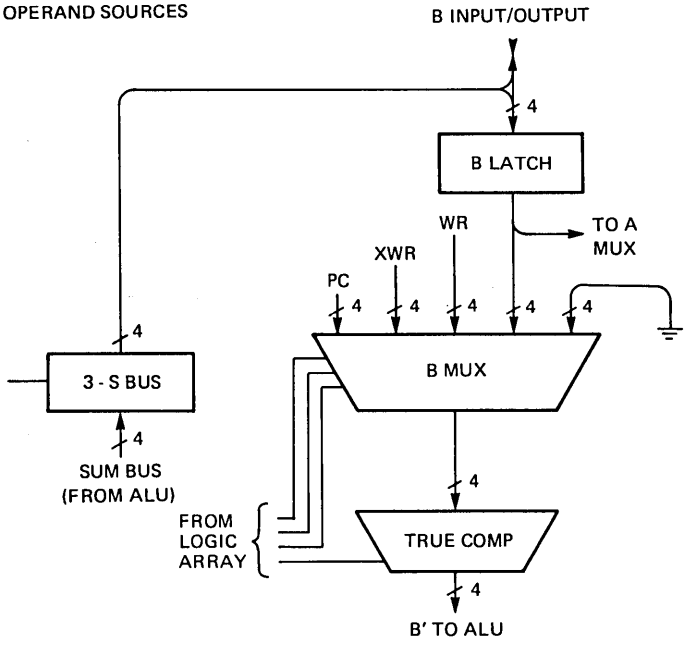


A INPUT SELECTIONS

$\overline{A}$ IN → A'
LOGIC ONE'S → A'
LOGIC ZERO'S → A'
B IN → A'
$\overline{B}$ IN → A'
WR → A'
$\overline{WR}$ → A'

3

B OPERAND SOURCES



B INPUT/OUTPUT SELECTIONS

B IN → B'
$\overline{B}$ IN → B'
LOGIC ONE'S → B'
LOGIC ZERO'S → B'
(B IN) • (WR) → B'
$\overline{(B\ IN) \cdot (WR)}$ → B'
WR → B'
$\overline{WR}$ → B'
(B IN) • (XWR) → B'
$\overline{(B\ IN) \cdot (XWR)}$ → B'
XWR → B'
$\overline{XWR}$ → B'
(B IN) • (PC) → B'
$\overline{(B\ IN) \cdot (PC)}$ → B'
PC → B'
$\overline{PC}$ → B'

FIGURE 4 – ALU OPERAND SOURCES

2.6 ARITHMETIC/LOGIC UNIT (ALU)

The 4-bit, parallel, binary arithmetic/logic unit provides the arithmetic/Boolean operand combination/modification mechanism including magnitude and overflow status. The ALU performs, as directed by the resident operation form, one of four basic functions which, when combined with the operand selections at the A and B multiplexers, extends the arithmetic/logic capabilities to that of a full 16-function ALU.

When compared to other bit-slice processor elements, unique to the 'LS481/'S481 arithmetic architecture are the parallel input ports and fully microprogrammable symmetry for all ALU functions within the selections of the A and B input multiplexers.

Logical and arithmetic operation forms for the 'LS481/'S481 are shown in Table 5. The full functional power of the 'LS481/'S481 can be visualized only if it is understood that although both ALU's have parallel A and B input ports, the 'S481 architecture not only provides access to multiple sources but has the capability to route true or complement of any source to the A and B ALU port. This means that for a subtract operation, the subtrahend may be either an A or B input. In addition to maximizing data routing capabilities of the 'LS481/'S481 at minimum logic/gate levels, this architecture permits fully symmetrical operations to be performed on the A or B sources within the selections offered by these 'S481 arithmetic/logical operation forms.

TABLE 5
'LS481/'S481 ALU AND LOGIC FUNCTIONS

DATA INPUT		TWO'S COMPLEMENT INTEGER ARITHMETIC OP'S		LOGICAL OP'S (FORM VIII) $\overline{CIN}$ = H OR L		
A PORT	B PORT	$\overline{CIN}$ = L	$\overline{CIN}$ = H	OR	NOR	EX-NOR
ZEROS	ZEROS	1	0	ZEROS	ONES	ONES
ZEROS	ONES	0	MINUS 1	ONES	ZEROS	ZEROS
ONES	ZEROS	0	MINUS 1	ONES	ZEROS	ZEROS
ONES	ONES	MINUS 1	MINUS 2	ONES	ZEROS	ONES
A	ZEROS	A PLUS 1	A	A	$\overline{A}$	$\overline{A}$
A	ONES	A	A MINUS 1	ONES	ZEROS	A
$\overline{A}$	ZEROS	MINUS A	MINUS A MINUS 1	$\overline{A}$	A	A
$\overline{A}$	ONES	MINUS A MINUS 1	MINUS A MINUS 2	ONES	ZEROS	$\overline{A}$
ZEROS	B	B PLUS 1	B	B	$\overline{B}$	$\overline{B}$
ONES	B	B	B MINUS 1	ONES	ZEROS	B
ZEROS	$\overline{B}$	MINUS B	MINUS B MINUS 1	$\overline{B}$	B	B
ONES	$\overline{B}$	MINUS B MINUS 1	MINUS B MINUS 2	ONES	ZEROS	$\overline{B}$
A	B	A PLUS B PLUS 1	A PLUS B	A + B	$\overline{A} \cdot \overline{B}$	$\overline{A \oplus B}$
A	$\overline{B}$	A MINUS B	A MINUS B MINUS 1	A + $\overline{B}$	$\overline{A} \cdot B$	A ⊕ B
$\overline{A}$	B	B MINUS A	B MINUS A MINUS 1	$\overline{A}$ + B	A · $\overline{B}$	A ⊕ B
$\overline{A}$	$\overline{B}$	MINUS A MINUS B MINUS 1	MINUS A MINUS B MINUS 2	$\overline{A}$ + B	A · B	$\overline{A \oplus B}$

Some unique one-clock arithmetic/iterative capabilities of the 'LS481/'S481 are listed in Table 6.

TABLE 6
EXTENDED ALU FUNCTIONS OF 'LS481/'S481

FORM NO.	FUNCTION
I	A (ALU) B · WR A (ALU) B · XWR A (ALU) B · PC
II	A (ALU) B DOUBLE-PRECISION SHIFTED LOGICAL LEFT OR RIGHT
III	A (ALU) B SINGLE-PRECISION SHIFTED LOGICAL OR ARITHMETIC LEFT OR RIGHT

Table 5 also indicates the 16 logical combinations of two Boolean variables which are selectable for the OR, NOR, and exclusive-NOR functions. Full symmetry of the ALU and the ability to select the complement of input data extends the logic functions for performance of:

a. NAND
b. AND
c. Exclusive-OR
d. Mixed combinations of each
e. Transfer functions for true or inverted data
f. All ones or all zeros.

2.7 ALU MAGNITUDE AND CARRY FUNCTIONS

The 'LS481/'S481 ALU is fully decoded on chip to generate three magnitude outputs (status lines) and both ripple and look-ahead carry functions. The magnitude outputs and their status indications are as follows:

2.7.1 Equal (EQ, See Figure 5)

The results of the resident ALU operation are compared at the sum-bus for all bits high during subtract and left-shift arithmetic operations, or for all bits low during other operations.

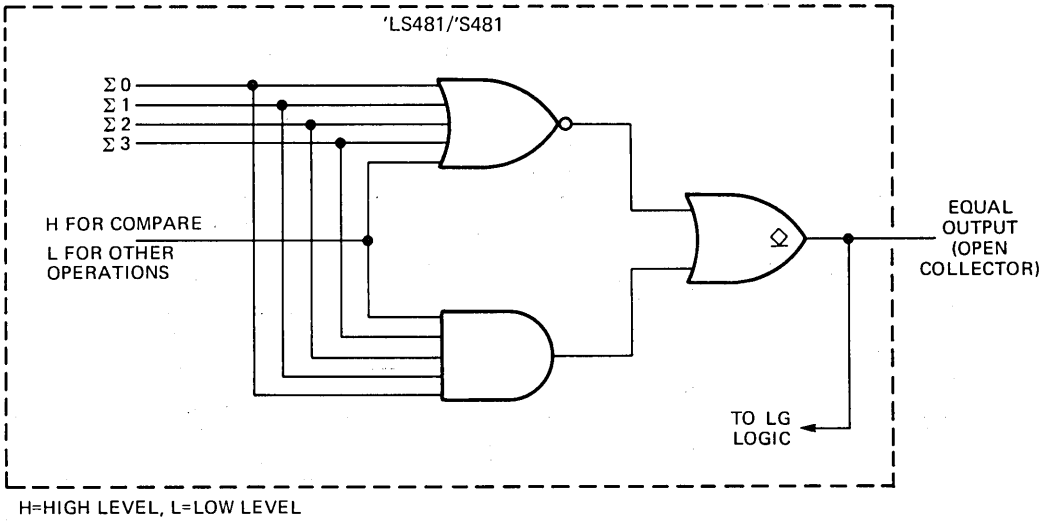


FIGURE 5 – EQUAL OUTPUT

2.7.2 Logically-Greater Than (LG, See Figure 6)

In the most-significant package (MSP) the X look-ahead function from the ALU is inhibited and the logically-greater-than (LG) output is enabled. See Figure 6. The MSP LG output is active during arithmetic and shift operation forms to provide a status indication that can be used when it is desirable to compare two unsigned integer numbers. The specific status for each operation form is listed in Table 7.

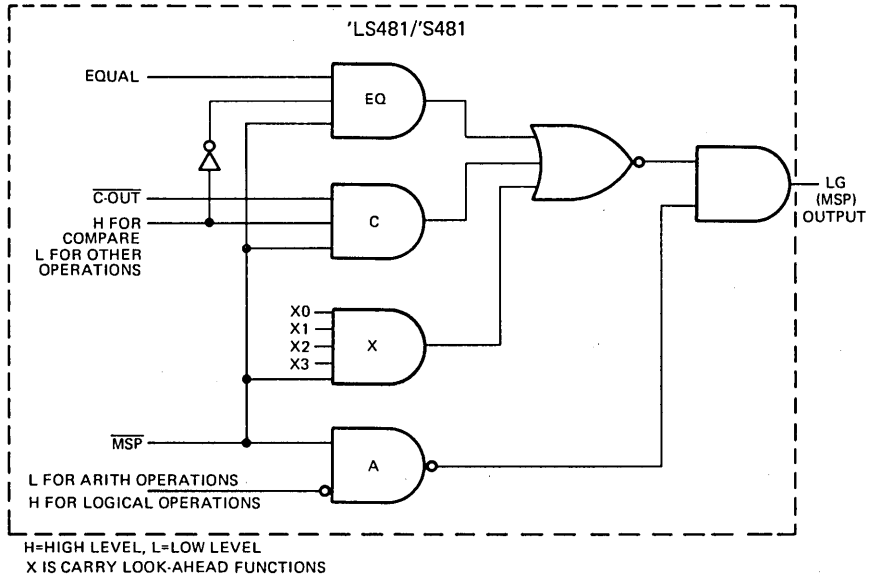


FIGURE 6 – MSP LOGICALLY-GREATER-THAN (LG) OUTPUT

TABLE 7
MSP LOGICALLY-GREATER-THAN (LG) OUTPUT

OP FORM	TYPE OF OP	LG = H INDICATES
I or II (ARITH)	ALL	Σ-BUS ≠ ZERO (EQ = L)
III (ARITH WITH SHIFT)	LSL, RSL	Σ-BUS ≠ ZERO (EQ = L)
	LSA or RSA	ADDER C-OUT
IV, V, or VI (SHIFTS)	ALL	AI ≠ ZERO (EQ = L)
VII (COMPARE)	A : B	A IS LG THAN B
	B : A	B IS LG THAN A
VIII (LOGICAL)	ALL	Σ-BUS ≠ ZERO (EQ = L)
IX (NO OP)	ZERO Σ-BUS	LG = L (EQ = H)
X THRU XIV	HARDWIRED ALGORITHMS	SEE OPERATION FORM DESCRIPTION

2.7.3 Arithmetically-Greater Than (AG, See Figure 7)

In the most-significant package (MSP) the Y look-ahead function from the ALU is inhibited and the arithmetically-greater-than (AG) output is enabled. The MSP AG output is active during arithmetic and shift operation forms to provide a status indication that can be used when it is desirable to compare two signed integer numbers. The specific status for each operation form is listed in Table 8.

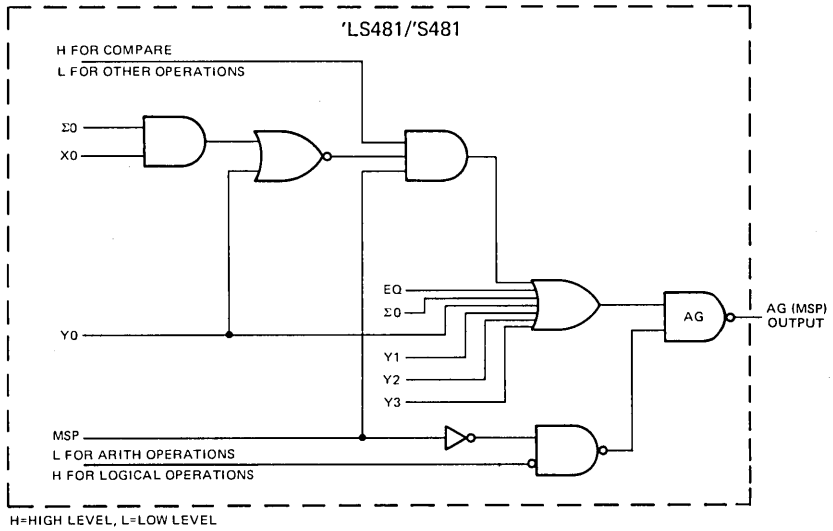


FIGURE 7 – MSP ARITHMETICALLY-GREATER-THAN (AG) OUTPUT

TABLE 8
ALU CARRY AND MSP ARITHMETICALLY-GREATER-THAN (AG) OUTPUTS

OPERATION FORM	LSP AND IP				MSP			
	X	Y	EQ	$\overline{C\text{-}OUT}$	LG	AG	EQ	$\overline{C\text{-}OUT}$
LOGICAL OPERATIONS	L	H	Σ-BUS = 0	$\overline{C\text{-}IN}$	Σ-BUS ≠ 0	Σ-BUS > 0	Σ-BUS = 0	$\overline{C\text{-}IN}$
ARITHMETIC OPERATIONS:								
COMPARE	X	Y	A=B	$\overline{C\text{-}OUT}$	A LG B or B LG A	A AG B or B AG A	A = B	$\overline{C\text{-}OUT}$
ALL OTHER ARITHMETIC	X	Y	Σ-BUS = 0	$\overline{C\text{-}OUT}$	Σ-BUS ≠ 0	Σ-BUS AG 0	Σ-BUS AG 0	$\overline{C\text{-}OUT}$

X and Y are carry look-ahead functions.

2.8 OPERAND OVERFLOW

In the most-significant package (MSP) the counter-carry output ($\overline{CCO}$) function from the program/memory counter is inhibited and the overflow (OV) output is enabled. The MSP OV output is active during arithmetic and shift operation forms to provide a status indication that the result of the operation cannot be correctly represented with the number of bit positions available. When the OV output goes high, it indicates that the next clock will:

a. During arithmetic operations, cause the ALU to overflow.
b. During left-shift arithmetic operations, cause the shifted register to overflow.

Table 9 enumerates the specific indicators generated.

TABLE 9
MSP OVERFLOW (OV) OUTPUT

OP FORM	TYPE OF OP	OV = H INDICATES
I or II (ARITH)	ADD or SUB	ALU OVERFLOW
III (ARITH WITH SHIFT)	LSL, RSL	ALU OVERFLOW
	RSA	OV = L
	LSA	NEXT CLOCK WILL CAUSE SHIFT OVERFLOW
IV, V, or VI (SHIFTS)	LSA	NEXT CLOCK WILL CAUSE SHIFT OVERFLOW
	ALL OTHERS	OV ≡ L
VII (COMPARE)	A : B	UNDEFINED
	B : A	UNDEFINED
VIII (LOGICAL)	ALL	OV ≡ L
IX (NO OP)	ZERO Σ-BUS	OV ≡ L
X THRU XIV	HARDWIRED ALGORITHMS	SEE OPERATION FORM DESCRIPTIONS

H = high level, L = low level

2.9 SUM' BUS MULTIPLEXER

The sum'-bus multiplexer, sourced by the ALU, provides a means for accomplishing a shift operation on the ALU operand without affecting the contents of WR, XWR, PC or MC (See Figure 8). Functionally, this multiplexer can be used to:

a. Shift the operand left or right (one bit position) arithmetic, logical, or circulate
b. Pass the operand without shift to the Σ' bus.

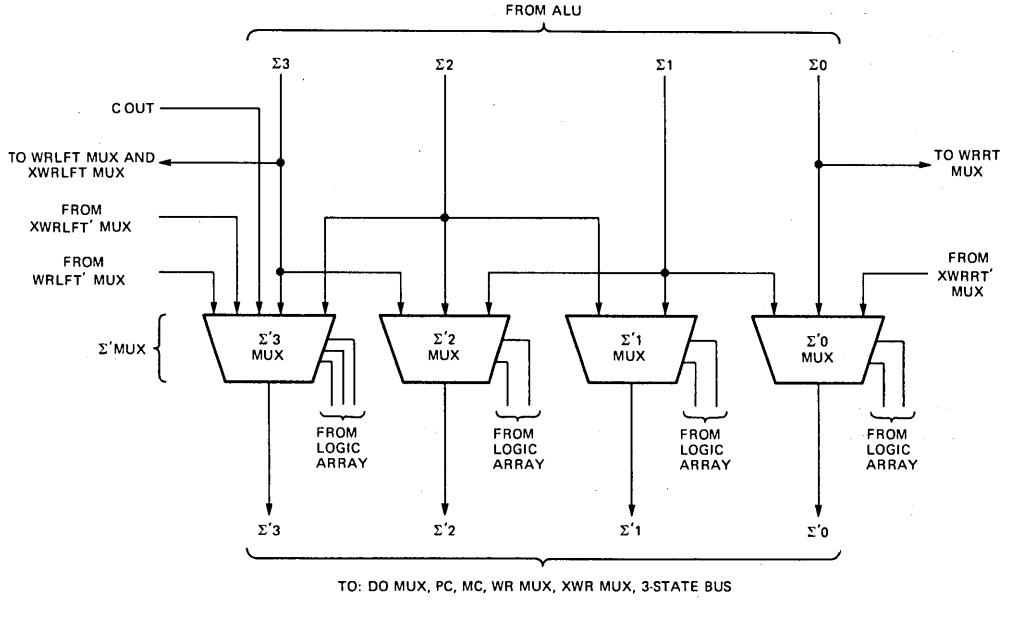


FIGURE 8 – SUM BUS MULTIPLEXER

Full sign protection and fill-in is provided in the MSP and LSP under control of the relative position inputs.

Information on the Σ' bus can be accessed during some operations through the 3-state Σ' bus control buffer at the B input/output port.

The parallel data input ports and the I/O capability of the B port, combined with the Σ-bus access, provides considerable flexibility for performing simple shifts or combinations of operation-and-shift on data or operands resident in the external working memory locations.

2.10 B-INPUT/OUTPUT CONTROL

The B-input/output port is isolated from the sum' bus by a 3-state control buffer when the buffer outputs are at a high-impedance. Enabling the buffer routes the sum' bus data to the B-port. The low-current inputs of the B port latch minimizes loading effects, and the buffers can source 6.5 mA or sink 10 mA of drive current in the output mode. During the output mode, the 'bus data can be latched in the B input latch. Enabling or disabling is accomplished by the I/O control input. See Table 10 and Figure 9.

TABLE 10
B-INPUT/OUTPUT CONTROL

I/O CONTROL	I/O BUFFER OUTPUT
L	SUM' BUS DATA
H	HIGH-IMPEDANCE

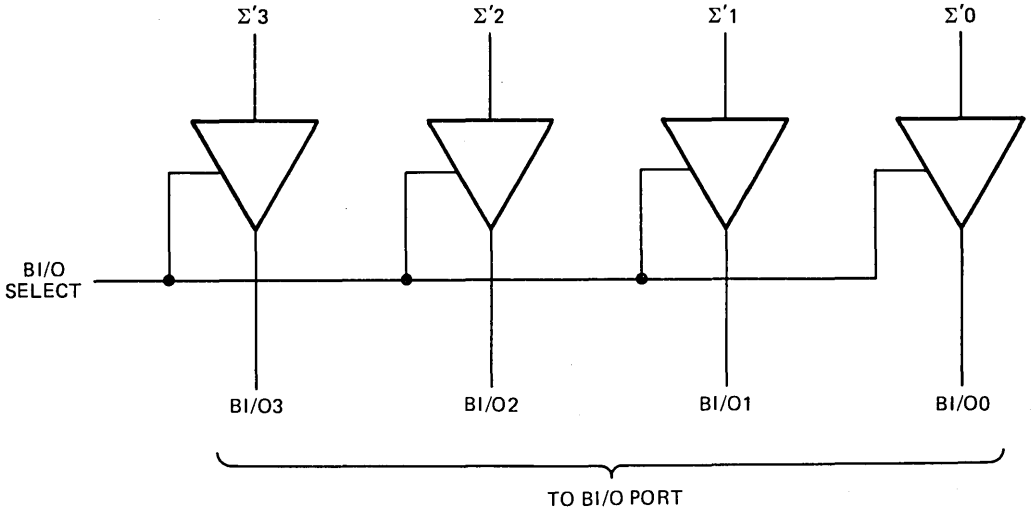


FIGURE 9 – B-INPUT/OUTPUT CONTROL

2.11 WORKING REGISTER

The working register (WR) is a 4-bit D-type register which functions as an accumulator during iterative arithmetic operations or as a temporary holding register for intermediate operands (see Figure 10). It is sourced by the WR multiplexer. Storage of setup data, under control of the resident operation forms which permit the WR to be a destination, occurs on the positive transition of the clock. WR shifting capabilities are implemented in the WR multiplexer. The working register can be selected to source the data-out port multiplexer (DO MUX), A-input multiplexer (A MUX), or B-input multiplexer (B MUX). The MSB of the WR is sourced to the WRLFT MUX, and the LSB of the WR is sourced to the WRRT MUX to facilitate expansion.

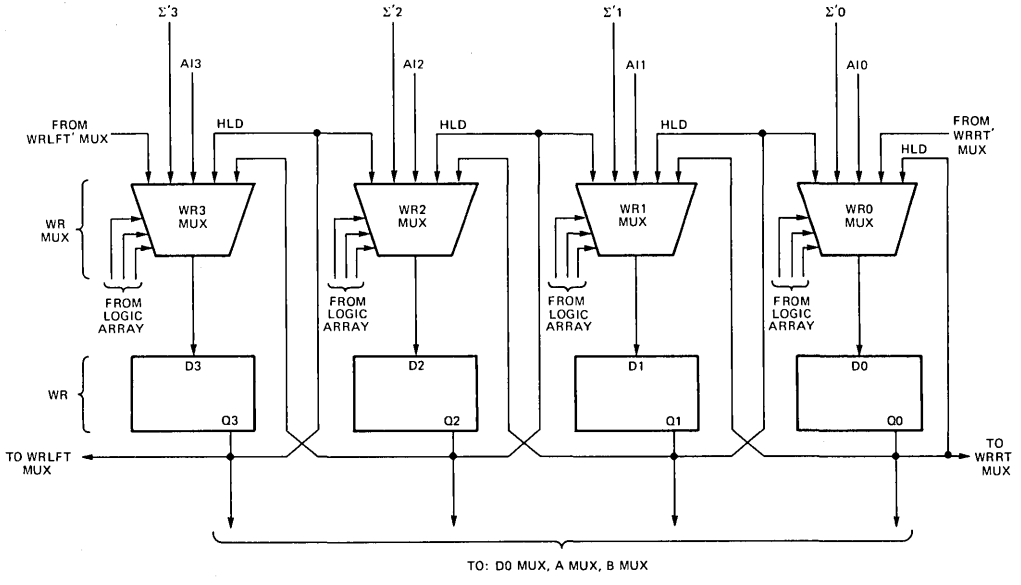


FIGURE 10 – WORKING REGISTER (WR) AND WR MULTIPLEXER

An asynchronous control line, $\overline{\text{LDWR}}$, is available to facilitate loading the working register directly from the A input port in combination with the resident micro-operation.

2.12 WORKING REGISTER MULTIPLEXER (WR MUX)

The working register multiplexer provides source selection, including the bidirectional shifting capability, for the working register. See Figure 10. Under direction of the resident operation, the WR MUX asynchronously selects either:

a. A input port for direct loading
b. Σ' bus for ALU operand results

c. Hold mode for no change
d. Shift left
e. Shift right

End conditions for both shift left and shift right operations are routed to or from WR MSB (WR3) or WRLSB (WR0) to the WRLFT/WRLFT' multiplexers or to the WRRT/WRRT' multiplexers respectively.

2.13 EXTENDED WORKING REGISTER

The extended working register (XWR) is a 4-bit D-type register which functions primarily as an extension of the working register to provide the double-precision operation capabilities needed for iterative multiply and divide routines (see Figure 11). Additionally, the storage capabilities of the XWR are available for use as another temporary holding register for intermediate operands during a number of the single-precision operation forms. It is sourced by the XWR multiplexer. Storage of setup data, under control of resident operation forms which permit the XWR to be a destination, occurs on the positive transition of the clock. XWR shifting capabilities are implemented in the XWR multiplexer. The XWR can be selected to source the data-out port multiplexer (DO MUX), B-input multiplexer (B MUX), or the XWR multiplexer (XWR MUX). The MSB of the XWR is sourced to the XWRLFT' MUX, and the LSB of the XWR is sourced to the XWRRT' MUX to facilitate expansion.

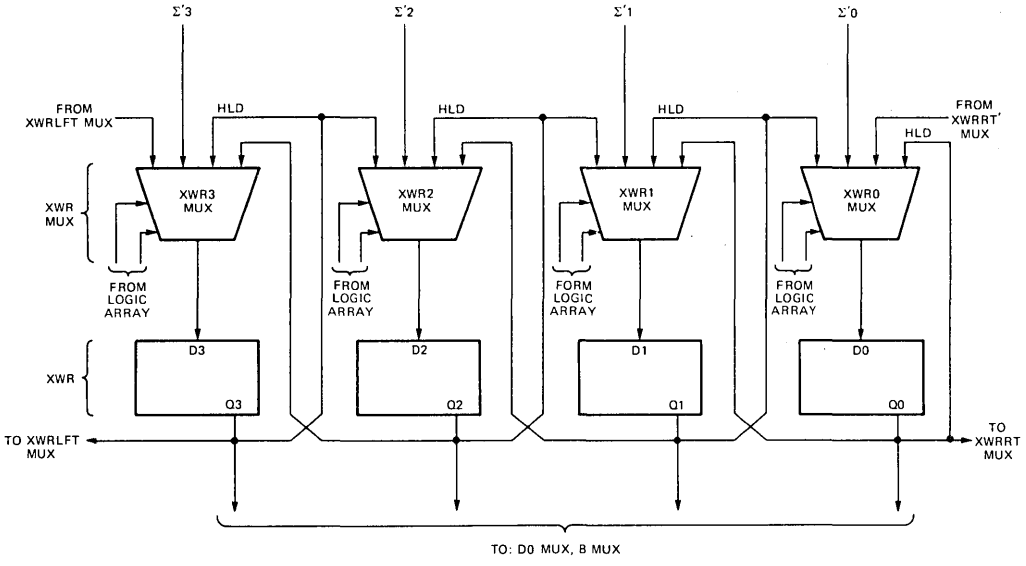


FIGURE 11 – EXTENDED WORKING REGISTER (XWR) AND XWR MULTIPLEXER

2.14 EXTENDED WORKING REGISTER MULTIPLEXER (XWR MUX)

The extended working register multiplexer provides source selection, including the bidirectional shifting capability, for the extended working register (see Figure 11). Under direction of the resident operation, the XWR MUX asynchronously selects either:

a. Σ' bus for ALU operand results
b. Hold mode for no change

c. Shift left
d. Shift right.

End conditions for both shift left and shift right operations are routed to or from XWR MSB (XWR3) or XWR LSB (XWR0) to the XWRLFT/XWRLFT' multiplexers or to the XWRRT/XWRRT' multiplexers respectively.

2.14.1 Σ-Bus, WR, XWR MSB Shift Transfer Multiplexers

The MSB shift transfers are accomplished by the WRLFT, XWRLFT input/output multiplexers and the WRLFT', XWRLFT' sum-bus/register MSB input multiplexers. All four multiplexers, and the impedance of the 3-state I/O lines of the WRLFT and XWRLFT multiplexer outputs are under control of the resident operation code and the relative position control (POS). Data paths of the multiplexers are illustrated in Figure 12, and bit transfers with respect to each of the shift operations are enumerated in Tables 11 through 14.

2.14.2 WRLFT, XWRLFT Multiplexers

The WRLFT, XWRLFT input/output multiplexers facilitate routing of the working register, extended working register, or sum bus MSB out the WRLFT, XWRLFT I/O's during output modes. In an input mode, the three-state output is at a high impedance permitting the WRLFT and/or the XWRLFT pins to be used as inputs.

2.14.3 WRLFT', XWRLFT' Multiplexers

The WRLFT' multiplexer selects the source for either the sum bus or working register MSB. Sign bit protection and right-shift bit-fill functions are all handled on-chip by these multiplexers under control of the operation code and relative position. The WRLFT' sources are:

a. WRLFT (input)
b. ALU carry out (for sign-fill)
c. Low level (for zero-fill)
d. XWRLFT input
e. XWR MSB
f. WR MSB (sign-fill in for RSA)
g. Sign fill in for RSA (see Figure 12)

The XWRLFT multiplexer selects the source for XWR MSB and provides sign-bit protection and right-shift-fill functions for the XWR. The XWRLFT sources are:

a. XWRLFT (input)
b. WRLFT
c. XWR MSB (sign-fill in for RSA)

2.14.4 WR, XWR LSB Shift Transfer Multiplexers

The LSB shift transfers are accomplished by the WRRT, XWRRT input/output multiplexers and the WRRT', XWRRT' sum-bus/register LSB input multiplexers. All four multiplexers, and the impedance of the 3-state I/O lines of the WRRT and XWRRT multiplexer outputs, are under control of the resident operation code and the relative position control (POS). Data paths of the multiplexers are illustrated in Figure 13.

2.14.5 WRRT Multiplexer, XWRRT Buffer

The WRRT input/output multiplexer facilitates routing of sum-bus or working register LSB out the WRRT I/O during output modes. The XWRRT I/O buffer can access and source the XWR LSB. In an input mode, the three-state output is at a high impedance permitting the WRRT and/or XWRRT pins to be used as inputs.

2.14.6 WRRT', XWRRT' Multiplexers

The WRRT' multiplexer selects either the WRRT input or a low logic level (fill) input as the LSB source for either the working register or the sum-bus. The XWRRT' multiplexer selects between the XWRRT input and low logic level (fill) input as the XWR LSB source.

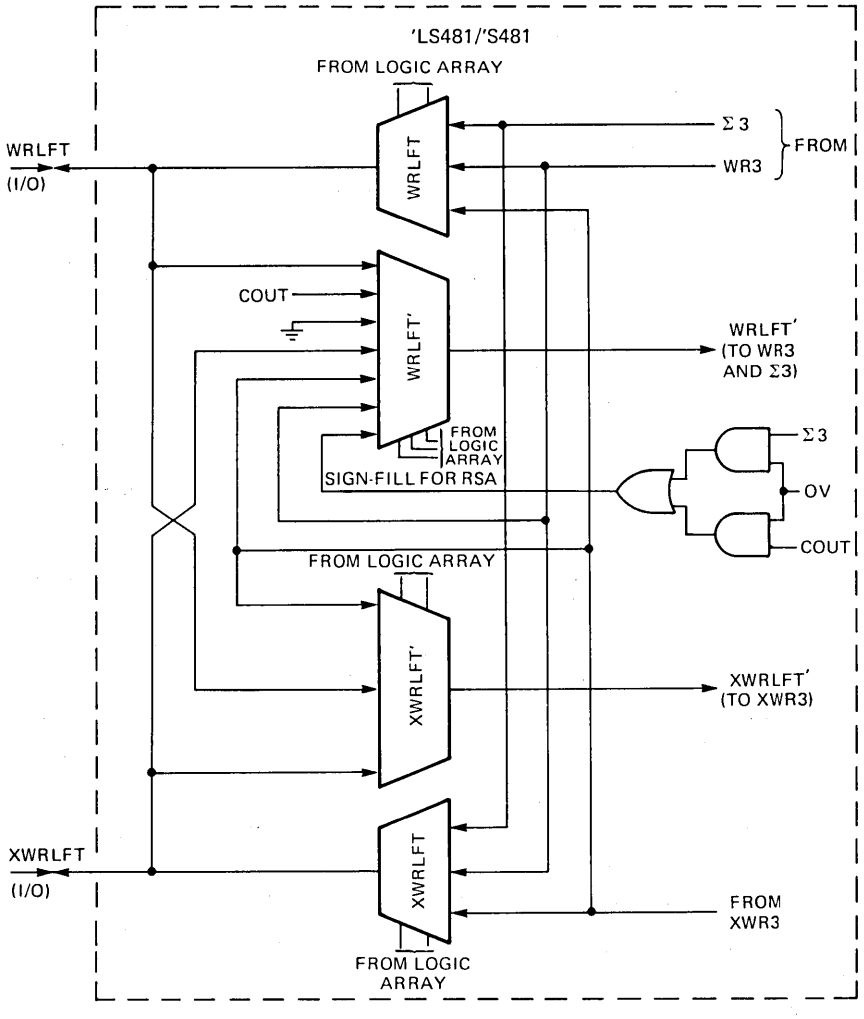


FIGURE 12 – SUM-BUS, WR, XWR MSB SHIFT TRANSFER MULTIPLEXERS

TABLE 11
WORKING REGISTER BIT TRANSFERS TO WRLFT/WRRT

SHIFT MODE	MOST-SIGNIFICANT POSITION				INTERMEDIATE POSITION				LEAST-SIGNIFICANT POSITION			
	WRLFT	WRLFT'	WRRT'	WRRT	WRLFT	WRLFT'	WRRT'	WRRT	WRLFT	WRLFT'	WRRT'	WRRT
LSL (SP)	Z	X	WRRT	Z	WR3	X	WRRT	Z	WR3	X	WRRT	Z
LSL (DP)	XWR3	X	WRRT	Z	WR3	X	WRRT	Z	WR3	X	WRRT	Z
LSA (SP)	WR3	X	WRRT	Z	WR3	X	WRRT	Z	WR3	X	L	Z
LSA (DP)	XWR3	X	WRRT	Z	WR3	X	WRRT	Z	WR3	X	WRRT	Z
LCIR (SP)	WR3	X	WRRT	Z	WR3	X	WRRT	Z	WR3	X	WRRT	Z
LCIR (DP)	XWR3	X	WRRT	Z	WR3	X	WRRT	Z	WR3	X	WRRT	Z
RSL (SP)	Z	WRLFT	X	WR0	Z	WRLFT	X	WR0	Z	WRLFT	X	Z
RSL (DP)	Z	L	X	WR0	Z	WRLFT	X	WR0	Z	WRLFT	X	WR0
RSA (SP)	Z	WR3	X	WR0	Z	WRLFT	X	WR0	Z	WRLFT	X	WR0
RSA (DP)	Z	WR3	X	WR0	Z	WRLFT	X	WR0	Z	WRLFT	X	WR0
RCIR (SP)	Z	WRLFT	X	WR0	Z	WRLFT	X	WR0	Z	WRLFT	X	WR0
RCIR (DP)	Z	WRLFT	X	WR0	Z	WRLFT	X	WR0	Z	WRLFT	X	WR0

TABLE 12
SUM-BUS BIT TRANSFERS TO WRLFT/WRRT

SHIFT MODE	MOST-SIGNIFICANT POSITION				INTERMEDIATE POSITION				LEAST-SIGNIFICANT POSITION			
	WRLFT	WRLFT'	WRRT'	WRRT	WRLFT	WRLFT'	WRRT'	WRRT	WRLFT	WRLFT'	WRRT'	WRRT
LSL (SP)	Z	X	WRRT	Z	Σ3	X	WRRT	Z	Σ3	X	WRRT	Z
LSL (DP)	XWR3	X	WRRT	Z	Σ3	X	WRRT	Z	Σ3	X	WRRT	Z
LSA (SP)	Σ3	X	WRRT	Z	Σ3	X	WRRT	Z	Σ3	X	L	Z
LSA (DP)	XWR3	X	WRRT	Z	Σ3	X	WRRT	Z	Σ3	X	WRRT	Z
LCIR (SP)	Σ3	X	WRRT	Z	Σ3	X	WRRT	Z	Σ3	X	WRRT	Z
LCIR (DP)	XWR3	X	WRRT	Z	Σ3	X	WRRT	Z	Σ3	X	WRRT	Z
RSL (SP)	Z	WRLFT	X	Σ0	Z	WRLFT	X	Σ0	Z	WRLFT	X	Σ0
RSL (DP)	Z	C-OUT	X	Σ0	Z	WRLFT	X	Σ0	Z	WRLFT	X	Σ0
RSA (SP)	Z	*	X	Σ0	Z	WRLFT	X	Σ0	Z	WRLFT	X	Σ0
RSA (DP)	Z	*	X	Σ0	Z	WRLFT	X	Σ0	Z	WRLFT	X	Σ0
RCIR (SP)	Z	WRLFT	X	Σ0	Z	WRLFT	X	Σ0	Z	WRLFT	X	Σ0
RCIR (DP)	Z	XWRLFT	X	Σ0	Z	WRLFT	X	Σ0	Z	WRLFT	X	Σ0

*VARIABLE = (Σ3 • ALU OVERFLOW) + (C-OUT • ALU OVERFLOW)

TABLE 13
EXTENDED WORKING REGISTER BIT TRANSFERS TO XWRLFT/XWRRT

SHIFT MODE	MOST-SIGNIFICANT POSITION				INTERMEDIATE POSITION				LEAST-SIGNIFICANT POSITION			
	XWRLFT	XWRLFT'	XWRRT'	XWRRT	XWRLFT	XWRLFT'	XWRRT'	XWRRT	XWRLFT	XWRLFT'	XWRRT'	XWRRT
LSL (SP)	Z	X	XWRRT	Z	XWR3	X	XWRRT	Z	XWR3	X	XWRRT	Z
LSL (DP)	Z	X	XWRRT	Z	XWR3	X	XWRRT	Z	XWR3	X	XWRRT	Z
LSA (SP)	XWR3	X	XWRRT	Z	XWR3	X	XWRRT	Z	XWR3	X	L	Z
LSA (DP)	WR3	X	XWRRT	Z	XWR3	X	XWRRT	Z	XWR3	X	L	Z
LCIR (SP)	XWR3	X	XWRRT	Z	XWR3	X	XWRRT	Z	XWR3	X	XWRRT	Z
LCIR (DP)	WR3	X	XWRRT	Z	XWR3	X	XWRRT	Z	XWR3	X	XWRRT	Z
RSL (SP)	Z	XWRLFT	X	XWR0	Z	XWRLFT	X	XWR0	Z	XWRLFT	X	Z
RSL (DP)	Z	WRLFT	X	XWR0	Z	XWRLFT	X	XWR0	Z	XWRLFT	X	XWR0
RSA (SP)	Z	XWR3	X	XWR0	Z	XWRLFT	X	XWR0	Z	XWRLFT	X	XWR0
RSA (DP)	Z	WRLFT	X	XWR0	Z	XWRLFT	X	XWR0	Z	XWRLFT	X	XWR0
RCIR (SP)	Z	XWRLFT	X	XWR0	Z	XWRLFT	X	XWR0	Z	XWRLFT	X	XWR0
RCIR (DP)	Z	WRLFT	X	XWR0	Z	XWRLFT	X	XWR0	Z	XWRLFT	X	XWR0

TABLE 14
SUM-BUS BIT TRANSFERS TO XWRLFT (MSP)

SHIFT MODE	MOST-SIGNIFICANT POSITION XWRLFT	XWRLFT'	XWRRT'	XWRRT
LSL (SP)	Z	X	XWRRT	Z
LSL (DP)	Z	X	XWRRT	Z
LSA (SP)	XWR3	X	XWRRT	Z
LSA (DP)	Σ3	X	XWRRT	Z
LCIR (SP)	XWR3	X	XWRRT	Z
LCIR (DP)	Σ3	X	XWRRT	Z
RSL (SP)	Z	XWRLFT	X	XWR0
RSL (DP)	Z	WRLFT	X	XWR0
RSA (SP)	Z	XWR3	X	XWR0
RSA (DP)	Z	WRLFT	X	XWR0
RCIR (SP)	Z	XWRLFT	X	XWR0
RCIR (DP)	Z	WRLFT	X	XWR0

NOTE: Intermediate and Least-Significant Positions are the same as shown in Table 13.

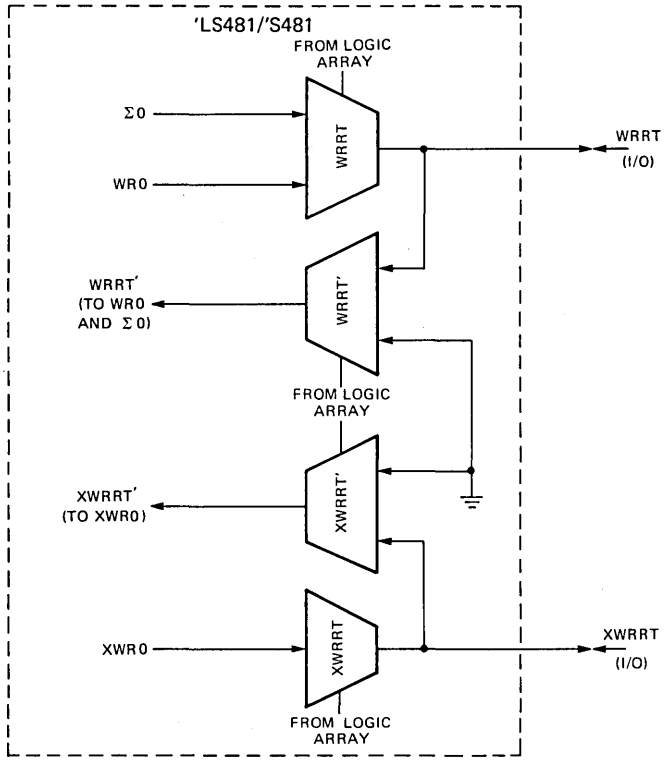


FIGURE 13 – SUM-BUS, WR, XWR LSB SHIFT TRANSFER MULTIPLEXERS

2.15 SHIFT FUNCTIONS

The 'LS481/'S481 contains the necessary controls and data paths to perform single or double length logical, arithmetic, or circulate bidirectional shift functions in a single clock cycle. Each of the six shift functions implemented are selectable by a single microinstruction; and, additionally two single clock operation forms are included which provide the capability of performing an add/subtract in conjunction with a shift. The six shift functions and the basic operation forms offering them are enumerated in Table 15.

TABLE 15
MICROPROGRAMMABLE SHIFT FUNCTIONS

FUNCTION	OPERATION FORMS			
	SIMPLE SHIFT		ADD/SUBTRACT WITH SHIFT	
	SINGLE LENGTH	DOUBLE LENGTH	SINGLE LENGTH	DOUBLE LENGTH
LEFT CIRCULATE (LCIR)	IV, V	VI		
LEFT SHIFT ARITHMETIC (LSA)	IV, V	VI	III	
LEFT SHIFT LOGICAL (LSL)	IV, V	VI	III	II
RIGHT CIRCULATE (RCIR)	IV, V	VI		
RIGHT SHIFT ARITHMETIC (RSA)	IV, V	VI	III	
RIGHT SHIFT LOGICAL (RSL)	IV, V	VI	III	II

2.15.1 CIRCULATE (SHIFT) FUNCTIONS (MICROPROGRAMMABLE)

Operation forms IV and V provide the system designer with the capability of programming a single precision circulate (or rotate) of the Σ' bus, working register, or extended working register and operation form VI provides the capability of circulating or rotating a double-length word resident in the WR/XWR. A single-bit-position left or right circulate is accomplished on each clock without the loss of any bits as the shift transfer multiplexers, under control of the resident operation and position input, interconnect the bus or register as illustrated in Figure 14.

The remaining end conditions are handled on chip by the shift transfer multiplexers to interconnect the bit transfer mechanisms for MSB → LSB for single precision circulates and for transfers to or from the Σ' bus or working register and the extended working register during double-precision circulates. Data flow between packages in an expanded word-length system is via the interconnected WRRT/WRLFT and XWRRT/XWRLFT terminals.

2.15.2 ARITHMETIC SHIFT FUNCTIONS (MICROPROGRAMMABLE)

Operation forms III, IV, V and VI provide the system designer with the capability of programming the following arithmetic shifts.

Form III – A single-precision arithmetic left or sign-protected right shift of the sum or difference of the A and B operands destined for either the WR or XWR.

Form IV – A single-precision arithmetic left or sign-protected right shift of the A operand destined for the Σ' bus.

Form V – A single-precision arithmetic left or sign-protected right shift of the WR or XWR contents.

Form VI – A double-precision arithmetic left or sign-protected right shift of the WR and XWR contents.

SN74LS481/SN74S481 4-BIT-SLICE SCHOTTKY PROCESSOR ELEMENT

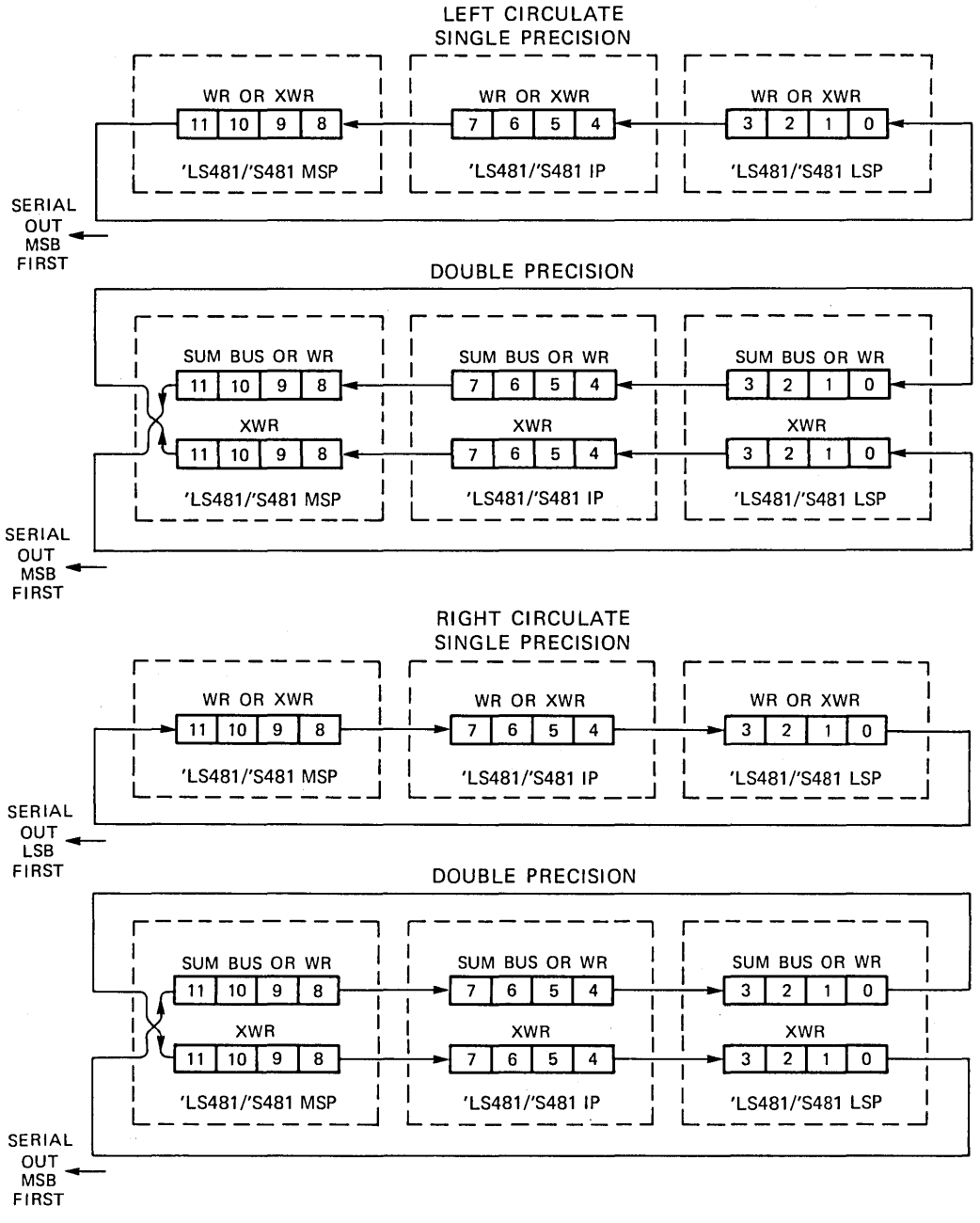


FIGURE 14 – CIRCULATE FUNCTIONS

A single-bit-position shift is accomplished on each clock with right-shift sign-protection and left shift LSB zero-fill operations controlled by the shift transfer multiplexers under direction of the resident operation and the position input. See Figure 15.

The remaining end conditions are handled on chip by the shift transfer multiplexers to interconnect the bit transfer mechanisms for transfers to or from the Σ' bus or working register and the extended working register during double-precision arithmetic shifts. Data flow between packages in an expanded word-length system is via the interconnected WRRT/WRLFT and XWRRT/XWRLFT terminals.

2.15.3 LOGICAL SHIFT FUNCTIONS (MICROPROGRAMMABLE)

Operation Forms II, III, IV, V and VI provide the system designer with the capability of programming the following logical shifts:

Form II – A double-precision left or right shift of the sum or difference of the A and B operands destined for the WR in conjunction with the XWR.

Form III – A single-precision left or right logical shift of the sum or difference of the A and B operands destined for the WR or the XWR.

Form IV – A single-precision left or right logical shift of the A operand destined for the Σ' bus.

Form V – A single-precision left or right logical shift of the WR or XWR contents.

Form VI – A double-precision left or right logical shift of the WR and XWR contents.

A single-bit-position shift is accomplished on each clock with MSB and LSB fill operations controlled by the shift transfer multiplexers under direction of the resident operation and the position input. See Figure 16.

The remaining end conditions are handled on chip by the shift transfer multiplexers to interconnect the bit transfer mechanisms for transfers to and from the Σ' bus or working register and the extended working register during double-precision logical shifts. Data flow between packages in an expanded word length system is via the interconnected WRRT/WRLFT and XWRRT/XWRLFT terminals.

2.16 DATA-OUT PORT MULTIPLEXER (DO MUX)

The data-out port multiplexer, Figure 17, provides selection for routing the contents of either the sum'-bus, working register, or extended working register to the parallel output port. Additionally, the multiplexer is equipped with 3-state outputs providing the capability to isolate the 'LS481/'S481 from the system data bus. Source selections and high-impedance controls are detailed in Table 16.

Each data output is capable of sourcing 6.5 and sinking 10 milliamperes of drive current.

2.17 MEMORY AND PROGRAM COUNTERS

Dual counters provide the system designer with a processor element containing both an iteration counter and the capability of generating and/or storing locations of operands/data.

Either counter can be loaded or preset to any value or result from the sum bus in operations forms as follows:

	SELECTABLE AS DESTINATION	
OP FORM	PC	MC
I	Yes	Yes
III	No	Yes
VIII	Yes	No

SN74LS481/SN74S481 4-BIT-SLICE SCHOTTKY PROCESSOR ELEMENT

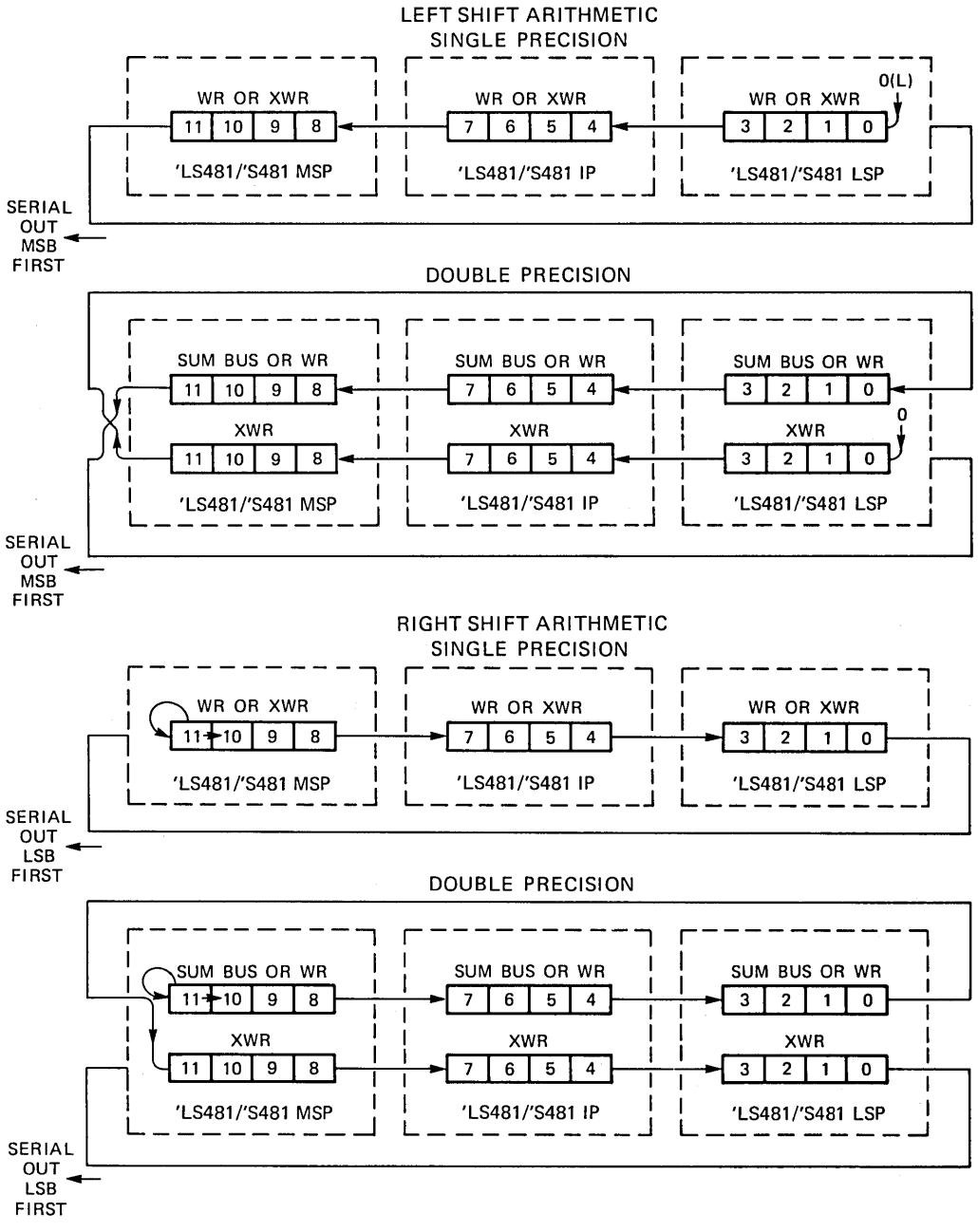


FIGURE 15 – ARITHMETIC SHIFT FUNCTIONS

SN74LS481/SN74S481 4-BIT-SLICE SCHOTTKY PROCESSOR ELEMENT

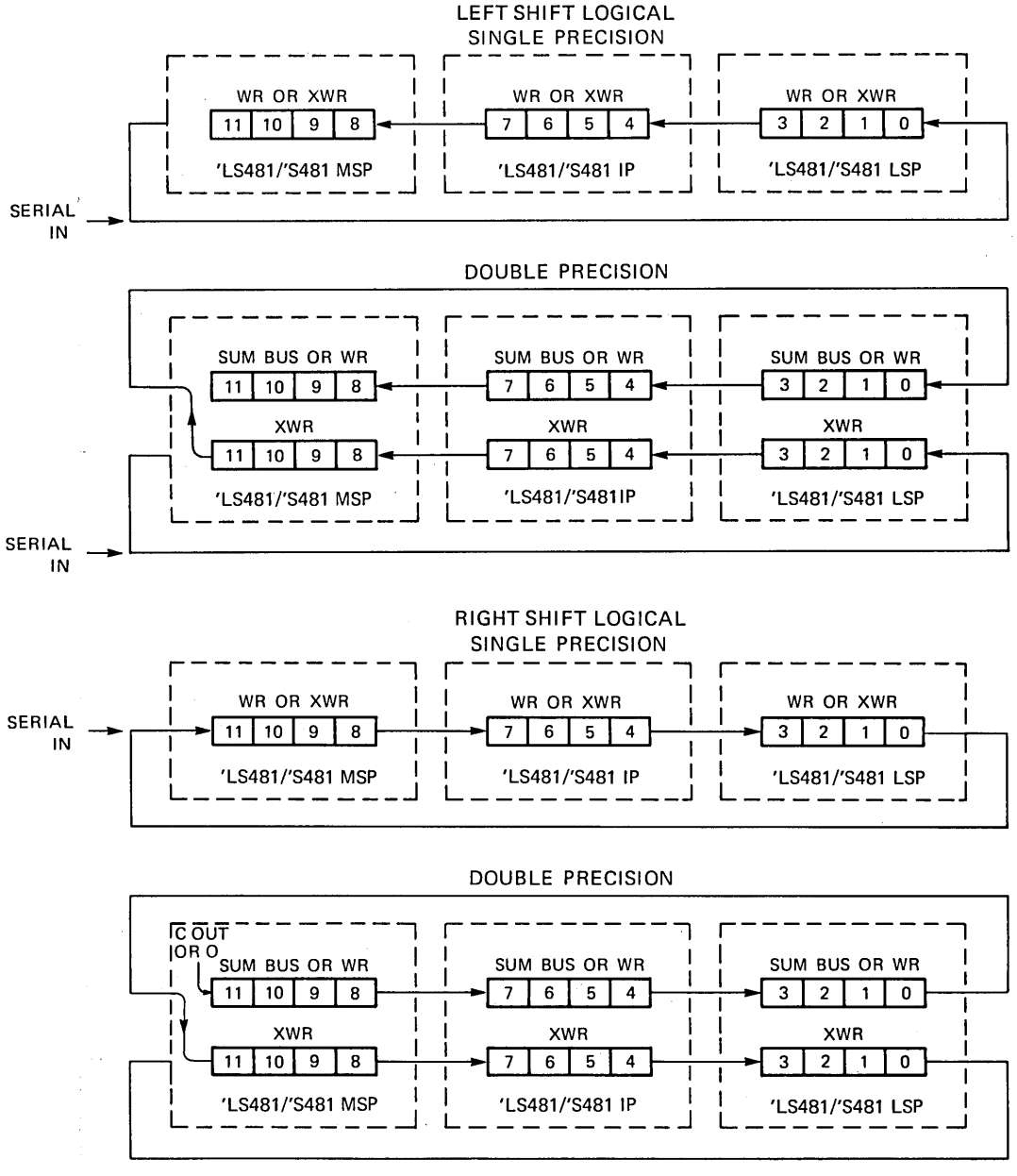


FIGURE 16 – LOGICAL SHIFT FUNCTIONS

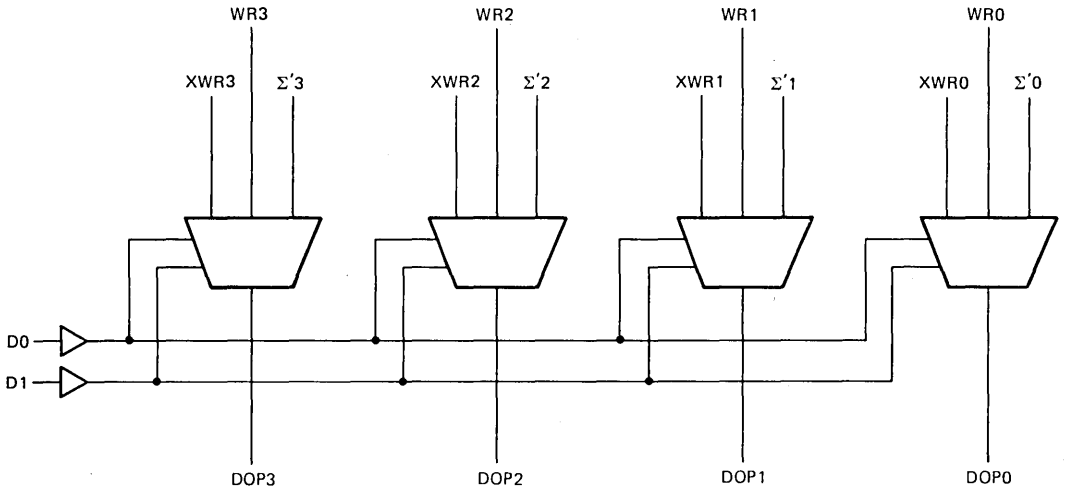


FIGURE 17 – DATA-OUT PORT MULTIPLEXER (DO MUX)

Under control of the position (POS) input and the resident operation code, the $\overline{CCO}$/OV output facilitates cascading the program and memory counters. In the least-significant and intermediate positions, the $\overline{CCO}$ pins of lesser significant packages are connected to the $\overline{CCI}$ pins of more significant packages to complete the counter interconnections to the bit-size of the processor element.

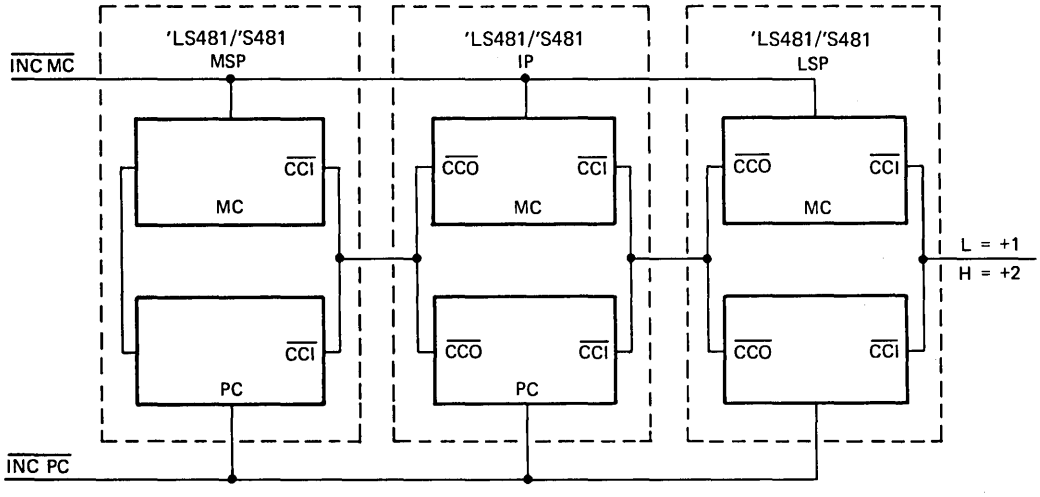
TABLE 16
DATA-OUT PORT CONTROL

CONTROL INPUTS		SOURCE OR FUNCTION
D1	D0	
L	L	Σ'-BUS
L	H	EXTENDED WORKING REGISTER
H	L	WORKING REGISTER
H	H	HIGH-IMPEDANCE

The functionally identical program and memory counters, sharing a common counter carry input ($\overline{CCI}$) control pin and a common counter carry output ($\overline{CCO}$) pin, feature individual control lines ($\overline{INC\ PC}$, $\overline{INC\ MC}$) which can be used to instruct either (but normally not both) or neither counter to increment on the next clock transition in any of the 14 operation forms. Additionally, the counter in the LSP, under command of the POS input, has the capability of incrementing its value by one or by two to facilitate the generation of even or odd address locations in a single clock cycle. Contents of the counters can be read out from the address out port asynchronously under control of the address output multiplexer (AO MUX) select input.

Typical counter functions with respect to package relative positions are shown in Figure 18.

In the MSP, the $\overline{CCO}$/OV output, as a result of the position (POS) control, becomes the ALU/shift overflow (OV) status output.



INPUTS			CK	COUNTER VALUE			
INC PC	INC MC	CCI		LSP MC	LSP PC	MSP, IP MC	MSP, IP PC
H	H	X	↑	NO CHG	NO CHG	NO CHG	NO CHG
L	H	L	↑	NO CHG	+1	NO CHG	+1
L	H	H	↑	NO CHG	+2	NO CHG	NO CHG
H	L	L	↑	+1	NO CHG	+1	NO CHG
H	L	H	↑	+2	NO CHG	NO CHG	NO CHG
X	X	X	L	NO CHG	NO CHG	NO CHG	NO CHG
X	X	X	H	NO CHG	NO CHG	NO CHG	NO CHG

H=HIGH LEVEL, L=LOW LEVEL, X=IRRELEVANT, ↑=LOW-TO-HIGH TRANSITION

FIGURE 18 – PROGRAM AND MEMORY COUNTER FUNCTIONS

2.18 ADDRESS-OUT PORT MULTIPLEXER (AO MUX)

The address-out port multiplexer, Figure 19, provides for direct parallel access to the contents of either the program or memory counter contents. A single line controls selection as shown in Table 17.

TABLE 17
ADDRESS-OUT PORT CONTROL

CONTROL INPUT A0	COUNTER SELECTED
L	MEMORY
H	PROGRAM

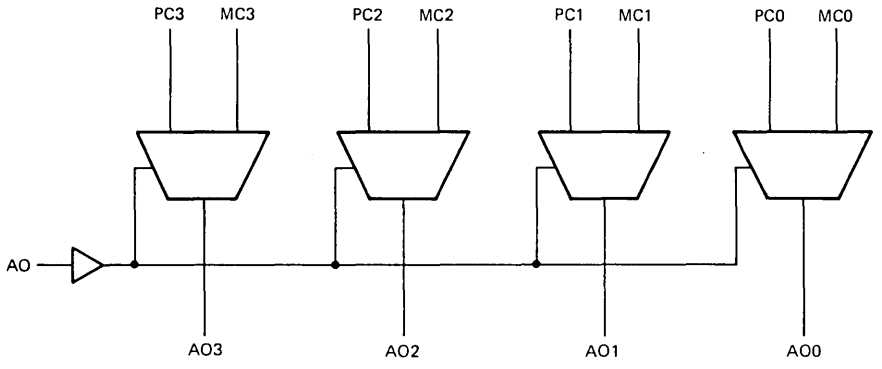


FIGURE 19 – ADDRESS-OUT PORT MULTIPLEXER (AO MUX)

3

2.19 EXPANDING THE WORD LENGTH

The 'LS481/'S481 processor element contains on-chip personality circuitry designed specifically to minimize the external discrete components required to cascade 4-bit slices to form larger work lengths. At the processor-element level, three external resistors are all that is required: one to pull-up the open-collector outputs and two to establish the position control input voltage at the LSP. Figure 20 shows a typical 16-bit processor element and illustrates the parallel bus arrangements for I/O and control with an SN74S182 performing ALU look-ahead across the 16-bit word. Interconnectivity for the shift, arithmetic, and counter functions is accomplished by hardwiring the functions as shown.

At the system level, standard techniques commonly employed for power-supply bypass, termination of unused pins, and system grounding of high-performance Schottky TTL systems are recommended.

3. OPERATIONAL DESCRIPTIONS

3.1 MICRO/MACRO-OPERATIONS

The micro/macro-operations resident in the micro-decode logic array can be accessed with an eleven-bit operation-select word. Operational flexibility is maximized by the fact that the op-select word format has been defined individually for each of the 14 different operation forms.

Operation Forms I, II, and III are primarily ALU functions. Forms II and III combine logical or arithmetic shifting functions with the ALU result. Form II can be used for double-precision shifting. Sources, specific ALU function, shift format, and destinations are detailed for each op-select word format.

Forms IV, V, and VI perform either logical or arithmetic, bidirectional shifting of the single- and double-precision buses and registers.

Form VII can be used to compare the magnitude of A source to B source, or B source to A source.

Form VIII provides the capability to logically combine the values of the A and B sources.

Form IX zeros the Σ' bus with the effect of providing no operation.

Forms X through XIV are macroprogrammable operations which provide:

a. CRC partial sum update (normally $\frac{N}{2}$ clocks)
b. Signed Divide (N + 3 clocks)
c. Unsigned Divide (N + 1 clocks)
d. N-bit-by-N-bit double-precision unsigned multiply (N clocks)
e. N-bit-by-N-bit double-precision signed multiply (N clocks)

The 14 operation forms, symbols, and number of unique operations are detailed in Table 18.

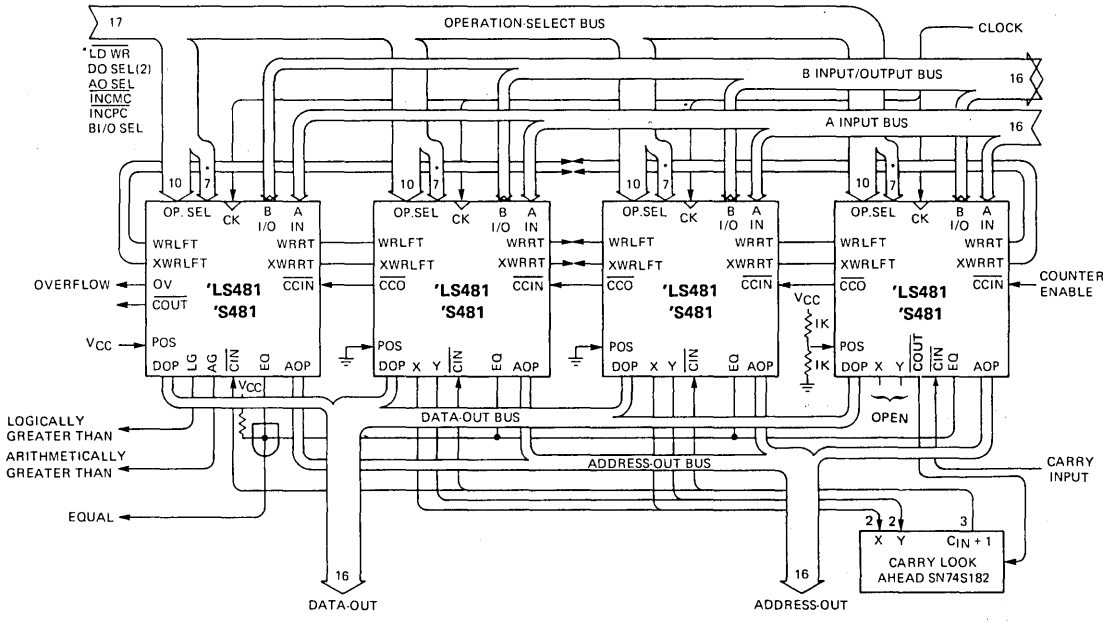


FIGURE 20—TYPICAL 16-BIT PROCESSOR

TABLE 18 – OPERATION FORM, COMMAND FORMAT, AND TEST OUTPUTS

OPERATION FORM		COMMAND FORMAT											TEST OUTPUTS							
													MSP		ALL		MSP		MSP	MSP
NO.	OPERATION	OP0 (7)[1]	OP1 (8)	OP2 (9)	OP3 (10)	OP4 (17)	OP5 (14)	OP6 (13)	OP7 (11)	OP8 (15)	OP9 (16)	LSP $\overline{CIN}$ (18)	LG (21)	AG (20)	EQ (23)	$\overline{C\text{-}OUT}$ (22)	X (21)	Y (20)	OVFL (37)	$\overline{CCO}$ (37)
IA	(±A ±B + $\overline{CIN}$) → Σ′ BUS ONLY[2]	H	L	L	A SOURCE		B SOURCE			A′ FNCT	B′ FNCT	L = CARRY H = NO CARRY	Σ′≠ZERO	Σ′>ZERO	Σ′=ZERO	$\overline{C\text{-}OUT}$	X[4]	Y[4]	OVFL	$\overline{CCO}$
IB	(±A ±B + $\overline{CIN}$) → REGISTER	L	REGISTER		LL = AI → A LH = H′S → A HL = BI → A HH = WR → A		LLL = BI → B LLH = H′S → B LHL = BI · WR → B LHH = WR → B HLL = BI · XWR → B HLH = XWR → B HHL = BI · PC → B HHH = PC → B			L = A → A′ H = $\overline{A}$ → A′	L = B → B′ H = $\overline{B}$ → B′									
			LL = Σ′ → WR LH = Σ′ → XWR HL = Σ′ → PC HH = Σ′ → MC																	
IIA	(A + B + $\overline{CIN}$) ↠ WR, XWR[2]	H	H	H	L	H	L	FUNCT L = A → A′ H = $\overline{A}$ → A′	B′ SRC L = BI → B′ H = WR → B′	A′ SRC L = AI → A′ H = BI → A′	SHIFT L = LFT H = RT	L = SUB H = ADD	Σ≠ZERO	Σ>ZERO	Σ′=ZERO	$\overline{C\text{-}OUT}$	X	Y	OVFL	$\overline{CCO}$
IIB	(B − A − 1) ↠ WR, XWR	H	H	H	L	H	L													
III	(A + B + $\overline{CIN}$) ↠ REGISTER	H	H	L	H	A′ SRC L = AI → A′ H = BI → A′	REGISTER L = Σ′ → MC H = Σ′ → XWR	B′ SOURCE LL = BI → B′ LH = WR → B′ HL = XWR → B′ HH* = L′S → B′		SHIFT L = LOG H = *ARITH	TYPE L = LFT H = RT	L = CARRY H = NO CARRY	Σ′≠ZERO	Σ′>ZERO	Σ′=ZERO	$\overline{C\text{-}OUT}$	X	Y	OVFL	$\overline{CCO}$
													*DURING ARITHMETIC SHIFTS A′ + C IS COMPARED TO −1						SHIFT OVFL	
													Σ′≠ −1	Σ′> −1	Σ′= −1	$\overline{C\text{-}OUT}$	X	Y		$\overline{CCO}$
IV	AI ↠ Σ′ BUS	H	H	H	L	H	H	REG OR AI LL = AI ↠ Σ′		SHIFT LL = LOG LH = ARITH HL = ROTATE HH (NOT DEFINED)		TYPE L = LFT H = RT	AI≠ZERO	AI>ZERO	AI=ZERO	$\overline{CIN}$	X	Y	L (FOR LSA OVFL)	$\overline{CCO}$
VA	WR ↠ WR	H	H	H	L	H	H	LH = WR ↠ WR												
VB	XWR ↠ XWR	H	H	H	L	H	H	HL = XWR ↠ XWR												
VI	WR, XWR ↠ WR, XWR	H	H	H	L	H	H	HH = WR,XWR → WR,XWR												
VIIA	A:B (N1:N2)	H	H	H	L	L	B′ SOURCE (SAME AS FORM I ABOVE)			A′ SRC L = AI → A′ H = WR → A′	OPER L = A:B H = B:A	H	N1>N2	N1>N2	N1=N2	=LG	X	Y	–	$\overline{CCO}$
VIIB	B:A (N1:N2)	H	H	H	L	L														
VIIIA	NOR/AND LOGICAL OPERATIONS	H	FUNCTION LHL = NOR LHH = OR HLL = XOR			A′ SRC L = AI → A H = WR → A	REG[3] LL = WR LH = XWR HL = PC HH = Σ′	B SOURCE LL = BI → B LH = WR → B HL = XWR → B HH = PC → B		A′ FNCT L = A → A′ H = $\overline{A}$ → A′	B′ FNCT L = B → B′ H = $\overline{B}$ → B′	REG[3] (SEE UNDER OP5 COLUMN)	Σ≠ZERO	Σ′>ZERO	Σ′=ZERO	=$\overline{CIN}$	X	Y	L	$\overline{CCO}$
VIIIB	OR/NAND LOGICAL OPERATIONS	H																		
VIIIC	EX OR/EX NOR LOGICAL OPERATIONS	H																		
IX	NO OPERATION (ZERO → Σ′ BUS)	H	H	H	H	H	H or L	H or L	H or L	H or L	H or L	H or L	L	L	H	=$\overline{CIN}$	X	Y	L	$\overline{CCO}$
X	CRC ACCUMULATION	H	H	H	H	L	L	L	L	L	O/I[5]	H	–	–	–	–	X	Y	L	$\overline{CCO}$
XI	SIGNED INTEGER DIVIDE A. START	H	H	H	H	L	L	H	L	H	H	H	–	–	DIV=ZERO	–	–	–	–	–
	B. ITERATE (N-1 CLKS)	H	H	H	H	L	H	L	H	O/I[6]	O/I[6]	H	–	–	–	–	–	–	–	–
	C. ITERATE FINISH	H	H	H	H	L	H	H	L	O/I[6]	O/I[6]	H	–	–	–	–	–	–	–	–
	D. FIX REMAINDER	H	H	H	H	L	H	L	L	O/I[6]	O/I[6]	H	–	–	–	–	–	–	–	–
	E. ADJUST QUOTIENT	H	H	H	H	L	L	H	H	O/I[6]	O/I[6]	H	–	–	–	–	–	–	–	–
XII	UNSIGNED DIVIDE A. START	H	H	H	H	L	L	L	L	H	H	L	–	DIV OVFL	–	–	–	–	–	–
	B. ITERATE (N-1 CLKS)	H	H	H	H	L	L	L	H	H	O/I[6]	L	–	–	–	–	–	–	–	–
	C. FINISH	H	H	H	H	L	L	L	H	L	O/I[6]	L	–	–	–	–	–	–	–	–
XIII	UNSIGNED MULTIPLY	H	H	H	H	L	L	H	L	L	O/I[6]	H	–	–	–	–	–	–	–	–
XIV	SIGNED INTEGER MULTIPLY	H	H	H	H	L	H	H	H	O/I[6]	O/I[6]	H	–	–	–	–	–	–	–	–

AO SEL (42)
L MC
H PC

DO1 SEL (29)
DO2 SEL (30)
LL Σ′ BUS
LH WR
HL XWR
HH HI-Z

BI/O SEL (29)
L OUTPUT
H INPUT

LD WR (24)
L AI → WR
H NO LOAD

INC MC (35)
L INC
H HOLD

INC PC (43)
L INC
H HOLD

CCI (44)
LSP L: x 1
LSP H: x 2
MID OR MSP
L CARRY
H NO CARRY

POS (19)
0 V = MID
2.4 V = LSP
5 V = MSP

DATA PORTS					
PIN NUMBER	AI	BI/O	DOP	AOP	BIT (2^n)
	(6)	(46)	(34)	(38)	0 (LSB)
	(5)	(47)	(33)	(39)	1
	(4)	(1)	(32)	(40)	2
	(3)	(2)	(31)	(41)	3 (MSB)

PIN ASSIGNMENTS

WRRT (26)	CK (45)
WRLFT (25)	V_{CC} (12)
XWRRT (28)	GND (36)
XWRLFT (27)	

NOTES:
1. NUMERALS IN PARENTHESIS ARE PIN NUMBERS
2. → DESTINED FOR ↠ SHIFTED AND DESTINED FOR
3. H = HIGH VOLTAGE LEVEL, L = LOW VOLTAGE LEVEL
4. X AND Y ARE CARRY LOOK-AHEAD FUNCTIONS
5. O IS OUTPUT ON LSP, I IS INPUT ON $\overline{LSP}$
6. O IS OUTPUT ON MSP, I IS INPUT ON $\overline{MSP}$
7. VOLTAGE VALUES ARE NOMINAL

3.2 OPERATION FORM I – ADD/SUBTRACT → REGISTER

Operation Form I is designed specifically to perform the addition or symmetrial subtraction of two operands. The operation form shown in Figure 21, is composed of two distinct capabilities:

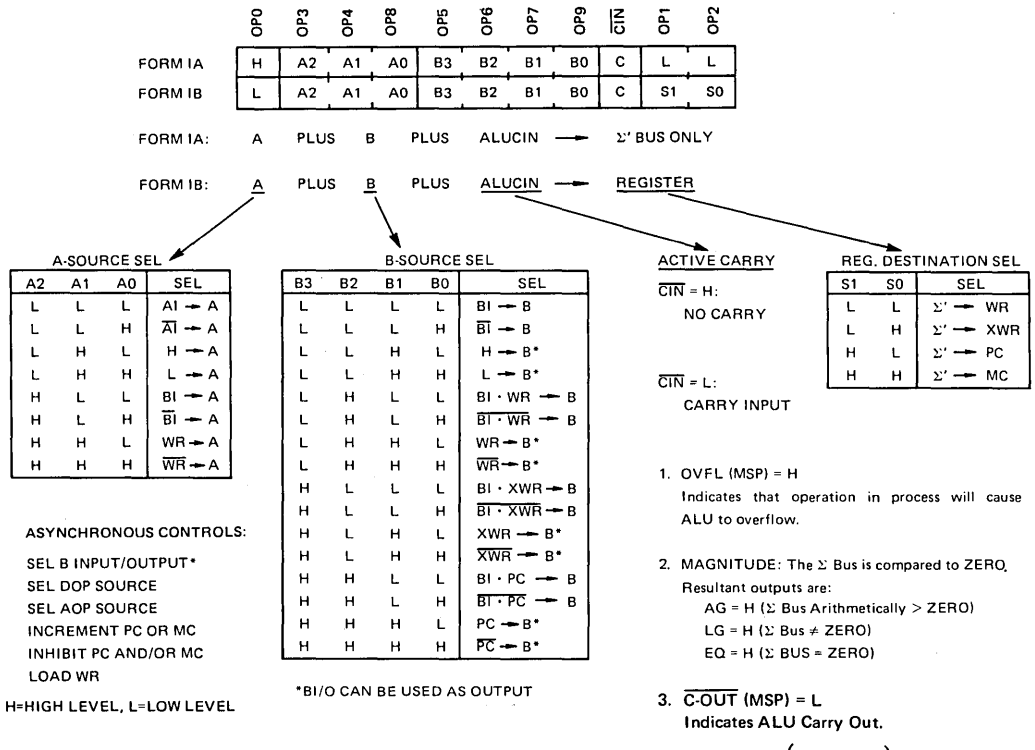


FIGURE 21 – FORM I–ARITHMETIC OPERATIONS: A PLUS B PLUS ALUCIN → { Σ' BUS / REGISTER }

a. Form IA provides the capability of adding or subtracting two operands and routing the results to the Σ' bus. Symbolically, this operation can be expressed as:

$$A \begin{Bmatrix} \text{PLUS} \\ \text{MINUS} \end{Bmatrix} B \text{ PLUS ALUCIN} \rightarrow \Sigma' \text{ BUS}$$

This form provides the capability of choosing from any one of the A and any one of the B sources listed in Figure 21 as the operands to accomplish the add/subtract. The example illustrated in Figure 22 utilizes the I/O capability of the B input/output port. Input data at the AI or B I/O is setup and then latched into the 'LS481/'S481 A or B input latch on the negative transition of the 'LS481/'S481 clock.

During Form IA operations, the contents of the extended working register are not changed and the working register may be saved or loaded directly. The program or memory counters under control of the asynchronous increment, inhibit, and LSP $\overline{CCI}$ can be saved or either may be incremented by one or two. Sources for the DOP and AOP are also selectable.

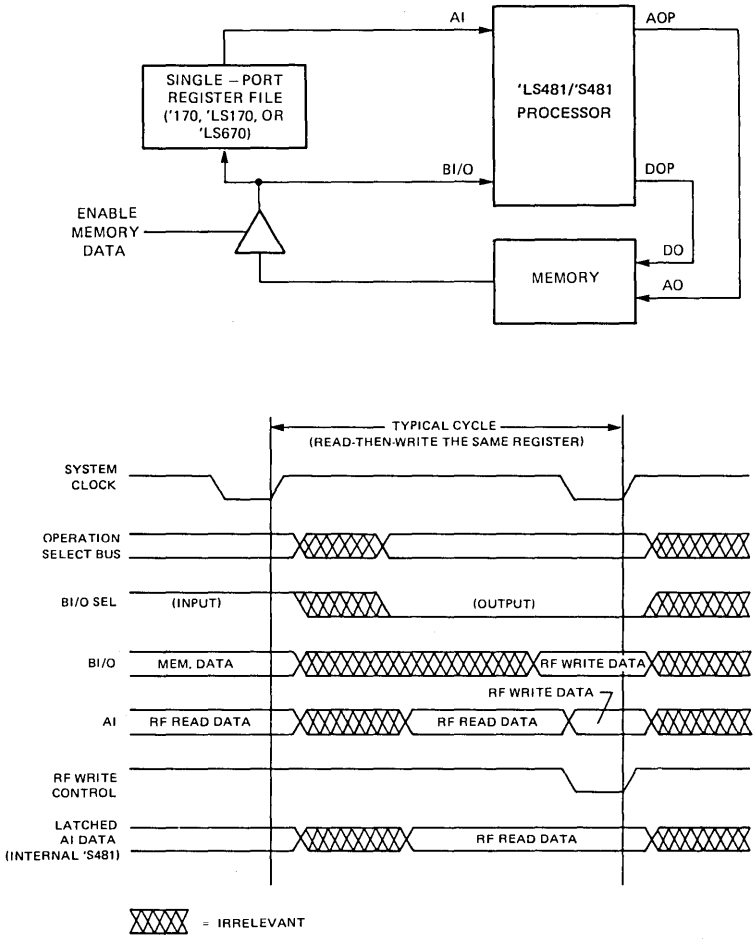


FIGURE 22 – 'LS481/'S481 OPERATION WITH SINGLE-PORT REGISTER FILE

The overflow and magnitude status lines are active as enumerated in Figure 21.

b. Form IB provides the capability of adding or subtracting two operands and routing the results to one of the four 'S481 storage destinations: the working register (WR), the extended working register (XWR), the program counter (PC), or the memory counter (MC). Symbolically, this operation can be expressed as:

$$A \left\{ \begin{matrix} \text{PLUS} \\ \text{MINUS} \end{matrix} \right\} \text{B PLUS ALUCIN} \rightarrow \text{REGISTER}$$

This form provides the capability of choosing from any one of the A and any one of the B sources listed in Figure 21 as the operands to accomplish the add/subtract.

3.3 OPERATION FORM II – ADD/SUBTRACT WITH DOUBLE-PRECISION SHIFT

Operation Form II is designed specifically to perform one of two classical iterations used frequently to implement microprogrammed multiply and divide algorithms. This form provides the system designer with the capability of selecting a single microinstruction which will complete both the add-and-shift or subtract-and-shift functions in a single clock cycle. Available microinstructions are illustrated in Figure 23. Symbolically, Form II operations can be represented as:

(A PLUS B PLUS ALUCIN)	SHIFTED → WR, XWR
(B MINUS A MINUS 1)	SHIFTED → WR, XWR

Hardwired algorithms for double-precision multiply and divide routines can be selected in operation forms XI, XII, XIII, or XIV.

During Form II operations the status, overflow, and asynchronous controls are the same as described for Form I.

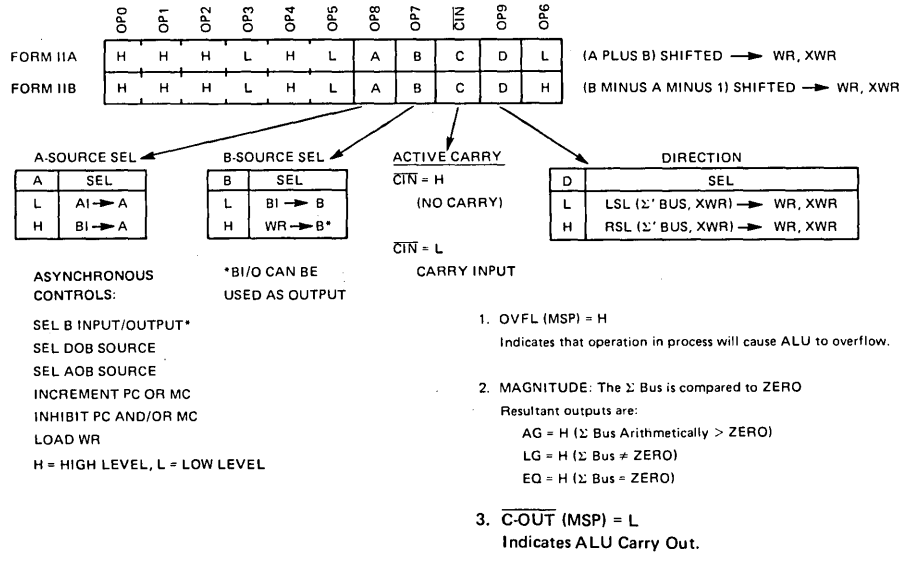


FIGURE 23 – FORM II–ARITHMETIC WITH DOUBLE-PRECISION SHIFT

$$\left\{\begin{matrix}A\\B\end{matrix}\right\} \text{ PLUS } \left\{\begin{matrix}B\\A\end{matrix}\right\} \text{ PLUS CARRY SHIFTED} \rightarrow \text{WR, XWR}$$

(MULTIPLY AND DIVIDE SHIFT OPERATIONS WITHOUT AUTOMATIC CONTROL)

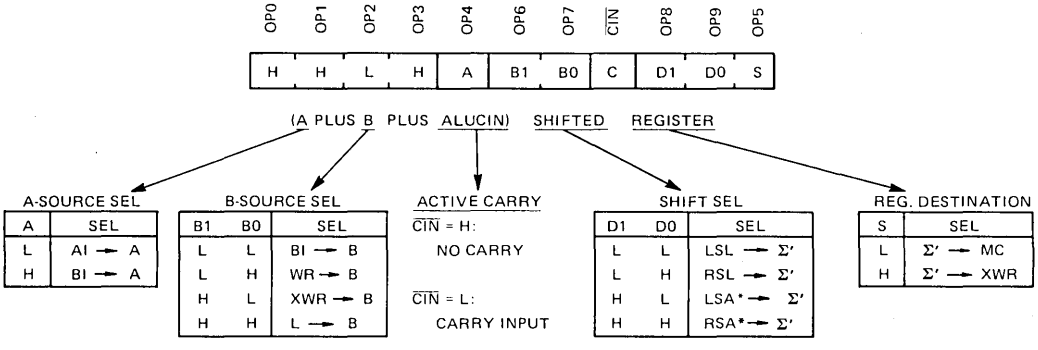
3.4 OPERATION FORM III – ADD WITH SINGLE-PRECISION SHIFT

Operation Form III is a universal microinstruction providing the designers with the capability of performing an add-and-shift function in a single clock cycle. Sources and destinations are shown in Figure 24. Also enumerated are the shift functions which are selectable as part of the microinstruction.

Magnitude and overflow status indicators are active as enumerated in Figure 24. Form III can be represented symbolically as:

(A PLUS B PLUS ALUCIN) SHIFTED → XWR, OR MC

During Form III operation the contents of the working register are not changed unless an asynchronous load is selected. If not selected as the destination, the extended working register will be saved. The memory counter can be the operand destination, or it and the program counter can be saved, or one can be incremented by one or two on selection. Sources for the DOP and AOP are also selectable.



ASYNCHRONOUS CONTROLS:

- SEL B INPUT/OUTPUT
- SEL DOB SOURCE
- SEL AOB SOURCE
- INCREMENT PC OR MC
- INHIBIT PC AND/OR MC
- LOAD WR

H = HIGH LEVEL, L = LOW LEVEL

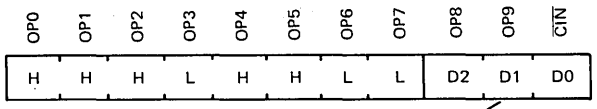
1. OVFL (MSP) = H Indicates that the shift operation in process will cause the selected register to overflow.
2. *MAGNITUDE: During LSA or RSA, A plus C (N1) is compared to $\overline{B}$ (N2); during the remaining operations, the Σ Bus is compared to ZERO. Resultant outputs are:
   AG = H (N1 ARITHMETICALLY > N2) or (Σ BUS ARITHMETICALLY > ZERO)
   LG = H (N1 > N2) or (Σ BUS ≠ ZERO)
   EQ = H (N1 = N2) or (Σ BUS = ZERO)
3. $\overline{COUT}$ (MSP) = L Indicates ALU Carry Out.

FIGURE 24 – FORM III–ARITHMETIC WITH SINGLE-PRECISION SHIFT (A PLUS B PLUS ALUCIN) SHIFTED → XWR OR MC

3.5 OPERATION FORM IV – AI SHIFTED → Σ' BUS

Operation Form IV is designed specifically for performing a single bit-position logical, arithmetic, or circular shift of the data applied at the A input port. This single clock operation can be used to shift information residing in any of the external working memory register locations simply by enabling the output capability of the BI/O port and writing the shifted word back into the same (or any other selected) memory location.

Asynchronous controls are the same as described for Operation Form IA, and the magnitude status lines are active and overflow is active during left-shift arithmetic (LSA) operation as enumerated in Figure 25.



SHIFT SEL

D2	D1	D0	SEL
L	L	L	LSL
L	L	H	RSL
L	H	L	LSA
L	H	H	RSA
H	L	L	LCIR
H	L	H	RCIR
H	H	L	NOT DEFINED
H	H	H	NOT DEFINED

ASYNCHRONOUS CONTROLS:

SEL B INPUT/OUTPUT
SEL DOB SOURCE
SEL AOB SOURCE
INCREMENT PC OR MC
INHIBIT PC AND/OR MC
LOAD WR

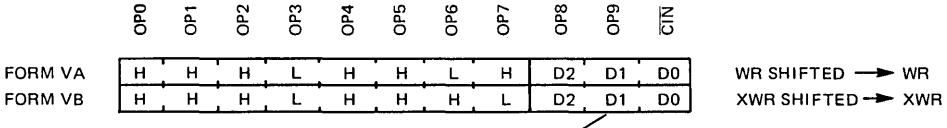
H = HIGH LEVEL, L = LOW LEVEL

1. $\overline{COUT} = \overline{CIN}$
2. OVFL (MSP = H)
   Indicates that LSA operation in process will cause shift overflow. For all other operations, OVFL = L.
3. MAGNITUDE: AI is compared to ZERO. Resultant outputs are:
   AG = H (AI > ZERO)
   LG = H (AI ≠ ZERO)
   EQ = H (AI = ZERO)

FIGURE 25 – FORM IV–AI SHIFTED → Σ' BUS

3.6 OPERATION FORM V – SINGLE-LENGTH SHIFT

Operation Form V performs a single-bit position, logical, arithmetic, or circular shift of either the working register or extended working register. Magnitude status indicators are active and overflow is active during left-shift arithmetic (LSA) operations as enumerated in Figure 26. Asynchronous controls are the same as described for Operation Form IA.



SHIFT SEL

D2	D1	D0	SEL
L	L	L	LSL
L	L	H	RSL
L	H	L	LSA
L	H	H	RSA
H	L	L	LCIR
H	L	H	RCIR
H	H	L	NOT DEFINED
H	H	H	NOT DEFINED

ASYNCHRONOUS CONTROLS:

SEL B INPUT/OUTPUT
SEL DOB SOURCE
SEL AOB SOURCE
INCREMENT PC OR MC
INHIBIT PC AND/OR MC
LOAD WR

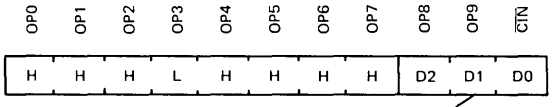
H = HIGH LEVEL, L = LOW LEVEL

1. $\overline{COUT} = \overline{CIN}$
2. OVFL (MSP - H)
   Indicates that LSA operation in process will cause shift overflow. For all other operations, OVFL ≡ L.
3. MAGNITUDE: AI is compared to ZERO. Resultant outputs are:
   AG = H (AI > ZERO)
   LG = H (AI ≠ ZERO)
   EQ = H (AI = ZERO)

FIGURE 26 – FORM V: {WR / XWR} SHIFTED → {WR / XWR}

3.7 OPERATION FORM VI – DOUBLE-PRECISION SHIFTS

Operation Form VI performs a double-precision logical, arithmetic, or circular shift of a double-length word residing in the working register and extended working register. Magnitude status indicators are active and overflow is active during left-shift arithmetic (LSA) operations as enumerated in Figure 27. Asynchronous controls are the same as described for operation form IA.



SHIFT SEL

D2	D1	D0	SEL
L	L	L	LSL
L	L	H	RSL
L	H	L	LSA
L	H	H	RSA
H	L	L	LCIR
H	L	H	RCIR
H	H	L	NOT DEFINED
H	H	H	NOT DEFINED

ASYNCHRONOUS CONTROLS:

SEL B INPUT/OUTPUT
SEL DOB SOURCE
SEL AOB SOURCE
INCREMENT PC OR MC
INHIBIT PC AND/OR MC
LOAD WR
H = HIGH LEVEL, L = LOW LEVEL

1. $\overline{COUT} = \overline{CIN}$
2. OVFL (MSP = H)
   Indicates that LSA operation in process will cause shift overflow. For all other operations, OVFL = L.
3. MAGNITUDE: AI is compared to ZERO. Resultant outputs are:

   AG = H (AI > ZERO)
   LG = H (AI ≠ ZERO)
   EQ = H (AI = ZERO)

FIGURE 27 – FORM VI–DOUBLE-PRECISION SHIFTS: (WR, XWR)SHIFTED →(WR, XWR)

3.8 OPERATION FORM VII – COMPARE (A:B OR B:A)

Operation Form VII is designed specifically to provide the system designer with the capability of symmetrically comparing either operands A-to-B or operands B-to-A. The operands selectable are enumerated in Figure 28 as the A source select or B source select. The carry output, overflow, and magnitude status lines decode and indicate the logical and arithmetic relationship of the operands being compared as shown in Figure 28. Asynchronous controls are the same as described for Operation Form IA.

3.9 OPERATION FORM VIII – LOGICAL FUNCTIONS

The ALU with its carry circuit functionally inactivated in Form VIII operations can be microprogrammed in conjunction with the source operands to perform any of the possible combinatorial Boolean functions on two binary variables. See Figure 29. Simple transfer functions are performed with the arithmetic operations in Form I, and combinatorial transfer and shift operations are available in Form III.

As with the arithmetic operations, a highly flexible source selection extends performance of single clock combinatorial logical operations between two (external) operands applied at the A and B input ports, or combinations of resident data in 'LS481/'S481 registers or counters can be combined logically with another register or external source. The specific combinations selectable are enumerated in the following paragraphs.

	OP0	OP1	OP2	OP3	OP4	OP8	OP5	OP6	OP7	OP9	$\overline{CIN}$	N1:N2
FORM VIIA	H	H	H	L	L	A	B2	B1	B0	L	H	A : B
FORM VIIB	H	H	H	L	L	A	B2	B1	B0	H	H	B : A

A-SOURCE SEL

A	SEL
L	AI
H	WR

B-SOURCE SEL

B2	B1	B0	SEL
L	L	L	BI
L	L	H	H*
L	H	L	BI · WR
L	H	H	WR*
H	L	L	BI · XWR
H	L	H	XWR*
H	H	L	BI · PC
H	H	H	PC*

ASYNCHRONOUS CONTROLS:

SEL B INPUT/OUTPUT*
SEL DOB SOURCE
SEL AOB SOURCE
INCREMENT PC OR MC
INHIBIT PC AND/OR MC
LOAD WR

*BI/O CAN BE USED AS OUTPUT (Σ BUS = N1–N2–1)

1. $\overline{COUT}$ = LG
2. MAGNITUDE: A or B (N1) is compared to B or A (N2), respectively. The resultant outputs are:
   AG = H (N1 arithmetically > N2)
   LG = H (N1 logically > N2)
   EQ = H (N1 = N2)
3. OVFL (MSP) IS NOT DEFINED.

H = HIGH LEVEL, L = LOW LEVEL

FIGURE 28 – FORM VII–COMPARE: $\begin{bmatrix} A:B \\ B:A \end{bmatrix}$

	OP0	OP1	OP2	OP3	OP4	OP8	OP6	OP7	OP9	OP5	$\overline{CIN}$	
FORM VIIA	H	L	H	L	A1	A0	B2	B1	B0	S1	S0	NOR
FORM VIIB	H	L	H	H	A1	A0	B2	B1	B0	S1	S0	OR
FORM VIIC	H	H	L	L	A1	A0	B2	B1	B0	S1	S0	EX-OR

A $\left\{\begin{matrix}\text{NOR}\\\text{OR}\\\text{X-OR}\end{matrix}\right\}$ B → REG

A-SOURCE SEL

A1	A0	SEL
L	L	AI → A
L	H	$\overline{AI}$ → A
H	L	WR → A
H	H	$\overline{WR}$ → A

B-SOURCE SEL

B2	B1	B0	SEL
L	L	L	BI → B
L	L	H	$\overline{BI}$ → B
L	H	L	WR → B*
L	H	H	$\overline{WR}$ → B*
H	L	L	XWR → B*
H	L	H	$\overline{XWR}$ → B*
H	H	L	PC → B*
H	H	H	$\overline{PC}$ → B*

REG DESTINATION SEL

S1	S0	SEL
L	L	Σ' → WR
L	H	Σ' → XWR
H	L	Σ' → PC
H	H	Σ' ONLY

*BI/O CAN BE USED AS OUTPUT.

ASYNCHRONOUS CONTROLS:

SEL B INPUT/OUTPUT*
SEL DOB SOURCE
SEL AOB SOURCE
INCREMENT PC OR MC
INHIBIT PC AND/OR MC
LOAD WR

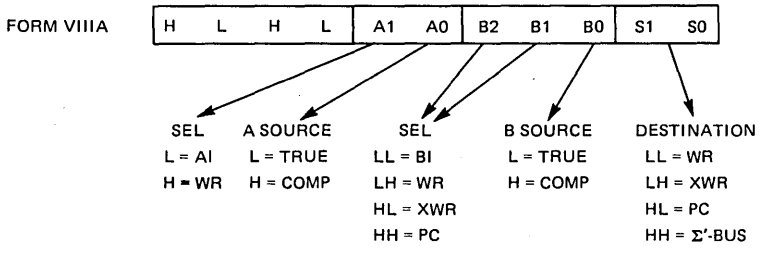
H = HIGH LEVEL, L = LOW LEVEL

1. $\overline{OVFL}$ = LOW
2. $\overline{COUT}$ = $\overline{CIN}$
3. MAGNITUDE: The Σ Bus is compared to ZERO. Resultant outputs are:
   AG = H (Σ Bus Arithmetically > ZERO)
   LG = H (Σ Bus ≠ ZERO)
   EQ = H (Σ Bus = ZERO)

FIGURE 29 – FORM VIII–LOGICAL OPERATIONS: A $\left\{\begin{matrix}\text{NOR}\\\text{OR}\\\text{X-OR}\end{matrix}\right\}$ B → REGISTER

3.9.1 NOR/AND Logical Operations

Operation Form VIIIA can be used to perform the NOR or AND logical combination of two selectable operands and route the results to one of four destinations. The operation microcode is:



H=HIGH LEVEL, L=LOW LEVEL

As shown above, the A and B sources are selectable by the A1, B1, and B2 bits in their true or complementary form (bits A0, B0) to facilitate performing the NOR, mixed NOR/AND, and the AND functions. As implemented, see Figure 30, the NOR function is performed when the sources are both true, mixed NOR/AND functions are performed with one source complemented, and the AND function is performed when both sources are selected in their complement form. Both implementation and other/equal logic symbols are shown in Figure 30. Also provided are the function tables and Boolean equations.

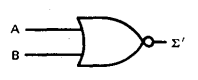
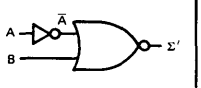
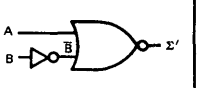
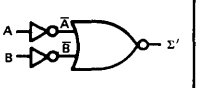
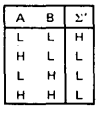
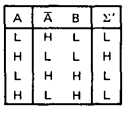
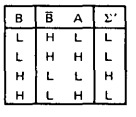
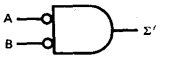
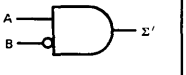
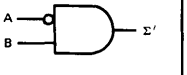
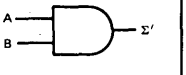
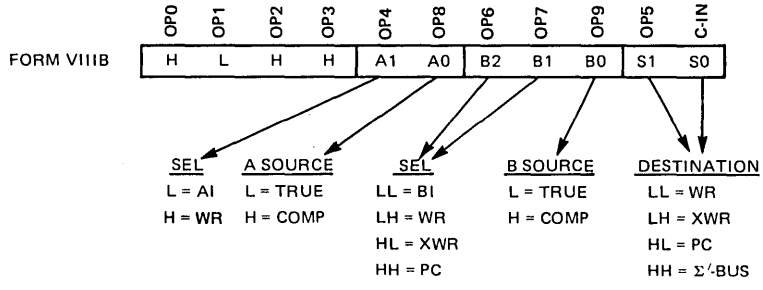
	SELECTIONS AVAILABLE			
	TRUE	A = COMP	B = COMP	A and B = COMP
IMPLEMENTATION				
FUNCTION TABLES (H = HIGH LEVEL, L = LOW LEVEL)	 OP8 = OP9 = L	 OP8 = H, OP9 = L	 OP8 = L, OP9 = H	 OP8 = OP9 = H
OTHER OR EQUAL SYMBOLS				
BOOLEAN FUNCTIONS	$\Sigma' = \overline{A + B}$	$\Sigma' = A\overline{B}$	$\Sigma' = \overline{A}B$	$\Sigma' = AB$

FIGURE 30 – FORM VIIIA NOR/AND LOGICAL OPERATIONS

3.9.2 OR/NAND Logical Operations

Operation Form VIIIB can be used to perform the OR or NAND logical combination of two selectable operands and route the results to one of four destinations. The operation microcode is:



H=HIGH LEVEL, L=LOW LEVEL

As shown above, the A and B sources are selectable by the A1, B1, and B2 bits in their true or complementary form (bits A0, B0) to facilitate performing the OR, mixed OR/NAND, and the NAND functions. As implemented, see Figure 31, the OR function is performed when the sources are both true, mixed OR/NAND functions are performed with one source complemented, and the NAND function is performed when both sources are selected in their complement form. Both implementation and other/equal logic symbols are shown in Figure 31. Also provided are the function tables and Boolean equations.

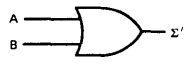
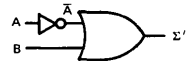
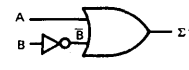
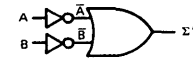
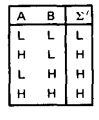
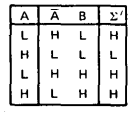
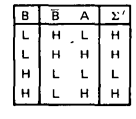
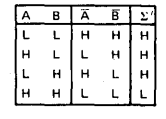
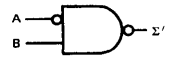
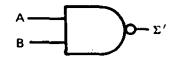
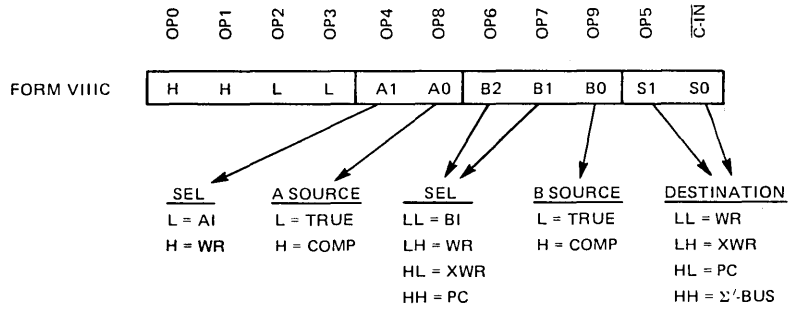
	SELECTIONS AVAILABLE			
	TRUE	A = COMP	B = COMP	A and B = COMP
IMPLEMENTATION				
FUNCTION TABLES (H = HIGH LEVEL, L = LOW LEVEL)	 OP8 = OP9 = L	 OP8 = H, OP9 = L	 OP8 = L, OP9 = H	 OP8 = OP9 = H
OTHER OR EQUAL SYMBOLS				
BOOLEAN FUNCTIONS	$\Sigma' = A + B$	$\Sigma' = \overline{A} + B$	$\Sigma' = A + \overline{B}$	$\Sigma' = \overline{A}\,\overline{B}$

FIGURE 31 – FORM VIIIB OR/NAND LOGICAL OPERATIONS

3.9.3 Exclusive-OR/Exclusive-NOR Logical Operations

Operation Form VIIIC can be used to perform the exclusive-OR/exclusive-NOR logical combination of two selectable operands and route the results to one of four destinations. The operation microcode is:



H = HIGH LEVEL, L = LOW LEVEL

As shown above, the A and B sources are selectable by the A1, B1, and B2 bits in their true or complementary form (bits A0, B0) to facilitate both exclusive-OR and exclusive-NOR operations. As implemented, see Figure 32, the exclusive-NOR function is performed when the sources are both true or both complemented. When either the A or the B source (not both) are complemented, the exclusive-OR function is performed. Both implementation and other/equal logic symbols are shown in Figure 32. Also provided are the function tables and Boolean equations.

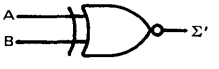
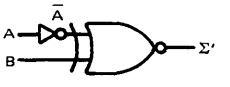
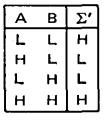
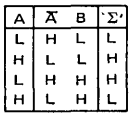
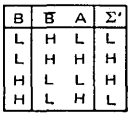
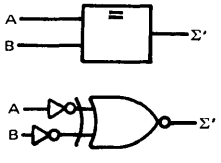
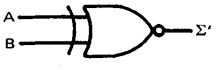
	ALL TRUE OR ALL COMPLEMENT SOURCES	ONE SOURCE COMPLEMENTED	
IMPLEMENTATION			
FUNCTION TABLES (H = HIGH LEVEL, L = LOW LEVEL)	 OP8 = OP9 = L	 OP8 = H, OP9 = L	 OP8 = L, OP9 = H
EQUAL OR OTHER SYMBOLS			
BOOLEAN FUNCTIONS	$\Sigma' = \overline{A \oplus B}$	$\Sigma' = A \oplus B$	$\Sigma' = A \oplus B$

FIGURE 32–FORM VIIIC EXCLUSIVE-OR/EXCLUSIVE-NOR OPERATIONS

3.10 OPERATION FORM IX – NO OP

Operation Form IX is designed specifically to clear the Σ′ bus force AG and LG low, and force EQ high; and, during this operation form data in the 'LS481/'S481 registers, counters and latches remain unchanged unless directed to do otherwise by the asynchronous control inputs as shown in Figure 33.

The memory or program counter can be incremented (by one or two) on each clock transition, or the working register can be loaded on each clock. Additionally, the B input/output can be specified, as well as sources for the address or data out ports. States of the carry and overflow outputs are not interrupted.

OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	OP8	OP9	$\overline{CIN}$
H	H	H	H	H	X	X	X	X	X	X

H = HIGH LEVEL, L = LOW LEVEL, X = IRRELEVANT

ASYNCHRONOUS CONTROLS:

SEL B INPUT/OUTPUT	
SEL DOB SOURCE	AG = ZERO
SEL AOB SOURCE	LG = ZERO
INCREMENT PC OR MC	EQ = HIGH
INHIBIT PC AND/OR MC	
LOAD WR	

FIGURE 33 – FORM IX–NO OPERATION: ZERO → Σ′ BUS

3.11 OPERATION FORM X – CYCLIC REDUNDANCY CHARACTER ACCUMULATION

Operation Form X is a macroinstruction which can be used to update a 16-bit cyclic redundancy character (CRC) partial sum in eight clock cycles, assuming 8-bit data characters. The updated CRC partial sum resides in the working register. The flow diagram of this algorithm is illustrated in Figure 34.

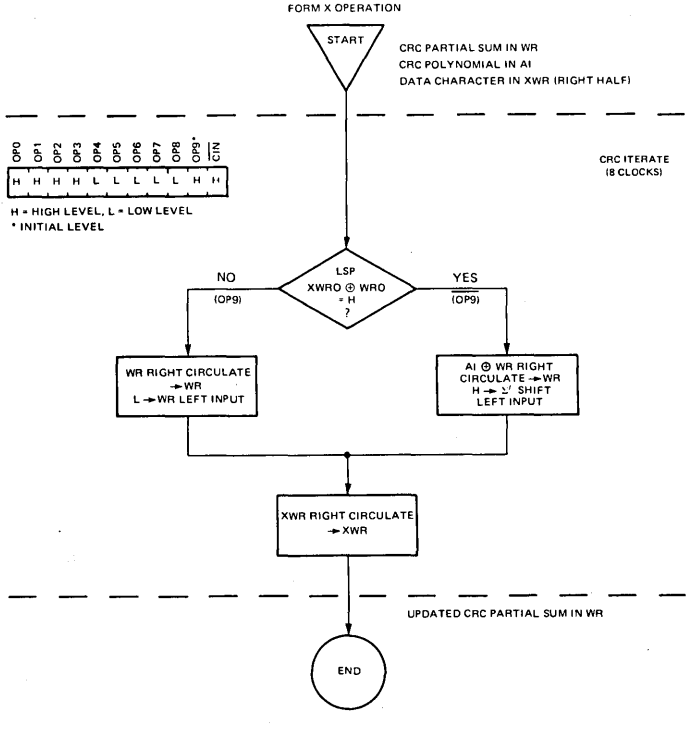


FIGURE 34 – CYCLIC REDUNDANCY CHARACTER ACCUMULATION

Setup conditions include the existence or placement of the previous CRC partial sum in the working register, the CRC polynomial at the A input port, and the data character in the eight least significant bits of the extended working register. All decisions after setup are decoded on chip for each of the eight iterations. Microcontrol open-collector output OP9 of the LSP assumes control during the iterations to generate one of two microinstructions requires to accomplish the CRC update.

3.12 OPERATION FORM XI – SIGNED INTEGER DIVIDE

Operation Form XI consists of the micro/macroinstructions needed to perform the signed division of a double length dividend by an N-bit divisor in N + 3 clock times. After the division routine the quotient will reside in the extended working register (XWR) and the remainder will be in the working register (WR). Negative results are in two's complement. The flow diagram of this algorithm is illustrated in Figure 35.

Setup conditions include the existence or placement of the double length dividend in the WR, XWR and application of the divisor at the A input port. To obtain a legitimate result, the divisor must not be arithmetically zero as indicated during the start command by the EQ output being low. The dividend must be of a nature that it could be generated by a signed multiply and add operation on the divisor. Status outputs LG, AG, C OUT and OV are undefined, as is EQ after the start command.

After setup, all decisions are decoded on chip for start, iterate, iteration finish, fix remainder, and adjust quotient. The iterate macroinstruction (Form XIB) internally decodes the status of the stored signs, carry out, and working register and the OP8 and OP9 microcontrol open-collector outputs of the MSP assume control generating one of four microinstructions required to accomplish the signed divide.

3.13 OPERATION FORM XII – UNSIGNED DIVIDE

Operation Form XII consists of micro/macroinstructions needed to perform the unsigned division of a double length dividend by an N-bit divisor in N + 1 clock times. After the division routine the binary magnitude quotient will reside in the extended working register (XWR) and the binary magnitude remainder will be in the working register (WR). The flow diagram of this algorithm is illustrated in Figure 36.

Setup conditions include the existence or placement of the double length dividend in the WR, XWR; application of the divisor at the A input port and that the last operation was not a divide command. To obtain a legitimate result, the N-bit divisor must be logically greater than the most-significant N-bits resident in the working register. A-input data compared to working register (AI:WR) prior to the unsigned divide can be used to obtain validity to start by asserting LG true.

After setup, all decisions are decoded on chip for start, iterate and finish. The iterate macroinstruction (Form XIIB) internally decodes the status of C OUT or FORCE LOAD FLAG and the OP9 microcontrol open-collector output of the MSP assumes control generating one of two microinstructions required to accomplish the unsigned divide.

3.14 OPERATION FORM XIII – UNSIGNED MULTIPLY

Operation Form XIII consists of a macroinstruction which performs the unsigned multiplication of two N-bit words in N clock times. After the multiply routine the double length product is residing in the working register (most-significant N-bits) and the extended working register (least-significant N-bits). The flow diagram of this algorithm is illustrated in Figure 37.

Setup conditions include clearing the working register to all zeros, loading (not shifting) the multiplier into the extended working register, and applying the multiplicand at the A input port. Arithmetic shift commands must not occur between multiplier load and the first iteration. Status outputs (EQ, AG, LG, C OUT and OV) are undefined during this algorithm.

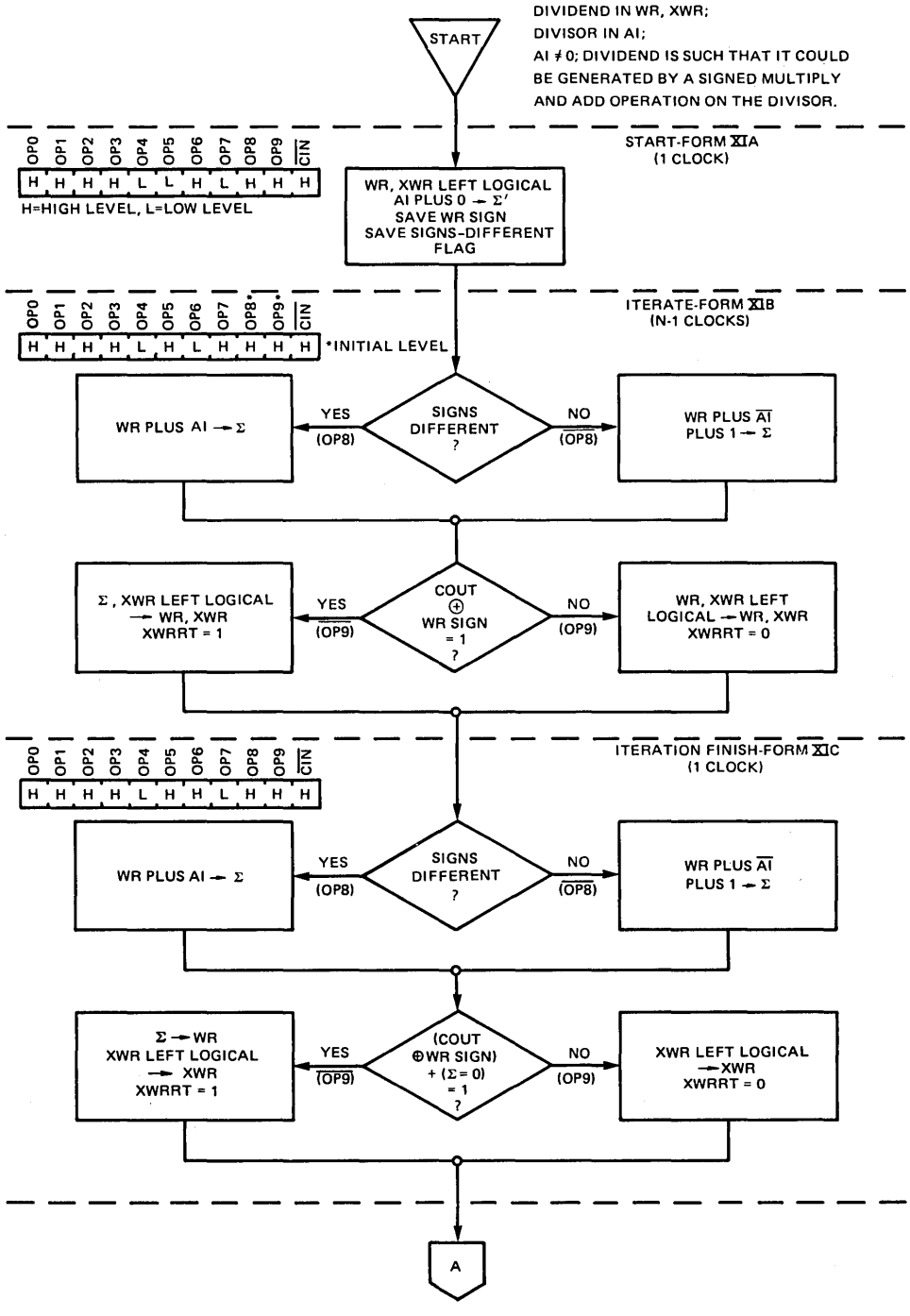


FIGURE 35 – FORM XI–SIGNED INTEGER DIVIDE (SHEET 1 OF 2)

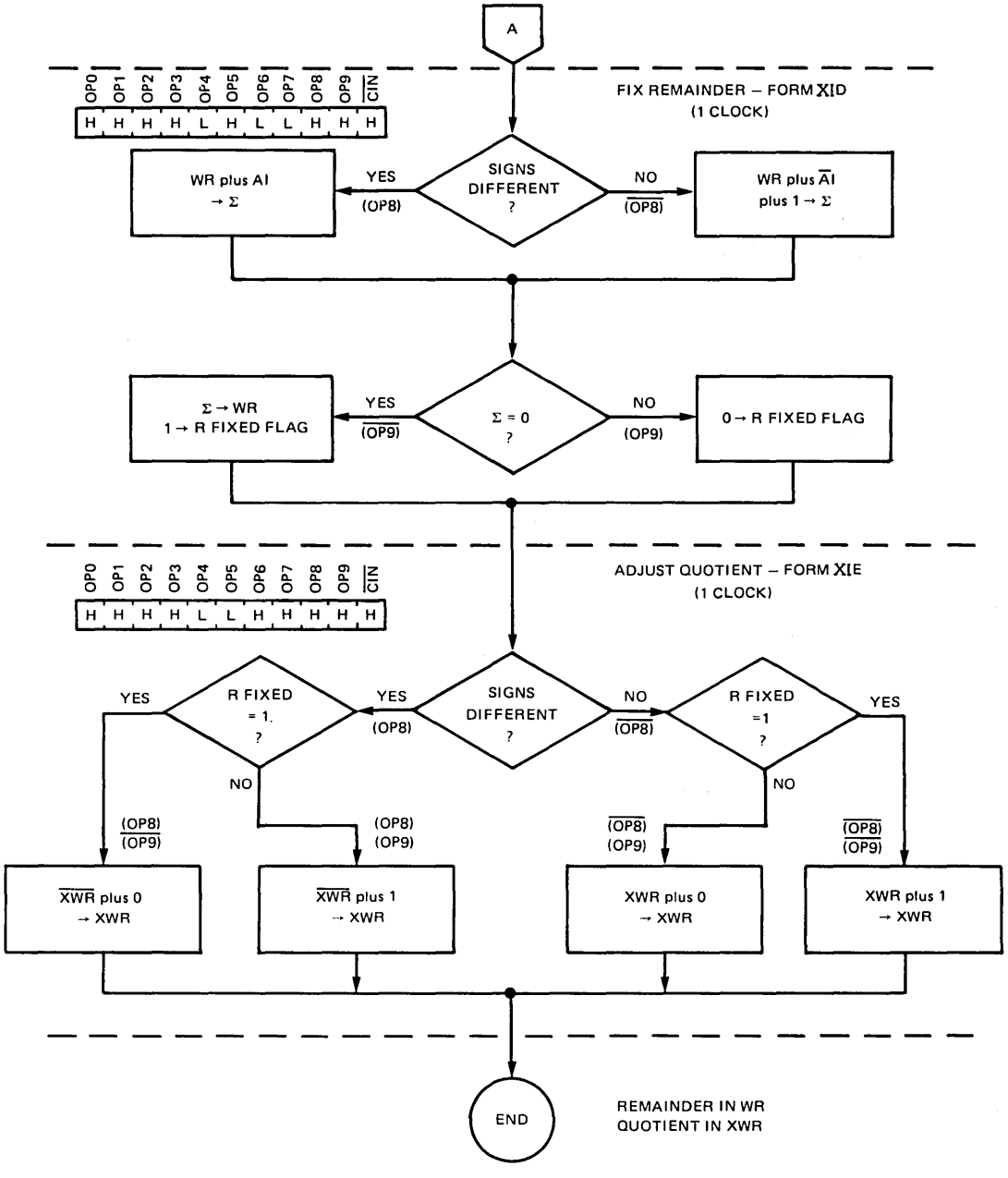


FIGURE 35 – FORM XI–SIGNED INTEGER DIVIDE (SHEET 2 OF 2)

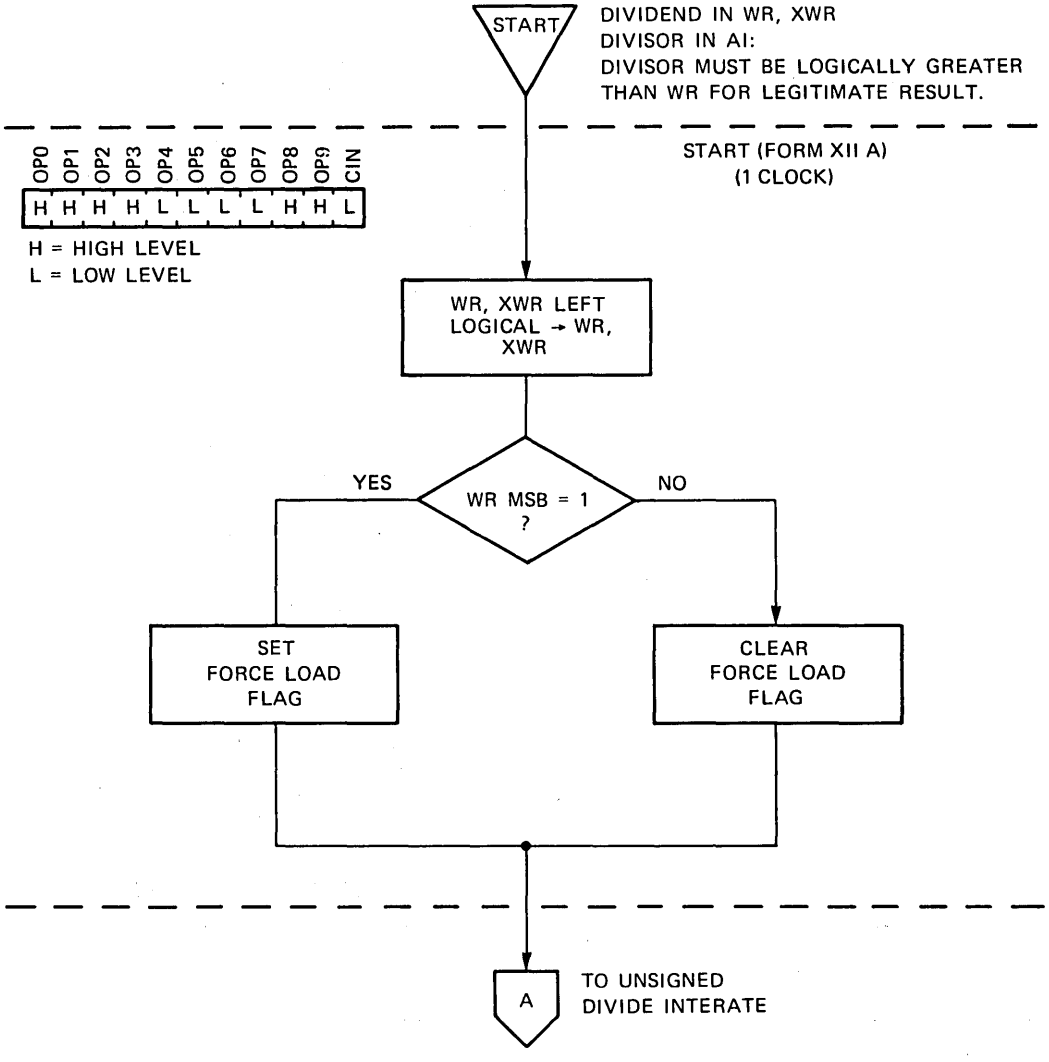


FIGURE 36 – FORM XII–UNSIGNED DIVIDE (SHEET 1 OF 2)

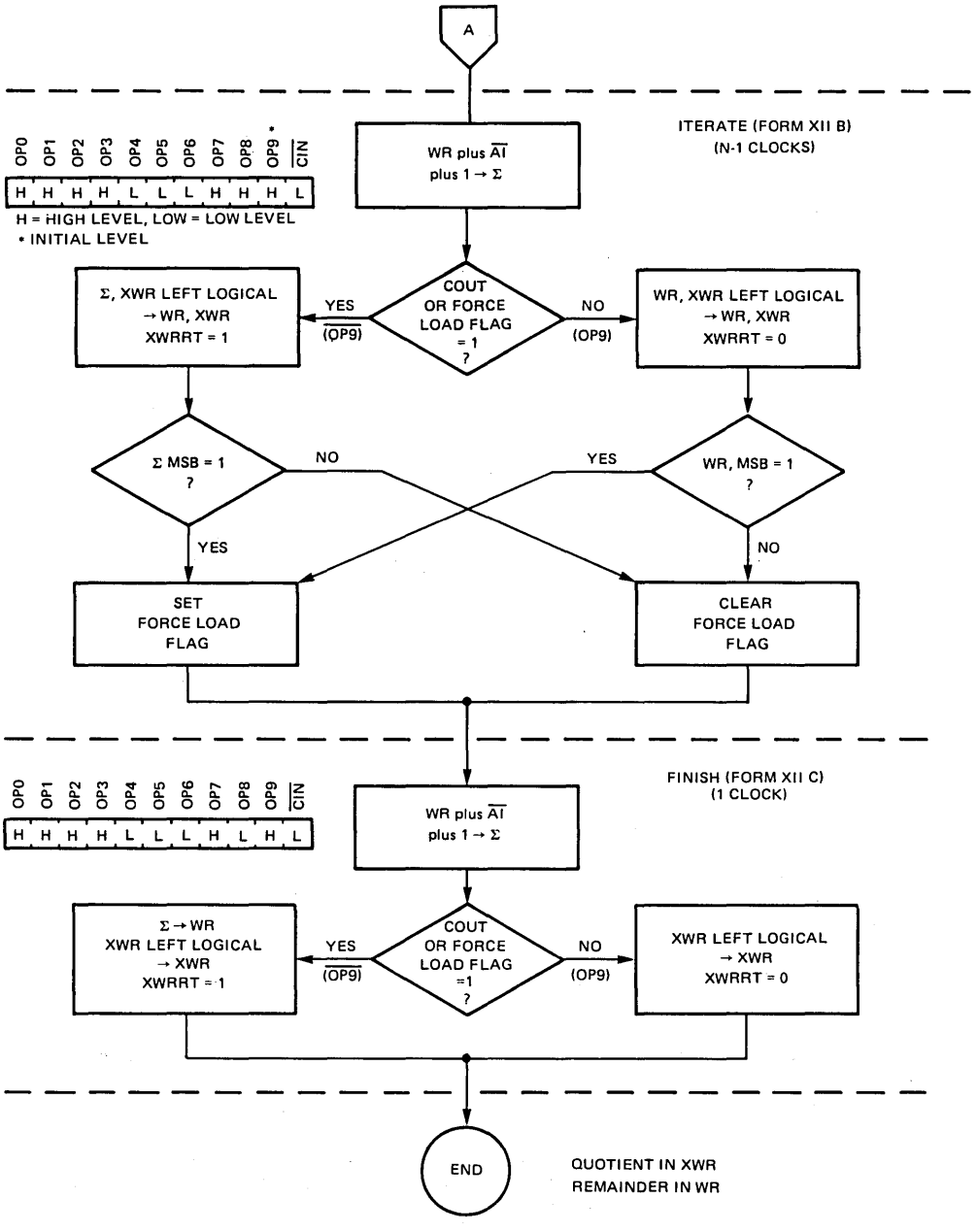


FIGURE 36 – FORM XII–UNSIGNED DIVIDE (SHEET 2 OF 2)

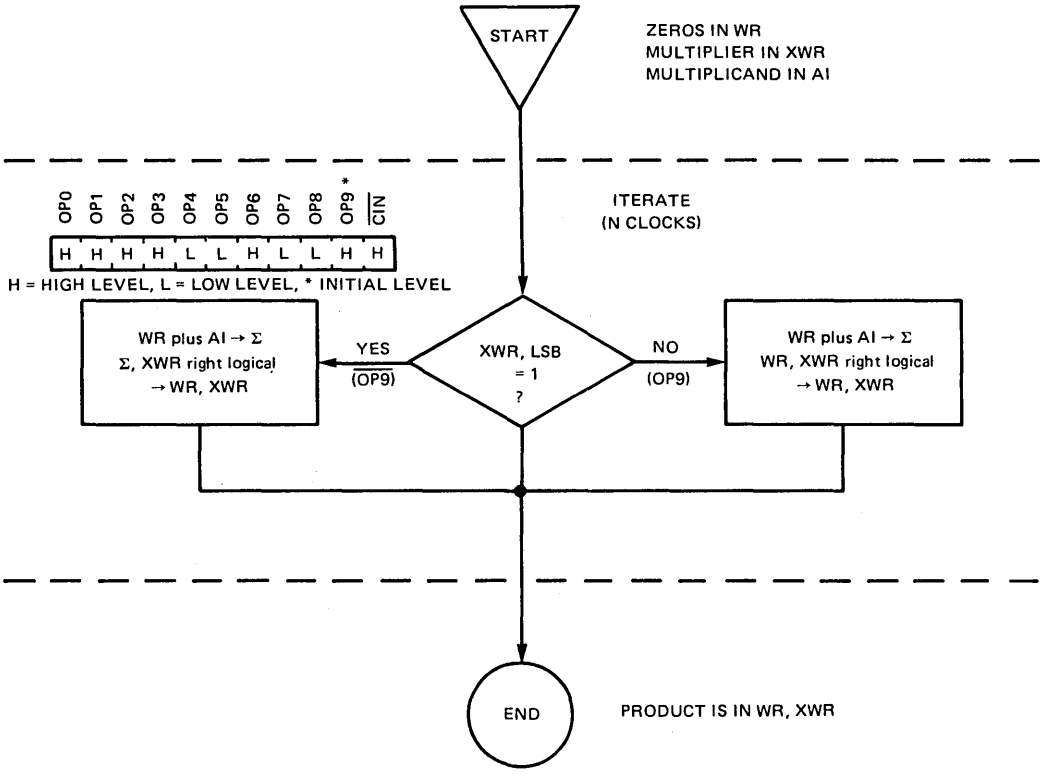


FIGURE 37 – FORM XIII–UNSIGNED MULTIPLY

The iterate macroinstruction internally decodes the status of the XWR LSB and the OP9 microcontrol open-collector output of the MSP assumes control generating one of two microinstructions required to accomplish the unsigned multiply.

3.15 OPERATION FORM XIV – SIGNED INTEGER MULTIPLY

Operation Form XIV consists of a macroinstruction which performs the signed multiplication of two N-bit signed integers in N clock times. After the multiply routine, the double precision signed product resides in the working register (most-significant N-bits) and the extended working register (least-significant N-bits). Negative products are in two's complement. The flow diagram of this algorithm is illustrated in Figure 38.

Setup conditions include clearing the working register to all zeros, loading (not shifting) the multiplier into the extended working register, and applying the multiplicand at the A input port. Arithmetic shifts must not occur between multiplier load and the first iteration. Status outputs (EO, AG, LG, C-OUT, and OV) are undefined during this algorithm.

The iterate macroinstruction internally decodes the status of the multiplier (XWR) sign-bit flag, the multiplier LSB, and the multiplier LSB flag and the OP8 and OP9 microcontrol open-collector outputs of the MSP assume control generating one of four microinstructions required to accomplish the signed multiply.

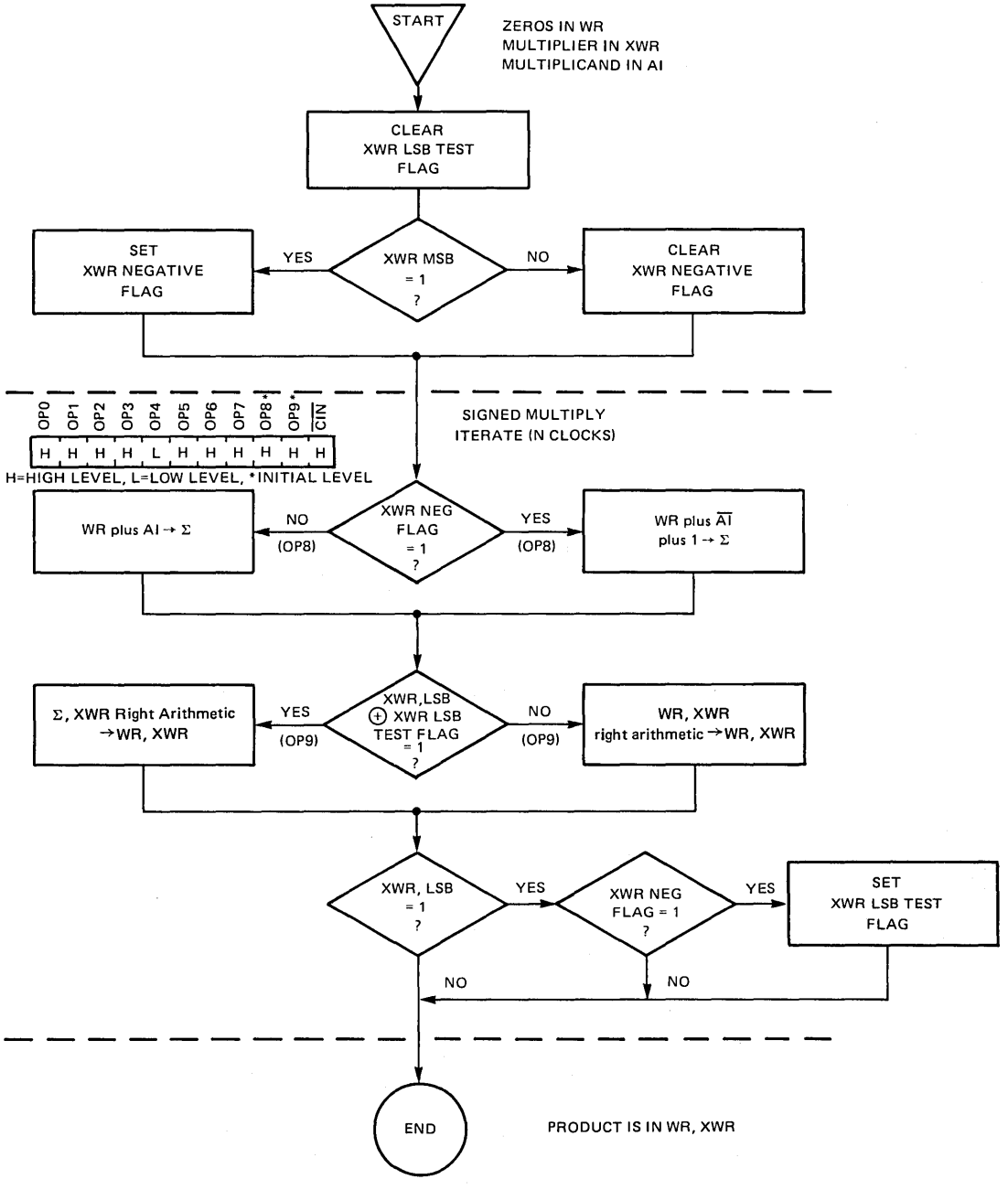


FIGURE 38 – FORM XIV–SIGNED INTEGER MULTIPLY

4. SPECIFICATIONS

TABLE 19 – SN74LS481/SN74S481 RECOMMENDED OPERATING CONDITIONS

		SN74LS481			SN74S481			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.75	5	5.25	4.75	5	5.25	V
High-level output voltage at EQ, OP8, OP9; V_O				5.5			5.5	V
Low-level output current, I_{OL}	AOP, BI/O, DOP, $\overline{CCO}$/OV, $\overline{COUT}$			10			10	mA
	EQ, OP8, OP9			8			8	
	WRLFT, WRRT, XWRLFT, XWRRT			4			6	
	X/LG, Y/AG			16			16	
High-level output current, I_{OH}	BI/O, DOP			6.5			6.5	mA
	All other outputs or I/O except EQ, OP8, OP9			1			1	
Width of clock pulse, t_w	High logic level	35			35			ns
	Low logic level	25			25			
Clock frequency				8			10	MHz
Setup time, t_{su}	AI, BI/O Latch	20↓			15↓			ns
	AI → WR	20↑			15↑			
	AI, BI/O → ALU → MPC, PC, WR, XWR	80↑			60↑			
	$\overline{CCI}$, $\overline{INCMC}$, $\overline{INCPC}$, $\overline{LDWR}$	40↑			30↑			
	OP0 thru OP9	140↑			100↑			
	$\overline{CIN}$	50↑			40↑			
	WRLFT, WRRT, XWRLFT, XWRRT	35↑			25↑			
Hold time, t_h	AI, BI/O → Latch	5↓			10↓			ns
	AI → WR	10↑			10↓			
	AI, BI/O → ALU → MC, PC, WR, XWR			−20↑			−20↑	
	$\overline{CCI}$, $\overline{INCMC}$, $\overline{INCPC}$, $\overline{LDWR}$	0↑			10↑			
	OP0 thru OP9			−15↑			−5↑	
	$\overline{CIN}$	0↑			0↑			
	WRLFT, WRRT, XWRLFT, XWRRT	0↑			5↑			
Operating free-air temperature range, T_A		0		70	0		70	°C

↑↓ The arrow indicates the transition of the clock input used for reference; ↑ for the low-to-high transition, ↓ for the high-to-low transition.

TABLE 20 – SN74S481 ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)

PARAMETER		TEST CONDITIONS†	SN74LS481			SN74S481			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage	see Note 1		2			2			V
V_{IL} Low-level input voltage	see Note 1				0.8			0.8	V
V_{IK} Input clamp voltage		V_{CC}=MIN, I_I=−18 mA			−1.2			−1.2	V
V_{OH} High-level output voltage	Any I/O or output except EQ, OP8, OP9	V_{CC}=MIN, V_{IH}=2 V, V_{IL}=0.8 V, I_{OH}=MAX	2.7	3.4		2.7	3.4		V
V_{OL} Low-level output voltage		V_{CC}=MIN, V_{IH}=2 V, V_{IL}=0.8 V, I_{OL}=MAX			0.5			0.5	V
I_{OH} High-level output current	EQ, OP8, OP9	V_{CC}=MAX, V_O=5.5 V			100			100	μA
I_I Input current at maximum input voltage	POS	V_{CC}=MAX, V_I=V_{CC}			1			1	mA
	Any other input	V_{CC}=MAX, V_I=5.5 V			1			1	
I_{IH} High-level input current	OP0, OP1, OP2, OP3, $\overline{CIN}$	V_{CC}=MAX, V_I=2.7 V			200			200	μA
	Any other (see Note 1)				100			100	μA
I_{IL} Low-level input current	OP0 thru OP3, $\overline{CIN}$, POS, $\overline{CCI}$	V_{CC}=MAX, V_I=0.5 V			−4			−8	mA
	WRRT, WRLFT, XWRRT, XWRLFT, CLOCK				−2			−6	
	Any other input				−1			−2	
I_{OS} Short-circuit output current§	Any output or I/O except EQ, OP8, OP9	V_{CC}=MAX	−30		−100			−100	mA
I_{CC} Supply current		V_{CC}=MAX		220	325		380	425	mA

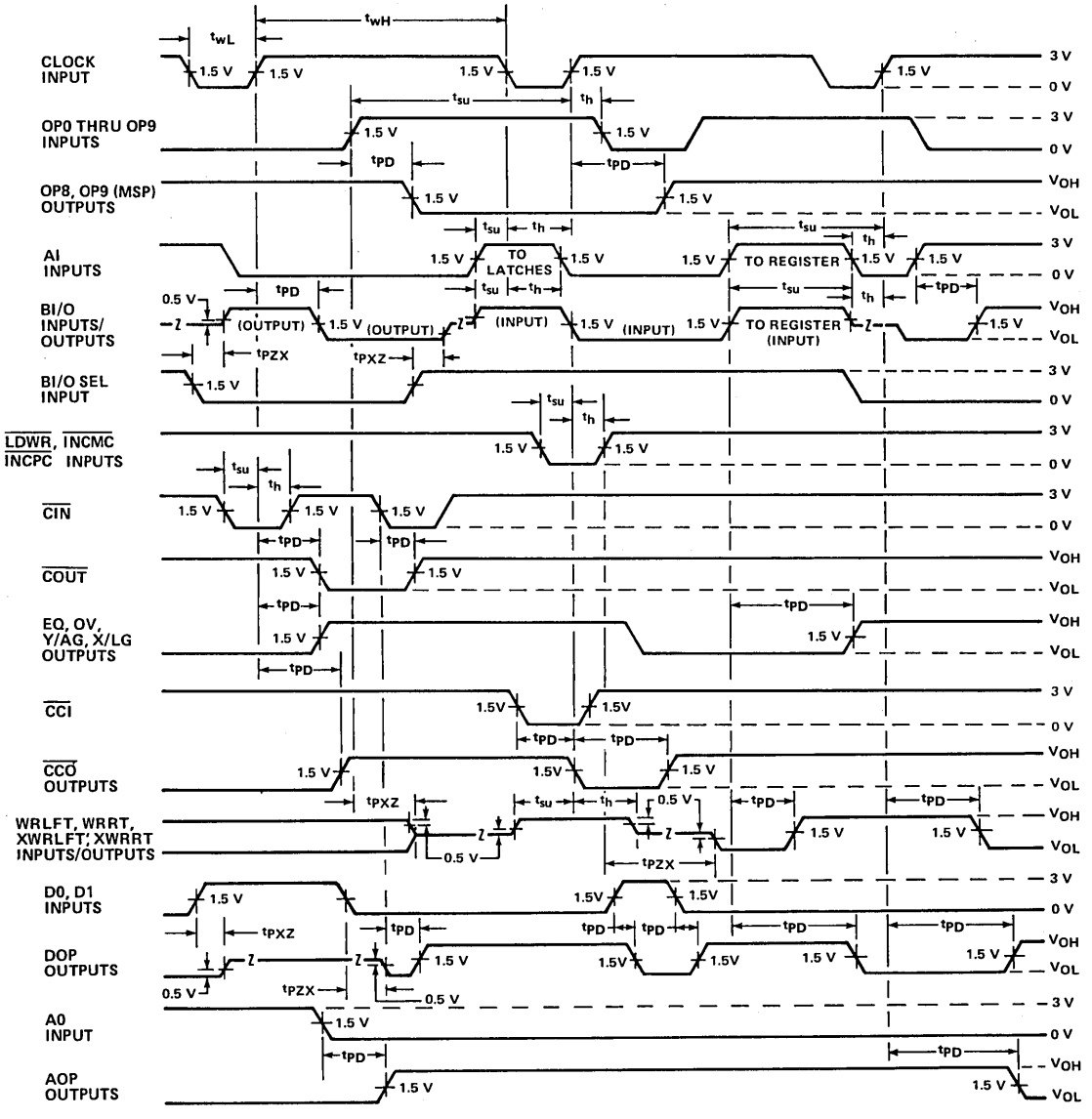
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.
NOTE 1: For POS input value see Table 3 on page 3-10.

TABLE 21
SN74S481 SWITCHING CHARACTERISTICS (OVER OPERATING RANGE OF V_{CC} AND T_A)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OPERATION ROUTING	SN74LS481		SN74S481		UNIT
				TYP	MAX	TYP	MAX	
t_{PD}	AL, BI/O	DOP	LATCH → ALU, DOP	56	80	42	65	ns
		X, Y,	LATCH → ALU	40	60	32	50	
		$\overline{COUT}$	LATCH → ALU	35	55	30	45	
		EQ	LATCH → ALU	55	85	45	65	
		OV	LATCH → ALU	45	65	35	45	
		AG, LG	LATCH → ALU	73	105	60	80	
		WRLFT, WRRT, XWRLFT, XWRRT	LATCH → ALU	60	85	45	65	
t_{PD}	OP0 thru OP9	WRLFT, WRRT, XWRLFT, XWRRT		100	135		95	ns
		$\overline{COUT}$		75	120	55	80	
		X, Y		75	120	60	85	
		EQ		75	120	55	75	
		OV		75	120	60	90	
		AG, LG		100	150	75	110	
		DOP		90	130	70	95	
t_{PD}	AI, BI/O	BI/O	LATCH → ALU	55	75	50	55	ns
t_{PD}	CIN	$\overline{COUT}$		35	55	30	45	ns
t_{PD}	$\overline{CCI}$	$\overline{CCO}$		55	80	37	60	ns
t_{PD}	A0	AOP		20	40	15	30	ns
t_{PD}	D0, D1	DOP		20	40	15	30	ns
t_{PXZ}	BI/O SEL or D0, D1	BI/O or DOP		20	30	15	30	ns
t_{PXZ}	OP0 thru OP9	WRLFT, WRRT, XWRLFT, XWRRT		60	100	45	80	ns
t_{PZX}	BI/O SEL or D0, D1	BI/O or DOP		20	30	15	30	ns
t_{PZX}	OP0 thru OP9	WRLFT, WRRT, XWRLFT, XWRRT		55	100	45	80	ns
t_{PD}	CLOCK	AOP, DOP	NO SHIFT	32	55	26	40	ns
		WRLFT, WRRT, XWRLFT, XWRRT	[WR, XWR, ΣBUS]	50	75	40	60	
		AOP, DOP	SHIFTED	40	50	35	40	
		OV		75	95	50	70	
		$\overline{CCO}$		35	50	25	40	
		$\overline{COUT}$		60	85	47	65	
		OP8, OP9		65	90	45	75	
		X, Y		65	90	48	75	
t_{PD}	$\overline{CIN}$	DOP		56	80	42	60	ns

t_{PD} ≡ Propagation delay
t_{PXZ} ≡ Disable time to Hi-Z
t_{PZX} ≡ Enable time (Hi-Z-to-Enable)
For load circuit and waveforms, see page 1-12.

3



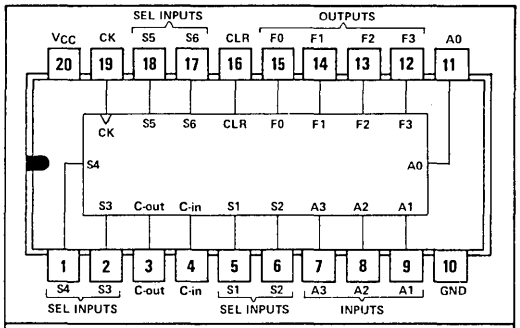
NOTE: Input pulses are supplied by a generator having the following characteristics:
$t_r \leq 5$ ns, tp ≤ 5 ns, PRR ≥ 1 MHz, ZOUT $\approx 50\ \Omega$

A0001385

FIGURE 39 – SWITCHING-TIME VOLTAGE WAVEFORMS

- 4-Bit Slice is Cascadable to N-Bits
- Designed Specifically for Microcontroller/ Next-Address Generator Functions
- Increment/Decrement by One (Immediate or Direct Symbolic Addressing Modes)
- Offset, Vector, or Branch (Indexed or Relative Addressing Modes)
- Store Up to Four Returns or Links (Program Return Address from Subroutine)
- Program Start or Initialize (Return to Zero or Clear Mode)
- On-Chip Edge-Triggered Output Register (Provides Steady-State Micro-Address/ Instruction)
- High-Density 20-Pin Dual-in-Line Package with 300-Mil Row Pin Spacing

SN54S482 . . . J PACKAGE
SN74S482 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: See function table.

These devices are also available in chip carriers. See Product Guide, Section 7, for pin assignments.

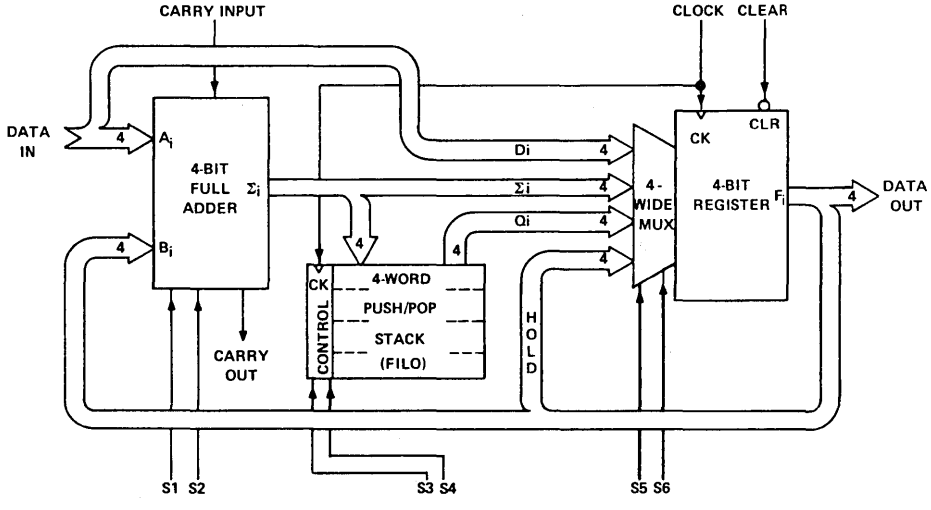
3

description

The 'S482 is a high-performance Schottky TTL 4-bit-slice control element for use in any computer/control application requiring the coupling of high-performance bipolar speeds with the flexibility of microprogram control and bit-slice expandability. When used as a next-address generator, two 'S482 elements can address up to 256 words of microprogram; three elements can address up to 4096 words of microprogram; or a number of 'S482 elements can generate N words in multiples of four lines.

Comprised of an output register, push-pop stack, and a full adder, the 'S482 provides the capability to implement multiway testing needed to generate or to determine and select the source of the next function of microprogram address.

functional block diagram



679

output register and source functions

The 4-bit edge-triggered register provides a steady-state output throughout each system clock cycle. An asynchronous clear extends the multiway testing to directly implement system initialization at ROM address zero.

Two source-select lines (S5, S6) provide the output register with access to either the current instruction (no change), an operand or address stored in the push-pop stack, the output of a four-function full adder, or a direct data-in address port. The sources and functions are summarized in Table I and II.

In bus applications, provision must be made to control negative spikes. When low, the output latches can be disturbed if the outputs are forced more negative than –0.5 V.

TABLE I. REGISTER-SOURCE FUNCTIONS

SELECT		REGISTER INPUT SOURCE
S5	S6	
L	L	DATA-IN PORT (Di)
L	H	FULL ADDER OUTPUTS (Σi)
H	L	PUSH-POP STACK OUTPUTS (Qi)
H	H	REGISTER OUTPUTS (HOLD)

H ≡ high level, L ≡ low level

TABLE II. PUSH-POP STACK CONTROL AND REGISTER-SOURCE FUNCTIONS

	INPUTS						INTERNAL	OUTPUTS
	S3	S4	S5	S6	CLOCK	CLEAR	QiA	Fi
HOLD	X	X	X	X	L	H	QiA0	Fi0
CLEAR	X	X	X	X	X	L	QiA0	L
PUSH-POP STACK "HOLD"	L	L	L	L	↑	H	QiA0*	Di
	L	L	L	H	↑	H	QiA0*	Σi
	L	L	H	L	↑	H	QiA0*	QiA0
	L	L	H	H	↑	H	QiA0*	Fi0
PUSH-POP STACK "LOAD"	L	H	L	L	↑	H	Σi*	Di
	L	H	L	H	↑	H	Σi*	Σi
	L	H	H	L	↑	H	Σi*	QiA0
	L	H	H	H	↑	H	Σi*	Fi0
PUSH-POP STACK "POP"	H	L	L	L	↑	H	QiB0†	Di
	H	L	L	H	↑	H	QiB0†	Σi
	H	L	H	L	↑	H	QiB0†	QiA0
	H	L	H	H	↑	H	QiB0†	Fi0
PUSH-POP STACK "PUSH"	H	H	L	L	↑	H	Σi‡	Di
	H	H	L	H	↑	H	Σi‡	Σi
	H	H	H	L	↑	H	Σi‡	QiA0
	H	H	H	H	↑	H	Σi‡	Fi0

MSB LSB
i ≡ 3, 2, 1, 0
Ai ≡ Data inputs
QiA ≡ Push-pop stack word A output (internal)
QiA0 ≡ the level of Qi before the indicated inputs conditions were established.

Fi ≡ Device outputs
Fi0 ≡ the level of Fi before the indicated input conditions were established.
Σi ≡ Adder outputs (internal)
*QiB, QiC, QiD do not change
†QiD0 → QiD, QiD0 → QiC, QiC0 → QiB, QiB0 → QiA
‡QiA0 → QiB, QiB0 → QiC, QiC0 → QiD

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

push-pop stack control

The 4-word push-pop stack can be used for nesting up to four levels of program or return (link) addresses. In the load mode, the first (top) word is filled with new data from the output of the full adder, and no push occurs meaning that previous data at that location is lost. However, all other word locations in the push-pop stack remain unchanged. In the push mode, the new word is again entered in the first (top) location; however, previous data residing in the top three words are pushed down one word location and retained at their new locations. The bottom word is written over and lost.

In the pop mode, words in the push-pop stack move up one location on each clock transition. A unique function is provided by the bottom (fourth) register as its content is retained during the pop mode, and after 3 clock transitions, all words in the stack are filled with the operand/address that occupied the bottom register.

The operand/address will remain available indefinitely if stack functions are limited to the pop or hold modes.

The push-pop stack functions are shown in Tables II and III.

TABLE III. PUSH-POP STACK FUNCTIONS

	FUNCTION	SEL. S3	SEL. S4	REG. D	REG. C	REG. B	REG. A	INPUT/ OUTPUT
BIT 0	LOAD	L	H	QiD0	QiC0	QiB0	← Σi	Σi IN
BIT 1	PUSH	H	H	← QiC0	← QiB0	← QiA0	← Σi	Σi IN
BIT 2	POP	H	L	↶ → QiD0	→ QiD0	→ QiC0	→ QiB0	QiA OUT
BIT 3	HOLD	L	L	QiD0	QiC0	QiB0	QiA0	QiA OUT

μlink operations show previous data location after clock transition.

full adder

The four-function full adder is controllable from select inputs S1 and S2 to perform:

A or B incrementation, or decrementation of B

Unconditional jumps or relative offsets

No change

Return to zero or one

Incrementation can be implemented by forcing a carry (high) into the ALU. In this mode either of the following options are possible:

1. Increment (A plus zero plus carry)
2. Increment B (zero plus B plus carry), or decrement B (all highs at A then A plus B with carry input low and disregard, don't use, carry out)
3. Increment the jump or offset (A plus B plus carry)

full adder (continued)

4. Start at zero or one and increment on each clock (select zero plus zero plus carry, then select zero plus B plus carry), or set register to N and decrement B (see 2 above).
5. No change (carry input is always active and removal of carry combined with either the ALU or register hold mode will retain the current address).

Unconditional jumps can be implemented by applying and selecting the jump directly from the data inputs to the output register. Offset can be accomplished by summing the output register with the offset magnitude (A plus B) with carry low.

The ALU functions are shown in Table IV.

TABLE IV. ADDRESS CONTROL FUNCTIONS

INPUTS		INTERNAL
S1	S2	Σi
H	H	0 PLUS 0 PLUS C-in
H	L	0 PLUS Bi PLUS C-in
L	H	Ai PLUS 0 PLUS C-in
L	L	Ai PLUS Bi PLUS C-in

compound generator functions

As the function-select lines of the register sources, push-pop stack, and adder are independent, compound functions can be selected to occur on the next clock transition.

Subroutine branches and returns can be simplified by saving the return or link addresses in the push-pop stack. This branch-and-save function can be accomplished on the same clock time as follows:

DATA-IN	ADDER	PUSH-POP STACK	REGISTER SOURCE
Branch address	Zero plus B plus one (S1 = H, S2 = L)	Push (S3 = S4 = H)	Data-in (S5 = S6 = L)

Up to four branches can be made with the return stored in the 4-word push-pop stack.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54S482 . . . . . −55°C to 125°C
SN74S482 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1. All voltage values are with respect to network ground terminal.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

recommended operating conditions

PARAMETER		SN54S482			SN74S482			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	Carry output			−1			−1	mA
	Any F output			−2			−2	
Low-level output current, I_{OL}	Carry output			10			10	mA
	Any F output							
Setup time, t_{su}	Data-in, S5, S6	0↑			0↑			ns
	Data-in via adder to stack	35↑			30↑			
	Data-in via adder to output latch	25↑			20↑			
	S1, S2	40↑			30↑			
	S3, S4	20↑			15↑			
	Clear-inactive state	0↑			0↑			
Pulse width, t_w	Clock (high or low)	50			30			ns
	Clear (low)	15			15			
Clock input rise time, t_r		20			25			ns
Hold time, t_h	Data-in, S5, S6	30↑			25↑			ns
	Data-in via adder	15↑			10↑			
	S1, S2	15↑			10↑			
	S3, S4	25↑			20↑			
Operating free-air temperature, T_A		−55		125	0		70	°C

↑ The arrow indicates that the rising edge of the clock pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54S482			SN74S482			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = MAX	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = MAX			0.5			0.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	S1, S2, Cin	V_{CC} = MAX,	V_I = 2.7 V			50			50	μA
		S3, S4, S5, S6, clock					100			100	
		Clear					250			250	
		Any A					150			150	
I_{IL}	Low-level input current	S1, S2	V_{CC} = MAX,	V_I = 0.5 V			−1			−1	mA
		C-in					−0.8			−0.8	
		S3, S4					−1.2			−1.2	
		Any A, S5, S6, CK					−2			−2	
		Clear					−4			−4	
		Clock					−2.8			−2.8	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−40		−110	−40		−110	mA
I_{CC}	Supply current		V_{CC} = MAX			90	130		90	140	mA

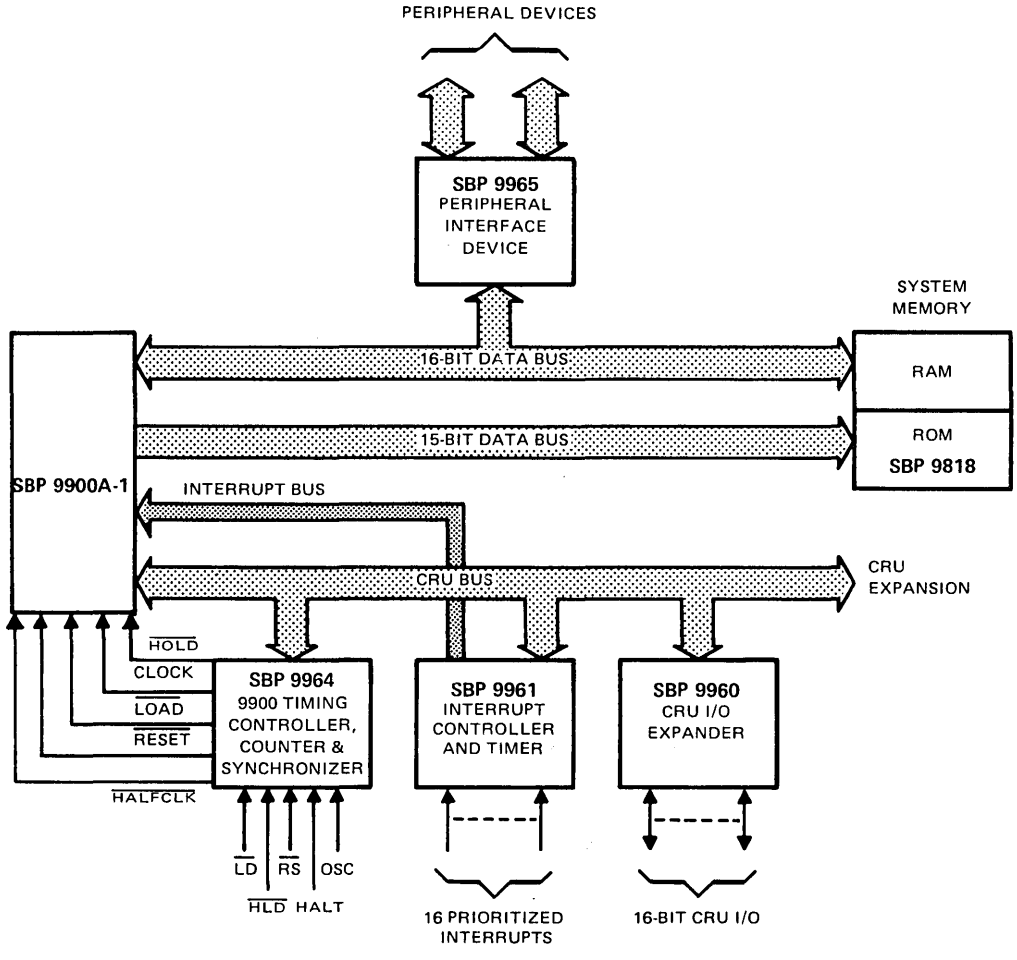
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

switching characteristics over recommended operating ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	SN54S482			SN74S482			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	CLOCK	DATA OUT	C_L = 15 pF, R_L = 280 Ω, See page 1-12		12	30		12	25	ns
t_{PHL}					15	30		15	25	
t_{PHL}	CLEAR	DATA OUT			12	25		12	20	ns
t_{PLH}	CARRY IN	CARRY OUT			12	22		12	18	ns
t_{PHL}					10	22		10	18	
t_{PLH}	DATA IN	CARRY OUT			17	30		17	25	ns
t_{PHL}					12	30		12	25	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

I^2L Microcomputer Components



I²L MICROPROCESSOR SYSTEM

PAGE

SBP 9900A-1 Microprocessors

Texas Instruments invented the integrated circuit, microprocessor and microcomputer, which have made TI synonymous with reliability, affordability, and compactness. The SBP9900A-1 16-bit microprocessor carries on TI's tradition of technology leadership.

TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

4

LIST OF ILLUSTRATIONS

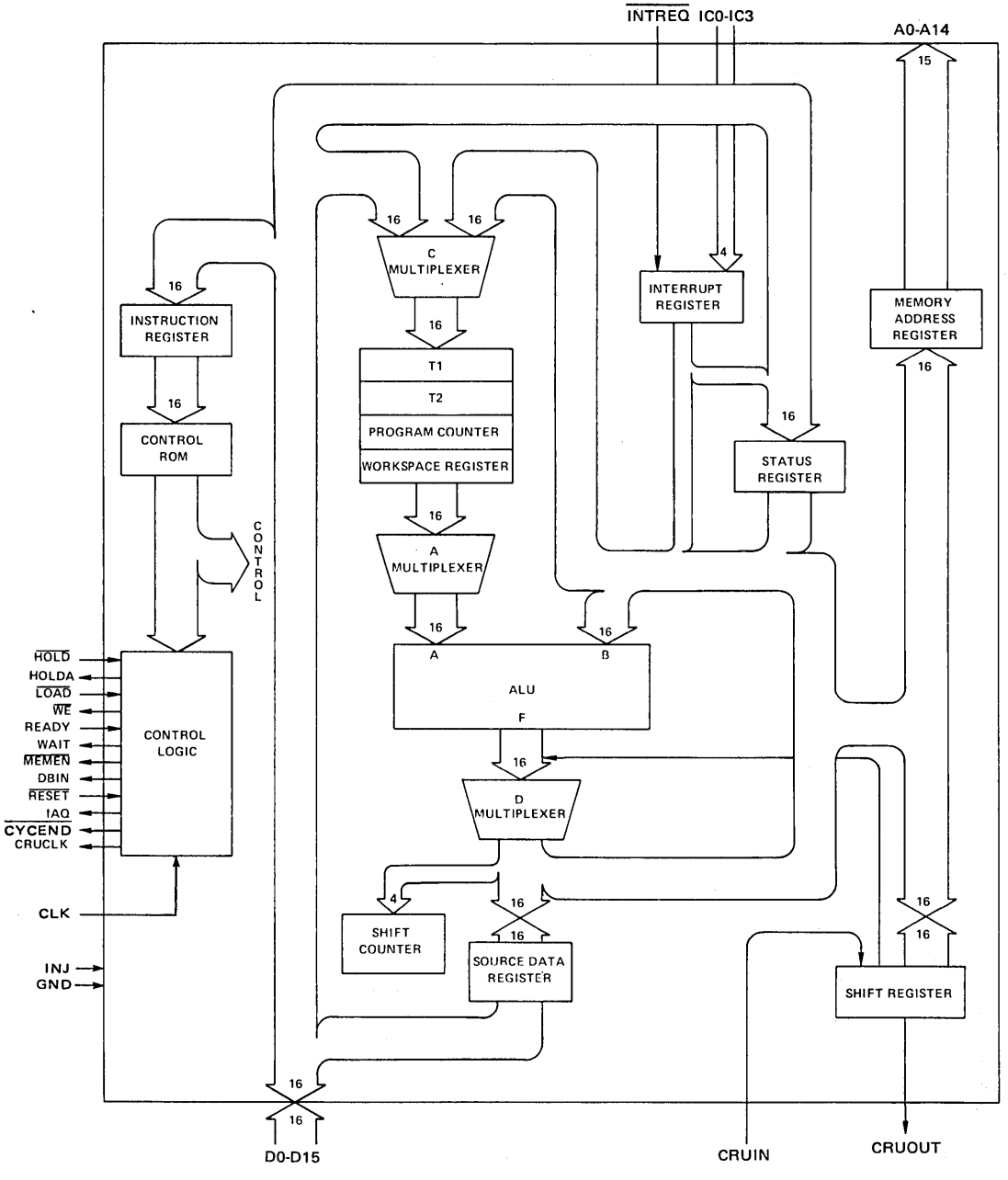


FIGURE 1 – SBP 9900A-1 ARCHITECTURE

1. INTRODUCTION

1.1 DESCRIPTION

The SBP 9900A microprocessor is a ruggedized monolithic Central Processing Unit (CPU) fabricated with Integrated Injection Logic (I^2L) technology. The SBP 9900A combines the properties of I^2L technology with a 16-bit word length, an advanced memory-to-memory architecture, and a full minicomputer instruction set to extend the end application reach of Texas Instruments 9900 microprocessor family into those applications requiring efficient, stable, reliable performance in severe operating environments. I^2L technology enables the SBP 9900A to operate over a very wide ambient temperature range from a dc power source. Static Logic is used throughout with directly TTL compatible I/O permitting use with standard logic and memory devices and thereby eliminating the need for special clock and interface functions. The SBP 9900A is software compatible with other 9900 microprocessor family members and shares a common body of hardware/software with Texas Instruments 990 minicomputer family.

1.2 KEY FEATURES

- Parallel 16-Bit Word Length
- Full Minicomputer Instruction Set Includes Multiply and Divide
- Directly Addresses Up to 65,536 Bytes/32,768 Words of Memory
- Advanced Memory-To-Memory Architecture
- Multiple 16-Word Register Files (Work Spaces) Reside in Memory
- Separate I/O, Memory and Interrupt Bus Structures
- 16 Prioritized Hardware Interrupts
- 16 Software Interrupts (XOPS)
- Programmed and DMA I/O Capability
- Serial I/O Via Communications-Register-Unit (CRU)
- 64-Pin Package
- Software Compatible with TI 9900 Microprocessor/9900 Minicomputer Family
- I^2L Technology:
  - Single dc Power Supply
  - Fully Static Operation
  - Single Phase Clock
  - Directly TTL Compatible I/O (Including Clock)
  - Operates Over Wide Temperature Range:
    - –55°C to 125°C for SBP 9900AM, SBP 9900AN (883 B)
    - –40°C to 85°C for SBP 9900AE
    - 0°C to 70°C for SBP 9900AC
- SBP 9900A-N Provided with 100% Processing in accordance with Method 5004 of MIL-STD-883B.

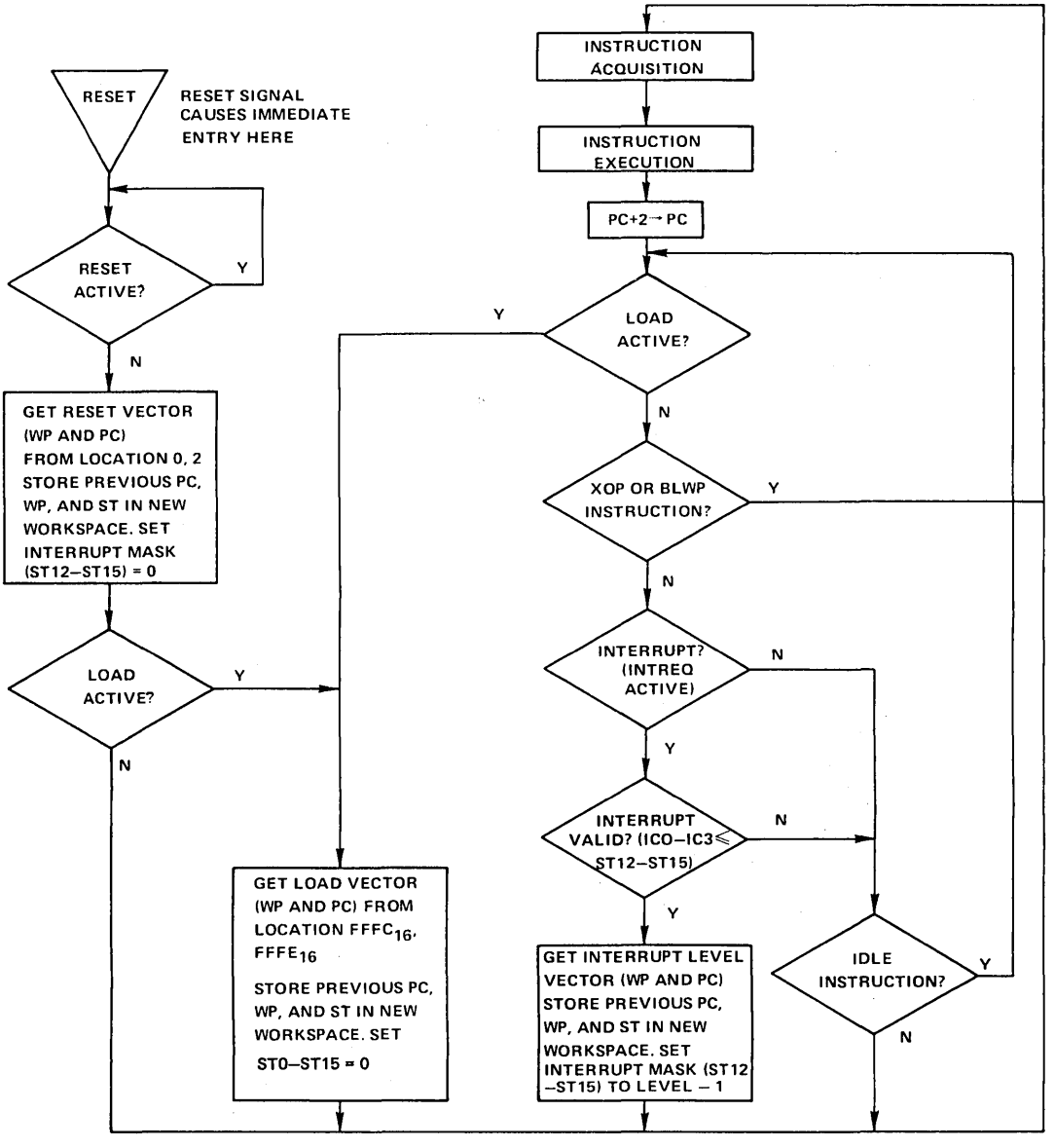


FIGURE 2 – 9900 CPU FLOW CHART

The SBP 9900A is a 16-bit processor with 69 instructions including byte and bit addressing. The 16-bit word is used to address 32K words or 65K bytes of memory. Processing power comes not only from the 16-bit word length, but also from eight powerful addressing modes and the use of memory as working registers. It is, in fact, this concept called the "Workspace Register" concept that is the most outstanding architectural feature of the SBP 9900A. In contrast to the pushdown stack found in many minicomputers and microprocessors, the workspace register file is a contiguous block of 16 words in memory used as working registers. Storage of intermediate results and subroutine return addresses, as well as index register functions, is accomplished in the workspace.

Most important of all is that each small routine, program or subroutine may have its own 16-word workspace. A workspace pointer (a 16-bit register within the arithmetic unit) points to the first word of the appropriate workspace for any given program. This is especially significant in systems where interrupt processing is used, or where multifunction applications require frequent changes of program context. When an interrupt occurs, for example, there is no need to save register contents and a return address in a stack or other block of memory, because they are all in the workspace. The Program Counter, Status Register, and Workspace Pointer (PC, ST, WP) are saved in three words of the workspace, the WP is set to a new value, pointing to the appropriate service routine, and processing resumes around a new set of workspace registers.

The primary impact of the workspace is to give the program designer 16 "working registers" for *every routine and subroutine;* and because the "registers" are actually memory words, there is no need to save and restore register contents when jumping from one routine to another.

Other important features of the SBP 9900A are vectored interrupts (16 levels), an asynchronous I/O bus, and a Communications Register Unit (CRU) to accommodate I/O circuit cards for a wide variety of peripherals and general interface requirements.

4

2. ARCHITECTURE

The memory word of the 9900 is 16 bits long. Each word is also defined as 2 bytes of 8 bits. The instruction set of the 9900 allows both word and byte operands. Thus, all memory locations are on even address boundaries and byte instructions can address either the even or odd byte. The memory space is 65,536 bytes or 32,768 words. The word and byte formats are shown in Figure 3.

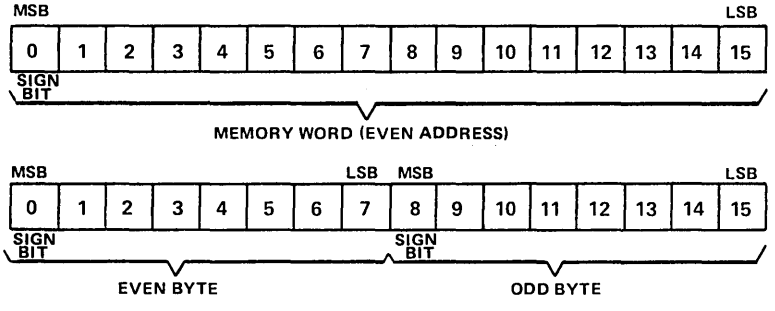


FIGURE 3 – WORD AND BYTE FORMATS

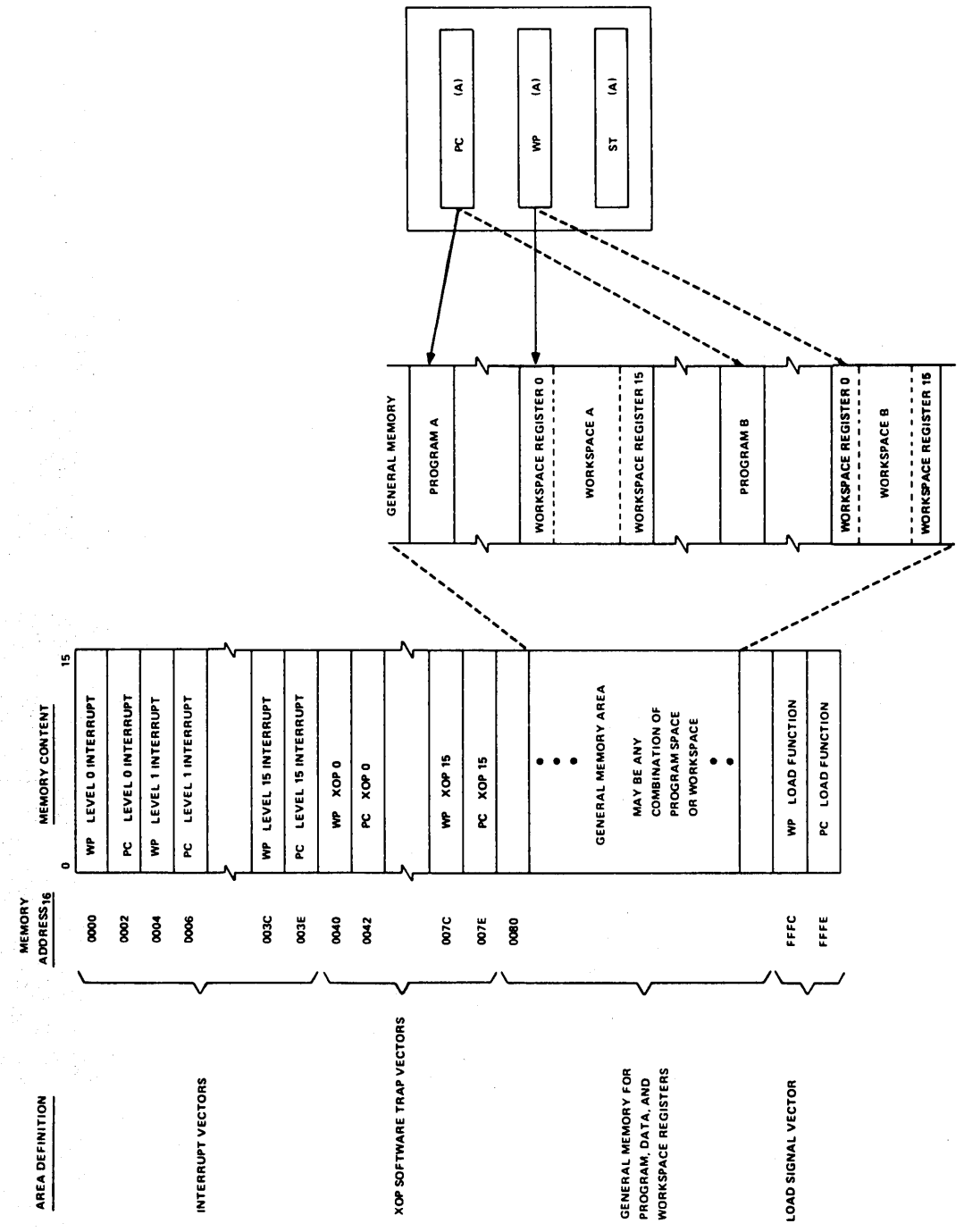


FIGURE 4 – MEMORY MAP AND WORKSPACE CONCEPT

2.1 REGISTERS AND MEMORY

The 9900 employs an advanced memory-to-memory architecture. The 9900 memory map is shown in Figure 4.

The first 32 words are used for interrupt trap vectors. The next contiguous block of 32 memory words is used by the extended operation (XOP) instruction for trap vectors. The last two memory words, $FFFC_{16}$ and $FFFE_{16}$, are used for the trap vector of the $\overline{LOAD}$ signal. The remaining memory is then available for programs, data, and workspace registers. If desired, any of the special areas may also be used as general memory.

Three internal registers are accessible to the user. The program counter (PC) contains the address of the instruction following the current instruction being executed. This address is referenced by the processor to fetch the next instruction from memory and is then automatically incremented. The status register (ST) contains the present state of the processor and will be further defined in Section 3.4. The workspace pointer (WP) contains the address of the first word in the currently active set of workspace registers.

A workspace-register file occupies 16 contiguous memory words in the general memory area (see Figure 4). Each workspace register may hold data or addresses and function as operand registers, accumulators, address registers, or index registers. During instruction execution, the processor addresses any register in the workspace by adding the register number to the contents of the workspace pointer and initiating a memory request for the word. The relationship between the workspace pointer and its corresponding workspace is shown in Figure 4.

The workspace concept is particularly valuable during operations that require a context switch which is a change from one program environment to another (as in the case of an interrupt) or to a subroutine. Such an operation, using a conventional multi-register arrangement, requires that at least part of the contents of the register file be stored and reloaded. A memory cycle is required to store or fetch each word. By exchanging the program counter, status register, and workspace pointer in the 9900 concept accomplishes a complete context switch withonly three store cycles and three fetch cycles. See Figure 4. After the switch the workspace pointer contains the starting address of a new 16-word workspace in memory for use in the new routine. A corresponding time saving occurs when the original context is restored. Instructions in the 9900 that result in a context switch include:

1. Branch and Load Workspace Pointer (BLWP)
2. Return from Subroutine (RTWP)
3. Extended Operation (XOP).

Device interrupts, $\overline{RESET}$, and $\overline{LOAD}$ also cause a context switch by forcing the processor to trap to a service subroutine.

2.2 INTERRUPTS

The 9900 employs 16 interrupt levels with the highest priority level 0 and lowest level 15. Level 0 is reserved for the $\overline{RESET}$ function and all other levels may be used for external devices. The external levels may also be shared by several device interrupts, depending upon system requirements.

The 9900 continuously compares the interrupt code (IC0 through IC3) with the interrupt mask contained in status-register bits 12 through 15. When the level of the pending interrupt is less than or equal to the enabling mask level (higher or equal priority interrupt), the processor recognizes the interrupt and initiates a context switch following completion of the currently executing instruction. The processor fetches the new context WP and PC from the interrupt vector locations. Then, the previous context WP, PC, and ST are stored in workspace registers 13, 14, and 15, respectively, of the new workspace. The 9900 then forces the interrupt mask to a value that is one less than

the level of the interrupt being serviced. This allows only interrupts of higher priority to interrupt a service routine. The processor also inhibits interrupts until the first instruction of the service routine has been executed. All interrupt requests should remain active until recognized by the processor in the device-service routine. The individual service routines must reset the interrupt requests before the routine is complete.

If a higher priority interrupt occurs, a second context switch occurs to service the higher priority interrupt. When that routine is complete, a return instruction (RTWP) restores the first service routine parameters to the processor to complete processing of the lower-priority interrupt. All interrupt subroutines should terminate with the return instruction to restore original program parameters. The interrupt-vector locations, device assignment, enabling-mask value, and the interrupt code are shown in Table 1.

TABLE 1
INTERRUPT LEVEL DATA

Interrupt Level	Vector Location (Memory Address In Hex)	Device Assignment	Interrupt Mask Values To Enable Respective Interrupts (ST12 thru ST15)	Interrupt Codes IC0 thru IC3
(Highest priority) 0	00	Reset	0 through F*	0000
1	04	External device	1 through F	0001
2	08		2 through F	0010
3	0C		3 through F	0011
4	10		4 through F	0100
5	14		5 through F	0101
6	18		6 through F	0110
7	1C		7 through F	0111
8	20		8 through F	1000
9	24		9 through F	1001
10	28		A through F	1010
11	2C		B through F	1011
12	30		C through F	1100
13	34		D through F	1101
14	38		E and F	1110
(Lowest priority) 15	3C	External device	F only	1111

*Level 0 can not be disabled.

The 9900 interrupt interface utilizes standard TTL components as shown in Figure 5. Note that for eight or less external interrupts a single SN54/74148 is required and for one external interrupt $\overline{\text{INTREQ}}$ is used as the interrupt signal with a hard-wired code IC0 through IC3.

2.3 I/O INTERFACE COMMUNICATIONS-REGISTER-UNIT (CRU)

The SBP 9900A communications-register-unit (CRU) is a versatile, direct command-driven serial I/O interface. The CRU may directly address, in bit-fields of one to sixteen, up to 4096 peripheral input bits and up to 4096 peripheral output bits. The SBP 9900A executes three single-bit and two multiple-bit CRU instructions. The single-bit instructions include TEST BIT (TB), SET BIT TO ONE (SBO), and SET BIT TO ZERO (SBZ); the multiple-bit instructions include LOAD CRU (LDCR) and STORE CRU (STCR).

The SBP 9900A employs three dedicated I/O signals CRUIN, CRUOUT, CRUCLK, and the least significant twelve bits of the address bus to support the CRU interface. CRU interface timing is shown in Section 2.9.

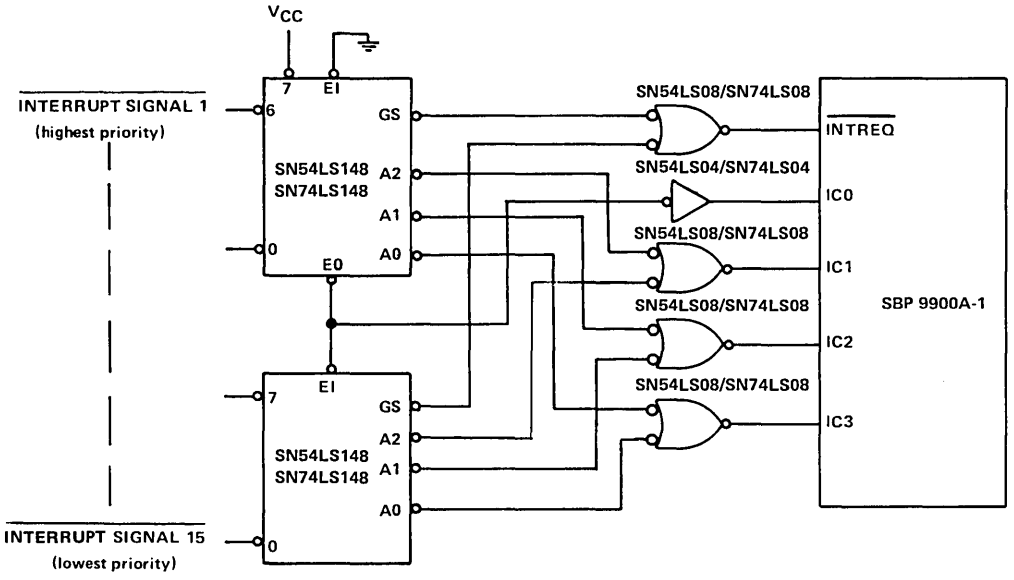


FIGURE 5 – SBP 9900A-1 INTERRUPT INTERFACE

2.4 SINGLE-BIT CRU OPERATIONS

The 9900 performs three single-bit CRU functions: test bit (TB), set bit to one (SBO), and set bit to zero (SBZ). To identify the bit to be operated upon, the 9900 develops a CRU-bit address and places it on the address bus, A3 to A14.

For the two output operations (SBO and SBZ), the processor also generates a CRUCLK pulse, indicating an output operation to the CRU device, and places bit 7 of the instruction word on the CRUOUT line to accomplish the specified operation (bit 7 is a one for SBO and a zero for SBZ). A test-bit instruction transfers the addressed CRU bit from the CRUIN input line to bit 2 of the status register (EQUAL).

The 9900 develops a CRU-bit address for the single-bit operations from the CRU-base address contained in workspace register 12 and the signed displacement count contained in bits 8 through 15 of the instruction. The displacement allows two's complement addressing from base minus 128 bits through base plus 127 bits. The base address from W12 is added to the signed displacement specified in the instruction and the result is loaded onto the address bus. Figure 6 illustrates the development of a single-bit CRU address.

2.5 MULTIPLE-BIT CRU OPERATIONS

The 9900 performs two multiple-bit CRU operations: store communications register (STCR) and load communications register (LDCR). Both operations perform a data transfer from the CRU-to-memory or from memory-to-CRU as illustrated in Figure 8. Although the figure illustrates a full 16-bit transfer operation, any number of bits from 1 through 16 may be involved. The LDCR instruction fetches a word from memory and right-shifts it to serially transfer it to CRU output bits. If the LDCR involves eight or fewer bits, those bits come from the right-justified field within the addressed byte of the memory word. If the LDCR involves nine or more bits, those bits come from the right-justified field within the whole memory word. When transferred to the CRU interface, each successive bit receives an address that is sequentially greater than the address for the previous bit. This addressing mechanism results

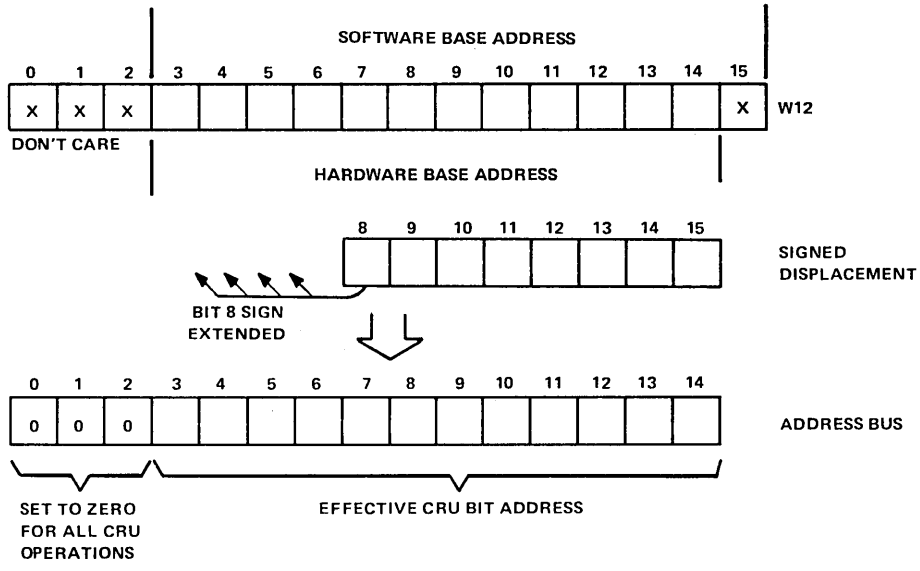


FIGURE 6 – 9900 SINGLE-BIT CRU ADDRESS DEVELOPMENT

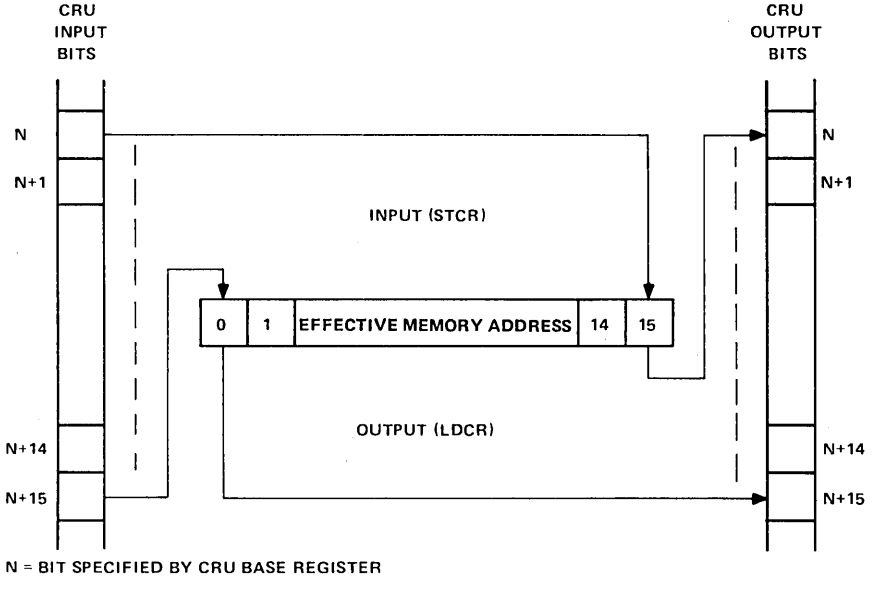


FIGURE 7 – 9900 LDCR/STCR DATA TRANSFERS

in an order reversal of the bits; that is, bit 15 of the memory word (or bit 7) becomes the lowest addressed bit in the CRU and bit 0 becomes the highest addressed bit in the CRU field.

An STCR instruction transfers data from the CRU to memory. If the operation involves a byte or less transfer, the transferred data will be stored right-justified in the memory byte with leading bits set to zero. If the operation involves from nine to 16 bits, the transferred data is stored right-justified in the memory word with leading bits set to

zero. When the input from the CRU device is complete, the first bit from the CRU is the least-significant-bit position in the memory word or byte.

Figure 8 illustrates how to implement a 16-bit input and a 16-bit output register in the CRU interface. CRU addresses are decoded as needed to implement up to 256 such 16-bit interface registers. In system application, however, only the exact number of interface bits needed to interface specific peripheral devices are implemented. It is not necessary to have a 16-bit interface register to interface an 8-bit device.

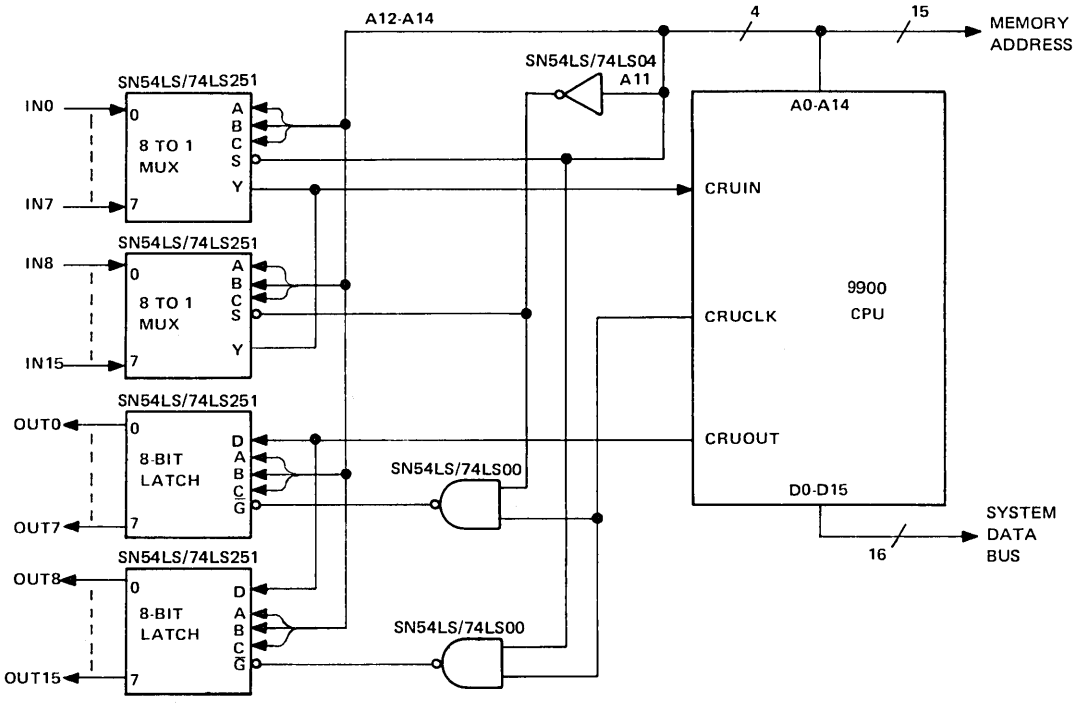


FIGURE 8 – 9900 16-BIT INPUT/OUTPUT INTERFACE

2.6 EXTERNAL INSTRUCTIONS

The 9900 has five external instructions that allow user-defined external functions to be initiated under program control. These instructions are CKON, CKOF, RSET, IDLE, and LREX. These mnemonics, except for IDLE, relate to functions implemented in the 990 minicomputer and do not restrict use of the instructions to initiate various user-defined functions. IDLE causes the 9900 to enter the idle state and remain until an interrupt, $\overline{\text{RESET}}$, or $\overline{\text{LOAD}}$ occurs. When any of these five instructions are executed by the 9900, a unique 3-bit code appears on the most-significant 3 bits of the address bus (A0 through A2) along with a CRUCLK pulse. When the 9900 is in an idle state, the 3-bit code and CRUCLK pulses occur repeatedly until the idle state is terminated. The codes are shown in Table 2.

Figure 9 illustrates typical external decode logic to implement these instructions. Note that a signal is generated to inhibit CRU decodes during external instructions.

TABLE 2
EXTERNAL INSTRUCTIONS

EXTERNAL INSTRUCTION	A0	A1	A2
LREX	H	H	H
CKOF	H	H	L
CKON	H	L	H
RSET	L	H	H
IDLE	L	H	L

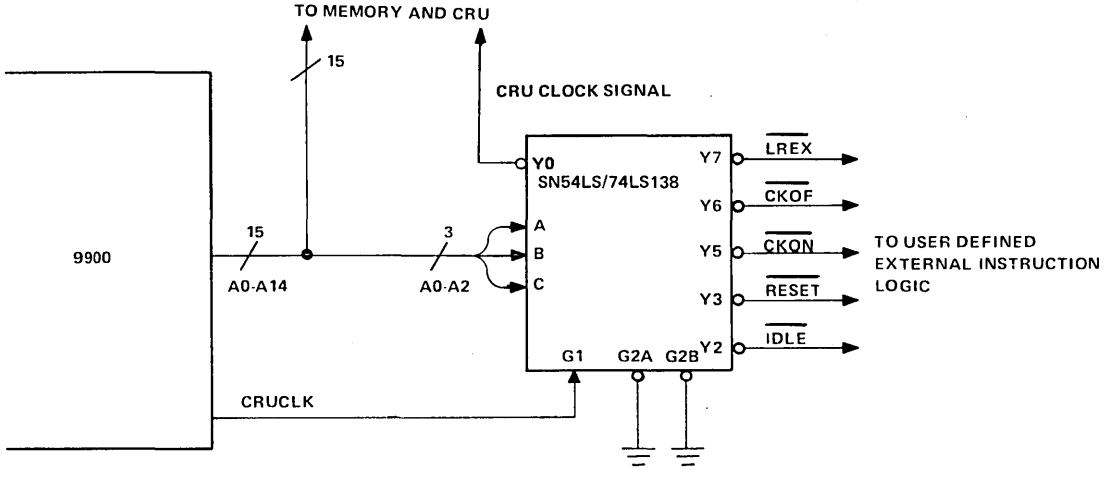


FIGURE 9 – EXTERNAL INSTRUCTION DECODE LOGIC

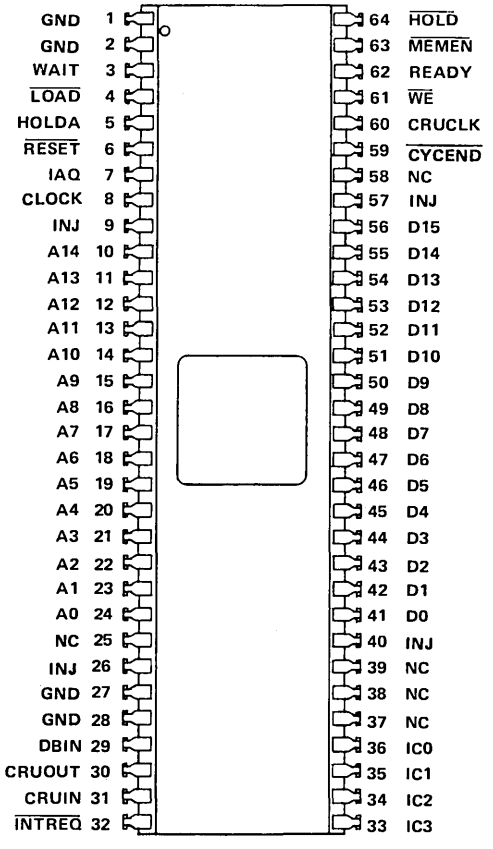
2.7 LOAD FUNCTION

The $\overline{\text{LOAD}}$ signal allows cold-start ROM loaders and front panels to be implemented for the 9900. When active, $\overline{\text{LOAD}}$ causes the 9900 to initiate an interrupt sequence immediately following the instruction being executed. Memory location FFFC is used to obtain the vector (WP and PC). The old PC, WP and ST are loaded into the new workspace and the interrupt mask is set to 0000. Then, program execution resumes using the new PC and WP.

2.8 SBP 9900A-1 PIN DESCRIPTION

TABLE 3
9900 PIN ASSIGNMENTS AND FUNCTIONS

SIGNATURE	PIN	I/O	DESCRIPTION
			ADDRESS BUS
A0 (MSB)	24	OUT	A0 (MSB) through A14 (LSB) comprise the address bus. This open-collector bus provides the memory-address vector to the external-memory system when $\overline{\text{MEMEN}}$ is active, and I/O-bit addresses to the I/O system when $\overline{\text{MEMEN}}$ is inactive. When HOLDA is active, the address bus is pulled to the logic level HIGH state by the individual pull-up resistors tied to each respective open-collector output.
A14 (LSB)	10	OUT	
			DATA BUS
D0 (MSB)	41	I/O	D0 (MSB) through D15 (LSB) comprise the bidirectional open-collector data bus. This bus transfers memory data to (when writing) and from (when reading) the external-memory system when $\overline{\text{MEMEN}}$ is active. When HOLDA is active, the data bus is pulled to the logic level HIGH state by the individual pull-up resistors tied to each respective open-collector output.
D15 (LSB)	56	I/O	
			POWER SUPPLY
INJ	9		Injector Supply Current
INJ	26		Injector Supply Current
INJ	40		Injector Supply Current
INJ	57		Injector Supply Current
GND	1		Ground Reference
GND	2		Ground Reference
GND	27		Ground Reference
GND	28		Ground Reference
			CLOCK
CLOCK	8	IN	CLOCK
			BUS CONTROL
DBIN	29	OUT	DATA BUS IN. When active (pulled to logic level HIGH), DBIN indicates that the SBP 9900 has disabled its output buffers to allow the memory to place memory-read data on the data bus during $\overline{\text{MEMEN}}$. DBIN remains at logic level LOW in all other cases except when HOLDA is active (pulled to logic level HIGH).
$\overline{\text{MEMEN}}$	63	OUT	MEMORY ENABLE. When active (logic level LOW), $\overline{\text{MEMEN}}$ indicates that the address bus contains a memory address.
$\overline{\text{WE}}$	61	OUT	WRITE ENABLE. When active (logic level LOW), $\overline{\text{WE}}$ indicates that the SBP 9900A data bus is outputting data to be written into memory.



NC—No internal connection

TABLE 3 (CONTINUED)

SIGNATURE	PIN	I/O	DESCRIPTION
CRUCLK	60	OUT	COMMUNICATIONS-REGISTER-UNIT (CRU) CLOCK. When active (pulled to logic level HIGH), CRUCLK indicates to the external interface logic the presence of output data on CRUOUT, or the presence of an encoded external instruction on A0 through A2.
CRUIN	31	IN	CRU DATA IN. CRUIN, normally driven by 3-state or open-collector devices, receives input data from the external interface logic. When the SBP 9900A executes a STCR or TB instruction, it samples CRUIN for the level of the CRU input bit specified by the address bus (A3 through A14).
CRUOUT	30	OUT	CRU DATA OUT. CRUOUT ouputs serial data when the SBP 9900A executes a LDCR, SBZ, SBO instruction. The data on CRUOUT should be sampled by the external interface logic when CRUCLK goes active (pulled to logic level HIGH).
			INTERRUPT CONTROL
$\overline{\text{INTREQ}}$	32	IN	INTERRUPT REQUEST. When active (logic level LOW), $\overline{\text{INTREQ}}$ indicates that an external interrupt is requesting service. If $\overline{\text{INTREQ}}$ is active, the SBP 9900A loads the data on the interrupt-code input lines IC0 through IC3 into the internal interrupt-code storage register. The code is then compared to the interrupt mask bits of the status register. If equal or higher priority than the enabled interrupt level (interrupt code equal or less than status register bits 12 through 15), the SBP 9900A initiates the interrupt sequence. If the comparison fails, the SBP 9900A ignores the interrupt request. In that case, $\overline{\text{INTREQ}}$ should be held active. The SBP 9900A will continue to sample IC0 through IC3 until the program enables a sufficiently low interrupt level to accept the requesting interrupt.
IC0 (MSB) ↓ IC3 (LSB)	36 ↓ 33	IN ↓ IN	INTERRUPT CODES. IC0 (MSB) through IC3 (LSB), receiving an interrupt identity code, are sampled by the SBP 9900A when $\overline{\text{INTREQ}}$ is active (logic level LOW). When IC0 through IC3 are LLLH, the highest priority *external* interrupt is requesting service; when HHHH, the lowest priority external interrupt is requesting service.
			MEMORY CONTROL
$\overline{\text{HOLD}}$	64	IN	When active (logic level LOW), $\overline{\text{HOLD}}$ indicates to the SBP 9900A that an external controller (e.g., DMA device) desires to use both the address bus and data bus to transfer data to or from memory. In response, the SBP 9900A enters the hold state after completion of its present memory cycle. The SBP 9900A then allows its address bus, data bus, $\overline{\text{WE}}$, $\overline{\text{MEMEN}}$, DBIN, and HOLDA facilities to be pulled to the logic level HIGH state. When $\overline{\text{HOLD}}$ is deactivated, the SBP 9900A returns to normal operation from the point at which it was stopped.
HOLDA	5	OUT	HOLD ACKNOWLEDGE. When active (pulled to logic level HIGH), HOLDA indicates that the SBP 9900A is in the hold state and that its address bus, data bus, $\overline{\text{WE}}$, $\overline{\text{MEMEN}}$, and DBIN facilities are pulled to the logic level HIGH state.
READY	62	IN	When active (logic level HIGH), READY indicates that the memory will be ready to read or write during the next clock cycle. When not-ready is indicated during a memory operation, the SBP 9900A enters a wait state and suspends internal operation until the memory systems activate READY.
WAIT	3	OUT	When active (pulled to logic level HIGH), WAIT indicates that the SBP 9900A has entered a wait state in response to a not-ready condition from memory.
			TIMING AND CONTROL
IAQ	7	OUT	INSTRUCTION ACQUISITION. IAQ is active (pulled to logic level HIGH) during any SBP 9900A initiated instruction acquisition memory cycle. Consequently, IAQ may be used to facilitate detection of illegal op codes.
$\overline{\text{CYCEND}}$	59	OUT	CYCLE END. When active (logic level LOW), $\overline{\text{CYCEND}}$ indicates that the SBP 9900A will ihitiate a new machine cycle on the low-to-high transition of the next CLOCK.
$\overline{\text{LOAD}}$	4	IN	When active (logic level LOW), $\overline{\text{LOAD}}$ causes the SBP 9900A to execute a nonmaskable interrupt with memory addresses FFFC_{16} and FFFE_{16} containing the associated trap vectors (WP and PC). The load sequence is initiated after the instruction being executed is completed. $\overline{\text{LOAD}}$ will also terminate an idle state. If $\overline{\text{LOAD}}$ is active during the time $\overline{\text{RESET}}$ is active, the $\overline{\text{LOAD}}$ trap will occur after the $\overline{\text{RESET}}$ function is completed. $\overline{\text{LOAD}}$ should remain active for one instruction execution period (IAQ may be

TABLE 3 (CONCLUDED)

SIGNATURE	PIN	I/O	DESCRIPTION
$\overline{\text{LOAD}}$ (Cont.)			used to monitor instruction boundaries). $\overline{\text{LOAD}}$ may be used to implement cold-start ROM loaders. Additionally, front-panel routines may be implemented using CRU bits as front-panel-interface signals, and software-control routines to direct the panel operations.
$\overline{\text{RESET}}$	6	IN	When active (logic level LOW), $\overline{\text{RESET}}$ causes the SBP 9900A to reset itself and inhibit $\overline{\text{WE}}$ and CRUCLK. When $\overline{\text{RESET}}$ is released, the SBP 9900A initiates a level-zero interrupt sequence acquiring the WP and PC trap vectors from memory locations 0000_{16} and 0002_{16}, sets all status register bits to logic level LOW, and then fetches the first instruction of the reset program environment. $\overline{\text{RESET}}$ must be held active for a minimum of three CLOCK cycles.

2.9 SBP 9900A-1 TIMING

2.9.1 SBP 9900A-1 MEMORY

The SBP 9900A basic memory timing for a memory-read cycle with no wait states and for a memory-write cycle with one wait state is as shown in Figure 10. During each memory-read or memory-write, $\overline{\text{MEMEN}}$ becomes active (logic level LOW) along with valid memory-address data appearing on the address bus (A0 through A14).

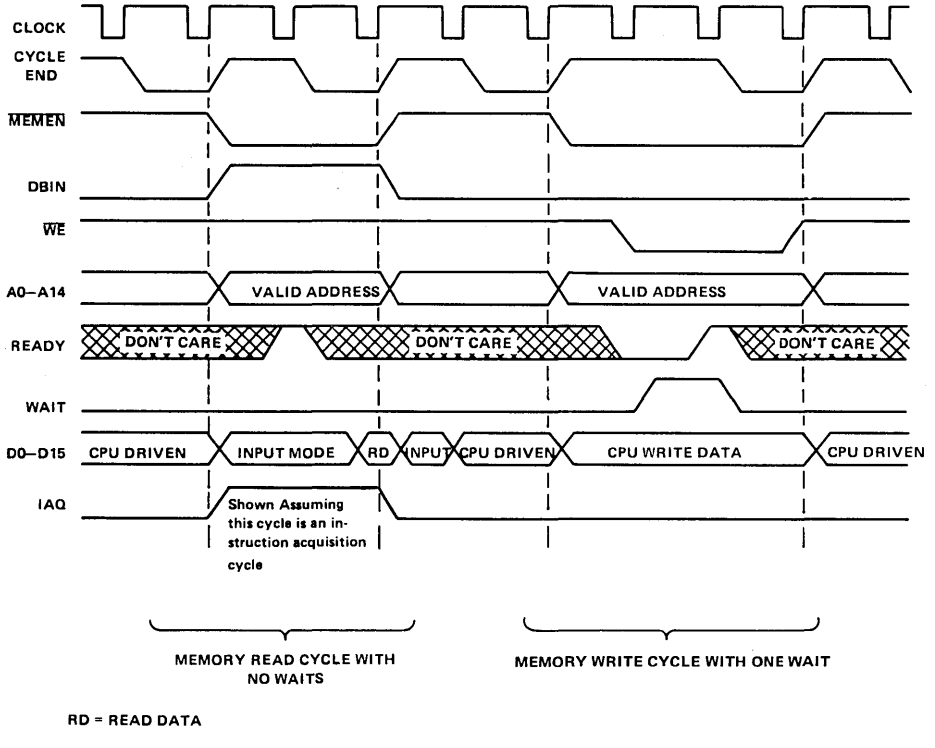


FIGURE 10 – SBP 9900A-1 MEMORY BUS TIMING

In the case of a memory-read cycle, DBIN becomes active (pulled to logic level HIGH) at the same time memory-address data becomes valid; the memory write strobe $\overline{WE}$ remains inactive (pulled to logic level HIGH). If the memory-read cycle is initiated for acquisition of an instruction, IAQ becomes active (pulled to logic level HIGH) at the same time $\overline{MEMEN}$ becomes active. At the end of a memory-read cycle, $\overline{MEMEN}$ and DBIN together become inactive. At that time, though the address may change, the data bus remains in the input mode until terminated by the next high-to-low transition of the clock.

In the case of a memory-write cycle, $\overline{WE}$ becomes active (logic level LOW) with the first high-to-low transition of the clock after $\overline{MEMEN}$ becomes active; DBIN remains inactive. At the end of a memory-write cycle, $\overline{WE}$ and $\overline{MEMEN}$ together become inactive.

During either a memory-read or a memory-write operation, READY may be used to extend the duration of the associated memory cycle such that the speed of the memory system may be coordinated with the speed of the SBP 9900. If READY is inactive (logic level LOW) during the first low-to-high transition of the clock after $\overline{MEMEN}$ becomes active, the SBP 9900A will enter a wait state suspending further progress of the memory cycle. The first low-to-high transistion of the clock after READY becomes active terminates the wait state and allows normal completion of the memory cycle.

2.9.2 SBP 9900A-1 HOLD

The hold facilities allow both the SBP 9900A and external devices to share a common memory. To gain memory-bus control, an external device requiring direct memory access (DMA) sends a hold request ($\overline{HOLD}$) to the SBP 9900A. When the next available non-memory cycle occurs, the SBP 9900A enters a hold state and signals its surrender of the memory-bus to the external device via a hold acknowledge (HOLDA). Receiving the hold acknowledgement, the external device proceeds to utilize the common memory. After its memory requirements have been satisfied, the external device returns memory-bus control to the SBP 9900A by releasing $\overline{HOLD}$.

When $\overline{HOLD}$ becomes active (logic level LOW), the SBP 9900A enters a hold state at the beginning of the next available non-memory cycle as shown in Figure 11. Upon entering a hold state, HOLDA becomes active (pulled to logic level HIGH) with the following signals pulled to a HIGH logic level by the individual pull-up resistors tied to each respective open-collector output: DBIN, $\overline{MEMEN}$, $\overline{WE}$, A0 through A14, and D0 through D15. When $\overline{HOLD}$ becomes inactive, the SBP 9900A exits the hold state and regains memory-bus control. If $\overline{HOLD}$ becomes active during a CRU operation, the SBP 9900A uses an extra clock cycle after the deactivation of $\overline{HOLD}$ to reassert the CRU address thereby providing the normal setup time for the CRU-bit transfer.

2.9.3 SBP 9900A-1 CRU

The transfer of two data-bits from memory to a peripheral CRU device and the transfer of one data-bit from a peripheral CRU device memory are shown in Figure 12. To transfer a data-bit to a peripheral CRU device, the SBP 9900A outputs the corresponding CRU-bit-address on address bus bits A3 through A14 and the respective data-bit on CRUOUT. During the second clock cycle of the operation, the SBP 9900A outputs a pulse, on CRUCLK, indicating to the peripheral CRU device the presence of a data-bit. This process is repeated until transfer of the entire field of data-bits specified by the CRU instruction has been accomplished. To transfer a data-bit from a peripheral CRU device, the SBP 9900A outputs the corresponding CRU-bit-address on address bus bits A3 through A14 and receives the respective data-bit on CRUIN. No CRUCLK pulses occur during a CRU input operation.

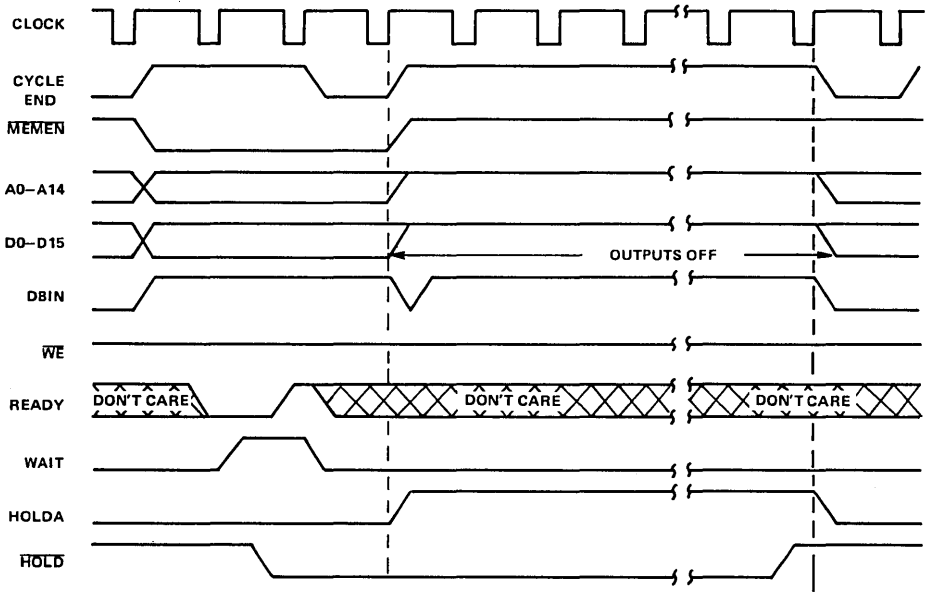


FIGURE 11 – SBP 9900A-1 HOLD TIMING

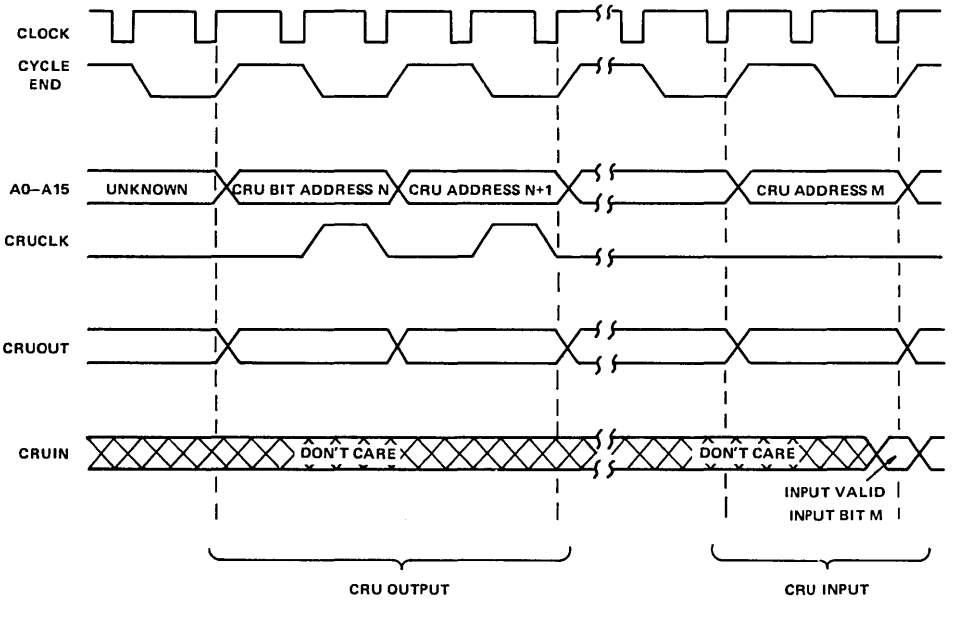


FIGURE 12 – SBP 9900A-1 CRU INTERFACE TIMING

3. 9900 INSTRUCTION SET

3.1 DEFINITION

Each 9900 instruction performs one of the following operations:

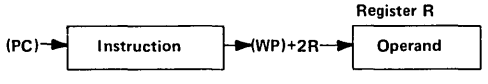
- Arithmetic, logical, comparison, or manipulation operations on data
- Loading or storage of internal registers (program counter, workspace pointer, or status)
- Data transfer between memory and external devices via the CRU
- Control functions.

3.2 ADDRESSING MODES

The 9900 instructions contain a variety of available modes for addressing random-memory data (e.g., program parameters and flags), or formatted memory data (character strings, data lists, etc.). The following figures graphically describe the derivation of the effective address for each addressing mode. The applicability of addressing modes to particular instructions is described in Section 3.5 along with the description of the operations performed by the instruction. The symbols following the names of the addressing modes [R, *R, *R+, @ LABEL, or @ TABLE (R)] are the general forms used by 9900 assemblers to select the addressing mode for register R.

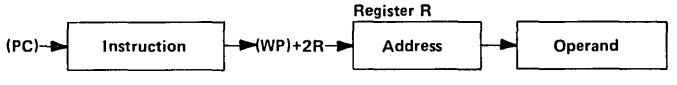
3.2.1 WORKSPACE REGISTER ADDRESSING R

Workspace Register R contains the operand.



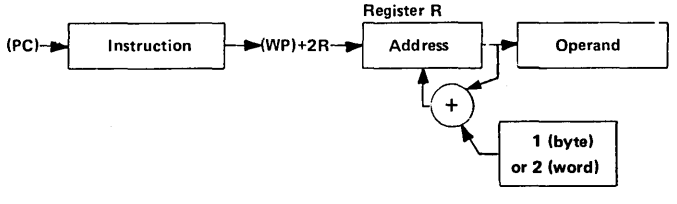
3.2.2 WORKSPACE REGISTER INDIRECT ADDRESSING *R

Workspace Register R contains the address of the operand.



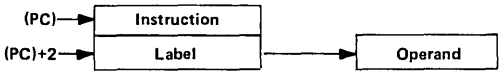
3.2.3 WORKSPACE REGISTER INDIRECT AUTO INCREMENT ADDRESSING *R+

Workspace Register R contains the address of the operand. After acquiring the operand, the contents of workspace register R are incremented.



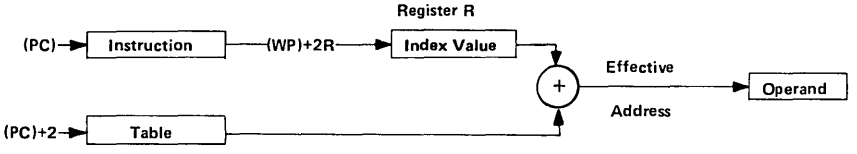
3.2.4 SYMBOLIC (DIRECT) ADDRESSING @ LABEL

The word following the instruction contains the address of the operand.



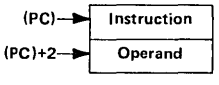
3.2.5 INDEXED ADDRESSING @ TABLE (R)

The word following the instruction contains the base address. Workspace register R contains the index value. The sum of the base address and the index value results in the effective address of the operand.



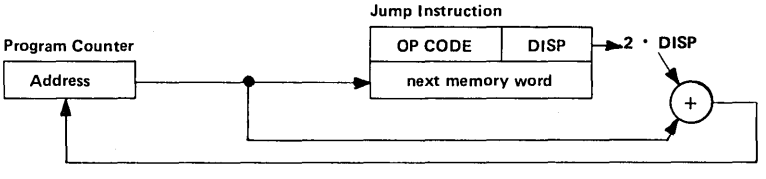
3.2.6 IMMEDIATE ADDRESSING

The word following the instruction contains the operand.



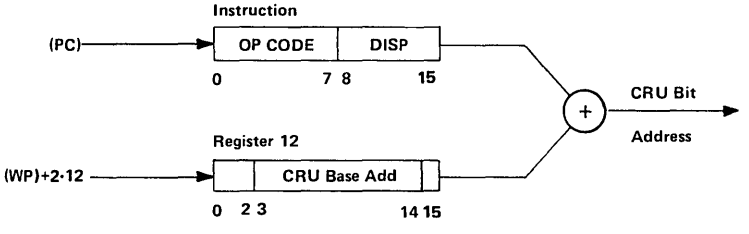
3.2.7 PROGRAM COUNTER RELATIVE ADDRESSING

The 8-bit signed displacement in the right byte (bits 8 through 15) of the instruction is multiplied by 2 and added to the updated contents of the program counter. The result is placed in the PC.



3.2.8 CRU RELATIVE ADDRESSING

The 8-bit signed displacement in the right byte of the instruction is added to the CRU base address (bits 3 through 14 of the workspace register 12). The result is the CRU address of the selected CRU bit.



3.3 TERMS AND DEFINITIONS

The terms used in describing the instructions of the 9900 are defined in Table 4.

TABLE 4
TERM DEFINITIONS

TERM	DEFINITION
B	Byte indicator (1=byte, 0 = word)
C	Bit count
D	Destination address register
DA	Destination address
IOP	Immediate operand
LSB(n)	Least significant (right most) bit of (n)
MSB(n)	Most significant (left most) bit of (n)
N	Don't care
PC	Program counter
Result	Result of operation performed by instruction
S	Source address register
SA	Source address
ST	Status register
STn	Bit n of status register
T_D	Destination address modifier
T_S	Source address modifier
WR	Workspace register (working register)
WRn	Workspace register n
(n)	Contents of n
a → b	a is transferred to b
|n|	Absolute value of n
+	Arithmetic addition
–	Arithmetic subtraction
AND	Logical AND
OR	Logical OR
⊕	Logical exclusive OR
$\overline{n}$	Logical complement of n

3.4 STATUS REGISTER

The status register contains the interrupt mask level and information pertaining to the instruction operation. Table 5 explains the bit indications.

0	1	2	3	4	5	6	7 8 9 10 11	12 13 14 15
ST0	ST1	ST2	ST3	ST4	ST5	ST6	not used (=0)	ST12 ST13 ST14 ST15
L>	A>	=	C	O	P	X		Interrupt Mask

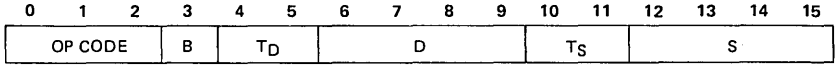
TABLE 5
STATUS REGISTER BIT DEFINITIONS

BIT	NAME	INSTRUCTION	CONDITION TO SET BIT TO 1
ST0	LOGICAL GREATER THAN	C,CB	If MSB(SA) = 1 and MSB(DA) = 0, or if MSB(SA) = MSB(DA) and MSB of [(DA)-(SA)] = 1
		CI	If MSB(WR) = 1 and MSB of IOP = 0, or if MSB(WR) = MSB of IOP and MSB of [IOP-(WR)] = 1
		ABS	If (SA) ≠ 0
		All Others	If result ≠ 0
ST1	ARITHMETIC GREATER THAN	C,CB	If MSB(SA) = 0 and MSB(DA) = 1, or if MSB(SA) = MSB(DA) and MSB of [(DA)-(SA)] = 1
		CI	If MSB(WR) = 0 and MSB of IOP = 1, or if MSB(WR) = MSB of IOP and MSB of [IOP-(WR)] = 1
		ABS	If MSB(SA) = 0 and (SA) ≠ 0
		All Others	If MSB of result = 0 and result ≠ 0
ST2	EQUAL	C, CB	If (SA) = (DA)
		C1	If (WR) = IOP
		COC	If (SA) and $(\overline{DA})$ = 0
		CZC	If (SA) and (DA) = 0
		TB	If CRUIN = 1
		ABS	If (SA) = 0
		All Others	If result = 0
ST3	CARRY	A, AB, ABS, AI, DEC, DECT, INC, INCT, NEG, S, SB	If CARRY OUT = 1
		SLA, SRA, SRC, SRL	If last bit shifted out = 1
ST4	OVERFLOW	A, AB	If MSB(SA) = MSB(DA) and MSB of result ≠ MSB(DA)
		AI	If MSB(WR) = MSB of IOP and MSB of result ≠ MSB(WR)
		S, SB	If MSB(SA) ≠ MSB(DA) and MSB of result ≠ MSB(DA)
		DEC, DECT	If MSB(SA) = 1 and MSB of result = 0
		INC, INCT	If MSB(SA) = 0 and MSB of result = 1
		SLA	If MSB changes during shift
		DIV	If MSB(SA) = 0 and MSB(DA) = 1, or if MSB(SA) = MSB(DA) and MSB of [(DA)-(SA)] = 0
		ABS, NEG	If (SA) = 8000_{16}
ST5	PARITY	CB, MOVB	If (SA) has odd number of 1's
		LDCR, STCR	If 1 ⩽ C ⩽ 8 and (SA) has odd number of 1's
		AB, SB, SOCB, SZCB	If result has odd number of 1's
ST6	XOP	XOP	If XOP instruction is executed
ST12–ST15	INTERRUPT MASK	LIMI	If corresponding bit of IOP is 1
		RTWP	If corresponding bit of WR15 is 1

3.5 INSTRUCTIONS

3.5.1 Dual Operand Instructions with Multiple Addressing Modes for Source and Destination Operand

General format:



If B = 1 the operands are bytes and the operand addresses are byte addresses. If B = 0 the operands are words and the operand addresses are word addresses.

The addressing mode for each operand is determined by the T field of that operand.

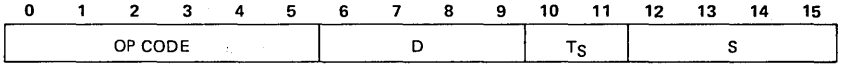
T_S OR T_D	S OR D	ADDRESSING MODE	NOTES
00	0, 1, . . . 15	Workspace register	1
01	0, 1, . . . 15	Workspace register indirect	
10	0	Symbolic	4
10	1, 2, . . . 15	Indexed	2,4
11	0, 1, . . . 15	Workspace register indirect auto-increment	3

NOTES: 1. When a workspace register is the operand of a byte instruction (bit 3 = 1), the left byte (bits 0 through 7) is the operand and the right byte (bits 8 through 15) is unchanged.
2. Workspace register 0 may not be used for indexing.
3. The workspace register is incremented by 1 for byte instructions (bit 3 = 1) and is incremented by 2 for word instructions (bit 3 = 0).
4. When $T_S = T_D = 10$, two words are required in addition to the instruction word. The first word is the source operand base address and the second word is the destination operand base address.

MNEMONIC	OP CODE 0 1 2	B 3	MEANING	RESULT COMPARED TO 0	STATUS BITS AFFECTED	DESCRIPTION
A	1 0 1	0	Add	Yes	0-4	(SA)+(DA) → (DA)
AB	1 0 1	1	Add bytes	Yes	0-5	(SA)+(DA) → (DA)
C	1 0 0	0	Compare	No	0-2	Compare (SA) to (DA) and set appropriate status bits
CB	1 0 0	1	Compare bytes	No	0-2,5	Compare (SA) to (DA) and set appropriate status bits
S	0 1 1	0	Subtract	Yes	0-4	(DA) – (SA) → (DA)
SB	0 1 1	1	Subtract bytes	Yes	0-5	(DA) – (SA) → (DA)
SOC	1 1 1	0	Set ones corresponding	Yes	0-2	(DA) OR (SA) → (DA)
SOCB	1 1 1	1	Set ones corresponding bytes	Yes	0-2,5	(DA) OR (SA) → (DA)
SZC	0 1 0	0	Set zeroes corresponding	Yes	0-2	(DA) AND ($\overline{SA}$) → (DA)
SZCB	0 1 0	1	Set zeroes corresponding bytes	Yes	0-2,5	(DA) AND ($\overline{SA}$) → (DA)
MOV	1 1 0	0	Move	Yes	0-2	(SA) → (DA)
MOVB	1 1 0	1	Move bytes	Yes	0-2,5	(SA) → (DA)

3.5.2 Dual Operand Instructions with Multiple Addressing Modes for the Source Operand and Workspace Register Addressing for the Destination

General format:



The addressing mode for the source operand is determined by the T_S field.

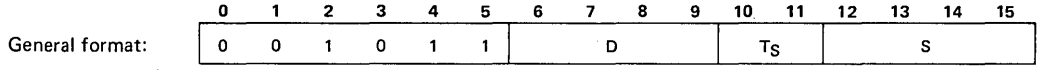
T_S	S	ADDRESSING MODE	NOTES
00	0, 1, . . . 15	Workspace register	
01	0, 1, . . . 15	Workspace register indirect	
10	0	Symbolic	
10	1, 2, . . . 15	Indexed	1
11	0, 1, . . . 15	Workspace register indirect auto increment	2

NOTES: 1. Workspace register 0 may not be used for indexing.
2. The workspace register is incremented by 2.

MNEMONIC	OP CODE 0 1 2 3 4 5	MEANING	RESULT COMPARED TO 0	STATUS BITS AFFECTED	DESCRIPTION
COC	0 0 1 0 0 0	Compare ones corresponding	No	2	Test (D) to determine if 1's are in each bit position where 1's are in (SA). If so, set ST2.
CZC	0 0 1 0 0 1	Compare zeros corresponding	No	2	Test (D) to determine if 0's are in each bit position where 1's are in (SA). If so, set ST2.
XOR	0 0 1 0 1 0	Exclusive OR	Yes	0-2	(D) ⊕ (SA) → (D)
MPY	0 0 1 1 1 0	Multiply	No		Multiply unsigned (D) by unsigned (SA) and place unsigned 32-bit product in D (most significant) and D+1 (least significant). If WR15 is D, the next word in memory after WR15 will be used for the least significant half of the product.
DIV	0 0 1 1 1 1	Divide	No	4	If unsigned (SA) is less than or equal to unsigned (D), perform no operation and set ST4. Otherwise, divide unsigned (D) and (D+1) by unsigned (SA). Quotient → (D), remainder → (D+1). If D = 15, the next word in memory after WR 15 will be used for the remainder.

4

3.5.3 Extended Operation (XOP) Instruction

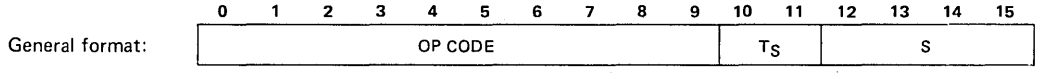


The T_S and S fields provide multiple mode addressing capability for the source operand. When the XOP is executed, ST6 is set and the following transfers occur:

$(40_{16} + 4D) \rightarrow$ (WP)
$(42_{16} + 4D) \rightarrow$ (PC)
SA → (new WR11)
(old WP) → (new WR13)
(old PC) → (new WR14)
(old ST) → (new WR15)

The 9900 does not test interrupt requests ($\overline{\text{INTREQ}}$) upon completion of the XOP instruction.

3.5.4 Single Operand Instructions



The T_S and S fields provide multiple mode addressing capability for the source operand.

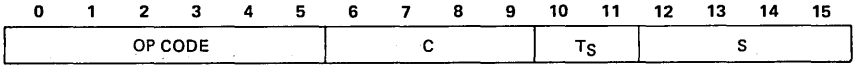
MNEMONIC	OP CODE 0 1 2 3 4 5 6 7 8 9	MEANING	RESULT COMPARED TO 0	STATUS BITS AFFECTED	DESCRIPTION
B	0 0 0 0 0 1 0 0 0 1	Branch	No	–	SA → (PC)
BL	0 0 0 0 0 1 1 0 1 0	Branch and link	No	–	(PC) → (WR11); SA → (PC)
BLWP	0 0 0 0 0 1 0 0 0 0	Branch and load workspace pointer	No	–	(SA) → (WP); (SA+2) → (PC); (old WP) → (new WR13); (old PC) → (new WR14); (old ST) → (new WR15); the interrupt input ($\overline{\text{INTREQ}}$) is not tested upon completion of the BLWP instruction.
CLR	0 0 0 0 0 1 0 0 1 1	Clear operand	No	–	0 → (SA)
SETO	0 0 0 0 0 1 1 1 0 0	Set to ones	No	–	$FFFF_{16}$ → (SA)
INV	0 0 0 0 0 1 0 1 0 1	Invert	Yes	0-2	$(\overline{SA})$ → (SA)
NEG	0 0 0 0 0 1 0 1 0 0	Negate	Yes	0-4	–(SA) → (SA)
ABS	0 0 0 0 0 1 1 1 0 1	Absolute value*	No	0-4	|(SA)| → (SA)
SWPB	0 0 0 0 0 1 1 0 1 1	Swap bytes	No	–	(SA), bits 0 thru 7 → (SA), bits 8 thru 15; (SA), bits 8 thru 15 → (SA), bits 0 thru 7.
INC	0 0 0 0 0 1 0 1 1 0	Increment	Yes	0-4	(SA) + 1 → (SA)
INCT	0 0 0 0 0 1 0 1 1 1	Increment by two	Yes	0-4	(SA) + 2 → (SA)
DEC	0 0 0 0 0 1 1 0 0 0	Decrement	Yes	0-4	(SA) – 1 → (SA)
DECT	0 0 0 0 0 1 1 0 0 1	Decrement by two	Yes	0-4	(SA) – 2 → (SA)
X†	0 0 0 0 0 1 0 0 1 0	Execute	No	–	Execute the instruction at SA.

*Operand is compared to zero for status bit.

†If additional memory words for the execute instruction are required to define the operands of the instruction located at SA, these words will be accessed from PC and the PC will be updated accordingly. The instruction acquisition signal (IAQ) will not be true when the 9900 accesses the instruction at SA. Status bits are affected in the normal manner for the instruction executed.

3.5.5 CRU Multiple-Bit Instructions

General format:

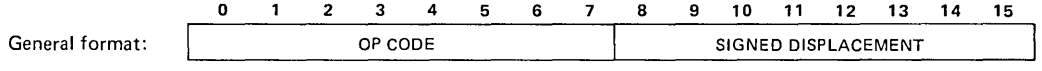


The C field specifies the number of bits to be transferred. If C = 0, 16 bits will be transferred. The CRU base register (WR12, bits 3 through 14) defines the starting CRU bit address. The bits are transferred serially and the CRU address is incremented with each bit transfer, although the contents of WR12 is not affected. T_S and S provide multiple mode addressing capability for the source operand. If 8 or fewer bits are transferred (C = 1 through 8), the source address is a byte address. If 9 or more bits are transferred (C = 0, 9 through 15), the source address is a word address. If the source is addressed in the workspace register indirect auto increment mode, the workspace register is incremented by 1 if C = 1 through 8, and is incremented by 2 otherwise.

MNEMONIC	OP CODE 0 1 2 3 4 5	MEANING	RESULT COMPARED TO 0	STATUS BITS AFFECTED	DESCRIPTION
LDCR	0 0 1 1 0 0	Load communcation register	Yes	0-2,5†	Beginning with LSB of (SA), transfer the specified number of bits from (SA) to the CRU.
STCR	0 0 1 1 0 1	Store communcation register	Yes	0-2,5†	Beginning with LSB of (SA), transfer the specified number of bits from the CRU to (SA). Load unfilled bit positions with 0.

†ST5 is affected only if $1 \leqslant C \leqslant 8$.

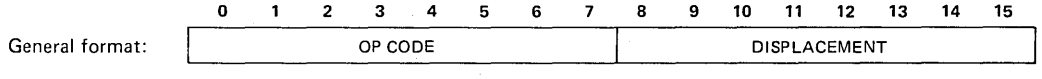
3.5.6 CRU Single-Bit Instructions



CRU relative addressing is used to address the selected CRU bit.

MNEMONIC	OP CODE 0 1 2 3 4 5 6 7	MEANING	STATUS BITS AFFECTED	DESCRIPTION
SBO	0 0 0 1 1 1 0 1	Set bit to one	—	Set the selected CRU output bit to 1.
SBZ	0 0 0 1 1 1 1 0	Set bit to zero	—	Set the selected CRU output bit to 0.
TB	0 0 0 1 1 1 1 1	Test bit	2	If the selected CRU input bit = 1, set ST2.

3.5.7 Jump Instructions

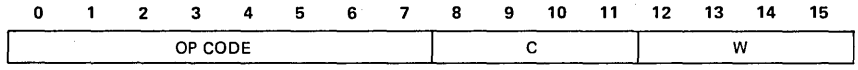


Jump instructions cause the PC to be loaded with the value selected by PC relative addressing if the bits of ST are at specified values. Otherwise, no operation occurs and the next instruction is executed since PC points to the next instruction. The displacement field is a word count to be added to PC. Thus, the jump instruction has a range of −128 to 127 words from memory-word address following the jump instruction. No ST bits are affected by jump instruction.

MNEMONIC	OP CODE 0 1 2 3 4 5 6 7	MEANING	ST CONDITION TO LOAD PC
JEQ	0 0 0 1 0 0 1 1	Jump equal	ST2 = 1
JGT	0 0 0 1 0 1 0 1	Jump greater than	ST1 = 1
JH	0 0 0 1 1 0 1 1	Jump high	ST0 = 1 and ST2 = 0
JHE	0 0 0 1 0 1 0 0	Jump high or equal	ST0 = 1 or ST2 = 1
JL	0 0 0 1 1 0 1 0	Jump low	ST0 = 0 and ST2 = 0
JLE	0 0 0 1 0 0 1 0	Jump low or equal	ST0 = 0 or ST2 = 1
JLT	0 0 0 1 0 0 0 1	Jump less than	ST1 = 0 and ST2 = 0
JMP	0 0 0 1 0 0 0 0	Jump unconditional	unconditional
JNC	0 0 0 1 0 1 1 1	Jump no carry	ST3 = 0
JNE	0 0 0 1 0 1 1 0	Jump not equal	ST2 = 0
JNO	0 0 0 1 1 0 0 1	Jump no overflow	ST4 = 0
JOC	0 0 0 1 1 0 0 0	Jump on carry	ST3 = 1
JOP	0 0 0 1 1 1 0 0	Jump odd parity	ST5 = 1

3.5.8 Shift Instructions

General format:

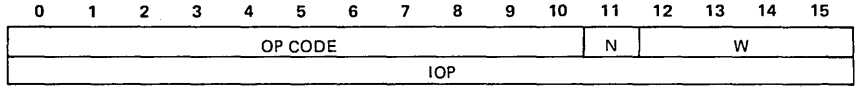


If C = 0, bits 12 through 15 of WR0 contain the shift count. If C = 0 and bits 12 through 15 of WR0 = 0, the shift count is 16.

MNEMONIC	OP CODE 0 1 2 3 4 5 6 7	MEANING	RESULT COMPARED TO 0	STATUS BITS AFFECTED	DESCRIPTION
SLA	0 0 0 0 1 0 1 0	Shift left arithmetic	Yes	0-4	Shift (WR) left. Fill vacated bit positions with 0.
SRA	0 0 0 0 1 0 0 0	Shift right arithmetic	Yes	0-3	Shift (WR) right. Fill vacated bit positions with original MSB of (WR).
SRC	0 0 0 0 1 0 1 1	Shift right circular	Yes	0-3	Shift (WR) right. Shift previous LSB into MSB.
SRL	0 0 0 0 1 0 0 1	Shift right logical	Yes	0-3	Shift (WR) right. Fill vacated bit positions with 0's.

3.5.9 Immediate Register Instructions

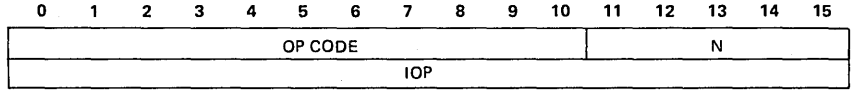
General format:



MNEMONIC	OP CODE 0 1 2 3 4 5 6 7 8 9 10	MEANING	RESULT COMPARED TO 0	STATUS BITS AFFECTED	DESCRIPTION
AI	0 0 0 0 0 0 1 0 0 0 1	Add immediate	Yes	0-4	(WR) + IOP → (WR)
ANDI	0 0 0 0 0 0 1 0 0 1 0	AND immediate	Yes	0-2	(WR) AND IOP → (WR)
CI	0 0 0 0 0 0 1 0 1 0 0	Compare immediate	Yes	0-2	Compare (W) to IOP and set appropriate status bits
LI	0 0 0 0 0 0 1 0 0 0 0	Load immediate	Yes	0-2	IOP → (WR)
ORI	0 0 0 0 0 0 1 0 0 1 1	OR immediate	Yes	0-2	(WR) OR IOP → (WR)

3.5.10 Internal Register Load Immediate Instructions

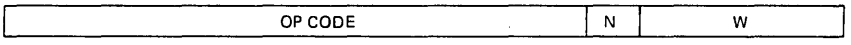
General format:



MNEMONIC	OP CODE 0 1 2 3 4 5 6 7 8 9 10	MEANING	DESCRIPTION
LWPI	0 0 0 0 0 0 1 0 1 1 1	Load workspace pointer immediate	IOP → (WP), no ST bits affected
LIMI	0 0 0 0 0 0 1 1 0 0 0	Load interrupt mask	IOP, bits 12 thru 15 → ST12 thru ST15

3.5.11 Internal Register Store Instructions

General format:

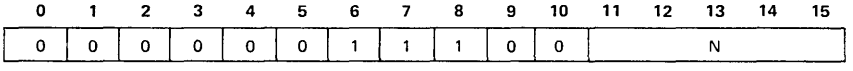


No ST bits are affected.

MNEMONIC	OP CODE 0 1 2 3 4 5 6 7 8 9 10	MEANING	DESCRIPTION
STST	0 0 0 0 0 0 1 0 1 1 0	Store status register	(ST) → (WR)
STWP	0 0 0 0 0 0 1 0 1 0 1	Store workspace pointer	(WP) → (WR)

3.5.12 Return Workspace Pointer (RTWP) Instruction

General format:

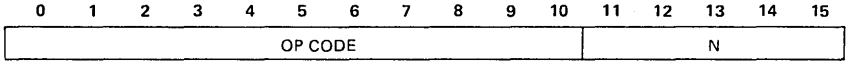


The RTWP instruction causes the following transfers to occur:

(WR15) → (ST)
(WR14) → (PC)
(WR13) → (WP)

3.5.13 External Instructions

General format:



External instructions cause the three most-significant address lines (A0 through A2) to be set to the below-described levels and the CRUCLK line to be pulsed, allowing external control functions to be initiated.

MNEMONIC	OP CODE 0 1 2 3 4 5 6 7 8 9 10	MEANING	STATUS BITS AFFECTED	DESCRIPTION	ADDRESS BUS A0	A1	A2
IDLE	0 0 0 0 0 0 1 1 0 1 0	Idle	–	Suspend SBP 9900A instruction execution until an interrupt, $\overline{\text{LOAD}}$, or $\overline{\text{RESET}}$ occurs	L	H	L
RSET	0 0 0 0 0 0 1 1 0 1 1	Reset	12–15	0 → ST12 thru ST15	L	H	H
CKOF	0 0 0 0 0 0 1 1 1 1 0	User defined		———	H	H	L
CKON	0 0 0 0 0 0 1 1 1 0 1	User defined		———	H	L	H
LREX	0 0 0 0 0 0 1 1 1 1 1	User defined		———	H	H	H

3.6 MICROINSTRUCTION CYCLE

The SBP 9900A includes circuitry which will indicate the completion of a microinstruction cycle. Designated as the $\overline{\text{CYCEND}}$ function, it provides CPU status that can simplify system design. The $\overline{\text{CYCEND}}$ output will go to a low logic level as a result of the low-to-high transistion of each clock pulse which initiates the last clock of a microinstruction.

3.7 SBP 9900A INSTRUCTION EXECUTION TIMES

Instruction execution times for the SBP 9900A are a function of:

1) Clock cycle time, t_c

2) Addressing mode used where operands have multiple addressing mode capability

3) Number of wait states required per memory access.

The following Table 6 lists the number of clock cycles and memory accesses required to execute each SBP 9900A instruction. For instructions with multiple addressing modes for either or both operands, the table lists the number of clock cycles and memory accesses with all operands addressed in the workspace-register mode. To determine the additional number of clock cycles and memory accesses required for modified addressing, add the appropriate values from the referenced tables. The total instruction-execution time for an instruction is:

$$T = t_c (C + W \cdot M)$$

where:

T = total instruction execution time;
t_c = clock cycle time;
C = number of clock cycles for instruction execution plus address modification;
W = number of required wait states per memory access for instruction execution plus address modification;
M = number of memory accesses.

As an example, the instruction MOVB is used in a system with $t_c = 0.5\ \mu s$ and no wait states are required to access memory. Both operands are addressed in the workspace register mode:

$$T = t_c (C + W \cdot M) = 0.5\ (14 + 0 \cdot 4)\ \mu s = 7\ \mu s.$$

If two wait states per memory access were required, the execution time is:

$$T = 0.5\ (14 + 2 \cdot 4)\ \mu s = 11\ \mu s.$$

If the source operand was addressed in the symbolic mode and two wait states were required:

$$T = t_c (C + W \cdot M)$$
$$C = 14 + 8 = 22$$
$$M = 4 + 1 = 5$$
$$T = 0.5\ (22 + 2 \cdot 5)\ \mu s = 16\ \mu s.$$

TABLE 6
INSTRUCTION EXECUTION TIMES

INSTRUCTION	CLOCK CYCLES C	MEMORY ACCESS M	ADDRESS MODIFICATION† SOURCE	ADDRESS MODIFICATION† DEST	INSTRUCTION	CLOCK CYCLES C	MEMORY ACCESS M	ADDRESS MODIFICATION† SOURCE	ADDRESS MODIFICATION† DEST
A	14	4	A	A	LWPI	10	2	–	–
AB	14	4	B	B	MOV	14	4	A	A
ABS (MSB = 0)	12	2	A	–	MOVB	14	4	B	B
(MSB = 1)	14	3	A	–	MPY	52	5	A	–
AI	14	4	–	–	NEG	12	3	A	–
ANDI	14	4	–	–	ORI	14	4	–	–
B	8	2	A	–	RSET	12	1	–	–
BL	12	3	A	–	RTWP	14	4	–	–
BLWP	26	6	A	–	S	14	4	A	A
C	14	3	A	A	SB	14	4	B	B
CB	14	3	B	B	SBO	12	2	–	–
CI	14	3	–	–	SBZ	12		–	–
CKOF	12	1	–	–	SETO	10	3	A	–
CKON	12	1	–	–	Shift (C ≠ 0)	12+2C	3	–	–
CLR	10	3	A	–	(C = 0, Bits 12–15				
COC	14	3	A	–	of WRO = 0)	52	4	–	–
CZC	14	3	A	–	(C = 0, Bits 12–15)				
DEC	10	3	A	–	of WRO = K ≠ 0)	20+2K	4	–	–
DECT	10	3	A	–	SOC	14	4	A	A
DIV (ST4 is set)	16	3	A	–	SOCB	14	4	B	B
DIV (ST4 is reset)*	92-124	6	A	–	STCR (C = 0)	60	4	A	–
IDLE	12	1	–	–	(1<C<7)	42	4	B	–
INC	10	3	A	–	(C = 8)	44	4	B	–
INCT	10	3	A	–	(9<C<15)	58	4	A	–
INV	10	3	A	–	STST	8	2	–	–
Jump (PC is changed)	10	1	–	–	STWP	8	2	–	–
(PC is not changed)	8	1	–	–	SWPB	10	3	A	–
LDCR (C = 0)	52	3	A	–	SZC	14	4	A	A
(1<C<8)	20+2C	3	B	–	SZCB	14	4	B	B
(9<C<15)	20+2C	3	A	–	TB	12	2	–	–
LI	12	3	–	–	X**	8	2	A	–
LIMI	14	2	–	–	XOP	36	8	A	–
LREX	12	1	–	–	XOR	14	4	A	–
RESET function	26	5	–	–	Undefined op codes:				
LOAD function	22	5	–	–	0000-01FF,0320-033F,0C00-0FFF,	6	1	–	–
Interrupt context switch	22	5	–	–	0780-07FF				

*Execution time is dependent upon the partial quotient after each clock cycle during execution.

**Execution time is added to the execution time of the instruction located at the source address minus 4 clock cycles and 1 memory access time.

†The letters A and B refer to the respective columns in the Address Modification Table.

ADDRESS MODIFICATION

ADDRESSING MODE	COLUMN A CLOCK CYCLES C	COLUMN A MEMORY ACCESSES M	COLUMN B CLOCK CYCLES C	COLUMN B MEMORY ACCESSES M
WR (T_S or T_D = 00)	0	0	0	0
WR indirect (T_S or T_D = 01)	4	1	4	1
WR indirect auto-increment (T_S or T_D = 11)	8	2	6	2
Symbolic (T_S or T_D = 10, S or D = 0)	8	1	8	1
Indexed (T_S or T_D = 10, S or D ≠ 0)	8	2	8	2

4. INTERFACING

The input/output (I/O) accommodations have been designed for TTL compatibility. Direct interfacing, supportable by the entire families of catalog devices, is shown in Figure 13.

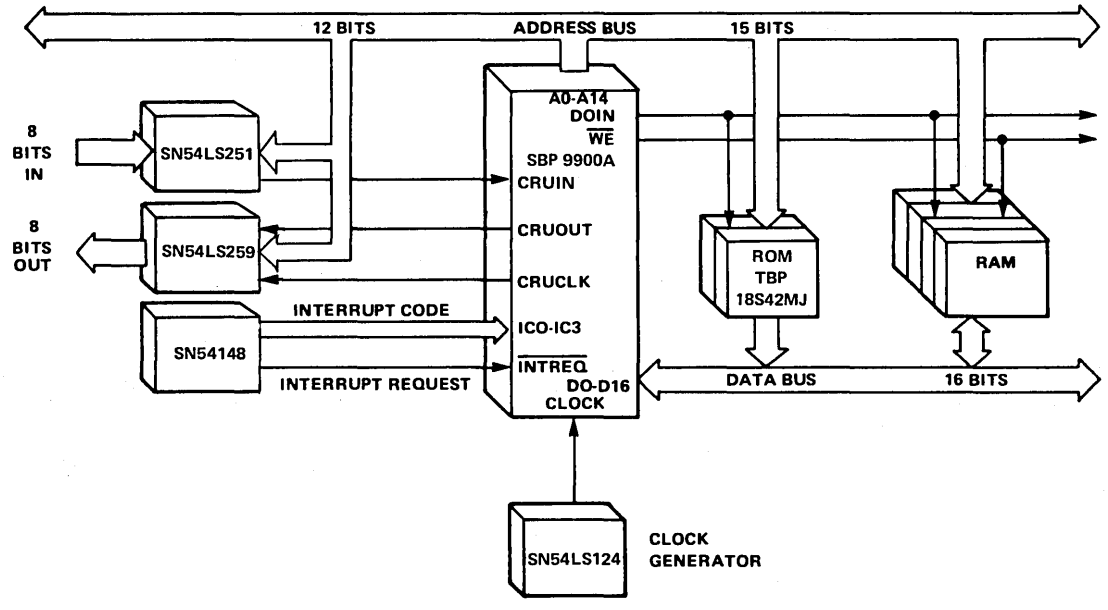


FIGURE 13 – MINIMUM SBP 9900A-1 SYSTEM

4.1 INPUT CIRCUIT

The input circuit used on the SBP 9900A is basically an RTL configuration which has been modified for TTL compatibility as shown in Figure 14. An input-clamping diode is incorporated to limit negative excursions (ringing) when the SBP 9900A is on the receiving end of a transmission line; and input switching threshold of nominally +1.5 volts has been specified for improved noise immunity. This threshold is achieved via two resistors which function as a voltage divider to increase the one V_{BE} threshold of the I^2L input transistor to +1.5 volts.

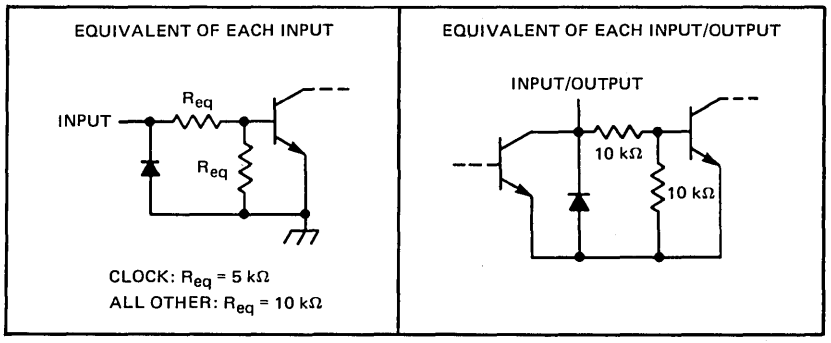


FIGURE 14 – SCHEMATICS OF INPUTS AND INPUT/OUTPUTS

The input circuit characteristics for input current versus input voltage are shown in Figure 15. The 10-kΩ and 20-kΩ load lines and threshold knee at +1.5 volts provide a high-impedance characteristic to reduce input loading and improve the low-logic-level input noise immunity over some standard TTL inputs. Full compatibility is maintained with virtually all 5-volt-logic families even when the SBP 9900A is powered down (injector current reduced).

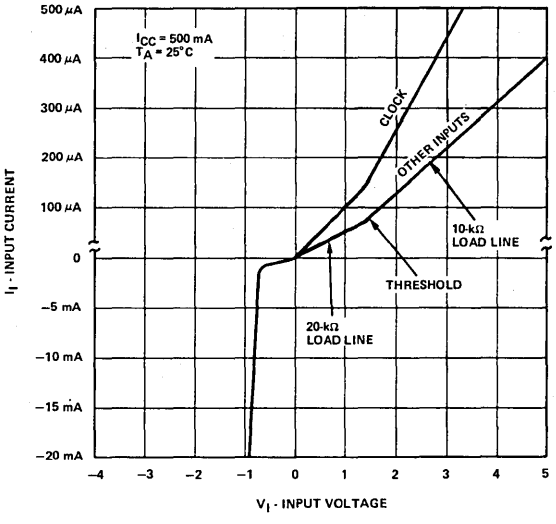


FIGURE 15 – TYPICAL INPUT CHARACTERISTICS

4.1.1 Sourcing Inputs

The inputs may be driven directly by most 5-volt-logic families. Functions that feature internal pull-up resistors at their outputs usually require no external interface components. Functions that feature open-collector outputs generally require external pull-up resistors.

4.1.2 Terminating Unused Inputs

Inputs that are selected to be hardwired to a logic-level low may be connected directly to ground. Inputs that are selected to be hardwired to a logic-level high must be tied, via a current limiting (pull-up) resistor, to a logic-level-high low-impedance voltage source such as V_{CC}. A single resistor common to all (N) inputs may be used for transient protection.

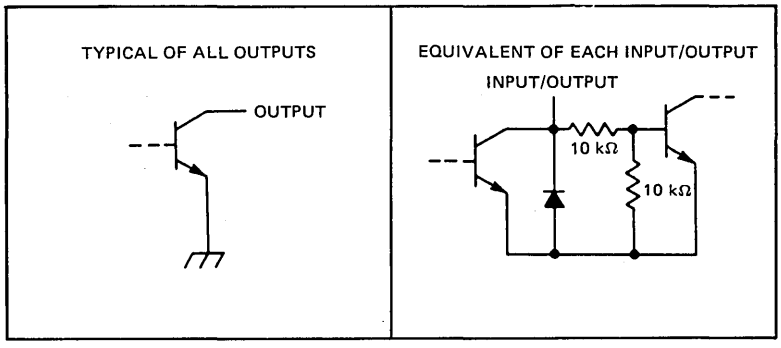


FIGURE 16 – SCHEMATICS OF OUTPUTS AND INPUT/OUTPUTS

4.2 OUTPUT CIRCUIT

The output circuit selected for the SBP 9900A is a current-injected, open-collector transistor shown in Figure 16. Since this transistor is current-injected, output sourcing capability is directly related to injector current. In other words, the number of loads that may be driven by an SBP 9900A output is directly reduced as injector current is reduced.

The output circuit characteristic for low-level output voltage (V_{OL}) versus low-level output current (I_{OL}) is shown in Figure 17. At rated injector current, the SBP 9900A output circuit offers a low-level output voltage of typically 220 mV.

The output circuit characteristics for 1) high-level output voltage (V_{OH}) and current (I_{OH}), 2) rise times, and 3) next stage input noise immunity, are a function of the load circuit being driven. The load circuit may be either:

A) the direct input of a five-volt logic family if no source current is required

or, for greater noise immunity and improved rise times,

B) the direct input of a five-volt logic family in conjunction with a discrete pull-up resistor.

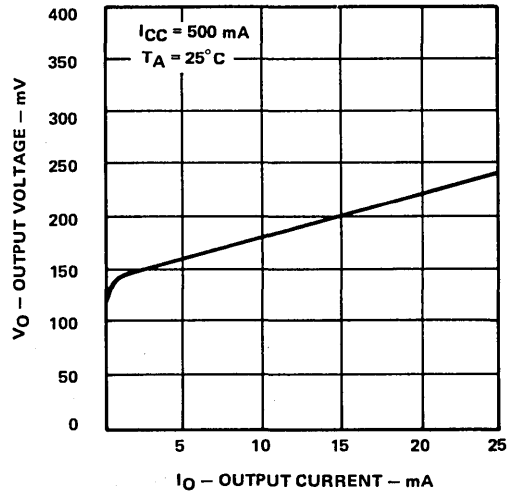


FIGURE 17 – TYPICAL OUTPUT CHARACTERISTICS

4.2.1 OUTPUT LOAD RESISTOR

When a discrete pull-up resistor R_L is utilized, the fanout requirements will restrict both its maximum and minimum values. The maximum load resistor value $R_{L(max)}$ will maintain the high-level output voltage minimum (2.4 V) while conducting $I_{OH} + N \cdot I_{IH(load)}$. $R_{L(max)}$ may be calculated as shown in Figure 18.

The minimum load resistor $R_{L(min)}$ should insure that the arithmetic sum of the current through R_L and the sink currents of the loads is less than I_{OL}. $R_{L(min)}$ may be calculated as shown in Figure 18.

Table 7 shows, for convenience, $R_{L(Min)}$ and $R_{L(Max)}$ values for several fanout values.

HIGH-LEVEL (OFF-STATE) CIRCUIT CALCULATIONS

The allowable voltage drop across the load resistor (V_{RL}) is the difference between the pull-up source and the V_{OH} level required at the load:

$$V_{RL} = V_{source} - V_{OH\ min}$$

The total current through the load resistor (I_{RL}) is the sum of the load current and the high-level output current (I_{OH}):

I_{RL} = Load Current (into the load inputs) + I_{OH}
where: I_{OH} = 400 μA max

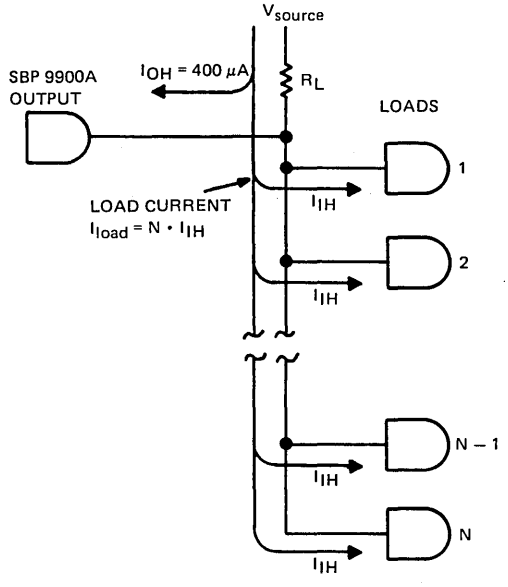
Therefore, calculations for the maximum value of R_L would be:

$$R_{L(max)} \text{ in ohms} = \frac{V_{source} - V_{OH\ min}}{\text{Load Current} + 400\ \mu A}$$

LOW-LEVEL (ON-STATE) CIRCUIT CALCULATIONS

The maximum current through the load resistor when the output is on, plus the amount of current from the low-level input load, must be limited to the I_{OL} capability of the output. Therefore, the equation is:

$$R_{L(min)} = \frac{V_{source} - V_{OL\ max}}{I_{OL} - I_{load}}$$

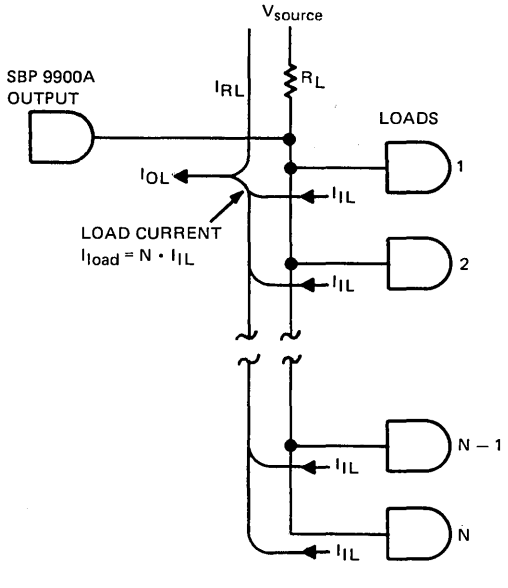


Assume: V_{source} = 5 V, $V_{OH(min)}$ = 2.4 V, N = 5, I_{IH} = 50 μA

$$R_{L(max)} = \frac{V_{source} - V_{OH}}{I_{load} + I_{OH}}$$

$$R_{L(max)} = \frac{5\ V - 2.4\ V}{250\ \mu A + 400\ \mu A} = \frac{2.6}{0.00065}\ \Omega = 4000\ \Omega$$

A. R_L MAXIMUM CALCULATIONS



Assume: V_{source} = 5 V, V_{OL} = 0.4 V, I_{IL} = 2 mA, N = 5, I_{OL} capability = 20 mA

$$R_{L(min)} = \frac{V_{source} - V_{OL}}{I_{OL} - I_{load}}$$

$$R_{L(min)} = \frac{5\ V - 0.4\ V}{20\ mA - 10\ mA} = \frac{4.6}{0.01}\ \Omega = 460\ \Omega$$

B. R_L MINIMUM CALCULATIONS

FIGURE 18 – OUTPUT LOAD RESISTOR CALCULATIONS

TABLE 7
OUTPUT LOAD RESISTOR VALUES (R_L)

TYPE OF LOGIC	DRIVING 1 LOAD		DRIVING 5 LOADS		DRIVING 10 LOADS	
	$R_{L(min)}$	$R_{L(max)}$	$R_{L(min)}$	$R_{L(max)}$	$R_{L(min)}$	$R_{L(max)}$
54LS/74LS	234 Ω	6190 Ω	252 Ω	5200 Ω	280 Ω	4333 Ω
54/74	250 Ω	5909 Ω	383 Ω	4333 Ω	1150 Ω	3250 Ω
54S/74S	256 Ω	5777 Ω	460 Ω	4160 Ω	2300 Ω	2888 Ω
MOS	230 Ω	6341 Ω	230 Ω	5777 Ω	231 Ω	5200 Ω
C-MOS	230 Ω	6500 Ω	230 Ω	6500 Ω	231 Ω	6498 Ω

CONDITIONS:	And unit loads of:	I_{IL}	I_{IH}
V_{source} = 5 V,	54LS/74LS	0.36 mA	10 μA
V_{OH} = 2.4 V (Satisfies most 5-V logic),	54/74	1.6 mA	40 μA
V_{OL} = 0.4 V,	54S/74S	2 mA	50 μA
I_{OH} = 400 μA (Maximum leakage),	N-MOS	10 μA	10 μA
I_{OL} = 20 mA	C-MOS	10 pA	10 pA

5. POWER SOURCE

I^2L is a current-injected logic. When the injector and ground pins are placed across a curve tracer, the processor V-1 characteristic will resemble that of a silicon switching diode. Any voltage or current source capable of supplying the desired current at the injector node voltage required will suffice. A regulated current source is recommended.

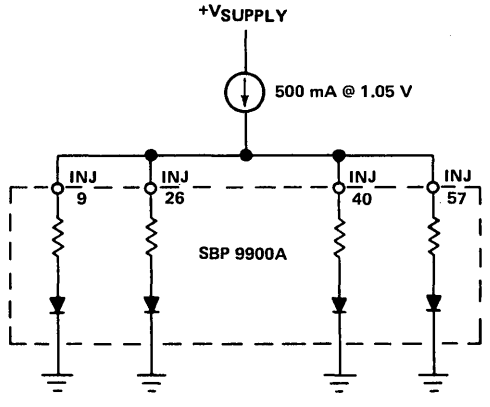
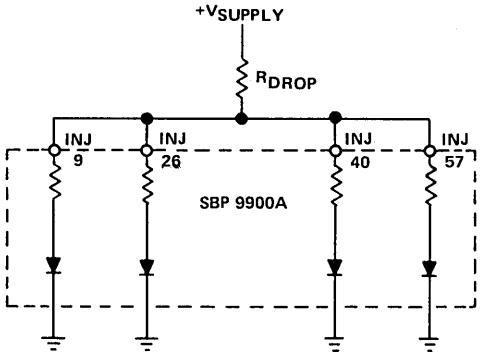


FIGURE 19 – INJECTOR CURRENT SOURCE



GENERAL FORMULA (OHM'S LAW)

$$R_{DROP} = \frac{V_{SUPPLY} - V_{CC}}{I_{CC}}$$

EXAMPLE FOR V_{SUPPLY} = 5V, AND I_{CC} = 500 mA:

$$R_{DROP} = \frac{5 - 1.05}{0.5} = \frac{3.95}{0.5} = 7.9 \text{ OHMS}$$

FIGURE 20 – INJECTOR CURRENT CALCULATIONS

4

Figures 21 and 22 show the typical injector node voltages that occur across the temperature and injector current ranges.

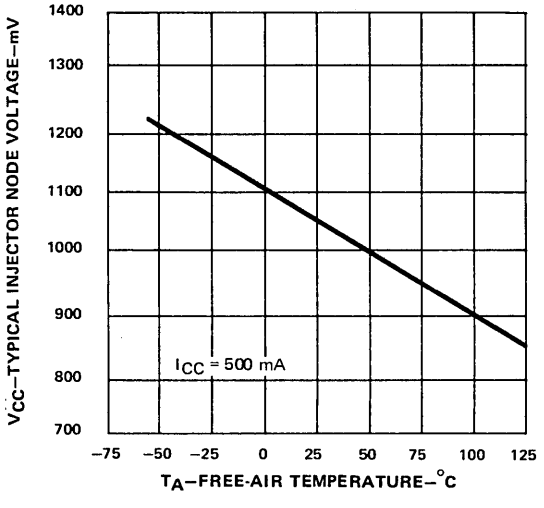


FIGURE 21 – INJECTOR-NODE VOLTAGE vs FREE-AIR TEMPERATURE

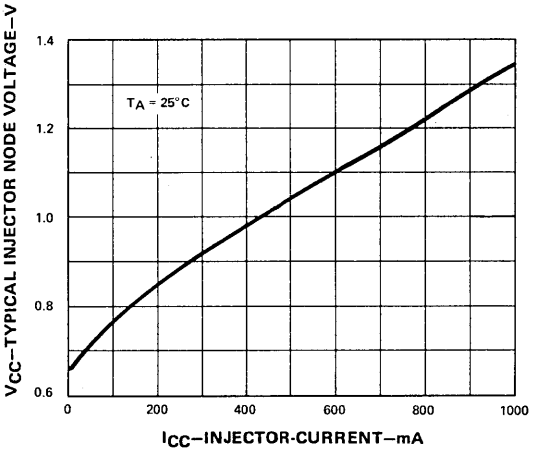


FIGURE 22 – INJECTOR-NODE VOLTAGE vs INJECTOR CURRENT

6. ELECTRICAL AND MECHANICAL SPECIFICATIONS

6.1 SBP 9900A-1 RECOMMENDED OPERATING CONDITIONS AT I_{CC} = 500 mA (UNLESS OTHERWISE NOTED)

PARAMETER		MIN	NOM	MAX	UNIT
Supply current, I_{CC}	SBP 9900A MJ-1/NJ-1/EJ-1	500	525	550	mA
	SBP 9900ACJ	500	550	620	
High-level output voltage, V_{OH}				5.5	V
Low-level output current, I_{OL}				20	mA
Clock frequency, f_{clock}		0		3	MHz
Width of clock pulse, t_w	High (67%)	222			ns
	Low (33%)	111			
Clock rise time, t_r				20	ns
Clock fall time, t_f				20	ns
Setup time, t_{su} (see Figure 23)†	HOLD	110†			ns
	READY	70†			
	D0 thru D15	65†			
	CRUIN	50†			
	INTREQ	25†			
	IC0 thru IC3	25†			
Hold time, t_h (see Figure 23)†	HOLD	25†			ns
	READY	50†			
	D0 thru D15	40†			
	CRUIN	40†			
	INTREQ	55†			
	IC0 thru IC3	55†			
Operating free-air temperature, T_A	SBP 9900AMJ-1, SBP 9900ANJ-1	−55		125	°C
	SBP 9900AEJ-1	−40		85	
	SBP 9900ACJ-1	0		70	

NOTE: The SBP 9900ANJ-1 is electrically equivalent to MIL-M-38510/46001 and is processed in accordance with Method 5004 of MIL-STD-883B.

† The set-up and hold times on the HOLD, RESET, and LOAD inputs can be satisfied by synchronizing these signals to the CPU clock.

DESIGN GOAL

This page provides tentative information on a product in the developmental stage. Texas Instruments reserves the right to change or discontinue this product without notice.

6.2 SBP 9900A-1 CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		I_{CC} = MIN,	I_I = –12 mA			–1.5	V
I_{OH}	High-level output current	I/O Pins	I_{CC} = MIN,	V_{IH} = 2 V,			350	μA
		Other outputs	V_{IL} = 0.8 V,	V_{OH} = 2.4 V			50	μA
		I/O Pins	I_{CC} = MIN,	V_{IH} = 2 V			1	mA
		Other outputs	V_{IL} = 0.8 V,	V_{OH} = 5.5 V			250	μA
V_{OL}	Low-level output voltage		I_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V I_{OL} = 20 mA			0.4	V
I_I	Input current	Clock	I_{CC} = MIN,	V_I = 2.4 V		0.6	1	mA
		All other inputs				200	300	μA

6.3 SBP 9900A-1 SWITCHING CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED), I_{CC} = 500 mA, SEE FIGURES 23 AND 24

PARAMETER	FROM	TO	TEST CONDITIONS†	SBP 9900A-1			UNIT
				MIN	TYP	MAX	
t_{PLH} or t_{PHL}	CLOCK	ADDRESS BUS (A0 – A14)	C_L = 150 pF		90	140	ns
t_{PLH} or t_{PHL}	CLOCK	DATA BUS (D0 – D15)			105	155	ns
t_{PLH} or t_{PHL}	CLOCK	WRITE ENABLE (WE)			100	185	ns
t_{PLH} or t_{PHL}	CLOCK	CYCLE END (CYCEND)			90	145	ns
t_{PLH} or t_{PHL}	CLOCK	DATA BUS IN (DBIN)			115	160	ns
t_{PLH} or t_{PHL}	CLOCK	MEMORY ENABLE (MEMEN)			90	140	ns
t_{PLH} or t_{PHL}	CLOCK	CRU CLOCK (CRUCK)			95	155	ns
t_{PLH} or t_{PHL}	CLOCK	CRU DATA OUT (CRUOUT)			110	185	ns
t_{PLH} or t_{PHL}	CLOCK	HOLD ACKNOWLEDGE (HLDA)			190	290	ns
t_{PLH} or t_{PHL}	CLOCK	WAIT			90	130	ns
t_{PLH} or t_{PHL}	CLOCK	INSTRUCTION ACQUISITION (IAQ)			90	130	ns

† For conditions shown MIN, NOM, or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at I_{CC} = 500 mA, T_A = 25°C.

4

DESIGN GOAL

381 This page provides tentative information on a product in the developmental stage. Texas Instruments reserves the right to change or discontinue this product without notice.

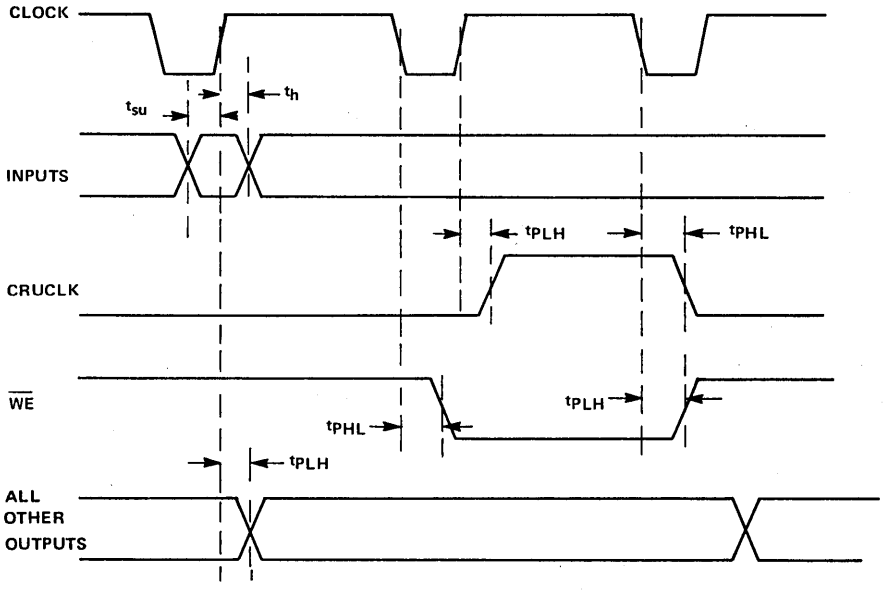


FIGURE 23 – SWITCHING-TIME VOLTAGE WAVEFORMS

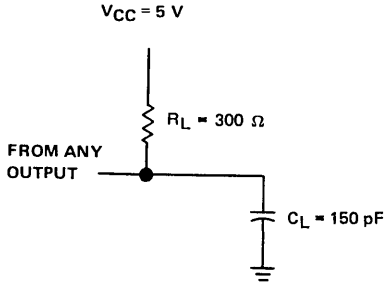


FIGURE 24 – SWITCHING-TIME LOAD-CIRCUITS

6.4 CLOCK FREQUENCY VS. TEMPERATURE

Stability of the operational frequency over the full temperature range of –55°C to 125°C is illustrated in Figure 25. The effects of temperature on clock frequency are nil above 0°C. Below 0°C the effects are typically less than –5% with respect to the typical performance.

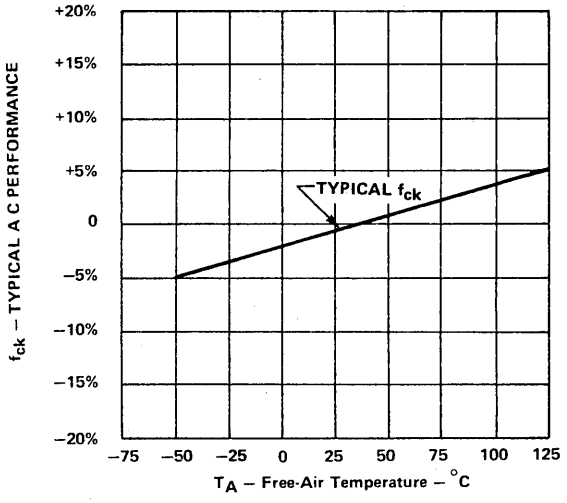
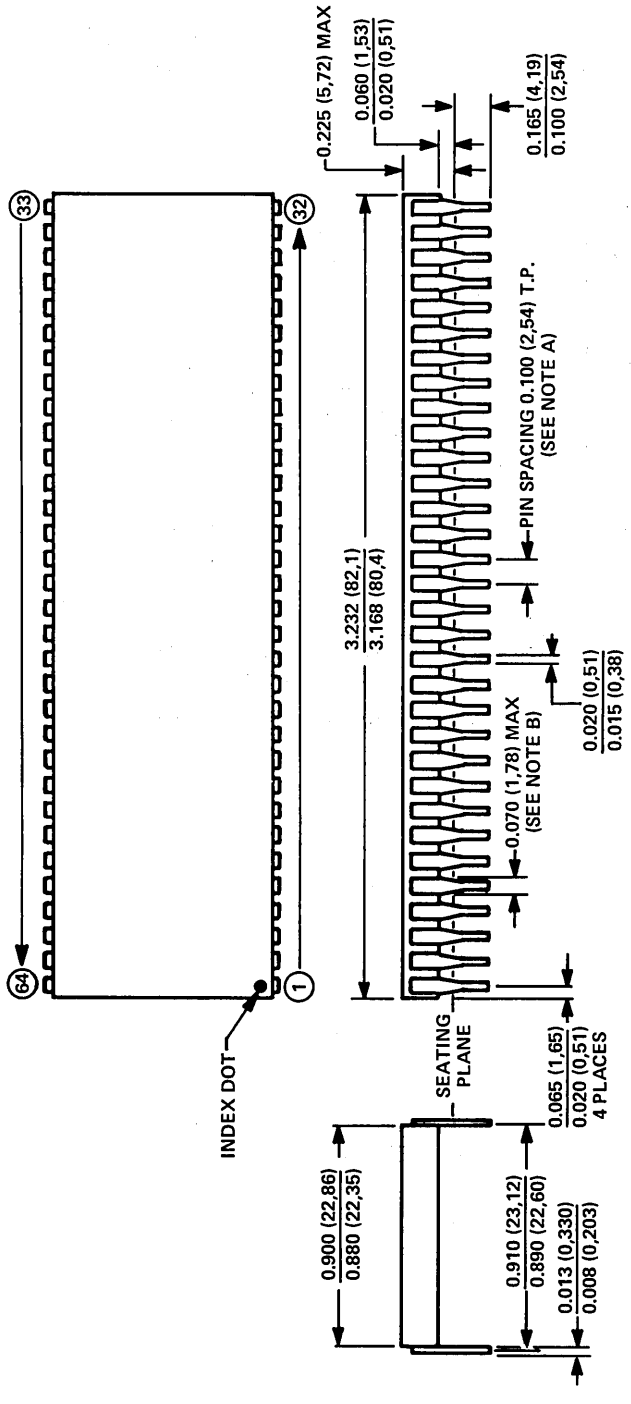


FIGURE 25 – AC PERFORMANCE FREE-AIR TEMPERATURE

7. MECHANICAL DATA



NOTES: A. Each pin centerline is located within 0.010 (2,54) of its true longitudinal position.
B. The minimum limit for this dimension may be 0.020 (0,51) for leads 1, 32, 33, and 64 only.
C. All dimensions are in inches and parenthetically in millimeters. Inch dimensions govern.

781

SBP 9960 Programmable CRU I/O Expander

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

SBP 9960
PROGRAMMABLE CRU I/O EXPANDER

1.0 INTRODUCTION

1.1 GENERAL DESCRIPTION

The SBP 9960 Programmable CRU I/O Expander is a ruggedized monolithic software-configurable input/output device fabricated with oxide separated Integrated Injection Logic (I^2L) technology. The SBP 9960 provides a flexible and efficient Communications Register Unit (CRU) based interface between the CPU and auxiliary systems functions ranging from bit-oriented sensors and actuators to byte/word/n-bit-field oriented peripherals.

Under software control, each of the SBP 9960's sixteen single-bit I/O ports may be individually configured to either the input or output mode. I^2L technology enables the SBP 9960's static logic, and TTL compatible I/O, to operate over a very wide ambient temperature range from a single d-c power source with output current sink capability up to 24 mA.

1.2 KEY FEATURES

- SBP 9900/SBP 9989 Series Microprocessor Family Peripheral
- 16 Individual, Single Bit, Software Configurable I/O Ports
- 12/24 mA current Sinking Outputs
- TTL Compatible I/O
- Wide Ambient Temperature Operation
  - — SBP 9960NJ: −55°C to +125°C (screened to MIL-STD-883B)
- I^2L Technology
  - — Constant Current Power Source
  - — Fully Static Operation
  - — Wide Temperature Stability

2.0 FUNCTIONAL DESCRIPTION

2.1 SBP 9960/CPU INTERFACE

The SBP 9960 communicates with the CPU through the communications Register Unit (CRU) interface as shown in Figures 1 and 3. The SBP 9960's CRU interface consists of: a) five CRU address select lines (S0-S4), B) a single chip enable ($\overline{CE}$), c) a 9960 to CPU serial data-bit line (CRUIN), d) a CPU to 9960 serial data-bit line (CRUOUT), and e) a CPU to 9960 serial data-bit clock (CRUCLK). When $\overline{CE}$ is activated (logic-level low), S0-S4 select a specific single-bit I/O port as indicated in Table 1. In the case of an SBP 9960 write operation, the datum is transferred from the CPU to the SBP 9960 via the CRUOUT line. The CRUOUT datum is strobed into the selected single-bit port by CRUCLK. In the case of a SBP 9960 read operation, the selected single-bit port is sampled by the CPU via the CRUIN line.

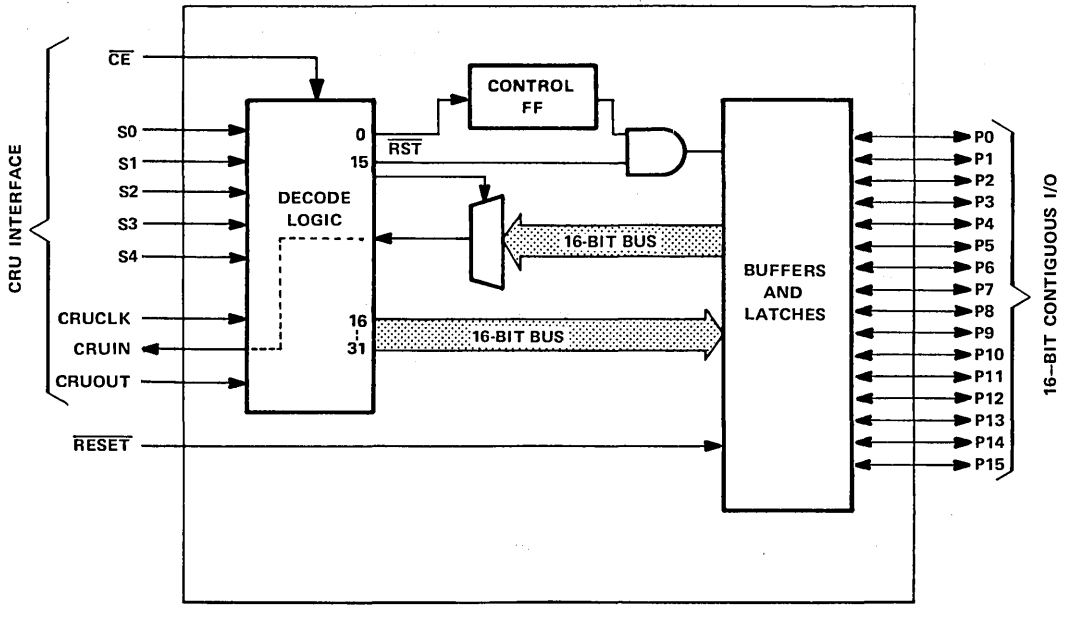


FIGURE 1. SBP9960 FUNCTIONAL BLOCK DIAGRAM

2.2 CRU BIT ASSIGNMENTS

Table 1 describes the SBP 9960's CRU bit assignments. Note that CRU bits 1-14 have been reserved for the SBP 9961.

2.3 INPUT/OUTPUT

One of sixteen SBP 9960, single-bit, combination open-collector-output/resistor-divider-input I/O ports is conversationally represented in figure 2. As a direct result of the open-collector output structure, the data flow direction through the port is determined by the stored logic-level of the associated output-register bit in combination with the data flow direction of the external device serviced by the port. When

the output-register bit (Q) is at logic-level high, the corresponding package pin (P) is essentially floating and therefore free to be externally pulled to either the high or low logic-level. In other words, when Q is at logic-level high, the ports data flow direction can be either inward, where an external device pulls P to the high or low logic-level; or the data flow direction can be outward, where an external resistor (R) both pulls P to logic-level high and sources current drive into the inputs of external devices. When Q is at logic-level low, the ports unconditional data flow direction is outward, where P has the capacity to sink 12/24*mA of current from external devices. Q can be reset to logic-level low through CPU execution of a SET BIT TO ZERO (SBZ) instruction; Q can be set to logic-level high through: 1) a hardware initiated reset ($\overline{\text{RESET}}$), 2) a software initiated reset ($\overline{\text{RST}}$: CRU BIT 15) preceded by setting the control bit (CRU BIT 0) to logic-level high, or 3) CPU execution of a SET BIT TO ONE (SBO) instruction. Note that both $\overline{\text{RESET}}$ and $\overline{\text{RST}}$ affect all sixteen single-bit I/O ports while CPU execution of either an SBO or SBZ instruction can be targeted at an individual single-bit port independent of uninvolved ports. Once the data flow direction has been established for each single-bit port, CPU communication with the external devices driven or sensed by each individual port is effected through execution of the CRU instructions: LDCR, STCR, SBO, SBZ, and TB.

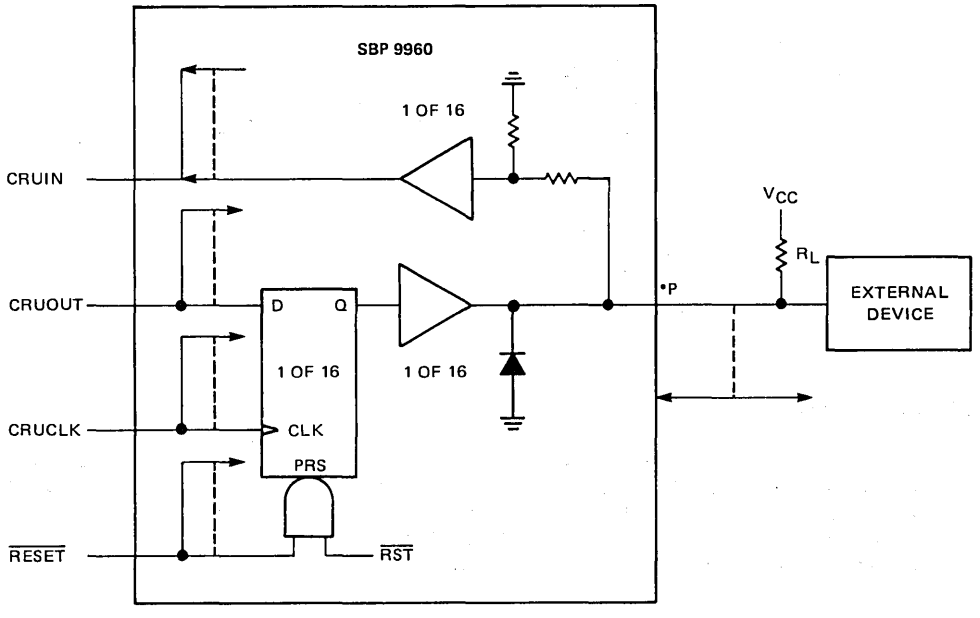


FIGURE 2. 1 OF 16 SINGLE-BIT I/O PORTS

*Outputs P0, P1, P2, and P3 have extended current sink capability to 24 mA.

TABLE 1 – SBP 9960 CRU BIT ASSIGNMENTS

CRU BIT	S0	S1	S2	S3	S4	CRU READ DATA	CRU WRITE DATA
0	0	0	0	0	0	Control Bit	Control Bit
1-14						Note 1	Note 1
15	0	1	1	1	1	"1"	No Operation/ $\overline{RST}$ (2)
16	1	0	0	0	0	P0 Input(3)	P0 Output(4) (5)
17	1	0	0	0	1	P1	P1 (5)
18	1	0	0	1	0	P2	P2 (5)
19	1	0	0	1	1	P3	P3 (5)
20	1	0	1	0	0	P4	P4
21	1	0	1	0	1	P5	P5
22	1	0	1	1	0	P6	P6
23	1	0	1	1	1	P7	P7
24	1	1	0	0	0	P8	P8
25	1	1	0	0	1	P9	P9
26	1	1	0	1	0	P10	P10
27	1	1	0	1	1	P11	P11
28	1	1	1	0	0	P12	P12
29	1	1	1	0	1	P13	P13
30	1	1	1	1	0	P14	P14
31	1	1	1	1	1	P15 Input(3)	P15 Output(4)

NOTES: (1) Bits 1-14 reserved for SBP 9961
(2) Writing a zero to bit 15 while CONTROL = 1 executes a software reset of the I/O ports.
(3) Data present on the port will be read without affecting the data.
(4) Writing data to the port will both program the port to the output mode and output the data.
(5) These outputs are provided with extended sink-current capability to 24 mA.

2.4 SYSTEM OPERATION

During a typical power-up sequence of a SBP 9960-based system, $\overline{RESET}$ should be activated (logic-level low) to force the SBP 9960 to the state where each of the sixteen individual single-bit I/O ports is in the input mode. System software should then configure each single-bit port as required. If a given port is to be used as an input, the associated output register bit must be set to a logic level high through CPU execution of an SBO instruction.

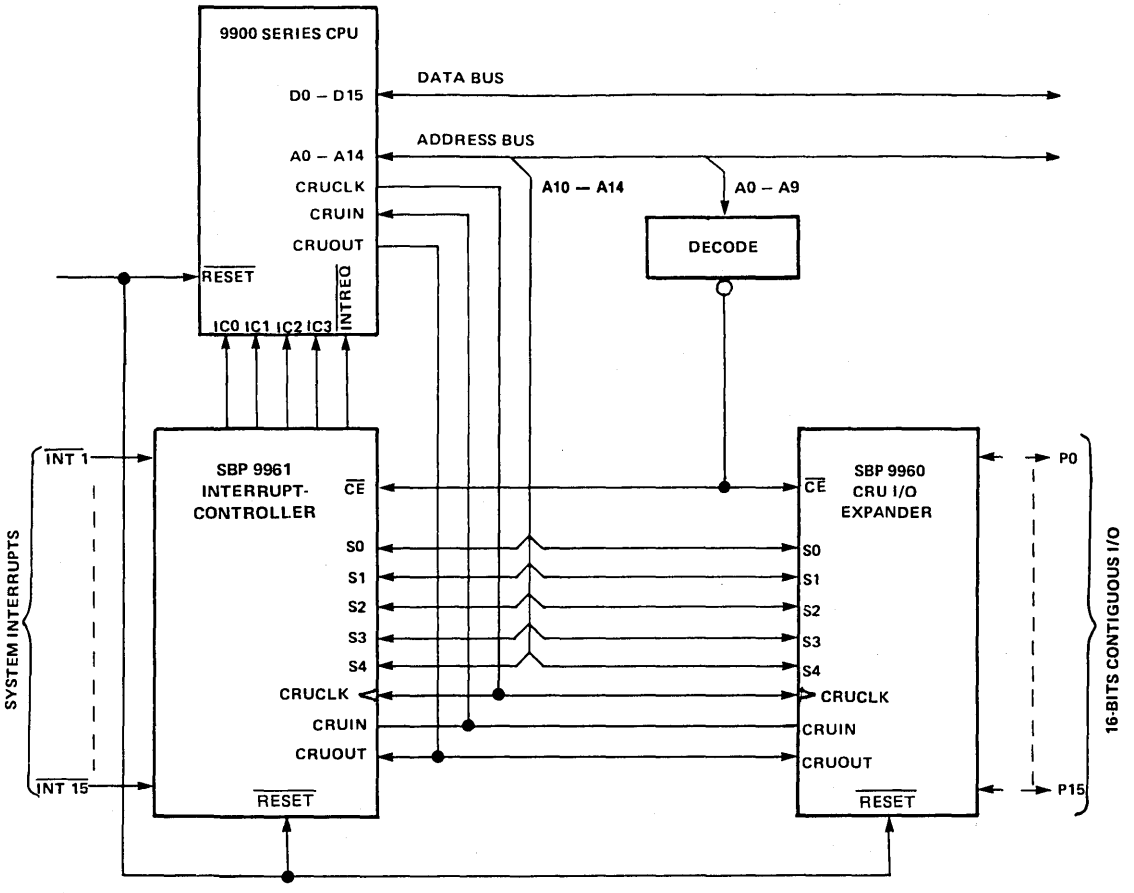
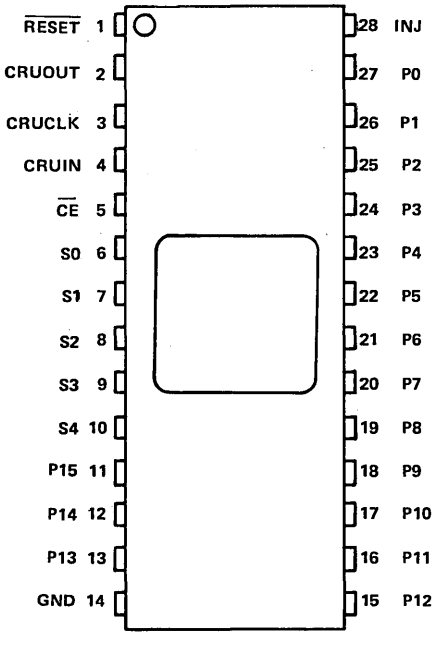


FIGURE 3 – SYSTEM CONFIGURATION USING SBP 9960 AND SBP 9961

2.5 SBP 9960 PIN ASSIGNMENTS AND FUNCTIONS

SIGNATURE	PIN	I/O	DESCRIPTION
S0	6	IN	ADDRESS SELECT LINES. The data bit being accessed by the CRU interface is specified by the 5-bit code appearing on S0-S4.
S1	7	IN	
S2	8	IN	
S3	9	IN	
S4	10	IN	
CRUIN	4	OUT	CRU DATA IN (to CPU). Data specified by S0-S4 is transmitted to the CPU by CRUIN. When $\overline{CE}$ is not active, CRUIN is pulled to logic-level high.
CRUOUT	2	IN	CRU DATA OUT (from CPU). When $\overline{CE}$ is active data present on the CRUOUT input will be strobed by CRUCLK and written into the CRU bit specified by S0-S4.
CRUCLK	3	IN	CRU CLOCK (from CPU). CRUCLK specifies that valid data is present on the CRUOUT line.
$\overline{RESET}$	1	IN	POWER-UP RESET. When active (low), $\overline{RESET}$ forces all I/O's (P0-P15) to input mode.
$\overline{CE}$	5	IN	CHIP ENABLE. When active (low), data may be bidirectionally transferred between the SBP 9960 and the CPU.
INJ	28		Supply Current
GND	14		Ground Reference
P0	27	I/O	I/O pins
P1	26	I/O	
P2	25	I/O	
P3	24	I/O	
P4	23	I/O	
P5	22	I/O	
P6	21	I/O	
P7	20	I/O	
P8	19	I/O	
P9	18	I/O	
P10	17	I/O	
P11	16	I/O	
P12	15	I/O	
P13	13	I/O	
P14	12	I/O	
P15	11	I/O	



3.0 ELECTRICAL SPECIFICATIONS

3.1 RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply current, I_{CC}†		70	77	84	mA
High-level output voltage, V_{OH}				5.5	V
Low-level output current, I_{OL}	P0, P1, P2, P3			24	mA
	Other outputs			12	
Operating free-air temperature, T_A		−55		125	°C

†Typical injector voltage, V_{INJ} = 1.2 V

3.2 ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE

PARAMETER			TEST CONDITIONS‡		MIN	MAX	UNIT
V_{IH}	High-level input voltage				2		V
V_{IL}	Low-level input voltage					0.7	V
V_{IK}	Input clamp voltage		I_{CC} = 70 mA, I_I = 12 mA			−1.5	V
I_{OH}	High-level output current	I/O port	I_{CC} = 77 mA, V_{IH} = 2 V, V_{IL} = 0.7 V	V_{OH} = 2.4 V		400	µA
		CRUIN output				50	µA
		I/0 port		V_{OH} = 5.5 V		1	mA
		CRUIN output				250	µA
V_{OL}	Low-level output voltage		I_{CC} = 77 mA, V_{IH} = 2 V, V_{IL} = 0.7 V,	I_{OL} = MAX		0.5	V
I_{IH}	High-level input current		I_{CC} = 77 mA	V_I = 2.4 V		400	µA
				V_I = 5.5 V		1	mA

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

3.3 TIMING REQUIREMENTS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS

PARAMETER			MIN	MAX	UNIT
t_w	Width of CRUCLK pulse		55		ns
t_{su}	Setup time	Address or select to CRUCLK	130		ns
		CRUOUT to CRUCLK	0		
t_h	Hold time	Address or select after CRUCLK	100		ns
		Data after CRUCLK	65		

3.4 SWITCHING CHARACTERISTICS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS

PARAMETER§	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH} or t_{PHL}	CRUCLK	I/O port	C_L = 100 pF,		220	ns
t_{PLH} or t_{PHL}	Address or select	CRUIN	R_L = 390 Ω,		250	ns
t_{PLH} or t_{PHL}	I/O port	CRUIN	See Figures 4, 5 and 6		100	ns

§ t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output

4

PRODUCT PREVIEW

581 This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

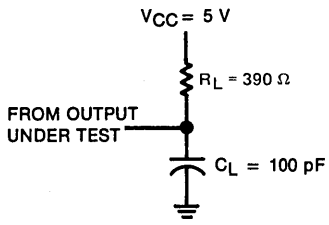


FIGURE 4 – SWITCHING TIME LOAD CIRCUIT

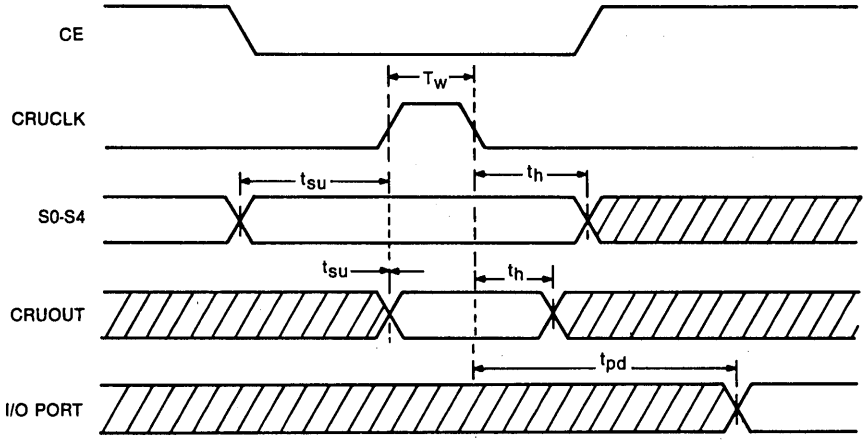


FIGURE 5 — SBP9960 CPU TO I/O PORT TIMING DIAGRAM

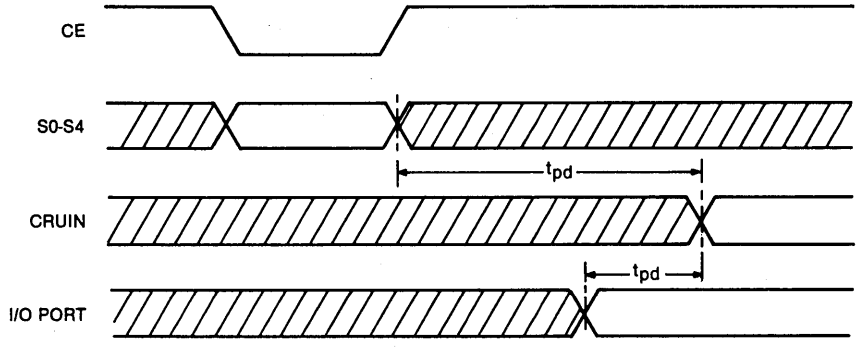
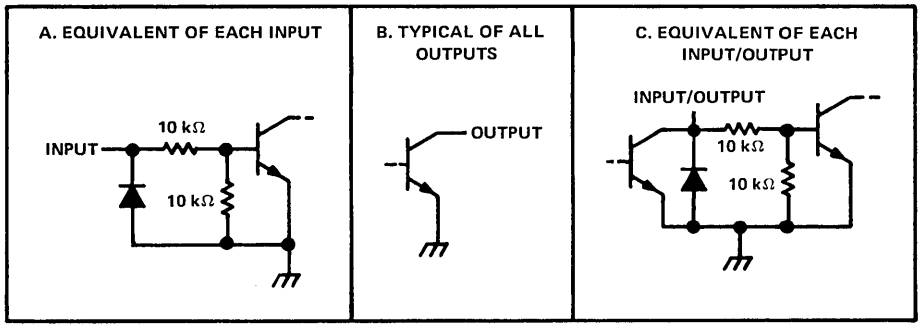
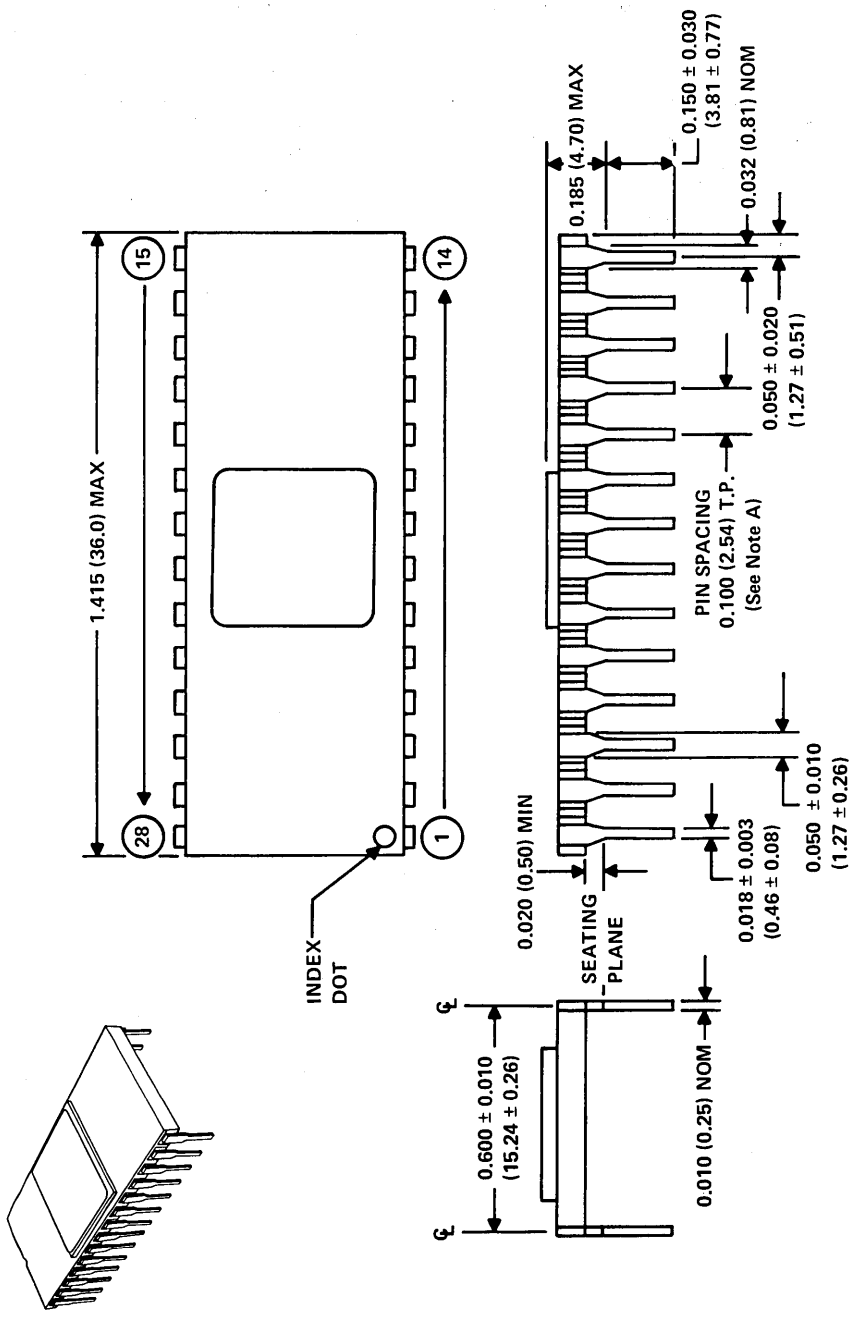


FIGURE 6 — I/O PORT TO CPU

581


A. EQUIVALENT OF EACH INPUT
INPUT
10 kΩ
10 kΩ
B. TYPICAL OF ALL OUTPUTS
OUTPUT
C. EQUIVALENT OF EACH INPUT/OUTPUT
INPUT/OUTPUT
10 kΩ
10 kΩ

5.0 MECHANICAL DATA — 28-PIN CERAMIC DUAL-IN-LINE PACKAGE



NOTES: A. EACH PIN CENTERLINE IS LOCATED WITHIN 0.100 OF ITS TRUE LONGITUDINAL POSITION.

B. ALL LINEAR DIMENSIONS ARE IN INCHES (AND PARENTHETICALLY IN MILLIMETERS FOR REFERENCE ONLY). INCH DIMENSIONS GOVERN.

SBP 9961
Interrupt Controller

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

SBP 9961 INTERRUPT CONTROLLER

1.0 INTRODUCTION

1.1 GENERAL DESCRIPTION

The SBP 9961 Controller is a ruggedized, monolithic, programmable, multifunction system support device fabricated with oxide separated Integrated Injection Logic (I^2L) technology. The SBP 9961 provides the SBP 9900 series Family of Microprocessors with a maskable prioritized interrupt encoding capability. I^2L technology enables the SBP 9961's static logic and TTL compatible I/O to operate over a very wide ambient temperature range from a single d-c power source.

1.2 KEY FEATURES

- SBP 9900 Series Microprocessor Family Peripheral
- 15 Dedicated, Maskable, Prioritized, Encoded Interrupts
- 12 mA Current Sinking Outputs
- 40-Pin Package
- TTL Compatible I/O
- Wide Ambient Temperature Operation
  - SBP 9961NJ: −55°C to +125°C (with high-reliability processing) (screened to MIL-STD 883B)
- I^2L Technology
  - Constant-Current Power Source
  - Fully Static Operation
  - Single-Phase Edge-Triggering Clock
  - Wide Temperature Stability

2.0 FUNCTIONAL DESCRIPTION

2.1 SBP 9961/CPU INTERFACE

The SBP 9961 communicates with the CPU through the Communications Register Unit (CRU) interface as shown in Figures 1 and 3. The SBP 9961's CRU interface consists of: a) five CRU address select lines (S0-S4) b) a single chip enable (CE), c) a 9961-to-CPU serial data-bit line (CRUIN), d) a CPU-to-9961 serial data-bit line (CRUOUT), and e) a CPU-to-9961 serial data-bit clock (CRUCLK). When $\overline{CE}$ is activated (logic-level low), S0-S4 selects a specific CRU bit function as indicated in Table 1. In the case of a SBP 9961 write operation, the datum is transferred from the CPU to the SBP 9961 via the CRUOUT line. The CRUOUT datum is strobed into the selected 9961 CRU bit function by CRUCLK. In the case of a SBP 9961 read operation, the selected CRU bit function is sampled by the CPU via the CRUIN line.

TABLE 1 – CRU BIT ASSIGNMENTS

CRU BIT	S0	S1	S2	S3	S4	CRU READ DATA	CRU WRITE DATA
0	0	0	0	0	0	Control Bit	Control Bit(1)
1	0	0	0	0	1	$\overline{INT1}$ (2)	Mask1 (3)
2	0	0	0	1	0	$\overline{INT2}$	Mask2
3	0	0	0	1	1	$\overline{INT3}$	Mask3
4	0	0	1	0	0	$\overline{INT4}$	Mask4
5	0	0	1	0	1	$\overline{INT5}$	Mask5
6	0	0	1	1	0	$\overline{INT6}$	Mask6
7	0	0	1	1	1	$\overline{INT7}$	Mask7
8	0	1	0	0	0	$\overline{INT8}$	Mask8
9	0	1	0	0	1	$\overline{INT9}$	Mask9
10	0	1	0	1	0	$\overline{INT10}$	Mask10
11	0	1	0	1	1	$\overline{INT11}$	Mask11
12	0	1	1	0	0	$\overline{INT12}$	Mask12
13	0	1	1	0	1	$\overline{INT13}$	Mask13
14	0	1	1	1	1	$\overline{INT14}$	Mask14
15	0	1	1	1	1	$\overline{INT15}/\overline{INTREQ}$	Mask 15

NOTES: (1) 0 = Interrupt Mode; 1 = No operation except CRU bit 15 – $\overline{INTREQ}$
(2) Data present on $\overline{INT}$ input will be read regardless of mask value.
(3) While in the Interrupt Mode (Control Bit = 0), writing a "1" into a mask will enable interrupt, "0" will disable.

2.2 INTERRUPT CONTROL

A block diagram of the SBP 9961 interrupt control section is shown in Figure 2. The interrupt inputs are sampled on the positive-going edge of CLOCK and are ANDed with their respective mask bits. If an interrupt input is active (low) and enabled (MASK = 1), the signal is passed through the priority encoder where the highest priority signal is encoded into a 4-bit binary word as shown in Table 2. This word, along with an interrupt request, is then output to the CPU on the positive-going edge of the next CLOCK.

The output signals will remain valid until either the corresponding interrupt input is removed, the interrupt is disabled (MASK = 0), or a higher priority enabled interrupt becomes active. When the highest priority enabled interrupt is removed, the code corresponding to the next highest priority enabled interrupt is output. If no enabled interrupt is active, $\overline{INTREQ}$ will be pulled to logic-level high with IC0–IC3 retaining the last asserted interrupt code. $\overline{RESET}$ (power-up reset) will force the interrupt code IC0–IC3 to (0,0,0,0) with $\overline{INTREQ}$ pulled high, and will reset all mask bits low (interrupts disabled). Individual interrupts can be subsequently enabled (disabled) by programming the appropriate mask bits. Unused interrupt inputs may be used as data inputs by disabling the interrupt (MASK = 0).

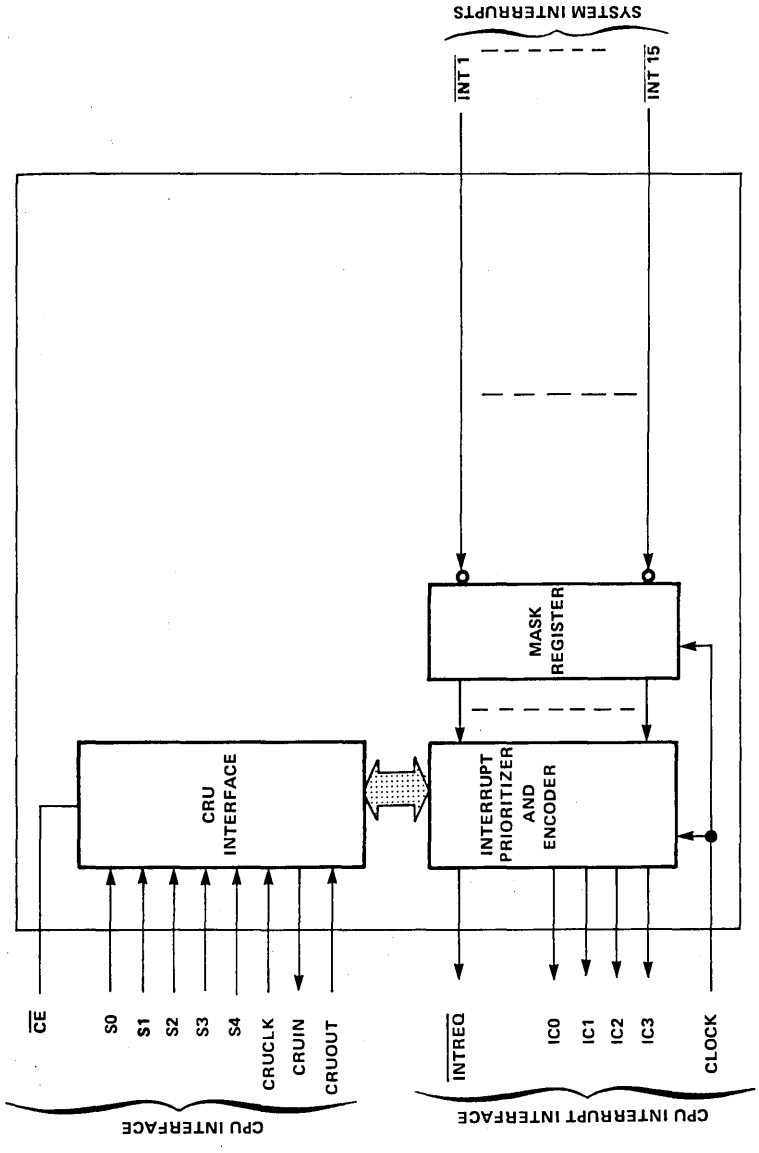


FIGURE 1 – SBP 9961 BLOCK DIAGRAM

4

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

681

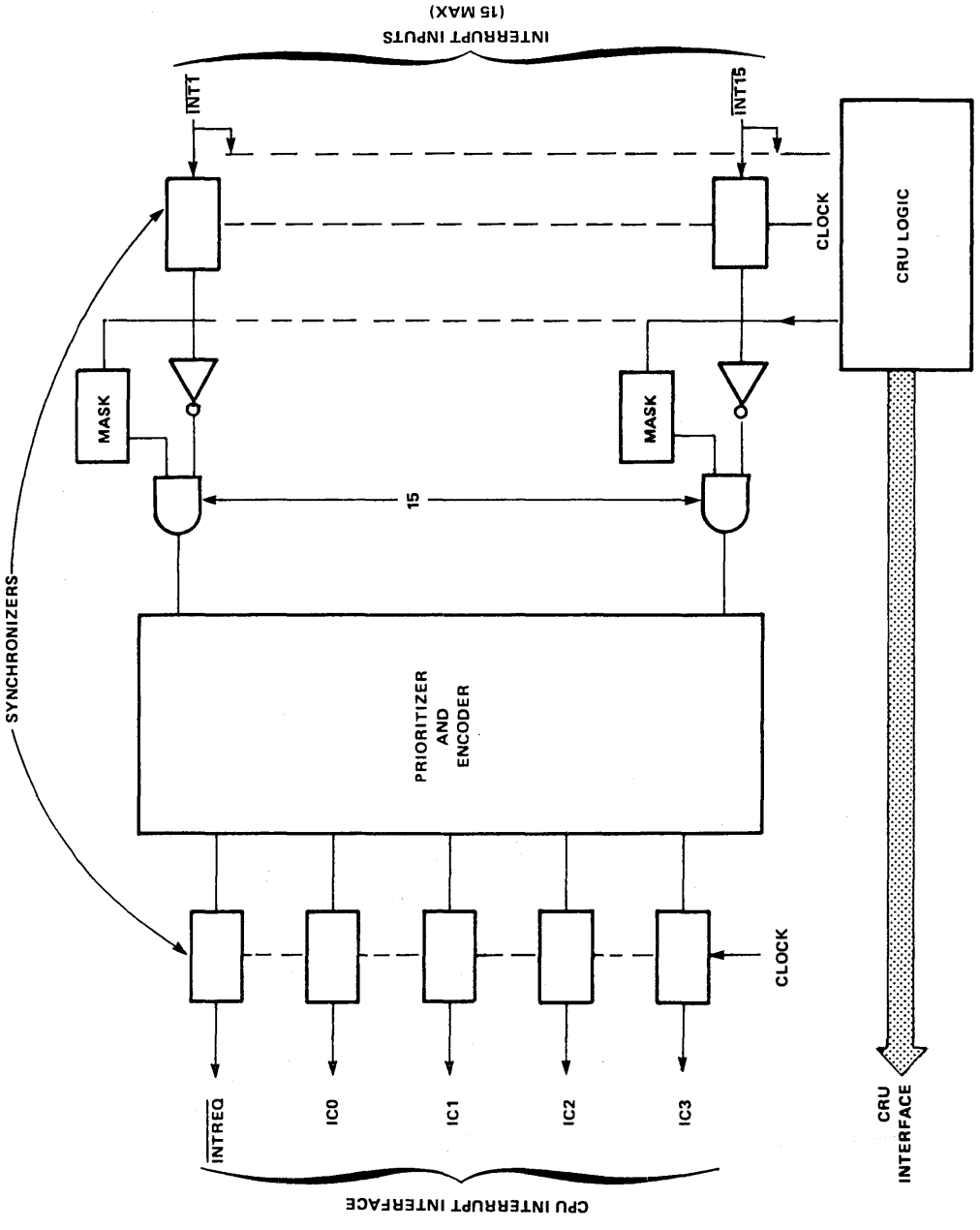


FIGURE 2 – INTERRUPT CONTROL LOGIC

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TABLE 2
INTERRUPT CODE GENERATION

INTERRUPT/STATE	PRIORITY	I_{C0}	I_{C1}	I_{C2}	I_{C3}	$\overline{INTREQ}$
$\overline{INT}$ 1	1 (HIGHEST)	0	0	0	1	0
$\overline{INT}$ 2	2	0	0	1	0	0
$\overline{INT}$ 3	3	0	0	1	1	0
$\overline{INT}$ 4	4	0	1	0	0	0
$\overline{INT}$ 5	5	0	1	0	1	0
$\overline{INT}$ 6	6	0	1	1	0	0
$\overline{INT}$ 7	7	0	1	1	1	0
$\overline{INT}$ 8	8	1	0	0	0	0
$\overline{INT}$ 9	9	1	0	0	1	0
$\overline{INT}$ 10	10	1	0	1	0	0
$\overline{INT}$ 11	11	1	0	1	1	0
$\overline{INT}$ 12	12	1	1	0	0	0
$\overline{INT}$ 13	13	1	1	0	1	0
$\overline{INT}$ 14	14	1	1	1	0	0
$\overline{INT}$ 15	15 (LOWEST)	1	1	1	1	0
NO INTERRUPT	—	Note 1	Note 1	Note 1	Note 1	1

(1) IC0-IC3 hold the level code of the previous interrupt.

4

681

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

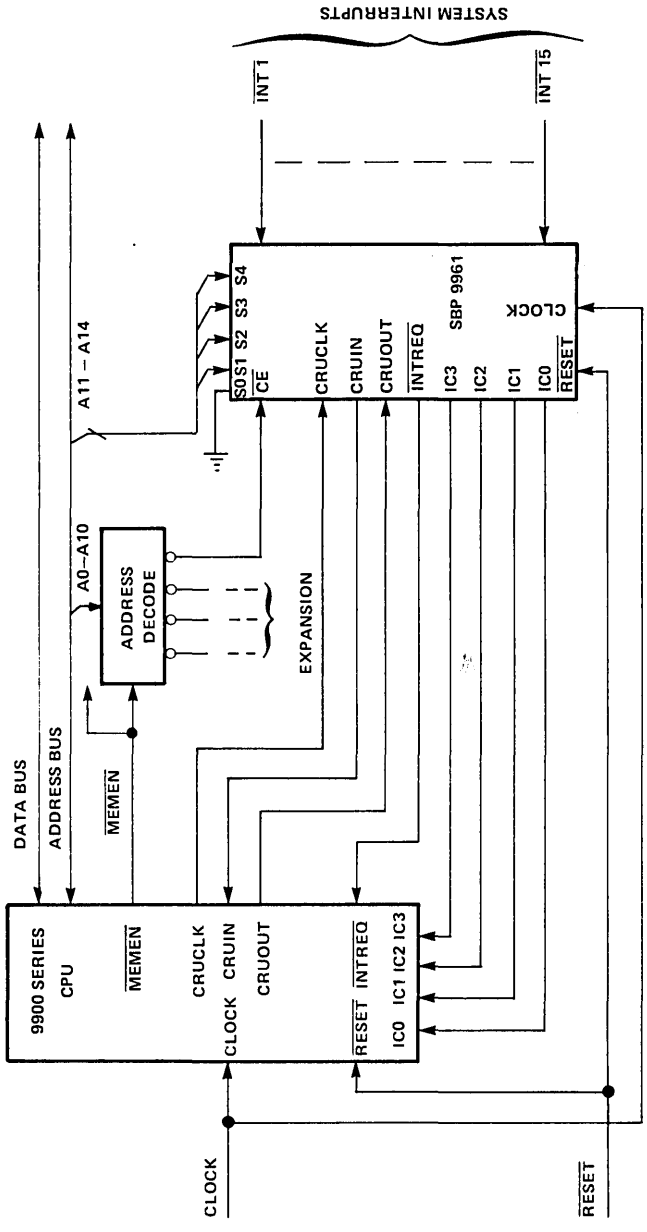


FIGURE 3 – SBP 9961 SYSTEM CONFIGURATION

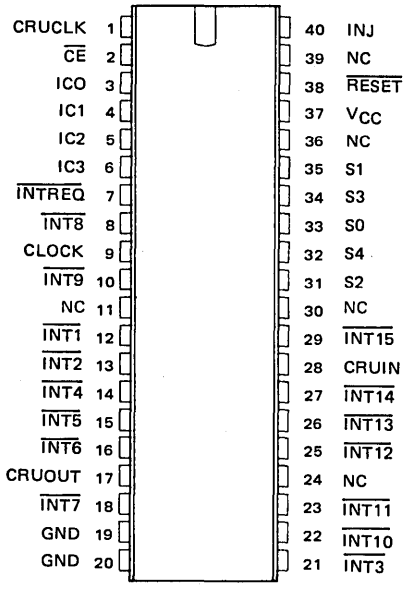
PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

2.6 SBP 9961 PIN ASSIGNMENTS AND FUNCTIONS

SIGNATURE	PIN	I/O	DESCRIPTION
S0	33	IN	ADDRESS SELECT LINES. The data bit being accessed by the CRU interface is specified by the 4-bit code appearing on S1–S4. S0 is used as the high order select line when the SBP 9961 is used with the SBP 9960. Otherwise, tie S0 to logic-level low.
S1	35	IN	
S2	31	IN	
S3	34	IN	
S4	32	IN	
CRUIN	28	OUT	CRU DATA IN (to CPU). Data specified by S0-S4 is transmitted to the CPU by CRUIN. When $\overline{CE}$ is not active, CRUIN is logic-level high.
CRUOUT	17	IN	CRU DATA OUT (from CPU). When $\overline{CE}$ is active, data present on the CRUOUT input will be sampled during CRUCLK and written into the CRU bit specified by S0-S4.
CRUCLK	1	IN	CRU CLOCK (from CPU). CRUCLK specifies that valid data is present on the CRUOUT line.
$\overline{RESET}$	38	IN	POWER-UP RESET. When active (low), $\overline{RESET}$ forces all interrupt masks to "0", and disables the clock.
$\overline{CE}$	2	IN	CHIP ENABLE. When active (low), data transfers may occur between the CPU and the SBP 9961.
	11	NC	
	24	NC	
	30	NC	
	36	NC	
	39	NC	
IC0	3	OUT	INTERRUPT CODE LINES (to CPU). IC0 (MSB) through IC3 output the binary code corresponding to the highest priority enabled interrupt most recently asserted.
IC1	4	OUT	
IC2	5	OUT	
IC3	6	OUT	
$\overline{INTREQ}$	7	OUT	INTERRUPT REQUEST (to CPU). When active (low) $\overline{INTREQ}$ indicates to the CPU that an enabled interrupt has been asserted, prioritized, and encoded.
CLOCK	9	IN	CPU SYSTEM CLOCK. Used by the SBP 9961 to synchronize the interrupt interface ($\overline{INTREQ}$, IC0-IC3) to the CPU.
INJ	40		Supply Current
GND	19, 20		Ground
V_{CC}	37		Common voltage return/reference for all output pull-up resistors.
$\overline{INT1}$	12	IN	INTERRUPT INPUTS. When active (low), the signal is ANDed with its corresponding mask bit and if enabled sent to the interrupt control section. $\overline{INT1}$ has highest priority.
$\overline{INT2}$	13	IN	
$\overline{INT3}$	21	IN	
$\overline{INT4}$	14	IN	
$\overline{INT5}$	15	IN	
$\overline{INT6}$	16	IN	
$\overline{INT7}$	18	IN	
$\overline{INT8}$	8	IN	
$\overline{INT9}$	10	IN	
$\overline{INT10}$	22	IN	
$\overline{INT11}$	23	IN	
$\overline{INT12}$	25	IN	
$\overline{INT13}$	26	IN	
$\overline{INT14}$	27	IN	
$\overline{INT15}$	29	IN	

SBP 9961



3.0 ELECTRICAL SPECIFICATIONS

3.1 RECOMMENDED OPERATING CONDITIONS, UNLESS OTHERWISE NOTED I_{CC}= 130 mA

	MIN	NOM	MAX	UNIT
Supply current, I_{CC}	115	130	145	mA
High-level output voltage, V_{OH}			5.5	V
Low-level output current, I_{OL}			12	mA
Operating free-air temperature, T_A	−55		125	°C

3.2 ELECTRICAL CHARACTERISTICS (OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE, UNLESS OTHERWISE NOTED)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	I_{CC} = MIN,	I_I = −12 mA			−1.5	V
I_{OH}	High-level output current	I_{CC} = 130 mA, V_{IL} = 0.8 V,	V_{IH} = 2 V, V_{OH} = 5.5 V			−400	μA
V_{OL}	Low-level output voltage	I_{CC} = 130 mA, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 12 mA			0.5	V
I_I	Input current	I_{CC} = 130 mA,	V_I = 2.4 V		180		μA

†For conditions shown as MAX, use the appropriate value specified under recommended operating conditions
‡All typical values are at I_{CC} = 130 mA, T_A = 25°C.

PRODUCT PREVIEW
This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

3.3 TIMING REQUIREMENTS OVER FULL RANGE OF OPERATING CONDITIONS

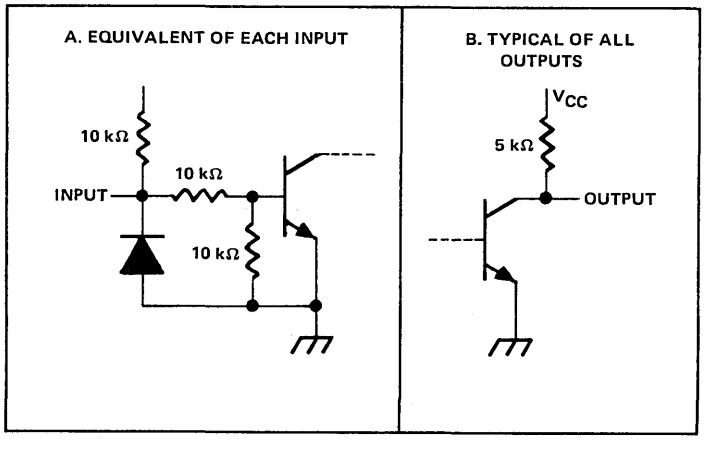
PARAMETER		MIN	NOM	MAX	UNIT
t_c	Clock cycle time	333			ns
t_r	Clock rise time		10	20	ns
t_f	Clock fall time		10	20	ns
t_{wL}	Clock pulse low width	111			ns
t_{wH}	Clock pulse high width	222			ns
t_{su}	Setup time for S0-S4, $\overline{CE}$, or CRUOUT before CRUCLK		200		ns
t_{su}	Setup time, input before valid CRUIN		200		ns
t_{su}	Setup time, interrupt before clock high		60		ns
$t_{w(CRUCLK)}$	CRU clock pulse width		100		ns
t_h	Address hold time		80		ns

3.4 SWITCHING CHARACTERISTICS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PD}	Propagation delay, ↑ CLOCK to valid $\overline{INTREQ}$, IC0-IC3	C_L = 100 pF. R_L = 390 Ω		150		ns
t_{PD}	Propagation delay, S0-S4 or $\overline{CE}$ to valid CRUIN	C_L = 100 pF, R_L = 390 Ω		330		ns

4

4.0 INPUT, OUTPUT STRUCTURES

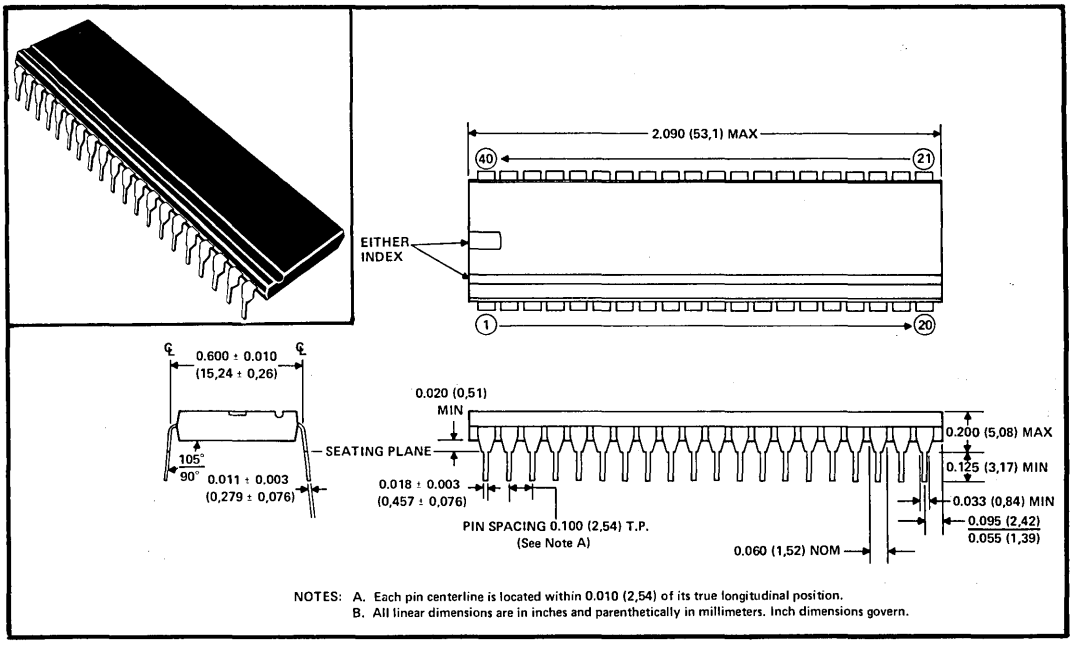


PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

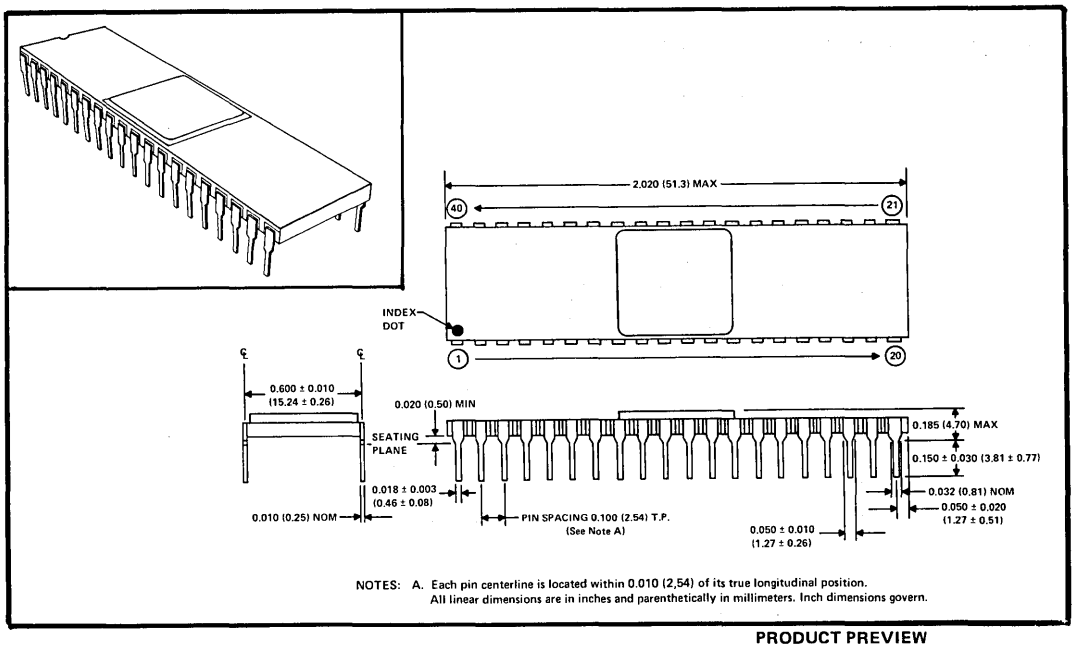
5.0 MECHANICAL DATA

5.1 40-PIN PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. Each pin centerline is located within 0.010 (2,54) of its true longitudinal position.
B. All linear dimensions are in inches and parenthetically in millimeters. Inch dimensions govern.

5.2 40-PIN CERAMIC DUAL-IN-LINE PACKAGE



NOTES: A. Each pin centerline is located within 0.010 (2,54) of its true longitudinal position.
All linear dimensions are in inches and parenthetically in millimeters. Inch dimensions govern.

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

SBP 9964
Timing Controller

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TIMING CONTROLLER FOR THE SBP9900A

1. INTRODUCTION

1.1 KEY FEATURES

- 14-Bit Interval Timer-Event Counter
- RESET, HOLD, and LOAD synchronization
- SBP9900A clock generation
- 24-pin package
- TTL-compatible, open-collector I/O

1.2 DESCRIPTION

The SBP9964 is a 14-bit, interval timer/event counter, an SBP9900A clock generator, and an SBP9900A RESET, HOLD, and LOAD signal synchronizer. The interval timer-event counter communicates with the SBP9900A/SBP9989 through the SBP9900A/SBP9989 Communication Register Unit (CRU) I/O interface. The interval timer/event counter may be efficiently applied to a variety of applications in which timing the interval between external events, counting the number of external events, or initiating periodic events is desired. RESET, HOLD, and LOAD synchronizers provide for SBP9900A compatible synchronization of these signals from asynchronously applied external signals.

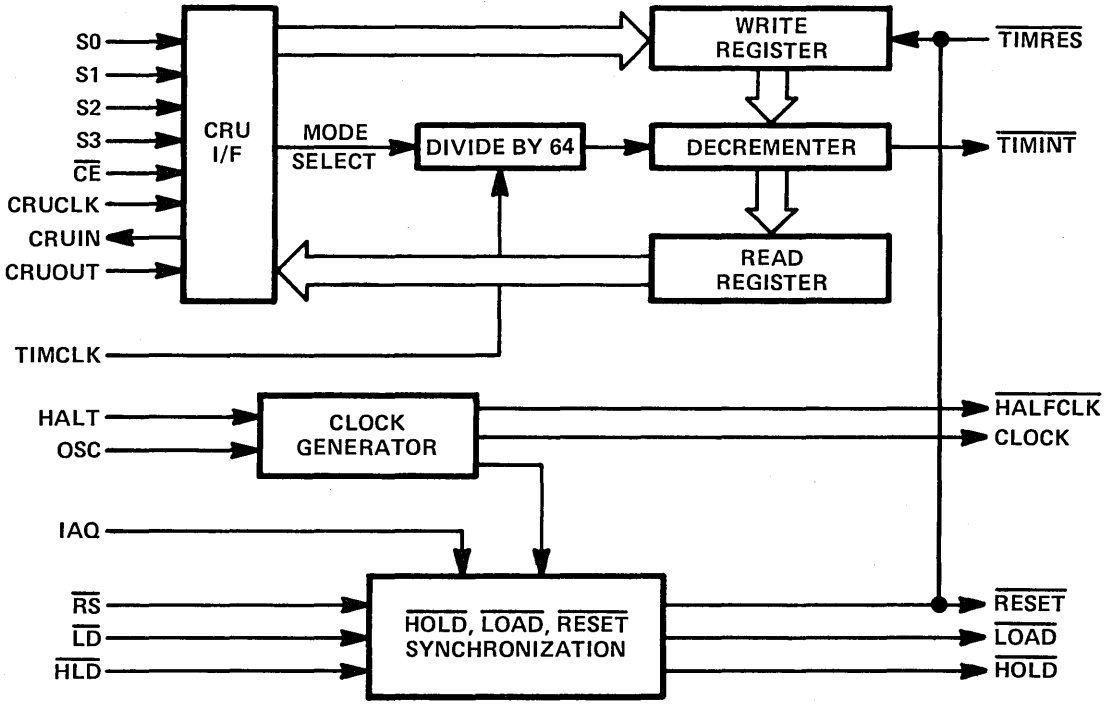
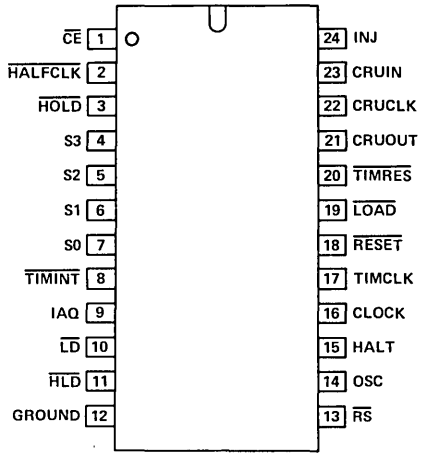


FIGURE 1 – SBP9964 INTERNAL STRUCTURE

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

2. SBP9964 PIN ASSIGNMENTS



3. SBP9964 PIN DESCRIPTIONS

SIGNATURE	PIN	I/O	DESCRIPTION
INJ	24		Injector Current Source
GND	12		Ground Reference
$\overline{CE}$	1	IN	Chip Enable: When active (low), S0-S3 select the CRU bit that is to be read or written to by the CPU. Additionally, when $\overline{CE}$ is active, the read register retains its current value and is not affected by decrementer operation until $\overline{CE}$ becomes inactive (high).
S0	7	IN	Select Lines: When $\overline{CE}$ is active (low), S0-S3 select one of 16 CRU bits to be read or written to (see Table 1).
S1	6	IN	
S2	5	IN	
S3	4	IN	
CRUIN	23	OUT	CRU Data In: When $\overline{CE}$ is active (low), data specified by S0-S3 is transmitted to the 9900A/9989 by CRUIN. When $\overline{CE}$ is not active (high), CRUIN is logic-level high.
CRUOUT	21	IN	CRU Data Out: When $\overline{CE}$ is active (low), data present on the CRUOUT input is sampled during CRUCLK and written into the CRU bit specified by S0-S3.
CRUCLK	22	IN	CRU Clock: CRUCLK specifies that valid data is present on the CRUOUT line.
$\overline{TIMRES}$	20	IN	Timer Reset: When active (low), the Timer write-register is cleared (all zeros) disabling the timer, and the INTMSK bit (bit 15) is set to zero disabling the interrupt.
$\overline{HALFCLK}$	2	OUT	The $\overline{HALFCLK}$ output has the same frequency and duty cycle as the clock, but the rising edge of the signal occurs midway between rising and falling edge of the CLOCK output signal.
HALT	15	IN	An active signal on this input halts the CLOCK before the next negative transition.
$\overline{TIMINT}$	8	OUT	Timer Interrupt: If the INTMSK bit is set to one (bit 15), and, if the decrementer decrements to zero, $\overline{TIMINT}$ will become active (low). $\overline{TIMINT}$ remains active until the INTMSK bit is rewritten into or is reset using $\overline{TIMRES}$ or RS.
$\overline{RS}$	13	IN	$\overline{RESET}$ Sense Input: A negative transition occurring on this input causes the internal timer and $\overline{LOAD}$ registers to be reset, and also causes an active signal, synchronous with the CLOCK, to be placed on the $\overline{RESET}$ output.
$\overline{RESET}$	18	OUT	$\overline{RESET}$ Output: The $\overline{RESET}$ output is synchronously active with the CLOCK output when an active signal (low) is placed on $\overline{RS}$.

SIGNATURE	PIN	I/O	DESCRIPTION
$\overline{LD}$	10	IN	$\overline{LOAD}$ Sense Input: A negative transition occurring on this input causes $\overline{LOAD}$ to become active until two IAQ pulses are received from the SBP9900A.
IAQ	9	IN	Instruction Acquisition: This input from the SBP9900A is used to determine the active time of the $\overline{LOAD}$ signal.
$\overline{LOAD}$	19	OUT	$\overline{LOAD}$ Output: The $\overline{LOAD}$ output is synchronized with the CLOCK upon the occurrence of a high-to-low transition on the $\overline{LD}$ input. $\overline{LOAD}$ remains active until two IAQ pulses have been received.
$\overline{HLD}$	11	IN	$\overline{HOLD}$ Sense Input: A negative transition on this input causes $\overline{HOLD}$ to become active synchronously with the CLOCK.
$\overline{HOLD}$	3	OUT	$\overline{HOLD}$ Output: The $\overline{HOLD}$ output becomes synchronously active with the CLOCK when a negative transition occurs on $\overline{HLD}$.
TIMCLK	17	IN	Timer Clock: External clock used for the internal timer or event counter.
OSC	14	IN	Oscillator Input: An oscillator input of three times the desired CLOCK output and having a 50 percent duty cycle is used to generate the SBP9900A CLOCK input.
CLOCK	16	OUT	CLOCK output: This output is SBP9900A-compatible CLOCK input, which is one-third of the OSC input frequency. This output has a 67 percent duty cycle.

TABLE 1 – TIMER BIT ASSIGNMENT

	BIT ADDRESS					
BIT	S0	S1	S2	S3	WRITE REGISTER DATA	READ REGISTER DATA
0	0	0	0	0	CLK1	CLK1
1	0	0	0	1	CLK2	CLK2
2	0	0	1	0	CLK3	CLK3
3	0	0	1	1	CLK4	CLK4
4	0	1	0	0	CLK5	CLK5
5	0	1	0	1	CLK6	CLK6
6	0	1	1	0	CLK7	CLK7
7	0	1	1	1	CLK8	CLK8
8	1	0	0	0	CLK9	CLK9
9	1	0	0	1	CLK10	CLK10
10	1	0	1	0	CLK11	CLK11
11	1	0	1	1	CLK12	CLK12
12	1	1	0	0	CLK13	CLK13
13	1	1	0	1	CLK14	CLK14
14	1	1	1	0	MODE[1]	MODE[1]
15	1	1	1	1	INTMSK[2]	$\overline{TIMINT}$

[1]MODE = 0 interval timer mode; MODE = 1 event counter mode.
[2]INTMSK = 0 TIMINT will not be active when Decrementer = 0;
INTMSK = 1 TIMINT will be latched active when Decrementer = 0.

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

4. ELECTRICAL SPECIFICATIONS

4.1 RECOMMENDED OPERATING CONDITIONS

PARAMETER		MIN	NOM	MAX	UNIT
Supply current, I_{CC}		115	130	145	mA
High-level output voltage, V_{OH}				5.5	V
Low-level output current, I_{OL}				12	mA
Operating free-air temperature, T_A	SBP9964CJ	0		70	°C
	SBP9964NJ	–55		125	

4.2 TIMING REQUIREMENTS OVER FULL RANGE OF OPERATING CONDITIONS

	PARAMETER	MIN	NOM	MAX	UNIT
$t_{c(OSC)}$	Oscillator cycle time		110		ns
t_{TC}	TIMCLK cycle time		100		ns
$t_{w(RS)}$	Width of reset pulse		100		ns
$t_{w(HLD)}$	Width of hold pulse		100		ns
$t_{w(LD)}$	Width of load pulse		100		ns
$t_{su(A)}$	Setup time for S0-S3, CE, or CRUOUT		200		ns
t_{su}	Setup time, hold before clock		100		ns
$t_{w(CRUCLK)}$	CRU clock pulse width		100		ns
t_h	Hold time for address or data		100		ns

SBP 9965 Peripheral Interface Adapter

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

PERIPHERAL INTERFACE ADAPTOR

1. INTRODUCTION

1.1 GENERAL DESCRIPTION

The SBP9965 Peripheral Interface Adaptor is a byte-oriented parallel input/output device that interfaces with the CPU through the memory bus. This technique allows parallel transfers of data between the peripheral device and the CPU, increasing throughput rate to memory bus speeds.

The SBP9965 is a ruggedized, monolithic, software-configurable input/output device fabricated with oxide-separated Integrated Injection Logic (I^2L) technology.

Built into the SBP9965 are internal mask registers from which an interrupt may be asserted when the input/output data is equal to the mask register data. This feature is useful for CPU- or DMA-initiated byte search operations as well as special character recognition schemes on input/output data.

1.2 KEY FEATURES

- SBP9900A/SBP9989 memory-mapped peripheral
- Dual 8-bit input/output peripheral ports
- Two-Wire Handshake Control (each port)
- Dual Port Mask Registers
- 40-pin package
- Wide ambient temperature operating range

  SBP9965NJ: $-55^{\circ}C$ to $+125^{\circ}C$ (screened to MIL-STD-883B)

  SBP9965CJ: $0^{\circ}C$ to $+70^{\circ}C$
- I^2L technology
  - Single dc power source
  - Fully static operation
  - Wide temperature stability
  - TTL-compatible, open-collector I/O

4

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

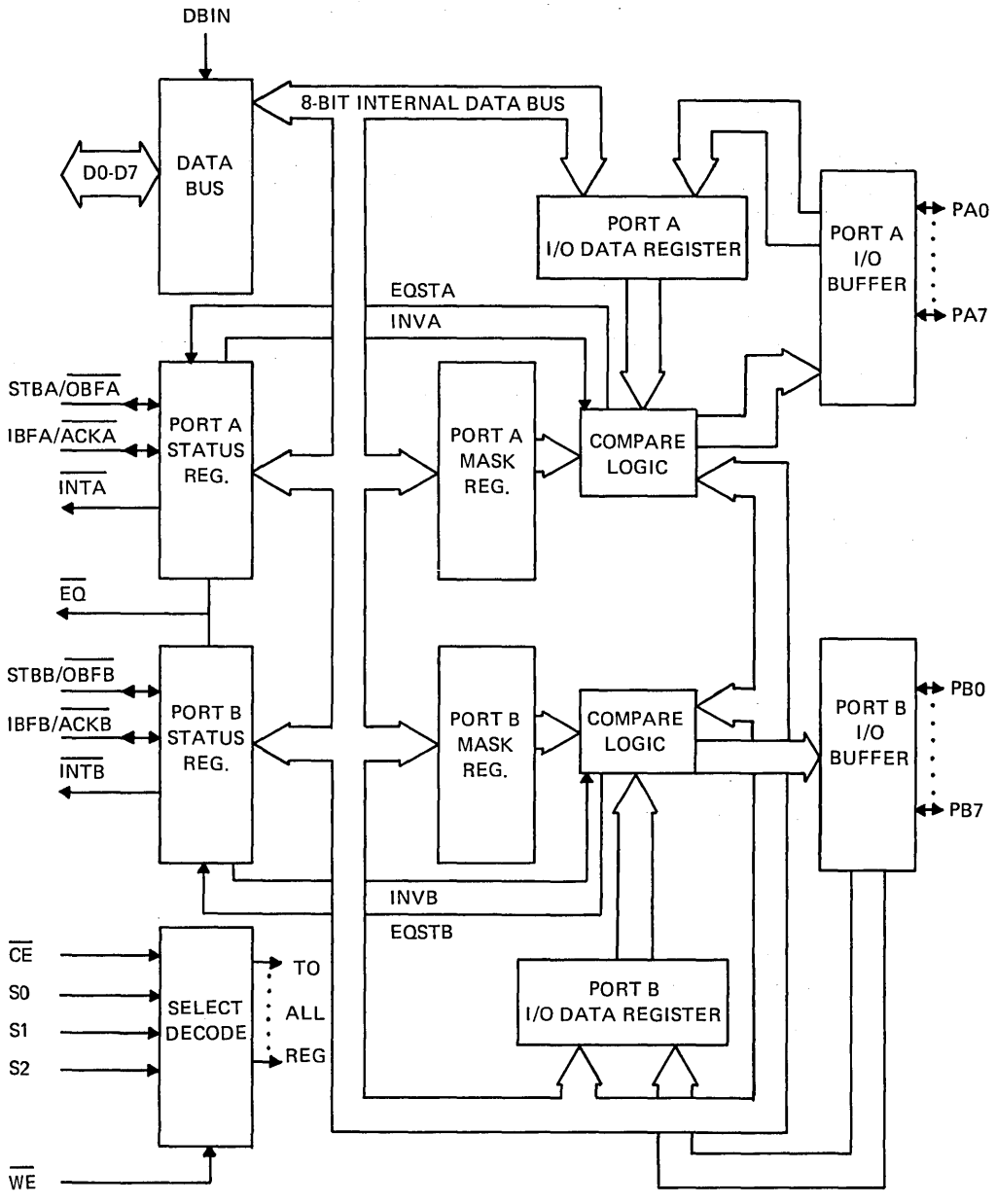


FIGURE 1 – FUNCTIONAL BLOCK DIAGRAM, SBP9965 INTERNAL STRUCTURE

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

2. FUNCTIONAL DESCRIPTION

2.1 REGISTERS

Figure 1 diagrams the internal structure of the SBP9965. Note there are six internal 8-bit registers, which are defined in the following pages. Table 1 tabulates the bit assignments and the select address for each register.

TABLE 1 – SBP9965 INTERNAL REGISTERS

S0	S1	S2	REGISTER NAME	BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
0	0	0	PORT A I/O DATA REG	PA0	PA1	PA2	PA3	PA4	PA5	PA6	PA7
0	0	1	PORT A STATUS REG	$\overline{OBFA}$	IBFA	IOSELA	INTMSKA	EQSTA	EQMSKA	INVA	
0	1	0	PORT A MASK REG	MSKA0	MSKA1	MSKA2	MSKA3	MSKA4	MSKA5	MSKA6	MSKA7
0	1	1	PORT B I/O DATA REG	PB0	PB1	PB2	PB3	PB4	PB5	PB6	PB7
1	0	0	PORT B STATUS REG	$\overline{OBFB}$	IBFB	IOSELB	INTMSKB	EQSTB	EQMSKB	INVB	
1	0	1	PORT B MASK REG	MSKB0	MSKB1	MSKB2	MSKB3	MSKB4	MSKB5	MSKB6	MSKB7

2.1.1 Port A and Port B I/O Data Registers

The Port A and Port B I/O data registers hold data that is transferred between the CPU and the peripheral device. When a port is in the output mode, the I/O data registers are loaded with data from the D0-D7 data bus on the rising edge of $\overline{WE}$. When a port is in the input mode, data is loaded from PA/B0 – PA/B7 on the rising edge of STBA/B input line from a peripheral device.

2.1.2 Port A Status Register

The Port A status register contains configuration and status bits with which the CPU may control the operation of Port A I/O's. Note that (See Figure 1, Table 1) the first two bits of this register, OBF and IBF, represent external signal functions; all the other bits function internally. The Port A status register bit descriptions follow.

$\overline{\text{OBFA}}$ (Bit 0) (Output Mode)	Output Buffer Full A: This bit is set to "0" on the rising edge of the $\overline{\text{WE}}$ input, indicating that the CPU has written data to the Port A output port. Thus output signal $\overline{\text{OBFA}}$ (pin 11) goes active (low) as a direct result. The peripheral indicates receipt of data by sending an active (low) signal to the acknowledge input $\overline{\text{ACKA}}$ of the 9965. This sets bit 0 ($\overline{\text{OBFA}}$) to "1", causing $\overline{\text{OBFA}}$ output signal to go inactive (high).
(Input Mode)	Bit 0 ($\overline{\text{OBFA}}$) is set to "1", causing $\overline{\text{OBFA}}$ output signal to be inactive (high).
IBFA (Bit 1)	Input Buffer Full A: This bit indicates when the peripheral device has loaded data into the port A I/O data register. IFBA is set to "1" on the rising edge of the STBA input from the peripheral. IBFA output signal goes active as a direct result. When the CPU has read the contents of Port A I/O data register, Bit 1 (IBFA) is set to "0" causing IBFA (pin 12) to become inactive.
IOSELA (Bit 2)	Port A I/O Select: A "0" (low) written into this bit position configures Port A as an input port. A "1" (high) written into this bit position configures Port A as an output port.
INTMSKA (Bit 3)	Port A Interrupt Mask: A "1" written into this bit position enables generation of an active (low) interrupt signal upon the occurrence of the rising edge of STBA when in the input mode, or upon the falling edge of $\overline{\text{ACKA}}$ when in the output mode. The interrupt may be cleared by reading Port A I/O data register in the input mode, or by writing to Port A I/O data register when in the output mode.
EQSTA (Bit 4)	Port A Equal Status: When the data in the Port A I/O data register equals the data in Port A mask register, the EQSTA bit will be "1". If these two values are not equal, EQSTA = 0. EQSTA is not affected by the EQMSKA bit (Bit 5). EQSTA is cleared only by satisfying an inequality condition between the data register and the mask register.
EQMSKA (Bit 5)	Port A Equal Status Output Mask: When EQMSKA = 0, the equal status of Port A is inhibited from affecting the $\overline{\text{EQ}}$ output pin. If EQMSKA = 1, the $\overline{\text{EQ}}$ will become active when an equal condition exists between Port A I/O data register and Port A Mask Register. The $\overline{\text{EQ}}$ output may be reset (high) if (1) Port B equal status is not affecting this output, (2) if Port A equal status is inhibited through EQMSKA or (3) if an inequality condition is setup between the I/O data register and the mask register.
INVA (Bit 6)	Invert Port A Data: When INVA = 1, data in the Port A I/O data register is inverted prior to outputting on the D0-D7 data bus when in the input mode, or inverted prior to outputting on PA0-PA7 when in the output mode. If INVA = 0, data is unaffected.

2.1.3 Port B Status Register

Port B status register is functionally identical to the Port A status register. It controls Port B operation.

2.1.4 Mask Register A and Mask Register B

These mask registers are used in conjunction with the Port A and Port B I/O data registers and internal compare logic to generate the EQST bits of the status registers and to generate the $\overline{\text{EQ}}$ output when enabled by the EQMSK bits.

2.2 RESET CONFIGURATION

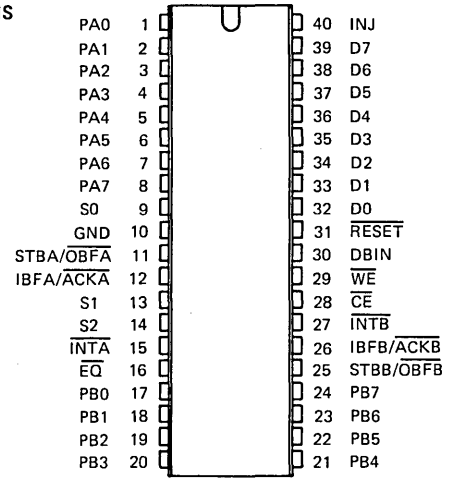
An active (low) signal on the $\overline{\text{RESET}}$ pin (31) of the SBP9965 caused the unit to assume a known I/O configuration as detailed in Table 2. $\overline{\text{RESET}}$ will ordinarily be asserted by the system environment during power-up sequencing.

TABLE 2 – SBP9965 RESET CONFIGURATION

REGISTER NAME	BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
PORT A I/O DATA REG	X	X	X	X	X	X	X	X
PORT A STATUS REG	1	0	0	0	1	0	0	X
PORT A MASK REG	X	X	X	X	X	X	X	X
PORT B I/O DATA REG	X	X	X	X	X	X	X	X
PORT B STATUS REG	1	0	0	0	1	0	0	X
PORT B MASK REG	X	X	X	X	X	X	X	X

X = Don't care

3. SBP9965 PIN DESCRIPTIONS



SIGNATURE	PIN	I/O	DESCRIPTION
INJ	40	PWR	Injector Current Source
GND	10	PWR	Ground Reference
$\overline{CE}$	28	IN	Chip Enable: When $\overline{CE}$ is active (low), the internal register, addressed by S0, S1, and S2, may be read or written to by the CPU.
$\overline{WE}$	29	IN	Write Enable: Data on D0-D7 is written by the CPU to the register addressed by S0, S1, and S2 on the falling edge of $\overline{WE}$ when $\overline{CE}$ is active.
DBIN	30	IN	Data Bus Enable: When $\overline{CE}$ and DBIN are active (high), the contents of the register addressed by S0, S1, and S2 are output on D0-D7 to the CPU.
S0	9	IN	Select Lines: S0, S1, and S2 address the register to be read or written to by the CPU when $\overline{CE}$ is active.
S1	13	IN	
S2	14	IN	

SIGNATURE	PIN	I/O	DESCRIPTION
PA0-PA7	1-8	I/O	I/O Port A: When IOSELA of the Port A I/O status register is a "1", PA0-PA7 serve as the Port A output data port. When IOSELA = 0, PA0-PA7 serve as Port A input data lines.
PB0-PB7	17-24	I/O	I/O Port B: When IOSELB of the Port B I/O status register is a "1", PB0-PB7 serve as the Port B output data port. When IOSELB = 0, PB0-PB7 serve as Port B input data lines.
STBA/$\overline{\text{OBFA}}$	11	I/O	Input Strobe A/Output Buffer Full A: When Port A is in the input mode, STBA serves as an input strobe from the peripheral device, which loads data into the Port A I/O data register on the rising edge of STBA. When Port A is in the output mode, $\overline{\text{OBFA}}$ serves as an output to the peripheral device indicating that the Port A I/O data register has been loaded with output data by the CPU. $\overline{\text{OBFA}}$ is cleared inactive by an active $\overline{\text{ACKA}}$ input from the peripheral device acknowledging receipt of output data.
STBB/$\overline{\text{OBFB}}$	25	I/O	Input Strobe B/Output Buffer Full B: Same STBA/$\overline{\text{OBFA}}$ except applies to Port B operation.
IBFA/$\overline{\text{ACKA}}$	12	I/O	Input Buffer Full A/Acknowledge A: When Port A is in the input mode, IBFA serves as an output that becomes active (high) on the rising edge of STBA and is reset inactive when the CPU reads the input data from the Port A I/O data register. When Port A is in the output mode, $\overline{\text{ACKA}}$ is an input to the SBP9965 from the peripheral device to acknowledge receipt of output data.
IBFB/$\overline{\text{ACK}}$	26	I/O	Input Buffer Full B/Acknowledge B: Same as IBFA/$\overline{\text{ACKA}}$ except applies to Port B operation.
D0-D7	32-39	I/O	Bidirectional Data Bus: This bidirectional, 8-bit, data bus connects to the CPU memory data bus for data transfers between the CPU memory and the SBP9965. The direction of D0-D7 is controlled by DBIN.
$\overline{\text{INTA}}$	15	OUT	Port A Interrupt Output: The $\overline{\text{INTA}}$ output is enabled when INTMSKA = 1 and becomes active (low) on the rising edge of STBA in the input mode or on the falling edge of $\overline{\text{ACKA}}$ in the output mode. $\overline{\text{INTA}}$ is cleared by reading or writing to the Port A I/O data register.
$\overline{\text{INTB}}$	27	OUT	Port A Interrupt Output: Same as $\overline{\text{INTA}}$, but applies to Port B operation.
$\overline{\text{EQ}}$	16	OUT	Equal Status Output: This output is the result of a logical OR between the Port A equal status and Port B equal status. Each port's equal status may be individually masked off through the EQMSKA and EQMSKB bits of the respective status registers. To clear an active (low) $\overline{\text{EQ}}$ output, the output must be, disabled through the EQMSK bit of the port causing the active level. Alternatively an unequal condition must be established between the mask register and I/O port causing the active level by changing either the mask value or the port I/O data register value. Figure 2 is a logic representation of the output source to the $\overline{\text{EQ}}$ pin.
$\overline{\text{RESET}}$	31	IN	Power-On Reset: $\overline{\text{RESET}}$ is used upon power-up to reset the SBP9965 to a known, inactive state. Table 2 shows the reset condition of the SBP9965.

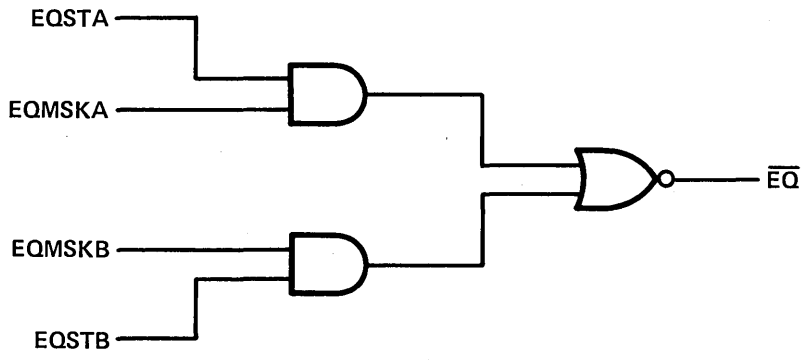


FIGURE 2 – $\overline{EQ}$ (EQUAL) GENERATOR

4.1 RECOMMENDED OPERATING CONDITIONS, I_{CC} = 130 mA (UNLESS OTHERWISE NOTED)

PARAMETER		MIN	NOM	MAX	UNITS
Supply current, I_{CC}	V_{INJ} = 1.2 V TYP	115	130	145	mA
High-level output voltage, V_{OH}				5.5	V
Low-level output current, I_{OL}				12	mA
Operating free-air temperature, T_A	SBP9965CJ	0		70	°C
	SBP9965NJ	–55		125	

4.2 ELECTRICAL CHARACTERISTICS OVER RECOMMENDED FREE-AIR TEMPERATURE RANGE UNLESS OTHERWISE NOTED)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	I_{CC} = 115 mA,	I_I = –12 mA			–1.5	V
I_{OH}	High-level output current	I_{CC} = 130 mA, V_{IL} = 0.8 V,	V_{IH} = 2 V V_{OH} = 5.5 V			–250	μA
V_{OL}	Low-level output voltage	I_{CC} = 130 mA, V_{IL} = 0.8 V,	V_{IH} = 2 V I_{OL} = 12 mA			0.5	V
I_I	Input current	I_{CC} = 130 mA,	V_I = 5.5 V		600	1000	μA

† All typical values are at I_{CC} = 130 mA, T_A = 25°C.

4.3 TIMING REQUIREMENTS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS

PARAMETER		MIN	NOM	MAX	UNIT
$t_{h(AD)}$	Hold time, select after $\overline{WE}$ inactive	300			ns
$t_{h(DA)}$	Hold time, data after $\overline{WE}$ active	100			ns
$t_{w(ACK)}$	Acknowledge pulse width	150			ns
$t_{w(WE)}$	Write enable pulse width	100			ns
$t_{w(STB)}$	Strobe pulse width	100			ns
$t_{su(AD)}$	Setup time, select before $\overline{WE}$ active	75			ns
$t_{su(DA)}$	Setup time, data before $\overline{WE}$ active	0			ns
$t_{su(DS)}$	Setup time, data before STB	50			ns
$t_{h(DS)}$	Hold time, data after strobe active	75			ns

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

4.4 SWITCHING CHARACTERISTICS, R_L = 390 Ω, C_L = 100 pF

PARAMETER	FROM	TO	MODE	MIN	TYP†	MAX	UNIT
t_{PD1}	$\overline{WE}$	Port Outputs	Output mode		220		ns
t_{PD2}	$\overline{WE}$	STB/$\overline{OBF}$ Low	Output mode		300		ns
t_{PD3}	$\overline{WE}$	$\overline{EQ}$ Active	Output mode		280		ns
t_{PD4}	IBF/$\overline{ACK}$ Low	STB/$\overline{OBF}$ High	Output Mode		130		ns
t_{PD5}	IBF/$\overline{ACK}$ Low	$\overline{INT}$ Active	Output mode		170		ns
t_{PD6}	S0-S2	Bus Outputs	Output mode		220		ns
t_{PD7}	$\overline{CE}$ (Strobe High)	Bus Outputs Enabled	Output mode		220		ns
t_{PD8}	$\overline{CE}$ (Strobe High)	Bus Outputs Disabled	Output mode		110		ns
t_{PD9}	DBIN	Bus Outputs Enabled	Output mode		220		ns
t_{PD10}	DBIN	Bus Outputs Disabled	Output mode		70		ns
t_{PD11}	STB/$\overline{OBF}$ High ($\overline{CE}$ Low)	Bus Outputs Enabled	Input mode		240		ns
t_{PD12}	STB/$\overline{OBF}$ High	IBF/$\overline{ACK}$ High	Input mode		130		ns
t_{PD13}	STB/$\overline{OBF}$ High	$\overline{INT}$ Low	Input mode		160		ns
t_{PD14}	STROBE	$\overline{EQ}$ Active	Input mode		280		ns
t_{PD15}	$\overline{CE}$, S0-S2	IBF/$\overline{ACK}$ Low	Input mode		270		ns
t_{PD16}	$\overline{CE}$, S0-S2	$\overline{INT}$ Inactive	Input mode		230		ns
t_{PD17}	$\overline{RESET}$	Input mode			170		ns

†All typical values are at T_A = 25°C

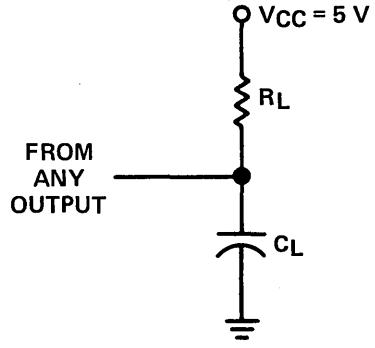
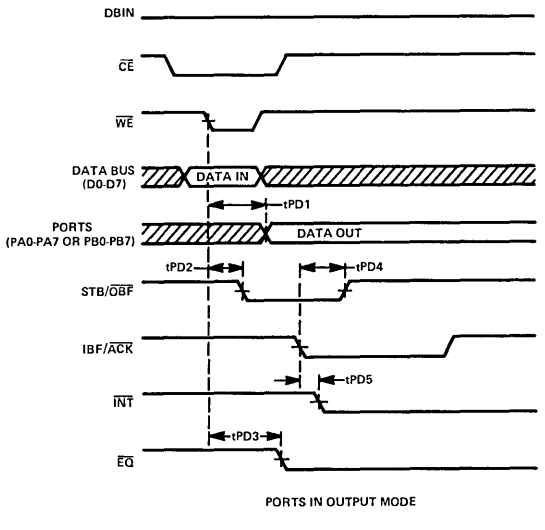


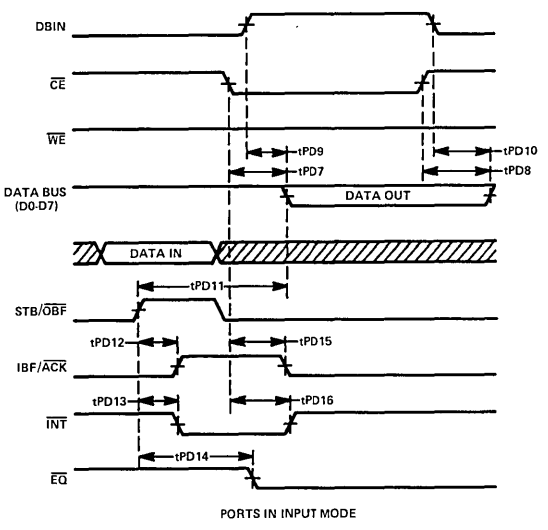
FIGURE 3 – SWITCHING TIME LOAD CIRCUIT

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

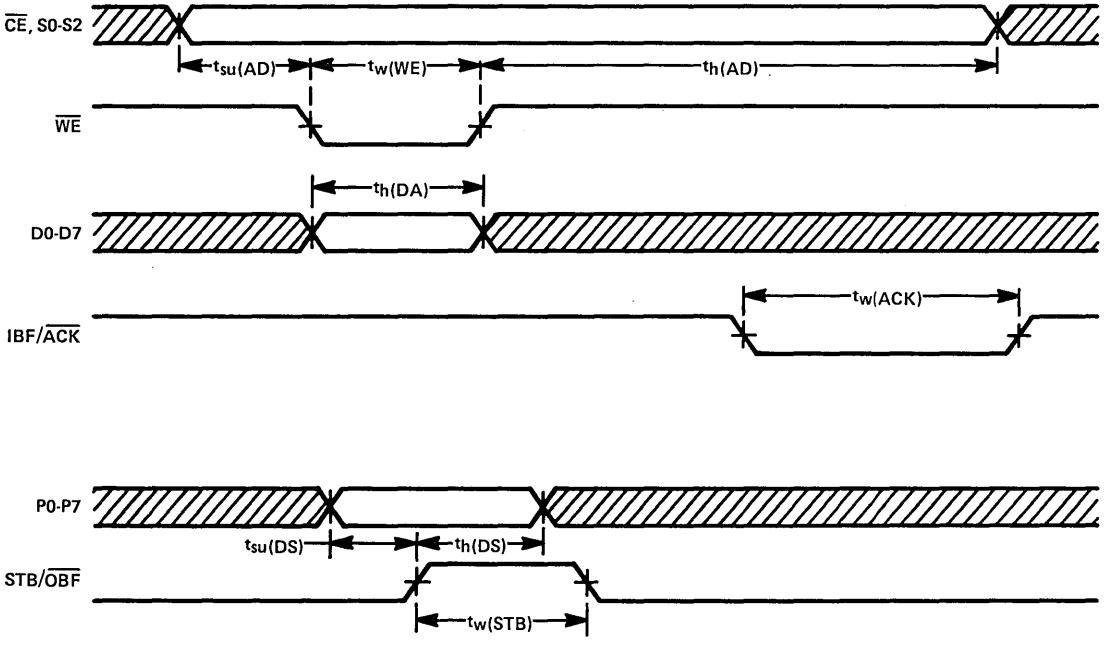


PORTS IN OUTPUT MODE



PORTS IN INPUT MODE

4



TIMING REQUIREMENTS

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

SBP 9989 Microprocessor

Texas Instruments invented the integrated circuit, microprocessor and microcomputer, which have made TI synonymous with reliability, affordability, and compactness. The SBP9989 16-bit microprocessor carries on TI's tradition of technology leadership.

INTRODUCTION

The 9900 Family

The 9900 Family is a compatible set of microprocessors, microcomputers, microcomputer modules, and minicomputers. It is supported with peripheral devices, development systems, and software and provides the designer with a system solution that has built-in protection against technological obsolescence. The family features true software compatibility, I/O bus compatibility and price/performance ratios which encompass a wide range of applications. The family is designed with a unique flexible architecture to allow technological changes to be easily incorporated while minimizing the impact these changes have on an overall system design.

The SBP9989 I^2L 16-Bit Microprocessor

The SBP9989 is a second-generation, bipolar 16-bit microprocessor offering twice the performance of the original SBP9900A. Implemented in TI's Advanced I^2L Technology, the SBP9989 combines environmental ruggedness and inherent reliability with a 16-bit word length, an advanced memory-to-memory architecture, and a full minicomputer instruction set to extend the end application reach of the Texas Instruments 9900 microprocessor family into those applications requiring efficient, stable, reliable performance in severe operating conditions.

The instruction set of the SBP9989 includes the capabilities offered by full minicomputers and is a superset of the 9900 instruction repertoire. The SBP9989 can be used to upgrade existing SBP9900A systems or to implement new system designs requiring the increased through-put and doubled memory capability.

KEY FEATURES

The SBP9989 is downward-compatible with all of TI's existing microcomputer and minicomputer products and employs the advanced, memory-to-memory architecture that ensures optimal performance in the structured, I/O-intensive applications of the 80's.

- Memory-to-memory architecture.
- 73 basic instructions include all 69 instructions of the SBP9900A plus Signed Multiply, Signed Divide, Load WP, and Load ST. The signed multiply and divide instructions allow significant improvements in system through-put in numerical applications, while load workspace register and load status register are essential to the efficient implementation of advanced operating systems.
- User extension to the basic instruction set allows undefined op codes to be assigned meanings during system design. The processor detects undefined op codes in an instruction stream and allows either software interpretation and execution of the code or hardware execution in special, user-designed "attached processors". Coordination between the SBP9989 and its attached processors is achieved via a new input signal to the microprocessor designated $\overline{\text{XIPP}}$ (External Instruction Processor Present).
- Direct access to 128 kilobytes of memory from the SBP9989 is provided by a new output signal designated $\overline{\text{MPEN}}$ (Memory Map Enable) which can be used directly as an additional address bit from the processor. This bit is represented in the processor Status Register as Status Bit 8, which may be manipulated by the user to allow access to two 64-kilobyte pages of memory. $\overline{\text{MPEN}}$ can also be used with the SN54LS610 Memory Mapper to allow access to as much as 16 megabytes of memory. All traps cause Status Bit 8 to be forced to zero during a context switch, ensuring consistent interrupt operation and full software and hardware compatibility with other TI products.
- Multiprocessor system features allow coordination between several processing elements that must share memory and other resources. These features include:

  MPILCK (Multiprocessor Interlock), a new output signal that allows a processor to secure and hold a system resource against possible access contention with other processing elements.

  INTACK (Interrupt Acknowledge), a new output signal which allows the SBP9989 to acknowledge the presence of an interrupt during those times when it may not have control of the system resources.

  $\overline{\text{XIPP}}$ (Extended Instruction Processor Present), a new input signal that establishes a protocol for orderly transfer of bus control between host and slave processors that share memory resources.

  LOAD WP and LOAD ST (Load Workspace Pointer and Load Status Register) instructions that allow the SBP9989 to capture a complete software context from an external source.

- Fully static design allows the SBP9989 to be clocked up to 4.4 MHz, or single stepped. The TTL-compatible I/O permits any standard logic and memory devices to be used.
- Simplified clock requirements consist of single-phase clock with a 50% duty cycle.
- Improved microcode within the processor enhances the efficiency of the SBP9989 over its predecessors. Microcycles were removed from more than half of the instructions, resulting in a 15% to 20% improvement in operating efficiency.
- Improved external instruction, utilizing five address lines, provides a total of 160 forms available to the user.
- Improved HOLD and WAIT interfaces.
- Implemented in Advanced I^2L . . . a proven bipolar technology for high-reliability applications.

The single most important feature of the SBP9989, and all of TI's microprocessors, is its memory-to-memory concept. The user has access to an unlimited number of effective registers, and may completely change register context (an operation equivalent to sixteen push and sixteen pop stack operations in a conventional registered architecture) in just five memory cycle times. The ability to change register content rapidly becomes of prime importance in systems that rely on multiprocessor architectures and high-level languages for efficient software . . . trends which will gain momentum as embedded computer applications become increasingly more complex.

DEVELOPMENT SUPPORT

AMPL System Advanced Microprocessor Prototyping Lab

The AMPL System is a complete set of software and hardware tools that maximize software productivity for the 9900 family. It includes a video display terminal, multiuser hard disk or floppy diskette options, and extensive software. Programs can be edited, assembled, loaded, and executed with easy self-prompting commands.

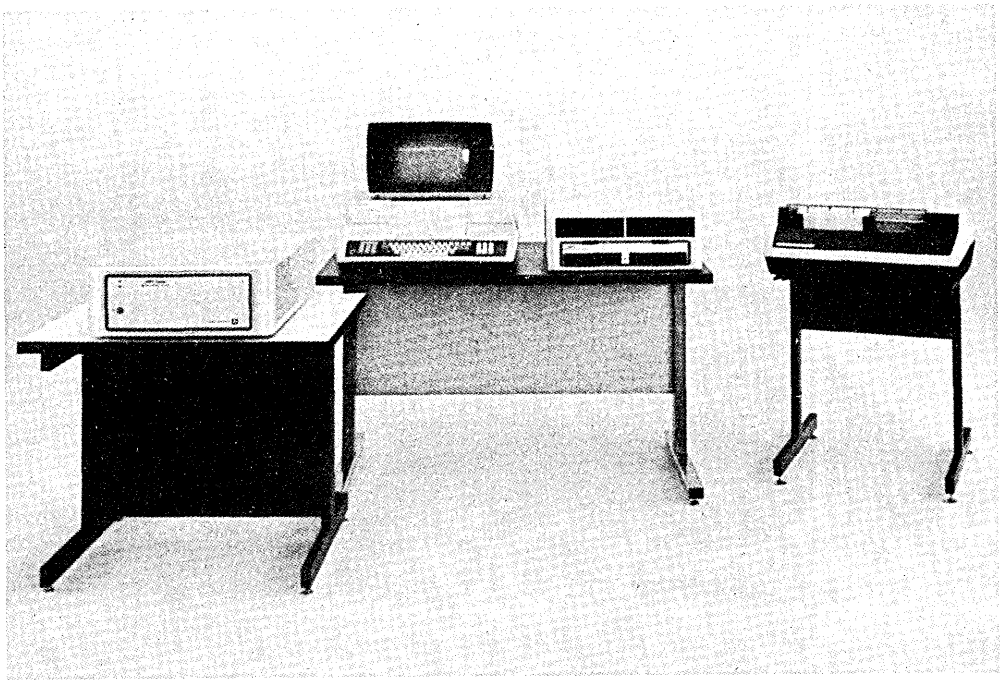
The AMPL system supports software development as well as in-circuit emulation for existing 9900 family CPU's. The logic-state trace capability features interactive on-line control and analysis to provide fast data reduction, and programmable emulation control based on the result of this analysis. The high-level language has designed-in features to simplify orientation for the new user while providing extensive flexibility and support for the experienced user.

PROM programming implements target-system memory in PROM and EPROM while the AMPL interactive process makes it easy to identify and implement needed design changes.

AMPL support for the SBP9989 is currently under development.

Transportable Assembler

The SBP9989 is supported by a transportable general assembler (TI part number TMAM4015). This assembler allows the use of symbolic instructions and assembler directives supporting the full instruction set. The 9900 family instruction set is composed of a base set of 69 instructions plus extensions peculiar to each CPU which provide the input and output manipulation comparison of words and bytes, and ASCII-character data. This product can be executed in TI 990, IBM, or DEC environments.



TMAM6011 – AMPL STATION

I^2L TECHNOLOGY

I^2L is an integrated-injection-circuit logic where current steering is used to control gate switching levels. A lateral PNP transistor is used as an injector to supply base current to the vertical NPN transistor as shown in the figure. The NPN actually serves as the gate that is controlled by placing either a high or low voltage on the base that steers the injector current into or out of the NPN base.

I^2L technology provides inherent advantages to the user when compared to other technologies.

- **–55°C to +125°C Temperature Range**

  Circuits are designed to operate over the full military temperature range of –55°C to +125°C rather than just being selected by screening. This provides added design margin that enhances system reliability.

- **Low Power Consumption**

  The SBP9989 dissipates less than 0.75 watts, depending upon the state of the I/O's.

- **Radiation Hardness**

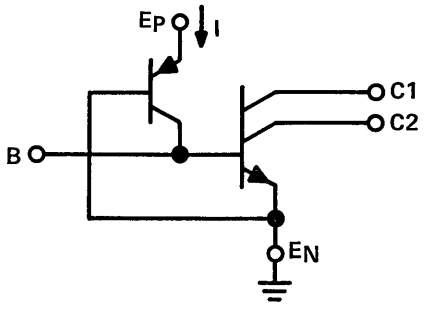
  Also inherent with I^2L as used on the SBP9989 is tolerance to radiation. It's tolerance to transient upset is among the best observed on LSI parts while the simplicity of the process eliminates latch-up.

- **Low Internal Stress Voltage**

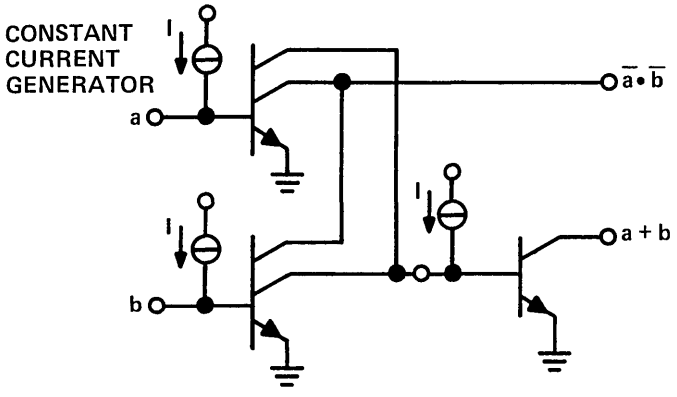
  High internal voltages have been eliminated with I^2L, thereby assuring further gains in reliability. The 5,000 internal gates of the SBP9989 are stressed only with the V_{INJ}, which is typically 1.2 volts. Only the inputs and outputs are exposed to high stress voltages.

- **High Reliability**

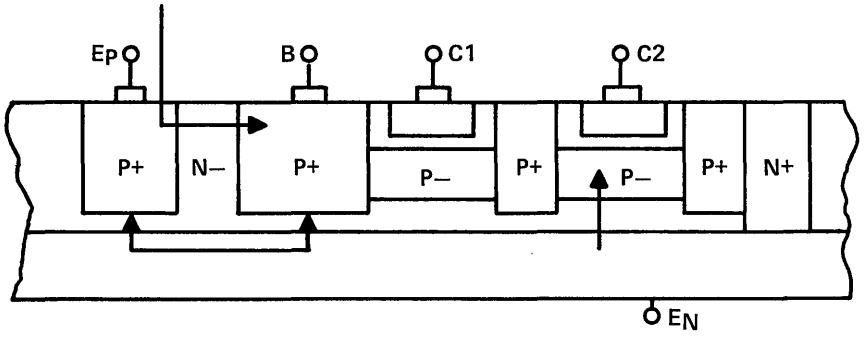
  While the SBP9989 has been designed and fabricated with processes to assure the highest levels of reliability, the SBP9989NJ is 100% processed to Method 5004 of MIL-STD-883B. Each part is individually identified to assure complete traceability and complete data availability.



I^2L CIRCUIT SCHEMATIC



I^2L LOGIC



I^2L DEVICE STRUCTURE

COMPATIBILITY WITH SBP9900A SYSTEMS

The SBP9989 is pin-for-pin compatible with the SBP9900A except for 4 new I/O controls ($\overline{\text{MPEN}}$, INTACK, MPILCK, and $\overline{\text{XIPP}}$) assigned to pins that were not used on the original device. The modifications required to plug an SBP9989 into an existing SBP9900A socket are listed below.

Hardware

- Deactivating $\overline{\text{XIPP}}$ (tie Pin 58 to V_{CC} through a pull-up resistor).
- Provision for an increase in injector voltage to 1.25 V and a reduction in injector current to 400 mA.
- Verifying that Pin 25 ($\overline{\text{MPEN}}$), Pin 37 (INTACK), and Pin 39 (MPILCK) are open or grounded.
- Verifying fan-out compatibility (I_{OL} = 20 mA for SBP9900A, I_{OL} = 16 mA for SBP9989).

Software

- Although software written for the SBP9900A can be executed by the SBP9989, a reduction of 15% to 20% in execution time should be anticipated. Software timing loops will need new time constants to compensate for the reduced execution times.
- Any unused op codes used as NOP's in the SBP9900A software will cause the SBP9989 to execute a level 2 interrupt trap.

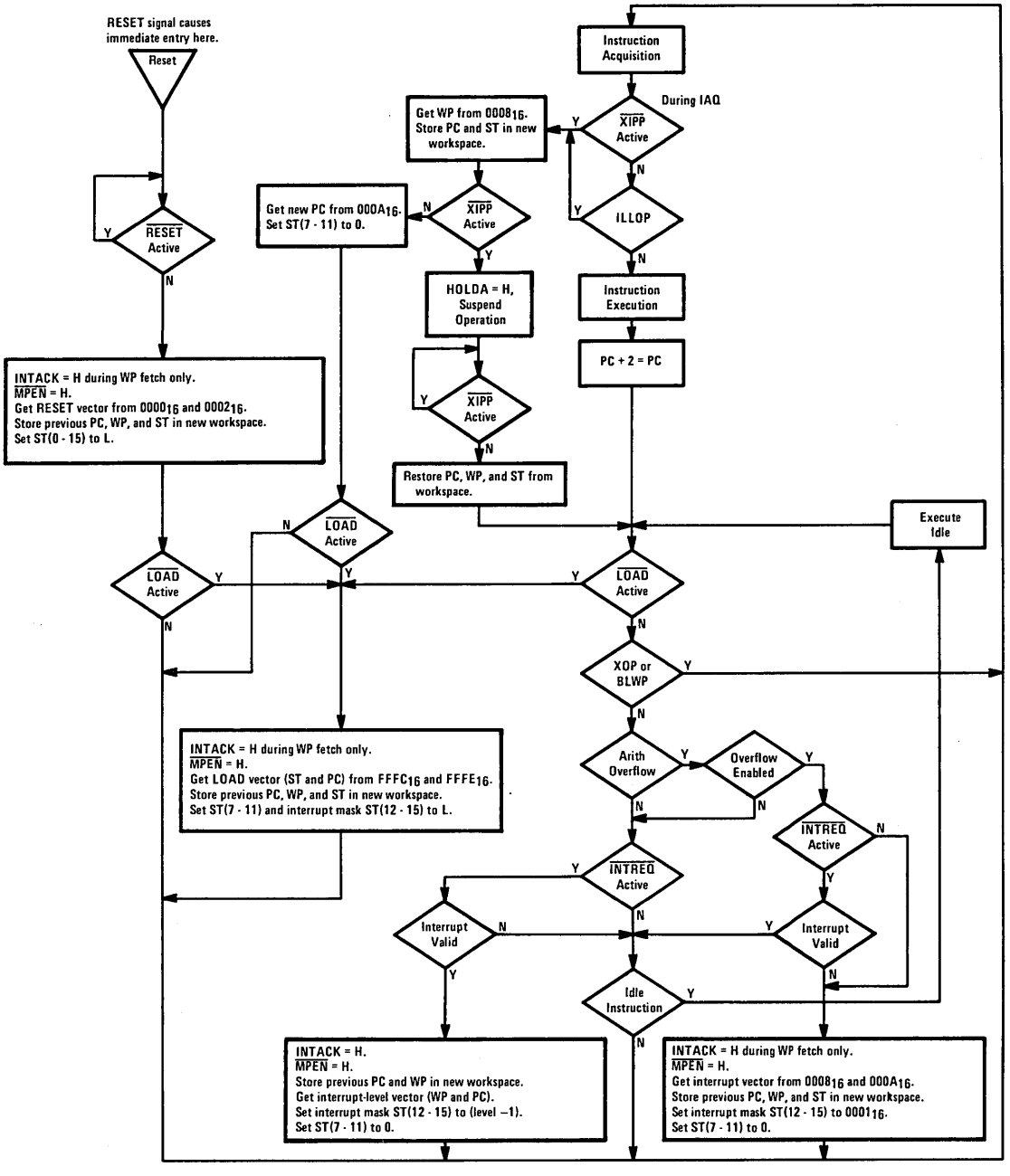
DEVICES FOR MILITARY-TEMPERATURE APPLICATIONS

The SBP9989 is a member of the ever growing family of military microprocessor components.

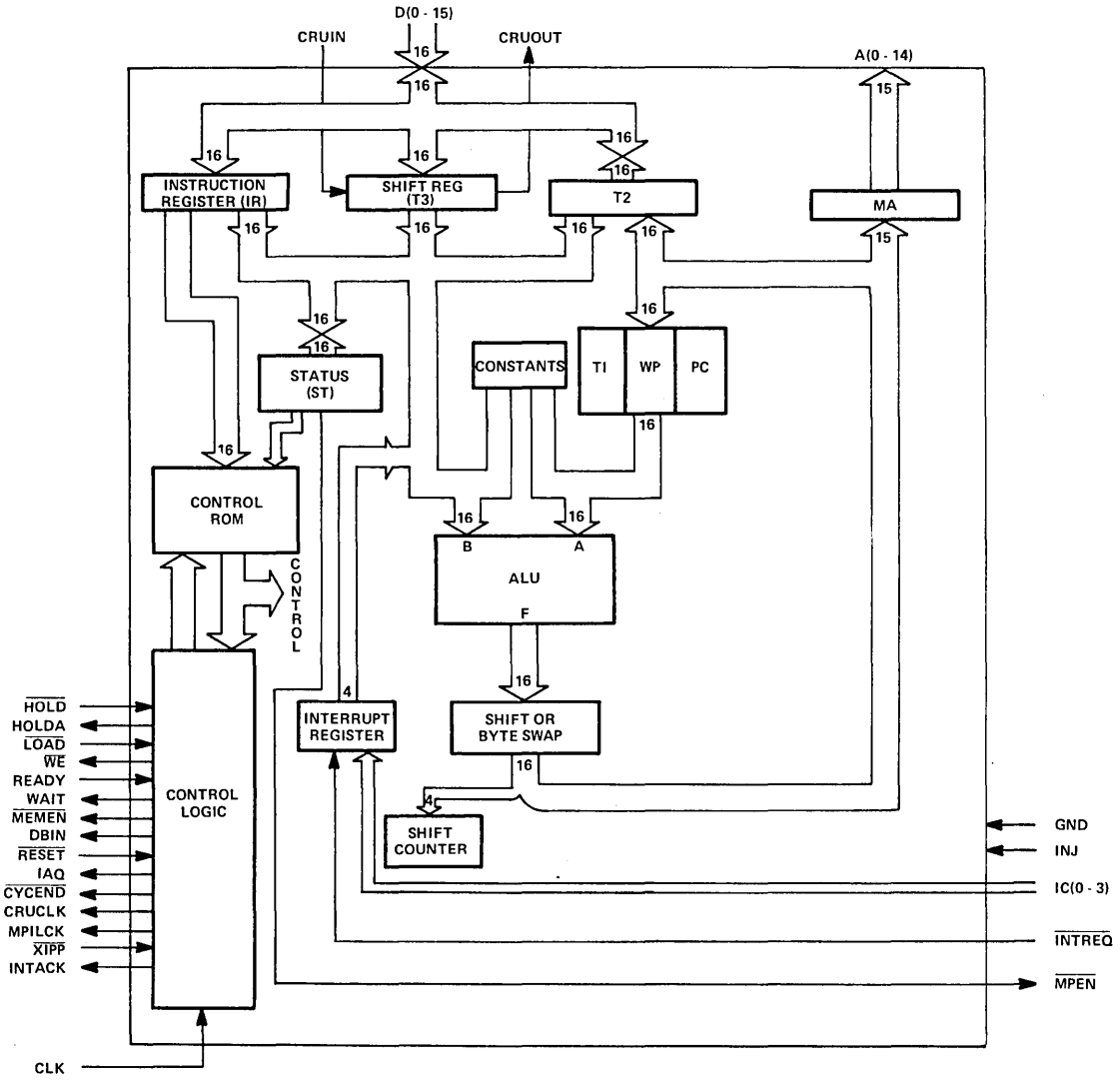
SBP9989	16-Bit Advanced Hi-Rel Microprocessor
SBP9900A	16-Bit Hi-Rel Microprocessor
SBP9960	Programmable CRU I/O Expander
SBP9961*	Interrupt Controller
SBP9964*	Timing Controller for the SBP9900A
SBP9965	Peripheral Interface Adapter
SN54LS124	Dual Voltage-Controlled Oscillator
SN54LS244	Octal Buffer/Line Driver/Line Receiver
SN54LS373	Octal D-Type Transparent Latch
SN54LS374	Octal D-Type Edge-Triggered Flip-Flop
SN54LS412	Multi-Mode Buffered Latches
SN54LS610	Memory Mapper
SN54LS630	16-Bit Parallel Error Detection and Correction Unit
SN54LS644	Octal Bus Transceiver
SN54LS645	Octal Bus Transceiver
SN54LS673	16-Bit Shift Register
SN54LS674	16-Bit Shift Register
SN54S189	64-Bit (16 x 4) RAM
SN54S287	1024-Bit (256 x 4) PROM
SN54S288	256-Bit (32 x 8) PROM
SN54S289	64-Bit (16 x 4) RAM
TBP18S030	256-Bit (32 x 8) PROM
TBP18S46	4096-Bit (512 x 8) PROM
TBP28L86	8192-Bit (1024 x 8) PROM
TBP28S86	8192-Bit (1024 x 8) PROM

*Under development.

FLOW CHART

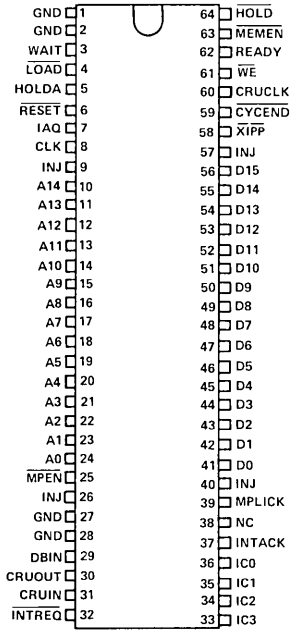

RESET signal causes immediate entry here.
Reset
RESET Active
Y
N
INTACK = H during WP fetch only.
MPEN = H.
Get RESET vector from 0000$_{16}$ and 0002$_{16}$.
Store previous PC, WP, and ST in new workspace.
Set ST(0 - 15) to L.
LOAD Active
INTACK = H during WP fetch only.
MPEN = H.
Get LOAD vector (ST and PC) from FFFC$_{16}$ and FFFE$_{16}$.
Store previous PC, WP, and ST in new workspace.
Set ST(7 - 11) and interrupt mask ST(12 - 15) to L.
Instruction Acquisition
During IAQ
XIPP Active
Get WP from 0008$_{16}$.
Store PC and ST in new workspace.
ILLOP
Get new PC from 000A$_{16}$.
Set ST(7 - 11) to 0.
HOLDA = H, Suspend Operation
Restore PC, WP, and ST from workspace.
Instruction Execution
PC + 2 = PC
Execute Idle
XOP or BLWP
Arith Overflow
Overflow Enabled
INTREQ Active
Interrupt Valid
Idle Instruction
INTACK = H.
MPEN = H.
Store previous PC and WP in new workspace.
Get interrupt-level vector (WP and PC).
Set interrupt mask ST(12 - 15) to (level −1).
Set ST(7 - 11) to 0.
INTACK = H during WP fetch only.
MPEN = H.
Get interrupt vector from 0008$_{16}$ and 000A$_{16}$.
Store previous PC, WP, and ST in new workspace.
Set interrupt mask ST(12 - 15) to 0001$_{16}$.
Set ST(7 - 11) to 0.

BLOCK DIAGRAM

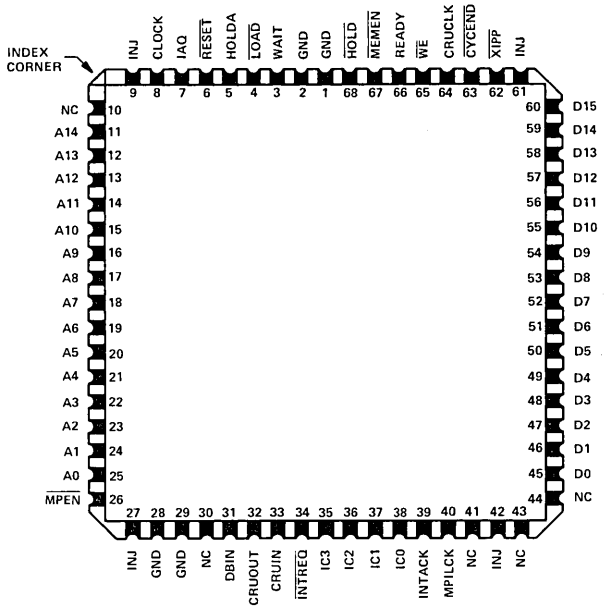


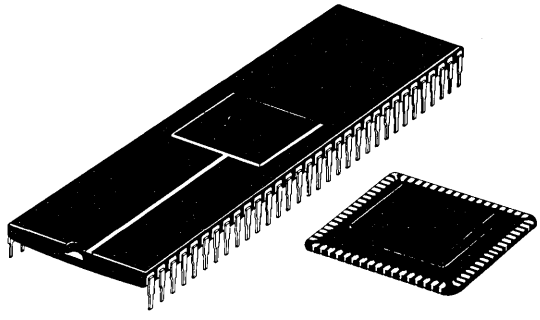
PIN ASSIGNMENTS

SBP9989NJ
64-PIN CERAMIC DUAL-IN-LINE PACKAGE
(TOP VIEW)



SBP9989NFD
68-TERMINAL CERAMIC CHIP CARRIER
(TOP VIEW)





4

SBP 9989

PIN ASSIGNMENTS AND FUNCTIONS (PIN NUMBERS ARE FOR 64-PIN DIP)

SIGNATURE	PIN #	I/O	DESCRIPTION
			ADDRESS BUS
A0 (MSB) ↓ ↓ A14 (LSB)	24 ↓ 10	OUT*	A0-A14 comprise the address bus. This open-collector bus provides the memory address to the memory system when $\overline{\text{MEMEN}}$ is active and CRU I/O bit addresses to the I/O system when $\overline{\text{MEMEN}}$ is inactive and DBIN is active.
$\overline{\text{MPEN}}$	25	OUT*	MEMORY MAP ENABLE. $\overline{\text{MPEN}}$ represents the inverted value of Status Register Bit 8 (ST8). $\overline{\text{MPEN}}$ can be changed by any instruction (i.e., LST, etc.) affecting ST8 and will be set to 1 during SBP9989 trap addressing; namely interrupts, $\overline{\text{LOAD}}$, $\overline{\text{RESET}}$, XOP and ILLOP, $\overline{\text{MPEN}}$ may be used to allow memory expansion to 64 kilowords.
			DATA BUS
D0 (MSB) ↓ ↓ D15 (LSB)	41 ↓ 56	I/O*	D0-D15 comprise the bidirectional, open-collector data bus. This bus transfers memory data to (when writing) and from (when reading) the external memory system when $\overline{\text{MEMEN}}$ is active.
			POWER SUPPLY
INJ	9		Injector-Supply Current
INJ	26		Injector-Supply Current
INJ	40		Injector-Supply Current
INJ	57		Injector-Supply Current
GND	1		Ground
GND	2		Ground
GND	27		Ground
GND	28		Ground
			CLOCK
CLK	8	IN	Single-phase clock input
			BUS CONTROL
$\overline{\text{MEMEN}}$	63	OUT*	MEMORY ENABLE. When active (low), $\overline{\text{MEMEN}}$ indicates that the address bus contains a valid memory address.
DBIN	29	OUT*	DATA BUS IN. When activated (high) by the SBP9989 during $\overline{\text{MEMEN}}$, DBIN indicates that the SBP9989 has disabled its output buffers to allow the memory system to place memory read data on the bus. The SBP9989 will also activate DBIN during all CRU operations and during the execution of the five external instructions. In all other cases except when HOLDA is active, the SBP9989 will maintain DBIN at a low logic level.
$\overline{\text{WE}}$	61	OUT*	WRITE ENABLE. When active (low), $\overline{\text{WE}}$ indicates that the SBP9989 data bus is outputting data to be written into memory.

*When HOLDA is active, these terminals are high.

SIGNATURE	PIN#	I/O	DESCRIPTION
			COMMUNICATION REGISTER UNIT (CRU)
CRUCLK	60	OUT	CRU CLOCK. When active (high), CRUCLK indicates to the external logic the presence of output data on CRUOUT or the presence of an encoded external instruction on A0-A2.
CRUIN	31	IN	CRU DATA IN. CRUIN receives input data from the external interface logic. When the SBP9989 executes a STCR or TB instruction, it samples CRUIN for the level of the CRU bit specified by the address bus (A3-A14).
CRUOUT	30	OUT	CRU DATA OUT. CRUOUT outputs serial data when the SBP9989 executes a LDCR, SBZ, or SB0 instruction. The data on CRUOUT should be sampled by the external interface logic when CRUCLK goes active.
			INTERRUPT CONTROL
$\overline{\text{INTREQ}}$	32	IN	INTERRUPT REQUEST. When active (low), $\overline{\text{INTREQ}}$ indicates that an external interrupt is requesting service. If $\overline{\text{INTREQ}}$ is active the SBP9989 loads the data on the interrupt code input lines IC0-IC3 into the internal interrupt-code storage register. The code is then compared to the interrupt mask bits of the status register. If the interrupt code is equal to or less than Status Register Bits 12-15 (equal or higher priority than the previous enabled interrupt level), the SBP9989 initiates the interrupt sequence. If the comparison fails, the SBP9989 ignores the interrupt request. In that case, $\overline{\text{INTREQ}}$ should be held active. The SBP9989 will continue to sample IC0-IC3 until the program enables a sufficiently low interrupt level to accept the requesting interrupt.
IC0 (MSB) ↓ ↓ IC3 (LSB)	36 ↓ 33	IN	INTERRUPT CODES. IC0 (MSB)-IC3 (LSB), indicating an interrupt identity code, are sampled by the SBP9989 when $\overline{\text{INTREQ}}$ is active (low). When IC0-IC3 are LLLL, the highest-priority external interrupt is requesting service; when HHHH, the lowest-priority external interrupt is requesting service.
INTACK	37	OUT	INTERRUPT ACKNOWLEDGE. When active (high) during non-hold states, INTACK indicates the SBP9989 has initiated a trap sequence caused by the receipt of a valid interrupt, $\overline{\text{LOAD}}$ or $\overline{\text{RESET}}$. INTACK shall be activated in the trap sequence while the SBP9989 is obtaining the new WP value from memory. An external device may determine which function or interrupt level is being serviced by monitoring the address bus during the INTACK time. When the SBP9989 is in a hold state (caused by activation of $\overline{\text{XIPP}}$ or $\overline{\text{HOLD}}$) INTACK indicates SBP9989 has received a valid interrupt (level is less than value of interrupt mask), a $\overline{\text{LOAD}}$ or $\overline{\text{RESET}}$. INTACK will remain valid (high) until the SBP9989 leaves a hold state ($\overline{\text{HOLD}}$ or $\overline{\text{XIPP}}$ released) or until the signal requesting interrupt is released.

SIGNATURE	PIN#	I/O	DESCRIPTION
			MEMORY CONTROL
$\overline{\text{HOLD}}$	64	IN	HOLD. When active (low), $\overline{\text{HOLD}}$ indicates to the SBP9989 that an external controller (e.g., DMA device) desires to use the memory bus for direct memory data transfers. In response, the SBP9989 enters the hold state after completion of its present cycle (memory or nonmemory). The SBP9989 then asserts HOLDA and allows its address bus, $\overline{\text{MPEN}}$, data bus, $\overline{\text{MEMEN}}$, $\overline{\text{WE}}$, DBIN, IAQ and $\overline{\text{CYCEND}}$ to be pulled to the high logic state. When $\overline{\text{HOLD}}$ is deactivated, the SBP9989 reassumes bus control and continues operation by resuming execution of the suspended instruction.
HOLDA	5	OUT	HOLD ACKNOWLEDGE. When active (high) HOLDA indicates that the SBP9989 is in a hold state and that its address bus, $\overline{\text{MPEN}}$, data bus, $\overline{\text{MEMEN}}$, $\overline{\text{WE}}$, DBIN, IAQ, and $\overline{\text{CYCEND}}$ are pulled to the high state. The SBP9989 will enter a hold state in response to the activation of $\overline{\text{HOLD}}$ or $\overline{\text{XIPP}}$ (during the activation of an ILLOP or XOP instruction).
READY	62	IN	READY. When active (high) READY indicates that the memory (for memory operations) or CRU device (for CRU operations) will be ready to read or write during the next clock cycle. When READY is not active (low), the SBP9989 enters a wait state and suspends internal operations until the memory system or CRU device activates READY.
WAIT	3	OUT	WAIT. When active (high), WAIT indicates the SBP9989 has entered a wait state in response to a not READY condition from a memory system or a CRU device.
			TIMING AND CONTROL
IAQ	7	OUT*	INSTRUCTION ACQUISITION. IAQ is activated (high) by the SBP9989 during any SBP9989 initiated instruction acquisition memory cycle. Consequently, IAQ may be used by an external device as an indication of when to sample the memory data bus to obtain instruction operations code data.
$\overline{\text{CYCEND}}$	59	OUT*	END OF CYCLE. When active (low), $\overline{\text{CYCEND}}$ indicates that the SBP9989 will initiate a new microinstruction cycle on the next low-to-high transition of the clock.
MPILCK	39	OUT	MULTIPROCESSOR INTERLOCK. When active (high) MPILCK indicates the SBP9989 is performing the operations associated with operand transfer and manipulation for the ABS instruction. MPILCK shall be activated by the SBP9989 during any ABS instruction upon initiation of the operand read operation and remain active until the completion of the instruction (i.e., MPILCK remains active for the duration of the SBP9989 read-modify-write operation cycle for the ABS instruction). Consequently, MPILCK may be used in the implementation of a nonseparable test and set capability. $\overline{\text{HOLD}}$ is sampled during MPILCK activation, so MPILCK can be used to control assertion of $\overline{\text{HOLD}}$.

*When HOLDA is active, these terminals are high.

SIGNATURE	PIN#	I/O	DESCRIPTION
$\overline{XIPP}$	58	IN	EXTENDED INSTRUCTION PROCESSOR PRESENT. When activated (low) by an external device (an extended instruction processor, XIP) upon detection of the acquisition of an SBP9989 undefined op code. $\overline{XIPP}$ indicates the XIP will execute the undefined instruction. Recognition of $\overline{XIPP}$ will cause the SBP9989 to allow its memory bus signals to be pulled high, activate HOLDA and enter a hold state (i.e., suspend internal operation) after it has stored its WP, PC and ST in the workspace defined by the interrupt-level-2 trap vector. Upon receipt of HOLDA, the XIP may then proceed to execute the undefined instruction. During the instruction execution, the XIP may utilize the WP, PC and ST previously stored in memory by the SBP9989. Upon completion of its instruction execution, the XIP releases $\overline{XIPP}$ and allows the SBP9989 to resume bus control and restart instruction execution. The SBP9989 will resume operation by reloading (from memory) its WP, PC and ST. $\overline{XIPP}$ may also be used to initiate a trap to interrupt-level-2 by going active during IAQ for any instruction. This is useful for implementing break points or maintenance panels.
$\overline{LOAD}$	4	IN	LOAD. When active (low), $\overline{LOAD}$ causes the SBP9989 to set $\overline{MPEN}$ high, issue INTACK, store old PC, WP, and ST, set Status Register Bits 9-15 low, and execute a nonmaskable interrupt with unmapped memory addresses $FFFC_{16}$ and $FFFE_{16}$ containing the associated trap vectors (WP and PC). The load sequence is initiated after the instruction being executed is completed. $\overline{LOAD}$ will also terminate an idle state. If $\overline{LOAD}$ is active at the end of a reset function, the $\overline{LOAD}$ trap will occur after the reset function is completed. If $\overline{LOAD}$ is activated during a hold state (caused by $\overline{XIPP}$ or $\overline{HOLD}$), the SBP9989 will activate INTACK to indicate a pending $\overline{LOAD}$ needs to be serviced. During hold states, $\overline{LOAD}$ will remain active until the SBP9989 leaves the hold state and the above conditions are met. $\overline{LOAD}$ may be used to implement bootstrap loaders. Additionally, front-panel routines may be implemented using CRU bits as front panel interface signals, and software control routines to direct the panel operations.
$\overline{RESET}$	6	IN	RESET. When active (low logic level), $\overline{RESET}$ causes the SBP9989 to reset itself, and inhibit $\overline{WE}$ and CRUCLK. When $\overline{RESET}$ is released, the SBP9989 goes through a level-zero interrupt sequence by causing $\overline{MPEN}$ to go to high, issuing INTACK, storing old PC, WP and ST, setting all status register bits low, acquiring the WP and PC trap vectors from memory locations 0000_{16} and 0002_{16}, and then fetching the first instruction of the reset program environment if $\overline{LOAD}$ is not active. The SBP9989 continuously samples $\overline{RESET}$ on low-to-high clock transitions. $\overline{RESET}$ must be active for one low-to-high transition of the clock and satisfy the hold time requirements of this signal.

Each SBP9989 instruction performs one of the following operations:

1. Arithmetic, logical, comparison, or manipulation operation on data.
2. Loading or storage of internal registers (program counter, workspace pointer, or status).
3. Data transfer between memory and external devices via the CRU.
4. Control functions.

TERMS AND DEFINITIONS

The terms used in describing the instructions and status bits of the SBP9989 are defined below.

TERMS AND DEFINITIONS

TERM	DEFINITION
B	Byte Indicator (1 = byte; 0 = word)
C	Bit Count
D	Destination address register
DA	Destination address
IOP	Immediate operand
LSB(n)	Least significant (right-most) bit of n
MSB(n)	Most significant (left-most) bit of n
PC	Program Counter
Result	Result of operation performed by instruction
S	Source address register
SA	Source address
ST	Status register
STn	Bit n of status register
T_D	Destination-address-mode control
T_S	Source-address-mode control
WR	Workspace register
WRn	Workspace register n
WR(0,1)	Concatenation of WR0 and WR1 to form a 32-bit register
a → b	a is transferred to b
|n|	Absolute value of n
+	Arithmetic addition
–	Arithmetic subtraction
AND	Logical AND
OR	Logical OR
$\oplus$	Logical exclusive OR
$\overline{n}$	Logical complement of n
x	Arithmetic multiplication

ADDRESSING MODES

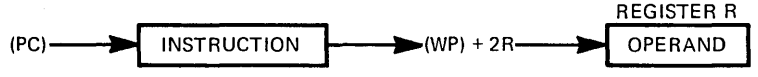
The SBP9989 instructions contain a variety of available modes for addressing random memory data (e.g., program parameters and flags), or formatted memory data (character strings, data lists, etc.). These addressing modes are:

- o Workspace Register Addressing
- o Workspace Register Indirect Addressing
- o Workspace Register Indirect Auto Increment Addressing
- o Symbolic (Direct) Addressing
- o Indexed Addressing
- o Immediate Addressing
- o Program Counter Relative Addressing
- o CRU Relative Addressing

The following figures graphically describe the derivation of the effective address for each addressing mode. The applicability of addressing modes to particular instructions is described next along with the description of the operations performed by the instruction. The symbols following the names of the addressing modes (R, *R, *R+, @LABEL, or @TABLE(R)) are general forms used by 9900 assemblers to select the addressing modes for Register R.

Workspace Register Addressing . . . R

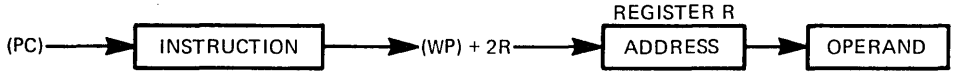
The workspace register addressing mode is specified by setting the 2-bit T field (T_S or T_D) of the instruction word equal to 00. Workspace register R contains the operand.



4

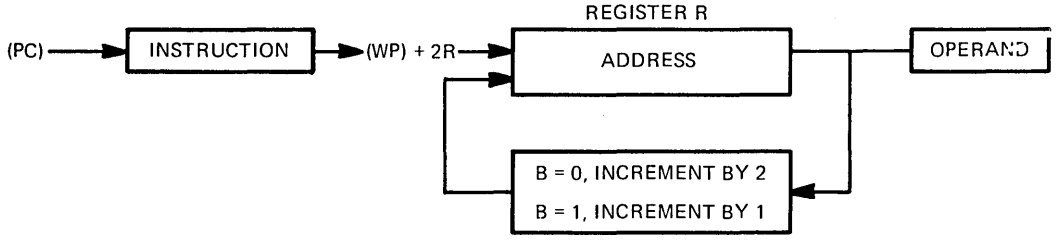
Workspace Register Indirect Addressing . . . *R

The workspace register indirect addressing mode is specified by setting the 2-bit T field (T_S or T_D) in the instruction word equal to 01. Workspace register R contains the address of the operand.



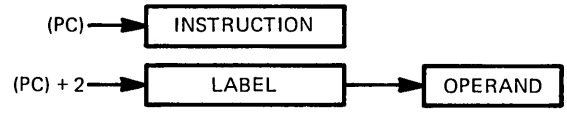
Workspace Register Indirect Auto Increment Addressing . . . *R+

The workspace register indirect auto-increment addressing mode is specified by setting the 2-bit T field (T_S or T_D) in the instruction word equal to 11. Workspace register R contains the address of the operand. After the address of the operand is acquired, the contents of workspace register R is incremented.



Symbolic (Direct) Addressing . . . @LABEL

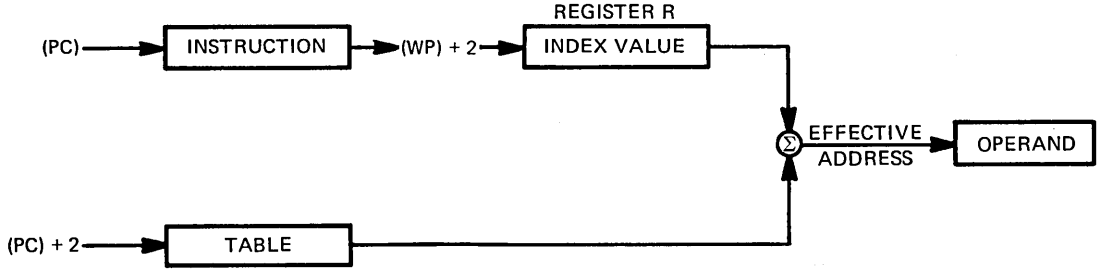
The symbolic addressing mode is specified by setting the 2-bit T field (T_S or T_D) in the instruction word equal to 10 and setting the corresponding S or D field equal to 0. The word following the instruction contains the address of the operand.



Indexed Addressing . . . @TABLE(R)

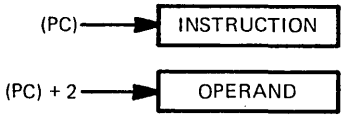
The indexed addressing mode is specified by setting the 2-bit T field (T_S or T_D) of the instruction word equal to 10. The value in the corresponding S or D field is the register which contains the index value. Register 0 may not be used for indexed addressing.

The word following the instruction contains the base address. Workspace register R contains the index value. The sum of the base address and the index value results in the effective address of the operand.



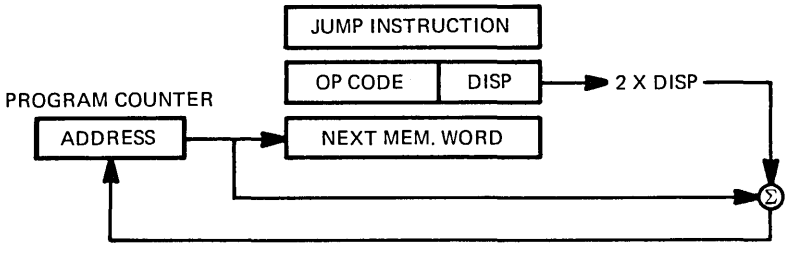
Immediate Addressing

The word following the instruction contains the operand.



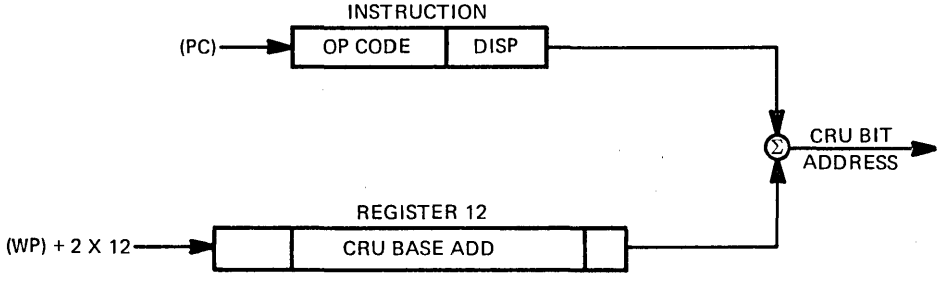
Program Counter Relative Addressing

The 8-bit signed displacement in the right byte (bits 8-15) of the instruction is multiplied by 2 and added to the updated contents of the program counter. The result is placed in the PC.



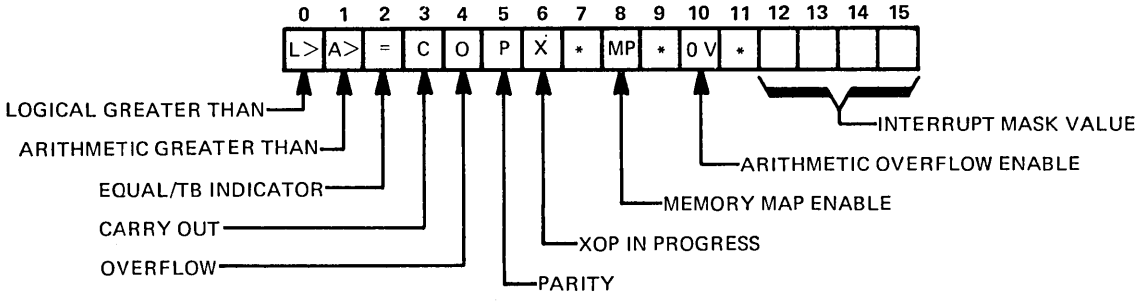
CRU Relative Addressing

The 8-bit signed displacement in the right byte of the instruction is added to the CRU base address (bits 3-14 of the workspace register 12). The result is the CRU address of the selected CRU bit.



STATUS REGISTER MANIPULATION

Various SBP9989 machine instructions affect the status register. The figure below shows the status register bit assignments and the following table lists the effects of the instructions on each status bit.



*These bits are functionally uncommitted and are available to the user.

TABLE 5. STATUS REGISTER BIT DEFINITIONS

BIT	NAME	INSTRUCTION	CONDITION TO SET BIT TO 1
STO	Logical Greater Than	C, CB	If MSB(SA) = 1 and MSB(DA) = 0, or if MSB(SA) = MSB(DA) and MSB OF [(DA) – (SA)] = 1.
		CI	If MSB(WR) = 1 and MSB of IOP = 0, or if MSB(WR) = MSB of IOP and MSB of [IOP – (WR)] = 1.
		ABS, LDCR	If (SA) ≠ 0.
		RTWP	If Bit (0) of WR15 is 1.
		LST	If Bit (0) of selected WR is 1.
		All others	If result ≠ 0.
ST1	Arithmetic Greater Than	C, CB	If MSB(SA) = 0 and MSB(DA) = 1, or if MSB(SA) = MSB(DA) and MSB of [(DA) – (SA)] = 1.
		CI	If MSB(WR) = 0 and MSB of IOP = 1, or if MSB(WR) = MSB of IOP and MSB of [IOP – (WR)] = 1.
		ABS, LDCR	If MSB(SA) = 0 and (SA) ≠ 0.
		RTWP	If Bit (1) of WR15 is 1.
		LST	If Bit (1) of selected WR is 1.
		All others	If MSB of result = 0 and result ≠ 0.
ST2	Equal	C, CB	If (SA) = (DA).
		CI	If (WR) = IOP.
		COC	If (SA) and $\overline{(DA)}$ = 0.
		CZC	If (SA) and (DA) = 0.
		TB	If CRUIN = 1.
		ABS, LDCR	If (SA) = 0.
		RTWP	If Bit (2) of WR15 is 1.
		LST	If Bit (2) of selected WR is 1.
		All others	If result = 0.

STATUS REGISTER BIT DEFINITIONS (Continued)

BIT	NAME	INSTRUCTION	CONDITION TO SET BIT TO 1
ST3	CARRY	A, AB, ABS, AI, DEC, DECT, INC, INCT, NEG, S, SB	If CARRY OUT = 1.
		SRA, SLA, SRL, SRC	If last bit shifted out = 1.
		RTWP	If Bit (3) of WR15 is 1.
		LST	If Bit (3) of selected WR is 1.
ST4	OVERFLOW	A, AB	If MSB(SA) = MSB(DA) and MSB of result ≠ MSB (DA)
		AI	If MSB(WR) = MSB of IOP and MSB of result ≠ MSB(WR).
		S, SB	If MSB(SA) ≠ MSB(DA) and MSB of result ≠ MSB(DA).
		DEC, DECT	If MSB(SA) = 1 and MSB of result = 0.
		INC, INCT	If MSB(SA) = 0 and MSB of result = 1.
		SLA	If MSB changes during shift.
		DIV	If MSB(SA) = 0 and MSB(DA) = 1 or if MSB(SA) = MSB(DA) and MSB of [(DA) – (SA)] = 0.
		DIVS	If (SA) = 0000 or if MSB(SA) = MSB(WR0) and $\lvert 2^{15} \times (SA) \rvert \leqslant WR(0,1)$.
		ABS, NEG	If (SA) = 8000_{16}.
		RTWP	If Bit (4) of WR15 is 1.
		LST	If Bit (4) of selected WR is 1.
ST5	PARITY	CB, MOVB	If (SA) had odd number of 1's.
		LDCR	If $1 \leqslant C \leqslant 8$ and (SA) has odd number of 1's.
		AB, SB, SOCB, SZCB	If result has odd number of 1's.
		RTWP	If Bit (5) of WR15 is 1.
		LST	If Bit (5) of Selected WR is 1.
		STCR	If $1 \leqslant C \leqslant 8$ and result has odd number of 1's.
ST6	XOP	XOP	If XOP instruction is executed.
		RTWP	If Bit (6) of WR15 is 1.
		LST	If Bit (6) of selected WR is 1.
ST7, ST9 or ST11	User defined	RTWP	If corresponding bit of WR15 is 1 or
		LST	If corresponding bit of selected WR is 1.
ST8	MEMORY MAP	RTWP	If Bit (8) of WR15 is 1.
		LST	If Bit (8) of selected WR is 1.
ST10	ARITHMETIC OVERFLOW ENABLE	RTWP	If Bit (10) of WR15 is 1.
		LST	If Bit (10) of selected WR is 1.
ST12 THRU ST15	INTERRUPT MASK	LIMI	If corresponding bit of IOP is 1.
		RTWP	If corresponding bit of WR15 is 1.
		LST	If corresponding bit of selected WR is 1.

NOTE: Interrupt, $\overline{\text{LOAD}}$, XOPs, ILLOPs, and $\overline{\text{RESET}}$ operations sets Bits (7 - 11) to 0.

4

Dual-Operand Instructions with Multiple Addressing for Source and Destination Operands

0 1 2	3	4 5	6 7 8 9	10 11	12 13 14 15
OP CODE	B	T_D	D	T_S	S

If B = 1, the operands are bytes and the operand addresses are byte addresses. If B = 0, the operands are words and the operand addresses are word addresses. The addressing mode for each operand is determined by the T field of that operand.

T_S or T_D	S or D	ADDRESSING MODE	NOTES
00	0 - 15	Workspace register	1
01	0 - 15	Workspace register indirect	
10	0	Symbolic	4
10	1 - 15	Indexed	2, 4
11	0 - 15	Workspace register indirect auto-increment	3

NOTES:
1. When a workspace register is the operand of a byte instruction (Bit (3) = 1), the most significant (left) byte (Bits (0-7)) is the operand and the least significant (right) byte (Bits (8-15)) remains unchanged.
2. Workspace register 0 may not be used for indexing.
3. The workspace register is incremented by 1 for byte instructions (Bit (3) = 1) and is incremented by 2 for word instructions (Bit (3) = 0).
4. When T_S and T_D = 10, two words are required in addition to the instruction word. The first word is the source operand base address and the second word is the destination operand base address.

MNEMONIC	MEANING	OP CODE	B	RESULT COMPARED TO 0	STATUS BITS AFFECTED	DESCRIPTION
A	Add	101	0	Yes	0 - 4	(SA) + (DA) → (DA)
AB	Add bytes	101	1	Yes	0 - 5	(SA) + (DA) → (DA)
C	Compare	100	0	No	0 - 2	Compare (SA) to (DA) and set appropriate status bits
CB	Compare bytes	100	1	No	0 - 2, 5	Compare (SA) to (DA) and set appropriate status bits
S	Subtract	011	0	Yes	0 - 4	(DA) − (SA) → (DA)
SB	Subtract bytes	011	1	Yes	0 - 5	(DA) − (SA) → (DA)
SOC	Set ones corresponding	111	0	Yes	0 - 2	(DA) OR (SA) → (DA)
SOCB	Set ones corresponding bytes	111	1	Yes	0 - 2, 5	(DA) OR (SA) → (DA)
SZC	Set zeros corresponding	010	0	Yes	0 - 2	(DA) AND $\overline{(SA)}$ → (DA)
SZCB	Set zeros corresponding bytes	010	1	Yes	0 - 2, 5	(DA) AND $\overline{(SA)}$ → (DA)
MOV	Move	110	0	Yes	0 - 2	(SA) → (DA)
MOVB	Move bytes	110	1	Yes	0 - 2, 5	(SA) → (DA)

Dual-Operand Instructions with Multiple Addressing for Source Operand and Workspace Register Addressing for the Destination

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
OP CODE						D				T_S		S			

The addressing mode for the source operand is determined by the T_S field.

T_S	S	ADDRESSING MODE	NOTES
00	0 - 15	Workspace register	
01	0 - 15	Workspace register indirect	
10	0	Symbolic	
10	1 - 15	Indexed	1
11	0 - 15	Workspace register indirect auto increment	2

NOTES: 1. Workspace register 0 may not be used for indexing.
2. The workspace register is incremented by 2.

MNEMONIC	MEANING	OP CODE	RESULT COMPARED TO 0	STATUS BITS AFFECTED	DESCRIPTION
COC	Compare ones corresponding	001000	No	2	Test (D) to determine if 1's are in each bit position where 1's are in (SA). If so, set ST2.
CZC	Compare zeros corresponding	001001	No	2	Test (D) to determine if 0's are in each bit position where 1's are in (SA). If so, set ST2.
XOR	Exclusive OR	001010	Yes	0 - 2	(D)⊕(SA) → (D)
MPY	Multiply	001110	No		Multiply unsigned (D) by unsigned (SA) and place unsigned 32-bit product in D (most significant) and D + 1 (least significant). If WR15 is D, the next word in memory after WR15 will be used for the least-significant half of the product.
DIV	Divide	001111	No	4	If unsigned (SA) is less than or equal to unsigned (D), perform no operation and set ST4. Otherwise, divide unsigned (D) and (D + 1) by unsigned (SA). Quotient → (D), remainder → (D + 1). If D is WR15, the next word in memory after WR15 will be used for the remainder.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
OP CODE										T_S		S			

The addressing mode for the source operand is determined by the T_S field.

T_S	S	ADDRESSING MODE	NOTES
00	0 - 15	Workspace register	1
01	0 - 15	Workspace register indirect	1
10	0	Symbolic	1
10	1 - 15	Indexed	1, 2
11	0 - 15	Workspace register indirect auto increment	1, 3

NOTES: 1. Workspace registers 0 and 1 contain operands used in the signed multiply and divide operations.
2. Workspace register 0 may not be used for indexing.
3. The workspace register is incremented by 2.

MNEMONIC	MEANING	OP CODE	RESULT COMPARED TO 0	STATUS BITS AFFECTED	DESCRIPTION
MPYS	Signed Multiply	000000111	Yes	0 - 2	Multiply signed 2's-complement integer in WR0 by signed 2's complement integer (SA) and place signed 32-bit product in WR0 (most significant) and WR1 (least significant)
DIVS	Signed Divide	000000110	Yes	0 - 2, 4	If (SA) = 0000 or if MSB (SA) = MSB (WR0) and $\|2^{15} \times (SA)\| \leq \|WR(0, 1)\|$ or if MSB (SA) ≠ MSB (WR0) and $\|(2^{15} + 1) \times (SA)\| \leq \|WR(0, 1)\|$ set ST4. Otherwise, divide signed 2's-complement in integer in WR0 and WR1 by the signed 2's-complement integer (SA) and place the signed quotient in WR0 and the signed remainder in WR1. The sign of the quotient is determined by algebraic rules. The sign of the remainder is the same as the sign of the dividend.

Single-Operand Instructions

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
OP CODE										T_S		S			

The T_S and S fields provide multiple-mode addressing capability for the source operand.

MNEMONIC	MEANING	OP CODE	RESULT COMPARED TO 0	STATUS BITS AFFECTED	DESCRIPTION
B	Branch	0000010001	No		SA → (PC)
BL	Branch and link	0000011010	No		(PC) → (WR11); SA → (PC)
BLWP	Branch and load workspace pointer	0000010000	No		(SA) → (WP); (SA + 2) → (PC); (old WP) → (new WR13); (old PC) → (new WR14); (old ST) → (new WR15); the interrupt input ($\overline{\text{INTREQ}}$) is not tested upon completion of the BLWP instruction.
CLR	Clear operand	0000010011	No		0 → (SA)
SETO	Set to ones	0000011100	No		$FFFF_{16}$ → (SA)
INV	Invert	0000010101	Yes	0 - 2	$\overline{(SA)}$ → (SA)
NEG	Negate	0000010100	Yes	0 - 4	−(SA) → (SA)
ABS	Absolute value*	0000011101	No	0 - 4	|(SA)| → (SA)
SWPB	Swap bytes	0000011011	No		Bits (0 - 7) of SA → Bits (8 - 15) of SA; Bits (8 - 15) of SA → Bits (0 - 7) of SA.
INC	Increment	0000010110	Yes	0 - 4	(SA) + 1 → (SA)
INCT	Increment by 2	0000010111	Yes	0 - 4	(SA) + 2 → (SA)
DEC	Decrement	0000011000	Yes	0 - 4	(SA) − 1 → (SA)
DECT	Decrement by 2	0000011001	Yes	0 - 4	(SA) − 2 → (SA)
X**	Execute	0000010010	No		Execute the instruction at SA.

*Operand is compared to zero for status bit.

**If additional memory words for the execute instruction are required to define the operands of the instruction located at SA, these words will be accessed from PC and the PC will be updated accordingly. The instruction acquisition signal (IAQ) will not be true when the SBP9989 accesses the instruction at SA. Status bits are affected in the normal manner for the instruction executed.

CRU Multiple-Bit Instructions

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
OP CODE						C				T_S		S			

The C field specifies the number of bits to be transferred. If C = 0, 16 bits will be transferred. The CRU base register (WR12, Bits 3 - 14) defines the starting CRU bit address. The bits are transferred serially and the CRU address is incremented with each bit transfer, although the contents of WR12 are not affected. T_S and S provide multiple mode addressing capability for the source operand. If 8 or fewer bits are transferred ($1 \leqslant C \leqslant 8$), the source address is a byte address. If 9 or more bits are transferred ($C = 0, C \geqslant 9$), the source address is a word address. If the source is addressed in the workspace register indirect auto increment mode, the workspace register indirect auto increment mode, the workspace register is incremented by 1 if $1 \leqslant C \leqslant 8$, and is incremented by 2 otherwise.

MNEMONIC	MEANING	OP CODE	RESULT COMPARED TO 0	STATUS BITS AFFECTED	DESCRIPTION
LDCR	Load communication register	001100	Yes	0 - 2, 5*	Beginning with LSB of (SA), transfer the specified number of bits from (SA) to the CRU.
STCR	Store communication register	001101	Yes	0 - 2, 5*	Beginning with LSB of (SA), transfer the specified number of bits from the CRU to (SA). Load unfilled bit positions with 0.

*ST5 is affected only if $1 \leqslant C \leqslant 8$

CRU Single-Bit Instructions

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
OP CODE								SIGNED DISPLACEMENT							

CRU relative addressing is used to address the selected CRU bit.

MNEMONIC	MEANING	OP CODE	STATUS BITS AFFECTED	DESCRIPTION
SBO	Set bit to one	00011101		Set the selected CRU output bit to 1.
SBZ	Set bit to zero	00011110		Set the selected CRU output bit to 0.
TB	Test bit	00011111	2	If the selected CRU input bit = 1, set ST2 to 1 If the selected CRU input bit = 0, set ST2 to 0.

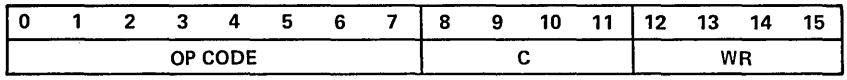
Jump Instructions

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
OP CODE								DISPLACEMENT							

Jump instructions cause the PC to be loaded with the value selected by PC relative addressing if the status register condition is met. Otherwise, no operation occurs and the next instruction is executed since the PC points to the next instruction. The displacement field in 2's-complement form is a word count to be added to PC. Thus, the jump instruction has a range of −128 to 127 words from the memory-word address following the jump instruction. No ST bits are affected by jump instructions.

MNEMONIC	MEANING	OP CODE	STATUS REGISTER CONDITION TO LOAD PC
JEQ	Jump equal	00010011	ST2 = 1
JGT	Jump greater than	00010101	ST1 = 1
JH	Jump high	00011011	ST0 = 1 and ST2 = 0
JHE	Jump high or equal	00010100	ST0 = 1 or ST2 = 1
JL	Jump low	00011010	ST0 = 0 and ST2 = 0
JLE	Jump low or equal	00010010	ST0 = 0 or ST2 = 1
JLT	Jump less than	00010001	ST1 = 0 and ST2 = 0
JMP	Jump unconditional	00010000	unconditional
JNC	Jump no carry	00010111	ST3 = 0
JNE	Jump not equal	00010110	ST2 = 0
JNO	Jump no overflow	00011001	ST4 = 0
JOC	Jump on carry	00011000	ST3 = 1
JOP	Jump odd parity	00011100	ST5 = 1

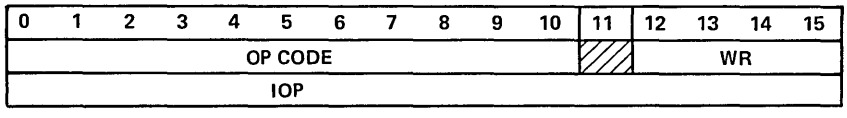
Shift Instructions



If C = 0, Bits 12 - 15 of WR0 contain the shift count. If C = 0 and Bits 12 - 15 of WR0 = 0, the shift count is 16.

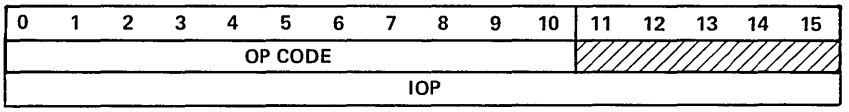
MNEMONIC	MEANING	OP CODE	RESULT COMPARED TO 0	STATUS BITS AFFECTED	DESCRIPTION
SLA	Shift left arithmetic	00001010	Yes	0 - 4	Shift (WR) left. Fill vacated bit positions with 0.
SRA	Shift right arithmetic	00001000	Yes	0 - 3	Shift (WR) right. Fill vacated bit positions with original MSB of (WR).
SRC	Shift right circular	00001011	Yes	0 - 3	Shift (WR) right. Shift previous LSB into MSB.
SRL	Shift right logical	00001001	Yes	0 - 3	Shift (WR) right. Fill vacated bit positions with 0's.

Immediate Register Instructions



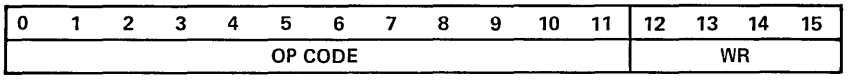
MNEMONIC	MEANING	OP CODE	RESULT COMPARED TO 0	STATUS BITS AFFECTED	DESCRIPTION
AI	Add immediate	00000010001	Yes	0 - 4	(WR) + IOP → (WR)
ANDI	AND immediate	00000010010	Yes	0 - 2	(WR) AND IOP → (WR)
CI	Compare immediate	00000010100	No	0 - 2	Compare (WR) to IOP and set appropriate status bits.
LI	Load immediate	00000010000	Yes	0 - 2	IOP → (WR)
ORI	OR immediate	00000010011	Yes	0 - 2	[(WR) OR IOP] → (WR)

Internal Register Load Immediate Instructions



MNEMONIC	MEANING	OP CODE	DESCRIPTION
LWPI	Load workspace pointer immediate	00000010111	IOP → (WP), no ST bits affected.
LIMI	Load interrupt mask immediate	00000011000	Bits (12 - 15) of IOP → ST (12-15)

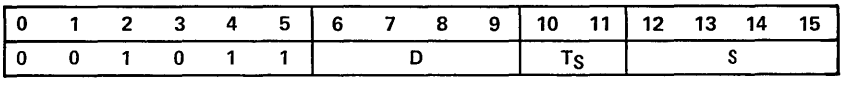
Internal Register Load and Store Instructions



MNEMONIC	MEANING	OP CODE	STATUS BITS AFFECTED	DESCRIPTION
STST	Store status register	00000010110X		(ST) → (WR)
LST	Load status register	000000001000	0 - 15	(WR) → (ST)
STWP	Store workspace pointer	00000010101X		(WP) → (WR)
LWP	Load workspace pointer	000000001001		(WR) → (WP)

X ≡ don't care

Extended Operation (XOP) Instruction



The T_S and S fields provide multiple-mode addressing capability for the source operand. When the XOP is executed, ST6 is set and the following transfers occur:

$(40_{16} + 4 \times D) \rightarrow (WP)$
$(42_{16} + 4 \times D) \rightarrow (PC)$
(ST7 - ST11) → 00000
SA → (New WR11)
(Old WP) → (New WR13)
(Old PC) → (New WR14)
(Old ST) → (New WR15)
$\overline{MPEN} \rightarrow 1$

The SBP9989 does not test interrupt requests ($\overline{INTREQ}$) upon completion of the XOP instruction.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	0	1	1	1	0	0					

The RTWP instruction causes the following transfers to occur:

(WR15) → (ST)
(WR14) → (PC)
(WR13) → (WP)

External Instructions

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
OP CODE											C				

External instructions cause the three most significant address lines (A0 - A2) to be set to the levels described below, address lines A3 - A7 to be set to the 5-bit value specified in the C field of the instruction, the DBIN output to be activated, and the CRUCLK line to be pulsed, allowing external control functions to be initiated.

MNEMONIC†	MEANING	OP CODE	STATUS BITS AFFECTED	DESCRIPTION	ADDRESS BUS		
					A0	A1	A2
IDLE	Idle	00000011010		Suspend SBP9989 instruction execution until an Interrupt, $\overline{\text{LOAD}}$ or $\overline{\text{RESET}}$ occurs	L	H	L
RSET	Reset	00000011011	7 - 15	0 → ST (7 - 15)	L	H	H
CKOF	User defined	00000011110			H	H	L
CKON	User defined	00000011101			H	L	H
LREX	User defined	00000011111			H	H	H

†The mnemonics associated with these instructions relate to their use in the TI 990/4 minicomputer and have no special significance.

Microinstruction Cycle

The SBP9989 includes circuitry which will indicate the completion of a microinstruction cycle. Designated as the $\overline{\text{CYCEND}}$ function, it provides CPU status that can simplify system design. The $\overline{\text{CYCEND}}$ output will go to a low logic level as a result of the low-to-high transition of each clock pulse which initiates the last clock cycle of a microinstruction.

Instruction Execution Times

Instruction execution times for the SBP9989 are a function of:

1) Clock cycle time, t_C.
2) Addressing mode used where operands have multiple addressing mode capability.
3) Number of wait states required per memory access.
4) Number of wait states required per CRU operation.

Table 6 lists the number of clock cycles, memory-access cycles and CRU operations required to execute each SBP9989 instruction. For instructions with multiple addressing modes for either or both operands, the table lists the number of clock cycles and memory-access cycles with all operands addressed in the workspace register mode. To determine the additional number of clock cycles and memory-access cycles required for modified addressing, add the appropriate values from the referenced table. For the five CRU instructions (i.e., STCR, LDCR, SBO, SBZ, TB), the table lists the number of clock cycles assuming no wait states for CRU operations. To determine the additional number of CRU-related clock cycles, add one clock cycle for each wait state incurred as the result of a CRU operation. The total execution time for an instruction is given by:

$$T = t_C [C_T + (W_M \times M_T)] + t_C (W_C \times P)$$

where:

T = total instruction execution time;

t_C = clock cycle time;

C_T = total number of clock cycles (clock cycles for instruction execution plus clock cycles for address modification);

W_M = number of required wait states per memory access;

M_T = total number of memory-accesses (memory accesses for instruction execution plus memory accesses for address modification);

P = number of CRU operations;

W_C = number of required wait states per CRU operation.

As an example, the instruction MOVB is used in a system with $t_C = 0.250\ \mu s$ and no wait states are required to access memory. Both operands are addressed in the workspace register mode. The instruction execution time is given by:

$$T = t_C [C_T + (W_M \times M_T)] + t_C (W_C \times P)$$
$$= 0.250 [12 + (0 \times 4)] + 0.250 (0) = 3\ \mu s$$

If two wait states per memory access were required, the execution time would become:

$$T = 0.250 [12 + (2 \times 4)] + 0.250 (0) = 5\ \mu s$$

If the source operand were addressed in the symbolic mode and two wait states were required:

$$T = t_C [C_T + (W_M \times M_T)] + t_C (W_C \times P)$$
$$C_T = 12 + 6 = 18$$
$$M_T = 4 + 1 = 5$$
$$T = 0.250 [18 + (2 \times 5)] + 0.250 (0) = 7\ \mu s$$

INSTRUCTION	CLOCK CYCLES		MEMORY CYCLES		ADDRESS MODIFICATION		CRU OPERATIONS
	SBP9989	Δ FROM SBP9900A	SBP9989	Δ FROM SBP9900A	SOURCE	DEST.	P
A	12	−2	4		Table 1	Table 1	
AB	12	−2	4		Table 1		
ABS: (MSB=0)	10	−2	2		Table 1		
(MSB=1)	14		3		Table 1		
AI	14		4				
ANDI	14		4				
B	6	−2	1	−1	Table 1		
BL	10	−2	2	−1	Table 1		
BLWP	24	−2	6		Table 1		
C	12	−2	3		Table 1	Table 1	
CB	12	−2	3		Table 1	Table 1	
CI	12	−2	3				
CKOF	10	−2	1				
CKON	10	−2	1				
CLR	8	−2	2	−1	Table 1		
COC	12	−2	3		Table 1		
CZC	12	−2	3		Table 1		
DEC	10		3		Table 1		
DECT	12		3		Table 1		
DIV: (ST4 is set)	20	+4	4	+1	Table 1		
(ST4 is reset)	56	−38 to −68	6		Table 1		
DIVS: (ST4 is set)	56	new	4		Table 1		
(ST4 is reset)	60	new	6		Table 1		
IDLE	10	−2	1				
INC	10		3		Table 1		
INCT	10		3		Table 1		
INV	10		3		Table 1		
JUMP: (PC is changed)	6	−4	1				
(PC is not changed)	6	−2	1				
LDCR: (C=0)	48	−4	3		Table 1		16
(1 ⩽ C ⩽ 15)	16 + 2C	−4	3		Table 1		C
LI	12		3				
LIMI	12	−2	2				
LREX	10	−2	1				
LST	10	new	2				
LWP	10	new	2				
LWPI	12	+2	2				
MOV	10	−4	3	−1	Table 1	Table 1	
MOVB	12	−2	4		Table 1	Table 1	
MPY	52		5		Table 1		
MPYS	56	new	5		Table 1		
NEG	12		3		Table 1		
ORI	14		4				
RSET	10	−2	1				
RTWP	16	+2	4				

INSTRUCTION	CLOCK CYCLES		MEMORY CYCLES		ADDRESS MODIFICATION		CRU OPERATIONS
	SBP9989	Δ FROM SBP9900A	SBP9989	Δ FROM SBP9900A	SOURCE	DEST.	P
S	12	−2	4		Table 1	Table 1	
SB	12	−2	4		Table 1	Table 1	
SBO	12		2				1
SBZ	12		2				1
SETO	8	−2	2	−1	Table 1		
SHIFTS:							
(C≠0)	12 + 2C		3				
(C=0, Bits (12 - 15) of WR0 = 0)	52		4				
(C=0, Bits (12 - 15) of WR0 ≠ 0)	Note 1		4				
SOC	12	−2	4		Table 1	Table 1	
SOCB	12	−2	4		Table 1	Table 1	
STCR: (C=0)	56	−4	4		Table 1		16
(1 ⩽ C ⩽ 8)	40	−2 to −4	4		Table 1		C
(9 ⩽ C ⩽ 15)	56	−2	4		Table 1		C
STST	8		2				
STWP	8		2				
SWPB	10		3		Table 1		
SZC	12	−2	4		Table 1	Table 1	
SZCB	12	−2	4		Table 1	Table 1	
TB	12		2				1
X**	4		1		Table 1		
XOP	28	−8	7	−1			
XOR	12	−2	4		Table 1		
Reset function	20	−6	5				
Load function	20	−2	5				
Interrupt Context Switch	20	−2	5				
UNDEFINED OP CODES: 0000_{16}-$007F_{16}$ $00A0_{16}$-$017F_{16}$ 0320_{16}-$033F_{16}$ 0780_{16}-$07FF_{16}$ $0C00_{16}$-$0FFF_{16}$	24	+20	6	+5			

*Execution time is added to the execution time of the source address.

**Execution time includes time to perform a trap (i.e., subroutine call) operation resulting from $\overline{XIPP}$ being inactive.

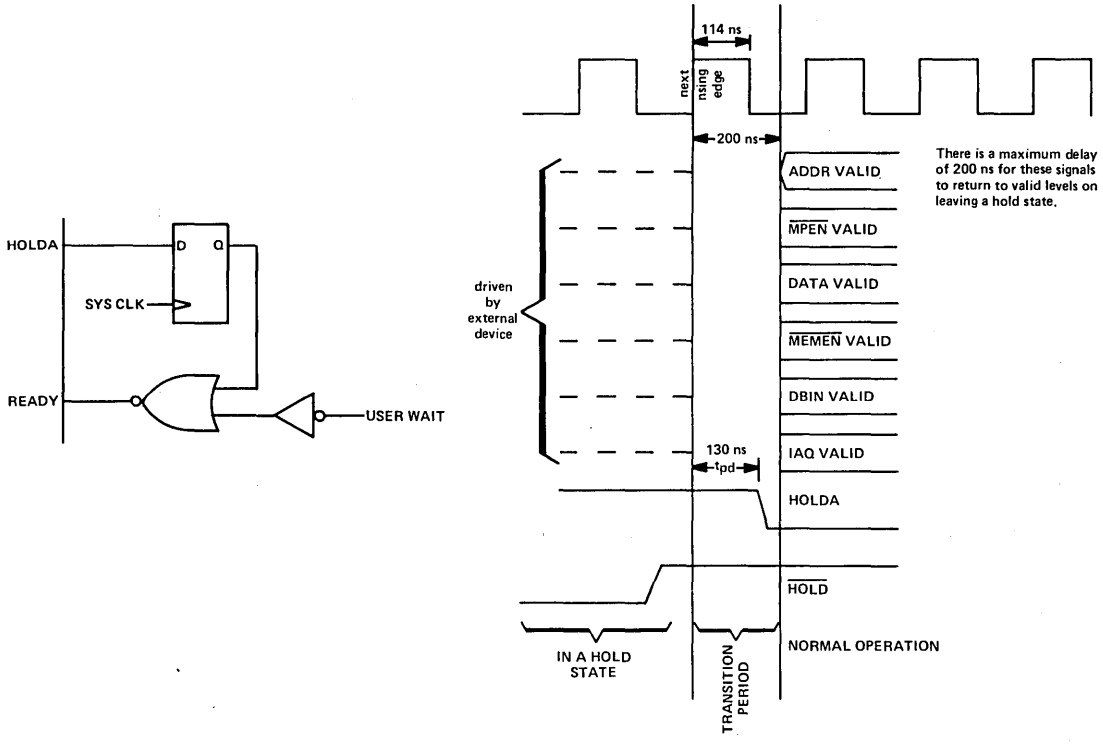
NOTE 1: The number of clock cycles is twenty plus twice the value of Bits (12 - 15) of WR0.

TABLE 1. ADDRESS MODIFICATION

ADDRESSING MODE	CLOCK CYCLES		MEMORY CYCLES
	SBP9989	Δ FROM SBP9900A	
WR (T_S or T_D = 00)	0		0
WR indirect (T_S or T_D = 01)	4		1
WR indirect auto-increment (T_S or T_D = 11)	6	0 to −2	2
Symbolic (T_S or T_D = 10, S or D = 0)	6	−2	1
Indexed (T_S or T_D = 10, S or D = 0)	6	−2	2

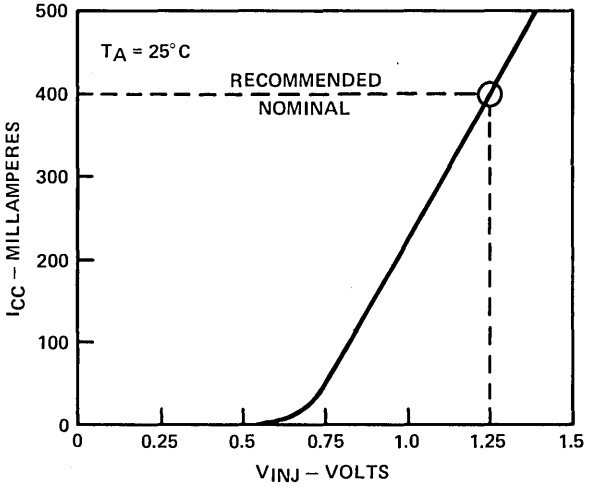
Leaving a Hold State

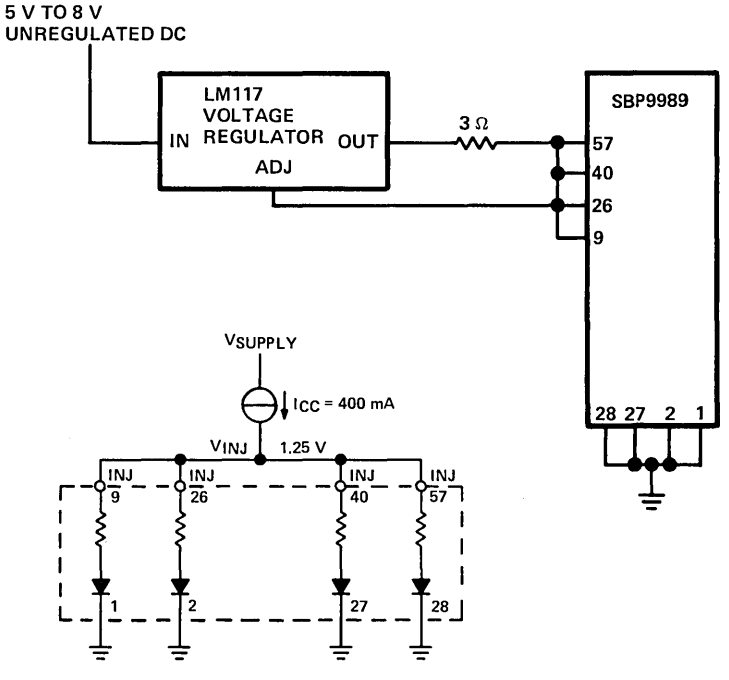
When the SBP9989 leaves a hold state, the time required for the signals to return to their proper levels is different from the other delay times. This difference is on the order of 10 to 20 nanoseconds. If your system does not use hold states or can tolerate the longer delay times, there will be no problems. If these delay times are too long, add a wait state at the end of a hold state to allow the signals to come to their proper levels as shown in Figure 8.



POWER SOURCE

I^2L is a current-injected logic. When the injector and ground pins are placed across a curve tracer, the processor V-I characteristic will resemble that of a silicon diode. Although any voltage or current source capable of supplying the desired current at the injector voltage required will suffice, a regulated current source is recommended. This is because the injector voltage will vary over the temperature range. One approach to a suitable, highly stable regulator is shown in the figure below.





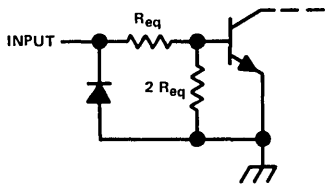
PROCESSING

These devices are processed in accordance with Method 5004 of MIL-STD-883B.

ELECTRICAL DATA

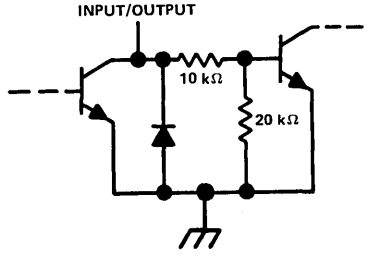
EQUIVALENT SCHEMATICS

EQUIVALENT OF EACH INPUT

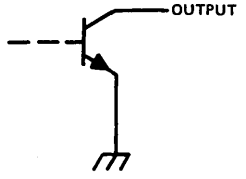


CLOCK: R_{eq} = 5 kΩ
ALL OTHER: R_{eq} = 10 kΩ

EQUIVALENT OF EACH INPUT/OUTPUT



TYPICAL OF ALL OUTPUTS



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply current, I_{CC}		380	400	420	mA
High-level output voltage, V_{OH}				5.5	V
Low-level output current, I_{OL}				16	mA
Clock frequency, f_{clock}		0		4.4	MHz
Width of clock pulse, t_w		114			ns
Clock rise time, t_r				20	ns
Clock fall time, t_f				20	ns
Setup time, t_{su}	$\overline{HOLD}$	0			ns
	READY	25			
	D0 - D15	45			
	CRUIN	70			
	$\overline{INTREQ}$	55			
	IC0 - IC3	55			
	$\overline{XIPP}$	50			
	$\overline{LOAD}$	20			
	$\overline{RESET}$	0			
Hold time, t_h	$\overline{HOLD}$	20			ns
	READY	30			
	D0 - D15	35			
	CRUIN	25			
	$\overline{INTREQ}$	25			
	IC0 - IC3	25			
	$\overline{XIPP}$	5			
	$\overline{LOAD}$	25			
	$\overline{RESET}$	45			
Operating free-air temperature, T_A	SBP9989NJ, SBP9989NFD	−55		125	°C

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

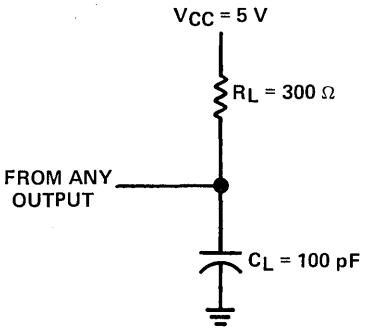
ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING TEMPERATURE RANGE

PARAMETER			TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage		I_{CC} = NOM		2			V
V_{IL}	Low-level input voltage		I_{CC} = NOM				0.7	V
V_{IK}	Input clamp voltage		I_{CC} = NOM,	I_{IH} = –12 mA			–1.5	V
I_{OH}	High-level output current	I/O Pins	I_{CC} = NOM,	V_{IH} = 2 V,			1000	µA
		Other outputs	V_{IL} = 0.7,	V_{OH} = 5.5 V			250	
V_{OL}	Low-level output voltage		I_{CC} = NOM, V_{IL} = 0.7 V,	V_{IH} = 2 V, I_{OL} = 16 mA			0.4	V
I_{IH}	Input current	Clock	I_{CC} = NOM,	V_{IN} = 2.4 V			600	µA
		Other inputs					300	
V_{INJ}	Injector voltage		I_{CC} = NOM			1.25		V

†For test conditions shown as NOM, see the appropriate value under Recommended Operating Conditions.

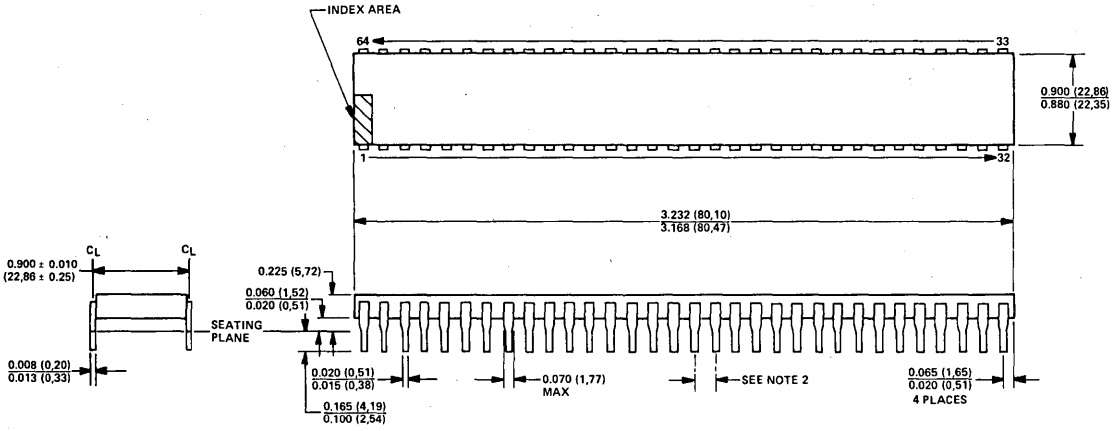
SWITCHING CHARACTERISTICS OVER RECOMMENDED OPERATING TEMPERATURE RANGE

PARAMETER	FROM	TO	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PD}	CLK↑	Address bus (A0 - A14)	C_L = 100 pF			140	ns
	CLK↑	Memory map enable ($\overline{MPEN}$)				140	
	CLK↑	Data bus (D0 - D15)				140	
	CLK↓	Write enable ($\overline{WE}$)				180	
	CLK↑	Cycle end ($\overline{CYCEND}$)				175	
	CLK↑	Data bus in (DBIN)				145	
	CLK↑	Memory enable ($\overline{MEMEN}$)				140	
	CLK↑	↑CRU clock (CRUCLK)				185	
	CLK↓	↓CRU clock (CRUCLK)				185	
	CLK↑	CRU data out (CRUOUT)				175	
	CLK↑	Hold acknowledge (HOLDA)				130	
	CLK↑	Wait				130	
	CLK↑	Instruction Acquisition (IAQ)				130	
	CLK↑	Multiprocessor interlock (MPILCK)				135	
	CLK↑	Interrupt acknowledge (INTACK)				150	
t_{PD}	CLK↑	Address bus (A0 - A14)	When leaving a Hold State, C_L = 100 pF			200	ns
	CLK↑	Memory map enable ($\overline{MPEN}$)				200	
	CLK↑	Data bus (D0 - D15)				200	
	CLK↑	Memory enable ($\overline{MEMEN}$)				200	
	CLK↑	Data bus in (DBIN)				200	
	CLK↑	Instruction Acquisition (IAQ)				200	



SWITCHING-TIME LOAD CIRCUIT

64-PIN CERAMIC DUAL-IN-LINE PACKAGE



NOTES: 1. Dimensions are in inches and parenthetically in millimeters.
2. Pin spacing is .100 (2.54 mm) between centerlines. Each pin centerline shall be located within ±.010 (.25 mm) of its exact longitudinal position relative to pin 1 and 64.

68-TERMINAL CHIP CARRIER

INFORMATION AVAILABLE SOON

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

Miscellaneous 9900 Family Products

SBP/TMS 9900 TRANSPORTABLE CROSS-SUPPORT SOFTWARE PRODUCT DESCRIPTION

- ## PACKAGING

The SBP/TMS 9900 transportable cross-support package, which is now available for sales and distribution, is composed of three distinct products: 9900 Cross Assembler, Simulator, and ROM Utility. The part number for the package is *TMSW101T-18.* The *Product Name* is *TMS 9900 Transportable Cross-Support Software.* Initially, the package will be manufactured only on *½ inch, 9 track PE encoded* (IBM compatible) magnetic tape recorded at *1600 BPI.* The tape will be *un-labeled, un-blocked* with *80 ASCII bytes per data record* and will contain *131 files.* The first file on the tape is a data file which contains:

a) A one-time descriptor for each file on the tape

b) A bill of materials (to verify that the complete package has been received), and

c) An errata list of problems and known solutions for the software version on that tape.

Each file on the tape is terminated by an EOF mark except for the last file which is terminated with a double EOF to indicate *end-of-logical tape.*

Included in the shipping package is a *User Manual* for each of the three programs and an *Installation Manual* covering each of the three programs (4 manuals, total).

- ## OPERATING ENVIRONMENT

The programs are written to conform to ANSI STANDARD X3.0 (1966) 16-BIT FORTRAN and are designed to execute on any minicomputer with the following minimum characteristics.

1) ANSI STANDARD X3.0 (1966) 16-BIT FORTRAN COMPILER

2) Two's complement arithmetic

3) Disc capacity for up to 7 simultaneously active sequential files.

4) A 20K-word user program-memory partition.

To date, the package has been extensively tested on the TI 990/10 under DX10V2.2, DEC PDP11/10 under RSX-11M (FIN IV PLUS), and System 370/160 under MVS.

- ## 9900 CROSS ASSEMBLER DESCRIPTION

The SBP/TMS 9900 Assembly Language source is translated by the 9900 Cross Assembler into relocatable linkable SBP/TMS 9900 Object module format. Both the source input and the object output are fully compatible with the AMPL Prototype Development System.

- ## SBP/TMS 9900 SIMULATOR DESCRIPTION

Object modules generated by the Cross Assembler along with "link-control" statements are input to the first stage of the simulator. The output from this stage, an *absolute,* non-relocatable load module, plus simulation/debug control statements to the second stage of simulation. This stage may be operated in "batchmode" or interactively (e.g., the simulation/debug control stream is entered to the Simulator from a Keyboard/Display device). In this second phase of Simulation the user's program logic is verified and the program's performance characteristics are ascertained. Performance parameterization is supported for considerations such as target system clock speed, memory characteristics, and I/O part descriptions. Debug features include multiple breakpoints, full instruction trace and snapshots, plus the normal inspect/modify for CPU registers. All program references may be made symbolically, using symbols defined in the user's source program.

- ## ROM UTILITY DESCRIPTION

When the application program has been satisfactorily verified, the object module may be input to the ROM Utility Program for translation into a format acceptable for production of a gate placement program (preparatory to mass production). Alternatively, the utility may be used to generate a BNPF formatted file which may be input to a PROM Programmer (DATA I/O) to produce a PROM version of the program. In all, there are 12 acceptable input formats and 12 output formats in support of the TMS 1000 and the SBP/TMS 9900 microprocessors.

AMPL . . . A COMPLETE MICROPROCESSOR PROTOTYPING LAB

The AMPL* Microprocessor Prototyping Lab combines the high performance 990 computer with the low-cost flexibility of the floppy disk to provide a complete microprocessor prototyping lab. The AMPL lab provides in-circuit emulation support, logic-state trace and analysis, read-only memory implementation aids, and SBP 9900A software development support. This microprocessor lab provides the user a dedicated design center where 9900-based systems can be developed in an integrated software-hardware design and debug sequence. Substantial savings in design cost and design time in each phase of new product development is ensured with this system.

Multi-AMPL Systems: Highest performance . . . lowest cost per user

An entire team can now develop software and hardware simultaneously using a single system. The hard-disk Multi-AMPL* Systems from Texas Instruments allow as many as eight program designers to work at the same time. Software investment per user is reduced by maintaining a single data base, program time is cut drastically, and the lowest possible cost per user is achieved.

Multi-AMPL Systems are available in three configurations designed to meet particular needs. Each system is a complete set of software and hardware tools providing multiple processor emulation and concurrent multi-task operation: compile, assemble, debug, edit, print. Also included are data and address trace, data and address breakpoints, a high-level debug and test procedure language, and EPROM and PROM programming. The systems support Microprocessor Pascal, Component Software, and Fortran languages.

AMPL SYSTEMS

DESCRIPTION	MULTI-AMPL PACKAGED SYSTEMS			SINGLE-USER SYSTEM
	TMAM9010	TMAM9020	TMAM9040	TMAM9000
Main Memory (BYTES)	256K	256K	320K	64K
Total Disk Storage (Formatted BYTES)	9.4M	18.8M	89.4M	2.2M
No. of Disk Drives	1(DUAL)	2(DUAL)	2	2 DSDD
Fixed Disk Storage	1-4.7M	2-4.7M		
Removable Disk Storage (BYTES)	4.7M	2-4.M	2-44.7M	2-1.1M
No. Terminals Included	1	2	4	1
AMPL Station Link	Yes	Yes	Yes	Yes
Software	Multi-Amplus O.S. Macro Assembler AMPL Utility Diagnostic Text Editor Link Editor PROM Programming Utility			9900 Amplus Assembler AMPL Utility

In-Circuit Emulation Support

The SBP 9900A in-circuit emulation feature includes the SBP 9900A emulator, SBP 9900A buffer, and SBP 9900A target connector. This feature allows the SBP 9900A microprocessor-based system design engineer to simulate his target system by utilizing the dedicated 4096 words of emulator memory and the SBP 9900A microprocessor emulator. All functions of the proposed system can be simulated except input/output, and benchmark data can be tabulated.

SBP 9900A emulation is designed to aid the design engineer through each stage of his prototype implementation. Emulation control provided by the FS9900 system allows the design engineer to step through the developed code, setting breakpoints and instruction traces to start/stop tests at desired points within his code.

Two significant advantages included in the emulation feature are the use of dedicated emulator memory and the ability under interactive software control to switch back and forth between target system memory and emulator memory. The dedicated 4096 16-bit words of emulator memory provides a significant speed advantage over systems which utilize host system memory on a cycle-stealing basis. The faster, dedicated emulator is designed so that this dedicated memory can have precedence over target system memory so that even after target system memory is implemented, 9900 code changes can be quickly evaluated and tested before implementing this change in target system ROM/PROM.

Logic-State Trace

The logic-state trace feature adds a dramatic new dimension to the integration and checkout of the target system.

The AMPL system trace/emulation features interactive on-line control and analysis to provide fast data reduction and programmable emulation control based on the results of this analysis.

The trace feature can be interconnected with the emulator module or it can utilize the general-purpose Trace Data Probe. When interconnected to the emulator, the design engineer can trace 256 events of both address and 16-bit data. The Trace Data Probe provides 20 individual logic-line trace probes.

These probes can be used by the design engineer to trace any TTL logic lines desired in his target system. The sampling rate can be controlled by a 10-megahertz internal clock or by an external clock up to 10 megahertz. Of the 20 trace probes, 4 have a special glitch latch feature and can detect noise pulses down to 10 nanoseconds in width.

In addition to the 20 trace data probes, 4 general-purpose trace clock qualifier probes are provided to allow the user to prequalify trace conditions based on logic-state conditions within his target system. By using the interactive programming features within the host system, the design engineer can define procedures and functions to automatically process incoming trace data from these events, perform data reduction looking for defined conditions, display or print only the desired results, or branch into other emulation/trace procedures. Thus, for example the design engineer can set qualifying conditions and start trace and emulation in a continuous cycle while looking for those random troublesome noise glitches. Upon detecting a glitch, the trace/emulation cycle can be programmed to pause momentarily, analyze and print conditions, and then continue the trace/emulation sequence looking for the next glitch. This feature can mean tremendous savings in manpower and design checkout time since the full speed and power of the 990 computer is processing the problem.

Microprocessor Pascal System

TI's Microprocessor Pascal system, developed for the 16-bit 9900 Family, provides an increased applications capability and decreases development time. TI Microprocessor Pascal is third-generation Pascal resulting from TI's pioneering efforts with the language. It allows designers to solve applications problems without becoming involved with the intricacies of machine architecture. The code is easier to write, document, read, and modify, and results in fewer programming errors. Direct CRU commands are available for direct bit and byte manipulation. Microprocessor Pascal has concurrency extensions particularly suitable for realtime multitasking applications.

TI's Microprocessor Pascal system consists of five parts:

- Source Editor – Specifically designed to create/edit Pascal programs and check program syntax before compilation.
- Compiler – Compiles conventional Pascal programs as well as TI's Pascal concurrent extensions into interpretive code, which can then be executed directly or converted to 9900 native machine code.
- Host Debugger – More than 15 options for tracing variables and modifying data.
- Configurator – Enables the target system to retain only the part of the runtime support necessary for program execution.
- Run-Time Support – Both interpretive and native-code execution provide a speed/memory tradeoff.

Programmable Logic Arrays

* 'ALS VERSIONS OF 4 POPULAR PAL®* DEVICES

  TWICE AS FAST, TYPICAL PROPAGATION DELAY . . . 12NS

  IDENTICAL PROGRAMMING PROCEDURE

  PIN FOR PIN COMPATIBLE

DESCRIPTION

THESE FIXED-OR ARRAYS (THREE-STATE OUTPUTS) COMBINE THE ADVANCED LOW-POWER SCHOTTKY TECHNOLOGY WITH PROVEN TIW FUSE LINKS TO PROVIDE A RELIABLE, HIGH-PERFORMANCE REPLACEMENT FOR CONVENTIONAL TTL, WITH THE ADVANTAGE OF QUICK DESIGN CHANGES AND MORE COMPACT BOARDS.

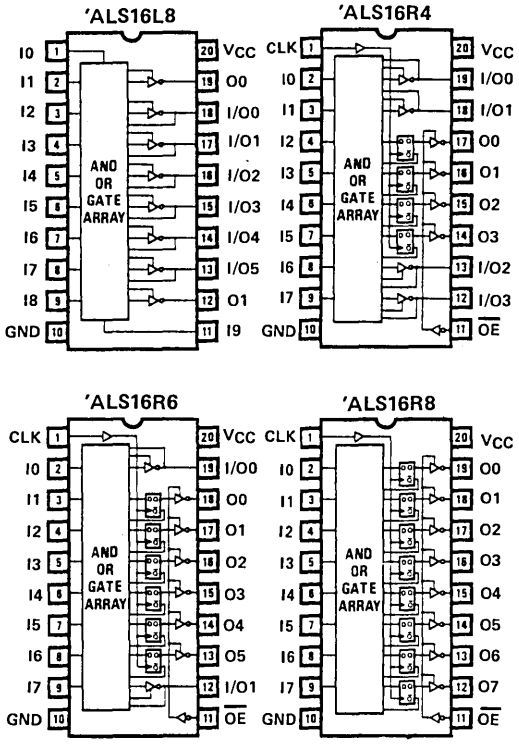
THE DEVICES WITH REGISTERS STORE THE OUTPUT OF THE AND-OR ARRAY ON THE LOW-TO-HIGH TRANSITION OF THE CLOCK.

ORDERING INFORMATION

FP 74ALS 16 R 6 N

* PREFIX
  - FP-STANDARD PREFIX
  - FPJ-MIL STD 883B
* 74 - 0°C TO 70°C
  - 54 - -55°C TO 125°C
  - ALS - ADVANCED LOW-POWER SCHOTTKY PROCESS
* NUMBER OF ARRAY INPUTS
* OUTPUT TYPES:
  - L - ACTIVE LOW
  - R - REGISTERED
* NUMBER OF SPECIAL OUTPUTS
* PACKAGE TYPE

J OR N PACKAGE (TOP VIEW)



PROGRAMMERS		
MANUFACTURER	PERSONALITY CARD	SOCKET ADAPTOR
STRUCTURED DESIGN	SD-20/24	
DATA I/O CORP.	SYSTEM 19 919-1427	715-1428-2
PRO-LOG CORP.	PM9068	
CITEL CO.	SYS 37,CP37-1	
KONTRON CORP.	MPP 80	
STAG SYSTEMS INC.	PM202-2	

PART #	DESCRIPTION
'ALS16L8	OCTAL 16-INPUT AND-OR-INVERT GATE ARRAY
'ALS16R8	OCTAL 16-INPUT REGISTERED AND-OR GATE ARRAY
'ALS16R6	HEX 16-INPUT REGISTERED AND-OR GATE ARRAY
'ALS16R4	QUAD 16-INPUT REGISTERED AND-OR GATE ARRAY

*PAL IS THE REGISTERED TRADEMARK OF MONOLITHIC MEMORIES, INC.

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, V_{CC}	7V
INPUT VOLTAGE	5.5V
OFF-STATE OUTPUT VOLTAGE	5.5V
STORAGE TEMPERATURE	-65° TO 150°C

RECOMMENDED OPERATING CONDITIONS

		FP54ALS'			FP74ALS'			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
V_{CC}	SUPPLY VOLTAGE	4.5	5	5.5	4.75	5	5.25	V
I_{OH}	HIGH-LEVEL OUTPUT CURRENT			-1			-2.6	mA
I_{OL}	LOW-LEVEL OUTPUT CURRENT			12			24	mA
T_A	OPERATING FREE-AIR TEMPERATURE	-55		125	0		70	°C

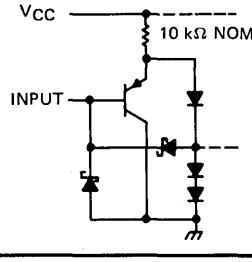
ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)

PARAMETER		TEST CONDITIONS		FP54ALS' MIN	FP54ALS' TYP*	FP54ALS' MAX	FP74ALS' MIN	FP74ALS' TYP*	FP74ALS' MAX	UNIT
V_{IH}	HIGH-LEVEL INPUT VOLTAGE			2			2			V
V_{IL}	LOW-LEVEL INPUT VOLTAGE					0.8			0.8	V
V_{IK}	INPUT CLAMP VOLTAGE	V_{CC} = MIN, I_I = -18mA				-1.5			-1.5	V
V_{OH}	HIGH-LEVEL OUTPUT VOLTAGE	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = 2V		2.4	3.2		2.4	3.3		V
V_{OL}	LOW-LEVEL OUTPUT VOLTAGE	V_{CC} = MIN, V_{IH} = 2V, I_{OL} = MAX, V_{IL} = 0.8V			0.25	0.4		0.35	0.5	V
I_I	INPUT CURRENT AT MAX INPUT VOLTAGE	V_{CC} = MAX, V_{IH} = 5.5V				0.1			0.1	mA
I_{IH}	HIGH-LEVEL INPUT CURRENT	V_{CC} = MAX, V_{IH} = 2.7V				20			20	uA
I_{IL}	LOW-LEVEL INPUT CURRENT	V_{CC} = MAX, V_{IL} = 0.4V				-0.4			-0.4	mA
I_O	OUTPUT CURRENT	V_O = 2.25V		-15	-33	-65	-15	-33	-65	mA
I_{OZH}	OFF-STATE OUTPUT CURRENT, HIGH-LEVEL VOLTAGE APPLIED	V_{CC}=MAX, V_{IH}=2V, V_{IL}=.8V, V_O=2.7V	0 PINS			20			20	uA
			I/O PINS			100			100	
I_{OZL}	OFF-STATE OUTPUT CURRENT, LOW-LEVEL VOLTAGE APPLIED	V_{CC}=MAX, V_{IH}=2V, V_{IL}=.8V, V_O=0.4V	0 PINS			-20			-20	uA
			I/O PINS			-100			-100	
I_{CC}	SUPPLY CURRENT	V_{CC}=MAX, V_I=0V, OUTPUTS OPEN	16L8		110	210		110	180	mA
			16R8,6,4		115	225		115	190	

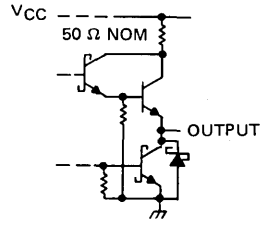
*ALL TYPICAL VALUES ARE AT V_{CC} = 5 V, T_A = 25°C

SCHEMATICS OF INPUTS AND OUTPUTS

EQUIVALENT OF EACH INPUT



TYPICAL OF OUTPUTS



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

'ALS16R8, 'ALS16R6, 'ALS16R4 TIMING REQUIREMENTS

		MIN	MAX	UNIT
CLOCK FREQUENCY, FCLOCK		0	35	MHz
WIDTH OF CLOCK PULSE, TW	HIGH	12		NS
	LOW	12		
SETUP TIME FROM INPUT OR FEEDBACK, TSU		15		NS
HOLD TIME, TH		0		NS

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS	FP54ALS' MIN	FP54ALS' TYP	FP54ALS' MAX	FP74ALS' MIN	FP74ALS' TYP	FP74ALS' MAX	UNIT
FMAX	MAXIMUM CLOCK FREQUENCY		35			35			MHz
TPLH	INPUT OR FEEDBACK TO NON-REGISTERED OUTPUT	R_L = 667 OHM TO V_{CC}, C_L = 45PF			12			12	NS
TPHL					12			12	
TPLH	CLOCK TO OUTPUT OR FEEDBACK NOT APPLICABLE TO '16L8				10			10	NS
TPHL					10			10	
TPZH	OUTPUT ENABLE TIME FROM $\overline{OE}$ NOT APPLICABLE TO '16L8	R_L = 667 OHM TO V_{CC}, C_L = 5PF			8			8	NS
TPZL					8			8	
TPHZ	OUTPUT DISABLE TIME FROM $\overline{OE}$ NOT APPLICALBE TO '16L8				8			8	NS
TPLZ					8			8	
TPZH	OUTPUT ENABLE TIME FROM I INPUT NOT APPLICABLE TO '16R8				12			12	NS
TPZL					12			12	
TPHZ	OUTPUT DISABLE TIME FROM I INPUT NOT APPLICABLE TO '16R8				12			12	NS
TPLZ					12			12	

PROGRAMMING PARAMETERS, T_A = 25°C

PARAMETER			MIN	NOM	MAX	UNIT
VIHH	PROGRAM-LEVEL INPUT VOLTAGE		11	11.5	12	V
IIHH	PROGRAM-LEVEL INPUT CURRENT	OUTPUT PROGRAM PULSE			50	MA
		$\overline{OE}$, I/R			25	
		ALL OTHER INPUTS			5	
ICCH	PROGRAM SUPPLY CURRENT				400	MA
TP	PROGRAM PULSE WIDTH		10		50	US
TD	DELAY TIME		100			NS
TDV	DELAY TIME TO VERIFY		100			US
	PROGRAM PULSE DUTY CYCLE				25	%
	VERIFY-PROTECT-INPUT VOLTAGE		20	21	22	V
	VERIFY-PROTECT-INPUT CURRENT				400	MA
	VERIFY-PROTECT-PULSE WIDTH		20		50	MS

5

Programming Procedure

The fuses are programmed using a low-voltage linear-select procedure. The array is divided into two groups, products 0 thru 31 and products 32 thru 63, for which pin identifications are shown in the pin configurations on following page. To program a particular fuse, both an input line and a product line are selected according to the following procedure:

Step 1 Raise Output Enable, $\overline{OE}$, to V_{IHH}.
Step 2 Select an input line by applying voltages to I_0, I_1, I_2, I_3, I_4, I_5, I_6, I_7, and L/R, as shown in Table 1.
Step 3 Select a product line by applying voltages to A_0, A_1, and A_2 as shown in Table 2.
Step 4 Raise V_{CC} (pin 20) to V_{IHH}.
Step 5 Program the fuse by pulsing the output O3, O2, O1, or O0 of the selected product group to V_{IHH} as shown in Table 2.
Step 6 Lower V_{CC} (pin 20) to 6.0 V.
Step 7 Pulse the CLOCK pin and verify the output pin, O3, O2, O1, or O0 to be Low.
Step 8 Lower V_{CC} (pin 20) to 4.5 V and repeat step 7.
Step 9 Should the output not verify, repeat steps 1 thru 8 up to five (5) times.

This procedure is repeated for all fuses to be blown (see Programming Waveforms).

To prevent further verification, two last fuses may be blown by raising pin 1 and pin 11 to V_P. V_{CC} is not required during this operation.

Voltage Legend:
L = Low-level input voltage, V_{IL} HH = High-level program, V_{IHH}
H = High-level input voltage, V_{IH} Z = High impedance (e.g., 10 kilohms to 5 V)

INPUT LINE NUMBER	PIN IDENTIFICATION								
	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	L/R
0	HH	HH	HH	HH	HH	HH	HH	L	Z
1	HH	HH	HH	HH	HH	HH	HH	H	Z
2	HH	HH	HH	HH	HH	HH	HH	L	HH
3	HH	HH	HH	HH	HH	HH	HH	H	HH
4	HH	HH	HH	HH	HH	HH	L	HH	Z
5	HH	HH	HH	HH	HH	HH	H	HH	Z
6	HH	HH	HH	HH	HH	HH	L	HH	HH
7	HH	HH	HH	HH	HH	HH	H	HH	HH
8	HH	HH	HH	HH	HH	L	HH	HH	Z
9	HH	HH	HH	HH	HH	H	HH	HH	Z
10	HH	HH	HH	HH	HH	L	HH	HH	HH
11	HH	HH	HH	HH	HH	H	HH	HH	HH
12	HH	HH	HH	HH	L	HH	HH	HH	Z
13	HH	HH	HH	HH	H	HH	HH	HH	Z
14	HH	HH	HH	HH	L	HH	HH	HH	HH
15	HH	HH	HH	HH	H	HH	HH	HH	HH
16	HH	HH	HH	L	HH	HH	HH	HH	Z
17	HH	HH	HH	H	HH	HH	HH	HH	Z
18	HH	HH	HH	L	HH	HH	HH	HH	HH
19	HH	HH	HH	H	HH	HH	HH	HH	HH
20	HH	HH	L	HH	HH	HH	HH	HH	Z
21	HH	HH	H	HH	HH	HH	HH	HH	Z
22	HH	HH	L	HH	HH	HH	HH	HH	HH
23	HH	HH	H	HH	HH	HH	HH	HH	HH
24	HH	L	HH	HH	HH	HH	HH	HH	Z
25	HH	H	HH	HH	HH	HH	HH	HH	Z
26	HH	L	HH	HH	HH	HH	HH	HH	HH
27	HH	H	HH	HH	HH	HH	HH	HH	HH
28	L	HH	HH	HH	HH	HH	HH	HH	Z
29	H	HH	HH	HH	HH	HH	HH	HH	Z
30	L	HH	HH	HH	HH	HH	HH	HH	HH
31	H	HH	HH	HH	HH	HH	HH	HH	HH

TABLE 1 INPUT LINE SELECT

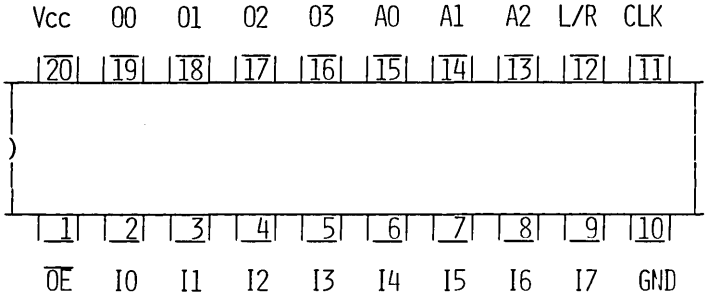
PRODUCT LINE NUMBER	PIN IDENTIFICATION						
	O_3	O_2	O_1	O_0	A_2	A_1	A_0
0,32	Z	Z	Z	HH	Z	Z	Z
1,33	Z	Z	Z	HH	Z	Z	HH
2,34	Z	Z	Z	HH	Z	HH	Z
3,35	Z	Z	Z	HH	Z	HH	HH
4,36	Z	Z	Z	HH	HH	Z	Z
5,37	Z	Z	Z	HH	HH	Z	HH
6,38	Z	Z	Z	HH	HH	HH	Z
7,39	Z	Z	Z	HH	HH	HH	HH
8,40	Z	Z	HH	Z	Z	Z	Z
9,41	Z	Z	HH	Z	Z	Z	HH
10,42	Z	Z	HH	Z	Z	HH	Z
11,43	Z	Z	HH	Z	Z	HH	HH
12,44	Z	Z	HH	Z	HH	Z	Z
13,45	Z	Z	HH	Z	HH	Z	HH
14,46	Z	Z	HH	Z	HH	HH	Z
15,47	Z	Z	HH	Z	HH	HH	HH
16,48	Z	HH	Z	Z	Z	Z	Z
17,49	Z	HH	Z	Z	Z	Z	HH
18,50	Z	HH	Z	Z	Z	HH	Z
19,51	Z	HH	Z	Z	Z	HH	HH
20,52	Z	HH	Z	Z	HH	Z	Z
21,53	Z	HH	Z	Z	HH	Z	HH
22,54	Z	HH	Z	Z	HH	HH	Z
23,55	Z	HH	Z	Z	HH	HH	HH
24,56	HH	Z	Z	Z	Z	Z	Z
25,57	HH	Z	Z	Z	Z	Z	HH
26,58	HH	Z	Z	Z	Z	HH	Z
27,59	HH	Z	Z	Z	Z	HH	HH
28,60	HH	Z	Z	Z	HH	Z	Z
29,61	HH	Z	Z	Z	HH	Z	HH
30,62	HH	Z	Z	Z	HH	HH	Z
31,63	HH	Z	Z	Z	HH	HH	HH

TABLE 2 PRODUCT LINE SELECT

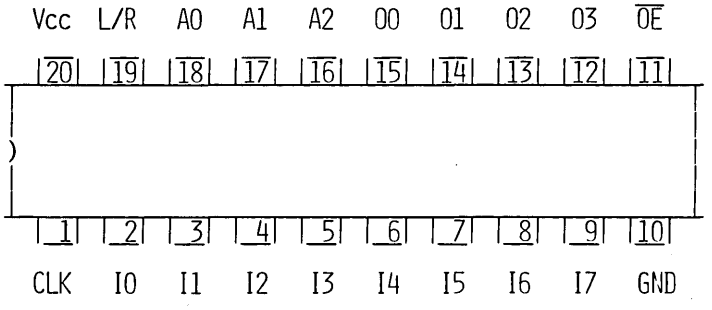
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

PIN CONFIGURATIONS FOR PROGRAMMING ONLY

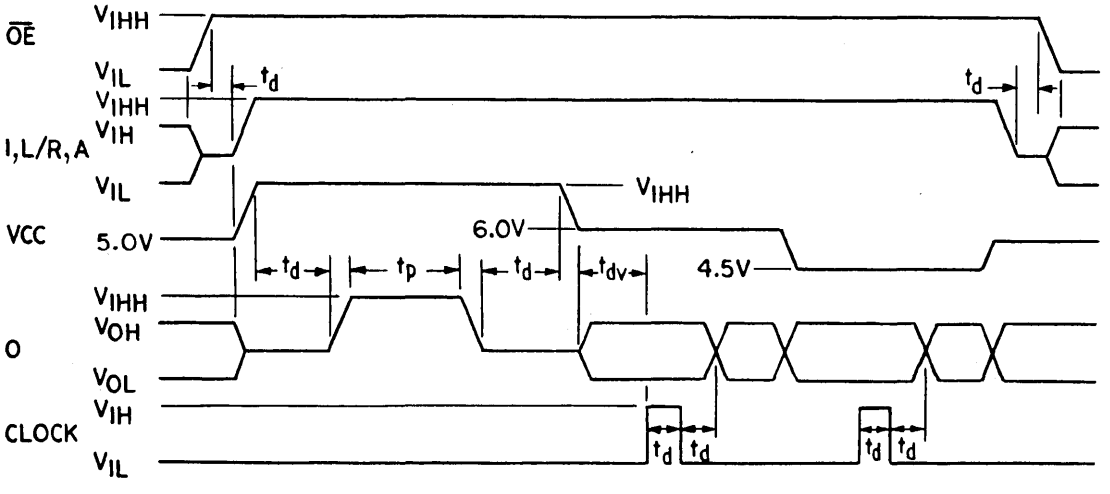
PRODUCTS 0 THRU 31



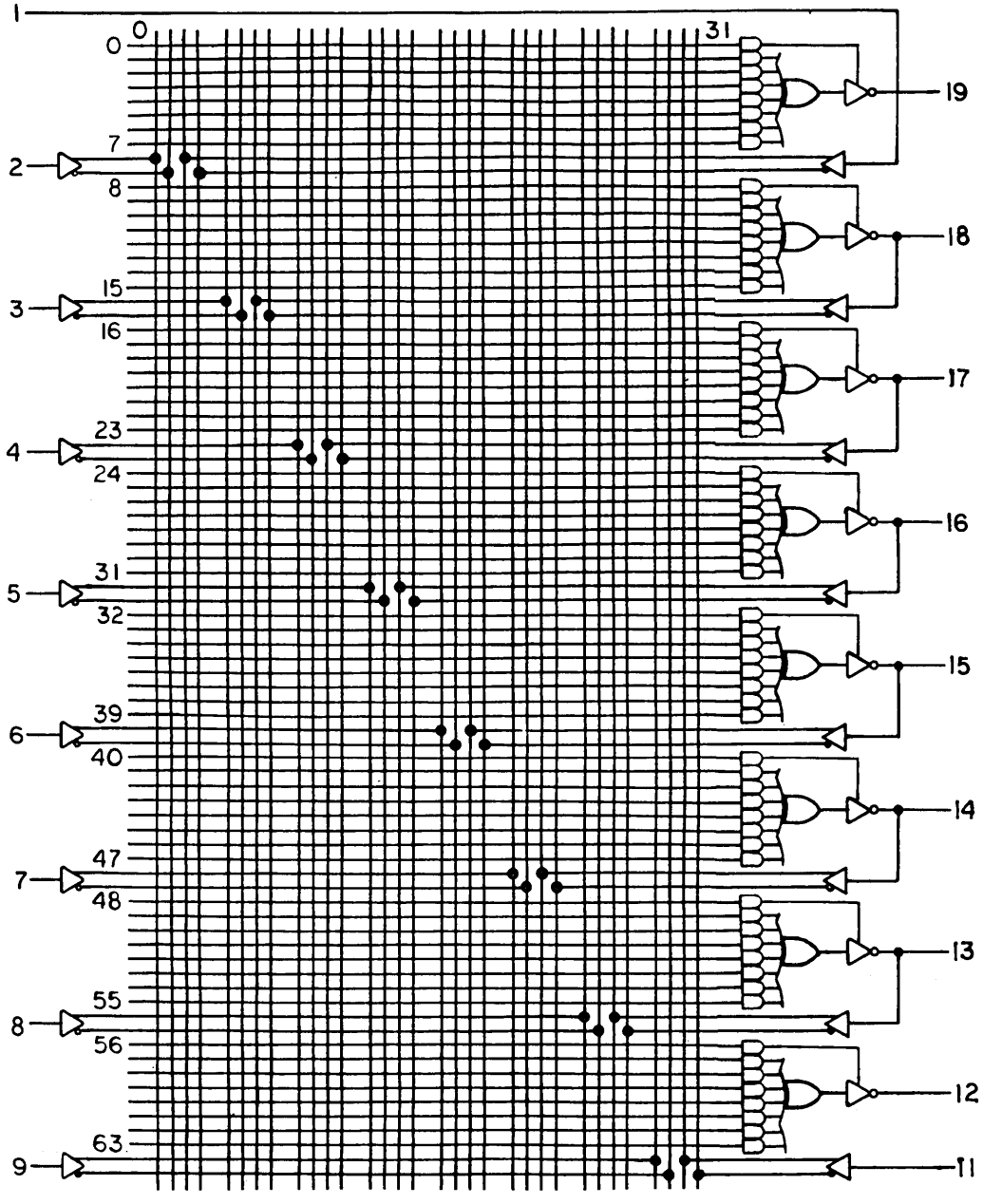
PRODUCTS 32 THRU 63



PROGRAMMING WAVEFORMS

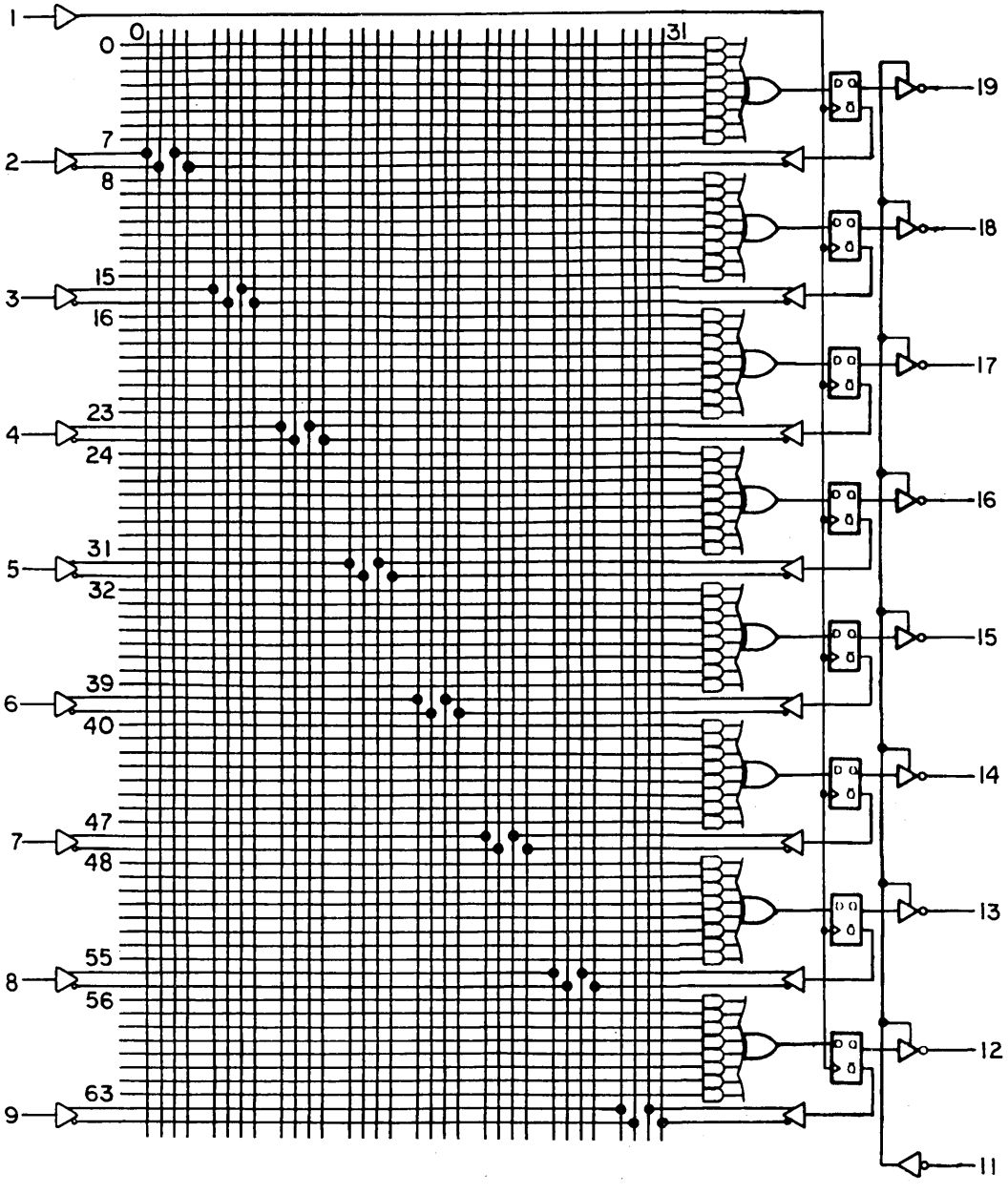


LOGIC DIAGRAM



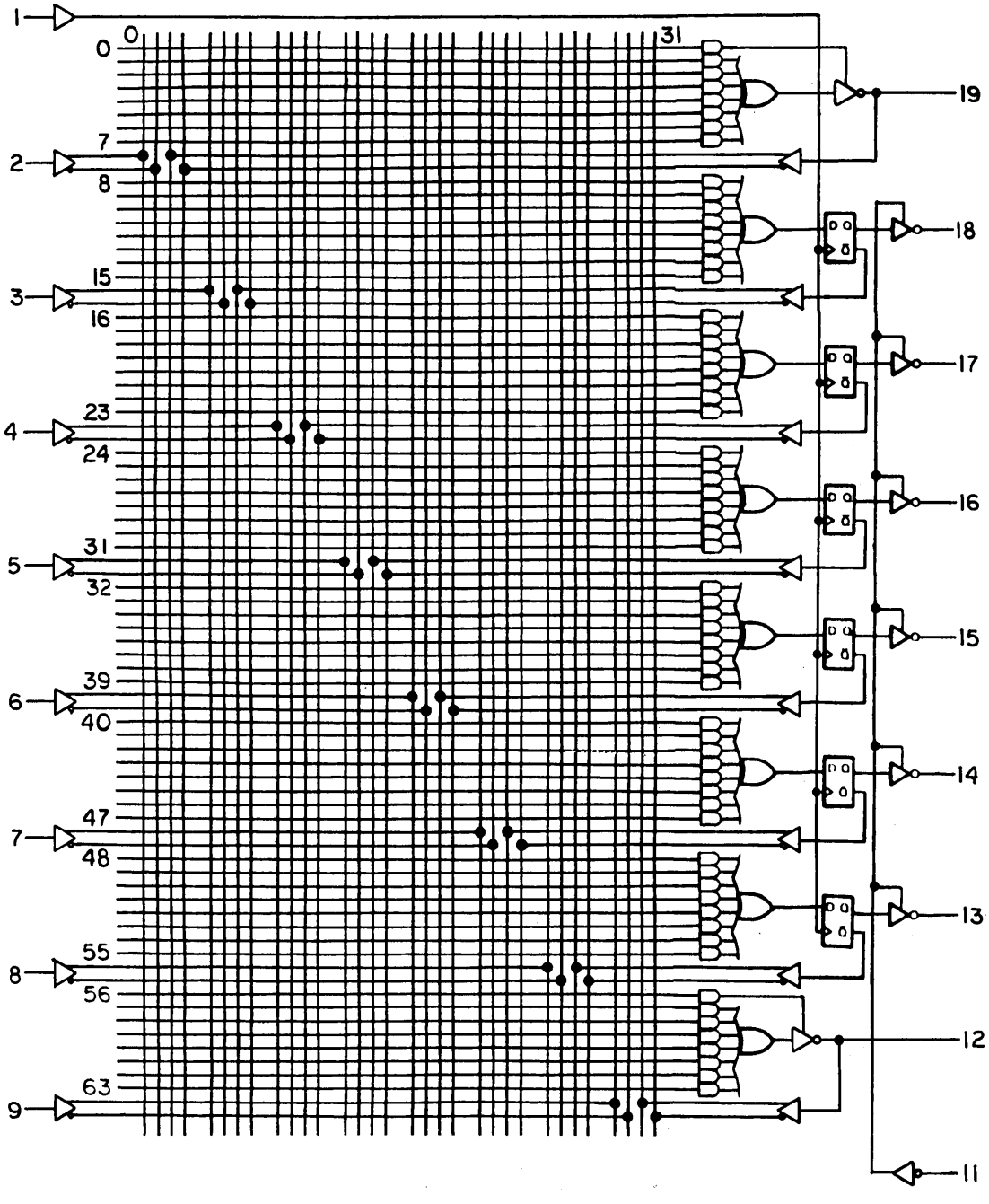
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

LOGIC DIAGRAM



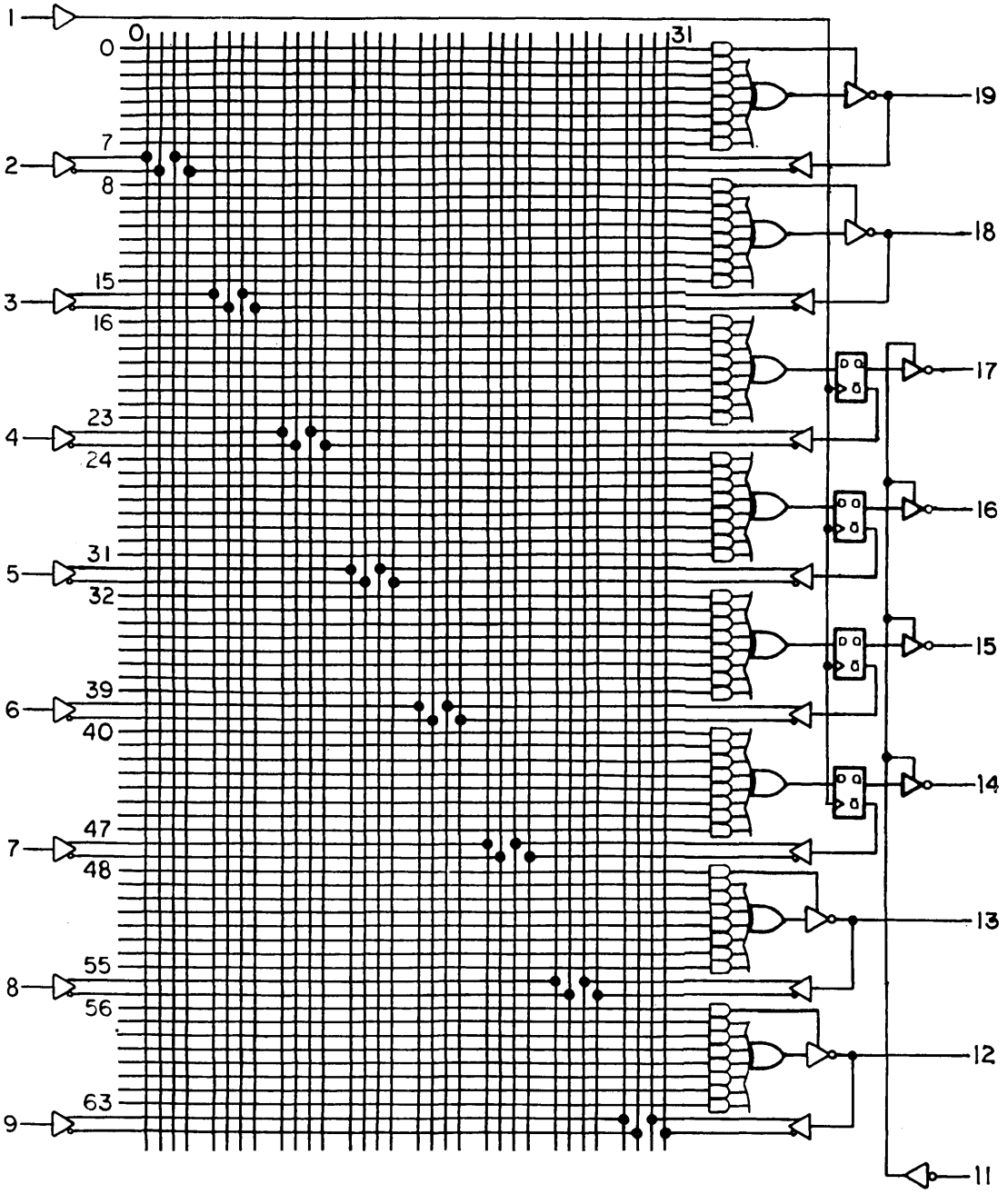
5

LOGIC DIAGRAM



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

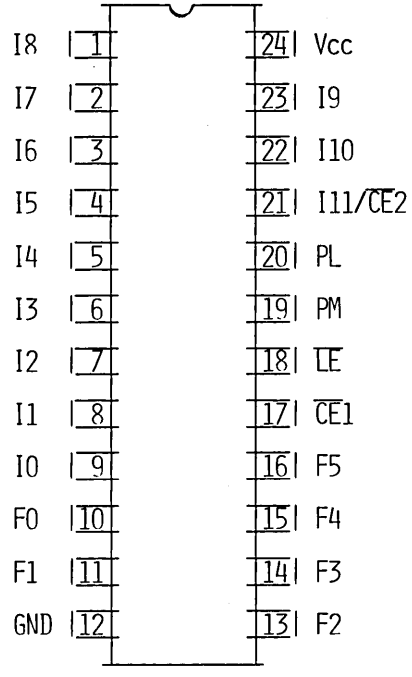
LOGIC DIAGRAM



5

- 45 ns TYPICAL INPUT to OUTPUT PROPAGATION DELAY
- 24-PIN, 300-mil SLIM LINE PACKAGES
- LOW-POWER, 350 mW TYPICAL POWER DISSIPATION
- 12 INPUT VARIABLES
- 32 PRODUCT TERMS
- 6-BIT OUTPUT LATCH
- 4-BIT STATE REGISTER

JT or NT PACKAGE
(TOP VIEW)



DESCRIPTION

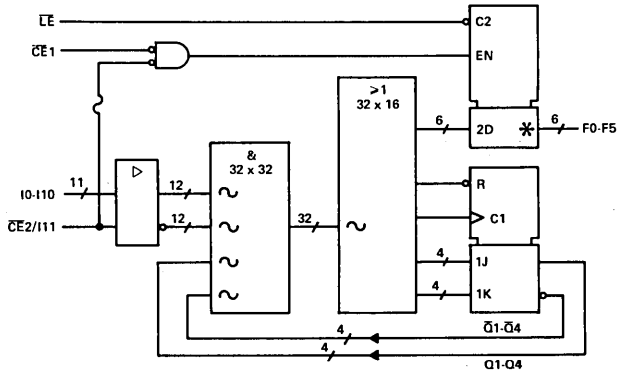
The 'LS333 (three-state outputs) and the 'LS335 (open-collector outputs) are Low-Power Schottky Bipolar TTL field-programmable logic sequencers designed to solve state-machine problems of the Mealy type. They contain four completely buried J-K flip-flops in the feedbath path between the OR and AND matrices. The common clock and clear lines are also programmable by separate OR terms, in addition to the four J inputs and four K inputs.

The output-function levels are stored by a common asynchronous latch enable pin ($\overline{LE}$) that controls the 6-bit output transparent latches.

Pin 21 is a user programmable option: it must be programmed to function as a 12th input or as a chip enable AND'ed with pin 17 for 3-state control of the outputs. An auto chip-enable option for expansion of terms is available through the manufacturer.

The program mode (PM), and the program latch (PL) pins are unique programming control inputs that simplify the programming procedure as described later. These pins are to be grounded during normal device operation.

FUNCTIONAL BLOCK DIAGRAM
(POSITIVE LOGIC)



denotes fused inputs.
* 'LS333 has 3-state (▽) outputs; 'LS335 has open-collector (Ω) outputs.

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

881

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, V_{CC}	7V
INPUT VOLTAGE	7V
OFF-STATE OUTPUT VOLTAGE	5.5V
STORAGE TEMPERATURE	-65° TO 150°C

RECOMMENDED OPERATING CONDITIONS

		FP54LS'			FP74LS'			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
V_{CC}	SUPPLY VOLTAGE	4.5	5	5.5	4.75	5	5.25	V
I_{OH}	HIGH-LEVEL OUTPUT CURRENT			-1			-2.6	mA
I_{OL}	LOW-LEVEL OUTPUT CURRENT			12			24	mA
T_A	OPERATING FREE-AIR TEMPERATURE	-55		125	0		70	°C

ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)

PARAMETER		TEST CONDITIONS	FP54LS' MIN	FP54LS' TYP*	FP54LS' MAX	FP74LS' MIN	FP74LS' TYP*	FP74LS' MAX	UNIT
V_{IH}	HIGH-LEVEL INPUT VOLTAGE		2			2			V
V_{IL}	LOW-LEVEL INPUT VOLTAGE				0.7			0.8	V
V_{IK}	INPUT CLAMP VOLTAGE	V_{CC}=MIN, I_I=-18mA			-1.5			-1.5	V
V_{OH}	HIGH-LEVEL OUTPUT VOLTAGE	V_{CC}=MIN, V_{IH}=2V, V_{IL}=MAX, I_{OH}=MAX	2.4	3.1		2.4	3.1		V
V_{OL}	LOW-LEVEL OUTPUT VOLTAGE	V_{CC}=MIN, V_{IH}=2V, V_{IH}=MAX, I_{OL}=MAX		0.25	0.4		0.25	0.4	V
I_I	INPUT CURRENT AT MAXIMUM INPUT VOLTAGE	V_{CC}=MAX, V_{IH}=5.5V			0.1			0.1	mA
I_{IH}	HIGH-LEVEL INPUT CURRENT	V_{CC}=MAX, V_{IH}=2.7V			20			20	uA
I_{IL}	LOW-LEVEL INPUT CURRENT	V_{CC}=MAX, V_{IL}=0.4V | PL			-0.4			-0.4	mA
		V_{CC}=MAX, V_{IL}=0.4V | ALL OTHER			-0.2			-0.2	mA
I_O	OUTPUT CURRENT	V_O=2.25V	-15		-65	-15		-65	mA
I_{OZH}	OFF-STATE OUTPUT CURRENT, HIGH-LEVEL VOLTAGE APPLIED	V_{CC}=MAX, CE1@2V, V_O=2.7V			20			20	uA
I_{OZL}	OFF-STATE OUTPUT CURRENT, LOW-LEVEL VOLTAGE APPLIED	V_{CC}=MAX, CE1@2V, V_O=2.7V			-20			-20	uA
I_{CC}	SUPPLY CURRENT	V_{CC}=MAX, CE1@4.5V, ALL OTHER INPUTS=0V		70			70		mA

*ALL TYPICAL VALUES ARE AT V_{CC} = 5V, T_A = 25°C

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TPLH, TPHL	INPUT TO OUTPUT	R_L = 667 OHMS, C_L = 45 pF			45	NS
TPLH, TPHL	CLOCK TO OUTPUT				65	NS
TPLH, TPHL	CLEAR TO OUTPUT				60	NS
TPXZ, TPZX	CE TO OUTPUT	R_L = 667 OHMS, C_L = 5 pF			20	NS
TPLH, TPHL	LE TO OUTPUT				25	NS
TPXZ, TPZX	AUTO CHIP ENABLE TO OUTPUT				50	NS

PROGRAMMING PARAMETERS, T_A = 25°C

	PARAMETER	MIN	NOM	MAX	UNIT
V_{IHH}	PROGRAM-LEVEL INPUT VOLTAGE	10	10.5	11	V
I_{CCH}	PROGRAM SUPPLY CURRENT		300		mA
TP	PROGRAM PULSE WIDTH	100		1000	us
TR	PROGRAM PULSE RISE TIME		100		NS
	PROGRAM PULSE DUTY CYCLE		25	35	%

Programming Procedure

I11/$\overline{CE2}$ INPUT

If pin 21 is to function as $\overline{CE2}$, both AND/$\overline{AND}$ links at each of the 32 product terms must be fused per AND matrix programming procedure creating a don't care for input I11. If it is to become the 12th data input, $\overline{CE2}$ is removed as follows:

Step 1: Set Vcc to 5 V, PM, PL, & GND to 0 V.
Step 2: Apply Vihh to IO-I11.
Step 3: Address product term 45 by applying its binary code to outputs F5 to F0 with F0 as LSB, using TTL logic levels, H=1 & L=0.
Step 4: a) Ramp PL to Vihh.
b) Pulse Vcc to Vihh.
c) Lower Vcc to 5 V.

AND MATRIX, input variables 0 to 11

Step 1: Set Vcc to 5V,PM,PL,& GND to 0 V.
Step 2: Latch out f/f outputs by applying Vih to IO-I4 and raising PL to 5V.
Step 3: Apply the true logic level to the input to be programmed and raise all remaining inputs to Vihh.
Step 4: Address the product term to be programmed (0-31).
Step 5: a) Ramp program latch (PL) to Vihh.
b) Pulse Vcc to Vihh for a MAX of 1 ms (35% duty cycle).
c) Return PL to 5 V.
Step 6: Disable the programmed input with Vihh.
Step 7: Repeat 3-6 for all other input variables and product terms.

AND MATRIX, Feedback input lines Q/$\overline{Q}$

Step 1: Set Vcc to 5 V, PM, PL, & GND to 0 V.
Step 2: Select the F/F output (to be programmed true) by applying TTL logic levels to inputs IO-I4 using the addresses in Table 1. Apply Vihh to I5-I11.
Step 3: Address the product term.
Step 4: a) Ramp PL to Vihh.
b) Disable inputs IO-I4 with Vihh.
c) Pulse Vcc to Vihh.
d) Return PL to 0V.
Step 5: Repeat 2-4 for all other Q/$\overline{Q}$ AND input lines and product terms.

OR MATRIX

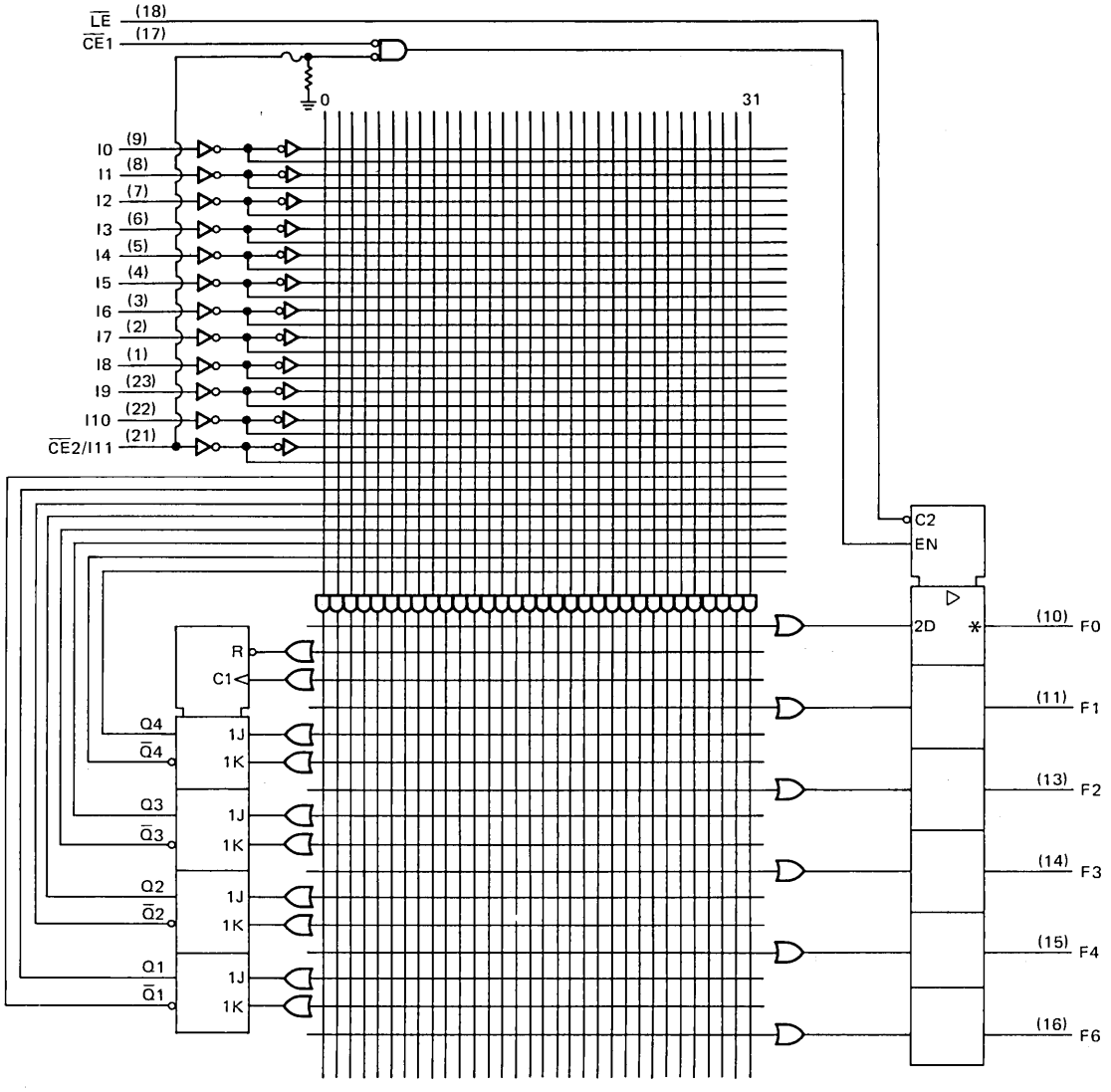
Step 1: Set Vcc to 5 V, PM to Vihh, PL and GND to 0 V.
Step 2: Select the output function or f/f input line by applying TTL logic levels to inputs IO to I4 using the addresses in Table 1. Apply Vihh to I5-I11.
Step 3: Ramp PL to 5 V.
Step 4: Disable inputs IO-I4 with Vihh.
Step 5: Address the product term.
Step 6: Pulse Vcc to Vihh.
Step 7: Repeat 5-6 for each of the product terms to be false in the addressed output function or f/f input line.
Step 8: Return PL to 0 V.
Step 9: Repeat 2-8 for each output function and f/f input line.

TABLE 1

ADDRESS APPLIED TO INPUTS I4 I3 I2 I1 I0	AND PROG MODE F/F OUTPUT TO BE TRUE	OR PROG MODE TERM TO BE FALSE IN SUM
L L L L L	$\overline{Q4}$	CLK
L L L L H	Q4	CLR
L L L H L	$\overline{Q3}$	J4
L L L H H	Q3	K4
L L H L L	$\overline{Q2}$	J3
L L H L H	Q2	K3
L L H H L	$\overline{Q1}$	J2
L L H H H	Q1	K2
L H L L L	NONE	J1
L H L L H		K1
L H L H L		F0
L H L H H		F1
L H H L L		F2
L H H L H		F3
L H H H L		F4
L H H H H		F5
H H H H H		NONE

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

LOGIC DIAGRAM

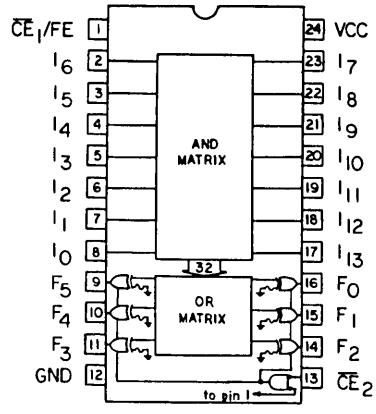


~denotes fused inputs.
*'LS333 has 3-state (▽) outputs; 'LS335 has open-collector (Ω) outputs.

TYPES FP54AS839, FP54AS840, FP74AS839, FP74AS840
14 X 32 X 6 FIELD-PROGRAMMABLE LOGIC ARRAYS

JT OR NT PACKAGE

(TOP VIEW)



* 10 NS TYPICAL INPUT TO OUTPUT PROPAGATION DELAY
* 24-PIN, 300-MIL SLIM LINE PACKAGES
* 725 MW TYPICAL POWER DISSIPATION
* PROGRAMMABLE OUTPUT POLARITY

LOGIC FUNCTION

$F = P_0+P_1+\ldots+P_{31}$ FOR POLARITY LINK INTACT

$F = \overline{P_0}*\overline{P_1}*\ldots*\overline{P_{31}}$ FOR POLARITY LINK OPEN

WHERE P_0 THRU P_{31} ARE PRODUCT TERMS OF INPUT VARIABLES I_0 THRU I_{13}

DESCRIPTION

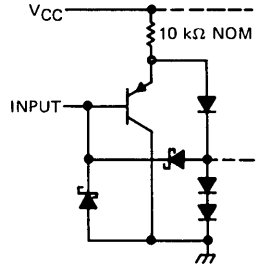
THE 'AS839 (THREE-STATE OUTPUTS) AND THE 'AS840 (OPEN-COLLECTOR OUTPUTS) ARE ADVANCED SCHOTTKY BIPOLAR TTL FIELD-PROGRAMMABLE LOGIC ARRAYS, CONTAINING 32 PRODUCT TERMS (AND TERMS), AND 6 SUM TERMS (OR TERMS). EACH OF THE 6 SUM-OF-PRODUCTS OUTPUT FUNCTIONS CAN BE PROGRAMMED EITHER TRUE ACTIVE-HIGH OR TRUE ACTIVE-LOW. THE TRUE OF EACH OUTPUT FUNCTION IS ACTIVATED BY THE PROGRAMMED LOGICAL MINTERMS OF 14 OR LESS INPUT VARIABLES. THE OUTPUTS ARE CONTROLLED BY TWO CHIP-ENABLE PINS ALLOWING OUTPUT INHIBIT AND EXPANSION OF TERMS.

THESE DEVICES ARE IDEALLY SUITED FOR HIGH-SPEED DATA PATH LOGIC REPLACEMENT, WHERE SEVERAL CONVENTIONAL SSI FUNCTIONS CAN BE DESIGNED INTO A SINGLE PACKAGE.

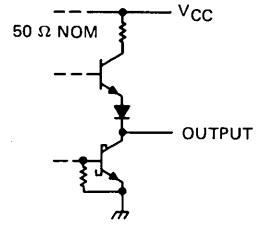
THE FP54AS839 AND FP54AS840 ARE CHARACTERIZED FOR OPERATION OVER THE FULL MILITARY TEMPERATURE RANGE OF -55°C TO 125°C. THE FP74AS839 AND FP74AS840 ARE CHARACTERIZED FOR OPERATION FROM 0°C TO 70°C.

SCHEMATICS OF INPUTS AND OUTPUTS

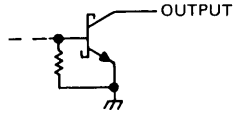
EQUIVALENT OF EACH INPUT



TYPICAL OF OUTPUTS OF 'AS839



TYPICAL OF OUTPUTS OF 'AS840



PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, V_{CC}	7V
INPUT VOLTAGE	5.5V
OFF-STATE OUTPUT VOLTAGE	5.5V
STORAGE TEMPERATURE	-65° TO 150°C

RECOMMENDED OPERATING CONDITIONS

	PARAMETER	FP54AS' MIN	FP54AS' NOM	FP54AS' MAX	FP74AS' MIN	FP74AS' NOM	FP74AS' MAX	UNIT
V_{CC}	SUPPLY VOLTAGE	4.5	5	5.5	4.75	5	5.25	V
I_{OH}	HIGH-LEVEL OUTPUT CURRENT			-1			-2.6	mA
I_{OL}	LOW-LEVEL OUTPUT CURRENT			32			48	mA
T_A	OPERATING FREE-AIR TEMPERATURE	-55		125	0		70	°C

ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)

PARAMETER		TEST CONDITION	FP54AS' MIN	FP54AS' TYP*	FP54AS' MAX	FP74AS' MIN	FP74AS' TYP*	FP74AS' MAX	UNIT
V_{IH}	HIGH-LEVEL INPUT VOLTAGE		2			2			V
V_{IL}	LOW-LEVEL INPUT VOLTAGE				0.8			0.8	V
V_{IK}	INPUT CLAMP VOLTAGE	V_{CC} = MIN, I_I = -18mA			-1.2			-1.2	V
V_{OH}	HIGH-LEVEL OUTPUT VOLTAGE	V_{CC} = MIN, V_{IL} =0.4V, I_{OH} = -2.6mA, V_{IH} =2V	2.4	3.2		2.4	3.4		V
V_{OL}	LOW-LEVEL OUTPUT VOLTAGE	V_{CC} = MIN, V_{IL} =0.8V, I_{OL} = 48mA, V_{IH} = 2V		0.25	0.5		0.37	0.5	V
I_I	INPUT CURRENT AT MAX INPUT VOLTAGE	V_{CC} = MAX, V_{IH} = 5.5V			0.1			0.1	mA
I_{IH}	HIGH-LEVEL INPUT CURRENT	V_{CC} = MAX, V_{IH} = 2.7V			20			20	uA
I_{IL}	LOW-LEVEL INPUT CURRENT	V_{CC} = MAX, V_{IL} = 0.4V			-0.4			-0.4	mA
I_O	OUTPUT CURRENT	V_O = 2.25V	-15	-33	-65	-15	-33	-65	mA
I_{OZH}	OFF-STATE OUTPUT CURRENT, HIGH-LEVEL VOLTAGE APPLIED	V_{CC} = MAX, V_{IH} = 2V, V_{IL} = 0.8V, V_O = 2.7V			20			20	uA
I_{OZL}	OFF-STATE OUTPUT CURRENT, LOW-LEVEL VOLTAGE APPLIED	V_{CC} = MAX, V_{IH} = 2V, V_{IL} = 0.8V, V_O = 0.4V			-20			-20	uA
I_{CC}	SUPPLY CURRENT	V_{CC} = 5V, V_I = 0V, $\overline{CE}$ INPUTS AT 5V		145			145		mA

*ALL TYPICAL VALUES ARE AT V_{CC} = 5 V, T_A = 25°C

5

SWITCHING CHARACTERISTICS, V_{CC} = +5V, T_A = 25°C

PARAMETER	FROM INPUT	TEST CONDITIONS	FP54AS' MIN	FP54AS' TYP	FP54AS' MAX	FP74AS' MIN	FP74AS' TYP	FP74AS' MAX	UNIT
TPLH		OUTPUT FUSE INTACT, R_L=500 OHMS TO GND, C_L=50pF TO GND		10			10		NS
TPHL				10			10		
TPLH		OUTPUT FUSE OPEN, R_L=500 OHMS TO GND, C_L=50pF TO GND		11			11		NS
TPHL				12			12		
TPZH	PIN 1 OR 13	R_{L1}=500 OHMS TO 7V, R_{L2}=500 OHMS TO GND, C_L=50pF TO GND		6			6		NS
TPZL				6			6		
TPHZ				6			6		NS
TPLZ				6			6		

PROGRAMMING PARAMETERS, T_A = 25°C

	PARAMETER		MIN	NOM	MAX	UNIT
V_{IHH}	POLARITY AND FUSE ENABLE PROGRAM-LEVEL INPUT VOLTAGE			20		V
I_{IHH}	PROGRAM-LEVEL INPUT CURRENT	POLARITY OUTPUT		100		mA
		CE1/FE		100		
V_{CCH}	POLARITY VERIFY-LEVEL SUPPLY, 'OR' PROGRAM/VERIFY-LEVEL SUPPLY			8.5		V
V_{CC}	'AND' PROGRAM/VERIFY-LEVEL V_{CC} SUPPLY VOLTAGE			5		
V_{CCL}	POLARITY PROGRAM-LEVEL V_{CC} SUPPLY VOLTAGE			0		
I_{CC}	'AND'/'OR' PROGRAM SUPPLY CURRENT		0.5		1	A
V_{IX}	INPUT DISABLE VOLTAGE, CE2 PROGRAM ENABLE LEVEL, 'OR' PROGRAM-LEVEL INPUT VOLTAGE			10		V
I_{IX}	INPUT CURRENT	INPUT VARIABLES			2	mA
		CE2			5	
		'OR' PROGRAM OUTPUT			10	
TP	PROGRAM PULSE WIDTH	CE2		400		US
TD	DELAY TIME		10			US
TR	RISE TIME			25		US
	PROGRAMMING PULSE DUTY CYCLE				50	%

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

PROGRAMMING PROCEDURE

(Load all output pins with a 10-kilohm resistor to 5V, set GND (pin 12) to 0V)

PROGRAM OUTPUT POLARITY

Program the output polarity before programming either the AND matrix or the OR matrix. A virgin device has all of its 6 outputs set to active high. When the polarity link of an output is fused, that output function becomes active low. Note that all outputs of a virgin device are at a low logic level. Program one output at a time as follows:

Step 1: Set $\overline{CE}_1$/FE (pin 1) to 0V.
Step 2: Set V_{CC} (pin 24) to 0V, set $\overline{CE}_2$ (pin 13) and I_0 to I_{13} to V_{IH}.
Step 3: Pulse the appropriate output to V_{IHH} and remove after tp.
Step 4: Repeat step 4 for each output to be programmed active low.

VERIFY OUTPUT POLARITY

Step 1: Set $\overline{CE}_1$/FE (pin 1) to 0V; set V_{CC} (pin 24) to V_{CCH}.
Step 2: Enable the device by applying V_{IL} to $\overline{CE}_2$, (pin 13).
Step 3: Set all inputs I_0 thru I_{13} to V_{IH}.
Step 4: Sense the logic state of all 6 outputs. An output at V_{OH} has been programmed active low, while an output at V_{OL} has remained active high.
Step 5: Remove V_{CC}.

PROGRAM 'AND' MATRIX

Program each input separately for each product term, one fuse at a time. Unused terms do not require fusing, however, all input variables of a selected product term must be programmed either true, complement, or don't care (both links are blown), as follows:

Step 1: Set $\overline{CE}_1$/FE (pin 1) to 0V; set V_{CC} (pin 24) to 5V.
Step 2: Disable all outputs by applying V_{IH} to $\overline{CE}_2$ (pin 13).
Step 3: Disable all inputs by applying V_{IX} to inputs I_0 thru I_{13}.
Step 4: Address the product term to be programmed (0 thru 31) by applying its binary code (V_{IH} for '1', V_{IL} for '0') to outputs F_0 thru F_4 with F_0 as the least significant bit.
Step 5: Lower the voltage on the first input to V_{IH} for a true, or to V_{IL} for the complement.
Step 6: After td, raise $\overline{CE}_1$/FE to V_{IHH}.
Step 7: After additional td, pulse the $\overline{CE}_2$ input to V_{IX} for t_p.
Step 8: After a td delay, lower $\overline{CE}_1$/FE to 0V.
Step 9: Disable programmed input by raising it back to V_{IX}.
Step 10: Repeat steps 5-9 for each input.
Step 11: Repeat steps 4-10 for each product term.

VERIFY 'AND' MATRIX

Step 1: Set $\overline{CE}_1$/FE (pin 1) to 0V; set V_{CC} (pin 24) to 5V.
Step 2: Enable F_5 output by setting $\overline{CE}_2$ to V_{IX}.
Step 3: Disable all inputs by applying V_{IX} to inputs I_0 thru I_{13}.
Step 4: Address the product term to be verified (0-31) by applying its corresponding binary code on outputs F_0 thru F_4.
Step 5: Lower the input voltage on the first input to V_{IH} and check the logic level of output F_5, then lower the same input to V_{IL} and again check the level of

5

PROGRAMMING PROCEDURE (CONT.)

F_5. The input variable state contained in the product term is determined from the following table: (Note that two tests are required to verify the programmed state of each variable).

I	F5	STATE
L	L	TRUE
H	H	
L	H	COMPLEMENT
H	L	
L	H	DON'T CARE
H	H	
L	L	INACTIVE
H	L	

Step 6: Disable verified input by raising it back to V_{IX}.
Step 7: Repeat steps 5-6 for all other inputs.
Step 8: Repeat steps 4-7 for all other product terms.

PROGRAM 'OR' MATRIX

If the product term is contained in the output function, no fusing is needed. Unwanted terms are deleted by programming one at a time, as follows:

Step 1: Set $\overline{CE}_1$/FE (pin 1) to 0V.
Step 2: Disable the outputs by setting $\overline{CE}_2$ (pin 13) to V_{IH}.
Step 3: Wait td and raise V_{CC} (pin 24) to the program level, V_{CCH}.
Step 4: Use the inputs I_0 thru I_5 to address the product term (0-31) that is to be removed by applying the corresponding binary code with input I_0 as the LSB.
Step 5: Raise the output pin to V_{IX}.
Step 6: Wait td, then raise $\overline{CE}_1$/FE to V_{IHH}.
Step 7: Wait td, then pulse $\overline{CE}_2$ to V_{IX} for a period of t_p.
Step 8: Wait td, then lower $\overline{CE}_1$/FE to 0V
Step 9: Wait td, then remove V_{IX} from output pin.
Step 10: Repeat steps 5-9 for all other output functions.
Step 11: Repeat steps 4-10 for all other product terms.
Step 12: Lower V_{CC} to 5V.

VERIFY 'OR' MATRIX

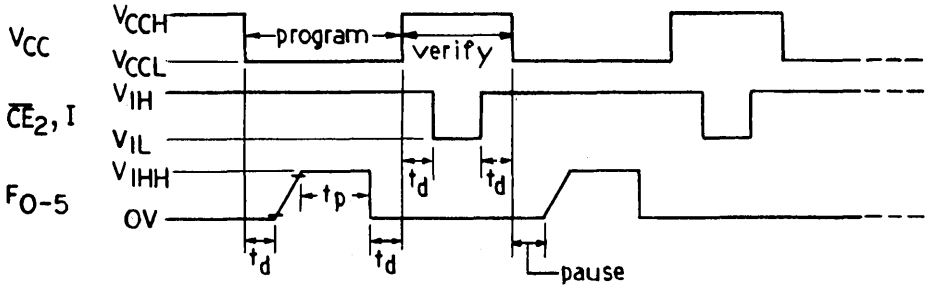
Step 1: Set $\overline{CE}_1$/FE (pin 1) to 0V.
Step 2: Disable the outputs by setting $\overline{CE}_2$ to V_{IH}.
Step 3: Wait td and set V_{CC} (pin 24) to the verify level, V_{CCH}.
Step 4: Address the product term to be verified (0-31) by applying its binary code to inputs I_0 thru I_5.
Step 5: Wait td, and set $\overline{CE}_2$ (pin 13) to V_{IL}.
Step 6: Sense the state of all 6 outputs F_0 thru F_5 to determine the status of the 'OR' matrix from the following table:

OUTPUT		
ACTIVE HIGH	ACTIVE LOW	'OR' FUSE LINK
L	H	FUSED
H	L	PRESENT

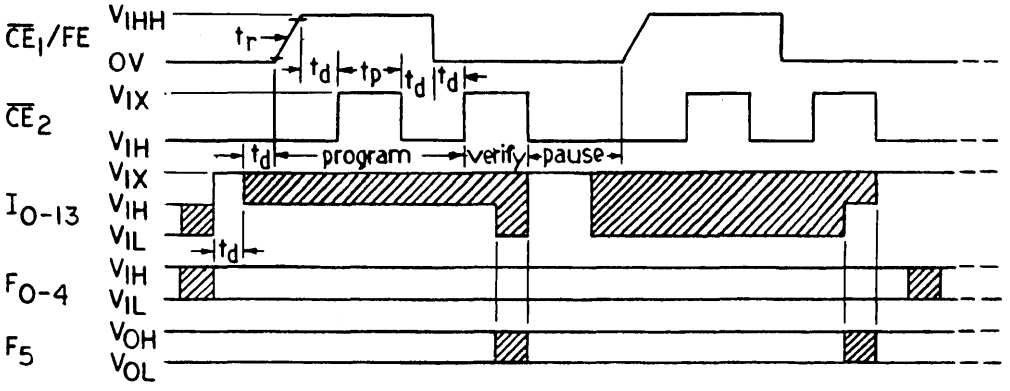
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

PROGRAMMING WAVEFORMS

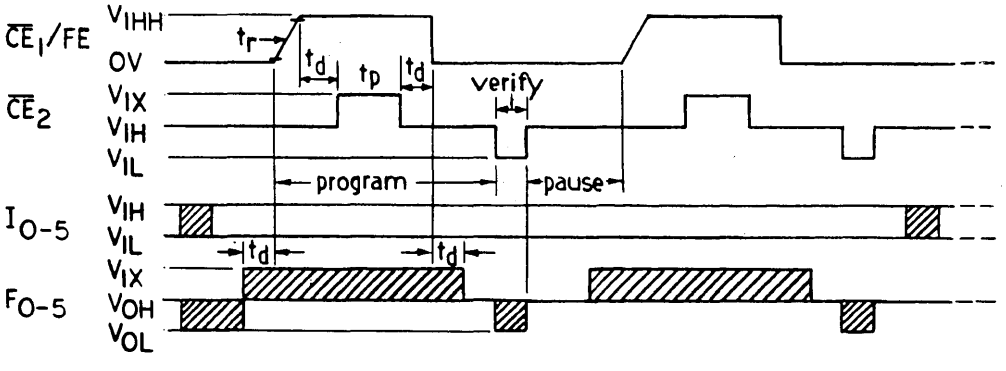
OUTPUT POLARITY



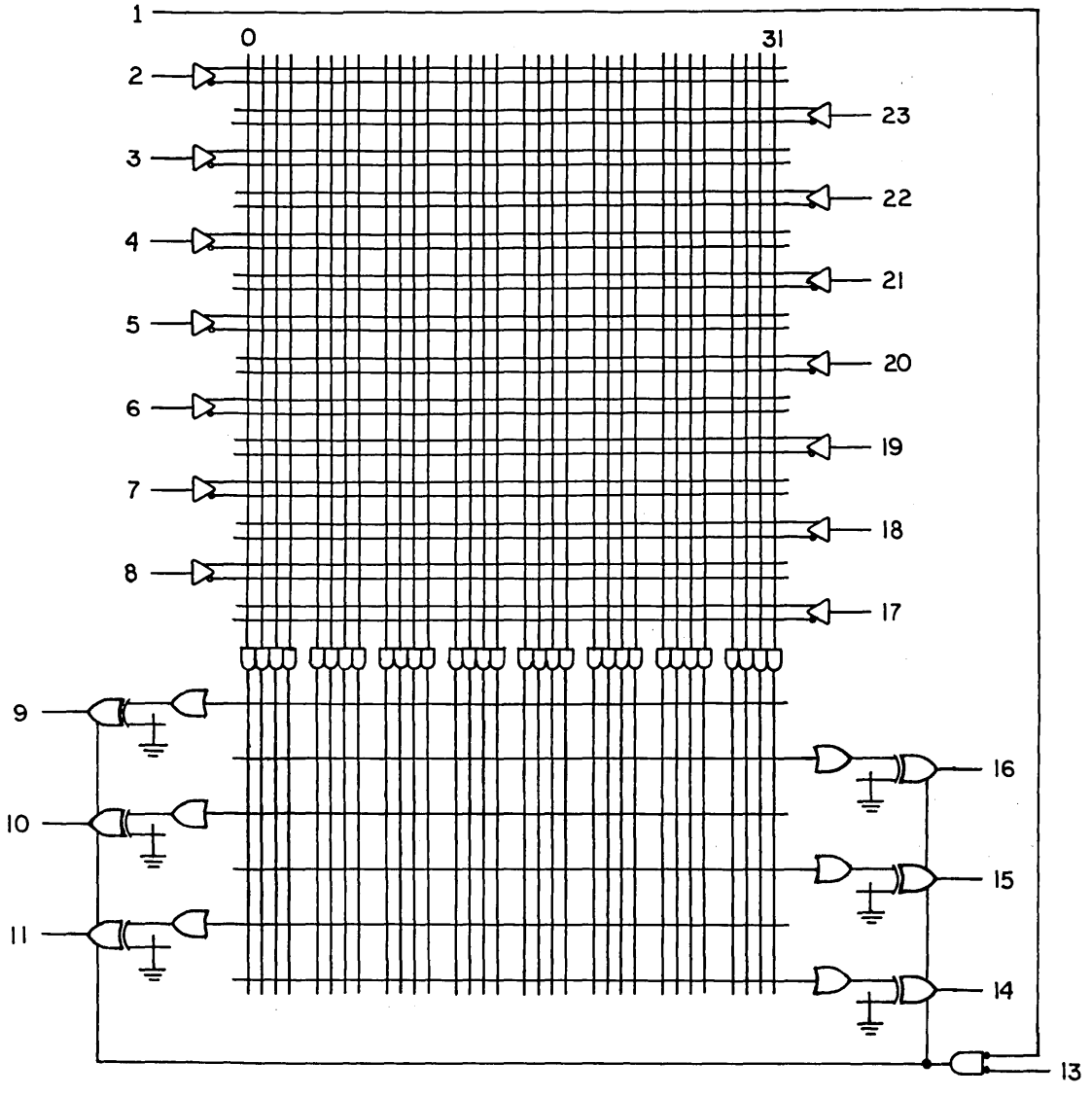
AND MATRIX



OR MATRIX



LOGIC DIAGRAM



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

Functional Index Selection Guide for Bipolar Digital Products

FUNCTIONAL INDEX/SELECTION GUIDE

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

GATES AND EXPANDERS

POSITIVE-NAND GATES AND INVERTERS

DESCRIPTION	TYPE	TECHNOLOGY							PAGE NO.†
		STD TTL	ALS	AS	H	L	LS	S	
Hex 2-Input Gates	'804		▲	•					S-275
Hex Inverters	'04	•	•		•	•	•	•	T5-7 S-232
	'1004		▲						
Quadruple 2-Input Gates	'00	•	•		•	•	•	•	T5-6 S-228
	'1000		•						S-264
Triple 3-Input Gates	'10	•	•		•	•	•	•	T5-8
	'1010		•						S-236
Dual 4-Input Gates	'20	•	•		•	•	•	•	T5-10 S-240
	'1020		•						S-266
8-Input Gates	'30	•	•		•	•	•	•	T5-12 S-245
13-Input Gates	'133		•					•	T5-38 S-255

POSITIVE-NAND GATES AND INVERTERS WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY							PAGE NO.†
		STD TTL	ALS	AL	H	L	LS	S	
Hex Inverters	'05	•	•		•		•	•	T5-7 S-233
	'1005		▲						
Quadruple 2-Input Gates	'01	•	•		•	•	•		T5-6 S-229
	'03	•	•			•	•	•	T5-7 S-231
Triple 3-Input Gates	'1003		•						S-266
	'12	•	•				•		T5-9 S-238
Dual 4-Input Gates	'22	•	•		•		•	•	T5-11 S-242

POSITIVE-AND GATES

DESCRIPTION	TYPE	TECHNOLOGY							PAGE NO.†
		STD TTL	ALS	AS	H	L	LS	S	
Hex 2-Input Gates	'808		▲	•					S-277
Quadruple 2-Input Gates	'08	•	•				•	•	T5-8 S-234
	'1008		•						
Triple 3-Input Gates	'11		•		•		•	•	T5-11 S-237
	'1011		•						
Dual 4-Input Gates	'21		•		•		•		T5-11 S-241
Triple 4-Input AND/NAND	'800			▲					S-273

POSITIVE-AND GATES WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY							PAGE NO.†
		STD TTL	ALS	AS	H	L	LS	S	
Quadruple 2-Input Gates	'09	•	•				•	•	T5-8
Triple 3-Input Gates	'15		•		•		•	•	T5-10 S-239

POSITIVE-OR GATES

DESCRIPTION	TYPE	TECHNOLOGY					PAGE NO.†
		STD TTL	ALS	AS	LS	S	
Hex 2-Input Gates	'832		▲	•			S-278
Quadruple 2-Input Gates	'32	•	•		•	•	T5-13 S-246
	'1032		•				
Triple 4-Input OR/NOR	'802			▲			S-274

POSITIVE-NOR GATES

DESCRIPTION	TYPE	TECHNOLOGY							PAGE NO.†
		STD TTL	ALS	AS	H	L	LS	S	
Hex 2-Input Gates	'805		▲	•					S-276
Quadruple 2-Input Gates	'02	•	•			•	•	•	T5-6 S-230
	'1002		•						S-265
Triple 3-Input Gates	'27	•	•				•		T5-12 S-243
Dual 4-Input Gates With Strobe	'25	•							T5-11
Dual 5-Input Gates	'260							•	T5-57

SCHMITT-TRIGGER POSITIVE-NAND GATES AND INVERTERS

DESCRIPTION	TYPE	TECHNOLOGY					PAGE NO.†
		STD TTL	ALS	AS	LS	S	
Hex Inverters	'14	•			•		T5-9
	'19				•		S-17
Dual 4-Input Positive-NAND	'13	•			•		T5-9
	'18				•		S-17
Quadruple 2-Input Positive-NAND	'24				•		S-17
	'132	•			•	•	T-537

AND-OR-INVERT GATES

DESCRIPTION	TYPE	TECHNOLOGY							PAGE NO.†
		STD TTL	ALS	AS	H	L	LS	S	
2-Wide 4-Input	'55				•	•	•		T5-19
4-Wide 4-2-3-2-Input	'64							•	T5-20
4-Wide 2-2-3-2-Input	'54				•				T5-18
4-Wide 2-Input	'54	•							T5-18
4-Wide 2-3-3-2-Input	'54						•		T5-18
4-Wide 2-3-3-2-Input	'54					•			T5-18
Dual 2-Wide 2-Input	'51	•			•	•	•	•	T5-16

AND-OR-INVERT GATES WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY				PAGE NO.†
		ALS	AS	LS	S	
4-Wide 4-2-3-2-Input	'65				•	T5-20

EXPANDABLE GATES

DESCRIPTION	TYPE	TECHNOLOGY							PAGE NO.†
		STD TTL	ALS	AS	H	L	LS	S	
Dual 4-Input Positive-NOR With Strobe	'23	•							T5-11
4-Wide AND-OR	'52				•				T5-17
4-Wide AND-OR-Invert	'53	•			•				T5-17
2-Wide AND-OR-Invert	'55				•	•	•		T5-19
Dual 2-Wide AND-OR-Invert	'50	•			•				T5-16

EXPANDERS

DESCRIPTION	TYPE	TECHNOLOGY					PAGE NO.†
		STD TTL	ALS	AS	H	LS	
Dual 4-Input	'60	•			•		T5-19
Triple 3-Input	'61				•		T5-19
3-2-2-3-Input AND-OR	'62				•		T5-20

CURRENT-SENSING-GATES

DESCRIPTION	TYPE	TECHNOLOGY			PAGE NO.†
		ALS	AS	LS	
Hex	'63			•	T5-20

† Page numbers with "T" preceding them refer to pages in *The TTL Data Book for Design Engineers*, second edition. Those with "S" preceding them refer to the *1981 Supplement to the TTL Data Book for Design Engineers*, second edition. Those with no letter prefix refer to pages in this book.

• Denotes available technology.

▲ Denotes planned new products.

BUFFERS, DRIVERS, BUS TRANSCEIVERS, AND INTERFACE GATES

BUFFERS, CLOCK/MEMORY DRIVERS

DESCRIPTION	TYPE	TECHNOLOGY						PAGE NO.†
		STD TTL	ALS	AS	H	LS	S	
Quad 2-Input Positive-NOR	'28	•	•			•		T5-37
Quad 2-Input Positive-NAND	'37	•	•			•	•	T5-13 S-248
Dual 4-Input Positive-NAND	'40	•	•		•	•	•	T5-14 S-248
Line Driver/Memory Driver (Has Series Damping Resistor)	'436						•	S-77
Line Driver/Memory Driver	'437						•	S-77
Quad 2-Input Positive-NAND	'1000		•					S-264
Hex Inverter	'1004			▲				
Quad 2-Input Positive-NOR	'1002		•					S-265
Quad 2-Input Positive-AND	'1008		•					
Triple 3-Input Positive-NAND	'1010		•					S-266
Triple 3-Input Positive-AND	'1011		•					
Dual 4-Input Positive-NAND	'1020		•					S-266
Quad 2-Input Positive-OR	'1032		•					
Triple 4-Input AND/NAND	'800			▲				S-273
Triple 4-Input OR/NOR	'802			▲				S-274
Hex 2-Input Positive-NAND	'804		▲	•				S-275
Hex 2-Input Positive-NOR	'805		▲	•				S-276
Hex 2-Input Positive-AND	'808		▲	•				S-277
Hex 2-Input Positive-OR	'832		▲	•				S-278

50-OHM/75-OHM LINE DRIVERS

DESCRIPTION	TYPE	TECHNOLOGY					PAGE NO.†
		STD TTL	ALS	AS	LS	S	
Dual 4-Input Positive-NAND	'140					•	T5-39
Quad 2-Input Positive-NOR	'128	•					T5-37
Hex 2-Input Positive-NAND	'804		▲	•			S-275
Hex 2-Input Positive-NOR	'805		▲	•			S-276
Hex 2-Input Positive-AND	'808		▲	•			S-277
Hex 2-Input Positive-OR	'832		▲	•			S-278

OCTAL BI-DIRECTIONAL BUS TRANSCEIVERS

DESCRIPTION		TYPE OF OUTPUT	TYPE	TECHNOLOGY			PAGE NO.†
				ALS	AS	LS	
12 mA/24 mA Sink	Low Power	3-State	'245	▲		•	T7-349
		3-State	'620	▲		•	S-141
		OC	'621	▲		•	S-141
		OC	'622	▲		•	S-141
		3-State	'623	▲		•	S-141
	Very Low Power	3-State	1620	▲			
		OC	'1621	▲			
		OC	'1622	▲			
		3-State	'1623	▲			
12 mA/24 mA/ 48 mA Sink	Low Power	3-State	'640	▲		•	S-161
		OC	'641	▲		•	S-161
		OC	'642	▲		•	S-161
		3-State	'643	▲		•	S-161
		OC	'644	▲		•	S-161
		3-State	'645	▲		•	S-161
	Very Low Power	3-State	'1640	▲			
		OC	'1641	▲			
		OC	'1642	▲			
		3-State	'1643	▲			
		OC	'1644	▲			
		3-State	'1645	▲			
Registered With Multiplexed 12/24 mA Outputs		3-State	'646			•	S-168
		OC	'647			•	S-168
		3-State	'648			•	S-168
		OC	'649			•	S-168
Inverting 12/24 mA Sink	Low Power	OC	'638	▲		•	S-157
		3-State	'639	▲		•	S-157
		3-State	'651			•	S-175
	Very Low Power	OC	'1638	▲			
		3-State	'1639	▲			
Non-Inverting Octal Bus Transceivers		3-State	'652			•	S-175
Octal I/O Storing Transceivers		3-State	'877		▲		

BUFFER AND INTERFACE GATES WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY					PAGE NO.†
		STD TTL	ALS	AS	LS	S	
Hex	'07	•					T5-8
	'17	•					T5-10
Hex Inverter	'06	•					T5-7
	'16	•					T5-10
	'1005		▲				
Quad 2-Input Positive-NAND	'26	•			•		T5-12
	'38	•	•		•	•	T5-13 S-249
	'1003		•				S-266
Quad 2-Input Positive-NOR	'33	•	•		•		T5-13 S-247

GATES, BUFFERS, DRIVERS, AND BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY					PAGE NO.†
		STD TTL	ALS	AS	LS	S	
12-Input NAND Gate	'134					•	T5-38
Quadruple Bus Buffers/ Drivers With Independent Output Controls	'125	•			A		T5-37
	'126	•			A		T5-37
	'425	•					T5-71
	'426	•					T5-72
Hex Buffers/Drivers	'365	A			A		T5-66
	'366	A			A		T5-66
	'367	A			A		T5-66
	'368	A			A		T5-66
Octal Bus Buffers/Drivers	'240		▲	▲	•	•	T5-53
	'241		▲	▲	•	•	T5-54
	'244		▲	▲	•		T5-54
	'340					•	T7-445
	'341					•	T7-445
	'344					•	T7-445
	'540		▲		•		S-98
	'541		▲		•		S-98
	'1240¶		▲				
	'1241¶		▲				
	'1244¶		▲				
Controller and Bus Driver for 8080A System	'428					•	T7-514
	'438					•	T7-514
Quadruple Transceivers Inverting 3-State Output	'242		▲	▲	•		T5-54
	'1242¶		▲				
Quadruple Transceivers Non-Inverting 3-State Output	'243		▲	▲	•		T5-54
	'1243¶		▲				
Quadruple Transceivers With Storage	'226					•	T7-345
Octal Transceivers	'245		▲		•		T7-349
Octal Buffer 3-State	'465		▲		•		S-95
	'467		▲		•		S-95
Inv. Octal Buffer 3-State	'466		▲		•		S-95
	'468		▲		•		S-95

BI-TRI-DIRECTIONAL BUS TRANSCEIVERS AND DRIVERS

DESCRIPTION	TYPE OF OUTPUT	TYPE	TECHNOLOGY				PAGE NO.†
			ALS	AS	LS	S	
Controller and Bus Driver For 8080A Systems		'428				•	T7-514
		'438				•	T7-514
4-Bit With Storage	3-State	'226				•	T7-345
Quad With Bit-Direction Controls	3-State	'446			•		S-89
	3-State	'449			•		S-89
Quad Tridirection	OC	'440			•		S-81
	OC	'441			•		S-81
	3-State	'442			•		S-81
	3-State	'443			•		S-81
	3-State	'444			•		S-81
	OC	'448			•		S-81

† Page numbers with "T" preceding them refer to pages in *The TTL Data Book for Design Engineers*, second edition. Those with "S" preceding them refer to the *1981 Supplement to the TTL Data Book for Design Engineers*, second edition. Those with no letter prefix refer to pages in this book.

• Denotes available technology.

A Denotes "A" suffix version available in the technology indicated.

▲ Denotes planned new products.

¶ Denotes very low power.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

FLIP-FLOPS, LATCHES, MULTIVIBRATORS, CLOCK GENERATORS AND OSCILLATORS

DUAL AND SINGLE FLIP-FLOPS

DESCRIPTION	TYPE	TECHNOLOGY							PAGE NO.†
		STD TTL	ALS	AS	H	L	LS	S	
Dual J-K Edge-Triggered	'73						A		T5-22
	'76						A		T5-23
	'78						A		T5-24
	'103				•				T5-31
	'106				•				T5-32
	'107						A		T5-32
	'108				•				T5-32
	'109	•	•	▲			A		T5-33 S-251
	'112		•	▲			A	•	T5-34 S-252
	'113		•	▲			A	•	T5-34 S-253
	'114		•	▲			A	•	T5-34 S-254
Single J-K Edge-Triggered	'70	•							T5-21
	'101				•				T5-31
	'102				•				T5-31
Dual Pulse-Triggered	'73	•			•	•			T5-22
	'76	•			•				T5-23
	'78				•	•			T5-24
	'107	•							T5-32
Single Pulse-Triggered	'71				•	•			T5-21
	'72	•			•	•			T5-22
Dual J-K With Data Lockout	'111	•							T5-33
Single J-K With Data Lockout	'110	•							T5-33
Dual D-Type	'74	•	•	▲	•	•	A	•	T5-22 S-250

QUAD AND HEX FLIP-FLOPS

DESCRIPTION	NO. FFs	OUTPUTS	TYPE	TECHNOLOGY					PAGE NO.†
				STD TTL	ALS	AS	LS	S	
D Type With Enable	6	Q	'378				•		T7-481
	4	Q, $\overline{Q}$	'379				•		T7-481
D Type With Clear	6	Q	'174	•	▲	▲	•	•	T7-253
	4	Q, $\overline{Q}$	'175	•	▲	▲	•	•	T7-253
J-K, Separate Clocks	4	Q	'276	•					T7-401
J-K, Common Clock	4	Q	'376	•					T7-479

OCTAL D-TYPE FLIP-FLOPS

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY					PAGE NO.†
			STD TTL	ALS	AS	LS	S	
True Data	3-State	'374		▲	▲	•	•	T7-471
	3-State	'574		•	▲			S-257
True Data With Clear	2-State	'273	•	▲		•		T7-388
	3-State	'874		•	▲			S-261
True Data With Enable	2-State	'377				•		T7-481
Inverting	3-State	'576		•	▲			S-258
Inverting With Preset	3-State	'876		•	▲			S-262

LATCHES

DESCRIPTION	NO. OF BITS	TYPE	TECHNOLOGY					PAGE NO.
			STD TTL	ALS	AS	L	LS	S	
Multi-Mode Buffered	8	'412						•	T7-502
Addressable	8	'259	•	▲			•		T7-376
Transparent	8	'373		▲	▲		•	•	T7-471
Dual 4-Bit With Independent Enable	8	'100	•						T7-113
		'116	•						T7-115
Dual 2-Bit With Independent Enable	4	'75	•			•	•		T7-35
		'77	•			•	•		T7-35
		'375					•		T7-478
Quad $\overline{S}$-$\overline{R}$	4	'279	•				•		T5-59

$\overline{S}$-$\overline{R}$ LATCHES

DESCRIPTION	TYPE	TECHNOLOGY				PAGE NO.†
		STD TTL	ALS	AS	LS	
Quadruple	'279	•			•	T5-59

OCTAL LATCHES

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY					PAGE NO.†
			STD TTL	ALS	AS	LS	S	
Transparent	3-State	'373		▲	▲	•	•	T7-441
	3-State	'573		•	▲			S-256
	3-State	'873		•	▲			S-283
Inverting Transparent	3-State	'580		•	▲			S-259
	3-State	'880		•	▲			S-263
2-Input Multiplexed	3-State	'604				•		S-124
	OC	'605				•		S-124
	3-State	'606				•		S-124
	OC	'607				•		S-124

MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

DESCRIPTION	TYPE	TECHNOLOGY					PAGE NO.†
		STD TTL	ALS	AS	L	LS	
Single	'121	•			•		T5-35
Dual	'221	•				•	T5-53

RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

DESCRIPTION	TYPE	TECHNOLOGY					PAGE NO.†
		STD TTL	ALS	AS	L	LS	
Single	'122	•			•	•	T5-36
	'422					•	S-73
Dual	'123	•			•	•	T5-36
	'423					•	S-73

CLOCK GENERATOR CIRCUITS

DESCRIPTION	TYPE	TECHNOLOGY					PAGE NO.†
		STD TTL	ALS	AS	LS	S	
Quadruple Complementary-Output Logic Elements	'265	•					T5-57
Dual Pulse Synchronizers/Drivers	'120	•					T7-118
Crystal-Controlled Oscillators	'320				•		S-44
	'321				•		S-44
Digital Phase-Lock Loop	'297				•		S-38
Programmable Frequency Dividers/Digital Timers	'292				•		S-31
	'294				•		S-31
Triple 4-Input AND/NAND Drivers	'800			▲			S-273
Triple 4-Input OR/NOR Drivers	'802			▲			S-274

VOLTAGE-CONTROLLED OSCILLATORS

DESCRIPTION						TYPE	TECHNOLOGY					PAGE NO.†
NUMBER VCO'S	COMP'L Z_{OUT}	ENABLE	RANGE INPUT	R_{EXT}	f_{max} MHz		STD TTL	ALS	AS	LS	S	
Single	Yes	Yes	Yes	No	20	'624				•		S-145
Single	Yes	Yes	Yes	Yes	20	'628				•		S-145
Dual	No	Yes	Yes	No	60	'124					•	T7-123
Dual	Yes	No	No	No	20	'625				•		S-145
Dual	Yes	Yes	No	No	20	'626				•		S-145
Dual	No	No	No	No	20	'627				•		S-145
Dual	No	Yes	Yes	No	20	'629				•		S-145

† Page numbers with "T" preceding them refer to pages in *The TTL Data Book for Design Engineers*, second edition. Those with "S" preceding them refer to the *1981 Supplement to the TTL Data Book for Design Engineers*, second edition. Those with no letter prefix refer to pages in this book.

• Denotes available technology.

A Denotes "A" suffix version available in the technology indicated.

▲ Denotes planned new products.

REGISTERS AND COUNTERS

REGISTER FILES

DESCRIPTION	TYPE	TECHNOLOGY				PAGE NO.†
		STD TTL	ALS	AS	LS	
Eight Words of Two Bits	'172	•				T7-245
Four Words of Four Bits	'170	•			•	T7-237
Four Words of Four Bits (3-State Outputs)	'670				•	T7-526
Dual 16-Word X 4-Bit Register Files With 3-State Output	'870			▲		S-281
	'871			▲		S-281

SHIFT REGISTERS

DESCRIPTION	NO. OF BITS	MODES				TYPE	TECHNOLOGY						PAGE NO.†
		SR‡	SL‡	LOAD	HOLD		STD TTL	ALS	AS	L	LS	S	
8-Bit Sign Protected Register	8	X		X	X	'322					A		S-47
Parallel-In, Parallel-Out (Bidirectional)	8	X	X	X	X	'198	•						T7-338
		X	X	X	X	'299		▲			•	•	T7-437
		X	X	X	X	'323		▲			•		T7-443
	4	X	X	X	X	'194	•				A	•	T7-316
Parallel-In Parallel-Out, Registered Outputs	4	X	X	X	X	'671					•		S-187
		X	X	X	X	'672					•		S-187
Parallel-In, Parallel-Out	8	X		X	X	'199	•						T7-338
	5	X		X		'96	•			•	•		T7-95
	4	X		X		'95	A			•	B		T7-89
		X		X		'99				•			T7-109
		X		X	X	'178	•						T7-265
		X		X	X	'179	•						T7-265
		X		X		'195	•				A	•	T7-324
		X		X		'295					B		T7-429
		X		X		'395					A		T7-496
Serial-In, Parallel-Out	16	X		X	X	'673					•		S-193
	8	X				'164	•			•	•		T7-206
Parallel-In, Serial-Out	16	X		X	X	'674					•		S-193
	8	X		X	X	'165	•				A		T7-212
		X		X	X	'166	•				A		T7-217
Serial-In, Serial-Out	8	X				'91	A			•	•		T7-81
	4	X		X		'94	•						T7-86

SHIFT REGISTERS WITH LATCHES

DESCRIPTION	NO. OF BITS	TYPE OF OUTPUT	TYPE	TECHNOLOGY			PAGE NO.†
				ALS	AS	LS	
Serial-In, Parallel-Out Shift Registers With Storage	8	3-State	'595			•	S-110
		OC	'596			•	S-110
	16	2-State	'673			•	S-193
Parallel-In, Serial-Out Shift Register With Storage	8	2-State	'597			•	S-114
	16	3-State	'674			•	S-193
I/O Ports Provide Parallel Shift Register Outputs & Multiplexed Serial Data Inputs	8	3-State	'598			•	S-114

OTHER REGISTERS

DESCRIPTION	TYPE	TECHNOLOGY						PAGE NO.†
		STD TTL	ALS	AS	L	LS	S	
Quadruple Multiplexers With Storage	'98				•			T7-107
	'298	•				•		T7-432
	'398					•		T7-499
	'399					•		T7-499
8-Bit Universal Shift Registers	'299		▲			•	•	T7-437
Quadruple Bus-Buffer Registers	'173	•				A		T7-249
Octal Storage Register	'396					•		S-71

ACCUMULATOR REGISTERS/SCALERS

DESCRIPTION	NO. OF BITS	MODES				TYPE	TECHNOLOGY			PAGE NO.†
		SR‡	SL‡	LOAD	HOLD		ALS	AS	LS	
Sign-Protected Register	8	X		X	X	'322			A	S-47
Expandable Multifunction Binary/Hexadecimal Scaler	4	X	X	X	X	'894		▲		S-294

SYNCHRONOUS COUNTERS – POSITIVE-EDGE TRIGGERED

DESCRIPTION	PARALLEL LOAD	TYPE	TECHNOLOGY						PAGE NO.†
			STD TTL	ALS	AS	L	LS	S	
Decade	Sync	'160	•	▲	▲		A		T7-190
	Sync	'162	•	▲	▲		A	•	T7-190
	Sync	'668					•		S-179
	Sync	'690					•		S-211
	Sync	'692					•		S-211
	Sync	'560		▲					
Decade Up/Down	Sync	'168		▲	▲			•	T7-226
	Async	'190	•	▲			•		T7-296
	Async	'192	•	▲		•	•		T7-306
	Sync	'696					•		S-217
	Sync	'698					•		S-217
	Sync	'568		▲					
Decade Rate $\frac{1}{N10}$ Multiplier,	Async Set-To-9	'167	•						T7-222
4-Bit Binary	Sync	'161	•	▲	▲		A		T7-190
	Sync	'163	•	▲	▲		A	•	T7-190
	Sync	'561		▲					
	Sync	'669					•		S-179
	Sync	'691					•		S-211
	Sync	'693					•		S-211
4-Bit Binary Up/Down	Sync	'169		▲	▲		A	•	T7-226
	Async	'191	•	▲			•		T7-296
	Async	'193	•	▲		•	•		T7-306
	Sync	'569		▲					
	Sync	'697					•		S-217
	Sync	'699					•		S-217
6-Bit Binary Rate $\frac{1}{N2}$ Multiplier,		'97	•						T7-102
8-Bit UP/Down	Sync	'867			▲				S-280
	Sync	'869			▲				S-280

ASYNCHRONOUS COUNTERS (RIPPLE CLOCK) – NEGATIVE-EDGE TRIGGERED

DESCRIPTION	PARALLEL LOAD	TYPE	TECHNOLOGY						PAGE NO.†
			STD TTL	ALS	AS	L	LS	S	
Decade	Set-To-9	'90	A			•	•		T7-72
	Yes	'176	•						T7-259
	Yes	'196	•				•	•	T7-331
	Set-To-9	'290	•				•		T7-423
4-Bit Binary	None	'93	A			•	•		T7-72
	Yes	'177	•						T7-259
	Yes	'197	•				•	•	T7-331
	None	'293	•				•		T7-423
Divide-By-12	None	'92	A				•		T7-72
Dual Decade	None	'390	•				•		T7-489
	Set-To-9	'490	•				•		T7-520
Dual 4-Bit Binary	None	'393	•				•		T7-489

8-BIT BINARY COUNTERS WITH REGISTERS

DESCRIPTION	TYPE OF OUTPUT	TYPE	TECHNOLOGY			PAGE NO.†
			ALS	AS	LS	
Parallel Register Outputs	3-State	'590			•	S-101
	OC	'591			•	S-101
Parallel Register Inputs	2-State	'592			•	S-105
Parallel I/O	3-State	'593			•	S-105

† Page numbers with "T" preceding them refer to pages in *The TTL Data Book for Design Engineers*, second edition. Those with "S" preceding them refer to the *1981 Supplement to the TTL Data Book for Design Engineers*, second edition. Those with no letter prefix refer to pages in this book.

‡ SR = shift right, S-L = shift left.

• Denotes available technology.

A Denotes "A" suffix version available in the technology indicated.

B Denotes "B" suffix version available in the technology indicated.

▲ Denotes planned new products.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

DECODERS, ENCODERS, CODE CONVERTERS, AND DATA SELECTORS/MULTIPLEXERS

DECODERS/DEMULTIPLEXERS

DESCRIPTION	TYPE OF OUTPUT	TYPE	TECHNOLOGY						PAGE NO.†
			STD TTL	ALS	AS	L	LS	S	
4-To-16	2-State	'154	•			•			T7-171
	OC	'159	•						T7-188
4-To-10 BCD-To-Decimal	2-State	'42	A			•	•		T7-15
4-To-10 Excess-3-To-Decimal	2-State	'43	A			•			T7-15
4-To-10 Excess-3-Gray-To-Decimal	2-State	'44	A			•			T7-15
3-To-8 With Address Latches	2-State	'137		▲			•		S-19
3-To-8	2-State	'138		▲			•	•	T7-134
	3-State	'538		▲					
Dual 2-To-4	2-State	'139		▲			•	•	T7-134
	2-State	'155	•				•		T7-175
	OC	'156	•				•		T7-175
Dual 1-To-4 Decoders	3-State	'539		▲					

OPEN-COLLECTOR DISPLAY DECODERS/DRIVERS

DESCRIPTION	OFF-STATE OUTPUT VOLTAGE	TYPE	TECHNOLOGY					PAGE NO.†
			STD TTL	ALS	AS	L	LS	
BCD-To-Decimal	30 V	'45	•					T7-20
	60 V	'141	•					T7-138
	15 V	'145	•				•	T7-148
	7 V	'445					•	S-87
BCD-To-Seven-Segment	30 V	'46	A			•		T7-22
	15 V	'47	A			•	•	T7-22
	5.5 V	'48	•				•	T7-22
	5.5 V	'49	•				•	T7-22
	30 V	'246	•					T7-351
	15 V	'247	•				•	T7-351
	7 V	'347					•	S-51
	7 V	'447					•	S-93
	5.5 V	'248	•				•	T7-351
	5.5 V	'249	•				•	T7-351

OPEN-COLLECTOR DISPLAY DECODERS/DRIVERS WITH COUNTERS/LATCHES

DESCRIPTION	TYPE	TECHNOLOGY			PAGE NO.†
		STD TTL	ALS	AS	
BCD Counter/4-Bit Latch/BCD-To-Decimal Decoder/Driver	'142	•			T7-140
BCD Counter/4-Bit Latch/BCD-To-Seven-Segment Decoder/Led Driver	'143	•			T7-143
BCD Counter/4-Bit Latch/BCD-To-Seven-Segment Decoder/Lamp Driver	'144	•			T7-143

DATA SELECTORS/MULTIPLEXERS

DESCRIPTION	TYPE OF OUTPUT	TYPE	TECHNOLOGY						PAGE NO.†
			STD TTL	ALS	AS	L	LS	S	
16-To-1	2-State	'150	•						T7-157
Dual 8-To-1	3-State	'351	•						T7-451
8-To-1	2-State	'151	A	▲	▲		•	•	T7-157
	2-State	'152	A	▲			•		T7-157
	3-State	'251	•	▲	▲		•	•	T7-362
	3-State	'354					•		S-53
	2-State	'355					•		S-53
	3-State	'356					•		S-53
	2-State	'357					•		S-53
Dual 4-To-1	2-State	'153	•	▲	▲	•	•	•	T7-165
	3-State	'253		▲	▲		•		T7-369
	2-State	'352		▲			•		T7-454
	3-State	'353		▲			•		T7-457
Octal 2-To-1 With Storage	3-State	'604					•		S-124
	OC	'605					•		S-124
	3-State	'606					•		S-124
	OC	'607					•		S-124
Quad 2-To-1 With Storage	2-State	'98				•			T7-107
	2-State	'298	•				•		T7-432
	2-State	'398					•		T7-499
	2-State	'399					•		T7-499
Quadruple 2-To-1	2-State	'157	•	▲		•	•	•	T7-181
	2-State	'158		▲			•	•	T7-181
	3-State	'257		▲			•	•	T7-372
	3-State	'258		▲			•	•	T7-372
6-Line-To-1-Line Universal Multiplexer	3-State	'857		▲	▲				S-279

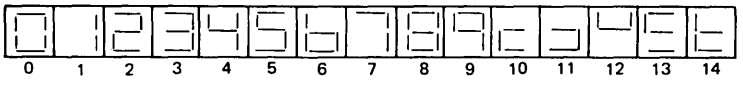
PRIORITY ENCODERS/REGISTERS

DESCRIPTION	TYPE	TECHNOLOGY				PAGE NO.†
		STD TTL	ALS	AS	LS	
Full BCD	'147	•			•	T7-151
Cascadable Octal	'148	•			•	T7-151
Cascadable Octal With 3-State Outputs	'348				•	T7-448
4-Bit Cascadable With Registers	'278	•				T7-403

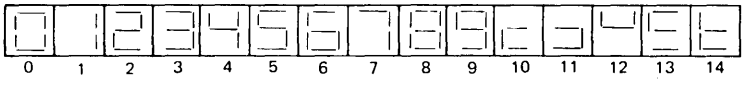
CODE CONVERTERS

DESCRIPTION	TYPE	TECHNOLOGY		PAGE NO.
		STD TTL	S	
6-Line-BCD To 6-Line Binary, Or 4-Line To 4-Line BCD 9's/BCD 10's Converters	'184	•		T7-290
6-Bit-Binary To 6-Bit-BCD Converters	'185	A		T7-290
BCD-To-Binary Converters	'484		•	2-71
Binary-To-BCD Converters	'485		•	2-71

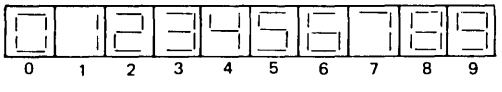
RESULTANT DISPLAYS USING '46A, '47A, '48, '49, 'L46, 'L47, 'LS47, 'LS48, 'LS49, 'LS347



RESULTANT DISPLAYS USING '246, '247, '248, '249, 'LS247, 'LS248, 'LS249, 'LS447



RESULTANT DISPLAYS USING '143, '144



† Page numbers with "T" preceding them refer to pages in *The TTL Data Book for Design Engineers*, second edition. Those with "S" preceding them refer to the *1981 Supplement to the TTL Data Book for Design Engineers*, second edition. Those with no letter prefix refer to pages in this book.

• Denotes available technology.

A Denotes "A" suffix version available in the technology indicated.

▲ Denotes planned new products.

ARITHMETIC CIRCUITS, ERROR DETECTION CIRCUITS, PROCESSORS AND CONTROLLERS

PARALLEL BINARY ADDERS

DESCRIPTION	TYPE	TECHNOLOGY						PAGE NO.†
		STD TTL	ALS	AS	H	LS	S	
1-Bit Gated	'80	•						T7-41
2-Bit	'82	•						T7-49
4-Bit	'83	A				A		T7-53
	'283	•				•	•	T7-415
Dual 1-Bit Carry-Save	'183				•	•		T7-287

ACCUMULATORS, ARITHMETIC LOGIC UNITS, LOOK-AHEAD CARRY GENERATORS

DESCRIPTION		TYPE	TECHNOLOGY					PAGE NO.†
			STD TTL	ALS	AS	LS	S	
4-Bit Parallel Binary Accumulators		'281					•	T7-410
		'681				•		S-197
4-Bit Arithmetic Logic Units/ Function Generators		'181	•		•	•	•	T7-271
		'381				•	•	T-484 S-60
		'881			•			S-288
Arithmetic Logic Unit With Ripple Carry		'382				•		S-291
Look-Ahead Carry Generators	16-Bit	'182	•				•	T7-282
	32-Bit	'882			•			S-291
Quad Serial Adder/Subtractor		'385				•		S-69
4-Bit-Slice Element		'481				•	•	3-3
8-Bit-Slice Element		'888			▲			

MULTIPLIERS

DESCRIPTION	TYPE	TECHNOLOGY					PAGE NO.†
		STD TTL	ALS	AS	LS	S	
2-Bit-By-4-Bit Parrallel Binary Multipliers	'261				•		T7-380
4-Bit-By-4-Bit Parrallel Binary Multipliers	'274					•	T7-391
	'284	•					T7-420
	'285	•					T7-420
7-Bit-Slice Wallace Trees	'275				•	•	T7-391
25-MHz 6-Bit-Binary Rate Multipliers	'97	•					T7-102
25-MHz Decade Rate Multipliers	'167	•					T7-222
8-Bit X 1-Bit 2's Complement Multiplier	'384				•		S-65
16-Bit Parallel Multiplier	'1616		▲				

COMPARATORS

DESCRIPTION						TYPE	TECHNOLOGY					PAGE NO.†
BITS	P=Q	P > Q	P < Q	OUTPUT	OUTPUT ENABLE		STD TTL	ALS	AS	L	LS	S	
4	Yes	Yes	No	2-State	Yes	'85	•				•	•	•	T7-57
	Yes	No	No	2-State	Yes	'521		▲						
8 with 20-kΩ Pull-Up Input	Yes	Yes	No	2-State	No	'682						•		S-203
	Yes	Yes	No	OC	No	'683						•		S-203
8	Yes	Yes	No	2-State	No	'684						•		S-203
	Yes	Yes	No	OC	No	'685						•		S-203
	Yes	Yes	No	2-State	Yes	'686						•		S-203
	Yes	Yes	No	OC	Yes	'687						•		S-203
	Yes	No	No	2-State	Yes	'688						•		S-203
	Yes	No	No	OC	Yes	'689						•		S-203
8 with Latched P Inputs	No	Yes	Yes	2-State	Yes	'885				•				S-293
8 with Latched P/Q Inputs	Yes	Yes	Yes	Latched	Yes	'856				▲				

OTHER ARITHMETIC OPERATORS

DESCRIPTION	TYPE	TECHNOLOGY							PAGE NO.†
		STD TTL	ALS	AS	H	L	LS	S	
Quad 2-Input Exclusive-OR Gates With Totem-Pole Outputs	'86	•	▲			•	•	•	T7-65
	'386						•		T7-487
Quad 2-Input Exclusive-OR Gates With Open-Collector Outputs	'136	•					•		T7-131
Quad 2-Input Exclusive-NOR Gates	'266						•		T7-386
Quad Exclusive OR/NOR Gates	'135							•	T7-129
4-Bit True/Complement, Element	'87				•				T7-70

ERROR DETECTION AND CORRECTION CIRCUITS, FARITY GENERATORS/CHECKERS

DESCRIPTION		TYPE	TECHNOLOGY					PAGE NO.†
			STD TTL	ALS	AS	LS	S	
9-Bit Odd/Even Parity Generators/Checkers		'280			▲	•	•	T7-406
8-Bit Odd/Even Parity Generators/Checkers		'180	•					T7-269
16-Bit Parallel Error Detection/Correction Circuit	3-State	'630				•		S-151
	OC	'631				•		S-151
32-Bit Parallel Error Detection/Correction Circuit		'632		▲				

BIPOLAR BIT-SLICE PROCESSOR ELEMENTS

DESCRIPTION	CASCADABLE TO N-BITS	TYPE	TECHNOLOGY				PAGE NO.†
			ALS	AS	LS	S	
4-Bit-Slice	Yes	'481			•	•	3-3
8-Bit-Slice	Yes	'888		▲			

MEMORY/MICROPROCESSOR CONTROLLERS

DESCRIPTION			TYPE	TECHNOLOGY				PAGE NO.†
				ALS	AS	LS	S	
System Controllers For 8080A			'428				•	T7-514
			'438				•	T7-514
System Controller, Universal			'482				•	3-57
System Controller, Universal (or for '888)			'890		▲			
Memory Refresh Controllers	Transparent, Burst Modes	4K, 16K	'600			•		S-119
		64K	'601			•		S-119
	Cycle Steal, Burst Modes	4K, 16K	'602			•		S-119
		64K	'603			•		S-119
Memory Cycle Controller			'608			•		S-128
Memory Mappers		3-State‡	'612			•		S-133
		OC‡	'613			•		S-133
Memory Mappers With Output Latches		3-State‡	'610			•		S-133
		OC‡	'611			•		S-133
Multi-Mode Latches (8080A Applications)			'412				•	T7-502

† Page numbers with "T" preceding them refer to pages in *The TTL Data Book for Design Engineers*, second edition. Those with "S" preceding them refer to the *1981 Supplement to the TTL Data Book for Design Engineers*, second edition. Those with no letter prefix refer to pages in this book.

‡ Map output type.

• Denotes available technology.

A Denotes "A" suffix version available in the technology indicated.

▲ Denotes planned new products.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

MEMORIES AND PROGRAMMABLE LOGIC ARRAYS

USER-PROGRAMMABLE READ-ONLY MEMORIES (PROM'S)
STANDARD PROM'S

DESCRIPTION	TYPE	ORGANIZATION	TYPE OUTPUT	PAGE NO.†
16K-Bit Arrays	▲ TBP28S165	2048W x 8B	3-State	
	▲ TBP28S165-55	2048W x 8B	3-State	
	TBP28S166	2048W x 8B	3-State	2-13
	TBP28SA166	2048W x 8B	OC	2-13
	▲ TBP28S166-55	2048W x 8B	3-State	
8K-Bit Arrays	TBP24S81	2048W x 4B	3-State	2-13
	‡ TBP24S81-55	2048W x 4B	3-State	2-13
	TBP24SA81	2048W x 4B	OC	2-13
	‡ TBP24SA81-55	2048W x 4B	OC	2-13
	TBP28S86	1024W x 8B	3-State	2-13
	‡ TBP28S86-60	1024W x 8B	3-State	2-13
	TBP28SA86	1024W x 8B	OC	2-13
	‡ TBP28SA86-60	1024W x 8B	OC	2-13
	TBP28S2708	1024W x 8B	3-State	2-13
	▲ TBP28S85	1024W x 8B	3-State	2-13
4K-Bit Arrays	TBP28S42	512W x 8B	3-State	2-13
	TBP28SA42	512W x 8B	OC	2-13
	▲ TBP28S45	512W x 8B	3-State	2-13
	TBP28S46	512W x 8B	3-State	2-13
	TBP28SA46	512W x 8B	OC	2-13
	TBP24S41	1024W x 4B	3-State	2-13
	TBP24SA41	1024W x 4B	OC	2-13
	√TBP18S46	512W x 8B	3-State	2-7
	√TBP18SA46	512W x 8B	OC	2-7
	√TBP18S42	512W x 8B	3-State	2-7
	√TBP18SA42	512W x 8B	OC	2-7
2K-Bit Arrays	√TBP18S22	256W x 8B	3-State	2-7
	√TBP18SA22	256W x 8B	OC	2-7
1K-Bit Arrays	√TBP14S10	256W x 4B	3-State	2-7
	√TBP14SA10	256W x 4B	OC	2-7
	TBP24S10	256W x 4B	3-State	2-13
	TBP24SA10	256W x 4B	OC	2-13
256-Bit Arrays	TBP18S030	32W x 8B	3-State	2-7
	TBP18SA030	32W x 8B	OC	2-7

LOW-POWER PROM'S

DESCRIPTION	TYPE	ORGANIZATION	TYPE OUTPUT	PAGE NO.†
16K-Bit Arrays	▲ TBP28L166	2048W x 8B	3-State	2-13
8K-Bit Arrays	▲ TBP28L85	1024W x 8B	3-State	2-13
	TBP28L86	1024W x 8B	3-State	2-13
4K-Bit Arrays	TBP28L42	512W x 8B	3-State	2-13
	▲ TBP28L45	512W x 8B	3-State	2-13
	TBP28L46	512W x 8B	3-State	2-13
2K-Bit Arrays	TBP28L22	256W x 8B	3-State	2-13
	TBP28LA22	256W x 8B	OC	2-13

POWER-DOWN PROM'S

DESCRIPTION	TYPE	ORGANIZATION	TYPE OUTPUT	PAGE NO.†
16K-Bit Arrays	▲ TBP28P165	2048W x 8B	3-State	
	▲ TBP28P166	2048W x 8B	3-State	2-13
8K-Bit Arrays	▲ TBP28P85	1024W x 8B	3-State	2-13
	▲ TBP28P86	1024W x 8B	3-State	
4K-Bit Arrays	▲ TBP28P42	512W x 8B	3-State	2-13
	▲ TBP28P45	512W x 8B	3-State	2-13
	▲ TBP28P46	512W x 8B	3-State	

REGISTERED PROM'S

DESCRIPTION	TYPE	ORGANIZATION	TYPE OUTPUT	PAGE NO.†
16K-Bit Arrays	▲ TBP28R166	2048W x 8B	3-State	2-13
	▲ TBP28R165	2048W x 8B	3-State	2-13
8K-Bit Arrays	▲ TBP28R85	1024W x 8B	3-State	2-13
4K-Bit Arrays	▲ TBP28R45	512W x 8B	3-State	2-13

READ-ONLY MEMORIES (ROM'S)

DESCRIPTION	ORGANIZATION	TYPE OF OUTPUT	TYPE	TECHNOLOGY				PAGE NO.†
				STD TTL	ALS	AS	S	
2048-Bit Arrays	512x4	OC	'270				•	T5-58
	256x8	OC	'271				•	T5-58
	512x4	3-State	'370				•	T5-67
	256x8	3-State	'371				•	T5-67
1024-Bit Arrays	256x4	OC	'187	•				T5-49
256-Bit Arrays	32x8	OC	'88	A				T5-27

RANDOM-ACCESS READ-WRITE MEMORIES (RAM'S)

DESCRIPTION	ORGANIZATION	TYPE OF OUTPUT	TYPE	TECHNOLOGY						PAGE NO.†
				STD TTL	ALS	AS	LS	S		
256-Bit Arrays	256x1	3-State	'201					•		2-50
	256x1	OC	'301					•		2-50
64-Bit Arrays	16x4	OC	'89	•						2-38
	16x4	3-State	'189				A	A		2-42
	16x4	3-State	'219				A			2-46
	16x4	OC	'289				A	A		2-42
	16x4	OC	'319				A			2-46
16-Bit Arrays	16x1	OC	'81	A						2-33
	16x1	OC	'84	A						2-33
16-Bit Multiple-Port Register File	8x2	3-State	'172	•						T7-245
16-Bit Register File	4x4	OC	'170	•			•			T7-237
	4x4	3-State	'670				•			T7-526
Dual 64-Bit Register Files	16x4, 16x4	3-State	'870			▲				S-281
	16x4, 16x4	3-State	'871			▲				S-281

FIRST-IN FIRST-OUT MEMORIES (FIFO'S)

DESCRIPTION		TYPE OF OUTPUT	TYPE	TECHNOLOGY				PAGE NO.†
				ALS	AS	LS	S	
Asynchronous 16 X 5		3-State	'225				•	2-61
Asynchronous 16 X 4	Gated Input, Output Ready	3-State	'222			•		2-53
		3-State	'224			•		2-53
	Single Input, Output Ready	OC	'227			•		2-53
		OC	'228			•		2-53

PROGRAMMABLE LOGIC ARRAYS

DESCRIPTION	TYPE	TECHNOLOGY			PAGE NO.†
		ALS	AS	LS	
Octal 16-Input AND-OR-Invert Gate Array	FP'16L8	•			5-3
Octal 16-Input Registered AND-OR Gate Array	FP'16R8	•			5-3
Hex 16-Input Registered AND-OR Gate Array	FP'16R6	•			5-3
Quad 16-Input Registered AND-OR Gate Array	FP'16R4	•			5-3
Field-Programmable Logic Sequencers With 3-State Outputs	FP'333			•	5-12
Field-Programmable Logic Sequencers With Open-Collector Outputs	FP'335			•	5-12
14 x 32 x 6 Field-Programmable Logic Arrays With 3-State Output	FP'839		•		5-16
14 x 32 x 6 Field-Programmable Logic Arrays With Open-Collector outputs	FP'840		•		5-16

† Page numbers with "T" preceding them refer to pages in *The TTL Data Book for Design Engineers*, second edition. Those with "S" preceding them refer to the *1981 Supplement to the TTL Data Book for Design Engineers*, second edition. Those with no letter prefix refer to pages in this book.

‡ Suffix indicates maximum address access time (ns).

√ Replaced with Series 24/28.

▲ Denotes planned new products.

Explanation of New Logic Symbols

EXPLANATION OF NEW LOGIC SYMBOLS

TABLE OF CONTENTS

LIST OF TABLES

If you have questions on this Explanation of New Logic Symbols, please contact:

F.A. Mann MS 84
Texas Instruments Incorporated
P.O. Box 225012
Dallas, Texas 75265
Telephone (214) 995-3746

IEEE Standards may be purchased from:

Institute of Electrical and Electronics Engineers, Inc.
345 East 47th Street
New York, N.Y. 10017

International Electrotechnical Commission (IEC) publications may be purchased from:

American National Standards Institute, Inc.
1430 Broadway
New York, N.Y. 10018

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

by F. A. Mann

1 INTRODUCTION

The International Electrotechnical Commission (IEC) has been developing a very powerful symbolic language that can show the relationship of each input of a digital logic circuit to each output without showing explicitly the internal logic. At the heart of the system is dependency notation, which will be explained in Section 4.

The system was introduced in the USA in a rudimentary form in IEEE/ANSI Standard Y32.14-1973. Lacking at that time a complete development of dependency notation, it offered little more than a substitution of rectangular shapes for the familiar distinctive shapes for representing the basic functions of AND, OR, negation, etc. This is no longer the case.

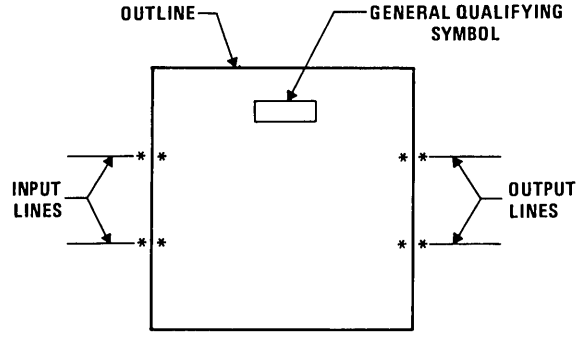
Internationally, Working Group 2 of IEC Technical Committee TC-3 is preparing a new document (Publication 617-12) that will consolidate the original work started in the mid 1960's and published in 1972 (Publication 117-15) and the amendments and supplements that have followed. Similarly for the USA, IEEE Committee SCC 11.9 is revising the publication IEEE Std 91/ANSI Y32.14. Texas Instruments is participating in the work of both organizations and this Supplement to the TTL Data Book introduces new logic symbols in anticipation of the new standards. When changes are made as the standards develop, future editions of the TTL Data Book will take those changes into account.

The following explanation of the new symbolic language is necessarily brief and greatly condensed from what the standards publications will finally contain. This is not intended to be sufficient for those people who will be developing symbols for new devices. It is primarily intended to make possible the understanding of the symbols used in this book; comparing the symbols with functional block diagrams and/or function tables will further help that understanding.

2 SYMBOL COMPOSITION

A symbol comprises an outline or a combination of outlines together with one or more qualifying symbols. The shape of the symbols is not significant. As shown in Figure 1, general qualifying symbols are used to tell exactly what logical operation is performed by the elements. Table I shows the general qualifying symbols used in this data book. Input lines are placed on the left and output lines are placed on the right. When an exception is made to that convention, the direction of signal flow is indicated by an arrow as shown in Figure 11.

All outputs of a single, unsubdivided element always have identical internal logic states determined by the function of the element except when otherwise indicated by an associated qualifying symbol or label inside the element.



*Possible positions for qualifying symbols relating to inputs and outputs

FIGURE 1 – SYMBOL COMPOSITION

The outlines of elements may be abutted or embedded in which case the following conventions apply. There is no logic connection between the elements when the line common to their outlines is in the direction of signal flow. There is at least one logic connection between the elements when the line common to their outlines is perpendicular to the direction of signal flow. The number of logic connections between elements will be clarified by the use of qualifying symbols and this is discussed further under that topic. If no indications are shown on either side of the common line, it is assumed there is only one connection.

When a circuit has one or more inputs that are common to more than one element of the circuit, the common-control block may be used. This is the only distinctively shaped outline used in the IEC system. Figure 2 shows that unless otherwise qualified by dependency notation, an input to the common-control block is an input to each of the elements below the common-control block.

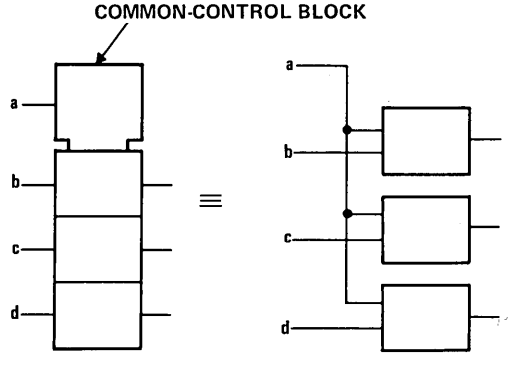


FIGURE 2 – ILLUSTRATION OF COMMON- CONTROL BLOCK

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

A common output depending on all elements of the array can be shown as the output of a common-output element. Its distinctive visual feature is the double line at its top. In addition the common-output element may have other inputs as shown in Figure 3. The function of the common-output element must be shown by use of a general qualifying symbol.

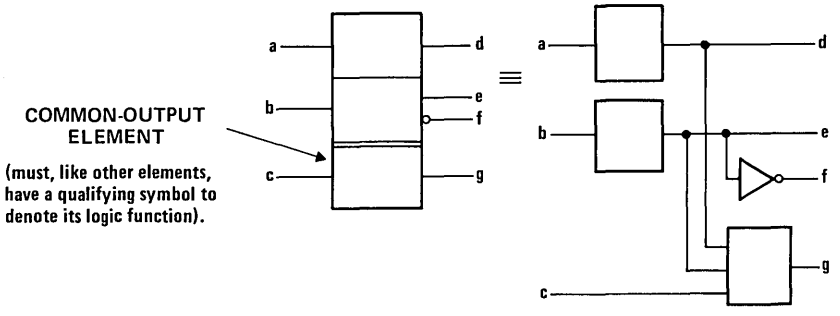


FIGURE 3 – ILLUSTRATION OF COMMON-OUTPUT ELEMENT

3 QUALIFYING SYMBOLS

3.1 General Qualifying Symbols

Table I shows the general qualifying symbols used in this data book. These characters are placed near the top center or the geometric center of a symbol or symbol element to define the basic function of the device represented by the symbol or of the element.

3.2 Qualifying Symbols for Inputs and Outputs

Qualifying symbols for inputs and outputs are shown in Table II and will be familiar to most users with the possible exception of the logic polarity and analog signal indicators. The older logic negation indicator means that the external 0 state produces the internal 1 state. The internal 1 state means the active state. Logic negation may be used in pure logic diagrams; in order to tie the external 1 and 0 logic states to the levels H (high) and L (low), a statement of whether positive logic (1 = H, 0 = L) or negative logic (1 = L, 0 = H) is being used is required or must be assumed. Logic polarity indicators eliminate the need for calling out the logic convention and are used in this data book in the symbology for actual devices. The presence of the triangular polarity indicator indicates that the L logic level will produce the internal 1 state (the active state) or that, in the case of an output, the internal 1 state will produce the external L level. Note how the active direction of transition for a dynamic input is indicated in positive logic, negative logic, and with polarity indication.

EXPLANATION OF NEW LOGIC SYMBOLS

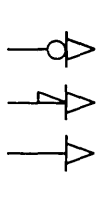
TABLE I – GENERAL QUALIFYING SYMBOLS

SYMBOL	DESCRIPTION	EXAMPLE
&	AND gate or function.	SN7400
≥1	OR gate or function. The symbol was chosen to indicate that at least one active input is needed to activate the output.	SN7402
=1	Exclusive OR. One and only one input must be active to activate the output.	SN7486
=	Logic identity. All inputs must stand at same state.	SN74180
2k	An even number of inputs must be active.	SN74180
2k+1	An odd number of inputs must be active.	*
1	The one input must be active.	SN7404
▷ or ◁	A buffer or element with more-than usual output capability (symbol is oriented in the direction of signal flow).	SN74S436
⊓	Schmitt trigger; element with hysteresis.	SN74LS18
X/Y	Coder, code converter (DEC/BCD, BIN/OUT, BIN/7-SEG, etc.).	SN74LS347
MUX	Multiplexer/data selector.	SN74150
DMUX or DX	Demultiplexer.	SN74138
Σ	Adder.	SN74LS385
P–Q	Subtracter.	SN74LS385
CPG	Look-ahead carry generator.	SN74182
π	Multiplier.	SN74LS384
COMP	Magnitude comparator.	SN74LS682
ALU	Arithmetic logic unit.	SN74LS381
⊓	Retriggerable monostable.	SN74LS422
1⊓	Non-retriggerable monostable (one-shot).	SN74121
G⊓	Astable element. Showing waveform is optional.	SN74LS320
!G⊓	Synchronously starting astable.	SN74LS624
G!⊓	Astable element that stops with a completed pulse.	
SRGm	Shift register. m = number of bits.	SN74LS595
CTRm	Counter. m = number of bits; cycle length = 2^m.	SN54LS590
CTR DIVm	Counter with cycle length = m.	SN74LS668
ROM	Read-only memory.	SN74187
RAM	Random-access read/write memory.	SN74170
FIFO	First-in, first-out memory.	SN74LS222
I=0	Element powers up cleared to 0 state.	SN74AS877
Φ	Highly complex function; "gray box" symbol with limited detail shown under special rules.	SN74LS608

*Not all of the general qualifying symbols have been used in this book, but they are included here for the sake of completeness.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TABLE II – QUALIFYING SYMBOLS FOR INPUTS AND OUTPUTS

	Logic negation at input. External 0 produces internal 1.
	Logic negation at output. Internal 1 produces external 0.
	Active-low input. Equivalent to  in positive logic.
	Active-low output. Equivalent to  in positive logic.
	Active-low input in the case of right-to-left signal flow.
	Active-low output in the case of right-to-left signal flow.
	Signal flow from right to left. If not otherwise indicated, signal flow is from left to right.
	Bidirectional signal flow.
	Dynamic inputs active on indicated transition. POSITIVE LOGIC: 1→0 (not used); 0→1. NEGATIVE LOGIC: 0→1 (not used); 1→0. POLARITY INDICATION: not used; H→L; L→H.
	Nonlogic connection. A label inside the symbol will usually define the nature of this pin.
	Input for analog signals.
	Internal connection. 1 state on left produces 1 state on right.
	Negated internal connection. 1 state on left produces 0 state on right.
	Dynamic internal connection. Transition from 0 to 1 on left produces transitory 1 state on right.
	Internal input (virtual input). It always stands at its internal 1 state unless affected by an overriding dependency relationship.
	Internal output (virtual output). Its effect on an internal input to which it is connected is indicated by dependency notation.

The internal connections between logic elements abutted together in a symbol may be indicated by the symbols shown. Each logic connection may be shown by the presence of qualifying symbols at one or both sides of the common line and if confusion can arise about the numbers of connections, use can be made of one of the internal connection symbols.

The internal (virtual) input is an input originating somewhere else in the circuit and is not connected directly to a terminal. The internal (virtual) output is likewise not connected directly to a terminal.

TABLE III – SYMBOLS INSIDE THE OUTLINE

¬	Postponed output (of a pulse-triggered flip-flop). The output changes when input initiating change (e.g., a C input) returns to its initial external state or level. See § 5.
⊓	Bi-threshold input (input with hysteresis)
◇	NPN open-collector or similar output that can supply a relatively low-impedance L level when not turned off. Requires external pull-up. Capable of positive-logic wired-AND connection. 
◈	Passive-pull-up output is similar to NPN open-collector output but is suplemented with a built-in passive pull-up.
◇	NPN open-emitter or similar output that can supply a relatively low-impedance H level when not turned off. Requires external pull-down. Capable of positive-logic wired-OR connection. 
◈	Passive-pull-down output is similar to NPN open-emitter output but is supplemented with a built-in passive pull-down.
▽	3-state output
EN	Enable input When at its internal 1-state, all outputs are enabled. When at its internal 0-state, open-collector and open-emitter outputs are off, three-state outputs are at normally defined internal logic states and at external high-impedance state, and all other outputs (e.g., totem-poles) are at the internal 0-state.
J, K, R, S, T	Usual meanings associated with flip-flops (e.g., R = reset, T = toggle)
D	Data input to a storage element equivalent to: 
→m ←m	Shift right (left) inputs, m = 1, 2, 3 etc. If m = 1, it is usually not shown.
+m −m	Counting up (down) inputs, m = 1, 2, 3 etc. If m = 1, it is usually not shown.
0 m	Binary grouping. m is highest power of 2.
CT = 15	The contents-setting input, when active, causes the content of a register to take on the indicated value.
CT = 9	The content output is active if the content of the register is as indicated.
	Input line grouping . . . . indicates two or more terminals used to implement a single logic input. e.g., The paired expander inputs of SN7450. 
"1"	Fixed-state output always stands at its internal 1 state. For example, see SN74185.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

The application of internal inputs and outputs requires an understanding of dependency notation, which is explained in Section 4.

In an array of elements, if the same general qualifying symbol and the same qualifying symbols associated with inputs and outputs would appear inside each of the elements of the array, these qualifying symbols are usually shown only in the first element. This is done to reduce clutter and to save time in recognition. Similarly, large identical elements that are subdivided into smaller elements may each be represented by an unsubdivided outline. The SN54LS440 symbol illustrates this principle.

3.3 Symbols Inside the Outline

Table III shows some symbols used inside the outline. Note particularly that open-collector, open-emitter, and three-state outputs have distinctive symbols. Also note that an EN input affects all of the outputs of the circuit and has no effect on inputs. When an enable input affects only certain outputs and/or affects one or more inputs, a form of dependency notation will indicate this (see 4.9). The effects of the EN input on the various types of outputs are shown.

It is particularly important to note that a D input is always the data input of a storage element. At its internal 1 state, the D input sets the storage element to its 1 state, and at its internal 0 state it resets the storage element to its 0 state.

The binary grouping symbol will be explained more fully in Section 8. Binary-weighted inputs are arranged in order and the binary weights of the least-significant and the most-significant lines are indicated by numbers. In this data book weights of input and output lines will be represented by powers of two usually only when the binary grouping symbol is used, otherwise, decimal numbers will be used. The grouped inputs generate an internal number on which a mathematical function can be performed or that can be an identifying number for dependency notation. See Figure 28. A frequent use is in addresses for memories.

Reversed in direction, the binary grouping symbol can be used with outputs. The concept is analogous to that for the inputs and the weighted outputs will indicate the internal number assumed to be developed within the circuit.

Other symbols are used inside the outlines in this data book in accordance with the IEC/IEEE standards but are not shown here. Generally these are associated with arithmetic operations and are self-explanatory.

When nonstandardized information is shown inside an outline, it is usually enclosed in square brackets [like these].

4 DEPENDENCY NOTATION

4.1 General Explanation

Dependency notation is the powerful tool that sets the IEC symbols apart from previous systems and makes compact, meaningful, symbols possible. It provides the means of denoting the relationship between inputs, outputs, or inputs and outputs without actually showing all the elements and interconnections involved. The information provided by dependency notation supplements that provided by the qualifying symbols for an element's function.

In the convention for the dependency notation, use will be made of the terms "affecting" and "affected". In cases where it is not evident which inputs must be considered as being the affecting or the affected ones (e.g., if they stand in an AND relationship), the choice may be made in any convenient way.

So far, ten types of dependency have been defined and all of these are used in this data book. They are listed below in the order in which they are presented and are summarized in Table IV following 4.11.

Section	Dependency Type or Other Subject
4.2	G, AND
4.3	General rules for dependency notation
4.4	V, OR
4.5	N, Negate, (Exclusive OR)
4.6	Z, Interconnection
4.7	C, Control
4.8	S, Set and R, Reset
4.9	EN, Enable
4.10	M, Mode
4.11	A, Address

4.2 G (AND) Dependency

A common relationship between two signals is to have them ANDed together. This has traditionally been shown by explicitly drawing an AND gate with the signals connected to the inputs of the gate. The 1972 IEC publication and the 1973 IEEE/ANSI standard showed several ways to show this AND relationship using dependency notation. While nine other forms of dependency have since been defined, the ways to invoke AND dependency are now reduced to one.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

In Figure 4 input **b** is ANDed with input **a** and the complement of **b** is ANDed with **c**. The letter G has been chosen to indicate AND relationships and is placed at input **b**, inside the symbol. A number considered appropriate by the symbol designer (1 has been used here) is placed after the letter G and also at each affected input. Note the bar over the 1 at input **c**.

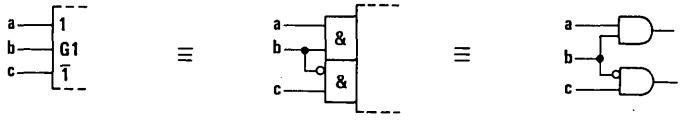


FIGURE 4 – G DEPENDENCY BETWEEN INPUTS

In Figure 5, output **b** affects input **a** with an AND relationship. The lower example shows that it is the internal logic state of **b**, unaffected by the negation sign, that is ANDed. Figure 6 shows input **a** to be ANDed with a dynamic input **b**.

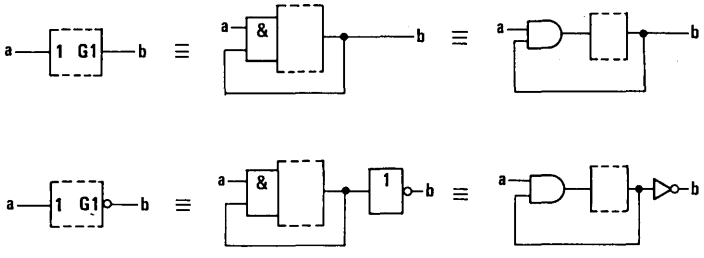


FIGURE 5 – G DEPENDENCY BETWEEN OUTPUTS AND INPUTS

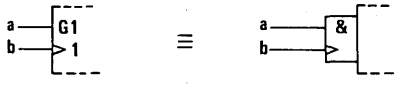


FIGURE 6 – G DEPENDENCY WITH A DYNAMIC INPUT

The rules for G dependency can be summarized thus:

When a G*m* input or output (*m* is a number) stands at its internal 1 state, all inputs and outputs affected by G*m* stand at their normally defined internal logic states. When the G*m* input or output stands at its 0 state, all inputs and outputs affected by G*m* stand at their internal 0 states.

4.3 Conventions for the Application of Dependency Notation in General

The rules for applying dependency relationships in general follow the same pattern as was illustrated for G dependency.

Application of dependency notation is accomplished by:

1) labeling the input (or output) *affecting* other inputs or outputs with the letter symbol indicating the relationship involved (e.g., G for AND) followed by an identifying number, appropriately chosen, and
2) labeling each input or output *affected* by that affecting input (or output) with that same number.

If it is the complement of the internal logic state of the affecting input or output that does the affecting, then a bar is placed over the identifying numbers at the affected inputs or outputs. See Figure 4.

If two affecting inputs or outputs have the same letter and same identifying number, they stand in an OR relationship to each other. See Figure 7.

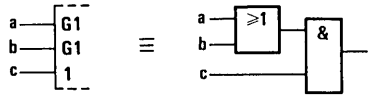


FIGURE 7 – OR'ED AFFECTING INPUTS

If the affected input or output requires a label to denote its function (e.g., "D"), this label will be *prefixed* by the identifying number of the affecting input. See Figure 12.

If an input or output is affected by more than one affecting input, the identifying numbers of each of the affecting inputs will appear in the label of the affected one, separated by commas. The normal reading order of these numbers is the same as the sequence of the affecting relationships. See Figure 12.

If the labels denoting the functions of affected inputs or outputs must be numbers, (e.g., outputs of a coder), the identifying numbers to be associated with both affecting inputs and affected inputs or outputs will be replaced by another character selected to avoid ambiguity, e.g., Greek letters. See Figure 8.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

FIGURE 8 – SUBSTITUTION FOR NUMBERS

4.4 V (OR) Dependency

The symbol denoting OR dependency is the letter V. See Figure 9.

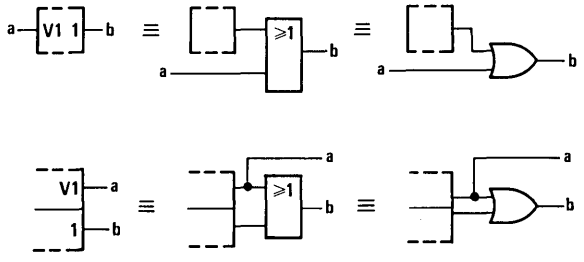
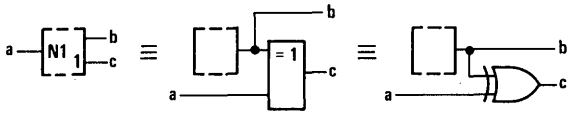


FIGURE 9 – V (OR) DEPENDENCY

When a V*m* input or output stands at its internal 1 state, all inputs and outputs affected by V*m* stand at their internal 1 states. When the V*m* input or output stands at its internal 0 state, all inputs and outputs affected by V*m* stand at their normally defined internal logic states.

4.5 N (Negate) (X-OR) Dependency

The symbol denoting negate dependency is the letter N. See Figure 10. Each input or output affected by an N*m* input or output stands in an exclusive-OR relationship with the N*m* input or output.



If a = 0, then c = b
If a = 1, then c = b

FIGURE 10 – N (NEGATE) (X-OR) DEPENDENCY

When an N*m* input or output stands at its internal 1 state, the internal logic state of each input and each output affected by N*m* is the complement of what it would otherwise be. When an N*m* input or output stands at its internal 0 state, all inputs and outputs affected by N*m* stand at their normally defined internal logic states.

4.6 Z (Interconnection) Dependency

The symbol denoting interconnection dependency is the letter Z.

Interconnection dependency is used to indicate the existence of internal logic connections between inputs, outputs, internal inputs, and/or internal outputs.

The internal logic state of an input or output affected by a Z*m* input or output will be the same as the internal logic state of the Z*m* input or output, unless modified by additional dependency notation. See Figure 11.

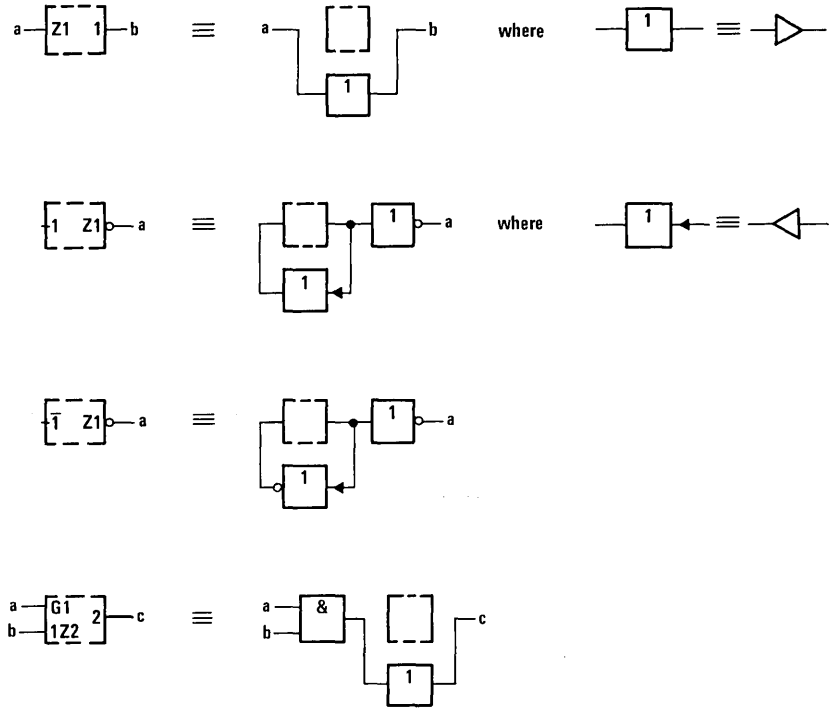


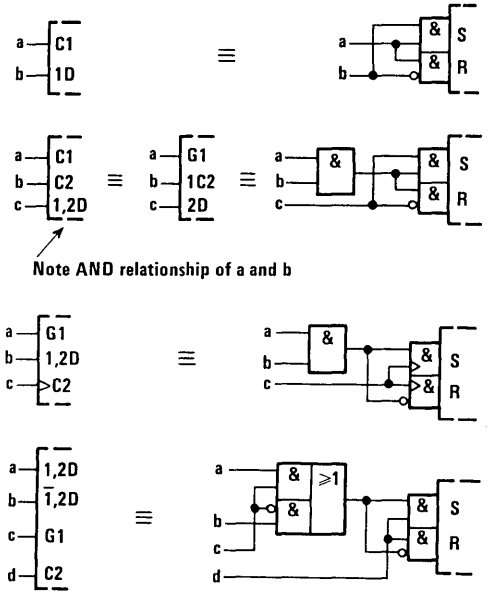
FIGURE 11 – Z (INTERCONNECTION) DEPENDENCY

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

4.7 C (Control) Dependency

The symbol denoting control dependency is the letter C.

Control inputs are usually used to enable or disable the data (D, J, K, R, or S) inputs of storage elements. They may take on their internal 1 states (be active) either statically or dynamically. In the latter case the dynamic input symbol is used as shown in the third example of Figure 12.



Input c selects which of a or b is stored when d goes low.

FIGURE 12 – C (CONTROL) DEPENDENCY

When a C*m* input or output stands at its internal 1 state, the inputs affected by C*m* have their normally defined effect on the function of the element, i.e., these inputs are enabled. When a C*m* input or output stands at its internal 0 state, the inputs affected by C*m* are disabled and have no effect on the function of the element.

4.8 S (Set) and R (Reset) Dependencies

The symbol denoting set dependency is the letter S. The symbol denoting reset dependency is the letter R.

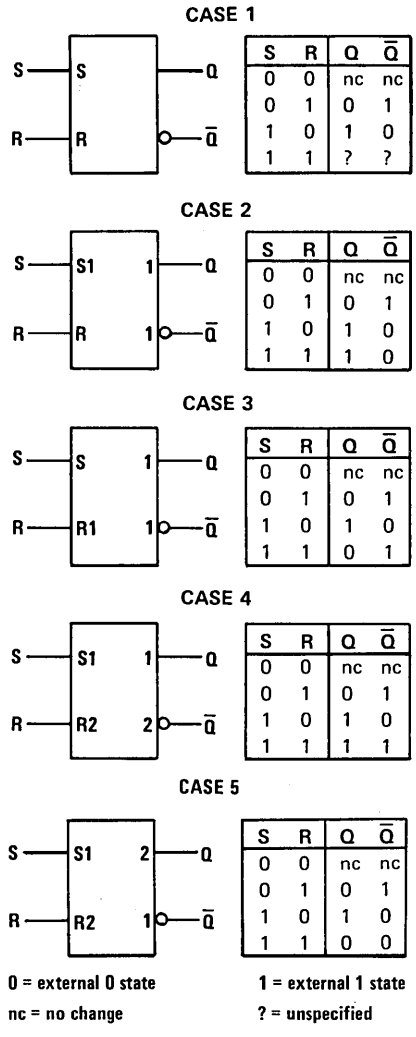
Set and reset dependenies are used if it is necessary to specify the effect of the combination R=S=1 on a bistable element. Case 1 in Figure 13 does not use S or R dependency.

When an S*m* input is at its internal 1 state, outputs affected by the Sm input will react, regardless of the state of an R input, as they normally would react to the combination S=1, R=0. See cases 2, 4, and 5 in Figure 13.

When an R*m* input is at its internal 1 state, outputs affected by the Rm input will react, regardless of the state of an S input, as they normally would react to the combination S=0, R=1. See cases 3, 4, and 5 in Figure 13.

When an S*m* or R*m* input is at its internal 0 state, it has no effect.

Note that the noncomplementary output patterns in cases 4 and 5 are only pseudo stable. The simultaneous return of the inputs to S=R=0 produces an unforeseeable stable and complementary output pattern.



S	R	Q	Q̄
0	0	nc	nc
0	1	0	1
1	0	1	0
1	1	?	?

S	R	Q	Q̄
0	0	nc	nc
0	1	0	1
1	0	1	0
1	1	1	0

S	R	Q	Q̄
0	0	nc	nc
0	1	0	1
1	0	1	0
1	1	0	1

S	R	Q	Q̄
0	0	nc	nc
0	1	0	1
1	0	1	0
1	1	1	1

S	R	Q	Q̄
0	0	nc	nc
0	1	0	1
1	0	1	0
1	1	0	0

FIGURE 13 – S (SET) AND R (RESET) DEPENDENCIES

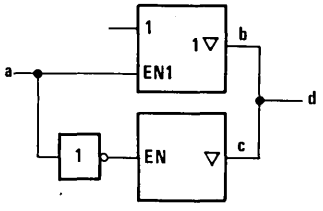
4.9 EN (Enable) Dependency

The symbol denoting enable dependency is the combination of letters EN.

An EN*m* input has the same effect on outputs as an EN input, see 3.1, but it effects only those outputs labeled with the identifying number *m*. It also affects those inputs labeled with the identifying number *m*. By contrast, an EN input affects all outputs and no inputs. The effect of an EN*m* input on an affected input is identical to that of a C*m* input. See Figure 14.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

When an EN*m* input stands at its internal 1 state, the inputs affected by EN*m* have their normally defined effect on the function of the element and the outputs affected by this input stand at their normally defined internal logic states, i.e., these inputs and outputs are enabled.



If a = 0, b is disabled and d = c
If a = 1, c is disabled and d = b

FIGURE 14 – EN (ENABLE) DEPENDENCY

When an EN*m* input stands at its internal 0 state, the inputs affected by EN*m* are disabled and have no effect on the function of the element, and the outputs affected by EN*m* are also disabled. Open-collector outputs are turned off, three-state outputs stand at their normally defined internal logic states but externally exhibit high impedance, and all other outputs (e.g., totem-pole outputs) stand at their internal 0 states.

4.10 M (Mode) Dependency

The symbol denoting mode dependency is the letter M.

Mode dependency is used to indicate that the effects of particular inputs and outputs of an element depend on the mode in which the element is operating.

If an input or output has the same effect in different modes of operation, the identifying numbers of the relevant affecting M*m* inputs will appear in the label of that affected input or output between parentheses and separated by solidi. See Figure 19.

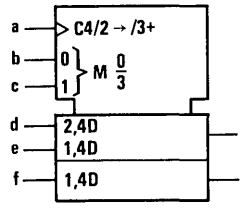
7

4.10.1 M Dependency Affecting Inputs

M dependency affects inputs the same as C dependency. When an M*m* input or M*m* output stands at its internal 1 state, the inputs affected by this M*m* input or M*m* output have their normally defined effect on the function of the element, i.e., the inputs are enabled.

When an M*m* input or M*m* output stands at its internal 0 state, the inputs affected by this M*m* input or M*m* output have no effect on the function of the element. When an affected input has several sets of labels separated by solidi (e.g., C4/2→/3+), any set in which the identifying number of the M*m* input or M*m* output appears has no effect and is to be ignored. This represents disabling of some of the functions of a multifunction input.

The circuit in Figure 15 has two inputs, **b** and **c**, that control which one of four modes (0, 1, 2, or 3) will exist at any time. Inputs **d**, **e**, and **f** are D inputs subject to dynamic control (clocking) by the **a** input. The numbers 1 and 2 are in the series chosen to indicate the modes so inputs **e** and **f** are only enabled in mode 1 (for parallel loading) and input **d** is only enabled in mode 2 (for serial loading). Note that input **a** has three functions. It is the clock for entering data. In mode 2, it causes right shifting of data, which means a shift away from the control block. In mode 3, it causes the contents of the register to be incremented by one count.



Note that all operations are synchronous.

In MODE 0 (b = 0, c = 0), the outputs remain at their existing states as none of the inputs has an effect.

In MODE 1 (b = 1, c = 0), parallel loading takes place thru inputs e and f.

In MODE 2 (b = 0, c = 1), shifting down and serial loading thru input d take place.

In MODE 3 (b = c = 1), counting up by increment of 1 per clock pulse takes place.

FIGURE 15 – M (MODE) DEPENDENCY AFFECTING INPUTS

4.10.2 M Dependency Affecting Outputs

When an M*m* input or M*m* output stands at its internal 1 state, the affected outputs stand at their normally defined internal logic states, i.e., the outputs are enabled.

When an M*m* input or M*m* output stands at its internal 0 state, at each affected output any set of labels containing the identifying number of that M*m* input or M*m* output has no effect and is to be ignored. When an output has several different sets of labels separated by solidi (e.g., 2,4/3,5), only those sets in which the identifying number of this M*m* input or M*m* output appears are to be ignored.

In Figure 16, mode 1 exists when the **a** input stands at its internal 1 state. The delayed output symbol is effective only in mode 1 (when input **a** = 1) in which case the device functions as a pulse-triggered flip-flop. See Section 5. When input **a** = 0, the device is not in mode 1 so the delayed output symbol has no effect and the device functions as a transparent latch.

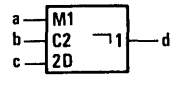


FIGURE 16 – TYPE OF FLIP-FLOP DETERMINED BY MODE

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

In Figure 17, if input **a** stands at its internal 1 state establishing mode 1, output **b** will stand at its internal 1 state only when the content of the register equals 9. Since output **b** is located in the common-control block with no defined function outside of mode 1, this output will stand at its internal 0 state when input **a** stands at its internal 0 state, regardless of the register content.

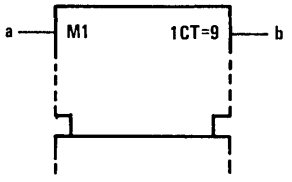


FIGURE 17 – DISABLING AN OUTPUT OF THE COMMON-CONTROL BLOCK

In Figure 18, if input **a** stands at its internal 1 state establishing mode 1, output **b** will stand at its internal 1 state only when the content of the register equals 15. If input **a** stands at its internal 0 state, output **b** will stand at its internal 1 state only when the content of the register equals 0.

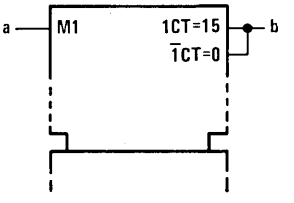


FIGURE 18 – DETERMINING AN OUTPUT'S FUNCTION

In Figure 19 inputs **a** and **b** are binary weighted to generate the numbers 0, 1, 2, or 3. This determines which one of the four modes exists.

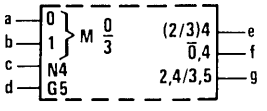


FIGURE 19 – DEPENDENT RELATIONSHIPS AFFECTED BY MODE

At output **e** the label set causing negation (if **c** = 1) is effective only in modes 2 and 3. In modes 0 and 1 this output stands at its normally defined state as if it had no labels. At output **f** the label set has effect when the mode is not 0 so output **e** is negated (if **c** = 1) in modes 1, 2, and 3. In mode 0 the label set has no effect so the output stands at its normally defined state. In this example 0,4 is equivalent to (1/2/3)4. At output **g** there are two label sets. The first set, causing negation (if **c** = 1), is effective only in mode 2. The second set, subjecting **g** to AND dependency on **d**, has effect only in mode 3.

Note that in mode 0 none of the dependency relationships has any effect on the outputs, so **e**, **f**, and **g** will all stand at the same state.

4.11 A (Address) Dependency

The symbol denoting address dependency is the letter A.

Address dependency provides a clear representation of those elements, particularly memories, that use address control inputs to select specified sections of a multidimensional array. Such a section of a memory array is usually called a word. The purpose of address dependency is to allow a symbolic presentation of the entire array. An input of the array shown at a particular element of this general section is common to the corresponding elements of all selected sections of the array. An output of the array shown at a particular element of this general section is the result of the OR function of the outputs of the corresponding elements of selected sections. If the label of an output of the array shown at a particular element of this general section indicates that this output is an open-circuit output or a three-state output, then this indication refers to the output of the array and not to those of the sections of the array.

Inputs that are not affected by any affecting address input have their normally defined effect on all sections of the array, whereas inputs affected by an address input have their normally defined effect only on the section selected by that address input.

An affecting address input is labelled with the letter A followed by an identifying number that corresponds with the address of the particular section of the array selected by this input. Within the general section presented by the symbol, inputs and outputs affected by an A*m* input are labelled with the letter A, which stands for the identifying numbers, i.e., the addresses, of the particular sections.

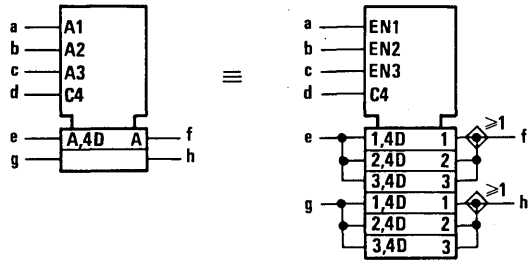


FIGURE 20 – A (ADDRESS) DEPENDENCY

Figure 20 shows a 3-word by 2-bit memory having a separate address line for each word and uses EN dependency to explain the operation. To select word 1, input a is taken to its 1 state, which establishes mode 1. Data can now be clocked into the inputs marked "1,4D". Unless words 2 and 3 are also selected, data cannot be clocked in at the inputs marked "2,4D" and "3,4D". The outputs will be the OR functions of the selected outputs, i.e., only those enabled by the active EN functions.

The identifying numbers of affecting address inputs correspond with the addresses of the sections selected by these inputs. They need not necessarily differ from those of other affecting dependency-inputs (e.g., G, V, N, . . .), because in the general section presented by the symbol they are replaced by the letter A.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

If there are several sets of affecting *Am* inputs for the purpose of independent and possibly simultaneous access to sections of the array, then the letter A is modified to 1A, 2A, . . . Because they have access to the same sections of the array, these sets of A inputs may have the same identifying numbers.

Figure 21 is another illustration of the concept.

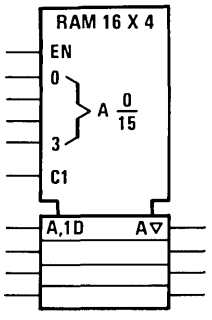


FIGURE 21

FIGURE 21 – ARRAY OF 16 SECTIONS OF FOUR TRANSPARENT LATCHES WITH 3-STATE OUTPUTS COMPRISING A 16-WORD X 4-BIT RANDOM-ACCESS MEMORY

TABLE IV – SUMMARY OF DEPENDENCY NOTATION

TYPE OF DEPENDENCY	LETTER SYMBOL*	AFFECTING INPUT AT ITS 1-STATE	AFFECTING INPUT AT ITS 0-STATE
Address	A	Permits action (address selected)	Prevents action (address not selected)
Control	C	Permits action	Prevents action
Enable	EN	Permits action	Prevents action of inputs. ◇outputs off. ▽outputs at external high impedance, no change in internal logic state. Other outputs at internal 0 state.
AND	G	Permits action	Imposes 0 state
Mode	M	Permits action (mode selected)	Prevents action (mode not selected)
Negate (X-OR)	N	Complements state	No effect
RESET	R	Affected output reacts as it would to S = 0, R = 1	No effect
SET	S	Affected output reacts as it would to S = 1, R = 0	No effect
OR	V	Imposes 1 state	Permits action
Interconnection	Z	Imposes 1 state	Imposes 0 state

*These letter symbols appear at the AFFECTING input (or output) and are followed by a number. Each input (or output) AFFECTED by that input is labeled with that same number. When the labels EN, R, and S appear at inputs without the following numbers, the descriptions above do not apply. The action of these inputs is described under "Symbols Inside The Outline", see 3.1.

BISTABLE ELEMENTS

The dynamic input symbol, the postponed output symbol, and dependency notation provide the tools to differentiate four main types of bistable elements and make synchronous and asynchronous inputs easily recognizable. See Figure 22. The first column shows the essential distinguishing features; the other columns show examples.

Transparent latches have a level-operated control input. The D input is active as long as the C input is at its internal 1 state. The outputs respond immediately. Edge-triggered elements accept data from D, J, K, R, or S inputs on the active transition of C. Pulse-triggered elements require the setup of data before the start of the control pulse; the C input is considered static since the data must be maintained as long as C is at its 1 state. The output is postponed until C returns to its 0 state. The data-lock-out element is similar to the pulse-triggered version except that the C input is considered dynamic in that shortly after C goes through its active transition, the data inputs are disabled and data does not have to be held. However, the output is still postponed until the C input returns to its initial external level.

Notice that synchronous inputs can be readily recognized by their dependency labels (1D, 1J, 1K, 1S, 1R) compared to the asynchronous inputs (S, R), which are not dependent on the C inputs.

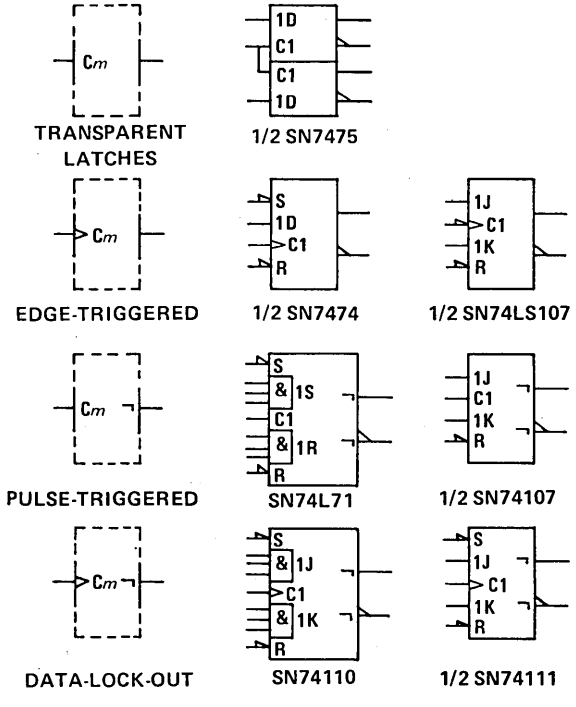


FIGURE 22 – FOUR TYPES OF BISTABLE CIRCUITS

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

6 CODERS

The general symbol for a coder or code converter is shown in Figure 23. X and Y may be replaced by appropriate indications of the code used to represent the information at the inputs and at the outputs, respectively.

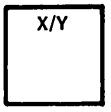


FIGURE 23 – CODER GENERAL SYMBOL

Indication of code conversion is based on the following rule:

> Depending on the input code, the internal logic states of the inputs determine an internal value. This value is reproduced by the internal logic states of the outputs, depending on the output code.

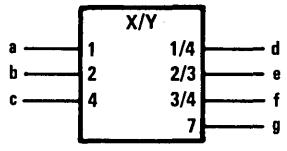
The indication of the relationships between the internal logic states of the inputs and the internal value is accomplished by:

1) labelling the inputs with numbers. In this case the internal value equals the sum of the weights associated with those inputs that stand at their internal 1-state, or by
2) replacing X by an appropriate indication of the input code and labelling the inputs with characters that refer to this code.

The relationships between the internal value and the internal logic states of the outputs are indicated by:

1) labelling each output with a list of numbers representing those internal values that lead to the internal 1-state of that output. These numbers shall be separated by solidi as in Figure 24. This labelling may also be applied when Y is replaced by a letter denoting a type of dependency (see Section 7). If a continuous range of internal values produces the internal 1 state of an output, this can be indicated by two numbers that are inclusively the beginning and the end of the range, with these two numbers separated by three dots, e.g., 4 . . . 9 = 4/5/6/7/8/9, or by
2) replacing Y by an appropriate indication of the output code and labelling the outputs with characters that refer to this code as in Figure 25.

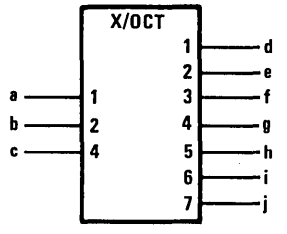
Alternatively, the general symbol may be used together with an appropriate reference to a table in which the relationship between the inputs and outputs is indicated. This is a recommended way to symbolize a PROM after it has been programmed.



TRUTH TABLE

INPUTS			OUTPUTS			
c	b	a	g	f	e	d
0	0	0	0	0	0	0
0	0	1	0	0	0	1
0	1	0	0	0	1	0
0	1	1	0	1	1	0
1	0	0	0	1	0	1
1	0	1	0	0	0	0
1	1	0	0	0	0	0
1	1	1	1	0	0	0

FIGURE 24 – AN X/Y CODE CONVERTER



TRUTH TABLE

INPUTS			OUTPUTS						
c	b	a	j	i	h	g	f	e	d
0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	1
0	1	0	0	0	0	0	0	1	0
0	1	1	0	0	0	0	1	0	0
1	0	0	0	0	0	1	0	0	0
1	0	1	0	0	1	0	0	0	0
1	1	0	0	1	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0

FIGURE 25 – AN X/OCTAL CODE CONVERTER

7 USE OF A CODER TO PRODUCE AFFECTING INPUTS

It often occurs that a set of affecting inputs for dependency notation is produced by decoding the signals on certain inputs to an element. In such a case use can be made of the symbol for a coder as an embedded symbol. See Figure 26.

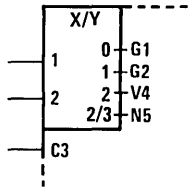


FIGURE 26 – PRODUCING VARIOUS TYPES OF DEPENDENCIES

If all affecting inputs produced by a coder are of the same type and their identifying numbers correspond with the numbers shown at the outputs of the coder, Y (in the qualifying symbol X/Y) may be replaced by the letter denoting the type of dependency. The indications of the affecting inputs should then be omitted. See Figure 27.

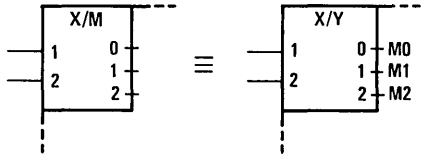


FIGURE 27 – PRODUCING ONE TYPE OF DEPENDENCY

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

8 USE OF BINARY GROUPING TO PRODUCE AFFECTING INPUTS

If all affecting inputs produced by a coder are of the same type and have consecutive identifying numbers not necessarily corresponding with the numbers that would have been shown at the outputs of the coder, use can be made of the binary grouping symbol (see 3.1). k external lines effectively generate 2^k internal inputs. The bracket is followed by the letter denoting the type of dependency followed by $\frac{m1}{m2}$. The m1 is to be replaced by the smallest identifying number and the m2 by the largest one, as shown in Figure 28.

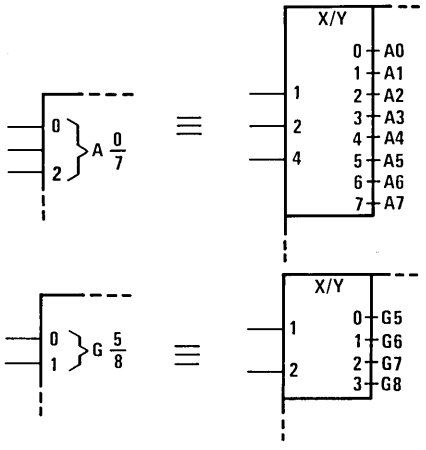


FIGURE 28 – USE OF THE BINARY GROUPING SYMBOL

9 SEQUENCE OF INPUT LABELS

If an input having a single functional effect is affected by other inputs, the qualifying symbol (if there is any) for that functional effect is preceded by the labels corresponding to the affecting inputs. The left-to-right order of these preceding labels is the order in which the effects or modifications must be applied. The affected input has no functional effect on the element if the logic state of any one of the affecting inputs, considered separately, would cause the affected input to have no effect, regardless of the logic states of other affecting inputs.

If an input has several different functional effects or has several different sets of affecting inputs, depending on the mode of action, the input may be shown as often as required. However, there are cases in which this method of presentation is not advantageous. In those cases the input may be shown once with the different sets of labels separated by solidi. See Figure 29. No meaning is attached to the order of these sets of labels. If one of the functional effects of an input is that of an unlabelled input of the element, a solidus will precede the first set of labels shown.

If all inputs of a combinational element are disabled (caused to have no effect on the function of the element), the internal logic states of the outputs of the element are not specified by the symbol. If all inputs of a sequential element are disabled, the content of this element is not changed and the outputs remain at their existing internal logic states.

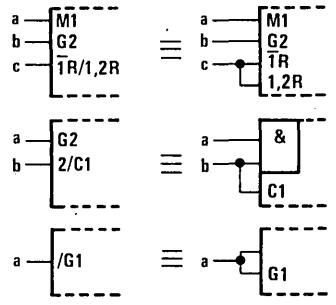


FIGURE 29 – INPUT LABELS

Labels may be factored using algebraic techniques.

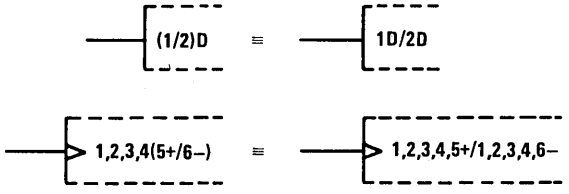


FIGURE 30 – FACTORING INPUT LABELS

10 SEQUENCE OF OUTPUT LABELS

If an output has a number of different labels, regardless of whether they are identifying numbers of affecting inputs or outputs or not, these labels are shown in the following order:

1) if the postponed output symbol has to be shown, this comes first, if necessary preceded by the indications of the inputs to which it must be applied;

2) followed by the labels indicating modifications of the internal logic state of the output, such that the left-to-right order of these labels corresponds with the order in which their effects must be applied;

3) followed by the label indicating the effect of the output on inputs and other outputs of the element.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

Symbols for open-circuit or three-state outputs, where applicable, are placed just inside the outside boundary of the symbol adjacent to the output line. See Figure 31.

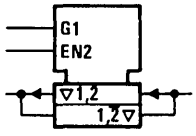


FIGURE 31 – PLACEMENT OF 3-STATE SYMBOLS

If an output needs several different sets of labels that represent alternative functions (e.g., depending on the mode of action), these sets may be shown on different output lines that must be connected outside the outline. However, there are cases in which this method of presentation is not advantageous. In those cases the output may be shown once with the different sets of labels separated by solidi. See Figure 32.

Two adjacent identifying numbers of affecting inputs in a set of labels that are not already separated by a nonnumeric character should be separated by a comma.

If a set of labels of an output not containing a solidus contains the identifying number of an affecting M*m* input standing at its internal 0 state, this set of labels has no effect on that output.

Labels may be factored using algebraic techniques.

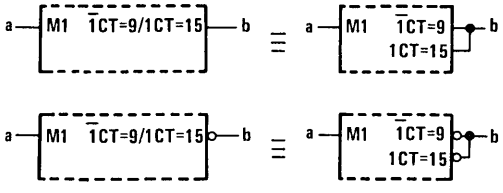


FIGURE 32 – OUTPUT LABELS

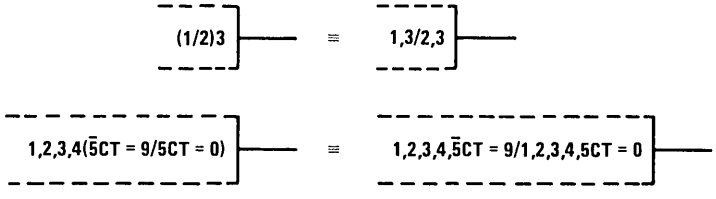


FIGURE 33 – FACTORING OUTPUT LABELS

If you have questions on this Explanation of New Logic Symbols, please contact:

F.A. Mann MS 84
Texas Instruments Incorporated
P.O. Box 225012
Dallas, Texas 75265
Telephone (214) 995-3746

IEEE Standards may be purchased from:

Institute of Electrical and Electronics Engineers, Inc.
345 East 47th Street
New York, N.Y. 10017

International Electrotechnical Commission (IEC) publications may be purchased from:

American National Standards Institute, Inc.
1430 Broadway
New York, N.Y. 10018

Product Guide
Bipolar Digital Products

00

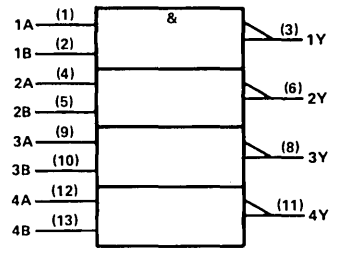
QUADRUPLE 2-INPUT POSITIVE-NAND GATES

typical performance

TYPE	POWER	DELAY
'00	10 mW	10 ns
'ALS00	1.28 mW	4.5 ns
'H00	22 mW	6 ns
'L00	1 mW	33 ns
'LS00	2 mW	9.5 ns
'S00	19 mW	3 ns

SN5400 (J,FC) SN7400 (J,N)
SN54ALS00 (J,FC) SN74ALS00 (J,N,FN)
SN54H00 (J,FC) SN74H00 (J,N)
SN54L00 (J)
SN54LS00 (J,FC) SN74LS00 (J,N)
SN54S00 (J,FC) SN74S00 (J,N,FN)

logic symbol†



positive logic: $Y = \overline{AB}$

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	1A	8	3Y	1	nc	11	3Y
2	1B	9	3A	2	nc	12	nc
3	1Y	10	3B	3	1A	13	3A
4	2A	11	4Y	4	1B	14	nc
5	2B	12	4A	5	1Y	15	3B
6	2Y	13	4B	6	2A	16	4Y
7	GND	14	V_{CC}	7	2B	17	nc
				8	nc	18	4A
				9	2Y	19	4B
				10	GND	20	V_{CC}

See *The TTL Data Book*

01

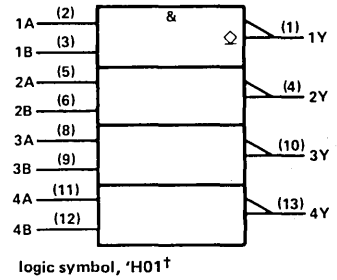
QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

typical performance

TYPE	POWER	DELAY
'01	10 mW	22 ns
'ALS01	1.28 mW	16 ns
'H01	22 mW	8 ns
'LS01	2 mW	16 ns

SN5401 (J,FC) SN7401 (J,N)
SN54ALS01 (J,FC) SN74ALS01 (J,N,FN)
SN54H01 (J,FC) SN74H01 (J,N)
SN54LS01 (J,FC) SN74LS01 (J,N)

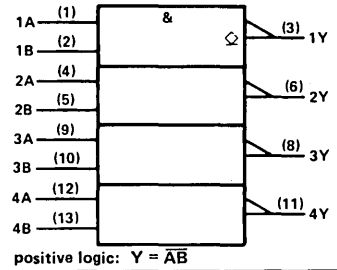
logic symbol, '01, 'ALS01, 'LS01†



pin assignments, '01, 'ALS01, 'LS01

J, N PACKAGES				FC, FN PACKAGES			
1	1Y	8	3A	1	nc	11	3A
2	1A	9	3B	2	1Y	12	nc
3	1B	10	3Y	3	nc	13	3B
4	2Y	11	4A	4	1A	14	nc
5	2A	12	4B	5	1B	15	3Y
6	2B	13	4Y	6	2Y	16	4A
7	GND	14	V_{CC}	7	2A	17	4B
				8	nc	18	nc
				9	2B	19	4Y
				10	GND	20	V_{CC}

logic symbol, 'H01†



positive logic: $Y = \overline{AB}$

pin assignments, 'H01

J, N PACKAGES				FC, FN PACKAGES			
1	1A	8	3Y	1	nc	11	3Y
2	1B	9	3A	2	1A	12	nc
3	1Y	10	3B	3	nc	13	3A
4	2A	11	4Y	4	1B	14	nc
5	2B	12	4A	5	1Y	15	3B
6	2Y	13	4B	6	2A	16	4Y
7	GND	14	V_{CC}	7	2B	17	4A
				8	nc	18	nc
				9	2Y	19	4B
				10	GND	20	V_{CC}

See *The TTL Data Book*

02

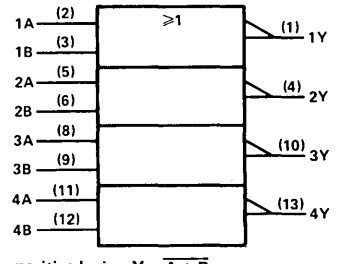
QUADRUPLE 2-INPUT POSITIVE-NOR GATES

typical performance

TYPE	POWER	DELAY
'02	14 mW	10 ns
'ALS02	1.89 mW	5.5 ns
'L02	1.5 mW	33 ns
'LS02	2.75 mW	10 ns
'S02	29 mW	3.5 ns

SN5402 (J,FC) SN7402 (J,N)
SN54ALS02 (J,FC) SN74ALS02 (J,N,FN)
SN54L02 (J)
SN54LS02 (J,FC) SN74LS02 (J,N)
SN54S02 (J,FC) SN74S02 (J,N,FN)

logic symbol†



positive logic: $Y = \overline{A + B}$

See *The TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	1Y	8	3A	1	nc	11	3A
2	1A	9	3B	2	1Y	12	nc
3	1B	10	3Y	3	nc	13	3B
4	2Y	11	4A	4	1A	14	nc
5	2A	12	4B	5	1B	15	3Y
6	2B	13	4Y	6	2Y	16	4A
7	GND	14	V_{CC}	7	2A	17	4B
				8	nc	18	nc
				9	2B	19	4Y
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection

03

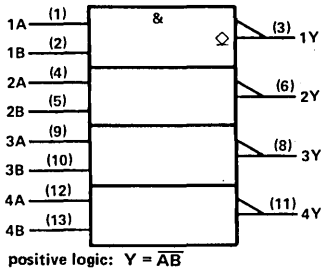
QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

typical performance

TYPE	POWER	DELAY
'03	10 mW	22 ns
'ALS03	1.28 mW	16 ns
'L03	1 mW	46 ns
'LS03	2 mW	16 ns
'S03	17.5 mW	16 ns

SN5403 (J,FC) SN7403 (J,N)
SN54ALS03 (J,FC) SN74ALS03 (J,N,FN)
SN54L03 (J)
SN54LS03 (J,FC) SN74LS03 (J,N)
SN54S03 (J,FC) SN74S03 (J,N,FN)

logic symbol†



positive logic: $Y = \overline{AB}$
See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	1A	8	3Y	1	nc	11	3Y
2	1B	9	3A	2	nc	12	nc
3	1Y	10	3B	3	1A	13	3A
4	2A	11	4Y	4	1B	14	nc
5	2B	12	4A	5	1Y	15	3B
6	2Y	13	4B	6	2A	16	4Y
7	GND	14	V_{CC}	7	2B	17	nc
				8	nc	18	4A
				9	2Y	19	4B
				10	GND	20	V_{CC}

04

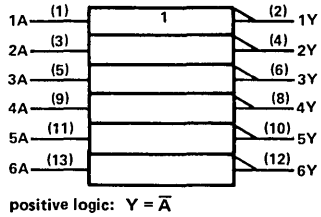
HEX INVERTERS

typical performance

TYPE	POWER	DELAY
'04	10 mW	10 ns
'ALS04	1.27 mW	3.5 ns
'H04	22 mW	6 ns
'L04	1 mW	33 ns
'LS04	2 mW	9.5 ns
'S04	19 mW	3 ns

SN5404 (J,FC) SN7404 (J,N)
SN54ALS04 (J,FC) SN74ALS04 (J,N,FN)
SN54H04 (J,FC) SN74H04 (J,N)
SN54L04 (J)
SN54LS04 (J,FC) SN74LS04 (J,N)
SN54S04 (J,FC) SN74S04 (J,N,FN)

logic symbol†



positive logic: $Y = \overline{A}$
See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	1A	8	4Y	1	1A	11	nc
2	1Y	9	4A	2	nc	12	4Y
3	2A	10	5Y	3	nc	13	nc
4	2Y	11	5A	4	1Y	14	4A
5	3A	12	6Y	5	2A	15	5Y
6	3Y	13	6A	6	2Y	16	5A
7	GND	14	V_{CC}	7	3A	17	6Y
				8	nc	18	nc
				9	3Y	19	6A
				10	GND	20	V_{CC}

05

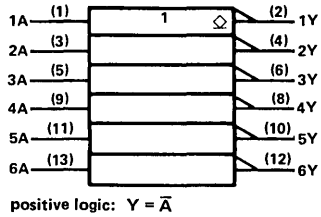
HEX INVERTERS WITH OPEN-COLLECTOR OUTPUTS

typical performance

TYPE	POWER	DELAY
'05	10 mW	24 ns
'ALS05	1.27 mW	13.5 ns
'H05	22 mW	8 ns
'LS05	2 mW	16 ns
'S05	17.5 mW	5 ns

SN5405 (J,FC) SN7405 (J,N)
SN54ALS05 (J,FC) SN74ALS05 (J,N,FN)
SN54H05 (J,FC) SN74H05 (J,N)
SN54LS05 (J,FC) SN74LS05 (J,N)
SN54S05 (J,FC) SN74S05 (J,N,FN)

logic symbol†



positive logic: $Y = \overline{A}$
See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	1A	8	4Y	1	1A	11	nc
2	1Y	9	4A	2	nc	12	4Y
3	2A	10	5Y	3	nc	13	nc
4	2Y	11	5A	4	1Y	14	4A
5	3A	12	6Y	5	2A	15	5Y
6	3Y	13	6A	6	2Y	16	5A
7	GND	14	V_{CC}	7	3A	17	6Y
				8	nc	18	nc
				9	3Y	19	6A
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

06

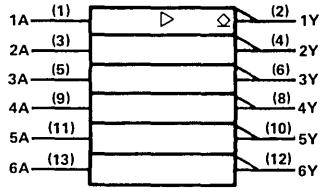
HEX INVERTER BUFFER/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

typical performance

TYPE	HIGH-LEVEL OUTPUT VOLTAGE	LOW-LEVEL OUTPUT CURRENT	TYPICAL DELAY TIME	TYPICAL POWER PER GATE
SN54'	30 V	30 mA	12.5 ns	26 mW
SN74'	30 V	40 mA	12.5 ns	26 mW

SN5406 (J,FC) SN7406 (J,N)

logic symbol†



positive logic: $Y = \overline{A}$

See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES	
1	1A	8	4Y	1 1A	11 nc
2	1Y	9	4A	2 nc	12 4Y
3	2A	10	5Y	3 nc	13 nc
4	2Y	11	5A	4 1Y	14 4A
5	3A	12	6Y	5 2A	15 5Y
6	3Y	13	6A	6 2Y	16 5A
7	GND	14	V_{CC}	7 3A	17 6Y
				8 nc	18 nc
				9 3Y	19 6A
				10 GND	20 V_{CC}

07

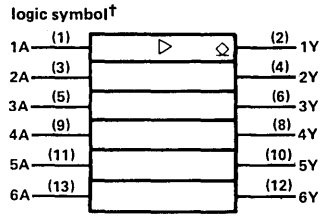
HEX BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

typical performance

TYPE	HIGH-LEVEL OUTPUT VOLTAGE	LOW-LEVEL OUTPUT CURRENT	TYPICAL DELAY TIME	TYPICAL POWER PER GATE
SN54'	30 V	30 mA	13 ns	21 mW
SN74'	30 V	40 mA	13 ns	21 mW

SN5407 (J,FC) SN7407 (J,N)

logic symbol†



positive logic: Y = A

See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES	
1	1A	8	4Y	1 1A	11 nc
2	1Y	9	4A	2 nc	12 4Y
3	2A	10	5Y	3 nc	13 nc
4	2Y	11	5A	4 1Y	14 4A
5	3A	12	6Y	5 2A	15 5Y
6	3Y	13	6A	6 2Y	16 5A
7	GND	14	V_{CC}	7 3A	17 6Y
				8 nc	18 nc
				9 3Y	19 6A
				10 GND	20 V_{CC}

08

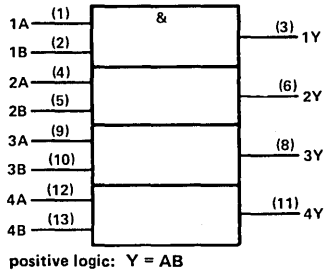
QUADRUPLE 2-INPUT POSITIVE-AND GATES

typical performance

TYPE	POWER	DELAY
'08	19 mW	15 ns
'ALS08	2.19 mW	6.5 ns
'LS08	4.25 mW	12 ns
'S08	32 mW	4.75 ns

SN5408 (J,FC) SN7408 (J,N)
SN54ALS08 (J,FC) SN74ALS08 (J,N,FN)
SN54LS08 (J,FC) SN74LS08 (J,N)
SN54S08 (J,FC) SN74S08 (J,N,FN)

logic symbol†



positive logic: Y = AB

See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES	
1	1A	8	3Y	1 nc	11 3Y
2	1B	9	3A	2 nc	12 nc
3	1Y	10	3B	3 1A	13 3A
4	2A	11	4Y	4 1B	14 nc
5	2B	12	4A	5 1Y	15 3B
6	2Y	13	4B	6 2A	16 4Y
7	GND	14	V_{CC}	7 2B	17 nc
				8 nc	18 4A
				9 2Y	19 4B
				10 GND	20 V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

8

09

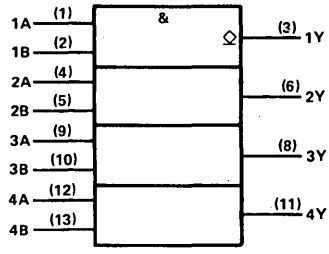
QUADRUPLE 2-INPUT POSITIVE-AND GATES WITH OPEN-COLLECTOR OUTPUTS

SN5409 (J,FC) SN7409 (J,N)
SN54ALS09 (J,FC) SN74ALS09 (J,N,FN)
SN54LS09 (J,FC) SN74LS09 (J,N)
SN54S09 (J,FC) SN74S09 (J,N,FN)

typical performance

TYPE	POWER	DELAY
'09	19.4 mW	18.5 ns
'ALS09	2.22 mW	15 ns
'LS09	4.25 mW	20 ns
'S09	32 mW	6.5 ns

logic symbol†



positive logic: Y = AB
See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES	
1 1A	8 3Y	1 nc	11 3Y		
2 1B	9 3A	2 nc	12 nc		
3 1Y	10 3B	3 1A	13 3A		
4 2A	11 4Y	4 1B	14 nc		
5 2B	12 4A	5 1Y	15 3B		
6 2Y	13 4B	6 2A	16 4Y		
7 GND	14 V_{CC}	7 2B	17 nc		
		8 nc	18 4A		
		9 2Y	19 4B		
		10 GND	20 V_{CC}		

10

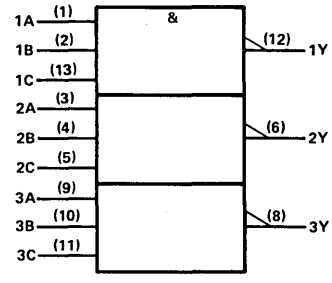
TRIPLE 3-INPUT POSITIVE-NAND GATES

SN5410 (J,FC) SN7410 (J,N)
SN54ALS10 (J,FC) SN74ALS10 (J,N,FN)
SN54H10 (J,FC) SN74H10 (J,N)
SN54L10 (J)
SN54LS10 (J,FC) SN74LS10 (J,N)
SN54S10 (J,FC) SN74S10 (J,N,FN)

typical performance

TYPE	POWER	DELAY
'10	10 mW	10 ns
'ALS10	1.27 mW	7 ns
'H10	22 mW	6 ns
'L10	1 mW	33 ns
'LS10	2 mW	9.5 ns
'S10	19 mW	3 ns

logic symbol†



positive logic: $Y = \overline{ABC}$
See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES	
1 1A	8 3Y	1 1A	11 nc		
2 1B	9 3A	2 nc	12 3Y		
3 2A	10 3B	3 nc	13 nc		
4 2B	11 3C	4 1B	14 nc		
5 2C	12 1Y	5 2A	15 3A		
6 2Y	13 1C	6 2B	16 3B		
7 GND	14 V_{CC}	7 2C	17 3C		
		8 nc	18 1Y		
		9 2Y	19 1C		
		10 GND	20 V_{CC}		

11

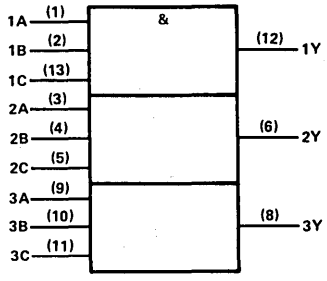
TRIPLE 3-INPUT POSITIVE-AND GATES

SN54ALS11 (J,FC) SN74ALS11 (J,N,FN)
SN54H11 (J,FC) SN74H11 (J,N)
SN54LS11 (J,FC) SN74LS11 (J,N)
SN54S11 (J,FC) SN74S11 (J,N,FN)

typical performance

TYPE	POWER	DELAY
'ALS11	2.17 mW	9 ns
'H11	40 mW	8.2 ns
'LS11	4.25 mW	12 ns
'S11	31 mW	4.75 ns

logic symbol†



positive logic: Y = ABC
See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES	
1 1A	8 3Y	1 1A	11 nc		
2 1B	9 3A	2 nc	12 3Y		
3 2A	10 3B	3 nc	13 nc		
4 2B	11 3C	4 1B	14 nc		
5 2C	12 1Y	5 2A	15 3A		
6 2Y	13 1C	6 2B	16 3B		
7 GND	14 V_{CC}	7 2C	17 3C		
		8 nc	18 1Y		
		9 2Y	19 1C		
		10 GND	20 V_{CC}		

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

12

TRIPLE 3-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

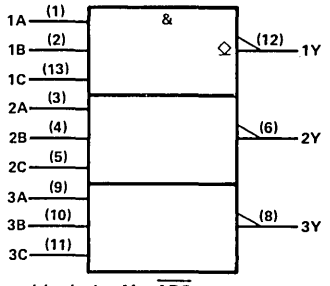
SN5412 (J,FC)
SN54ALS12 (J,FC)
SN54LS12 (J,FC)

SN7412 (J,N)
SN74ALS12 (J,N,FN)
SN74LS12 (J,N)

typical performance

TYPE	POWER	DELAY
'12	10 mW	22 ns
'ALS12	1.27 mW	17.5 ns
'LS12	2 mW	16 ns

logic symbol†



positive logic: $Y = \overline{ABC}$

See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES	
1	1A	8	3Y	1 1A	11 nc
2	1B	9	3A	2 nc	12 3Y
3	2A	10	3B	3 nc	13 nc
4	2B	11	3C	4 1B	14 nc
5	2C	12	1Y	5 2A	15 3A
6	2Y	13	1C	6 2B	16 3B
7	GND	14	V_{CC}	7 2C	17 3C
				8 nc	18 1Y
				9 2Y	19 1C
				10 GND	20 V_{CC}

13

DUAL 4-INPUT POSITIVE-NAND SCHMITT TRIGGERS

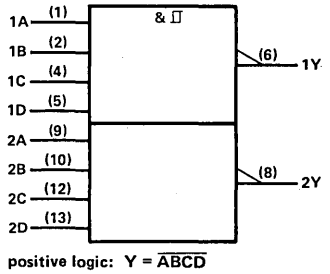
SN5413 (J,FC)
SN54LS13 (J,FC)

SN7413 (J,N)
SN74LS13 (J,N)

typical performance

TYPE	HYSTERESIS	DELAY
'13	0.8 V	16.5 ns
'LS13	0.8 V	16.5 ns

logic symbol†



positive logic: $Y = \overline{ABCD}$

See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES	
1	1A	8	2Y	1 nc	11 nc
2	1B	9	2A	2 nc	12 2Y
3	nc	10	2B	3 1A	13 nc
4	1C	11	nc	4 nc	14 nc
5	1D	12	2C	5 1B	15 2A
6	1Y	13	2D	6 1C	16 2B
7	GND	14	V_{CC}	7 1D	17 2C
				8 nc	18 nc
				9 1Y	19 2D
				10 GND	20 V_{CC}

14

HEX SCHMITT-TRIGGER INVERTERS

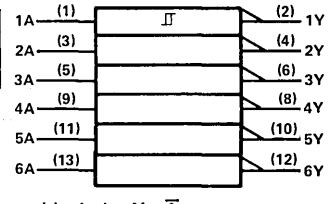
SN5414 (J,FC)
SN54LS14 (J,FC)

SN7414 (J,N)
SN74LS14 (J,N)

typical performance

TYPE	HYSTERESIS	DELAY
'14	0.8 V	15 ns
'LS14	0.8 V	15 ns

logic symbol†



positive logic: $Y = \overline{A}$

See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES	
1	1A	8	4Y	1 1A	11 nc
2	1Y	9	4A	2 nc	12 4Y
3	2A	10	5Y	3 nc	13 nc
4	2Y	11	5A	4 1Y	14 4A
5	3A	12	6Y	5 2A	15 5Y
6	3Y	13	6A	6 2Y	16 5A
7	GND	14	V_{CC}	7 3A	17 6Y
				8 nc	18 nc
				9 3Y	19 6A
				10 GND	20 V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

15

TRIPLE 3-INPUT POSITIVE-AND GATES WITH OPEN-COLLECTOR OUTPUTS

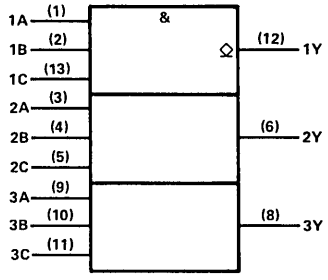
typical performance

TYPE	POWER	DELAY
'ALS15	2.22 mW	15 ns
'H15	38 mW	10.5 ns
'LS15	4.25 mW	15 ns
'S15	28 mW	15 ns

SN54ALS15 (J,FC)
SN54H15 (J,FC)
SN54LS15 (J,FC)
SN54S15 (J,FC)

SN74ALS15 (J,N,FN)
SN74H15 (J,N)
SN74LS15 (J,N)
SN74S15 (J,N,FN)

logic symbol†



positive logic: Y = ABC

See *TTL Data Book*

pin assignments

J, N PACKAGES			
1	1A	8	3Y
2	1B	9	3A
3	2A	10	3B
4	2B	11	3C
5	2C	12	1Y
6	2Y	13	1C
7	GND	14	V_{CC}

FC, FN PACKAGES			
1	1A	11	nc
2	nc	12	3Y
3	nc	13	nc
4	1B	14	nc
5	2A	15	3A
6	2B	16	3B
7	2C	17	3C
8	nc	18	1Y
9	2Y	19	1C
10	GND	20	V_{CC}

16

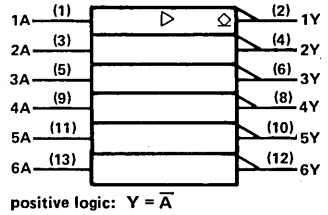
HEX INVERTER BUFFER/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

typical performance

TYPE	HIGH-LEVEL OUTPUT VOLTAGE	LOW-LEVEL OUTPUT CURRENT	TYPICAL DELAY TIME	TYPICAL POWER PER GATE
SN74'	15 V	40 mA	12.5 ns	26 mW
SN54'	15 V	30 mA	12.5 ns	26 mW

SN5416 (J)
SN7416 (J,N)

logic symbol†



positive logic: $Y = \overline{A}$

See *TTL Data Book*

pin assignments

J, N PACKAGES			
1	1A	8	4Y
2	1Y	9	4A
3	2A	10	5Y
4	2Y	11	5A
5	3A	12	6Y
6	3Y	13	6A
7	GND	14	V_{CC}

17

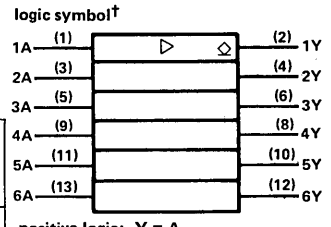
HEX BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

typical performance

TYPE	HIGH-LEVEL OUTPUT VOLTAGE	LOW-LEVEL OUTPUT CURRENT	TYPICAL DELAY TIME	TYPICAL POWER PER GATE
SN74'	15 V	40 mA	13 ns	21 mW
SN54'	15 V	30 mA	13 ns	21 mW

SN5417 (J)
SN7417 (J,N)

logic symbol†



positive logic: Y = A

See *TTL Data Book*

pin assignments

J, N PACKAGES			
1	1A	8	4Y
2	1Y	9	4A
3	2A	10	5Y
4	2Y	11	5A
5	3A	12	6Y
6	3Y	13	6A
7	GND	14	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

18

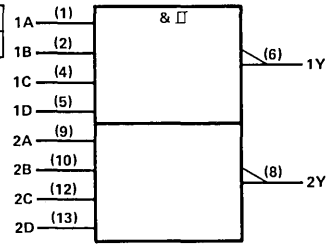
SCHMITT-TRIGGER POSITIVE-NAND GATES WITH TOTEM-POLE OUTPUTS

SN54LS18 (J) SN74LS18 (J,N)

typical performance

TYPE	HYSTERESIS	DELAY
'LS18	0.7 V	25 ns

logic symbol†



positive logic: $Y = \overline{ABCD}$

See *TTL Data Book*

pin assignments

J, N PACKAGES			
1	1A	8	2Y
2	1B	9	2A
3	nc	10	2B
4	1C	11	nc
5	1D	12	2C
6	1Y	13	2D
7	GND	14	V_{CC}

19

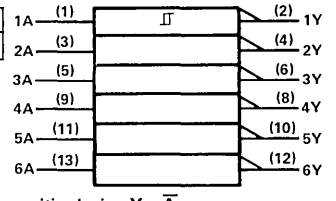
SCHMITT-TRIGGER INVERTERS WITH TOTEM-POLE OUTPUTS

SN54LS19 (J) SN74LS19 (J,N)

typical performance

TYPE	HYSTERESIS	DELAY
'LS19	0.7 V	16 ns

logic symbol†



positive logic: $Y = \overline{A}$

See *TTL Data Book*

pin assignments

J, N PACKAGES			
1	1A	8	4Y
2	1Y	9	4A
3	2A	10	5Y
4	2Y	11	5A
5	3A	12	6Y
6	3Y	13	6A
7	GND	14	V_{CC}

20

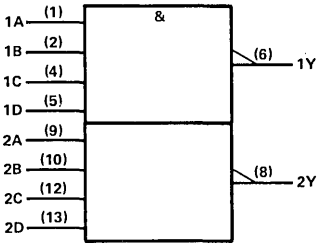
DUAL 4-INPUT POSITIVE-NAND GATES

SN5420 (J,FC) SN7420 (J,N)
SN54ALS20 (J,FC) SN74ALS20 (J,N,FN)
SN54H20 (J,FC) SN74H20 (J,N)
SN54L20 (J)
SN54LS20 (J,FC) SN74LS20 (J,N)
SN54S20 (J,FC) SN74S20 (J,N,FN)

typical performance

TYPE	POWER	DELAY
'20	10 mW	10 ns
'ALS20	1.29 mW	12 ns
'H20	22 mW	6 ns
'L20	1 mW	33 ns
'LS20	2 mW	9.5 ns
'S20	19 mW	3 ns

logic symbol†



positive logic: $Y = \overline{ABCD}$

See *TTL Data Book*

pin assignments

J, N PACKAGES			
1	1A	8	2Y
2	1B	9	2A
3	nc	10	2B
4	1C	11	nc
5	1D	12	2C
6	1Y	13	2D
7	GND	14	V_{CC}

FC, FN PACKAGES			
1	nc	11	nc
2	nc	12	2Y
3	1A	13	nc
4	nc	14	nc
5	1B	15	2A
6	1C	16	2B
7	1D	17	2C
8	nc	18	nc
9	1Y	19	2D
10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

21

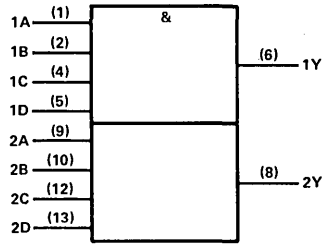
DUAL 4-INPUT POSITIVE-AND GATES

typical performance

TYPE	POWER	DELAY
'ALS21	2.21 mW	8.5 ns
'H21	40 mW	8.2 ns
'LS21	4.25 mW	12 ns

SN54ALS21 (J,FC) SN74ALS21 (J,N,FN)
SN54H21 (J,FC) SN74H21 (J,N)
SN54LS21 (J,FC) SN74LS21 (J,N)

logic symbol†



positive logic: $Y = ABCD$
See *TTL Data Book*

pin assignments

J, N PACKAGES			
1	1A	8	2Y
2	1B	9	2A
3	nc	10	2B
4	1C	11	nc
5	1D	12	2C
6	1Y	13	2D
7	GND	14	V_{CC}

FC, FN PACKAGES			
1	nc	11	nc
2	nc	12	2Y
3	1A	13	nc
4	nc	14	nc
5	1B	15	2A
6	1C	16	2B
7	1D	17	2C
8	nc	18	nc
9	1Y	19	2D
10	GND	20	V_{CC}

22

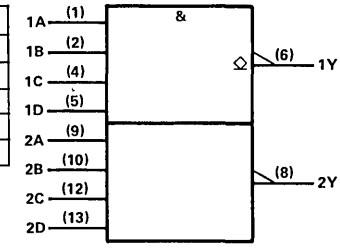
DUAL 4-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

typical performance

TYPE	POWER	DELAY
'22	10 mW	22 ns
'ALS22	1.28 mW	19.5 ns
'H22	22 mW	8 ns
'LS22	2 mW	16 ns
'S22	17.5 mW	5 ns

SN5422 (J,FC) SN7422 (J,N)
SN54ALS22 (J,FC) SN74ALS22 (J,N,FN)
SN54H22 (J,FC) SN74H22 (J,N)
SN54LS22 (J,FC) SN74LS22 (J,N)
SN54S22 (J,FC) SN74S22 (J,N,FN)

logic symbol†



positive logic: $Y = \overline{ABCD}$
See *TTL Data Book*

pin assignments

J, N PACKAGES			
1	1A	8	2Y
2	1B	9	2A
3	nc	10	2B
4	1C	11	nc
5	1D	12	2C
6	1Y	13	2D
7	GND	14	V_{CC}

FC, FN PACKAGES			
1	nc	11	nc
2	nc	12	2Y
3	1A	13	nc
4	nc	14	nc
5	1B	15	2A
6	1C	16	2B
7	1D	17	2C
8	nc	18	nc
9	1Y	19	2D
10	GND	20	V_{CC}

23

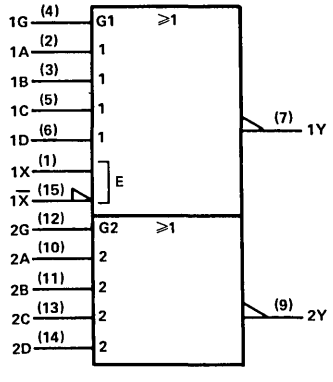
EXPANDABLE DUAL 4-INPUT POSITIVE-NOR GATES WITH STROBE

typical performance

TYPE	POWER	DELAY
'23	23 mW	10.5 ns

SN5423 (J) SN7423 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	1X	9	2Y
2	1A	10	2A
3	1B	11	2B
4	1G	12	2G
5	1C	13	2C
6	1D	14	2D
7	1Y	15	$1\bar{X}$
8	GND	16	V_{CC}

positive logic:
$1Y = \overline{1G\,(1A+1B+1C+1D)+X}$
$2Y = \overline{2G\,(2A+2B+2C+2D)}$
X = output of SN5460/SN7460
See *TTL Data Book*

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

24

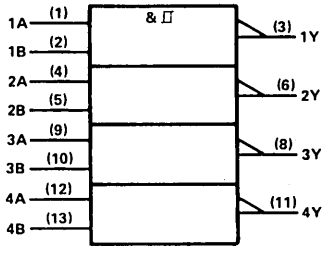
SCHMITT-TRIGGER POSITIVE-NAND GATES/INVERTERS WITH TOTEM POLE OUTPUTS

typical performance

TYPE	HYSTERESIS	DELAY
'LS24	0.7 V	19 ns

SN54LS24 (J) SN74LS24 (J,N)

logic symbol†



positive logic: $Y = \overline{AB}$

See *TTL Data Book*

pin assignments

J, N PACKAGES			
1	1A	8	3Y
2	1B	9	3A
3	1Y	10	3B
4	2A	11	4Y
5	2B	12	4A
6	2Y	13	4B
7	GND	14	V_{CC}

25

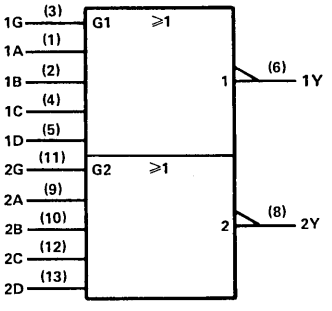
DUAL 4-INPUT POSITIVE-NOR GATES WITH STROBE

typical performance

TYPE	POWER	DELAY
'25	23 mW	10.5 ns

SN5425 (J,FC) SN7425 (J,N)

logic symbol†



positive logic: $Y = \overline{G(A+B+C+D)}$

See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES		
1	1A	8	2Y	1	1A	11	2Y
2	1B	9	2A	2	1B	12	2A
3	1G	10	2B	3	1G	13	nc
4	1C	11	2G	4	nc	14	2B
5	1D	12	2C	5	1C	15	2G
6	1Y	13	2D	6	1D	16	2C
7	GND	14	V_{CC}	7	1Y	17	2D
				8	nc	18	nc
				9	nc	19	nc
				10	GND	20	V_{CC}

26

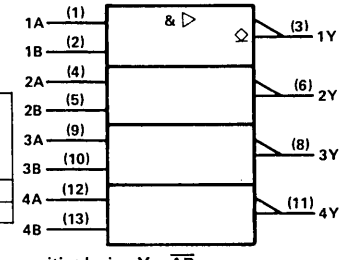
QUADRUPLE 2-INPUT HIGH-VOLTAGE INTERFACE POSITIVE-NAND GATES

typical performance

TYPE	HIGH-LEVEL OUTPUT VOLTAGE	LOW-LEVEL OUTPUT CURRENT	POWER	DELAY
'26	15 V	16 mA	10 mW	13.5 ns
'LS26	15 V	4 mA	2 mW	16 ns

SN5426 (J,FC) SN7426 (J,N)
SN54LS26 (J,FC) SN74LS26 (J,N)

logic symbol†



positive logic: $Y = \overline{AB}$

See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES		
1	1A	8	3Y	1	nc	11	3Y
2	1B	9	3A	2	nc	12	nc
3	1Y	10	3B	3	1A	13	3A
4	2A	11	4Y	4	1B	14	nc
5	2B	12	4A	5	1Y	15	3B
6	2Y	13	4B	6	2A	16	4Y
7	GND	14	V_{CC}	7	2B	17	nc
				8	nc	18	4A
				9	2Y	19	4B
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

27

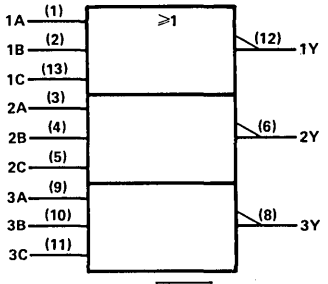
TRIPLE 3-INPUT POSITIVE-NOR GATES

typical performance

TYPE	POWER	DELAY
'27	22 mW	8.5 ns
'ALS27	2.48 mW	6 ns
'LS27	4.5 mW	10 ns

SN5427 (J,FC) SN7427 (J,N)
SN54ALS27 (J,FC) SN74ALS27 (J,N,FN)
SN54LS27 (J,FC) SN74LS27 (J,N)

logic symbol†



positive logic: $Y = \overline{A+B+C}$
See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	1A	8	3Y	1	1A	11	nc
2	1B	9	3A	2	nc	12	3Y
3	2A	10	3B	3	nc	13	nc
4	2B	11	3C	4	1B	14	nc
5	2C	12	1Y	5	2A	15	3A
6	2Y	13	1C	6	2B	16	3B
7	GND	14	V_{CC}	7	2C	17	3C
				8	nc	18	1Y
				9	2Y	19	1C
				10	GND	20	V_{CC}

28

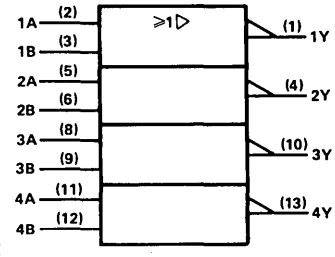
QUADRUPLE 2-INPUT POSITIVE-NOR BUFFERS

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT	POWER	DELAY
'28	48 mA	−2.4 mA	28 mW	7 ns
'ALS28	12 mA	−1 mA	4.06 mW	4 ns
SN54LS'	12 mA	−1.2 mA	5.5 mW	12 ns
SN74LS'	24 mA	−1.2 mA	5.5 mW	12 ns

SN5428 (J,FC) SN7428 (J,N)
SN54ALS28 (J,FC) SN74ALS28 (J,N,FN)
SN54LS28 (J,FC) SN74LS28 (J,N)

logic symbol†



positive logic: $Y = \overline{A+B}$
See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	1Y	8	3A	1	nc	11	3A
2	1A	9	3B	2	1Y	12	nc
3	1B	10	3Y	3	nc	13	3B
4	2Y	11	4A	4	1A	14	nc
5	2A	12	4B	5	1B	15	3Y
6	2B	13	4Y	6	2Y	16	4A
7	GND	14	V_{CC}	7	2A	17	4B
				8	nc	18	nc
				9	2B	19	4Y
				10	GND	20	V_{CC}

30

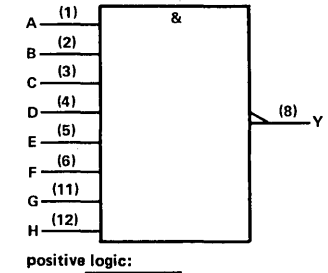
8-INPUT POSITIVE-NAND GATE

typical performance

TYPE	POWER	DELAY
'30	10 mW	10 ns
'ALS30	1.9 mW	7 ns
'H30	22 mW	6 ns
'L30	1 mW	33 ns
'LS30	2.4 mW	17 ns
'S30	19 mW	3 ns

SN5430 (J,FC) SN7430 (J,N)
SN54ALS30 (J,FC) SN74ALS30 (J,N,FN)
SN54H30 (J,FC) SN74H30 (J,N)
SN54L30 (J)
SN54LS30 (J,FC) SN74LS30 (J,N)
SN54S30 (J,FC) SN74S30 (J,N,FN)

logic symbol†



positive logic:
$Y = \overline{ABCDEFGH}$
See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	A	8	Y	1	A	11	nc
2	B	9	nc	2	B	12	Y
3	C	10	nc	3	nc	13	nc
4	D	11	G	4	C	14	nc
5	E	12	H	5	D	15	G
6	F	13	nc	6	E	16	H
7	GND	14	V_{CC}	7	F	17	nc
				8	nc	18	nc
				9	nc	19	nc
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

32

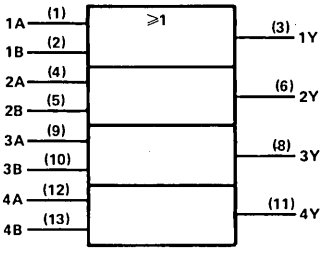
QUADRUPLE 2-INPUT POSITIVE-OR GATE

typical performance

TYPE	POWER	DELAY
'32	24 mW	12 ns
'ALS32	2.81 mW	5.5 ns
'LS32	5 mW	12 ns
'S32	35 mW	4 ns

SN5432 (J,FC) SN7432 (J,N)
SN54ALS32 (J,FC) SN74ALS32 (J,N,FN)
SN54LS32 (J,FC) SN74LS32 (J,N)
SN54S32 (J,FC) SN74S32 (J,N,FN)

logic symbol†



positive logic: $Y = A+B$
See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	1A	8	3Y	1	nc	11	3Y
2	1B	9	3A	2	nc	12	nc
3	1Y	10	3B	3	1A	13	3A
4	2A	11	4Y	4	1B	14	nc
5	2B	12	4A	5	1Y	15	3B
6	2Y	13	4B	6	2A	16	4Y
7	GND	14	V_{CC}	7	2B	17	nc
				8	nc	18	4A
				9	2Y	19	4B
				10	GND	20	V_{CC}

33

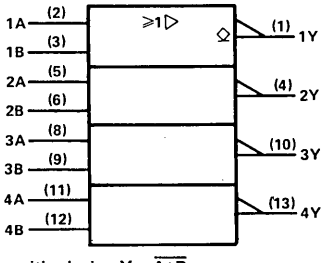
QUADRUPLE 2-INPUT POSITIVE-NOR BUFFERS WITH OPEN-COLLECTOR OUTPUTS

typical performance

TYPE	HIGH-LEVEL OUTPUT VOLTAGE	LOW-LEVEL OUTPUT CURRENT	POWER	DELAY
'33	5.5 V	48 mA	28 mW	11 ns
'ALS33	5.5 V	12 mA	4.06 mW	14.5 ns
SN54LS'	5.5 V	24 mA	5.45 mW	19 ns
SN74LS'	5.5 V	12 mA	5.45 mW	19 ns

SN5433 (J,FC) SN7433 (J,N)
SN54ALS33 (J,FC) SN74ALS33 (J,N)
SN54LS33 (J,FC) SN74LS33 (J,N,FN)

logic symbol†



positive logic: $Y = \overline{A+B}$
See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	1Y	8	3A	1	nc	11	3A
2	1A	9	3B	2	1Y	12	nc
3	1B	10	3Y	3	nc	13	3B
4	2Y	11	4A	4	1A	14	nc
5	2A	12	4B	5	1B	15	3Y
6	2B	13	4Y	6	2Y	16	4A
7	GND	14	V_{CC}	7	2A	17	4B
				8	nc	18	nc
				9	2B	19	4Y
				10	GND	20	V_{CC}

37

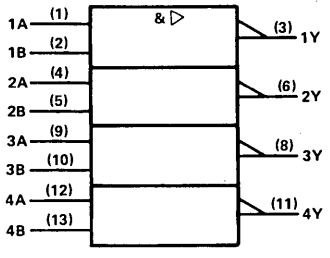
QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT	POWER	DELAY
'37	4.8 mA	−1.2 mA	27 mW	10.5 ns
'ALS37	12 mA	−1 mA	3.04 mW	4 ns
SN54LS'	12 mA	−1.2 mA	4.3 mW	12 ns
SN74LS'	24 mA	−1.2 mA	4.3 mW	12 ns
'S37	60 mA	−3 mA	41 mW	4 ns

SN5437 (J,FC) SN7437 (J,N)
SN54ALS37 (J,FC) SN74ALS37 (J,N,FN)
SN54LS37 (J,FC) SN74LS37 (J,N)
SN54S37 (J,FC) SN74S37 (J,N,FN)

logic symbol†



positive logic: $Y = \overline{AB}$
See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	1A	8	3Y	1	nc	11	3Y
2	1B	9	3A	2	nc	12	nc
3	1Y	10	3B	3	1A	13	3A
4	2A	11	4Y	4	1B	14	nc
5	2B	12	4A	5	1Y	15	3B
6	2Y	13	4B	6	2A	16	4Y
7	GND	14	V_{CC}	7	2B	17	nc
				8	nc	18	4A
				9	2Y	19	4B
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

8

38

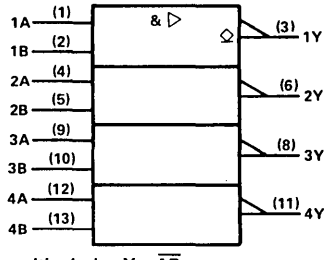
QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS WITH OPEN-COLLECTOR OUTPUTS

typical performance

TYPE	HIGH-LEVEL OUTPUT VOLTAGE	LOW-LEVEL OUTPUT CURRENT	POWER	DELAY
'38	5.5 V	48 mA	24.4 mW	12.5 ns
'ALS38	5.5 V	12 mA	3.04 mW	14.5 ns
SN54LS'	5.5 V	12 mA	4.3 mW	19 ns
SN74LS'	5.5 V	24 mA	4.3 mW	19 ns
'S38	5.5 V	60 mA	41 mW	6.5 ns

SN5438 (J,FC) SN7438 (J,N)
SN54ALS38 (J,FC) SN74ALS38 (J,N,FN)
SN54LS38 (J,FC) SN74LS38 (J,N)
SN54S38 (J,FC) SN74S38 (J,N,FN)

logic symbol†



positive logic: $Y = \overline{AB}$

See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	1A	8	3Y	1	nc	11	3Y
2	1B	9	3A	2	nc	12	nc
3	1Y	10	3B	3	1A	13	3A
4	2A	11	4Y	4	1B	14	nc
5	2B	12	4A	5	1Y	15	3B
6	2Y	13	4B	6	2A	16	4Y
7	GND	14	V_{CC}	7	2B	17	nc
				8	nc	18	4A
				9	2Y	19	4B
				10	GND	20	V_{CC}

40

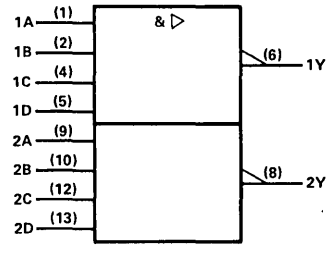
DUAL 4-INPUT POSITIVE-NAND BUFFERS

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT	POWER	DELAY
'40	48 mA	−1.2 mA	26 mW	10.5 ns
'ALS40	12 mA	−1 mA	3.04 mW	4 ns
'H40	60 mA	−1.5 mA	44 mW	7.5 ns
SN54LS'	12 mA	−1.2 mA	4.3 mW	12 ns
SN74LS'	24 mA	−1.2 mA	4.3 mW	12 ns
'S40	60 mA	−3 mA	44 mW	4 ns

SN5440 (J,FC) SN7440 (J,N)
SN54ALS40 (J,FC) SN74ALS40 (J,N,FN)
SN54H40 (J,FC) SN74H40 (J,N)
SN54LS40 (J,FC) SN74LS40 (J,N)
SN54S40 (J,FC) SN74S40 (J,N,FN)

logic symbol†



positive logic: $Y = \overline{ABCD}$

See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	1A	8	2Y	1	nc	11	nc
2	1B	9	2A	2	nc	12	2Y
3	nc	10	2B	3	1A	13	nc
4	1C	11	nc	4	nc	14	nc
5	1D	12	2C	5	1B	15	2A
6	1Y	13	2D	6	1C	16	2B
7	GND	14	V_{CC}	7	1D	17	2C
				8	nc	18	nc
				9	1Y	19	2D
				10	GND	20	V_{CC}

42

4-LINE TO 10-LINE DECODERS

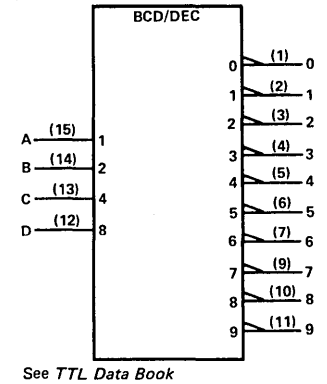
(BCD to decimal)

typical performance

TYPE	SELECT TIME	POWER
'42A	17 ns	140 mW
'L42	34 ns	70 mW
'LS42	17 ns	35 mW

SN5442A (J,FC) SN7442A (J,N)
SN54L42 (J)
SN54LS42 (J,FC) SN74LS42 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	0	9	7	1	0	11	7
2	1	10	8	2	1	12	8
3	2	11	9	3	2	13	nc
4	3	12	D	4	nc	14	9
5	4	13	C	5	3	15	D
6	5	14	B	6	4	16	C
7	6	15	A	7	5	17	B
8	GND	16	V_{CC}	8	nc	18	nc
				9	6	19	A
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

43

4-LINE TO 10-LINE DECODERS (EXCESS 3 TO DECIMAL)

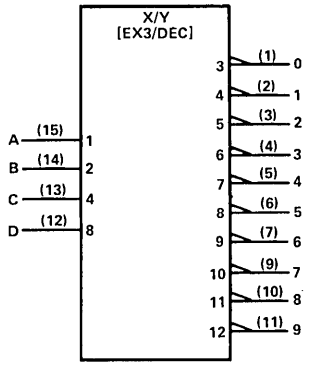
SN5443A (J,FC)
SN54L43 (J)

SN7443A (J,N)

typical performance

TYPE	SELECT TIME	POWER
'43A	17 ns	140 mW
'L43	34 ns	70 mW

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 0	9 7	1 0	11 7
2 1	10 8	2 1	12 8
3 2	11 9	3 2	13 nc
4 3	12 D	4 nc	14 9
5 4	13 C	5 3	15 D
6 5	14 B	6 4	16 C
7 6	15 A	7 5	17 B
8 GND	16 V_{CC}	8 nc	18 nc
		9 6	19 A
		10 GND	20 V_{CC}

44

4-LINE TO 10-LINE DECODERS (EXCESS 3-GRAY TO DECIMAL)

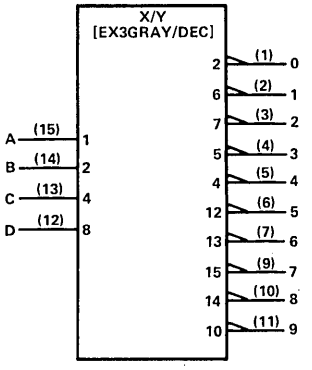
SN5444A (J,FC)
SN54L44 (J)

SN7444A (J,N)

typical performance

TYPE	SELECT TIME	POWER
'44A	17 ns	140 mW
'L44	34 ns	70 mW

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 0	9 7	1 0	11 7
2 1	10 8	2 1	12 8
3 2	11 9	3 2	13 nc
4 3	12 D	4 nc	14 9
5 4	13 C	5 3	15 D
6 5	14 B	6 4	16 C
7 6	15 A	7 5	17 B
8 GND	16 V_{CC}	8 nc	18 nc
		9 6	19 A
		10 GND	20 V_{CC}

45

BCD-TO-DECIMAL DECODER/DRIVER

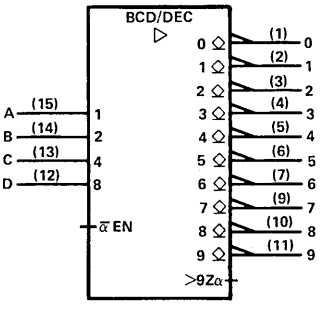
SN5445 (J,FC)

SN7445 (J,N)

typical performance

TYPE	OFF-STATE OUTPUT VOLTAGE	POWER
'45	30 V	215 mW

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 0	9 7	1 0	11 7
2 1	10 8	2 1	12 8
3 2	11 9	3 2	13 nc
4 3	12 D	4 nc	14 9
5 4	13 C	5 3	15 D
6 5	14 B	6 4	16 C
7 6	15 A	7 5	17 B
8 GND	16 V_{CC}	8 nc	18 nc
		9 6	19 A
		10 GND	20 V_{CC}

8

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

46,47

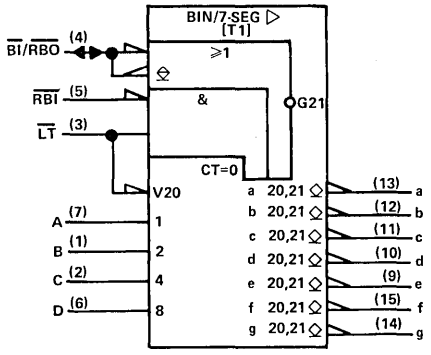
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS
(46 - 30 V OUTPUTS
47 - 15 V OUTPUTS)

typical performance

TYPE	OFF-STATE OUTPUT VOLTAGE	POWER
'46A	30 V	320 mW
'L46	30 V	133 mW
'47A	15 V	320 mW
'L47	15 V	133 mW
'LS47	15 V	35 mW

SN5446A (J,FC) SN7446A (J,N)
SN54L46 (J)
SN5447A (J,FC) SN7447A (J,N)
SN54L47 (J)
SN54LS47 (J,FC) SN74LS47 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	B	9	e	1	B	11	e
2	C	10	d	2	C	12	d
3	$\overline{LT}$	11	c	3	nc	13	nc
4	$\overline{BI}$/$\overline{RBO}$	12	b	4	$\overline{LT}$	14	c
5	$\overline{RBI}$	13	a	5	$\overline{BI}$/$\overline{RBO}$	15	b
6	D	14	g	6	$\overline{RBI}$	16	a
7	A	15	f	7	D	17	g
8	GND	16	V_{CC}	8	nc	18	nc
				9	A	19	f
				10	GND	20	V_{CC}

48

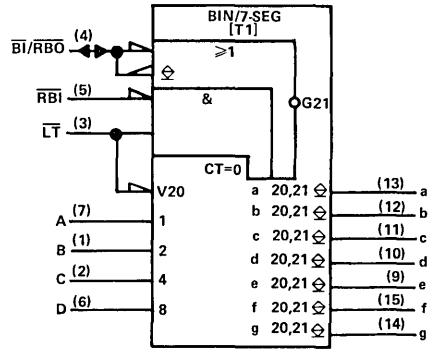
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

typical performance

TYPE	OFF-STATE OUTPUT VOLTAGE	POWER
'48	5.5 V	265 mW
'LS48	5.5 V	125 mW

SN5448 (J,FC) SN7448 (J,N)
SN54LS48 (J,FC) SN74LS48 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	B	9	e	1	B	11	e
2	C	10	d	2	C	12	d
3	$\overline{LT}$	11	c	3	nc	13	nc
4	$\overline{BI}$/$\overline{RBO}$	12	b	4	$\overline{LT}$	14	c
5	$\overline{RBI}$	13	a	5	$\overline{BI}$/$\overline{RBO}$	15	b
6	D	14	g	6	$\overline{RBI}$	16	a
7	A	15	f	7	D	17	g
8	GND	16	V_{CC}	8	nc	18	nc
				9	A	19	f
				10	GND	20	V_{CC}

49

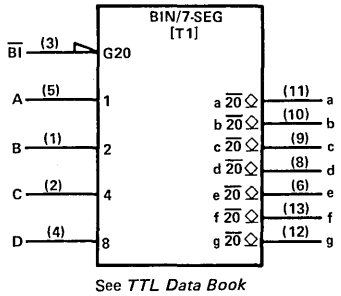
BCD TO SEVEN SEGMENT DECODERS/DRIVERS
(OPEN-COLLECTOR OUTPUTS)

typical performance

TYPE	OFF-STATE OUTPUT VOLTAGE	POWER
'49	5.5 V	165 mW
'LS49	5.5 V	40 mW

SN5449 (J,FC) SN7449 (J,N)
SN54LS49 (J,FC) SN74LS49 (J,N)

logic symbol†



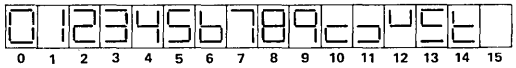
See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	B	8	d	1	B	11	d
2	C	9	c	2	C	12	c
3	$\overline{BI}$	10	b	3	nc	13	nc
4	D	11	a	4	$\overline{BI}$	14	nc
5	A	12	g	5	D	15	b
6	e	13	f	6	A	16	a
7	GND	14	V_{CC}	7	nc	17	g
				8	nc	18	nc
				9	e	19	f
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

FONT TABLE T1 – FOR '46, '47, '48, '49



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

50

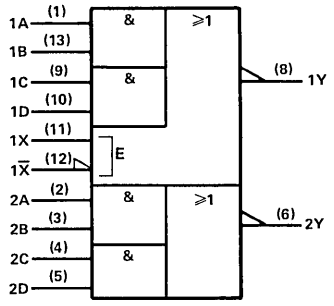
DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATES (ONE GATE EXPANDABLE)

SN5450 (J) SN7450 (J,N)
SN54H50 (J) SN74H50 (J,N)

typical performance

TYPE	POWER	DELAY
'50	14 mW	10.5 ns
'H50	29 mW	6.5 ns

logic symbol†



positive logic: $Y = \overline{AB+CD+X}$
'50: X = output of SN5460/SN7460
'H50: X = output of SN54H60/SN74H60 or SN54H62/SN74H62

pin assignments

J, N PACKAGES			
1	1A	8	1Y
2	2A	9	1C
3	2B	10	1D
4	2C	11	1X
5	2D	12	1X̄
6	2Y	13	1B
7	GND	14	V_{CC}

See *TTL Data Book*

51

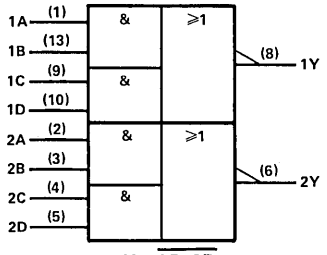
AND-OR INVERT GATES

SN5451 (J,FC) SN7451 (J,N)
SN54H51 (J,FC) SN74H51 (J,N)
SN54L51 (J)
SN54LS51 (J,FC) SN74LS51 (J,N)
SN54S51 (J,FC) SN74S51 (J,N,FN)

typical performance

TYPE	POWER	DELAY
'51	14 mW	10.5 ns
'H51	29 mW	65 ns
'L51	1.5 mW	43 ns
'LS51	2.75 mW	12.5 ns
'S51	28 mW	3.5 ns

logic symbol, '51, 'H51, 'S51†

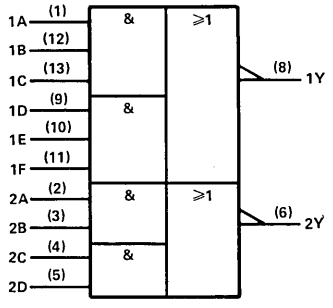


positive logic: $Y = \overline{AB+CD}$

pin assignments, '51, 'H51, 'S51

J, N PACKAGES				FC, FN PACKAGES			
1	1A	8	1Y	1	1A	11	nc
2	2A	9	1C	2	nc	12	1Y
3	2B	10	1D	3	nc	13	nc
4	2C	11	nu	4	2A	14	1C
5	2D	12	nu	5	2B	15	1D
6	2Y	13	1B	6	2C	16	nc
7	GND	14	V_{CC}	7	2D	17	nc
				8	nc	18	nc
				9	2Y	19	1B
				10	GND	20	V_{CC}

logic symbol, 'L51, 'LS51†



positive logic:

$1Y = \overline{(1A \cdot 1B \cdot 1C)+(1D \cdot 1E \cdot 1F)}$

$2Y = \overline{(2A \cdot 2B)+(2C \cdot 2D)}$

pin assignments, 'L51, 'LS51

J, N PACKAGES				FC, FN PACKAGES			
1	1A	8	1Y	1	1A	11	nc
2	2A	9	1D	2	nc	12	1Y
3	2B	10	1E	3	nc	13	nc
4	2C	11	1F	4	2A	14	1D
5	2D	12	1B	5	2B	15	1E
6	2Y	13	1C	6	2C	16	1F
7	GND	14	V_{CC}	7	2D	17	1B
				8	nc	18	nc
				9	2Y	19	1C
				10	GND	20	V_{CC}

See *TTL Data Book*

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.
nu — make no external connection.

52

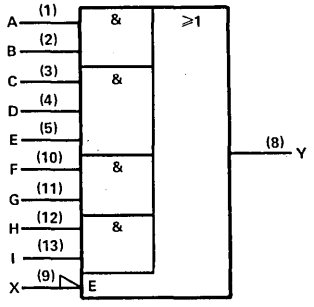
EXPANDABLE 4-WIDE AND-OR GATES

typical performance

TYPE	POWER	DELAY
'H52	88 mW	9.9 ns

SN54H51 (J) SN74H51 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	A	8	Y
2	B	9	X
3	C	10	F
4	D	11	G
5	E	12	H
6	nc	13	I
7	GND	14	V_{CC}

positive logic: $Y = AB+CDE+FG+HI+X$

X = output of SN54H61/SN74H61

See *TTL Data Book*

53

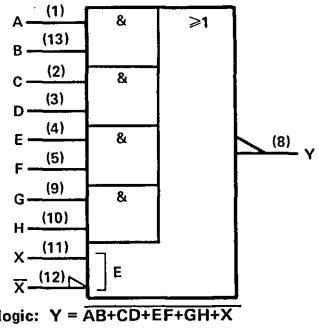
EXPANDABLE 4-WIDE AND-OR-INVERT GATES

typical performance

TYPE	POWER	DELAY
'53	23 mW	10.5 ns
'H53	41 mW	6.6 ns

SN5453 (J) SN7453 (J,N)
SN54H53 (J) SN74H53 (J,N)

logic symbol, '53†



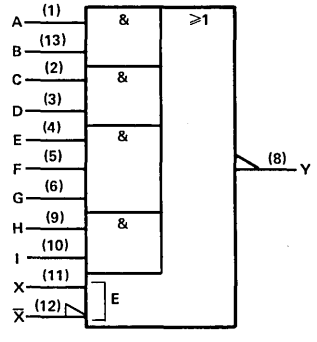
pin assignments, '53

J, N PACKAGES			
1	A	8	Y
2	C	9	G
3	D	10	H
4	E	11	X
5	F	12	$\overline{X}$
6	nc	13	B
7	GND	14	V_{CC}

positive logic: $Y = \overline{AB+CD+EF+GH+X}$

X = output of SN5460/SN7460

logic symbol, 'H53†



pin assignments, 'H53

J, N PACKAGES			
1	A	8	Y
2	C	9	H
3	D	10	I
4	E	11	X
5	F	12	$\overline{X}$
6	G	13	B
7	GND	14	V_{CC}

positive logic: $Y = \overline{AB+CD+EFG+HI+X}$

X = output of SN54H60/SN74H60
or SN54H62/SN74H62

See *TTL Data Book*

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

54

4-WIDE AND-OR-INVERT GATES

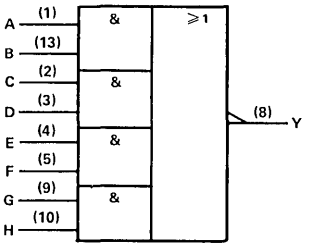
typical performance

TYPE	POWER	DELAY
'54	23 mW	10.5 ns
'H54	41 mW	6.6 ns
'L54	1.5 mW	43 ns
'LS54	4.5 mW	12.5 ns

SN5454 (J,FC)
SN54H54 (J,FC)
SN54L54 (J,FC)
SN54LS54 (J,FC)

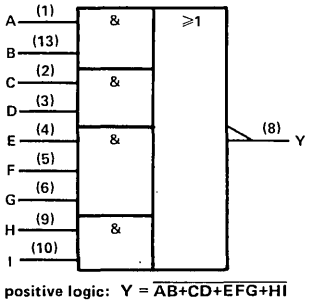
SN7454 (J,N)
SN74H54 (J,N)
SN74LS54 (J,N)

logic symbol, '54†



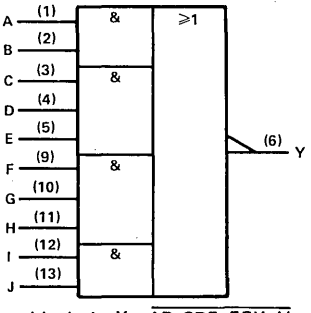
positive logic: $Y = \overline{AB+CD+EF+GH}$

logic symbol, 'H54†



positive logic: $Y = \overline{AB+CD+EFG+HI}$

logic symbol, 'L54, 'LS54†



positive logic: $Y = \overline{AB+CDE+FGH+IJ}$

See *TTL Data Book*

pin assignments, '54

J, N PACKAGES				FC, FN PACKAGES			
1	A	8	Y	1	nc	11	Y
2	C	9	G	2	A	12	G
3	D	10	H	3	nc	13	nc
4	E	11	nu	4	C	14	nc
5	F	12	nu	5	D	15	H
6	nc	13	B	6	E	16	nc
7	GND	14	V_{CC}	7	nc	17	nc
				8	nc	18	nc
				9	F	19	B
				10	GND	20	V_{CC}

pin assignments, 'H54

J, N PACKAGES				FC, FN PACKAGES			
1	A	8	Y	1	nc	11	nc
2	C	9	H	2	A	12	nc
3	D	10	I	3	nc	13	nc
4	E	11	nu	4	C	14	Y
5	F	12	nu	5	D	15	H
6	G	13	B	6	E	16	I
7	GND	14	V_{CC}	7	F	17	nc
				8	nc	18	nc
				9	G	19	B
				10	GND	20	V_{CC}

pin assignments, 'L54, 'LS54

J, N PACKAGES				FC, FN PACKAGES			
1	A	8	nc	1	A	11	nc
2	B	9	F	2	nc	12	nc
3	C	10	G	3	nc	13	nc
4	D	11	H	4	B	14	F
5	E	12	I	5	C	15	G
6	Y	13	J	6	D	16	H
7	GND	14	V_{CC}	7	E	17	I
				8	nc	18	nc
				9	Y	19	J
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.
nu — make no external connection.

55

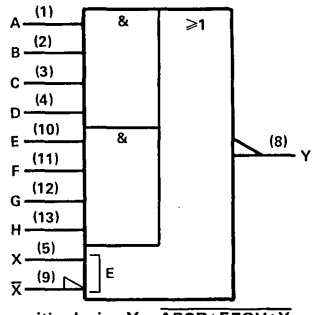
2-WIDE 4-INPUT AND-OR-INVERT GATES

typical performance

TYPE	POWER	DELAY
'H55	30 mW	6.8 ns
'L55	1.5 mW	43 ns
'LS55	2.75 mW	12.5 ns

SN54H55 (J,FC) SN74H55 (J,N)
SN54L55 (J)
SN54LS55 (J,FC) SN74LS55 (J,N)

logic symbol, 'H55†



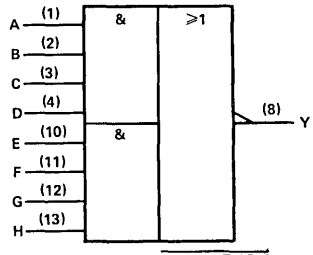
positive logic: $Y = \overline{ABCD+EFGH+X}$

pin assignments, 'H55

J, N PACKAGES				FC, FN PACKAGES			
1	A	8	Y	1	nc	11	nc
2	B	9	$\overline{X}$	2	A	12	Y
3	C	10	E	3	nc	13	nc
4	D	11	F	4	B	14	$\overline{X}$
5	X	12	G	5	C	15	E
6	nc	13	H	6	D	16	F
7	GND	14	V_{CC}	7	nc	17	G
				8	nc	18	nc
				9	X	19	H
				10	GND	20	V_{CC}

X = Output of SN54H60/SN74H60 or SN54H62/SN74H62

logic symbol, 'L55, 'LS55†



positive logic: $Y = \overline{ABCD+EFGH}$

pin assignments, 'L55, 'LS55

J, N PACKAGES				FC, FN PACKAGES			
1	A	8	Y	1	A	11	nc
2	B	9	nc	2	B	12	Y
3	C	10	E	3	nc	13	nc
4	D	11	F	4	nc	14	nc
5	nc	12	G	5	nc	15	E
6	nc	13	H	6	C	16	F
7	GND	14	V_{CC}	7	D	17	G
				8	nc	18	nc
				9	nc	19	H
				10	GND	20	V_{CC}

See *TTL Data Book*

60

DUAL 4-INPUT EXPANDERS

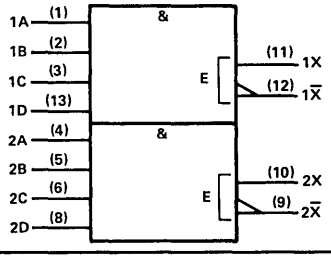
typical performance

TYPE	POWER
'60	4 mW
'H60	6 mW

SN5460 (J) SN7460 (J,N)
SN54H60 (J) SN74H60 (J,N)

'60 positive logic:
X = ABCD when connected to X and $\overline{X}$ inputs of SN5423/SN7423, SN5450/SN7450, or SN5453/SN7453
'H60 positive logic:
X = ABCD when connected to X and $\overline{X}$ inputs of SN54H50/SN74H50, SN54H53/SN74H53, or SN54H55/SN74H55

logic symbol†



pin assignments

J, N PACKAGES			
1	1A	8	2D
2	1B	9	$2\overline{X}$
3	1C	10	2X
4	2A	11	1X
5	2B	12	$1\overline{X}$
6	2C	13	1D
7	GND	14	V_{CC}

See *TTL Data Book*

61

TRIPLE 3-INPUT EXPANDERS

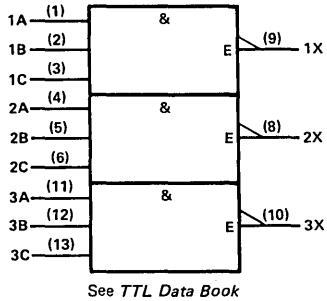
typical performance

TYPE	POWER
'H61	13 mW

SN54H61 (J) SN74H61 (J,N)

positive logic:
X = ABC when connected to X input of SN54H52/SN74H52

logic symbol†



pin assignments

J, N PACKAGES			
1	1A	8	2X
2	1B	9	1X
3	1C	10	3X
4	2A	11	3A
5	2B	12	3B
6	2C	13	3C
7	GND	14	V_{CC}

See *TTL Data Book*

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

62

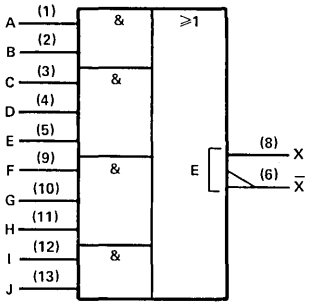
4-WIDE AND-OR EXPANDERS

typical performance

TYPE	POWER
'H62	25 mW

SN54H62 (J) SN74H62 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	A	8	X
2	B	9	F
3	C	10	G
4	D	11	H
5	E	12	I
6	$\overline{X}$	13	J
7	GND	14	V_{CC}

See *TTL Data Book*

63

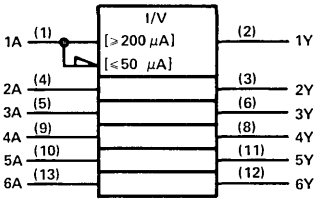
HEX CURRENT-SENSING INTERFACE GATES

typical performance

TYPE	POWER	DELAY
'LS63	3.3 mW	21 ns

SN54LS63 (J,FC) SN74LS63 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES			
1	1A	8	4Y
2	1Y	9	4A
3	2Y	10	5A
4	2A	11	5Y
5	3A	12	6Y
6	3Y	13	6A
7	GND	14	V_{CC}

FC, FN PACKAGES			
1	nc	11	nc
2	1A	12	4Y
3	nc	13	nc
4	1Y	14	4A
5	2Y	15	5A
6	2A	16	5Y
7	3A	17	6Y
8	nc	18	nc
9	3Y	19	6A
10	GND	20	V_{CC}

64,65

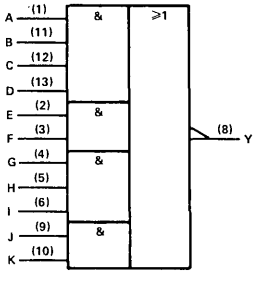
4-2-3-2 INPUT AND-OR-INVERT GATES

typical performance

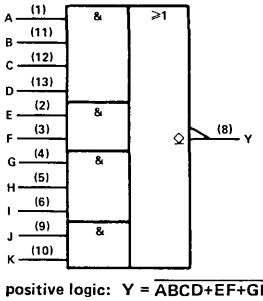
TYPE	OUTPUT	POWER	DELAY
'S64	TOTEM POLE	29 mW	3.5 ns
'S65	OPEN-COLLECTOR	36 mW	5.5 ns

SN54S64 (J,FC) SN74S64 (J,N,FN)
SN54S65 (J,FC) SN74S65 (J,N,FN)

logic symbol, 'S64†



logic symbol, 'S65†



positive logic: $Y = \overline{ABCD+EF+GHI+JK}$

See *TTL Data Book*

pin assignments

J, N PACKAGES			
1	A	8	Y
2	E	9	J
3	F	10	K
4	G	11	B
5	H	12	C
6	I	13	D
7	GND	14	V_{CC}

FC, FN PACKAGES			
1	A	11	Y
2	nc	12	nc
3	nc	13	nc
4	E	14	J
5	F	15	K
6	G	16	B
7	H	17	C
8	nc	18	nc
9	I	19	D
10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

70

AND-GATED J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS

typical performance

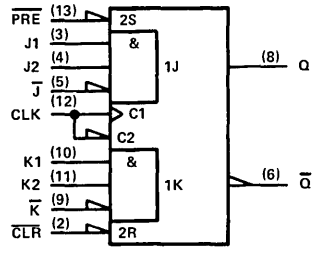
TYPE	f_{max}	PWR/FF	SET-UP	HOLD
'70	35 MHz	65 mW	20 ns↑	5 ns↑

↑ Rising edge of clock pulse.
↓ Falling edge of clock pulse.

SN5470 (J) SN7470 (J,N)

See *TTL Data Book*

logic symbol†



positive logic: $J = J1 \cdot J2 \cdot \overline{J}$
$K = K1 \cdot K2 \cdot \overline{K}$
If inputs J and K are not used, they must be grounded.
Preset or clear function can occur only when the clock input is low.

pin assignments

J, N PACKAGES			
1	nc	8	Q
2	$\overline{CLR}$	9	$\overline{K}$
3	J1	10	K1
4	J2	11	K2
5	$\overline{J}$	12	CLK
6	$\overline{Q}$	13	$\overline{PRE}$
7	GND	14	V_{CC}

71

'H71: AND-OR-GATED J-K MASTER-SLAVE FLIP-FLOPS WITH PRESET

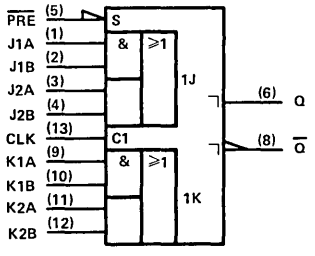
typical performance

TYPE	f_{max}	PWR/FF	SET-UP	HOLD
'H71	30 MHz	80 mW	0 ns↑	0 ns↓
'L71	30 MHz	3.8 mW	0 ns↑	0 ns↓

↑ Rising edge of clock pulse.
↓ Falling edge of clock pulse.

SN54H71 (J) SN74H71 (J,N)

logic symbol, 'H71†



positive logic: $J = (J1A \cdot J1B) + (J2A \cdot J2B)$
$K = (K1A \cdot K1B) + (K2A \cdot K2B)$

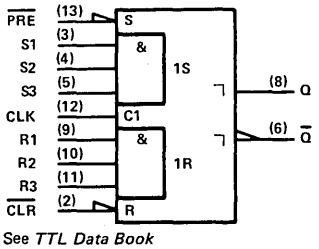
pin assignments, 'H71

J, N PACKAGES			
1	J1A	8	$\overline{Q}$
2	J1B	9	K1A
3	J2A	10	K1B
4	J2B	11	K2A
5	$\overline{PRE}$	12	K2B
6	Q	13	CLK
7	GND	14	V_{CC}

'L71: AND-GATED R-S MASTER-SLAVE FLIP-FLOPS WITH PRESET AND CLEAR

SN54L71 (J)

logic symbol, 'L71†



See *TTL Data Book*

positive logic: $R = R1 \cdot R2 \cdot R3$
$S = S1 \cdot S2 \cdot S3$

pin assignments, 'L71

J, N PACKAGES			
1	nc	8	Q
2	$\overline{CLR}$	9	R1
3	S1	10	R2
4	S2	11	R3
5	S3	12	CLK
6	$\overline{Q}$	13	$\overline{PRE}$
7	GND	14	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

72

AND-GATED J-K MASTER-SLAVE FLIP-FLOPS WITH PRESET AND CLEAR

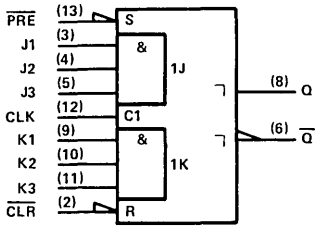
typical performance

TYPE	f_{max}	PWR/ FF	SET-UP	HOLD
'72	20 MHz	50 mW	0 ns↑	0 ns↓
'H72	30 MHz	80 mW	0 ns↑	0 ns↓
'L72	3 MHz	3.8 mW	0 ns↑	0 ns↓

↑ Rising edge of clock pulse.
↓ Falling edge of clock pulse.

SN5472 (J,FC)
SN54H72 (J,FC)
SN54L72 (J)
SN7472 (J,N)
SN74H72 (J,N)

logic symbol†



positive logic: J = J1·J2·J3; K1·K2·K3

See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	nc	8	Q	1	nc	11	nc
2	$\overline{CLR}$	9	K1	2	$\overline{CLR}$	12	Q
3	J1	10	K2	3	nc	13	nc
4	J2	11	K3	4	nc	14	K1
5	J3	12	CLK	5	J1	15	K2
6	$\overline{Q}$	13	$\overline{PRE}$	6	J2	16	K3
7	GND	14	V_{CC}	7	J3	17	CLK
				8	nc	18	nc
				9	$\overline{Q}$	19	$\overline{PRE}$
				10	GND	20	V_{CC}

73

DUAL J-K FLIP-FLOPS WITH CLEAR

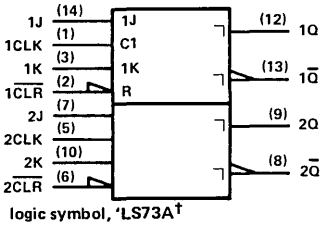
typical performance

TYPE	f_{max}	PWR/ F-F	SET-UP	HOLD
'73	20 MHz	5 mW	0 ns↑	0 ns↓
'H73	30 MHz	80 mW	0 ns↑	0 ns↓
'L73	3 MHz	3.8 mW	0 ns↑	0 ns↓
'LS73A	45 MHz	10 mW	20 ns↓	0 ns↓

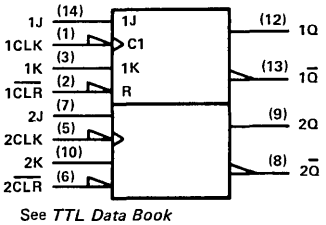
↑ Rising edge of clock pulse.
↓ Falling edge of clock pulse.

SN5473 (J,FC)
SN54H73 (J,FC)
SN54L73 (J)
SN54LS73A (J,FC)
SN7473 (J,N)
SN74H73 (J,N)
SN74LS73A (J,N)

logic symbol' '73, 'H73, 'L73†



logic symbol, 'LS73A†



See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	1CLK	8	2Q̄	1	nc	11	1Q
2	1CLR	9	2Q	2	2CLK	12	1Q̄
3	1K	10	2K	3	nc	13	nc
4	V_{CC}	11	GND	4	2CLR	14	nc
5	2CLK	12	1Q	5	2J	15	1J
6	2CLR	13	1Q̄	6	2Q̄	16	1CLK
7	2J	14	1J	7	2Q	17	1CLR
				8	nc	18	nc
				9	2K	19	1K
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

74

DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

typical performance

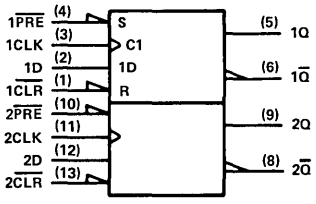
TYPE	f_{max}	PWR/ F-F	SET-UP	HOLD
'74	25 MHz	43 mW	20 ns†	5 ns†
'ALS74	50 MHz	6 mW	15 ns†	0 ns†
'H74	43 MHz	75 mW	15 ns†	5 ns†
'L74	3 MHz	4 mW	50 ns†	15 ns†
'LS74A	33 MHz	10 mW	20 ns†	5 ns†
'S74	110 MHz	75 mW	3 ns†	2 ns†

† Rising edge of clock pulse.

SN5474 (J,FC)
SN54ALS74 (J,FC)
SN54H74 (J,FC)
SN54L74 (J)
SN54LS74A (J,FC)
SN54S74 (J,FC)

SN7474 (J,N)
SN74ALS74 (J,N,FN)
SN74H74 (J,N)
SN74LS74A (J,N)
SN74S74 (J,N,FN)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	1CLR	8	2Q̄	1	nc	11	2Q̄
2	1D	9	2Q	2	1CLR	12	2Q
3	1CLK	10	2PRE	3	1D	13	nc
4	1PRE	11	2CLK	4	nc	14	nc
5	1Q	12	2D	5	1CLK	15	2PRE
6	1Q̄	13	2CLR	6	1PRE	16	2CLK
7	GND	14	V_{CC}	7	1Q	17	2D
				8	nc	18	nc
				9	1Q̄	19	2CLR
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

75

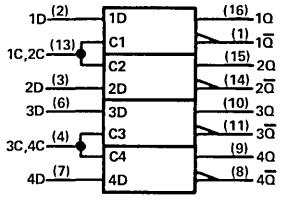
4-BIT BISTABLE LATCHES

typical performance

TYPE	OUTPUTS	DELAY	TOTAL POWER
'75	Q,$\overline{Q}$	15 ns	160 mW
'L75	Q,$\overline{Q}$	30 ns	80 mW
'LS75	Q,$\overline{Q}$	11 ns	32 mW

SN5475 (J,FC) SN7475 (J,N)
SN54L75 (J)
SN54LS75 (J,FC) SN74LS75 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	1Q̄	9	4Q	1	nc	11	1C,2C
2	1D	10	3Q	2	3D	12	2Q̄
3	2D	11	3Q̄	3	nc	13	nc
4	3C,4C	12	GND	4	4D	14	2Q
5	V_{CC}	13	1C,2C	5	4Q̄	15	1Q
6	3D	14	2Q̄	6	4Q	16	1Q̄
7	4D	15	2Q	7	3Q	17	1D
8	4Q̄	16	1Q	8	nc	18	2D
				9	3Q̄	19	3C,4C
				10	GND	20	V_{CC}

76

DUAL J-K FLIP-FLOPS WITH PRESET AND CLEAR

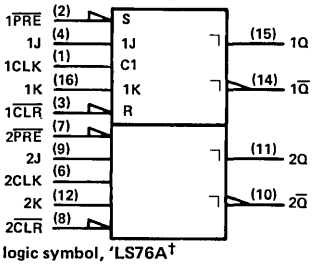
typical performance

TYPE	f_{max}	PWR/F-F	SET-UP	HOLD
'76	20 MHz	50 mW	0 ns↑	0 ns↓
'H76	30 MHz	80 mW	0 ns↑	0 ns↓
'LS76A	45 MHz	10 mW	20 ns↓	0 ns↓

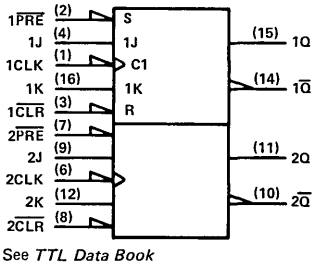
↑ Rising edge of clock pulse.
↓ Falling edge of clock pulse.

SN5476 (J,FC) SN7476 (J,N)
SN54H76 (J,FC) SN74H76 (J,N)
SN54LS76A (J,FC) SN74LS76A (J,N)

logic symbol, '76, 'H76†



logic symbol, 'LS76A†



See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	1CLK	9	2J	1	2CLK	11	1Q̄
2	1PRE	10	2Q̄	2	2PRE	12	1Q
3	1CLR	11	2Q	3	nc	13	nc
4	1J	12	2K	4	2CLR	14	1K
5	V_{CC}	13	GND	5	2J	15	1CLK
6	2CLK	14	1Q̄	6	2Q̄	16	1PRE
7	2PRE	15	1Q	7	2Q	17	1CLR
8	2CLR	16	1K	8	nc	18	nc
				9	2K	19	1J
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

77

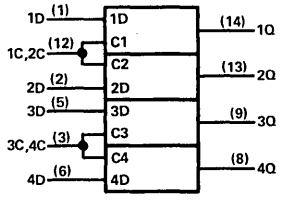
4-BIT BISTABLE LATCHES

typical performance

TYPE	OUTPUTS	DELAY	TOTAL POWER
'77	Q	15 ns	160 mW
'L77	Q	30 ns	80 mW
'LS77	Q	10 ns	35 mW

SN5477 (J,FC)
SN54L77 (J)
SN54LS77 (J,FC)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	1D	8	4Q	1	1D	11	4Q
2	2D	9	3Q	2	2D	12	3Q
3	3C,4C	10	nc	3	nc	13	nc
4	V_{CC}	11	GND	4	nc	14	nc
5	3D	12	1C,2C	5	nc	15	GND
6	4D	13	2Q	6	3C,4C	16	1C,2C
7	nc	14	1Q	7	V_{CC}	17	nc
				8	3D	18	nc
				9	4D	19	2Q
				10	nc	20	1Q

78

DUAL J-K FLIP-FLOPS WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

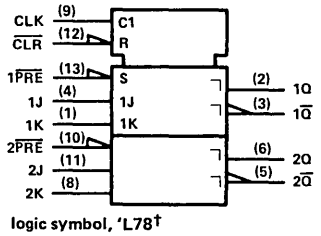
typical performance

TYPE	f_{max}	PWR/F-F	SET-UP	HOLD
'H78	30 MHz	80 mW	0 ns↑	0 ns↓
'L78	3 MHz	3.8 mW	0 ns↑	0 ns↓
'LS78A	45 MHz	10 mW	20 ns↓	0 ns↓

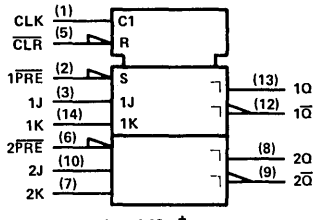
↑ Rising edge of clock pulse.
↓ Falling edge of clock pulse.

SN54H78 (J) SN74H78 (J,N)
SN54L78 (J)
SN54LS78A (J,FC) SN74LS78A (J,N)

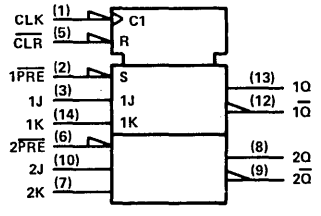
logic symbol, 'H78†



logic symbol, 'L78†



logic symbol, 'LS78A†



See *TTL Data Book*

pin assignments, 'H78

J, N PACKAGES			
1	1K	8	2K
2	1Q	9	CLK
3	1Q̄	10	2PRĒ
4	1J	11	2J
5	2Q̄	12	CLR̄
6	2Q	13	1PRĒ
7	GND	14	V_{CC}

pin assignments, 'L78, 'LS78A

J, N PACKAGES				FC, FN PACKAGES			
1	CLK	8	2Q	1	CLR̄	11	1Q̄
2	1PRĒ	9	2Q̄	2	2PRĒ	12	1Q
3	1J	10	2J	3	nc	13	nc
4	V_{CC}	11	GND	4	nc	14	nc
5	CLR̄	12	1Q̄	5	2K	15	1K
6	2PRĒ	13	1Q	6	2Q	16	CLK
7	2K	14	1K	7	2Q̄	17	1PRĒ
				8	nc	18	nc
				9	2J	19	1J
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc – no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

80

GATED FULL ADDERS

typical performance

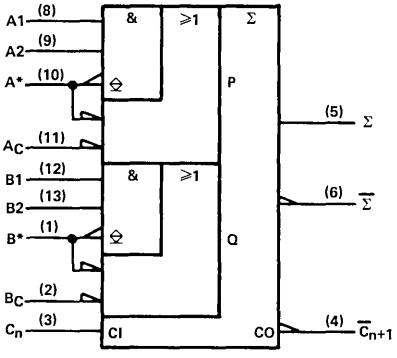
TYPE	CARRY TIME	ADD TIME	POWER PER BIT
'80	10.5 ns	52 ns	105 mW

SN5480 (J) SN7480 (J,N)

NOTES: 1. $A = \overline{A_C} + \overline{A^*} + A1 \cdot A2$, $B = \overline{B_C} + \overline{B^*} + B1 \cdot B2$

2. When A* is used as an input, A1 or A2 must be low. When B* is used as an input, B1 or B2 must be low.
3. When A1 and A2 or B1 and B2 are used as inputs, A* or B*, respectively, must be open or used to perform dot-AND logic.

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES			
1	B*	8	A1
2	B_C	9	A2
3	C_n	10	A*
4	$\overline{C}_{n+1}$	11	A_C
5	Σ	12	B1
6	$\overline{\Sigma}$	13	B2
7	GND	14	V_{CC}

81

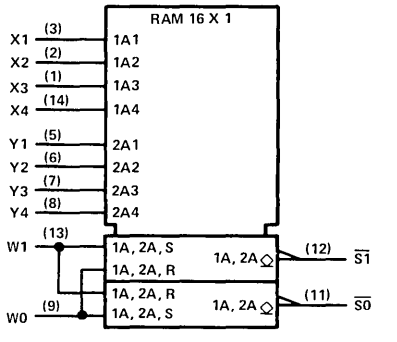
16-BIT RANDOM-ACCESS MEMORIES

typical performance

TYPE	ADDRESS TIME	ENABLE TIME	POWER PER BIT
'81A	15 ns	15 ns	14 mW

SN5481A (J) SN7481A (J,N)

logic symbol†



See Page 2-35

pin assignments

J, N PACKAGES			
1	X3	8	Y4
2	X2	9	W0
3	X1	10	GND
4	V_{CC}	11	$\overline{S0}$
5	Y1	12	$\overline{S1}$
6	Y2	13	W1
7	Y3	14	X4

82

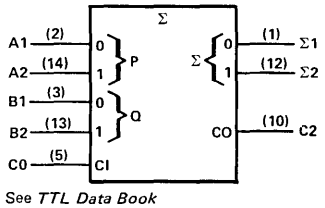
2-BIT BINARY FULL ADDERS

typical performance

TYPE	CARRY TIME	ADD TIME	POWER PER BIT
'82	14.5 ns	25 ns	87 mW

SN5482 (J) SN7482 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES			
1	Σ1	8	nc
2	A1	9	nc
3	B1	10	C2
4	V_{CC}	11	GND
5	C0	12	Σ2
6	nc	13	B2
7	nc	14	A2

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

8

83

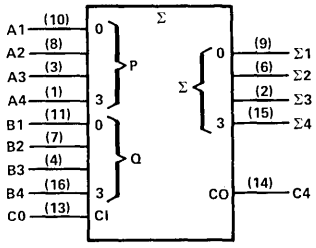
4-BIT BINARY FULL ADDERS WITH FAST CARRY

typical performance

TYPE	CARRY TIME	ADD TIME	POWER PER BIT
'83A	10 ns	16 ns	76 mW
'LS83A	10 ns	15 ns	24 mW

SN5483A (J,FC) SN7483A (J,N)
SN54LS83A (J,FC) SN74LS83A (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	A4	9	Σ1	1	Σ2	11	C0
2	Σ3	10	A1	2	B2	12	C4
3	A3	11	B1	3	nc	13	Σ4
4	B3	12	GND	4	nc	14	B4
5	V_{CC}	13	C0	5	A2	15	A4
6	Σ2	14	C4	6	Σ1	16	Σ3
7	B2	15	Σ4	7	A1	17	A3
8	A2	16	B4	8	nc	18	nc
				9	B1	19	B3
				10	GND	20	V_{CC}

84

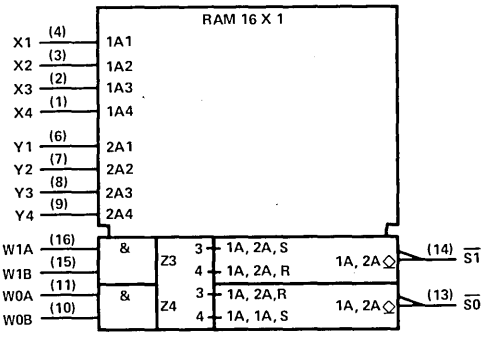
16-BIT RANDOM-ACCESS MEMORIES

typical performance

TYPE	ADDRESS TIME	ENABLE TIME	POWER PER BIT
'84A	15 ns	15 ns	14 mW

SN5484A (J) SN7484A (J,N)

logic symbol†



See Page 2-35

pin assignments

J, N PACKAGES			
1	X4	9	Y4
2	X3	10	W0B
3	X2	11	W0A
4	X1	12	GND
5	V_{CC}	13	$\overline{S0}$
6	Y1	14	$\overline{S1}$
7	Y2	15	W1B
8	Y3	16	W1A

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

85

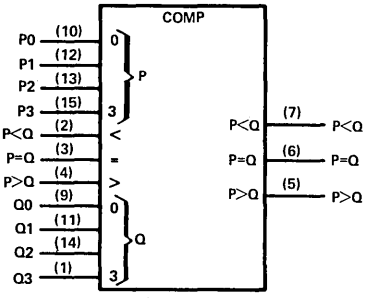
4-BIT MAGNITUDE COMPARATORS

typical performance

TYPE	COMPARE TIME	POWER
'85	21 ns	275 mW
'L85	82 ns	20 mW
'LS85	23.5 ns	52 mW
'S85	11.5 ns	365 mW

SN5485 (J,FC) SN7485 (J,N)
SN54L85 (J)
SN54LS85 (J,FC) SN74LS85 (J,N)
SN54S85 (J,FC) SN74S85 (J,N,FN)

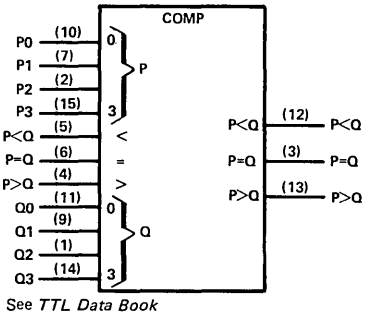
logic symbol, '85, 'LS85, 'S85†



pin assignments, '85, 'LS85, 'S85

J, N PACKAGES		FC, FN PACKAGES	
1 Q3	9 Q0	1 Q3	11 Q0
2 P<Qin	10 P0	2 P<Qin	12 P0
3 P=Qin	11 Q1	3 nc	13 nc
4 P>Qin	12 P1	4 P=Qin	14 Q1
5 P>Qout	13 P2	5 P>Qin	15 P1
6 P=Qout	14 Q2	6 P>Qout	16 P2
7 P<Qout	15 P3	7 P=Qout	17 Q2
8 GND	16 V_{CC}	8 nc	18 nc
		9 P<Qout	19 P3
		10 GND	20 V_{CC}

logic symbol, 'L85†



pin assignments, 'L85

J, N PACKAGES	
1 Q2	9 Q1
2 P2	10 P0
3 P=Qout	11 Q0
4 P>Qin	12 P<Qout
5 P<Qin	13 P>Qout
6 P=Qin	14 Q3
7 P1	15 P3
8 GND	16 V_{CC}

See *TTL Data Book*

86

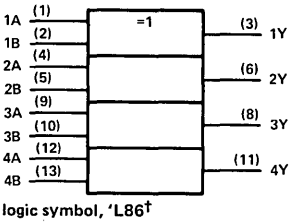
QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

typical performance

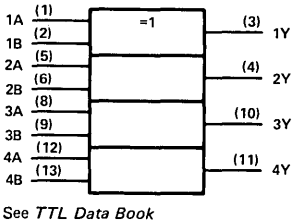
TYPE	POWER	DELAY
'86	150 mW	14 ns
'L86	15 mW	55 ns
'LS86	30 mW	10 ns
'S86	250 mW	7 ns

SN5486 (J,FC) SN7486 (J,N)
SN54L86 (J)
SN54LS86 (J,FC) SN74LS86 (J,N)
SN54S86 (J,FC) SN74S86 (J,N,FN)

logic symbol, '86, 'LS86, 'S86†



logic symbol, 'L86†



See *TTL Data Book*

positive logic: $Y = A \oplus B = \bar{A}B + A\bar{B}$

pin assignments, '86, 'LS86, 'S86

J, N PACKAGES		FC, FN PACKAGES	
1 1A	8	1 nc	11 3Y
2 1B	9 3A	2 nc	12 nc
3 1Y	10 3B	3 1A	13 3A
4 2A	11 4Y	4 1B	14 nc
5 2B	12 4A	5 1Y	15 3B
6 2Y	13 4B	6 2A	16 4Y
7 GND	14 V_{CC}	7 2B	17 nc
		8 nc	18 4A
		9 2Y	19 4B
		10 GND	20 V_{CC}

pin assignments, 'L86

J, N PACKAGES	
1 1A	8 3A
2 1B	9 3B
3 1Y	10 3Y
4 2Y	11 4Y
5 2A	12 4A
6 2B	13 4B
7 GND	14 V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

87

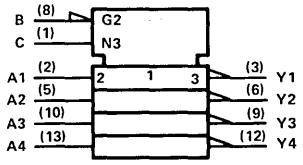
4-BIT TRUE/ COMPLEMENT, ZERO/ONE ELEMENTS

SN54H87 (J) SN74H87 (J,N)

typical performance

TYPE	POWER	DELAY
'H87	270 mW	14 ns

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES			
1	C	8	B
2	A1	9	Y3
3	Y1	10	A3
4	nc	11	nc
5	A2	12	Y4
6	Y2	13	A4
7	GND	14	V_{CC}

88 §

256-BIT READ-ONLY MEMORIES

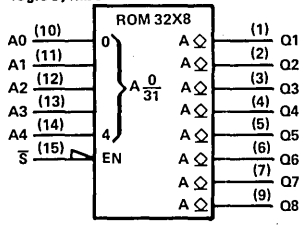
typical performance

TYPE	ADDRESS TIME	ENABLE TIME	POWER PER BIT
'88A	26 ns	22 ns	1.1 mW

SN5488A (J,FC) SN7488A (J,N)

§ For more information on these devices, contact the factory

logic symbol†



pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	Q1	9	Q8	1	Q1	11	Q8
2	Q2	10	A0	2	Q2	12	A0
3	Q3	11	A1	3	nc	13	nc
4	Q4	12	A2	4	Q3	14	A1
5	Q5	13	A3	5	Q4	15	A2
6	Q6	14	A4	6	Q5	16	A3
7	Q7	15	S̄	7	Q6	17	A4
8	GND	16	V_{CC}	8	nc	18	nc
				9	Q7	19	S̄
				10	GND	20	V_{CC}

89

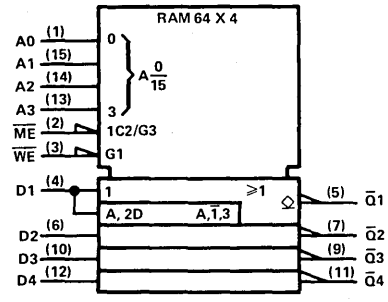
64-BIT READ/WRITE MEMORIES

typical performance

TYPE	ADDRESS TIME	ENABLE TIME	POWER PER BIT
'89	32 ns	30 ns	5.9 mW

SN7489 (J,N)

logic symbol†



See Page 2-41

pin assignments

J, N PACKAGES			
1	A0	9	Q̄3
2	ME	10	D3
3	WE	11	Q̄4
4	D1	12	D4
5	Q̄1	13	A3
6	D2	14	A2
7	Q̄2	15	A1
8	GND	16	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

90

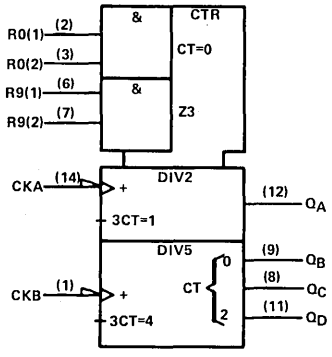
DECADE COUNTERS

typical performance

TYPE	COUNT FREQUENCY	CLEAR	TOTAL POWER
'90A	32 MHz	HIGH	160 mW
'L90	3 MHz	HIGH	20 mW
'LS90	32 MHz	HIGH	40 mW

SN5490A (J,FC) SN7490A (J,N)
SN54L90 (J)
SN54LS90 (J,FC) SN74LS90 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	CKB	8	QC	1	nc	11	QD
2	R0(1)	9	QB	2	nc	12	QA
3	R0(2)	10	GND	3	nc	13	nc
4	nc	11	QD	4	nc	14	nc
5	V_{CC}	12	QA	5	R9(1)	15	CKA
6	R9(1)	13	nc	6	R9(2)	16	CKB
7	R9(2)	14	CKA	7	QC	17	R0(1)
				8	nc	18	nc
				9	QB	19	R0(2)
				10	GND	20	V_{CC}

91

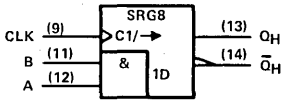
8-BIT SHIFT REGISTERS

typical performance

TYPE	SHIFT FREQUENCY	SERIAL DATA INPUT	TOTAL POWER
'91A	10 MHz	GATED D	175 mW
'L91	3 MHz	GATED D	17.5 mW
'LS91	25 MHz	GATED D	60 mW

SN5491A (J,FC) SN7491A (J,N)
SN54L91 (J)
SN54LS91 (J,FC) SN74LS91 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	nc	8	nc	1	nc	11	B
2	nc	9	CLK	2	nc	12	A
3	nc	10	GND	3	nc	13	nc
4	nc	11	B	4	nc	14	nc
5	V_{CC}	12	A	5	nc	15	QH
6	nc	13	QH	6	nc	16	$\overline{Q}H$
7	nc	14	$\overline{Q}H$	7	CLK	17	nc
				8	nc	18	nc
				9	nc	19	nc
				10	GND	20	V_{CC}

92

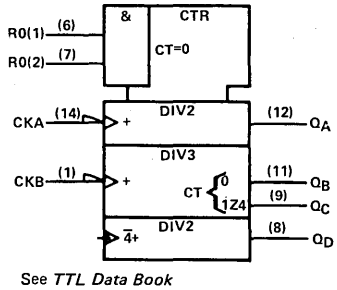
DIVIDE-BY-12 COUNTERS

typical performance

TYPE	COUNT FREQUENCY	CLEAR	TOTAL POWER
'92A	32 MHz	HIGH	160 mW
'LS92	32 MHz	HIGH	39 mW

SN5492A (J,FC) SN7492A (J,N)
SN54LS92 (J,FC) SN74LS92 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	CKB	8	QD	1	nc	11	QB
2	nc	9	QC	2	R0(1)	12	QA
3	nc	10	GND	3	nc	13	nc
4	nc	11	QB	4	nc	14	nc
5	V_{CC}	12	QA	5	R0(2)	15	nc
6	R0(1)	13	nc	6	QD	16	CKA
7	R0(2)	14	CKA	7	QC	17	CKB
				8	nc	18	nc
				9	nc	19	nc
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

93

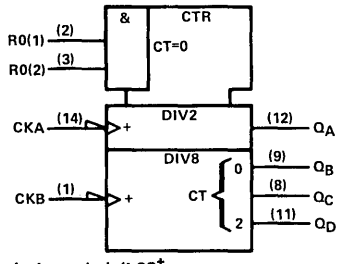
4-BIT BINARY COUNTERS

typical performance

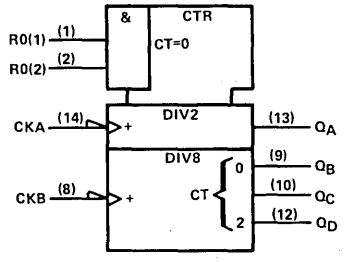
TYPE	COUNT FREQUENCY	CLEAR	TOTAL POWER
'93A	32 MHz	HIGH	160 mW
'L93	3 MHz	HIGH	20 mW
'LS93	32 MHz	HIGH	39 mW

SN5493A (J,FC) SN7493A (J,N)
SN54L93 (J)
SN54LS93 (J,FC) SN74LS93 (J,N)

logic symbol, '93A, 'LS93†



logic symbol, 'L93†



See *TTL Data Book*

pin assignments, '93A, 'LS93

J, N PACKAGES				FC, FN PACKAGES			
1	CKB	8	QC	1	nc	11	QD
2	R0(1)	9	QB	2	nc	12	QA
3	R0(2)	10	GND	3	nc	13	nc
4	nc	11	QD	4	nc	14	nc
5	V_{CC}	12	QA	5	nc	15	CKA
6	nc	13	nc	6	nc	16	CKB
7	nc	14	CKA	7	QC	17	R0(1)
				8	nc	18	nc
				9	QB	19	R0(2)
				10	GND	20	V_{CC}

pin assignments, 'L93

J, N PACKAGES			
1	R0(1)	8	CKB
2	R0(2)	9	QB
3	nc	10	QC
4	V_{CC}	11	GND
5	nc	12	QD
6	nc	13	QA
7	nc	14	CKA

94

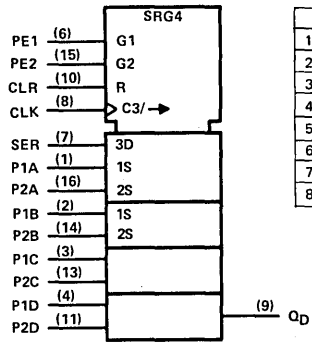
4-BIT SHIFT REGISTERS (DUAL ASYNCHRONOUS PRESETS)

typical performance

TYPE	SHIFT FREQUENCY	SERIAL DATA INPUT	ASYNC CLEAR	TOTAL POWER
'94	10 MHz	D	HIGH	175 mW

SN5494 (J) SN7494 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES			
1	P1A	9	QD
2	P1B	10	CLR
3	P1C	11	P2D
4	P1D	12	GND
5	V_{CC}	13	P2C
6	PE1	14	P2B
7	SER	15	PE2
8	CLK	16	P2A

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

95

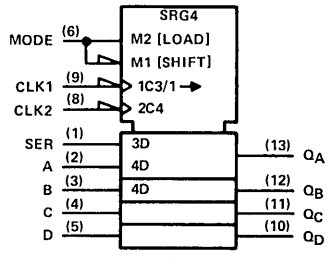
4-BIT SHIFT REGISTERS (PARALLEL IN/PARALLEL OUT, SHIFT RIGHT, SHIFT LEFT, SERIAL INPUT)

typical performance

TYPE	SHIFT FREQUENCY	SERIAL DATA INPUT	TOTAL POWER
'95A	25 MHz	D	195 mW
'L95	3 MHz	D	19 mW
'LS95B	30 MHz	D	65 mW

SN5495 A (J,FC) SN7495A (J,N)
SN54L95 (J)
SN54LS95B (J,FC) SN74LS95B (J,N)

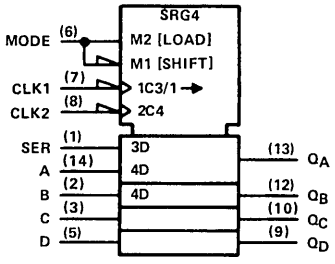
logic symbol, '95A, 'LS95B†



pin assignments, '95A, 'LS95B

J, N PACKAGES		FC, FN PACKAGES	
1 SER	8 CLK2	1 nc	11 CLK2
2 A	9 CLK1	2 SER	12 CLK1
3 B	10 QD	3 A	13 nc
4 C	11 QC	4 B	14 nc
5 D	12 QB	5 C	15 QD
6 MODE	13 QA	6 D	16 QC
7 GND	14 V_{CC}	7 nc	17 QB
		8 nc	18 nc
		9 MODE	19 QA
		10 GND	20 V_{CC}

logic symbol, 'L95†



pin assignments, 'L95

J, N PACKAGES			
1	SER	8	CLK2
2	B	9	QD
3	C	10	QC
4	V_{CC}	11	GND
5	D	12	QB
6	MODE	13	QA
7	CLK1	14	A

See *TTL Data Book*

96

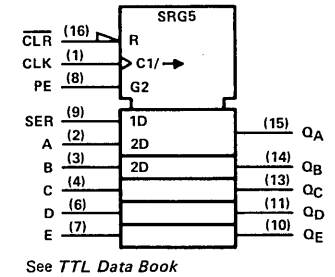
5-BIT SHIFT REGISTERS

typical performance

TYPE	SHIFT FREQUENCY	SERIAL DATA INPUT	ASYNC CLEAR	TOTAL POWER
'96	10 MHz	D	LOW	240 mW
'L96	5 MHz	D	LOW	120 mW
'LS96	10 MHz	D	LOW	60 mW

SN5496 (J,FC) SN7496 (J,N)
SN54L96 (J)
SN54LS96 (J,FC) SN74LS96 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	CLK	9	SER	1	nc	11	QC
2	A	10	QE	2	D	12	QB
3	B	11	QD	3	nc	13	QA
4	C	12	GND	4	E	14	nc
5	V_{CC}	13	QC	5	PE	15	$\overline{CLR}$
6	D	14	QB	6	SER	16	CLK
7	E	15	QA	7	QE	17	A
8	PE	16	$\overline{CLR}$	8	nc	18	B
				9	QD	19	C
				10	GND	20	V_{CC}

97

SYNCHRONOUS 6-BIT BINARY RATE MULTIPLIERS

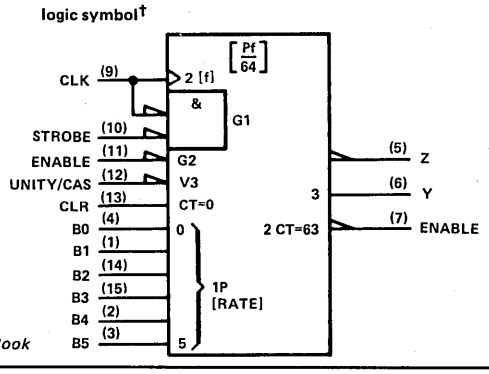
typical performance

TYPE	POWER	FREQ‡
'97	345 mW	32 MHz

‡ Maximum clock frequency

SN5497 (J) SN7497 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES			
1	B1	9	CLK
2	B4	10	STRB
3	B5	11	ENin
4	B0	12	UNITY/CAS
5	Z	13	CLR
6	Y	14	B2
7	ENout	15	B3
8	GND	16	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

8

98

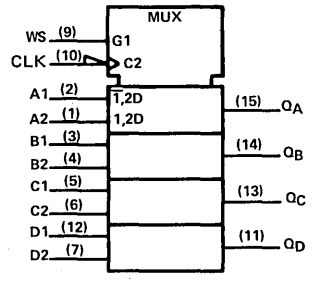
4-BIT DATA SELECTOR/ STORAGE REGISTERS

typical performance

TYPE	FREQUENCY	POWER
'L98	3 MHz	25 mW

SN54L98 (J)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES			
1	A2	9	WS
2	A1	10	CLK
3	B1	11	QD
4	B2	12	D1
5	C1	13	QC
6	C2	14	QB
7	D2	15	QA
8	GND	16	V_{CC}

99

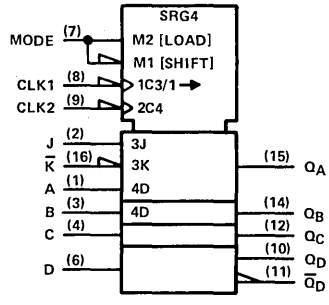
4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

typical performance

TYPE	SHIFT FREQUENCY	SERIAL DATA INPUT	TOTAL POWER
'L99	3 MHz	J-$\overline{K}$	19 mW

SN54L99 (J)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES			
1	A	9	CLK2
2	J	10	QD
3	B	11	$\overline{Q}D$
4	C	12	QC
5	V_{CC}	13	GND
6	D	14	QB
7	MODE	15	QA
8	CLK1	16	$\overline{K}$

100

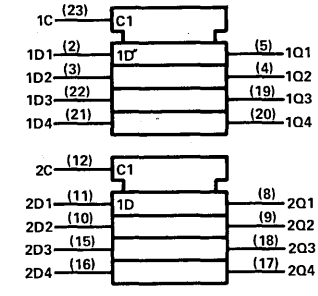
8-BIT BISTABLE LATCHES

typical performance

TYPE	OUTPUTS	DELAY	TOTAL POWER
'100	Q	15 ns	320 mW

SN54100 (J) SN74100 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES			
1	nc	13	nc
2	1D1	14	nc
3	1D2	15	2D3
4	1Q2	16	2D4
5	1Q1	17	2Q4
6	nc	18	2Q3
7	GND	19	1Q3
8	2Q1	20	1Q4
9	2Q2	21	1D4
10	2D2	22	1D3
11	2D1	23	1C
12	2C	24	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

101

AND-OR-GATED J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET

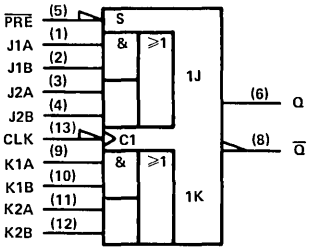
typical performance

TYPE	NO. OF F-F'S	f_{max}	PWR/ F-F	SET-UP	HOLD
'H101	1	50 MHz	100 mW	13 ns↓	0 ns↓

↓ Falling edge of clock pulse

SN54H101 (J) SN74H101 (J,N)

logic symbol†



pin assignments

J, N PACKAGES	
1 J1A	8 Q̄
2 J1B	9 K1A
3 J2A	10 K1B
4 J2B	11 K2A
5 PRE	12 K2B
6 Q	13 CLK
7 GND	14 V_{CC}

positive logic: $J = (J1A \cdot J1B) + (J2A \cdot J2B)$

$K = (K1A \cdot K1B) + (K2A \cdot K2B)$

See *TTL Data Book*

102

AND-GATED J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

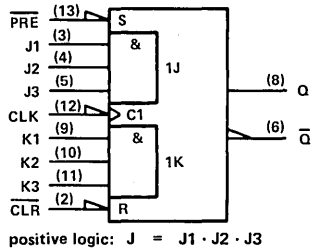
typical performance

TYPE	f_{max}	PWR/ F-F	SET-UP	HOLD
'H102	50 MHz	100 mW	13 ns↓	0 ns↓

↓ Falling edge of clock pulse

SN54H102 (J,FC) SN74H102 (J,N)

logic symbol†



positive logic: $J = J1 \cdot J2 \cdot J3$

$K = K1 \cdot K2 \cdot K3$

See *TTL Data Book*

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 NC	8 Q	1 nc	11 Q
2 CLR	9 K1	2 CLR	12 K1
3 J1	10 K2	3 nc	13 nc
4 J2	11 K3	4 nc	14 nc
5 J3	12 CLK	5 J1	15 K2
6 Q̄	13 PRE	6 nc	16 K3
7 GND	14 V_{CC}	7 J2	17 CLK
		8 J3	18 nc
		9 Q̄	19 PRE
		10 GND	20 V_{CC}

103

DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR

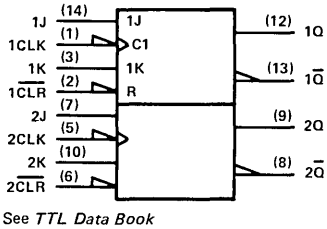
typical performance

TYPE	f_{max}	PWR/ F-F	SET-UP	HOLD
'H103	50 MHz	100 mW	13 ns↓	0 ns↓

↓ Falling edge of clock pulse

SN54H103 (J,FC) SN74H103 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 1CLK	8 2Q̄	1 2CLK	11 1Q
2 1CLR	9 2Q	2 2CLR	12 1Q̄
3 1K	10 2K	3 nc	13 nc
4 V_{CC}	11 GND	4 nc	14 nc
5 2CLK	12 1Q	5 2J	15 1J
6 2CLR	13 1Q̄	6 2Q̄	16 1CLK
7 2J	14 1J	7 2Q	17 1CLR
		8 nc	18 nc
		9 2K	19 1K
		10 GND	20 V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

8

106

DUAL J-K NEGATIVE-EDGE TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

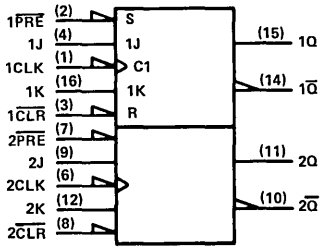
typical performance

TYPE	f_{max}	PWR/ F-F	SET-UP	HOLD
'H106	50 MHz	100 mW	13 ns↓	0 ns↓

↓ Falling edge of clock pulse

SN54H106 (J) SN74H106 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES			
1	1CLK	9	2J
2	1PRE	10	2Q̄
3	1CLR	11	2Q
4	1J	12	2K
5	V_{CC}	13	GND
6	2CLK	14	1Q̄
7	2PRE	15	1Q
8	2CLR	16	1K

107

DUAL J-K FLIP-FLOPS WITH CLEAR

typical performance

TYPE	f_{max}	PWR/ F-F	SET-UP	HOLD
'107	20 MHz	50 mW	0 ns↑	0 ns↓
'LS107A	45 MHz	10 mW	20 ns↓	0 ns↓

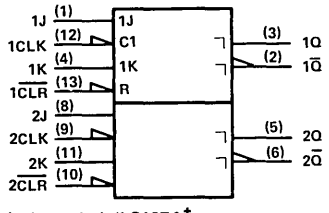
↑ Rising edge of clock pulse

↓ Falling edge of clock pulse

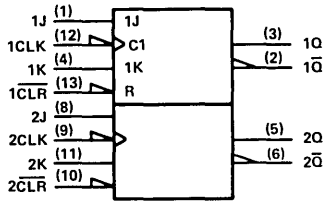
SN54107 (J,FC) SN74107 (J,N)

SN54LS107A (J,FC) SN74LS107A (J,N)

logic symbol, '107†



logic symbol, 'LS107A†



See *TTL Data Book*

pin assignments

J, N PACKAGES			
1	1J	8	2J
2	1Q̄	9	2CLK
3	1Q	10	2CLR
4	1K	11	2K
5	2Q	12	1CLK
6	2Q̄	13	1CLR
7	GND	14	V_{CC}

FC, FN PACKAGES			
1	1J	11	2J
2	1Q̄	12	2CLK
3	nc	13	nc
4	nc	14	2CLR
5	1Q	15	2K
6	1K	16	nc
7	2Q	17	1CLK
8	nc	18	nc
9	2Q̄	19	1CLR
10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

108

DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

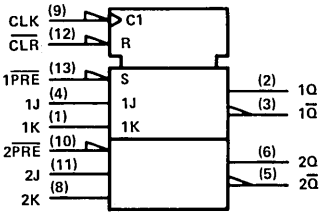
typical performance

TYPE	f_{max}	PWR/ F-F	SET-UP	HOLD
'H108	50 MHz	100 mW	13 ns↓	0 ns↓

↓ Falling edge of clock pulse

SN54H108 (J) SN74H108 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES			
1	1K	8	2K
2	1Q	9	CLK
3	1Q̄	10	2PRE
4	1J	11	2J
5	2Q̄	12	CLR
6	2Q	13	1PRE
7	GND	14	V_{CC}

109

DUAL J-K̄ POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

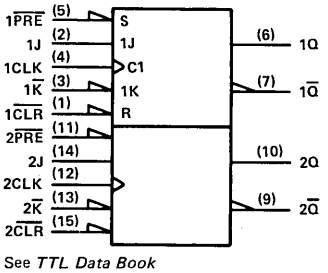
typical performance

TYPE	f_{max}	PWR/ F-F	SET-UP	HOLD
'109	33 MHz	45 mW	10 ns↑	6 ns↑
'ALS109	50 MHz	6 mW	15 ns↑	0 ns↑
'LS109A	33 MHz	10 mW	20 ns↑	5 ns↑

↑ Rising edge of clock pulse

SN54109 (J,FC) SN74109 (J,N)
SN54ALS109 (J,FC) SN74ALS109 (J,N,FN)
SN54LS109A (J,FC) SN74LS109A (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES			
1	1CLR	9	2Q̄
2	1J	10	2Q
3	1K̄	11	2PRE
4	1CLK	12	2CLK
5	1PRE	13	2K̄
6	1Q	14	2J
7	1Q̄	15	2CLR
8	GND	16	V_{CC}

FC, FN PACKAGES			
1	nc	11	2Q̄
2	1CLR	12	2Q
3	1J	13	nc
4	1K̄	14	nc
5	1CLK	15	2PRE
6	1PRE	16	2CLK
7	1Q	17	2K̄
8	nc	18	2J
9	1Q̄	19	2CLR
10	GND	20	V_{CC}

110

AND-GATED J-K MASTER-SLAVE FLIP-FLOPS WITH DATA LOCKOUT

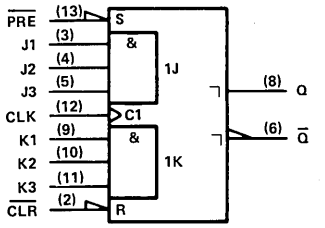
typical performance

TYPE	f_{max}	PWR/ F-F	SET-UP	HOLD
'110	25 MHz	100 mW	20 ns↑	5 ns↑

↑ Rising edge of clock pulse

SN54110 (J) SN74110 (J,N)

logic symbol†



positive logic: J = J1 · J2 · J3
K = K1 · K2 · K3

See *TTL Data Book*

pin assignments

J, N PACKAGES			
1	nc	8	Q
2	CLR	9	K1
3	J1	10	K2
4	J2	11	K3
5	J3	12	CLK
6	Q̄	13	PRE
7	GND	14	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

8

111

DUAL J-K MASTER-SLAVE FLIP-FLOPS WITH DATA LOCKOUT

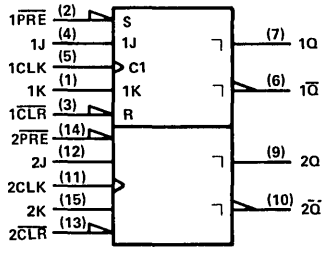
typical performance

TYPE	f_{max}	PWR/ F-F	SET-UP	HOLD
'111	25 MHz	70 mW	0 ns†	30 ns†

† Rising edge of clock pulse

SN54111 (J) SN74111 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES			
1	1K	9	2Q
2	1PRE	10	2Q̄
3	1CLR	11	2CLK
4	1J	12	2J
5	1CLK	13	2CLR
6	1Q̄	14	2PRE
7	1Q	15	2K
8	GND	16	V_{CC}

112

DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

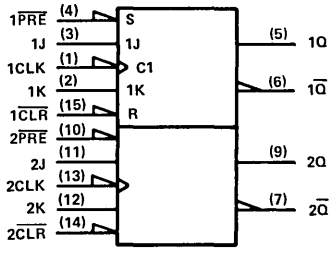
typical performance

TYPE	f_{max}	PWR/ F-F	SET-UP	HOLD
'ALS112	40 MHz	6 mW	25 ns↓	0 ns↓
'LS112A	45 MHz	10 mW	20 ns↓	0 ns↓
'S112	125 MHz	75 mW	3 ns↓	0 ns↓

↓ Falling edge of clock pulse

SN54ALS112 (J,FC) SN74ALS112 (J,N,FN)
SN54LS112A (J,FC) SN74LS112A (J,N)
SN54S112 (J,FC) SN74S112 (J,N,FN)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES			
1	1CLK	9	2Q
2	1K	10	2PRE
3	1J	11	2J
4	1PRE	12	2K
5	1Q	13	2CLK
6	1Q̄	14	2CLR
7	2Q̄	15	1CLR
8	GND	16	V_{CC}

FC, FN PACKAGES			
1	1CLK	11	2Q
2	1K	12	nc
3	1J	13	2PRE
4	nc	14	2J
5	1PRE	15	2K
6	1Q	16	2CLK
7	1Q̄	17	2CLR
8	nc	18	nc
9	2Q̄	19	1CLR
10	GND	20	V_{CC}

113

DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET

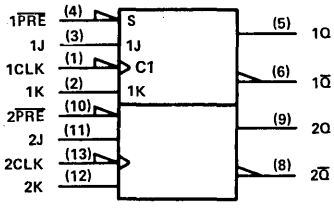
typical performance

TYPE	f_{max}	PWR/ F-F	SET-UP	HOLD
'ALS113	40 MHz	6 mW	25 ns↓	0 ns↓
'LS113A	45 MHz	10 mW	20 ns↓	0 ns↓
'S113	125 MHz	75 mW	3 ns↓	0 ns↓

↓ Falling edge of clock pulse

SN54ALS113 (J,FC) SN74ALS113 (J,N,FN)
SN54LS113A (J,FC) SN74LS113A (J,N)
SN54S113 (J,FC) SN74S113 (J,N,FN)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES			
1	1CLK	8	2Q̄
2	1K	9	2Q
3	1J	10	2PRE
4	1PRE	11	2J
5	1Q	12	2K
6	1Q̄	13	2CLK
7	GND	14	V_{CC}

FC, FN PACKAGES			
1	nc	11	2Q̄
2	1CLK	12	2Q
3	nc	13	nc
4	1K	14	nc
5	1J	15	2PRE
6	1PRE	16	2J
7	1Q	17	2K
8	nc	18	nc
9	1Q̄	19	2CLK
10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

114

DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET, COMMON, AND COMMON CLOCK

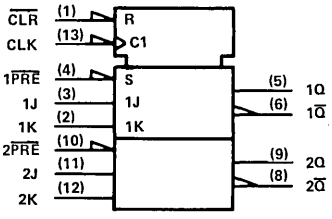
typical performance

TYPE	f_{max}	PWR/ F-F	SET-UP	HOLD
'ALS114	40 MHz	6 mW	25 ns↓	0 ns↓
'LS114A	45 MHz	10 mW	20 ns↓	0 ns↓
'S114	125 MHz	75 mW	3 ns↓	0 ns↓

↓ Falling edge of clock pulse

SN54ALS114 (J,FC) SN74ALS114 (J,N,FN)
SN54LS114A (J,FC) SN74LS114A (J,N)
SN54S114 (J,FC) SN74S114 (J,N,FN)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 CLR	8 2Q̄	1 nc	11 2Q̄
2 1K	9 2Q	2 CLR	12 2Q
3 1J	10 2PRE	3 nc	13 nc
4 1PRE	11 2J	4 1K	14 nc
5 1Q	12 2K	5 1J	15 2PRE
6 1Q̄	13 CLK	6 1PRE	16 2J
7 GND	14 V_{CC}	7 1Q	17 2K
		8 nc	18 nc
		9 1Q̄	19 CLK
		10 GND	20 V_{CC}

116

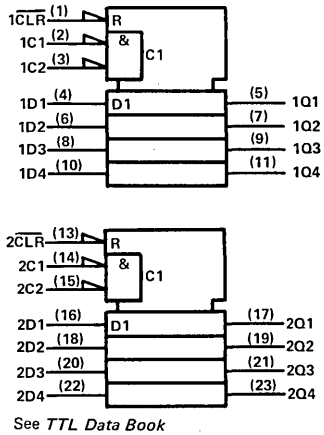
DUAL 4-BIT LATCHES

typical performance

TYPE	BITS	CLEAR	OUT-PUTS	DELAY	TOTAL POWER
'116	8	LOW	Q	11 ns	250 mW

SN54116 (J,FC) SN74116 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 1CLR	13 2CLR	1 1CLR	15 2CLR
2 1C1	14 2C1	2 1C1	16 2C1
3 1C2	15 2C2	3 1C2	17 2C2
4 1D1	16 2D1	4 nc	18 nc
5 1Q1	17 2Q1	5 1D1	19 2D1
6 1D2	18 2D2	6 1Q1	20 2Q1
7 1Q2	19 2Q2	7 1D2	21 2D2
8 1D3	20 2D3	8 1Q2	22 2Q2
9 1Q3	21 2Q3	9 1D3	23 2D3
10 1D4	22 2D4	10 1Q3	24 2Q3
11 1Q4	23 2Q4	11 nc	25 2D4
12 GND	24 V_{CC}	12 1D4	26 nc
		13 1Q4	27 2Q4
		14 GND	28 V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

120

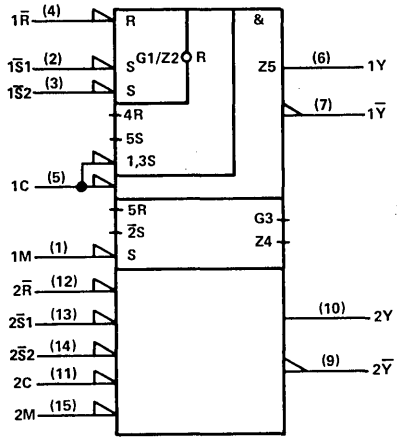
DUAL PULSE SYNCHRONIZERS/ DRIVERS

typical performance

TYPE	ENABLE INPUT	COMP OUTPUT	FREQ RANGE	POWER
'120	YES	YES	DC to 30 MHz	255 mW

SN54120 (J) SN74120 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES			
1	1M	9	2Ȳ
2	1S̄1	10	2Y
3	1S̄2	11	2C
4	1R̄	12	2R̄
5	1C	13	2S̄1
6	1Y	14	2S̄2
7	1Ȳ	15	2M
8	GND	16	V_{CC}

121

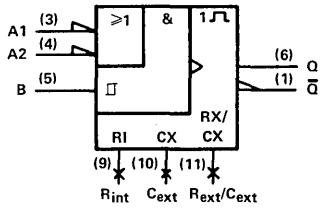
MONOSTABLE MULTIVIBRATORS

typical performance

TYPE	NO. OF INPUTS HI	NO. OF INPUTS LO	OUTPUT PULSE RANGE	TOTAL POWER
'121	1	2	40 ns-28 s	90 mW
'L121	1	2	40 ns-28 s	40 mW

SN54121 (J) SN74121 (J,N)
SN54L121 (J)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES			
1	Q̄	8	nc
2	nc	9	R_{int}
3	A1	10	C_{ext}
4	A2	11	R_{ext}/C_{ext}
5	B	12	nc
6	Q	13	nc
7	GND	14	V_{CC}

'121 . . . R_{int} = 2 kΩ nominal
'L121 . . . R_{int} = 4 kΩ nominal

122

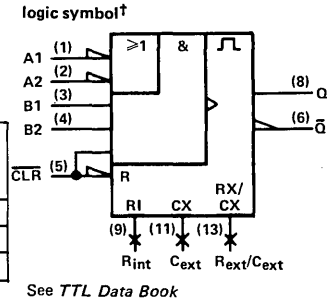
RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH CLEAR

typical performance

TYPE	NO. OF INPUTS HI	NO. OF INPUTS LO	DIRECT CLEAR	OUTPUT PULSE RANGE	TOTAL POWER
'122	2	2	YES	45 ns-∞	115 mW
'L122	2	2	YES	90 ns-∞	55 mW
'LS122	2	2	YES	45 ns-∞	30 mW

SN54122 (J,FC) SN74122 (J,N)
SN54L122 (J)
SN54LS122 (J,FC) SN74LS122 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES			
1	A1	8	Q
2	A2	9	R_{int}
3	B1	10	nc
4	B2	11	C_{ext}
5	CLR	12	nc
6	Q̄	13	R_{ext}/C_{ext}
7	GND	14	V_{CC}

FC, FN PACKAGES			
1	A1	11	Q
2	A2	12	R_{int}
3	nc	13	nc
4	nc	14	nc
5	B1	15	C_{ext}
6	B2	16	nc
7	CLR	17	nc
8	nc	18	nc
9	Q̄	19	R_{ext}/C_{ext}
10	GND	20	V_{CC}

'122 . . . R_{int} = 10 kΩ nominal
'L122 . . . R_{int} = 20 kΩ nominal
'LS122 . . . R_{int} = 10 kΩ nominal

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

123

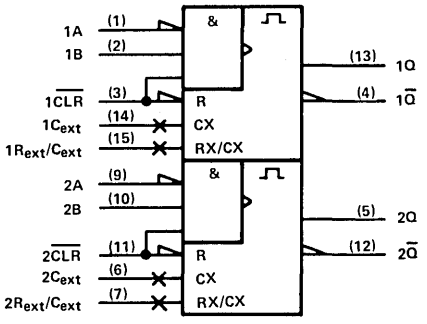
DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH POSITIVE AND NEGATIVE INPUTS AND DIRECT CLEAR

typical performance

TYPE	OUTPUT PULSE RANGE	TOTAL POWER
'123	45 ns-∞	230 mW
'L123	90 ns-∞	115 mW
'LS123	45 ns-∞	60 mW

SN54123 (J,FC) SN74123 (J,N)
SN54L123 (J)
SN54LS123 (J,FC) SN74LS123 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 1A	9 2A	1 1A	11 2A
2 1B	10 2B	2 1B	12 2B
3 1CLR	11 2CLR	3 nc	13 nc
4 1Q	12 2Q	4 1CLR	14 nc
5 2Q	13 1Q	5 1Q	15 2CLR
6 2Cext	14 1Cext	6 2Q	16 2Q
7 2Rext/Cext	15 1Rext/Cext	7 2Cext	17 1Q
8 GND	16 VCC	8 nc	18 1Cext
		9 2Rext/Cext	19 1Rext/Cext
		10 GND	20 VCC

124

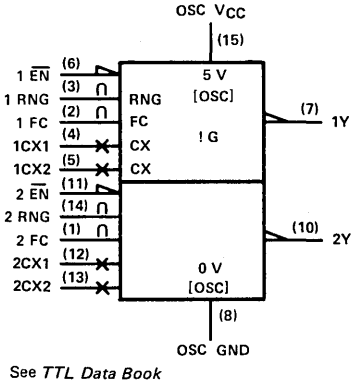
DUAL VOLTAGE-CONTROLLED OSCILLATORS WITH ENABLE INPUTS

typical performance

TYPE	FREQ RANGE	POWER
'S124	1 Hz to 60 MHz	525 mW

SN54S124 (J,FC) SN74S124 (J,N,FN)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 2FC	9 GND	1 2FC	11 GND
2 1FC	10 2Y	2 1FC	12 2Y
3 1RNG	11 2EN	3 nc	13 nc
4 1CX1	12 2CX1	4 1RNG	14 nc
5 1CX2	13 2CX2	5 1CX1	15 2EN
6 1EN	14 2RNG	6 1CX2	16 2CX1
7 1Y	15 OSC VCC	7 1EN	17 2CX2
8 OSC GND	16 VCC	8 nc	18 2RNG
		9 1Y	19 OSC VCC
		10 OSC GND	20 VCC

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

125

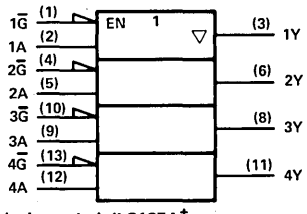
QUADRUPLE BUS BUFFER GATES WITH THREE-STATE OUTPUTS

typical performance

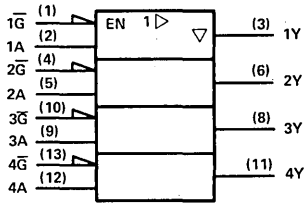
TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54125	10 ns	−2 mA	16 mA
SN74125	10 ns	−5.2 mA	16 mA
SN54LS125A	8 ns	−1 mA	12 mA
SN74LS125A	8 ns	−2.6 mA	24 mA

SN54125 (J,FC) SN74125 (J,N)
SN54LS125A (J,FC) SN74LS125A (J,N)

logic symbol, '125†



logic symbol, 'LS125A†



positive logic: Y = A

See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES	
1	1G̅	8	3Y	1 nc	11 3Y
2	1A	9	3A	2 1G̅	12 3A
3	1Y	10	3G̅	3 nc	13 nc
4	2G̅	11	4Y	4 1A	14 nc
5	2A	12	4A	5 1Y	15 3G̅
6	2Y	13	4G̅	6 2G̅	16 4Y
7	GND	14	V_{CC}	7 2A	17 4A
				8 nc	18 nc
				9 2Y	19 4G̅
				10 GND	20 V_{CC}

126

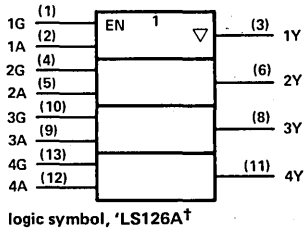
QUADRUPLE BUS BUFFER GATES WITH THREE-STATE OUTPUTS

typical performance

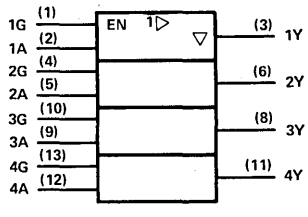
TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54126	10 ns	−2 mA	16 mA
SN74126	10 ns	−5.2 mA	16 mA
SN54LS126A	8.5 ns	−1 mA	12 mA
SN74LS126A	8.5 ns	−2.6 mA	24 mA

SN54126 (J,FC) SN74126 (J,N)
SN54LS126A (J,FC) SN74LS126A (J,N)

logic symbol, '126†



logic symbol, 'LS126A†



positive logic: Y = A

See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES	
1	1G	8	3Y	1 nc	11 3Y
2	1A	9	3A	2 1G	12 3A
3	1Y	10	3G	3 nc	13 nc
4	2G	11	4Y	4 1A	14 nc
5	2A	12	4A	5 1Y	15 3G
6	2Y	13	4G	6 2G	16 4Y
7	GND	14	V_{CC}	7 2A	17 4A
				8 nc	18 nc
				9 2Y	19 4G
				10 GND	20 V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

128

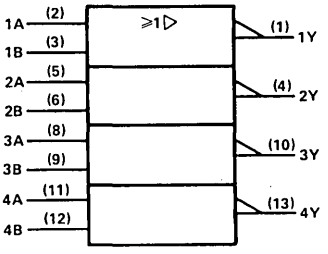
LINE DRIVERS
(SN54128 . . . 75 Ω DRIVER
SN74128 . . . 50 Ω DRIVER)

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT	DELAY
SN54128	48 mA	−29 mA	7 ns
SN74128	48 mA	−42.4 mA	7 ns

SN54128 (J,FC) SN74128 (F,N)

logic symbol†



positive logic: $Y = \overline{A + B}$

See *TTL Data Book*

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 1Y	8 3A	1 nc	11 3A
2 1A	9 3B	2 1Y	12 nc
3 1B	10 3Y	3 nc	13 3B
4 2Y	11 4A	4 1A	14 nc
5 2A	12 4B	5 1B	15 3Y
6 2B	13 4Y	6 2Y	16 4A
7 GND	14 V_{CC}	7 2A	17 4B
		8 nc	18 nc
		9 2B	19 4Y
		10 GND	20 V_{CC}

132

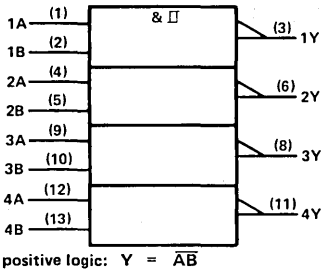
QUADRUPLE 2-INPUT POSITIVE-NAND SCHMITT TRIGGERS

typical performance

TYPE	HYSTERESIS	DELAY
'132	0.8 V	15 ns
'LS132	0.8 V	15 ns
'S132	0.55 V	8 ns

SN54132 (J,FC) SN74132 (J,N)
SN54LS132 (J,FC) SN74LS132 (J,N)
SN54S132 (J,FC) SN74S132 (J,N,FN)

logic symbol†



positive logic: $Y = \overline{AB}$

See *TTL Data Book*

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 1A	8 3Y	1 nc	11 3Y
2 1B	9 3A	2 nc	12 nc
3 1Y	10 3B	3 1A	13 3A
4 2A	11 4Y	4 1B	14 nc
5 2B	12 4A	5 1Y	15 3B
6 2Y	13 4B	6 2A	16 4Y
7 GND	14 V_{CC}	7 2B	17 nc
		8 nc	18 4A
		9 2Y	19 4B
		10 GND	20 V_{CC}

133

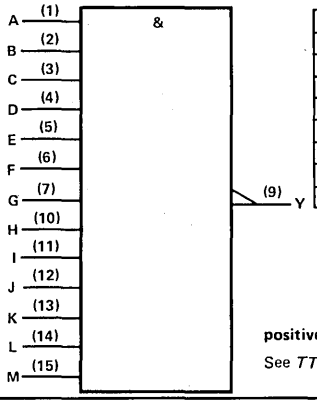
13-INPUT POSITIVE-NAND GATES

typical performance

TYPE	POWER	DELAY
'ALS133	0.15 mW	8 ns
'S133	19 mW	3 ns

SN54ALS133 (J,FC) SN74ALS133 (J,N,FN)
SN54S133 (J,FC) SN74S133 (J,N,FN)

logic symbol†



positive logic: $Y = \overline{ABCDEFGHIJKLM}$

See *TTL Data Book*

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 A	9 Y	1 A	11 Y
2 B	10 H	2 B	12 H
3 C	11 I	3 nc	13 nc
4 D	12 J	4 C	14 I
5 E	13 K	5 D	15 J
6 F	14 L	6 E	16 K
7 G	15 M	7 F	17 L
8 GND	16 V_{CC}	8 nc	18 nc
		9 G	19 M
		10 GND	20 V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

134

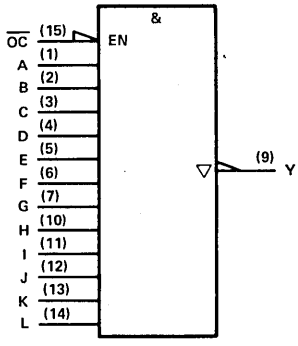
12-INPUT POSITIVE-NAND GATES WITH THREE-STATE OUTPUTS

typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54S134	4.5 ns	−2 mA	20 mA
SN74S134	4.5 ns	−6.5 mA	20 mA

SN54S134 (J,FC) SN74S134 (J,N,FN)

logic symbol†



positive logic: $Y = \overline{ABCDEFGHIJKL}$

See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	A	9	Y	1	A	11	Y
2	B	10	H	2	B	12	H
3	C	11	I	3	nc	13	nc
4	D	12	J	4	C	14	I
5	E	13	K	5	D	15	J
6	F	14	L	6	E	16	K
7	G	15	$\overline{OC}$	7	F	17	L
8	GND	16	V_{CC}	8	nc	18	$\overline{OC}$
				9	G	19	nc
				10	GND	20	V_{CC}

135

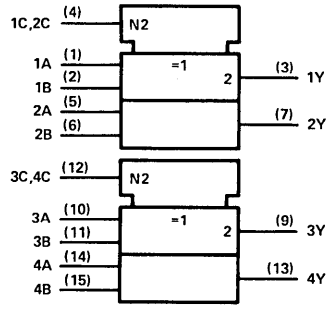
QUAD EXCLUSIVE OR/NOR GATES

typical performance

TYPE	POWER	DELAY
'S135	325 mW	8 ns

SN54S135 (J,FC) SN74S135 (J,N,FN)

logic symbol†



positive logic: $Y = A \oplus B \oplus C = A\overline{B}\overline{C} + \overline{A}B\overline{C} + \overline{A}\overline{B}C + ABC$

See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	1A	9	3Y	1	1A	11	3Y
2	1B	10	3A	2	1B	12	3A
3	1Y	11	3B	3	nc	13	nc
4	1C,2C	12	3C,4C	4	1Y	14	3B
5	2A	13	4Y	5	1C,2C	15	3C,4C
6	2B	14	4A	6	2A	16	4Y
7	2Y	15	4B	7	2B	17	4A
8	GND	16	V_{CC}	8	nc	18	nc
				9	2Y	19	4B
				10	GND	20	V_{CC}

136

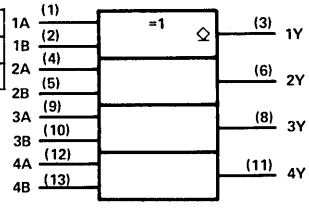
QUAD EXCLUSIVE-OR GATES WITH OPEN-COLLECTOR OUTPUTS

typical performance

TYPE	POWER	DELAY
'136	150 mW	27 ns
'LS136	30 mW	18 ns

SN54136 (J,FC) SN74136 (J,N)
SN54LS136 (J,FC) SN74LS136 (J,N)

logic symbol†



positive logic: $Y = A \oplus B = A\overline{B} + \overline{A}B$

See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	1A	8	3Y	1	nc	11	3Y
2	1B	9	3A	2	nc	12	nc
3	1Y	10	3B	3	1A	13	3A
4	2A	11	4Y	4	1B	14	nc
5	2B	12	4A	5	1Y	15	3B
6	2Y	13	4B	6	2A	16	4Y
7	GND	14	V_{CC}	7	2B	17	nc
				8	nc	18	4A
				9	2Y	19	4B
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

137

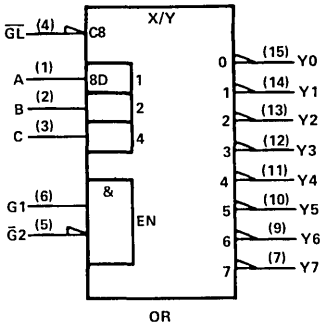
3- TO 8-LINE DECODERS/ DEMULTIPLEXERS WITH ADDRESS LATCHES

typical performance

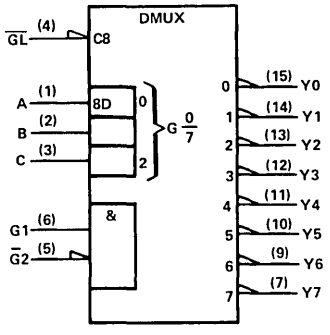
TYPE	SELECT TIME	ENABLE TIME	TOTAL POWER
'LS137	17.5 ns	16 ns	55 mW

SN54LS137 (J,FC) SN74LS137 (J,N)

logic symbol†



OR



pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 A	9 Y6	1 A	11 nc
2 B	10 Y5	2 B	12 Y6
3 C	11 Y4	3 nc	13 nc
4 $\overline{GL}$	12 Y3	4 C	14 Y5
5 $\overline{G2}$	13 Y2	5 nc	15 Y4
6 G1	14 Y1	6 $\overline{GL}$	16 Y3
7 Y7	15 Y0	7 $\overline{G2}$	17 Y2
8 GND	16 V_{CC}	8 G1	18 Y1
		9 Y7	19 Y0
		10 GND	20 V_{CC}

See *TTL Data Book*

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

138

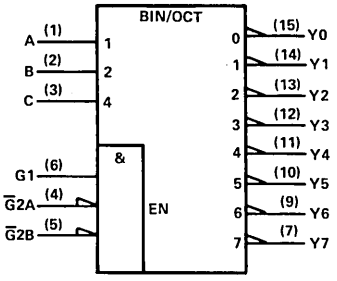
3- TO 8-LINE DECODERS/ DEMULTIPLEXERS

typical performance

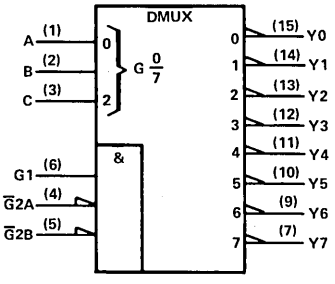
TYPE	SELECT TIME	ENABLE TIME	TOTAL POWER
'LS138	22 ns	21 ns	31 mW
'S138	8 ns	7 ns	245 mW

SN54LS138 (J,FC) SN74LS138 (J,N)
SN54S138 (J,FC) SN74S138 (J,N,FN)

logic symbol†



OR



See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	A	9	Y6	1	A	11	nc
2	B	10	Y5	2	B	12	Y6
3	C	11	Y4	3	nc	13	nc
4	$\overline{G}$2A	12	Y3	4	C	14	Y5
5	$\overline{G}$2B	13	Y2	5	nc	15	Y4
6	G1	14	Y1	6	$\overline{G}$2A	16	Y3
7	Y7	15	Y0	7	$\overline{G}$2B	17	Y2
8	GND	16	V_{CC}	8	G1	18	Y1
				9	Y7	19	Y0
				10	GND	20	V_{CC}

139

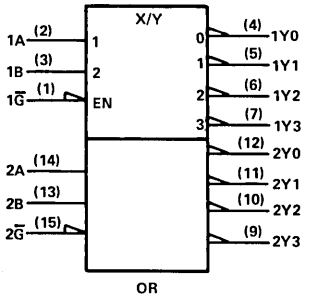
DUAL 2- TO 4-LINE DECODERS/DEMULTIPLEXERS

typical performance

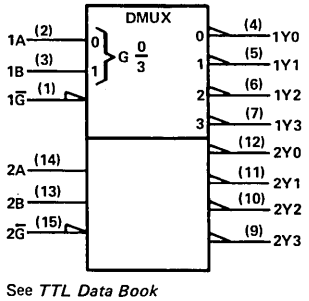
TYPE	SELECT TIME	ENABLE TIME	TOTAL POWER
'LS139	22 ns	19 ns	34 mW
'S139	7.5 ns	6 ns	300 mW

SN54LS139 (J,FC) SN74LS139 (J,N)
SN54S139 (J,FC) SN74S139 (J,N,FN)

logic symbol†



OR



See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	$\overline{1G}$	9	2Y3	1	$\overline{1G}$	11	2Y3
2	1A	10	2Y2	2	1A	12	2Y2
3	1B	11	2Y1	3	nc	13	nc
4	1Y0	12	2Y0	4	1B	14	2Y1
5	1Y1	13	2B	5	1Y0	15	2Y0
6	1Y2	14	2A	6	1Y1	16	2B
7	1Y3	15	$2\overline{G}$	7	1Y2	17	2A
8	GND	16	V_{CC}	8	nc	18	nc
				9	1Y3	19	$2\overline{G}$
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

140

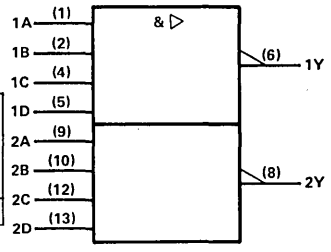
DUAL 4-INPUT POSITIVE-NAND 50-OHM LINE DRIVERS

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT	DELAY	POWER PER GATE
'S140	60 mA	–40 mA	4 ns	44 mW

SN54S140 (J,FC) SN74S140 (J,N,FN)

logic symbol†



positive logic: $Y = \overline{ABCD}$

See *TTL Data Book*

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 1A	8 2Y	1 nc	11 nc
2 1B	9 2A	2 nc	12 2Y
3 nc	10 2B	3 1A	13 nc
4 1C	11 nc	4 nc	14 nc
5 1D	12 2C	5 1B	15 2A
6 1Y	13 2D	6 1C	16 2B
7 GND	14 V_{CC}	7 1D	17 2C
		8 nc	18 nc
		9 1Y	19 2D
		10 GND	20 V_{CC}

141

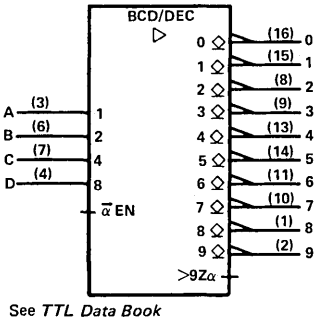
BCD-TO-DECIMAL DECODER/DRIVER

typical performance

TYPE	OUTPUT SINK CURRENT	OFF-STATE OUTPUT VOLTAGE	TOTAL POWER
'141	7 mA	60 V	80 mW

SN74141 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES	
1 8	9 3
2 9	10 7
3 A	11 6
4 D	12 GND
5 V_{CC}	13 4
6 B	14 5
7 C	15 1
8 2	16 0

142

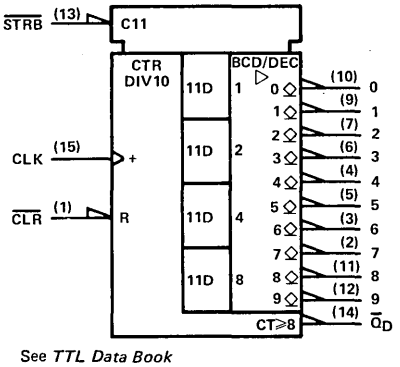
COUNTER/LATCH/DECODER/DRIVER

typical performance

TYPE	OUTPUT SINK CURRENT	OFF-STATE OUTPUT VOLTAGE	TOTAL POWER
'142	7 mA	55 V	340 mW

SN74142 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES	
1 $\overline{CLR}$	9 1
2 7	10 0
3 6	11 8
4 4	12 9
5 5	13 $\overline{STRB}$
6 3	14 $\overline{QD}$
7 2	15 CLK
8 GND	16 V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

8

143,144

COUNTERS/LATCHES/ DECODERS/DRIVERS

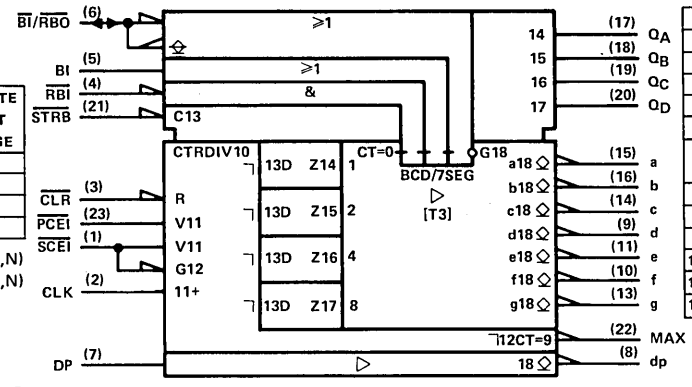
typical performance

TYPE	OUTPUT SINK CURRENT	OFF-STATE OUTPUT VOLTAGE
SN54143	15 mA*	7 V
SN74143	15 mA*	7 V
SN54144	20 mA	15 V
SN74144	25 mA	15 V

SN54143 (J) SN74143 (J,N)
SN54144 (J) SN74144 (J,N)

* Constant current

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES			
1	$\overline{SCEI}$	13	g
2	CLK	14	c
3	$\overline{CLR}$	15	a
4	$\overline{RBI}$	16	b
5	BI	17	QA
6	$\overline{BI}/\overline{RBO}$	18	QB
7	DP	19	QC
8	dp	20	QD
9	d	21	$\overline{STRB}$
10	f	22	MAX
11	e	23	$\overline{PCEI}$
12	GND	24	V_{CC}

145

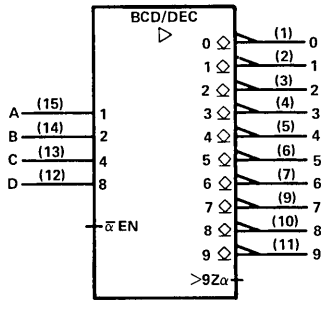
BCD-TO-DECIMAL DECODERS/ DRIVERS FOR LAMPS, RELAYS, MOS

typical performance

TYPE	OUTPUT SINK CURRENT	OFF-STATE OUTPUT VOLTAGE	TOTAL POWER
'145	80 mA	15 V	215 mW
'54LS145	12 mA	15 V	35 mW
'74LS145	80 mA	15 V	35 mW

SN54145 (J,FC) SN74145 (J,N)
SN54LS145 (J,FC) SN74LS145 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	0	9	7	1	0	11	7
2	1	10	8	2	1	12	8
3	2	11	9	3	nc	13	nc
4	3	12	D	4	2	14	9
5	4	13	C	5	3	15	D
6	5	14	B	6	4	16	C
7	6	15	A	7	5	17	B
8	GND	16	V_{CC}	8	nc	18	nc
				9	6	19	A
				10	GND	20	V_{CC}

147

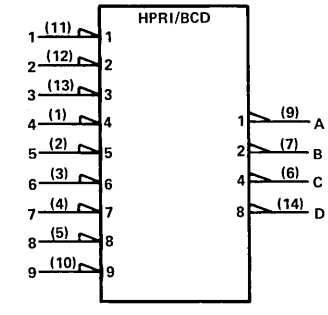
10-LINE DECIMAL TO 4-LINE BCD PRIORITY ENCODERS

typical performance

TYPE	POWER	DELAY
'147	225 mW	10 ns
'LS147	60 mW	15 ns

SN54147 (J,FC) SN74147 (J,N)
SN54LS147 (J,FC) SN74LS147 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	4	9	A	1	4	11	A
2	5	10	9	2	5	12	9
3	6	11	1	3	nc	13	nc
4	7	12	2	4	6	14	nc
5	8	13	3	5	7	15	1
6	C	14	D	6	8	16	2
7	B	15	nc	7	C	17	3
8	GND	16	V_{CC}	8	nc	18	nc
				9	B	19	D
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

FONT TABLE T3 — RESULTANT DISPLAYS USING '143, '144

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

148

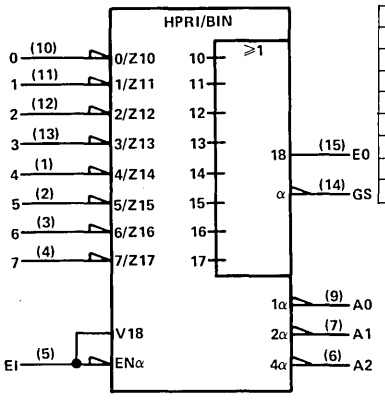
8- TO 3-LINE OCTAL PRIORITY ENCODERS

typical performance

TYPE	POWER	DELAY
'148	190 mW	12 ns
'LS148	60 mW	15 ns

SN54148 (J,FC) SN74148 (J,N)
SN54LS148 (J,FC) SN74LS148 (J,N)†

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	4	9	A0	1	4	11	A0
2	5	10	0	2	5	12	0
3	6	11	1	3	nc	13	nc
4	7	12	2	4	6	14	1
5	E1	13	3	5	7	15	2
6	A2	14	GS	6	E1	16	3
7	A1	15	E0	7	A2	17	GS
8	GND	16	V_{CC}	8	nc	18	nc
				9	A1	19	E0
				10	GND	20	V_{CC}

150

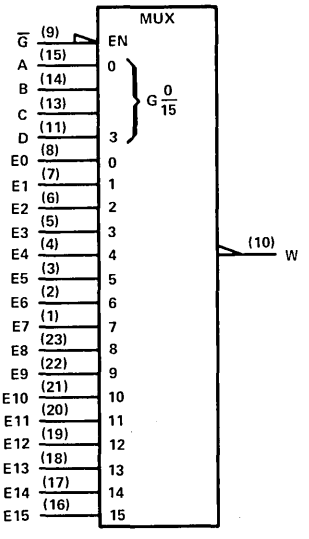
1-OF-16 DATA SELECTORS/ MULTIPLEXERS

typical performance

TYPE	DATA TO INV OUTPUT	FROM ENABLE	TOTAL POWER
'150	11 ns	18 ns	200 mW

SN54150 (J,FC) SN74150 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	E7	13	C	1	E7	15	C
2	E6	14	B	2	E6	16	B
3	E5	15	A	3	E5	17	A
4	E4	16	E15	4	nc	18	nc
5	E3	17	E14	5	E4	19	nc
6	E2	18	E13	6	E3	20	E15
7	E1	19	E12	7	E2	21	E14
8	E0	20	E11	8	E1	22	E13
9	$\overline{G}$	21	E10	9	E0	23	E12
10	W	22	E9	10	$\overline{G}$	24	E11
11	D	23	E8	11	W	25	E10
12	GND	24	V_{CC}	12	nc	26	E9
				13	D	27	E8
				14	GND	28	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

151

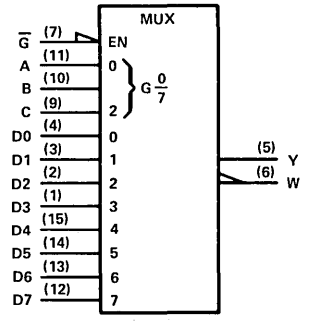
1-OF-8 DATA SELECTORS/ MULTIPLEXERS

typical performance

TYPE	DELAY TIMES: DATA TO INV OUTPUT	DELAY TIMES: DATA TO NON-INV OUTPUT	DELAY TIMES: FROM ENABLE	TOTAL POWER
'151A	8 ns	16 ns	22 ns	145 mW
'LS151	11 ns	18 ns	27 ns	30 mW
'S151	4.5 ns	8 ns	9 ns	225 mW

SN54151A (J,FC) SN74151A (J,N)
SN54LS151 (J,FC) SN74LS151 (J,N)
SN54S151 (J,FC) SN74S151 (J,N,FN)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 D3	9 C	1 D3	11 C
2 D2	10 B	2 D2	12 B
3 D1	11 A	3 nc	13 nc
4 D0	12 D7	4 D1	14 A
5 Y	13 D6	5 D0	15 D7
6 W	14 D5	6 Y	16 D6
7 $\overline{G}$	15 D4	7 W	17 D5
8 GND	16 V_{CC}	8 nc	18 nc
		9 $\overline{G}$	19 D4
		10 GND	20 V_{CC}

152

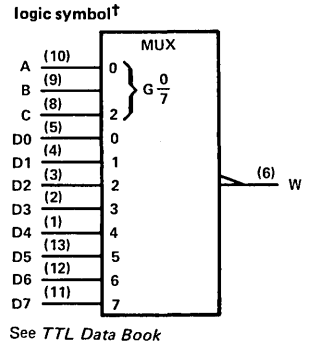
1-OF-8 DATA SELECTORS/ MULTIPLEXERS

typical performance

TYPE	DELAY TIMES: DATA TO INV OUTPUT	DELAY TIMES: FROM ENABLE	TOTAL POWER
'152A	8 ns	–	130 mW
'LS152	11 ns	18 ns	28 mW

SN54152A (J,FC)
SN54LS152 (J,FC)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 D4	8 C	1 D4	11 C
2 D3	9 B	2 D3	12 nc
3 D2	10 A	3 D2	13 nc
4 D1	11 D7	4 D1	14 B
5 D0	12 D6	5 D0	15 A
6 W	13 D5	6 nc	16 D7
7 GND	14 V_{CC}	7 W	17 D6
		8 nc	18 nc
		9 nc	19 D5
		10 GND	20 V_{CC}

153

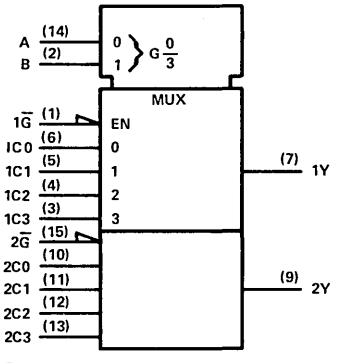
DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

typical performance

TYPE	DELAY TIMES: DATA TO NON-INV OUTPUT	DELAY TIMES: FROM ENABLE	TOTAL POWER
'153	14 ns	17 ns	180 mW
'L153	27 ns	34 ns	90 mW
'LS153	14 ns	17 ns	31 mW
'S153	6 ns	9.5 ns	225 mW

SN54153 (J,FC) SN74153 (J,N)
SN54L153 (J)
SN54LS153 (J,FC) SN74LS153 (J,N)
SN54S153 (J,FC) SN74S153 (J,N,FN)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 1$\overline{G}$	9 2Y	1 1$\overline{G}$	11 2Y
2 B	10 2C0	2 B	12 2C0
3 1C3	11 2C1	3 nc	13 nc
4 1C2	12 2C2	4 1C3	14 2C1
5 1C1	13 2C3	5 1C2	15 2C2
6 1C0	14 A	6 1C1	16 2C3
7 1Y	15 2$\overline{G}$	7 1C0	17 A
8 GND	16 V_{CC}	8 nc	18 nc
		9 1Y	19 2$\overline{G}$
		10 GND	20 V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

154

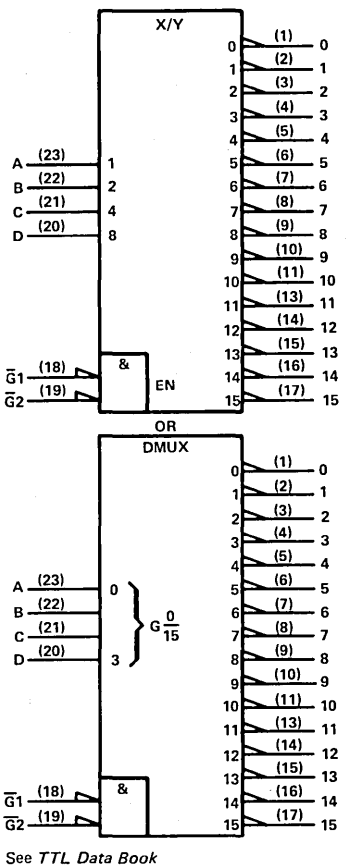
4-LINE TO 16-LINE DECODERS/ DEMULTIPLEXERS

typical performance

TYPE	SELECT TIME	ENABLE TIME	TOTAL POWER
'154	23 ns	19 ns	170 mW
'L154	46 ns	38 ns	85 mW

SN54154 (J) SN74154 (J,N)
SN54L154 (J)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES	
1 0	13 11
2 1	14 12
3 2	15 13
4 3	16 14
5 4	17 15
6 5	18 $\overline{G1}$
7 6	19 $\overline{G2}$
8 7	20 D
9 8	21 C
10 9	22 B
11 10	23 A
12 GND	24 V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

155

DECODERS/DEMULTIPLEXERS

(totem pole outputs)

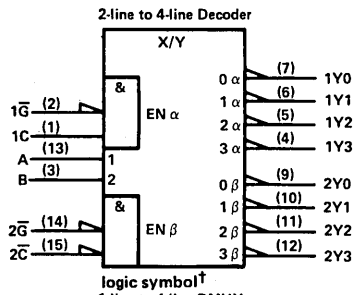
typical performance

TYPE	SELECT TIME	ENABLE TIME	TOTAL POWER
'155	21 ns	16 ns	125 mW
'LS155	18 ns	15 ns	30 mW

SN54155 (J,FC) SN74155 (J,N)
SN54LS155 (J,FC) SN74LS155 (J,N)

logic symbol†

2-line to 4-line Decoder

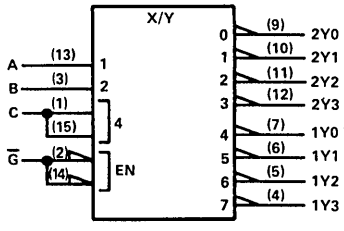


pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 1C	9 2Y0	1 1C	11 2Y0
2 1$\overline{G}$	10 2Y1	2 1$\overline{G}$	12 2Y1
3 B	11 2Y2	3 nc	13 nc
4 1Y3	12 2Y3	4 B	14 2Y2
5 1Y2	13 A	5 1Y3	15 2Y3
6 1Y1	14 2$\overline{G}$	6 1Y2	16 A
7 1Y0	15 2$\overline{C}$	7 1Y1	17 2$\overline{G}$
8 GND	16 V_{CC}	8 nc	18 nc
		9 1Y0	19 2$\overline{C}$
		10 GND	20 V_{CC}

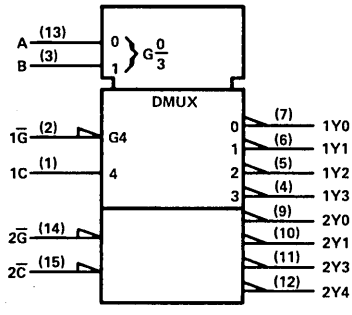
logic symbol†

3-line to 8-line Decoder



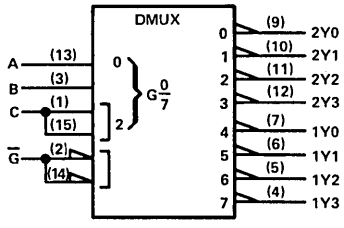
logic symbol†

1-line to 4-line DMUX



logic symbol†

1-line to 8-line DMUX



See *TTL Data Book*

156

DECODERS/DEMULTIPLEXERS

(open-collector outputs)

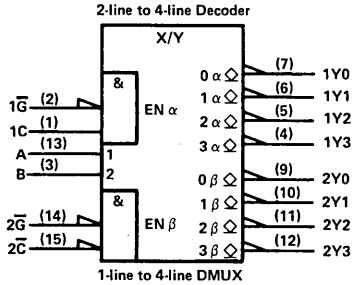
typical performance

TYPE	SELECT TIME	ENABLE TIME	TOTAL POWER
'156	23 ns	18 ns	125 mW
'LS156	33 ns	26 ns	31 mW

SN54156 (J,FC) SN74156 (J,N)
SN54LS156 (J,FC) SN74LS156 (J,N)

logic symbol†

2-line to 4-line Decoder

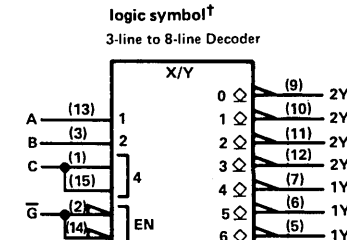


pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 1C	9 2Y0	1 1C	11 2Y0
2 1$\overline{G}$	10 2Y1	2 1$\overline{G}$	12 2Y1
3 B	11 2Y2	3 nc	13 nc
4 1Y3	12 2Y3	4 B	14 2Y2
5 1Y2	13 A	5 1Y3	15 2Y3
6 1Y1	14 2$\overline{G}$	6 1Y2	16 A
7 1Y0	15 2$\overline{C}$	7 1Y1	17 2$\overline{G}$
8 GND	16 V_{CC}	8 nc	18 nc
		9 1Y0	19 2$\overline{C}$
		10 GND	20 V_{CC}

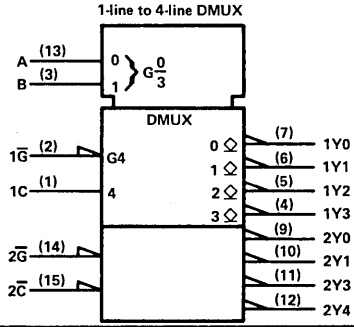
logic symbol†

3-line to 8-line Decoder



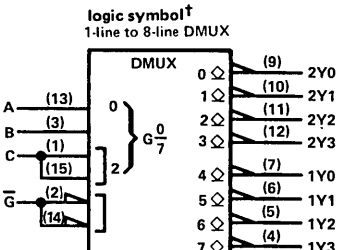
logic symbol†

1-line to 4-line DMUX



logic symbol†

1-line to 8-line DMUX



See *TTL Data Book*

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

157

QUAD 2- TO 1-LINE DATA SELECTORS/MULTIPLEXERS

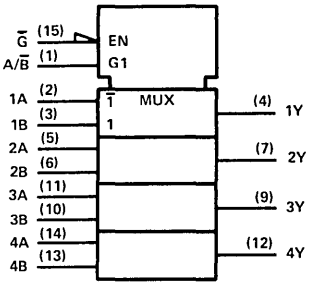
(non-inverted data outputs)

typical performance

TYPE	DELAY TIMES: DATA TO NON-INV OUTPUT	DELAY TIMES: FROM ENABLE	TOTAL POWER
'157	9 ns	14 ns	150 mW
'L157	18 ns	27 ns	75 mW
'LS157	9 ns	14 ns	49 mW
'S157	5 ns	8 ns	250 mW

SN54157 (J,FC) SN74157 (J,N)
SN54L157 (J)
SN54LS157 (J,FC) SN74LS157 (J,N)
SN54S157 (J,FC) SN74S157 (J,N,FN)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	A/$\overline{B}$	9	3Y	1	nc	11	3Y
2	1A	10	3B	2	A/$\overline{B}$	12	3B
3	1B	11	3A	3	nc	13	nc
4	1Y	12	4Y	4	1A	14	3A
5	2A	13	4B	5	1B	15	4Y
6	2B	14	4A	6	1Y	16	4B
7	2Y	15	$\overline{G}$	7	2A	17	4A
8	GND	16	V_{CC}	8	2B	18	nc
				9	2Y	19	$\overline{G}$
				10	GND	20	V_{CC}

158

QUAD 2- TO 1-LINE DATA SELECTORS/MULTIPLEXERS

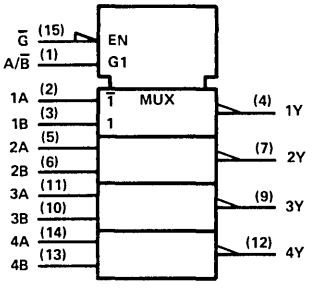
(inverted data outputs)

typical performance

TYPE	DELAY TIMES: DATA TO INV OUTPUT	DELAY TIMES: FROM ENABLE	TOTAL POWER
'LS158	7 ns	12 ns	24 mW
'S158	4 ns	7 ns	195 mW

SN54LS158 (J,FC) SN74LS158 (J,N)
SN54S158 (J,FC) SN74S158 (J,N,FN)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	A/$\overline{B}$	9	3Y	1	nc	11	3Y
2	1A	10	3B	2	A/$\overline{B}$	12	3B
3	1B	11	3A	3	nc	13	nc
4	1Y	12	4Y	4	1A	14	3A
5	2A	13	4B	5	1B	15	4Y
6	2B	14	4A	6	1Y	16	4B
7	2Y	15	$\overline{G}$	7	2A	17	4A
8	GND	16	V_{CC}	8	2B	18	nc
				9	2Y	19	$\overline{G}$
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

159

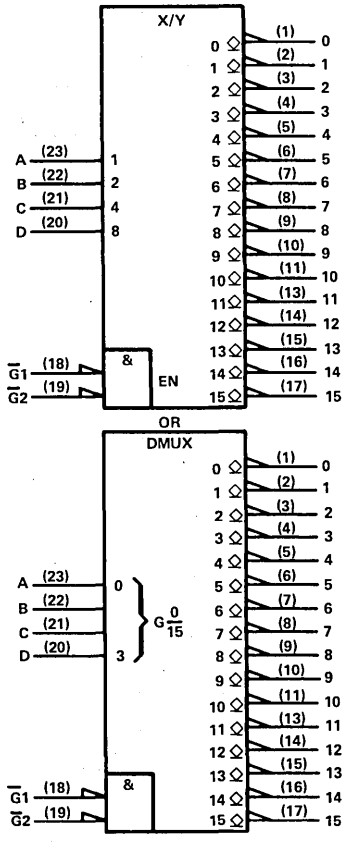
4- TO 16-LINE DECODERS/ DEMULTIPLEXERS
(open-collector outputs)

typical performance

TYPE	SELECT TIME	ENABLE TIME	TOTAL POWER
'159	24 ns	19 ns	170 mW

SN54159 (J) SN74159 (J,N)

logic symbol, '159†



pin assignments

J, N PACKAGES	
1 0	13 11
2 1	14 12
3 2	15 13
4 3	16 14
5 4	17 15
6 5	18 $\overline{G1}$
7 6	19 $\overline{G2}$
8 7	20 D
9 8	21 C
10 9	22 B
11 10	23 A
12 GND	24 V_{CC}

See *TTL Data Book*

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

160

SYNCHRONOUS 4-BIT COUNTERS

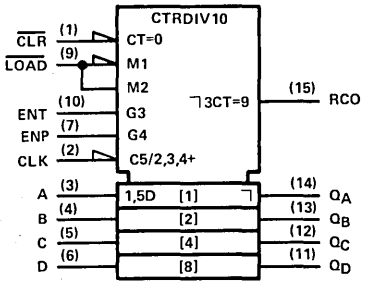
(decade, direct clear)

typical performance

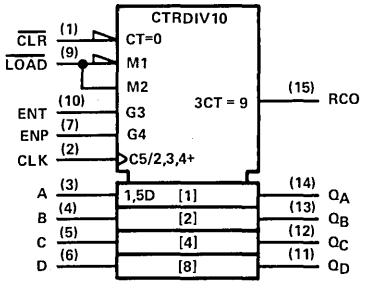
TYPE	COUNT FREQ	CLEAR	TOTAL POWER
'160	25 MHz	ASYNC-L	305 mW
'LS160A	25 MHz	ASYNC-L	93 mW

SN54160 (J,FC) SN74160 (J,N)
SN54LS160A (J,FC) SN74LS160A (J,N)

logic symbol, '160†



logic symbol, 'LS160A†



pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 $\overline{CLR}$	9 $\overline{LOAD}$	1 $\overline{CLR}$	11 $\overline{LOAD}$
2 CLK	10 ENT	2 CLK	12 ENT
3 A	11 QD	3 nc	13 nc
4 B	12 QC	4 nc	14 nc
5 C	13 QB	5 A	15 QD
6 D	14 QA	6 B	16 QC
7 ENP	15 RCO	7 C	17 QB
8 GND	16 V_{CC}	8 D	18 QA
		9 ENP	19 RCO
		10 GND	20 V_{CC}

See *TTL Data Book*

161

SYNCHRONOUS 4-BIT COUNTERS

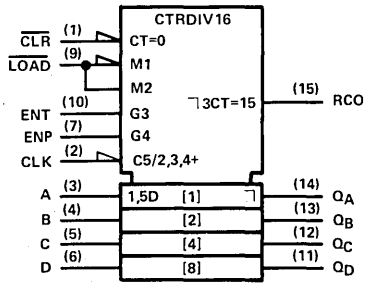
(binary, direct clear)

typical performance

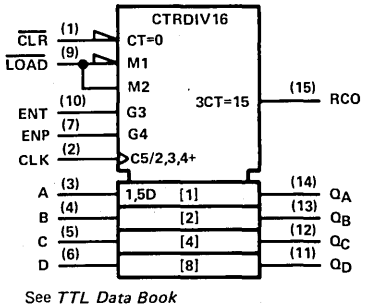
TYPE	COUNT FREQ	CLEAR	TOTAL POWER
'161	25 MHz	ASYNC-L	305 mW
'LS161A	25 MHz	ASYNC-L	93 mW

SN54161 (J,FC) SN74161 (J,N)
SN54LS161A (J,FC) SN74LS161A (J,N)

logic symbol, '161†



logic symbol, 'LS161A†



pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 $\overline{CLR}$	9 $\overline{LOAD}$	1 $\overline{CLR}$	11 $\overline{LOAD}$
2 CLK	10 ENT	2 CLK	12 ENT
3 A	11 QD	3 nc	13 nc
4 B	12 QC	4 nc	14 nc
5 C	13 QB	5 A	15 QD
6 D	14 QA	6 B	16 QC
7 ENP	15 RCO	7 C	17 QB
8 GND	16 V_{CC}	8 D	18 QA
		9 ENP	19 RCO
		10 GND	20 V_{CC}

See *TTL Data Book*

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

8

162

SYNCHRONOUS 4-BIT COUNTERS

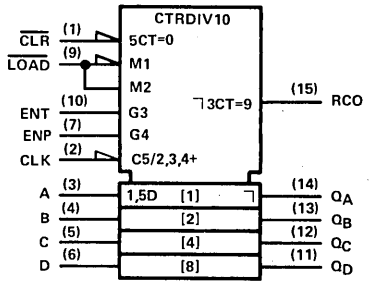
(decade, synchronous clear)

typical performance

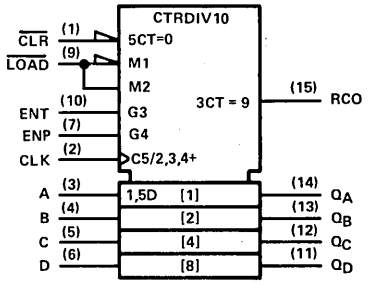
TYPE	COUNT FREQ	CLEAR	TOTAL POWER
'162	25 MHz	SYNC-L	305 mW
'LS162A	25 MHz	SYNC-L	93 mW
'S162	40 MHz	SYNC-L	475 mW

SN54162 (J,FC) SN74162 (J,N)
SN54LS162A (J,FC) SN74LS162A (J,N)
SN54S162 (J,FC) SN74S162 (J,N,FN)

logic symbol, '162†



logic symbol, 'LS162A, 'S162†



pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	$\overline{CLR}$	9	$\overline{LOAD}$	1	$\overline{CLR}$	11	$\overline{LOAD}$
2	CLK	10	ENT	2	CLK	12	ENT
3	A	11	QD	3	nc	13	nc
4	B	12	QC	4	nc	14	nc
5	C	13	QB	5	A	15	QD
6	D	14	QA	6	B	16	QC
7	ENP	15	RCO	7	C	17	QB
8	GND	16	V_{CC}	8	D	18	QA
				9	ENP	19	RCO
				10	GND	20	V_{CC}

See *TTL Data Book*

163

SYNCHRONOUS 4-BIT COUNTERS

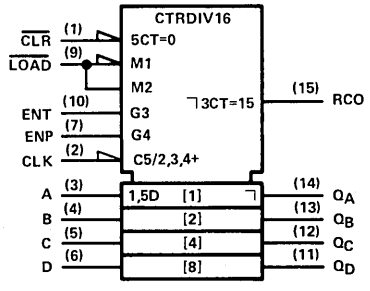
(binary, synchronous clear)

typical performance

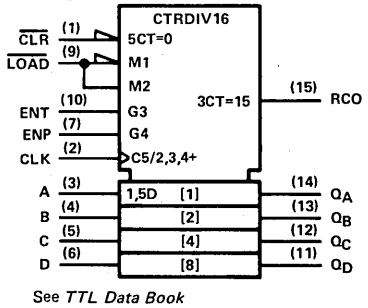
TYPE	COUNT FREQ	CLEAR	TOTAL POWER
'163	25 MHz	SYNC-L	305 mW
'LS163A	25 MHz	SYNC-L	93 mW
'S163	40 MHz	SYNC-L	475 mW

SN54163 (J,FC) SN74163 (J,N)
SN54LS163A (J,FC) SN74LS163A (J,N)
SN54S163 (J,FC) SN74S163 (J,N,FN)

logic symbol, '163†



logic symbol, 'LS163A, 'S163†



pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	$\overline{CLR}$	9	$\overline{LOAD}$	1	$\overline{CLR}$	11	$\overline{LOAD}$
2	CLK	10	ENT	2	CLK	12	ENT
3	A	11	QD	3	nc	13	nc
4	B	12	QC	4	nc	14	nc
5	C	13	QB	5	A	15	QD
6	D	14	QA	6	B	16	QC
7	ENP	15	RCO	7	C	17	QB
8	GND	16	V_{CC}	8	D	18	QA
				9	ENP	19	RCO
				10	GND	20	V_{CC}

See *TTL Data Book*

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

164

8-BIT PARALLEL OUTPUT SERIAL SHIFT REGISTERS

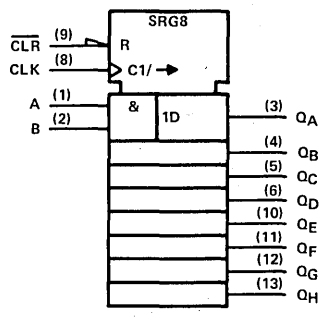
(asynchronous clear)

typical performance

TYPE	SHIFT FREQ	SERIAL DATA INPUT	ASYNC CLEAR	TOTAL POWER
'164	25 MHz	GATED D	LOW	167 mW
'L164	12 MHz	GATED D	LOW	84 mW
'LS164	25 MHz	GATED D	LOW	80 mW

SN54164 (J,FC) SN74164 (J,N)
SN54L164 (J)
SN54LS164 (J,FC) SN74LS164 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	A	8	CLK	1	A	11	CLK
2	B	9	$\overline{CLR}$	2	B	12	nc
3	QA	10	QE	3	nc	13	$\overline{CLR}$
4	QB	11	QF	4	nc	14	QE
5	QC	12	QG	5	QA	15	QF
6	QD	13	QH	6	QB	16	QG
7	GND	14	V_{CC}	7	QC	17	QH
				8	QD	18	nc
				9	nc	19	nc
				10	GND	20	V_{CC}

165

8-BIT SHIFT REGISTERS

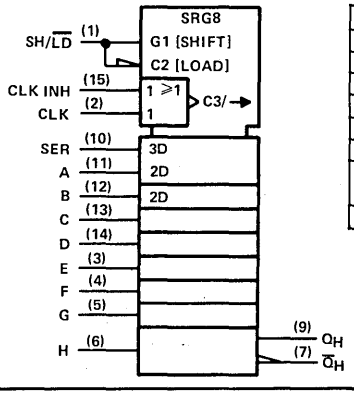
(parallel-load with complementary outputs)

typical performance

TYPE	SHIFT FREQ	SERIAL DATA INPUT	ASYNC CLEAR	TOTAL POWER
'165	25 MHz	D	NONE	210 mW
'LS165	35 MHz	D	NONE	105 mW

SN54165 (J,FC) SN74165 (J,N)
SN54LS165 (J,FC) SN74LS165 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	SH/$\overline{LD}$	9	QH	1	SH/$\overline{LD}$	11	QH
2	CLK	10	SER	2	CLK	12	SER
3	E	11	A	3	nc	13	A
4	F	12	B	4	E	14	B
5	G	13	C	5	F	15	C
6	H	14	D	6	G	16	D
7	$\overline{Q}H$	15	CLK INH	7	H	17	CLK INH
8	GND	16	V_{CC}	8	nc	18	nc
				9	$\overline{Q}H$	19	nc
				10	GND	20	V_{CC}

166

8-BIT SHIFT REGISTERS

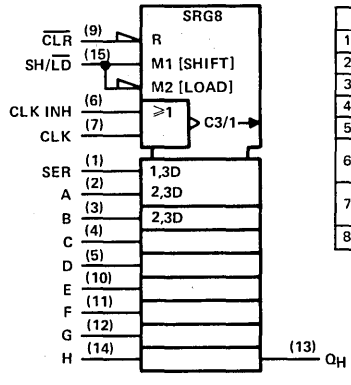
(parallel/serial input; serial output)

typical performance

TYPE	SHIFT FREQ	SERIAL DATA INPUT	ASYNC CLEAR	TOTAL POWER
'166	20 MHz	D	LOW	360 mW
'LS166	35 MHz	D	LOW	110 mW

SN54166 (J,FC) SN74166 (J,N)
SN54LS166 (J,FC) SN74LS166 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	SER	9	$\overline{CLR}$	1	SER	11	$\overline{CLR}$
2	A	10	E	2	nc	12	nc
3	B	11	F	3	A	13	nc
4	C	12	G	4	B	14	E
5	D	13	QH	5	C	15	F
6	CLK INH	14	H	6	D	16	G
7	CLK	15	SH/$\overline{LD}$	7	CLK INH	17	QH
8	GND	16	V_{CC}	8	nc	18	H
				9	CLK	19	SH/$\overline{LD}$
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

167

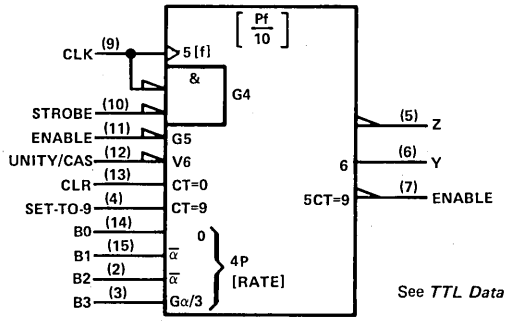
SYNCHRONOUS DECADE RATE MULTIPLIERS

typical performance

TYPE	COUNT FREQ	CLEAR	TOTAL POWER
'167	25 MHz	ASYNC-H	270 mW

SN54167 (J) SN74167 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1 nc		9	CLK
2 B2		10	STRB
3 B3		11	ENin
4	SET-TO-9	12	UNITY/CAS
5 Z		13	CLR
6 Y		14	B0
7 ENout		15	B1
8 GND		16	V_{CC}

See *TTL Data Book*

168

4-BIT UP/DOWN SYNCHRONOUS COUNTERS

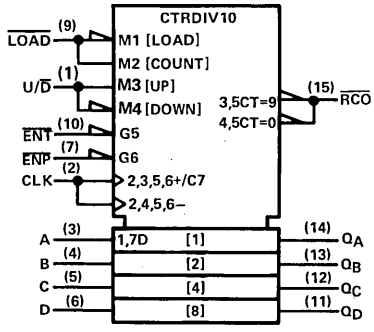
(decade)

typical performance

TYPE	COUNT FREQ	CLEAR	TOTAL POWER
'S168	40 MHz	NONE	500 mW

SN54S168 (J,FC) SN74S168 (J,N)

logic symbol†



pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1 U/$\overline{D}$		9	$\overline{LOAD}$	1 U/$\overline{D}$		11	$\overline{LOAD}$
2 CLK		10	$\overline{ENT}$	2 CLK		12	$\overline{ENT}$
3 A		11	QD	3 nc		13	nc
4 B		12	QC	4 A		14	QD
5 C		13	QB	5 B		15	QC
6 D		14	QA	6 C		16	QB
7 $\overline{ENP}$		15	$\overline{RCO}$	7 D		17	QA
8 GND		16	V_{CC}	8 nc		18	nc
				9 $\overline{ENP}$		19	$\overline{RCO}$
				10 GND		20	V_{CC}

See *TTL Data Book*

169

4-BIT UP/DOWN SYNCHRONOUS COUNTERS

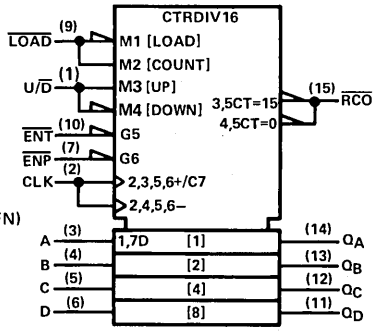
(binary)

typical performance

TYPE	COUNT FREQ	CLEAR	TOTAL POWER
'S169	40 MHz	NONE	500 mW

SN54S169 (J,FC) SN74S169 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1 U/$\overline{D}$		9	$\overline{LOAD}$	1 U/$\overline{D}$		11	$\overline{LOAD}$
2 CLK		10	$\overline{ENT}$	2 CLK		12	$\overline{ENT}$
3 A		11	QD	3 nc		13	nc
4 B		12	QC	4 A		14	QD
5 C		13	QB	5 B		15	QC
6 D		14	QA	6 C		16	QB
7 $\overline{ENP}$		15	$\overline{RCO}$	7 D		17	QA
8 GND		16	V_{CC}	8 nc		18	nc
				9 $\overline{ENP}$		19	$\overline{RCO}$
				10 GND		20	V_{CC}

See *TTL Data Book*

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

170

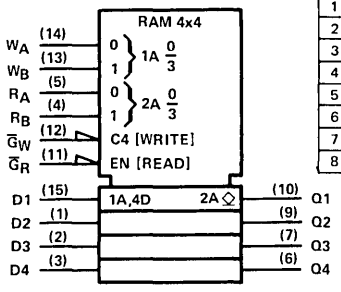
4-BY-4 REGISTER FILES

typical performance

TYPE	TYPE OF OUTPUT	ADDRESS TIME	POWER PER BIT
'170	O-C	30 ns	40 mW
'LS170	O-C	27 ns	7.8 mW

SN54170 (J,FC) SN74170 (J,N)
SN54LS170 (J,FC) SN74LS170 (J,N)

logic symbol†



pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 D2	9 Q2	1 D2	11 Q2
2 D3	10 Q1	2 D3	12 Q1
3 D4	11 $\overline{G}$R	3 nc	13 nc
4 RB	12 $\overline{G}$W	4 D4	14 $\overline{G}$R
5 RA	13 WB	5 RB	15 $\overline{G}$W
6 Q4	14 WA	6 RA	16 WB
7 Q3	15 D1	7 Q4	17 WA
8 GND	16 V_{CC}	8 nc	18 nc
		9 Q3	19 D1
		10 GND	20 V_{CC}

See *TTL Data Book*

172

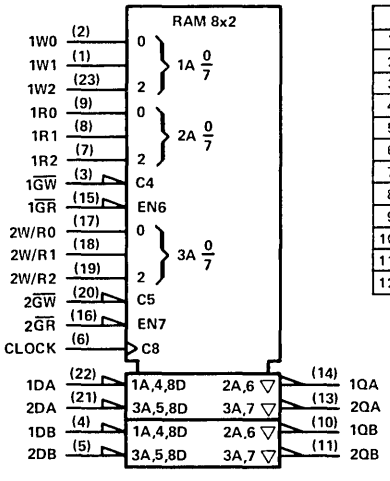
16-BIT REGISTER FILES

typical performance

TYPE	ORG	TYPE OF OUTPUT	ADDRESS TIME	POWER PER BIT
'172	8X2	3-State	33 ns	35 mW

SN74172 (J,N)

logic symbol†



pin assignments

J, N PACKAGES	
1 1W1	13 2QA
2 1W0	14 1QA
3 1$\overline{G}$W	15 1$\overline{G}$R
4 1DB	16 2$\overline{G}$R
5 2DB	17 2W/R0
6 CLK	18 2W/R1
7 1R2	19 2W/R2
8 1R1	20 2$\overline{G}$W
9 1R0	21 2DA
10 1QB	22 1DA
11 2QB	23 1W2
12 GND	24 V_{CC}

See *TTL Data Book*

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

173

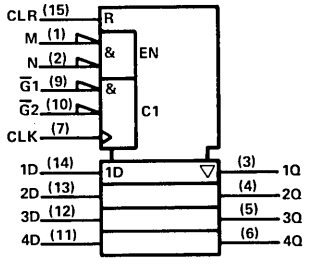
4-BIT D-TYPE REGISTERS
(3-state outputs)
typical performance

TYPE	FREQ	ASYNC CLEAR	TOTAL POWER
'173	25 MHz	HIGH	250 mW
'LS173A	50 MHz	HIGH	85 mW

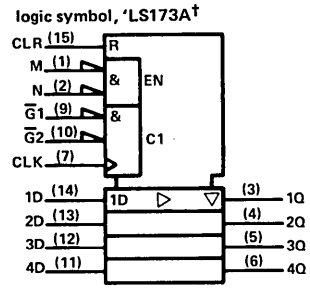
SN54173 (J,FC) SN74173 (J,N)
SN54LS173A (J,FC) SN74LS173A (J,N)

See *TTL Data Book*

logic symbol, '173†



logic symbol, 'LS173A†



pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 M	9 $\overline{G1}$	1 M	11 $\overline{G1}$
2 N	10 $\overline{G2}$	2 N	12 $\overline{G2}$
3 1Q	11 4D	3 nc	13 nc
4 2Q	12 3D	4 1Q	14 4D
5 3Q	13 2D	5 2Q	15 3D
6 4Q	14 1D	6 3Q	16 2D
7 CLK	15 CLR	7 4Q	17 1D
8 GND	16 V_{CC}	8 nc	18 nc
		9 CLK	19 CLR
		10 GND	20 V_{CC}

174

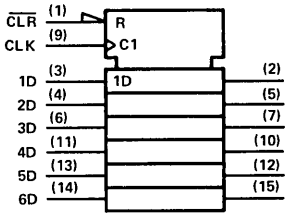
HEX D-TYPE FLIP-FLOPS
(single-rail outputs, common direct clear)
typical performance

TYPE	FREQ	POWER PER F-F	DELAY TIMES	
			SETUP	HOLD
'174	35 MHz	38 mW	20 ns†	5 ns†
'LS174	40 MHz	10.6 mW	20 ns†	5 ns†
'S174	110 MHz	75 mW	5 ns†	3 ns†

† Rising edge of clock pulse

SN54174 (J,FC) SN74174 (J,N)
SN54LS174 (J,FC) SN74LS174 (J,N)
SN54S174 (J,FC) SN74S174 (J,N,FN)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 $\overline{CLR}$	9 CLK	1 $\overline{CLR}$	11 CLK
2 1Q	10 4Q	2 1Q	12 4Q
3 1D	11 4D	3 1D	13 nc
4 2D	12 5Q	4 nc	14 4D
5 2Q	13 5D	5 2D	15 5Q
6 3D	14 6D	6 2Q	16 5D
7 3Q	15 6Q	7 3D	17 6D
8 GND	16 V_{CC}	8 nc	18 nc
		9 3Q	19 6Q
		10 GND	20 V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

175

QUAD D-TYPE FLIP-FLOPS
(complementary outputs, common direct clear)

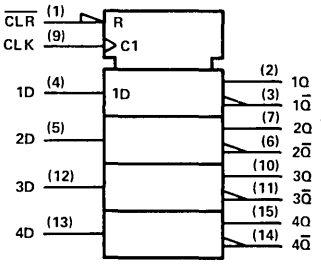
typical performance

TYPE	FREQ	POWER PER F-F	DELAY TIMES SETUP	HOLD
'175	35 MHz	38 mW	20 ns†	5 ns†
'LS175	40 MHz	10.6 mW	20 ns†	5 ns†
'S175	110 MHz	75 mW	5 ns†	3 ns†

† Rising edge of clock pulse

SN54175 (J,FC) SN74175 (J,N)
SN54LS175 (J,FC) SN74LS175 (J,N)
SN54S175 (J,FC) SN74S175 (J,N,FN)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 $\overline{CLR}$	9 CLK	1 $\overline{CLR}$	11 CLK
2 1Q	10 3Q	2 1Q	12 3Q
3 1$\overline{Q}$	11 3$\overline{Q}$	3 nc	13 3$\overline{Q}$
4 1D	12 3D	4 nc	14 nc
5 2D	13 4D	5 1$\overline{Q}$	15 3D
6 2$\overline{Q}$	14 4$\overline{Q}$	6 1D	16 4D
7 2Q	15 4Q	7 2D	17 4$\overline{Q}$
8 GND	16 V_{CC}	8 2$\overline{Q}$	18 nc
		9 2Q	19 4Q
		10 GND	20 V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

8

176

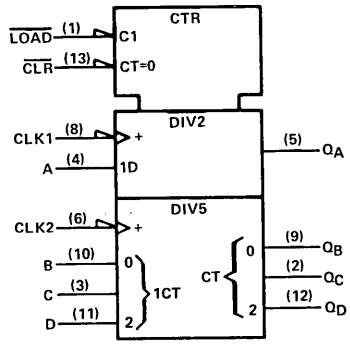
PRESETTABLE DECADE/ BIQUINARY COUNTERS

typical performance

TYPE	COUNT FREQ	CLEAR	TOTAL POWER
'176	35 MHz	LOW	150 mW

SN54176 (J) SN74176 (J,N)

logic symbol, '176†



See *TTL Data Book*

pin assignments

J, N PACKAGES			
1	$\overline{\text{LOAD}}$	8	CLK1
2	QC	9	QB
3	C	10	B
4	A	11	D
5	QA	12	QD
6	CLK2	13	$\overline{\text{CLR}}$
7	GND	14	V_{CC}

177

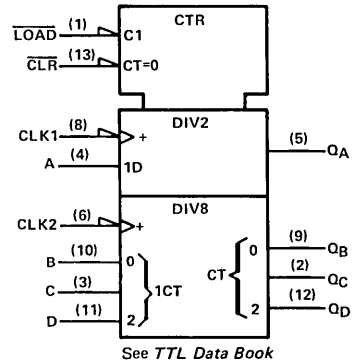
PRESETTABLE BINARY COUNTERS

typical performance

TYPE	COUNT FREQ	CLEAR	TOTAL POWER
'177	35 MHz	LOW	150 mW

SN54177 (J) SN74177 (J,N)

logic symbol, '177†



See *TTL Data Book*

pin assignments

J, N PACKAGES			
1	$\overline{\text{LOAD}}$	8	CLK1
2	QC	9	QB
3	C	10	B
4	A	11	D
5	QA	12	QD
6	CLK2	13	$\overline{\text{CLR}}$
7	GND	14	V_{CC}

178

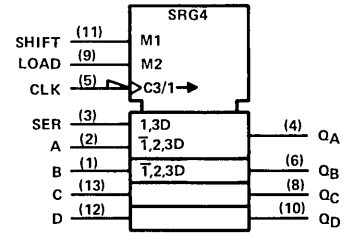
4-BIT UNIVERSAL SHIFT REGISTER

typical performance

TYPE	SHIFT FREQ	SERIAL DATA INPUT	ASYNC CLEAR	TOTAL POWER
'178	25 MHz	D	NONE	230 mW

SN54178 (J,FC) SN74178 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES			
1	B	8	QC
2	A	9	LOAD
3	SER	10	QD
4	QA	11	SHIFT
5	CLK	12	D
6	QB	13	C
7	GND	14	V_{CC}

FC, FN PACKAGES			
1	B	11	QC
2	nc	12	LOAD
3	nc	13	nc
4	A	14	QD
5	SER	15	nc
6	QA	16	SHIFT
7	CLK	17	D
8	nc	18	nc
9	QB	19	C
10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

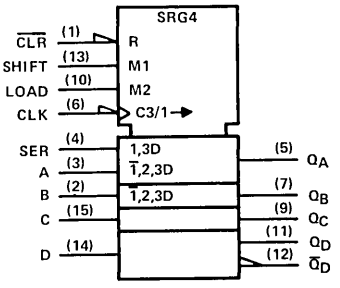
179

4-BIT UNIVERSAL SHIFT REGISTERS
(direct clear; Q_D complementary outputs)
typical performance

TYPE	SHIFT FREQ	SERIAL DATA INPUT	ASYNC CLEAR	TOTAL POWER
'179	25 MHz	D	LOW	230 mW

SN54179 (J,FC) SN74179 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	$\overline{CLR}$	9	QC	1	$\overline{CLR}$	11	QC
2	B	10	LOAD	2	B	12	LOAD
3	A	11	QD	3	nc	13	nc
4	SER	12	$\overline{QD}$	4	A	14	QD
5	QA	13	SHIFT	5	SER	15	$\overline{QD}$
6	CLK	14	D	6	QA	16	SHIFT
7	QB	15	C	7	CLK	17	D
8	GND	16	V_{CC}	8	nc	18	nc
				9	QB	19	C
				10	GND	20	V_{CC}

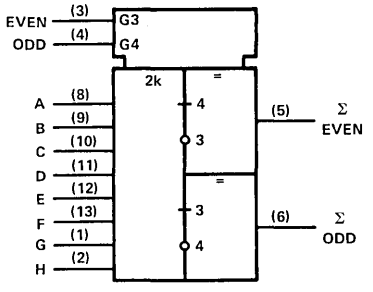
180

9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS
typical performance

TYPE	POWER	DELAY
'180	170 mW	35 ns

SN54180 (J) SN74180 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES			
1	G	8	A
2	H	9	B
3	EVEN	10	C
4	ODD	11	D
5	ΣEVEN	12	E
6	ΣODD	13	F
7	GND	14	V_{CC}

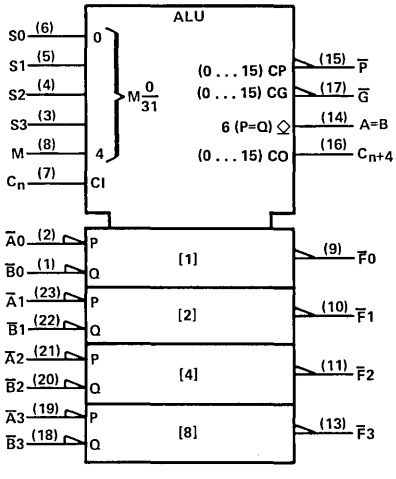
181

ARITHMETIC LOGIC UNITS/ FUNCTION GENERATORS
(16 arithmetic operations, 16 logic functions)
typical performance

TYPE	CARRY TIME	ADD TIME	TOTAL POWER
'181	12.5 ns	24 ns	455 mW
'AS181	6 ns	5 ns	560 mW
'LS181	16 ns	24 ns	102 mW
'S181	7 ns	11 ns	600 mW

SN54181 (J,FC) SN74181 (J,N)
SN54AS181 (J,FC) SN74AS181 (J,N,FN)
SN54LS181 (J,FC) SN74LS181 (J,N)
SN54S181 (J,FC) SN74S181 (J,N,FN)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	$\overline{B}0$	13	$\overline{F}3$	1	$\overline{B}0$	15	$\overline{F}3$
2	$\overline{A}0$	14	A=B	2	$\overline{A}0$	16	A=B
3	S3	15	$\overline{P}$	3	S3	17	nc
4	S2	16	C_{n+4}	4	nc	18	nc
5	S1	17	$\overline{G}$	5	nc	19	$\overline{P}$
6	S0	18	$\overline{B}3$	6	S2	20	C_{n+4}
7	C_n	19	$\overline{A}3$	7	S1	21	$\overline{G}$
8	M	20	$\overline{B}2$	8	S0	22	$\overline{B}3$
9	$\overline{F}0$	21	$\overline{A}2$	9	C_n	23	$\overline{A}3$
10	$\overline{F}1$	22	$\overline{B}1$	10	M	24	$\overline{B}2$
11	$\overline{F}2$	23	$\overline{A}1$	11	$\overline{F}0$	25	$\overline{A}2$
12	GND	24	V_{CC}	12	$\overline{F}1$	26	$\overline{B}1$
				13	$\overline{F}2$	27	$\overline{A}1$
				14	GND	28	V_{CC}

8

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

182

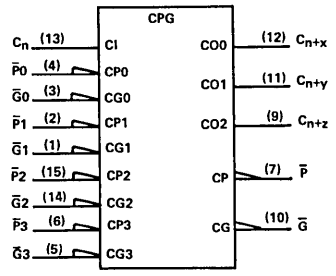
LOOK-AHEAD CARRY GENERATORS

typical performance

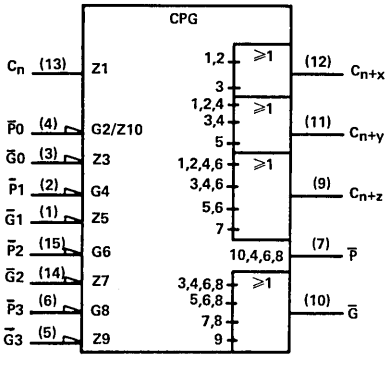
TYPE	POWER	CARRY TIME
'182	180 mW	13 ns
'S182	260 mW	7 ns

SN54182 (J,FC)
SN54S182 (J,FC)
SN74182 (J,N)
SN74S182 (J,N,FN)

logic symbols†



OR



See *TTL Data Book*

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 $\overline{G}1$	9 C_{n+z}	1 $\overline{G}1$	11 C_{n+z}
2 $\overline{P}1$	10 $\overline{G}$	2 $\overline{P}1$	12 $\overline{G}$
3 $\overline{G}0$	11 C_{n+Y}	3 nc	13 nc
4 $\overline{P}0$	12 C_{n+X}	4 $\overline{G}0$	14 C_{n+Y}
5 $\overline{G}3$	13 C_n	5 $\overline{P}0$	15 C_{n+X}
6 $\overline{P}3$	14 $\overline{G}2$	6 $\overline{G}3$	16 C_n
7 $\overline{P}$	15 $\overline{P}2$	7 $\overline{P}3$	17 $\overline{G}2$
8 GND	16 V_{CC}	8 nc	18 nc
		9 $\overline{P}$	19 $\overline{P}2$
		10 GND	20 V_{CC}

183

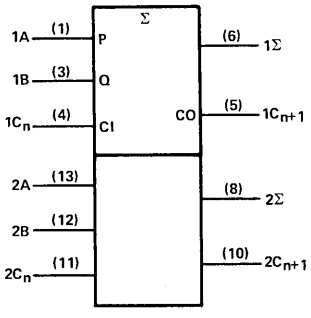
DUAL CARRY-SAVE FULL ADDERS

typical performance

TYPE	CARRY TIME	ADD TIME	POWER PER BIT
'H183	11 ns	11 ns	110 mW
'LS183	15 ns	15 ns	23 mW

SN54H183 (J,FC)
SN54LS183 (J,FC)
SN74H183 (J,N)
SN74LS183 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 1A	8 2Σ	1 1A	11 nc
2 nc	9 nc	2 1B	12 2Σ
3 1B	10 $2C_{n+1}$	3 nc	13 nc
4 $1C_n$	11 $2C_n$	4 nc	14 nc
5 $1C_{n+1}$	12 2B	5 nc	15 $2C_{n+1}$
6 1Σ	13 2A	6 $1C_n$	16 $2C_n$
7 GND	14 V_{CC}	7 $1C_{n+1}$	17 2B
		8 nc	18 nc
		9 1Σ	19 2A
		10 GND	20 V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

184

CODE CONVERTERS

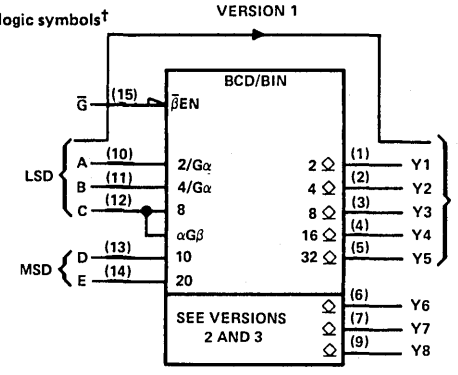
(BCD to binary)

typical performance

TYPE	POWER	DELAY
'184	280 mW	25 ns

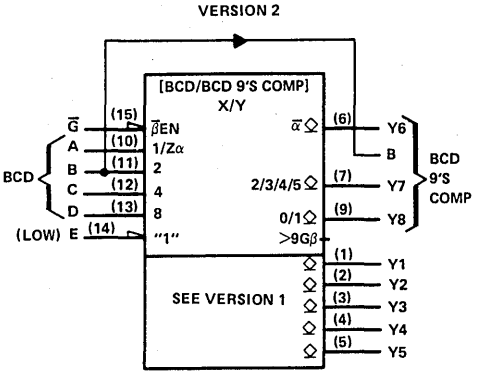
SN54184 (J) SN74184 (J,N)

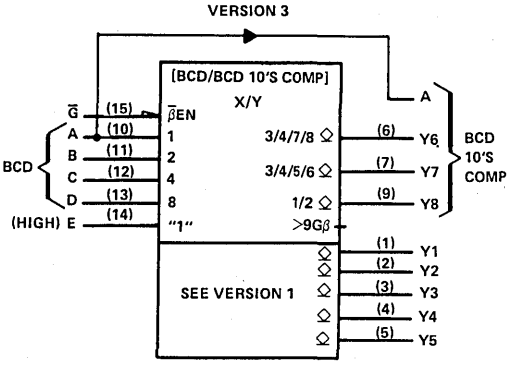
logic symbols†



pin assignments

J, N PACKAGES	
1 Y1	9 Y8
2 Y2	10 A
3 Y3	11 B
4 Y4	12 C
5 Y5	13 D
6 Y6	14 E
7 Y7	15 $\overline{G}$
8 GND	16 V_{CC}





See *TTL Data Book*

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

185

CODE CONVERTERS

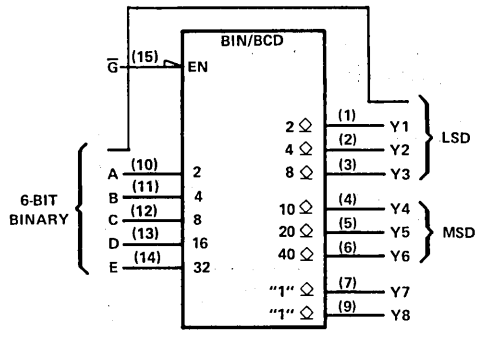
(binary to BCD)

typical performance

TYPE	POWER	DELAY
'185A	280 mW	25 ns

SN54185A (J) SN74185A (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES	
1 Y1	9 Y8
2 Y2	10 A
3 Y3	11 B
4 Y4	12 C
5 Y5	13 D
6 Y6	14 E
7 Y7	15 $\overline{G}$
8 GND	16 V_{CC}

187

1024-BIT READ-ONLY MEMORIES

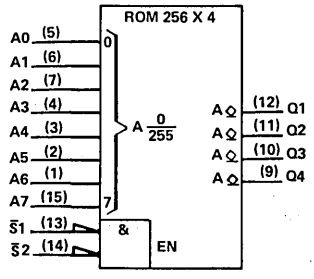
(256 4-bit words; open-collector outputs)

typical performance

TYPE	ACCESS TIMES	
	CHIP-SELECT	ADDRESS
'187	20 ns	40 ns

SN54187 (J,FC) SN74187 (J,N)

logic symbol†



pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 A6	9 Q4	1 A6	11 Q4
2 A5	10 Q3	2 A5	12 Q3
3 A4	11 Q2	3 nc	13 nc
4 A3	12 Q1	4 A4	14 Q2
5 A0	13 $\overline{S}1$	5 A3	15 Q1
6 A1	14 $\overline{S}2$	6 A0	16 $\overline{S}1$
7 A2	15 A7	7 A1	17 $\overline{S}2$
8 GND	16 V_{CC}	8 nc	18 nc
		9 A2	19 A7
		10 GND	20 V_{CC}

188

256-BIT PROGRAMMABLE READ-ONLY MEMORIES

(This number has been changed to TBP18SA030. Product Guide information for this TTL circuit can be found at the end of this section.)

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

189

64-BIT RANDOM-ACCESS MEMORIES

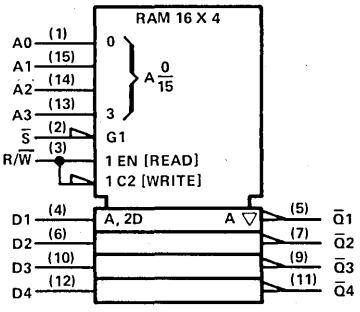
(16 4-bit words; three-state outputs)

typical performance

TYPE	ADDRESS TIME	ENABLE TIME	POWER PER BIT
'LS189A	50 ns	35 ns	2.7 mW
'S189A	25 ns	12 ns	5.9 mW

SN54LS189A (J,FC) SN74LS189A (J,N)
SN54S189A (J,FC) SN74189A (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 A0	9 $\overline{Q3}$	1 A0	11 $\overline{Q3}$
2 $\overline{S}$	10 D3	2 $\overline{S}$	12 D3
3 R/$\overline{W}$	11 $\overline{Q4}$	3 nc	13 nc
4 D1	12 D4	4 R/$\overline{W}$	14 $\overline{Q4}$
5 $\overline{Q1}$	13 A3	5 D1	15 D4
6 D2	14 A2	6 $\overline{Q1}$	16 A3
7 $\overline{Q2}$	15 A1	7 D2	17 A2
8 GND	16 V_{CC}	8 nc	18 nc
		9 $\overline{Q2}$	19 A1
		10 GND	20 V_{CC}

See Pages 2-45 and 2-49

190

SYNCHRONOUS UP/DOWN COUNTERS

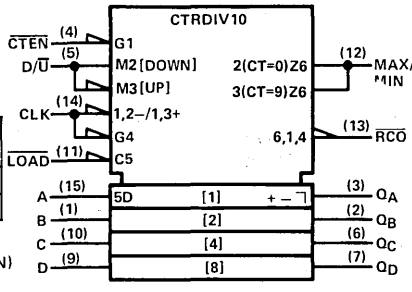
(BCD)

typical performance

TYPE	COUNT FREQ	PARALLEL LOAD	TOTAL POWER
'190	20 MHz	ASYNC	325 mW
'LS190	20 MHz	ASYNC	100 mW

SN54190 (J,FC) SN74190 (J,N)
SN54LS190 (J,FC) SN74LS190 (J,N)

logic symbol†



pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 B	9 D	1 B	11 D
2 QB	10 C	2 QB	12 C
3 QA	11 $\overline{LOAD}$	3 nc	13 $\overline{LOAD}$
4 $\overline{CTEN}$	12 MAX/MIN	4 QA	14 MAX/MIN
5 D/$\overline{U}$	13 $\overline{RCO}$	5 $\overline{CTEN}$	15 $\overline{RCO}$
6 QC	14 CLK	6 D/$\overline{U}$	16 CLK
7 QD	15 A	7 QC	17 nc
8 GND	16 V_{CC}	8 nc	18 nc
		9 QD	19 A
		10 GND	20 V_{CC}

See *TTL Data Book*

191

SYNCHRONOUS UP/DOWN COUNTERS

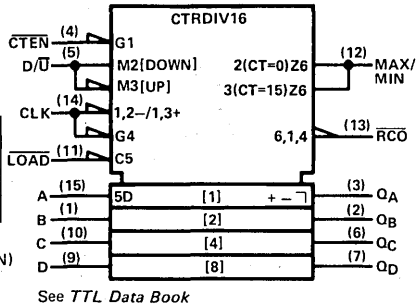
(binary)

typical performance

TYPE	COUNT FREQ	PARALLEL LOAD	TOTAL POWER
'191	20 MHz	ASYNC	325 mW
'LS191	20 MHz	ASYNC	90 mW

SN54191 (J,FC) SN74191 (J,N)
SN54LS191 (J,FC) SN74LS191 (J,N)

logic symbol†



pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 B	9 D	1 B	11 D
2 QB	10 C	2 QB	12 C
3 QA	11 $\overline{LOAD}$	3 nc	13 $\overline{LOAD}$
4 $\overline{CTEN}$	12 MAX/MIN	4 QA	14 MAX/MIN
5 D/$\overline{U}$	13 $\overline{RCO}$	5 $\overline{CTEN}$	15 $\overline{RCO}$
6 QC	14 CLK	6 D/$\overline{U}$	16 CLK
7 QD	15 A	7 QC	17 nc
8 GND	16 V_{CC}	8 nc	18 nc
		9 QD	19 A
		10 GND	20 V_{CC}

See *TTL Data Book*

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

192

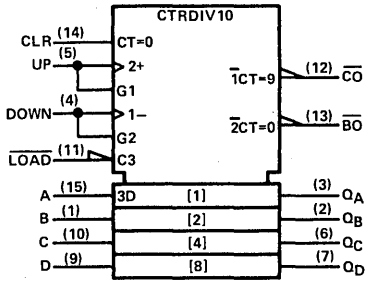
SYNCHRONOUS UP/DOWN DUAL CLOCK COUNTERS
(BCD with clear)

typical performance

TYPE	COUNT FREQ	PARALLEL LOAD	TOTAL POWER
'192	25 MHz	ASYNC	325 mW
'L192	3 MHz	ASYNC	42 mW
'LS192	25 MHz	ASYNC	85 mW

SN54192 (J,FC) SN74192 (J,N)
SN54L192 (J)
SN54LS192 (J,FC) SN74LS192 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES	
1 B	9 D			1 B	11 D
2 QB	10 C			2 QB	12 C
3 QA	11 $\overline{LOAD}$			3 nc	13 $\overline{LOAD}$
4 DOWN	12 $\overline{CO}$			4 nc	14 $\overline{CO}$
5 UP	13 $\overline{BO}$			5 QA	15 $\overline{BO}$
6 QC	14 CLR			6 DOWN	16 CLR
7 QD	15 A			7 UP	17 nc
8 GND	16 V_{CC}			8 QC	18 nc
				9 QD	19 A
				10 GND	20 V_{CC}

193

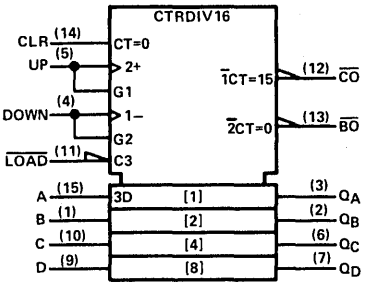
SYNCHRONOUS UP/DOWN DUAL CLOCK COUNTERS
(binary with clear)

typical performance

TYPE	COUNT FREQ	PARALLEL LOAD	TOTAL POWER
'193	25 MHz	ASYNC	325 mW
'L193	3 MHz	ASYNC	42 mW
'LS193	25 MHz	ASYNC	85 mW

SN54193 (J,FC) SN74193 (J,N)
SN54L193 (J)
SN54LS193 (J,FC) SN74LS193 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES	
1 B	9 D			1 B	11 D
2 QB	10 C			2 QB	12 C
3 QA	11 $\overline{LOAD}$			3 nc	13 $\overline{LOAD}$
4 DOWN	12 $\overline{CO}$			4 nc	14 $\overline{CO}$
5 UP	13 $\overline{BO}$			5 QA	15 $\overline{BO}$
6 QC	14 CLR			6 DOWN	16 CLR
7 QD	15 A			7 UP	17 nc
8 GND	16 V_{CC}			8 QC	18 nc
				9 QD	19 A
				10 GND	20 V_{CC}

194

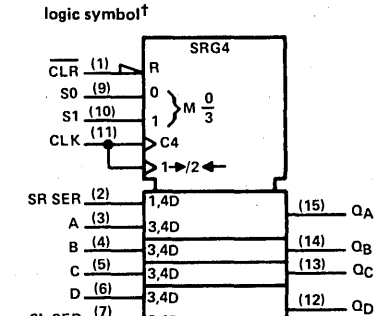
4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

typical performance

TYPE	SHIFT FREQ	SERIAL DATA INPUT	TOTAL POWER
'194	25 MHz	D	195 mW
'LS194A	25 MHz	D	75 mW
'S194	70 MHz	D	450 mW

SN54194 (J,FC) SN74194 (J,N,FN)
SN54LS194A (J,FC) SN74LS194A (J,N)
SN54S194 (J,FC) SN74S194 (J,N,FN)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES	
1 $\overline{CLR}$	9 S0			1 nc	11 S0
2 SR SER	10 S1			2 $\overline{CLR}$	12 S1
3 A	11 CLK			3 SR SER	13 nc
4 B	12 QD			4 A	14 CLK
5 C	13 QC			5 B	15 QD
6 D	14 QB			6 C	16 QC
7 SL SER	15 QA			7 D	17 QB
8 GND	16 V_{CC}			8 nc	18 nc
				9 SL SER	19 QA
				10 GND	20 V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

195

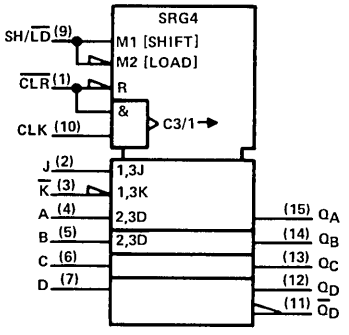
4-BIT PARALLEL-ACCESS SHIFT REGISTERS

typical performance

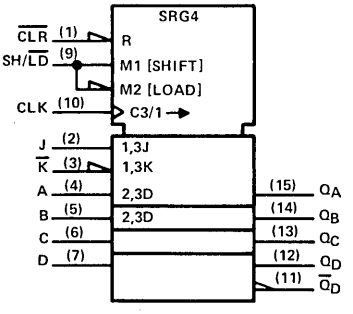
TYPE	SHIFT FREQ	SERIAL DATA INPUT	TOTAL POWER
'195	30 MHz	J-$\overline{K}$	195 mW
'LS195A	30 MHz	J-$\overline{K}$	70 mW
'S195	70 MHz	J-$\overline{K}$	375 mW

SN54195 (J,FC) SN74195 (J,N)
SN54LS195A (J,FC) SN74LS195A (J,N)
SN54S195 (J,FC) SN74S195 (J,N,FN)

logic symbol, '195†



logic symbol, 'LS195A, 'S195†



See *TTL Data Book*

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 $\overline{CLR}$	9 SH/$\overline{LD}$	1 $\overline{CLR}$	11 SH/$\overline{LD}$
2 J	10 CLK	2 nc	12 CLK
3 $\overline{K}$	11 $\overline{QD}$	3 J	13 nc
4 A	12 QD	4 $\overline{K}$	14 $\overline{QD}$
5 B	13 QC	5 A	15 QD
6 C	14 QB	6 B	16 QC
7 D	15 QA	7 C	17 QB
8 GND	16 V_{CC}	8 nc	18 nc
		9 D	19 QA
		10 GND	20 V_{CC}

196

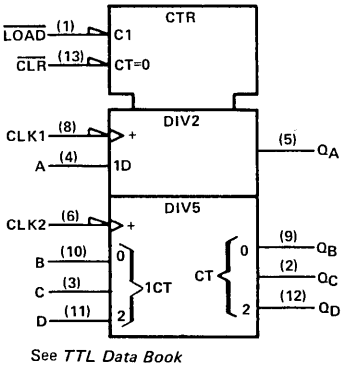
PRESETTABLE DECADE/ BIQUINARY COUNTERS/ LATCHES

typical performance

TYPE	COUNT FREQ	PARALLEL LOAD	CLEAR	TOTAL POWER
'196	50 MHz	YES	LOW	240 mW
'LS196	30 MHz	YES	LOW	60 mW
'S196	100 MHz	YES	LOW	375 mW

SN54196 (J,FC) SN74196 (J,N)
SN54LS196 (J,FC) SN74LS196 (J,N)
SN54S196 (J,FC) SN74S196 (J,N,FN)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 $\overline{LOAD}$	8 CLK1	1 $\overline{LOAD}$	11 CLK1
2 QC	9 QB	2 QC	12 QB
3 C	10 B	3 nc	13 nc
4 A	11 D	4 nc	14 nc
5 QA	12 QD	5 C	15 B
6 CLK2	13 $\overline{CLR}$	6 A	16 D
7 GND	14 V_{CC}	7 QA	17 QD
		8 nc	18 nc
		9 CLK2	19 $\overline{CLR}$
		10 GND	20 V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

197

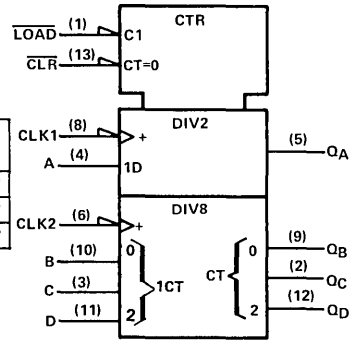
PRESETTABLE BINARY COUNTERS/LATCHES

typical performance

TYPE	COUNT FREQ	PARALLEL LOAD	CLEAR	TOTAL POWER
'197	50 MHz	YES	LOW	240 mW
'LS197	30 MHz	YES	LOW	60 mW
'S197	100 MHz	YES	LOW	375 mW

SN54197 (J,FC) SN74197 (J,N)
SN54LS197 (J,FC) SN74LS197 (J,N)
SN54S197 (J,FC) SN74S197 (J,N,FN)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 $\overline{LOAD}$	8 CLK1	1 $\overline{LOAD}$	11 CLK1
2 QC	9 QB	2 QC	12 QB
3 C	10 B	3 nc	13 nc
4 A	11 D	4 nc	14 nc
5 QA	12 QD	5 C	15 B
6 CLK2	13 $\overline{CLR}$	6 A	16 D
7 GND	14 V_{CC}	7 QA	17 QD
		8 nc	18 nc
		9 CLK2	19 $\overline{CLR}$
		10 GND	20 V_{CC}

198

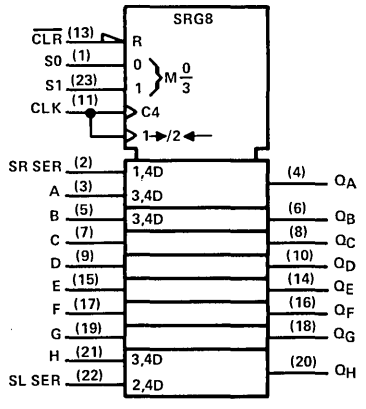
8-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

typical performance

TYPE	SHIFT FREQ	SERIAL DATA INPUT	ASYNC CLEAR	TOTAL POWER
'198	25 MHz	D	LOW	360 mW

SN54198 (J) SN74198 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES	
1 S0	13 $\overline{CLR}$
2 SR SER	14 QE
3 A	15 E
4 QA	16 QF
5 B	17 F
6 QB	18 QG
7 C	19 G
8 QC	20 QH
9 D	21 H
10 QD	22 SL SER
11 CLK	23 S1
12 GND	24 V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

199

8-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

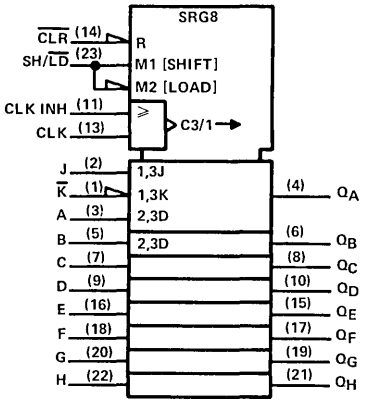
(J-$\overline{K}$ serial inputs)

typical performance

TYPE	SHIFT FREQ	SERIAL DATA INPUT	ASYNC CLEAR	TOTAL POWER
'199	25 MHz	J-$\overline{K}$	LOW	360 mW

SN54199 (J) SN74199 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES	
1 $\overline{K}$	13 CLK
2 J	14 $\overline{CLR}$
3 A	15 QE
4 QA	16 E
5 B	17 QF
6 QB	18 F
7 C	19 QG
8 QC	20 G
9 D	21 QH
10 QD	22 H
11 CLK INH	23 SH/$\overline{LD}$
12 GND	24 V_{CC}

201

256-BIT RANDOM-ACCESS MEMORIES

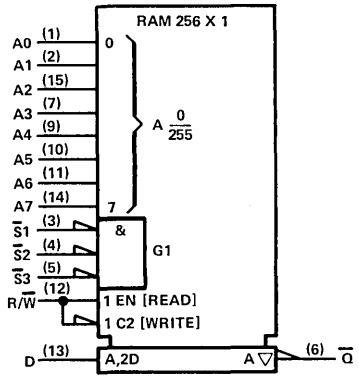
(256 1-bit words; three-state output)

typical performance

TYPE	ADDRESS TIME	ENABLE TIME	POWER/ BIT
'S201	42 ns	17 ns	1.9 mW

SN74S201 (J,N)

logic symbol†



See Page 2-53

pin assignments

J, N PACKAGES	
1 A0	9 A4
2 A1	10 A5
3 $\overline{S1}$	11 A6
4 $\overline{S2}$	12 R/$\overline{W}$
5 $\overline{S3}$	13 D
6 $\overline{Q}$	14 A7
7 A3	15 A2
8 GND	16 V_{CC}

219

64-BIT RANDOM-ACCESS MEMORIES

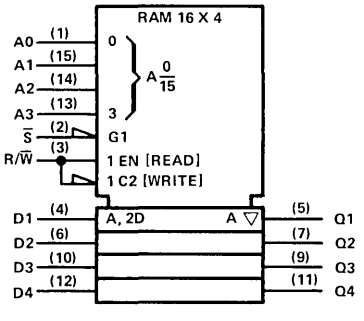
(16 words of 4 bits each; three-state non-inverting output)

typical performance

TYPE	ADDRESS TIME	ENABLE TIME	POWER/ BIT
'LS219A	50 ns	35 ns	2.7 mW

SN54LS219A (J,FC) SN74LS219A (J,N)

logic symbol†



See Page 2-45

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 A0	9 Q3	1 A0	11 Q3
2 $\overline{S}$	10 D3	2 $\overline{S}$	12 D3
3 R/$\overline{W}$	11 Q4	3 nc	13 nc
4 D1	12 D4	4 R/$\overline{W}$	14 Q4
5 Q1	13 A3	5 D1	15 D4
6 D2	14 A2	6 Q1	16 A3
7 Q2	15 A1	7 D2	17 A2
8 GND	16 V_{CC}	8 nc	18 nc
		9 Q2	19 A1
		10 GND	20 V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

8

221

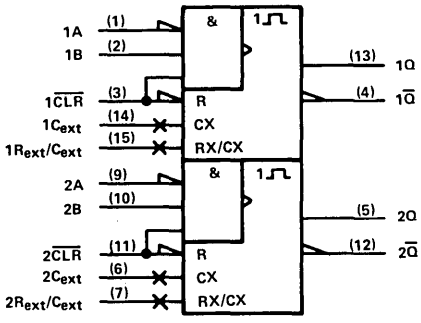
DUAL MONOSTABLE MULTIVIBRATORS

typical performance

TYPE	OUTPUT PULSE RANGE	TOTAL POWER
SN54221	20 ns - 21s	130 mW
SN74221	20 ns - 28s	130 mW
SN54LS221	20 ns - 49s	23 mW
SN74LS221	20 ns - 70 s	23 mW

SN54221 (J,FC) SN74221 (J,N)
SN54LS221 (J,FC) SN74LS221 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 1A	9 2A	1 1A	11 2A
2 1B	10 2B	2 1B	12 2B
3 1CLR	11 2CLR	3 nc	13 nc
4 1Q̄	12 2Q̄	4 1CLR	14 nc
5 2Q	13 1Q	5 1Q̄	15 2CLR
6 2Cext	14 1Cext	6 2Q	16 2Q̄
7 2Rext/Cext	15 1Rext/Cext	7 2Cext	17 1Q
8 GND	16 VCC	8 nc	18 1Cext
		9 2Rext/Cext	19 1Rext/Cext
		10 GND	20 VCC

222

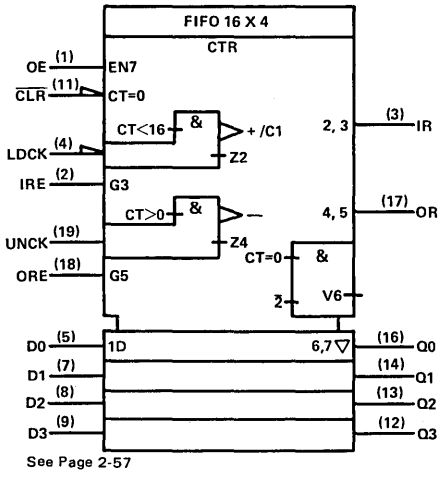
64-BIT FIFO MEMORIES
16 4-BIT WORDS
(input-ready enable, output-ready enable, and three-state output)

typical performance

TYPE	DELAY TIME FROM CLOCK	TOTAL POWER
'LS222	47 ns	433 mW

SN54LS222 (J,FC) SN74LS222 (J,N)

logic symbol†



See Page 2-57

pin assignments

J, N PACKAGES	
1 OE	11 CLR
2 IRE	12 Q3
3 IR	13 Q2
4 LDCK	14 Q1
5 D0	15 nc
6 nc	16 Q0
7 D1	17 OR
8 D2	18 ORE
9 D3	19 UNCK
10 GND	20 VCC

FC, FN PACKAGES	
1 OE	15 CLR
2 IRE	16 Q3
3 IR	17 Q2
4 nc	18 nc
5 LDCK	19 nc
6 D0	20 Q1
7 nc	21 nc
8 nc	22 nc
9 nc	23 Q0
10 D1	24 OR
11 nc	25 nc
12 D2	26 ORE
13 D3	27 UNCK
14 GND	28 VCC

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

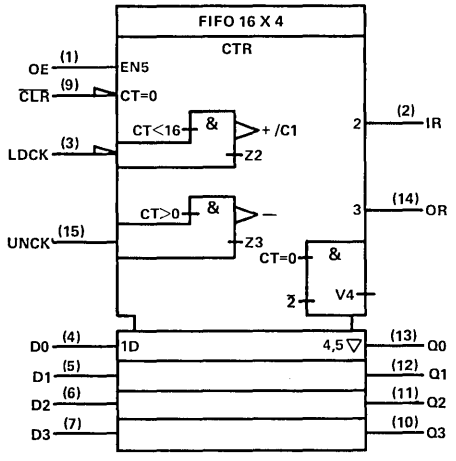
224

64-BIT FIFO MEMORIES
16 4-BIT WORDS
(three-state output)
typical performance

TYPE	DELAY TIME FROM CLOCK	TOTAL POWER
'LS224	47 ns	433 mW

SN54LS224 (J,FC) SN74LS224 (J,N)

logic symbol†



See Page 2-57

pin assignments

J, N PACKAGES	
1 OE	9 $\overline{CLR}$
2 IR	10 Q3
3 LDCK	11 Q2
4 D0	12 Q1
5 D1	13 Q0
6 D2	14 OR
7 D3	15 UNCK
8 GND	16 V_{CC}

FC, FN PACKAGES	
1 OE	15 $\overline{CLR}$
2 nc	16 Q3
3 IR	17 Q2
4 nc	18 nc
5 LDCK	19 nc
6 D0	20 Q1
7 nc	21 nc
8 nc	22 nc
9 nc	23 Q0
10 D1	24 OR
11 nc	25 nc
12 D2	26 nc
13 D3	27 UNCK
14 GND	28 V_{CC}

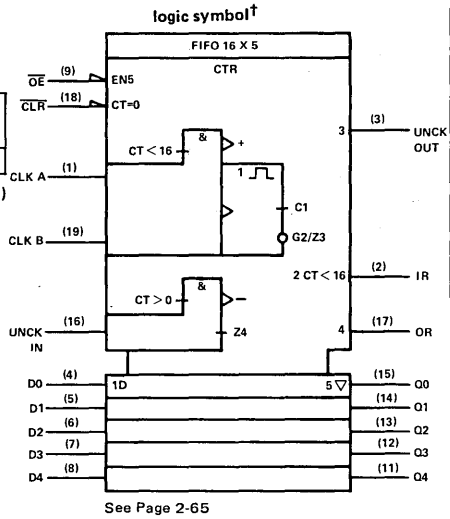
225

80-BIT FIFO MEMORIES
16 5-BIT WORDS
typical performance

OUTPUT	DELAY TIME FROM CLOCK	TOTAL POWER
3-State	50 ns	400 mW

SN74S225 (J,N,FN)

logic symbol†



See Page 2-65

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 CLKA	11 Q4	1 CLKA	11 Q4
2 IR	12 Q3	2 IR	12 Q3
3 UNCK OUT	13 Q2	3 UNCK OUT	13 Q2
4 D0	14 Q1	4 D0	14 Q1
5 D1	15 Q0	5 D1	15 Q0
6 D2	16 UNCK IN	6 D2	16 UNCK IN
7 D3	17 OR	7 D3	17 OR
8 D4	18 $\overline{CLR}$	8 D4	18 $\overline{CLR}$
9 $\overline{OE}$	19 CLKB	9 $\overline{OE}$	19 CLKB
10 GND	20 V_{CC}	10 GND	20 V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

8

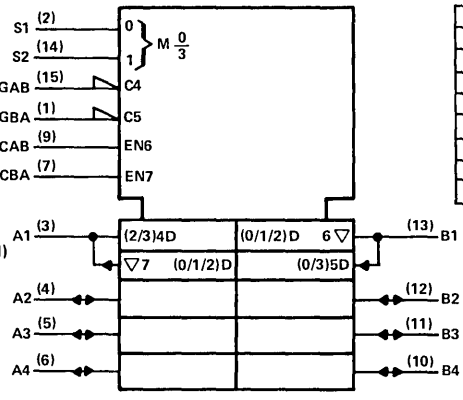
226

4-BIT PARALLEL LATCHED BUS TRANSCEIVERS
(three-state outputs)
typical performance

TYPE	MAX SOURCE CURRENT	MAX SINK CURRENT
'S226	−6.5 mA	20 mA

SN54S226 (J,FC) SN74S226 (J,N,FN)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 GBA	9 OCAB	1 GBA	15 OCAB
2 S1	10 B4	2 nc	16 B4
3 A1	11 B3	3 S1	17 nc
4 A2	12 B2	4 nc	18 nc
5 A3	13 B1	5 nc	19 nc
6 A4	14 S2	6 A1	20 B3
7 OCBA	15 GAB	7 A2	21 B2
8 GND	16 V_{CC}	8 A3	22 B1
		9 A4	23 nc
		10 nc	24 S2
		11 nc	25 nc
		12 nc	26 nc
		13 OCBA	27 GAB
		14 GND	28 V_{CC}

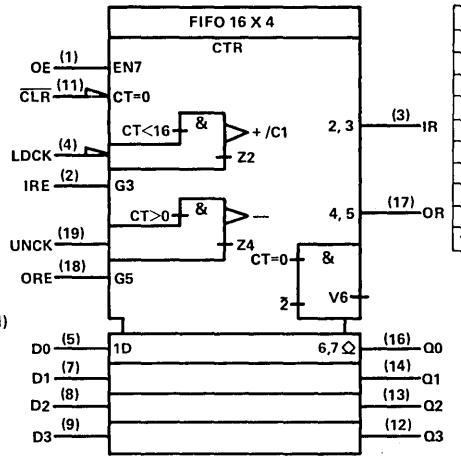
227

64-BIT FIFO MEMORIES
16 4-BIT WORDS
(input-ready enable, output-ready enable, open-collector outputs)
typical performance

TYPE	DELAY TIME FROM CLOCK	TOTAL POWER
'LS227	57.5 ns	433 mW

SN54LS227 (J,FC) SN74LS227 (J,N)

logic symbol†



See Page 2-57

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 OE	11 $\overline{CLR}$	1 OE	15 $\overline{CLR}$
2 IRE	12 Q3	2 IRE	16 Q3
3 IR	13 Q2	3 IR	17 Q2
4 LDCK	14 Q1	4 nc	18 nc
5 D0	15 nc	5 LDCK	19 nc
6 nc	16 Q0	6 D0	20 Q1
7 D1	17 OR	7 nc	21 nc
8 D2	18 ORE	8 nc	22 nc
9 D3	19 UNCK	9 nc	23 Q0
10 GND	20 V_{CC}	10 D1	24 OR
		11 nc	25 nc
		12 D2	26 ORE
		13 D3	27 UNCK
		14 GND	28 V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

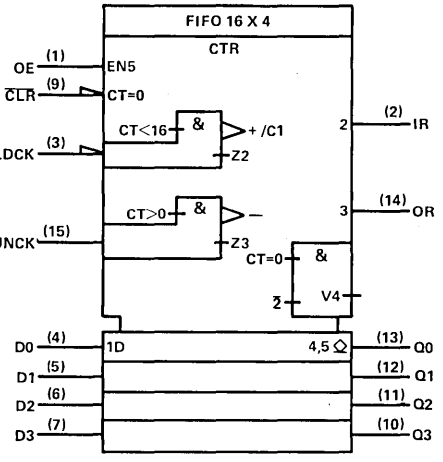
228

64-BIT FIFO MEMORIES
16 4-BIT WORDS
(open-collector outputs)
typical performance

TYPE	DELAY TIME FROM CLOCK	TOTAL POWER
'LS228	57.5 ns	433 mW

SN54LS228 (J,FC) SN74LS228 (J,N)

logic symbol†



See Page 2-57

pin assignments

J, N PACKAGES				FC, FN PACKAGES	
1 OE	9 $\overline{CLR}$			1 OE	15 $\overline{CLR}$
2 IR	10 Q3			2 nc	16 Q3
3 LDCK	11 Q2			3 IR	17 Q2
4 D0	12 Q1			4 nc	18 nc
5 D1	13 Q0			5 LDCK	19 nc
6 D2	14 OR			6 D0	20 Q1
7 D3	15 UNCK			7 nc	21 nc
8 GND	16 V_{CC}			8 nc	22 nc
				9 nc	23 Q0
				10 D1	24 OR
				11 nc	25 nc
				12 D2	26 nc
				13 D3	27 UNCK
				14 GND	28 V_{CC}

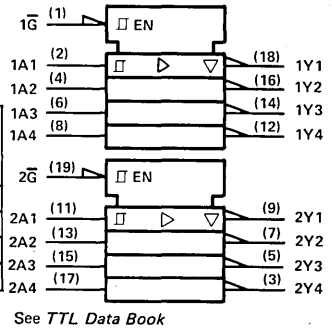
240

OCTAL BUFFERS/LINE
DRIVERS/LINE RECEIVERS
(inverted three-state outputs)
typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54LS240	10 ns	−12 mA	12 mA
SN74LS240	10 ns	−15 mA	24 mA
SN54S240	5 ns	−12 mA	48 mA
SN74S240	5 ns	−15 mA	64 mA

SN54LS240 (J,FC) SN74LS240 (J,N)
SN54S240 (J,FC) SN74S240 (J,N,FN)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES	
1 1$\overline{G}$	11 2A1			1 1$\overline{G}$	11 2A1
2 1A1	12 1Y4			2 1A1	12 1Y4
3 2Y4	13 2A2			3 2Y4	13 2A2
4 1A2	14 1Y3			4 1A2	14 1Y3
5 2Y3	15 2A3			5 2Y3	15 2A3
6 1A3	16 1Y2			6 1A3	16 1Y2
7 2Y2	17 2A4			7 2Y2	17 2A4
8 1A4	18 1Y1			8 1A4	18 1Y1
9 2Y1	19 2$\overline{G}$			9 2Y1	19 2$\overline{G}$
10 GND	20 V_{CC}			10 GND	20 V_{CC}

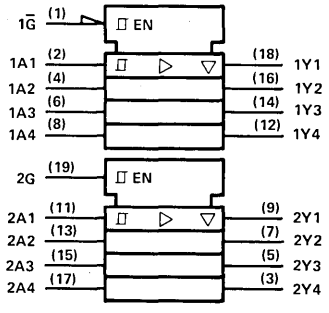
241

OCTAL BUFFERS/LINE
DRIVERS/LINE RECEIVERS
(non-inverted three-state outputs)
typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54LS241	10 ns	−12 mA	12 mA
SN74LS241	10 ns	−15 mA	24 mA
SN54S241	5 ns	−12 mA	48 mA
SN74S241	5 ns	−15 mA	64 mA

SN54LS241 (J,FC) SN74LS241 (J,N)
SN54S241 (J,FC) SN74S241 (J,N,FN)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES	
1 1$\overline{G}$	11 2A1			1 1$\overline{G}$	11 2A1
2 1A1	12 1Y4			2 1A1	12 1Y4
3 2Y4	13 2A2			3 2Y4	13 2A2
4 1A2	14 1Y3			4 1A2	14 1Y3
5 2Y3	15 2A3			5 2Y3	15 2A3
6 1A3	16 1Y2			6 1A3	16 1Y2
7 2Y2	17 2A4			7 2Y2	17 2A4
8 1A4	18 1Y1			8 1A4	18 1Y1
9 2Y1	19 2G			9 2Y1	19 2G
10 GND	20 V_{CC}			10 GND	20 V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

8

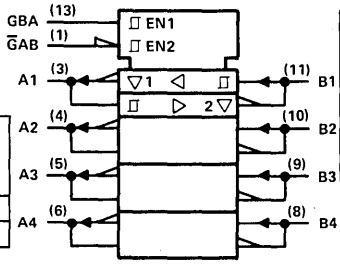
242

QUADRUPLE BUS TRANSCEIVERS
(inverted three-state outputs)
typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54LS242	11 ns	−12 mA	12 mA
SN74LS242	11 ns	−15 mA	24 mA

SN54LS242 (J,FC) SN74LS242 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES	
1	GAB	8	B4	1 nc	11 B4
2	nc	9	B3	2 GAB	12 nc
3	A1	10	B2	3 nc	13 nc
4	A2	11	B1	4 nc	14 nc
5	A3	12	nc	5 A1	15 B3
6	A4	13	GBA	6 A2	16 B2
7	GND	14	V_{CC}	7 A3	17 B1
				8 nc	18 nc
				9 A4	19 GBA
				10 GND	20 V_{CC}

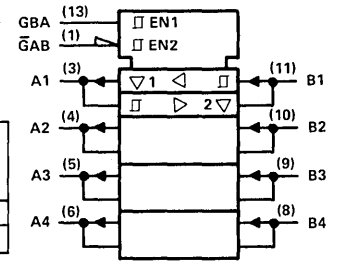
243

QUADRUPLE BUS TRANSCEIVERS
(non-inverted three-state outputs)
typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54LS243	12 ns	−12 mA	12 mA
SN74LS243	12 ns	−15 mA	24 mA

SN54LS243 (J,FC) SN74LS243 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES	
1	GAB	8	B4	1 nc	11 B4
2	nc	9	B3	2 GAB	12 nc
3	A1	10	B2	3 nc	13 nc
4	A2	11	B1	4 nc	14 nc
5	A3	12	nc	5 A1	15 B3
6	A4	13	GBA	6 A2	16 B2
7	GND	14	V_{CC}	7 A3	17 B1
				8 nc	18 nc
				9 A4	19 GBA
				10 GND	20 V_{CC}

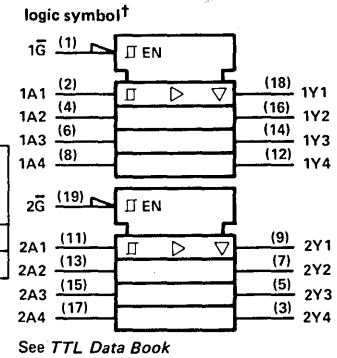
244

OCTAL BUFFERS/LINE DRIVERS/LINE RECEIVERS
(non-inverted three-state outputs)
typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54LS244	10 ns	−12 mA	12 mA
SN74LS244	10 ns	−15 mA	24 mA

SN54LS244 (J,FC) SN74LS244 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES	
1	1G	11	2A1	1 1G	11 2A1
2	1A1	12	1Y4	2 1A1	12 1Y4
3	2Y4	13	2A2	3 2Y4	13 2A2
4	1A2	14	1Y3	4 1A2	14 1Y3
5	2Y3	15	2A3	5 2Y3	15 2A3
6	1A3	16	1Y2	6 1A3	16 1Y2
7	2Y2	17	2A4	7 2Y2	17 2A4
8	1A4	18	1Y1	8 1A4	18 1Y1
9	2Y1	19	2G	9 2Y1	19 2G
10	GND	20	V_{CC}	10 GND	20 V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

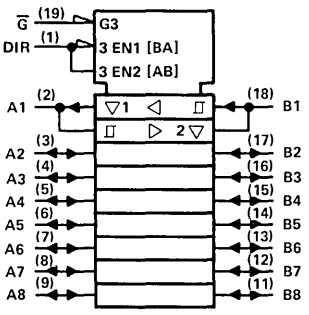
245

OCTAL BUS TRANSCEIVERS
(non-inverted three-state outputs)
typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54LS245	12 ns	−12 mA	12 mA
SN74LS245	12 ns	−15 mA	24 mA

SN54LS245 (J,FC) SN74LS245 (J,N)

logic symbol†



See *TTL Data Book*

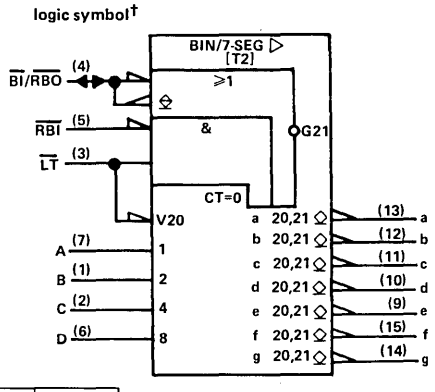
pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	DIR	11	B8	1	DIR	11	B8
2	A1	12	B7	2	A1	12	B7
3	A2	13	B6	3	A2	13	B6
4	A3	14	B5	4	A3	14	B5
5	A4	15	B4	5	A4	15	B4
6	A5	16	B3	6	A5	16	B3
7	A6	17	B2	7	A6	17	B2
8	A7	18	B1	8	A7	18	B1
9	A8	19	$\overline{G}$	9	A8	19	$\overline{G}$
10	GND	20	V_{CC}	10	GND	20	V_{CC}

246
247

BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS WITH RIPPLE BLANKING
(246-active-low, open-collector, 30-volt outputs)
(247-active-low, open-collector, 15-volt outputs)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	B	9	e	1	B	11	e
2	C	10	d	2	C	12	d
3	$\overline{LT}$	11	c	3	nc	13	nc
4	$\overline{BI}/\overline{RBO}$	12	b	4	$\overline{LT}$	14	c
5	$\overline{RBI}$	13	a	5	$\overline{BI}/\overline{RBO}$	15	b
6	D	14	g	6	$\overline{RBI}$	16	a
7	A	15	f	7	D	17	g
8	GND	16	V_{CC}	8	nc	18	nc
				9	A	19	f
				10	GND	20	V_{CC}

typical performance

TYPE	OUTPUT SINK CURRENT	OFF-STATE OUTPUT VOLTAGE	TOTAL POWER
'246	40 mA	30 V	320 mW
'247	40 mA	15 V	320 mW
SN54LS247	12 mA	15 V	35 mW
SN74LS247	24 mA	15 V	35 mW

SN54246 (J,FC) SN74246 (J,N)
SN54247 (J,FC) SN74247 (J,N)
SN54LS247 (J,FC) SN74LS247 (J,N)

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

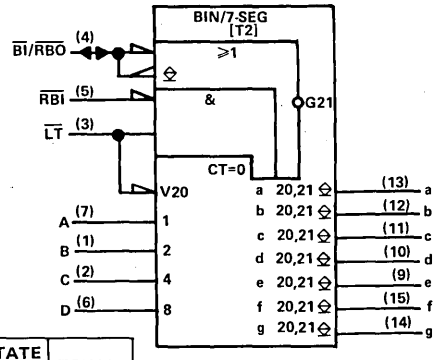
FONT TABLE T2 — RESULTANT DISPLAYS USING '246 AND '247

8

248

BCD-TO-SEVEN SEGMENT DECODERS/DRIVERS
(internal pull-up outputs)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	B	9	e	1	B	11	e
2	C	10	d	2	C	12	d
3	$\overline{LT}$	11	c	3	nc	13	nc
4	$\overline{BI}$/$\overline{RBO}$	12	b	4	$\overline{LT}$	14	c
5	$\overline{RBI}$	13	a	5	$\overline{BI}$/$\overline{RBO}$	15	b
6	D	14	g	6	$\overline{RBI}$	16	a
7	A	15	f	7	D	17	g
8	GND	16	V_{CC}	8	nc	18	nc
				9	A	19	f
				10	GND	20	V_{CC}

typical performance

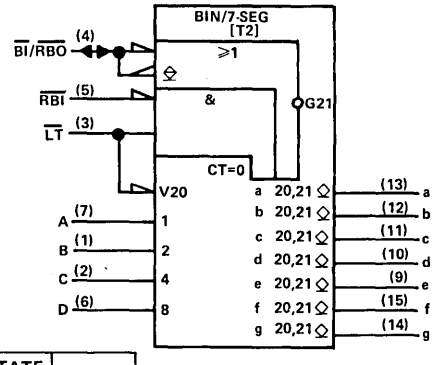
TYPE	OUTPUT SINK CURRENT	OFF-STATE OUTPUT VOLTAGE	TOTAL POWER
'248	6.4 mA	5.5 V	265 mW
SN54LS248	2 mA	5.5 V	125 mW
SN74LS248	6 mA	5.5 V	125 mW

SN54248 (J,FC) SN74248 (J,N)
SN54LS248 (J,FC) SN74LS248 (J,N)

249

BCD-TO-SEVEN SEGMENT DECODERS/DRIVERS
(open-collector outputs)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	B	9	e	1	B	11	e
2	C	10	d	2	C	12	d
3	$\overline{LT}$	11	c	3	nc	13	nc
4	$\overline{BI}$/$\overline{RBO}$	12	b	4	$\overline{LT}$	14	c
5	$\overline{RBI}$	13	a	5	$\overline{BI}$/$\overline{RBO}$	15	b
6	D	14	g	6	$\overline{RBI}$	16	a
7	A	15	f	7	D	17	g
8	GND	16	V_{CC}	8	nc	18	nc
				9	A	19	f
				10	GND	20	V_{CC}

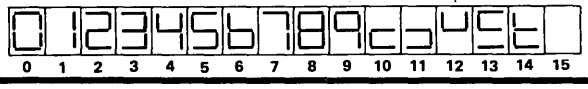
typical performance

TYPE	OUTPUT SINK CURRENT	OFF-STATE OUTPUT VOLTAGE	TOTAL POWER
'249	10 mA	5.5 V	265 mW
SN54LS249	4 mA	5.5 V	40 mW
SN74LS249	8 mA	5.5 V	40 mW

SN54249 (J,FC) SN74249 (J,N)
SN54LS249 (J,FC) SN74LS249 (J,N)

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

FONT TABLE T2 — RESULTANT DISPLAYS USING '248 AND '249



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

251

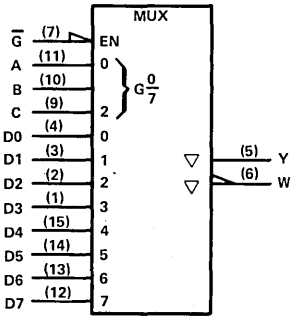
DATA SELECTORS/ MULTIPLEXERS
(true and inverted three-state outputs)

typical performance

TYPE	DELAY TIMES			TOTAL POWER
	DATA TO INV OUTPUT	DATA TO NON-INV OUTPUT	FROM ENABLE	
'251	17 ns	21 ns	21 ns	250 mW
'LS251	17 ns	21 ns	21 ns	35 mW
'S251	4.5 ns	8 ns	14 ns	275 mW

SN54251 (J,FC) SN74251 (J,N)
SN54LS251 (J,FC) SN74LS251 (J,N)
SN54S251 (J,FC) SN74S251 (J,N,FN)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	D3	9	C	1	D3	11	C
2	D2	10	B	2	D2	12	B
3	D1	11	A	3	nc	13	nc
4	D0	12	D7	4	D1	14	A
5	Y	13	D6	5	D0	15	D7
6	W	14	D5	6	Y	16	D6
7	$\overline{G}$	15	D4	7	W	17	D5
8	GND	16	V_{CC}	8	nc	18	nc
				9	$\overline{G}$	19	D4
				10	GND	20	V_{CC}

253

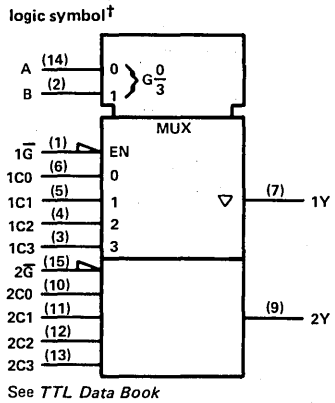
DUAL DATA SELECTORS/ MULTIPLEXERS
(three-state outputs)

typical performance

TYPE	DELAY TIMES		TOTAL POWER
	DATA TO NON-INV OUTPUT	FROM ENABLE	
'LS253	12 ns	16 ns	35 mW

SN54LS253 (J,FC) SN74LS253 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	$1\overline{G}$	9	2Y	1	$1\overline{G}$	11	2Y
2	B	10	2C0	2	B	12	2C0
3	1C3	11	2C1	3	nc	13	nc
4	1C2	12	2C2	4	1C3	14	2C1
5	1C1	13	2C3	5	1C2	15	2C2
6	1C0	14	A	6	1C1	16	2C3
7	1Y	15	$2\overline{G}$	7	1C0	17	A
8	GND	16	V_{CC}	8	nc	18	nc
				9	1Y	19	$2\overline{G}$
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

257

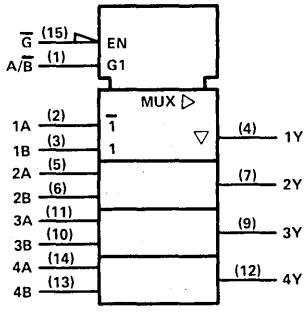
QUAD DATA SELECTORS/ MULTIPLEXERS

(non-inverted three-state outputs)

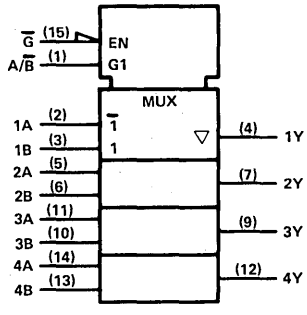
TYPE	DELAY TIMES		TOTAL POWER
	DATA TO NON-INV OUTPUT	FROM ENABLE	
'LS257	11 ns	19 ns	60 mW
'S257	5 ns	14 ns	320 mW

SN54LS257 (J,FC)
SN54S257 (J,FC)
SN74LS257 (J,N)
SN74S257 (J,N,FN)

logic symbol, 'LS257†



logic symbol, 'S257†



See *TTL Data Book*

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 A/B	9 3Y	1 nc	11 3Y
2 1A	10 3B	2 A/B	12 3B
3 1B	11 3A	3 nc	13 nc
4 1Y	12 4Y	4 1A	14 3A
5 2A	13 4B	5 1B	15 4Y
6 2B	14 4A	6 1Y	16 4B
7 2Y	15 G	7 2A	17 4A
8 GND	16 V_{CC}	8 2B	18 nc
		9 2Y	19 G
		10 GND	20 V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

258

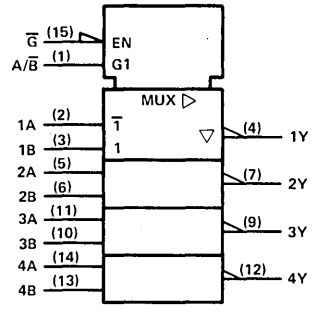
QUAD DATA SELECTORS/ MULTIPLEXERS
(inverted three-state outputs)

typical performance

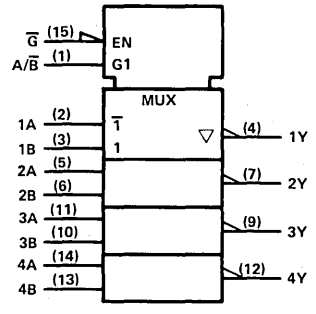
TYPE	DELAY TIMES: DATA TO INV OUTPUT	DELAY TIMES: FROM ENABLE	TOTAL POWER
'LS258	11 ns	19 ns	60 mW
'S258	4 ns	14 ns	280 mW

SN54LS258 (J,FC) SN74LS258 (J,N)
SN54S258 (J,FC) SN74S258 (J,N,FN)

logic symbol, 'LS258†



logic symbol, 'S258†



See *TTL Data Book*

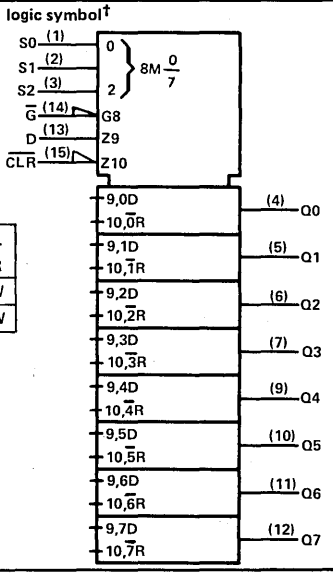
pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	A/B	9	3Y	1	nc	11	3Y
2	1A	10	3B	2	A/B	12	3B
3	1B	11	3A	3	nc	13	nc
4	1Y	12	4Y	4	1A	14	3A
5	2A	13	4B	5	1B	15	4Y
6	2B	14	4A	6	1Y	16	4B
7	2Y	15	G	7	2A	17	4A
8	GND	16	V_{CC}	8	2B	18	nc
				9	2Y	19	G
				10	GND	20	V_{CC}

259

8-BIT ADDRESSABLE LATCHES

logic symbol†



typical performance

TYPE	CLEAR	OUTPUTS	DELAY	TOTAL POWER
'259	LOW	Q	12 ns	300 mW
'LS259	LOW	Q	17 ns	110 mW

SN54259 (J,FC) SN74259 (J,N)
SN54LS259 (J,FC) SN74LS259 (J,N)

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	S0	9	Q4	1	S0	11	Q4
2	S1	10	Q5	2	S1	12	Q5
3	S2	11	Q6	3	nc	13	nc
4	Q0	12	Q7	4	S2	14	Q6
5	Q1	13	D	5	Q0	15	nc
6	Q2	14	G	6	Q1	16	Q7
7	Q3	15	CLR	7	Q2	17	D
8	GND	16	V_{CC}	8	nc	18	G
				9	Q3	19	CLR
				10	GND	20	V_{CC}

See *TTL Data Book*

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

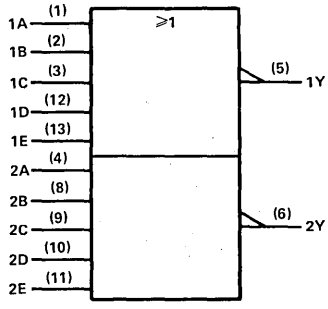
260

DUAL 5-INPUT POSITIVE-NOR GATES

TYPE	POWER/ GATE	DELAY
'S260	54 mW	4 ns

SN54S260 (J,FC) SN74S260 (J,N,FN)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 1A	8 2B	1 1A	11 nc
2 1B	9 2C	2 1B	12 2B
3 1C	10 2D	3 nc	13 nc
4 2A	11 2E	4 nc	14 2C
5 1Y	12 1D	5 1C	15 2D
6 2Y	13 1E	6 2A	16 2E
7 GND	14 V_{CC}	7 1Y	17 1D
		8 nc	18 nc
		9 2Y	19 1E
		10 GND	20 V_{CC}

positive logic: $Y = \overline{ABCD}$

261

2-BIT BY 4-BIT PARALLEL BINARY MULTIPLIERS

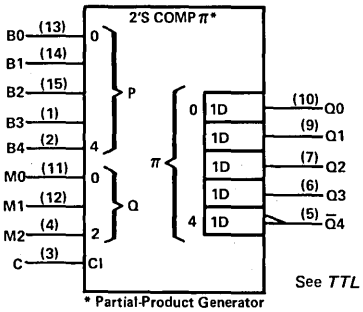
typical performance

TYPE	POWER	TIME**
'LS261	100 mW	25 ns

SN54LS261 (J,FC) SN74LS261 (J,N)

** 5-Bit Product Time

logic symbol†



* Partial-Product Generator

See *TTL Data Book*

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 B3	9 Q1	1 B3	11 Q1
2 B4	10 Q0	2 B4	12 Q0
3 C	11 M0	3 nc	13 nc
4 M2	12 M1	4 C	14 M0
5 Q̄4	13 B0	5 M2	15 M1
6 Q3	14 B1	6 Q̄4	16 B0
7 Q2	15 B2	7 Q3	17 B1
8 GND	16 V_{CC}	8 nc	18 nc
		9 Q2	19 B2
		10 GND	20 V_{CC}

265

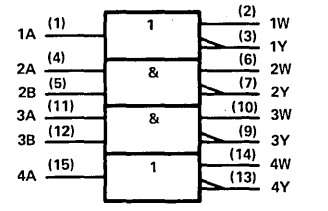
QUAD COMPLEMENTARY-OUTPUT ELEMENTS

typical performance

TYPE	POWER
'265	125 mW

SN54265 (J) SN74265 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES	
1 1A	9 3Y
2 1W	10 3W
3 1Y	11 3A
4 2A	12 3B
5 2B	13 4Y
6 2W	14 4W
7 2Y	15 4A
8 GND	16 V_{CC}

266

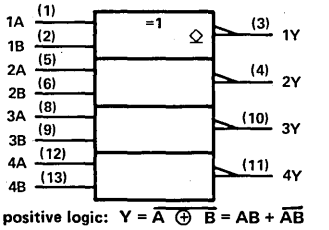
QUAD 2-INPUT EXCLUSIVE-NOR GATES WITH OPEN-COLLECTOR OUTPUTS

typical performance

TYPE	POWER	DELAY
'LS266	40 mW	18 ns

SN54LS266 (J,FC) SN74LS266 (J,N)

logic symbol†



positive logic: $Y = \overline{A \oplus B} = AB + \overline{A}\,\overline{B}$

See *TTL Data Book*

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 1A	8 3A	1 nc	11 3A
2 1B	9 3B	2 nc	12 nc
3 1Y	10 3Y	3 1A	13 3B
4 2Y	11 4Y	4 1B	14 nc
5 2A	12 4A	5 1Y	15 3Y
6 2B	13 4B	6 2Y	16 4Y
7 GND	14 V_{CC}	7 2A	17 nc
		8 nc	18 4A
		9 2B	19 4B
		10 GND	20 V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

270

2048-BIT READ-ONLY MEMORIES
(open-collector outputs, 512 4-bit words)

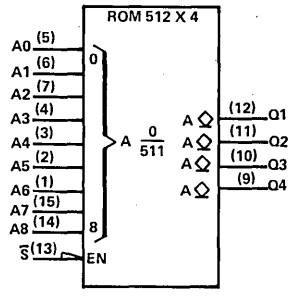
typical performance

TYPE	ADDRESS TIME	ENABLE TIME	POWER/ BIT
'S270	45 ns	15 ns	0.26 mW

SN54S270 (J,FC) SN74S270 (J,N,FN)

For more information contact factory

logic symbol†



pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 A6	9 Q4	1 A6	15 Q4
2 A5	10 Q3	2 A5	16 Q3
3 A4	11 Q2	3 A4	17 nc
4 A3	12 Q1	4 nc	18 nc
5 A0	13 S̄	5 A3	19 nc
6 A1	14 A8	6 A0	20 Q2
7 A2	15 A7	7 nc	21 Q1
8 GND	16 V_{CC}	8 nc	22 S̄
		9 nc	23 A8
		10 A1	24 nc
		11 A2	25 A7
		12 nc	26 nc
		13 nc	27 nc
		14 GND	28 V_{CC}

271

2048-BIT READ-ONLY MEMORIES
(open-collector outputs, 256 8-bit words)

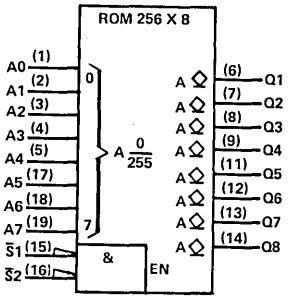
typical performance

TYPE	ADDRESS TIME	ENABLE TIME	POWER/ BIT
'S271	45 ns	15 ns	0.26 mW

SN54S271 (J,FC) SN74S271 (J,N,FN)

For more information contact factory

logic symbol†



pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 A0	11 Q5	1 A0	15 Q5
2 A1	12 Q6	2 A1	16 Q6
3 A2	13 Q7	3 A2	17 nc
4 A3	14 Q8	4 nc	18 Q7
5 A4	15 S̄1	5 A3	19 Q8
6 Q1	16 S̄2	6 A4	20 nc
7 Q2	17 A5	7 nc	21 S̄1
8 Q3	18 A6	8 nc	22 S̄2
9 Q4	19 A7	9 Q1	23 A5
10 GND	20 V_{CC}	10 Q2	24 nc
		11 nc	25 A6
		12 Q3	26 A7
		13 Q4	27 nc
		14 GND	28 V_{CC}

273

OCTAL D-TYPE FLIP-FLOPS
(common clock, single-rail outputs)

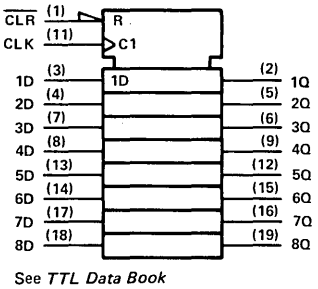
typical performance

TYPE	FREQ	POWER/ F-F	DATA TIMES SETUP	HOLD
'273	40 MHz	39 mW	20 ns†	5 ns†
'LS273	40 MHz	10.6 mW	20 ns†	5 ns†

† Rising edge of clock pulse

SN54273 (J,FC) SN74273 (J,N)
SN54LS273 (J,FC) SN74LS273 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 CLR	11 CLK	1 CLR	11 CLK
2 1Q	12 5Q	2 1Q	12 5Q
3 1D	13 5D	3 1D	13 5D
4 2D	14 6D	4 2D	14 6D
5 2Q	15 6Q	5 2Q	15 6Q
6 3Q	16 7Q	6 3Q	16 7Q
7 3D	17 7D	7 3D	17 7D
8 4D	18 8D	8 4D	18 8D
9 4Q	19 8Q	9 4Q	19 8Q
10 GND	20 V_{CC}	10 GND	20 V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

274

4-BIT BY 4-BIT BINARY MULTIPLIERS

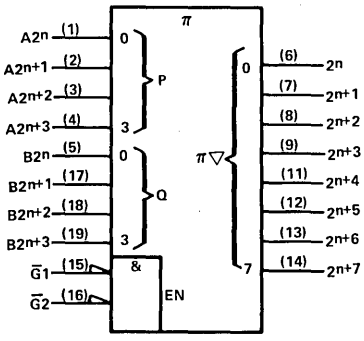
typical performance

TYPE	POWER	TIME*
'S274	525 mW	50 ns

SN54S274 (J,FC)
SN74S274 (J,N,FN)

* 8-Bit Product Time

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES			
1	$A2^n$	11	2^{n+4}
2	$A2^{n+1}$	12	2^{n+5}
3	$A2^{n+2}$	13	2^{n+6}
4	$A2^{n+3}$	14	2^{n+7}
5	$B2^n$	15	$\overline{G}1$
6	2^n	16	$\overline{G}2$
7	2^{n+1}	17	$B2^{n+1}$
8	2^{n+2}	18	$B2^{n+2}$
9	2^{n+3}	19	$B2^{n+3}$
10	GND	20	V_{CC}

FC, FN PACKAGES			
1	$A2^n$	15	2^{n+4}
2	$A2^{n+1}$	16	2^{n+5}
3	$A2^{n+2}$	17	nc
4	nc	18	nc
5	$A2^{n+3}$	19	nc
6	$B2^n$	20	2^{n+6}
7	nc	21	2^{n+7}
8	nc	22	$\overline{G}1$
9	2^n	23	$\overline{G}2$
10	2^{n+1}	24	$B2^{n+1}$
11	nc	25	$B2^{n+2}$
12	2^{n+2}	26	nc
13	2^{n+3}	27	$B2^{n+3}$
14	GND	28	V_{CC}

275

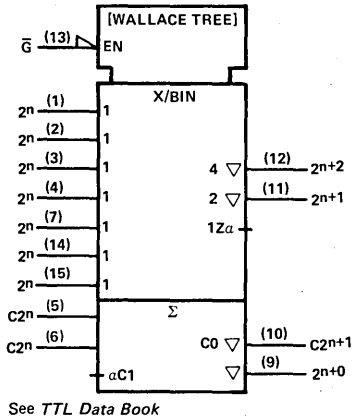
7-BIT-SLICE WALLACE TREES

typical performance

TYPE	POWER
'LS275	125 mW
'S275	525 mW

SN54LS275 (J,FC)
SN54S275 (J,FC)
SN74LS275 (J,N)
SN74S275 (J,N,FN)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES			
1	2^n	9	2^{n+0}
2	2^n	10	$C2^{n+1}$
3	2^n	11	2^{n+1}
4	2^n	12	2^{n+2}
5	$C2^n$	13	$\overline{G}$
6	$C2^n$	14	2^n
7	2^n	15	2^n
8	GND	16	V_{CC}

FC, FN PACKAGES			
1	2^n	15	2^{n+0}
2	2^n	16	$C2^{n+1}$
3	2^n	17	nc
4	nc	18	nc
5	nc	19	nc
6	nc	20	2^{n+1}
7	2^n	21	2^{n+2}
8	$C2^n$	22	nc
9	nc	23	$\overline{G}$
10	$C2^n$	24	2^n
11	2^n	25	2^n
12	nc	26	nc
13	nc	27	nc
14	GND	28	V_{CC}

276

QUAD J-$\overline{K}$ FLIP-FLOPS
(separate clocks, edge-triggering, common direct clear and preset)

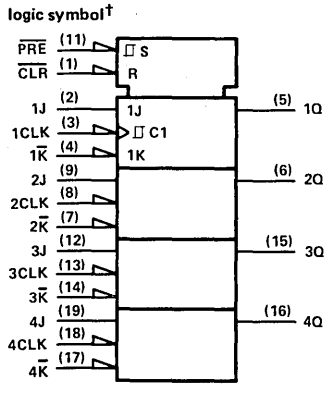
typical performance

TYPE	FREQ	POWER/ F-F	DATA TIMES SETUP	HOLD
'276	50 MHz	75 mW	3 ns↓	10 ns↓

↓ Falling edge of clock pulse

SN54276 (J) SN74276 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES			
1	$\overline{CLR}$	11	$\overline{PRE}$
2	1J	12	3J
3	1CLK	13	3CLK
4	1$\overline{K}$	14	3$\overline{K}$
5	1Q	15	3Q
6	2Q	16	4Q
7	2$\overline{K}$	17	4$\overline{K}$
8	2CLK	18	4CLK
9	2J	19	4J
10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

278

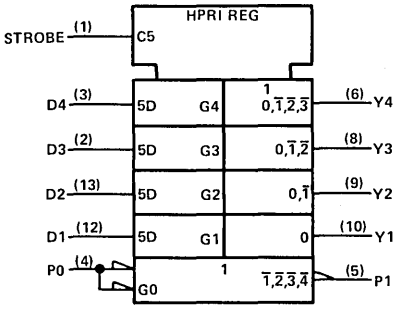
4-BIT CASCADABLE PRIORITY REGISTERS

typical performance

TYPE	POWER	DELAY
'278	275 mW	35 ns

SN54278 (J) SN74278 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES			
1	STRB	8	Y3
2	D3	9	Y2
3	D4	10	Y1
4	P0	11	nc
5	P1	12	D1
6	Y4	13	D2
7	GND	14	V_{CC}

279

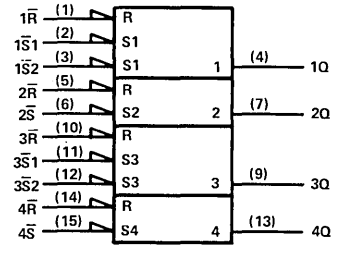
QUAD $\overline{S}$-$\overline{R}$ LATCHES

typical performance

TYPE	POWER	DELAY
'279	90 mW	12 ns
'LS279	19 mW	12 ns

SN54279 (J,FC) SN74279 (J,N,FN)
SN54LS279 (J,FC) SN74LS279 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	1R̄	9	3Q	1	1R̄	11	3Q
2	1S̄1	10	3R̄	2	1S̄1	12	3R̄
3	1S̄2	11	3S̄1	3	nc	13	nc
4	1Q	12	3S̄2	4	1S̄2	14	3S̄1
5	2R̄	13	4Q	5	1Q	15	3S̄2
6	2S̄	14	4R̄	6	2R̄	16	4Q
7	2Q	15	4S̄	7	2S̄	17	4R̄
8	GND	16	V_{CC}	8	nc	18	nc
				9	2Q	19	4S̄
				10	GND	20	V_{CC}

280

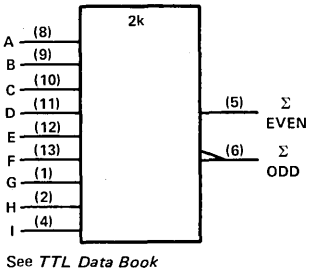
9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

typical performance

TYPE	POWER	DELAY
'LS280	80 mW	31 ns
'S280	335 mW	13 ns

SN54LS280 (J,FC) SN74LS280 (J,N)
SN54S280 (J,FC) SN74S280 (J,N,FN)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	G	8	A	1	G	11	A
2	H	9	B	2	H	12	B
3	nc	10	C	3	nc	13	nc
4	I	11	D	4	nc	14	nc
5	ΣEVEN	12	E	5	nc	15	C
6	ΣODD	13	F	6	I	16	D
7	GND	14	V_{CC}	7	ΣEVEN	17	E
				8	nc	18	nc
				9	ΣODD	19	F
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

8

281

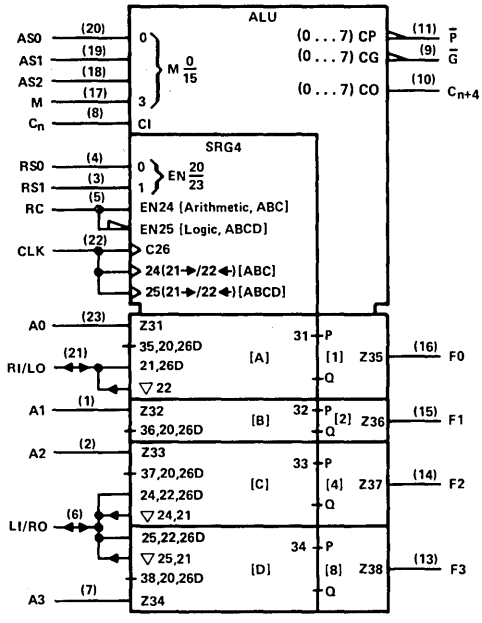
4-BIT PARALLEL BINARY ACCUMULATORS

typical performance

TYPE	ADD TIME	TOTAL POWER
'S281	20 ns	720 mW

SN54S281 (J,FC)
SN74S281 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 A1	13 F3	1 A1	15 F3
2 A2	14 F2	2 A2	16 F2
3 RS1	15 F1	3 RS1	17 F1
4 RS0	16 F0	4 nc	18 nc
5 RC	17 M	5 nc	19 F0
6 LI/RO	18 AS2	6 RS0	20 M
7 A3	19 AS1	7 RC	21 AS2
8 C_n	20 AS0	8 LI/RO	22 AS1
9 $\overline{G}$	21 RI/LO	9 A3	23 AS0
10 C_{n+4}	22 CLK	10 C_n	24 RI/LO
11 $\overline{P}$	23 A0	11 $\overline{G}$	25 CLK
12 GND	24 V_{CC}	12 C_{n+4}	26 nc
		13 $\overline{P}$	27 A0
		14 GND	28 V_{CC}

See *TTL Data Book*

283

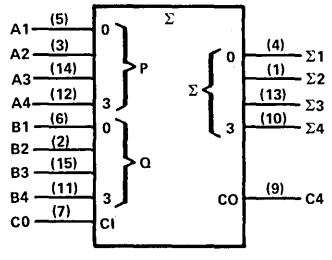
4-BIT BINARY FULL ADDERS

typical performance

TYPE	CARRY TIME	ADD TIME	POWER/ BIT
'283	10 ns	16 ns	76 mW
'LS283	10 ns	15 ns	24 mW
'S283	11 ns	7 ns	124 mW

SN54283 (J,FC) SN74283 (J,N)
SN54LS283 (J,FC) SN74LS283 (J,N)
SN54S283 (J,FC) SN74S283 (J,N,FN)

logic symbol†



See *TTL Data Book*

typical performance

J, N PACKAGES		FC, FN PACKAGES	
1 Σ2	9 C4	1 Σ2	11 C4
2 B2	10 Σ4	2 B2	12 Σ4
3 A2	11 B4	3 nc	13 nc
4 Σ1	12 A4	4 A2	14 B4
5 A1	13 Σ3	5 Σ1	15 A4
6 B1	14 A3	6 A1	16 Σ3
7 C0	15 B3	7 B1	17 A3
8 GND	16 V_{CC}	8 nc	18 nc
		9 C0	19 B3
		10 GND	20 V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

284

4-BIT BY 4-BIT PARALLEL BINARY MULTIPLIERS USED WITH '285

- MSB's for 4 X 4 multiplier ('285 provides LSB's)
- Use 'S274, 'LS275, 'S275 for new designs/larger multipliers

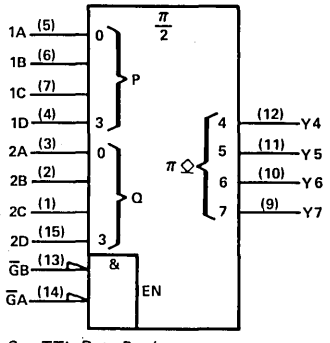
typical performance

TYPE	POWER	TIME*
'284	460 mW	40 ns

SN54284 (J) SN74284 (J,N)

* 8-Bit Product Time

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES	
1 2C	9 Y7
2 2B	10 Y6
3 2A	11 Y5
4 1D	12 Y4
5 1A	13 $\overline{GB}$
6 1B	14 $\overline{GA}$
7 1C	15 2D
8 GND	16 V_{CC}

285

4-BIT BY 4-BIT PARALLEL BINARY MULTIPLIERS USED WITH '284

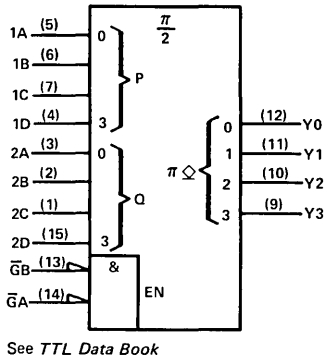
- LSB's for 4 X 4 multiplier ('284 provides MSB's)
- Use 'S274, 'LS275, 'S275 for new designs/larger multipliers

typical performance

TYPE	POWER
'285	460 mW

SN54285 (J) SN74285 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES	
1 2C	9 Y3
2 2B	10 Y2
3 2A	11 Y1
4 1D	12 Y0
5 1A	13 $\overline{GB}$
6 1B	14 $\overline{GA}$
7 1C	15 2D
8 GND	16 V_{CC}

287

(This number has been changed to TBP14S10. Product Guide information for this TTL circuit can be found at the end of this section.)

288

(This number has been changed to TBP18S030. Product Guide information for this TTL circuit can be found at the end of this section.)

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

289

64-BIT RANDOM-ACCESS MEMORIES

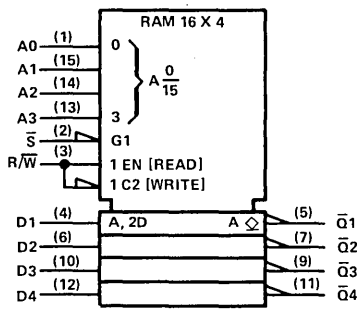
(16 4-bit words, open-collector outputs)

typical performance

TYPE	ADDRESS TIME	ENABLE TIME	POWER/ BIT
'LS289A	50 ns	35 ns	2.7 mW
'S289A	25 ns	12 ns	5.9 mW

SN54LS289A (J,FC) SN74LS289A (J,N)
SN54S289A (J,FC) SN74S289A (J,N,FN)

logic symbol†



See Pages 2-45 and 2-49

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	A0	9	Q̄3	1	A0	11	Q̄3
2	S̄	10	D3	2	S̄	12	D3
3	R/W̄	11	Q̄4	3	nc	13	nc
4	D1	12	D4	4	R/W̄	14	Q̄4
5	Q̄1	13	A3	5	D1	15	D4
6	D2	14	A2	6	Q̄1	16	A3
7	Q̄2	15	A1	7	D2	17	A2
8	GND	16	V_{CC}	8	nc	18	nc
				9	Q̄2	19	A1
				10	GND	20	V_{CC}

290

DECADE COUNTERS

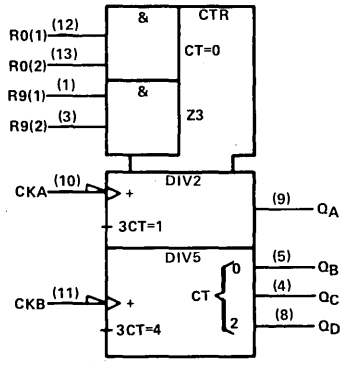
(divide-by-two and divide-by-five)

typical performance

TYPE	COUNT FREQ	CLEAR	TOTAL POWER
'290	32 MHz	HIGH	160 mW
'LS290	32 MHz	HIGH	40 mW

SN54290 (J,FC) SN74290 (J,N)
SN54LS290 (J,FC) SN74LS290 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	R9(1)	8	QD	1	R9(1)	11	QD
2	nc	9	QA	2	nc	12	QA
3	R9(2)	10	CKA	3	nc	13	nc
4	QC	11	CKB	4	nc	14	nc
5	QB	12	R0(1)	5	R9(2)	15	CKA
6	nc	13	R0(2)	6	QC	16	CKB
7	GND	14	V_{CC}	7	QB	17	R0(1)
				8	nc	18	nc
				9	nc	19	R0(2)
				10	GND	20	V_{CC}

292

PROGRAMMABLE FREQUENCY DIVIDERS/DIGITAL TIMERS

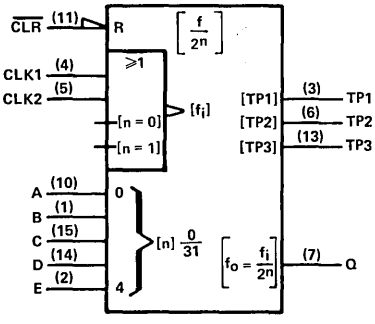
(digitally programmable from 2^2 to 2^{31})

typical performance

TYPE	POWER	f_{max}
'LS292	200 mW	50 MHz

SN54LS292 (J) SN74LS292 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES			
1	B	9	nc
2	E	10	A
3	TP1	11	CLR
4	CLK1	12	nc
5	CLK2	13	TP3
6	TP2	14	D
7	Q	15	C
8	GND	16	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

293

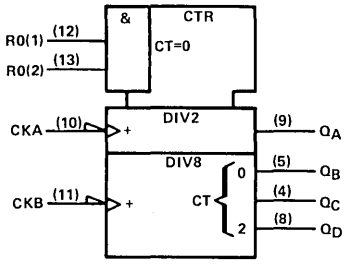
4-BIT BINARY COUNTERS
(divide-by-two and divide-by-eight)

typical performance

TYPE	COUNT FREQ	CLEAR	TOTAL POWER
'293	32 MHz	HIGH	160 mW
'LS293	32 MHz	HIGH	39 mW

SN54293 (J,FC) SN74293 (J,N)
SN54LS293 (J,FC) SN74LS293 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 nc	8 QD	1 nc	11 QD
2 nc	9 QA	2 nc	12 QA
3 nc	10 CKA	3 nc	13 nc
4 QC	11 CKB	4 nc	14 nc
5 QB	12 R0(1)	5 nc	15 CKA
6 nc	13 R0(2)	6 QC	16 CKB
7 GND	14 V_{CC}	7 QB	17 R0(1)
		8 nc	18 nc
		9 nc	19 R0(2)
		10 GND	20 V_{CC}

294

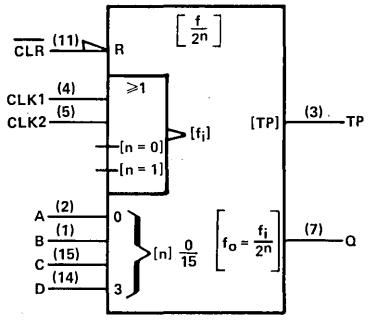
PROGRAMMABLE FREQUENCY DIVIDERS/DIGITAL TIMERS
(digitally programmable from 2^2 to 2^{15})

typical performance

TYPE	POWER	f_{max}
'LS294	150 mW	50 MHz

SN54LS294 (J) SN74LS294 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES	
1 B	9 nc
2 A	10 nc
3 TP	11 $\overline{CLR}$
4 CLK1	12 nc
5 CLK2	13 nc
6 nc	14 D
7 Q	15 C
8 GND	16 V_{CC}

295

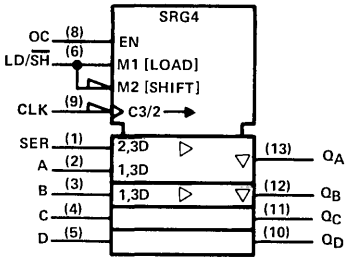
4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

typical performance

TYPE	SHIFT FREQ	SERIAL DATA INPUT	TOTAL POWER
'LS295B	30 MHz	D	70 mW

SN54LS295B (J,FC) SN74LS295B (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 SER	8 OC	1 SER	11 OC
2 A	9 CLK	2 nc	12 CLK
3 B	10 QD	3 nc	13 nc
4 C	11 QC	4 A	14 nc
5 D	12 QB	5 B	15 QD
6 LD/$\overline{SH}$	13 QA	6 C	16 QC
7 GND	14 V_{CC}	7 D	17 QB
		8 nc	18 nc
		9 LD/$\overline{SH}$	19 QA
		10 GND	20 V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

297

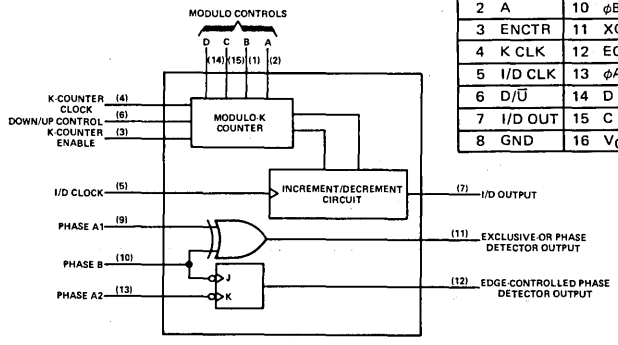
DIGITAL PHASE-LOCKED-LOOP FILTERS
(cascadable for higher-order loops)

typical performance

TYPE	POWER	f_{max}		DELAY (FROM I/DCLK)
		KCLK	I/DCLK	
'LS297	375 mW	50 MHz	35 MHz	18.5 ns

SN54LS297 (J) SN74LS297 (J,N)

simplified block diagram†



pin assignments

J, N PACKAGES	
1 B	9 ϕA1
2 A	10 ϕB
3 ENCTR	11 XORPD
4 K CLK	12 ECPD
5 I/D CLK	13 ϕA2
6 D/$\overline{U}$	14 D
7 I/D OUT	15 C
8 GND	16 V_{CC}

See *TTL Data Book*

298

QUAD 2-INPUT MULTIPLEXERS WITH STORAGE

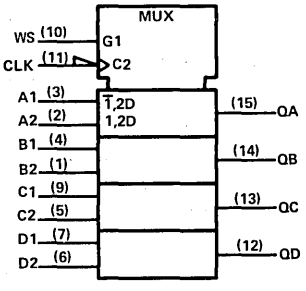
typical performance

TYPE	POWER	DELAY*
'298	195 mW	20 ns
'LS298	65 mW	20 ns

* From clock to non-inverted output

SN54298 (J,FC) SN74298 (J,N)
SN54LS298 (J,FC) SN74LS298 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 B2	9 C1	1 B2	11 C1
2 A2	10 WS	2 A2	12 WS
3 A1	11 CLK	3 nc	13 nc
4 B1	12 QD	4 A1	14 CLK
5 C2	13 QC	5 B1	15 QD
6 D2	14 QB	6 C2	16 QC
7 D1	15 QA	7 D2	17 QB
8 GND	16 V_{CC}	8 nc	18 nc
		9 D1	19 QA
		10 GND	20 V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

299

8-BIT BIDIRECTIONAL UNIVERSAL SHIFT/STORAGE REGISTERS

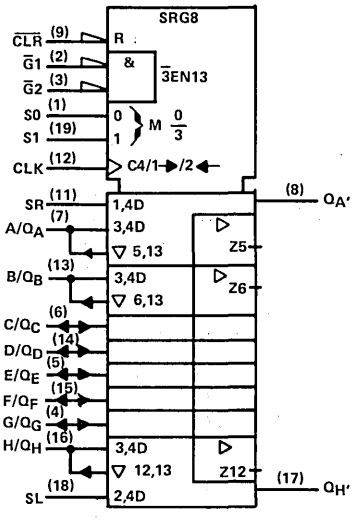
(three-state outputs)

typical performance

TYPE	SHIFT FREQ	SERIAL DATA INPUT	ASYNC CLEAR	TOTAL POWER
'LS299	35 MHz	D	LOW	175 mW
'S299	50 MHz	D	LOW	750 mW

SN54LS299 (J,FC) SN74LS299 (J,N)
SN54S299 (J,FC) SN74S299 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 S0	11 SR	1 S0	11 SR
2 $\overline{G}1$	12 CLK	2 $\overline{G}1$	12 CLK
3 $\overline{G}2$	13 B/QB	3 $\overline{G}2$	13 B/QB
4 G/QG	14 D/QD	4 G/QG	14 D/QD
5 E/QE	15 F/QF	5 E/QE	15 F/QF
6 C/QC	16 H/QH	6 C/QC	16 H/QH
7 A/QA	17 $Q_{H'}$	7 A/QA	17 $Q_{H'}$
8 $Q_{A'}$	18 SL	8 $Q_{A'}$	18 SL
9 $\overline{CLR}$	19 S1	9 $\overline{CLR}$	19 S1
10 GND	20 V_{CC}	10 GND	20 V_{CC}

See *TTL Data Book*

301

256-BIT RANDOM-ACCESS MEMORIES

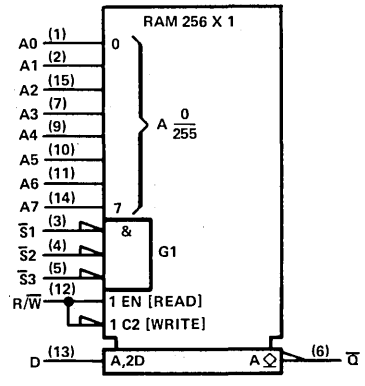
(256 1-bit words, open-collector output)

typical performance

TYPE	ADDRESS TIME	ENABLE TIME	POWER/ BIT
'S301	42 ns	13 ns	1.9 mW

SN74S301 (J,N)

logic symbol†



pin assignments

J, N PACKAGES	
1 A0	9 A4
2 A1	10 A5
3 $\overline{S}1$	11 A6
4 $\overline{S}2$	12 R/$\overline{W}$
5 $\overline{S}3$	13 D
6 $\overline{Q}$	14 A7
7 A3	15 A2
8 GND	16 V_{CC}

See Page 2-53

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

319

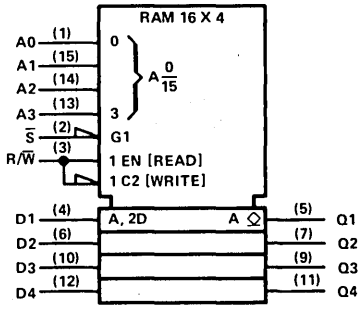
64-BIT RANDOM ACCESS MEMORIES
(16-four bit words, open-collector outputs)

typical performance

TYPE	ADDRESS TIME	ENABLE TIME	POWER/ BIT
'LS319A	50 ns	35 ns	2.7 mW

SN54LS319A (J,FC) SN74LS319A (J,N)

logic symbol†



pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	A0	9	Q3	1	A0	11	Q3
2	S̄	10	D3	2	S̄	12	D3
3	R/W̄	11	Q4	3	nc	13	nc
4	D1	12	D4	4	R/W̄	14	Q4
5	Q1	13	A3	5	D1	15	D4
6	D2	14	A2	6	Q1	16	A3
7	Q2	15	A1	7	D2	17	A2
8	GND	16	V_{CC}	8	nc	18	nc
				9	Q2	19	A1
				10	GND	20	V_{CC}

See Page 2-45

320

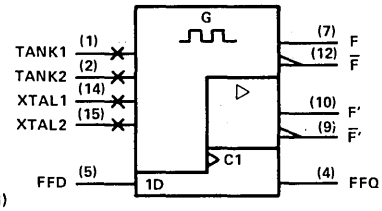
CRYSTAL-CONTROLLED OSCILLATORS

typical performance

TYPE	f_{max}	POWER
'LS320	30 MHz	210 mW

SN54LS320 (J,FC) SN74LS320 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	TANK1	9	F̄'	1	TANK1	11	F̄'
2	TANK2	10	F'	2	TANK2	12	F'
3	GND1	11	$V_{CC'}$	3	GND1	13	$V_{CC'}$
4	FFQ	12	F̄	4	FFQ	14	nc
5	FFD	13	nc	5	FFD	15	F̄
6	nc	14	XTAL1	6	nc	16	nc
7	F	15	XTAL2	7	F̄	17	XTAL1
8	GND2	16	V_{CC}	8	nc	18	nc
				9	nc	19	XTAL2
				10	GND2	20	V_{CC}

321

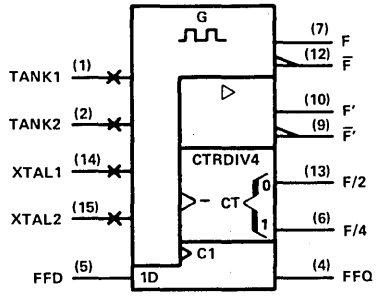
CRYSTAL-CONTROLLED OSCILLATORS
(with F/2 and F/4 count-down outputs)

typical performance

TYPE	FREQ	POWER
'LS321	30 MHz	235 mW

SN54LS321 (J,FC) SN74LS321 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	TANK1	9	F̄'	1	TANK1	11	F̄'
2	TANK2	10	F'	2	TANK2	12	F'
3	GND1	11	$V_{CC'}$	3	GND1	13	$V_{CC'}$
4	FFQ	12	F̄	4	FFQ	14	nc
5	FFD	13	F/2	5	FFD	15	F̄
6	F/4	14	XTAL1	6	F/4	16	F/2
7	F	15	XTAL2	7	F	17	XTAL1
8	GND2	16	V_{CC}	8	nc	18	nc
				9	nc	19	XTAL2
				10	GND2	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

322

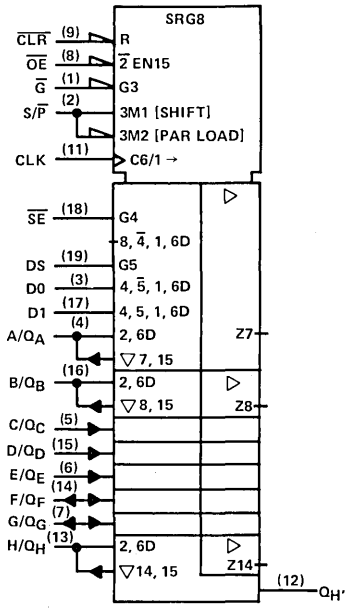
8-BIT SHIFT REGISTERS WITH SIGN EXTEND
(three-state outputs, multiplexed I/O)

typical performance

TYPE	SHIFT FREQ	SERIAL DATA INPUT	ASYNC CLEAR	POWER
'LS322A	35 MHz	D	LOW	175 mW

SN54LS322A (J,FC) SN74LS322A (J,N)

logic symbol†



pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 $\overline{G}$	11 CLK	1 $\overline{G}$	11 CLK
2 S/$\overline{P}$	12 QH'	2 S/$\overline{P}$	12 QH'
3 D0	13 H/QH	3 D0	13 H/QH
4 A/QA	14 F/QF	4 A/QA	14 F/QF
5 C/QC	15 D/QD	5 C/QC	15 D/QD
6 E/QE	16 B/QB	6 E/QE	16 B/QB
7 G/QG	17 D1	7 G/QG	17 D1
8 $\overline{OE}$	18 $\overline{SE}$	8 $\overline{OE}$	18 $\overline{SE}$
9 $\overline{CLR}$	19 DS	9 $\overline{CLR}$	19 DS
10 GND	20 V_{CC}	10 GND	20 V_{CC}

See *TTL Data Book*

323

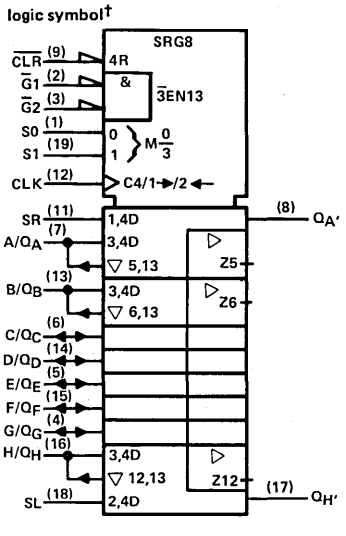
8-BIT BIDIRECTIONAL SHIFT/STORAGE REGISTERS
(three-state outputs)

typical performance

TYPE	SHIFT FREQ	SERIAL DATA INPUT	POWER
'LS323	35 MHz	D	175 mW

SN54LS323 (J,FC) SN74LS323 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 S0	11 SR	1 S0	11 SR
2 $\overline{G1}$	12 CLK	2 $\overline{G1}$	12 CLK
3 $\overline{G2}$	13 B/QB	3 $\overline{G2}$	13 B/QB
4 G/QG	14 D/QD	4 G/QG	14 D/QD
5 E/QE	15 F/QF	5 E/QE	15 F/QF
6 C/QC	16 H/QH	6 C/QC	16 H/QH
7 A/QA	17 $Q_{H'}$	7 A/QA	17 $Q_{H'}$
8 $Q_{A'}$	18 SL	8 $Q_{A'}$	18 SL
9 $\overline{CLR}$	19 S1	9 $\overline{CLR}$	19 S1
10 GND	20 V_{CC}	10 GND	20 V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

340

OCTAL BUFFERS/ LINE DRIVERS

(three-state inverted outputs)

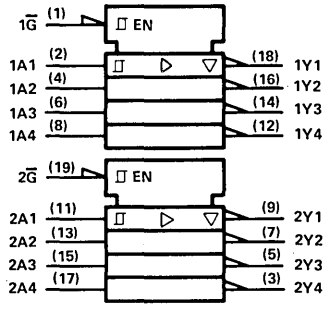
- 300 mV guaranteed hysteresis

typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT
'S340	8 ns	−15 mA	64 mA

SN54S340 (J,FC) SN74S340 (J,N,FN)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 1G̅	11 2A1	1 1G̅	15 2A1
2 1A1	12 1Y4	2 1A1	16 nc
3 2Y4	13 2A2	3 nc	17 nc
4 1A2	14 1Y3	4 nc	18 nc
5 2Y3	15 2A3	5 2Y4	19 1Y4
6 1A3	16 1Y2	6 1A2	20 2A2
7 2Y2	17 2A4	7 2Y3	21 1Y3
8 1A4	18 1Y1	8 1A3	22 2A3
9 2Y1	19 2G̅	9 2Y2	23 1Y2
10 GND	20 V_{CC}	10 1A4	24 2A4
		11 nc	25 1Y1
		12 2Y1	26 nc
		13 nc	27 2G̅
		14 GND	28 V_{CC}

341

OCTAL BUFFERS/ LINE DRIVERS

(three-state non-inverted outputs)

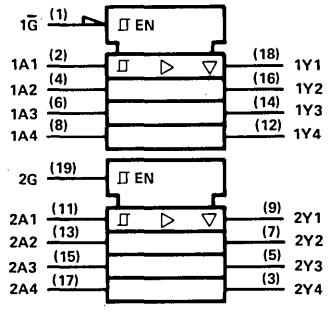
- 300 mV guaranteed hysteresis

typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT
'S341	9 ns	−15 mA	64 mA

SN54S341 (J,FC) SN74S341 (J,N,FN)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 1G̅	11 2A1	1 1G̅	15 2A1
2 1A1	12 1Y4	2 1A1	16 nc
3 2Y4	13 2A2	3 nc	17 nc
4 1A2	14 1Y3	4 nc	18 nc
5 2Y3	15 2A3	5 2Y4	19 1Y4
6 1A3	16 1Y2	6 1A2	20 2A2
7 2Y2	17 2A4	7 2Y3	21 1Y3
8 1A4	18 1Y1	8 1A3	22 2A3
9 2Y1	19 2G	9 2Y2	23 1Y2
10 GND	20 V_{CC}	10 1A4	24 2A4
		11 nc	25 1Y1
		12 2Y1	26 nc
		13 nc	27 2G
		14 GND	28 V_{CC}

344

OCTAL BUFFERS/ LINE DRIVERS

(three-state non-inverted outputs)

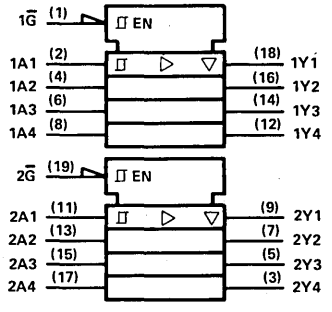
- 300 mV guaranteed hysteresis

typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT
'S344	9 ns	−15 mA	64 mA

SN54S344 (J,FC) SN74S344 (J,N,FN)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 1G̅	11 2A1	1 1G̅	15 2A1
2 1A1	12 1Y4	2 1A1	16 nc
3 2Y4	13 2A2	3 nc	17 nc
4 1A2	14 1Y3	4 nc	18 nc
5 2Y3	15 2A3	5 2Y4	19 1Y4
6 1A3	16 1Y2	6 1A2	20 2A2
7 2Y2	17 2A4	7 2Y3	21 1Y3
8 1A4	18 1Y1	8 1A3	22 2A3
9 2Y1	19 2G̅	9 2Y2	23 1Y2
10 GND	20 V_{CC}	10 1A4	24 2A4
		11 nc	25 1Y1
		12 2Y1	26 nc
		13 nc	27 2G̅
		14 GND	28 V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

347

BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

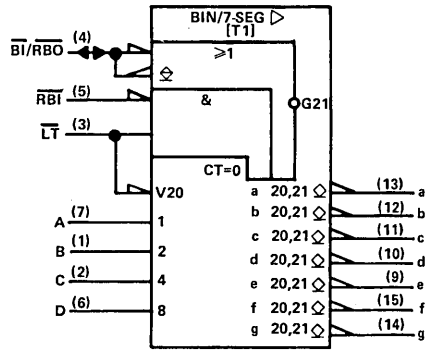
(open-collector outputs, low-voltage version of 'LS47)

typical performance

TYPE	OUTPUT SINK CURRENT	OFF-STATE OUTPUT VOLTAGE	POWER
SN54LS347	12 mA	7 V	35 mW
SN74LS347	24 mA	7 V	35 mW

SN54LS347 (J) SN74LS347 (J,N)

logic symbol†



pin assignments

J, N PACKAGES	
1 B	9 e
2 C	10 d
3 $\overline{LT}$	11 c
4 $\overline{BI}$/$\overline{RBO}$	12 b
5 $\overline{RBI}$	13 a
6 D	14 g
7 A	15 f
8 GND	16 V_{CC}

See *TTL Data Book*

348

8-LINE TO 3-LINE PRIORITY ENCODERS

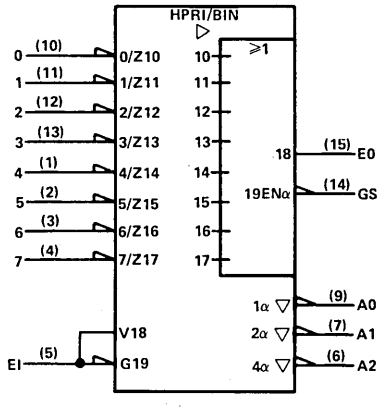
(with three-state outputs)

typical performance

TYPE	DELAY	POWER
'LS348	16 ns	63 mW

SN54LS348 (J,FC) SN74LS348 (J,N)

logic symbol†



pin assignments

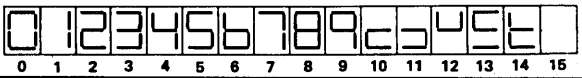
J, N PACKAGES		FC, FN PACKAGES	
1 4	9 A0	1 4	11 A0
2 5	10 0	2 5	12 0
3 6	11 1	3 nc	13 nc
4 7	12 2	4 6	14 1
5 EI	13 3	5 7	15 2
6 A2	14 GS	6 EI	16 3
7 A1	15 EO	7 A2	17 GS
8 GND	16 V_{CC}	8 nc	18 nc
		9 A1	19 EO
		10 GND	20 V_{CC}

See *TTL Data Book*

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

FONT TABLE T1 — NUMERICAL DESIGNATIONS AND RESULTANT DISPLAYS USING 'LS347



351

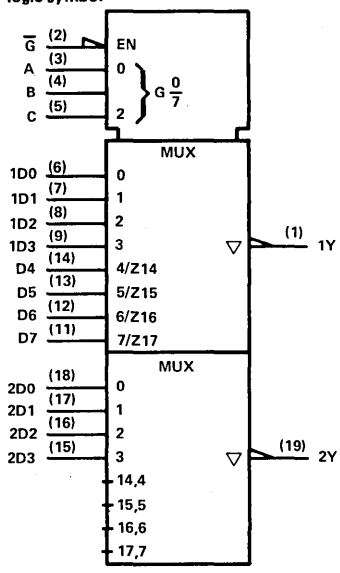
DUAL 8-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS
(three-state outputs; four common data inputs)

typical performance

TYPE	DELAY TIMES		TOTAL POWER
	DATA TO INV OUTPUT	FROM ENABLE	
'351	10 ns	17 ns	220 mW

SN54351 (J) SN74351 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES	
1 1Y	11 D7
2 $\overline{G}$	12 D6
3 A	13 D5
4 B	14 D4
5 C	15 2D3
6 1D0	16 2D2
7 1D1	17 2D1
8 1D2	18 2D0
9 1D3	19 2Y
10 GND	20 V_{CC}

352

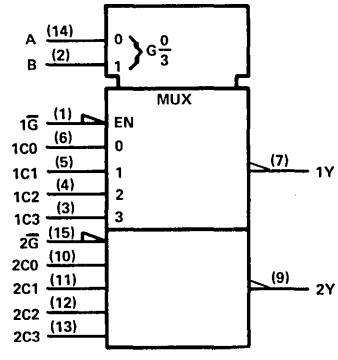
DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS
(inverting version of 'LS153)

typical performance

TYPE	DELAY TIMES		TOTAL POWER
	DATA TO INV OUTPUT	FROM ENABLE	
'LS352	15 ns	22 ns	31 mW

SN54LS352 (J,FC) SN74LS352 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 1$\overline{G}$	9 2Y	1 1$\overline{G}$	11 2Y
2 B	10 2C0	2 B	12 2C0
3 1C3	11 2C1	3 nc	13 nc
4 1C2	12 2C2	4 1C3	14 2C1
5 1C1	13 2C3	5 1C2	15 2C2
6 1C0	14 A	6 1C1	16 2C3
7 1Y	15 2$\overline{G}$	7 1C0	17 A
8 GND	16 V_{CC}	8 nc	18 nc
		9 1Y	19 2$\overline{G}$
		10 GND	20 V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

353

DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

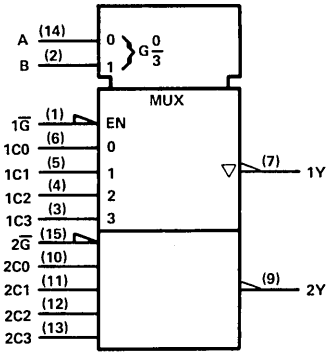
(three-state outputs, inverting version of 'LS253

typical performance

TYPE	DELAY TIMES		TOTAL POWER
	DATA TO INV OUTPUT	FROM ENABLE	
'LS353	12 ns	21 ns	43 mW

SN54LS353 (J,FC) SN74LS353 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 1G̅	9 2Y	1 1G̅	11 2Y
2 B	10 2C0	2 B	12 2C0
3 1C3	11 2C1	3 nc	13 nc
4 1C2	12 2C2	4 1C3	14 2C1
5 1C1	13 2C3	5 1C2	15 2C2
6 1C0	14 A	6 1C1	16 2C3
7 1Y	15 2G̅	7 1C0	17 A
8 GND	16 V_{CC}	8 nc	18 nc
		9 1Y	19 2G̅
		10 GND	20 V_{CC}

354

8-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS/ TRANSPARENT REGISTERS

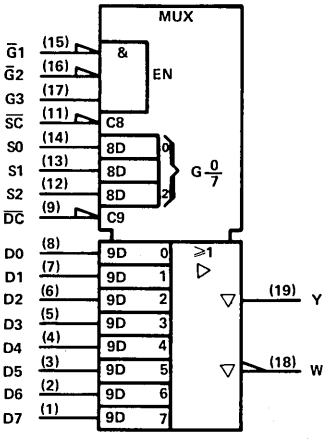
(three-state outputs)

typical performance

TYPE	DELAY TIMES		
	DATA TO INV OUTPUT	DATA TO NON-INV OUTPUT	FROM ENABLE
'LS354	27.5 ns	27 ns	33 ns

SN54LS354 (J,FC) SN74LS354 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 D7	11 SC̅	1 D7	11 SC̅
2 D6	12 S2	2 D6	12 S2
3 D5	13 S1	3 D5	13 S1
4 D4	14 S0	4 D4	14 S0
5 D3	15 G1̅	5 D3	15 G1̅
6 D2	16 G2̅	6 D2	16 G2̅
7 D1	17 G3	7 D1	17 G3
8 D0	18 W	8 D0	18 W
9 DC̅	19 Y	9 DC̅	19 Y
10 GND	20 V_{CC}	10 GND	20 V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

8

355

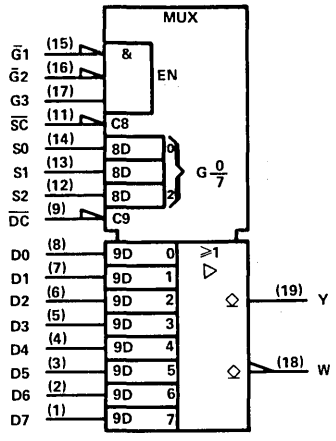
8-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS/ TRANSPARENT REGISTERS
(open-collector outputs)

typical performance

DELAY TIMES		
DATA TO INV OUTPUT	DATA TO NON-INV OUTPUT	FROM ENABLE
36 ns	34.5 ns	44 ns

SN54LS355 (J,FC) SN74LS355 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 D7	11 $\overline{SC}$	1 D7	11 $\overline{SC}$
2 D6	12 S2	2 D6	12 S2
3 D5	13 S1	3 D5	13 S1
4 D4	14 S0	4 D4	14 S0
5 D3	15 $\overline{G1}$	5 D3	15 $\overline{G1}$
6 D2	16 $\overline{G2}$	6 D2	16 $\overline{G2}$
7 D1	17 G3	7 D1	17 G3
8 D0	18 W	8 D0	18 W
9 $\overline{DC}$	19 Y	9 $\overline{DC}$	19 Y
10 GND	20 V_{CC}	10 GND	20 V_{CC}

356

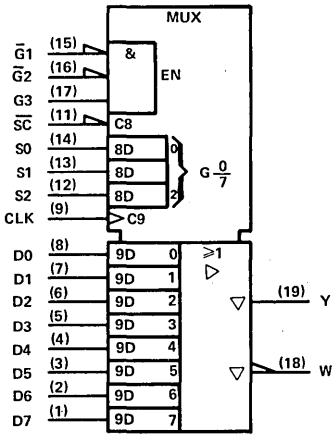
8-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS/ EDGE-TRIGGERED REGISTERS
(three-state output)

typical performance

DELAY TIMES		
DATA TO INV OUTPUT	DATA TO NON-INV OUTPUT	FROM ENABLE
21 ns	25.5 ns	36 ns

SN54LS356 (J,FC) SN74LS356 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 D7	11 $\overline{SC}$	1 D7	11 $\overline{SC}$
2 D6	12 S2	2 D6	12 S2
3 D5	13 S1	3 D5	13 S1
4 D4	14 S0	4 D4	14 S0
5 D3	15 $\overline{G1}$	5 D3	15 $\overline{G1}$
6 D2	16 $\overline{G2}$	6 D2	16 $\overline{G2}$
7 D1	17 G3	7 D1	17 G3
8 D0	18 W	8 D0	18 W
9 CLK	19 Y	9 CLK	19 Y
10 GND	20 V_{CC}	10 GND	20 V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

357

8-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS/ EDGE-TRIGGERED REGISTERS

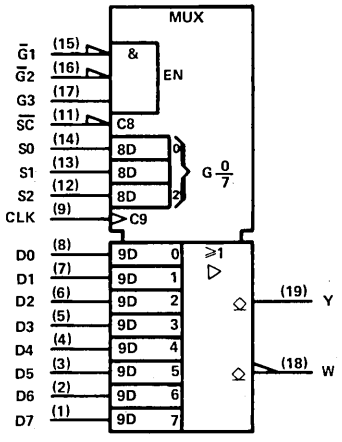
(open-collector outputs)

typical performance

DELAY TIMES		
DATA TO INV OUTPUT	DATA TO NON-INV OUTPUT	FROM ENABLE
27.5 ns	30.5 ns	42 ns

SN54LS357 (J,FC) SN74LS357 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 D7	11 $\overline{SC}$	1 D7	11 $\overline{SC}$
2 D6	12 S2	2 D6	12 S2
3 D5	13 S1	3 D5	13 S1
4 D4	14 S0	4 D4	14 S0
5 D3	15 $\overline{G1}$	5 D3	15 $\overline{G1}$
6 D2	16 $\overline{G2}$	6 D2	16 $\overline{G2}$
7 D1	17 G3	7 D1	17 G3
8 D0	18 W	8 D0	18 W
9 CLK	19 Y	9 CLK	19 Y
10 GND	20 V_{CC}	10 GND	20 V_{CC}

365

HEX BUS DRIVERS

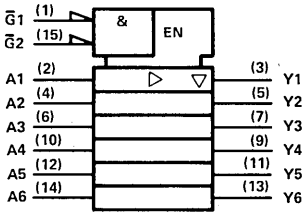
(non-inverted three-state outputs, gated enable inputs)

typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54365A	12 ns	−2 mA	32 mA
SN74365A	12 ns	−5.2 mA	32 mA
SN54LS365A	9.5 ns	−1 mA	12 mA
SN74LS365A	9.5 ns	−2.6 mA	24 mA

SN54365A (J,FC) SN74365A (J,N)
SN54LS365A (J,FC) SN74LS365A (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 $\overline{G1}$	9 Y4	1 $\overline{G1}$	11 Y4
2 A1	10 A4	2 nc	12 A4
3 Y1	11 Y5	3 nc	13 nc
4 A2	12 A5	4 A1	14 nc
5 Y2	13 Y6	5 Y1	15 Y5
6 A3	14 A6	6 A2	16 A5
7 Y3	15 $\overline{G2}$	7 Y2	17 Y6
8 GND	16 V_{CC}	8 A3	18 A6
		9 Y3	19 $\overline{G2}$
		10 GND	20 V_{CC}

366

HEX BUS DRIVERS

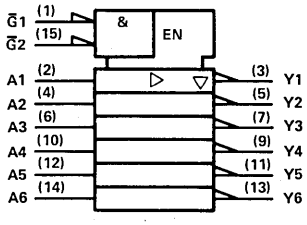
(inverted three-state outputs, gated enable inputs)

typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54366A	11 ns	−2 mA	32 mA
SN74366A	11 ns	−5.2 mA	32 mA
SN54LS366A	9.5 ns	−1 mA	12 mA
SN74LS366A	9.5 ns	−2.6 mA	24 mA

SN54366A (J,FC) SN74366A (J,N)
SN54LS366A (J,FC) SN74LS366A (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 $\overline{G1}$	9 Y4	1 $\overline{G1}$	11 Y4
2 A1	10 A4	2 nc	12 A4
3 Y1	11 Y5	3 nc	13 nc
4 A2	12 A5	4 A1	14 nc
5 Y2	13 Y6	5 Y1	15 Y5
6 A3	14 A6	6 A2	16 A5
7 Y3	15 $\overline{G2}$	7 Y2	17 Y6
8 GND	16 V_{CC}	8 A3	18 A6
		9 Y3	19 $\overline{G2}$
		10 GND	20 V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

8

367

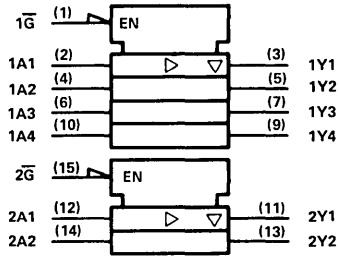
HEX BUS DRIVERS
(non-inverted three-state outputs organized to facilitate handling of 4-bit data)

typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54367A	12 ns	−2 mA	32 mA
SN74367A	12 ns	−5.2 mA	32 mA
SN54LS367A	9.5 ns	−1 mA	12 mA
SN74LS367A	9.5 ns	−2.6 mA	24 mA

SN54367A (J,FC) SN74367A (J,N)
SN54LS367A (J,FC) SN74LS367A (J,N)

logic symbol†



pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	1$\overline{G}$	9	1Y4	1	1$\overline{G}$	11	1Y4
2	1A1	10	1A4	2	nc	12	1A4
3	1Y1	11	2Y1	3	nc	13	nc
4	1A2	12	2A1	4	1A1	14	nc
5	1Y2	13	2Y2	5	1Y1	15	2Y1
6	1A3	14	2A2	6	1A2	16	2A1
7	1Y3	15	2$\overline{G}$	7	1Y2	17	2Y2
8	GND	16	V_{CC}	8	1A3	18	2A2
				9	1Y3	19	2$\overline{G}$
				10	GND	20	V_{CC}

See *TTL Data Book*

368

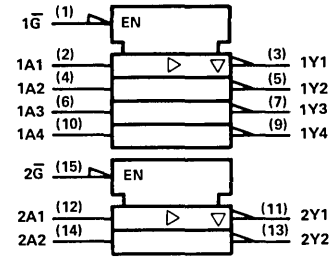
HEX BUS DRIVERS
(inverted three-state outputs organized to facilitate handling of 4-bit data)

typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54368A	11 ns	−2 mA	32 mA
SN74368A	11 ns	−5.2 mA	32 mA
SN54LS368A	9.5 ns	−1 mA	12 mA
SN74LS368A	9.5 ns	−2.6 mA	24 mA

SN54368A (J,FC) SN74368A (J,N)
SN54LS368A (J,FC) SN74LS368A (J,N)

logic symbol†



pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	1$\overline{G}$	9	1Y4	1	1$\overline{G}$	11	1Y4
2	1A1	10	1A4	2	nc	12	1A4
3	1Y1	11	2Y1	3	nc	13	nc
4	1A2	12	2A1	4	1A1	14	nc
5	1Y2	13	2Y2	5	1Y1	15	2Y1
6	1A3	14	2A2	6	1A2	16	2A1
7	1Y3	15	2$\overline{G}$	7	1Y2	17	2Y2
8	GND	16	V_{CC}	8	1A3	18	2A2
				9	1Y3	19	2$\overline{G}$
				10	GND	20	V_{CC}

See *TTL Data Book*

370

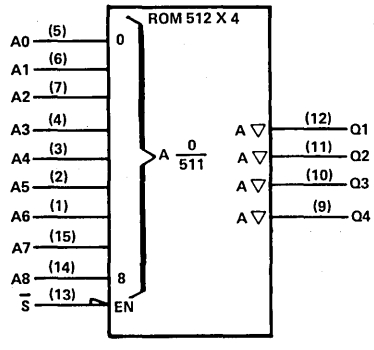
2048-BIT READ-ONLY MEMORIES
(512 4-bit words; three-state outputs)

typical performance

TYPE	ADDRESS TIME	ENABLE TIME	POWER/ BIT
'S370	45 ns	15 ns	0.26 mW

SN54S370 (J,FC) SN74S370 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	A6	9	Q4	1	A6	15	Q4
2	A5	10	Q3	2	A5	16	Q3
3	A4	11	Q2	3	A4	17	nc
4	A3	12	Q1	4	nc	18	nc
5	A0	13	$\overline{S}$	5	A3	19	nc
6	A1	14	A8	6	A0	20	Q2
7	A2	15	A7	7	nc	21	Q1
8	GND	16	V_{CC}	8	nc	22	$\overline{S}$
				9	nc	23	A8
				10	A1	24	nc
				11	A2	25	A7
				12	nc	26	nc
				13	nc	27	nc
				14	GND	28	V_{CC}

For more information contact the factory.

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

371

2048-BIT READ-ONLY MEMORIES
(256 8-bit words; three-state outputs)

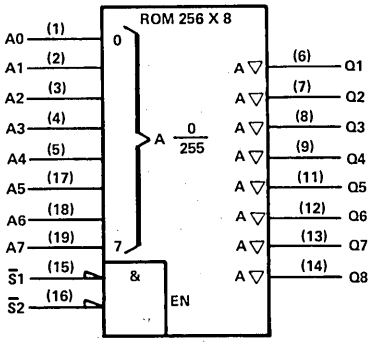
typical performance

TYPE	ADDRESS TIME	ENABLE TIME	POWER/ BIT
'S371	45 ns	15 ns	0.26 mW

SN54S371 (J,FC) SN74S371 (J,N,FN)

For more information contact the factory.

logic symbol†



pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 A0	11 Q5	1 A0	15 Q5
2 A1	12 Q6	2 A1	16 Q6
3 A2	13 Q7	3 A2	17 nc
4 A3	14 Q8	4 nc	18 Q7
5 A4	15 $\overline{S1}$	5 A3	19 Q8
6 Q1	16 $\overline{S2}$	6 A4	20 nc
7 Q2	17 A5	7 nc	21 $\overline{S1}$
8 Q3	18 A6	8 nc	22 $\overline{S2}$
9 Q4	19 A7	9 Q1	23 A5
10 GND	20 V_{CC}	10 Q2	24 nc
		11 nc	25 A6
		12 Q3	26 A7
		13 Q4	27 nc
		14 GND	28 V_{CC}

373

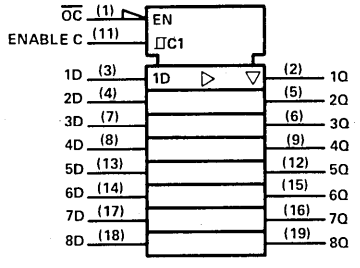
OCTAL D-TYPE LATCHES
(three-state outputs, common output control, common enable)

typical performance

TYPE	OUT-PUTS	DELAY	TOTAL POWER
'LS373	Q	19 ns	120 mW
'S373	Q	7 ns	525 mW

SN54LS373 (J,FC) SN74LS373 (J,N)
SN54S373 (J,FC) SN74S373 (J,N,FN)

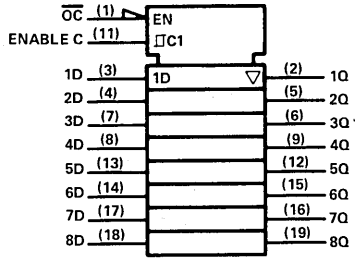
logic symbol, 'LS373†



pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 $\overline{OC}$	11 EN C	1 $\overline{OC}$	11 EN C
2 1Q	12 5Q	2 1Q	12 5Q
3 1D	13 5D	3 1D	13 5D
4 2D	14 6D	4 2D	14 6D
5 2Q	15 6Q	5 2Q	15 6Q
6 3Q	16 7Q	6 3Q	16 7Q
7 3D	17 7D	7 3D	17 7D
8 4D	18 8D	8 4D	18 8D
9 4Q	19 8Q	9 4Q	19 8Q
10 GND	20 V_{CC}	10 GND	20 V_{CC}

logic symbol, 'S373†



See *TTL Data Book*

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

374

OCTAL D-TYPE FLIP-FLOPS
(three-state outputs, common output control, common clock)

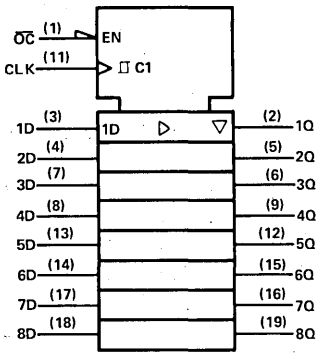
typical performance

TYPE	FREQ	POWER PER F-F	DATA TIMES SET-UP	DATA TIMES HOLD
'LS374	50 MHz	17 mW	20 ns†	0 ns†
'S374	100 MHz	56 mW	5 ns†	2 ns†

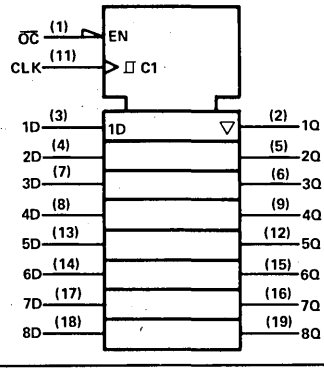
† Rising edge of clock pulse

SN54LS374 (J,FC) SN74LS374 (J,N)
SN54S374 (J,FC) SN74S374 (J,N,FN)

logic symbol, 'LS374†



logic symbol, 'S374†



pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 $\overline{OC}$	11 CLK	1 $\overline{OC}$	11 CLK
2 1Q	12 5Q	2 1Q	12 5Q
3 1D	13 5D	3 1D	13 5D
4 2D	14 6D	4 2D	14 6D
5 2Q	15 6Q	5 2Q	15 6Q
6 3Q	16 7Q	6 3Q	16 7Q
7 3D	17 7D	7 3D	17 7D
8 4D	18 8D	8 4D	18 8D
9 4Q	19 8Q	9 4Q	19 8Q
10 GND	20 V_{CC}	10 GND	20 V_{CC}

See *TTL Data Book*

375

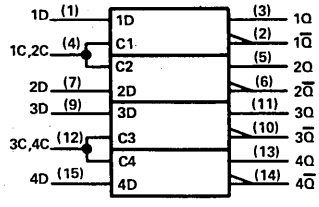
4-BIT BISTABLE LATCHES

typical performance

OUTPUTS	DELAY	TOTAL POWER
Q,$\overline{Q}$	12 ns	32 mW

SN54LS375 (J,FC) SN74LS375 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 1D	9 3D	1 1D	11 3D
2 1Q	10 3Q	2 1Q	12 3Q
3 1Q	11 3Q	3 nc	13 nc
4 1C,2C	12 3C,4C	4 1Q	14 3Q
5 2Q	13 4Q	5 1C,2C	15 3C,4C
6 2Q	14 4Q	6 2Q	16 4Q
7 2D	15 4D	7 2Q	17 4Q
8 GND	16 V_{CC}	8 nc	18 nc
		9 2D	19 4D
		10 GND	20 V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

376

QUAD J-$\overline{K}$ FLIP-FLOPS
(common clock, common clear)

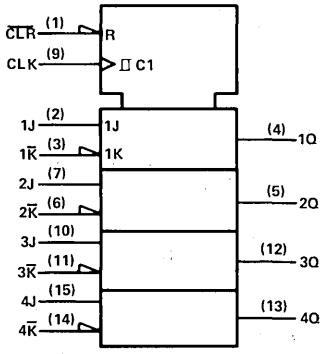
typical performance

FREQ	POWER PER F-F	DATA TIMES SET-UP	DATA TIMES HOLD
45 MHz	65 mW	0 ns†	20 ns†

† Rising edge of clock pulse

SN54376 (J) SN74376 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES	
1 $\overline{CLR}$	9 CLK
2 1J	10 3J
3 1$\overline{K}$	11 3$\overline{K}$
4 1Q	12 3Q
5 2Q	13 4Q
6 2$\overline{K}$	14 4$\overline{K}$
7 2J	15 4J
8 GND	16 V_{CC}

377

OCTAL D-TYPE FLIP-FLOPS
(single-rail outputs, common enable, common clock)

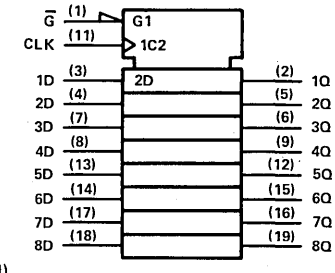
typical performance

FREQ	POWER PER F-F	DATA TIMES SET-UP	DATA TIMES HOLD
40 MHz	10.6 mW	20 ns†	5 ns†

† Rising edge of clock pulse

SN54LS377 (J,FC) SN74LS377 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 G	11 CLK	1 G	11 CLK
2 1Q	12 5Q	2 1Q	12 5Q
3 1D	13 5D	3 1D	13 5D
4 2D	14 6D	4 2D	14 6D
5 2Q	15 6Q	5 2Q	15 6Q
6 3Q	16 7Q	6 3Q	16 7Q
7 3D	17 7D	7 3D	17 7D
8 4D	18 8D	8 4D	18 8D
9 4Q	19 8Q	9 4Q	19 8Q
10 GND	20 V_{CC}	10 GND	20 V_{CC}

378

HEX D-TYPE FLIP-FLOPS
(single-rail outputs, common enable, common clock)

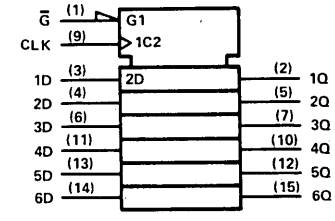
typical performance

FREQ	POWER PER F-F	DATA TIMES SET-UP	DATA TIMES HOLD
40 MHz	10.6 mW	20 ns†	5 ns†

† Rising edge of clock pulse

SN54LS378 (J,FC) SN74LS378 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 G	9 CLK	1 G	11 CLK
2 1Q	10 4Q	2 1Q	12 4Q
3 1D	11 4D	3 1D	13 nc
4 2D	12 5Q	4 nc	14 4D
5 2Q	13 5D	5 2D	15 5Q
6 3D	14 6D	6 2Q	16 5D
7 3Q	15 6Q	7 3D	17 6D
8 GND	16 V_{CC}	8 nc	18 nc
		9 3Q	19 6Q
		10 GND	20 V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

8

379

QUAD D-TYPE FLIP-FLOPS
(double-rail outputs, common enable, common clock)

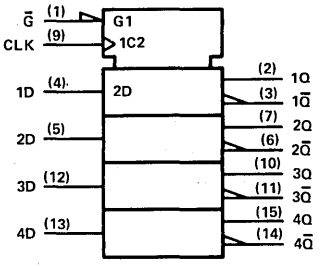
typical performance

FREQ	POWER PER F-F	DATA TIMES SET-UP	DATA TIMES HOLD
40 MHz	10.6 mW	20 ns†	5 ns†

† Rising edge of clock pulse

SN54LS379 (J,FC) SN74LS379 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 G̅	9 CLK	1 G̅	11 CLK
2 1Q	10 3Q	2 1Q	12 3Q
3 1Q̄	11 3Q̄	3 nc	13 3Q̄
4 1D	12 3D	4 nc	14 nc
5 2D	13 4D	5 1Q̄	15 3D
6 2Q̄	14 4Q̄	6 1D	16 4D
7 2Q	15 4Q	7 2D	17 4Q̄
8 GND	16 V_{CC}	8 2Q̄	18 nc
		9 2Q	19 4Q
		10 GND	20 V_{CC}

381

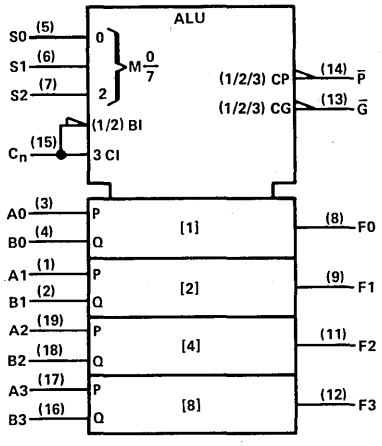
ARITHMETIC LOGIC UNITS/ FUNCTION GENERATORS
(8 binary functions, use 'S182 for look-ahead carry)

typical performance

TYPE	CARRY TIME	ADD TIME	TOTAL POWER
'LS381	16 ns	21 ns	175 mW
'S381	11 ns	20 ns	525 mW

SN54LS381 (J,FC) SN74LS381 (J,N)
SN54S381 (J,FC) SN74S381 (J,N,FN)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 A1	11 F2	1 A1	11 F2
2 B1	12 F3	2 B1	12 F3
3 A0	13 G̅	3 A0	13 G̅
4 B0	14 P̄	4 B0	14 P̄
5 S0	15 C_n	5 S0	15 C_n
6 S1	16 B3	6 S1	16 B3
7 S2	17 A3	7 S2	17 A3
8 F0	18 B2	8 F0	18 B2
9 F1	19 A2	9 F1	19 A2
10 GND	20 V_{CC}	10 GND	20 V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

382

ARITHMETIC LOGIC UNITS/ FUNCTION GENERATORS

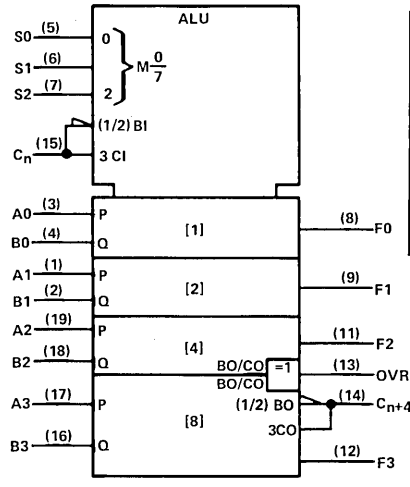
(ripple carry and overflow outputs)

typical performance

TYPE	CARRY TIME	ADD TIME	TOTAL POWER
'LS382	27 ns	18 ns	175 mW

SN54LS382 (J,FC) SN74LS382 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 A1	11 F2	1 A1	11 F2
2 B1	12 F3	2 B1	12 F3
3 A0	13 OVR	3 A0	13 OVR
4 B0	14 C_{n+4}	4 B0	14 C_{n+4}
5 S0	15 C_n	5 S0	15 C_n
6 S1	16 B3	6 S1	16 B3
7 S2	17 A3	7 S2	17 A3
8 F0	18 B2	8 F0	18 B2
9 F1	19 A2	9 F1	19 A2
10 GND	20 V_{CC}	10 GND	20 V_{CC}

384

8-BIT BY 1-BIT TWO'S-COMPLEMENT MULTIPLIERS

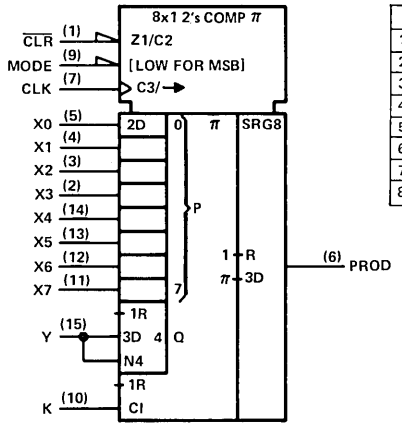
- Magnitude-only multiplication
- Cascadable for any number of bits
- Serial multiplier data input
- Serial data output for multiplication product
- 8-Bit parallel multiplicand data input
- 40 MHz typical max clock frequency

typical performance

MAX CLOCK FREQ	DELAY FROM CLOCK	DELAY FROM CLEAR	TOTAL POWER
40 MHz	15 ns	17 ns	455 mW

SN54LS384 (J,FC) SN74LS384 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 CLR	9 MODE	1 CLR	11 MODE
2 X3	10 K	2 nc	12 K
3 X2	11 X7	3 nc	13 nc
4 X1	12 X6	4 X3	14 X7
5 X0	13 X5	5 X2	15 X6
6 PROD	14 X4	6 X1	16 X5
7 CLK	15 Y	7 X0	17 X4
8 GND	16 V_{CC}	8 PROD	18 nc
		9 CLK	19 Y
		10 GND	20 V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

8

385

QUADRUPLE SERIAL ADDERS/ SUBTRACTORS

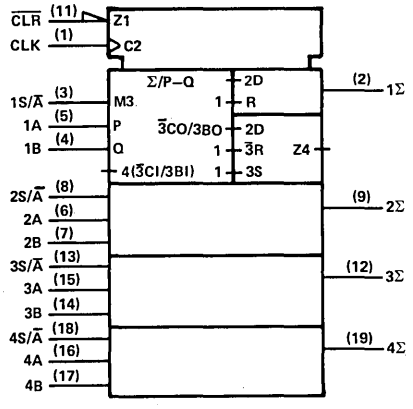
- Buffered clock, direct clear inputs
- Independent two's-complement addition/subtraction

typical performance

f_{max}	DELAY	POWER
40 MHz	16 ns	240 mW

SN54LS385 (J,FC) SN74LS385 (J,N)

logic symbol†



pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 CLK	11 $\overline{CLR}$	1 CLK	11 $\overline{CLR}$
2 1Σ	12 3Σ	2 1Σ	12 3Σ
3 1S/$\overline{A}$	13 3S/$\overline{A}$	3 1S/$\overline{A}$	13 3S/$\overline{A}$
4 1B	14 3B	4 1B	14 3B
5 1A	15 3A	5 1A	15 3A
6 2A	16 4A	6 2A	16 4A
7 2B	17 4B	7 2B	17 4B
8 2S/$\overline{A}$	18 4S/$\overline{A}$	8 2S/$\overline{A}$	18 4S/$\overline{A}$
9 2Σ	19 4Σ	9 2Σ	19 4Σ
10 GND	20 V_{CC}	10 GND	20 V_{CC}

See *TTL Data Book*

386

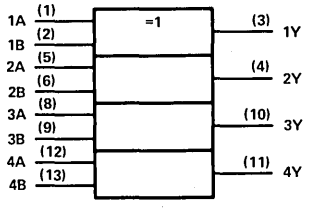
QUAD 2-INPUT EXCLUSIVE-OR GATES

typical performance

TYPE	DELAY	TOTAL POWER
'LS386	10 ns	30 mW

SN54LS386 (J,FC) SN74LS386 (J,N)

logic symbol†



positive logic: $Y = A \oplus B = \overline{A}B + A\overline{B}$

See *TTL Data Book*

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 1A	8 3A	1 nc	11 3A
2 1B	9 3B	2 nc	12 nc
3 1Y	10 3Y	3 1A	13 3B
4 2Y	11 4Y	4 1B	14 nc
5 2A	12 4A	5 1Y	15 3Y
6 2B	13 4B	6 2Y	16 4Y
7 GND	14 V_{CC}	7 2A	17 nc
		8 nc	18 4A
		9 2B	19 4B
		10 GND	20 V_{CC}

387

(This number has been changed to TBP14SA10. Product Guide information for this PROM can be found at the end of this section.)

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

390

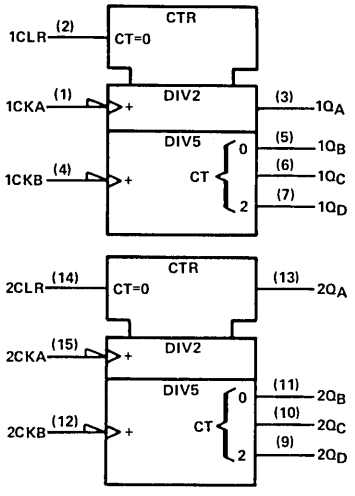
DUAL DECADE COUNTERS
(bi-quinary or bcd sequences)

typical performance

TYPE	COUNT FREQ	CLEAR	TOTAL POWER
'390	25 MHz	HIGH	210 mW
'LS390	35 MHz	HIGH	75 mW

SN54390 (J,FC) SN74390 (J,N)
SN54LS390 (J,FC) SN74LS390 (J,N)

logic symbol†



pin assignments

J, N PACKAGES				FC, FN PACKAGES	
1	1CKA	9	2QD	1 nc	11 nc
2	1CLR	10	2QC	2 1CKA	12 2QD
3	1QA	11	2QB	3 nc	13 nc
4	1CKB	12	2CKB	4 1CLR	14 2QC
5	1QB	13	2QA	5 1QA	15 2QB
6	1QC	14	2CLR	6 1CKB	16 2CKB
7	1QD	15	2CKA	7 1QB	17 2QA
8	GND	16	V_{CC}	8 1QC	18 2CLR
				9 1QD	19 2CKA
				10 GND	20 V_{CC}

See *TTL Data Book*

393

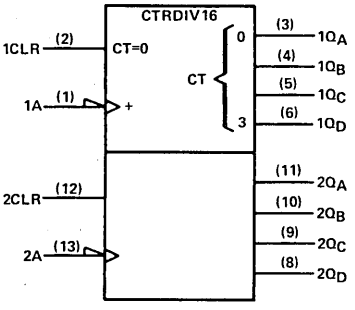
DUAL 4-BIT BINARY COUNTERS

typical performance

TYPE	COUNT FREQ	CLEAR	TOTAL POWER
'393	25 MHz	HIGH	190 mW
'LS393	35 MHz	HIGH	75 mW

SN54393 (J,FC) SN74393 (J,N)
SN54LS393 (J,FC) SN74LS393 (J,N)

logic symbol†



pin assignments

J, N PACKAGES				FC, FN PACKAGES	
1	1A	8	2QD	1 nc	11 nc
2	1CLR	9	2QC	2 1A	12 2QD
3	1QA	10	2QB	3 nc	13 nc
4	1QB	11	2QA	4 1CLR	14 2QC
5	1QC	12	2CLR	5 1QA	15 2QB
6	1QD	13	2A	6 nc	16 nc
7	GND	14	V_{CC}	7 1QB	17 2QA
				8 1QC	18 2CLR
				9 1QD	19 2A
				10 GND	20 V_{CC}

See *TTL Data Book*

395

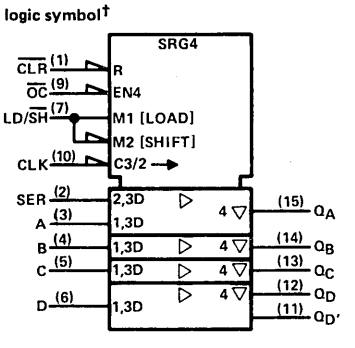
4-BIT UNIVERSAL SHIFT REGISTERS
(three-state outputs)

typical performance

SHIFT FREQ	SERIAL DATA INPUT	ASYNC CLEAR	TOTAL POWER
30 MHz	D	LOW	75 mW

SN54LS395A (J,FC) SN74LS395A (J,N)

logic symbol†



pin assignments

J, N PACKAGES				FC, FN PACKAGES	
1	$\overline{CLR}$	9	$\overline{OC}$	1 $\overline{CLR}$	11 $\overline{OC}$
2	SER	10	CLK	2 SER	12 CLK
3	A	11	QD'	3 nc	13 QD'
4	B	12	QD	4 A	14 nc
5	C	13	QC	5 B	15 QD
6	D	14	QB	6 C	16 QC
7	LD/$\overline{SH}$	15	QA	7 D	17 QB
8	GND	16	V_{CC}	8 nc	18 nc
				9 LD/$\overline{SH}$	19 QA
				10 GND	20 V_{CC}

See *TTL Data Book*

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

8

396

OCTAL STORAGE REGISTERS

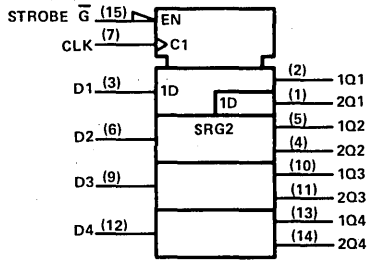
- Parallel access
- Applications:
  - N-bit storage files
  - HEX/BCD serial to parallel converters

typical performance

TYPE	MAX CLOCK FREQ	DELAY	POWER
'LS396	30 MHz	20 ns	120 mW

SN54LS396 (J,FC) SN74LS396 (J,N)

logic symbol†



pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 2Q1	9 D3	1 2Q1	11 D3
2 1Q1	10 1Q3	2 nc	12 nc
3 D1	11 2Q3	3 nc	13 nc
4 2Q2	12 D4	4 1Q1	14 1Q3
5 1Q2	13 1Q4	5 D1	15 2Q3
6 D2	14 2Q4	6 2Q2	16 D4
7 CLK	15 $\overline{G}$	7 1Q2	17 1Q4
8 GND	16 V_{CC}	8 D2	18 2Q4
		9 CLK	19 $\overline{G}$
		10 GND	20 V_{CC}

See *TTL Data Book*

398

QUAD 2-INPUT MULTIPLEXERS WITH STORAGE

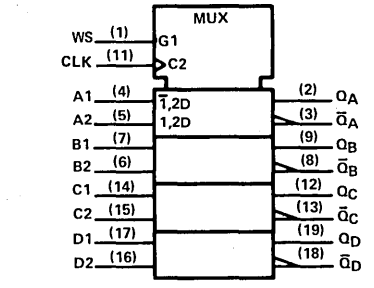
(double-rail outputs)

typical performance

TYPE	DELAY TIMES		TOTAL POWER
	CLOCK TO INV OUTPUT	CLOCK TO NON-INV OUTPUT	
'LS398	20 ns	20 ns	32 mW

SN54LS398 (J,FC) SN74LS398 (J,N)

logic symbol†



pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 WS	11 CLK	1 WS	11 CLK
2 QA	12 QC	2 QA	12 QC
3 $\overline{Q}A$	13 $\overline{Q}C$	3 $\overline{Q}A$	13 $\overline{Q}C$
4 A1	14 C1	4 A1	14 C1
5 A2	15 C2	5 A2	15 C2
6 B2	16 D2	6 B2	16 D2
7 B1	17 D1	7 B1	17 D1
8 $\overline{Q}B$	18 $\overline{Q}D$	8 $\overline{Q}B$	18 $\overline{Q}D$
9 QB	19 QD	9 QB	19 QD
10 GND	20 V_{CC}	10 GND	20 V_{CC}

See *TTL Data Book*

399

QUAD 2-INPUT MULTIPLEXERS WITH STORAGE

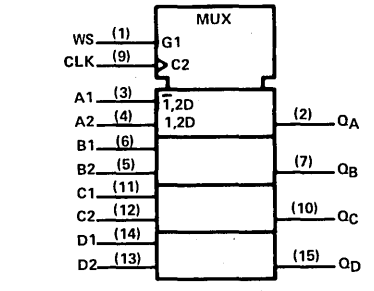
typical performance

TYPE	DELAY	TOTAL POWER
'LS399	20 ns*	37 mW

* From clock to output

SN54LS399 (J,FC) SN74LS399 (J,N)

logic symbol†



pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 WS	9 CLK	1 WS	11 CLK
2 QA	10 QC	2 QA	12 QC
3 A1	11 C1	3 nc	13 nc
4 A2	12 C2	4 A1	14 C1
5 B2	13 D2	5 A2	15 C2
6 B1	14 D1	6 B2	16 D2
7 QB	15 QD	7 B1	17 D1
8 GND	16 V_{CC}	8 nc	18 nc
		9 QB	19 QD
		10 GND	20 V_{CC}

See *TTL Data Book*

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

412

MULTI-MODE BUFFERED 8-BIT LATCHES

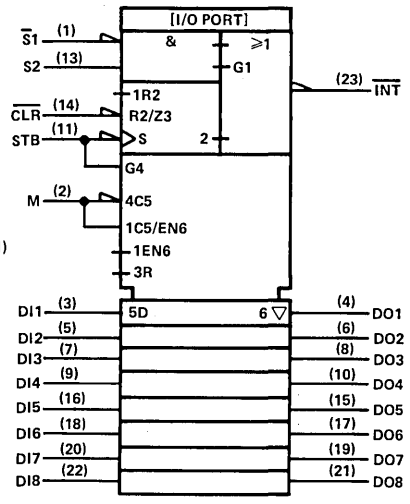
(three-state outputs; direct clear)

typical performance

CLEAR	OUTPUTS	DELAY	TOTAL POWER
LOW	Q	11 ns	410 mW

SN54S412 (J,FC) SN74S412 (J,N,FN)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	S1	13	S2	1	S1	15	S2
2	M	14	CLR	2	M	16	CLR
3	DI1	15	DO5	3	DI1	17	nc
4	DO1	16	DI5	4	nc	18	DO5
5	DI2	17	DO6	5	DO1	19	nc
6	DO2	18	DI6	6	DI2	20	DI5
7	DI3	19	DO7	7	DO2	21	DO6
8	DO3	20	DI7	8	DI3	22	DI6
9	DI4	21	DO8	9	DO3	23	DI7
10	DO4	22	DI8	10	DI4	24	DI7
11	STB	23	INT	11	DO4	25	DO8
12	GND	24	V_{CC}	12	nc	26	DI8
				13	STB	27	INT
				14	GND	28	V_{CC}

422

RE-TRIGGERABLE MONOSTABLE MULTIVIBRATORS

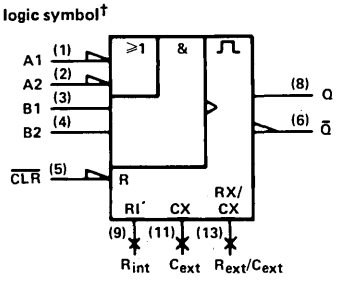
- Internal timing resistor
- Up to 100% duty cycle
- Will not trigger from clear

typical performance

NO. OF INPUTS		OUTPUT PULSE RANGE	TOTAL POWER
HIGH	LOW		
2	2	40 ns-∞	30 mW

SN54LS422 (J,FC) SN74LS422 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	A1	8	Q	1	A1	11	Q
2	A2	9	R_{int}	2	A2	12	R_{int}
3	B1	10	nc	3	nc	13	nc
4	B2	11	C_{ext}	4	B1	14	nc
5	CLR	12	nc	5	B2	15	nc
6	Q̄	13	R_{ext}/C_{ext}	6	CLR	16	C_{ext}
7	GND	14	V_{CC}	7	Q̄	17	R_{ext}/C_{ext}
				8	nc	18	nc
				9	nc	19	nc
				10	GND	20	V_{CC}

423

RE-TRIGGERABLE MONOSTABLE MULTIVIBRATORS

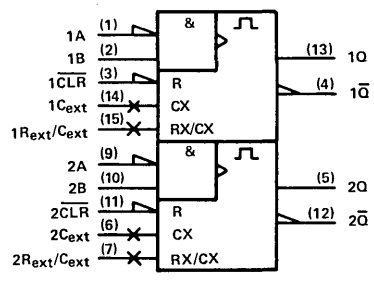
- Up to 100% duty cycle
- Will not trigger from clear

typical performance

NO. OF INPUTS		OUTPUT PULSE RANGE	TOTAL POWER
HIGH	LOW		
1	1	40 ns-∞	60 mW

SN54LS423 (J,FC) SN74LS423 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	1A	9	2A	1	1A	11	2A
2	1B	10	2B	2	1B	12	2B
3	1CLR	11	2CLR	3	nc	13	nc
4	1Q̄	12	2Q̄	4	1CLR	14	nc
5	2Q	13	1Q	5	1Q̄	15	2CLR
6	$2C_{ext}$	14	$1C_{ext}$	6	2Q	16	2Q̄
7	$2R_{ext}/C_{ext}$	15	$1R_{ext}/C_{ext}$	7	$2C_{ext}$	17	1Q
8	GND	16	V_{CC}	8	nc	18	$1C_{ext}$
				9	$2R_{ext}/C_{ext}$	19	$1R_{ext}/C_{ext}$
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

8

425

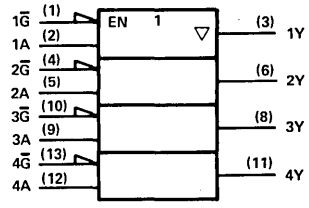
QUAD GATES
(three-state outputs, active-low enabling)

typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54425	10 ns	−2 mA	16 mA
SN74425	10 ns	−5.2 mA	16 mA

SN54425 (J) SN74425 (J,N)

logic symbol†



positive logic: Y = A

pin assignments

J, N PACKAGES	
1 1G̅	8 3Y
2 1A	9 3A
3 1Y	10 3G̅
4 2G̅	11 4Y
5 2A	12 4A
6 2Y	13 4G̅
7 GND	14 V_{CC}

See *TTL Data Book*

426

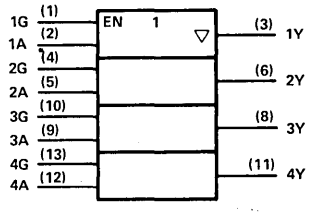
QUAD GATES
(three-state outputs, active-high enabling)

typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54426	10 ns	−2 mA	16 mA
SN74426	10 ns	−5.2 mA	16 mA

SN54426 (J) SN74426 (J,N)

logic symbol†



positive logic: Y = A

pin assignments

J, N PACKAGES	
1 1G	8 3Y
2 1A	9 3A
3 1Y	10 3G
4 2G	11 4Y
5 2A	12 4A
6 2Y	13 4G
7 GND	14 V_{CC}

See *TTL Data Book*

428, 438

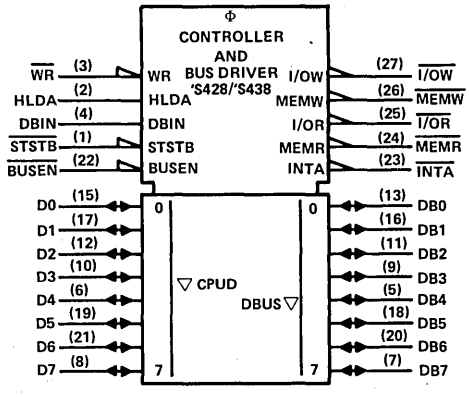
SYSTEM CONTROLLER FOR 8080A

typical performance

TYPE	POWER
'S428	700 mW
'S438	700 mW

SN74S428 (J,N,FN)
SN74S438 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 STSTB	15 D0	1 STSTB	15 D0
2 HLDA	16 DB1	2 HLDA	16 DB1
3 WR	17 D1	3 WR	17 D1
4 DBIN	18 DB5	4 DBIN	18 DB5
5 DB4	19 D5	5 DB4	19 D5
6 D4	20 DB6	6 D4	20 DB6
7 DB7	21 D6	7 DB7	21 D6
8 D7	22 BUSEN	8 D7	22 BUSEN
9 DB3	23 INTA	9 DB3	23 INTA
10 D3	24 MEMR	10 D3	24 MEMR
11 DB2	25 I/OR	11 DB2	25 I/OR
12 D2	26 MEMW	12 D2	26 MEMW
13 DB0	27 I/OW	13 DB0	27 I/OW
14 GND	28 V_{CC}	14 GND	28 V_{CC}

See *TTL Data Book*

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

436, 437

LINE DRIVER/MEMORY DRIVER CIRCUITS – MOS MEMORY INTERFACE

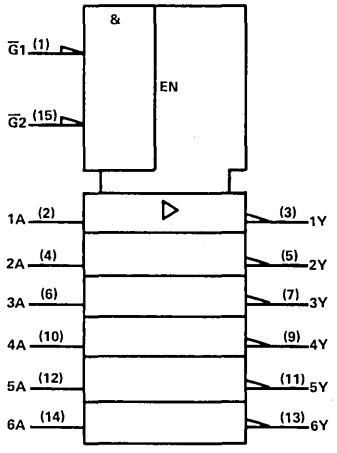
- Drives high-impedance loads
- Provides high-speed switching
- Requires minimum input current
- Damping output resistor for reducing transients ('436)
- Total power . . . 70 mW

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT	DELAY
'S436	150 mA	–1 mA	5.5 ns
'S437	150 mA	–1 mA	5.5 ns

SN54S436 (J) SN74S436 (J,N)
SN54S437 (J) SN74S437 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES	
1 $\overline{G1}$	9 4Y
2 1A	10 4A
3 1Y	11 5Y
4 2A	12 5A
5 2Y	13 6Y
6 3A	14 6A
7 3Y	15 $\overline{G2}$
8 GND	16 V_{CC}

QUAD TRIDIRECTIONAL BUS TRANSCEIVERS

440 (OPEN-COLLECTOR OUTPUTS, NONINVERTED LOGIC)
441 (OPEN-COLLECTOR OUTPUTS, INVERTED LOGIC)
442 (THREE-STATE OUTPUTS, NONINVERTED LOGIC)
443 (THREE-STATE OUTPUTS, INVERTED LOGIC)
444 (THREE-STATE OUTPUTS, INVERTED AND NONINVERTED LOGIC)
448 (OPEN-COLLECTOR OUTPUTS, INVERTED AND NONINVERTED LOGIC)

typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54LS440	22 ns	–	12 mA
SN74LS440	22 ns	–	24 mA
SN54LS441	15 ns	–	12 mA
SN74LS441	15 ns	–	24 mA
SN54LS442	11.5 ns	–12 mA	12 mA
SN74LS442	11.5 ns	–15 mA	24 mA
SN54LS443	8 ns	–12 mA	12 mA
SN74LS443	8 ns	–15 mA	24 mA
SN54LS444	9 ns	–12 mA	12 mA
SN74LS444	9 ns	–15 mA	24 mA
SN54LS448	17.5 ns	–	12 mA
SN74LS448	17.5 ns	–	24 mA

SN54LS440 (J,FC) SN74LS440 (J,N)
SN54LS441 (J,FC) SN74LS441 (J,N)
SN54LS442 (J,FC) SN74LS442 (J,N)
SN54LS443 (J,FC) SN74LS443 (J,N)
SN54LS444 (J,FC) SN74LS444 (J,N)
SN54LS448 (J,FC) SN74LS448 (J,N)

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 $\overline{CS}$	11 S0	1 $\overline{CS}$	11 S0
2 B1	12 S1	2 B1	12 S1
3 C1	13 A4	3 C1	13 A4
4 C2	14 A3	4 C2	14 A3
5 B2	15 A2	5 B2	15 A2
6 B3	16 A1	6 B3	16 A1
7 C3	17 $\overline{GA}$	7 C3	17 $\overline{GA}$
8 C4	18 $\overline{GB}$	8 C4	18 $\overline{GB}$
9 B4	19 $\overline{GC}$	9 B4	19 $\overline{GC}$
10 GND	20 V_{CC}	10 GND	20 V_{CC}

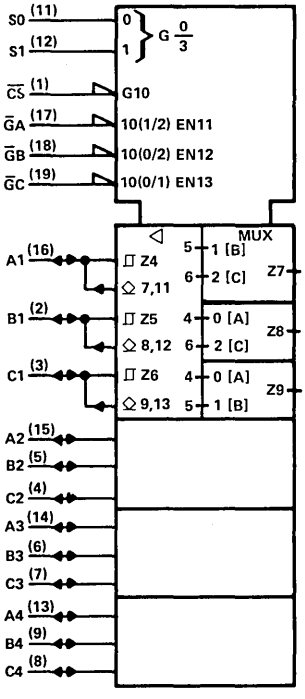
For logic symbols see next two pages.

† Pin numbers shown on logic symbols are for J and N packages only.
nc – no internal connection.

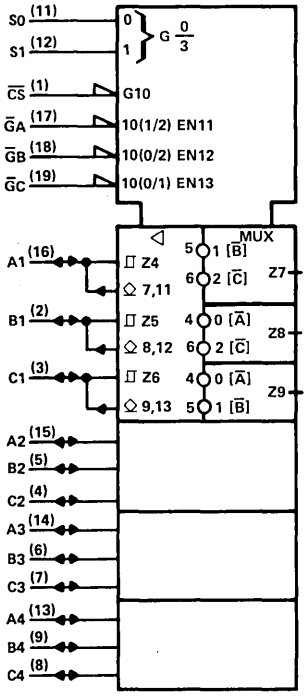
440, 441, 442, 443, 444, 448 (continued)

logic symbol

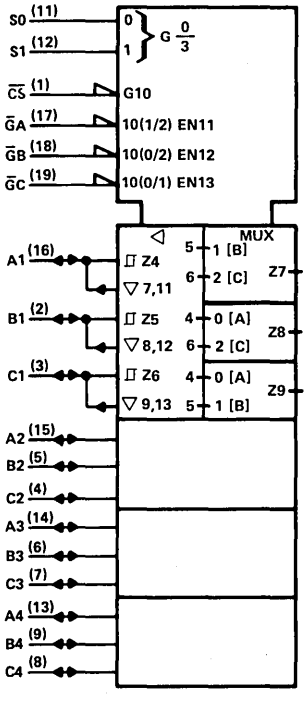
'LS440†



'LS441†



'LS442†



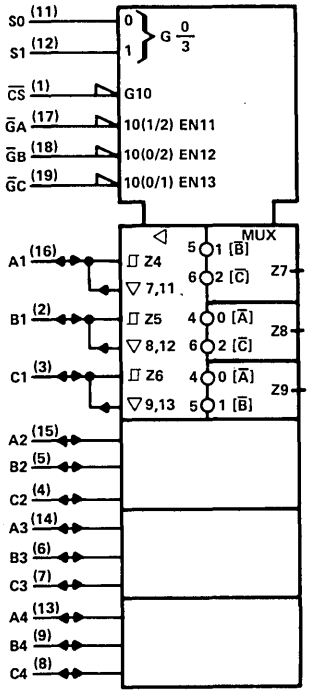
† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

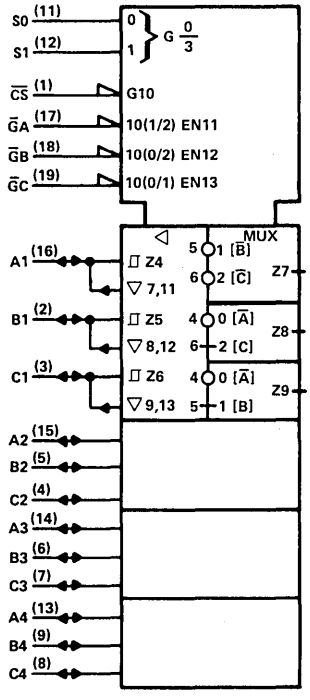
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

440, 441, 442, 443, 444, 448 (continued)

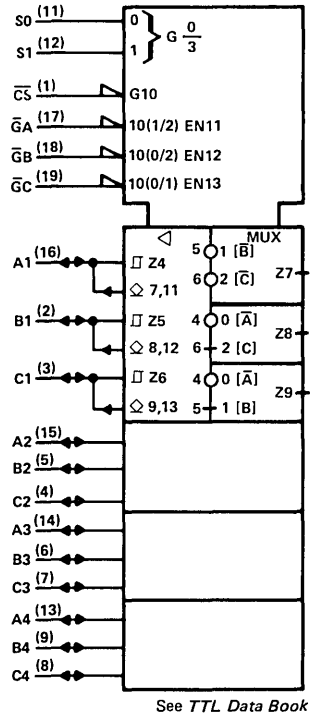
'LS443†



'LS444†



'LS448†



See *TTL Data Book*

445

BCD-TO-DECIMAL DECODERS/DRIVERS

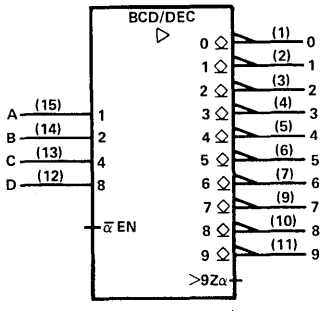
- Use as lamp, relay, or MOS driver
- Low-voltage version of 'LS145
- Full decoding of input logic
- All outputs off for invalid BCD input conditions

typical performance

OUTPUT SINK CURRENT	OFF-STATE OUTPUT VOLTAGE	TOTAL POWER
80 mA	7 V	35 mW

SN54LS445 (J) SN74LS445 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES	
1 0	9 7
2 1	10 8
3 2	11 9
4 3	12 D
5 4	13 C
6 5	14 B
7 6	15 A
8 GND	16 V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

446, 449

QUAD BUS TRANSCEIVERS WITH DIRECTION CONTROLS

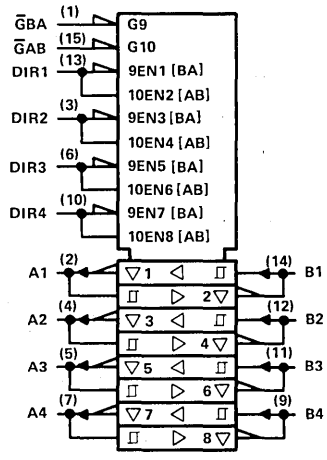
- Three-state outputs
- True ('LS449) and inverting ('LS446) outputs
- P-N-P inputs to reduce dc bus line loading

typical performance

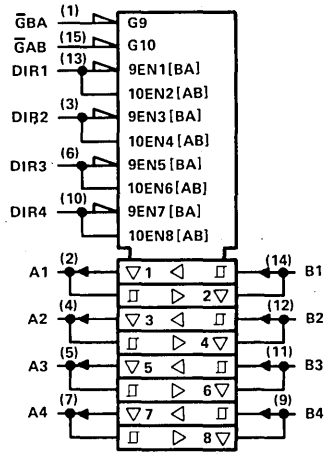
TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54LS446	7.5 ns	−12 mA	12 mA
SN74LS446	7.5 ns	−15 mA	24 mA
SN54LS449	10.5 ns	−12 mA	12 mA
SN74LS449	10.5 ns	−15 mA	24 mA

SN54LS446 (J,FC) SN74LS446 (J,N)
SN54LS449 (J,FC) SN74LS449 (J,N)

logic symbol, 'LS446†



logic symbol, 'LS449†



See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	$\overline{G}$BA	9	B4	1	$\overline{G}$BA	11	B4
2	A1	10	DIR4	2	nc	12	nc
3	DIR2	11	B3	3	nc	13	nc
4	A2	12	B2	4	A1	14	DIR4
5	A3	13	DIR1	5	DIR2	15	B3
6	DIR3	14	B1	6	A2	16	B2
7	A4	15	$\overline{G}$AB	7	A3	17	DIR1
8	GND	16	V_{CC}	8	DIR3	18	B1
				9	A4	19	$\overline{G}$AB
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

447

BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

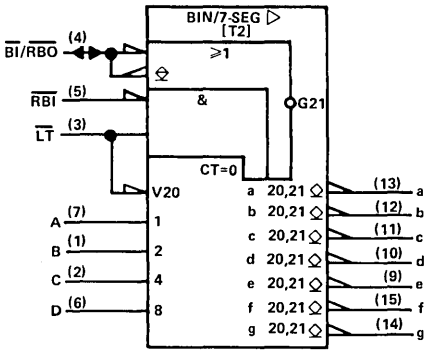
- Low-voltage version of 'LS247
- Open-collector outputs drive indicators directly
- Ripple blanking

typical performance

TYPE	OUTPUT SINK CURRENT	OFF-STATE OUTPUT VOLTAGE	TOTAL POWER
SN54LS447	1.6 mA	7 V	35 mW
SN74LS447	3.2 mA	7 V	35 mW

SN54LS447 (J) SN74LS447 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	B	9	e
2	C	10	d
3	$\overline{LT}$	11	c
4	$\overline{BI}$/$\overline{RBO}$	12	b
5	$\overline{RBI}$	13	a
6	D	14	g
7	A	15	f
8	GND	16	V_{CC}

See *TTL Data Book*

465, 466

OCTAL BUFFERS WITH THREE-STATE OUTPUTS

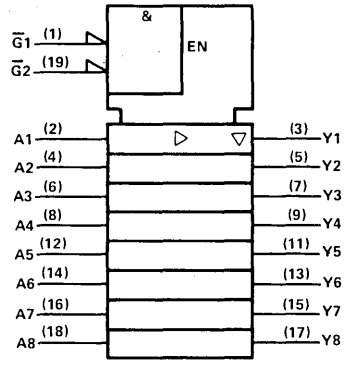
- P-N-P inputs reduce bus loading
- '465 true outputs
- '466 inverted outputs

typical performance

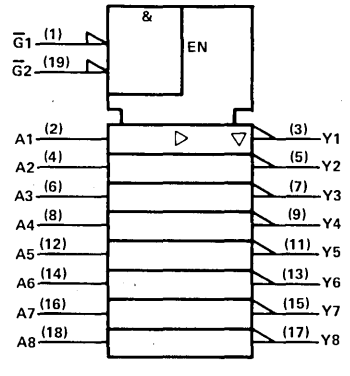
TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54LS465	11 ns	−1 mA	12 mA
SN74LS465	11 ns	−2.5 mA	24 mA
SN54LS466	8 ns	−1 mA	12 mA
SN74LS466	8 ns	−2.5 mA	24 mA

SN54LS465 (J) SN74LS465 (J,N)
SN54LS466 (J) SN74LS466 (J,N)

logic symbol, 'LS465†



logic symbol, 'LS466†



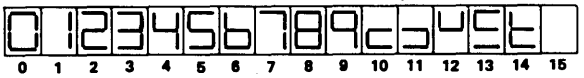
pin assignments

J, N PACKAGES			
1	$\overline{G1}$	11	Y5
2	A1	12	A5
3	Y1	13	Y6
4	A2	14	A6
5	Y2	15	Y7
6	A3	16	A7
7	Y3	17	Y8
8	A4	18	A8
9	Y4	19	$\overline{G2}$
10	GND	20	V_{CC}

See *TTL Data Book*

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

FONT TABLE T2 — NUMERICAL DESIGNATIONS AND RESULTANT DISPLAYS USING '447



8

467, 468

OCTAL BUFFERS WITH THREE-STATE OUTPUTS

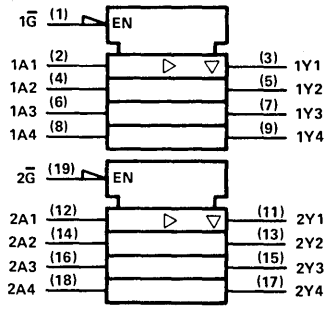
- P-N-P inputs reduce bus loading
- '467 true outputs
- '468 inverted outputs

typical performance

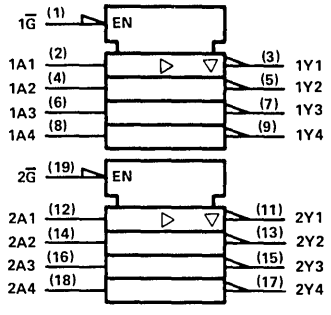
TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54LS467	11 ns	−1 mA	12 mA
SN74LS467	11 ns	−2.5 mA	24 mA
SN54LS468	8 ns	−1 mA	12 mA
SN74LS468	8 ns	−2.5 mA	24 mA

SN54LS467 (J) SN74LS467 (J,N)
SN54LS468 (J) SN74LS468 (J,N)

logic symbol, 'LS467†



logic symbol, 'LS468†



See *TTL Data Book*

pin assignments

J, N PACKAGES			
1	1G̅	11	2Y1
2	1A1	12	2A1
3	1Y1	13	2Y2
4	1A2	14	2A2
5	1Y2	15	2Y3
6	1A3	16	2A3
7	1Y3	17	2Y4
8	1A4	18	2A4
9	1Y4	19	2G̅
10	GND	20	V_{CC}

470

(This number has been changed to TBP18SA22. Product Guide information for this PROM can be found at the end of this section.)

471

(This number has been changed to TBP18S22. Product Guide information for this PROM can be found at the end of this section.)

472

(This number has been changed to TBP18S42. Product Guide information for this PROM can be found at the end of this section.)

473

(This number has been changed to TBP18SA42. Product Guide information for this PROM can be found at the end of this section.)

474

(This number has been changed to TBP18S46. Product Guide information for this PROM can be found at the end of this section.)

475

(This number has been changed to TBP18SA46. Product Guide information for this PROM can be found at the end of this section.)

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

481

4-BIT-SLICE
CASCADABLE
PROCESSOR
ELEMENTS

typical performance

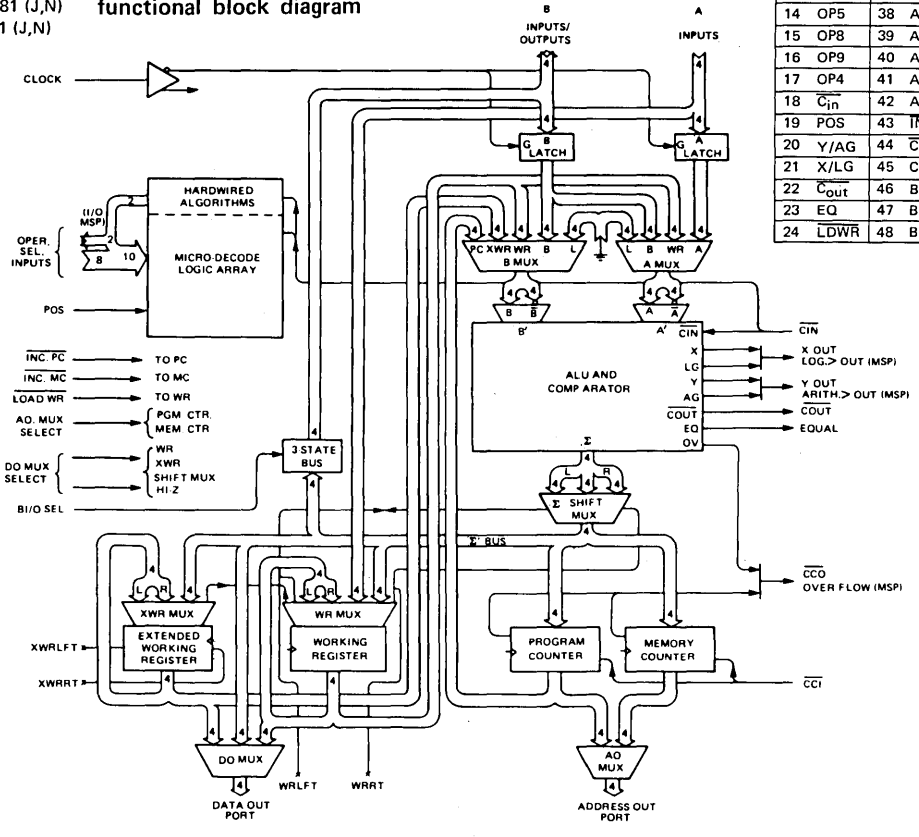
TYPE	OPERATION TIME
'LS481	120 ns
'S481	100 ns

SN74LS481 (J,N)
SN74S481 (J,N)

pin assignments

J, N PACKAGES			
1	BI/02	25	WRLFT
2	BI/03	26	WRRT
3	AI3	27	XWRLFT
4	AI2	28	XWRRT
5	AI1	29	D0
6	AI0	30	D1
7	OP0	31	DOP3
8	OP1	32	DOP2
9	OP2	33	DOP1
10	OP3	34	DOP0
11	OP7	35	$\overline{\text{INC MC}}$
12	V_{CC}	36	GND
13	OP6	37	$\overline{\text{CCO}}$/OV
14	OP5	38	AOP0
15	OP8	39	AOP1
16	OP9	40	AOP2
17	OP4	41	AOP3
18	$\overline{C_{in}}$	42	AOSEL
19	POS	43	$\overline{\text{INC PC}}$
20	Y/AG	44	$\overline{\text{CCI}}$
21	X/LG	45	CLK
22	$\overline{C_{out}}$	46	BI/O0
23	EQ	47	BI/01
24	$\overline{\text{LDWR}}$	48	BI/O SEL

functional block diagram



See Page 3-3

482

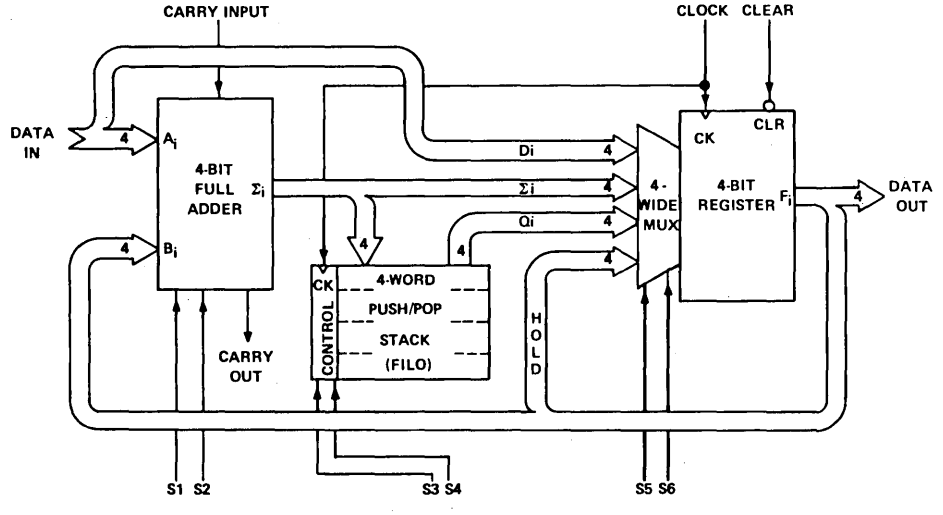
4-BIT-SLICE EXPANDABLE CONTROL ELEMENTS

SN54S482 (J,FC)
SN74S482 (J,N,FN)

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	S4	11	A0	1	S4	15	A0
2	S3	12	F3	2	nc	16	nc
3	C_{out}	13	F2	3	S3	17	F3
4	C_{in}	14	F1	4	nc	18	nc
5	S1	15	F0	5	C_{out}	19	F2
6	S2	16	$\overline{CLR}$	6	C_{in}	20	F1
7	A3	17	S6	7	S1	21	F0
8	A2	18	S5	8	S2	22	nc
9	A1	19	CLK	9	A3	23	$\overline{CLR}$
10	GND	20	V_{CC}	10	A2	24	S6
				11	nc	25	S5
				12	nc	26	nc
				13	A1	27	CLK
				14	GND	28	V_{CC}

functional block diagram



See Page 3-57.

nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

484, 485

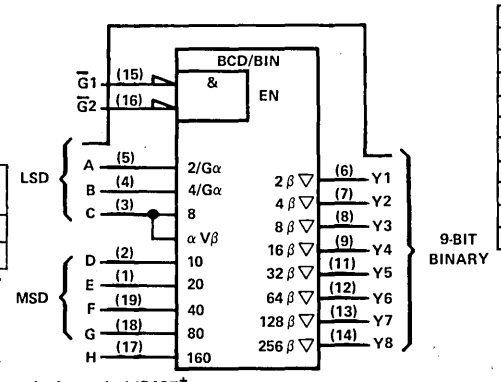
BCD-TO-BINARY AND BINARY-TO-BCD CODE CONVERTERS
('484 BCD-to-binary)
('485 binary-to-BCD)
typical performance

TYPE	DELAY TIME PER PKG LEVEL	TOTAL POWER
'S484	45 ns	525 mW
'S485	45 ns	525 mW

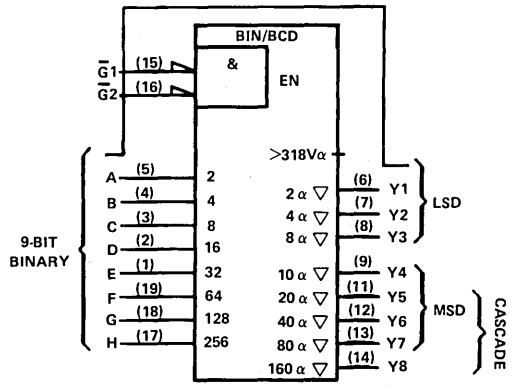
SN54S484 (J,FC)
SN54S485 (J,FC)

SN74S484 (J,N,FN)
SN74S485 (J,N,FN)

logic symbol 'S484†



logic symbol 'S485†



pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 E	11 Y5	1 E	15 Y5
2 D	12 Y6	2 D	16 Y6
3 C	13 Y7	3 C	17 nc
4 B	14 Y8	4 nc	18 nc
5 A	15 $\overline{G1}$	5 B	19 nc
6 Y1	16 $\overline{G2}$	6 A	20 Y7
7 Y2	17 H	7 nc	21 Y8
8 Y3	18 G	8 nc	22 $\overline{G1}$
9 Y4	19 F	9 Y1	23 $\overline{G2}$
10 GND	20 V_{CC}	10 Y2	24 H
		11 nc	25 G
		12 Y3	26 nc
		13 Y4	27 F
		14 GND	28 V_{CC}

See Page 2-71

490

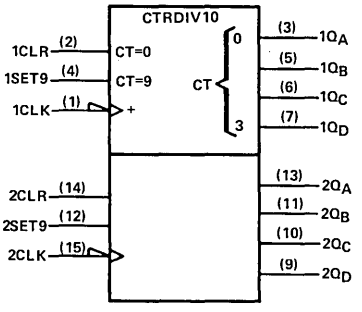
DUAL DECADE COUNTERS
typical performance

TYPE	COUNT FREQ	CLEAR	TOTAL POWER
'490	25 MHz	HIGH	225 mW
'LS490	35 MHz	HIGH	75 mW

SN54490 (J,FC)
SN54LS490 (J,FC)

SN74490 (J,N)
SN74LS490 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 1CLK	9 2QD	1 1CLK	11 nc
2 1CLR	10 2QC	2 nc	12 2QD
3 1QA	11 2QB	3 1CLR	13 2QC
4 1SET9	12 2SET9	4 1QA	14 2QB
5 1QB	13 2QA	5 1SET9	15 2SET9
6 1QC	14 2CLR	6 1QB	16 2QA
7 1QD	15 2CLK	7 1QC	17 2CLR
8 GND	16 V_{CC}	8 nc	18 nc
		9 1QD	19 2CLK
		10 GND	20 V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

540, 541

OCTAL BUFFERS AND LINE DRIVERS

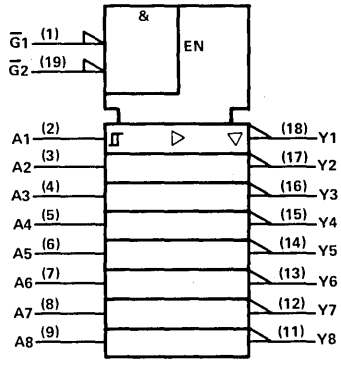
- Three-state output drives bus lines or buffer memory address registers
- 'LS540 for inverted data output
- 'LS541 for true data output

typical performance

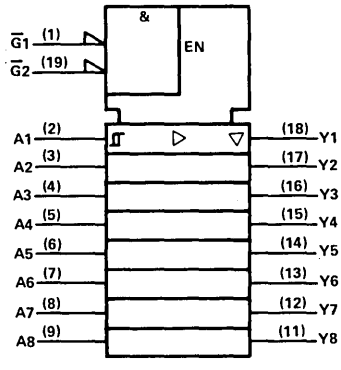
TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54LS540	9 ns	−12 mA	12 mA
SN74LS540	9.5 ns	−15 mA	24 mA
SN54LS541	9 ns	−12 mA	12 mA
SN74LS541	9.5 ns	−15 mA	24 mA

SN54LS540 (J,FC) SN74LS540 (J,N)
SN54LS541 (J,FC) SN74LS541 (J,N)

logic symbol, 'LS540†



logic symbol, 'LS541†



See *TTL Data Book*

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 $\overline{G}1$	11 Y8	1 $\overline{G}1$	11 Y8
2 A1	12 Y7	2 A1	12 Y7
3 A2	13 Y6	3 A2	13 Y6
4 A3	14 Y5	4 A3	14 Y5
5 A4	15 Y4	5 A4	15 Y4
6 A5	16 Y3	6 A5	16 Y3
7 A6	17 Y2	7 A6	17 Y2
8 A7	18 Y1	8 A7	18 Y1
9 A8	19 $\overline{G}2$	9 A8	19 $\overline{G}2$
10 GND	20 V_{CC}	10 GND	20 V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

573

OCTAL D-TYPE TRANSPARENT LATCHES

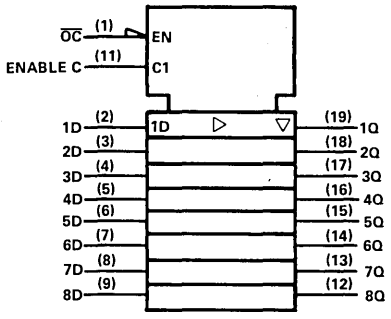
- Functionally equivalent to 'LS373 and 'S373
- Three-state buffer-type outputs drive bus lines directly
- Approximately half the power of 'LS373

typical performance

TYPE	OUTPUTS	DELAY	TOTAL POWER
'ALS573	Q	11 ns	67.5 mW

SN54ALS573 (J,FC) SN74ALS573 (N,FN)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 $\overline{OC}$	11 ENC	1 $\overline{OC}$	11 ENC
2 1D	12 8Q	2 1D	12 8Q
3 2D	13 7Q	3 2D	13 7Q
4 3D	14 6Q	4 3D	14 6Q
5 4D	15 5Q	5 4D	15 5Q
6 5D	16 4Q	6 5D	16 4Q
7 6D	17 3Q	7 6D	17 3Q
8 7D	18 2Q	8 7D	18 2Q
9 8D	19 1Q	9 8D	19 1Q
10 GND	20 V_{CC}	10 GND	20 V_{CC}

574

OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS

- Functionally equivalent to 'LS374 and 'S374
- Three-state buffer-type outputs drive bus lines directly
- Approximately half the power of 'LS374

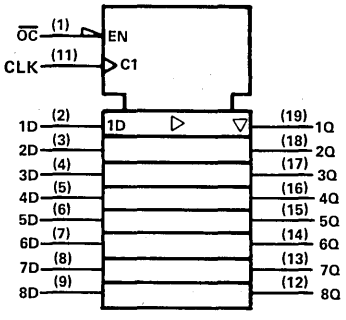
typical performance

TYPE	f_{max}	PWR/ F-F	DATA TIMES	
			SET-UP	HOLD
'ALS574	50 MHz	8.44 mW	10 ns†	4 ns†

† Rising edge of clock pulse

SN54ALS574 (J,FC) SN74ALS574 (N,FN)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 $\overline{OC}$	11 CLK	1 $\overline{OC}$	11 CLK
2 1D	12 8Q	2 1D	12 8Q
3 2D	13 7Q	3 2D	13 7Q
4 3D	14 6Q	4 3D	14 6Q
5 4D	15 5Q	5 4D	15 5Q
6 5D	16 4Q	6 5D	16 4Q
7 6D	17 3Q	7 6D	17 3Q
8 7D	18 2Q	8 7D	18 2Q
9 8D	19 1Q	9 8D	19 1Q
10 GND	20 V_{CC}	10 GND	20 V_{CC}

576

OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS

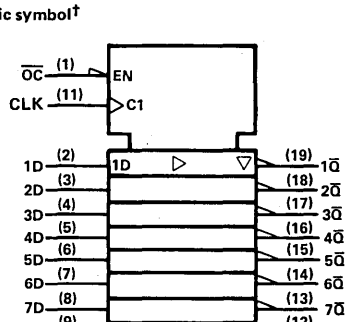
- Buffer-type outputs drive bus lines directly
- Inverted outputs

typical performance

TYPE	f_{max}	PWR/ F-F
'ALS576	50 MHz	8.4 mW

SN54ALS576 (J,FC) SN74ALS576 (N,FN)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 $\overline{OC}$	11 CLK	1 $\overline{OC}$	11 CLK
2 1D	12 8$\overline{Q}$	2 1D	12 8$\overline{Q}$
3 2D	13 7$\overline{Q}$	3 2D	13 7$\overline{Q}$
4 3D	14 6$\overline{Q}$	4 3D	14 6$\overline{Q}$
5 4D	15 5$\overline{Q}$	5 4D	15 5$\overline{Q}$
6 5D	16 4$\overline{Q}$	6 5D	16 4$\overline{Q}$
7 6D	17 3$\overline{Q}$	7 6D	17 3$\overline{Q}$
8 7D	18 2$\overline{Q}$	8 7D	18 2$\overline{Q}$
9 8D	19 1$\overline{Q}$	9 8D	19 1$\overline{Q}$
10 GND	20 V_{CC}	10 GND	20 V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

8

580

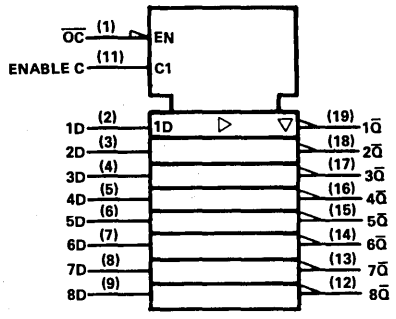
OCTAL D-TYPE TRANSPARENT LATCHES WITH INVERTED OUTPUTS

- Three-state buffer-type outputs drive bus lines directly

typical performance

TYPE	DELAY	TOTAL POWER
'ALS580	11 ns	67.5 mW

logic symbol†



pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 $\overline{OC}$	11 ENC	1 $\overline{OC}$	11 ENC
2 1D	12 $8\overline{Q}$	2 1D	12 $8\overline{Q}$
3 2D	13 $7\overline{Q}$	3 2D	13 $7\overline{Q}$
4 3D	14 $6\overline{Q}$	4 3D	14 $6\overline{Q}$
5 4D	15 $5\overline{Q}$	5 4D	15 $5\overline{Q}$
6 5D	16 $4\overline{Q}$	6 5D	16 $4\overline{Q}$
7 6D	17 $3\overline{Q}$	7 6D	17 $3\overline{Q}$
8 7D	18 $2\overline{Q}$	8 7D	18 $2\overline{Q}$
9 8D	19 $1\overline{Q}$	9 8D	19 $1\overline{Q}$
10 GND	20 V_{CC}	10 GND	20 V_{CC}

See *TTL Data Book*

SN54ALS580 (J,FC) SN74ALS580 (N,FN)

590, 591

8-BIT BINARY COUNTERS WITH OUTPUT REGISTERS

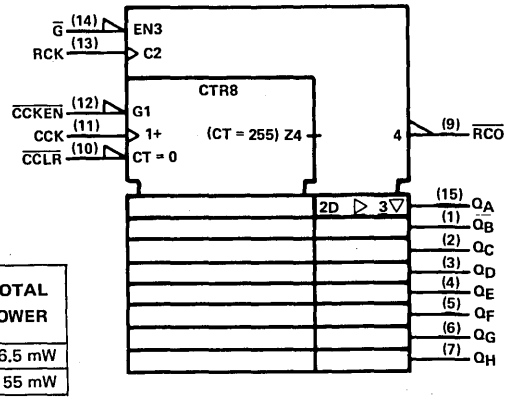
- 'LS590 has three-state register outputs
- 'LS591 has open-collector register outputs
- Counter has direct clear

typical performance

TYPE	MAX COUNT FREQ	PARALLEL LOAD	CLEAR	TOTAL POWER
'LS590	20 MHz	SYNC	SYNC-L	166.5 mW
'LS591	20 MHz	SYNC	SYNC-L	155 mW

SN54LS590 (J) SN74LS590 (J,N)
SN54LS591 (J) SN74LS591 (J,N)

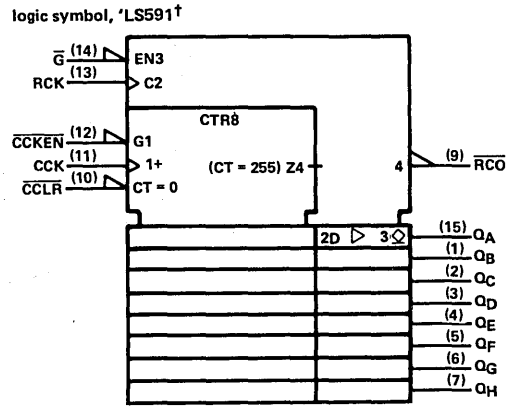
logic symbol, 'LS590†



pin assignments

J, N PACKAGES	
1 QB	9 $\overline{RCO}$
2 QC	10 $\overline{CCLR}$
3 QD	11 CCK
4 QE	12 $\overline{CCKEN}$
5 QF	13 RCK
6 QG	14 $\overline{G}$
7 QH	15 QA
8 GND	16 V_{CC}

logic symbol, 'LS591†



See *TTL Data Book*

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

592

8-BIT BINARY COUNTERS WITH INPUT REGISTERS

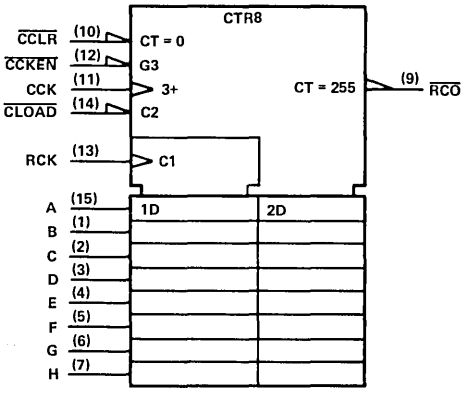
- Has parallel register inputs
- Counter has direct overriding load and clear
- Guaranteed counter frequency . . . dc to 20 MHz

typical performance

MAX COUNT FREQ	PARALLEL LOAD	CLEAR	TOTAL POWER
20 MHz	SYNC	SYNC-L	130 mW

SN54LS592 (J) SN74LS592 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES	
1 B	9 RCO
2 C	10 CCLR
3 D	11 CCK
4 E	12 CCKEN
5 F	13 RCK
6 G	14 CLOAD
7 H	15 A
8 GND	16 V_{CC}

593

8-BIT BINARY COUNTERS WITH INPUT REGISTERS

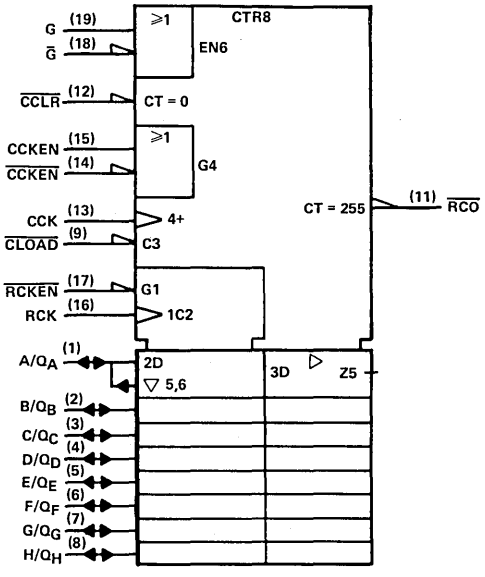
- Has parallel three-state I/O: register inputs/counter outputs
- Counter has direct overriding load and clear
- Guaranteed counter frequency . . . dc to 20 MHz

typical performance

MAX COUNT FREQ	PARALLEL LOAD	CLEAR	TOTAL POWER
20 MHz	SYNC	SYNC-L	177 mW

SN54LS593 (J) SN74LS593 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES	
1 A/QA	11 RCO
2 B/QB	12 CCLR
3 C/QC	13 CCK
4 D/QD	14 CCKEN
5 E/QE	15 CCKEN
6 F/QF	16 RCK
7 G/QG	17 RCKEN
8 H/QH	18 G̅
9 CLOAD	19 G
10 GND	20 V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

8

595, 596

8-BIT SHIFT REGISTERS WITH OUTPUT LATCHES

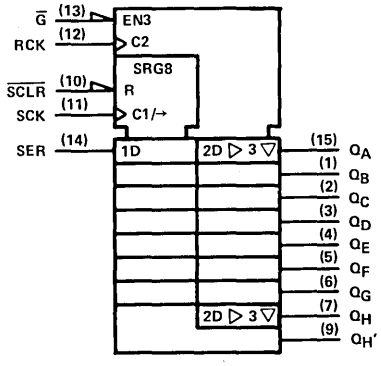
- Serial-in, parallel-out shift registers with storage
- 'LS595 has three-state parallel outputs
- 'LS596 has open-collector parallel outputs
- Guaranteed shift frequency . . . dc to 20 MHz

typical performance

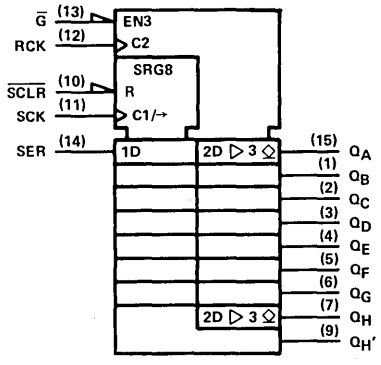
TYPE	SERIAL DATA INPUT	ASYNC CLEAR	TOTAL POWER
'LS595	D	LOW	167 mW
'LS596	D	LOW	160 mW

SN54LS595 (J) SN74LS595 (J,N)
SN54LS596 (J) SN74LS596 (J,N)

logic symbol, 'LS595†



logic symbol, 'LS596†



pin assignments

J, N PACKAGES	
1 QB	9 QH'
2 QC	10 SCLR
3 QD	11 SCK
4 QE	12 RCK
5 QF	13 G
6 QG	14 SER
7 QH	15 QA
8 GND	16 V_{CC}

See *TTL Data Book*

597

8-BIT SHIFT REGISTERS WITH INPUT LATCHES

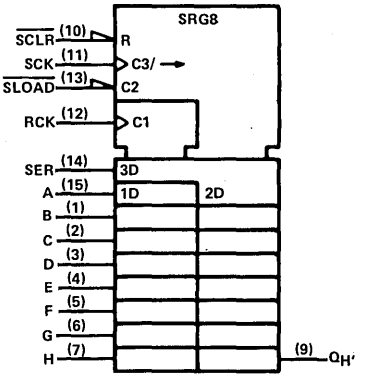
- Has parallel storage register inputs
- Shift register has direct overriding load and clear
- Guaranteed shift frequency . . . dc to 20 MHz

typical performance

TYPE	SERIAL DATA INPUT	ASYNC CLEAR	TOTAL POWER
'LS597	D	LOW	130 mW

SN54LS597 (J) SN74LS597 (J,N)

logic symbol†



pin assignments

J, N PACKAGES	
1 B	9 QH'
2 C	10 SCLR
3 D	11 SCK
4 E	12 RCK
5 F	13 SLOAD
6 G	14 SER
7 H	15 A
8 GND	16 V_{CC}

See *TTL Data Book*

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

598

8-BIT SHIFT REGISTERS WITH INPUT LATCHES

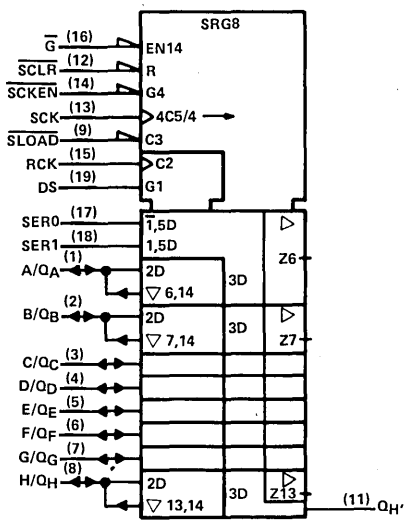
- Has parallel three-state I/O storage register inputs, shift register outputs
- Shift register has direct overriding load and clear
- Guaranteed shift frequency . . . dc to 20 MHz

typical performance

TYPE	SERIAL DATA INPUT	ASYNC CLEAR	TOTAL POWER
'LS598	D	LOW	177 mW

SN54LS598 (J) SN74LS598 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES			
1	A/QA	11	QH'
2	B/QB	12	$\overline{SCLR}$
3	C/QC	13	SCK
4	D/QD	14	$\overline{SCKEN}$
5	E/QE	15	RCK
6	F/QF	16	$\overline{G}$
7	G/QG	17	SER0
8	H/QH	18	SER1
9	$\overline{SLOAD}$	19	DS
10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

600

MEMORY REFRESH CONTROLLERS

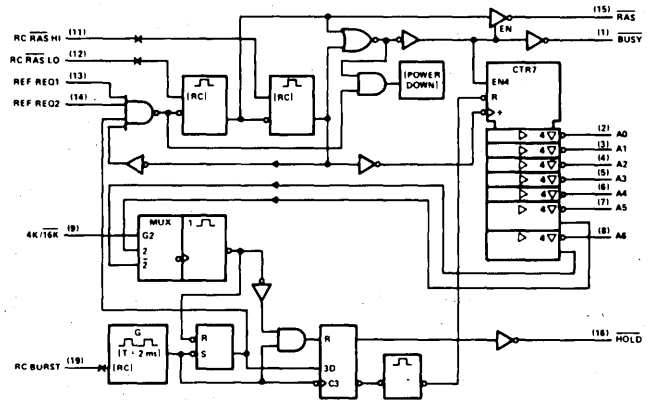
- Controls refresh cycle of 4K or 16K dynamic RAM's
- Three-state outputs drive bus lines directly
- Time to initiate refresh request is typically 30 ns
- Refresh modes: transparent, burst

SN54LS600 (J,FC) SN74LS600 (J,N)

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 $\overline{BUSY}$	11 RC $\overline{RAS}$ HI	1 $\overline{BUSY}$	11 RC $\overline{RAS}$ HI
2 A0	12 RC $\overline{RAS}$ LO	2 A0	12 RC $\overline{RAS}$ LO
3 A1	13 REF REQ1	3 A1	13 REF REQ2
4 A2	14 REF REQ2	4 A2	14 REF REQ1
5 A3	15 $\overline{RAS}$	5 A3	15 $\overline{RAS}$
6 A4	16 $\overline{HOLD}$	6 A4	16 $\overline{HOLD}$
7 A5	17 nc	7 A5	17 nc
8 A6	18 nc	8 A6	18 nc
9 4K/$\overline{16K}$	19 RC BURST	9 4K/$\overline{16K}$	19 RC BURST
10 GND	20 V_{CC}	10 GND	20 V_{CC}

functional block diagram†



See *TTL Data Book*

601

MEMORY REFRESH CONTROLLERS

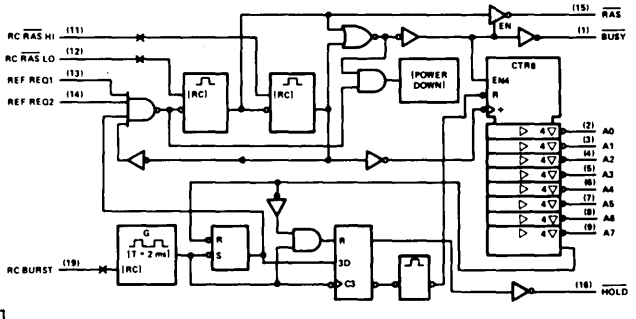
- Controls refresh cycle of 64K dynamic RAM's
- Three-state outputs drive bus lines directly
- Time to initiate refresh request is typically 30 ns
- Refresh modes: transparent, burst

SN54LS601 (J,FC) SN74LS601 (J,N)

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 $\overline{BUSY}$	11 RC $\overline{RAS}$ HI	1 $\overline{BUSY}$	11 RC $\overline{RAS}$ HI
2 A0	12 RC $\overline{RAS}$ LO	2 A0	12 RC $\overline{RAS}$ LO
3 A1	13 REF REQ1	3 A1	13 REF REQ2
4 A2	14 REF REQ2	4 A2	14 REF REQ1
5 A3	15 $\overline{RAS}$	5 A3	15 $\overline{RAS}$
6 A4	16 $\overline{HOLD}$	6 A4	16 $\overline{HOLD}$
7 A5	17 nc	7 A5	17 nc
8 A6	18 nc	8 A6	18 nc
9 A7	19 RC BURST	9 A7	19 RC BURST
10 GND	20 V_{CC}	10 GND	20 V_{CC}

functional block diagram†



See *TTL Data Book*

†Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

602

MEMORY REFRESH CONTROLLERS

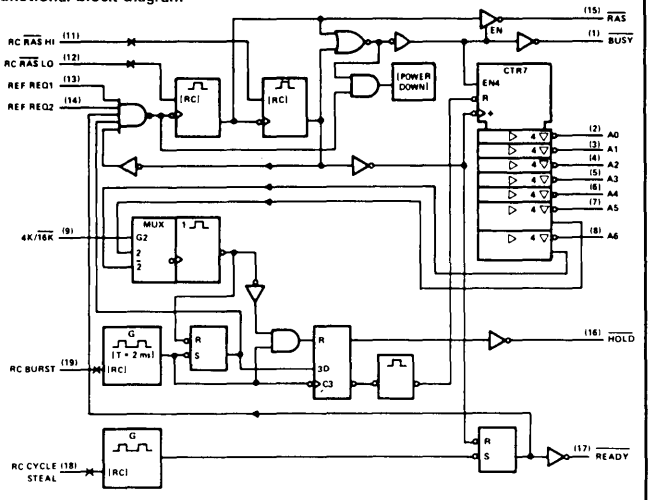
- Controls refresh cycle of 4K or 16K dynamic RAM's
- Three-state outputs drive bus lines directly
- Time to initiate refresh request is typically 30 ns
- Refresh modes: cycle steal, burst

SN54LS602 (J,FC) SN74LS602 (J,N)

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	$\overline{BUSY}$	11	RC $\overline{RAS}$ HI	1	$\overline{BUSY}$	11	RC $\overline{RAS}$ HI
2	A0	12	RC $\overline{RAS}$ LO	2	A0	12	RC $\overline{RAS}$ LO
3	A1	13	REF REQ1	3	A1	13	REF REQ2
4	A2	14	REF REQ2	4	A2	14	REF REQ1
5	A3	15	$\overline{RAS}$	5	A3	15	$\overline{RAS}$
6	A4	16	$\overline{HOLD}$	6	A4	16	$\overline{HOLD}$
7	A5	17	$\overline{READY}$	7	A5	17	$\overline{READY}$
8	A6	18	RC CYCLE STEAL	8	A6	18	RC CYCLE STEAL
9	4K/$\overline{16K}$	19	RC BURST	9	4K/$\overline{16K}$	19	RC BURST
10	GND	20	V_{CC}	10	GND	20	V_{CC}

functional block diagram†



See *TTL Data Book*

603

MEMORY REFRESH CONTROLLERS

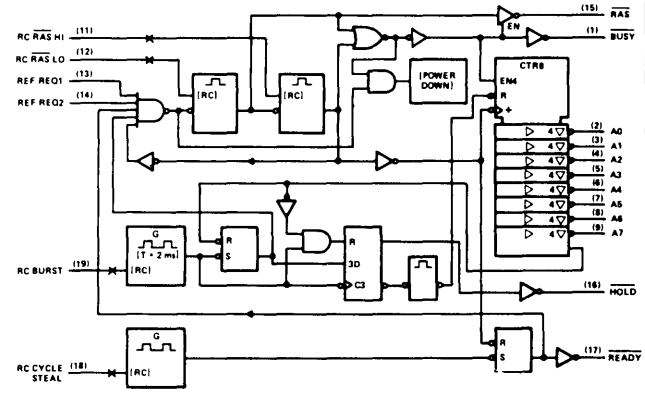
- Controls refresh cycle of 64K dynamic RAM's
- Three-state outputs drive bus lines directly
- Time to initiate refresh request is typically 30 ns
- Refresh modes: cycle steal, burst

SN54LS603 (J,FC) SN74LS603 (J,N)

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	$\overline{BUSY}$	11	RC $\overline{RAS}$ HI	1	$\overline{BUSY}$	11	RC $\overline{RAS}$ HI
2	A0	12	RC $\overline{RAS}$ LO	2	A0	12	RC $\overline{RAS}$ LO
3	A1	13	REF REQ1	3	A1	13	REF REQ2
4	A2	14	REF REQ2	4	A2	14	REF REQ1
5	A3	15	$\overline{RAS}$	5	A3	15	$\overline{RAS}$
6	A4	16	$\overline{HOLD}$	6	A4	16	$\overline{HOLD}$
7	A5	17	$\overline{READY}$	7	A5	17	$\overline{READY}$
8	A6	18	RC CYCLE STEAL	8	A6	18	RC CYCLE STEAL
9	A7	19	RC BURST	9	A7	19	RC BURST
10	GND	20	V_{CC}	10	GND	20	V_{CC}

functional block diagram†



See *TTL Data Book*

†Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

8

604, 605
606, 607

OCTAL 2-INPUT MULTIPLEXED LATCHES

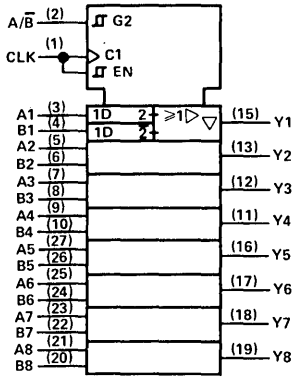
- 16 D-type registers — one for each data input
- 'LS604 and 'LS606 feature three-state outputs
- Multiplexers select stored data from either A or B bus
- Application-oriented:
  - max speed - ('LS604, 'LS605)
  - glitch-free operation - ('LS606, 'LS607)

typical performance

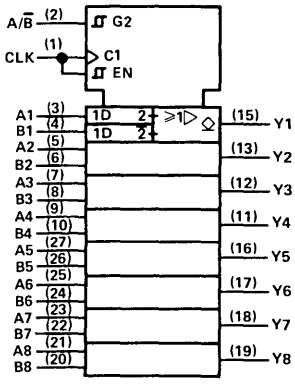
TYPE	DELAY	POWER
'LS604	23.5 ns	275 mW
'LS605	26 ns	200 mW
'LS606	31 ns	275 mW
'LS607	31 ns	200 mW

SN54LS604 (J,FC) SN74LS604 (JD,N)
SN54LS605 (J,FC) SN74LS605 (JD,N)
SN54LS606 (J,FC) SN74LS606 (JD,N)
SN54LS607 (J,FC) SN74LS607 (JD,N)

logic symbol, 'LS604, 'LS606†



logic symbol, 'LS605, 'LS607†



See *TTL Data Book*

pin assignments

J, JD, N PACKAGES				FC, FN PACKAGES			
1	CLK	15	Y1	1	CLK	15	Y1
2	$A/\overline{B}$	16	Y5	2	$A/\overline{B}$	16	Y5
3	A1	17	Y6	3	A1	17	Y6
4	B1	18	Y7	4	B1	18	Y7
5	A2	19	Y8	5	A2	19	Y8
6	B2	20	B8	6	B2	20	B8
7	A3	21	A8	7	A3	21	A8
8	B3	22	B7	8	B3	22	B7
9	A4	23	A7	9	A4	23	A7
10	B4	24	B6	10	B4	24	B6
11	Y4	25	A6	11	Y4	25	A6
12	Y3	26	B5	12	Y3	26	B5
13	Y2	27	A5	13	Y2	27	A5
14	GND	28	V_{CC}	14	GND	28	V_{CC}

† Pin numbers shown on logic symbols are for J, JD, and N packages only.

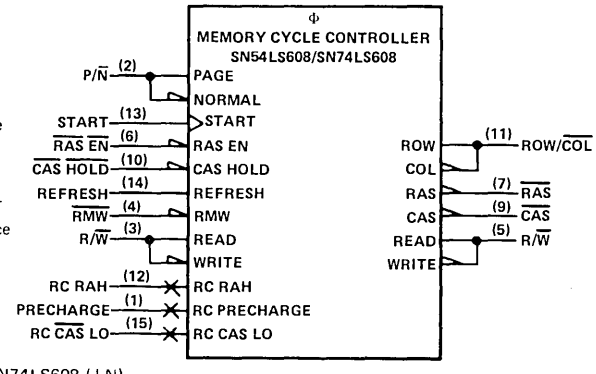
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

608

MEMORY CYCLE CONTROLLERS

- Read cycle
- Write cycle
- Read, modify, write cycle
- RAS only refresh cycle
- Page or normal modes
- Stand-alone controller for CPU-to-memory interface

logic symbol†



pin assignments

J, N PACKAGES			
1	PRECHARGE	9	CAS
2	P/N	10	CAS HOLD
3	R/W	11	ROW/COL
4	RMW	12	RC RAH
5	R/W	13	START
6	RAS EN	14	REFRESH
7	RAS	15	RC CAS LO
8	GND	16	V_{CC}

SN54LS608 (J) SN74LS608 (J,N)

See *TTL Data Book*

† Pin numbers shown on logic symbols are for J, JD, and N packages only.

8

610, 611 612, 613

MEMORY MAPPERS

typical performance

TYPE	MAP OUTPUTS LATCHED	MAP OUTPUT TYPE
'LS610	Yes	3-State
'LS611	Yes	O-C
'LS612	No	3-State
'LS613	No	O-C

- Designed for paged memory mapping
- Expands four address lines to 12 address lines

SN54LS610 (J,FC) SN74LS610 (JD,N)
SN54LS611 (J,FC) SN74LS611 (JD,N)
SN54LS612 (J,FC) SN74LS612 (JD,N)
SN54LS613 (J,FC) SN74LS613 (JD,N)

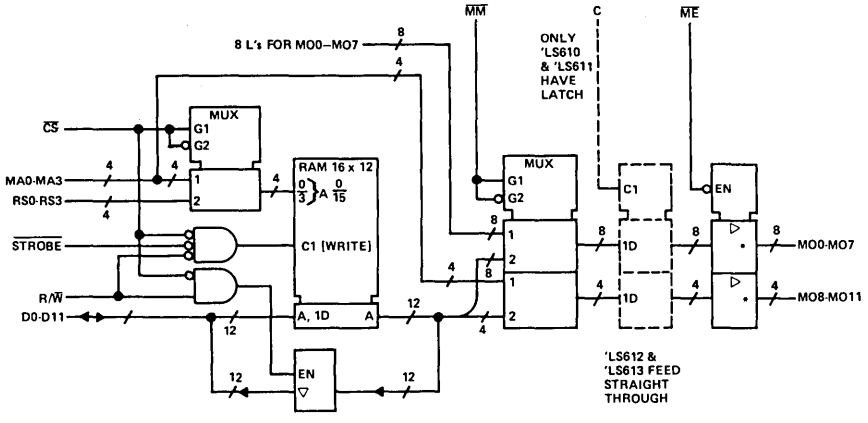
pin assignments

J, JD, N PACKAGES		FC, FN PACKAGES	
1 RS2	21 $\overline{ME}$	1 RS2	23 $\overline{ME}$
2 MA3	22 MO6	2 MA3	24 MO6
3 RS3	23 MO7	3 RS3	25 MO7
4 $\overline{CS}$	24 MO8	4 $\overline{CS}$	26 MO8
5 $\overline{STROBE}$	25 MO9	5 $\overline{STROBE}$	27 MO9
6 R/$\overline{W}$	26 MO10	6 nc	28 nc
7 D0	27 MO11	7 R/$\overline{W}$	29 MO10
8 D1	28 ★	8 D0	30 MO11
9 D2	29 D6	9 D1	31 ★
10 D3	30 D7	10 D2	32 D6
11 D4	31 D8	11 D3	33 D7
12 D5	32 D9	12 D4	34 D8
13 $\overline{MM}$	33 D10	13 D5	35 D9
14 MO0	34 D11	14 $\overline{MM}$	36 D10
15 MO1	35 MA0	15 MO0	37 D11
16 MO2	36 RS0	16 MO1	38 MA0
17 MO3	37 MA1	17 nc	39 nc
18 MO4	38 RS1	18 MO2	40 RS0
19 MO5	39 MA2	19 MO3	41 MA1
20 GND	40 V_{CC}	20 MO4	42 RS1
		21 MO5	43 MA2
		22 GND	44 V_{CC}

★ C on 'LS610 and 'LS611
nc on 'LS612 and 'LS613

See *TTL Data Book*

functional block diagram (positive logic)



*'LS610 and 'LS612 have 3-state (▽) map outputs.
'LS611 and 'LS613 have open-collector (◇) map outputs.

nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

620, 621
622, 623

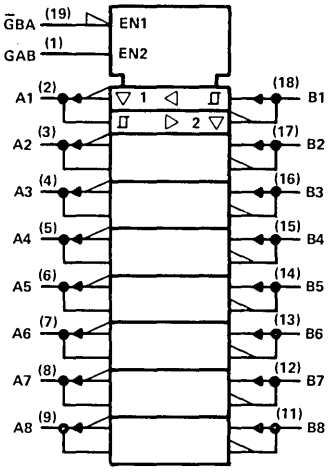
OCTAL BUS TRANSCEIVERS

- Bidirectional bus transceivers
- Local bus latch capability

typical performance

TYPE	OUTPUT	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54LS620	3-State	−12 mA	12 mA
SN74LS620	3-State	−15 mA	24 mA
SN54LS621	O-C	N/A	12 mA
SN74LS621	O-C	N/A	24 mA
SN54LS622	O-C	N/A	12 mA
SN74LS622	O-C	N/A	24 mA
SN54LS623	3-State	−12 mA	12 mA
SN74LS623	3-State	−15 mA	24 mA

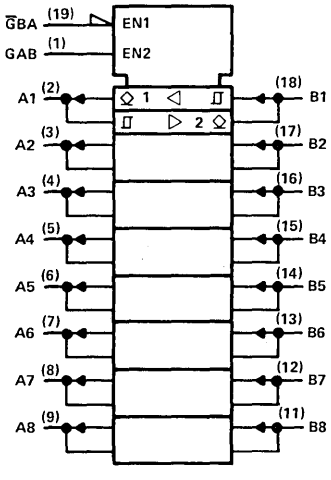
logic symbol, 'LS620†



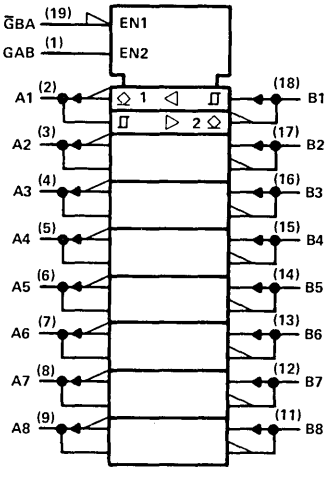
pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 GAB	11 B8	1 GAB	11 B8
2 A1	12 B7	2 A1	12 B7
3 A2	13 B6	3 A2	13 B6
4 A3	14 B5	4 A3	14 B5
5 A4	15 B4	5 A4	15 B4
6 A5	16 B3	6 A5	16 B3
7 A6	17 B2	7 A6	17 B2
8 A7	18 B1	8 A7	18 B1
9 A8	19 GBA	9 A8	19 GBA
10 GND	20 V_{CC}	10 GND	20 V_{CC}

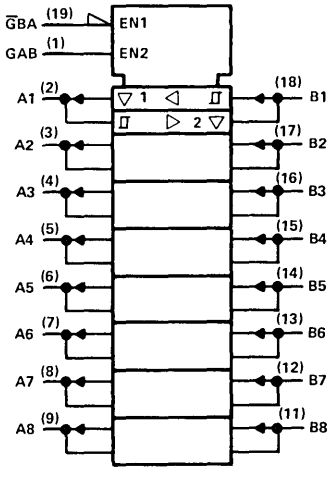
logic symbol, 'LS621†



logic symbol, 'LS622†



logic symbol, 'LS623†



SN54LS620 (J,FC) SN74LS620 (J,N)
SN54LS621 (J,FC) SN74LS621 (J,N)
SN54LS622 (J,FC) SN74LS622 (J,N)
SN54LS623 (J,FC) SN74LS623 (J,N)

See *TTL Data Book*

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

624

VOLTAGE-CONTROLLED OSCILLATORS

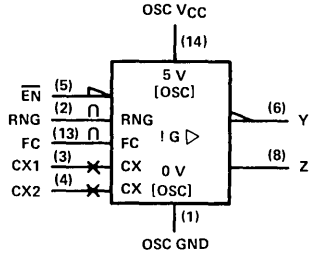
typical performance

TYPE	REPLACES
'LS624	'LS324

- Separate supply voltage pins for isolation of input/output signals
- Maximum output frequency = 20 MHz
- Improved version of original VCO family

SN54LS624 (J,FC) SN74LS624 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	OSC GND	8	Z	1	OSC GND	11	Z
2	RNG	9	V_{CC}	2	RNG	12	V_{CC}
3	CX1	10	nc	3	nc	13	nc
4	CX2	11	nc	4	CX1	14	nc
5	$\overline{EN}$	12	nc	5	CX2	15	nc
6	Y	13	FREQ CONTROL	6	nc	16	nc
7	GND	14	OSC V_{CC}	7	$\overline{EN}$	17	nc
				8	nc	18	nc
				9	Y	19	FREQ CONTROL
				10	GND	20	OSC V_{CC}

625

VOLTAGE-CONTROLLED OSCILLATORS

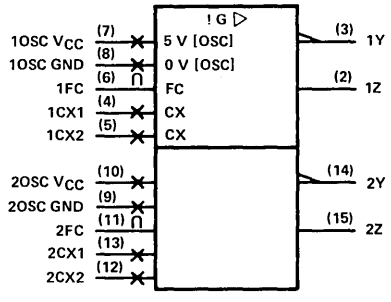
typical performance

TYPE	REPLACES
'LS625	'LS325

- Separate supply voltage pins for input/output isolation
- Maximum output frequency = 20 MHz
- Improved version of original family

SN54LS625 (J,FC) SN74LS625 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	GND	9	2OSC GND	1	GND	11	2OSC GND
2	1Z	10	2OSC V_{CC}	2	1Z	12	2OSC V_{CC}
3	1Y	11	2FC	3	nc	13	nc
4	1CX1	12	2CX2	4	1Y	14	2FC
5	1CX2	13	2CX1	5	1CX1	15	2CX2
6	1FC	14	2Y	6	1CX2	16	2CX1
7	1OSC V_{CC}	15	2Z	7	1FC	17	2Y
8	1OSC GND	16	V_{CC}	8	nc	18	nc
				9	1OSC V_{CC}	19	2Z
				10	1OSC GND	20	V_{CC}

626

VOLTAGE-CONTROLLED OSCILLATORS

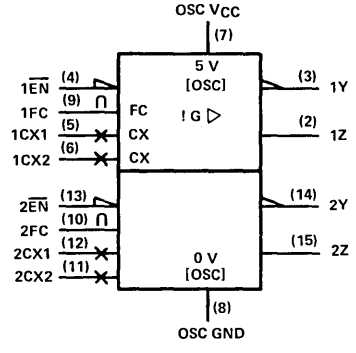
typical performance

TYPE	REPLACES
'LS626	'LS326

- Separate supply voltage pins for input/output isolation
- Maximum output frequency = 20 MHz
- Improved version of original family

SN54LS626 (J,FC) SN74LS626 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	GND	9	1FC	1	GND	11	1FC
2	1Z	10	2FC	2	1Z	12	2FC
3	1Y	11	2CX2	3	nc	13	nc
4	1$\overline{EN}$	12	2CX1	4	1Y	14	2CX2
5	1CX1	13	2$\overline{EN}$	5	1$\overline{EN}$	15	2CX1
6	1CX2	14	2Y	6	1CX1	16	2$\overline{EN}$
7	OSC V_{CC}	15	2Z	7	1CX2	17	2Y
8	OSC GND	16	V_{CC}	8	nc	18	nc
				9	OSC V_{CC}	19	2Z
				10	OSC GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

627

VOLTAGE-CONTROLLED OSCILLATORS

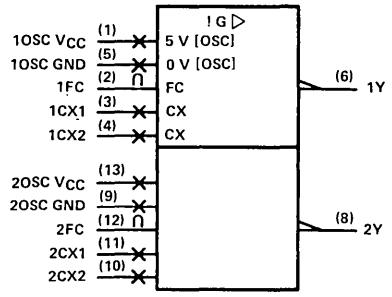
TYPE	REPLACES
'LS627	'LS327

- Separate supply voltage pins for input/output isolation
- Maximum output frequency = 20 MHz
- Improved version of original family

SN54LS627 (J,FC) SN74LS627 (J,N)

typical performance

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	1OSC VCC	8	2Y	1	1OSC VCC	11	2Y
2	1FC	9	2OSC GND	2	1FC	12	nc
3	1CX1	10	2CX2	3	nc	13	nc
4	1CX2	11	2CX1	4	nc	14	nc
5	1OSC GND	12	2FC	5	1CX1	15	2OSC GND
6	1Y	13	2OSC VCC	6	1CX2	16	2CX2
7	GND	14	VCC	7	1OSC GND	17	2CX1
				8	nc	18	2FC
				9	1Y	19	2OSC VCC
				10	GND	20	VCC

628

VOLTAGE-CONTROLLED OSCILLATORS

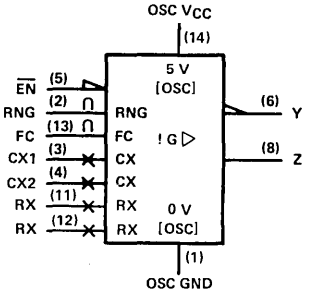
TYPE	REPLACES
'LS628	'LS324

- Separate supply voltage pins for input/output oscillators
- Maximum output frequency = 20 MHz
- Improved version of original family

SN54LS628 (J,FC) SN74LS628 (J,N)

typical performance

logic symbol†



pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	OSC GND	8	Z	1	OSC GND	11	Z
2	RNG	9	VCC	2	RNG	12	VCC
3	CX1	10	nc	3	nc	13	nc
4	CX2	11	RX	4	CX1	14	nc
5	EN	12	RX	5	CX2	15	nc
6	Y	13	FC	6	nc	16	RX
7	GND	14	OSC VCC	7	EN	17	RX
				8	nc	18	nc
				9	Y	19	FC
				10	GND	20	OSC VCC

629

VOLTAGE-CONTROLLED OSCILLATORS

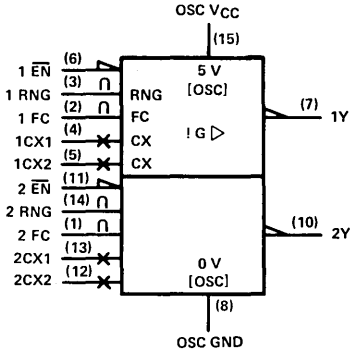
TYPE	REPLACES
'LS629	'LS124

- Separate power supply pins for input/output isolation
- Maximum output frequency = 20 MHz
- Improved version of original family

SN54LS629 (J,FC) SN74LS629 (J,N)

typical performance

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	2FC	9	GND	1	2FC	11	GND
2	1FC	10	2Y	2	1FC	12	2Y
3	1RNG	11	2EN	3	nc	13	nc
4	1CX1	12	2CX1	4	1RNG	14	nc
5	1CX2	13	2CX2	5	1CX1	15	2EN
6	1EN	14	2RNG	6	1CX2	16	2CX1
7	1Y	15	OSC VCC	7	1EN	17	2CX2
8	OSC GND	16	VCC	8	nc	18	2RNG
				9	1Y	19	OSC VCC
				10	OSC GND	20	VCC

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

630, 631

16-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

- Fast processing times:
  - Write cycle: generates check word in 45 ns typical
  - Read cycle: flags errors in 27 ns typical
- Detects and corrects single bit error
- Detects and flags dual-bit errors

typical performance

TYPE	OUTPUT	DELAY	POWER
'LS630	3-State	27 ns	715 mW
'LS631	O-C	28 ns	565 mW

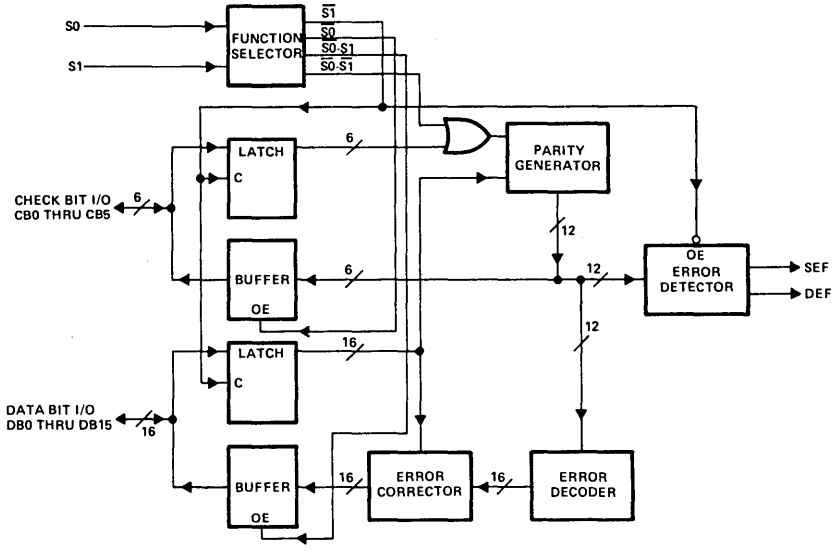
SN54LS630 (J,FC) SN74LS630 (JD,N)
SN54LS631 (J,FC) SN74LS631 (JD,N)

pin assignments

J, JD, N PACKAGES		FC, FN PACKAGES	
1 DEF	15 DB12	1 DEF	15 DB12
2 DB0	16 DB13	2 DB0	16 DB13
3 DB1	17 DB14	3 DB1	17 DB14
4 DB2	18 DB15	4 DB2	18 DB15
5 DB3	19 CB5	5 DB3	19 CB5
6 DB4	20 CB4	6 DB4	20 CB4
7 DB5	21 CB3	7 DB5	21 CB3
8 DB6	22 CB2	8 DB6	22 CB2
9 DB7	23 CB1	9 DB7	23 CB1
10 DB8	24 CB0	10 DB8	24 CB0
11 DB9	25 S0	11 DB9	25 S0
12 DB10	26 S1	12 DB10	26 S1
13 DB11	27 SEF	13 DB11	27 SEF
14 GND	28 V_{CC}	14 GND	28 V_{CC}

See *TTL Data Book*

functional block diagram



nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

638, 639

OCTAL BUS TRANSCEIVERS

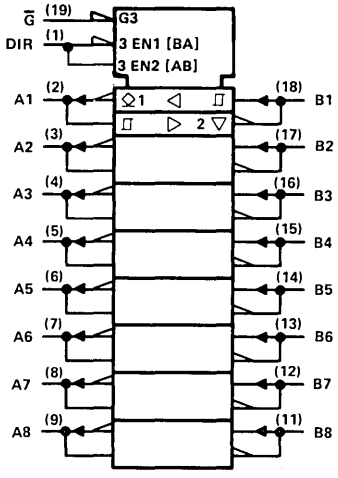
- Bidirectional bus transceivers
- "A" bus outputs are open-collector; "B" bus outputs are three-state
- 'LS638 — inverting logic
- 'LS639 — true logic

typical performance

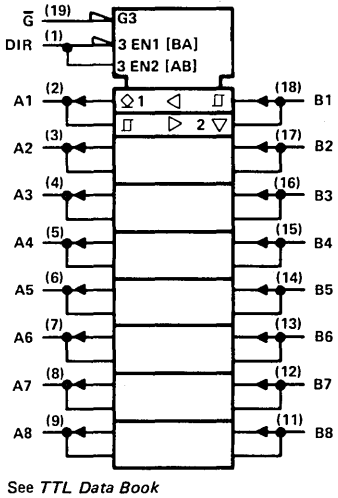
TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54LS638	11 ns	−12 mA	12 mA
SN74LS638	11 ns	−15 mA	24 mA
SN54LS639	13.5 ns	−12 mA	12 mA
SN74LS639	13.5 ns	−15 mA	24 mA

SN54LS638 (J) SN74LS638 (J,N)
SN54LS639 (J) SN74LS639 (J,N)

logic symbol, 'LS638†



logic symbol, 'LS639†



See *TTL Data Book*

pin assignments

J, N PACKAGES			
1	DIR	11	B8
2	A1	12	B7
3	A2	13	B6
4	A3	14	B5
5	A4	15	B4
6	A5	16	B3
7	A6	17	B2
8	A7	18	B1
9	A8	19	$\overline{G}$
10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

640, 641, 642
643, 644, 645

OCTAL BUS TRANSCEIVERS

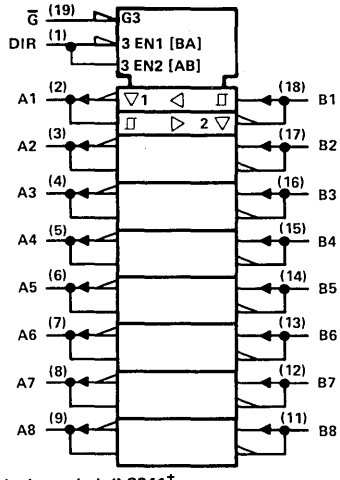
TYPE	OUTPUT	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54LS640	3-State	7 ns	–12 mA	12 mA
SN74LS640	3-State	7 ns	–15 mA	24 mA
SN74LS640-1	3-State	7 ns	–15 mA	48 mA
SN54LS641	O-C	16.5 ns	N/A	12 mA
SN74LS641	O-C	16.5 ns	N/A	24 mA
SN74LS641-1	O-C	16.5 ns	N/A	48 mA
SN54LS642	O-C	16.5 ns	N/A	12 mA
SN74LS642	O-C	16.5 ns	N/A	24 mA
SN74LS642-1	O-C	16.5 ns	N/A	48 mA
SN54LS643	3-State	8.5 ns	–12 mA	12 mA
SN74LS643	3-State	8.5 ns	–15 mA	24 mA
SN74LS643-1	3-State	8.5 ns	–15 mA	48 mA
SN54LS644	O-C	16.5 ns	N/A	12 mA
SN74LS644	O-C	16.5 ns	N/A	24 mA
SN74LS644-1	O-C	16.5 ns	N/A	48 mA
SN54LS645	3-State	9.5 ns	–12 mA	12 mA
SN74LS645	3-State	9.5 ns	–15 mA	24 mA
SN74LS645-1	3-State	9.5 ns	–15 mA	48 mA

SN54LS640 (J,FC) SN74LS640 (J,N)
SN54LS641 (J,FC) SN74LS641 (J,N)
SN54LS642 (J,FC) SN74LS642 (J,N)
SN54LS643 (J,FC) SN74LS643 (J,N)
SN54LS644 (J,FC) SN74LS644 (J,N)
SN54LS645 (J,FC) SN74LS645 (J,N)

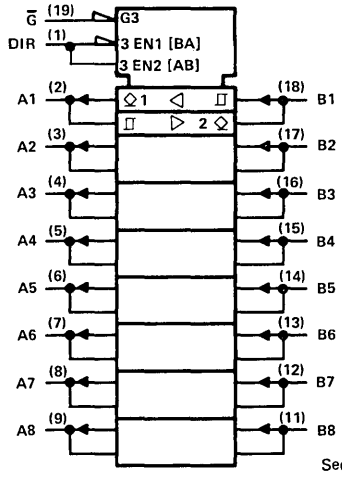
pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 DIR	11 B8	1 DIR	11 B8
2 A1	12 B7	2 A1	12 B7
3 A2	13 B6	3 A2	13 B6
4 A3	14 B5	4 A3	14 B5
5 A4	15 B4	5 A4	15 B4
6 A5	16 B3	6 A5	16 B3
7 A6	17 B2	7 A6	17 B2
8 A7	18 B1	8 A7	18 B1
9 A8	19 $\overline{G}$	9 A8	19 $\overline{G}$
10 GND	20 V_{CC}	10 GND	20 V_{CC}

logic symbol, 'LS640†



logic symbol, 'LS641†



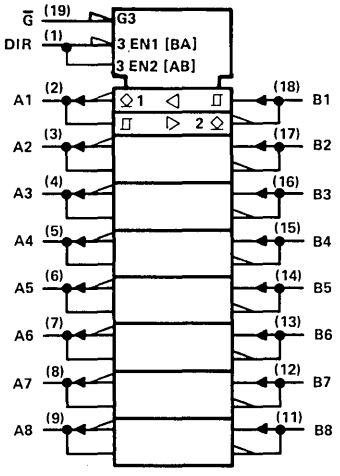
See *TTL Data Book*

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

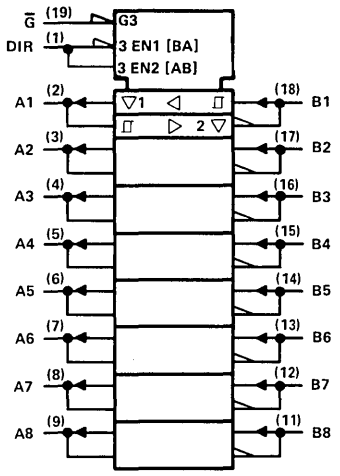
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

640, 641, 642
643, 644 645 continued

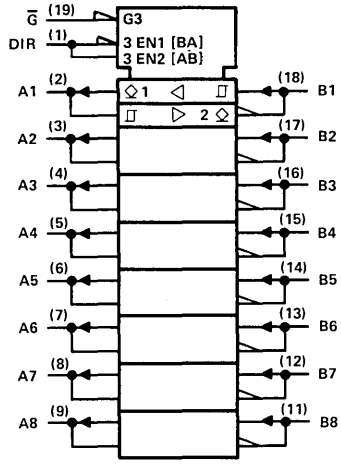
logic symbol, 'LS642†



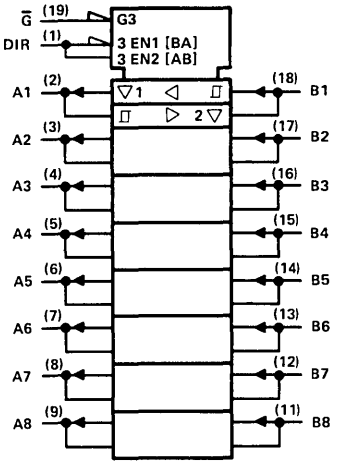
logic symbol, 'LS643†



logic symbol, 'LS644†



logic symbol, 'LS645†



See *TTL Data Book*

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

646, 647
648, 649

OCTAL BUS TRANSCEIVERS AND REGISTERS

- Bidirectional
- Independent registers for A and B busses

typical performance

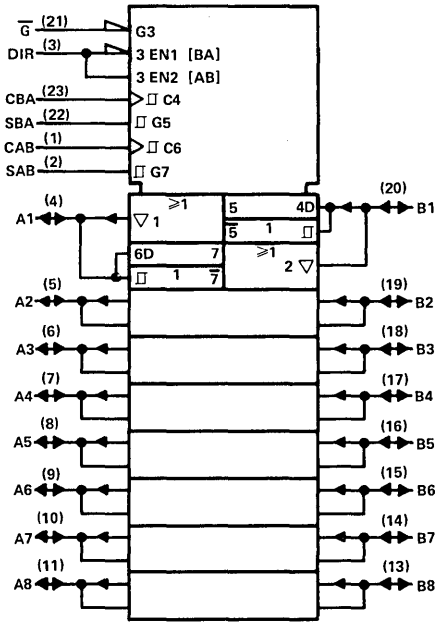
TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT	OUTPUT	
				TYPE	INV
SN54LS646	19 ns	−12 mA	12 mA	3-State	No
SN74LS646	19 ns	−15 mA	24 mA	3-State	No
SN74LS647	25 ns	–	12 mA	O-C	No
SN74LS647	25 ns	–	24 mA	O-C	No
SN54LS648	20.5 ns	−12 mA	12 mA	3-State	Yes
SN74LS648	20.5 ns	−15 mA	24 mA	3-State	Yes
SN54LS649	25 ns	–	12 mA	O-C	Yes
SN74LS649	25 ns	–	24 mA	O-C	Yes

pin assignments

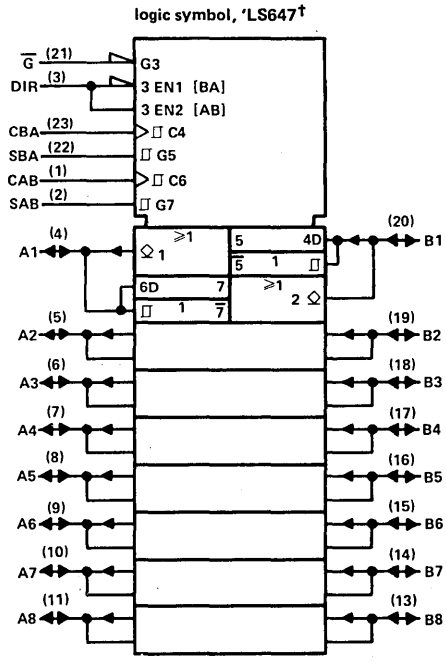
J, JT, NT PACKAGES				FC, FN PACKAGES			
1	CAB	13	B8	1	CAB	15	B8
2	SAB	14	B7	2	SAB	16	nc
3	DIR	15	B6	3	DIR	17	B7
4	A1	16	B5	4	nc	18	B6
5	A2	17	B4	5	nc	19	nc
6	A3	18	B3	6	A1	20	B5
7	A4	19	B2	7	A2	21	B4
8	A5	20	B1	8	A3	22	B3
9	A6	21	$\overline{G}$	9	A4	23	B2
10	A7	22	SBA	10	A5	24	B1
11	A8	23	CBA	11	A6	25	$\overline{G}$
12	GND	24	V_{CC}	12	A7	26	SBA
				13	A8	27	CBA
				14	GND	28	V_{CC}

SN54LS646 (J,FC) SN74LS646 (JT,NT)
SN54LS647 (J,FC) SN74LS647 (JT,NT)
SN54LS648 (J,FC) SN74LS648 (JT,NT)
SN54LS649 (J,FC) SN74LS649 (JT,NT)

logic symbol, 'LS646†



logic symbol, 'LS647†



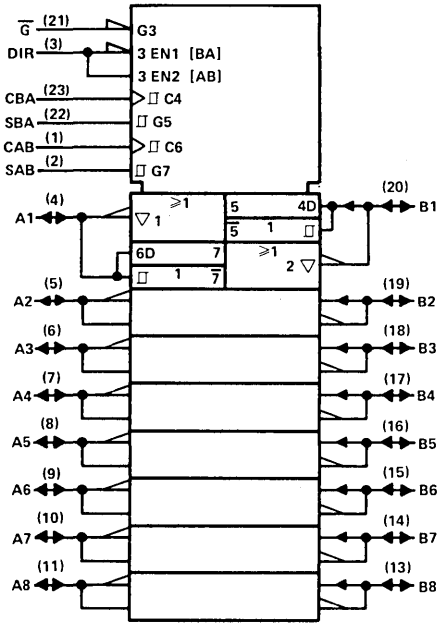
See *TTL Data Book*

†Pin numbers shown on logic symbols are for J, JT, and NT packages only.
nc — no internal connection.

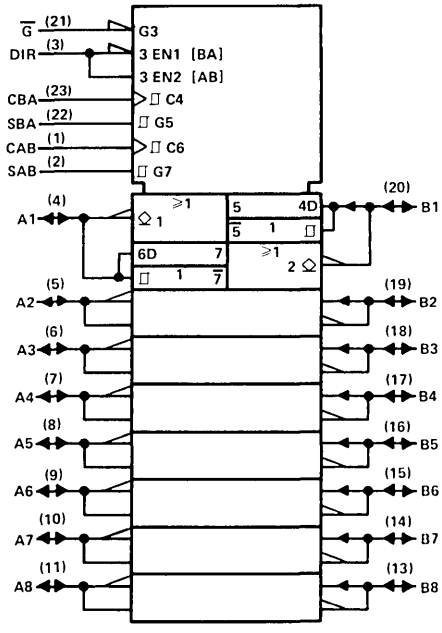
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

646, 647, 648, 649 continued

logic symbol, 'LS648†



logic symbol, 'LS649†



See *TTL Data Book*

†Pin numbers shown on logic symbols are for J, JT, and NT packages only.
nc — no internal connection.

651, 652

OCTAL BUS TRANSCEIVERS AND REGISTERS

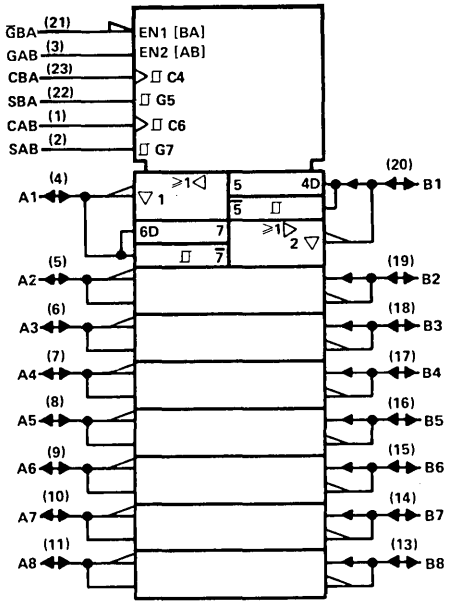
- Bidirectional
- Independent registers for A and B busses

typical performance

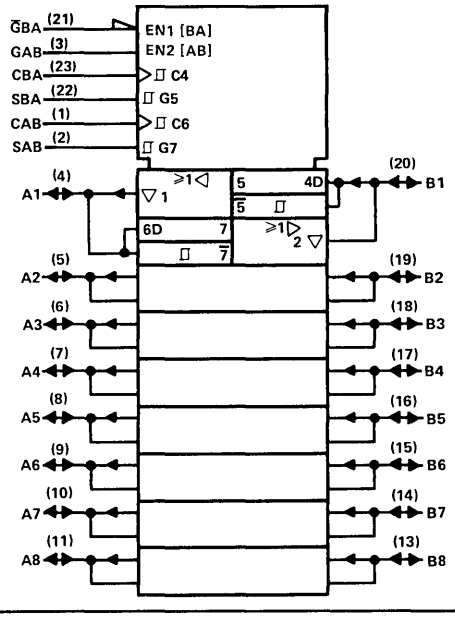
TYPE	MAX SOURCE CURRENT	MAX SINK CURRENT	OUTPUT	
			TYPE	INV
SN54LS651	−12 mA	12 mA	3-State	Yes
SN74LS651	−15 mA	24 mA	3-State	Yes
SN54LS652	−12 mA	12 mA	3-State	No
SN74LS652	−15 mA	24 mA	3-State	No

SN54LS651 (J) SN74LS651 (J,N)
SN54LS652 (J) SN74LS652 (J,N)

logic symbol, 'LS651†



logic symbol, 'LS652†



pin assignments

J, N PACKAGES			
1	CAB	13	B8
2	SAB	14	B7
3	GAB	15	B6
4	A1	16	B5
5	A2	17	B4
6	A3	18	B3
7	A4	19	B2
8	A5	20	B1
9	A6	21	GBA
10	A7	22	SBA
11	A8	23	CBA
12	GND	24	V_{CC}

See *TTL Data Book*

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

668, 669

SYNCHRONOUS 4-BIT UP/ DOWN COUNTERS

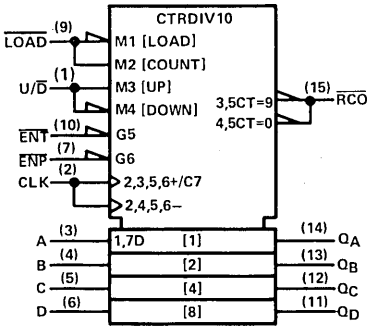
- Programmable, look-ahead
- Decade counter ('LS668)
- Binary counter ('LS669)

typical performance

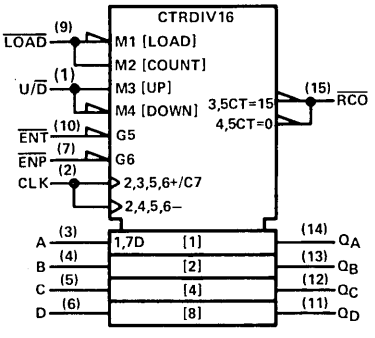
TYPE	COUNT FREQ	PARALLEL LOAD	TOTAL POWER
'LS668	32 MHz	Sync	100 mW
'LS669	32 MHz	Sync	100 mW

SN54LS668 (J,FC) SN74LS668 (J,N)
SN54LS669 (J,FC) SN74LS669 (J,N)

logic symbol, 'LS668†



logic symbol, 'LS669†



pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 U/$\overline{D}$	9 $\overline{LOAD}$	1 U/$\overline{D}$	11 $\overline{LOAD}$
2 CLK	10 $\overline{ENT}$	2 CLK	12 $\overline{ENT}$
3 A	11 QD	3 nc	13 nc
4 B	12 QC	4 A	14 QD
5 C	13 QB	5 B	15 QC
6 D	14 QA	6 C	16 QB
7 $\overline{ENP}$	15 $\overline{RCO}$	7 D	17 QA
8 GND	16 V_{CC}	8 nc	18 nc
		9 $\overline{ENP}$	19 $\overline{RCO}$
		10 GND	20 V_{CC}

See *TTL Data Book*

670

4-BY-4 REGISTER FILES

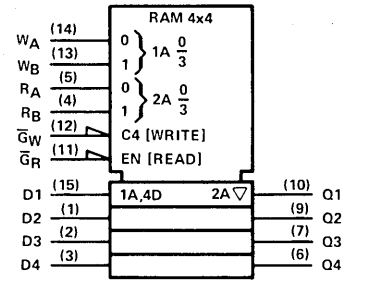
- 3-state outputs
- Simultaneous read/write
- Expandable to 1024 words

typical performance

ADDRESS TIME	ENABLE TIME	POWER/ BIT
24 ns	19 ns	9.3 mW

SN54LS670 (J,FC) SN74LS670 (J,N)

logic symbol†



pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 D2	9 Q2	1 D2	11 Q2
2 D3	10 Q1	2 D3	12 Q1
3 D4	11 $\overline{GR}$	3 nc	13 nc
4 RB	12 $\overline{GW}$	4 D4	14 $\overline{GR}$
5 RA	13 WB	5 RB	15 $\overline{GW}$
6 Q4	14 WA	6 RA	16 WB
7 Q3	15 D1	7 Q4	17 WA
8 GND	16 V_{CC}	8 nc	18 nc
		9 Q3	19 D1
		10 GND	20 V_{CC}

See *TTL Data Book*

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

671, 672

4-BIT UNIVERSAL SHIFT REGISTERS/LATCHES WITH THREE-STATE OUTPUTS

- '671 has direct SR clear
- '672 has synchronous SR clear
- Expandable to any word length
- Multiplexed outputs for shift register or latched data
- Four modes of shift register
  - Inhibit clock
  - Shift right
  - Shift left
  - Parallel load

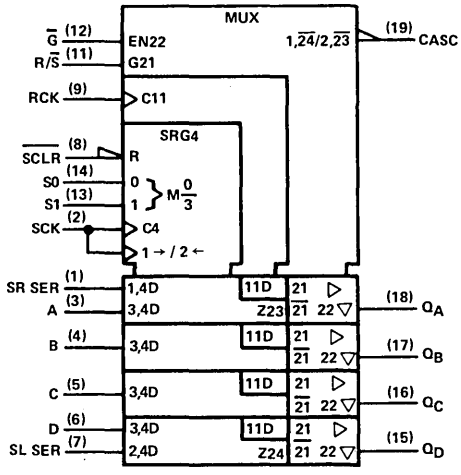
typical performance

TYPE	TOTAL POWER
'LS671	170 mW
'LS672	170 mW

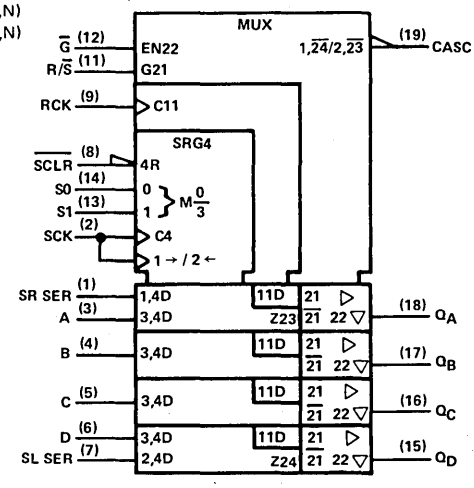
SN54LS671 (J)
SN54LS672 (J)

SN74LS671 (J,N)
SN74LS672 (J,N)

logic symbol, 'LS671†



logic symbol, 'LS672†



See *TTL Data Book*

pin assignments

J, N PACKAGES	
1 SR SER	11 R/S
2 SCK	12 G
3 A	13 S1
4 B	14 S0
5 C	15 QD
6 D	16 QC
7 SL SER	17 QB
8 SCLR	18 QA
9 RCK	19 CASC
10 GND	20 V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

673

16-BIT SHIFT REGISTERS

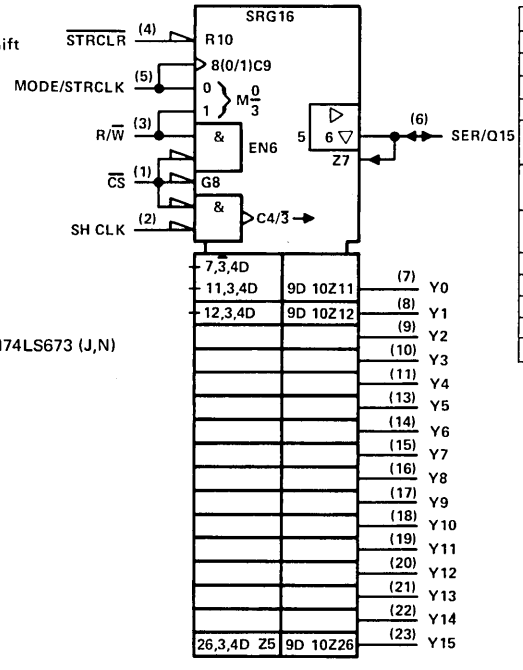
- 16-bit serial-in/serial-out shift register with three-state outputs
- 16-bit parallel-out storage register
- Converts serial to parallel data flow

typical performance

TYPE	SHIFT FREQ	TOTAL POWER
'LS673	20 MHz	255 mW

SN54LS673 (J,FC) SN74LS673 (J,N)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	$\overline{CS}$	13	Y5	1	$\overline{CS}$	15	Y5
2	SH CLK	14	Y6	2	SH CLK	16	Y6
3	R/$\overline{W}$	15	Y7	3	R/$\overline{W}$	17	Y7
4	$\overline{STRCLR}$	16	Y8	4	nc	18	Y8
5	MODE/ STRCLK	17	Y9	5	$\overline{STRCLR}$	19	nc
6	SER/ Q15	18	Y10	6	MODE/ STRCLK	20	Y9
7	Y0	19	Y11	7	SER/ Q15	21	Y10
8	Y1	20	Y12	8	Y0	22	Y11
9	Y2	21	Y13	9	Y1	23	Y12
10	Y3	22	Y14	10	Y2	24	Y13
11	Y4	23	Y15	11	nc	25	nc
12	GND	24	V_{CC}	12	Y3	26	Y14
				13	Y4	27	Y15
				14	GND	28	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

8

674

16-BIT SHIFT REGISTER

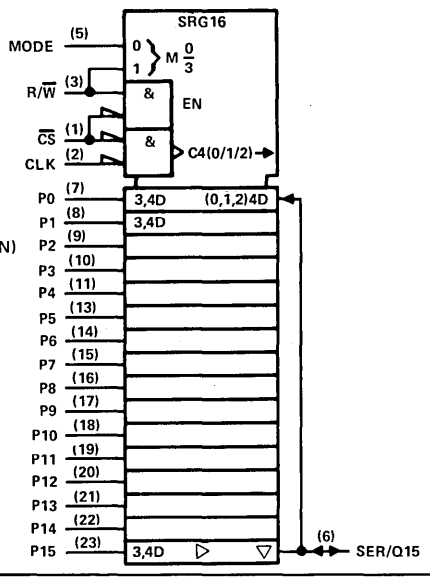
- Performs parallel to serial conversion
- Three-state outputs

typical performance

TYPE	SHIFT FREQ	TOTAL POWER
'LS674	20 MHz	125 mW

SN54LS674 (J,FC) SN74LS674 (J,N)

logic symbol†



pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 $\overline{CS}$	13 P5	1 $\overline{CS}$	15 P5
2 CLK	14 P6	2 CLK	16 P6
3 R/$\overline{W}$	15 P7	3 R/$\overline{W}$	17 P7
4 nc	16 P8	4 nc	18 P8
5 MODE	17 P9	5 nc	19 nc
6 SER/Q15	18 P10	6 MODE	20 P9
7 P0	19 P11	7 SER/Q15	21 P10
8 P1	20 P12	8 P0	22 P11
9 P2	21 P13	9 P1	23 P12
10 P3	22 P14	10 P2	24 P13
11 P4	23 P15	11 nc	25 nc
12 GND	24 V_{CC}	12 P3	26 P14
		13 P4	27 P15
		14 GND	28 V_{CC}

See *TTL Data Book*

681

4-BIT PARALLEL BINARY ACCUMULATORS

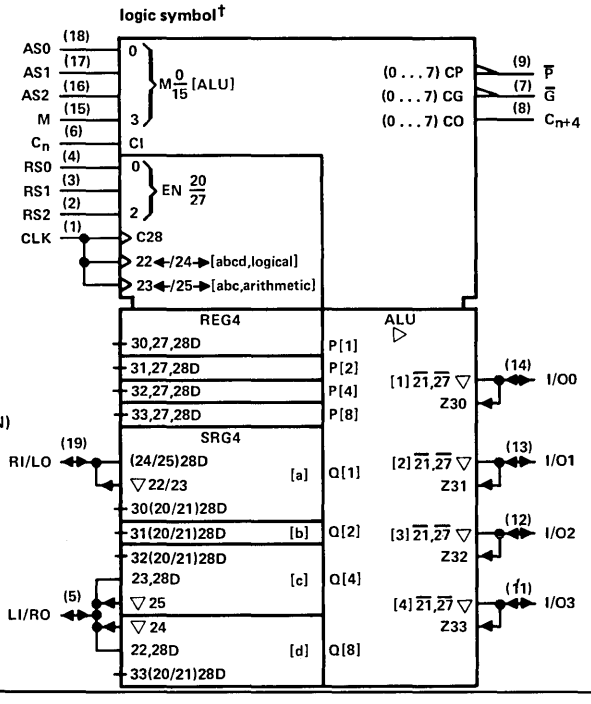
- Contains two synchronous registers
- B register frequency = 20 MHz
- Arithmetic operations include B minus A and A minus B
- Bus-driving I/O ports

typical performance

TYPE	LOAD TIME	ACC TIME
'LS681	75 ns	50 ns

SN54LS681 (J) SN74LS681 (J,N)

logic symbol†



pin assignments

J, N PACKAGES	
1 CLK	11 I/O3
2 RS2	12 I/O2
3 RS1	13 I/O1
4 RS0	14 I/O0
5 LI/RO	15 M
6 C_n	16 AS2
7 $\overline{G}$	17 AS1
8 C_{n+4}	18 AS0
9 $\overline{P}$	19 RI/LO
10 GND	20 V_{CC}

See *TTL Data Book*

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

682, 683
684, 685

8-BIT MAGNITUDE COMPARATORS

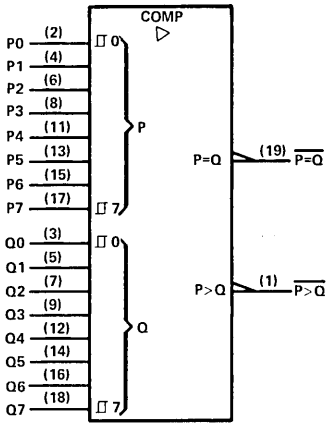
- Compares two 8-bit words
- 'LS682 and 'LS683 includes 20-kilohm pull-up resistor on Q inputs

typical performance

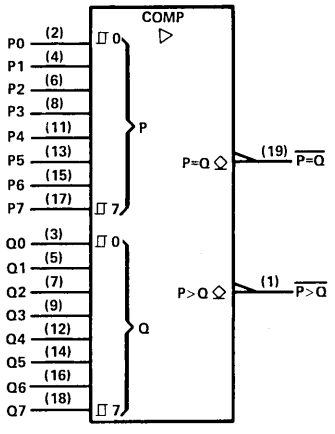
TYPE	COMPARE TIME	TYPE OUTPUT	TOTAL POWER
'LS682	14 ns	Totem Pole	210 mW
'LS683	24 ns	O-C	210 mW
'LS684	16 ns	Totem Pole	200 mW
'LS685	24 ns	O-C	200 mW

SN54LS682 (J,FC) SN74LS682 (J,N)
SN54LS683 (J,FC) SN74LS683 (J,N)
SN54LS684 (J,FC) SN74LS684 (J,N)
SN54LS685 (J,FC) SN74LS685 (J,N)

logic symbol, 'LS682, 'LS684†



logic symbol, 'LS683, 'LS685†



See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	$\overline{P>Q}$	11	P4	1	$\overline{P>Q}$	15	P4
2	P0	12	Q4	2	nc	16	Q4
3	Q0	13	P5	3	nc	17	P5
4	P1	14	Q5	4	nc	18	nc
5	Q1	15	P6	5	P0	19	nc
6	P2	16	Q6	6	Q0	20	Q5
7	Q2	17	P7	7	P1	21	P6
8	P3	18	Q7	8	Q1	22	Q6
9	Q3	19	$\overline{P=Q}$	9	P2	23	P7
10	GND	20	V_{CC}	10	Q2	24	Q7
				11	nc	25	$\overline{P=Q}$
				12	P3	26	nc
				13	Q3	27	nc
				14	GND	28	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

8

686, 687

8-BIT MAGNITUDE COMPARATORS

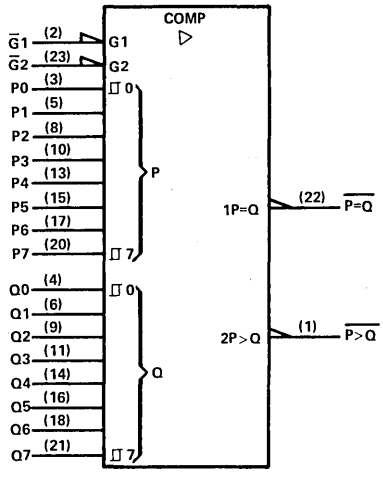
- Compares two 8-bit words

typical performance

TYPE	COMPARE TIME	TYPE OUTPUT	TOTAL POWER
'LS686	17 ns	Totem-Pole	220 mW
'LS687	22 ns	O-C	220 mW

SN54LS686 (J,FC) SN74LS686 (JT,NT)
SN54LS687 (J,FC) SN74LS687 (JT,NT)

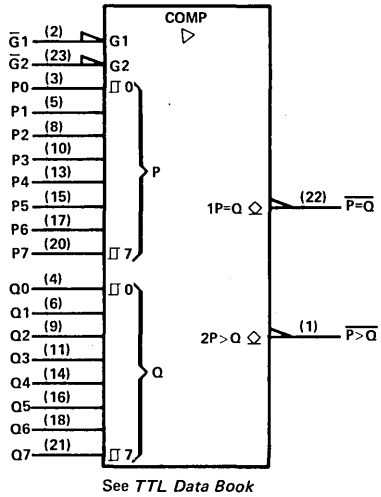
logic symbol, 'LS686†



pin assignments

J, JT, NT PACKAGES				FC, FN PACKAGES			
1	P>Q	13	P4	1	P>Q	15	P4
2	G1	14	Q4	2	nc	16	Q4
3	P0	15	P5	3	G1	17	P5
4	Q0	16	Q5	4	nc	18	nc
5	P1	17	P6	5	P0	19	nc
6	Q1	18	Q6	6	Q0	20	Q5
7	nc	19	nc	7	P1	21	P6
8	P2	20	P7	8	Q1	22	Q6
9	Q2	21	Q7	9	P2	23	P7
10	P3	22	P=Q	10	Q2	24	Q7
11	Q3	23	G2	11	nc	25	P=Q
12	GND	24	V_{CC}	12	P3	26	nc
				13	Q3	27	G2
				14	GND	28	V_{CC}

logic symbol, 'LS687†



See *TTL Data Book*

† Pin numbers shown on logic symbols are for J, JT, NT, N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

688, 689

8-BIT MAGNITUDE COMPARATORS

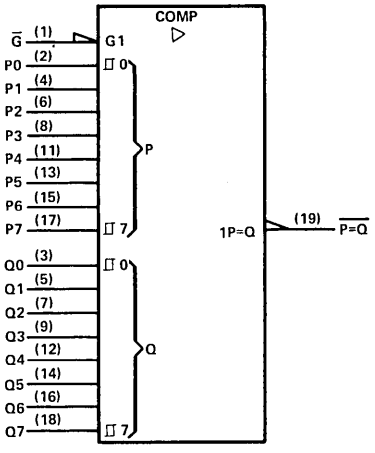
- Compares two 8-bit words

typical performance

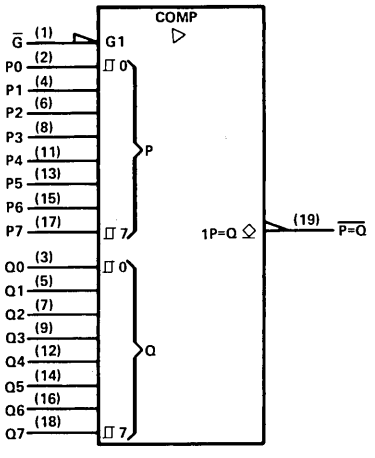
TYPE	COMPARE TIME	TYPE OUTPUT	TOTAL POWER
'LS688	14.5 ns	Totem-Pole	200 mW
'LS689	23 ns	O-C	200 mW

SN54LS688 (J,FC) SN74LS688 (J,N)
SN54LS689 (J,FC) SN74LS689 (J,N)

logic symbol, 'LS688†



logic symbol, 'LS689†



See *TTL Data Book*

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	$\overline{G}$	11	P4	1	nc	15	P4
2	P0	12	Q4	2	nc	16	Q4
3	Q0	13	P5	3	$\overline{G}$	17	P5
4	P1	14	Q5	4	nc	18	nc
5	Q1	15	P6	5	P0	19	nc
6	P2	16	Q6	6	Q0	20	Q5
7	Q2	17	P7	7	P1	21	P6
8	P3	18	Q7	8	Q1	22	Q6
9	Q3	19	$\overline{P=Q}$	9	P2	23	P7
10	GND	20	V_{CC}	10	Q2	24	Q7
				11	nc	25	$\overline{P=Q}$
				12	P3	26	nc
				13	Q3	27	nc
				14	GND	28	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc – no internal connection.

8

690, 691
692, 693

SYNCHRONOUS COUNTERS WITH OUTPUT REGISTERS

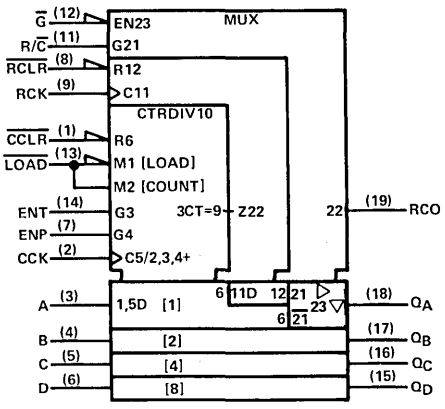
- Multiplexed three-state outputs
- 4-bit counters/registers
- 'LS690, 'LS692: Decade counters
- 'LS691, 'LS693: Binary counters

typical performance

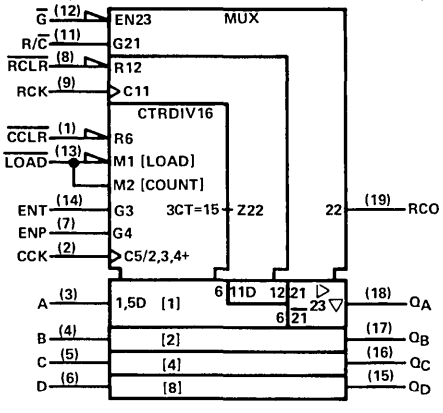
TYPE	CLEAR	MAX CLOCK FREQ	TOTAL POWER
'LS690	Direct	20 MHz	237 mW
'LS691	Direct	20 MHz	237 mW
'LS692	Sync-L	20 MHz	237 mW
'LS693	Sync-L	20 MHz	237 mW

SN54LS690 (J) SN74LS690 (J,N)
SN54LS691 (J) SN74LS691 (J,N)
SN54LS692 (J) SN74LS692 (J,N)
SN54LS693 (J) SN74LS693 (J,N)

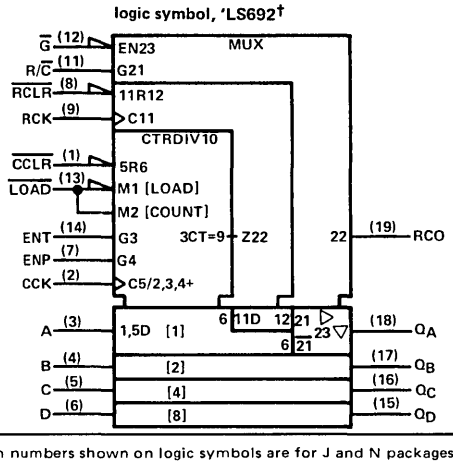
logic symbol, 'LS690†



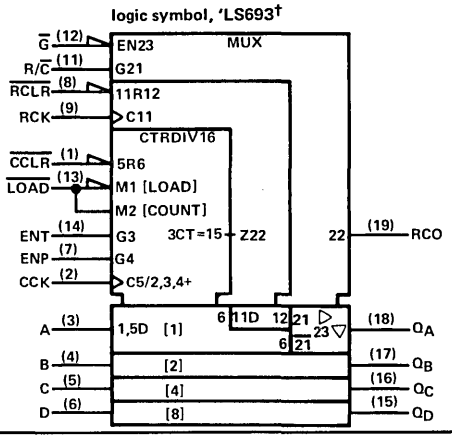
logic symbol, 'LS691†



logic symbol, 'LS692†



logic symbol, 'LS693†



pin assignments

J, N PACKAGES			
1	$\overline{CCLR}$	11	R/$\overline{C}$
2	CCK	12	$\overline{G}$
3	A	13	$\overline{LOAD}$
4	B	14	ENT
5	C	15	QD
6	D	16	QC
7	ENP	17	QB
8	$\overline{RCLR}$	18	QA
9	RCK	19	RCO
10	GND	20	V_{CC}

See *TTL Data Book*

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

696, 697
698, 699

SYNCHRONOUS UP/DOWN COUNTERS WITH OUTPUT REGISTERS, MULTIPLEXED THREE-STATE OUTPUTS

- 4-bit counters/registers
- 'LS696, 'LS698: Decade counters
- 'LS697, 'LS699: Binary counters

pin assignments

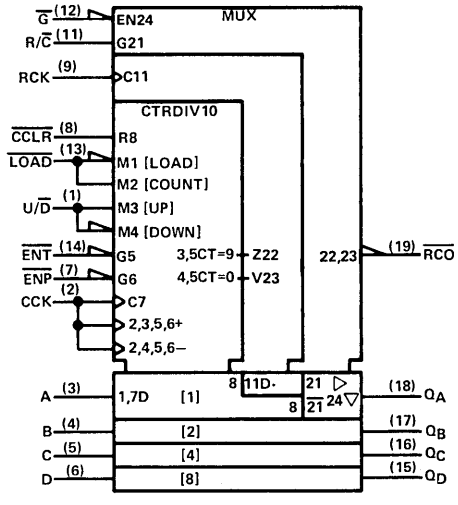
J, N PACKAGES			
1	$U/\overline{D}$	11	$R/\overline{C}$
2	CCK	12	$\overline{G}$
3	A	13	$\overline{LOAD}$
4	B	14	$\overline{ENT}$
5	C	15	QD
6	D	16	QC
7	$\overline{ENP}$	17	QB
8	$\overline{CCLR}$	18	QA
9	RCK	19	$\overline{RCO}$
10	GND	20	V_{CC}

typical performance

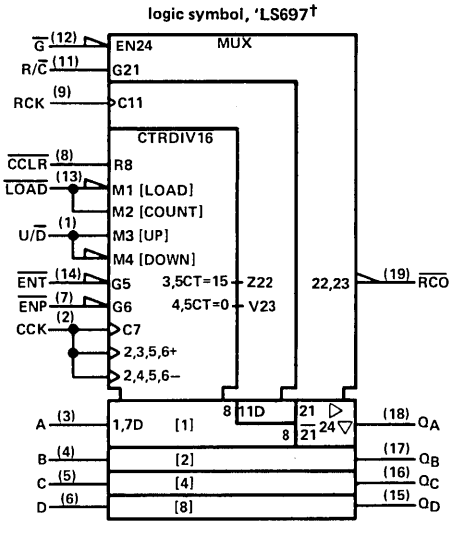
TYPE	MAX CLOCK FREQ	CLEAR	TOTAL POWER
'LS696	20 MHz	Async-L	237 mW
'LS697	20 MHz	Async-L	237 mW
'LS698	20 MHz	Sync-L	237 mW
'LS699	20 MHz	Sync-L	237 mW

SN54LS696 (J) SN74LS696 (J,N)
SN54LS697 (J) SN74LS697 (J,N)
SN54LS698 (J) SN74LS698 (J,N)
SN54LS699 (J) SN74LS699 (J,N)

logic symbol, 'LS696†



logic symbol, 'LS697†

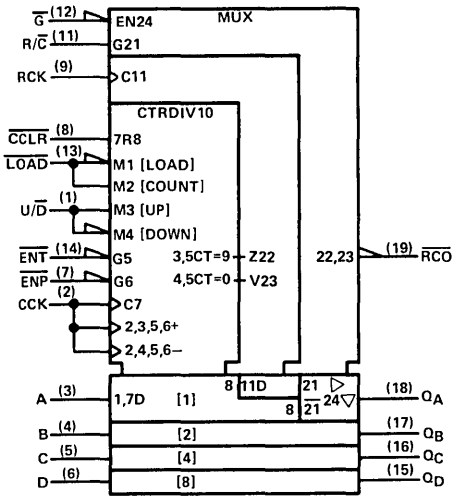


See *TTL Data Book*

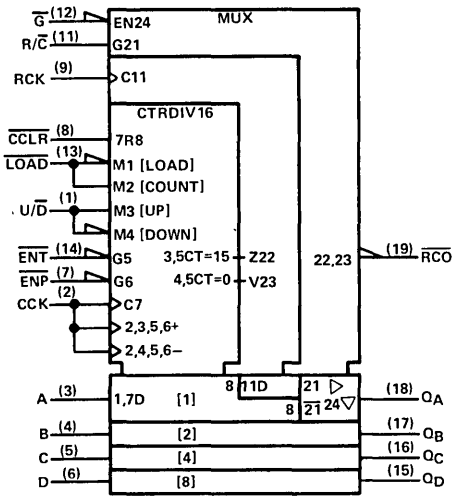
† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

696, 697, 698, 699 continued

logic symbol, 'LS698†



logic symbol, 'LS699†



See *TTL Data Book*

800

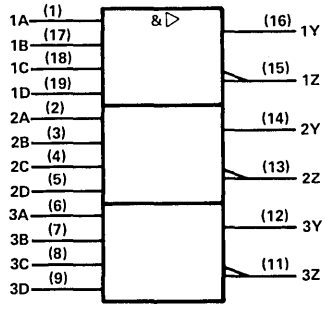
TRIPLE 4-INPUT AND/NAND DRIVERS

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT	POWER/GATE
SN54AS800	40 mA	−40 mA	25 mW
SN74AS800	48 mA	−48 mA	25 mW

SN54AS800 (J,FC) SN74AS800 (J,N,FN)

logic symbol†



positive logic: $Y = ABCD$
$Z = \overline{ABCD}$

pin assignments

J, N PACKAGES			
1	1A	11	3Z
2	2A	12	3Y
3	2B	13	2Z
4	2C	14	2Y
5	2D	15	1Z
6	3A	16	1Y
7	3B	17	1B
8	3C	18	1C
9	3D	19	1D
10	GND	20	V_{CC}

FC, FN PACKAGES			
1	1A	11	3Z
2	2A	12	3Y
3	2B	13	2Z
4	2C	14	2Y
5	2D	15	1Z
6	3A	16	1Y
7	3B	17	1B
8	3C	18	1C
9	3D	19	1D
10	GND	20	V_{CC}

See *TTL Data Book*

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

802

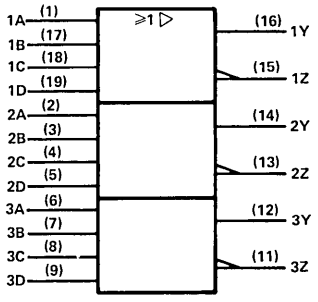
TRIPLE 4-INPUT OR/NOR LINE DRIVERS

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT	POWER/GATE
SN54AS802	40 mA	–40 mA	25 mW
SN74AS802	48 mA	–48 mA	25 mW

SN54AS802 (J,FC) SN74AS802 (J,N,FN)

logic symbol†



positive logic: $Y = A+B+C+D$

$Z = \overline{A+B+C+D}$

pin assignments

J, N PACKAGES	
1 1A	11 3Z
2 2A	12 3Y
3 2B	13 2Z
4 2C	14 2Y
5 2D	15 1Z
6 3A	16 1Y
7 3B	17 1B
8 3C	18 1C
9 3D	19 1D
10 GND	20 V_{CC}

FC, FN PACKAGES	
1 1A	11 3Z
2 2A	12 3Y
3 2B	13 2Z
4 2C	14 2Y
5 2D	15 1Z
6 3A	16 1Y
7 3B	17 1B
8 3C	18 1C
9 3D	19 1D
10 GND	20 V_{CC}

See *TTL Data Book*

804

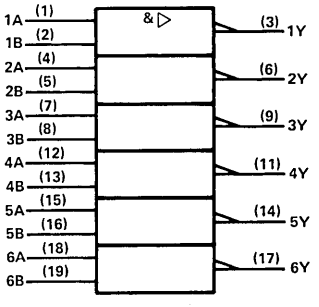
HEX 2-INPUT NAND DRIVERS

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT	DELAY	POWER/GATE
SN54ALS804	12 mA	–12 mA		
SN74ALS804	24 mA	–15 mA		
SN54AS804	40 mA	–40 mA	2 ns	22 mW
SN74AS804	48 mA	–48 mA	2 ns	22 mW

SN54ALS804 (J,FC) SN74ALS804 (J,N,FN)
SN54AS804 (J,FC) SN74AS804 (J,N,FN)

logic symbol†



positive logic: $Y = \overline{AB}$

pin assignments

J, N PACKAGES	
1 1A	11 4Y
2 1B	12 4A
3 1Y	13 4B
4 2A	14 5Y
5 2B	15 5A
6 2Y	16 5B
7 3A	17 6Y
8 3B	18 6A
9 3Y	19 6B
10 GND	20 V_{CC}

FC, FN PACKAGES	
1 1A	11 4Y
2 1B	12 4A
3 1Y	13 4B
4 2A	14 5Y
5 2B	15 5A
6 2Y	16 5B
7 3A	17 6Y
8 3B	18 6A
9 3Y	19 6B
10 GND	20 V_{CC}

See *TTL Data Book*

† Pin numbers shown on logic symbols are for J and N packages only.
nc – no internal connection.

8

805

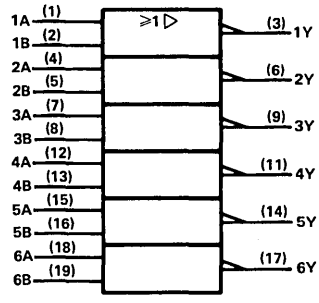
HEX 2-INPUT NOR DRIVERS

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT	DELAY	POWER/GATE
SN54ALS805	12 mA	–12 mA		
SN74ALS805	24 mA	–15 mA		
SN54AS805	40 mA	–40 mA	2 ns	30 mW
SN74AS805	48 mA	–48 mA	2 ns	30 mW

SN54ALS805 (J,FC) SN74ALS805 (J,N,FN)
SN54AS805 (J,FC) SN74AS805 (J,N,FN)

logic symbol†



positive logic: $Y = \overline{A+B}$

pin assignments

J, N PACKAGES	
1 1A	11 4Y
2 1B	12 4A
3 1Y	13 4B
4 2A	14 5Y
5 2B	15 5A
6 2Y	16 5B
7 3A	17 6Y
8 3B	18 6A
9 3Y	19 6B
10 GND	20 V_{CC}

FC, FN PACKAGES	
1 1A	11 4Y
2 1B	12 4A
3 1Y	13 4B
4 2A	14 5Y
5 2B	15 5A
6 2Y	16 5B
7 3A	17 6Y
8 3B	18 6A
9 3Y	19 6B
10 GND	20 V_{CC}

See *TTL Data Book*

808

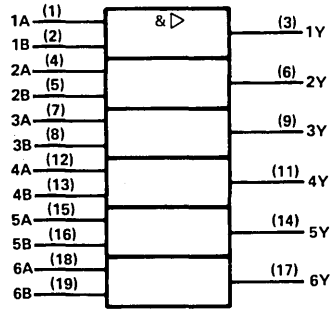
HEX 2-INPUT AND DRIVERS

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT	DELAY	POWER/GATE
SN54ALS808	12 mA	–12 mA		
SN74ALS808	24 mA	–15 mA		
SN54AS808	40 mA	–40 mA	3 ns	34 mW
SN74AS808	48 mA	–48 mA	3 ns	34 mW

SN54ALS808 (J,FC) SN74ALS808 (J,N,FN)
SN54AS808 (J,FC) SN74AS808 (J,N,FN)

logic symbol†



positive logic: $Y = AB$

pin assignments

J, N PACKAGES	
1 1A	11 4Y
2 1B	12 4A
3 1Y	13 4B
4 2A	14 5Y
5 2B	15 5A
6 2Y	16 5B
7 3A	17 6Y
8 3B	18 6A
9 3Y	19 6B
10 GND	20 V_{CC}

FC, FN PACKAGES	
1 1A	11 4Y
2 1B	12 4A
3 1Y	13 4B
4 2A	14 5Y
5 2B	15 5A
6 2Y	16 5B
7 3A	17 6Y
8 3B	18 6A
9 3Y	19 6B
10 GND	20 V_{CC}

See *TTL Data Book*

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

832

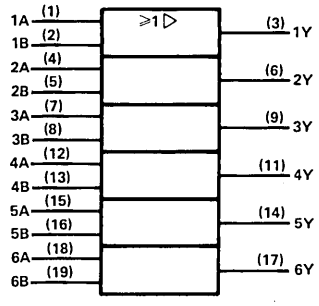
HEX 2-INPUT OR DRIVERS

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT	DELAY	POWER/GATE
SN54ALS832	12 mA	−12 mA		
SN74ALS832	24 mA	−15 mA		
SN54AS832	40 mA	−40 mA	3 ns	43 mW
SN74AS832	48 mA	−48 mA	3 ns	43 mW

SN54ALS832 (J,FC) SN74ALS832 (J,N,FN)
SN54AS832 (J,FC) SN74AS832 (J,N,FN)

logic symbol†



positive logic: Y = A+B

pin assignments

J, N PACKAGES	
1 1A	11 4Y
2 1B	12 4A
3 1Y	13 4B
4 2A	14 5Y
5 2B	15 5A
6 2Y	16 5B
7 3A	17 6Y
8 3B	18 6A
9 3Y	19 6B
10 GND	20 V_{CC}

FC, FN PACKAGES	
1 1A	11 4Y
2 1B	12 4A
3 1Y	13 4B
4 2A	14 5Y
5 2B	15 5A
6 2Y	16 5B
7 3A	17 6Y
8 3B	18 6A
9 3Y	19 6B
10 GND	20 V_{CC}

See *TTL Data Book*

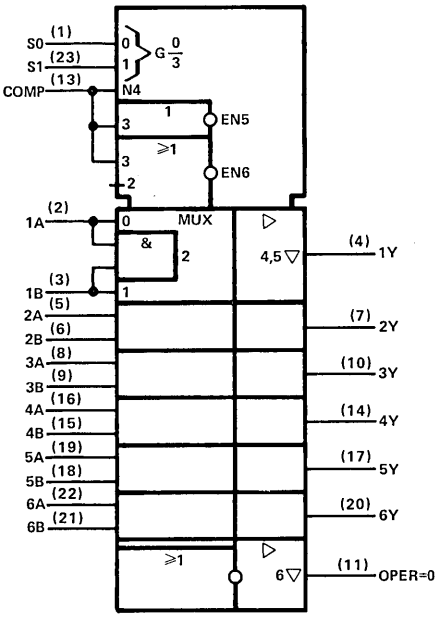
857

HEX 2-TO-1 UNIVERSAL MULTIPLEXER

- Three-state buffer-type outputs
- True or complementary data

SN54ALS857 (J,FC) SN74ALS857 (JT,NT,FN)
SN54AS857 (J,FC) SN74AS857 (JT,NT,FN)

logic symbol†



pin assignments

J, JT, NT PACKAGES	
1 S0	13 COMP
2 1A	14 4Y
3 1B	15 4B
4 1Y	16 4A
5 2A	17 5Y
6 2B	18 5B
7 2Y	19 5A
8 3A	20 6Y
9 3B	21 6B
10 3Y	22 6A
11 OPER=0	23 S1
12 GND	24 V_{CC}

FC, FN PACKAGES	
1 S0	15 COMP
2 1A	16 4Y
3 1B	17 4B
4 1Y	18 4A
5 nc	19 nc
6 nc	20 nc
7 2A	21 5Y
8 2B	22 5B
9 2Y	23 5A
10 3A	24 6Y
11 3B	25 6B
12 3Y	26 6A
13 OPER=0	27 S1
14 GND	28 V_{CC}

See *TTL Data Book*

† Pin numbers shown on logic symbols are for J, JT and NT packages only.
nc — no internal connection.

8

867, 869

8-BIT SYNCHRONOUS BIDIRECTIONAL COUNTERS

- 'AS867 has asynchronous clear
- 'AS869 has synchronous clear
- Ripple carry output for N-bit cascading
- Fully programmable with synchronous counting and loading

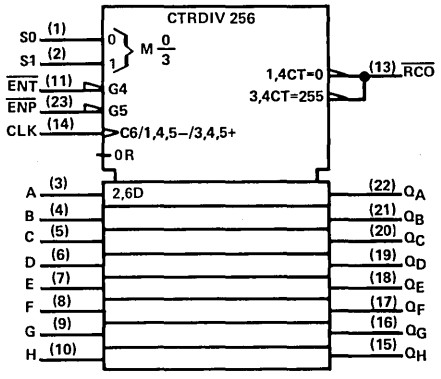
FUNCTION TABLE

S1	S0	FUNCTION
L	L	Clear
L	H	Count Down
H	L	Load
H	H	Count Up

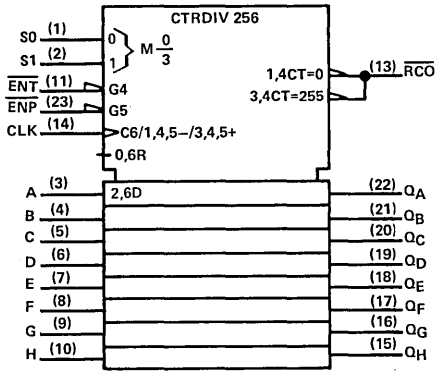
Supersedes table in *1981 Supplement to TTL Data Book*

SN54AS867 (J,FC) SN74AS867 (J,JT,NT)
SN54AS869 (J,FC) SN74AS869 (J,JT,NT)

logic symbol 'AS867†



logic symbol 'AS869†



pin assignments

J, JT, NT PACKAGES			
1	S0	13	$\overline{RCO}$
2	S1	14	CLK
3	A	15	QH
4	B	16	QG
5	C	17	QF
6	D	18	QE
7	E	19	QD
8	F	20	QC
9	G	21	QB
10	H	22	QA
11	$\overline{ENT}$	23	$\overline{ENP}$
12	GND	24	V_{CC}

FC, FN PACKAGES			
1	S0	15	$\overline{RCO}$
2	S1	16	CLK
3	A	17	QH
4	B	18	QG
5	nc	19	nc
6	nc	20	nc
7	C	21	QF
8	D	22	QE
9	E	23	QD
10	F	24	QC
11	G	25	QB
12	H	26	QA
13	$\overline{ENT}$	27	$\overline{ENP}$
14	GND	28	V_{CC}

See *TTL Data Book*

† Pin numbers shown on logic symbols are for J, JT and NT packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

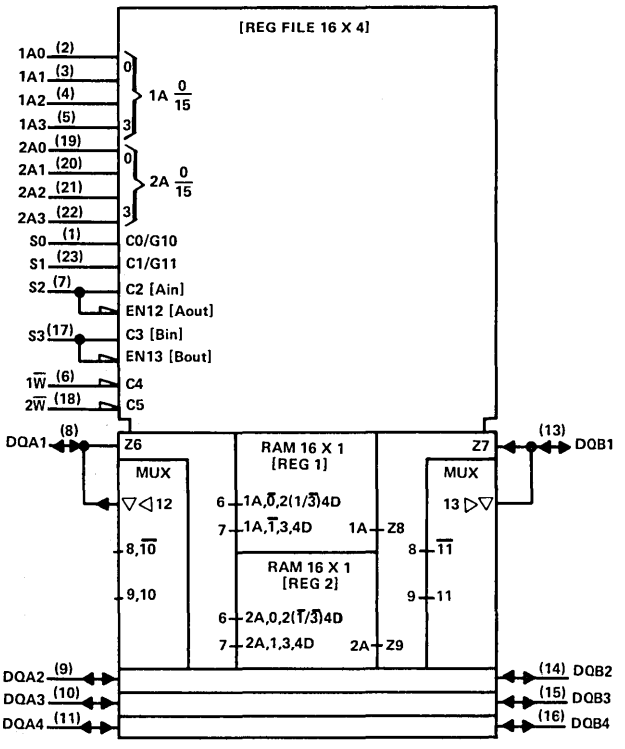
870

DUAL 16-BY-4 REGISTER FILES

- Each register file has individual write/enable controls and address lines
- Has two 4-bit data I/O ports
- 24-pin 300-mil package

SN54AS870 (J,FC)
SN74AS870 (JT,NT,FN)

logic symbol†



See *TTL Data Book*

pin assignments

J, JT, NT PACKAGES			
1	S0	13	DQB1
2	1A0	14	DQB2
3	1A1	15	DQB3
4	1A2	16	DQB4
5	1A3	17	S3
6	$\overline{1W}$	18	$\overline{2W}$
7	S2	19	2A0
8	DQA1	20	2A1
9	DQA2	21	2A2
10	DQA3	22	2A3
11	DQA4	23	S1
12	GND	24	V_{CC}

FC, FN PACKAGES			
1	S0	15	DQB1
2	1A0	16	DQB2
3	1A1	17	DQB3
4	1A2	18	DQB4
5	nc	19	nc
6	nc	20	nc
7	1A3	21	S3
8	$\overline{1W}$	22	$\overline{2W}$
9	S2	23	2A0
10	DQA1	24	2A1
11	DQA2	25	2A2
12	DQA3	26	2A3
13	DQA4	27	S1
14	GND	28	V_{CC}

† Pin numbers shown on logic symbols are for J, JT and NT packages only.
nc — no internal connection.

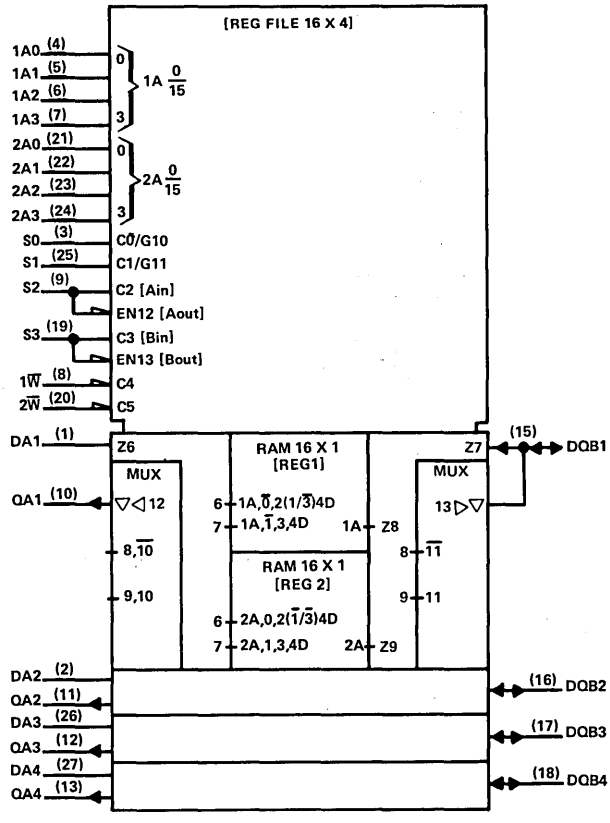
871

DUAL 16-BY-4 REGISTER FILES

- Each register file has individual write/enable controls and address lines
- Has one 4-bit data I/O port; the other 4-bit data word has individual data inputs and data outputs
- 28-pin, 600-mil package

SN54AS871 (J,FC)
SN74AS871 (J,N,FN)

logic symbol†



See *TTL Data Book*

pin assignments

J, N PACKAGES	
1 DA1	15 DQB1
2 DA2	16 DQ
3 S0	17 DQB2
4 1A0	18 DQB4
5 1A1	19 S3
6 1A2	20 2W
7 1A3	21 2A0
8 1W	22 2A1
9 S2	23 2A2
10 QA1	24 2A3
11 QA2	25 S1
12 QA3	26 DA3
13 QA4	27 DA4
14 GND	28 V_{CC}

FC, FN PACKAGES	
1 DA1	15 DQB1
2 DA2	16 DQB2
3 S0	17 DQB3
4 1A0	18 DQB4
5 1A1	19 S3
6 1A2	20 2W
7 1A3	21 2A0
8 1W	22 2A1
9 S2	23 2A2
10 QA1	24 2A3
11 QA2	25 S1
12 QA3	26 DA3
13 QA4	27 DA4
14 GND	28 V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

873

DUAL 4-BIT D-TYPE LATCHES

- Three-state buffer-type outputs drive bus lines directly
- Each 4-bit word has enable, clear, and output control inputs

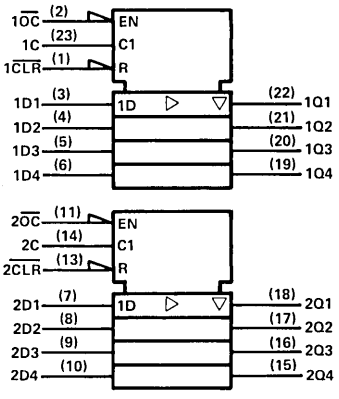
typical performance

TYPE	CLEAR	OUTPUT	DELAY	POWER
'ALS873	LOW	Q	11 ns	67.5 mW

SN54ALS873 (J,FC) SN74ALS873 (JT,NT,FN)
SN54AS873 (J,FC) SN74AS873 (JT,NT,FN)

See *TTL Data Book*

logic symbol†



pin assignments

J, JT, NT PACKAGES		FC, FN PACKAGES	
1 $1\overline{CLR}$	13 $2\overline{CLR}$	1 $1\overline{CLR}$	15 $2\overline{CLR}$
2 $1\overline{OC}$	14 2C	2 $1\overline{OC}$	16 2C
3 1D1	15 2Q4	3 1D1	17 2Q4
4 1D2	16 2Q3	4 1D2	18 2Q3
5 1D3	17 2Q2	5 nc	19 nc
6 1D4	18 2Q1	6 nc	20 nc
7 2D1	19 1Q4	7 1D3	21 2Q2
8 2D2	20 1Q3	8 1D4	22 2Q1
9 2D3	21 1Q2	9 2D1	23 1Q4
10 2D4	22 1Q1	10 2D2	24 1Q3
11 $2\overline{OC}$	23 1C	11 2D3	25 1Q2
12 GND	24 V_{CC}	12 2D4	26 1Q1
		13 $2\overline{OC}$	27 1C
		14 GND	28 V_{CC}

874

DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS

- Three-state buffer-type outputs
- Each 4-bit word has clock, clear, and output control inputs

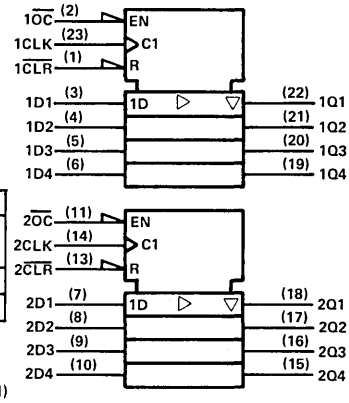
typical performance

TYPE	FREQ	POWER	DATA TIMES	
			SET-UP	HOLD
SN54ALS874	50 MHz	86.7 mW	10 ns†	4 ns†
SN74ALS874	50 MHz	86.7 mW	10 ns†	0 ns†

† Rising edge of clock pulse

SN54ALS874 (J,FC) SN74ALS874 (JT,NT,FN)
SN54AS874 (J,FC) SN74AS874 (JT,NT,FN)

logic symbol†



pin assignments

J, JT, NT PACKAGES		FC, FN PACKAGES	
1 $1\overline{CLR}$	13 $2\overline{CLR}$	1 $1\overline{CLR}$	15 $2\overline{CLR}$
2 $1\overline{OC}$	14 2CLK	2 $1\overline{OC}$	16 2CLK
3 1D1	15 2Q4	3 1D1	17 2Q4
4 1D2	16 2Q3	4 1D2	18 2Q3
5 1D3	17 2Q2	5 nc	19 nc
6 1D4	18 2Q1	6 nc	20 nc
7 2D1	19 1Q4	7 1D3	21 2Q2
8 2D2	20 1Q3	8 1D4	22 2Q1
9 2D3	21 1Q2	9 2D1	23 1Q4
10 2D4	22 1Q1	10 2D2	24 1Q3
11 $2\overline{OC}$	23 1CLK	11 2D3	25 1Q2
12 GND	24 V_{CC}	12 2D4	26 1Q1
		13 $2\overline{OC}$	27 1CLK
		14 GND	28 V_{CC}

See *TTL Data Book*

† Pin numbers shown on logic symbols are for J, JT and NT packages only.
nc — no internal connection.

8

876

DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH INVERTED OUTPUTS

- Three-state buffer-type outputs drive bus lines directly
- Each 4-bit word has own clock, preset, and output control inputs

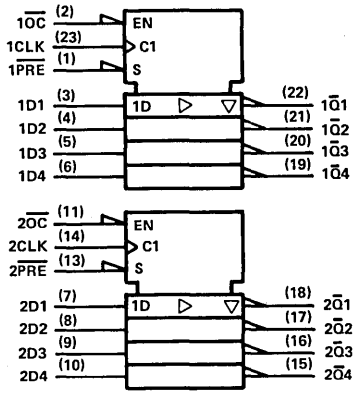
typical performance

TYPE	FREQ	POWER	DATA TIMES	
			SET-UP	HOLD
SN54ALS876	50 MHz	86.7 mW	10 ns†	4 ns†
SN74ALS876	50 MHz	86.7 mW	10 ns†	0 ns†

† Rising edge of clock pulse

SN54ALS876 (J,FC)
SN54AS876 (J,FC)
SN74ALS876 (JT,NT,FN)
SN74AS876 (JT,NT,FN)

logic symbol†



pin assignments

J, JT, NT PACKAGES			
1	1PRE	13	2PRE
2	1OC	14	2CLK
3	1D1	15	2Q4
4	1D2	16	2Q3
5	1D3	17	2Q2
6	1D4	18	2Q1
7	2D1	19	1Q4
8	2D2	20	1Q3
9	2D3	21	1Q2
10	2D4	22	1Q1
11	2OC	23	1CLK
12	GND	24	V_{CC}

FC, FN PACKAGES			
1	1PRE	15	2PRE
2	1OC	16	2CLK
3	1D1	17	2Q4
4	1D2	18	2Q3
5	nc	19	nc
6	nc	20	nc
7	1D3	21	2Q2
8	1D4	22	2Q1
9	2D1	23	1Q4
10	2D2	24	1Q3
11	2D3	25	1Q2
12	2D4	26	1Q1
13	2OC	27	1CLK
14	GND	28	V_{CC}

See *TTL Data Book*

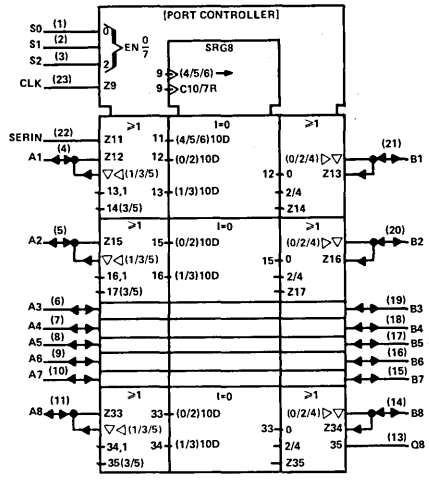
877

8-BIT UNIVERSAL TRANSCEIVER/PORT CONTROLLERS

- 8 selectable transceiver/port functions
- 3-state buffer-type outputs drive bus lines directly
- 24-pin 300-mil package

SN54AS877 (J,FC)
SN74AS877 (JT,NT,FN)

logic symbol†



pin assignments

JT, NT, FN PACKAGES				FC, FN PACKAGES			
1	S0	13	Q8	1	S0	15	Q8
2	S1	14	B8	2	S1	16	B8
3	S2	15	B7	3	S2	17	B7
4	A1	16	B6	4	A1	18	B6
5	A2	17	B5	5	nc	19	nc
6	A3	18	B4	6	nc	20	nc
7	A4	19	B3	7	A2	21	B5
8	A5	20	B2	8	A3	22	B4
9	A6	21	B1	9	A4	23	B3
10	A7	22	SERIN	10	A5	24	B2
11	A8	23	CLK	11	A6	25	B1
12	GND	24	V_{CC}	12	A7	26	SERIN
				13	A8	27	CLK
				14	GND	28	V_{CC}

See *TTL Data Book*

† Pin numbers shown on logic symbols are for J, JT and NT packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

880

DUAL 4-BIT D-TYPE LATCHES WITH INVERTED OUTPUTS

- Three-state buffer-type outputs drive bus lines directly
- Each 4-bit word has enable, preset, and output control inputs

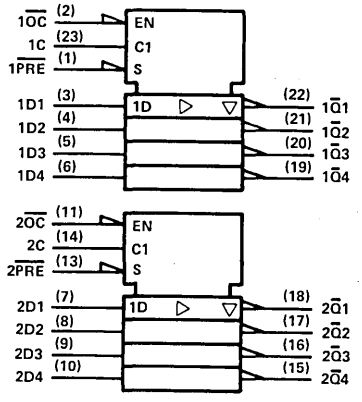
typical performance

TYPE	OUTPUT	DELAY	POWER
'ALS880	$\overline{Q}$	11.5 ns	88 mW

SN54ALS880 (J,FC) SN74ALS880 (JT,NT,FN)
SN54AS880 (J,FC) SN74AS880 (JT,NT,FN)

See *TTL Data Book*

logic symbol†



pin assignments

J, JT, NT PACKAGES		FC, FN PACKAGES	
1 $\overline{1PRE}$	13 $\overline{2PRE}$	1 $\overline{1PRE}$	15 $\overline{2PRE}$
2 $\overline{1OC}$	14 2C	2 $\overline{1OC}$	16 2C
3 1D1	15 $\overline{2Q4}$	3 1D1	17 $\overline{2Q4}$
4 1D2	16 $\overline{2Q3}$	4 1D2	18 $\overline{2Q3}$
5 1D3	17 $\overline{2Q2}$	5 nc	19 nc
6 1D4	18 $\overline{2Q1}$	6 nc	20 nc
7 2D1	19 $\overline{1Q4}$	7 1D3	21 $\overline{2Q2}$
8 2D2	20 $\overline{1Q3}$	8 1D4	22 $\overline{2Q1}$
9 2D3	21 $\overline{1Q2}$	9 2D1	23 $\overline{1Q4}$
10 2D4	22 $\overline{1Q1}$	10 2D2	24 $\overline{1Q3}$
11 $\overline{2OC}$	23 1C	11 2D3	25 $\overline{1Q2}$
12 GND	24 V_{CC}	12 2D4	26 $\overline{1Q1}$
		13 $\overline{2OC}$	27 1C
		14 GND	28 V_{CC}

881

ARITHMETIC LOGIC UNITS/ FUNCTION GENERATORS

- 4-bit ALU's/Function Generators
- Same operating modes as 'AS181, 'S181 expanded to include status register checks

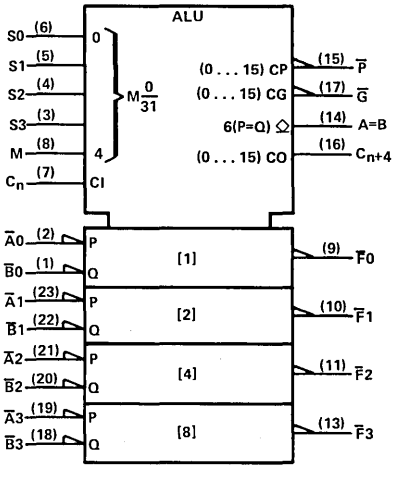
typical performance

TYPE	CARRY TIME	16-BIT ADD TIME	TOTAL POWER
'AS881	7.5 ns	20 ns	560 mW

SN54AS881 (J,FC)

SN74AS881 (JT,NT,FN)

logic symbol†



pin assignments

J, JT, NT PACKAGES		FC, FN PACKAGES	
1 $\overline{B0}$	13 $\overline{F3}$	1 $\overline{B0}$	15 $\overline{F3}$
2 $\overline{A0}$	14 A=B	2 $\overline{A0}$	16 A=B
3 S3	15 $\overline{P}$	3 S3	17 nc
4 S2	16 C_{n+4}	4 nc	18 nc
5 S1	17 $\overline{G}$	5 nc	19 $\overline{P}$
6 S0	18 $\overline{B3}$	6 S2	20 C_{n+4}
7 C_n	19 $\overline{A3}$	7 S1	21 $\overline{G}$
8 M	20 $\overline{B2}$	8 S0	22 $\overline{B3}$
9 $\overline{F0}$	21 $\overline{A2}$	9 C_n	23 $\overline{A3}$
10 $\overline{F1}$	22 $\overline{B1}$	10 M	24 $\overline{B2}$
11 $\overline{F2}$	23 $\overline{A1}$	11 $\overline{F0}$	25 $\overline{A2}$
12 GND	24 V_{CC}	12 $\overline{F1}$	26 $\overline{B1}$
		13 $\overline{F2}$	27 $\overline{A1}$
		14 GND	28 V_{CC}

See *TTL Data Book*

† Pin numbers shown on logic symbols are for J, JT and NT packages only.
nc — no internal connection.

882

32-BIT LOOK-AHEAD CARRY GENERATORS

- Directly compatible with 'AS181, 'AS881, and 'S181 ALU's

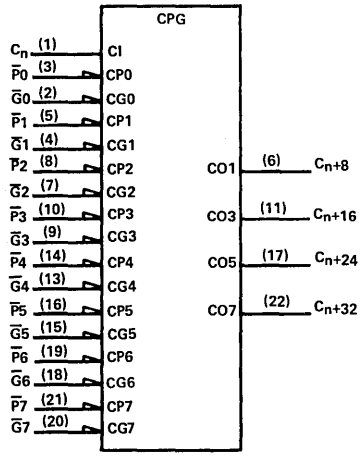
typical performance

TYPE	CARRY TIME	TOTAL POWER
'AS882	8 ns	325 mW

SN54AS882 (J,FC)

SN74AS882 (JT,NT,FN)

logic symbol†



pin assignments

J, JT, NT PACKAGES				FC, FN PACKAGES			
1	C_n	13	$\overline{G}4$	1	C_n	15	$\overline{G}4$
2	$\overline{G}0$	14	$\overline{P}4$	2	$\overline{G}0$	16	$\overline{P}4$
3	$\overline{P}0$	15	$\overline{G}5$	3	$\overline{P}0$	17	$\overline{G}5$
4	$\overline{G}1$	16	$\overline{P}5$	4	$\overline{G}1$	18	$\overline{P}5$
5	$\overline{P}1$	17	C_{n+24}	5	nc	19	nc
6	C_{n+8}	18	$\overline{G}6$	6	nc	20	nc
7	$\overline{G}2$	19	$\overline{P}6$	7	$\overline{P}1$	21	C_{n+24}
8	$\overline{P}2$	20	$\overline{G}7$	8	C_{n+8}	22	$\overline{G}6$
9	$\overline{G}3$	21	$\overline{P}7$	9	$\overline{G}2$	23	$\overline{P}6$
10	$\overline{P}3$	22	C_{n+32}	10	$\overline{P}2$	24	$\overline{G}7$
11	C_{n+16}	23	nc	11	$\overline{G}3$	25	$\overline{P}7$
12	GND	24	V_{CC}	12	$\overline{P}3$	26	C_{n+32}
				13	C_{n+16}	27	nc
				14	GND	28	V_{CC}

See *TTL Data Book*

885

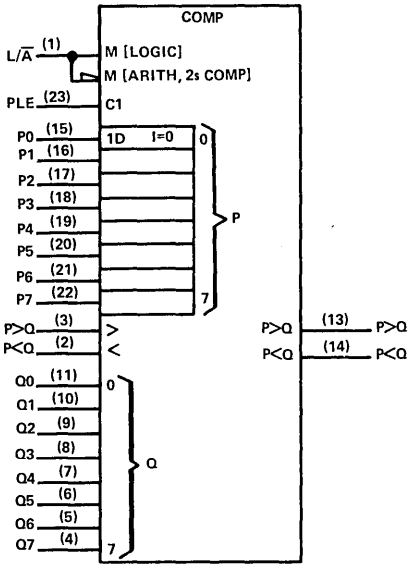
8-BIT MAGNITUDE COMPARATORS

- Choice of logical or arithmetic comparisons
- Latchable P input ports; power clear

SN54AS885 (J,FC)

SN74AS885 (JT,NT,FN)

logic symbol†



pin assignments

J, JT, NT PACKAGES				FC, FN PACKAGES			
1	L/$\overline{A}$	13	P>Qout	1	L/$\overline{A}$	15	P>Qout
2	P<Qin	14	P<Qout	2	P<Qin	16	P<Qout
3	P>Qin	15	P0	3	P>Qin	17	P0
4	Q7	16	P1	4	Q7	18	P1
5	Q6	17	P2	5	nc	19	nc
6	Q5	18	P3	6	nc	20	nc
7	Q4	19	P4	7	Q6	21	P2
8	Q3	20	P5	8	Q5	22	P3
9	Q2	21	P6	9	Q4	23	P4
10	Q1	22	P7	10	Q3	24	P5
11	Q0	23	PLE	11	Q2	25	P6
12	GND	24	V_{CC}	12	Q1	26	P7
				13	Q0	27	PLE
				14	GND	28	V_{CC}

See *TTL Data Book*

† Pin numbers shown on logic symbols are for J, JT and NT packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

894

EXPANDABLE MULTI-FUNCTION BINARY/HEXADECIMAL SCALERS

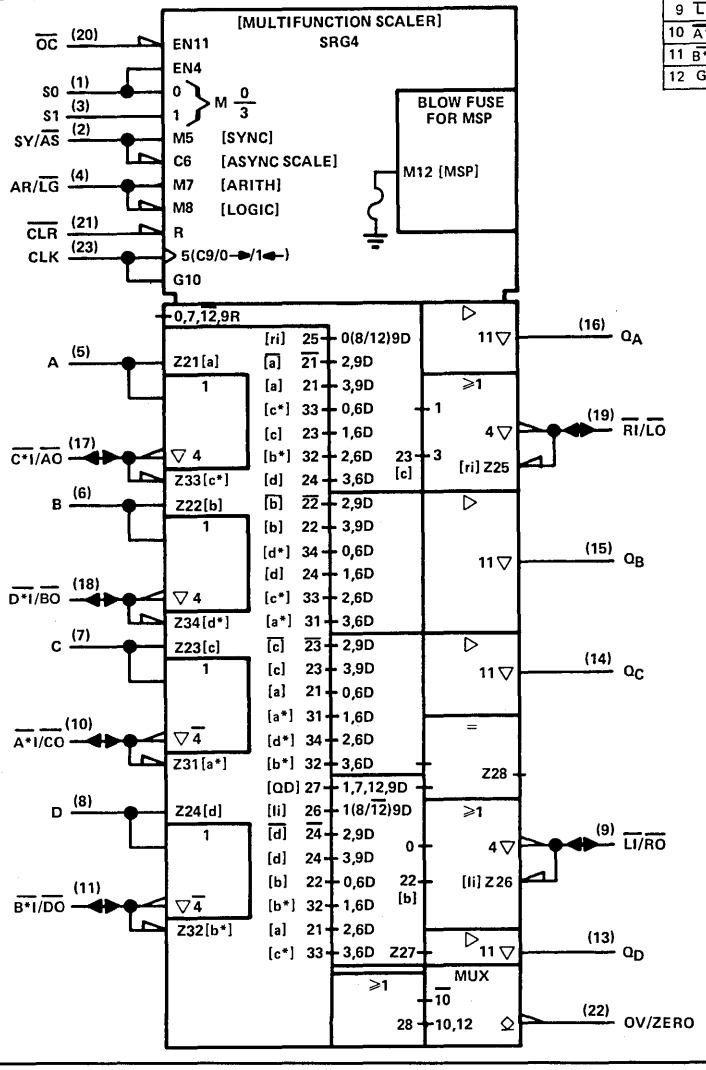
- Buffer-type outputs
- 100 MHz typical shift rate

SN54AS894 (J,FC) SN74AS894 (JT,NT,FN)

pin assignments

J, JT, NT PACKAGES		FC, FN PACKAGES	
1 S0	13 QD	1 S0	15 QD
2 SY/$\overline{AS}$	14 QC	2 SY/$\overline{AS}$	16 QC
3 S1	15 QB	3 S1	17 QB
4 AR/$\overline{LG}$	16 QA	4 AR/$\overline{LG}$	18 QA
5 A	17 $\overline{C*I/AO}$	5 nc	19 nc
6 B	18 $\overline{D*I/BO}$	6 nc	20 nc
7 C	19 $\overline{RI/LO}$	7 A	21 $\overline{C*I/AO}$
8 D	20 $\overline{OC}$	8 B	22 $\overline{D*I/BO}$
9 $\overline{LI/RO}$	21 $\overline{CLR}$	9 C	23 $\overline{RI/LO}$
10 $\overline{A*I/CO}$	22 OV/ZERO	10 D	24 $\overline{OC}$
11 $\overline{B*I/DO}$	23 CLK	11 $\overline{LI/RO}$	25 $\overline{CLR}$
12 GND	24 V_{CC}	12 $\overline{A*I/CO}$	26 OV/ZERO
		13 $\overline{B*I/DO}$	27 CLK
		14 GND	28 V_{CC}

logic symbol†



Since publication of the *1981 Supplement to the TTL Data Book*, several changes in nomenclature have been made. The actual device has not changed. Several pin names have been changed and the shift in the direction Q_A towards Q_D is designated right instead of left.

See *TTL Data Book*

† Pin numbers shown on logic symbols are for J, JT, NT, and N packages only.
nc — no internal connection.

1000

QUAD 2-INPUT NAND GATES

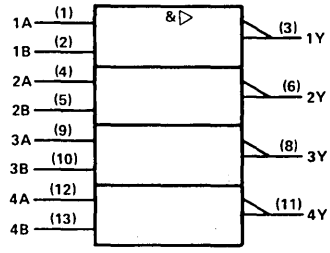
- Increased output drive capability over 'LS00

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT	DELAY	POWER/GATE
SN54ALS1000	12 mA	−1 mA	4 ns	3 mW
SN74ALS1000	24 mA	−2.6 mA	4 ns	3 mW

SN54ALS1000 (J,FC) SN74ALS1000 (J,N,FN)

logic symbol†



positive logic: $Y = \overline{AB}$

pin assignments

J, N PACKAGES	
1 1A	8 3Y
2 1B	9 3A
3 1Y	10 3B
4 2A	11 4Y
5 2B	12 4A
6 2Y	13 4B
7 GND	14 V_{CC}

FC, FN PACKAGES	
1 nc	11 3Y
2 nc	12 nc
3 1A	13 3A
4 1B	14 nc
5 1Y	15 3B
6 2A	16 4Y
7 2B	17 nc
8 nc	18 4A
9 2Y	19 4B
10 GND	20 V_{CC}

See *TTL Data Book*

1002

QUAD 2-INPUT NOR BUFFER GATES

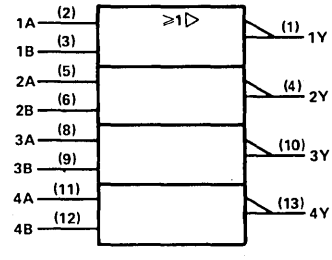
- Increased output drive capability over 'LS02

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT	DELAY	POWER/GATE
SN54ALS1002	12 mA	−1 mA	4 ns	4 mW
SN74ALS1002	24 mA	−2.6 mA	4 ns	4 mW

SN54ALS1002 (J,FC) SN74ALS1002 (J,N,FN)

logic symbol†



positive logic: $Y = \overline{A+B}$

pin assignments

J, N PACKAGES	
1 1Y	8 3A
2 1A	9 3B
3 1B	10 3Y
4 2Y	11 4A
5 2A	12 4B
6 2B	13 4Y
7 GND	14 V_{CC}

FC, FN PACKAGES	
1 nc	11 3A
2 1Y	12 nc
3 nc	13 3B
4 1A	14 nc
5 1B	15 3Y
6 2Y	16 4A
7 2A	17 4B
8 nc	18 nc
9 2B	19 4Y
10 GND	20 V_{CC}

See *TTL Data Book*

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

1003

QUAD 2-INPUT NAND BUFFER GATES WITH OPEN-COLLECTOR OUTPUTS

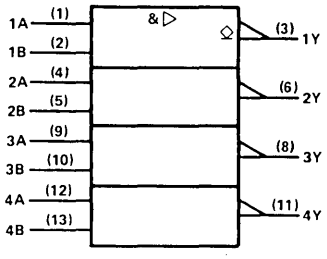
- Increased drive capability over 'LS03

typical performance

TYPE	HIGH-LEVEL OUTPUT VOLTAGE	LOW-LEVEL OUTPUT CURRENT	DELAY	POWER/GATE
SN54ALS1003	5.5 V	12 mA	14.5 ns	3 mW
SN74ALS1003	5.5 V	24 mA	14.5 ns	3 mW

SN54ALS1003 (J,FC) SN74ALS1003 (J,N,FN)

logic symbol†



positive logic: $Y = \overline{AB}$

pin assignments

J, N PACKAGES			
1	1A	8	3Y
2	1B	9	3A
3	1Y	10	3B
4	2A	11	4Y
5	2B	12	4A
6	2Y	13	4B
7	GND	14	V_{CC}

FC, FN PACKAGES			
1	nc	11	3Y
2	nc	12	nc
3	1A	13	3A
4	1B	14	nc
5	1Y	15	3B
6	2A	16	4Y
7	2B	17	nc
8	nc	18	4A
9	2Y	19	4B
10	GND	20	V_{CC}

See *TTL Data Book*

1004

HEX INVERTER BUFFER GATES

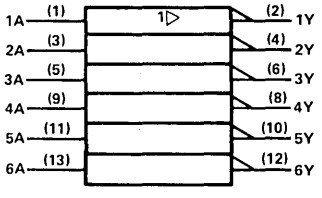
- Functionally and pin-for-pin compatible with TTL counterparts

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT
SN54ALS1004	12 mA	−1 mA
SN74ALS1004	24 mA	−2.6 mA

SN54ALS1004 (J,FC) SN74ALS1004 (J,N,FN) See *TTL Data Book*

logic symbol†



positive logic: $Y = \overline{A}$

pin assignments

J, N PACKAGES			
1	1A	8	4Y
2	1Y	9	4A
3	2A	10	5Y
4	2Y	11	5A
5	3A	12	6Y
6	3Y	13	6A
7	GND	14	V_{CC}

FC, FN PACKAGES			
1	1A	11	nc
2	nc	12	4Y
3	nc	13	nc
4	1Y	14	4A
5	2A	15	5Y
6	2Y	16	5A
7	3A	17	6Y
8	nc	18	nc
9	3Y	19	6A
10	GND	20	V_{CC}

1005

HEX INVERTER BUFFER GATES WITH OPEN-COLLECTOR OUTPUTS

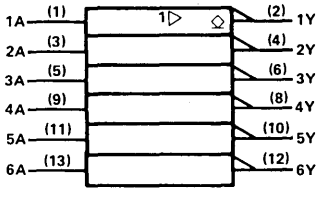
- Functionally and pin-for-pin compatible with TTL counterparts

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT
SN54ALS1005	12 mA	−1 mA
SN74ALS1005	24 mA	−2.6 mA

SN54ALS1005 (J,FC) SN74ALS1005 (J,N,FN) See *TTL Data Book*

logic symbol†



positive logic: $Y = \overline{A}$

pin assignments

J, N PACKAGES			
1	1A	8	4Y
2	1Y	9	4A
3	2A	10	5Y
4	2Y	11	5A
5	3A	12	6Y
6	3Y	13	6A
7	GND	14	V_{CC}

FC, FN PACKAGES			
1	1A	11	nc
2	nc	12	4Y
3	nc	13	nc
4	1Y	14	4A
5	2A	15	5Y
6	2Y	16	5A
7	3A	17	6Y
8	nc	18	nc
9	3Y	19	6A
10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

1008

QUADRUPLE 2-INPUT POSITIVE-AND BUFFER GATES

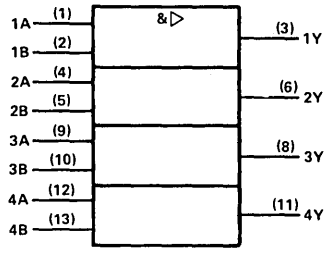
- Functionally and pin-for-pin compatible with TTL counterparts

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT
SN54ALS1008	12 mA	−1 mA
SN74ALS1008	24 mA	−2.6 mA

SN54ALS1008 (J,FC) SN74ALS1008 (J,N,FN)

logic symbol†



positive logic: Y = AB

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 1A	8 3Y	1 nc	11 3Y
2 1B	9 3A	2 nc	12 nc
3 1Y	10 3B	3 1A	13 3A
4 2A	11 4Y	4 1B	14 nc
5 2B	12 4A	5 1Y	15 3B
6 2Y	13 4B	6 2A	16 4Y
7 GND	14 V_{CC}	7 2B	17 nc
		8 nc	18 4A
		9 2Y	19 4B
		10 GND	20 V_{CC}

See *TTL Data Book*

1010

TRIPLE 3-INPUT POSITIVE-NAND BUFFER GATES

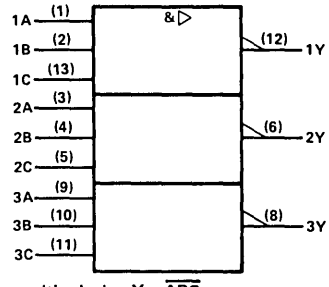
- Functionally and pin-for-pin compatible with TTL counterparts

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT
SN54ALS1010	12 mA	−1 mA
SN74ALS1010	24 mA	−2.6 mA

SN54ALS1010 (J,FC) SN74ALS1010 (J,N,FN)

logic symbol†



positive logic: $Y = \overline{ABC}$

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 1A	8 3Y	1 1A	11 nc
2 1B	9 3A	2 nc	12 3Y
3 2A	10 3B	3 nc	13 nc
4 2B	11 3C	4 1B	14 nc
5 2C	12 1Y	5 2A	15 3A
6 2Y	13 1C	6 2B	16 3B
7 GND	14 V_{CC}	7 2C	17 3C
		8 nc	18 1Y
		9 2Y	19 1C
		10 GND	20 V_{CC}

See *TTL Data Book*

1011

TRIPLE 3-INPUT POSITIVE-AND BUFFER GATES

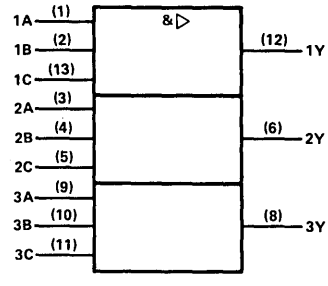
- Functionally and pin-for-pin compatible with TTL counterparts

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT
SN54ALS1011	12 mA	−1 mA
SN74ALS1011	24 mA	−2.6 mA

SN54ALS1011 (J,FC) SN74ALS1011 (J,N,FN)

logic symbol†



positive logic: Y = ABC

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 1A	8 3Y	1 1A	11 nc
2 1B	9 3A	2 nc	12 3Y
3 2A	10 3B	3 nc	13 nc
4 2B	11 3C	4 1B	14 nc
5 2C	12 1Y	5 2A	15 3A
6 2Y	13 1C	6 2B	16 3B
7 GND	14 V_{CC}	7 2C	17 3C
		8 nc	18 1Y
		9 2Y	19 1C
		10 GND	20 V_{CC}

See *TTL Data Book*

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

1020

DUAL 4-INPUT NAND BUFFER GATES

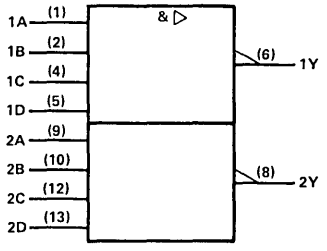
- Functionally and pin-for-pin compatible with TTL counterparts

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT
SN54ALS1020	12 mA	−1 mA
SN74ALS1020	24 mA	−2.6 mA

SN54ALS1020 (J,FC) SN74ALS1020 (J,N,FN)

logic symbol†



positive logic: $Y = \overline{ABCD}$

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 1A	8 2Y	1 nc	11 nc
2 1B	9 2A	2 nc	12 2Y
3 nc	10 2B	3 1A	13 nc
4 1C	11 nc	4 nc	14 nc
5 1D	12 2C	5 1B	15 2A
6 1Y	13 2D	6 1C	16 2B
7 GND	14 V_{CC}	7 1D	17 2C
		8 nc	18 nc
		9 1Y	19 2D
		10 GND	20 V_{CC}

See *TTL Data Book*

1032

QUADRUPLE 2-INPUT POSITIVE-OR BUFFER GATE

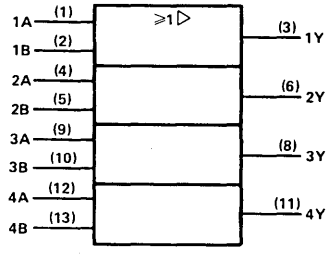
- Functionally and pin-for-pin compatible with TTL counterparts

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT
SN54ALS1032	12 mA	−1 mA
SN74ALS1032	24 mA	−2.6 mA

SN54ALS1032 (J,FC) SN74ALS1032 (J,N,FN)

logic symbol†



positive logic: A+B

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 1A	8 3Y	1 nc	11 3Y
2 1B	9 3A	2 nc	12 nc
3 1Y	10 3B	3 1A	13 3A
4 2A	11 4Y	4 1B	14 nc
5 2B	12 4A	5 1Y	15 3B
6 2Y	13 4B	6 2A	16 4Y
7 GND	14 V_{CC}	7 2B	17 nc
		8 nc	18 4A
		9 2Y	19 4B
		10 GND	20 V_{CC}

See *TTL Data Book*

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

8

FP'ALS16L8

FIELD-PROGRAMMABLE LOGIC, FIXED-OR ARRAYS

typical performance

TYPE	DELAY	TOTAL POWER
'ALS16L8	12 ns	550 mW

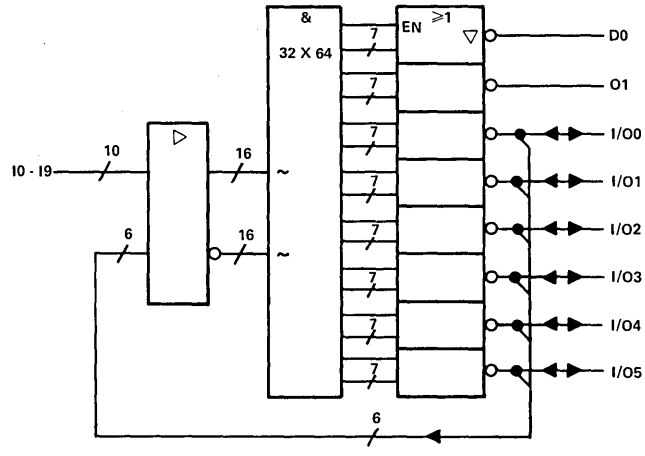
- Octal 16-input AND-OR-INVERT gate array

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	I0	11	I9	1	I0	11	I9
2	I1	12	O1	2	I1	12	O1
3	I2	13	I/O5	3	I2	13	I/O5
4	I3	14	I/O4	4	I3	14	I/O4
5	I4	15	I/O3	5	I4	15	I/O3
6	I5	16	I/O2	6	I5	16	I/O2
7	I6	17	I/O1	7	I6	17	I/O1
8	I7	18	I/O0	8	I7	18	I/O0
9	I8	19	O0	9	I8	19	O0
10	GND	20	V_{CC}	10	GND	20	V_{CC}

FP54ALS16L8 (J,FC) FP74ALS16L8 (J,N,FN)

functional block diagram



See Page 5-3

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

FP'ALS16R4

FIELD-PROGRAMMABLE LOGIC, FIXED-OR ARRAYS

typical performance

TYPE	DELAY	TOTAL POWER
'ALS16R4	12 ns	575 mW

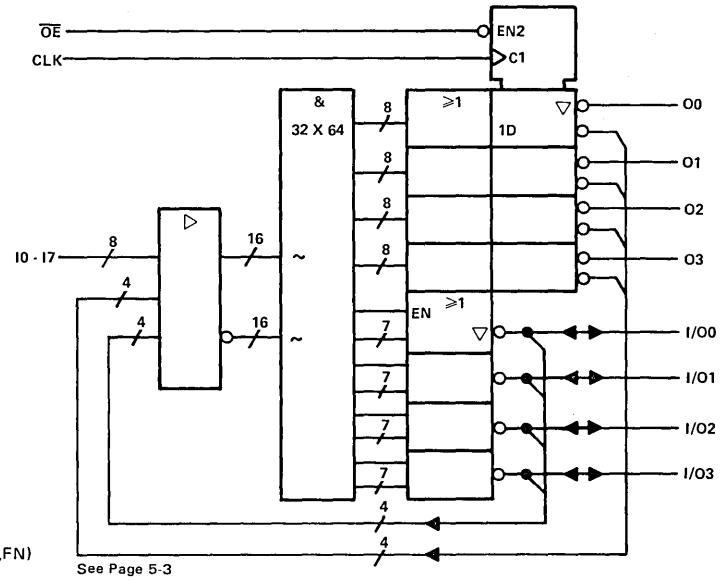
- Quad 16-input registered AND-OR gate array

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	CLK	11	$\overline{OE}$	1	CLK	11	$\overline{OE}$
2	I0	12	I/O3	2	I0	12	I/O3
3	I1	13	I/O2	3	I1	13	I/O2
4	I2	14	O3	4	I2	14	O3
5	I3	15	O2	5	I3	15	O2
6	I4	16	O1	6	I4	16	O1
7	I5	17	O0	7	I5	17	O0
8	I6	18	I/O1	8	I6	18	I/O1
9	I7	19	I/O0	9	I7	19	I/O0
10	GND	20	V_{CC}	10	GND	20	V_{CC}

FP54ALS16R4 (J,FC) FP74ALSR4 (J,N,FN)

functional block diagram



See Page 5-3

FP'ALS16R6

FIELD-PROGRAMMABLE LOGIC, FIXED-OR ARRAYS

typical performance

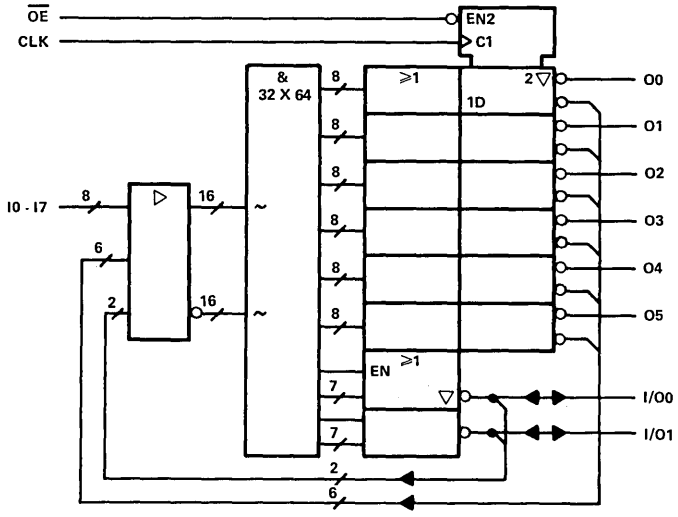
TYPE	DELAY	TOTAL POWER
'ALS16R6	12 ns	575 mW

- Hex 16-input registered AND-OR gate array

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 CLK	11 $\overline{OE}$	1 CLK	11 $\overline{OE}$
2 I0	12 I/O1	2 I0	12 I/O1
3 I1	13 O5	3 I1	13 O5
4 I2	14 O4	4 I2	14 O4
5 I3	15 O3	5 I3	15 O3
6 I4	16 O2	6 I4	16 O2
7 I5	17 O1	7 I5	17 O1
8 I6	18 O0	8 I6	18 O0
9 I7	19 I/O0	9 I7	19 I/O0
10 GND	20 V_{CC}	10 GND	20 V_{CC}

functional block diagram



See Page 5-3

FP54ALS16R6 (J,FC) FP74ALS16R6 (J,N,FN)

~ denotes fused inputs.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

FP'ALS16R8

FIELD-PROGRAMMABLE LOGIC, FIXED-OR ARRAYS

typical performance

TYPE	DELAY	TOTAL POWER
'ALS16R8	12 ns	575 mW

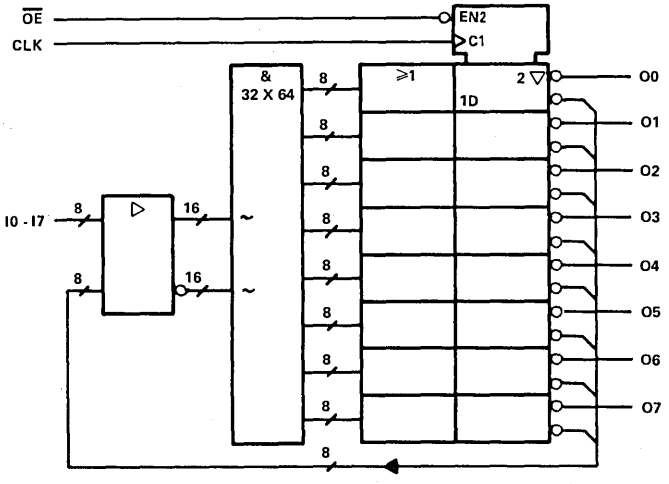
- Octal 16-input registered AND-OR gate array

pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	CLK	11	$\overline{OE}$	1	CLK	11	$\overline{OE}$
2	I0	12	O7	2	I0	12	O7
3	I1	13	O6	3	I1	13	O6
4	I2	14	O5	4	I2	14	O5
5	I3	15	O4	5	I3	15	O4
6	I4	16	O3	6	I4	16	O3
7	I5	17	O2	7	I5	17	O2
8	I6	18	O1	8	I6	18	O1
9	I7	19	O0	9	I7	19	O0
10	GND	20	V_{CC}	10	GND	20	V_{CC}

FP54ALS16R8 (J,FC) FP74ALS16R8 (J,N,FN)

functional block diagram



See Page 5-3

~ denotes fused inputs.

8

FP'LS333, FP'LS335

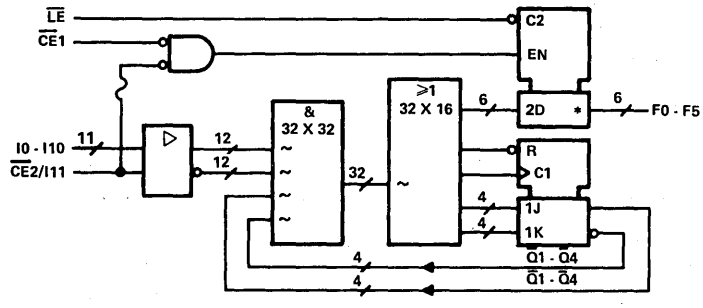
FIELD-PROGRAMMABLE LOGIC SEQUENCERS

typical performance

TYPE	DELAY	TOTAL POWER
'LS333	45 ns	350 mW
'LS335	45 ns	350 mW

- FP'LS333 — three-state outputs
- FP'LS335 — open-collector outputs
- 12 input variables
- 32 product terms
- 6-bit output latch
- 4-bit state register

functional block diagram



~ denotes fused inputs.

* 'LS333 has 3-state (▽) outputs; 'LS335 has open-collector (◇) outputs.

pin assignments

J, JT, NT PACKAGES				FC, FN PACKAGES			
1	I8	13	F2	1	nc	15	nc
2	I7	14	F3	2	I8	16	F2
3	I6	15	F4	3	I7	17	F3
4	I5	16	F5	4	I6	18	F4
5	I4	17	$\overline{CE1}$	5	I5	19	F5
6	I3	18	$\overline{LE}$	6	I4	20	$\overline{CE1}$
7	I2	19	PM	7	I3	21	$\overline{LE}$
8	I1	20	PL	8	I2	22	PM
9	I0	21	I11/$\overline{CE2}$	9	I1	23	PL
10	F0	22	I10	10	I0	24	I11/$\overline{CE2}$
11	F1	23	I9	11	F0	25	I10
12	GND	24	V_{CC}	12	F1	26	I9
				13	nc	27	nc
				14	GND	28	V_{CC}

FP54LS333 (J,FC) FP74LS333 (JT,NT,FN)
FP54LS335 (J,FC) FP74LS335 (JT,NT,FN)

See Page 5-12

nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

FP'AS839, FP'AS840

FIELD-PROGRAMMABLE LOGIC ARRAYS

typical performance

TYPE	DELAY	TOTAL POWER
'AS839	10 ns	725 mW
'AS840	10 ns	725 mW

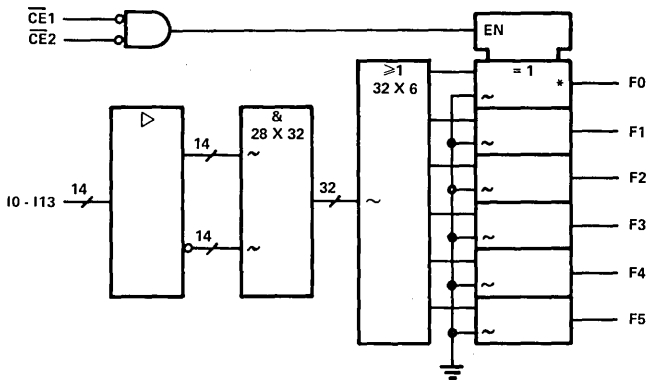
- FP'AS839 – three-state outputs
- FP'AS840 – open-collector outputs
- Programmable output polarity

pin assignments

J, JT, NT PACKAGES				FC, FN PACKAGES			
1	$\overline{CE1}$/FE	13	$\overline{CE2}$	1	nc	15	nc
2	I6	14	F2	2	$\overline{CE1}$/FE	16	$\overline{CE2}$
3	I5	15	F1	3	I6	17	F2
4	I4	16	F0	4	I5	18	F1
5	I3	17	I13	5	I4	19	F0
6	I2	18	I12	6	I3	20	I13
7	I1	19	I11	7	I2	21	I12
8	I0	20	I10	8	I1	22	I11
9	F5	21	I9	9	I0	23	I10
10	F4	22	I8	10	F5	24	I9
11	F3	23	I7	11	F4	25	I8
12	GND	24	V_{CC}	12	F3	26	I7
				13	nc	27	nc
				14	GND	28	V_{CC}

FP54AS839 (J,FC) FP74AS839 (JT,NT,FN)
FP54AS840 (J,FC) FP74AS840 (JT,NT,FN)

functional block diagram



~ denotes fused inputs.

* 'AS839 has 3-state (▽) outputs; 'AS840 has open-collector (◇) outputs.

See Page 5-16

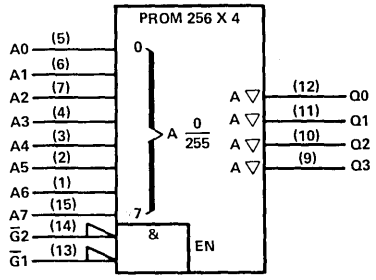
nc – no internal connection.

TBP14S10 ('S287)

PROGRAMMABLE READ-ONLY MEMORIES

- 256 X 4
- Three-state outputs
- Typical address access time . . . 42 ns
- Typical power . . . 500 mW

logic symbol†



pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	A6	9	Q3	1	nc	11	nc
2	A5	10	Q2	2	A6	12	Q3
3	A4	11	Q1	3	A5	13	Q2
4	A3	12	Q0	4	A4	14	Q1
5	A0	13	$\overline{G}1$	5	A3	15	nc
6	A1	14	$\overline{G}2$	6	A0	16	Q0
7	A2	15	A7	7	A1	17	$\overline{G}1$
8	GND	16	V_{CC}	8	A2	18	$\overline{G}2$
				9	nc	19	A7
				10	GND	20	V_{CC}

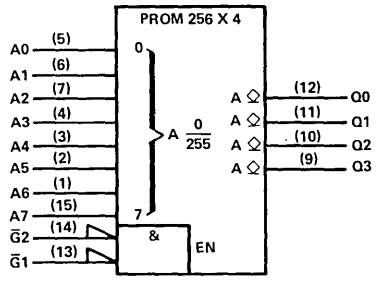
See Page 2-7

TBP14SA10 ('S387)

PROGRAMMABLE READ-ONLY MEMORIES

- 256 X 4
- Open-collector outputs
- Typical address access time . . . 42 ns
- Typical power . . . 500 mW

logic symbol†



pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	A6	9	Q3	1	nc	11	nc
2	A5	10	Q2	2	A6	12	Q3
3	A4	11	Q1	3	A5	13	Q2
4	A3	12	Q0	4	A4	14	Q1
5	A0	13	$\overline{G}1$	5	A3	15	nc
6	A1	14	$\overline{G}2$	6	A0	16	Q0
7	A2	15	A7	7	A1	17	$\overline{G}1$
8	GND	16	V_{CC}	8	A2	18	$\overline{G}2$
				9	nc	19	A7
				10	GND	20	V_{CC}

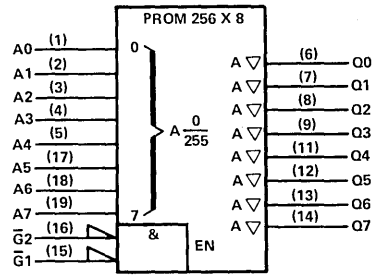
See Page 2-7

TBP18S22 ('S471)

PROGRAMMABLE READ-ONLY MEMORIES

- 256 X 8
- Three-state outputs
- Typical address access time . . . 50 ns
- Typical power . . . 550 mW

logic symbol†



pin assignments

J, N PACKAGES			
1	A0	11	Q4
2	A1	12	Q5
3	A2	13	Q6
4	A3	14	Q7
5	A4	15	$\overline{G}1$
6	Q0	16	$\overline{G}2$
7	Q1	17	A5
8	Q2	18	A6
9	Q3	19	A7
10	GND	20	V_{CC}

For chip carrier options and information, contact the factory.

See Page 2-7

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

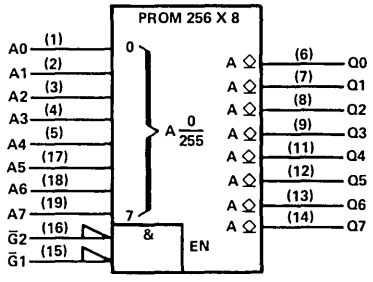
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TBP18SA22 ('S470)

PROGRAMMABLE READ-ONLY MEMORIES

- 256 X 8
- Open-collector outputs
- Typical address access time . . . 50 ns
- Typical power . . . 550 mW

logic symbol†



pin assignments

J, N PACKAGES			
1	A0	11	Q4
2	A1	12	Q5
3	A2	13	Q6
4	A3	14	Q7
5	A4	15	$\overline{G}1$
6	Q0	16	$\overline{G}2$
7	Q1	17	A5
8	Q2	18	A6
9	Q3	19	A7
10	GND	20	V_{CC}

For chip carrier options and information, contact the factory.

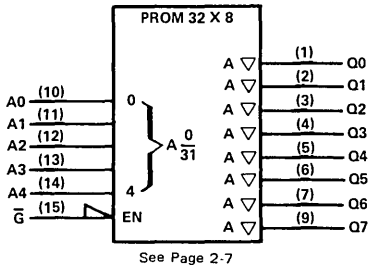
See Page 2-7

TBP18S030 ('S288)

PROGRAMMABLE READ-ONLY MEMORIES

- 32 X 8
- Three-state outputs
- Typical address access time . . . 25 ns
- Typical power . . . 400 mW

logic symbol†



pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	Q0	9	Q7	1	Q0	11	Q7
2	Q1	10	A0	2	Q1	12	A0
3	Q2	11	A1	3	nc	13	nc
4	Q3	12	A2	4	Q2	14	A1
5	Q4	13	A3	5	Q3	15	A2
6	Q5	14	A4	6	Q4	16	A3
7	Q6	15	$\overline{G}$	7	Q5	17	A4
8	GND	16	V_{CC}	8	nc	18	nc
				9	Q6	19	$\overline{G}$
				10	GND	20	V_{CC}

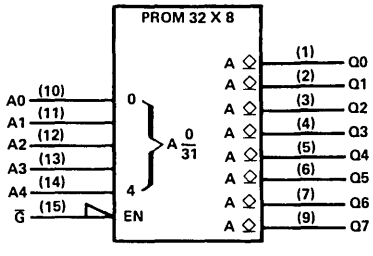
See Page 2-7

TBP18SA030 ('S188)

PROGRAMMABLE READ-ONLY MEMORIES

- 32 X 8
- Open-collector outputs
- Typical address access time . . . 25 ns
- Typical power . . . 400 mW

logic symbol†



pin assignments

J, N PACKAGES				FC, FN PACKAGES			
1	Q0	9	Q7	1	Q0	11	Q7
2	Q1	10	A0	2	Q1	12	A0
3	Q2	11	A1	3	nc	13	nc
4	Q3	12	A2	4	Q2	14	A1
5	Q4	13	A3	5	Q3	15	A2
6	Q5	14	A4	6	Q4	16	A3
7	Q6	15	$\overline{G}$	7	Q5	17	A4
8	GND	16	V_{CC}	8	nc	18	nc
				9	Q6	19	$\overline{G}$
				10	GND	20	V_{CC}

See Page 2-7

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

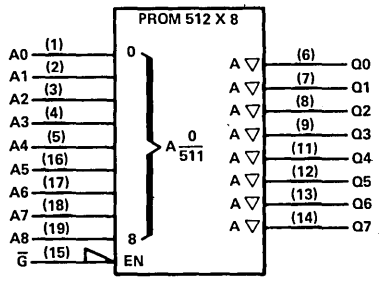
8

TBP18S42 ('S472)

PROGRAMMABLE READ-ONLY MEMORIES

- 512 X 8
- Three-state outputs
- Typical address access time . . . 55 ns
- Typical power . . . 600 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A0	11 Q4
2 A1	12 Q5
3 A2	13 Q6
4 A3	14 Q7
5 A4	15 $\overline{G}$
6 Q0	16 A5
7 Q1	17 A6
8 Q2	18 A7
9 Q3	19 A8
10 GND	20 V_{CC}

For chip carrier options and information, contact the factory.

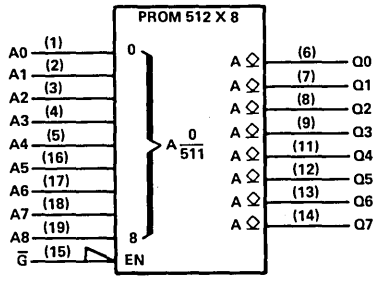
See Page 2-7

TBP18SA42 ('S473)

PROGRAMMABLE READ-ONLY MEMORIES

- 512 X 8
- Open-collector outputs
- Typical address access time . . . 55 ns
- Typical power . . . 600 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A0	11 Q4
2 A1	12 Q5
3 A2	13 Q6
4 A3	14 Q7
5 A4	15 $\overline{G}$
6 Q0	16 A5
7 Q1	17 A6
8 Q2	18 A7
9 Q3	19 A8
10 GND	20 V_{CC}

For chip carrier options and information, contact the factory.

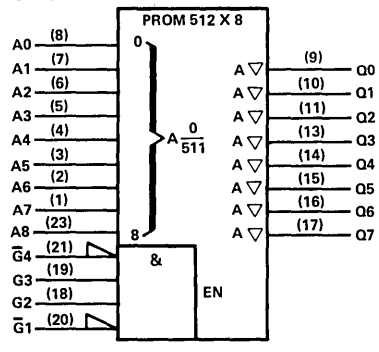
See Page 2-7

TBP18S46 ('S474)

PROGRAMMABLE READ-ONLY MEMORIES

- 512 X 8
- Three-state outputs
- Typical address access time . . . 55 ns
- Typical power . . . 600 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 G2
7 A1	19 G3
8 A0	20 $\overline{G1}$
9 Q0	21 $\overline{G4}$
10 Q1	22 nc
11 Q2	23 A8
12 GND	24 V_{CC}

For chip carrier options and information, contact the factory.

See Page 2-7

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

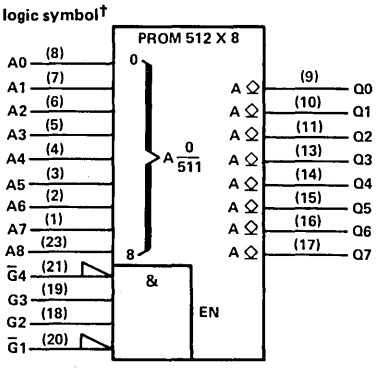
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TBP18SA46 ('S475)

PROGRAMMABLE READ-ONLY MEMORIES

- 512 X 8
- Open-collector outputs
- Typical address access time . . . 55 ns
- Typical power . . . 600 mW

logic symbol†



See Page 2-7

pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 G2
7 A1	19 G3
8 A0	20 $\overline{G}1$
9 Q0	21 $\overline{G}4$
10 Q1	22 nc
11 Q2	23 A8
12 GND	24 V_{CC}

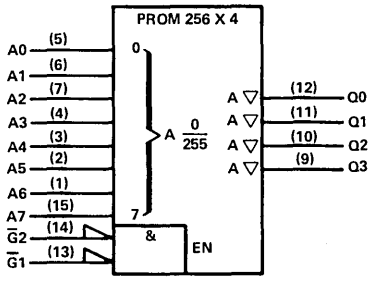
For chip carrier options and information, contact the factory.

TBP24S10

PROGRAMMABLE READ-ONLY MEMORIES

- 256 X 4
- Three-state outputs
- Typical address access time . . . 35 ns
- Typical select time . . . 20 ns
- Typical power . . . 375 mW

logic symbol†



See Page 2-13

pin assignments

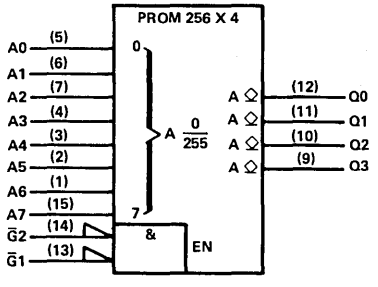
J, N PACKAGES		FC, FN PACKAGES	
1 A6	9 Q3	1 nc	11 nc
2 A5	10 Q2	2 A6	12 Q3
3 A4	11 Q1	3 A5	13 Q2
4 A3	12 Q0	4 A4	14 Q1
5 A0	13 $\overline{G}1$	5 A3	15 nc
6 A1	14 $\overline{G}2$	6 A0	16 Q0
7 A2	15 A7	7 A1	17 $\overline{G}1$
8 GND	16 V_{CC}	8 A2	18 $\overline{G}2$
		9 nc	19 A7
		10 GND	20 V_{CC}

TBP24SA10

PROGRAMMABLE READ-ONLY MEMORIES

- 256 X 4
- Open-collector outputs
- Typical address access time . . . 35 ns
- Typical select time . . . 20 ns
- Typical power . . . 375 mW

logic symbol†



See Page 2-13

pin assignments

J, N PACKAGES		FC, FN PACKAGES	
1 A6	9 Q3	1 nc	11 nc
2 A5	10 Q2	2 A6	12 Q3
3 A4	11 Q1	3 A5	13 Q2
4 A3	12 Q0	4 A4	14 Q1
5 A0	13 $\overline{G}1$	5 A3	15 nc
6 A1	14 $\overline{G}2$	6 A0	16 Q0
7 A2	15 A7	7 A1	17 $\overline{G}1$
8 GND	16 V_{CC}	8 A2	18 $\overline{G}2$
		9 nc	19 A7
		10 GND	20 V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

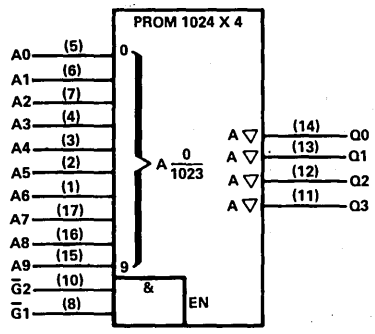
TBP24S41 ('S476)

PROGRAMMABLE READ-ONLY MEMORIES

- 1024 X 4
- Three-state outputs
- Typical address access time . . . 40 ns
- Typical select time . . . 20 ns
- Typical power . . . 475 mW

See Page 2-13

logic symbol†



pin assignments

J, N PACKAGES	
1 A6	10 $\overline{G2}$
2 A5	11 Q3
3 A4	12 Q2
4 A3	13 Q1
5 A0	14 Q0
6 A1	15 A9
7 A2	16 A8
8 $\overline{G1}$	17 A7
9 GND	18 V_{CC}

For chip carrier options and information, contact the factory.

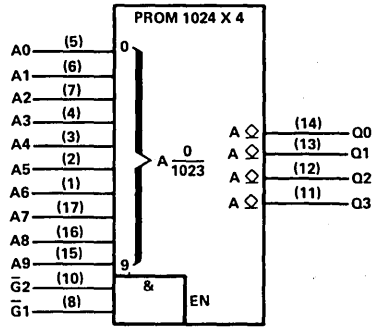
TBP24SA41 ('S477)

PROGRAMMABLE READ-ONLY MEMORIES

- 1024 X 4
- Open-collector outputs
- Typical address access time . . . 40 ns
- Typical select time . . . 20 ns
- Typical power . . . 475 mW

See Page 2-13

logic symbol†



pin assignments

J, N PACKAGES	
1 A6	10 $\overline{G2}$
2 A5	11 Q3
3 A4	12 Q2
4 A3	13 Q1
5 A0	14 Q0
6 A1	15 A9
7 A2	16 A8
8 $\overline{G1}$	17 A7
9 GND	18 V_{CC}

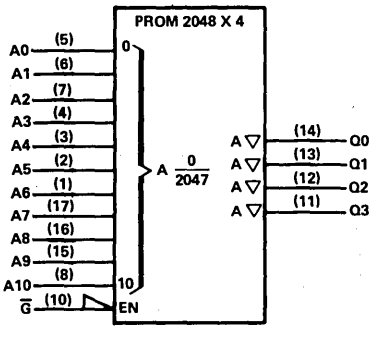
For chip carrier options and information, contact the factory.

TBP24S81 ('S454)
TBP24S81-55

PROGRAMMABLE READ-ONLY MEMORIES

- 2048 X 4
- Three-state outputs
- Typical address access time . . . 45 ns
- TBP24S81-55 maximum address access time . . . 55 ns
- Typical select time . . . 20 ns
- Typical power . . . 625 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A6	10 $\overline{G}$
2 A5	11 Q3
3 A4	12 Q2
4 A3	13 Q1
5 A0	14 Q0
6 A1	15 A9
7 A2	16 A8
8 A10	17 A7
9 GND	18 V_{CC}

For chip carrier options and information, contact the factory.

See Page 2-13

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

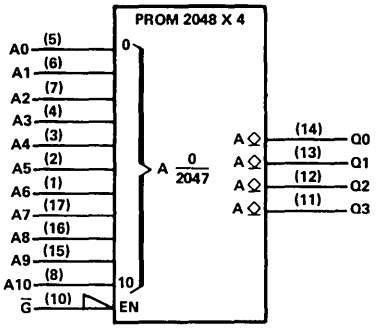
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TBP24SA81 ('S455)
TBP24SA81-55

PROGRAMMABLE READ-ONLY MEMORIES

- 2048 X 4
- Open-collector outputs
- Typical address access time . . . 45 ns
- TBP24SA81-55 maximum address access time . . . 55 ns
- Typical select time . . . 20 ns
- Typical power . . . 625 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A6	10 $\overline{G}$
2 A5	11 Q3
3 A4	12 Q2
4 A3	13 Q1
5 A0	14 Q0
6 A1	15 A9
7 A2	16 A8
8 A10	17 A7
9 GND	18 V_{CC}

For chip carrier options and information, contact the factory.

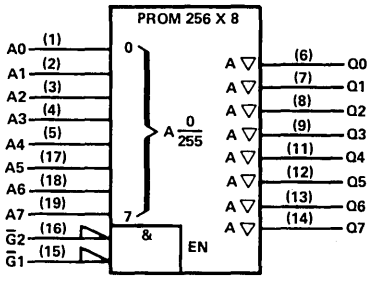
See Page 2-13

TBP28L22

LOW-POWER PROGRAMMABLE READ-ONLY MEMORIES

- 256 X 8
- Three-state outputs
- Typical address access time . . . 45 ns
- Typical select time . . . 20 ns
- Typical power . . . 375 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A0	11 Q4
2 A1	12 Q5
3 A2	13 Q6
4 A3	14 Q7
5 A4	15 $\overline{G1}$
6 Q0	16 $\overline{G2}$
7 Q1	17 A5
8 Q2	18 A6
9 Q3	19 A7
10 GND	20 V_{CC}

For chip carrier options and information, contact the factory.

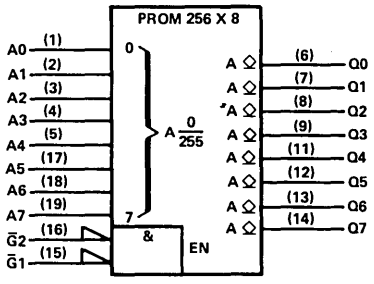
See Page 2-13

TBP28LA22

LOW-POWER PROGRAMMABLE READ-ONLY MEMORIES

- 256 X 8
- Open-collector outputs
- Typical address access time . . . 45 ns
- Typical select time . . . 20 ns
- Typical power . . . 375 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A0	11 Q4
2 A1	12 Q5
3 A2	13 Q6
4 A3	14 Q7
5 A4	15 $\overline{G1}$
6 Q0	16 $\overline{G2}$
7 Q1	17 A5
8 Q2	18 A6
9 Q3	19 A7
10 GND	20 V_{CC}

For chip carrier options and information, contact the factory.

See Page 2-13

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

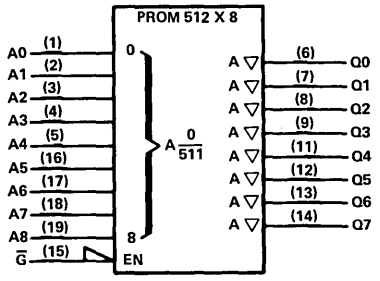
8

TBP28L42

LOW-POWER PROGRAMMABLE READ-ONLY MEMORIES

- 512 X 8
- Three-state outputs
- Typical address access time . . . 60 ns
- Typical select time . . . 30 ns
- Typical power . . . 250 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A0	11 Q4
2 A1	12 Q5
3 A2	13 Q6
4 A3	14 $\overline{G}$
5 A4	15 Q7
6 Q0	16 A5
7 Q1	17 A6
8 Q2	18 A7
9 Q3	19 A8
10 GND	20 V_{CC}

For chip carrier options and information, contact the factory.

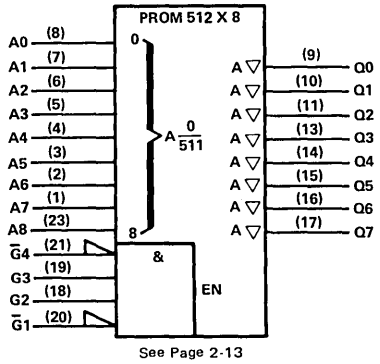
See Page 2-13

TBP28L45
TBP28L46

LOW-POWER PROGRAMMABLE READ-ONLY MEMORIES

- 512 X 8
- Three-state outputs
- Typical address access time . . . 60 ns
- Typical select time . . . 30 ns
- Typical power . . . 250 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 G2
7 A1	19 G3
8 A0	20 $\overline{G}$1
9 Q0	21 $\overline{G}$4
10 Q1	22 nc
11 Q2	23 A8
12 GND	24 V_{CC}

For chip carrier options and information, contact the factory.

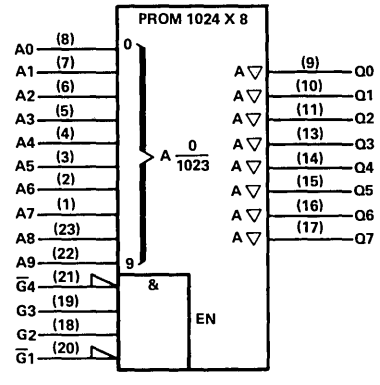
See Page 2-13

TBP28L85

LOW-POWER PROGRAMMABLE READ-ONLY MEMORIES

- 1024 X 8
- Three-state outputs
- Typical address access time . . . 65 ns
- Typical select time . . . 30 ns
- Typical power . . . 275 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 G2
7 A1	19 G3
8 A0	20 $\overline{G}$1
9 Q0	21 $\overline{G}$4
10 Q1	22 A9
11 Q2	23 A8
12 GND	24 V_{CC}

For chip carrier options and information, contact the factory.

See Page 2-13

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

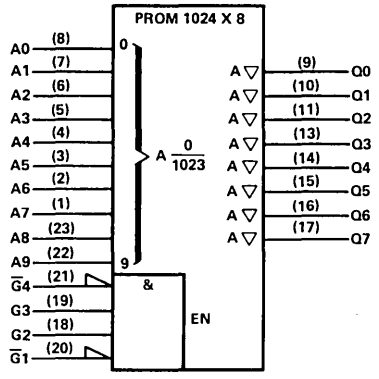
TBP28L86 ('LS478)

LOW-POWER PROGRAMMABLE READ-ONLY MEMORIES

- 1024 X 8
- Three-state outputs
- Typical address access address time . . . 80 ns
- Typical select time . . . 35 ns
- Typical power . . . 350 mW

See Page 2-13

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 G2
7 A1	19 G3
8 A0	20 $\overline{G}$1
9 Q0	21 $\overline{G}$4
10 Q1	22 A9
11 Q2	23 A8
12 GND	24 V_{CC}

For chip carrier options and information, contact the factory.

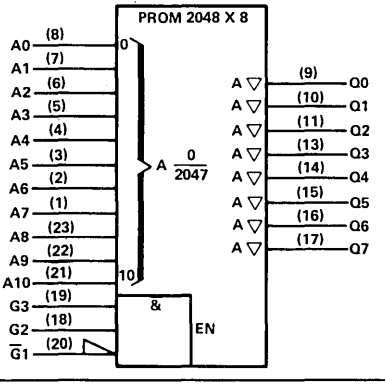
TBP28L166

LOW-POWER PROGRAMMABLE READ-ONLY MEMORIES

- 2048 X 8
- Three-state outputs
- Typical address access time . . . 65 ns
- Typical select time . . . 30 ns
- Typical power . . . 350 mW

See Page 2-13

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 G2
7 A1	19 G3
8 A0	20 $\overline{G}$1
9 Q0	21 A10
10 Q1	22 A9
11 Q2	23 A8
12 GND	24 V_{CC}

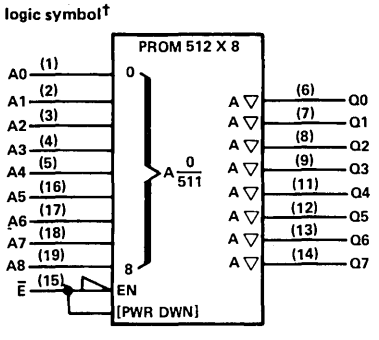
For chip carrier options and information, contact the factory.

TBP28P42

POWER-DOWN PROGRAMMABLE READ-ONLY MEMORIES

- 512 X 8
- Three-state outputs
- Typical address access time . . . 35 ns
- Typical select time . . . 55 ns
- Typical power . . . 500/60 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A0	11 Q4
2 A1	12 Q5
3 A2	13 Q6
4 A3	14 Q7
5 A4	15 $\overline{E}$
6 Q0	16 A5
7 Q1	17 A6
8 Q2	18 A7
9 Q3	19 A8
10 GND	20 V_{CC}

For chip carrier options and information, contact the factory.

See Page 2-13

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

8

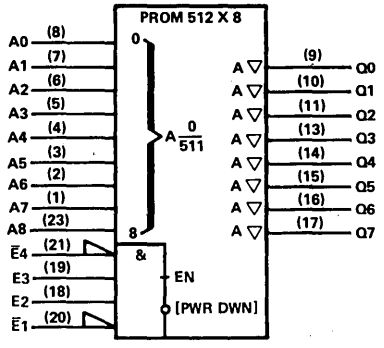
TBP28P45

POWER-DOWN PROGRAMMABLE READ-ONLY MEMORIES

- 512 X 8
- Three-state outputs
- Multiple enables
- Typical address access time . . . 35 ns
- Typical select time . . . 55 ns
- Typical power . . . 500/60 mW

See Page 2-13

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 E2
7 A1	19 E3
8 A0	20 $\overline{E1}$
9 Q0	21 $\overline{E4}$
10 Q1	22 nc
11 Q2	23 A8
12 GND	24 V_{CC}

For chip carrier options and information, contact the factory.

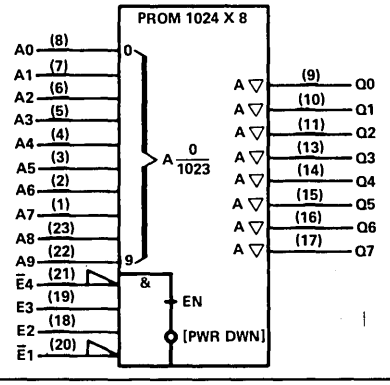
TBP28P85

POWER-DOWN PROGRAMMABLE READ-ONLY MEMORIES

- 1024 X 8
- Three-state outputs
- Typical address access time . . . 35 ns
- Typical select time . . . 55 ns
- Typical power . . . 500/60 mW

See Page 2-13

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 E2
7 A1	19 E3
8 A0	20 $\overline{E1}$
9 Q0	21 $\overline{E4}$
10 Q1	22 A9
11 Q2	23 A8
12 GND	24 V_{CC}

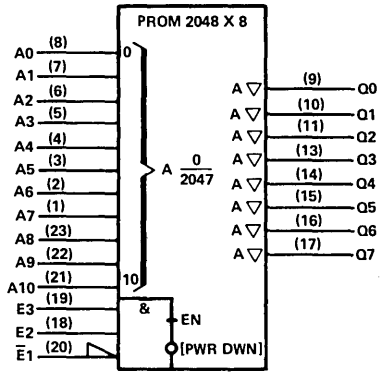
For chip carrier options and information, contact the factory.

TBP28P166

POWER-DOWN PROGRAMMABLE READ-ONLY MEMORIES

- 2048 X 8
- Three-state outputs
- Typical address access time . . . 35 ns
- Typical power . . . 650/125 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 E2
7 A1	19 E3
8 A0	20 E1
9 Q0	21 A10
10 Q1	22 A9
11 Q2	23 A8
12 GND	24 V_{CC}

For chip carrier options and information, contact the factory.

See Page 2-13

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

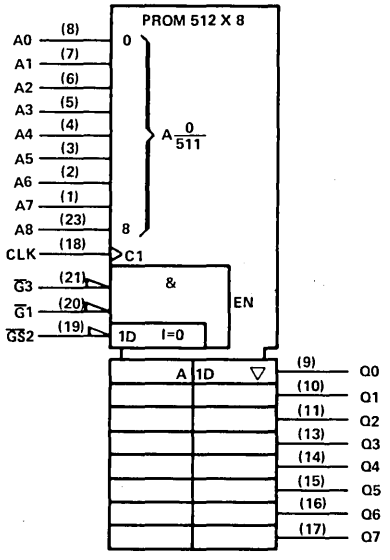
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TBP28R45

REGISTERED PROGRAMMABLE READ-ONLY MEMORIES

- 512 X 8
- Three-state outputs
- Typical clock-to-output time . . . 20 ns
- Typical address setup time . . . 20 ns
- Typical power . . . 550 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 CLK
7 A1	19 $\overline{GS2}$
8 A0	20 $\overline{G1}$
9 Q0	21 $\overline{G3}$
10 Q1	22 nc
11 Q2	23 A8
12 GND	24 V_{CC}

For chip carrier options and information, contact the factory.

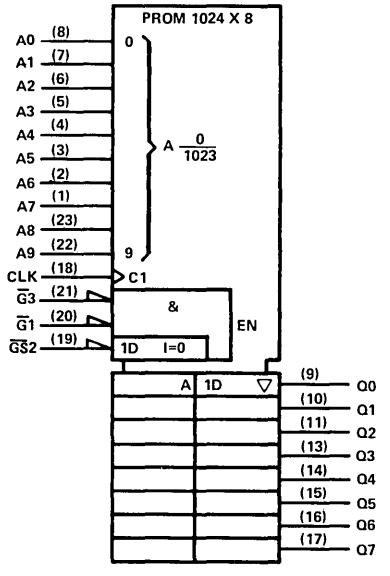
See Page 2-13

TBP28R85

REGISTERED PROGRAMMABLE READ-OUT MEMORIES

- 1024 X 8
- Three-state outputs
- Typical clock-to-output time . . . 20 ns
- Typical address setup time . . . 20 ns
- Typical power . . . 600 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 CLK
7 A1	19 $\overline{GS2}$
8 A0	20 $\overline{G1}$
9 Q0	21 $\overline{G3}$
10 Q1	22 A9
11 Q2	23 A8
12 GND	24 V_{CC}

For chip carrier options and information, contact the factory.

See Page 2-13

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

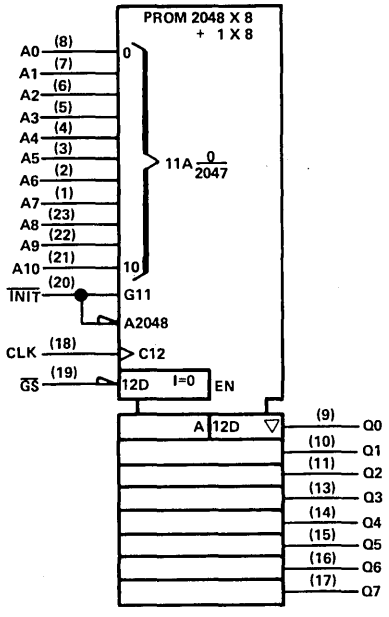
8

TBP28R165

REGISTERED PROGRAMMABLE READ-ONLY MEMORIES WITH INITIALIZE

- Single dedicated input provides output initialize to user-programmed preset, clear, or any state
- 2048 X 8
- Three-state outputs
- Typical clock-to-output time . . . 20 ns
- Typical address setup time . . . 20 ns
- Typical power . . . 700 mW

logic symbol†



See Page 2-13

pin assignments

J, N PACKAGES			
1	A7	13	Q3
2	A6	14	Q4
3	A5	15	Q5
4	A4	16	Q6
5	A3	17	Q7
6	A2	18	CLK
7	A1	19	$\overline{GS}$
8	A0	20	$\overline{INIT}$
9	Q0	21	A10
10	Q1	22	A9
11	Q2	23	A8
12	GND	24	V_{CC}

For chip carrier options and information, contact the factory.

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

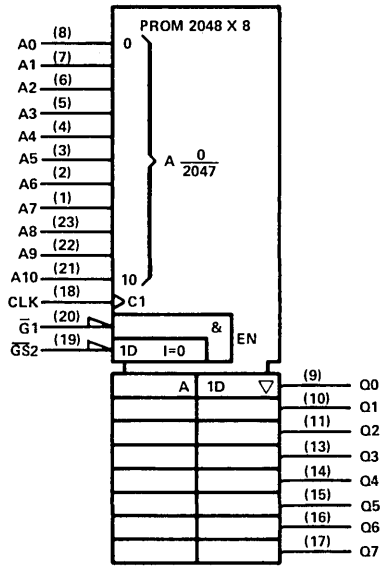
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TBP28R166

REGISTERED PROGRAMMABLE READ-ONLY MEMORIES

- 2048 X 8
- Three-state outputs
- Typical clock-to-output time . . . 20 ns
- Typical address setup time . . . 20 ns
- Typical power . . . 700 mW

logic symbol†



pin assignments

J, N PACKAGES			
1	A7	13	Q3
2	A6	14	Q4
3	A5	15	Q5
4	A4	16	Q6
5	A3	17	Q7
6	A2	18	CLK
7	A1	19	$\overline{GS2}$
8	A0	20	$\overline{G1}$
9	Q0	21	A10
10	Q1	22	A9
11	Q2	23	A8
12	GND	24	V_{CC}

For chip carrier options and information, contact the factory.

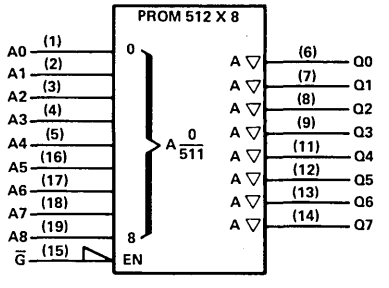
See Page 2-13

TBP28S42

PROGRAMMABLE READ-ONLY MEMORIES

- 512 X 8
- Three-state outputs
- Typical address access time . . . 35 ns
- Typical select time . . . 20 ns
- Typical power . . . 500 mW

logic symbol†



pin assignments

J, N PACKAGES			
1	A0	11	Q4
2	A1	12	Q5
3	A2	13	Q6
4	A3	14	Q7
5	A4	15	$\overline{G}$
6	Q0	16	A5
7	Q1	17	A6
8	Q2	18	A7
9	Q3	19	A8
10	GND	20	V_{CC}

For chip carrier options and information, contact the factory.

See Page 2-13

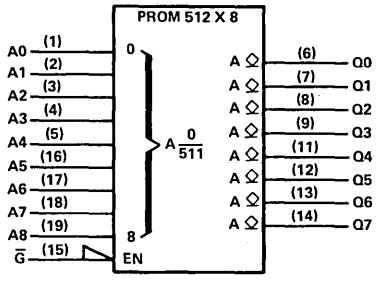
† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TBP28SA42

PROGRAMMABLE READ-ONLY MEMORIES

- 512 X 8
- Open-collector outputs
- Typical address access time . . . 35 ns
- Typical select time . . . 20 ns
- Typical power . . . 500 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A0	11 Q4
2 A1	12 Q5
3 A2	13 Q6
4 A3	14 Q7
5 A4	15 $\overline{G}$
6 Q0	16 A5
7 Q1	17 A6
8 Q2	18 A7
9 Q3	19 A8
10 GND	20 V_{CC}

For chip carrier options and information, contact the factory.

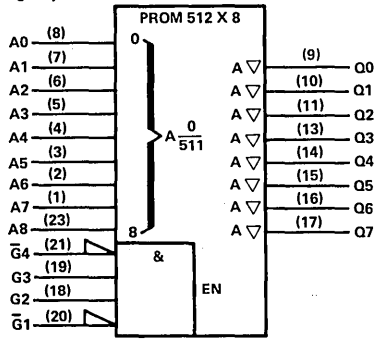
See Page 2-13

TBP28S45
TBP28S46

PROGRAMMABLE READ-ONLY MEMORIES

- 512 X 8
- Three-state outputs
- Typical address access time . . . 35 ns
- Typical select time . . . 20 ns
- Typical power . . . 500 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 G2
7 A1	19 G3
8 A0	20 $\overline{G1}$
9 Q0	21 $\overline{G4}$
10 Q1	22 nc
11 Q2	23 A8
12 GND	24 V_{CC}

For chip carrier options and information, contact the factory.

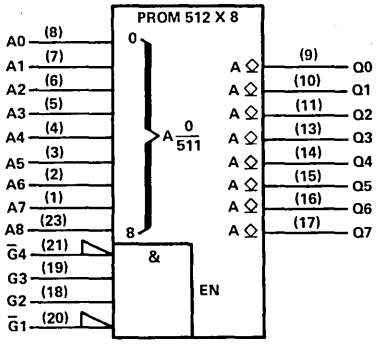
See Page 2-13

TBP28SA46

PROGRAMMABLE READ-ONLY MEMORIES

- 512 X 8
- Open-collector outputs
- Typical address access time . . . 35 ns
- Typical select time . . . 20 ns
- Typical power . . . 500 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 G2
7 A1	19 G3
8 A0	20 $\overline{G1}$
9 Q0	21 $\overline{G4}$
10 Q1	22 nc
11 Q2	23 A8
12 GND	24 V_{CC}

For chip carrier options and information, contact the factory.

See Page 2-13

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

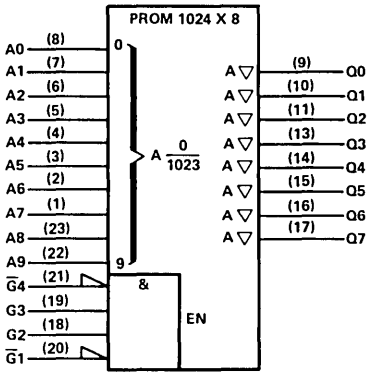
TBP28S85

PROGRAMMABLE READ-ONLY MEMORIES

- 1024 X 8
- Three-state outputs
- Typical address access time . . . 35 ns
- Typical select time . . . 15 ns
- Typical power . . . 550 mW

See Page 2-13

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 G2
7 A1	19 G3
8 A0	20 $\overline{G}$1
9 Q0	21 $\overline{G}$4
10 Q1	22 A9
11 Q2	23 A8
12 GND	24 V_{CC}

For chip carrier options and information, contact the factory.

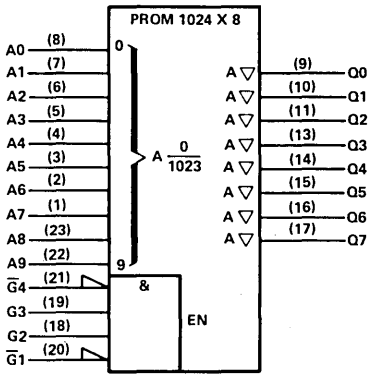
TBP28S86 ('S478)
TBP28S86-60

PROGRAMMABLE READ-ONLY MEMORIES

- 1024 X 8
- Three-state outputs
- Typical address access time . . . 45 ns
- TBP28S86-60 maximum address access time . . . 60 ns
- Typical select time . . . 20 ns
- Typical power . . . 625 mW

See Page 2-13

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 G2
7 A1	19 G3
8 A0	20 $\overline{G}$1
9 Q0	21 $\overline{G}$4
10 Q1	22 A9
11 Q2	23 A8
12 GND	24 V_{CC}

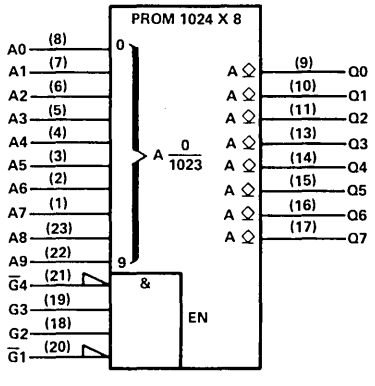
For chip carrier options and information, contact the factory.

TBP28SA86 ('S479)
TBP28SA86-60

PROGRAMMABLE READ-ONLY MEMORIES

- 1024 X 8
- Open-collector outputs
- Typical address access time . . . 45 ns
- TBP28SA86-60 maximum address access time . . . 60 ns
- Typical select time . . . 20 ns
- Typical power . . . 625 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 G2
7 A1	19 G3
8 A0	20 $\overline{G}$1
9 Q0	21 $\overline{G}$4
10 Q1	22 A9
11 Q2	23 A8
12 GND	24 V_{CC}

For chip carrier options and information, contact the factory.

See Page 2-13

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

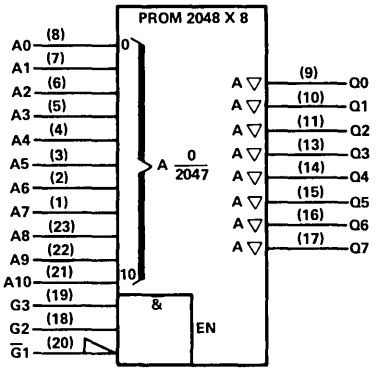
TBP28S166

PROGRAMMABLE READ-ONLY MEMORIES

- 2048 X 8
- Three-state outputs
- Typical address access time . . . 35 ns
- Typical select time . . . 15 ns
- Typical power . . . 650 mW

See Page 2-13

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 G2
7 A1	19 G3
8 A0	20 $\overline{G}$1
9 Q0	21 A10
10 Q1	22 A9
11 Q2	23 A8
12 GND	24 V_{CC}

For chip carrier options and information, contact the factory.

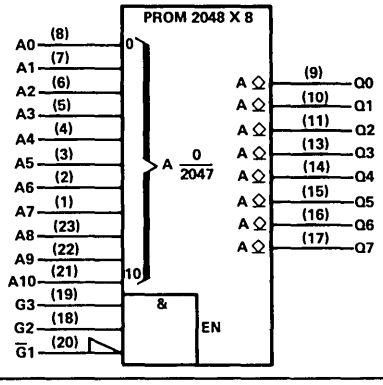
TBP28SA166

PROGRAMMABLE READ-ONLY MEMORIES

- 2048 X 8
- Open-collector outputs
- Typical address access time . . . 35 ns
- Typical select time . . . 15 ns
- Typical power . . . 650 mW

See Page 2-13

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 G2
7 A1	19 G3
8 A0	20 $\overline{G}$1
9 Q0	21 A10
10 Q1	22 A9
11 Q2	23 A8
12 GND	24 V_{CC}

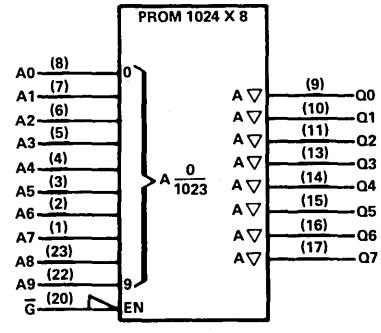
For chip carrier options and information, contact the factory.

TBP28S2708 ('S2708)

PROGRAMMABLE READ-ONLY MEMORIES

- 1024 X 8
- Three-state outputs
- Typical address access time . . . 45 ns
- Typical select time . . . 20 ns
- Typical power . . . 625 mW

logic symbol†



See Page 2-13

pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 nc
7 A1	19 nc
8 A0	20 $\overline{G}$
9 Q0	21 nc
10 Q1	22 A9
11 Q2	23 A8
12 GND	24 V_{CC}

For chip carrier options and information, contact the factory.

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TIM8228	is the same as SN74S428
TIM8238	is the same as SN74S438
TIM9905	is the same as SN74LS251
TIM9906	is the same as SN74LS259
TIM9907	is the same as SN74148
TIM9908	is the same as SN74LS348

MECHANICAL DATA

ORDERING INSTRUCTIONS

Orders for devices from this book should include the package outline letter(s) at the end of the type number.

Examples: SN54S482J, SN74S740N

It is necessary to use only the first letter of the package type (J or N) unless the device is available in more than one type of J (dual-in-line ceramic) package, or in more than one type of N (dual-in-line plastic) package.

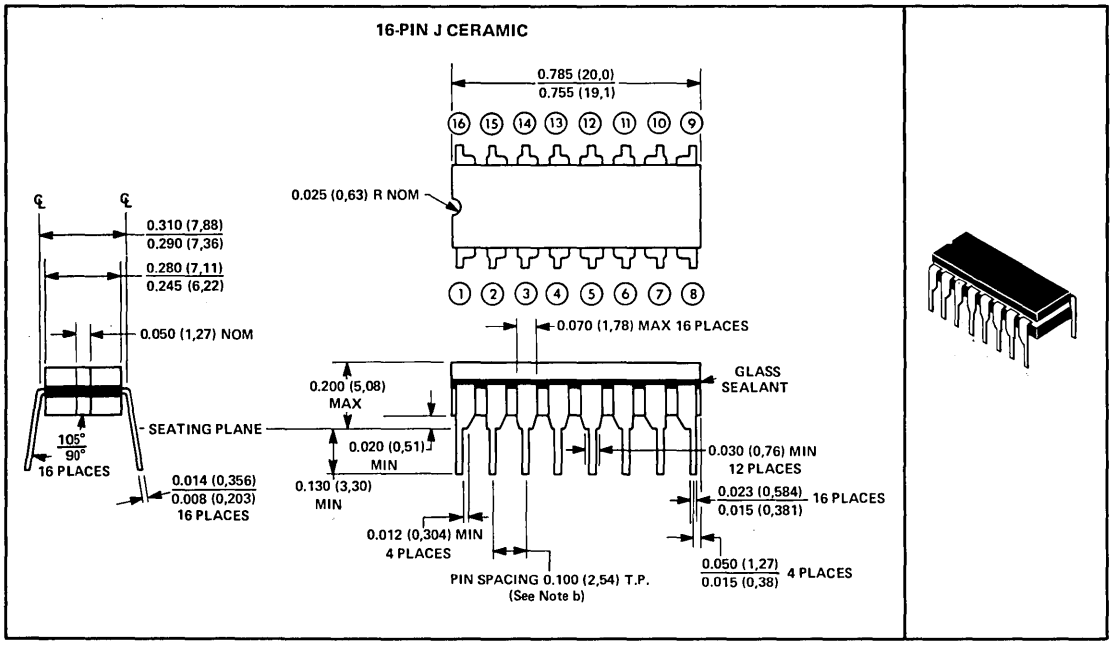
Special ordering instructions for programmable read-only memories (PROMs) are found on page 2-2.

J ceramic packages (including JT and JW dual-in-line and JQ quad-in-line packages)

These hermetically sealed dual-in-line packages consist of a ceramic base, ceramic cap, and a 16-, 18-, 20-, 24-, 28-, or 48-lead frame. Hermetic sealing is accomplished with glass. The JT packages are intended for insertion in mounting-hole rows on 0.300 (7,62) centers, JW packages for mounting-hole rows on 0.600 (15,24) centers, and the JQ quad-in-line package for mounting-hole rows on 0.600 (15,24) and 0.800 (20,32) centers. Once the leads are compressed and inserted sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.

NOTE: For the 16-, 28-, and 20-pin packages, the letter J is used by itself since these packages are available only in the 0.300 (7,62) row spacing. For the 24-pin packages, if no second letter nor row spacing is specified, the package is assumed to have 0.600 (15,24) row spacing.

16-PIN J CERAMIC

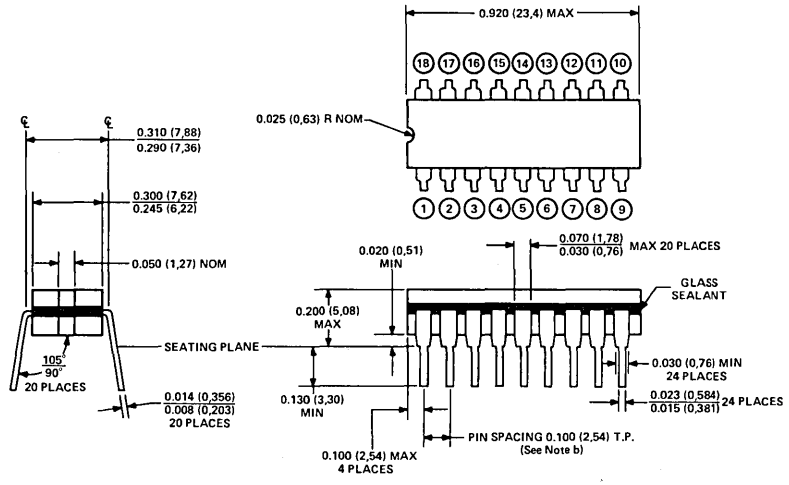


NOTES: a. All dimensions are shown in inches (and parenthetically in millimeters for reference only). Inch dimensions govern.
b. Each pin centerline is located within 0.010 (0,26) of its true longitudinal position.

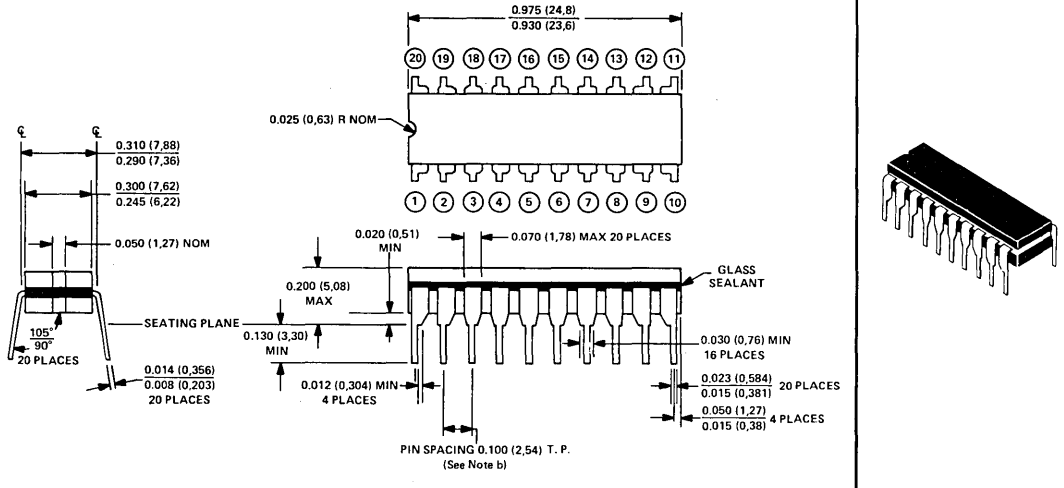
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

J ceramic packages (continued)

18-PIN J CERAMIC

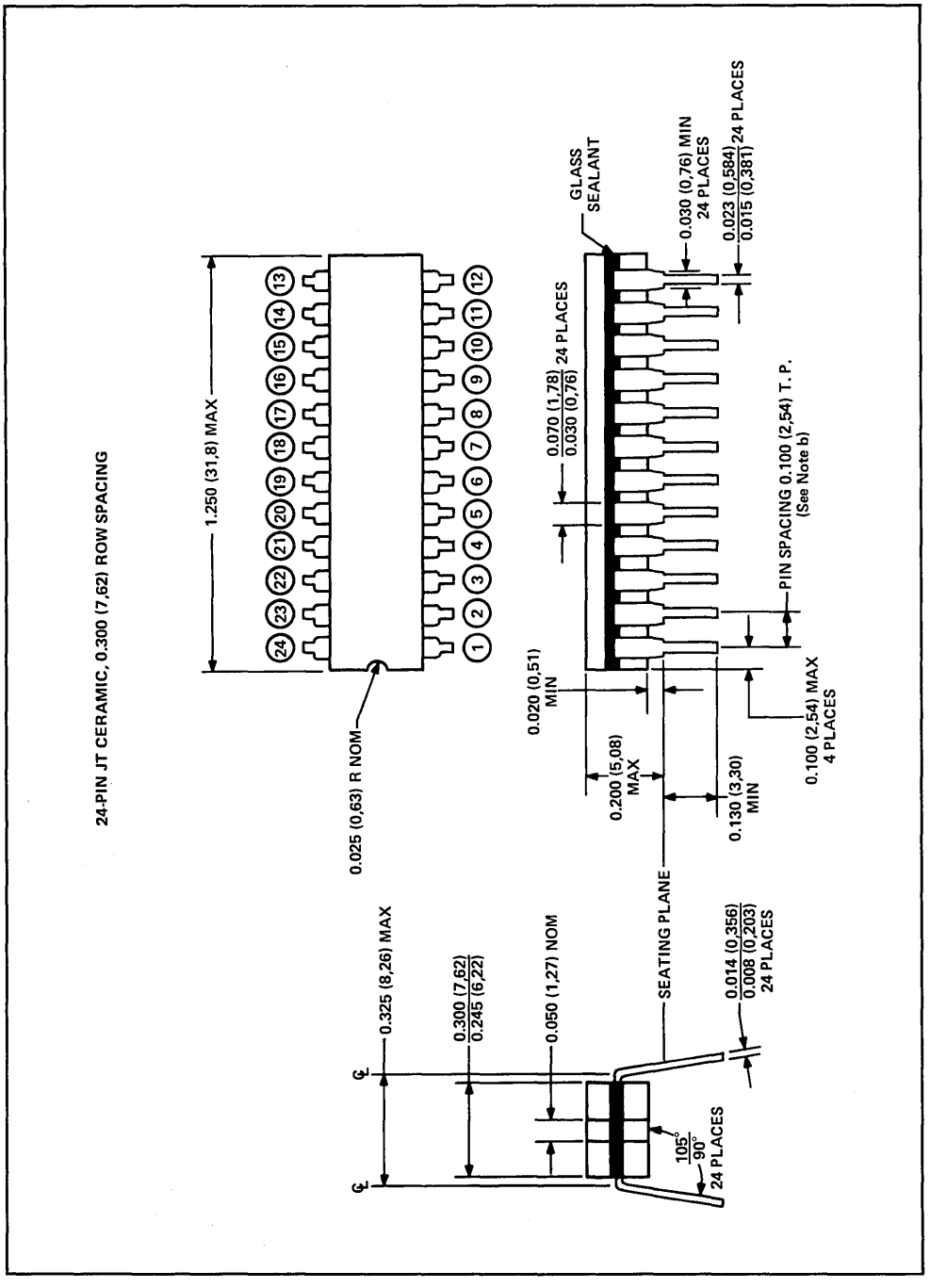


20-PIN J CERAMIC



NOTES: a. All dimensions are shown in inches (and parenthetically in millimeters for reference only). Inch dimensions govern.
b. Each pin centerline is located within 0.010 (0,26) of its true longitudinal position.

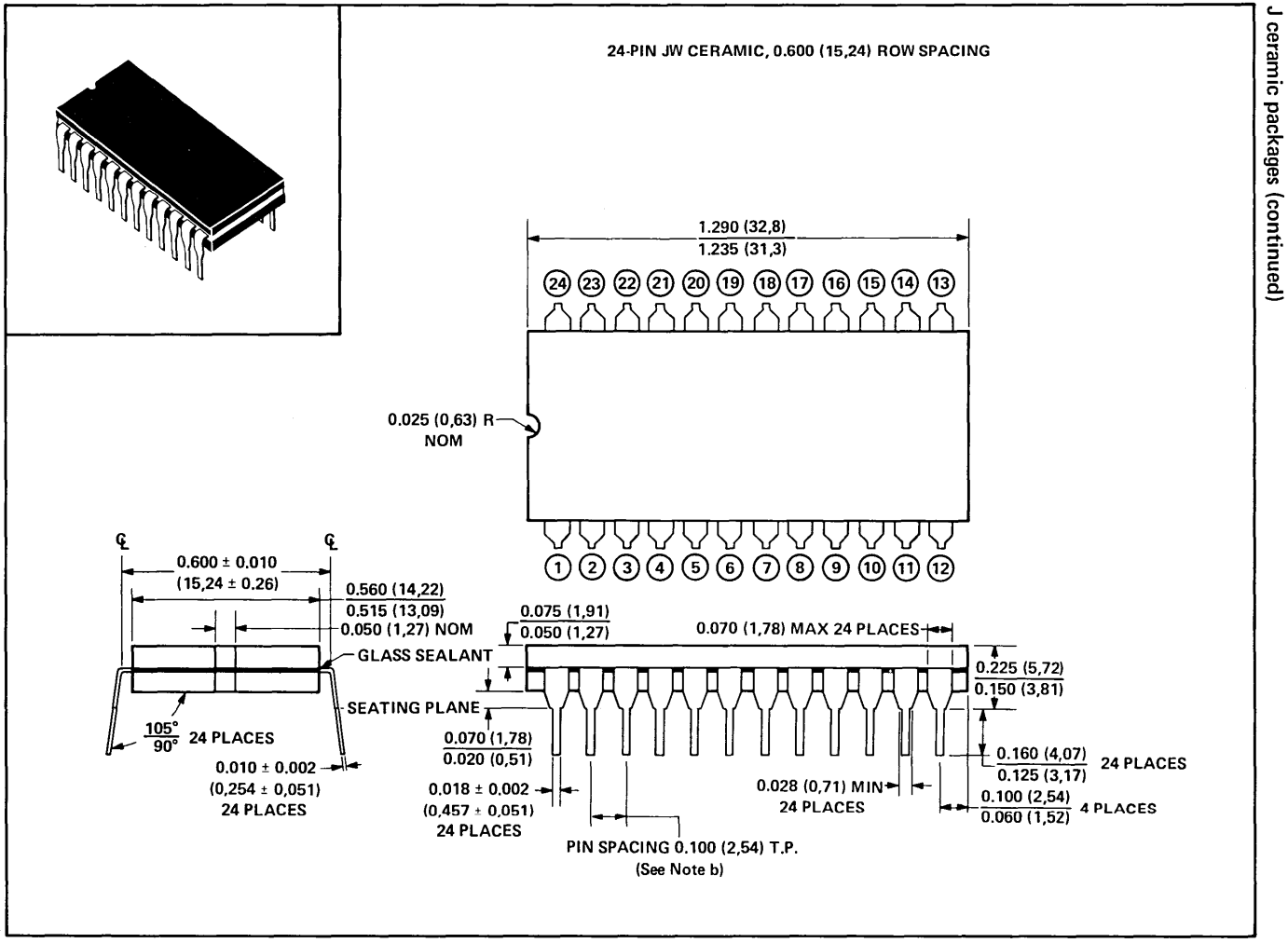
J ceramic packages (continued)



NOTES: a. All dimensions are shown in inches (and parenthetically in millimeters for reference only). Inch dimensions govern.
b. Each pin centerline is located within 0.010 (0,26) of its true longitudinal position.

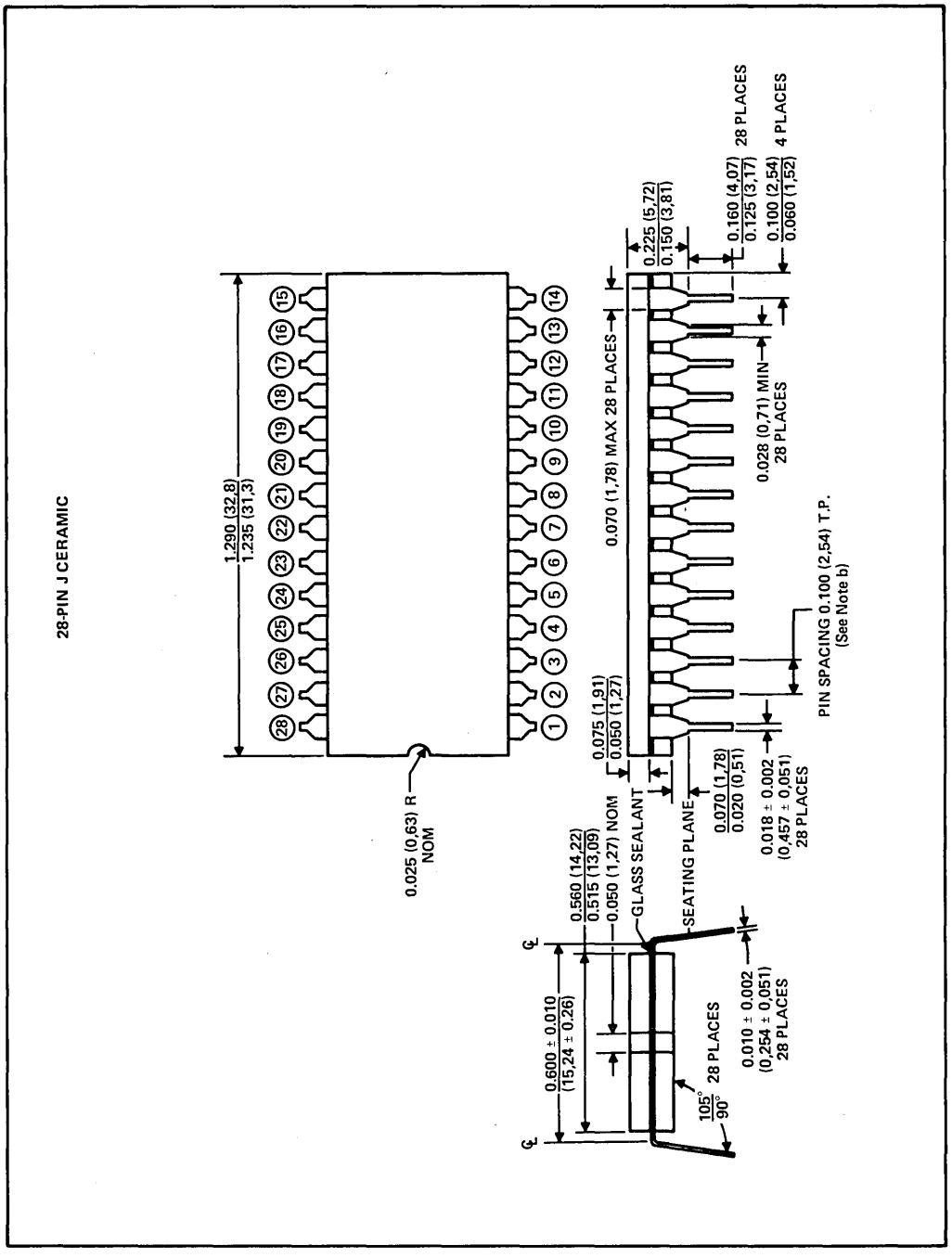
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

J ceramic packages (continued)



NOTES: a. All dimensions are shown in inches (and parenthetically in millimeters for reference only). Inch dimensions govern.
b. Each pin centerline is located within 0.010 (0,26) of its true longitudinal position.

J ceramic packages (continued)

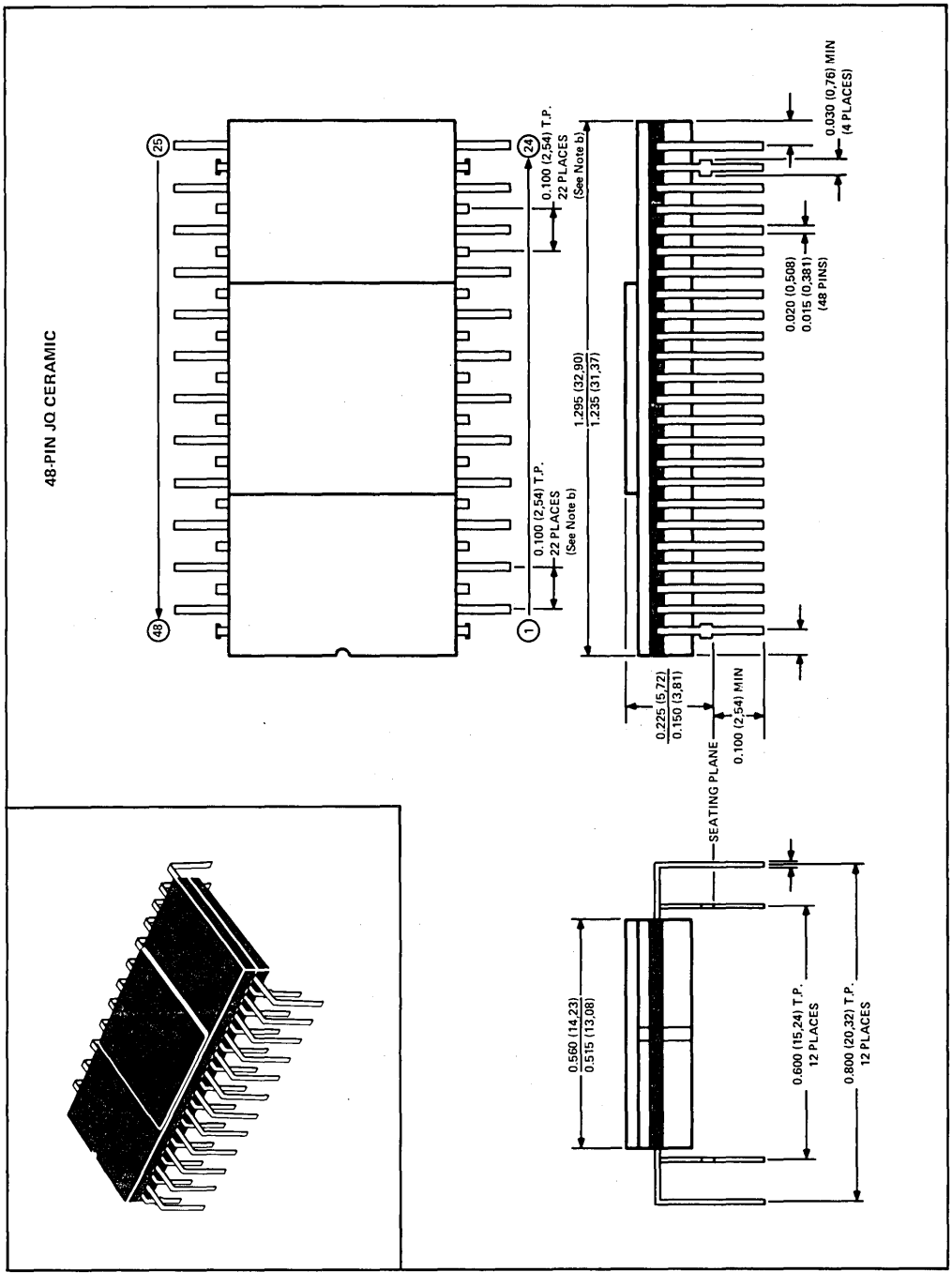


NOTES: a. All dimensions are shown in inches (and parenthetically in millimeters for reference only). Inch dimensions govern.
b. Each pin centerline is located within 0.010 (0,26) of its true longitudinal position.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

J ceramic packages (continued)

48-PIN JQ CERAMIC



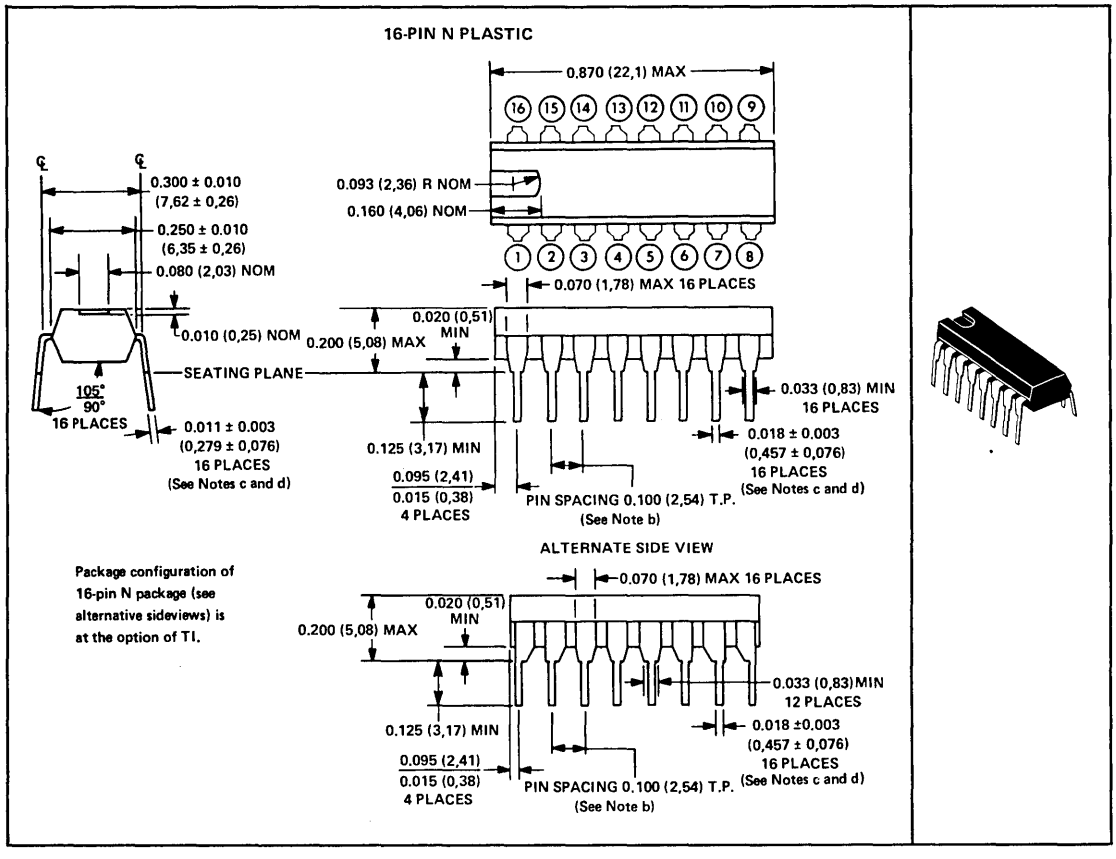
NOTES: a. All dimensions are shown in inches (and parenthetically in millimeters for reference only). Inch dimensions govern.
b. Each pin centerline is located within 0.010 (0,26) of its true longitudinal position.

9

N plastic packages (including NT and NW dual-in-line packages)

These dual-in-line packages consist of a circuit mounted on a 16-, 18-, 20-, 24-, or 28-pin lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. The packages are intended for insertion in mounting-hole rows on 0.300 (7,62) centers for the NT packages and on 0.600 (15,24) centers for the NW packages. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

NOTE: For the 16-, 18-, 20-, and 28-pin packages, the letter N is used by itself since these packages are available in only one row-spacing width — 0.300 (7,62) for the 16-, 18-, and 20-pin packages and 0.600 (15,24) for the 28-pin package. For the 24-pin package, if no second letter nor row spacing is specified, the package is assumed to have 0.600 (15,24) row spacing.

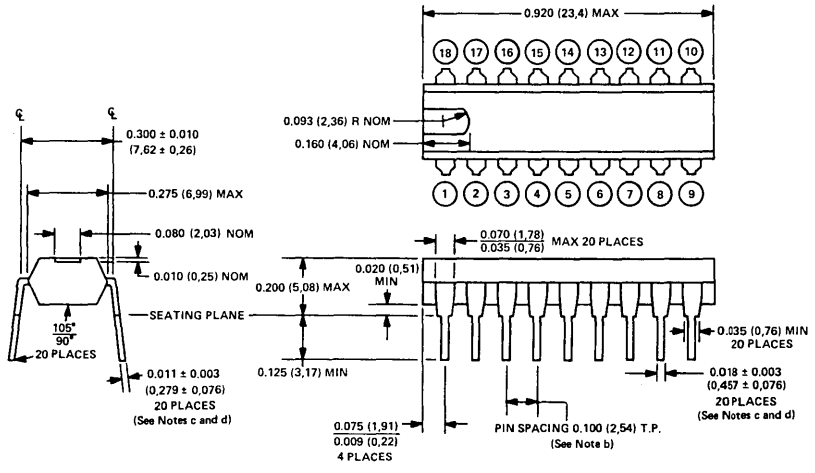


NOTES: a. All dimensions are shown in inches (and parenthetically in millimeters for reference only). Inch dimensions govern.
b. Each pin centerline is located within 0.010 (0,26) of its true longitudinal position.

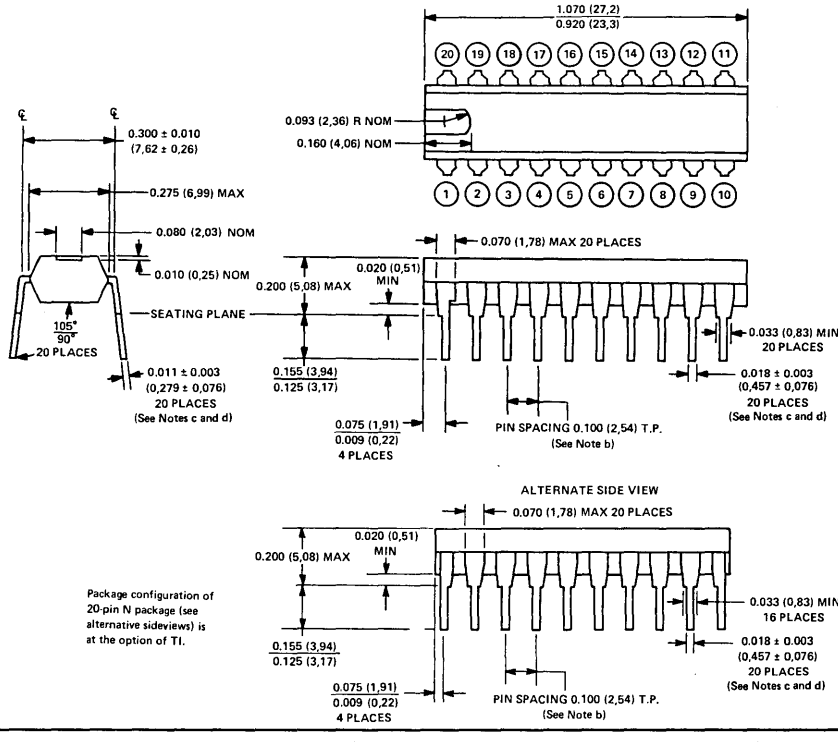
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

N plastic packages (continued)

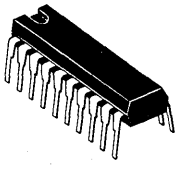
18-PIN N PLASTIC



20-PIN N PLASTIC



Package configuration of 20-pin N package (see alternative sideviews) is at the option of TI.

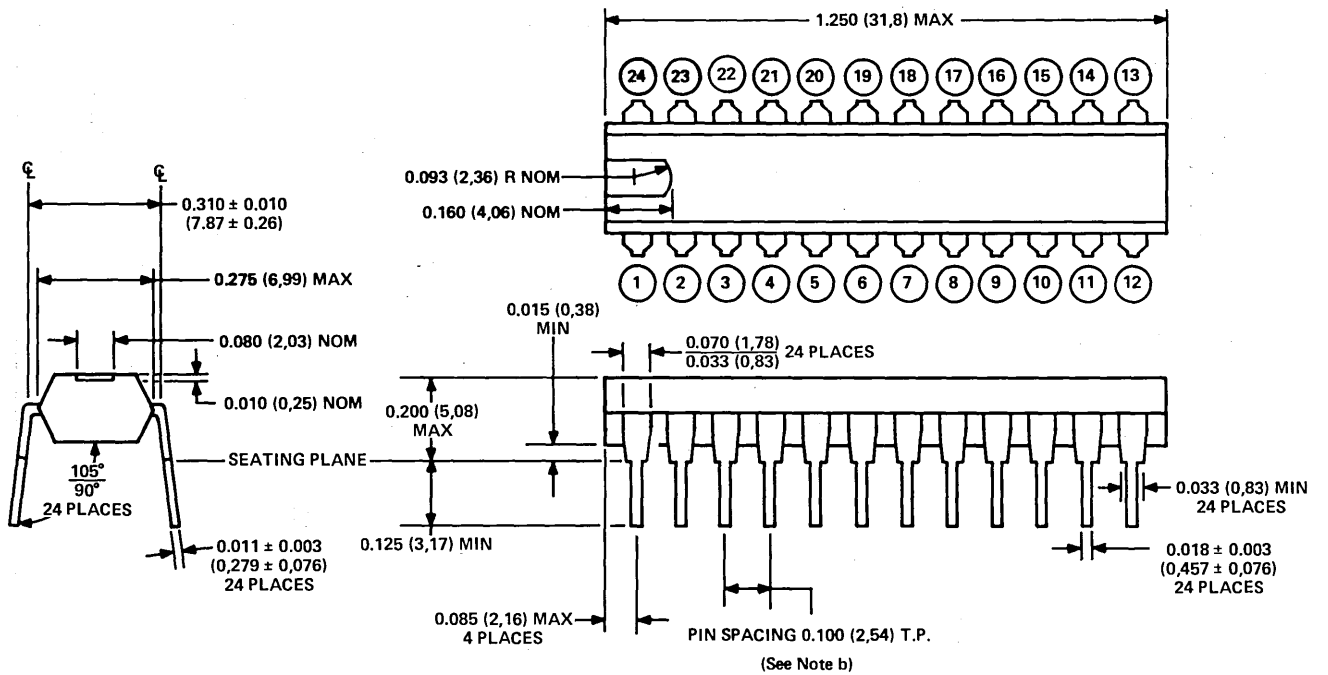


NOTES: a. All dimensions are shown in inches (and parenthetically in millimeters for reference only). Inch dimensions govern.
b. Each pin centerline is located within 0.010 (0,26) of its true longitudinal position.

9

N plastic packages (continued)

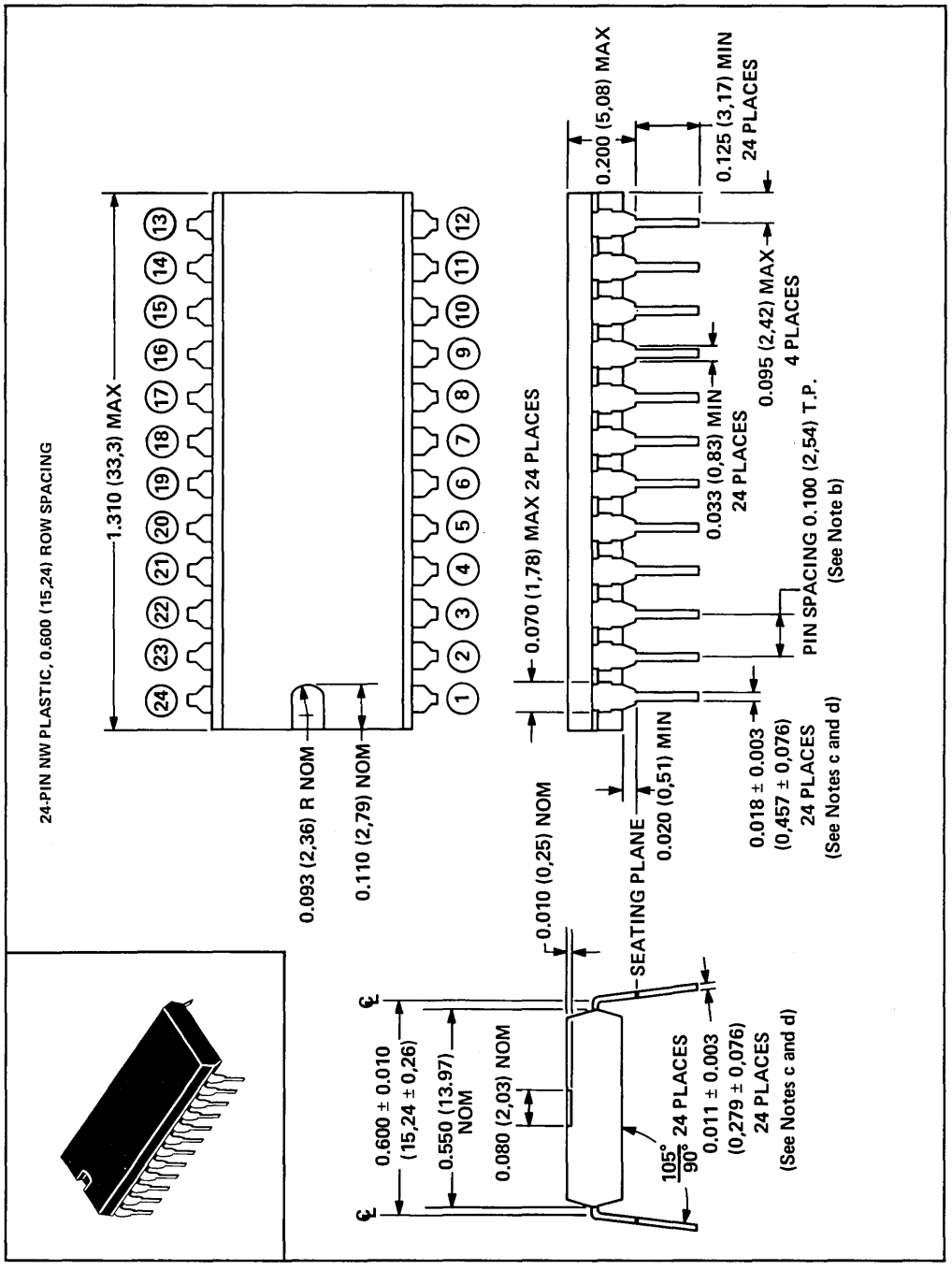
24-PIN NT PLASTIC, 0.300 (7,62) ROW SPACING



NOTES: a. All dimensions are shown in inches (and parenthetically in millimeters for reference only). Inch dimensions govern.
b. Each pin centerline is located within 0.010 (0,26) of its true longitudinal position.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

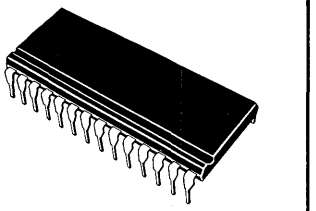
N plastic packages (continued)



NOTES: a. All dimensions are shown in inches (and parenthetically in millimeters for reference only). Inch dimensions govern.
b. Each pin centerline is located within 0.010 (0,26) of its true longitudinal position.

9

N plastic packages (continued)



28-PIN N PLASTIC

NOTES: a. All dimensions are shown in inches (and parenthetically in millimeters for reference only). Inch dimensions govern.
b. Each pin centerline is located within 0.010 (0,26) of its true longitudinal position.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

FN plastic chip carrier package

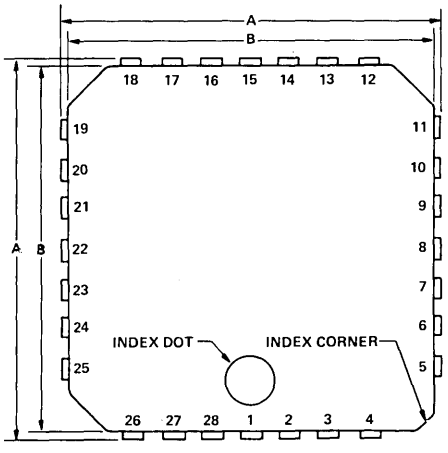
Each of these chip carrier packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound withstands soldering temperatures with no deformation, and circuit performance characteristics remain stable when the devices are operated in high-humidity conditions. The packages are intended for surface mounting on solder lands on 0.050-inch centers. Leads require no additional cleaning or processing when used in soldered assembly.

The following bipolar digital device families will be offered in these plastic chip carrier packages: Advanced Schottky and Advanced Low-Power Schottky, all bipolar PROMs, some Schottky and some Low-Power Schottky.

Products in design will be offered in 44-lead (MS007AB), 52-lead (MS007AC), and 68-lead (MS007AD) packages.

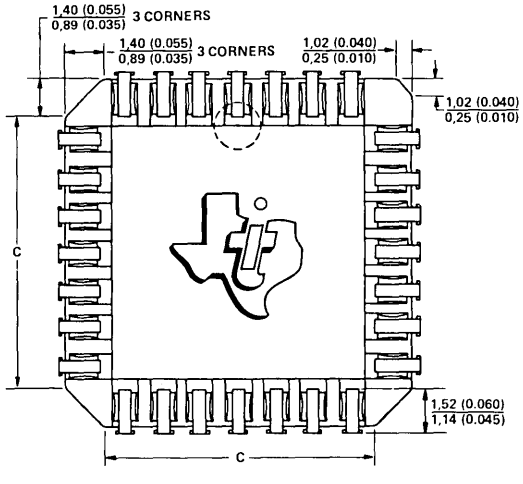
FN PLASTIC CHIP CARRIER PACKAGE

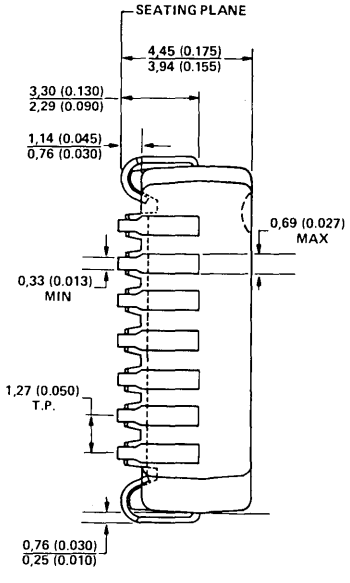
(28-terminal package shown)



JEDEC OUTLINE DESIGNATION*	NO. OF TERMINALS	A MIN	A MAX	B MIN	B MAX	C MIN	C MAX
	20	9,40 (0.370)	10,41 (0.410)	8,64 (0.340)	9,14 (0.360)	6,35 (0.250)	6,48 (0.255)
MS007AA	28	11,94 (0.470)	12,95 (0.510)	11,18 (0.440)	11,68 (0.460)	8,76 (0.345)	9,02 (0.355)

*All dimensions and notes for the specified JEDEC outline apply.





NOTE: Dimensions are in millimeters and (inches).

CHIP CARRIER MECHANICAL DATA

FC and FD ceramic chip carrier packages

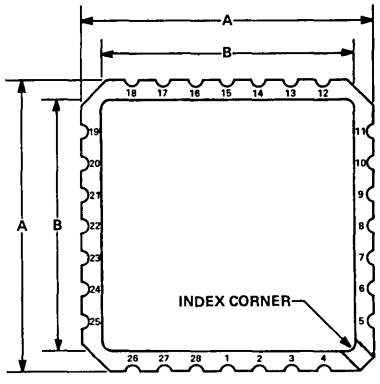
Both versions of these hermetically sealed chip carrier packages have ceramic bases. The FC package has a single-layer base with a ceramic lid and glass seal. The FD package has a three-layer base with either a metal lid and braze seal or a ceramic lid and glass seal, at the option of Texas Instruments.

The packages are intended for surface mounting on solder lands on 0.050-inch centers. Terminals require no additional cleaning or processing when used in soldered assembly.

The full-military-temperature-range versions of the following bipolar digital device families will be offered in these or similar ceramic chip carrier packages: Advanced Low-Power Schottky, PROMs and RAMs, and certain memory support functions (i.e., 'S225, 184A, 185, 284, 285 and 'LS630).

Products in design will be offered in 44-terminal (MS004CD), 52-terminal (MS004CE), 68-terminal (MS004CF), and 84-terminal (MS004CG) packages.

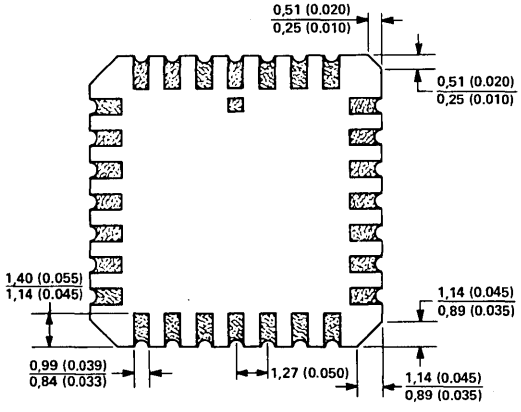
FC AND FD CERAMIC CHIP CARRIER PACKAGES
(28-terminal package shown)

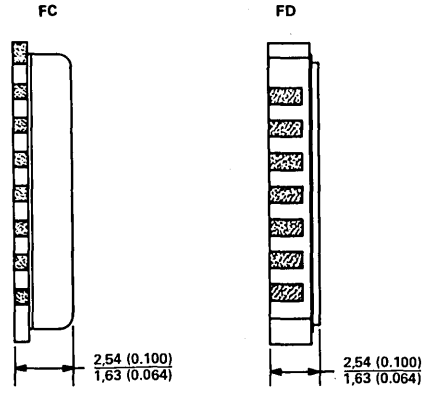


CERAMIC CHIP CARRIERS

JEDEC OUTLINE DESIGNATION*	NUMBER OF TERMINALS	A MIN	A MAX	B MIN	B MAX	C MIN	C MAX
MS004CB	20	8,69 (0.342)	9,09 (0.358)	7,8 (0.307)	9,1 (0.358)	1,6 (0.064)	2,5 (0.100)
MS004CC	28	11,23 (0.442)	11,63 (0.458)	10,3 (0.406)	11,6 (0.458)	1,6 (0.064)	2,5 (0.100)
MS004CD	44	16,26 (0.640)	16,76 (0.660)	12,6 (0.495)	14,2 (0.560)	1,8 (0.069)	3,0 (0.120)
MS004CF	68	23,83 (0.938)	24,43 (0.962)	12,6 (0.495)	21,9 (0.862)	2,1 (0.082)	3,0 (0.120)

*All dimensions and notes for the specified JEDEC outline apply.





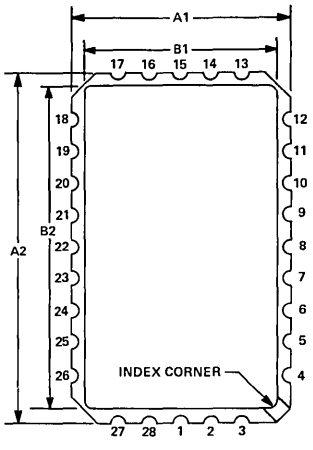
All dimensions are in millimeters and parenthetically in inches.

FE ceramic chip carrier packages

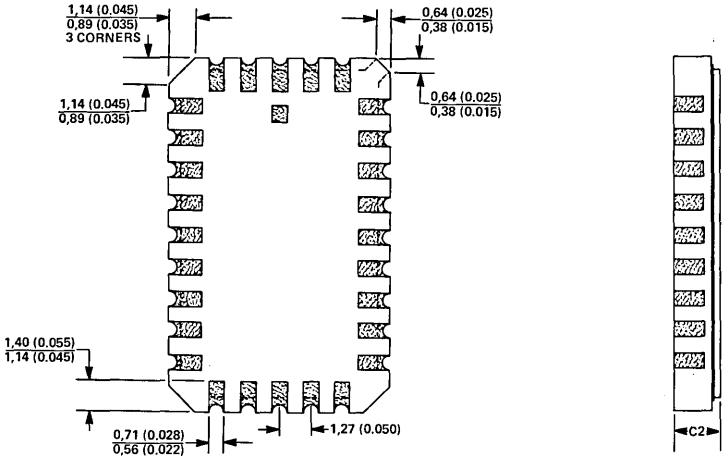
Each of these hermetically sealed leadless chip carrier packages has a metal cap, a 3-layer ceramic base, and a brazed seal. The packages are intended for surface mounting on solder lands on 0.050-inch centers. Terminals require no additional cleaning or processing when used in soldered assembly.

The full-military-temperature-range versions of the following memories will be offered in these or similar ceramic chip carrier packages: PROMs, SRAMs, DRAMs, and EPROMs.

RECTANGULAR FE CERAMIC CHIP CARRIER PACKAGE
(28-terminal package shown)



NUMBER OF TERMINALS	A1		A2		B1		B2		C2	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
28	8,76 (0.345)	9,02 (0.355)	13,84 (0.545)	14,10 (0.555)	7,80 (0.307)	7.95 (0.313)	12,88 (0.507)	13,03 (0.513)	1,65 (0.065)	2,01 (0.079)
32	11,30 (0.445)	11,56 (0.455)	13,84 (0.545)	14,10 (0.555)	10,34 (0.407)	13,03 (0.513)	12,88 (0.507)	13,03 (0.513)	1,65 (0.065)	2,01 (0.079)



Dimensions are in millimeters and parenthetically in inches.

LCC5831

PRINTED IN U.S.A.