SMYD006

MOS Memory Data Book

1986

Commercial and Military Specifications

TEXAS INSTRUMENTS

BRAD WARWICK

MOS Memory Data Book

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TEXAS INSTRUMENTS

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Specifications contained in this data book supersede all data for these products published by TI in the United States before November 1985.

INTRODUCTION

The 1986 MOS Memory Data Book from Texas Instruments includes complete detailed specifications on the expanding MOS Memory product line including Dynamic Random-Access Memories (DRAMs), Single-In-Line Package DRAM Memory Modules (SIPs), Eraseable Programmable Read-Only Memories (EPROMs), MOS one-time Programmable Read-Only Memories (PROMs), and Read-Only Memories (ROMs) for the United States market. Also provided are military specifications for the DRAM product line. This is TI's first MOS Memory data book to include specifications for complementary MOS (CMOS) memory devices (which now span all MOS Memory product lines). Surface-mount packaging is now available on all 64K, 256K and 1 MEG DRAMs and CMOS ROMs. Another packaging option for DRAMs is the SIP which can increase memory density by over 3.5 times that of dual-in-line packages.

This data book is divided into 12 sections. Section 1, General Information, includes the table of contents, an alphanumeric index for quickly finding device numbers, plus a device selection guide and a product reference guide for quick overview of the broad TI MOS Memory product line. Page numbers are included on the product reference guide for easy access to the detailed specifications. In Section 2, the Interchangeability Guide lists alternate vendor part numbering examples in addition to alternate sources to TI devices (based on published data). Product specifications for 71 devices can be found in Sections 4 through 8.

Recently published design considerations, product applications, and technical articles can be found in Section 9. Also included is a section (Section 12) on guidelines for handling ESD sensitive devices, since all MOS Memory devices are ESD sensitive.

The data sheets within each section are in alphanumeric order; Product Preview information is included at the end of the section. Data Sheets listed with a "TMX" prefix and Product Preview disclaimer include target specifications for products that are currently under development at TI. The inclusion of these specifications does not imply that these products are or will be in production, or will meet these parameters.

Additional and/or updated information on these products is available from:

Texas Instruments
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CONTENTS

WORDS	BITS PER WORD		
	1	4	8
1K			
2K			
4K			(32K) EPROM: TMS2732A PROM: TMS27P32A ROMs: TMS2332, TMS4732
8K			(64K) EPROMs: TMS2764, TMS27C64 PROM: TMS27P64 ROMs: TMS2364, TMS4764
16K	(16K) DRAM: TMS4116	(64K) DRAMs: TMS4416, SMJ4416	(128K) EPROM: TMS27C128 PROM: TMX27PC128 ROM: TMS47128
32K			(256K) EPROM: TMS27C256 PROM: TMX27PC256 ROMs: TMS47256, TMS47C256
64K	(64K) DRAMs: TMS4161, TMS4164, SMJ4161, SMJ4164	(256K) DRAMs: TMS4464, TMX4461	(512K) EPROM: TMX27C512 ROM: TMS47C512
128K	(128K) DRAM: TMS41128B		
256K	(256K) DRAMs: TMS4256, TMS4257, SMJ4256, SMJ4257	(1024K) DRAMs: TMX44C256, TMX44C257, TMX44C259	(1024K) ROM: TMS47C1024
1024K	(1024K) DRAMs: TMX4C1024, TMX4C1025, TMX4C1026, TMX4C1027, TMX4C1029		

Numbers in parentheses indicate overall complexity.

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WORDS	BITS PER WORD				
	1	4	5	8	9
16K				TM4416KU8	
64K		(256K) TM4164EC4	(320K) TM4164EQ5	(512K) TM4164FL8 TM4164FM8 TM4464LU8	(576K) TM4164EL9 TM4164FM9
64K Multiport Video RAM		(256K) TM4161EV4 TM4161GW4 TM4161GY4	(320K) TM4161EP5		
256K		(1024K) TM4256EC4 TM4257EC4	(1280K) TM4256EQ5 TM4257EQ5	(2048K) TM4256FL8 TM4257FL8 TM4256GU8 TM4257GU8 TM4256GP8 TM4256GV8	(2304K) TM4256EL9 TM4257EL9 TM4256GU9 TM4257GU9 TM4256GP8 TM4256GV9
512K		(2048K) TM4256HE4			
1 Meg	(1024K) TM4256FC1 TM4257FC1				

DRAM SELECTION GUIDE

Density	Device Number	Organization	Access Time Max (ns) $t_{a(R)}$	Cycle Time Min (ns)	Power Supplies (V)	Power Dissipation Max (mW) Active	Power Dissipation Max (mW) Standby	Pins	Package†	Page
16K	TMS4116-15	16K X 1	150	375	±5, 12	462	20	16	N	4-3
	TMS4116-20		200	375						
	TMS4116-25		250	410						
64K	TMS4164-12	64 X 1	120	230	5	264	28	16	N, FP	4-41
	TMS4164-15		150	260		248	28			
	TMS4164-20		200	330		204	28			
64K	TMS4416-12	16K X 4	120	230	5	297	28	18	N, FP	4-99
	TMS4416-15		150	260		264	28			
	TMS4416-20		200	330		231	28			
64K	TMS4161-15	64K X 1, Multiport Video RAM	150	240	5	523	110	20	N, FM	4-17
	TMS4161-20		200	315	5	495	110	20	N, FM	
256K	TMS4256-12	256K X 1, Page Mode	120	230	5	413	25	16	N, FM	4-75
	TMS4256-15		150	260		358	25			
	TMS4256-20		200	330		275	25			
256K	TMS4257-12	256K X 1, Nibble Mode	120	230	5	413	25	16	N, FM	4-75
	TMS4257-15		150	260		358	25			
	TMS4257-20		200	330		275	25			
256K	TMS4464-12	64K X 4	120	230	5	440	28	18	N, FM	4-117
	TMS4464-15		150	260		385	28			
	TMS4464-20		200	330		330	28			
256K	TMX4461-12‡	64K X 4, Multiport Video RAM	120	230	5	TBD	TBD	24	N	4-135
	TMX4461-15‡		150	260		TBD	TBD			
1 MEG	TMX4C102_-10‡	1M X 1	100	200	5	TBD	TBD	18	N, DJ	4-139
	TMX4C102_-12‡		120	230		TBD	TBD			
	TMX4C102_-15‡		150	260		TBD	TBD			
1 MEG	TMX44C25_-10‡	256K X 4	100	200	5	TBD	TBD	20	N, DJ	4-137
	TMX44C25_-12‡		120	230		TBD	TBD			
	TMX44C25_-15‡		150	260		TBD	TBD			

†N = Plastic DIP
FP = Plastic Chip Carrier
FM = Plastic Chip Carrier
DJ = Plastic SOJ Package
‡Preliminary Target Specifications for product under development by TI.

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DYNAMIC RAM MODULE SELECTION GUIDE

Density	Device Number	Organization	Access Time Max (ns)	Cycle Time Min (ns)	Power Supply (V)	Power Dissipation Max (mW)		Pins	Package	Page
						Active	Standby			
128K	TM4416KU8-12	16K X 8	120	230	5	594	55	30	Socketable	5-237
	TM4416KU8-15		150	260		528	55			
256K	TM4164EC4-12	64K X 4	120	230	5	1056	112	22	Leaded	5-51
	TM4164EC4-15		150	260		992	112			
	TM4164EC4-20		200	330		816	112			
256K	TM4161EV4-15	64K X 4, Multiport Video RAM	150	240	5	2092	440	31	Leaded	5-25
	TM4161EV4-20		200	315		1980	440			
256K	TM4161GW4-15	64K X 4, Multiport Video RAM	150	240	5	2092	440	30	Socketable	5-47
	TM4161GW4-20		200	315		1980	440			
256K	TM4161GY4-15	64K X 4, Multiport Video RAM	150	240	5	2092	440	30	Leaded	5-47
	TM4161GY4-20		200	315		1980	440			
320K	TM4161EP5-15	64K X 5, Multiport Video RAM	150	240	5	2615	550	35	Leaded	5-3
	TM4161EP5-20		200	315		2475	550			
320K	TM4164EQ5-12	64K X 5	120	230	5	1320	140	24	Leaded	5-81
	TM4164EQ5-15		150	260		1240	140			
	TM4164EQ5-20		200	330		1020	140			
512K	TM4164FL8-12	64K X 8	120	230	5	2112	224	30	Leaded	5-99
	TM4164FL8-15		150	260		1984	224			
	TM4164FL8-20		200	330		1632	224			
512K	TM4164FM8-12	64K X 8	120	230	5	2112	224	30	Socketable	5-99
	TM4164FM8-15		150	260		1984	224			
	TM4164FM8-20		200	330		1632	224			
512K	TM4464LU8-12	64K X 8	120	230	5	880	55	30	Socketable	5-247
	TM4464LU8-15		150	260		770	55			
576K	TM4164EL9-12	64K X 9	120	230	5	2376	252	30	Leaded	5-67
	TM4164EL9-15		150	260		2232	252			
	TM4164EL9-20		200	330		1836	252			
576K	TM4164FM9-12	64K X 9	120	230	5	2376	252	30	Socketable	5-67
	TM4164FM9-15		150	260		2232	252			
	TM4164FM9-20		200	330		1836	252			
1024K	TM4256FC1-12†	1M X 1	120	230	5	429	99	22	Leaded	5-181
	TM4256FC1-15†		150	260		374	99			
	TM4256FC1-20†		200	330		319	99			
1024K	TM4256EC4-12†	256K X 4	120	230	5	1716	99	22	Leaded	5-111
	TM4256EC4-15†		150	260		1496	99			
	TM4256EC4-20†		200	330		1276	99			

Continued next page.

†All 256K DRAM SIPs available with page-mode access (TM4256___) or nibble-mode access (TM4257___).

DYNAMIC RAM MODULE SELECTION GUIDE (CONCLUDED)

Density	Device Number	Organization	Access Time Max (ns)	Cycle Time Min (ns)	Power Supply (V)	Power Dissipation Max (mW)		Pins	Package	Page
						Active	Standby			
1280K	TM4256EQ5-12†	256K X 5	120	230	5	2145	124	22	Leaded	5-157
	TM4256EQ5-15†		150	260		1870	124			
	TM4256EQ5-20†		200	330		1595	124			
2048K	TM4256FL8-12†	256K X 8	120	230	5	3432	201	30	Leaded	5-205
	TM4256FL8-15†		150	260		2992	201			
	TM4256FL8-20†		200	330		2552	201			
2048K	TM4256GU8-12†	256K X 8	120	230	5	3432	201	30	Socketable	5-205
	TM4256GU8-15†		150	260		2992	201			
	TM4256GU8-20†		200	330		2552	201			
2048K	TM4256GP8-12†	256K X 8	120	230	5	3432	201	30	Low Profile, Socketable with Presence Detect	5-225
	TM4256GP8-15†		150	260		2992	201			
	TM4256GP8-20†		200	330		2552	201			
2048K	TM4256GV8-12†	256K X 8	120	230	5	3432	201	30	Low Profile, Leaded with Presence Detect	5-225
	TM4256GV8-15†		150	260		2992	201			
	TM4256GV8-20†		200	330		2552	201			
2048K	TM4256HE4-12†	512K X 4	120	230	5	1716	99	24	Leaded	5-233
	TM4256HE4-15†		150	260		1496	99			
	TM4256HE4-20†		200	330		1276	99			
2304K	TM4256EL9-12†	256K X 9	120	230	5	3861	226	30	Leaded	5-137
	TM4256EL9-15†		150	260		3366	226			
	TM4256EL9-20†		200	330		2871	226			
2304K	TM4256GU9-12†	256K X 9	120	230	5	3861	226	30	Socketable with Presence Detect	5-137
	TM4256GU9-15†		150	260		3366	226			
	TM4256GU9-20†		200	330		2871	226			
2304K	TM4256GP9-12†	256K X 9	120	230	5	3861	226	30	Low Profile, Socketable with Presence Detect	5-229
	TM4256GP9-15†		150	260		3366	226			
	TM4256GP9-20†		200	330		2871	226			
2304K	TM4256GV9-12†	256K X 9	120	230	5	3861	226	30	Low Profile, Leaded with Presence Detect	5-229
	TM4256GV9-15†		150	260		3366	226			
	TM4256GV9-20†		200	330		2871	226			

†All 256K DRAM SIPs available with page-mode access (TM4256___) or nibble-mode access (TM4257___).

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EPROM SELECTION GUIDE

Density	Device Number	Organization	Process	Access Time Max (ns)	Cycle Time Min (ns)	Power Supply/ Tolerance (V)	Power Dissipation Max (mW)		Pins	Package†	Page
							Active	Standby			
32K	TMS2732A-17	4K X 8	NMOS	170	170	5 ± 5%	657	158	24	J	6-3
	TMS2732A-20			200	200						
	TMS2732A-25			250	250						
	TMS2732A-45			450	450						
64K	TMS2764-17	8K X 8	NMOS	170	170	5 ± 5%	788	184	28	J	6-11
	TMS2764-20			200	200						
	TMS2764-25			250	250						
	TMS2764-45			450	450						
64K	TMS27C64-1‡	8K X 8	CMOS	150	150	5 ± 5%	210	1.4	28	J	6-21
	TMS27C64-15‡			150	150	5 ± 10%	220				
	TMS27C64-2‡			200	200	5 ± 5%	210				
	TMS27C64-20‡			200	200	5 ± 10%	220				
	TMS27C64‡			250	250	5 ± 5%	210				
	TMS27C64-25‡			250	250	5 ± 10%	220				
	TMS27C64-3‡			300	300	5 ± 5%	210				
	TMS27C64-30‡			300	300	5 ± 10%	220				
	TMS27C64-4‡			450	450	5 ± 5%	210				
	TMS27C64-45‡			450	450	5 ± 10%	220				
128K	TMS27C128-1	16K X 8	CMOS	150	150	5 ± 5%	210	1.4	28	J	6-29
	TMS27C128-15			150	150	5 ± 10%	220				
	TMS27C128-2			200	200	5 ± 5%	210				
	TMS27C128-20			200	200	5 ± 10%	220				
	TMS27C128			250	250	5 ± 5%	210				
	TMS27C128-25			250	250	5 ± 10%	220				
	TMS27C128-3			300	300	5 ± 5%	210				
	TMS27C128-30			300	300	5 ± 10%	220				
	TMS27C128-4			450	450	5 ± 5%	210				
	TMS27C128-45			450	450	5 ± 10%	220				
256K	TMS27C256-1	32K X 8	CMOS	170	170	5 ± 5%	210	1.4	28	J	6-37
	TMS27C256-17			170	170	5 ± 10%	220				
	TMS27C256-2			200	200	5 ± 5%	210				
	TMS27C256-20			200	200	5 ± 10%	220				
	TMS27C256			250	250	5 ± 5%	210				
	TMS27C256-25			250	250	5 ± 10%	220				
	TMS27C256-3			300	300	5 ± 5%	210				
	TMS27C256-30			300	300	5 ± 10%	220				
	TMS27C256-4			450	450	5 ± 5%	210				
	TMS27C256-45			450	450	5 ± 10%	220				

Continued next page.

†J = Ceramic DIP

‡Advance information for product under development by TI.

EPROM SELECTION GUIDE (CONCLUDED)

Density	Device Number	Organization	Process	Access Time Max (ns)	Cycle Time Min (ns)	Power Supply/ Tolerance (V)	Power Dissipation Max (mW)		Pins	Package†	Page
							Active	Standby			
512K	TMX27C512-2‡	64K X 8	CMOS	200	200	5 ± 5%	263	1.4	28	J	6-45
	TMX27C512-20‡			200	200	5 ± 10%	275				
	TMX27C512‡			250	250	5 ± 5%	263				
	TMX27C512-25‡			250	250	5 ± 10%	275				
	TMX27C512-3‡			300	300	5 ± 5%	263				
	TMX27C512-30‡			300	300	5 ± 10%	275				
	TMX27C512-4‡			450	450	5 ± 5%	263				
	TMX27C512-45‡			450	450	5 ± 10%	275				

†J = Ceramic DIP
‡ Preliminary Target Specifications for product under development by TI.

PROM (OTP) SELECTION GUIDE

Density	Device Number	Organization	Process	Access Time Max (ns)	Cycle Time Min (ns)	Power Supply/ Tolerance (V)	Power Dissipation Max (mW)		Pins	Package†	Page
							Active	Standby			
32K	TMS27P32A-25	4K X 8	NMOS	250	250	5 ± 5%	657	158	24	N	6-47
	TMS27P32A-30			300	300						
	TMS27P32A-45			450	450						
64K	TMS27P64-25	8K X 8	NMOS	250	250	5 ± 5%	788	184	28	N	6-53
	TMS27P64-30			300	300						
	TMS27P64-45			450	450						
128K	TMX27PC128-2‡	16K X 8	CMOS	200	200	5 ± 5%	210	1.4	28	N	6-61
	TMX27PC128-20‡			200	200	5 ± 10%	220				
	TMX27PC128‡			250	250	5 ± 5%	210				
	TMX27PC128-25‡			250	250	5 ± 10%	220				
	TMX27PC128-3‡			300	300	5 ± 5%	210				
	TMX27PC128-30‡			300	300	5 ± 10%	220				
	TMX27PC128-4‡			450	450	5 ± 5%	210				
	TMX27PC128-45‡			450	450	5 ± 10%	220				
256K	TMX27PC256-2‡	32K X 8	CMOS	200	200	5 ± 5%	210	1.4	28	N	6-63
	TMX27PC256-20‡			200	200	5 ± 10%	220				
	TMX27PC256‡			250	250	5 ± 5%	210				
	TMX27PC256-25‡			250	250	5 ± 10%	220				
	TMX27PC256-3‡			300	300	5 ± 5%	210				
	TMX27PC256-30‡			300	300	5 ± 10%	220				
	TMX27PC256-4‡			450	450	5 ± 5%	210				
	TMX27PC256-45‡			450	450	5 ± 10%	220				

†N = Plastic DIP
‡ Preliminary Target Specifications for products under development by TI.

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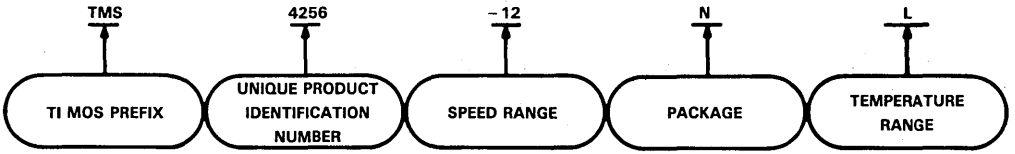
ROM SELECTION GUIDE

Density	Device Number	Organization	Process	Access Time Max (ns)	Cycle Time Min (ns)	Power Supply (V)	Power Dissipation Max (mW)		Pins	Package†	Page
							Active	Standby			
32K	TMS2332-15 TMS2332-20 TMS2332-25	4K X 8	NMOS	150 200 250	150 200 250	5	330	83	24	N	7-3
32K	TMS4732-15 TMS4732-20 TMS4732-25	4K X 8	NMOS	150 200 250	150 200 250	5	330	83	24	N	7-15
64K, JEDEC Approved Pinout	TMS2364-15 TMS2364-20 TMS2364-25	8K X 8	NMOS	150 200 250	150 200 250	5	330	83	28	N	7-9
64K	TMS4764-15 TMS4764-20 TMS4764-25	8K X 8	NMOS	150 200 250	150 200 250	5	330	83	24	N	7-21
128K	TMS47128-20 TMS47128-25 TMS47128-35	16K X 8	NMOS	200 250 350	200 250 350	5	330	83	28	N	7-27
256K	TMS47256-20 TMS47256-25 TMS47256-35	32K X 8	NMOS	200 250 350	200 250 350	5	330	83	28, 32	N, FM	7-33
256K	TMS47C256-15‡ TMS47C256-20‡ TMS47C256-25‡	32K X 8	CMOS	150 200 250	150 200 250	5	220	3	28, 32	N, FM	7-39
512K	TMS47C512-20‡ TMS47C512-25‡ TMS47C512-30‡	64K X 8	CMOS	200 250 300	200 250 300	5	TBD	TBD	28, 32	N, FM	7-45
1024K	TMS47C1024-20‡ TMS47C1024-25‡ TMS47C1024-30‡	128K X 8	CMOS	200 250 300	200 250 300	5	TBD	TBD	28, 32	N, FM	7-51

†N = Plastic DIP
FM = Plastic Chip Carrier
‡Advance Information for products under development by TI.

PART I — ALTERNATE VENDOR PART NUMBERING (EXAMPLES) BASED ON AVAILABLE PUBLISHED DATA

TEXAS INSTRUMENTS (TI)



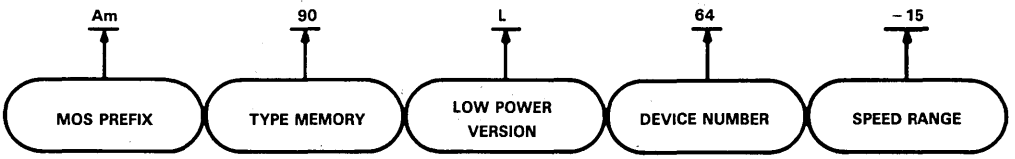
TMS Commercial MOS
SMJ Military MOS
TMX Pre-production MOS

Max Access	
- 4 45 ns	-20 200 ns
- 5 55 ns	-25 250 ns
- 7 70 ns	-30 300 ns
-10 100 ns	-35 350 ns
-12 120 ns	-45 450 ns
-15 150 ns	

DJ Plastic SOJ
FE Ceramic Chip Carrier
FG Ceramic Chip Carrier
FM Plastic Chip Carrier
FP Plastic Chip Carrier
J Cerpak/Cerdip
JD Side Braze
N Plastic DIP

E -40°C to 85°C
L 0°C to 70°C
M -55°C to 125°C
S -55°C to 100°C

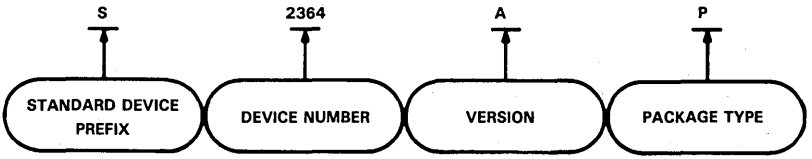
ADVANCED MICRO DEVICES (AMD)



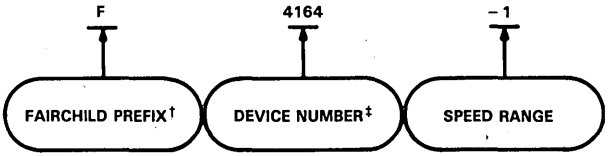
90 DRAM
91 MOS RAM
92 MOS
27 EPROM

Max Access
-2 200 ns -10 100 ns
-3 300 ns -15 150 ns
-4 450 ns -20 200 ns

AMERICAN MICROSYSTEMS, INC. (AMI)



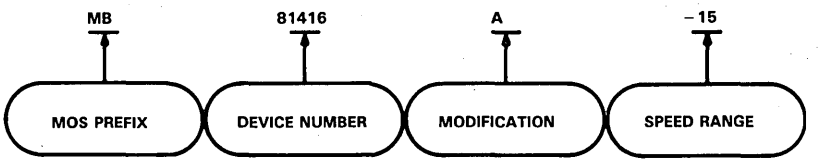
FAIRCHILD



Max Access	
-1	120 ns
-2	150 ns
-3	200 ns
-4	250 ns

†May be omitted.
‡Inclusion of an "L" indicates low-power version.

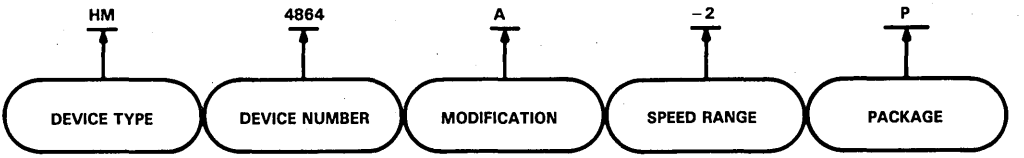
FUJITSU



MB Fujitsu
MBM Industry Standard Prefix

Max Access	
-10	100 ns
-12	120 ns
-15	150 ns

HITACHI



HM RAM
HN ROM

Max Access			
-1	Fastest	-15	150 ns
-2		-20	200 ns
-3		-25	250 ns
-4	Slowest	-30	300 ns
-12	120 ns	-45	450 ns

P Plastic

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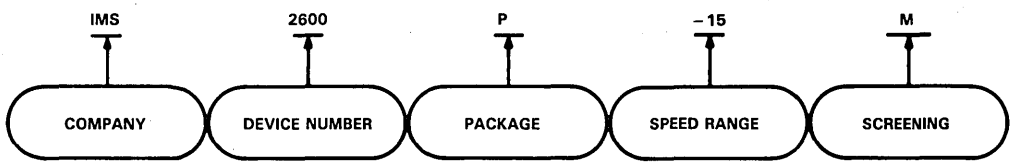
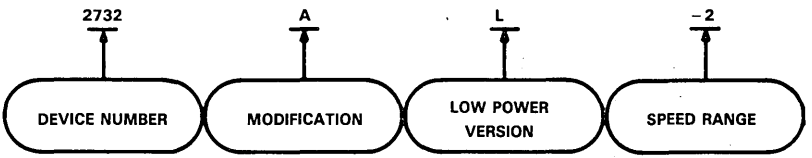
INMOS



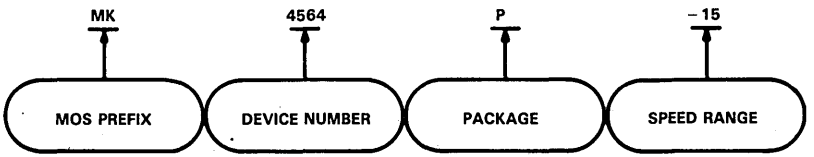
PACKAGE	SPEED RANGE		SCREENING
		Max Access	
P Plastic DIP	-45	45 ns	Blank Commercial
S Ceramic DIP	-55	55 ns	M MIL-883B
	-10	100 ns	E Extended
	-12	120 ns	Temperature
	-15	150 ns	

INTEL



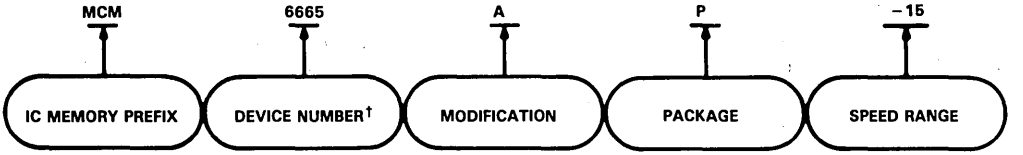
SPEED RANGE	Max Access
-10	100 ns
-12	120 ns
-2	200 ns
-3	300 ns
-4	450 ns

MOSTEK



MOS PREFIX	DEVICE NUMBER	PACKAGE	SPEED RANGE			
				Max Access		
MK Standard Prefix	4___ RAM	P Sidebrazed ceramic DIP	-8	80 ns	-15	150 ns
MKB Military Prefix		N Plastic	-10	100 ns	-20	200 ns
		E Ceramic Leadless Chip Carrier	-12	120 ns	-25	250 ns

MOTOROLA



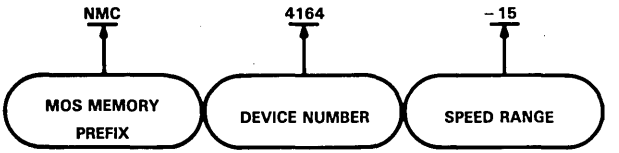
P Plastic

Max Access

–10	100 ns	–25	250 ns
–12	120 ns	–30	300 ns
–15	150 ns	–45	450 ns
–20	200 ns		

†Inclusion of an "L" indicates low power version.

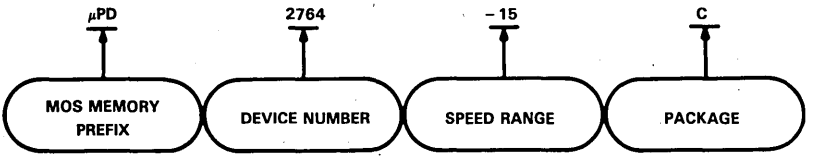
NATIONAL SEMICONDUCTOR



Max Access

–12	120 ns
–15	150 ns
–20	200 ns

NEC

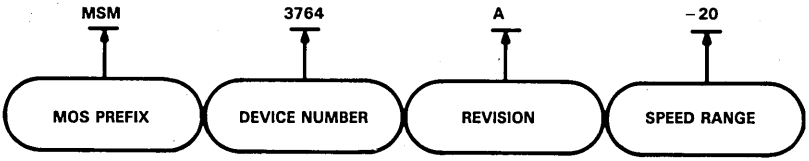


Max Access

–10	100 ns	–20	200 ns
–12	120 ns	–25	250 ns
–15	150 ns	–30	300 ns

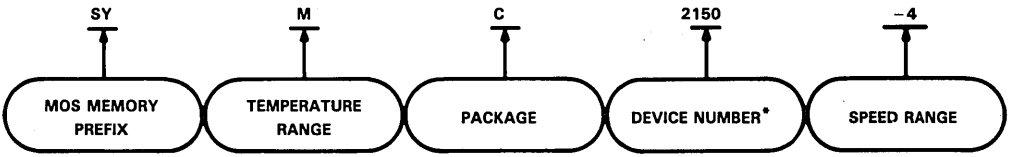
C Plastic DIP
D Ceramic DIP

OKI SEMICONDUCTOR (OKI)



Max Access
-10 100 ns
-12 120 ns
-15 150 ns
-20 200 ns

SYNERTEK

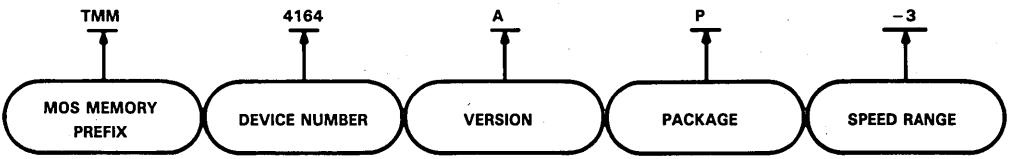


C Ceramic
P Molded

Max Access
-2 200 ns
-3 300 ns
-4 45 ns
-5 55 ns

*Inclusion of an alpha character indicates a device modification.

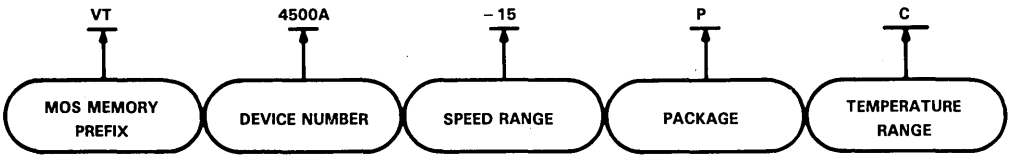
TOSHIBA



P Plastic
C Ceramic

Max Access
-12 120 ns
-15 150 ns
-20 200 ns
-25 250 ns

VLSI TECHNOLOGY



Max Access
-15 150 ns
-20 200 ns
-25 250 ns

C Commercial
M Military

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PART II — ALTERNATE SOURCES†

DYNAMIC RAMS

ORGANIZATION	VENDOR		PART NUMBER
	TI	ALTERNATE SOURCES	
16K X 1 (3 Supply)	TI		TMS4116
		AMD	AM9016F
		ITT	ITT4116
		Mostek	MK4116
		Motorola	MCM4116B
		National	MM5290
		NEC	μPD416
		Toshiba	TMM416
64K X 1 (5 V)	TI		TMS4164‡
		AMD	AM9064
		Fairchild	F64K
		Fujitsu	MB8264A/MB8265A
		Hitachi	HM4864/HM4864A
		Inmos	IMS2600‡
		Intel	2164A
		Matsushita	MN4164
		Micron Tech.	MT4264‡
		Mitsubishi	M5K4164
		Mostek	MK4564
		Motorola	MCM6665A
		National	NMC4164‡
		NEC	μPD4164
		Oki	MSM3764
		Siemens	HYB4164
		Toshiba	TMM4164
		TRISTAR	KM4164A
64 K X 1 Multiport Video RAM (5 V)	TI		TMS4161
		AT&T	M51064PX
16K X 4 (5 V)	TI		TMS4416
		Fujitsu	MB81416
		Hitachi	HM48416A
		Inmos	IMS2620
		Mitsubishi	M5M4416

Continued next page.

†Based on available published data. (Official alternate sourcing agreements not necessarily implied.) All devices listed operate over the 0°C to 70°C temperature range.

‡These devices have a 256 cycle, 4 ms refresh scheme. All others refresh in 2 ms.

DYNAMIC RAMS (CONCLUDED)

ORGANIZATION	VENDOR		PART NUMBER
	TI	ALTERNATE SOURCES	
256K X 1	TI		TMS4256/TMS4257
		Fujitsu	MB81257/MB81256
		Hitachi	HM50256/HM50257
		Micron Tech.	MT1256
		Mitsubishi	M5M4256
		Motorola	MCM6256
		NEC	μPD41256/μPD41257
		Oki	MSM37256
		Toshiba	TMM41256
		Western Electric	WCM41256
64K X 4 (5 V)	TI		TMS4464
		Hitachi	HM50464/HM50465
		Micron Tech.	MT4064
		NEC	μPD41256

EPROMS

ORGANIZATION	VENDOR		PART NUMBER
	TI	ALTERNATE SOURCES	
4K X 8 (5 V)	TI		TMS2732A
		AMD	Am2732
		Fujitsu	MBM2732A
		Hitachi	HN462732
		Intel	2732A
		Mitsubishi	M5L2732
		NEC	μPD2732
		Oki	MSM2732
		Toshiba	TMM2732
8K X 8 (5 V)	TI		TMS2764
		AMD	Am2764
		Fairchild	2764
		Fujitsu	MBM2764
		Hitachi	HN482764
		Intel	2764
		Mitsubishi	M5L2764
		NEC	μPD2764
		Oki	MSM2764A
		Seeq	2764
		Toshiba	TMM2764
8K X 8 (5 V)	TI		TMS27C64
		AMD	Am27C64
		Fujitsu	MBM27C64
		Hitachi	HN27C64
		Intel	27C64
		NEC	μPD27C64

Continued next page.

EPROMS (CONCLUDED)

ORGANIZATION	VENDOR		PART NUMBER
	TI	ALTERNATE SOURCES	
16K X 8 (5 V)	TI		TMS27C128
		AMD	Am27128A
		Fujitsu	MBM27128
		Hitachi	HN4827128
		Intel	27128
		Mitsubishi	M5L27128
		NEC	μPD27128
		Oki	MSM27128A
		Seeq	27128
		Toshiba	TMM27128
32K X 8 (5 V)	TI		TMS27C256
		AMD	Am27256
		Fujitsu	MBM27256
		Hitachi	HN27256
		Intel	27256/27C256
		National	NM27C256
		NEC	μPD27256/μPD27C256
		Seeq	27C256
		Toshiba	TC57256

ROMS

ORGANIZATION	VENDOR		PART NUMBER
	TI	ALTERNATE SOURCES	
4K X 8 (5 V)	TI		TMS4732
		AMD	Am9232
		GI	RO-3-9332
		Motorola	MCM68A332
		NEC	μPD2332
		Oki	MSM2932
		Signetics	2632A
		Synertek	SY2332
		Toshiba	TMM333
		VTI	VT2332
4K X 8 (5 V)	TI		TMS2332
		AMD	Am9233
		GI	RO9333
		Synertek	SY2333
		Toshiba	TMM2332
		VTI	VT2333
8K X 8 (5 V) 24 pin	TI		TMS4764
		AMD	Am9264C
		GI	RO9464C
		GTE Micro	G2364
		Mostek	MK36000
		Motorola	MCM68364
		NCR	NCR2364
		NEC	μPD2364
		Oki	MSM2965
		Rockwell	R2364A
		SGS	M2364
		Signetics	2664A
		Synertek	SY2364
		VTI	VT2364
8K X 8 (5 V) 28 pin	TI		TMS2364
		AMD	Am9265C
		GI	RO9864C
		Motorola	MCM68370
		NCR	NCR2365
		Rockwell	R2364B
		SGS	M37000
		Synertek	SY2365
		VTI	VT2365

Continued next page.

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ROMS (CONCLUDED)

ORGANIZATION	VENDOR		PART NUMBER
	TI	ALTERNATE SOURCES	
16K X 8 (5 V)	TI		TMS47128
		AMD	Am92128D
		EXEL	XLS23128
		GI	RO9128C
		Gould AMI	S23128B
		NCR	NCR23128
		NEC	μPD23128
		Oki	MSM38128A
		Sharp	LH23128
		Signetics	23128
		VTI	23128
32K X 8 (5 V)	TI		TMS47256
		AMD	Am92256
		EXEL	XLS23256
		Gould AMI	S23256C
		Mostek	MK38000
		NCR	NCR23256
		NEC	μPD23256
		Signetics	23256A
		Synertek	SY23256
		VTI	VT23256
32K X 8 (5 V)	TI		TMS47C256
		Fujitsu	MB83256
		GTE Micro	G53256
		Hitachi	HN613256H
		Motorola	MCM65256
		NCR	NCR23C256
		Oki	MSM53256
		RCA	CDM53256
		SMOS	SMM2325/SMM2326
		Toshiba	TMM23256
64 K X 8 (5 V)	TI		TMS47C512
		GI	RO9512
		Sharp	LH53512
		VTI	VT23512
128K X 8 (5 V)	TI		TMS47C1024
		GI	RO91000 (NMOS)
		Hitachi	HN62301
		NEC	μPD231000 (NMOS)

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PART I — GENERAL CONCEPTS AND TYPES OF MEMORIES

Address — Any given memory location in which data can be stored or from which it can be retrieved.

Automatic Chip-Select/Power Down — (see Chip Enable Input)

Bit — Contraction of Binary digIT, i.e., a 1 or a 0; in electrical terms the value of a bit may be represented by the presence or absence of charge, voltage, or current.

Byte — A word of 8 bits (see word)

Chip Enable Input — A control input to an integrated circuit that when active permits operation of the integrated circuit for input, internal transfer, manipulation, refreshing, and/or output of data and when inactive causes the integrated circuit to be in a reduced power standby mode.

Chip Select Input — Chip select inputs are gating inputs that control the input to and output from the memory. They may be of two kinds:

1. Synchronous—Clocked/latched with the memory clock. Affects the inputs and outputs for the duration of that memory cycle.
2. Asynchronous—Has direct asynchronous control of inputs and outputs. In the read mode, an asynchronous chip select functions like an output enable.

Column Address Strobe (CAS) — A clock used in dynamic RAMs to control the input of column addresses. It can be active high (CAS) or active low ($\overline{\text{CAS}}$).

Data — Any information stored or retrieved from a memory device.

Dynamic (Read/Write) Memory (DRAM) — A read/write memory in which the cells require the repetitive application of control signals in order to retain the stored data.

NOTES:
1. The words "read/write" may be omitted from the term when no misunderstanding will result.
2. Such repetitive application of the control signals is normally called a refresh operation.
3. A dynamic memory may use static addressing or sensing circuits.
4. This definition applies whether the control signals are generated inside or outside the integrated circuit.

Electrically Alterable Read-Only Memory (EAROM) — A nonvolatile memory that can be field-programmed like a PROM or EPROM, but that can be electrically erased by a combination of electrical signals at its inputs.

Erasable and Programmable Read-Only Memory (EPROM)/Reprogrammable Read-Only Memory — A field-programmable read-only memory that can have the data content of each memory cell altered more than once.

Erase — Typically associated with EPROMs and EAROMs. The procedure whereby programmed data is removed and the device returns to its unprogrammed state.

Field-Programmable Read-Only Memory — A read-only memory that after being manufactured, can have the data content of each memory cell altered.

Fixed Memory — A common term for ROMs, EPROMs, EAROMs, etc., containing data that is not normally changed. A more precise term for EPROMs and EAROMs is nonvolatile since their data may be easily changed.

Fully Static RAM — In a fully static RAM, the periphery as well as the memory array is fully static. The periphery is thus always active and ready to respond to input changes without the need for clocks. There is no precharge required for static periphery.

K — When used in the context of specifying a given number of bits of information, $1K = 2^{10} = 1024$ bits. Thus, $64K = 64 \times 1024 = 65{,}536$ bits.

Large-Scale Integration (LSI) — The description of any IC technology that enables condensing more than 100 gates onto a single chip.

Mask-Programmed Read-Only Memory — A read-only memory in which the data content of each cell is determined during manufacture by the use of a mask, the data content thereafter being unalterable.

Memory — A medium capable of storage of information from which the information can be retrieved.

Memory Cell — The smallest subdivision of a memory into which a unit of data has been or can be entered, in which it is or can be stored, and from which it can be retrieved.

Metal-Oxide Semiconductor (MOS) — The technology involving photolithographic layering of metal and oxide to produce a semiconductor device.

NMOS — A type of MOS technology in which the basic conduction mechanism is governed by electrons. (Short for N-channel MOS)

Nonvolatile Memory — A memory in which the data content is maintained whether the power supply is connected or not.

Output Enable — A control input that, when true, permits data to appear at the memory output, and when false, causes the output to assume a high-impedance state. (See also chip select)

PMOS — A type of MOS technology in which the basic conduction mechanism is governed by holes. (Short for P-channel MOS)

Parallel Access — A feature of a memory by which all the bits of a byte or word are entered simultaneously at several inputs or retrieved simultaneously from several outputs.

Power Down — A mode of a memory device during which the device is operating in a low-power or standby mode. Normally read or write operations of the memory are not possible under this condition.

Program — Typically associated with EPROM memories, the procedure whereby logical 0's (or 1's) are stored into various desired locations in a previously erased device.

Program Enable — An input signal that when true, puts a programmable memory device into the program mode.

Programmable Read-Only Memory (PROM) — A memory that permits access to any of its address locations in any desired sequence with similar access time to each location.
NOTE: The term as commonly used denotes a read/write memory.

Read — A memory operation whereby data is output from a desired address location.

Read-Only Memory (ROM) — A memory in which the contents are not intended to be altered during normal operation.
NOTE: Unless otherwise qualified, the term "read-only memory" implies that the content is determined by its structure and is unalterable.

Read/Write Memory — A memory in which each cell may be selected by applying appropriate electrical input signals and the stored data may be either (a) sensed at appropriate output terminals, or (b) changed in response to other similar electrical input signals.

Row Address Strobe (RAS) — A clock used in dynamic RAMs to control the input of the row addressed. It can be active high (RAS) or active low ($\overline{\text{RAS}}$).

Scaled-MOS (SMOS) — MOS technology under which the device is scaled down in size in three dimensions and in operating voltages allowing improved performance.

Semi-Static (Quasi-Static, Pseudo-Static) RAM — In a semi-static RAM, the periphery is clock-activated (i.e., dynamic). Thus the periphery is inactive until clocked, and only one memory cycle is permitted per clock. The peripheral circuitry must be allowed to reset after each active memory cycle for a minimum precharge time. No refresh is required.

Serial Access — A feature of a memory by which all the bits are entered sequentially at a single input or retrieved sequentially form a single output.

Static RAM (SRAM) — A read/write random-access device within which information is stored as latched voltage levels. The memory cell is a static latch that retains data as long as power is applied to the memory array. No refresh is required. The type of periphery circuitry sub-categorizes static RAMS.

Very-Large-Scale Integration (VLSI) — The description of any IC technology that is much more complex than large-scale integration (LSI), and involves a much higher equivalent gate count. At this time an exact definition including a minimum gate count has not been standardized by JEDEC or the IEEE.

Volatile Memory — A memory in which the data content is lost when power supplied is disconnected.

Word — A series of one or more bits that occupy a given address location and that can be stored and retrieved in parallel.

Write — A memory operation whereby data is written into a desired address location.

Write Enable — A control signal that when true causes the memory to assume the write mode, and when false causes it to assume the read mode.

PART II — OPERATING CONDITIONS AND CHRACTERISTICS (INCLUDING LETTER SYMBOLS)

Capacitance

The inherent capacitance on every pin, which can vary with various inputs and outputs.

Example symbology:

C_i	Input capacitance
C_o	Output capacitance
$C_{i(D)}$	Input capacitance, data input

Current

High-level input current, I_{IH}
The current into an input when a high-level voltage is applied to that input.

High-level output current, I_{OH}
The current into* an output with input conditions applied that according to the product specification will establish a high level at the output.

Low-level input current, I_{IL}
The current into an input when a low-level voltage is applied to that input.

Low-level output current, I_{OL}
The current into* an output with input conditions applied that according to the product specification will establish a low level at the output.

Off-state (high-impedance-state) output current (of a three-state output), I_{OZ}
The current into* an output having three-state capability with input conditions applied that according to the product specification will establish the high-impedance state at the output.

Short-circuit output current, I_{OS}
The current into* an output when the output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potential).

Supply current, I_{BB}, I_{CC}, I_{DD}, I_{PP}
The current into, respectively, the V_{BB}, V_{CC}, V_{DD}, V_{PP} supply terminals.

*Current out of a terminal is given as a negative value.

Operating Free-Air Temperature

The temperature (T_A) range over which the device will operate and meet the specified electrical characteristics.

Operating Case Temperature

The case temperature (T_C) range over which the device will operate and meet the specified electrical characteristics.

Voltage

High-level input voltage, V_{IH}

An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.

NOTE: A minimum is specified that is the least positive value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.

High-level output voltage, V_{OH}

The voltage at an output terminal with input conditions applied that according to the product specification will establish a high level at the output.

Low-level input voltage, V_{IL}

An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables.

NOTE: A maximum is specified that is the most positive value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

Low-level output voltage, V_{OL}

The voltage at an output terminal with input conditions applied that according to the product specification will establish a low level at the output.

Supply voltages, V_{BB}, V_{CC}, V_{DD}, V_{PP}

The voltages supplied to the corresponding voltage pins that are required for the device to function. From one to four of these supplies may be necessary, along with ground, V_{SS}.

Time Intervals

New or revised data sheets in this book use letter symbols in accordance with standards recently adopted by JEDEC, the IEEE, and the IEC. Two basic forms are used. The first form is usually used in this book when intervals can easily be classified as access, cycle, disable, enable, hold, refresh, setup, transition, or valid times and for pulse durations. The second form can be used generally but in this book is used primarily for time intervals not easily classifiable. The second (unclassified) form will be described first. Since some manufacturers use this form for all time intervals, symbols in the unclassified form are given with the examples for most of the classified time intervals.

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Unclassified time intervals

Generalized letter symbols can be used to identify almost any time interval without classifying it using traditional or contrived definitions. Symbols for unclassified time intervals identify two signal events listed in from-to sequence using the format:

$$t_{AB\text{-}CD}$$

Subscripts A and C indicate the names of the signals for which changes of state or level or establishment of state or level constitute signal events assumed to occur first and last, respectively, that is, at the beginning and end of the time interval. Every effort is made to keep the A and C subscript length down to one letter, if possible (e.g., R for $\overline{RAS}$ and C for $\overline{CAS}$ of TMS4116).

Subscripts B and D indicate the direction of the transitions and/or the final states or levels of the signals represented by A and C, respectively. One or two of the following is used:

H = high or transition to high
L = low or transition to low
V = a valid steady-state level
X = unknown, changing, or "don't care" level
Z = high-impedance (off) state

The hyphen between the B and C subscripts is omitted when no confusion is likely to occur.

For examples of symbols of this type, see TMS4116 (e.g., t_{RLCL}).

Classified time intervals (general comments, specific times follow)

Because of the information contained in the definitions, frequently the identification of one or both of the two signal events that begin and end the intervals can be significantly shortened compared to the unclassified forms. For example, it is not necessary to indicate in the symbol that an access time ends with valid data at the output. However, if both signals are named (e.g., in a hold time), the from-to sequence is maintained.

Access time

The time interval between the application of a specific input pulse and the availability of valid signals at an output.

Example symbology:

Classified	Unclassified	Description
$t_{a(A)}$	t_{AVQV}	Access time from address
$t_{a(S)}$, $t_{a(CS)}$	t_{SLQV}	Access time from chip select (low)

Cycle time

The time interval between the start and end of a cycle.

NOTE: The cycle time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval that must be allowed for the digital circuit to perform a specified function (e.g., read, write, etc.) correctly.

Example symbology:

Classified	Unclassified	Description
$t_{c(R)}$, $t_{c(rd)}$	$t_{AVAV(R)}$	Read cycle time
$t_{c(W)}$	$t_{AVAV(W)}$	Write cycle time

NOTE: R is usually used as the abbreviation for "read"; however, in the case of dynamic memories, "rd" is used to permit R to stand for RAS.

Disable time (of a three-state output)

The time interval between the specified reference points on the input and output voltage waveforms, with the three-state output changing from either of the defined active levels (high or low) to a high-impedance (off) state.

Example symbology:

Classified	Unclassified	Description
$t_{dis(S)}$	t_{SHQZ}	Output disable time after chip select (high)
$t_{dis(W)}$	t_{WLQZ}	Output disable time after write enable (low)

These symbols supersede the older forms t_{PVZ} or t_{PXZ}.

Enable time (of a three-state output)

The time interval between the specified reference points on the input and output voltage waveforms, with the three-state output changing from a high-impedance (off) state to either of the defined active levels (high or low).

NOTE: For memories these intervals are often classified as access times.

Example symbology:

Classified	Unclassified	Description
$t_{en(SL)}$	t_{SLQV}	Output enable time after chip select low

These symbols supersede the older form t_{PZV}.

Hold time

The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.

NOTES:
1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.
2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is guaranteed.

Example symbology:

Classified	Unclassified	Description
$t_{h(D)}$	t_{WHDX}	Data hold time (after write high)
$t_{h(RHrd)}$	t_{RHWH}	Read (write enable high) hold time after $\overline{RAS}$ high)
$t_{h(CHrd)}$	t_{CHWH}	Read (write enable high) hold time after $\overline{CAS}$ high)
$t_{h(CLCA)}$	$t_{CL\text{-}CAX}$	Column address hold time after $\overline{CAS}$ low
$t_{h(RLCA)}$	$t_{RL\text{-}CAX}$	Column address hold time after $\overline{RAS}$ low
$t_{h(RA)}$	$t_{RL\text{-}RAX}$	Row address hold time (after $\overline{RAS}$ low)

These last three symbols supersede the older forms:

NEW FORM	OLD FORM
$t_{h(CLCA)}$	$t_{h(ACL)}$
$t_{h(RLCA)}$	$t_{h(ARL)}$
$t_{h(RA)}$	$t_{h(AR)}$

NOTE: The from-to sequence in the order of subscripts in the unclassified form is maintained in the classified form. In the case of hold times, this causes the order to seem reversed from what would be suggested by the terms.

Pulse duration (width)

The time interval between specified reference points on the leading and trailing edges of the pulse waveform.

Example symbology:

Classified	Unclassified	Description
$t_{w(W)}$	tWLWH	Write pulse duration
$t_{w(RL)}$	tRLRH	Pulse duration, $\overline{RAS}$ low

Refresh time interval

The time interval between the beginnings of successive signals that are intended to restore the level in a dynamic memory cell to its original level.

NOTE: The refresh time interval is the actual time interval between two refresh operations and is determined by the system in which the digital circuit operates. A maximum value is specified that is the longest interval for which correct operation of the digital circuit is guaranteed.

Example symbology:

Classified	Unclassified	Description
t_{rf}		Refresh time interval

Setup time

The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal.

NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.
2. The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is guaranteed.

Example symbology:

Classified	Unclassified	Description
$t_{su(D)}$	tDVWH	Data setup time (before write high)
$t_{su(CA)}$	tCAV-CL	Column address setup time (before $\overline{CAS}$ low)
$t_{su(RA)}$	tRAV-RL	Row address setup time (before $\overline{RAS}$ low)

Transition times (also called rise and fall times)

The time interval between two reference points (10% and 90% unless otherwise specified) on the same waveform that is changing from the defined low level to the defined high level (rise time) or from the defined high level to the defined low level (fall time).

Example symbology:

Classified	Unclassified	Description
t_t		Transition time (general)
$t_{t(CH)}$	tCHCH	Low-to-high transition time of $\overline{CAS}$
$t_{r(C)}$	tCHCH	$\overline{CAS}$ rise time
$t_{f(C)}$	tCLCL	$\overline{CAS}$ fall time

Valid time

(a) General

The time interval during which a signal is (or should be) valid.

(b) Output data-valid time

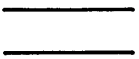
The time interval in which output data continues to be valid following a change of input conditions that could cause the output data to change at the end of the interval.

Example symbology:

Classified	Unclassified	Description
$t_{v(A)}$	tAXQX	Output data valid time after change of address.

This supersedes the older form t_{PVX}.

PART III — TIMING DIAGRAMS CONVENTIONS

TIMING DIAGRAM SYMBOL	MEANING: INPUT FORCING FUNCTIONS	MEANING: OUTPUT RESPONSE FUNCTIONS
	Must be steady high or low	Will be steady high or low
	High-to-low changes permitted	Will be changing from high to low some time during designated interval
	Low-to-high changes permitted	Will be changing from low to high sometime during designated interval
	Don't Care	State unknown or changing
	(Does not apply)	Centerline represents high-impedance (off) state.

PART IV — BASIC DATA SHEET STRUCTURE

The front page of the data sheet begins with a list of key *features* such as organization, interface, compatibility, operation (static or dynamic), access and cycle times, technology (N or P channel, silicon or metal oxide gate), and power. In addition, the top view of the device is shown with the *pinout* provided. Next a general *description* of the device, system interface considerations, and elaboration on other device characteristics are presented. The next section is an explanation of the device's *operation* which includes the function of each pin (i.e., the relationship between each input (output) and a given type of memory). The functions basically involve starting, achieving, and ending a given type of memory cycle (e.g., programming or erasing EPROMs, or reading a memory location).

Augmenting the descriptive text there appears a *logic symbol* prepared in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12 and explained in Section 10 of this book. Following the symbol is usually a *functional block diagram*, a flowchart of the basic internal structure of the device showing the signal paths for data, addresses, and control signals, as well as the internal architecture. Usually the next few pages contain the absolute maximum ratings (e.g., voltage supplies, input voltage, and temperature) applicable over the *operating free-air temperature range*. If the device is used outside of these values, it

may be permanently destroyed or at least it would not function as intended. Next, typically, are the *recommended operating conditions,* (e.g., supply voltages, input voltages, and operating temperature). The memory device is guaranteed to work reliably and to meet all data sheet parameters when operated in accord with the recommended operating conditions and within the specified timing. If the device is operated outside of these limits (minimum/maximum), the device's operation is no longer guaranteed to meet the data sheet parameters. Operation beyond the absolute maximum ratings as just described can result in catastrophic failures.

The next section provides a table of *electrical characteristics over full ranges of recommended operating conditions* (e.g., input and output currents, output voltages, etc.). These are presented as minimum, typical, and maximum values. Typical values are representative of operation at an ambient temperature of T_A = 25°C with all power supply voltages at nominal value. Next, input and output capacitances are presented. Each pin has a capacitance (whether an input, an output, or control pin). Minimum capacitances are not given, as the typical and maximum values are the most crucial.

The next few tables involve the device timing charateristics. The parameters are presented as minimum, typical (or nominal), and maximum. The *timing requirements over recommended supply voltage range and operating free-air temperature* indicate the device control requirements such as hold times, setup times, and transition times. These values are referenced to the relative positioning of signals on the timing diagrams, which follow. The *switching characteristics over recommended supply voltage range* are device performance characteristics inherent to device operation once the inputs are applied. These parameters are guaranteed for the test conditions given. The interrelationship of the timing requirements to the switching characteristics is illustrated in *timing diagrams* for each type of memory cycle (e.g., read, write, program.)

At the end of a data sheet additional *applications information* may be provided such as how to use the device, graphs of electrical characteristics, or other data on electrical characteristics.

ATTENTION

These devices contain circuits to protect the inputs and outputs against damage due to high static voltages or electrostatic fields; however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits.

Unused inputs must always be connected to an appropriate logic voltage level, preferably either supply voltage or ground.

Additional information concerning the handling of ESD sensitive devices is provided in Section 12 in a document entitled *"Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies."*

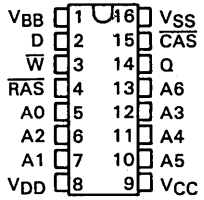
OCTOBER 1977—REVISED NOVEMBER 1985

- 16,384 X 1 Organization
- 10% Tolerance on All Supplies
- All Inputs Including Clocks TTL Compatible
- Unlatched Three-State Fully TTL-Compatible Output
- Performance Ranges:

	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	READ-MODIFY-WRITE† CYCLE (MIN)
TMS4116-15	150 ns	100 ns	375 ns	375 ns
TMS4116-20	200 ns	135 ns	375 ns	375 ns
TMS4116-25	250 ns	165 ns	410 ns	515 ns

- Page-Mode Operation for Faster Access Time
- Common I/O Capability with Early Write Feature
- Low-Power Dissipation
  - Operating . . . 462 mW (Max)
  - Standby . . . 20 mW (Max)
- 1-T Cell Design, N-Channel Silicon-Gate Technology
- 16-Pin 300-Mil (7,62-mm) Package Configuration

N PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A6	Addresses
$\overline{CAS}$	Column-Address Strobe
D	Data Input
Q	Data Output
$\overline{RAS}$	Row-Address Strobe
V_{BB}	−5-V Power Supply
V_{CC}	5-V Power Supply
V_{DD}	12-V Power Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The TMS4116 series is composed of monolithic high-speed dynamic 16,384-bit MOS random-access memories organized as 16,384 one-bit words, and employs single-transistor storage cells and N-channel silicon-gate technology.

All inputs and outputs are compatible with Series 74 TTL circuits including clocks: Row-Address Strobe $\overline{RAS}$ (or $\overline{R}$) and Column-Address Strobe $\overline{CAS}$ (or $\overline{C}$). All address lines (A0 through A6) and data in (D) are latched on chip to simplify system design. Data out (Q) is unlatched to allow greater system flexibility.

Typical power dissipation is less than 350 milliwatts active and 6 milliwatts during standby (V_{CC} is not required during standby operation). To retain data, only 10 milliwatts average power is required which includes the power consumed to refresh the contents of the memory.

The TMS4116 series is offered in a 16-pin dual-in-line plastic (N suffix) package and is guaranteed for operation from 0°C to 70°C. The package is designed for insertion in mounting-hole rows on 7,62-mm (300-mil) centers.

operation

address (A0-A6)

Fourteen address bits are required to decode 1 of 16,384 storage cell locations. Seven row-address bits are set up on pins A0 through A6 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the

†The term "read-write cycle" is sometimes used as an alternative to "read-modify-write cycle."

seven column-address bits are set up on pins A0 through A6 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$, data out will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data in ($\overline{D}$)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. This latch can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data out (Q)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan out of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle, the output goes active after the enable time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ is satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low; $\overline{CAS}$ going high returns it to a high-impedance state. In an early write cycle, the output is always in the high-impedance state. In a delayed-write or read-modify-write cycle, the output will follow the sequence for the read cycle.

refresh

A refresh operation must be performed at least every two milliseconds to retain data. Since the output buffer is in the high-impedance state unless $\overline{CAS}$ is applied, the $\overline{RAS}$-only refresh sequence avoids any output during refresh. Strobing each of the 128 row addresses (A0 through A6) with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ remains high (inactive) for this refresh sequence, thus conserving power.

page mode

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the chip. Thus, the time required to setup and strobe sequential row addresses on the same page is eliminated. To extend beyond the 128 column locations on a single RAM, the row address and $\overline{RAS}$ is applied to multiple 16K RAMs; $\overline{CAS}$ is decoded to select the proper RAM.

power up

V_{BB} must be applied to the device either before or at the same time as the other supplies and removed last. Failure to observe this precaution will cause dissipation in excess of the absolute maximum ratings due to internal forward bias conditions. This also applies to system use, where failure of the V_{BB} supply must immediately shut down the other supplies. After power up, eight $\overline{RAS}$ cycles must be performed to achieve proper device operation.

TEXAS INSTRUMENTS
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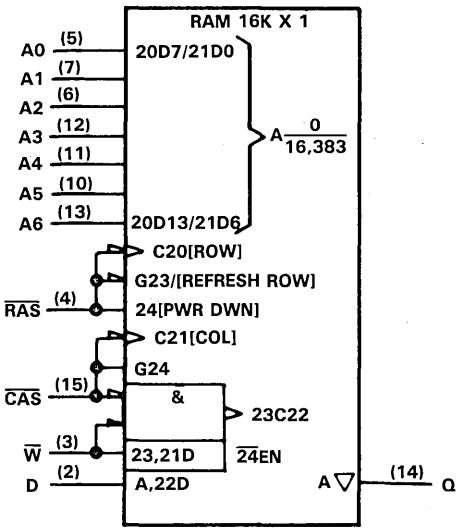
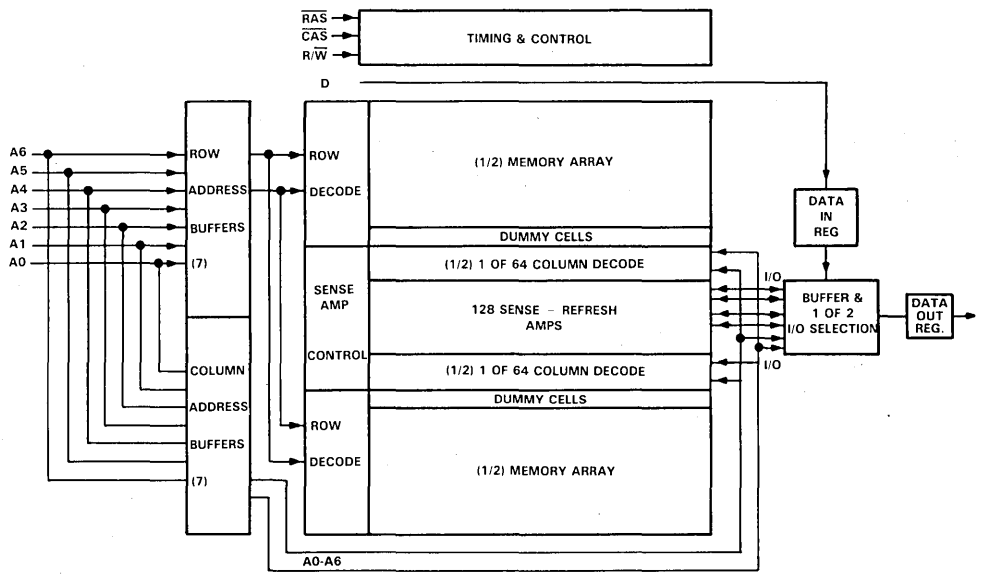
logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage on any pin (see Note 1) . . . . . −0.5 V to 20 V
Voltage on V_{CC}, V_{DD} supplies with respect to V_{SS} . . . . . −1 V to 15 V
Short circuit output current . . . . . 50 mA
Power dissipation . . . . . 1 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings, voltage values are with respect to the most-negative supply voltage, V_{BB} (substrate), unless otherwise noted. Throughout the remainder of this data sheet, voltage values are with respect to V_{SS}.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{BB}	Supply voltage		−4.5	−5	−5.5	V
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{DD}	Supply voltage		10.8	12	13.2	V
V_{SS}	Supply voltage			0		V
V_{IH}	High-level input voltage	All inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.4		7	V
		$\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.7		7	
V_{IL}	Low-level input voltage (see Note 2)		−1	0	0.8	V
T_A	Operating free-air temperature		0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as maximum, is used in this data sheet for logic voltage only.

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electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 7 V, All other pins = 0 V except V_{BB} = −5 V			10	μA
I_O	Output current (leakage)	V_O = 0 to 5.5 V, $\overline{CAS}$ high			±10	μA
I_{BB1}	Average operating current during read or write cycle	Minimum cycle time		50	200	μA
I_{CC1}‡					4§	mA
I_{DD1}				27	35	mA
I_{BB2}	Standby current	After 1 memory cycle $\overline{RAS}$ and $\overline{CAS}$ high		10	100	μA
I_{CC2}					±10	μA
I_{DD2}				0.5	1.5	mA
I_{BB3}	Average refresh current	Minimum cycle time $\overline{RAS}$ cycling, $\overline{CAS}$ high		50	200	μA
I_{CC3}					±10	μA
I_{DD3}				20	27	mA
I_{BB4}	Average page-mode current	Minimum cycle time $\overline{RAS}$ low, $\overline{CAS}$ cycling		50	200	μA
I_{CC4}‡					4§	mA
I_{DD4}				20	27	mA

† All typical values are at T_A = 25°C and nominal supply voltages.
‡ V_{CC} is applied only to the output buffer, so I_{CC} depends on output loading.
§ Output loading two standard TTL loads.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

PARAMETER		TYP†	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs	4	5	pF
$C_{i(D)}$	Input capacitance, data input	4	5	pF
$C_{i(RC)}$	Input capacitance, strobe inputs	8	10	pF
$C_{i(W)}$	Input capacitance, write enable input	8	10	pF
C_o	Output capacitance	5	7	pF

switching characteristics over recommended supply voltage range and operating free-air temperature range

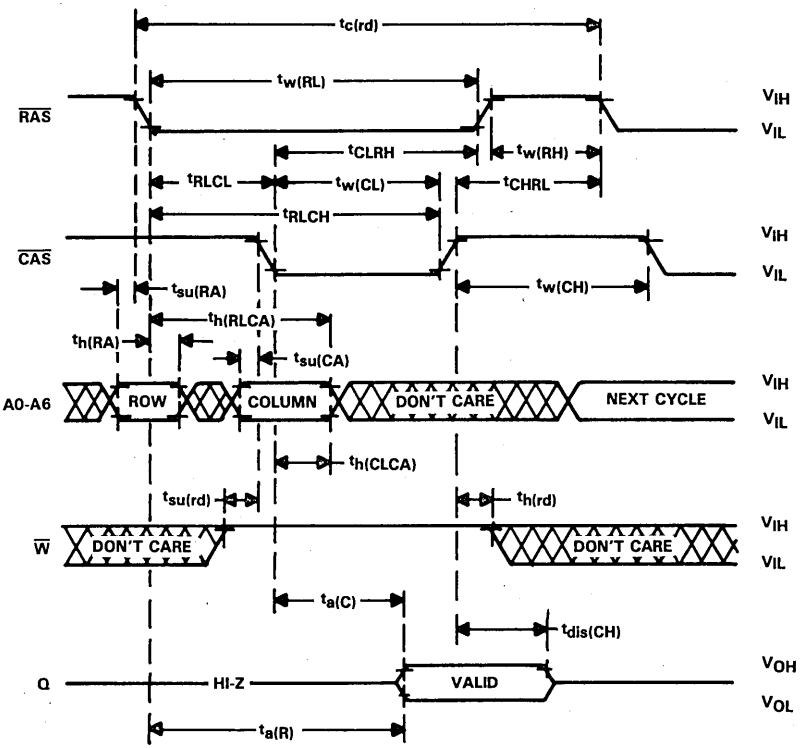
PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TMS4116-15		TMS4116-20		TMS4116-25		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		100		135		165	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, C_L = 100 pF, Load = 2 Series, 74 TTL gates	t_{RAC}		150		200		250	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	40	0	50	0	60	ns

† All typical values are at T_A = 25°C and nominal supply voltages.

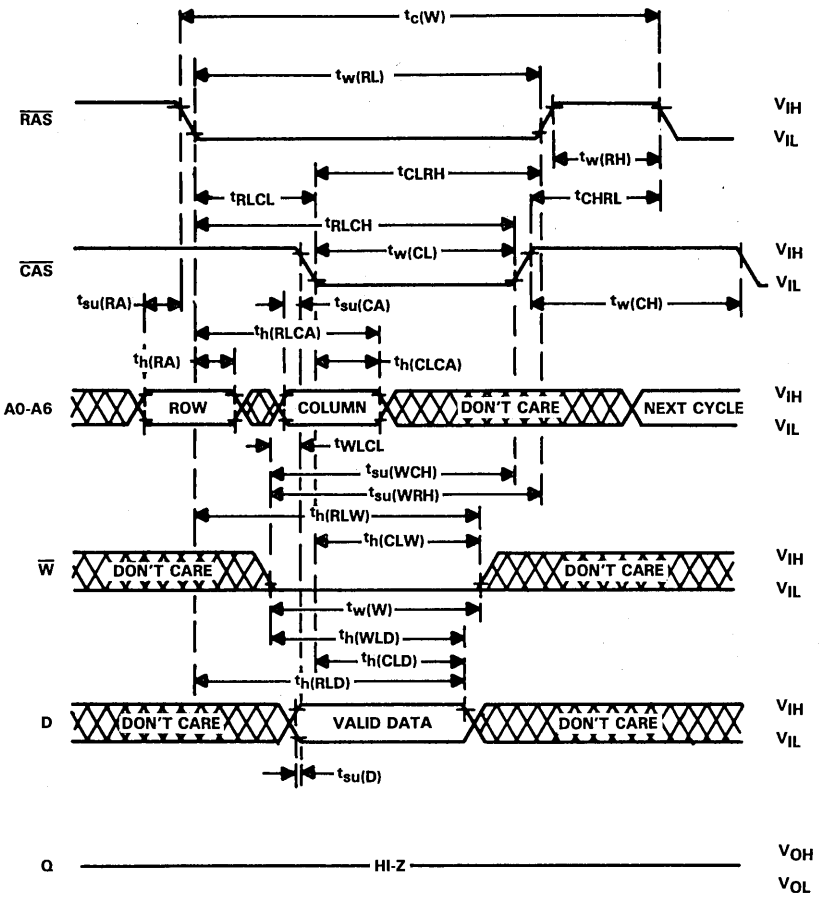
timing requirements over recommended supply voltage range and operating free-air temperature range

		ALT. SYMBOL	TMS4116-15		TMS4116-20		TMS4116-25		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(P)}$	Page-mode cycle time	t_{PC}	170		225		275		ns
$t_{c(rd)}$	Read cycle time	t_{RC}	375		375		410		ns
$t_{c(W)}$	Write cycle time	t_{WC}	375		375		410		ns
$t_{c(rdW)}$	Read-modify-write cycle time	t_{RWC}	375		375		515		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (precharge time)	t_{CP}	60		80		100		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low	t_{CAS}	100	10,000	135	10,000	165	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge time)	t_{RP}	100		120		150		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low	t_{RAS}	150	10,000	200	10,000	250	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	45		55		75		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and CAS	t_T	3	35	3	50	3	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	−10		−10		−10		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		0		0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	60		80		100		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	60		80		100		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	45		55		75		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	20		25		35		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	95		120		160		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DHC}	45		55		75		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	95		120		160		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DHW}	45		55		75		ns
$t_{h(rd)}$	Read-command hold time	t_{RCH}	0		0		0		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	45		55		75		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	95		120		160		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	150		200		250		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	−20		−20		−20		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	100		135		165		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write-cycle only)	t_{CWD}	70		95		125		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	20	50	25	65	35	85	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write-cycle only)	t_{RWD}	120		160		200		ns
t_{WLCL}	Delay time, W low to $\overline{CAS}$ low (early write cycle)	t_{WCS}	−20		−20		−20		ns
t_{rf}	Refresh time interval	t_{REF}		2		2		2	ms

read cycle timing



early write cycle timing



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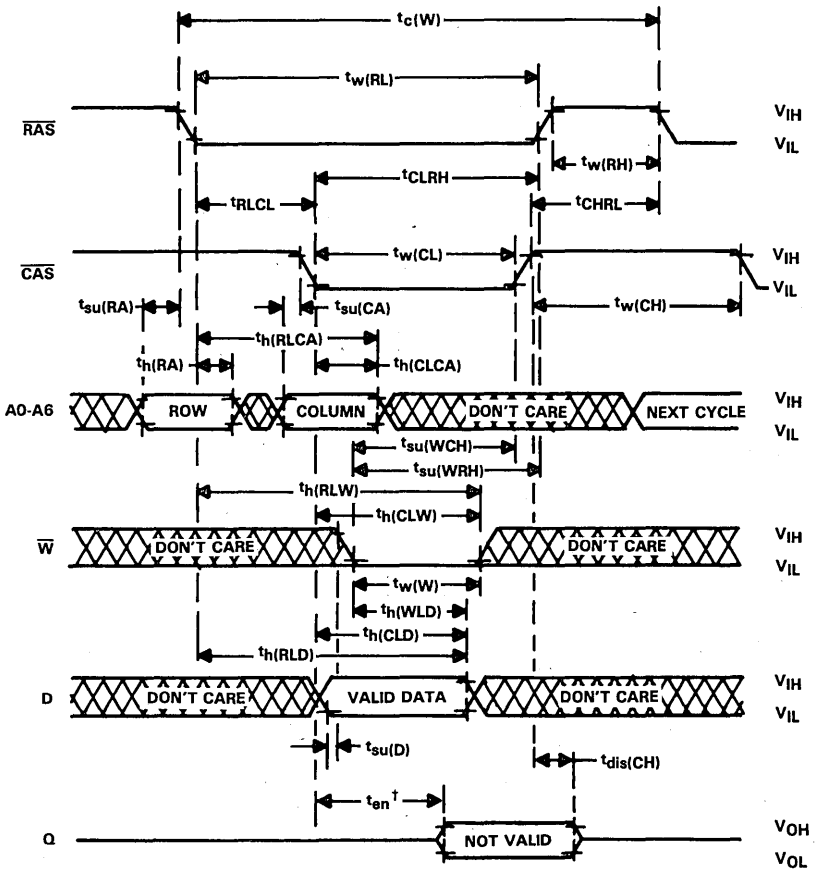
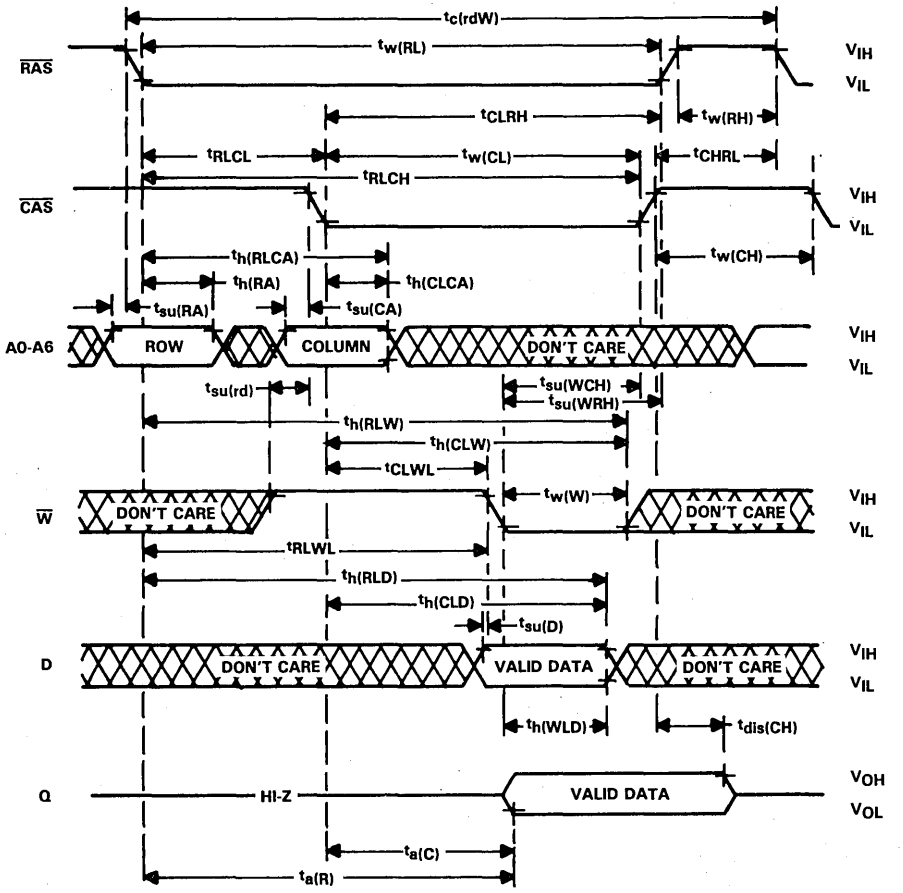
write cycle timing



† The enable time (t_{en}) for a write cycle is equal in duration to the access time from $\overline{CAS}$ ($t_{a(C)}$) in a read cycle; but the same active levels at the output are invalid.

read-write/read-modify-write cycle timing



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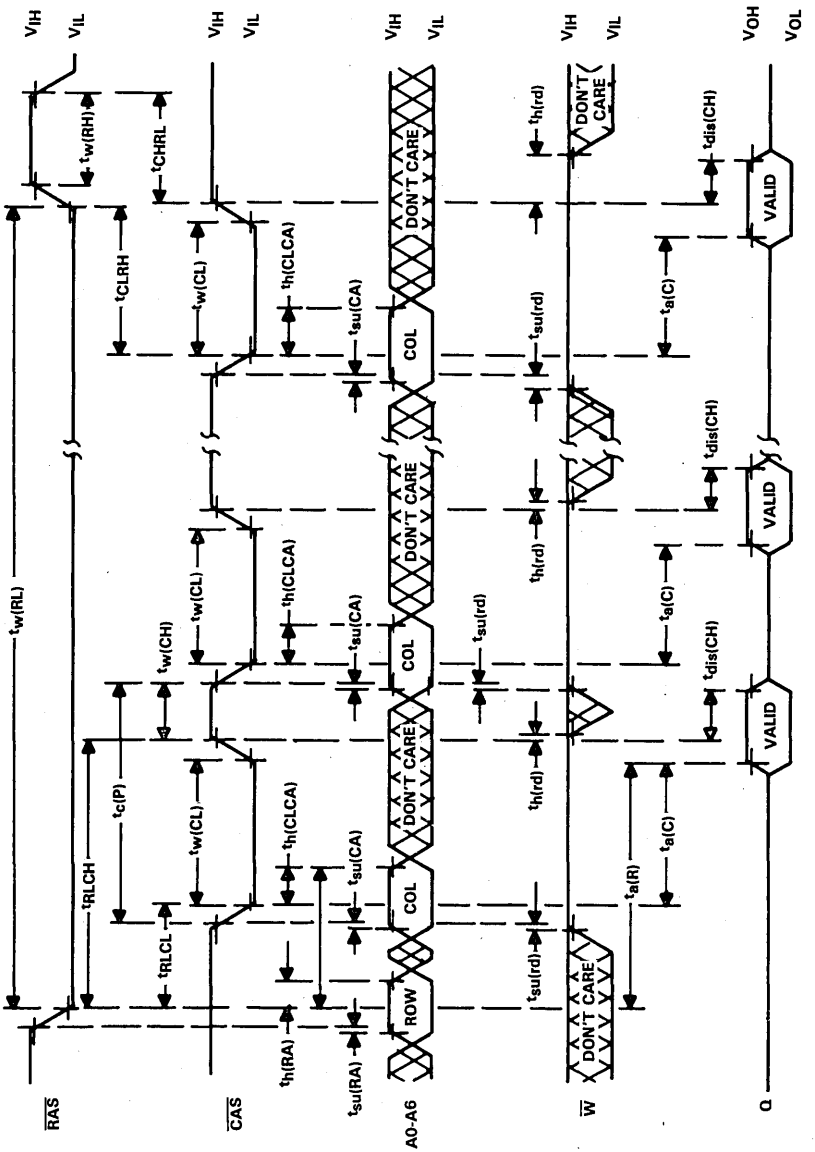
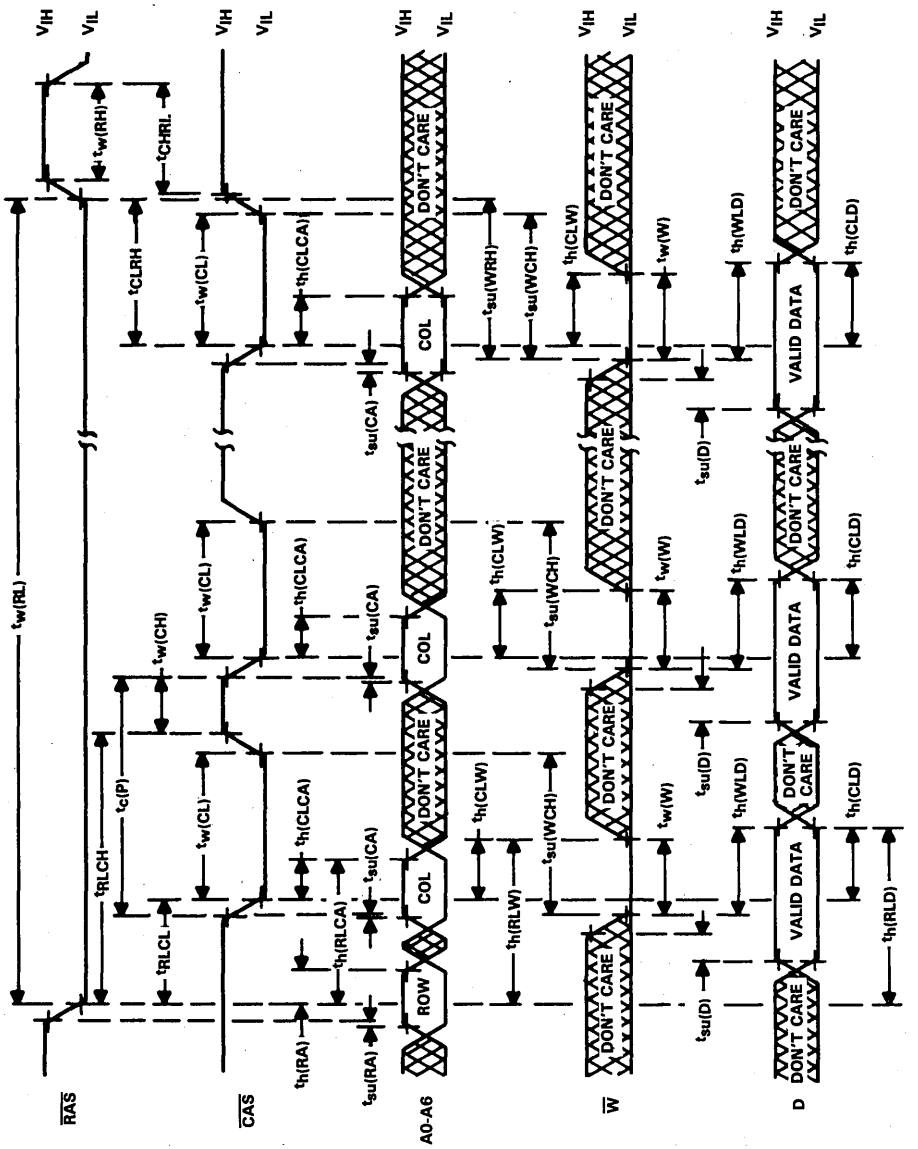
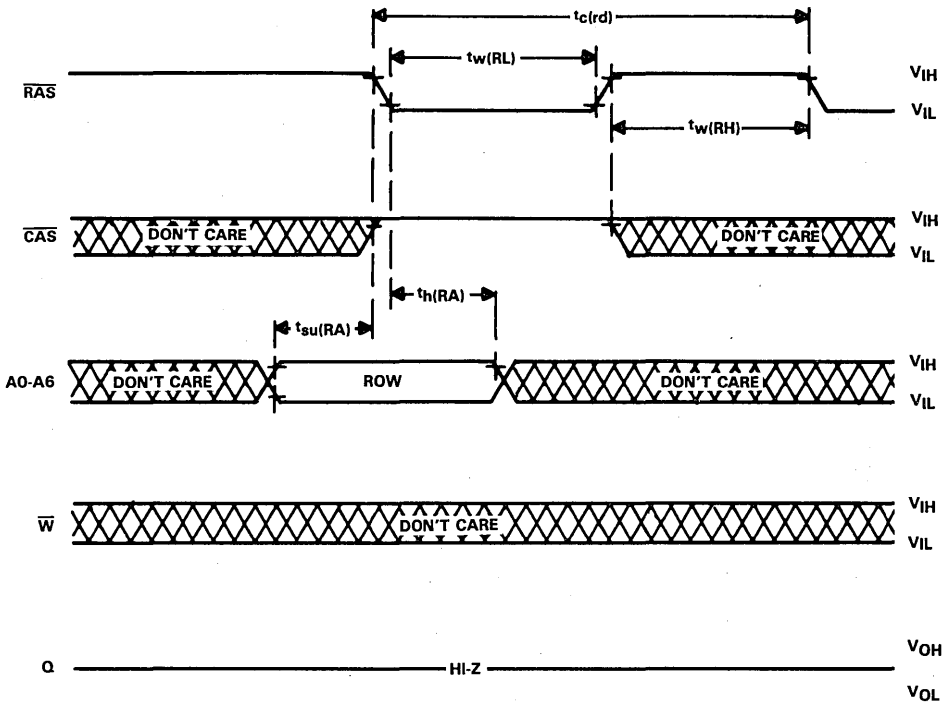
page-mode read cycle timing



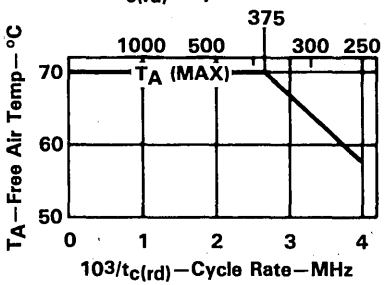
page-mode write cycle timing



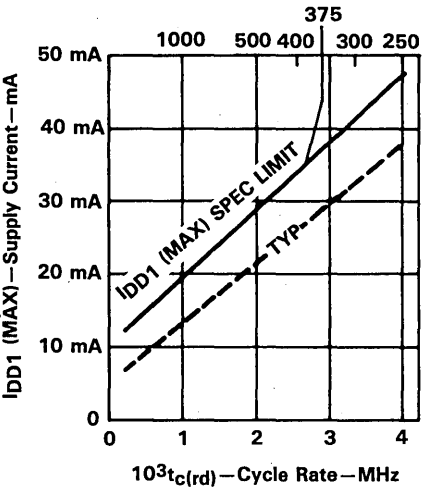
$\overline{\text{RAS}}$-only refresh timing



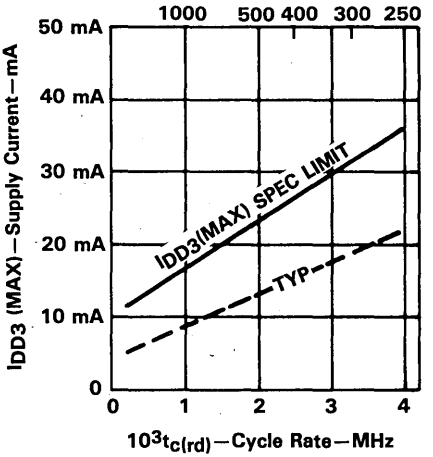
CYCLE RATE (& TIME)
vs
TEMPERATURE



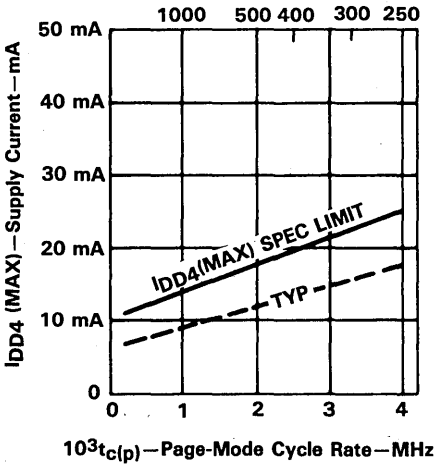
CYCLE RATE (& TIME)
vs
MAX SUPPLY CURRENT, I_{DD1}



CYCLE RATE (& TIME)
vs
MAX SUPPLY CURRENT, I_{DD3}



PAGE-MODE CYCLE RATE (& TIME)
vs
MAX SUPPLY CURRENT, I_{DD4}



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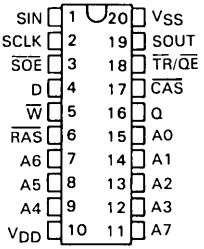
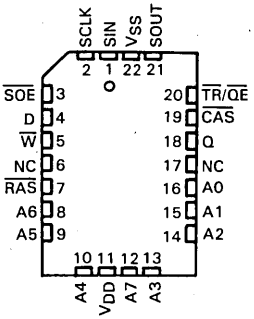
JULY 1983—REVISED NOVEMBER 1985

- Dual Accessibility — One Port Sequential Access, One Port Random Access
- Four Cascaded 64-Bit Serial Shift Registers for Sequential Access Applications
- Designed for Both Video and Non-Video Applications
- Fast Serial Port . . . Can Be Configured for Video Data Rates in Excess of 150 MHz
- $\overline{TR}/\overline{QE}$ as Output Enable Allows Direct Connection of D, Q and Address Lines to Simplify System Design
- Random Access Port Looks Exactly Like a TMS4164
- Separate Serial In and Serial Out to Allow Simultaneous Shift In and Out
- 65,536 × 1 Organization
- Supported by TI's TMS34061 Video System Controller (VSC)
- Maximum Access Time from $\overline{RAS}$ Less Than 150 ns
- Minimum Cycle Time (Read or Write) Less Than 240 ns
- Long Refresh Period . . . 4 ms
- Low Refresh Overhead Time . . . As Low As 1.7% of Total Refresh Period
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Unlatched Outputs for Both Random and Serial Access
- Common I/O Capability with "Early Write" Feature
- Page-Mode Operation for Faster Access
- Low Power Dissipation (TMS4161-15)
  —Operating . . . 250 mW (Typical)
  —Standby . . . 80 mW (Typical)
- New SMOS (Scaled-MOS) N-Channel Technology
- $\overline{SOE}$ Simplifies Multiplexing of Serial Data Streams
- Available with MIL-STD-883B Processing and L(0°C to 70°C), E(−40°C to 85°C), or S(−55°C to 100°C) Temperature Ranges

N PACKAGE
(TOP VIEW)



FM PACKAGE
(TOP VIEW)



PIN NOMENCLATURE			
A0-A7	Address Inputs	SIN	Serial Data In
$\overline{CAS}$	Column-Address Strobe	$\overline{SOE}$	Serial Output Enable
D	Random-Access Data In	SOUT	Serial Data Out
		$\overline{TR}/\overline{QE}$	Register Transfer/ Q Output Enable
NC	No Connection		
Q	Random-Access Data Out	V_{DD}	5-V Supply
		V_{SS}	Ground
$\overline{RAS}$	Row-Address Strobe	$\overline{W}$	Write Enable
SCLK	Serial Data Clock		

description

The TMS4161 is a high-speed, dual-access 65,536-bit dynamic random-access memory. The random-access port makes the memory look like it is organized as 65,536 words of one bit each like the TMS4164. The sequential access port is interfaced to an internal 256-bit dynamic shift register organized as four cascaded 64-bit shift registers which makes the memory look like it is organized as up to 256 words of up to 256 bits each which are accessed serially. One, two, three, or four 64-bit shift registers can be sequentially read out after a transfer cycle depending on a two-bit code applied to the two most significant column address inputs. The TMS4161 employs state-of-the-art SMOS (Scaled-MOS) N-channel double-level polysilicon gate technology for very high performance combined with low cost and improved reliability.

The TMS4161 features full asynchronous dual access capability except when transferring data between the shift register and the memory array.

Refresh period is extended to 4 milliseconds, and during this period each of the 256 rows must be strobed with $\overline{RAS}$ in order to retain data. $\overline{CAS}$ can remain high during the refresh sequence to conserve power. Note that the transfer of a row of data from the memory array to the shift register also refreshes that row.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address lines and data in are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TMS4161 is offered in 20-pin plastic dual-in-line and 22-pin plastic chip carrier packages. It is guaranteed for operation from 0°C to 70°C. The dual-in-line package is designed for insertion in mounting-hole rows on 7,62-mm (300-mil) centers.

random access address space to sequential address space mapping

The TMS4161 is designed with each row divided into four, 64-column sections (see functional block diagram). The first column section to be shifted out is selected by the two most significant column address bits. If the two bits represent binary 00, then one to four registers can be shifted out in order. If the two bits represent binary 01, then only 1 to 3 (the most significant) registers can be shifted out in order. If the two bits represent 10, then one to two of the most significant registers can be shifted out in order. Finally, if the two bits represent 11 only the most significant register can be shifted out. All registers are shifted out with the least significant bit (bit 0) first and the most significant bit (bit 63) last. Note that if the two column address bits equal 00 during the last register transfer cycle ($\overline{TR}/\overline{QE}$ at logic level "0" as $\overline{RAS}$ falls) a total of 256 bits can be sequentially read out.

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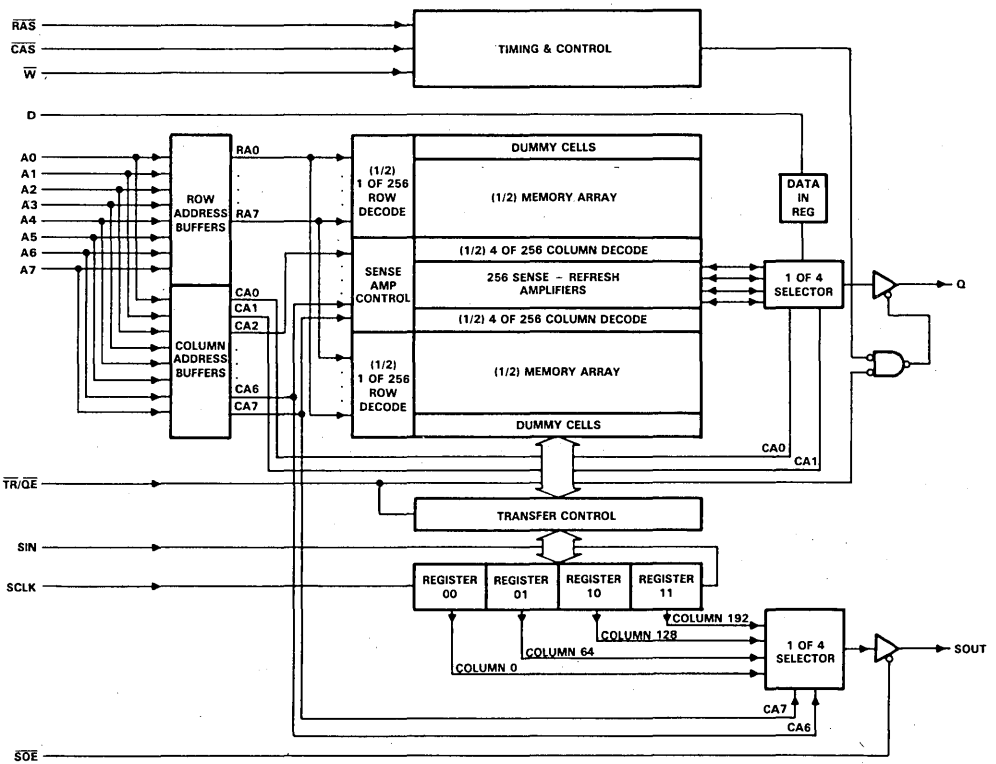
functional block diagram



random-access operation

TR/QE

The TR/QE pin has two functions. First, it selects either register transfer or random-access operation as RAS falls, and second, if this is a random-access operation, it functions as an output enable after CAS falls.

To use the TMS4161 in the random-access mode, TR/QE must be high as RAS falls. Holding TR/QE high as RAS falls keeps the 256 elements of the shift registers disconnected from the corresponding 256 bit lines of the memory array. If data is to be shifted, the shift registers must be disconnected from the bit lines. Holding TR/QE low as RAS falls enables the 256 switches that connect the shift registers to the bit lines and indicates that a transfer will occur between the shift registers and one of the memory rows.

During random-access operation, once CAS has been pulled low, TR/QE controls when the data will appear at the Q output (if this is a read cycle). Whenever TR/QE is held high during random-access operation, the Q output will be in the high-impedance state. This feature removes the possibility of an overlap between data on the address lines and data appearing on the Q output making it possible to connect the address lines to the Q and D lines (Use of this organization prohibits the use of the early write cycle.).

address (A0 through A7)

Sixteen address bits are required to decode 1 of 65,536 storage cell locations. Eight row-address bits are set up on pins A0 through A7 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the eight column-address bits are set up on pins A0 through A7 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable (W) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$, data out will remain inthe high-impedance state for the entire cycle permitting common I/O operation.

data in (D)

Data is written during a write or read-modify-write cycle. The falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. This latch can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data out (Q)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan out of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state as long as $\overline{CAS}$ or $\overline{TR}/\overline{QE}$ is held high. Data will not appear on the output until after both $\overline{CAS}$ and $\overline{TR}/\overline{QE}$ have been brought low. In a read cycle, the guaranteed maximum output enable access time is valid only if t_{CQE} is greater than t_{CQE} MAX, and t_{RLCL} is greater than t_{RLCL} MAX. Likewise, $t_{a(C)}$ MAX is valid only if t_{RLCL} is greater than t_{RLCL} MAX. Once the output is valid, it will remain valid while $\overline{CAS}$ and $\overline{TR}/\overline{QE}$ are both low; $\overline{CAS}$ or $\overline{TR}/\overline{QE}$ going high will return the output to a high-impedance state. In an early write cycle, the output is always in a high-impedance state. In a delayed write or ready-modify-write cycle, the output will follow the sequence for the read cycle. In a register transfer cycle, the output will always be in a high-impedance state.

refresh

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffer is in high-impedance state unless $\overline{CAS}$ is applied, the $\overline{RAS}$-only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses (A0 through A7) with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power.

page mode

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the chip. Thus, the time required to setup and strobe sequential row addresses for the same page is eliminated. To extend beyond the 256 column locations on a single RAM, the row address and $\overline{RAS}$ are applied to multiple 64K RAMs. $\overline{CAS}$ is then decoded to select the proper RAM.

power up

After power up, the power supply must remain at its steady-state value for 1 ms. In addition, $\overline{RAS}$ must remain high for 100 μs immediately prior to initialization. Initialization consists of performing eight $\overline{RAS}$ cycles before proper device operation is achieved.

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sequential-access operation

$\overline{TR}/\overline{QE}$

Memory transfer operations involving parallel use of the shift register are first indicated by bringing $\overline{TR}/\overline{QE}$ low before $\overline{RAS}$ falls low. This enables the switches connecting the 256 elements of the shift register to the 256 bit lines of the memory array. The $\overline{W}$ line determines whether the data will be transferred from or to the shift registers.

write enable ($\overline{W}$)

In the sequential access mode, $\overline{W}$ determines whether a transfer will occur from the shift registers to the memory array, or from the memory array to the shift registers. To transfer from the shift registers to the memory array, $\overline{W}$ is held low as $\overline{RAS}$ falls, and, to transfer from the memory array to the shift registers, $\overline{W}$ is held high as $\overline{RAS}$ falls. Thus, reads and writes are always with respect to the memory array. The write setup and hold times are referenced to the falling edge of $\overline{RAS}$ for this mode of operation.

row address (A0 through A7)

Eight address bits are required to select one of the 256 possible rows involved in the transfer of data to or from the shift registers. A0-A7, $\overline{W}$, and $\overline{TR}/\overline{QE}$ are latched on the falling edge of $\overline{RAS}$.

register column address (A7, A6)

To select one of the four shift registers (transfer from memory to register only), the appropriate 2-bit column address (A7, A6) must be valid when $\overline{CAS}$ falls. However, the $\overline{CAS}$ and register address signals need not be supplied every transfer cycle, only when it is desired to change or select a new register.

SCLK

Data is shifted in and out on the rising edge of SCLK. This makes it possible to view the shift registers as though it were made of 256 rising edge D flip-flops connected D to Q. The TMS4161 is designed to work with a wide range duty cycle clock to simplify system design. Note that data will appear at the SOUT pin not only on the rising edge of SCLK but also after an access time of $t_{a(RSO)}$ from $\overline{RAS}$ high during a parallel load of the shift registers.

SIN and SOUT

Data is shifted in through the SIN pin and is shifted out through the SOUT pin. The TMS4161 is designed such that it requires 3 ns hold time on SIN as SCLK rises. SOUT is guaranteed not to change for at least 8 ns after SLCK rises. These features make it possible to easily connect TMS4161s together, to allow SOUT to be connected to SIN, and to give external circuitry a full SLCK cycle time to allow manipulation of the serial data. When loading data into the shift register from the serial input in preparation for a shift register to memory transfer operation, the serial clock must be clocked an even number of times. To guarantee proper serial clock sequence after power up, a transfer cycle must be initiated before a serial data stream is applied at SIN.

$\overline{SOE}$

The serial output enable pin controls the impedance of the serial output, allowing multiplexing of more than one bank of TMS4161 memories into the same external video circuitry. When $\overline{SOE}$ is at a logic low level, SOUT will be enabled and the proper data read out. When $\overline{SOE}$ is at a logic high level, SOUT will be disabled and be in the high-impedance state.

refresh

The shift registers are also dynamic storage elements. The data held in the registers will be lost unless SCLK goes high to shift the data one bit position, a transfer write operation is invoked, or the data is reloaded from the memory array. See specifications for maximum register data retention times. Important: If the shift register has remained idle for a time period which exceeds the maximum SCLK high or SCLK low time, the dynamic clock circuits will also lose charge. Under these conditions, the shift register clocks must be re-enabled by performing any transfer cycle before data can be shifted into or out of the shift register.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin except V_{DD} and data out (see Note 1) . . . . . −1.5 V to 10 V
Voltage range on V_{DD} supply and data out with respect to V_{SS} . . . . . −1 V to 6 V
Short circuit output current . . . . . 50 mA
Power dissipation . . . . . 1 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		$V_{DD}+0.3$	V
V_{IL}	Low-level input voltage (see Notes 2 and 3)	−0.6		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTES: 2. The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.
3. Due to input protection circuitry, the applied voltage may begin to clamp at −0.6 V; test conditions must comprehend this occurrence.
4. See application report entitled "TMS4164A and TMS4416 Input Protection Diode" on page 9-5.

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electrical characteristics over full range of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TMS4161-15			TMS4161-20			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage (Q, SOUT)	I_{OH} = −5 mA	2.4			2.4			V
V_{OL}	Low-level output voltage (Q, SOUT)	I_{OL} = 4.2 mA			0.4			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 5.8 V, V_{DD} = 5 V, All other pins = 0 V			±10			±10	μA
I_O	Output current (leakage) (Q, SOUT)	V_O = 0.4 V to 5.5 V, V_{DD} = 5 V			±10			±10	μA
I_{DD1}	Average operating current during read or write cycle	$t_{c(rd)}$ = minimum cycle time, $\overline{TR}/\overline{QE}$ low after $\overline{RAS}$ falls,‡ SCLK and SIN low, $\overline{SOE}$ high, No load on Q and SOUT		50	70		50	70	mA
I_{DD2}§	Standby current	After 1 $\overline{RAS}$ cycle, $\overline{RAS}$ and $\overline{CAS}$ high, SCLK and SIN low, $\overline{SOE}$ high, No load on Q and SOUT		16	20		16	20	mA
I_{DD3}	Average refresh current	$t_{c(rd)}$ = minimum cycle time, $\overline{CAS}$ high, $\overline{RAS}$ cycling, SCLK and SIN low, $\overline{SOE}$ high, $\overline{TR}/\overline{QE}$ high, No load on Q and SOUT		42	55		37	50	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle time, $\overline{RAS}$ low, $\overline{CAS}$ cycling, $\overline{TR}/\overline{QE}$ low after $\overline{RAS}$ falls, SCLK and SIN low, $\overline{SOE}$ high, No load on Q and SOUT		45	55		40	50	mA
I_{DD5}	Average shift register current (includes I_{DD2})	$\overline{RAS}$ and $\overline{CAS}$ high, No load on Q and SOUT, $t_{c(SCLK)}$ = $t_{c(SCLK)}$ min		30	40		30	40	mA
I_{DD6}	Worst case average DRAM and shift register current	$t_{c(rd)}$ = minimum cycle time, $t_{c(SCLK)}$ = minimum cycle time, $\overline{TR}/\overline{QE}$ low after $\overline{RAS}$ falls, No load on Q and SOUT		85	95		80	90	mA

NOTE 5: Additional information on I_{DD1} – I_{DD6} on page 4-40.
† All typical values are at T_A = 25°C and nominal supply voltages.
‡ See appropriate timing diagram.
§ V_{IL} > −0.6 V.

capacitance over recommended supply voltage and operating free-air temperature range, f = 1 MHz

PARAMETER		TYP†	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs	4	5	pF
$C_{i(D)}$	Input capacitance, data input	4	5	
$C_{i(RC)}$	Input capacitance, strobe inputs	8	10	
$C_{i(W)}$	Input capacitance, write enable input	8	10	
$C_{i(CK)}$	Input capacitance, serial clock	8	10	
$C_{i(SI)}$	Input capacitance, serial in	4	5	
$C_{i(SOE)}$	Input capacitance, serial output enable	4	5	
$C_{i(TR)}$	Input capacitance, register transfer input	4	5	
$C_{o(Q)}$	Output capacitance, random-access data	5	7	
$C_{o(SOUT)}$	Output capacitance, serial out	5	7	

† All typical values are at T_A = 25°C and nominal supply voltages.

switching characteristics over recommended supply voltage range and operating free-air temperature range (see Figure 1)

PARAMETER		TEST CONDITIONS†	ALT. SYMBOL	TMS4161-15		TMS4161-20		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 100 pF	t_{CAC}		100		135	ns
$t_{a(QE)}$	Access time of Q from $\overline{TR}/\overline{QE}$ low	C_L = 100 pF			40		50	
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, C_L = 100 pF	t_{RAC}		150		200	
$t_{a(RSO)}$	SOUT access time from $\overline{RAS}$ high	C_L = 30 pF			65		85	
$t_{a(SOE)}$	Access time from $\overline{SOE}$ low to SOUT	C_L = 30 pF			20		25	
$t_{a(SO)}$	Access time from SCLK	C_L = 30 pF			45		50	
$t_{dis(CH)}$‡	Q output disable time from $\overline{CAS}$ high	C_L = 100 pF	t_{OFF}		40		40	
$t_{dis(QE)}$‡	Q output disable time from $\overline{TR}/\overline{QE}$ high	C_L = 100 pF			30		40	
$t_{dis(SOE)}$‡	Serial output disable time from $\overline{SOE}$ high	C_L = 30 pF			20		25	

† Figure 1 shows the load circuit.
‡ The maximum values for $t_{dis(CH)}$, $t_{dis(QE)}$, and $t_{dis(SOE)}$ define the time at which the output achieves the open circuit condition and are not referenced to V_{OH} or V_{OL}.

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timing requirements over recommended supply voltage range and operating free-air temperature range

		ALT. SYMBOL	TMS4161-15		TMS4161-20		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(P)}$	Page-mode cycle time	t_{PC}	160		225		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	240		315		ns
$t_{c(W)}$	Write cycle time	t_{WC}	240		315		ns
$t_{c(TW)}$	Transfer write cycle time‡		240		315		ns
$t_{c(Trd)}$	Transfer read cycle time		240		315		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	265		330		ns
$t_{c(SCLK)}$	Serial-clock cycle time	t_{SCC}	45	50,000	50	50,000	ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (precharge time§	t_{CP}	50		80		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low¶	t_{CAS}	100	10,000	135	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge time)	t_{RP}	80		105		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low#	t_{RAS}	150	10,000	200	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	45		45		ns
$t_{w(CKL)}$	Pulse duration, SCLK low		10		10		ns
$t_{w(CKH)}$	Pulse duration, SCLK high		12		12		ns
$t_{w(QE)}$	$\overline{TR}/\overline{QE}$ pulse duration low time (read cycle)		40		40		ns
t_t	Transition times (rise and fall) $\overline{RAS}$, $\overline{CAS}$, and SCLK	t_T	3	50	3	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		0		ns
$t_{su(RW)}$	$\overline{W}$ setup time before $\overline{RAS}$ low with $\overline{TR}/\overline{QE}$ low		0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		0		ns
$t_{su(WCL)}$	Early write-command setup time before $\overline{CAS}$ low	t_{WCS}	−5		−5		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	40		60		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	40		60		ns
$t_{su(TR)}$	$\overline{TR}/\overline{QE}$ setup time before $\overline{RAS}$ low		0		0		ns
$t_{su(SI)}$	Serial-data setup time before SCLK high		6		6		ns
$t_{h(SI)}$	Serial-data-in hold time after SCLK high		3		3		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	45		55		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	20		25		ns
$t_{h(RW)}$	$\overline{W}$ hold time after $\overline{RAS}$ low with $\overline{TR}/\overline{QE}$ low		20		20		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	95		120		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	60		80		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	110		145		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	45		55		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		ns

(Continued next page.)

NOTE 6: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, V_{IL} max and V_{IH} min must be met at the 10% and 90% points.

†All cycle times assume t_t = 5 ns except $t_{c(SCLK)}$ which assumes t_t = 3 ns.

‡Multiple transfer write cycles require separation by either a 500 ns $\overline{RAS}$-precharge interval or any other active $\overline{RAS}$-cycle.

§Page-mode only.

¶In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$). This applies to page-mode read-modify-write also.

#In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).

timing requirements over recommended supply voltage range and operating free-air temperature range (concluded)

		ALT. SYMBOL	TMS4161-15		TMS4161-20		UNIT
			MIN	MAX	MIN	MAX	
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	5		5		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	60		80		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	110		145		ns
$t_{h(RSO)}$	Serial-data-out hold time after $\overline{RAS}$ low with $\overline{TR}/\overline{QE}$ low		30		30		ns
$t_{h(SO)}$	Serial-data-qut hold time after SCLK high		8		8		ns
$t_{h(TR)}$	$\overline{TR}/\overline{QE}$ hold time after $\overline{RAS}$ low (transfer)		20		20		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	150		200		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
t_{CLQEH}	Delay time, $\overline{CAS}$ low to $\overline{QE}$ high		100		135		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	100		135		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{CWD}	65		75		ns
t_{CQE}	Delay time, $\overline{CAS}$ low to $\overline{QE}$ low (maximum value specified only to guarantee $t_{a(QE)}$ access time)			60		85	ns
t_{RHSC}	Delay time, $\overline{RAS}$ high to SCLK high		80	50,000	80	50,000	ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	25	50	30	65	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{RWD}	135		150		ns
t_{CKRL}	Delay time, SCLK high before $\overline{RAS}$ low with $\overline{TR}/\overline{QE}$ low‖		10	50,000	10	50,000	ns
$t_{rf(MA)}$	Refresh time interval, memory array	t_{REF1}		4		4	ms
$t_{rf(SR)}$	Refresh time interval, shift register☆	t_{REF2}		50,000		50,000	ns

NOTE 6: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, V_{IL} max and V_{IH} min must be met at the 10% and 90% points.

‖SCLK may be high or low during $t_{w(RL)}$, but there can not be any positive edge transitions on SCLK for a minimum of 10 ns prior to $\overline{RAS}$ going low with $\overline{TR}/\overline{QE}$ low (i.e., before a transfer cycle).

☆See "refresh" on page 4-22.

PARAMETER MEASUREMENT INFORMATION

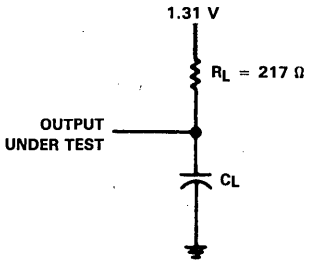

FIGURE 1. LOAD CIRCUIT

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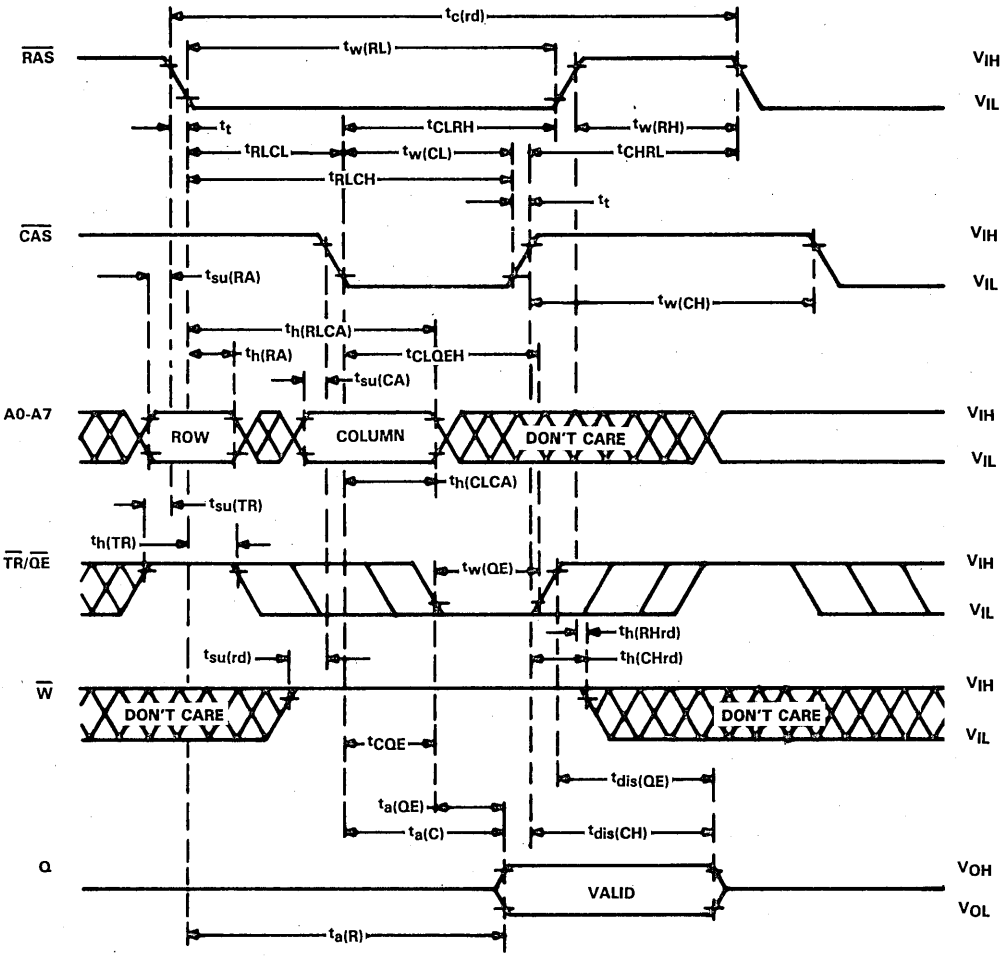
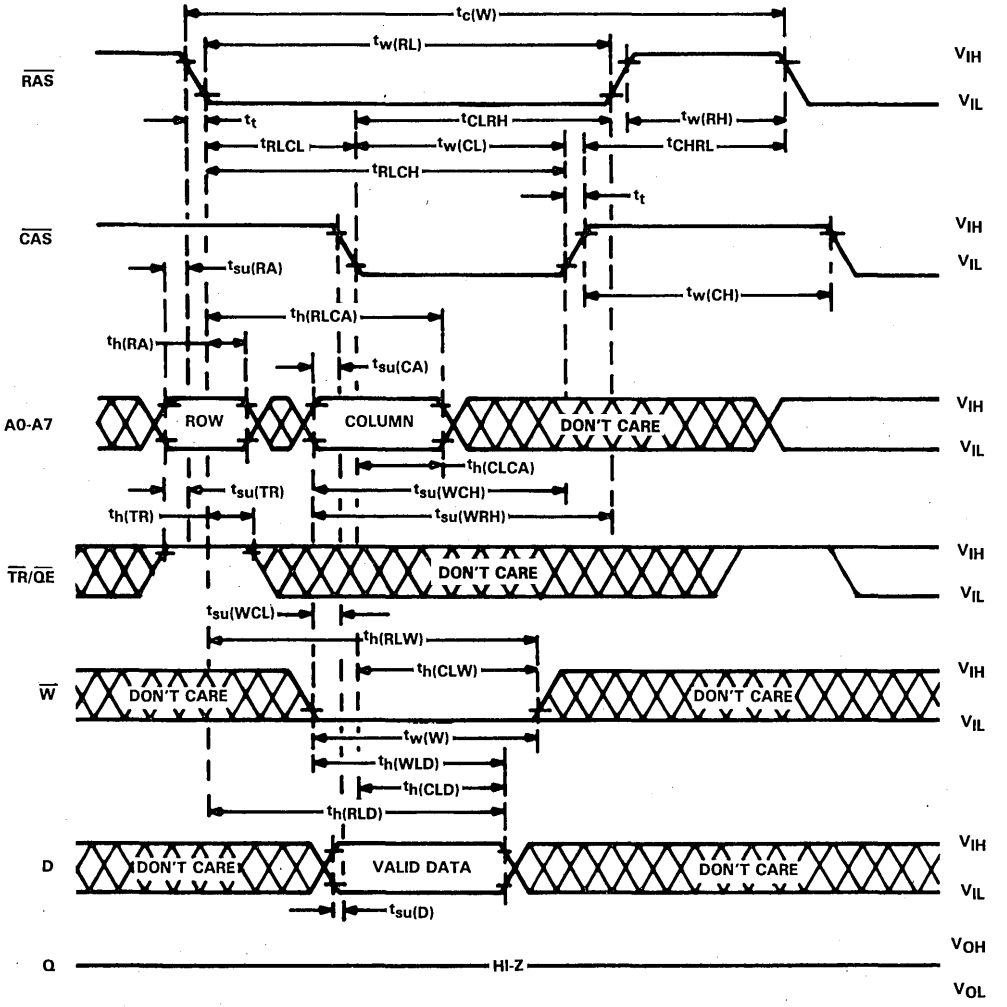
read cycle timing



early write cycle timing



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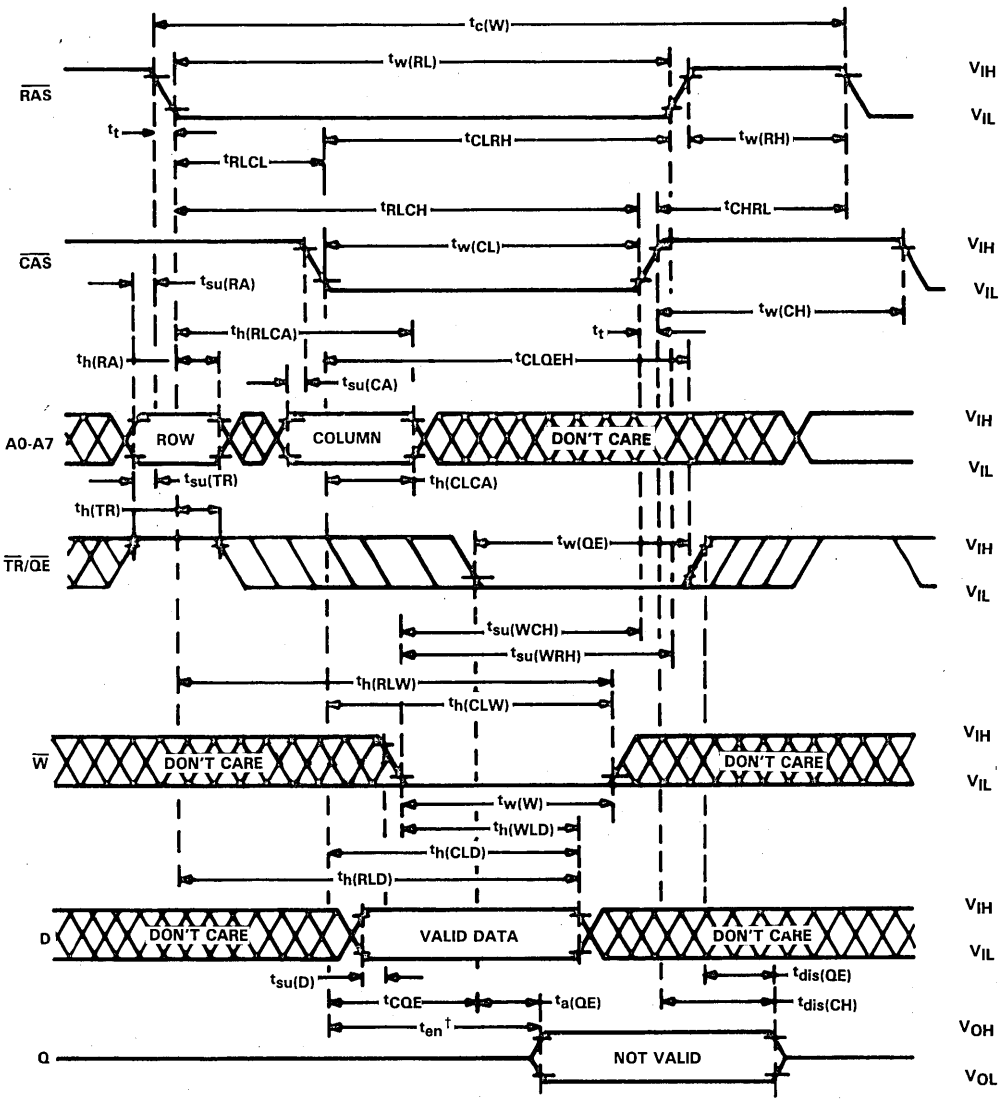
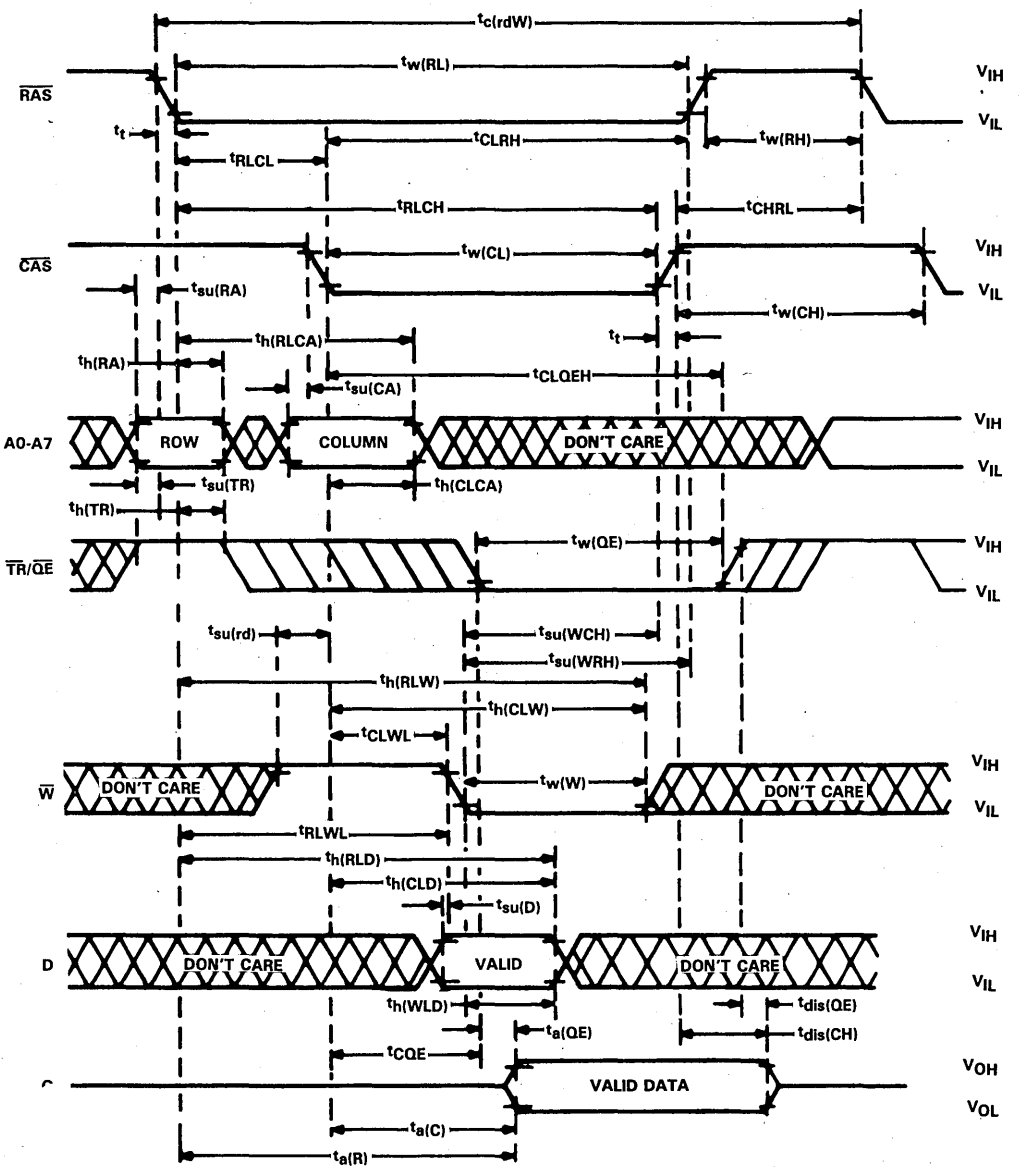
write cycle timing

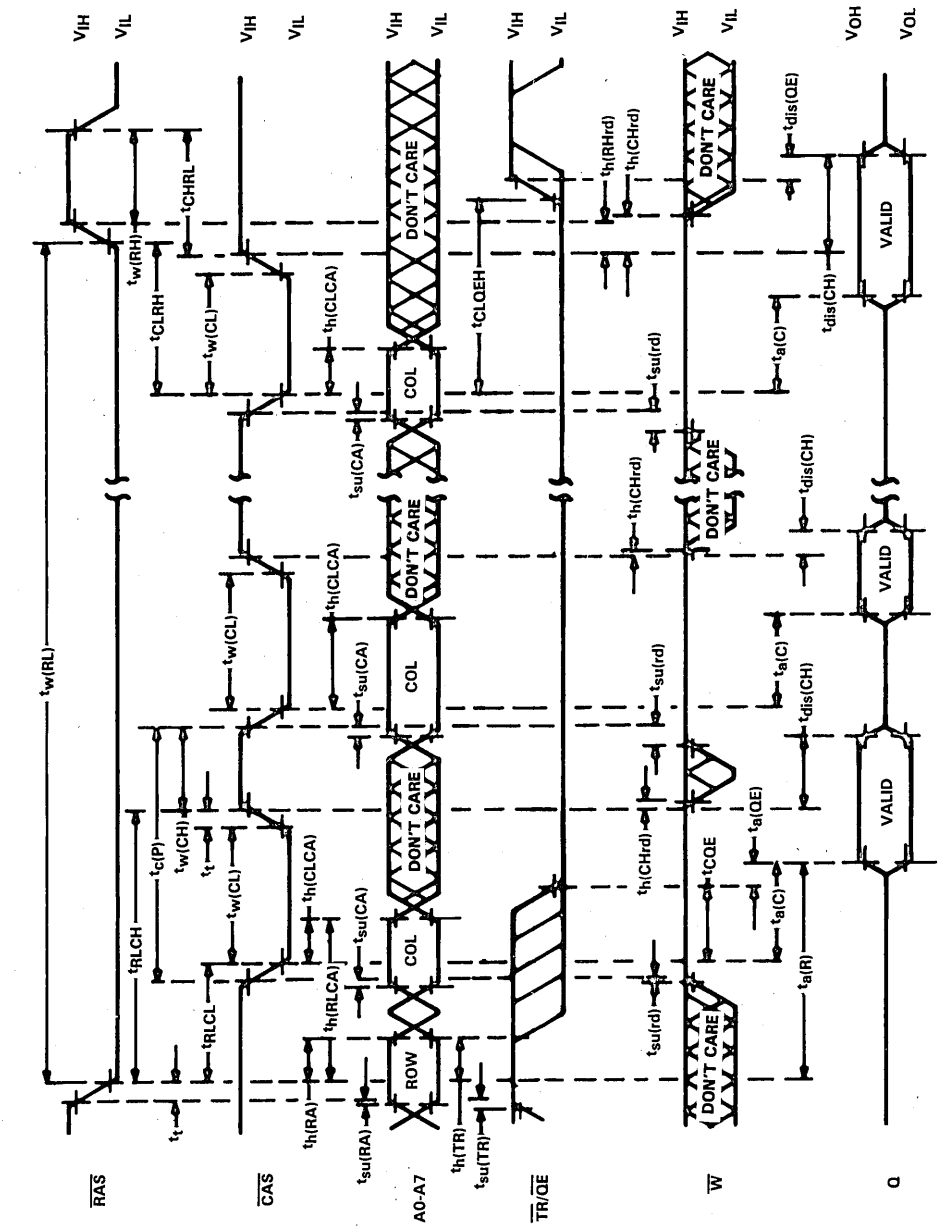


†The enable time (t_{en}) for a write cycle is equal in duration to the access time from $\overline{CAS}$ ($t_{a(C)}$) in a read cycle; but the active levels at the output are invalid.

read-write/read-modify-write cycle timing

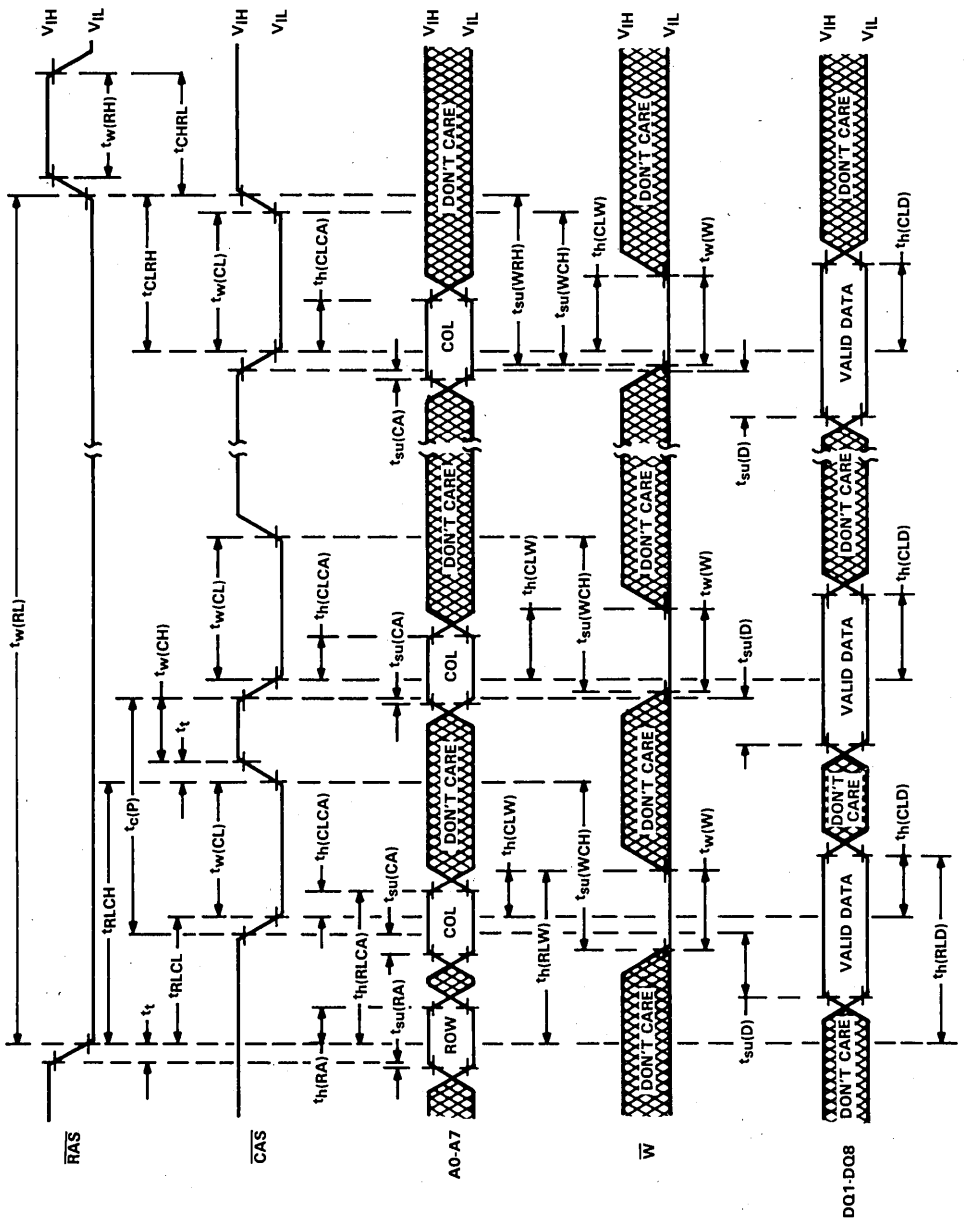


page-mode read cycle timing



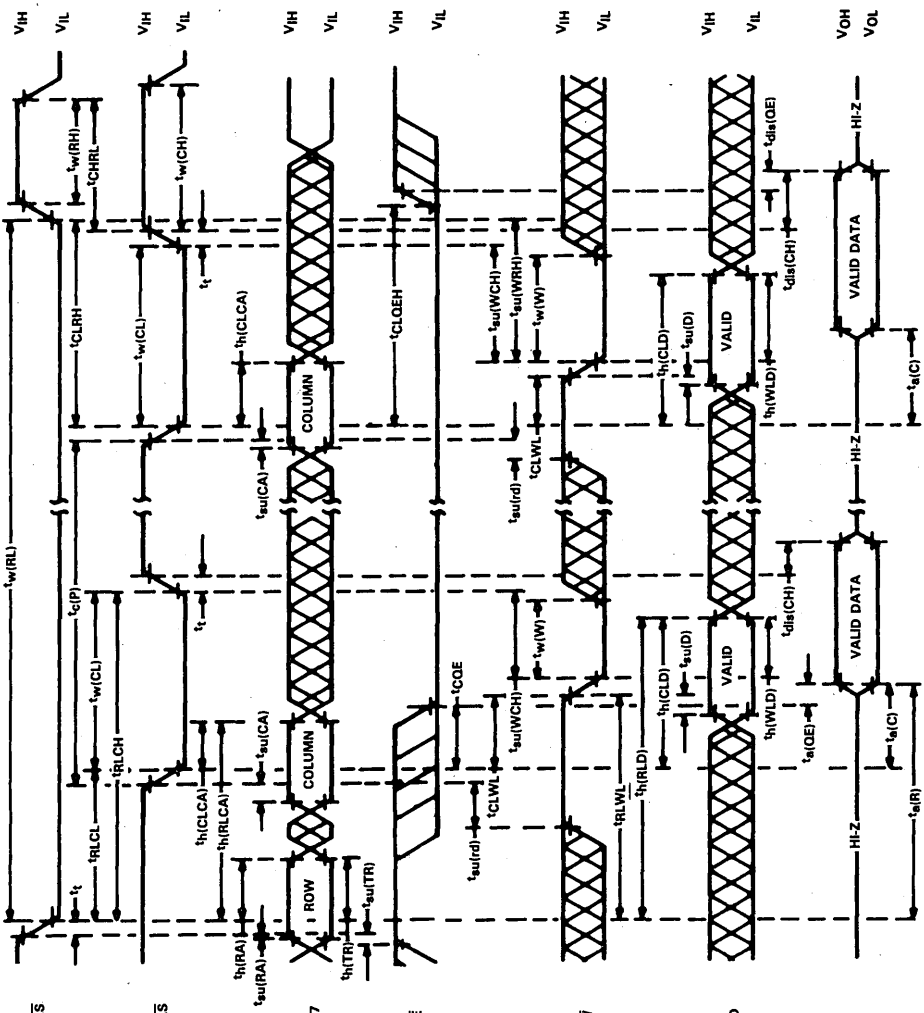
NOTES: 7. Timing is for non-multiplexed D, Q, and Address lines.
8. A write cycle or a read-modify-write cycle can be intermixed with read cycles as long as the write and read-modify-write timing specifications are not violated.

page-mode write cycle timing



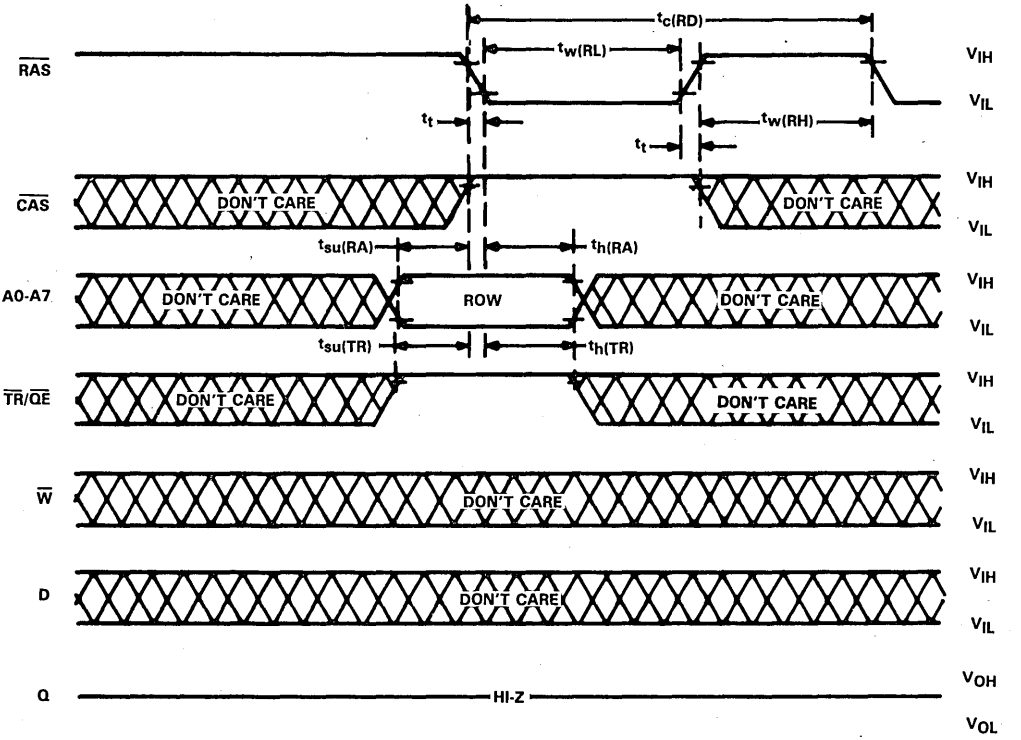
NOTES: 7. Timing is for non-multiplexed D, Q, and Address lines.
9. A read cycle or a read-modify-write cycle can be intermixed with write cycles as long as the read and read-modify-write timing specifications are not violated.

page-mode read-modify-write cycle timing

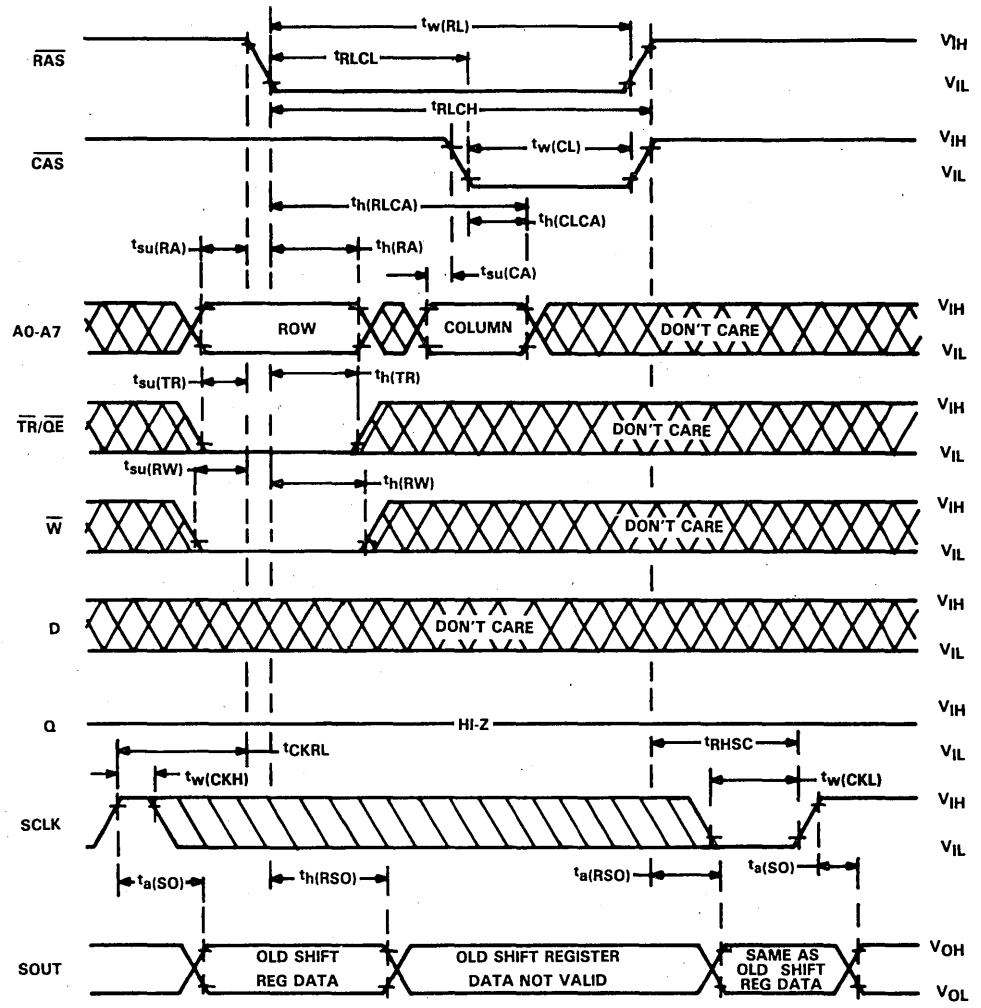


NOTES: 7. Timing is for non-multiplexed D, Q, and Address lines.
10. A read cycle or a write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

$\overline{\text{RAS}}$-only refresh timing



shift register to memory timing

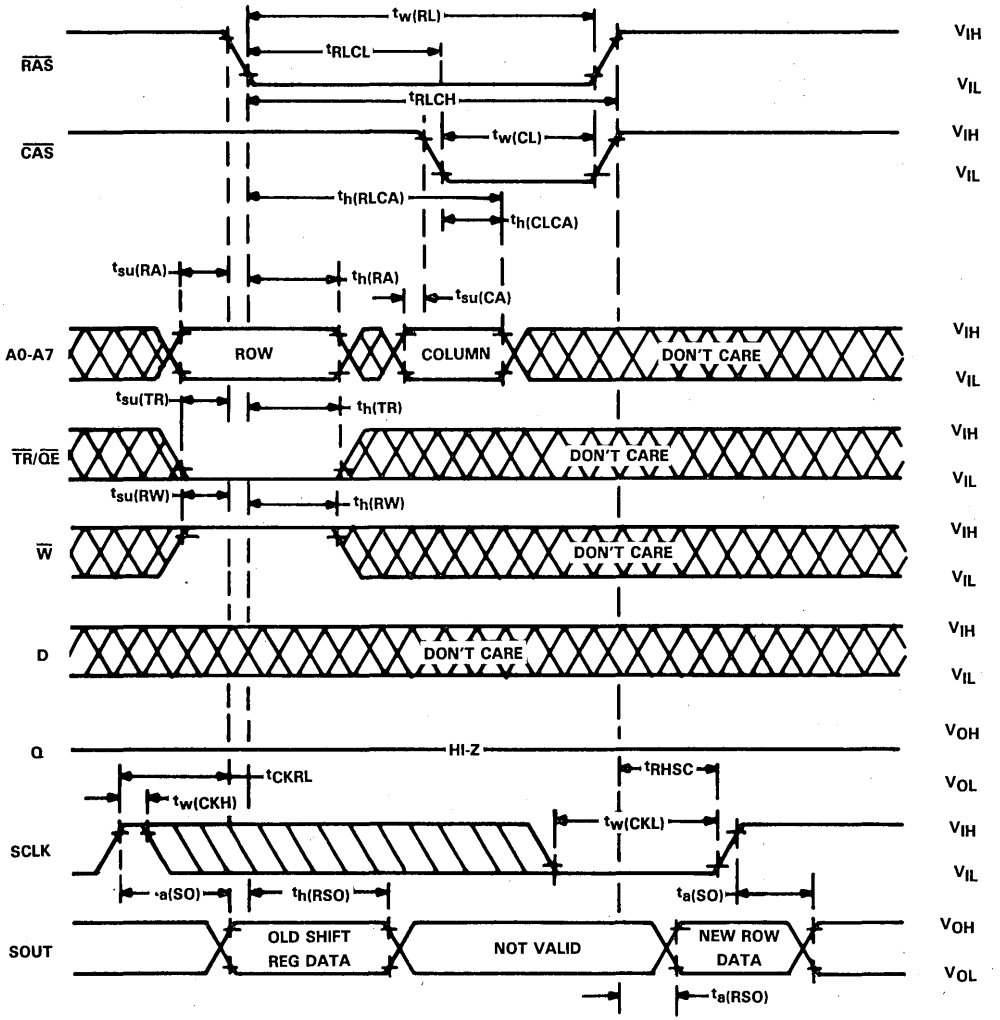


NOTES: 11. The shift register to memory cycle is used to transfer data from the shift register to the memory array. Every one of the 256 locations in the shift register is written into the 256 columns of the selected row. Note that the data that was in the shift register may have resulted, either from a serial shift in or from a parallel load of the shift register from one of the memory array rows.

12. $\overline{SOE}$ assumed low.

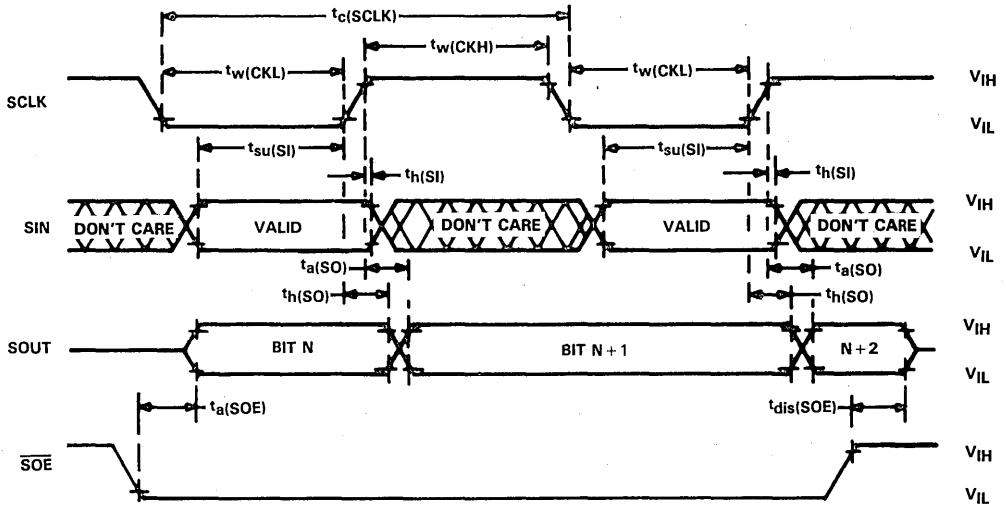
13. SCLK may be high or low during $t_{w(RL)}$.

memory to shift register timing



NOTES: 12. $\overline{SOE}$ assumed low.
13. SCLK may be high or low during $t_{w(RL)}$.
14. The memory to shift register cycle is used to load the shift register in parallel from the memory array. Every one of the 256 locations in the shift register are written into from the 256 columns of the selected row. Note that the data that is loaded into the shift register may be either shifted out or written back into another row.

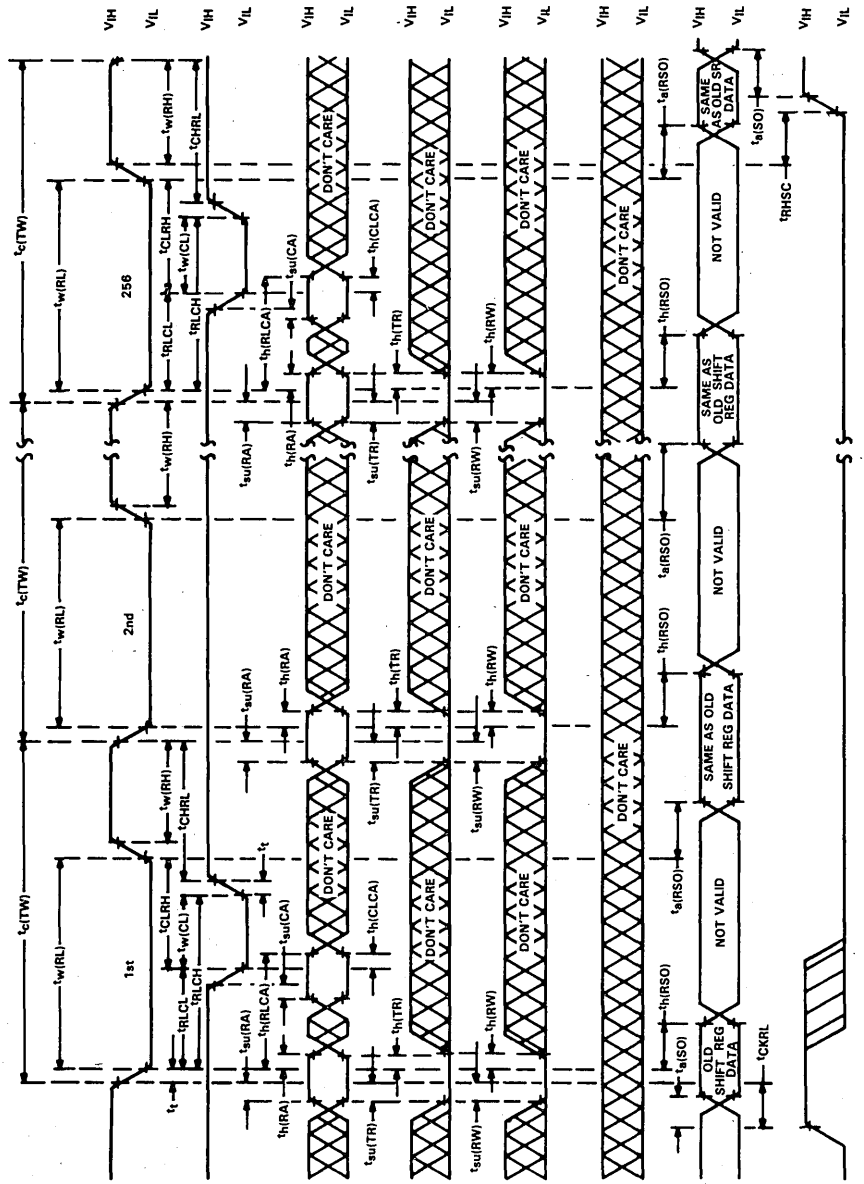
serial data shift timing



NOTES: 15. When loading data into the shift register from the serial input in preparation for a shift register to memory transfer operation, the serial clock must be clocked an even number of times.

16. While shifting data through the serial shift register, the state of $\overline{TR}/\overline{QE}$ is a don't care as long as $\overline{TR}/\overline{QE}$ is held high when $\overline{RAS}$ goes low and $t_{su(TR)}$ and $t_{h(TR)}$ timings are observed. This requirement avoids the initiation of a register-to-memory or memory-to-register data transfer operation. The serial data transfer cycle is used to shift data in and/or out of the shift register.

shift register to memory multiple timing



†$\overline{CAS}$ and register address need not be supplied every cycle, only when it is desired to change or select a new register length.

NOTES: 12. $\overline{SOE}$ assumed low.

17. The shift register to memory multiple cycle is used to write the shift register data to more than one row of the memory array. An application of this could be clearing all memory. To do this, the SIN line would be held at 0 to fill all locations in the shift register with 0's. The shift register would then be written into all 256 rows of the memory array in 256 cycles. The random output port Q will be in a high-impedance state as long as register transfer cycles are selected.

18. SCLK is a don't care except that no positive transitions on SCLK can occur for a period equal to t_{CKRL} prior to $\overline{RAS}$ falling with $\overline{TR/OE}$ low.

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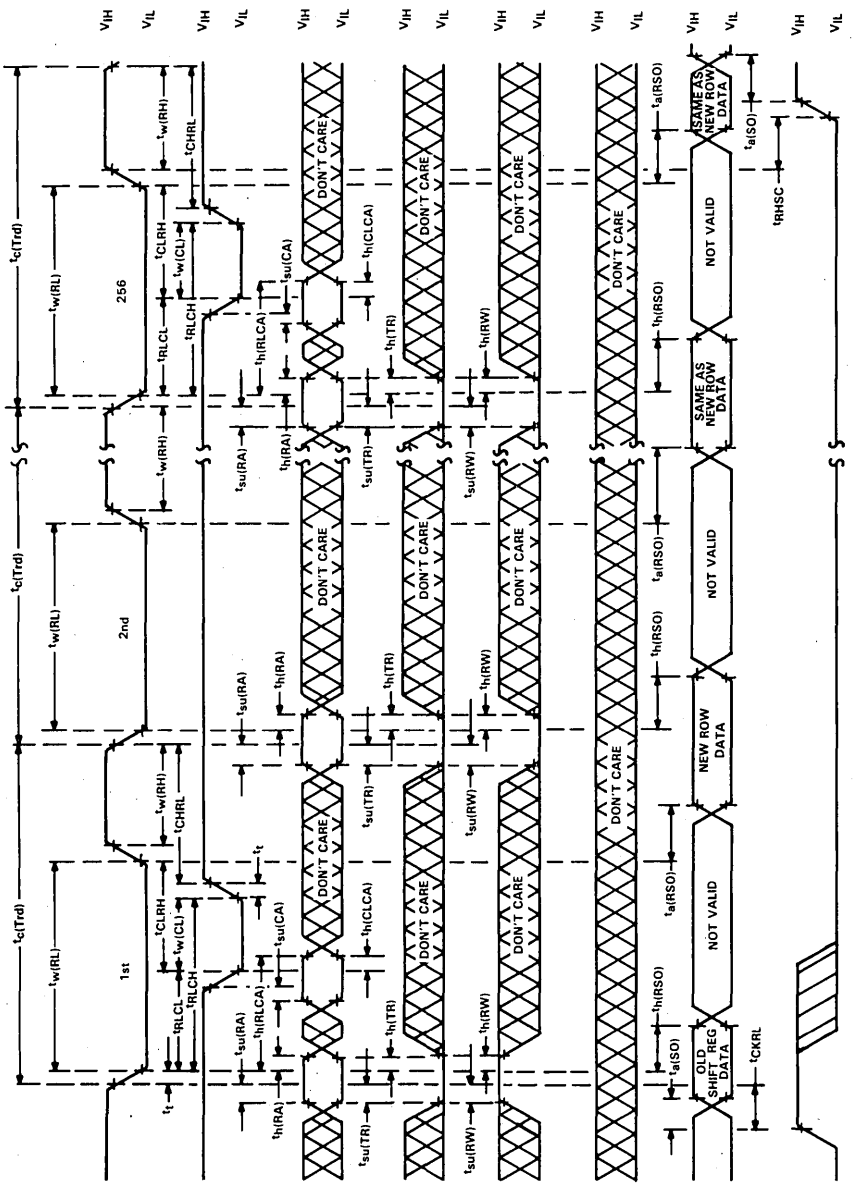
memory to shift register to memory multiple timing

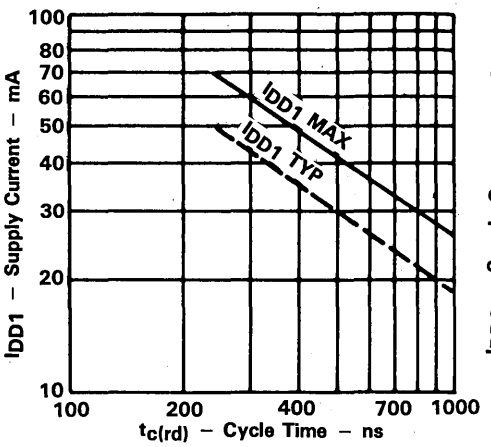


†CAS and register address need not be supplied every transfer cycle, only when it is desired to change from one register address to another.

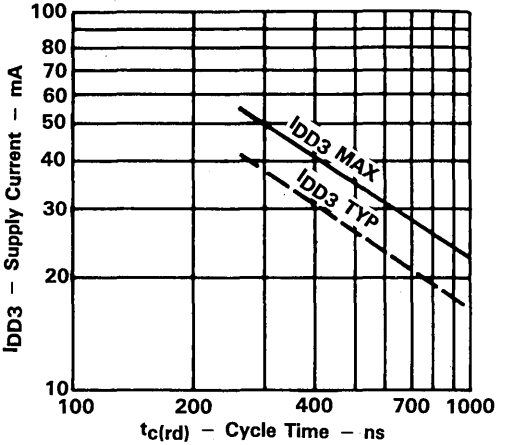
NOTES: 12. SOE assumed low.

18. SCLK is a don't care except that no positive transitions on SCLK can occur for a period equal to tCKRL prior to RAS falling with TR/OE low.
19. The memory to shift register to memory multiple cycle is used to reorder the rows within the memory array itself. First, the data in a row is stored in the shift register and then it is written into other selected rows. The random output port Q will be in a high-impedance state as long as register transfer cycles are selected.

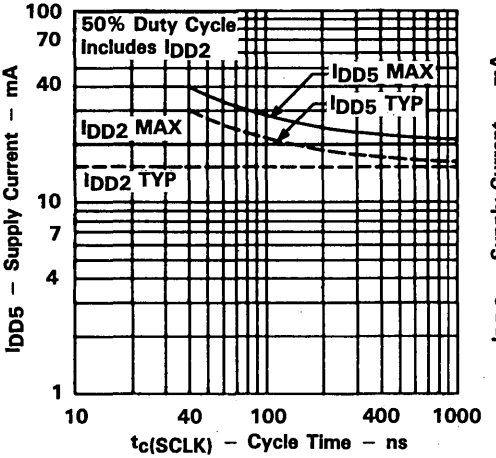
I_{DD1} vs CYCLE TIME



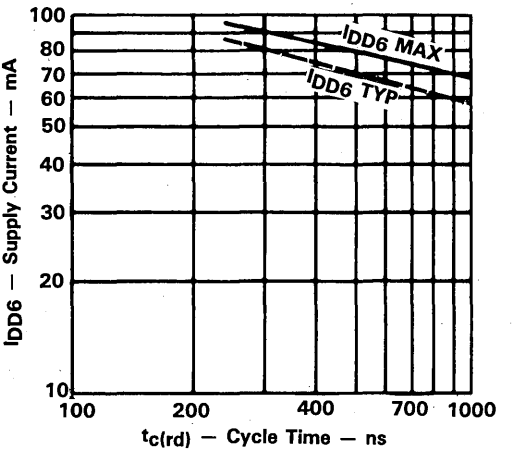
I_{DD3} vs CYCLE TIME



I_{DD5} vs CYCLE TIME



I_{DD6} vs CYCLE TIME



MAY 1985—REVISED NOVEMBER 1985

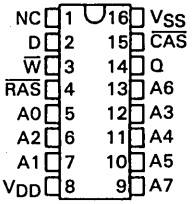
This Data Sheet Is Applicable to All TMS4164s Symbolized with Code "A" as Described on Page 4-57.

- 65,536 X 1 Organization
- Single 5-V Supply (10% Tolerance)
- JEDEC Standardized Pinout in Dual-in-Line Package
- Performance Ranges:

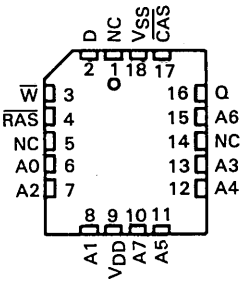
	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	READ-MODIFY-WRITE CYCLE (MIN)
'4164-12	120 ns	70 ns	230 ns	255 ns
'4164-15	150 ns	85 ns	260 ns	290 ns
'4164-20	200 ns	135 ns	330 ns	345 ns

- Upward Pin Compatible with TMS4116 (16K Dynamic RAM)
- First Military Version of 64K DRAM
- Also Available with MIL-STD-883B Processing and L(0°C to 70°C), E(−40°C to 85°C), S(−55°C to 100°C), or M(−55°C to 125°C) Temperature Ranges
- Operations of the TMS4164 Can Be Controlled by TI's TMS4500A and/or THCT4501 Dynamic RAM Controllers
- Long Refresh Period . . . 4 ms
- Low Refresh Overhead Time . . . As Low As 1.8% of Total Refresh Period
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Unlatched Output
- Common I/O Capability with Early Write Feature
- Page-Mode Operation for Faster Access
- Low Power Dissipation
  - Operating . . . 135 mW (Typ)
  - Standby . . . 17.5 mW (Typ)
- SMOS (Scaled-MOS) N-Channel Technology

N PACKAGE
(TOP VIEW)



FP PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A7	Address Inputs
$\overline{CAS}$	Column-Address Strobe
D	Data In
NC	No Connection
Q	Data Out
$\overline{RAS}$	Row-Address Strobe
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The TMS4164 is a high-speed, 65,536-bit, dynamic random-access memory, organized as 65,536 words of one bit each. It employs state-of-the-art SMOS (scaled MOS) N-channel double-level polysilicon gate technology for very high performance combined with low cost and improved reliability.

The TMS4164 features $\overline{RAS}$ access times of 120 ns, 150 ns, and 200 ns maximum. Power dissipation is 135 mW typical operating and 17.5 mW typical standby.

Refresh period is extended to 4 milliseconds, and during this period each of the 256 rows must be strobed with $\overline{RAS}$ in order to retain data. $\overline{CAS}$ can remain high during the refresh sequence to conserve power.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address lines and data in are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility. Pin 1 has no internal connection to allow compatibility with other 64K RAMs that use this pin for an additional function.

The TMS4164 is offered in 16-pin dual-in-line plastic (N suffix) and 18-lead plastic chip carrier (FP suffix) packages. The dual-in-line plastic package is designed for insertion in mounting-hole rows on 7,62-mm (300-mil) centers. The TMS4164 is guaranteed for operation from 0°C to 70°C.

operation

address (A0 through A7)

Sixteen address bits are required to decode 1 of 65,536 storage cell locations. Eight row-address bits are set up on pins A0 through A7 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the eight column-address bits are set up on pins A0 through A7 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$, data out will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data in (D)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. This latch can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data out (Q)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan out of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output goes active after the access time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ is satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low; $\overline{CAS}$ going high returns it to a high-impedance state. In an early write cycle, the output is always in the high-impedance state. In a delayed-write or read-modify-write cycle, the output will follow the sequence for the read cycle.

refresh

A refresh operation must be performed at least every four milliseconds to retain data. Since the ouput buffer is in the high-impedance state unless $\overline{CAS}$ is applied, The $\overline{RAS}$-only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses (A0 through A7) with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power.

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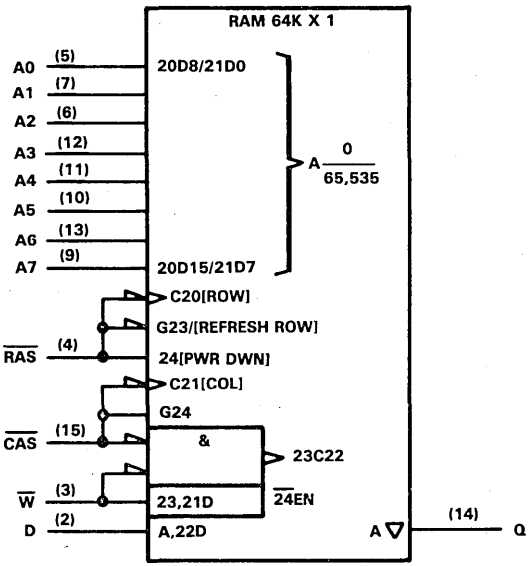
page mode

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing random column addresses onto the chip. Thus, the time required to setup and strobe sequential row addresses for the same page is eliminated. To extend beyond the 256 column locations on a single RAM, the row address and $\overline{RAS}$ are applied to multiple 64K RAMs. $\overline{CAS}$ is then decoded to select the proper RAM.

power up

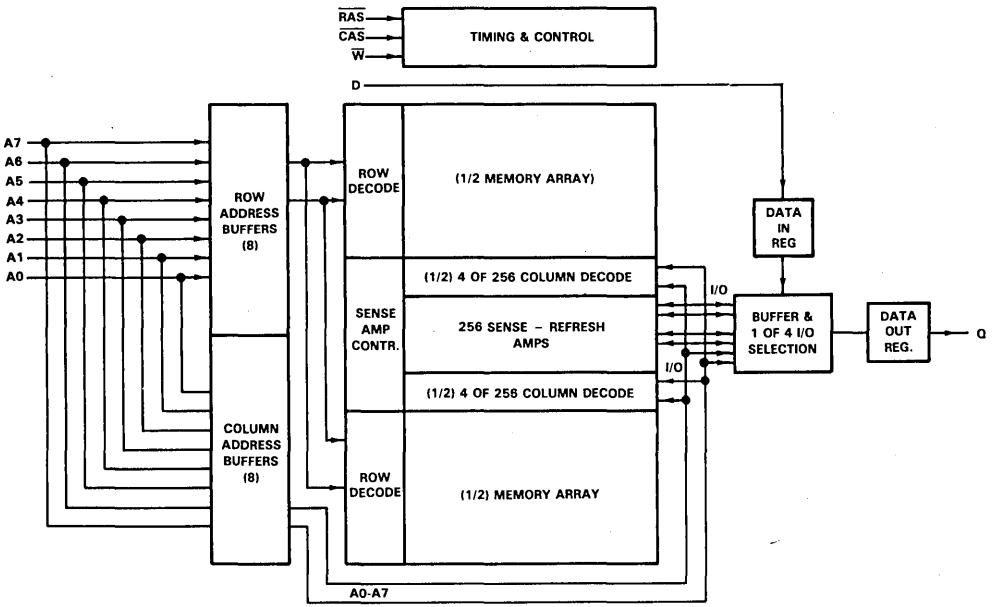
After power up, the power supply must remain at its steady-state value for 1 ms. In addition, $\overline{RAS}$ must remain high for 100 μs immediately prior to initialization. Initialization consists of performing eight $\overline{RAS}$ cycles before proper device operation is achieved.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the dual-in-line package.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage on any pin except V_{DD} and data out (see Note 1) . . . . . −1.5 V to 10 V
Voltage on V_{DD} supply and data out with respect to V_{SS} . . . . . −1 V to 6 V
Short circuit output current . . . . . 50 mA
Power dissipation . . . . . 1 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values in this data sheet are with respect to V_{SS}.
2. Additional information concerning the handling of ESD sensitive devices is available in a document entitled *"Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies"* in Section 12.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		4.5	5	5.5	V
V_{SS}	Supply voltage			0		V
V_{IH}		V_{DD} = 4.5 V	2.4		4.8	V
		V_{DD} = 5.5 V	2.4		6	
V_{IL}	Low-level input voltage (see Notes 3 and 4)		−0.6		0.8	V
T_A	Operating free-air temperature		0		70	°C

NOTES: 3. The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

4. Due to input protection circuitry, the applied voltage may begin to clamp at −0.6 V. Test conditions must comprehend this occurrence. See application report entitled "TMS4164A and TMS4416 Input Protection Diode" on page 9-5.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TMS4164-12			TMS4164-15			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4			2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 5.8 V, V_{DD} = 5 V, All other pins = 0 V			±10			±10	μA
I_O	Output current (leakage)	V_O = 0.4 to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10			±10	μA
I_{DD1}‡	Average operating current during read or write cycle	t_c = minimum cycle, All outputs open		40	48		35	45	mA
I_{DD2}§	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, All outputs open		3.5	5		3.5	5	mA
I_{DD3}‡	Average refresh current	t_c = minimum cycle, $\overline{CAS}$ high and $\overline{RAS}$ cycling, All outputs open		28	40		25	37	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low and $\overline{CAS}$ cycling, All outputs open		28	40		25	37	mA

† All typical values are at T_A = 25°C and nominal supply voltages.
‡ Additional information on page 4-58.
§ V_{IL} > −0.6V. See application report entitled "TMS4164A and TMS4416 Input Protection Diode" on page 9-5.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TMS4164-20			UNIT
			MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 5.8 V, V_{DD} = 5 V All other pins = 0 V			±10	μA
I_O	Output current (leakage)	V_O = 0.4 to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10	μA
I_{DD1}‡	Average operating current during read or write cycle	t_c = minimum cycle All outputs open		27	37	mA
I_{DD2}§	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, All outputs open		3.5	5	mA
I_{DD3}‡	Average refresh current	t_c = minimum cycle, $\overline{CAS}$ high and $\overline{RAS}$ cycling, All outputs open		20	32	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low and $\overline{CAS}$ cycling, All outputs open		20	32	mA

† All typical values are at T_A = 25°C and nominal supply voltages.
‡ Additional information on page 4-58.
§ V_{IL} > −0.6V. See application report entitled "TMS4164A and TMS4416 Input Protection Diode" on page 9-5.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

PARAMETER		TYP†	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs	4	5	pF
$C_{i(D)}$	Input capacitance, data input	4	5	pF
$C_{i(RC)}$	Input capacitance strobe inputs	6	8	pF
$C_{i(W)}$	Input capacitance, write enable input	6	8	pF
C_o	Output capacitance	5	6	pF

† All typical values are at T_A = 25°C and nominal supply voltages.

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TMS4164-12		TMS4164-15		UNIT
				MIN	MAX	MIN	MAX	
$t_{A(C)}$	Access time from $\overline{CAS}$	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		70		85	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	C_L = 100 pF, t_{RLCL} = MAX, Load = 2 Series 74 TTL gates	t_{RAC}		120		150	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	40	0	40	ns

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switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TMS4164-20		UNIT
				MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		135	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	C_L = 100 pF, t_{RLCL} = MAX, Load = 2 Series 74 TTL gates	t_{RAC}		200	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	50	ns

timing requirements over recommended supply voltage range and operating free-air temperature range (see Note 1)

		ALT. SYMBOL	TMS4164-12		TMS4164-15		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(P)}$	Page-mode cycle time	t_{PC}	130		145		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	230		260		ns
$t_{c(W)}$	Write cycle time	t_{WC}	230		260		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	255		290		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (precharge time)‡	t_{CP}	50		50		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low§	t_{CAS}	70	10,000	85	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge time)	t_{RP}	80		100		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low¶	t_{RAS}	120	10,000	150	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	40		45		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	50	3	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	−5		−5		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	50		50		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	50		50		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	40		45		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	15		20		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	85		95		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DHC}	40		45		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	85		95		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DHW}	40		45		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	5		5		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	40		45		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	85		95		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	120		150		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	70		85		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{CWD}	40		60		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	15	50	20	65	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{RWD}	110		120		ns
t_{WLCL}	Delay time, $\overline{W}$ low to $\overline{CAS}$ low (early write cycle)	t_{WCS}	−5		−5		ns
t_{rf}	Refresh time interval	t_{REF}		4		4	ms

NOTE 1: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, V_{IL} max and V_{IH} min must be met at the 10% and 90% points.

† All cycle times assume t_t = 5 ns.

‡ Page mode only.

§ In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$). This applies to page-mode read-modify-write also.

¶ In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).

timing requirements over recommended supply voltage range and operating free-air temperature range (see Note 1)

		ALT. SYMBOL	TMS4164-20 MIN	TMS4164-20 MAX	UNIT
$t_{c(P)}$	Page-mode cycle time	t_{PC}	225		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	330		ns
$t_{c(W)}$	Write cycle time	t_{WC}	330		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	345		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (precharge time)‡	t_{CP}	80		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low§	t_{CAS}	135	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge time)	t_{RP}	120		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low¶	t_{RAS}	200	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	55		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	−5		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	60		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	60		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	55		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	25		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	120		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DHC}	55		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	145		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DHW}	55		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	5		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	55		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	145		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	200		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	135		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{CWD}	65		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	25	65	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{RWD}	130		ns
t_{WLCL}	Delay time, $\overline{W}$ low to $\overline{CAS}$ low (early write cycle)	t_{WCS}	−5		ns
t_{rf}	Refresh time interval	t_{REF}		4	ms

NOTE 1: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, V_{IL} max and V_{IH} min must be met at the 10% and 90% points.

† All cycle times assume t_t = 5 ns.

‡ Page mode only.

§ In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$). This applies to page-mode read-modify-write also.

¶ In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).

PARAMETER MEASUREMENT INFORMATION

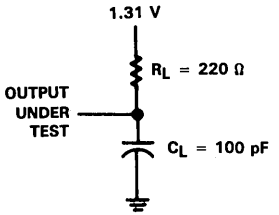
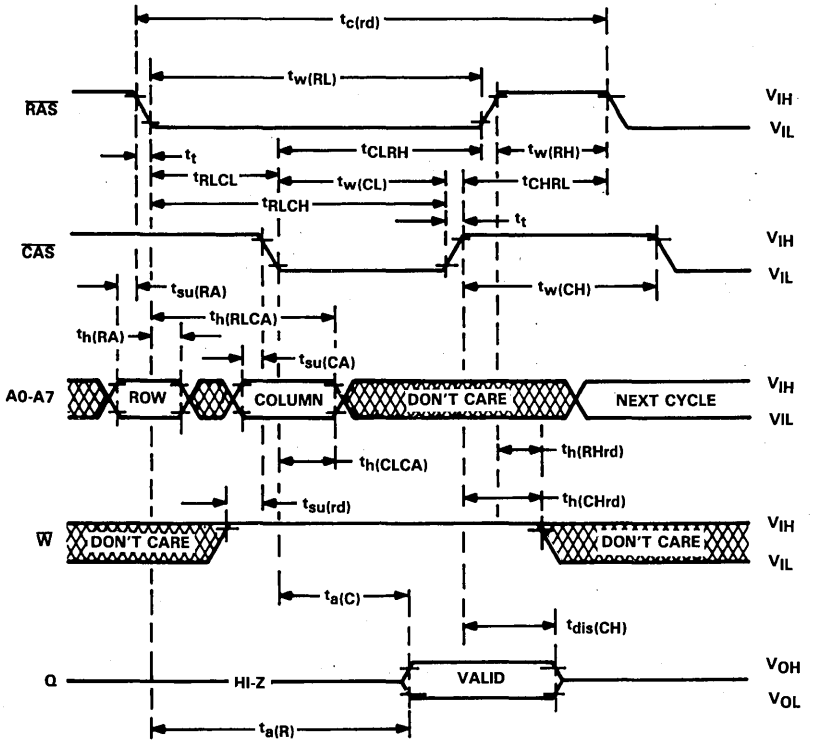


FIGURE 1. LOAD CIRCUIT

read cycle timing



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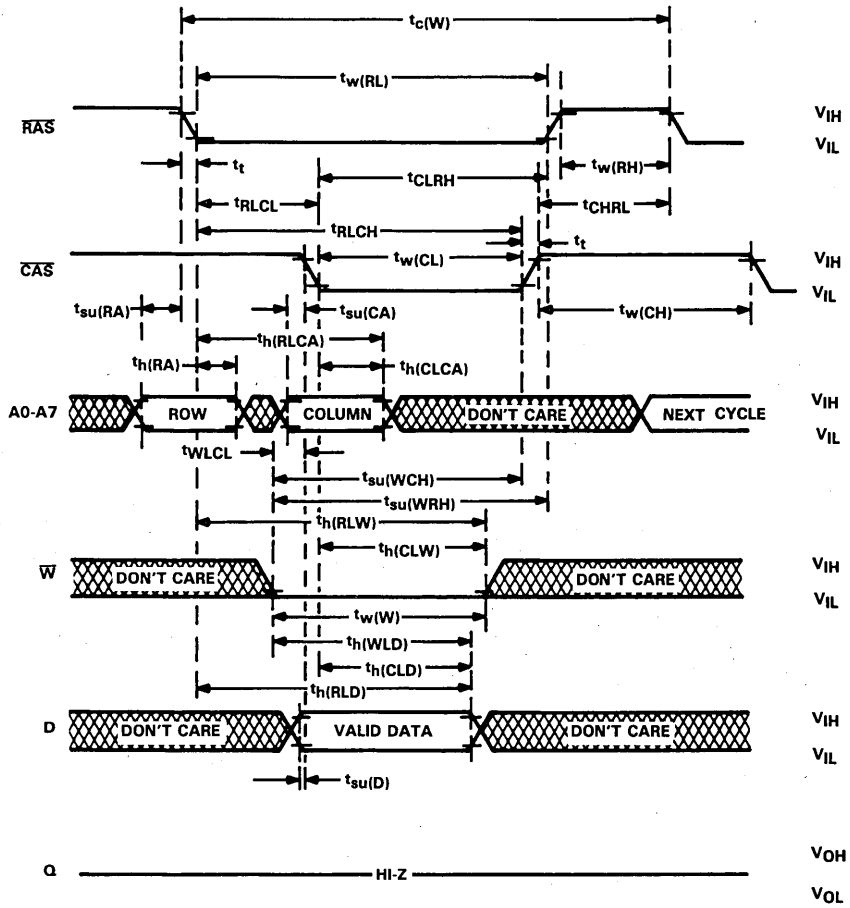
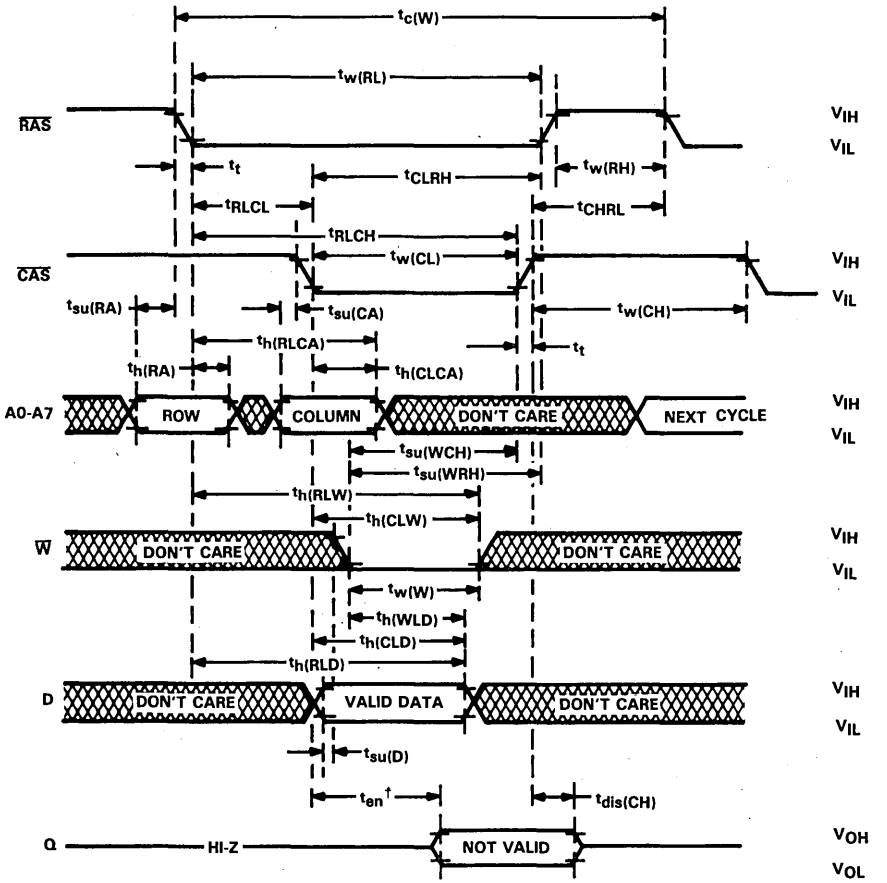
early write cycle timing

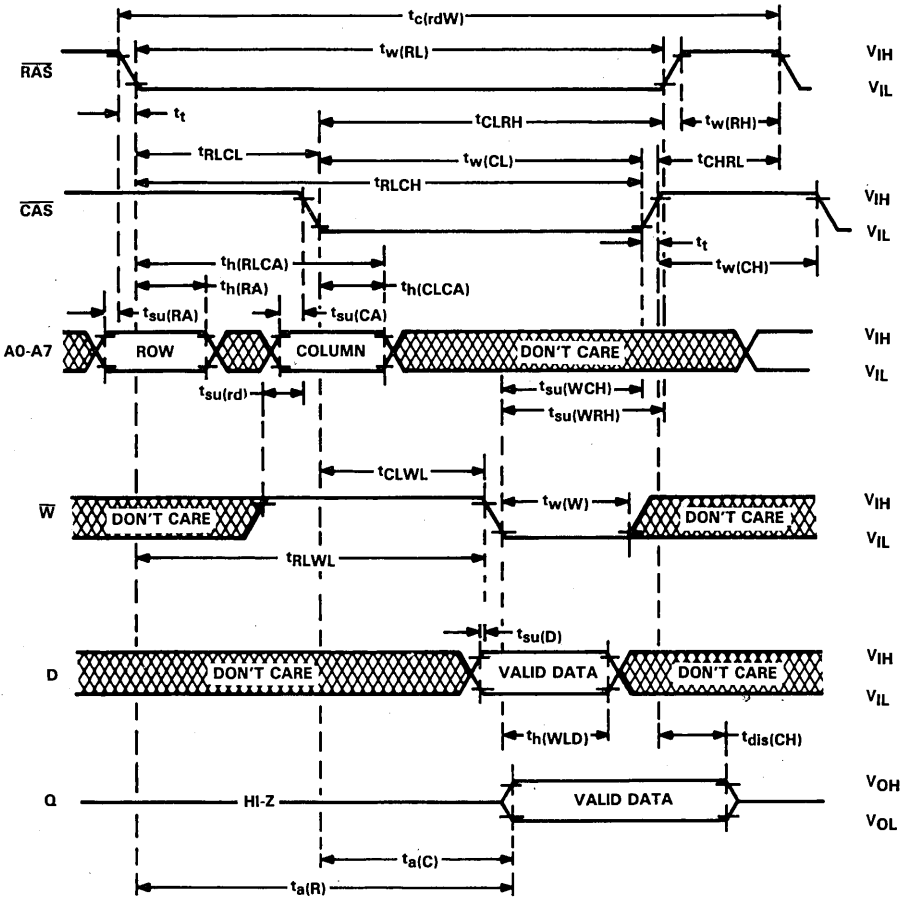


write cycle timing

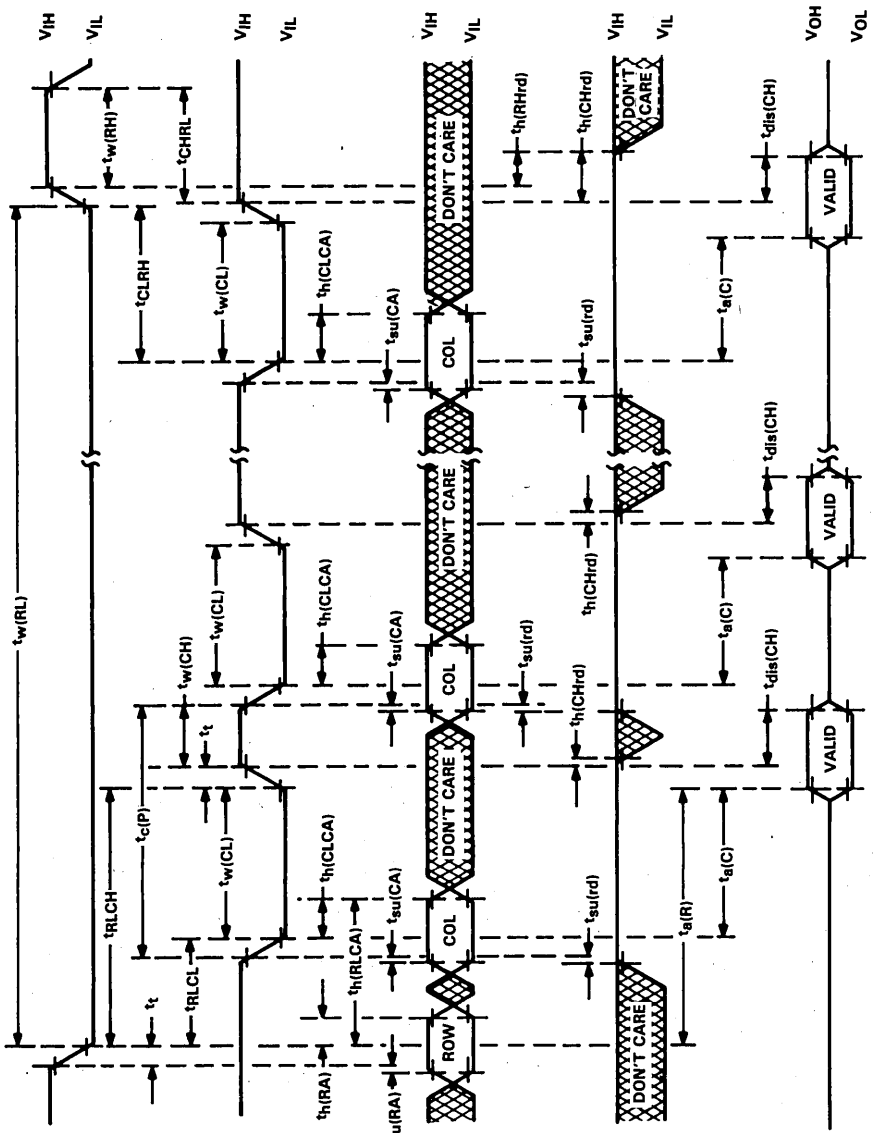


† The enable time (t_{en}) for a write cycle is equal in duration to the access time from $\overline{CAS}$ ($t_{a(C)}$) in a read cycle; but the active levels at the output are invalid.

read-modify-write cycle timing

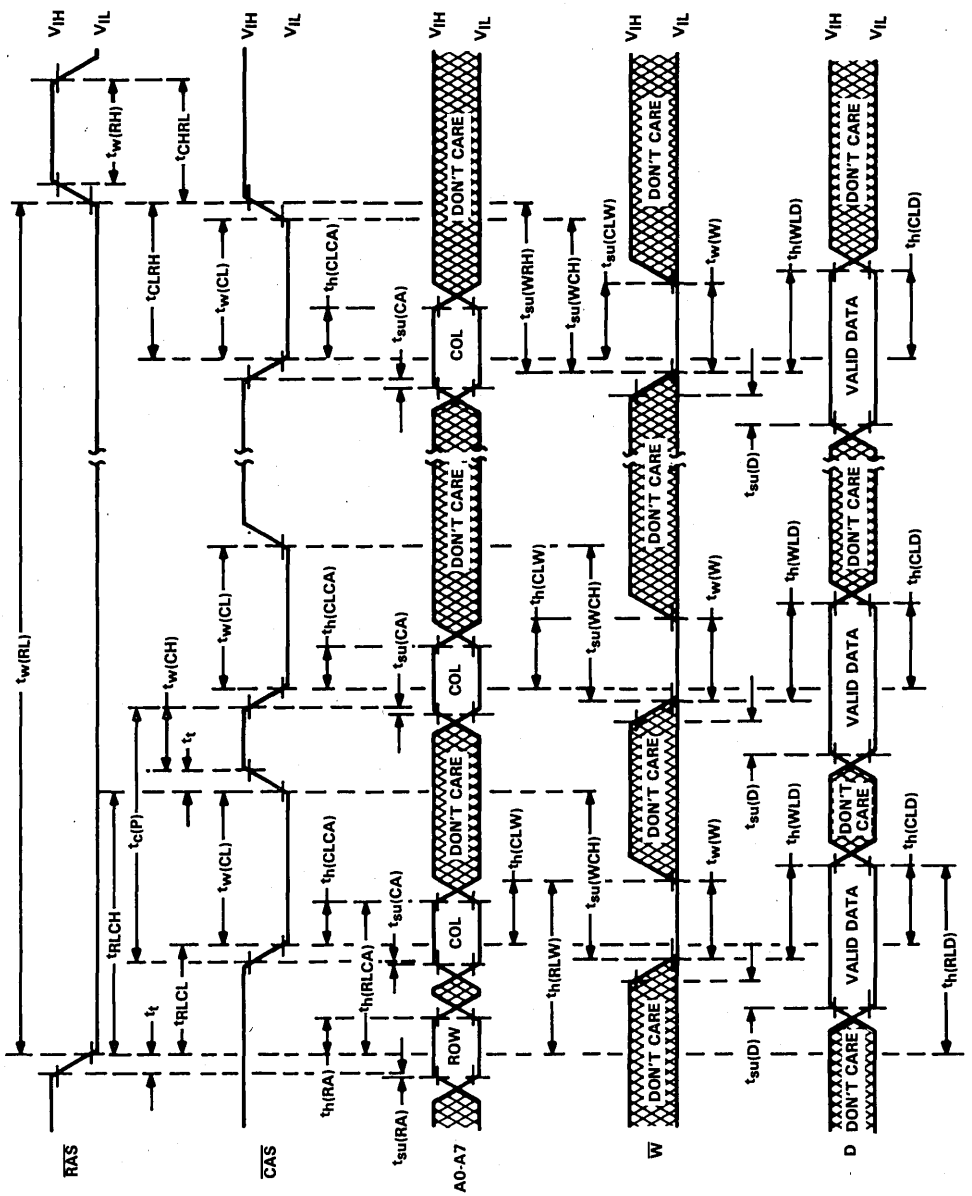


page-mode read cycle timing



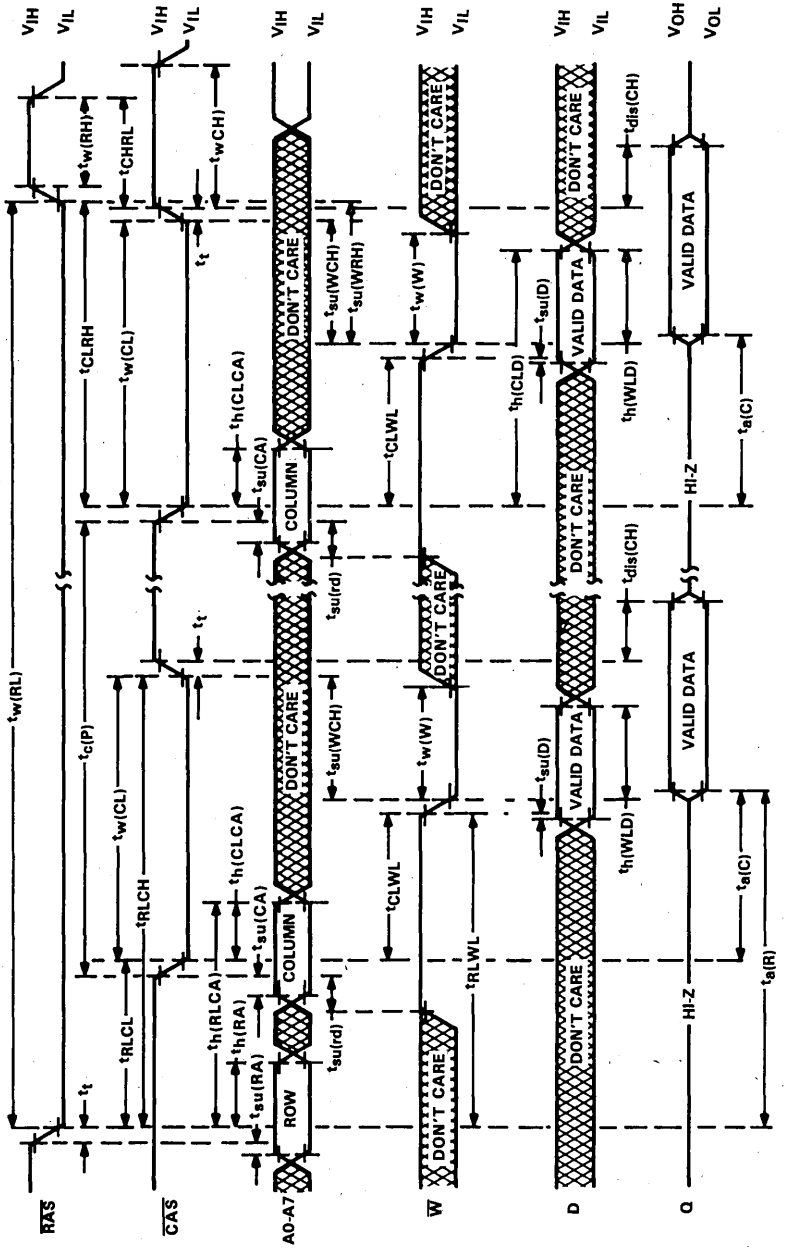
NOTE 2: A write cycle or a read-modify-write cycle can be intermixed with read cycles as long as the write and read-modify-write timing specifications are not violated.

page-mode write cycle timing



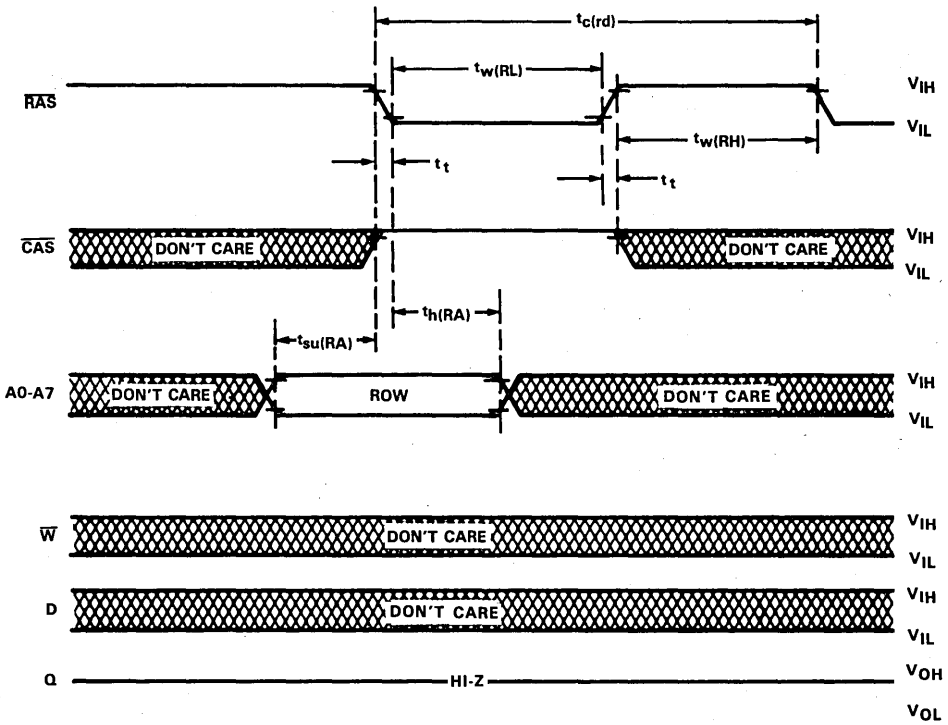
NOTE 3: A read cycle or a read-modify-write cycle can be intermixed with write cycles as long as the read and read-modify-write timing specifications are not violated.

page-mode read-modify-write cycle timing



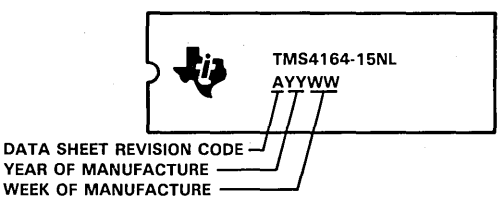
NOTE 4: A read or a write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

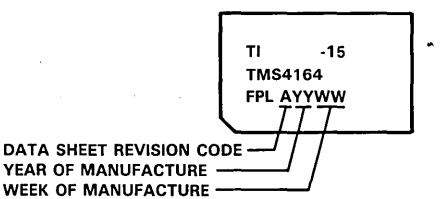
$\overline{\text{RAS}}$-only refresh timing



device symbolization

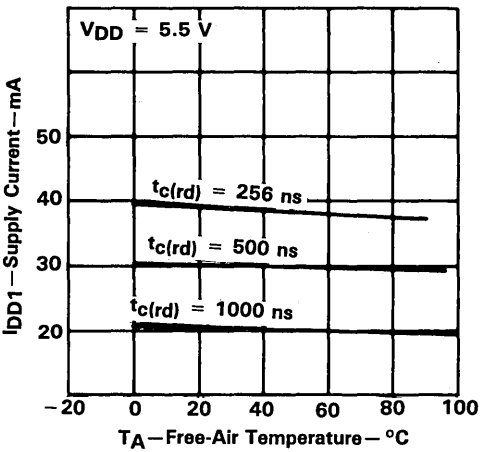
This data sheet is applicable to all TI TMS4164 Dynamic RAMs with the code "A" to the left of the date code as shown below:



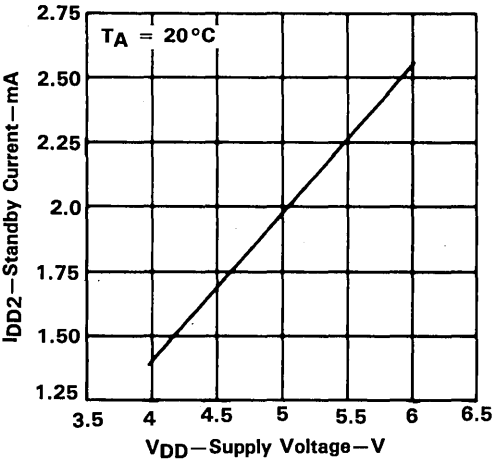


TYPICAL CHARACTERISTICS

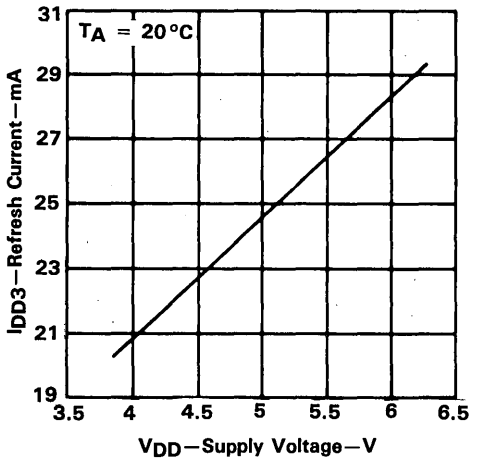
TYPICAL SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE



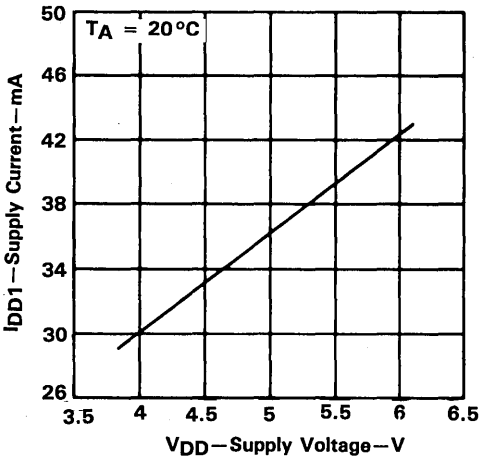
TYPICAL SUPPLY CURRENT
vs
SUPPLY VOLTAGE



TYPICAL SUPPLY CURRENT
vs
SUPPLY VOLTAGE



TYPICAL SUPPLY CURRENT
vs
SUPPLY VOLTAGE



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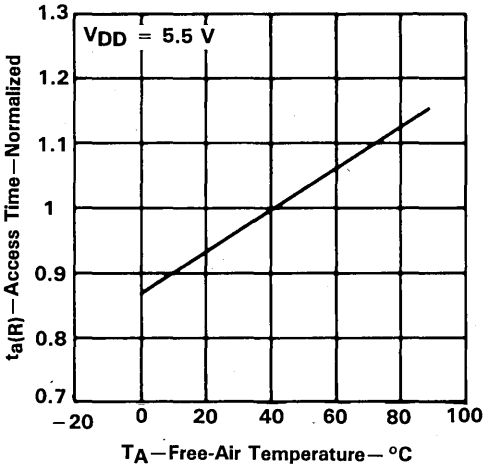
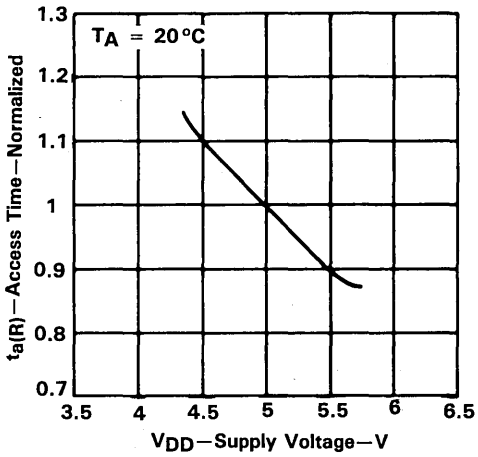
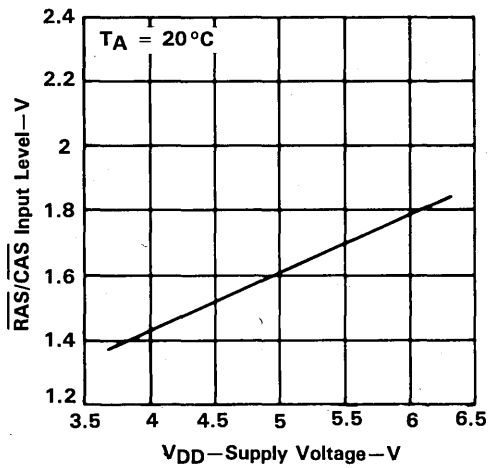
ACCESS TIME
vs
FREE-AIR TEMPERATURE



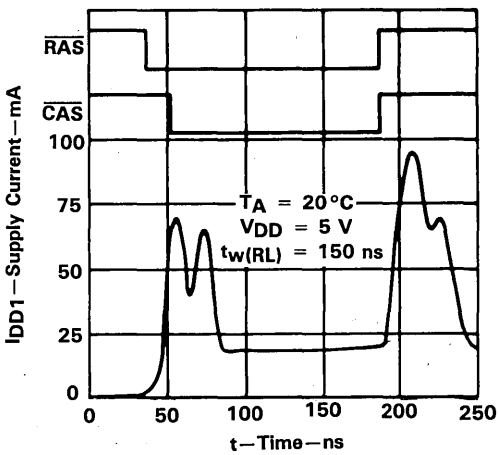
ACCESS TIME
vs
SUPPLY VOLTAGE



$\overline{RAS}/\overline{CAS}$ INPUT LEVEL
vs
SUPPLY VOLTAGE



AVERAGE CURRENT
DURING AN OPERATING CYCLE



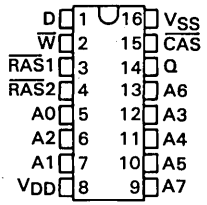
APRIL 1985—REVISED NOVEMBER 1985

- 2 X 65,536 X 1 Organization
- Single 5-V Supply (10% Tolerance)
- Operating Free-Air Temperature . . . 0°C to 70°C
- Long Refresh Period . . . 4 ms
- Low Refresh Overhead Time . . . As Low As 1.8% of Total Refresh Period
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Unlatched Output
- Common I/O Capability with "Early Write" Feature
- Page-Mode Operation for Faster Access
- Low Power Dissipation
  - Operating . . . 193 mW (Typ)
  - Standby . . . 35 mW (Typ)
- Max Access/Min Cycle Times:

	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	READ-MODIFY-WRITE CYCLE (MIN)
TMS41128B-15	150 ns	85 ns	260 ns	315 ns

- SMOS (Scaled-MOS) N-Channel Technology

16-PIN PLASTIC
DUAL-IN-LINE STACKED PACKAGES †
(TOP VIEW)



† RAS1 (pin 3) selects the lower DRAM, and pin 3 on the upper DRAM is a no connect. RAS2 (pin 4) selects the upper DRAM, and pin 4 on the lower DRAM is a no connect.

PIN NOMENCLATURE	
A0-A7	Address Inputs
CAS	Column-Address Strobe
D	Data In
Q	Data Out
RAS1, RAS2	Row-Address Strobes
V_{DD}	5-V Supply
V_{SS}	Ground
W	Write Enable

4

Dynamic RAMs

description

The TMS41128B consists of two high-speed, 65,536-bit, dynamic random-access memories that are separately packaged. These DRAMs are electrically similar to TMS4164s; however, the pin out is different. The two packages are permanently connected, pin for pin, one on top of the other. The result is a 16-pin memory device organized as 131,072 words of one bit each with essentially the same characteristics of the TMS4164 NMOS dynamic RAM.

A logic low on the RAS1 input selects the lower DRAM; a logic low on the RAS2 input selects the upper DRAM.

The TMS41128B-15 features a RAS access time of 150 ns. Power dissipation is 193 mW typical operating, 35 mW typical standby.

Refresh period is extended to 4 ms, and during this period each of the 256 rows must be strobed with RAS1 and RAS2 in order to retain data. CAS can remain high during the refresh sequence to conserve power.

All inputs and outputs, including clock, are compatible with Series 74 TTL. All address lines and data in are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TMS41128B is offered in 16-pin plastic dual-in-line stacked packages and is guaranteed for operation from 0°C to 70°C. This package is designed for insertion in mounting-hole rows on 300-mil (7,62-mm) centers.

operation

address (A0 through A7)

Sixteen address bits are required to decode 1 of 65,536 storage cell locations. Eight row-address bits are set up on pins A0 through A7 and latched onto the chip by the row-address strobe ($\overline{RAS}1$ or $\overline{RAS}2$). Then the eight column-address bits are set up on pins A0 through A7 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}1$, $\overline{RAS}2$, and $\overline{CAS}$. $\overline{RAS}1$ and $\overline{RAS}2$ are similar to a chip enable in that they activate the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers. When $\overline{CAS}$ is applied to the device, only one of the $\overline{RAS}$ signals (either $\overline{RAS}1$ or $\overline{RAS}2$) must be applied to select either the lower DRAM or the upper DRAM. When a $\overline{RAS}$-only refresh is performed ($\overline{CAS}$ logic high), both $\overline{RAS}1$ and $\overline{RAS}2$ may be applied simultaneously.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$, data out will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data in (D)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. This latch can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data out (Q)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan out of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output goes active after the access time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ is satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low; $\overline{CAS}$ going high returns it to a high-impedance state. In an early write cycle, the output is always in the high-impedance state. In a delayed-write or read-modify-write cycle, the output will follow the sequence for the read cycle.

refresh

A refresh operation must be performed at least every 4 ms on both DRAMs to retain data. Since the output buffer is in the high-impedance state unless $\overline{CAS}$ is applied, The $\overline{RAS}$-only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses (A0 through A7) with both $\overline{RAS}1$ and $\overline{RAS}2$ causes all bits in each row to be refreshed. $\overline{CAS}$ must remain high (inactive) for this refresh sequence.

page mode

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the chip. Thus, the time required to setup and strobe sequential row addresses for the same page is eliminated. To extend beyond the 256 column locations on a single RAM, the row address and $\overline{RAS}$ are applied to multiple 64K RAMs. $\overline{CAS}$ is then decoded to select the proper RAM.

power-up

After power up, $\overline{RAS}1$ and $\overline{RAS}2$ must remain high for 100 μs immediately prior to initialization. Initialization consists of performing eight $\overline{RAS}$ cycles before proper device operation is achieved.

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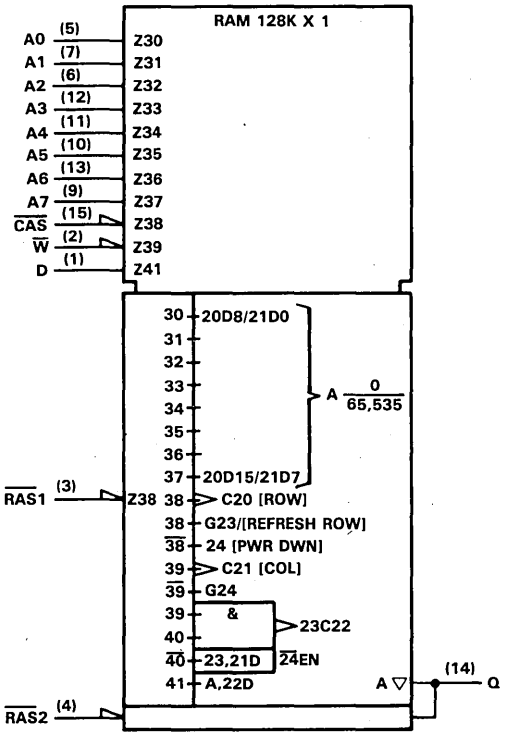
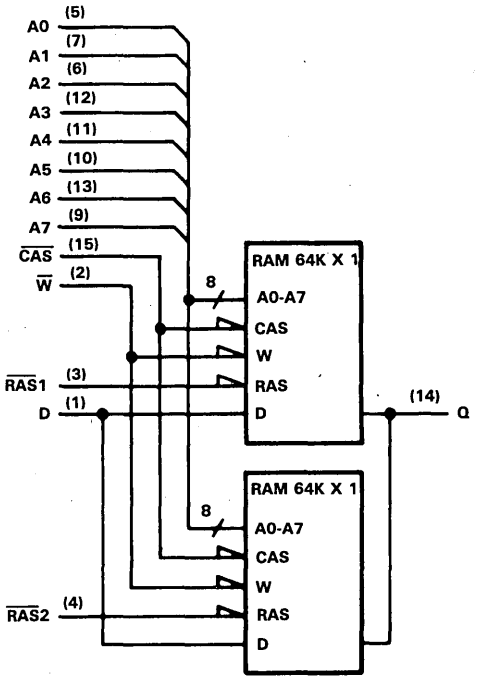
logic symbol†



functional block diagram



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage on any pin except V_{DD} and data out (see Note 1) . . . . . −1.5 V to 10 V
Voltage on V_{DD} supply and data out with respect to V_{SS} . . . . . −1 V to 6 V
Short circuit output current . . . . . 50 mA
Power dissipation . . . . . 2 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values in this data sheet are with respect to V_{SS}.
2. Additional information concerning the handling of ESD sensitive devices is available in a document entitled *"Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies"* in Section 12.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		4.5	5	5.5	V
V_{SS}	Supply voltage			0		V
V_{IH}	High-level input voltage	V_{DD} = 4.5 V	2.4		4.8	V
		V_{DD} = 5.5 V	2.4		6	
V_{IL}	Low-level input voltage (see Notes 3 and 4)		−0.6		0.8	V
T_A	Operating free-air temperature		0		70	°C

NOTES: 3. The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.
4. Due to input protection circuitry, the applied voltage may begin to clamp at −0.6 V. Test conditions must comprehend this occurrence. See application report entitled "TMS4164A and TMS4416 Input Protection Diode" on page 9-5.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 5.8 V, V_{DD} = 5 V, All other pins = 0 V			±20	μA
I_O	Output current (leakage)	V_O = 0.4 to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±20	μA
I_{DD1}	Average operating current during read or write cycle	t_c = minimum cycle, All outputs open		38.5	65	mA
I_{DD2}‡	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, All outputs open		7	10	mA
I_{DD3}	Average refresh current	t_c = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ high, All outputs open			90	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling, All outputs open			90	mA

† All typical values are at T_A = 25°C and nominal supply voltages.
‡ V_{IL} > −0.6 V.

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capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

PARAMETER		TYP†	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs	8	14	pF
$C_{i(D)}$	Input capacitance, data input	8	14	pF
$C_{i(RC)}$	Inpuut capacitance strobe inputs	16	20	pF
$C_{i(W)}$	Input capacitance, write-enable input	16	20	pF
C_o	Output capacitance	10	16	pF

† All typical values are at T_A = 25°C and nominal supply voltages.

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	MIN	MAX	UNIT
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		85	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, Load = 2 Series 74 TTL gates	t_{RAC}		150	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	40	ns

timing requirements over recommended supply voltage range and operating free-air temperature range

		ALT. SYMBOL	MIN	MAX	UNIT
$t_{c(P)}$	Page-mode cycle time	t_{PC}	160		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	260		ns
$t_{c(W)}$	Write cycle time	t_{WC}	260		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	315		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (precharge time)‡	t_{CP}	60		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low§	t_{CAS}	85	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge time)	t_{RP}	100		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low¶	t_{RAS}	150	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	45		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	55		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	55		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	45		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	20		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	110		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	45		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	120		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	45		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	20		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	60		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	120		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	150		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	10		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	85		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{CWD}	75		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	30	65	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{RWD}	150		ns
t_{WLCL}	Delay time, $\overline{W}$ low to $\overline{CAS}$ low (early write cycle)	t_{WCS}	0		ns
t_{rf}	Refresh time interval	t_{REF}		4	ms

NOTE 5: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, V_{IL} max and V_{IH} min must be met at the 10% and 90% points.

† All cycle times assume t_t = 5 ns.

‡ Page mode only.

§ In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$). This applies to page-mode read-modify-write cycles also.

¶ In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).

PARAMETER MEASUREMENT INFORMATION

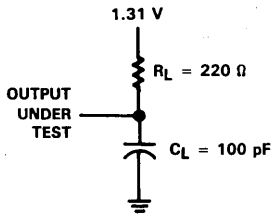
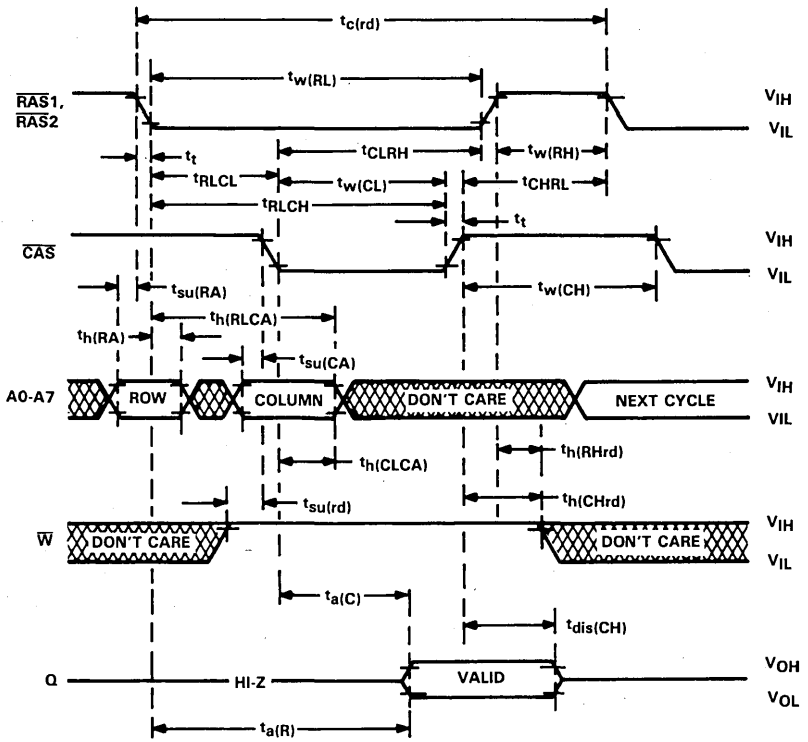
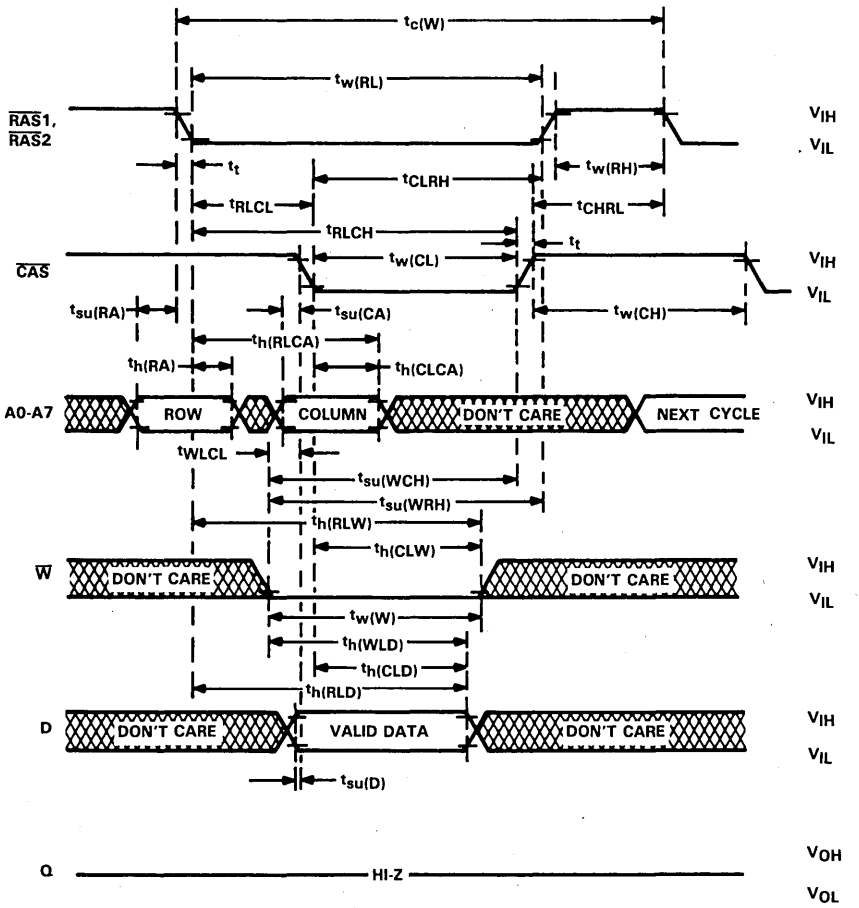


FIGURE 1. LOAD CIRCUIT

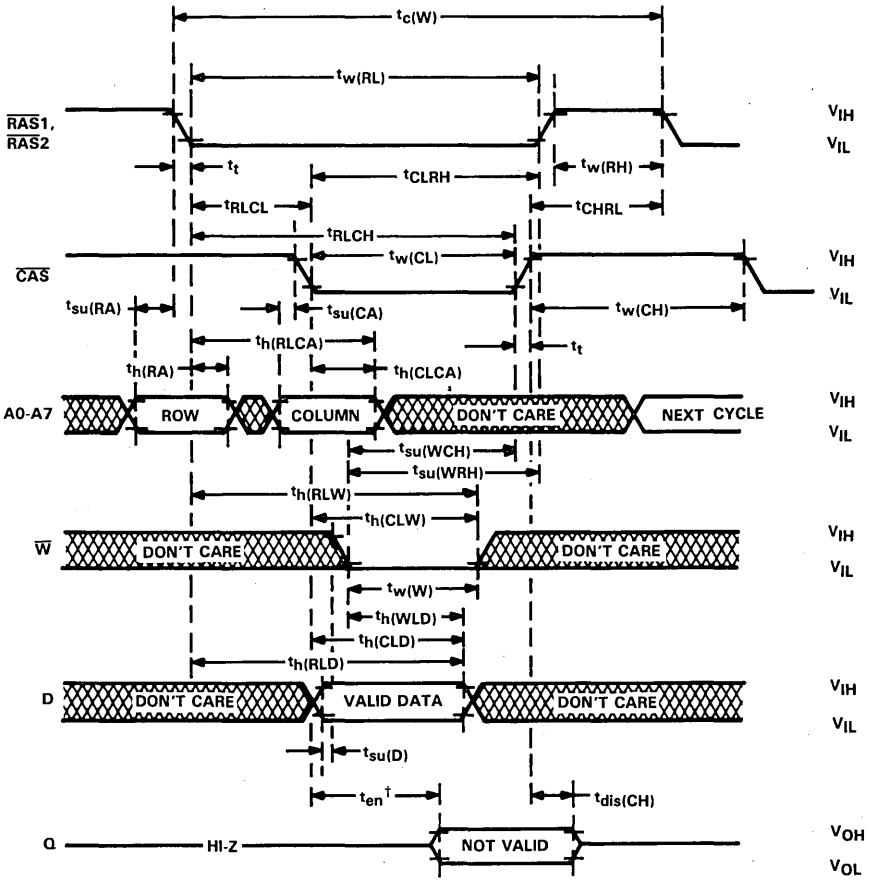
read cycle timing



early write cycle timing

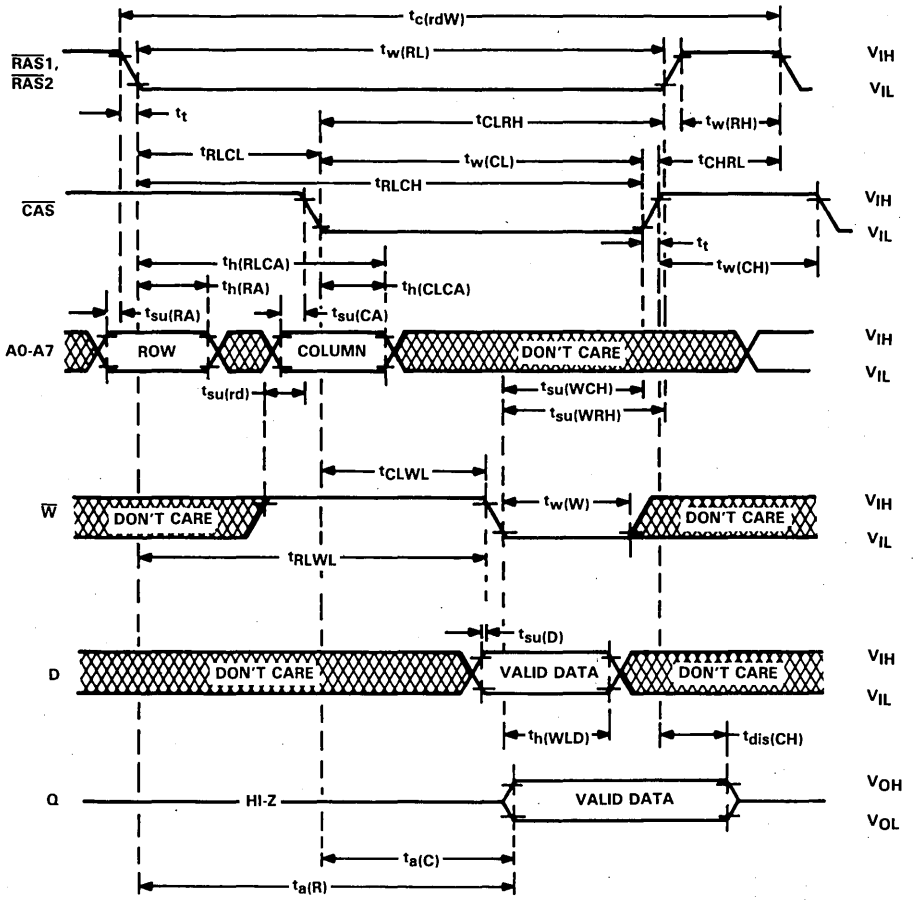


write cycle timing



† The enable time (t_{en}) for a write cycle is equal in duration to the access time from $\overline{CAS}$ ($t_{a(C)}$) in a read cycle; but the active levels at the output are invalid.

read-modify-write cycle timing



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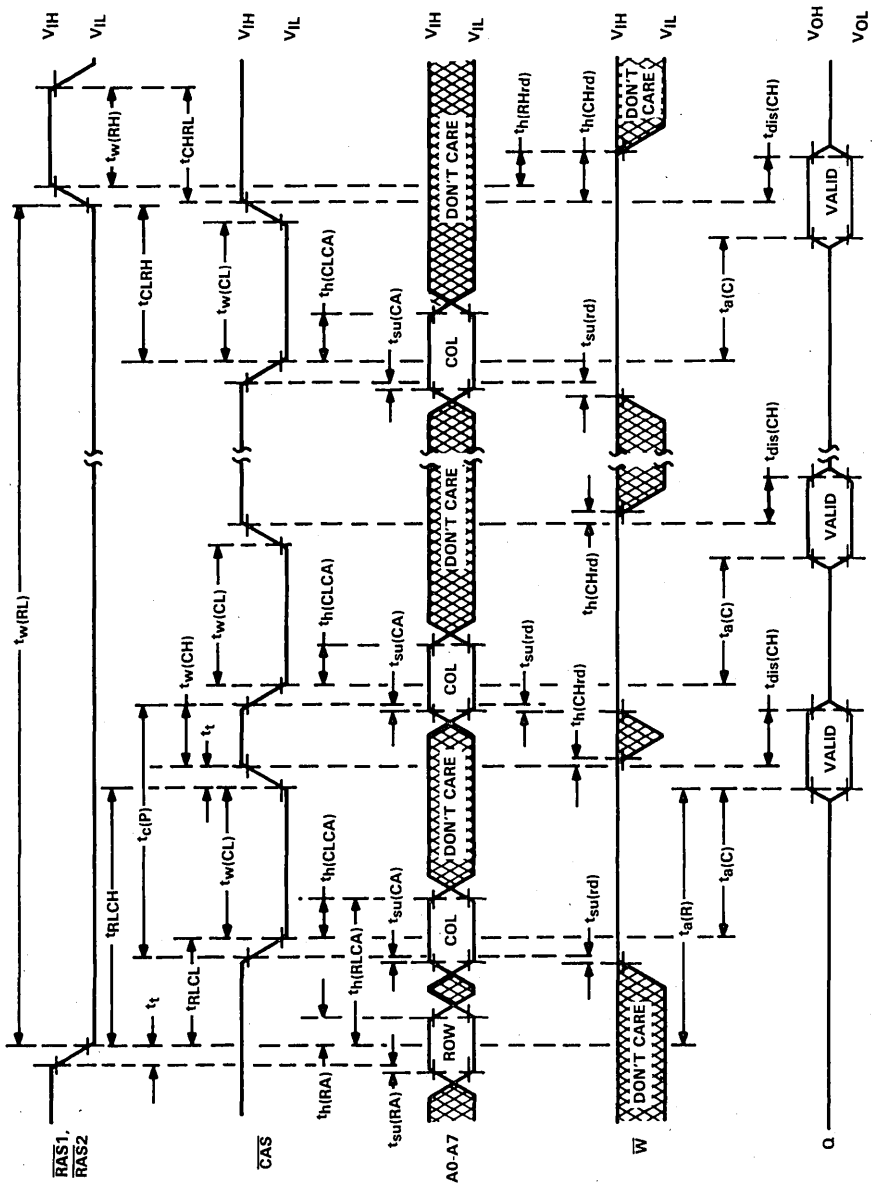
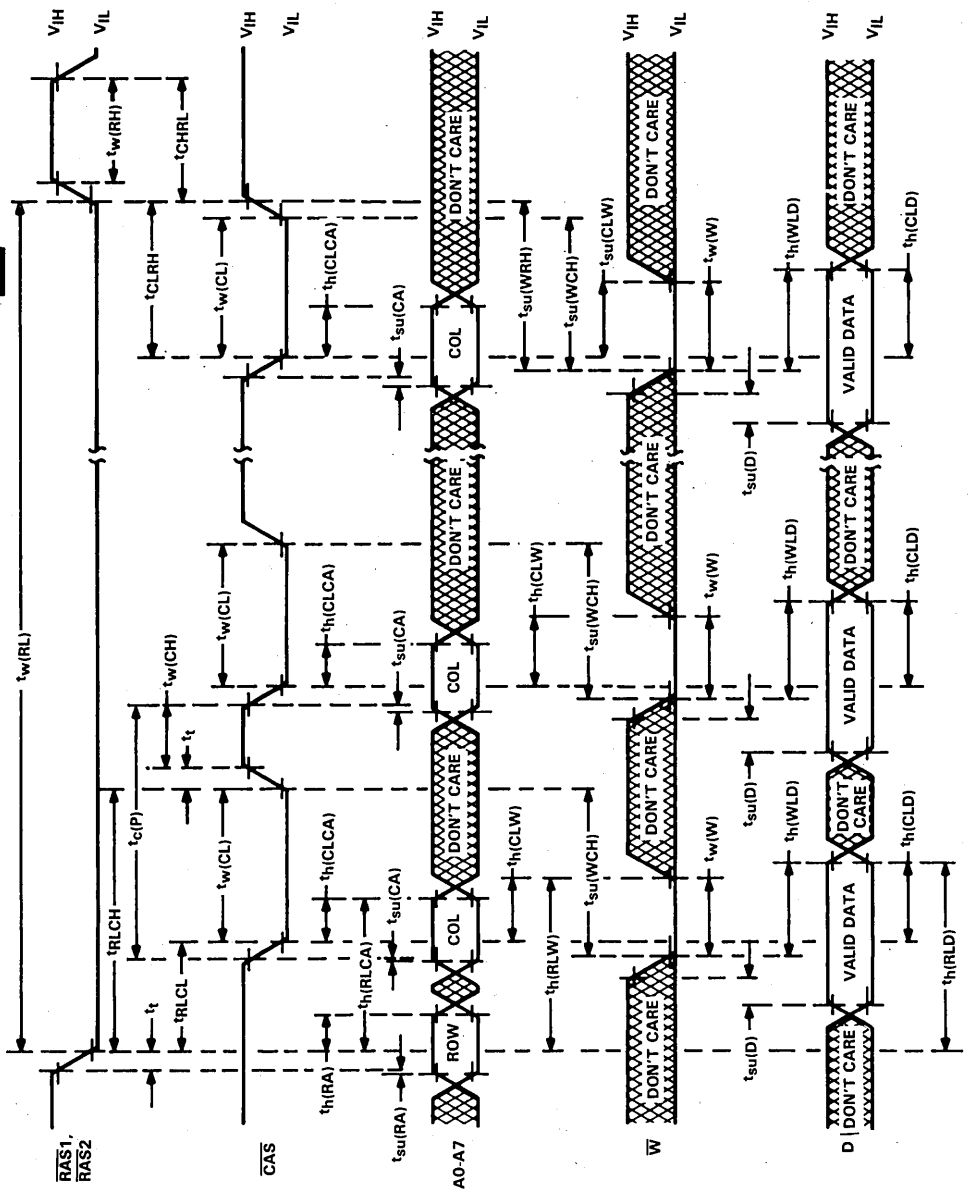
page-mode read cycle timing



NOTE 6: A write cycle or a read-modify-write cycle can be intermixed with read cycles as long as the write and read-modify-write timing specifications are not violated.

page-mode write cycle timing



NOTE 7: A read cycle or a read-modify-write cycle can be intermixed with write cycles as long as the read and read-modify-write timing specifications are not violated.

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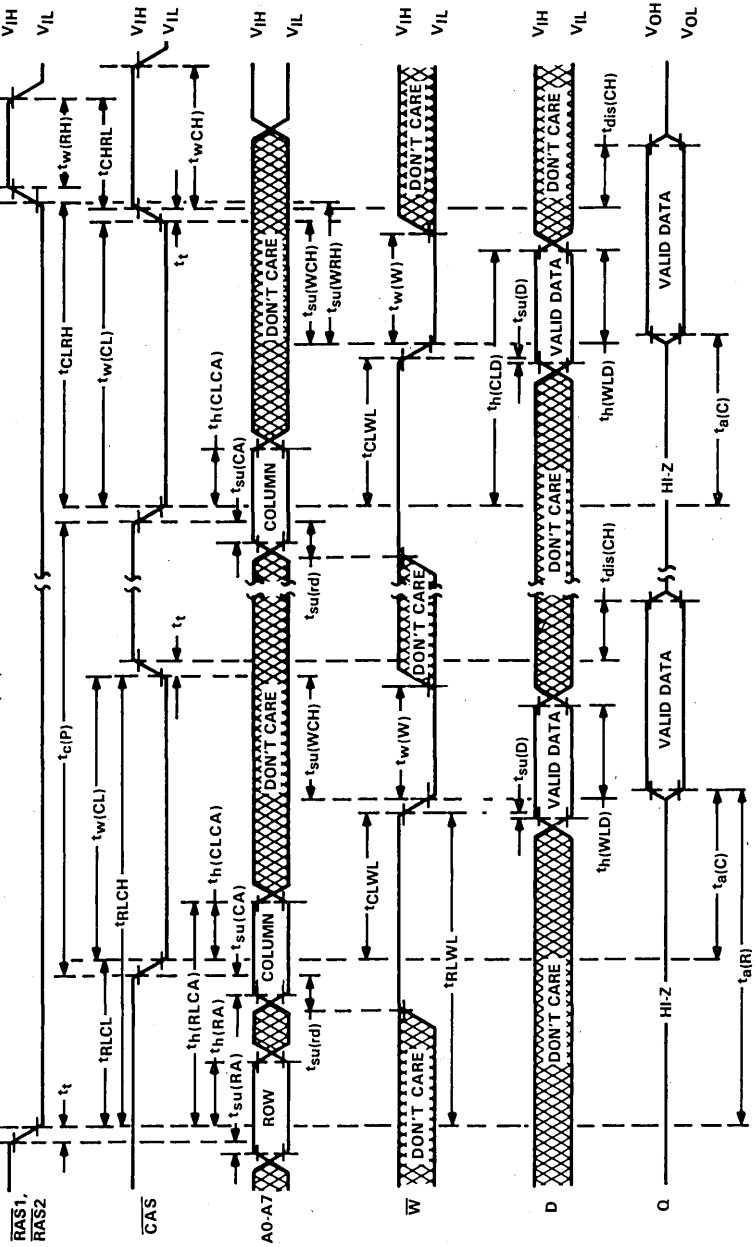
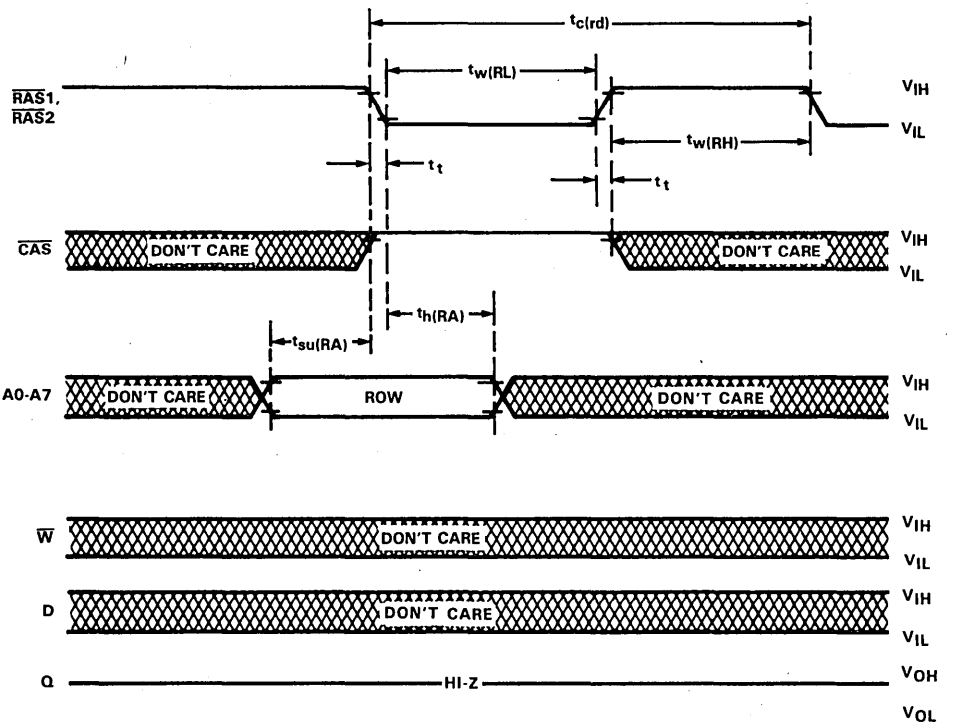
page-mode read-modify-write cycle timing



NOTE 8: A read or a write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

$\overline{\text{RAS}}$-only refresh timing



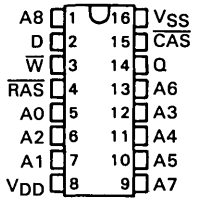
MAY 1983—REVISED NOVEMBER 1985

- 262,144 X 1 Organization
- Single 5-V Supply (10% Tolerance)
- JEDEC Standardized Pinout
- Upward Pin Compatible with TMS4164 (64K Dynamic RAM)
- Performance Ranges:

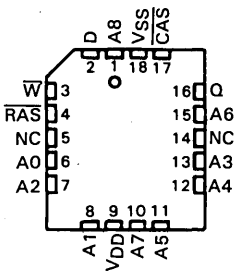
DEVICE	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)
TMS4256-12 TMS4257-12	120 ns	60 ns	230 ns
TMS4256-15 TMS4257-15	150 ns	75 ns	260 ns
TMS4256-20 TMS4257-20	200 ns	100 ns	330 ns

- Long Refresh Period . . . 4 ms (Max)
- Low Refresh Overhead Time . . . As Low As 1.3% of Total Refresh Period
- On-Chip Substrate Bias Generator
- Operations of the TMS4256/TMS4257 Can Be Controlled by TI's THCT4502 Dynamic RAM Controller
- All Inputs, Outputs, and Clocks Fully TTL Compatible
- 3-State Unlatched Output
- Common I/O Capability with "Early Write" Feature
- Page ('4256) or Nibble-Mode ('4257) Options for Faster Access Operation
- Power Dissipation As Low As
  —Operating . . . 275 mW (Typ)
  —Standby . . . 12.5 mW (Typ)
- $\overline{RAS}$-Only Refresh Mode
- Hidden Refresh Mode

N PACKAGE
(TOP VIEW)



FM PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A8	Address Inputs
$\overline{CAS}$	Column-Address Strobe
D	Data In
NC	No Connection
Q	Data Out
$\overline{RAS}$	Row-Address Strobe
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

- $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Mode
- Available with MIL-STD-883B Processing and L(0°C to 70°C), E(−40°C to 85°C), or S(−55°C to 100°C) Temperature Ranges

description

The '4256 and '4257 are high-speed, 262,144-bit dynamic random-access memories, organized as 262,144 words of one bit each. They employ state-of-the-art SMOS (scaled MOS) N-channel double-level polysilicon/polycide gate technology for very high performance combined with low cost and improved reliability.

These devices feature maximum $\overline{RAS}$ access times of 120 ns, 150 ns, or 200 ns. Typical power dissipation is as low as 275 mW operating and 12.5 mW standby.

New SMOS technology permits operation from a single 5-V supply, reducing system power supply and decoupling requirements, and easing board layout. I_{DD} peaks are 125 mA typical, and a −1-V input voltage undershoot can be tolerated, minimizing system noise considerations.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address and data-in lines are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The '4256 and '4257 are offered in 16-pin plastic dual-in-line and 18-lead plastic chip carrier packages. They are guaranteed for operation from 0°C to 70°C. The dual-in-line package is designed for insertion in mounting-hole rows on 7,62-mm (300-mil) centers.

operation

address (A0 through A8)

Eighteen address bits are required to decode 1 of 262,144 storage cell locations. Nine row-address bits are set up on pins A0 through A8 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the nine column-address bits are set up on pins A0 through A8 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$, data out will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data in (D)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. This latch can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data out (Q)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan out of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output goes active after the access time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ is satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low; $\overline{CAS}$ going high returns it to a high-impedance state. In a read-modify-write cycle, the output will follow the sequence for the read cycle.

refresh

A refresh operation must be performed at least once every four milliseconds to retain data. This can be achieved by strobing each of the 256 rows (A0-A7). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, thus conserving power as the output buffer remains in the high-impedance state.

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$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh

The $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh is utilized by bringing $\overline{\text{CAS}}$ low earlier than $\overline{\text{RAS}}$ (see parameter t_{CLRL}) and holding it low after $\overline{\text{RAS}}$ falls (see parameter t_{RLCHR}). For successive $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycles, $\overline{\text{CAS}}$ can remain low while cycling $\overline{\text{RAS}}$. The external address is ignored and the refresh address is generated internally.

hidden refresh

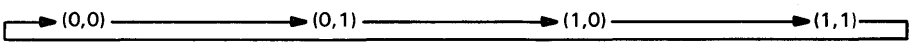
Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{\text{CAS}}$ at V_{IL} after a read operation and cycling $\overline{\text{RAS}}$ after a specified precharge period, similar to a "$\overline{\text{RAS}}$-only" refresh cycle. The external address is also ignored during the hidden refresh cycles.

page mode (TMS4256)

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing random column addresses onto the chip. Thus, the time required to setup and strobe sequential row addresses for the same page is eliminated. The maximum number of columns that can be addressed is determined by $t_{w(RL)}$, the maximum $\overline{\text{RAS}}$ low pulse duration.

nibble mode (TMS4257)

Nibble-mode operation allows high-speed serial read, write, or read-modify-write access of 1 to 4 bits of data. The first bit is accessed in the normal manner with read data coming out at $t_{a(C)}$ time. The next sequential nibble bits can be read or written by cycling $\overline{\text{CAS}}$ while $\overline{\text{RAS}}$ remains low. The first bit is determined by the row and column addresses, which need to be supplied only for the first access. Column A8 and row A8 (CA8, RA8) provide the two binary bits for initial selection of the nibble addresses. Thereafter, the falling edge of $\overline{\text{CAS}}$ will access the next bit of the circular 4-bit nibble in the following sequence:

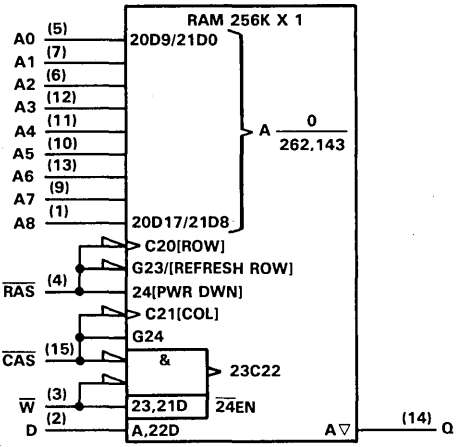


In nibble-mode, all normal memory operations (read, write, or ready-modify-write) may be performed in any desired combination.

power-up

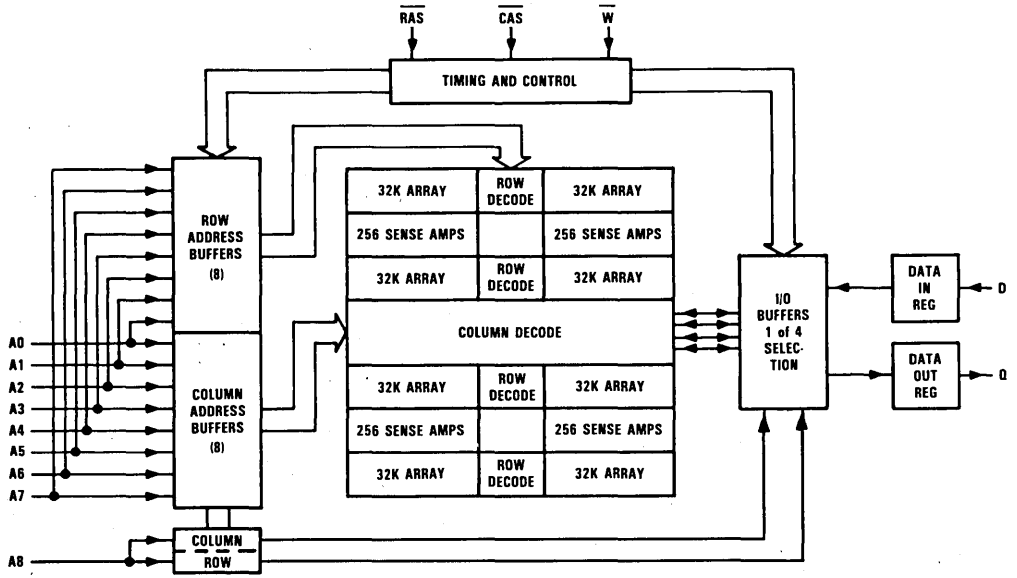
To achieve proper device operation, an initial pause of 200 μs is required after power up followed by a minimum of eight initialization cycles.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
The pin numbers shown are for the 16-pin dual-in-line package.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range for any pin including V_{DD} supply (see Note 1) . . . . . −1 V to 7 V
Short circuit output current . . . . . 50 mA
Power dissipation . . . . . 1 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	−1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as maximum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TMS4256-12 TMS4257-12			UNIT
			MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 6.5 V, V_{DD} = 5 V, All other pins = 0 V to 6.5 V			±10	μA
I_O	Output current (leakage)	V_O = 0 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10	μA
I_{DD1}	Average operating current during read or write cycle	t_c = minimum cycle, Output open		65	78	mA
I_{DD2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, Output open		2.5	4.5	mA
I_{DD3}	Average refresh current	t_c = minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high, Output open		45	60	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling, Output open		35	48	mA
I_{DD5}	Average nibble-mode current	$t_{c(N)}$ = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling, Output open		32	44	mA

PARAMETER		TEST CONDITIONS	TMS4256-15 TMS4257-15			TMS4256-20 TMS4257-20			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4			2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 6.5 V, V_{DD} = 5 V, All other pins = 0 V to 6.5 V			±10			±10	μA
I_O	Output current (leakage)	V_O = 0 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10			±10	μA
I_{DD1}	Average operating current during read or write cycle	t_c = minimum cycle, Output open		55	68		45	58	mA
I_{DD2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, Output open		2.5	4.5		2.5	4.5	mA
I_{DD3}	Average refresh current	t_c = minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high, Output open		40	53		35	48	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling, Output open		30	43		25	35	mA
I_{DD5}	Average nibble-mode current	$t_{c(N)}$ = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling, Output open		27	39		22	32	mA

†All typical values are at T_A = 25°C and nominal supply voltages.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

PARAMETER		TYP†	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs	4	7	pF
$C_{i(D)}$	Input capacitance, data input	4	7	pF
$C_{i(RC)}$	Input capacitance strobe inputs	4	8	pF
$C_{i(W)}$	Input capacitance, write enable input	4	8	pF
C_o	Output capacitance	5	10	pF

†All typical values are at T_A = 25°C and nominal supply voltages.

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TMS4256-12 TMS4257-12		UNIT
				MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	$t_{RLCL} \geq$ MAX, C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		60	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{RAC}		120	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	30	ns

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TMS4256-15 TMS4257-15		TMS4256-20 TMS4257-20		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	$t_{RLCL} \geq$ MAX, C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		75		100	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{RAC}		150		200	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	30	0	35	ns

timing requirements over recommended supply voltage range and operating free-air temperature range

		ALT. SYMBOL	TMS4256-12 TMS4257-12		UNIT
			MIN	MAX	
$t_{c(P)}$	Page-mode cycle time (read or write cycle)	t_{PC}	120		ns
$t_{c(PM)}$	Page-mode cycle time (read-modify-write cycle)	t_{PCM}	165		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	230		ns
$t_{c(W)}$	Write cycle time	t_{WC}	230		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	275		ns
$t_{w(CH)P}$	Pulse duration, $\overline{CAS}$ high (page mode)	t_{CP}	50		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (non-page mode)	t_{CPN}	25		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low‡	t_{CAS}	60	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high	t_{RP}	100		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low§	t_{RAS}	120	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	40		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		ns
$t_{su(WCL)}$	Early write-command setup time before $\overline{CAS}$ low	t_{WCS}	0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	40		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	40		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	20		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	15		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	80		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	35		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	95		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	35		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	10		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	35		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	95		ns

Continued next page.

NOTE 3: Timing measurements are referenced to V_{IL} max and V_{IH} min.

†All cycle times assume t_t = 5 ns.

‡In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$). This applies to page-mode read-modify-write also.

§In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).

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timing requirements over recommended supply voltage range and operating free-air temperature range (continued)

		ALT. SYMBOL	TMS4256-12 TMS4257-12		UNIT
			MIN	MAX	
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	120		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	60		ns
t_{RLCHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high¶	t_{CHR}	25		ns
t_{CLRL}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low¶	t_{CSR}	25		ns
t_{RHCL}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low¶	t_{RPC}	20		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{CWD}	60		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	25	60	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{RWD}	120		ns
t_{rf}	Refresh time interval	t_{REF}		4	ms

Continued next page.

NOTE 3: Timing measurements are referenced to V_{IL} max and V_{IH} min.

¶$\overline{CAS}$-before-$\overline{RAS}$ refresh only.

timing requirements over recommended supply voltage range and operating free-air temperature range (continued)

		ALT. SYMBOL	TMS4256-15 TMS4257-15		TMS4256-20 TMS4257-20		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(P)}$	Page-mode cycle time (read or write cycle)	t_{PC}	145		190		ns
$t_{c(PM)}$	Page-mode cycle time (read-modify-write cycle)	t_{PCM}	190		245		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	260		330		ns
$t_{c(W)}$	Write cycle time	t_{WC}	260		330		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	305		370		ns
$t_{w(CH)P}$	Pulse duration, $\overline{CAS}$ high (page mode)	t_{CP}	60		80		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (non-page mode)	t_{CPN}	25		30		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low‡	t_{CAS}	75	10,000	100	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high	t_{RP}	100		120		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low§	t_{RAS}	150	10,000	200	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	45		55		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	50	3	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		0		ns
$t_{su(WCL)}$	Early write-command setup time before $\overline{CAS}$ low	t_{WCS}	0		0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	45		60		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	45		60		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	25		30		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	15		20		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	100		130		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	45		55		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	120		155		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	45		55		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	10		15		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	45		55		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	120		155		ns

Continued next page.

NOTE 3: Timing measurements are referenced to V_{IL} max and V_{IH} min.

†All cycle times assume t_t = 5 ns.

‡In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$). This applies to page-mode read-modify-write also.

§In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).

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timing requirements over recommended supply voltage range and operating free-air temperature range (concluded)

		ALT. SYMBOL	TMS4256-15 TMS4257-15		TMS4256-20 TMS4257-20		UNIT
			MIN	MAX	MIN	MAX	
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	150		200		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	75		100		ns
t_{RLCHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high¶	t_{CHR}	30		35		ns
t_{CLRL}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low¶	t_{CSR}	30		35		ns
t_{RHCL}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low¶	t_{RPC}	20		25		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{CWD}	70		90		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	25	75	30	100	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{RWD}	145		190		ns
t_{rf}	Refresh time interval	t_{REF}		4		4	ms

NOTE 3: Timing measurements are referenced to V_{IL} max and V_{IH} min.
¶$\overline{CAS}$-before-$\overline{RAS}$ refresh only.

NIBBLE-MODE CYCLE

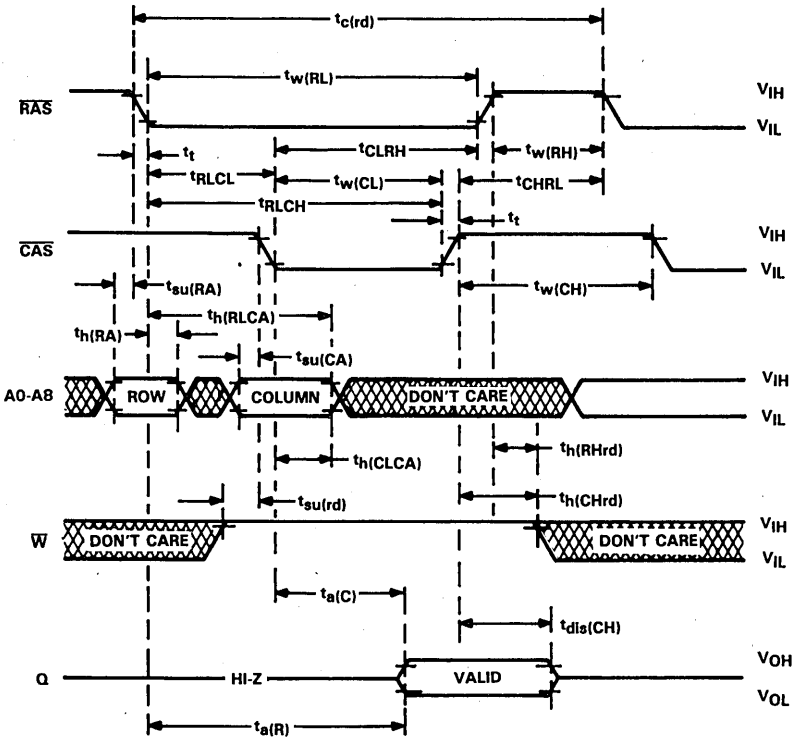
switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		ALT. SYMBOL	TMS4257-12		TMS4257-15		TMS4257-20		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(CN)}$	Nibble-mode access time from $\overline{CAS}$	t_{NCAC}		30		40		50	ns

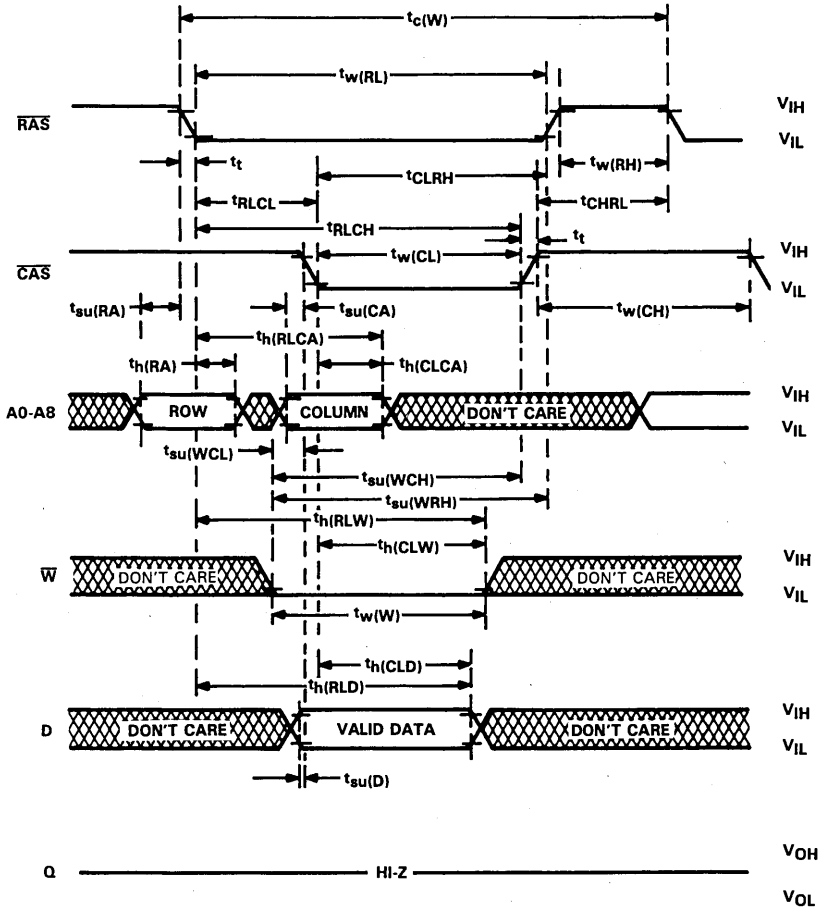
timing requirements over recommended supply voltage range and operating free-air temperature range

		ALT. SYMBOL	TMS4257-12		TMS4257-15		TMS4257-20		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(N)}$	Nibble-mode cycle time	t_{NC}	60		75		90		ns
$t_{c(rdWN)}$	Nibble-mode read-modify-write cycle time	t_{NRMW}	85		105		130		
t_{CLRHN}	Nibble-mode delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{NRSH}	30		40		50		
t_{CLWLN}	Nibble-mode delay time, $\overline{CAS}$ to $\overline{W}$ delay	t_{NCWD}	25		30		40		
$t_{w(CLN)}$	Nibble-mode pulse duration, $\overline{CAS}$ low	t_{NCAS}	30		40		50		
$t_{w(CHN)}$	Nibble-mode pulse duration, $\overline{CAS}$ high	t_{NCP}	20		25		30		
$t_{w(CRWN)}$	Nibble-mode read-modify-write pulse duration, $\overline{CAS}$ low	t_{NCRW}	55		70		90		
$t_{su(WCHN)}$	Nibble-mode write command setup time before $\overline{CAS}$ high	t_{NCWL}	25		35		45		

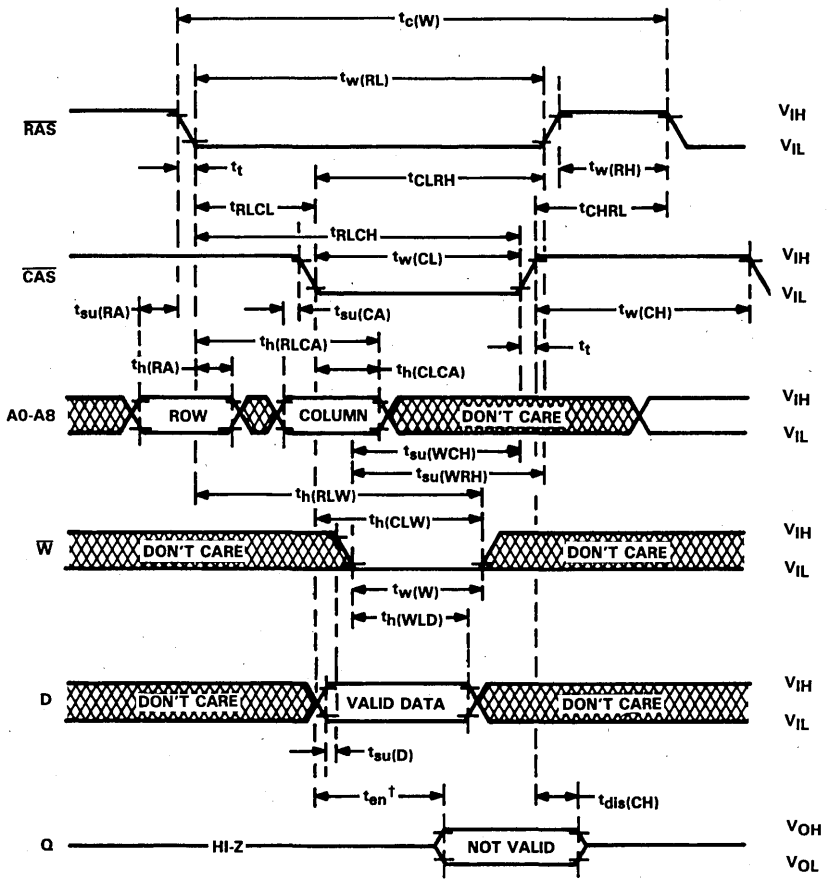
read cycle timing



early write cycle timing



write cycle timing



†The enable time (t_{en}) for a write cycle is equal in duration to the access time from $\overline{CAS}$ ($t_{a(C)}$) in a read cycle; but the active levels at the output are invalid.

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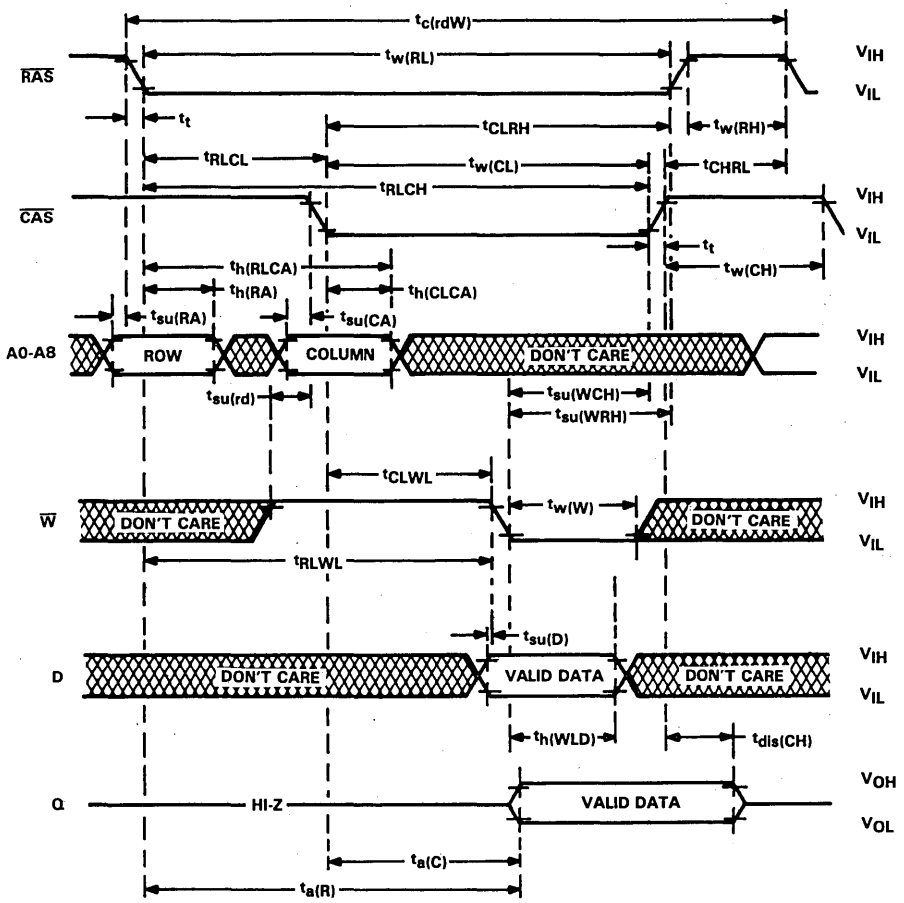
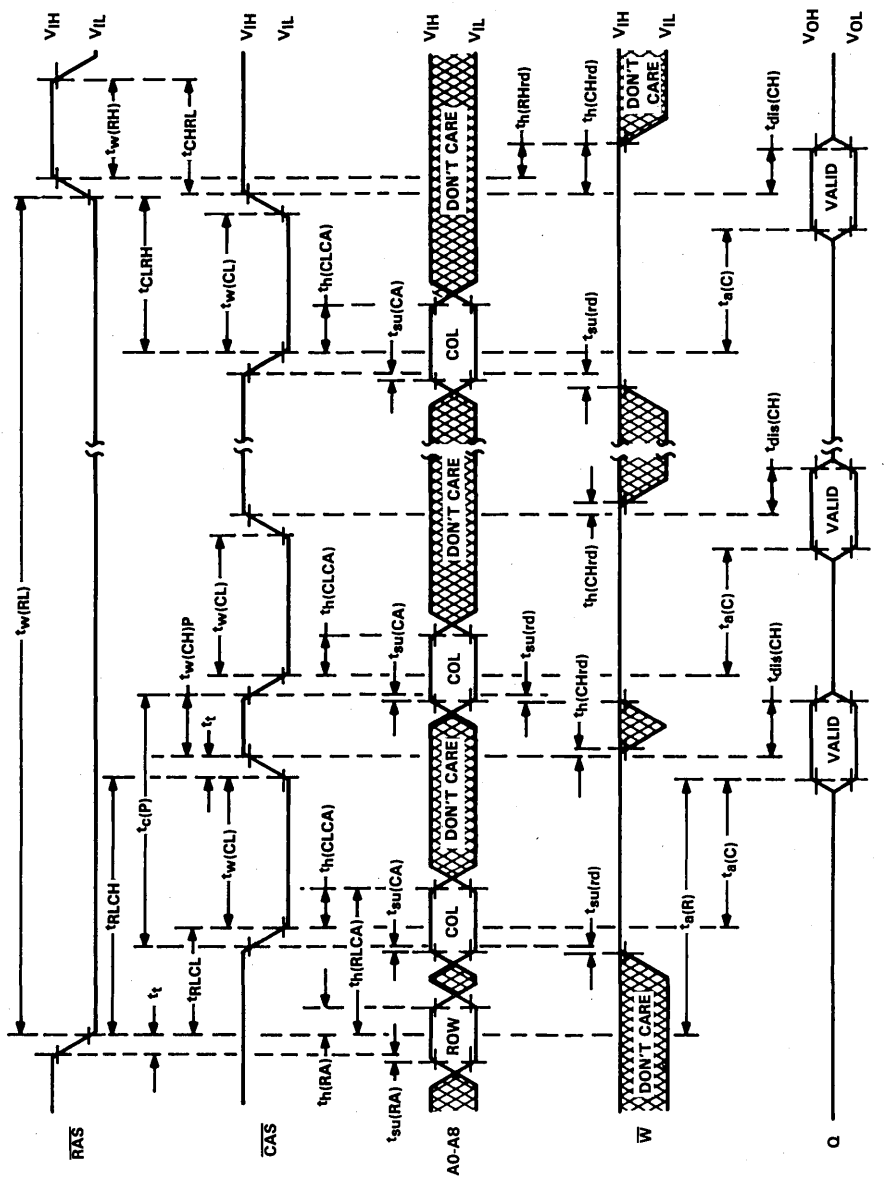
read-write/read-modify-write cycle timing

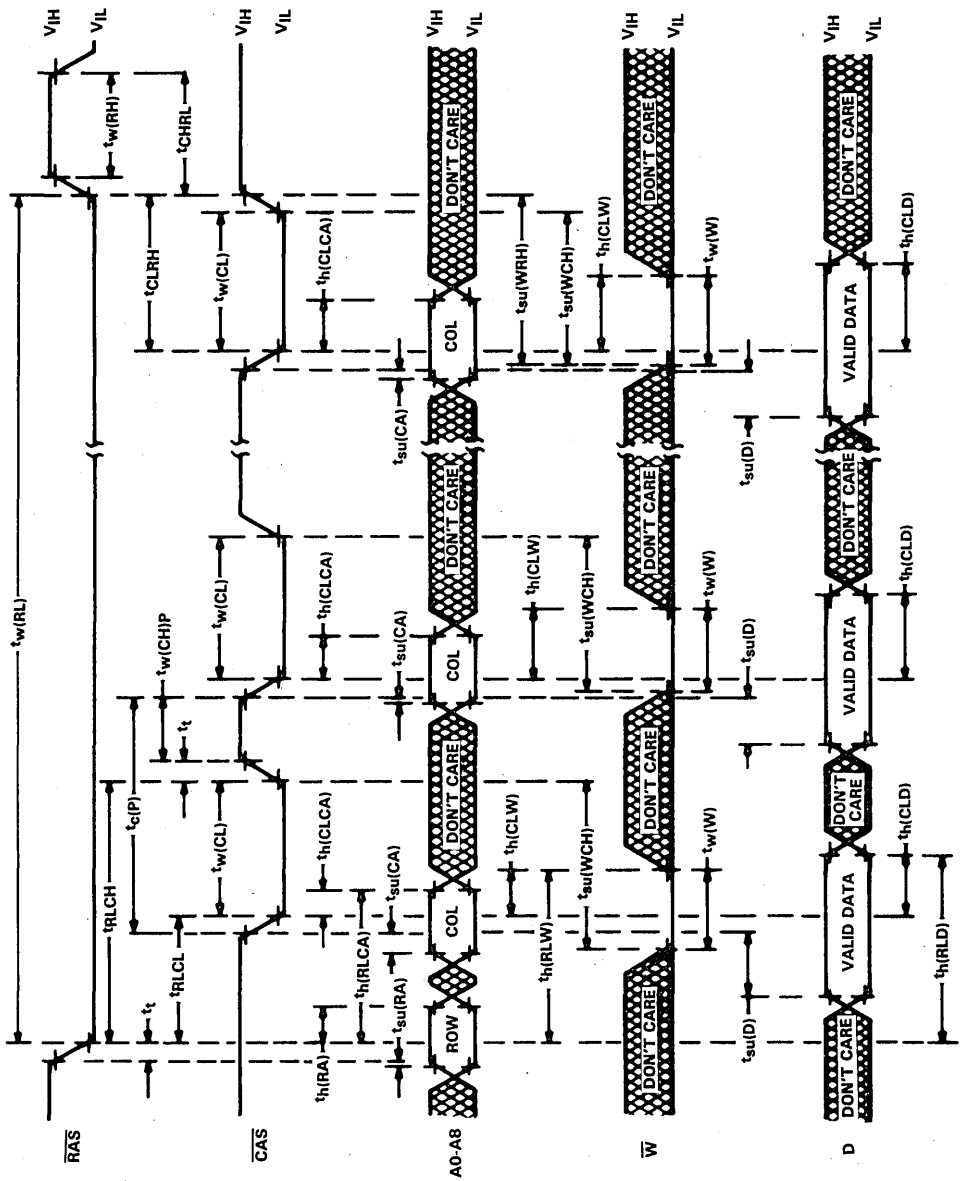


page-mode read cycle timing



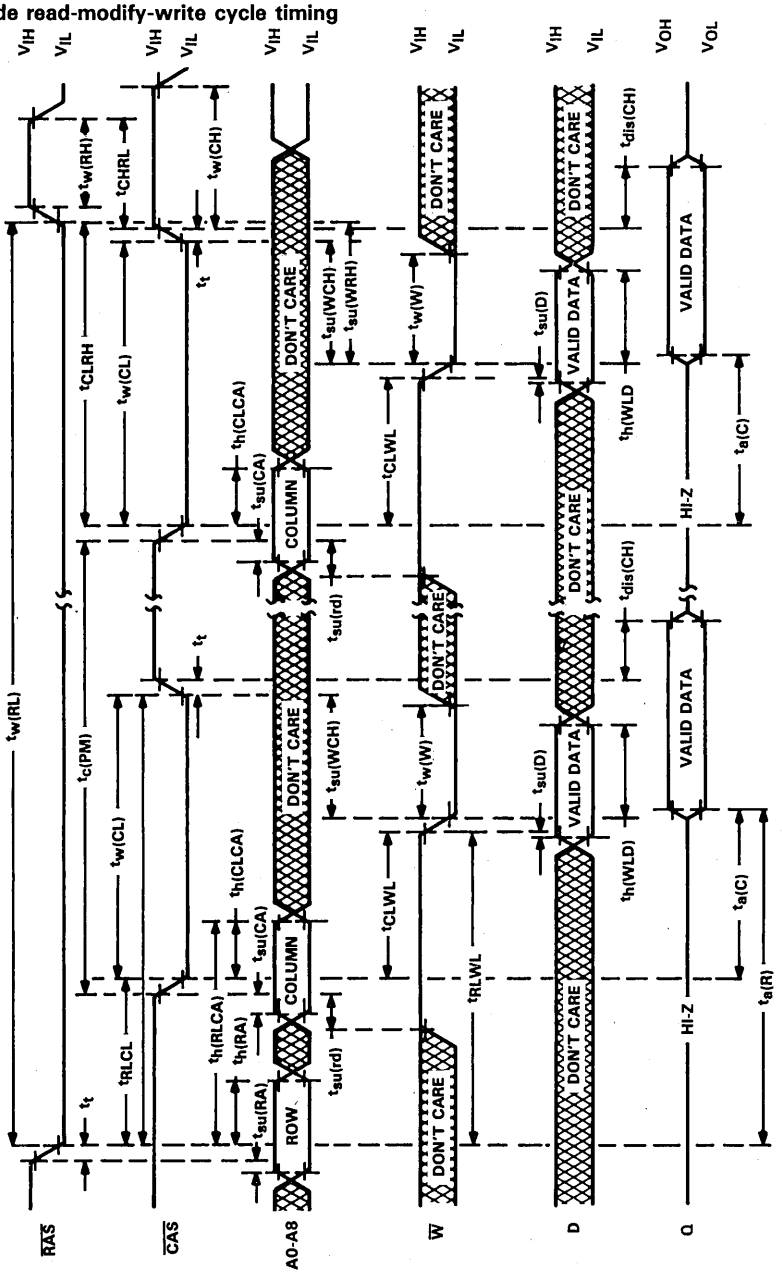
NOTE 4: A write cycle or a read-modify-write cycle can be intermixed with read cycles as long as the write and read-modify-write timing specifications are not violated.

page-mode write cycle timing



NOTE 5: A read cycle or a read-modify-write cycle can be intermixed with write cycles as long as read and read-modify-write timing specifications are not violated.

page-mode read-modify-write cycle timing



NOTE 6: A read or a write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

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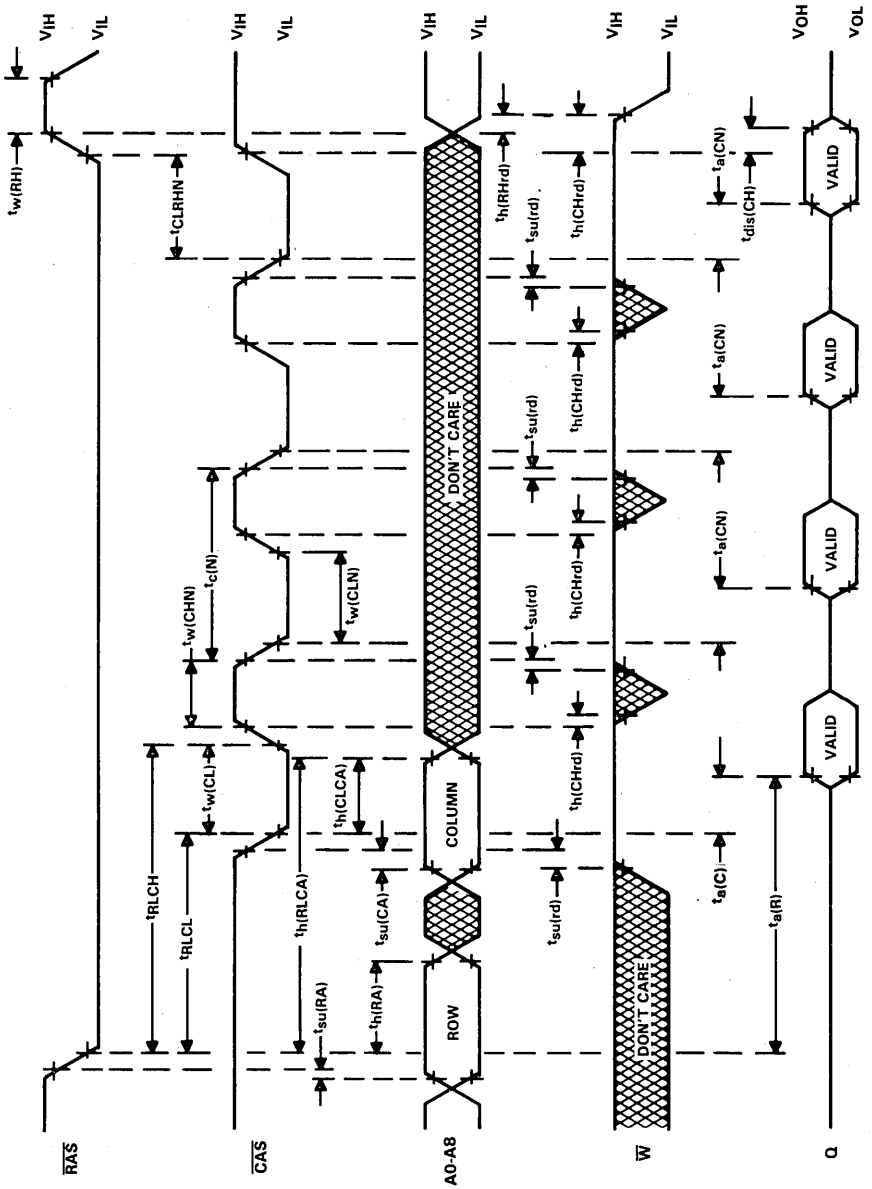
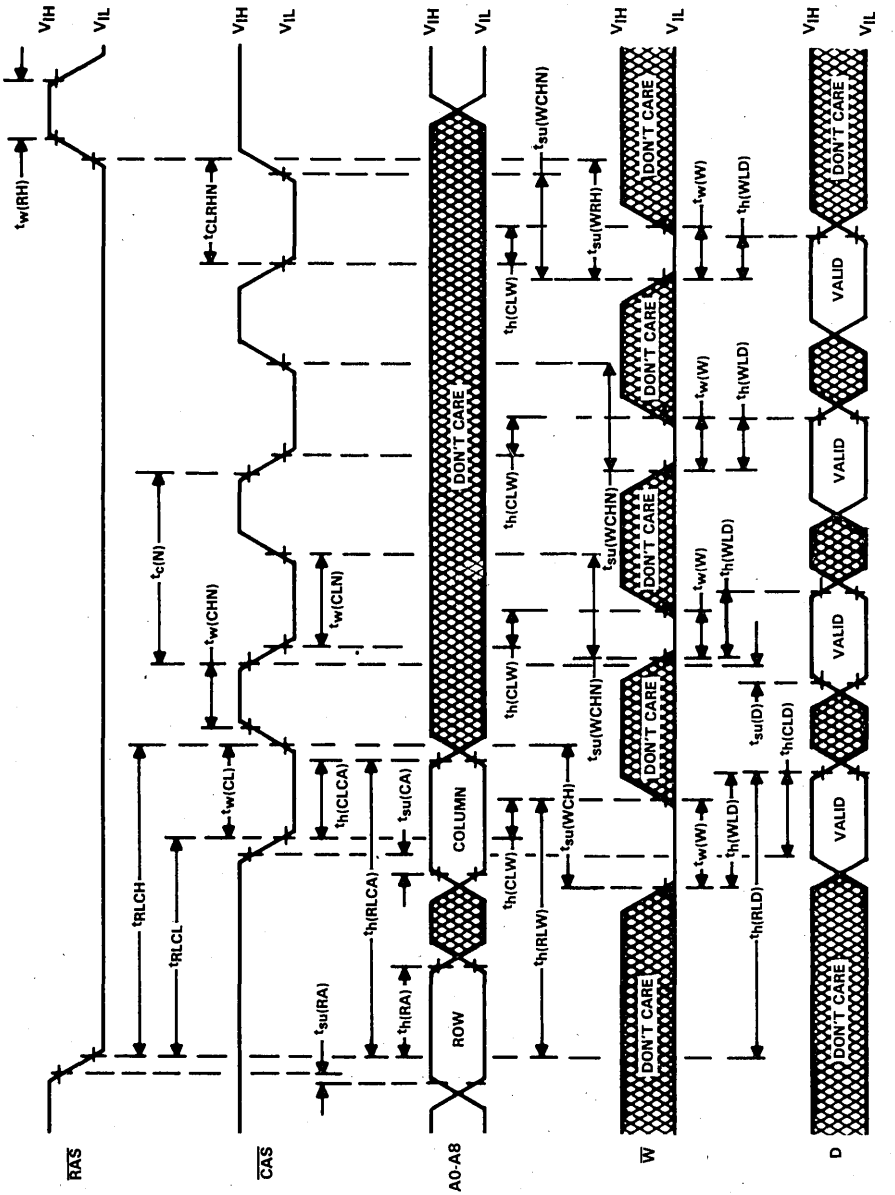
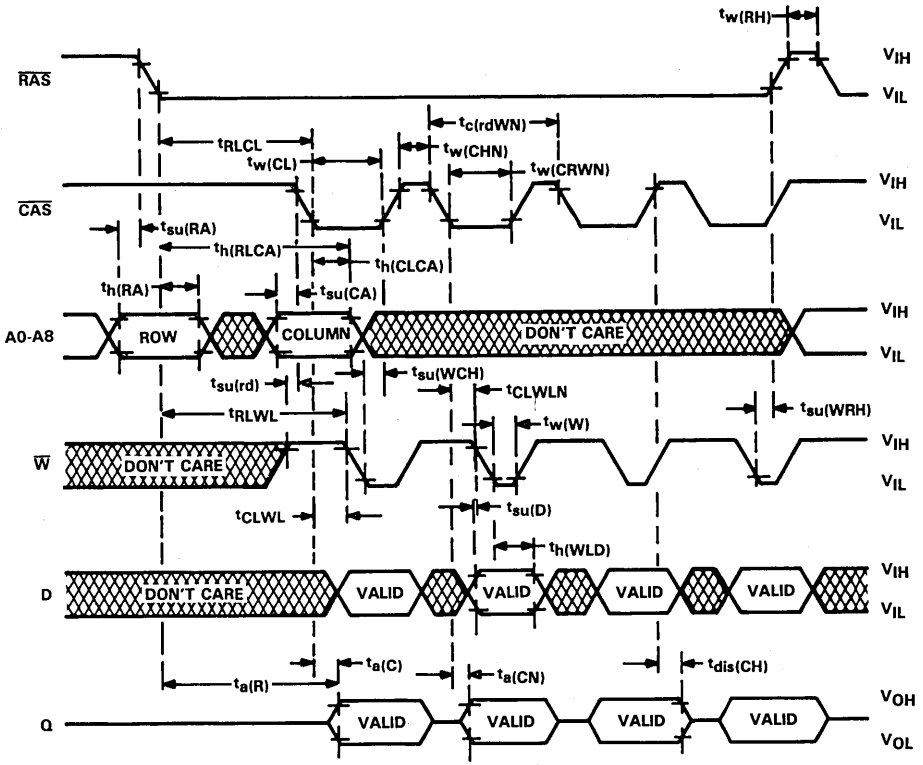
nibble-mode read cycle timing



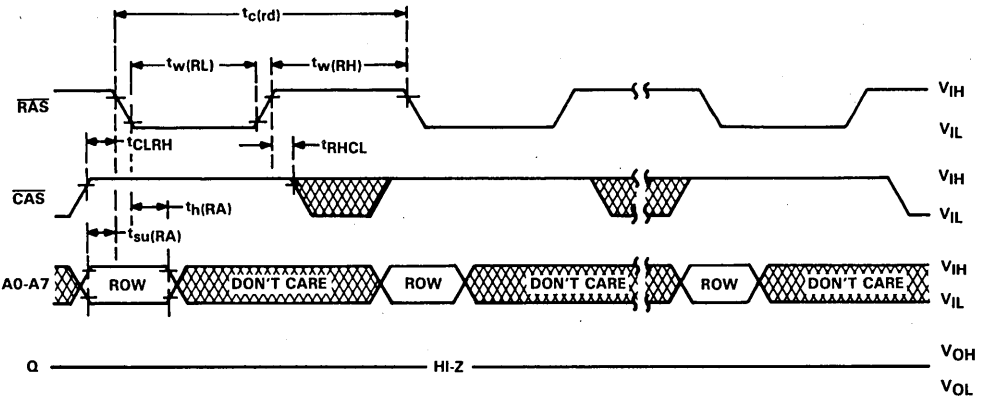
nibble-mode write cycle timing



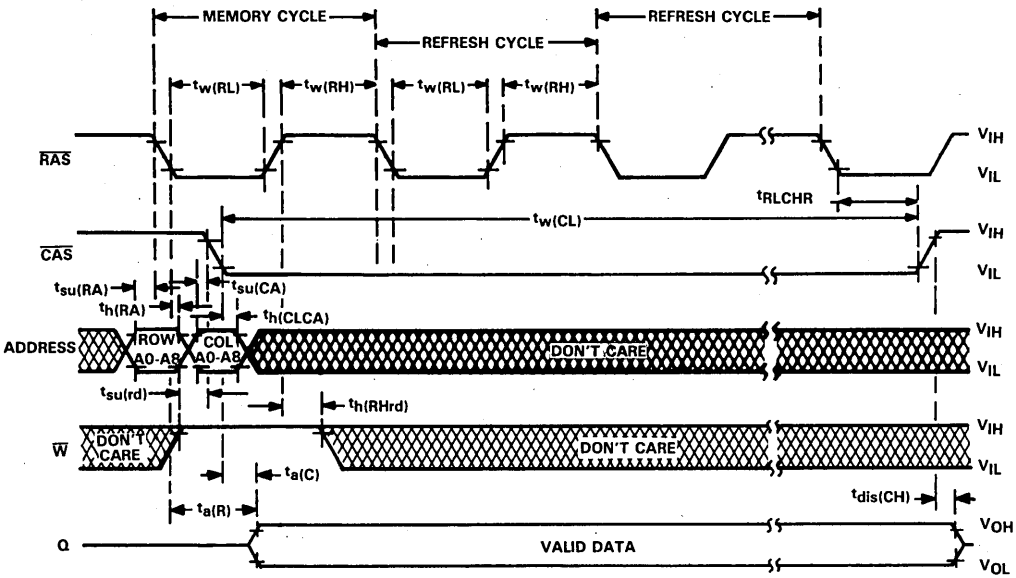
nibble-mode read-modify-write-cycle timing



RAS-only refresh cycle timing



hidden refresh cycle timing



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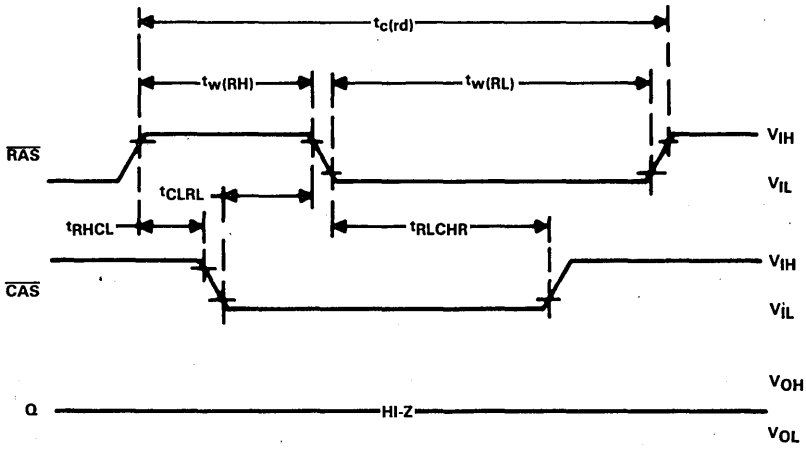
automatic ($\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$) refresh cycle timing



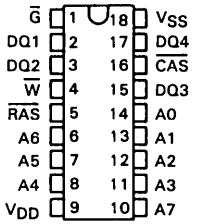
AUGUST 1980—REVISED NOVEMBER 1985

- 16,384 X 4 Organization
- Single 5-V Supply (10% Tolerance)
- Performance Ranges:

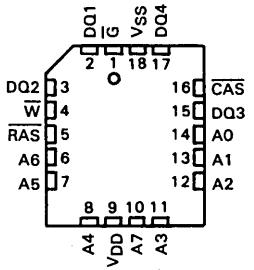
	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	READ-MODIFY-WRITE CYCLE (MIN)
TMS4416-12	120 ns	70 ns	230 ns	315 ns
TMS4416-15	150 ns	80 ns	260 ns	365 ns
TMS4416-20	200 ns	120 ns	330 ns	445 ns

- Available with MIL-STD-883B Processing and L(0°C to 70°C), E(−40°C to 85°C), or S(−55°C to 100°C) Temperature Ranges
- Long Refresh Period . . . 4 ms
- Low Refresh Overhead Time . . . As Low As 1.7% of Total Refresh Period
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Unlatched Outputs
- Early Write or $\overline{G}$ to Control Output Buffer Impedance
- Page-Mode Operation for Faster Access
- Low Power Dissipation
  - Operation . . . 200 mW (Typ)
  - Standby . . . 17.5 mW (Typ)
- SMOS (Scaled-MOS) N-Channel Technology

N PACKAGE
(TOP VIEW)



FP PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A7	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1-DQ4	Data In/Data Out
$\overline{G}$	Output Enable
$\overline{RAS}$	Row-Address Strobe
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The TMS4416 is a high-speed, 65,536-bit, dynamic, random-access memory, organized as 16,384 words of 4 bits each. It employs state-of-the-art SMOS (scaled MOS) N-channel double-level polysilicon gate technology for very high performance combined with low cost and improved reliability.

The TMS4416 features $\overline{RAS}$ access times to 120 ns maximum. Power dissipation is 200 mW typical operating, 17.5 mW typical standby.

SMOS technology permits operation from a single 5-V supply, reducing system power supply and decoupling requirements, and easing board layout. I_{DD} peaks have been reduced to 60 mA typical, and a −1-V input voltage undershoot can be tolerated, minimizing system noise considerations. Input clamp diodes are used to ease system design.

Refresh period is extended to 4 milliseconds, and during this period each of the 256 rows must be strobed with $\overline{RAS}$ in order to retain data. $\overline{CAS}$ can remain high during the refresh sequence to conserve power.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address lines and data in are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TMS4416 is offered in 18-pin plastic dual-in-line and 18-lead plastic chip carrier packages. It is guaranteed for operation from 0°C to 70°C. The dual-in-line package is designed for insertion in mounting-hole rows on 7,62-mm (300-mil) centers.

operation

address (A0 through A7)

Fourteen address bits are required to decode 1 of 16,384 storage locations. Eight row-address bits are set up on pins A0 through A7 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the six column-address bits are set up on pins A1 through A6 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable (W) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$, data out will remain in the high-impedance state allowing a write cycle with $\overline{G}$ grounded.

data in (DQ1 through DQ4)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latches. These latches can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal. In a delayed or read-modify-write cycle, $\overline{G}$ must be high to bring the output buffers to high impedance prior to impressing data on the I/O lines.

data out (DQ1 through DQ4)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan out of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output goes active after the access time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ and $t_{a(G)}$ are satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ and $\overline{G}$ are low. $\overline{CAS}$ or $\overline{G}$ going high returns it to a high-impedance state. In an early write cycle, the output is always in the high-impedance state. In a delayed-write or read-modify-write cycle, the output must be put in the high-impedance state prior to applying data to the DQ input. This is accomplished by bringing $\overline{G}$ high prior to applying data, thus satisfying t_{GHD}.

output enable ($\overline{G}$)

The $\overline{G}$ input controls the impedance of the output buffers. When $\overline{G}$ is high, the buffers will remain in the high-impedance state. Bringing $\overline{G}$ low during a normal cycle will activate the output buffers putting them

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in the low-impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CAS}$ to be brought low for the output buffers to go into the low-impedance state. Once in the low-impedance state, they will remain in the low-impedance state until $\overline{G}$ or $\overline{CAS}$ is brought high.

refresh

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffer is in the high-impedance state unless $\overline{CAS}$ is applied, the $\overline{RAS}$-only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses (A0 through A7) with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power.

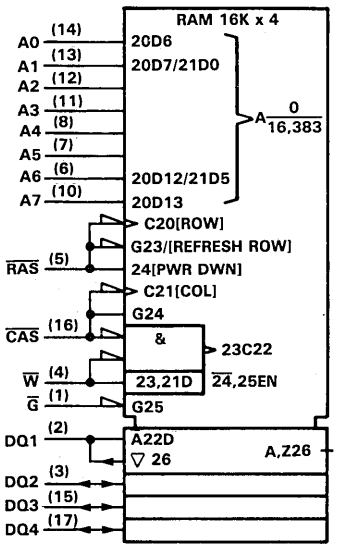
page mode

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the chip. Thus, the time required to setup and strobe sequential row addresses for the same page is eliminated. To extend beyond the 64 column locations on a single RAM, the row address and $\overline{RAS}$ are applied to multiple 16K × 4 RAMs. $\overline{CAS}$ is then decoded to select the proper RAM.

power up

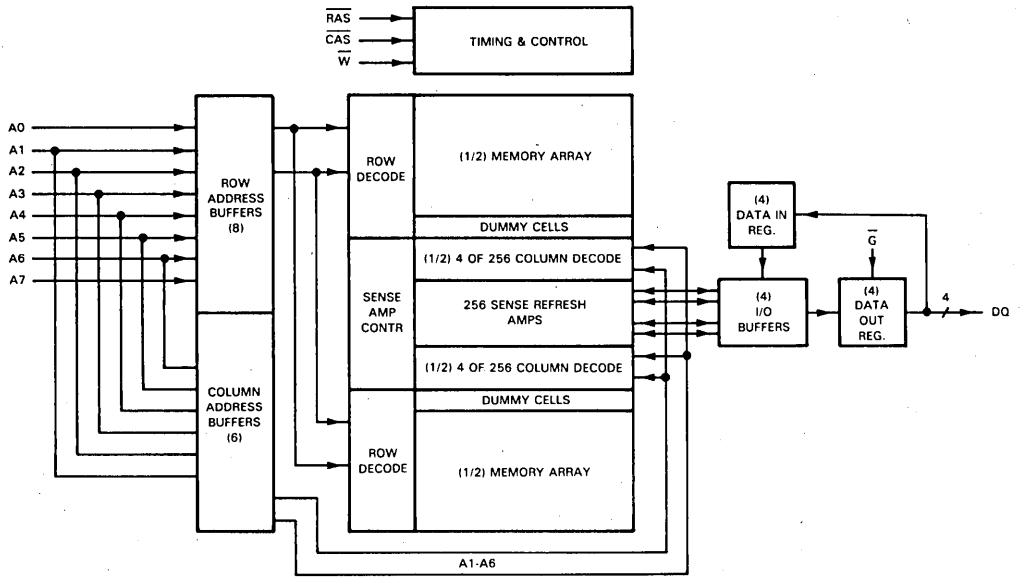
After power up, the power supply must remain at its steady-state value for 1 ms. In addition, the $\overline{RAS}$ input must remain high for 100 μs immediately prior to initialization. Initialization consists of performing eight $\overline{RAS}$ cycles before proper device operation is achieved.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std.91-1984 and IEC Publication 617-12.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range for any pin except V_{DD} and data out (see Note 1) . . . . . −1.5 V to 10 V
Voltage range for V_{DD} supply and data out with respect to V_{SS} . . . . . −1 V to 6 V
Short circuit output current . . . . . 50 mA
Power dissipation . . . . . 1 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values in this data sheet are with respect to V_{SS}.
2. Additional information concerning the handling of ESD sensitive devices is available in a document entitled *"Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies"* in Section 12.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		4.5	5	5.5	V
V_{SS}	Supply voltage			0		V
V_{IH}	High-level input voltage	V_{DD} = 4.5 V	2.4		4.8	V
		V_{DD} = 5.5 V	2.4		5.8	
V_{IL}	Low-level input voltage (see Notes 3 and 4)		−0.6	0	0.8	V
T_A	Operating free-air temperature		0		70	°C

NOTES: 3. The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

4. Due to input protection circuitry, the applied voltage may begin to clamp at −0.6 V. Test conditions must comprehend this occurrence. See application report entitled "TMS4164A and TMS4416 Input Protection Diode" on page 9-5.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TMS4416-12			UNIT
			MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −2 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 5.8 V, V_{DD} = 5V, All other pins = 0 V			±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10	μA
I_{DD1}	Average operating current during read or write cycle	t_c = minimum cycle, All outputs open			54	mA
I_{DD2}	Standby current (see Note 5)	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, All outputs open		3.5	5	mA
I_{DD3}	Average refresh current	t_c = minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high, All outputs open			46	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling, All outputs open			46	mA

† All typical values are at T_A = 25°C and nominal supply voltages.

NOTE 5: $V_{IL} \geq -0.6V$ on all inputs. See application report entitled "TMS4164A and TMS4416 Input Protection Diode" on page 9-5.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TMS4416-15			TMS4416-20			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −2 mA	2.4			2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 5.8 V, V_{DD} = 5V, All other pins = 0 V			±10			±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10			±10	μA
I_{DD1}	Average operating current during read or write cycle	t_c = minimum cycle, All outputs open		40	48		35	42	mA
I_{DD2}	Standby current (see Note 5)	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, All outputs open		3.5	5		3.5	5	mA
I_{DD3}	Average refresh current	t_c = minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high, All outputs open		25	40		21	34	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling, All outputs open		25	40		21	34	mA

† All typical values are at T_A = 25°C and nominal supply voltages.
NOTE 5: $V_{IL} \geq -0.6V$ on all inputs. See application report entitled "TMS4164A and TMS4416 Input Protection Diode" on page 9-5.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

PARAMETER		TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs	5	7	pF
$C_{i(RC)}$	Input capacitance, strobe inputs	8	10	pF
$C_{i(W)}$	Input capacitance, write-enable input	8	10	pF
$C_{i/o}$	Input/output capacitance, data ports	8	10	pF

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switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TMS4416-12		UNIT
				MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		70	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, C_L = 100 pF, Load = 2 Series, 74 TTL gates	t_{RAC}		120	ns
$t_{a(G)}$	Access time after $\overline{G}$ low	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OEA}		30	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	30	ns
$t_{dis(G)}$	Output disable time after $\overline{G}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OEZ}	0	30	ns

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TMS4416-15		TMS4416-20		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		80		120	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, C_L = 100 pF, Load = 2 Series, 74 TTL gates	t_{RAC}		150		200	ns
$t_{a(G)}$	Access time after $\overline{G}$ low	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OEA}		40		50	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	30	0	40	ns
$t_{dis(G)}$	Output disable time after $\overline{G}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OEZ}	0	30	0	40	ns

timing requirements over recommended supply voltage range and operating free-air temperature range

		ALT. SYMBOL	TMS4416-12 MIN	TMS4416-12 MAX	UNIT
$t_{c(P)}$	Page-mode cycle time	t_{PC}	120		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	230		ns
$t_{c(W)}$	Write cycle time	t_{WC}	230		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	315		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (precharge time)‡	t_{CP}	40		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low§	t_{CAS}	70	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge time)	t_{RP}	80		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low¶	t_{RAS}	120	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	30		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	50		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	50		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	35		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	15		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	85		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	40		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	90		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	30		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	10		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	40		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	90		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	120		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	70		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write-cycle only)#	t_{CWD}	120		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	20	50	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write-cycle only)#	t_{RWD}	170		ns
t_{WLCL}	Delay time, $\overline{W}$ low to $\overline{CAS}$ low (early write cycle)	t_{WCS}	−5		ns
t_{GHD}	Delay time, $\overline{G}$ high before data applied at DQ	t_{OED}	30		ns
t_{rf}	Refresh time interval	t_{REF}		4	ms

† All cycle times assume $t_t = 5$ ns.
‡ Page mode only.
§ In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time $t_{w(CL)}$.
¶ In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time $t_{w(RL)}$.
# Necessary to insure $\overline{G}$ has disabled the output buffers prior to applying data to the device.

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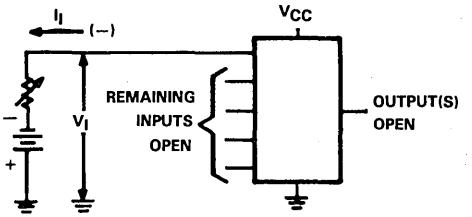
timing requirements over recommended supply voltage range and operating free-air temperature range

		ALT. SYMBOL	TMS4416-15 MIN	TMS4416-15 MAX	TMS4416-20 MIN	TMS4416-20 MAX	UNIT
$t_{c(P)}$	Page-mode cycle time	t_{PC}	140		210		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	260		330		ns
$t_{c(W)}$	Write cycle time	t_{WC}	260		330		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	365		445		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (precharge time)‡	t_{CP}	50		80		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low§	t_{CAS}	80	10,000	120	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge time)	t_{RP}	100		120		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low¶	t_{RAS}	150	10,000	200	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	40		50		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	50	3	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	60		80		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	60		80		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	40		50		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	20		25		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	110		130		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	60		80		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	130		160		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	40		50		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	10		10		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	60		80		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	130		160		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	150		200		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	80		120		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write-cycle only)#	t_{CWD}	120		150		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	20	70	25	80	ns
t_{RLWL}	Delay time, RAS low to $\overline{W}$ low (read-modify-write-cycle only)#	t_{RWD}	190		230		ns
t_{WLCL}	Delay time, $\overline{W}$ low to $\overline{CAS}$ low (early write cycle)	t_{WCS}	−5		−5		ns
t_{GHD}	Delay time, $\overline{G}$ high before data applied at DQ	t_{OED}	30		40		ns
t_{rf}	Refresh time interval	t_{REF}		4		4	ms

† All cycle times assume $t_t = 5$ ns.
‡ Page mode only.
§ In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time $t_{w(CL)}$.
¶ In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time $t_{w(RL)}$.
# Necessary to insure $\overline{G}$ has disabled the output buffers prior to applying data to the device.

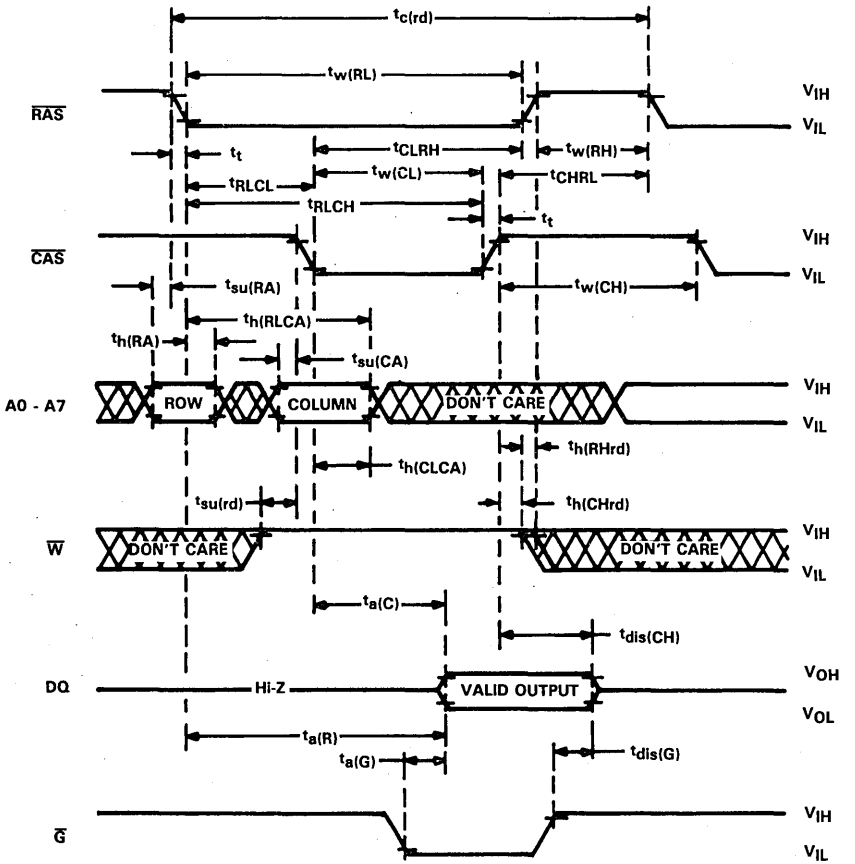
PARAMETER MEASUREMENT INFORMATION



NOTE 6: Each input is tested separately.

FIGURE 1. INPUT CLAMP VOLTAGE TEST CIRCUIT

read cycle timing



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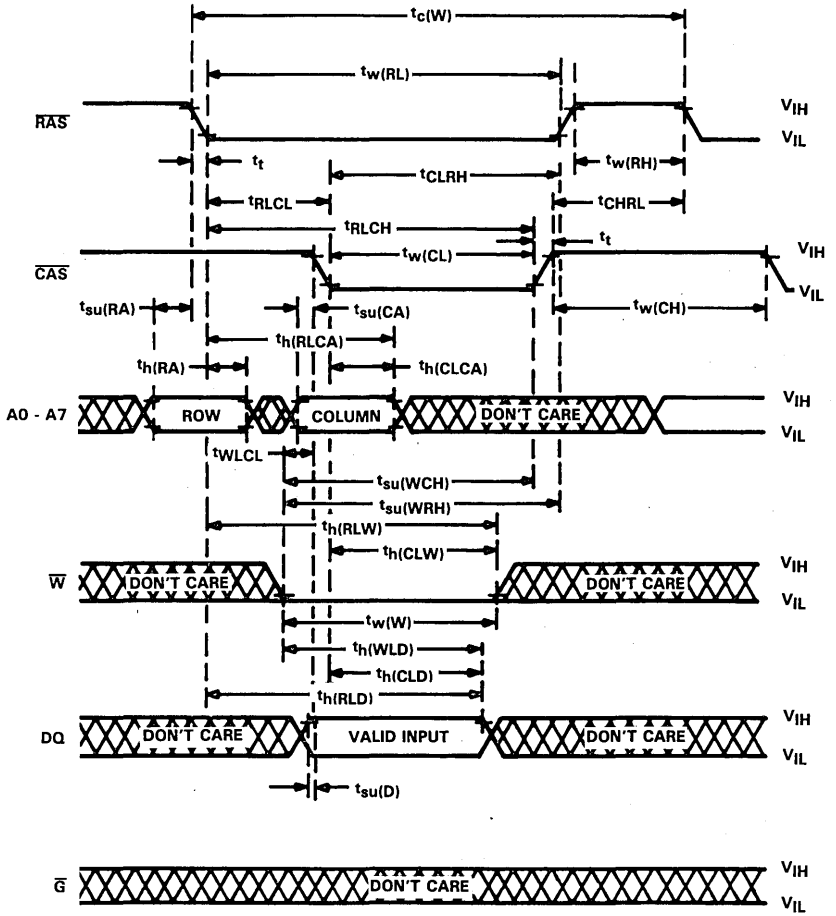
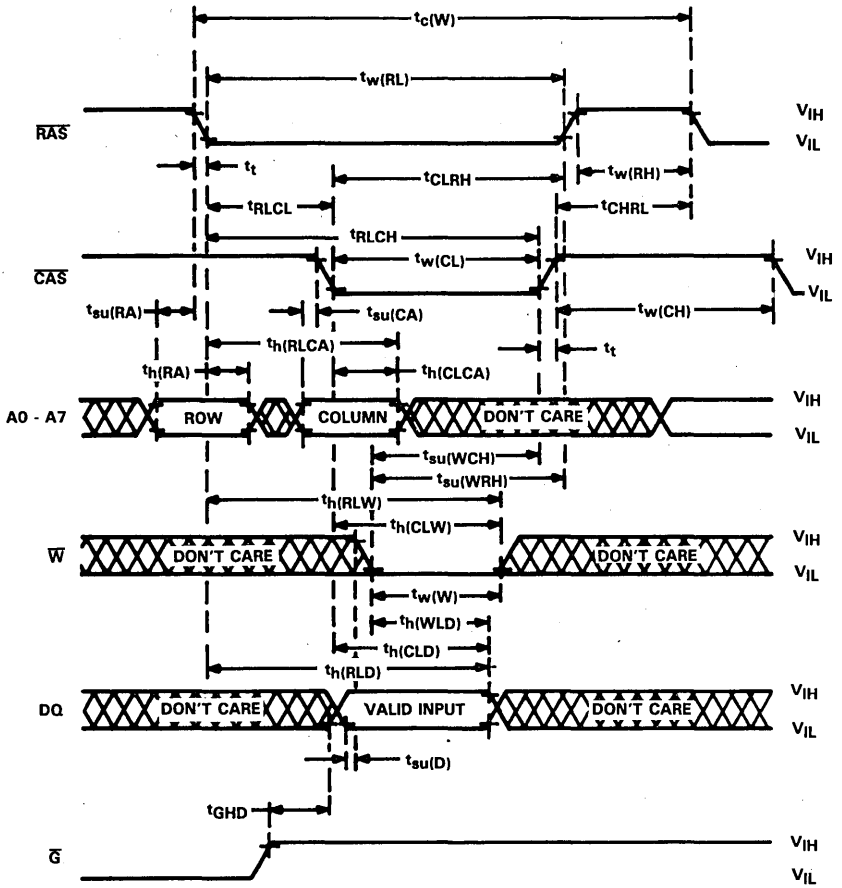
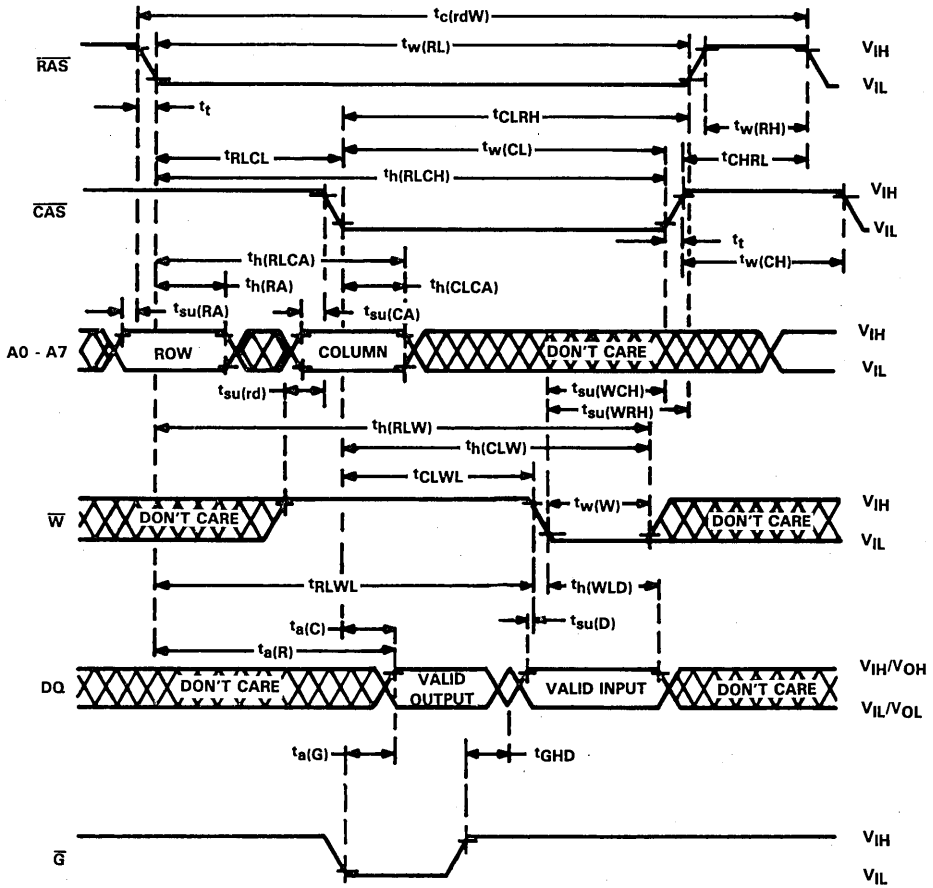
early write cycle timing



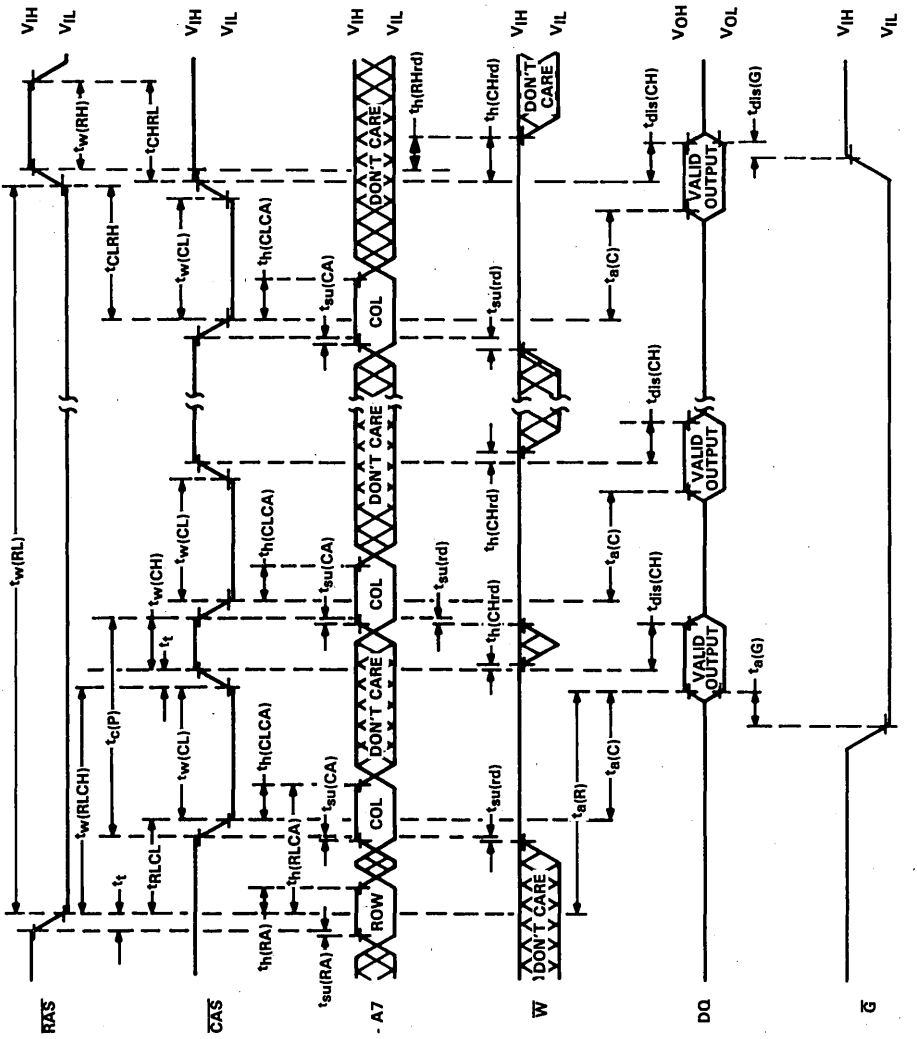
write cycle timing



read-write/read-modify-write cycle timing

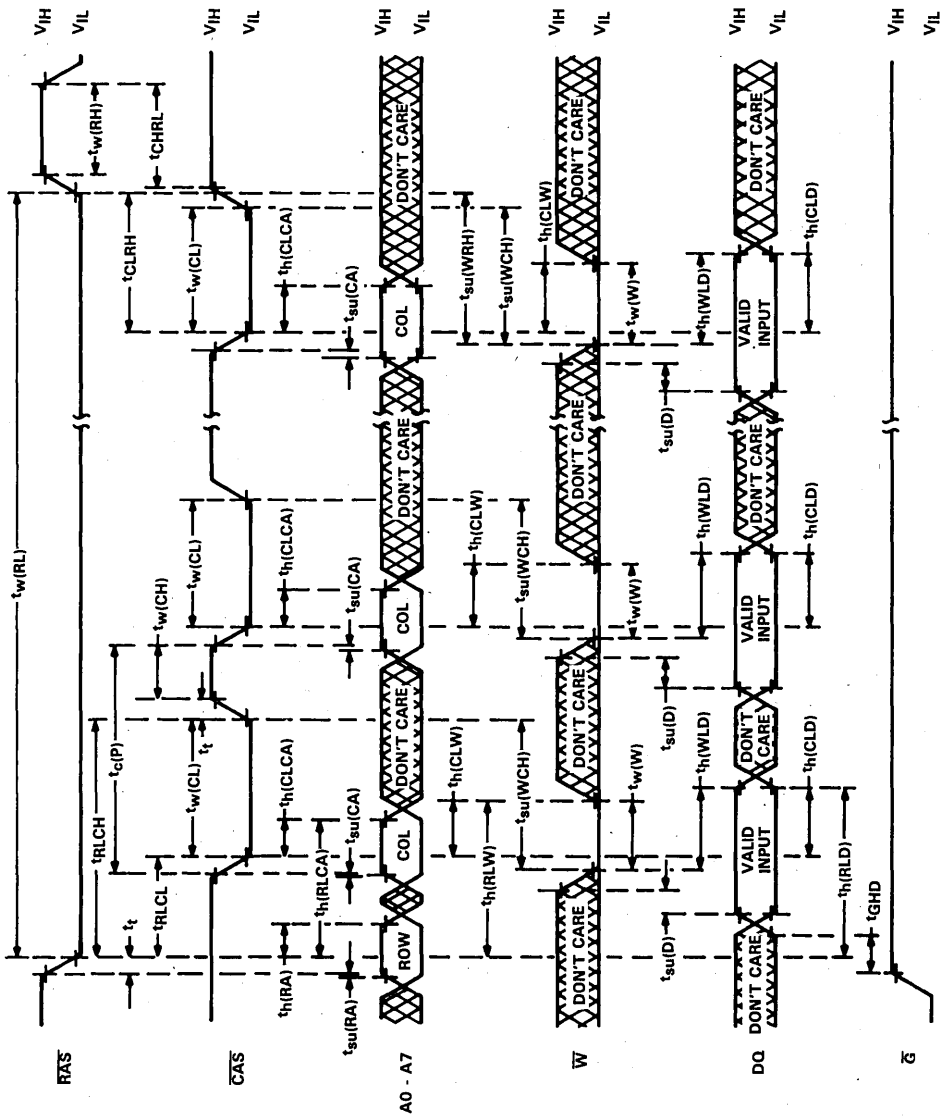


page-mode read cycle timing



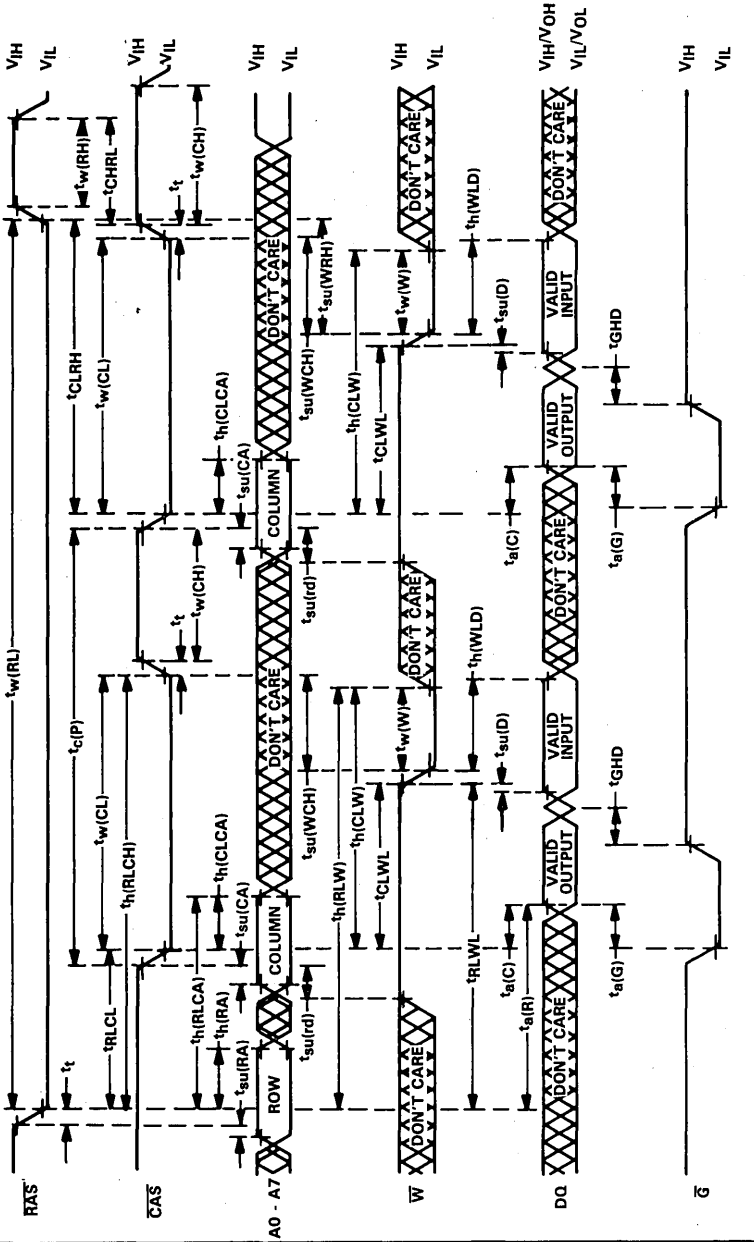
NOTE 7: A write cycle or read-modify-write cycle can be intermixed with read cycles as long as the write and read-modify-write timing specifications are not violated.

page-mode write cycle timing



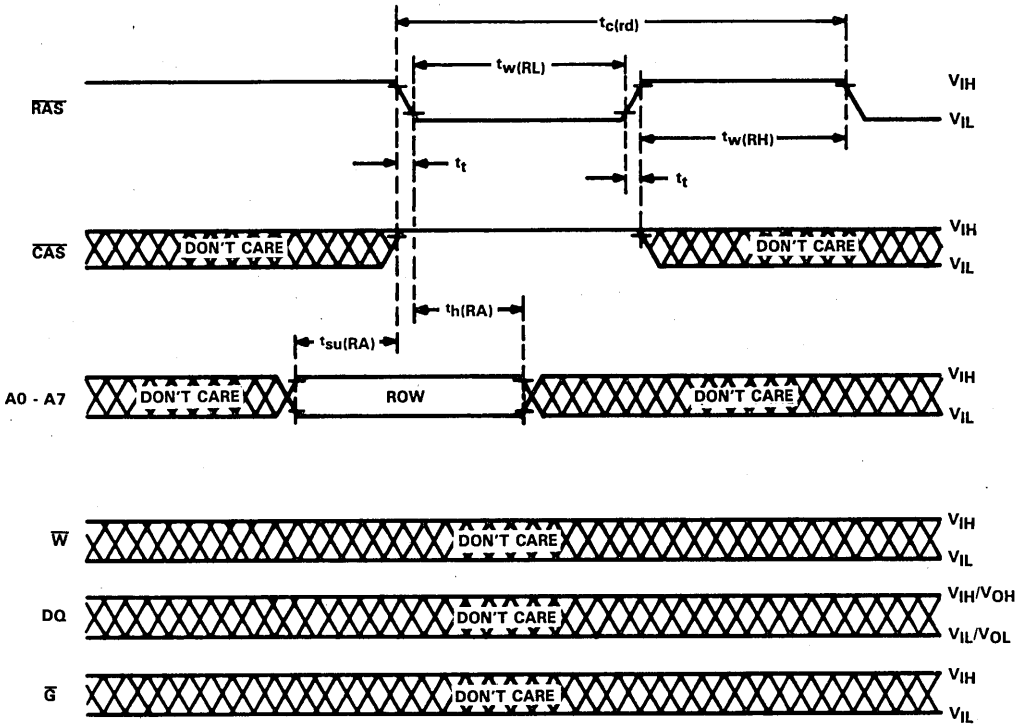
NOTE 8: A read cycle or a read-modify-write cycle can be intermixed with write cycles as long as read and read-modify-write timing specifications are not violated.

page-mode read-modify-write timing

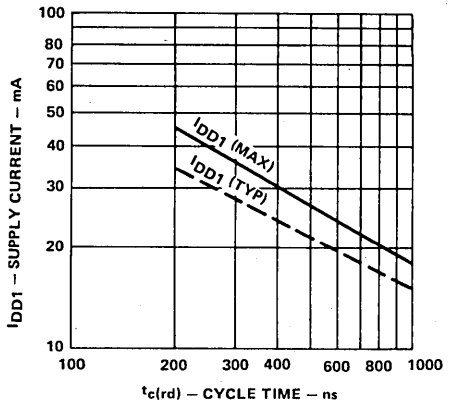


NOTE 9: A read cycle or a write cycle can be intermixed with read-modify-write cycles as long as read and write timing specifications are not violated.

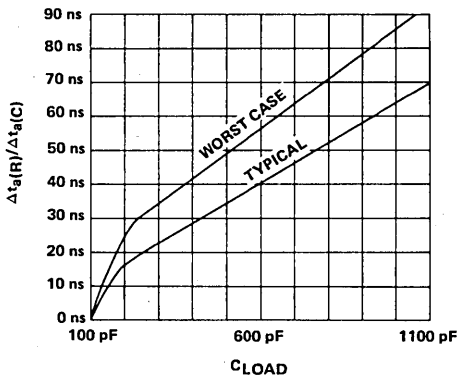
RAS-only refresh timing



I_{DD1} VS CYCLE TIME



ACCESS TIME DERATING CURVE



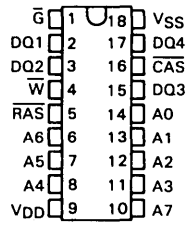
NOVEMBER 1983—REVISED NOVEMBER 1985

- 65,536 X 4 Organization
- Single 5-V Supply (10% Tolerance)
- JEDEC Standardized Pinout
- Pinout Identical to TMS4416 (16K X 4 Dynamic RAM)
- Performance Ranges:

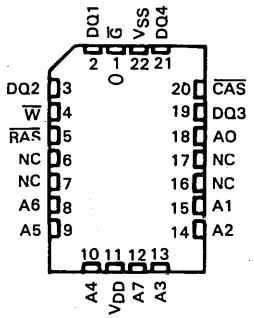
	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	READ-MODIFY-WRITE CYCLE (MIN)
TMS4464-12	120 ns	60 ns	230 ns	310 ns
TMS4464-15	150 ns	75 ns	260 ns	345 ns
TMS4464-20	200 ns	100 ns	330 ns	435 ns

- Long Refresh Period . . . 4 ms (Max)
- Low Refresh Overhead Time . . . As Low As 1.3% of Total Refresh Period
- On-Chip Substrate Bias Generator
- All Inputs, Outputs, and Clocks Fully TTL Compatible
- 3-State Unlatched Output
- Early Write or $\overline{G}$ to Control Output Buffer Impedance
- Page-Mode Operation for Faster Access
- Power Dissipation As Low As:
  - Operating . . . 275 mW (Typ)
  - Standby . . . 12.5 mW (Typ)
- $\overline{RAS}$-Only Refresh Mode
- $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Mode

N PACKAGE
(TOP VIEW)



FM PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A7	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1-DQ4	Data In/Data Out
$\overline{G}$	Output Enable
NC	No Connection
$\overline{RAS}$	Row-Address Strobe
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The TMS4464 is a high-speed, 262,144-bit dynamic random-access memory, organized as 65,536 words of four bits each. It employs state-of-the-art SMOS (scaled MOS) N-channel double-level polysilicon/polycide gate technology for very high performance combined with low cost and improved reliability.

This device features maximum $\overline{RAS}$ access times of 120 ns, 150 ns, or 200 ns. Typical power dissipation is as low as 275 mW operating and 12.5 mW standby.

New SMOS technology permits operation from a single 5-V supply, reducing system power supply and decoupling requirements, and easing board layout. I_{DD} peaks are 125 mA typical, and a −1-V input voltage undershoot can be tolerated, minimizing system noise considerations.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address and data-in lines are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

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The TMS4464 is offered in 18-pin plastic dual-in-line and 22-lead plastic chip carrier packages. It is guaranteed for operation from 0°C to 70°C. The dual-in-line package is designed for insertion in mounting-hole rows on 7,62-mm (300-mil) centers.

operation

address (A0 through A7)

Sixteen address bits are required to decode 1 of 65,536 storage locations. Eight row-address bits are set up on pins A0 through A7 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the eight column-address bits are set up on pins A0 through A7 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$, data out will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data in (DQ1-DQ4)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latches. These latches can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal. In a delayed or read-modify-write cycle, $\overline{G}$ must be high to bring the output buffers to high impedance prior to impressing data on the I/O lines.

data out (DQ1-DQ4)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan out of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output goes active after the access time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ and $t_{a(G)}$ are satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ and $\overline{G}$ are low. $\overline{CAS}$ or $\overline{G}$ going high returns it to a high-impedance state. In a delayed-write or read-modify-write cycle, the output must be put in the high-impedance state prior to applying data to the DQ input. This is accomplished by bringing $\overline{G}$ high prior to applying data, thus satisfying t_{GHD}.

output enable ($\overline{G}$)

The $\overline{G}$ input controls the impedance of the output buffers. When $\overline{G}$ is high, the buffers will remain in the high-impedance state. Bringing $\overline{G}$ low during a normal cycle will activate the output buffers putting them in the low-impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CAS}$ to be brought low for the output buffers to go into the low-impedance state. Once in the low-impedance state they will remain in the low-impedance state until $\overline{G}$ or $\overline{CAS}$ is brought high.

refresh

A refresh operation must be performed at least once every four milliseconds to retain data. This can be achieved by strobing each of the 256 rows (A0-A7). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, thus conserving power as the output buffer remains in the high-impedance state.

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$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh

The $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh is utilized by bringing $\overline{\text{CAS}}$ low earlier than $\overline{\text{RAS}}$ (see parameter t_{CLRL}) and and holding it low after $\overline{\text{RAS}}$ falls (see parameter t_{RLCHR}). For successive $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycles, $\overline{\text{CAS}}$ can remain low while cycling $\overline{\text{RAS}}$. The external address is ignored and the refresh address is generated internally.

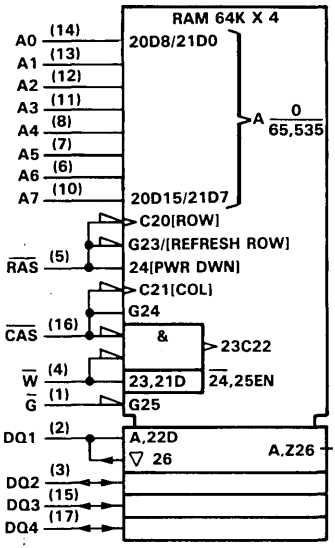
page mode

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing random column addresses onto the chip. Thus, the time required to setup and strobe sequential row addresses for the same page is eliminated. The maximum number of columns that can be addressed is determined by $t_{W(RL)}$, the maximum $\overline{\text{RAS}}$ low pulse duration.

power up

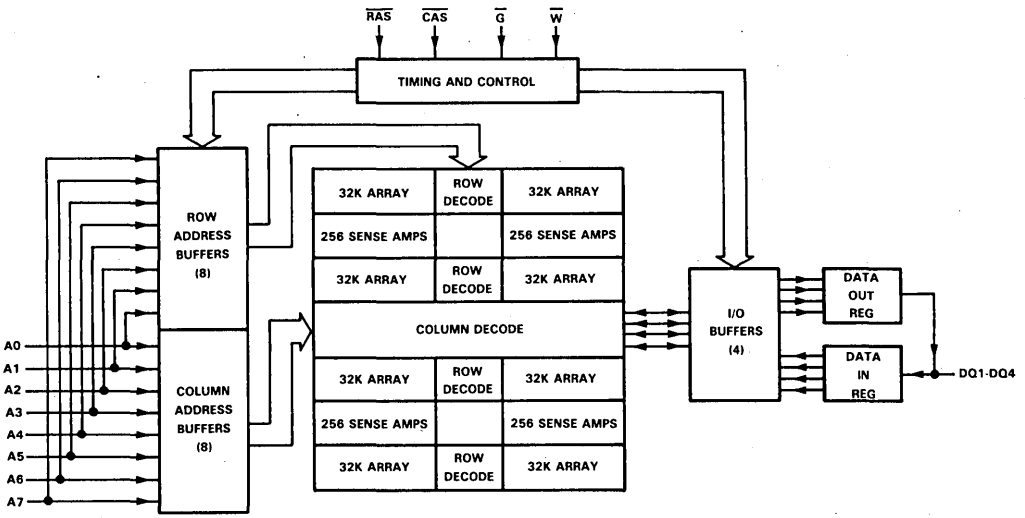
To achieve proper device operation, an initial pause of 200 μs is required after power up followed by a minimum of eight initialization cycles.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the dual-in-line package.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage on any pin including V_{DD} supply (see Note 1) . . . . . −1 V to 7 V
Short circuit output current . . . . . 50 mA
Power dissipation . . . . . 1 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		$V_{DD}+1$	V
V_{IL}	Low-level input voltage (see Note 2)	−1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as maximum, is used in this data sheet for logic voltage levels only.

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electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TMS4464-12			UNIT
			MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 6.5 V, V_{DD} = 5 V, All other pins = 0 V to 6.5 V			±10	μA
I_O	Output current (leakage)	V_O = 0 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high, All outputs open			±10	μA
I_{DD1}	Average operating current during read or write cycle	t_c = minimum cycle, All outputs open		65	80	mA
I_{DD2}	Standby current	After 1 memory cycle, DQ1-DQ4 held at > 0 V, $\overline{RAS}$ and $\overline{CAS}$ high, All outputs open		2.5	5	mA
I_{DD3}	Average refresh current	t_c = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ high, All outputs open		50	60	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling, All outputs open		45	55	mA

PARAMETER		TEST CONDITIONS	TMS4464-15			TMS4464-20			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4			2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 6.5 V, V_{DD} = 5 V, All other pins = 0 V to 6.5 V			±10			±10	μA
I_O	Output current (leakage)	V_O = 0 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high All outputs open			±10			±10	μA
I_{DD1}	Average operating current during read or write cycle	t_c = minimum cycle All outputs open		55	70		50	60	mA
I_{DD2}	Standby current	After 1 memory cycle, DQ1-DQ4 held at > 0 V, $\overline{RAS}$ and $\overline{CAS}$ high, All outputs open		2.5	5		2.5	5	mA
I_{DD3}	Average refresh current	t_c = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ high, All outputs open		45	55		40	50	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling, All outputs open		40	50		30	40	mA

†All typical values are at T_A = 25°C and nominal supply voltages.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

PARAMETER		TMS4464		UNIT
		TYP†	MAX	
$C_{i(A)}$	Input capacitance, address inputs	4	7	pF
$C_{i(RC)}$	Input capacitance strobe inputs	8	10	pF
$C_{i(W)}$	Input capacitance, write enable input	8	10	pF
$C_{i/o}$	Output capacitance	8	10	pF

† All typical values are at T_A = 25 °C and nominal supply voltages.

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TMS4464-12		UNIT
				MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	$t_{RLCL} \geq$ MAX, C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		60	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{RAC}		120	ns
$t_{a(G)}$‡	Access time after $\overline{G}$ low	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{GAC}		35	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	30	ns
$t_{dis(G)}$	Output disable time after $\overline{G}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{GOFF}	0	30	ns

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TMS4464-15		TMS4464-20		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	$t_{RLCL} \geq$ MAX, C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		75		100	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{RAC}		150		200	ns
$t_{a(G)}$‡	Access time after $\overline{G}$ low	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{GAC}		45		55	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	30	0	35	ns
$t_{dis(G)}$	Output disable time after $\overline{G}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{GOFF}	0	30	0	35	ns

‡ $t_{a(C)}$ and $t_{a(R)}$ must be satisfied to guarantee $t_{a(G)}$.

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timing requirements over recommended supply voltage range and operating free-air temperature range

		ALT. SYMBOL	TMS4464-12		UNIT
			MIN	MAX	
$t_{c(P)}$	Page-mode cycle time	t_{PC}	120		ns
$t_{c(PM)}$	Page-mode cycle time (read-modify-write cycle)	t_{PCM}	200		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	230		ns
$t_{c(W)}$	Write cycle time	t_{WC}	230		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	310		ns
$t_{w(CH)P}$	Pulse duration, $\overline{CAS}$ high (page mode)	t_{CP}	50		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (non-page mode)	t_{CPN}	50		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low‡	t_{CAS}	60	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high	t_{RP}	100		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low§	t_{RAS}	120	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	40		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		ns
$t_{su(WCL)}$	Early-write command setup time before $\overline{CAS}$ low	t_{WCS}	0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	40		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	40		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	20		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	15		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	80		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	35		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	95		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	35		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	10		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	35		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	95		ns

Continued next page.

†All cycle times assume t_t = 5 ns.

‡In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$).

§In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).

timing requirements over recommended supply voltage range and operating free-air temperature range (continued)

		ALT. SYMBOL	TMS4464-12 MIN	TMS4464-12 MAX	UNIT
t_{RLCHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high¶	t_{CHR}	25		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	120		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		ns
t_{RHCL}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low¶	t_{RCP}	0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	60		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)#	t_{CWD}	95		ns
t_{CLRL}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low¶	t_{CSR}	25		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	25	60	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)#	t_{RWD}	155		ns
t_{GHD}	Delay time, $\overline{G}$ high before data applied at DQ	t_{GDD}	30		ns
t_{rf}	Refresh time interval	t_{REF}		4	ms

¶ $\overline{CAS}$-before-RAS refresh option only.
# $\overline{G}$ must disable the output buffers prior to applying data to the device.

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timing requirements over recommended supply voltage range and operating free-air temperature range (continued)

		ALT. SYMBOL	TMS4464-15		TMS4464-20		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(P)}$	Page-mode cycle time	t_{PC}	145		190		ns
$t_{c(PM)}$	Page-mode cycle time (read-modify-write cycle)	t_{PCM}	230		295		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	260		330		ns
$t_{c(W)}$	Write cycle time	t_{WC}	260		330		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	345		435		ns
$t_{w(CH)P}$	Pulse duration, $\overline{CAS}$ high (page mode)	t_{CP}	60		80		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (non-page mode)	t_{CPN}	60		80		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low‡	t_{CAS}	75	10,000	100	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high	t_{RP}	100		120		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low§	t_{RAS}	150	10,000	200	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	45		55		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	50	3	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		0		ns
$t_{su(WCL)}$	Early-write command setup time before $\overline{CAS}$ low	t_{WCS}	0		0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	45		60		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	45		60		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	25		45		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	15		20		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	100		145		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	45		55		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	120		155		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	45		55		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	10		15		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	45		55		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	120		155		ns

Continued next page.

†All cycle times assume t_t = 5 ns.

‡In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$).

§In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).

timing requirements over recommended supply voltage range and operating free-air temperature range (concluded)

		ALT. SYMBOL	TMS4464-15		TMS4464-20		UNIT
			MIN	MAX	MIN	MAX	
t_{RLCHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high¶	t_{CHR}	30		35		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	150		200		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
t_{RHCL}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low¶	t_{RCP}	0		0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	75		100		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)#	t_{CWD}	110		140		ns
t_{CLRL}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low¶	t_{CSR}	30		35		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	25	75	30	100	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)#	t_{RWD}	185		240		ns
t_{GHD}	Delay time, $\overline{G}$ high before data applied at DQ	t_{GDD}	30		35		ns
t_{rf}	Refresh time interval	t_{REF}		4		4	ms

¶$\overline{CAS}$-before-$\overline{RAS}$ refresh option only.
#$\overline{G}$ must disable the output buffers prior to applying data to the device.

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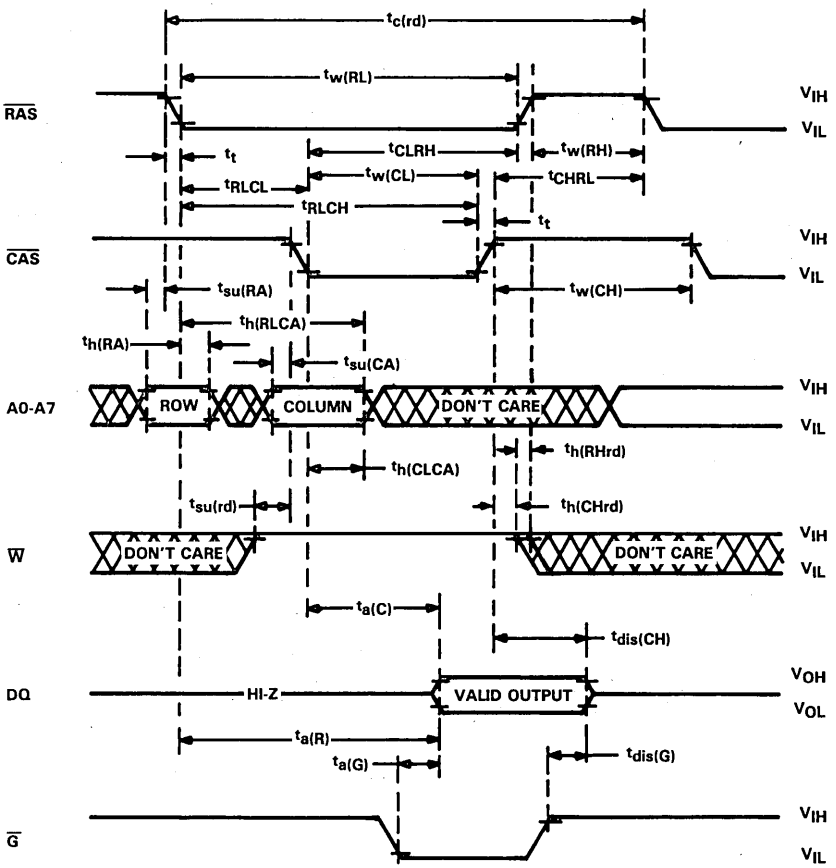
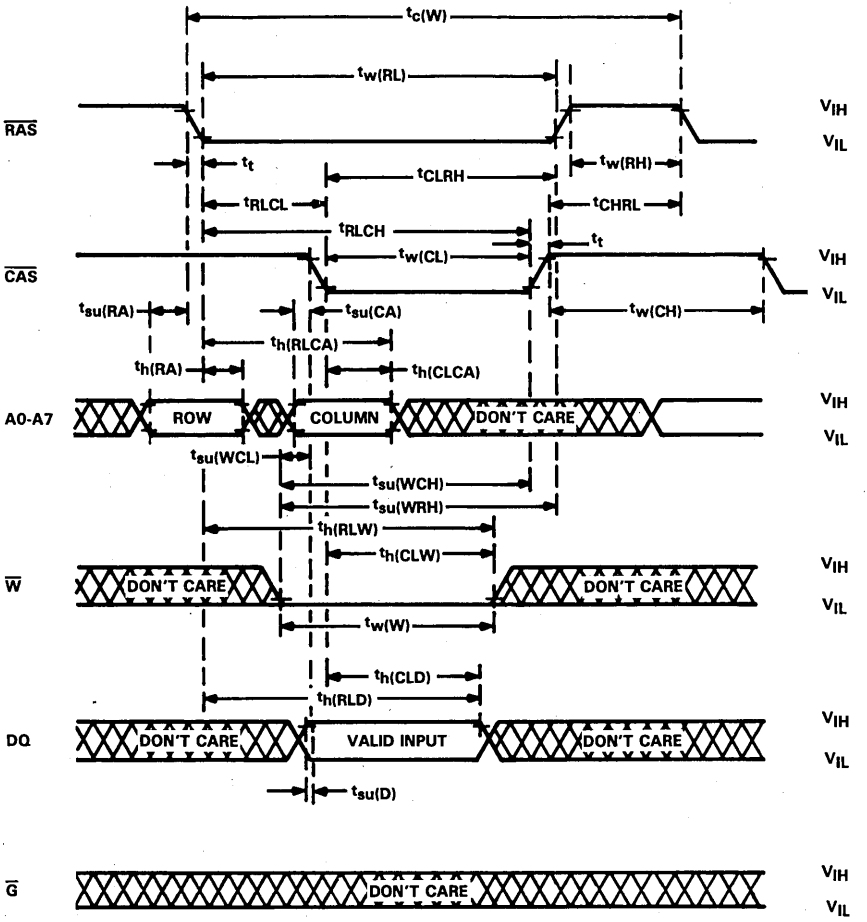
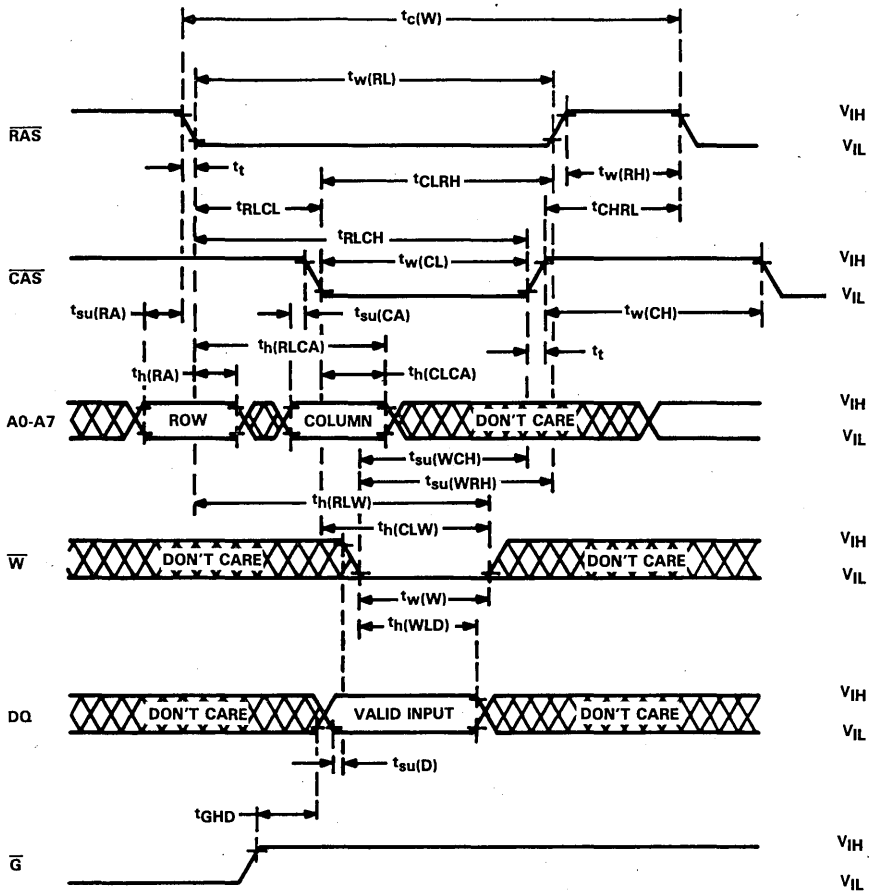
read cycle timing



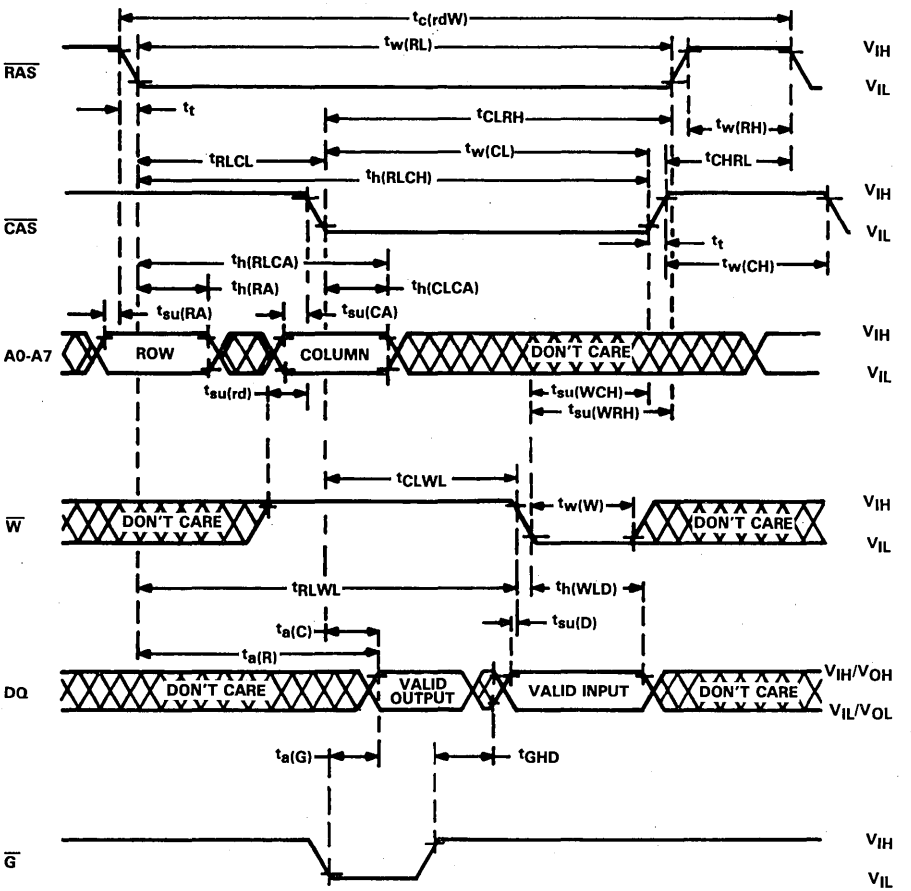
early write cycle timing



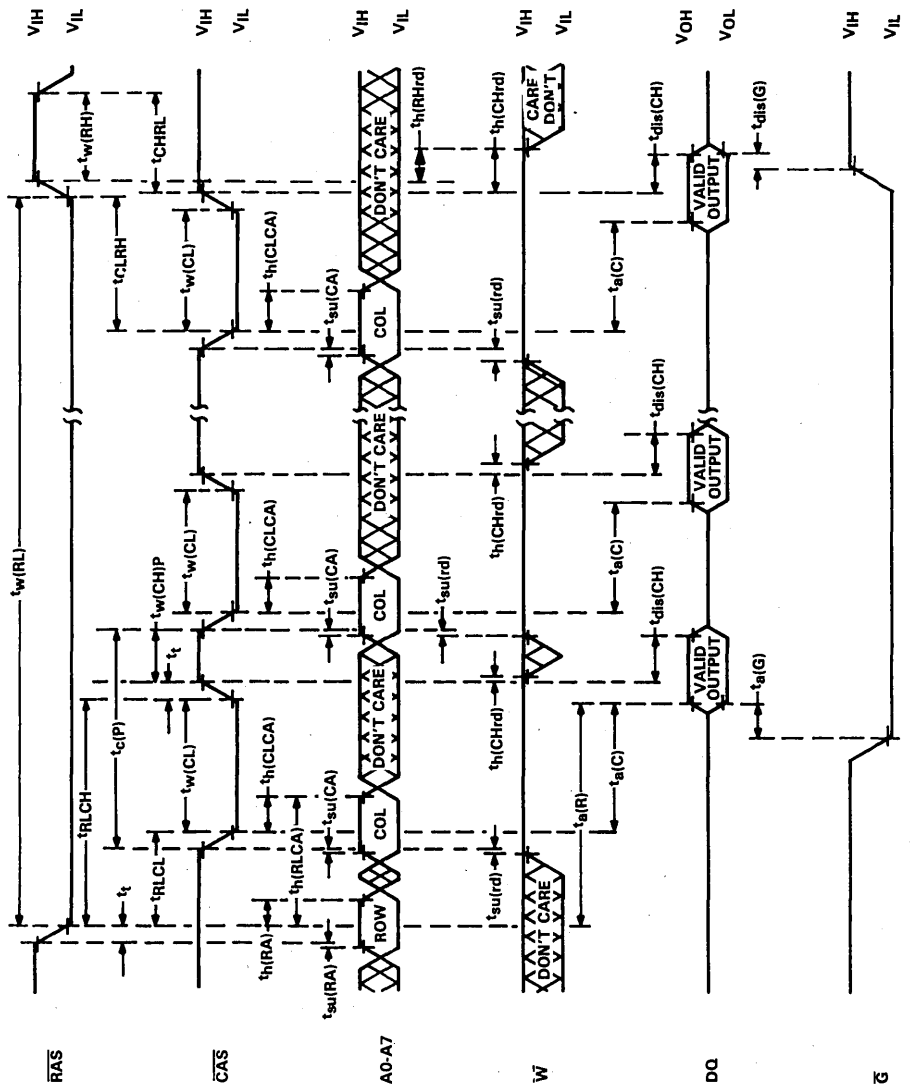
write cycle timing



read-write/read-modify-write cycle timing

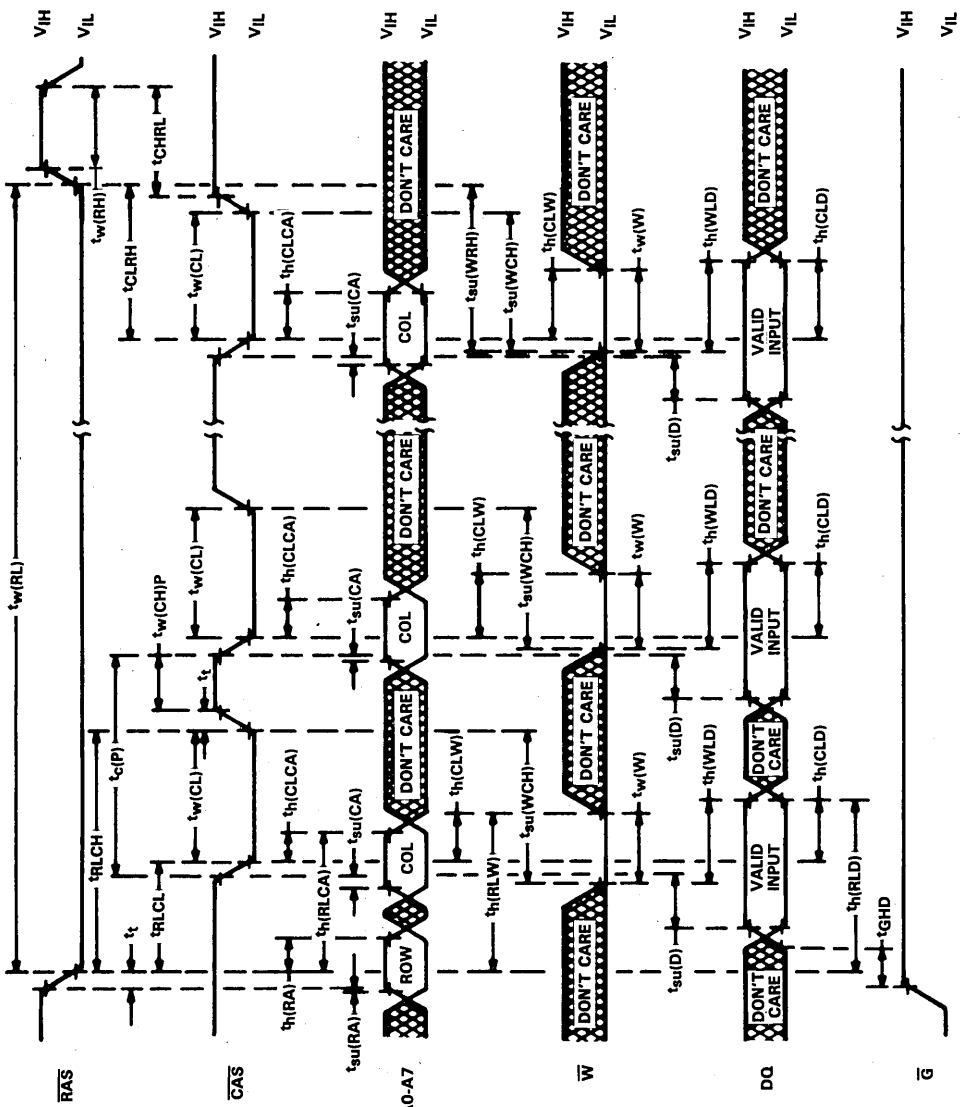


page-mode read cycle timing



NOTE 3: A write cycle or read-modify-write cycle can be intermixed with read cycles as long as the write and read-modify-write timing specifications are not violated.

page-mode write cycle timing



NOTE 4: A read cycle or a read-modify write cycle can be intermixed with write cycles as long as read and read-modify-write timing specifications are not violated.

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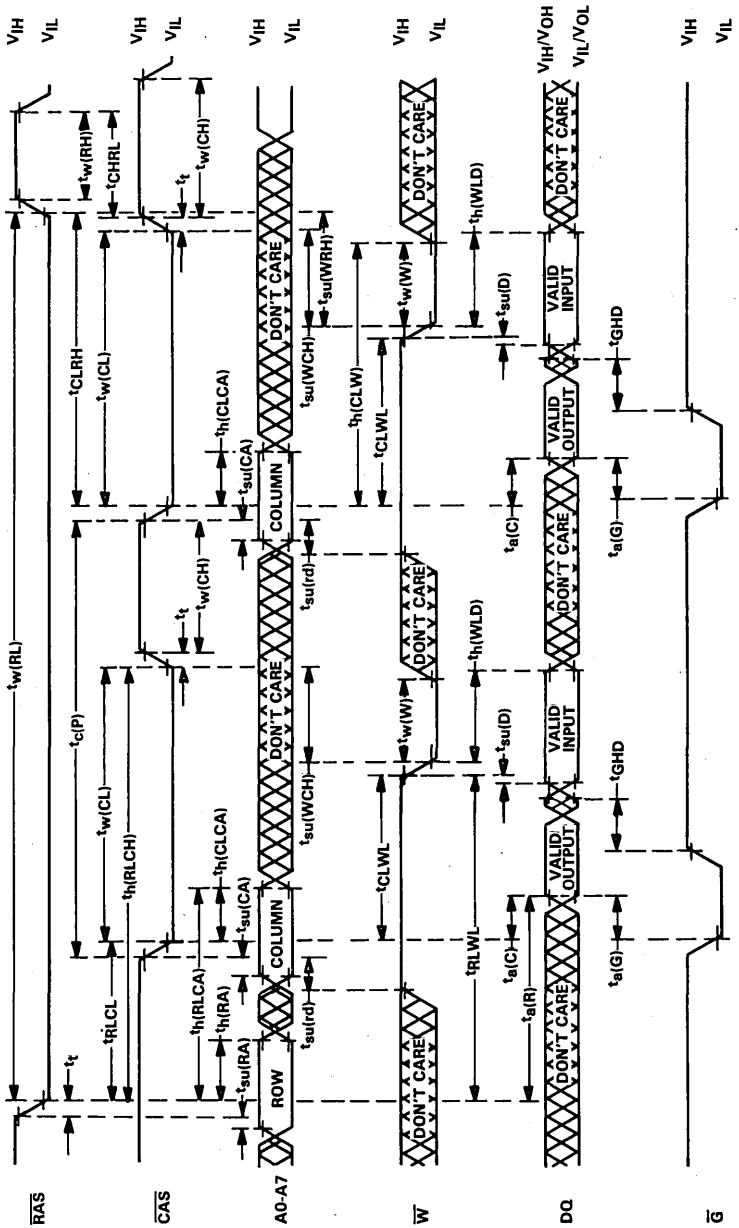
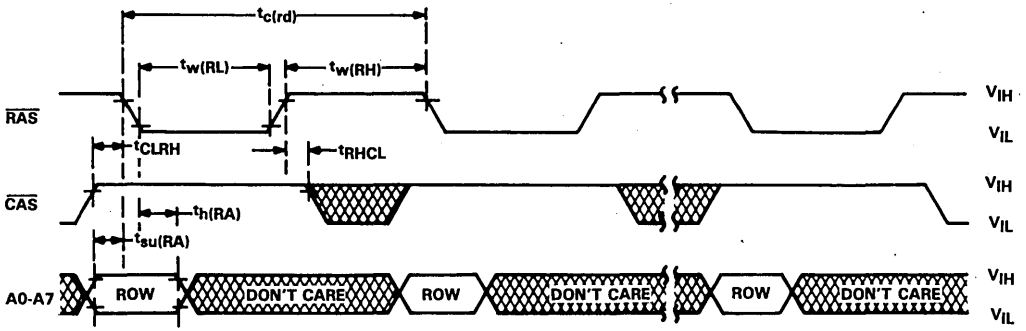
page-mode read-modify-write cycle timing

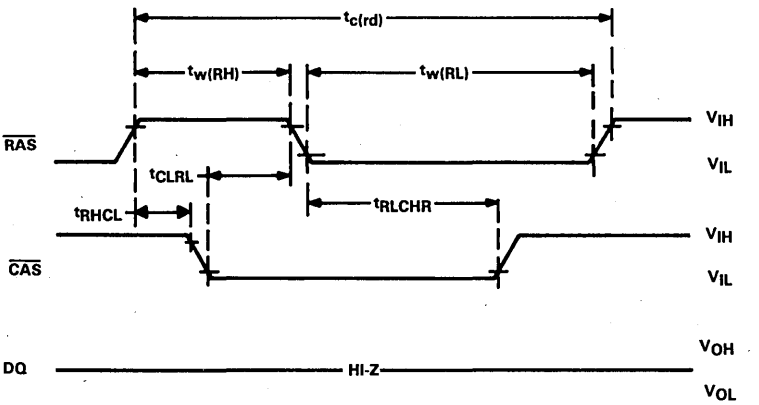


NOTE 5: A read cycle or a write cycle can be intermixed with read-modify-write cycles as long as read and write timing specifications are not violated.

$\overline{RAS}$-only refresh cycle timing



$\overline{CAS}$-before-$\overline{RAS}$ refresh cycle timing

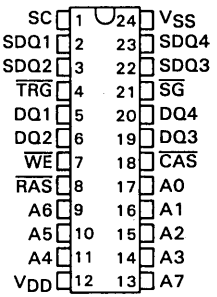


TMX4461
262,144-BIT MULTIPORT VIDEO RAM

NOVEMBER 1985

- 65,536 X 4 Organization
- Dual-Port Accessibility — Four I/O's for Sequential Access, Four I/O's for Random Access
- One Serial Data Register Built into Each Serial I/O for Sequential-Access Applications
- Fast Serial Ports . . . 30-MHz Shift Rate
- Mid-Scan Load — Serial Data Streams Uninterrupted by Register Reload
- $\overline{TRG}$ as Output Enable Allows Direct Connection of DQ and Address Lines to Simplify System Design
- Random-Access Port Is Compatible with the TMS4464, 64K X 4 DRAM
- 3-State Serial I/O's Allow Easy Multiplexing of Video Data Streams
- Maximum Access Time from $\overline{RAS}$ . . . 120 ns
- Minimum Cycle Time (Read or Write) . . . 200 ns
- Long Refresh Period . . . 4 ms
- Low Refresh Overhead Time . . . As Low As 1.3% of Total Refresh Period
- All Inputs, Outputs, Clocks Fully TTL Compatible
- Three-State Unlatched Random-Access Outputs
- Common Random-Access I/O Capability with "Early Write" Feature
- High-Speed Page-Mode Operation for Faster Access
- $\overline{CAS}$-Before-$\overline{RAS}$ Refresh and Hidden Refresh Modes

N PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A7	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1-DQ4	Random-Access Data In/ Data Out/Write-Mask Bit
$\overline{RAS}$	Row-Address Strobe
SC	Serial Data Clock
SDQ1-SDQ4	Serial Data In/Data Out
$\overline{SG}$	Serial Output Enable
$\overline{TRG}$	Transfer Register/ Q Output Enable
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{WE}$	Write-Mask Select/ Write Enable

- Low Power Dissipation —Operating . . . 250 mW (Typical, DRAM Port)
- 24-Pin, 400-Mil Dual-in-Line Package

description

The 256K Multiport Video RAM is a high-speed dual-ported 65,536 × 4 bit dynamic random-access memory with on-chip data registers. The random-access port makes the memory look like it is organized as 65,536 words of four bits each like the TMS4464. The sequential-access port is interfaced to four internal 256-bit dynamic data registers which make the memory look like it is organized as 256 four-bit words of up to 256 bits each which are accessed serially.

The 256K Multiport Video RAM employs state-of-the art double-level polysilicon/polycide gate technology for very high performance combined with low cost and improved reliability.

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TMX44C256, TMX44C257, TMX44C259
262,144-WORD BY 4-BIT DYNAMIC RANDOM-ACCESS MEMORIES

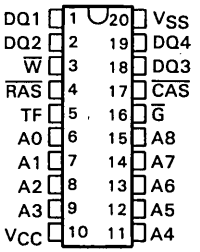
NOVEMBER 1985

- 262,144 X 4 Organization
- Single 5-V Supply (10% Tolerance)
- Pinout to Proposed JEDEC Standard
- Performance Ranges:

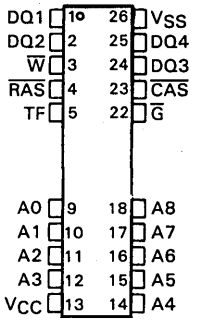
	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)
TMX44C25_-10	100 ns	50 ns	200 ns
TMX44C25_-12	120 ns	60 ns	230 ns
TMX44C25_-15	150 ns	75 ns	260 ns

- Multiple Operations Options:
  TMX44C256 — Page Mode/Enhanced Page Mode
  TMX44C257 — Static Column Mode
  TMX44C259 — 256 X 4 Bit Nibble Mode (Serial Mode)
- Long Refresh Period
  512-Cycle Refresh in 8 ms (Max)
- Three-State Unlatched Output
- Lower Power Dissipation
- New Scaled-CMOS Technology
- Low Standby Power with CMOS-Level Inputs
- High-Reliability Plastic 20-Pin 300-Mil-Wide DIP or Surface-Mount Packages

N PACKAGE
(TOP VIEW)



DJ PACKAGE†
(TOP VIEW)



†The packages shown here are for pinout reference only. The DJ package is actually 75% of the length of the N package.

description

The Megabit DRAM devices are high-speed, 1,048,576-bit dynamic random-access memories organized as 262,144 words of four bits each. They employ state-of-the-art TIC-MOS (Scaled CMOS) technology for high performance, reliability and lower power at a low cost.

PIN NOMENCLATURE	
A0-A8	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1-DQ4	Data In/Data Out
$\overline{G}$	Data Output Enable
$\overline{RAS}$	Row-Address Strobe
TF	Test Function
$\overline{W}$	Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

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TMX4C1024, TMX4C1025, TMX4C1026, TMX4C1027, TMX4C1029
1,048,576-BIT DYNAMIC RANDOM-ACCESS MEMORIES

NOVEMBER 1985

- 1,048,576 X 1 Organization
- Single 5-V Supply (10% Tolerance)
- Pinout to Proposed JEDEC Standard
- Performance Ranges:

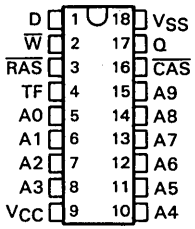
	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)
TMX4C102_-10	100 ns	50 ns	200 ns
TMX4C102_-12	120 ns	60 ns	230 ns
TMX4C102_-15	150 ns	75 ns	260 ns

- Multiple Operations Options:
  - TMX4C1024 — Page Mode/Enhanced Page Mode
  - TMX4C1025 — 4-Bit Nibble Mode
  - TMX4C1026 — 8-Bit Nibble (Byte)
  - TMX4C1027 — Static Column Mode
  - TMX4C1029 — 1024-Bit Nibble Mode (Serial Mode)
- Long Refresh Period 512-Cycle Refresh in 8 ms (Max)
- Three-State Unlatched Output
- Lower Power Dissipation
- New Scaled-CMOS Technology
- All Inputs and Clocks Are TTL Compatible
- Low Standby Power with CMOS-Level Inputs
- High-Reliability Plastic 18-Pin 300-Mil-Wide DIP or Surface-Mount Packages

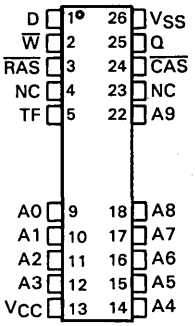
description

The Megabit DRAM devices are high-speed, 1,048,576-bit dynamic random-access memories organized as 1,048,576 words of one bit each. They employ state-of-the-art TIC-MOS (Scaled CMOS) technology for high performance, reliability and lower power at a low cost.

N PACKAGE
(TOP VIEW)



DJ PACKAGE†
(TOP VIEW)



†The packages shown here are for pinout reference only. The DJ package is actually 75% of the length of the N package.

PIN NOMENCLATURE	
A0-A9	Address Inputs
$\overline{CAS}$	Column-Address Strobe
D	Data In
NC	No Connection
Q	Data Out
$\overline{RAS}$	Row-Address Strobe
TF	Test Function
$\overline{W}$	Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

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ATTENTION

These devices contain circuits to protect the inputs and outputs against damage due to high static voltages or electrostatic fields; however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits.

Unused inputs must always be connected to an appropriate logic voltage level, preferably either supply voltage or ground.

Additional information concerning the handling of ESD sensitive devices is provided in Section 12 in a document entitled *"Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies."*

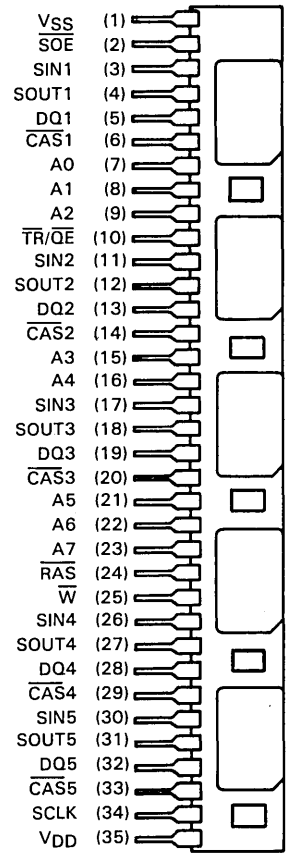
JULY 1984 — REVISED NOVEMBER 1985

- 65,536 X 5 Organization
- Single 5-V Supply (10% Tolerance)
- 35-Pin Single-in-Line Package (SIP)
- Utilizes Five Multiport Video RAMs in Plastic Chip Carriers
- Serial In/Serial Out Capability
- Dual Accessibility — One Port Sequential Access, One Port Random Access
- Five Serial Shift Registers for Sequential Access Applications, Each Comprised of Four Cascaded 64-Bit Segments
- Designed for both Video and Non-Video Applications
- Fast Serial Port . . . Can Be Configured for Video Data Rates in Excess of 150 MHz
- $\overline{TR}/\overline{QE}$ as Output Enable Allows Direct Connection of DQ and Address Lines to Simplify System Design
- Separate Serial In and Serial Out to Allow Simultaneous Shift In and Out
- Supported by TI's TMS34061 Video System Controller (VSC)
- $\overline{SOE}$ Simplifies Multiplexing of Serial Data Streams
- Long Refresh Period . . . 4 ms (256 Cycles)
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Outputs
- Performance Ranges:

	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)
TM4161EP5-15	150 ns	100 ns	240 ns
TM4161EP5-20	200 ns	135 ns	315 ns

- Separate $\overline{CAS}$ Control with Common Data-In and Data-Out Lines
- Low Power Dissipation:
  —Operating . . . 1250 mW (Typ)
  —Standby . . . 400 mW (Typ)
- Operating Free-Air Temperature . . . 0°C to 70°C

P SINGLE-IN-LINE PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A7	Address Inputs
$\overline{CAS}1$-$\overline{CAS}5$	Column-Address Strobes
DQ1-DQ5	Random-Access Data In/Data Out
$\overline{RAS}$	Row-Address Strobe
SCLK	Serial Data Clock
SIN1-SIN5	Serial Data In
$\overline{SOE}$	Serial Output Enable
SOUT1-SOUT5	Serial Data Out
$\overline{TR}/\overline{QE}$	Register Transfer/Q Output Enable
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The TM4161EP5 is a 320K dual-access dynamic random-access memory module organized as 65,536 × 5-bits in a 35-pin single-in-line package comprising five TMS4161FML, 65,536 × 1-bit Multiport Video RAMs in 22-lead plastic chip carriers mounted on top of a substrate together with five decoupling capacitors. The random-access port makes the module look like it is organized as 65,536 words of five bits each. The sequential-access port is interfaced to five internal 256-bit dynamic shift registers each organized as four cascaded 64-bit shift register segments which are accessed serially. One, two, three, or four 64-bit shift register segments can be sequentially read out after a transfer cycle depending on a two-bit code applied to the two most significant column address inputs.

The TM4161EP5 features full asynchronous dual access capability except when transferring data between the shift registers and the memory array.

Refresh period is extended to 4 milliseconds, and during this period each of the 256 rows must be strobed with $\overline{RAS}$ in order to retain data. $\overline{CAS}$ can remain high during the refresh sequence to conserve power. Note that the transfer of a row of data from the memory array to the shift registers also refreshes that row.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address lines and data in are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TM4161EP5 is guaranteed for operation from 0°C to 70°C.

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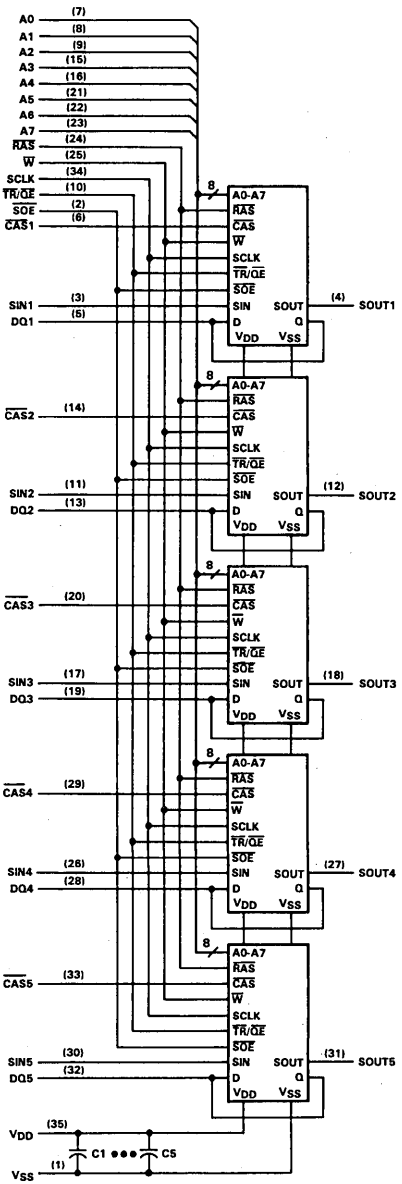
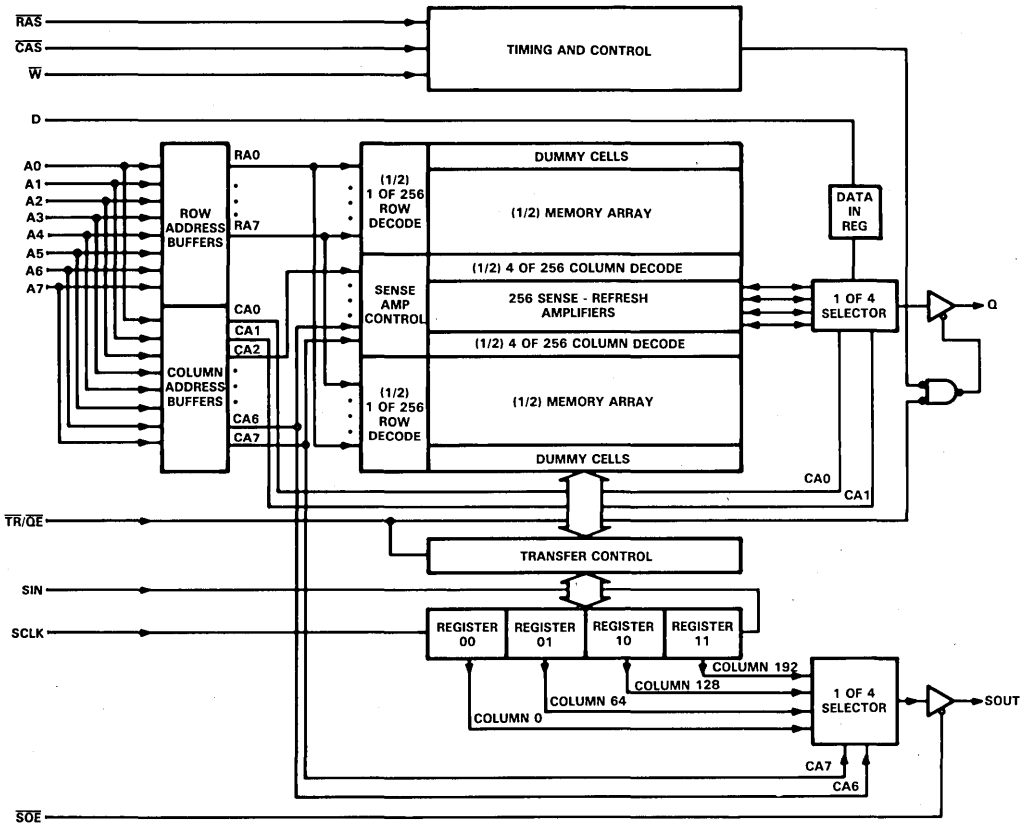
functional block diagram



TMS4161 functional block diagram



random-access address space to sequential address space mapping

The TM4161EP5 is designed with each row divided into four, 64-column sections which map directly onto the four segments of each shift register (see TMS4161 functional block diagram). The first column section to be shifted out is selected by the two most-significant column-address bits. If the two bits represent binary 00, then one to four register segments can be shifted out in order. If the two bits represent binary 01, then only 1 to 3 (the most significant) register segments can be shifted out in order. If the two bits represent 10, then one to two of the most-significant register segments can be shifted out in order. Finally, if the two bits represent 11 only the most-significant register segment can be shifted out. All register segments are shifted out with the least-significant bit (bit 0) first and the most-significant bit (bit 63) last. Note that if the two column-address bits equal 00 during the last register transfer cycle ($\overline{TR}/\overline{QE}$ at logic level "0" as $\overline{RAS}$ falls) a total of 256 bits can be sequentially read out of each serial output pin.

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random-access operation

$\overline{TR}/\overline{QE}$

The $\overline{TR}/\overline{QE}$ pin has two functions. First, it selects either register transfer or random-access operation as $\overline{RAS}$ falls, and second, during a random-access operation, it functions as an output enable after $\overline{CAS}$ falls.

To use the TM4161EP5 in the random-access mode, $\overline{TR}/\overline{QE}$ must be high as $\overline{RAS}$ falls. Holding $\overline{TR}/\overline{QE}$ high as $\overline{RAS}$ falls keeps the 256 elements of the shift registers disconnected from the corresponding 256 bit lines of the memory array. If data is to be shifted, the shift registers must be disconnected from the bit lines. Holding $\overline{TR}/\overline{QE}$ low as $\overline{RAS}$ falls enables the 256 switches that connect the shift registers to the bit lines and indicates that a transfer will occur between the shift registers and one of the memory rows.

During random-access operation, once $\overline{CAS}$ has been pulled low, $\overline{TR}/\overline{QE}$ controls when the data will appear at the Q output (if this is a read cycle). Whenever $\overline{TR}/\overline{QE}$ is held high during random-access operation, the Q output will be in the high-impedance state. This feature removes the possibility of an overlap between data on the address lines and data appearing on the Q output making it possible to connect the address lines to the Q and D lines (Use of this organization prohibits the use of the early write cycle.).

address (A0 through A7)

Sixteen address bits are required to decode 1 of 65,536 storage cell locations. Eight row-address bits are set up on pins A0 through A7 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the eight column-address bits are set up on pins A0 through A7 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and outputs buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data inputs are disabled when the read mode is selected. The common I/O feature of the TM4161EP5 dictates the use of early write cycles to prevent contention on DQ. When $\overline{W}$ goes low prior to $\overline{CAS}$, the data outputs will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data in (DQ1-DQ5)

Data is written during a write or read-modify-write cycle. The falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. This latch can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal.

data out (DQ1-DQ5)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan out of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state as long as $\overline{CAS}$ or $\overline{TR}/\overline{QE}$ is held high. Data will not appear on the output until after both $\overline{CAS}$ and $\overline{TR}/\overline{QE}$ have been brought low. In a read cycle, the guaranteed maximum output enable access time is valid only if t_{CQE} is greater than t_{CQE} MAX, and t_{RLCL} is greater than t_{RLCL} MAX. Likewise, $t_{a(C)}$ MAX is valid only if t_{RLCL} is greater than t_{RLCL} MAX. Once the output is valid, it will remain valid while $\overline{CAS}$ and $\overline{TR}/\overline{QE}$ are both low; $\overline{CAS}$ or $\overline{TR}/\overline{QE}$ going high will return the output to a high-impedance state. In an early write cycle, the output is always in a high-impedance state. In a register transfer cycle, the output will always be in a high-impedance state.

refresh

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffer is in high-impedance state unless $\overline{CAS}$ is applied, the $\overline{RAS}$-only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses (A0 through A7) with $\overline{RAS}$ causes all bits in each row to be refreshed. CAS can remain high (inactive) for this refresh sequence to conserve power.

page mode

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the module. Thus, the time required to setup and strobe sequential row addresses for the same page is eliminated. To extend beyond the 256 column locations on M1-M5, the row address and $\overline{RAS}$ are applied to multiple modules. $\overline{CAS}$ is then decoded to select the proper module.

power up

After power up, the power supply must remain at its steady-state value for 1 ms. In addition, $\overline{RAS}$ must remain high for 100 μs immediately prior to initialization. Initialization consists of performing eight $\overline{RAS}$ cycles before proper device operation is achieved.

sequential-access operation

$\overline{TR}/\overline{QE}$

Memory transfer operations involving parallel use of the shift registers are first indicated by bringing $\overline{TR}/\overline{QE}$ low before $\overline{RAS}$ falls low. This enables the switches connecting the 256 elements of the shift registers to the 256 bit lines of the memory array. The $\overline{W}$ line determines whether the data will be transferred from or to the shift registers.

write enable ($\overline{W}$)

In the sequential-access mode, $\overline{W}$ determines whether a transfer will occur from the shift registers to the memory array, or from the memory array to the shift registers. To transfer from the shift registers to the memory array, $\overline{W}$ is held low as $\overline{RAS}$ falls, and, to transfer from the memory array to the shift registers, $\overline{W}$ is held high as $\overline{RAS}$ falls. Thus, reads and writes are always with respect to the memory array. The write setup and hold times are referenced to the falling edge of $\overline{RAS}$ for this mode of operation.

row address (A0 through A7)

Eight address bits are required to select one of the 256 possible rows involved in the transfer of data to or from the shift registers. A0-A7, $\overline{W}$, and $\overline{TR}/\overline{QE}$ are latched on the falling edge of $\overline{RAS}$.

register column address (A7, A6)

To select one of the four shift register segments within each shift register (transfer from memory to register only), the appropriate 2-bit column address (A7, A6) must be valid when $\overline{CAS}$ falls. However, the $\overline{CAS}$ and segment address signals need not be supplied every transfer cycle, only when it is desired to change or select a new segment.

SCLK

Data is shifted in and out on the rising edge of SCLK. This makes it possible to view each shift register as though it were made of 256 rising edge D flip-flops connected D to Q. The TM4161EP5 is designed to work with a wide range duty cycle clock to simplify system design. Note that data will appear at the SOUT pins not only on the rising edge of SCLK but also after an access time of $t_{a(RSO)}$ from $\overline{RAS}$ high during a parallel load of the shift registers.

SIN and SOUT

Data is shifted in through the SIN pins and is shifted out through the SOUT pins. The TM4161EP5 is designed such that it requires 3 ns hold time on SIN as SCLK rises. SOUT is guaranteed not to change for at least

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8 ns after SCLK rises. When loading data into the shift registers from the serial inputs in preparation for a shift register to memory transfer operation, the serial clock must be clocked an even number of times. To guarantee proper serial clock sequence after power up, a transfer cycle must be initiated before a serial data stream is applied at SIN.

$\overline{SOE}$

The serial output enable pin controls the impedance of the serial outputs, allowing multiplexing of more than one bank of TM4161EP5 memories into the same external video circuitry. When $\overline{SOE}$ is at a logic low level, the SOUTs will be enabled and the proper data read out. When $\overline{SOE}$ is at a logic high level, the SOUTs will be disabled and be in the high-impedance state.

refresh

The shift registers are also dynamic storage elements. The data held in the registers will be lost unless SCLK goes high to shift the data one bit position, a transfer write operation is invoked, or the data is reloaded from the memory array. See specifications for maximum register data retention times. Important: If the shift registers have remained idle for a time period which exceeds the maximum SCLK high or SCLK low time, the dynamic clock circuits will lose charge. Under these conditions, the shift register clocks must be re-enabled by performing any transfer cycle before data can be shifted into or out of the shift registers.

single-in-line package and components

PC substrate: 0,79 mm (0.031 inch) minimum thickness
Bypass capacitors: Multilayer ceramic
Leads: Tin/lead solder coated over phosphor-bronze

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin except V_{DD} and data out (see Note 1) . . . . . −1.5 V to 10 V
Voltage range on V_{DD} supply and data out with respect to V_{SS} . . . . . −1 V to 6 V
Short circuit output current . . . . . 50 mA
Power dissipation . . . . . 5 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		$V_{DD}+0.3$	V
V_{IL}	Low-level input voltage (see Notes 2 and 3)	−0.6		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTES: 2. The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.
3. Due to input protection circuitry, the applied voltage may begin to clamp at −0.6 V; test conditions must comprehend this occurrence.
4. See application report entitled "TMS4164A and TMS4416 Input Protection Diode" on page 9-5.

electrical characteristics over full range of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TM4161EP5-15			TM4161EP5-20			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage (DQ1-DQ5, SOUT1-SOUT5)	I_{OH} = −5 mA	2.4			2.4			V
V_{OL}	Low-level output voltage (DQ1-DQ5, SOUT1-SOUT5)	I_{OL} = 4.2 mA			0.4			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 5.8 V, V_{DD} = 5 V, All other pins = 0 V			±10			±10	μA
I_O	Output current (leakage) (DQ1-DQ5, SOUT1-SOUT5)	V_O = 0.4 V to 5.5 V, V_{DD} = 5 V			±10			±10	μA
I_{DD1}	Average operating current during read or write cycle	$t_{c(rd)}$ = minimum cycle time, $\overline{TR}/\overline{QE}$ low after $\overline{RAS}$ falls,‡ SCLK and SIN low, $\overline{SOE}$ high, No load on DQ1-DQ5 and SOUT1-SOUT5		250	350		250	350	mA
I_{DD2}§	Standby current	After 1 $\overline{RAS}$ cycle, $\overline{RAS}$ and $\overline{CAS}$ high, SCLK and SIN low, $\overline{SOE}$ high, No load on DQ1-DQ5 and SOUT1-SOUT5		80	100		80	100	mA
I_{DD3}	Average refresh current	$t_{c(rd)}$ = minimum cycle time, $\overline{CAS}$ high, $\overline{RAS}$ cycling, SCLK and SIN low, $\overline{SOE}$ high, $\overline{TR}/\overline{QE}$ high, No load on DQ1-DQ5 and SOUT1-SOUT5		210	275		185	250	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle time, $\overline{RAS}$ low, $\overline{CAS}$ cycling, $\overline{TR}/\overline{QE}$ low after $\overline{RAS}$ falls, SCLK and SIN low, $\overline{SOE}$ high, No load on DQ1-DQ5 and SOUT1-SOUT5		225	275		200	250	mA
I_{DD5}	Average shift register current (includes I_{DD2})	$\overline{RAS}$ and $\overline{CAS}$ high, $t_{c(SCLK)}$ = $t_{c(SCLK)}$ min, No load on DQ1-DQ5 and SOUT1-SOUT5		150	200		150	200	mA
I_{DD6}	Worst case average DRAM and shift register current	$t_{c(rd)}$ = minimum cycle time, $t_{c(SCLK)}$ = minimum cycle time, $\overline{TR}/\overline{QE}$ low after $\overline{RAS}$ falls, No load on DQ1-DQ5 and SOUT1-SOUT5		425	475		400	450	mA

†All typical values are at T_A = 25°C and nominal supply voltages.
‡See appropriate timing diagram.
§V_{IL} > −0.6 V

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capacitance over recommended supply voltage and operating free-air temperature range, f = 1 MHz

PARAMETER		MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs	35	pF
$C_{i(DQ)}$	Input capacitance, data inputs	25	
$C_{i(RC)}$	Input capacitance, strobe inputs	50	
$C_{i(W)}$	Input capacitance, write enable input	50	
$C_{i(CK)}$	Input capacitance, serial clock	50	
$C_{i(SI)}$	Input capacitance, serial in	25	
$C_{i(SOE)}$	Input capacitance, serial output enable	30	
$C_{i(TR)}$	Input capacitance, register transfer input	35	
$C_{o(SOUT)}$	Output capacitance, serial out	35	

†All typical values are at T_A = 25°C and nominal supply voltages.

switching characteristics over recommended supply voltage range and operating free-air temperature range (see Figure 1)

PARAMETER		TEST CONDITIONS†	ALT. SYMBOL	TM4161EP5-15		TM4161EP5-20		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 100 pF	t_{CAC}		100		135	ns
$t_{a(QE)}$	Access time of Q from $\overline{TR}/\overline{QE}$ low	C_L = 100 pF			40		50	
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, C_L = 100 pF	t_{RAC}		150		200	
$t_{a(RSO)}$	$\overline{SOUT}$ access time from $\overline{RAS}$ high	C_L = 30 pF			65		85	
$t_{a(SOE)}$	Access time from $\overline{SOE}$ low to SOUT	C_L = 30 pF			30		30	
$t_{a(SO)}$	Access time from SCLK	C_L = 30 pF			45		50	
$t_{dis(CH)}$‡	Q output disable time from $\overline{CAS}$ high	C_L = 100 pF	t_{OFF}		40		40	
$t_{dis(QE)}$‡	Q output disable time from $\overline{TR}/\overline{QE}$ high	C_L = 100 pF			40		40	
$t_{dis(SOE)}$‡	Serial output disable time from $\overline{SOE}$ high	C_L = 30 pF			30		30	

†Figure 1 shows the load circuit.
‡The maximum values for $t_{dis(CH)}$, $t_{dis(QE)}$, and $t_{dis(SOE)}$ define the time at which the output achieves the open circuit condition and are not referenced to V_{OH} or V_{OL}.

timing requirements over recommended supply voltage range and operating free-air temperature range

		ALT. SYMBOL	TM4161EP5-15		TM4161EP5-20		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(P)}$	Page-mode cycle time	t_{PC}	160		225		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	240		315		ns
$t_{c(W)}$	Write cycle time	t_{WC}	240		315		ns
$t_{c(TW)}$	Transfer write cycle time‡		240		315		ns
$t_{c(Trd)}$	Transfer read cycle time		240		315		ns
$t_{c(SCLK)}$	Serial-clock cycle time	t_{SCC}	45	50,000	50	50,000	ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (precharge time)§	t_{CP}	50		80		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low	t_{CAS}	100	10,000	135	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge time)	t_{RP}	80		105		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low	t_{RAS}	150	10,000	200	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	45		45		ns
$t_{w(CKL)}$	Pulse duration, SCLK low		10		10		ns
$t_{w(CKH)}$	Pulse duration, SCLK high		12		12		ns
$t_{w(QE)}$	$\overline{TR}/\overline{QE}$ pulse duration low time (read cycle)		40		40		ns
t_t	Transition times (rise and fall) $\overline{RAS}$, $\overline{CAS}$, and SCLK	t_T	3	50	3	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		0		ns
$t_{su(RW)}$	$\overline{W}$ setup time before $\overline{RAS}$ low with $\overline{TR}/\overline{QE}$ low		0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		0		ns
$t_{su(WCL)}$	Early write-command setup time before $\overline{CAS}$ low	t_{WCS}	−5		−5		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	40		60		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	40		60		ns
$t_{su(TR)}$	$\overline{TR}/\overline{QE}$ setup time before $\overline{RAS}$ low		0		0		ns
$t_{su(SI)}$	Serial-data setup time before SCLK high		6		6		ns
$t_{h(SI)}$	Serial-data-in hold time after SCLK high		3		3		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	45		55		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	20		25		ns
$t_{h(RW)}$	$\overline{W}$ hold time after $\overline{RAS}$ low with $\overline{TR}/\overline{QE}$ low		20		20		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	95		120		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	60		80		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	110		145		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	45		55		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		ns

(Continued next page.)

NOTE 5: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, V_{IL} max and V_{IH} min must be met at the 10% and 90% points.

†All cycle times assume t_t = 5 ns except $t_{c(SCLK)}$ which assumes t_t = 3 ns.

‡Multiple transfer write cycles require separation by either a 500-ns $\overline{RAS}$-precharge interval or any other active $\overline{RAS}$-cycle.

§Page-mode only.

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timing requirements over recommended supply voltage range and operating free-air temperature range (concluded)

		ALT. SYMBOL	TM4161EP5-15		TM4161EP5-20		UNIT
			MIN	MAX	MIN	MAX	
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	5		5		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	60		80		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	110		145		ns
$t_{h(RSO)}$	Serial-data-out hold time after $\overline{RAS}$ low with $\overline{TR}/\overline{QE}$ low		30		30		ns
$t_{h(SO)}$	Serial-data-out hold time after SCLK high		8		8		ns
$t_{h(TR)}$	$\overline{TR}/\overline{QE}$ hold time after $\overline{RAS}$ low (transfer)		20		20		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	150		200		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
t_{CLQEH}	Delay time, $\overline{CAS}$ low to $\overline{QE}$ high		100		135		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	100		135		ns
t_{CQE}	Delay time, $\overline{CAS}$ low to $\overline{QE}$ low (maximum value specified only to guarantee $t_{a(QE)}$ access time)			60		85	ns
t_{RHSC}	Delay time, $\overline{RAS}$ high to SCLK high		80	50,000	80	50,000	ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	25	50	30	65	ns
t_{CKRL}	Delay time, SCLK high before $\overline{RAS}$ low with $\overline{TR}/\overline{QE}$ low¶		10	50,000	10	50,000	ns
$t_{rf(MA)}$	Refresh time interval, memory array	t_{REF1}		4		4	ms
$t_{rf(SR)}$	Refresh time interval, shift register#	t_{REF2}		50,000		50,000	ns

NOTE 5: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, V_{IL} max and V_{IH} min must be met at the 10% and 90% points.

¶SCLK may be high or low during $t_{w(RL)}$, but there can not be any positive edge transitions on SCLK for a minimum of 10 ns prior to $\overline{RAS}$ going low with $\overline{TR}/\overline{QE}$ low (i.e., before a transfer cycle).

#See "refresh" on page 5-9.

PARAMETER MEASUREMENT INFORMATION

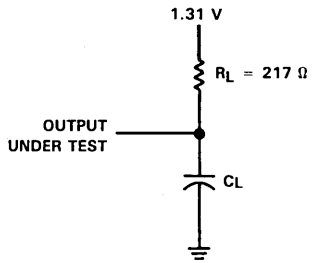
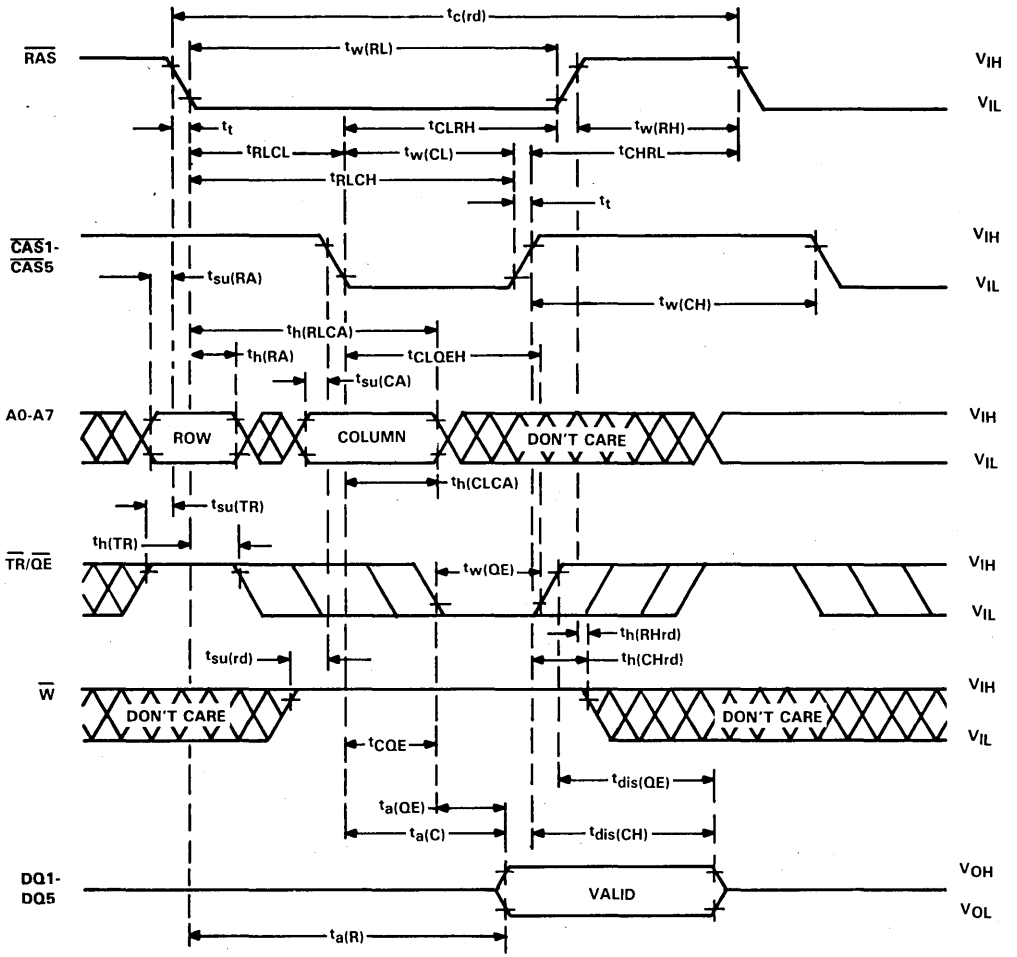


FIGURE 1. LOAD CIRCUIT

read cycle timing



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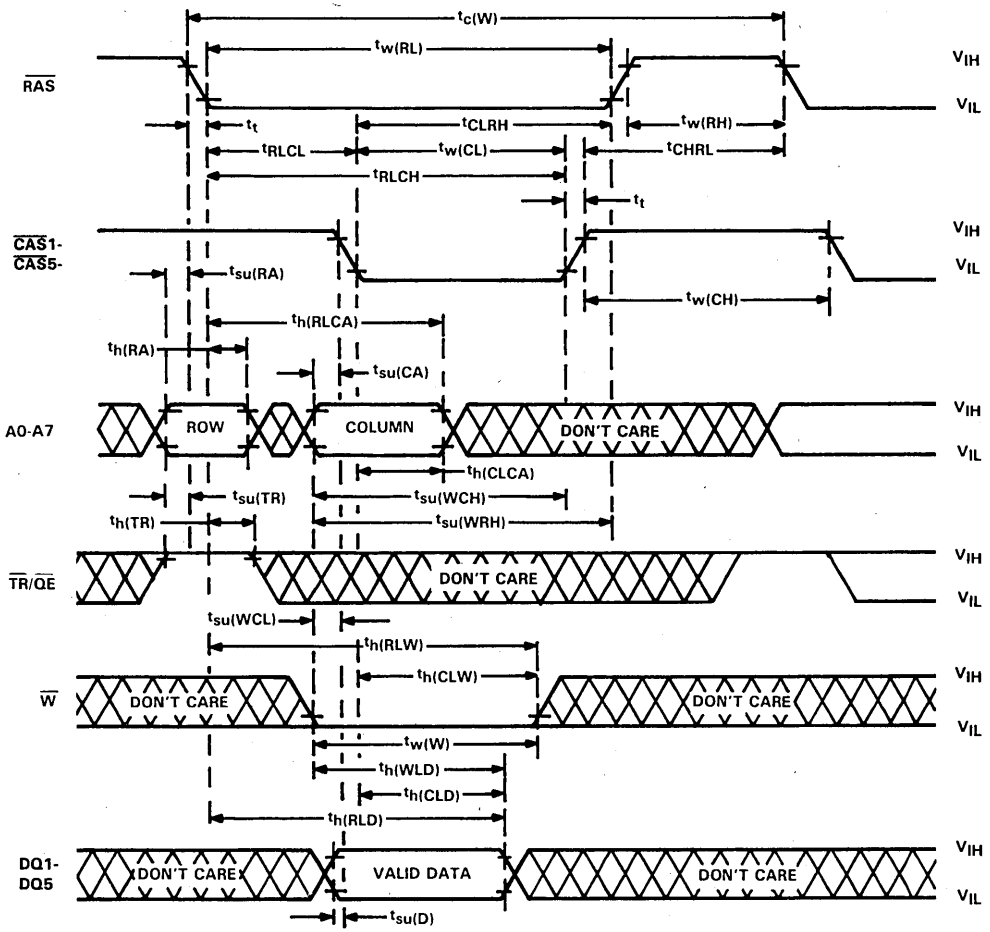
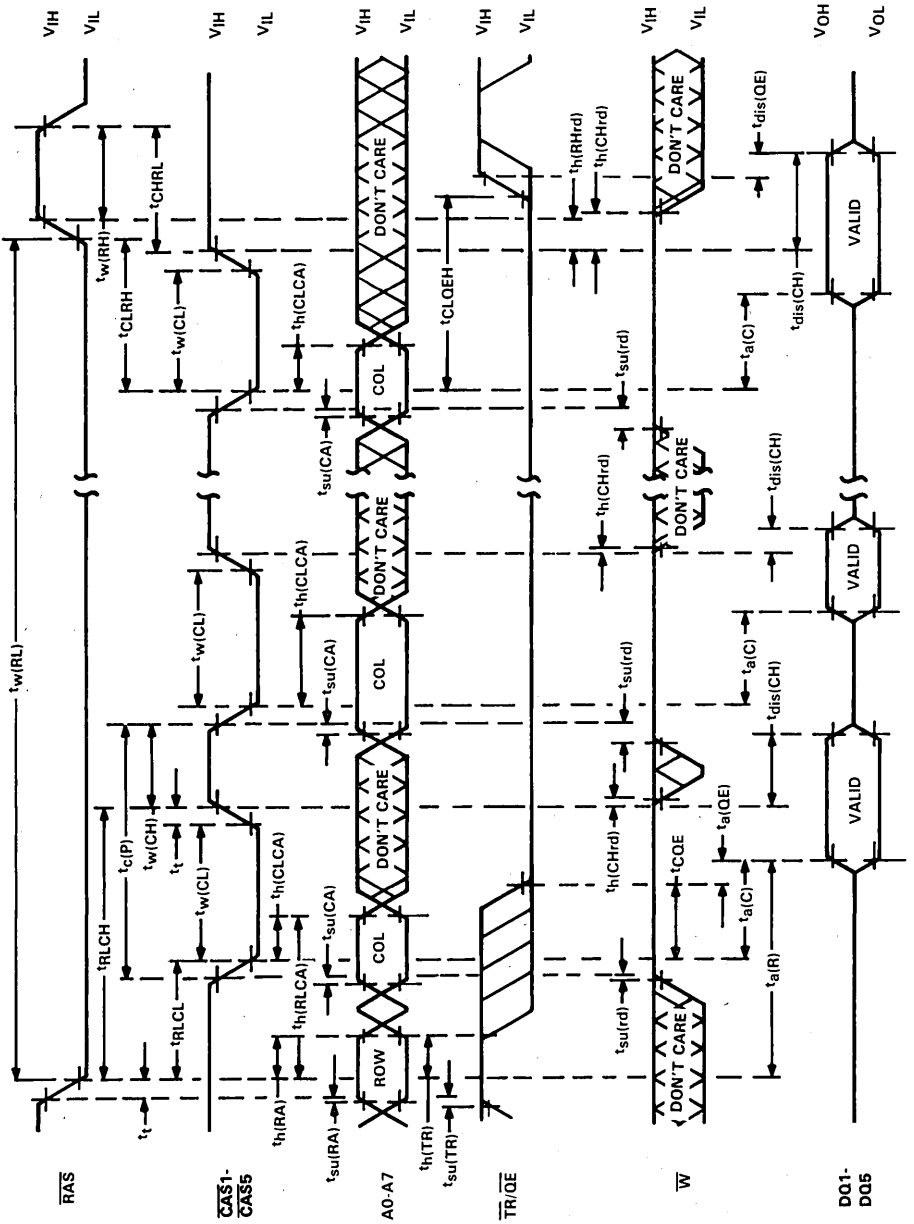
early write cycle timing

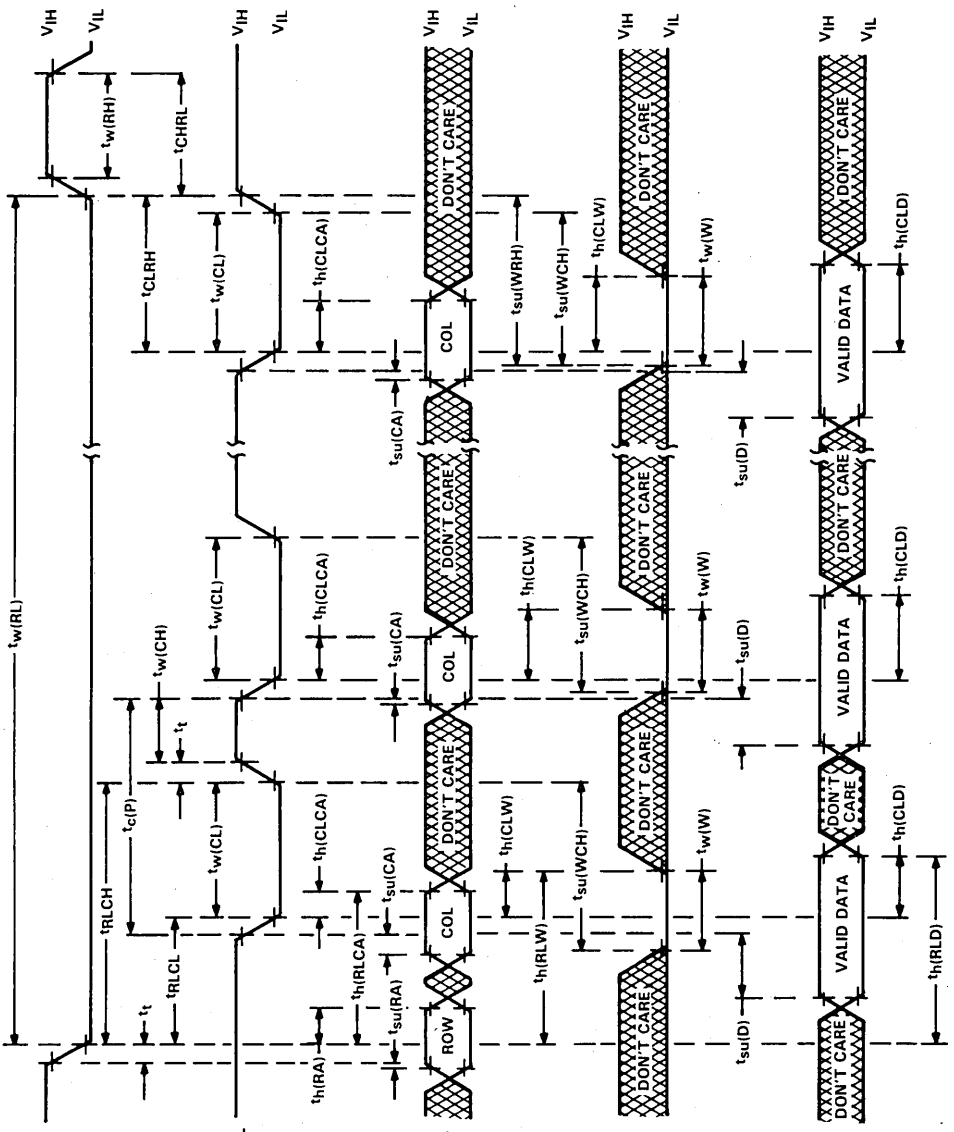


page-mode read cycle timing



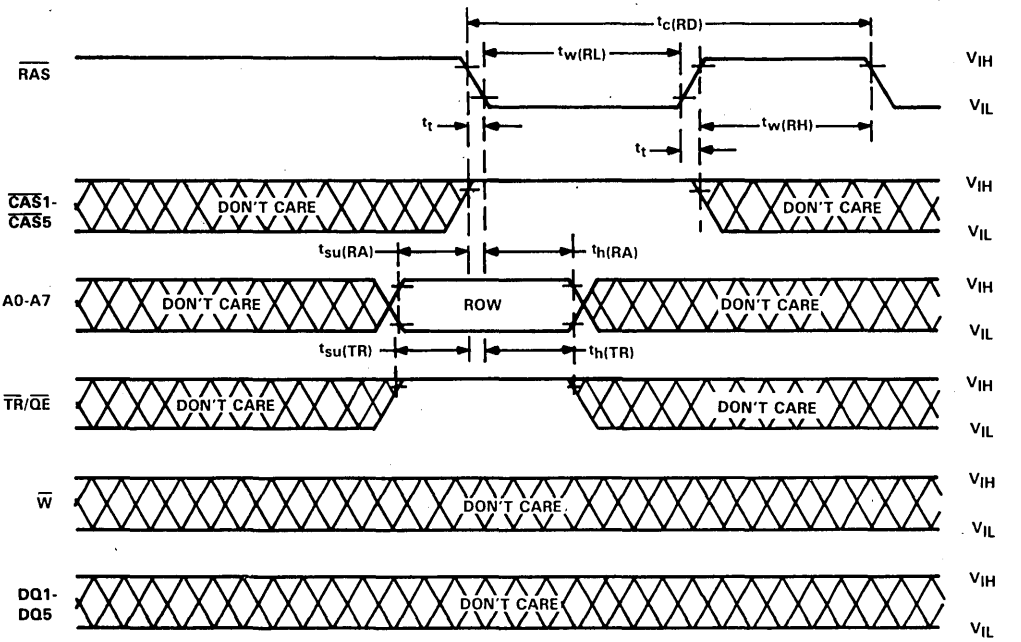
NOTES: 6. Timing is for non-multiplexed DQ and address lines.
7. A write cycle or a read-modify-write cycle can be intermixed with read cycles as long as the write and read-modify-write timing specifications are not violated.

page-mode write cycle timing



NOTES: 6. Timing is for non-multiplexed DQ and address lines.
8. A read cycle or a read-modify-write cycle can be intermixed with write cycles as long as the read and read-modify-write timing specifications are not violated.

$\overline{RAS}$-only refresh timing



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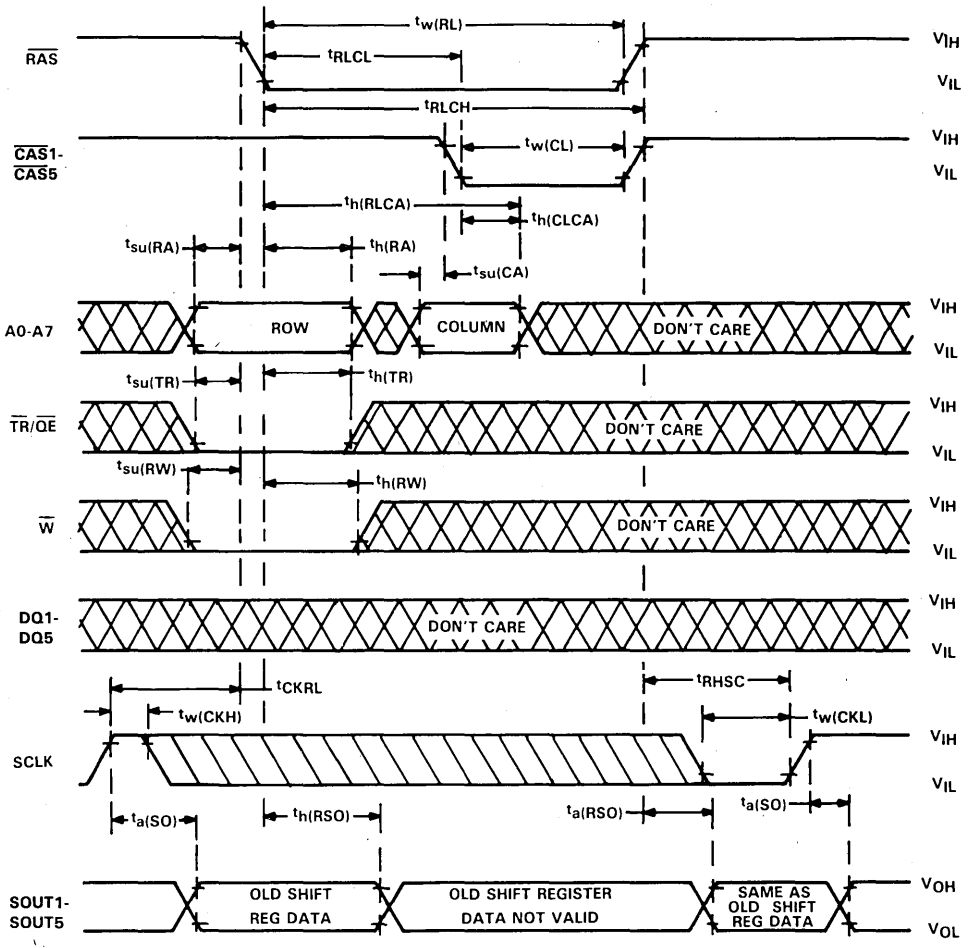
shift register to memory timing

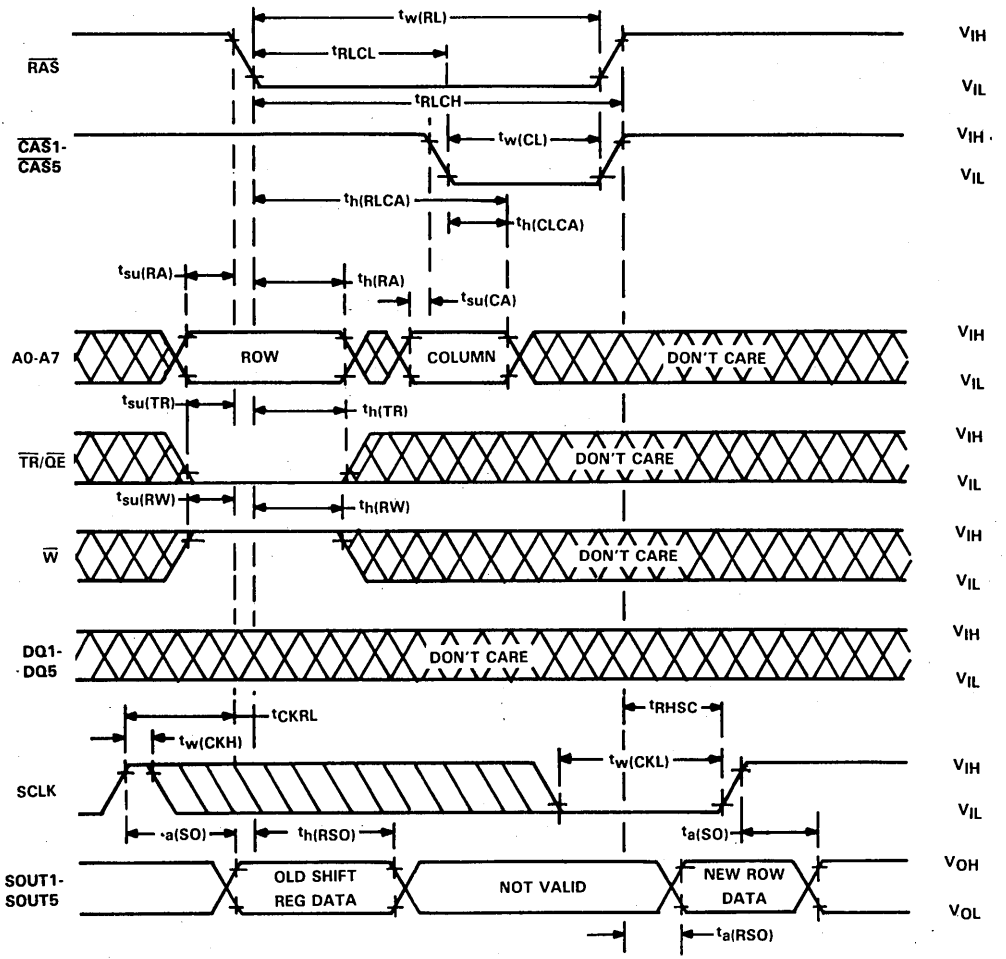


NOTES: 9. The shift register to memory cycle is used to transfer data from the shift registers to the memory array. Every one of the 256 locations in each shift register is written into the 256 columns of the selected row. Note that the data that was in the shift registers may have resulted, either from a serial shift in or from a parallel load of the shift registers from one of the memory array rows.

10. $\overline{SOE}$ assumed low.

11. SCLK may be high or low during $t_{w(RL)}$.

memory to shift register timing



NOTES: 10. $\overline{SOE}$ assumed low.
11. SCLK may be high or low during $t_{w(RL)}$.
12. The memory to shift register cycle is used to load the shift registers in parallel from the memory array. Every one of the 256 locations in each shift register are written into from the 256 columns of the selected row. Note that the data that is loaded into the shift registers may be either shifted out or written back into another row.

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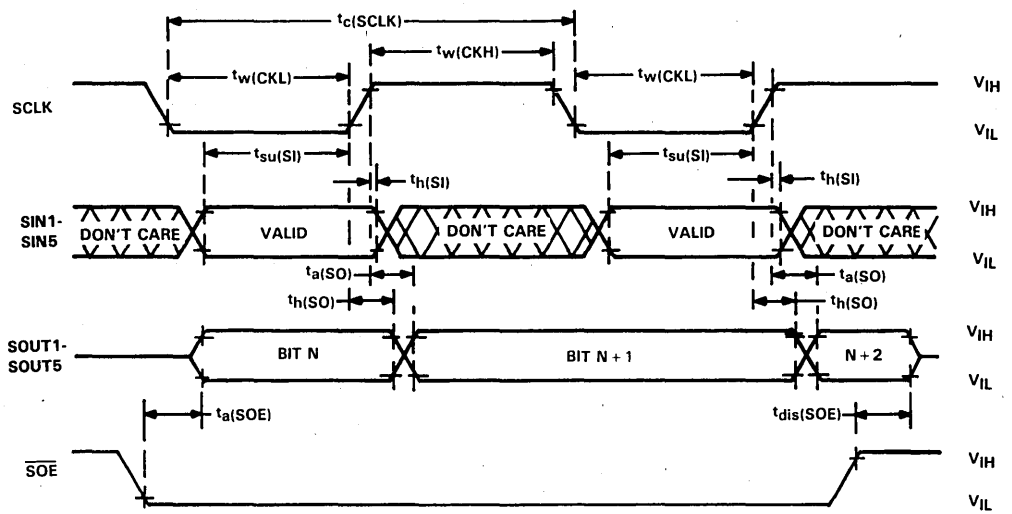
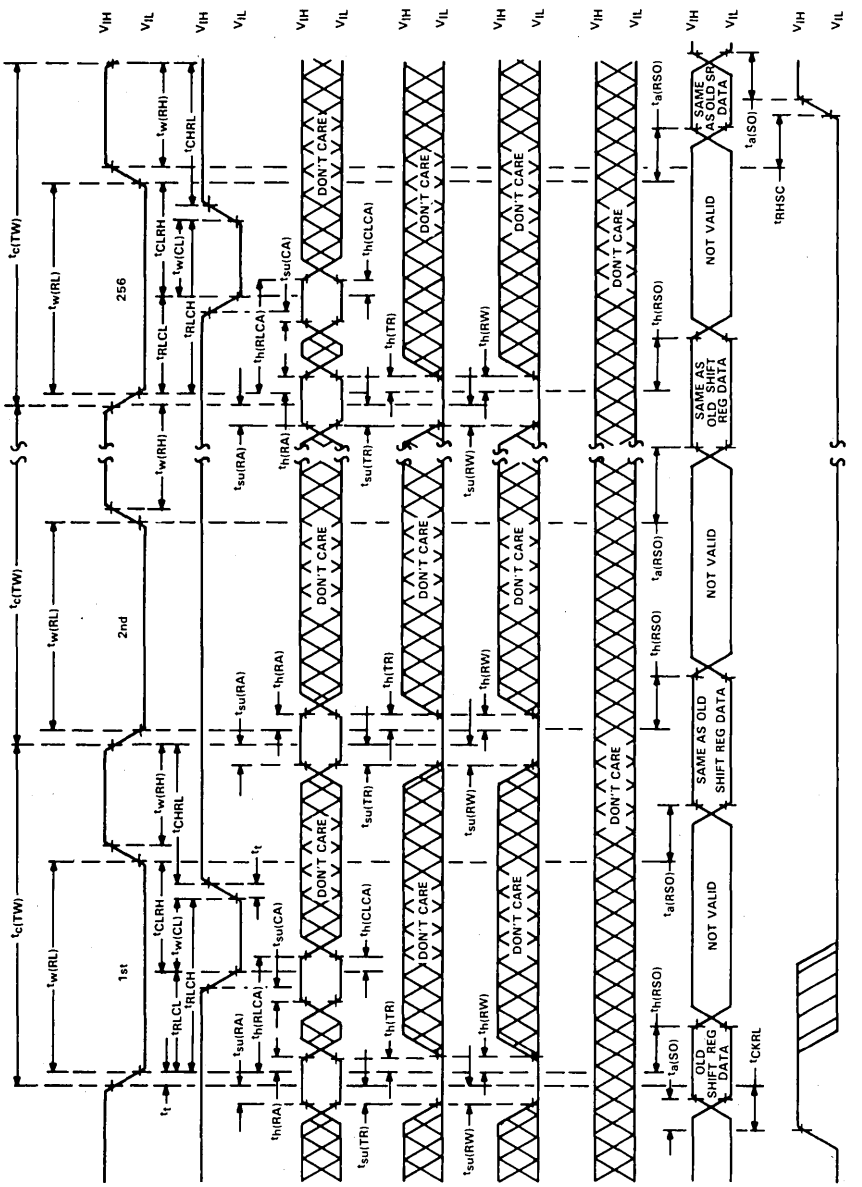
serial data shift timing



NOTES: 13. When loading data into the shift registers from the serial input in preparation for a shift register to memory transfer operation, the serial clock must be clocked an even number of times.

14. While shifting data through the serial shift registers, the state of $\overline{TR}/\overline{QE}$ is a don't care as long as $\overline{TR}/\overline{QE}$ is held high when $\overline{RAS}$ goes low and $t_{su(TR)}$ and $t_{h(TR)}$ timings are observed. This requirement avoids the initiation of a register-to-memory or memory-to-register data transfer operation. The serial data transfer cycle is used to shift data in and/or out of the shift registers.

shift register to memory multiple timing



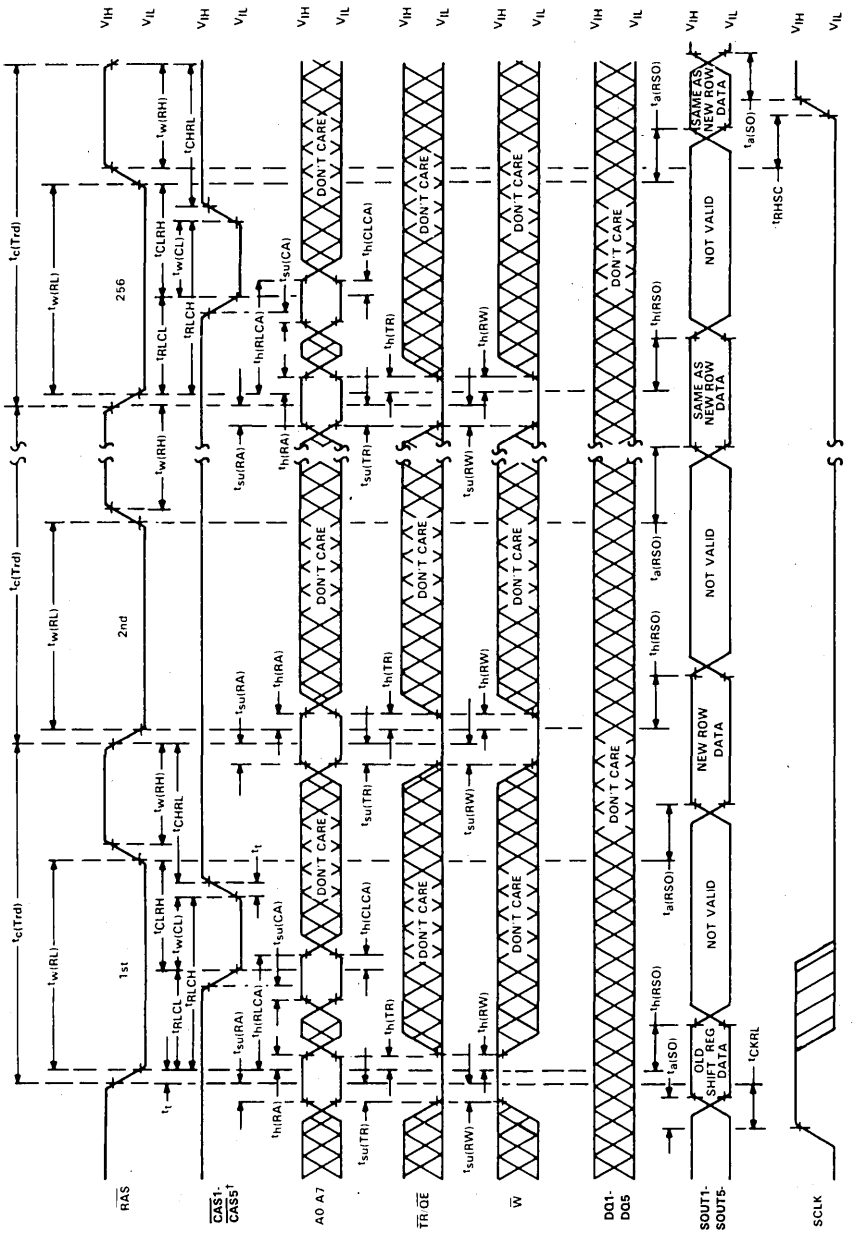
†CAS and register address need not be supplied every cycle, only when it is desired to change or select a new register length.

NOTES: 10. $\overline{SOE}$ assumed low.

15. The shift register to memory multiple cycle is used to write the shift register data to more than one row of the memory array. An application of this could be clearing all memory. To do this, the SIN lines would be held at 0 to fill all locations in the shift registers with 0's. The shift registers would then be written into all 256 rows of the memory array in 256 cycles. The random output ports (DQ1-DQ5) will be in a high-impedance state as long as register transfer cycles are selected.

16. SCLK is a don't care except that no positive transitions on SCLK can occur for a period equal to t_{CKRL} prior to $\overline{RAS}$ falling with $\overline{TR}/\overline{QE}$ low.

memory to shift register to memory multiple timing

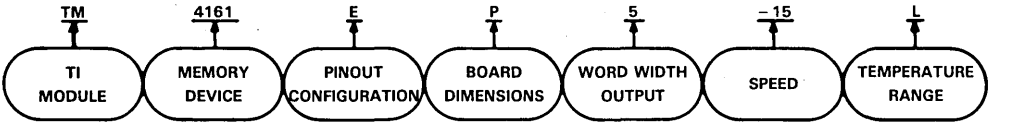


†$\overline{CAS}$ and register address need not be supplied every cycle, only when it is desired to change from one register address to another.

NOTES: 10. $\overline{SOE}$ assumed low.

16. SCLK is a don't care except that no positive transitions on SCLK can occur for a period equal to t_{CKRL} prior to $\overline{RAS}$ falling with $\overline{TR}/\overline{QE}$ low.
17. The memory to shift register to memory multiple cycle is used to reorder the rows within the memory array itself. First, the data in a row is stored in the shift register and then it is written into other selected rows. The random output port Q will be in a high-impedance state as long as register transfer cycles are selected.

TI single-in-line package nomenclature



(88,9 x 11,4 mm)
(3.5 x 0.45 inches)

Max Access
–15 150 ns
–20 200 ns

L 0°C to 70°C

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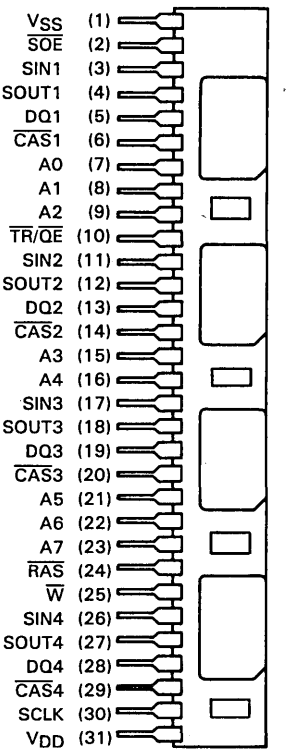
JULY1984 — REVISED NOVEMBER 1985

- 65,536 X 4 Organization
- Single 5-V Supply (10% Tolerance)
- 31-Pin Single-in-Line Package (SIP)
- Utilizes Four Multiport Video RAMs in Plastic Chip Carriers
- Serial In/Serial Out Capability
- Dual Accessibility — One Port Sequential Access, One Port Random Access
- Four Serial Shift Registers for Sequential Access Applications, Each Comprised of Four Cascaded 64-Bit Segments
- Designed for both Video and Non-Video Applications
- Fast Serial Port . . . Can Be Configured for Video Data Rates in Excess of 150 MHz
- $\overline{TR}/\overline{QE}$ as Output Enable Allows Direct Connection of DQ and Address Lines to Simplify System Design
- Separate Serial In and Serial Out to Allow Simultaneous Shift In and Out
- Supported by TI's TMS34061 Video System Controller (VSC)
- $\overline{SOE}$ Simplifies Multiplexing of Serial Data Streams
- Long Refresh Period . . . 4 ms (256 Cycles)
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Outputs
- Performance Ranges:

	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)
TM4161EV4-15	150 ns	100 ns	240 ns
TM4161EV4-20	200 ns	135 ns	315 ns

- Separate $\overline{CAS}$ Control with Common Data-In and Data-Out Lines
- Low Power Dissipation:
  - —Operating . . . 1000 mW (Typ)
  - —Standby . . . 320 mW (Typ)
- Operating Free-Air Temperature . . . 0°C to 70°C

V SINGLE-IN-LINE PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A7	Address Inputs
$\overline{CAS}1$-$\overline{CAS}4$	Column-Address Strobes
DQ1-DQ4	Random-Access Data In/Data Out
$\overline{RAS}$	Row-Address Strobe
SCLK	Serial Data Clock
SIN1-SIN4	Serial Data In
$\overline{SOE}$	Serial Output Enable
SOUT1-SOUT4	Serial Data Out
$\overline{TR}/\overline{QE}$	Register Transfer/Q Output Enable
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The TM4161EV4 is a 256K dual-access dynamic random-access memory module organized as 65,536 × 4-bits in a 31-pin single-in-line package comprising four TMS4161FML, 65,536 × 1-bit Multiport Video RAMs in 22-lead plastic chip carriers mounted on top of a substrate together with four decoupling capacitors. The random-access port makes the memory look like it is organized as 65,536 words of four bits each. The sequential access port is interfaced to four internal 256-bit dynamic shift registers each organized as four cascaded 64-bit shift register segments which are accessed serially. One, two, three, or four 64-bit shift register segments can be sequentially read out after a transfer cycle depending on a two-bit code applied to the two most significant column address inputs.

The TM4161EV4 features full asynchronous dual access capability except when transferring data between the shift registers and the memory array.

Refresh period is extended to 4 milliseconds, and during this period each of the 256 rows must be strobed with $\overline{RAS}$ in order to retain data. $\overline{CAS}$ can remain high during the refresh sequence to conserve power. Note that the transfer of a row of data from the memory array to the shift registers also refreshes that row.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address lines and data in are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TM4161EV4 is guaranteed for operation from 0°C to 70°C.

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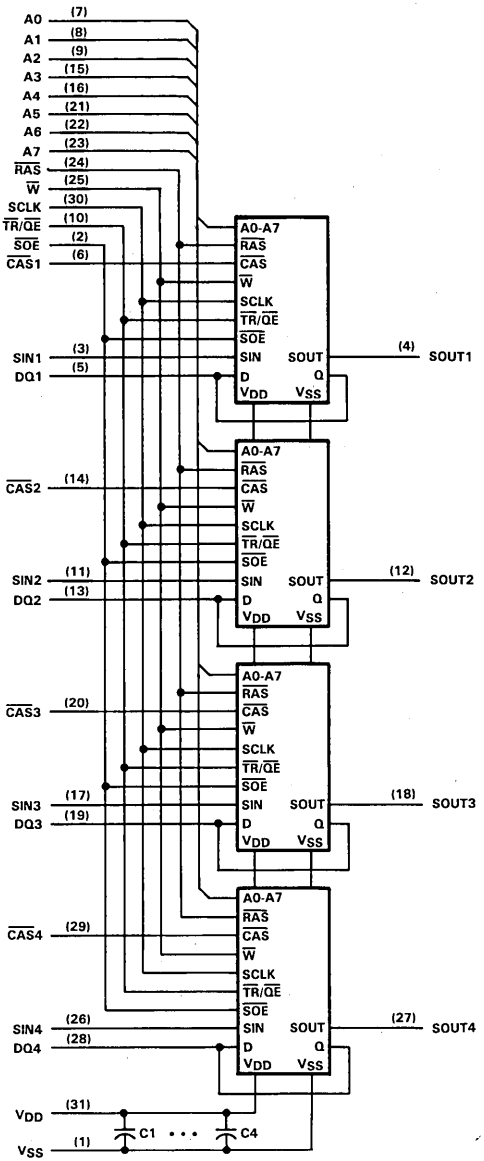
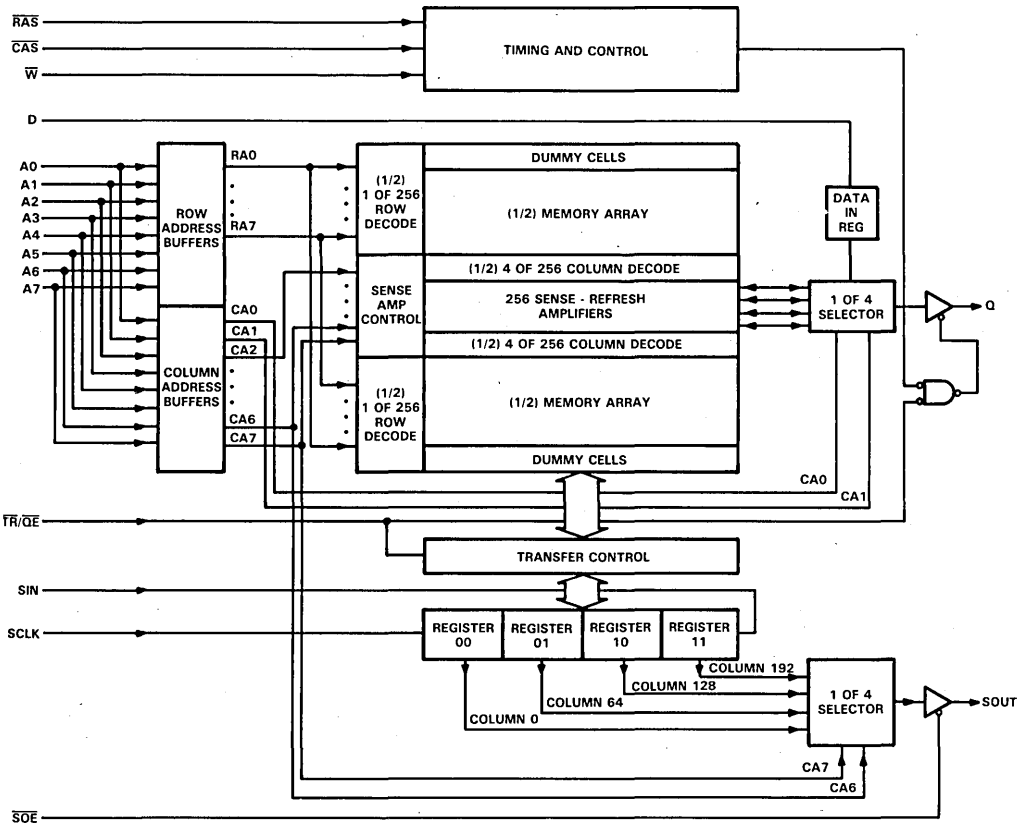
functional block diagram



TMS4161 functional block diagram



random-access address space to sequential-address space mapping

The TM4161EV4 is designed with each row divided into four, 64-column sections which map directly onto the four segments of each shift register (see TMS4161 functional block diagram). The first column section to be shifted out is selected by the two most-significant column-address bits. If the two bits represent binary 00, then one to four register segments can be shifted out in order. If the two bits represent binary 01, then only 1 to 3 (the most significant) register segments can be shifted out in order. If the two bits represent 10, then one to two of the most-significant register segments can be shifted out in order. Finally, if the two bits represent 11 only the most-significant register segment can be shifted out. All register segments are shifted out with the least-significant bit (bit 0) first and the most-significant bit (bit 63) last. Note that if the two column-address bits equal 00 during the last register transfer cycle ($\overline{TR}/\overline{QE}$ at logic level "0" as $\overline{RAS}$ falls) a total of 256 bits can be sequentially read out of each serial output pin.

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random-access operation

$\overline{TR}/\overline{QE}$

The $\overline{TR}/\overline{QE}$ pin has two functions. First, it selects either register transfer or random-access operation as $\overline{RAS}$ falls, and second, during a random-access operation, it functions as an output enable after $\overline{CAS}$ falls.

To use the TM4161EV4 in the random-access mode, $\overline{TR}/\overline{QE}$ must be high as $\overline{RAS}$ falls. Holding $\overline{TR}/\overline{QE}$ high as $\overline{RAS}$ falls keeps the 256 elements of the shift registers disconnected from the corresponding 256 bit lines of the memory array. If data is to be shifted, the shift registers must be disconnected from the bit lines. Holding $\overline{TR}/\overline{QE}$ low as $\overline{RAS}$ falls enables the 256 switches that connect the shift registers to the bit lines and indicates that a transfer will occur between the shift registers and one of the memory rows.

During random-access operation, once $\overline{CAS}$ has been pulled low, $\overline{TR}/\overline{QE}$ controls when the data will appear at the Q output (if this a read cycle). Whenever $\overline{TR}/\overline{QE}$ is held high during random-access operation, the Q output will be in the high-impedance state. This feature removes the possibility of an overlap between data on the address lines and data appearing on the Q output making it possible to connect the address lines to the Q and D lines (Use of this organization prohibits the use of the early write cycle.).

address (A0 through A7)

Sixteen address bits are required to decode 1 of 65,536 storage cell locations. Eight row-address bits are set up on pins A0 through A7 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the eight column-address bits are set up on pins A0 through A7 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data inputs are disabled when the read mode is selected. The common I/O feature of the TM4161EV4 dictates the use of early write cycles to prevent contention on DQ. When $\overline{W}$ goes low prior to $\overline{CAS}$, the data outputs will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data in (DQ1-DQ4)

Data is written during a write or read-modify-write cycle. The falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. This latch can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal.

data out (DQ1-DQ4)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan out of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state as long as $\overline{CAS}$ or $\overline{TR}/\overline{QE}$ is held high. Data will not appear on the output until after both $\overline{CAS}$ and $\overline{TR}/\overline{QE}$ have been brought low. In a read cycle, the guaranteed maximum output enable access time is valid only if t_{CQE} is greater than t_{CQE} MAX, and t_{RLCL} is greater than t_{RLCL} MAX. Likewise, $t_{a(C)}$ MAX is valid only if t_{RLCL} is greater than t_{RLCL} MAX. Once the output is valid, it will remain valid while $\overline{CAS}$ and $\overline{TR}/\overline{QE}$ are both low; $\overline{CAS}$ or $\overline{TR}/\overline{QE}$ going high will return the output to a high-impedance state. In an early write cycle, the output is always in a high-impedance state. In a register transfer cycle, the output will always be in a high-impedance state.

refresh

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffer is in high-impedance state unless $\overline{CAS}$ is applied, the $\overline{RAS}$-only refresh sequence avoids any output

during refresh. Strobing each of the 256 row addresses (A0 through A7) with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power.

page mode

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the module. Thus, the time required to setup and strobe sequential row addresses for the same page is eliminated. To extend beyond the 256 column locations on M1-M4, the row address and $\overline{RAS}$ are applied to multiple modules. $\overline{CAS}$ is then decoded to select the proper module.

power up

After power up, the power supply must remain at its steady-state value for 1 ms. In addition, $\overline{RAS}$ must remain high for 100 μs immediately prior to initialization. Initialization consists of performing eight $\overline{RAS}$ cycles before proper device operation is achieved.

sequential-access operation

$\overline{TR}/\overline{QE}$

Memory transfer operations involving parallel use of the shift registers are first indicated by bringing $\overline{TR}/\overline{QE}$ low before $\overline{RAS}$ falls low. This enables the switches connecting the 256 elements of the shift registers to the 256 bit lines of the memory array. The $\overline{W}$ line determines whether the data will be transferred from or to the shift registers.

write enable ($\overline{W}$)

In the sequential-access mode, $\overline{W}$ determines whether a transfer will occur from the shift registers to the memory array, or from the memory array to the shift registers. To transfer from the shift registers to the memory array, $\overline{W}$ is held low as $\overline{RAS}$ falls, and, to transfer from the memory array to the shift registers, $\overline{W}$ is held high as $\overline{RAS}$ falls. Thus, reads and writes are always with respect to the memory array. The write setup and hold times are referenced to the falling edge of $\overline{RAS}$ for this mode of operation.

row address (A0 through A7)

Eight address bits are required to select one of the 256 possible rows involved in the transfer of data to or from the shift registers. A0-A7, $\overline{W}$, and $\overline{TR}/\overline{QE}$ are latched on the falling edge of $\overline{RAS}$.

register column address (A7, A6)

To select one of the four shift register segments within each shift register (transfer from memory to register only), the appropriate 2-bit column address (A7, A6) must be valid when $\overline{CAS}$ falls. However, the $\overline{CAS}$ and segment address signals need not be supplied every transfer cycle, only when it is desired to change or select a new segment.

SCLK

Data is shifted in and out on the rising edge of SCLK. This makes it possible to view each shift register as though it were made of 256 rising edge D flip-flops connected D to Q. The TM4161EV4 is designed to work with a wide range duty cycle clock to simplify system design. Note that data will appear at the SOUT pins not only on the rising edge of SCLK but also after an access time of $t_{a(RSO)}$ from $\overline{RAS}$ high during a parallel load of the shift registers.

SIN and SOUT

Data is shifted in through the SIN pins and is shifted out through the SOUT pins. The TM4161EV4 is designed such that it requires 3 ns hold time on SIN as SCLK rises. SOUT is guaranteed not to change for at least 8 ns after SCLK rises. When loading data into the shift registers from the serial inputs in preparation for a shift register to memory transfer operation, the serial clock must be clocked an even number of times. To guarantee proper serial clock sequence after power up, a transfer cycle must be initiated before a serial data stream is applied at SIN.

$\overline{SOE}$

The serial output enable pin controls the impedance of the serial outputs, allowing multiplexing of more than one bank of TM4161EV4 memories into the same external video circuitry. When $\overline{SOE}$ is at a logic low level, the SOUTs will be enabled and the proper data read out. When $\overline{SOE}$ is at a logic high level, the SOUTs will be disabled and be in the high-impedance state.

refresh

The shift registers are also dynamic storage elements. The data held in the registers will be lost unless SCLK goes high to shift the data one bit position, a transfer write operation is invoked, or the data is reloaded from the memory array. See specifications for maximum register data retention times. Important: If the shift registers have remained idle for a time period which exceeds the maximum SCLK high or SCLK low time, the dynamic clock circuits will lose charge. Under these conditions, the shift register clocks must be re-enabled by performing any transfer cycle before data can be shifted into or out of the shift registers.

single-in-line package and components

PC substrate: 0,79 mm (0.031 inch) minimum thickness
Bypass capacitors: Multilayer ceramic
Leads: Tin/lead solder coated over phosphor-bronze

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin except V_{DD} and data out (see Note 1) . . . . . −1.5 V to 10 V
Voltage range on V_{DD} supply and data out with respect to V_{SS} . . . . . −1 V to 6 V
Short circuit output current . . . . . 50 mA
Power dissipation . . . . . 4 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		$V_{DD}+0.3$	V
V_{IL}	Low-level input voltage (see Notes 2 and 3)	−0.6		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTES: 2. The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.
3. Due to input protection circuitry, the applied voltage may begin to clamp at −0.6 V; test conditions must comprehend this occurrence.
4. See application report entitled "TMS4164A and TMS4416 Input Protection Diode" on page 9-5.

electrical characteristics over full range of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TM4161EV4-15			TM4161EV4-20			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage (DQ1-DQ4, SOUT1-SOUT4)	I_{OH} = −5 mA	2.4			2.4			V
V_{OL}	Low-level output voltage (DQ1-DQ4, SOUT1-SOUT4)	I_{OL} = 4.2 mA			0.4			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 5.8 V, V_{DD} = 5 V, All other pins = 0 V			±10			±10	μA
I_O	Output current (leakage) (DQ1-DQ4, SOUT1-SOUT4)	V_O = 0.4 V to 5.5 V, V_{DD} = 5 V			±10			±10	μA
I_{DD1}	Average operating current during read or write cycle	$t_{c(rd)}$ = minimum cycle time, $\overline{TR/QE}$ low after $\overline{RAS}$ falls,‡ SCLK and SIN low, $\overline{SOE}$ high, No load on DQ1-DQ4 and SOUT1-SOUT4		200	280		200	280	mA
I_{DD2}§	Standby current	After 1 $\overline{RAS}$ cycle, $\overline{RAS}$ and $\overline{CAS}$ high, SCLK and SIN low, $\overline{SOE}$ high, No load on DQ1-DQ4 and SOUT1-SOUT4		64	80		64	80	mA
I_{DD3}	Average refresh current	$t_{c(rd)}$ = minimum cycle time, $\overline{CAS}$ high, $\overline{RAS}$ cycling, SCLK and SIN low, $\overline{SOE}$ high, $\overline{TR/QE}$ high, No load on DQ1-DQ4 and SOUT1-SOUT4		168	220		148	220	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle time, $\overline{RAS}$ low, $\overline{CAS}$ cycling, $\overline{TR/QE}$ low after $\overline{RAS}$ falls, SCLK and SIN low, $\overline{SOE}$ high, No load on DQ1-DQ4 and SOUT1-SOUT4		180	220		160	220	mA
I_{DD5}	Average shift register current (includes I_{DD2})	$\overline{RAS}$ and $\overline{CAS}$ high, $t_{c(SCLK)}$ = $t_{c(SCLK)}$ min, No load on DQ1-DQ4 and SOUT1-SOUT4		120	160		120	160	mA
I_{DD6}	Worst case average DRAM and shift register current	$t_{c(rd)}$ = minimum cycle time, $t_{c(SCLK)}$ = minimum cycle time, $\overline{TR/QE}$ low after $\overline{RAS}$ falls, No load on DQ1-DQ4 and SOUT1-SOUT4		340	380		320	360	mA

†All typical values are at T_A = 25°C and nominal supply voltages.
‡See appropriate timing diagram.
§V_{IL} > −0.6 V

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capacitance over recommended supply voltage and operating free-air temperature range, f = 1 MHz

PARAMETER		MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs	35	pF
$C_{i(DQ)}$	Input capacitance, data inputs	20	
$C_{i(RC)}$	Input capacitance, strobe inputs	40	
$C_{i(W)}$	Input capacitance, write enable input	40	
$C_{i(CK)}$	Input capacitance, serial clock	30	
$C_{i(SI)}$	Input capacitance, serial in	20	
$C_{i(SOE)}$	Input capacitance, serial output enable	30	
$C_{i(TR)}$	Input capacitance, register transfer input	30	
$C_{o(SOUT)}$	Output capacitance, serial out	20	

†All typical values are at T_A = 25°C and nominal supply voltages.

switching characteristics over recommended supply voltage range and operating free-air temperature range (see Figure 1)

PARAMETER		TEST CONDITIONS†	ALT. SYMBOL	TM4161EV4-15		TM4161EV4-20		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 100 pF	t_{CAC}		100		135	ns
$t_{a(QE)}$	Access time of Q from $\overline{TR}/\overline{QE}$ low	C_L = 100 pF			40		50	
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, C_L = 100 pF	t_{RAC}		150		200	
$t_{a(RSO)}$	SOUT access time from $\overline{RAS}$ high	C_L = 30 pF			65		85	
$t_{a(SOE)}$	Access time from $\overline{SOE}$ low to SOUT	C_L = 30 pF			30		30	
$t_{a(SO)}$	Access time from SCLK	C_L = 30 pF			45		50	
$t_{dis(CH)}$‡	Q output disable time from $\overline{CAS}$ high	C_L = 100 pF	t_{OFF}		40		40	
$t_{dis(QE)}$‡	Q output disable time from $\overline{TR}/\overline{QE}$ high	C_L = 100 pF			40		40	
$t_{dis(SOE)}$‡	Serial output disable time from $\overline{SOE}$ high	C_L = 30 pF			30		30	

†Figure 1 shows the load circuit.
‡The maximum values for $t_{dis(CH)}$, $t_{dis(QE)}$, and $t_{dis(SOE)}$ define the time at which the output achieves the open circuit condition and are not referenced to V_{OH} or V_{OL}.

timing requirements over recommended supply voltage range and operating free-air temperature range

		ALT. SYMBOL	TM4161EV4-15		TM4161EV4-20		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(P)}$	Page-mode cycle time	t_{PC}	160		225		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	240		315		ns
$t_{c(W)}$	Write cycle time	t_{WC}	240		315		ns
$t_{c(TW)}$	Transfer write cycle time‡		240		315		ns
$t_{c(Trd)}$	Transfer read cycle time		240		315		ns
$t_{c(SCLK)}$	Serial-clock cycle time	t_{SCC}	45	50,000	50	50,000	ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (precharge time)§	t_{CP}	50		80		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low	t_{CAS}	100	10,000	135	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge time)	t_{RP}	80		105		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low	t_{RAS}	150	10,000	200	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	45		45		ns
$t_{w(CKL)}$	Pulse duration, SCLK low		10		10		ns
$t_{w(CKH)}$	Pulse duration, SCLK high		12		12		ns
$t_{w(QE)}$	$\overline{TR}/\overline{QE}$ pulse duration low time (read cycle)		40		40		ns
t_t	Transition times (rise and fall) $\overline{RAS}$, $\overline{CAS}$, and SCLK	t_T	3	50	3	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		0		ns
$t_{su(RW)}$	$\overline{W}$ setup time before $\overline{RAS}$ low with $\overline{TR}/\overline{QE}$ low		0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		0		ns
$t_{su(WCL)}$	Early write-command setup time before $\overline{CAS}$ low	t_{WCS}	−5		−5		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	40		60		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	40		60		ns
$t_{su(TR)}$	$\overline{TR}/\overline{QE}$ setup time before $\overline{RAS}$ low		0		0		ns
$t_{su(SI)}$	Serial-data setup time before SCLK high		6		6		ns
$t_{h(SI)}$	Serial-data-in hold time after SCLK high		3		3		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	45		55		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	20		25		ns
$t_{h(RW)}$	$\overline{W}$ hold time after $\overline{RAS}$ low with $\overline{TR}/\overline{QE}$ low		20		20		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	95		120		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	60		80		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	110		145		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	45		55		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		ns

(Continued next page.)

NOTE 5: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, V_{IL} max and V_{IH} min must be met at the 10% and 90% points.

†All cycle times assume t_t = 5 ns except $t_{c(SCLK)}$ which assumes t_t = 3 ns.

‡Multiple transfer write cycles require separation by either a 500 ns $\overline{RAS}$-precharge interval or any other active $\overline{RAS}$-cycle.

§Page-mode only.

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timing requirements over recommended supply voltage range and operating free-air temperature range (concluded)

		ALT. SYMBOL	TM4161EV4-15		TM4161EV4-20		UNIT
			MIN	MAX	MIN	MAX	
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	5		5		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	60		80		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	110		145		ns
$t_{h(RSO)}$	Serial-data-out hold time after $\overline{RAS}$ low with $\overline{TR}/\overline{QE}$ low		30		30		ns
$t_{h(SO)}$	Serial-data-out hold time after SCLK high		8		8		ns
$t_{h(TR)}$	$\overline{TR}/\overline{QE}$ hold time after $\overline{RAS}$ low (transfer)		20		20		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	150		200		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
t_{CLQEH}	Delay time, $\overline{CAS}$ low to $\overline{QE}$ high		100		135		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	100		135		ns
t_{CQE}	Delay time, $\overline{CAS}$ low to $\overline{QE}$ low (maximum value specified only to guarantee $t_{a(QE)}$ access time)			60		85	ns
t_{RHSC}	Delay time, $\overline{RAS}$ high to SCLK high		80	50,000	80	50,000	ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	25	50	30	65	ns
t_{CKRL}	Delay time, SCLK high before $\overline{RAS}$ low with $\overline{TR}/\overline{QE}$ low¶		10	50,000	10	50,000	ns
$t_{rf(MA)}$	Refresh time interval, memory array	t_{REF1}		4		4	ms
$t_{rf(SR)}$	Refresh time interval, shift register#	t_{REF2}		50,000		50,000	ns

NOTE 5: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, V_{IL} max and V_{IH} min must be met at the 10% and 90% points.

¶SCLK may be high or low during $t_{w(RL)}$, but there can not be any positive edge transitions on SCLK for a minimum of 10 ns prior to $\overline{RAS}$ going low with $\overline{TR}/\overline{QE}$ low (i.e., before a transfer cycle).

#See "refresh" on page 5-31.

PARAMETER MEASUREMENT INFORMATION

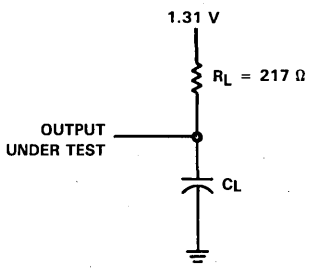
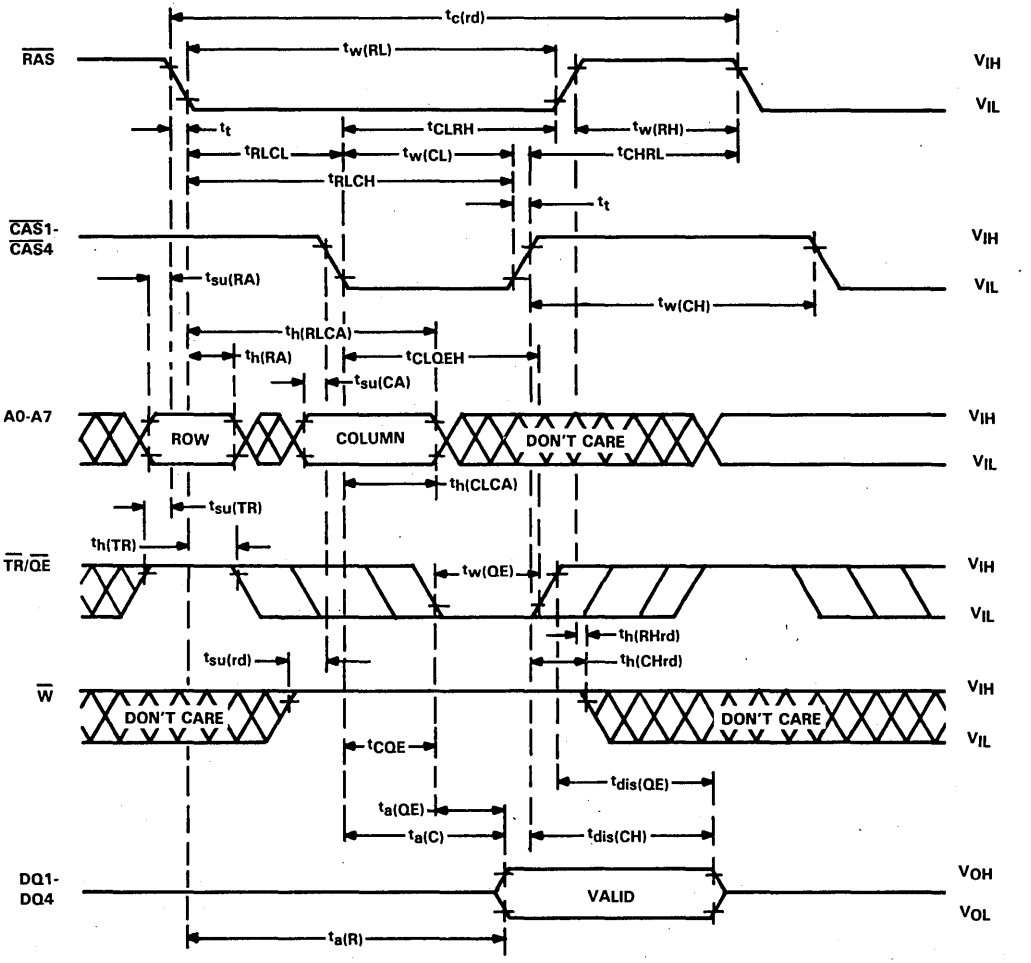


FIGURE 1. LOAD CIRCUIT

read cycle timing



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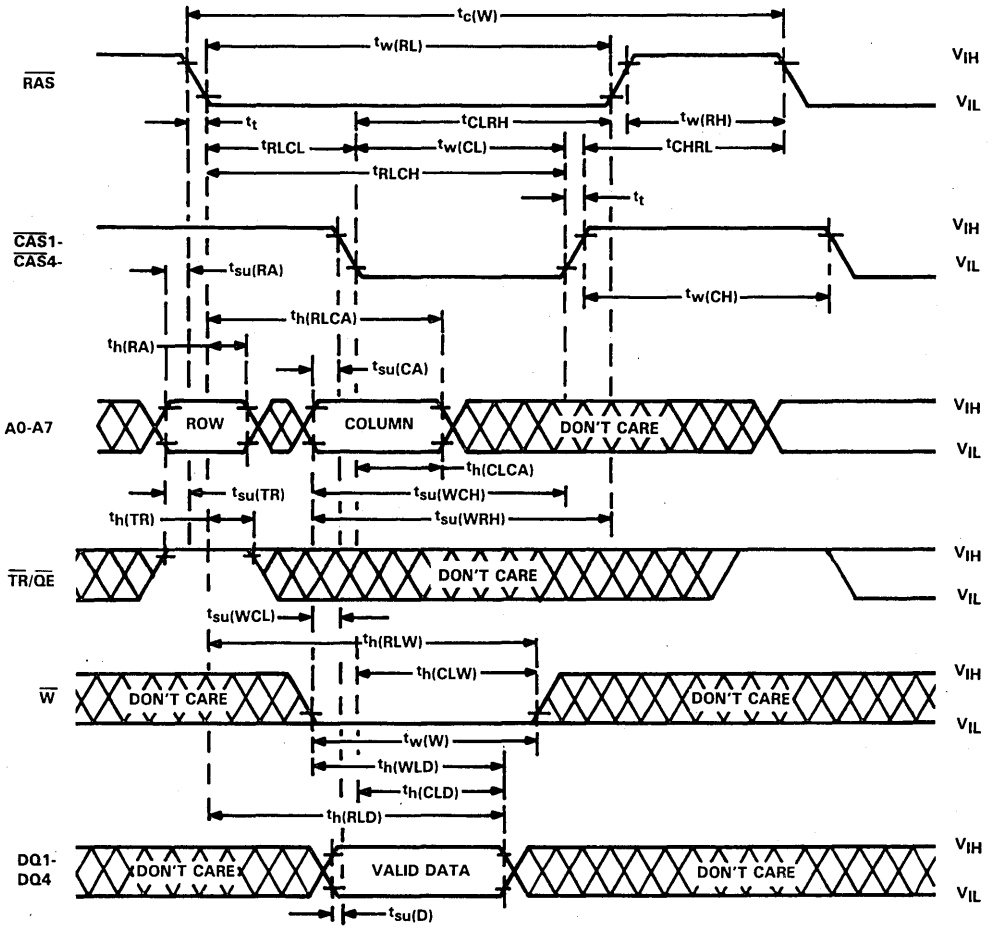
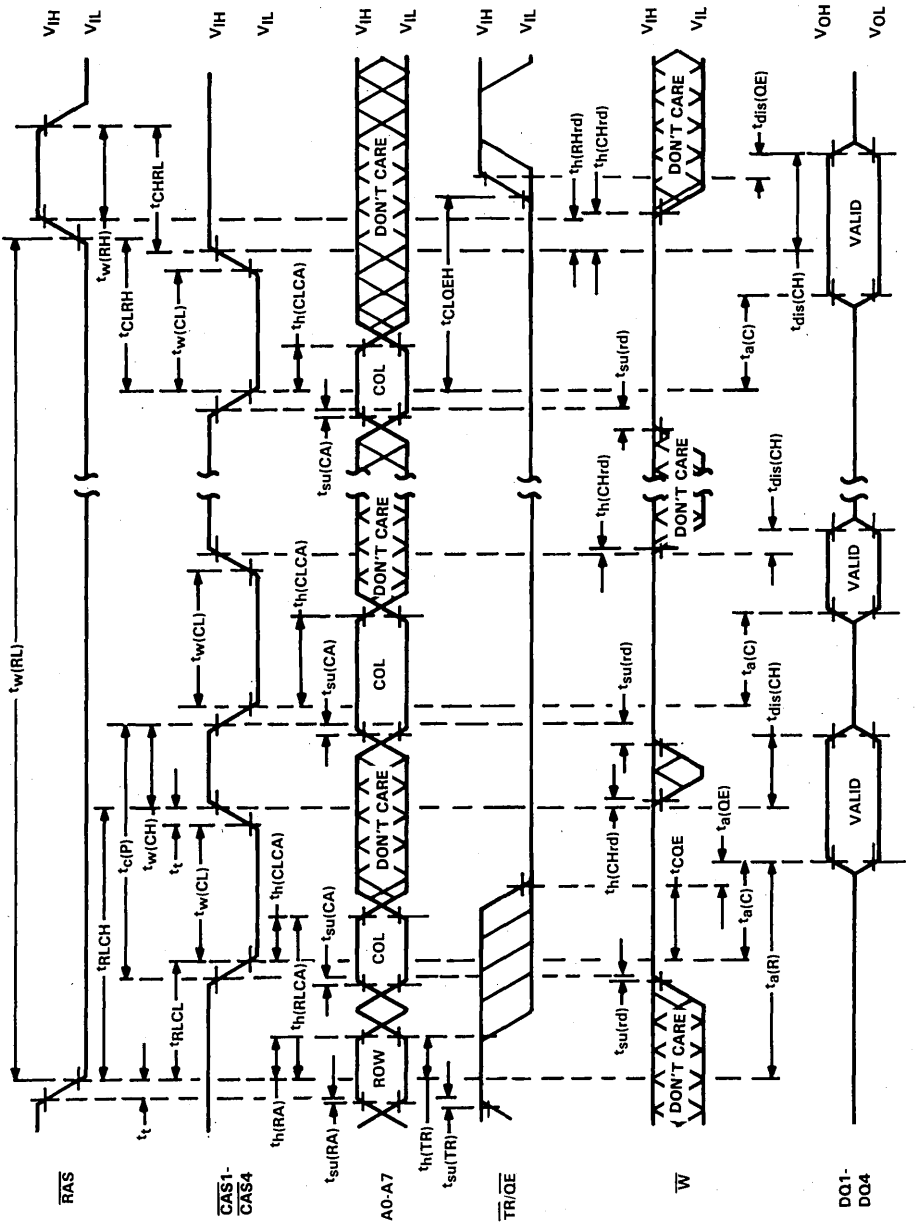
early write cycle timing

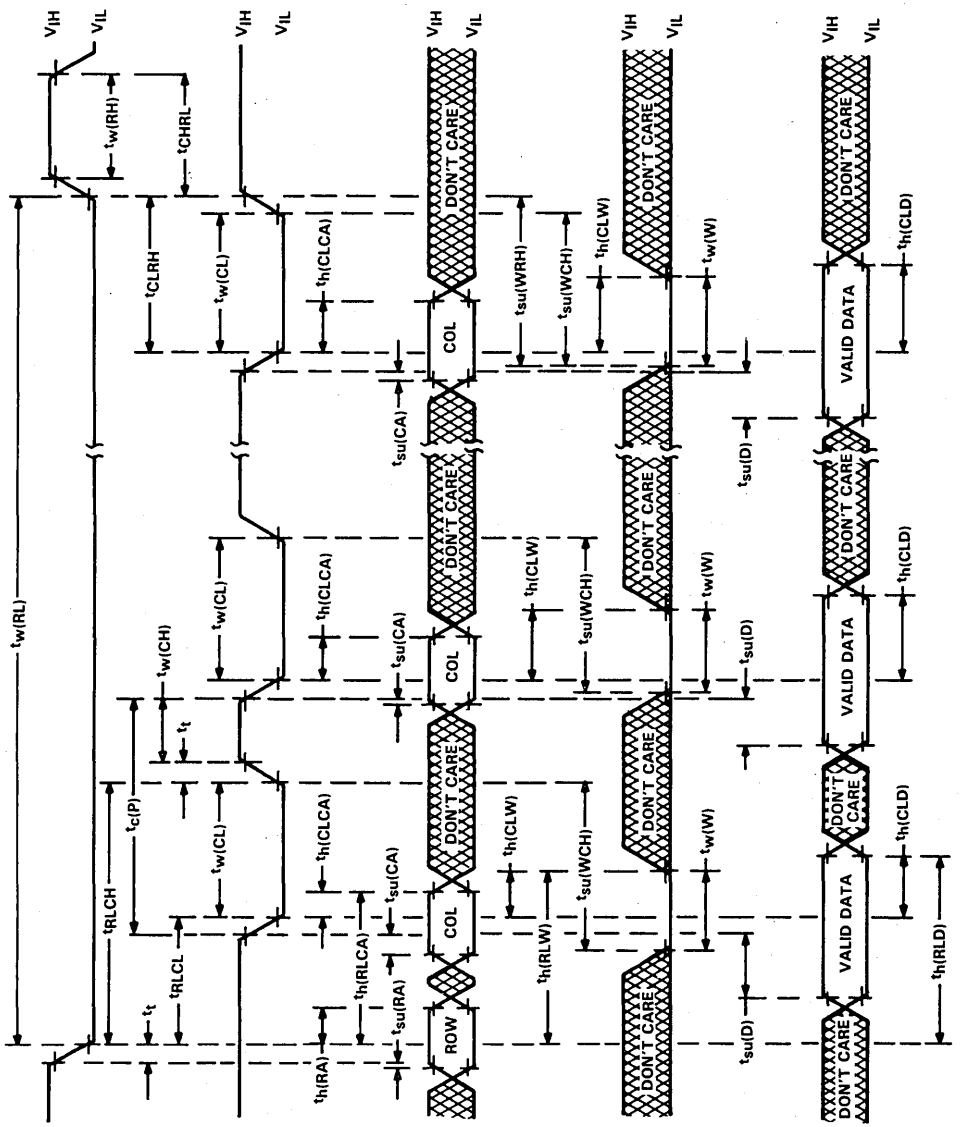


page-mode read cycle timing



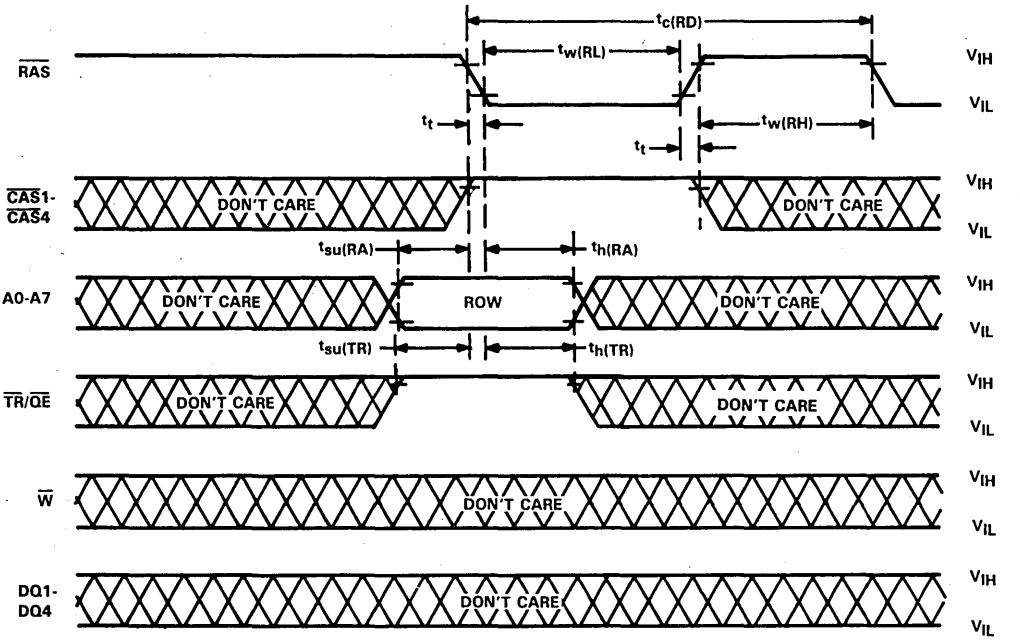
NOTES: 6. Timing is for non-multiplexed DQ and Address lines.
7. A write cycle or a read-modify-write cycle can be intermixed with read cycles as long as the write and read-modify-write timing specifications are not violated.

page-mode write cycle timing



NOTES: 6. Timing is for non-multiplexed DQ and Address lines.
8. A read cycle or a read-modify-write cycle can be intermixed with write cycles as long as the read and read-modify-write timing specifications are not violated.

$\overline{\text{RAS}}$-only refresh timing



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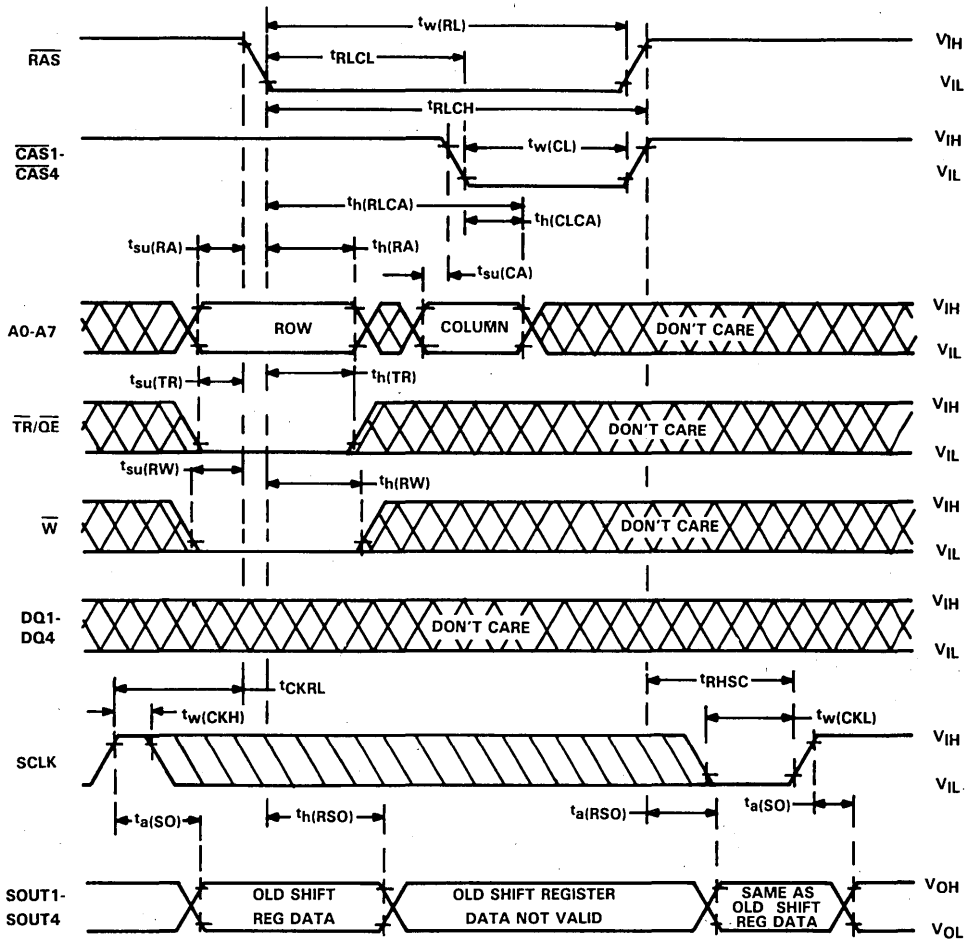
shift register to memory timing

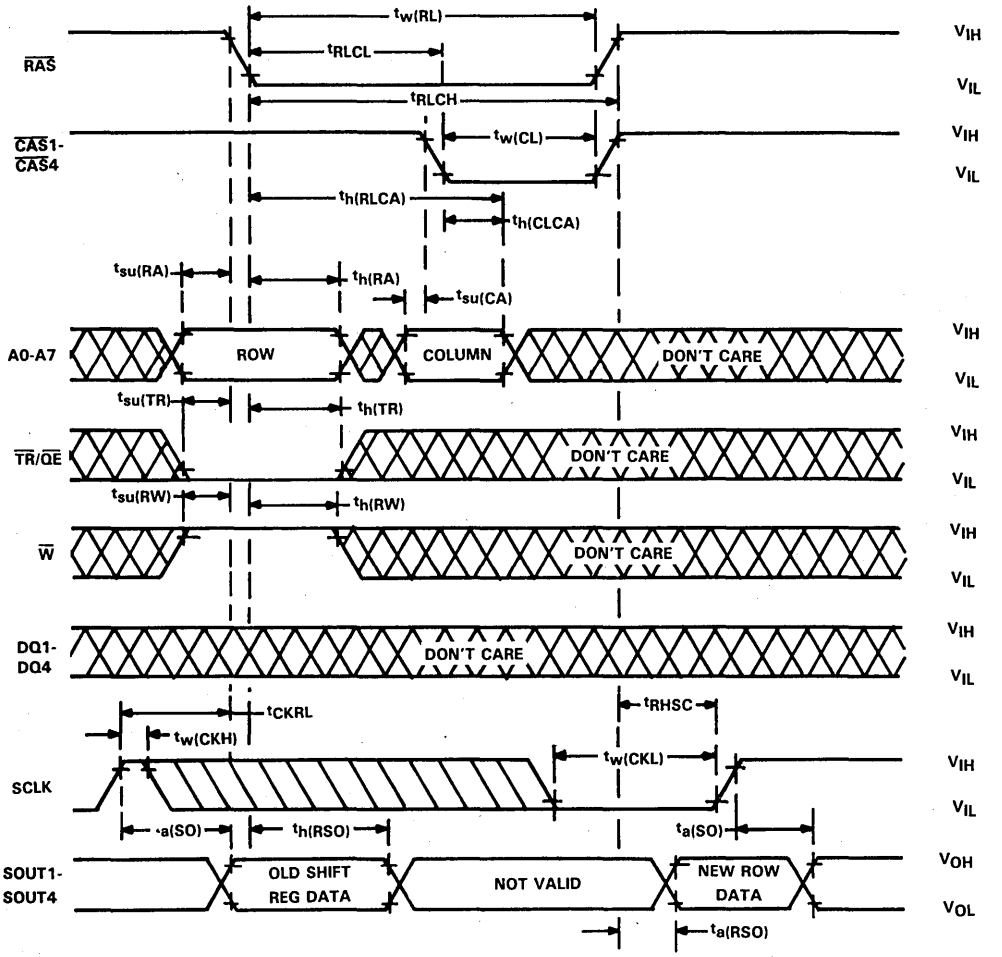


NOTES: 9. The shift register to memory cycle is used to transfer data from the shift registers to the memory array. Every one of the 256 locations in each shift register is written into the 256 columns of the selected row. Note that the data that was in the shift registers may have resulted, either from a serial shift in or from a parallel load of the shift registers from one of the memory array rows.

10. $\overline{SOE}$ assumed low.

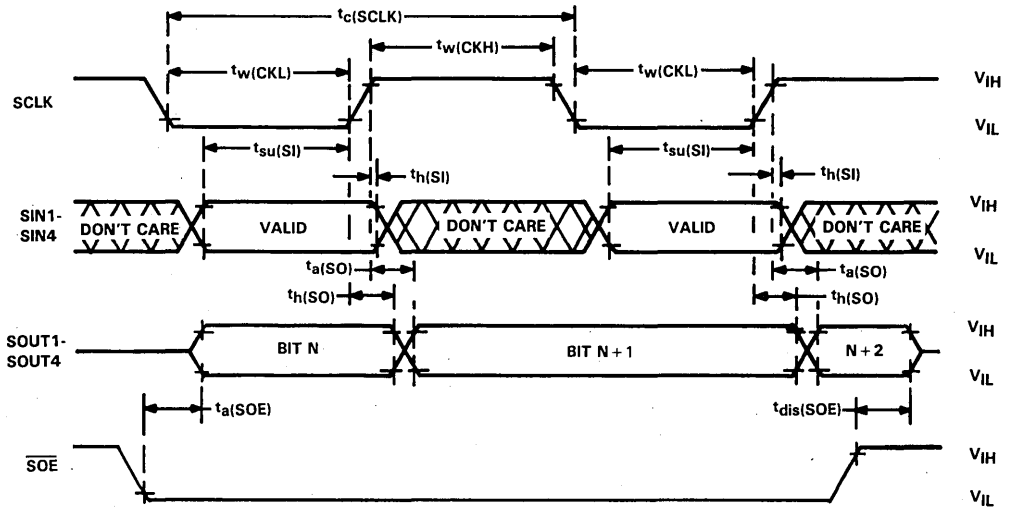
11. SCLK may be high or low during $t_{w(RL)}$.

memory to shift register timing



NOTES: 10. $\overline{SOE}$ assumed low.
11. SCLK may be high or low during $t_{w(RL)}$.
12. The memory to shift register cycle is used to load the shift registers in parallel from the memory array. Every one of the 256 locations in each shift register are written into from the 256 columns of the selected row. Note that the data that is loaded into the shift registers may be either shifted out or written back into another row.

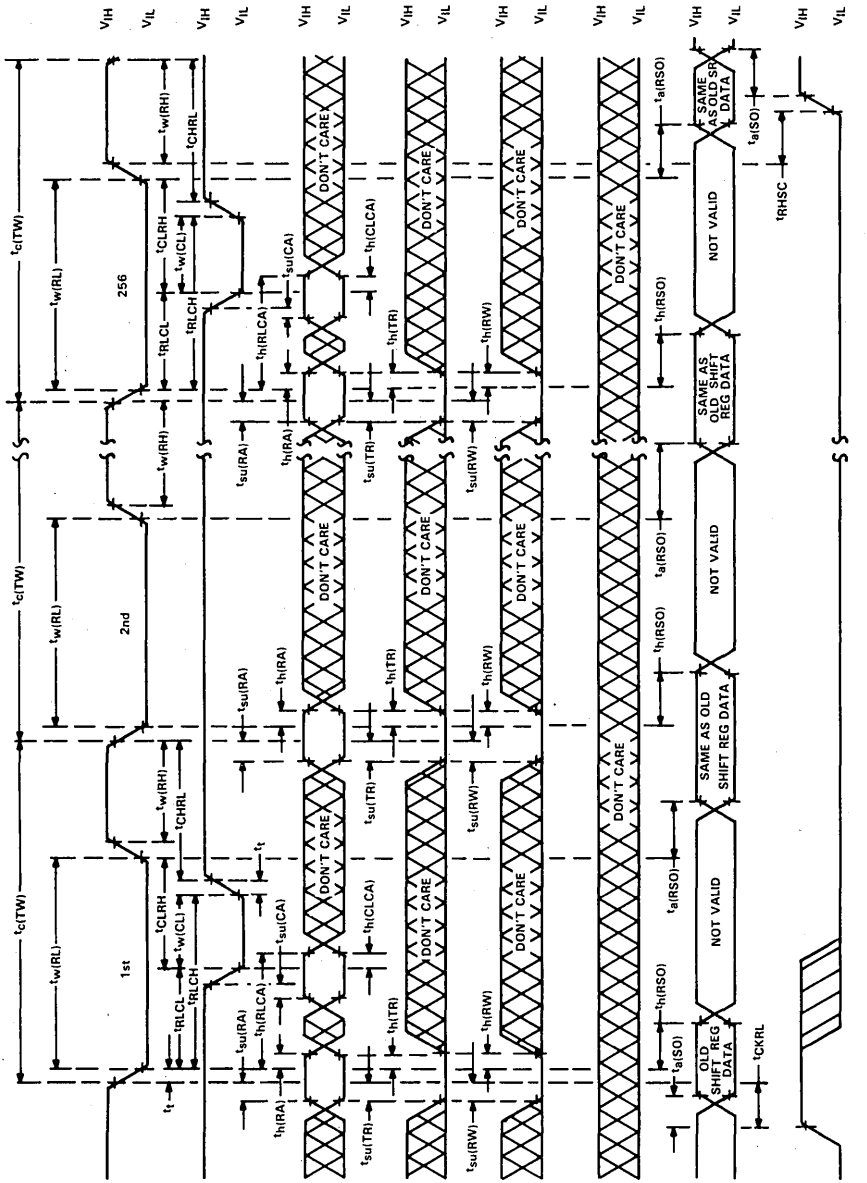
serial data shift timing



NOTES: 13. When loading data into the shift registers from the serial input in preparation for a shift register to memory transfer operation, the serial clock must be clocked an even number of times.

14. While shifting data through the serial registers, the state of $\overline{TR}/\overline{QE}$ is a don't care as long as $\overline{TR}/\overline{QE}$ is held high when $\overline{RAS}$ goes low and $t_{su(TR)}$ and $t_{h(TR)}$ timings are observed. This requirement avoids the initiation of a register-to-memory or memory-to-register data transfer operation. The serial data transfer cycle is used to shift data in and/or out of the shift registers.

shift register to memory multiple timing



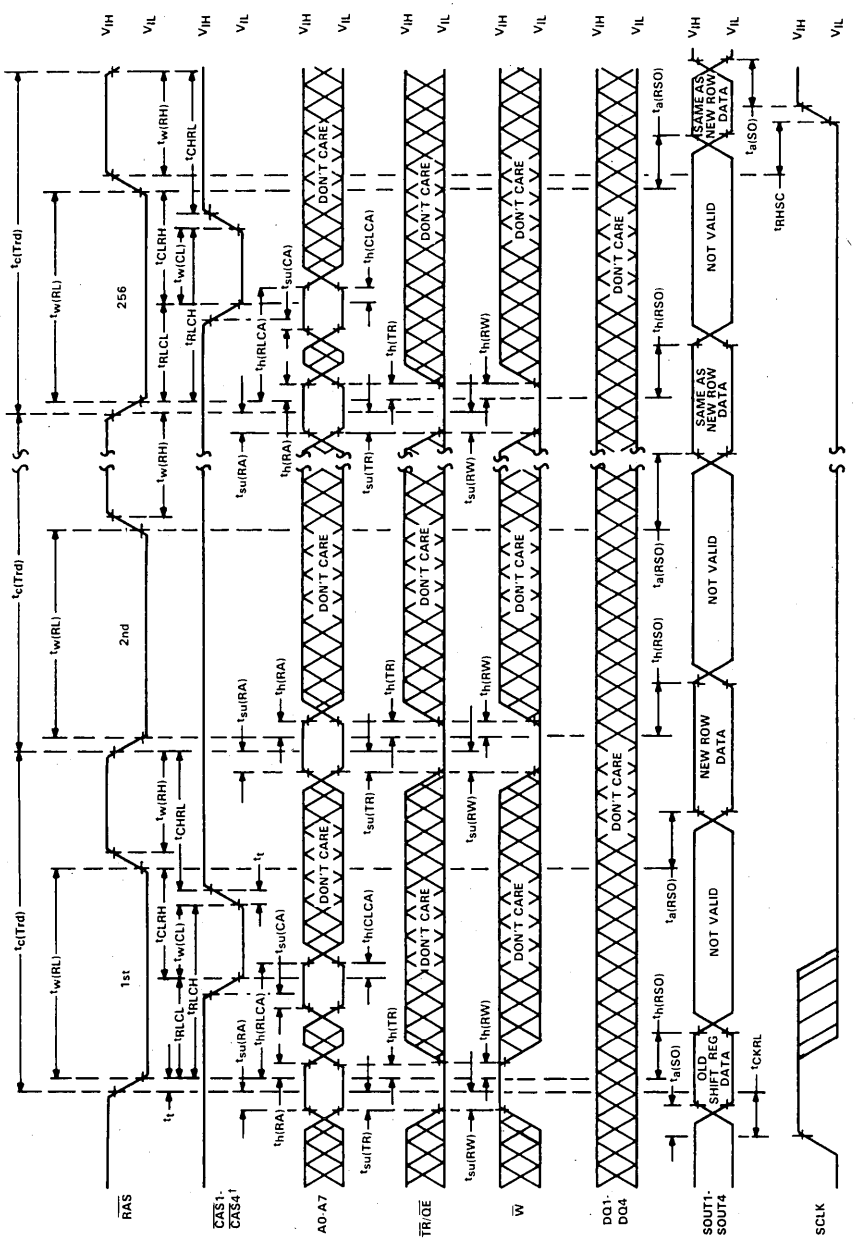
†CAS and register address need not be supplied every cycle, only when it is desired to change or select a new register length.

NOTES: 10. $\overline{SOE}$ assumed low.

15. The shift register to memory multiple cycle is used to write the shift register data to more than one row of the memory array. An application of this could be clearing all memory. To do this, the SIN lines would be held at 0 to fill all locations in the shift registers with 0's. The shift registers would then be written into all 256 rows of the memory array in 256 cycles. The random output port Q will be in a high-impedance state as long as register transfer cycles are selected.

16. SCLK is a don't care except that no positive transitions on SCLK can occur for a period equal to t_{CKRL} prior to $\overline{RAS}$ falling with $\overline{TR}/\overline{QE}$ low.

memory to shift register to memory multiple timing



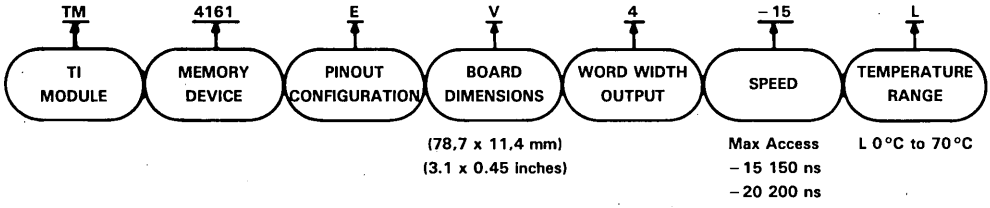
†CAS and register address need not be supplied every cycle, only when it is desired to change from one register address to another.

NOTES: 10. SOE assumed low.

16. SCLK is a don't care except that no positive transitions on SCLK can occur for a period equal to tCKRL prior to RAS falling with TR/OE low.

17. The memory to shift register to memory multiple cycle is used to reorder the rows within the memory array itself. First, the data in a row is stored in the shift register and then it is written into other selected rows. The random output port Q will be in a high-impedance state as long as register transfer cycles are selected.

TI single-in-line package nomenclature



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TM4161GW4, TM4161GY4
65,536 BY 4-BIT DYNAMIC RAM MODULES

NOVEMBER 1985

- 65,536 X 4 Organization
- Single 5-V Supply (10% Tolerance)
- 30-Pin Single-in-Line Package (SIP)
  - —Pinned Version for Through-Hole Insertion (TM4161GY4)
  - —Leadless Version for Use with Sockets (TM4161GW4)
- Utilizes Four Multiport Video RAMs in Plastic Chip Carriers
- Long Refresh Period . . . 4 ms (256 Cycles)
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Outputs
- Performance of Unmounted RAMs:

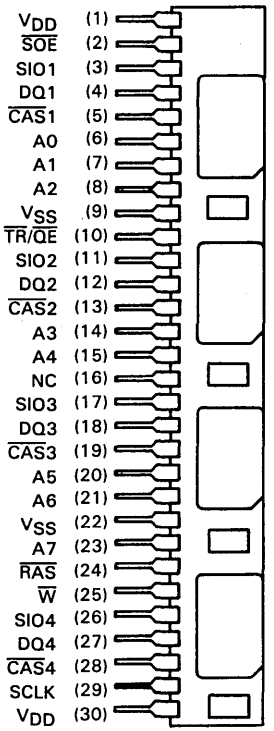
	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	READ-MODIFY-WRITE CYCLE (MIN)
TMS4161-15	150 ns	100 ns	240 ns	265 ns
TMS4161-20	200 ns	135 ns	315 ns	330 ns

- Separate $\overline{CAS}$ Control with Common Data-In and Data-Out Lines
- Low Power Dissipation:

	OPERATING (TYP)	STANDBY (TYP)
TM4161G_4-15	1000 mW	256 mW
TM4161G_4-20	1000 mW	256 mW

- Operating Free-Air Temperature . . . 0°C To 70°C

TM4161GW4 . . . W SINGLE-IN-LINE PACKAGE†
TM4161GY4 . . . Y SINGLE-IN-LINE PACKAGE†
(TOP VIEW)



†TM4161GY4 package is shown.

description

The TM4161G_4 series are 256K dual-access dynamic random-access memory modules organized as 65,536 × 4-bits in a 30-pin single-in-line package. This module is comprised of four TMS4161FML, 65,536 × 1-bit Multiport Video RAMs in 22-lead plastic chip carriers mounted on top of a substrate together with four decoupling capacitors. Each TMS4161FML is described in the TMS4161 data sheet and is fully electrically tested and processed according to TI's MIL-STD-883B (as amended for commercial applications) flows prior to assembly. After assembly onto the substrate, a further set of electrical tests is performed. The TM4161G_4 is rated for operation from 0°C to 70°C.

PIN NOMENCLATURE	
A0-A7	Address Inputs
$\overline{CAS}$1-$\overline{CAS}$4	Column-Address Strobes
DQ1-DQ4	Random-Access Data In/Data Out
NC	No Connection
$\overline{RAS}$	Row-Address Strobe
SCLK	Serial Data Clock
SIO1-SIO4	Serial-Access Data In/Data Out
$\overline{SOE}$	Serial Output Enable
$\overline{TR/QE}$	Register Transfer/Q Output Enable
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

operation

The TM4161G_4 operates as four TMS4161's connected as shown in the functional block diagram. Refer to the TMS4161 data sheet for details of its operation.

specifications

For TMS4161 electrical specifications, refer to the TMS4161 data sheet.

single-in-line package components

PC substrate: TM4164GY4 . . . 0,79 mm (0.031 inch) minimum thickness
TM4161GW4 . . . 1,35 mm (0.053 inch) maximum thickness
Bypass capacitors: Multilayer ceramic
Leads: Tin/lead solder coated over phosphor-bronze
Contact area for socketable devices: Nickel plate and solder plate on top of copper

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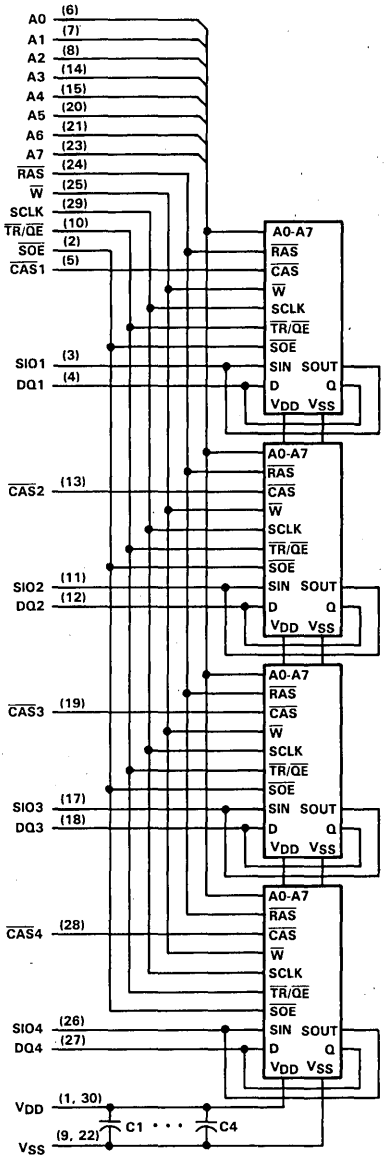
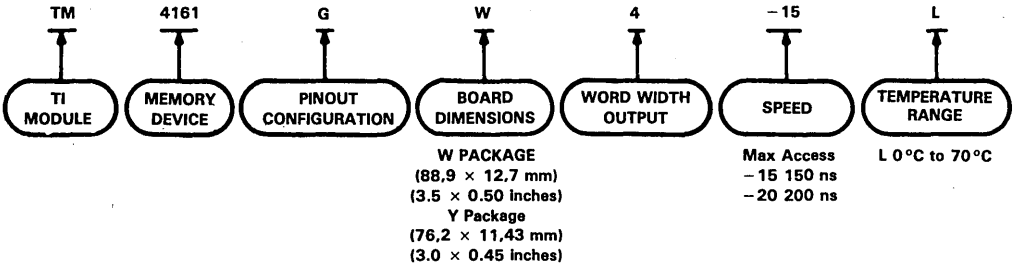
functional block diagram



TI single-in-line package nomenclature



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NOVEMBER 1983 – REVISED NOVEMBER 1985

- 65,536 X 4 Organization
- Single 5-V Supply (10% Tolerance)
- 22-Pin Single-in-Line Package (SIP)
- Utilizes Four 64K Dynamic RAMs in Plastic Chip Carrier
- Long Refresh Period . . . 4 ms (256 cycles)
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Outputs
- Performance Ranges:

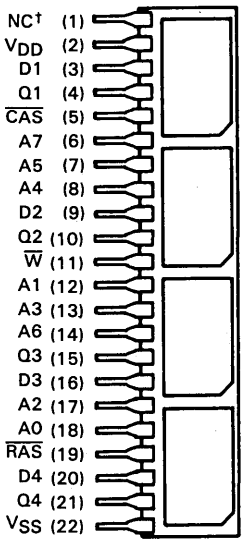
	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	READ-MODIFY-WRITE CYCLE (MIN)
TM4164EC4-12	120 ns	75 ns	230 ns	260 ns
TM4164EC4-15	150 ns	90 ns	260 ns	285 ns
TM4164EC4-20	200 ns	135 ns	326 ns	345 ns

- Common $\overline{CAS}$ Control with Separate Data-In and Data-Out Lines with an "Early Write" Feature
- Low Power Dissipation:

	OPERATING (TYP)	STANDBY (TYP)
TM4164EC4-12	800 mW	70 mW
TM4164EC4-15	700 mW	70 mW
TM4164EC4-20	540 mW	70 mW

- Operating Free-Air Temperature . . . 0°C to 70°C
- Upward Compatible with 256K X 4 Single-In-Line Package

SINGLE-IN-LINE PACKAGE
(TOP VIEW)



†Reserved for A8 on TM4256EC4

PIN NOMENCLATURE	
A0-A7	Address Inputs
$\overline{CAS}$	Column-Address Strobe
D1-D4	Data Inputs
NC	No Connection
Q1-Q4	Data Outputs
$\overline{RAS}$	Row-Address Strobe
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The TM4164EC4 is a 256K, dynamic random-access memory module organized as 65,536 × 4 bits in a 22-pin single-in-line package comprising four TMS4164FPL, 65,536 × 1 bit dynamic RAM's in 18-lead plastic chip carriers mounted on top of a substrate together with four 0.1 μF decoupling capacitors. The onboard capacitors eliminate the need for bypassing on the motherboard and offer superior performance over equivalent leaded capacitors due to reduced lead inductance. Also, with 0.3 inch board spacing the TM4164EC4 has a density of six devices per square inch (approximately 2.4X the density of DIPs). With the elimination of bypass capacitors on the motherboard, reduced PC board size, and fewer plated-through holes, a cost savings can be realized.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address lines and data in are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TM4164EC4 is rated for operation from 0°C to 70°C.

upward compatibility

Future 256K × 4 memory modules in single-in-line packages will have identical pin functions and spacing, and will be directly upward compatible. Pin 1 of the TM4256EC4 (256K X 4 SIP) module will be memory address A8.

operation

address (A0 through A7)

Sixteen address bits are required to decode 1 of 65,536 storage cell locations on each of the four chips. Eight row-address bits are set up on pins A0 through A7 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the eight column-address bits are set up on Pins A0 through A7 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data inputs are disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$, the data-outs will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data in (D1-D4)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. This latch can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data out (Q1-Q4)

The three-state output buffers provide direct TTL compatibility (no pull-up resistor required) with a fan out of two Series 74 TTL loads for each output. Data out is the same polarity as data in. The outputs are in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the outputs go active after the access time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ is satisfied. The outputs become valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low; $\overline{CAS}$ going high returns them to a high-impedance state. In an early write cycle, the outputs are always in the high-impedance state. In a delayed-write or read-modify-write cycle, the outputs will follow the sequence for the read cycle.

refresh

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffers are in the high-impedance state unless $\overline{CAS}$ is applied, the $\overline{RAS}$-only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses (A0 through A7) with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power.

page mode

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the module. Thus, the time required to setup and strobe sequential row addresses for the same page is eliminated. To extend beyond the 256 column locations on a single module, the row address and $\overline{RAS}$ are applied to multiple modules. $\overline{CAS}$ is then decoded to select the proper module.

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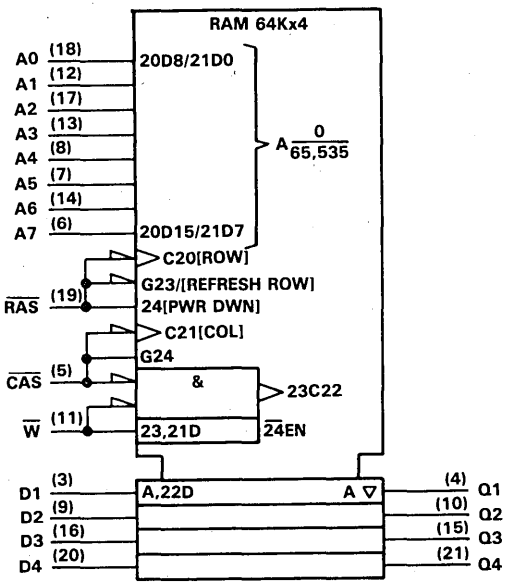
power up

After power up, the power supply must remain at its steady-state value for 1 ms. In addition, $\overline{RAS}$ must remain high for 100 μs immediately prior to initialization. Initialization consists of performing eight $\overline{RAS}$ cycles before proper device operation is achieved.

single-in-line package and components

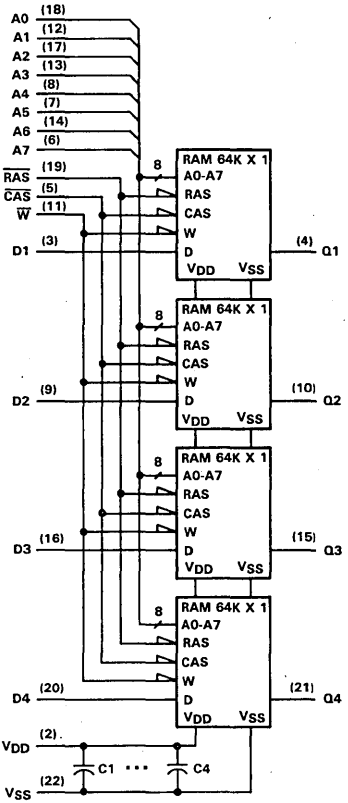
PC substrate: 0,79 mm (0.031 inch) minimum thickness
Bypass capacitors: Multilayer ceramic
Leads: Tin/lead solder coated over phosphor-bronze

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin except V_{DD} and data out (see Note 1) . . . . . −1.5 V to 10 V
Voltage range on V_{DD} supply and data out with respect to V_{SS} . . . . . −1 V to 6 V
Short circuit output current for any output . . . . . 50 mA
Power dissipation . . . . . 4 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		4.5	5	5.5	V
V_{SS}	Supply voltage			0		V
V_{IH}	High-level input voltage	V_{DD} = 4.5 V	2.4		4.8	V
		V_{DD} = 5.5 V	2.4		6	
V_{IL}	Low-level input voltage (see Notes 2 and 3)		−0.6		0.8	V
T_A	Operating free-air temperature		0		70	°C

NOTES: 2. The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

3. Due to input protection circuitry, the applied voltage may begin to clamp at −0.6 V. Test conditions should comprehend this occurrence. See application report entitled "TMS4164A and TMS4416 Input Protection Diode" on page 9-5.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TM4164EC4-12			TM4164EC4-15			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4			2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4			0.4	V
I_I	Input current (leakage)	V_I=0 V to 5.8 V, V_{DD}=5 V, All other pins = 0 V			±10			±10	μA
I_O	Output current (leakage)	V_O = 0.4 to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10			±10	μA
I_{DD1}	Average operating current during read or write cycle	t_c = minimum cycle, All outputs open		160	192		140	180	mA
I_{DD2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, All outputs open,		14	20		14	20	mA
I_{DD3}	Average refresh current	t_c = minimum cycle, $\overline{CAS}$ high and $\overline{RAS}$ cycling, All outputs open		112	160		100	148	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low and $\overline{CAS}$ cycling, All outputs open		112	160		100	148	mA

†All typical values are at T_A = 25°C and nominal supply voltages.

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electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TM4164EC4-20			UNIT
			MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 5.8 V, V_{DD} = 5 V, All other pins = 0 V			±10	μA
I_O	Output current (leakage)	V_O = 0.4 to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10	μA
I_{DD1}	Average operating current during read or write cycle	t_c = minimum cycle, All outputs open		108	148	mA
I_{DD2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, All outputs open		14	20	mA
I_{DD3}	Average refresh current	t_c = minimum cycle, $\overline{CAS}$ high and $\overline{RAS}$ cycling, All outputs open		80	128	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low and $\overline{CAS}$ cycling, All outputs open		80	128	mA

† All typical values are at T_A = 25°C and nominal supply voltages.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

PARAMETER		MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs	20	pF
$C_{i(D)}$	Input capacitance, data input	5	pF
$C_{i(RC)}$	Input capacitance, strobe inputs	32	pF
$C_{i(W)}$	Input capacitance, write enable input	32	pF
C_o	Output capacitance	6	pF

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TM4164EC4-12		TM4164EC4-15		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		75		90	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, Load = 2 Series 74 TTL gates	t_{RAC}		120		150	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	40	0	40	ns

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TM4164EC4-20		UNIT
				MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 100 pF Load = 2 Series 74 TTL gates	t_{CAC}		135	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX,* Load = 2 Series 74 TTL gates	t_{RAC}		200	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	50	ns

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timing requirements over recommended supply voltage range and operating free-air temperature range

		ALT. SYMBOL	TM4164EC4-12		TM4164EC4-15		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(P)}$	Page-mode cycle time	t_{PC}	130		160		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	230		260		ns
$t_{c(W)}$	Write cycle time	t_{WC}	230		260		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	260		285		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (precharge time)‡	t_{CP}	50		50		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low§	t_{CAS}	75	10,000	90	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge time)	t_{RP}	80		100		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low¶	t_{RAS}	120	10,000	150	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	40		45		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	5	50	5	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	50		50		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	50		50		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	40		45		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	20		25		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	85		105		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DHC}	45		50		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	90		100		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DHW}	45		50		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	5		5		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	45		50		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	90		100		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	120		150		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	60		100		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{CWD}	50		60		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	25	45	30	60	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{RWD}	110		120		ns
t_{WLCL}	Delay time, $\overline{W}$ low to $\overline{CAS}$ low (early write cycle)	t_{WCS}	0		0		ns
t_{rf}	Refresh time interval	t_{REF}		4		4	ms

NOTE 4: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, V_{IL} max and V_{IH} min must be met at the 10% and 90% points.

†All cycle times assume t_t = 5 ns.

‡Page mode only.

§In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$). This applies to page mode read-modify-write also.

¶In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).

timing requirements over recommended supply voltage range and operating free-air temperature range

		ALT. SYMBOL	TM4164EC4-20 MIN	TM4164EC4-20 MAX	UNIT
$t_{c(P)}$	Page-mode cycle time	t_{PC}	206		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	326		ns
$t_{c(W)}$	Write cycle time	t_{WC}	326		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	345		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (precharge time)‡	t_{CP}	80		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low§	t_{CAS}	135	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge time)	t_{RP}	120		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low¶	t_{RAS}	200	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	55		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	60		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	60		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	55		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	30		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	120		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DHC}	60		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	125		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DHW}	60		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	5		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	60		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	145		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	200		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	135		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{CWD}	65		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	35	65	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{RWD}	130		ns
t_{WLCL}	Delay time, $\overline{W}$ low to $\overline{CAS}$ low (early write cycle)	t_{WCS}	0		ns
t_{rf}	Refresh time interval	t_{REF}		4	ms

NOTE 4: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, V_{IL} max and V_{IH} min must be met at the 10% and 90% points.

†All cycles times assume t_t = 5 ns.

‡Page mode only.

§In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$). This applies to page mode read-modify-write also.

¶In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).

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PARAMETER MEASUREMENT INFORMATION

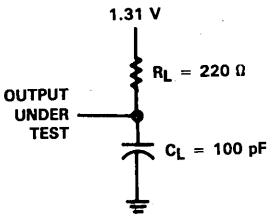
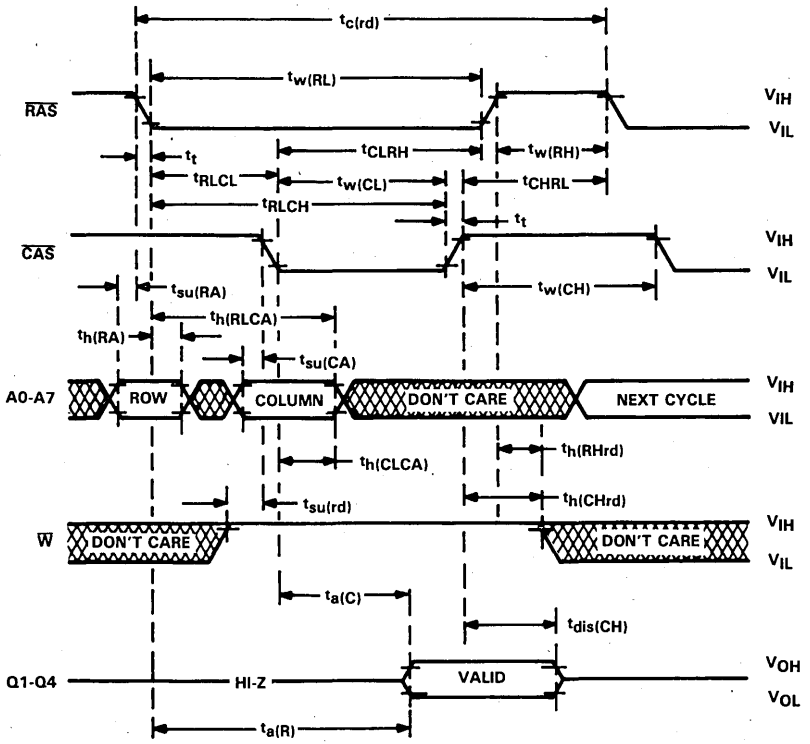
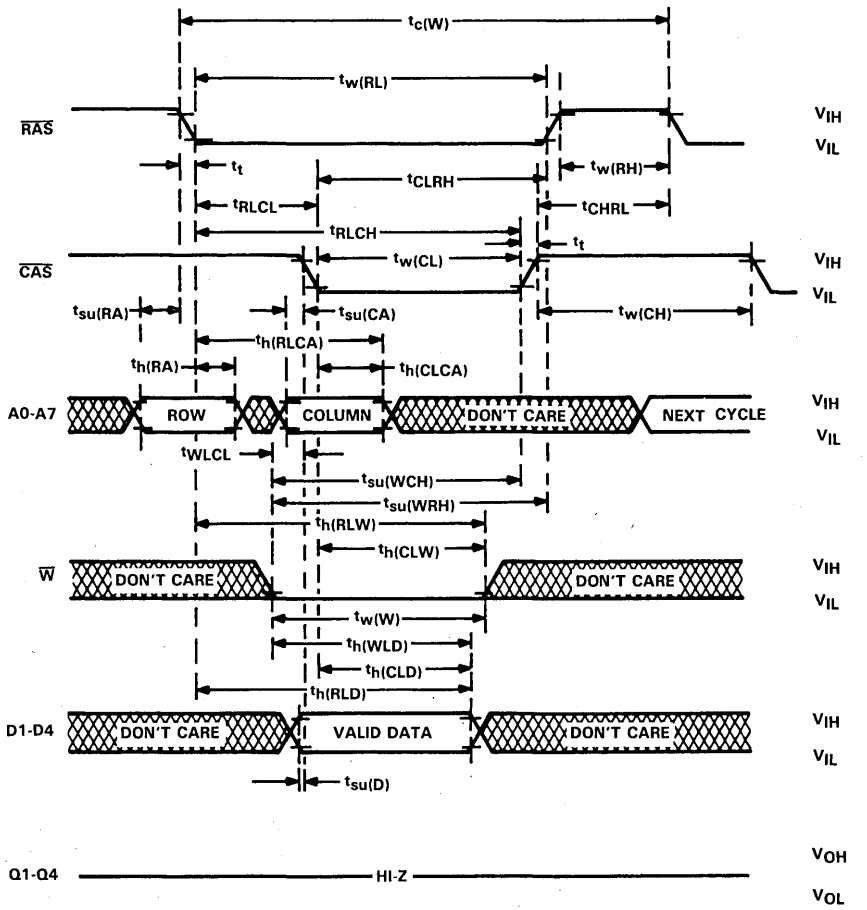


FIGURE 1. LOAD CIRCUIT

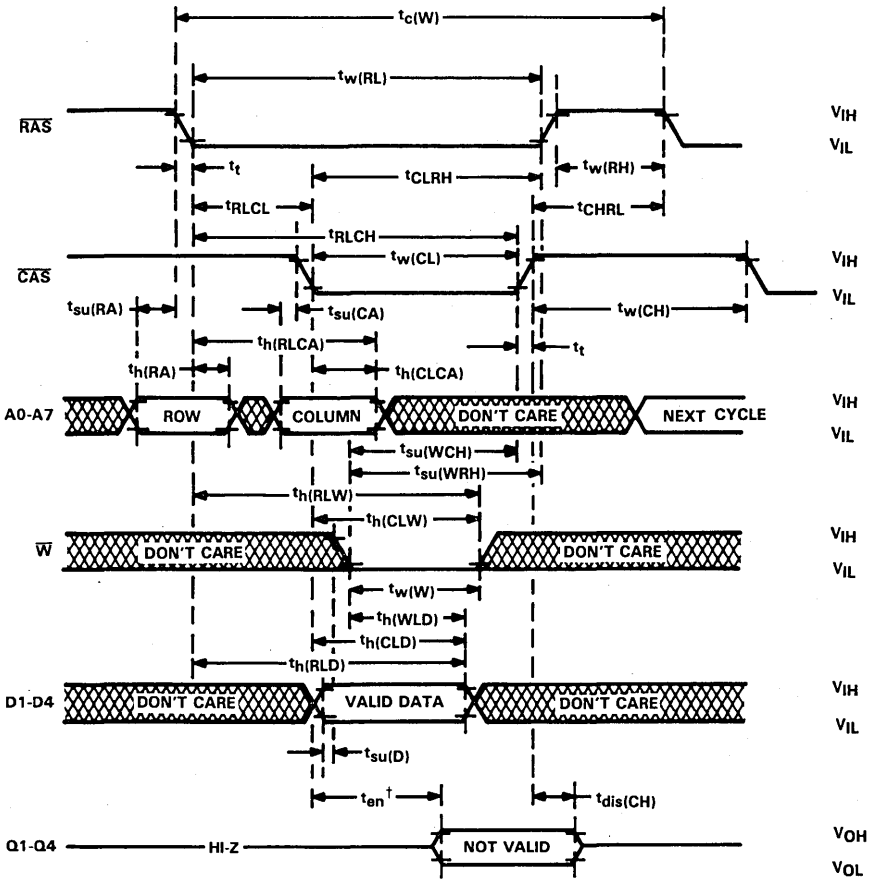
read cycle timing



early write cycle timing

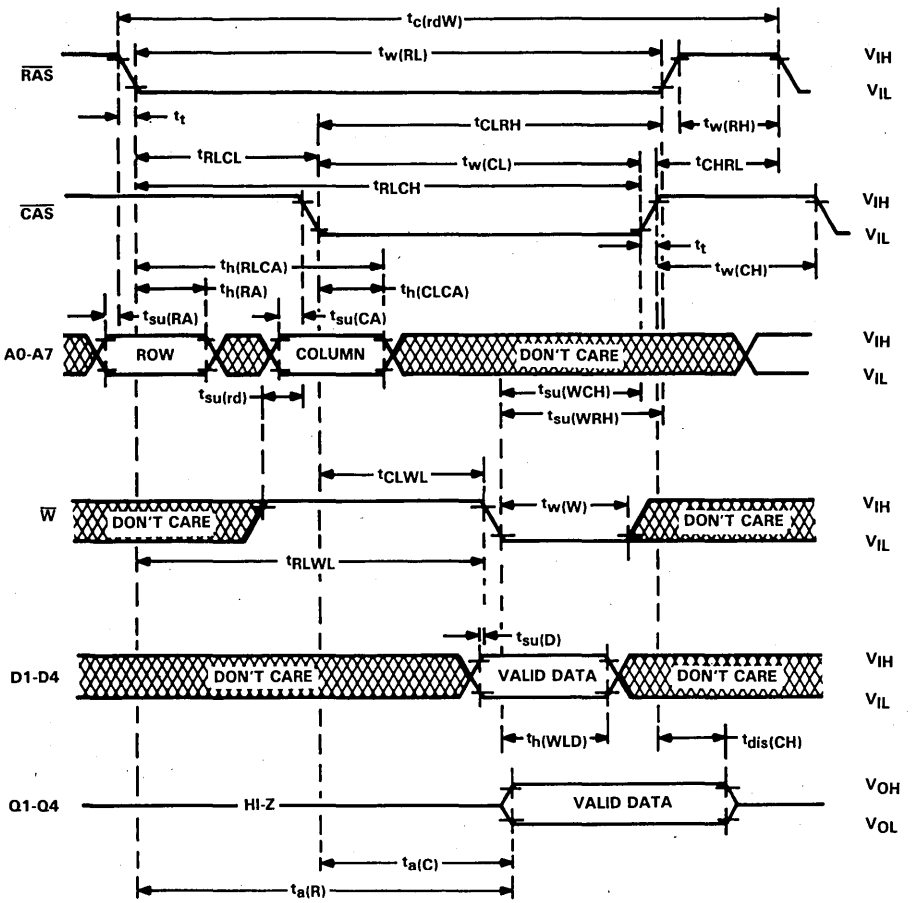


write cycle timing

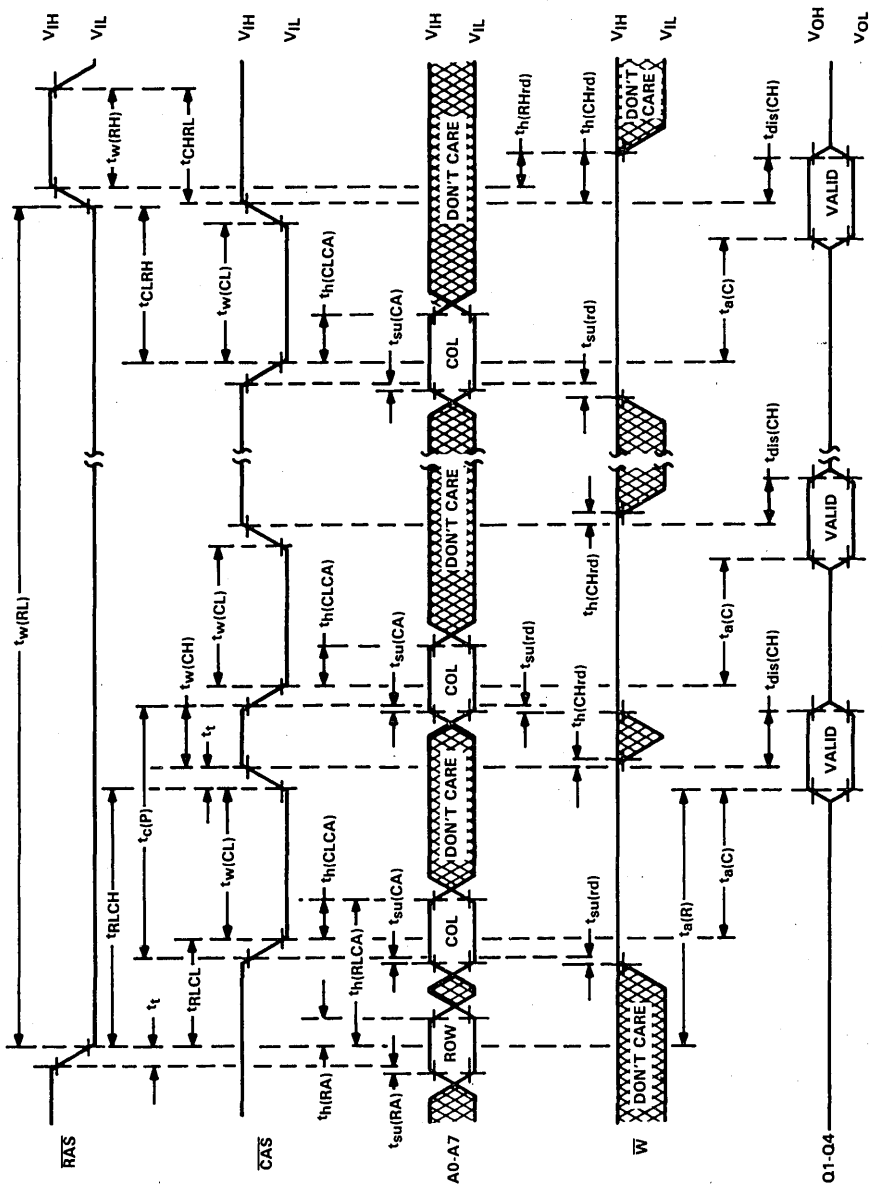


† The enable time (t_{en}) for a write cycle is equal in duration to the access time from $\overline{CAS}$ ($t_{a(C)}$) in a read cycle; but the active levels at the output are invalid.

read-write/read-modify-write cycle timing

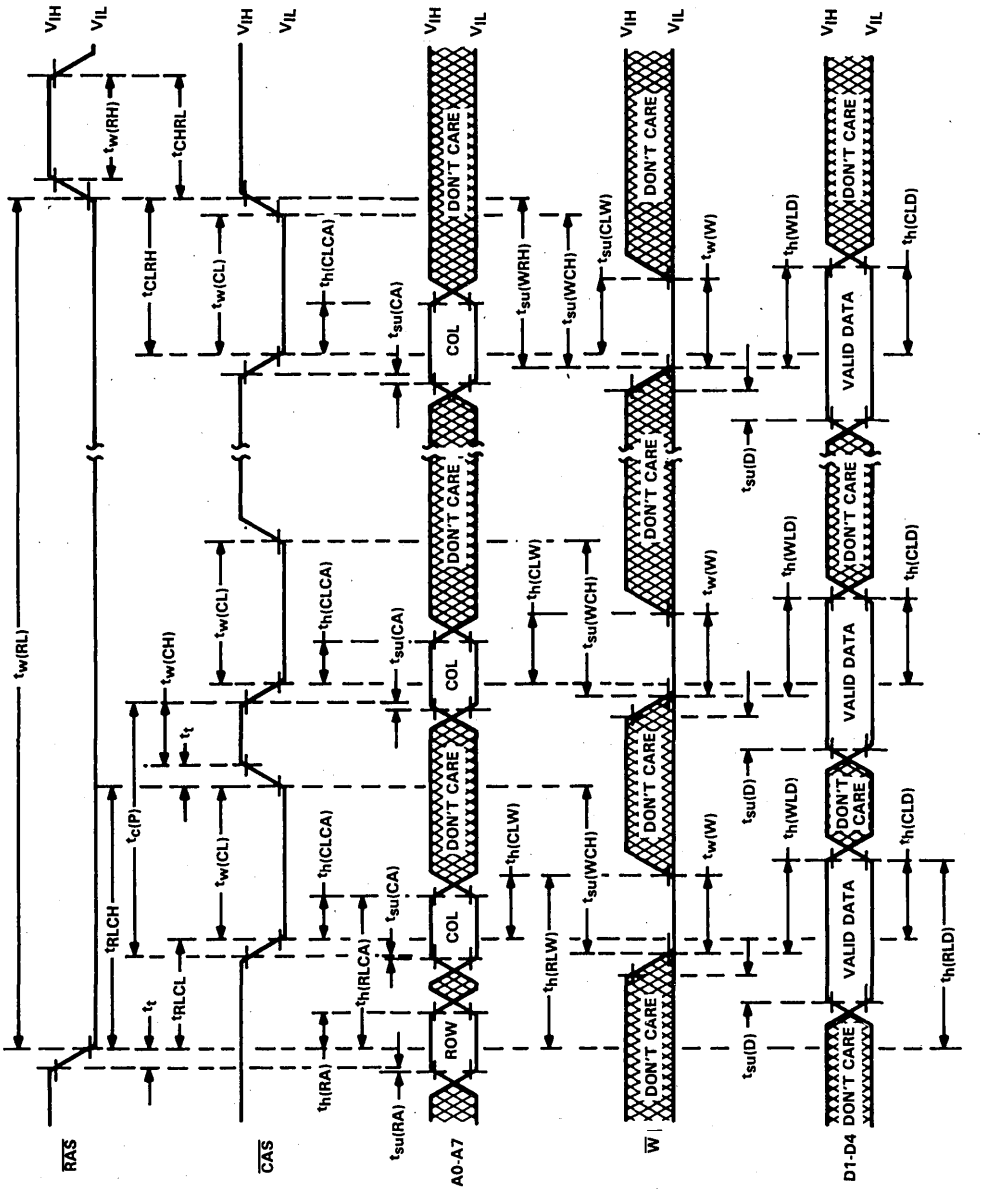


page-mode read cycle timing



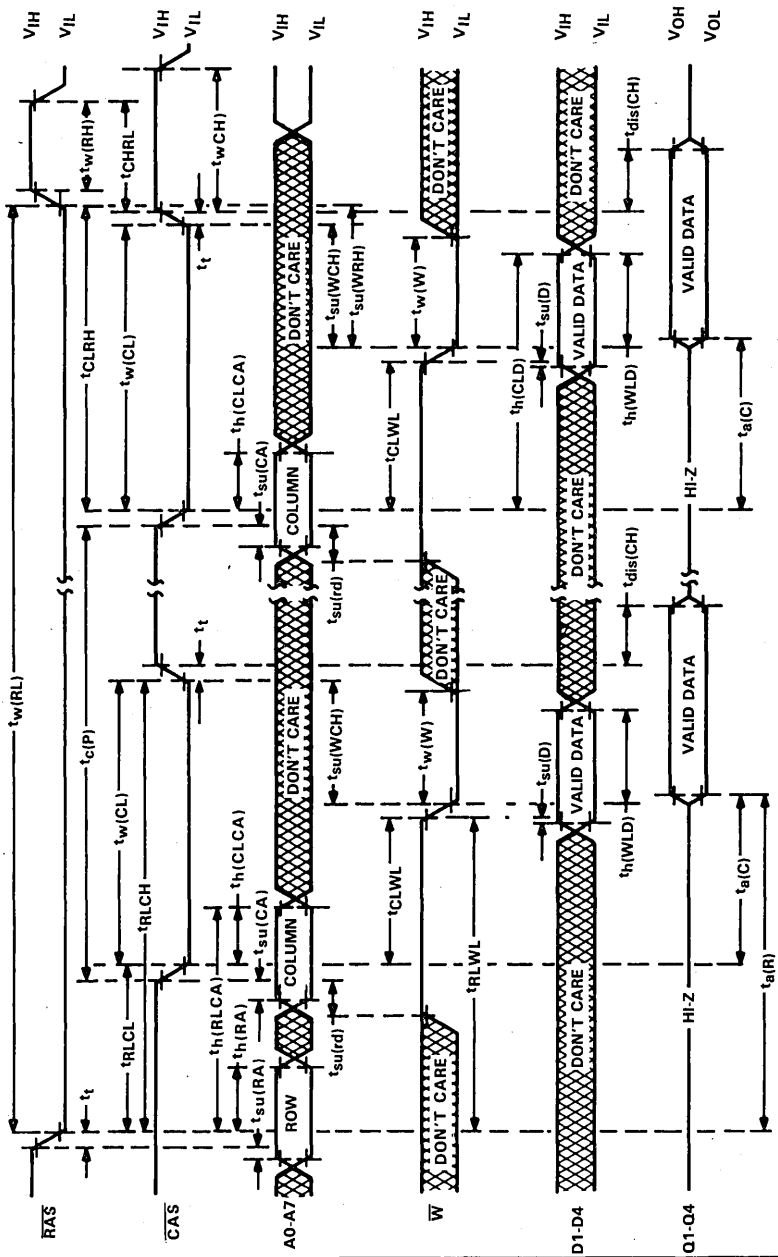
NOTE 5: A write cycle or a read-modify-write cycle can be intermixed with read cycles as long as the write and ready-modify-write timing specifications are not violated.

page-mode write cycle timing



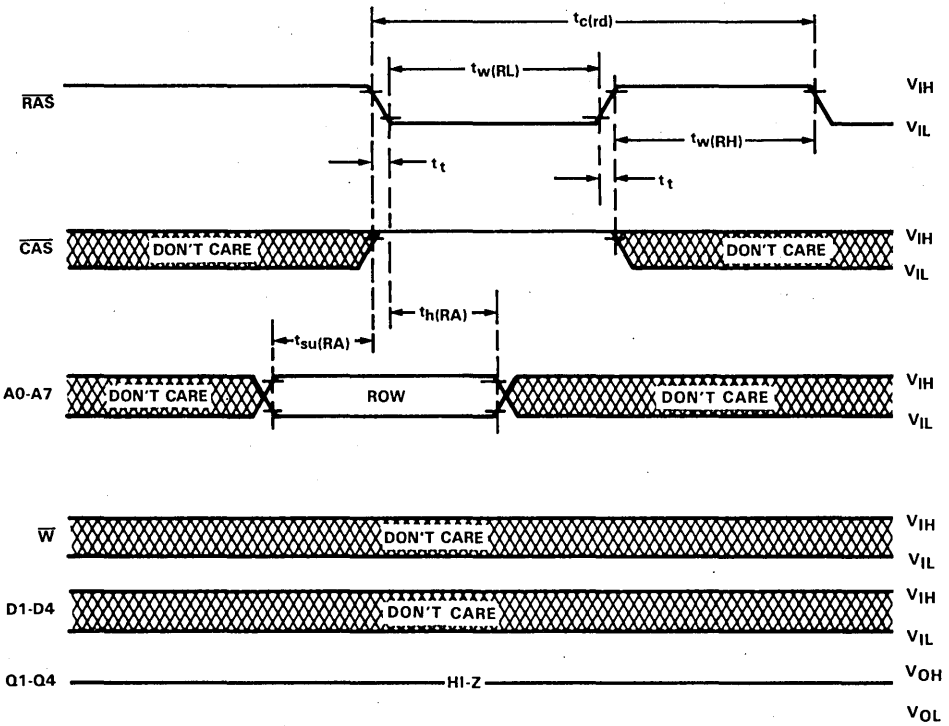
NOTE 6: A read cycle or a read-modify-write cycle can be intermixed with write cycles as long as read and read-modify-write timing specifications are not violated.

page-mode read-modify-write cycle timing

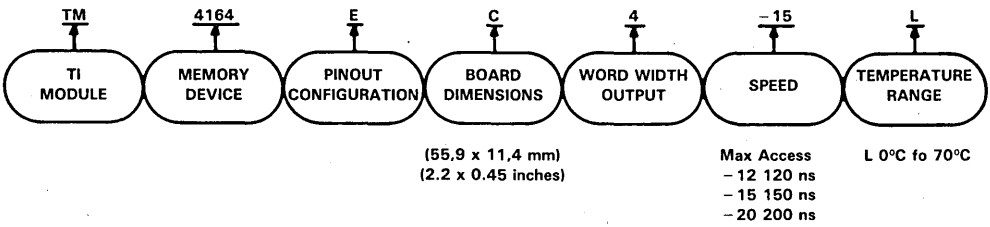


NOTE 7: A read or a write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

$\overline{\text{RAS}}$-only refresh timing



TI single-in-line package nomenclature



NOVEMBER 1983 — REVISED NOVEMBER 1985

- 65,536 X 9 Organization
- Single 5-V Supply (10% Tolerance)
- 30-Pin Single-in-Line Package (SIP)
- Utilizes Nine 64K Dynamic RAMs in Plastic Chip Carrier
- Long Refresh Period . . . 4 ms (256 Cycles)
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Outputs
- Performance Ranges:

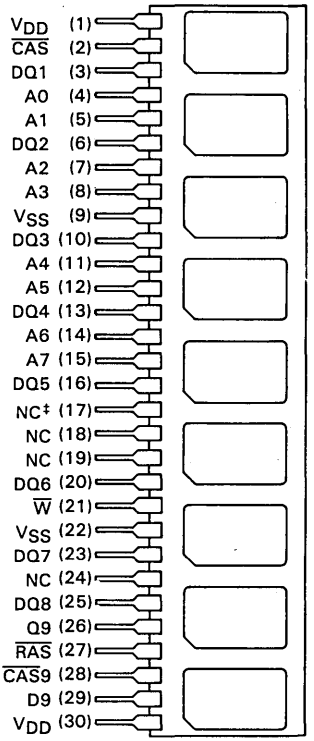
	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)
TM4164__9-12	120 ns	75 ns	230 ns
TM4164__9-15	150 ns	90 ns	260 ns
TM4164__9-20	200 ns	135 ns	326 ns

- Common $\overline{CAS}$ Control for Eight Common Data-In and Data-Out Lines
- Separate $\overline{CAS}$ Control for One Separate Pair of Data-In and Data-Out Lines
- Low Power Dissipation:

	OPERATING (TYP)	STANDBY (TYP)
TM4164__9-12	1800 mW	157.5 mW
TM4164__9-15	1575 mW	157.5 mW
TM4164__9-20	1215 mW	157.5 mW

- Operating Free-Air Temperature . . . 0°C to 70°C

TM4164EL9 . . . L SINGLE-IN-LINE PACKAGE†
TM4164FM9 . . . M SINGLE-IN-LINE PACKAGE
(TOP VIEW)



†TM4164EL9 package is shown.
‡Pin 17 of the 256K × 9 SIP will be memory address A8.

description

The TM4164__9 series are 576K, dynamic random-access memory modules organized as 65,536 × 9 bits [bit nine (D9, Q9) is generally used for parity and is controlled by $\overline{CAS9}$] in a 30-pin single-in-line package comprising nine TMS4164FPL, 65,536 × 1 bit dynamic RAM's in 18-lead plastic chip carriers mounted on top of a substrate together with nine 0.1 μF decoupling capacitors mounted beneath the chip carriers. The onboard capacitors eliminate the need for bypassing on the motherboard and offer superior performance over equivalent leaded capacitors due to reduced lead inductance. Also, with 0.3 inch board spacing the TM4164__9 has a density of ten devices per square inch (approximately 4X the density of DIPs). With the elimination of bypass capacitors on the motherboard, reduced PC board size, and fewer plated-through holes, a cost savings can be realized.

PIN NOMENCLATURE	
A0-A7	Address Inputs
$\overline{CAS}$, $\overline{CAS9}$	Column-Address Strobes
DQ1-DQ8	Data In/Data Out
D9	Data In
NC	No Connection
Q9	Data Out
$\overline{RAS}$	Row-Address Strobe
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

The TM4164__9 features $\overline{RAS}$ access times of 120 ns, 150 ns, and 200 ns maximum. Power dissipation as low as 1215 mW typical operating and 157.5 mW typical standby.

Refresh period is extended to 4 milliseconds, and during this period each of the 256 rows must be strobed with $\overline{RAS}$ in order to retain data. $\overline{CAS}$ can remain high during the refresh sequence to conserve power.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address lines and data in are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TM4164__9 is rated for operation from 0°C to 70°C.

operation

address (A0 through A7)

Sixteen address bits are required to decode 1 of 65,536 storage cell locations on each of the nine chips. Eight row-address bits are set up on pins A0 through A7 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the eight column-address bits are set up on pins A0 through A7 and latched onto the chip by the column-address strobes ($\overline{CAS}$ for M1 thru M8 and $\overline{CAS}$9 for M9). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers for M1-M8. $\overline{CAS}$9 is used similarly for M9.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data inputs are disabled when the read mode is selected. The common I/O feature of the TM4164__9 dictates the use of early write cycles to prevent contention on D and Q. When $\overline{W}$ goes low prior to $\overline{CAS}$, the data outs will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data in (DQ1-DQ8, D9)

Data is written during a write cycle. The falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latches. These latches can be driven from standard TTL circuits without a pull-up resistor. In the early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal.

data out (DQ1-DQ8, Q9)

The three-state output buffers provide direct TTL compatibility (no pull-up resistor required) with a fan out of two Series 74 TTL loads for each output. Data out is the same polarity as data in. The outputs are in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the outputs go active after the access time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ is satisfied. The outputs become valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low; $\overline{CAS}$ going high returns it to a high-impedance state. In the early write cycle, the outputs are always in the high-impedance state, a necessity due to the common I/O feature of the TM4164__9.

refresh

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffers are in the high-impedance state unless $\overline{CAS}$ is applied, the $\overline{RAS}$-only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses (A0 through A7) with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power.

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page mode

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the module. Thus, the time required to setup and strobe sequential row addresses for the same page is eliminated. To extend beyond the 256 column locations on M1-M9, the row address and $\overline{RAS}$ are applied to multiple modules. $\overline{CAS}$ is then decoded to select the proper module.

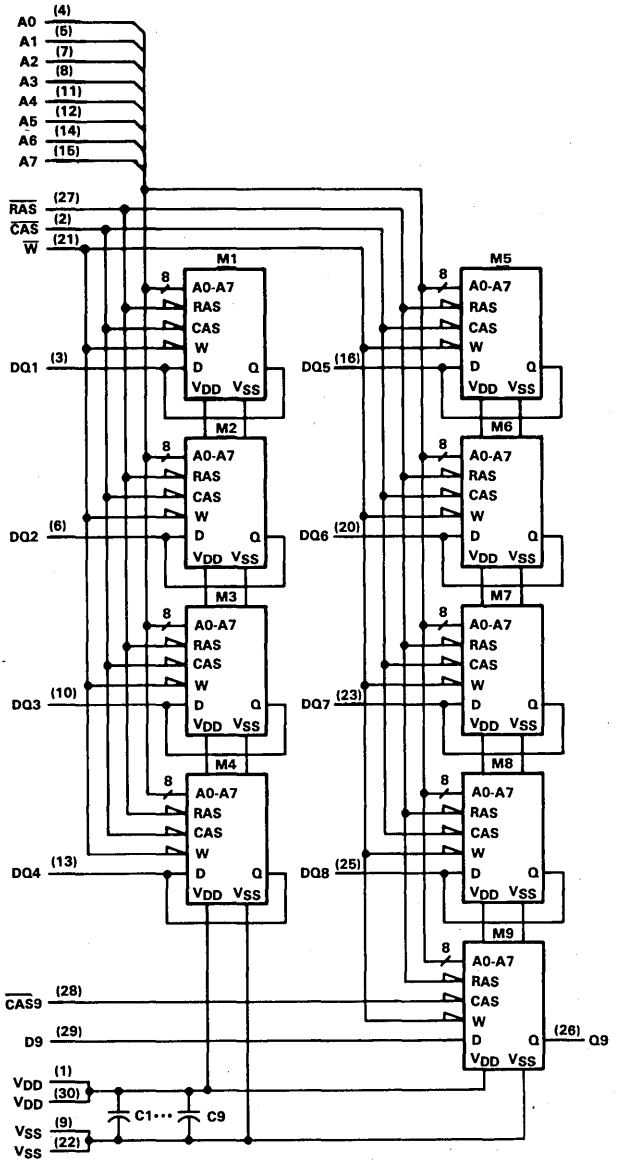
power up

After power up, the power supply must remain at its steady-state value for 1 ms. In addition, $\overline{RAS}$ must remain high for 100 μs immediately prior to initialization. Initialization consists of performing eight $\overline{RAS}$ cycles before proper device operation is achieved.

single-in-line package and components

PC substrate: 0,79 mm (0.031 inch) minimum thickness
Bypass capacitors: Multilayer ceramic
Leads: Tin/lead solder coated over phosphor-bronze
Contact area for socketable devices: Nickel plate and solder plate on top of copper

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range for any pin except V_{DD} and data out (see Note 1) . . . . . −1.5 V to 10 V
Voltage range on V_{DD} supply and data out with respect to V_{SS} . . . . . −1 V to 6 V
Short circuit output current for any output . . . . . 50 mA
Power dissipation . . . . . 9 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		4.5	5	5.5	V
V_{SS}	Supply voltage			0		V
V_{IH}	High-level input voltage	V_{DD} = 4.5 V	2.4		4.8	V
		V_{DD} = 5.5 V	2.4		6	
V_{IL}	Low-level input voltage(see Notes 2 and 3)		−0.6		0.8	V
T_A	Operating free-air temperature		0		70	°C

NOTES: 2. The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

3. Due to input protection circuitry, the applied voltage may begin to clamp at −0.6 V. Test conditions should comprehend this occurrence. See application report entitled "TMS4164A and TMS4416 Input Protection Diode" on page 9-5.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TM4164__9-12			TM4164__9-15			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4			2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4			0.4	V
I_I	Input current (leakage)	V_I=0 V to 5.8 V, V_{DD}=5 V, All other pins = 0 V			±10			±10	μA
I_O	Output current (leakage)	V_O = 0.4 to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10			±10	μA
I_{DD1}‡	Average operating current during read or write cycle	t_c = minimum cycle, All outputs open		360	432		315	405	mA
I_{DD2}‡	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, All outputs open		31.5	45		31.5	45	mA
I_{DD3}‡	Average refresh current	t_c = minimum cycle, $\overline{CAS}$ high and $\overline{RAS}$ cycling, All outputs open		252	360		225	333	mA
I_{DD4}‡	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low and $\overline{CAS}$ cycling, All outputs open		252	360		225	333	mA

†All typical values are at T_A = 25°C and nominal supply voltages.
‡I_{DD1}-I_{DD4} are measured with M1-M9 in the same mode (i.e., operating, standby, refresh or page mode).

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TM4164__9-20			UNIT
			MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 5.8 V, V_{DD} = 5 V All other pins = 0 V			±10	μA
I_O	Output current (leakage)	V_O = 0.4 to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10	μA
I_{DD1}‡	Average operating current during read or write cycle	t_c = minimum cycle, All outputs open		243	333	mA
I_{DD2}‡	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, All outputs open		31.5	45	mA
I_{DD3}‡	Average refresh current	t_c = minimum cycle, $\overline{CAS}$ high and $\overline{RAS}$ cycling, All outputs open		180	288	mA
I_{DD4}‡	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low and $\overline{CAS}$ cycling, All outputs open		180	288	mA

†All typical values are at T_A = 25°C and nominal supply voltages.
‡I_{DD1}-I_{DD4} are measured with M1-M9 in the same mode (i.e., operating, standby, refresh or page mode).

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

PARAMETER		MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs	45	pF
$C_{i(DQ)}$	Input capacitance, data inputs	11	pF
$C_{i(RAS)}$	Input capacitance, $\overline{RAS}$ input	72	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$ input	72	pF
$C_{i(CAS9)}$	Input capacitance, $\overline{CAS}$9 input	8	pF
$C_{i(CAS)}$	Input capacitance, $\overline{CAS}$ input	72	pF
$C_{i(D9)}$	Input capacitance, D9 input	5	pF
$C_{o(Q9)}$	Output capacitance, Q9 output	6	pF

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TM4164__9-12		TM4164__9-15		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		75		90	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, Load = 2 Series 74 TTL gates	t_{RAC}		120		150	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	40	0	40	ns

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switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TM4164__9-20		UNIT
				MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		135	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, Load = 2 Series 74 TTL gates	t_{RAC}		200	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	50	ns

timing requirements over recommended supply voltage range and operating free-air temperature range

		ALT. SYMBOL	TM4164__9-12		TM4164__9-15		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(P)}$	Page-mode cycle time	t_{PC}	130		160		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	230		260		ns
$t_{c(W)}$	Write cycle time	t_{WC}	230		260		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (precharge time)‡	t_{CP}	50		50		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low	t_{CAS}	75	10,000	90	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge time)	t_{RP}	80		100		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low	t_{RAS}	120	10,000	150	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	40		45		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	10	50	10	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	50		50		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	50		50		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	40		45		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	20		25		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	90		100		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DHC}	45		50		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	90		100		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	5		5		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	45		50		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	90		100		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	120		150		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	60		100		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only) to guarantee access time)	t_{RCD}	25	45	30	60	ns
t_{WLCL}	Delay time $\overline{W}$ low to $\overline{CAS}$ low (early write cycle)	t_{WCS}	0		0		ns
t_{rf}	Refresh time interval	t_{REF}		4		4	ms

NOTE 4: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, V_{IL} max and V_{IH} min must be met at the 10% and 90% points.

†All cycle times assume t_t = 5 ns. The specified t_t is due to testing limitations. Transition times may be as little as 3 ns in system use.

‡Page mode only.

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timing requirements over recommended supply voltage range and operating free-air temperature range

		ALT. SYMBOL	TM4164__9-20		UNIT
			MIN	MAX	
$t_{c(P)}$	Page-mode cycle time	t_{PC}	206		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	236		ns
$t_{c(W)}$	Write cycle time	t_{WC}	326		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (precharge time)‡	t_{CP}	80		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low	t_{CAS}	135	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge time)	t_{RP}	120		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low	t_{RAS}	200	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	55		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	10	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	60		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	60		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	55		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	30		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	125		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DHC}	60		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	145		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	5		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	60		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	145		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	200		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	135		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	35	65	ns
t_{WLCL}	Delay time, $\overline{W}$ low to $\overline{CAS}$ low (early write cycle)	t_{WCS}	0		ns
t_{rf}	Refresh time interval	t_{REF}		4	ms

NOTE 4: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, V_{IL} max and V_{IH} min must be met at the 10% and 90% points.

†All cycle times assume t_t = 5 ns. The specified t_t is due to testing limitations. Transition times may be as little as 3 ns in system use.

‡Page mode only.

PARAMETER MEASUREMENT INFORMATION

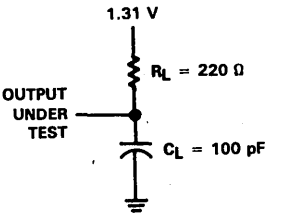
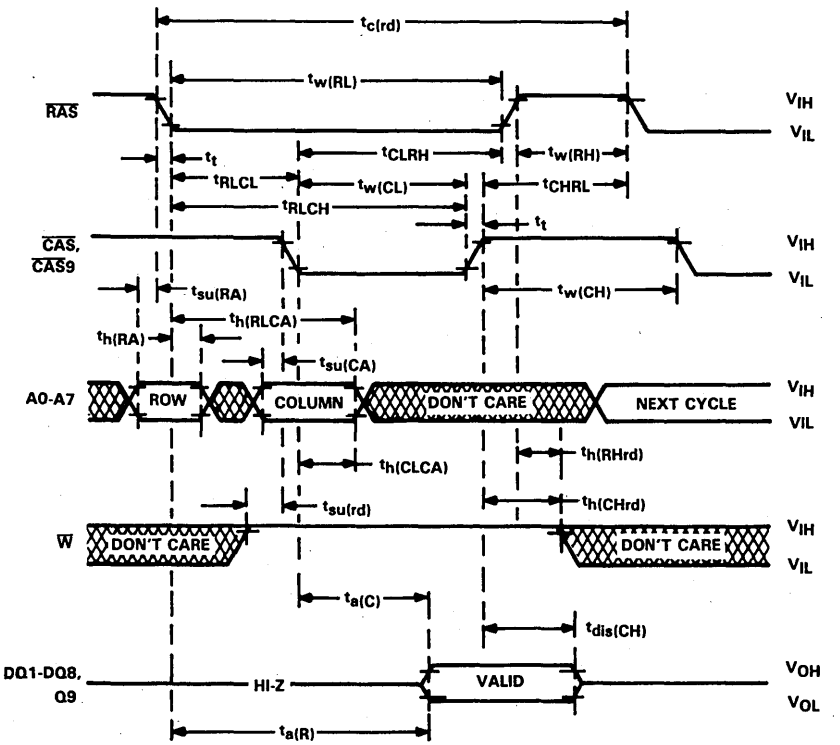


FIGURE 1. LOAD CIRCUIT

read cycle timing



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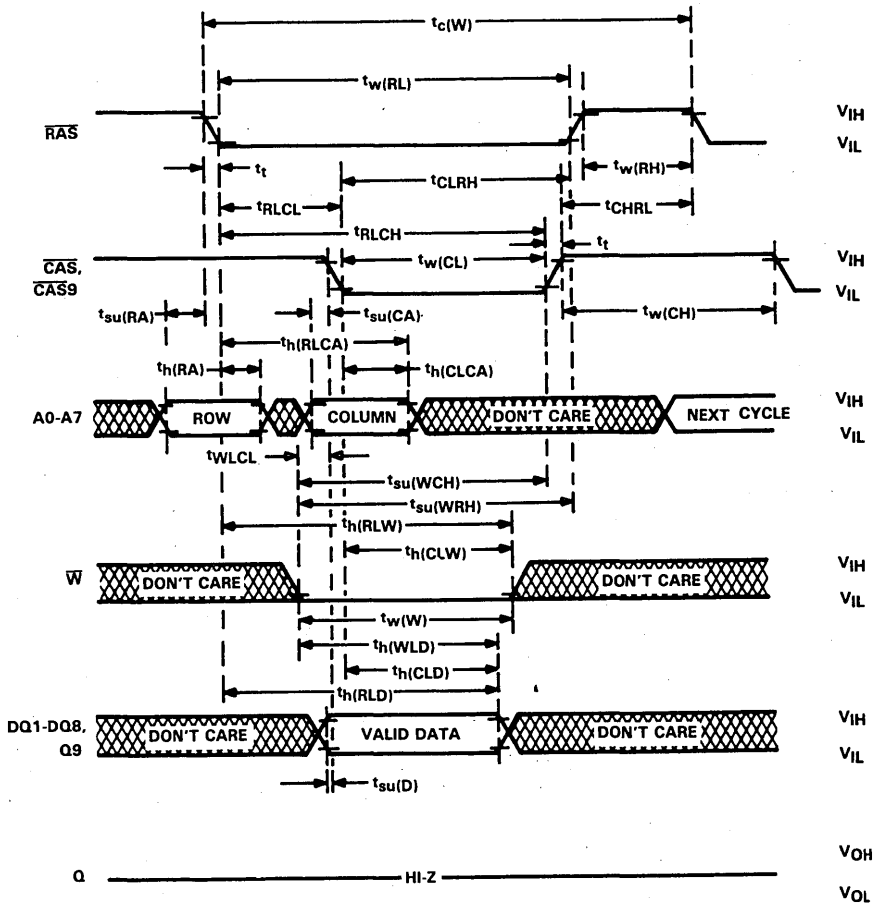
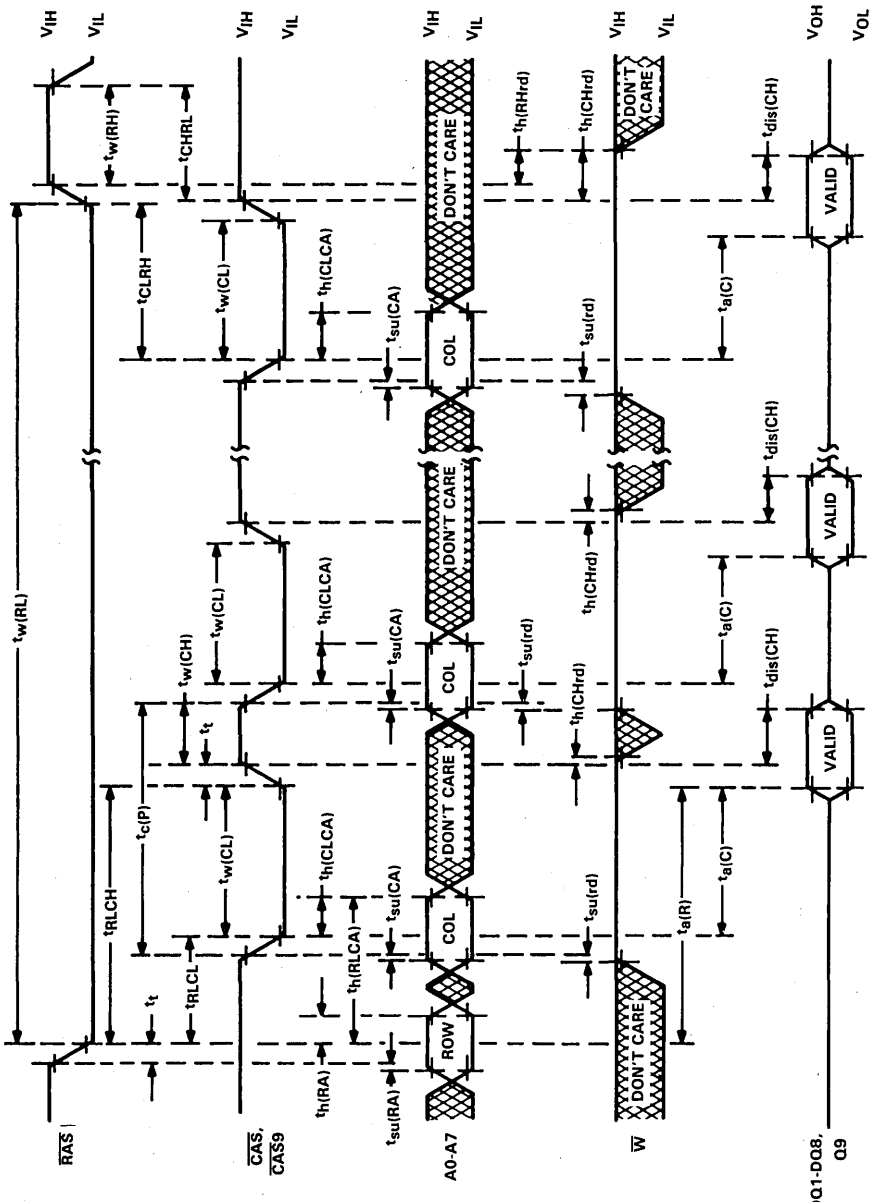
early-write cycle timing

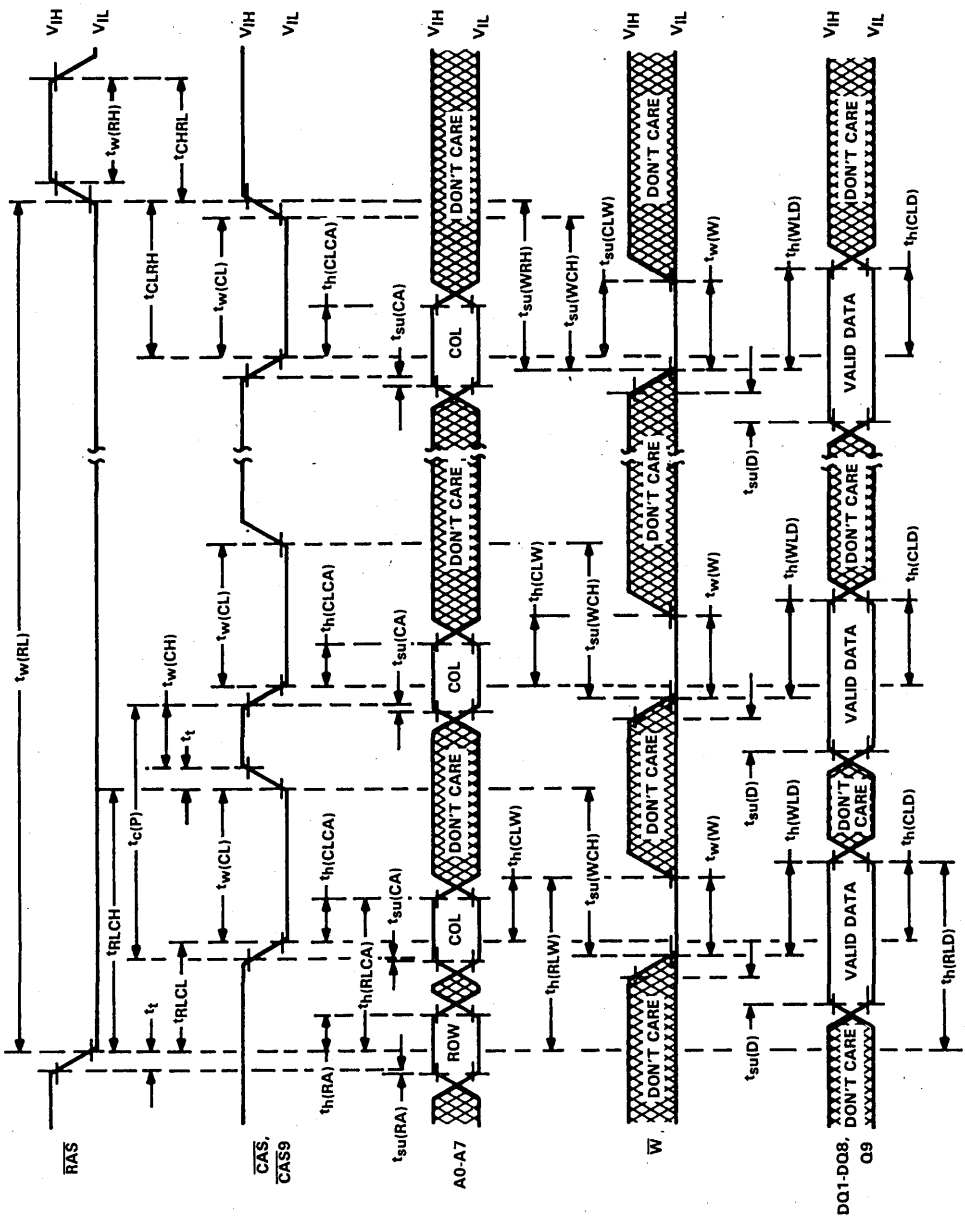


page-mode read cycle timing



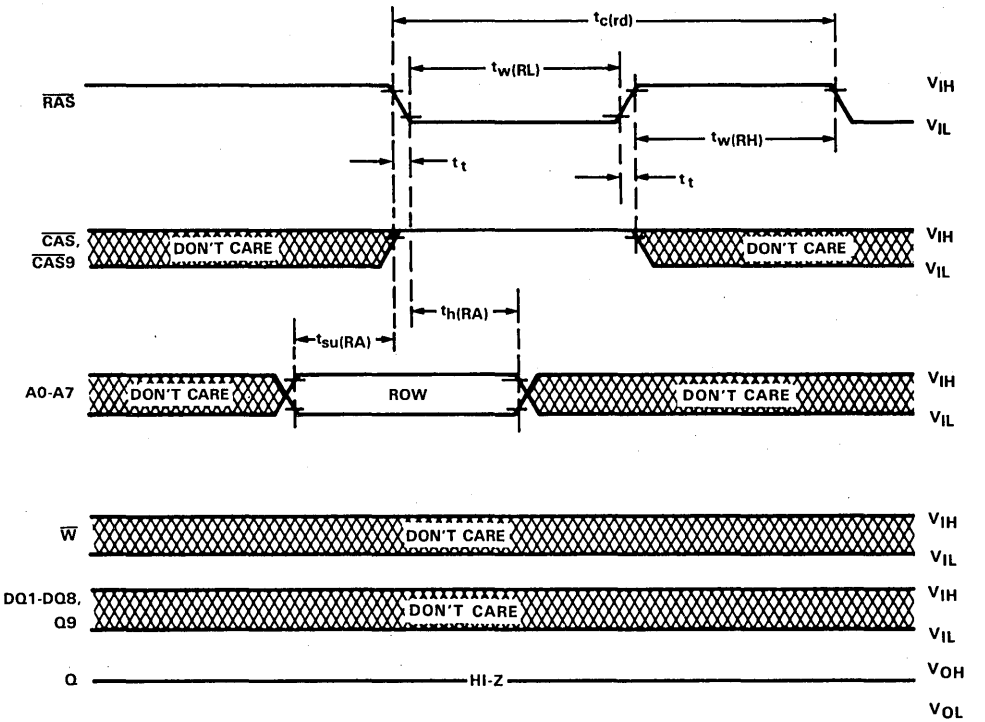
NOTE: 5. A write cycle or a read-modify-write cycle can be intermixed with read cycles as long as the write and read-modify-write timing specifications are not violated.

page-mode write cycle timing

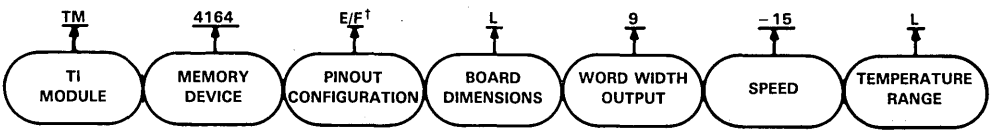


NOTE: 6. A read cycle or a read-modify-write cycle can be intermixed with write cycles as long as the read and read-modify-write timing specifications are not violated.

$\overline{\text{RAS}}$-only refresh timing



TI single-in-line package nomenclature



L Package
(76,2 x 16,5 mm)
(3.0 x 0.65 inches)

M Package
(88,9 x 15,24 mm)
(3.5 x 0.6 inches)

Max Access
–12 120 ns
–15 150 ns
–20 200 ns

L 0°C fo 70°C

†The E pinout configuration designator is used when specifying the L package; the F pinout configuration version designator is used when specifying the M package.

TM4164EQ5
65,536 BY 5-BIT DYNAMIC RAM MODULE

SEPTEMBER 1985 – REVISED NOVEMBER 1985

- 65,536 X 5 Organization
- Single 5-V Supply (10% Tolerance)
- 24-Pin Single-in-Line Package (SIP)
- Utilizes Five 64K Dynamic RAMs in Plastic Chip Carrier
- Long Refresh Period . . . 4 ms (256 cycles)
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Outputs
- Performance Ranges:

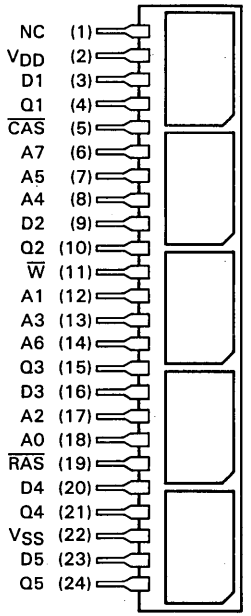
	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	READ-MODIFY-WRITE CYCLE (MIN)
TM4164EQ5-12	120 ns	75 ns	230 ns	260 ns
TM4164EQ5-15	150 ns	90 ns	260 ns	285 ns
TM4164EQ5-20	200 ns	135 ns	330 ns	345 ns

- Common $\overline{CAS}$ Control with Separate Data-In and Data-Out Lines with an "Early Write" Feature
- Low Power Dissipation:

	OPERATING (TYP)	STANDBY (TYP)
TM4161EQ5-12	1000 mW	88 mW
TM4164EQ5-15	875 mW	88 mW
TM4164EQ5-20	675 mW	88 mW

- Operating Free-Air Temperature . . . 0°C to 70°C
- Upward Compatible with 256K X 5 Single-in-Line Package

Q SINGLE-IN-LINE PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A7	Address Inputs
$\overline{CAS}$	Column-Address Strobe
D1-D5	Data Inputs
NC	No Connection
Q1-Q5	Data Outputs
$\overline{RAS}$	Row-Address Strobe
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The TM4164EQ5 is a 320K, dynamic random-access memory module organized as 65,536 × 5 bits in a 24-pin single-in-line package comprising five TMS4164FPL, 65,536 × 1 bit dynamic RAM's in 18-lead plastic chip carriers mounted on top of a substrate together with five 0.1 μF decoupling capacitors. The onboard capacitors eliminate the need for bypassing on the motherboard and offer superior performance over equivalent capacitors due to reduced lead inductance. Also, with 0.3 inch board spacing the TM4164EQ5 has a density of six devices per square inch (approximately 2.4X the density of DIPs). With the elimination of bypass capacitors on the motherboard, reduced PC board size, and fewer plated-through holes, a cost savings can be realized.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address lines and data in are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TM4164EQ5 is rated for operation from 0°C to 70°C.

upward compatibility

Future 256K × 5 memory modules in single-in-line packages will have identical pin functions and spacing, and will be directly upward compatible. Pin 1 of the TM4256EQ5 (256K × 5 SIP) module will be memory address A8.

operation

address (A0 through A7)

Sixteen address bits are required to decode 1 of 65,536 storage cell locations on each of the five chips. Eight row-address bits are set up on pins A0 through A7 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the eight column-address bits are set up on pins A0 through A7 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data inputs are disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$, the data-outs will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data in (D1-D5)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. This latch can be driven from standard TTL circuits without a pull-up resistor. In an early-write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data out (Q1-Q5)

The three-state output buffers provide direct TTL compatibility (no pull-up resistor required) with a fan out of two Series 74 TTL loads for each output. Data out is the same polarity as data in. The outputs are in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the outputs go active after the access time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ is satisfied. The outputs become valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low; $\overline{CAS}$ going high returns them to a high-impedance state. In the early write cycle, the outputs are always in the high-impedance state. In a delayed-write or read-modify-write cycle, the outputs will follow the sequence for the read cycle.

refresh

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffers are in the high-impedance state unless $\overline{CAS}$ is applied, the $\overline{RAS}$-only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses (A0 through A7) with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power.

page mode

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the module. Thus, the time required to setup and strobe sequential row addresses for the same page is eliminated. To extend beyond the 256 column locations on a single module, the row address and $\overline{RAS}$ are applied to multiple modules. $\overline{CAS}$ is then decoded to select the proper module.

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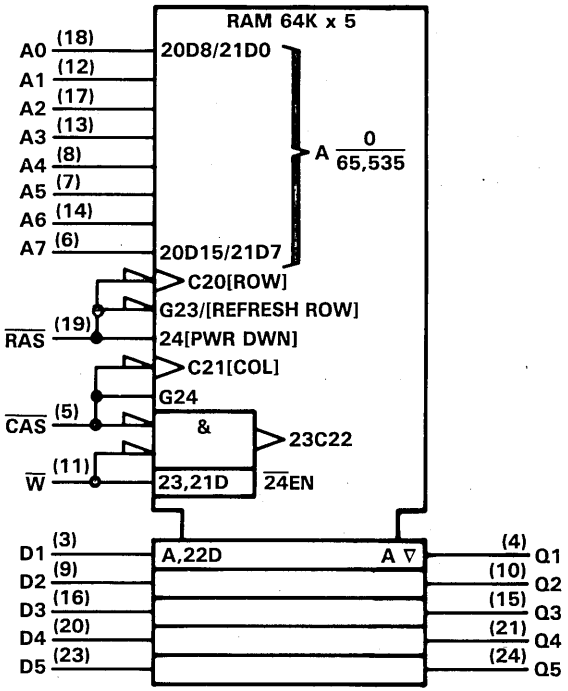
power up

After power up, the power supply must remain at its steady-state value for 1 ms. In addition, $\overline{RAS}$ must remain high for 100 μs immediately prior to initialization. Initialization consists of performing eight $\overline{RAS}$ cycles before proper device operation is achieved.

single-in-line package and components

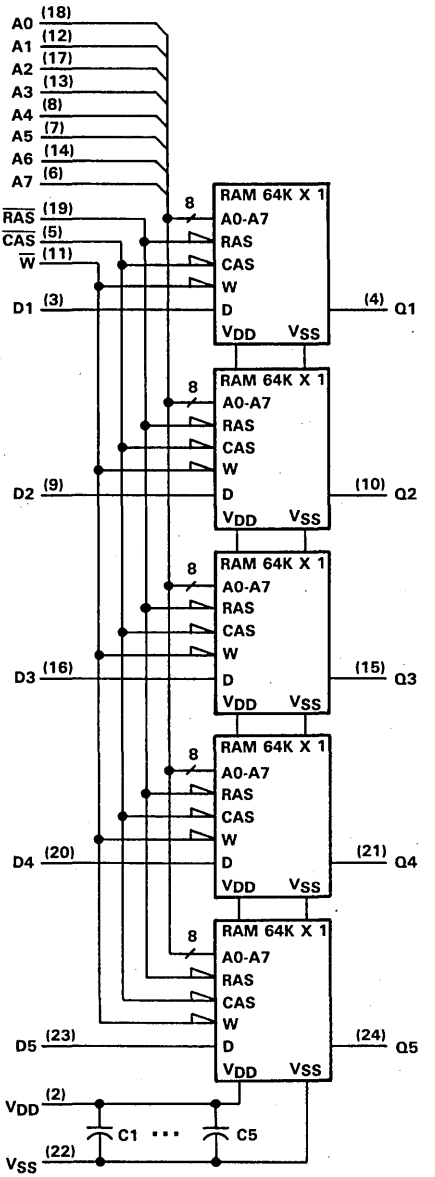
PC substrate: 0,79 mm (0.031 inch) minimum thickness
Bypass capacitors: Multilayer ceramic
Leads: Tin/lead solder coated over phosphor-bronze

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin except V_{DD} and data out (see Note 1) ..... −1.5 V to 10 V
Voltage range on V_{DD} supply and data out with respect to V_{SS} ..... −1 V to 6 V
Short circuit output current for any output ..... 50 mA
Power dissipation ..... 4 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		4.5	5	5.5	V
V_{SS}	Supply voltage			0		V
V_{IH}	High-level input voltage	V_{DD} = 4.5 V	2.4		4.8	V
		V_{DD} = 5.5 V	2.4		6	
V_{IL}	Low-level input voltage (see Notes 2 and 3)		−0.6		0.8	V
T_A	Operating free-air temperature		0		70	°C

NOTES: 2. The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

3. Due to input protection circuitry, the applied voltage may begin to clamp at −0.6 V. Test conditions should comprehend this occurrence. See application report entitled "TMS4164A and TMS4416 Input Protection Diode" on page 9-5.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TM4164EQ5-12			TM4164EQ5-15			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4			2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 5.8 V, V_{DD} = 5 V, All other pins = 0 V			±10			±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10			±10	μA
I_{DD1}	Average operating current during read or write cycle	t_c = minimum cycle, All outputs open		160	192		140	180	mA
I_{DD2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, All outputs open		14	20		14	20	mA
I_{DD3}	Average refresh current	t_c = minimum cycle, $\overline{CAS}$ high and $\overline{RAS}$ cycling, All outputs open		112	160		100	148	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low and $\overline{CAS}$ cycling, All outputs open		112	160		100	148	mA

†All typical values are at T_A = 25°C and nominal supply voltages.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TM4164EQ5-20			UNIT
			MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 5.8 V, V_{DD} = 5 V, All other pins = 0 V			±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10	μA
I_{DD1}	Average operating current during read or write cycle	t_c = minimum cycle, All outputs open		108	148	mA
I_{DD2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, All outputs open		14	20	mA
I_{DD3}	Average refresh current	t_c = minimum cycle, $\overline{CAS}$ high and $\overline{RAS}$ cycling, All outputs open		80	128	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low and $\overline{CAS}$ cycling, All outputs open		80	128	mA

†All typical values are at T_A = 25°C and nominal supply voltages.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

PARAMETER		MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs	TBD	pF
$C_{i(D)}$	Input capacitance, data input	TBD	pF
$C_{i(RC)}$	Input capacitance strobe inputs	TBD	pF
$C_{i(W)}$	Input capacitance, write enable input	TBD	pF
C_o	Output capacitance	TBD	pF

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TM4164EQ5-12		TM4164EQ5-15		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		75		90	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, Load = 2 Series 74 TTL gates	t_{RAC}		120		150	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	40	0	40	ns

Additional information on these products can be obtained from the factory as it becomes available.

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switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TM4164EQ5-20		UNIT
				MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		135	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, Load = 2 Series 74 TTL gates	t_{RAC}		200	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	50	ns

timing requirements over recommended supply voltage and operating free-air temperature range

		ALT. SYMBOL	TM4164EQ5-12		TM4164EQ5-15		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(P)}$	Page-mode cycle time	t_{PC}	130		160		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	230		260		ns
$t_{c(W)}$	Write cycle time	t_{WC}	230		260		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	260		285		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (precharge time)‡	t_{CP}	50		50		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low§	t_{CAS}	75	10,000	90	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge time)	t_{RP}	80		100		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low¶	t_{RAS}	120	10,000	150	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	40		45		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	5	50	5	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	50		50		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	50		50		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	40		45		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	20		25		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	90		100		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DHC}	45		50		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	90		100		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DHW}	40		45		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	5		5		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	45		50		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	90		100		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	120		150		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	60		100		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{CWD}	50		60		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	20	45	25	60	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{RWD}	110		120		ns
t_{WLCL}	Delay time, $\overline{W}$ low to $\overline{CAS}$ low (early write cycle)	t_{WCS}	0		0		ns
t_{rf}	Refresh time interval	t_{REF}		4		4	ms

NOTE 4: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, V_{IL} max and V_{IH} min must be met at the 10% and 90% points.

†All cycles times assume t_t = 5 ns.

‡Page mode only.

§In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$). This applies to page mode read-modify-write also.

¶In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).

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timing requirements over recommended supply voltage range and operating free-air temperature range

		ALT. SYMBOL	TM4164EQ5-20 MIN	TM4164EQ5-20 MAX	UNIT
$t_{c(P)}$	Page-mode cycle time	t_{PC}	206		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	326		ns
$t_{c(W)}$	Write cycle time	t_{WC}	326		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	345		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (precharge time)‡	t_{CP}	80		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low§	t_{CAS}	135	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge time)	t_{RP}	120		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low¶	t_{RAS}	200	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	55		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	60		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	60		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	55		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	30		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	125		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DHC}	60		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	145		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DHW}	55		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	5		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	60		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	145		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	200		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	135		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{CWD}	65		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	30	65	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{RWD}	130		ns
t_{WLCL}	Delay time, $\overline{W}$ low to $\overline{CAS}$ low (early write cycle)	t_{WCS}	0		ns
t_{rf}	Refresh time interval	t_{REF}		4	ms

NOTE 4: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, V_{IL} max and V_{IH} min must be met at the 10% and 90% points.

†All cycles times assume t_t = 5 ns.

‡Page mode only.

§In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$). This applies to page mode read-modify-write also.

¶In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).

PARAMETER MEASUREMENT INFORMATION

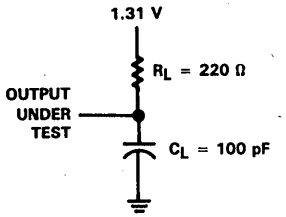
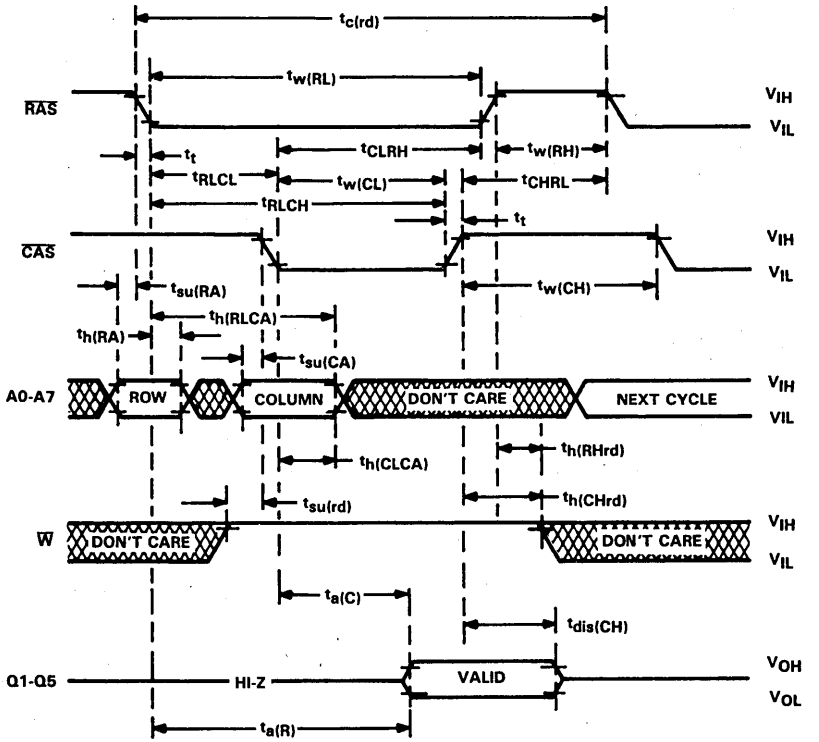


FIGURE 1. LOAD CIRCUIT

read cycle timing



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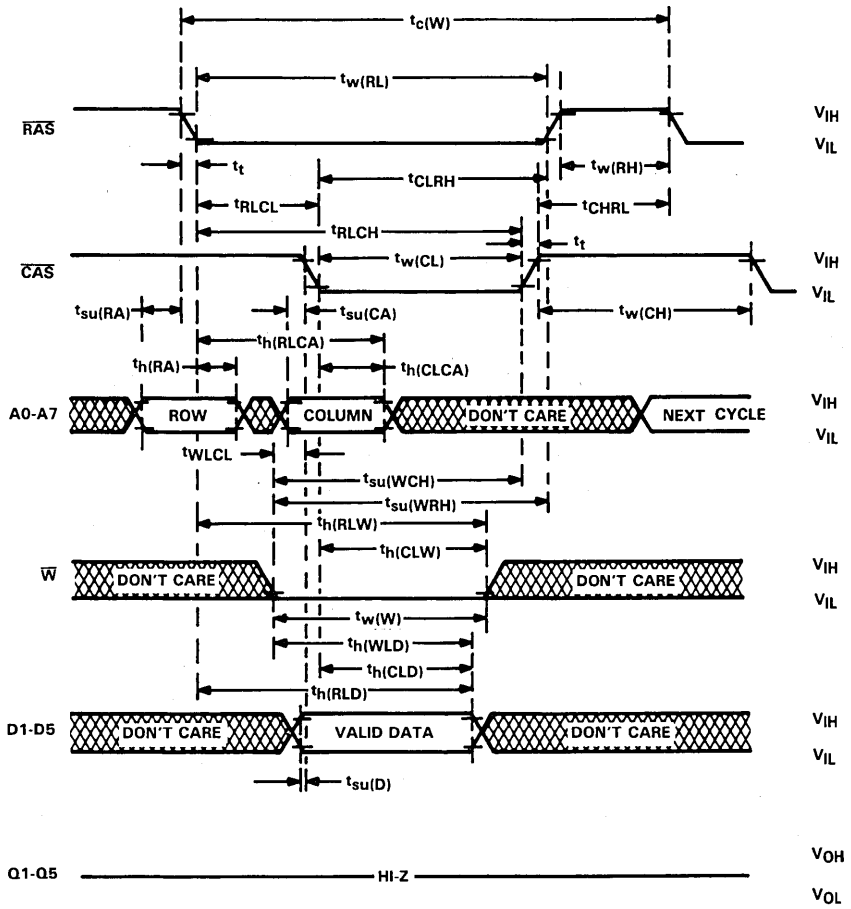
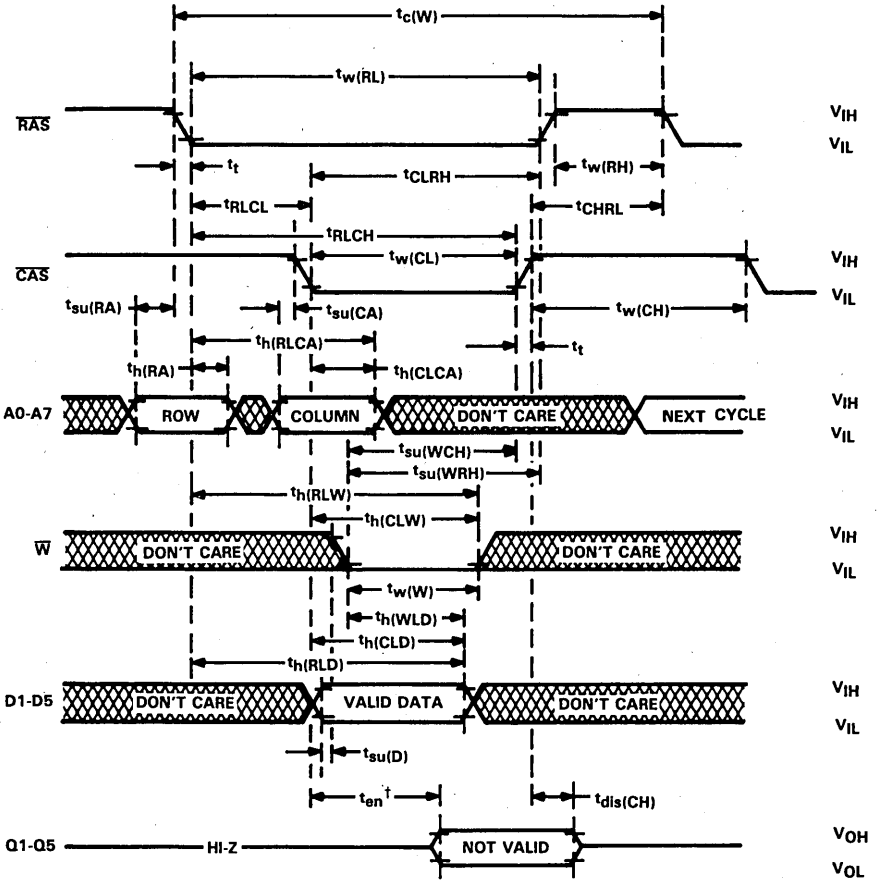
early write cycle timing



write cycle timing



† The enable time (t_{en}) for a write cycle is equal in duration to the access time from $\overline{CAS}$ ($t_{a(C)}$) in a read cycle; but the active levels at the output are invalid.

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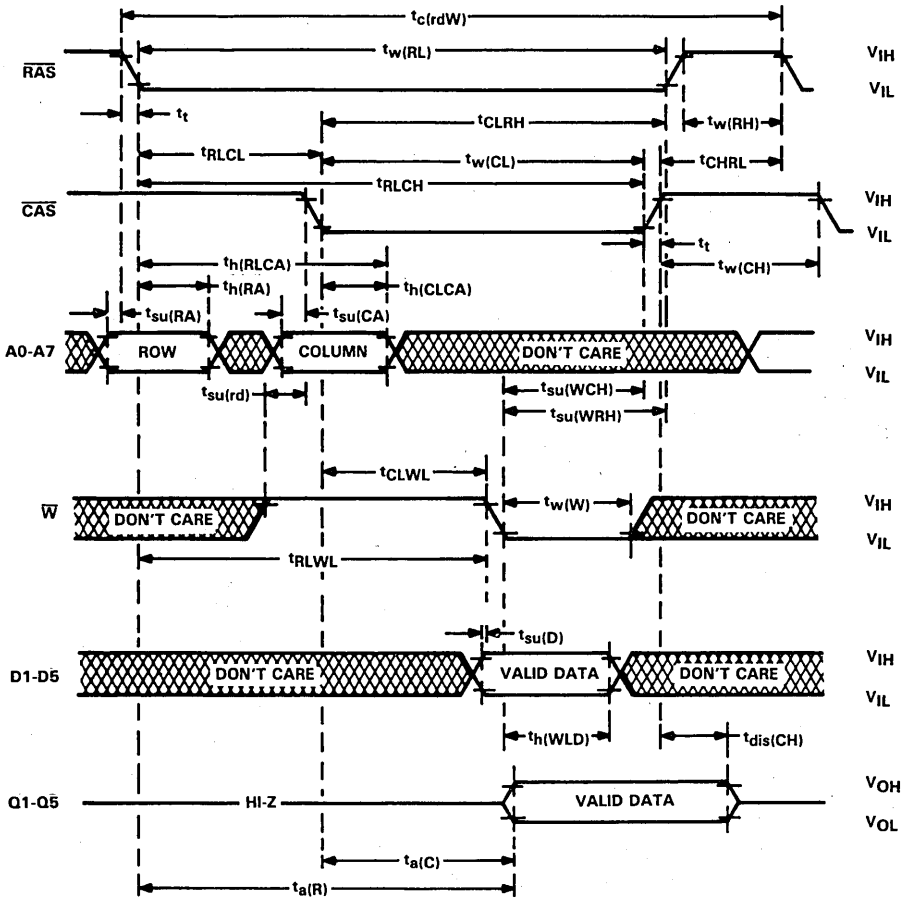
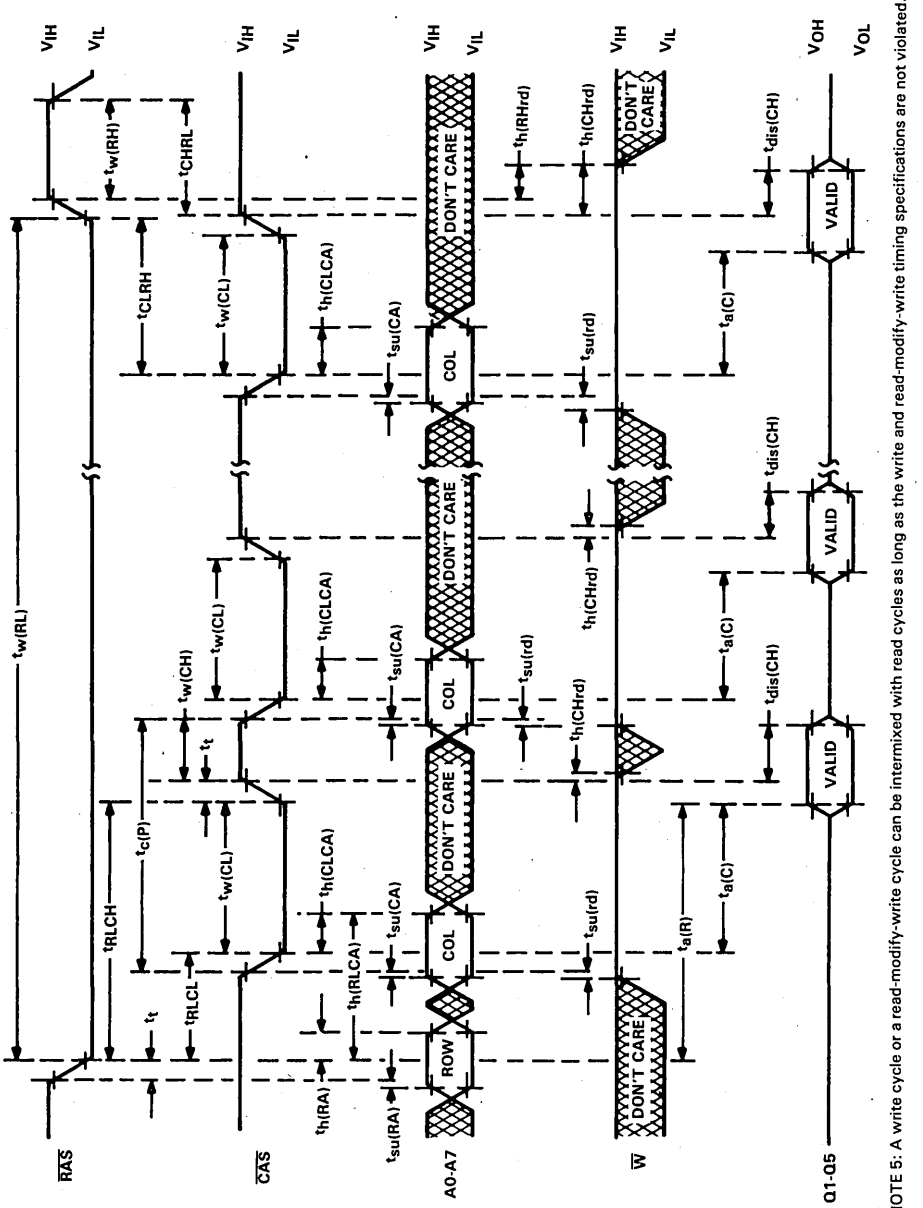
read-write/read-modify-write cycle timing

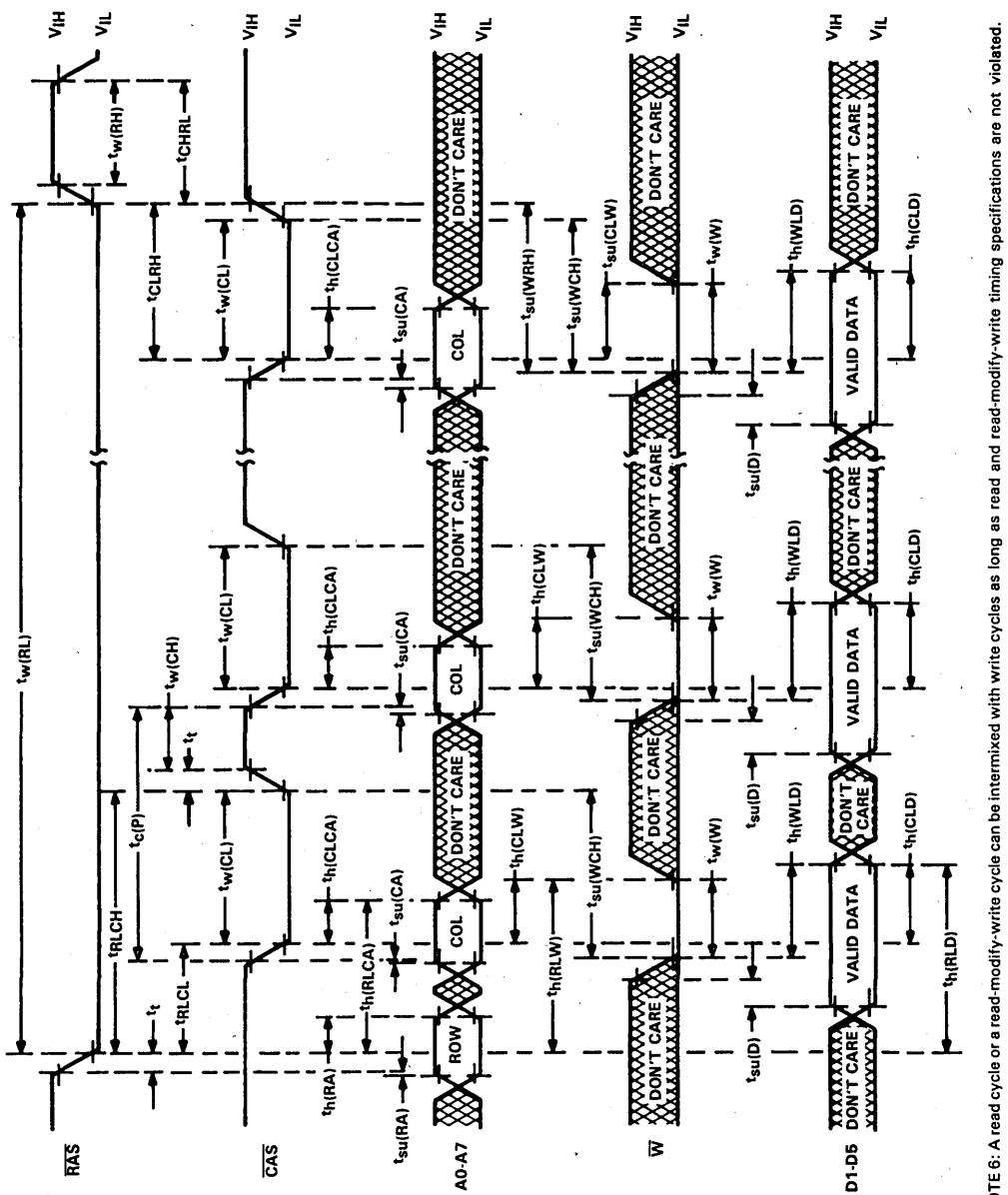


page-mode read cycle timing



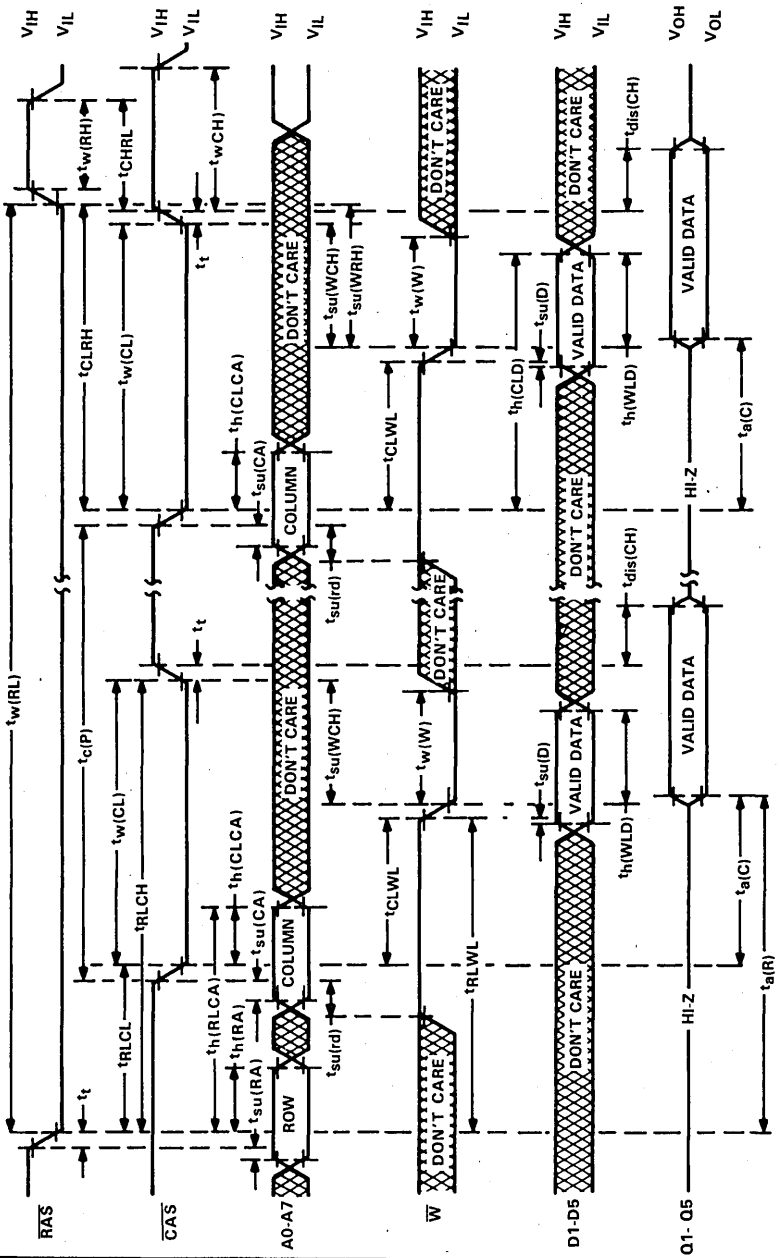
NOTE 5: A write cycle or a read-modify-write cycle can be intermixed with read cycles as long as the write and read-modify-write timing specifications are not violated.

page-mode write cycle timing



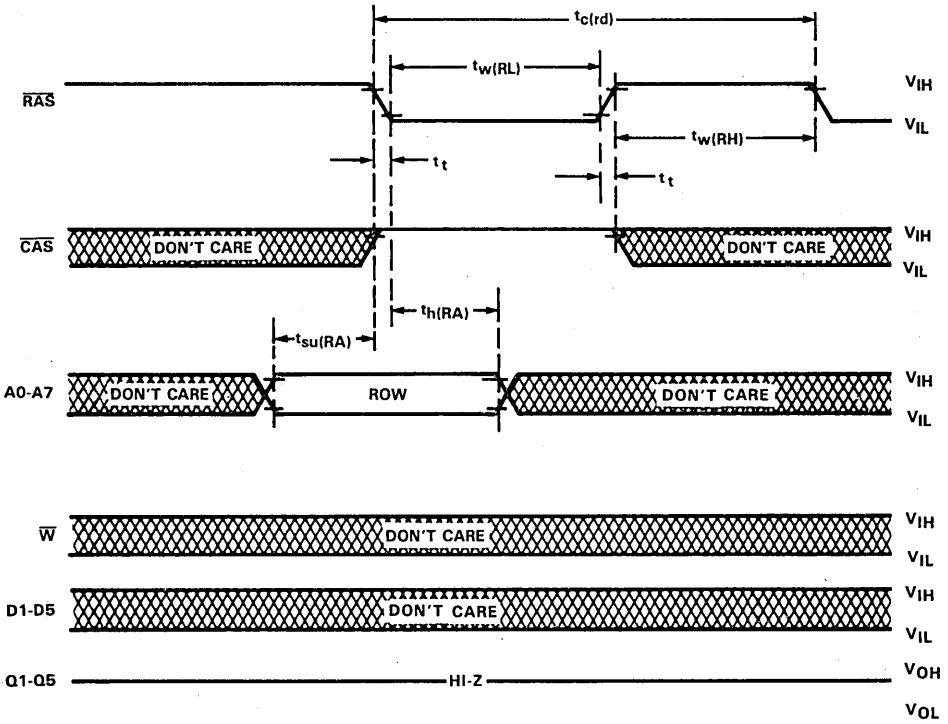
NOTE 6: A read cycle or a read-modify-write cycle can be intermixed with write cycles as long as read and read-modify-write timing specifications are not violated.

page-mode read-modify-write cycle timing

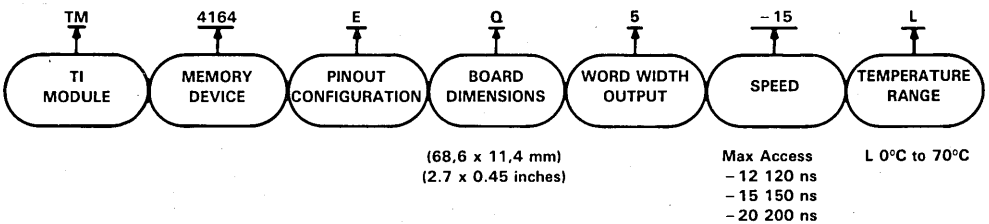


NOTE 7: A read or a write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

$\overline{\text{RAS}}$-only refresh timing



TI single-in-line package nomenclature



NOVEMBER 1983 — REVISED NOVEMBER 1985

- 65,536 X 8 Organization
- Single 5-V Supply (10% Tolerance)
- 30-Pin Single-in-Line Package (SIP)
- Utilizes Eight 64K Dynamic RAMs in Plastic Chip Carrier
- Long Refresh Period . . . 4 ms (256 Cycles)
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Outputs
- Performance Ranges:

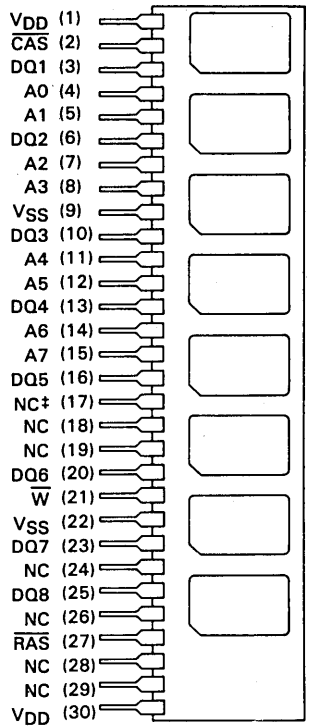
	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)
TM4164__8-12	120 ns	75 ns	230 ns
TM4164__8-15	150 ns	90 ns	260 ns
TM4164__8-20	200 ns	135 ns	326 ns

- Common $\overline{CAS}$ Control for Eight Common Data-In and Data-Out Lines
- Low Power Dissipation:

	OPERATING (TYP)	STANDBY (TYP)
TM4164__8-12	1600 mW	140 mW
TM4164__8-15	1400 mW	140 mW
TM4164__8-20	1080 mW	140 mW

- Operating Free-Air Temperature . . . 0°C to 70°C

TM4164FL8 . . . L SINGLE-IN-LINE PACKAGE†
TM4164FM8 . . . M SINGLE-IN-LINE PACKAGE
(TOP VIEW)



†TM4164FL8 package is shown.
‡Pin 17 of the 256K x 8 SIP is memory address A8.

description

The TM4164__8 series are 512K, dynamic random-access memory modules organized as 65,536 × 8-bits in a 30-pin single-in-line package comprising eight TMS4164FPL, 65,536 × 1-bit dynamic RAM's in 18-lead plastic chip carriers mounted on top of a substrate together with eight 0.1 μF decoupling capacitors mounted beneath the chip carriers. The onboard capacitors eliminate the need for bypassing on the motherboard and offer superior performance over equivalent leaded capacitors due to reduced lead inductance. Also, with 0.3 inch board spacing the TM4164__8 has a density of 8.5 devices per square inch (approximately 3.5X the density of of DIPs). With the elimination of bypass capacitors on the motherboard, reduced PC board size, and fewer plated-through holes, a cost savings can be realized.

PIN NOMENCLATURE	
A0-A7	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1-DQ8	Data In/Data Out
NC	No Connection
$\overline{RAS}$	Row-Address Strobe
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

The TM4164__8 features $\overline{RAS}$ access times of 120 ns, 150 ns, and 200 ns maximum. Power dissipation as low as 1080 mW typical operating and 140 mW typical standby.

Refresh period is extended to 4 milliseconds, and during this period each of the 256 rows must be strobed with $\overline{RAS}$ in order to retain data. $\overline{CAS}$ can remain high during the refresh sequence to conserve power.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address lines and data in are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TM4164__8 is rated for operation from 0°C to 70°C.

operation

address (A0 through A7)

Sixteen address bits are required to decode 1 of 65,536 storage cell locations on each of the eight chips. Eight row-address bits are set up on pins A0 through A7 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the eight column-address bits are set up on pins A0 through A7 and latched onto the chip by the column-address strobes. All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers for M1-M8.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data inputs are disabled when the read mode is selected. The common I/O feature of the TM4164__8 dictates the use of early write cycles to prevent contention on D and Q. When $\overline{W}$ goes low prior to $\overline{CAS}$, the data outs will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data in (DQ1-DQ8)

Data is written during a write cycle. The falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latches. These latches can be driven from standard TTL circuits without a pull-up resistor. In the early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal.

data out (DQ1-DQ8)

The three-state output buffers provide direct TTL compatibility (no pull-up resistor required) with a fan out of two Series 74 TTL loads for each output. Data out is the same polarity as data in. In a read cycle the outputs go active after the access time interval $t_a(C)$ that begins with the negative transition of $\overline{CAS}$ as long as $t_a(R)$ is satisfied. The outputs become valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low; $\overline{CAS}$ going high returns it to a high-impedance state. In the early write cycle, the outputs are always in the high-impedance state, a necessity due to the common I/O feature of the TM4164__8.

refresh

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffers are in the high-impedance state unless $\overline{CAS}$ is applied, the $\overline{RAS}$-only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses (A0 through A7) with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power.

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page mode

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the module. Thus, the time required to setup and strobe sequential row addresses for the same page is eliminated. To extend beyond the 256 column locations on M1-M8, the row address and $\overline{RAS}$ are applied to multiple modules. $\overline{CAS}$ is then decoded to select the proper module.

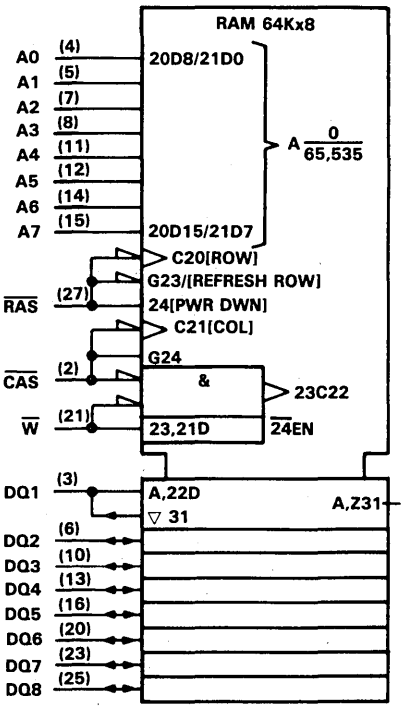
power up

After power up, the power supply must remain at its steady-state value for 1 ms. In addition, $\overline{RAS}$ must remain high for 100 μs immediately prior to initialization. Initialization consists of performing eight $\overline{RAS}$ cycles before proper device operation is achieved.

single-in-line package and components

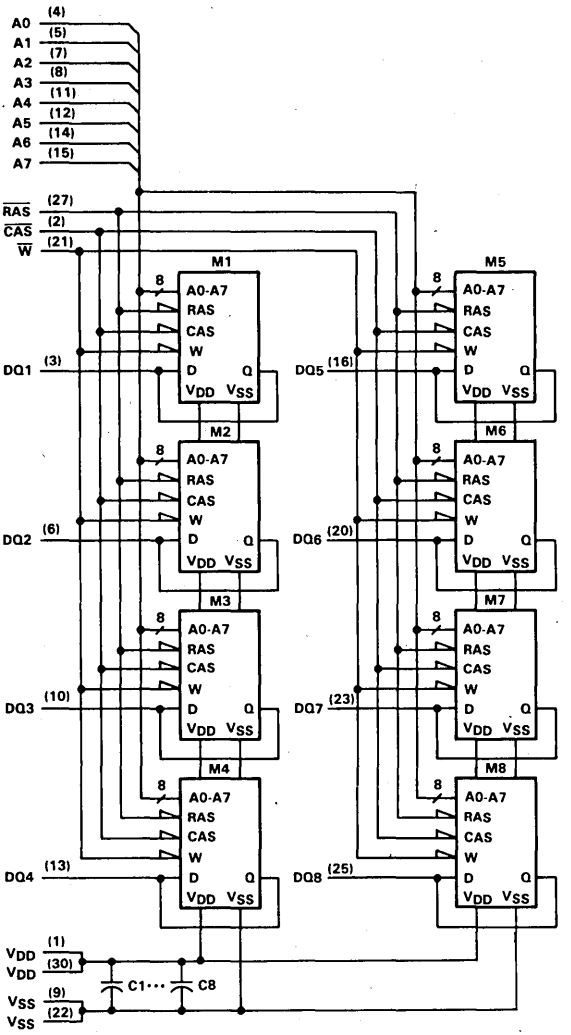
PC substrate: 0,79 mm (0.031 inch) minimum thickness
Bypass capacitors: Multilayer ceramic
Leads: Tin/lead solder coated over phosphor-bronze
Contact area for socketable devices: Nickel plate and solder plate on top of copper

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

functional block diagram



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin except V_{DD} and data out (see Note 1) . . . . . −1.5 V to 10 V
Voltage range on V_{DD} supply and data out with respect to V_{SS} . . . . . −1 V to 6 V
Short circuit output current for any output . . . . . 50 mA
Power dissipation . . . . . 8 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		4.5	5	5.5	V
V_{SS}	Supply voltage			0		V
V_{IH}	High-level input voltage	V_{DD} = 4.5 V	2.4		4.8	V
		V_{DD} = 5.5 V	2.4		6	
V_{IL}	Low-level input voltage (see Notes 2 and 3)		−0.6		0.8	V
T_A	Operating free-air temperature		0		70	°C

NOTES: 2. The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

3. Due to input protection circuitry, the applied voltage may begin to clamp at −0.6 V. Test conditions should comprehend this occurrence. See application report entitled "TMS4164A and TMS4416 Input Protection Diode" on page 9-5.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TM4164__8-12			TM4164__8-15			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4			2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 5.8 V, V_{DD} = 5 V, All other pins = 0 V			±10			±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10			±10	μA
I_{DD1}‡	Average operating current during read or write cycle	t_c = minimum cycle, All outputs open		320	384		280	360	mA
I_{DD2}‡	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, All outputs open		28	40		28	40	mA
I_{DD3}‡	Average refresh current	t_c = minimum cycle, $\overline{CAS}$ high and $\overline{RAS}$ cycling, All outputs open		224	320		200	296	mA
I_{DD4}‡	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low and $\overline{CAS}$ cycling, All outputs open		224	320		200	296	mA

† All typical values are at T_A = 25°C and nominal supply voltages.
‡ I_{DD1}-I_{DD4} are measured with M1-M8 in the same mode (i.e., operating, standby, refresh or page mode).

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TM4164__8-20			UNIT
			MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 5.8 V, V_{DD} = 5 V, All other pins = 0 V			±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10	μA
I_{DD1}‡	Average operating current during read or write cycle	t_c = minimum cycle, All outputs open		216	296	mA
I_{DD2}‡	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, All outputs open		28	40	mA
I_{DD3}‡	Average refresh current	t_c = minimum cycle, $\overline{CAS}$ high and $\overline{RAS}$ cycling, All outputs open		160	256	mA
I_{DD4}‡	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low and $\overline{CAS}$ cycling, All outputs open		160	256	mA

† All typical values are at T_A = 25°C and nominal supply voltages.
‡ I_{DD1}-I_{DD4} are measured with M1-M8 in the same mode (i.e., operating, standby, refresh or page mode).

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

PARAMETER		MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs	40	pF
$C_{i(DQ)}$	Input capacitance, data inputs	11	pF
$C_{i(RAS)}$	Input capacitance, $\overline{RAS}$ input	64	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$ input	64	pF
$C_{i(CAS)}$	Input capacitance, $\overline{CAS}$ input	64	pF

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TM4164__8-12		TM4164__8-15		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		75		90	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, Load = 2 Series 74 TTL gates	t_{RAC}		120		150	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	40	0	40	ns

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switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TM4164__8-20		UNIT
				MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		135	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, Load = 2 Series 74 TTL gates	t_{RAC}		200	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	50	ns

timing requirements over recommended supply voltage range and operating free-air temperature range

		ALT. SYMBOL	TM4164__8-12		TM4164__8-15		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(P)}$	Page-mode cycle time	t_{PC}	130		160		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	230		260		ns
$t_{c(W)}$	Write cycle time	t_{WC}	230		260		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (precharge time)‡	t_{CP}	50		50		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low	t_{CAS}	75	10,000	90	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge time)	t_{RP}	80		100		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low	t_{RAS}	120	10,000	150	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	40		45		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$ †	t_T	10	50	10	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	50		50		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	50		50		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	40		45		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	20		25		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	85		100		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DHC}	45		50		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	90		100		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	5		5		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	45		50		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	90		100		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	120		150		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	60		100		ns
t_{RLCL}	Delay, time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	25	45	30	60	ns
t_{WLCL}	Delay time, $\overline{W}$ low to $\overline{CAS}$ low (early write cycle)	t_{WCS}	0		0		ns
t_{rf}	Refresh time interval	t_{REF}		4		4	ms

NOTE 4: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, V_{IL} max and V_{IH} min must be met at the 10% and 90% points.

†All cycle times assume t_t = 5 ns. The specified t_t = is due to testing limitations. Transition times may be as little as 3 ns in system use.

‡Page mode only.

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timing requirements over recommended supply voltage range and operating free-air temperature range

		ALT. SYMBOL	TM4164__8-20		UNIT
			MIN	MAX	
$t_{c(P)}$	Page-mode cycle time	t_{PC}	206		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	326		ns
$t_{c(W)}$	Write cycle time	t_{WC}	326		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (precharge time)‡	t_{CP}	80		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low	t_{CAS}	135	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge time)	t_{RP}	120		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low	t_{RAS}	200	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	55		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$†	t_T	10	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	60		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	60		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	55		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	30		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	125		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DHC}	60		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	145		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	5		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	60		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	145		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	200		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	135		ns
t_{RLCL}	Delay, time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	35	65	ns
t_{WLCL}	Delay time, $\overline{W}$ low to $\overline{CAS}$ low (early write cycle)	t_{WCS}	0		ns
t_{rf}	Refresh time interval	t_{REF}		4	ms

NOTE 4: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, V_{IL} max and V_{IH} min must be met at the 10% and 90% points.

†All cycle times assume t_t = 5 ns. The specified t_t = is due to testing limitations. Transition times may be as little as 3 ns in system use.

‡Page mode only.

PARAMETER MEASUREMENT INFORMATION

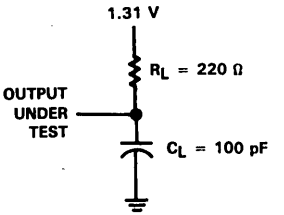
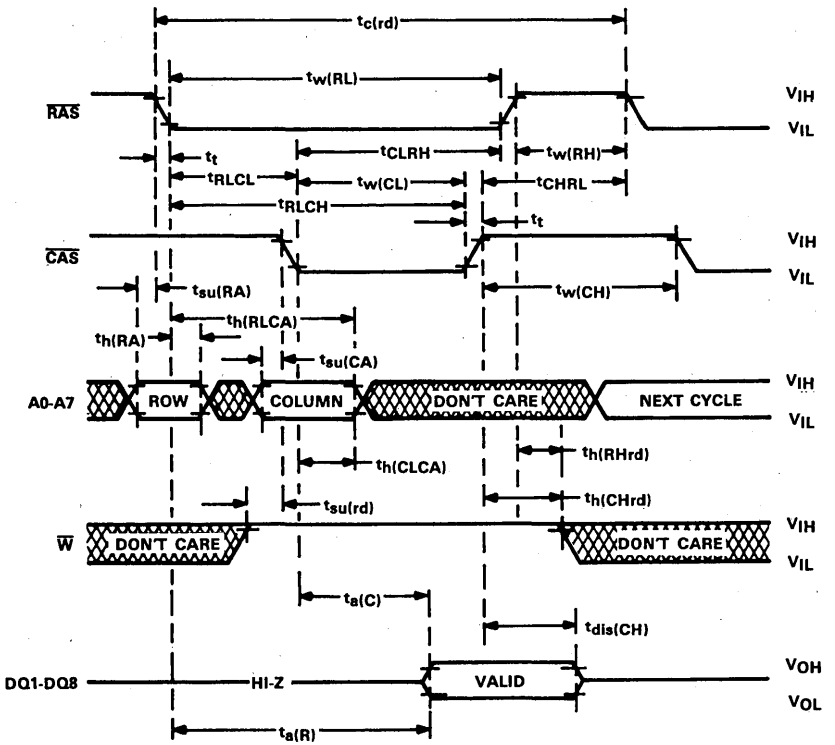


FIGURE 1. LOAD CIRCUIT

read cycle timing



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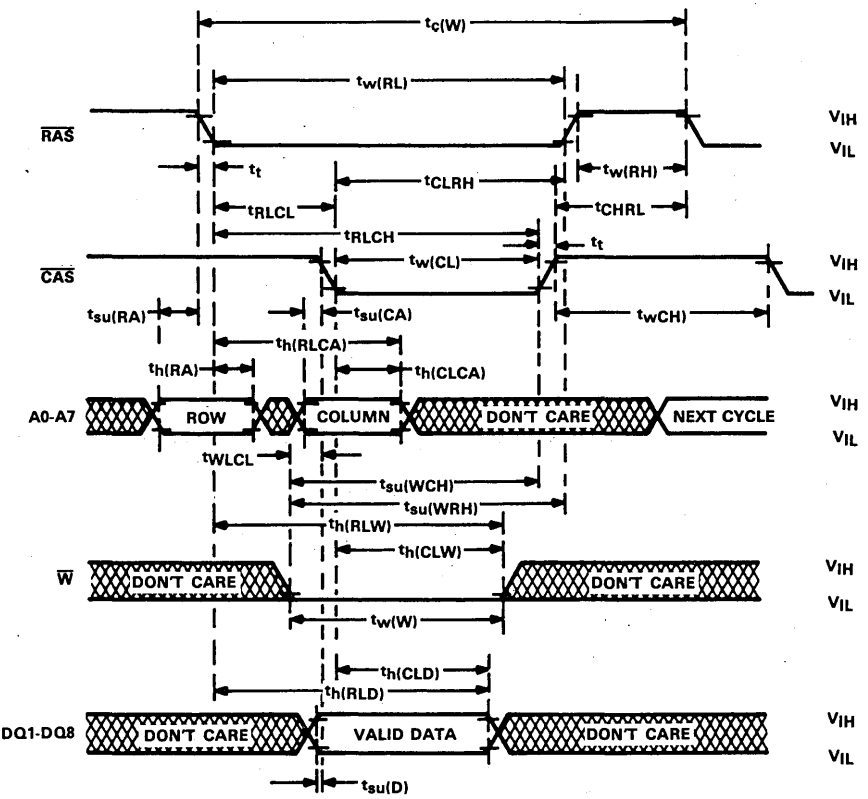
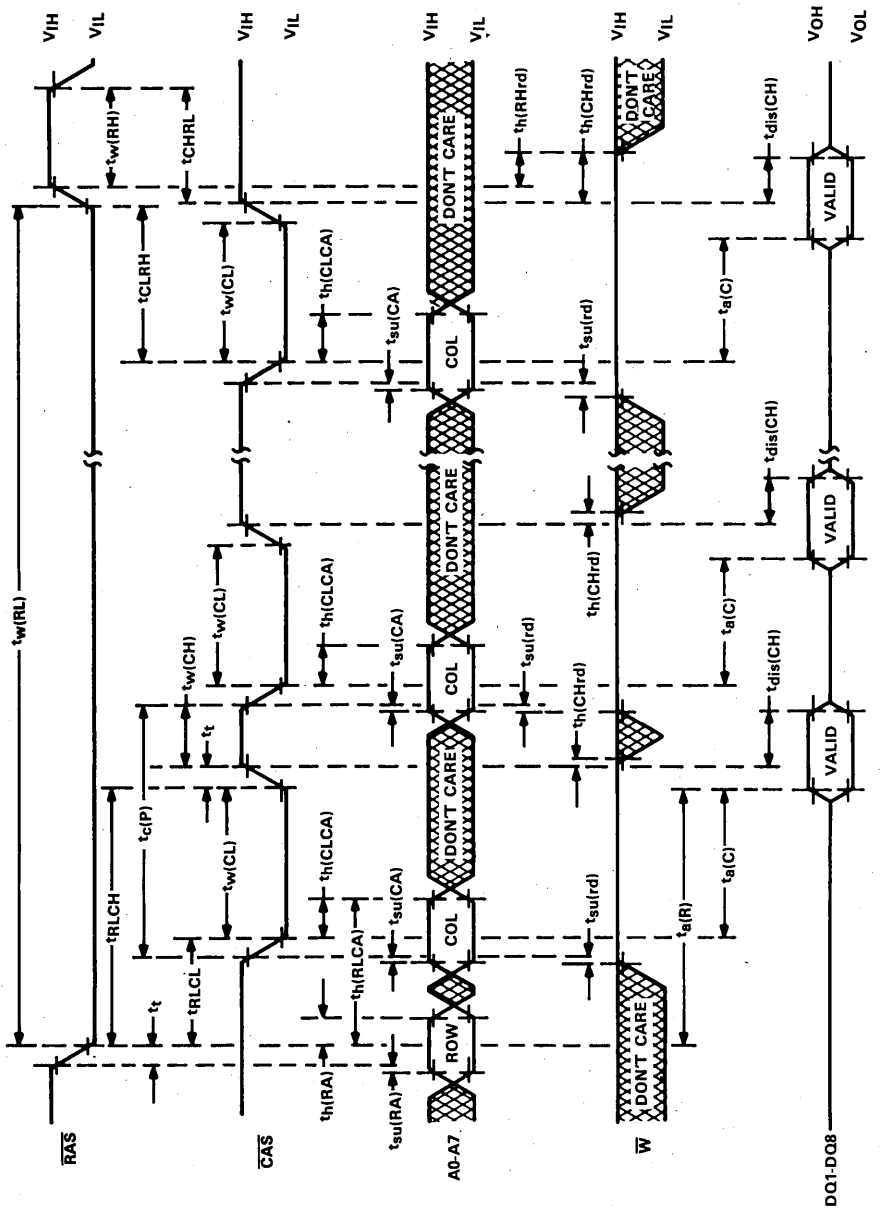
early write cycle timing

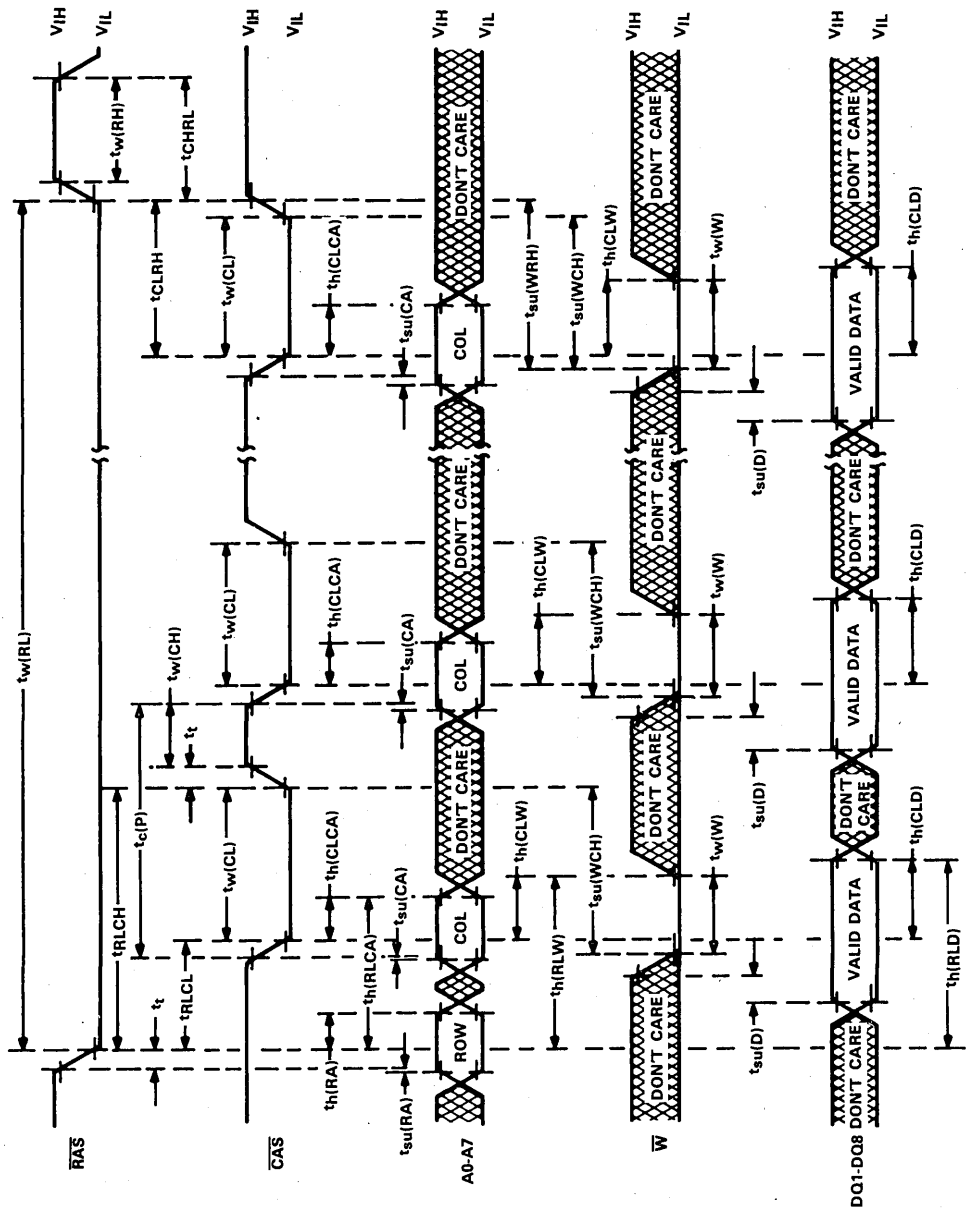


page-mode read cycle timing



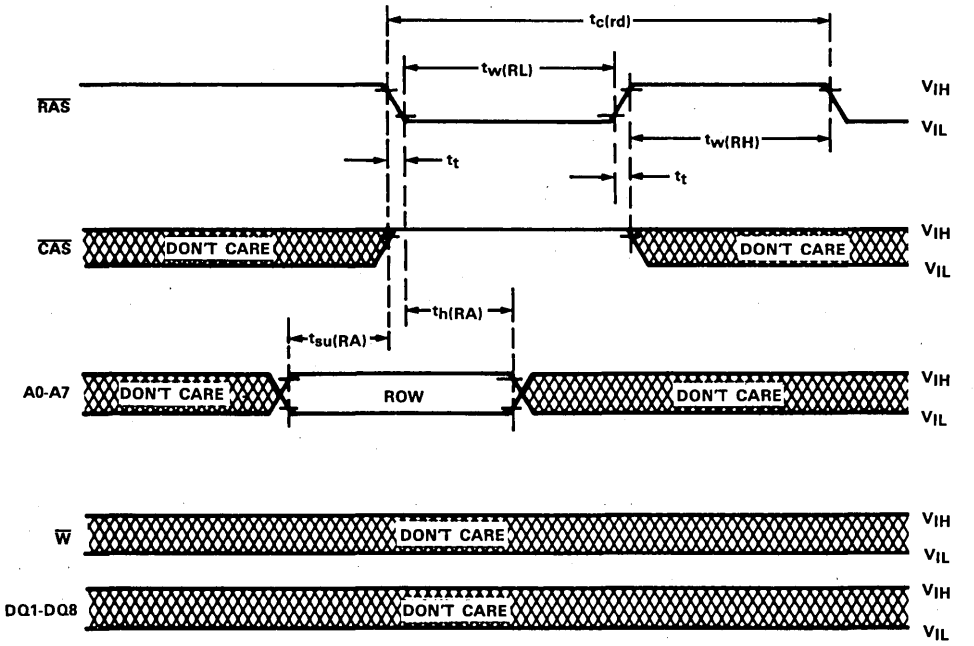
NOTE 5: A write cycle or a read-modify-write cycle can be intermixed with read cycles as long as the write and read-modify-write timing specifications are not violated.

page-mode write cycle timing

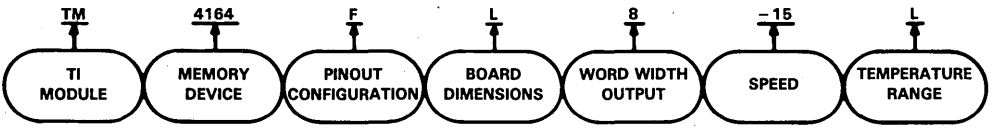


NOTE 6: A read cycle or a read-modify-write can be intermixed with write cycles as long as the read and read-modify-write timing specifications are not violated.

$\overline{\text{RAS}}$-only refresh timing



TI single-in-line package nomenclature



L Package
(76,2 x 16,5 mm)
(3.1 x 0.65 inches)
M Package
(88,9 x 15,24 mm)
(3.5 x 0.60 inches)

Max Access
–12 120 ns
–15 150 ns
–20 200 ns

L 0°C to 70°C

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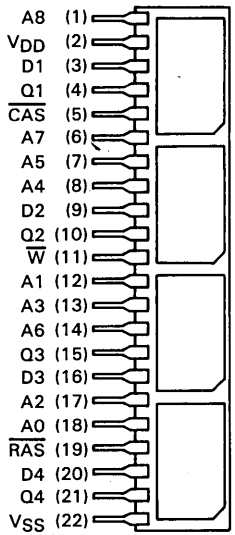
SEPTEMBER 9185 – REVISED NOVEMBER 1985

- 262,144 X 4 Organization
- Single 5-V Supply (10% Tolerance)
- 22-Pin Single-in-Line Package (SIP)
- Utilizes Four 256K Dynamic RAMs in Plastic Chip Carrier
- Long Refresh Period . . . 4 ms (256 Cycles)
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Outputs
- Performance Ranges:

	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	READ-MODIFY-WRITE CYCLE (MIN)
TM425_EC4-12	120 ns	60 ns	230 ns	275 ns
TM425_EC4-15	150 ns	75 ns	260 ns	305 ns
TM425_EC4-20	200 ns	100 ns	330 ns	370 ns

- Common $\overline{CAS}$ Control with Separate Data Input and Output Lines
- Operating Free-Air Temperature . . . 0°C to 70°C
- Downward Compatible with 64K X 4 Single-in-Line Package (TM4164EC4)

C SINGLE-IN-LINE PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A8	Address Inputs
$\overline{CAS}$	Column-Address Strobe
D1-D4	Data Inputs
NC	No Connection
Q1-Q4	Data Outputs
$\overline{RAS}$	Row-Address Strobe
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The TM425_EC4 is a 1024K, dynamic random-access memory module organized as 262,144 × 4 bits in a 22-pin single-in-line package comprising four TMS425_FML, 262,144 × 1 bit dynamic RAM's in 18-lead plastic chip carriers mounted on top of a substrate together with decoupling capacitors mounted beneath the chip carriers. The onboard capacitors eliminate the need for bypassing on the motherboard and offer superior performance over equivalent leaded capacitors due to reduced lead inductance. Also, with 0.3 inch board spacing the TM425_EC4 has a density of ten devices per square inch (approximately 4X the density of DIPs). With the elimination of bypass capacitors on the motherboard, reduced PC board size, and fewer plated-through holes, a cost savings can be realized.

The TM425_EC4 features $\overline{RAS}$ access times of 120 ns, 150 ns, and 200 ns maximum. Power dissipation as low as 900 mW typical operating and 50 mW typical standby.

Refresh period is extended to 4 milliseconds, and during this period each of the 256 rows must be strobed with $\overline{RAS}$ in order to retain data. $\overline{CAS}$ can remain high during the refresh sequence to conserve power.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address lines and data in are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TM425_EC4 is rated for operation from 0°C to 70°C.

operation

address (A0 through A8)

Eighteen address bits are required to decode 1 of 262,144 storage cell locations on each of the four chips. Nine row-address bits are set up on pins A0 through A8 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the nine column-address bits are set up on pins A0 through A8 and latched onto the chip by the column-address strobe. All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data inputs are disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$, the data outs will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data in (D1-D4)

Data is written during a write cycle. The falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latches. These latches can be driven from standard TTL circuits without a pull-up resistor. In the early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal.

data out (Q1-Q4)

The three-state output buffers provide direct TTL compatibility (no pull-up resistor required) with a fan out of two Series 74 TTL loads for each output. Data out is the same polarity as data in. The outputs are in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the outputs go active after the access time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ is satisfied. The outputs become valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low; $\overline{CAS}$ going high returns it to a high-impedance state. In the early write cycle, the outputs are always in the high-impedance state.

refresh

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffers are in the high-impedance state unless $\overline{CAS}$ is applied, the $\overline{RAS}$-only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses (A0 through A7) with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

The $\overline{CAS}$-before-$\overline{RAS}$ refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CLRL}) and holding it low after $\overline{RAS}$ falls (see parameter t_{RLCHR}). For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally.

hidden refresh

Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a "$\overline{RAS}$-only" refresh cycle. The external address is also ignored during the hidden refresh cycles.

page mode (TM4256EC4)

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the module. Thus, the time required to setup and strobe sequential row addresses for the same page is eliminated.

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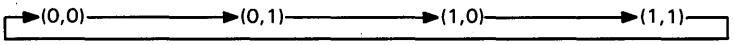
nibble mode (TM4257EC4)

Nibble-mode operation allows high-speed serial read, write, or read-modify-write access of 1 to 4 bits of data. The first bit is accessed in the normal manner with read data coming out at $t_{a(C)}$ time. The next sequential nibble bits can be read or written by cycling $\overline{CAS}$ while $\overline{RAS}$ remains low. The first bit is determined by the row and column addresses, which need to be supplied only for the first access. Column A8 and row A8 (CA8, RA8) provide the two binary bits for initial selection of the nibble addresses. Thereafter, the falling edge of $\overline{CAS}$ will access the next bit of the circular 4-bit nibble in the following sequence:



In nibble-mode, all normal memory operations (read, write, or ready-modify-write) may be performed in any desired combination.

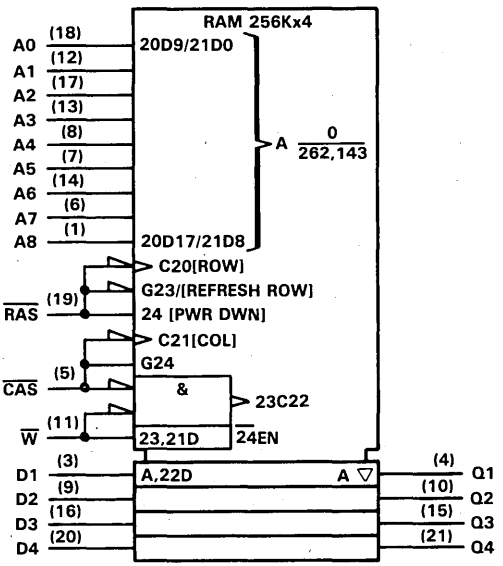
power up

To achieve proper device operation, an initial pause of 200 μs is required after power up followed by a minimum of eight initialization cycles.

single-in-line package and components

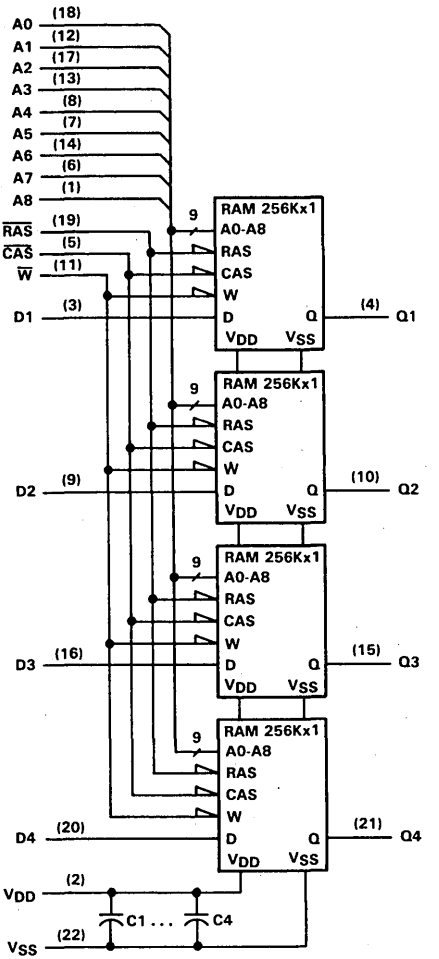
PC substrate: 0,79 mm (0.031 inch) minimum thickness
Bypass capacitors: Multilayer ceramic
Leads: Tin/lead solder coated over phosphor-bronze

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range for any pin except V_{DD} and data out (see Note 1) . . . . . −1.5 V to 10 V
Voltage range on V_{DD} supply and data out with respect to V_{SS} . . . . . −1 V to 7 V
Short circuit output current for any output . . . . . 50 mA
Power dissipation . . . . . 4 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	−1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TM425_EC4-12			TM425_EC4-15			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4		V_{DD}	2.4		V_{DD}	V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA	0		0.4	0		0.4	V
I_I	Input current (leakage)	V_I = 0 V to 6.5 V, V_{DD} = 5 V, All other pins = 0 V			±10			±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10			±10	μA
I_{DD1}	Average operating current during read or write cycle	t_c = minimum cycle, All outputs open		260	312		220	272	mA
I_{DD2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, All outputs open		10	18		10	18	mA
I_{DD3}	Average refresh current	t_c = minimum cycle, $\overline{CAS}$ high and $\overline{RAS}$ cycling, All outputs open		180	240		160	212	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low and $\overline{CAS}$ cycling, All outputs open		140	192		120	172	mA
I_{DD5}	Average nibble-mode current	$t_{c(N)}$ = minimum cycle, $\overline{RAS}$ low and $\overline{CAS}$ cycling, All outputs open		128	176		108	156	mA

†All typical values are at T_A = 25°C and nominal supply voltages.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TM425_EC4-20			UNIT
			MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4		V_{DD}	V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA	0		0.4	V
I_I	Input current (leakage)	V_I = 0 V to 6.5 V, V_{DD} = 5 V, All other pins = 0 V			±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10	μA
I_{DD1}	Average operating current during read or write cycle	t_c = minimum cycle, All outputs open		180	232	mA
I_{DD2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, All outputs open		10	18	mA
I_{DD3}	Average refresh current	t_c = minimum cycle, $\overline{CAS}$ high and $\overline{RAS}$ cycling, All outputs open		140	192	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low and $\overline{CAS}$ cycling, All outputs open		100	140	mA
I_{DD5}	Average nibble-mode current	$t_{c(N)}$ = minimum cycle, $\overline{RAS}$ low and $\overline{CAS}$ cycling, All outputs open		88	128	mA

†All typical values are at T_A = 25°C and nominal supply voltages.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		28	pF
$C_{i(D)}$	Input capacitance, data inputs		28	pF
$C_{i(RAS)}$	Input capacitance, $\overline{RAS}$ input		32	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$ input		32	pF
$C_{i(CAS)}$	Input capacitance, $\overline{CAS}$ input		32	pF
$C_{o(Q)}$	Output capacitance, data outputs		40	pF
$C_{o(VDD)}$	Decoupling capacitance	0.4		μF

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switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TM425_EC4-12		TM425_EC4-15		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		60		75	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, Load = 2 Series 74 TTL gates	t_{RAC}		120		150	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	35	0	35	ns

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TM425_EC4-20		UNIT
				MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		100	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, Load = 2 Series 74 TTL gates	t_{RAC}		200	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	35	ns

timing requirements over recommended supply voltage range and operating free-air temperature range

		ALT. SYMBOL	TM425_EC4-12 MIN	TM425_EC4-12 MAX	UNIT
$t_{c(P)}$	Page-mode cycle time (read or write cycle)	t_{PC}	120		ns
$t_{c(PM)}$	Page-mode cycle time (read-modify-write cycle)	t_{PCM}	165		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	230		ns
$t_{c(W)}$	Write cycle time	t_{WC}	230		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	275		ns
$t_{w(CH)P}$	Pulse duration, $\overline{CAS}$ high (page mode)	t_{CP}	50		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (non-page mode)	t_{CPN}	25		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low‡	t_{CAS}	60	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high	t_{RP}	100		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low§	t_{RAS}	120	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	40		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		ns
$t_{su(WCL)}$	Early write-command setup time before $\overline{CAS}$ low	t_{WCS}	0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	40		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	40		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	20		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	15		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	80		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DHC}	35		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	95		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DHW}	35		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	10		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	35		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	95		ns

Continued next page.

NOTE 3: Timing measurements are referenced to V_{IL} max and V_{IH} min.

†All cycle times assume t_t = 5 ns.

‡In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$). This applies to page-mode read-modify-write also.

§In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).

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timing requirements over recommended supply voltage range and operating free-air temperature range (continued)

		ALT. SYMBOL	TMS425_EC4-12		UNIT
			MIN	MAX	
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	120		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	60		ns
t_{RLCHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high¶	t_{CHR}	25		ns
t_{CLRL}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low¶	t_{CSR}	25		ns
t_{RHCL}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low¶	t_{RPC}	20		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{CWD}	60		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	25	60	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{RWD}	120		ns
t_{rf}	Refresh time interval	t_{REF}		4	ms

Continued next page.

NOTE 3: Timing measurements are referenced to V_{IL} max and V_{IH} min.

¶$\overline{CAS}$-before-$\overline{RAS}$ refresh only.

timing requirements over recommended supply voltage range and operating free-air temperature range (continued)

		ALT. SYMBOL	TM425_EC4-15		TM425_EC4-20		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(P)}$	Page-mode cycle time (read or write cycle)	t_{PC}	145		190		ns
$t_{c(PM)}$	Page-mode cycle time (read-modify-write cycle)	t_{PCM}	190		245		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	260		330		ns
$t_{c(W)}$	Write cycle time	t_{WC}	260		330		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	305		370		ns
$t_{w(CH)P}$	Pulse duration, $\overline{CAS}$ high (page mode)	t_{CP}	60		80		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (non-page mode)	t_{CPN}	25		30		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low‡	t_{CAS}	75	10,000	100	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high	t_{RP}	100		120		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low§	t_{RAS}	150	10,000	200	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	45		55		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	50	3	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		0		ns
$t_{su(WCL)}$	Early write-command setup time before $\overline{CAS}$ low	t_{WCS}	0		0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	45		60		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	45		60		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	25		30		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	15		20		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	100		130		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DHC}	45		55		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	120		155		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DHW}	45		55		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	10		15		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	45		55		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	120		155		ns

Continued next page.

NOTE 3: Timing measurements are referenced to V_{IL} max and V_{IH} min.

†All cycle times assume t_t = 5 ns.

‡In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time $t_{w(CL)}$. This applies to page-mode read-modify-write also.

§In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).

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timing requirements over recommended supply voltage range and operating free-air temperature range (concluded)

		ALT. SYMBOL	TM425_EC4-15		TM425_EC4-20		UNIT
			MIN	MAX	MIN	MAX	
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	150		200		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	75		100		ns
t_{RLCHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high¶	t_{CHR}	30		35		ns
t_{CLRL}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low¶	t_{CSR}	30		35		ns
t_{RHCL}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low¶	t_{RPC}	20		25		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{CWD}	70		90		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	25	75	30	100	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{RWD}	145		190		ns
t_{rf}	Refresh time interval	t_{REF}		4		4	ms

NOTE 3: Timing measurements are referenced to V_{IL} max and V_{IH} min.
¶$\overline{CAS}$-before-$\overline{RAS}$ refresh only.

NIBBLE-MODE CYCLE

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		ALT. SYMBOL	TM4257EC4-12		TM4257EC4-15		TM4257EC4-20		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(CN)}$	Nibble-mode access time from $\overline{CAS}$	t_{NCAC}		30		40		50	ns

timing requirements over recommended supply voltage range and operating free-air temperature range

		ALT. SYMBOL	TM4257EC4-12		TM4257EC4-15		TM4257EC4-20		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(N)}$	Nibble-mode cycle time	t_{NC}	60		75		90		ns
$t_{c(rdWN)}$	Nibble-mode read-modify-write cycle time	t_{NRMW}	85		105		130		
t_{CLRHN}	Nibble-mode delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{NRSH}	30		40		50		
t_{CLWLN}	Nibble-mode delay time, $\overline{CAS}$ to $\overline{W}$ delay	t_{NCWD}	25		30		40		
$t_{w(CLN)}$	Nibble-mode pulse duration, $\overline{CAS}$ low	t_{NCAS}	30		40		50		
$t_{w(CHN)}$	Nibble-mode pulse duration, $\overline{CAS}$ high	t_{NCP}	20		25		30		
$t_{w(CRWN)}$	Nibble-mode read-modify-write pulse duration, $\overline{CAS}$ low	t_{NCRW}	55		70		90		
$t_{su(WCHN)}$	Nibble-mode write command setup time before $\overline{CAS}$ high	t_{NCWL}	25		35		45		

PARAMETER MEASUREMENT INFORMATION

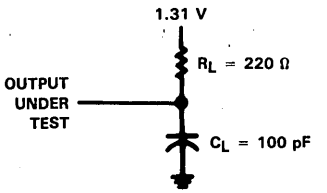
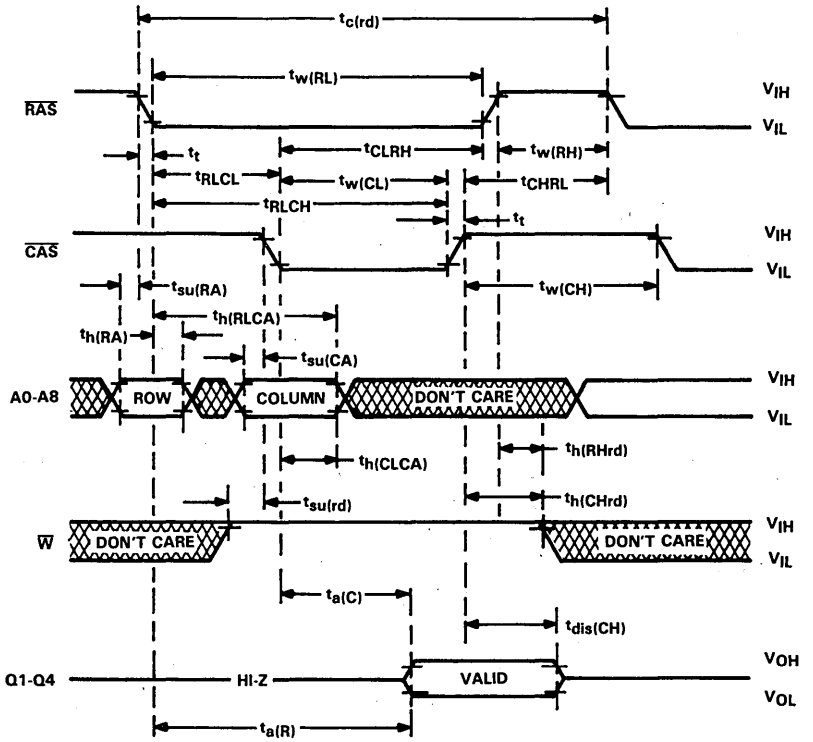


FIGURE 1. LOAD CIRCUIT

read cycle timing



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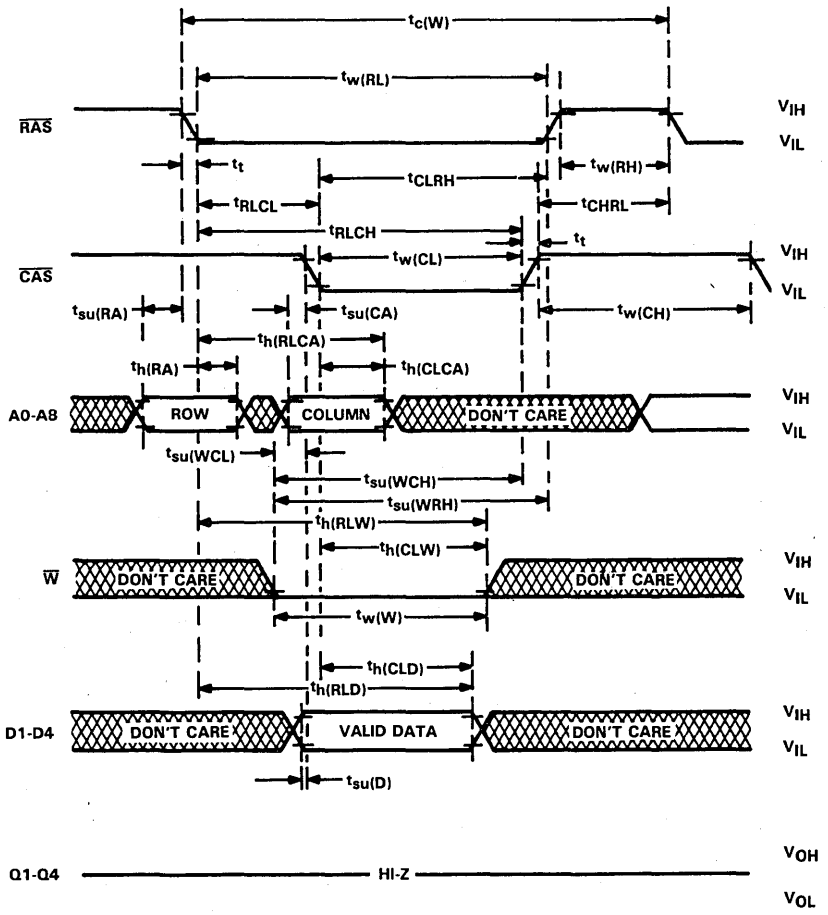
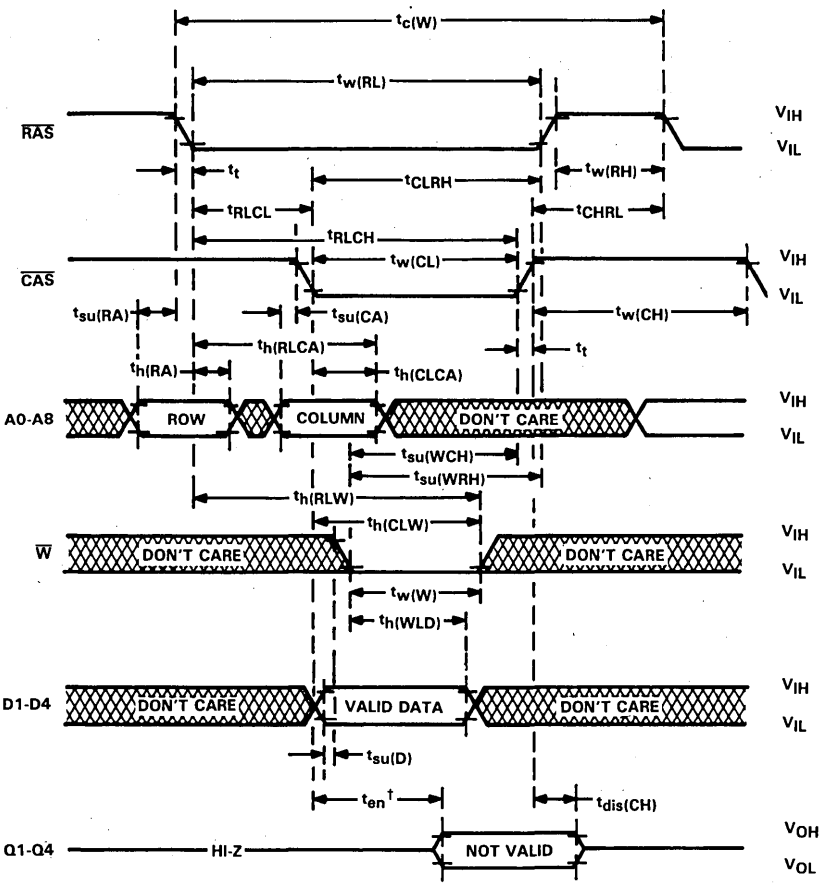
early write cycle timing



write cycle timing



†The enable time (t_{en}) for a write cycle is equal in duration to the access time from $\overline{CAS}$ ($t_{a(C)}$) in a read cycle; but the active levels at the output are invalid.

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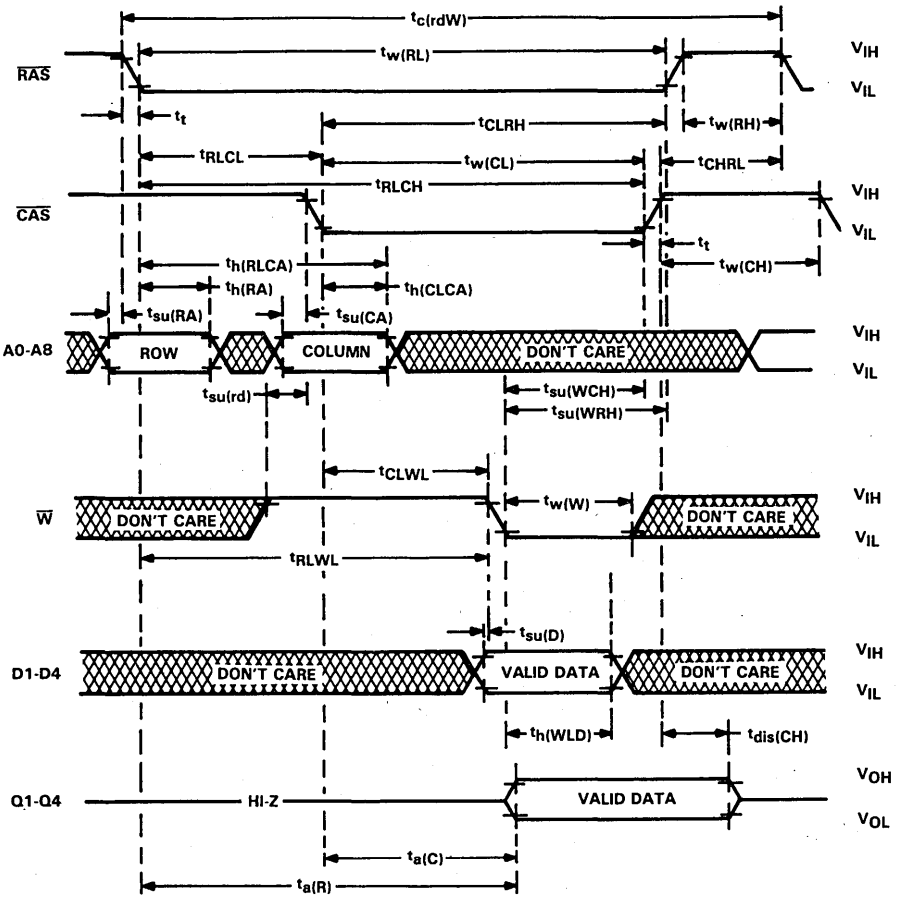
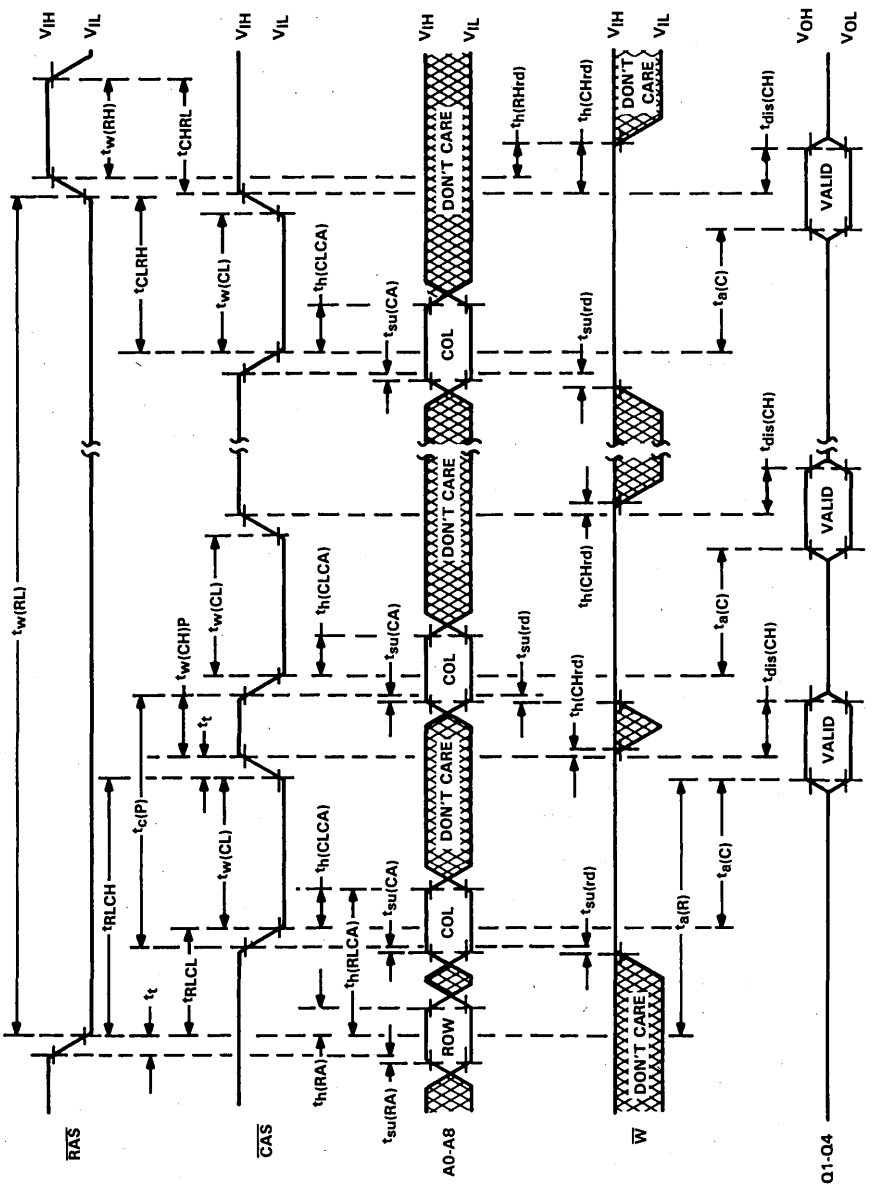
read-write/read-modify-write cycle timing

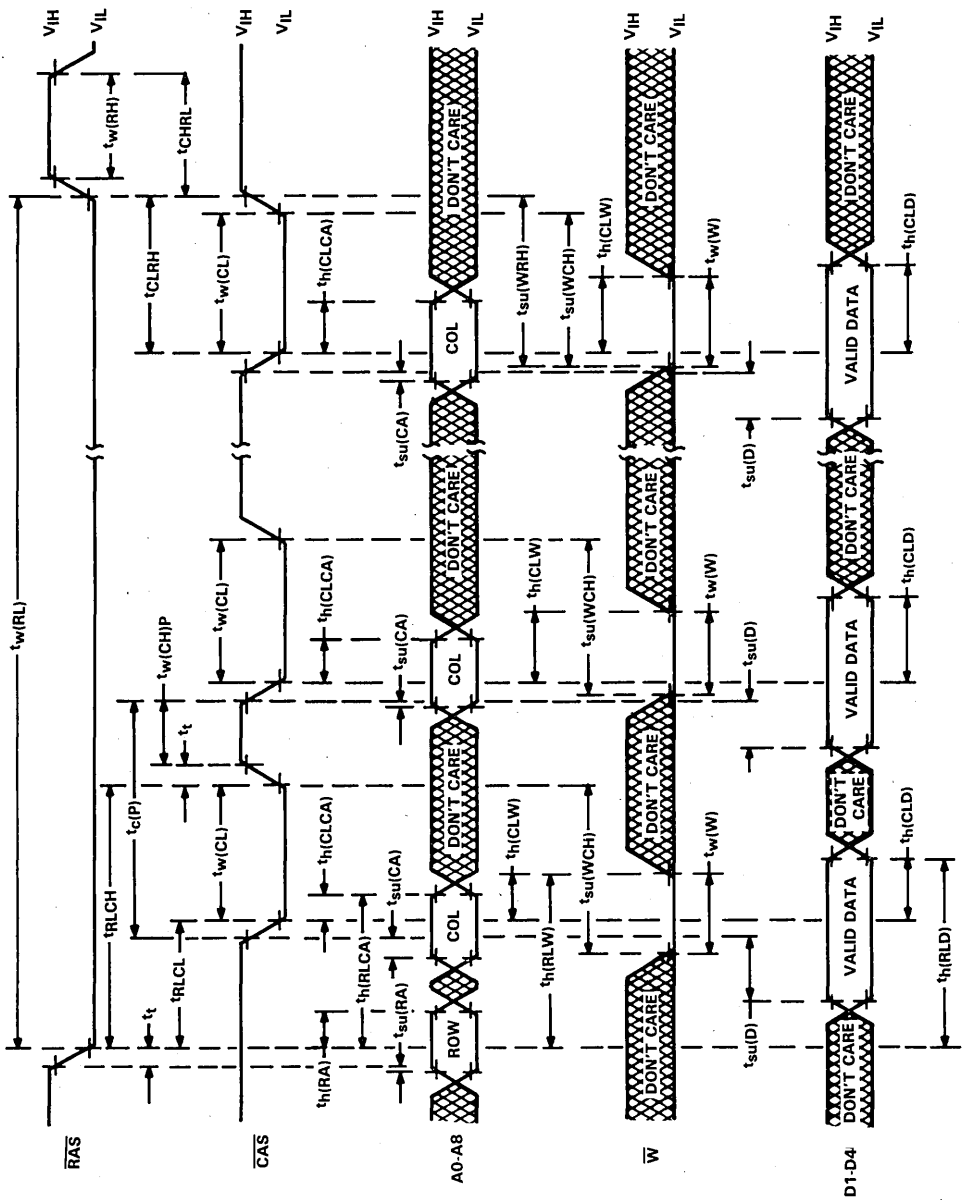


page-mode read cycle timing



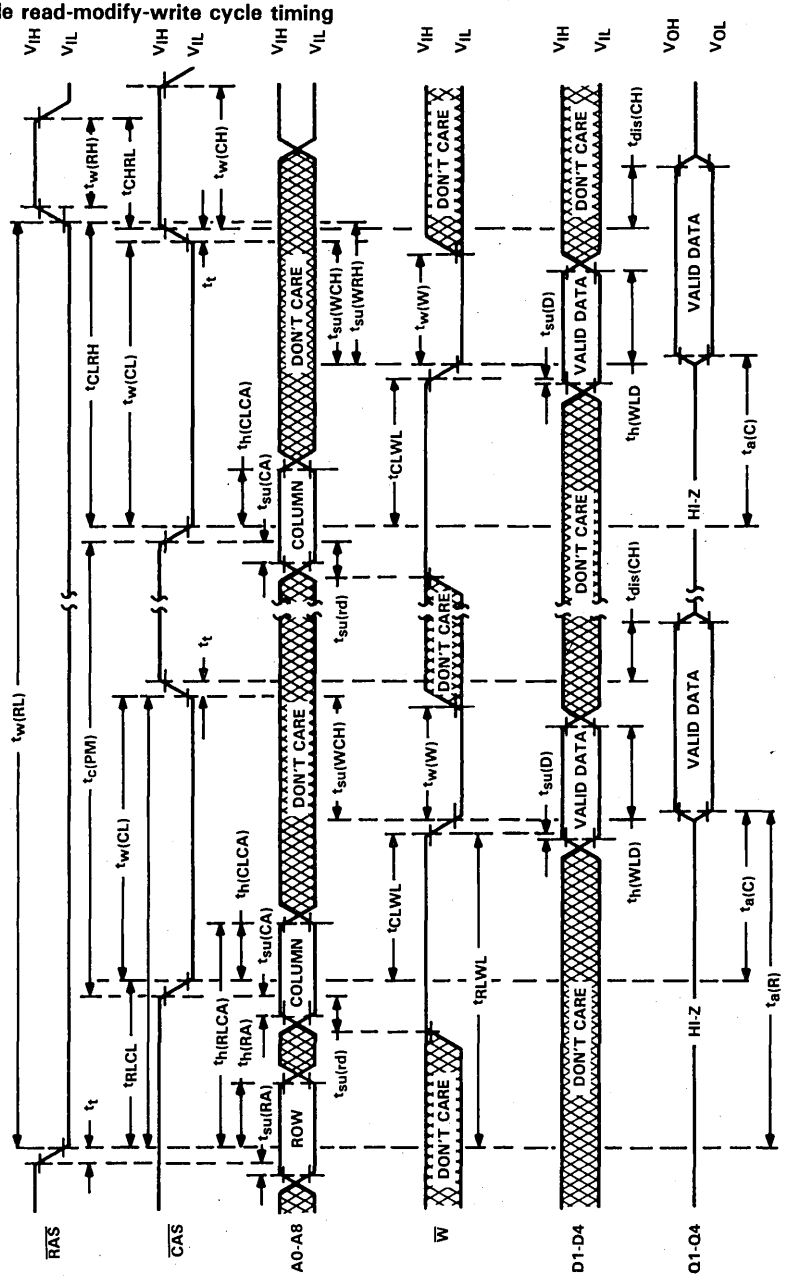
NOTE 4: A write cycle or a read-modify-write cycle can be intermixed with read cycles as long as the write and read-modify write timing specifications are not violated.

page-mode write cycle timing



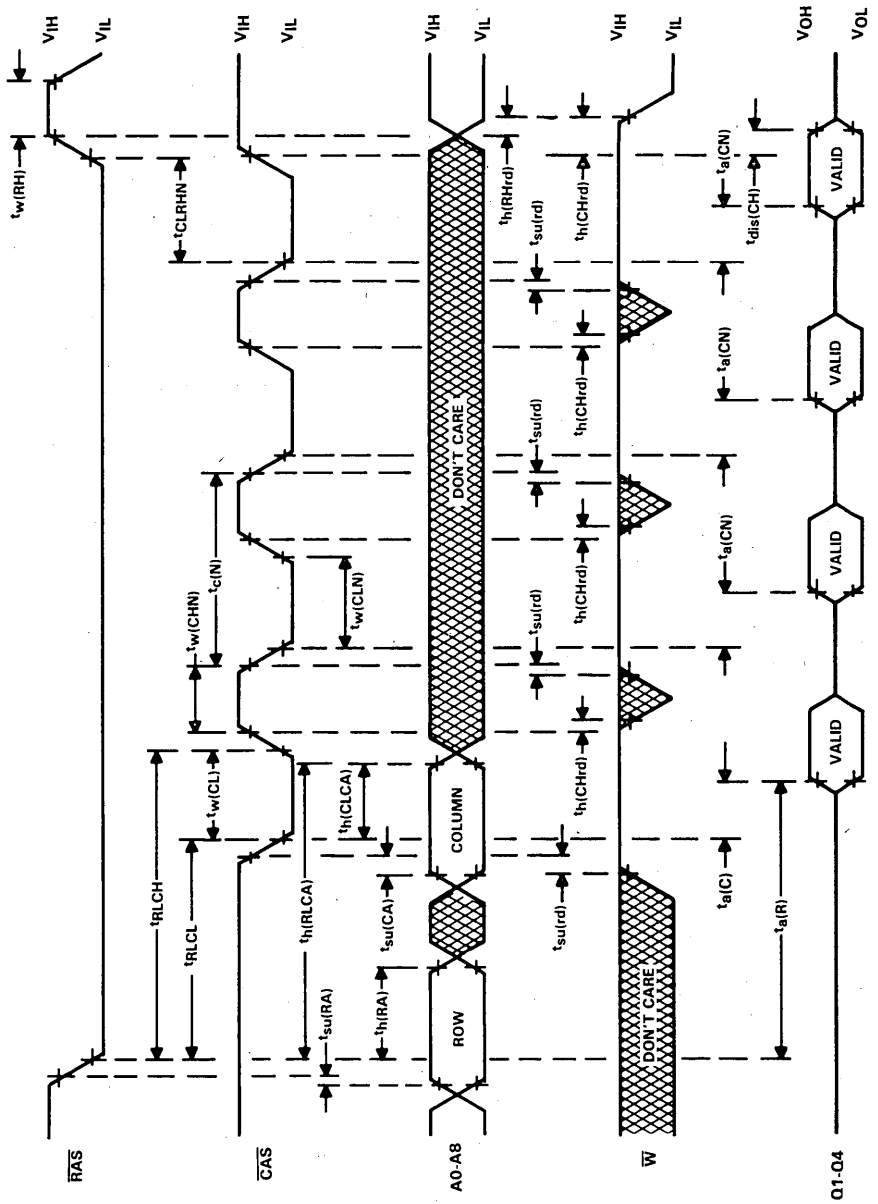
NOTE 5: A read cycle or a read-modify-write cycle can be intermixed with write cycles as long as read and read-modify-write timing specifications are not violated.

page-mode read-modify-write cycle timing

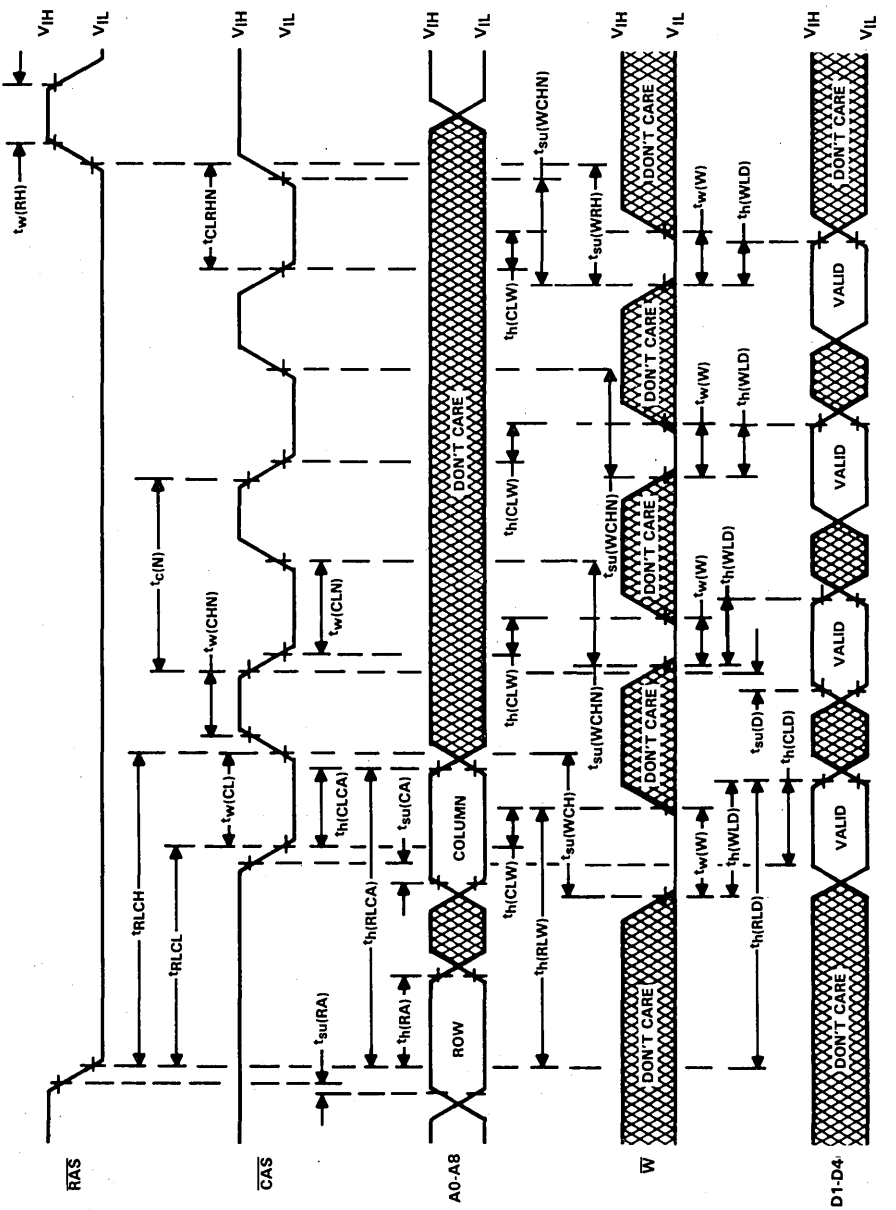


NOTE 6: A read or a write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

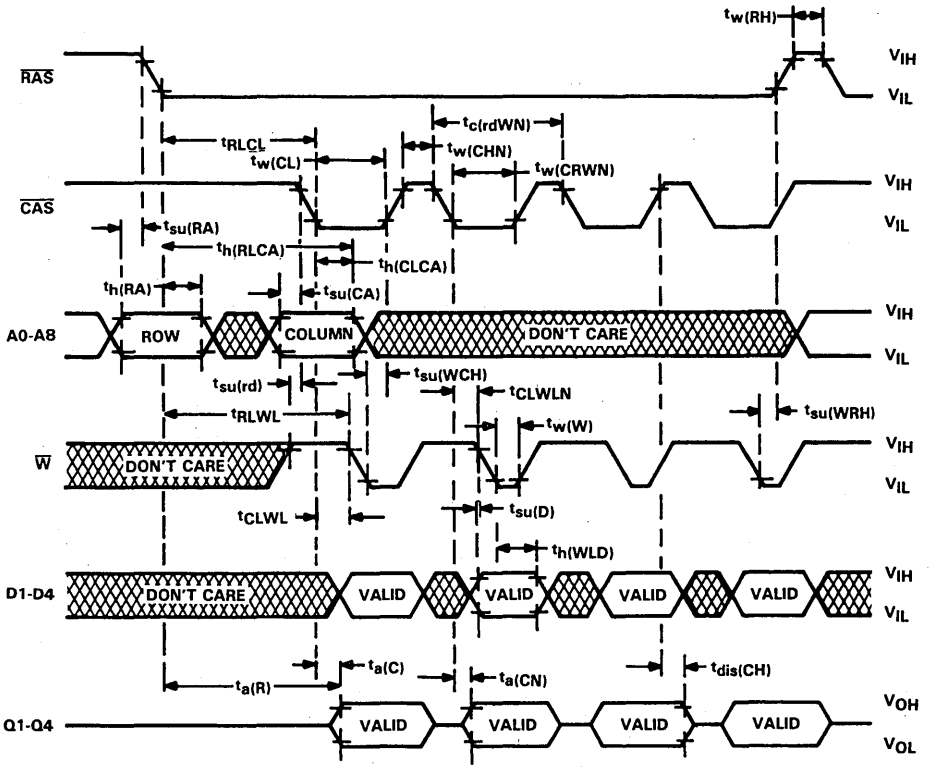
nibble-mode read cycle timing



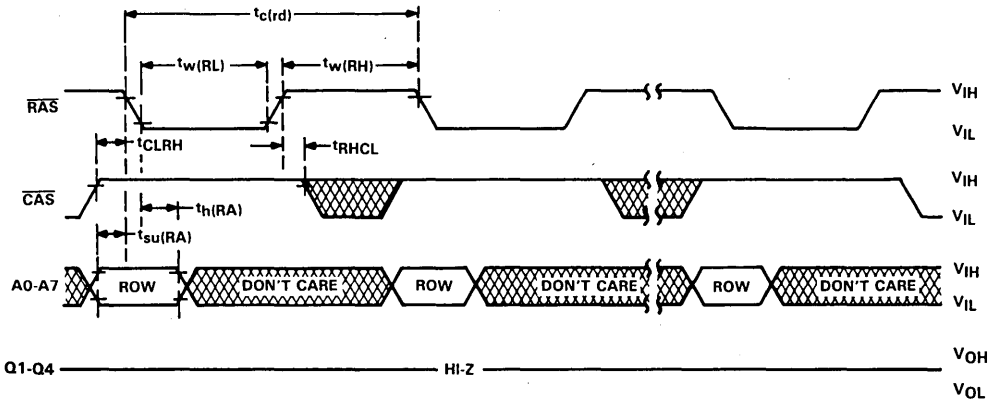
nibble-mode write cycle timing



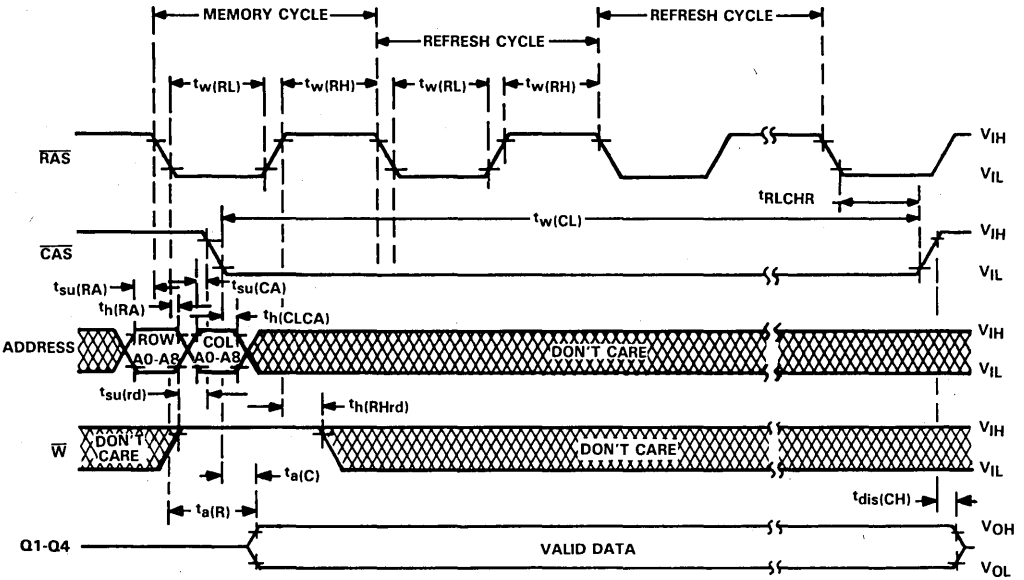
nibble-mode read-modify-write-cycle timing



$\overline{RAS}$-only refresh cycle timing



hidden refresh cycle timing



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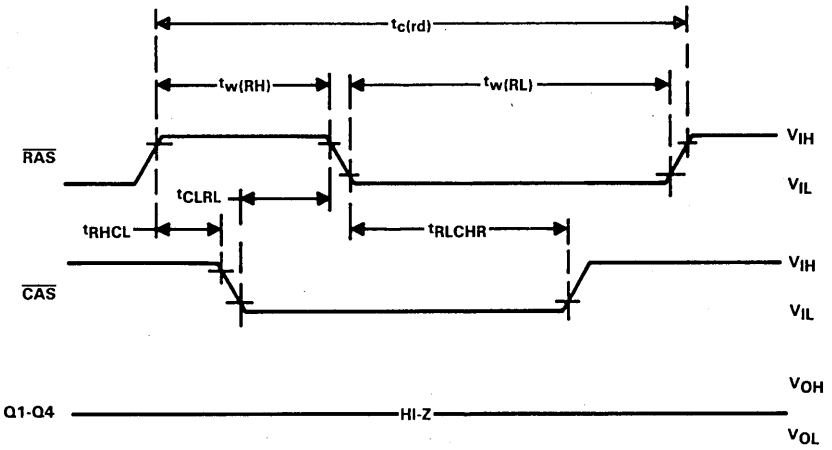
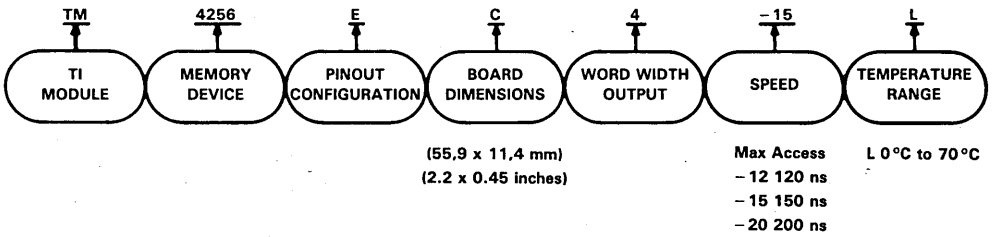
automatic ($\overline{CAS}$-before-$\overline{RAS}$) refresh cycle timing



TI single-in-line package nomenclature



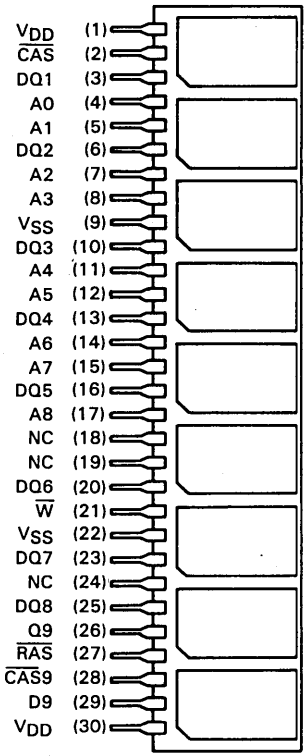
SEPTEMBER 1985 — REVISED NOVEMBER 1985

- 262,144 X 9 Organization
- Single 5-V Supply (10% Tolerance)
- 30-Pin Single-in-Line Package (SIP)
  - —Pinned Module for Through-Hole Insertion (TM425_EL9)
  - —Leadless Module for Use with Sockets (TM425_GU9)
- Utilizes Nine 256K Dynamic RAMs in Plastic Chip Carrier
- Long Refresh Period . . . 4 ms (256 Cycles)
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Outputs
- Performance Ranges:

	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)
TM425___9-12	120 ns	60 ns	230 ns
TM425___9-15	150 ns	75 ns	260 ns
TM425___9-20	200 ns	100 ns	330 ns

- Common $\overline{CAS}$ Control for Eight Common Data-In and Data-Out Lines
- Separate $\overline{CAS}$ Control for One Separate Pair of Data-In and Data-Out Lines
- Low Power Dissipation
- Operating Free-Air Temperature . . . 0°C to 70°C
- Downward Compatible with 64K X 9 SIP (TM4164EL9, TM4164FM9)

TM425_EL9 . . . L SINGLE-IN-LINE PACKAGE
(TOP VIEW)



description

The TM425___9 series are 2304K, dynamic random-access memory modules organized as 262,144 × 9 bits [bit nine (D9, Q9) is generally used for parity and is controlled by $\overline{CAS9}$] in a 30-pin single-in-line package comprising nine TMS425_FML, 262,144 × 1 bit dynamic RAM's in 18-lead plastic chip carriers mounted on top of a substrate together with decoupling capacitors mounted beneath the chip carriers. The onboard capacitors eliminate the need for bypassing on the motherboard and offer superior performance over equivalent leaded capacitors due to reduced lead inductance. Also, with 0.3

PIN NOMENCLATURE TM425_EL9	
A0-A8	Address Inputs
$\overline{CAS}$, $\overline{CAS9}$	Column-Address Strobes
DQ1-DQ8	Data In/Data Out
D9	Data In
NC	No Connection
Q9	Data Out
$\overline{RAS}$	Row-Address Strobe
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

inch board spacing the TM425___9 has a density of ten devices per square inch (approximately 4X the density of DIPs). With the elimination of bypass capacitors on the motherboard, reduced PC board size, and fewer plated-through holes, a cost savings can be realized.

The TM425___9 features $\overline{RAS}$ access times of 120 ns, 150 ns, and 200 ns maximum. Power dissipation as low as 2025 mW typical operating and 115 mW typical standby for 200 ns devices.

Refresh period is extended to 4 milliseconds, and during this period each of the 256 rows must be strobed with $\overline{RAS}$ in order to retain data. $\overline{CAS}$ can remain high during the refresh sequence to conserve power.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address lines and data in are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TM425___9 is rated for operation from 0°C to 70°C.

presence detect

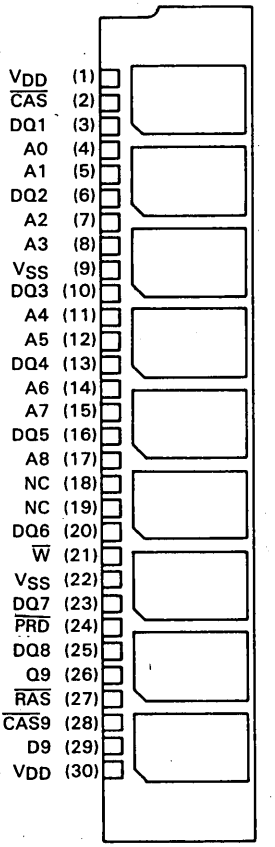
This feature is included on the TM425_GU9 to allow for hardware presence detection of the memory module. The $\overline{PRD}$ pin for each module in the system should be pulled high through a pull-up resistor, resulting in a logic one when no module is present. When a module is present, $\overline{PRD}$ is a logic zero as this pin is connected to V_{SS} on the module. $\overline{PRD}$ can only be used to detect a modules' presence, not its functionality. In a system not requiring presence detect, it is recommended that this pin be left as a no connect; this allows the use of either type of module without adverse effects.

operation

address (A0 through A8)

Eighteen address bits are required to decode 1 of 262,144 storage cell locations on each of the nine chips. Nine row-address bits are set up on pins A0 through A8 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the nine column-address bits are set up on pins A0 through A8 and latched onto the chip by the

TM425_GU9 . . . U SINGLE-IN-LINE PACKAGE
(TOP VIEW)



PIN NOMENCLATURE TM425_GU9	
A0-A8	Address Inputs
$\overline{CAS}$, $\overline{CAS9}$	Column-Address Strobes
DQ1-DQ8	Data In/Data Out
D9	Data In
NC	No Connection
$\overline{PRD}$	Presence Detect (V_{SS})
Q9	Data Out
$\overline{RAS}$	Row-Address Strobe
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

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column-address strobes ($\overline{CAS}$ for M1 thru M8 and $\overline{CAS}$9 for M9). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers for M1-M8. $\overline{CAS}$9 is used similarly for M9.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data inputs are disabled when the read mode is selected. The common I/O feature of the TM425___9 dictates the use of early write cycles to prevent contention on D and Q. When $\overline{W}$ goes low prior to $\overline{CAS}$, the data outs will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data in (DQ1-DQ8, D9)

Data is written during a write cycle. The falling edge of $\overline{CAS}$ strobes data into the on-chip data latches. These latches can be driven from standard TTL circuits without a pull-up resistor. In the early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal.

data out (DQ1-DQ8, D9)

The three-state output buffers provide direct TTL compatibility (no pull-up resistor required) with a fan out of two Series 74 TTL loads for each output. Data out is the same polarity as data in. The outputs are in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the outputs go active after the access time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ is satisfied. The outputs become valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low: $\overline{CAS}$ going high returns it to a high-impedance state. In the early write cycle, the outputs are always in the high-impedance state, a necessity due to the common I/O feature of the TM425___9.

refresh

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffers are in the high-impedance state unless $\overline{CAS}$ is applied, the $\overline{RAS}$-only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses (A0 through A7) with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

The $\overline{CAS}$-before-$\overline{RAS}$ refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CLRL}) and holding it low after $\overline{RAS}$ falls (see parameter t_{RLCHR}). For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally.

hidden refresh

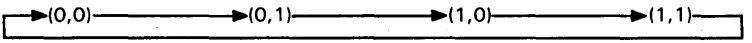
Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a "$\overline{RAS}$-only" refresh cycle. The external address is also ignored during the hidden refresh cycles.

page-mode (TM4256__9)

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the module. Thus, the time required to setup and strobe sequential row addresses for the same page is eliminated.

nibble mode (TM4257__9)

Nibble-mode operation allows high-speed serial read, write, or read-modify-write access of 1 to 4 bits of data. The first bit is accessed in the normal manner with read data coming out at $t_{a(C)}$ time. The next sequential nibble bits can be read or written by cycling $\overline{CAS}$ while $\overline{RAS}$ remains low. The first bit is determined by the row and column addresses, which need to be supplied only for the first access. Column A8 and row A8 (CA8, RA8) provide the two binary bits for initial selection of the nibble addresses. Thereafter, the falling edge of $\overline{CAS}$ will access the next bit of the circular 4-bit nibble in the following sequence:



In nibble-mode, all normal memory operations (read, write, or ready-modify-write) may be performed in any desired combination.

power up

To achieve proper operation, an initial pause of 200 μs is required after power up followed by a minimum of eight initialization cycles.

single-in-line package and components

PC substrate: 0,79 mm (0.031 inch) minimum thickness
Bypass capacitors: Multilayer ceramic
Leads: Tin/lead solder coated over phosphor-bronze
Contact area for socketable devices: Nickel plate and solder plate on top of copper

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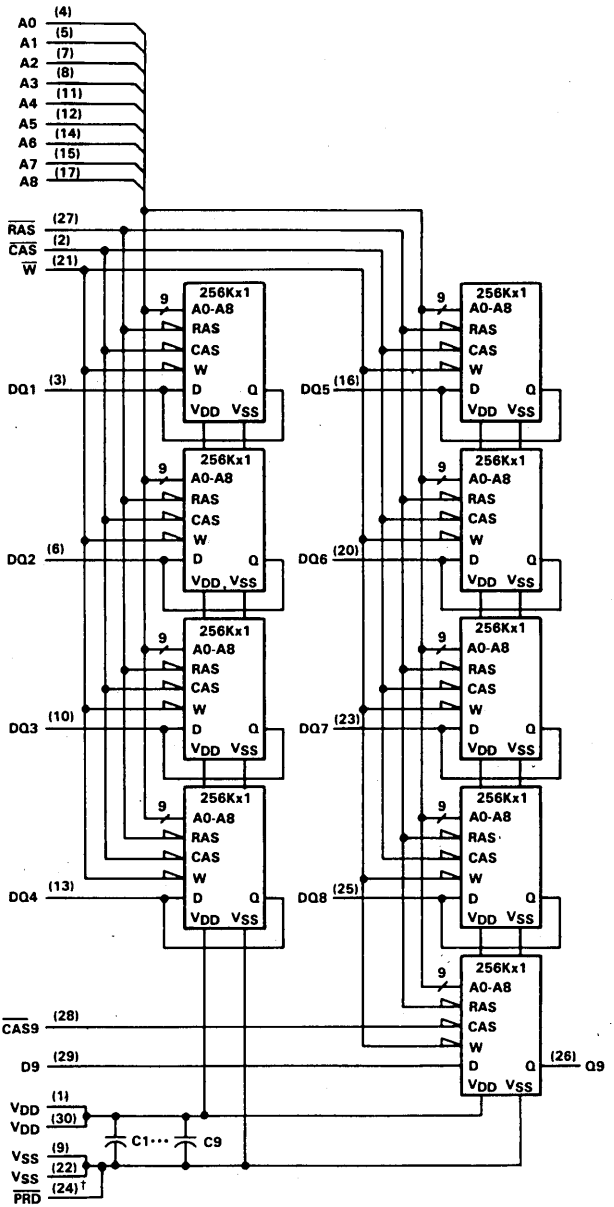
functional block diagram



†TM425_GU9 only.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range for any pin except V_{DD} and data out (see Note 1) . . . . . −1.5 V to 10 V
Voltage range on V_{DD} supply and data out with respect to V_{SS} . . . . . −1 V to 7 V
Short circuit output current for any output . . . . . 50 mA
Power dissipation . . . . . 9 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	−1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TM425___9-12			TM425___9-15			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4		V_{DD}	2.4		V_{DD}	V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA	0		0.4	0		0.4	V
I_I	Input current (leakage)	V_I = 0 V to 6.5 V, V_{DD} = 5 V, All other pins = 0 V			±10			±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10			±10	μA
I_{DD1}‡	Average operating current during read or write cycle	t_c = minimum cycle, All outputs open		585	702		495	612	mA
I_{DD2}‡	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, All outputs open		23	41		23	41	mA
I_{DD3}‡	Average refresh current	t_c = minimum cycle, $\overline{CAS}$ high and $\overline{RAS}$ cycling, All outputs open		405	540		360	477	mA
I_{DD4}‡	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low and $\overline{CAS}$ cycling, All outputs open		315	432		270	387	mA
I_{DD5}‡	Average nibble-mode current	$t_{c(N)}$ = minimum cycle, $\overline{RAS}$ low and $\overline{CAS}$ cycling, All outputs open		288	396		243	351	mA

†All typical values are at T_A = 25°C and nominal supply voltages.
‡I_{DD1}-I_{DD5} are measured with M1-M9 in the same mode (i.e., operating, standby, refresh, page mode, nibble mode).

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electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TM425___9-20			UNIT
			MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4		V_{DD}	V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA	0		0.4	V
I_I	Input current (leakage)	V_I = 0 V to 6.5 V, V_{DD} = 5 V, All other pins = 0 V			±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10	μA
I_{DD1}‡	Average operating current during read or write cycle	t_c = minimum cycle, All outputs open		405	522	mA
I_{DD2}‡	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, All outputs open		23	41	mA
I_{DD3}‡	Average refresh current	t_c = minimum cycle, $\overline{CAS}$ high and $\overline{RAS}$ cycling, All outputs open		315	432	mA
I_{DD4}‡	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low and $\overline{CAS}$ cycling, All outputs open		225	315	mA
I_{DD5}‡	Average nibble-mode current	$t_{c(N)}$ = minimum cycle, $\overline{RAS}$ low and $\overline{CAS}$ cycling, All outputs open		198	288	mA

†All typical values are at T_A = 25°C and nominal supply voltages.
‡I_{DD1}-I_{DD5} are measured with M1-M9 in the same mode (i.e., operating, standby, refresh, page mode, nibble mode).

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		63	pF
$C_{i(DQ)}$	Input capacitance, data inputs		17	pF
$C_{i(RAS)}$	Input capacitance, $\overline{RAS}$ input		72	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$ input		72	pF
$C_{i(CAS9)}$	Input capacitance, $\overline{CAS}$9 input		8	pF
$C_{i(CAS)}$	Input capacitance, $\overline{CAS}$ input		64	pF
$C_{i(D9)}$	Input capacitance, D9 input		7	pF
$C_{o(Q9)}$	Output capacitance, Q9 output		10	pF
$C_{o(VDD)}$	Decoupling capacitance	0.8		μF

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TM425___9-12		TM425___9-15		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		60		75	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, Load = 2 Series 74 TTL gates	t_{RAC}		120		150	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	35	0	35	ns

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TM425___9-20		UNIT
				MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		100	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, Load = 2 Series 74 TTL gates	t_{RAC}		200	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	35	ns

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timing requirements over recommended supply voltage range and operating free-air temperature range

		ALT. SYMBOL	TM425___9-12 MIN	TM425___9-12 MAX	UNIT
$t_{c(P)}$	Page-mode cycle time (read or write cycle)	t_{PC}	120		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	230		ns
$t_{c(W)}$	Write cycle time	t_{WC}	230		ns
$t_{w(CH)P}$	Pulse duration, $\overline{CAS}$ high (page mode)	t_{CP}	50		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (non-page mode)	t_{CPN}	25		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low	t_{CAS}	60	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge time)	t_{RP}	100		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low	t_{RAS}	120	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	40		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		ns
$t_{su(WCL)}$	Early write-command setup time before $\overline{CAS}$ low	t_{WCS}	0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	40		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	40		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	20		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	15		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	80		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	35		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	95		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	10		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	35		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	95		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	120		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	60		ns
t_{RLCHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high‡	t_{CHR}	25		ns
t_{CLRL}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low‡	t_{CSR}	25		ns
t_{RHCL}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low‡	t_{RPC}	20		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	30	60	ns
t_{rf}	Refresh time interval	t_{REF}		4	ms

NOTE 3: Timing measurements are referenced to V_{IL} max and V_{IH} min.
†All cycle times assume t_t = 5 ns.
‡$\overline{CAS}$-before-$\overline{RAS}$ refresh only.

timing requirements over recommended supply voltage range and operating free-air temperature range

		ALT. SYMBOL	TM425___9-15		TM425___9-20		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(P)}$	Page-mode cycle time (read or write cycle)	t_{PC}	145		190		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	260		330		ns
$t_{c(W)}$	Write cycle time	t_{WC}	260		330		ns
$t_{w(CH)P}$	Pulse duration, $\overline{CAS}$ high (page mode)	t_{CP}	60		80		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (non-page mode)	t_{CPN}	25		30		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low	t_{CAS}	75	10,000	100	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge time)	t_{RP}	100		120		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low	t_{RAS}	150	10,000	200	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	45		55		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	50	3	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		0		ns
$t_{su(WCL)}$	Early write-command setup time before $\overline{CAS}$ low	t_{WCS}	0		0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	45		60		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	45		60		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	25		30		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	15		20		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	100		130		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	45		55		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	120		155		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	10		15		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	45		55		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	120		155		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	150		200		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	75		100		ns
t_{RLCHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high‡	t_{CHR}	30		35		ns
t_{CLRL}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low‡	t_{CSR}	30		35		ns
t_{RHCL}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low‡	t_{RPC}	20		25		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	30	75	30	100	ns
t_{rf}	Refresh time interval	t_{REF}		4		4	ms

NOTE 3: Timing measurements are referenced to V_{IL} max and V_{IH} min.
†All cycle times assume t_t = 5 ns.
‡$\overline{CAS}$-before-$\overline{RAS}$ refresh only.

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NIBBLE-MODE CYCLE

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		ALT. SYMBOL	TM4257__9-12		TM4257__9-15		TM4257__9-20		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(CN)}$	Nibble-mode access time from $\overline{CAS}$	t_{NCAC}		30		40		50	ns

timing requirements over recommended supply voltage range and operating free-air temperature range

		ALT. SYMBOL	TM4257__9-12		TM4257__9-15		TM4257__9-20		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(N)}$	Nibble-mode cycle time	t_{NC}	60		75		90		ns
t_{CLRHN}	Nibble-mode delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{NRSH}	30		40		50		
t_{CLWLN}	Nibble-mode delay time, $\overline{CAS}$ to $\overline{W}$ delay	t_{NCWD}	25		30		40		
$t_{w(CLN)}$	Nibble-mode pulse duration, $\overline{CAS}$ low	t_{NCAS}	30		40		50		
$t_{w(CHN)}$	Nibble-mode pulse duration, $\overline{CAS}$ high	t_{NCP}	20		25		30		
$t_{su(WCHN)}$	Nibble-mode write command setup time before $\overline{CAS}$ high	t_{NCWL}	25		35		45		

PARAMETER MEASUREMENT INFORMATION

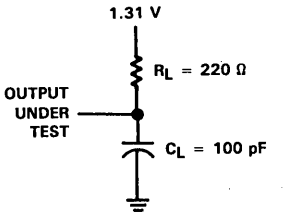
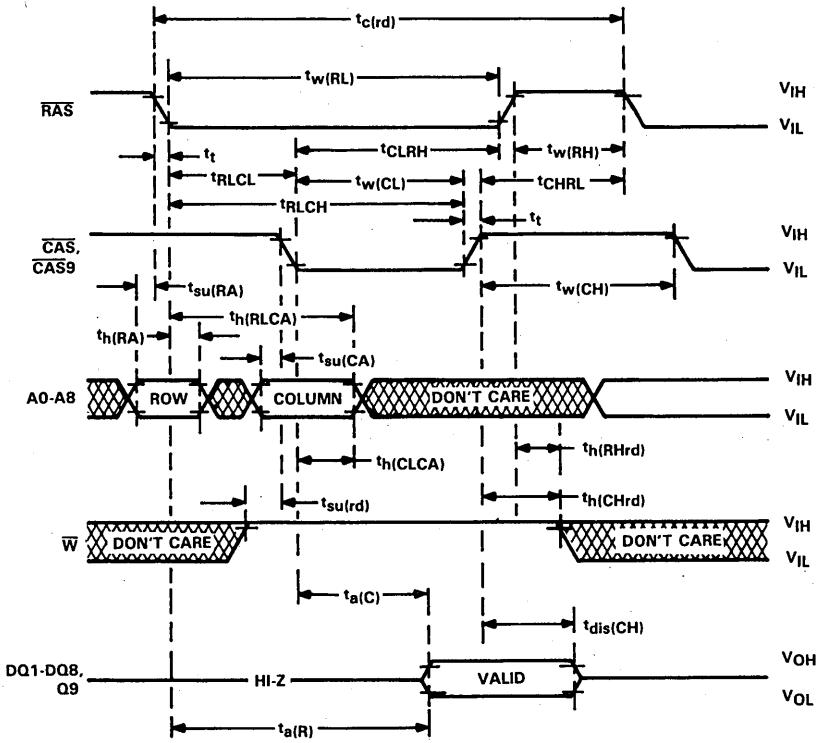


FIGURE 1. LOAD CIRCUIT

read cycle timing



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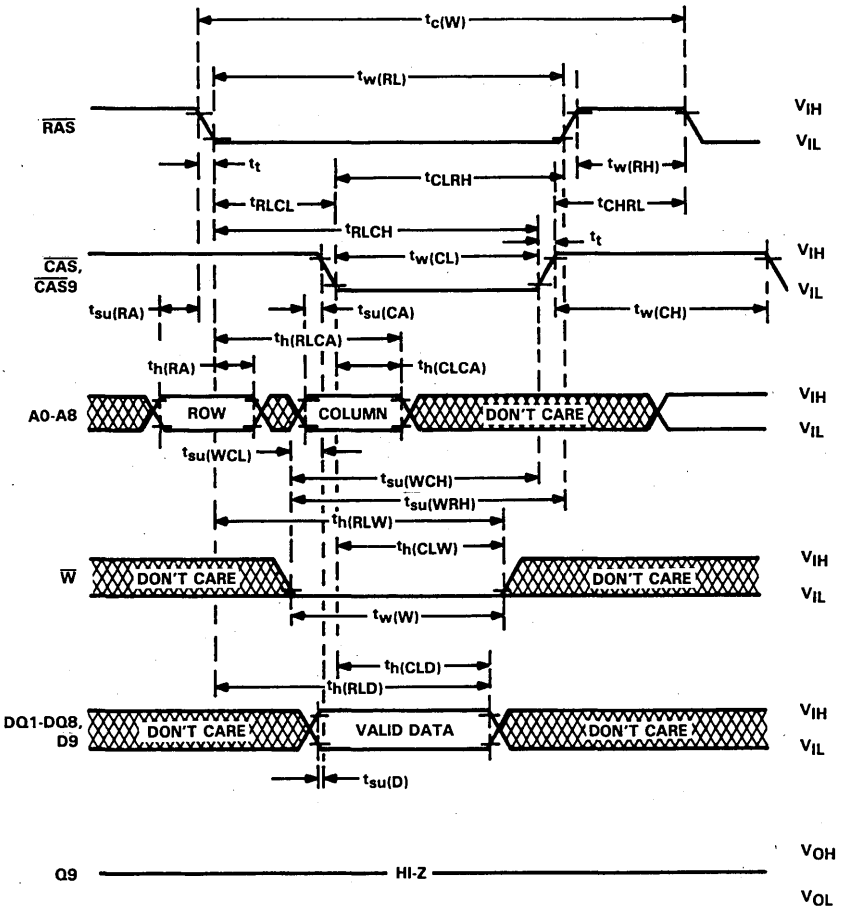
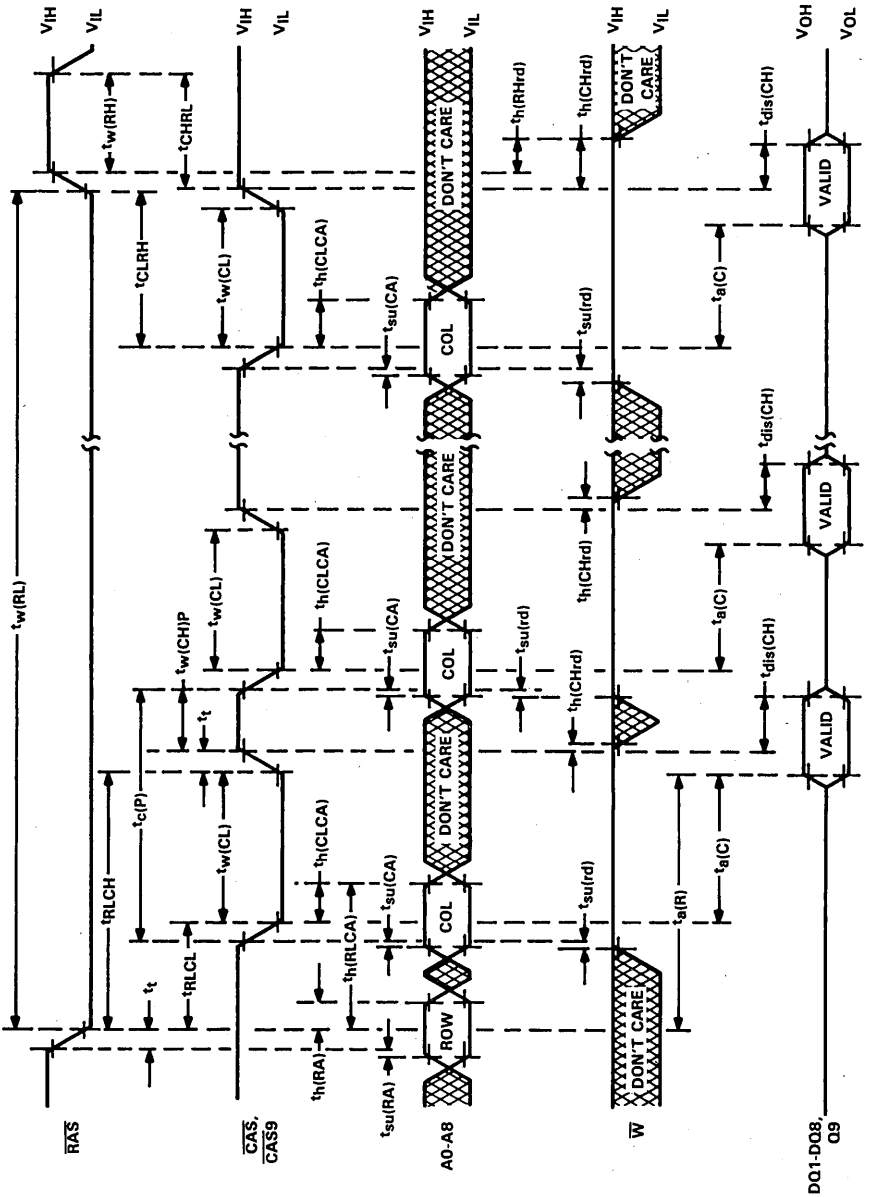
early write cycle timing

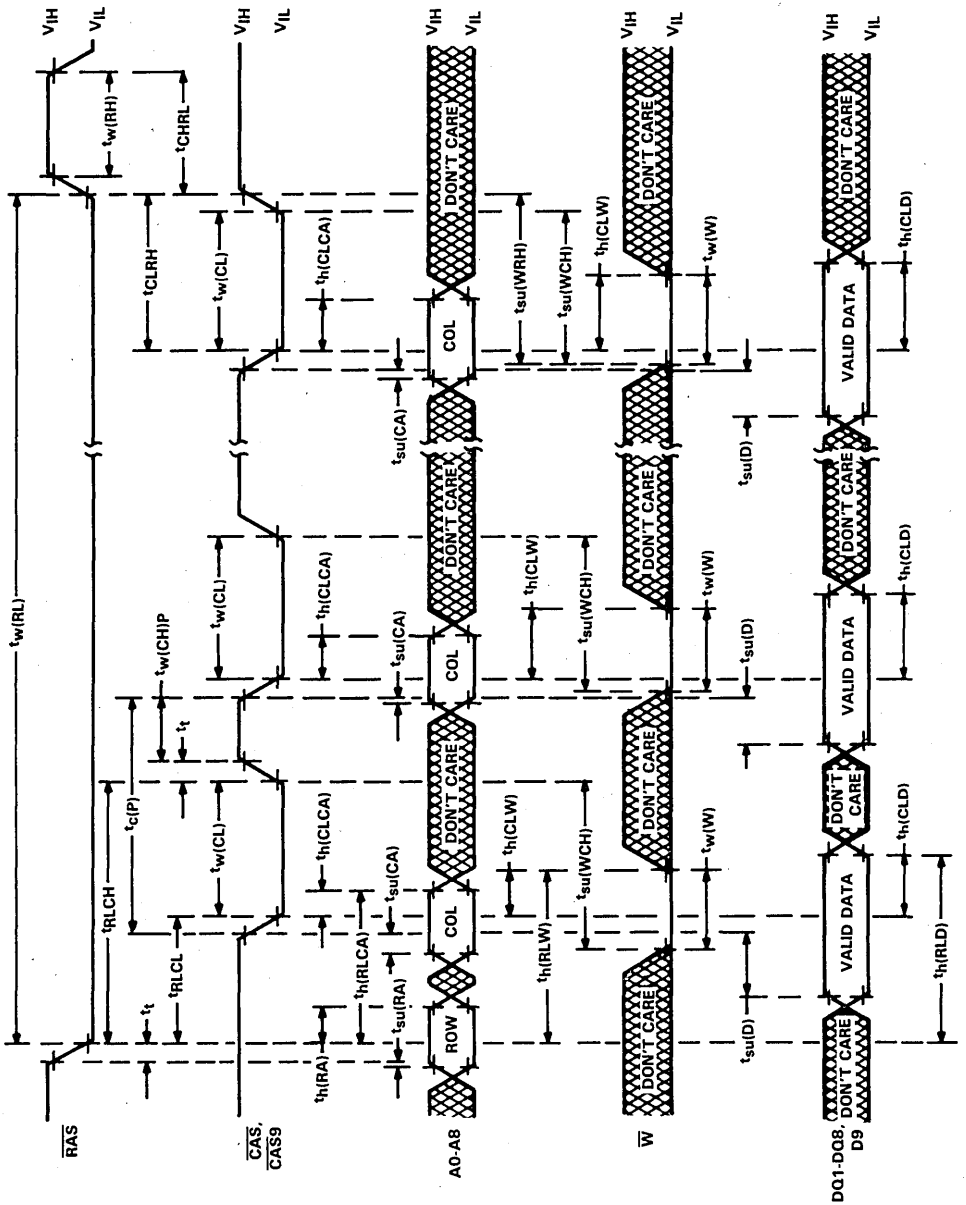


page-mode read cycle timing



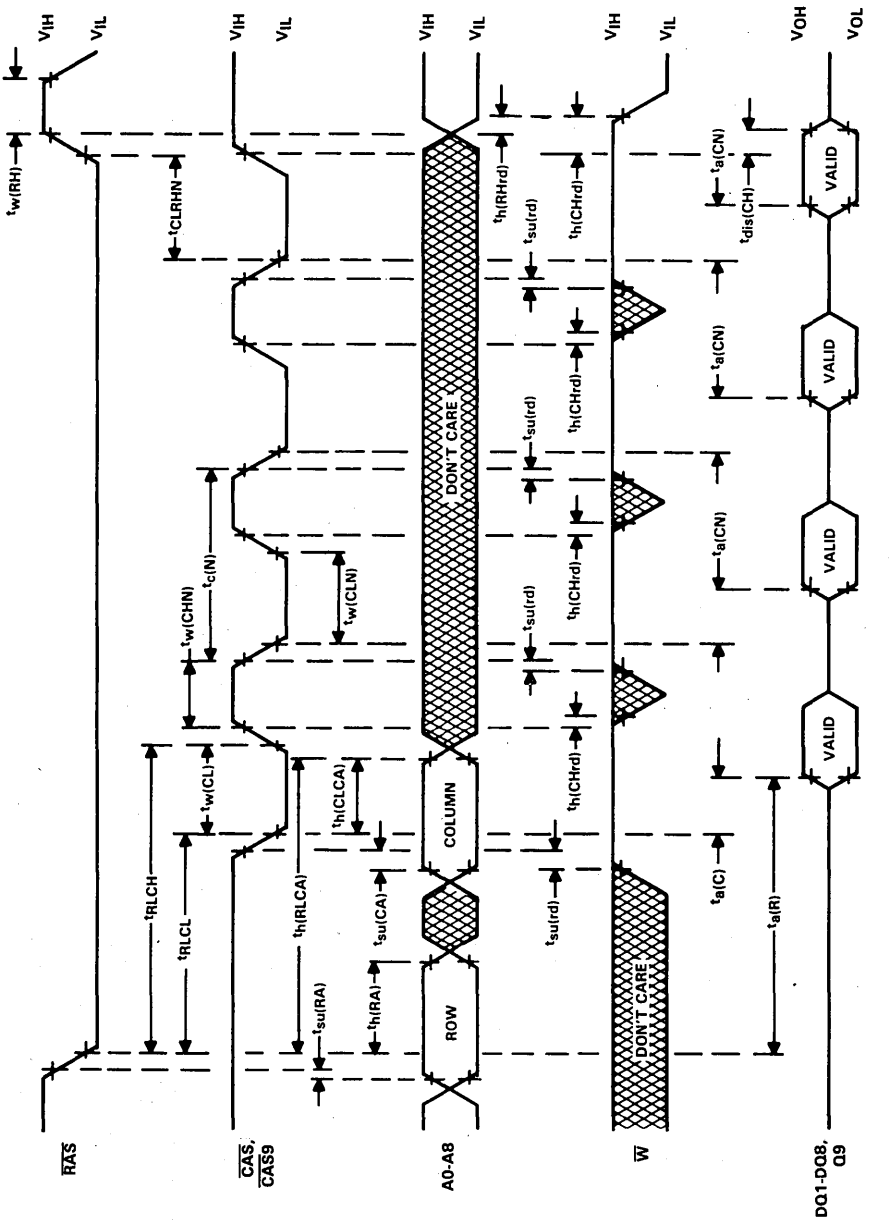
NOTE 4: A write cycle can be intermixed with read cycles as long as the write timing specifications are not violated.

page-mode write cycle timing



NOTE 5: A read cycle can be intermixed with write cycles as long as read timing specifications are not violated.

nibble-mode read cycle timing



5 Dynamic RAM Modules

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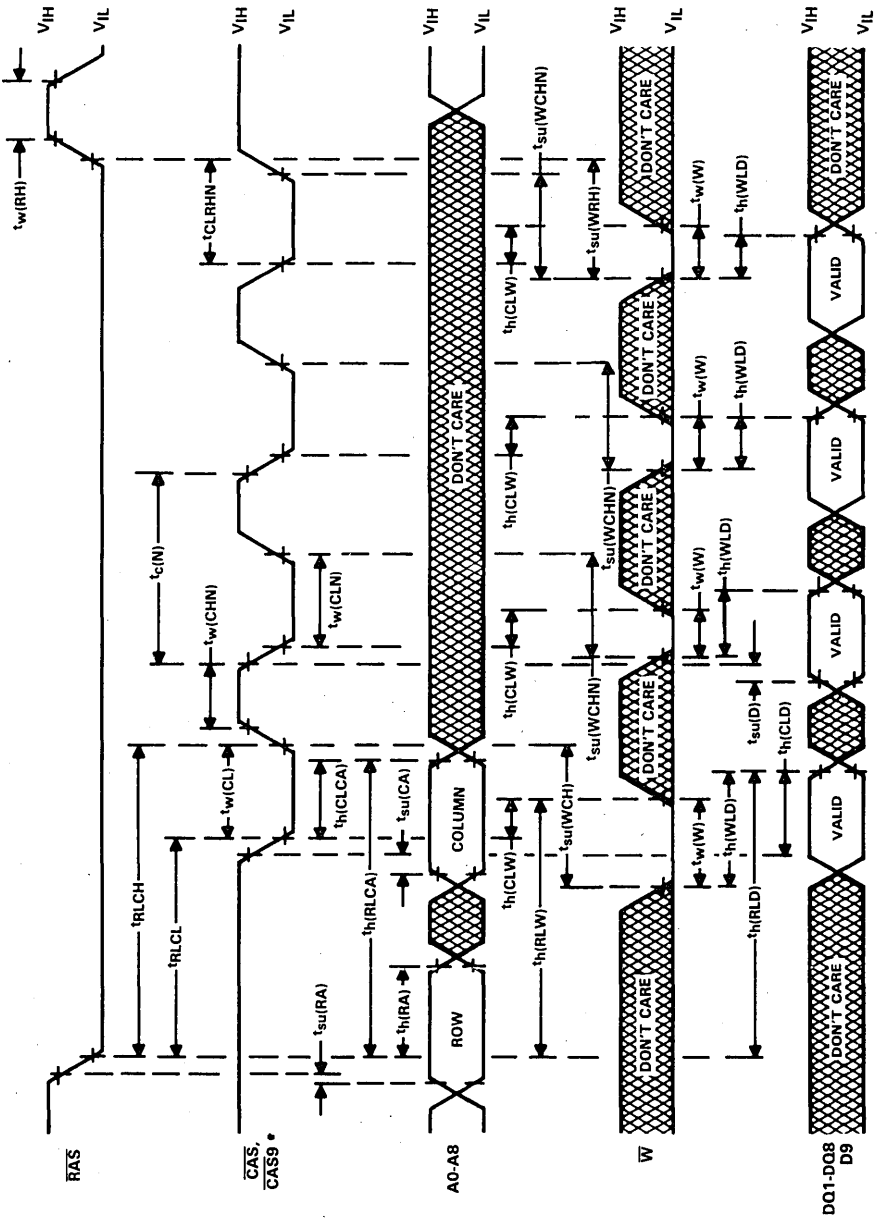
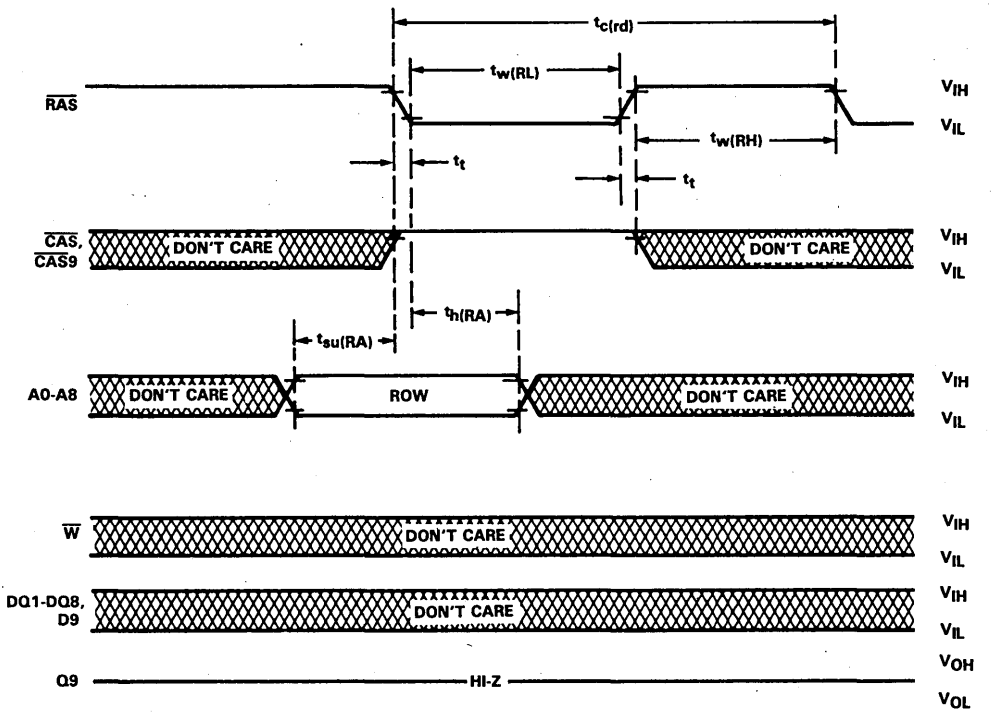
nibble-mode write cycle timing



$\overline{\text{RAS}}$-only refresh timing



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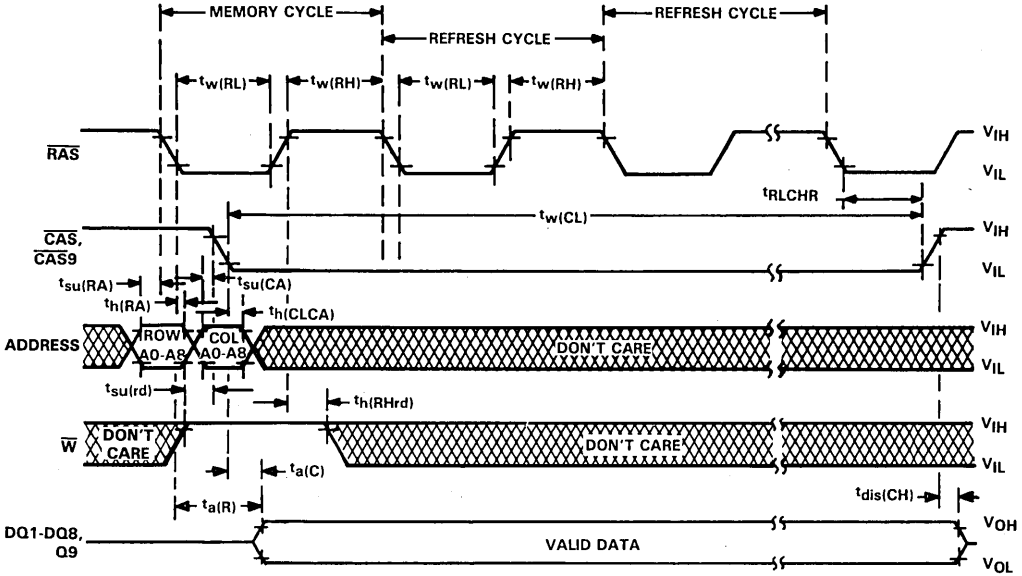
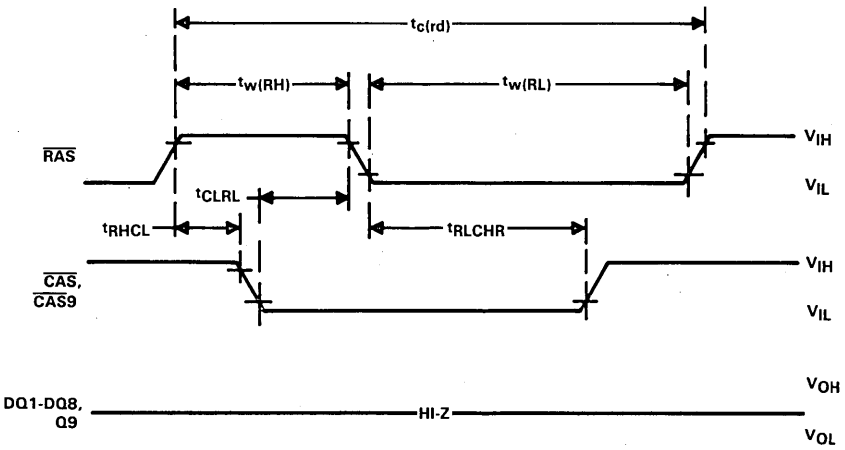
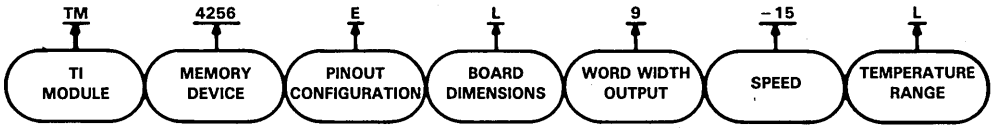
hidden refresh cycle timing



automatic ($\overline{CAS}$-before-$\overline{RAS}$) refresh cycle timing



TI single-in-line package nomenclature†



E Version	L Package	Max Access	L 0°C to 70°C
Pin 24-No Connect	(76,2 x 16,5 mm)	–12 120 ns	
G Version	(3.0 x 0.65 inches)	–15 150 ns	
Pin 24-PRD	U Package	–20 200 ns	
	(88,9 x 16,5 mm)		
	(3.5 x 0.65 inches)		

†The E pinout configuration designator is used when specifying the L package; the G pinout configuration version designator is used when specifying the U package.

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TM4256EQ5, TM4257EQ5
262,144 BY 5-BIT DYNAMIC RAM MODULES

OCTOBER 1985– REVISED NOVEMBER 1985

- 262,144 X 5 Organization
- Single 5-V Supply (10% Tolerance)
- 24-Pin Single-in-Line Package (SIP)
- Utilizes Five 256K Dynamic RAMs in Plastic Chip Carrier
- Long Refresh Period . . . 4 ms (256 cycles)
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Outputs
- Performance Ranges:

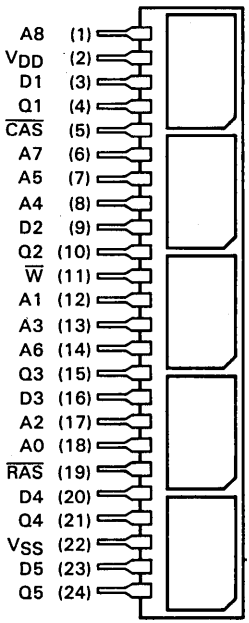
	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	READ-MODIFY-WRITE CYCLE (MIN)
TM425_EQ5-12	120 ns	60 ns	230 ns	275 ns
TM425_EQ5-15	150 ns	75 ns	260 ns	305 ns
TM425_EQ5-20	200 ns	100 ns	330 ns	370 ns

- Common $\overline{CAS}$ Control with Separate Data-Input and Output Lines
- Low Power Dissipation:

	OPERATING (TYP)	STANDBY (TYP)
TM425_EQ5-12	1625 mW	65 mW
TM425_EQ5-15	1375 mW	65 mW
TM425_EQ5-20	1125 mW	65 mW

- Operating Free-Air Temperature . . . 0°C to 70°C
- Downward Compatible with 64K X 5 Single-in-Line Package (TM4164EQ5)

Q SINGLE-IN-LINE PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A8	Address Inputs
$\overline{CAS}$	Column-Address Strobe
D1-D5	Data Inputs
NC	No Connection
Q1-Q5	Data Outputs
$\overline{RAS}$	Row-Address Strobe
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The TM425_EQ5 is a 1280K, dynamic random-access memory module organized as 262,144 × 5 bits in a 24-pin single-in-line package comprising five TMS425_FML, 262,144 × 1 bit dynamic RAM's in 18-lead plastic chip carriers mounted on top of a substrate together with five 0.1 μF decoupling capacitors mounted beneath the chip carriers. The onboard capacitors eliminate the need for bypassing on the motherboard and offer superior performance over equivalent leaded capacitors due to reduced lead inductance. Also, with 0.3 inch board spacing the TM425_EQ5 has a density of ten devices per square inch (approximately 4X the density of DIPs). With the elimination of bypass capacitors on the motherboard, reduced PC board size, and fewer plated-through holes, a cost savings can be realized.

The TM425_EQ5 features $\overline{RAS}$ access times of 120 ns, 150 ns, and 200 ns maximum. Power dissipation as low as 1125 mW typical operating and 65 mW typical standby.

Refresh period is extended to 4 milliseconds, and during this period each of the 256 rows must be strobed with $\overline{RAS}$ in order to retain data. $\overline{CAS}$ can remain high during the refresh sequence to conserve power.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address lines and data in are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TM425_EQ5 is rated for operation from 0°C to 70°C.

operation

address (A0 through A8)

Eight address bits are required to decode 1 of 262,144 storage cell locations on each of the five chips. Nine row-address bits are set up on pins A0 through A8 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the nine column-address bits are set up on pins A0 through A8 and latched onto the chip by the column-address strobe. All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data inputs are disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$, the data-outs will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data-in (D1-D5)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latches. These latches can be driven from standard TTL circuits without a pull-up resistor. In the early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data-out (Q1-Q5)

The three-state output buffers provide direct TTL compatibility (no pull-up resistor required) with a fan out of two Series 74 TTL loads for each output. Data out is the same polarity as data in. The outputs are in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the outputs go active after the access time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ is satisfied. The outputs become valid after the access time has elapsed and remain valid while $\overline{CAS}$ is low; $\overline{CAS}$ going high returns it to a high-impedance state. In the early write cycle, the outputs are always in the high-impedance state. In a delayed-write or read-modify-write cycle, the outputs will follow the sequence for the read cycle.

refresh

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffers are in the high-impedance state unless $\overline{CAS}$ is applied, the $\overline{RAS}$-only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses (A0 through A7) with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

The $\overline{CAS}$-before-$\overline{RAS}$ refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CLRL}) and holding it low after $\overline{RAS}$ falls (see parameter t_{RLCHR}). For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally.

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hidden refresh

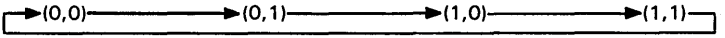
Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a "$\overline{RAS}$-only" refresh cycle. The external address is also ignored during the hidden refresh cycles.

page-mode (TM4256EQ5)

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the module. Thus, the time required to setup and strobe sequential row addresses for the same page is eliminated. To extend beyond the 256 column locations on a single module, the row address and $\overline{RAS}$ are applied to multiple modules. $\overline{CAS}$ is then decoded to select the proper module.

nibble mode (TM4257EQ5)

Nibble-mode operation allows high-speed serial read, write, or read-modify-write access of 1 to 4 bits of data. The first bit is accessed in the normal manner with read data coming out at $t_{a(C)}$ time. The next sequential nibble bits can be read or written by cycling $\overline{CAS}$ while $\overline{RAS}$ remains low. The first bit is determined by the row and column addresses, which need to be supplied only for the first access. Column A8 and row A8 (CA8, RA8) provide the two binary bits for initial selection of the nibble addresses. Thereafter, the falling edge of $\overline{CAS}$ will access the next bit of the circular 4-bit nibble in the following sequence:



In nibble-mode, all normal memory operations (read, write, or read-modify-write) may be performed in any desired combination.

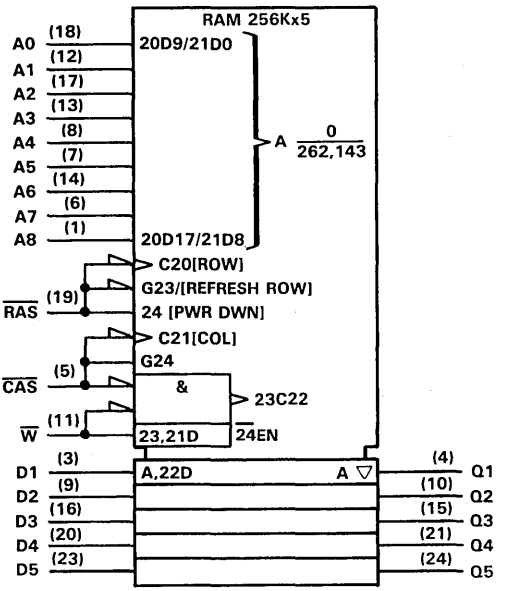
power up

To achieve proper device operation, an initial pause of 200 μs is required after power up followed by a minimum of eight initialization cycles.

single-in-line package and components

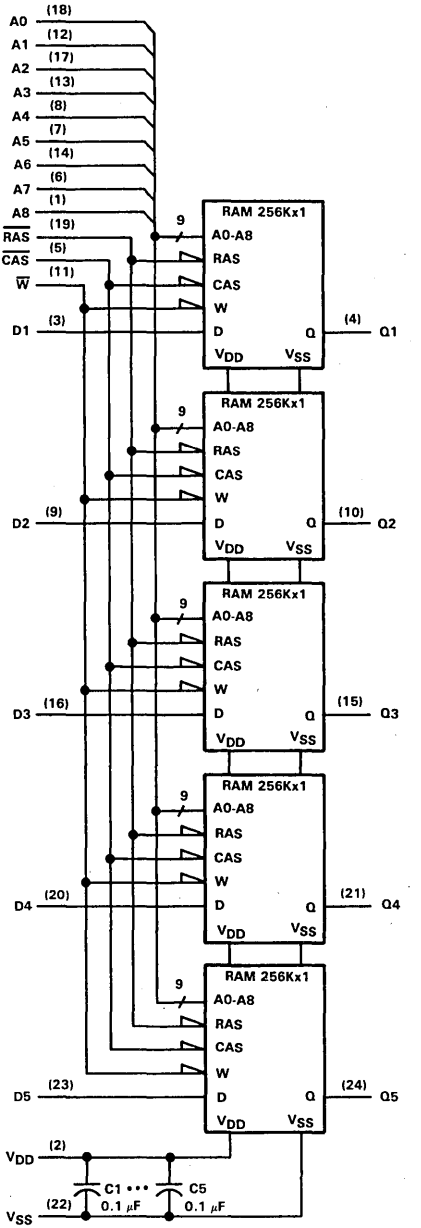
PC substrate: 0,79 mm (0.031 inch) minimum thickness
Bypass capacitors: Multilayer ceramic
Leads: Tin/lead solder coated over phosphor-bronze

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range for any pin except V_{DD} and data out (see Note 1) . . . . . −1.5 V to 10 V
Voltage range on V_{DD} supply and data out with respect to V_{SS} . . . . . −1 V to 6 V
Short circuit output current for any output . . . . . 50 mA
Power dissipation . . . . . 5 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	−1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TM425_EQ5-12			TM425_EQ5-15			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4		V_{DD}	2.4		V_{DD}	V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA	0		0.4	0		0.4	V
I_I	Input current (leakage)	V_I = 0 V to 6.5 V, V_{DD} = 5 V, All other pins = 0 V			±10			±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10			±10	μA
I_{DD1}	Average operating current during read or write cycle	t_c = minimum cycle, All outputs open		325	390		275	340	mA
I_{DD2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, All outputs open		13	23		13	23	mA
I_{DD3}	Average refresh current	t_c = minimum cycle, $\overline{CAS}$ high and $\overline{RAS}$ cycling, All outputs open		225	300		200	265	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low and $\overline{CAS}$ cycling, All outputs open		175	240		150	215	mA
I_{DD5}	Average nibble-mode current	$t_{c(N)}$ = minimum cycle, $\overline{RAS}$ low and $\overline{CAS}$ cycling, All outputs open		160	220		135	160	mA

†All typical values are at T_A = 25°C and nominal supply voltages.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TM425_EQ5-20			UNIT
			MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4		V_{DD}	V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA	0		0.4	V
I_I	Input current (leakage)	V_I = 0 V to 6.5 V, V_{DD} = 5 V, All other pins = 0 V			±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10	μA
I_{DD1}	Average operating current during read or write cycle	t_c = minimum cycle, All outputs open		225	290	mA
I_{DD2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, All outputs open		13	23	mA
I_{DD3}	Average refresh current	t_c = minimum cycle, $\overline{CAS}$ high and $\overline{RAS}$ cycling, All outputs open		175	240	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low and $\overline{CAS}$ cycling, All outputs open		125	175	mA
I_{DD5}	Average nibble-mode current	$t_{c(N)}$ = minimum cycle, $\overline{RAS}$ low and $\overline{CAS}$ cycling, All outputs open		110	160	mA

†All typical values are at T_A = 25°C and nominal supply voltages.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		35	pF
$C_{i(D)}$	Input capacitance, data inputs		35	pF
$C_{i(RAS)}$	Input capacitance, $\overline{RAS}$ input		40	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$ input		40	pF
$C_{i(CAS)}$	Input capacitance, $\overline{CAS}$ input		40	pF
$C_{o(Q)}$	Output capacitance, data outputs		10	pF
$C_{o(VDD)}$	Decoupling capacitance	0.6		μF

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switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TM425_EQ5-12		TM425_EQ5-15		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		60		75	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, Load = 2 Series 74 TTL gates	t_{RAC}		120		150	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	35	0	35	ns

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TM425_EQ5-20		UNIT
				MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		100	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, Load = 2 Series 74 TTL gates	t_{RAC}		200	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	35	ns

timing requirements over recommended supply voltage range and operating free-air temperature range

		ALT. SYMBOL	TM425_EQ5-12 MIN	TM425_EQ5-12 MAX	UNIT
$t_{c(P)}$	Page-mode cycle time (read or write cycle)	t_{PC}	120		ns
$t_{c(PM)}$	Page-mode cycle time (read-modify-write cycle)	t_{PCM}	165		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	230		ns
$t_{c(W)}$	Write cycle time	t_{WC}	230		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	275		ns
$t_{w(CH)P}$	Pulse duration, $\overline{CAS}$ high (page mode)	t_{CP}	50		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (non-page mode)	t_{CPN}	25		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low‡	t_{CAS}	60	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high	t_{RP}	100		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low§	t_{RAS}	120	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	40		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		ns
$t_{su(WCL)}$	Early write-command setup time before $\overline{CAS}$ low	t_{WCS}	0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	40		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	40		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	20		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	15		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	80		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DHC}	35		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	95		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DHW}	35		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	10		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	35		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	95		ns

Continued next page.

NOTE 3: Timing measurements are referenced to V_{IL} max and V_{IH} min.

†All cycle times assume t_t = 5 ns.

‡In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$). This applies to page-mode read-modify-write also.

§In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).

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timing requirements over recommended supply voltage range and operating free-air temperature range (continued)

		ALT. SYMBOL	TMS425_EQ5-12		UNIT
			MIN	MAX	
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	120		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	60		ns
t_{RLCHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high¶	t_{CHR}	25		ns
t_{CLRL}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low¶	t_{CSR}	25		ns
t_{RHCL}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low¶	t_{RPC}	20		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{CWD}	60		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	30	60	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{RWD}	120		ns
t_{rf}	Refresh time interval	t_{REF}		4	ms

Continued next page.

NOTE 3: Timing measurements are referenced to V_{IL} max and V_{IH} min.

¶$\overline{CAS}$-before-$\overline{RAS}$ refresh only.

timing requirements over recommended supply voltage range and operating free-air temperature range (continued)

		ALT. SYMBOL	TM425_EQ5-15		TM425_EQ5-20		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(P)}$	Page-mode cycle time (read or write cycle)	t_{PC}	145		190		ns
$t_{c(PM)}$	Page-mode cycle time (read-modify-write cycle)	t_{PCM}	190		245		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	260		330		ns
$t_{c(W)}$	Write cycle time	t_{WC}	260		330		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	305		370		ns
$t_{w(CH)P}$	Pulse duration, $\overline{CAS}$ high (page mode)	t_{CP}	60		80		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (non-page mode)	t_{CPN}	25		30		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low‡	t_{CAS}	75	10,000	100	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high	t_{RP}	100		120		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low§	t_{RAS}	150	10,000	200	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	45		55		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	50	3	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		0		ns
$t_{su(WCL)}$	Early write-command setup time before $\overline{CAS}$ low	t_{WCS}	0		0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	45		60		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	45		60		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	25		30		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	15		20		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	100		130		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DHC}	45		55		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	120		155		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DHW}	45		55		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	10		15		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	45		55		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	120		155		ns

Continued next page.

NOTE 3: Timing measurements are referenced to V_{IL} max and V_{IH} min.

†All cycle times assume t_t = 5 ns.

‡In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time $t_{w(CL)}$. This applies to page-mode read-modify-write also.

§In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).

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timing requirements over recommended supply voltage range and operating free-air temperature range (concluded)

		ALT. SYMBOL	TM425_EQ5-15		TM425_EQ5-20		UNIT
			MIN	MAX	MIN	MAX	
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	150		200		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	75		100		ns
t_{RLCHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high¶	t_{CHR}	30		35		ns
t_{CLRL}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low¶	t_{CSR}	30		35		ns
t_{RHCL}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low¶	t_{RPC}	20		25		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{CWD}	70		90		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	30	75	30	100	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{RWD}	145		190		ns
t_{rf}	Refresh time interval	t_{REF}		4		4	ms

NOTE 3: Timing measurements are referenced to V_{IL} max and V_{IH} min.
¶$\overline{CAS}$-before-$\overline{RAS}$ refresh only.

NIBBLE-MODE CYCLE

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		ALT. SYMBOL	TM4257EQ5-12		TM4257EQ5-15		TM4257EQ5-20		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(CN)}$	Nibble-mode access time from $\overline{CAS}$	t_{NCAC}		30		40		50	ns

timing requirements over recommended supply voltage range and operating free-air temperature range

		ALT. SYMBOL	TM4257EQ5-12		TM4257EQ5-15		TM4257EQ5-20		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(N)}$	Nibble-mode cycle time	t_{NC}	60		75		90		ns
$t_{c(rdWN)}$	Nibble-mode read-modify-write cycle time	t_{NRMW}	85		105		130		
t_{CLRHN}	Nibble-mode delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{NRSH}	30		40		50		
t_{CLWLN}	Nibble-mode delay time, $\overline{CAS}$ to $\overline{W}$ delay	t_{NCWD}	25		30		40		
$t_{w(CLN)}$	Nibble-mode pulse duration, $\overline{CAS}$ low	t_{NCAS}	30		40		50		
$t_{w(CHN)}$	Nibble-mode pulse duration, $\overline{CAS}$ high	t_{NCP}	20		25		30		
$t_{w(CRWN)}$	Nibble-mode read-modify-write pulse duration, $\overline{CAS}$ low	t_{NCRW}	55		70		90		
$t_{su(WCHN)}$	Nibble-mode write command setup time before $\overline{CAS}$ high	t_{NCWL}	25		35		45		

PARAMETER MEASUREMENT INFORMATION

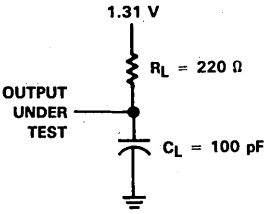
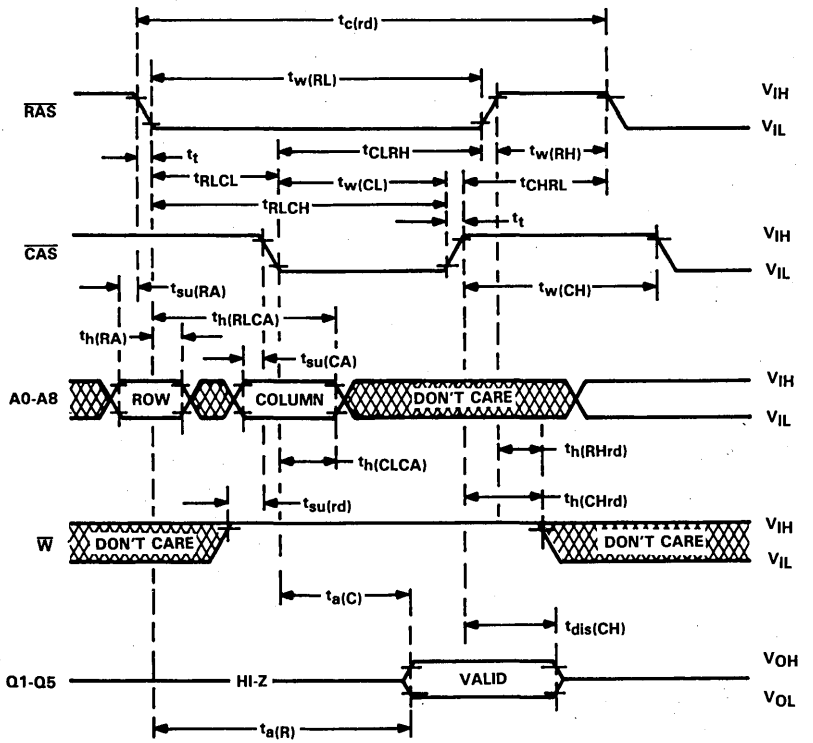


FIGURE 1. LOAD CIRCUIT

read cycle timing



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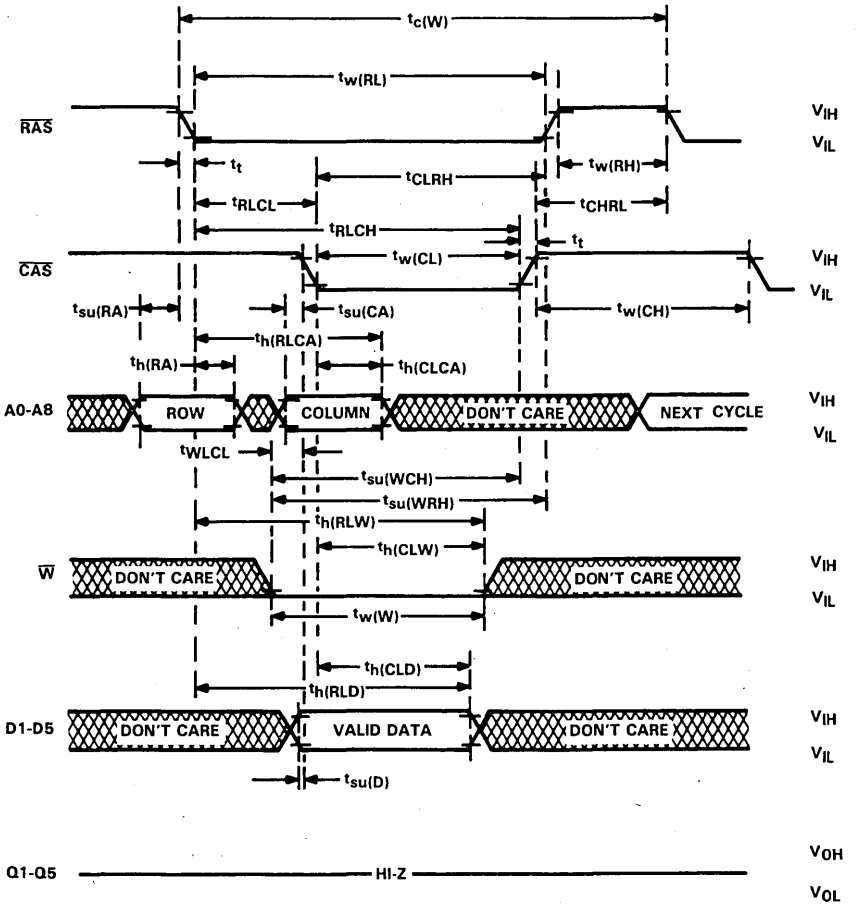
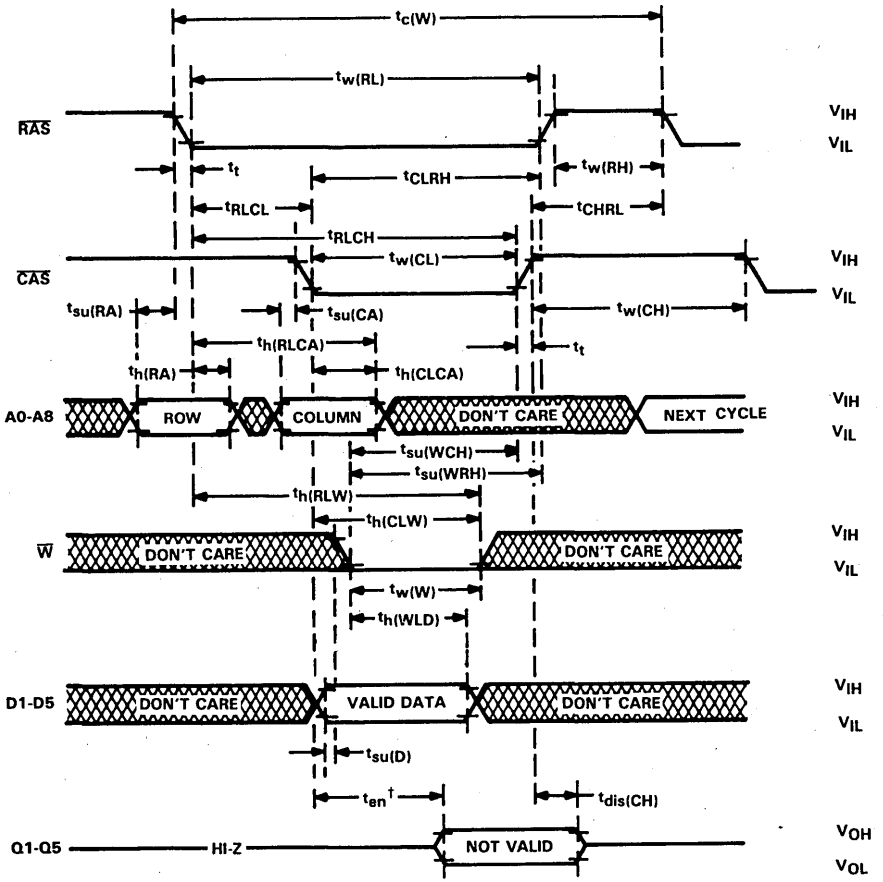
early write cycle timing



write cycle timing



†The enable time (t_{en}) for a write cycle is equal in duration to the access time from $\overline{CAS}$ ($t_{a(C)}$) in a read cycle; but the active levels at the output are invalid.

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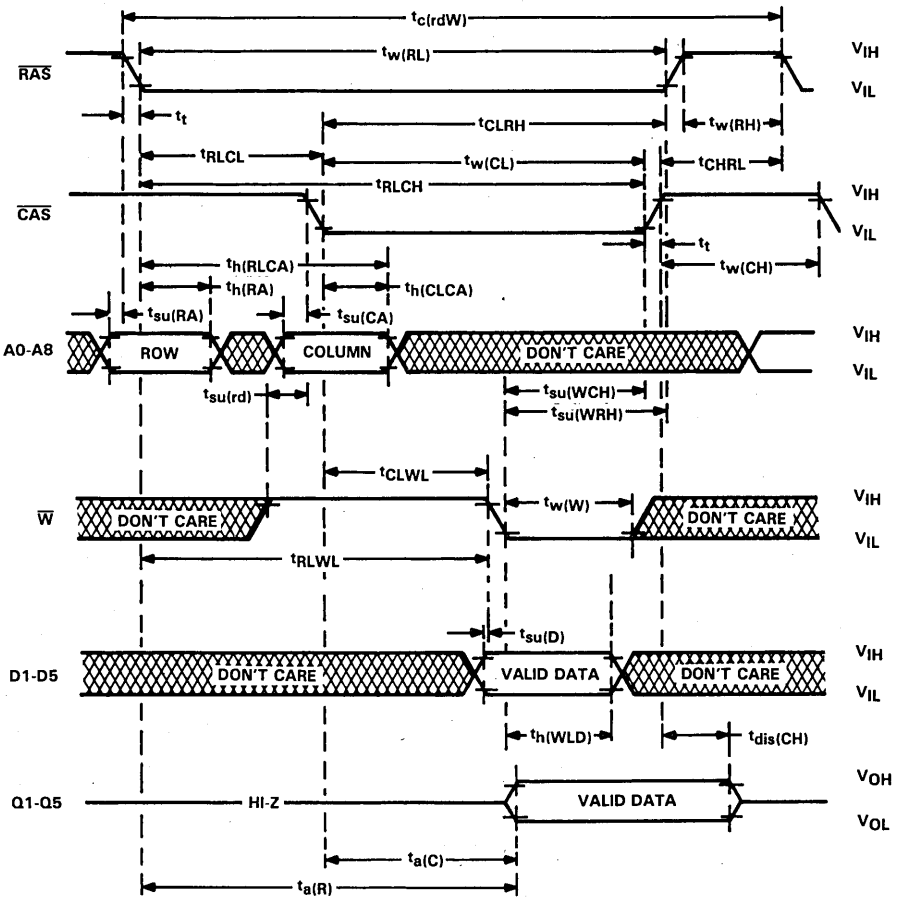
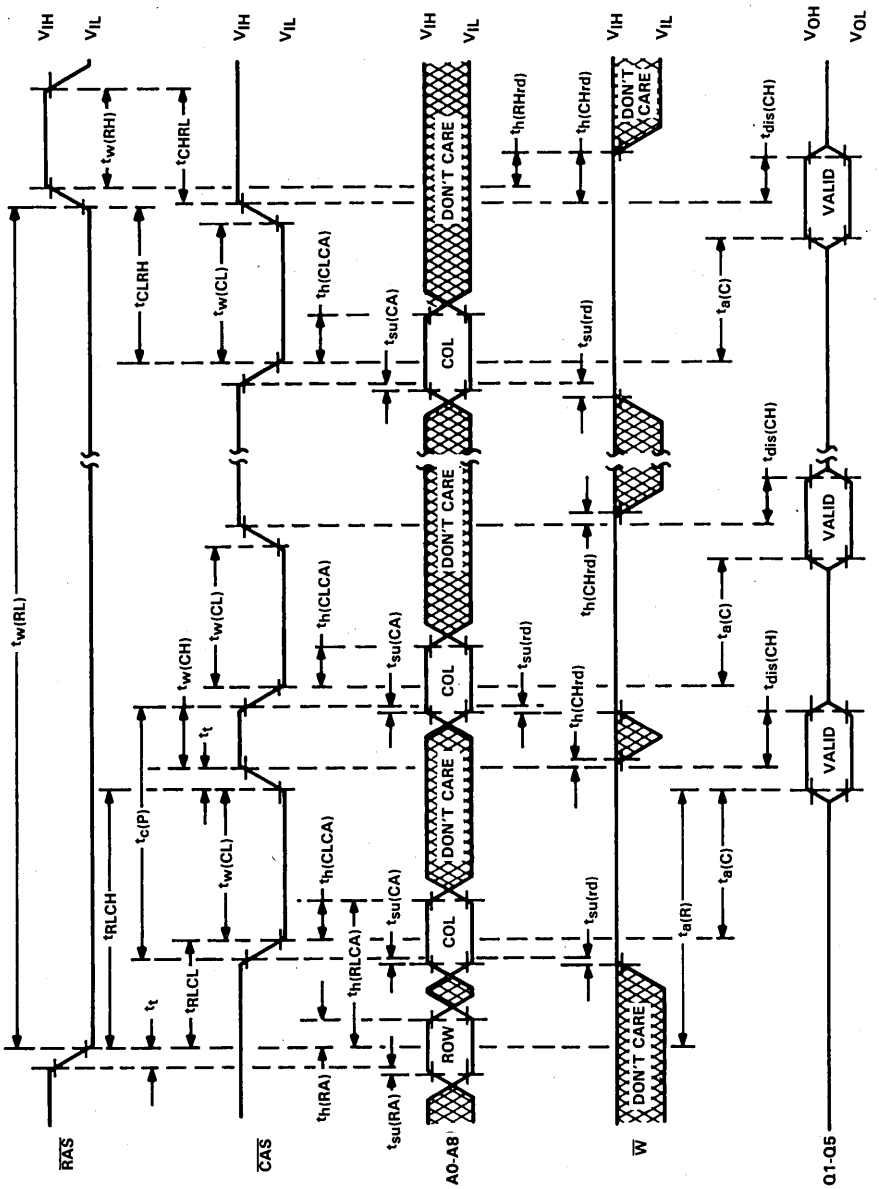
read-write/read-modify-write cycle timing

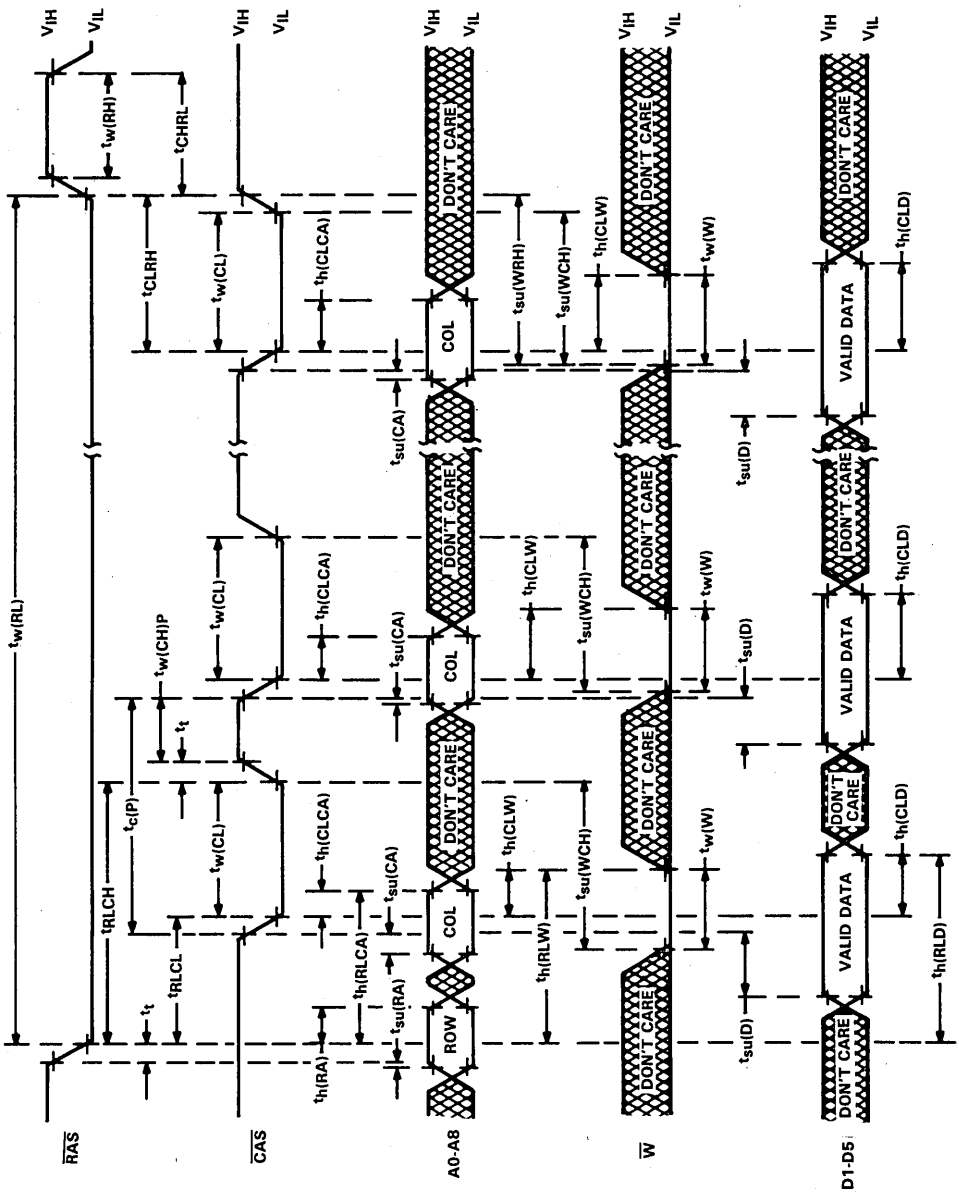


page-mode read cycle timing



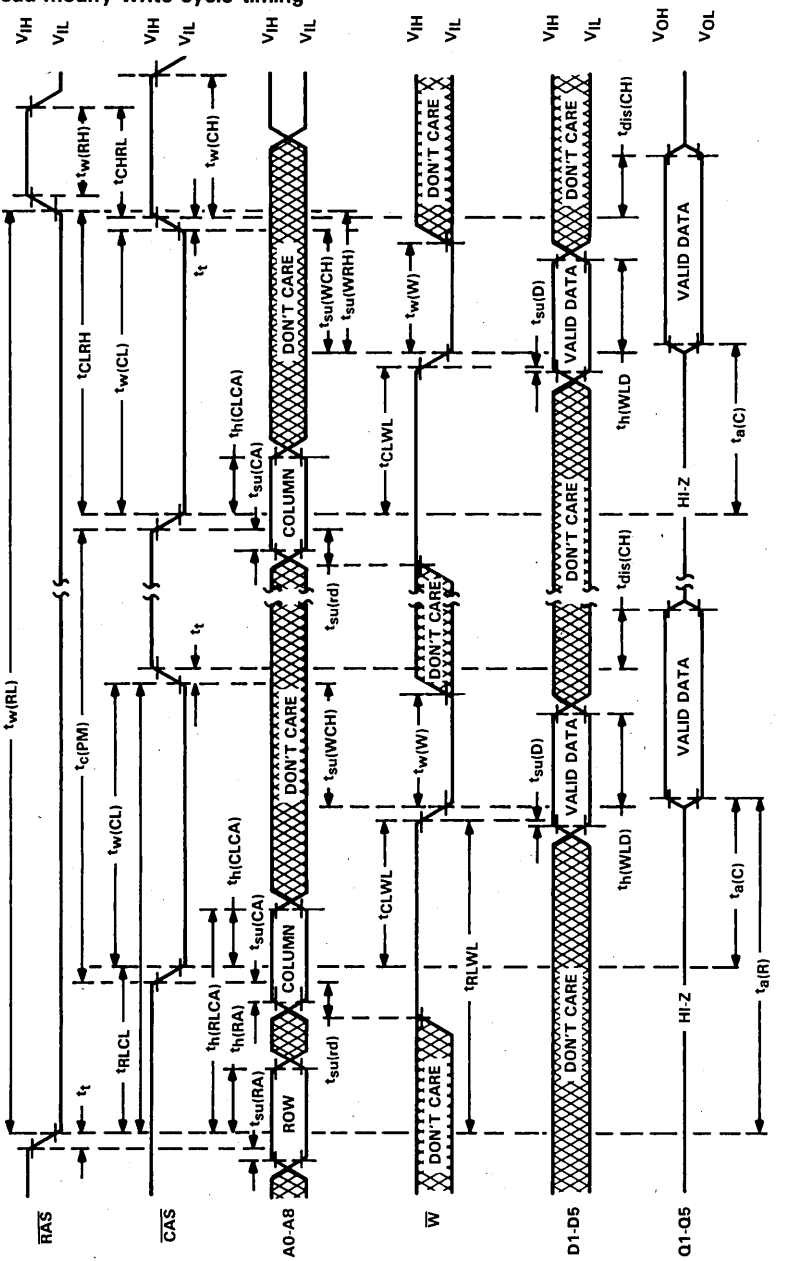
NOTE 4: A write cycle or a read-modify-write cycle can be intermixed with read cycles as long as the write and read-modify write timing specifications are not violated.

page-mode write cycle timing



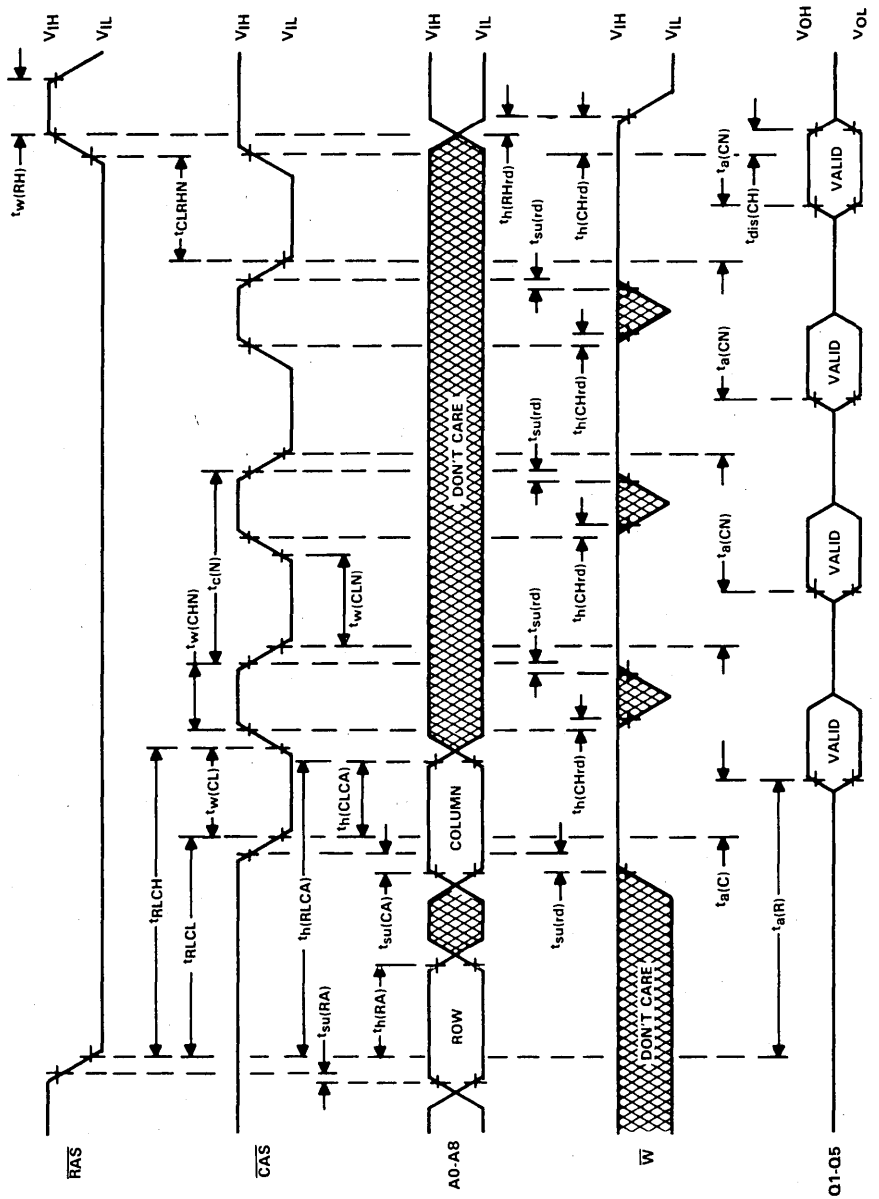
NOTE 5: A read cycle or a read-modify-write cycle can be intermixed with write cycles as long as read and read-modify-write timing specifications are not violated.

page-mode read-modify-write cycle timing

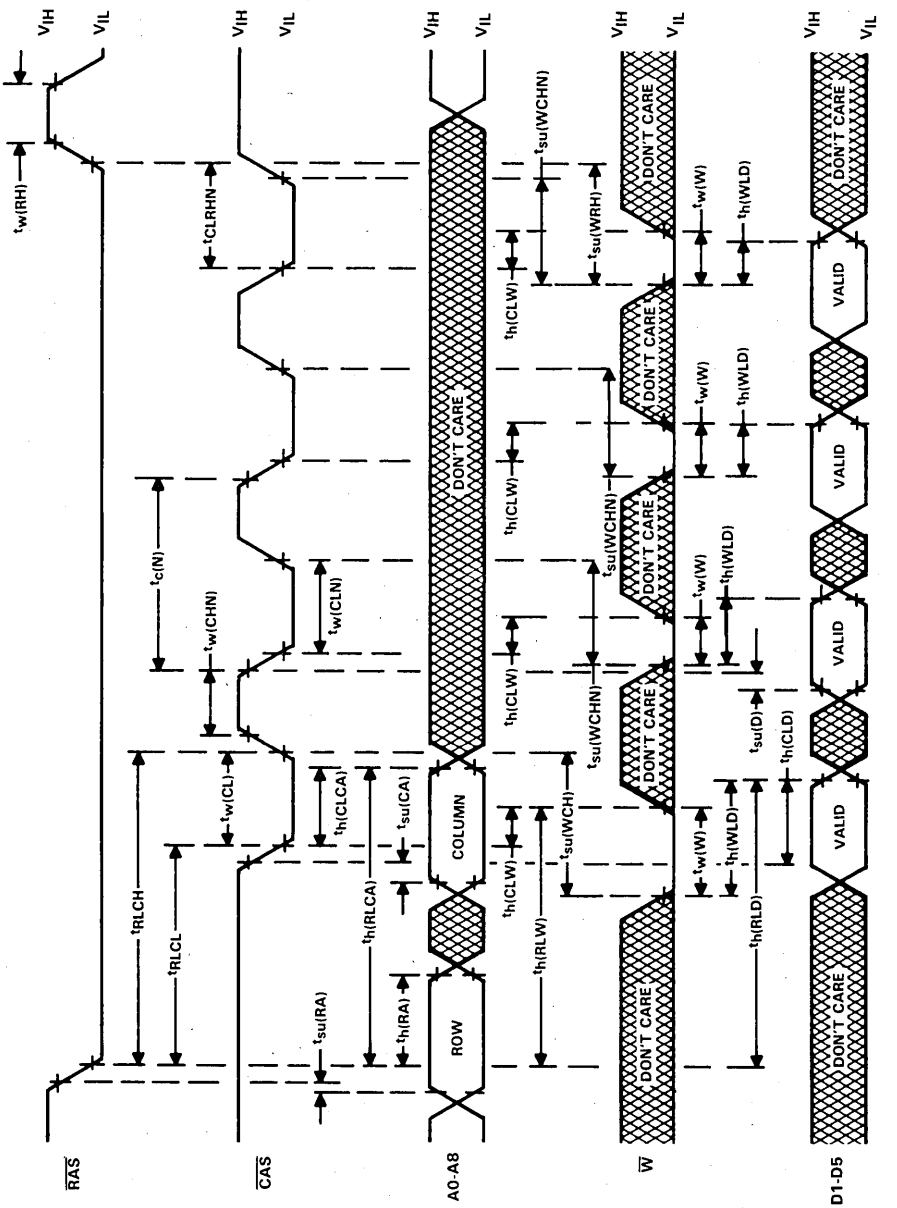


NOTE 6: A read or a write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

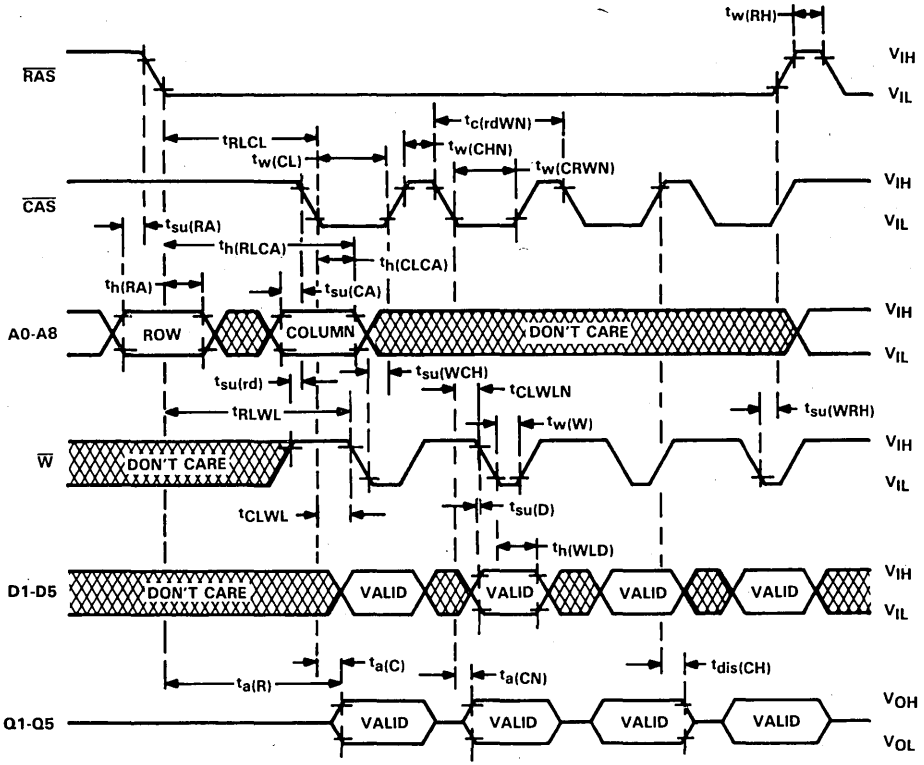
nibble-mode read cycle timing



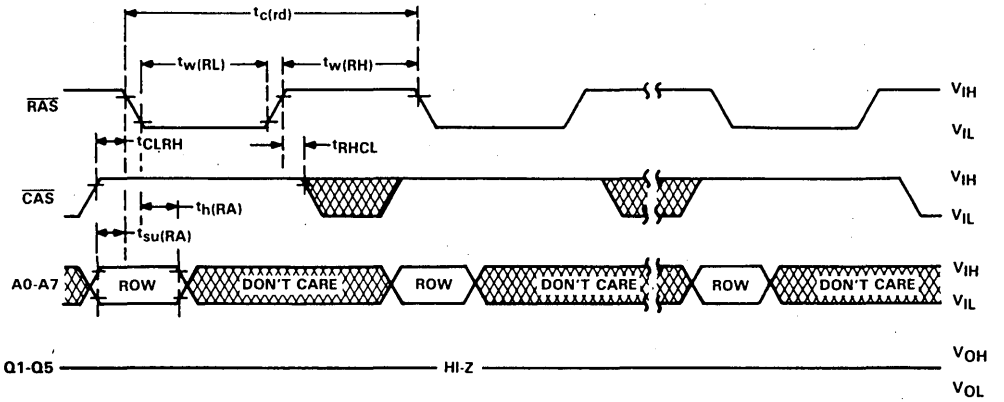
nibble-mode write cycle timing



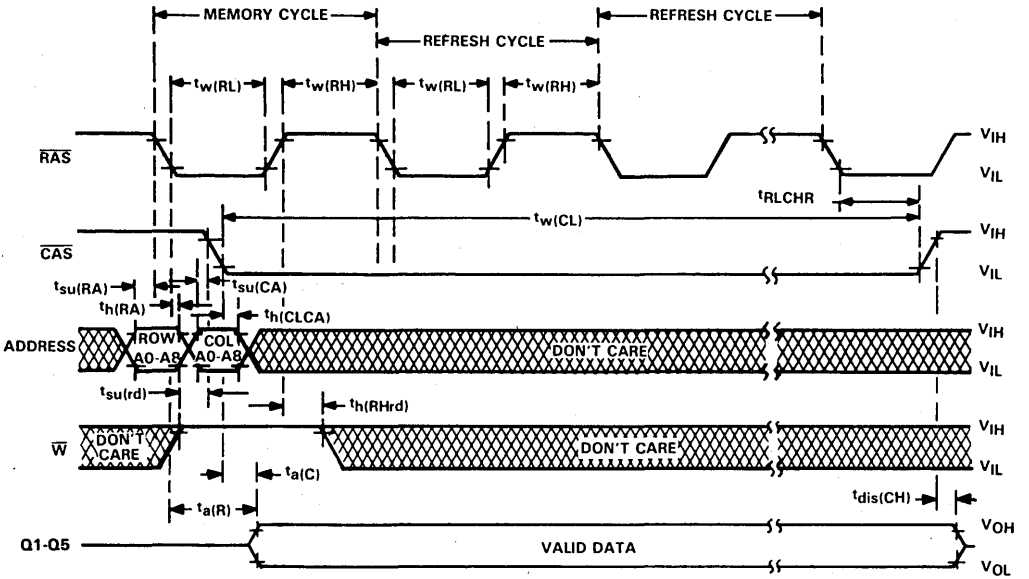
nibble-mode read-modify-write-cycle timing



$\overline{\text{RAS}}$-only refresh cycle timing



hidden refresh cycle timing



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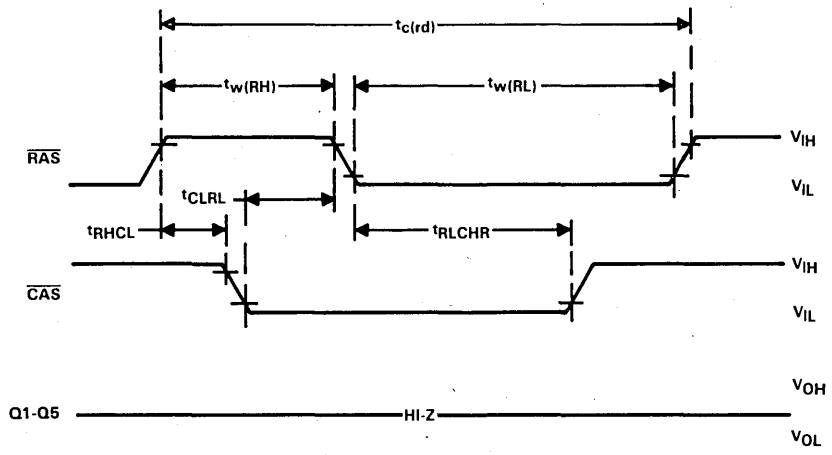
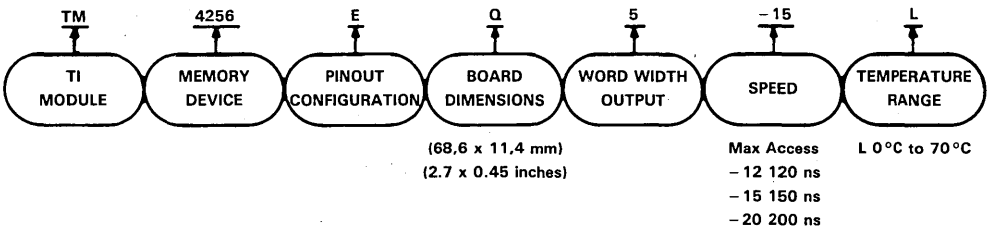
automatic ($\overline{CAS}$-before-$\overline{RAS}$) refresh cycle timing



TI single-in-line package nomenclature



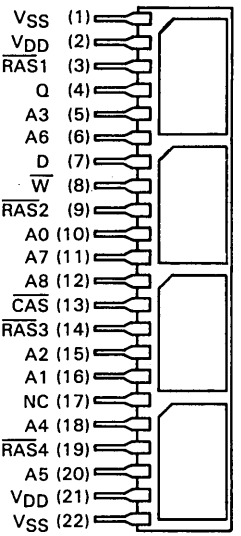
OCTOBER 1985 – REVISED NOVEMBER 1985

- 1,048,576 X 1 Organization
- Single 5-V Supply (10% Tolerance)
- 22-Pin Single-in-Line Package (SIP)
- Utilizes Four 256K Dynamic RAMs in Plastic Chip Carrier
- Long Refresh Period . . . 4 ms (256 Cycles)
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Outputs
- Performance Range:

	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	READ-MODIFY-WRITE CYCLE (MIN)
TM425_FC1-12	120 ns	60 ns	230 ns	275 ns
TM425_FC1-15	150 ns	75 ns	260 ns	305 ns
TM425_FC1-20	200 ns	100 ns	330 ns	370 ns

- Common $\overline{CAS}$ Control with Separate Data Input and Output Lines
- Operating Free-Air Temperature . . . 0°C to 70°C

C SINGLE-IN-LINE PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A8	Address Inputs
$\overline{CAS}$	Column-Address Strobe
D	Data Input
NC	No Connection
Q	Data Output
$\overline{RAS1}$-$\overline{RAS4}$	Row-Address Strobes
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The TM425_FC1 series are 1024K, dynamic random-access memory modules organized as 1,048,576 × 1 bit in a 22-pin single-in-line package comprising four TMS425_FML, 262,144 × 1 bit dynamic RAM's in 18-lead plastic chip carriers mounted on top of a substrate together with decoupling capacitors mounted beneath the chip carriers. The onboard capacitors eliminate the need for bypassing on the motherboard and offer superior performance over equivalent leaded capacitors due to reduced lead inductance. Also, with 0.3 inch board spacing the TM425_FC1 has a density of ten devices per square inch (approximately 4X the density of DIPs). With the elimination of bypass capacitors on the motherboard, reduced PC board size, and fewer plated-through holes, a cost savings can be realized.

The TM425_FC1 features $\overline{RAS}$ access times of 120 ns, 150 ns, and 200 ns maximum. Power dissipation as low as 225 mW typical operating and 50 mW typical standby.

Refresh period is extended to 4 milliseconds, and during this period each of the 256 rows must be strobed with $\overline{RAS}$ in order to retain data. $\overline{CAS}$ can remain high during the refresh sequence to conserve power.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address lines and data in are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TM425_FC1 is rated for operation from 0°C to 70°C.

operation

address (A0 through A8)

Eighteen address bits are required to decode 1 of 262,144 storage cell locations on each of the four chips. Nine row-address bits are set up on pins A0 through A8 and latched onto the chip by the row-address strobes ($\overline{RAS}1$-$\overline{RAS}4$). Then the nine column-address bits are set up on pins A0 through A8 and latched onto the chip by the column-address strobe. All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data inputs are disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$, the data outs will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data in (D)

Data is written during a write cycle. The falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latches. These latches can be driven from standard TTL circuits without a pull-up resistor. In the early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal.

data out (Q)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan out of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output goes active after the access time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ is satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low: $\overline{CAS}$ going high returns it to a high-impedance state. In the early write cycle, the output is always in the high-impedance state.

refresh

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffers are in the high-impedance state unless $\overline{CAS}$ is applied, the $\overline{RAS}$-only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses (A0 through A7) with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power. All four devices may be refreshed together by enabling $\overline{RAS}1$-$\overline{RAS}4$ simultaneously.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

The $\overline{CAS}$-before-$\overline{RAS}$ refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CLRL}) and holding it low after $\overline{RAS}$ falls (see parameter t_{RLCHR}). For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally.

hidden refresh

Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a "$\overline{RAS}$-only" refresh cycle. The external address is also ignored during the hidden refresh cycles.

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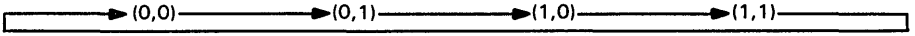
page mode (TM4256FC1)

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the module. Thus, the time required to setup and strobe sequential row addresses for the same page is eliminated.

nibble mode (TM4257FC1)

Nibble-mode operation allows high-speed serial read, write, or read-modify-write access of 1 to 4 bits of data. The first bit is accessed in the normal manner with read data coming out at $t_{a(C)}$ time. The next sequential nibble bits can be read or written by cycling $\overline{CAS}$ while $\overline{RAS}$ remains low. The first bit is determined by the row and column addresses, which need to be supplied only for the first access. Column A8 and row A8 (CA8, RA8) provide the two binary bits for initial selection of the nibble addresses. Thereafter, the falling edge of $\overline{CAS}$ will access the next bit of the circular 4-bit nibble in the following sequence:



In nibble-mode, all normal memory operations (read, write, or ready-modify-write) may be performed in any desired combination.

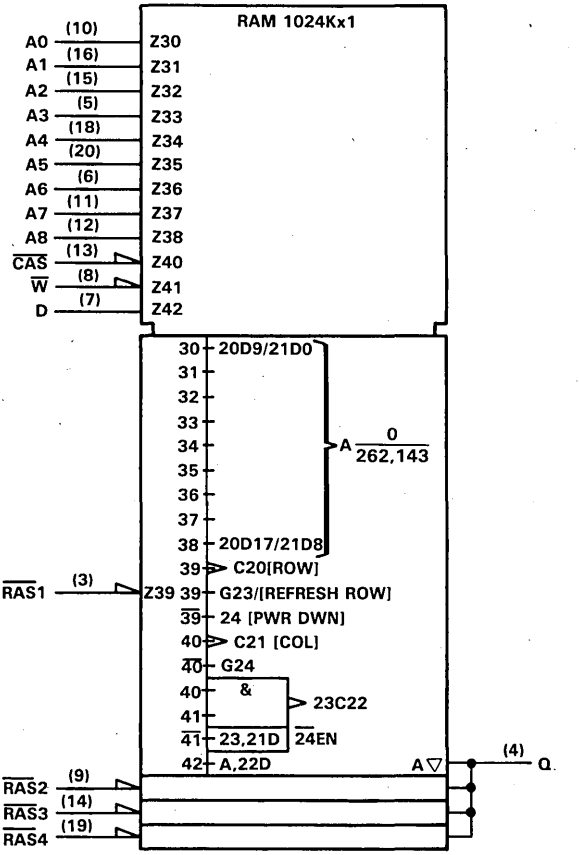
power up

To achieve proper operation, an initial pause of 200 μs is required after power up followed by a minimum of eight initialization cycles.

single-in-line package and components

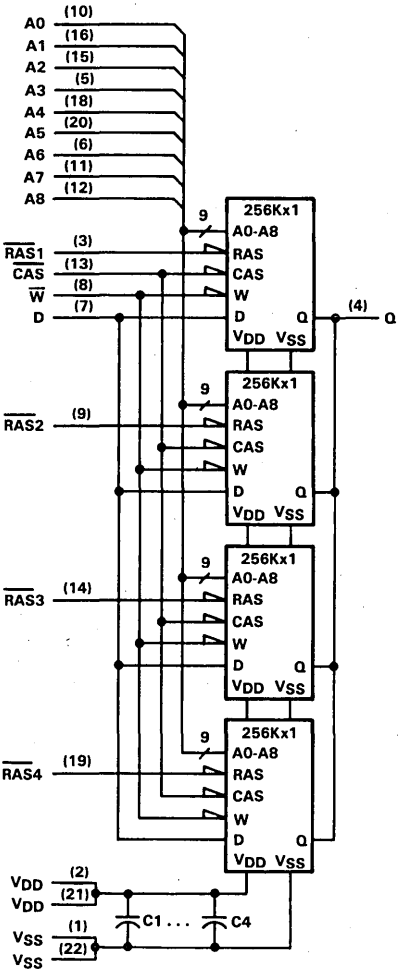
PC substrate: 0,79 mm (0.031 inch) minimum thickness
Bypass capacitors: Multilayer ceramic
Leads: Tin/lead solder coated over phosphor-bronze

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range for any pin except V_{DD} and data out (see Note 1) . . . . . −1.5 V to 10 V
Voltage range on V_{DD} supply and data out with respect to V_{SS} . . . . . −1 V to 7 V
Short circuit output current for any output . . . . . 50 mA
Power dissipation . . . . . 4 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	−1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TM425_FC1-12			TM425_FC1-15			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4		V_{DD}	2.4		V_{DD}	V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA	0		0.4	0		0.4	V
I_I	Input current (leakage)	V_I = 0 V to 6.5 V, V_{DD} = 5 V, All other pins = 0 V			±10			±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10			±10	μA
I_{DD1}	Average operating current during read or write cycle	t_c = minimum cycle, Output open‡		65	78		55	68	mA
I_{DD2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, Output open		10	18		10	18	mA
I_{DD3}	Average refresh current	t_c = minimum cycle, $\overline{CAS}$ high and $\overline{RAS}$ cycling, Output open		180	240		160	212	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low and $\overline{CAS}$ cycling, Output open‡		35	48		30	43	mA
I_{DD5}	Average nibble-mode current	$t_{c(N)}$ = minimum cycle, $\overline{RAS}$ low and $\overline{CAS}$ cycling, Output open‡		32	44		27	39	mA

†All typical values are at T_A = 25°C and nominal supply voltages.
‡Assuming standard operation of one device access.

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electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TM425_FC1-20			UNIT
			MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4		V_{DD}	V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA	0		0.4	V
I_I	Input current (leakage)	V_I = 0 V to 6.5 V, V_{DD} = 5 V, All other pins = 0 V			±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10	μA
I_{DD1}	Average operating current during read or write cycle	t_c = minimum cycle, Output open‡		45	58	mA
I_{DD2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, Output open		10	18	mA
I_{DD3}	Average refresh current	t_c = minimum cycle, $\overline{CAS}$ high and $\overline{RAS}$ cycling, Output open		140	192	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low and $\overline{CAS}$ cycling, Output open‡		25	35	mA
I_{DD5}	Average nibble-mode current	$t_{c(N)}$ = minimum cycle, $\overline{RAS}$ low and $\overline{CAS}$ cycling, Output open‡		22	32	mA

†All typical values are at T_A = 25°C and nominal supply voltages.
‡Assuming standard operation of one device access.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		28	pF
$C_{i(D)}$	Input capacitance, data inputs		28	pF
$C_{i(RAS)}$	Input capacitance, $\overline{RAS}$ inputs		8	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$ input		32	pF
$C_{i(CAS)}$	Input capacitance, $\overline{CAS}$ input		32	pF
$C_{o(Q)}$	Output capacitance, data output		40	pF
$C_{o(VDD)}$	Decoupling capacitance	0.4		μF

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TM425_FC1-12		TM425_FC1-15		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		60		75	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, Load = 2 Series 74 TTL gates	t_{RAC}		120		150	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	30	0	30	ns

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TM425_FC1-20		UNIT
				MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		100	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, Load = 2 Series 74 TTL gates	t_{RAC}		200	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	35	ns

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timing requirements over recommended supply voltage range and operating free-air temperature range

		ALT. SYMBOL	TM425_FC1-12 MIN	TM425_FC1-12 MAX	UNIT
$t_{c(P)}$	Page-mode cycle time (read or write cycle)	t_{PC}	120		ns
$t_{c(PM)}$	Page-mode cycle time (read-modify-write cycle)	t_{PCM}	165		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	230		ns
$t_{c(W)}$	Write cycle time	t_{WC}	230		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	275		ns
$t_{w(CH)P}$	Pulse duration, $\overline{CAS}$ high (page mode)	t_{CP}	50		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (non-page mode)	t_{CPN}	25		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low‡	t_{CAS}	60	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high	t_{RP}	100		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low§	t_{RAS}	120	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	40		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		ns
$t_{su(WCL)}$	Early write-command setup time before $\overline{CAS}$ low	t_{WCS}	0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	40		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	40		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	20		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	15		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	80		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	35		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	95		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	35		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	10		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	35		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	95		ns

Continued next page.

NOTE 3: Timing measurements are referenced to V_{IL} max and V_{IH} min.

†All cycle times assume t_t = 5 ns.

‡In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$). This applies to page-mode read-modify-write also.

§In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).

timing requirements over recommended supply voltage range and operating free-air temperature range (continued)

		ALT. SYMBOL	TM425_FC1-12 MIN	TM425_FC1-12 MAX	UNIT
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	120		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	60		ns
t_{RLCHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high¶	t_{CHR}	25		ns
t_{CLRL}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low¶	t_{CSR}	25		ns
t_{RHCL}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low¶	t_{RPC}	20		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{CWD}	60		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	30	60	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{RWD}	120		ns
t_{rf}	Refresh time interval	t_{REF}		4	ms

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NOTE 3: Timing measurements are referenced to V_{IL} max and V_{IH} min.
¶$\overline{CAS}$-before-$\overline{RAS}$ refresh only.

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timing requirements over recommended supply voltage range and operating free-air temperature range (continued)

		ALT. SYMBOL	TM425_FC1-15		TM425_FC1-20		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(P)}$	Page-mode cycle time (read or write cycle)	t_{PC}	145		190		ns
$t_{c(PM)}$	Page-mode cycle time (read-modify-write cycle)	t_{PCM}	190		245		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	260		330		ns
$t_{c(W)}$	Write cycle time	t_{WC}	260		330		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	305		370		ns
$t_{w(CH)P}$	Pulse duration, $\overline{CAS}$ high (page mode)	t_{CP}	60		80		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (non-page mode)	t_{CPN}	25		30		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low‡	t_{CAS}	75	10,000	100	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high	t_{RP}	100		120		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low§	t_{RAS}	150	10,000	200	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	45		55		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	50	3	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		0		ns
$t_{su(WCL)}$	Early write-command setup time before $\overline{CAS}$ low	t_{WCS}	0		0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	45		60		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	45		60		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	25		30		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	15		20		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	100		130		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	45		55		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	120		155		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	45		55		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	10		15		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	45		55		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	120		155		ns

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NOTE 3: Timing measurements are referenced to V_{IL} max and V_{IH} min.

†All cycle times assume t_t = 5 ns.

‡In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$). This applies to page-mode read-modify-write also.

§In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).

timing requirements over recommended supply voltage range and operating free-air temperature range (concluded)

		ALT. SYMBOL	TM425_FC1-15		TM425_FC1-20		UNIT
			MIN	MAX	MIN	MAX	
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	150		200		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	75		100		ns
t_{RLCHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high¶	t_{CHR}	30		35		ns
t_{CLRL}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low¶	t_{CSR}	30		35		ns
t_{RHCL}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low¶	t_{RPC}	20		25		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{CWD}	70		90		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	30	75	30	100	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{RWD}	145		190		ns
t_{rf}	Refresh time interval	t_{REF}		4		4	ms

NOTE 3: Timing measurements are referenced to V_{IL} max and V_{IH} min.
¶$\overline{CAS}$-before-$\overline{RAS}$ refresh only.

NIBBLE-MODE CYCLE

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		ALT. SYMBOL	TM4257FC1-12		TM4257FC1-15		TM4257FC1-20		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(CN)}$	Nibble-mode access time from $\overline{CAS}$	t_{NCAC}		30		40		50	ns

timing requirements over recommended supply voltage range and operating free-air temperature range

		ALT. SYMBOL	TM4257FC1-12		TM4257FC1-15		TM4257FC1-20		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(N)}$	Nibble-mode cycle time	t_{NC}	60		75		90		ns
$t_{c(rdWN)}$	Nibble-mode read-modify-write cycle time	t_{NRMW}	85		105		130		
t_{CLRHN}	Nibble-mode delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{NRSH}	30		40		50		
t_{CLWLN}	Nibble-mode delay time, $\overline{CAS}$ to $\overline{W}$ delay	t_{NCWD}	25		30		40		
$t_{w(CLN)}$	Nibble-mode pulse duration, $\overline{CAS}$ low	t_{NCAS}	30		40		50		
$t_{w(CHN)}$	Nibble-mode pulse duration, $\overline{CAS}$ high	t_{NCP}	20		25		30		
$t_{w(CRWN)}$	Nibble-mode read-modify-write pulse duration, $\overline{CAS}$ low	t_{NCRW}	55		70		90		
$t_{su(WCHN)}$	Nibble-mode write command setup time before $\overline{CAS}$ high	t_{NCWL}	25		35		45		

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PARAMETER MEASUREMENT INFORMATION

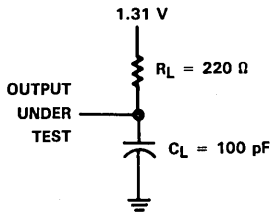
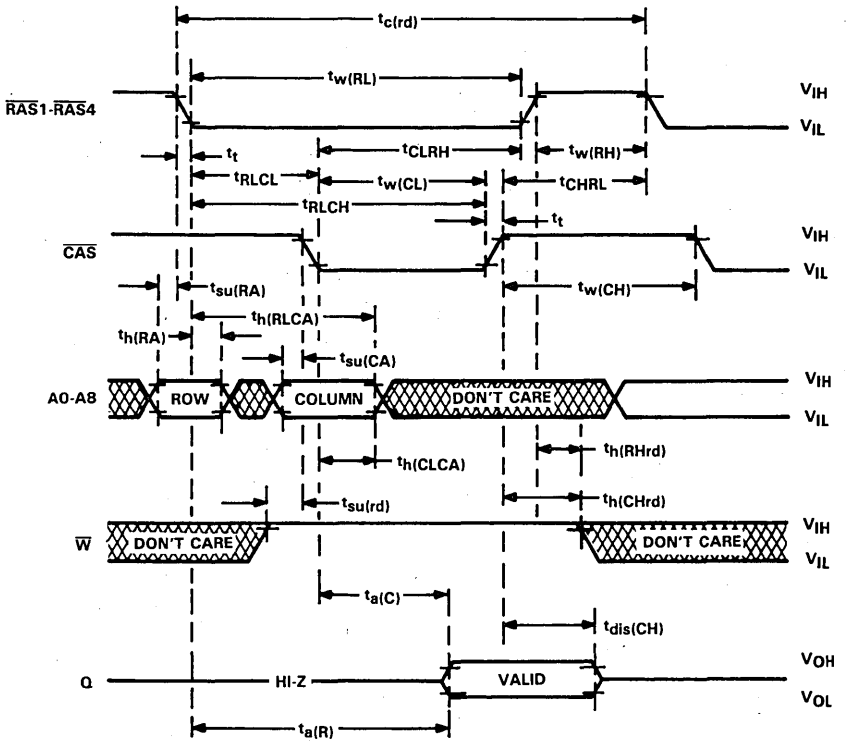
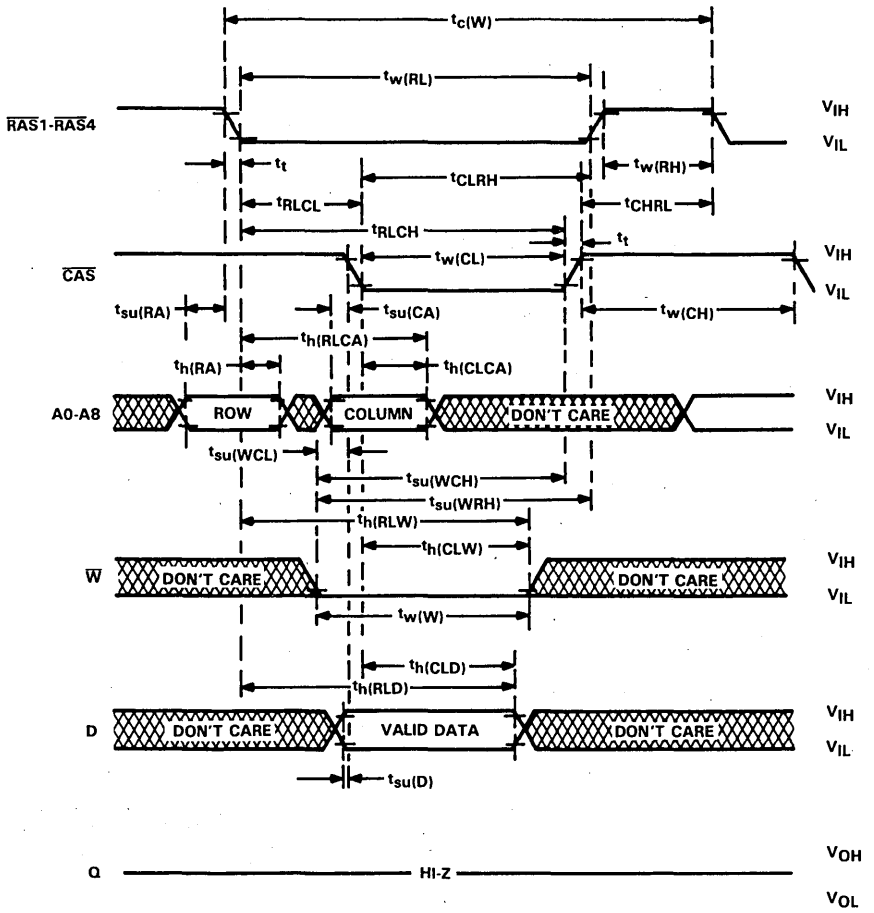


FIGURE 1. LOAD CIRCUIT

read cycle timing



early write cycle timing



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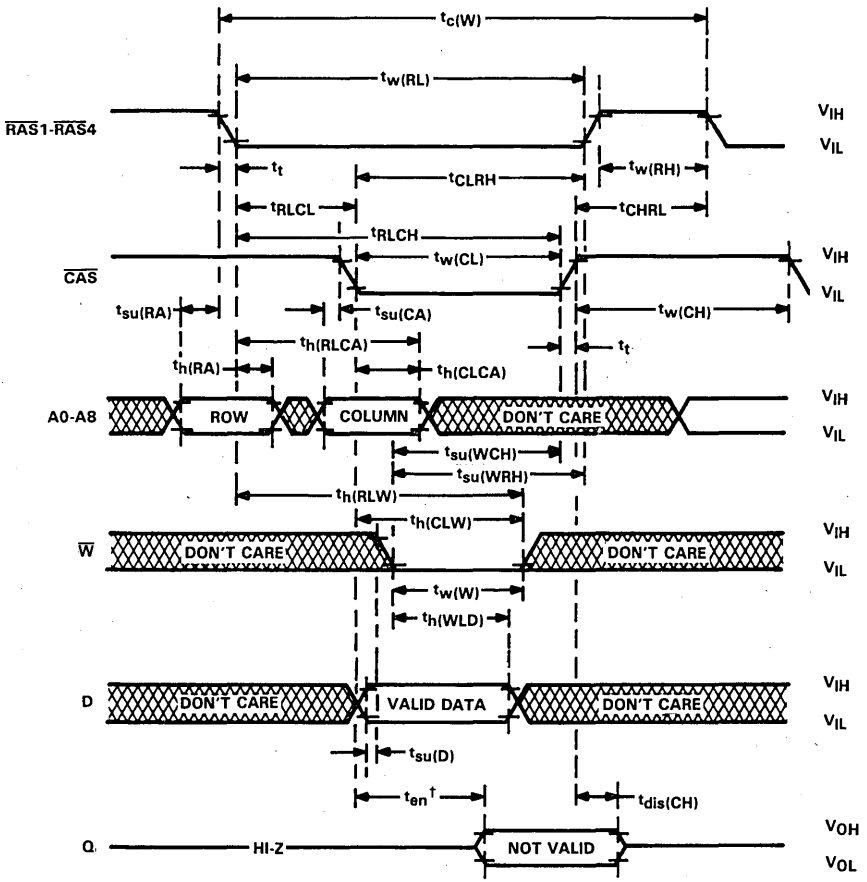
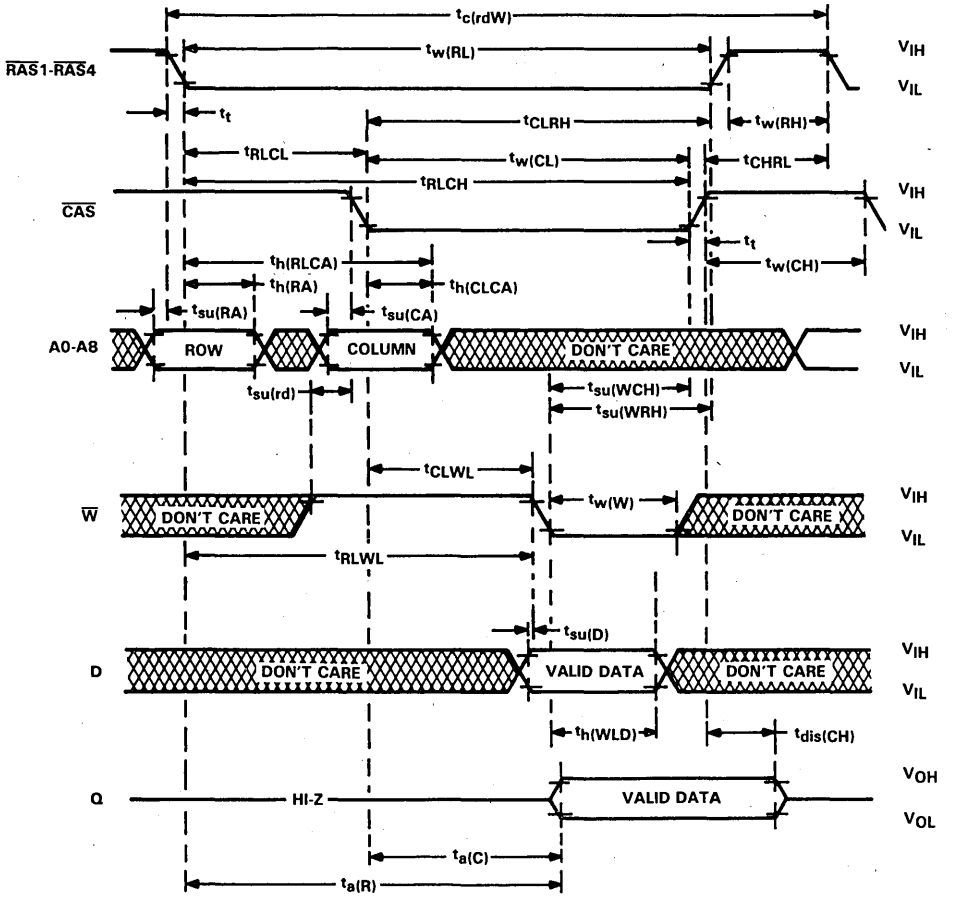
write cycle timing



†The enable time (t_{en}) for a write cycle is equal in duration to the access time from $\overline{CAS}$ ($t_{a(C)}$) in a read cycle; but the active levels at the output are invalid.

read-write/read-modify-write cycle timing



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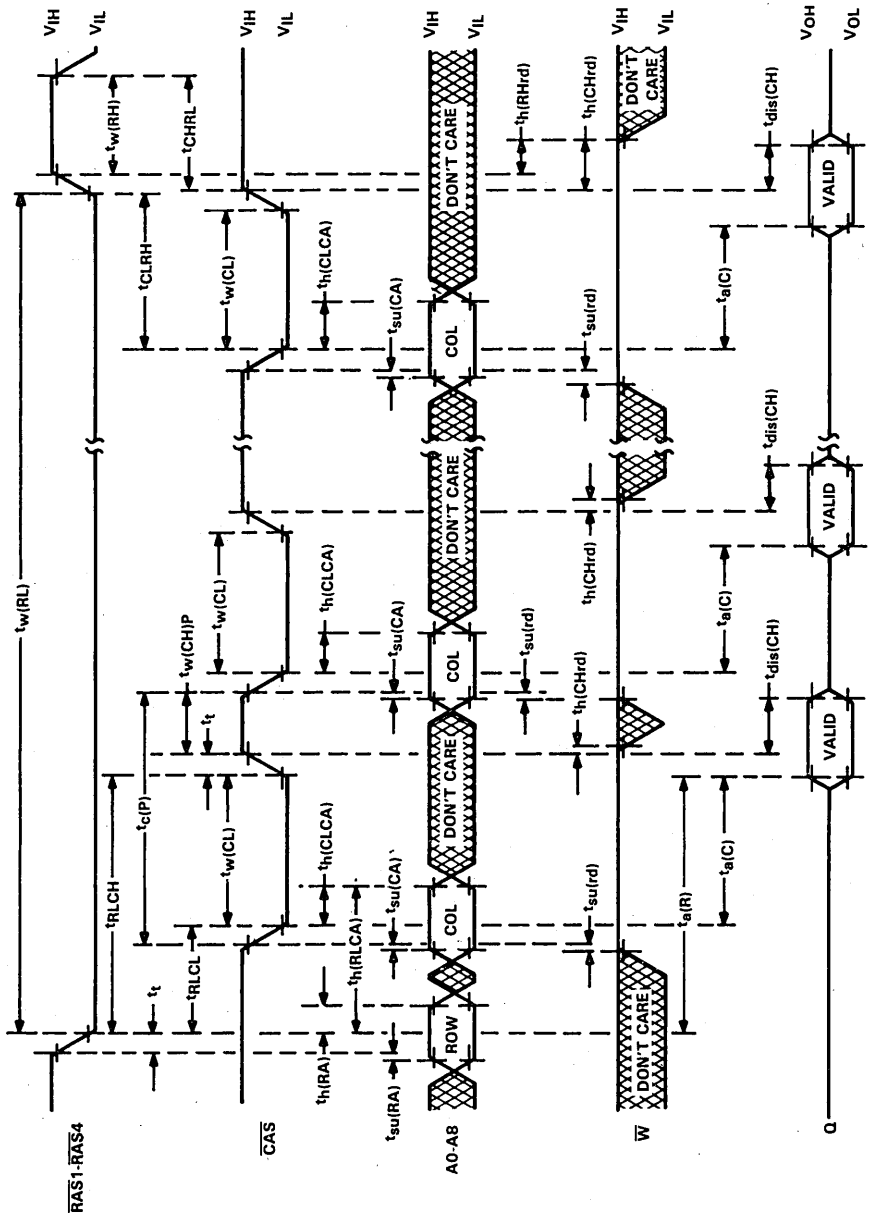
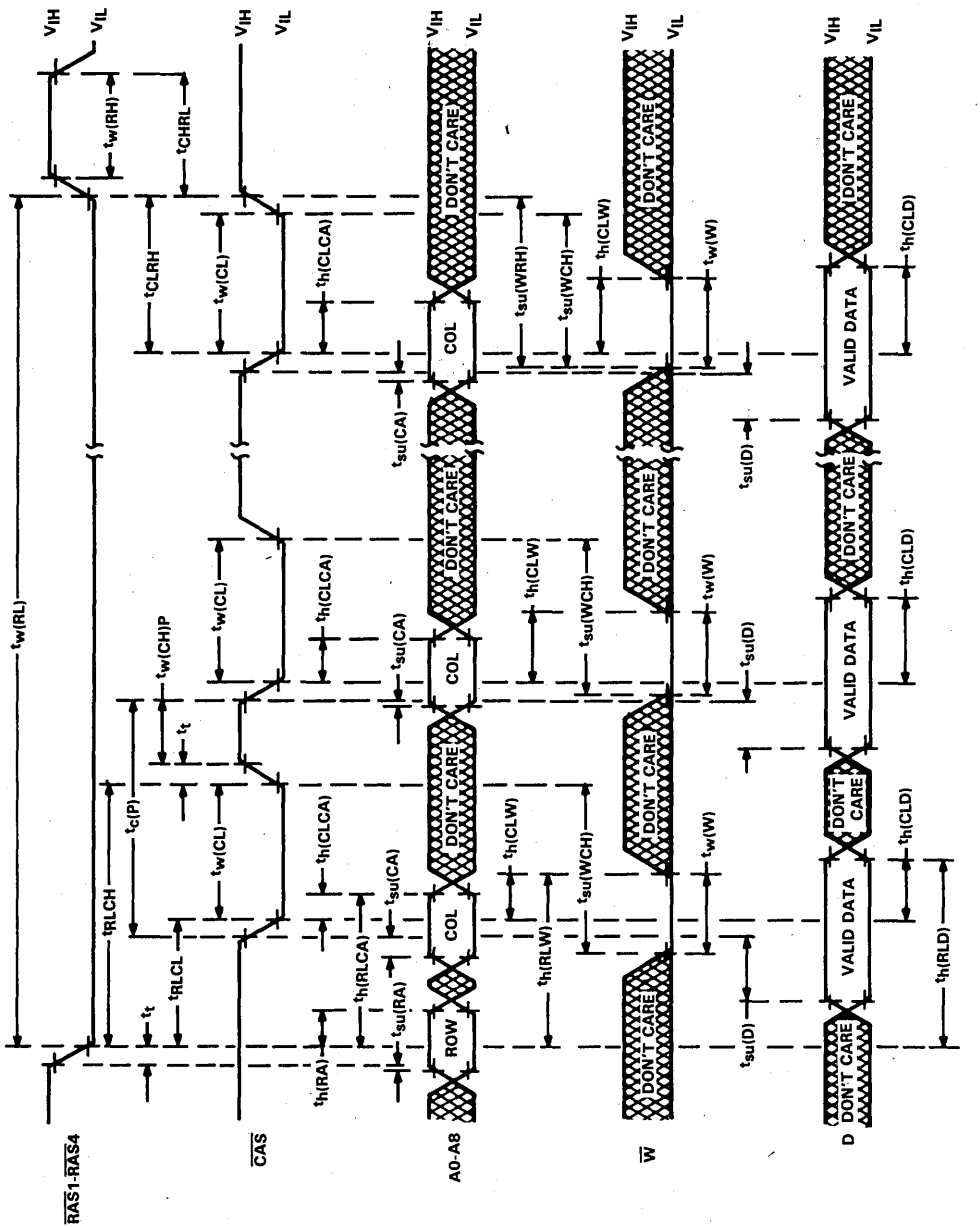
page-mode read cycle timing



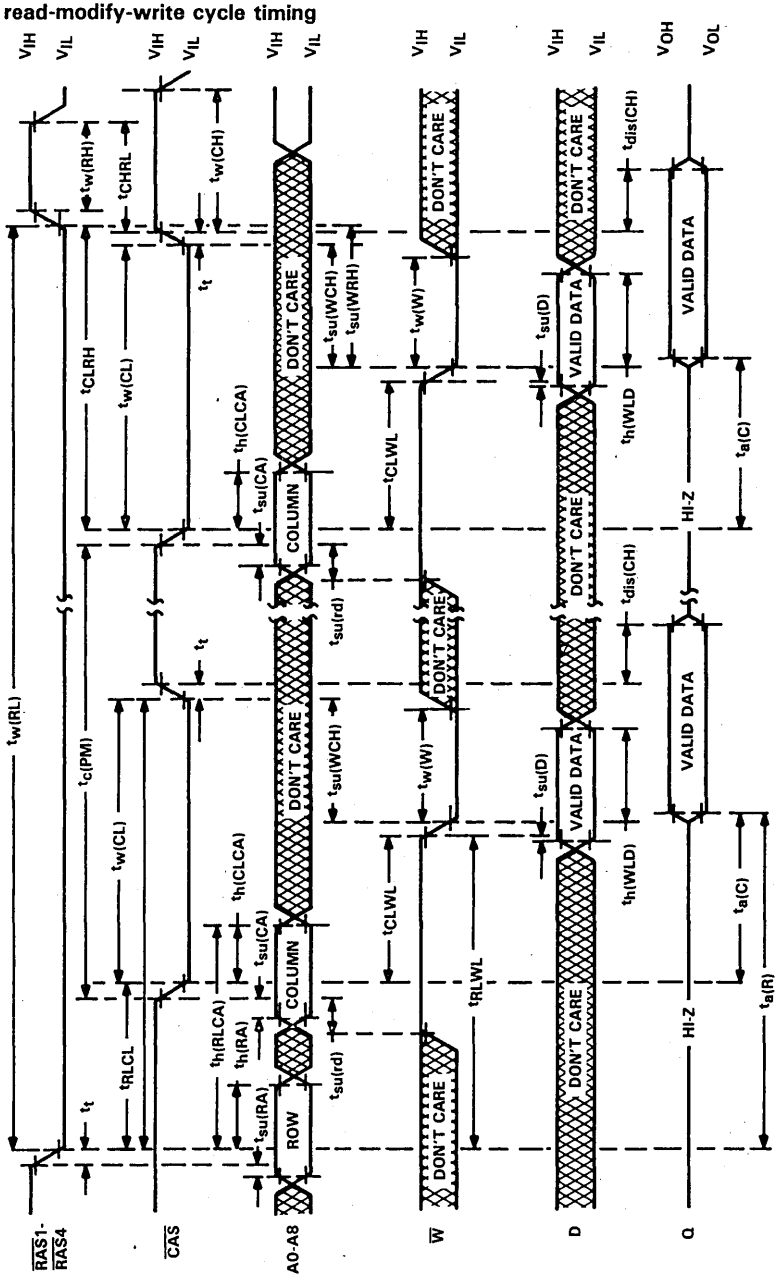
NOTE 4: A write cycle can be intermixed with read cycles as long as the write timing specifications are not violated.

page-mode write cycle timing



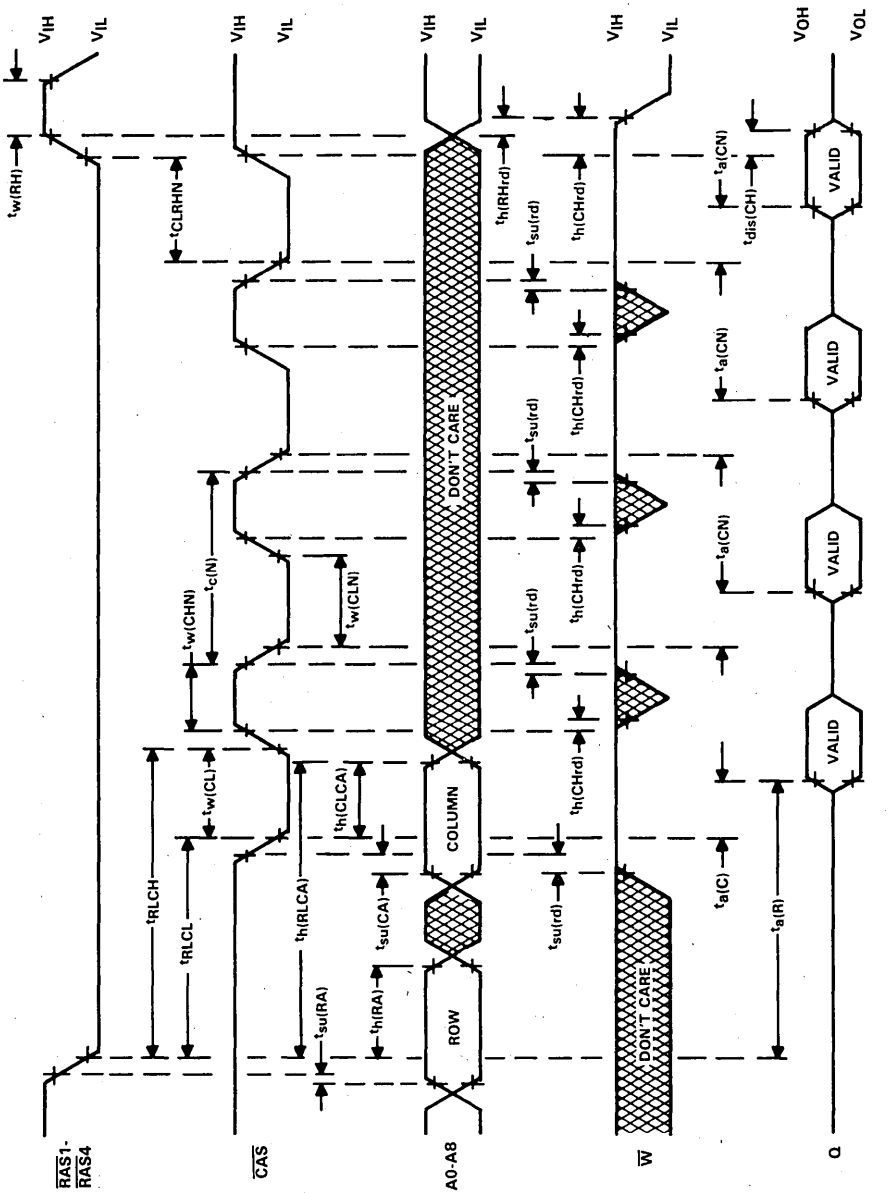
NOTE 5: A read cycle can be intermixed with write cycles as long as read timing specifications are not violated.

page-mode read-modify-write cycle timing



NOTE 6: A read or a write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

nibble-mode read cycle timing



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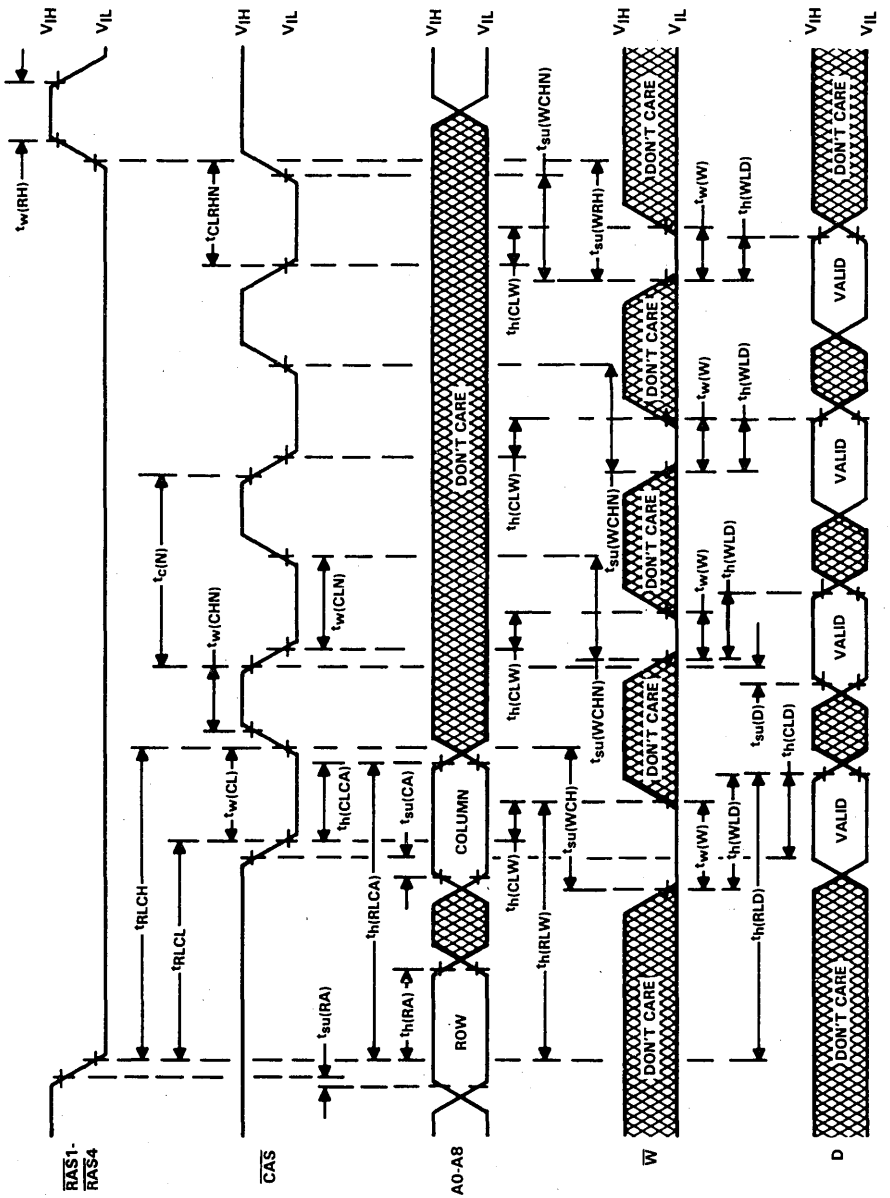
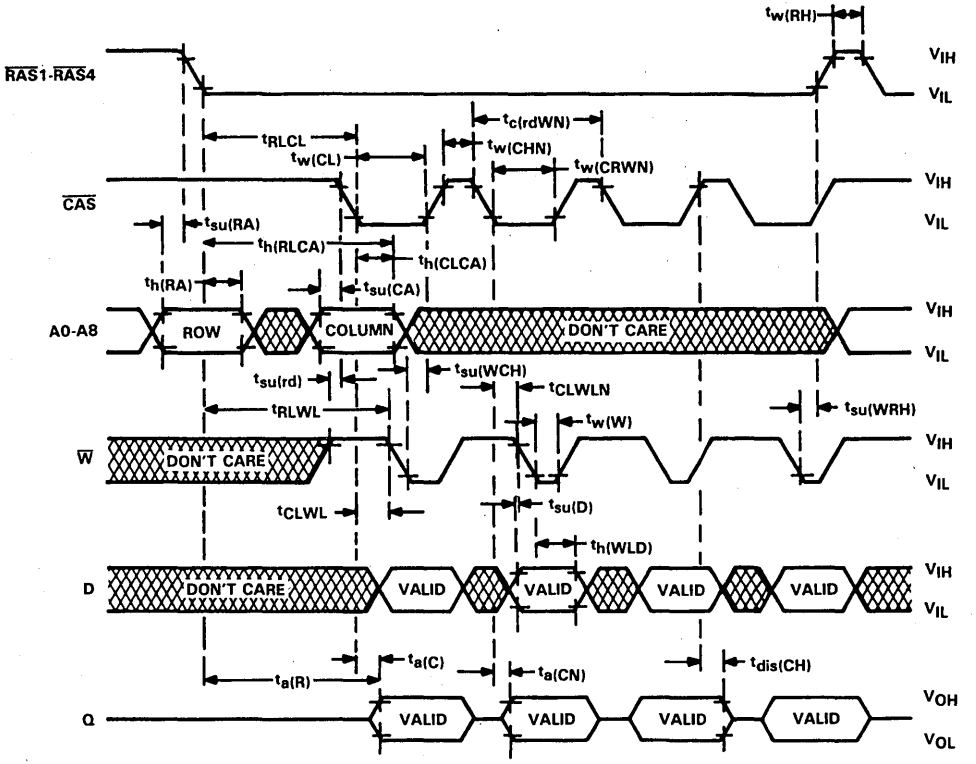
nibble-mode write cycle timing



nibble-mode read-modify-write-cycle timing



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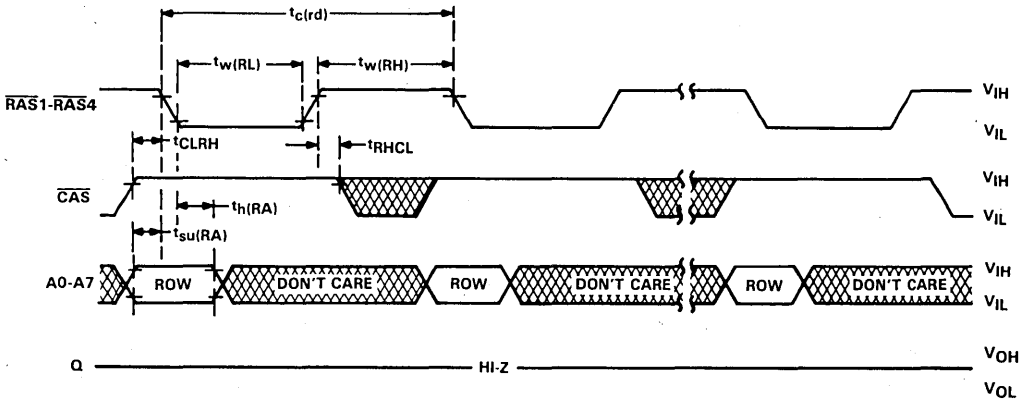
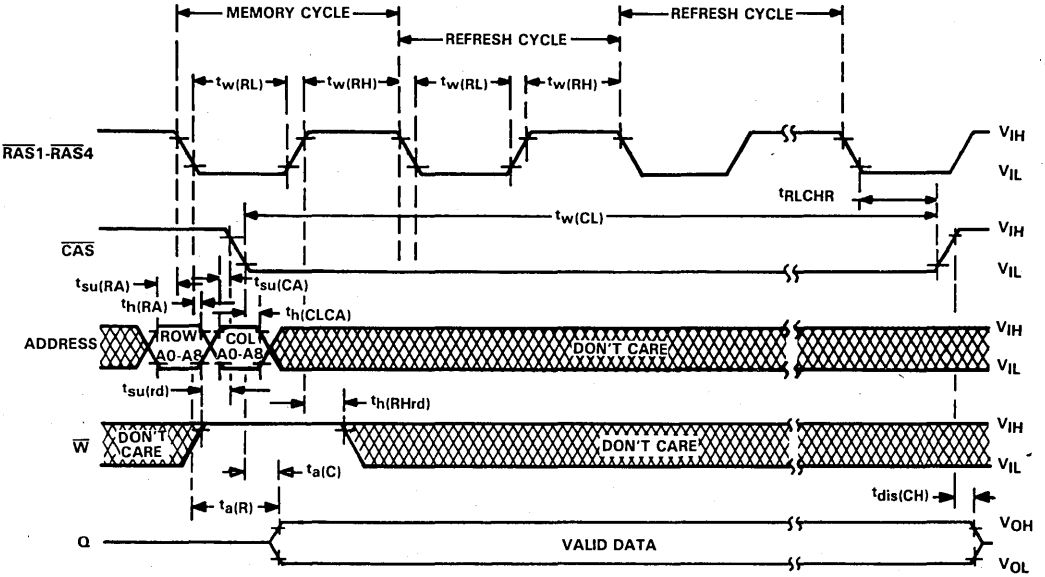
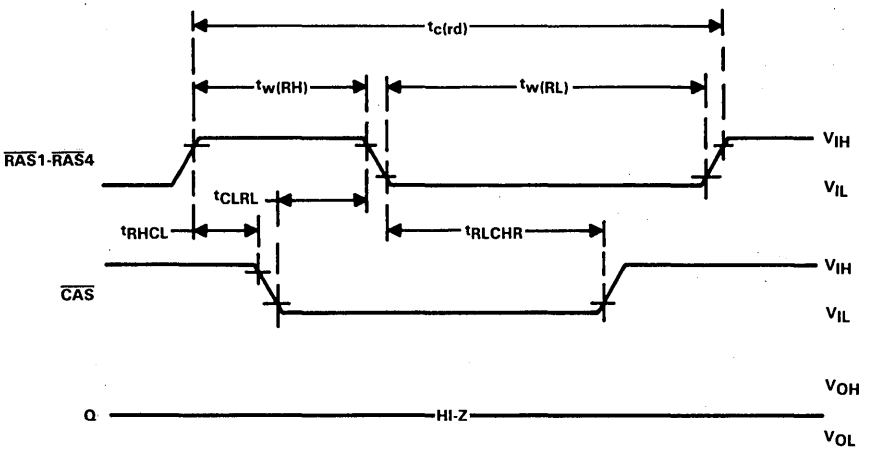
$\overline{RAS}$-only refresh cycle timing



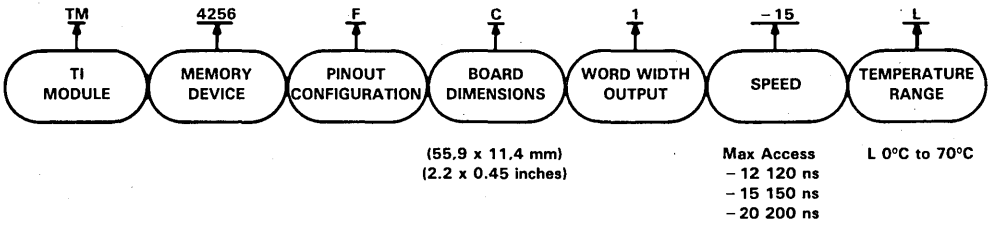
hidden refresh cycle timing



automatic ($\overline{CAS}$-before-$\overline{RAS}$) refresh cycle timing



TI single-in-line package nomenclature



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TM4256FL8, TM4256GU8, TM4257FL8, TM4257GU8
262,144 BY 8-BIT DYNAMIC RAM MODULES

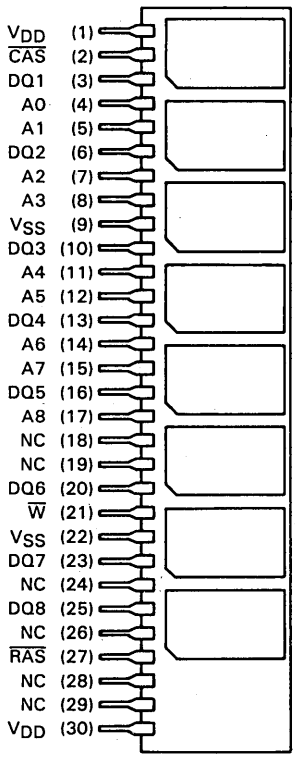
OCTOBER 1985 – REVISED NOVEMBER 1985

- 262,144 X 8 Organization
- Single 5-V Supply (10% Tolerance)
- 30-Pin Single-in-Line Package (SIP)
  - —Pinned Module for Through-Hole Insertion (TM425_FL8)
  - —Leadless Module for Use with Sockets (TM425_GU8)
- Utilizes Eight 256K Dynamic RAMs in Plastic Chip Carrier
- Long Refresh Period . . . 4 ms (256 Cycles)
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Outputs
- Performance Ranges:

	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)
TM425___8-12	120 ns	60 ns	230 ns
TM425___8-15	150 ns	75 ns	260 ns
TM425___8-20	200 ns	100 ns	330 ns

- Common $\overline{CAS}$ Control for Eight Common Data-In and Data-Out Lines
- Low Power Dissipation
- Operating Free-Air Temperature . . . 0°C to 70°C
- Downward Compatible with 64K X 8 SIP (TM4164FL8, TM4164FM8)

TM425_FL8 . . . L SINGLE-IN-LINE PACKAGE
(TOP VIEW)



description

The TM425___8 series are 2048K, dynamic random-access memory modules organized as 262,144 × 8 bits in a 30-pin single-in-line package comprising eight TMS425_FML, 262,144 × 1 bit dynamic RAM's in 18-lead plastic chip carriers mounted on top of a substrate together with decoupling capacitors mounted beneath the chip carriers. The onboard capacitors eliminate the need for bypassing on the motherboard and offer superior performance over equivalent leaded capacitors due to reduced lead inductance. Also, with 0.3 inch board spacing the TM425___8 has a density of ten devices per square inch (approximately 4X the density of DIPs). With the elimination of bypass capacitors on the motherboard, reduced PC

PIN NOMENCLATURE TM425_FL8	
A0-A8	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1-DQ8	Data In/Data Out
NC	No Connection
$\overline{RAS}$	Row-Address Strobe
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

board size, and fewer plated-through holes, a cost savings can be realized.

The TM425___8 features $\overline{RAS}$ access times of 120 ns, 150 ns, and 200 ns maximum. Power dissipation as low as 2200 mW typical operating and 100 mW typical standby for 200 ns devices.

Refresh period is extended to 4 milliseconds, and during this period each of the 256 rows must be strobed with $\overline{RAS}$ in order to retain data. $\overline{CAS}$ can remain high during the refresh sequence to conserve power.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address lines and data in are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TM425___8 is rated for operation from 0°C to 70°C.

presence detect

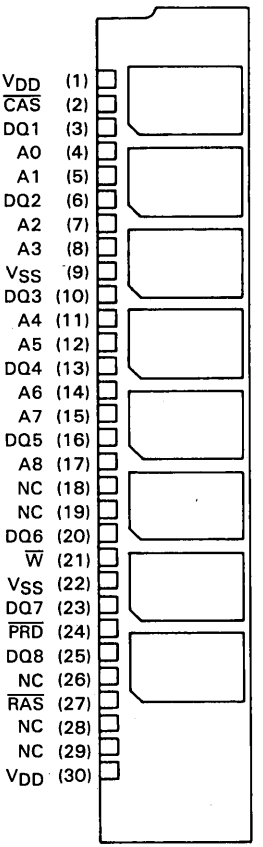
This feature is included on the TM425_GU8 to allow for hardware presence detection of the memory module. The $\overline{PRD}$ pin for each module in the system should be pulled high through a pull-up resistor, resulting in a logic one when no module is present. When a module is present, $\overline{PRD}$ is a logic zero as this pin is connected to V_{SS} on the module. $\overline{PRD}$ can only be used to detect a modules' presence, not its functionality. In a system not requiring presence detect, it is recommended that this pin be left as a no connect; this allows the use of either type of module without adverse effects.

operation

address (A0 through A8)

Eighteen address bits are required to decode 1 of 262,144 storage cell locations on each of the eight chips. Nine row-address bits are set up on pins A0 through A8 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the nine column-address bits are set up on pins A0 through A8 and latched onto the chip by the column-address strobes. All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers for M1-M8.

TM425_GU8 . . . U SINGLE-IN-LINE PACKAGE
(TOP VIEW)



PIN NOMENCLATURE TM425_GU8	
A0-A8	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1-DQ8	Data In/Data Out
NC	No Connection
$\overline{PRD}$	Presence Detect (V_{SS})
$\overline{RAS}$	Row-Address Strobe
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

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write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data inputs are disabled when the read mode is selected. The common I/O feature of the TM425___8 dictates the use of early write cycles to prevent contention on DQ. When $\overline{W}$ goes low prior to $\overline{CAS}$, the data outs will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data in (DQ1-DQ8)

Data is written during a write cycle. The falling edge of $\overline{CAS}$ strobes data into the on-chip data latches. These latches can be driven from standard TTL circuits without a pull-up resistor. In the early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal.

data out (DQ1-DQ8)

The three-state output buffers provide direct TTL compatibility (no pull-up resistor required) with a fan out of two Series 74 TTL loads for each output. Data out is the same polarity as data in. The outputs are in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the outputs go active after the access time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ is satisfied. The outputs become valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low: $\overline{CAS}$ going high returns it to a high-impedance state. In the early write cycle, the outputs are always in the high-impedance state, a necessity due to the common I/O feature of the TM425___8.

refresh

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffers are in the high-impedance state unless $\overline{CAS}$ is applied, the $\overline{RAS}$-only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses (A0 through A7) with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

The $\overline{CAS}$-before-$\overline{RAS}$ refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CLRL}) and holding it low after $\overline{RAS}$ falls (see parameter t_{RLCHR}). For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally.

hidden refresh

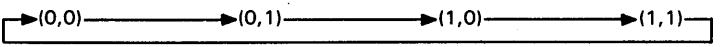
Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a "$\overline{RAS}$-only" refresh cycle. The external address is also ignored during the hidden refresh cycles.

page-mode (TM4256__8)

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the module. Thus, the time required to setup and strobe sequential row addresses for the same page is eliminated.

nibble mode (TM4257__8)

Nibble-mode operation allows high-speed serial read, write, or read-modify-write access of 1 to 4 bits of data. The first bit is accessed in the normal manner with read data coming out at $t_{a(C)}$ time. The next sequential nibble bits can be read or written by cycling $\overline{CAS}$ while $\overline{RAS}$ remains low. The first bit is determined by the row and column addresses, which need to be supplied only for the first access. Column A8 and row A8 (CA8, RA8) provide the two binary bits for initial selection of the nibble addresses. Thereafter, the falling edge of $\overline{CAS}$ will access the next bit of the circular 4-bit nibble in the following sequence:



In nibble-mode, all normal memory operations (read, write, or ready-modify-write) may be performed in any desired combination.

power up

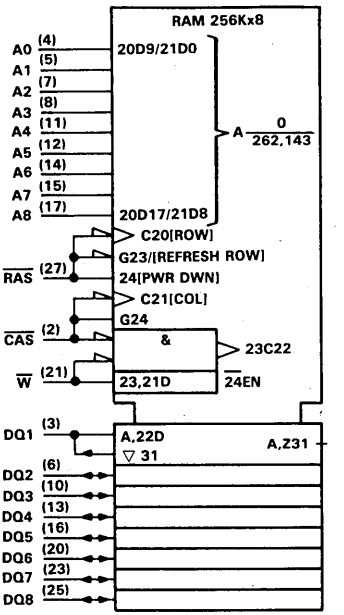
To achieve proper operation, an initial pause of 200 μs is required after power up followed by a minimum of eight initialization cycles.

5 Dynamic RAM Modules

single-in-line package and components

PC substrate: 0,79 mm (0.031 inch) minimum thickness
Bypass capacitors: Multilayer ceramic
Leads: Tin/lead solder coated over phosphor-bronze
Contact area for socketable devices: Nickel plate and solder plate on top of copper

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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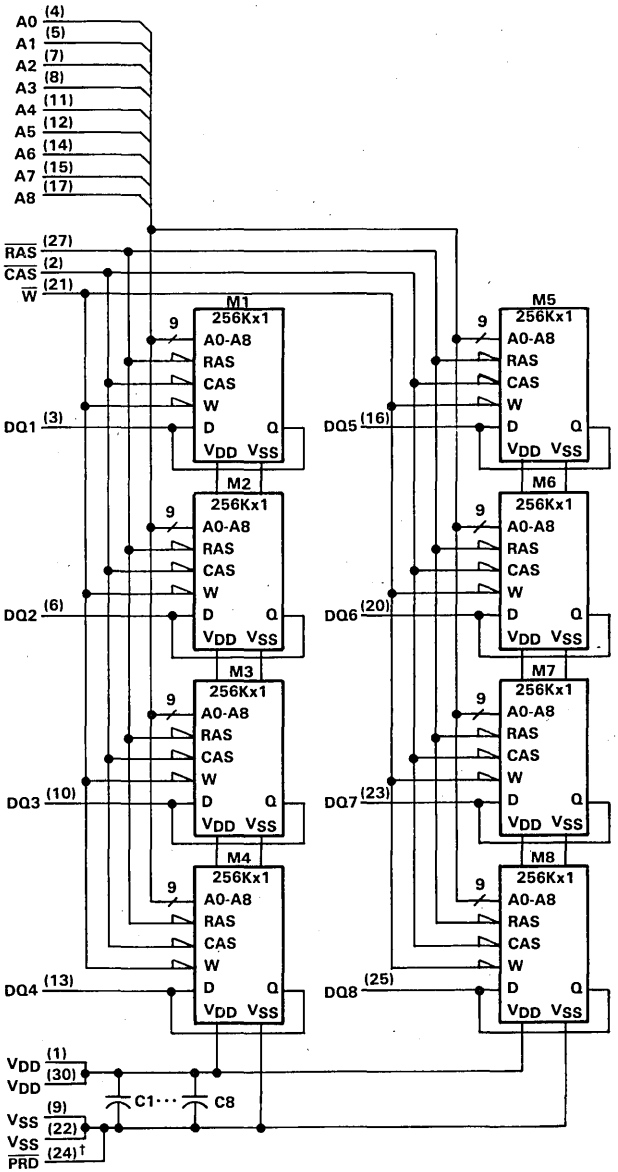
functional block diagram



†TM425_GU8 only.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range for any pin except V_{DD} and data out (see Note 1) . . . . . −1.5 V to 10 V
Voltage range on V_{DD} supply and data out with respect to V_{SS} . . . . . −1 V to 7 V
Short circuit output current for any output . . . . . 50 mA
Power dissipation . . . . . 8 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	−1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TM425___8-12			TM425___8-15			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4		V_{DD}	2.4		V_{DD}	V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA	0		0.4	0		0.4	V
I_I	Input current (leakage)	V_I = 0 V to 6.5 V, V_{DD} = 5 V, All other pins = 0 V			±10			±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10			±10	μA
I_{DD1}‡	Average operating current during read or write cycle	t_c = minimum cycle, All outputs open		520	624		440	544	mA
I_{DD2}‡	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, All outputs open		20	36		20	36	mA
I_{DD3}‡	Average refresh current	t_c = minimum cycle, $\overline{CAS}$ high and $\overline{RAS}$ cycling, All outputs open		360	480		320	424	mA
I_{DD4}‡	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low and $\overline{CAS}$ cycling, All outputs open		280	384		240	344	mA
I_{DD5}‡	Average nibble-mode current	$t_{c(N)}$ = minimum cycle, $\overline{RAS}$ low and $\overline{CAS}$ cycling, All outputs open		256	352		216	312	mA

†All typical values are at T_A = 25°C and nominal supply voltages.
‡I_{DD1}-I_{DD5} are measured with M1-M8 in the same mode (i.e., operating, standby, refresh, page mode, nibble mode).

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electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TM425___8-20			UNIT
			MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4		V_{DD}	V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA	0		0.4	V
I_I	Input current (leakage)	V_I = 0 V to 6.5 V, V_{DD} = 5 V, All other pins = 0 V			±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10	μA
I_{DD1}‡	Average operating current during read or write cycle	t_c = minimum cycle, All outputs open		360	464	mA
I_{DD2}‡	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, All outputs open		20	36	mA
I_{DD3}‡	Average refresh current	t_c = minimum cycle, $\overline{CAS}$ high and $\overline{RAS}$ cycling, All outputs open		280	384	mA
I_{DD4}‡	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low and $\overline{CAS}$ cycling, All outputs open		200	280	mA
I_{DD5}‡	Average nibble-mode current	$t_{c(N)}$ = minimum cycle, $\overline{RAS}$ low and $\overline{CAS}$ cycling, All outputs open		176	256	mA

†All typical values are at T_A = 25°C and nominal supply voltages.
‡I_{DD1}-I_{DD5} are measured with M1-M8 in the same mode (i.e., operating, standby, refresh, page mode, nibble mode).

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		56	pF
$C_{i(DQ)}$	Input capacitance, data inputs		TBD	pF
$C_{i(RAS)}$	Input capacitance, $\overline{RAS}$ input		64	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$ input		64	pF
$C_{i(CAS)}$	Input capacitance, $\overline{CAS}$ input		64	pF
$C_{o(VDD)}$	Decoupling capacitance	0.8		μF

Additional information on these products can be obtained from the factory as it becomes available.

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TM425___8-12		TM425___8-15		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		60		75	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, Load = 2 Series 74 TTL gates	t_{RAC}		120		150	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	35	0	35	ns

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TM425___8-20		UNIT
				MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		100	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, Load = 2 Series 74 TTL gates	t_{RAC}		200	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	35	ns

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timing requirements over recommended supply voltage range and operating free-air temperature range

		ALT. SYMBOL	TM425___8-12 MIN	TM425___8-12 MAX	UNIT
$t_{c(P)}$	Page-mode cycle time (read or write cycle)	t_{PC}	120		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	230		ns
$t_{c(W)}$	Write cycle time	t_{WC}	230		ns
$t_{w(CH)P}$	Pulse duration, $\overline{CAS}$ high (page mode)	t_{CP}	50		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (non-page mode)	t_{CPN}	25		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low	t_{CAS}	60	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge time)	t_{RP}	100		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low	t_{RAS}	120	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	40		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		ns
$t_{su(WCL)}$	Early write-command setup time before $\overline{CAS}$ low	t_{WCS}	0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	40		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	40		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	20		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	15		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	80		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	35		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	95		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	10		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	35		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	95		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	120		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	60		ns
t_{RLCHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high‡	t_{CHR}	25		ns
t_{CLRL}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low‡	t_{CSR}	25		ns
t_{RHCL}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low‡	t_{RPC}	20		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	30	60	ns
t_{rf}	Refresh time interval	t_{REF}		4	ms

NOTE 3: Timing measurements are referenced to V_{IL} max and V_{IH} min.
†All cycle times assume t_t = 5 ns.
‡$\overline{CAS}$-before-$\overline{RAS}$ refresh only.

timing requirements over recommended supply voltage range and operating free-air temperature range

		ALT. SYMBOL	TM425___8-15		TM425___8-20		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(P)}$	Page-mode cycle time (read or write cycle)	t_{PC}	145		190		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	260		330		ns
$t_{c(W)}$	Write cycle time	t_{WC}	260		330		ns
$t_{w(CH)P}$	Pulse duration, $\overline{CAS}$ high (page mode)	t_{CP}	60		80		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (non-page mode)	t_{CPN}	25		30		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low	t_{CAS}	75	10,000	100	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge time)	t_{RP}	100		120		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low	t_{RAS}	150	10,000	200	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	45		55		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	50	3	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		0		ns
$t_{su(WCL)}$	Early write-command setup time before $\overline{CAS}$ low	t_{WCS}	0		0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	45		60		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	45		60		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	25		30		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	15		20		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	100		130		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	45		55		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	120		155		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	10		15		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	45		55		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	120		155		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	150		200		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	75		100		ns
t_{RLCHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high‡	t_{CHR}	30		35		ns
t_{CLRL}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low‡	t_{CSR}	30		35		ns
t_{RHCL}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low‡	t_{RPC}	20		25		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	30	75	30	100	ns
t_{rf}	Refresh time interval	t_{REF}		4		4	ms

NOTE 3: Timing measurements are referenced to V_{IL} max and V_{IH} min.
†All cycle times assume t_t = 5 ns.
‡$\overline{CAS}$-before-$\overline{RAS}$ refresh only.

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NIBBLE-MODE CYCLE

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		ALT. SYMBOL	TM4257__8-12		TM4257__8-15		TM4257__8-20		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(CN)}$	Nibble-mode access time from $\overline{CAS}$	t_{NCAC}		30		40		50	ns

timing requirements over recommended supply voltage range and operating free-air temperature range

		ALT. SYMBOL	TM4257__8-12		TM4257__8-15		TM4257__8-20		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(N)}$	Nibble-mode cycle time	t_{NC}	60		75		90		ns
t_{CLRHN}	Nibble-mode delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{NRSH}	30		40		50		
t_{CLWLN}	Nibble-mode delay time, $\overline{CAS}$ to $\overline{W}$ delay	t_{NCWD}	25		30		40		
$t_{w(CLN)}$	Nibble-mode pulse duration, $\overline{CAS}$ low	t_{NCAS}	30		40		50		
$t_{w(CHN)}$	Nibble-mode pulse duration, $\overline{CAS}$ high	t_{NCP}	20		25		30		
$t_{su(WCHN)}$	Nibble-mode write command setup time before $\overline{CAS}$ high	t_{NCWL}	25		35		45		

PARAMETER MEASUREMENT INFORMATION

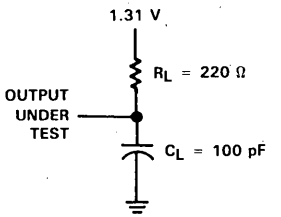
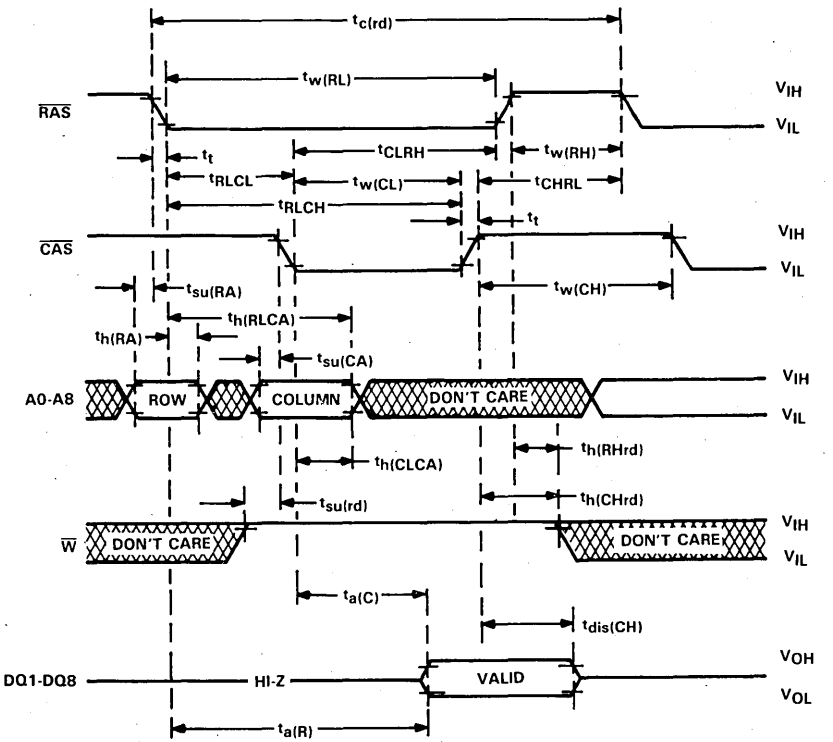


FIGURE 1. LOAD CIRCUIT

read cycle timing



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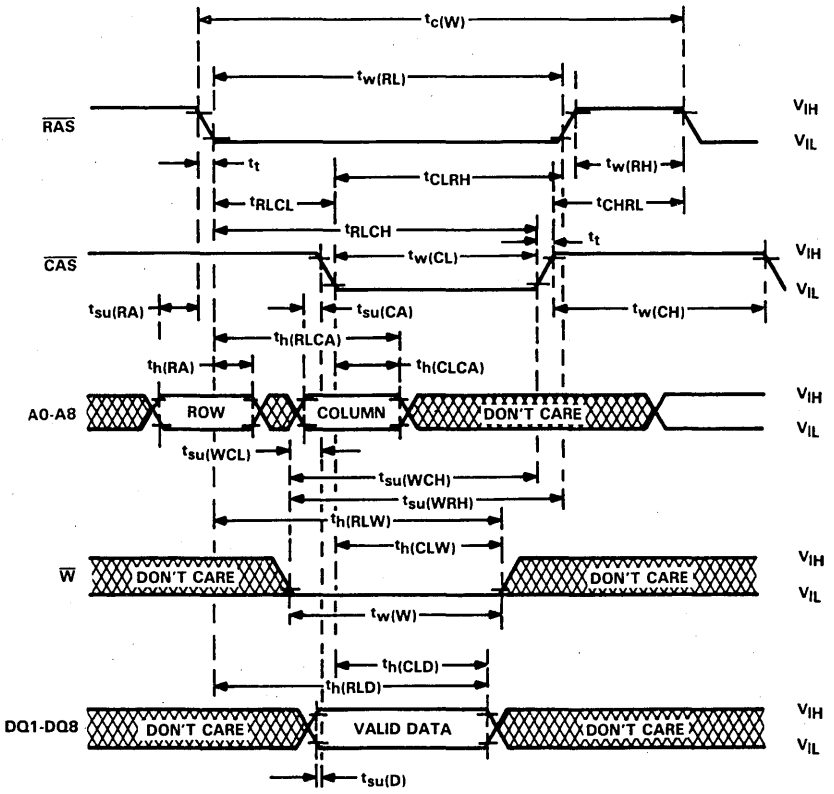
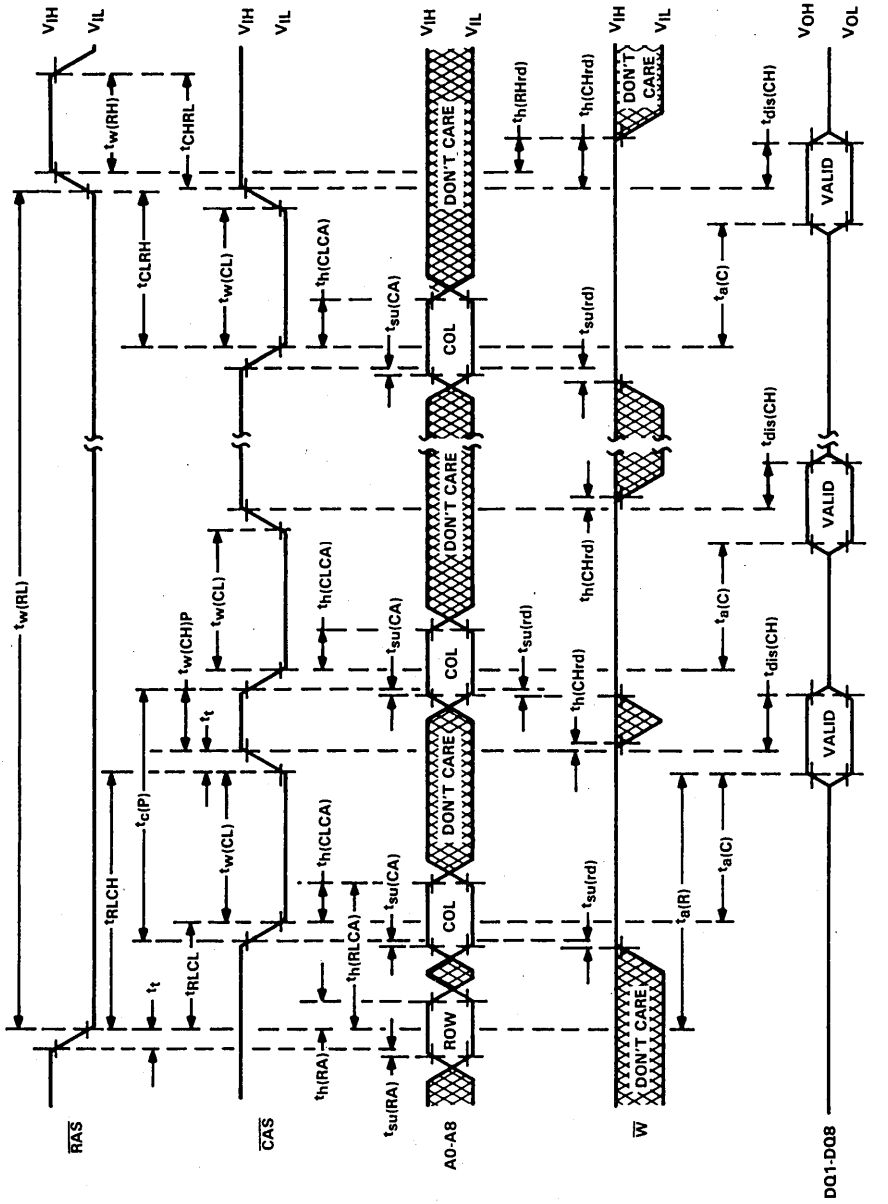
early write cycle timing

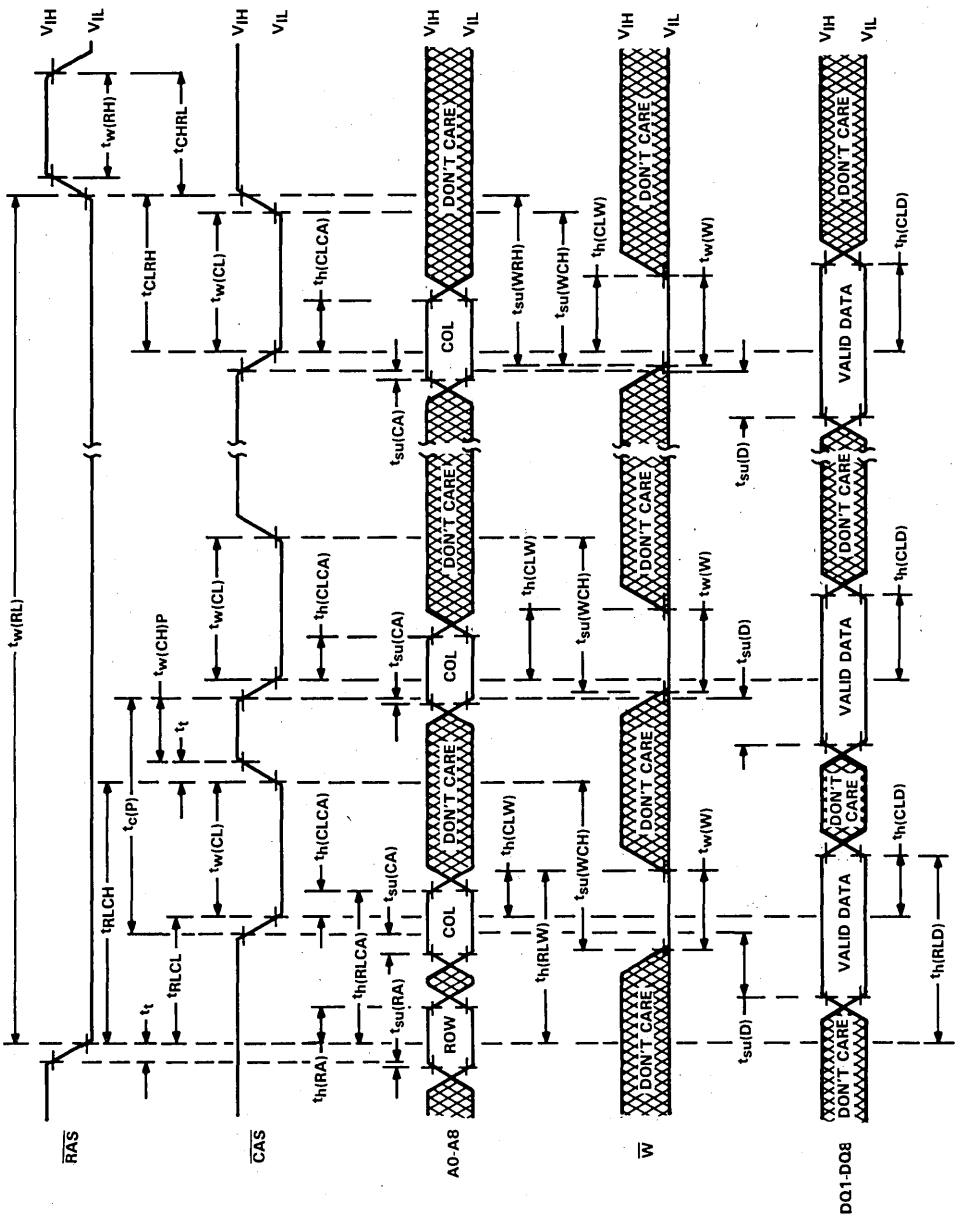


page-mode read cycle timing



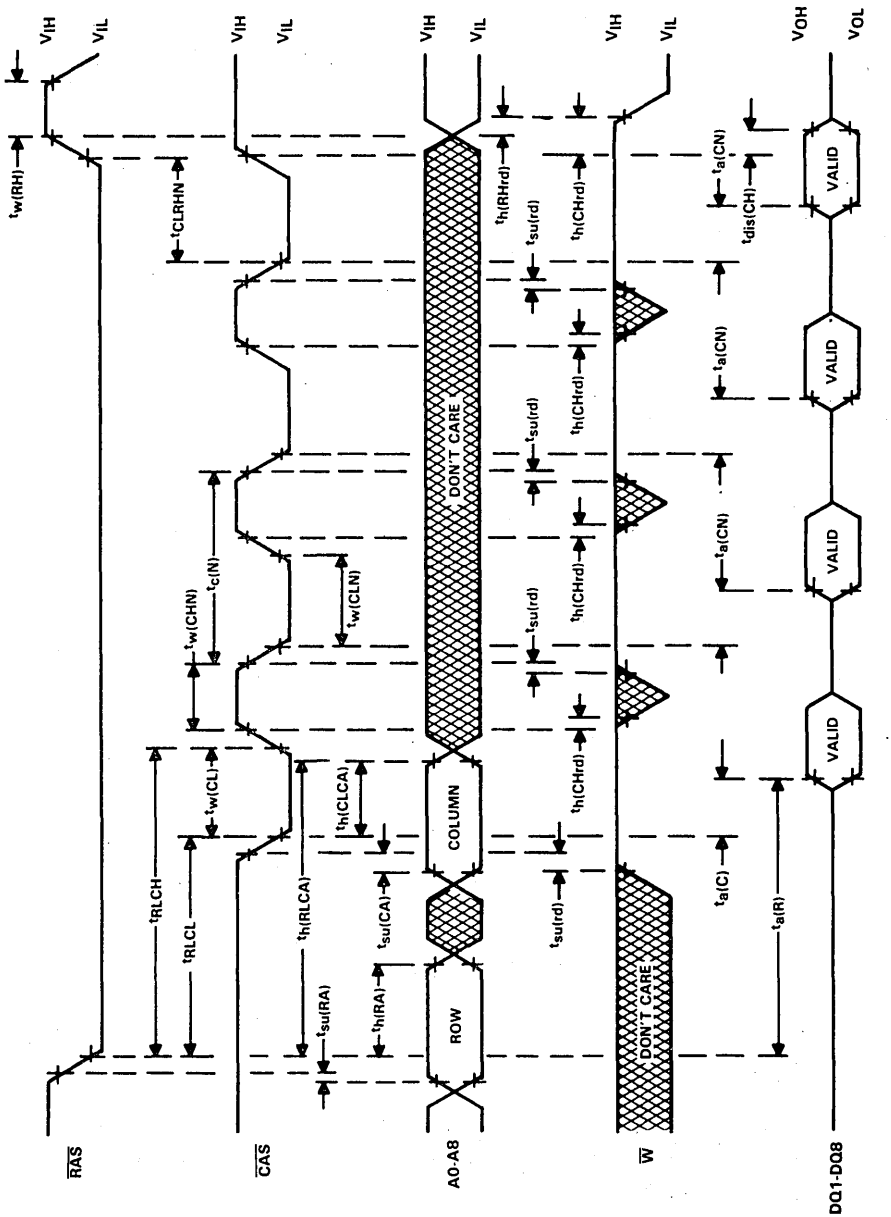
NOTE 4: A write cycle can be intermixed with read cycles as long as the write timing specifications are not violated.

page-mode write cycle timing



NOTE 5: A read cycle can be intermixed with write cycles as long as read timing specifications are not violated.

nibble-mode read cycle timing



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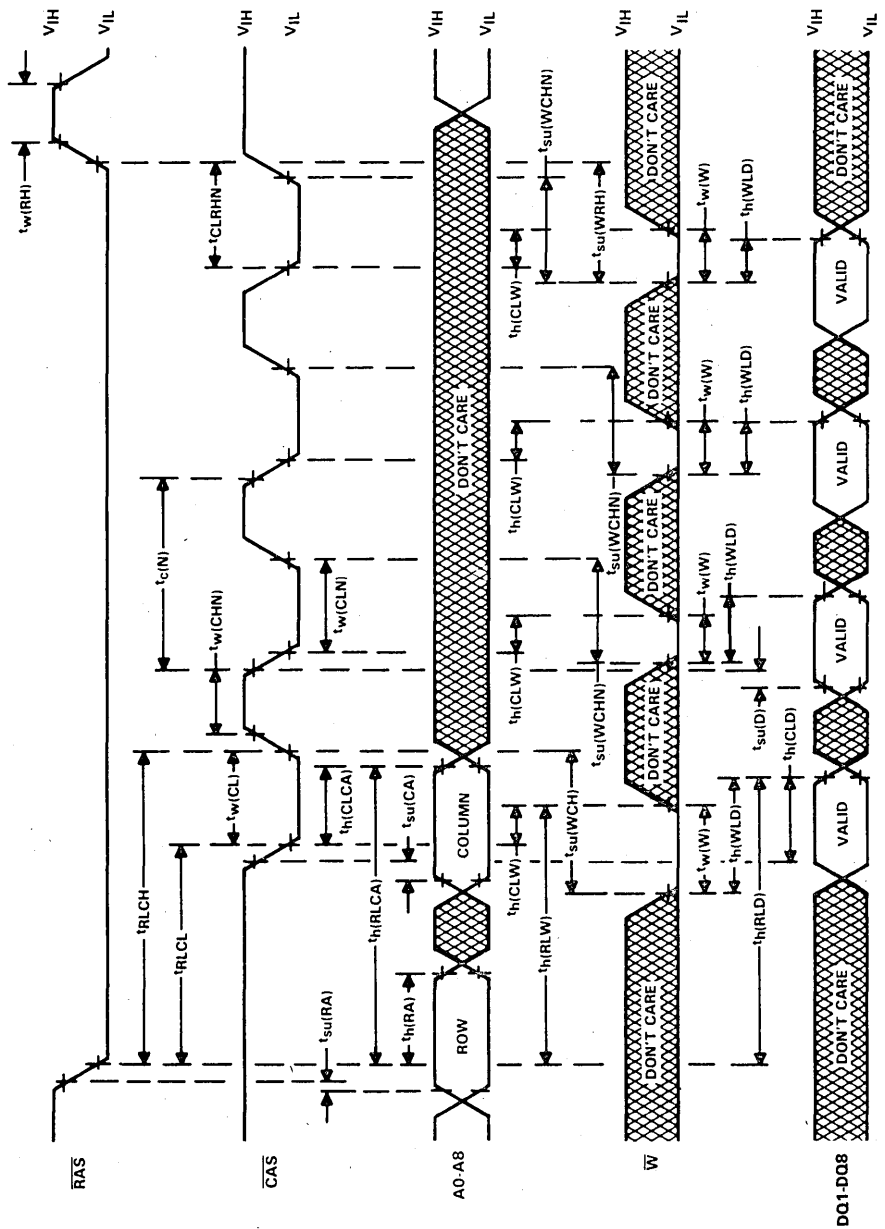
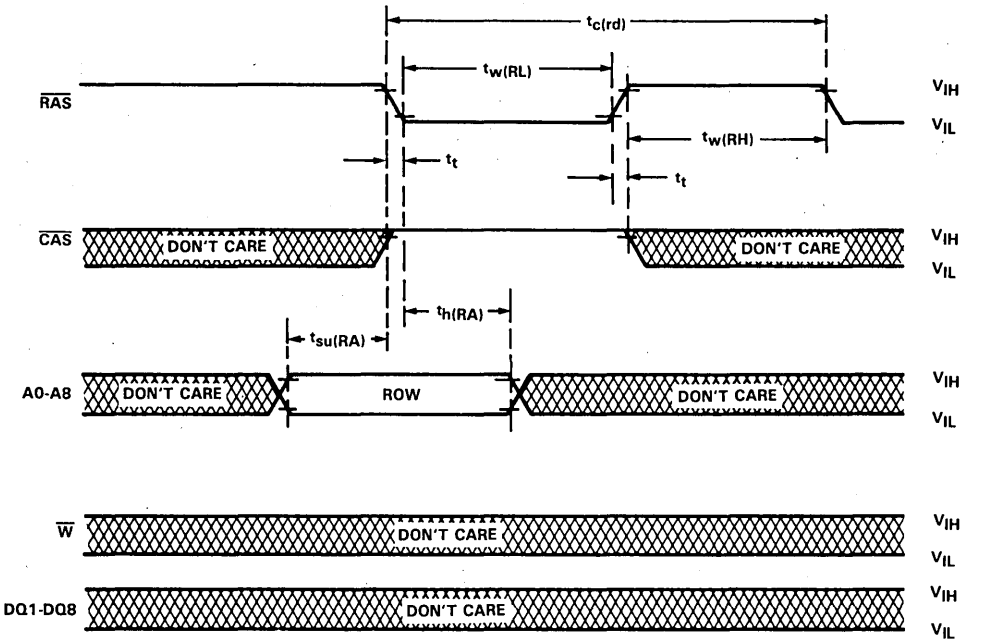
nibble-mode write cycle timing



$\overline{\text{RAS}}$-only refresh timing



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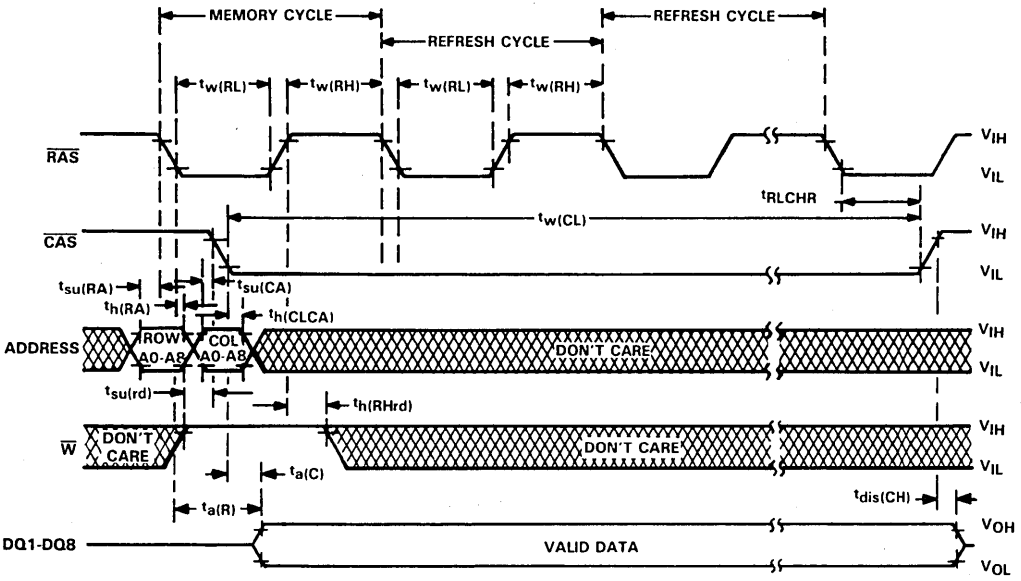
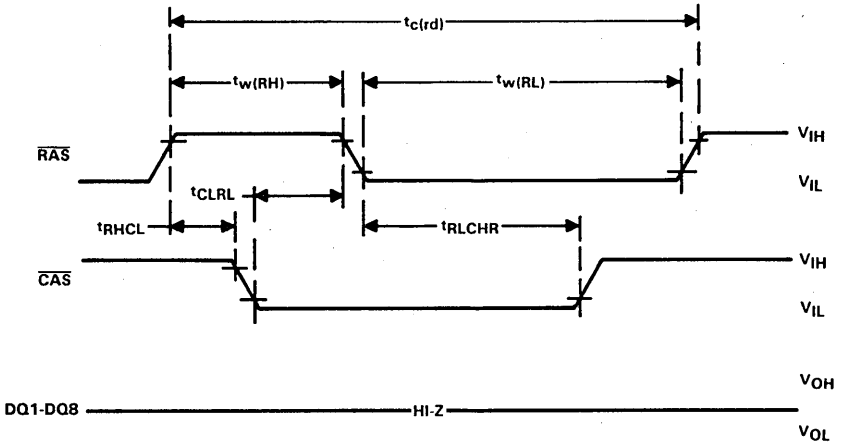
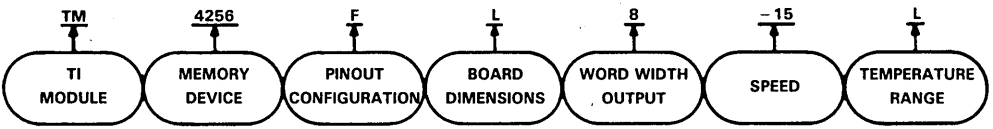
hidden refresh cycle timing



automatic (CAS-before-RAS) refresh cycle timing



TI single-in-line package nomenclature†



PINOUT CONFIGURATION	BOARD DIMENSIONS	SPEED	TEMPERATURE RANGE
F Version	L Package	Max Access	L 0°C to 70°C
Pin 24-No Connect	(76,2 x 16,5 mm)	–12 120 ns	
G Version	(3.0 x 0.65 inches)	–15 150 ns	
Pin 24-$\overline{PRD}$	U Package	–20 200 ns	
	(88,9 x 16,5 mm)		
	(3.5 x 0.65 inches)		

†The F pinout configuration designator is used when specifying the L package; the G pinout configuration version designator is used when specifying the U package.

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TM4256GP8, TM4256GV8
262,144 BY 8-BIT DYNAMIC RAM MODULES

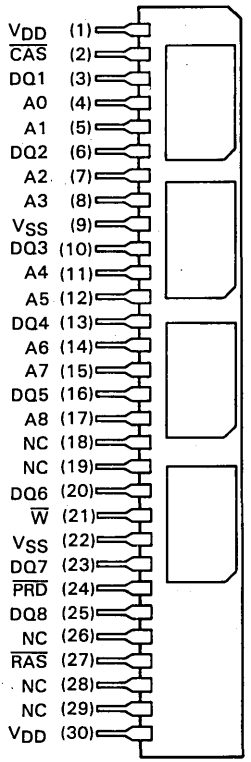
OCTOBER 1985 – REVISED NOVEMBER 1985

- 262,144 X 8 Organization
- Single 5-V Supply (10% Tolerance)
- 30-Pin Single-in-Line Package (SIP)
  - —Pinned Module for Through-Hole Insertion (TM4256GV8)
  - —Leadless Module for Use with Sockets (TM4256GP8)
- Low Profile, Double-Side Mount . . . 0.45" Height
- Utilizes Eight 256K Dynamic RAMs in Plastic Chip Carrier
- Long Refresh Period . . . 4 ms (256 Cycles)
- All inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Outputs
- Performance of Unmounted RAMs:

	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	READ-MODIFY-WRITE-CYCLE (MIN)
TMS4256-12	120 ns	60 ns	230 ns	270 ns
TMS4256-15	150 ns	75 ns	260 ns	305 ns
TMS4256-20	200 ns	100 ns	330 ns	370 ns

- Common $\overline{CAS}$ Control with Common Data-In and Data-Out Lines
- Low Power Dissipation
- Operating Free-Air Temperature . . . 0°C to 70°C
- Upward Compatible with Planned 1 Meg DRAM Family (Height and Length May Increase)

V SINGLE-IN-LINE PACKAGE†
(TOP VIEW)



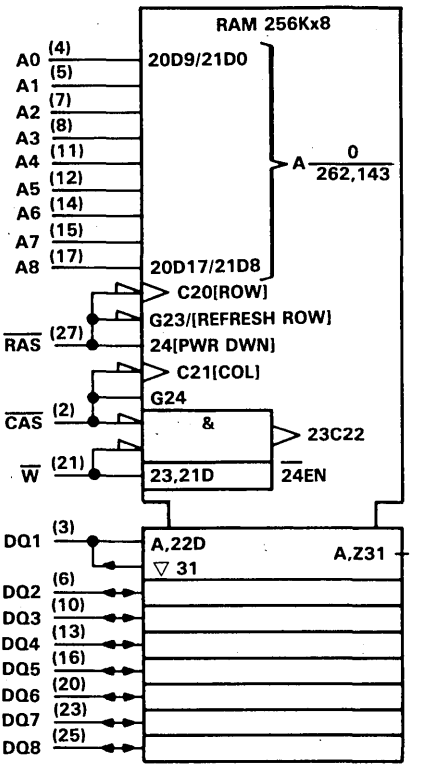
†TM4256GV8 package is shown.

PIN NOMENCLATURE	
A0-A8	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1-DQ8	Data In/Data Out
NC	No Connection
$\overline{PRD}$	Presence Detect
$\overline{RAS}$	Row-Address Strobe
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

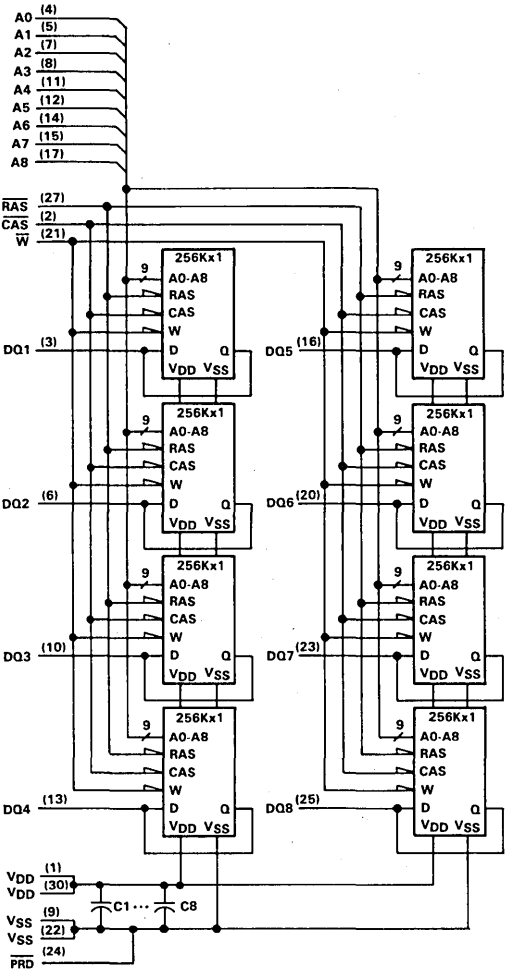
The TM4256G_8 series are 2048K, dynamic random-access memory modules organized as 262,144 × 8 bits in a 30-pin single-in-line package comprising eight TMS4256FML, 262,144 × 1 bit dynamic RAM's in 18-lead plastic chip carriers mounted on top of a substrate together with eight 0.2 μF decoupling capacitors. Each TMS4256FML is described in the data sheet and is fully electrically tested and processed according to TI's MIL-STD-883B (as amended for commercial applications) flows prior to assembly. After assembly onto the SIP, a further set of electrical tests is performed. The module is rated for operation from 0°C to 70°C.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

functional block diagram



operation

The TM4256G_8 operates as eight TMS4256s connected as shown in the functional block diagram. Refer to the TMS4256 data sheet for details of its operation. The common I/O feature of the TM4256G_8 requires the use of early-write cycles to prevent contention on D and Q.

presence detect

This feature allows for hardware presence detection of the memory module. The $\overline{PRD}$ pin for each module in the system should be pulled high through a pull-up resistor, resulting in a logic one when no module is present. When a module is present, $\overline{PRD}$ is a logic zero as this pin is connected to V_{SS} on the module. $\overline{PRD}$ can only be used to detect a modules' presence, not its functionality. In a system not requiring presence detect, it is recommended that this pin be left as a no connect; this allows the use of either type of module without adverse effects.

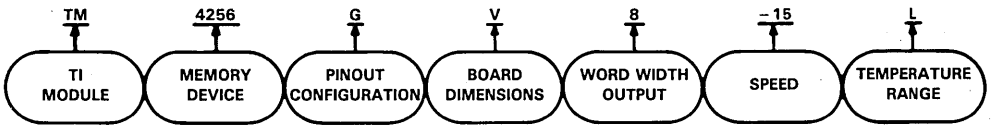
specifications

For TMS4256 electrical specifications, refer to the TMS4256 data sheet. The common I/O feature of the TM4256G_8 dictates the use of early-write cycles to prevent contention on D and Q.

single-in-line package and components

PC substrate: 0,79 mm (0.031 inch) minimum thickness
Bypass capacitors: Multilayer ceramic
Leads: Tin/lead solder coated over phosphor-bronze
Contact area for socketable devices: Nickel plate and solder plate on top of copper

TI single-in-line package nomenclature



V Package (78,7 x 11,4 mm) (3.1 x 0.45 inches) P Package (88,9 x 11,4 mm) (3.5 x 0.45 inches)	Max Access -12 120 ns -15 150 ns -20 200 ns	L 0°C to 70°C

TM4256GP9, TM4256GV9
262,144 BY 9-BIT DYNAMIC RAM MODULES

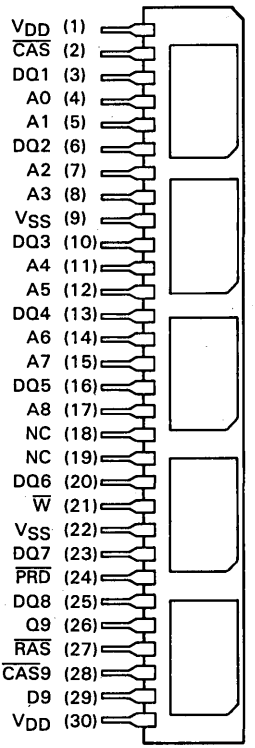
OCTOBER 1985 — REVISED NOVEMBER 1985

- 262,144 X 9 Organization
- Single 5-V Supply (10% Tolerance)
- 30-Pin Single-in-Line Package (SIP)
  - —Pinned Module for Through-Hole Insertion (TM4256GV9)
  - —Leadless Module for Use with Sockets (TM4256GP9)
- Low Profile, Double-Side Mount . . . 0.45" Height
- Utilizes Nine 256K Dynamic RAMs in Plastic Chip Carrier
- Long Refresh Period . . . 4 ms (256 Cycles)
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Outputs
- Performance of Unmounted RAMs:

	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	READ-MODIFY-WRITE CYCLE (MIN)
TMS4256-12	120 ns	60 ns	230 ns	270 ns
TMS4256-15	150 ns	75 ns	260 ns	305 ns
TMS4256-20	200 ns	100 ns	330 ns	370 ns

- Common $\overline{CAS}$ Control for Eight Common Data-In and Data-Out Lines
- Separate $\overline{CAS}$ Control for One Separate Pair of Data-In and Data-Out Lines
- Low Power Dissipation
- Operating Free-Air Temperature . . . 0°C to 70°C
- Upward Compatible with Planned 1 Meg DRAM Family (Height and Length May Increase)

V SINGLE-IN-LINE PACKAGE†
(TOP VIEW)



†TM4256GV9 package is shown.

PIN NOMENCLATURE	
A0-A8	Address Inputs
$\overline{CAS}$, $\overline{CAS9}$	Column-Address Strobes
DQ1-DQ8	Data In/Data Out
D9	Data In
NC	No Connection
$\overline{PRD}$	Presence Detect
Q9	Data Out
$\overline{RAS}$	Row-Address Strobe
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The TM4256G_9 series is a 2304K, dynamic random-access memory module organized as 262,144 × 9 bits [bit nine (D9, Q9) is generally used for parity and is controlled by $\overline{CAS9}$] in a 30-pin single-in-line package comprising nine TMS4256FML, 262,144 × 1 bit dynamic RAM's in 18-lead plastic chip carriers mounted on top of a substrate together with nine 0.2 μF decoupling capacitors mounted beneath the chip carriers. Each TMS4256FML is described in the data sheet and is fully electrically tested and processed according to TI's MIL-STD-883B (as amended for commercial

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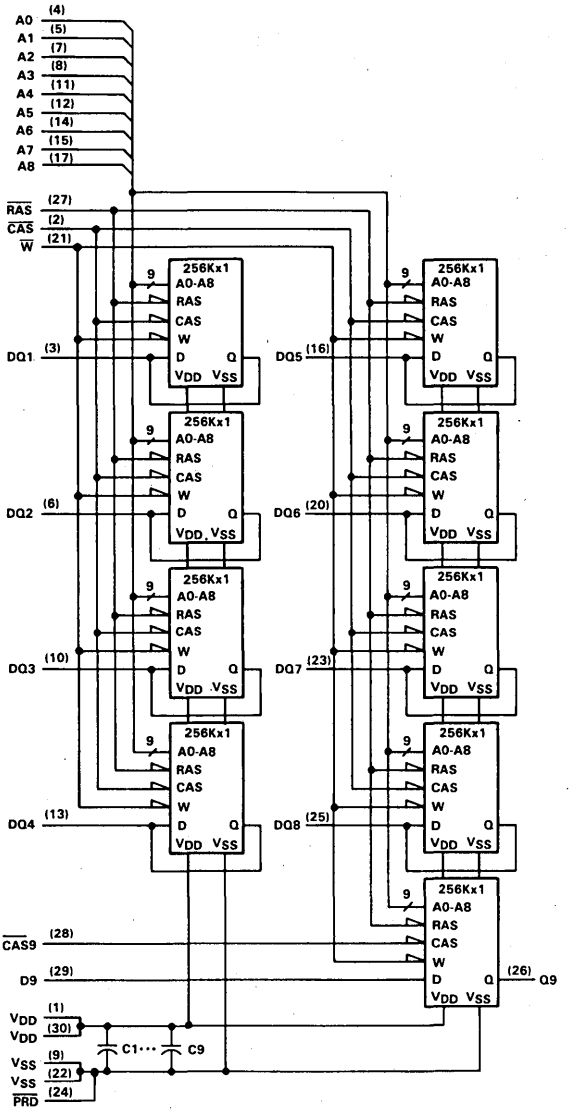
applications) flows prior to assembly. After assembly onto the SIP, a further set of electrical tests is performed. The module is rated for operation from 0°C to 70°C.

functional block diagram



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operation

The TM4256G_9 operates as nine TMS4256s connected as shown in the functional block diagram. Refer to the TMS4256 data sheet for details of its operation. The common I/O feature of the TM4256G_9 dictates the use of early-write cycles to prevent contention on D and Q.

specifications

For TMS4256 electrical specifications, refer to the TMS4256 data sheet. The common I/O feature of the TM4256G_9 dictates the use of early-write cycles to prevent contention on D and Q.

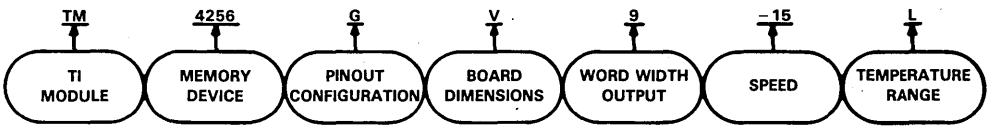
presence detect

This feature allows for hardware presence detection of the memory module. The $\overline{PRD}$ pin for each module in the system should be pulled high through a pull-up resistor, resulting in a logic one when no module is present. When a module is present, $\overline{PRD}$ is a logic zero as this pin is connected to V_{SS} on the module. $\overline{PRD}$ can only be used to detect a modules' presence, not its functionality. In a system not requiring presence detect, it is recommended that this pin be left as a no connect; this allows the use of either type of module without adverse effects.

single-in-line package and components

PC substrate: 0,79 mm (0.031 inch) minimum thickness
Bypass capacitors: Multilayer ceramic
Leads: Tin/lead solder coated over phosphor-bronze
Contact area for socketable devices: Nickel plate and solder plate on top of copper

TI single-in-line package nomenclature



V Package (78,7 x 11,43 mm) (3.1 x 0.45 inches) P Package (88,9 x 16,5 mm) (3.5 x 0.65 inches)	Max Access –12 120 ns –15 150 ns –20 200 ns	L 0°C to 70°C

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TM4256HE4
524,288 BY 4-BIT DYNAMIC RAM MODULE

SEPTEMBER 1985 — REVISED NOVEMBER 1985

- 524,288 X 4 Organization
- Single 5-V Supply (10% Tolerance)
- 24-Pin Single-in-Line Package (SIP)
- Utilizes Eight 256K Dynamic RAMs in Plastic Chip Carrier
- Long Refresh Period . . . 4 ms (256 Cycles)
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Outputs
- Performance of Unmounted RAMs:

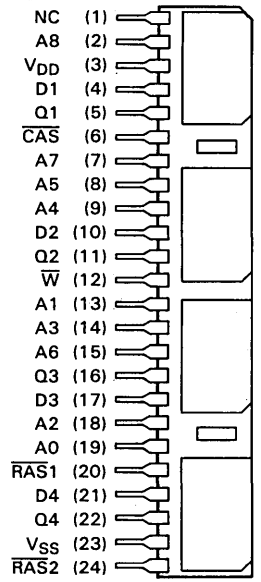
	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	READ-MODIFY-WRITE CYCLE (MIN)
TMS4256-12	120 ns	60 ns	230 ns	270 ns
TMS4256-15	150 ns	75 ns	260 ns	305 ns
TMS4256-20	200 ns	100 ns	330 ns	370 ns

- Common $\overline{CAS}$ Control with Separate Data-In and Data-Out Lines
- Low Power Dissipation:

	OPERATING (TYP)	STANDBY (TYP)
TM4256HE4-12	2600 mW	100 mW
TM4256HE4-15	2400 mW	100 mW
TM4256HE4-20	1800 mW	100 mW

- Operating Free-Air Temperature . . . 0°C to 70°C

E SINGLE-IN-LINE PACKAGE†
(TOP VIEW)



†$\overline{RAS}1$ is the row-address strobe for side 1, and $\overline{RAS}2$ is the row-address strobe for side 2. Side 1 is shown in top view.

PIN NOMENCLATURE	
A0-A8	Address Inputs
$\overline{CAS}$	Column-Address Strobe
D1-D4	Data Inputs
NC	No Connection
Q1-Q4	Data Outputs
$\overline{RAS}1$, $\overline{RAS}2$	Row-Address Strobes
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The TM4256HE4 is a 2048K, dynamic random-access memory module organized as 524,288 X 4 bits in a 24-pin single-in-line package (SIP) comprising eight TMS4256FML, 262,144 X 1 bit dynamic RAM's in 18-lead plastic-chip carriers mounted on both sides of a substrate together with four 0.2 μF decoupling capacitors. The on-board capacitors eliminate the need for bypassing on the motherboard and offer superior performance over equivalent leaded capacitors due to reduced lead inductance. Also, with 0.475 inch board spacing, the TM4256HE4 has a density of seven devices per square inch (approximately 2.8X the density of DIPs). With the elimination of bypass capacitors on the motherboard, reduced PC board size, and fewer plated-through holes, a cost savings can be realized.

The TM4256HE4 is organized as two banks of 256K X 4 selected by $\overline{RAS}1$, $\overline{RAS}2$; $\overline{CAS}$ and $\overline{W}$ which are common to all devices. The D and Q signals are common to pairs of devices on opposing sides of the substrate. This configuration requires that only one $\overline{RAS}$ signal be active during a read or write cycle to prevent data bus contention or writing erroneous data. On refresh cycles ($\overline{CAS}$ high), $\overline{RAS}1$ and $\overline{RAS}2$ can be low at the same time.

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Each TMS4256FML is described in the TMS4256 data sheet and is fully electrically tested and processed according to TI's MIL-STD-883B (as amended for commercial applications) flows prior to assembly. After assembly onto the substrate, a further set of electrical tests is performed.

operation

The TM4256HE4 operates as eight TMS4256s connected as shown in the functional block diagram. Refer to the TMS4256 data sheet for details of its operation.

specifications

For TMS4256 electrical specifications, refer to the TMS4256 data sheet.

single-in-line package and components

PC substrate: 1,14 mm (0.045 inch) minimum thickness
Bypass capacitors: Multilayer ceramic
Leads: Tin/lead solder coated over phosphor-bronze

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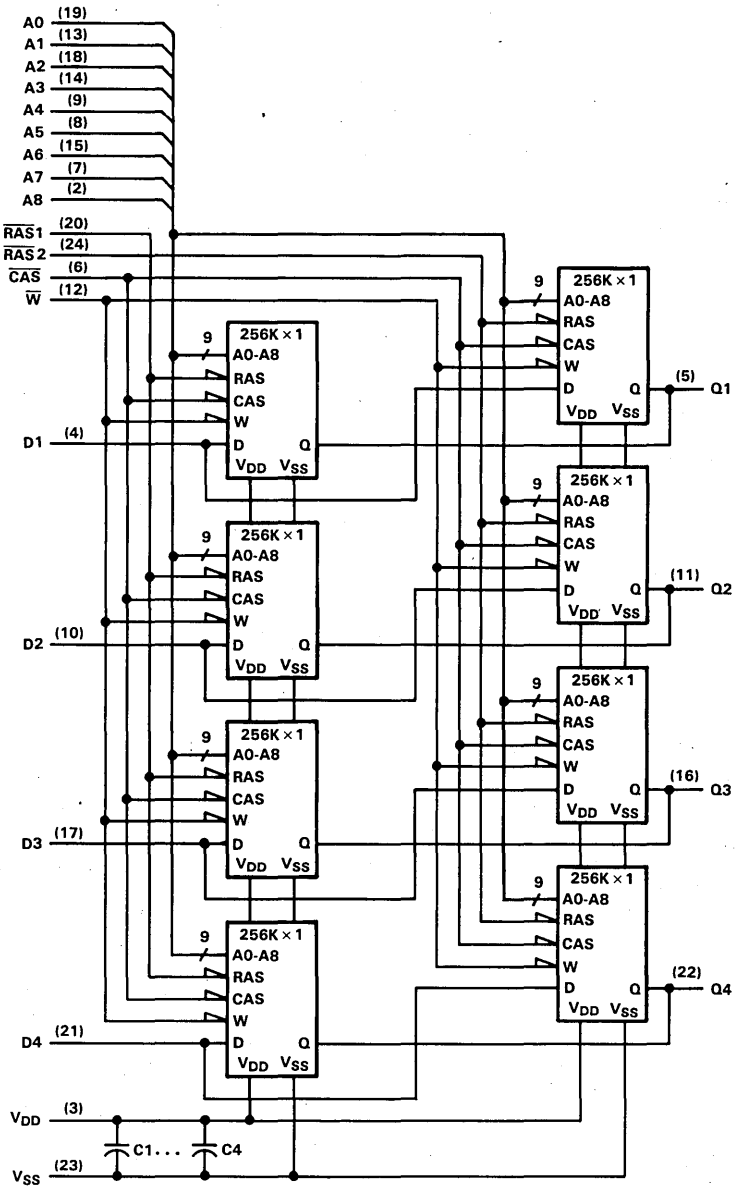
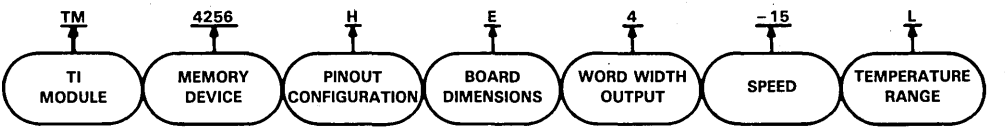
functional block diagram



TI single-in-line package nomenclature



(61 x 11,4 mm)
(2.4 x 0.45 inches)

Max Access
-12 120 ns
-15 150 ns
-20 200 ns

L 0°C to 70°C

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TM4416KU8
16,384 BY 8-BIT DYNAMIC RAM MODULE

SEPTEMBER 1985 – REVISED NOVEMBER 1985

- 16,384 X 8 Organization
- Single 5-V Supply (10% Tolerance)
- 30-Pin Single-in-Line Package (SIP)
- Utilizes Two 16K X 4 Dynamic RAMs in Plastic Chip Carrier
- Long Refresh Period . . . 4 ms (256 Cycles)
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Outputs
- Performance Ranges:

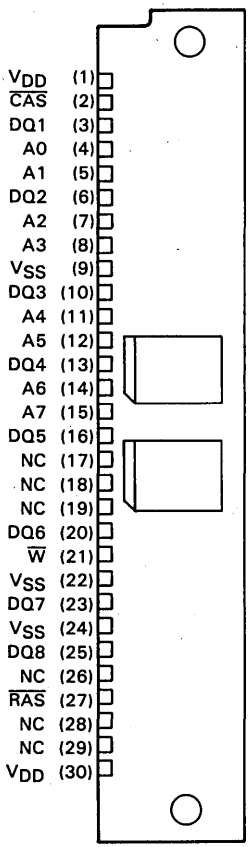
	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)
TM4416KU8-12	120 ns	70 ns	230 ns
TM4416KU8-15	150 ns	80 ns	260 ns

- Low Power Dissipation:

	OPERATING (TYP)	STANDBY (TYP)
TM4416KU8-12	400 mW	30 mW
TM4416KU8-15	350 mW	30 mW

- Operating Free-Air Temperature . . . 0°C to 70°C

U SINGLE-IN-LINE PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A7	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1-DQ8	Data In/Data Out
NC	No Connection
$\overline{RAS}$	Row-Address Strobe
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The TM4416KU8 is a 128K, dynamic random-access memory module organized as 16,384 × 8 bits in a 30-pin single-in-line package comprising two TMS4416FPL, 16,384 x 4 bit dynamic RAM's in 18-lead plastic chip carriers mounted on top of a substrate together with two 0.2 μF decoupling capacitors mounted beneath the chip carriers. The onboard capacitors eliminate the need for bypassing on the motherboard and offer superior performance over equivalent leaded capacitors due to reduced lead inductance.

operation

address (A0 through A7)

Fourteen address bits are required to decode 1 of 16,384 storage locations. Eight row-address bits are set up on pins A0 through A7 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the six column-address bits are set up on pins A1 through A6 and latched onto the

chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data inputs are disabled when the read mode is selected. The grounded output-enable ($\overline{G}$) dictates the use of early write cycles to prevent contention on DQ. When $\overline{W}$ goes low prior to $\overline{CAS}$, the data outputs will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data in (DQ1-DQ8)

Data is written during a write cycle. The falling edge of $\overline{CAS}$ strobes data into the on-chip data latches. These latches can be driven from standard TTL circuits without a pull-up resistor. In the early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal.

data out (DQ1-DQ8)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan out of two Series 74 TTL loads for each output. Data out is the same polarity as data in. In a read cycle the outputs go active after the access time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ is satisfied. The outputs become valid after the access time has elapsed and remain valid while $\overline{CAS}$ is low; $\overline{CAS}$ going high returns it to a high-impedance state. In the early write cycle, the outputs are always in the high-impedance state. In the early write cycle, the outputs are always in the high-impedance state, a necessity due to the grounded output enable.

refresh

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffers are in the high-impedance state unless $\overline{CAS}$ is applied, the $\overline{RAS}$-only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses (A0 through A7) with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power.

page mode

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the chip. Thus, the time required to setup and strobe sequential row addresses for the same page is eliminated. To extend beyond the 64 column locations on a single module, the row address and $\overline{RAS}$ are applied to multiple modules. $\overline{CAS}$ is then decoded to select the proper module.

power up

After power up, the power supply must remain at its steady-state value for 1 ms. In addition, the $\overline{RAS}$ input must remain high for 100 μs immediately prior to initialization. Initialization consists of performing eight $\overline{RAS}$ cycles before proper device operation is achieved.

single-in-line package and components

PC substrate: 0,79 mm (0.031 inch) minimum thickness
Bypass capacitor: Multilayer ceramic
Contact area for socketable devices: Nickel plate and solder plate on top of copper

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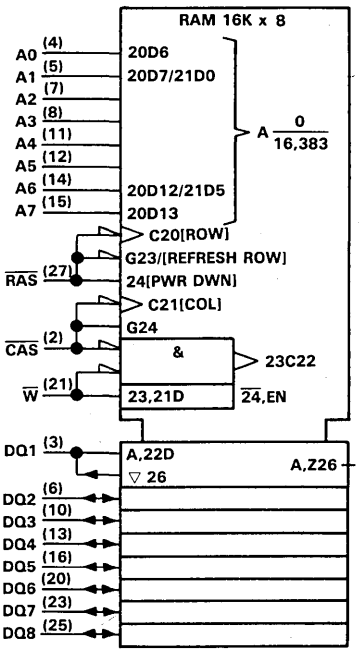
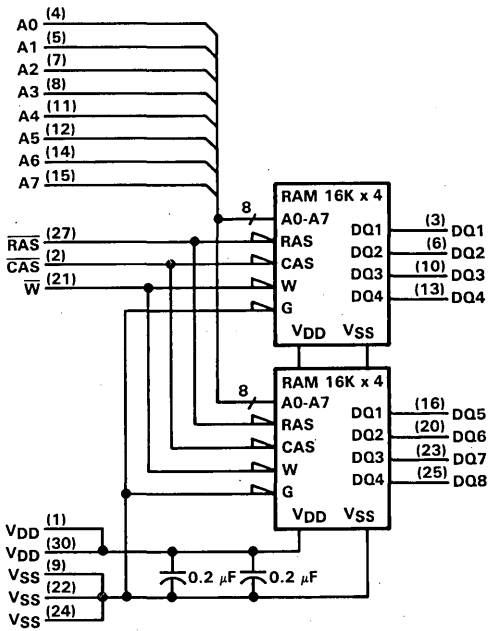
logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range for any pin except V_{DD} and data out (see Note 1) . . . . . −1.5 V to 10 V
Voltage range for V_{DD} supply and data out with respect to V_{SS} . . . . . −1 V to 6 V
Short circuit output current . . . . . 50 mA
Power dissipation . . . . . 2 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values in this data sheet are with respect to V_{SS}.
2. Additional information concerning the handling of ESD sensitive devices is available in a document entitled "Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies" in Section 12.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		4.5	5	5.5	V
V_{SS}	Supply voltage			0		V
V_{IH}	High-level input voltage	V_{DD} = 4.5 V	2.4		4.8	V
		V_{DD} = 5.5 V	2.4		5.8	
V_{IL}	Low-level input voltage (see Notes 3 and 4)		−0.6	0	0.8	V
T_A	Operating free-air temperature		0		70	°C

NOTES: 3. The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

4. Due to input protection circuitry, the applied voltage may begin to clamp at −0.6 V. Test conditions must comprehend this occurrence. See Application Report entitled "TMS4164A and TMS4416 Input Diode Protection" on page 9-5.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TM4416KU8-12			TM4416KU8-15			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −2 mA	2.4			2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 5.8 V, V_{DD} = 5 V, All other pins = 0 V			±10			±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10			±10	μA
I_{DD1}	Average operating current during read or write cycle	t_c = minimum cycle, All outputs open			108			96	mA
I_{DD2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, All outputs open			10			10	mA
I_{DD3}	Average refresh current	t_c = minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high, All outputs open			92			80	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling, All outputs open			92			80	mA

†All typical values are at T_A = 25°C and nominal supply voltages.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

PARAMETER		MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs	14	pF
$C_{i(RC)}$	Input capacitance, strobe inputs	20	pF
$C_{i(W)}$	Input capacitance, write-enable input	20	pF
$C_{i/o}$	Input/output capacitance, data ports	10	pF

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switching characteristics over recommended supply voltage range and operating free-air temperature range

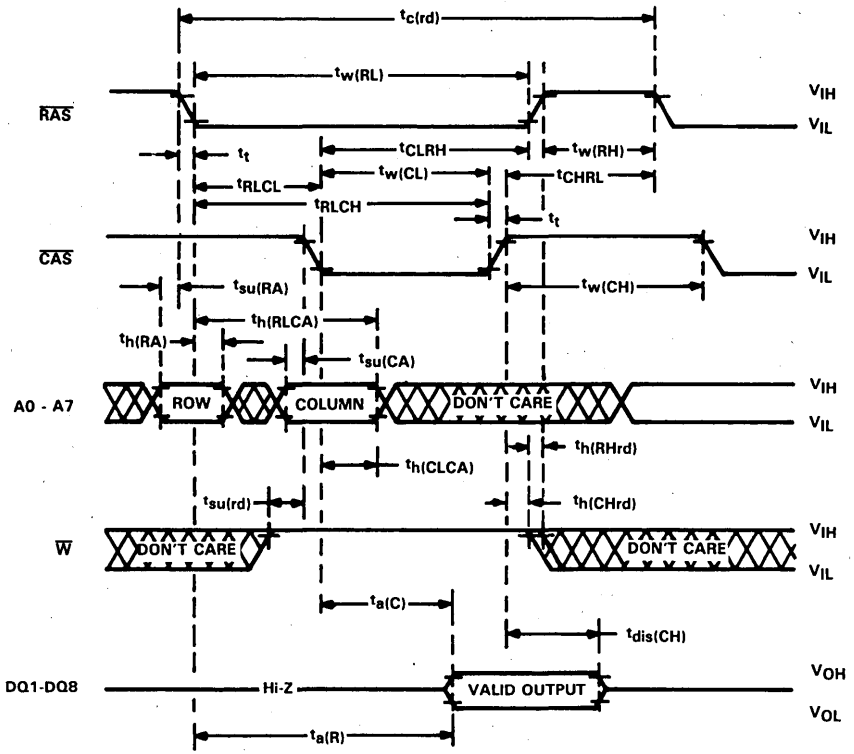
PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TM4416KU8-12		TM4416KU8-15		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		70		80	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{RAC}		120		150	ns

timing requirements over recommended supply voltage range and operating free-air temperature range

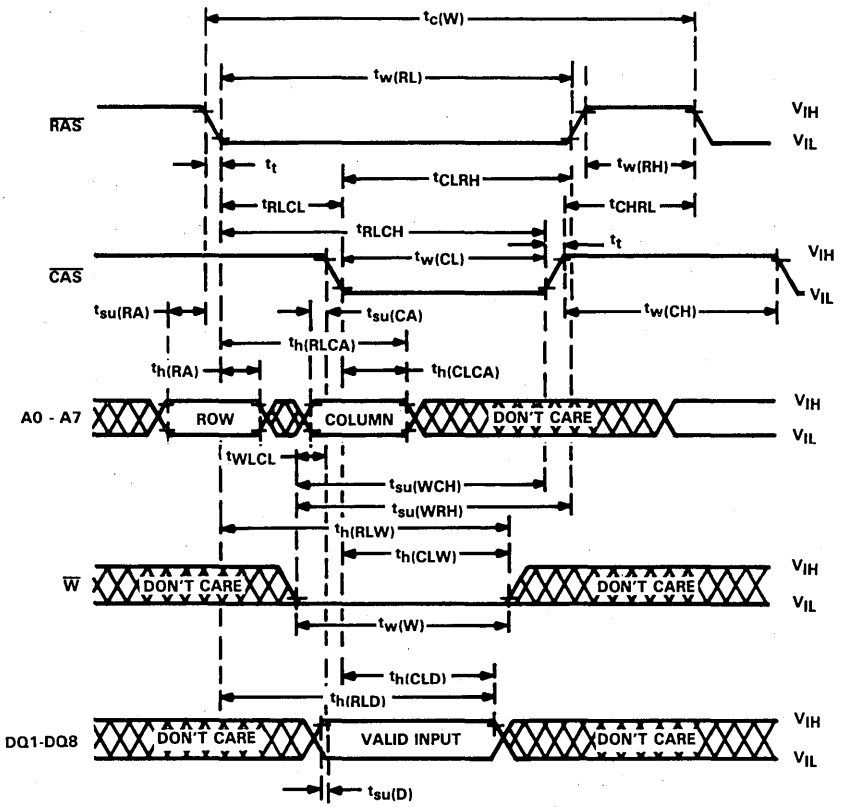
		ALT. SYMBOL	TM4416KU8-12		TM4416KU8-15		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(P)}$	Page-mode cycle time	t_{PC}	120		140		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	230		260		ns
$t_{c(W)}$	Write cycle time	t_{WC}	230		260		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	315		365		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (precharge time)‡	t_{CP}	40		50		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low	t_{CAS}	70	10,000	80	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge time)	t_{RP}	80		100		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low	t_{RAS}	120	10,000	150	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	30		40		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	50	3	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	5		5		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	50		60		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	50		60		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	35		40		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	20		30		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	85		110		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	40		60		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	90		130		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	10		10		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	40		60		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	90		130		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	120		150		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	70		80		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	25	50	25	70	ns
t_{WLCL}	Delay time, $\overline{W}$ low to $\overline{CAS}$ low (early write cycle)	t_{WCS}	−5		−5		ns
t_{rf}	Refresh time interval	t_{REF}		4		4	ms

†All cycle times assume t_t = 5 ns.
‡Page mode only.

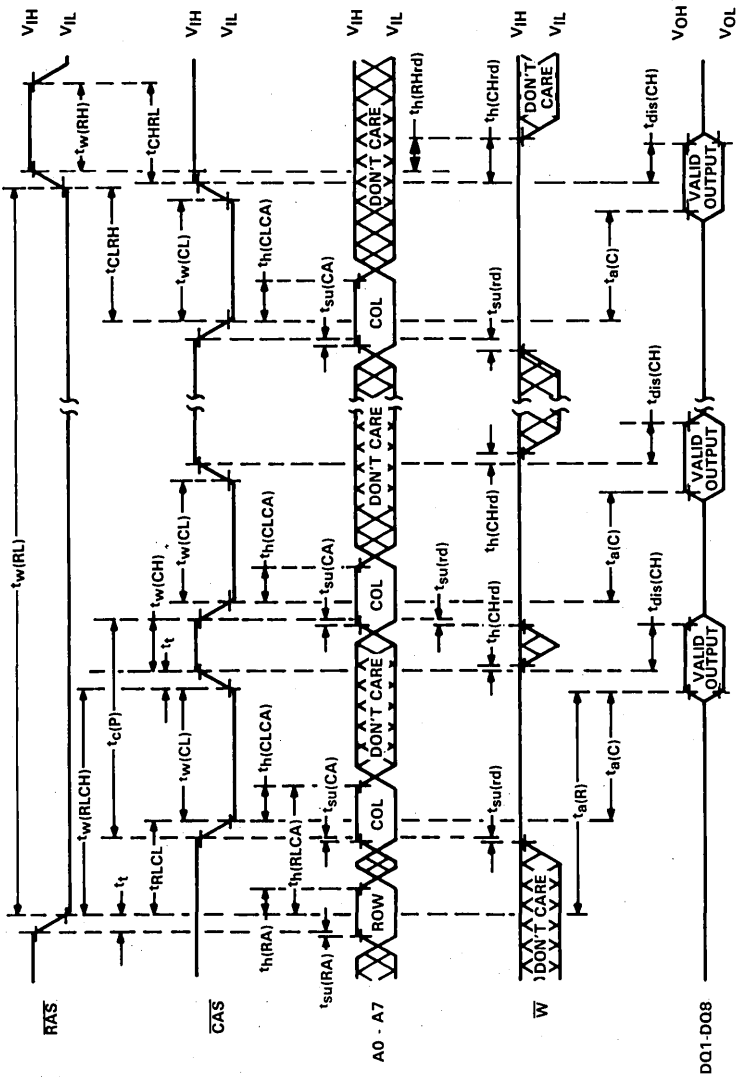
read cycle timing



early write cycle timing

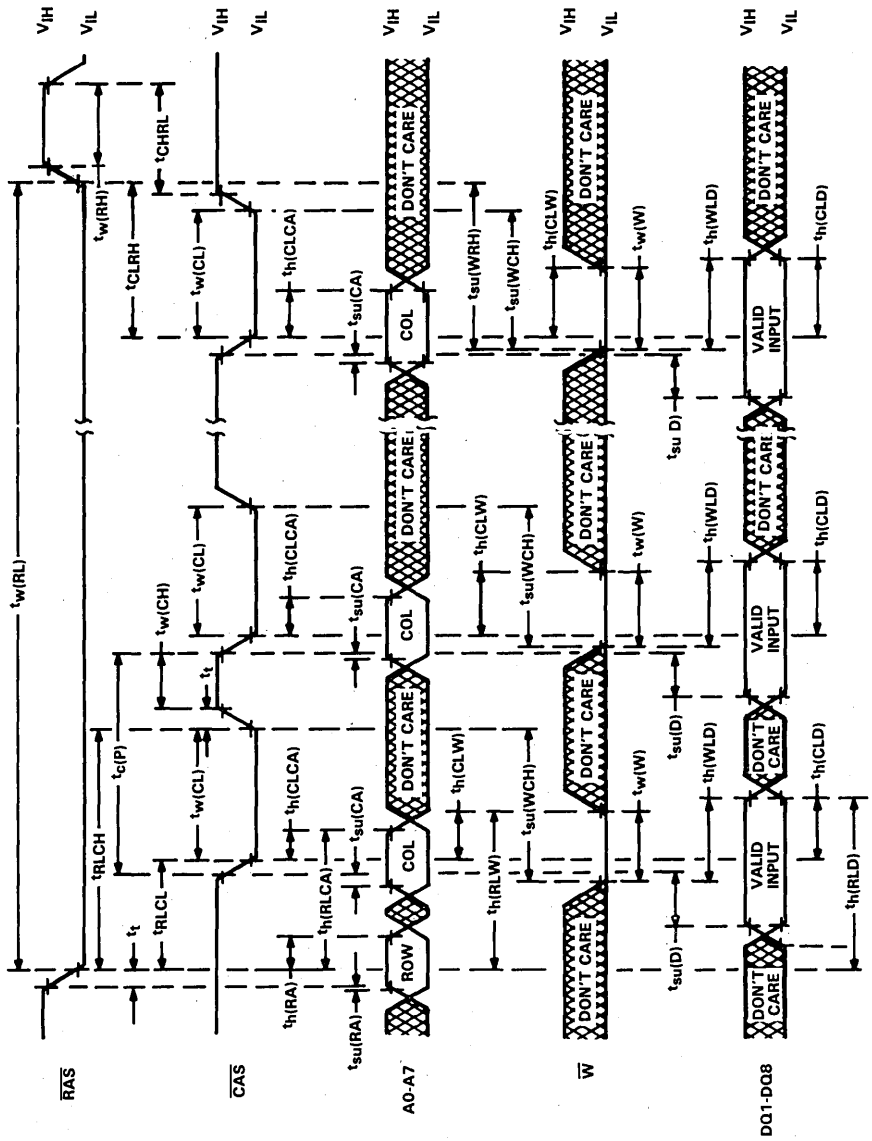


page-mode read cycle timing



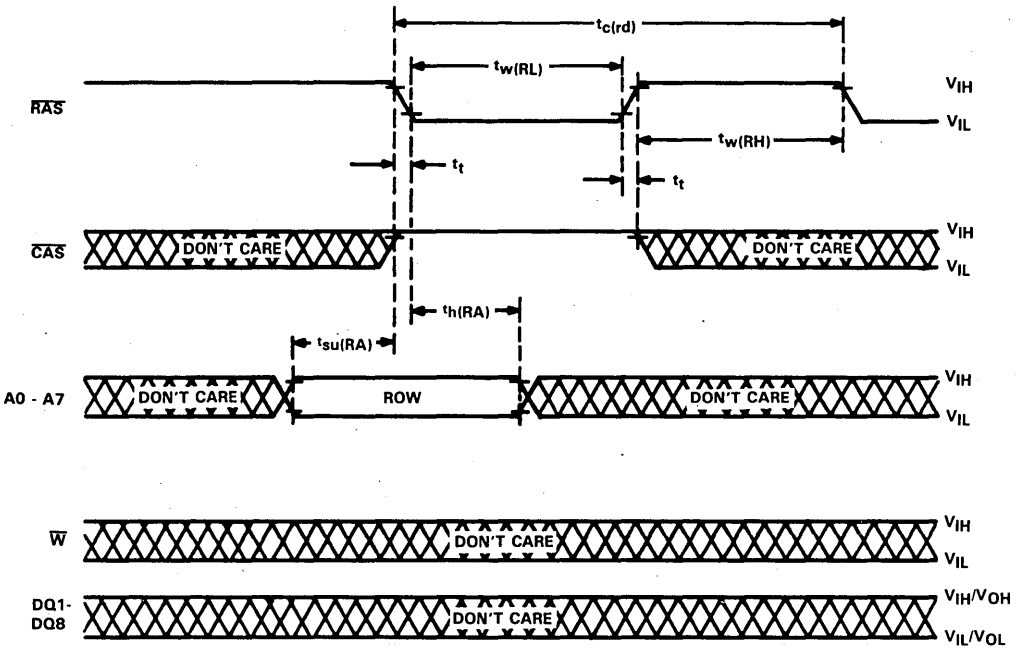
NOTE 5: A write cycle or a read-modify-write cycle can be intermixed with read cycles as long as the write and read-modify-write timing specifications are not violated.

page-mode write cycle timing

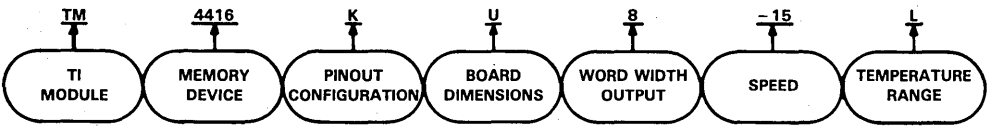


NOTE 6: A read or a read-modify-write cycle can be intermixed with write cycles as long as read and read-modify-write timing specifications are not violated.

$\overline{\text{RAS}}$-only refresh timing



TI single-in-line package nomenclature



(88,9 x 16,5 mm)
(3.5 x 0.65 inches)

Max Access
-12 120 ns
-15 150 ns

L 0°C fo 70°C

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TM4464LU8
65,536 BY 8-BIT DYNAMIC RAM MODULE

OCTOBER 9185 – REVISED NOVEMBER 1985

- 65,536 X 8 Organization
- Single 5-V Supply (10% Tolerance)
- 30-Pin Single-in-Line Package (SIP)
- Utilizes Two 64K X 4 Dynamic RAMs in Plastic Chip Carrier
- Long Refresh Period . . . 4 ms (256 Cycles)
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Outputs
- Performance Ranges:

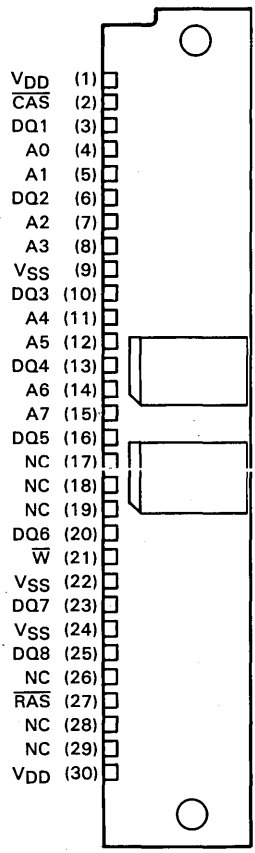
	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)
TM4464LU8-12	120 ns	60 ns	230 ns
TM4464LU8-15	150 ns	75 ns	260 ns

- Low Power Dissipation:

	OPERATING (TYP)	STANDBY (TYP)
TM4464LU8-12	650 mW	25 mW
TM4464LU8-15	550 mW	25 mW

- Operating Free-Air Temperature . . . 0°C to 70°C

U SINGLE-IN-LINE PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A7	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1-DQ8	Data In/Data Out
NC	No Connection
$\overline{RAS}$	Row-Address Strobe
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The TM4464LU8 is a 512K, dynamic random-access memory module organized as 65,536 × 8 bits in a 30-pin single-in-line package comprising two TMS4464FML, 65,536 × 4 bit dynamic RAM's in 22-lead plastic chip carriers mounted on top of a substrate together with two 0.2 μF decoupling capacitors mounted beneath the chip carriers. The onboard capacitors eliminate the need for bypassing on the motherboard and offer superior performance over equivalent leaded capacitors due to reduced lead inductance.

operation

address (A0 through A7)

Fourteen address bits are required to decode 1 of 65,536 storage locations. Eight row-address bits are set up on pins A0 through A7 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the six column-address bits are set up on pins A1 through A6 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

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write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data inputs are disabled when the read mode is selected. The common I/O feature of the TM4464LU8 dictates the use of early write cycles to prevent contention on DQ. When $\overline{W}$ goes low prior to $\overline{CAS}$, the data outputs will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data in (DQ1-DQ8)

Data is written during a write cycle. The falling edge of $\overline{CAS}$ strobes data into the on-chip data latches. These latches can be driven from standard TTL circuits without a pull-up resistor. In the early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal.

data out (DQ1-DQ8)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan out of two Series 74 TTL loads for each output. Data out is the same polarity as data in. In a read cycle the outputs go active after the access time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ is satisfied. The outputs become valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low; $\overline{CAS}$ going high returns it to a high-impedance state. In the early write cycle, the outputs are always in the high-impedance state, a necessity due to the grounded output enable.

refresh

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffers are in the high-impedance state unless $\overline{CAS}$ is applied, the $\overline{RAS}$-only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses (A0 through A7) with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power.

page mode

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the chip. Thus, the time required to setup and strobe sequential row addresses for the same page is eliminated. To extend beyond the 64 column locations on a single module, the row address and $\overline{RAS}$ are applied to multiple modules. $\overline{CAS}$ is then decoded to select the proper module.

power up

After power up, the power supply must remain at its steady-state value for 1 ms. In addition, the $\overline{RAS}$ input must remain high for 100 μs immediately prior to initialization. Initialization consists of performing eight $\overline{RAS}$ cycles before proper device operation is achieved.

single-in-line package and components

PC substrate: 0,79 mm (0.031 inch) minimum thickness
Bypass capacitors: Multilayer ceramic
Contact area for socketable devices: Nickel plate and solder plate on top of copper

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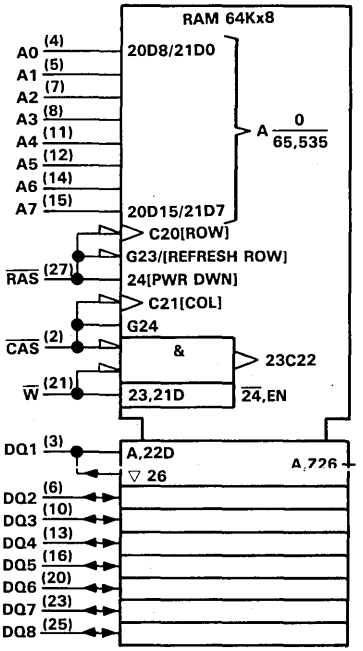
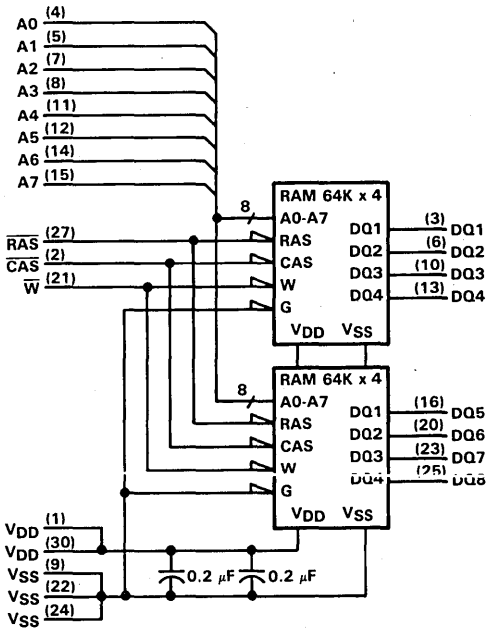
logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range for any pin except V_{DD} and data out (see Note 1) . . . . . −1.5 V to 10 V
Voltage range for V_{DD} supply and data out with respect to V_{SS} . . . . . −1 V to 6 V
Short circuit output current . . . . . 50 mA
Power dissipation . . . . . 2 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values in this data sheet are with respect to V_{SS}.
2. Additional information concerning the handling of ESD sensitive devices is available in a document entitled "Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies" in Section 12.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		4.5	5	5.5	V
V_{SS}	Supply voltage			0		V
V_{IH}	High-level input voltage	V_{DD} = 4.5 V	2.4		4.8	V
		V_{DD} = 5.5 V	2.4		5.8	
V_{IL}	Low-level input voltage (see Note 3)		−1	0	0.8	V
T_A	Operating free-air temperature		0		70	°C

NOTE 3: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TM4464LU8-12			TM4464LU8-15			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −2 mA	2.4			2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 5.8 V, V_{DD} = 5 V, All other pins = 0 V			±10			±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10			±10	μA
I_{DD1}	Average operating current during read or write cycle	t_c = minimum cycle, All outputs open		130	160		110	140	mA
I_{DD2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, All outputs open		5	10		5	10	mA
I_{DD3}	Average refresh current	t_c = minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high, All outputs open		100	120		90	110	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling, All outputs open		90	110		80	100	mA

†All typical values are at T_A = 25°C and nominal supply voltages.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		14	pF
$C_{i(RC)}$	Input capacitance, strobe inputs		20	pF
$C_{i(W)}$	Input capacitance, write-enable input		20	pF
$C_{i/o}$	Input/output capacitance, data ports		10	pF
$C_{o(VDD)}$	Decoupling capacitance	0.4		μF

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switching characteristics over recommended supply voltage range and operating free-air temperature range

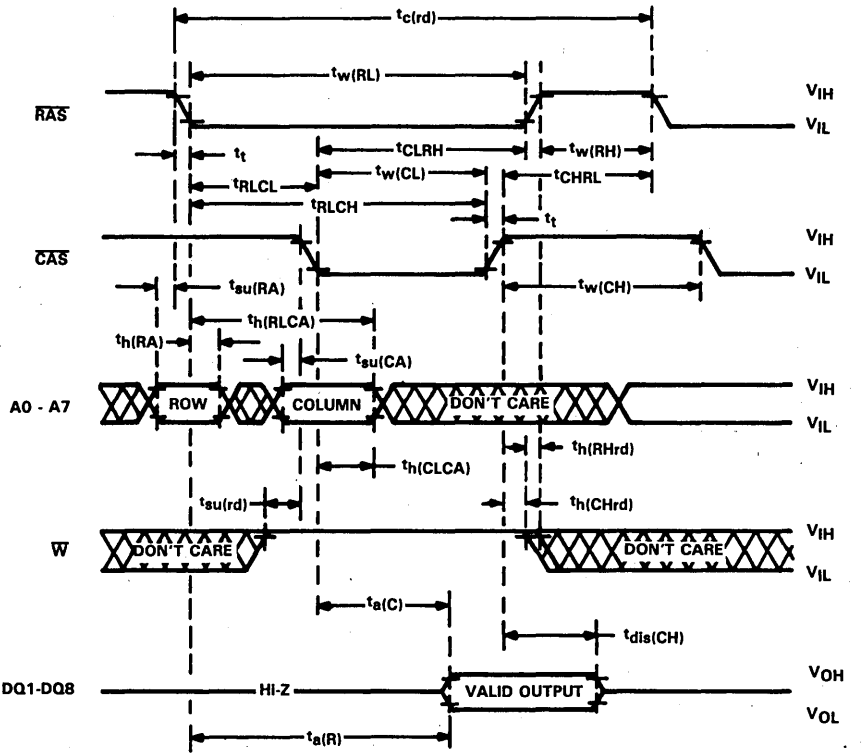
PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TM4464LU8-12		TM4464LU8-15		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		70		80	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{RAC}		120		150	ns

timing requirements over recommended supply voltage range and operating free-air temperature range

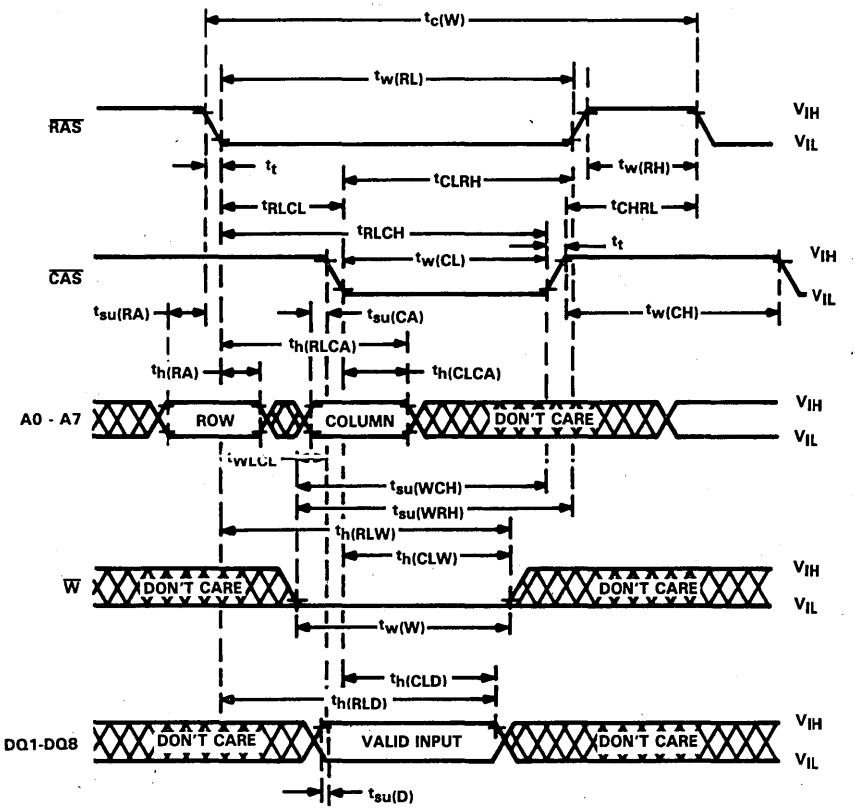
		ALT. SYMBOL	TM4464LU8-12		TM4464LU8-15		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(P)}$	Page-mode cycle time	t_{PC}	120		140		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	230		260		ns
$t_{c(W)}$	Write cycle time	t_{WC}	230		260		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	315		365		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (precharge time)‡	t_{CP}	40		50		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low	t_{CAS}	70	10,000	80	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge time)	t_{RP}	80		100		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low	t_{RAS}	120	10,000	150	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	30		40		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	50	3	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	5		5		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	50		60		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	50		60		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	35		40		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	20		30		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	85		110		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	40		60		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	90		130		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	10		10		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	40		60		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	90		130		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	120		150		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	70		80		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	30	50	30	70	ns
t_{WLCL}	Delay time, $\overline{W}$ low to $\overline{CAS}$ low (early write cycle)	t_{WCS}	−5		−5		ns
t_{rf}	Refresh time interval	t_{REF}		4		4	ms

†All cycle times assume t_t = 5 ns.
‡Page mode only.

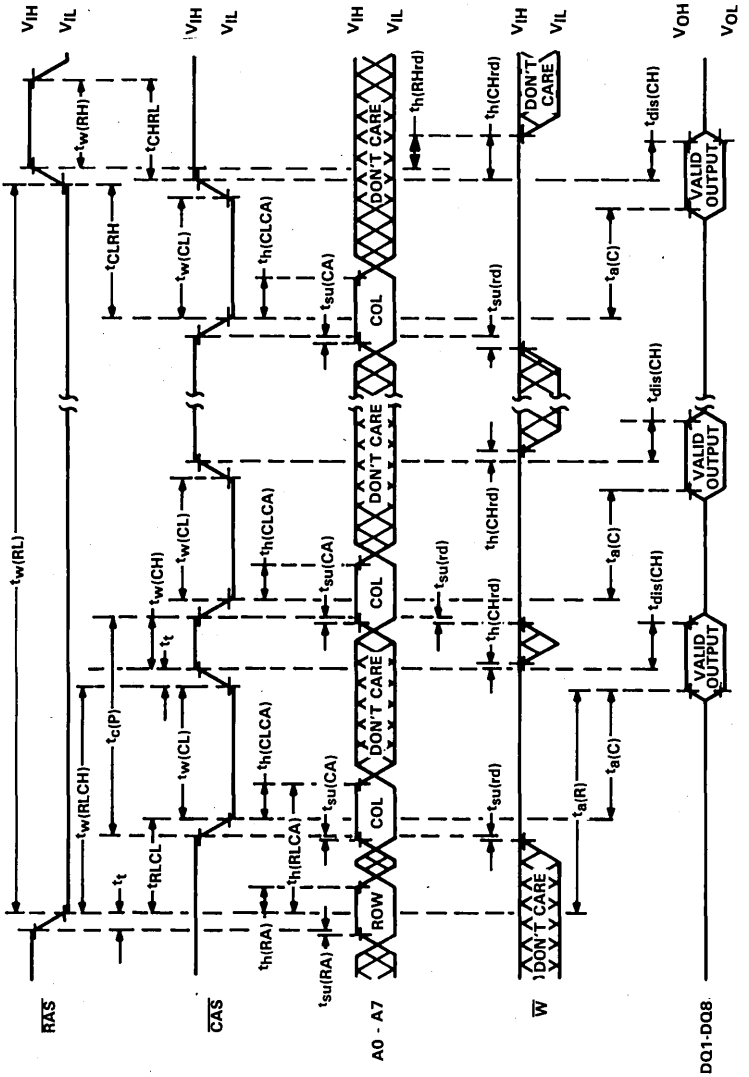
read cycle timing



early write cycle timing

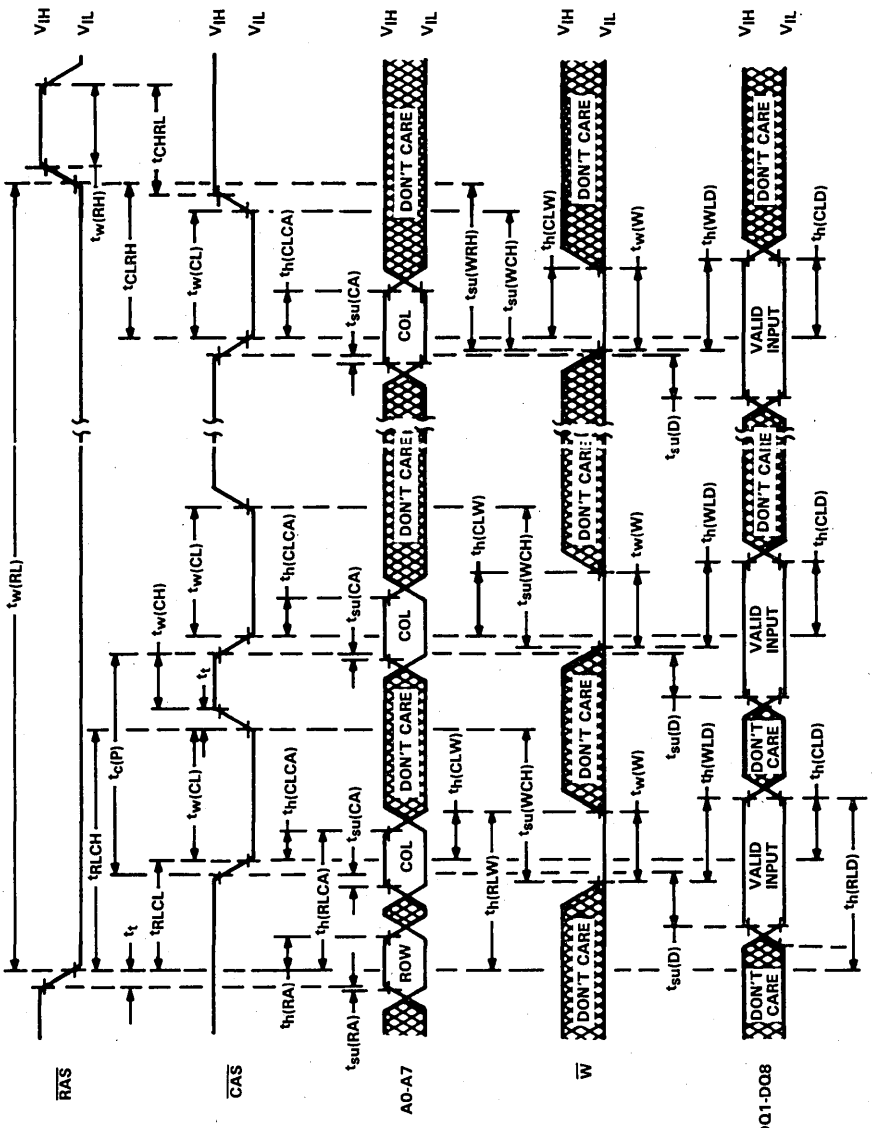


page-mode read cycle timing



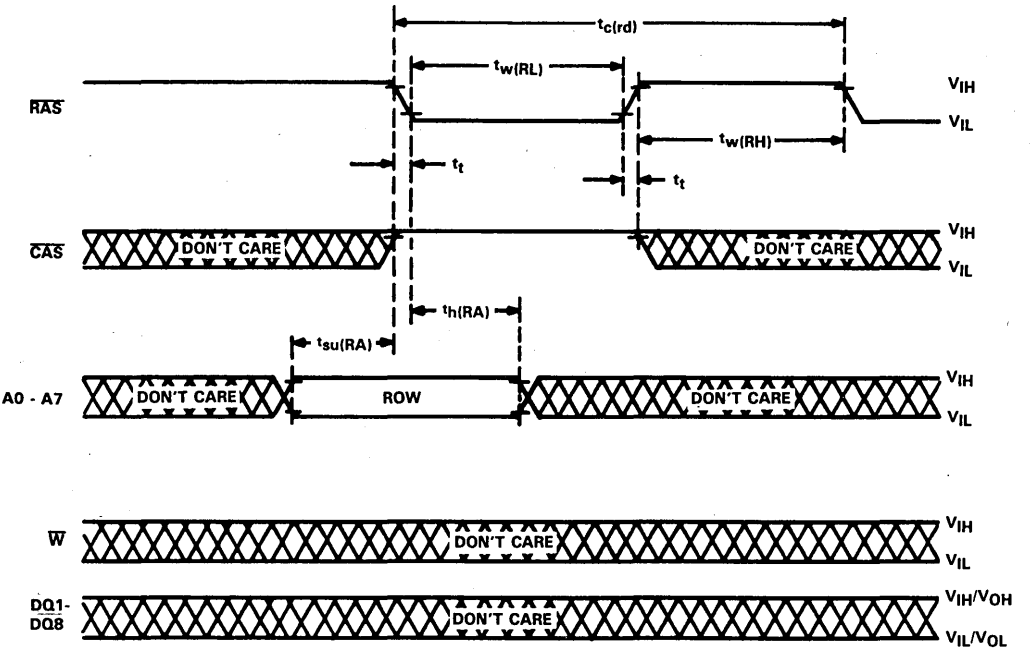
NOTE 4: A write cycle or a read-modify-write cycle can be intermixed with read cycles as long as the write and read-modify-write timing specifications are not violated.

page-mode write cycle timing

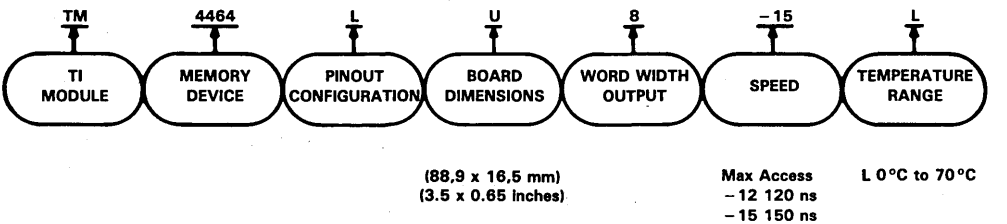


NOTE 5: A read or a read-modify-write cycle can be intermixed with write cycles as long as read and read-modify-write timing specifications are not violated.

RAS-only refresh timing



TI single-in-line package nomenclature



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ATTENTION

These devices contain circuits to protect the inputs and outputs against damage due to high static voltages or electrostatic fields; however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits.

Unused inputs must always be connected to an appropriate logic voltage level, preferably either supply voltage or ground.

Additional information concerning the handling of ESD sensitive devices is provided in Section 12 in a document entitled *"Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies."*

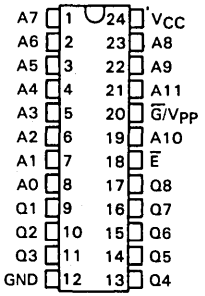
AUGUST 1983 — REVISED NOVEMBER 1985

- Organization . . . 4096 X 8
- Single 5-V Power Supply
- All Inputs and Outputs Are TTL Compatible
- Max Access/Min Cycle Time

TMS2732A-17	170 ns
TMS2732A-20	200 ns
TMS2732A-25	250 ns
TMS2732A-45	450 ns

- Low Standby Power Dissipation . . . 158 mW (Maximum)
- JEDEC Approved Pinout . . . Industry Standard
- 21-V Power Supply Required for Programming
- N-Channel Silicon-Gate Technology
- PEP4 Version Available with 168 Hour Burn-in and Guaranteed Operating Temperature Range from −10°C to 85°C (TMS2732A-_JP4)

J PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A11	Address Inputs
$\overline{E}$	Chip Enable
$\overline{G}/V_{PP}$	Output Enable/21 V
GND	Ground
Q1-Q8	Outputs
V_{CC}	5-V Power Supply

description

The TMS2732A is an ultraviolet light-erasable, electrically programmable read-only memory. It has 32,768 bits organized as 4,096 words of 8-bit length. The TMS2732A only requires a single 5-volt power supply with a tolerance of ±5%.

The TMS2732A provides two output control lines: Output Enable ($\overline{G}$) and Chip Enable ($\overline{E}$). This feature allows the $\overline{G}$ control line to eliminate bus contention in multibus microprocessor systems. The TMS2732A has a power-down mode that reduces maximum power dissipation from 657 mW to 158 mW when the device is placed on standby.

This EPROM is supplied in a 24-pin dual-in-line ceramic package and is designed for operation from 0°C to 70°C.

operation

The six modes of operation for the TMS2732A are listed in the following table.

FUNCTION (PINS)	MODE					
	Read	Deselect	Power Down (Standby)	Program	Program Verification	Inhibit Programming
$\overline{E}$ (18)	V_{IL}	X	V_{IH}	V_{IL}	V_{IL}	V_{IH}
$\overline{G}/V_{PP}$ (20)	V_{IL}	V_{IH}	X	21 V	V_{IL}	21 V
V_{CC} (24)	5 V	5 V	5 V	5 V	5 V	5 V
Q1-Q8 (9 to 11, 13 to 17)	Q	HI-Z	HI-Z	D	Q	HI-Z

X = V_{IH} or V_{IL}

read

The two control pins ($\overline{E}$ and $\overline{G}/V_{PP}$) must have low-level TTL signals in order to provide data at the outputs. Chip enable ($\overline{E}$) should be used for device selection. Output enable ($\overline{G}/V_{PP}$) should be used to gate data to the output pins.

power down

The power-down mode reduces the maximum power dissipation from 657 mW to 158 mW. A TTL high-level signal applied to $\overline{E}$ selects the power-down mode. In this mode, the outputs assume a high-impedance state, independent of $\overline{G}/V_{PP}$.

program

The programming procedure for the TMS2732A is the same as that for the TMS2532, except that in the program mode, $\overline{G}/V_{PP}$ is taken from a TTL low level to 21 V.

The program mode consists of the following sequence of events. With the level on $\overline{G}/V_{PP}$ equal to 21 V, data to be programmed is applied in parallel to output pins Q8-Q1. The location to be programmed is addressed. Once data and addresses are stable, a 10-millisecond TTL low-level pulse is applied to $\overline{E}$. The maximum width of this pulse is 11 milliseconds. The programming pulse must be applied at each location that is to be programmed. Locations may be programmed in any order.

Several TMS2732As can be programmed simultaneously by connecting them in parallel and following the programming sequence previously described.

program verify

After the EPROM has been programmed, the programmed bits should be verified. To verify bit states, $\overline{G}/V_{PP}$ and $\overline{E}$ are set to V_{IL}.

program inhibit

The program inhibit is useful when programming multiple TMS2732As connected in parallel with different data. Program inhibit can be implemented by applying a high-level signal to $\overline{E}$ of the device that is not to be programmed.

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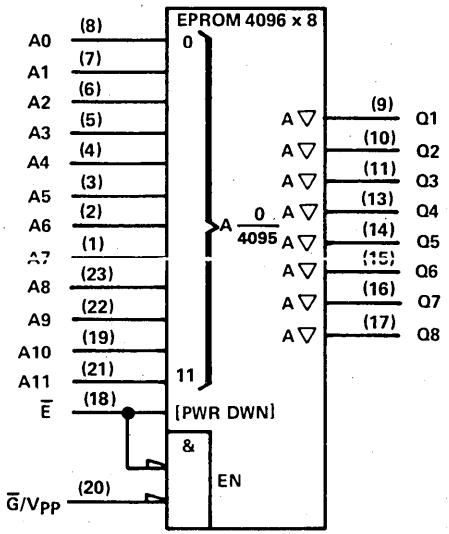
erasure

The TMS2732A is erased by exposing the chip to shortwave ultraviolet light that has a wavelength of 253.7 nanometers (2537 angstroms). The recommended minimum exposure dose (UV intensity × exposure time) is fifteen watt-seconds per square centimeter. The lamp should be located about 2.5 centimeters (1 inch) above the chip during erasure. After erasure, all bits are at a high level. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS2732A, the window should be covered with an opaque label.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.3 V to 7 V
Supply voltage range, V_{PP}	−0.3 V to 22 V
Input voltage range (except program)	−0.3 V to 7 V
Output voltage range	−0.3 V to 7 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (see Note 1)	4.75	5	5.25	V
V_{PP}	Supply voltage (see Note 2)		V_{CC}		V
V_{IH}	High-level input voltage	2		$V_{CC}+1$	V
V_{IL}	Low-level input voltage	−0.1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTES: 1. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.
2. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be $I_{CC} + I_{PP}$. During programming, V_{PP} must be maintained at 21 V (±0.5 V).

electrical characteristics over full ranges of recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −400 μA	2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 2.1 mA		0.45	V
I_I	Input current (leakage)	V_I = 0 V to 5.25 V		±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.25 V		±10	μA
I_{CC1}	V_{CC} supply current (standby)	$\overline{E}$ at V_{IH}, $\overline{G}$ at V_{IL}		30	mA
I_{CC2}	V_{CC} supply current (active)	$\overline{E}$ and $\overline{G}$ at V_{IL}		125	mA

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz†

PARAMETER			TEST CONDITIONS	TYP‡	MAX	UNIT
C_i	Input capacitance	All except $\overline{G}/V_{PP}$	V_I = 0 V	4	6	pF
		$\overline{G}/V_{PP}$			20	
C_o	Output capacitance		V_O = 0 V	8	12	pF

†These parameters are tested on sample basis only.
‡Typical values are at T_A = 25°C and nominal voltages.

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	TMS2732A-17		TMS2732A-20		TMS2732A-25		TMS2732A-45		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL Load, $t_r \le 20$ ns, $t_f \le 20$ ns, See Figure 1 and Note 3		170		200		250		450	ns
$t_{a(E)}$	Access time from $\overline{E}$			170		200		250		450	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			65		70		100		150	ns
t_{dis}†	Output disable time from $\overline{E}$ or $\overline{G}$, whichever occurs first		0	60	0	60	0	85	0	130	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first		0		0		0		0		ns

NOTE 3: The timing reference levels for inputs and outputs are 0.8 V and 2 V. Input pulse levels are 0.40 V and 2.4 V.
†Value calculated from 0.5 V delta to measured output level. This parameter is only sampled and not 100% tested.

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recommended conditions for programming, T_A = 25°C (see Note 4)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{PP}	Supply voltage	20.5	21	21.5	V
V_{IH}	High-level input voltage	2		$V_{CC}+1$	V
V_{IL}	Low-level input voltage	−0.1		0.8	V
$t_{w(E)}$	$\overline{E}$ pulse duration	9	10	11	ms
$t_{su(A)}$	Address setup time	2			μs
$t_{su(D)}$	Data setup time	2			μs
$t_{su(VPP)}$	V_{PP} setup time	2			μs
$t_{h(A)}$	Address hold time	0			μs
$t_{h(D)}$	Data hold time	2			μs
$t_{h(VPP)}$	V_{PP} hold time	2			μs
$t_{rec(PG)}$	V_{PP} recovery time	2			μs
$t_{r(PG)G}$	$\overline{G}$ rise time during programming	50			ns
t_{EHD}	Delay time, data valid after $\overline{E}$ low			1	μs

NOTE 4: When programming the TMS2732A, connect a 0.1 μF capacitor between V_{PP} and GND to suppress spurious voltage transients which may damage the device.

programming characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage		2		$V_{CC}+1$	V
V_{IL}	Low-level input voltage		−0.1		0.8	V
V_{OH}	High-level output voltage (verify)	I_{OH} = −400 μA	2.4			V
V_{OL}	Low-level output voltage (verify)	I_{OL} = 2.1 mA			0.45	V
I_I	Input current (all inputs)	$V_I = V_{IL}$ or V_{IH}			10	μA
I_{PP}	Supply current	$\overline{E} = V_{IL}$, $\overline{G} = V_{PP}$			50	mA
I_{CC}	Supply current				125	mA
$t_{dis(PR)}$	Output disable time		0		130	ns

PARAMETER MEASUREMENT INFORMATION

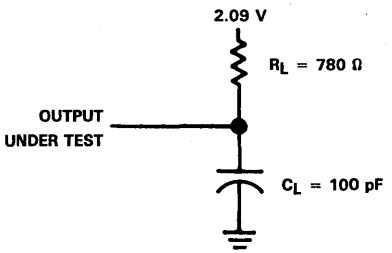
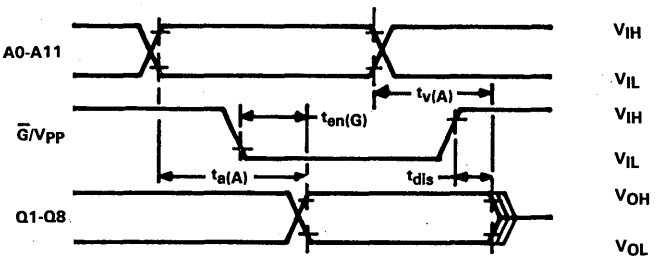
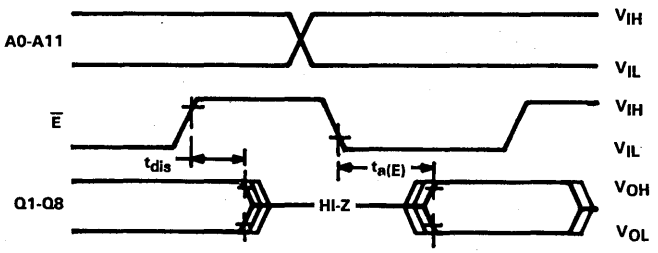


FIGURE 1. TYPICAL OUTPUT LOAD CIRCUIT

read cycle timing



standby mode



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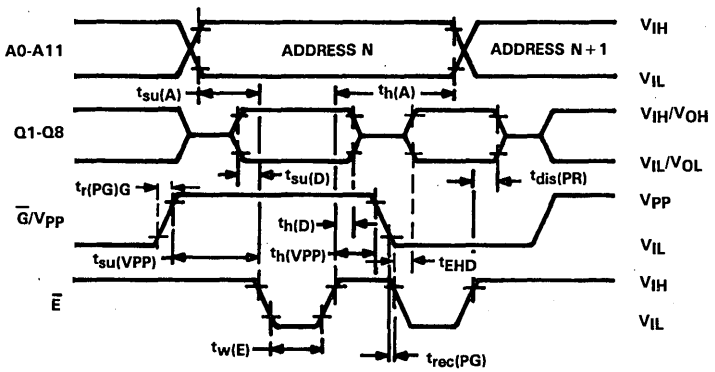
program cycle timing



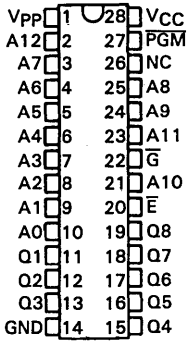
JULY 1983 – REVISED NOVEMBER 1985

- Organization . . . 8192 X 8
- Single 5-V Power Supply
- Pin Compatible with TMS2732A EPROM
- All Inputs and Outputs Are TTL Compatible
- Max Access/Min Cycle Time

TMS2764-17	170 ns
TMS2764-20	200 ns
TMS2764-25	250 ns
TMS2764-45	450 ns

- Low Standby Power Dissipation . . . 184 mW (Maximum)
- JEDEC Approved Pinout
- 21-V Power Supply Required for Programming
- Fast Programming Algorithm
- N-Channel Silicon-Gate Technology
- PEP4 Version Available with 168 Hour Burn-in and Guaranteed Operating Temperature Range from −10°C to 85°C (TMS2764-_JP4)

J PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A12	Address Inputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
GND	Ground
NC	No Connection
$\overline{PGM}$	Program
Q1-Q8	Outputs
V_{CC}	5-V Power Supply
V_{PP}	21-V Power Supply

description

The TMS2764 is an ultraviolet light-erasable, electrically programmable read-only memory. It has 65,536 bits organized as 8,192 words of 8-bit length. The TMS2764-17 only requires a single 5-volt power supply with a tolerance of ±5%, and has a maximum access time of 170 ns. This access time is compatible with high-performance microprocessors.

The TMS2764 provides two output control lines: Output Enable ($\overline{G}$) and Chip Enable ($\overline{E}$). This feature allows the $\overline{G}$ control line to eliminate bus contention in microprocessor systems. The TMS2764 has a power-down mode that reduces maximum power dissipation from 150 mA to 35 mA when the device is placed on standby.

This EPROM is supplied in a 28-pin, 15,2-mm (600-mil) dual-in-line ceramic package and is designed for operation from 0°C to 70°C.

operation

The six modes of operation for the TMS2764 are listed in the following table.

FUNCTION (PINS)	MODE					
	Read	Output Disable	Power Down (Standby)	Fast Programming	Program Verification	Inhibit Programming
$\overline{E}$ (20)	V_{IL}	X	V_{IH}	V_{IL}	V_{IL}	V_{IH}
$\overline{G}$ (22)	V_{IL}	V_{IH}	X	V_{IH}	V_{IL}	X
$\overline{PGM}$ (27)	V_{IH}	V_{IH}	X	V_{IL}	V_{IH}	X
V_{PP} (1)	V_{CC}	V_{CC}	V_{CC}	V_{PP}	V_{PP}	V_{PP} or V_{CC}
V_{CC} (28)	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
Q1-Q8 (11 to 13, 15 to 19)	Q	HI-Z	HI-Z	D	Q	HI-Z

X = V_{IH} or V_{IL}

read

The two control pins ($\overline{E}$ and $\overline{G}$) must have low-level TTL signals in order to provide data at the outputs. Chip enable ($\overline{E}$) should be used for device selection. Output enable ($\overline{G}$) should be used to gate data to the output pins.

power down

The power-down mode reduces the maximum active current from 150 mA to 35 mA. A TTL high-level signal applied to $\overline{E}$ selects the power-down mode. In this mode, the outputs assume a high-impedance state, independent of $\overline{G}$.

erasure

Before programming, the TMS2764 is erased by exposing the chip to shortwave ultraviolet light that has a wavelength of 253.7 nanometers (2537 angstroms). The recommended minimum exposure dose (UV intensity × exposure time) is fifteen watt-seconds per square centimeter. A typical 12 mW/cm2 UV lamp will erase the device in approximately 20 minutes. The lamp should be located about 2.5 centimeters (1 inch) above the chip during erasure. After erasure, all bits are at a high level. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS2764, the window should be covered with an opaque label.

fast programming

Note that the application of a voltage in excess of 22 V to V_{PP} may damage the TMS2764.

After erasure, logic "0's" are programmed into the desired locations. Programming consists of the following sequence of events. With the level on V_{PP} equal to 21 V and $\overline{E}$ at TTL low, data to be programmed is applied in parallel to output pins Q8-Q1. The location to be programmed is addresed. Once data and addresses are stable, a TTL low-level pulse is applied to $\overline{PGM}$. Programming pulses must be applied at each location that is to be programmed. Locations may be programmed in any order.

Programming uses two types of programming pulse: Prime and Final. The length of the Prime pulse is 1 millisecond; this pulse is applied X times. After each application the byte being programmed is verified. If the correct data is read, the Final programming pulse is then applied, if correct data is not read, a further 1 millisecond programming pulse is applied up to a maximum X of 15. The Final programming pulse is 4X milliseconds long. This sequence of programming pulses and byte verification is done at V_{CC} = 6.0 V and V_{PP} = 21.0 V. When the full fast programming routine is complete, all bits are verified with V_{CC} = V_{PP} = 5 V. A flowchart of the fast programming routine is shown in Figure 1.

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multiple device programming

Several TMS2764's can be programmed simultaneously by connecting them in parallel and following the programming sequence previously described.

program inhibit

The program inhibit is useful when programming multiple TMS2764's connected in parallel with different data. Program inhibit can be implemented by applying a high-level signal to $\overline{E}$ or $\overline{PGM}$ of the device that is not to be programmed.

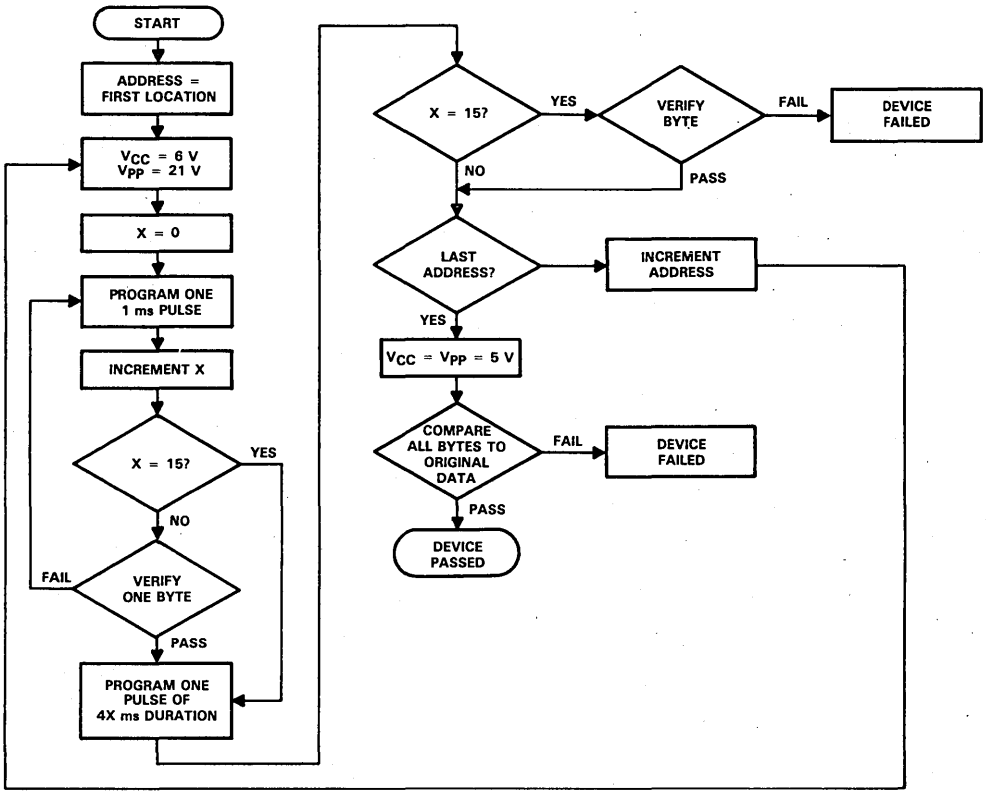
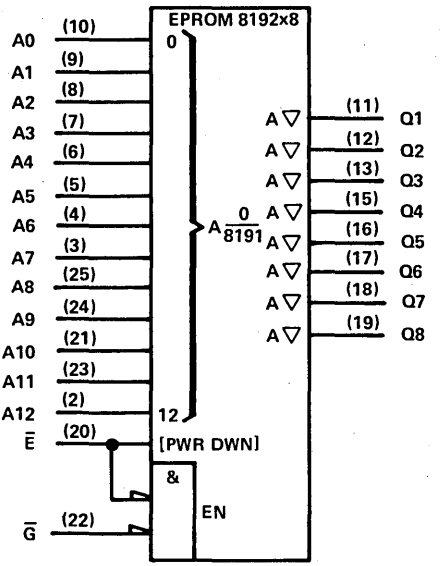


FIGURE 1. FAST PROGRAMMING FLOWCHART

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} . . . . . −0.6 V to 7 V
Supply voltage range, V_{PP} . . . . . −0.6 V to 22 V
Input voltage range . . . . . −0.6 V to 7 V
Output voltage range . . . . . −0.6 V to 7 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

‡Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{PP}	Supply voltage		V_{CC}		V
V_{IH}	High-level input voltage	2		$V_{CC}+1$	V
V_{IL}	Low-level input voltage (see Note 1)	−0.1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 1: The algebraic convention, where the more negative (less positive) limit is designated as minimum is used in this data sheet for logic voltage levels only.

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electrical characteristics over full ranges of recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −400 μA	2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 2.1 mA		0.45	V
I_I	Input current (load)	V_I = 0 V to 5.25 V		±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.25 V		±10	μA
I_{PP1}	V_{PP} supply current (read)	V_{PP} = 5.25 V		15	mA
I_{PP2}	V_{PP} supply current (program)	$\overline{E}$ and $\overline{PGM}$ at V_{IL}		50	mA
I_{CC1}	V_{CC} supply current (standby)	$\overline{E}$ at V_{IH}		35	mA
I_{CC2}	V_{CC} supply current (active)	$\overline{E}$ and $\overline{G}$ at V_{IL}		150	mA

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz†

PARAMETER		TEST CONDITIONS	TYP‡	MAX	UNIT
C_i	Input capacitance	V_I = 0 V	4	6	pF
C_o	Output capacitance	V_O = 0 V	8	12	pF

†Capacitance measurements are made on a sample basis only.
‡Typical values are at T_A = 25°C and nominal voltage.

switching characteristics over recommended supply voltage range and operating free-air temperature range, C_L = 100 pF, 1 Series 74 TTL load (see Note 2 and Figure 2)

PARAMETER		TMS2764-17		TMS2764-20		TMS2764-25		TMS2764-45		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address		170		200		250		450	ns
$t_{a(E)}$	Access time from $\overline{E}$		170		200		250		450	ns
$t_{en(G)}$	Output enable time from $\overline{G}$		65		75		100		150	ns
$t_{dis(G)}$‡	Output disable time from $\overline{G}$	0	60	0	60	0	85	0	130	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first	0		0		0		0		ns

NOTE 2: For all switching characteristics and timing measurements, input pulse levels are 0.40 V and 2.4 V. Input and output timing reference levels are 0.8 V and 2 V.
‡Value clacluated from 0.5 volt delta to measured output level; $t_{dis(G)}$ is specified from $\overline{G}$ or $\overline{E}$, whichever occurs first. Refer to read cycle timing diagram. This parameter is only sampled and is not 100% tested.

recommended conditions for fast programming routine, T_A = 25°C (see Note 2 and fast programming cycle timing diagram)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (see Note 3)	5.75	6	6.25	V
V_{PP}	Supply voltage (see Note 4)	20.5	21	21.5	V
$t_{w(IPGM)}$	$\overline{PGM}$ initial program pulse duration (see Note 5)	0.95	1	1.05	ms
$t_{w(FPGM)}$	$\overline{PGM}$ final pulse duration (see Note 6)	3.8		63	ms
$t_{su(A)}$	Address setup time	2			μs
$t_{su(D)}$	Data setup time	2			μs
$t_{su(VPP)}$	V_{PP} setup time	2			μs
$t_{su(VCC)}$	V_{CC} setup time	2			μs
$t_{h(A)}$	Address hold time	0			μs
$t_{h(D)}$	Data hold time	2			μs
$t_{su(E)}$	$\overline{E}$ setup time	2			μs
$t_{su(G)}$	$\overline{G}$ setup time	2			μs

fast programming characteristics, T_A = 25°C (see Note 2 and fast programming cycle timing diagram)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{dis(G)FP}$	Output disable time from $\overline{G}$ (see Note 7)	C_L = 100 pF	0		130	ns
$t_{en(G)FP}$	Output enable time from $\overline{G}$	1 Series 74 TTL Load			150	

NOTES: 2. For all switching characteristics and timing measurements, input pulse levels are 0.40 V and 2.4 V. Input and output timing reference levels are 0.8 V and 2 V.
3. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
4. When programming the TMS2764, connect a 0.1 μF capacitor between V_{PP} and GND to suppress spurious voltage transients which may damage the device.
5. The Initial program pulse duration tolerance is 1 ms ±5%.
6. The length of the Final pulse will vary from 3.8 ms to 63 ms depending on the number of Initial pulse applications (X).
7. This parameter is only sampled and is not 100% tested.

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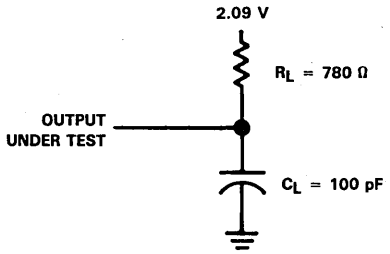
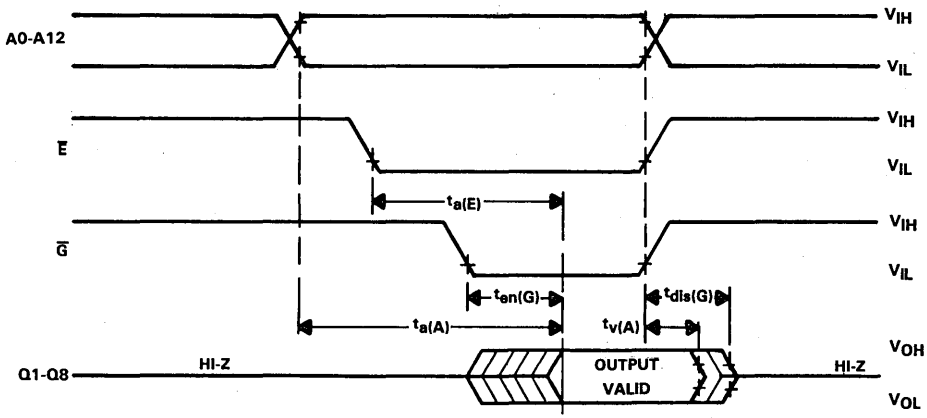
PARAMETER MEASUREMENT INFORMATION



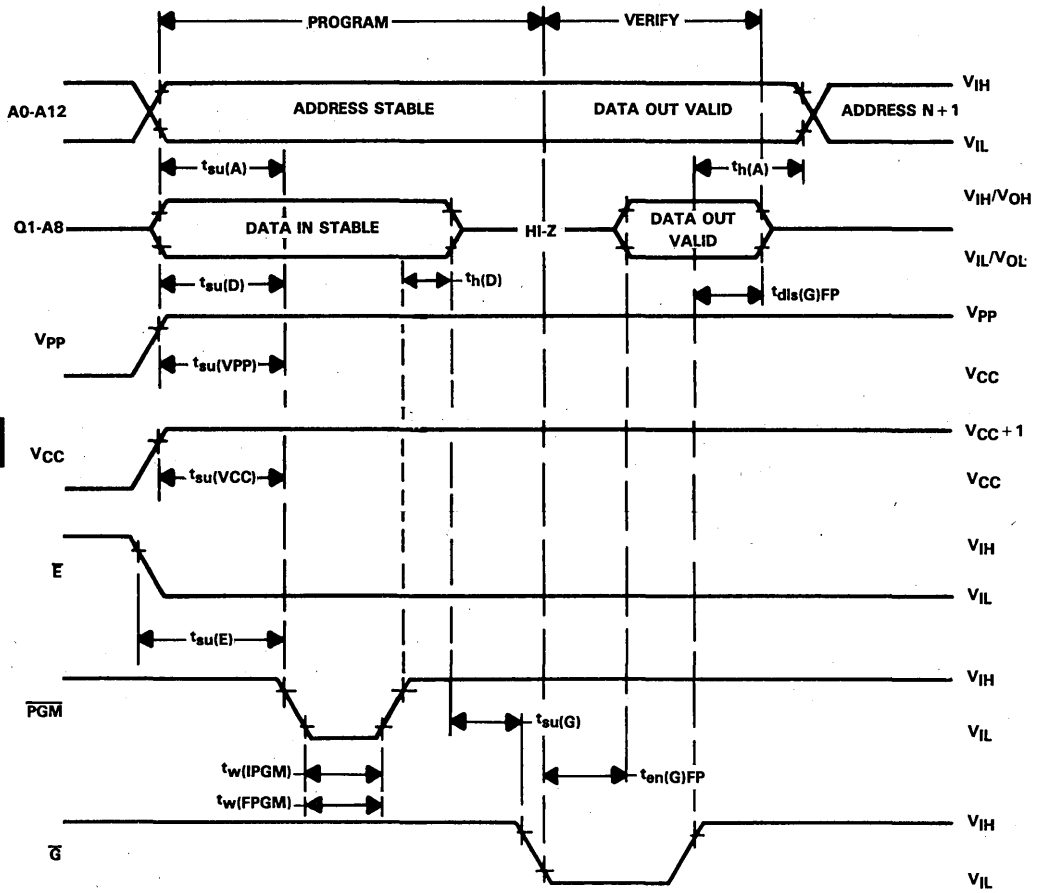
NOTE 8: $t_f \leq 20$ ns and $t_r \leq 20$ ns.

FIGURE 2. TYPICAL OUTPUT LOAD CIRCUIT

read cycle timing



fast program cycle timing



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ENHANCED PERFORMANCE EPROMS — PEP4

- 168 hr ± 8 hr Burn-in at 125°C
- Tested to 0.1% AQL
- Extended Temperature Range

Texas Instruments offers extended temperature range EPROMs which provide an enhanced degree of reliability.

The PEP4 designation signifies:

- Devices Subjected to Electrical Testing over a Temperature Range Exceeding Commercial Requirements.
- All Devices Have Received a 168 hr ± 8 hr 125°C Burn-in with a PDA of 2%.

This combination results in an improved quality and reliability level for those applications which deem it necessary. The user benefits from improved long term cost realized through reduced system down-time.

PEP4 PRODUCT FAMILY

DEVICE	ORGANIZATION	MAXIMUM ACCESS TIME (ns)	V_{CC} SUPPLY VOLTAGE (V) MIN	MAX	OPERATING TEMPERATURE RANGE (°C)
TMS2732A-__JP4	4096 X 8	250	4.5	5.5	−10 to 85
		450	4.5	5.5	−10 to 85
TMS2764-__JP4	8192 X 8	250	4.5	5.5	−10 to 85
		450	4.5	5.5	−10 to 85

ELECTRICAL CHARACTERISTICS

PEP4 EPROM devices meet or exceed all the electrical and timing parameters specified in the standard data sheet with the following exceptions.

PARAMETER		TMS2732A-__JP4 MAX	TMS2764-__JP4 MAX	UNIT
I_{CC1}	V_{CC} supply current (standby)	35	40	mA
I_{CC2}	V_{CC} supply current (active)	150		mA

TMS27C64
65,536-BIT ERASABLE PROGRAMMABLE READ-ONLY MEMORY

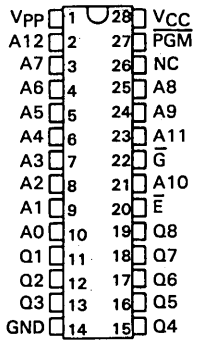
NOVEMBER 1985

- Organization . . . 8K × 8
- Single 5-V Power Supply
- Pin Compatible with Existing 64K EPROMs and TMS2732A
- All Inputs/Outputs Fully TTL Compatible
- Max Access/Min Cycle Time

'27C64-1,	'27C64-15	150 ns
'27C64-2,	'27C64-20	200 ns
'27C64,	'27C64-25	250 ns
'27C64-3,	'27C64-30	300 ns
'27C64-4,	'27C64-45	450 ns

- HVCMOS Technology
- 3-State Output Buffers
- 400 mV Guaranteed DC Noise Immunity with Standard TTL Loads
- Low Power Dissipation (V_{CC} = 5.25 V)
  - —Active . . . 210 mW Worst Case
  - —Standby . . . 1.4 mW Worst Case (CMOS-Input Levels)

J PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A12	Address Inputs
$\overline{E}$	Chip Enable/Power Down
$\overline{G}$	Output Enable
GND	Ground
NC	No Connection
$\overline{PGM}$	Program
Q1-Q8	Outputs
V_{CC}	5-V Power Supply
V_{PP}	12.5-V Power Supply

description

The TMS27C64 series are 65,536-bit, ultraviolet-light erasable, electrically programmable read-only memories. These devices are fabricated using HVCMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull-up resistors, and each output can drive one Series 74 TTL circuit without external resistors. The data outputs are three-state for connecting multiple devices to a common bus. The TMS27C64 is pin compatible with existing 28-pin ROMs and EPROMs. It is offered in a dual-in-line ceramic package (J suffix) rated for operation from 0°C to 70°C.

Since these EPROMs operate from a single 5-V supply (in the read mode), they are ideal for use in microprocessor-based systems. One other (12.5 V) supply is needed for programming, but all programming signals are TTL level. For programming outside the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random.

operation

There are seven modes of operation for the TMS27C64 listed on the following page. Read mode requires a single 5-V supply. All inputs are TTL level except for V_{PP} during programming (12.5 V) and 12 V on A9 for signature mode.

FUNCTION (PINS)	MODE							
	Read	Output Disable	Standby	Programming	Verify	Program Inhibit	Signature Mode	
$\overline{E}$ (20)	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	
$\overline{G}$ (22)	V_{IL}	V_{IH}	X†	V_{IH}	V_{IL}	X	V_{IL}	
$\overline{PGM}$ (27)	V_{IH}	V_{IH}	X	V_{IL}	V_{IH}	X	V_{IH}	
V_{PP} (1)	V_{CC}	V_{CC}	V_{CC}	V_{PP}	V_{PP}	V_{PP}	V_{CC}	
V_{CC} (28)	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A9 (24)	X	X	X	X	X	X	V_H‡	V_H‡
A0 (10)	X	X	X	X	X	X	V_{IL}	V_{IH}
Q1-Q8 (11-13, 15-19)	D_{OUT}	HI-Z	HI-Z	D_{IN}	D_{OUT}	HI-Z	CODE	
							MFG	DEVICE
							97	07

†X can be V_{IL} or V_{IH}.
‡V_H = 12 V ± 0.5 V.

read/output disable

When the outputs of two or more TMS27C64's are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. To read the output of the TMS27C64, a low-level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins. Output data is accessed at pins Q1 to Q8.

power down

Active I_{CC} current can be reduced from 40 mA to 500 μA (TTL-level inputs) or 250 μA (CMOS-level inputs) by applying a high TTL signal to the $\overline{E}$ pin. In this mode all outputs are in the high-impedance state.

erasure

Before programming, the TMS27C64 is erased by exposing the chip through the transparent lid to high intensity ultraviolet light (wavelength 2537 angstroms). The recommended minimum exposure dose (UV intensity × exposure time) is fifteen watt-seconds per square centimeter. A typical 12 milliwatt per square centimeter, filterless UV lamp will erase the device in 21 minutes. The lamp should be located about 2.5 centimeters above the chip during erasure. After erasure, all bits are in the high state. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS27C64, the window should be covered with an opaque label.

fast programming

After erasure (all bits in logic '1' state), logic '0's are programmed into the desired locations. A programmed '0' can only be erased by ultraviolet light. Data is presented in parallel (eight bits) on pins Q1 to Q8. Once addresses and data are stable, $\overline{PGM}$ is pulsed. The programming mode is achieved when V_{PP} = 12.5 V, $\overline{PGM}$ = V_{IL}, V_{CC} = 6.0 V, $\overline{G}$ = V_{IH}, and $\overline{E}$ = V_{IL}. More than one TMS27C64 can be programmed when the devices are connected in parallel. Locations can be programmed in any order.

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Programming uses two types of programming pulses: Prime and Final. The length of the Prime pulse is 1 millisecond; this pulse is applied X times. After each Prime pulse, the byte being programmed is verified. If the correct data is read, the Final programming pulse is applied; if correct data is not read, an additional 1 millisecond pulse is applied up to a maximum X of 25. The Final programming pulse is 3X long. This sequence of programming and verification is performed at V_{CC} = 6.0 V and V_{PP} = 12.5 V. When the full fast programming routine is complete, all bits are verified with V_{CC} = V_{PP} = 5 V (see Figure 1).

program inhibit

Programming may be inhibited by maintaining a high level input on the $\overline{E}$ pin or $\overline{PGM}$ pin.

program verify

Programmed bits may be verified with V_{PP} = 12.5 V when $\overline{G}$ = V_{IL}, $\overline{E}$ = V_{IL} and $\overline{PGM}$ = V_{IH}.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 (pin 24) is forced to 12 V ± 0.5 V. Two identifier bytes are accessed by A0 (pin 10) i.e., A0 = V_{IL} – manufacturer; A0 = V_{IH} – device. All other addresses must be held at V_{IL}. Each byte possesses odd parity on bit Q8. The manufacturer code for this device is 97, and the device code is 07.

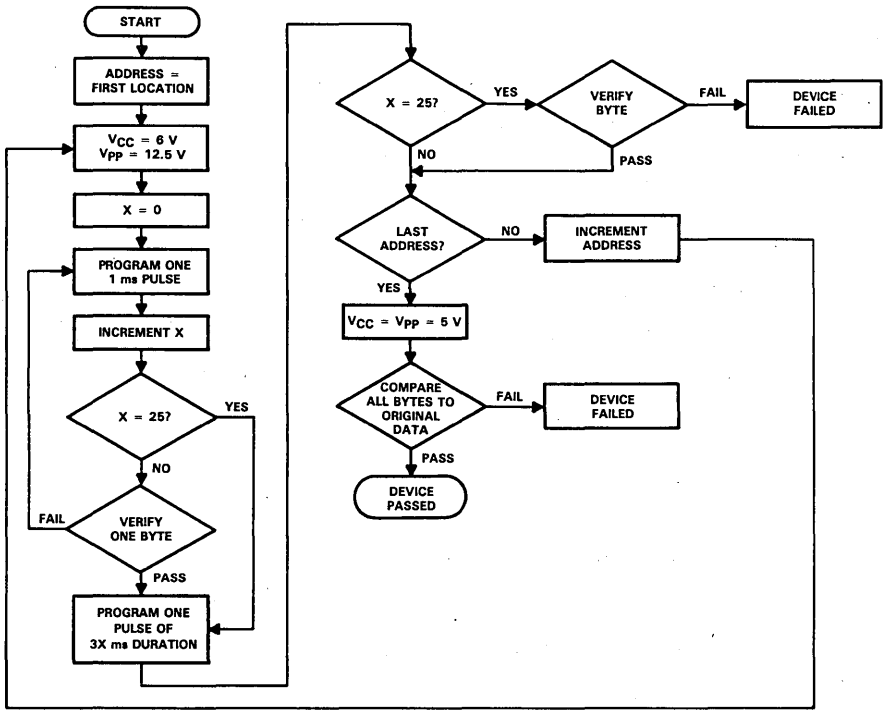
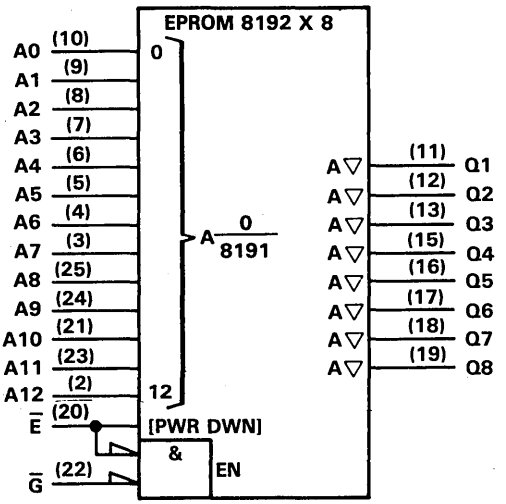


FIGURE 1. FAST PROGRAMMING FLOWCHART

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.6 V to 7 V
Supply voltage range, V_{PP} (see Note 1) . . . . . −0.6 V to 14 V
Input voltage range (see Note 1): All inputs except A9 . . . . . −0.6 V to 6.5 V
A9 . . . . . −0.6 V to 13.5 V
Output voltage range (see Note 1) . . . . . −0.6 V to V_{CC} + 1 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings, voltage values are with respect to GND.

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recommended operating conditions

			TMS27C64-1, TMS27C64-2, TMS27C64, TMS27C64-3, TMS27C64-4			TMS27C64-15, TMS27C64-20, TMS27C64-25, TMS27C64-30, TMS27C64-45			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)		4.75	5	5.25	4.5	5	5.5	V
V_{PP}	Supply voltage (see Note 3)			V_{CC}			V_{CC}		V
V_{IH}	High-level input voltage	TTL	2		$V_{CC}+1$	2		$V_{CC}+1$	V
		CMOS	$V_{CC}-0.2$		$V_{CC}+0.2$	$V_{CC}-0.2$		$V_{CC}+0.2$	V
V_{IL}	Low-level input voltage	TTL	−0.5		0.8	−0.5		0.8	V
		CMOS	GND−0.2		GND+0.2	GND−0.2		GND+0.2	V
T_A	Operating free-air temperature		0		70	0		70	°C

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.
3. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be $I_{CC}+I_{PP}$. During programming, V_{PP} must be maintained at 12.5 V (±0.5 V).

electrical characteristics over full ranges of recommended operating conditions

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = −400 μA	2.4			V
V_{OL}	Low-level output voltage		I_{OL} = 2.1 mA			0.4	V
I_I	Input current (leakage)		V_I = 0 V to 5.5 V			±10	μA
I_O	Output current (leakage)		V_O = 0 V to V_{CC}			±10	μA
I_{PP1}	V_{PP} supply current		V_{PP} = V_{CC} = 5.5 V			100	μA
I_{PP2}	V_{PP} supply current (during program pulse)		V_{PP} = 13 V		30	50	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{IH}			500	μA
		CMOS-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{CC}			250	μA
I_{CC2}	V_{CC} supply current (active)		V_{CC} = 5.5 V, $\overline{E}$ = V_{IL}, t_{cycle} = minimum cycle time, outputs open		30	40	mA

†Typical values are at T_A = 25°C and nominal voltages.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz†

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
C_i	Input capacitance	V_I = 0 V, f = 1 MHz		6	9	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz		8	12	pF

†Capacitance measurements are made on sample basis only.
‡Typical values are at T_A = 25°C and nominal voltages.

switching characteristics over full ranges of recommended operating conditions (see Note 4)

PARAMETER		TEST CONDITIONS (SEE NOTES 4 AND 5)	'27C64-1 '27C64-15		'27C64-2 '27C64-20		'27C64 '27C64-25		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL Load, Input $t_r \leq 20$ ns, Input $t_f \leq 20$ ns		150		200		250	ns
$t_{a(E)}$	Access time from chip enable			150		200		250	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			75		75		100	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first†		0	60	0	60	0	60	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first†		0		0		0		ns

PARAMETER		TEST CONDITIONS (SEE NOTES 4 AND 5)	'27C64-3 '27C64-30		'27C64-4 '27C64-45		UNIT
			MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL Load, Input $t_r \leq 20$ ns, Input $t_f \leq 20$ ns		300		450	ns
$t_{a(E)}$	Access time from chip enable			300		450	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			120		150	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first†		0	105	0	130	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first†		0		0		ns

†Value calculated from 0.5 V delta to measured output level. This parameter is only sampled and not 100% tested.

recommended timing requirements for programming, T_A = 25°C, V_{CC} = 6 V, V_{PP} = 12.5 V (see Note 4)

		MIN	NOM	MAX	UNIT
$t_{w(IPGM)}$	Initial program pulse duration	0.95	1	1.05	ms
$t_{w(FPGM)}$	Final pulse duration	2.85		78.75	ms
$t_{su(A)}$	Address setup time	2			µs
$t_{su(E)}$	$\overline{E}$ setup time	2			µs
$t_{su(G)}$	$\overline{G}$ setup time	2			µs
$t_{dis(G)}$	Output disable time from $\overline{G}$	0		130	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			150	ns
$t_{su(D)}$	Data setup time	2			µs
$t_{su(VPP)}$	V_{PP} setup time	2			µs
$t_{su(VCC)}$	V_{CC} setup time	2			µs
$t_{h(A)}$	Address hold time	0			µs
$t_{h(D)}$	Data hold time	2			µs

NOTES: 4. For all switching characteristics and timing measurements, input pulse levels are 0.40 V to 2.4 V and V_{PP} = 12.5 V ±0.5 V during programming.
5. Common test conditions apply for $t_{dis(G)}$ except during programming.

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PARAMETER MEASUREMENT INFORMATION

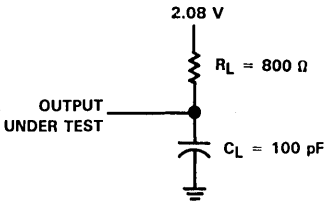
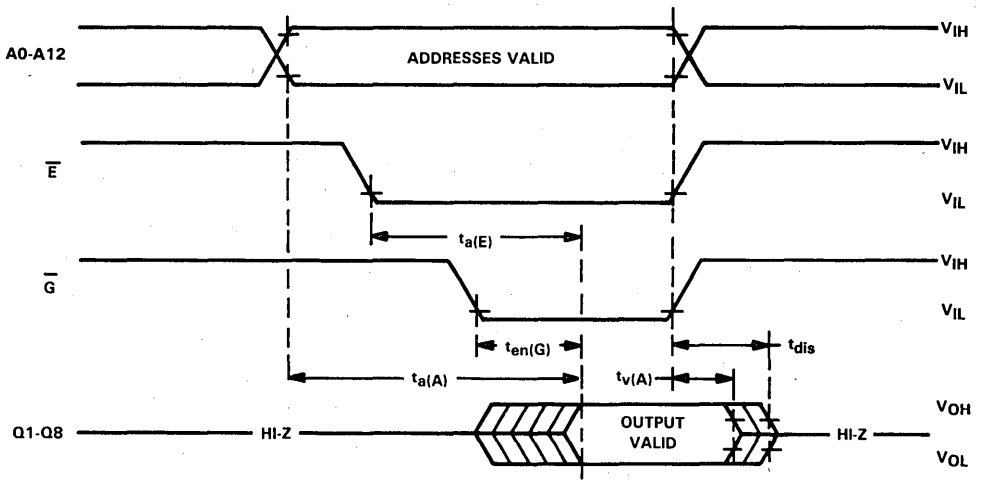
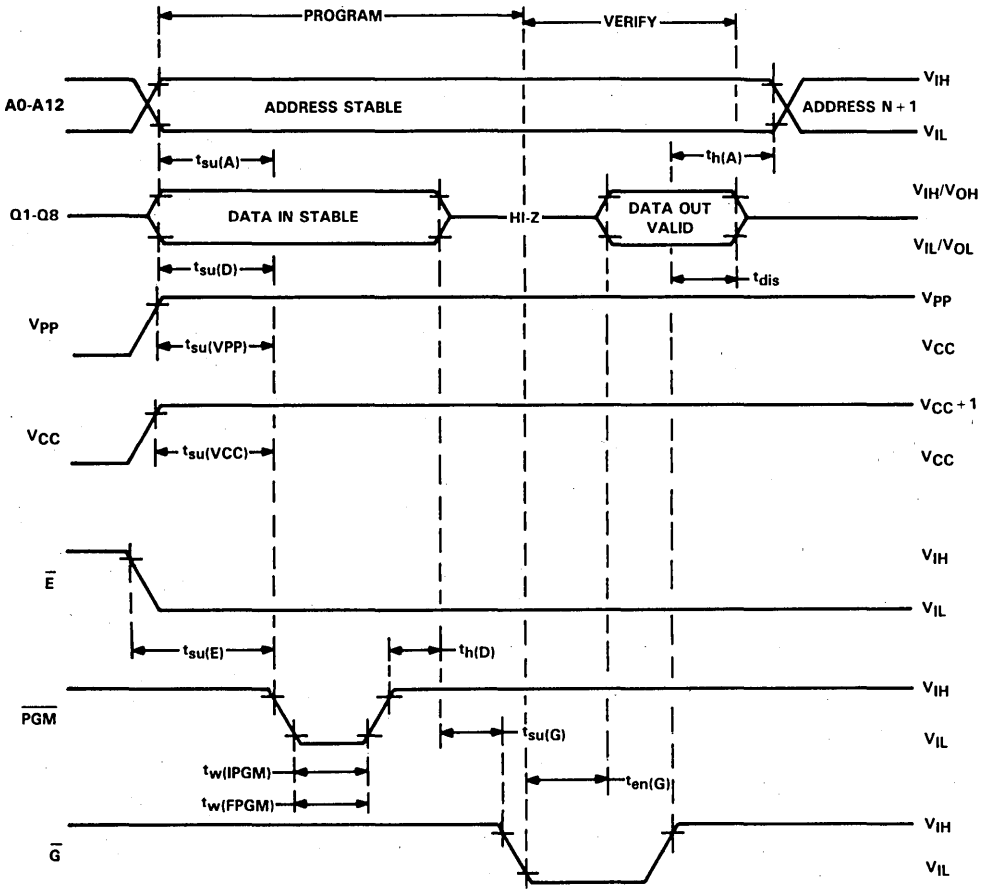


FIGURE 2. OUTPUT LOAD CIRCUIT

read cycle timing



program cycle timing



TEXAS INSTRUMENTS
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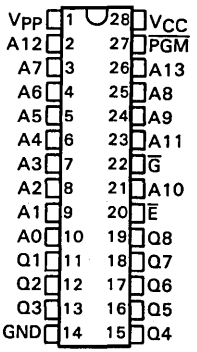
OCTOBER 1984 – REVISED NOVEMBER 1985

- Organization . . . 16K × 8
- Single 5-V Power Supply
- Pin Compatible with Existing 64K and 128K EPROMs
- All Inputs/Outputs Fully TTL Compatible
- Max Access/Min Cycle Time

'27C128-1,	'27C128-15	150 ns
'27C128-2,	'27C128-20	200 ns
'27C128,	'27C128-25	250 ns
'27C128-3,	'27C128-30	300 ns
'27C128-4,	'27C128-45	450 ns

- HVCMOS Technology
- 3-State Output Buffers
- 400 mV Guaranteed DC Noise Immunity with Standard TTL Loads
- Low Power Dissipation (V_{CC} = 5.25 V)
  - —Active . . . 210 mW Worst Case
  - —Standby . . . 1.4 mW Worst Case (CMOS-Input Levels)

J PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A13	Address Inputs
$\overline{E}$	Chip Enable/Power Down
$\overline{G}$	Output Enable
GND	Ground
$\overline{PGM}$	Program
Q1-Q8	Outputs
V_{CC}	5-V Power Supply
V_{PP}	12.5-V Power Supply

description

The TMS27C128 series are 131,072-bit, ultraviolet-light erasable, electrically programmable read-only memories. These devices are fabricated using HVCMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull-up resistors, and each output can drive one Series 74 TTL circuit without external resistors. The data outputs are three state for connecting multiple devices to a common bus. The TMS27C128 is pin compatible with existing 28-pin ROMs and EPROMs. It is offered in a dual-in-line ceramic package (J suffix) rated for operation from 0°C to 70°C.

Since these EPROMs operate from a single 5-V supply (in the read mode), they are ideal for use in microprocessor-based systems. One other (12.5 V) supply is needed for programming, but all programming signals are TTL level. For programming outside the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random.

operation

There are seven modes of operation for the TMS27C128 listed on the following page. Read mode requires a single 5-V supply. All inputs are TTL level except for V_{PP} during programming (12.5 V) and 12 V on A9 for signature mode.

FUNCTION (PINS)	MODE							
	Read	Output Disable	Standby	Programming	Verify	Program Inhibit	Signature Mode	
$\overline{E}$ (20)	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	
$\overline{G}$ (22)	V_{IL}	V_{IH}	X†	V_{IH}	V_{IL}	X	V_{IL}	
$\overline{PGM}$ (27)	V_{IH}	V_{IH}	X	V_{IL}	V_{IH}	X	V_{IH}	
V_{PP} (1)	V_{CC}	V_{CC}	V_{CC}	V_{PP}	V_{PP}	V_{PP}	V_{CC}	
V_{CC} (28)	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A9 (24)	X	X	X	X	X	X	V_H‡	V_H‡
A0 (10)	X	X	X	X	X	X	V_{IL}	V_{IH}
Q1-Q8 (11-13, 15-19)	D_{OUT}	HI-Z	HI-Z	D_{IN}	D_{OUT}	HI-Z	CODE	
							MFG	DEVICE
							97	83

†X can be V_{IL} or V_{IH}.
‡V_H = 12 V ± 0.5 V.

read/output disable

When the outputs of two or more TMS27C128's are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. To read the output of the TMS27C128, a low-level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins. Output data is accessed at pins Q1 to Q8.

power down

Active I_{CC} current can be reduced from 40 mA to 500 μA (TTL-level inputs) or 250 μA (CMOS-level inputs) by applying a high TTL signal to the $\overline{E}$ pin. In this mode all outputs are in the high-impedance state.

erasure

Before programming, the TMS27C128 is erased by exposing the chip through the transparent lid to high intensity ultraviolet light (wavelength 2537 angstroms). The recommended minimum exposure dose (UV intensity × exposure time) is fifteen watt-seconds per square centimeter. A typical 12 milliwatt per square centimeter, filterless UV lamp will erase the device in 21 minutes. The lamp should be located about 2.5 centimeters above the chip during erasure. After erasure, all bits are in the high state. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS27C128, the window should be covered with an opaque label.

fast programming

After erasure (all bits are in logic '1' state), logic '0's are programmed into the desired locations. A programmed '0' can only be erased by ultraviolet light. Data is presented in parallel (eight bits) on pins Q1 to Q8. Once addresses and data are stable, $\overline{PGM}$ is pulsed. The programming mode is achieved when V_{PP} = 12.5 V, $\overline{PGM}$ = V_{IL}, V_{CC} = 6.0 V, $\overline{G}$ = V_{IH}, and $\overline{E}$ = V_{IL}. More than one TMS27C128 can be programmed when the devices are connected in parallel. Locations can be programmed in any order.

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Programming uses two types of programming pulses: Prime and Final. The length of the Prime pulse is 1 millisecond; this pulse is applied X times. After each Prime pulse, the byte being programmed is verified. If the correct data is read, the Final programming pulse is applied; if correct data is not read, an additional 1 millisecond pulse is applied up to a maximum X of 25. The Final programming pulse is 3X long. This sequence of programming and verification is performed at V_{CC} = 6.0 V and V_{PP} = 12.5 V. When the full fast programming routine is complete, all bits are verified with V_{CC} = V_{PP} = 5 V (see Figure 1).

program inhibit

Programming may be inhibited by maintaining a high level input on the $\overline{E}$ pin or $\overline{PGM}$ pin.

program verify

Programmed bits may be verified with V_{PP} = 12.5 V when $\overline{G}$ = V_{IL}, $\overline{E}$ = V_{IL}, and $\overline{PGM}$ = V_{IH}.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 (pin 24) is forced to 12 V ± 0.5 V. Two identifier bytes are accessed by A0 (pin 10) i.e., A0 = V_{IL} – manufacturer; A0 = V_{IH} – device. All other addresses must be held at V_{IL}. Each byte possesses odd parity on bit Q8. The manufacturer code for this device is 97, and the device code is 83.

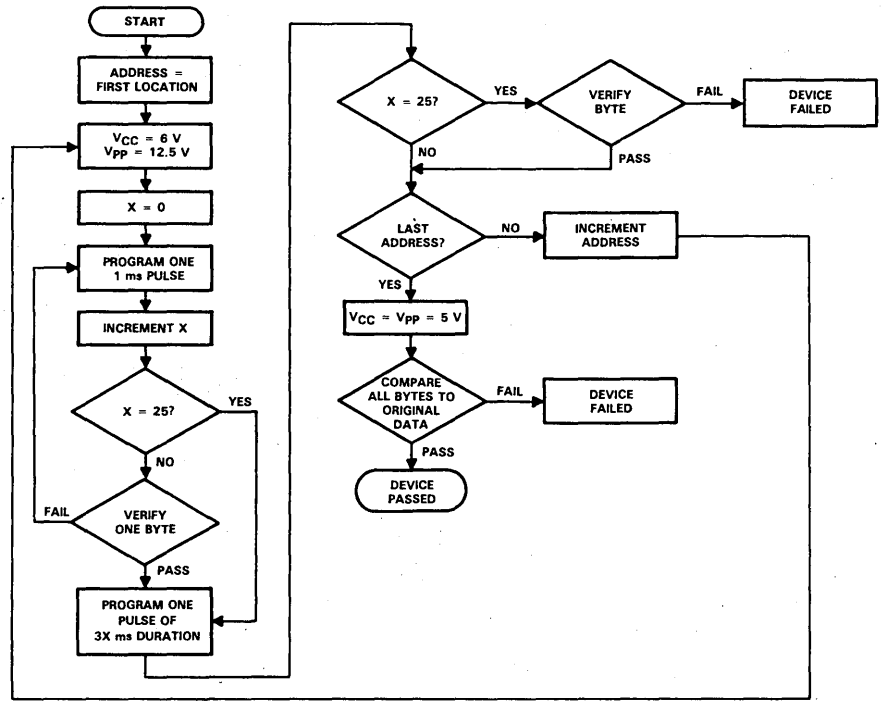
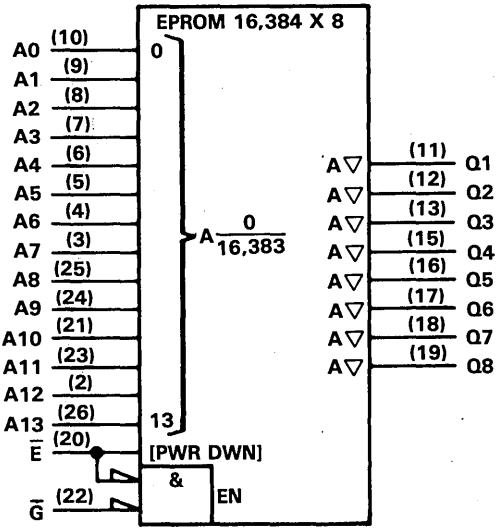


FIGURE 1. FAST PROGRAMMING FLOWCHART

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.6 V to 7 V
Supply voltage range, V_{PP} (see Note 1) . . . . . −0.6 V to 14 V
Input voltage range (see Note 1): All inputs except A9 . . . . . −0.6 V to 6.5 V
A9 . . . . . −0.6 V to 13.5 V
Output voltage range (see Note 1) . . . . . −0.6 V to V_{CC} + 1 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings, voltage values are with respect to GND.

TEXAS INSTRUMENTS
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recommended operating conditions

			TMS27C128-1 TMS27C128-2 TMS27C128 TMS27C128-3 TMS27C128-4			TMS27C128-15 TMS27C128-20 TMS27C128-25 TMS27C128-30 TMS27C128-45			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)		4.75	5	5.25	4.5	5	5.5	V
V_{PP}	Supply voltage (see Note 3)			V_{CC}			V_{CC}		V
V_{IH}	High-level input voltage	TTL	2		$V_{CC}+1$	2		$V_{CC}+1$	V
		CMOS	$V_{CC}-0.2$		$V_{CC}+0.2$	$V_{CC}-0.2$		$V_{CC}+0.2$	V
V_{IL}	Low-level input voltage	TTL	−0.5		0.8	−0.5		0.8	V
		CMOS	GND−0.2		GND+0.2	GND−0.2		GND+0.2	V
T_A	Operating free-air temperature		0		70	0		70	°C

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.
3. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be $I_{CC}+I_{PP}$. During programming, V_{PP} must be maintained at 12.5 V (±0.5V).

electrical characteristics over full ranges of recommended operating conditions

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = −400 μA	2.4			V
V_{OL}	Low-level output voltage		I_{OL} = 2.1 mA			0.4	V
I_I	Input current (leakage)		V_I = 0 V to 5.5 V			±10	μA
I_O	Output current (leakage)		V_O = 0 V to V_{CC}			±10	μA
I_{PP1}	V_{PP} supply current		V_{PP} = V_{CC} = 5.5 V			100	μA
I_{PP2}	V_{PP} supply current (during program pulse)		V_{PP} = 13 V		30	50	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{IH}			500	μA
		CMOS-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{CC}			250	μA
I_{CC2}	V_{CC} supply current (active)		V_{CC} = 5.5 V, $\overline{E}$ = V_{IL}, t_{cycle} = minimum cycle time, outputs open		30	40	mA

†Typical values are at T_A = 25°C and nominal voltages.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz†

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
C_i	Input capacitance	V_I = 0 V, f = 1 MHz		6	9	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz		8	12	pF

†Capacitance measurements are made on sample basis only.
‡Typical values are at T_A = 25°C and nominal voltages.

switching characteristics over full ranges of recommended operating conditions (see Note 4)

PARAMETER		TEST CONDITIONS (SEE NOTES 4 AND 5)	'27C128-1 '27C128-15		'27C128-2 '27C128-20		'27C128 '27C128-25		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL Load, Input $t_r \leq 20$ ns, Input $t_f \leq 20$ ns		150		200		250	ns
$t_{a(E)}$	Access time from chip enable			150		200		250	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			75		75		100	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first†		0	60	0	60	0	60	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first†		0		0		0		ns

PARAMETER		TEST CONDITIONS (SEE NOTES 4 AND 5)	'27C128-3 '27C128-30		'27C128-4 '27C128-45		UNIT
			MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL Load, Input $t_r \leq 20$ ns, Input $t_f \leq 20$ ns		300		450	ns
$t_{a(E)}$	Access time from chip enable			300		450	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			120		150	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first†		0	105	0	130	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first†		0		0		ns

†Value calculated from 0.5 V delta to measured output level. This parameter is only sampled and not 100% tested.

recommended timing requirements for programming, T_A = 25°C, V_{CC} = 6 V, V_{PP} = 12.5 V (see Note 4)

		MIN	NOM	MAX	UNIT
$t_{w(IPGM)}$	Initial program pulse duration	0.95	1	1.05	ms
$t_{w(FPGM)}$	Final pulse duration	2.85		78.75	ms
$t_{su(A)}$	Address setup time	2			μs
$t_{su(E)}$	$\overline{E}$ setup time	2			μs
$t_{su(G)}$	$\overline{G}$ setup time	2			μs
$t_{dis(G)}$	Output disable time from $\overline{G}$	0		130	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			150	ns
$t_{su(D)}$	Data setup time	2			μs
$t_{su(VPP)}$	V_{PP} setup time	2			μs
$t_{su(VCC)}$	V_{CC} setup time	2			μs
$t_{h(A)}$	Address hold time	0			μs
$t_{h(D)}$	Data hold time	2			μs

NOTES: 4. For all switching characteristics and timing measurements, input pulse levels are 0.40 V to 2.4 V and V_{PP} = 12.5 V ±0.5 V during programming.
5. Common test conditions apply for $t_{dis(G)}$ except during programming.

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PARAMETER MEASUREMENT INFORMATION

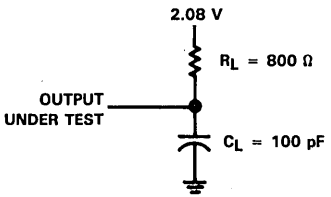
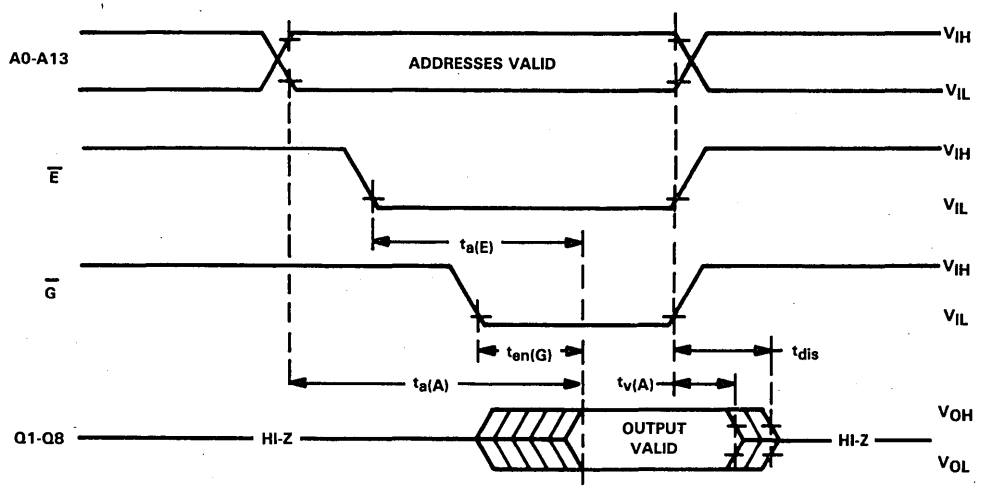
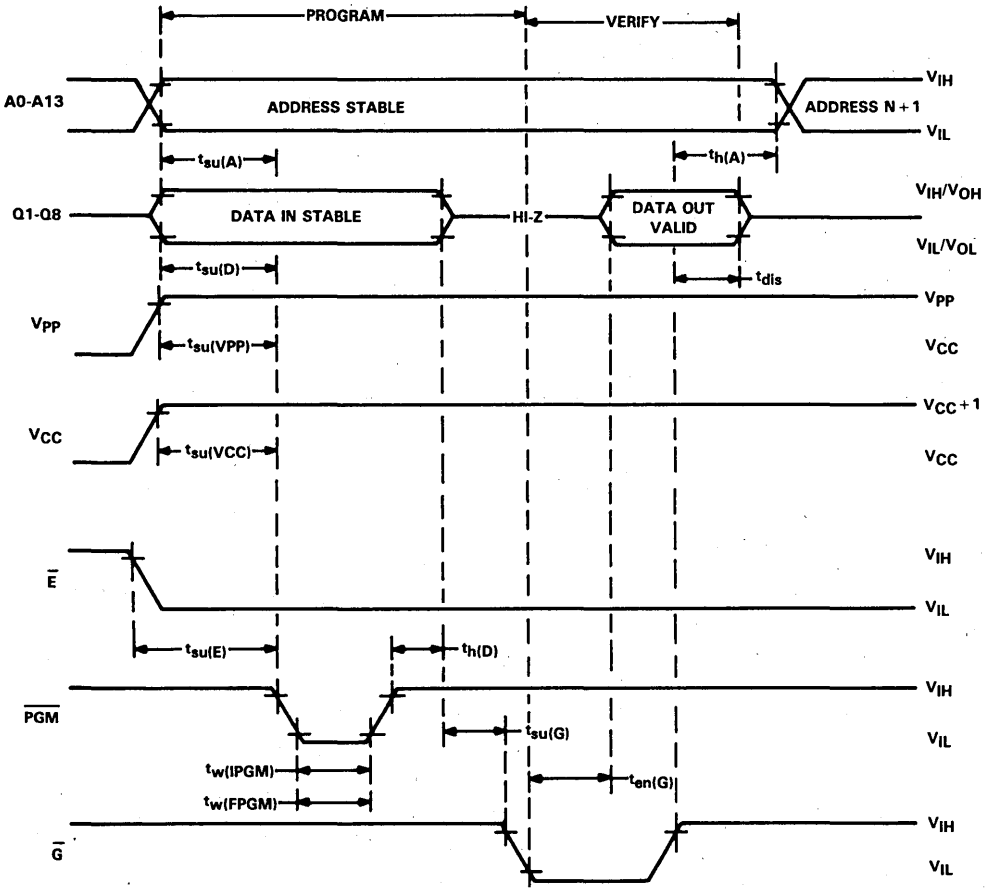


FIGURE 2. OUTPUT LOAD CIRCUIT

read cycle timing



program cycle timing



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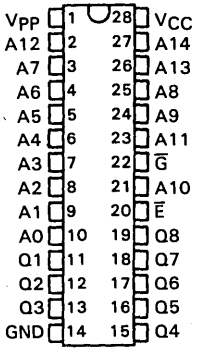
SEPTEMBER 1984 — REVISED NOVEMBER 1985

- Organization . . . 32K × 8
- Single 5-V Power Supply
- Pin Compatible with Existing 128K and 256K EPROMs
- All Inputs/Outputs Fully TTL Compatible
- Max Access/Min Cycle Time

'27C256-1,	'27C256-17	170 ns
'27C256-2,	'27C256-20	200 ns
'27C256,	'27C256-25	250 ns
'27C256-3,	'27C256-30	300 ns
'27C256-4,	'27C256-45	450 ns

- HVCMOS Technology
- 3-State Output Buffers
- 400 mV Guaranteed DC Noise Immunity with Standard TTL Loads
- Low Power Dissipation (V_{CC} = 5.25 V)
  —Active . . . 210 mW Worst Case
  —Standby . . . 1.4 mW Worst Case (CMOS-Input Levels)

J PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A14	Address Inputs
$\overline{E}$	Chip Enable/Power Down
$\overline{G}$	Output Enable
GND	Ground
Q1-Q8	Outputs
V_{CC}	5-V Power Supply
V_{PP}	12.5-V Power Supply

description

The TMS27C256 series are 262,144-bit, ultraviolet-light erasable, electrically programmable read-only memories. These devices are fabricated using HVCMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull-up resistors, and each output can drive one Series 74 TTL circuit without external resistors. The data outputs are three state for connecting multiple devices to a common bus. The TMS27C256 is pin compatible with existing 28-pin ROMs and EPROMs. It is offered in a dual-in-line ceramic package (J suffix) rated for operation from 0°C to 70°C.

Since these EPROMs operate from a single 5-V supply (in the read mode), they are ideal for use in microprocessor-based systems. One other (12.5 V) supply is needed for programming, but all programming signals are TTL level. For programming outside the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random.

operation

There are seven modes of operation for the TMS27C256 listed on the following page. Read mode requires a single 5-V supply. All inputs are TTL level except for V_{PP} during programming (12.5 V) and 12 V on A9 for signature mode.

FUNCTION (PINS)	MODE							
	Read	Output Disable	Standby	Programming	Verify	Program Inhibit	Signature Mode	
$\overline{E}$ (20)	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	
$\overline{G}$ (22)	V_{IL}	V_{IH}	X†	V_{IH}	V_{IL}	VIH	V_{IL}	
V_{PP} (1)	V_{CC}	V_{CC}	V_{CC}	V_{PP}	V_{PP}	V_{PP}	V_{CC}	
V_{CC} (28)	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A9 (24)	X	X	X	X	X	X	V_H‡	V_H‡
A0 (10)	X	X	X	X	X	X	V_{IL}	V_{IH}
Q1-Q8 (11-13, 15-19)	D_{OUT}	HI-Z	HI-Z	D_{IN}	D_{OUT}	HI-Z	CODE	
							MFG	DEVICE
							97	04

†X can be V_{IL} or V_{IH}.
‡V_H = 12 V ± 0.5 V.

read/output disable

When the outputs of two or more TMS27C256's are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. To read the output of the TMS27C256, a low-level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins. Output data is accessed at pins Q1 to Q8.

power down

Active I_{CC} current can be reduced from 40 mA to 500 μA (TTL-level inputs) or 250 μA (CMOS-level inputs) by applying a high TTL signal to the $\overline{E}$ pin. In this mode all outputs are in the high-impedance state.

erasure

Before programming, the TMS27C256 is erased by exposing the chip through the transparent lid to high intensity ultraviolet light (wavelength 2537 angstroms). The recommended minimum exposure dose (UV intensity × exposure time) is fifteen watt-seconds per square centimeter. A typical 12 milliwat per square centimeter, filterless UV lamp will erase the device in 21 minutes. The lamp should be located about 2.5 centimeters above the chip during erasure. After erasure, all bits are in the high state. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS27C256, the window should be covered with an opaque label.

fast programming

After erasure (all bits in logic '1' state), logic '0's are programmed into the desired locations. A programmed '0' can only be erased by ultraviolet light. Data is presented in parallel (eight bits) on pins Q1 to Q8. Once addresses and data are stable, $\overline{E}$ is pulsed. The programming mode is achieved when V_{PP} = 12.5 V, V_{CC} = 6.0 V, $\overline{G}$ = V_{IH}, and $\overline{E}$ = V_{IL}. More than one TMS27C256 can be programmed when the devices are connected in parallel. Locations can be programmed in any order.

Programming uses two types of programming pulses: Prime and Final. The length of the Prime pulse is 1 millisecond; this pulse is applied X times. After each Prime pulse, the byte being programmed is verified. If the correct data is read, the Final programming pulse is applied; if correct data is not read, an additional

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1 millisecond pulse is applied up to a maximum X of 25. The Final programming pulse is 3X long. This sequence of programming and verification is performed at V_{CC} = 6.0 V and V_{PP} = 12.5 V. When the full fast programming routine is complete, all bits are verified with V_{CC} = V_{PP} = 5 V (see Figure 1).

program inhibit

Programming may be inhibited by maintaining a high level input on the $\overline{E}$ pin.

program verify

Programmed bits may be verified with V_{PP} = 12.5 V when $\overline{G}$ = V_{IL}, and $\overline{E}$ = V_{IH}.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 (pin 24) is forced to 12 V ± 0.5 V. Two identifier bytes are accessed by A0 (pin 10) i.e., A0 = V_{IL} – manufacturer; A0 = V_{IH} – device. All other addresses must be held at V_{IL}. Each byte possesses odd parity on bit Q8. The manufacturer code for this device is 97, and the device code is 04.

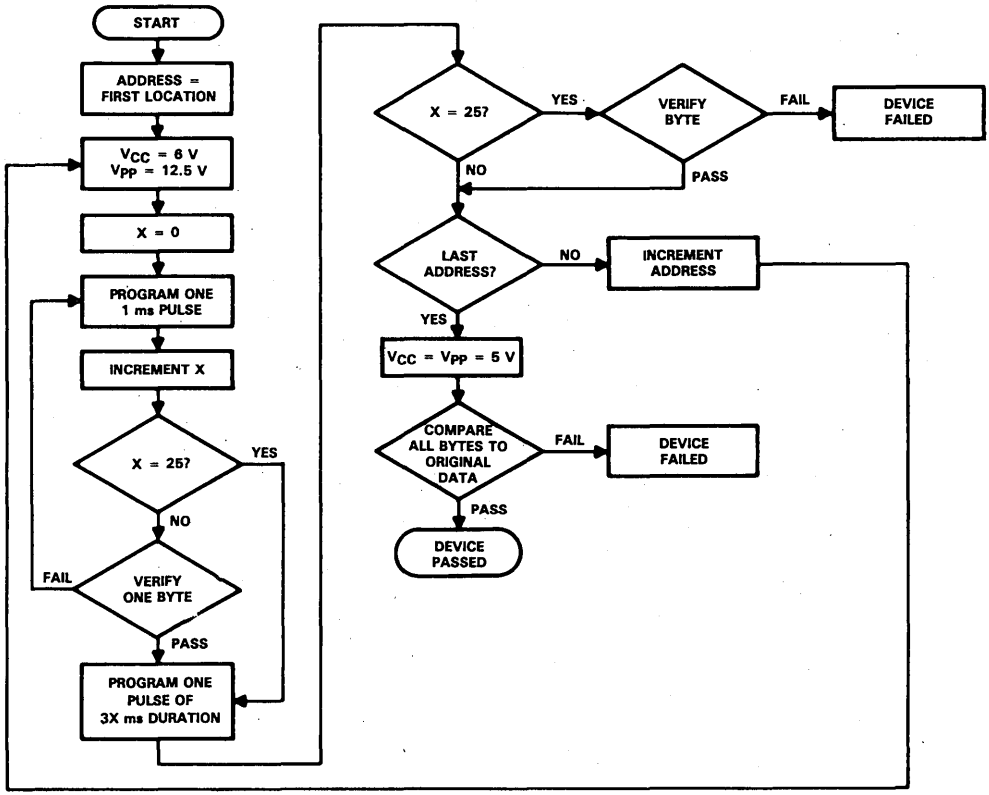
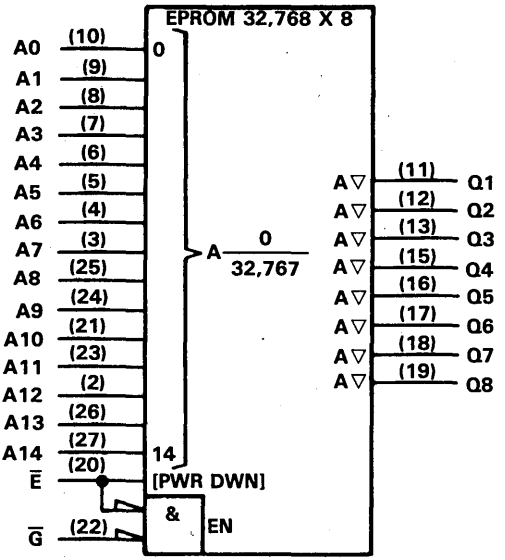


FIGURE 1. FAST PROGRAMMING FLOWCHART

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.6 V to 7 V
Supply voltage range, V_{PP} (see Note 1) . . . . . −0.6 V to 14 V
Input voltage range (see Note 1): All inputs except A9 . . . . . −0.6 V to 6.5 V
A9 . . . . . −0.6 V to 13.5 V
Output voltage range (see Note 1) . . . . . −0.6 V to V_{CC} + 1 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Under absolute maximum ratings, voltage values are with respect to GND.

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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recommended operating conditions

			TMS27C256-1, TMS27C256-2, TMS27C256, TMS27C256-3, TMS27C256-4			TMS27C256-17, TMS27C256-20, TMS27C256-25, TMS27C256-30, TMS27C256-45			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)		4.75	5	5.25	4.5	5	5.5	V
V_{PP}	Supply voltage (see Note 3)			V_{CC}			V_{CC}		V
V_{IH}	High-level input voltage	TTL	2		$V_{CC}+1$	2		$V_{CC}+1$	V
		CMOS	$V_{CC}-0.2$		$V_{CC}+0.2$	$V_{CC}-0.2$		$V_{CC}+0.2$	V
V_{IL}	Low-level input voltage	TTL	−0.5		0.8	−0.5		0.8	V
		CMOS	GND−0.2		GND+0.2	GND−0.2		GND+0.2	V
T_A	Operating free-air temperature		0		70	0		70	°C

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.

3. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be $I_{CC}+I_{PP}$. During programming, V_{PP} must be maintained at 12.5 V (±0.5 V).

electrical characteristics over full ranges of recommended operating conditions

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = −400 μA	2.4			V
V_{OL}	Low-level output voltage		I_{OL} = 2.1 mA			0.4	V
I_I	Input current (leakage)		V_I = 0 V to 5.5 V			±10	μA
I_O	Output current (leakage)		V_O = 0 V to V_{CC}			±10	μA
I_{PP1}	V_{PP} supply current		V_{PP} = V_{CC} = 5.5 V			100	μA
I_{PP2}	V_{PP} supply current (during program pulse)		V_{PP} = 13 V		35	50	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{IH}			500	μA
		CMOS-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{CC}			250	μA
I_{CC2}	V_{CC} supply current (active)		V_{CC} = 5.5 V, $\overline{E}$ = V_{IL}, t_{cycle} = minimum cycle time, outputs open		30	40	mA

†Typical values are at T_A = 25°C and nominal voltages.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz†

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
C_i	Input capacitance	V_I = 0 V, f = 1 MHz		6	9	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz		8	12	pF

†Capacitance measurements are made on sample basis only.
‡Typical values are at T_A = 25°C and nominal voltages.

switching characteristics over full ranges of recommended operating conditions (see Note 4)

PARAMETER		TEST CONDITIONS (SEE NOTES 4 AND 5)	'27C256-1 '27C256-17		'27C256-2 '27C256-20		'27C256 '27C256-25		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL Load, Input $t_r \leq$ 20 ns, Input $t_f \leq$ 20 ns		170		200		250	ns
$t_{a(E)}$	Access time from chip enable			170		200		250	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			75		75		100	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first†		0	60	0	60	0	60	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first†		0		0		0		ns

PARAMETER		TEST CONDITIONS (SEE NOTES 4 AND 5)	'27C256-3 '27C256-30		'27C256-4 '27C256-45		UNIT
			MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL Load, Input $t_r \leq$ 20 ns, Input $t_f \leq$ 20 ns		300		450	ns
$t_{a(E)}$	Access time from chip enable			300		450	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			120		150	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first†		0	105	0	130	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first†		0		0		ns

†Value calculated from 0.5 V delta to measured output level. This parameter is only sampled and not 100% tested.

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recommended timing requirements for programming, T_A = 25°C, V_{CC} = 6 V, V_{PP} = 12.5 V (see Note 4)

		MIN	NOM	MAX	UNIT
$t_{w(IPGM)}$	Initial program pulse duration	0.95	1	1.05	ms
$t_{w(FPGM)}$	Final pulse duration	2.85		78.75	ms
$t_{su(A)}$	Address setup time	2			μs
$t_{su(G)}$	$\overline{G}$ setup time	2			μs
$t_{dis(G)}$	Output disable time from $\overline{G}$	0		130	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			150	ns
$t_{su(D)}$	Data setup time	2			μs
$t_{su(VPP)}$	V_{PP} setup time	2			μs
$t_{su(VCC)}$	V_{CC} setup time	2			μs
$t_{h(A)}$	Address hold time	0			μs
$t_{h(D)}$	Data hold time	2			μs

NOTES: 4. For all switching characteristics and timing measurements, input pulse levels are 0.40 V to 2.4 V and V_{PP} = 12.5 V ±0.5 V during programming.
5. Common test conditions apply for $t_{dis(G)}$ except during programming.

PARAMETER MEASUREMENT INFORMATION

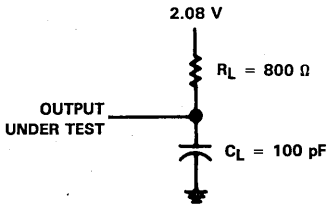
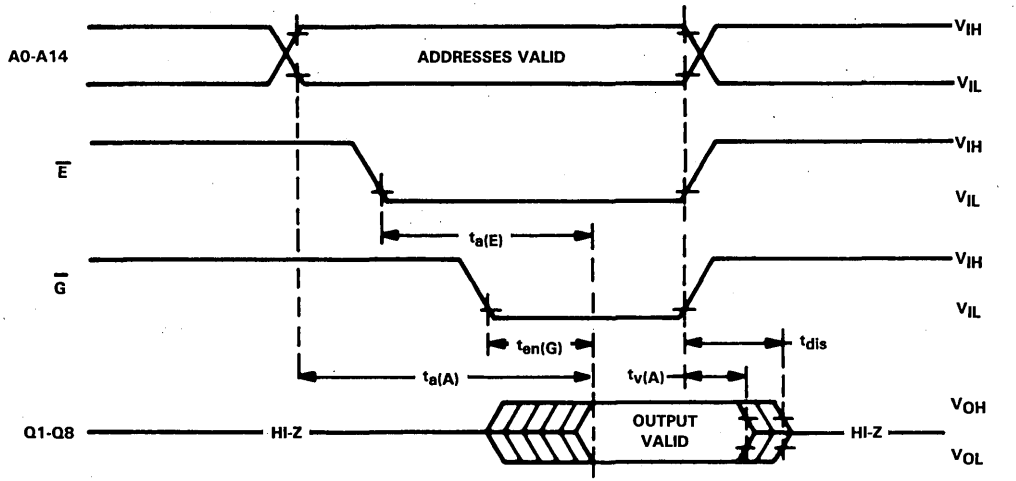
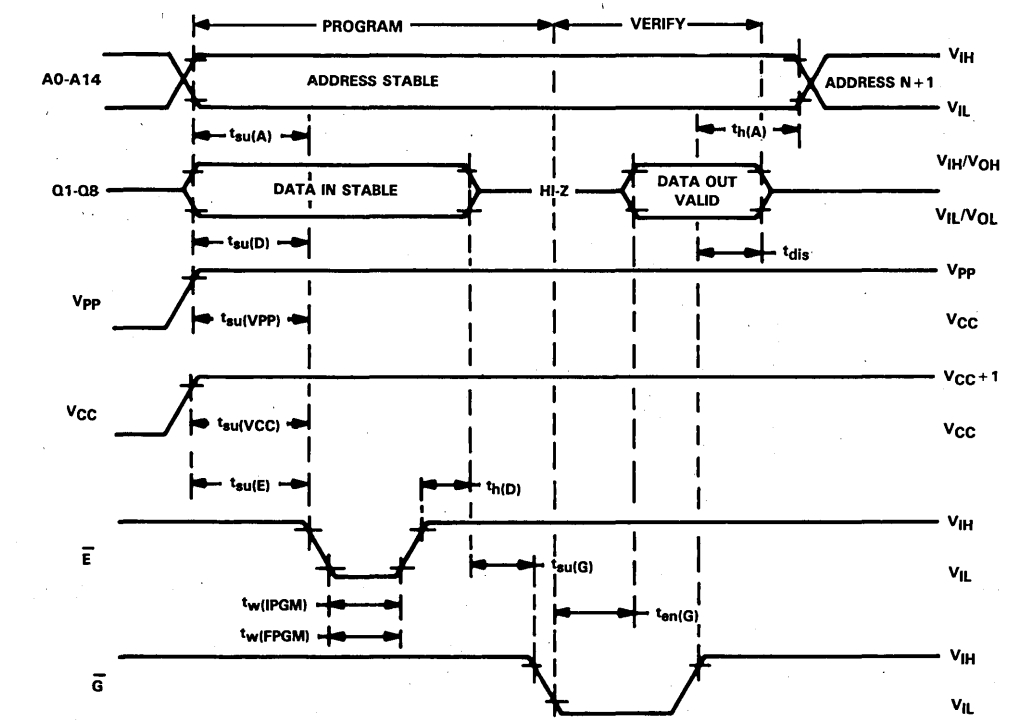


FIGURE 2. OUTPUT LOAD CIRCUIT

read cycle timing



program cycle timing



TEXAS INSTRUMENTS
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TMX27C512
524,288-BIT ERASABLE PROGRAMMABLE READ-ONLY MEMORY

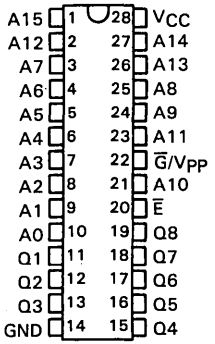
NOVEMBER 1985

- Organization . . . 64K × 8
- Single 5-V Power Supply
- Pin Compatible with Existing 512K EPROMs
- All Inputs/Outputs Fully TTL Compatible
- Max Access/Min Cycle Time

'27C512-2,	'27C512-20	200 ns
'27C512,	'27C512-25	250 ns
'27C512-3,	'27C512-30	300 ns
'27C512-4,	'27C512-45	450 ns

- HVCMOS Technology
- 3-State Output Buffers
- 400 mV Guaranteed DC Noise Immunity with Standard TTL Loads
- Low Power Dissipation (V_{CC} = 5.25 V)
  - —Active . . . 263 mW Worst Case
  - —Standby . . . 1.4 mW Worst Case (CMOS-Input Levels)

J PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A15	Address Inputs
$\overline{E}$	Chip Enable/Power Down
GND	Ground
Q1-Q8	Outputs
V_{CC}	5-V Power Supply
$\overline{G}/V_{PP}$	12.5-V Power Supply/ Output Enable

description

The TMX27C512 series are 524,288-bit, ultraviolet-light erasable, electrically programmable read-only memories. These devices are fabricated using HVCMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull-up resistors, and each output can drive one Series 74 TTL circuit without external resistors. The data outputs are three state for connecting multiple devices to a common bus. The TMX27C512 is pin compatible with existing 28-pin ROMs and EPROMs. It is offered in a dual-in-line ceramic package (J suffix) rated for operation from 0°C to 70°C.

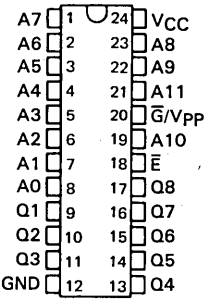
Since these EPROMs operate from a single 5-V supply (in the read mode), they are ideal for use in microprocessor-based systems. One other (12.5 V) supply is needed for programming, but all programming signals are TTL level. For programming outside the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random.

TMS27P32A
32,768-BIT PROGRAMMABLE READ-ONLY MEMORY

NOVEMBER 1985

- **Organization . . . 4096 X 8**
- **Single 5-V Power Supply**
- **All Inputs and Outputs Are TTL Compatible**
- **Max Access/Min Cycle Time**
  TMS27P32A-25 250 ns
  TMS27P32A-30 300 ns
  TMS27P32A-45 450 ns
- **Low Standby Power Dissipation . . . 158 mW (Maximum)**
- **JEDEC Approved Pinout . . . Industry Standard**
- **21-V Power Supply Required for Programming**
- **N-Channel Silicon-Gate Technology**

N PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A11	Address Inputs
$\overline{E}$	Chip Enable
$\overline{G}/V_{PP}$	Output Enable/21 V
GND	Ground
Q1-Q8	Outputs
V_{CC}	5-V Power Supply

description

The TMS27P32A is a one-time, electrically programmable read-only memory. It has 32,768 bits organized as 4,096 words of 8-bit length. The TMS27P32A only requires a single 5-volt power supply with a tolerance of ±5%.

The TMS27P32A provides two output control lines: Output Enable ($\overline{G}$) and Chip Enable ($\overline{E}$). This feature allows the $\overline{G}$ control line to eliminate bus contention in multibus microprocessor systems. The TMS27P32A has a power-down mode that reduces maximum power dissipation from 657 mW to 158 mW when the device is placed on standby.

This PROM is supplied in a 24-pin dual-in-line plastic package and is designed for operation from 0°C to 70°C.

operation

The six modes of operation for the TMS27P32A are listed in the following table.

FUNCTION (PINS)	MODE					
	Read	Deselect	Power Down (Standby)	Program	Program Verification	Inhibit Programming
$\overline{E}$ (18)	V_{IL}	X	V_{IH}	V_{IL}	V_{IL}	V_{IH}
$\overline{G}/V_{PP}$ (20)	V_{IL}	V_{IH}	X	21 V	V_{IL}	21 V
V_{CC} (24)	5 V	5 V	5 V	5 V	5 V	5 V
Q1-Q8 (9 to 11, 13 to 17)	Q	HI-Z	HI-Z	D	Q	HI-Z

X = V_{IH} or V_{IL}

read

The two control pins ($\overline{E}$ and $\overline{G}$/Vpp) must have low-level TTL signals in order to provide data at the outputs. Chip enable ($\overline{E}$) should be used for device selection. Output enable ($\overline{G}$/Vpp) should be used to gate data to the output pins.

power down

The power-down mode reduces the maximum power dissipation from 657 mW to 158 mW. A TTL high-level signal applied to $\overline{E}$ selects the power-down mode. In this mode, the outputs assume a high-impedance state, independent of $\overline{G}$/Vpp.

program

The programming procedure for the TMS27P32A is the same as that for the TMS2732A.

The program mode consists of the following sequence of events. With the level on $\overline{G}$/Vpp equal to 21 V, data to be programmed is applied in parallel to output pins Q8-Q1. The location to be programmed is addressed. Once data and addresses are stable, a 10-millisecond TTL low-level pulse is applied to $\overline{E}$. The maximum width of this pulse is 11 milliseconds. The programming pulse must be applied at each location that is to be programmed. Locations may be programmed in any order.

Several TMS27P32As can be programmed simultaneously by connecting them in parallel and following the programming sequence previously described.

program verify

After the PROM has been programmed, the programmed bits should be verified. To verify bit states, $\overline{G}$/Vpp and $\overline{E}$ are set to V_{IL}.

program inhibit

The program inhibit is useful when programming multiple TMS27P32As connected in parallel with different data. Program inhibit can be implemented by applying a high-level signal to $\overline{E}$ of the device that is not to be programmed.

TEXAS INSTRUMENTS
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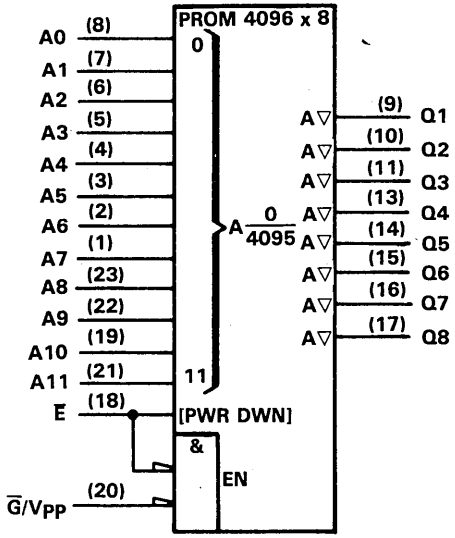
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . −0.3 V to 7 V
Supply voltage range, V_{PP} . . . . . −0.3 V to 22 V
Input voltage range (except program) . . . . . −0.3 V to 7 V
Output voltage range . . . . . −0.3 V to 7 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 125°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (see Note 1)	4.75	5	5.25	V
V_{PP}	Supply voltage (see Note 2)		V_{CC}		V
V_{IH}	High-level input voltage	2		$V_{CC}+1$	V
V_{IL}	Low-level input voltage	−0.1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTES: 1. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.
2. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be I_{CC} + I_{PP}. During programming, V_{PP} must be maintained at 21 V (±0.5 V).

electrical characteristics over full ranges of recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −400 μA	2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 2.1 mA		0.45	V
I_I	Input current (leakage)	V_I = 0 V to 5.25 V		±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.25 V		±10	μA
I_{CC1}	V_{CC} supply current (standby)	$\overline{E}$ at V_{IH}, $\overline{G}$ at V_{IL}		30	mA
I_{CC2}	V_{CC} supply current (active)	$\overline{E}$ and $\overline{G}$ at V_{IL}		125	mA

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz†

PARAMETER			TEST CONDITIONS	TYP‡	MAX	UNIT
C_i	Input capacitance	All except $\overline{G}/V_{PP}$	V_I = 0 V	4	6	pF
		$\overline{G}/V_{PP}$			20	
C_o	Output capacitance		V_O = 0 V	8	12	pF

†Capacitance measurements are made on a sample basis only.
‡Typical values are at T_A = 25°C and nominal voltages.

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS (SEE NOTE 3)	TMS27P32A-25		TMS27P32A-30		TMS27P32A-45		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL Load, $t_r \leq 20$ ns, $t_f \leq 20$ ns, See Figure 1		250		300		450	ns
$t_{a(E)}$	Access time from $\overline{E}$			250		300		450	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			100		150		150	ns
t_{dis}†	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first		0	85	0	105	0	130	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first		0		0		0		ns

NOTE 3: The timing reference levels for inputs and outputs are 0.8 V and 2 V. Input pulse levels are 0.40 V and 2.4 V.
†Value calculated from 0.5 V delta to measured output level. This parameter is only sampled and not 100% tested.

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

recommended conditions for programming, T_A = 25°C (see Note 4)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{PP}	Supply voltage	20.5	21	21.5	V
V_{IH}	High-level input voltage	2		$V_{CC}+1$	V
V_{IL}	Low-level input voltage	−0.1		0.8	V
$t_{w(E)}$	$\overline{E}$ pulse duration	9	10	11	ms
$t_{su(A)}$	Address setup time	2			μs
$t_{su(D)}$	Data setup time	2			μs
$t_{su(VPP)}$	V_{PP} setup time	2			μs
$t_{h(A)}$	Address hold time	0			μs
$t_{h(D)}$	Data hold time	2			μs
$t_{h(VPP)}$	V_{PP} hold time	2			μs
$t_{rec(PG)}$	V_{PP} recovery time	2			μs
$t_{r(PG)G}$	$\overline{G}$ rise time during programming	50			ns
t_{EHD}	Delay time, data valid after $\overline{E}$ low			1	μs

NOTE 4: When programming the TMS27P32A, connect a 0.1 μF capacitor between V_{PP} and GND to suppress spurious voltage transients which may damage the device.

programming characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage		2		$V_{CC}+1$	V
V_{IL}	Low-level input voltage		−0.1		0.8	V
V_{OH}	High-level output voltage (verify)	I_{OH} = −400 μA	2.4			V
V_{OL}	Low-level output voltage (verify)	I_{OL} = 2.1 mA			0.45	V
I_I	Input current (all inputs)	$V_I = V_{IL}$ or V_{IH}			10	μA
I_{PP}	Supply current	$\overline{E} = V_{IL}$, $\overline{G} = V_{PP}$			50	mA
I_{CC}	Supply current				125	mA
$t_{dis(PR)}$	Output disable time		0		130	ns

PARAMETER MEASUREMENT INFORMATION

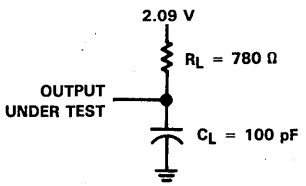
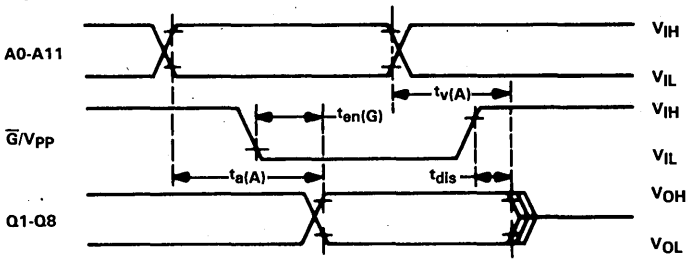
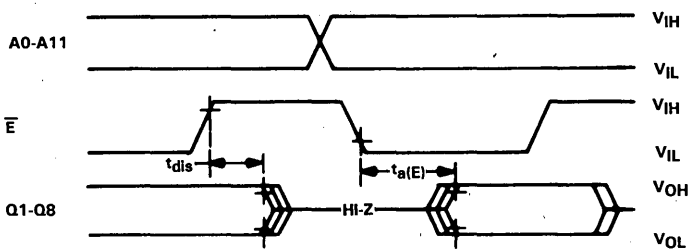


FIGURE 1. TYPICAL OUTPUT LOAD CIRCUIT

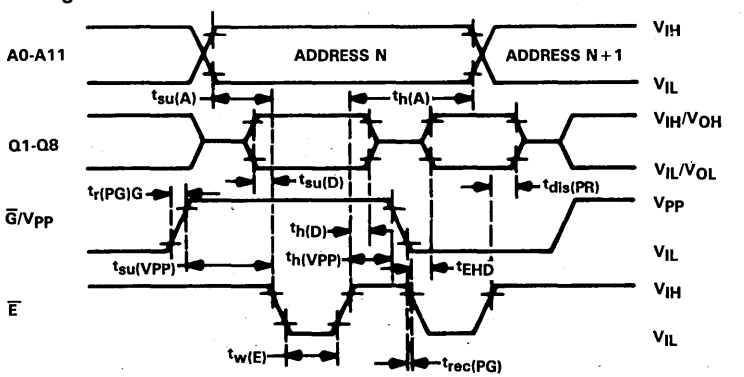
read cycle timing



standby mode



program cycle timing



TEXAS INSTRUMENTS
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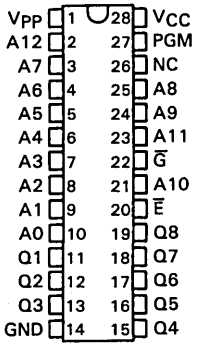
TMS27P64
65,536-BIT PROGRAMMABLE READ-ONLY MEMORY

NOVEMBER 1985

- Organization . . . 8192 X 8
- Single 5-V Power Supply
- Pin Compatible with TMS2732A and TMS2764 EPROMs
- All Inputs and Outputs Are TTL Compatible
- Max Access/Min Cycle Time
  TMS27P64-25 250 ns
  TMS27P64-30 300 ns
  TMS27P64-45 450 ns
- Low Standby Power Dissipation . . . 184 mW (MAX)
- JEDEC Approved Pinout
- 21-V Power Supply Required for Programming
- Fast Programming Algorithm
- N-Channel Silicon-Gate Technology

N PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A12	Address Inputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
GND	Ground
NC	No Connection
$\overline{PGM}$	Program
Q1-Q8	Outputs
V_{CC}	5-V Power Supply
V_{PP}	21-V Power Supply

description

The TMS27P64 is a one-time, electrically programmable read-only memory. It has 65,536 bits organized as 8,192 words of 8-bit length. The TMS27P64-25 only requires a single 5-volt power supply with a tolerance of ±5%, and has a maximum access time of 250 ns.

The TMS27P64 provides two output control lines: Output Enable ($\overline{G}$) and Chip Enable ($\overline{E}$). This feature allows the $\overline{G}$ control line to eliminate bus contention in microprocessor systems. The TMS27P64 has a power-down mode that reduces maximum active current from 150 mA to 35 mA when the device is placed on standby.

This PROM is supplied in a 28-pin, 15,24-mm (600-mil) dual-in-line plastic package and is designed for operation from 0°C to 70°C.

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operation

The six modes of operation for the TMS27P64 are listed in the following table.

FUNCTION (PINS)	MODE					
	Read	Output Disable	Power Down (Standby)	Fast Programming	Program Verification	Inhibit Programming
$\overline{E}$ (20)	V_{IL}	X	V_{IH}	V_{IL}	V_{IL}	V_{IH}
$\overline{G}$ (22)	V_{IL}	V_{IH}	X	V_{IH}	V_{IL}	X
$\overline{PGM}$ (27)	V_{IH}	V_{IH}	X	V_{IL}	V_{IH}	X
V_{PP} (1)	V_{CC}	V_{CC}	V_{CC}	V_{PP}	V_{PP}	V_{PP} or V_{CC}
V_{CC} (28)	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
Q1-Q8 (11 to 13, 15 to 19)	Q	HI-Z	HI-Z	D	Q	HI-Z

X = V_{IL} or V_{IH}

read

The dual control pins ($\overline{E}$ and $\overline{G}$) must have low-level TTL signals in order to provide data at the outputs. Chip enable ($\overline{E}$) should be used for device selection. Output enable ($\overline{G}$) should be used to gate data to the output pins.

power down

The power-down mode reduces the maximum active current from 150 mA to 35 mA. A TTL high-level signal applied to $\overline{E}$ selects the power-down mode. In this mode, the outputs assume a high-impedance state, independent of $\overline{G}$.

fast programming

Note that the application of a voltage in excess of 22 V to V_{PP} may damage the TMS27P64.

Initially all locations are logic "1's," logic "0's" are programmed into the desired locations. Programming consists of the following sequence of events. With the level on V_{PP} equal to 21 V and $\overline{E}$ at TTL low, data to be programmed is applied in parallel to output pins Q8-Q1. The location to be programmed is addressed. Once data and addresses are stable, a TTL low-level pulse is applied to $\overline{PGM}$. Programming pulses must be applied at each location that is to be programmed. Locations may be programmed in any order.

Programming uses two types of programming pulse: Prime and Final. The length of the Prime pulse is 1 millisecond; this pulse is applied X times. After each application the byte being programmed is verified. If the correct data is read, the Final programming pulse is then applied, if correct data is not read, a further 1 millisecond programming pulse is applied up to a maximum X of 15. The Final programming pulse is 4X milliseconds long. This sequence of programming pulses and byte verification is done at V_{CC} = 6.0 V and V_{PP} = 21.0 V. When the full fast programming routine is complete, all bits are verified with V_{CC} = V_{PP} = 5 V. A flowchart of the fast programming routine is shown in Figure 1.

multiple device programming

Several TMS27P64's can be programmed simultaneously by connecting them in parallel and following the programming sequence previously described.

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program inhibit

The program inhibit is useful when programming multiple TMS27P64's connected in parallel with different data. Program inhibit can be implemented by applying a high-level signal to $\overline{E}$ or $\overline{PGM}$ of the device that is not to be programmed.

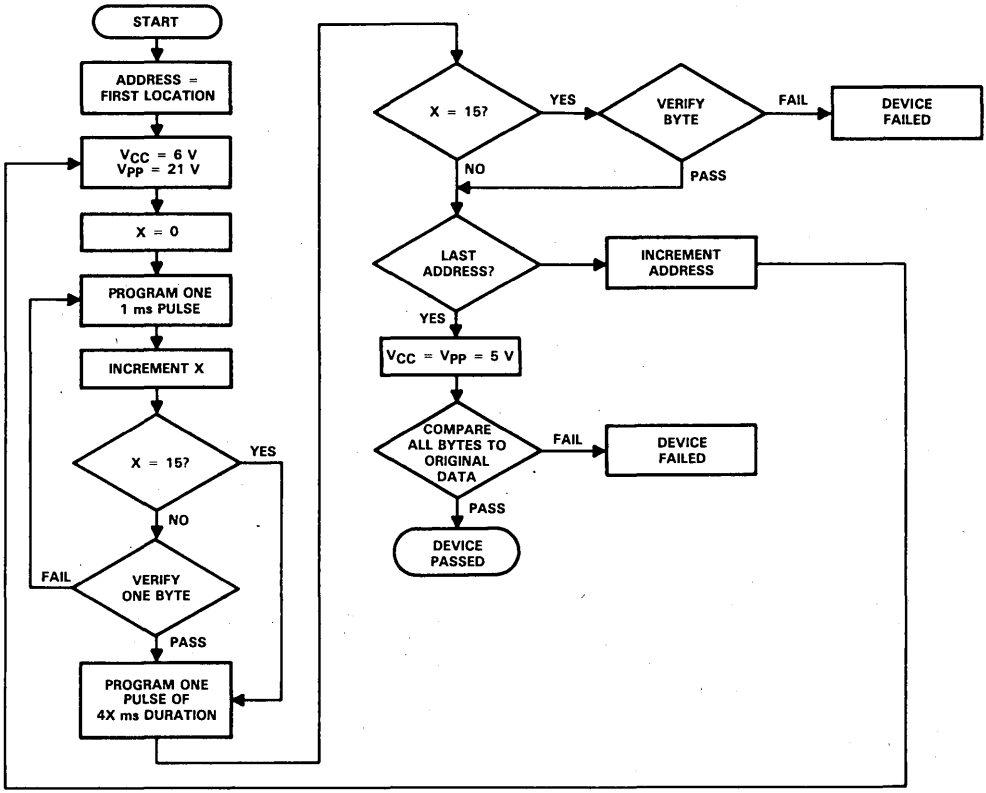
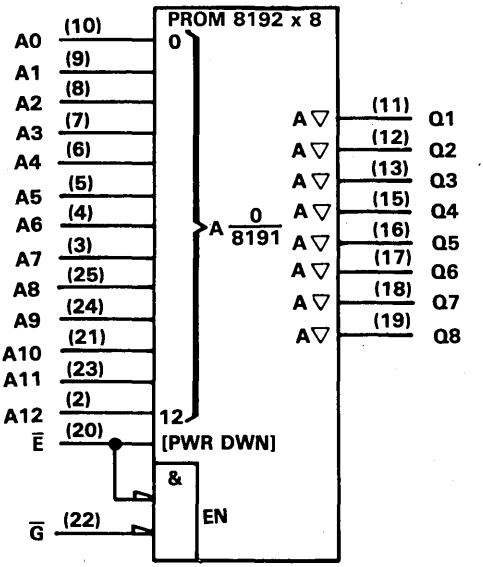


FIGURE 1. FAST PROGRAMMING FLOWCHART

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . −0.6 V to 7 V
Supply voltage range, V_{PP} . . . . . −0.6 V to 22 V
Input voltage range . . . . . −0.6 V to 7 V
Output voltage range . . . . . −0.6 V to 7 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 125°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{PP}	Supply voltage		VCC		V
V_{IH}	High-level input voltage	2		$V_{CC}+1$	V
V_{IL}	Low-level input voltage (see Note 1)	−0.1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 1: The algebraic convention, where the more negative (less positive) limit is designated as minimum is used in this data sheet for logic voltage levels only.

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electrical characteristics over full ranges of recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −400 μA	2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 2.1 mA		0.45	V
I_I	Input current (load)	V_I = 0 V to 5.25 V		±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.25 V		±10	μA
I_{PP1}	V_{PP} supply current (read)	V_{PP} = 5.25 V		15	mA
I_{PP2}	V_{PP} supply current (program)	$\overline{E}$ and $\overline{PGM}$ at V_{IL}		50	mA
I_{CC1}	V_{CC} supply current (standby)	$\overline{E}$ at V_{IH}		35	mA
I_{CC2}	V_{CC} supply current (active)	$\overline{E}$ and $\overline{G}$ at V_{IL}		150	mA

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz†

PARAMETER		TEST CONDITIONS	TYP‡	MAX	UNIT
C_i	Input capacitance	V_I = 0 V	4	6	pF
C_o	Output capacitance	V_O = 0 V	8	12	pF

†Capacitance measurements are made on a sample basis only.
‡Typical values are at T_A = 25°C and nominal voltages.

switching characteristics over recommended supply voltage range and operating free-air temperature range, C_L = 100 pF, 1 Series 74 TTL load (see Note 2 and Figure 2)

PARAMETER		TMS27P64-25		TMS27P64-30		TMS27P64-45		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address		250		300		450	ns
$t_{a(E)}$	Access time from $\overline{E}$		250		300		450	ns
$t_{en(G)}$	Output enable time from $\overline{G}$		100		120		150	ns
$t_{dis(G)}$‡	Output disable time from $\overline{G}$	0	85	0	105	0	130	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first	0		0		0		ns

NOTE 2: For all switching characteristics and timing measurements, input pulse levels are 0.40 V and 2.4 V. Input and output timing reference levels are 0.8 V and 2 V.
‡Value claculated from 0.5 volt delta to measured output level; $t_{dis(G)}$ is specified from $\overline{G}$ or $\overline{E}$, whichever occurs first. Refer to read cycle timing diagram. This parameter is only sampled and is not 100% tested.

recommended conditions for fast programming routine, T_A = 25°C (see Note 2 and fast programming cycle timing diagram)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (see Note 3)	5.75	6	6.25	V
V_{PP}	Supply voltage (see Note 4)	20.5	21	21.5	V
$t_{w(IPGM)}$	$\overline{PGM}$ initial program pulse duration (see Note 5)	0.95	1	1.05	ms
$t_{w(FPGM)}$	$\overline{PGM}$ final pulse duration (see Note 6)	3.8		63	ms
$t_{su(A)}$	Address setup time	2			μs
$t_{su(D)}$	Data setup time	2			μs
$t_{su(VPP)}$	V_{PP} setup time	2			μs
$t_{su(VCC)}$	V_{CC} setup time	2			μs
$t_{h(A)}$	Address hold time	0			μs
$t_{h(D)}$	Data hold time	2			μs
$t_{su(E)}$	$\overline{E}$ setup time	2			μs
$t_{su(G)}$	$\overline{G}$ setup time	2			μs

fast programming characteristics, T_A = 25°C (see Note 2 and fast programming cycle timing diagram)

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
$t_{dis(G)FP}$	Output disable time from $\overline{G}$ (see Note 7)	C_L = 100 pF	0	130	ns
$t_{en(G)FP}$	Output enable time from $\overline{G}$	1 Series 74 TTL load		150	

NOTES: 2. For all switching characteristics and timing measurements, input pulse levels are 0.40 V and 2.4 V. Input and output timing reference levels are 0.8 V and 2 V.
3. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
4. When programming the TMS27P64, connect a 0.1 μF capacitor between V_{PP} and GND to suppress spurious voltage transients which may damage the device.
5. The Initial program pulse duration tolerance is 1 ms ± 5%.
6. The length of the Final pulse will vary from 3.8 ms to 63 ms depending on the number of Initial pulse applications (X).
7. This parameter is only sampled and is not 100% tested.

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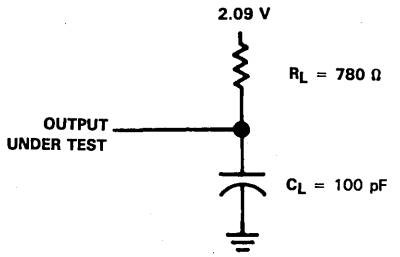
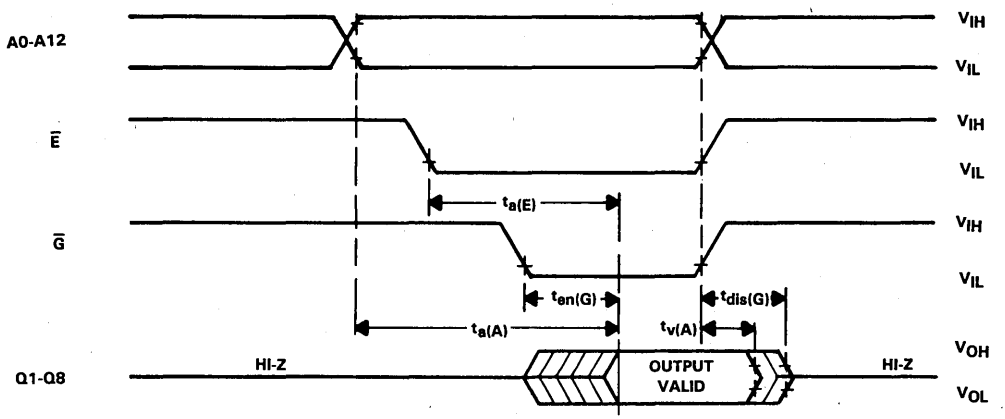
PARAMETER MEASUREMENT INFORMATION



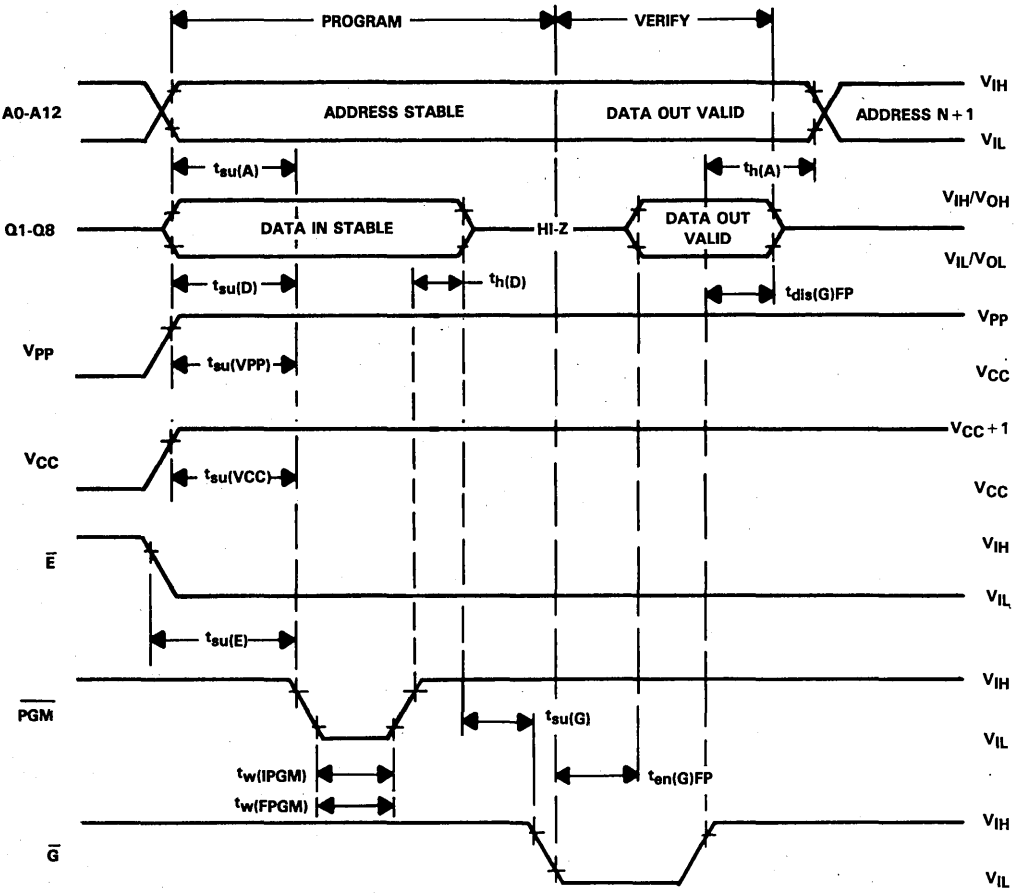
NOTE 8: $t_f \leq 20$ ns and $t_r \leq 20$ ns.

FIGURE 2. TYPICAL OUTPUT LOAD CIRCUIT

read cycle timing



fast program cycle timing



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TMX27PC128
131,072-BIT PROGRAMMABLE READ-ONLY MEMORY

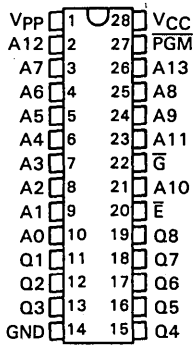
NOVEMBER 1985

- Organization . . . 16K × 8
- Single 5-V Power Supply
- Pin Compatible with Existing 64K and 128K EPROMs
- All Inputs/Outputs Fully TTL Compatible
- Max Access/Min Cycle Time

'27PC128-2,	'27PC128-20	200 ns
'27PC128,	'27PC128-25	250 ns
'27PC128-3,	'27PC128-30	300 ns
'27PC128-4,	'27PC128-45	450 ns

- HVCMOS Technology
- 3-State Output Buffers
- 400 mV Guaranteed DC Noise Immunity with Standard TTL Loads
- Low Power Dissipation (V_{CC} = 5.25 V)
  —Active . . . 210 mW Worst Case
  —Standby . . . 1.4 mW Worst Case (CMOS-Input Levels)

N PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A13	Address Inputs
$\overline{E}$	Chip Enable/Power Down
$\overline{G}$	Output Enable
GND	Ground
$\overline{PGM}$	Program
Q1-Q8	Outputs
V_{CC}	5-V Power Supply
V_{PP}	12.5-V Power Supply

description

The TMX27PC128 series are 131,072-bit, one-time, electrically programmable read-only memories. These devices are fabricated using HVCMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull-up resistors, and each output can drive one Series 74 TTL circuit without external resistors. The data outputs are three state for connecting multiple devices to a common bus. The TMX27PC128 is pin compatible with existing 28-pin ROMs and EPROMs. It is offered in a dual-in-line plastic package (N suffix) rated for operation from 0°C to 70°C.

Since these PROMs operate from a single 5-V supply (in the read mode), they are ideal for use in microprocessor-based systems. One other (12.5 V) supply is needed for programming, but all programming signals are TTL level. For programming outside the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random.

TEXAS INSTRUMENTS
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TMX27PC256
262,144-BIT PROGRAMMABLE READ-ONLY MEMORY

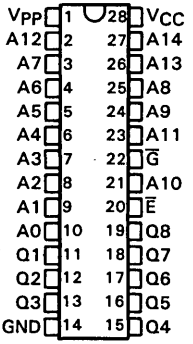
NOVEMBER 1985

- Organization . . . 32K × 8
- Single 5-V Power Supply
- Pin Compatible with Existing 64K, 128K and 256K EPROMs
- All Inputs/Outputs Fully TTL Compatible
- Max Access/Min Cycle Time

'27PC256-2,	'27PC256-20	200 ns
'27PC256,	'27PC256-25	250 ns
'27PC256-3,	'27PC256-30	300 ns
'27PC256-4,	'27PC256-45	450 ns

- HVCMOS Technology
- 3-State Output Buffers
- 400 mV Guaranteed DC Noise Immunity with Standard TTL Loads
- Low Power Dissipation (V_{CC} = 5.25 V)
  - —Active . . . 210 mW Worst Case
  - —Standby . . . 1.4 mW Worst Case (CMOS-Input Levels)

N PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A14	Address Inputs
$\overline{E}$	Chip Enable/Power Down
$\overline{G}$	Output Enable
GND	Ground
Q1-Q8	Outputs
V_{CC}	5-V Power Supply
V_{PP}	12.5-V Power Supply

description

The TMX27PC256 series are 262,144-bit, one-time, electrically programmable read-only memories. These devices are fabricated using HVCMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull-up resistors, and each output can drive one Series 74 TTL circuit without external resistors. The data outputs are three state for connecting multiple devices to a common bus. The TMX27PC256 is pin compatible with existing 28-pin ROMs and EPROMs. It is offered in a dual-in-line plastic package (N suffix) rated for operation from 0°C to 70°C.

Since these PROMs operate from a single 5-V supply (in the read mode), they are ideal for use in microprocessor-based systems. One other (12.5 V) supply is needed for programming, but all programming signals are TTL level. For programming outside the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random.

ATTENTION

These devices contain circuits to protect the inputs and outputs against damage due to high static voltages or electrostatic fields; however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits.

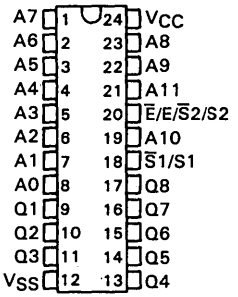
Unused inputs must always be connected to an appropriate logic voltage level, preferably either supply voltage or ground.

Additional information concerning the handling of ESD sensitive devices is provided in Section 12 in a document entitled *"Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies."*

SEPTEMBER 1984 — REVISED NOVEMBER 1985

- 4096 X 8 Organization
- All Inputs and Outputs TTL Compatible
- Fully Static (No Clocks, No Refresh)
- Single 5-V Power Supply
- Maximum Access Time from Address
  TMS2332-15 150 ns
  TMS2332-20 200 ns
  TMS2332-25 250 ns
- Pin Compatible with 2732A EPROM
- Optional Power Down or Chip Select
- Two Output-Enable Controls for Chip Select Flexibility
- Worst Case Active Power Dissipation . . . 330 mW
- Worst Case Standby Power Dissipation . . . 82.5 mW

N PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A11	Address Inputs
Ē/E/S̄2/S2	Chip Enable/Power Down or Chip Select
Q1-Q8	Data Out
S̄1/S1	Chip Select
V_{CC}	5-V Supply
V_{SS}	Ground

description

The TMS2332 is a 32,768-bit read-only memory organized as 4,096 words of 8-bit length. This makes the TMS2332 ideal for microprocessor-based systems. The device is fabricated using N-channel self-aligned silicon-gate technology for high speed and simple interface with bipolar and CMOS circuits.

The TMS2332 is fully compatible with Series 74, 74S, or 74LS TTL and CMOS logic. The data outputs are three state for OR-tying multiple devices on a common bus. Pins 18 and 20 are mask programmable, providing additional system flexibility. The data at the outputs is always available during a read cycle. It is not dependent on external clocking of pins 18 and 20.

This ROM is supplied in a 24-pin dual-in-line plastic (N suffix) package designed for insertion in mounting-hole rows on 15,24-mm (600-mil) centers. The device is designed for operation from 0°C to 70°C.

operation

address (A0-A11)

The address-valid interval determines the device cycle time. The 12-bit positive-logic address is decoded on chip to select one of 4096 words of 8-bit length in the memory array. A0 is the least-significant bit and A11 is the most-significant bit of the word address.

chip selects (S̄1 or S1 and S̄2 or S2)

Each of these pins can be programmed during mask fabrication to be active with either a high- or a low-level input. When both signals are active, all eight outputs are enabled and the eight-bit addressed word can be read. When either signal is not active, all eight outputs are in a high-impedance state.

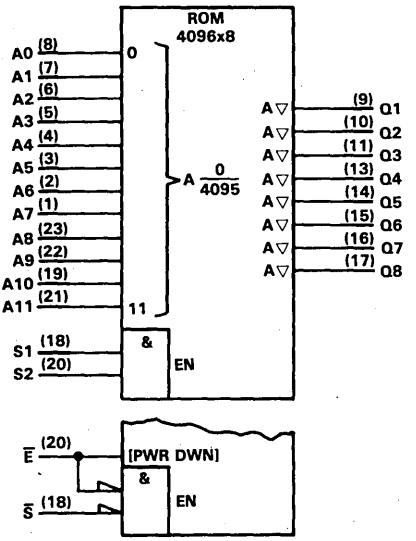
chip enable/power down ($\overline{E}$ or E) or chip select ($\overline{S}2$ or S2)

Pin 20 can be programmed during mask fabrication to be a chip-enable/power-down pin ($\overline{E}$ or E) or a secondary chip-select pin ($\overline{S}2$ or S2). Each option can be active high or active low. When the chip-enable/power-down pin is inactive, the chip is put into the standby mode. This reduces I_{CC1}, which in the active state is 60 mA, to a standby I_{CC2} of 15 mA. When pin 20 is programmed as a chip-select pin, it is functionally identical to pin 18.

data out (Q1-Q8)

The eight outputs must be enabled by pins 18 and 20 before the output word can be read. Data will remain valid until the address is changed or the outputs are disabled (chip deselected). When disabled, the three-state outputs are in a high-impedance state. Q1 is considered the least-significant bit, Q8 the most-significant bit.

logic symbol†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pins 18 and 20 can be active high as shown in the upper symbol or active low as shown in the lower (partial) symbol. In addition, pin 20 can be either a second chip-select ($\overline{S}2$ or S2) or a chip-enable/power-down ($\overline{E}$ or E) pin.

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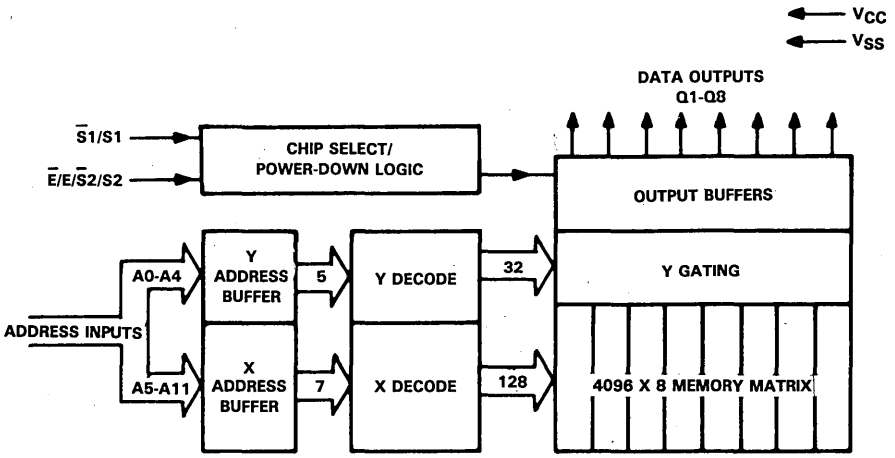
functional block diagram



absolute maximum ratings

Supply voltage range (see Note 1) . . . . . −0.5 V to 7 V
Output voltage range (see Note 1) . . . . . −1 V to 7 V
Input voltage range (see Note 1) . . . . . −1 V to 7 V
Power dissipation . . . . . 500 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 150°C

NOTE 1: Voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2		$V_{CC}+1$	V
V_{IL}	Low-level input voltage	−1		0.8	V
T_A	Operating free-air temperature	0		70	°C

electrical characteristics, T_A = 0°C to 70°C, V_{CC} = 5 V ±10% (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5 V,	I_{OL} = 2.1 mA		0.4	V
I_I	Input current	V_{CC} = 5.5 V,	0 V ≤ V_{IN} ≤ 5.5 V		10	μA
I_O	Output leakage current	V_O = 0.4 V to V_{CC},	Chip deselected		±10	μA
I_{CC1}	Supply current from V_{CC} (active)	V_{CC} = 5.5 V,	V_I = V_{CC} output not loaded		60	mA
I_{CC2}	Supply current from V_{CC} (power down)	V_{CC} = 5.5 V			15	mA
C_i	Input capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		6	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		12	pF

switching characteristics, T_A = 0°C to 70°C, V_{CC} = 5 V ± 10% (see Figure 1)†

PARAMETER		TMS2364-15		TMS2332-20		TMS2332-25		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address		150		200		250	ns
$t_{a(S)}$	Access time from chip select		120		120		120	ns
$t_{a(PD)}$	Access time from chip enable/power down		150		200		250	ns
$t_{v(A)}$	Output data valid after address change	0		0		0		ns
t_{dis}	Output disable time from chip select/chip enable		100		100		100	ns

† All AC measurements are made at 10% and 90% points.

PARAMETER MEASUREMENT INFORMATION

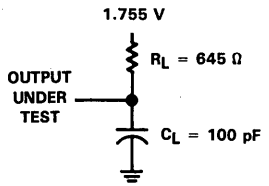


FIGURE 1. LOAD CIRCUIT

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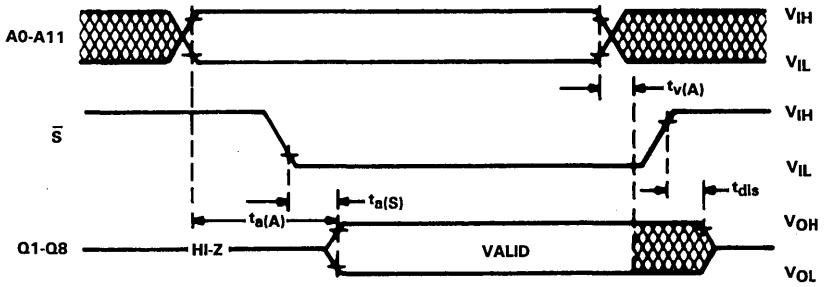
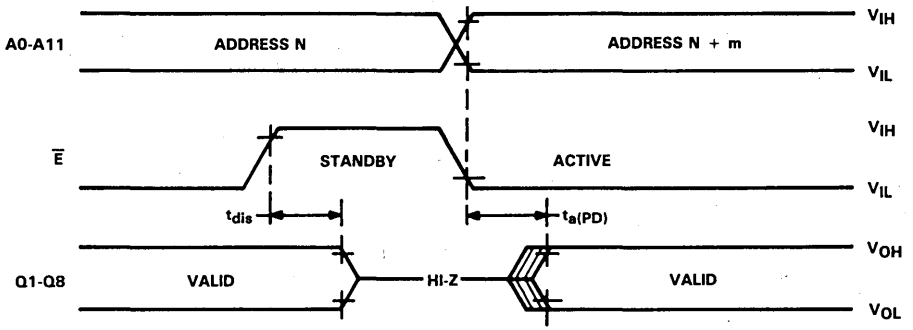
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

read cycle timing



standby mode



PROGRAMMING REQUIREMENTS AND CODE ACQUISITION

PROGRAMMING REQUIREMENTS: The TMS2332 is a fixed-program memory in which the programming is performed by TI at the factory during the manufacturing cycle to the specific customer code inputs supplied. The device is organized as 4,096 8-bit words with address locations numbered 0 to 4,095. The 8-bit words are coded as a 2-digit hexadecimal number between 00 and FF. Q1 is considered the least-significant bit and Q8 the most-significant bit. For addresses, A0 is the least-significant bit and A11 is the most-significant bit.

CODE ACQUISITION: The input media containing the customer programming data can be in the form of EPROMs, or data formatted in card images and transmitted via computer modem. (Contact TI for details on card image transmission.) 32K EPROMS can be used to supply the customer data. In addition to the input media, the information requested in Table 1 is required at the same time in order to insure proper programming of device options and accurate data control.

TABLE 1. CUSTOMER/DEVICE INFORMATION

CUSTOMER: _____

SPECIFICATION NUMBER: _____

ROM CODE NAME: _____ ROM CODE CHECKSUM: _____

CUSTOMER PART NUMBER/SYMBOLIZATION:
CUSTOMER IS ALLOWED TWO (2) LINES OF UP TO
15 ALPHANUMERIC CHARACTERS PER LINE _____
_____

ADDRESS ACCESS TIME (SPEED): _____

PACKAGE TYPE: PLASTIC (N)_____

PIN OPTIONS: 1 = HIGH, 0 = LOW, PD = POWER DOWN, CS = CHIP SELECT

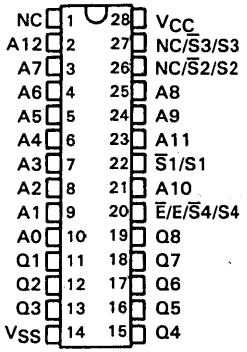
PIN 18: _____ PIN 20: _____ PD/CS: _____

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

SEPTEMBER 1984 — REVISED NOVEMBER 1985

- 8192 X 8 Organization
- Fully Static (No Clocks, No Refresh)
- All Inputs and Outputs TTL Compatible
- Single 5-V Power Supply
- Optional Power Down or Chip Select
- Maximum Access Time from Address or Power Down
  TMS2364-15 150 ns
  TMS2364-20 200 ns
  TMS2364-25 250 ns
- Pin Compatible with 2764 EPROMs
- Worst Case Active Power Dissipation . . . 330 mW
- Worst Case Standby Power Dissipation . . . 82.5 mW

N PACKAGE
(TOP VIEW)



description

The TMS2364 is a 65,536-bit read-only memory organized as 8192 words of 8-bit length. This makes the TMS2364 ideal for microprocessor-based systems. The device is fabricated using N-channel self-aligned silicon-gate technology for high speed and simple interface with bipolar and CMOS circuits.

PIN NOMENCLATURE	
A0-A12	Address Inputs
Ē/E/S̄4/S4	Chip Enable/Power Down or Chip Select
NC	No Connection
Q1-Q8	Data Out
S̄1/S1, S̄2/S2, S̄3/S3	Chip Selects
VCC	5-V Supply
VSS	Ground

The TMS2364 is fully compatible with Series 74, 74S, or 74LS TTL and CMOS logic. The data outputs are three state for OR-tying multiple devices on a common bus. Pins 20, 22, 26, and 27 are mask programmable, providing additional system flexibility. The data at the outputs is always available during a read cycle. It is not dependent on external clocking of pins 20, 22, 26, or 27.

This ROM is supplied in a 28-pin dual-in-line plastic (N suffix) package designed for insertion in mounting-hole rows on 15,24-mm (600-mil) centers. The device is designed for operation from 0°C to 70°C.

operation

address (A0-A12)

The address-valid interval determines the device cycle time. The 13-bit positive-logic address is decoded on chip to select one of 8192 words of 8-bit length in the memory array. A0 is the least-significant bit and A12 the most-significant bit of the word address.

chip selects ($\overline{S}1$ or S1, $\overline{S}2$ or S2, $\overline{S}3$ or S3)

Pins 26 and 27 can be programmed during mask fabrication to be either chip selects or no connection (NC) at the inputs. Any pin(s) programmed as chip select(s) can also be programmed to be active with either a high- or a low-level input. If pins 26 and 27 are programmed as chip selects, and pins 20, 22, 26, and 27 are active, all eight outputs are enabled; and the eight-bit addressed word can be read. When any of the signals on pins 20, 22, 26, and 27 are not active, all eight outputs are in a high-impedance state. If pins 26 and 27 are programmed as no connection (NC), the previous discussion applies to the remaining active chip select(s).

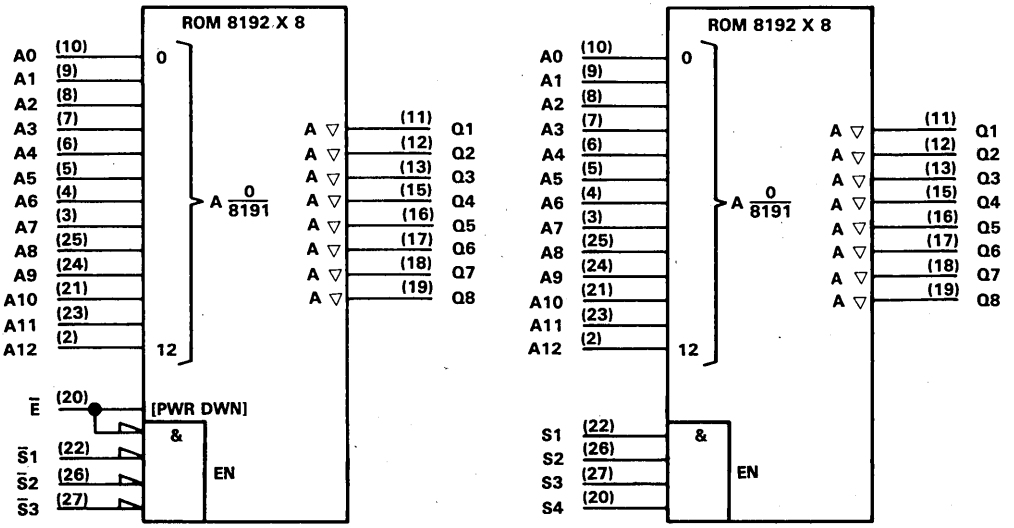
chip enable/power down ($\overline{E}$ or E) or chip select ($\overline{S}4$ or S4)

Pin 20 can be programmed during mask fabrication to be a chip-enable/power-down pin ($\overline{E}$ or E) or a fourth chip-select pin ($\overline{S}4$ or S4). Each option can be active high or active low. When the chip-enable/power-down pin is inactive, the chip is put into the standby mode. This reduces I_{CC1}, which in the active state is 60 mA, to a standby I_{CC2} of 15 mA. With the chip-select option, pin 20 is functionally identical to pin 22.

data out (Q1-Q8)

The eight outputs must be enabled by pins 20 and 22, and pins 26 and 27 if programmed as chip selects, before the output word can be read. Data will remain valid until the address is changed or the outputs are disabled (chip deselected). When disabled, the three-state outputs are in a high-impedance state. Q1 is considered the least-significant bit, Q8 the most-significant bit.

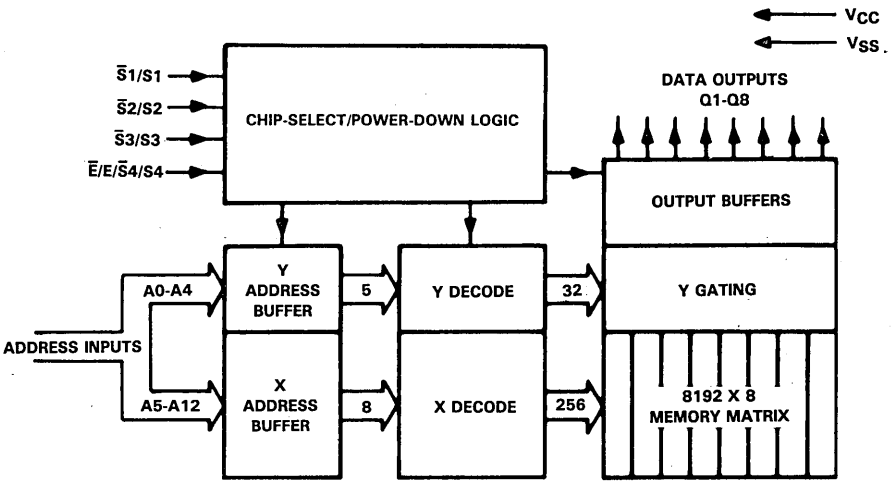
logic symbols†



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pins 20 and 22, plus pins 26 and 27 if programmed as chip selects, can be active low as shown in the symbol on the left or active high as shown in the symbol on the right. In addition, pin 20 can be either a fourth chip select ($\overline{S}4$ or S4) or a chip enable/power down ($\overline{E}$ or E).

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

functional block diagram†



† The diagram above assumes that pins 26 and 27 are programmed as chip selects.

absolute maximum ratings

Supply voltage range (see Note 1) . . . . . −0.5 V to 7 V
Output voltage range (see Note 1) . . . . . −1 V to 7 V
Input voltage range (see Note 1) . . . . . −1 V to 7 V
Power dissipation . . . . . 500 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 150°C

NOTE 1: Voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2		$V_{CC}+1$	V
V_{IL}	Low-level input voltage	−1		0.8	V
T_A	Operating free-air temperature	0		70	°C

electrical characteristics, T_A = 0°C to 70°C, V_{CC} = 5 V ± 10% (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5 V,	I_{OL} = 2.1 mA		0.4	V
I_I	Input current	V_{CC} = 5.5 V,	0 V ≤ V_{IN} ≤ 5.5 V		10	μA
I_O	Output leakage current	V_O = 0.4 V to V_{CC},	Chip deselected		±10	μA
I_{CC1}	Supply current from V_{CC} (active)	V_{CC} = 5.5 V,	V_I = V_{CC} output not loaded		60	mA
I_{CC2}	Supply current from V_{CC} (power down)	V_{CC} = 5.5 V			15	mA
C_i	Input capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		6	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		12	pF

switching characteristics, T_A = 0°C to 70°C, V_{CC}, = 5 V ± 10% (see Figure 1†)

PARAMETER		TMS2364-15		TMS2364-20		TMS2364-25		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address		150		200		250	ns
$t_{a(S)}$	Access time from chip select		120		120		120	
$t_{a(PD)}$	Access time from chip enable/power down		150		200		250	
$t_{v(A)}$	Output data valid after address change	0		0		0		
t_{dis}	Output disable time from chip select/chip enable		100		100		100	

†All AC measurements are made at 10% and 90% points.

PARAMETER MEASUREMENT INFORMATION

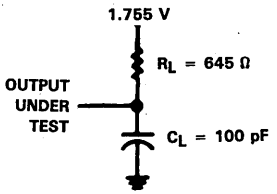
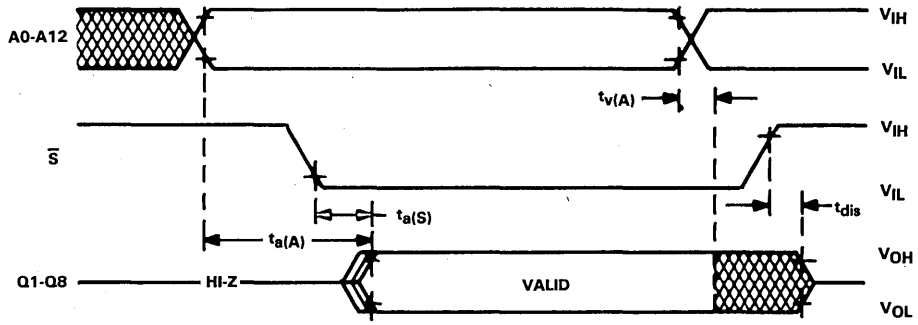


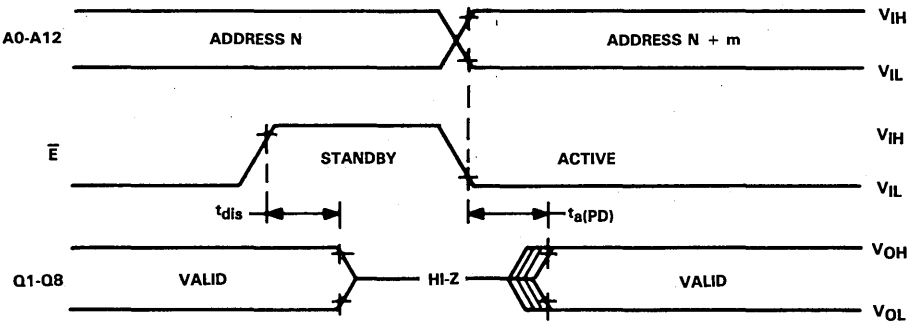
FIGURE 1. LOAD CIRCUIT

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

read cycle timing



standby mode



PROGRAMMING REQUIREMENTS AND CODE ACQUISITION

PROGRAMMING REQUIREMENTS: The TMS2364 is a fixed-program memory in which the programming is performed by TI at the factory during the manufacturing cycle to the specific customer code inputs supplied. The device is organized as 8,192 8-bit words with address locations numbered 0 to 8,191. The 8-bit words can be coded as a 2-bit hexadecimal number between 00 and FF. Q1 is considered the least-significant bit and Q8 the most-significant bit. For addresses, A0 is the least-significant bit and A12 is the most-significant bit.

CODE ACQUISITION: The input media containing the customer programming data can be in the form of EPROMs, or data formatted in card images and transmitted via computer modem (contact TI for details on card image transmission). Either 32K or 64K EPROMS can be used to supply the customer data. In addition to the input media, the information requested in Table 1 is required at the same time in order to insure proper programming of device options and accurate data control.

TABLE 1. CUSTOMER/DEVICE INFORMATION

CUSTOMER: _____
SPECIFICATION NUMBER: _____
ROM CODE NAME: _____ ROM CODE CHECKSUM: _____

CUSTOMER PART NUMBER/SYMBOLIZATION:
CUSTOMER IS ALLOWED TWO (2) LINES OF UP TO 15 ALPHANUMERIC CHARACTERS PER LINE _____ _____

ADDRESS ACCESS TIME (SPEED): _____

PACKAGE TYPE: PLASTIC (N)_____

PIN OPTIONS: 1 = HIGH, 0 = LOW, NC = NO CONNECT, PD = POWER DOWN, CS = CHIP SELECT

PIN 20: _____ PIN 22: _____ PD/CS: _____

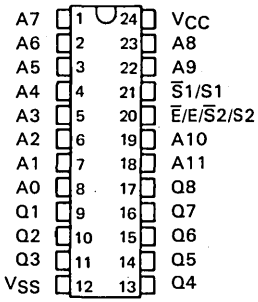
PIN 26: _____ PIN 27: _____

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

MAY 1977 – REVISED NOVEMBER 1985

- 4096 X 8 Organization
- All Inputs and Outputs TTL Compatible
- Fully Static (No Clocks, No Refresh)
- Single 5-V Power Supply
- Maximum Access Time from Address
  TMS4732-15 150 ns
  TMS4732-20 200 ns
  TMS4732-25 250 ns
- Pin-Compatible with TMS2532 EPROM
- Optional Power Down or Chip Select
- Two Output-Enable Controls for Chip Select Flexibility
- Worst Case Active Power Dissipation . . . 330 mW
- Worst Case Standby Power Dissipation . . . 82.5 mW

N PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A11	Address Inputs
Ē/E/S̄2/S2	Chip Enable/Power Down or Chip Select
Q1-Q8	Data Out
S̄1/S1	Chip Select
V_{CC}	5-V Supply
V_{SS}	Ground

description

The TMS4732 is a 32,768-bit read-only memory organized as 4,096 words of 8-bit length. This makes the TMS4732 ideal for microprocessor-based systems. The device is fabricated using N-channel self-aligned silicon-gate technology for high speed and simple interface with bipolar and CMOS circuits.

The TMS4732 is fully compatible with Series 74, 74S, or 74LS TTL and CMOS logic. The data outputs are three state for OR-tying multiple devices on a common bus. Pins 20 and 21 are mask programmable, providing additional system flexibility. The data at the outputs is always available during a read cycle. It is not dependent on external clocking of pins 20 and 21.

This ROM is supplied in a 24-pin dual-in-line plastic (N suffix) package designed for insertion in mounting-hole rows on 15,24-mm (600-mil) centers. The device is designed for operation from 0°C to 70°C.

operation

address (A0-A11)

The address-valid interval determines the device cycle time. The 12-bit positive-logic address is decoded on chip to select one of 4096 words of 8-bit length in the memory array. A0 is the least-significant bit and A11 the most-significant bit of the word address.

chip selects (S̄1 or S1 and S̄2 or S2)

Each of these pins can be programmed during mask fabrication to be active with either a high- or a low-level input. When both signals are active, all eight outputs are enabled and the eight-bit addressed word can be read. When either signal is not active, all eight outputs are in a high-impedance state.

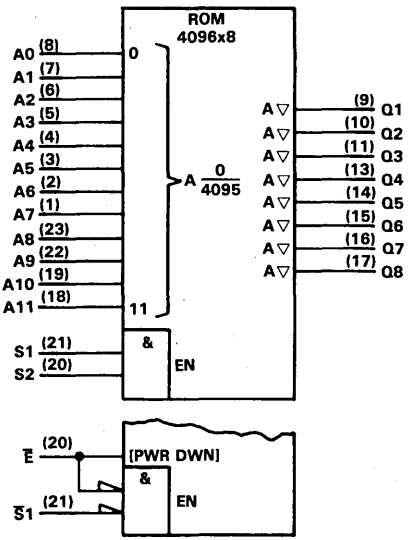
chip enable/power down ($\overline{E}$ or E) or chip select ($\overline{S}2$ or S2)

Pin 20 can be programmed during mask fabrication to be a chip-enable/power-down pin ($\overline{E}$ or E) or a secondary chip-select pin ($\overline{S}2$ or S2). Each option can be active high or active low. When the chip-enable/power-down pin is inactive, the chip is put into the standby mode. This reduces I_{CC1}, which in the active state is 60 mA, to a standby I_{CC2} of 15 mA. With pin 20 programmed as a chip-select pin, it is functionally identical to pin 21.

data out (Q1-Q8)

The eight outputs must be enabled by pins 20 and 21 before the output word can be read. Data will remain valid until the address is changed or the outputs are disabled (chip deselected). When disabled, the three-state outputs are in a high-impedance state. Q1 is considered the least-significant bit, Q8 the most-significant bit.

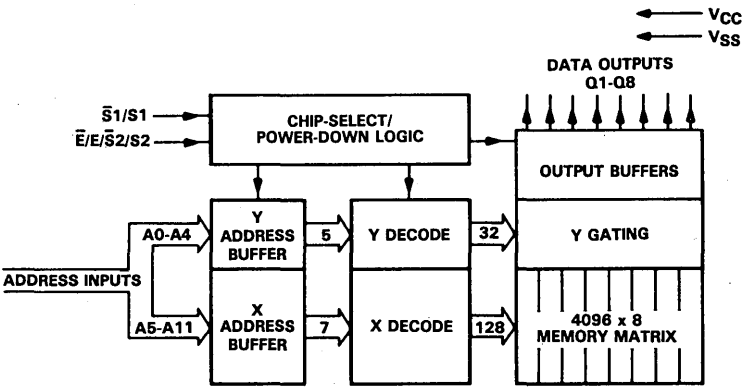
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pins 20 and 21 can be active high as shown in the upper symbol or active low as shown in the lower (partial) symbol. In addition, pin 20 can be either a second chip-select ($\overline{S}2$ or S2) or a chip-enable/power-down ($\overline{E}$ or E) pin.

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

functional block diagram



absolute maximum ratings

Supply voltage range (see Note 1) . . . . . −0.5 V to 7 V
Output voltage range (see Note 1) . . . . . −1 V to 7 V
Input voltage range (see Note 1) . . . . . −1 V to 7 V
Power dissipation . . . . . 500 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 150°C

NOTE 1: Voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2		$V_{CC}+1$	V
V_{IL}	Low-level input voltage	−1		0.8	V
T_A	Operating free-air temperature	0		70	°C

electrical characteristics, T_A = 0°C to 70°C, V_{CC} = 5 V ± 10% (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5 V,	I_{OL} = 2.1 mA		0.4	V
I_I	Input current	V_{CC} = 5.5 V,	0 V ≤ V_{IN} ≤ 5.5 V		10	μA
I_O	Output leakage current	V_O = 0.4 V to V_{CC},	Chip deselected		±10	μA
I_{CC1}	Supply current from V_{CC} (active)	V_{CC} = 5.5 V,	V_I = V_{CC} output not loaded		60	mA
I_{CC2}	Supply current from V_{CC} (power down)	V_{CC} = 5.5 V			15	mA
C_i	Input capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		6	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		12	pF

switching characteristics, T_A = 0°C to 70°C, V_{CC} = 5 V ± 10% (see Figure 1)†

PARAMETER		TMS4732-15		TMS4732-20		TMS4732-25		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address		150		200		250	ns
$t_{a(S)}$	Access time from chip select		120		120		120	ns
$t_{a(PD)}$	Access time from chip enable/power down		150		200		250	ns
$t_{v(A)}$	Output data valid after address change	0		0		0		ns
t_{dis}	Output disable time from chip select or chip enable		100		100		100	ns

† All AC measurements are made at 10% and 90% points.

PARAMETER MEASUREMENT INFORMATION

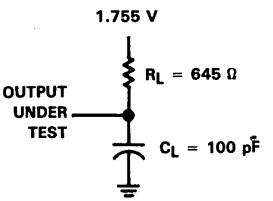
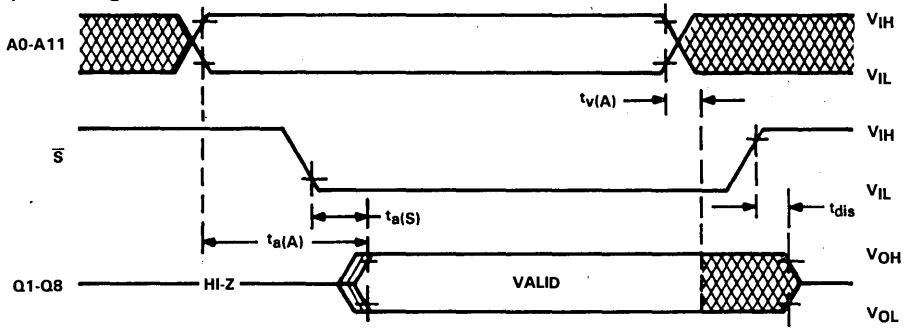


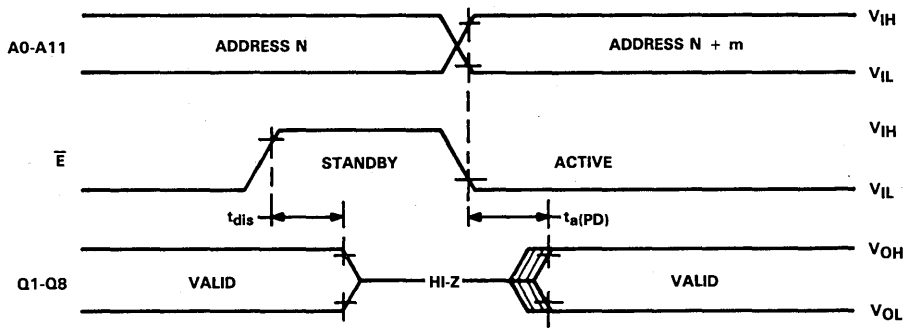
FIGURE 1. LOAD CIRCUIT

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

read cycle timing



standby mode



PROGRAMMING REQUIREMENTS AND CODE ACQUISITION

PROGRAMMING REQUIREMENTS: The TMS4732 is a fixed-program memory in which the programming is performed by TI at the factory during the manufacturing cycle to the specific customer code inputs supplied. The device is organized as 4,096 8-bit words with address locations numbered 0 to 4,095. The 8-bit words can be coded as a 2-bit hexadecimal number between 00 and FF. Q1 is considered the least-significant bit and Q8 the most-significant bit. For addresses, A0 is the least-significant bit and A11 is the most-significant bit.

CODE ACQUISITION: The input media containing the customer programming data can be in the form of EPROMs, or data formatted in card images and transmitted via computer modem (contact TI for details on card image transmission). 32K EPROMS can be used to supply the customer data. In addition to the input media, the information requested in Table 1 is required at the same time in order to insure proper programming of device options and accurate data control.

TABLE 1. CUSTOMER/DEVICE INFORMATION

CUSTOMER: _____

SPECIFICATION NUMBER: _____

ROM CODE NAME: _____ ROM CODE CHECKSUM: _____

CUSTOMER PART NUMBER/SYMBOLIZATION:
CUSTOMER IS ALLOWED TWO (2) LINES OF UP TO
15 ALPHANUMERIC CHARACTERS PER LINE _____
_____

ADDRESS ACCESS TIME (SPEED): _____

PACKAGE TYPE: PLASTIC (N) _____

PIN OPTIONS: 1 = HIGH, 0 = LOW, PD = POWER DOWN, CS = CHIP SELECT

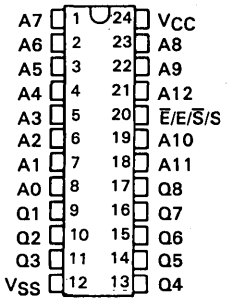
PIN 20: _____ PIN 21: _____ PD/CS: _____

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

JUNE 1981 – REVISED NOVEMBER 1985

- 8192 X 8 Organization
- Fully Static (No Clocks, No Refresh)
- All Inputs and Outputs TTL Compatible
- Optional Power Down or Chip Select
- Single 5-V Power Supply
- Maximum Access Time from Address
  TMS4764-15 150 ns
  TMS4764-20 200 ns
  TMS4764-25 250 ns
- Worst Case Active Power Dissipation . . . 330 mW
- Worst Case Standby Power Dissipation . . . 82.5 mW

N PACKAGE
(TOP VIEW)



description

The TMS4764 is a 65,536-bit read-only memory organized as 8,192 words of 8-bit length. This makes the TMS4764 ideal for microprocessor-based systems. The device is fabricated using N-channel self-aligned silicon-gate technology for high speed and simple interface with bipolar and CMOS circuits.

PIN NOMENCLATURE	
A0-A12	Address Inputs
$\overline{E}$/E/$\overline{S}$/S	Chip Enable/Power Down or Chip Select
Q1-Q8	Data Out
V_{CC}	5-V Supply
V_{SS}	Ground

The TMS4764 is fully compatible with Series 74, 74S, or 74LS TTL and CMOS logic. The data outputs are three state for OR-tying multiple devices on a common bus. Pin 20 is mask programmable, providing additional system flexibility. The data at the outputs is always available during a read cycle. It is not dependent on external clocking of pin 20.

This ROM is supplied in a 24-pin dual-in-line plastic (N suffix) package designed for insertion in mounting-hole rows on 15,24-mm (600-mil) centers. The device is designed for operation from 0°C to 70°C.

operation

address (A0-A12)

The address-valid interval determines the device cycle time. The 13-bit positive-logic address is decoded on chip to select one of 8192 words of 8-bit length in the memory array. A0 is the least-significant bit and A12 the most-significant bit of the word address.

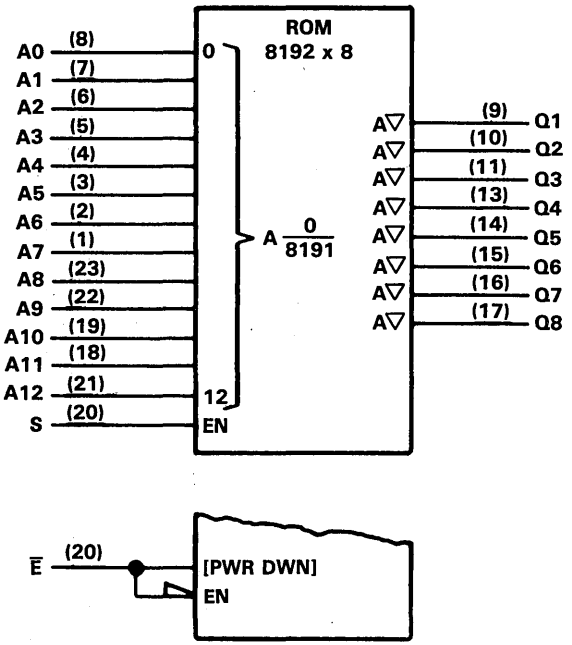
chip enable/power down ($\overline{E}$ or E or chip select $\overline{S}$ or S)

Pin 20 can be programmed during mask fabrication to be a chip-enable/power-down pin ($\overline{E}$ or E) or a chip-select pin ($\overline{S}$ or S). Each option can be active high or active low. When the chip-enable/power-down pin is inactive, the chip is put into the standby mode. This reduces I_{CC1}, which in the active mode is 60 mA, to a standby current of 15 mA. When the signal on pin 20 is active, all eight outputs are enabled and the eight-bit addressed word can be read. When the signal is not active, all eight outputs are in a high-impedance state.

data out (Q1-Q8)

The eight outputs must be enabled by pin 20 before the output word can be read. Data will remain valid until the address is changed or the outputs are disabled (chip deselected). When disabled, the three-state outputs are in a high-impedance state. Q1 is considered the least-significant bit, Q8 the most-significant bit.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin 20 can be active-high as shown in the upper symbol or active low as shown in the lower (partial) symbol. It can be either a chip select ($\overline{S}$ or S) or a chip enable/power down ($\overline{E}$ or E).

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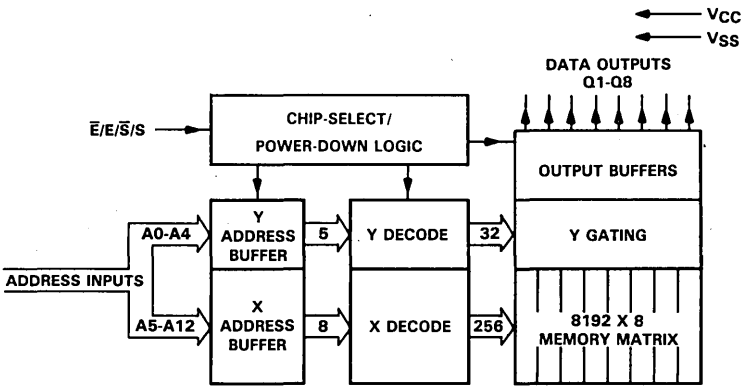
functional block diagram



absolute maximum ratings

Supply voltage range (see Note 1) . . . . . -0.5 V to 7 V
Output voltage range (see Note 1) . . . . . -1 V to 7 V
Input voltage range (see Note 1) . . . . . -1 V to 7 V
Power dissipation . . . . . 500 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . -55°C to 150°C

NOTE 1: Voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2		$V_{CC}+1$	V
V_{IL}	Low-level input voltage	-1		0.8	V
T_A	Operating free-air temperature	0		70	°C

electrical characteristics, T_A = 0°C to 70°C, V_{CC} = 5 V ±10% (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = 4.5 V,	I_{OH} = -1 mA	2.4		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5 V,	I_{OL} = 2.1 mA		0.4	V
I_I	Input current	V_{CC} = 5.5 V,	0 V ≤ V_{IN} ≤ 5.5 V		10	μA
I_O	Output leakage current	V_O = 0.4 V to V_{CC},	Chip deselected		±10	μA
I_{CC1}	Supply current from V_{CC} (active)	V_{CC} = 5.5 V,	V_I = V_{CC} output not loaded		60	mA
I_{CC2}	Supply current from V_{CC} (power down)	V_{CC} = 5.5 V			15	mA
C_i	Input capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		6	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		12	pF

switching characteristics, T_A = 0°C to 70°C, V_{CC} = 5 V ± 10% (see Figure 1)†

PARAMETER		TMS4764-15		TMS4764-20		TMS4764-25		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address		150		200		250	ns
$t_{a(S)}$	Access time from chip select		120		120		120	
$t_{a(PD)}$	Access time from chip enable/power down		150		200		250	
$t_{v(A)}$	Output data valid after address change	0		0		0		
t_{dis}	Output disable time from chip select or chip enable		100		100		100	

†All AC measurements are made at 10% and 90% points.

PARAMETER MEASUREMENT INFORMATION

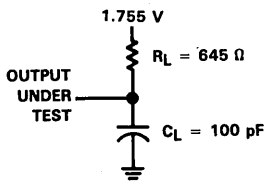
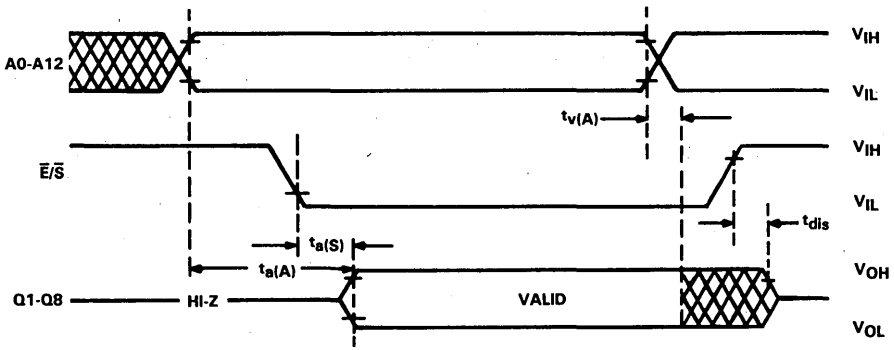


FIGURE 1. LOAD CIRCUIT

read cycle timing



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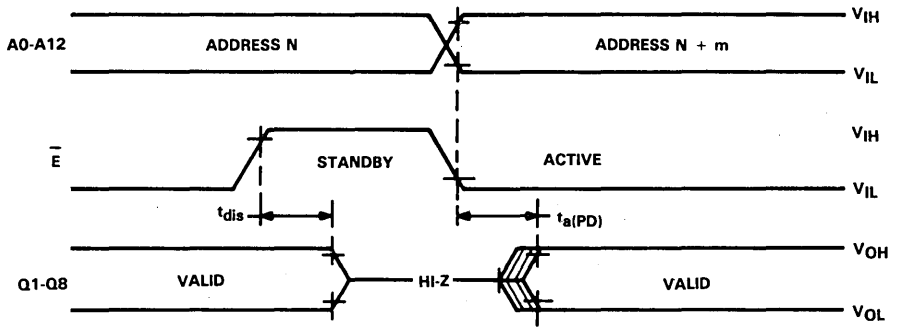
standby mode



PROGRAMMING REQUIREMENTS AND CODE ACQUISITION

PROGRAMMING REQUIREMENTS: The TMS4764 is a fixed-program memory in which the programming is performed by TI at the factory during the manufacturing cycle to the specific customer code inputs supplied. The device is organized as 8,192 8-bit words with address locations numbered 0 to 8,191. The 8-bit words are coded as a 2-digit hexadecimal number between 00 and FF. Q1 is considered the least-significant bit and Q8 the most-significant bit. For addresses, A0 is the least-significant bit and A12 is the most-significant bit.

CODE ACQUISITION: The input media containing the customer programming data can be in the form of EPROMs, or data formated in card images and transmitted via computer modem. (Contact TI for details on card image transmission.) Either 32K or 64K EPROMS can be used or any combination of them to supply the customer data. In addition to the input media, the information requested in Table 1 is required at the same time in order to insure proper programming of device options and accurate data control.

TABLE 1. CUSTOMER/DEVICE INFORMATION

CUSTOMER: _____
SPECIFICATION NUMBER: _____
ROM CODE NAME: _____ ROM CODE CHECKSUM: _____

CUSTOMER PART NUMBER/SYMBOLIZATION:
CUSTOMER IS ALLOWED TWO (2) LINES OF UP TO 15 ALPHANUMERIC CHARACTERS PER LINE _____ _____

ADDRESS ACCESS TIME (SPEED): _____

PACKAGE TYPE: PLASTIC (N)_____

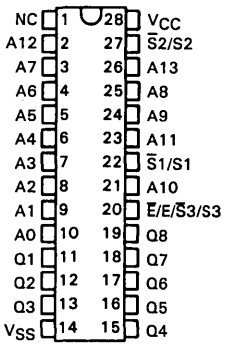
PIN OPTIONS: 1 = HIGH, 0 = LOW, PD = POWER DOWN, CS = CHIP SELECT

PIN 20: _____ PD/CS: _____

JUNE 1983 — REVISED NOVEMBER 1985

- 16,384 X 8 Organization
- Fully Static (No Clocks, No Refresh)
- All Inputs and Outputs TTL Compatible
- Single 5-V Power Supply
- Optional Power Down or Chip Select
- Maximum Access Time from Address or Power Down
  TMS47128-20 200 ns
  TMS47128-25 250 ns
  TMS47128-35 350 ns
- Pin Compatible with 27128 EPROMs
- Worst Case Active Power Dissipation . . . 330 mW
- Worst Case Standby Power Dissipation . . . 82.5 mW

N PACKAGE
(TOP VIEW)



description

The TMS47128 is a 131,072-bit read-only memory organized as 16,384 words of 8-bit length. This makes the TMS47128 ideal for microprocessor-based systems. The device is fabricated using N-channel self-aligned silicon-gate technology for high speed and simple interface with bipolar and CMOS circuits.

PIN NOMENCLATURE	
A0-A13	Address Inputs
Ē/E/S̄3/S3	Chip Enable/Power Down or Chip Select
NC	No Connection
Q1-Q8	Data Out
S̄1/S1, S̄2/S2	Chip Selects
VCC	5-V Supply
VSS	Ground

The TMS47128 is fully compatible with Series 74, 74S, or 74LS TTL and CMOS logic. The data outputs are three-state for OR-tying multiple devices on a common bus. Pins 20, 22, and 27 are mask-programmable, providing additional system flexibility. The data at the outputs is always available during a read cycle. It is not dependent on external clocking of pins 20, 22 and 27.

This ROM is supplied in a 28-pin dual-in-line plastic (N suffix) package designed for insertion in mounting-hole rows on 15,24 mm (600-mil) centers. The device is designed for operation from 0°C to 70°C.

operation, standard ROM

address (A0-A13)

The address-valid interval determines the device cycle time. The 14-bit positive-logic address is decoded on chip to select one of 16,384 words of 8-bit length in the memory array. A0 is the least-significant bit and A13 is the most-significant bit of the word address.

chip select (S̄1 or S1 and S̄2 or S2)

Pins 22 and 27 can be programmed during mask fabrication to be active with either a high- or a low-level input. When the signals on pins 20, 22, and 27 are active, all eight outputs are enabled; and the eight-bit addressed word can be read. When any of the signals on pins 20, 22, and 27 are not active, all eight outputs are in a high-impedence state.

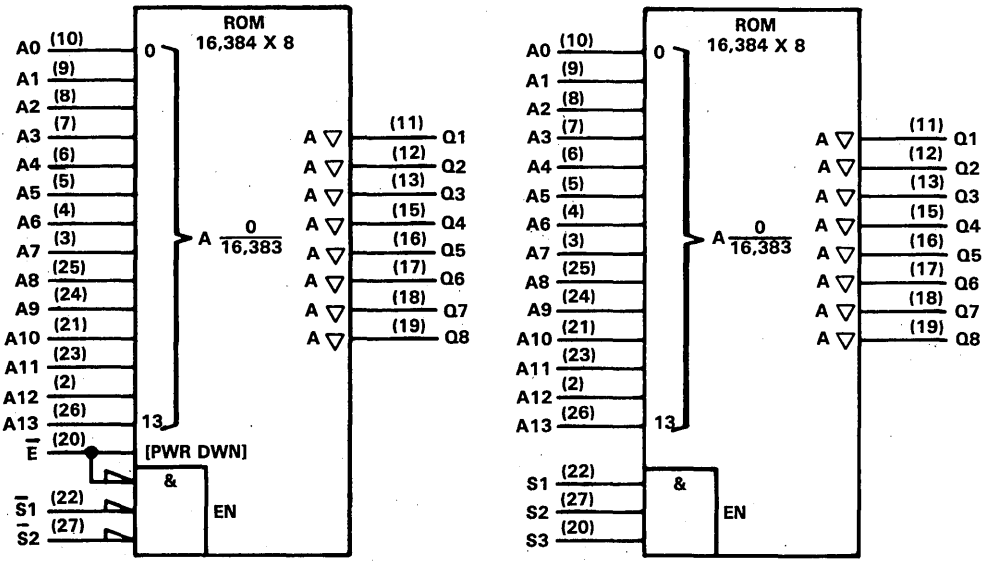
chip enable/power down (E or $\overline{E}$) or chip select (S3 or $\overline{S3}$)

Pin 20 can be programmed during mask fabrication to be a chip-enable/power-down pin (E or $\overline{E}$) or a third chip-select pin (S3 or $\overline{S3}$). Each option can be active high or active low. When the chip-enable/power-down pin is inactive, the chip is put into the standby mode. This reduces I_{CC1}, which in the active state is 60 mA, to a standby of I_{CC2} 15 mA. With the chip-select option, pin 20 is functionally identical to pins 22 and 27.

data out (Q1-Q8)

The eight outputs must be enabled by pins 20, 22, and 27 before the output word can be read. Data will remain valid until the address is changed or the outputs are disabled (chip deselected). When disabled, the three-state outputs are in a high-impedance state. Q1 is considered the least-significant bit, Q8 the most-significant bit.

logic symbols†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pins 20, 22 and 27 can be active low as shown in the symbol on the left or active high as shown in the symbol on the right. In addition, pin 20 can be either a third chip select (S3 or $\overline{S3}$) or a chip enable/power down (E or $\overline{E}$).

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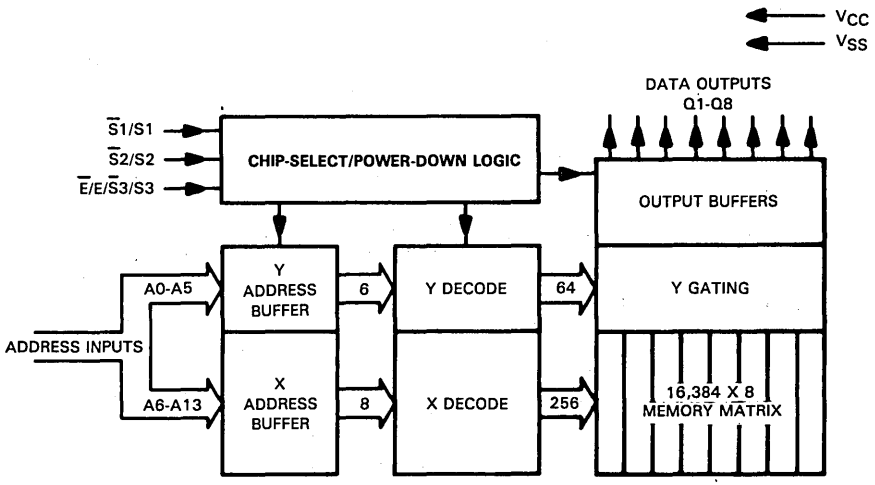
functional block diagram



absolute maximum ratings

Supply voltage range (see Note 1) . . . . . −0.5 V to 7 V
Output voltage range (see Note 1) . . . . . −1 V to 7 V
Input voltage range (see Note 1) . . . . . −1 V to 7 V
Power dissipation . . . . . 500 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 150°C

NOTE 1: Voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2		$V_{CC}+1$	V
V_{IL}	Low-level input voltage	−1		0.8	V
T_A	Operating free-air temperature	0		70	°C

electrical characteristics, T_A = 0°C to 70°C, V_{CC} = 5 V ±10% (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5 V,	I_{OL} = 2.1 mA		0.4	V
I_I	Input current	V_{CC} = 5.5 V,	0 V ≤ V_{IN} ≤ 5.5 V		10	μA
I_O	Output leakage current	V_O = 0.4 V to V_{CC},	Chip deselected		±10	μA
I_{CC1}	Supply current from V_{CC} (active)	V_{CC} = 5.5 V,	V_I = V_{CC} output not loaded		60	mA
I_{CC2}	Supply current from V_{CC} (power down)	V_{CC} = 5.5 V			15	mA
C_i	Input capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		6	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		12	pF

switching characteristics, T_A = 0°C to 70°C, V_{CC} = 5 V ± 10% (see Figure 1)†

PARAMETER		TMS47128-20		TMS47128-25		TMS47128-35		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address		200		250		350	ns
$t_{a(S)}$	Access time from chip select		120		120		150	
$t_{a(PD)}$	Access time from power down/chip enable		200		250		350	
$t_{v(A)}$	Output data valid after address change	0		0		0		
t_{dis}	Output disable time from chip select/chip enable		100		100		100	

†All AC measurements are made at 10% and 90% points.

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PARAMETER MEASUREMENT INFORMATION

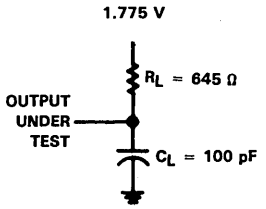
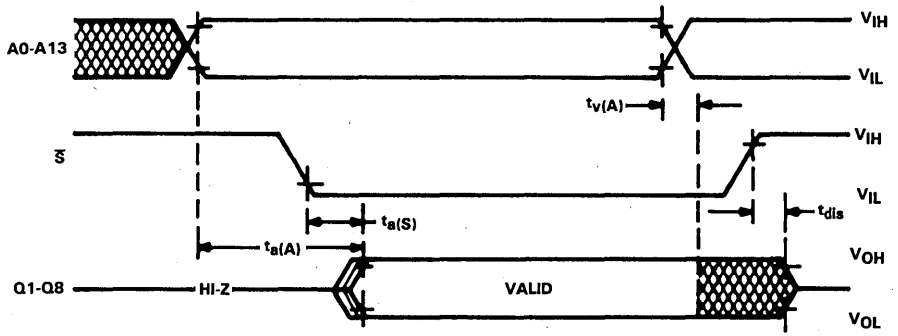
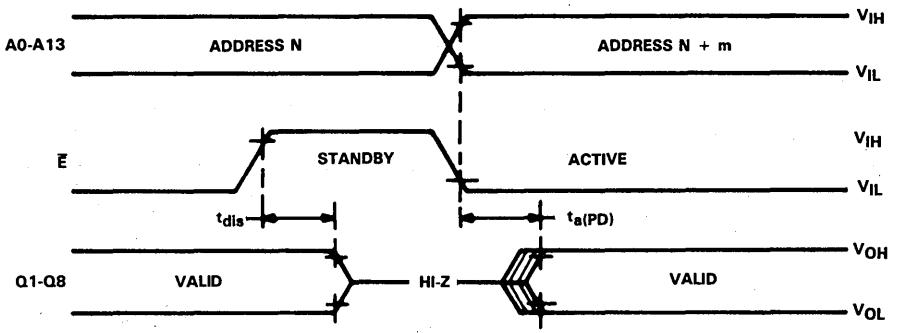


FIGURE 1. LOAD CIRCUIT

read cycle timing



standby mode



PROGRAMMING REQUIREMENTS AND CODE ACQUISITION

PROGRAMMING REQUIREMENTS: The TMS47128 is a fixed-program memory in which the programming is performed by TI at the factory during the manufacturing cycle to the specific customer code inputs supplied. The device is organized as 16,384 8-bit words with address locations numbered 0 to 16,383. The 8-bit words are coded as a 2-digit hexadecimal number between 00 and FF. Q1 is considered the least-significant bit and Q8 the most-significant bit. For addresses, A0 is the least-significant bit and A13 is the most-significant bit.

CODE ACQUISITION: The input media containing the customer programming data can be in the form of EPROMs, or data formated in card images and transmitted via computer modem. (contact TI for details on card image transmission.) Either 64K or 128K EPROMS can be used or any combination of them to supply the customer data. In addition to the input media, the information requested in Table 1 is required at the same time in order to insure proper programming of device options and accurate data control.

TABLE 1. CUSTOMER/DEVICE INFORMATION

CUSTOMER: _____
SPECIFICATION NUMBER: _____
ROM CODE NAME: _____ ROM CODE CHECKSUM: _____

CUSTOMER PART NUMBER/SYMBOLIZATION:
CUSTOMER IS ALLOWED TWO (2) LINES OF UP TO
15 ALPHANUMERIC CHARACTERS PER LINE _____
_____

ADDRESS ACCESS TIME (SPEED): _____

PACKAGE TYPE: PLASTIC (N)_____

PIN OPTIONS: 1 = HIGH, 0 = LOW, PD = POWER DOWN, CS = CHIP SELECT

PIN 20: _____ PIN 22: _____ PD/CS: _____

PIN 27: _____

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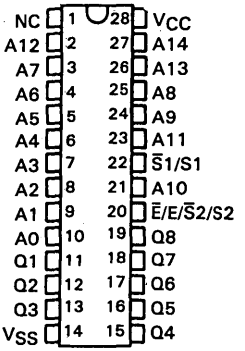
JUNE 1983 — REVISED NOVEMBER 1985

- 32,768 X 8 Organization
- Fully Static (No Clocks, No Refresh)
- All Inputs and Outputs TTL Compatible
- Single 5-V Power Supply
- Optional Power Down or Chip Select
- Maximum Access Time from Address or Power Down

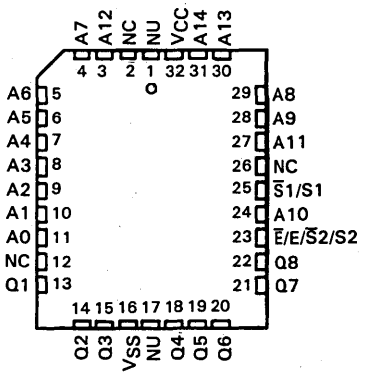
TMS47256-20	200 ns
TMS47256-25	250 ns
TMS47256-30	300 ns

- Worst Case Active Power Dissipation . . . 330 mW
- Worst Case Standby Power Dissipation . . . 82.5 mW
- Pin Compatible with 27256 and 27C256 Type EPROMs

N PACKAGE
(TOP VIEW)



FM PACKAGE
(TOP VIEW)



description

The TMS47256 is a 262,144-bit read-only memory organized as 32,768 words of 8-bit length. This makes the TMS47256 ideal for microprocessor-based systems. The device is fabricated using N-channel self-aligned silicon-gate technology for high speed and simple interface with bipolar and CMOS circuits.

The TMS47256 is fully compatible with Series 74, 74S, or 74LS TTL and CMOS logic. The data outputs are three state for OR-tying multiple devices on a common bus. Pins 20 and 22 (dual-in-line package) and pins 23 and 25 (chip carrier) are mask programmable, providing additional system flexibility. The data at the outputs is always available during a read cycle. It is not dependent on external clocking of $\overline{E}$ and $\overline{S}$ pins.

This ROM is supplied in a 28-pin dual-in-line plastic (N suffix) package designed for insertion in mounting-hole rows on 15,24-mm (600-mil) centers. It is also supplied in a 32-lead plastic leaded chip carrier package designed for surface mount applications using 1,25-mm (50-mil) lead spacing. Both package styles conform to JEDEC standards. The device is designed for operation from 0°C to 70°C.

PIN NOMENCLATURE	
A0-A14	Address Inputs
$\overline{E}/E/\overline{S}2/S2$	Chip Enable/Power Down or Chip Select
NC	No Connection
NU	Make No External Connection
Q1-Q8	Data Out
$\overline{S}1/S1$	Chip Select
V_{CC}	5-V Supply
V_{SS}	Ground

operation

address (A0-A14)

The address-valid interval determines the device cycle time. The 15-bit positive-logic address is decoded on chip to select one of 32,768 words of 8-bit length in the memory array. A0 is the least-significant bit and A14 is the most-significant bit of the word address.

chip select ($\overline{S}1$ or S1)

Pin 22 (dual-in-line package) and pin 25 (chip carrier) can be programmed during mask fabrication to be active with either a high- or low-level input. When the signal on both pins 22 and 20 (dual-in-line package) and pins 23 and 25 (chip carrier) are active, all eight outputs are enabled; and the eight-bit addressed word can be read. When the signal on either of these pins is not active, all eight outputs are in a high-impedance state.

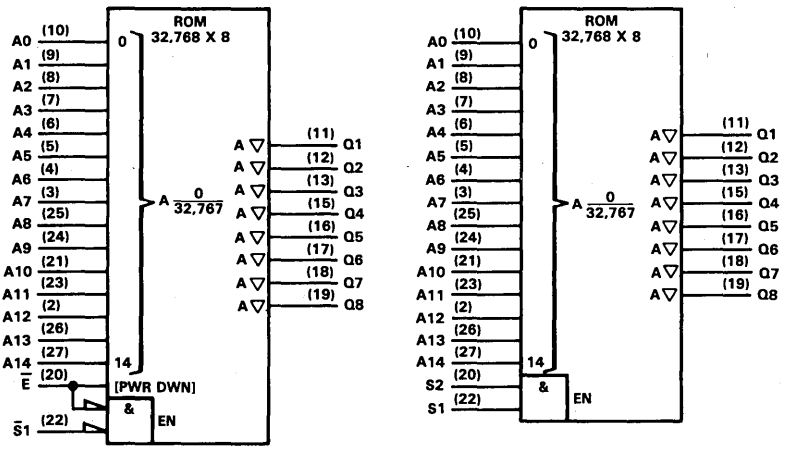
chip enable/power down ($\overline{E}$ or E) or chip select ($\overline{S}2$ or S2)

Pin 20 (dual-in-line package) and pin 23 (chip carrier) can be programmed during mask fabrication to be a chip-enable/power down pin ($\overline{E}$ or E) or a secondary chip-select pin ($\overline{S}2$ or S2). Each option can be active high or active low. When the chip-enable/power-down pin is inactive, the chip is put in the standby mode. This reduces I_{CC1}, which in the active state is 60 mA, to a standby I_{CC2} of 15 mA. With the chip-select option, pin 20 is functionally identical to pin 22 for the dual-in-line package and pin 23 is functionally identical to pin 25 for the chip carrier.

data out (Q1-Q8)

The eight outputs must be enabled by the $\overline{E}$ and $\overline{S}$ pins before the output word can be read. Data will remain valid until the address is changed or the outputs are disabled (chip deselected). When disabled, the three-state outputs are in a high-impedance state. Q1 is considered the least-significant bit, Q8 the most-significant bit.

logic symbols†



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pins 20 and 22 can be active low as shown in the symbol on the left or active high as shown in the symbol on the right. In addition, pin 20 can be either a secondary chip select (S2 or $\overline{S}2$) or a chip enable/power down (E or $\overline{E}$). The pin numbers shown are for the 28-pin dual-in-line package.

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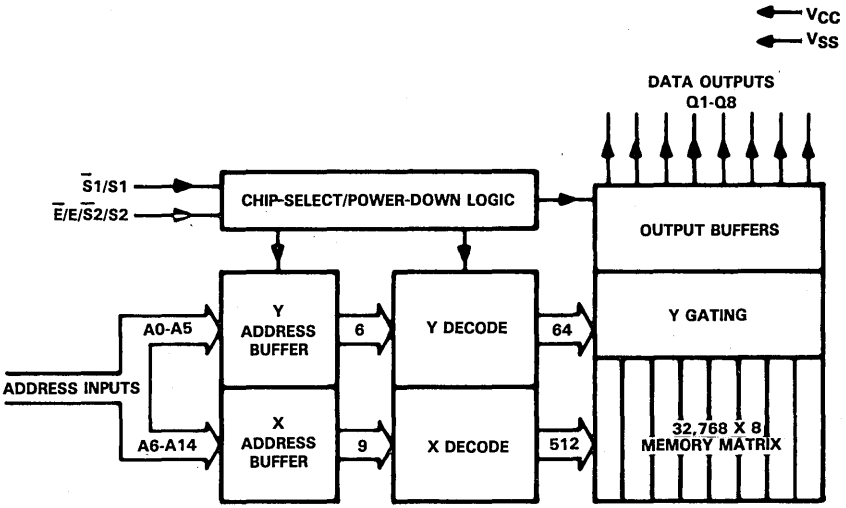
functional block diagram



absolute maximum ratings

Supply voltage to ground potential (see Note 1) . . . . . -0.5 V to 7 V
Applied output voltage (see Note 1) . . . . . -1 V to 7 V
Applied input voltage (see Note 1) . . . . . -1 V to 7 V
Power dissipation . . . . . 500 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . -55°C to 150°C

NOTE 1: Voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2		$V_{CC}+1$	V
V_{IL}	Low-level input voltage	-1		0.8	V
T_A	Operating free-air temperature	0		70	°C

electrical characteristics, T_A = 0°C to 70°C, V_{CC} = 5 V ±10% (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5 V,	I_{OL} = 2.1 mA		0.4	V
I_I	Input current	V_{CC} = 5.5 V,	0 V ≤ V_{IN} ≤ 5.5 V		10	μA
I_O	Output leakage current	V_O = 0 V to V_{CC},	Chip deselected		±10	μA
I_{CC1}	Supply current from V_{CC} (active)	V_{CC} = 5.5 V,	V_I = V_{CC} Output not loaded		60	mA
I_{CC2}	Supply current from V_{CC} (power down)	V_{CC} = 5.5 V			15	mA
C_i	Input capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		6	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		12	pF

switching characteristics, T_A = 0°C to 70°C, V_{CC} = 5 V ±10% (see Figure 1)†

PARAMETER		TMS47256-20		TMS47256-25		TMS47256-30		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(AD)}$	Access time from address		200		250		300	ns
$t_{a(S)}$	Access time from chip select		120		120		120	
$t_{a(PD)}$	Access time from power down/chip enable		200		250		300	
$t_{v(A)}$	Output data valid after address change	0		0		0		
t_{dis}	Output disable time from chip select/chip enable		100		100		100	

†All AC measurements are made at 10% and 90% points.

PARAMETER MEASUREMENT INFORMATION

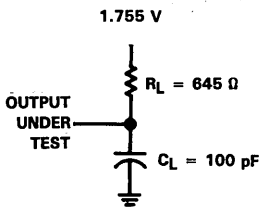
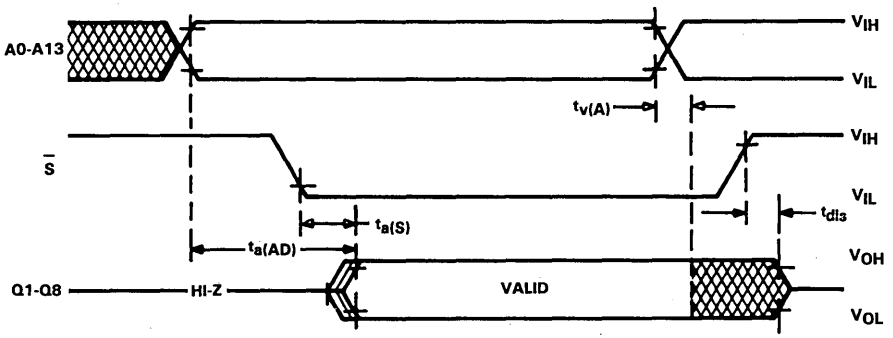


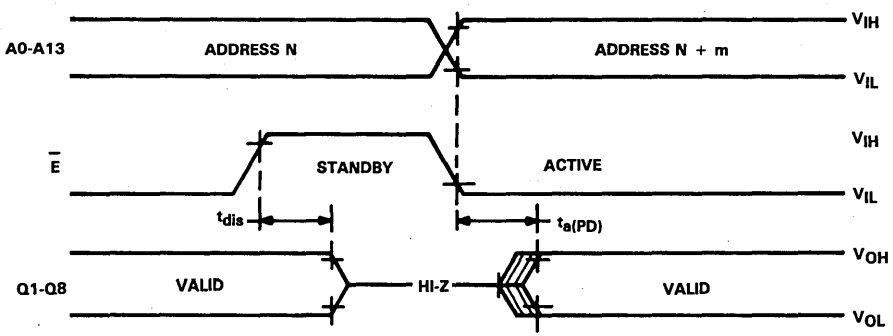
FIGURE 1. LOAD CIRCUIT

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

read cycle timing



standby mode



PROGRAMMING REQUIREMENTS AND CODE ACQUISITION

PROGRAMMING REQUIREMENTS: The TMS47256 is a fixed-program memory in which the programming is performed by TI at the factory during the manufacturing cycle to the specific customer code inputs supplied. The device is organized as 32,768 8-bit words with address locations numbered 0 to 32,767. The 8-bit words are coded as a 2-digit hexadecimal number from 00 and FF. Q1 is considered the least-significant bit and Q8 is the most-significant bit. For addresses, A0 is the least-significant bit and A14 is the most-significant bit.

CODE ACQUISITION: The input media containing the customer programming data can be in the form of EPROMs, or data formatted in card images and transmitted via computer modem (contact TI for details on card image transmission). Either 64K, 128K, or 256K EPROMS can be used or any combination of them to supply the customer data. In addition to the input media, the information requested in Table 1 is required at the same time in order to insure proper programming of device options and accurate data control.

TABLE 1. CUSTOMER/DEVICE INFORMATION

CUSTOMER: _____
SPECIFICATION NUMBER: _____
ROM CODE NAME: _____ ROM CODE CHECKSUM: _____

CUSTOMER PART NUMBER/SYMBOLIZATION:
CUSTOMER IS ALLOWED TWO (2) LINES OF UP TO
15 ALPHANUMERIC CHARACTERS PER LINE _____
_____

ADDRESS ACCESS TIME (SPEED): _____

PACKAGE TYPE: PLASTIC (N)_____ SURFACE MOUNT (FM)_____

PIN OPTIONS: 1 = HIGH, 0 = LOW, PD = POWER DOWN, CS = CHIP SELECT

N PACKAGE: PIN 20 _____ PIN 22 _____ PD/CS _____

FM PACKAGE: PIN 23 _____ PIN 25_____ PD/CS _____

TEXAS INSTRUMENTS
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TMS47C256
32,768-WORD BY 8-BIT READ-ONLY MEMORY

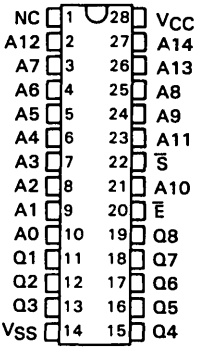
NOVEMBER 1985

- 32,768 X 8 Organization
- Fully Static (No Clocks, No Refresh)
- All Inputs and Outputs TTL Compatible
- Single 5-V Power Supply
- HVCMOS Technology
- Maximum Access Time from Address or Power Down

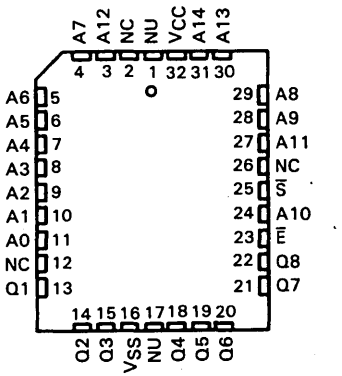
TMS47C256-15	150 ns
TMS47C256-20	200 ns
TMS47C256-25	250 ns

- Pin Compatible with 27256 EPROMs
- Worst Case Active Power Dissipation . . . 275 mW
- Worst Case Standby Power Dissipation . . . 2.8 mW

N PACKAGE
(TOP VIEW)



FM PACKAGE
(TOP VIEW)



description

The TMS47C256 is a 262,144-bit read-only memory organized as 32,768 words of 8-bit length. This makes the TMS47C256 ideal for microprocessor-based systems. The device is fabricated using HVCMOS technology for high speed and simple interface with bipolar and CMOS circuits.

The TMS47C256 is fully compatible with Series 74, 74S, or 74LS TTL and CMOS logic. The data outputs are three state for OR-tying multiple devices on a common bus. The data at the outputs is always available during a read cycle. It is not dependent on external clocking of the chip-select pin(s).

This ROM is supplied in a 28-pin dual-in-line plastic (N suffix) package designed for insertion in mounting-hole rows on 15,24-mm (600-mil) centers. It is also supplied in a 32-lead plastic leaded chip carrier package using 1,25-mm (50-mil) lead spacing. Both package styles conform to JEDEC standards. The device is designed for operation from 0°C to 70°C.

PIN NOMENCLATURE	
A0-A14	Address Inputs
Ē	Chip Enable/Power Down
NC	No Connection
NU	Make No External Connection
Q1-Q8	Data Out
S̄	Chip Select
VCC	5-V Supply
VSS	Ground

operation

address (A0-A14)

The address-valid interval determines the device cycle time. The 15-bit positive-logic address is decoded on-chip to select one of 32,768 words of 8-bit length in the memory array. A0 is the least-significant bit and A14 the most-significant bit of the word address.

TEXAS INSTRUMENTS
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chip select ($\overline{S}$)

When the signal on both the chip-select and chip-enable/power-down pins are active, all eight outputs are enabled; and the 8-bit addressed word can be read. When the signal on either the chip-select or the chip-enable/power-down pin is not active, all eight outputs are in a high-impedance state.

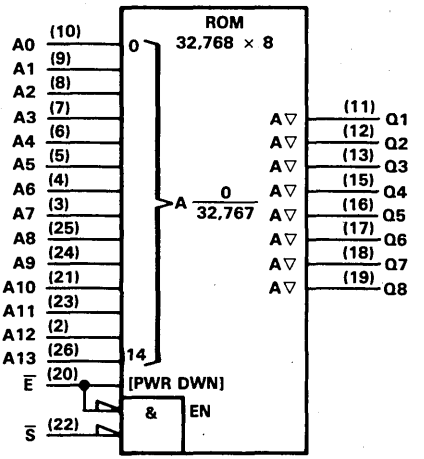
chip enable/power down ($\overline{E}$)

When the chip-enable/power-down pin is inactive, the chip is put in the standby mode. This reduces I_{CC1}, which in the active state is 50 mA, to a standby I_{CC2} of 500 μA. In this mode all outputs are in a high-impedance state.

data out (Q1-Q8)

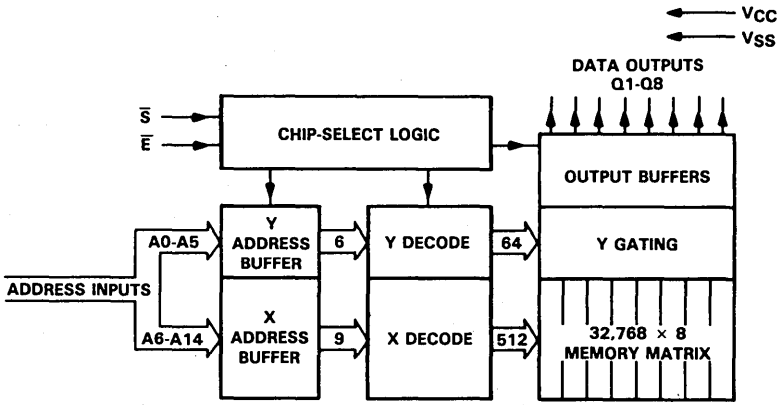
The eight outputs must be enabled by the chip-select and chip-enable/power-down pins before the output word can be read. Data will remain valid until the address is changed or the outputs are disabled (chip deselected). When disabled, the three-state outputs are in a high-impedance state. Q1 is considered the least-significant bit, Q8 the most-significant bit.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
The pin numbers shown are for the 28-pin dual-in-line package.

functional block diagram



absolute maximum ratings

Supply voltage to ground potential (see Note 1) . . . . . -0.5 V to 7 V
Applied output voltage (see Note 1) . . . . . -0.3 V to V_{CC} + 0.3 V
Applied input voltage (see Note 1) . . . . . -0.3 V to V_{CC} + 0.3 V
Power dissipation . . . . . 300 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . -55°C to 150°C

NOTE 1: Voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2		V_{CC}	V
V_{IL}	Low-level input voltage	-0.5		0.8	V
T_A	Operating free-air temperature	0		70	°C

electrical characteristics, T_A = 0°C to 70°C, V_{CC} = 5 V ±10% (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = 4.5 V,	I_{OH} = −400 μA	2.4		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5 V,	I_{OL} = 2.1 mA		0.4	V
I_I	Input current	V_{CC} = 5.5 V,	0 V ≤ V_{IN} ≤ 5.5 V		10	μA
I_O	Output leakage current	V_O = 0 V to V_{CC},	Chip deselected		±10	μA
I_{CC1}	Supply current from V_{CC} (active)	V_{CC} = 5.5 V,	V_I = V_{CC} Output not loaded		50	mA
I_{CC2}	Supply current from V_{CC} (power down)	V_{CC} = 5.5 V			500	μA
C_i	Input capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		6	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		12	pF

switching characteristics, T_A = 0°C to 70°C, V_{CC} = 5 V ±10% (see Figure 1)†

PARAMETER		TMS47C256-15		TMS47C256-20		TMS47C256-25		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address		150		200		250	ns
$t_{a(S)}$	Access time from chip select		75		75		100	
$t_{a(PD)}$	Access time from power down/chip enable		150		200		250	
$t_{v(A)}$	Output data valid after address change	0		0		0		
t_{dis}	Output disable time from chip select/chip enable		60		60		60	

†All AC measurements are made at 10% and 90% points.

PARAMETER MEASUREMENT INFORMATION

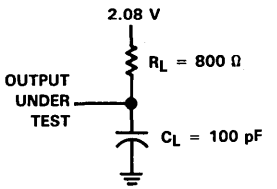


FIGURE 1. LOAD CIRCUIT

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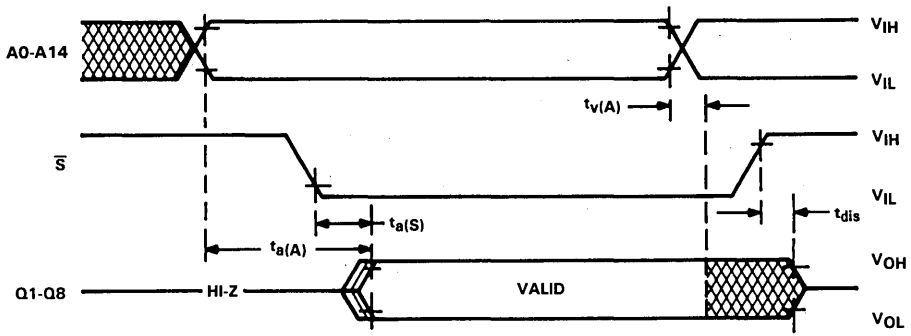
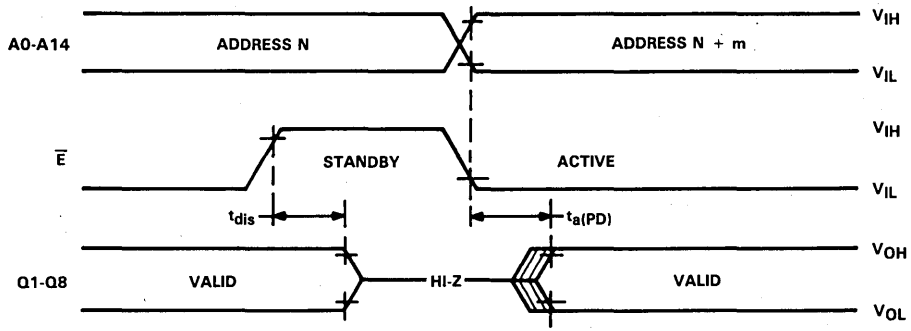
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

read cycle timing



standby mode



PROGRAMMING REQUIREMENTS AND CODE ACQUISITION

PROGRAMMING REQUIREMENTS: The TMS47C256 is a fixed program memory in which the programming is performed by TI at the factory during the manufacturing cycle to the specific customer code inputs supplied. The device is organized as 32,768 8-bit words with address locations numbered 0 to 32,767. The 8-bit words are coded as a 2-digit hexadecimal number between 00 and FF. Q1 is considered the least-significant bit and Q8 the most-significant bit. For addresses, A0 is the least-significant bit and A14 is the most-significant bit.

CODE ACQUISITION: The input media containing the customer programming data can be in the form of EPROMs, or data formatted in card images and transmitted via computer modem (contact TI for details on card image transmission). Either 64K, 128K, or 256K EPROMs can be used or any combination of them to supply the customer data. In addition to the input media, the information requested in Table 1 is required at the same time in order to insure proper programming of device options and accurate data control.

TABLE 1. CUSTOMER/DEVICE INFORMATION

CUSTOMER: _____

SPECIFICATION NUMBER: _____

ROM CODE NAME: _____ ROM CODE CHECKSUM: _____

CUSTOMER PART NUMBER/SYMBOLIZATION:
CUSTOMER IS ALLOWED TWO (2) LINES OF UP TO
15 ALPHANUMERIC CHARACTERS PER LINE _____
_____

ADDRESS ACCESS TIME (SPEED): _____

PACKAGE TYPE: PLASTIC (N)_____ SURFACE MOUNT (FM)_____

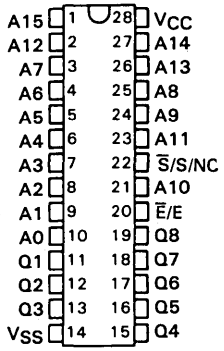
TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

TMS47C512
65,536-WORD BY 8-BIT READ-ONLY MEMORY

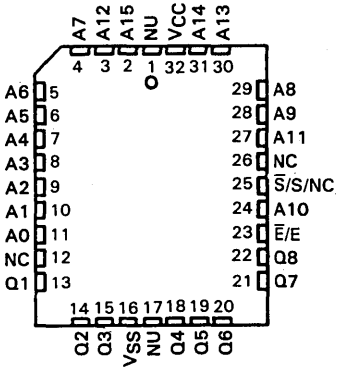
NOVEMBER 1985

- 65,536 X 8 Organization
- Fully Static (No Clocks, No Refresh)
- All Inputs and Outputs TTL and CMOS Compatible
- Single 5-V Power Supply
- Standby Mode for Minimum Power Usage
- Maximum Access Time from Address or Power Down
  TMS47C512-20 200 ns
  TMS47C512-25 250 ns
  TMS47C512-30 300 ns
- Pin Compatible with 27512 EPROMs

N PACKAGE
(TOP VIEW)



FM PACKAGE
(TOP VIEW)



description

The TMS47C512 is a 524,288-bit read-only memory organized as 65,536 words of 8-bit length. This makes the TMS47C512 ideal for microprocessor-based systems. The device is fabricated using HVCMOS technology for high speed and simple interface with bipolar and CMOS circuits.

The TMS47C512 is fully compatible with Series 74, 74S, or 74LS TTL and CMOS logic. The data outputs are three state for OR-tying multiple devices on a common bus. The chip-select and chip-enable/power-down pins are mask programmable, providing additional system flexibility. The data at the outputs is always available during a read cycle. It is not dependent on external clocking of the chip-select and chip-enable/power-down pins.

This ROM is supplied in a 28-pin dual-in-line plastic (N suffix) package designed for insertion in mounting-hole rows on 15,24-mm (600-mil) centers. It is also supplied in a 32-lead plastic leaded chip carrier package using 1,25-mm (50-mil) lead spacing. Both package styles conform to JEDEC standards. The device is designed for operation from 0°C to 70°C.

PIN NOMENCLATURE	
A0-A15	Address Inputs
$\overline{E}$/E	Chip Enable/Power Down
NC	No Connection
NU	Make No External Connection
Q1-Q8	Data Out
$\overline{S}$/S	Chip Select
V_{CC}	5-V Supply
V_{SS}	Ground

operation

address (A0-A15)

The address-valid interval determines the device cycle time. The 16-bit positive-logic address is decoded on-chip to select one of 65,636 words of 8-bit length in the memory array. A0 is the least-significant bit and A15 is the most-significant bit of the word address.

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chip select ($\overline{S}$ or S)

The chip-select pin (pin 23 for the dual-in-line package and pin 25 for the chip carrier) can be programmed during mask fabrication to be active with either a high- or low-level input. When the signal on both the chip-select and chip-enable/power-down pins are active, all eight outputs are enabled; and the 8-bit addressed word can be read. When the signals on the chip-select and chip-enable/power-down pins are not active, all eight outputs are in a high-impedance state. Pin 22 (dual-in-line package) and pin 25 (chip carrier) can also be programmed as a no connection if only a chip enable is required.

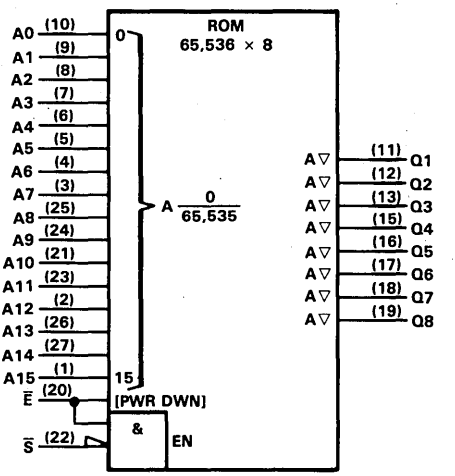
chip enable/power down ($\overline{E}$)

The chip-enable/power-down pin (pin 20 for the dual-in-line package and pin 23 for the chip carrier) can be programmed during mask fabrication to be active with either a high-level or low-level input. When the chip-enable/power-down pin is inactive, the chip is put into the standby mode. In this mode all outputs are in the high-impedance state.

data out (Q1-Q8)

The eight outputs must be enabled by the chip-select and chip-enable/power-down pins before the output word can be read. Data will remain valid until the address is changed or the outputs are disabled (chip deselected). When disabled, the three-state outputs are in a high-impedance state. Q1 is considered the least-significant bit, Q8 the most-significant bit.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
The pin numbers shown are for the 28-pin dual-in-line package. Pins 20 and 22 can be active low as shown in the symbol above or active high. In addition, pin 22 can be a no connection.

TEXAS INSTRUMENTS
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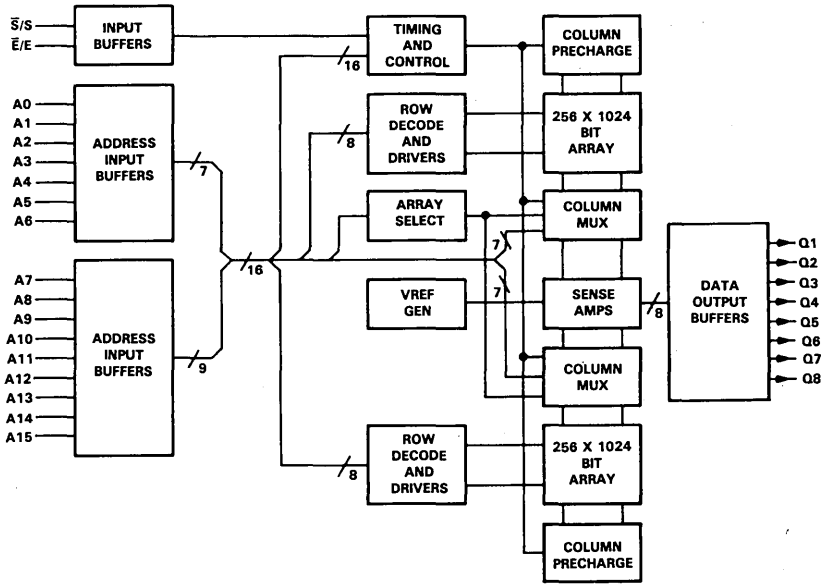
functional block diagram



absolute maximum ratings

Supply voltage to ground potential (see Note 1) . . . . . −0.5 V to 7 V
Applied output voltage (see Note 1) . . . . . −0.3 V to V_{CC} + 0.3 V
Applied input voltage (see Note 1) . . . . . −0.3 V to V_{CC} + 0.3 V
Power dissipation . . . . . T.B.D.
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 150°C

NOTE 1: Voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2		V_{CC}	V
V_{IL}	Low-level input voltage	−0.5		0.8	V
T_A	Operating free-air temperature	0		70	°C

Additional information on these products can be obtained from the factory as it becomes available.

electrical characteristics, T_A = 0°C to 70°C, V_{CC} = 5 V ±10% (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = 4.5 V,	I_{OH} = −400 μA	2.4		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5 V,	I_{OL} = 2.1 mA		0.4	V
I_I	Input leakage current	V_{CC} = 5.5 V,	0 V ≤ V_{IN} ≤ 5.5 V		10	μA
I_O	Output leakage current	V_O = 0 V to V_{CC},	Chip deselected		±10	μA
I_{CC1}	Supply current from V_{CC} (active)	V_{CC} = 5.5 V,	V_I = V_{CC} Output not loaded		T.B.D.	
I_{CC2}	Supply current from V_{CC} (standby)	V_{CC} = 5.5 V			T.B.D.	
C_i	Input capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		10	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		15	pF

switching characteristics, T_A = 0°C to 70°C, V_{CC} = 5 V ±10% (unless otherwise noted)

PARAMETER		TMS47C512-20		TMS47C512-25		TMS47C512-30		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address		200		250		300	ns
$t_{a(S)}$	Access time from chip select		100		100		100	
$t_{a(PD)}$	Access time from power down/chip enable		200		250		300	
$t_{v(A)}$	Output data valid after address change	0		0		0		
t_{dis}	Output disable time from chip select		100		100		100	

†All AC measurements are made at 10% and 90% points.

ROMs

7

PARAMETER MEASUREMENT INFORMATION

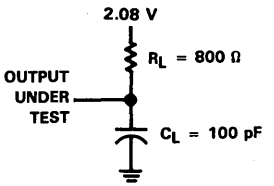


FIGURE 1. LOAD CIRCUIT

Additional information on these products can be obtained from the factory as it becomes available.

TEXAS INSTRUMENTS
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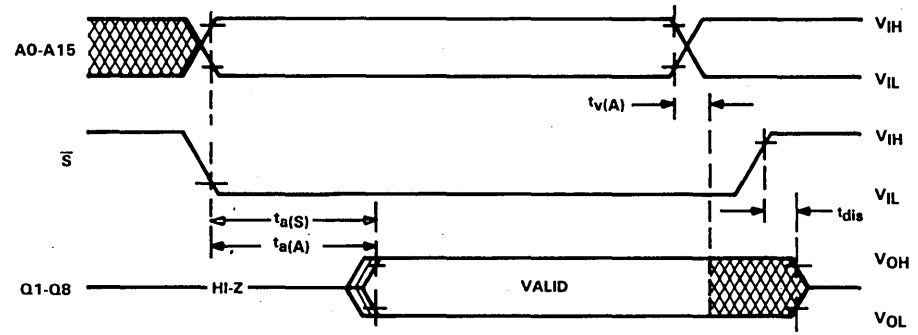
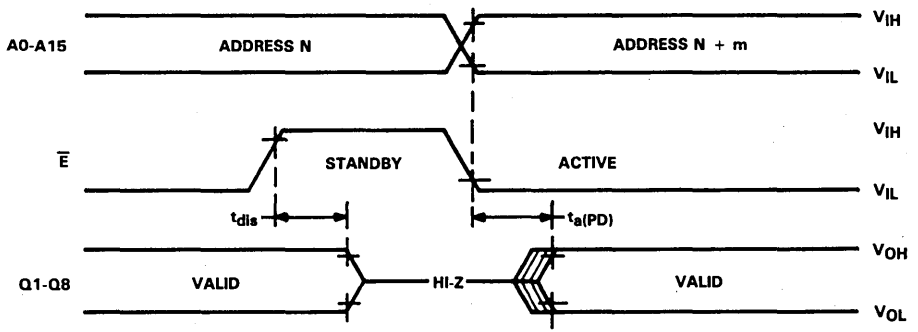
read cycle timing



standby mode



PROGRAMMING REQUIREMENTS AND CODE ACQUISITION

PROGRAMMING REQUIREMENTS: The TMS47C512 is a fixed-program memory in which the programming is performed by TI at the factory during the manufacturing cycle to the specific customer code requirements. The device is organized as 65,536 8-bit words with address locations numbered 0 to 65,535. The 8-bit words can be coded as a 2-digit hexadecimal number between 00 and FF. Q1 is considered the least-significant bit and Q8 the most-significant bit. For addresses, A0 is the least-significant bit and A15 is the most significant bit.

CODE ACQUISITION: The input media containing the customer programming data can be in the form of EPROMs, or data formatted in card images and transmitted via computer modem (contact TI for details on card image transmission). Either 64K, 128K, 256K, or 512K EPROMS can be used or any combination of them to supply the customer data. In addition to the input media, the information requested in Table 1 is required at the same time in order to insure proper programming of device options and accurate data control.

TABLE 1. CUSTOMER/DEVICE INFORMATION

CUSTOMER: _____

SPECIFICATION NUMBER: _____

ROM CODE NAME: _____ ROM CODE CHECKSUM: _____

CUSTOMER PART NUMBER/SYMBOLIZATION:
CUSTOMER IS ALLOWED TWO (2) LINES OF UP TO
15 ALPHANUMERIC CHARACTERS PER LINE _____
_____

ADDRESS ACCESS TIME (SPEED): _____

PACKAGE TYPE: PLASTIC (N) _____ SURFACE MOUNT (FM) _____

PIN OPTIONS: 1 = HIGH, 0 = LOW.

N PACKAGE:	PIN 20: _____	PIN 22: _____
PLCC:	PIN 23: _____	PIN 25 _____

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

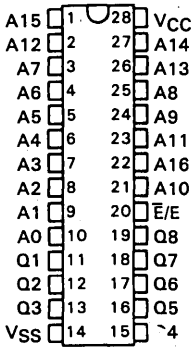
TMS47C1024
131,072-WORD BY 8-BIT READ-ONLY MEMORY

NOVEMBER 1985

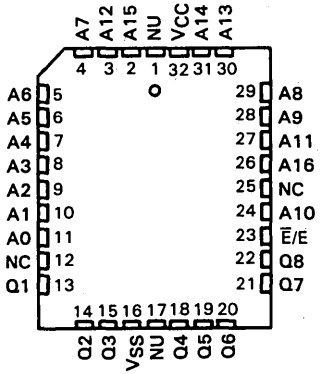
- 131,072 X 8 Organization
- Fully Static (No Clocks, No Refresh)
- All Inputs and Outputs TTL and CMOS Compatible
- Single 5-V Power Supply
- Standby Mode for Minimum Power Usage
- Maximum Access Time from Address or Power Down

TMS47C1024-20	200 ns
TMS47C1024-25	250 ns
TMS47C1024-30	300 ns

N PACKAGE
(TOP VIEW)



FM PACKAGE
(TOP VIEW)



description

The TMS47C1024 is a 1,048,576-bit read-only memory organized as 131,072 words of 8-bit length. This makes the TMS47C1024 ideal for microprocessor-based systems. The device is fabricated using HVCMOS technology for high speed and simple interface with bipolar and CMOS circuits.

The TMS47C1024 is fully compatible with Series 74, 74S, or 74LS TTL and CMOS logic. The data outputs are three state for OR-tying multiple devices on a common bus. The chip-enable/power-down pin is mask programmable, providing additional system flexibility. The data at the outputs is always available during a read cycle. It is not dependent on external clocking of the chip-enable/power-down pin.

This ROM is supplied in a 28-pin dual-in-line plastic (N suffix) package designed for insertion in mounting-hole rows on 15,24-mm (600-mil) centers. It is also supplied in a 32-lead plastic leaded chip carrier package using 1,25-mm (50-mil) lead spacing. Both package styles conform to JEDEC standards. The device is designed for operation from 0°C to 70°C.

PIN NOMENCLATURE	
A0-A16	Address Inputs
Ē/E	Chip Enable/Power Down
NC	No Connection
NU	Make No Internal Connection
Q1-Q8	Data Out
V_{CC}	5-V Supply
V_{SS}	Ground

operation

address (A0-A16)

The address-valid interval determines the device cycle time. The 17-bit positive-logic address is decoded on-chip to select one of 131,072 words of 8-bit length in the memory array. A0 is the least-significant bit and A16 is the most-significant bit of the word address.

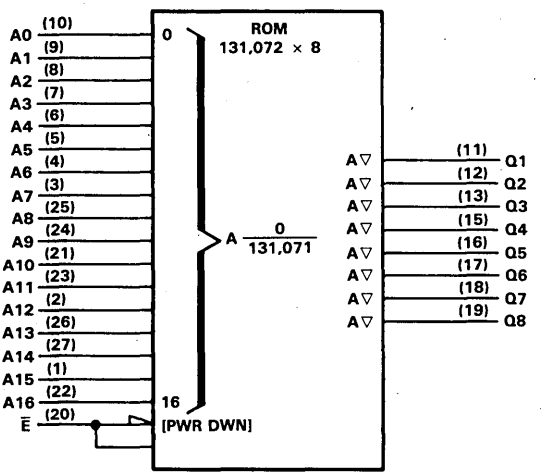
chip-enable/power down ($\overline{E}$ or E)

The chip-enable/power-down pin can be programmed during mask fabrication to be active with either a high- or low-level input. When the signal on the chip-enable/power-down pin is active, all eight outputs are enabled; and the 8-bit addressed word can be read. When the signal on the chip-enable/power-down pin is not active, all eight outputs are in a high-impedance state and the device goes into a standby current mode.

data out (Q1-Q8)

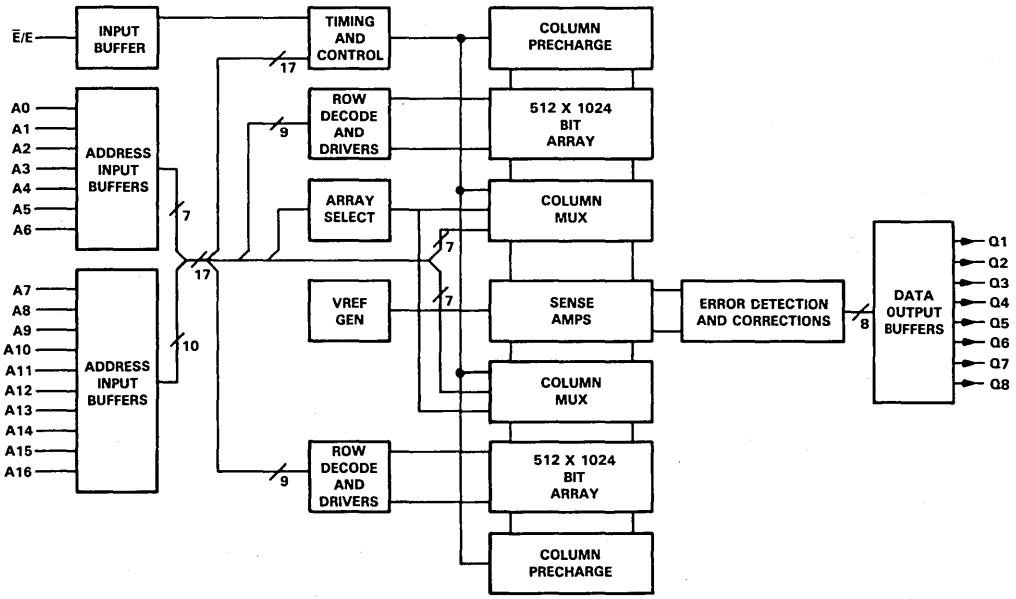
The eight outputs must be enabled by the chip-enable/power-down pin before the output word can be read. Data will remain valid until the address is changed or the outputs are disabled (chip deselected). When disabled, the three-state outputs are in a high-impedance state. Q1 is considered the least-significant bit, Q8 the most-significant bit.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
The pin numbers shown are for the 28-pin dual-in-line package. Pin 20 can be active low as shown in the symbol above or active high.

functional block diagram



absolute maximum ratings

Supply voltage to ground potential (see Note 1) . . . . . −0.5 V to 7 V
Applied output voltage (see Note 1) . . . . . −0.3 V to V_{CC} + 0.3 V
Applied input voltage (see Note 1) . . . . . −0.3 V to V_{CC} + 0.3 V
Power dissipation . . . . . T.B.D.
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 150°C

NOTE 1: Voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2		V_{CC}	V
V_{IL}	Low-level input voltage	−0.5		0.8	V
T_A	Operating free-air temperature	0		70	°C

Additional information on these products can be obtained from the factory as it becomes available.

electrical characteristics, T_A = 0°C to 70°C, V_{CC} = 5 V ±10% (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = 4.5 V,	I_{OH} = −400 μA	2.4		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5 V,	I_{OL} = 2.1 mA		0.4	V
I_I	Input leakage current	V_{CC} = 5.5 V,	0 V ≤ V_{IN} ≤ 5.5 V		±10	μA
I_O	Output leakage current	V_O = 0.4 V to V_{CC},	Chip deselected		±10	μA
I_{CC1}	Supply current from V_{CC} (active)	V_{CC} = 5.5 V,	V_I = V_{CC} Output not loaded		T.B.D.	
I_{CC2}	Supply current from V_{CC} (standby)	V_{CC} = 5.5 V			T.B.D.	
C_i	Input capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		10	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		15	pF

switching characteristics, T_A = 0°C to 70°C, V_{CC} = 5 V ±10% (see Figure 1)†

PARAMETER		TMS47C1024-20		TMS47C1024-25		TMS47C1024-30		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address		200		250		300	ns
$t_{a(E)}$	Access time from chip enable		200		250		300	
$t_{v(A)}$	Output data valid after address change	0		0		0		
t_{dis}	Output disable time from chip enable		100		100		100	

†All AC measurements are made at 10% and 90% points.

PARAMETER MEASUREMENT INFORMATION

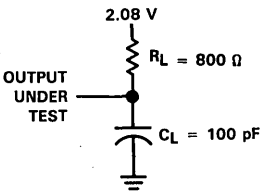


FIGURE 1. LOAD CIRCUIT

Additional information on these products can be obtained from the factory as it becomes available.

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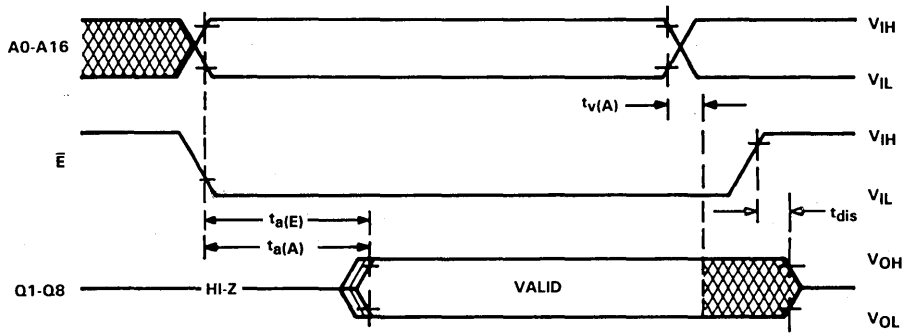
read cycle timing



PROGRAMMING REQUIREMENTS AND CODE ACQUISITION

PROGRAMMING REQUIREMENTS: The TMS47C1024 is a fixed-program memory in which the programming is performed by TI at the factory during the manufacturing cycle to the specific customer code inputs supplied. The device is organized as 131,072 8-bit words with address locations numbered 0 to 131,071. The 8-bit words can be coded as a 2-digit hexadecimal number between 00 and FF. Q1 is considered the least-significant bit and Q8 the most-significant bit. For addresses, A0 is the least-significant bit and A16 is the most-significant bit.

CODE ACQUISITION: The input media containing the customer programming data can be in the form of EPROMs, or data formatted in card images and transmitted via computer modem (contact TI for details on card image transmission). Either 64K, 128K, 256K, 512K, or 1024K EPROMS can be used or any combination of them to supply the customer data. In addition to the input media, the information requested in Table 1 is required at the same time in order to insure proper programming of device options and accurate data control.

TABLE 1. CUSTOMER/DEVICE INFORMATION

CUSTOMER: _____
SPECIFICATION NUMBER: _____
ROM CODE NAME: _____ ROM CODE CHECKSUM: _____

CUSTOMER PART NUMBER/SYMBOLIZATION:
CUSTOMER IS ALLOWED TWO (2) LINES OF UP TO 15 ALPHANUMERIC CHARACTERS PER LINE _____ _____

ADDRESS ACCESS TIME (SPEED): _____

PACKAGE TYPE: PLASTIC (N) _____ SURFACE MOUNT (FM)_____

PIN OPTIONS: 1 = HIGH, 0 = LOW

N PACKAGE: PIN 20: _____
PLCC: PIN 23 _____

ATTENTION

These devices contain circuits to protect the inputs and outputs against damage due to high static voltages or electrostatic fields; however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits.

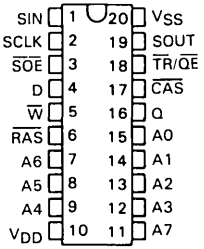
Unused inputs must always be connected to an appropriate logic voltage level, preferably either supply voltage or ground.

Additional information concerning the handling of ESD sensitive devices is provided in Section 12 in a document entitled *"Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies."*

NOVEMBER 1985

- MIL-STD-883C High-Reliability Processed and −55°C to 100°C (S Designator) Temperature Range, 20-Pin 300-Mil Ceramic Sidebrazed Package
- Dual Accessibility — One Port Sequential Access, One Port Random Access
- Four Cascaded 64-Bit Serial Shift Registers for Sequential Access Applications
- Designed for both Video and Non-Video Applications
- Fast Serial Port . . . Can Be Configured for Video Data Rates in Excess of 150 MHz
- $\overline{TR}/\overline{QE}$ as Output Enable Allows Direct Connection of D, Q and Address Lines to Simplify System Design
- Random-Access Port Looks Exactly Like a SMJ4164
- Separate Serial In and Serial Out to Allow Simultaneous Shift In and Out
- 65,536 × 1 Organization
- Supported by TI's Video System Controller (VSC)
- Maximum Access Time from $\overline{RAS}$ Less Than 150 ns
- Minimum Cycle Time (Read or Write) Less Than 240 ns
- Long Refresh Period . . . 4 ms
- Low Refresh Overhead Time . . . As Low As 1.7% of Total Refresh Period
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Unlatched Outputs for Both Random and Serial Access
- Common I/O Capability with Early Write Feature
- Page-Mode Operation for Faster Access
- Low Power Dissipation (SMJ4161-15)
  - Operating . . . 250 mW (Typical)
  - Standby . . . 80 mW (Typical)
- New SMOS (Scaled-MOS) N-Channel Technology
- $\overline{SOE}$ Simplifies Multiplexing of Serial Data Streams

JD PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A7	Address Inputs
$\overline{CAS}$	Column-Address Strobe
D	Random-Access Data In
Q	Random-Access Data Out
$\overline{RAS}$	Row-Address Strobe
SCLK	Serial Data Clock
SIN	Serial Data In
$\overline{SOE}$	Serial Output Enable
SOUT	Serial Data Out
$\overline{TR}/\overline{QE}$	Register Transfer/Q Output Enable
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The SMJ4161 is a high-speed, dual-access 65,536-bit dynamic random-access memory. The random-access port makes the memory look like it is organized as 65,536 words of one bit each like the SMJ4164. The sequential access port is interfaced to an internal 256-bit dynamic shift register organized as four cascaded 64-bit shift registers which makes the memory look like it is organized as up to 256 words of up to 256 bits each which are accessed serially. One, two, three, or four 64-bit shift registers can be sequentially read out after a transfer cycle depending on a two-bit code applied to the two most significant column address inputs. The SMJ4161 employs state-of-the-art SMOS (Scaled-MOS) N-channel double-level polysilicon gate technology for very high performance combined with low cost and improved reliability.

The SMJ4161 features full asynchronous dual access capability except when transferring data between the shift register and the memory array.

Refresh period is extended to 4 milliseconds, and during this period each of the 256 rows must be strobed with $\overline{RAS}$ in order to retain data. $\overline{CAS}$ can remain high during the refresh sequence to conserve power. Note that the transfer of a row of data from the memory array to the shift register also refreshes that row.

All inputs and outputs, including clocks, are compatible with Series 54 TTL. All address lines and data in are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The SMJ4161 is offered in a 20-pin ceramic dual-in-line package. It is guaranteed for operation from T_A = −55°C to T_C = 100°C. The dual-in-line package is designed for insertion in mounting-hole rows on 7,62-mm (300-mil) centers.

random access address space to sequential address space mapping

The SMJ4161 is designed with each row divided into four, 64-column sections (see functional block diagram). The first column section to be shifted out is selected by the two most significant column address bits. If the two bits represent binary 00, then one to four registers can be shifted out in order. If the two bits represent binary 01, then only 1 to 3 (the most significant) registers can be shifted out in order. If the two bits represent binary 10, then one to two of the most significant registers can be shifted out in order. Finally, if the two bits represent 11 only the most significant register can be shifted out. All registers are shifted out with the least significant bit (bit 0) first and the most significant bit (bit 63) last. Note that if the two column address bits equal 00 during the last register transfer cycle ($\overline{TR}/\overline{QE}$ at logic level "0" as $\overline{RAS}$ falls) a total fo 256 bits can be sequentially read out.

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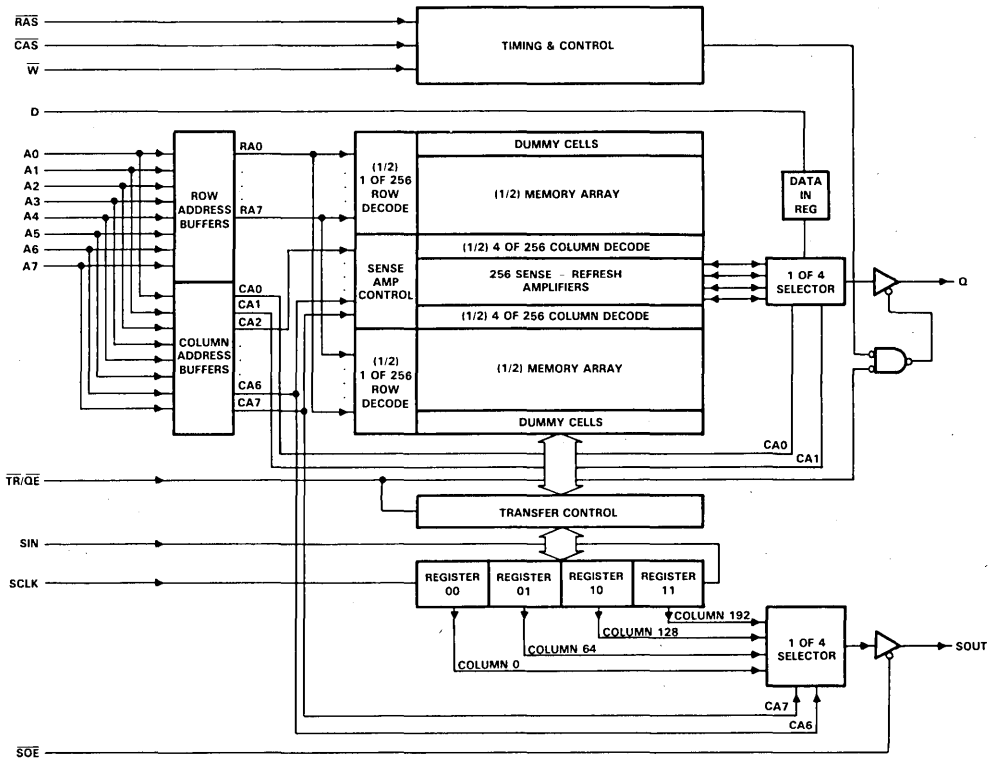
functional block diagram



random-access operation

TR/QE

The TR/QE pin has two functions. First, it selects either register transfer or random-access operation as RAS falls, and second, if this is a random-access operation, it functions as an output enable after CAS falls.

To use the SMJ4161 in the random-access mode, TR/QE must be high as RAS falls, Holding TR/QE high as RAS falls keeps the 256 elements of the shift registers disconnected from the corresponding 256 bit lines of the memory array. If data is to be transferred, the shift registers must be connected to the bit lines. Holding TR/QE low as RAS falls enables the 256 switches that connect the shift registers to the bit lines and indicates that a transfer will occur between the shift registers and one of the memory rows.

During random-access operation, once CAS has been pulled low, TR/QE controls when the data will appear at the Q output (if this is a read cycle). Whenever TR/QE is held high during random-access operation, the Q output will be in the high-impedance state. This feature removes the possibility of an overlap between data on the address lines and data appearing on the Q output making it possible to connect the address lines to the Q and D lines (Use of this organization prohibits the use of the early write cycle.).

address (A0 through A7)

Sixteen address bits are required to decode 1 of 65,536 storage cell locations. Eight row-address bits are set up on pins A0 through A7 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the eight column-address bits are set up on pins A0 through A7 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the write enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$, data out will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data in (D)

Data is written during a write or read-modify-write cycle. The falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. This latch can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data out (Q)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan out of two Series 54 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state as long as $\overline{CAS}$ or $\overline{TR/QE}$ is held high. Data will not appear on the output until after both $\overline{CAS}$ and $\overline{TR/QE}$ have been brought low. In a read cycle, the guaranteed maximum output enable access time time is valid only if t_{CQE} is greater than t_{CQE} MAX, and t_{RLCL} is greater than t_{RLCL} MAX. Likewise, $t_{a(C)}$ MAX is valid only if t_{RLCL} is greater than t_{RLCL} MAX. Once the output is valid, it will remain valid while $\overline{CAS}$ and $\overline{TR/QE}$ are both low; $\overline{CAS}$ or $\overline{TR/QE}$ going high will return the output to a high-impedance state. In an early write cycle, the output is always in a high-impedance state. In a delayed write or read-modify-write cycle, the output will follow the sequence for the read cycle. In a register transfer cycle, the output will always be in a high-impedance state.

refresh

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffer is in high-impedance state unless $\overline{CAS}$ is applied, the $\overline{RAS}$-only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses (A0 through A7) with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power.

page mode

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the chip. Thus, the time required to setup and strobe sequential row addresses for the same page is eliminated. To extend beyond the 256 column locations on a single RAM, the row address and $\overline{RAS}$ are applied to multiple 64K RAMs. $\overline{CAS}$ is then decoded to select the proper RAM.

power up

After power up, the power supply must remain at its steady-state value for 1 ms. In addition, $\overline{RAS}$ must remain high for 100 μs immediately prior to initialization. Initialization consists of performing eight $\overline{RAS}$ cycles before proper device operation is achieved.

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sequental access operation

$\overline{TR}/\overline{QE}$

Memory transfer operations involving parallel use of the shift register are first indicated by bringing $\overline{TR}/\overline{QE}$ low before $\overline{RAS}$ falls low. This enables the switches connecting the 256 elements of the shift register to the 256 bit lines of the memory array. The $\overline{W}$ line determines whether the data will be transferred from or to the shift registers.

write enable ($\overline{W}$)

In the sequential access mode, $\overline{W}$ determines whether a transfer will occur from the shift registers to the memory array, or from the memory array to the shift registers. To transfer from the shift registers to the memory array, $\overline{W}$ is held low as $\overline{RAS}$ falls, and, to transfer from the memory array to the shift registers, $\overline{W}$ is held high as $\overline{RAS}$ falls. Thus, reads and writes are always with respect to the memory array. The write setup and hold times are referenced to the falling edge of $\overline{RAS}$ for this mode of operation.

row address (A0 through A7)

Eight address bits are required to select one of the 256 possible rows involved in the transfer of data to or from the shift registers. A0-A7, $\overline{W}$, and $\overline{TR}/\overline{QE}$ are latched on the falling edge of $\overline{RAS}$.

register column address (A7, A6)

To select one of the four shift registers (transfer from memory to register only), the appropriate 2-bit column address (A7, A6) must be valid when $\overline{CAS}$ falls. However, the $\overline{CAS}$ and register address signals need not be supplied every cycle, only when it is desired to change or select a new register.

SCLK

Data is shifted in and out on the rising edge of SCLK. This makes it possible to view the shift registers as though it were made of 256 rising edge D flip-flops connected D to Q. The SMJ4161 is designed to work with a wide range duty cycle clock to simplify system design. Note that data will appear at the SOUT pin not only on the rising edge of SCLK but also after an access time of $t_{a(RSO)}$ from $\overline{RAS}$ high during a parallel load of the shift registers.

SIN and SOUT

Data is shifted in through the SIN pin and is shifted out through the SOUT pin. The SMJ4161 is designed such that it requires 3 ns hold time on SIN as SCLK rises. SOUT is guaranteed not to change for at least 6 ns after SCLK rises. These features make it possible to easily connect SMJ4161s together, to allow SOUT to be connected to SIN, and to give external circuitry a full SCLK cycle time to allow manipulation of the serial data. If SOUT is connected to SIN, the SCLK cycle time must include $t_{su(SI)}$. When loading data into the shift register from the serial input in preparation for a shift-register-to-memory transfer operation, the serial clock must be clocked an even number of times. To guarantee proper serial clock sequence after power up, a transfer cycle must be initiated before a serial data stream is applied at SIN.

$\overline{SOE}$

The serial output enable pin controls the impedance of the serial output, allowing multiplexing of more than one bank of SMJ4161 memories into the same external video circuitry. When $\overline{SOE}$ is at a logic low level, SOUT will be enabled and the proper data read out. When $\overline{SOE}$ is at a logic high level, SOUT will be disabled and be in the high-impedance state.

refresh

The shift registers are also dynamic storage elements. The data held in the registers will be lost unless SCLK goes high to shift the data one bit position, a transfer write operation is invoked, or the data is reloaded from the memory array. See specifications for maximum register data retention times.

absolute maximum ratings over operating temperature range (unless otherwise noted)†

Voltage on any pin except V_{DD} and data out (see Note 1) . . . . . −1.5 V to 10 V
Voltage on V_{DD} supply and data out with respect to V_{SS} . . . . . −1 V to 6 V
Short circuit output current . . . . . 50 mA
Power dissipation . . . . . 1 W
Minimum operating free-air temperature . . . . . −55°C
Operating case temperature . . . . . 100°C
Storage temperature range . . . . . −65°C to 150°C

†Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	4.75	5	5.25	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		V_{DD}+0.3	V
V_{IL}	Low-level input voltage (see Notes 2 and 3)	−0.6		0.8	V
T_A	Operating free-air temperature	−55			°C
T_C	Operating case temperature			100	°C

NOTES: 2. The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.
3. Due to input protection circuitry, the applied voltage may begin to clamp at −0.6 V; test conditions must comprehend this occurrence.
4. See application report entitled "TMS4164A and TMS4416 Input Protection Diode" on page 9-5.

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electrical characteristics over full range of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SMJ4161-15			SMJ4161-20			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage (Q, SOUT)	I_{OH} = −5 mA	2.4			2.4			V
V_{OL}	Low-level output voltage (Q, SOUT)	I_{OL} = 4.2 mA			0.4			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 5.8 V, V_{DD} = 5 V, All other pins = 0 V			±10			±10	μA
I_O‡	Output current (leakage) (Q,SOUT)	V_O = 0.4 V to 5.5 V, V_{DD} = 5 V			±10			±10	μA
I_{DD1}	Average operating current during read or write cycle	$t_{c(rd)}$ = minimum cycle time, $\overline{TR}/\overline{QE}$ low after $\overline{RAS}$ falls,§ SCLK and SIN low, $\overline{SOE}$ high, No load on Q and SOUT		50	75		45	75	mA
I_{DD2}¶	Standby current	After 1 − $\overline{RAS}$ cycle, $\overline{RAS}$ and $\overline{CAS}$ high, SCLK and SIN low, $\overline{SOE}$ high, No load on Q and SOUT		16	25		16	25	mA
I_{DD3}	Average refresh current	$t_{c(rd)}$ = minimum cycle time, $\overline{CAS}$ high, $\overline{RAS}$ cycling, SCLK and SIN low, $\overline{SOE}$ high, $\overline{TR}/\overline{QE}$ high, No load on Q and SOUT		42	60		37	60	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle time, $\overline{RAS}$ low, $\overline{CAS}$ cycling, $\overline{TR}/\overline{QE}$ low after $\overline{RAS}$ falls, SCLK and SIN low, $\overline{SOE}$ high, No load on Q and SOUT		45	75		40	75	mA
I_{DD5}	Average shift register current (includes I_{DD2})	$\overline{RAS}$ and $\overline{CAS}$ high, No load on Q and SOUT, $t_{c(SCLK)}$ = $t_{c(SCLK)}$ min		30	45		30	45	mA
I_{DD6}	Worst case average DRAM and shift register current	$t_{c(rd)}$ = minimum cycle time, $t_{c(SCLK)}$ = minimum cycle time, $\overline{TR}/\overline{QE}$ low after $\overline{RAS}$ falls, No load on Q and SOUT		85	100		85	100	mA

†All typical values are at T_A = 25°C and nominal supply voltages.
‡SOUT output current (leakage) is guaranteed but not tested.
§See appropriate timing diagram.
¶V_{IL} > −0.6 V.

capacitance over recommended supply voltage and operating temperature range, f = 1 MHz

PARAMETER		TYP†	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs	4		pF
$C_{i(D)}$	Input capacitance, data input	4		
$C_{i(RC)}$	Input capacitance, strobe inputs	8		
$C_{i(W)}$	Input capacitance, write enable input	8		
$C_{i(CK)}$	Input capacitance, serial clock	8		
$C_{i(SI)}$	Input capacitance, serial in	4		
$C_{i(SOE)}$	Input capacitance, serial output enable	4		
$C_{i(TR)}$	Input capacitance, register transfer input	4		
$C_{o(Q)}$	Output capacitance, random-access data	5		
$C_{o(SOUT)}$	Output capacitance, serial out	5		

†All typical values are at T_A = 25°C and nominal supply voltages.

switching characteristics over recommended supply voltage range and operating temperature range (see Figure 1)

PARAMETER		TEST CONDITIONS†	ALT. SYMBOL	SMJ4161-15		SMJ4161-20		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 80 pF, I_{OL} = 4.2 mA, I_{OH} = −5 mA	t_{CAC}		100		135	ns
$t_{a(QE)}$	Access time of Q from $\overline{TR}/\overline{QE}$ low				40		50	
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = max, C_L = 80 pF, I_{OL} = 4.2 mA, I_{OH} = −5 mA	t_{RAC}		150		200	
$t_{a(RSO)}$	SOUT access time from $\overline{RAS}$ high	C_L = 80 pF, I_{OL} = 4.2 mA, I_{OH} = −5 mA			65		85	
$t_{a(SOE)}$	Access time from $\overline{SOE}$ low to SOUT				45		50	
$t_{a(SO)}$	Access time from SCLK				45		55	
$t_{dis(CH)}$	Q output disable time from $\overline{CAS}$ high		t_{OFF}		40		40	
$t_{dis(QE)}$	Q output disable time from $\overline{TR}/\overline{QE}$ high				30		40	
$t_{dis(SOE)}$	Serial output disable time from $\overline{SOE}$ high				20		25	

†Figure 1 shows the load circuit; C_L values shown are typical for test system used.

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timing requirements over recommended supply voltage range and operating temperature range

		ALT. SYMBOL	SMJ4161-15		SMJ4161-20		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(P)}$	Page-mode cycle time	t_{PC}	160		225		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	240		315		ns
$t_{c(W)}$	Write cycle time	t_{WC}	240		315		ns
$t_{c(TW)}$	Transfer write cycle time‡		240		315		ns
$t_{c(Trd)}$	Transfer read cycle time		240		315		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	265		330		ns
$t_{c(SCLK)}$	Serial clock cycle time (see Note 5)	t_{SCC}	45	50,000	55	50,000	ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (precharge time)§	t_{CP}	50		80		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low¶	t_{CAS}	100	10,000	135	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge time)	t_{RP}	80		105		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low#	t_{RAS}	150	10,000	200	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	45		45		ns
$t_{w(CKL)}$	Pulse duration, SCLK low‖		20		20		ns
$t_{w(CKH)}$	Pulse duration, SCLK high‖		20		20		ns
$t_{w(QE)}$	$\overline{TR}/\overline{QE}$ pulse duration low time (read cycle)		50		50		ns
$t_{su(CA)}$	Column address setup time	t_{ASC}	0		0		ns
$t_{su(RA)}$	Row address setup time	t_{ASR}	0		0		ns
$t_{su(RW)}$	$\overline{W}$ setup time before $\overline{RAS}$ low with $\overline{TR}/\overline{QE}$ low		0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		ns
$t_{su(rd)}$	Read command setup time	t_{RCS}	5		5		ns
$t_{su(WCL)}$	Early write command setup time before $\overline{CAS}$ low	t_{WCS}	−5		−5		ns
$t_{su(WCH)}$	Write command setup time before $\overline{CAS}$ high	t_{CWL}	40		60		ns
$t_{su(WRH)}$	Write command setup time before $\overline{RAS}$ high	t_{RWL}	40		60		ns
$t_{su(TR)}$	$\overline{TR}/\overline{QE}$ setup time before $\overline{RAS}$ low		5		5		ns
$t_{su(SI)}$	Serial data setup time before SCLK high		6		6		ns
$t_{h(SI)}$	Serial data in hold time after SCLK high		3		3		ns
$t_{h(CLCA)}$	Column address hold time after $\overline{CAS}$ low	t_{CAH}	45		55		ns
$t_{h(RA)}$	Row address hold time	t_{RAH}	20		25		ns
$t_{h(RW)}$	$\overline{W}$ hold time after $\overline{RAS}$ low with $\overline{TR}/\overline{QE}$ low		30		30		ns
$t_{h(RLCA)}$	Column address hold time after $\overline{RAS}$ low	t_{AR}	95		120		ns

Continued next page.

NOTES: 5. $t_{c(SCLK)}$ min is tested by connecting SIN to SOUT and test conditions include $t_{su(SI)}$, see paragraph entitled SIN and SOUT on page 5.

6. Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, V_{IL} max and V_{IH} min must be met at the 10% and 90% points.

7. System transition times (rise and fall) for $\overline{RAS}$, $\overline{CAS}$, and SCLK are to be a minimum of 3 ns and a maximum of 50 ns.

†All cycle times assume t_t = 5 ns except $t_{c(SCLK)}$ which assumes t_t = 3 ns.

‡Multiple transfer write cycles require separation by either a 1-μs $\overline{RAS}$-precharge interval or any other active $\overline{RAS}$-cycle.

§Page-mode only.

¶In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$). This applies to page-mode read-modify-write also.

#In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).

‖This parameter is guaranteed but not tested.

timing requirements over recommended supply voltage range and operating case temperature range (concluded)

		ALT. SYMBOL	SMJ4161-15		SMJ4161-20		UNIT
			MIN	MAX	MIN	MAX	
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	60		80		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	110		145		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	45		55		ns
$t_{h(CHrd)}$	Read command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		ns
$t_{h(RHrd)}$	Read command hold time after $\overline{RAS}$ high	t_{RRH}	5		5		ns
$t_{h(CLW)}$	Write command hold time after $\overline{CAS}$ low	t_{WCH}	60		80		ns
$t_{h(RLW)}$	Write command hold time after $\overline{RAS}$ low	t_{WCR}	110		145		ns
$t_{h(RSO)}$	Serial data out hold time after $\overline{RAS}$ low with $\overline{TR}/\overline{QE}$ low‖		30		30		ns
$t_{h(SO)}$	Serial data out hold time after SCLK high		6		6		ns
$t_{h(TR)}$	$\overline{TR}/\overline{QE}$ hold time after $\overline{RAS}$ low (transfer)		40		40		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	150		200		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
t_{CLQEH}	Delay time $\overline{CAS}$ low to QE high		100		135		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	100		135		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{CWD}	65		75		ns
t_{CQE}	Delay time, $\overline{CAS}$ low to QE low (maximum value specified only to guarantee $t_{a(QE)}$ access time)			60		85	ns
t_{RHSC}	Delay time, $\overline{RAS}$ high to SCLK high		80		80		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	25	50	30	65	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{RWD}	135		150		ns
t_{CKRL}	Delay time, SCLK high before $\overline{RAS}$ low with $\overline{TR}/\overline{QE}$ low☆		10		10		ns
$t_{rf(MA)}$	Refresh time interval, memory array	t_{REF1}		4		4	ms
$t_{rf(SR)}$	Refresh time interval, shift register□	t_{REF2}		50,000		50,000	ns

NOTE 6: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, V_{IL} max and V_{IH} min must be met at the 10% and 90% points.

‖This parameter is guaranteed but not tested.

☆SCLK may be high or low during $t_{w(RL)}$, but there cannot be any positive edge transitions on SCLK for a minimum of 10 ns prior to $\overline{RAS}$ going low with $\overline{TR}/\overline{QE}$ low (i.e., before a transfer cycle).

□See "refresh" on page 8-7.

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PARAMETER MEASUREMENT INFORMATION

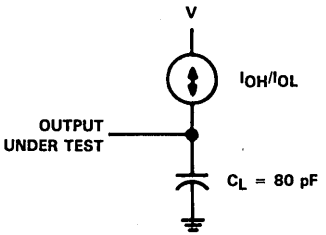
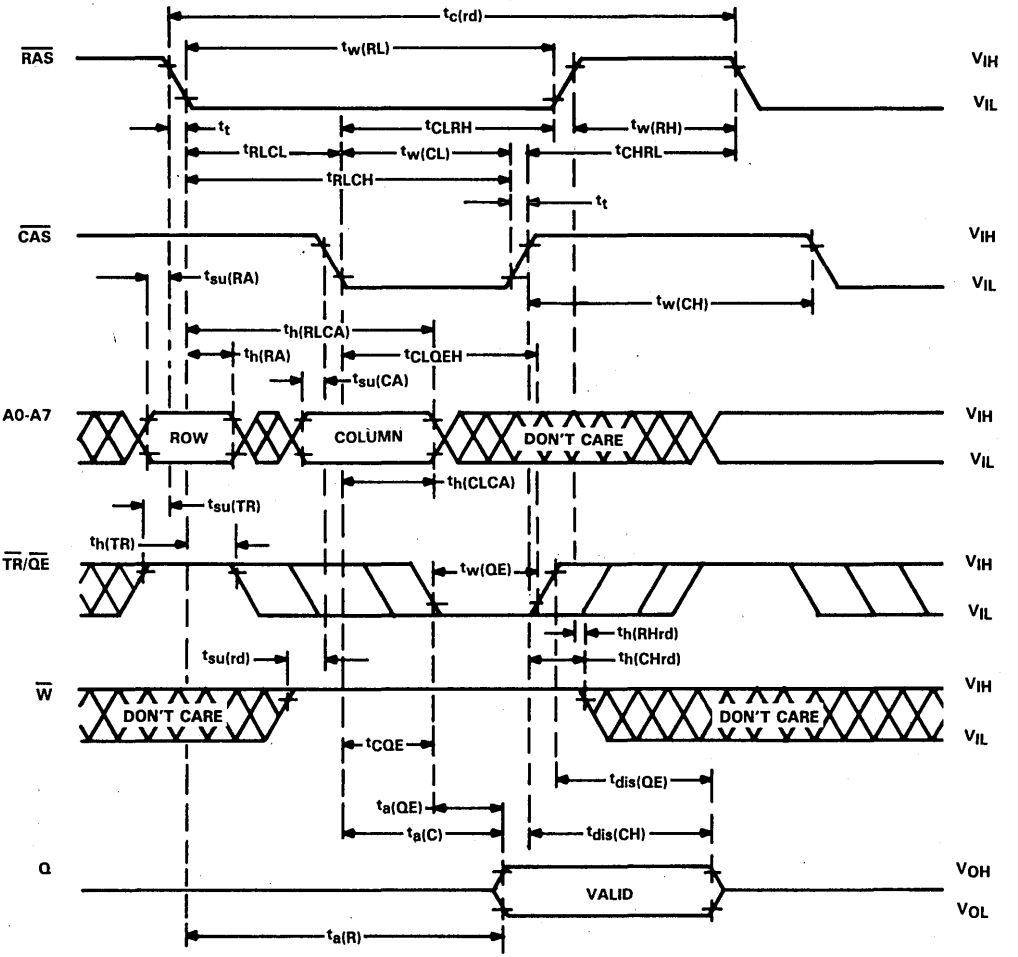


FIGURE 1. EQUIVALENT LOAD CIRCUIT

read cycle timing



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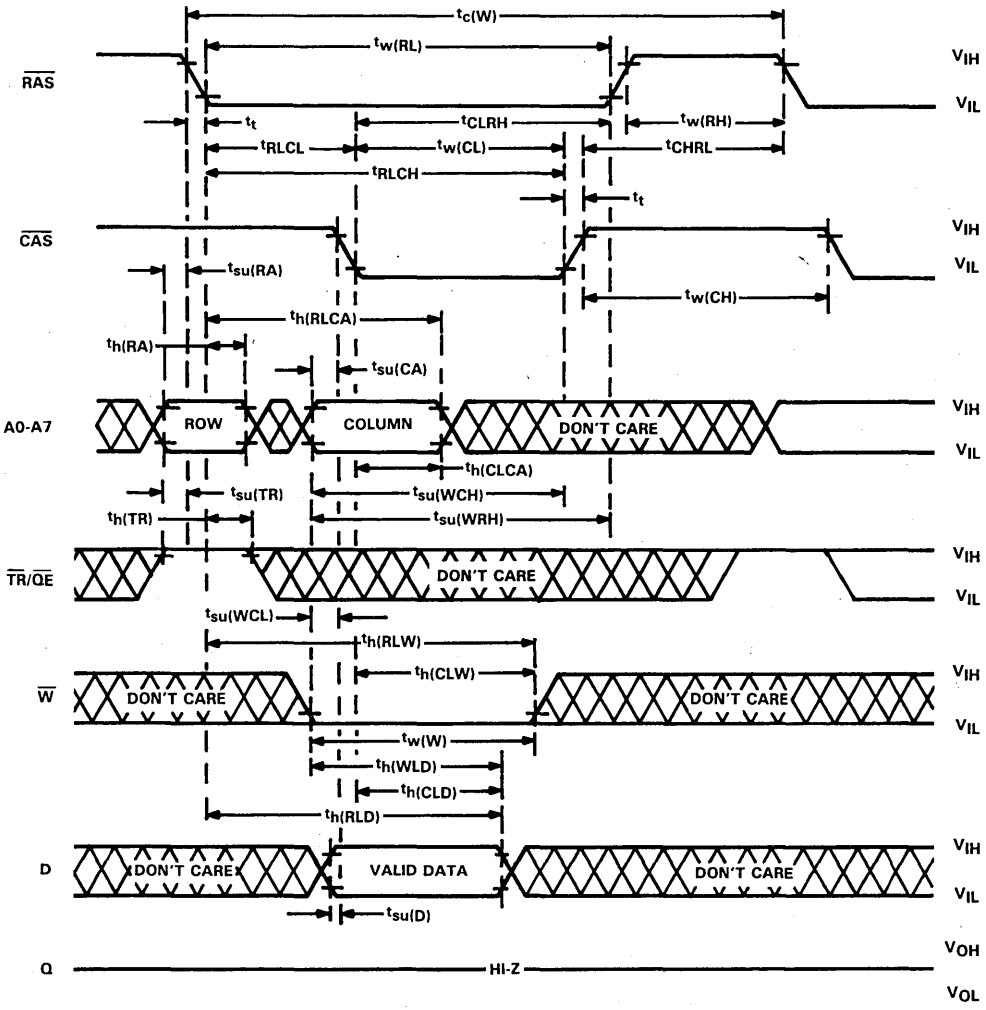
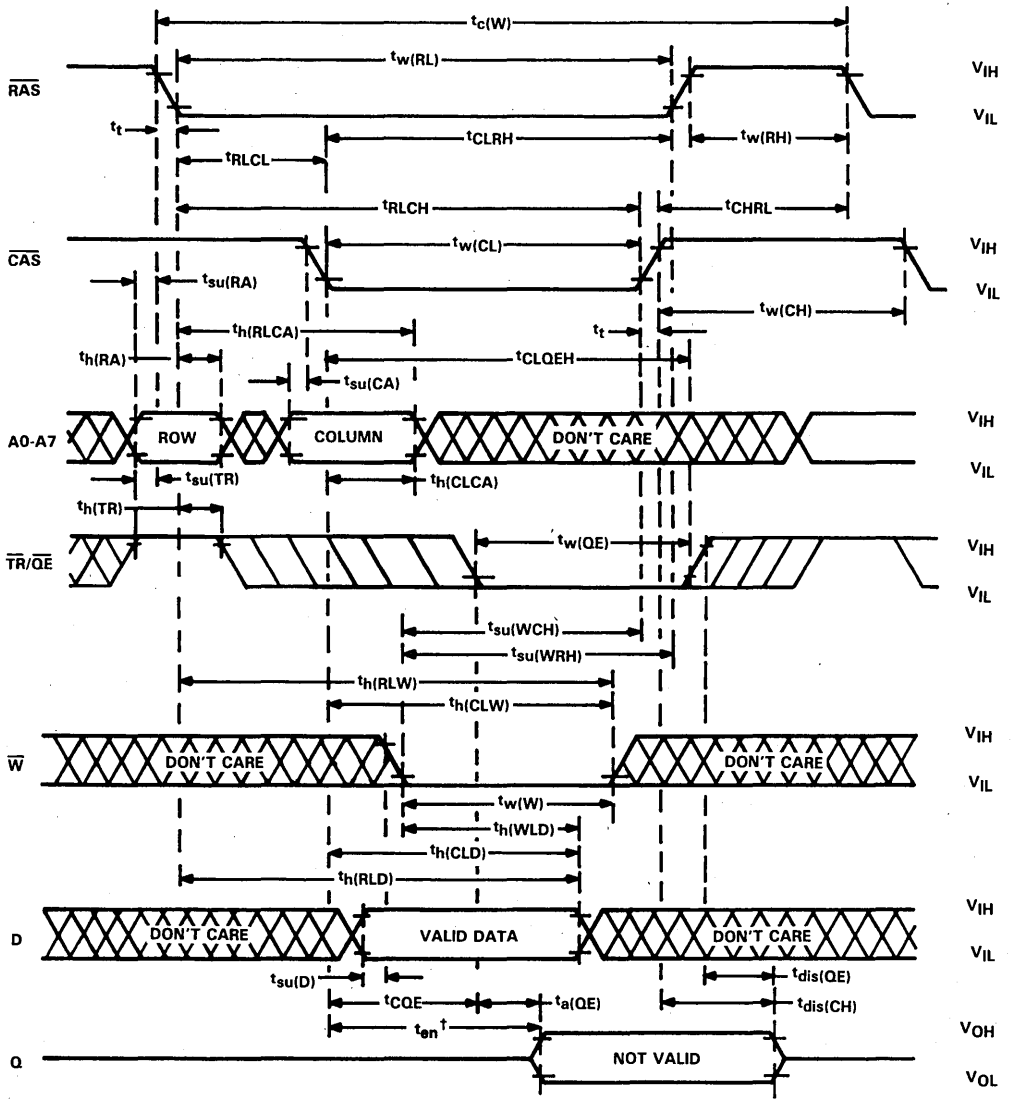
early write cycle timing



write cycle timing



†The enable time (t_{en}) for a write cycle is equal in duration to the access time from $\overline{CAS}$ ($t_{a(C)}$) in a read cycle; but the active levels at the output are invalid.

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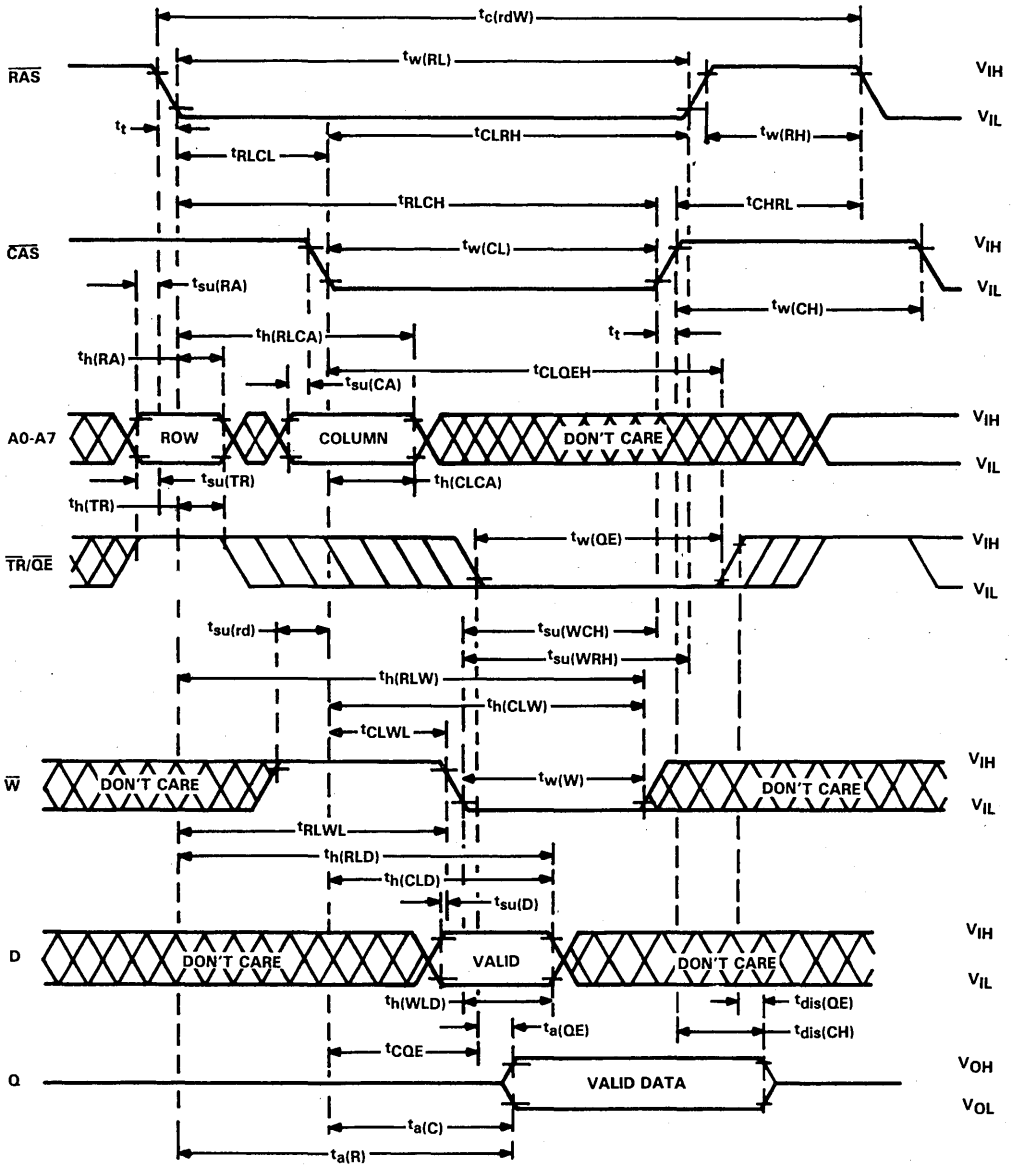
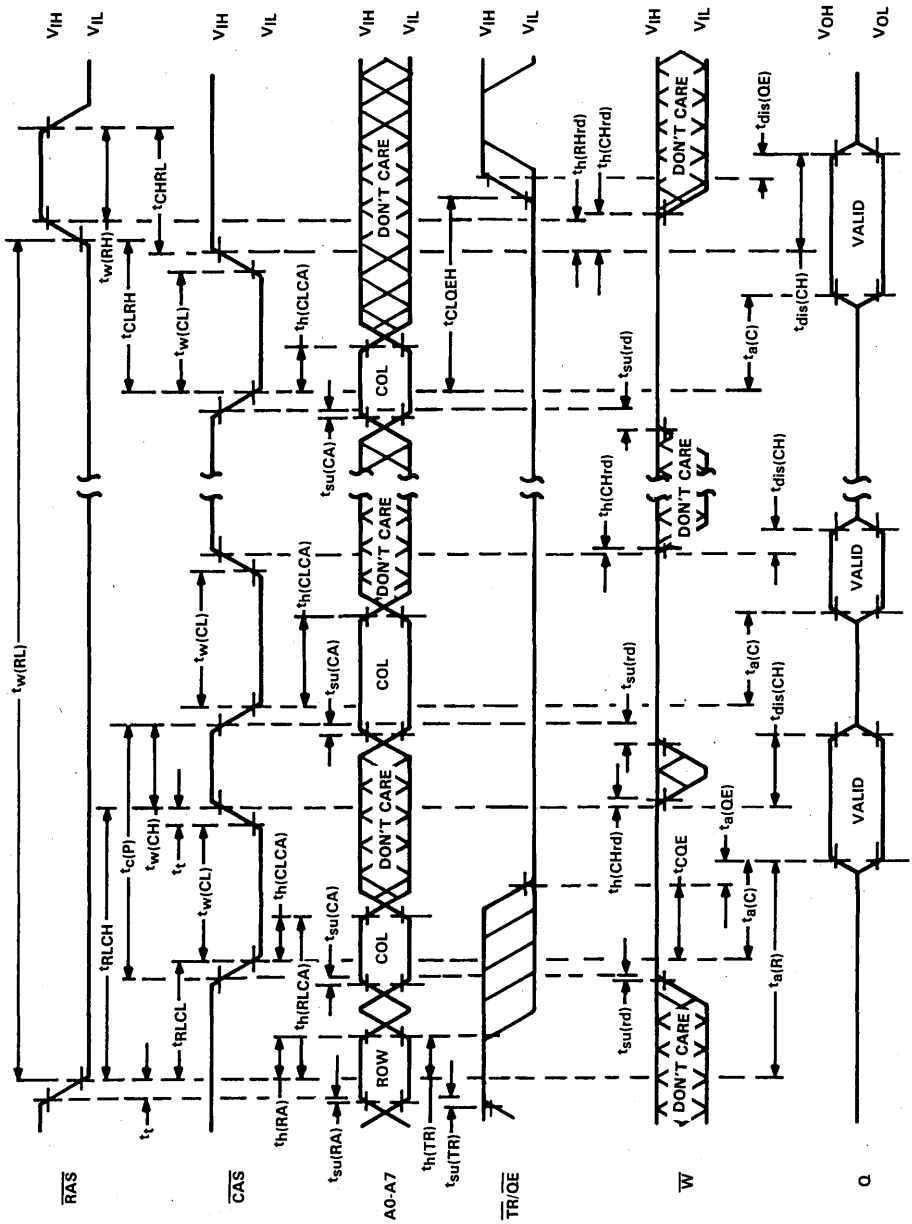
read-write/read-modify-write cycle timing



page-mode read cycle timing



NOTES: 8. Timing is for non-multiplexed D, Q, and Address lines.
9. A write cycle or a read-modify-write cycle can be intermixed with read cycles as long as the write and read-modify-write timing specifications are not violated.

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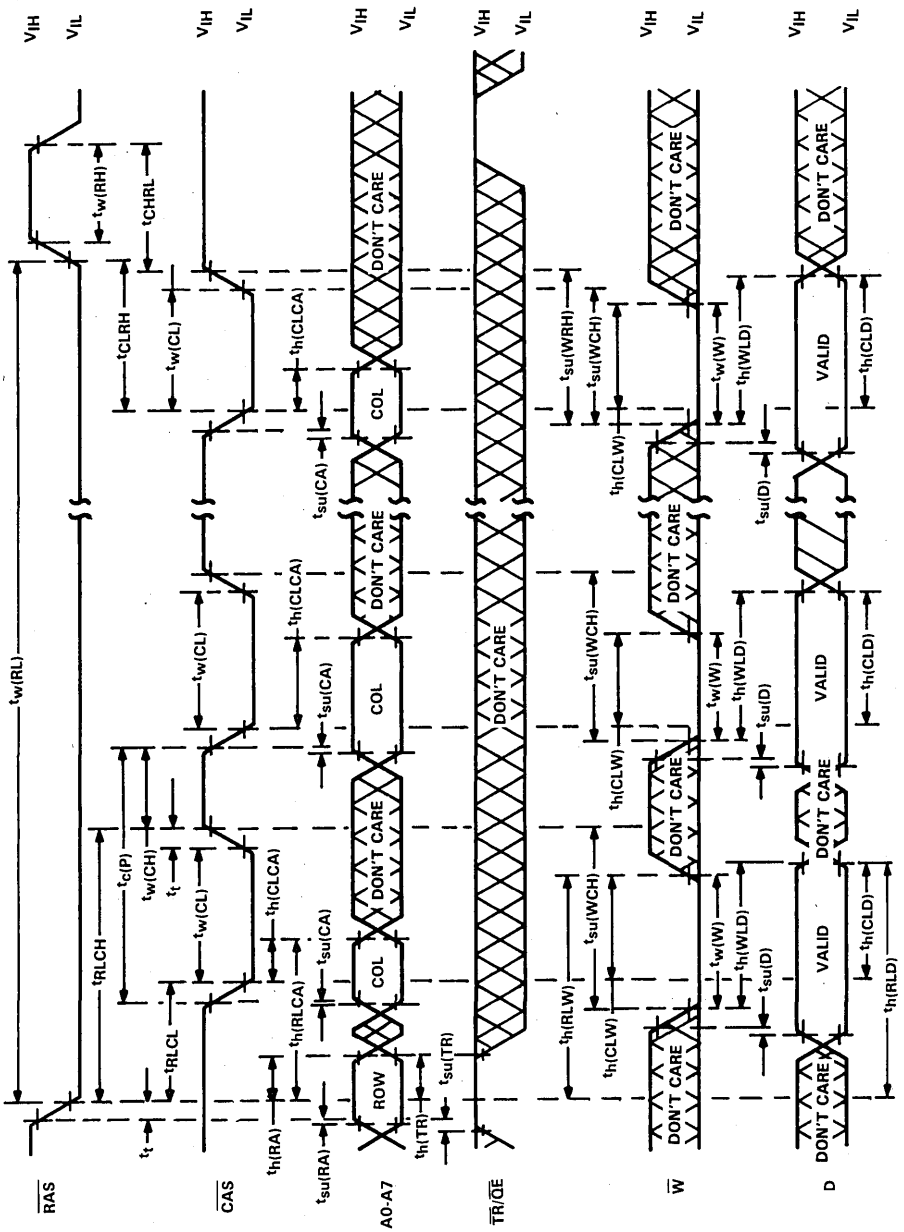
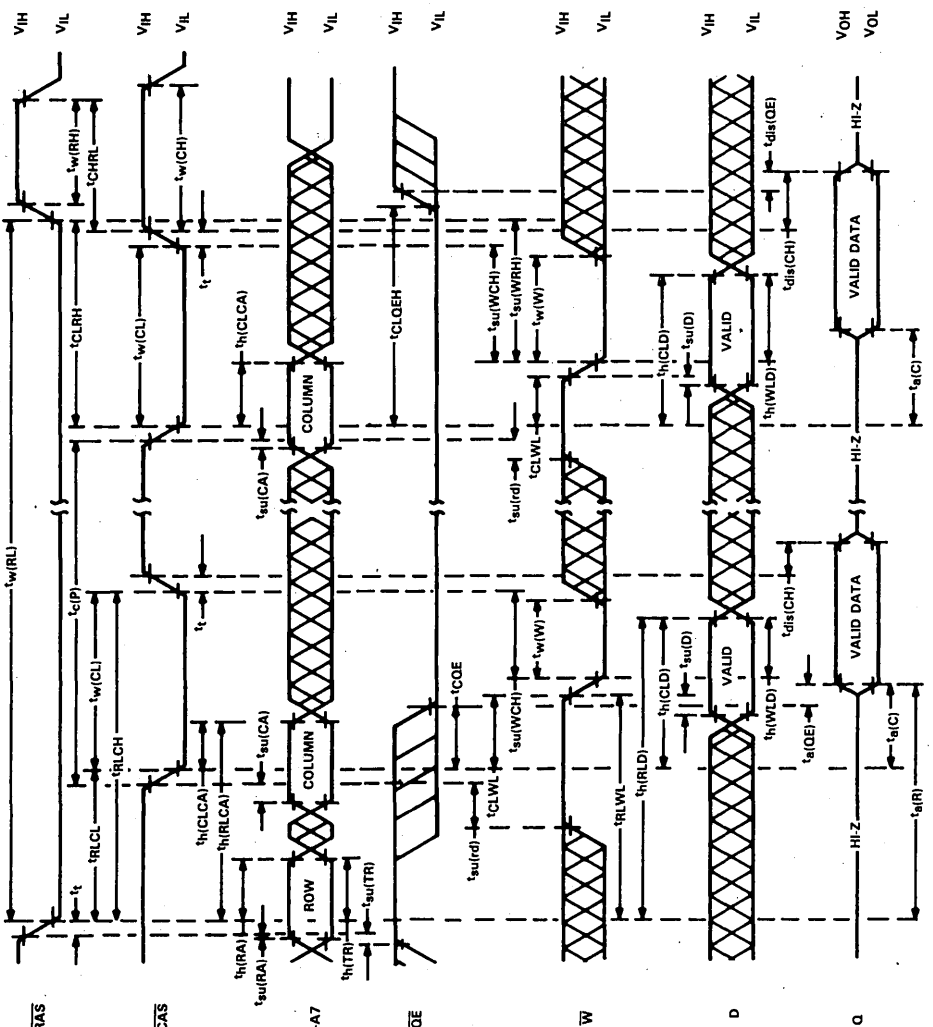
page-mode write cycle timing



NOTES: 8. Timing is for non-multiplexed D, Q, and Address lines.
10. A read cycle or a read-modify-write cycle can be intermixed with write cycles as long as the read and read-modify-write timing specifications are not violated.

page-mode read-modify-write cycle timing



NOTES: 8. Timing is for non-multiplexed D, Q, and Address lines.
11. A read cycle or a write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

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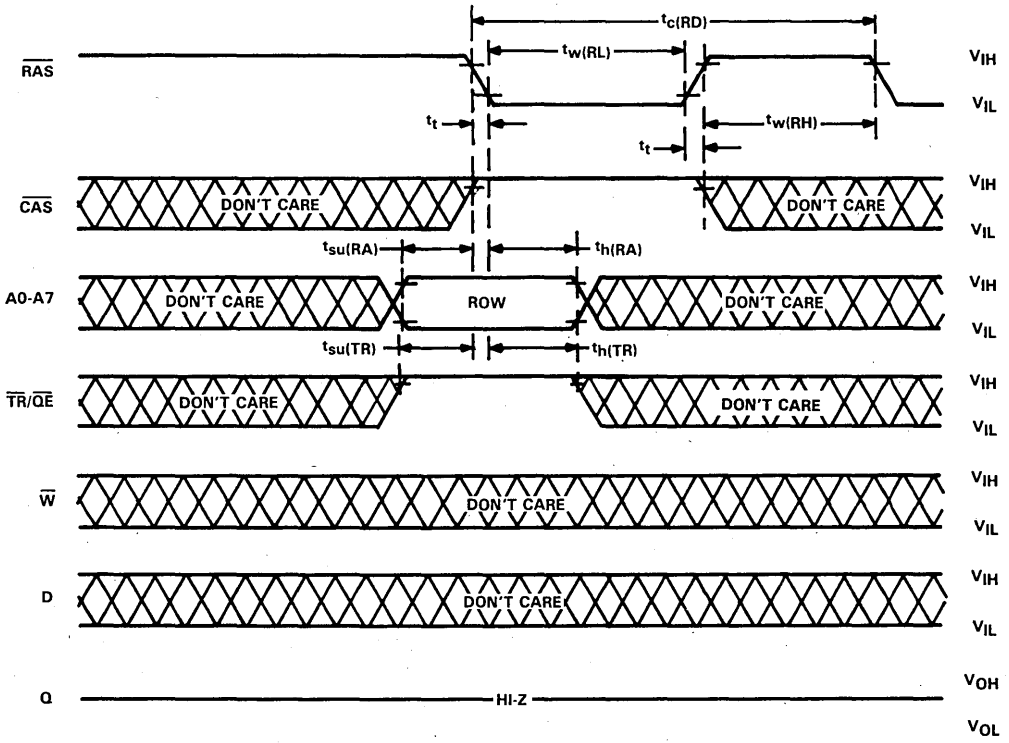
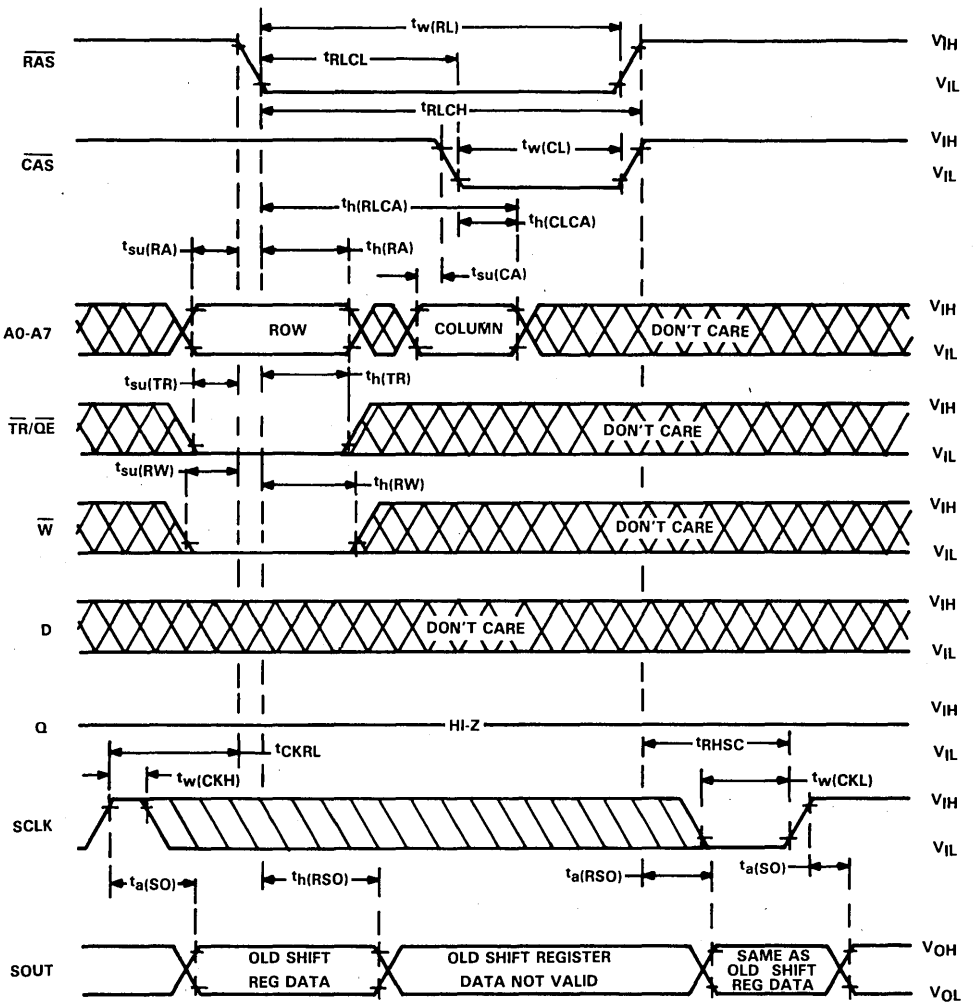
$\overline{\text{RAS}}$-only refresh timing



shift register to memory timing



NOTES: 12. The shift register to memory cycle is used to tranfer data from the shift register to the memory array. Every one of the 256 locations in the shift register is written into the 256 columns of the selected row. Note that the data that was in the shift register may have resulted, either from a serial shift in or from a parallel load of the shift register from one of the memory array rows.

13. $\overline{SOE}$ assumed low.

14. SCLK may be high or low during $t_{w(RL)}$.

15. Multiple transfer write cycles require either a 1-μs $\overline{RAS}$-precharge interval or any other active $\overline{RAS}$ cycle before initiation of the transfer write cycles and separation between any two consecutive transfer write cycles.

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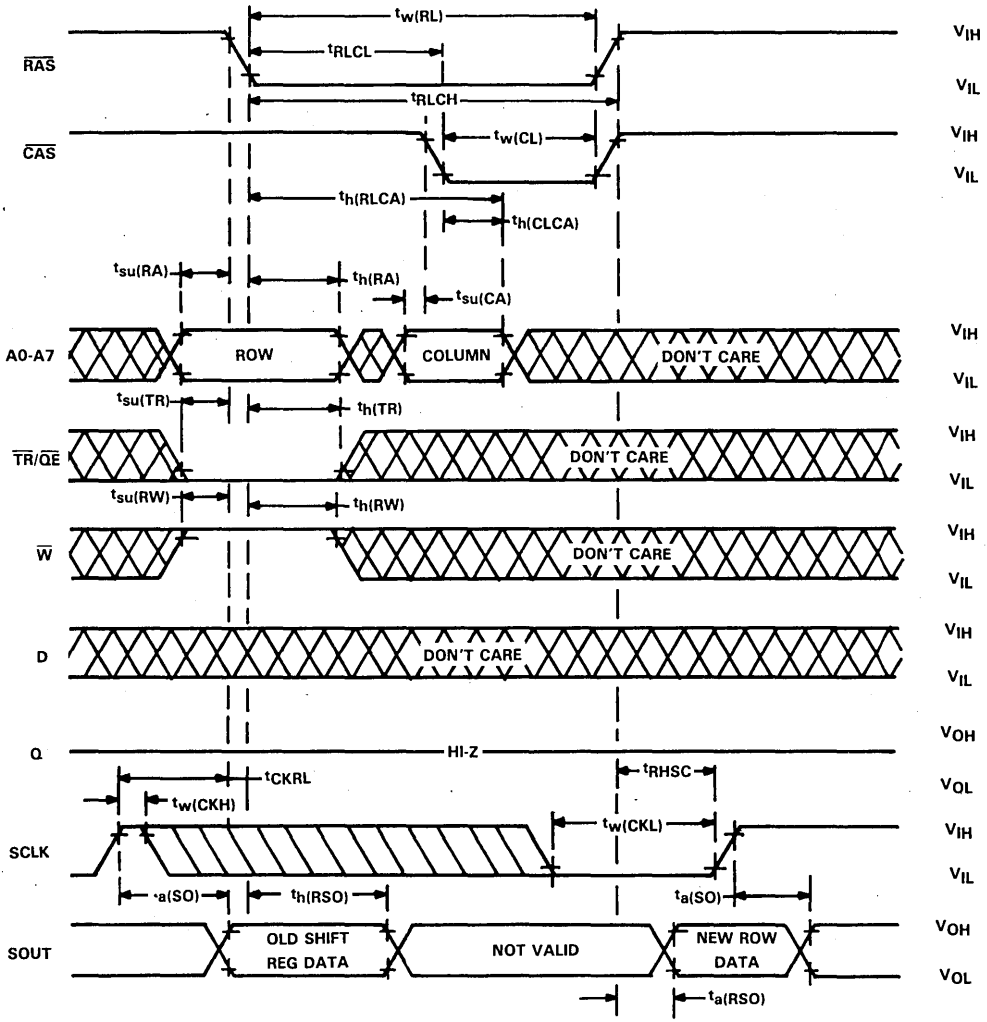
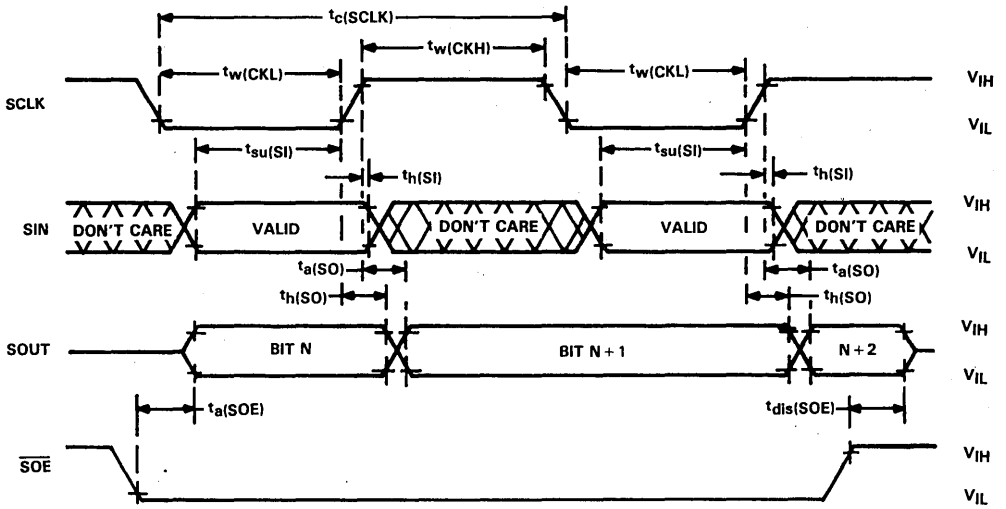
memory to shift register timing



NOTES: 13. $\overline{SOE}$ assumed low.
14. SCLK may be high or low during $t_{w(RL)}$.
15. Multiple transfer write cycles require either a 500-ns $\overline{RAS}$-precharge interval or any other active $\overline{RAS}$ cycle before initiation of the transfer write cycles and separation between any two consecutive transfer write cycles.
16. The memory to shift register cycle is used to load the shift register in parallel from the memory array. Every one of the 256 locations in the shift register are written into from the 256 columns of the selected row. Note that the data that is loaded into the shift register may be either shifted out or written back into another row.

serial data shift timing

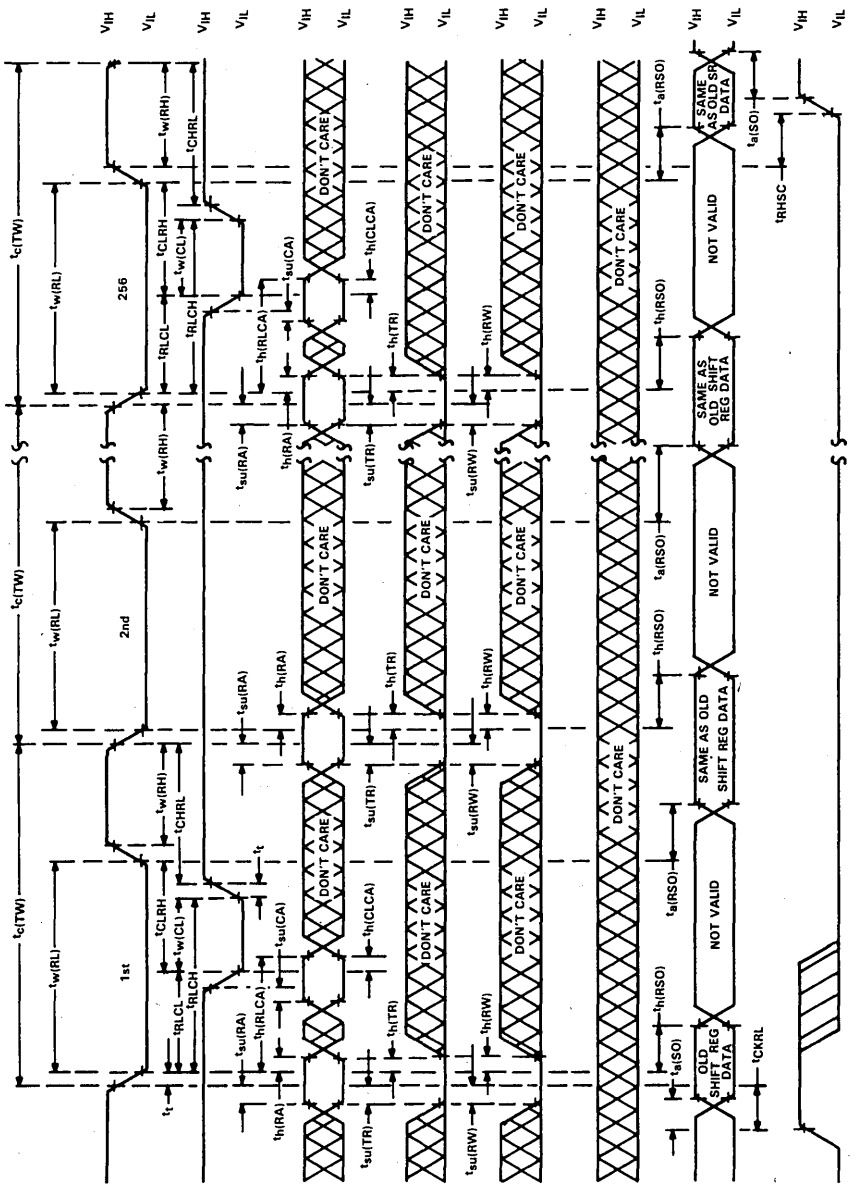


NOTES: 5. $t_{c(SCLK)}$ min is tested by connecting SIN to SOUT and test conditions include $t_{su(SI)}$, see paragraph entitled SIN and SOUT on page 5.

17. While shifting data through the serial shift register, the state of $\overline{TR}/\overline{QE}$ is a don't care as long as $\overline{TR}/\overline{QE}$ is held high when $\overline{RAS}$ goes low and $t_{su(TR)}$ and $t_{h(TR)}$ timings are observed. This requirement avoids the initiation of a register-to-memory or memory-to-register data transfer operation. The serial data transfer cycle is used to shift data in and/or out of the shift register.

18. When loading data into the shift register from the serial input in preparation for a shift-register-to-memory tranfer operation, the serial clock must be clocked an even number of times.

shift register to memory multiple timing



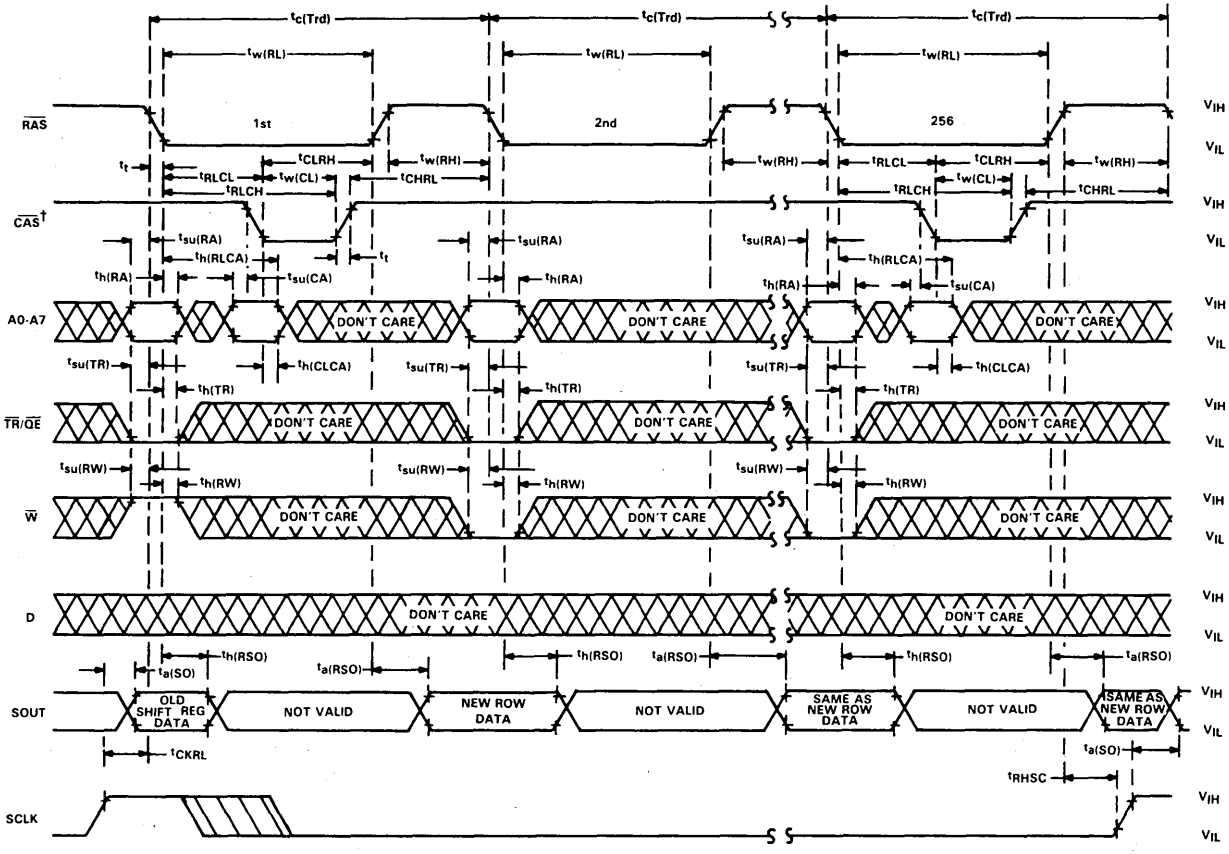
†$\overline{CAS}$ and register address need not be supplied every cycle, only when it is desired to change or select a new register length.

NOTES: 13. $\overline{SOE}$ assumed low.

19. The shift register to memory multiple cycle is used to write the shift register data to more than one row of the memory array. An application of this could be clearing all memory. To do this, the SIN line would be held at 0 to fill all locations in the shift register with 0's. The shift register would then be written into all 256 rows of the memory array in 256 cycles. The random output port Q will be in a high-impedance state as long as register transfer cycles are selected.

20. SCLK is a don't care except that no positive transitions on SCLK can occur for a period equal to t_{CKRL} prior to $\overline{RAS}$ falling with $\overline{TR}/\overline{QE}$ low.

memory to shift register to memory multiple timing



†$\overline{CAS}$ and register address need not be supplied every cycle, only when it is desired to change from one register to another.

NOTES: 13. $\overline{OE}$ assumed low.

20. SCLK is a don't care except that no positive transitions on SCLK can occur for a period equal to t_{CKRL} prior to $\overline{RAS}$ falling with $\overline{TR/QE}$ low.

21. The memory to shift register to memory multiple cycle is used to reorder the rows within the memory array itself. First, the data in a row is stored in the shift register and then it is written into other selected rows. The random output port Q will be in a high-impedance state as long as register transfer cycles are selected.

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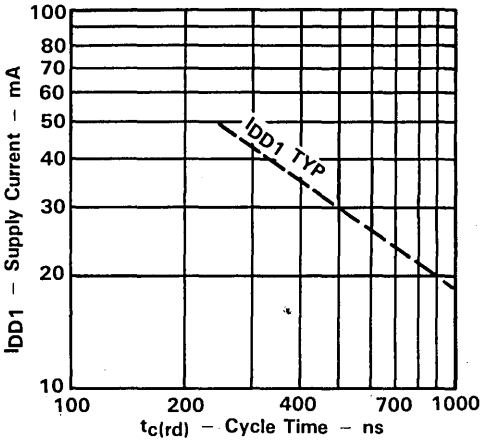
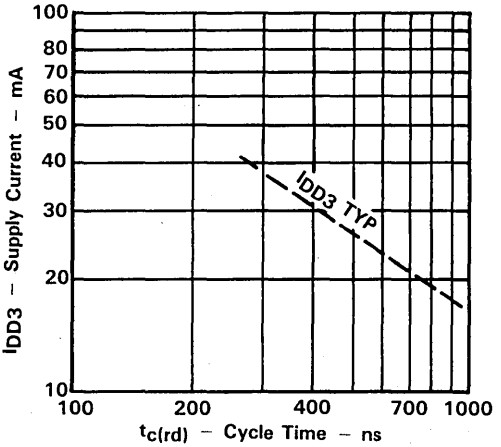
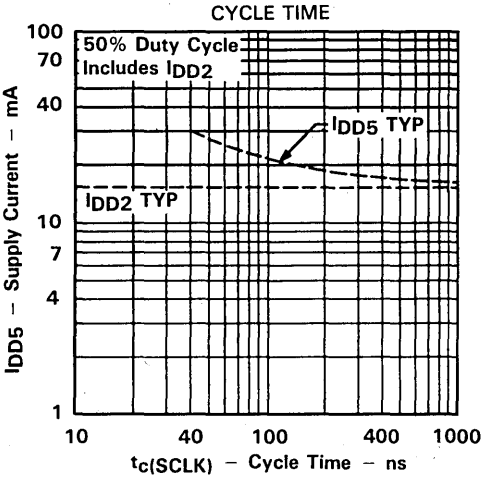
I_{DD1} vs CYCLE TIME



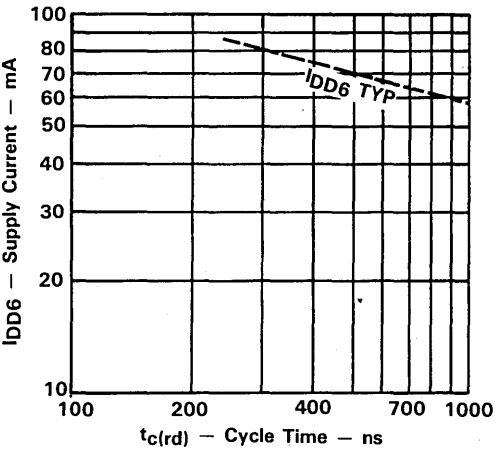
I_{DD3} vs CYCLE TIME



I_{DD5} vs CYCLE TIME



I_{DD6} vs CYCLE TIME



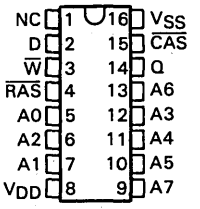
NOVEMBER 1985

- 65,536 X 1 Organization
- DESC Approved
  —SMJ4164-15JDS DESC No. 8201006EX
  —SMJ4164-20JDS DESC No. 8201007EX
- Single 5-V Supply (±10% Tolerance)
- JEDEC Standardized Pinout in Ceramic Dual-in-Line Package (JD Suffix)
- Upward Pin Compatible with '4116 (16K Dynamic RAM)
- Available Temperature Ranges with MIL-STD-883C High-Reliability Processing:
  —S . . . −55°C to 110°C
  —E . . . −40°C to 85°C
  —L . . . 0°C to 70°C
- Long Refresh Period . . . 4 ms
- Low Refresh Overhead Time . . . As Low As 1.8% of Total Refresh Period
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Unlatched Output
- Common I/O Capability with Early Write Feature
- Page-Mode Operation for Faster Access
- Low Power Dissipation
  —Operating . . . 125 mW (Typ)
  —Standby . . . 17.5 mW (Typ)
- Performance Ranges:

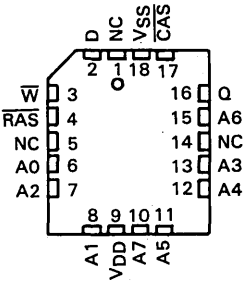
	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	READ-MODIFY-WRITE CYCLE (MIN)
'4164-12	120 ns	70 ns	230 ns	260 ns
'4164-15	150 ns	85 ns	260 ns	285 ns
'4164-20	200 ns	135 ns	326 ns	345 ns

- New SMOS (Scaled-MOS) N-Channel Technology

JD PACKAGE
(TOP VIEW)



FG PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A7	Address Inputs
$\overline{CAS}$	Column-Address Strobe
D	Data In
NC	No Connection
Q	Data Out
$\overline{RAS}$	Row-Address Strobe
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The SMJ4164 is a Military high-speed, 65,536-bit, dynamic random-access memory, organized as 65,536 words of one bit each. It employs state-of-the-art SMOS (scaled MOS) N-channel double-level polysilicon gate technology for very high performance combined with low cost and improved reliability.

The SMJ4164 features $\overline{RAS}$ access times of 120 ns, 150 ns, and 200 ns maximum. Power dissipation is 125 mW typical operating and 17.5 mW typical standby.

Refresh period is extended to 4 milliseconds, and during this period each of the 256 rows must be strobed with $\overline{RAS}$ in order to retain data. $\overline{CAS}$ can remain high during the refresh sequence to conserve power.

All inputs and outputs, including clocks, are compatible with Series 54/74 TTL. All address lines and data in are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility. Pin 1 has no internal connection to allow compatibility with other 64K RAMs that use this pin for an additional function.

The SMJ4164 is offered in a 16-pin dual-in-line ceramic sidebraze package (JD suffix) and in a leadless ceramic chip carrier package (FG suffix). The JD package is designed for insertion in mounting-hole rows on 7,62-mm (300-mil) centers whereas the FG package is intended for surface mounting on solder lands on 1,27-mm (0.050-inch) centers. The FG package is a three-layer, 18-pad, rectangular ceramic chip carrier with dimensions of 7,37 × 10,8 × 1,65 mm (0.290 × 0.425 × 0.065 inches).

operation

address (A0 through A7)

Sixteen address bits are required to decode 1 of 65,536 storage cell locations. Eight row-address bits are set up on pins A0 through A7 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the eight column-address bits are set up on pins A0 through A7 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$, data-out will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data in (D)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. This latch can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data out (Q)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan out of two Series 54/74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output goes active after the access time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ is satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low; $\overline{CAS}$ going high returns it to a high-impedance state. In an early write cycle, the output is always in the high-impedance state. In a delayed-write or read-modify-write cycle, the output will follow the sequence for the read cycle.

refresh

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffer is in the high-impedance state unless $\overline{CAS}$ is applied, the $\overline{RAS}$-only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses (A0 through A7) with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power.

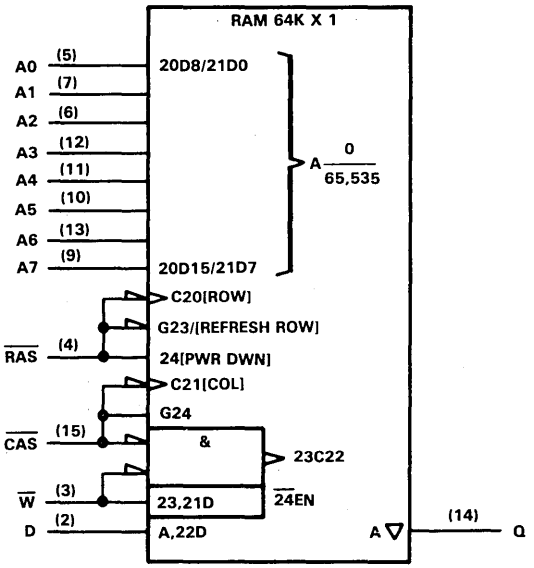
page mode

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the chip. Thus, the time required to setup and strobe sequential row addresses for the same page is eliminated. To extend beyond the 256 column locations on a single RAM, the row address and $\overline{RAS}$ are applied to multiple 64K RAMs. $\overline{CAS}$ is then decoded to select the proper RAM.

power up

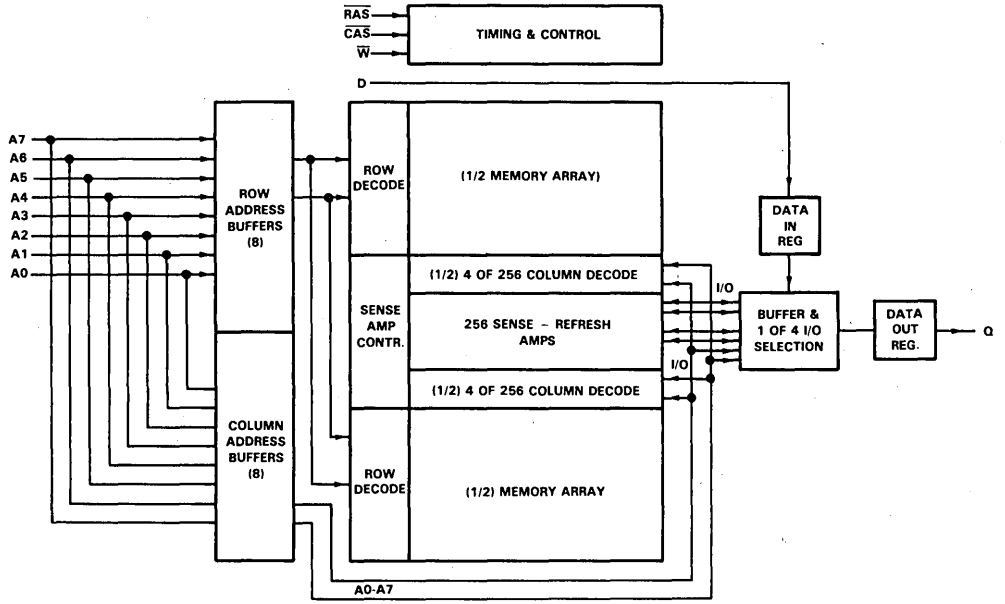
After power up, the power supply must remain at its steady-state value for 1 ms. In addition, $\overline{RAS}$ must remain high for 100 μs immediately prior to initialization. Initialization consists of performing eight $\overline{RAS}$ cycles before proper device operation is achieved.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the dual-in-line package.

functional block diagram



absolute maximum ratings over operating temperature range (unless otherwise noted)†

Voltage on any pin except V_{DD} and data out (see Note 1)	−1.5 V to 10 V
Voltage on V_{DD} supply and data out with respect to V_{SS}	−1 V to 6 V
Short circuit output current	50 mA
Power dissipation	1 W
Minimum operating free-air temperature: S version	−55°C
E version	−40°C
L version	0°C
Operating case temperature: S version	110°C
E version	85°C
L version	70°C
Storage temperature range	−65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values in this data sheet are with respect to V_{SS}.
2. Additional information concerning the handling of ESD sensitive devices is available in a document entitled *"Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies"* in Section 12.

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recommended operating conditions

		S VERSION			E VERSION			L VERSION			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
V_{DD}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
V_{SS}	Supply voltage		0			0			0		V
V_{IH}	High-level input voltage	2.4		V_{CC}+0.3	2.4		V_{CC}+0.3	2.4		V_{CC}+0.3	V
V_{IL}	Low-level input voltage (Notes 3 and 4)	−0.6		0.8	−0.6		0.8	−0.6		0.8	V
T_A	Operating free-air temperature	−55			−40			0			°C
T_C	Operating case temperature			110			85			70	°C

NOTES: 3. The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.
4. Due to input protection circuitry, the applied voltage may begin to clamp at −0.6 V. Test conditions should comprehend this occurrence. See Application Report entitled "TMS4164A and TMS4416 Input Diode Protection" on page 9-5.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SMJ4164-12			SMJ4164-15			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4			2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 5.8 V, V_{DD} = 5.5 V, All other pins = 0 V			±10			±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10			±10	μA
I_{DD1}‡	Average operating current during read or write cycle	t_c = minimum cycle, All outputs open		40	48		35	45	mA
I_{DD2}§	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, All outputs open		3.5	5		3.5	5	mA
I_{DD3}‡	Average refresh current	t_c = minimum cycle, $\overline{CAS}$ high and $\overline{RAS}$ cycling, All outputs open		28	40		25	37	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low and $\overline{CAS}$ cycling, All outputs open		28	40		25	37	mA

†All typical values are at T_C = 25°C and nominal supply voltages.
‡Additional information on page 8-46.
§V_{IL} > −0.6 V. See Application Report entitled "TMS4164A and TMS4416 Input Diode Protection" on page 9-5.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SMJ4164-20			UNIT
			MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 5.8 V, V_{DD} = 5.5 V, All other pins = 0 V			±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10	μA
I_{DD1}‡	Average operating current during read or write cycle	t_c = minimum cycle, All outputs open		27	37	mA
I_{DD2}§	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, All outputs open		3.5	5	mA
I_{DD3}‡	Average refresh current	t_c = minimum cycle, $\overline{CAS}$ high and $\overline{RAS}$ cycling, All outputs open		20	32	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low and $\overline{CAS}$ cycling, All outputs open		20	32	mA

†All typical values are at T_C = 25°C and nominal supply voltages.
‡Additional information on page 8-46.
§V_{IL} > −0.6 V. See Application Report entitled "TMS4164A and TMS4416 Input Diode Protection" on page 9-5.

capacitance over recommended supply voltage range and recommended temperature range, f = 1 MHz†

PARAMETER		SMJ4164		UNIT
		TYP‡	MAX	
$C_{i(A)}$	Input capacitance, address inputs	4	7	pF
$C_{i(D)}$	Input capacitance, data input	4	7	pF
$C_{i(RC)}$	Input capacitance strobe inputs	8	10	pF
$C_{i(W)}$	Input capacitance, write enable input	8	10	pF
C_o	Output capacitance	5	8	pF

†These parameters are guaranteed but not tested.
‡All typical values are at T_C = 25°C and nominal supply voltages.

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switching characteristics over recommended supply voltage range and recommended operating temperature range

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	SMJ4164-12		SMJ4164-15		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 80 pF, see Figure 1	t_{CAC}		70		85	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	C_L = 80 pF, t_{RLCL} = MAX, see Figure 1	t_{RAC}		120		150	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$	C_L = 80 pF, see Figure 1	t_{OFF}	0	40	0	40	ns

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	SMJ4164-20		UNIT
				MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 80 pF, see Figure 1	t_{CAC}		135	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	C_L = 80 pF, t_{RLCL} = MAX, see Figure 1	t_{RAC}		200	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 80 pF, see Figure 1	t_{OFF}	0	50	ns

timing requirements over recommended supply voltage range and recommended operating temperature range

		ALT. SYMBOL	SMJ4164-12		SMJ4164-15		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(P)}$	Page-mode cycle time	t_{PC}	130		160		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	230		260		ns
$t_{c(W)}$	Write cycle time	t_{WC}	230		260		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	260		285		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (precharge time)‡	t_{CP}	50		50		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low§	t_{CAS}	70	10,000	85	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge time)	t_{RP}	80		100		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low¶	t_{RAS}	120	10,000	150	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	40		45		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	50	3	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	−5		−5		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	50		50		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	50		50		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	40		45		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	15		20		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	85		95		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DHC}	40		45		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	85		95		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DHW}	40		45		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high‖	t_{RCH}	0		0		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high‖	t_{RRH}	5		5		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	40		45		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	85		95		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	120		150		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	70		85		ns

Continued next page.

NOTE 5: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, V_{IL} max and V_{IH} min must be met at the 10% and 90% points.

†All cycle times assume t_t = 5 ns.

‡Page-mode only.

§In a read-modify-cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$). This applies to page-mode read-modify-write also.

¶In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).

‖These parameters are guaranteed but not tested.

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timing requirements over recommended supply voltage range and recommended operating temperature range (continued)

		ALT. SYMBOL	SMJ4164-12		SMJ4164-15		UNIT
			MIN	MAX	MIN	MAX	
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{CWD}	40		60		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	15	45	20	50	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{RWD}	85		100		ns
t_{WLCL}	Delay time, $\overline{W}$ low to $\overline{CAS}$ low (early write cycle)	t_{WCS}	−5		−5		ns
t_{rf}	Refresh time interval	t_{REF}		4		4	ms

timing requirements over recommended supply voltage range and recommended operating temperature range (continued)

		ALT. SYMBOL	SMJ4164-20		UNIT
			MIN	MAX	
$t_{c(P)}$	Page-mode cycle time	t_{PC}	225		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	330		ns
$t_{c(W)}$	Write cycle time	t_{WC}	330		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	345		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (precharge time)‡	t_{CP}	80		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low§	t_{CAS}	135	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge time)	t_{RP}	120		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low¶	t_{RAS}	200	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	55		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	−5		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	80		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	80		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	55		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	25		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	140		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DHC}	80		ns

Continued next page.

NOTE 5: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, V_{IL} max and V_{IH} min must be met at the 10% and 90% points.

†All cycle times assume t_t = 5 ns.

‡Page-mode only.

§In a read-modify-cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$). This applies to page-mode read-modify-write also.

¶In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).

timing requirements over recommended supply voltage range and recommended operating temperature range (concluded)

		ALT SYMBOL	SMJ4164-20		UNIT
			MIN	MAX	
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	145		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DHW}	55		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high‖	t_{RCH}	0		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high‖	t_{RRH}	5		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	80		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	145		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	200		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	135		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{CWD}	65		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	25	65	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{RWD}	130		ns
t_{WLCL}	Delay time, $\overline{W}$ low to $\overline{CAS}$ low (early write cycle)	t_{WCS}	−5		ns
t_{rf}	Refresh time interval	t_{REF}		4	ms

‖These parameters are guaranteed but not tested.

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PARAMETER MEASUREMENT INFORMATION

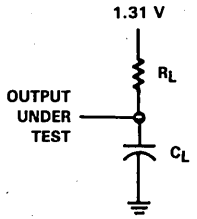
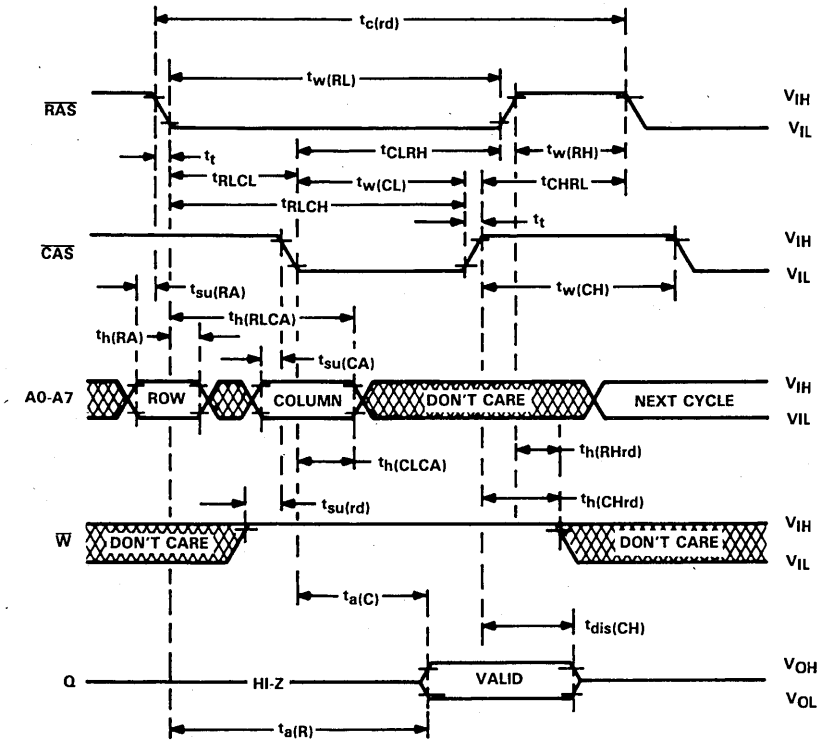
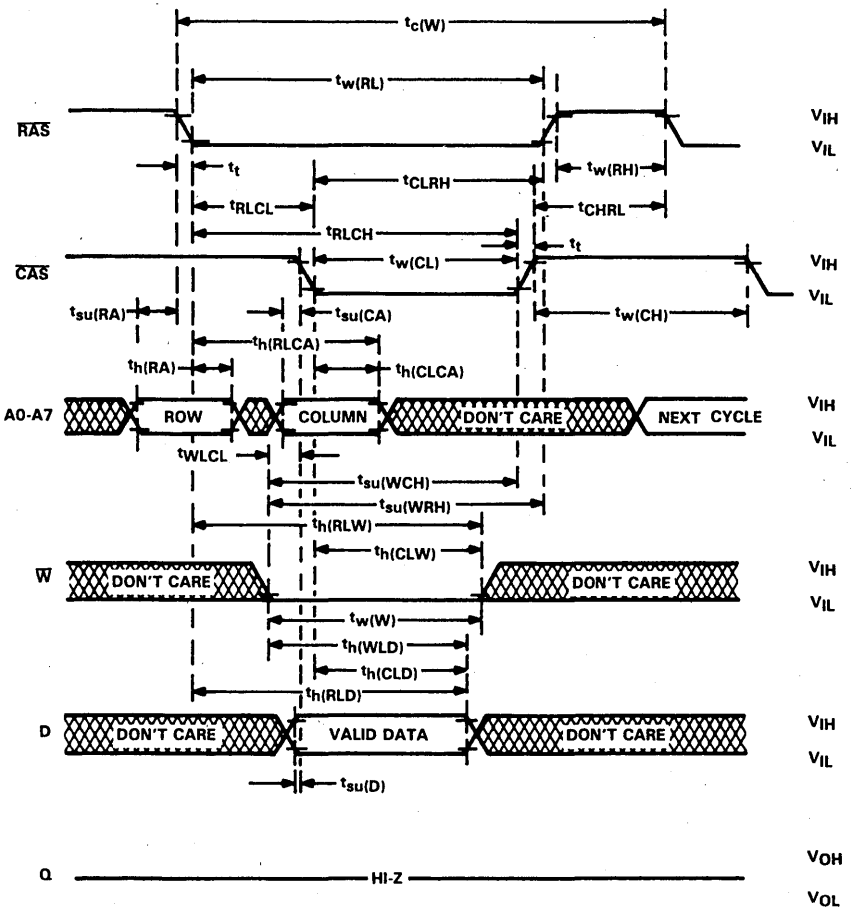


FIGURE 1. LOAD CIRCUIT

read cycle timing



early write cycle timing



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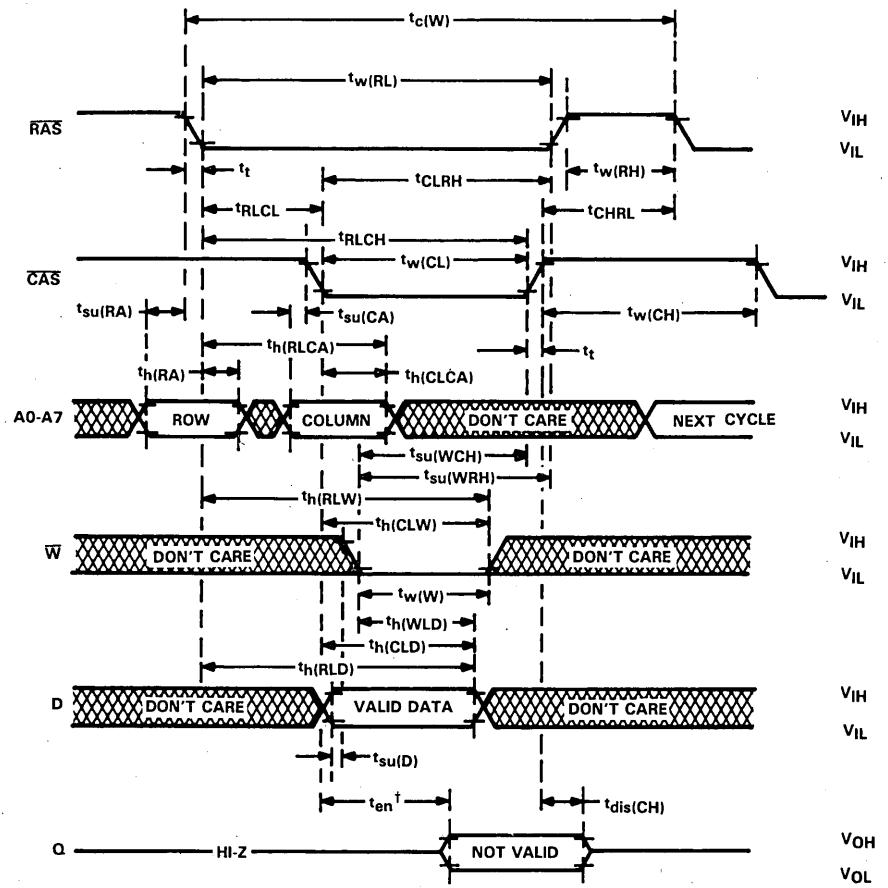
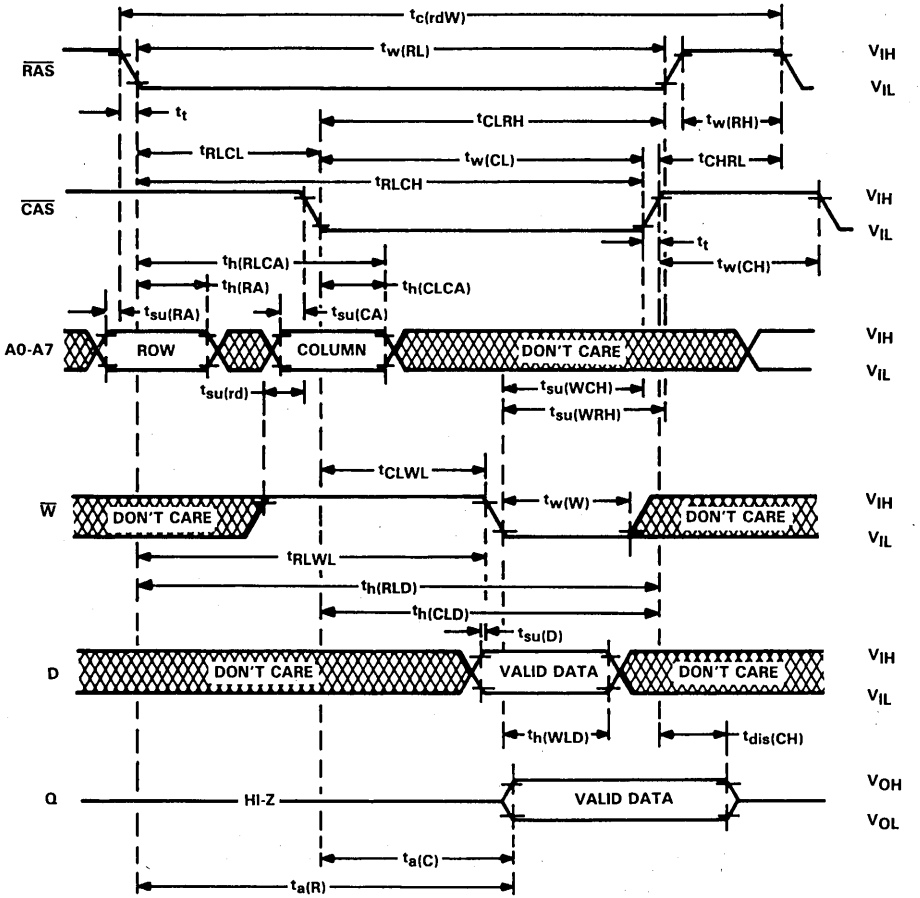
write cycle timing



† The enable time (t_{en}) for a write cycle is equal in duration to the access time from $\overline{CAS}$ ($t_{a(C)}$) in a read cycle; but the active levels at the output are invalid.

read-write/read-modify-write cycle timing



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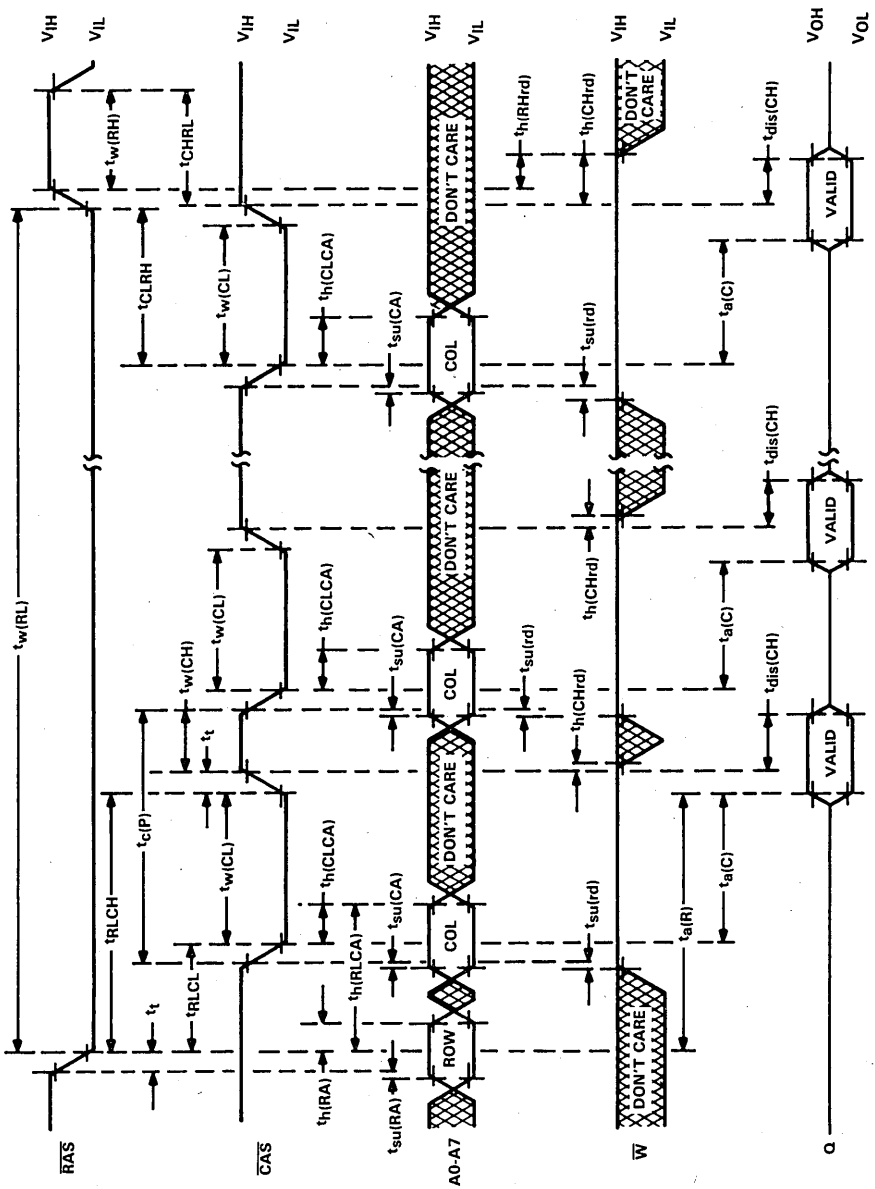
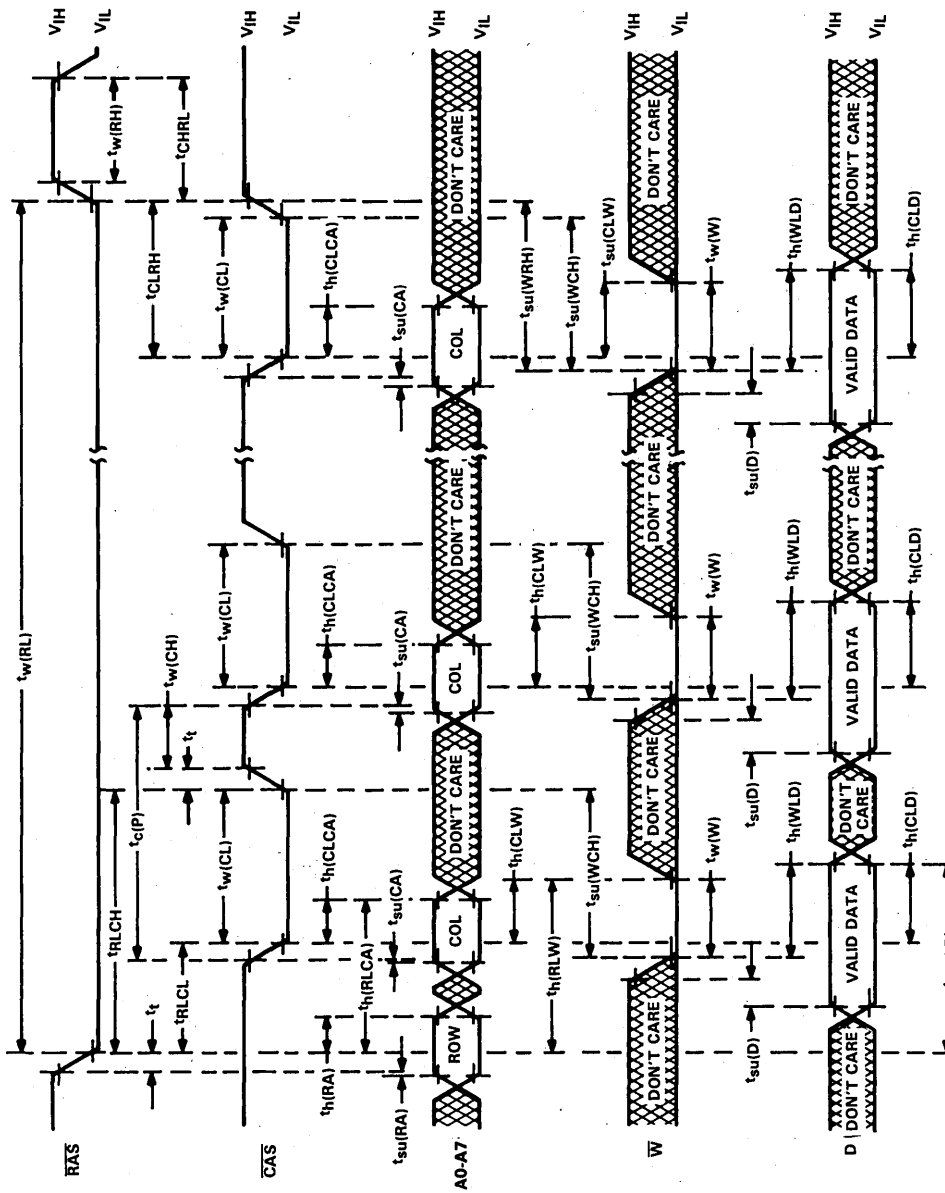
page-mode read cycle timing



NOTE 6: A write cycle or a read-modify-write cycle can be intermixed with read cycles as long as the write and read-modify-write timing specifications are not violated.

page-mode write cycle timing



NOTE 7: A read cycle or a read-modify-write cycle can be intermixed with write cycles as long as the read and read-modify-write timing specifications are not violated.

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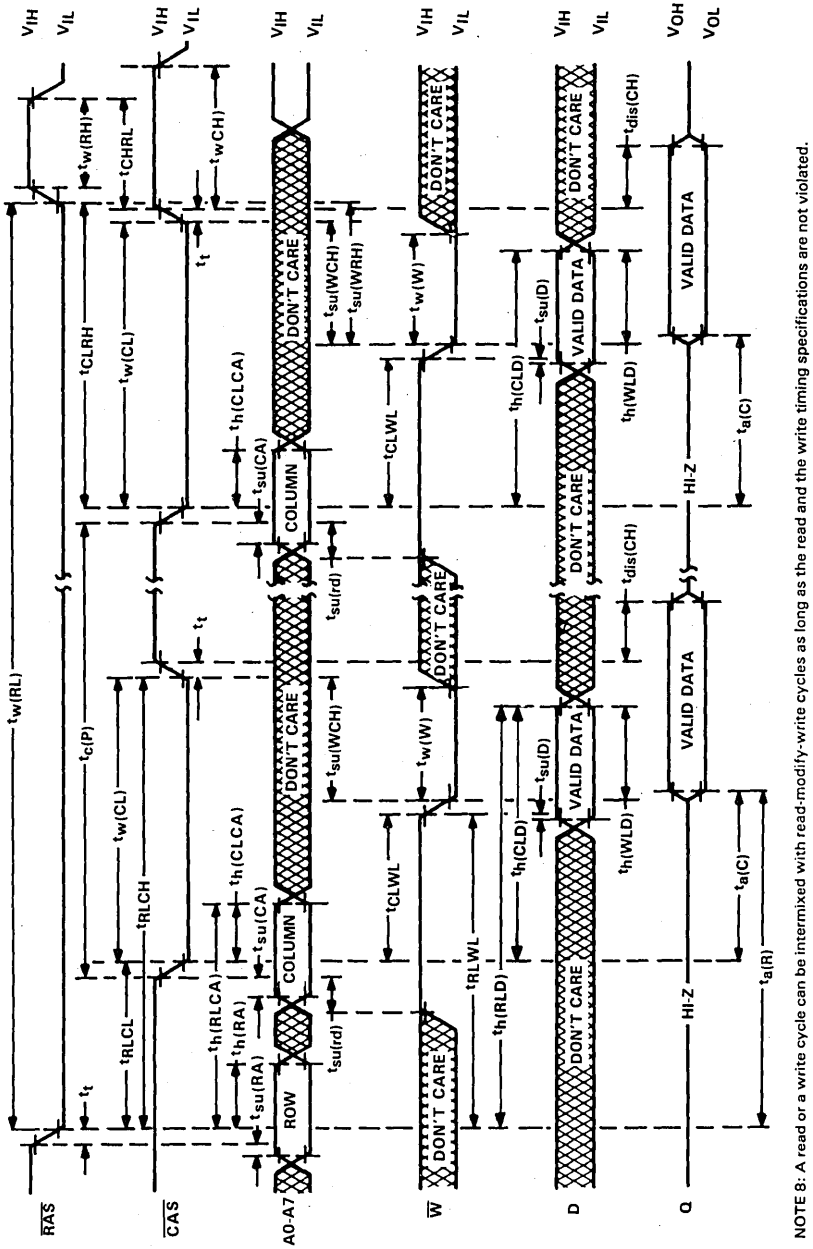
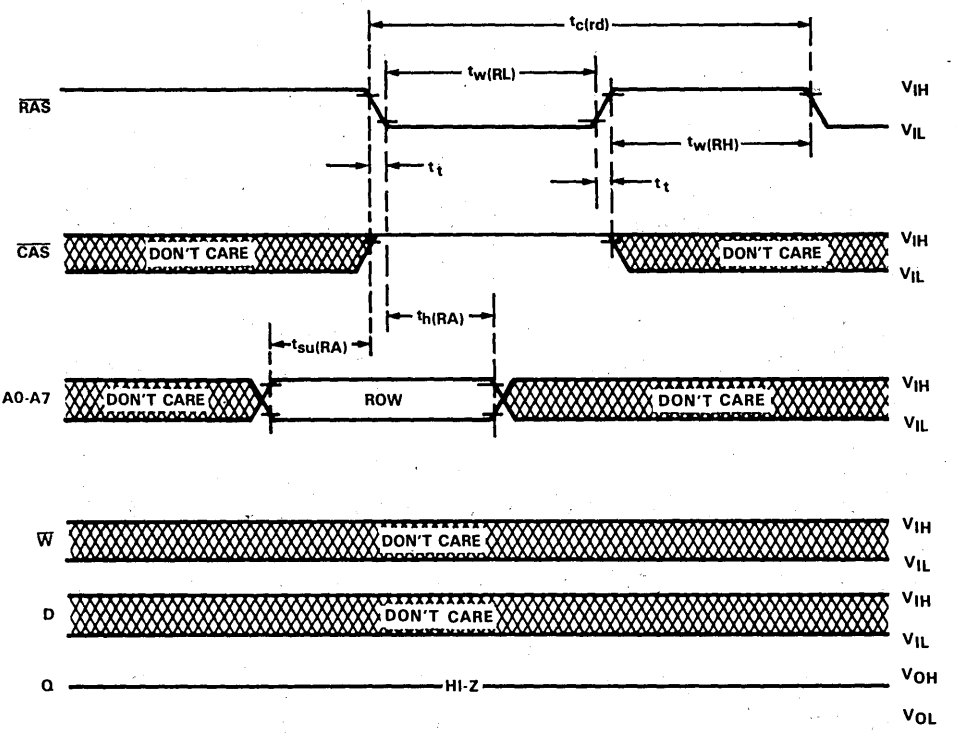
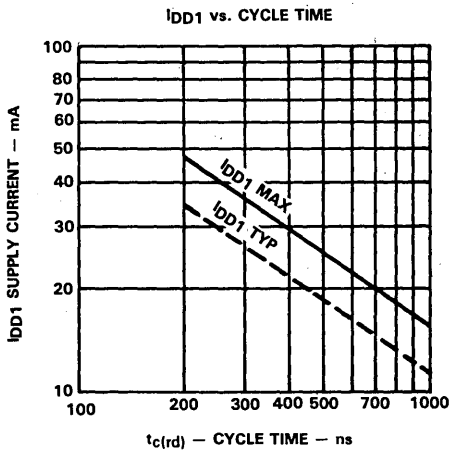
page-mode read-modify-write cycle timing

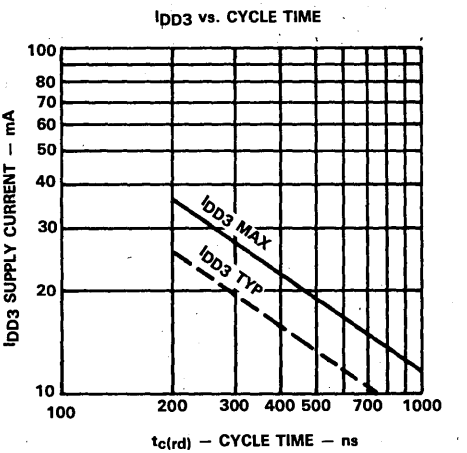


NOTE 8: A read or a write cycle can be intermixed with read-modify-write cycles as long as the read and the write timing specifications are not violated.

$\overline{RAS}$-only refresh timing







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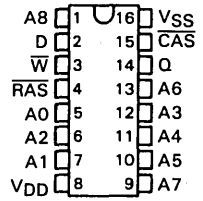
NOVEMBER 1985

- 262,144 X 1 Organization
- Single 5-V Supply
- JEDEC Standardized Pinout
- Upward Pin Compatible with SMJ4164 (64K Dynamic RAM)
- Performance Ranges:

	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)
SMJ4256-15	150 ns	80 ns	260 ns
SMJ4256-20	200 ns	100 ns	330 ns

- Long Refresh Period . . . 4 ms (Max)
- Low Refresh Overhead Time . . . As Low As 1.3% of Total Refresh Period
- On-Chip Substrate Bias Generator
- All Inputs, Outputs, and Clocks Fully TTL Compatible
- 3-State Unlatched Output
- Common I/O Capability with "Early Write" Feature
- Power Dissipation as Low As
  —Operating . . . 300 mW (Typ)
  —Standby . . . 12.5 mW (Typ)
- MIL-STD-883C Class B High-Reliability Processing

JD PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A8	Address Inputs
$\overline{CAS}$	Column-Address Strobe
D	Data In
Q	Data Out
$\overline{RAS}$	Row-Address Strobe
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

- $\overline{RAS}$-Only Refresh Mode
- Hidden Refresh Mode
- $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Mode
- Full Military DRAM Temperature Range Operation . . . −55°C to 110°C

description

The SMJ4256 is a high-speed, 262,144-bit dynamic random-access memory, organized as 262,144 words of one bit each. It employs state-of-the-art SMOS (scaled MOS) N-channel double-level polysilicon/polycide gate technology for very high performance combined with low cost and improved reliability.

The SMJ4256 features maximum $\overline{RAS}$ access times of 150 ns or 200 ns. Typical power dissipation is as low as 300 mW operating and 12.5 mW standby.

New SMOS technology permits operation from a single 5-V supply, reducing system power supply and decoupling requirements, and easing board layout. I_{DD} peaks are 125 mA typical, and a −0.5-V input voltage undershoot can be tolerated, minimizing system noise considerations.

All inputs and outputs, including clocks, are compatible with Series 54 TTL. All address and data-in lines are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The SMJ4256 is offered in a 16-pin ceramic dual-in-line package. It is guaranteed for operation from −55°C to 110°C. The dual-in-line package is designed for insertion in mounting-hole rows on 7,62-mm (300-mil) centers.

operation

address (A0 through A8)

Eighteen address bits are required to decode 1 of 262,144 storage cell locations. Nine row-address bits are set up on pins A0 through A8 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the nine column-address bits are set up on pins A0 through A8 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$, data out will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data in (D)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. This latch can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data out (Q)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan out of two Series 54 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output goes active after the access time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ is satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low; $\overline{CAS}$ going high returns it to a high-impedance state. In a read-modify-write cycle, the output will follow the sequence for the read cycle.

refresh

A refresh operation must be performed at least once every four milliseconds to retain data. This can be achieved by strobing each of the 256 rows (A0-A7). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, thus conserving power as the output buffer remains in the high-impedance state.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

The $\overline{CAS}$-before-$\overline{RAS}$ refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CLRL}) and holding it low after $\overline{RAS}$ falls (see parameter t_{RLCHR}). For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally.

hidden refresh

Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a "$\overline{RAS}$-only" refresh cycle. The external address is also ignored during the hidden refresh cycles.

page mode

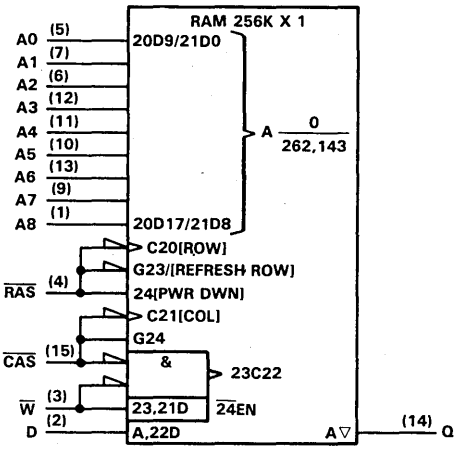
Page-mode operation allows effectively faster memory access by keeping the same row address and strobing random column addresses onto the chip. Thus, the time required to setup and strobe sequential row

addresses for the same page is eliminated. The maximum number of columns that can be addressed is determined by $t_{w(RL)}$, the maximum $\overline{RAS}$ low pulse duration.

power-up

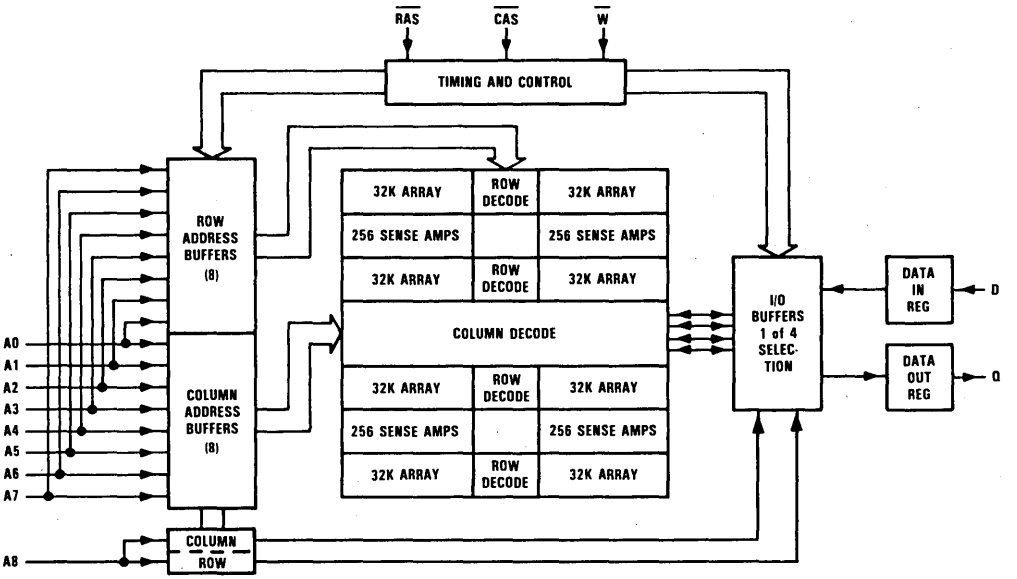
To achieve proper device operation, an initial pause of 200 μs is required after power up followed by a minimum of eight initialization cycles.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram



absolute maximum ratings over operating temperature range (unless otherwise noted)†

Voltage range for any pin including V_{DD} supply (see Note 1) . . . . . −1 V to 7 V
Short circuit output current . . . . . 50 mA
Power dissipation . . . . . 1 W
Minimum operating free-air temperature . . . . . −55°C
Operating case temperature . . . . . 100°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	4.75	5	5.25	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		5	V
V_{IL}	Low-level input voltage (see Note 2)	−0.5		0.6	V
T_A	Operating free-air temperature	−55			°C
T_C	Operating case temperature			110	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as maximum, is used in this data sheet for logic voltage levels only.

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electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SMJ4256-15			SMJ4256-20			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4			2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 5 V, V_{DD} = 5 V, All other pins = 0 V to 5 V			±10			±10	μA
I_O	Output current (leakage)	V_O = 0 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10			±10	μA
I_{DD1}	Average operating current during read or write cycle	t_c = minimum cycle, Output open		60	75		45	60	mA
I_{DD2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, Output open		2.5	5		2.5	5	mA
I_{DD3}	Average refresh current	t_c = minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high, Output open		45	60		35	45	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling, Output open		35	50		25	45	mA

†All typical values are at T_A = 25°C and nominal supply voltages.

capacitance over recommended supply voltage range and operating temperature range, f = 1 MHz

PARAMETER		TYP†	UNIT
$C_{i(A)}$	Input capacitance, address inputs	4	pF
$C_{i(D)}$	Input capacitance, data input	4	pF
$C_{i(RC)}$	Input capacitance strobe inputs	4	pF
$C_{i(W)}$	Input capacitance, write enable input	4	pF
C_o	Output capacitance	5	pF

†All typical values are at T_A = 25°C and nominal supply voltages.

switching characteristics over recommended supply voltage range and operating temperature range

PARAMETER		TEST CONDITIONS†	ALT. SYMBOL	SMJ4256-15		SMJ4256-20		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	$t_{RLCL} \geq$ MAX, C_L = 80 pF, I_{OH} = −5 mA, I_{OL} = 4.2 mA	t_{CAC}		80		100	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, C_L = 80 pF, I_{OH} = −5 mA, I_{OL} = 4.2 mA	t_{RAC}		150		200	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 80 pF, I_{OH} = −5 mA, I_{OL} = 4.2 mA	t_{OFF}	0	30	0	35	ns

†Figure 1 shows the load circuit; C_L values shown are typical for test system used.

timing requirements over recommended supply voltage range and operating temperature range

		ALT. SYMBOL	SMJ4256-15		SMJ4256-20		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(P)}$	Page-mode cycle time (read or write cycle)	t_{PC}	145		190		ns
$t_{c(PM)}$	Page-mode cycle time (read-modify-write cycle)	t_{PCM}	205		250		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	260		330		ns
$t_{c(W)}$	Write cycle time	t_{WC}	260		330		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	315		390		ns
$t_{w(CH)P}$	Pulse duration, $\overline{CAS}$ high (page mode)	t_{CP}	60		80		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (non-page mode)	t_{CPN}	60		80		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low‡	t_{CAS}	80	10,000	100	10,000	ns
$t_{w(RH)P}$	Pulse duration, $\overline{RAS}$ high (page mode)	t_{RP}	120		120		ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (non-page mode)	t_{RPN}	100		120		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low§	t_{RAS}	150	10,000	200	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	45		55		ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	5		5		ns
$t_{su(D)}$	Data setup time	t_{DS}	3		3		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	5		5		ns
$t_{su(WCL)}$	Early write-command setup time before $\overline{CAS}$ low	t_{WCS}	0		0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	45		65		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	45		65		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	30		45		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	20		25		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	100		145		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	50		55		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	120		155		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	45		55		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	10		15		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	50		55		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	120		155		ns

Continued next page.

NOTES: 3. Timing measurements are referenced to V_{IL} max and V_{IH} min.

4. System transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$ are to be a minimum of 3 ns and a maximum of 50 ns.

†All cycle times assume t_t = 5 ns.

‡In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time $t_{w(CL)}$. This applies to page-mode read-modify-write also.

§In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).

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timing requirements over recommended supply voltage range and operating temperature range (concluded)

		ALT. SYMBOL	SMJ4256-15		SMJ4256-20		UNIT
			MIN	MAX	MIN	MAX	
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	150		200		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	5		5		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	80		100		ns
t_{RLCHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high¶	t_{CHR}	30		40		ns
t_{CLRL}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low¶	t_{CSR}	30		35		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{CWD}	85		90		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	25	70	35	100	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{RWD}	155		190		ns
t_{rf}	Refresh time interval	t_{REF}		4		4	ms

NOTE 3: Timing measurements are referenced to V_{IL} max and V_{IH} min.
¶$\overline{CAS}$-before-$\overline{RAS}$ refresh only.

PARAMETER MEASUREMENT INFORMATION

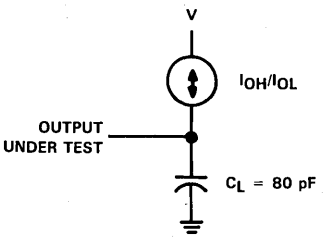
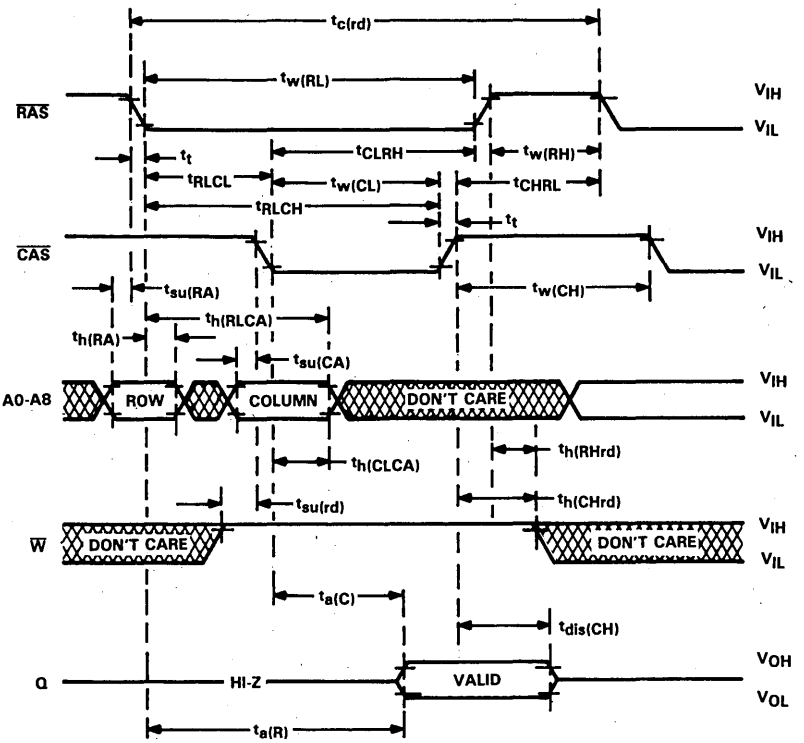


FIGURE 1. EQUIVALENT LOAD CIRCUIT

read cycle timing



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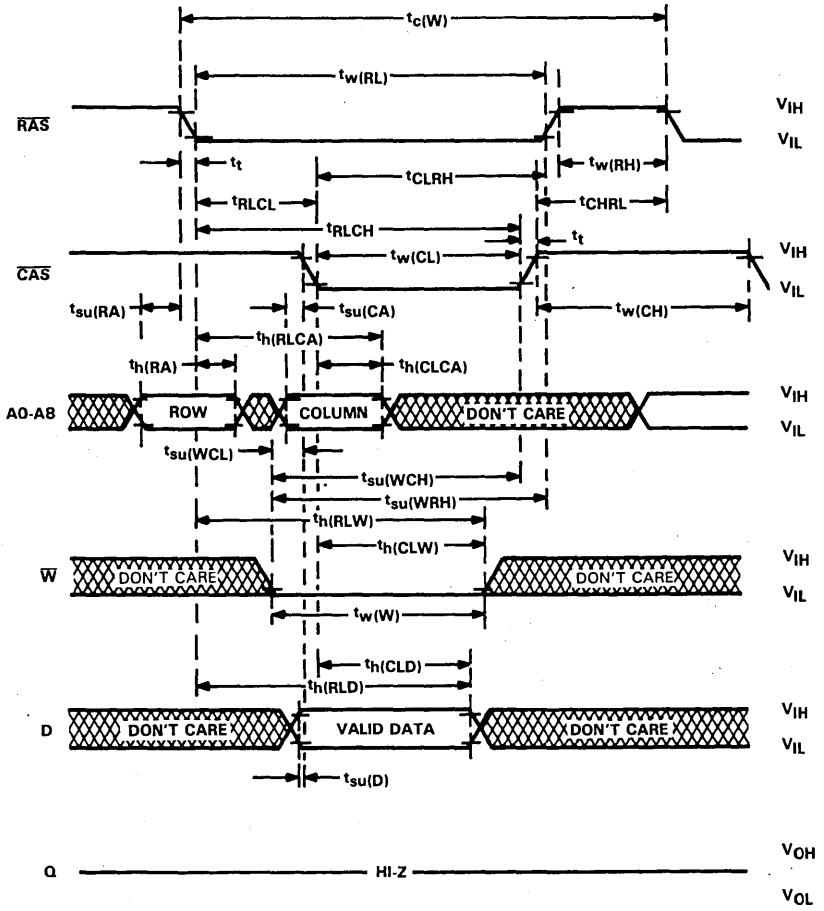
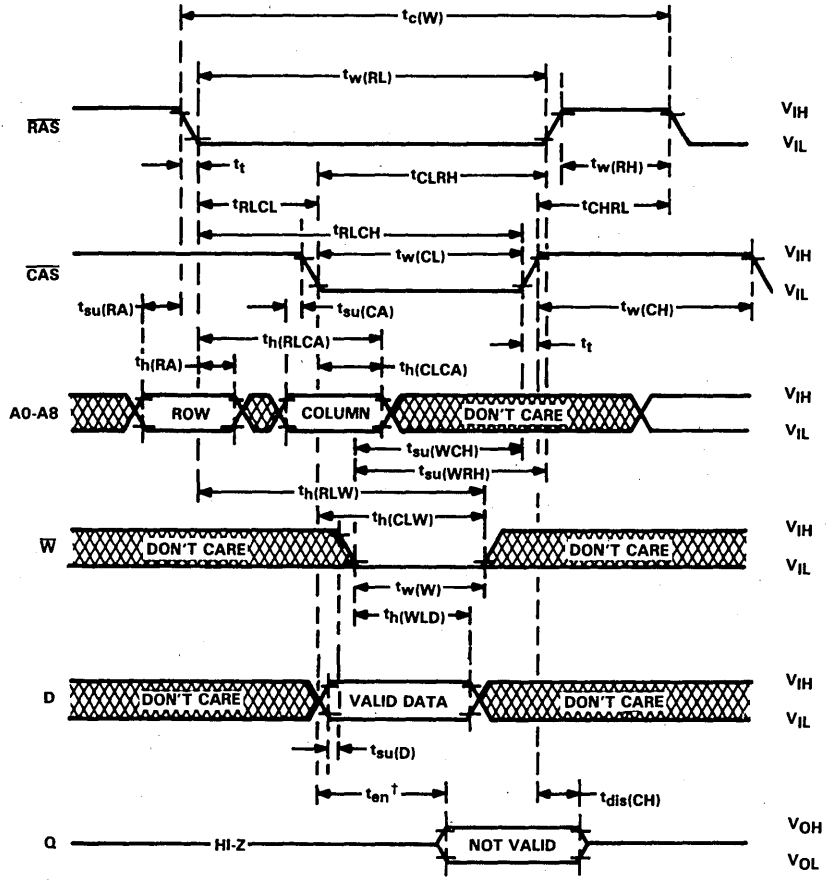
early write cycle timing

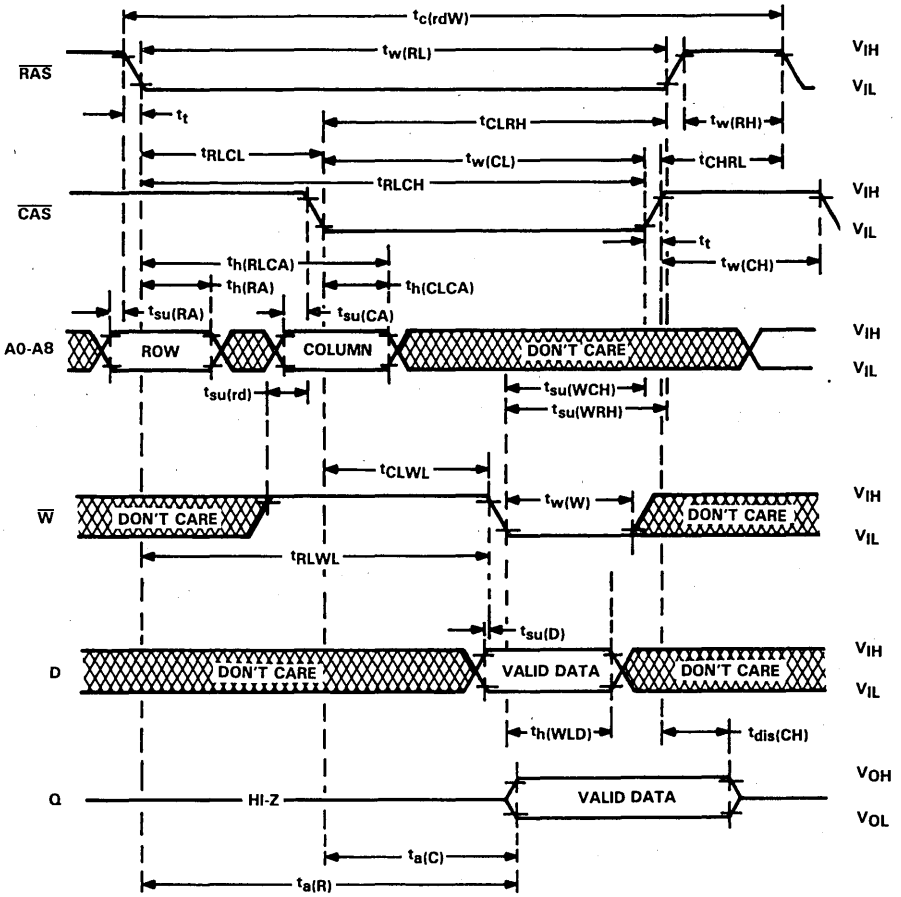


write cycle timing



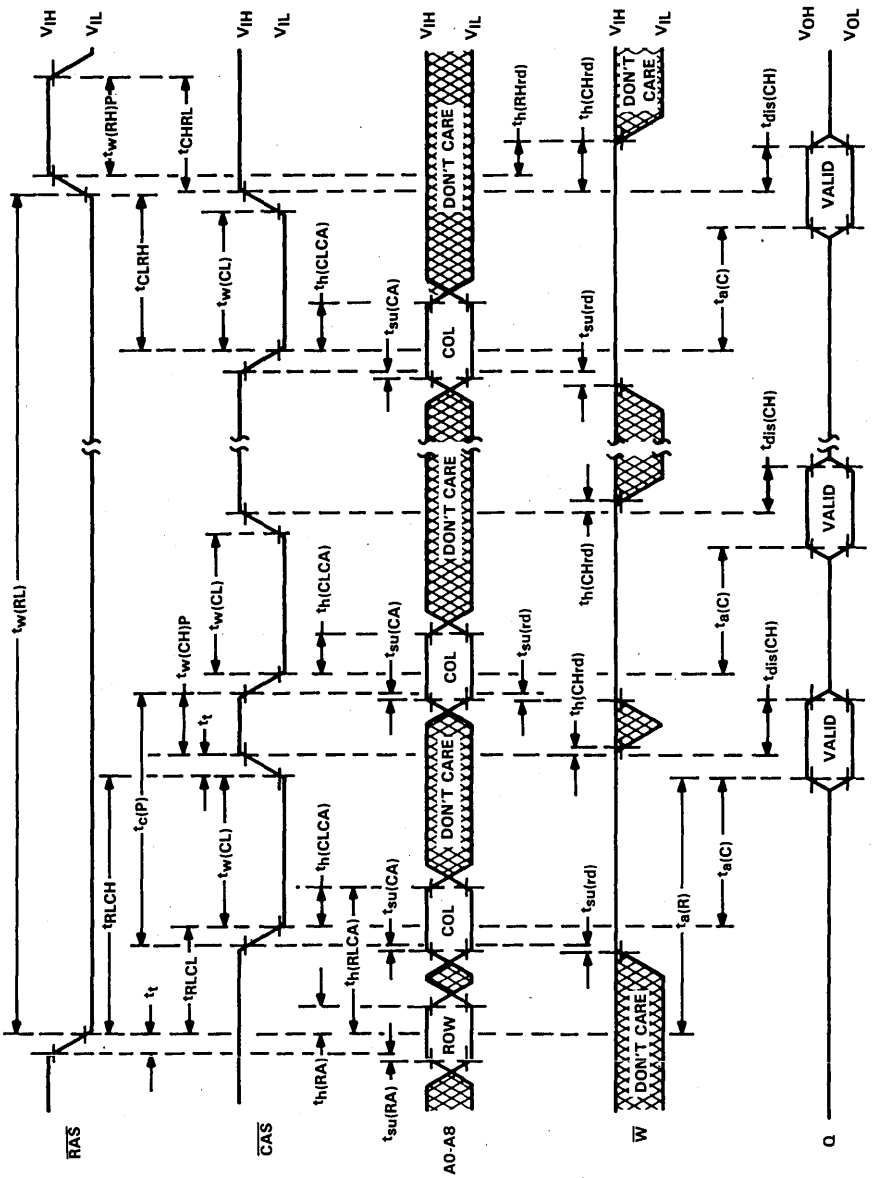
†The enable time (t_{en}) for a write cycle is equal in duration to the access time from $\overline{CAS}$ ($t_{a(C)}$) in a read cycle; but the active levels at the output are invalid.

read-write/read-modify-write cycle timing



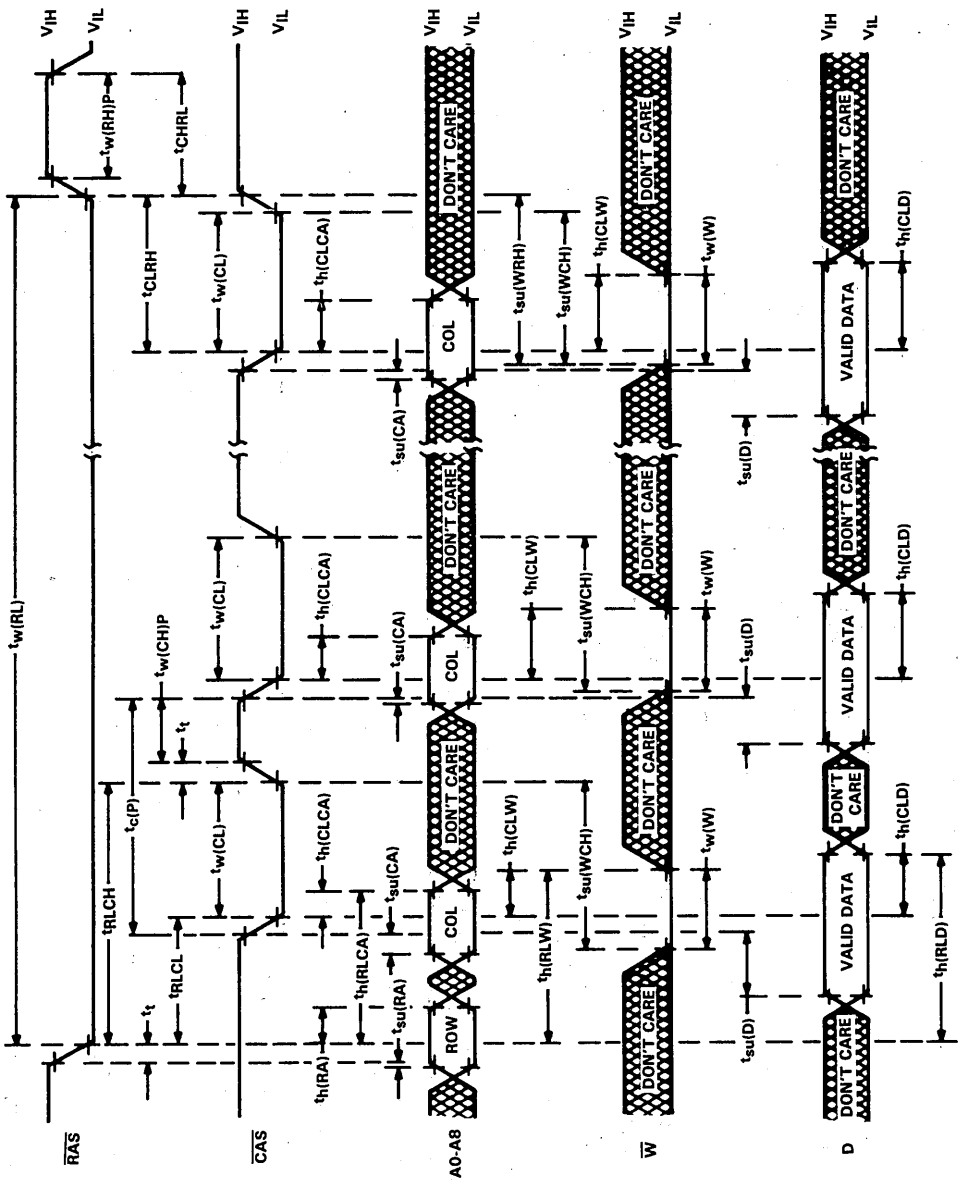
†The enable time (t_{en}) for a write cycle is equal in duration to the access time from $\overline{CAS}$ $t_{a(C)}$ in a read cycle; but the active levels at the output are invalid.

page-mode read cycle timing



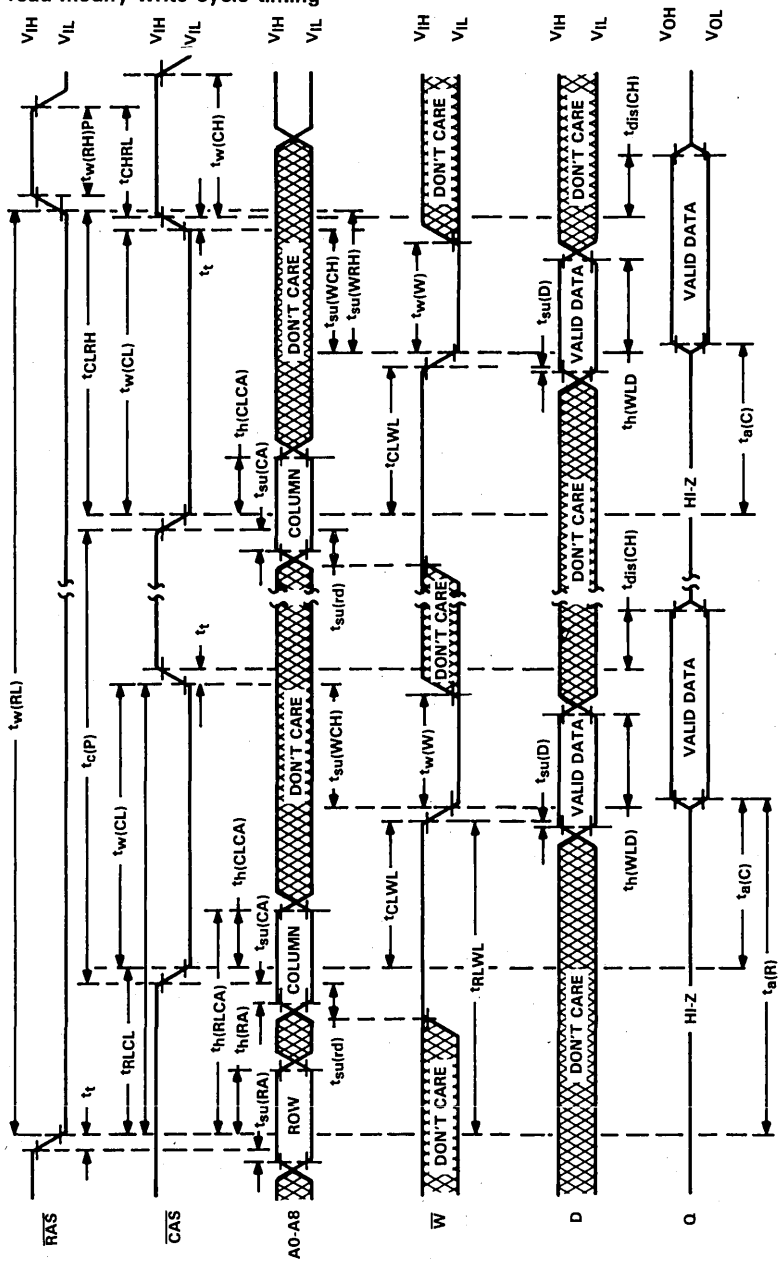
NOTE 5: A write cycle or a read-modify-write cycle can be intermixed with read cycles as long as the write and read-modify-write timing specifications are not violated.

page-mode write cycle timing



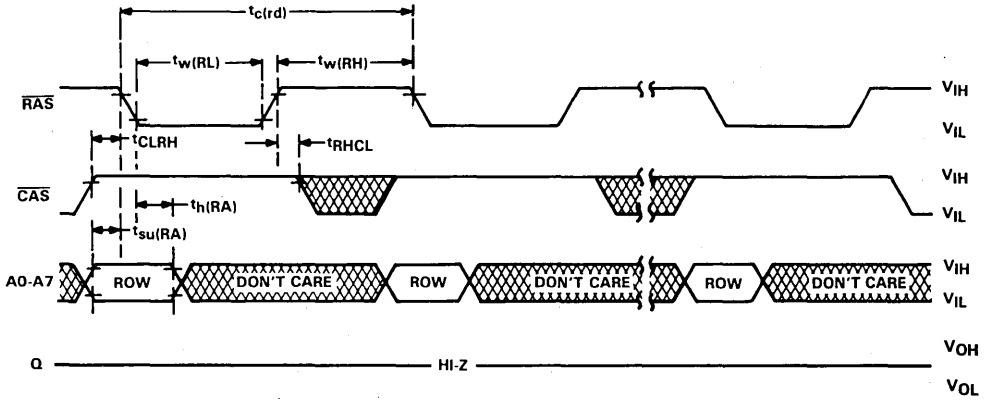
NOTE 6: A read cycle or a read-modify-write cycle can be intermixed with write cycles as long as read and read-modify-write timing specifications are not violated.

page-mode read-modify-write cycle timing

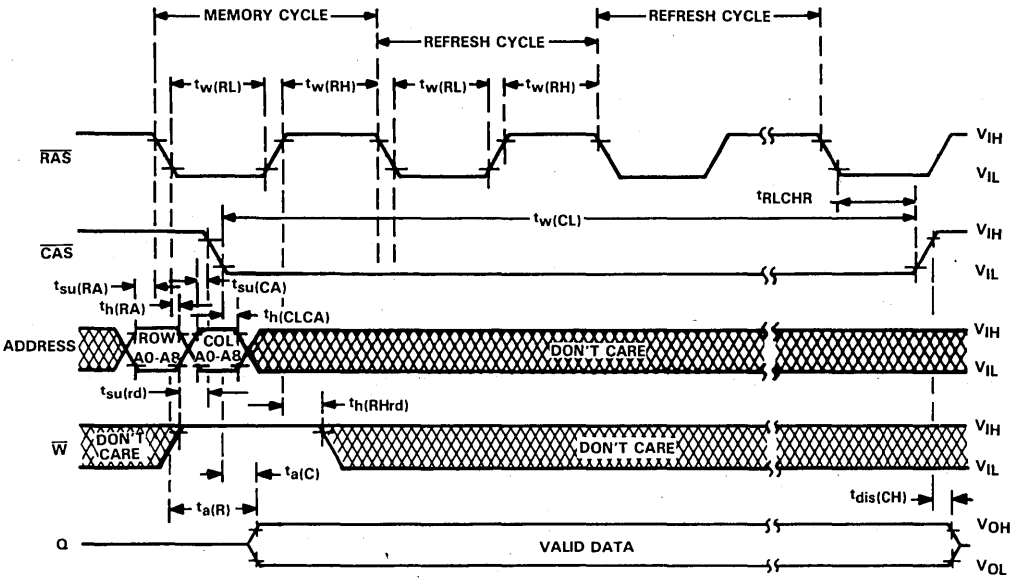


NOTE 7: A read or a write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

RAS-only refresh cycle timing



hidden refresh cycle timing†



†This timing is guaranteed but not tested.

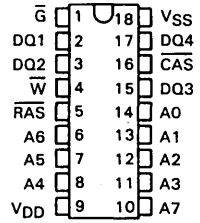
AUGUST 1980 – REVISED NOVEMBER 1985

- 16,384 X 4 Organization
- Single 5-V Supply (±10% Tolerance)
- Performance Ranges:

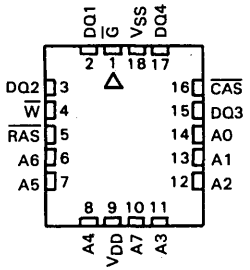
	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	READ-MODIFY-WRITE CYCLE (MIN)
'4416-12	120 ns	70 ns	230 ns	320 ns
'4416-15	150 ns	80 ns	260 ns	330 ns
'4416-20	200 ns	120 ns	330 ns	440 ns

- Available Temperature Ranges with MIL-STD-883C Class B High-Reliability Processing
  - –S . . . –55°C to 100°C
  - –E . . . –40°C to 85°C
  - –L . . . 0°C to 70°C
- Long Refresh Period . . . 4 ms
- Low Refresh Overhead Time . . . As Low As 1.7% of Total Refresh Period
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Unlatched Outputs
- Early Write or $\overline{G}$ to Control Output Buffer Impedance
- Page-Mode Operation for Faster Access
- Low Power Dissipation
  - –Operation . . . 200 mW (Typ)
  - –Standby . . . 17.5 mW (Typ)
- New SMOS (Scaled-MOS) N-Channel Technology

JD PACKAGE
(TOP VIEW)



FG PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A7	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1-DQ4	Data In/Data Out
$\overline{G}$	Output Enable
$\overline{RAS}$	Row-Address Strobe
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The SMJ4416 is a Military high-speed, 65,536-bit, dynamic, random-access memory, organized as 16,384 words of 4 bits each. It employs state-of-the-art SMOS (scaled MOS) N-channel double-level polysilicon gate technology for very high performance combined with low cost and improved reliability.

The SMJ4416 features $\overline{RAS}$ access times to 120 ns maximum. Power dissipation is 200 mW typical operating, 17.5 mW typical standby.

New SMOS technology permits operation from a single 5-V supply, reducing system power supply and decoupling requirements, and easing board layout. I_{DD} peaks have been reduced to 60 mA typical, and a –1-V input voltage undershoot can be tolerated, minimizing system noise considerations. Input clamp diodes are used to ease system design.

Refresh period is extended to 4 milliseconds, and during this period each of the 256 rows must be strobed with $\overline{RAS}$ in order to retain data. $\overline{CAS}$ can remain high during the refresh sequence to conserve power.

All inputs and outputs, including clocks, are compatible with Series 54/74 TTL. All address lines and data in are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The SMJ4416 is offered in 18-pin 300-mil ceramic side-braze dual-in-line and 18-pad ceramic chip-carrier packages. It is available in −55°C to 100°C, −40°C to 85°C, and 0°C to 70°C temperature ranges. Dual-in-line packages are designed for insertion in mounting-hole rows on 7,62 mm (300-mil) centers.

operation

address (A0 through A7)

Fourteen address bits are required to decode 1 of 16,384 storage locations. Eight row-address bits are set up on pins A0 through A7 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the six column-address bits are set up on pins A1 through A6 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$, data out will remain in the high-impedance state allowing a write cycle with $\overline{G}$ grounded.

data in (DQ1 through DQ4)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latches. These latches can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal. In delayed or read-modify-write, $\overline{G}$ must be high to bring the output buffers to high impedance prior to impressing data on the I/O lines.

data out (DQ1 through DQ4)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan out of two Series 54/74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output goes active after the access time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ and $t_{a(E)}$ are satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ and $\overline{G}$ are low. $\overline{CAS}$ or $\overline{G}$ going high returns it to a high-impedance state. In an early write cycle, the output is always in the high-impedance state. In a delayed-write or read-modify-write cycle, the output must be put in the high-impedance state prior to applying data to the DQ input. This is accomplished by bringing $\overline{G}$ high prior to applying data, thus satisfying t_{GHD}.

output enable ($\overline{G}$)

The $\overline{G}$ controls the impedance of the output buffers. When $\overline{G}$ is high, the buffers will remain in the high-impedance state. Bringing $\overline{G}$ low during a normal cycle will activate the output buffers putting them in the low-impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CAS}$ to be brought low for the output buffers to go into the low-impedance state. Once in the low-impedance state, they will remain in the low-impedance state until $\overline{G}$ or $\overline{CAS}$ is brought high.

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refresh

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffer is in the high-impedance state unless $\overline{CAS}$ is applied, the $\overline{RAS}$-only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses (A0 through A7) with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power.

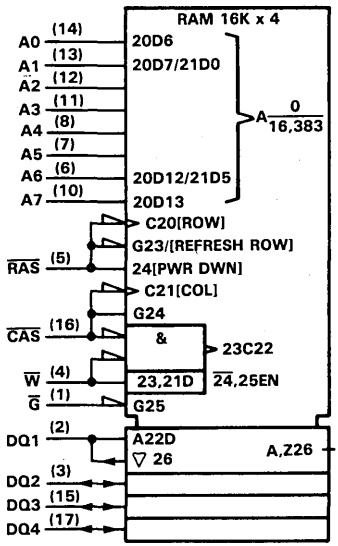
page mode

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the chip. Thus, the time required to setup and strobe sequential row addresses for the same page is eliminated. To extend beyond the 64 column locations on a single RAM, the row address and $\overline{RAS}$ are applied to multiple 16K × 4 RAMs. $\overline{CAS}$ is then decoded to select the proper RAM.

power up

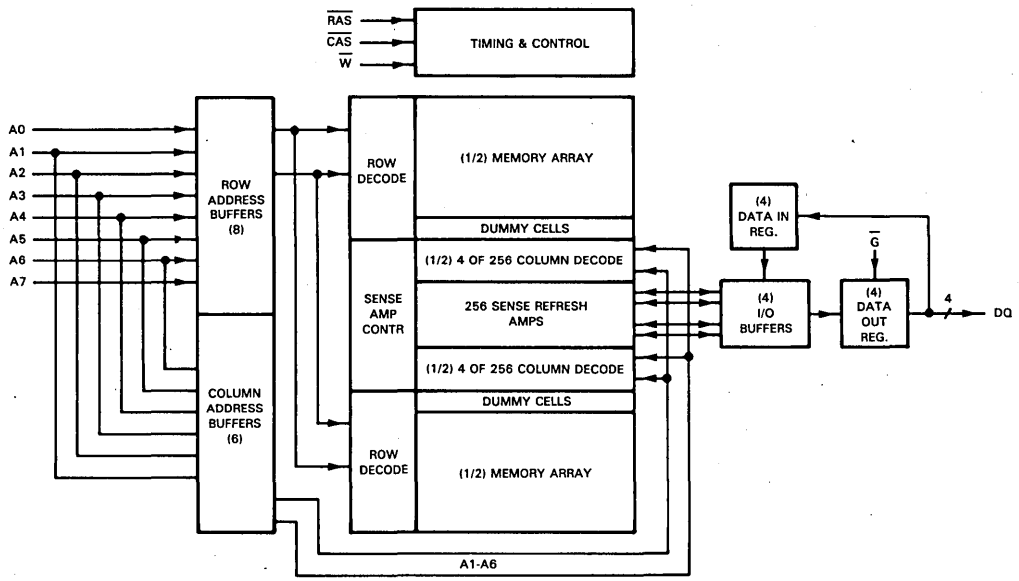
After power up, the power supply must remain at its steady-state value for 1 ms. In addition, the $\overline{RAS}$ input must remain high for 100 μs immediately prior to initialization. Initialization consists of performing eight $\overline{RAS}$ cycles before proper device operation is achieved.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the dual-in-line package.

functional block diagram



absolute maximum ratings over operating temperature range (unless otherwise noted)†

Voltage on any pin except V_{DD} and data out (see Note 1)	−1.5 V to 10 V
Voltage on V_{DD} supply and data out with respect to V_{SS}	−1 V to 6 V
Short circuit output current	50 mA
Power dissipation	1 W
Minimum operating free-air temperature: S version	−55°C
E version	−40°C
L version	0°C
Operating case temperature: S version	100°C
E version	85°C
L version	70°C
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values in this data sheet are with respect to V_{SS}.

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recommended operating conditions

			S VERSION			E VERSION			L VERSION			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
V_{DD}	Supply voltage		4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
V_{SS}	Supply voltage			0			0			0		V
V_{IH}	High-level input voltage	V_{DD} = 4.5 V	2.4		4.8	2.4		4.8	2.4		4.8	V
		V_{DD} = 5.5 V	2.4		5.8	2.4		5.8	2.4		5.8	
V_{IL}	Low-level input voltage		V_{IK}		0.8	V_{IK}		0.8	V_{IK}		0.8	V
T_A	Operating free-air temperature		−55			−40			0			°C
T_C	Operating case temperature				100			85			70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SMJ4416-12			UNIT
			MIN	TYP†	MAX	
V_{IK}	Input clamp voltage	I_I = −15 mA, see Figure 1			−1.2	V
V_{OH}	High-level output voltage	I_{OH} = −2 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 5.8 V, V_{DD} = 5 V, All other pins = 0 V			±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10	μA
I_{DD1}‡	Average operating current during read or write cycle	At t_c = minimum cycle			54	mA
I_{DD2}‡	Standby current (see Note 3)	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		3.5	5	mA
I_{DD3}‡	Average refresh current	t_c = minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high			46	mA
I_{DD4}‡	Average page-mode current	$t_{c(P)}$ = minimum cycle, RAS low, $\overline{CAS}$ cycling			46	mA

†All typical values are at T_C = 25°C and nominal supply voltages.
‡I_{DD1}-I_{DD4} are measured with open outputs.
NOTE 3: $V_{IL} \geq -0.6$ V on all inputs.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SMJ4416-15			SMJ4416-20			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	Input clamp voltage	I_I = −15 mA, see Figure 1			−1.2			−1.2	V
V_{OH}	High-level output voltage	I_{OH} = −2 mA	2.4			2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 5.8 V, V_{DD} = 5 V, All other pins = 0 V			±10			±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10			±10	μA
I_{DD1}‡	Average operating current during read or write cycle	At t_c = minimum cycle		40	48		35	42	mA
I_{DD2}‡	Standby current (see Note 3)	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		3.5	5		3.5	5	mA
I_{DD3}‡	Average refresh current	t_c = minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high		25	40		21	34	mA
I_{DD4}‡	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling		25	40		21	34	mA

†All typical values are at T_C = 25°C and nominal supply voltages.
‡I_{DD1}-I_{DD4} are measured with open outputs.
NOTE 3: $V_{IL} \geq -0.6$ V on all inputs.

capacitance over recommended supply voltage range and recommended temperature range, f = 1 MHz†

PARAMETER		SMJ4416		UNIT
		TYP‡	MAX	
$C_{i(A)}$	Input capacitance, address inputs	5	7	pF
$C_{i(RC)}$	Input capacitance, strobe inputs	8	10	pF
$C_{i(W)}$	Input capacitance, write enable input	8	10	pF
$C_{i/o}$	Input/output capacitance, data ports	8	10	pF

†These parameters are guaranteed but not tested.
‡All typical values are at T_C = 25°C and nominal supply voltages.

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switching characteristics over recommended supply voltage range and recommended operating temperature range

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	SMJ4416-12		UNIT
				MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 100 pF, Load = 2 Series 54 TTL gates	t_{CAC}		70	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, C_L = 100 pF Load = 2 Series, 54 TTL gates	t_{RAC}		120	ns
$t_{a(G)}$	Access time after $\overline{G}$ low	C_L = 100 pF, Load = 2 Series 54 TTL gates			30	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 54 TTL gates	t_{OFF}	0	30	ns
$t_{dis(G)}$	Output disable time after $\overline{G}$ high	C_L = 100 pF, Load = 2 Series 54 TTL gates		0	30	ns

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	SMJ4416-15		SMJ4416-20		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 100 pF, Load = 2 Series 54 TTL gates	t_{CAC}		80		120	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, C_L = 100 pF Load = 2 Series 54 TTL gates	t_{RAC}		150		200	ns
$t_{a(G)}$	Access time after $\overline{G}$ low	C_L = 100 pF, Load = 2 Series 54 TTL gates			40		50	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 54 TTL gates	t_{OFF}	0	30	0	40	ns
$t_{dis(G)}$	Output disable time after $\overline{G}$ high	C_L = 100 pF, Load = 2 Series 54 TTL gates		0	30	0	40	ns

timing requirements over recommended supply voltage range and recommended operating temperature range

		ALT. SYMBOL	SMJ4416-12 MIN	SMJ4416-12 MAX	UNIT
$t_{c(P)}$	Page-mode cycle time	t_{PC}	120		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	230		ns
$t_{c(W)}$	Write cycle time	t_{WC}	230		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	315		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (precharge time)‡	t_{CP}	40		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low§	t_{CAS}	70	5000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge time)	t_{RP}	80		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low¶	t_{RAS}	120	5000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	30		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	50		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	50		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	35		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	15		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	85		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	40		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	90		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	30		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high‖	t_{RRH}	10		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high‖	t_{RCH}	0		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	40		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	90		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	120		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	70		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write-cycle only)#	t_{CWD}	120		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	20	50	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write-cycle only)#	t_{RWD}	170		ns
t_{WLCL}	Delay time, $\overline{W}$ low to $\overline{CAS}$ low (early write cycle)	t_{WCS}	−5		ns
t_{GHD}	Delay time, $\overline{G}$ high before data applied at DQ		30		ns
t_{rf}	Refresh time interval	t_{REF}		4	ms

† All cycle times assume $t_t = 5$ ns.
‡ Page mode only.
§ In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time $t_{w(CL)}$.
¶ In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time $t_{w(RL)}$.
‖ These parameters are guaranteed but not tested.
Necessary to insure $\overline{G}$ has disabled the output buffers prior to applying data to the device.

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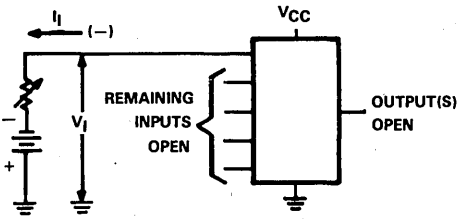
timing requirements over recommended supply voltage range and operating case temperature range

		ALT. SYMBOL	SMJ4416-15		SMJ4416-20		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(P)}$	Page-mode cycle time	t_{PC}	140		210		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	260		330		ns
$t_{c(W)}$	Write cycle time	t_{WC}	260		330		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	360		440		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (precharge time)‡	t_{CP}	50		80		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low§	t_{CAS}	80	5000	120	5000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge time)	t_{RP}	100		120		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low¶	t_{RAS}	150	5000	200	5000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	40		50		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	50	3	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	60		80		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	60		80		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	40		50		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	20		25		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	110		130		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	60		80		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	130		160		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	40		50		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high‖	t_{RRH}	10		10		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high‖	t_{RCH}	0		0		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	60		80		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	130		160		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	150		200		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	80		120		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write-cycle only)#	t_{CWD}	120		150		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	20	70	25	80	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write-cycle only)#	t_{RWD}	190		230		ns
t_{WLCL}	Delay time, $\overline{W}$ low to $\overline{CAS}$ low (early write cycle)	t_{WCS}	−5		−5		ns
t_{GHD}	Delay time, $\overline{G}$ high before data applied at DQ		30		40		ns
t_{rf}	Refresh time interval	t_{REF}		4		4	ms

† All cycle times assume $t_t = 5$ ns.
‡ Page mode only.
§ In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time $t_{w(CL)}$.
¶ In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time $t_{w(RL)}$.
‖ This parameter is guaranteed but not tested.

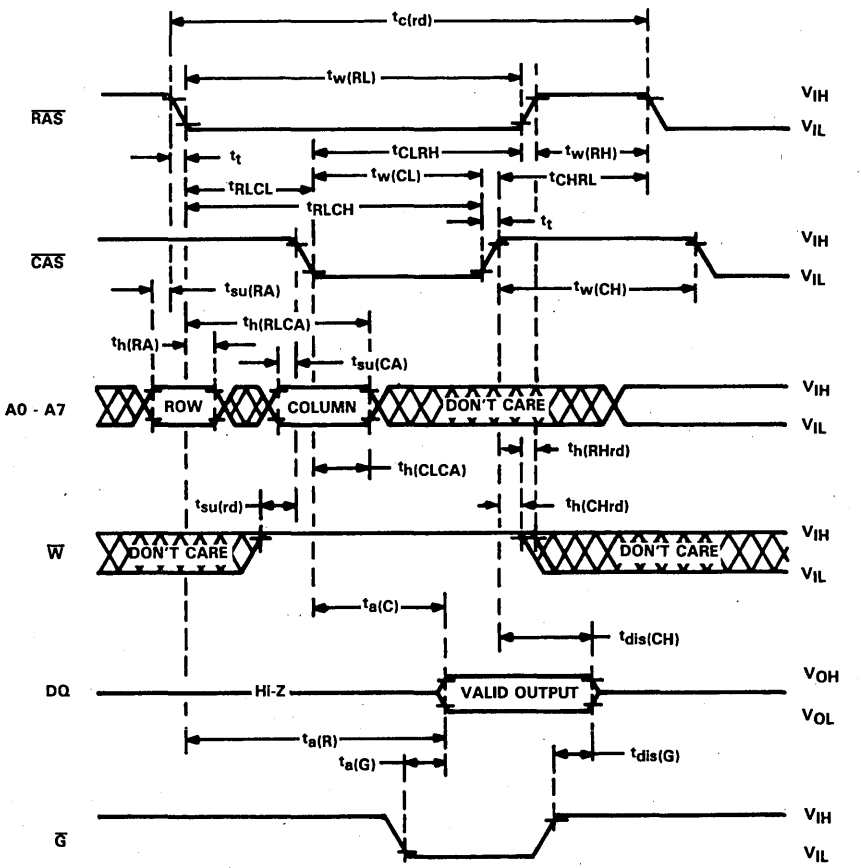
PARAMETER MEASUREMENT INFORMATION



NOTE 4: Each input is tested separately.

FIGURE 1. INPUT CLAMP VOLTAGE TEST CIRCUIT

read cycle timing



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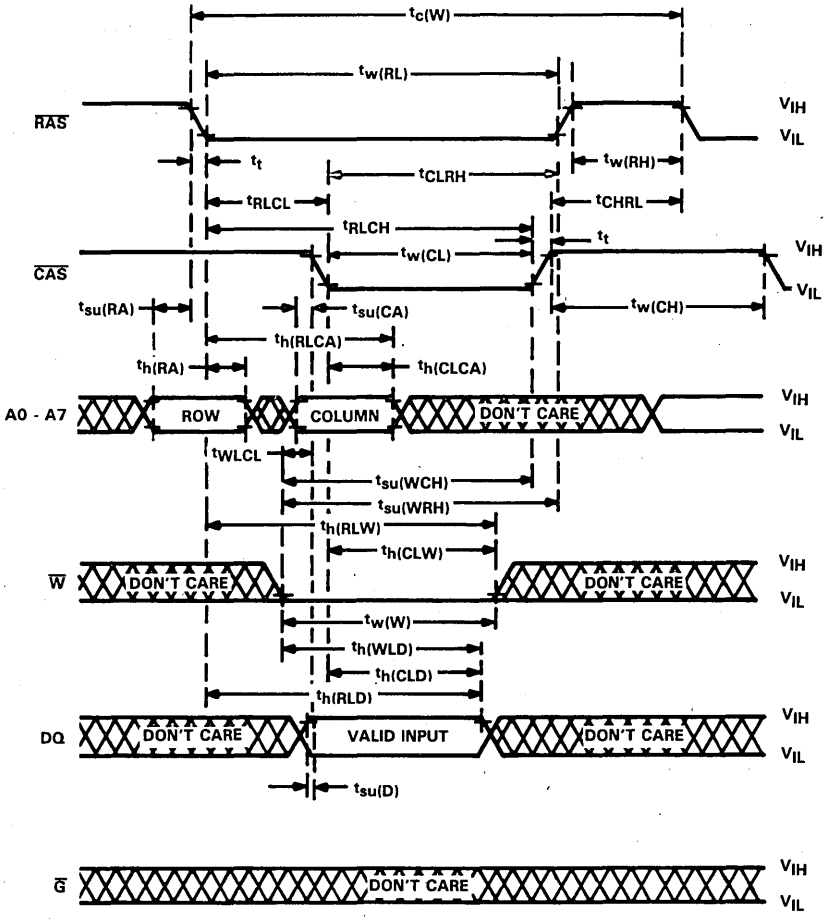
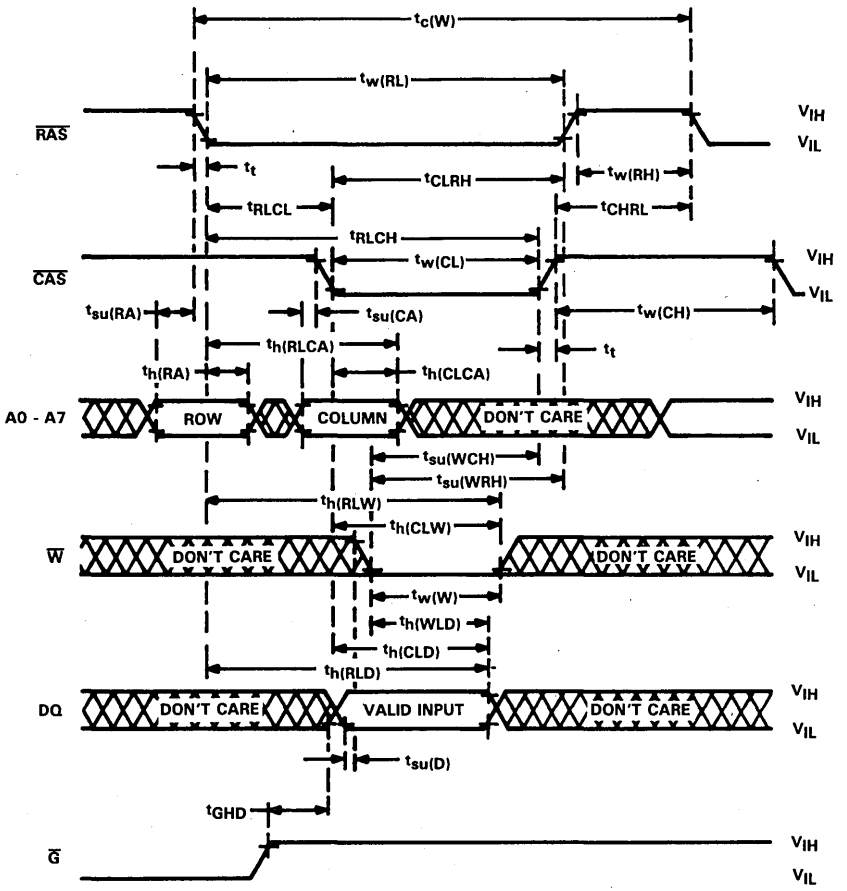
early write cycle timing



write cycle timing



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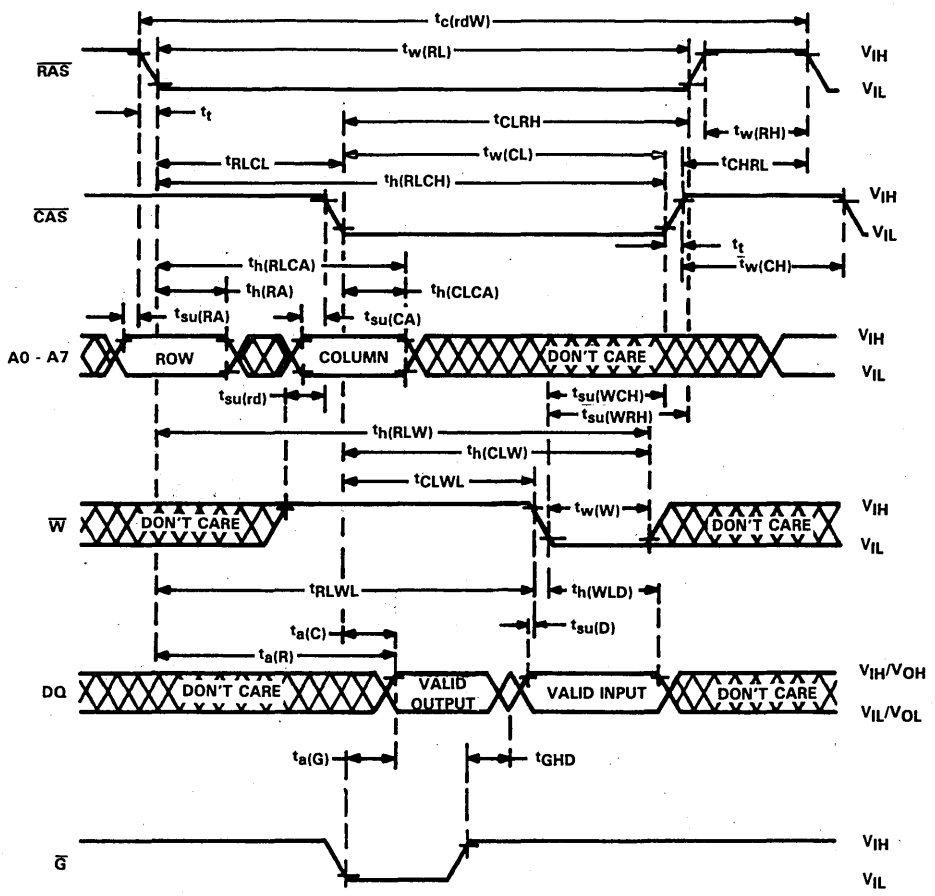
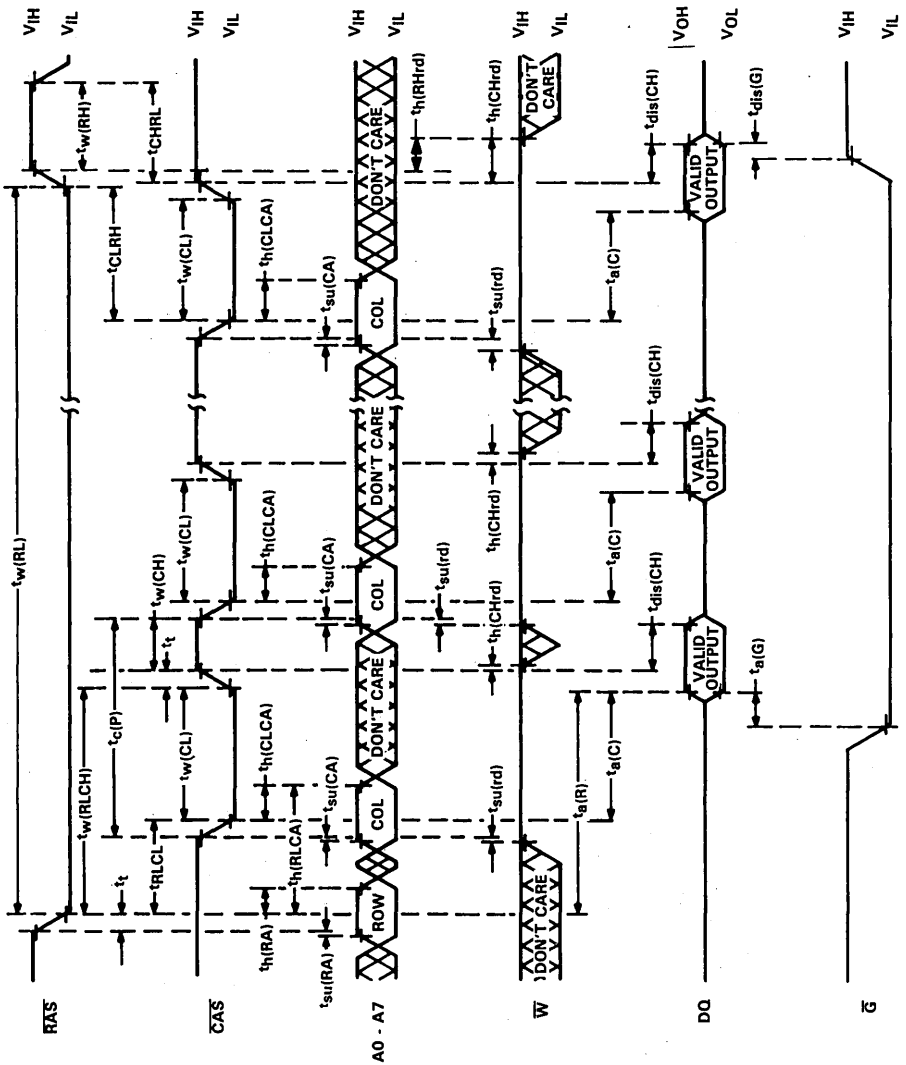
read-write/read-modify-write cycle timing



page-mode read cycle timing



NOTE 4: A write cycle or read-modify-write cycle can be intermixed with read cycles as long as the write and read-modify-write timing specifications are not violated.

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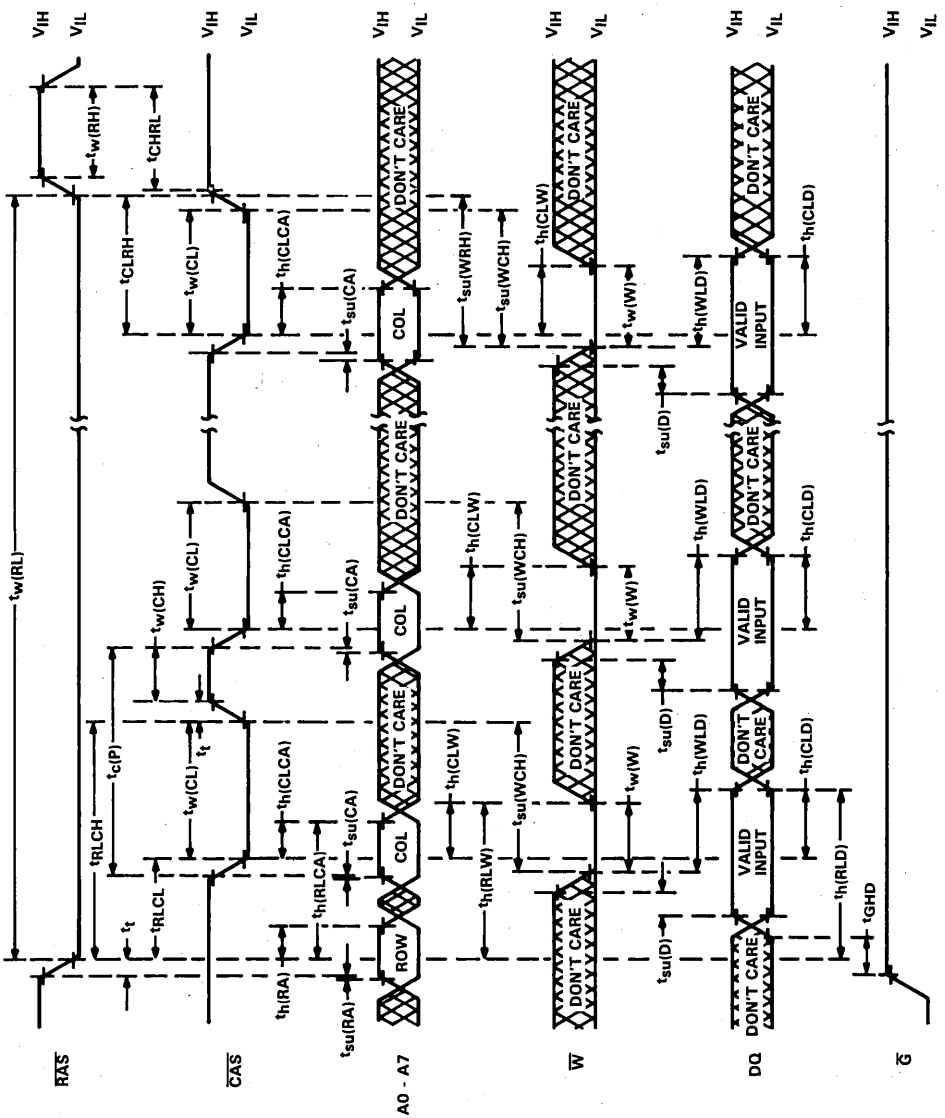
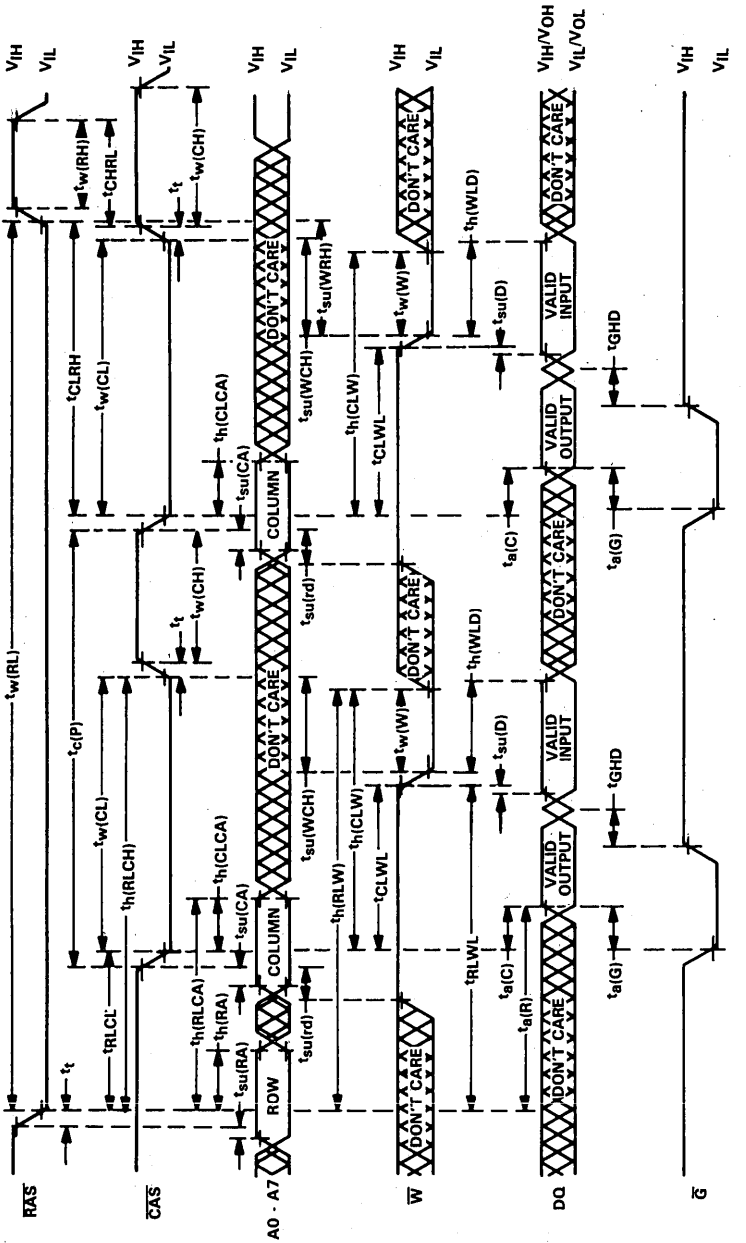
page-mode write cycle timing



NOTE 5: A read cycle or a read-modify-write cycle can be intermixed with write cycles as long as read and read-modify-write timing specifications are not violated.

page-mode read-modify-write timing



NOTE 6: A read cycle or a write cycle can be intermixed with read-modify-write cycles as long as read and write timing specifications are not violated.

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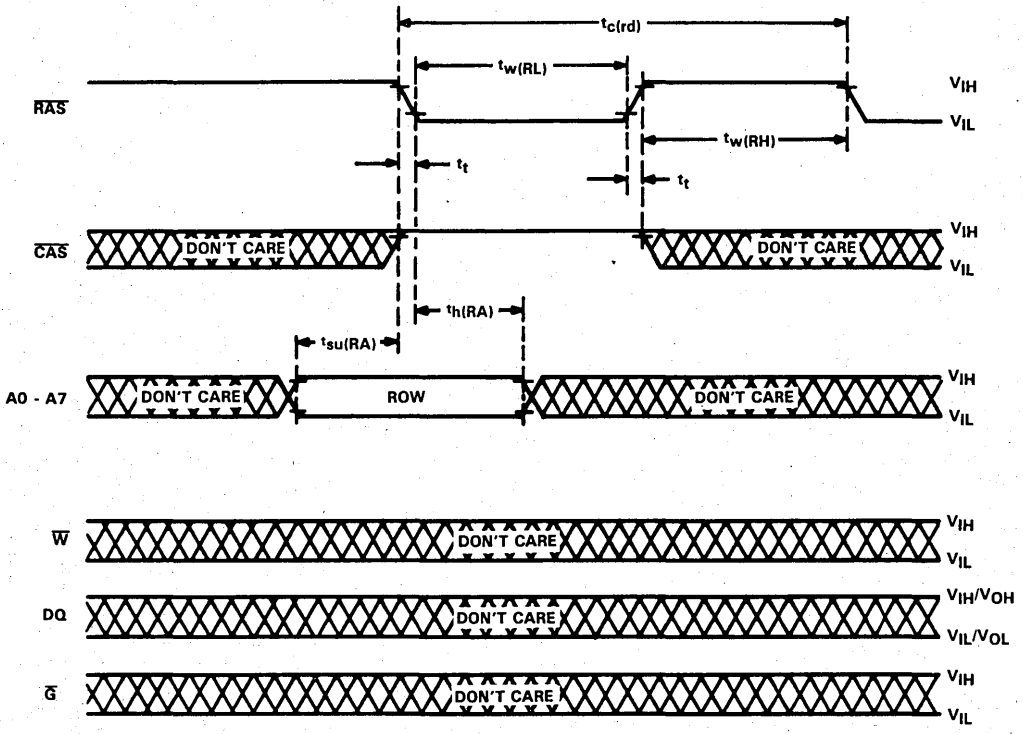
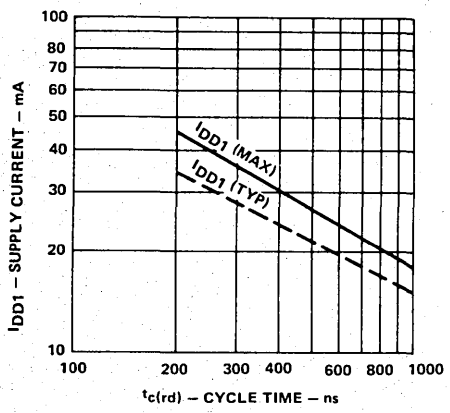
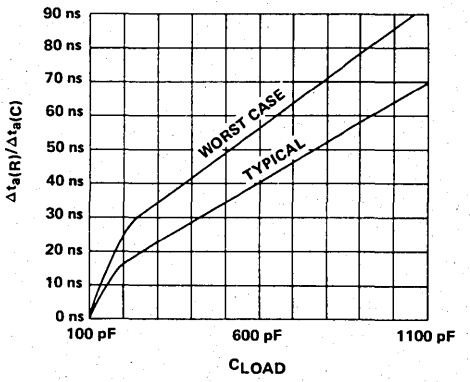
$\overline{RAS}$-only refresh timing



I_{DD1} VS CYCLE TIME



ACCESS TIME DERATING CURVE



TMS4164A and TMS4416 Input Diode Protection

The 64K DRAM family from Texas Instruments has departed from conventional input schemes for DRAMs to provide the user with improved ESD protection and input clamping diodes for negative undershoot. Both enhancements of device capability are possible due to the use by TI of a grounded epitaxial substrate in the manufacture of its 64K DRAMs. While the input circuit technique has provided the user with additional protection and ease of use, it may cause anomalous testing results for the unwary test engineer who tries to drive the inputs to large negative voltages.

Figure 1 shows an equivalent circuit for the input circuitry of the TMS4164A and the TMS4416.

The diode and transistor clamping circuit is the essential element in protecting the device from electrostatic discharge (ESD) damage. Figure 2 shows the physical layout of this circuit.

The essential element of the circuit is the input diode (A), which is surrounded by a diffused guard ring (B) connected to V_{SS}. This circuit can be viewed as a combination of a lateral NPN transistor, a bipolar diode, and a thick field transistor — all occupying the same area and connected to the input pad. The P−/P+ substrate is both the base of the transistor and the anode of the diode. Both are connected to V_{SS} through the resistance of the substrate from the surface of the chip to the backside. During an ESD with positive voltage, the input diffused area goes into reverse-bias breakdown, which turns on the bipolar transistor, thus clamping the input voltage. The action of the transistor is identical to second breakdown observed in conventional bipolar transistors. Once the transistor turns on, it can sink a large amount of transient current which is evenly distributed over the area of the input diffusion (collector of the lateral transistor). This avoids localized heating from the energy in the ESD. Localized heating could destroy the integrity of the input diode. For ESD with negative voltage, the diode and the transistor act to clamp the input voltage. When the input voltage drops below −0.7 V, the input diffusion appears as a cathode for a diode tied through the substrate resistance to ground. It also acts as an emitter for the lateral NPN transistor. Both elements turn on and tend to uniformly source the current in the input diffusion.

The polysilicon resistor included in the input circuit serves to limit the amount of voltage that reaches the thin oxide associated with the address buffers and clock inputs.

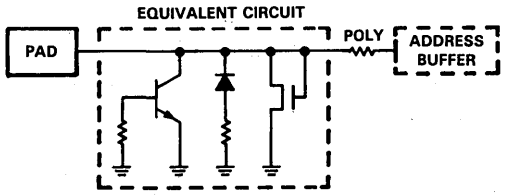
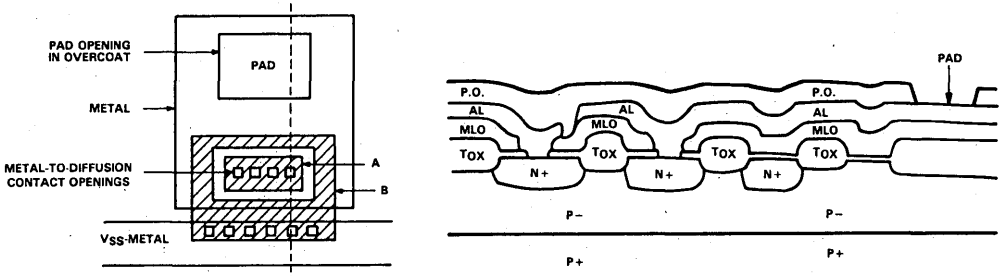


Figure 1. Equivalent Input Circuitry



(A) DIODE AND TRANSISTOR CLAMPING CIRCUIT

(B) CROSS SECTION OF CLAMPING CIRCUIT

Figure 2.

The dynamic impedance of the input clamping circuit is considerably lower than the resistance of the polysilicon resistor.

The input circuit also offers the advantage of clamping negative undershoots on the inputs during normal operation. While this provides advantage to the board and system designer, it can cause confusion for the test engineer unless he fully understands the limits of his tester. DRAMs have historically been specified with negative dc input voltages of -1 V. In addition, they are often tested/characterized to -3 V. This testing has been done to ensure that the devices will operate correctly with a negative input undershoot, which is transient. Such testing was required due to the inability of a MOSFET of reasonable size on the chip to clamp the negative-going input and due to the susceptibility of address input buffers on some MOS RAMs to negative input undershoots. The input clamping mechanism, provided on the TMS4164A and the TMS4416, can supply sufficient current to clamp the input transient.

Difficulty in testing the device with negative dc input voltages can occur due to the tester's output driver devices going into saturation when forward biasing the input diode. Also, most testers are unable to supply the large transient current requirement during reversal of bias on the input diode and transistor. Both effects will result in distortion of the tester's waveforms. What may appear to be poor setup and hold time margins of the device may actually be a tester's inability to supply the correct waveforms to the device at the proper time.

The improvement in both ESD protection and signal undershoot on system boards offered by the input circuit may be overlooked if erroneous conclusions are drawn from incoming testing with negative dc input voltages below -0.7 V.

TESTER LIMITATIONS WITH PROGRAMMED INPUT LOW LEVELS OF LESS THAN -0.7 V

Driver distortion occurs when input low levels are programmed for values below -0.7 V. The input diode/lateral NPN transistor shares a common PN junction which becomes forward biased at -0.7 V and below. The transistor collector, which is tied to V_{SS}, carries most of the forward-bias current (see Figure 3).

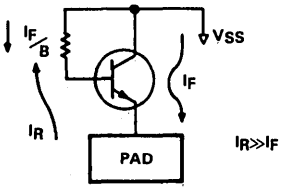
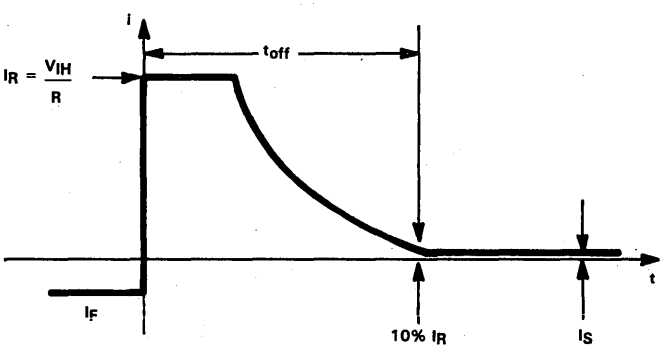


Figure 3. Forward- to Reverse-Bias Current

The diode exhibits a classical forward- to reverse-bias recovery delay due to a momentarily large reverse current of amplitude limited only by the programmed reverse voltage V_{IH} and driver output impedance R, i.e., the input approximates a momentary short circuit. An initially large short-circuit current plateau ($I_R = V_{IH}/R$) subsequently relaxes to the normal dc reverse-bias current I_S (see Figure 4). The time from the positive transition edge, corresponding to $t = 0$ in Figure 4, to the point where the reverse current surge relaxes to 10% of the plateau value is the diode recovery time (t_{off}).

Figure 5 shows how the driver output waveform is altered. During forward bias, the transistor clips the negative level at V_{FB} (in the range -0.7 V to -1.4 V) with the V_{IL}



R: Driver impedance
V_{IH}: Address input high-level (reverse-bias)

Figure 4. Forward- to Reverse-Bias Recovery Current

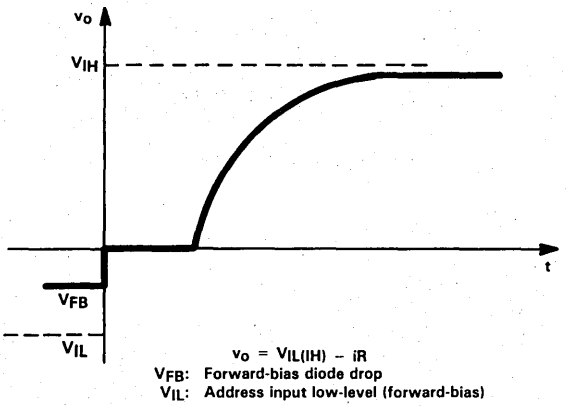


Figure 5. Address Driver Output Voltage

level programmed over the range of -0.7 V to -6 V. During the initial reverse bias, the driver output voltage v_O is given by the programmed V_{IH} level minus the iR drop across the driver output impedance, i.e.,

$$v_O = V_{IH} - iR$$

During the current plateau, the v_O value is essentially 0 V. The driver output voltage then recovers to the programmed value as the diode reverse current relaxes to the dc reverse-bias level I_S. In effect, the t_{off} value is a measure of the time that the output waveform is distorted if the unwary engineer programs V_{IL} values significantly below -0.7 V.

The following equation derived from diode switching theory serves to estimate the magnitude of the t_{off} values for input levels below -1 V.

$$t_{off} = 40\,[r - [r/(r + 1)]^2]\ \text{ns}$$
$$\text{where } r = -(V_{IL} + 1)/V_{IH}$$
$$\text{and } V_{IL} < -1\ \text{V}$$

The coefficient 40 ns is a characteristic of the diode structure and physical parameters of the material. For example, $V_{IL} = -3$ V and $V_{IH} = +3$ V give $t_{off} = 20$ ns. This estimate is not accurate at very small forward-bias values, because it ignores the rise time of the driver's positive transition edge. As long as the predicted value is greater than or equal to the edge transition time, the estimate is good. It is assumed that driver output impedance has the same value R at both upper and lower levels, V_{IH} and V_{IL}.

The distortion in driver waveform, shown in Figure 5, increases as the driver input low level is progressively driven more negative. Depending on driver output impedance, only slight distortion is observed in the positive transition for input levels near -0.7 V to -1 V. This irregularity corresponds to the onset of the recovery phenomenon short-circuiting the output of the driver. Significant distortion occurs at large negative values of V_{IL}, and the test engineer must be aware of this phenomenon to prevent erroneous conclusions as to the performance of the device.

The input transistor provides great advantage to device use in a system environment. In a system, the negative undershoot of an address line is caused by transient transmission-line reflections (undershoot of negative-edge transitions). Here the input transistor clips much of the swing below -0.7 V on the address line. Positive-edge transition from a settled negative address low level, which gives rise to the forward-to reverse-bias recovery delay, does not occur in the typical system environment.

TMS4164 and TMS4416 Interlock Clock

The TMS4164 (64K × 1) and TMS4416 (16K × 4) dynamic RAMs use a novel interlocked clock to yield enhanced immunity to process variations, temperature, and voltage induced parametric changes. The basic concept of an interlock clock structure is to provide a synchronous timing operation that eliminates race conditions. As an aid to understanding the interlock clock, an overview of the memory control structure and its functions will be presented first.

The TMS4164 (Figure 1) and TMS4416 (Figure 2) need a minimum of 16 address bits to address all of their 64K memory locations (2^{16} = 65,536). Instead of physically using 16 address pins, the DRAMs only use 8 address pins and receive the addresses in two parts of 8 bits each (8 (row) and 6 (column) in the case of the TMS4416). The first 8 addresses are called the row addresses; once stable on the address pins, they are latched by the low going edge of the row address strobe ($\overline{RAS}$) input. The 8 column address bits are then set up on the 8 address pins and latched by the low going edge of the column address strobe ($\overline{CAS}$) input. The TMS4416 only uses 6 of the column address lines, disregarding A0 and A7 (These will be utilized in next generation parts providing an address for 64K × 4 memories). This sharing of address lines is known as multiplexing which keeps the number of pins on a package to a minimum.

The TMS4164 and TMS4416 use a square array of memory cells consisting of 256 rows and 256 columns which is divided into an upper and lower half. A word line (which corresponds to a row) is connected to the transfer gates of 256 cells that comprise a row of memory. The transfer gates control access to the data stored on the memory cell capacitor. The bit line (which corresponds to a half of a column) has for each half of the array 128 memory cells and 1 dummy cell connected to it via the transfer gates. Located physically between the two halves of the memory array are 256 sense amps whose inputs connect to the bit lines from each half of the array. The dummy cell provides the reference (V_{REF}) to a sense amp to determine the state of the memory cell.

On an access cycle, the row decoders drive the selected word line high turning on all 256 transfer gates in the selected row and connect 1 memory cell to each bit line. Concurrently, dummy enable (DE) decodes and drives the transfer gates of one of the rows of dummy cells, and connects 1 dummy cell to each bit line on the opposite side of the sense amps. The dummy selection uses RA7 so that the row of dummy cells selected is on the opposite side of the sense amp from the selected row of memory cells. Connecting the memory and dummy cells to their respective bit lines causes a differential voltage to be established at the inputs of the sense amps. This differential voltage is then detected by the sense amps whose outputs will change to reflect the detected state of the memory cells. After sensing is completed, the output of the sense amp is driven back onto the bit lines to refresh the memory cells. Signal restoration is necessary because an access results in a destructive read (the memory cells no longer contain valid data after the access). This is due to the large bit line capacitance ($\approx$600 fF) and the relatively small capacitance of the cell (50 fF). Connecting the cell to the bit line depletes the cell charge, and makes refresh necessary to ensure valid data retention. This restoration is transparent to the user but should not be confused with providing external refresh. After sensing is completed, the data on the bit lines can now be selected by the column decoders. The column decoders select 4 of the 256 sense amps using A0-A5 (TMS4164) and A1-A6 (TMS4416) for the selection. On the TMS4164, these 4 bits are further decoded by a 1 of 4 decoder using A6 and A7 (the 4 bit output of the TMS4416 eliminates the need for the 1 of 4 decoder). This 1 of 4 selector acts as a bidirectional switch for data transfer to or from the sense amps. Now tha the basic blocks and functions of a DRAM have been described, a detailed look at the interlock scheme will be presented.

A simplified logic representation of the clock structure is shown in Figures 1 and 2. The clock interlock points are shown as inverting input NAND gates. The inputs represent timing events that must be complete before the output of the inverting input NAND gate can trigger a third event; this system provides interlocking. Approximately 60-100 clock signals are generated in a DRAM to control the various functions (address latching, decode timing, sensing, data transfers within the device, etc.); approximately 15 of these have been represented. The following discussion briefly shows the operation of the TMS4164 and TMS4416 DRAMs.

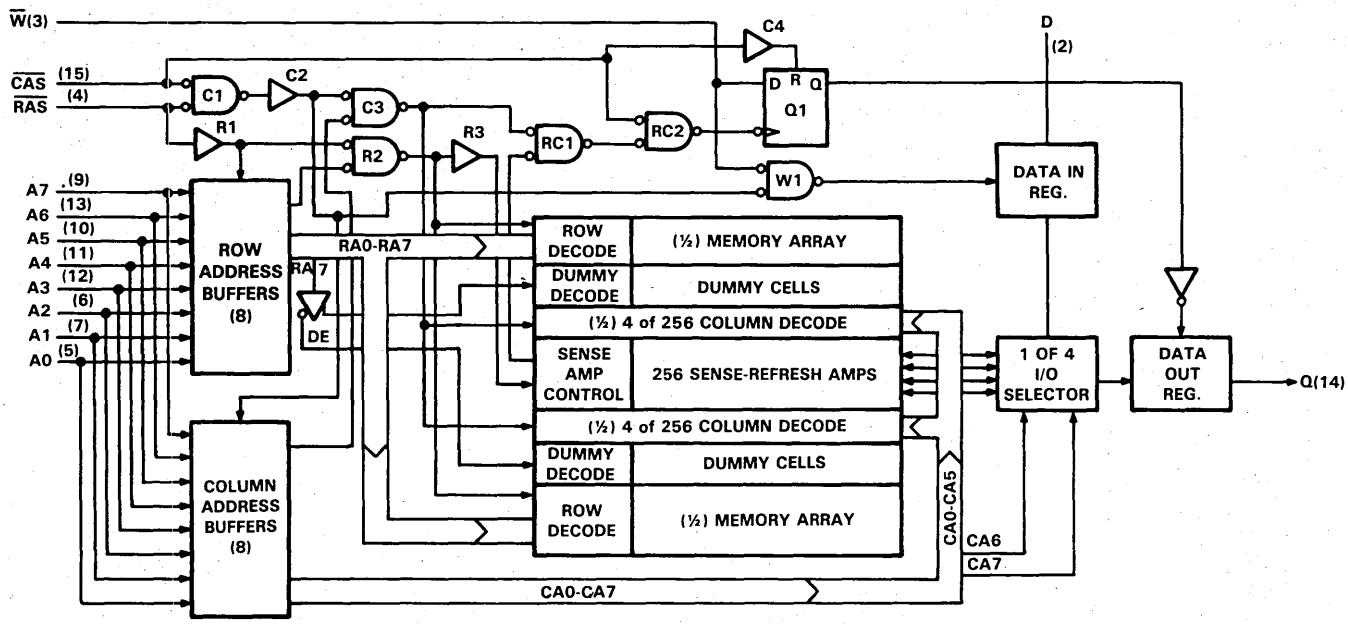


Figure 1. TMS4164 Block Diagram

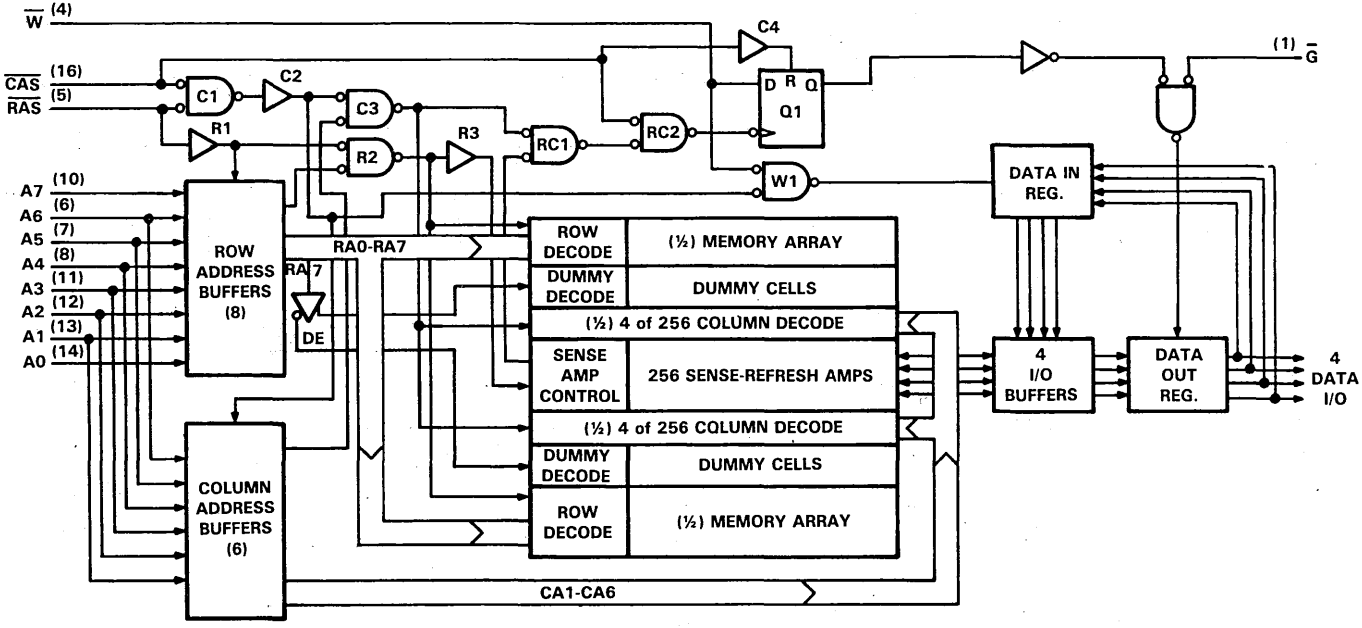


Figure 2. TMS4416 Block Diagram

The falling edge of $\overline{RAS}$ causes R1 to latch the row addresses into the row address buffers and enables interlock point R2. The row addresses are then amplified and drive the row decoders for row selection. When RA0-RA7 are valid, the row address buffers output a signal to interlock point R2. A delay stage within R2 allows the row decoders time to complete their decoding before the output of R2 goes low. R2 going low enables the row decoders to drive the selected word line high. Interlock R2 ensures two things: the row addresses are valid, and decoding is complete before the selected word line is activated. Address RA7 causes dummy enable (DE) to select the row of dummy cells on the opposite side of the array from the selected row of memory cells. After row and dummy selection is completed, the decoders then drive the appropriate word lines high, connecting the memory and dummy cells to their corresponding bit lines. The differential voltage at the inputs of the sense amp is sensed, amplified, and driven back onto the bit lines; this refreshes the memory cells in the selected row. The sense amp control then outputs a signal to interlock RC1 that indicates sensing is complete.

A high logic level on $\overline{CAS}$ holds the reset on Q1 active and forces the Q output of the data out buffer into a high-impedance state. A logic low level on $\overline{CAS}$ removes the reset to allow clocking.

The falling edge of $\overline{CAS}$ causes interlock C1 to go low (assuming $\overline{RAS}$ low) driving C2 low to latch the column addresses into the column address buffers. Interlock C1 ensures that the $\overline{CAS}$ cycle is inactive until $\overline{RAS}$ is low. The column addresses are then amplified and drive the column decoders for column selection. With CA0-CA7 valid, the column address buffers output a signal to interlock point C3. A delay stage within C3 allows the column decoders time to complete their decoding before the output of C3 goes low. C3 going low enables the column decoders to access the selected columns (4). Interlock C3 ensures two things: the column addresses are valid, and decoding is complete before the selected columns are accessed. After selection is completed, data can now either be input or output depending on the $\overline{W}$ signal timing. Interlocks RC1 and RC2 ensure that the sense amps are active and the proper column is selected before a read or write can take place.

In the case of a read or read-modify-write cycle, the high logic level on the write line ($\overline{W}$) prevents any transfer into the data in register by keeping the output of W1 high. The presence of $\overline{CAS}$ low and the output of RC1 low allows RC2's output to go low; this clocks the level of $\overline{W}$ into register Q1. Only in the case of an early write ($\overline{W}$ low prior to $\overline{CAS}$ low), when the output of Q1 is not clocked to a logic one, will the data out register be maintained in the high-impedance state. In any read cycle, the output of Q1 is a logic one and the data out register is enabled although data will not be valid until $\overline{RAS}$ and $\overline{CAS}$ access times are both satisfied.

In a write cycle, the low logic level on $\overline{W}$ allows the output of W1 to go low which latches the data present at D (thus the latter of either $\overline{CAS}$ or $\overline{W}$ going low latches the data). The logic level at the output of the data out register will remain until $\overline{CAS}$ returns to a high level. (When $\overline{CAS}$ is high, the output will go to a high-impedance state.) Data out reflects the data read from the cell rather than the new data that is written for read-modify-write cycles.

The $\overline{RAS}$ low time following sensing complete, is used to restore data to the memory cells currently selected by the word line (restoration after the destructive read). Any data that is changed by a write cycle causes alterations of the sense amplifier which then stores the new data in the memory cells. When $\overline{RAS}$ goes high, the word line is turned off and the cells now hold the data restored from the sense amps. $\overline{RAS}$ going high initializes a precharge state used to equalize the bit lines by charging them to full V_{DD} potential. Precharge is necessary to ensure the charge on the bit lines is equal on both sides of the sense amp. Another access cycle may begin once the precharge time has been met.

The representation used in Figures 1 and 2 is a simplified logic diagram which does not depict all points of signal interlocking. It does however demonstrate the principle of an interlocked clock scheme. The signal generation and timing becomes very critical as device delays decrease. In many dynamic RAMs there are over 100 timing signals used to control internal operations, and these timing signals are generated using delay chains without interlocking. The signal skew resulting from non-interlocked timing increases device sensitivity to operating conditions and process variations. Although the interlock clock is transparent to the user, its incorporation on the TMS4164 and TMS4416 offers greater component reliability and avoids timing race conditions inherent in previous generation DRAMs.

Introduction to Surface Mounting

ABSTRACT

The demand for high-density, cost-effective printed circuit boards has prompted the electronics industry to seek alternative methods to traditional plated-through-hole technology. One such alternative is surface mounting, a technology traditionally used in hybrid fabrication. The advantages of surface mounting are numerous but the bottom line is that it is cost effective and will begin to displace plated-through-hole technology as the availability of surface-mount components increases.

Texas Instruments is fully supporting the growth of the surface-mount industry with its line of plastic leaded chip carriers. An introduction to the surface-mount technology will be given in this application report.

INTRODUCTION

The post molded leaded chip carrier (PLCC) was developed by Texas Instruments in 1980 to improve the packing density of ICs on printed circuit (PC) boards and overcome some of the size constraints normally caused by dual-in-line (DIP) packages. The PLCC was also designed to be used under the same environmental conditions as the DIP without any reliability degradation. The PLCC occupies approximately 40% to 60% of the PC board area of an equivalent DIP, and requires no through holes (surface mount), therefore, it lowers the cost on PC boards. Unlike some surface-mounted packages, TI's PLCC requires no special PC board material considerations. The design of the lead provides compliance allowing the use of any commercial substrate. Digital, Linear, Gate Array, and MOS devices will be offered in 18-, 20-, 28-, 44-, 52-, 68-, and 84-pin packages through TI.

Package Outline

The mechanical data for the PLCCs is given in Figures 1 and 2; their thermal properties are listed in Table I. The following general statements apply to the packages:

1. Each of the chip carrier packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound withstands soldering temperatures with no deformation, and circuit performance characteristics remain stable when the devices are operated in high humidity conditions.
2. These packages are intended for surface mounting on solder pads with 1,27-mm (0.050-inch) centers. The leads require no additional cleaning or processing when used in soldered assembly.
3. All dimensions shown are metric units (millimeters), with English units (inches) shown parenthetically. Inch dimensions govern.
4. Lead spacing shall be measured within the zones specified.
5. Tolerances are noncumulative.
6. Lead material CD-155. T60 (Copper Alloy).
7. Dimple in top of package denotes pin 1.

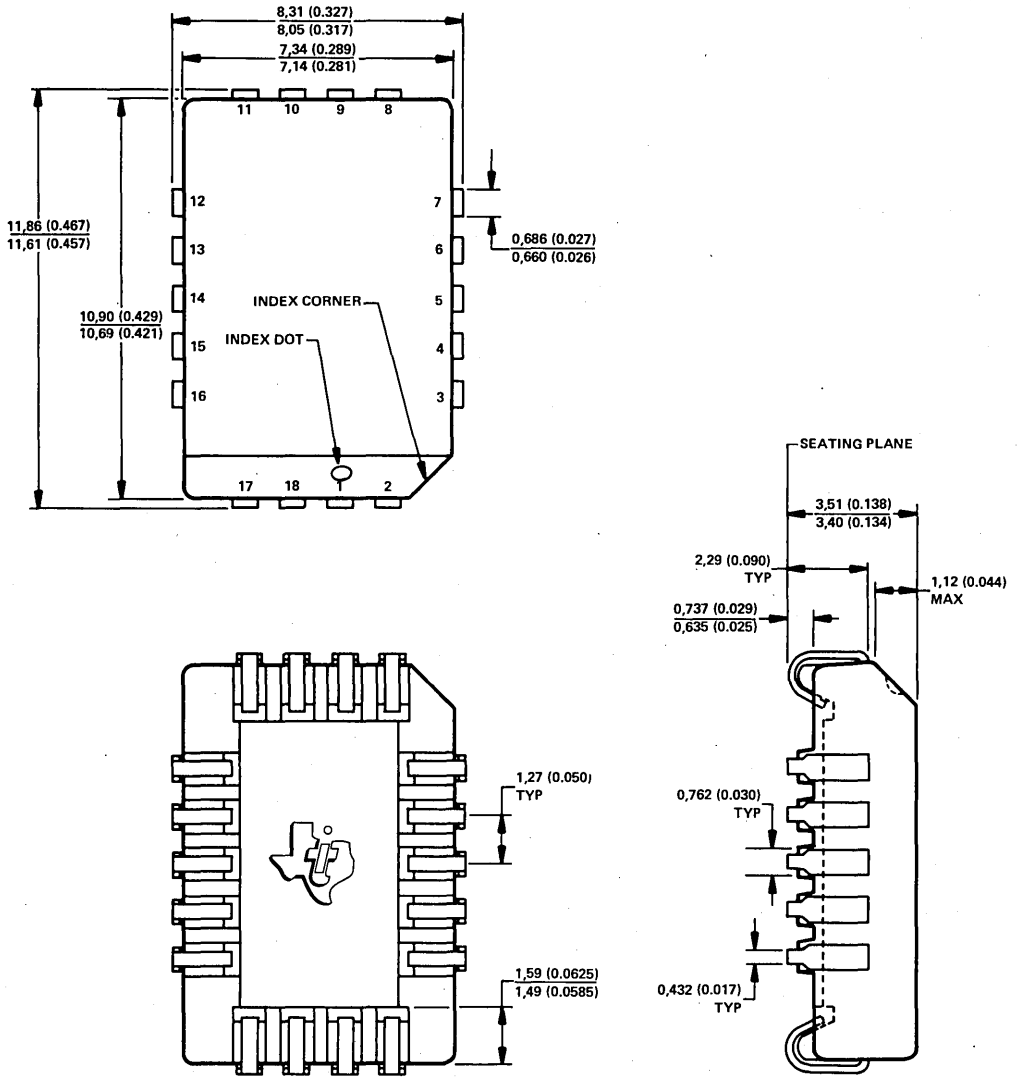
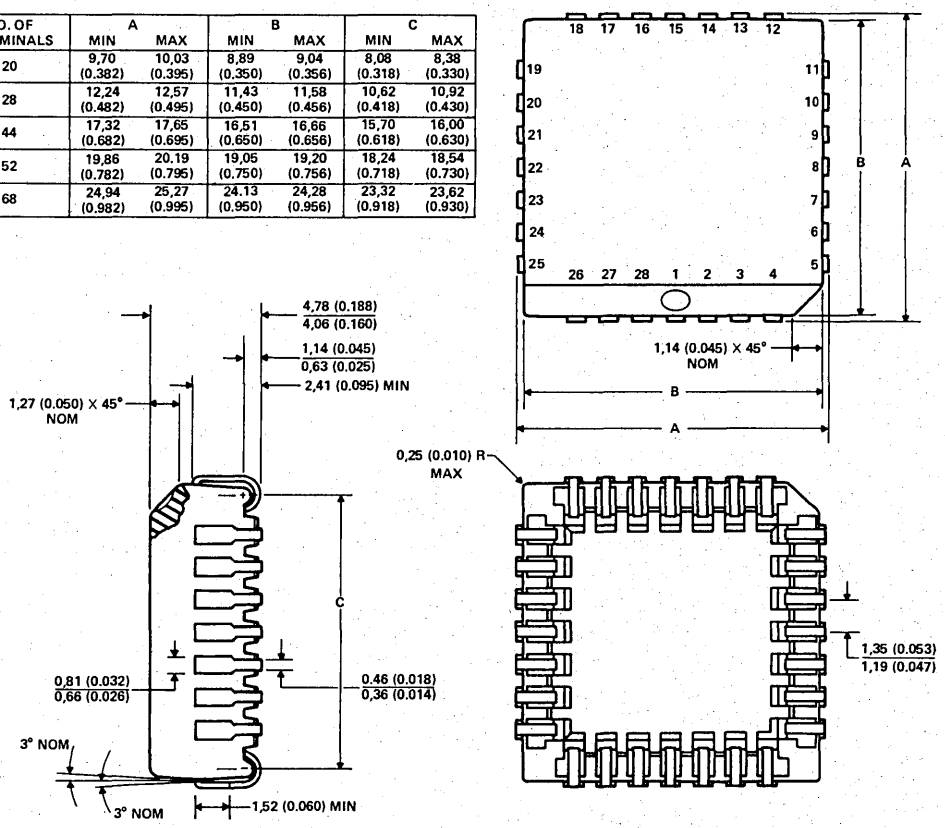


Figure 1. Plastic Chip Carrier Package (FP Suffix)

NO. OF TERMINALS	A		B		C	
	MIN	MAX	MIN	MAX	MIN	MAX
20	9,70 (0.382)	10,03 (0.395)	8,89 (0.350)	9,04 (0.356)	8,08 (0.318)	8,38 (0.330)
28	12,24 (0.482)	12,57 (0.495)	11,43 (0.450)	11,58 (0.456)	10,62 (0.418)	10,92 (0.430)
44	17,32 (0.682)	17,65 (0.695)	16,51 (0.650)	16,66 (0.656)	15,70 (0.618)	16,00 (0.630)
52	19,86 (0.782)	20.19 (0.795)	19,05 (0.750)	19,20 (0.756)	18,24 (0.718)	18,54 (0.730)
68	24,94 (0.982)	25,27 (0.995)	24.13 (0.950)	24,28 (0.956)	23,32 (0.918)	23,62 (0.930)



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

Figure 2. FN Plastic Chip Carrier Package

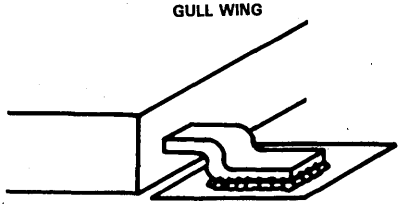
Table I. Thermal Properties, of Plastic Chip Carriers

NO. OF LEADS	PACKAGE DESIGNATION	θJA (° C/N)	θJC (° C/W)
18	FP	85.4	13.8
20	FN	113.6	37.1
28	FN	76.8	32.2
44	FN	68.0	20.3
68	FN	45.7	11.4

J-Lead Advantage

Texas Instruments PLCC packages are constructed with the J-lead structure due to its superior performance when mounted on a wide spectrum of substrates ranging from ceramic to epoxy-glass. This is possible due to the compliancy of the J-lead which compensates for the possible thermal mismatch between plastic packages and mounting substrates. More care must be taken when using ceramic leadless chip carriers mounted on nonceramic substrates in order to prevent solder joint fracturing under thermal cycling. The J-lead also offers advantages over plastic surface-mount packages using different lead structures. Figure 3 gives a comparison of the J-lead used on the PLCC to the "gull wing" commonly used on small-outline integrated circuits (SOICs) and "quad packs."

GULL WING



DEVICE AREA (16 L-PIN SOIC) = 111,6 mm^2 (0.173 in^2)

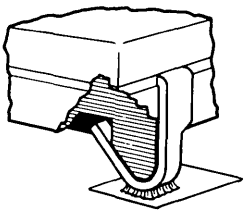
ADVANTAGES

- PROVEN PROCESS
- POSITIVE SOLDER "WITNESS"
- EASY AUTO-POSITIONING
- NESTED STACKING (PERIPHERAL)

DISADVANTAGES

- EXTENDS X-Y SIZE
- LEADS SUBJECT TO DAMAGE
- HIGH PIN COUNT PACKAGES IMPRACTICAL

J-LEAD



DEVICE AREA (18-PIN PLCC) = 98,6 mm^2 (0.153 in^2)

ADVANTAGES

- PROVEN PROCESS
- LEADS ARE COMPLIANT, USEABLE WITH PC BOARD AND CERAMIC SUBSTRATES
- MINIMUM X-Y SIZE, MAXIMUM BOARD DENSITY
- EASY AUTO POSITIONING
- LEADS WELL PROTECTED
- EASY REPLACEMENT
- SOCKETING EASY
- JEDEC STANDARDS EXIST
- STAND-OFF FROM THE BOARD ALLOWS EASY CLEANING
- LARGEST LINE OF AVAILABLE PACKAGES: FROM 18 TO 68 LEADS. HIGHER PIN COUNTS UNDER DEVELOPMENT

DISADVANTAGES

- TOTAL PACKAGE-HEIGHT THICKER THAN SOIC
- INFRARED (IR) REFLOW DIFFICULT

Figure 3. Gull Wing Vs. J-Lead

Area Savings with PLCC

The PC board area savings that can be realized with the PLCC is best demonstrated by a comparison of two Texas Instruments one megabyte memory boards (see Figure 4). The DIP board is eight layers, measuring 279,4 mm (11 inches) by 355,6 mm (14 inches) with 226 ICs. The PLCC board is four layers, measuring 165,1 mm (6.5 inches) by 243,84 mm (9.6 inches) also with 226 ICs. The savings that can be realized with the PLCC board amounts to 60% less board area at an overall cost savings of approximately 55%. This illustrates the viability of surface mount as a low cost means of improving circuit board density while reducing PC layout complexity.

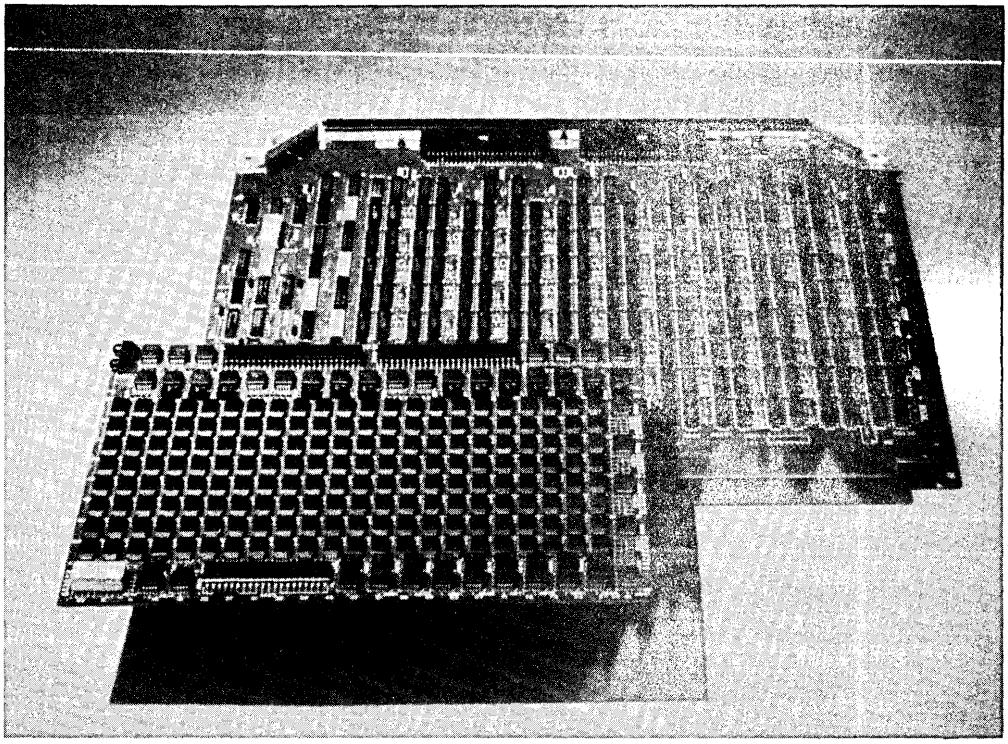


Figure 4. PLCC and DIP One Megabyte Memory Expansion Boards

Surface Mount Component Availability

Most IC manufacturers are presently producing surface-mount components for a large part of their product line. The devices available range from the sophisticated VLSI to the discrete transistor. Non-integrated circuit components ranging from chip resistors and capacitors to surface-mount connectors are also being produced in volume by major manufacturers. As the demand for surface-mount components increases, most products now produced for standard through-hole technology will also be available in surface mount. As of the printing of this application report TI produces over 700 ICs in surface mount packages.

Surface mounting consists of five basic steps:

1. PC board design
2. Solder paste application
3. Component mounting
4. Oven drying (optional)
5. Solder reflow

A brief description of each step will be given; detailed descriptions of the various steps can be obtained by component and equipment suppliers and from numerous technical articles on surface mounting.

PC Board Design

To produce reliable surface-mount PC boards the designer has to pay particular attention to IC solder pad (also termed footprint) layout. Not providing adequate footprint area and proper orientation will generally yield poor solder joints and lack of self-centering during reflow. Figure 5 shows the recommended footprints for the 18-pin PLCC. When laying out the IC footprints, as a general rule the footprint should extend approximately 10-15 mils past the outer edge of the PLCC lead. This provides a good solder fillet that will extend up the outer edge of the PLCC lead to yield a reliable solder joint that is easily inspected. The 70-80 mil length of the footprint should be a minimum, however a longer footprint can be used. It is recommended that the dimensions A and B never be less than the minimum width or length of the IC.

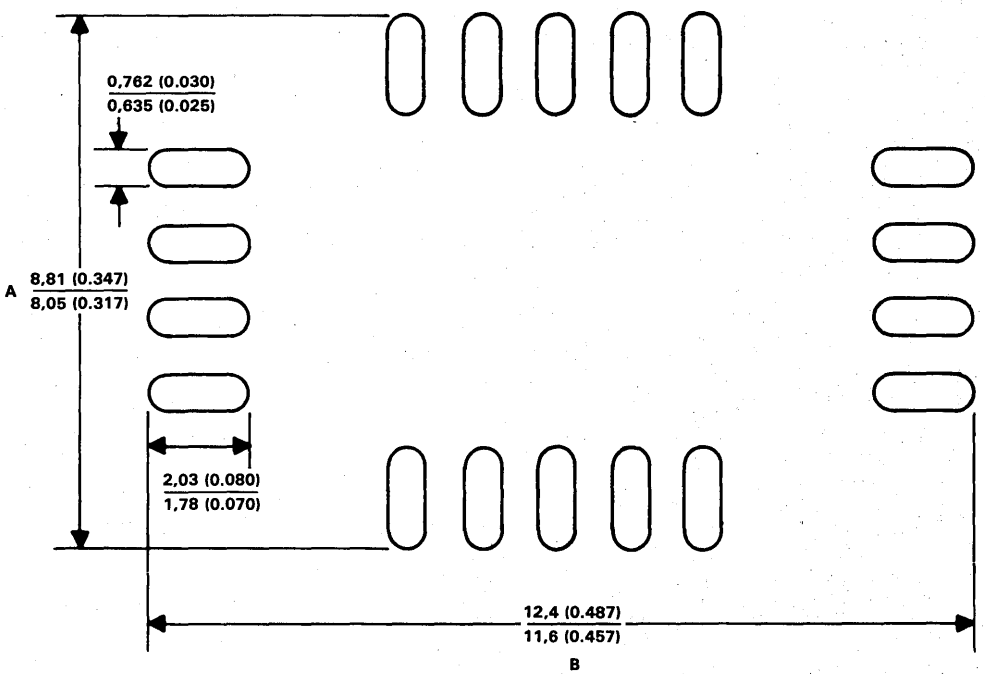


Figure 5. 18-Pin PLCC Footprint

Solder Paste Application

Solder paste can be applied using several methods: screening through a stencil or stainless steel mesh, pneumatic dispensing or by hand application with a syringe. Texas Instruments recommends screening through a stainless steel screen. The screen mesh must be chosen in accordance with the mesh of the solder paste to provide an adequate emulsion of the solder paste and to prevent screen clogging. In general an 80-100 mesh screen should be used with 200 mesh or finer solder paste particle. There are a number of factors that need to be considered when selecting a solder paste, a few key factors are as follows:

1. Particle size
2. Particle shape
3. Percentage of metal content
4. Temperature range

Component Placement

The components can be placed via several different modes into the still moist solder paste. In a production environment, the components are most efficiently placed with an automatic pick-and-place machine to achieve both speed and accuracy. Presently, pick-and-place machines can place between 600 and 600,000 components per hour and are priced accordingly. In a research and development environment, hand placement can be adequate due to the forgiving nature of surface mounting. When a component is placed off center it will tend to self-align during reflow due to the surface tension of the molten solder. Naturally there are limits to the amount of misalignment that can be corrected. Two important aspects of self-alignment are provision of adequate solder pad area, and proper placement of the solder pads with respect to the component.

Oven Drying

As solder pastes have evolved over the past several years, the drying process following component placement is not always necessary. In the past, drying was necessary to drive out the solvents in the solder paste. If the solvents were not driven out, the formation of solder balls was frequent due to the out gassing of the solvents prior to reflow. Today manufacturers of solder pastes report that drying is no longer necessary when using many of the new solder paste formulations. As a wide variety of solder pastes exists, it is necessary to consult the manufacturer before determining if drying is necessary in your process.

Solder Reflow

While several methods of solder reflow are available, vapor phase soldering has been the most successful and is becoming the industry standard.

Two types of vapor phase systems are the batch and the in-line.The batch system is a two-vapor system that uses a fluoroinert liquid such as FC-70 for the primary vapor and a clorofluorocarbon such as trichlorotrifluoroethane (R113) as the secondary liquid (see Figure 6). The secondary liquid has a lower boiling point (47.6°C) than the primary liquid (215°C) thus acting as a blanket to prevent loss of the expensive primary liquid. The in-line system (see Figure 7) is a single-vapor system using only a primary vapor (such as FC-70). The batch system is the forerunner of the in-line and is more suited to development and small production where the in-line is tailored to a mass production atmosphere requiring good throughput and minimal operating expense. Although the two systems are targeted to different markets their basic operation is the same. Both are capable of single and double sided surface mount.

Batch System Operation

The PC board complete with components is placed on an elevator and lowered into the secondary vapor. The elevator ascent-descent rate and dwell in the two vapor zones can be preset via the vapor phase machine front panel. The descent rate and hold time in the secondary zone should be set so as not to unnecessarily disrupt the secondary vapor blanket or cause defluxing of the solder paste. Lowering the board into the 215°C primary zone causes the solder to reflow. A dwell time of 10-30 seconds in the primary zone is generally sufficient for most PC boards. The dwell time in the primary zone is a function of the PC board mass. Once the solder is reflowed, the PC board is raised back into the secondary zone where the molten solder is allowed to solidify. In the batch system it is necessary to pay particular attention to the ascent-descent rate of the elevator as the disruption of the two-vapor zones will cause unnecessary loss of the expensive primary liquid.

In-Line System Operation

The operation of the in-line system is similar to that of the batch system except that there are no secondary vapor or dwell times with which to contend. The PC board is placed on a conveyor belt that transports it through the system at a constant speed. Passing through the vapor zone the solder becomes molten and solidifies as it moves toward the systems exit. Where the ascent-descent rate and dwell time are critical to the batch system, the conveyor speed is critical to the in-line system. The speed at which the conveyor should be set is also a function of the PC board mass.

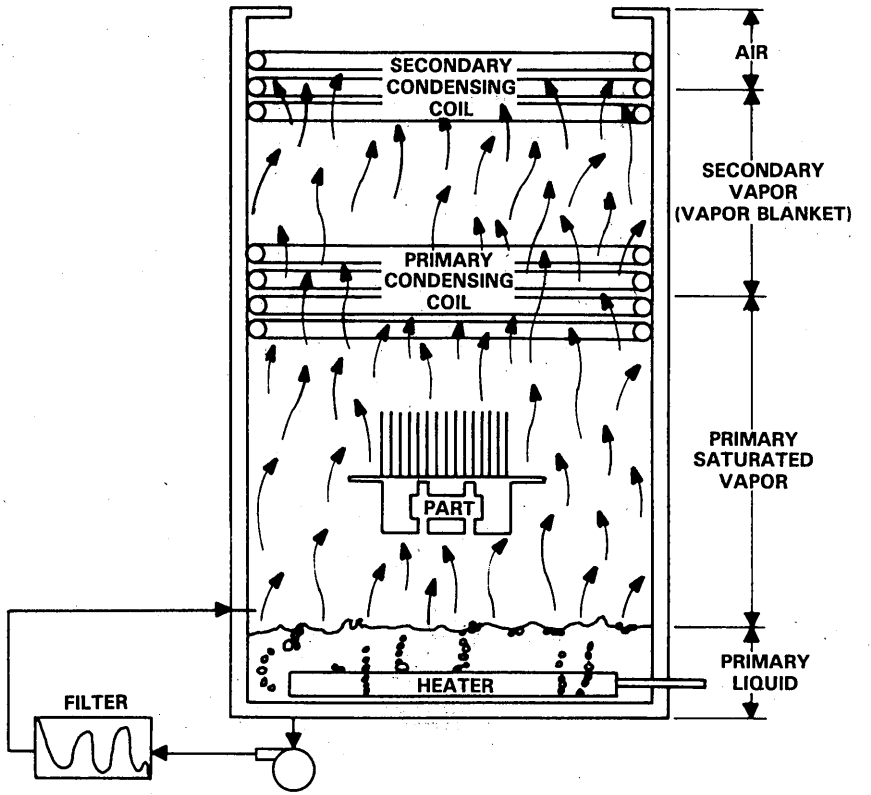


Figure 6. Vapor Phase Reflow System with Secondary Vapor Blanket

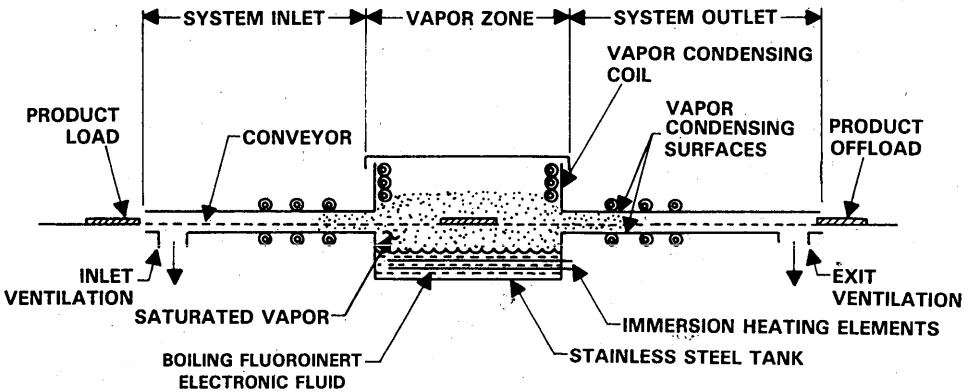


Figure 7. In-Line Single Vapor Heating System Schematic

Cleanup

Following the soldering process, it is necessary to remove the flux residues. These residues can be removed by traditional cleanup methods if the components have approximately 5 mils clearance to the PC board. One benefit of the PLCC with its J-leads is that it provides approximately 29 mils of clearance. Special soaking, agitation, or other methods will be necessary to provide adequate cleanup for components with less that 5 mils of clearance.

CONCLUSION

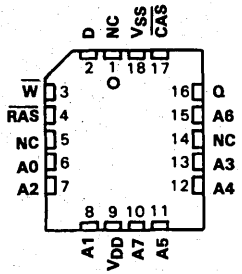
A brief overview of surface-mount technology has been given showing its advantages over standard plated-through-hole technology. Surface mounting is a cost-effective, sensible solution to the ever increasing demand for denser circuit boards. Detailed information about surface mounting is available from most major component and equipment manufacturers and through numerous technical articles on the subject. As the electronics industry strives to implement more functions in a given area, Texas Instruments believes surface mounting will become the predominant mounting technology of the future.

MOS Memory
Applications Engineering

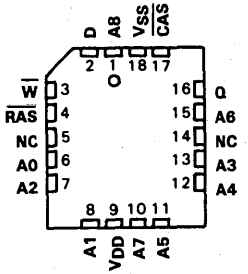
64K-256K Plastic-Leaded Chip Carrier Compatibility

Designing memory arrays compatible with Texas Instruments 64K and 256K DRAMs in plastic leaded chip carrier (PLCC) is easily accomplished through proper PC board design. Unlike the 64K and 256K DIP packages which are identical, the PLCC packages have definite physical differences. This Application Report will cover those differences and how to design for compatibility along with a few general rules on PLCC footprint layout.

To design a 64K-256K compatible PLCC memory array, pin and package outline compatibility need to be considered. Figures 1 and 2 show both devices with their respective pin assignments and package outlines. The pin assignments for both devices are identical with the exception of pin 1. On the 64K package, pin 1 is a no connect (NC) and on the 256K package, pin 1 is address eight (A8). This presents no problem as the 64K device will ignore this input. The major difference between the two packages is their physical size. The 64K device is packaged in the JEDEC standard 290 mil X 425 mil (nominal) PLCC while the 256K will be packaged in the 290 mil X 490 mil PLCC. The increase in package size for the 256K device is due to its larger chip size.



a. 64K X 1

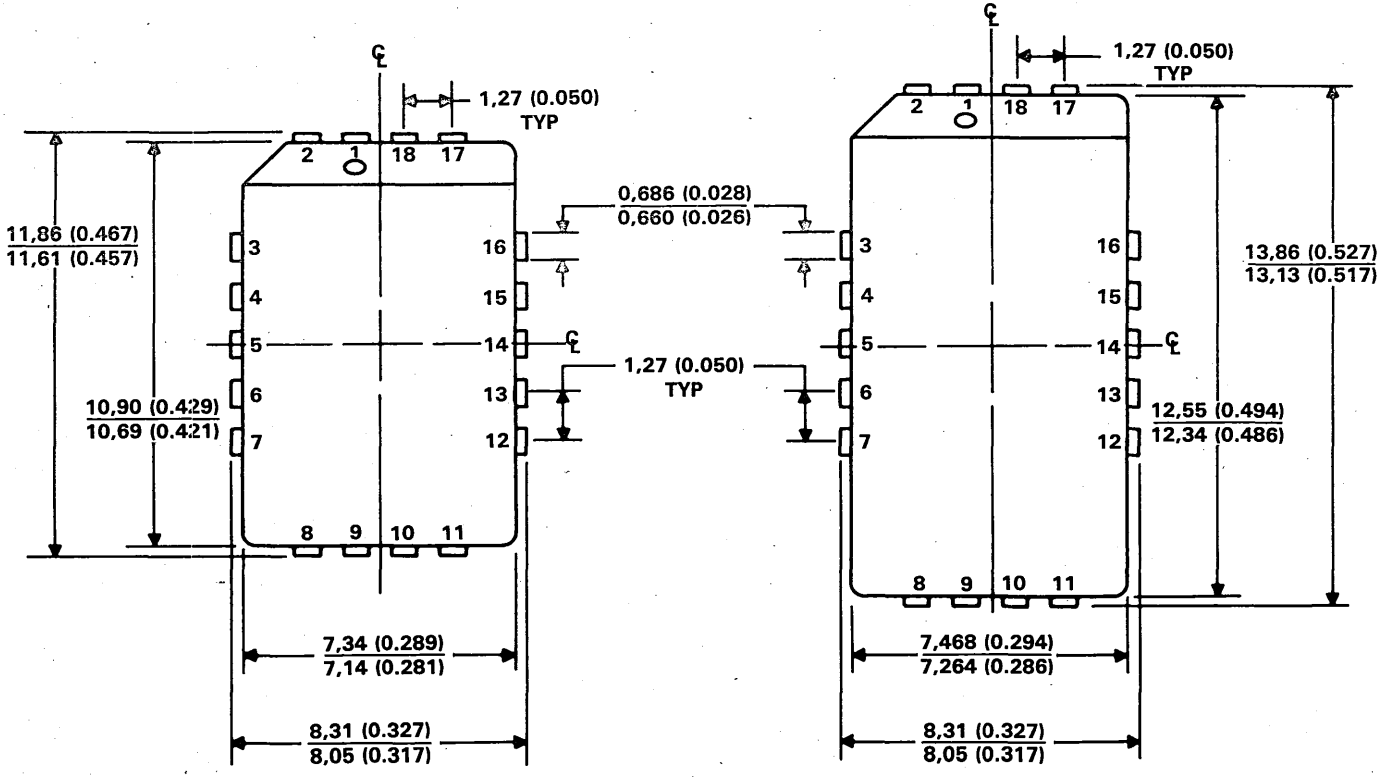


b. 256K X 1

c. 64K X 1/256K X 1

PIN NOMENCLATURE	
A0-A8	Address Inputs
$\overline{CAS}$	Column Address Strobe
D	Data In
NC	No Connection
Q	Data Out
$\overline{RAS}$	Row Address Strobe
V_{DD}	+5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

Figure 1. PLCC Pin Assignments



a. 64K X 1

b. 256K X 1

Figure 2. 64K and 256K PLCC Mechanical Data

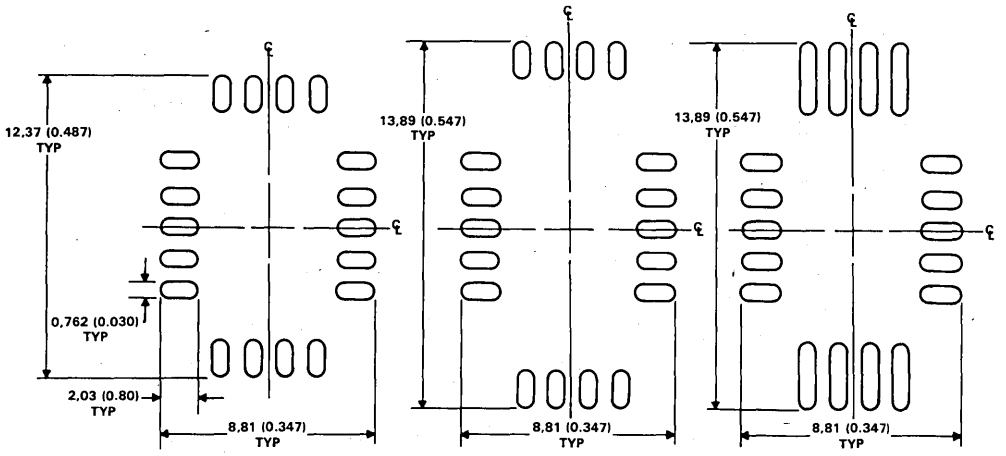


Figure 3. PLCC Footprints

Designing a PLCC memory array to accommodate both package sizes is accomplished through appropriate PLCC footprint layout. The 64K, 256K and 64K-256K PLCC footprints with recommended mechanical dimensions are given in Figure 3. The only difference between the 64K and 256K footprints are the location of the solder pads across the top and bottom of the footprints (necessary to accommodate the differences in package length). By overlaying the two footprints a 64K-256K compatible footprint can be obtained. Notice that the solder pads along both sides are unchanged from the 64K and 256K footprints while the solder pads across the top and bottom have been stretched. The only drawback to the 64K-256K compatible footprint is that when using 64K devices some memory density is sacrificed due to the extra pad length at the top and bottom of the footprint. However, this may not be a serious constraint compared to the cost of laying out and producing two separate memory boards.

To arrive at the PLCC footprint dimensions in Figure 2, several general design rules were used. Adhering to these design rules helps to ensure good solder joint integrity between the PC board and the PLCC.

1. Solder pad length should be 70-80 mils; shorter pads may cause poor solder joints, longer pads can be used but require more board area.
2. Solder pad width should be 25-30 mils.
3. The solder pads should extend a minimum of 10-15 mils past the outer edge of the PLCC leads. This provides a good solder fillet that will extend up the outer edge of the PLCC lead to yield a reliable solder joint that is easily inspected.
4. Footprints must be symmetrical. Solder pads on opposing sides should be of equal length and width. Solder pads on adjacent sides do not have to be of equal length and width.

This Application Report has illustrated that the 64K and 256K PLCC are compatible through proper footprint layout. Also several general footprint design rules were presented to help ensure solder joint integrity.

MOS Memory
Applications Engineering

High-Performance Memory Access with the TMS4161

The dual-port concept of the TMS4161 Multiport Video RAM eliminates the large bottleneck caused by display refresh overhead by dedicating a high-speed serial port to that requirement. This enhances performance by eliminating the need for processor access to share the random-access port with display refresh. The random-access port can also be configured with a system to provide enhanced system performance over a standard memory access cycle. This involves interleaving the display memory such that multiple CPU memory access cycles coincide with a single VRAM memory access cycle. This application report presents a method in which system timing generation supports the access of interleaved banks of display VRAMs.

Figure 1 exemplifies the memory configuration for a 1024 × 1024 resolution, four-plane graphics system. Memory mapping of the display requires 1024 × 1024 or 1M-bits of memory per plane or a total of 64 TMS4161 devices (16 in each of the four planes). Four pixel planes are utilized to enable 16 colors to be displayed on the screen simultaneously.

Four 16-bit parallel-to-serial shift registers are added externally to correspond to the four pixel planes. The serial port of the 16 TMS4161's feed into the 16-bit external shift register which will require a reload of the on-chip 256-bit shift register every 16 × 256 or every 4096 pixels (four scan lines). A TMS4161 shift register reload operation involves the transfer of a designated row of memory to the on-chip 256-bit shift register. This transfer operation is completed within a single memory cycle. In addition, the 256-bit shift register of the TMS4161 can be segmented into cascaded 64-bit increments by virtue of a selectable tap point. An alternate scheme to consider is to set the tap points on the internal 256-bit shift register of the 4161 to 64-bit increments. This allows an internal TMS4161 memory-to-shift-register transfer to occur on every scan line. With every scan line transfer, the tap point on the internal shift register will be set to the next sequential 64-bit tap point, and that section will be shifted out. Tap point utilization may serve to simplify graphics system design since memory transfer cycles will automatically occur after displaying every scan line.

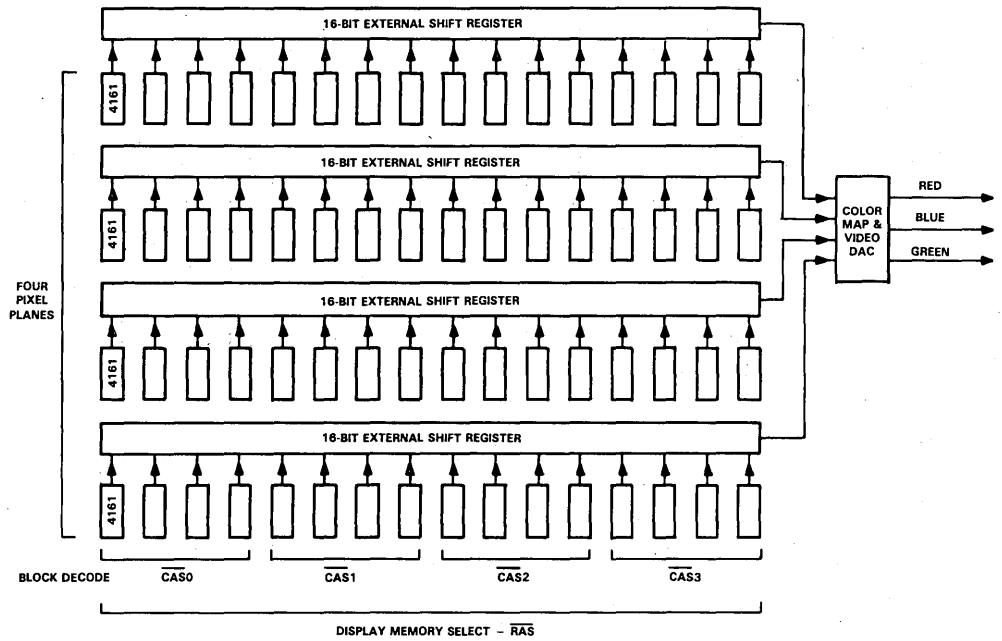


Figure 1. High Performance Display Memory Block Diagram

When a memory access is attempted by the processor, all 64 memory devices will be accessed simultaneously due to the single $\overline{RAS}$ decode signal (refer to Figure 1). The $\overline{CAS}$ signals are then used to interleave memory access so that 16-bit (four bits from four planes corresponding to four pixels) data increments coincide with individual processor memory accesses. Four $\overline{CAS}$ signals are generated from the control circuitry and correspond to the four banks of memory in Figure 1 ($\overline{CAS}$0-$\overline{CAS}$3). As a result, four consecutive memory access cycles are required to obtain all 64 data bits from all 64 TMS4161 devices. The initial processor access ($\overline{CAS}$0) will have to accommodate a wait state to realize a full DRAM access period (assuming a high-performance processor in the 125 to 150 ns cycle time range). Subsequent memory accesses ($\overline{CAS}$1-$\overline{CAS}$3), however, will approach the $\overline{CAS}$ access time of the device since $\overline{RAS}$ remains low and the minimum $\overline{RAS}$-to-$\overline{CAS}$ delay has already been satisfied. The only contention problem that may arise is between a fast $\overline{CAS}$ access of a successive access with the turnoff period (t_{OFF}) of the data from the preceding $\overline{CAS}$ access. The possibility of this contention is eliminated due to t_{CAS} (min) > 35 ns which is greater than t_{OFF} (max) < 20 ns. This system performance criteria allows the use of a graphics processor capable of a 125 to 150 ns cycle time because of the successive nature of the memory accesses. As mentioned previously, the first processor memory access will have to incorporate a wait state; however, subsequent accesses can operate at the processor cycle time. Figures 2 and 3 are the control signal schematic and control signal timing diagram for this implementation. In Figure 2, the first S175 quad D-type flip-flop enables the memory only with the first memory request from the processor. The subsequent three processor memory requests (generated from ALE) are used to latch data on the data bus as determined from the appropriate $\overline{CAS}$ bank enable. Circuitry and timings in Figures 2 and 3 show only the VRAM memory access timings for clarification purposes; the final system will have to arbitrate between memory access and memory transfer operations. Note that the actual cycle time of the memories, including $\overline{RAS}$ precharge periods, will be 640 ns (see Figure 3 where sixteen 40-ns clock cycles correspond to a complete memory cycle). The memory speed requirement corresponds to only the access time and not the cycle time since the memory banks are interleaved. A more practical implementation would allow for the number of memory access cycles to range from one to four to accommodate those

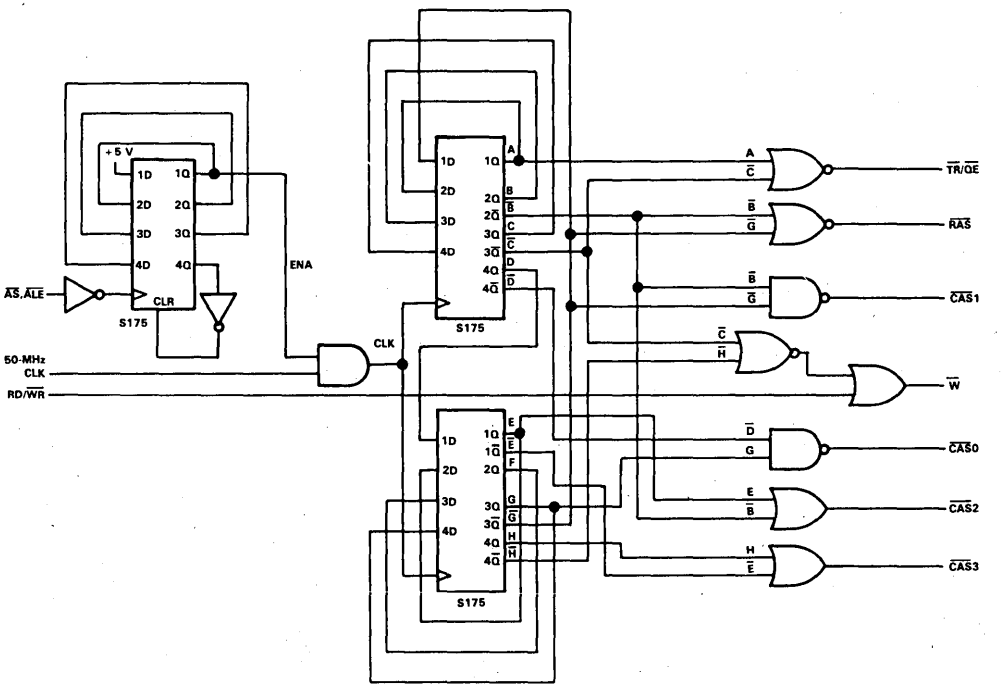


Figure 2. Control Logic Implementation of TMS4161 Banks

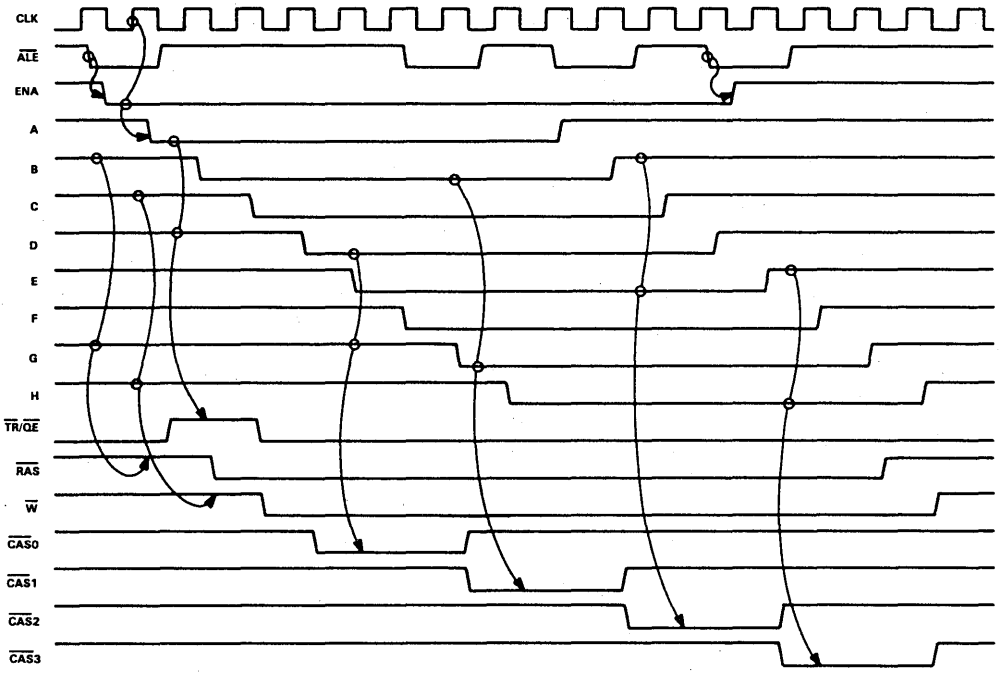


Figure 3. TMS4161 Control Timing Diagram

memory accesses which change only four pixel groups (software would be used to determine which one of four pixels to change). Peak performance will be achieved when memory is accessed in four processor memory cycle increments where average memory cycle time approaches the $\overline{CAS}$ access time. The utilization of delay lines or more optimized control signal generation could increase system performance at a greater implementation cost. Optimized control circuitry would allow timing edges to more closely align with actual memory and processor specifications to maximize performance.

The interleaved architecture offers a high performance memory access solution for those graphics system requiring:

1. The high-performance requirement of a high-resolution graphics or engineering work station (processor cycle time of 100-150 ns).
2. A high enough display resolution to require a large amount of memory. Specifically, the memory size must be large enough to establish a memory data path at least twofold the processor data bus width (i.e., 32-bit memory data path to a 16-bit processor).

High-performance microprocessor-based systems can take advantage of this scheme since the access time of the DRAM approaches that of the $\overline{CAS}$ access time instead of the total DRAM cycle time. In these applications, the TMS4161 VRAM devices can be configured to yield enhanced access performance through the random-access port while simultaneously shifting data out of the serial port.

Dual-Port Memory with High-Speed Serial Access

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SUMMARY

The demand for a friendlier user interface, versatility in displayed information, and color have made raster scanned bit-mapped graphics a viable and attractive approach to graphics. Traditionally, however, high resolution bit-mapped graphics systems have been cost prohibitive, owing greatly to the high cost of semiconductor memory and the system level cost of the support electronics needed to achieve the required video memory bandwidth. This paper describes a 64K × 1 dynamic RAM with an onchip 256-bit shift register and fast bulk data clear capability developed specifically for video applications. The RAM, designated the TMS4161 Multiport Memory, is intended to provide relief to the graphics system designer wishing to design a bit-mapped graphics system at a reasonable cost. It also provides attractive solutions for many non-video applications.

INTRODUCTION

Recently, there has been steady growth in the mid-to-high end arena of raster refreshed bit-mapped graphics displays, due largely to the growing demand for professional computers and work stations. Even the highest resolution displays found in CAD/CAM systems and flight simulators have turned to bit-mapped architectures. In bit-mapped displays, each pixel on the display can be controlled individually and independently, providing the ultimate in versatility. The growing appeal of bit-mapped systems is due largely to demand for:

- Friendly user interface
- Mixing of text and graphics on a single screen at will
- Flexibility in the types of information which can be displayed such as windowing, priority planing, and variable text fonts.

Design Challenges for Bit-Mapped Displays

These attractive features inherent with a bit-mapped display have historically been achievable only at high cost. The amount of memory needed to describe each pixel on the display usually dominates the system costs. Furthermore, the memory must not only be fast enough to deliver the pixel information to the display with no screen flicker, but the CPU must have enough access to the display memory to update it and prevent very long screen redraw times. Figure 1 shows the square law relationship between screen resolution, memory requirements and video pixel scan rate necessary to maintain a flickerless display operating at 60 Hz in non-interlaced mode. It is clear that high resolution bit-mapped

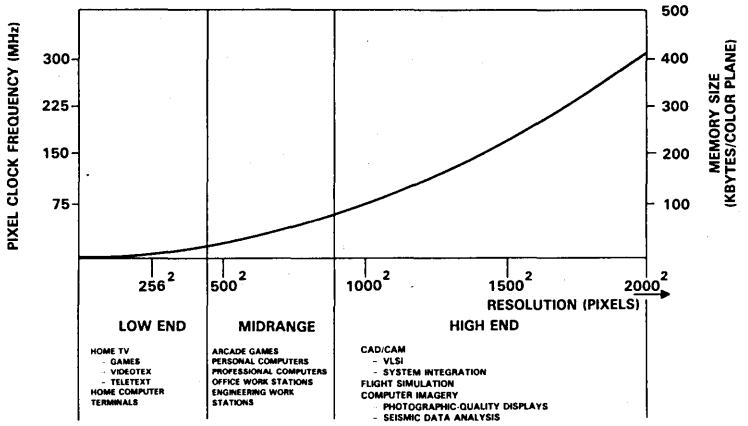


Figure 1. Video Memory Size and Bandwidth Requirements Vs. Resolution Showing Three Basic Categories.

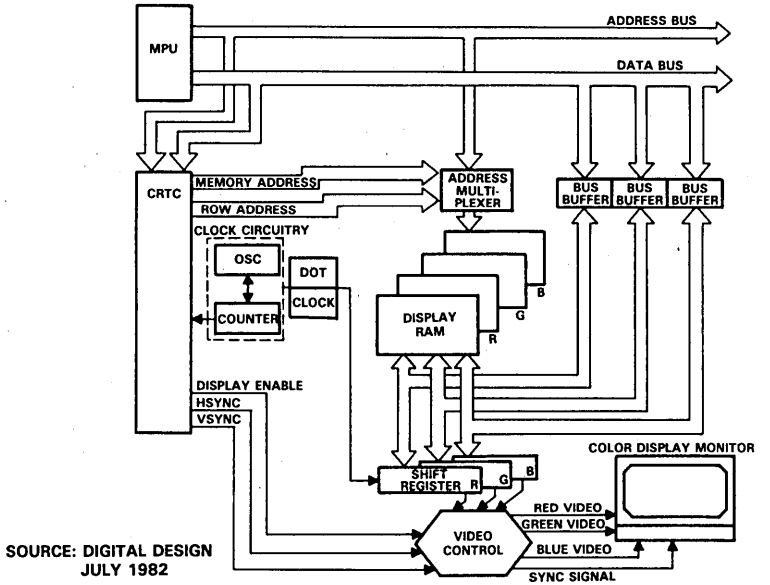


Figure 2. Typical Color Graphics System Illustrating Basic Blocks. Crucial to Such a Design are the CPU to Memory and Memory to Video Bandwidth

graphics systems are very memory intensive. In very high resolution systems (greater than 1K × 1K) incorporating color, the memory system alone, including shift registers, FIFOs multiplexers, and buffers, can represent 50% of the total graphics system cost. Previously, the high cost of the semiconductor memory chips themselves has limited the use of bit-mapped architectures. Furthermore, video memory bandwidth is often a limiting factor that the display system designer must consider. Obtaining memory chips with low cost-per-bit and high data rates has proven to be a burdensome task. Specifically, the architectures of high density dynamic RAMs have not until now been optimized for video applications.

Figure 2 illustrates a typical graphics system implementation. The key bandwidth requirements are twofold. First, the video display information contained in the bit-map memory must be transferred to the display on every vertical scan. Using available dynamic RAMs (typically 300 ns cycle time), this requires very wide (60 to 120 bit) data buses loaded in parallel into high speed TTL or ECL shift registers operating at the dot clock rate. Second, the graphics processor must be able to access the display memory often enough to keep it updated and not be locked out by the video memory controller which must keep the display refreshed.

Figure 3 shows a block diagram for a 1K × 1K black and white display system. To maintain a 60 Hz refresh rate requires a 12 ns dot clock rate assuming horizontal and vertical retrace times of 3.6 μs and 0.4 ms respectively. To achieve this data rate using conventional DRAMs with 300 ns cycle times requires a data bus of 32 bits or 32 16K × 1 dynamic RAMs, assuming that the processor is completely locked out during active scan. Typically, the processor will share access to the memory with the video controller on a fifty-fifty basis. That is, the video will have access on one cycle, the processor on the next, and so on. This doubles the necessary data bus width which means that all 64 chips necessary to hold the 1K × 1K display (64 × 16K = 1K × 1K = 1 megabit) will be brought out in parallel and loaded into a 64-bit shift register operating at the dot clock rate. In addition, arbitration logic must be included to determine whether the CPU or the video refresh has control of the display memory at any given time. Tristate buffers under the control of the arbiter connect the address and data buses to either the CPU or the video. Lastly, the wide video data bus creates a mismatch to the (typical) 16-bit data bus from the CPU, necessitating a bank decode of 16 bits from the CPU selected onto 16 of the 64 video data lines. Use of 16K × 4 dynamic RAMs which have become available recently[1] provides some relief to the chip count problem. They reduce the DRAM chip count from 64 to only 16. They do not, however, provide any improvement with respect to reducing bus widths, eliminating support circuits, or

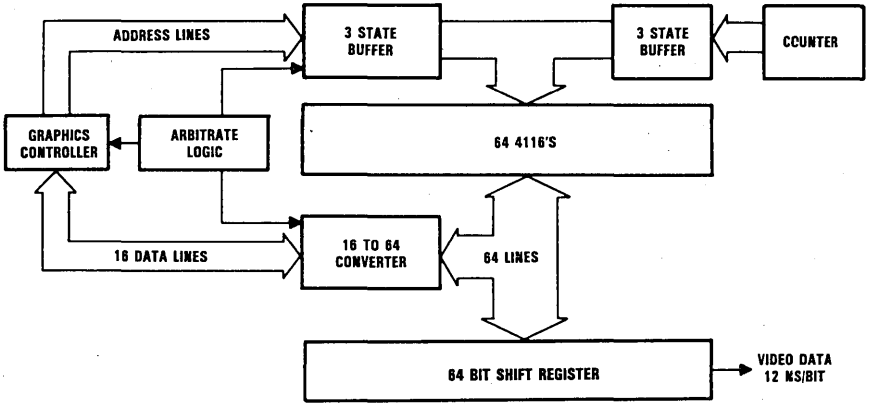


Figure 3. A 1K × 1K Black and White Graphics System Implemented with 16K × 1 Dynamic RAMs.

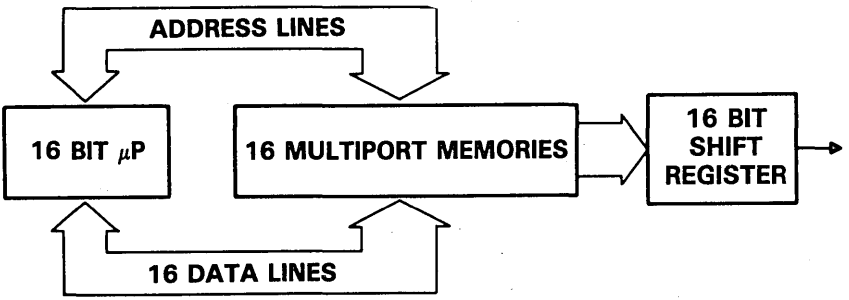


Figure 4. A 1K × 1K Black and White Graphics System Implemented with Multiport Memories.

increasing the available bandwidth between the memory and the graphics processor.

Clearly, a graphics system such as this one could be vastly improved in terms of cost and performance by: 1) decoupling the video data bus from the CPU side of the video memory, allowing simultaneous access to memory by the video and the CPU, and 2) integrating the high-speed support circuits onto the memory chips themselves.

Overview and Description of the TMS4161

The display refresh function in raster scanned bit-mapped systems is very regular. Therefore, rather than simply trying to build a faster DRAM, a new architecture concept for memory devices has been developed. The Multiport Memory interfaces a high-speed 64K DRAM to an internal 256-bit dynamic shift register. This gives the device, the TMS4161, a unique dual-port-like architecture that eliminates memory contention problems and reduces the hardware complexity of bit-mapped raster scanned displays.

To lend some perspective as to what the Multiport Memory can provide, Figure 4 illustrates the same 1K × 1K black and white graphics display system implemented using TMS4161 memory chips. The arbitration logic has been significantly reduced since the CPU has total access to the video memory during active scan. This also eliminates the need for large buffer/driver circuits. Also, since the serial ports of the memory chips can operate at speeds up to 40 ns without sharing access to the memory with the CPU, the 64-bit data bus can be reduced to 16 bits and still provide the necessary bandwidth to the video. Thus the CPU data bus width has been matched to the video bus and no bank decode is necessary. Lastly, the refresh counter can, in many applications, be eliminated or at least combined into the refresh circuits needed to refresh non-video system DRAM used to store graphics commands, display lists, etc. The TMS4161 would typically boast a reduction of 72 chips (48 memory and 24 logic) versus the system implemented with 16K × 1 DRAMs. Versus the system implemented with the 16K × 4 chips, the main chip reduction comes from the 24 logic chips.

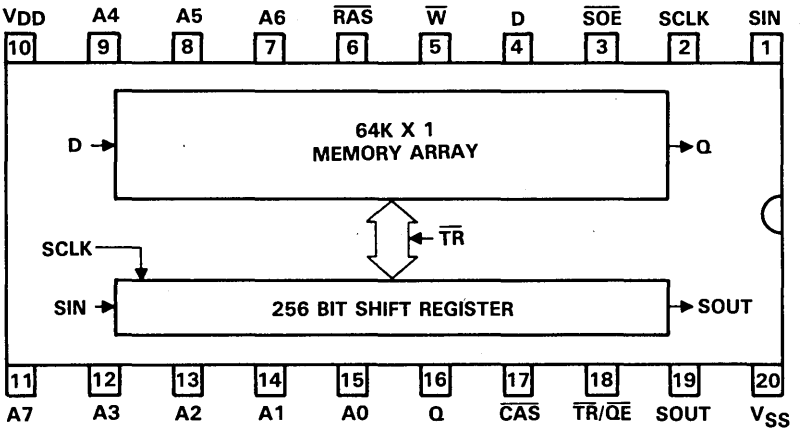
Figure 5 illustrates a block diagram of the TMS4161 showing all address, data, and control signals used for both normal DRAM (random) operation and sequential operation. The $\overline{RAS}$, $\overline{CAS}$, and R/$\overline{W}$ control signals; the 8-bit multiplexed row and column address inputs; and the random data-in (D) and data-out (Q) pins provide the same interface to the DRAM portion of the Multiport Memory as for normal 64K × 1 DRAMs. In addition, $\overline{RAS}$, $\overline{CAS}$, R/$\overline{W}$, and the address inputs provide information to the Multiport Memory during transfer operations in which 256 bits of information contained in one row of the memory array is transferred in parallel into the 256-bit shift register in one 260 ns RAS cycle time.

Five additional pin functions have been added to control the serial ports. The serial input (SIN) and serial output (SOUT) deliver data to and receive data from the on chip register respectively. The serial output enable ($\overline{SOE}$) pin is useful when multiplexing more than one video source into the same video circuitry. When $\overline{SOE}$ is low, the serial output is in a low-impedance state and data can be shifted out of the register. When $\overline{SOE}$ is high, the serial output is placed into a high-impedance state. The serial clock signal (SCLK) is the clock needed to shift data along the shift register. It is analogous to the clock input to 256 D flip-flops cascaded D to Q. The $\overline{TR}$/$\overline{QE}$ pin serves two functions. First, it controls whether or not data is to be transferred between the shift register and the memory array during $\overline{RAS}$ low. Second, it serves as an output enable of the normal random output after $\overline{CAS}$ goes low during random mode memory accesses. This makes it possible to multiplex address and data information onto the same bus.

The TMS4161 has three basic modes of operation:

1. Read from or write to the memory array via the Q and D ports.
2. Read from or write to the shift register via SOUT and SIN.
3. Transfer 256 bits of data between the shift register and the memory array.

Items 1 and 2, previously mentioned, can be performed simultaneously in the TMS4161. Since the shift register is disconnected from the memory array except when $\overline{TR}$/$\overline{QE}$ is latched low on $\overline{RAS}$ falling, the data in the register can be shifted in and out under control of the SCLK pin while normal DRAM reads and writes are taking place. The transfer of 256 bits between the register and the array can take place in either direction. That is, the memory array can be written to by transferring 256 bits into one of the memory rows or the memory array can be read from by transferring the contents of one of the memory rows into the shift register. This feature makes it possible to write a fixed row pattern to the entire memory array in just 256 cycles. This is particularly useful in double frame buffered systems in which



- DUAL PORT MEMORY – ONE PARALLEL (A LA 4164), ONE SERIAL (25 MHz)
- MODES OF OPERATION
  - READ/WRITE THE 64K X 1 ARRAY VIA THE D AND Q PORT (150 ns ACCESS)
  - READ/WRITE THE 256-BIT SHIFT REGISTER VIA SERIAL PORTS (25 MHz/40 ns BIT RATE)
  - TRANSFER 256 BITS FROM ARRAY TO SHIFT REGISTER AND VICE VERSA

Figure 5. Block Diagram of the TMS4161 Multiport Memory

the contents of one frame buffer must be cleared while the other is being displayed. This feature also allows re-ordering of the memory rows which is useful for scrolling operations.

Figure 6 shows the internal architecture of the TMS4161. The 256-bit shift register is divided into two sections. The top section contains the even numbered shift register locations and the bottom section contains the odd numbered shift register locations. The two sections are interfaced to interleaved buffer circuits at the SIN and SOUT ports to deliver the register data in the proper sequence. This has been made necessary since the shift register bit, which contains six transistors, cannot be laid out in the same area as the normal dynamic RAM storage cell which contains one transistor and one capacitor. Thus, the register bit consumes the pitch of two DRAM cells.

A key feature of the TMS4161 is its segmented register architecture. The 256-bit shift register has been optimized to provide for interlaced as well an non-interlaced displays by segmenting the register into four cascaded sections. The shift register is organized as a single 256-bit shift register that can be selectively tapped every 64 bits. A two-bit code, entered onto A6 and A7 instead of a column address during a shift register transfer cycle, is used to select the one-of-four tap points. For example, if the two bits are binary 00, the entire shift register of 256 bits can be shifted out in order. If the two bits are binary 01, then 192 bits starting at bit 64 can be shifted out in order. If the two bits are binary 10, then 128 bits starting at bit 128 can be shifted out in order. A binary 11 allows 64 bits starting at bit 192 to be shifted out. All bits are shifted out least-significant bit first, most-significant bit last with respect to the random access column address.

Consider a 1K × 1K graphics system similar to Figure 4 but using an interlaced display. In each horizontal row, 1024 pixels must be scanned. Using 16 Multiport Memory chips, this means that each chip will contain a bit of data for 64 pixels on each line. Furthermore, each time that the shift registers of the TMS4161's are loaded, the registers will contain 64 bits of information corresponding to pixels on four consecutive (adjacent) scan lines, with segment 00 being the topmost of the four scan lines and segment 11 being the bottommost of the four lines (CRT scans top to bottom). In interlaced systems, the CRT first traces out the even numbered scan lines (even field) and then the odd numbered scan lines (odd field) for every vertical scan. To start the display at scan line 0 of the even field, the register is loaded and A6 and A7 are set to 00 on the falling edge of $\overline{CAS}$, selecting the 00 tap point and the 64 bits in segment 00 are shifted out to the display. Since scan line 2 is needed next, the same row of 256 bits is reloaded into the shift register and segment (tap point) 10 is selected, skipping over the bits in segment 01 representing line 1. All other scan lines in the even field are put on the screen using the same procedure. After vertical retrace, the odd numbered lines are filled in by setting the tap point to 01 and then 11 during the register loads and shifting the data out.

Once the tap point is selected during a register load operation, that tap point will remain selected until $\overline{CAS}$ goes low during the next register load operation. Thus, for non-interlaced systems, the code 00 can be applied to A6 and

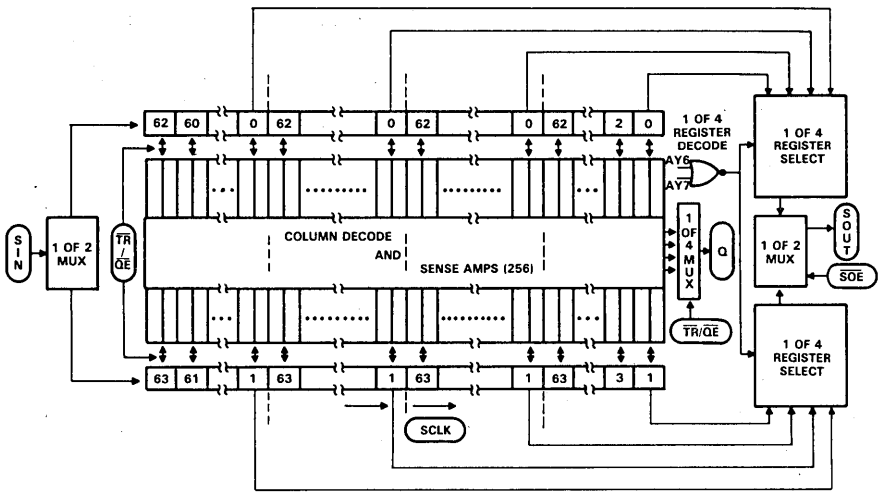


Figure 6. Block Diagram of the TMS4161 Showing Segmented Register Architecture.

A7 during the first transfer operation. Subsequently $\overline{CAS}$ can remain high during all future transfer operations and the 00 tap point will remain selected. The tap-point code is stored in static latches and will remain valid as long as power is supplied to the chip.

Figure 7 shows a timing diagram for a memory-to-register load operation followed by simultaneous and asynchronous operation of a random mode write cycle (e.g., CPU writing to video memory) and serial shift out of the register (to the video circuitry). The first bit out of the shift register is triggered off the rising edge of $\overline{RAS}$. All subsequent 255 bits are propagated through the register off the rising edge of SCLK. To simplify designs in which non-video DRAM is contained in the same address space as the video DRAM, the TMS4161 Multiport Memory has been designed to be spec compatible with industry standard 64K × 1 dynamic RAMs.

Graphics Applications of the TMS4161

Figure 8 shows a basic block diagram of a 1K × 1K black and white graphics system similar to that described in Figure 4. The 16-bit CPU operates on 16 pixels at once and the pixels have a regular one-to-one correspondence with the physical memory locations. The 16-bit data bus feeds directly into the D and Q ports of the Multiport Memories. The serial output ports of the 16 memory chips feed in parallel to an external 16-bit shift register which operates at the 12 ns dot clock rate determined earlier. The TMS4161 internal shift registers need only operate at one-sixteenth of the frequency of the video dot rate, or 192 ns, well within their minimum clock period of 40 ns.

The design simplicity inherent with the TMS4161 is illustrated in Figure 9, which shows the same 16 Multiport Memory chips configured into a 512 × 512 pixel display system with four bits per pixel giving 16 possible colors. The memory is organized into four color planes, each 512 × 512. Four memory chips are used for each color plane. Here the wiring of the CPU data bus onto the memory D and Q ports is slightly different. In this application the pixel information is read across the four color planes. That is, the CPU operates on four pixels at once and the computer word contains all four bits of information describing each of the four pixels as shown. The external 16-bit shift register is divided into four 4-bit registers each of which will supply one bit of information (corresponding to a single pixel) to a color look-up table on each dot clock cycle. It is interesting

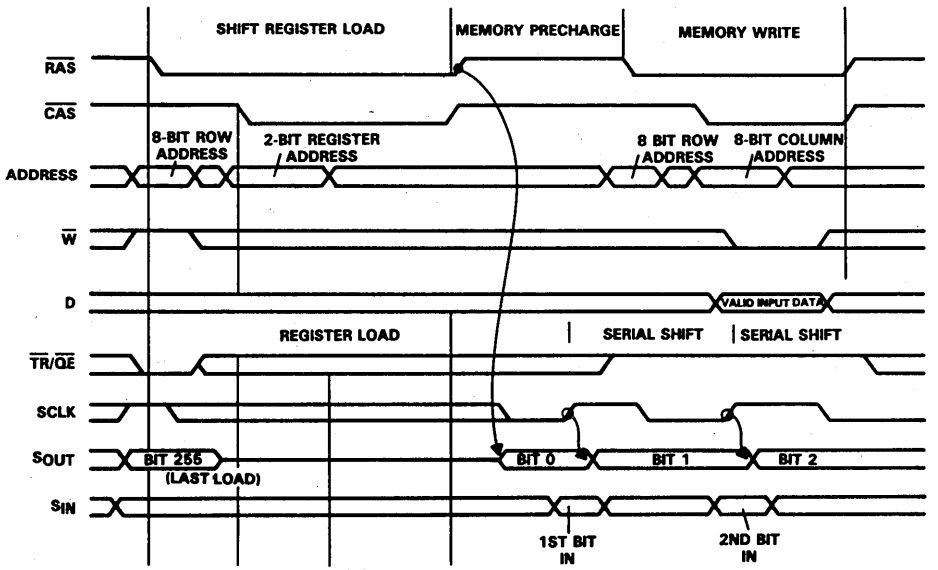


Figure 7. Timing Diagram of TMS4161 Register Load Followed by Simultaneous Serial and Random Mode Access.

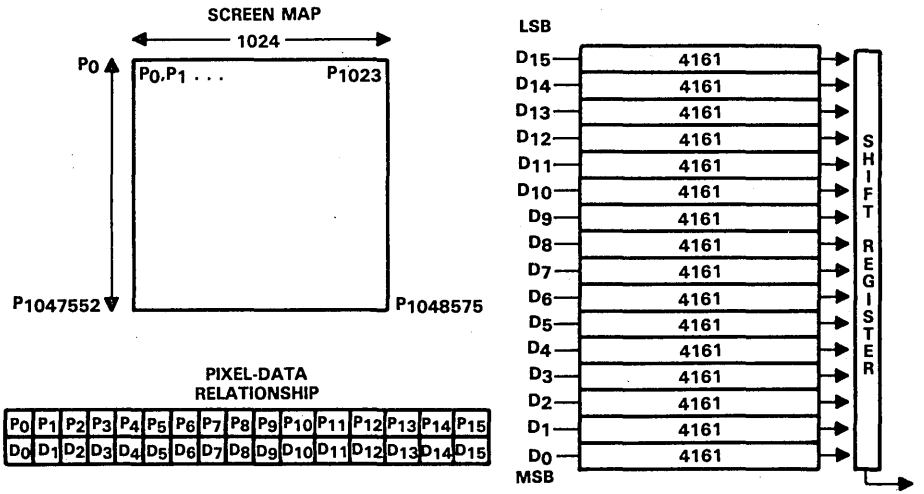


Figure 8. Memory Configuration of a 1K × 1K Black and White Graphics Showing Pixel-Data Relationship and Data Bus Configuration.

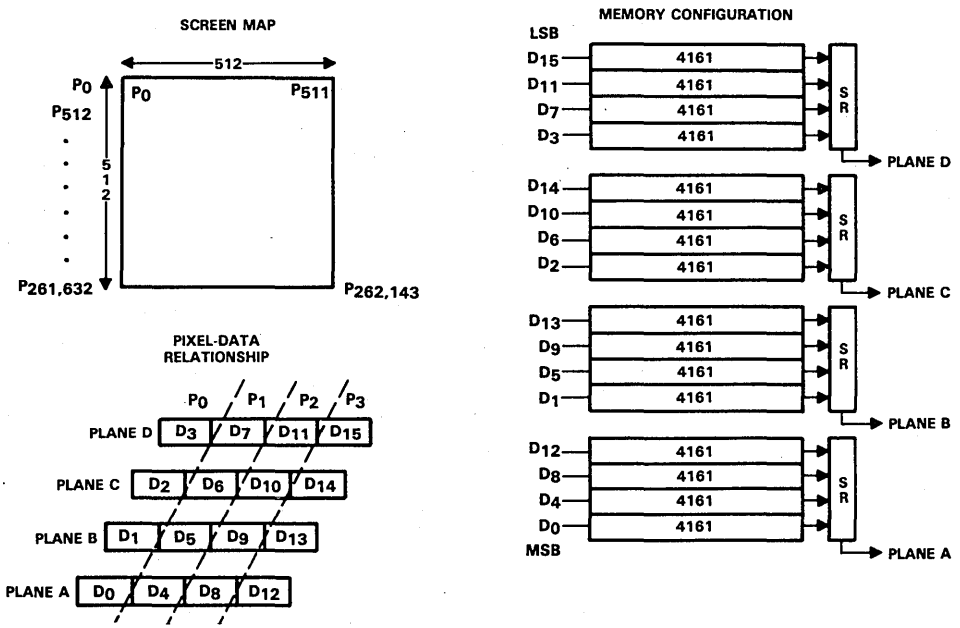


Figure 9. Memory Configuration of a 512 × 512 Graphics Featuring Four Bits Per Pixel. The Memory Timing of the TMS4161 Serial Ports is the same as the Black and White System in Figure 8.

to note that even though the internal shift registers of the TMS4161's must now operate at one-fourth the frequency of the external registers rather than one-sixteenth the frequency as in the previous case, there are only one-fourth as many pixels to display so the shift rate of the Multiport Memory shift registers remains 192 ns, exactly like the previous case. In fact, regardless of screen resolution and number of color planes, the shift rate required of the TMS4161 shift registers remains relatively constant. This points to a key plus in utilizing the TMS4161: design flexibility.

Non-Video Applications of the TMS4161

The serial input port of the TMS4161 significantly enhances the chip's usefulness in both video and non-video applications. For example, it can be used to load in a video data stream in an image processor application such as charge coupled device (CCD) imagers. Non-video applications which could benefit from such a device include main memory in high-speed memory systems whereby the dual-access nature of the device facilitates disc to main memory and main memory to cache memory bulk data transfers. Tag-bit processing is greatly simplified with a substantial increase in performance. The tag bits of a data word in a computer system are read from TMS4161 memory chips and thus can be quickly set and cleared sequentially as well as be completely cleared using the fast clear feature described earlier. This can be useful in virtual memory systems when keeping track of available physical memory space. Network communications is also an attractive application area for the TMS4161. Whether collision detection or token ring based, 10 MHz serial data transmissions can be handled easily using the serial ports of the TMS4161 while its memory array is being accessed.

CONCLUSION

The decreasing cost-per-bit of dynamic RAM coupled with an advanced memory architecture will provide both a cost reduction and a performance enhancement to todays' bit-mapped graphics systems. By providing asynchronous random and serial ports and integrating the necessary support electronics, the TMS4161 promises to provide unprecedented design simplicity in todays systems. The TMS4161 is also well suited for a variety of non-video applications, providing performance enhancements and design simplicity here as well.

REFERENCES

1. Peyton M. Cole, David W. Gulley, and Lionel White, "Wide-Word Memory Chips Spur New μP Applications", Electronic Design, Hayden: 1981.

This paper was initially presented at WESCON '83 and is reprinted with their permission.

Topological Structure of the TMS4161 Multiport Video RAM

In many applications, there will be a need to analyze the architecture of the TMS4161 Multiport Video RAM to confirm proper operation. The purpose of this application report is to define the internal architecture and function of the TMS4161 as they relate to its operation. In this manner, the memory array and shift register of the TMS4161 can be tested properly to guarantee device adherence to application requirements.

INTERNAL ADDRESS WEIGHTINGS

Sixteen address bits are needed to decode one of 65,536 memory locations in the memory array. The multiplexed addressing scheme provides for $\overline{RAS}$ (Row Address Strobe) to latch 8 row addresses, and $\overline{CAS}$ (Column Address Strobe) to latch 8 column addresses. A 256-bit shift register is integrated onto the TMS4161 to add an additional port for data access in a serial mode. The external pin address names correspond directly to the internal address weights of the memory array (i.e., RA7 has addressing weight of 2^7) as indicated by Table I.

Table I. Internal Address Weightings

Desired Row or Column Address	Weight	TMS4161	
		Pin Name	Pin Number
(MSB) RA7,CA7	2^7	A7	11
RA6,CA6	2^6	A6	7
RA5,CA5	2^5	A5	8
RA4,CA4	2^4	A4	9
RA3,CA3	2^3	A3	12
RA2,CA2	2^2	A2	13
RA1,CA1	2^1	A1	14
(LSB) RA0,CA0	2^0	A0	15

ARRAY TOPOLOGY

The same memory array layout is utilized with the TMS4161 as with the 64K × 1, TMS4164 DRAM (See Application Note MM4164A9 for further information concerning the TMS4164 topology). Translation from the pinout of the TMS4161 to the memory array topology is represented by Figures 1(a) through 1(d). The algorithms for determining near and nearest neighbors to a monitored memory cell are summarized in Tables II and III with (R,C) representing the cell location where R = row address and C = column address.

Table II. Near and Nearest Neighbors if Row and Column Addresses are Either Both Even or Both Odd

Row Address	Nearest Neighbors	Near Neighbors
≤7F	R−2, C+1	R−2, C+0
	R+0, C+1	R+2, C+0
		R−1, C+2
≥80	R−2, C−1	R−2, C+0
	R+0, C−1	R+2, C+0
		R−1, C−2

Table III. Near and Nearest Neighbors if Row and Column Addresses are Neither Both Even or Both Odd

Row Address	Nearest Neighbors	Near Neighbors
≤7F	R+0, C−1	R−2, C+0
	R+2, C−1	R+2, C+0
		R+1, C−2
≥80	R+0, C+1	R−2, C+0
	R+2, C+1	R+2, C+0
		R+1, C+2

INTERNAL DATA INVERSION

Note that the algorithm changes for each half of the array due to the fact that the top half is laid out as the mirror image of the bottom half. Data in the top half of the array is stored in inverted form while data in the lower half is stored in true form. This internal data inversion is transparent to the user; however, for generation of specific patterns, this data inversion must be taken into account. Row address bit seven selects between the upper and lower memory arrays, thus the circuit shown in Figure 2 may be used to compensate for this internal data inversion. This allows data written in and read out to be the same polarity as the data stored in the addressed memory cell.

MEMORY ARRAY ACCESS

During an access cycle, 256 column locations are enabled by $\overline{RAS}$ (corresponding to the selected row). Four of these 256 column locations are then decoded from CA0-CA5 after the addresses are latched by $\overline{CAS}$. The four column locations are then decoded by the least significant column address bits (CA0 and CA1) selecting a single bit to be read

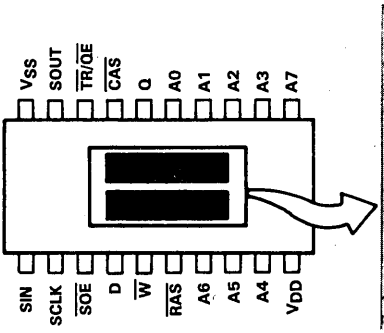


Figure 1a. TMS4161 Pinout

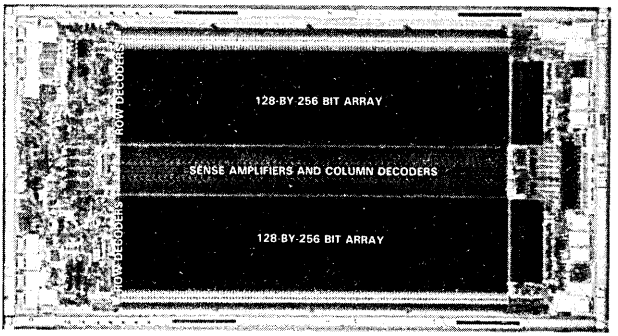


Figure 1b. Array Organization

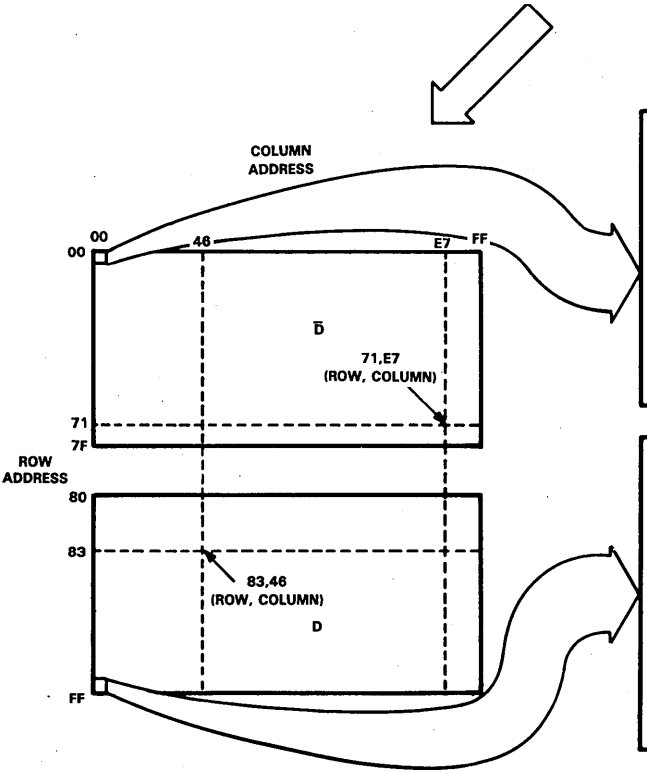


Figure 1c. TMS4161 Array Bit Map

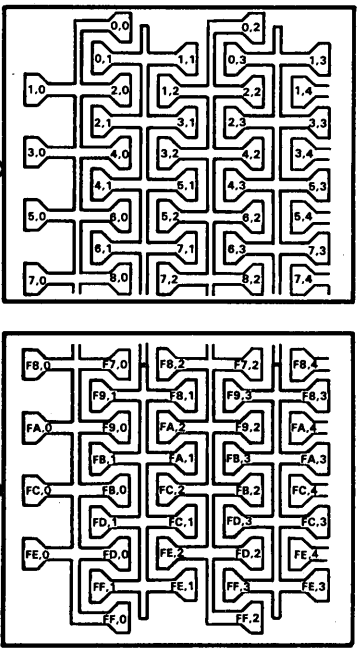


Figure 1d. Upper and Lower Array Cell Topology

Figure 1(a) shows the chip pinout, Figure 1(b) is a closeup of the array, Figure 1(c) shows the bit map for the rows and columns, and Figure 1(d) is a closeup of the cell topology in the array.

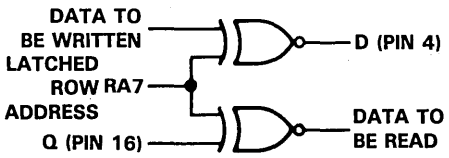


Figure 2. Circuit for Compensation of Internal Data Inversion

or written through the one-of-four data input/output selector (see Figure 3). As a result, the four internally accessed memory locations are obtained from four adjacent columns of a single accessed row. An algorithm can be developed which will calculate the other three accessed memory locations based on the position of the intended memory location in the array. This algorithm is shown in Table IV assuming the memory location (R,C) as the base location.

Table IV. Algorithm for Determination of Additional Accessed Memory Locations

Column Address		Additional Accessed Memory Locations		
CA7	CA6			
0	0	R+0, C+1	R+0, C+2	R+0, C+3
0	1	R+0, C−1	R+0, C+1	R+0, C+2
1	0	R+0, C−2	R+0, C−1	R+0, C+1
1	1	R+0, C−3	R+0, C−2	R+0, C−1

The algorithms can be useful in verifying that the one-of-four data input/output select function is operating correctly on the device.

SHIFT REGISTER FUNCTION

The significant difference between the TMS4164, 64K × 1 DRAM, and the TMS4161, Multiport Video RAM, is the addition of the 256-bit shift register on the TMS4161. Important tests to evaluate are the transfer of data from a

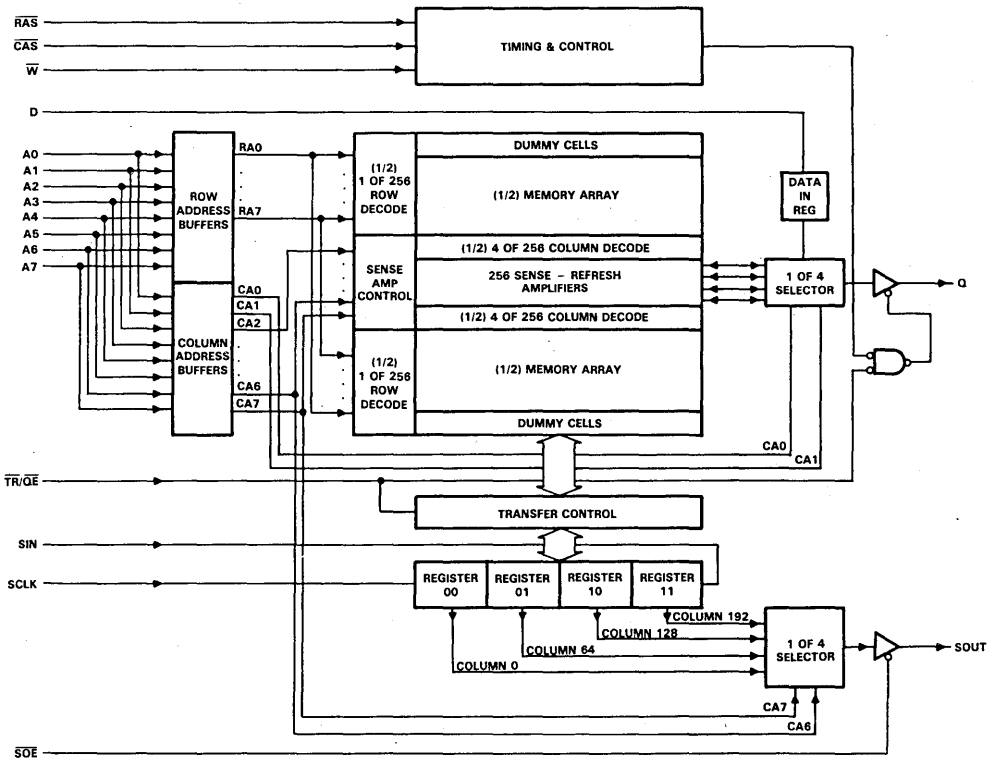


Figure 3. TMS4161 Functional Block Diagram

memory row to the shift register and from the shift register to a memory row. These transfers are easily verified since the column address of an individual data bit in the memory row to be transferred corresponds to the same position number of the shift register. For example, the data stored in column address 127 of the row being transferred will be written to position 127 of the shift register. As a result, the data obtained from the serial stream of the shift register will correspond, one for one, to the row of memory that was transferred. In a similar fashion, serial data can be input to the shift register position 255 by the SIN input. Subsequent shift clocks to the shift register will move the data from the most significant shift register bit to the least significant bit. When fully shifted (256 clocks), the data in the shift register can be transferred to the array and will correspond to that row of memory as if that row had been sequentially written in random access mode. For additional information concerning the testing of the TMS4161, refer to the "Testing Philosophy for the TMS4161" Application Report.

SHIFT REGISTER ARCHITECTURE

Figure 3 is a functional block diagram of the TMS4161, Multiport Video RAM (VRAM), and Figure 4 is a block diagram of the shift register and control circuitry of the VRAM. The shift register is actually subdivided into two sections; the sections correspond to the odd and even column loctions, respectively, of the memory row to be transferred. As shown in Figure 4, the even shift register is physically located adjacent to the top half of the array, while the odd shift register is adjacent to the bottom half of the array. The two shift register sections are interleaved to yield the sequential output of the memory row; the interleaving is done synchronously with the register shift clock and automatically selects the even shift register bit for the initial output of the shift register. This is accomplished transparent to the external device operation. For those operations where the shift register is to be loaded serially from the SIN input, a dummy transfer must first be made for initialization purposes (either to or from the shift register). This serves to properly

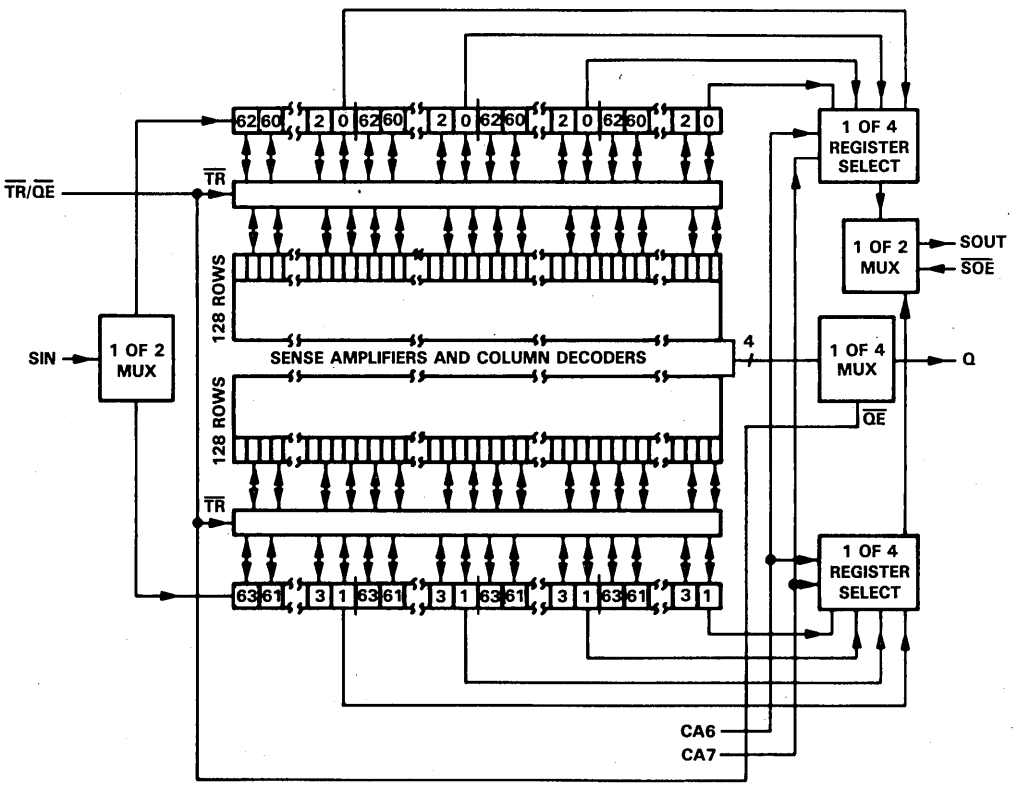


Figure 4. TMS4161 Shift Register and Control Block Diagram

set up the serial input sequence from the input multiplexer so that the even bit shift register will be loaded first. Subsequent serial input (from SIN) will switch between the two shift registers to achieve the proper input sequence.

SHIFT REGISTER TAP POINTS

The shift register is divided into four cascaded 64-bit shift registers segments based on the select function which is decoded by the two most significant column address bits. Tap points are set up along the 256-bit shift register at 64-bit increments. This allows the shift register to be tapped at less than 256 bits for those applications that may demand register addressability down to 64 bits. Table V illustrates the column addresses needed to select the desired tap point in the shift register.

Table V. Shift Register Tap Points

Column Address		Shift Register	Total Available	Corresponding Column
CA7	CA6	Position	S.R. Bits	Location
0	0	0	256	C0-C255
0	1	64	192	C64-C255
1	0	128	128	C128-C255
1	1	192	64	C192-C255

These tap points for the shift register are applicable only to the output of the shift register (SOUT); data into the shift register (SIN) is always shifted into position 255 (column bit 255) and shifts toward position 0 (column bit 0).

SUMMARY

With multiprocessor and dual-ported applications becoming very commonplace, the added features of the TMS4161 Multiport Video RAM make it an excellent choice to eliminate the bottlenecks that have previously occurred in accessing system memory. To ensure proper system performance of the TMS4161, the previous discussion has described the topological structure of the device and how it corresponds with device functionality. As a result, test algorithms can be configured which will comprehend a worst case system condition and ensure proper device operation. Texas Instruments is committed to the production of only the most reliable components, and will continue to supply the engineer with the necessary tools and support so that the components that are used will conform to his or her system and design requirements.

An Introduction to the TMS4256 and TMS4257

MOS Memory
Applications Engineering

INTRODUCTION

As applications utilizing dynamic RAM's have increased, the need for a flexible DRAM has also increased. The TMS4256 and TMS4257 expand this flexibility with the advent of the latest generation, 256K dynamic RAM devices. The TMS4256 is the page-mode version while the TMS4257 is the nibble-mode version of the 256K × 1 dynamic RAM's offered by Texas Instruments. The purpose of this application report is to guide the prospective DRAM user in the operation of the TMS4256 and TMS4257 to take full advantage of the device potential. Many of the same design and production techniques from the 64K DRAM generation are utilized with the 256K generation; however, there are important differences.

ARCHITECTURE

A primary consideration in the design and development of the 256K architecture was to retain the same refresh scheme as the previous 64K generation. Refresh for the 256K DRAM is accomplished by supplying 256 refresh cycles in a 4 ms-period. The memory array can be visualized as a matrix of 256 rows by 1024 columns which has been split into two arrays of 256 rows by 512 columns for the upper and lower halves of memory – the two halves actually mirror each other. A single refresh cycle causes a row in both upper and lower arrays to be refreshed. When a memory read or write is performed on the memory array, there are actually four memory locations that will be enabled. External to the memory array is a one-of-four selection function where one out of the four memory locations enabled from the memory array will be selected by decoding row address bit 8 and column address bit 8. As a result, a single data bit is placed at the Q output during a memory read, or a single memory location is enabled for writing the data bit D during a memory write. This architecture lends itself very easily to either nibble mode or ×4 arrangements.

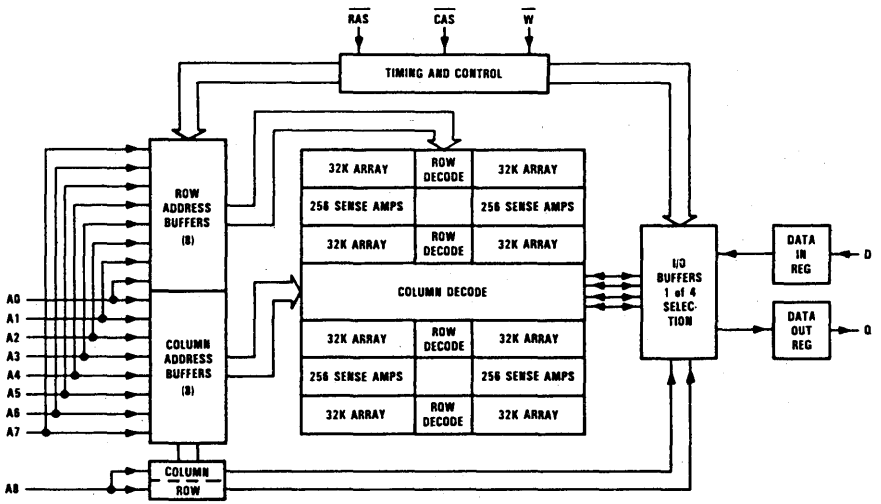


Figure 1. TMS4256/TMS4257 Functional Block Diagram

DEVICE ENHANCEMENTS

Several product improvements have been integrated into the TMS4256 and TMS4257 to enhance both performance of the device and user flexibility.

SUBSTRATE PUMPS

Internally, substrate pumps have been designed to minimize the effect of control signal undershoot. Compensation circuitry is utilized to minimize fluctuations in the substrate voltage. From the device point of view, the overall result of the substrate pump is the reduction of the charge injection of minority carriers into memory cell storage capacitors and periphery circuitry. From the system point of view, it provides the designer extra margin in minimizing the effects of excessive undershoot in the system and improving the overall performance of the system.

FOLDED METAL BIT LINES

Two important changes were implemented with the 256K device bit lines which improve both device noise immunity and performance. Aluminum (metal) bit lines are utilized in the TMS4256 and TMS4257 where diffused bit lines were used in previous generation devices. The capacitive loading of a metal bit line is significantly less than for a diffused bit line. The folded bit line approach makes use of excellent common mode noise rejection to minimize the effects of noise on the sensing margins. Approximately the same noise levels will be experienced by two bit lines that are input to the differential sense amplifier because they are physically close and parallel to one another. Since a differential sensing scheme is used, any common noise has little effect on the sense amplifier.

POLYCIDE WORDS LINES

The TMS4256 and TMS4257 utilize polycide film for the word lines for enhanced device speed. Polycide is a polysilicon material which has been sputtered with a metal for the purpose of signal propagation enhancement. The relative resistance of the polycide material is a factor of ten less than that of polysilicon. As a result, reduced signal delay is achieved through the word lines without the complexity and cost of a double-metal process (metal bit line and metal word line). Architectural analysis for the 256K revealed a higher performance device would be achieved with the utilization of metal bit lines instead of metal word lines. The use of polycide word lines with its metal-like properties, became the obvious approach to achieve the fast access times necessary to accommodate required system performance.

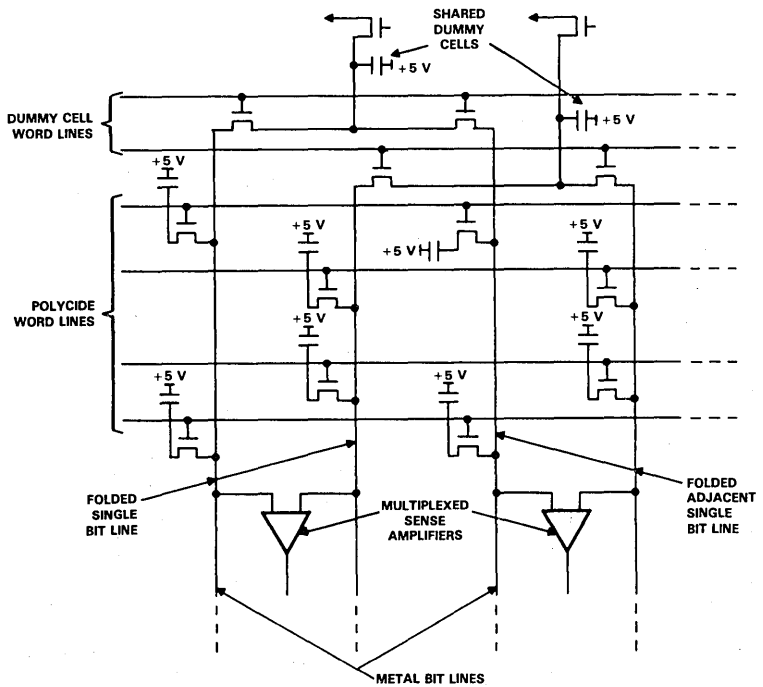


Figure 2. Folded Bit Line and Shared Dummy Cell Concept

SHARED FULL-SIZE DUMMY CELLS

A dummy cell is used as one input to the differential sense amplifier with the accessed memory cell being the other input. Typically, the charge from the dummy cell will create a differential voltage across the sense amplifier to distinguish between logic "1" and logic "0" of the memory cell. With the use of dummy cells that were only half the normal memory cell size (previous generation DRAM's), slight process deviations or marginalities would cause a larger performance degradation on the dummy cell than the memory cells (the net area reduction due to process variation depends directly on the perimeter of the cell). Figure 3 shows the relative effect of a 0.25 micron process deviation on both a full and half size cell. The TMS4256 and TMS4257 employ a full size dummy cell which is shared by the two columns enabled during a normal memory access cycle (see Figure 2). Recall that two rows and two columns are actually enabled in the memory array when memory read or write cycles are implemented. The overall charge distribution with respect to each bit line will be the same as with the half size dummy cell; however, process deviation effects on sense amplifier performance will be minimized. The relative voltage differential between a dummy and memory cell will remain the same despite minor process deviations.

REDUNDANCY

Redundancy is the technique of replacing initially defective memory locations with spare rows or columns. Redundancy has been implemented by adding two additional rows for each 64K section of the 256K DRAM (8 total), and four total additional columns. When defective memory locations are encountered on a chip during probe, one of the additional rows or columns will be physically enabled to replace the defective memory location(s) – this is accomplished by laser repair technology. This will be totally transparent to the device user, thus he will not notice a change in either performance or reliability of the part. Use of redundancy for the 256K generation enhances probe yield, especially in the early production life; this translates to lower device cost to the DRAM user.

MULITPLEXED SENSE AMPLIFIERS

An important parameter to examine in judging a dynamic RAM's sensing capability is the capacitance ratio of the bit lines to the memory cell. Ideally, the full storage voltage of a memory cell should appear on the sense amplifier input; however, this is not practical since the input to the sense amplifier is composed of a capacitive network. The objective then is to minimize the ratio of the bit line capacitance to the memory cell capacitance in order to minimize the voltage loss and time delay of a signal enroute from a memory cell to the sense amplifier input. The multiplexed scheme allows the sense amplifier to be placed in the middle of the bit line instead of at either end, allowing selection to occur in only half of the bit line as determined by row address bit 7. Only the half of the bit line selected at any given time will contribute to the capacitive loading on the selected cell. Consequently, the voltage loss and time delay of a memory cell signal will be half as much with the multiplexed sense amplifier architecture. The bit line to memory cell capacitance ratio for 256K generation devices is approximately 8:1.

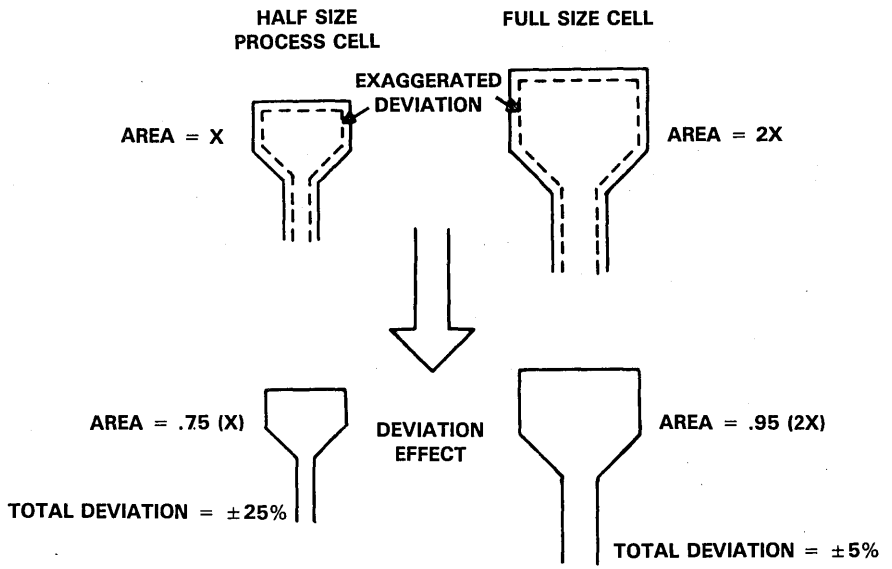


Figure 3. Process Deviation Effects on Dummy Cells

SHARED COLUMN DECODERS

In order to conserve silicon real estate, multiplexed column decoders are utilized with the 256K devices. Figure 1 shows how the column decoders are located down the middle of the device. Each column decoder corresponds to two sense amplifiers in both the upper and lower half of the memory array, which necessitates only 256 column decoders. Eight column addresses are needed to decode one of 256 column decoders. Each decoder selects four data bits from four columns to be sent to the periphery where row and column bit 8 is used to select one of the four bits. The resultant four columns are decoded outside of the memory array (see paragraph on Architecture).

CONTROL SIGNALS USED

In order to take advantage of the relative functional and space saving attributes of dynamic RAM's, necessary control signal implementation must be considered. These control signals follow along the line of standard DRAM control signal implementation.

ADDRESSES (A0-A8), $\overline{RAS}$, $\overline{CAS}$

Eighteen address bits are necessary to decode one of 262,144 different memory locations. Since minimizing the pin count on a dynamic RAM is essential, the eighteen address lines are multiplexed. The architecture of the TMS4256 and TMS4257 can be visualized externally as a 512 row × 512 column memory cell matrix. Operating together with the row and column addresses will be the row address strobe ($\overline{RAS}$) and column address strobe ($\overline{CAS}$) signals, respectively. Initially, $\overline{RAS}$ will select one of 512 rows from the nine row addresses presented at the DRAM address inputs. A multiplex (MUX) signal must be generated within the system in addition to $\overline{RAS}$ and $\overline{CAS}$ in order to cause multiplexing circuitry to switch from row to column addresses at the DRAM address inputs. A typical system will employ a shift register or delay line in generating $\overline{RAS}$, MUX, and $\overline{CAS}$ which will be synchronized by a system clock. It is important that generation of these control signals be synchronized with the host system to optimize the memory performance within the system.

WRITE ENABLE ($\overline{W}$)

A read or write function is determined by a high or low state, respectively, of the write enable signal ($\overline{W}$). $\overline{W}$ will be generated by the host controller directly or through some decoding circuitry to the DRAM memory. The way in which it will appear at the DRAM $\overline{W}$ input will depend on the type of memory cycle to be utilized with the dynamic memory. It is necessary that the generation of $\overline{W}$ be coordinated with other control signal generation to accommodate the TMS4256 and TMS4257 memory cycle specifications.

Various combinations of these basic operational signals give the TMS4256 and TMS4257 the flexibility to adapt to different modes of operation.

AVAILABLE MEMORY CYCLE TYPES

READ CYCLE (REFERENCE FIGURE 4)

A read cycle will be utilized at a point in a host controller instruction sequence where external memory is required. The condition which dictates a read cycle is to have $\overline{W}$ high for a specified setup time before the falling edge of $\overline{CAS}$ (t_{RCS}). Valid data will be available at the DRAM Q output after a specified maximum period of time following $\overline{CAS}$ low (t_{CAC}) and $\overline{RAS}$ low (t_{RAC}). $\overline{W}$ must be kept high until after both $\overline{CAS}$ and $\overline{RAS}$ return to high states. Data at output Q will remain valid for a maximum period of t_{OFF} following the rising edge of $\overline{CAS}$ before Q will go into a high-impedance condition.

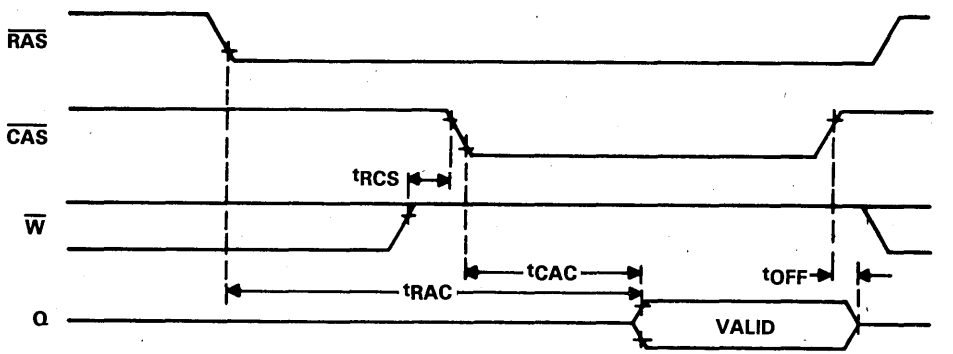


Figure 4. Read Cycle Timing

EARLY WRITE CYCLE (REFERENCE FIGURE 5)

Early write describes a write cycle where $\overline{W}$ is taken low a minimum time period (t_{WCS}) before $\overline{CAS}$ goes low. Valid data must be available before the falling edge of $\overline{CAS}$ (t_{DS}), and is latched by $\overline{CAS}$ at the D input. An important attribute of an early write cycle is that a high-impedance Q output is guaranteed. This will allow the user to connect both D and Q together without the utilization of three-state buffers for output control. A possible complication may arise in using a controller with a multiplexed address/data bus. Valid data will not be present on the address and data bus for a specified delay period following address latching; so $\overline{CAS}$ going low will be forced to wait for valid data before latching it. The $\overline{CAS}$ low period will still have to be satisfied which may cause the early write cycle to be longer than the corresponding implementation of a write cycle.

WRITE CYCLE (REFERENCE FIGURE 6)

A write cycle will be instituted at a point in the instruction sequence of a host controller when data is to be stored in external memory (DRAM in this case). Invalid data will be present on the DRAM Q output since the pre-condition of output three-state (t_{WCS} in the early write cycle) was not met. However, the Q output will not be utilized during a write cycle so valid data is not necessary at Q. A problem arises with the implementation of a bidirectional data bus where contention will occur between invalid data present at Q and valid data available at D. If bidirectional data lines are required, an external set of three-state buffers will be necessary to prohibit bus contention between input and output lines of the DRAM during a write cycle. A standard write cycle will have $\overline{W}$ going low following $\overline{CAS}$ – the data must be valid before $\overline{W}$ goes low. In addition, the minimum specified $\overline{CAS}$ low to $\overline{W}$ high hold time (t_{WCH}) is important in order to guarantee sufficient time to write data to the addressed memory location. Closely related to this are the requirements for minimum $\overline{W}$ low to $\overline{RAS}$ high (t_{RWL}) and $\overline{W}$ low to $\overline{CAS}$ high (t_{CWL}). A write cycle will typically be used with a system with multiplexed address and data lines where data does not become valid for some delay period following address latching. Also, the system may require $\overline{CAS}$ to go low as soon as possible in order to comprehend the minimum

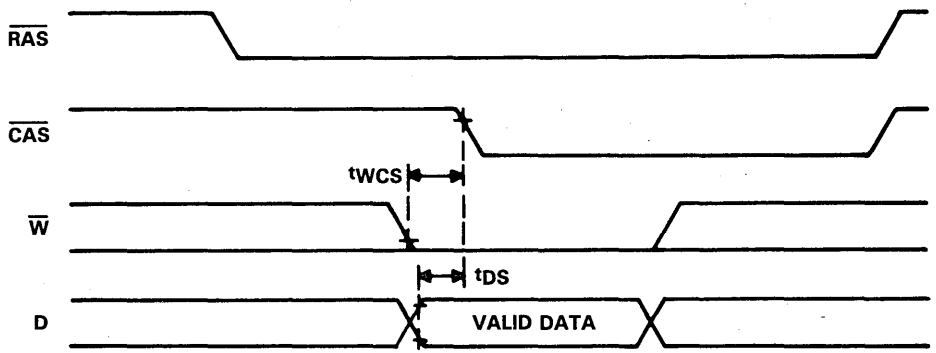


Figure 5. Early Write Cycle Timing

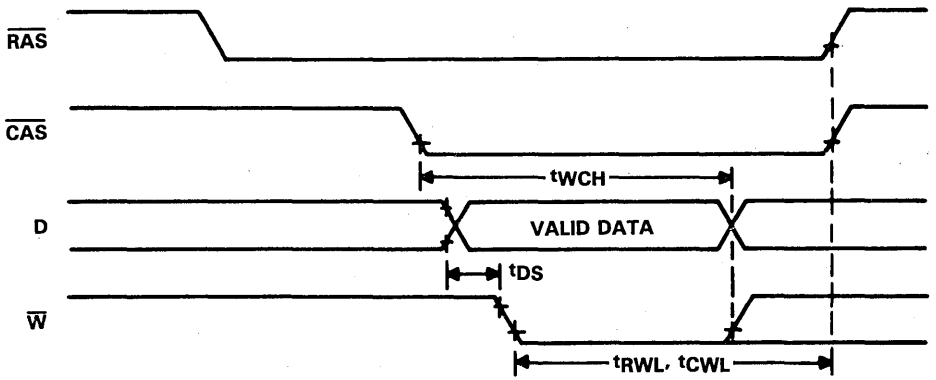


Figure 6. Write Cycle Timing

specified $\overline{CAS}$ low time – data may not be set up by this point which will prohibit an early write cycle.

READ-MODIFY-WRITE CYCLE (REFERENCE FIGURE 7)

For those applications which require a specific memory location to be read and written to in the same memory cycle, a read-modify-write cycle will be the most efficient cycle. $\overline{W}$ must be high a specified setup time before the falling edge of $\overline{CAS}$ to ensure that the memory location will be read. Recall that this is the same procedure as with a standard read cycle; so valid data will appear at the output Q a maximum t_{CAC} time from the falling edge of $\overline{CAS}$. A read-modify-write cycle can be instituted by bringing $\overline{W}$ low after a minimum time from the falling edge of $\overline{CAS}$ (t_{CWD}). This minimum time will guarantee sufficient time for the data located at the accessed memory location to be enabled and sensed during the read part of the cycle. The low edge of $\overline{W}$ will latch valid input data on the data bus to the D input of the DRAM. Subsequently, satisfying minimum periods for t_{CWL} and t_{RWL} will ensure that valid data at the D input will properly be written to the specified memory location. If a bidirectional data bus is to be utilized, three-state buffers will be necessary to ensure no contention on the data bus between input and output data of the DRAM. Any type of application where memory must be read and manipulated quickly may utilize read-modify-write cycles.

PAGE MODE (REFERENCE FIGURE 8)

Page mode is an optional mode, designated by TMS4256, which allows the user to generate numerous memory accesses with only a single $\overline{RAS}$ low edge. It is important to note that these accesses will occur only along the same row and will require subsequent $\overline{CAS}$ pulses to coincide with new column addresses. After a particular row is latched by the $\overline{RAS}$ low signal, $\overline{CAS}$ will latch individual memory locations as it accesses various column locations within the latched row. It is necessary to provide a different column address for every memory location that is desired. In this manner, page mode can be utilized in an accelerated access of nonsuccessive memory locations if the application demands it. The $\overline{RAS}$ low maximum specification (10.0 μs) is the limiting factor here and will allow approximately 64 read or write cycles, or 42 read-modify-write cycles before $\overline{RAS}$ must be taken high to satisfy DRAM precharge requirements (– 150 ns devices). Page mode memory access

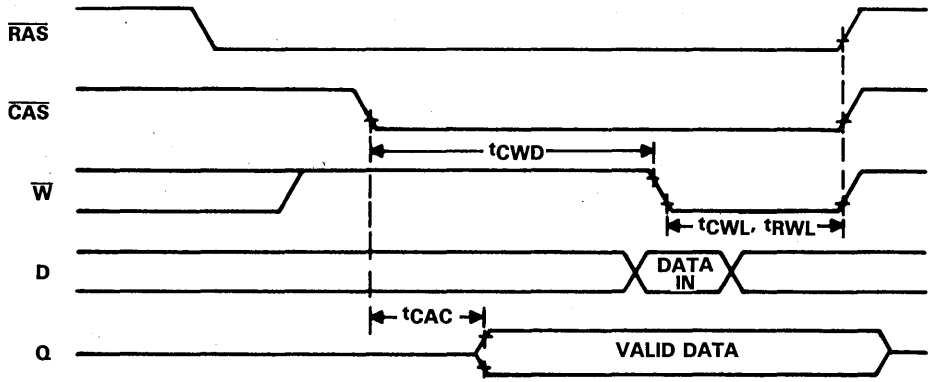


Figure 7. Read-Modify-Write Cycle Timing

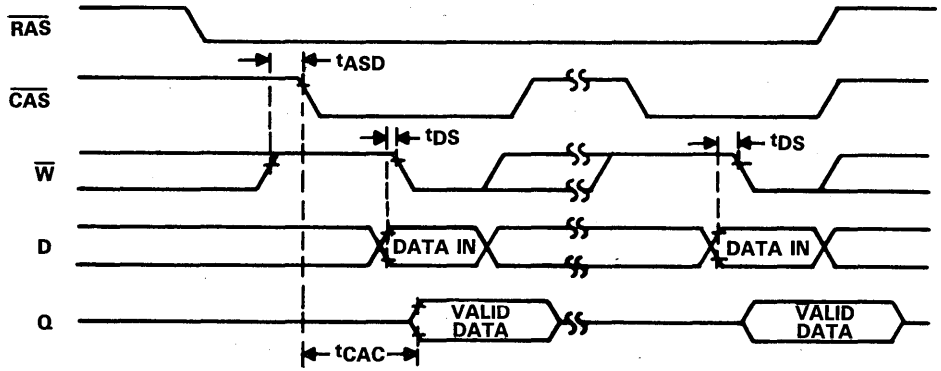


Figure 8. Page Mode R-M-W Cycle Timing

can be instituted for memory read, write, or read-modify-write cycles.

NIBBLE MODE (REFERENCE FIGURE 9)

A nibble mode cycle is a cycle where up to four successive bits are read from or written to memory in an accelerated manner over conventional cycles. The TMS4257 incorporates circuitry providing nibble mode operation. All preconditions for read, write, and read-modify-write cycles hold true with nibble mode as well. Only the initial memory address needs to be presented to the DRAM for proper nibble mode operation. $\overline{RAS}$ will stay low for the complete memory operation, while $\overline{CAS}$ is toggled up to four times to drive the desired memory cycle functions. If $\overline{CAS}$ continues to be toggled past four times, the same four bits will be recycled in a modular fashion. Note that only the initial column address is needed since the other three bits are linked to the first one.

NIBBLE MODE VS. PAGE MODE COMPARISON

Following examination of differences between page mode and nibble mode operation, the design engineer must decide which option will best suit his application. Basically, three factors need to be analyzed:

1. The relative performance improvement of one option over the other,
2. The required additional hardware to implement one option over the other, and
3. The interval at which the processor can be interrupted to reaccess the DRAM.

Examination of the specification for particular speed ranges reveals, on the average, a 25-30% performance improvement of nibble mode over page mode. Practical implementation, however, shows approximately a 10% performance improvement. This practical implementation involves aligning important signal edges with an appropriate clock according to device specification guidelines. Hardware implementation for both the TMS4256 and TMS4257 will be approximately the same. The major difference with respect to hardware is that nibble mode requires only one row and one column address for four output data bits, while page mode requires one row and a separate column address for every data output; however, if the column address are sequential, they could be generated by an external counter. Nibble mode requires a $\overline{RAS}$ precharge period and a new row and column address to continue past four output bits, while the $\overline{RAS}$ low period maximum dictates the maximum number of page mode cycles that can occur before a precharge period must be inserted. As a result, those applications which require the host controller to not be interrupted while reading or writing a long continuous data stream may warrant the use of the page mode option. If the host controller can afford to be interrupted every four bits (from the data stream perspective) or if only short data bursts (<four bits) are necessary, the nibble mode option may be preferred. It is important to note that nibble mode will continue to outperform page mode for long data streams; but this is at the expense of host controller interruption every four bits. In addition, page mode has the capability to manuever randomly through an accessed row if the application demands it.

REFRESH OPTION

Inherent with the design of a dynamic RAM memory subsystem is the need to refresh the dynamic RAM's. Refresh is necessary because charge in the individual memory cells is stored dynamically. Every row address cycle will regenerate the stored data in all memory locations of the addressed row. Thus the full memory may be refreshed in 256 cycles. Since refresh is an important consideration in the design of dynamic RAM systems, various refresh alternatives are important to retain system design flexibility. The TMS4256 and TMS4257 employ three separate ways in which dynamic RAM refresh can be implemented:

1. $\overline{RAS}$-only refresh,
2. $\overline{CAS}$-before-$\overline{RAS}$ refresh, and
3. Hidden refresh.

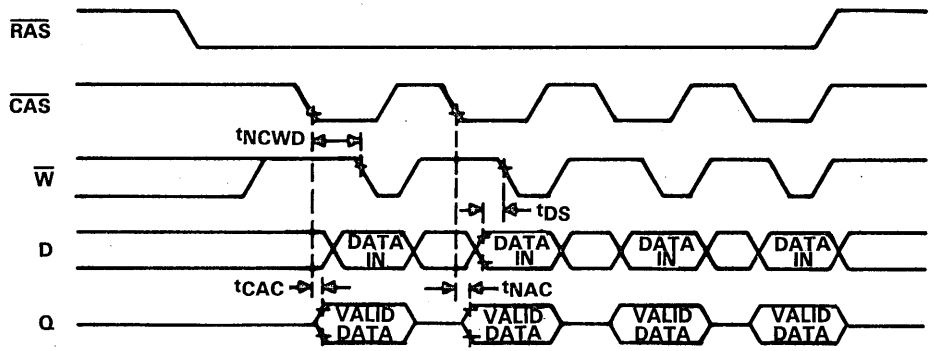


Figure 9. Nibble Mode R-M-W Cycle Timing

$\overline{\text{RAS}}$-ONLY REFRESH

This is the historical approach to refreshing dynamic RAM's. An external chip timer will enable an external counter at the appropriate refresh period to output the current row to be refreshed – the counter will be automatically incremented for the next refresh cycle. From the DRAM point of view, $\overline{\text{RAS}}$ is to be brought low a delay period following $\overline{\text{CAS}}$ going high (Figure 10). It is assumed that the row address has been generated by the external counter and it is valid a specified setup period before $\overline{\text{RAS}}$ goes low. Subsequent row refreshes can be done by bringing $\overline{\text{RAS}}$ high following the $\overline{\text{RAS}}$ low period, satisfying $\overline{\text{RAS}}$ high time (precharge), and again bringing $\overline{\text{RAS}}$ low (it is assumed again that the subsequent row address is valid and is setup a specified period before $\overline{\text{RAS}}$ goes low). There is no restriction as to the number of refresh cycles that can be accommodated sequentially. This is referred to as a "burst" refresh when several refresh cycles are done together. The periodic interjection of refresh cycles, one row at a time, is usually referred to as distributed refresh. Note that row address 8 is not necessary to accommodate the 256 cycle refresh.

$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH

This feature will be available on the TMS4256 and TMS4257 dynamic RAM's. This feature includes an on-chip refresh counter to eliminate the requirement for an external refresh counter. Examination of the cycle (Figure 11) reveals that $\overline{\text{CAS}}$ must be low a specified setup period before $\overline{\text{RAS}}$ goes low to enable a $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycle. For successive refresh cycles, $\overline{\text{CAS}}$ can remain low while $\overline{\text{RAS}}$ is taken high to satisfy precharge requirements and obtain the next refresh address. From a system point of view, the $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ option allows a level of address multiplexing (for refresh) and refresh counter circuitry to be eliminated from system dynamic $\overline{\text{RAM}}$ design. The on-chip counter will enable the present refresh address when the $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh preconditions are met. It is possible that the use of an available DRAM controller device, already provided with multiplexing and counter features, may not effectively utilize the $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh feature.

HIDDEN REFRESH

Hidden Refresh is a form of $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh which involves attaching a refresh cycle (or multiple refresh

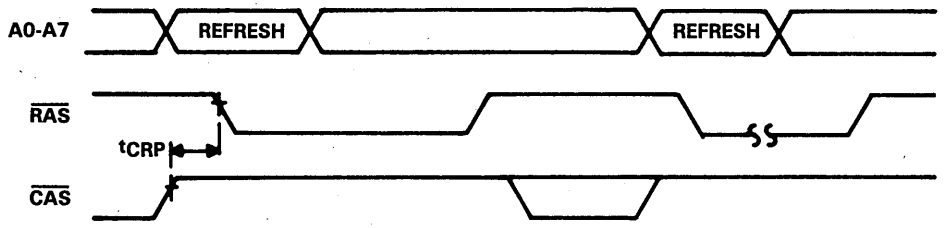


Figure 10. $\overline{\text{RAS}}$-Only Refresh

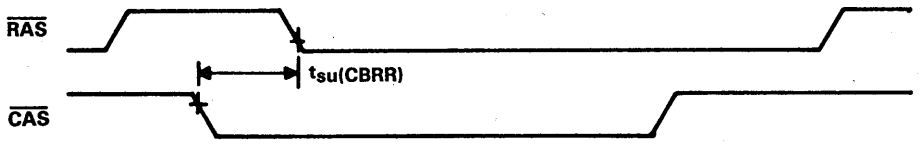


Figure 11. $\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh

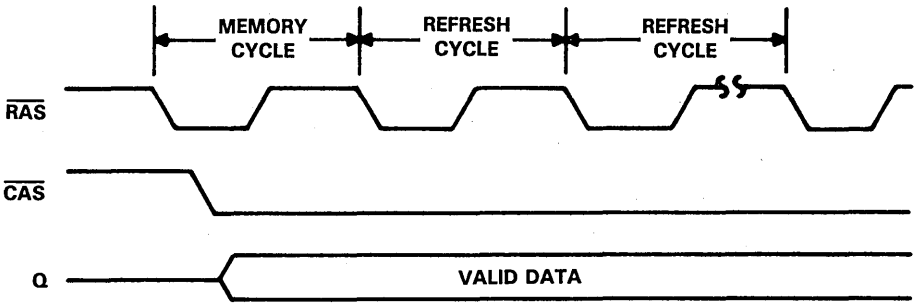


Figure 12. Hidden Refresh

cycles) directly behind a normal memory cycle (Figure 12). Instead of bringing $\overline{CAS}$ high at the end of the memory cycle as is normal, $\overline{CAS}$ remains low indicating hidden refresh cycles are to be implemented. $\overline{RAS}$ must be brought high before hidden refresh begins in order to satisfy $\overline{RAS}$ precharge requirements. This will allow sufficient time for the current refresh row address (internally generated) to be presented at the DRAM address inputs and select the appropriate row to be refreshed. Data that was presented at Q during the memory access cycle remains valid throughout the following refresh cycle(s). Multiple refresh cycles can be implemented simply by continuing to keep $\overline{CAS}$ low, bringing $\overline{RAS}$ high again to satisfy precharge, and providing the next refresh address at the appropriate time.

CONCLUSION

The purpose of this application note has been to introduce the potential 256K DRAM designer with 256K DRAM features and flexibility. Such features as nibble mode, page mode, read-modify-write, early write (etc.) allow the designer to use the memory to fit his particular application. Refresh, historically a problem in DRAM design, has been minimized as a problem with several options. The memory depth advantages of dynamic RAM's can be easily taken advantage of with the TMS4256 and TMS4257 with minimal interface problems.

TMS4256/TMS4257 Topology

INTRODUCTION

Effective dynamic RAM testing requires a thorough knowledge of the exact topology of the memory array. The most critical test routines test the pattern sensitivity of selected memory cells by performing memory accesses on surrounding cells, and monitoring the selected cells. Changes in the data stored in the monitored cell will reveal any sensitivities that the cells may have.

A total of eighteen address bits are needed to decode the one of 262,144 (256K) memory locations. The addresses are multiplexed as nine row addresses (latched by the falling edge of $\overline{RAS}$) and nine column addresses (latched by the falling edge of $\overline{CAS}$); which decode one of 512 rows or one of 512 columns, respectively. The nine addresses (A0-A8) appear on the pinout of the 256K in Figure 2(a), and are compatible with previous generation 64K DRAM devices. The only difference is the addition of the ninth address on pin 1 for the 256K device which was a no connect on 64K devices.

INTERNAL ADDRESS WEIGHTING

A closer examination of the internal addressing scheme reveals that the external pin address names do not correspond with internal address weightings. This is not relevant to system operations since the address translation will be transparent; however, testing for memory cell pattern sensitivity depends on true address weighting. This is necessary so that actual adjacent and diagonal memory cells will be exercised when monitoring a selected memory cell for pattern sensitivities. Tables I and II indicate the true row and column addresses as a function of the external address names. It is important to note that the respective row and column internal addresses do not correspond to the same external address pin names.

Table I. Row Address Weightings

Desired Row Address	Weight	TMS4256	
		Pin Name	Pin Number
RA8	2^8	A8	1
RA7	2^7	A7	9
RA6	2^6	A0	5
RA5	2^5	A2	6
RA4	2^4	A1	7
RA3	2^3	A5	10
RA2	2^2	A4	11
RA1	2^1	A3	12
RA0	2^0	A6	13

Table II. Column Address Weightings

Desired Column Address	Weight	TMS4256	
		Pin Name	Pin Number
CA8	2^8	A7	9
CA7	2^7	A0	5
CA6	2^6	A2	6
CA5	2^5	A1	7
CA4	2^4	A5	10
CA3	2^3	A4	11
CA2	2^2	A3	12
CA1	2^1	A6	13
CA0	2^0	A8	1

Since the external address names (A0-A8) correspond to different relative row and column address weights, the following multiplex configuration will simplify address decoding for the 256K DRAMs (Figure 1).

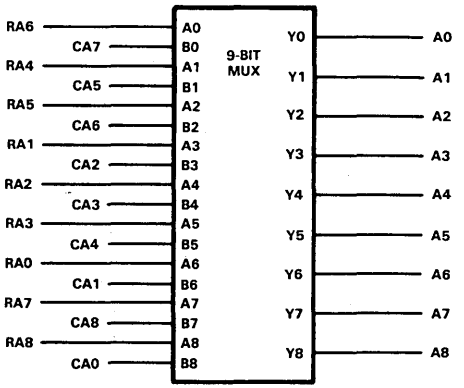


Figure 1. 256K DRAM Row and Column Multiplexer

CELL NEIGHBOR DEFINITION

With the internal address weights having been determined, the actual memory array layout must be examined to determine which memory cells are near and nearest neighbors to a given monitored memory cell. Figure 2 represents the steps of transition from the device package to the actual memory cell topology. Figure 2(a) is a representation of the TMS4256 or TMS4257 within the package, and Figure 2(b) is a photograph showing the major functional blocks of the 256K DRAM. The bit map of the memory ar-

ray is shown in Figure 2(c), while the actual cell topology for a portion of the upper and lower memory arrays are shown in Figure 2(d). From the topology (Figure 2d), there are four possible cell orientations which are dependent upon the row location of the monitored memory cell. The four memory cells outlined in Figure 2(d) indicate the four possible orientations that can occur (they are located in four separate rows). This fundamental set of cell orientations is repeated sequentially throughout the memory array. Using Figures 3(a) — 3(d) it can seen that there will be a total of 3 nearest neighbors and 9 near neighbors for each of the four orientations. In the figures, the cell marked with an X represents the cell of interest, the dark shaded cells are the nearest neighbors, and the light shaded cells represent the near neighbors.

Let (R,C) represent any cell location where R = row and C = column. The following simple routine can be utilized to develop an algorithm which calculates the nearest and near neighbors to the monitored memory cell. Simply take the row number of the monitored memory cell and divide it by four (R/4); the remainder from this calculation can be used to qualify four sets of algorithms pertaining to four sets of rows. Alternately, RA0 and RA1 may be used to determine the neighbors as indicated in the following routine.

Row =	0,4,8,...1FC RA0 = 0 RA1 = 0	1,5,9,...1FD RA0 = 1 RA1 = 0	2,6,A,...1FE RA0 = 0 RA1 = 1	3,7,B,...1FF RA0 = 1 RA1 = 1
Remainder of R/4 =	0	1	2	3
		NEAREST NEIGHBOR		
	R+1,C−1	R−2,C+0	R−2,C+0	R−1,C+0
	R+1,C+0	R−1,C+0	R+1,C+0	R−1,C+1
	R+2,C+0	R−1,C+1	R+1,C−1	R+2,C+0
		NEAR NEIGHBOR		
	R−2,C+0	R−3,C+0	R−2,C−1	R−3,C+0
	R−1,C−1	R−3,C+1	R−2,C+1	R−3,C+1
	R−1,C+0	R−2,C−1	R−1,C−1	R−2,C+0
	R+0,C−1	R−2,C+1	R−1,C+0	R+0,C−1
	R+0,C+1	R+0,C−1	R+0,C−1	R+0,C+1
	R+2,C−1	R+0,C+1	R+0,C+1	R+1,C+0
	R+2,C+1	R+1,C+0	R+2,C+0	R+1,C+1
	R+3,C−1	R+1,C+1	R+3,C−1	R+2,C−1
	R+3,C+0	R+2,C+0	R+3,C+0	R+2,C+1

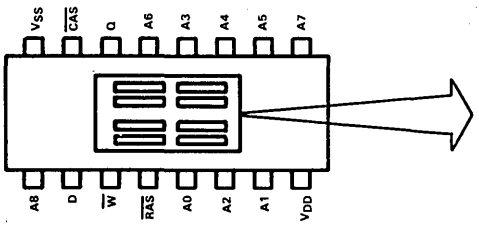


Figure 2(a). 256K DRAM Pinout

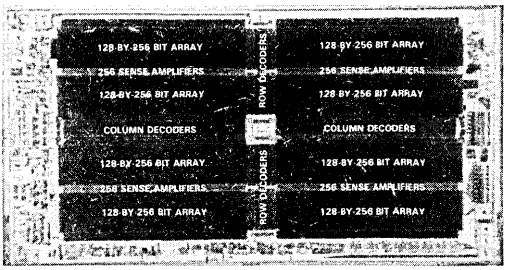


Figure 2(b). Functional Organization

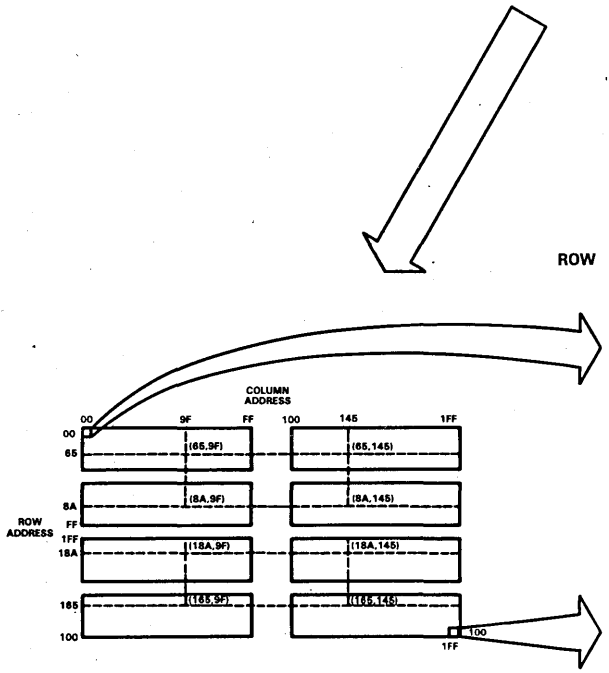


Figure 2(c). Memory Array Bit Map

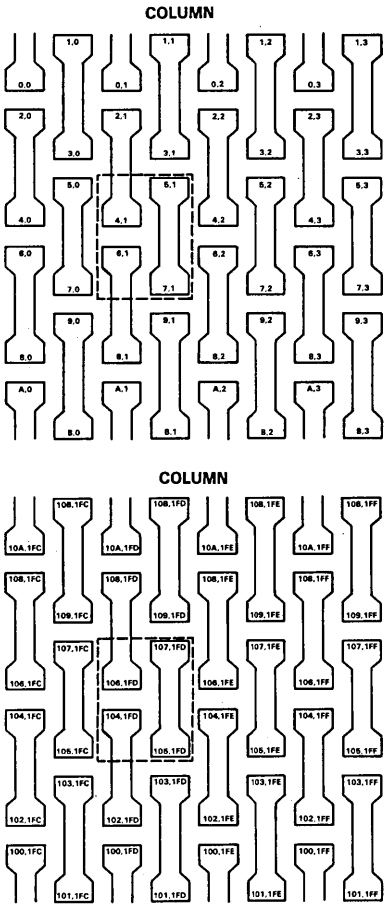
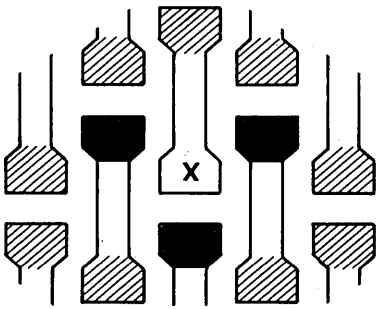
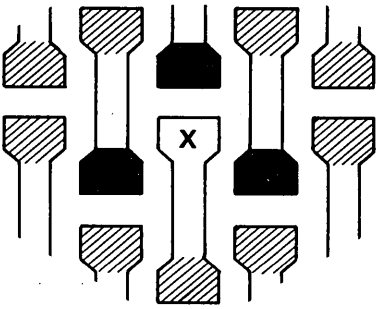


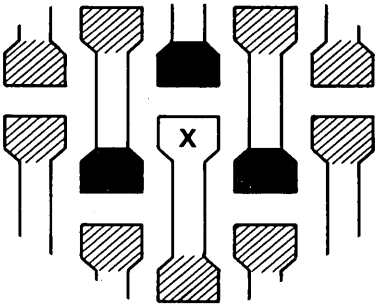
Figure 2(d). Upper and Lower Array Cell Topology



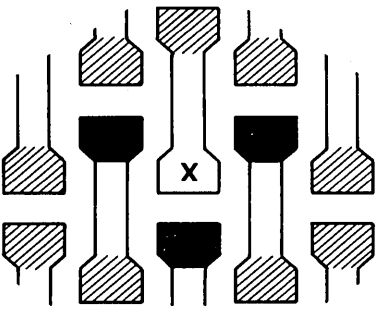
(a). Row = 0,4,8,...,1FC
Remainder of Row/4 = 0



(b). Row = 1,5,9,...,1FD
Remainder of Row/4 = 1



(c). Row = 2,6,A,...,1FE
Remainder of Row/4 = 2



(d). Row = 3,7,B,...,1FF
Remainder of Row/4 = 3

Figure 3. Near and Nearest Neighbors as a Function of Row

The algorithm for determination of nearest and near neighbors is dependent upon which of the four possible groups of rows the monitored cell is located (there is no column dependence). The lower half of the memory array mirrors that of the upper half; notice that the positive sequence of the row count proceeds from the bottom to the top in the lower half of the memory array. Consequently, the memory cell lay-out as shown in Figure 2(d) uses the above algorithms for both halves of the memory array.

INTERNAL DATA INVERSION

The data in the memory array is stored such that half of the cells are complemented with respect to the data input. The cells that store data in this inverted form are found in the odd rows; however, the internal data inversion is transparent to the device user as it is restored to a true state when read. As a result, the least significant row address (RA0) selects between true and complement data. The circuit shown in Figure 4 will provide the necessary data conversion if it is desired to compensate for the internal data inversion within the memory array.

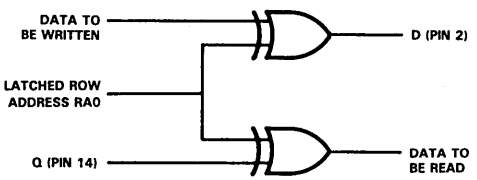


Figure 4. Circuit to Compensate for Internal Data Inversion

COMMON BIT SENSITIVITY

In order to allow the same basic memory design to implement nibble mode or x4 organization, there are actually four memory locations accessed during a single memory access cycle. The four data bits accessed are decoded by the most significant row and least significant column addresses (RA8 and CA0). RA8 selects between the upper and lower

halves of the memory array, while CA0 selects between adjacent bit lines. As a result, an algorithm can be developed which calculates the other three memory locations accessed based on the position of a given memory location. This algorithm is as follows assuming the memory location (R,C) as the base location:

CA0 =	0	1	0	1
RA8 =	0	0	1	1

MEMORY ALGORITHMS

R+0,C+1	R+0,C−1	R−256,C+0	R−256,C−1
R+256,C+0	R+256,C−1	R−256,C+1	R−256,C+0
R+256,C+1	R+256,C+0	R+0,C+1	R+0,C−1

WORD LINE SENSITIVITY

Further examination of the layout of the 256K (TMS4256) reveals that internally the word lines are in non-sequential order (0,1,3,2,...). To properly test for any word line to word line sensitivities that may occur, the testing routine must account for the non-sequential nature of the word lines. The same formula introduced earlier can be utilized to develop the algorithms for the adjacent word lines to the monitored word line (R = row). These algorithms will again be a function of the two least significant row addresses (RA0 and RA1) or the remainder of the current row divided by four.

Row =	0,4,8,...,1FC RA0=0 RA1=0	1,5,9,...,1FD RA0=1 RA1=0	2,6,A,...,1FE RA0=0 RA1=1	3,7,B,...,1FF RA0=1 RA1=1
Remainder of R/4 =	0	1	2	3
Adjacent Rows	R−2 R+1	R−1 R+2	R+1 R+2	R−2 R−1

TMS4464 Topology

INTRODUCTION

In order to effectively test the interaction between individual cells in the TMS4464, it is necessary to have a knowledge of the memory array organization and cell topology. Cell sensitivity can be tested by accessing surrounding cells and monitoring the selected cell for changes in the stored data.

Sixteen address bits are needed to decode 1 of 65,536 memory locations. Eight row address bits are set up on pins A0 through A7 and latched by the falling edge of $\overline{RAS}$. Then eight column address bits are set up on pins A0 through A7 and latched by the falling edge of $\overline{CAS}$. Data to or from memory is presented in 4-bit wide words, which must be taken into consideration when developing algorithms for cell sensitivity tests.

This report presents the pinout of the TMS4464, a bit map of the array showing the cell topology, formulas for finding "near" and "nearest" neighbor cells, a circuit for compensating for internal data inversion, and formulas for testing word line sensitivity.*

Table 1 shows the true address bit significance for both row and column addressing. This information along with Figure 1(c) can be used to write various data patterns to the array.

CELL NEIGHBOR DEFINITION

Figure 1 depicts a step-by-step magnification of the TMS4464 from a view of the package to a closeup of the array topology. Figure 1(a) shows the chip pinout and Figure 1(b) is a photograph showing the major functional blocks of the device. The bit map of the memory array is shown in Figure 1(c) while the actual cell topology for three portions of the array are shown in Figure 1(d). Note that the address of cells labeled in Figure 1(c) show (R,CD), where R is the internal row address and CD is the internal column/databit address of the cell.† Figure 1(d) best illustrates the location of each of the four databits.

Due to the folded bit line approach used in this memory array, cells shown to be horizontally adjacent in Figure 1(d) are actually paired so as to map to the same column/databit (CD). For example, cell (0,0) is shown in Figure 1(d) to be horizontally adjacent to cell (1,0). However, both are addressed in column/databit 0 (CD 0; column 0, databit 2). Likewise, cells (0,1) and (1,1) are both in column/databit 1 (CD 1; column 0, databit 4). All four of these cells, along with the mirrored cells in the lower half of the array corresponding to databits 1 and 3, are contained in column address 0. (Note that column address 0 addresses all cells referenced by CD 0 and CD 1.) In summary, a column address selects four databits and each databit is comprised of two horizontally adjacent cell arrays. Based on this addressing sequence, it can be seen that four unique cell orientations exist for each column/databit (CD) corresponding to four separate rows. The four orientations are shown by the outlined box in Figure 1(d). In this particular case the four rows are rows 4, 5, 6, and 7; however, this fundamental cell orientation is repeated throughout the memory array and is related, as shown in Figure 2, to row addresses 0 and 1 (RA0 and RA1).

* Throughout the text of this report, the terms DQ1–DQ4 and databit 1–databit 4 are used synonymously. In actuality, DQ1–DQ4 refer to the external pins of the TMS4464 and databit 1–databit 4 refer to the internal bits accessed.

† The column/databit addresses are not the same as the column addresses but rather increment twice as fast. To convert from column/databit to column address, divide the column/databit by two. The resulting integer is the actual column address. In order to determine the actual databit, take the remainder of the division and multiply it by two. This result is scaled depending on the location of the cell. If it is located in the upper half of the array, add two to the result; if it is found in the lower half of the array, add one to the result. This final sum is the databit in question.

Table 1. Address Weightings

Desired Column Address	Desired Row Address	Weight	TMS4464	
			Pin Name	Pin Number
CA7	RA7	2^7	A7	10
CA6	RA6	2^6	A6	6
CA5	RA5	2^5	A5	7
CA4	RA4	2^4	A4	8
CA3	RA3	2^3	A3	11
CA2	RA2	2^2	A2	12
CA1	RA1	2^1	A1	13
CA0	RA0	2^0	A0	14

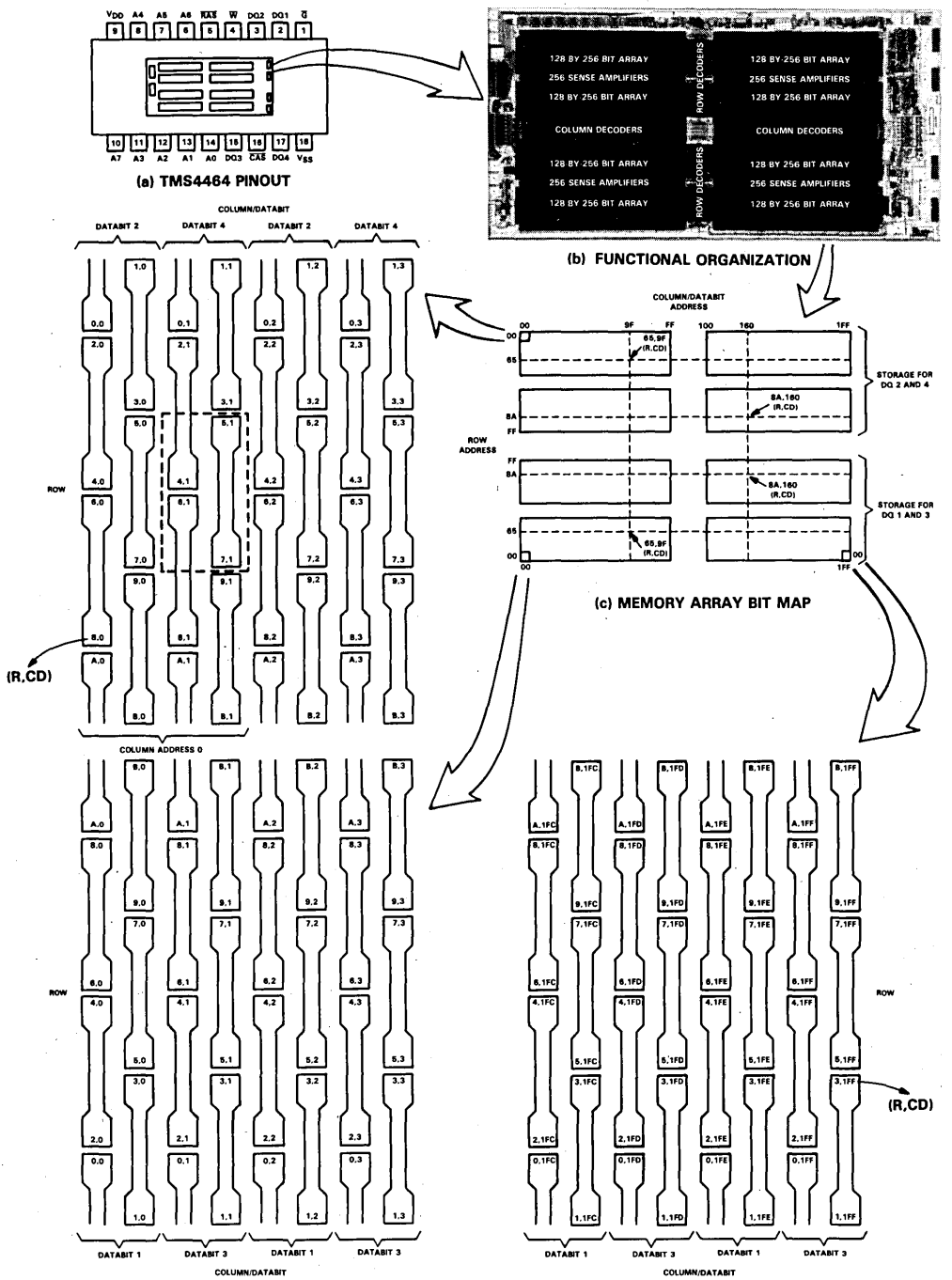

(a) TMS4464 PINOUT
(b) FUNCTIONAL ORGANIZATION
128 BY 256 BIT ARRAY
256 SENSE AMPLIFIERS
COLUMN DECODERS
ROW DECODERS
(c) MEMORY ARRAY BIT MAP
STORAGE FOR DQ 2 AND 4
STORAGE FOR DQ 1 AND 3
ROW ADDRESS
COLUMN/DATABIT ADDRESS
(R,CD)
COLUMN ADDRESS 0
DATABIT 1
DATABIT 2
DATABIT 3
DATABIT 4
COLUMN/DATABIT
ROW
(d) ARRAY CELL TOPOLOGY

Figure 1.

Figure 2 depicts the four possible cell orientations based on the row location of a selected cell. The boxes better show the selected cell orientation as it refers to the boxed area in Figure 1(d). Cells that surround any one given cell are called neighboring cells or neighbors, and are considered here for their degree of influence. As shown, there will be a total of 3 "nearest" neighbors and 9 "near" neighbors for each of the four orientations. In the figure, the cell marked with the X represents the monitored cell, the dark shaded cells are the nearest neighbors, and the light shaded cells represent the near neighbors. Near neighbors have a lesser degree of influence on the selected cell than do nearest neighbors. It should be noted here that one of the three nearest neighbors to a selected cell will always fall in an adjacent databit. If the selected cell is in databit 1 (DQ1), the adjacent databit will be DQ3 and a nearest neighbor will be located there. If the selected cell resides in DQ2, then one nearest neighbor will be in DQ4. A monitored cell in DQ3 will find a nearest neighbor in DQ1, and a monitored cell in DQ4 will have a nearest neighbor in DQ2. Further examples are shown in Appendix A.

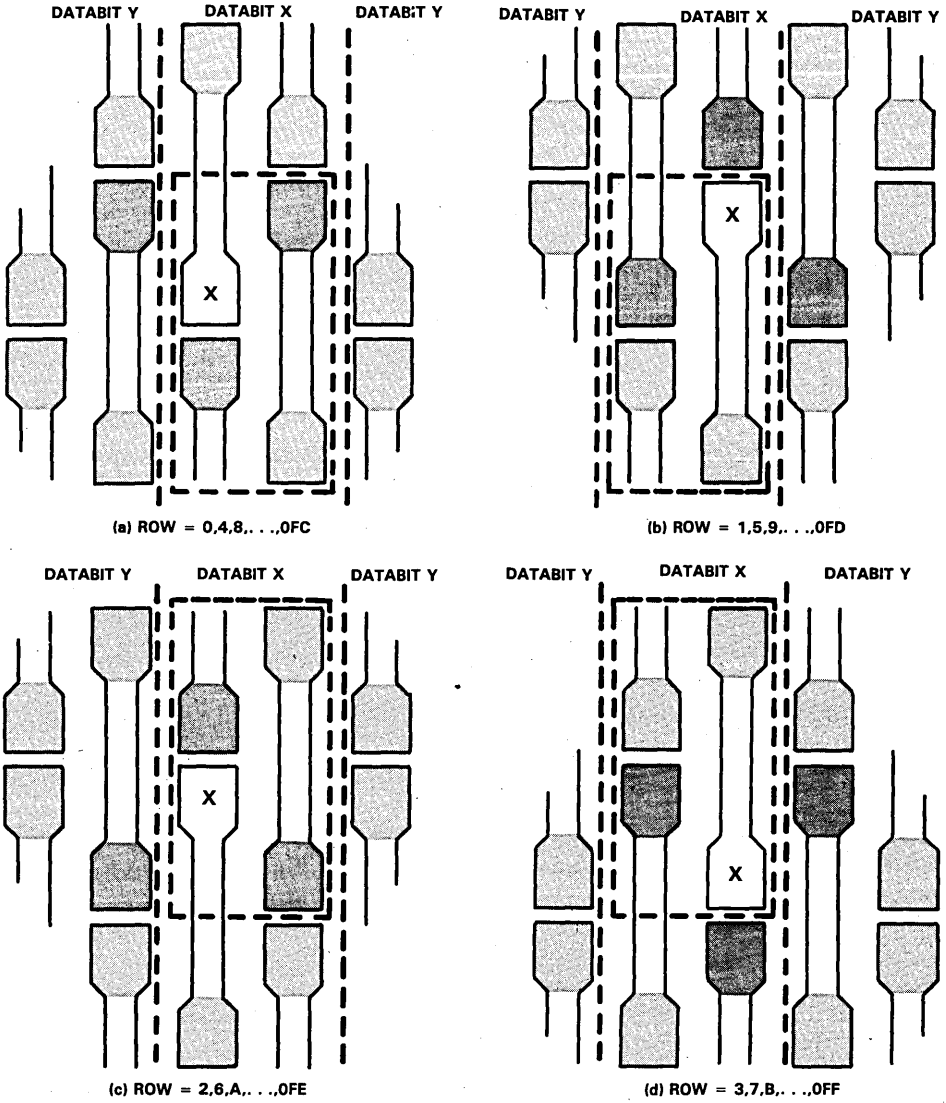


Figure 2. Near and Nearest Neighbors as a Function of Row

The formulas for finding the near and nearest neighbors are given below. The row address of the selected cell is divided by four (R/4) and the remainder of this calculation is used to qualify four sets of equations pertaining to the four rows in each orientation. An alternate method of using RA0 and RA1 to qualify the set is also shown.

Let (R,CD) represent any cell location where R = ROW ADDRESS and CD = COLUMN/DATABIT ADDRESS.

As can be seen by Figure 1(c), the lower half of the memory array mirrors that of the upper half. Note the positive sequence of the row count from bottom to top in the lower half of the array. Figure 1(d) illustrates the location of the four databits accessed during a read or write operation, two in the upper array and two in the mirrored lower array.

Row=	0,4,8,...,0FC RA0=0 RA1=0	1,5,9,...,0FD RA0=1 RA1=0	2,6,A,...,0FE RA0=0 RA1=1	3,7,B,...,0FF RA0=1 RA1=1
Remainder of R/4=	0	1	2	3
		NEAREST NEIGHBOR		
	R+1,CD−1	R−2,CD+0	R−2,CD+0	R−1,CD+0
	R+1,CD+0	R−1,CD+0	R+1,CD+0	R−1,CD+1
	R+2,CD+0	R−1,CD+1	R+1,CD−1	R+2,CD+0
		NEAR NEIGHBOR		
	R−2,CD+0	R−3,CD+0	R−2,CD−1	R−3,CD+0
	R−1,CD−1	R−3,CD+1	R−2,CD+1	R−3,CD+1
	R−1,CD+0	R−2,CD−1	R−1,CD−1	R−2,CD+0
	R+0,CD−1	R−2,CD+1	R−1,CD+0	R+0,CD−1
	R+0,CD+1	R+0,CD−1	R+0,CD−1	R+0,CD+1
	R+2,CD−1	R+0,CD+1	R+0,CD+1	R+1,CD+0
	R+2,CD+1	R+1,CD+0	R+2,CD+0	R+1,CD+1
	R+3,CD−1	R+1,CD+1	R+3,CD−1	R+2,CD−1
	R+3,CD+0	R+2,CD+0	R+3,CD+0	R+2,CD+1

WORD LINE SENSITIVITY

As can be deduced from the topology, the word lines of the TMS4464 are in nonsequential order (0, 1, 3, 2,...). In order to test for word line to word line sensitivity, this fact must be taken into consideration. The formulas shown earlier in the description of near and nearest neighbors can be utilized here to find the adjacent word lines to a monitored word line. Each equation is a function of the two least significant row addresses (RA0 and RA1) or the remainder of the current row divided by four (R=row).

Row=	0,4,8,...,0FC RA0=0 RA1=0	1,5,9,...,0FD RA0=1 RA1=0	2,6,A,...,0FE RA0=0 RA1=1	3,7,B,...,0FF RA0=1 RA1=1
Remainder of R/4=	0	1	2	3
Adjacent Rows	R−2 R+1	R−1 R+2	R+1 R+2	R−2 R−1

INTERNAL DATA INVERSION

Data is stored in the memory array such that half the cells are complemented with respect to the input data. The odd rows contain inverted data, while the even rows store the data in its true form. The inverted data is restored to a true state when read, making the inversion transparent to the user. The least significant row address selects between the true and complemented forms. Figure 3 shows a circuit to compensate for the internal data inversion within the memory array.

When row address 0 is low, the true data form is accessed and data is passed without inversion. When row address 0 is high, the inverted form is accessed and data is inverted as it is written to or read from the memory. Also, the 74LS241 remains ready to write data to the TMS4464 until $\overline{G}$ goes low. When this occurs, data is transferred from the TMS4464 to the system databus for read operations.

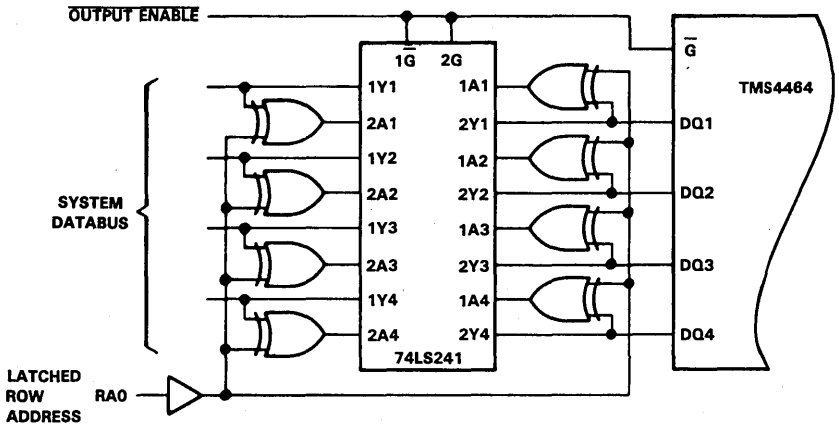


Figure 3. Circuit to Compensate for Internal Data Inversion

APPENDIX A

The two examples below use the formulas given in this report to find the nine near and three nearest neighbors to a selected cell. In order to illustrate the difference between column addresses and column/databit addresses, locations for the neighboring cells are stated using both notations.

The set of equations used will be determined by the selected row address (refer back to the listed equations on page 4 of the text). The equations to convert from column/databit (CD) to column address (Col) and from column address to column/databit are shown below.

CD=(Col*2)+constant1
where constant1=0 for DQ=1, DQ=2
constant1=1 for DQ=3, DQ=4

Col=INT[CD/2]
DQ=(MOD[CD/2]*2)+constant2
where constant2=1 for cell in lower half of array
constant2=2 for cell in upper half of array

In the examples, R=Row; C=Column,Col; CD=Column/Databit; DQ=Databit.

Example 1:

Row	5A		Row	5A
Col	F2	is equivalent to	Column/Databit(CD)	1E5
DQ	4			

(DQ4 indicates that cell is located in upper half of array)

NEAREST NEIGHBORS

Basic Formula	R,CD Format	R,C,DQ Format
R−2, CD+0	(R=58, CD=1E5)	(R=58, C=F2, DQ=4)
R+1, CD+0	(R=5B, CD=1E5)	(R=5B, C=F2, DQ=4)
R−1, CD+1	(R=59, CD=1E6)	(R=59, C=F3, DQ=2)

NEAR NEIGHBORS

R−2, CD−1	(R=58, CD=1E4)	(R=58, C=F2, DQ=2)
R−2, CD+1	(R=58, CD=1E6)	(R=58, C=F3, DQ=2)
R−1, CD−1	(R=59, CD=1E4)	(R=59, C=F2, DQ=2)
R−1, CD+0	(R=59, CD=1E5)	(R=59, C=F2, DQ=4)
R+0, CD−1	(R=5A, CD=1E4)	(R=5A, C=F2, DQ=2)
R+0, CD+1	(R=5A, CD=1E6)	(R=5A, C=F3, DQ=2)
R+2, CD+0	(R=5C, CD=1E5)	(R=5C, C=F2, DQ=4)
R+3, CD−1	(R=5D, CD=1E4)	(R=5D, C=F2, DQ=2)
R+3, CD+0	(R=5D, CD=1E5)	(R=5D, C=F2, DQ=4)

Example 2:

Row	A0		Row	A0
Col	46	is equivalent to	Column/Databit(CD)	8C
DQ	1			

(DQ1 indicates that cell is located in lower half of array)

NEAREST NEIGHBORS

Basic Formula	R,CD Format	R,C,DQ Format
R+1, CD−1	(R=A1, CD=8B)	(R=A1, C=45, DQ=3)
R+1, CD+0	(R=A1, CD=8C)	(R=A1, C=46, DQ=1)
R+2, CD+0	(R=A2, CD=8C)	(R=A2, C=46, DQ=1)

NEAR NEIGHBORS

R−2, CD+0	(R=9E, CD=8C)	(R=9E, C=46, DQ=1)
R−1, CD−1	(R=9F, CD=8B)	(R=9F, C=45, DQ=3)
R−1, CD+0	(R=9F, CD=8C)	(R=9F, C=46, DQ=1)
R+0, CD−1	(R=A0, CD=8B)	(R=A0, C=45, DQ=3)
R+0, CD+1	(R=A0, CD=8D)	(R=A0, C=46, DQ=3)
R+2, CD−1	(R=A2, CD=8B)	(R=A2, C=45, DQ=3)
R+2, CD+1	(R=A2, CD=8D)	(R=A2, C=46, DQ=3)
R+3, CD−1	(R=A3, CD=8B)	(R=A3, C=45, DQ=3)
R+3, CD+0	(R=A3, CD=8C)	(R=A3, C=46, DQ=1)

Latchup Immunity of the HVCMOS EPROM Family

CMOS technology provides N-Channel and P-channel MOS transistors as well as both NPN and PNP parasitic bipolar transitors. Figure 1 shows the HVCMOS process cross section illustrating the above mentioned devices.

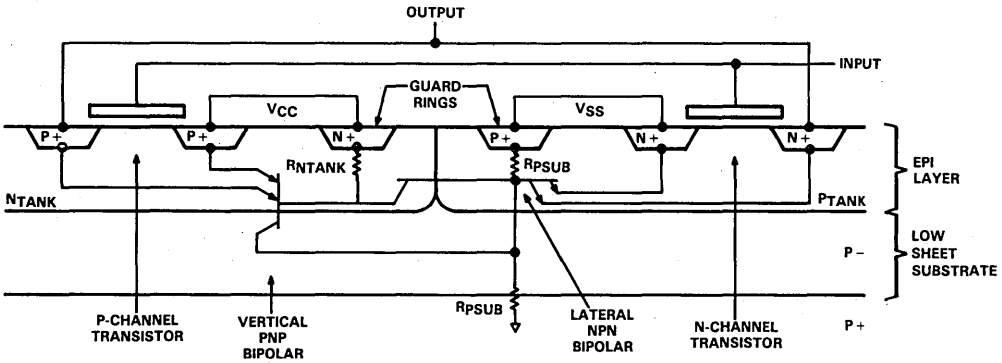


FIGURE 1. HVCMOS PROCESS CROSS SECTION

TI's HVCMOS family will drive full CMOS output levels due to the complimentary output driver configuration (N-channel pull down device and P-channel pull up device). This means that the system has direct access to the emitters of both parasitic bipolars via the output pins and access to the NPN parasitic bipolar emitter via the input pins. Figure 2 shows the equivalent parasitic SCR of the input pin. Figure 3 illustrates the output pin.

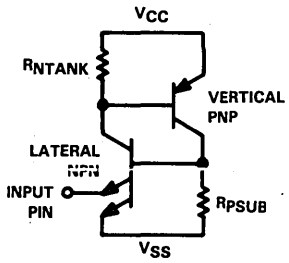


FIGURE 2. INPUT PIN PARASITIC SCR

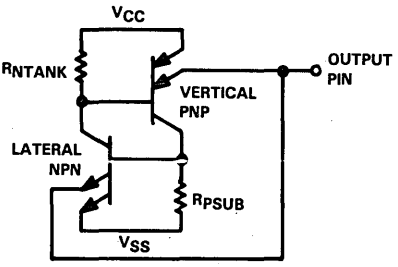


FIGURE 3. INPUT PIN PARASITIC SCR

The HVCMOS process and circuit design combine to offer significant improvements in system immunity:

- —The EPI substrate material lowers R_{PSUB} and is primarily responsible for holding off the lateral NPN device.
- —Full V_{CC} tank and V_{SS} substrate guardrings on inputs and outputs lower the critical base resistors R_{NTANK} and R_{PSUB}. This helps hold off the parasitic PNP and NPN respectively.
- —Maximum horizontal spacing from the emitter of the NPN to the vertical PNP (NPN base width) on all input and output pins minimizes the gain of the lateral NPN.

System latchup immunity on the TI HVCMOS EPROM family is a minimum of 250 mA on all input and output pins. This provides latchup immunity well beyond any potential current/voltage transients at the P.C. board level when the EPROM is interfaced to industry standard TTL or MOS logic devices.

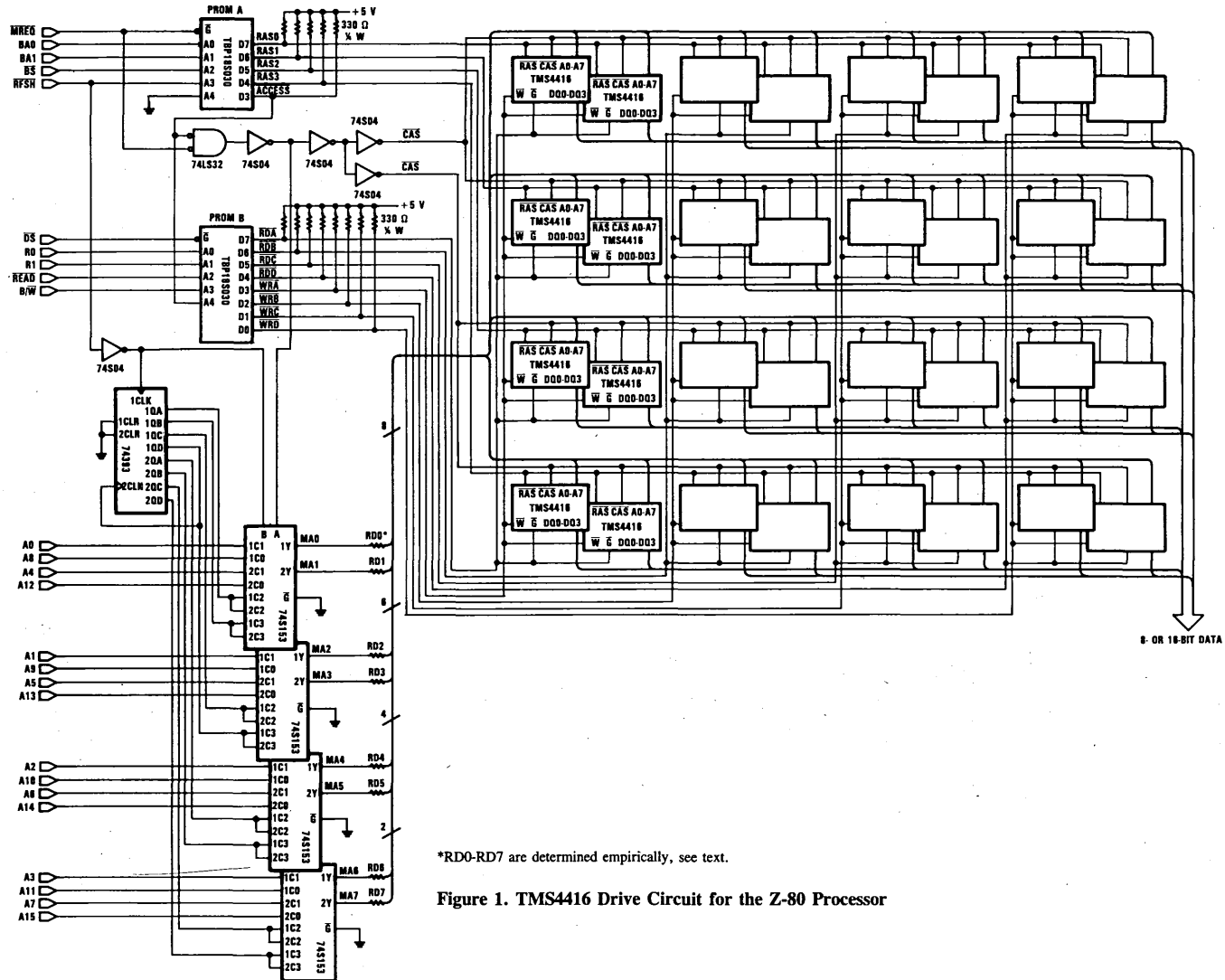
TTL Drivers for the TMS4416-15

Some form of driver circuitry is needed when DRAMs are used with processors, such as the Z-80 or Z-8000. One possible solution involves the use of a precision delay line; however, a more cost-effective and efficient approach uses TTL devices as drivers. Two versions of TTL driver circuits are shown in Figures 1 and 2. The first figure shows the drive circuit for a memory array using TMS4416-15 DRAMs and the Z-80 processor; Figure 2 shows the same array configured for use with the Z-8000 processor. Both circuits are designed to drive 256K bytes of memory arranged in either 8- or 16-bit words. They provide all DRAM control signals, address multiplexing, and refresh address generation. The circuits shown for the Z-80 and the Z-8000 use the hidden refresh provided by these devices so that refresh/access arbitration is not necessary. Time delays were selected to provide maximum performance from the TMS4416-15 with off-the-shelf components. (Enhanced operation could be obtained by hand selecting components for single applications.) A comparison of the two circuits will reveal the differences between the two. The following description applies to both circuits.

The memory array is arranged as 4 banks of 8 TMS4416s. Two TBP18S030 PROMs decode and generate the control signals for the drive circuit. BA0 and BA1 are used to select which bank of memory will be accessed. $\overline{\text{MREQ}}$ and $\overline{\text{ACCESS}}$ are NORed and then delayed by 3 inverters to provide a $\overline{\text{CAS}}$ signal. The MUX signal that is used to switch the 74S153 multiplexers and propagate the column address to the memories is taken from the output of the first inverter in the $\overline{\text{CAS}}$ delay. $\overline{\text{CAS}}$ is connected to all the devices in the array. (Since $\overline{\text{RAS}}$ acts as a chip enable, $\overline{\text{CAS}}$ will only activate the memories in the bank that has $\overline{\text{RAS}}$ active; this keeps the power consumption of the array lower than using $\overline{\text{CAS}}$ as select logic.) Two $\overline{\text{CAS}}$ drivers are used to reduce the effects of the capacitive load of the DRAM $\overline{\text{CAS}}$ inputs. (This also improves drive characteristics and reduces noise.) Series damping resistors have been added to reduce ringing on the address lines. These resistors should be between 15 and 68 ohms, depending on the circuit board layout, and can be determined by examining the address waveforms with an oscilloscope and selecting a value that produces the cleanest signal. The desired 8- or 16-bit data word from the active bank is selected using R0, R1, and the $\overline{\text{READ}}$ line. R0 and R1 can be address lines from the Z-8001 or they can be generated from memory mapping logic. If the $\overline{\text{READ}}$ input is low during an access cycle, the output enable of the TMS4416 will be activated ($\overline{\text{RDA}}$-$\overline{\text{RDD}}$); a high input to $\overline{\text{READ}}$ will select a write output ($\overline{\text{WRA}}$-$\overline{\text{WRD}}$). Using this matrix, the memory can be divided into sixteen 16K × 8 or eight 16K × 16 blocks. The desired word width of the data output will be dependent on the microprocessor being used. For an 8-bit data bus the two data busses shown in the diagram would be connected in parallel. Since the Z-80 only directly accesses 64K of memory, bank select logic must be included in this memory system to provide higher order address lines. The design of the bank select circuitry has been left up to the user, but might include memory mapping or other logic.

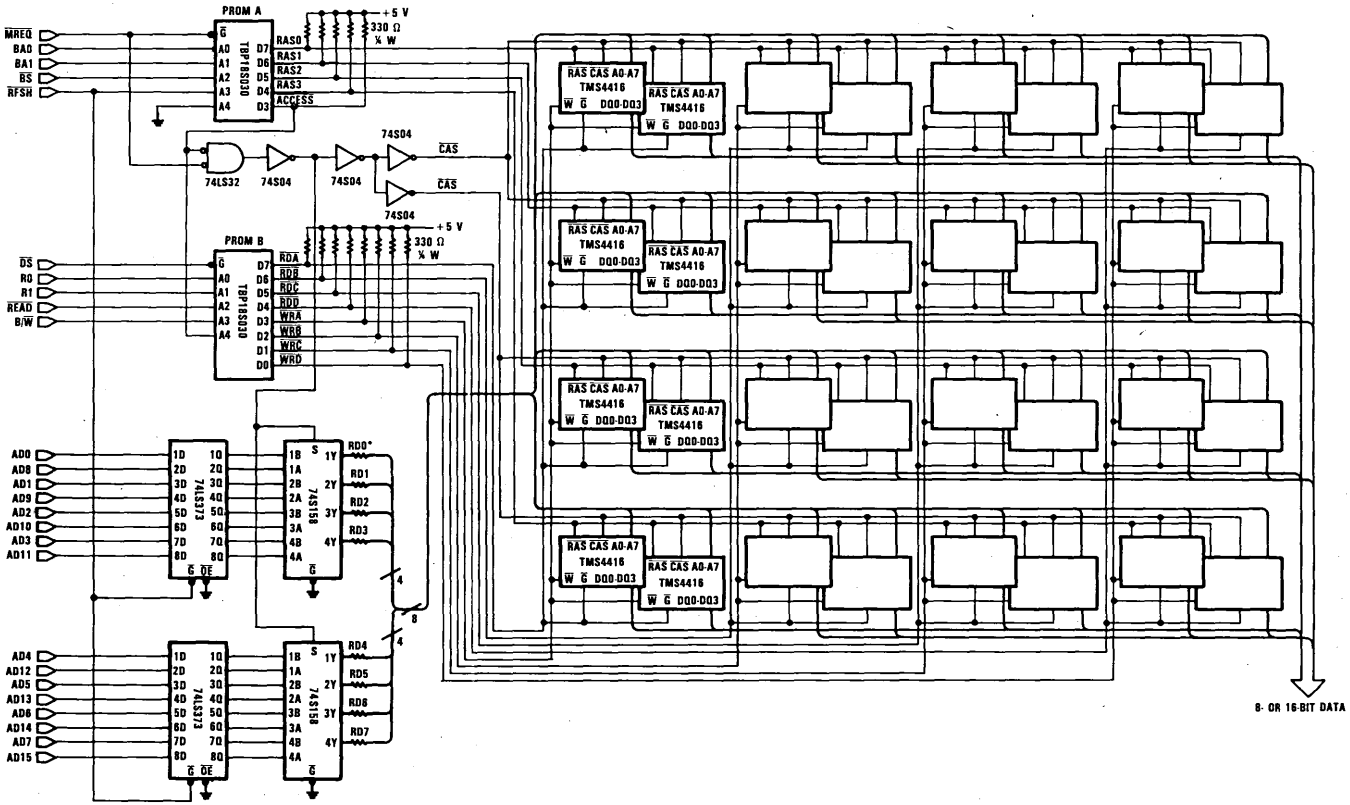
An external refresh counter has been added to the drive circuit for the Z-80 since the Z-80 internal refresh counter does not support 256 cycle refresh. (Application Brief DR-7 shows a circuit to add the extra refresh address bits similar to the implementation used here.) As the Z-8000 provides 9-refresh-address bits, its internal refresh counter was used.

A description of the signals used in both circuits previously illustrated is given in Table 1. Due to slight differences in the signals available from the Z-80 and Z-8000 processors, a slight modification of the interface between the processor and the TTL drive circuits shown will be required. The differences in the interface are shown in Figure 3. The $\overline{\text{DS}}$ signal is generated from the Z-80's $\overline{\text{RD}}$ and $\overline{\text{WR}}$ lines. The B/$\overline{\text{W}}$ input should be tied to a 5-10 kilohm pullup resistor. The $\overline{\text{RFSH}}$ signal can be decoded from the status lines of the Z-8000 as shown with the 74S138; however, it could also be done with other types of logic if desired. The address of the Z-8000A is only guaranteed valid for 35 ns so the address latches are necessary when using DRAMs with this microprocessor. $\overline{\text{MREQ}}$ is used to enable the 74LS373 transparent latches for both memory accesses and refresh cycles.



*RD0-RD7 are determined empirically, see text.

Figure 1. TMS4416 Drive Circuit for the Z-80 Processor



*RD0-RD7 are determined empirically, see text.

Figure 2. TMS4416 Drive Circuit for the Z-8000

Table 1. Signal Description

SIGNAL NAME	DESCRIPTION
$\overline{MREQ}$	From the Z-80 or Z-8000, indicates address valid
BA0, BA1	Address for $\overline{RAS}$ selection, decoded from high order addresses
$\overline{BS}$	Board select to designate DRAM access, decoded from high order addresses
$\overline{RFSH}$	Z-80 output or decoded from the Z-8000 status outputs. Signals a refresh cycle
$\overline{DS}$	Z-8000 output indicating data valid on the multiplexed address/data lines
R0, R1	Address for read or write selection, decoded from high order addresses
$\overline{READ}$	If low, indicates a memory read and if high, indicates a memory write
B/$\overline{W}$	Indicates if the Z-8000 is doing a 8- or 16-bit memory access
A0-A15	Z-80 address outputs
AD0-AD15	Z-8000 multiplexed address/data lines

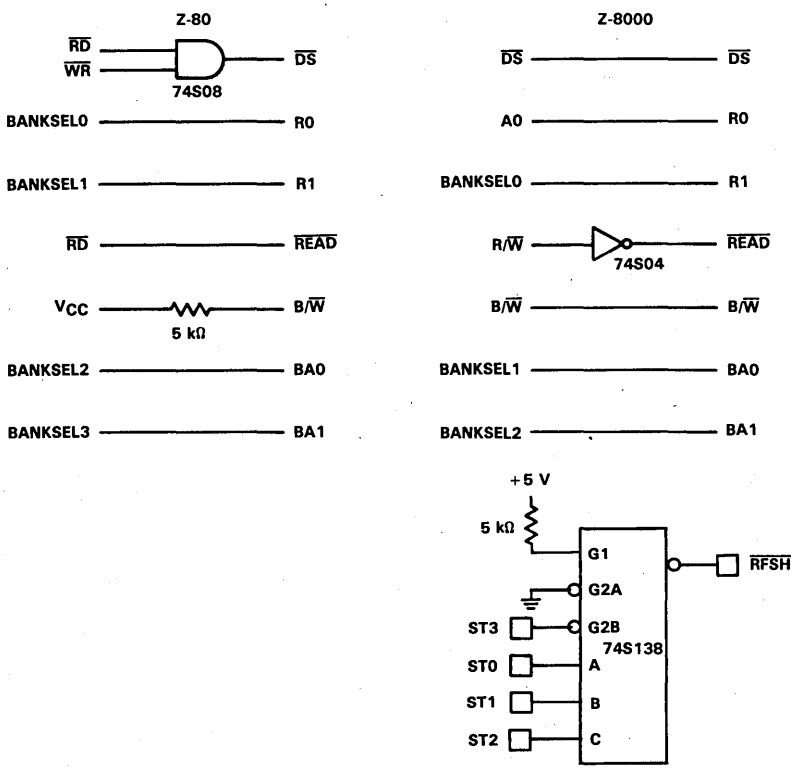


Figure 3. Interface Circuitry Differences

Tables 2 and 3 list the data for the PROMs to provide the control signals. Both the binary and hexadecimal programming data have been supplied.

The TTL drive circuits previously described allow the TMS4416-15 to operate at maximum speed. Although there are many ways to provide the necessary control signals for DRAMs, the drive circuits described will provide insight into the control logic that is necessary to use dynamic RAMs. TTL circuitry was selected in order to avoid the cost of a precision delay line.

Table 2. PROM A Program

PIN NAME	A3	A2	A1	A0	D7	D6	D5	D4	D3	HEX
FIGURE NAME	$\overline{RFSH}$	$\overline{BS}$	BA1	BA0	$\overline{RAS0}$	$\overline{RAS1}$	$\overline{RAS2}$	$\overline{RAS3}$	ACCESS	
	0	X	X	X	0	0	0	0	1	0F
	1	0	0	0	0	1	1	1	0	77
	1	0	0	1	1	0	1		0	B7
	1	0	1	0	1	1	0	1	0	D7
	1	0	1	1	1	1	1	0	0	E7
	1	1	0	0	1	1	1	1	1	FF
	1	1	0	1	1	1	1	1	1	FF
	1	1	1	0	1	1	1	1	1	FF
	1	1	1	1	1	1	1	1	1	FF

Table 3. PROM B Program

PIN NAME	$\overline{G}$	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	HEX
FIGURE NAME	$\overline{DS}$	B/$\overline{W}$	$\overline{READ}$	R1	R0	$\overline{RDA}$	$\overline{RDB}$	$\overline{RDC}$	$\overline{RDD}$	$\overline{WRA}$	$\overline{WRB}$	$\overline{WRC}$	$\overline{WRD}$	
	0	0	0	0	0	0	0	1	1	1	1	1	1	3F
	0	0	0	0	1	0	0	1	1	1	1	1	1	3F
	0	0	0	1	0	1	1	0	0	1	1	1	1	CF
	0	0	0	1	1	1	1	0	0	1	1	1	1	CF
	0	0	1	0	0	1	1	1	1	0	0	1	1	F3
	0	0	1	0	1	1	1	1	1	0	0	1	1	F3
	0	0	1	1	0	1	1	1	1	1	1	0	0	FC
	0	0	1	1	1	1	1	1	1	1	1	0	0	FC
	0	1	0	0	0	0	1	1	1	1	1	1	1	7F
	0	1	0	0	1	1	0	1	1	1	1	1	1	BF
	0	1	0	1	0	1	1	0	1	1	1	1	1	DF
	0	1	0	1	1	1	1	1	0	1	1	1	1	EF
	0	1	1	0	0	1	1	1	1	0	1	1	1	F7
	0	1	1	0	1	1	1	1	1	1	0	1	1	FB
	0	1	1	1	0	1	1	1	1	1	1	0	1	FD
	0	1	1	1	1	1	1	1	1	1	1	1	0	FE
	1	X	X	X	X	1	1	1	1	1	1	1	1	FF

TM4164EC4 Provides High-Density Memory Array

MOS Memory
Applications Engineering

This Application Report illustrates the use of the TM4164EC4 (64K × 4) Memory Module with the TMS4500A DRAM Controller (see Figure 1). The description of a memory board using both devices will be given along with full schematics, edge connector pinout, and signal description. An interface to the Intel 8086 microprocessor is also provided as a typical application.

BOARD DESCRIPTION

Designed by Texas Instruments to demonstrate the TM4164EC4 in a system environment, the board provides a flexible, high-density memory array which is adaptable to most applications.

The board uses one TMS4500A and eight TM4164EC4s for 256K bytes of dynamic RAM memory on a 3.25 inch × 4.5 inch card. The TMS4500A gives the board a static appearance in the system, providing many of the necessary timing and control signals to the DRAM array. Each TM4164EC4 is comprised of four TMS4164 plasitic-leaded-chip-carriers and two ceramic chip capacitors, that are surface mounted on a PC substrate to form a single-in-line package (SIP).[1] The cost savings that can be realized with SIPs include reduced PC board size, fewer plated-through-holes, and the elimination of bypass capacitors on the motherboard.

The TM4164EC4 SIPs are mounted on 0.350 inch centers, and occupy 6.16 square inches of board area

[1]See Appendix A.

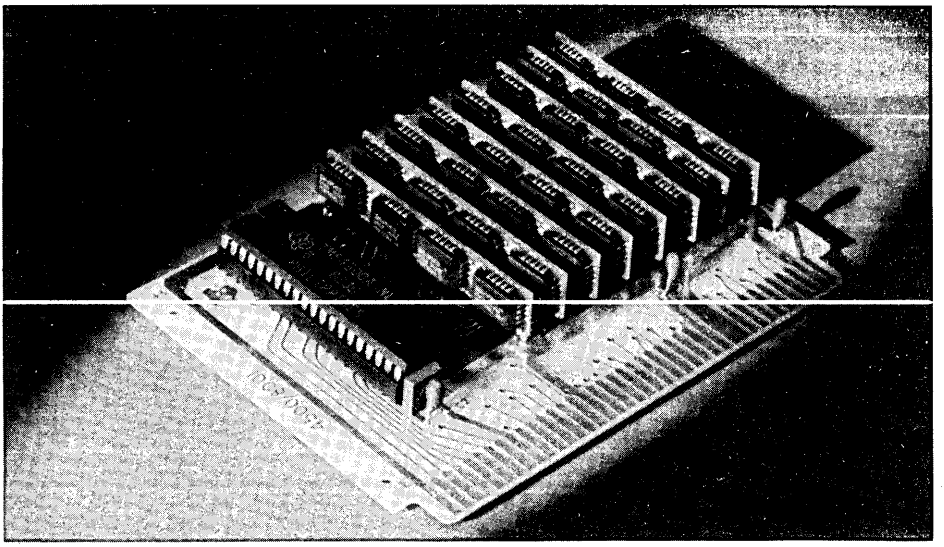


Figure 1. TM4164EC4/TMS4500A Memory Board

[8 × 0.350 × 2.2 inches (TM4164EC4 length)], for a density of greater than five memory devices per square inch. This is approximately a 2X density improvement with respect to DIPs. The TM4164EC4s can be mounted on centers as narrow as 0.200 inches if adequate cooling is provided. This would give a density of greater than nine memory devices per square inch or approximately a 3.5X improvement over DIPs for the above array.

The equivalent DIP implementation of the TM4164EC4 would require 68 plated-through-holes (four 16-pin packages and two, 2-lead capacitors) as opposed to the 22 required for a single TM4164EC4. The large number of plated-through-holes increase board cost and reduce the available PC board area for trace routing often requiring an increase in the number of board layers.

The on board capacitors eliminate the need for bypassing on the motherboard and offer superior performance over equivalent leaded capacitors due to the reduced lead inductance.

While the TMS4500A gives the board a static appearance and the TM4164EC4 provides a high-density memory array, the interconnect bus gives the board flexibility. All the signals necessary to provide for 8- or 16-bit operation, separate or common I/O, and internal or external memory refresh along with the address and control lines for the TMS4500A are brought to the board edge.

MEMORY ORGANIZATION

The memory is organized as two banks of 128K bytes, accessible in byte or word format (word = 16 bits). Each row is selected by $\overline{RAS0}$ or $\overline{RAS1}$ (see Figure 2) to provide 16 bits of available data. The 16 bits of data are then read or written in byte or word format by controlling the upper and lower $\overline{CAS}$ and $\overline{WR}$ signals ($\overline{UCAS}$, $\overline{LCAS}$, $\overline{UWR}$, and $\overline{LWR}$). The lower byte of data corresponds to D0-D7 and Q0-Q7, while upper data corresponds to D8-D15 and Q8-Q15. It is necessary to organize the memory as such to provide operation with 16-bit microprocessors that do both byte and word accesses. For microprocessors with 8-bit data busses, D0-D7 and Q0-Q7 are tied to D8-D15 and Q8-Q15, respectively. The $\overline{CAS}$ and $\overline{WR}$ signals are then used to multiplex and demultiplex the data onto and from the microprocessor data bus.

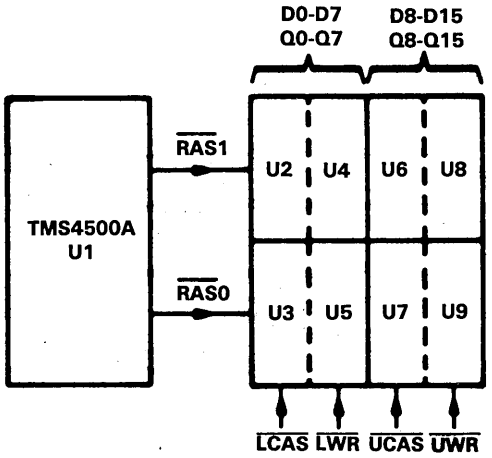


Figure 2. Block Diagram

Table I. Pin Nomenclature

Name	Description
A0-A15	Address Inputs
$\overline{ACR}$	Access Control, Read
$\overline{ACW}$	Access Control, Write
ALE	Address Latch Enable
$\overline{BRDEN}$	Board Enable
$\overline{CAS}$	Column Address Strobe
CLK	Clock Input
D0-D15	Data In
FS0	Frequency Select 0
FS1	Frequency Select 1
GND	Ground
$\overline{LCAS}$	Lower $\overline{CAS}$
$\overline{LWR}$	Lower Write
$\overline{REFREQ}$	Refresh Request
REN1	$\overline{RAS}$ Enable 1
RDY	Ready
Q0-Q15	Data Out
TWST	Timing/Wait Strap
$\overline{UCAS}$	Upper $\overline{CAS}$
$\overline{UWR}$	Upper Write
+5	+5 Volts

BOARD OPERATION

As mentioned earlier the board provides a 16-bit data bus with separate data-in and data-out connections (see Figure 3). This allows the board to be configured for common (D0-D15 tied to Q0-Q15) or separate input/output (I/O). Notice that corresponding D and Q lines are located across from each other for easy interconnection (see Table II). Common I/O operation requires the memory array to be accessed in the early-write mode ($\overline{WR}$ low prior to $\overline{CAS}$). The board provides flexible control of the memory array by bringing $\overline{CAS}$ from the TMS4500A to the board edge allowing it to be combined with external logic to derive the $\overline{UCAS}$ and $\overline{LCAS}$ signals. If desired the $\overline{CAS}$ signal from the TMS4500A can directly drive the memory array by connecting $\overline{CAS}$ to $\overline{UCAS}$ and $\overline{LCAS}$ via jumpers J1 and J2. This type of configuration necessitates the use of $\overline{LWR}$ and $\overline{UWR}$ to control access to the memory array on write cycles. Also, all 16 bits of data will be active on a read cycle for both byte and word accesses. All the necessary signals needed to interface to the TMS4500A have been brought to the board edge. Notice that the binary weighting on the memory address outputs of the TMS4500A do not correspond to that of the TM4164EC4 memory addresses. This does not in any way affect the operation of the board as the TM4164EC4s are random-access devices. This configuration was chosen to simplify the board layout. Table III gives the relationship between the TMS4500A and TM4164EC4 addresses.

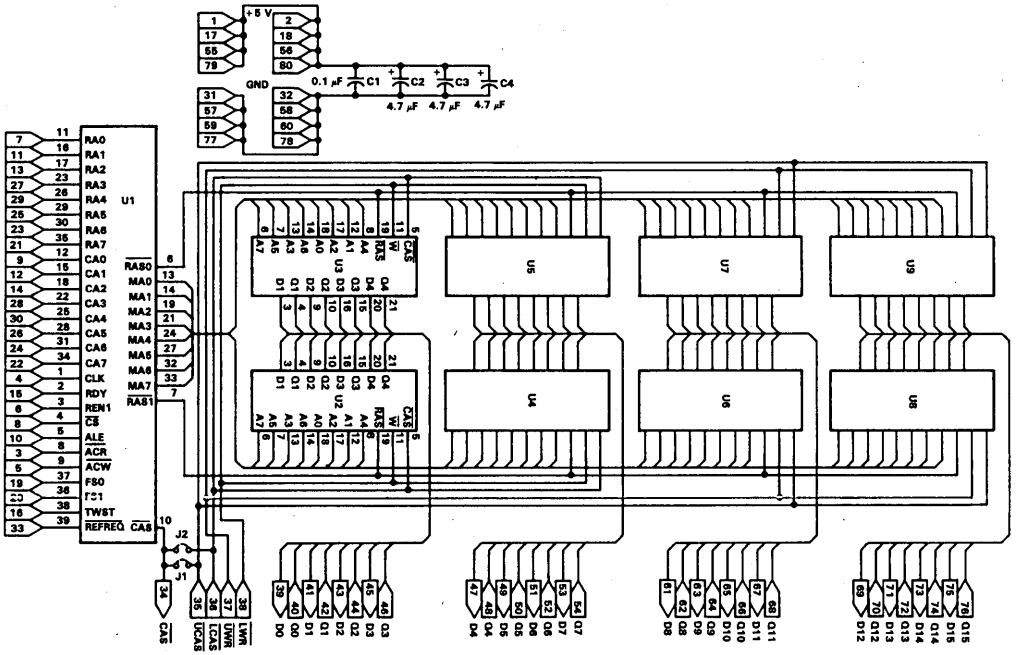


Figure 3. Board Schematic

Table II. Buss Format

Pin	Signal	Pin	Signal
1	+5	2	+5
3	$\overline{\text{ACR}}$	4	CLK
5	$\overline{\text{ACW}}$	6	REN1
7	A0	8	BRDEN
9	A8	10	ALE
11	A1	12	A9
13	A2	14	A10
15	RDY	16	TWST
17	+5	18	+5
19	FS0	20	FS1
21	A7	22	A15
23	A6	24	A14
25	A5	26	A13
27	A3	28	A11
29	A4	30	A12
31	GND	32	GND
33	$\overline{\text{REFREQ}}$	34	$\overline{\text{CAS}}$
35	$\overline{\text{UCAS}}$	36	$\overline{\text{LCAS}}$
37	$\overline{\text{UWR}}$	38	$\overline{\text{LWR}}$
39	D0	40	Q0
41	D1	42	Q1
43	D2	44	Q2
45	D3	46	Q3
47	D4	48	Q4
49	D5	50	Q5
51	D6	52	Q6
53	D7	54	Q7
55	+5	56	+5
57	GND	58	GND
59	GND	60	GND
61	D8	62	Q8
63	D9	64	Q9
65	D10	66	Q10
67	D11	68	Q11
69	D12	70	Q12
71	D13	72	Q13
73	D14	74	Q14
75	D15	76	Q15
77	GND	78	GND
79	+5	80	+5

Table III. Address Relationship

TMS4500A	TM4161EC4
MA0	A4
MA1	A1
MA2	A2
MA3	A0
MA4	A6
MA5	A3
MA6	A5
MA7	A7

8086 INTERFACE

The circuit is designed to operate with a 5 MHz 8086 in the maximum mode configuration without memory wait states (see Figure 4). The memory interface is simplified by configuring the memory for early write operation, which allows corresponding D and Q lines to be tied together for common I/O operation (see Table II). The board select logic is derived from addresses A18 and A19 and mapped via a 74S139 at address locations 40000-7FFFFhex (256K bytes). Address A17 is connected to REN1 of the TMS4500A to defferentiate between the two banks of memory (REN1 = 0, selects $\overline{\text{RAS}}$0; REN1 = 1, selects $\overline{\text{RAS}}$1). To provide for byte accesses, AD0 and $\overline{\text{BHE}}$ are combined with other logic to yield the necessary upper and lower $\overline{\text{CAS}}$ signals ($\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$). The 8284 is strapped for asynchronous ready operation to provide sufficient $\overline{\text{CAS}}$ access time on access-grant cycles. See the *TMS4500A Users Manual* for details of the TMS4500A operation. The $\overline{\text{AMWC}}$ and $\overline{\text{MRDC}}$ signals from the 8288 are used to derive $\overline{\text{ALE}}$ and $\overline{\text{ACR}}$ which initiates memory-access cycles. $\overline{\text{AMWC}}$ and $\overline{\text{MRDC}}$ are used instead of ALE from the 8288 to allow sufficient row address setup time to the memory (the row addresses are delayed by two propagation delays, 74LS373, and TMS4500A). This signal is also fed into the input of a 74S74 to be synchronized with the rising edge of CLK (see Figure 5). The output of the 74S74 is then combined with AD0 and $\overline{\text{BHE}}$ and $\overline{\text{CAS}}$ to form the upper and lower $\overline{\text{CAS}}$ signals. Synchronizing ALE of the TMS4500A with CLK ensures data valid at the memory

before the falling edge of $\overline{UCAS}$ and $\overline{LCAS}$ (necessary for early write operation). The $\overline{UWR}$ and $\overline{LWR}$ signals are driven by $\overline{AMWC}$ to guarantee them to be valid before $\overline{UCAS}$ and $\overline{LCAS}$ low. $\overline{AMWC}$ is buffered to drive the 32 DRAMs.

This Application Report has illustrated the use of the TMS4500A and TM4164EC4 for a flexible, high-density memory array. The TMS4500A gives the board a static appearance, while the TM4164EC4 provides a density of greater than five memory devices per square inch. Higher densities can be obtained with narrower SIP spacings requiring adequate cooling. The 8086 interface provides a typical application and demonstrates the flexibility of the board. As circuit board designers strive to reduce board space and implement more functions on a board, the use of SIPs such as the TM4164EC4 will provide a vehicle by which this goal can be achieved.

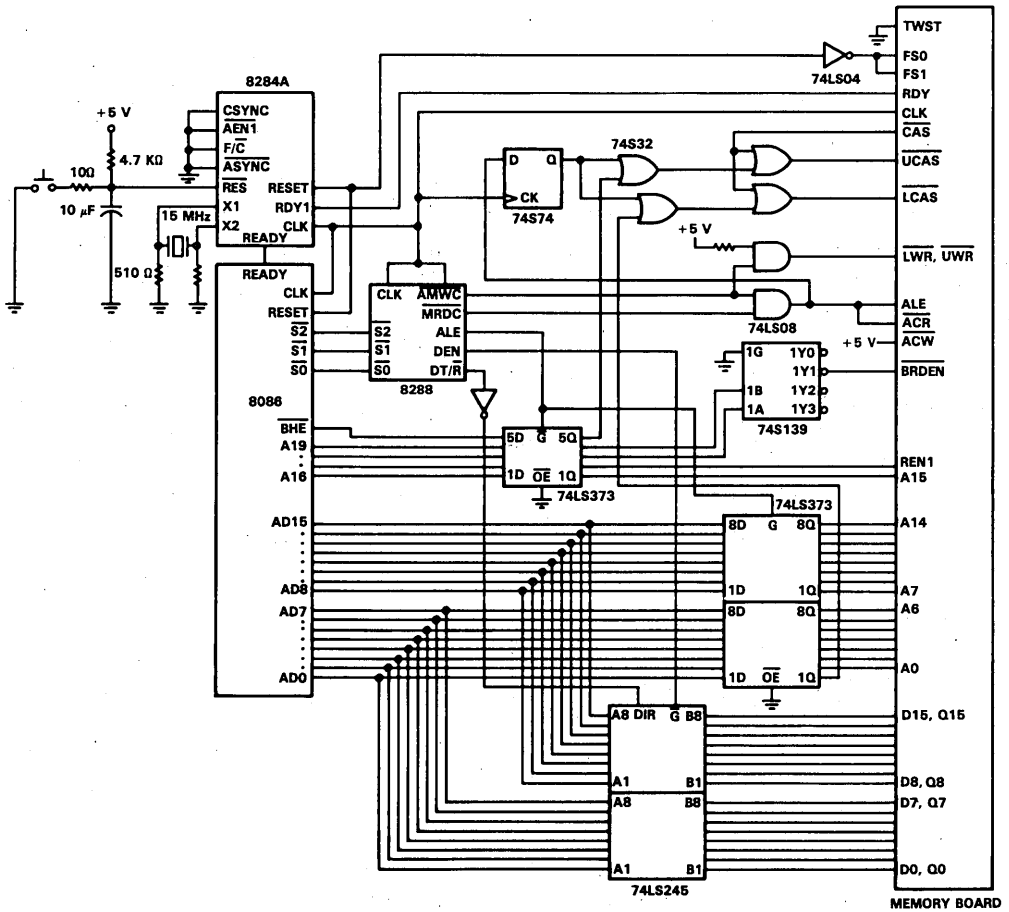


Figure 4. 8086 Interface

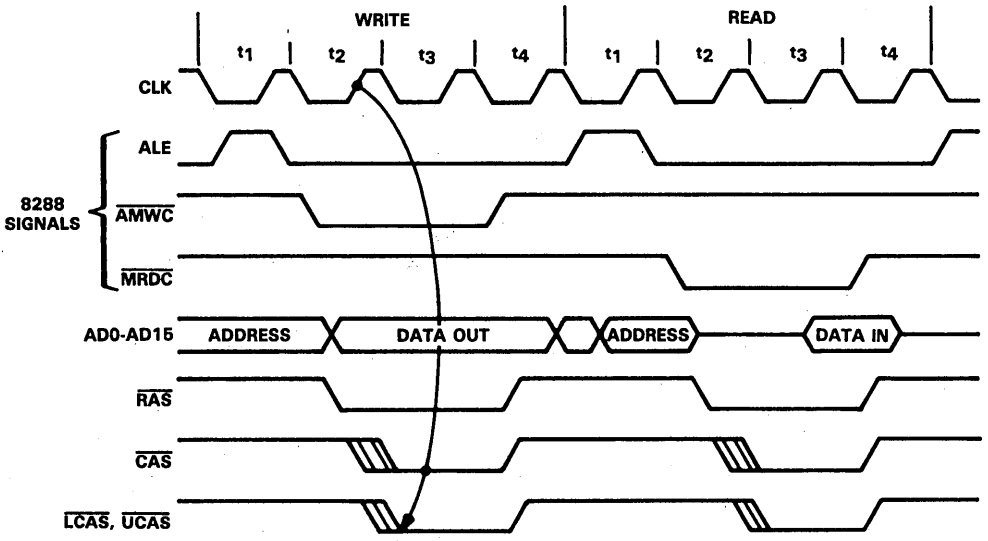
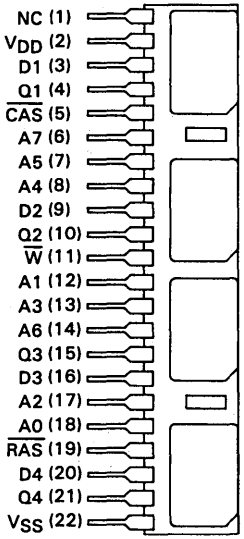


Figure 5. 8086 Interface Timing Diagram

APPENDIX A
TM4164EC4 PIN OUT AND FUNCTIONAL BLOCK DIAGRAM



(TOP VIEW)

Figure A-1. Pin Out Drawing

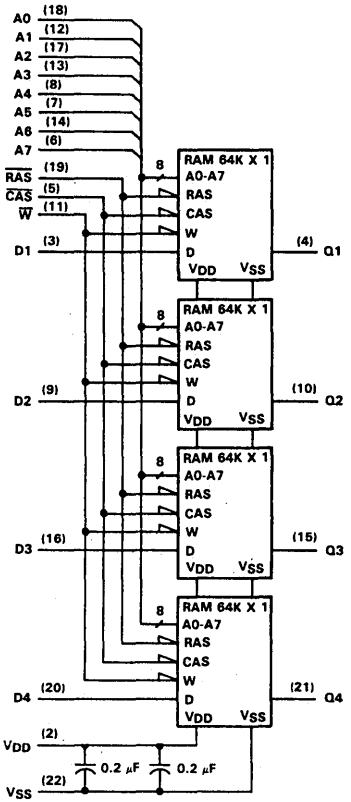
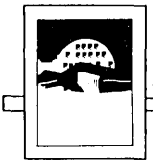


Figure A-2. Functional Block Diagram



JOINING TEXT AND GRAPHICS ENHANCES VIDEO PERFORMANCE

A dual-port RAM with a built-in shift register eliminates bottlenecks and speeds data transfers.

by David W. Gulley

Bit-mapped video graphics systems exemplify the need for higher density and higher performance semiconductor memories. Yet, all too often, these same memory devices are the bane of the system. The newest dynamic RAM devices, however, are allowing changes to the video graphics system organization. Thus, they are eliminating redundant support logic circuitry and providing a flexible system environment.

DRAMs, long associated with the frame buffer within the graphics section of a video system, provide the highest density and lowest cost storage for memory-intensive displays. High resolution graphics systems, such as those used in engineering workstations and computer aided design/computer aided manufacturing (CAD/CAM) terminals, require multiple memory planes to achieve the color capability necessary for a good user interface. In such a system, many parameters influence the available features while keeping the size and cost reasonable.

Often, the video display system designer is forced into "make-do" solutions when deciding on value-added features, especially where display memory is involved. Some features are common to many designs, and directly relate to the acceptance of a design in the market. Features considered high priority are the efficient integration of text and graphics, the time to redraw the screen image, the time to move objects onscreen, the amount of memory to map the display, and the support logic to use the memory effectively.

A typical video system contains separate text and graphics controllers (Fig 1). Thus, the system processor does not have to manipulate both the text display list and the graphics bit-mapped image. This system has evolved from the earliest text-only terminals, where there were no graphics requirements. In early systems, display memory consisted of perhaps 2 Kbytes for the display list RAM and 2 Kbytes for the character ROM. The need to place graphics images onscreen was first addressed using character graphics. By deepening the character ROM or adding a RAM to the character-generation circuit, user-defined characters could be produced.

To achieve more flexibility in image control, a bit-mapped memory is added into which the system can directly store images to be displayed. The mixed text

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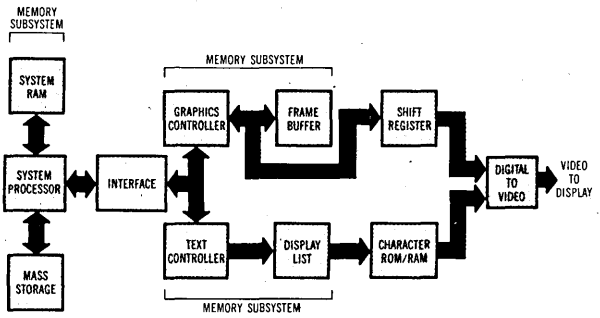

Fig 1 Mixed text and graphics systems, developed from simple text-only systems, have a lot of redundant circuitry.

and graphics solution is really a patch to add graphics capability to table-driven systems. However, future system design will treat text and graphics uniformly. New memory architectures are needed to make the transition to this type of system environment. The TMS4161 multiport video RAM is one device able to ensure this by providing a design path to the development of unified bit-mapped text and graphics systems (Fig 2).

Tracking the growth of video displays

Currently, uniformity is not in general use. Video display evolution has moved in another direction. As higher resolution and multiple gray-level or color planes were added, the screen refresh required higher data rates from the memory, giving less time to the system processor for data management in the frame buffer. As the resolution (pixels/in.^{2}) of the display increases by a factor of 2, the size of the display memory increases by 4, and the display interval for each pixel is reduced by a factor of 4.

The availability of dense, low cost DRAMs allowed expansion to higher resolutions (from a memory chip cost standpoint), but the DRAM architecture (1 bit wide) increased the data bus traffic needed to refresh the screen image. Graphics system controllers were added to the system to isolate the large bandwidth display bus from the system bus. If this isolation had not occurred, system processor throughput would have been seriously degraded. The data bus would be clogged with data passing from the frame buffer to the display.

The memory required for the frame buffer RAM is typically 10 (for black and white) to 40 (for 4 bits per pixel) times larger than the display list RAM in the mixed text system. Display data transferred to the screen loads the data bus so that there is considerably less time available to update the frame buffer memory than the display list RAM. Yet, since the nature of the data is single pixels, it requires more manipulating than display characters. More memory must then be accessed more often, and in less time. Hardware additions often implement many basic display functions, since there are not enough available memory accesses for software to optimally update the RAM.

The mixed video system consists of three memory subsystems, each containing a memory controller, memory logic, and glue logic. Glue logic also connects the controller to the system processor, and provides the required memory array drive. Each subsystem contains similar logic functions. Yet, the functions cannot be shared and still survive the data transfer bottleneck to the screen. Therefore, this is where DRAM features (actually, lack of features) have most influenced video system design. The many design approaches involving dedicated hardware control compensate for the limited accesses available to the memory. These approaches have partially relieved bus contention problems. But, the cost has

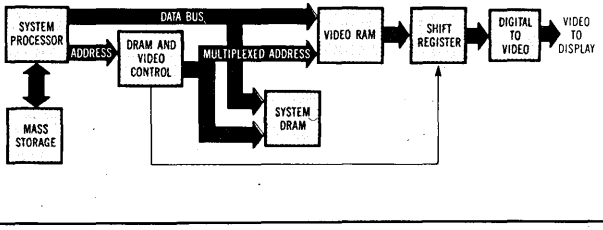

Fig 2 Unifying text and graphics eliminates redundancies. This results in faster and lower cost systems.

been a loss of system flexibility and compatibility for effective system upgrade. Dedicated controllers tend to lock the system into a set of fixed commands, character fonts, and data structures.

A high resolution (1024 x 1024 or 1280 x 1024) graphics display, as used in CAD systems, requires data from the refresh buffer at between 75 and 125 MHz from each plane, dependent upon the actual display device (monitor) specification. This is independent of the graphics controller's need to access the refresh buffer in order to update the image stored in memory. In the following analysis of system performance, a 1024 x 1024 noninterlaced display is used as a guide. Table 1 values describe the timings used in the analysis. Total frame time in Fig 3 consists of the active display interval, horizontal blanking interval (horizontal retrace), and the vertical blanking interval (vertical retrace).

TABLE 1
Display Parameters

Pixel clock frequency	88.00	MHz
Pixels per scan line	1380	
Lines per frame	1063	
Displayed pixels per scan line	1024	
Displayed lines	1024	
Horizontal blanking interval	4.05	μs
Vertical blanking interval	611.60	μs
Pixel time	11.36	ns

A typical video system design

The 88-MHz pixel data rate is in direct conflict with the need to update the memory quickly. The display refresh and the memory update must share the same data bus in the mixed text system. Updating the high resolution screen in a reasonable time frame requires some cycles to be available during the active display interval. A 1024 x 1024 display could be built using sixteen 64-Kbit DRAMs. But, even with the fastest parts, it is extremely difficult to get the video data rate required, and to be able to do useful screen image manipulations without reverting to a second (double) frame buffer.

The TMS4416 16-K x 4 RAM provides the large video bandwidth required in medium to high resolution video systems. Many systems that incorporate 16-K x 4 RAMs use the previous generation of 16-Kbit memories, and are using the x4 as a replacement for four 16-K parts. A wide-word architecture provides more data lines per depth of memory using standard DRAM access timing. Addressing four times as many bits per device simplifies the hardware needed to create the display frame buffer.

Wide-word devices used within the frame buffer provide the width needed to achieve the necessary bandwidth for display (Fig 4). This brute force design yields 64 data bits and requires a 64-bit shift register—all bits are loaded in parallel. The pixel clock is running at 88 MHz. S0 and S1 control the loading and shifting of the register. This approach contains the advantage of data access interleaving, first an interval for the processor access, and then an interval for the display access to the memory. It is more easily designed and manufactured than a similar approach using 16-K x 1 devices, and is much more reliable due to component and power reductions. The disadvantage is that there must be a way to buffer the data bus in order to convert from the 64-bit wide video section to the 16-bit wide system processor. In this design, a 64 to 16 multiplexer serves this function.

In the TMS4416 implementation of this circuit, there is one access available to the graphics controller for each display cycle. There are no highly critical access timings for the 16-K x 4, as the 64-bit shift register is loaded once each 727 ns (64 times 11.36 ns), and processor timing is assumed to be tightly coupled to the video shift rates. The storage cell refresh required by the DRAM is satisfied by reading across the memory chip rows for display accesses, and therefore does not require any additional logic or control. Even with all the data lines needed to connect the 64-bit shift register, this design runs at the top of its capability. If more flexible and higher performance systems are needed, the x4 RAM is not appropriate.

Many earlier high end video systems used the double buffer technique to avoid contention problems

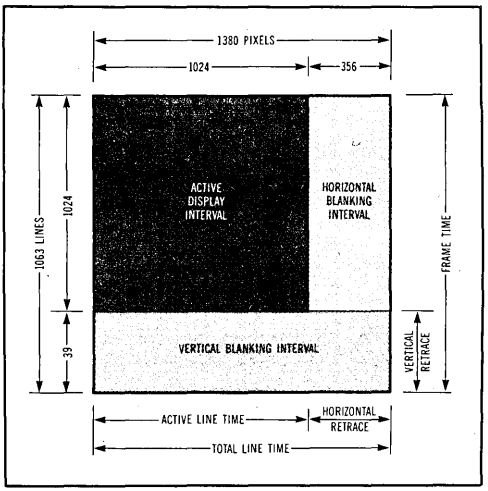

Fig 3 In a high resolution video display, the total frame time is the sum of active display time, and horizontal and vertical blanking intervals.

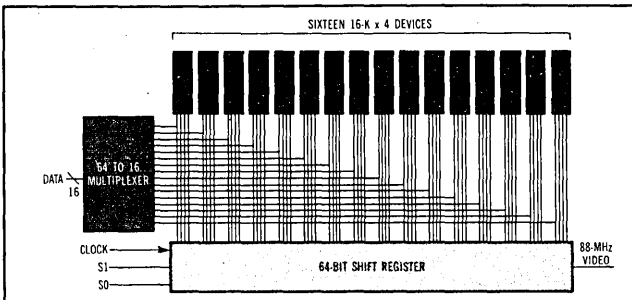

Fig 4 A brute force frame buffer design using wide-word memory devices provides interleaving of data accesses, and easier design and manufacturing compared with circuits using less dense memories.

between the graphics controller and the display refresh. In this scheme, two display frame buffers are used—one provides information for the display, the other is available to the graphics controller for updates. When the new drawing is complete, the system switches the function of the two buffers. Though this allows more interaction with the memory, it is at the expense of doubling the memory requirement. Also, when the buffers are switched, the graphics controller does not have a copy of the most recently available data image. In many systems, a form of DMA copies the data from one buffer to the other, effectively cutting the time available to the controller in half. Again, the system suffers from the lack of capability within DRAMs.

New systems are designed to be as functional to the end user as possible. The system must be flexible, tailored to individual needs, compatible with systems currently in use, and cost effective. Most new systems support multiple windows in order to display several simultaneous functions, and allow data manipulation within one window without affecting the contents of another window. But, there is a need to mix text and graphics information within a window.

Hardware control requires a large investment in design and components within the video system. New system architectures are needed to remove the display data-transfer bottleneck, eliminate redundant logic functions, and improve the system flexibility to conform to individual needs. Just as the industrial controller has progressed from a collection of SSI devices, to MSI, and now to single-chip processors, the video system control functions are moving from multiple subsystems to dedicated, optimized components.

Meeting the demands

The TMS4161 multiport video RAM remedies these problems by combining a standard 64-K x 1 DRAM with a 256-bit shift register, and the necessary controls to transfer data between the memory array and the shift register in a single package. By allowing simultaneous, asynchronous access to the two ports, the video RAM allows the system processor and the display refresh to work independently. Thus, the need for double buffering is removed, giving maximum time for the system processor to access the memory. The memory array access of the video RAM conforms to the signal and timing requirements of a standard DRAM. The onchip shift register supports high resolution data rates, and reduces video data shift logic and timing generation circuitry complexity. The shift register is configured as 4 linked 64-bit shift registers, able to provide shift lengths of 64, 128, 192 or 256 bits. These features help meet primary design criteria, and yield enhanced features for the video system.

The video RAM allows a more flexible approach to a video system design that eliminates mixed graphics approach patches. With the latter design, a bottleneck restricts data flow due to the single random access port on standard DRAM devices. Merging memory subsystems in a unified system substantially reduces design effort and cost. Redundant logic is eliminated by using the same functions for the video RAM as for system memory control. The logic required for the DRAM and video control section is currently implemented using several programmable logic arrays and MSI circuits (Fig 5). These could be placed in a gate array or other custom device.

The divider circuit is the only high speed device required, other than the external shift register, and provides the other logic with the appropriate timing signals. Not shown is the control to the external shift register, since it changes with implementation. A microprocessor or other controller can access the memory by issuing a MEMREQ/ with the appropriate read or write strobe. All other functions and timings are performed by the state sequencer.

A frame buffer using the video RAM could use a scan-line mapping architecture. This approach could also be used in the frame buffer of an existing design, although the full advantages of the dual-port would not be realized.

Scan-line mapping refers to positioning the memory devices to correspond to relative bit placements within a display scan line. Logic reduction in

the frame buffer is evident, since there is only a 16-bit shift register, and no data bus buffer/separator requirement, as in the x4 example. In this particular example, each transfer from the memory array to the shift register moves a total of 4096 bits, which provide the data for four 1024-pixel scan lines. Onchip shift register data is loaded into the 16-bit shift register to accelerate the data to the required 88 MHz. The data in the memory's shift register is clocked at 5.5 MHz, well below the device's maximum clock frequency of 25 MHz. The timing for the video RAM is derived from the pixel clock to keep the system timings synchronous.

For this design, the row address strobe (RAS) cycle consists of 10 pixel clocks for the 114-ns precharge period, and 15 clocks for the 170-ns RAS low time, for a total period of 284 ns. All cycles (refresh, read, write, and transfer between arrays and shift register) use the same timings, with differences in the sequencing of the other control inputs to the video RAM (CAS/, W/, and TR/QE/). Each device holds every sixteenth pixel along the scan line of 1024 pixels. Scan-line data comes from 64 adjacent columns in each of the 16 devices. A 16-bit processor can directly access the memory array for image manipulation if it recognizes the appropriate addressing arrangement. Thus, the system processor can issue the address of the row and column for the desired pixel. The decoding of the active chip (when accessing via the DRAM port) may be done in hardware or as an internal operation of the processor.

The 256-bit register on the video RAM can be used by the video control logic to manipulate data as well as shift the data to the display. One way to employ this register is to clear (erase) the display quickly. The processor can write to the 256 locations corresponding to one row in the memory. This row can be transferred to the shift register. The shift register to memory transfer of the memory clears the remaining rows of the memory in 255 cycles. [Alternately, the serial input (SIN), could be grounded and SCLK clocked 256 times to load the shift register with all 0s.] Thus, the frame can be erased in a fraction of the vertical retrace interval of 612 μs, for improved performance in those applications requiring rapid screen clear.

Unlimited access

Since the video RAM shift register can be loaded from memory as little as once each four scan-line times for CRT refresh, the system processor has virtually unlimited access to the display memory. During a single 16.67-ms frame time, there would need to be 256 display access cycles (one of the video RAM's shift registers loads from memory for each four scan lines), and 1087 memory cell refresh cycles (a minimum of 256 refresh each 4 ms), which remove a small portion of the available time for updating

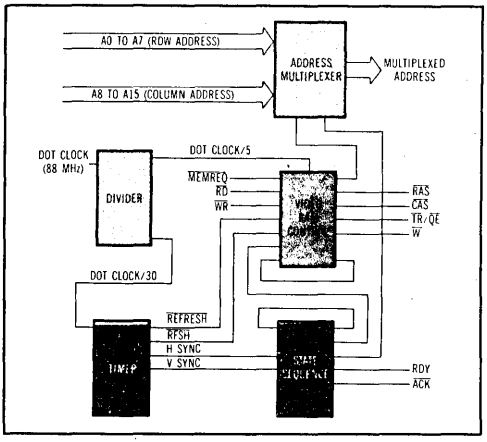

Fig 5 RAM and video control logic for a unified design can be implemented with programmable logic arrays and MSI circuits. A gate array or custom device could integrate the entire function in a high volume application.

the screen. The time for this overhead can therefore be calculated as:

MC x (#DIS + #REF)
284 x (256 + 1087) = 381 μs

Where MC is memory cycle time,
#DIS is the number of display cycles, and
#REF is the number of refresh cycles.

So, in a single frame, all but 381 μs (about 2.3 percent) of the interval to be used by the system processor for display update are available. The remaining 97.7 percent of the time to scan a complete frame is available for access by the system processor. This allows memory accesses to follow logical, predictable patterns, and consistent timing sequences. These uniform cycles reduce the system hardware burden to fit memory update accesses into a narrow window or burst.

Modern screen imaging techniques indicate that hardware should not be used for read scrolling, to maintain maximum system flexibility. Designs usually call for moving data within defined regions of the frame buffer. However, for systems with hardware scrolling, the 256-bit register on the video RAM can be used by the controller to manipulate scan-line data in the displayed image. Data from one memory row can be transferred to the shift register, and then transferred back to another row (without shifting the data), which moves the pixel data from one displayed row to another. Several such transfers can be made, giving the effect of scrolling a full screen image vertically. This will scroll the entire width of the screen, so it may not be appropriate in a system with windows, where the scroll must be done in software.

TABLE 2
Maximum Accesses to Arbitrarily Located Region

Region Size	Scan Line	Symmetric	Improvement
32 x 32	96	81	15 percent
18 x 18	54	25	54 percent
16 x 16	32	25	22 percent
10 x 10	20	9	55 percent
8 x 8	16	9	44 percent
4 x 4	8	4	100 percent

In scan-line architecture, a move of one row to an adjacent row within the video RAM results in moving the displayed line four scan lines vertically. To scroll an entire screen of lines would take:

(MTS + TC) x #ROW

(284 + 284) x 256 = 145 μs

Where MTS is the time for a memory to shift register transfer,

TC is the shift register to memory cycle time, and

#ROW is the number of rows to be moved.

This scroll operation could wrap the image around the screen, or the processor could update the display memory with a new portion of the image. The ability to move rapidly the screen image vertically may have application for some realtime systems or forms of animation, since it gives the system processor more time to update the displayed image.

The scan-line technique is preferred because it is simple and logical, and offers direct processor to memory mapping. Although scan-line mapping is generally best, other memory chip to pixel mapping schemes can be advantageous. In such a system, the drawing hardware may be able to update multiple pixels at each memory access. Unfortunately, it is exceptional for multiple pixels to occur in horizontal lines, such that writes could occur parallel to (along) the scan line. Data manipulations of the display involve the equally probable writing of multiple pixels vertically, diagonally, and horizontally to create an image. Most data manipulations involve pixels within an arbitrary region occupying multiple scan lines. Using the scan-line mapping technique, these arbitrary regions will most likely not align with the work boundaries accessed by the graphics controller, thus requiring multiple accesses.

Opting for the symmetrical architecture

One method to reduce the number of accesses necessary to transfer an arbitrary block, and to minimize the access of unnecessary pixels, is to use a symmetrical architecture for the frame buffer memory array. The symmetrical architecture uses one 4-bit shift register per plane rather than the 16-bit shift register of the scan-line approach. It cascades video RAMs by connecting the serial output of one device to the serial input of another to move 1024-column data bits to the 4-bit shift register. As in the scan-line method, an array-to-shift register transfer occurs once each four scan lines, but the data is now shifted out of the video RAMs at 22 MHz. The mapping to the screen shows that when the system processor operates on the frame buffer, it accesses a 4 x 4 block of pixels. The manipulation of an arbitrary memory image will generally require fewer accesses, since the number of pixels operated on by the system processor will be maximized (included unnecessary pixels will be minimized).

Table 2 compares the maximum number of accesses required to read or write variously sized, arbitrarily located regions using the implementations described. For the smaller regions, symmetrical mapping yields the greatest improvement in required accesses. The pixels of no interest occur at the boundary edge of the region. In addition, accesses internal to a large region do not contain any unnecessary pixels.

The symmetrical mapping architecture causes the scan-line data to correspond to the 256 columns within the same row of four memory devices. Each device corresponds to every fourth pixel in the scan

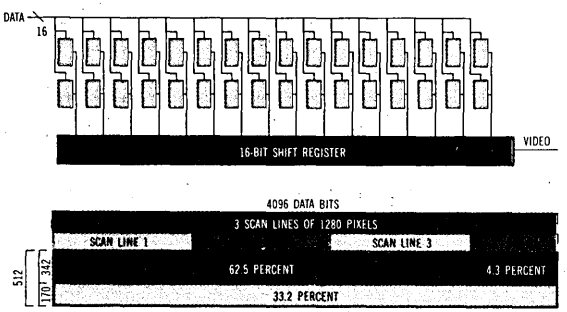

Fig 6 The video RAM organization offers the consolidation of memory, made possible by unified text and graphics design.

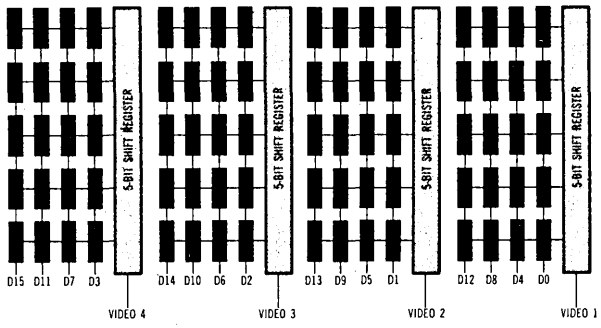

Fig 7 This frame buffer design provides four planes of display memory accessible to a 16-bit processor using 80 video RAMs.

line. A 16-bit processor can directly access the memory array for image manipulation, using the appropriate addressing arrangement. The system processor can directly issue the address of the row and column for the desired pixel. The decoding of the active chip may be done in hardware or as an internal operation of the processor.

To implement a 1280 x 1024 display (which is becoming somewhat standard), twenty 64-Kbit memory devices are required. There are apparent problems, however, with the use of a 16-bit processor with 20 memory devices. A bit-slice processor with 20 data bits could be used, but may not be practical for many systems. If a 16-bit processor is used, either the processor will access some or all of the memory as partial words (eg, 5 banks of 4 bits, or 1 bank of 16 bits and 1 bank of 4 bits), or extra memory is designated for use in video access. The use of partial words is possible. However, the added calculations to determine bit positions and increased number of accesses needed to update the display will cause some system performance degradation. This can be avoided by adding memory to fill out the data bus to a multiple of the processor width. This memory will not be wasted, since graphics systems typically require large regions of scratchpad memory to be used by the processors for placing text fonts, display lists, and for use in the calculations of drawing the displayed images.

Since more memory is required, the use of 32 video RAMs can simplify the task of matching the memory width to the processor width. If the memory is organized as shown in Fig 6, the transfer from array to shift register would place 4096 bits into the on-chip shift register. The data for 3 scan lines can be taken from these 4096 bits, leaving 256 unused bits. The display will use a total of 175,104 bytes (163,840 displayed and 11,264 left at the end of the rows) of the 262,144 bytes in the RAM. This noncontiguous memory amounts to about 4.3 percent of the total memory. The remaining 87,040 bytes consolidated within the second bank of video RAMs are available for use as system memory or scratchpad memory.

Lookup table eases calculations

To make the task of calculating the starting address of each scan line easier, a 1024-word table (2048 bytes), is set aside as a lookup table. Using a table to point to the start of the memory to be used for display allows rapid changes in portions of the screen image while not affecting other areas. When the same memory can be used for either display or system memory, the cost effectiveness and flexibility of the system is improved. The unified text and graphics design approach allows memory consolidation, especially in those systems where nonpower-of-two displays are used.

Fig 7 shows a possible implementation of a 1280 x 1024 frame buffer to provide four planes of display memory accessible to a 16-bit processor using 80 RAMs. The processor will access all four planes of data for each of four pixels, from what it considers as five banks of 16 memories. The data for display within each of the planes appears as four banks of five devices so that the array to shift register transfer will load four scan lines of data. The difference in this organization is the relative position of the four pixels accessed by the processor. The mapping separates the four pixels accessed by 1280 pixels into a vertical line. Depending on the address scrambling, the processor could map the memory sequentially in vertical rows rather than horizontal lines. The 5-bit shift registers allow the video dot rate to go up to 125 MHz before the data capacity of the RAMs is exceeded.

A 256K DRAM Organized for Applications Solutions

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ABSTRACT

The need for high density dynamic random access memory (DRAM) will continue to increase with the increased requirements of applications software. A 256K DRAM which combines increased memory density and high performance to satisfy more sophisticated applications is described. The 256K DRAM has been organized to provide for both a 256K × 1 and a 64K × 4 architecture. System requirements will dictate which architecture is more effective in satisfying an application. In addition, the refresh scheme and device pinouts allow the 256K DRAM family to be the first truly upwards compatible generation of 5 volt DRAMs. A technique where memory system upgrade can be accomplished in modular increments is demonstrated.

INTRODUCTION

As applications software becomes more sophisticated, the need for high density dynamic random access memory (DRAM) will continue to increase. On the average, system memory size will increase three to four fold requiring larger boards, additional boards, sophisticated packaging techniques, or denser memory. Figure 1 is a projection of the average increase in dynamic memory per system that will be necessary to accommodate more sophisticated applications programs over the next five years. Coincident with the increased memory requirements, however, is the introduction of the next generation DRAM, the 256K. These latest generation devices will provide four times the amount of memory in the same board area as with 64K DRAM's. In addition, more device features will provide the flexibility to maximize utilization of 256K DRAMs in specific applications. This paper will describe a 256K DRAM, its technology and architecture, and how it simplifies the needs of expanding applications.

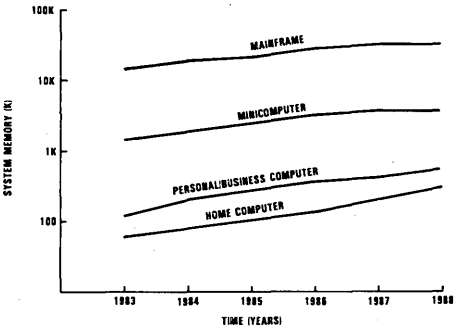

Figure 1. Projected DRAM Memory Increase Per System

FEATURES AND CHARACTERISTICS

The development of the 256K DRAM required new process technology [1] in addition to further scaling of the SMOS (Note 1) process.

With the announcement of the 256K DRAM's, it is apparent that the choice of architecture, silicide material, number of polysilicon/metal levels, and design techniques are numerous [2,3]. The TMS4256, 256K × 1 DRAM, is fabricated with a single metal, double level polysilicon (Note 2) process for performance and simplicity. The features of the technology are listed in Table I.

NOTES: 1. SMOS, scaled NMOS, is the proven technology of the TMS4164, 64K DRAM
2. Polysilicon and polysilicon/silicide

Table I. Technology Features

Bit Line	Aluminum
Word Line	Polycide
Tox (Periphery)	400 Angstrom
Tox (Cell)	200 Angstrom
Cell Capacitance	50 fF
C (bit line)/C (Cell)	8
Redundancy	Laser
Technology	Double Poly*
Design Rule	2 Micron
Metal Width (Min)	2 Micron
Chip Size	4.6mm × 8.7mm

*Polysilicon/polycide

Folded metal bit lines and polycide word lines provide an optimum signal for sensing and high speed performance. This signal is a result of low bit line capacitance and minimum word line delay. The double polysilicon approach required only the addition of a polycide process to an already proven technology.

The dimensions of the chip are 4.6 mm × 8.7 mm and can easily fit into a 300 mil plastic package. Over 72% of the die area is devoted to the memory array and decode circuitry as is illustrated by Figure 2, the chip photograph.

Four redundant columns and four redundant rows (Note 3) have been included to maximize yield in the early stages of production. Laser blowing of polycide fuses accomplishes the task of removing the defective row(s) or column(s) and replacing them with the proper redundant row(s) or column(s). Repaired memory has been characterized and no performance or reliability degradation was observed.

Typical speed and power characteristics are shown in Table II. The typical power dissipation at 3.8 MHz operation is 250 mW while in standby mode it is only 12.5 mW. Typical access speeds from row address strobe ($\overline{RAS}$) of 105 ns have been measured.

Table II. Typical Characteristics

Organization	256K × 1. 64K × 4
T (RAC)	105 ns T (RCD) = 25 ns
T (CAC)	62 ns
I_{DD} (operating)	50 mA T (RC) = 260 ns
I_{DD} (standby)	2.5 mA
Refresh	256 cycle, 4 ms
Package	16 Pin, 18 Pin 300 mil
Nibble Sequence	(0,0)→(0,1)→(1,0)→(1,1)
ESD	>2 kV*

*MIL-STD-883B. Method 3015

NOTE: 3. Physically, eight rows on the chip

The voltage range of operation is shown in Figure 3. The specified supply voltage, V_{DD} is 5 volts ±10%; the actual performance is shown to be from 3.5 volts to greater than 7.0 volts.

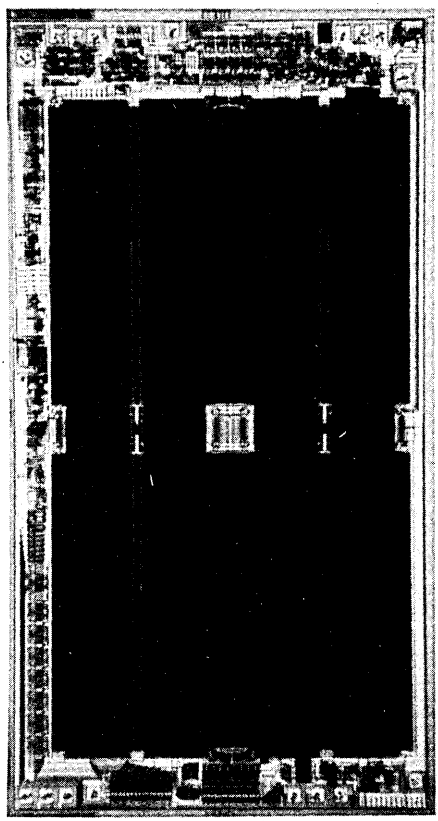

Figure 2. The 256K Chip Photograph

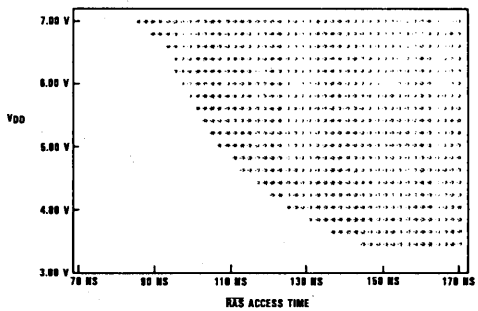

Figure 3. t_{RAC} Versus V_{DD}

ARRAY ARCHITECTURE

The 256K DRAM has been designed to provide optimum flexibility in terms of I/O's for system data bandwidth. The lead established by the 64K DRAM, with both 64K × 1 and 16K × 4 organizations, has been followed by the 256K DRAM. The memory architecture is designed for 256K × 1 and 64K × 4 I/O structures. One step further is the addition of a nibble mode option. Since its introduction [4], nibble mode has become an additional feature on many first generation 256K devices. The 256K offers the flexibility of utilizing either a nibble mode or page mode DRAM.

Furthermore, the memory array of the 256K DRAM is compatible with the following options:

1. 256K × 1 (TMS4256, Page Mode)
2. 256K × 1 (TMS4257, Nibble Mode)
3. 64K × 4 (TMS4464, Page Mode)

The functional block diagram of the 256K × 1 and 64K × 4 are shown in Figures 4 and 5. By examining these figures, two significant differences in the block diagrams are noted. First, on the 256K × 1 (Figure 4) the most significant address A8 performs a one of four selection to provide a single output. This address is not required for the 64K × 4 device as all four data bits are required, one for each DQ pin (Figure 5). Second, an additional control signal, $\overline{G}$ or output enable, is available on the 64K × 4 to provide additional HI-Z/enable flexibility on the DQ pins.

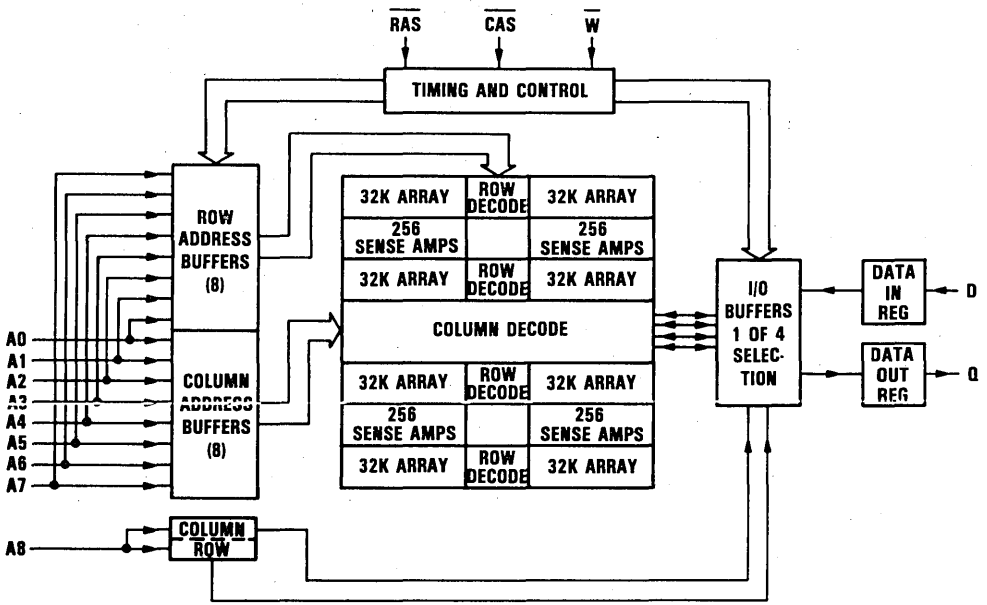

Figure 4. 256K × 1 Block Diagram

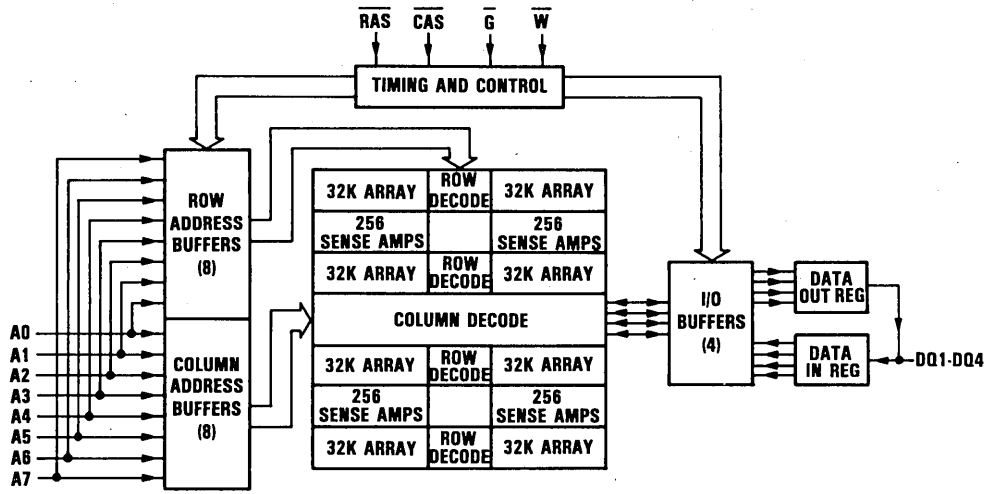

Figure 5. 64K × 4 Block Diagram

The unique array architecture can be appreciated by looking one level deeper into the functional diagram. Figure 6 illustrates how one memory array access generates four data bits internally. Essentially, the X-word lines for the top and bottom array are selected simultaneously (effectively one word line). One Y-decoder will select four sense amplifiers; as a result, four memory cells are accessed. The four bits can be: 1. decoded by RA8 and CA8 for the TMS4256; 2. shifted from the four intermediate output buffers using an A8 (AY8, AX8) sequence nibble operation for the TMS4257 (see Table II); or 3. loaded to four DQ buffers for the TMS4464.

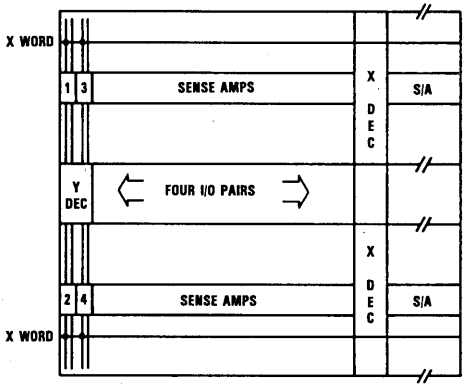

Figure 6. Functional Diagram

The array architecture also maintains the 256 cycle, four millisecond refresh that was standardized on the TMS4164 and TMS4416. This was accomplished by organizing the array as 256 rows and 1024 columns in four 64K blocks.

INCREASED REFRESH FLEXIBILITY

In addition to conventional refresh methods, the 256K DRAM family has been designed with expanded capabilities. Refreshing the device can be accomplished with any of the following techniques:

1. Normal Read/Write operation,
2. $\overline{\text{RAS}}$-only-refresh cycle,
3. $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycle (CBR), and
4. Hidden refresh cycle.

The 256K design includes an internal refresh address counter. This counter provides the row address to be refreshed in a CBR or Hidden refresh cycle. With this feature, an external refresh address does not have to be supplied by the user. The memory system design simplification is illustrated in Figures 7 and 8. Note that both an external refresh address counter and multiplexer have been eliminated with the utilization of $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh.

The timing diagrams for the various refresh cycles are shown in Figure 9. It is significant to observe from the timing diagrams that the address is in a "don't care" state during the $\overline{\text{RAS}}$ negative transition for the CBR or hidden refresh cycles.

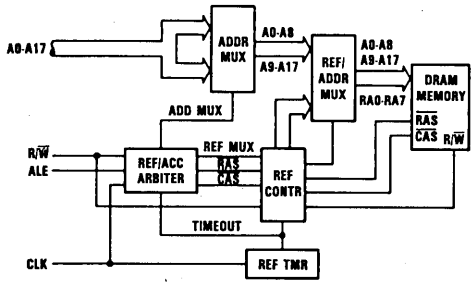

Figure 7. $\overline{RAS}$-Only Refresh Implementation

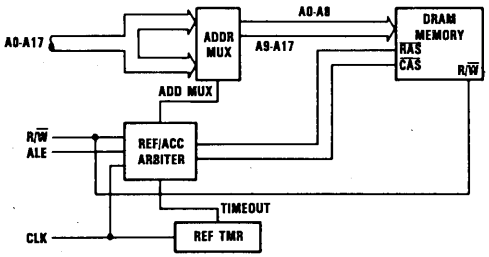

Figure 8. $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Implementation

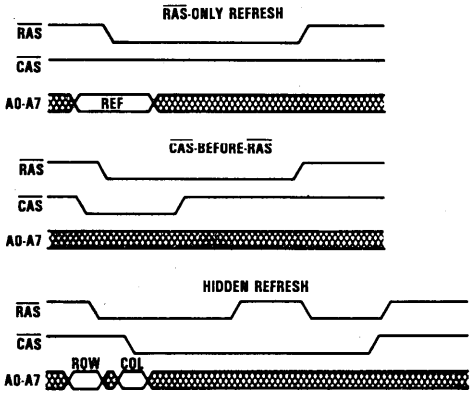

Figure 9. Refresh Cycle Alternatives

GENERATION TO GENERATION COMPATIBILITY

The pinout of the 256K × 1 and 64K × 1 devices (Figure 10) illustrates the pin-for-pin compatibility with the exception of pin 1 on the 256K × 1. This is designated as the ninth address pin since 18 addresses are necessary to decode one of 256K memory locations. From the board layout perspective, only an additional trace will be necessary to accommodate the ninth address pin. However, an additional multiplexer (2 to 1 MUX) is necessary since typically they are available in 4-bit increments only. If an external DRAM controller chip is to be utilized, a provision for the additional addressing bit may already be accommodated. The same refreshing scheme as used by the TMS4164, 64K × 1, generation devices will also be used by 256K × 1 devices; specifically, 256 cycles in a 4 ms period. The additional address pin is simply ignored by the refresh address generation circuitry when refresh occurs.

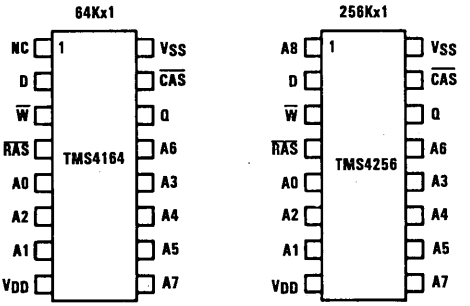

Figure 10. × 1 DRAM Pinouts

The 16K × 4 (TMS4416) and 64K × 4 (TMS4464) generation devices are the first entirely pin-for-pin compatible dynamic RAM generations (Figure 11). A system designed for TMS4416 devices will be able to immediately utilize a TMS4464 device. The main adaptation will be in the memory map circuitry where there is suddenly four times the available amount of memory. The TMS4416 devices employ an 8-row address, 6-column address decoding matrix to yield four bits from 65,536 possible memory locations. This decoding scheme provided the four bits all from the same row since the eight row address bits decode 1 of 256 rows, and the six column address bits decode 4 of 256 columns. Despite only 6 column bits being necessary, the trace layout included the eight address lines for row address decoding requirements. The 64K × 4 was designed to comprehend an

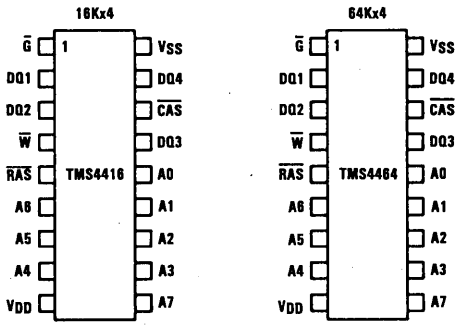

Figure 11. ×4 DRAM Pinouts

8 row address, 8 column address decoding matrix in order to maintain compatibility with the previous generation. Since the architecture is arranged as 256 rows by 1024 columns, all four data bits are selected on the same row. Eight traces have already been incorporated in the layout so no changes will be necessary for the TMS4464 board layout.

The generation-to-generation compatibility offers the ability to simply replace new generation devices for older generation devices with the appropriate board layout; thus, memory expansion can be taken advantage of with a minimum of board re-configuration. With the right support circuitry as illustrated by Figure 12, the memory size can be increased in a modular fashion to correspond with increased memory requirements from software. A TMS4416 to TMS4464 conversion system is a good example. Memory mapping for a TMS4164 to TMS4256 conversion system would be very similar except for the provision for a ninth address line. Consider an application that calls for a 16K word minimum memory requirement to be increased by minimal steps until a full 256K words are available by virtue of a fully populated 64K ×4 DRAM system (Figure 13.). This allows the user to increase memory to align it with his expanding software requirements without an immediate four-fold memory increase. In addition, devices will replace parts already existing on the board; so it is not necessary to purchase complete memory expansion boards. A 64K-word system will require 16 TMS4416 DRAM's arranged as four banks with four devices in each bank. Four TMS4416 DRAM's will provide the required word width.

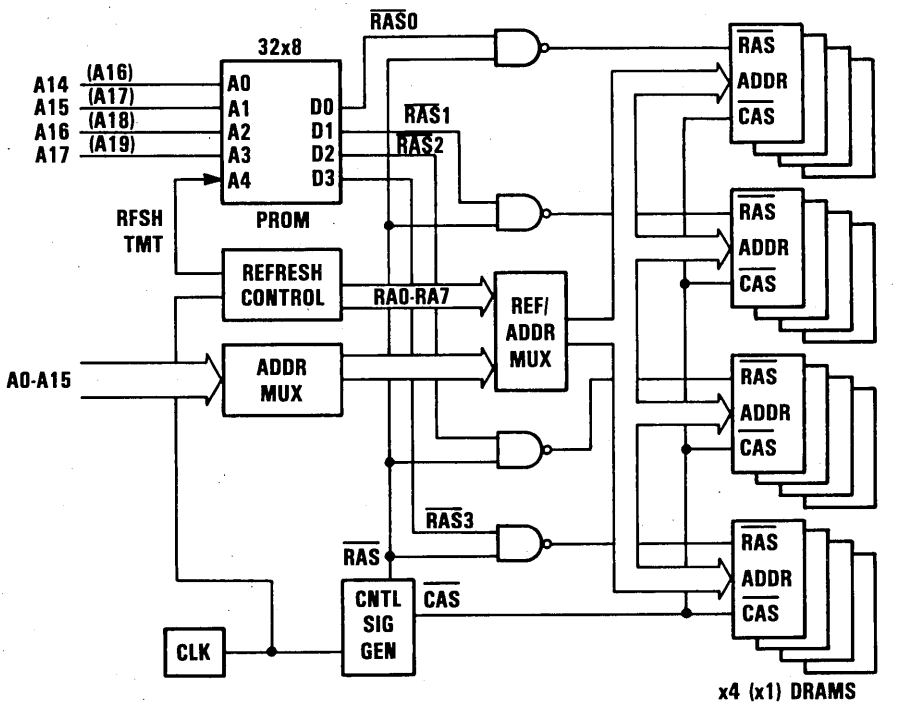

Figure 12. Memory Board Block Diagram

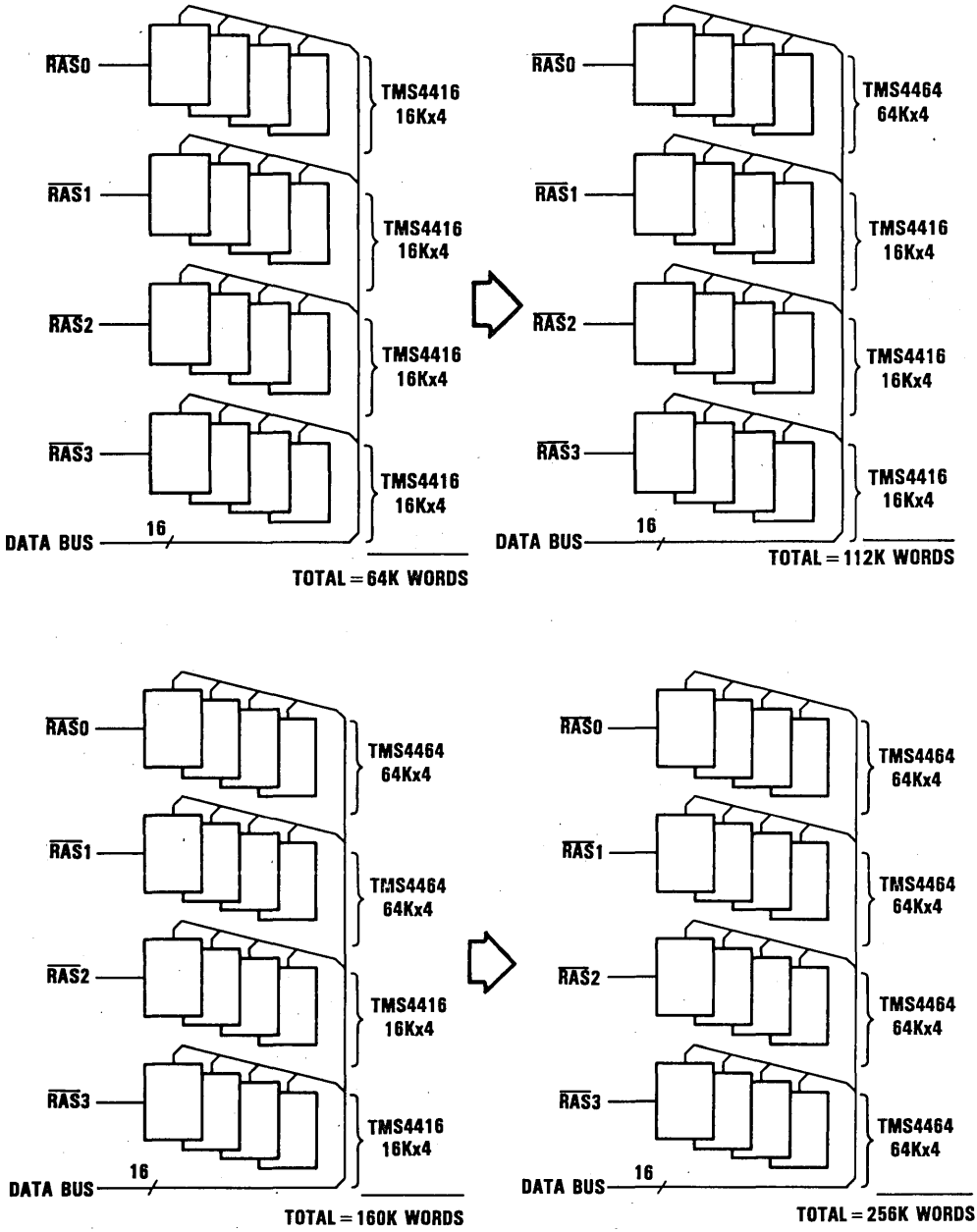

Figure 13. TMS4416 to TMS4464 Memory Expansion

The added consideration with this type of memory arrangement is mapping the memory from the onset to comprehend the memory increase. This can be accomplished by using addresses A14 to A17 to decode a 32 × 8 PROM to yield the four $\overline{RAS}$ bank select signals. Each × 8 location of the PROM (actually only four of the eight bits are used) corresponds to a 16K-word memory block. Table III is a truth table which indicates the decoding scheme for the four $\overline{RAS}$ bank selects. In the initial system of up to 64K words, memory will correspond to the first four memory locations (16K × 4 = 64K). As additional memory is added to the system, each additional 16K block of memory will correspond to subsequent PROM memory locations. Note that the addition of memory can happen in increments of one bank at a time (four devices). A fully populated TMS4464 DRAM system will absorb 16 out of the total 32 PROM memory locations. Thus the most significant PROM address bit, A4, is used as a refresh decode. All PROM memory locations (16, total) which correspond to A4 high activate all four $\overline{RAS}$ bank select signals. This allows refresh to occur on the current selected row for all system DRAM memory simultaneously. Remember that a TMS4464 DRAM has the same 256-cycle refresh scheme as a TMS4416 DRAM so a combination system will have no refresh constraints.

A TMS4256 conversion system (Figure 14) from a TMS4164 system will be very similar except that memory will be mapped in 64K-word blocks and would increase from a minimum of 64K-words to a maximum of 1M-words (a fully populated 256K DRAM system).

ORGANIZATION TRADEOFF

The previous compatibility examples illustrate significant differences in the implementation of either a × 1 or × 4 organized DRAM for a particular application. A complete evaluation of the system needs is necessary in order to decide on which organization DRAM to utilize. There are basically three categories to examine when evaluating your system:

1. Memory size requirements,
2. Memory speed requirements, and
3. Expandability requirements of the system.

Table III. PROM Truth Table

	PROM ADDRESSES					OUTPUTS								SELECTED BANK
$\overline{CS}$	A4	A3	A2	A1	A0	Q8	Q7	Q6	Q5	$\overline{RAS3}$ Q4	$\overline{RAS2}$ Q3	$\overline{RAS1}$ Q2	$\overline{RAS0}$ Q1	OF MEMORY
0	0	0	0	0	0	0	0	0	0	0	0	0	1	Bank 0
0	0	0	0	0	1	0	0	0	0	0	0	1	0	1
0	0	0	0	1	0	0	0	0	0	0	1	0	0	2
0	0	0	0	1	1	0	0	0	0	1	0	0	0	3
0	0	0	1	0	0	0	0	0	0	0	0	0	1	Bank 0
0	0	0	1	0	1	0	0	0	0	0	0	0	1	0
0	0	0	1	1	0	0	0	0	0	0	0	0	1	0
0	0	0	1	1	1	0	0	0	0	0	0	1	0	Bank 1
0	0	1	0	0	0	0	0	0	0	0	0	1	0	1
0	0	1	0	0	1	0	0	0	0	0	0	1	0	1
0	0	1	0	1	0	0	0	0	0	0	1	0	0	Bank 2
0	0	1	0	1	1	0	0	0	0	0	1	0	0	2
0	0	1	1	0	0	0	0	0	0	0	1	0	0	2
0	0	1	1	0	1	0	0	0	0	1	0	0	0	3
0	0	1	1	1	0	0	0	0	0	1	0	0	0	3
0	0	1	1	1	1	0	0	0	0	1	0	0	0	Bank 3
0	1	X	X	X	X	0	0	0	0	1	1	1	1	Refresh All Banks

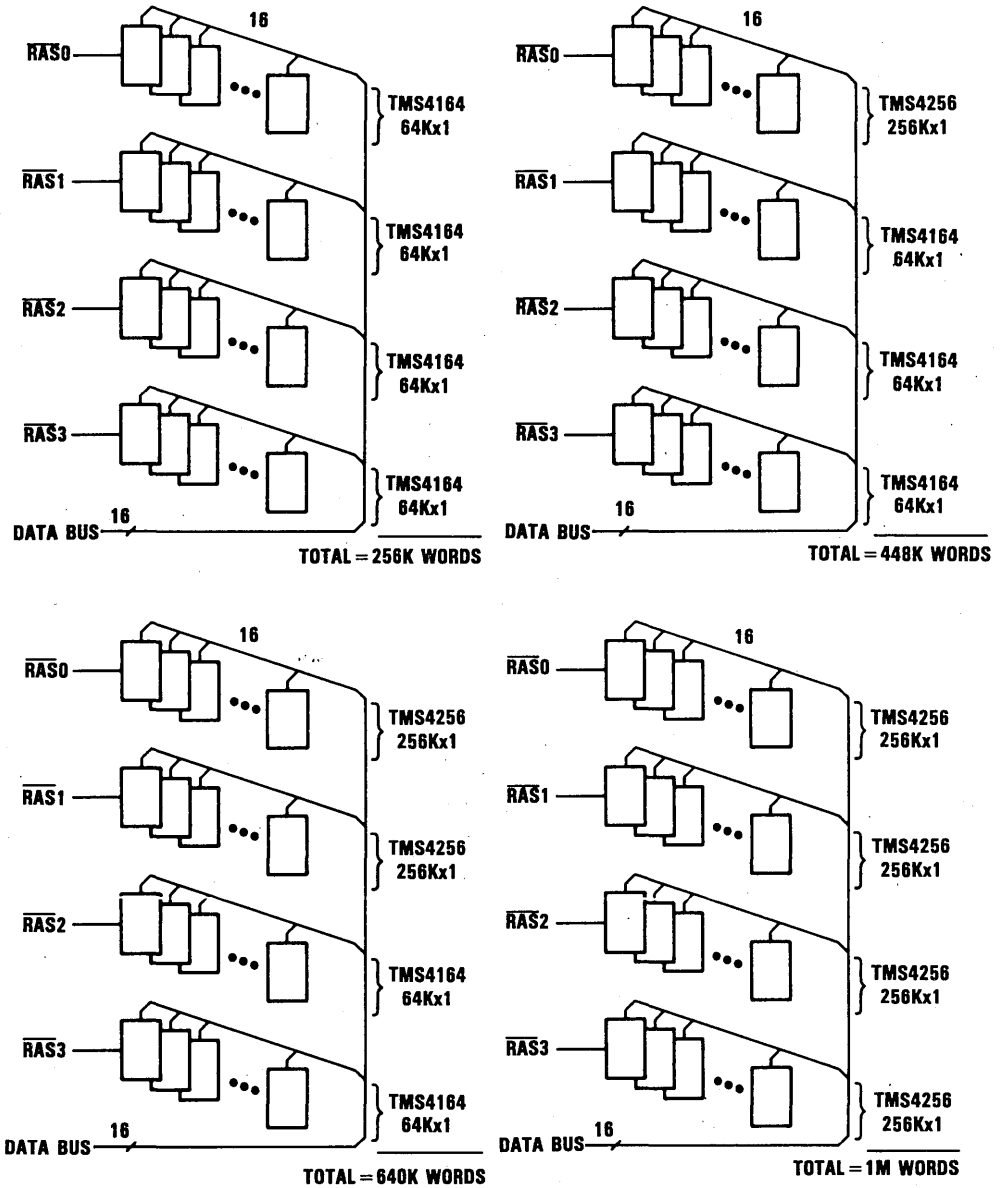

Figure 14. TMS4164 to TMS4256 Memory Expansion

Memory Size Requirements

The memory size needed to satisfy an application would be the first factor to evaluate in the consideration of either ×1 or a ×4 system implementation. A general rule to apply is to utilize the ×4 organization for memory requirements up to the ×1 memory size, or if N > 1, where N = ×1 memory size/memory needed. In the case of 256K DRAMs, for memory less than 256K (bytes, words, etc.) it would be advantageous to utilize 64K ×4 devices. Figures 15 and 16 show a comparison of a system which uses ×1 DRAMs and ×4 DRAMs, respectively, to provide 256K bytes. The same number of memory devices are utilized in each case, but the ×1 device takes up somewhat less space because of the 16-pin package over the 18-pin package of the ×4 device.

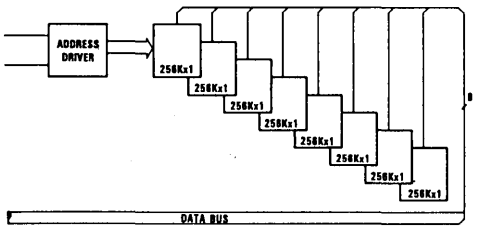

Figure 15. 256K Memory System Size (256K × 1 Implementation)

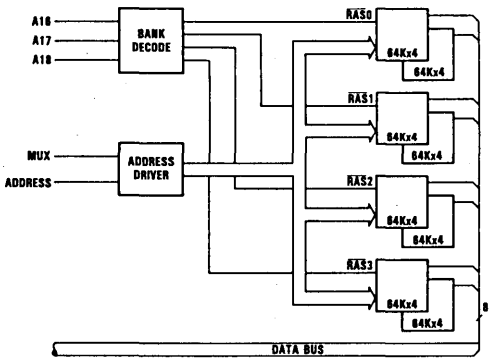

Figure 16. 256K Memory System Size (64K × 4 Implementation)

In addition, proper decoding circuitry will be necessary to decode one of the four memory banks of the ×4 implementation. The power savings of enabling only one bank at a time for a memory access will be offset by the power usage of the additional drive and decoding circuitry. The additional circuitry will also take up more board space, and require more signal routing to implement. A listing of relevant parameters is available in Table IV for both a ×1 and ×4 implementation of a 256K-byte system. Up to the 256K byte level, though, the bandwidth advantage of the ×4 devices allows better memory utilization and power savings by enabling one bank of DRAMs during any single memory access. Table V is a comparison of the same parameters for a TMS4464 and TMS4164 implementation of a 128K-byte system. The part count and board area savings of the TMS4464 implemented system is highlighted in Figures 17 and 18.

Table IV. 256K-Byte System

PARAMETERS	256K×1 DRAM	64K×4 DRAM
Component Count*	9	10
Board Area	3.34 sq."	4.0 sq."
Power	620 mA	375 mA

*Includes Support Circuitry

Table V. 128K-Byte System

PARAMETERS	64K×1 DRAM	64K×4 DRAM
Component Count*	18	6
Board Area	4.89 sq."	2.4 sq."
Power	590 mA	374 mA

*Includes Support Circuitry

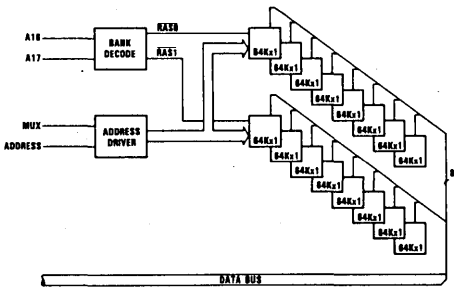

Figure 17. 128K Memory System Size (64K × 1 Implementation)

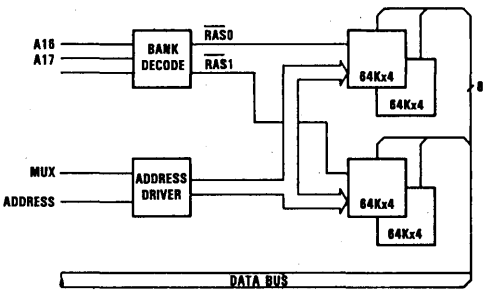

Figure 18. 128K Memory System Size (64K × 4 Implementation)

Memory Speed Requirement

The speed required to satisfy specifications for an application is another factor to consider when evaluating the use of ×1 or ×4 organized DRAMs. The minimum cycle time for a 150 ns dynamic RAM is 260 ns. With system decoding and buffer delays within the system, the realistic cycle time will be increased to 300 ns. Memory access becomes critical when the application demands a high performance microprocessor or bit slice controller. High performance microprocessor memory access periods are now reduced to under 200 ns in some cases, while a bit slice memory access period is under 100 ns. Direct interface of ×1 DRAMs would cause the fast processors to execute wait states while waiting for the memory. The example in Figure 19 shows a method in which the utilization of a ×4 device will decrease the average access time of each bit by a factor of up to four. The two least significant addresses decode one of the four latches which provide four times the data bus width worth of data. The processor will have to access the latches four times as often, as memory must be accessed to load the latches. The data from the first latch will be accessed in the normal DRAM access period (300 ns) as all four data latches will be filled. With a typical processor memory access period of 75 ns assumed, subsequent processor memory accesses will access memory from the other three latches allowing for memory access without wait states. This translates to an average cycle time of [300 ns+3*(75 ns)]/4 processor memory accesses or 131 ns. Since most processor instructions occur sequentially over short intervals and require multiple memory operations, the average memory access will be based upon enhanced access time. This compares with the previous average memory cycle time of 300 ns where the processor will be forced to wait for every memory access. Even further enhancement of apparent memory access time can be achieved in systems that allow memory access overlap or pipelined instruction execution. Such a system would have an apparent memory access time approaching 75 ns (or the cycle time of the processor). Obviously, memory speed and memory size are very interrelated when considering this trade-off.

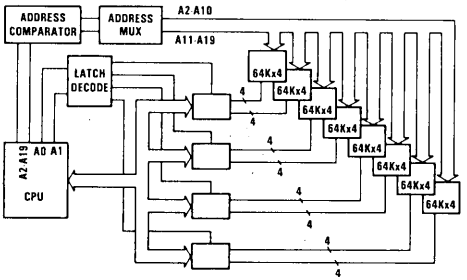

Figure 19. 64K × 4 Implemented System Performance Increase

Expandability

The expandability of a system can be sub-divided into two aspects: maximum memory size, and minimum memory increments. The compatibility examples are good illustrations of the granularity advantage of the ×4 devices over the ×1 devices where granularity is a measure of the smallest increment in which memory size can be increased. The increase of total memory size with the modular implementation of 64K ×4 DRAM's was only in 48K-byte increments; whereas the 256K × 1 system increased in units of 192K-bytes. By the same token, the maximum attainable memory size for the ×4 system will be 256K-words, whereas the ×1 system can be expanded to a maximum of 1M-words (if maintaining the same level of bank decode logic).

SYSTEM REFRESH CONSIDERATIONS

The use of dynamic RAMs in a system carries with it the responsibility of refreshing the DRAMs at regular intervals. Several refresh alternatives provide the designer the opportunity to adapt a particular refresh scheme to a particular application. The type of refresh to be implemented in a system depends directly on the type and speed of the processor being utilized, since these factors determine the length of time before memory access may be required. Typically in a memory sub-system design, refresh should be as transparent to the system operation as possible. This serves to reduce the interruption of processor access cycles to a minimum and thereby increase the performance of the system. For slow processors, hidden refresh provides the capability to complete a refresh cycle within a processor memory access cycle by latching the accessed data while the refresh is completed. As a result, separate hardware will provide for refresh cycle implementation, eliminating refresh responsibility from the processor. It is interesting to correlate refresh timing requirements of the DRAM memory with the memory access requirements of the processor. The refresh cycle time for a 150 ns DRAM is 260 ns. Hidden refresh implementation in a slow processor system allows enough time to complete both a memory access and a refresh cycle (Figure 20). There will be no affect on processor operation performance due to refresh requirements of the system. In a medium performance processor system, the period of time provided for memory access becomes critical when a refresh must occur. Wait cycles may have to be implemented during a processor memory access which occurs during a refresh cycle to accommodate the additional time that the refresh cycle adds to the memory access cycle. In a high performance system, the memory access cycle will cause the processor to be delayed to allow completion of the memory access. A refresh cycle will cause additional delay to be added to the memory access time. In systems with a processor that gives an indication that it will not be utilizing the memory, a refresh cycle may be inserted to eliminate the degradation of processor throughput because of refresh.

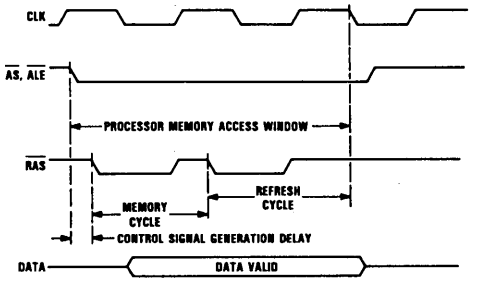

Figure 20. Slow Processor Transparent Refresh

SUMMARY

Design and process technology advances combine to allow the manufacture of a 256K DRAM that is upwards compatible with previous generation 64K DRAMs. The memory array architecture is adaptable to both 256K × 1 and 64K × 4 organizations. Device performance is improved due to the use of polycide film, thin gate dielectric insulator, and folded metal bit lines.

Generation-to-generation compatibility provides additional memory for new applications or reduced component count for present applications. Furthermore, the TMS4416 and TMS4464 are pin-for-pin compatible and require no hardware modifications to upgrade.

Refresh requirements are identical between generations of × 1 and × 4 DRAMs. The 256K DRAM is available with an internal refresh address counter to accommodate hidden and $\overline{CAS}$ before $\overline{RAS}$ refresh schemes.

The performance and flexibility of the 256K DRAM family will meet the increasing system memory requirements without increasing system complexity. As a result, more sophisticated software can be accommodated.

ACKNOWLEDGEMENTS

The authors wish to thank David Gulley for his ideas and directions in the development of this paper. In addition, they would like to thank Frank Miu, and the 256K Design Team for their contributions.

REFERENCES

[1] M. Smayling, M. Maekawa. "256K dynamic RAM is more than just an upgrade", Electronics, Vol. 56, no. 17, pp. 135-137, Aug. 25, 1983.

[2] T. Fujii et al., "A 90 ns 256K × 1 bit DRAM with Double-level Al Technology". IEEE J. Solid State Circuits, Vol SC-18, no. 5, pp. 437-440, Oct. 1983.

[3] T. Nakano et al., "A sub-100 ns 256K DRAM with open bit line scheme", IEEE J. Solid-State Circuits, Vol, SC-18, no. 5, pp. 452-456, Oct. 1983.

[4] S.S. Eaton, et al., "A 100 ns 64K dynamic RAM using redundancy techniques". Dig. Tech. Papers, ISSCC, 1981, pp. 84-85.

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EXPLANATION OF IEEE/IEC LOGIC SYMBOLS FOR MEMORIES

1. INTRODUCTION

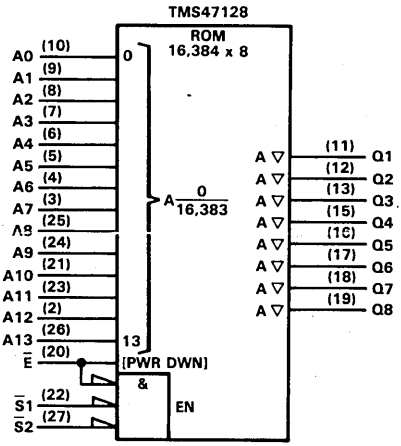
The International Electrotechnical Commission (IEC) has been developing a very powerful symbolic language that can show the relationship of each input of a digital logic circuit to each output without showing explicitly the internal logic. At the heart of the system is dependency notation, which will be partially explained below.

The system was introduced in the USA in a rudimentary form in IEEE/ANSI Standard Y32.14-1973. Lacking at that time a complete development of dependency notation, it offered little more than a substitution of rectangular shapes for the familiar distinctive shapes for representing the basic functions of AND, OR, negation, etc. This is no longer the case.

The current standards are IEC Publication 617-12, 1983, and ANSI/IEEE Standard 91-1984. Most of the data sheets in this data book include symbols prepared in accordance with these standards. The explanation that follows is necessarily brief and greatly condensed from the explanation given in the standards. This is not intended to be sufficient for those people who will be developing symbols for new devices. It is primarily intended to make possible the understanding of the symbols used in this book.

2. EXPLANATION OF A TYPICAL SYMBOL FOR A STATIC MEMORY

The TMS47128 symbol will be explained in detail. This symbol includes almost all the features found in the ROMs, PROMs, and EPROMS.



The address inputs are arranged in the order of their assigned binary weights and the range of addresses are shown as $A\frac{m}{n}$ where m is the decimal equivalent of the lowest address and n is the highest. The outputs affected by these addresses are designated by the letter A, as data inputs would also be if the device were a RAM.

The polarity indicator ▷ indicates that the external low level causes the internal 1-state (the active or asserted state) at an input or that the internal 1-state causes the external low level at an output. The effect is similar to specifying positive logic and using the negation symbol ○ .

The ▽ symbols indicate three-state outputs. Three-state outputs will always be controlled by an EN function. When EN stands at its internal 1-state, the outputs are enabled; when EN stands at its internal 0-state, the outputs stand at their high-impedance states. Sometimes the EN is a single input but in the illustrated case, it is the output of a three-input AND gate. All three inputs (pins 20, 22, and 27) are active low so if any one of them goes high, the outputs will be disabled. The upper one of these three inputs (pin 20) has another function. When nonstandard labels and explanatory labels are used within symbols, they are enclosed within square brackets. Here we find the label "[PWR DWN]". This is intended to indicate that if pin 20 is high, the memory will go to a low-power standby state.

3. THE BASICS

Section 3.1 illustrates the most common building blocks that are used in constructing symbols for memories. On the left are shown the symbols that specify the active levels for level-operated inputs, and the direction of active transition for dynamic inputs.

It is preferred to show all input lines on the left and all output lines on the right. When an exception is made to this left-to-right signal flow, an arrowhead is used to show the reverse signal flow.

Three symbols are shown that indicate 3-state, open-drain, and open-source outputs. If none of these are used, the output should be assumed to be totem-pole. The common control block is a point of placement for inputs that affect an array of elements.

The drawings on the right define the three forms of *dependency notation* used in this book. At an input (or output) that affects other inputs or outputs, a letter (G, C, or Z) is placed followed by a number. That same number is placed at the affected inputs and outputs. The letter G indicates that an AND relationship exists; if the affecting input stands at the 0-state, it imposes that 0-state on the affected input or output. The letter C indicates a control relationship, usually between a clock and a D (data) input. If the C input stands at its 0-state, the affected input is disabled. A D input is always an input to a storage element, which it either sets to the 1-state or resets to the 0-state, unless the D input is disabled to have no effect. Z dependency is used to transfer a signal from one place in a symbol to another, for example from the output at Z4 across to a terminal labeled "4", or from the output at Z5 back to the "5" where it serves as an input with no terminal attached.

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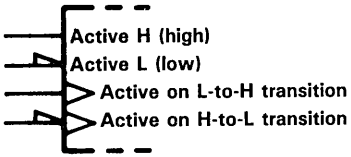
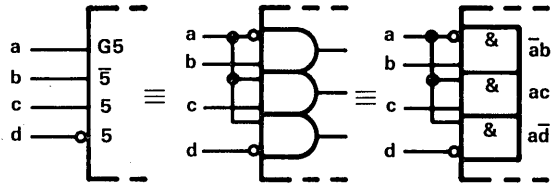
3.1 DIAGRAMATIC SUMMARY

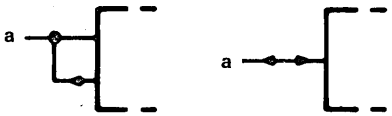
INPUTS



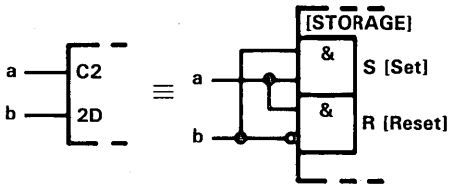
G (AND) DEPENDENCY



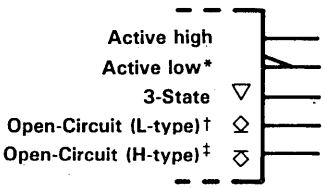
INPUT/OUTPUT



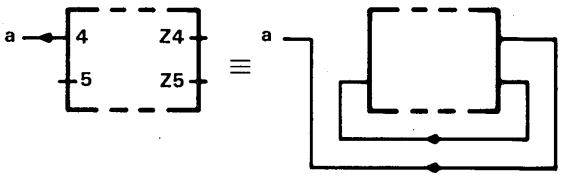
C (CONTROL) DEPENDENCY



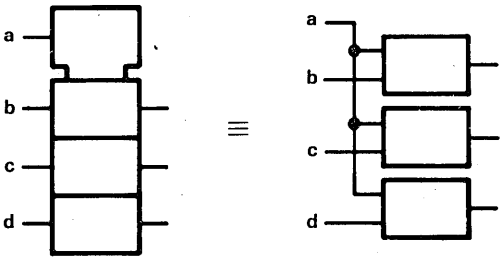
OUTPUTS



Z (INTERCONNECTION) DEPENDENCY



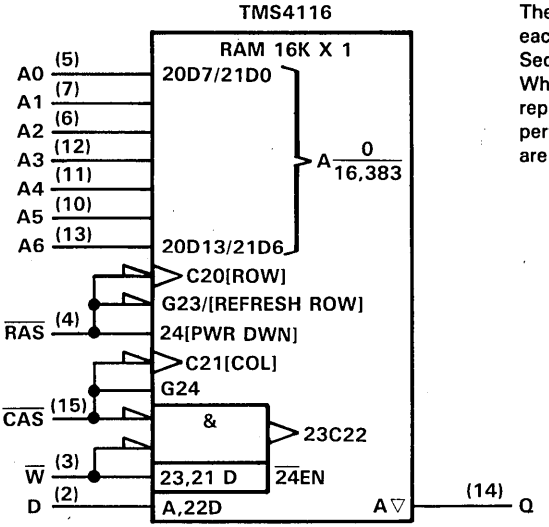
COMMON CONTROL BLOCK



*The active-low indicator may be used in combination with the 3-state and open-circuit indicators.
†L-types include N-channel open-drain and P-channel open-source outputs.
‡H-types include P-channel open-drain and N-channel open-source outputs.

4. EXPLANATION OF A TYPICAL SYMBOL FOR A DYNAMIC MEMORY

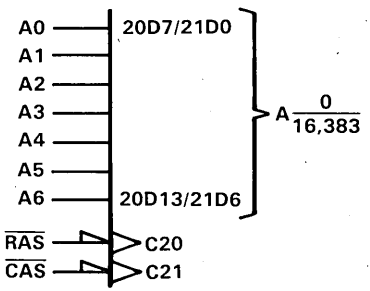
4.1 THE TMS4116 SYMBOL

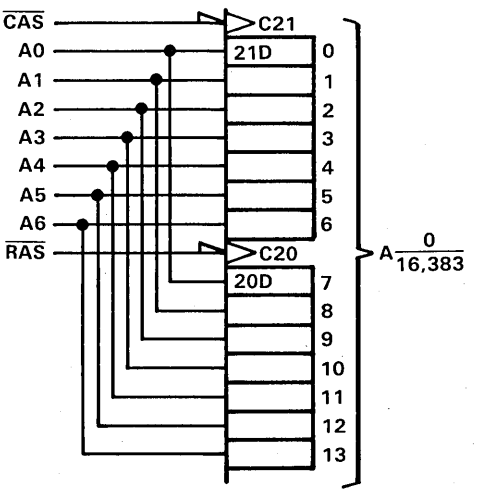


The TMS4116 symbol will be explained in detail for each operating function. The assumption is made that Sections 2 and 3 have been read and understood. While this symbol is complex, so is the device it represents and the symbol shows how the part will perform depending on the sequence in which signals are applied.

4.2 ADDRESSING

The symbol above makes use of an abbreviated form to show the multiplexed, latched addresses. The blocks representing the address latches are implied but not shown.





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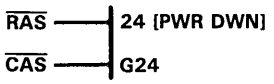
When $\overline{RAS}$ goes low, it momentarily enables (through C20, ▷ indicates a dynamic input) the D inputs of the seven address registers 7 through 13. When $\overline{CAS}$ goes low, it momentarily enables (through C21) the D inputs of the seven address registers 0 through 6. The outputs of the address registers are the 14 internal address lines that select 1 of 16,384 cells.

4.3 REFRESH

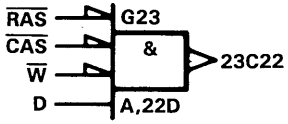
When $\overline{RAS}$ goes low, row refresh starts. It ends when $\overline{RAS}$ goes high. The other input signals required to carry out refreshing are not indicated by the symbol.

4.4 POWER DOWN



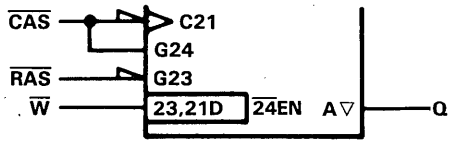
$\overline{CAS}$ is ANDed with $\overline{RAS}$ (through G24) so when $\overline{RAS}$ and $\overline{CAS}$ are both high, the device is powered down.

4.5 WRITE



By virtue of the AND relationship between $\overline{CAS}$ and $\overline{W}$ (explicitly shown), when either one of these inputs goes low with the other one and $\overline{RAS}$ already low ($\overline{RAS}$ is ANDed by G23), the D input is momentarily enabled (through C22). In an "early-write" cycle it is $\overline{W}$ that goes low first; this causes the output to remain off as explained below.

4.6 READ



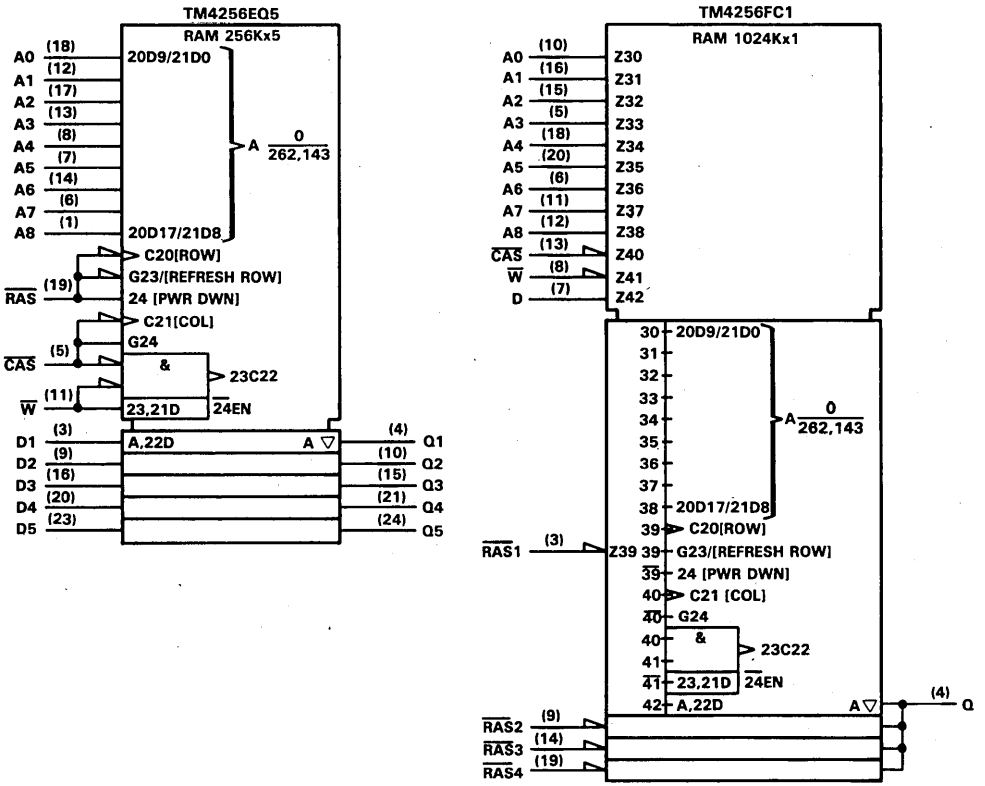
The ANDed result of $\overline{RAS}$ and $\overline{W}$ (produced by G23) is clocked into a latch (through C21) at the instant $\overline{CAS}$ goes low. This result will be a "1" if $\overline{RAS}$ is low and $\overline{W}$ is high. The complement of $\overline{CAS}$ is shown to be ANDed with the output of the latch (by G24 and $\overline{24}$). Therefore, as long as $\overline{CAS}$ stays low, the output is enabled. In the "early-write" cycle referred to above, a "0" was stored in the latch by $\overline{W}$ being low when $\overline{CAS}$ went low, so the output remained disabled.

5. SYMBOLS FOR DYNAMIC RAM MODULES

A dynamic RAM module is created by attaching separate DRAMs in chip-carrier packages to a common substrate. The symbols for the composite memory thus created starts with the symbol for the original DRAM and is used with as little change as possible.

So far, two types of organizations have evolved. In the first, all like address and control inputs are connected in parallel between the separate packages. Taking the TM4256EQ5 as typical of this group, the symbol starts with that of the TMS4256 with the qualifying symbol changed from "RAM 256K x 1" to "RAM 256K x 5", and this becomes a common control block for an array of five input-output elements shown below it.

In the second type of organization, of which the TM4256FC1 is typical, most of the address and control lines are parallel connected, but some are brought out separately for each of the DRAM packages. In order to maintain the recognizability of the original TMS4256 symbol, it has now been placed in the first element of the array. The empty rectangles located below the first element represent three other identical elements. Now interconnection (Z) dependency has been used (see 2 and 2.1) to show how CAS, W, D, and the address inputs connect to the first element, and since these inputs are located in the common control block, the connections apply equally to all the elements. The connections for $\overline{RAS}1$, $\overline{RAS}2$, $\overline{RAS}3$, and $\overline{RAS}4$ apply only to the individual elements.



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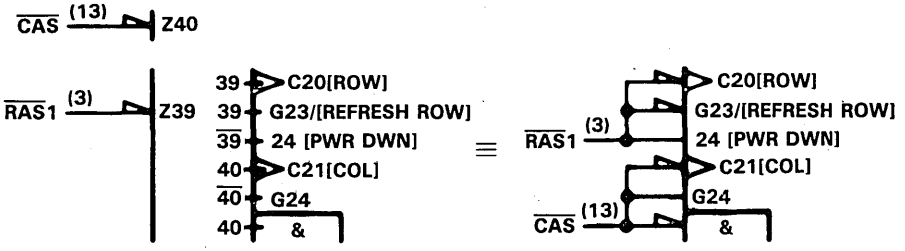
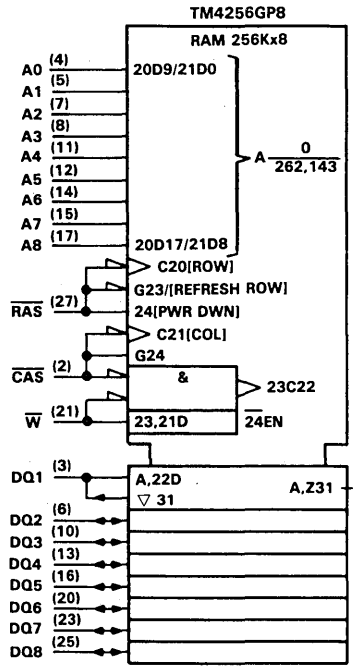
The drawings below illustrate the handling of control lines that in the original symbol were broken up into active-high and active-low functions. To make the combined symbol, the one of the two levels that seemed most appropriate was chosen, and then bars were used over the dependency numbers if necessary. For example, PWR DWN is an active-high function of pin 3, but it was decided that pin 3, $\overline{RAS}$, should be considered active low. The bar over the number 39 indicates that PWR DWN is a function of the *complement* of Z39 (ANDed with the complement of Z40 through G24), and the complement of active low is active high.



Another modification of the basic symbols that can occur in either organization is illustrated by the TM4256GP8. The TMS4256 has separate input and output pins. In the module, these have been connected together to form a single I/O port. In the module symbol, this is indicated using Z dependency to transfer the output signal from the right side to the left side.



If you have questions on this Explanation of IEEE/IEC Logic Symbols, please contact:

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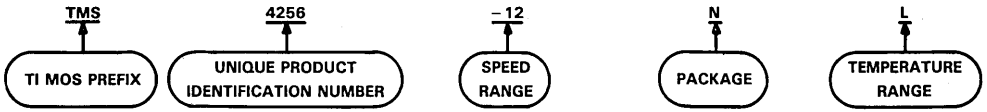
general

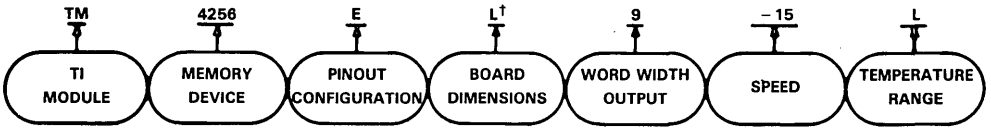
Electrical characteristics presented in this catalog, unless otherwise noted, apply to device type(s) listed in the page heading, regardless of package. Factory orders for devices described should include the complete part-type numbers listed on each page.

MOS memory device numbering system



		Max Access			
TMS Commercial MOS	− 4	45 ns	−20 200 ns	DJ Plastic SOJ Package	E −40°C to 85°C
SMJ Military MOS	− 5	55 ns	−25 250 ns	FM Plastic Chip Carrier	L 0°C to 70°C
TMX Pre-production MOS	− 7	70 ns	−30 300 ns	FP Plastic Chip Carrier	M −55°C to 125°C
	−10	100 ns	−35 350 ns	J Cerpak/Cerdip	S −55°C to 100°C
	−12	120 ns	−45 450 ns	JD Side Braze	
	−15	150 ns		N Plastic DIP	

TI single-in-line package nomenclature



Max Access	L 0°C to 70°C
−12 120 ns	
−15 150 ns	
−20 200 ns	

†The board dimensions for the various single-in-line package designators are given on pages 11-16 thru 11-23.

manufacturing information

Die-attach is by standard gold silicon eutectic or by conductive polymer.

Thermal compression gold wire bonding is used on plastic packaged circuits. Typical bond strength is 5 grams. Bond strength is monitored on a lot-to-lot basis. Any preseal bond strength of less than 2 grams causes rejection of the entire lot of devices. On hermetic devices either thermal compression or ultrasonic wire bonding is used. All hermetic MOS LSI and VLSI devices produced by TI are capable of withstanding 5×10^{-7} atm cc/sec inspection and may be screened to 5×10^{-8} atm cc/sec fine leak, if desired by the customer, for special applications.

All packages are capable of withstanding a shock of 3000 g. All packages are capable of passing a 20,000 g acceleration (centrifuge) test in the Y-axis. Pin strength is measured by a pin-shearing test. All pins are able to withstand the application of a force of 6 pounds at 45°C in the peel-off direction.

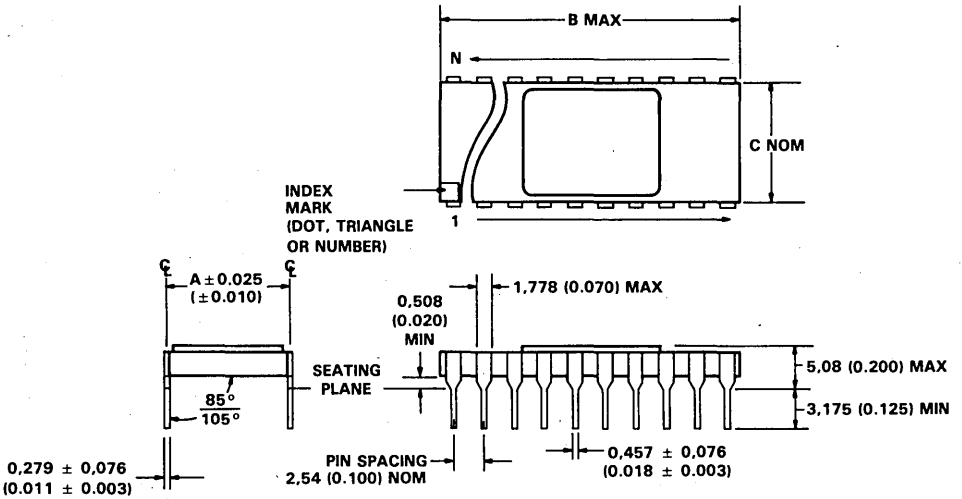
dual-in-line packages

A pin-to-pin spacing of 2,54 mm (100 mils) has been selected for standard dual-in-line packages (both plastic and ceramic).

TI uses three types of hermetically sealed ceramic dual-in-line packages: cerdip, cerpak, and sidebrazed. The cerdip and cerpak packages have tin-plated leads. The sidebraze package has gold-plated leads. The plastic package may have tin-plated leads, 60/40 solder-plated leads, or 60/40 hot-solder-dipped-finished-leads.

ceramic packages

side braze (JD suffix)



DIM \ PINS	16	18	20	22	24	24	28	40
A ± 0,025 (± 0.010)	7,62 (0.300)	7,62 (0.300)	7,62 (0.300)	10,16 (0.400)	7,62 (0.300)	15,24 (0.600)	15,24 (0.600)	15,24 (0.600)
B(MAX)	20,57 (0.810)	23,11 (0.910)	25,65 (1.010)	27,94 (1.100)	30,86 (1.215)	32,77 (1.290)	35,94 (1.415)	51,31 (2.020)
C(NOM)	7,493 (0.295)	7,493 (0.295)	7,493 (0.295)	10,03 (0.395)	7,493 (0.295)	15,11 (0.595)	15,11 (0.595)	15,11 (0.595)

ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

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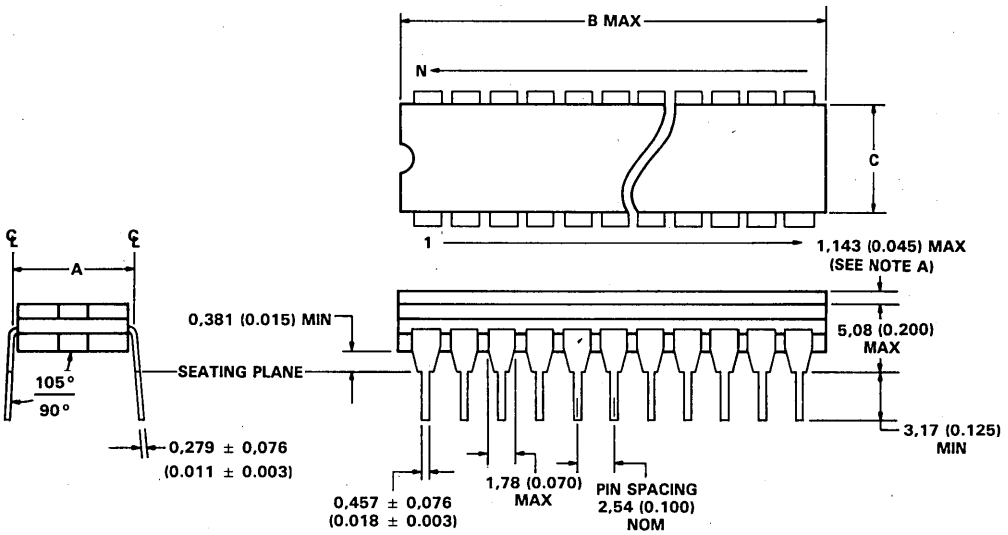
cerdip/300 mil cerpak (J suffix)

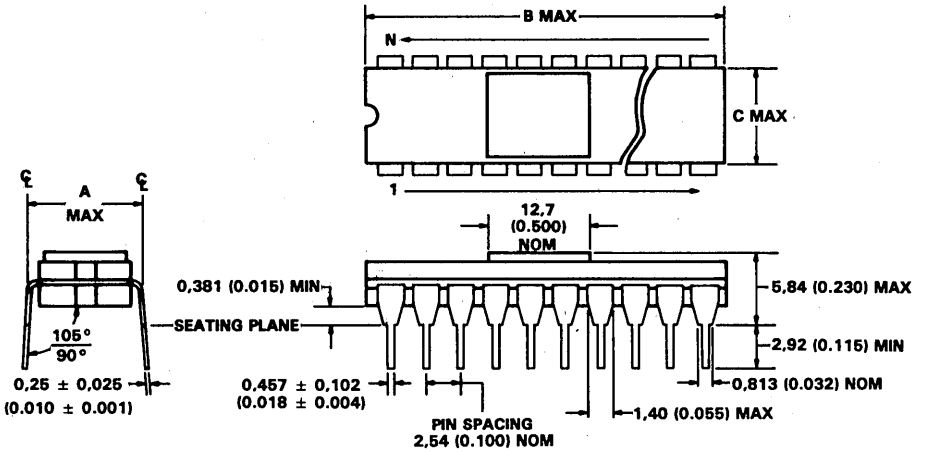


DIM \ PINS	16†	18	20	24
A(MAX)	8,255 (0.325)	8,255 (0.325)	8,255 (0.325)	8,255 (0.325)
B(MAX)	19,56 (0.770)	22,86 (0.900)	24,38 (0.960)	32,00 (1.260)
C(MAX)	7,645 (0.301)	7,645 (0.301)	7,645 (0.301)	7,645 (0.301)

†Dimensions A, B, and C are applicable for both 16-pin cerdip and cerpak.
NOTE A: Cerpak only

ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

600-mil cerpak (J suffix)



DIM \ PIN	24	28
A(MAX)	15,88 (0.625)	15,88 (0.625)
B(MAX)	32,77 (1.290)	37,85 (1.490)
C(MAX)	15,24 (0.600)	15,24 (0.600)

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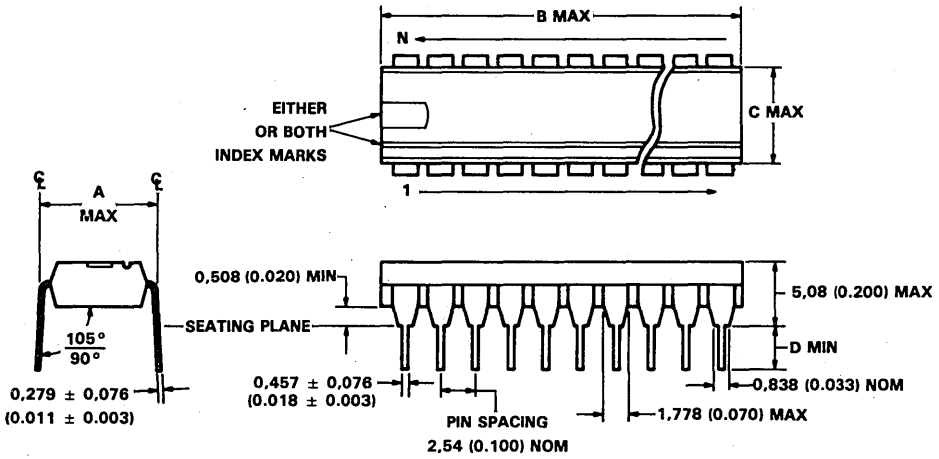
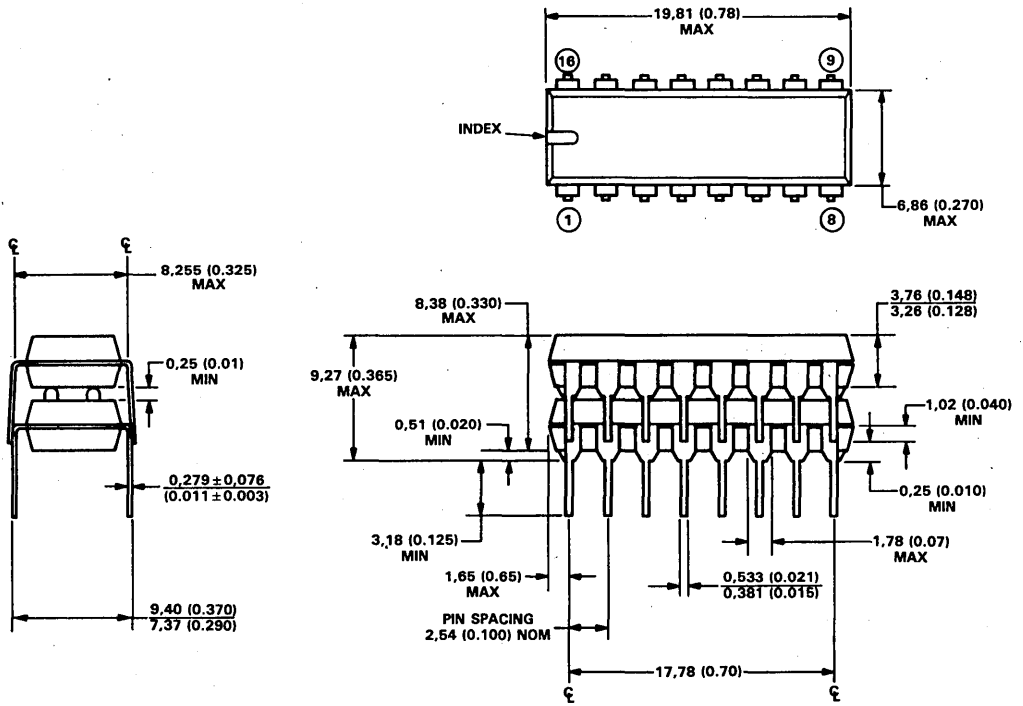
plastic packages (N suffix)



DIM \ PINS	16	18	20	22	24	28	40
A (MAX)	8,255 (0.325)	8,255 (0.325)	8,255 (0.325)	10,80 (0.425)	15,88 (0.625)	15,88 (0.625)	15,49 (0.61)
B (MAX)	22,1 (0.870)	23,37 (0.920)	27,18 (1.070)	28,45 (1.120)	32,26 (1.270)	36,58 (1.440)	53,1 (2.090)
C (MAX)	6,858 (0.270)	6,858 (0.270)	6,858 (0.270)	9.017 (0.355)	13,97 (0.550)	13,97 (0.550)	13,97 (0.550)
D (MIN)	3,175 (0.125)	2,921 (0.115)	2,921 (0.115)	3,175 (0.125)	2,921 (0.115)	2,921 (0.115)	3,175 (0.125)

ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

16-pin plastic dual-in-line stacked packages



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

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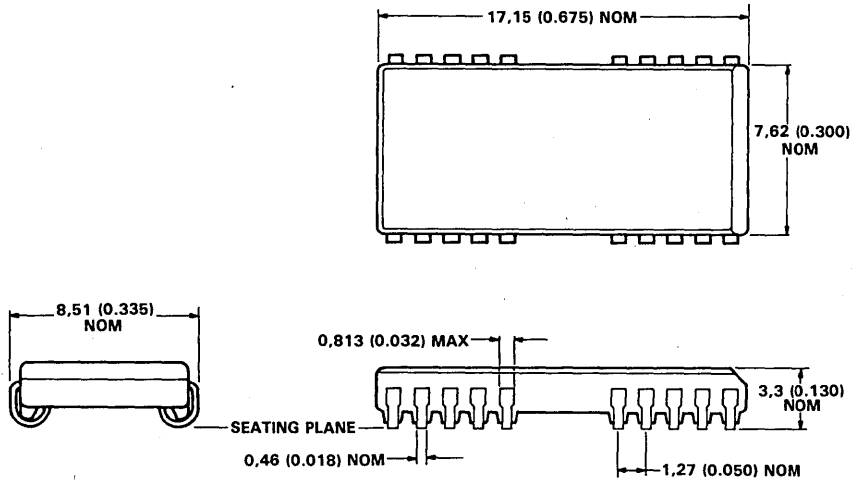
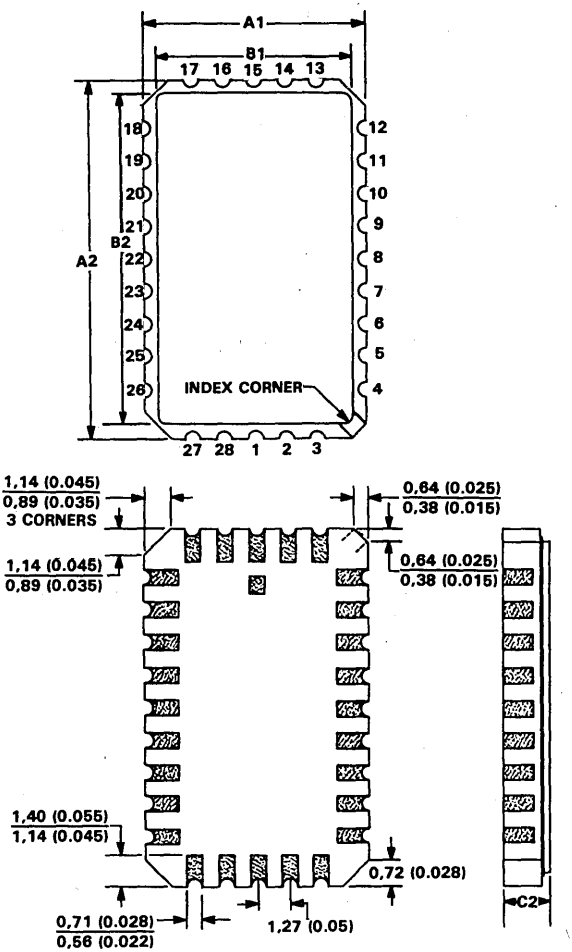
26/20-lead plastic small outline J-lead surface mount package (DJ suffix)



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

ceramic chip carrier packages

ceramic chip carrier package (FE suffix)



NUMBER OF TERMINALS	A1		A2		B1		B2		C2	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
28	8,76 (0.345)	9,02 (0.355)	13,84 (0.545)	14,10 (0.555)	7,80 (0.307)	7,95 (0.313)	12,88 (0.507)	13,03 (0.513)	1,65 (0.065)	2,01 (0.079)
32	11,30 (0.445)	11,56 (0.455)	13,84 (0.545)	14,10 (0.555)	10,34 (0.407)	13,03 (0.513)	12,88 (0.507)	13,03 (0.513)	1,65 (0.065)	2,01 (0.079)

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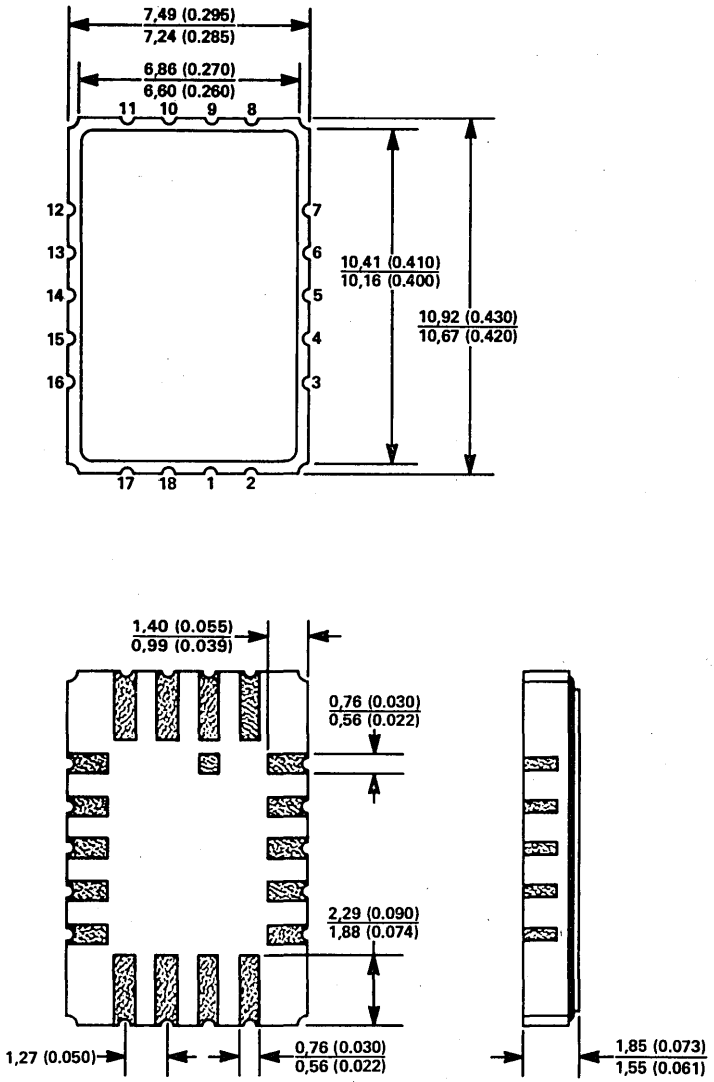
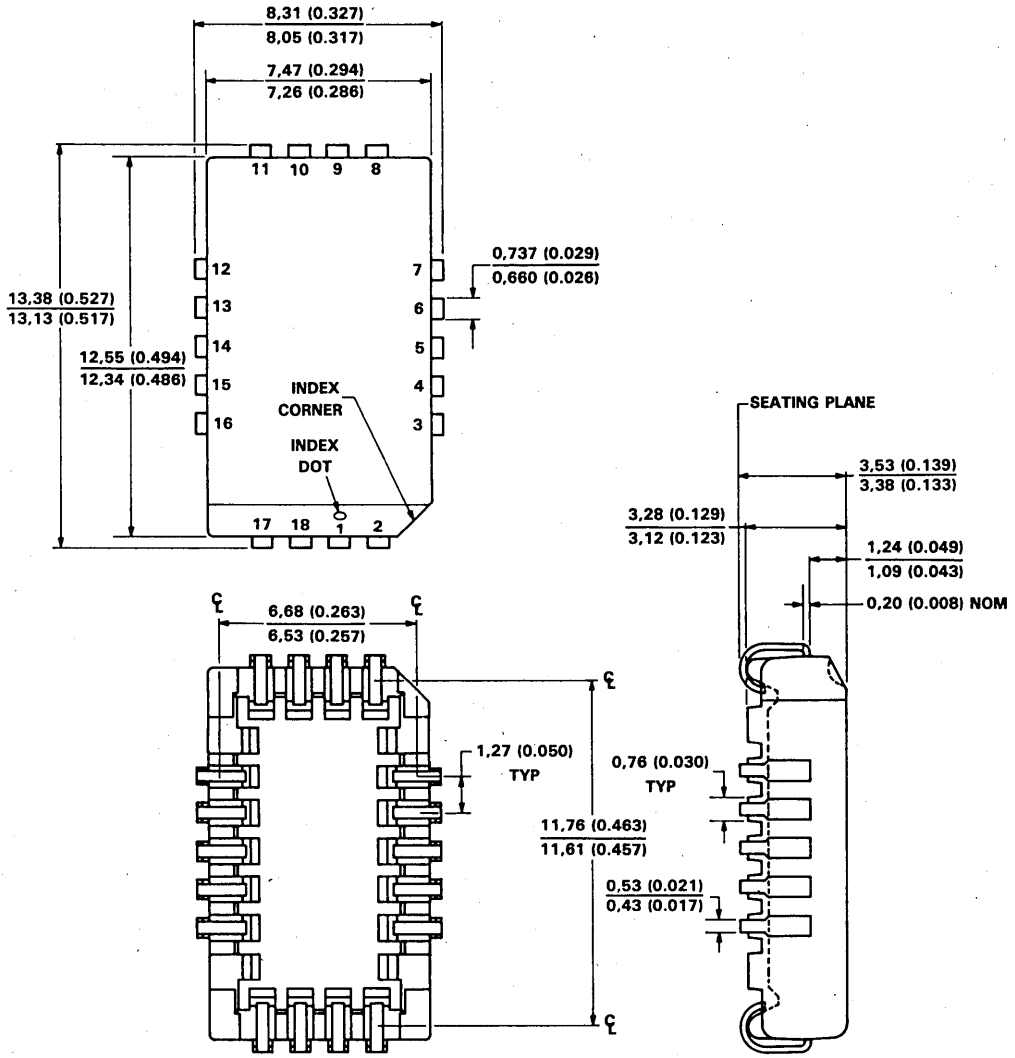
ceramic chip carrier package (FG suffix)



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

plastic chip carrier packages

18-lead plastic chip carrier package (FM suffix)



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

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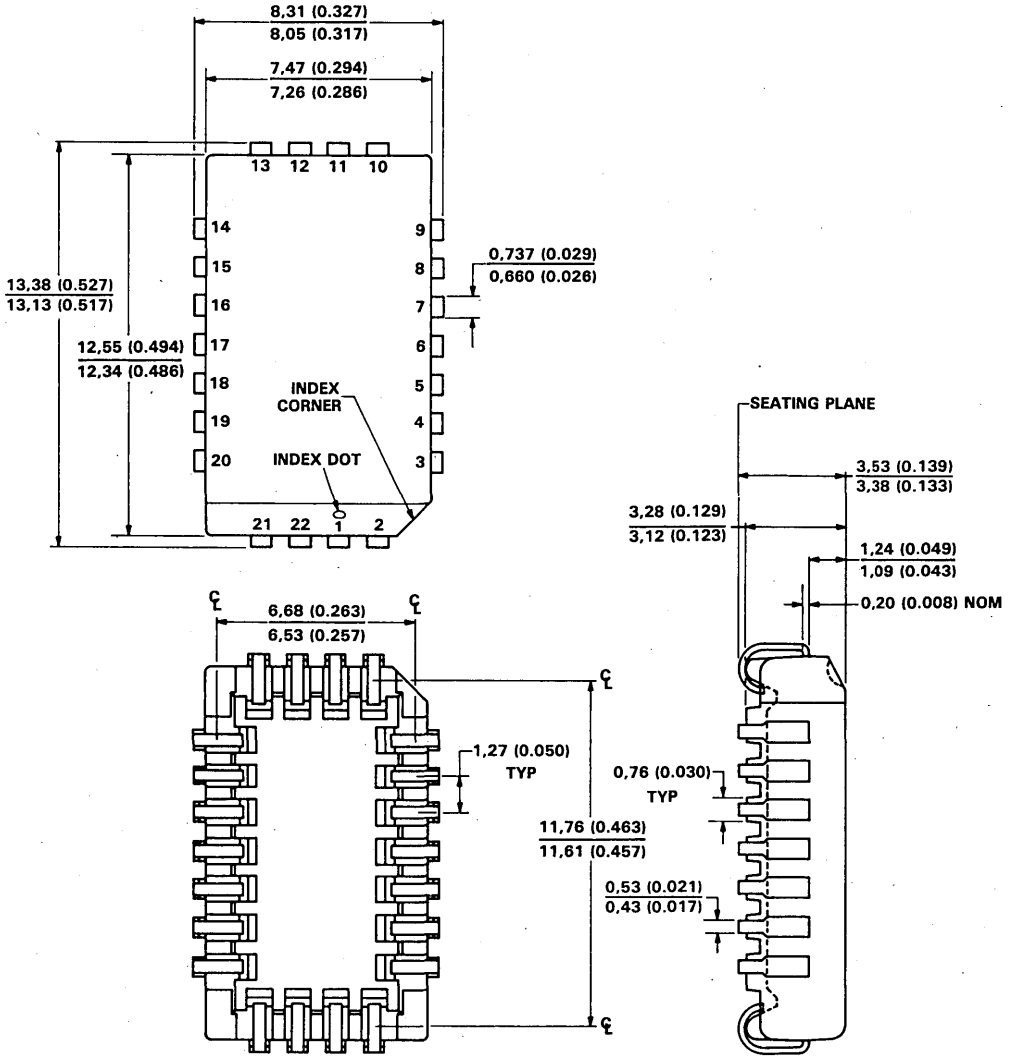
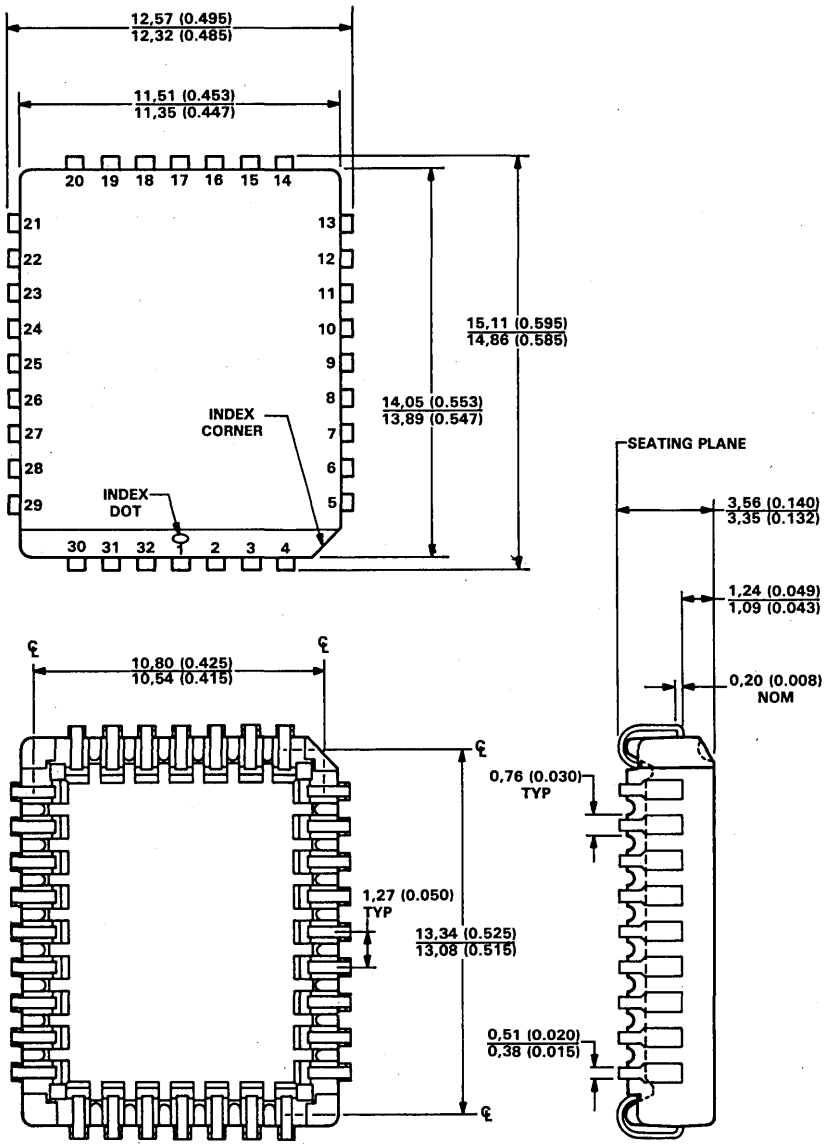
22-lead plastic chip carrier package (FM suffix)



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

32-lead plastic chip carrier package (FM suffix)



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

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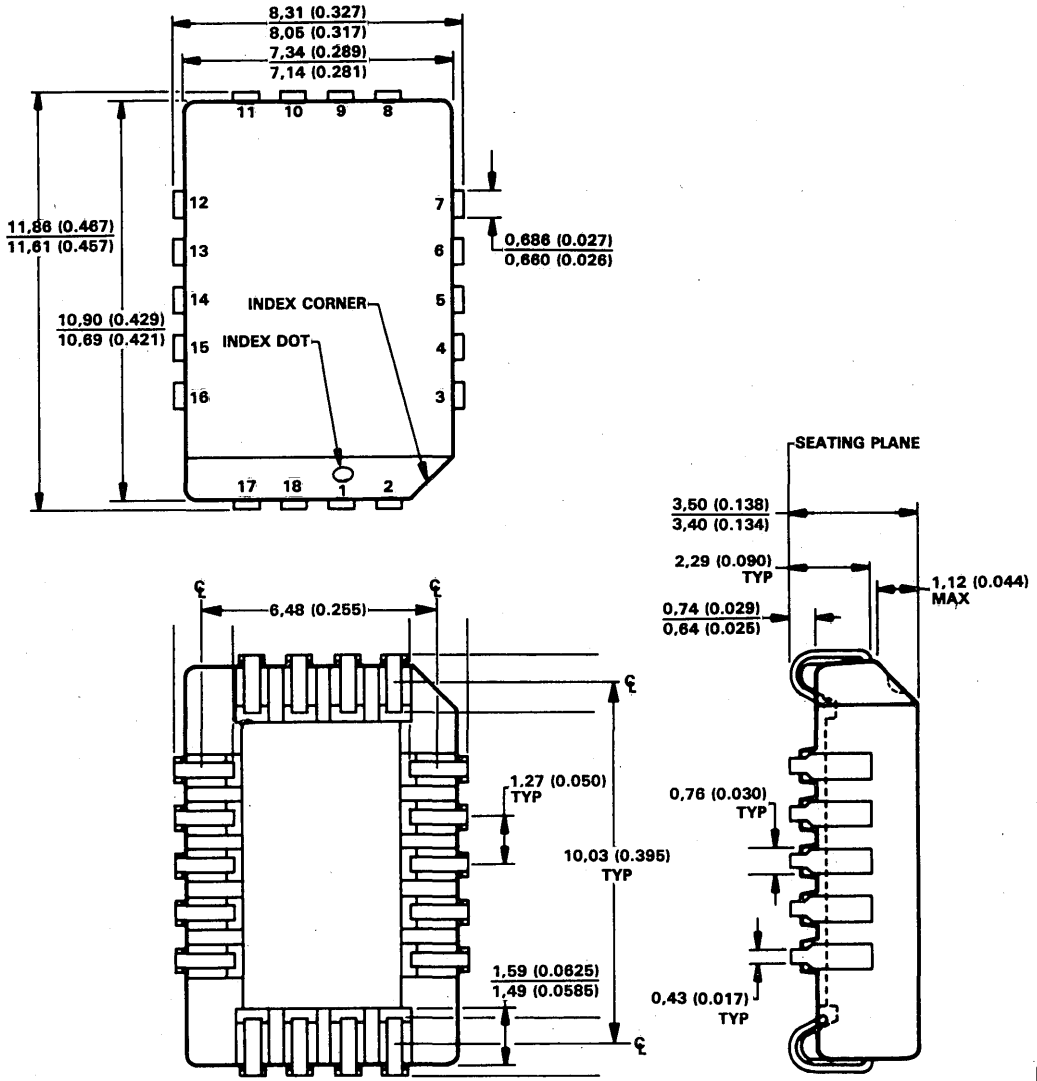
plastic chip carrier package (FP suffix)



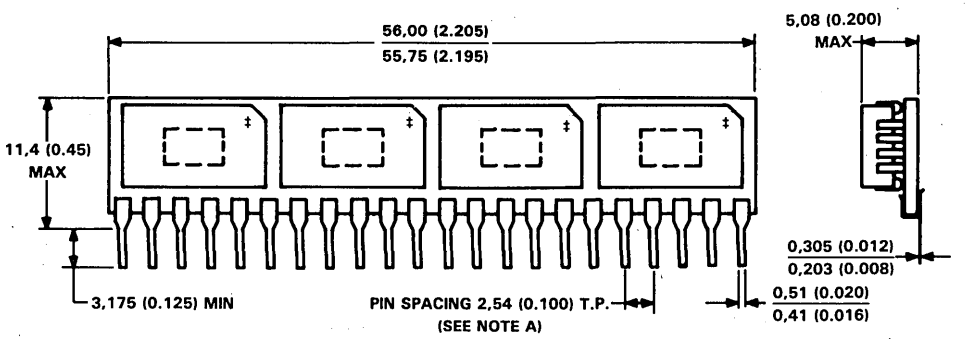
MECHANICAL DATA

single-in-line packages (C, E, L, M, P, Q, U, V, W, and Y designators)

TM · 4256 E L 9 -15 L

Package Designator

22-pin C single-in-line package†



†This package is used for the TM4164EC4, TM4256EC4, TM4256FC1, TM4257EC4, and TM4257FC1.
‡For specific chip carrier orientation, see the pinout drawing for that device.
NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

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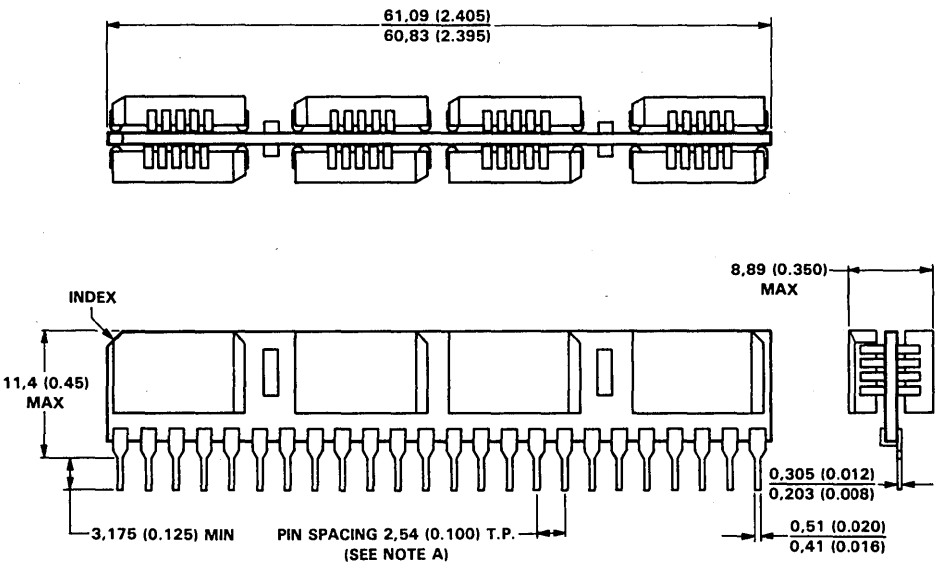
22-pin E single-in-line package†

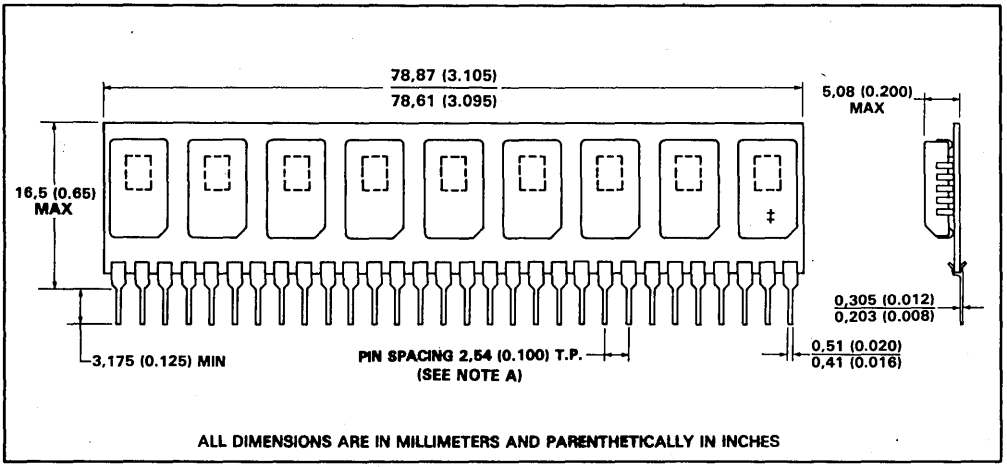


ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

†This package is used for the TM4256HE4.

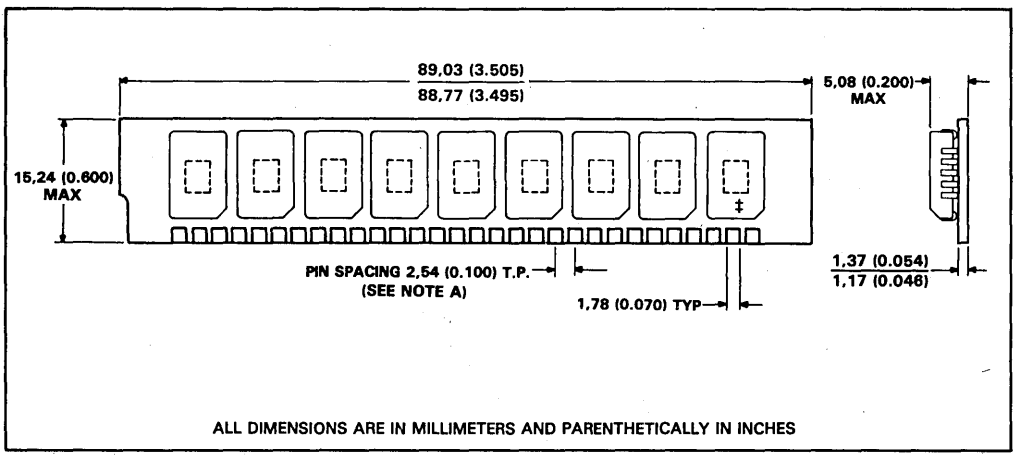
NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

30-pin L single-in-line package†



†This package is used for the TM4164EL9, TM4164FL8, TM4256EL9, TM4256FL8, TM4257EL9, and TM4257FL8.
‡This chip carrier is not present on the TM4164FL8, TM4256FL8, and TM4257FL8 packages.
NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

30-pin M single-in-line package†



†This package is used for the TM4164FM8 and TM4164FM9.
‡This chip carrier is not present on the TM4164FM8 package.
NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

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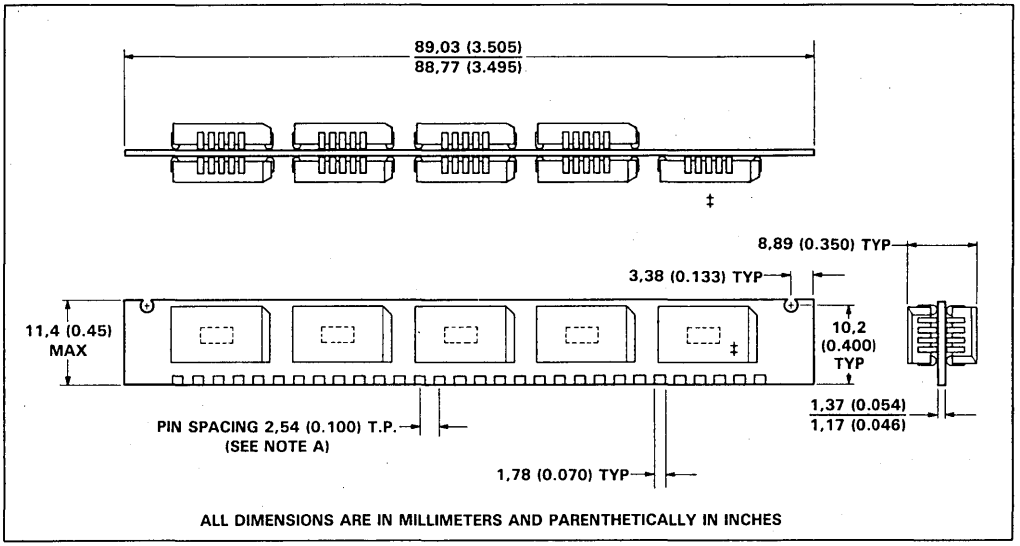
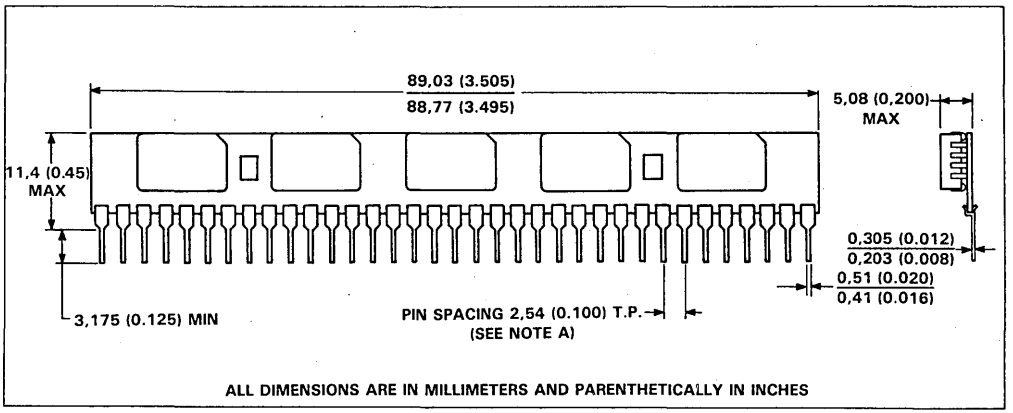
30-pin P single-in-line package†



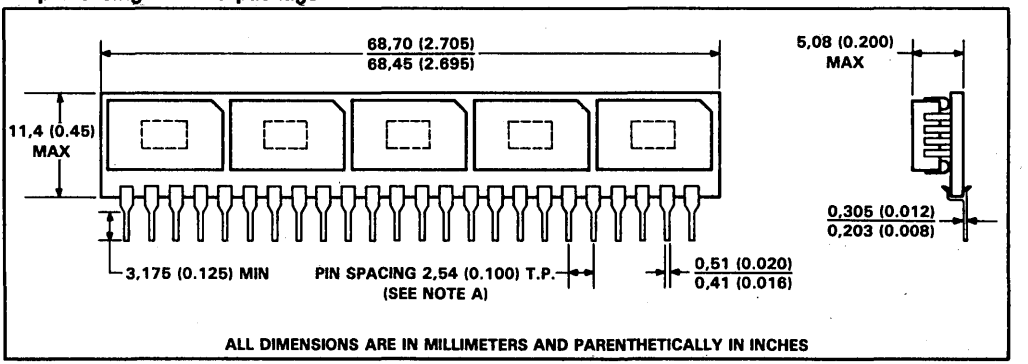
†This package is used for the TM4256GP8 and TM4256GP9.
‡This chip carrier is not present on the TM4256GP8.
NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

35-pin P single-in-line package†



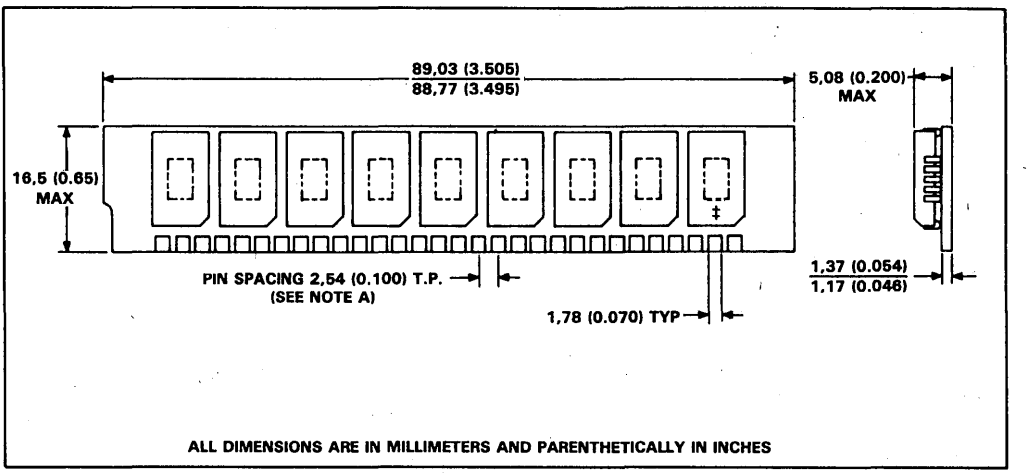
†This package is used for the TM4161EP5.
NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

24-pin Q single-in-line package†



†This package is used for the TM4164EQ5, TM4256EQ5, and TM4257EQ5.
NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

30-pin U single-in-line package†



†This package is used for the TM4256GU8, TM4256GU9, TM4257GU8, and TM4257GU9.
‡This chip carrier is not present on the TM4256GU8 and TM4257GU8.
NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

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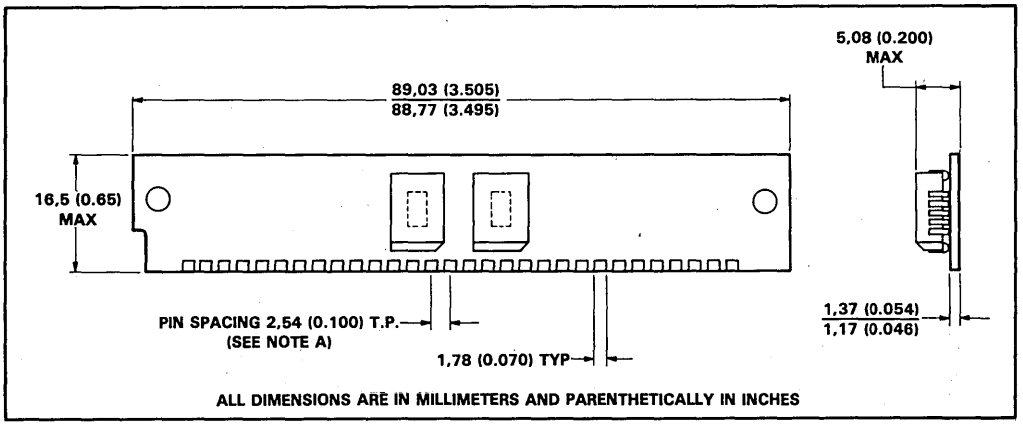
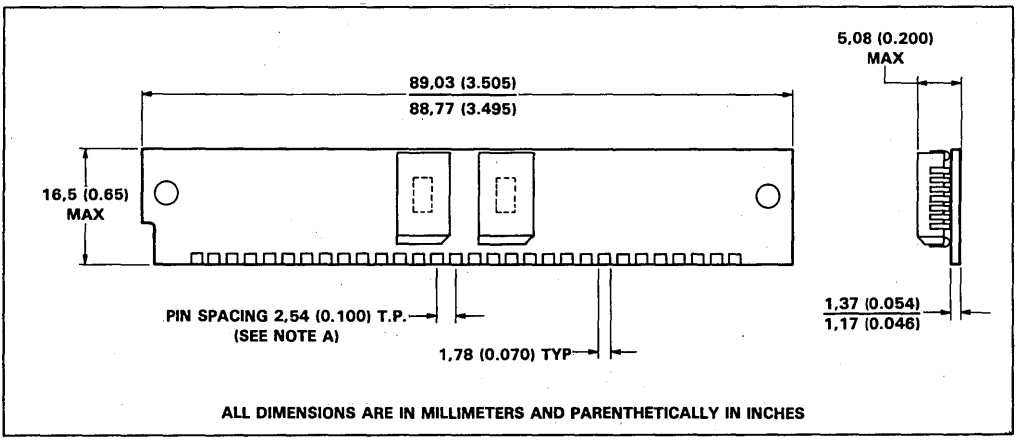
30-pin U single-in-line package†



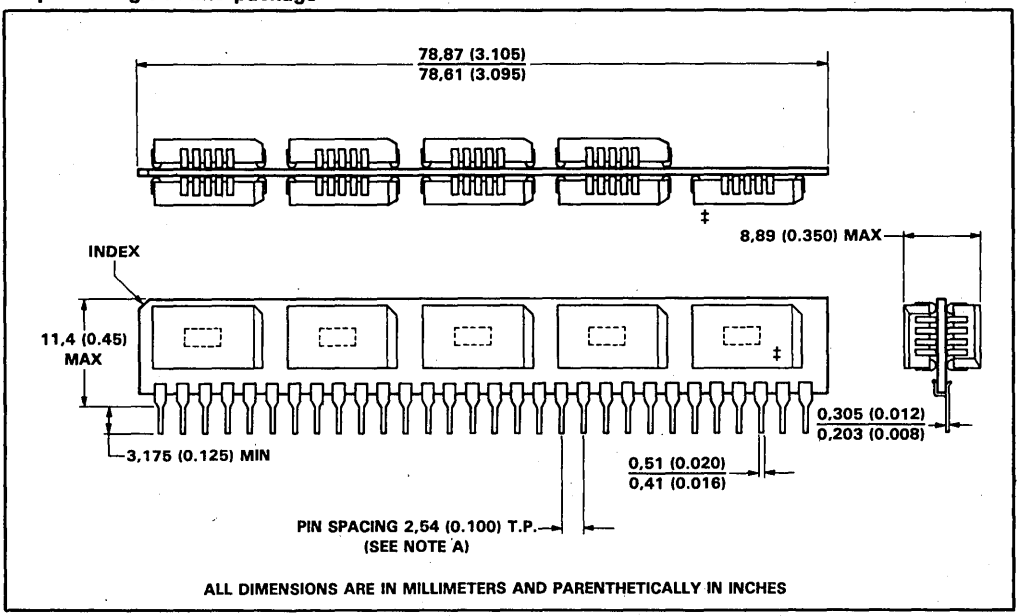
†This package is used for the TM4416KU8.
NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

30-pin U single-in-line package†



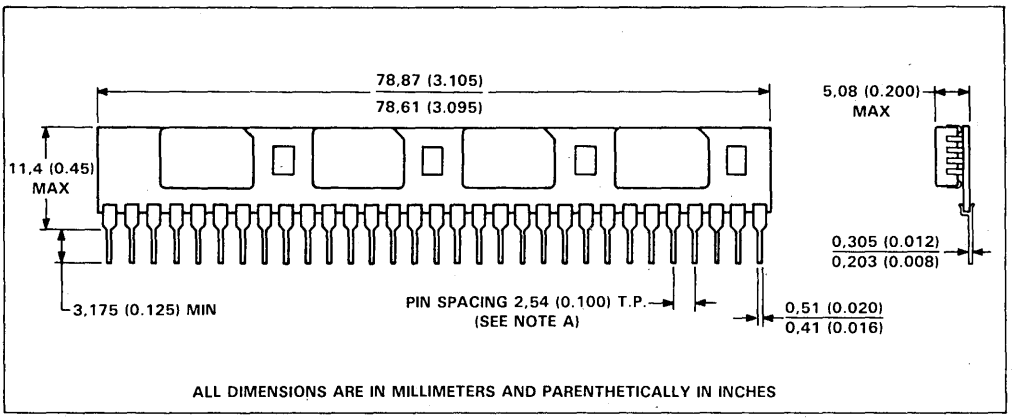
†This package is used for the TM4464LU8.
NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

30-pin V single-in-line package†



†This package is used for the TM4256GV8 and TM4256GV9.
‡This chip carrier is not present on the TM4256GV8.
NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

31-pin V single-in-line package†



†This package is used for the TM4161EV4.
NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

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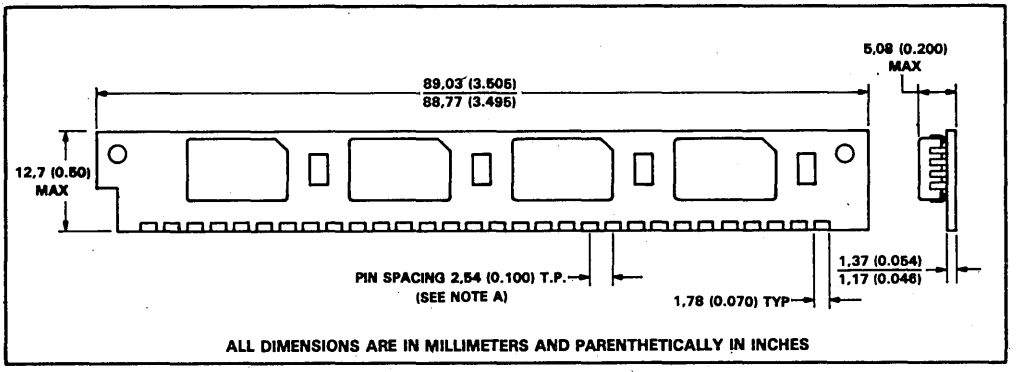
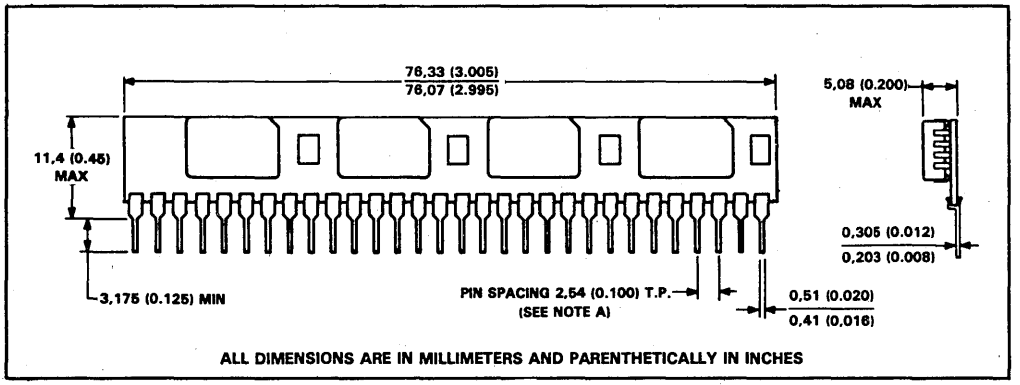
30-pin W single-in-line package†



†This package is used for the TM4161GW4.
NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

30-pin Y single-in-line package†



†This package is used for the TM4161GY4.
NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

Guidelines for Handling Electrostatic-Discharge Sensitive (ESDS) Devices and Assemblies

SCOPE

This specification establishes the requirements for methods and materials used to protect electronic parts, devices, and assemblies (items) susceptible to damage or degradation from electrostatic discharge (ESD). The electrostatic charges referred to in this specification are generated and stored on surfaces of ordinary plastics, most common textile garments, ungrounded people's bodies, and many other commonly unnoticed static generators. The passage of these charges through an electrostatic-sensitive part may result in catastrophic failure or performance degradation of the part.

The part types for which these requirements are applicable include, but are not limited to, those listed:

1) All metal-oxide semiconductor (MOS) devices, e.g., CMOS, PMOS, etc.
2) Junction field-effect transistors (JFET)
3) Bipolar digital and linear circuits
4) Op Amps, monolithic microcircuits with MOS compensating networks, on-board MOS capacitors, or other MOS elements
5) Hybrid microcircuits and assemblies containing any of the types of devices listed
6) Printed circuit boards and any other type of assembly containing static-sensitive devices.

Definitions

1. Antistatic material: ESD protective material having a surface resistivity between 10^9 and 10^{14} Ω/square.
2. Static dissipative material: ESD protective material having surface resistivity between 10^5 and 10^9 Ω/square.
3. Conductive material: ESD protective material having a surface resistivity of 10^5 Ω/square maximum.
4. Electrostatic discharge (ESD): A transfer of electrostatic charge between bodies at different electrostatic potentials caused by direct contact or induced by an electrostatic field.
5. Surface resistivity: An inverse measure of the conductivity of a material and is the resistance of unit length and unit width of a surface. Note: Surface resistivity of a material is numerically equal to the surface resistance between two electrodes forming opposite sides of a square. The size of the square is immaterial. Surface resistivity applies to both surface and volume conductive materials and has the dimension of Ω/square.
6. Volume resistivity: Also referred to as bulk resistivity. It is normally determined by measuring the resistance (R) of a square of material (surface resistivity) and multiplying this value by the thickness (T).
7. Ionizer: A blower that generates positive and negative ions, either by electrostatic means or by means of a radioactive energy source, in an airstream, and distributes a layer of low velocity ionized air over a work area to neutralize static charges.
8. Close proximity: For the purpose of this specification, is 6 inches or less.

Device Sensitivity per Test Circuit of Method 3015, MIL-STD-883

Devices are categorized according to their susceptibility to damage resulting from electrostatic discharge (ESD), and the type packaging required to adequately protect them.

1) Device electrostatic sensitivity:

Category	ESD Sensitivity (V)	Minimum Protective Packaging
A	20-2000	Antistatic Magazine & Conductive Bag/Box
B	> 2000	Antistatic Magazine & Antistatic Bag

2) Devices are to be categorized by their sensitivity
3) Devices are to be protected from ESD damage from receipt at incoming inspection through assembly, test and shipment of completed equipment.

APPLICABLE REFERENCE DOCUMENTS

The following reference documents (of latest issue) can provide additional information on ESD controls.

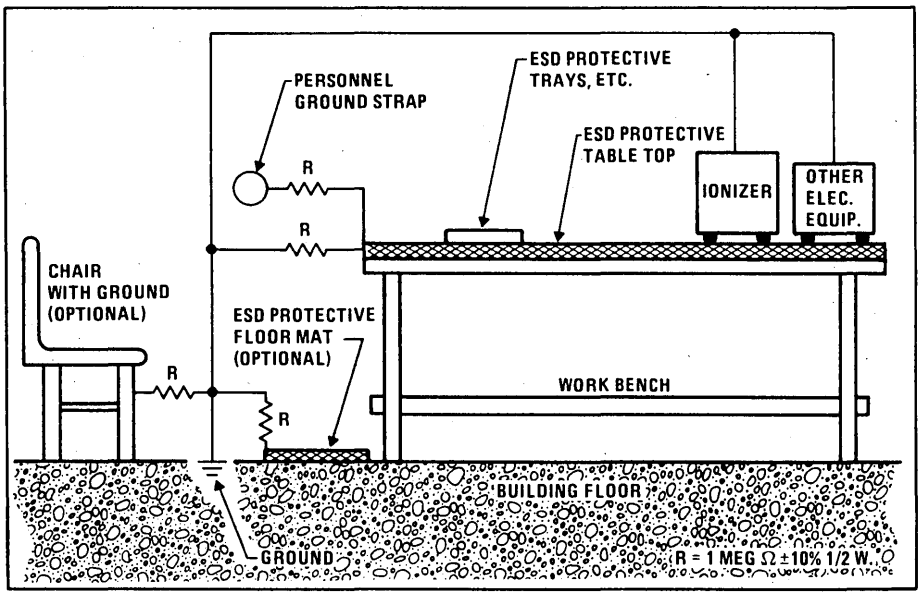
1) MIL-M-38510 Microcircuits, General Specification
2) MIL-STD-883 Test Methods and Procedures for Microelectronics
3) MIL-S-19491 Semiconductor Devices, Packaging of
4) MIL-M-55565 Microcircuits, Packaging of
5) DOD-HDBK-263 Electrostatic Discharge Control Handbook for Protection
6) DOD-STD-1686 Electrostatic Discharge Control Program
7) NAVSEA SE 003-11-TRN-010 Electrostatic Discharge Training Manual

FACILITIES FOR STATIC-FREE WORK STATION

The minimum acceptable static-free work station shall consist of the work surface covered with an ESD protective material attached to ground through a 1 MΩ ± 10% resistor, an attached grounding wrist strap with integral 1 MΩ ± 10% resistor for each operator, and air ionizer(s) of sufficient capacity for each operator. The wrist strap shall be connected to the ESD protective material. Ground shall utilize the standard building earth ground, refer to Figure 1. Conductive floor tile along with conductive shoes may be used in lieu of the conductive wrist straps. The Site Safety Engineer must review and approve all electrical connections at the static-free work station prior to its implementation.

Air ionizers shall be positioned so that the devices at the static-free work stations are within a 4-foot arc measured by a vertical line from the face of the ionizer and 45 degrees on each side of this line.

General grounding requirements are to be in accordance with Table 1.



All electrical equipment sitting on the conductive table top must be hard grounded but must be isolated from the conductive table top.

NOTE: Earth ground is not computer ground or RF ground or any other limited type ground.

Figure 1. Static-Free Work Station

Table 1. General Grounding Requirements

	TREATED WITH ANTISTATIC SOLUTION OR MADE OF CONDUCTIVE MATERIAL	GROUNDED TO COMMON POINT
Handling Equipment/Handtools	X	
Metal Parts of Fixtures and Tools/Storage Racks		X
Handling Trays/Tubes	X	
Soldering Irons/Bath		X
Table Tops/Floor Mats	X	X
Personnel		X Using Wrist Strap*

*With 1 MΩ ± 10% resistor

Usage of Antistatic Solution in Areas to Control the Generation of Static Charges

The use of antistatic chemicals (antistats) should be a supplemental part of an overall organized ESD program. Any antistatic chemical application shall be considered as a means to reduce or eliminate static charge generation on nonconductive materials in the manufacturing or storage areas.

The application of any antistatic chemical in a clean room of class 10,000 or less shall not be permitted. Accordingly, any user of antistatic solutions must consider the following precautions:

1. Do not apply antistatic spray or solutions in any form to energized electrical parts, assemblies, panels, or equipment.
2. Do not perform antistatic chemical applications in any area when bare chips, raw parts, packages, and/or personnel are exposed to spray mists and evaporation vapors.

The need for initial application and frequency of reapplication can only be established through routine electrostatic voltage measurements using an electrostatic voltmeter. The following durability schedule is a reasonable expectation.

1) Soft surfaces (carpet, fabric seats, foam padding, etc.): each 6 months or after cleaning, by spraying.
2) Hard abused surfaces (floors, table tops, tools, etc.): each week (or day for heavy use) and after cleaning, by wiping or mopping.
3) Hard unabused surfaces (cabinets, walls, fixtures, etc.): each 6 months or annually and after cleaning, by wiping or spraying.
4) Company-furnished and maintained clothing and smocks: after each cleaning, by spraying or adding antistatic concentrate to final rinse water when cleaned.

The use of antistatic chemicals, their application, and compliance with all appropriate specifications, precautions, and requirements shall be the responsibility of the Area Supervisor where antistatic chemicals are used.

ESD Labels and Signs in Work Areas

ESD caution signs at work stations and labels on static-sensitive parts and containers shall be consistent in color, symbols, class, and voltage sensitivity identification, and appropriate instructions. Signs shall be posted at all work stations performing any handling operations with static-sensitive items. These signs shall contain the following information.

CAUTION

STATIC CAN DAMAGE COMPONENTS

Do not handle ESDS items unless grounding wrist strap is properly worn and grounded. Do not let clothing or plain plastic materials contact or come in close proximity to ESDS items.

Labels shall be affixed to all containers containing static-sensitive items at a place readily visible and proper for the intended purpose. Additionally, labels must be consistently placed on containers and packages at a standard location to eliminate mishandling. Use only QC accepted and approved signs and labels to identify static-sensitive products and work areas. The use of ESD signs and labels, and their information content shall be the responsibility of the Area Supervisor to assure consistency and compatibility throughout the static-sensitive routing.

Relative Humidity Control

Since relative humidity has a significant impact on the generation of static electricity, when possible, the work area should be maintained within the following relative humidity ranges: incoming/assembly/test/storage 50%-65% (ref. Ashrae, 55—74), within ±5% to avoid static voltage monitor variations.

PREPARATION FOR WORKING AT STATIC-FREE WORK STATION

A work station with a conductive work surface connected to ground through a 1 MΩ ±10% resistor, a grounding wrist strap with the ground wire connected to the conductive work surface, and an ionizer constitute a static-free work station (Figure 42). An operator is properly grounded when the wrist strap is in snug (no slack) contact with the bare skin, usually positioned on the left wrist for a right-handed operator. The wrist strap must be worn the entire time an operator is at a static-free work station. The operator should first touch the grounded bench top before handling static-sensitive items. This precaution should be observed in addition to wearing the grouding wrist strap. If possible, operators should avoid touching leads or contacts even though grounded.

CAUTION

Personnel shall never be attached to ground without the presence of the 1 MΩ ±10% series resistor in the ground wire.

An operator's clothing should never make contact or come in close proximity with static sensitive items. They must be especially careful to prevent any static-sensitive items (being handled) from touching their clothing. Long sleeves must be rolled up or covered with antistatic sleeve protector banded to the bare wrist which shall "cage" the sleeve at least as far up as the elbow. Only antistatic finger cots may be used when handling static-sensitive items.

Any person not properly prepared, while at or near the work station, shall not touch or come in close proximity with any static-sensitive items. It is the responsibility of the operator and the Area Supervisor to ensure that the static-free work area is clear of unnecessary static hazards, including such personal items as plastic coated cups or wrappers, plastic cosmetic bottles or boxes, combs, tissue boxes, cigarette packages, and vinyl or plastic purses. All work-related items, including information sheets, fluid containers, tools, and parts carriers must be those approved for use at the static-free work station.

GENERAL HANDLING PROCEDURES AND REQUIREMENTS

1. All static-sensitive items must be received in an antistatic/conductive container and must not be removed from the container except at static-free work station. All protective folders or envelopes holding documentation (lot travelers, etc.) shall be made of nonstatic-generating material.
2. Each packing (outermost) container and package (internal or intermediate) shall have a bright yellow warning label attached, stating the following information or equivalent:

   The warning label shall be legible and easily readable to normal vision at a distance of 3 feet.
3. Static-sensitive items are to remain in their protective containers except when actually in work at the static-free station.
4. Before removing the items from their protective container, the operator should place the container on the conductive grounded bench top and make sure the wrist strap fits snugly around the wrist and is properly plugged into the ground receptacle, then touch hands to the conductive bench top.
5. All operations on the items should be performed with the items in contact with the grounded bench top as much as possible. Do not allow conductive magazine to touch hard grounded test gear on bench top.

6. Ordinary plastic solder-suckers and other plastic assembly aids shall not be used.
7. In cases where it is impossible or impractical to ground the operator with a wrist strap, a conductive shoe strap may be used along with conductive tile/mats.
8. When the operator moves from any other place to the static-free station, the start-up procedure shall be the same as in PREPARATION FOR WORKING AT STATIC-FREE WORK STATION.
9. The ionizer shall be in operation prior to presenting any static-sensitive items to the static-free station, and shall be in operation during the entire time period the items are at the station.
10. "Plastic snow" polystyrene foam, "peanuts," or other high-dielectric materials shall never come in contact with or be used around electrostatic sensitive items, unless they have been treated with an antistat (as evidenced by pink color and generation of less than ±100 volts).
11. Static-sensitive items shall not be transported or stored in trays, tote boxes, vials, or similar containers made of untreated plastic material unless items are protectively packaged in conductive material.

PACKAGING REQUIREMENTS

Packaging of static-sensitive items is to be in accordance with Device Sensitivity, item 1). The use of tape and plain plastic bags is prohibited. All outer and inner containers are to be marked as outlined in GENERAL HANDLING PROCEDURES AND REQUIREMENTS, item 2, and conductive magazines/boxes may be used in lieu of conductive bags.

SPECIFIC HANDLING PROCEDURES FOR STATIC-SENSITIVE ITEMS

Stockroom Operations

1. Containers of static-sensitive items are not to be accepted into stock unless adequately identified as containing static-sensitive items.
2. Items may be removed from the protective container (magazine/bag, etc.) for the purpose of subdividing for order issue only by a properly grounded operator at an approved static-free station as defined in FACILITIES FOR and PREPARATION FOR WORKING AT STATIC-FREE WORK STATION.
3. All subdivided lots must be carefully repackaged in protective containers (magazine/bag, etc.) prior to removal from the static-free work station and labeled to indicate that the package(s) contain static-sensitive items. If it is suspected that a static-sensitive item is not adequately protected, do not transfer it to another container, return it to the originator for disposition unless the originator is a Customer. In that case, the QC Engineer should contact the Customer and negotiate an appropriate disposition.
4. It is the responsibility of the Stockroom Supervisor to ensure that all personnel assigned to this operation are familiar with handling procedures as outlined in this specification. A copy of this specification is to be posted in the vicinity so that it is accessible to the operators. Stock handlers and all others who might have occasion to move stock are to be instructed to avoid direct contact with unprotected static-sensitive items.

Module and Subassembly Operations

1. Static-sensitive items are not to be received from a stockroom, kitting, or machine insertion area unless received in approved static-protective packaging, and properly labeled to indicate that its contents are static sensitive.
2. All single station, progressive line manual assembly operators, and visual inspectors prior to wave soldering operations are to be properly grounded with a grounding wrist strap when handling static-sensitive items.
3. Progressive lines used as single stations where operators will be working on a mix of boards, both static-sensitive and nonstatic-sensitive, will require that all operators working on the line be properly grounded. This is necessary to accommodate the sliding of static-sensitive boards along the assembly bench or across positions not engaged in the assembly of this type board.
4. It is the responsibility of the Area Supervisor to ensure that all personnel handling static-sensitive items are familiar with this procedure and fully aware of the damage or degradation of these units in the event of noncompliance. A periodic inspection should be made using an electrostatic voltmeter to assure that the static-free stations are in proper working order and to ensure that operators are wearing grounding wrist straps properly (snugly in contact with bare skin).

Soldering and Lead-Forming Operations

1. All soldering machines, conveyors, cleaning machines, and equipment shall be electrically grounded to ensure that they are at the same ground potential as the grounded operators working on their stations. No machine surfaces exposed to static-sensitive items are to be above the ground potential.
2. All processing equipment shall be grounded, including all loading and unloading stations, that is, the stations before and after each piece of processing equipment.
3. All nonmetallic, static-generating components in the handling systems shall be treated to ensure protection from static.
4. All stations shall be identified by posting signs as outlined in **ESD Labels and Signs in Work Areas.**
5. Operators are to be properly grounded with a grounding wrist strap during any handling, loading, unloading, inspection, rework, or proximity to static-sensitive items.
6. Unloading operators working at a grounded station shall place static-sensitive items into approved static-protective bags or containers.
7. All manual soldering, repair, and touch-up work stations on the solder line are to be static protected. Operators are to wear grounding wrist straps when working on static-sensitive items. Only grounded-tip soldering/desoldering irons are allowed when working on static-sensitive items.
8. It is the responsibility of the Area Spervisor to ensure that all personnel handling static-sensitive items are familiar with this procedure and fully aware of the damage or degradation of these units in the event of noncompliance. A periodic inspection should be made using an electrostatic voltmeter to assure that the static-free stations are in proper working order and to ensure that operators are wearing grounding wrist straps properly (comfortably snug in contact with bare skin).

Electrical Testing Operations

1. All electrical test stations shall be static protected. Operators shall be properly grounded when working on these items.
2. Reused antistatic magazines must be monitored for maintenance of antistatic characteristics.
3. Devices should be in an antistatic/conductive environment except at the moment when actually under test.
4. Devices should not be inserted into or removed from circuits or tester with the power on or with signals applied to inputs to prevent transient voltages from causing permanent damage.
5. All unused input leads should be biased if possible.
6. Device or module repairs must be performed at static-free stations with the operator attached to a grounding wrist strap. Grounded-tip soldering irons shall be used when working on static-sensitive items.
7. Static-sensitive items shall be handled through all electrical inspections in static protective containers. Removal of the items from the protective containers shall be done at a static-free work station as discussed in **PREPARATION FOR WORKING AT A STATIC-FREE WORK STATION.** The units must be returned to the containers before leaving the station.
8. All such items shall be shipped with an ESD warning label affixed as listed.
9. It is the responsibility of the Area Supervisor to ensure that all personnel handling static-sensitive items are familiar with this procedure and fully aware of the damage or possible degradation of these units in the event of noncompliance. A periodic inspection should be made using an electrostatic voltmeter to assure that the static-free stations are in proper working order and to ensure that operators are wearing grounding straps properly (snugly in contact with bare skin).

Packing Operations

1. Static-sensitive items are not to be accepted into the packing area unless they are contained in a static-protected bag or conductive container.
2. A static-sensitive item delivered to the packer within an approved container or bag and found to be in order regarding identification shall be packed in the standard shipping carton or other regular packaging material. Containers are to be labeled in accordance with **GENERAL HANDLING PROCEDURES AND REQUIREMENTS,** item 2.
3. Any void-fillers shall be made of an approved antistatic material.

Burn-In Operations

1. Burn-in board loading and unloading of static-sensitive items shall be done at a static-free station.
2. Shorting clips/shorted connectors shall be installed on the board plug-in tab prior to loading any units into the board sockets. The clip/connector shall be taken off just prior to plugging the board into the oven connector. The clip/connector shall be installed immediately upon removal of the board from the oven connector. Installation and removal of the clip/connector shall be done by a properly grounded operator.
3. All automatic or semiautomatic loading and unloading equipment shall be properly electrically grounded.
4. It is the responsibility of the Area Supervisor to ensure that all personnel handling static-sensitive items are familiar with this procedure and fully aware of the damage or possible degradation of these units in the event of noncompliance. A periodic inspection should be made using an electrostatic voltmeter to assure that the static-free stations are in proper working order and to ensure that operators are wearing grounding straps properly (snugly in contact with bare skin).

CUSTOMER RETURNED ITEM HANDLING PROCEDURE

Receipt of ESDS-labeled items is to be done at a static-free work station and handled in accordance with applicable sections within this guideline.

QUALITY CONTROL PROVISIONS

Sampling

Each manufacturing, stockroom, and testing operation handling ESDS devices will be audited a minimum of once each quarter for compliance with all terms of this specification by the responsible process control or QRA organization. Ground continuity and the presence of uncontrolled static voltages are considered critical and shall be checked more frequently as specified below.

Ground Continuity (minimum of once a week).

Ground connections (grounding wrist strap, ground wires on cords, etc.) shall be checked for electrical continuity. The presence of a 1 MΩ ±10% resistor in the ground connections between both the operator wrist straps to the work surface and the work surface to ground connector must be verified.

Grounded Conditions (minimum of once a week).

A visual inspection shall be made to determine full compliance with this specification at static-free work stations during handling of static-sensitive items, including operator being grounded as required, static-sensitive items not being handled in unprotected or unauthorized areas, and no static-generating materials at the grounded work station.

Sleeve Protectors (minimum of once a week).

A visual check shall be made to determine that each operator wearing loose-fitting or long-sleeved clothing either has sleeves properly rolled or covered with sleeve protectors properly grounded to the bare skin at the wrist.

Static Voltage Levels (minimum of once a week).

In addition to the visual inspections, a sample inspection using an electrostatic voltmeter will be used to check for uncontrolled electrostatic voltages at or near electrostatic-controlled work stations.

Conductive Floor Tiles (minimum of once a month).

Conductive floors must have a resistance of not less than 25 kΩ from any point on the tile to earth ground. Also, resistance from any point-to-point on the tile floor 3 feet apart shall be not less than 25 kΩ. The test methods to be used are ASTM-F-150-72 and NFPA 56.

Records

Written records must be kept of all these QC audits.

TRAINING

Training is applicable for all areas where individuals come in contact with ESDS (category A) devices. It is the responsibility of each Area Supervisor to make sure that his/her people receive ESD training initially and every 12 months thereafter to maintain proficiency. Training should include static fundamentals, a review of applicable parts of this specification, and actual applications in the work area.

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