SRSD001

2-μm CMOS Standard Cell Data Book

1986

SystemCell™ Series

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Specifications contained in this data book supersede all data for these products published by TI in the United States before September 1986.

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PREFACE

This data book contains a wealth of information to assist you in designing an Application-Specific IC (ASIC) using TI's new, 2-μm CMOS standard cell family — called **SystemCell™**. Included are; a selection guide, a cross-reference guide, a definition of symbols and glossary of common terms, a section on design guidelines, detailed mechanical data on the extensive range of **SystemCell™** package options and, comprehensive, detailed data sheets covering more than 320 cell types including:

- SSI logic functions (''gates'')
- MSI logic functions (''macros'')
- I/O cells
- Boolean functions
- CompilerCell™ functions (SRAM, ROM, PLA and Pipeline Test Register)

Fabricated in TI's advanced 2-μm (1.6-μm effective), double-level metal (DLM), twin-well, silicon-gate CMOS technology, ICs designed with the **SystemCell™** family can offer many significant benefits.

- Lower system cost
- Increased functionality
- Unique, secure product designs
- Shorter ''product-to-market'' times
- Reduced package count and board space
- Improved reliability

The advanced CMOS technology and high-volume production processes developed to support TI's high-density memory products provide the ''driving force'' behind the significant performance and density advances embodied in the new **SystemCell™** family. Using this approach, minimum feature sizes, an inverse indicator of performance and complexity, have been successfully reduced from 3-μm used in the CircuitCell™ family to 2-μm in the **SystemCell™** family, with a 1-μm family already on the horizon!

In designing the **SystemCell™** family, TI's ASIC development team was directed by the people who made TTL an industry standard and who then went on to invent Low Power Schottky† (LS-TTL). They were determined that TI's standard cell products should be easier to design with, and as well specified as conventional standard logic circuits.

Designers familiar with the industry standard SN54/74 TTL functions will immediately appreciate the easy transition to standard cell design. These same popular logic functions are replicated in TI's standard cell libraries. Wherever possible, the same function number as the standard product has been used. For example, if the 'LS244 is the function you need, simply select the 'ASC244—it's the same function!

The similarity with industry standard logic functions does not end with type numbers. Each individual **SystemCell™** data sheet presents the cell data in a format similar to the corresponding standard device data sheet and contains comprehensive, solid specifications (min's and max's over the full temperature range, not just typical values). In fact, just like TTL and LS-TTL, TI's **SystemCell™** family provides data you can depend on!

From design concept to a completed design, TI's Regional Technology Centers offer a worldwide network of customer and design support services. Local design support capabilities also are available through TI's authorized ASIC distributors across North America. In addition, **SystemCell™** is supported on many of the popular engineering workstations to allow maximum utilization of existing in-house design tools for those wishing to complete the design themselves.

To learn more about TI's **SystemCell™** family, the most comprehensively specified, fastest growing cell library in the industry, please read on.

† Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U.S. Patent Number 3,463,975

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CELL CROSS-REFERENCE

CROSS-REFERENCE INDEX

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HDL or cell names that start with an S (i.e., SxxxLH) are SOFTWARE MACROS.

INVERTERS AND BUFFERS (Delay at 1-pF Load)

DESCRIPTION	TYPE	TYPICAL DELAY (ns)	HDL OR CELL NAME	RELATIVE DRIVE FACTOR	COMMENTS
Buffers	'ASC2321	3.0	BU110LH	1X	Noninverting
		4.0	BU111LH	1X	Inverting
		3.0	BU112LH	1X	Noninverting
Delay Control	'ASC2508		DLC10LH	2X	
Delay Element	'ASC2507	3.0 to 12.0	DLE10LH	1X	Noninverting
Inverters	'ASC04	1.7	IV110LH	1X	
		1.1	IV120LH	2X	
		0.9	IV130LH	3X	
		0.8	IV140LH	4X	
		0.7	IV160LH	6X	
		0.6	IV180LH	8X	
		2.3	IV101LH	10X	
Inverting 3-State Buffers	'ASC2310	2.6	IV211LH	1X	Active-Low Enable
		1.7	IV221LH	2X	
		1.3	IV241LH	4X	
	'ASC2311	2.6	IV212LH	1X	Active-High Enable
		1.8	IV222LH	2X	
		1.3	IV242LH	4X	
Noninverting Delay Buffers	'ASC6120	1.7	BU120LH	2X	Delay
		1.7	BU130LH	3X	
	'ASC6121	2.3	BU221LH	2X	Active-Low Enable
		2.0	BU261LH	6X	
	'ASC6122	2.3	BU222LH	2X	Active-High Enable
		2.0	BU262LH	6X	

POSITIVE-NAND GATES (Delay at 1-pF Load)

DESCRIPTION	TYPE	TYPICAL DELAY (ns)	HDL OR CELL NAME	RELATIVE DRIVE FACTOR
2-Input NAND	'ASC00	2.0	NA210LH	1X
		1.3	NA220LH	2X
		1.1	NA230LH	3X
		1.0	NA240LH	4X
		0.8	NA260LH	6X
3-Input NAND	'ASC10	2.2	NA310LH	1X
		1.5	NA320LH	2X
		1.3	NA330LH	3X
		1.1	NA340LH	4X
4-Input NAND	'ASC20	2.6	NA410LH	1X
		1.8	NA420LH	2X
		1.5	NA430LH	3X
5-Input NAND	'ASC2022	2.7	NA510LH	1X
		2.1	NA520LH	2X
8-Input NAND	'ASC30	4.5	NA810LH	1X
		3.3	NA820LH	2X

POSITIVE-NOR GATES (Delay at 1-pF Load)

DESCRIPTION	TYPE	TYPICAL DELAY (ns)	HDL OR CELL NAME	RELATIVE DRIVE FACTOR
2-Input NOR	'ASC02	2.4	NO210LH	1X
		1.5	NO220LH	2X
		1.3	NO230LH	3X
		1.1	NO240LH	4X
3-Input NOR	'ASC27	3.2	NO310LH	1X
		2.1	NO320LH	2X
		1.8	NO330LH	3X
4-Input NOR	'ASC4002	4.1	NO410LH	1X
		2.6	NO420LH	2X
5-Input NOR	'ASC260	5.0	NO510LH	1X
		3.2	NO520LH	2X
8-Input NOR	'ASC4078	3.4	NO810LH	1X
		4.9	NO820LH	2X

POSITIVE-AND GATES (Delay at 1-pF Load)

DESCRIPTION	TYPE	TYPICAL DELAY (ns)	HDL OR CELL NAME	RELATIVE DRIVE FACTOR
2-Input AND	'ASC08	2.1	AN210LH	1X
		1.9	AN220LH	2X
		2.1	AN240LH	4X
		1.7	AN260LH	6X
3-Input AND	'ASC11	2.4	AN310LH	1X
		2.2	AN320LH	2X
		2.5	AN340LH	4X
		1.9	AN360LH	6X
4-Input AND	'ASC21	2.6	AN410LH	1X
		2.5	AN420LH	2X
		2.7	AN440LH	4X
		2.3	AN460LH	6X
5-Input AND	'ASC2024	2.9	AN510LH	1X
8-Input AND	'ASC6132	3.4	AN810LH	1X

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POSITIVE-OR GATES (Delay at 1-pF Load)

DESCRIPTION	TYPE	TYPICAL DELAY (ns)	HDL OR CELL NAME	RELATIVE DRIVE FACTOR
2-Input OR	'ASC32	2.3	OR210LH	1X
		2.1	OR220LH	2X
		1.8	OR240LH	4X
		1.7	OR260LH	6X
3-Input OR	'ASC4075	2.7	OR310LH	1X
		2.7	OR320LH	2X
		2.2	OR340LH	4X
		2.2	OR360LH	6X
4-Input OR	'ASC4072	3.1	OR410LH	1X
		3.1	OR420LH	2X
		2.7	OR440LH	4X
		2.7	OR460LH	6X
5-Input OR	'ASC6130	3.4	OR510LH	1X
8-Input OR	'ASC6131	3.3	OR810LH	1X

EXCLUSIVE-OR, -NOR, -AND-OR GATES (Delay at 1-pF Load)

DESCRIPTION	TYPE	TYPICAL DELAY (ns)	HDL OR CELL NAME	RELATIVE DRIVE FACTOR	COMMENTS
Exclusive-OR	'ASC86	2.3	EX210LH	1X	
		2.0	EX220LH	2X	
		2.0	EX240LH	4X	
Exclusive-NOR	'ASC266	2.4	EN210LH	1X	
AND-NOR	'ASC2330	2.6	AO221LH	1X	2-Wide, 2-Input
AND-OR	'ASC2331	2.6	AO220LH	1X	2-Wide, 2-Input

ANALOG FUNCTIONS

DESCRIPTION	TYPE	INPUT	CELL NAME
Crystal-Controlled Oscillator	'ASC2500	Crystal	OSE00LH
		Crystal	OSF02LH
		Crystal	OSE06LH
RC Oscillator	'ASC2502	RC	OSE03LH
Comparator	'ASC2503	P-Chan	CO212LH
		N-Chan	CO213LH
Delay Element	'ASC2507	P-Chan	DLE10LH
		N-Chan	
Delay Control	'ASC2508	P-Chan	DLC10LH
		N-Chan	
Medium-Drive Operational Amplifier	'ASC2519	Op-Amp	AMC12NH

BOOLEAN FUNCTIONS (Delay at 1-pF Load)

DESCRIPTION	TYPE	TYPICAL DELAY (ns)	HDL OR CELL NAME	EQUATION
AND-NOR	'ASC6002	2.7	BF002LH	$Y = \overline{A1 + (B1 \cdot B2 \cdot B3)}$
	'ASC6003	2.6	BF003LH	$Y = \overline{(A1 \cdot A2) + (B1 \cdot B2)}$
	'ASC6004	2.8	BF004LH	$Y = \overline{(A1 \cdot A2) + (B1 \cdot B2 \cdot B3)}$
	'ASC6005	3.0	BF005LH	$Y = \overline{(A1 \cdot A2 \cdot A3) + (B1 \cdot B2 \cdot B3)}$
	'ASC6006	3.2	BF006LH	$Y = \overline{A1 + A2 + (B1 \cdot B2)}$
	'ASC6007	3.7	BF007LH	$Y = \overline{A1 + A2 + (B1 \cdot B2 \cdot B3)}$
	'ASC6008	3.4	BF008LH	$Y = \overline{A1 + (B1 \cdot B2) + (C1 \cdot C2)}$
	'ASC6009	3.7	BF009LH	$Y = \overline{A1 + (B1 \cdot B2) + (C1 \cdot C2 \cdot C3)}$
	'ASC6012	3.7	BF012LH	$Y = \overline{(A1 \cdot A2) + (B1 \cdot B2) + (C1 \cdot C2 \cdot C3)}$
	'ASC6013	4.1	BF013LH	$Y = \overline{(A1 \cdot A2) + (B1 \cdot B2 \cdot B3) + (C1 \cdot C2 \cdot C3)}$
	'ASC6014	4.3	BF014LH	$Y = \overline{(A1 \cdot A2 \cdot A3) + (B1 \cdot B2 \cdot B3) + (C1 \cdot C2 \cdot C3)}$
	'ASC6017	2.5	BF001LH	$Y = \overline{A1 + (B1 \cdot B2)}$
	'ASC6018	3.9	BF010LH	$Y = \overline{A1 + (B1 \cdot B2 \cdot B3) + (C1 \cdot C2 \cdot C3)}$
	'ASC6019	3.5	BF011LH	$Y = \overline{(A1 \cdot A2) + (B1 \cdot B2) + (C1 \cdot C2)}$
OR-AND-NOR	'ASC6022	3.9	BF022LH	$Y = \overline{A1 \cdot A2 + [B1 \cdot B2 \cdot (C1 + C2)]}$
	'ASC6023	3.2	BF015LH	$Y = \overline{A1 + [B1 \cdot (C1 + C2)]}$
	'ASC6024	3.4	BF016LH	$Y = \overline{A1 + [(B1 + B2) \cdot (C1 + C2)]}$
	'ASC6025	3.5	BF025LH	$Y = \overline{A1 \cdot A2 \cdot A3 + [B1 \cdot (C1 + C2)]}$
	'ASC6026	3.7	BF017LH	$Y = \overline{A1 + [B1 \cdot B2 \cdot (C1 + C2)]}$
	'ASC6027	3.6	BF027LH	$Y = \overline{A1 \cdot A2 \cdot A3 + [B1 \cdot B2 \cdot (C1 + C2)]}$
	'ASC6028	3.6	BF028LH	$Y = \overline{A1 \cdot A2 \cdot A3 + [B1 \cdot (C1 + C2) \cdot (D1 + D2)]}$
	'ASC6029	3.4	BF020LH	$Y = \overline{A1 \cdot A2 + [B1 \cdot (C1 + C2)]}$
AND-OR-AND-NOR	'ASC6032	3.9	BF030LH	$Y = \overline{A1 + \{B1 \cdot [C1 + (D1 \cdot D2)]\}}$
	'ASC6034	3.6	BF034LH	$Y = \overline{(A1 \cdot A2) + \{B1 \cdot [C1 + (D1 \cdot D2)]\}}$
	'ASC6035	3.3	BF035LH	$Y = \overline{(A1 \cdot A2) + \{B1 \cdot [(C1 \cdot C2) + (D1 \cdot D2)]\}}$
OR-NAND	'ASC6048	2.4	BF051LH	$Y = \overline{A1 \cdot (B1 + B2)}$
	'ASC6049	3.8	BF060LH	$Y = \overline{A1 \cdot (B1 + B2 + B3) \cdot (C1 + C2 + C3)}$
	'ASC6052	3.2	BF052LH	$Y = \overline{A1 \cdot (B1 + B2 + B3)}$
	'ASC6053	2.6	BF053LH	$Y = \overline{(A1 + A2) \cdot (B1 + B2)}$
	'ASC6054	3.0	BF054LH	$Y = \overline{(A1 + A2) \cdot (B1 + B2 + B3)}$
	'ASC6055	3.3	BF055LH	$Y = \overline{(A1 + A2 + A3) \cdot (B1 + B2 + B3)}$
	'ASC6056	2.9	BF056LH	$Y = \overline{A1 \cdot A2 \cdot (B1 + B2)}$
	'ASC6057	3.7	BF057LH	$Y = \overline{A1 \cdot A2 \cdot (B1 + B2 + B3)}$
	'ASC6058	3.0	BF058LH	$Y = \overline{A1 \cdot (B1 + B2) \cdot (C1 + C2)}$
	'ASC6059	3.5	BF059LH	$Y = \overline{A1 \cdot (B1 + B2) \cdot (C1 + C2 + C3)}$
	'ASC6062	4.1	BF062LH	$Y = \overline{(A1 + A2) \cdot (B1 + B2) \cdot (C1 + C2 + C3)}$
	'ASC6063	4.2	BF063LH	$Y = \overline{(A1 + A2) \cdot (B1 + B2 + B3) \cdot (C1 + C2 + C3)}$
	'ASC6064	4.1	BF064LH	$Y = \overline{(A1 + A2 + A3) \cdot (B1 + B2 + B3) \cdot (C1 + C2 + C3)}$

NOTE: All have 1X drive factor.

BOOLEAN FUNCTIONS (Delay at 1-pF Load) (continued)

DESCRIPTION	TYPE	TYPICAL DELAY (ns)	HDL OR CELL NAME	EQUATION
AND-OR-NAND	'ASC6065	2.8	BF065LH	$Y = \overline{A1 \cdot [B1 + (C1 \cdot C2)]}$
	'ASC6066	2.9	BF066LH	$Y = \overline{A1 \cdot [(B1 \cdot B2) + (C1 \cdot C2)]}$
	'ASC6067	3.7	BF067LH	$Y = \overline{A1 \cdot (B1 + B2 + (C1 \cdot C2))}$
	'ASC6068	4.0	BF068LH	$Y = \overline{A1 \cdot [B1 + (C1 \cdot C2) + (D1 \cdot D2)]}$
	'ASC6069	4.2	BF069LH	$Y = \overline{A1 \cdot [(B1 \cdot B2) + (C1 \cdot C2) + (D1 \cdot D2)]}$
	'ASC6072	3.8	BF072LH	$Y = \overline{(A1 + A2) \cdot [B1 + B2 + (C1 \cdot C2)]}$
	'ASC6073	2.9	BF070LH	$Y = \overline{(A1 + A2) \cdot [B1 + (C1 \cdot C2)]}$
	'ASC6074	3.1	BF071LH	$Y = \overline{(A1 + A2) \cdot [(B1 \cdot B2) + (C1 \cdot C2)]}$
	'ASC6075	2.5	BF075LH	$Y = \overline{(A1 + A2 + A3) \cdot [B1 + (C1 \cdot C2)]}$
OR-AND-OR-NAND	'ASC6082	3.8	BF082LH	$Y = \overline{A1 \cdot [(B1 \cdot B2) + [C1 \cdot (D1 + D2)]]}$
	'ASC6083	3.7	BF080LH	$Y = \overline{A1 \cdot [B1 + [C1 \cdot (D1 + D2)]]}$
	'ASC6084	3.9	BF081LH	$Y = \overline{A1 \cdot [B1 + [(C1 + C2) \cdot (D1 + D2)]]}$
	'ASC6088	4.1	BF088LH	$Y = \overline{(A1 + A2 + A3) \cdot [B1 + [C1 \cdot (D1 + D2)]]}$

NOTE: All have 1X drive factor.

SPECIAL FUNCTIONS

DESCRIPTION	TYPE	HDL OR CELL NAME	COMMENTS
Power-Up Clear	'ASC2320	PUC00LH	4X Drive
Tie-Off Cell for Buffered Logical I/O	'ASC2325	TO010LH	ESD-Protected

BUS TRANSCEIVERS

DESCRIPTION	MACRO	OUTPUT	TYPICAL DELAY (ns)	HDL OR CELL NAME	COMMENTS
Octal	'ASC245	3-State	5.0	S245LH	
Bidirectional and Universal	'ASC651	3-State	10.4	S651LH	Inverted Data
	'ASC652	3-State	10.4	S652LH	True Data

DRIVERS

DESCRIPTION	MACRO	OUTPUT	TYPICAL DELAY (ns)	HDL OR CELL NAME	COMMENTS
Octal	'ASC244	3-State	2.4	S244LH	True Data

INPUT BUFFER CELLS (Delay at 1-pF Load)

TTL THRESHOLD

DESCRIPTION	MACRO	TYPICAL DELAY (ns)	HDL OR CELL NAME	RELATIVE DRIVE FACTOR	COMMENTS
Inverting	'ASC5001	2.1	IPE03LH	1X	
		2.1	IPF03LH	1X	
	'ASC5003	7.5	IPE08LH	1X	With Hysteresis
		8.1	IPF08LH	1X	With Hysteresis
	'ASC5005	2.1	IPE05LH	1X	With Pull-Up Tap
		2.1	IPF05LH	1X	With Pull-Up Tap
	'ASC5010	7.5	IPE10LH	1X	With Hysteresis
		7.5	IPF10LH	1X	and Pull-Up Tap
Noninverting	'ASC5007	2.1	IPE04LH	1X	
		2.1	IPF04LH	1X	
		1.6	IPF12LH	1X	
	'ASC5013	2.1	IPF13LH	1X	With Pull-Up Tap

INPUT BUFFER CELLS (Delay at 1-pF Load)

CMOS THRESHOLD

DESCRIPTION	MACRO	TYPICAL DELAY (ns)	HDL OR CELL NAME	RELATIVE DRIVE FACTOR	COMMENTS
Inverting	'ASC5000	1.1	IPE00LH	1X	
		1.1	IPF00LH	1X	
	'ASC5002	4.8	IPE06LH	1X	With Hysteresis
		4.8	IPF06LH	1X	With Hysteresis and Pull-Up Tap
	'ASC5004	1.0	IPF02LH	1X	With Pull-Up Tap
Noninverting	'ASC5006	1.9	IPE01LH	1X	
		1.1	IPF01LH	1X	

NOTE: IPE = Minimum Height; IPF = Minimum Width

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NONINVERTING OUTPUT BUFFER CELLS (Delay at 15-pF Load)

DESCRIPTION	TYPE	TYPICAL DELAY (ns)	HDL OR CELL NAME	OUTPUT CURRENT			
				I_{OL}(mA)		I_{OH}(mA)	
				54	74	54	74
Push-Pull	'ASC5100	2.7	OPE40LH	3.4	4.0	−3.4	−4.0
		2.7	OPF40LH	3.4	4.0	−3.4	−4.0
	'ASC5103	2.4	OPE60LH	5.1	6.0	−5.1	−6.0
		2.4	OPF60LH	5.1	6.0	−5.1	−6.0
	'ASC5106	2.0	OPE00LH	8.5	10.0	−8.5	−10.0
		2.0	OPF00LH	8.5	10.0	−8.5	−10.0
	'ASC5110	3.4	OPE42LH	3.2	4.0	−3.2	−4.0
		3.4	OPF42LH	3.2	4.0	−3.2	−4.0
	'ASC5120	1.7	OPFB0LH	20.4	24.0	−10.2	−12.0
3-State	'ASC5104	2.7	OPE63LH	5.1	6.0	−5.1	−6.0
		2.7	OPF63LH	5.1	6.0	−5.1	−6.0
	'ASC5107	2.7	OPE03LH	8.5	10.0	−8.5	−10.0
		2.7	OPF03LH	8.5	10.0	−8.5	−10.0
	'ASC5111	3.5	OPE43LH	3.4	4.0	−3.4	−4.0
		3.5	OPF43LH	3.4	4.0	−3.4	−4.0
	'ASC5124	2.5	OPFD3LH	37.4	44.0	−10.2	−12.0
	'ASC5125	2.8	OPFB3LH	20.4	24.0	−10.2	−12.0
Open Drain	'ASC5105	2.0	OPE61LH	5.1	6.0	—	—
		2.0	OPF61LH	5.1	6.0	—	—
	'ASC5108	1.7	OPE01LH	8.5	10.0	—	—
		1.7	OPF01LH	8.5	10.0	—	—
	'ASC5109	2.7	OPE41LH	3.4	4.0	—	—
		2.7	OPF41LH	3.4	4.0	—	—
	'ASC5121	1.7	OPFD1LH	37.4	44.0	—	—
	'ASC5123	1.5	OPFE1LH	40.8	48.0	—	—

NOTE 1. OPE = Minimum Height; OPF = Minimum Width

CLOCK GENERATORS

DESCRIPTION	TYPE	CELL NAME	COMMENTS
2-Phase	'ASC3011	CK4X0LH	Complementary Outputs

D-TYPE FLIP-FLOPS (Delay at 1-pF Load)

DESCRIPTION	MACRO OR TYPE	f_{max} (MHz)	HDL OR CELL NAME	RELATIVE DRIVE FACTOR	COMMENTS
With Preset and Clear	'ASC74	55.8	DTB10LH	1X	D Low
		46.3	DFB20LH	2X	
		59.2	DFZ20LH	2X	
Preset Only	'ASC74	55.8	DTP10LH	1X	D Low
		55.8	DFP20LH	2X	
		69.2	DFY20LH	2X	
Clear Only	'ASC74	52.1	DTC10LH	1X	
		52.1	DFC20LH	2X	
Neither Preset nor Clear	'ASC74	55.8	DTN10LH	1X	
		64.2	DFN20LH	2X	

D-TYPE FLIP-FLOPS

DESCRIPTION	MACRO OR TYPE	TYPICAL DELAY (ns)	HDL OR CELL NAME	RELATIVE DRIVE FACTOR	COMMENTS
Quad with Q Only	'ASC173	8.0	S173LH	1X	3-State Output
Hex	'ASC174	8.0	S174LH	1X	With Clear
Quad with Q, QZ	'ASC175	5.5	S175LH	1X	With Clear
Octal	'ASC273	5.0	S273LH	1X	With Clear

TOGGLE FLIP-FLOPS, UNGATED (Delay at 1-pF Load)

DESCRIPTION	TYPE	f_{max} (MHz)	HDL OR CELL NAME	RELATIVE DRIVE FACTOR
Preset and Clear	'ASC2102	54.2	TAB20LH	2X
Clear Only	'ASC2102	61.7	TAC20LH	2X
Preset Only	'ASC2102	65.8	TAP20LH	2X

J-$\overline{K}$-TYPE FLIP-FLOPS (Delay at 1-pF Load)

DESCRIPTION	TYPE	f_{max} (MHz)	HDL OR CELL NAME	RELATIVE DRIVE FACTOR	COMMENTS
Preset and Clear	'ASC109	44.2	JKB20LH	2X	Positive-Edge Trigger
	'ASC2108	44.2	JKB21LH	2X	Negative-Edge Trigger

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LATCHES

DESCRIPTION	MACRO OR TYPE	TYPICAL DELAY (ns)	HDL OR CELL NAME	RELATIVE DRIVE FACTOR	COMMENTS
D-Type	'ASC75	2.4	LAH10LH	1X	Active-High Enable
		2.0	LAH20LH	2X	Active-High Enable
Set-Reset	'ASC6125	3.9	LAL20LH	2X	Active-Low Enable
	'ASC279	2.8	LAB10LH	1X	
		2.7	LAB20LH	2X	
4-Bit Bistable	'ASC375	4.5	S375LH	1X	
8-Bit D-Type	'ASC373	5.0	S373LH	1X	3-State Output
	'ASC374	5.0	S374LH	1X	3-State Output
8-Bit Addressable	'ASC259	6.0	S259LH	1X	Active-Low Clear

GATED S-R LATCHES (Delay at 1-pF Load)

DESCRIPTION	MACRO OR TYPE	TYPICAL DELAY (ns)	HDL OR CELL NAME	RELATIVE DRIVE FACTOR	COMMENTS
4-Input	'ASC6100	2.8	GM010LH	1X	
5-Input	'ASC6101	3.6	GM110LH	1X	Separate Reset
5-Input	'ASC6102	3.6	GMS10LH	1X	Separate Set
6-Input	'ASC6103	3.6	GM210LH	1X	Separate Set/Reset
6-Input	'ASC6105	3.0	GM310LH	1X	
7-Input	'ASC6106	4.0	GM410LH	1X	Separate Reset
8-Input	'ASC6108	4.0	GM510LH	1X	Separate Set/Reset

GATED $\overline{S}$-$\overline{R}$ LATCHES (Delay at 1-pF Load)

DESCRIPTION	MACRO OR TYPE	TYPICAL DELAY (ns)	HDL OR CELL NAME	RELATIVE DRIVE FACTOR	COMMENTS
4-Input	'ASC6110	2.7	GS010LH	1X	
5-Input	'ASC6111	3.1	GS110LH	1X	Separate Reset
5-Input	'ASC6112	3.1	GSS10LH	1X	Separate Set
6-Input	'ASC6113	3.1	GS210LH	1X	Separate Set/Reset
6-Input	'ASC6115	3.4	GS310LH	1X	
7-Input	'ASC6116	3.8	GS410LH	1X	Separate Reset
8-Input	'ASC6118	4.0	GS510LH	1X	Separate Set/Reset

OSCILLATORS AND MULTIVIBRATORS

DESCRIPTION	TYPE	HDL OR CELL NAME	COMMENTS
Crystal-Controlled Oscillator	'ASC2500	OSE00LH	5 MHz
		OSF02LH	20 MHz
		OSE06LH	800 kHz
CMOS RC Oscillator	'ASC2502	OSE03LH	1 MHz
Retriggerable One-Shot	'ASC2322	MVF00LH	With Clear

4-BIT EXPANDABLE REGISTERS—POSITIVE-EDGE-TRIGGERED

DESCRIPTION	MACRO OR TYPE	OUTPUT	f_{max} (MHz)	HDL OR CELL NAME	COMMENTS
Serial Input/ Parallel Output	'ASC2401	Qn	59.6	R2401LH	Async Clear
Serial Input	'ASC2402	Qn, QnZ	59.6	R2402LH	Async Clear
Parallel Input/ Parallel Output	'ASC2403	Qn	59.6	R2403LH	Async Clear
Parallel Input	'ASC2404	Qn, QnZ	59.6	R2404LH	Async Clear

4-BIT EXPANDABLE REGISTERS—POSITIVE-EDGE-TRIGGERED

DESCRIPTION	MACRO OR TYPE	OUTPUT	TYPICAL DELAY (ns)	HDL OR CELL NAME	COMMENTS
Parallel Access	'ASC195A	Qn	5.5	S195ALH	Async Clear J-K Input First Stage
Parallel Input/ Parallel Output	'ASC194A	Qn	5.0	S194ALH	Bidirectional Shift Async Clear

8-BIT EXPANDABLE REGISTERS—POSITIVE-EDGE-TRIGGERED

DESCRIPTION	MACRO OR TYPE	OUTPUT	TYPICAL DELAY (ns)	HDL OR CELL NAME	COMMENTS
Serial Input/ Parallel Output	'ASC164	Qn	5.0	S164LH	Async Clear
	'ASC595	3-State	5.5	S595LH	Registered Outputs
Parallel Input/ Parallel Output	'ASC598X	3-State QH, QHZ	9.8	S598XLH	Input Latches
Parallel Input/ Serial Output	'ASC165	QH, QHZ	8.0	S165LH	Async Load
Parallel or Serial Input/ Serial Output	'ASC166	QH	6.0	S166LH	Async Clear Sync Load
Universal and Bidirectional	'ASC299	3-State I/O	7.1	S299LH	Async Clear Sync Load Multiplexed I/O
	'ASC299X	Separate I/O	5.0	S299XLH	Async Clear Sync Load

REGISTER FILE

DESCRIPTION	TYPE	TYPICAL ACCESS TIME (ns)	CELL NAME	COMMENTS
16-Word by 8-Bit	'ASC3103	8	RF408LH	Typical Cycle Time = 11 ns

4-BIT COUNTERS—POSITIVE-EDGE-TRIGGERED (RIPPLE COUNT)

DESCRIPTION	MACRO OR TYPE	OUTPUT	f_{max} (MHz)	HDL OR CELL NAME	COMMENTS
D-Type	'ASC2405	Qn	64.2	R2405LH	Async Clear
	'ASC2406	Qn, QnZ	64.2	R2406LH	Async Clear
	'ASC2407	3-State	36.3	R2407LH	Async Clear
Ripple Up	'ASC2408	Qn	59.6	R2408LH	Async Clear

4-BIT COUNTERS—POSITIVE-EDGE-TRIGGERED (RIPPLE COUNT)

DESCRIPTION	MACRO OR TYPE	OUTPUT	TYPICAL DELAY (ns)	HDL OR CELL NAME	COMMENTS
Programmable Divide by 2/8	'ASC177	Qn	22	S177LH	Async Clear
Dual 4-Bit	'ASC393	Qn1, Qn2	21	S393LH	Async Clear

SYNCHRONOUS COUNTERS—POSITIVE-EDGE-TRIGGERED

DESCRIPTION	MACRO	PARALLEL LOAD	TYPICAL DELAY (ns)	HDL OR CELL NAME	COMMENTS
4-Bit Binary	'ASC161A	Sync	12.0	S161ALH	Async Clear
	'ASC163A	Sync	9.0	S163ALH	Sync Clear
4-Bit Up/Down	'ASC191	Async	11.5	S191LH	With Mode Control
	'ASC193	Async	11.5	S193LH	Dual Clock
	'ASC669	Sync	10.0	S669LH	Internal Look-Ahead/Carry
8-Bit Binary	'ASC590	None	10.4	S590LH	Output Registers
	'ASC593X	Sync	10.0	S593XLH	Input Registers

DECODERS

DESCRIPTION	MACRO OR TYPE	TYPICAL DELAY (ns)	HDL OR CELL NAME	RELATIVE DRIVE FACTOR	COMMENTS
2- to 4-Line	'ASC2350	2.0	DE210LH	1X	
		2.5	DE212LH	1X	Active-Low Enable
3- to 8-Line	'ASC137	12.0	S137LH	1X	Latches
	'ASC138	7.0	S138LH	1X	3 Enables
Dual 2- to 4-Line	'ASC139	4.0	S139LH	1X	1 Enable

MULTIPLEXERS

DESCRIPTION	MACRO OR TYPE	OUTPUT	TYPICAL DELAY (ns)	HDL OR CELL NAME	COMMENTS
2- to 1-Line	'ASC2340	Y	3.7	MU110LH	Active-Low Enable
Dual 2- to 4-Line	'ASC155	Y1n, Y2n	5.0	S155LH	Active-Low Enable
Quad 2- to 1-Line	'ASC157	Yn	6.0	S157LH	
	'ASC158	Yn	6.2	S158LH	
	'ASC257A	Yn	5.0	S257ALH	3-State
	'ASC258A	Yn	5.0	S258ALH	3-State
	'ASC298	Qn	6.0	S298LH	Storage Latches
	'ASC398	Qn, QnZ	5.5	S398LH	Storage Latches
	'ASC399	Qn	5.0	S399LH	Storage Latches
4- to 1-Line	'ASC2341	Y	2.9	MU210LH	No Enable
Dual 4- to 1-Line	'ASC153	Yn	8.0	S153LH	Strobe
8- to 1-Line	'ASC151	Y, W	8.0	S151LH	Low Enable
	'ASC251	3-State	9.7	S251LH	Low Enable
	'ASC2342	Y	4.7	MU310LH	Active-Low Enable

NOTE: All have 1X drive factor.

PROGRAMMABLE DELAY ELEMENTS

DESCRIPTION	TYPE	TYPICAL DELAY RANGE	CELL NAME
Delay Element	'ASC2507	3 to 12 ns	DLE10LH
Control Element	'ASC2508		DLC10LH

OSCILLATORS AND MULTIVIBRATORS

DESCRIPTION	TYPE	HDL OR CELL NAME	COMMENTS
Crystal-Controlled Oscillator	'ASC2500	OSE00LH	5 MHz
		OSF02LH	20 MHz
		OSE06LH	800 kHz
CMOS RC Oscillator	'ASC2502	OSE03LH	1 MHz
Retriggerable One-Shot	'ASC2322	MVF00LH	With Clear

MAGNITUDE COMPARATORS AND ARITHMETIC CIRCUITS

DESCRIPTION	MACRO	BIT WIDTH	TYPICAL DELAY (ns)	HDL OR CELL NAME	COMMENTS
ALU	'ASC181	4	12.0	S181LH	
Binary Full Adder	'ASC283	4	8.5	S283LH	
Parity Generator	'ASC280	9	11.0	S280LH	
Comparator	'ASC85	4	12.0	S85LH	P = Q, P < Q, P > Q
	'ASC686	8	9.0	S686LH	P = Q, P > Q
Identity Comparator	'ASC688	8	7.5	S688LH	P = Q

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BIT-SLICE PROCESSOR ELEMENTS

DESCRIPTION	TYPE
8-Bit Processor Slice	'ASC888
14-Bit Microsequencer	'ASC890
4-Bit Microprocessor Slice	'ASC2901
Look-Ahead Carry Generator	'ASC2902
Status and Shift Controller	'ASC2904
12-Bit Microprogram Controller (Microsequencer)	'ASC2910

STATIC RANDOM ACCESS MEMORIES

DESCRIPTION	ORGANIZATION	TYPE	HDL OR CELL NAME
256-Bit	16 × 16	'ASC3003	RA416LH
512-Bit	64 × 8	'ASC3004	RA608LH
1024-Bit	256 × 4	'ASC3005	RA804LH
	128 × 8	'ASC3006	RA708LH

BIDIRECTIONAL 3-STATE NONINVERTING I/O CELLS (Delay at 15-pF Load)

INPUT	INV/TRUE	TYPE	TYPICAL DELAY (ns)	HDL OR CELL NAME	OUTPUT CURRENT			
					I_{OL} (mA)		I_{OH} (mA)	
					54	74	54	74
CMOS	Inverting	'ASC5200	3.3	IOE40LH	3.4	4.0	−3.4	−4.0
			3.3	IOF40LH	3.4	4.0	−3.4	−4.0
	Inverting	'ASC5202	3.6	IOF47LH	3.4	4.0	−3.4	−4.0
	True	'ASC5203	3.3	IOF48LH	3.4	4.0	−3.4	−4.0
	True	'ASC5206	3.3	IOE41LH	3.4	4.0	−3.4	−4.0
			3.3	IOF41LH	3.4	4.0	−3.4	−4.0
	Inverting	'ASC5220	2.9	IOE00LH	8.5	10.0	−8.5	−10.0
			2.9	IOF00LH	8.5	10.0	−8.5	−10.0
	Inverting	'ASC5221	2.7	IOF03LH	8.5	10.0	−8.5	−10.0
	True	'ASC5226	2.7	IOF01LH	8.5	10.0	−8.5	−10.0
	Inverting	'ASC5250	1.7	IOFD0LH	37.4	−44.0	—	—
TTL	Inverting	'ASC5201	3.5	IOE43LH	3.4	4.0	−3.4	−4.0
			3.5	IOF43LH	3.4	4.0	−3.4	−4.0
	True	'ASC5207	3.5	IOE44LH	3.4	4.0	−3.4	−4.0
			3.5	IOF44LH	3.4	4.0	−3.4	−4.0
	True	'ASC5217	2.7	IOF64LH	5.1	6.0	−5.1	−6.0
	True	'ASC5227	2.7	IOF04LH	8.5	10.0	−8.5	−10.0
	True	'ASC5239	2.7	IOFB8LH	20.4	24.0	−10.2	−12.0
	Inverting	'ASC5246	2.5	IOFD8LH	37.4	44.0	−10.2	−12.0

NOTE: IOE = Minimum Height; IOF = Minimum Width

INPUT/OUTPUT TERMINATING NETWORKS

DESCRIPTION	TYPE	SUPPLY CURRENT	HDL OR CELL NAME	COMMENTS
Active Pull-Up	'ASC2370	400 μA	PR400LH	Input or I/O with Tap
	'ASC2371	200 μA	PR250LH	
	'ASC2372	95 μA	PR095LH	
	'ASC2374	5 μA	PR005LH	
Active Pull-Down	'ASC2373	95 μA	PD095LH	

CompilerCell™ MEMORIES/REGISTERS

DESCRIPTION	TYPE	NUMBER OF WORDS	WORD LENGTH IN BITS	TOTAL NUMBER OF BITS
Static Random Access Memories	'ASC3010	4 to 1024	4 to 32	16 to 16384
Read-Only Memories—Single Array	'ASC3200	8 to 2048	4 to 32	512 to 16384
Read-Only Memories—Double Array	'ASC3200	8 to 4096	4 to 64	512 to 65536
Pipeline Test Register	'ASC3430	—	4 to 32	4- to 32-X-n

CompilerCell™ PROGRAMMABLE LOGIC ARRAYS

DESCRIPTION	TYPE	INPUTS	PRODUCT TERMS	OUTPUTS
Programmable Logic Arrays	'ASC3800	64	128	32

INTRODUCTION TO STANDARD CELLS

Leadership electronic solutions protect the unique value designed into your products. Using Texas Instruments **SystemCell**™ standard cells, you implement simple custom semiconductor solutions for your specific market opportunities. These custom solutions, also called Application Specific Integrated Circuits (ASICs), lock in the powerful combination of personalized electronics and increased system efficiency. Some benefits are

SystemCell™ FEATURES	**SYSTEM BENEFITS**
Custom design	Improves your market value by — Reducing cycle time — Reducing product development costs
Automated design process	Improves your market execution by — Reducing design resources — Enhancing market entry point
Selected density and package	Simplifies your system design by — Providing optimal circuit size — Reducing package count — Controlling costs — Improving reliability
Selected performance	Enhances your market appeal by — Providing timely application solutions — Using your specific functions — Integrating TI's custom circuits.

Using TI's standard cells greatly simplifies custom IC implementation. The **SystemCell**™ standard-cell family not only includes a number of the familiar TTL and HCMOS logic functions, but it also provides new and higher density standard-cell logic functions. When used in conjunction with computer-based workstations, the custom IC schematic is electronically captured for implementation in an automated chip-layout process. This combination is currently the most cost effective for achieving personalized, high-complexity semiconductor solutions.

Electronic workstations are the key to simplified, high-complexity IC design. Typically, the workstations incorporate high-level design tools to simplify component selection, schematic evaluation, and functional verification. Simulation tools, resident on most workstations, perform the equivalent of circuit breadboarding and debugging. Once the circuit design is complete, workstation utility software supplied by TI generates data base files containing both hardware and test descriptions. The data base is used as a source for generating the chip layout and testing the fabricated devices.

Custom ICs can be designed using one of many popular workstations or one of several personal computer systems. Once you decide on a workstation, you need only place one phone call to receive a copy of the TI documentation and software needed to begin a TI **SystemCell**™ design. If you decide not to invest in or use your own workstation, you can begin your standard-cell design with a sketch, and TI can work with you to complete the rest. Using TI's **SystemCell**™ family, you can decide how many, or how few, standard-cell design tasks you wish to perform.

TI has defined a variety of customer support and interface programs structured specifically for the most beneficial application of your resources. A description of these interface points is provided in the standard-cell design overview.

Customer Support

To assist you with a standard-cell IC design, TI has seven North American Regional Technology Centers (RTCs) staffed with experienced design personnel. The RTC staff can work with you to coordinate design specification development and implementation.

Total system design support is available at the RTC. A number of electronic workstations are available with a direct high-speed computer link to the TI design automation center in Dallas, Texas.

The RTC also provides assistance in the use of the TI standard-cell library, including installation, training, and library updates.

Once you have decided on a standard-cell approach, the RTC designers are available to perform the engineering design and test development. You decide the amount of work the RTC will do and the amount you will do. The more tasks you perform, the fewer charges there will be for nonrecurring engineering (NRE) work associated with IC design. The RTC can perform pre-design support, such as assisting with system analysis and circuit partitioning, as well as schematic capture and test pattern generation. Charges for these services are primarily based on fixed-fee contracts, providing predictable and manageable design costs.

In addition to RTC assistance, technical sales representatives and ASIC product specialists, located in TI sales offices, can help determine the best standard-cell IC approach.

Getting A Head Start: TI Standard-Cell Workshop

The RTC offers comprehensive training in standard-cell design using state-of-the-art design tools and software. The RTC-210 ASIC workshop is a three-day course that uses numerous lab exercises and concise lectures to introduce all phases of a standard-cell IC design. A listing of the RTC-210 course work follows.

RTC-210 ASIC Course Work Outline

Characteristics and advantages of gate arrays
Characteristics and advantages of standard cells
Semicustom design technique
Schematic capture
Packaging and interface considerations
Circuit simulation and test-pattern design
Generating a design data base using a workstation
IC layout and post-layout simulation.

Another important objective of the course is to help identify interface points and communication channels that will satisfy your specific requirements for standard-cell IC design.

The workshop is available at the nearest RTC. Or, if you have a number of designers who will be designing with standard cells, the workshop can be conducted at your facility.

The course is open to anyone interested, and the registration fee is deductible from your first standard-cell IC order. Contact the nearest TI Regional Technology Center (see listing in Table 1) to register for the workshop.

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Table 1. Texas Instruments North American Regional Technology Centers

REGION	RTC LOCATION	PHONE
West Coast – North	Santa Clara, CA	(408) 748-2220
West Coast – South	Irvine, CA	(714) 660-8140
Mid-West – North	Arlington Heights, IL	(312) 640-2909
Mid-West – South	Dallas, TX	(214) 680-5066
East Coast – North	Waltham, MA	(617) 895-9196
East Coast – South	Norcross, GA	(404) 662-7945
Canada	Nepean, Ontario	(613) 726-1970

TI SystemCell™ FAMILY

Since the IC was invented, manufacturers of electronic products have used each new advancement in integrated circuit technology to increase functionality, decrease size, enhance performance, and reduce system costs. This trend has led semiconductor producers from small-scale-integration (SSI), with only a few transistors per device, to today's very-large-scale-integration (VLSI), where a circuit consists of hundreds of thousands of transistors. These high levels of integration have required major improvements in the areas of process technology and production and fabrication techniques.

TI's **SystemCell**™ standard-cell product family takes advantage of these technological advancements to bring you high performance and functionality of custom ICs at semi-custom prices. The standard cells also offer added benefits of short design cycle time and reduced product development costs.

The TI **SystemCell**™standard-cell library includes basic gates, buffers, I/O drivers, and high-level functions called macros. These macros are supplied in two forms: a hard-wired form and a software form. Software macros of familiar TTL functions can be embedded in your design with a simple label, or they can be custom modified to enhance functionality and cost effectiveness. Hard-wired macros, providing a broad selection of predesigned and fully characterized functions, can also be included in your design with a single label.

New standard-cell functions are being added routinely to increase the effectiveness of automated design techniques. These new functions are described in the Advance Information and Product Preview sections of this book. A goal, maintained by TI, is to provide total semiconductor solutions to your needs. Requests for new cell designs will be carefully considered.

Other benefits available from the **SystemCell**™ Family are:

- CMOS or TTL compatible inputs and outputs
- Operation over V_{CC} range of 2 V to 6 V
- Specified parametrically over V_{CC} range of 4.5 V to 5.5 V
- Specified parametrically over industrial and military temperature ranges
- Internal gate propagation delays of less than 1 ns
- Flip-flop toggle frequencies up to 65.8 MHz
- Latch-up protection up to 400 mA
- Inputs and outputs designed to withstand up to 4 kV ESD, as tested using method 3015 of MIL-STD-883.
- Wide variety of package options: DIP, SOIC (D), PGA (GB) and Quad Flat-Pack.

SystemCell™ Technology

SystemCell™ products are fabricated using a twin-well polysilicon self-aligned CMOS process to produce 2-μm gate-length versions of CMOS standard cells. In this process, polysilicon is deposited over the gate oxide prior to the source and drain implants. After patterning the polysilicon gates, the source and drain are then implanted,

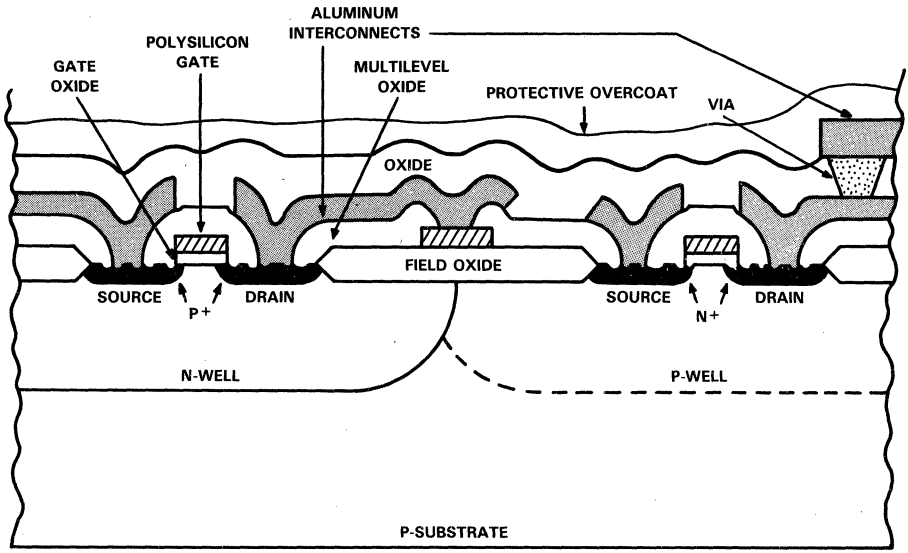

Figure 1. Cross Section of Double-Level Metal, Twin-Well CMOS Process

using the gates as the mask. This self-aligning process, illustrated in Figure 1, permits reduced junction areas, which are coupled with shallow implants to achieve several performance enhancements.

ICs created using **SystemCell**™ standard cells have speeds that meet or exceed HCMOS, Advanced HCMOS, and all but the most advanced bipolar logic characteristics. These improved speeds are due to reduced gate and junction capacitance.

Ring oscillator evaluations, shown in Figure 2, compare 2-μm CMOS gate propagation delay with 3-μm and 5-μm CMOS delays. The figure shows the technological improvements associated with high-density CMOS processes. The data are obtained from equivalent ring oscillators in which the gates are adjacent and interconnect capacitance is minimal.

The reduced power requirements of CMOS place its speed-power efficiency two orders of magnitude ahead of conventional bipolar logic families. The lower power requirements are achieved because of reduced channel lengths, more shallow junctions, smaller feature size, and lower junction capacitance of the high-density 2-μm CMOS technology.

Standard cell products from TI are characterized for performance over the full military temperature range of -55°C to 125°C and the industrial temperature range of -40°C to 85°C.

Cell Size and Construction

Each **SystemCell**™ is a custom-designed silicon implementation of a particular logic function.

The **SystemCell**™ data sheets compare the size of each cell or macro relative to the NA210LH two-input NAND gate, shown in Figure 3. This allows you to estimate the equivalent complexity of your design.

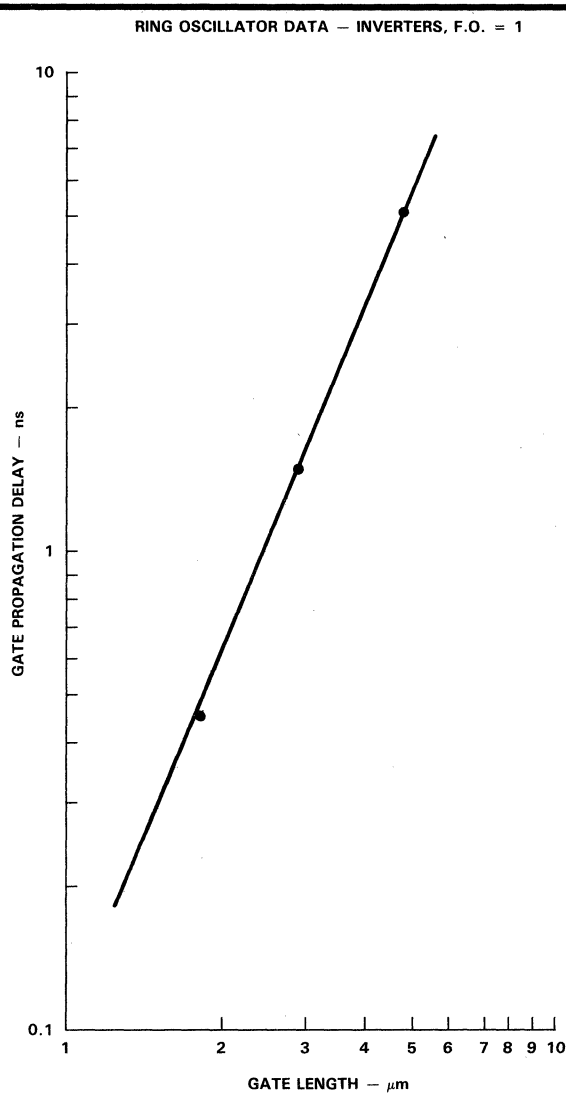

Figure 2. CMOS Performance

Within a cell, aluminum V_{CC} and ground lines run horizontally across the cell at the top and bottom as illustrated in Figure 3(A). The polysilicon gates run at right angles to the power buses, providing access to the inputs and outputs at both the top and bottom of the cell. The logic concept of the cell is shown in Figure 3(B).

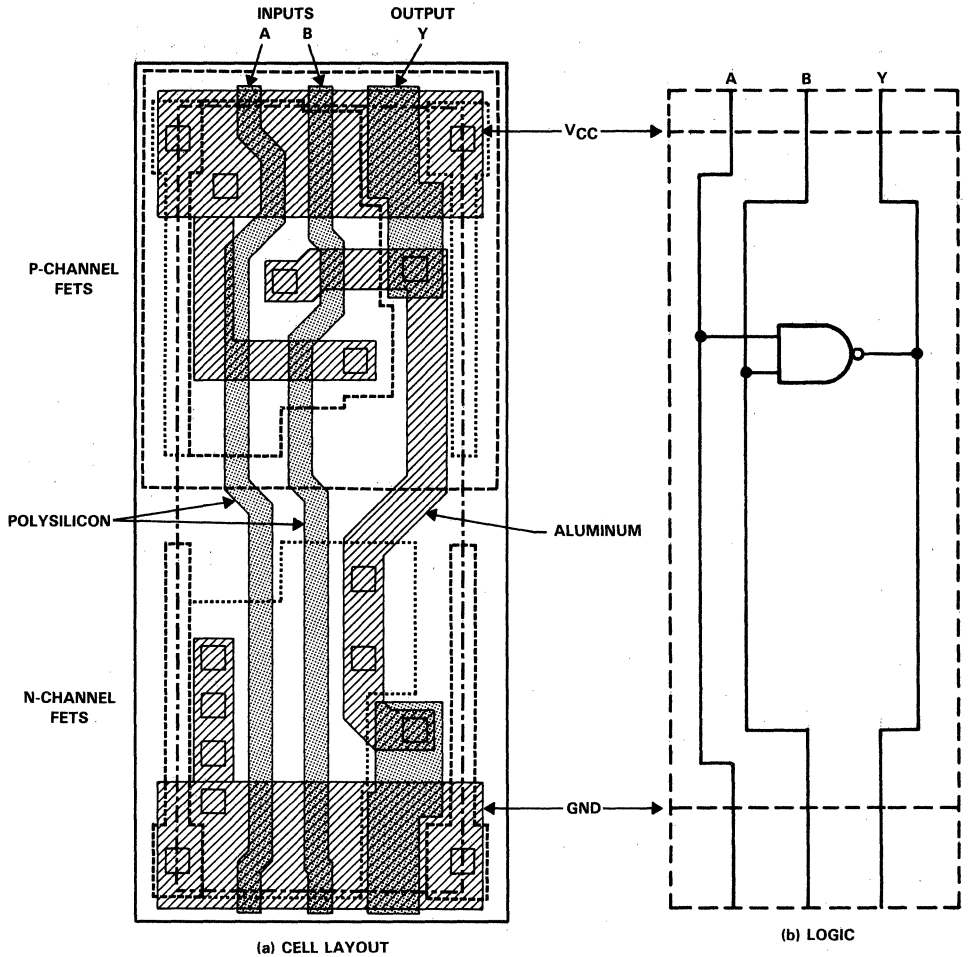

Figure 3. 2-Input NAND

This cell structure lends itself to automated layout by providing the capability of laying cells end-to-end in a continuous row of cells having a continuous power bus. High-density routing is achieved through the use of a second level of metal interconnect.

THE SystemCell™ LIBRARY

Computer-Aided Design with the Library

The **SystemCell**™ library provides full access to the latest technological advances in computer-aided design and state-of-the-art engineering workstations. A workstation employing the TI **SystemCell**™ library provides the familiar, simple entry for designing complex custom ICs.

The TI library can be installed on many popular workstations such as those available from Daisy™, Hewlett-Packard, Mentor Graphics™, and Valid Logic Systems Incorporated™. The library can also be used on PCs that support FutureNet® and P-CAD™.

The engineering workstations provide generic capabilities for schematic capture, simulation, test-vector generation, and netlist/test-vector formatting. The TI library contains five additional software programs implementing graphic, logic, delay, and interconnect capacitance models, along with data base translators. These programs are used to generate the layout and test-pattern files for your design and are then used directly by the TI design-automation system to produce the custom IC.

SystemCell™ Product Line

The **SystemCell**™ product line contains a broad functional variety of predesigned cells providing full design flexibility. The product line, ranging from simple inverters to complex LSI structures, has five classes of cells and macro functions that are used to achieve custom designs. For cell and product specifications, refer to specific data sheets in this book. A general overview of the product line is given in items 1 through 5 below.

Small-Scale Integration (SSI) Cells

SSI cells implement basic gates, Boolean and inverter functions. The hard-wired cells are modeled after the popular SN54/74HC, LS, and F series of SSI devices. Most cells in this class have a number of physical implementations providing varying levels of output drive. This permits the designer to selectively structure his system implementation for the required performance (i.e., minimum delay times or minimum power dissipations). As an example, the SN54ASC00 and SN74ASC00 offer five different drive capabilities. The optional cells are compared in Table 2. Figure 4 illustrates comparable layouts for the NA210, NA230, and NA260 cells.

Table 2. SSI Comparisons for Optional Cells

CELL NAME	RELATIVE OUTPUT DRIVE	INPUT CAPACITANCE (C_i)	TYPICAL PROPAGATION DELAY (t_{pd}) C_L = pF	INCREASE IN t_{pd} WITH ADDED CAPACITANCE (t_{pd})
NA210LH	1X	0.12	2 ns	1.1 ns/pF
NA220LH	2X	0.26	1.3 ns	0.6 ns/pF
NA230LH	3X	0.34	1.1 ns	0.4 ns/pF
NA240LH	4X	0.54	1 ns	0.3 ns/pF
NA260LH	6X	0.79	0.8 ns	0.2 ns/pF

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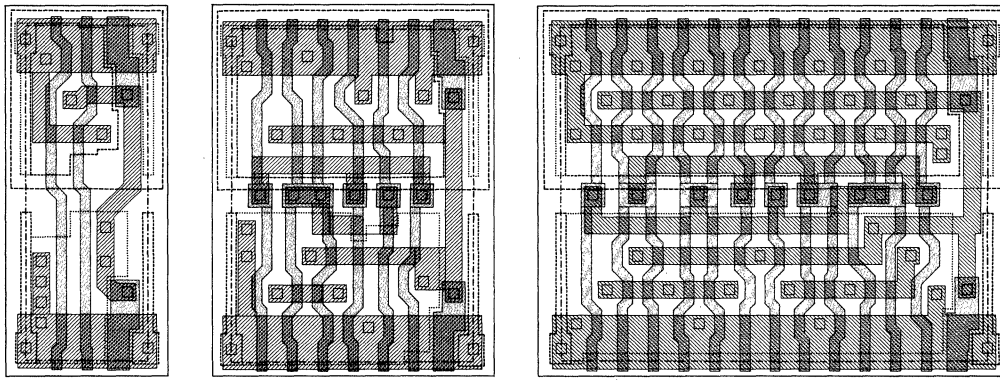

NA210NF1 NA230NF1 NA260NF1

Figure 4. Three Different Drive Layouts for 2-Input NAND Gate

Hard-Wired Medium-Scale Integration (MSI) Macro Cells

Hard-wired macros (hard macros) are dedicated designs implementing MSI-level building blocks such as flip-flops, latches, encoders, decoders, registers, 4-bit ALU, and other operator functions. They are optimized for a silicon-efficient layout.

Software Macro Functions

Predesigned pin-for-pin equivalents of 50 existing 54/74 LS,TTL and 54/74F SSI/MSI/LSI functions are implemented in the **SystemCell**™ software library. These software macros (soft macros) are library-resident netlists composed of a combination of SSI and hard-wired MSI cells. Additional user-defined software macros can be created on your workstation and added to your library under unique netlist labels.

The software macros are designated either as SN54ASC′ or as SN74ASC′, corresponding to the similar TTL prefix-numbering method described in naming conventions. Thus, an SN74ASC166 is functionally identical to the TTL SN74LS166A or the CMOS SN74HC166.

Hard-Wired Static RAM Memory Functions

The library contains four hard-wired memory organizations (see Table 3) that can be used in custom designs.

Table 3. Hard-Wired Memory Organizations for Custom Designs

DESCRIPTION	CELL NAME	ORGANIZATION	
		WORDS	BITS
256-Bit	RA416LH	16	16
512-Bit	RA608LH	64	8
1024-Bit	RA708LH	128	8
1024-Bit	RA804LH	256	4

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Input, Output, and Bidirectional I/O Functions

The **SystemCell**™ library includes ESD and latch-up protected cell designs implementing various combinations of input, output, or bidirectional I/O functions. By selecting the appropriate cell, you can interface to either TTL or CMOS voltage levels. The available buffer types and appropriate options are listed in Table 4.

Table 4. Available Buffer Types

BUFFER TYPES	OPTIONS
Input	TTL and CMOS switching thresholds Inverting or noninverting inputs with and without hysteresis and/or pullup resistors
Output	2 mA, 4 mA, 6 mA, and 10 mA current sink/source Push-Pull, 3-state, or open-drain
Bidirectional	3-state outputs; TTL or CMOS level inputs Inverting or noninverting inputs 2 mA, 4 mA, 6 mA, and 10 mA current sink/source CMOS or TTL output

Library Development

The following classes of functions are currently under development and planned for addition to future releases of the **SystemCell**™ library.

Compiler Functions

CompilerCell™ functions permit the system designer to implement custom functions simply by specifying dimensional parameters. Procedures for generating the physical layout and simulation values pertaining to the designed function are software routines that implement the specific high-level function described by the designer.

The following **CompilerCell**™ functions are available:

Static Random Access Memory (RAM)
Static Read Only Memory (ROM)
Programmable Logic Array (PLA)
Pipeline Test Register (PTR).

See the Product Preview describing each of these functions.

The following **CompilerCell**™ functions are planned:

Data Path Functions:

- Arithmetic Logic Unit (ALU)
- Adder
- Multiplexer
- Incrementer/Decrementer
- Shifter

Clock Generator.

Linear Functions

Linear function cells, integrated into the system design, can further reduce the number of ICs required at the system level. The following linear functions are in development:

Operational Amplifier (see Product Preview)
Crystal and RC Oscillators (see Product Preview)
User-Programmable Delay Elements (see Product Preview).

Digital Functions

The extent of compatible digital cells and macros offered in the TI **SystemCell**™ library will be expanded with the following planned functions:

- Multiple-Port Register File (see Product Preview)
- Hard-Wired TTL-Type MSI
- Timer Modules
- Universal Asynchronous Receiver/Transmitter (UART)
- Small Computer Systems Interface (SCSI)
- Serial Peripheral Interface (SPI)
- Interrupt Controller
- Direct Memory Access (DMA) Controller.
- PC/PC-AT Expansion Bus Interface
- Multiplier
- First-In/First Out (FIFO) Memories
- MegaModules™:
  'ASC888 8-Bit Slice
  'ASC890 Microsequencer
  'ASC2901 4-Bit Slice
  'ASC2902 ALU Look Ahead
  'ASC2904 Shift Controller
  'ASC2910 Micro Controller.

STANDARD-CELL NAMING CONVENTIONS

Each standard cell has two designations. The first is similar to the 54/74 series of numbers and is designated the function number. The second describes the implementation(s) of the cell and is therefore referred to as the cell name. This dual numbering/naming convention simplifies cross-reference to other digital logic families and aids in differentiating cells providing multiple drive levels.

Function Numbers

Generic functions (i.e., 2-input positive AND gates) are designated with either an SN54ASCXXX or an SN74ASCXXX prefix corresponding to the operating temperature range designations used for the TTL families. SN54ASCXXX standard cells are rated for operation over the full military temperature range of −55°C to 125°C, and SN74ASCXXX standard cells are rated for operation from −40°C to 85°C. Function numbers are assigned as defined in Table 5.

Table 5. Sequence for Generic Function Assignment

FUNCTION NUMBERS 54/74ASCXXX	APPLICATION		FUNCTIONAL CATEGORY
	INTERNAL CELL	I/O CELL	
00- 999	X		SSI/MSI macro cells (Equivalent to 74LS, 74HC, or 74F)
2000-2499	X		SSI/MSI macro cells
2500-2599	X		Analog cells
3000-3099	X		Memory and compiler cells
4000-4999	X		SSI macro cells (Equivalent to 74HC)
5000-5025		X	Input buffers
5100-5125		X	Output buffers
5200-5250		X	Bidirectional I/O buffers
6002-6199	X		SSI/MSI macro cells

Cell Names

Most SSI gates and flip-flop functions are offered with multiple cell implementations to satisfy various performance levels. Each cell is named in accordance with the specification shown in Figure 5. An index to the logic function prefixes follows Figure 5.

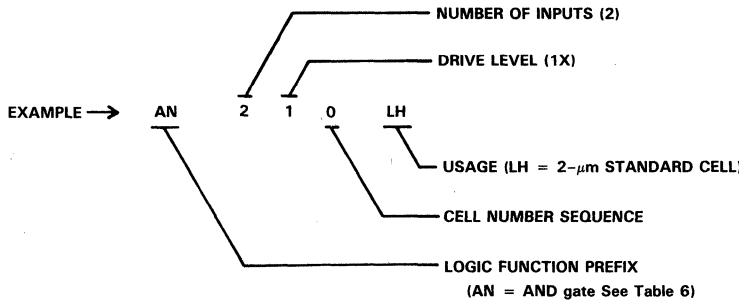

Figure 5. Cell Name Example

Table 6. Index to Cell and Macro Prefixes

AN	AND Gates
AO	AND-OR Gates
BF	Boolean Functions
BU	Buffers
CO	Comparators
D	Flip-Flops, D-Type
DE	Decoders
DL	Delay Elements
EN	EXCLUSIVE-NOR Gates
EX	EXCLUSIVE-OR Gates
GM	Latches, Gated S-R
GS	Latches, Gated-NOR S-R
IO	Bidirectional I/O Cells
IP	Input Cells
IV	Inverters
JK	Flip-Flops, J-K Type
LA	Latches, D-Type and S-R
MU	Multiplexers
MV	Multivibrator (One-Shot)
NA	NAND Gates
NO	NOR Gates
OP	Output Cells
OR	OR Gates
OS	Oscillators
PD	Pull-Down, Active
PR	Pull-Up, Active
PUC	Power-Up Clear (One-Shot)
R	Registers
RA	Hard-Wired RAM Macro Cells
RF	Register Files
S	Software Macros
T	Flip-Flop, Toggle Type
TO	Tie-Off

STANDARD-CELL DESIGN OVERVIEW

A standard-cell IC design execution can be broadly grouped into four basic phases:

- Phase 0 — Specifying the design
- Phase 1 — Creating the design database(s)
- Phase 2 — Generating the chip layout(s)
- Phase 3 — Fabricating and testing the device(s).

An overview of the four phases follows and is accompanied by a design flowchart, Figure 6. The flowchart specifies the milestones required to complete a design. The design flow has been developed in conjunction with

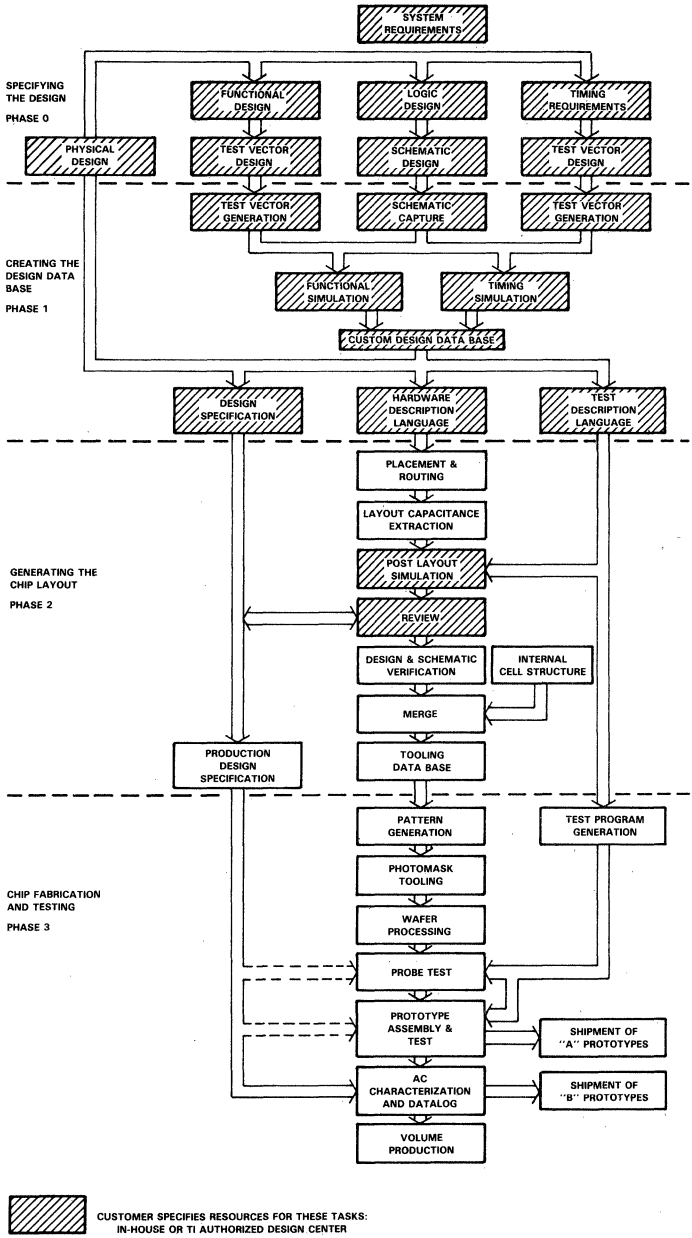

Figure 6. Standard-Cell Design Execution

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successful completion of many standard, semicustom, and custom ICs at TI. Strict adherence to the milestone verifications, simulations, reviews, and tests has yielded the most cost-effective success rate for IC design.

When adapted to standard-cell IC design, the milestones are structured specifically to maximize design resource utilization. In order to accommodate the user's own design resources, the milestones comprise varying levels of user involvement in the design phases, from simply supplying a logic diagram to a TI design center, to turning over a post-layout simulated data base for TI verification and production. In either case, the design flow is maintained to be equivalent. Key features of the design flow are:

- Applies design resources cost-effectively
- Structures development and verification of a design data base
- Updates design specifications routinely
- Utilizes a proven automated design system and production process.

Specifying the Design (Phase 0)

System requirements determine IC designs that satisfy the environmental, functional, logic, and performance requirements. Systems requiring more than a single IC will need to be partitioned. In all cases, complexity and use conditions will drive a hardware definition. Whether you intend to design the devices or ask TI to design them, they must be completely described. The following items should be specified before starting your standard-cell IC design.

Physical Design

End applications anticipated for the system design will determine physical properties utilized to manufacture the system. Likewise, the environment created within the system for the accommodation of custom semiconductor ICs will dictate the IC physical requirements.

Logic Design

A logic diagram is needed to define the boundary of the ICs, whether adapting an existing logic system or designing a new one.

Schematic Design

The schematic design reduces functions to their lowest functional-level components. An understanding of the standard-cell family and cell performance specifications will be beneficial to the designer. Reduction beyond cells, macros, and software macros is not needed if the IC design goals are achieved. Detailed guidelines and cell selection procedures are provided in TI design manuals issued for use with engineering workstations. Also, suggestions for evaluating, modifying, and using software macros are provided on the individual data sheets and in design guidelines provided in Section 7 of this data book. The resulting schematic diagram becomes the detailed reference document for cell conversion and schematic capture.

Interface (Input/Output) Buffers

The I/O buffers specify the inputs and outputs required to interface the custom IC into the system design.

Timing Test Vectors

These vectors specify the timing relationships needed between input pins and from inputs to outputs.

Functional Test Vectors

Functional test vectors specify the functional performance needed from the IC and include waveform diagrams and/or test patterns. Cost effectiveness is a direct function of testability. In some cases, I/O pins and additional logic are easily justified to achieve adequate test capability.

TI invites your request for new cells that are not available in the TI library. Software macros to satisfy most design requirements, if not currently in TI's library, can be generated on your workstation.

A blank, generic design specification, which can be used as a working document, is available from TI to guide you through the initial design steps.

Completion of Phase 0 will yield:

A schematic which includes the IC interfaces
Test vectors for both functional and delay time parameters
Packaging requirements for the IC.

Creating the Design Database (Phase I)

Phase 1 utilizes a workstation to capture the schematic diagram as a basis for simulating both functional behavior and timing relationships of the defined function. Phase 1 is accomplished as described in the following paragraphs.

Schematic Capture

Schematic capture consists of cell conversion and logic capture.

Cell Conversion

Each element of the given circuit is replaced with a standard-cell equivalent. This involves selecting the cells and macros that satisfy both functional and timing requirements, including dc sink/source current requirements of the I/O cells. Software macros can increase the efficiency of cell conversion, and simple modifications can make them custom for your current design. This is usually done on a workstation in conjunction with logic capture.

Logic Capture

This is the process of representing logic on the workstation by calling and naming each cell and macro to be used and by naming all input and output interconnections. A hierarchical design process permits the development of higher-level macros composed of cells and lower-order macros. These 'super' macros and their interconnections are also named. Within the limits of the particular workstation, this hierarchical design process is continued until the standard-cell IC is implemented. When completed, the workstation captures the defined logic in a hierarchical netlist database. This database is utilized by the **SystemCell**™ library Hardware Description Language (HDL) translator to convert the code into a TI design automation system code, called HDL. At this time, the workstation can provide a hard-copy logic diagram of the standard cell IC.

AC and DC Test Vector Generation

Utilizing the test vectors developed in Phase 0, files are input to the design workstation, which will overlay both functional and delay time attribute specifications on the schematic.

Functional and Timing Simulations

The workstation utilizes the ac and dc test vector files to verify pre-layout functionality and timing performance. This simulation uses the standard cell's intrinsic characteristics.

Test Description Language (TDL)

The workstation test vectors used in the pre-layout simulation are translated into TDL automatically by the **SystemCell**™ library TDL translator software. The extracted TDL patterns can be evaluated by programs that simulate faults at every node to see how effectively the test patterns are detecting faults. Test pattern grading is an optional procedure.

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Design Specification

The blank, generic, standard-cell IC design specification forms, available from TI, can be used as a working guideline to achieve successful pre-layout simulations. If so, most of the design specification data are captured during Phase 0 and 1. A formalized version can then be completed for joint approval by you and TI. Upon approval, both the design specification and data files are given to TI for Phase 2.

Successful completion of Phase 0 and Phase 1 yields the following results:

A database for the circuit description in HDL
A database for a set of test patterns expressed in TDL
A design specification.

Generating the Chip Layout (Phase 2)

During this phase of your standard-cell IC design, the HDL/TDL database, developed in Phase 1, is converted into an actual device layout.

Placement and Routing

Cells and interconnections are arranged according to your I/O design requirements. Using your HDL, a computer-automated layout is completed. Cells are first placed by the layout software, and then cell interconnections are made using the hierarchical netlist data base.

Layout Capacitance Extraction

Values of the interconnect capacitance for each network are extracted and added to cell capacitance to derive the total capacitive loading on each circuit node.

Post-Layout Simulation

Similar to the pre-layout functional and timing simulation, post-layout simulation combines the effects of intrinsic and interconnect capacitance and resistance values to simulate the performance based on the cell placement and chip layout.

Review

Results of the post-layout simulation are evaluated for conformance to design specification. Beyond conformance, the database results are evaluated for compliance with predictable norms defined for the design-automation-system process.

Design Specification

Based on results of the post-layout review, the design specification is confirmed and updated. Confirmation consists of a mutual agreement to proceed to Phase 3. An update is interactive and requires approval by both purchaser and TI. If necessary, options for the update are reviewed with the customer and specification changes, or database changes, that will meet the design requirements are proposed.

Design Verification

The layout database is checked by the design automation system to ensure that geometric design rules are met.

Schematic Verification

The schematic verification program uses the layout database and works backward to generate a new HDL, which is then compared to the pre-layout HDL description.

Merge Internal Cell Structure

The post-layout verified database is merged with a tooling-structure database, resident in the design automation system. This merge completes the tooling database.

Tooling Database

The tooling database is used to extract the test programs and pattern generator (PG) files. The files are needed to support wafer fabrication and chip testing.

Successful completion of Phase 3 yields the following results:

A test-program generation (TDL) database
A wafer-fabrication tooling database.

Chip Fabrication and Testing (Phase 3)

Prototypes of your standard-cell IC are fabricated and tested as described in the following paragraphs.

Photomask Tooling

The PG files are used to execute the photomask designs needed to produce the wafers containing the custom ICs.

Wafer Processing

CMOS standard-cell wafers are fabricated using a twin-well polysilicon self-aligned process (see Figure 1). Utilization of the 2-μm process, defined to remain a mainstream technology at TI, is based on long-term product plan commitments for both custom and standard IC products.

Probe Test

Standard wafer-probe techniques are applied to implement cost-effective utilization of fabrication materials and resources. A probe test ensures the assembled ICs are most likely to yield parametrically good devices.

Prototype Assembly and Test

Chips passing the probe test are used in the prototype fabrication. Prototypes are packaged in ceramic packs or carriers as an expedient method for completing design evaluations. Class "A" prototypes are typically tested at room temperature for functionality while being exercised at 1 MHz. Electrical characteristics of the input cells, output cells, and static supply current are "go-no-go" tested to the design specification. These class "A" prototypes are expedited to you for use in performing system functional testing.

AC Characterization and Data Log

The remaining prototypes (class "B") are tested/data logged by TI in accordance with the design specification. Typically, class "B" is tested for functionality at the rated performance range(s) over operating ranges of supply voltage and temperature. Standard data logging is limited to "go-no-go" conformance to the design specification. These prototypes permit the customer to perform system characterization and system prototype delivery prior to production start-up.

Volume Production

Acceptance of the characterized "B" prototypes as conforming to the design specification is required prior to the execution of production orders. Production quantities are packaged in accordance with the design specification.

SUMMARY

The TI **SystemCell**™ family provides simple electronic solutions for making your products uniquely innovative. The **SystemCell**™ family data sheets (see Section 3) and IC design considerations (see Section 7) provide additional information. For assistance beyond the scope of this data book, call the following sources:

ASIC product specialist(s) at TI field sales office(s)
Design engineer(s) at the TI Regional Technology Center(s)
The TI ASIC center in Dallas.

Definitions, Ratings, and Glossary

The following symbols are now being used in function tables on TI data sheets:

H	=	high level (steady state)
L	=	low level (steady state)
↑	=	transition from low to high level
↓	=	transition from high to low level
X	=	irrelevant (any input, including transitions)
Z	=	off (high-impedance) state of a 3-state output
a . . h	=	the level of steady-state inputs at inputs A through H, respectively
Q_0	=	level of Q before the indicated steady-state input conditions were established
$\bar{Q}_0$	=	complement of Q_0 or level of $\bar{Q}$ before the indicated steady-state input conditions were established
Q_n	=	level of Q before the most recent active transition indicated by ↑ or ↓
⎍	=	one high-level pulse
⎏	=	one low-level pulse
TOGGLE	=	each output changes to the complement of its previous level on each active transition indicated by ↑ or ↓.

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains, H, L, and/or X together with ↑ and/or ↓, this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, Q_0, or $\bar{Q}_0$), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output. (If the output is shown as a pulse, ⎍ or ⎏, the pulse follows the indicated input transition and persists for an interval dependent on the circuit.)

Among the most complex function tables in this book are those of the shift registers. These embody most of the symbols used in any of the function tables, plus more. Below is the function table of a 4-bit bidirectional universal shift register, e.g., SN74ASC194A.

FUNCTION TABLE

INPUTS										OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D
	S1	S0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{D0}

The first line of the table represents a synchronous clearing of the register and says that if clear is low, all four outputs will be reset low regardless of the other inputs. In the following lines, clear is inactive (high) and so has no effect.

The second line shows that so long as the clock input remains low (while clear is high), no other input has any effect and the outputs maintain the levels they assumed before the steady-state combination of clear high and clock low was established. Since on other lines of the table only the rising transition of the clock is shown to be active, the second line implicitly shows that no further change in the outputs will occur while the clock remains high or on the high-to-low transition of the clock.

The third line of the table represents synchronous parallel loading of the register and says that if S1 and S0 are both high then, without regard to the serial input, the data entered at A will be at output Q_A, data entered at B will be at Q_B, and so forth, following a low-to-high clock transition.

The fourth and fifth lines represent the loading of high- and low-level data, respectively, from the shift-right serial input and the shifting of previously entered data one bit; data previously at Q_A is now at Q_B, the previous levels of Q_B and Q_C are now at Q_C and Q_D respectively, and the data previously at Q_D is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is low and S0 is high and the levels at inputs A through D have no effect.

The sixth and seventh lines represent the loading of high- and low-level data, respectively, from the shift-left serial input and the shifting of previously entered data one bit; data previously at Q_B is now at Q_A, the previous levels of Q_C and Q_D are now at Q_B and Q_C, respectively, and the data previously at Q_A is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is high and S0 is low and the levels at inputs A through D have no effect.

The last line shows that as long as both mode inputs are low, no other input has any effect and, as in the second line, the outputs maintain the levels they assumed before the steady-state combination of clear high and both mode inputs low was established.

Table 1. Specifications for Internal Boolean and Macro Cells

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
Input voltage range . . . . . −0.5 V to 7 V
Operating free-air temperature range: SN54ASC' . . . . . −55°C to 125°C
SN74ASC' . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ASC'			SN74ASC'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
T_A	Operating temperature range	−55		125	−40		85	°C

Table 2. Specifications for Input Standard Cells

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Input voltage range . . . . . −0.5 V to 7 V
Operating free-air temperature range: SN54ASC' . . . . . −55°C to 125°C
SN74ASC' . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions for TTL-compatible inputs

		SN54ASC'			SN74ASC'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	0		200	0		200	ns
T_A	Operating temperature range	−55		125	−40		85	°C

recommended operating conditions for CMOS-compatible inputs

		SN54ASC'			SN74ASC'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	3.15			3.15			V
V_{IL}	Low-level input voltage			0.9			0.9	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	0		300	0		300	ns
T_A	Operating temperature range	−55		125	−40		85	°C

Table 3. Specifications for Output Standard Cells

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
Output clamp current, I_{OK} ($V_O<0$ or $V_O>V_{CC}$) . . . . . ±−20 mA
Continuous output current ($V_O=0$ to V_{CC}) . . . . . ±25 mA
Operating free-air temperature range: SN54ASC' . . . . . −55°C to 125°C
SN74ASC' . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ASC'			SN74ASC'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current†	As specified on individual data sheets						mA
I_{OL}	Low-level output current							mA
T_A	Operating temperature range	−55		125	−40		85	°C

†Applies for all except open-drain output cells.

Table 4. Specifications for Input/Output (I/O) Standard Cells

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
I/O clamp current, ($V_I<0$ or $V_I>V_{CC}$) . . . . . ±20 mA
Continuous output current ($V_O=0$ to V_{CC}) . . . . . ±25 mA
Operating free-air temperature range: SN54ASC' . . . . . −55°C to 125°C
SN74ASC' . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions for TTL-compatible I/Os

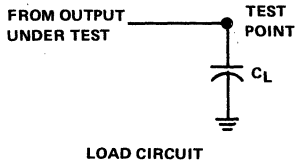
		SN54ASC'			SN74ASC'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current†	As specified on individual data sheets						mA
I_{OL}	Low-level output current							mA
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and and fall) times	0		200	0		200	ns
T_A	Operating temperature range	−55		125	−40		85	°C

†Applies for all except open-drain output cells.

recommended operating conditions for CMOS-compatible I/Os

		SN54ASC′			SN74ASC′			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current†	As specified on individual data sheets						mA
I_{OL}	Low-level output current							mA
V_{IH}	High-level input voltage	3.15			3.15			V
V_{IL}	Low-level input voltage			0.9			0.9	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and and fall) times	0		300	0		300	ns
T_A	Operating temperature range	−55		125	−40		85	°C

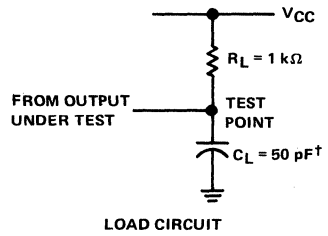
†Applies for all except open-drain output cells.



PARAMETER	CELLS	C_L†
t_{pd}	INTERNAL and INPUT	0 pF and 1 pF
t_{pd}	OUTPUTS	15 pF and 50 pF

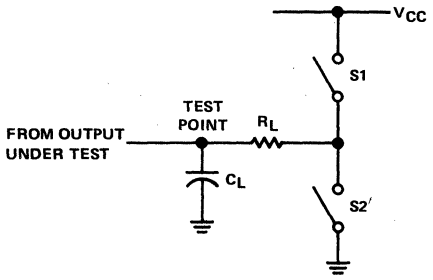
†C_L includes probe and test fixture capacitance.

FIGURE 1. TOTEM-POLE OUTPUTS



†C_L includes probe and test fixture capacitance.

FIGURE 2. OPEN-DRAIN OUTPUTS



PARAMETER		INTERNAL BUFFER		OUTPUT OR I/O		S1	S2
		R_L	C_L†	R_L	C_L†		
t_{en}	t_{PZH}	40 kΩ	1 pF	1 kΩ	15 pF and 50 pF	OPEN	CLOSED
	t_{PZL}	20 kΩ				CLOSED	OPEN
t_{dis}	t_{PHZ}	40 kΩ	1 pF	1 kΩ	50 pF	OPEN	CLOSED
	t_{PLZ}	20 kΩ				CLOSED	OPEN
t_{pd}	t_{PLH}	—	0 pF and 1 pF	—	15 pF and 50 pF	OPEN	OPEN
	t_{PHL}						

†C_L includes probe and test fixture capacitance.

FIGURE 3. 3-STATE OUTPUTS

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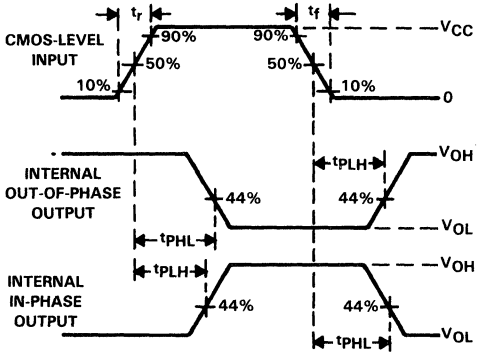


FIGURE 4. CMOS INPUT CELL AND CMOS 3-STATE BIDIRECTIONAL INPUT PROPAGATION DELAY TIME VOLTAGE WAVEFORMS

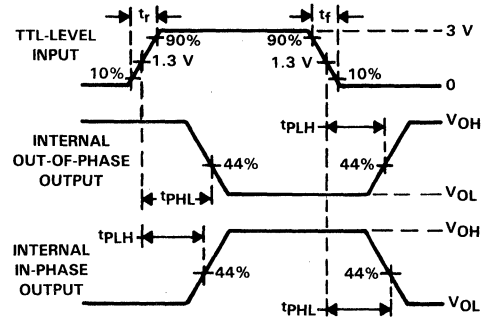


FIGURE 5. TTL INPUT CELL AND TTL 3-STATE BIDIRECTIONAL INPUT PROPAGATION DELAY TIME VOLTAGE WAVEFORMS

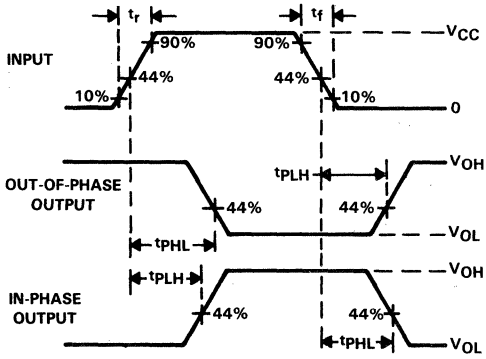


FIGURE 6. INTERNAL TOTEM-POLE OUTPUT PROPAGATION DELAY TIME VOLTAGE WAVEFORMS

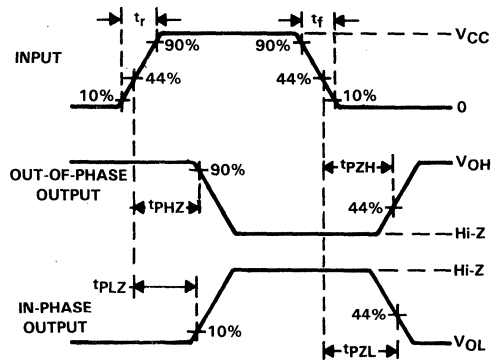


FIGURE 7. INTERNAL 3-STATE-OUTPUT BUFFER DISABLE AND ENABLE VOLTAGE WAVEFORMS

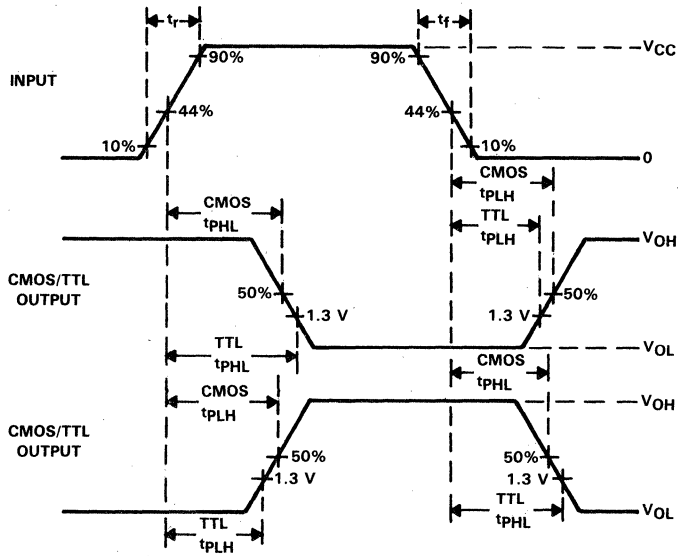


FIGURE 8. CMOS/TTL OUTPUT AND 3-STATE BIDIRECTIONAL INPUT/OUTPUT PROPAGATION DELAY TIME VOLTAGE WAVEFORMS

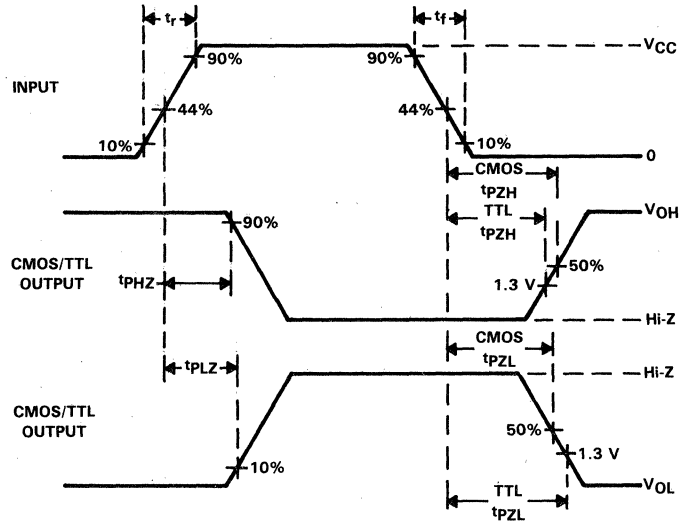


FIGURE 9. CMOS/TTL 3-STATE BIDIRECTIONAL INPUT/OUTPUT DISABLE AND ENABLE VOLTAGE WAVEFORMS

INTRODUCTION

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

OPERATING CONDITIONS AND CHARACTERISTICS (IN SEQUENCE BY LETTER SYMBOLS)

C_{pd} Power dissipation capacitance
Used to determine the no-load dynamic power dissipation per logic function (see individual circuit pages): $P_D = C_{pd} V_{CC}^2 f + I_{CC} V_{CC}$.

f_{max} Maximum clock frequency
The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.

I_{CC} Supply current
The current into* the V_{CC} supply terminal of an integrated circuit.

I_{IH} High-level input current
The current into* an input when a high-level voltage is applied to that input.

I_{IL} Low-level input current
The current into* an input when a low-level voltage is applied to that input.

I_{OH} High-level output current
The current into* an output with input conditions applied that, according to the product specification, will establish a high level at the output.

I_{OL} Low-level output current
The current into* an output with input conditions applied that, according to the product specification, will establish a low level at the output.

I_{OZ} Off-state (high-impedance-state) output current (of a three-state output)
The current flowing into* an output having three-state capability with input conditions established that, according to the production specification, will establish the high-impedance state at the output.

V_{IH} High-level input voltage
An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.
NOTE: A minimum is specified that is the least-positive value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{IL} Low-level input voltage
An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables.
NOTE: A minimum is specified that is the most-positive value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

*Current out of a terminal is given as a negative value.

V_{OH} **High-level output voltage**
The voltage at an output terminal with input conditions applied that, according to product specification, will establish a high level at the output.

V_{OL} **Low-level output voltage**
The voltage at an output terminal with input conditions applied that, according to product specification, will establish a low level at the output.

V_{T+} **Positive-going threshold level**
The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, V_{T-}.

V_{T-} **Negative-going threshold level**
The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, V_{T+}.

t_a **Access time**
The time interval between the application of a specified input pulse and the availability of valid signals at an output.

t_{dis} **Disable time (of a three-state output)**
The time interval between the specified reference points on the input and output voltage waveforms, with the three-state output changing from either of the defined active levels (high or low) to a high-impedance (off) state. (t_{dis} = t_{PHZ} or t_{PLZ}).

t_{en} **Enable time (of a three-state output)**
The time interval between the specified reference points on the input and output voltage waveforms, with the three-state output changing from a high-impedance (off) state to either of the defined active levels (high or low). (t_{en} = t_{PZH} or t_{PZL}).

t_f **Fall time**
The time interval between two reference points (90% and 10% unless otherwise specified) on a waveform that is changing from the defined high level to the defined low level.

t_h **Hold time**
The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.

NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is guaranteed.

t_{pd} **Propagation delay time**
The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level. (t_{pd} = t_{PHL} or t_{PLH}).

t_{PHL} **Propagation delay time, high-to-low level output**
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

t_{PHZ} **Disable time (of a three-state output) from high level**
The time interval between the specified reference points on the input and the output voltage waveforms with the three-state output changing from the defined high level to a high-impedance (off) state.

t_{PLH} **Propagation delay time, low-to-high-level output**
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.

t_{PLZ} **Disable time (of a three-state output) from low level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined low level to a high-impedance (off) state.

t_{PZH} **Enable time (of a three-state output) to high level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined high level.

t_{PZL} **Enable time (of a three-state output) to low level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined low level.

t_r **Rise time**
The time interval between two reference points (10% and 90% unless otherwise specified) on a waveform that is changing from the defined low level to the defined high level.

t_{sr} **Sense recovery time**
The time interval needed to switch a memory from a write mode to a read mode and to obtain valid data signals at the output.

t_{su} **Setup time**
The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal.

NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

2. The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is guaranteed.

t_t **Transition time (general)**
The time interval between two reference points (10% and 90% unless otherwise specified) on a waveform that is changing from the defined low level to the defined high level (rise time) or from the defined high level to the defined low level (fall time).

t_w **Pulse duration (width)**
The time interval between specified reference points on the leading and trailing edges of the pulse waveform.

00

2-INPUT POSITIVE-NAND GATES

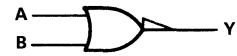
logic symbol

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
NA210LH	0.9	2.0	0.51
NA220LH	0.8	1.3	1.00
NA230LH	0.7	1.1	1.51
NA240LH	0.6	1.0	2.06
NA260LH	0.6	0.8	2.98
Label: NA2n0LH A,B,Y			

02

2-INPUT POSITIVE-NOR GATES

logic symbol



CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
NO210LH	0.9	2.4	0.33
NO220LH	0.8	1.5	0.52
NO230LH	0.8	1.3	0.80
NO240LH	0.7	1.1	0.98
Label: NO2n0LH A,B,Y;			

04

INVERTERS

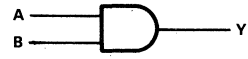
logic symbol

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
IV101LH	2.2	2.3	7.22
IV110LH	0.9	1.7	0.44
IV120LH	0.6	1.1	0.80
IV130LH	0.5	0.9	1.29
IV140LH	0.5	0.8	1.61
IV160LH	0.4	0.7	2.39
IV180LH	0.4	0.6	3.16
Label: IV1n0LH A,Y;			

08

2-INPUT POSITIVE-AND GATES

logic symbol



CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
AN210LH	1.3	2.1	0.90
AN220LH	1.5	1.9	1.20
AN240LH	1.9	2.1	2.32
AN260LH	1.5	1.7	3.08
Label: AN2n0LH A,B,Y;			

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3-INPUT POSITIVE-NAND GATES

logic symbol

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
NA310LH	0.8	2.2	0.50
NA320LH	0.9	1.5	0.94
NA330LH	0.8	1.3	1.41
NA340LH	0.8	1.1	1.86
Label: NA3n0LH A,B,C,Y;			

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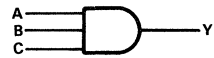
3-INPUT POSITIVE-AND GATES

logic symbol



CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
AN310LH	1.6	2.4	1.06
AN320LH	1.7	2.2	1.56
AN340LH	2.2	2.5	2.59
AN360LH	1.7	1.9	4.08
Label: AN3n0LH A,B,C,Y;			

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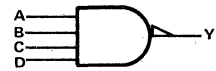
4-INPUT POSITIVE-NAND GATES

logic symbol



CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
NA410LH	0.8	2.6	0.50
NA420LH	1.0	1.8	0.96
NA430LH	1.0	1.5	1.46
Label: NA4n0LH A,B,C,D,Y;			

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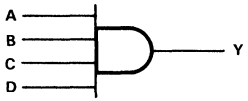
4-INPUT POSITIVE-AND GATES

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
AN410LH	1.8	2.6	1.18
AN420LH	2.0	2.5	1.72
AN440LH	2.4	2.7	2.77
AN460LH	2.1	2.3	4.58
Label: AN4n0LH A,B,C,D,Y;			

logic symbol



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3-INPUT POSITIVE-NOR GATES

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
NO310LH	1.1	3.2	0.32
NO320LH	1.1	2.1	0.56
NO330LH	1.0	1.8	0.85
Label: NO3n0LH A,B,C,Y;			

logic symbol

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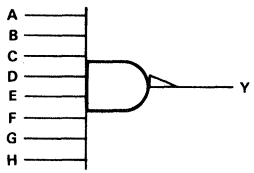
8-INPUT POSITIVE-NAND GATES

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
NA810LH	1.9	4.5	0.61
NA820LH	1.9	3.3	1.13
Label: NA8n0LH A,B,C,D,E,F,G,H,Y;			

logic symbol



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2-INPUT POSITIVE-OR GATES

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
OR210LH	1.5	2.3	0.86
OR220LH	1.7	2.1	1.62
OR240LH	1.6	1.8	3.09
OR260LH	1.5	1.7	4.70
Label: OR2n0LH A,B,Y;			

logic symbol

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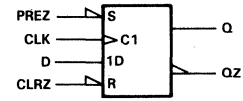
D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS

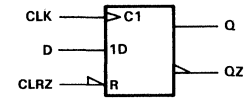
CELL NAME	fmax (MHz)	C_{pd} (pF)
DFB20LH	46.3	3.76
DTB10LH	55.8	2.12
Label: D__Bn0LH CLRZ,PREZ,D,CLK,Q,QZ;		
DFC20LH	52.1	3.39
DTC10LH	52.1	2.10
Label: D__Cn0LH CLRZ,D,CLK,Q,QZ;		
DFN20LH	64.2	2.71
DTN10LH	55.8	2.21
Label: D__Nn0LH D,CLK,Q,QZ;		
DFP20LH	55.8	3.49
DTP10LH	55.8	2.50
Label: D__Pn0LH PREZ,D,CLK,Q,QZ;		
DFY20LH	69.2	4.63
Label: DFY20LH PREZ,CLK,Q,QZ;		
DFZ20LH	59.2	4.94
Label: DFZ20LH CLRZ,PREZ,CLK,Q,QZ;		

logic symbol

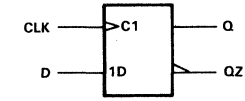
DFB20LH, DTB10LH



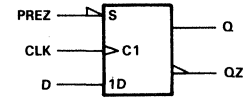
DFC20LH, DTC10LH



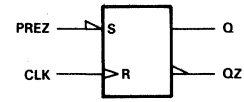
DFN20LH, DTN10LH



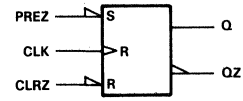
DFP20LH, DTP10LH



DFY20LH



DFZ20LH



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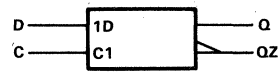
D-TYPE LATCHES WITH ACTIVE-HIGH ENABLE

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
LAH10LH	1.6	2.4	2.00
LAH20LH	1.6	2.0	2.81
Label: LAHn0LH D,C,Q,QZ;			

logic symbol



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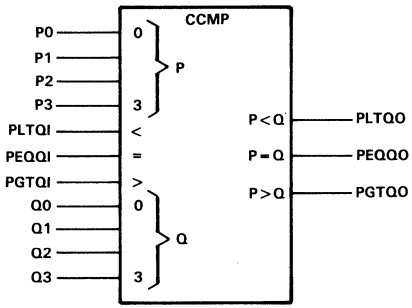
4-BIT MAGNITUDE COMPARATORS

CELL NAME	t_{pd} (ns)		C_{pd}† (pF)
	C_L = 0 pF	C_L = 1 pF	
S85LH	12.0	12.5	13.6
Label: S85LH P3,P2,P1,P0,Q3,Q2,Q1,Q0,PGTQ1,PLTQ1, PEQQ1,PGTQ0,PLTQ0,PEQQ0;			

logic symbol



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2-INPUT EXCLUSIVE-OR GATES

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
EX210LH	1.8	2.3	1.00
EX220LH	2.0	2.0	1.35
EX240LH	2.4	2.0	2.55
Label: EX2n0LH A,B,Y;			

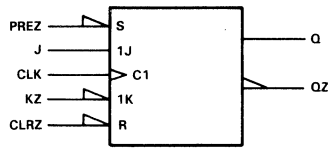
logic symbol

109

J-$\overline{K}$ POSITIVE-EDGE-TRIGGERED FLIP-FLOPS

CELL NAME	fmax (MHz)	C_{pd} (pF)
JKB20LH	44.2	4.81
Label: JKB20LH CLRZ,PREZ,J,KZ,CLK,Q,QZ;		

logic symbol



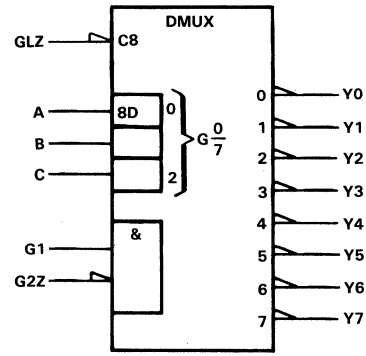
†The equivalent power dissipation capacitance does not include interconnect capacitance.

137

3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS WITH ADDRESS LATCHES

CELL NAME	t_{pd} (ns)		C_{pd}† (pF)
	C_L = 0 pF	C_L = 1 pF	
S137LH	12.0	12.7	17.59
Label: S137LH C,B,A,GLZ,G2Z,G1,Y0,Y1,Y2,Y3,Y4,Y5, Y6,Y7;			

logic symbol

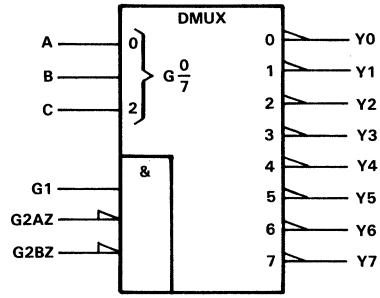


138

3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS

CELL NAME	t_{pd} (ns)		C_{pd}† (pF)
	C_L = 0 pF	C_L = 1 pF	
S138LH	7.0	7.7	13.77
Label: S138LH G1,G2AZ,G2BZ,A,B,C,Y0,Y1,Y2,Y3,Y4, Y5,Y6,Y7;			

logic symbol



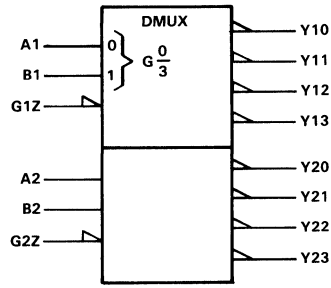
†The equivalent power dissipation capacitance does not include interconnect capacitance.

139

DUAL 2-LINE TO 4-LINE DECODERS/ DEMULTIPLEXERS

CELL NAME	t_{pd} (ns)		C_{pd}† (pF)
	C_L = 0 pF	C_L = 1 pF	
S139LH	4.0	4.6	12.64
Label: S139LH A1,B1,G1Z,A2,B2,G2Z,Y10,Y11,Y12, Y13,Y20,Y21,Y22,Y23;			

logic symbol

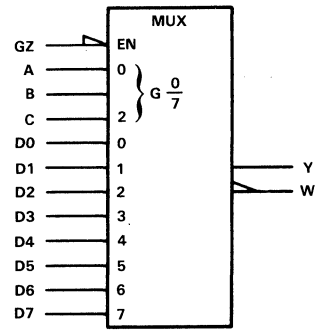


151

8-LINE TO 1-LINE MULTIPLEXERS

CELL NAME	t_{pd} (ns)		C_{pd}† (pF)
	C_L = 0 pF	C_L = 1 pF	
S151LH	8.0	10.6	10.09
Label: S151LH GZ,A,B,C,D0,D1,D2,D3,D4,D5,D6,D7, Y,W;			

logic symbol



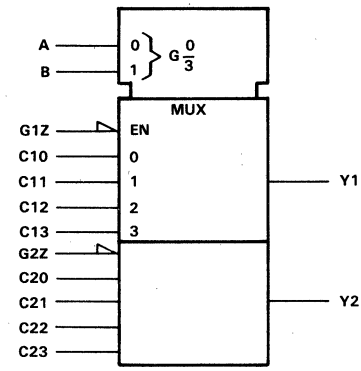
†The equivalent power dissipation capacitance does not include interconnect capacitance.

153

DUAL 4-LINE TO 1-LINE MULTIPLEXERS

CELL NAME	t_{pd} (ns)		C_{pd}† (pF)
	C_L = 0 pF	C_L = 1 pF	
S153LH	8.0	8.7	8.56
Label: S153LH G1Z,G2Z,A,B,C10,C11,C12,C13,C20, C21,C22,C23,Y1,Y2;			

logic symbol

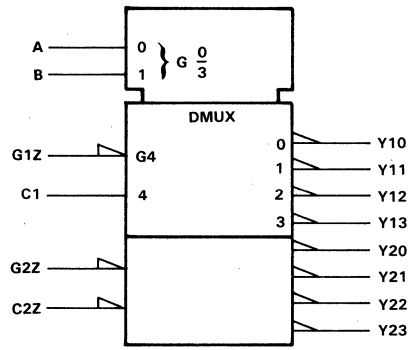


155

DUAL 2-LINE TO 4-LINE DECODERS/ DEMULTIPLEXERS WITH DATA AND ENABLE LINES

CELL NAME	t_{pd} (ns)		C_{pd}† (pF)
	C_L = 0 pF	C_L = 1 pF	
S155LH	5.0	5.6	12.20
Label: S155LH C1,G1Z,C2Z,G2Z,A,B,Y10,Y11,Y12,Y13, Y20,Y21,Y22,Y23;			

logic symbol



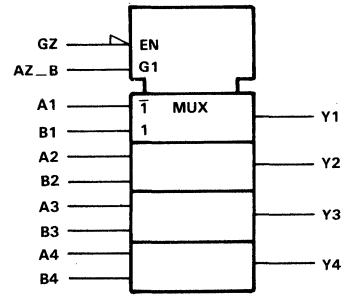
†The equivalent power dissipation capacitance does not include interconnect capacitance.

157

QUADRUPLE 2-LINE TO 1-LINE NONINVERTING MULTIPLEXERS

CELL NAME	t_{pd} (ns)		C_{pd}† (pF)
	C_L = 0 pF	C_L = 1 pF	
S157LH	6.0	7.1	9.40
Label: S157LH A1,A2,A3,A4,B1,B2,B3,B4,AZ_B,GZ, Y1,Y2,Y3,Y4;			

logic symbol

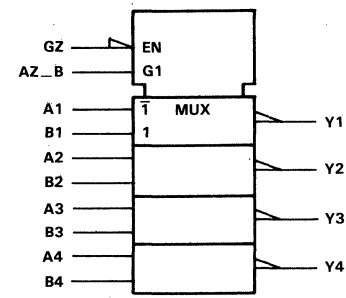


158

QUADRUPLE 2-LINE TO 1-LINE INVERTING MULTIPLEXERS

CELL NAME	t_{pd} (ns)		C_{pd}† (pF)
	C_L = 0 pF	C_L = 1 pF	
S158LH	6.2	6.6	12.16
Label: S158LH A1,A2,A3,A4,B1,B2,B3,B4,AZ_B,GZ, Y1,Y2,Y3,Y4;			

logic symbol



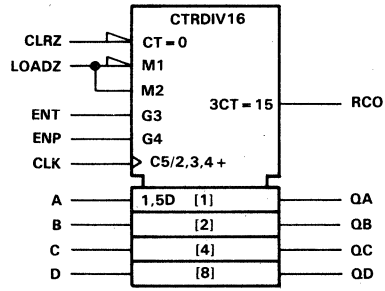
†The equivalent power dissipation capacitance does not include interconnect capacitance.

161A

SYNCHRONOUS 4-BIT BINARY COUNTERS WITH DIRECT CLEAR

CELL NAME	t_{pd} (ns)		C_{pd}† (pF)
	C_L = 0 pF	C_L = 1 pF	
S161ALH	12.0	13.0	31.54
Label: S161ALH D,C,B,A,CLK,CLRZ,ENP,ENT,LOADZ, QD,QC,QB,QA,RCO;			

logic symbol

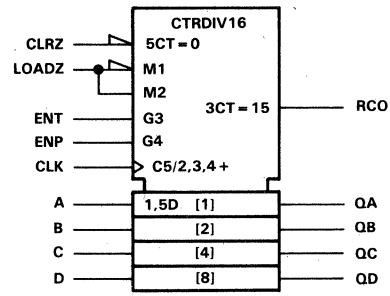


163A

SYNCHRONOUS 4-BIT BINARY COUNTERS

CELL NAME	t_{pd} (ns)		C_{pd}† (pF)
	C_L = 0 pF	C_L = 1 pF	
S163ALH	9.0	10.0	29.81
Label: S163ALH D,C,B,A,CLK,CLRZ,ENP,ENT,LOADZ, QD,QC,QB,QA,RCO;			

logic symbol

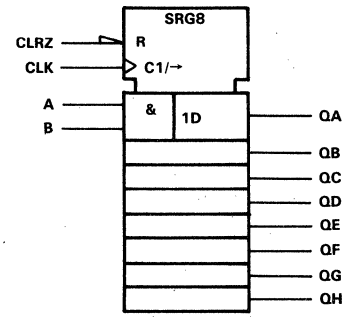


164

8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

CELL NAME	t_{pd} (ns)		C_{pd}† (pF)
	C_L = 0 pF	C_L = 1 pF	
S164LH	5.0	5.5	23.55
Label: S164LH A,B,CLK,CLRZ,QA,QB,QC,QD,QE,QF,QG, QH;			

logic symbol



†The equivalent power dissipation capacitance does not include interconnect capacitance.

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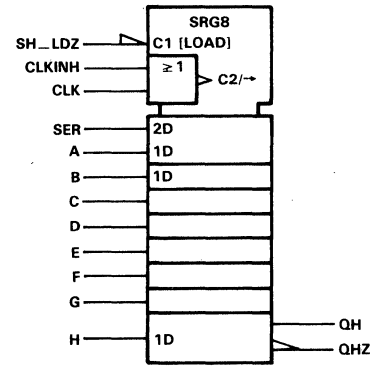
PARALLEL-LOAD 8-BIT SHIFT REGISTERS

CELL NAME	t_{pd} (ns)		C_{pd}† (pF)
	C_L = 0 pF	C_L = 1 pF	
S165LH	8.0	8.5	42.07
Label: S165LH A,B,C,D,E,F,G,H,CLK,CLKINH,SH_LDZ, SER,QH,QHZ;			

logic symbol

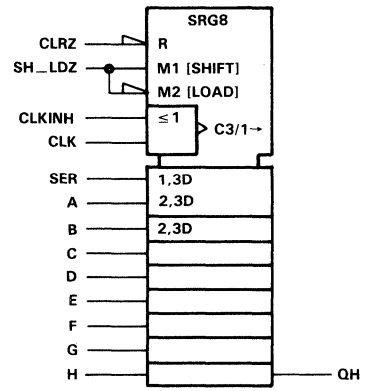


166

PARALLEL-LOAD 8-BIT SHIFT REGISTERS WITH DIRECT CLEAR

CELL NAME	t_{pd} (ns)		C_{pd}† (pF)
	C_L = 0 pF	C_L = 1 pF	
S166LH	7.5	8.4	33.15
Label: S166LH A,B,C,D,E,F,G,H,CLK,CLKINH,SER, SH_LDZ,CLRZ,QH;			

logic symbol



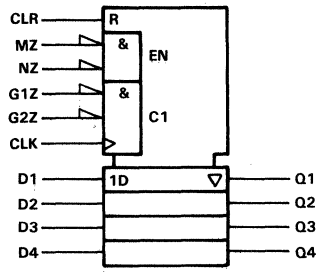
†The equivalent power dissipation capacitance does not include interconnect capacitance.

173

4-BIT D-TYPE REGISTERS WITH 3-STATE OUTPUTS

CELL NAME	t_{pd} (ns)		C_{pd}† (pF)
	C_L = 0 pF	C_L = 1 pF	
S173LH	7.1	8.0	24.00
Label: S173LH D1,D2,D3,D4,CLK,CLR,G1Z,G2Z,MZ,NZ, Q1,Q2,Q3,Q4;			

logic symbol

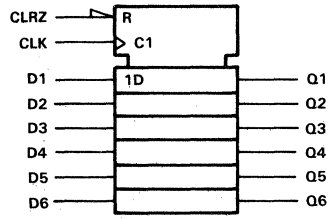


174

HEX D-TYPE FLIP-FLOPS

CELL NAME	t_{pd} (ns)		C_{pd}† (pF)
	C_L = 0 pF	C_L = 1 pF	
S174LH	8.0	8.5	24.44
Label: S174LH D1,D2,D3,D4,D5,D6,CLK,CLRZ,Q1,Q2, Q3,Q4,Q5,Q6;			

logic symbol

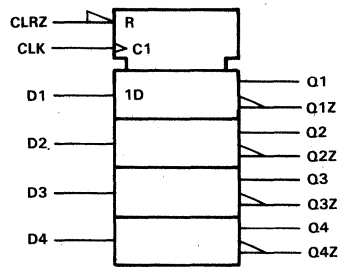


175

QUADRUPLE D-TYPE FLIP-FLOPS WITH COMPLEMENTARY OUTPUTS

CELL NAME	t_{pd} (ns)		C_{pd}† (pF)
	C_L = 0 pF	C_L = 1 pF	
S175LH	5.5	6.4	13.74
Label: S175LH D1,D2,D3,D4,CLK,CLRZ,Q1,Q1Z,Q2, Q2Z,Q3,Q3Z,Q4,Q4Z;			

logic symbol



†The equivalent power dissipation capacitance does not include interconnect capacitance.

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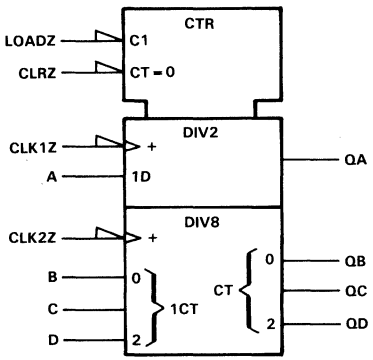
177

1-BIT AND 3-BIT BINARY RIPPLE COUNTERS

CELL NAME	t_{pd} (ns)		C_{pd}† (pF)
	C_L = 0 pF	C_L = 1 pF	
S177LH	22.0	22.5	23.56
Label: S177LH A,B,C,D,LOADZ,CLRZ,CLK1Z,CLK2Z,QA, QB,QC,QD;			

logic symbol

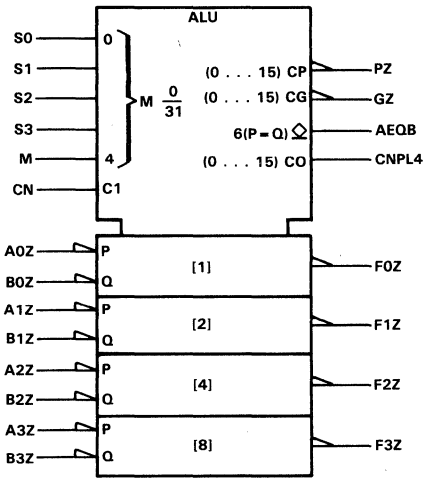


181

ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

CELL NAME	t_{pd} (ns)		C_{pd}† (pF)
	C_L = 0 pF	C_L = 1 pF	
S181LH	13.0	14.6	46.68
Label: S181LH A3Z,A2Z,A1Z,A0Z,B3Z,B2Z,B1Z,B0Z, CN,M,S3,S2,S1,S0,F3Z,F2Z,F1Z,F0Z,AEQB, GZ,PZ,CNPL4;			

logic symbol



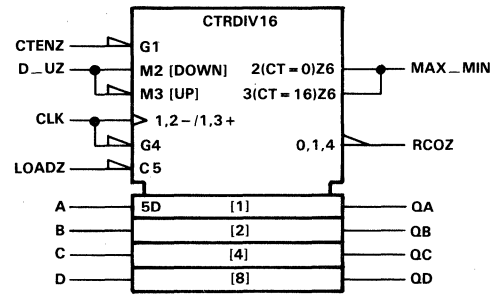
†The equivalent power dissipation capacitance does not include interconnect capacitance.

191

SYNCHRONOUS UP/DOWN BINARY COUNTERS WITH DOWN/UP MODE CONTROL

CELL NAME	t_{pd} (ns)		C_{pd}† (pF)
	C_L = 0 pF	C_L = 1 pF	
S191LH	11.5	12.6	37.26
Label: S191LH D,C,B,A,CLK,D__UZ,CTENZ,LOADZ,QD, QC,QB,QA,RCOZ,MAX__MIN;			

logic symbol

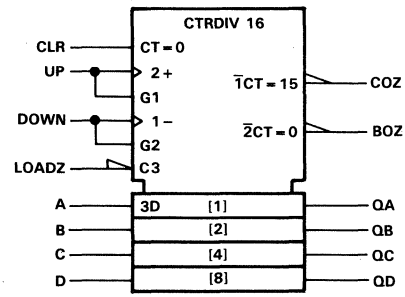


193

SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

CELL NAME	t_{pd} (ns)		C_{pd}† (pF)
	C_L = 0 pF	C_L = 1 pF	
S193LH	11.0	11.5	34.84
Label: S193LH A,B,C,D,UP,DOWN,LOADZ,CLR,BOZ,COZ, QA,QB,QC,QD;			

logic symbol



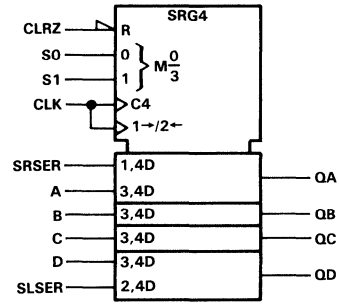
†The equivalent power dissipation capacitance does not include interconnect capacitance.

194A

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

CELL NAME	t_{pd} (ns)		C_{pd}† (pF)
	C_L = 0 pF	C_L = 1 pF	
S194ALH	5.0	5.9	25.45
Label: S194ALH A,B,C,D,SRSER,SLSER,CLK,CLRZ,S1,S0, QA,QB,QC,QD;			

logic symbol

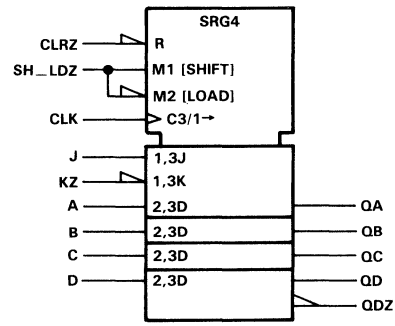


195A

4-BIT PARALLEL-ACCESS SHIFT REGISTERS

CELL NAME	t_{pd} (ns)		C_{pd}† (pF)
	C_L = 0 pF	C_L = 1 pF	
S195ALH	5.5	6.4	21.95
Label: S195ALH CLRZ,CLK,SH_LDZ,J,KZ,A,B,C,D,QA, QB,QC,QD,QDZ;			

logic symbol



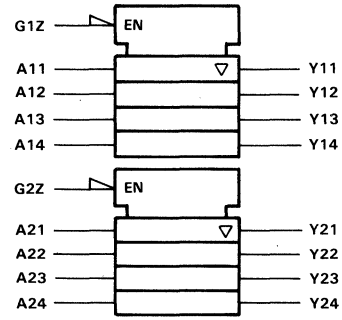
†The equivalent power dissipation capacitance does not include interconnect capacitance.

244

OCTAL INTERNAL 3-STATE BUS BUFFERS

CELL NAME	t_{pd} (ns)		C_{pd}† (pF)
	C_L = 0 pF	C_L = 1 pF	
S244LH	2.6	4.3	8.82
Label: S244LH A11,A12,A13,A14,G1Z,A21,A22,A23, A24,G2Z,Y11,Y12,Y13,Y14,Y21,Y22,Y23,Y24;			

logic symbol

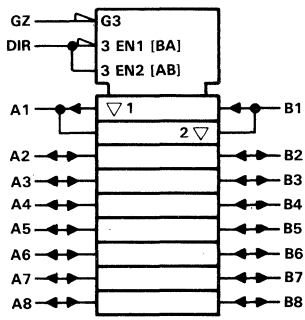


245

OCTAL INTERNAL 3-STATE BUS TRANSCEIVERS

CELL NAME	t_{pd} (ns)		C_{pd}† (pF)
	C_L = 0 pF	C_L = 1 pF	
S245LH	5.0	6.7	22.96
Label: S245LH A1,A2,A3,A4,A5,A6,A7,A8,B1,B2,B3, B4,B5,B6,B7,B8,GZ,DIR;			

logic symbol

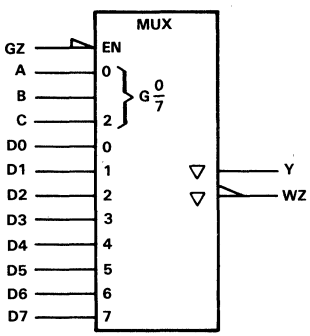


251

8-LINE TO 1-LINE MULTIPLEXERS WITH 3-STATE OUTPUTS

CELL NAME	t_{pd} (ns)		C_{pd}† (pF)
	C_L = 0 pF	C_L = 1 pF	
S251LH	9.7	11.4	12.85
Label: S251LH GZ,A,B,C,D0,D1,D2,D3,D4,D5,D6,D7, Y,WZ;			

logic symbol



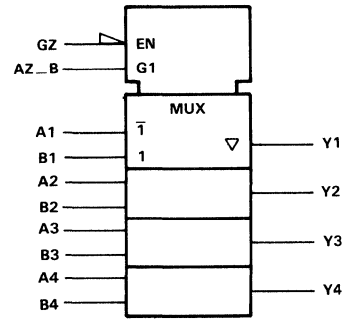
†The equivalent power dissipation capacitance does not include interconnect capacitance.

257A

QUADRUPLE 2-LINE TO 1-LINE MULTIPLEXERS WITH 3-STATE OUTPUTS

CELL NAME	t_{pd} (ns)		C_{pd}† (pF)
	C_L = 0 pF	C_L = 1 pF	
S257ALH	5.0	6.7	10.8
Label: S257ALH A1,A2,A3,A4,B1,B2,B3,B4,GZ,AZ__B, Y1,Y2,Y3,Y4;			

logic symbol

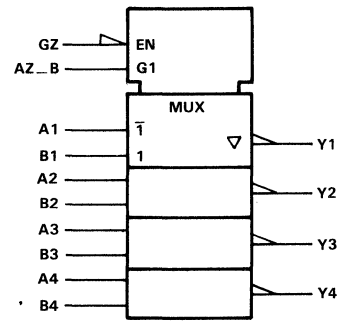


258A

QUADRUPLE 2-LINE TO 1-LINE INVERTING MULTIPLEXERS WITH 3-STATE OUTPUTS

CELL NAME	t_{pd} (ns)		C_{pd}† (pF)
	C_L = 0 pF	C_L = 1 pF	
S258ALH	5.0	6.7	7.28
Label: S258ALH A1,A2,A3,A4,B1,B2,B3,B4,GZ,AZ__B, Y1,Y2,Y3,Y4;			

logic symbol



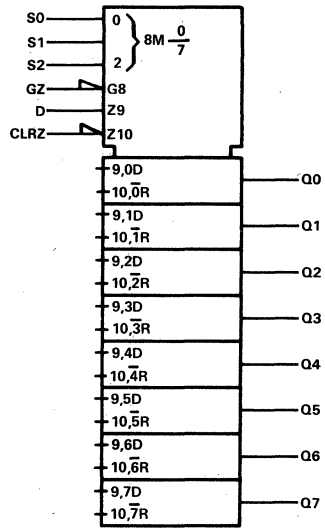
†The equivalent power dissipation capacitance does not include interconnect capacitance.

259

8-BIT ADDRESSABLE LATCHES

CELL NAME	t_{pd} (ns)		C_{pd}† (pF)
	C_L = 0 pF	C_L = 1 pF	
S259LH	6.0	6.6	40.59
Label: S259LH CLRZ,D,GZ,S0,S1,S2,Q0,Q1,Q2,Q3,Q4, Q5,Q6,Q7;			

logic symbol

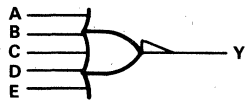


260

5-INPUT POSITIVE-NOR GATES

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
NO510LH	1.7	5.0	0.37
NO520LH	1.6	3.2	0.64
Label: NO5n0LH A,B,C,D,E,Y;			

logic symbol



266

2-INPUT EXCLUSIVE-NOR GATES

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
EN210LH	1.4	2.4	1.09
Label: EN210LH A,B,Y;			

logic symbol

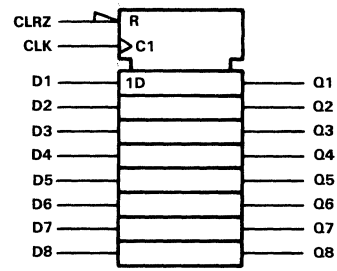
†The equivalent power dissipation capacitance does not include interconnect capacitance.

273

OCTAL D-TYPE FLIP-FLOPS

CELL NAME	t_{pd} (ns)		C_{pd}† (pF)
	C_L = 0 pF	C_L = 1 pF	
S273LH	5.0	5.8	22.45
Label: S273LH D1,D2,D3,D4,D5,D6,D7,D8,CLK,CLRZ, Q1,Q2,Q3,Q4,Q5,Q6,Q7,Q8;			

logic symbol

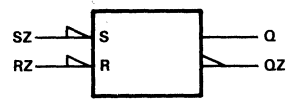


279

S-R LATCHES

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
LAB10LH	2.0	2.8	2.11
LAB20LH	2.2	2.7	3.20
Label: LABn0LH SZ,RZ,Q,QZ;			

logic symbol

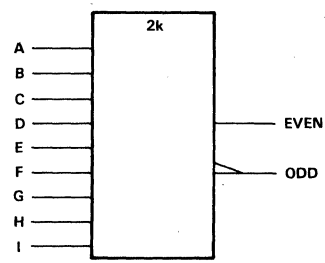


280

9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

CELL NAME	t_{pd} (ns)		C_{pd}† (pF)
	C_L = 0 pF	C_L = 1 pF	
S280LH	11.0	11.5	25.80
Label: S280LH A,B,C,D,E,G,H,I,EVEN,ODD;			

logic symbol



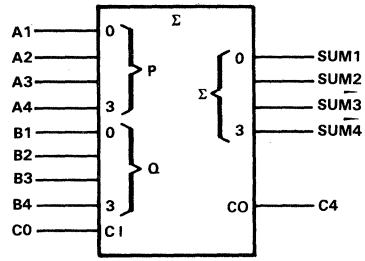
†The equivalent power dissipation capacitance does not include interconnect capacitance.

283

4-BIT BINARY FULL ADDERS WITH FAST CARRY

CELL NAME	t_{pd} (ns)		C_{pd}† (pF)
	C_L = 0 pF	C_L = 1 pF	
S283LH	8.5	9.1	36.28
Label: S283LH A4,A3,A2,A1,B4,B3,B2,B1,C0,SUM4, SUM3,SUM2,SUM1,C4;			

logic symbol

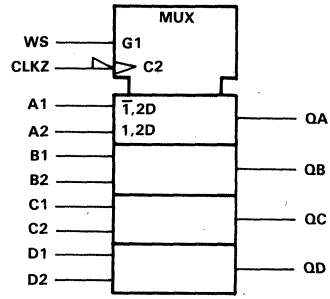


298

QUADRUPLE 2-INPUT MULTIPLEXERS WITH NEGATIVE-EDGE-TRIGGERED REGISTER

CELL NAME	t_{pd} (ns)		C_{pd}† (pF)
	C_L = 0 pF	C_L = 1 pF	
S298LH	6.0	6.8	18.72
Label: S298LH A1,A2,B1,B2,C1,C2,D1,D2, CLKZ,WS,QA,QB,QC,QD;			

logic symbol



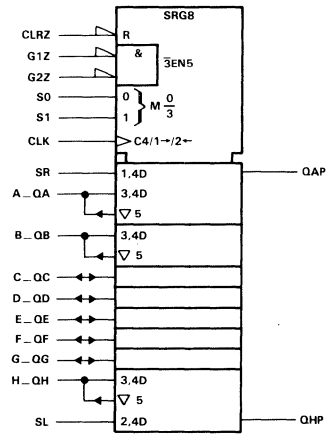
†The equivalent power dissipation capacitance does not include interconnect capacitance.

299

8-BIT BIDIRECTIONAL UNIVERSAL SHIFT/STORAGE REGISTERS

CELL NAME	t_{pd} (ns)		C_{pd}† (pF)
	C_L = 0 pF	C_L = 1 pF	
S299LH	7.1	8.0	60.02
Label: S299LH S0,S1,G1Z,G2Z,SL,SR,CLK,CLRZ,QAP, QHP,A_QA,B_QB,C_QC,D_QD,E_QE, F_QF,G_QG,H_QH;			

logic symbol

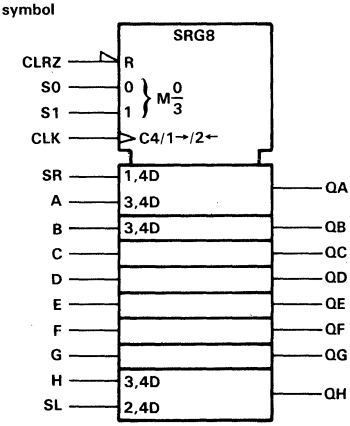


299X

8-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

CELL NAME	t_{pd} (ns)		C_{pd}† (pF)
	C_L = 0 pF	C_L = 1 pF	
S299XLH	5.0	5.9	48.89
Label: S299XLH A,B,C,D,E,F,G,H,S0,S1,SL,SR,CLK, CLRZ,QA,QB,QC,QD,QE,QF,QG,QH;			

logic symbol



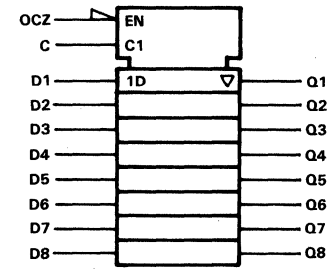
†The equivalent power dissipation capacitance does not include interconnect capacitance.

373

8-BIT D-TYPE LATCHES WITH 3-STATE OUTPUTS

CELL NAME	t_{pd} (ns)		C_{pd}† (pF)
	C_L = 0 pF	C_L = 1 pF	
S373LH	5.0	6.7	17.07
Label: S373LH D1,D2,D3,D4,D5,D6,D7,D8,C,OCZ,Q1, Q2,Q3,Q4,Q5,Q6,Q7,Q8;			

logic symbol

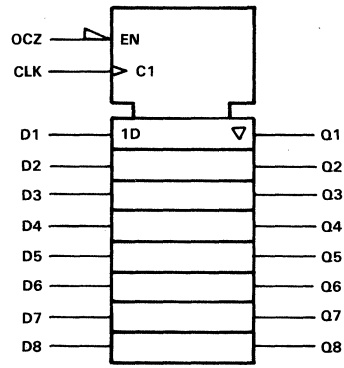


374

8-BIT D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

CELL NAME	t_{pd} (ns)		C_{pd}† (pF)
	C_L = 0 pF	C_L = 1 pF	
S374LH	5.0	6.7	22.80
Label: S374LH D1,D2,D3,D4,D5,D6,D7,D8,CLK,OCZ, Q1,Q2,Q3,Q4,Q5,Q6,Q7,Q8;			

logic symbol

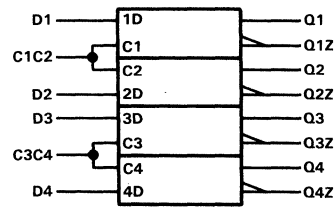


375

4-BIT BISTABLE LATCHES

CELL NAME	t_{pd} (ns)		C_{pd}† (pF)
	C_L = 0 pF	C_L = 1 pF	
S375LH	4.5	6.0	7.32
Label: S375LH D1,D2,D3,D4,C1C2,C3C4,Q1,Q1Z,Q2, Q2Z,Q3,Q3Z,Q4,Q4Z;			

logic symbol



†The equivalent power dissipation capacitance does not include interconnect capacitance.

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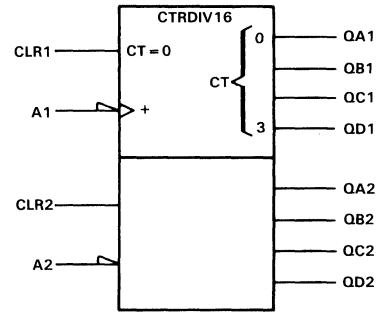
393

DUAL 4-BIT RIPPLE COUNTERS

CELL NAME	t_{pd} (ns)		C_{pd}† (pF)
	C_L = 0 pF	C_L = 1 pF	
S393LH	21.0	21.5	16.92
Label: S393LH A1,CLR1,A2,CLR2,QA1,QB1,QC1,QD1, QA2,QB2,QC2,QD2;			

logic symbol

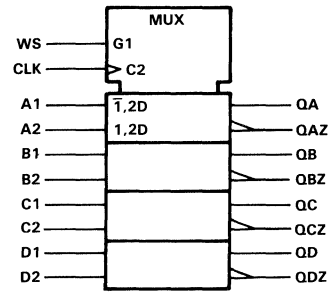


398

QUADRUPLE 2-INPUT MULTIPLEXERS WITH POSITIVE-EDGE-TRIGGERED COMPLEMENTARY OUTPUT REGISTER

CELL NAME	t_{pd} (ns)		C_{pd}† (pF)
	C_L = 0 pF	C_L = 1 pF	
S398LH	5.5	6.4	19.42
Label: S398LH A1,A2,B1,B2,C1,C2,D1,D2,CLK,WS,QA, QAZ,QB,QBZ,QC,QCZ,QD,QDZ;			

logic symbol



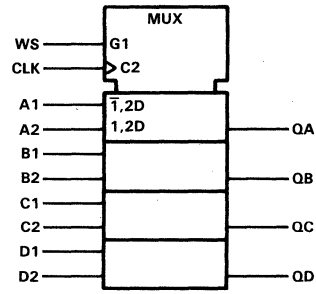
†The equivalent power dissipation capacitance does not include interconnect capacitance.

399

QUADRUPLE 2-INPUT MULTIPLEXERS WITH POSITIVE-EDGE-TRIGGERED REGISTER

CELL NAME	t_{pd} (ns)		C_{pd}† (pF)
	C_L = 0 pF	C_L = 1 pF	
S399LH	5.0	5.8	17.92
Label: S399LH A1,A2,B1,B2,C1,C2,D1,D2,CLK,WS,QA, QB,QC,QD;			

logic symbol

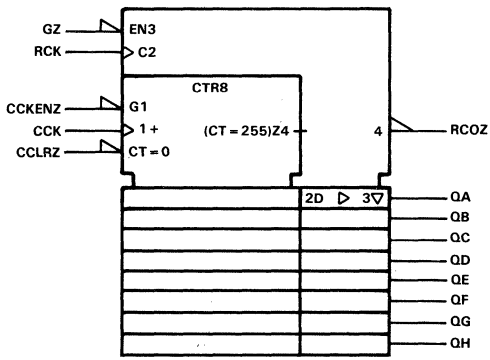


590

8-BIT BINARY COUNTERS WITH 3-STATE OUTPUT REGISTERS

CELL NAME	t_{pd} (ns)		C_{pd}† (pF)
	C_L = 0 pF	C_L = 1 pF	
S590LH	10.4	12.1	58.24
Label: S590LH CCK,CCKENZ,RCK,CCLRZ,GZ,QA,QB,QC, QD,QE,QF,QG,QH,RCOZ;			

logic symbol



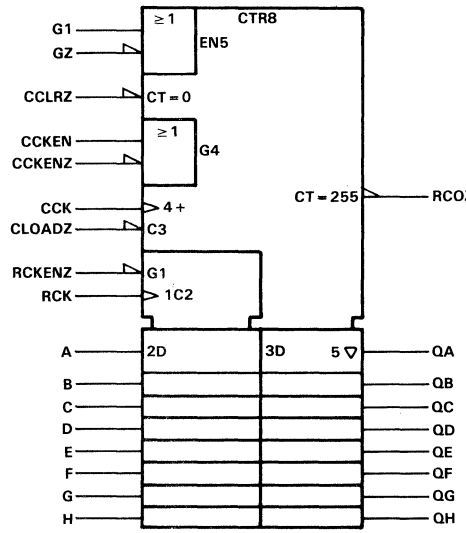
†The equivalent power dissipation capacitance does not include interconnect capacitance.

593X

8-BIT BINARY COUNTERS WITH INPUT REGISTERS

CELL NAME	t_{pd} (ns)		C_{pd}† (pF)
	C_L = 0 pF	C_L = 1 pF	
S593XLH	10.0	11.7	85.86
Label: S593XLH A,B,C,D,E,F,G,H,CCK,CCKEN,CCKENZ, RCK,RCKENZ,CCLRZ,CLOADZ,G1,GZ,QA,QB,QC, QD,QE,QF,QG,QH,RCOZ;			

logic symbol

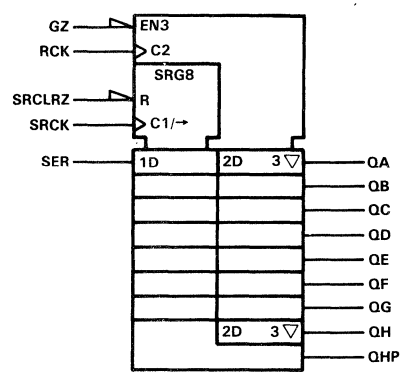


595

8-BIT SHIFT REGISTERS WITH OUTPUT REGISTERS

CELL NAME	t_{pd} (ns)		C_{pd}† (pF)
	C_L = 0 pF	C_L = 1 pF	
S595LH	5.5	7.2	44.64
Label: S595LH SER,SRCK,SRCLRZ,RCK,GZ,QA,QB,QC, QD,QE,QF,QG,QH,QHP;			

logic symbol



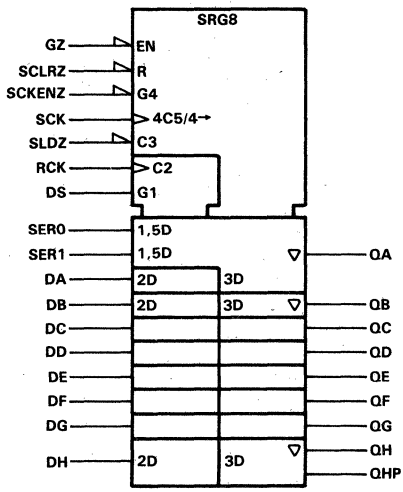
†The equivalent power dissipation capacitance does not include interconnect capacitance.

598X

8-BIT SHIFT REGISTERS WITH INPUT REGISTERS

CELL NAME	t_{pd} (ns)		C_{pd}† (pF)
	C_L = 0 pF	C_L = 1 pF	
S598XLH	9.8	11.5	82.63
Label: S598XLH A,B,C,D,E,F,G,H,RCK,SRCK,SRCKEZ, SRLOADZ,SRCLRZ,SER0,SER1,DS,GZ,QA,QB, QC,QD,QE,QF,QG,QH,QHP;			

logic symbol

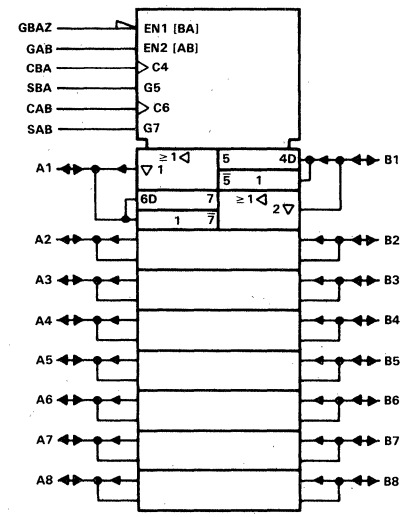


651

8-BIT BIDIRECTIONAL UNIVERSAL TRANSCEIVER REGISTERS

CELL NAME	t_{pd} (ns)		C_{pd}† (pF)
	C_L = 0 pF	C_L = 1 pF	
S651LH	10.4	11.3	91.06
Label: S651LH GBAZ,GAB,SBA,SAB,CBA,CAB,A1,A2,A3, A4,A5,A6,A7,A8,B1,B2,B3,B4,B5,B6,B7,B8;			

logic symbol



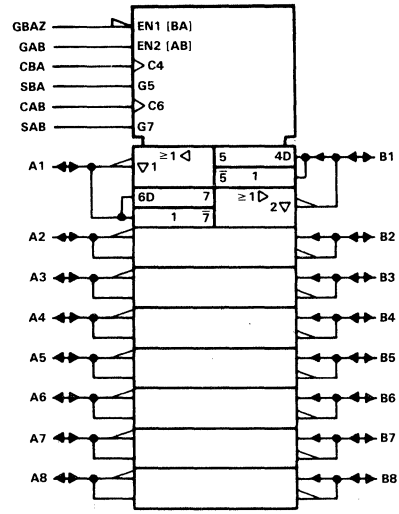
†The equivalent power dissipation capacitance does not include interconnect capacitance.

652

8-BIT BIDIRECTIONAL UNIVERSAL TRANSCEIVER REGISTERS

CELL NAME	t_{pd} (ns)		C_{pd}† (pF)
	C_L = 0 pF	C_L = 1 pF	
S652LH	10.4	11.3	104.10
Label: S652LH GBAZ,GAB,SBA,SAB,CBA,CAB,A1,A2,A3, A4,A5,A6,A7,A8,B1,B2,B3,B4,B5,B6,B7,B8;			

logic symbol

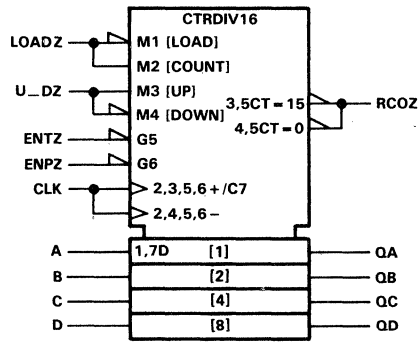


669

SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS WITH LOOK-AHEAD

CELL NAME	t_{pd} (ns)		C_{pd}† (pF)
	C_L = 0 pF	C_L = 1 pF	
S669LH	10.0	11.8	30.7
Label: S669LH D,C,B,A,CLK,U__DZ,ENPZ,ENTZ,LOADZ, QD,QC,QB,QA,RCOZ;			

logic symbol



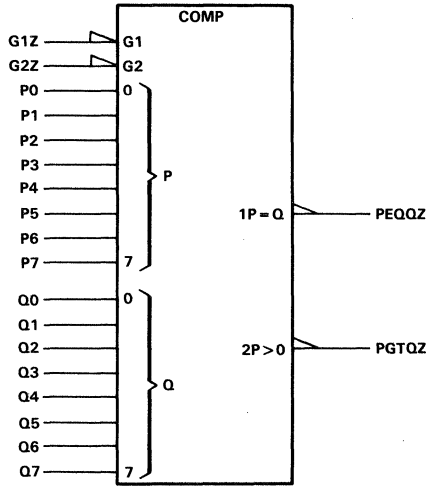
†The equivalent power dissipation capacitance does not include interconnect capacitance.

686

8-BIT MAGNITUDE COMPARATORS

CELL NAME	t_{pd} (ns)		C_{pd}† (pF)
	C_L = 0 pF	C_L = 1 pF	
S686LH	9.0	9.8	43.30
Label: S686LH P0,P1,P2,P3,P4,P5,P6,P7,Q0,Q1,Q2, Q3,Q4,Q5,Q6,Q7,G1Z,G2Z,PEQQZ,PGTQZ;			

logic symbol

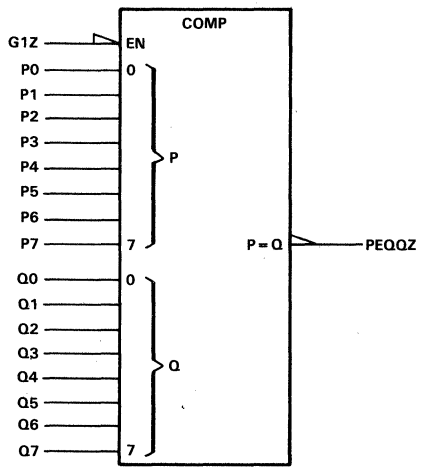


688

8-BIT IDENTITY COMPARATORS

CELL NAME	t_{pd} (ns)		C_{pd}† (pF)
	C_L = 0 pF	C_L = 1 pF	
S688LH	7.5	8.2	15.94
Label: S688LH P0,P1,P2,P3,P4,P5,P6,P7,Q0,Q1,Q2, Q3,Q4,Q5,Q6,Q7,G1Z,PEQQZ;			

logic symbol



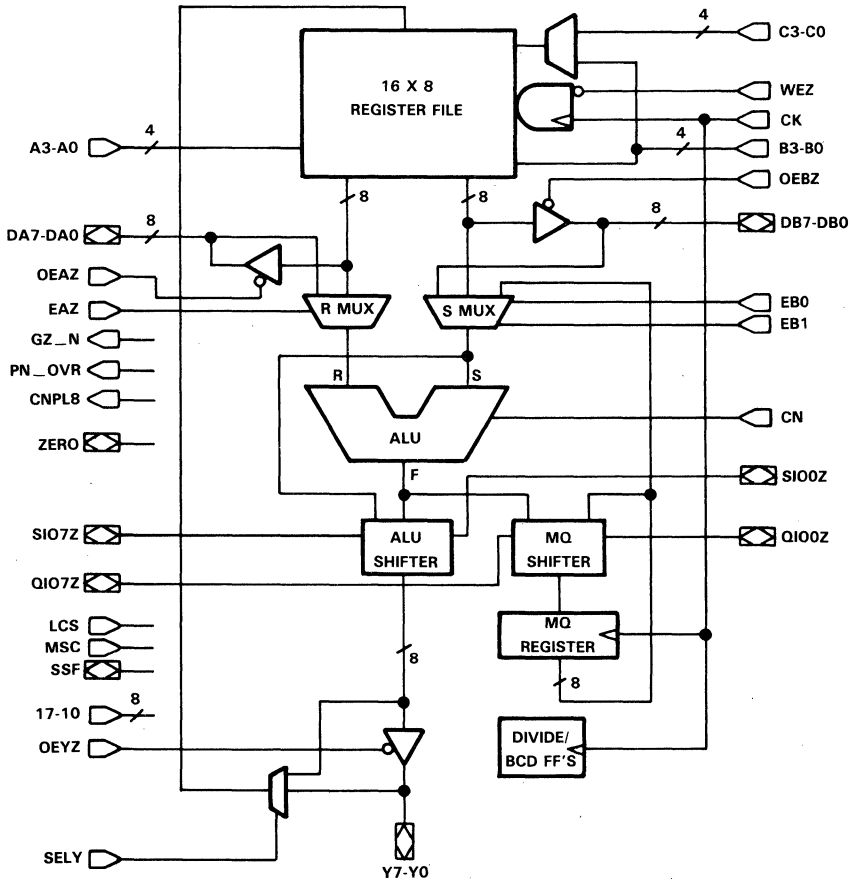
†The equivalent power dissipation capacitance does not include interconnect capacitance.

888

8-BIT PROCESSOR SLICES

- Parallel 8-bit ALU with expansion nodes
- Signed magnitude to/from two's complement conversion
- Single- and double-length normalize
- Signed and unsigned divides with overflow detection; input does not need to be prescaled
- Signed, mixed, and unsigned multiples
- Sign, carry out, overflow and zero-detect status capabilities
- 3-Operand register files allow an operation and a move instruction to be combined
- 3 data input/output ports maximize data throughput

functional block diagram

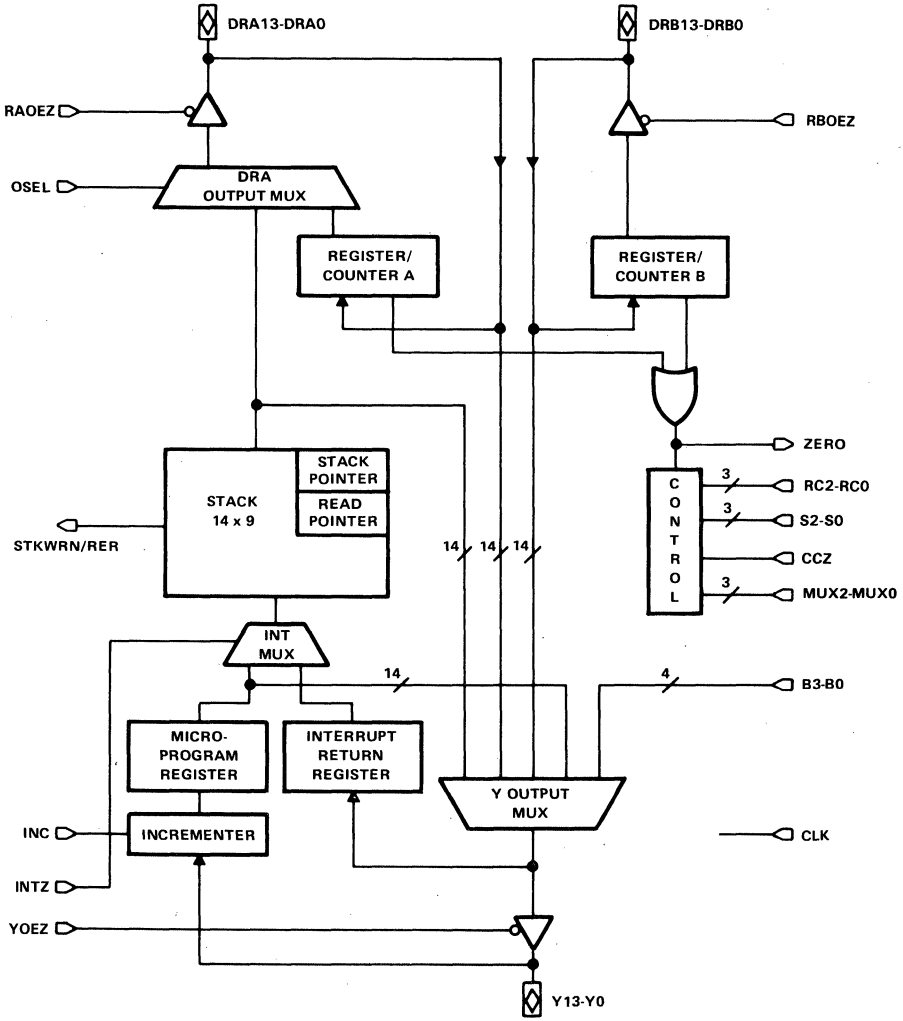


890

MICROSEQUENCES

- 14 bits wide-addresses up to 16,384 words of microcode with one megacell
- Selects address from one of eight sources
- Independent read pointer for aid in microcode diagnostics
- Supports read-time interrupts
- Two independent loop counters
- Supports 64 powerful instructions

functional block diagram



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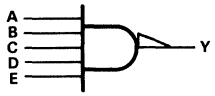
2022

5-INPUT POSITIVE-NAND GATES

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
NA510LH	1.3	2.7	0.52
NA520LH	1.2	2.1	1.02
Label: NA5n0LH A,B,C,D,E,Y;			

logic symbol

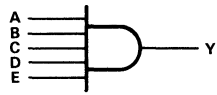


2024

5-INPUT POSITIVE-AND GATES

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
AN510LH	2.1	2.9	1.12
Label: AN510LH A,B,C,D,E,Y;			

logic symbol

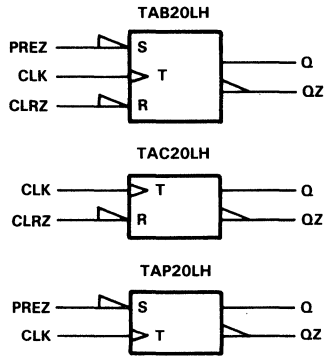


2102

TOGGLE FLIP-FLOPS WITH PRESET/CLEAR

CELL NAME	fmax (MHz)	C_{pd} (pF)
TAB20LH	54.2	4.20
Label: TAB20LH CLRZ,PREZ,CLK,Q,QZ;		
TAC20LH	61.7	3.79
Label: TAC20LH CLRZ,CLK,Q,QZ;		
TAP20LH	65.8	3.59
Label: TAP20LH PREZ,CLK,Q,QZ;		

logic symbol

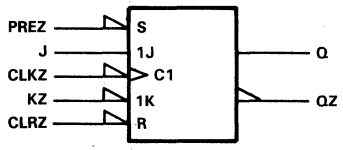


2108

J-$\overline{K}$-TYPE NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS

CELL NAME	fmax (MHz)	C_{pd} (pF)
JKB21LH	44.2	4.97
Label: JKB21LH CLRZ,PREZ,J,KZ,CLKZ,Q,QZ;		

logic symbol

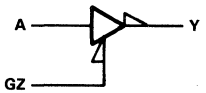


2310

INVERTING 3-STATE BUFFERS WITH ACTIVE-LOW ENABLE

logic symbol

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
IV211LH	0.9	2.6	0.49
IV221LH	0.9	1.7	1.00
IV241LH	0.8	1.3	1.88
Label: IV2n1LH A,GZ,Y;			

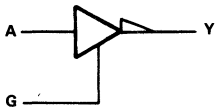


2311

INVERTING 3-STATE BUFFERS WITH ACTIVE-HIGH ENABLE

logic symbol

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
IV212LH	1.5	2.6	0.50
IV222LH	1.5	1.8	0.98
IV242LH	0.8	1.3	1.86
Label: IV2n2LH A,G,Y;			



2320

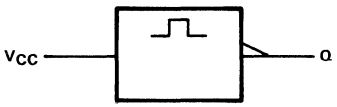
POWER-UP-CLEAR 1-SHOT

logic symbol

CELL NAME: PUC00LH

- Automatically triggered by rising edge of power-up supply voltage
- Provides initialization pulse for clearing/presetting registers

Label: PUC00LH Q;



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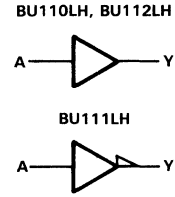
2321

BUFFERS

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
BU110LH	2.2	3.0	0.74
BU111LH	3.0	4.0	0.83
BU112LH	2.0	3.0	0.56
Label: BU11nLH A,Y;			

logic symbol

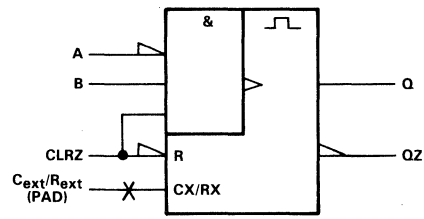


2322

RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
MVF00LH	8	9	20.5
Label: MVF00LH A,B,CLRZ,Q,QZ;			

logic symbol



2325

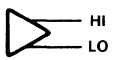
HIGH-LEVEL AND LOW-LEVEL TIE-OFF GATES

CELL NAME: TO010LH

- Provides dc termination for high- and low-level unused inputs

Label: TO010LH LO,HI;

logic symbol

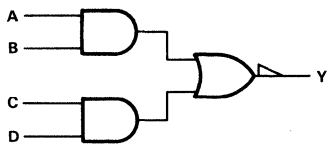


2330

2-WIDE, 2-INPUT AND-NOR GATES

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
AO221LH	1.2	2.6	0.59
Label: AO221LH A,B,C,D,Y;			

logic symbol

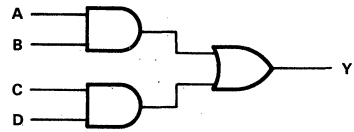


2331

2-WIDE, 2-INPUT AND-OR GATES

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
AO220LH	1.7	2.6	0.90
Label: AO220LH A,B,C,D,Y;			

logic symbol

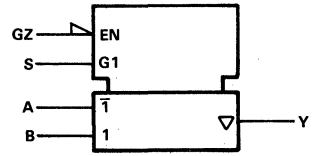


2340

2-LINE TO 1-LINE MULTIPLEXERS

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
MU110LH	2.3	3.7	0.92
Label: MU110LH A,B,S,GZ,Y;			

logic symbol

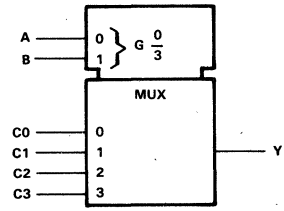


2341

4-LINE TO 1-LINE MULTIPLEXERS

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
MU210LH	2.1	2.9	1.28
Label: MU210LH C0,C1,C2,C3,A,B,Y;			

logic symbol

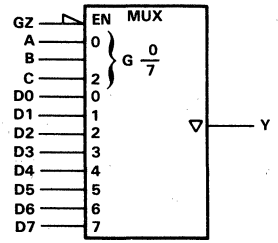


2342

8-LINE TO 1-LINE MULTIPLEXERS WITH 3-STATE OUTPUTS

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
MU310LH	3.2	4.7	1.68
Label: MU310LH A,B,C,D0,D1,D2,D3,D4,D5,D6,D7,GZ,Y;			

logic symbol



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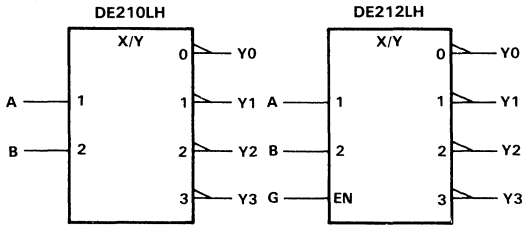
2350

2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
DE210LH	1.0	2.0	2.91
Label: DE210LH A,B,Y0,Y1,Y2,Y3;			
DE212LH	1.0	2.5	2.81
Label: DE212LH A,B,G,Y0,Y1,Y2,Y3;			

logic symbol



2370

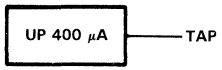
400-μA PULL-UP ACTIVE TERMINATORS

CELL NAME: PR400LH

- Provides active termination for inputs or I/Os

Label: PR400LH TAP;

logic symbol



2371

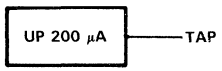
200-μA PULL-UP ACTIVE TERMINATORS

CELL NAME: PR250LH

- Provides active termination for inputs or I/Os

Label: PR250LH TAP;

logic symbol



2372

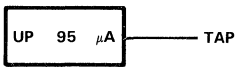
95-μA PULL-UP ACTIVE TERMINATORS

CELL NAME: PR095LH

- Provides active termination for inputs or I/Os

Label: PR095LH TAP;

logic symbol



2373

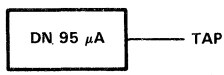
95-μA PULL-DOWN ACTIVE TERMINATORS

CELL NAME: PD095LH

- Provides active termination for inputs or I/Os

Label: PD095LH TAP;

logic symbol



2374

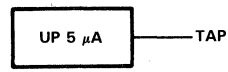
5-μA PULL-UP ACTIVE TERMINATORS

CELL NAME: PR005LH

- Provides active termination for inputs or I/Os

Label: PR005LH TAP;

logic symbol

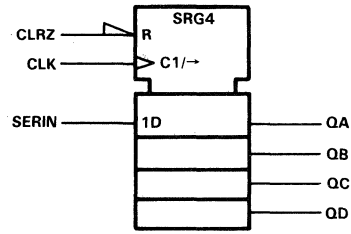


2401

4-BIT SHIFT REGISTERS

CELL NAME	fmax (MHz)	C_{pd} (pF)
R2401LH	59.6	10.30
Label: R2401LH CLRZ,SERIN,CLK,QA,QB,QC,QD;		

logic symbol

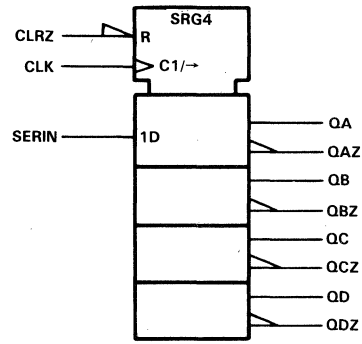


2402

4-BIT SHIFT REGISTERS

CELL NAME	fmax (MHz)	C_{pd} (pF)
R2402LH	59.6	12.10
Label: R2402LH CLRZ,SERIN,CLK,QA,QAZ,QB,QBZ,QC, QCZ,QD,QDZ;		

logic symbol



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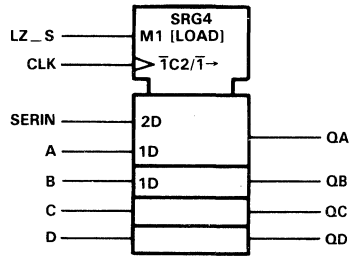
2403

4-BIT SHIFT REGISTERS

CELL NAME	fmax (MHz)	C_{pd} (pF)
R2403LH	59.6	11.10
Label: R2403LH SERIN,LZ_S,CLK,A,B,C,D,QA,QB, QC,QD;		

logic symbol

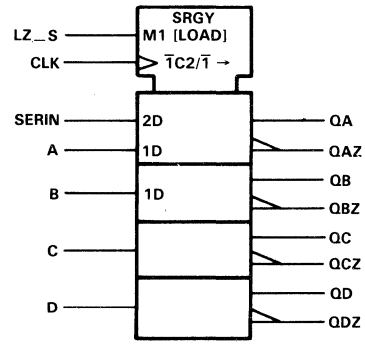


2404

4-BIT SHIFT REGISTERS

CELL NAME	fmax (MHz)	C_{pd} (pF)
R2404LH	59.6	12.10
Label: R2404LH SERIN,LZ_S,CLK,A,B,C,D,QA,QAZ, QB,QBZ,QC,QCZ,QD,QDZ;		

logic symbol

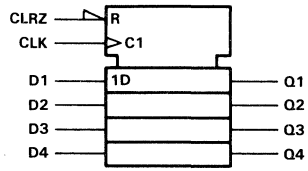


2405

4-BIT FLIP-FLOPS/REGISTERS

CELL NAME	fmax (MHz)	C_{pd} (pF)
R2405LH	64.2	10.20
Label: R2405LH CLRZ,D1,D2,D3,D4,CLK,Q1,Q2,Q3,Q4;		

logic symbol

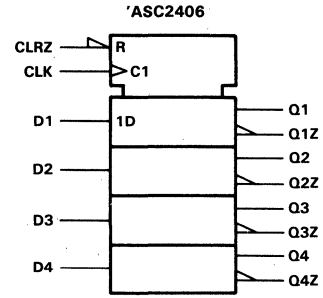


2406

4-BIT FLIP-FLOPS/REGISTERS

CELL NAME	fmax (MHz)	C_{pd} (pF)
R2406LH	64.2	11.70
Label: R2406LH CLRZ,D1,D2,D3,D4,CLK,Q1, Q1Z,Q2,Q2Z,Q3,Q3Z,Q4,Q4Z;		

logic symbol

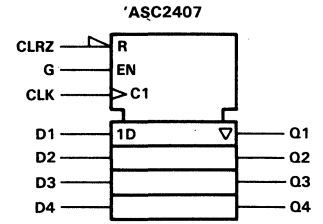


2407

4-BIT FLIP-FLOPS/REGISTERS

CELL NAME	fmax (MHz)	C_{pd} (pF)
R2407LH	36.3	11.00
Label: R2407LH CLRZ,D1,D2,D3,D4,CLK,G,Q1,Q2, Q3,Q4;		

logic symbol

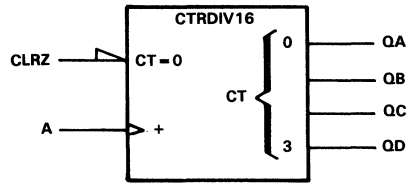


2408

4-BIT RIPPLE COUNTERS

CELL NAME	fmax (MHz)	C_{pd} (pF)
R2408LH	59.6	7.22
Label: R2408LH CLRZ,A,QA,QB,QC,QD;		

logic symbol

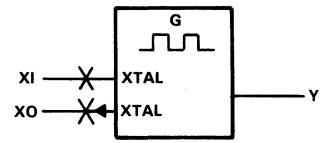


2500

CRYSTAL-CONTROLLED OSCILLATORS

CELL NAME	MAXIMUM FREQUENCY	C_{pd} (pF)
OSE00LH	5 MHz	8.13
OSF02LH	20 MHz	15.30
OSE06LH	800 MHz	6.82
Label: OSE03LH RC, Y;		

logic symbol



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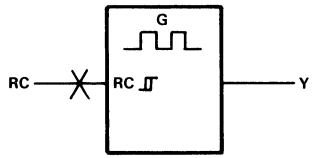
2502

RC OSCILLATORS

CELL NAME	TYPICAL FREQUENCY RANGE	C_{pd} (pF)
OSE03LH	5 to 20 MHz	2.44
Label: OSE03LH RC, Y;		

logic symbol



2503

DIFFERENTIAL COMPARATORS

logic symbol

CELL NAMES: C0212LH, C0213LH

- Single 5 volt supply with ± 10% tolerance
- Inputs are ESD-protected
- Input offset voltage--50 mV max
- Common mode input voltage: C0212LH – 0 V to 3.5 V
  C0213LH – 1.5 V to VCC

P-CHANNEL Label: CO212LH IN,INZ,OUT;
N-CHANNEL Label: CO213LH IN,INZ,OUT;

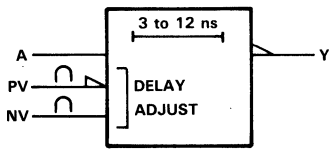
2507

DYNAMIC DELAY ELEMENT

logic symbol

CELL NAME: DLE10LH

Label: DLE10LH A,PV,NV,Y;



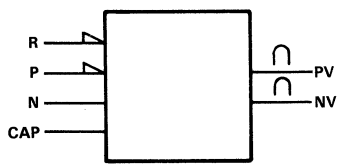
2508

CONTROL ELEMENT FOR DYNAMIC DELAY ELEMENT

logic symbol

CELL NAME: DLC10LH

Label: DLC10LH P,N,R,CAP,PV,NV;



2519

MEDIUM-DRIVE OPERATIONAL AMPLIFIER

logic symbol

CELL NAME: AMC12NH

- Single 5-volt supply ± 10%
- Internally frequency-compensated
- Inputs are ESD-protected
- Input offset voltage −50 mV typical
- Output voltage swing −1 V to 4.5 V

Label: AMC12NH, IN,INZ,OUT;

2901

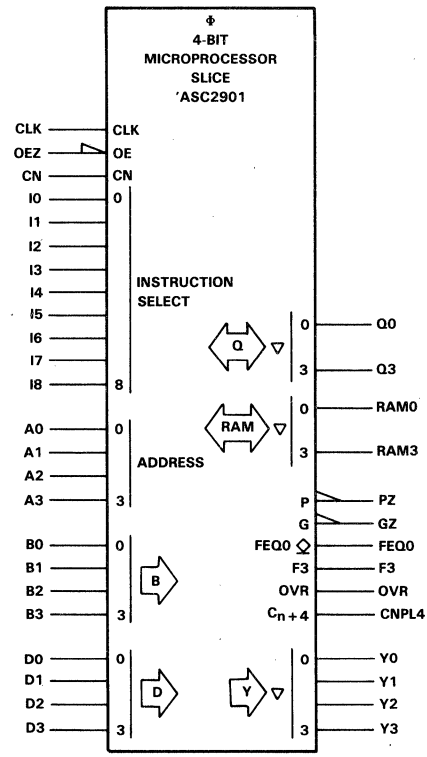
4-BIT MICROPROCESSOR SLICE

logic symbol

CELL NAME: M01MPLH

- Reduces 2901 4-bit microprocessor to a single cell
- Offers full system implementation on a single chip, when used with other members of the 2900 family

Label: M01MPLH CLK,QEZ,CN,I8 . . . I0,B3 . . . B0,A3 . . . A0, D3 . . . D0,Q3,Q0,RAM3,RAM0,GZ,PZ,F3, FEQ0,OVR,CNPL4,Y3 . . . Y0;



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2902

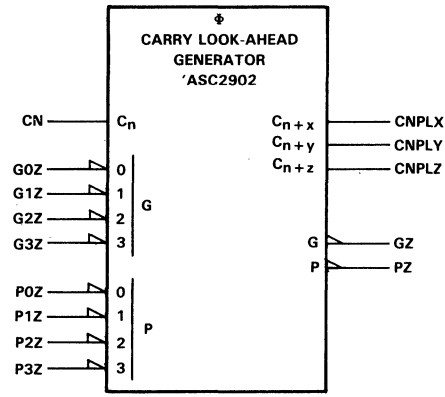
LOOK-AHEAD CARRY GENERATOR

CELL NAME: M02CGLH

- Designed to accept up to four pairs of carry-propagate and carry-generate signals, and a carry input
- Provides anticipated carries across four groups of binary ALUs

Label: M02CGLH CN,G3Z,P3Z,G2Z,P2Z,G1Z,P1Z,G0Z,P0Z, CNPLX,CNPLY,CNPLZ,GZ,PZ;

logic symbol



2904

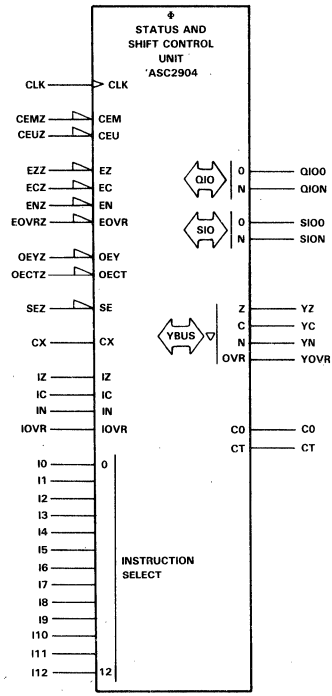
STATUS AND SHIFT CONTROLLER

CELL NAME: M04SSLH

- Generates the carry-in signal to the ALU and carry look-ahead
- Serves as interconnects for the data path, the auxiliary operations, and the ALU status flags testing
- Offers full system implementation on a single chip, when used with other members of the 2900 family

Label: M04SSLH CLK,CEMZ,CEUZ,EZZ,ECZ,ENZ,EOVRZ,OEYZ, OECTZ,SEZ,CX,IZ,IC,IN,IOVR,I12 . . . I0,YZ,YC,YN, YOVR,SIO0,SION,QIO0,QION,CO,CT;

logic symbol



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2910

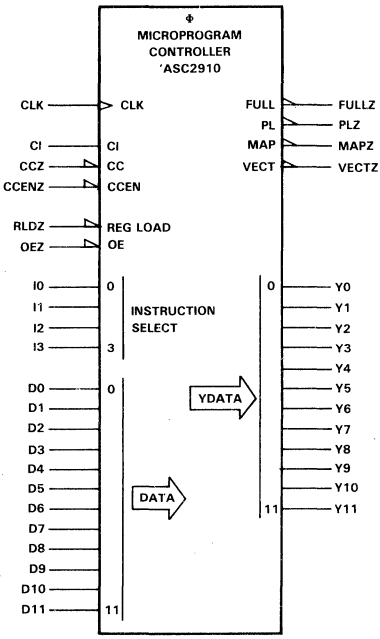
MICROPROGRAM CONTROLLER

CELL NAME: M10MCLH

- Supports the function of an address sequencer in controlling the execution of microinstructions stored in microprogram memory
- Last-in, first-out stack provides for nine levels of nesting microsubroutines

Label: M10MCLH CLK,CI,CCZ,CCENZ,RLDZ,OEZ,I3 . . . I0, D11 . . . D0,FULLZ,PLZ,MAPZ,VECTZ,Y11 . . . Y0;

logic symbol



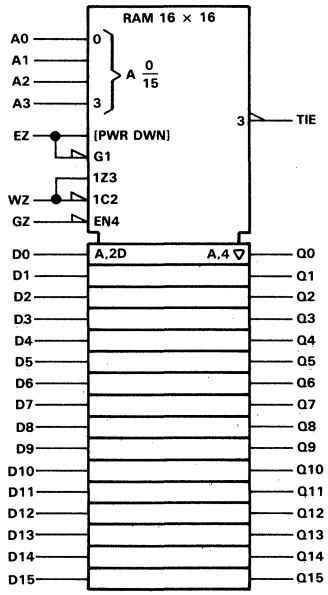
3003

STATIC 16W *X* 16B READ/WRITE RAMs WITH 3-STATE OUTPUTS

CELL NAME	ORGANIZATION	
	WORDS	BITS
RA416LH	16	16
Label: RA416LH D0,D1,D2,D3,D4,D5,D6,D7,D8,D9, D10,D11,D12,D13,D14,D15,A0,A1,A2,A3, EZ,WZ,GZ,Q0,Q1,Q2,Q3,Q4,Q5,Q6,Q7,Q8, Q9,Q10,Q11,Q12,Q13,Q14,Q15,TIE;		

logic symbol

RA416LH



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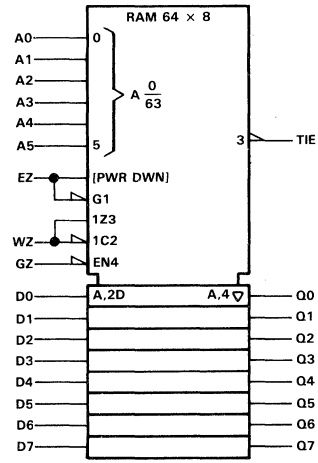
3004

STATIC 64W X 8B READ/WRITE RAMs WITH 3-STATE OUTPUTS

CELL NAME	ORGANIZATION	
	WORDS	BITS
RA608LH	64	8
Label: RA608LH D0,D1,D2,D3,D4,D5,D6,D7,A0,A1, A2,A3,A4,A5,EZ,WZ,GZ,Q0,Q1,Q2,Q3,Q4, Q5,Q6,Q7,TIE;		

logic symbol

RA608LH



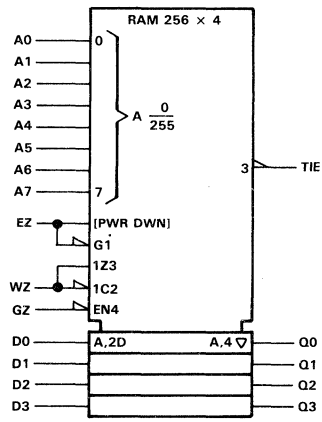
3005

STATIC 256W X 4B READ/WRITE RAMs WITH 3-STATE OUTPUTS

CELL NAME	ORGANIZATION	
	WORDS	BITS
RA804LH	256	4
Label: RA804LH D0,D1,D2,D3,A0,A1,A2,A3,A4,A5, A6,A7,EZ,WZ,GZ,Q0,Q1,Q2,Q3,TIE;		

logic symbol

RA804LH

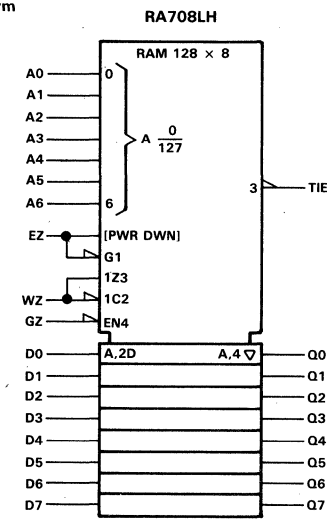


3006

STATIC 128W *X* 8B READ/WRITE RAMs WITH 3-STATE OUTPUTS

CELL NAME	ORGANIZATION	
	WORDS	BITS
RA708LH	128	8
Label: RA708LH D0,D1,D2,D3,D4,D5,D6,D7,A0,A1, A2,A3,A4,A5,A6,EZ,WZ,GZ,Q0,Q1,Q2,Q3, Q4,Q5,Q6,Q7,TIE;		

logic sym



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3010

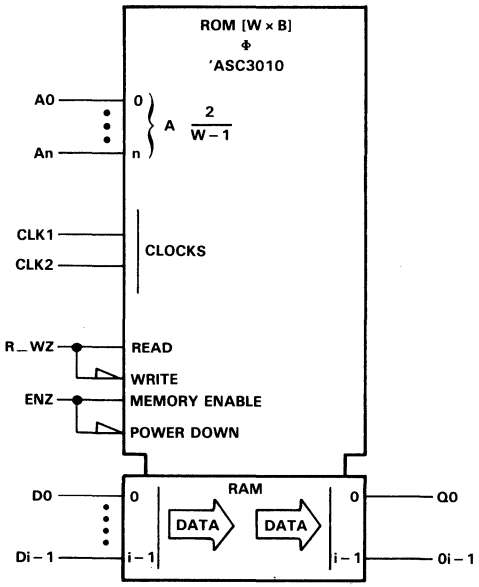
CompilerCell™
STATIC RANDOM ACCESS MEMORIES (SRAM)

SRAM Array Limits

CELL NAME	PARAMETERS	MIN	MAX	COMMENTS
AZRMLB†	Number of words ($W \geq 2^n$)	4	1024	Any even number
	Wordlength (B=i)	4	32	Number of data inputs = number of data outputs = wordlength
	Total number of bits (W×B)	16	16384	

Label†: AZRMLB D0,D1,D2 . . . Di-1,A0, . . . An,CLK1,CLK2, ENZ,R_WZ,Q0, . . . Qi-1:
AZ: Identifying symbol
LB: Wordlength in bits. Topology dependent value.
M: Number of columns multiplied into one output. A = 1:1, B = 2:1, C = 4:1, D = 8:1. Topology dependent value.
R: Number of rows. Topology dependent value.

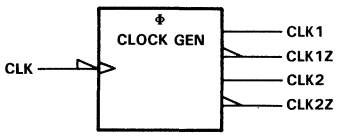
logic symbol



3011

2-PHASE CLOCK GENERATOR WITH COMPLEMENTARY OUTPUTS

logic symbol



CELL NAME: CK4X0LH

- Generates 2-phase clock for compiler cell functions
- Embedded function — requires no external connection
- Can be operated from single-phase of system on-chip clock

Label: CK4X0LH,CLK,CLK1,CLK1Z,CLK2,CLK2Z;

3103

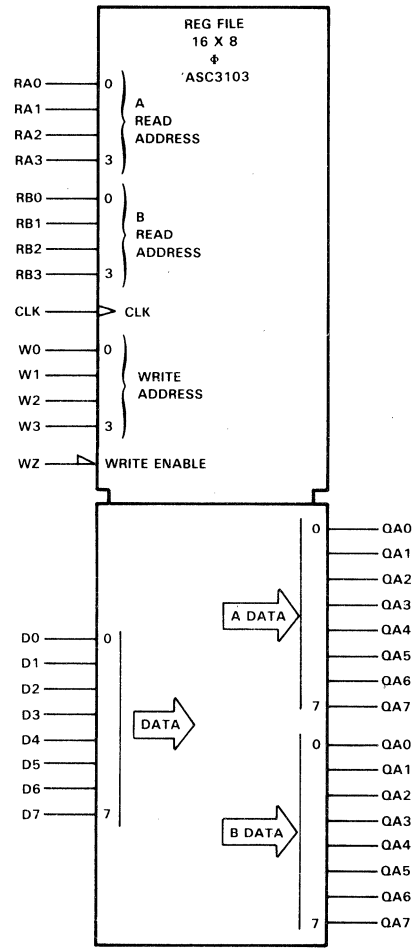
16-WORD BY 8-BIT EDGE-TRIGGERED 3-PORT REGISTER FILES

CELL NAME: RF408LH

- Full parallel access with one write and two read ports
- Typical access times:
  Write-then-read cycle time — 11 ns
  Address access time — 8 ns

Label: RF408LH, CLK,WZ,W0,W1,W2,W3,RA0,RA1,RA2,RA3, RB0,RB1,RB2,RB3,D0,D1,D2,D3,D4,D5,D6,D7,QA0, QA1,QA2,QA3,QA4,QA5,QA6,QA7,QB0,QB1,QB2, QB3,QB4,QB5,QB6,QB7;

logic symbol



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3200

CompilerCell™
READ-ONLY MEMORIES (ROM)

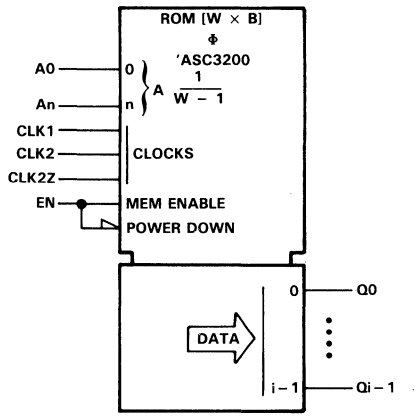
Single Array Parameter Limits

PARAMETERS	MIN	MAX	COMMENTS
Number of words ($W \geq 2^n$)	8	2048	Must be multiples of 4
Wordlength (B = i)	4	32	Even or odd
Total number of bits (W × B)	512	16384	

Double Array Parameter Limits

PARAMETERS	MIN	MAX	COMMENTS
Number of words ($W \geq 2^n$)	8	4096	Must be multiples of 4
Wordlength (B = i)	4	64	Must be even
Total number of bits (W × B)	512	65536	
Label: Label and cell name are developed as a function of cell design.			

logic symbol



3430

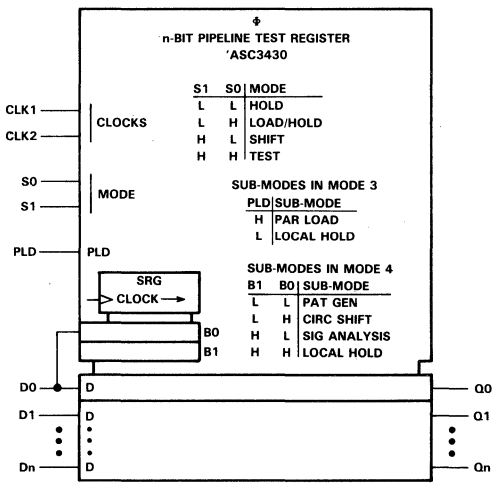
CompilerCell™
PIPELINE TEST REGISTERS (PTR)

Typical Modes of Operation:

- Pseudo-Random pattern generation
- Signature analysis
- Circular shift
- Local hold
- Serial or parallel load

Label: Label and cell name are developed as a function of cell design.

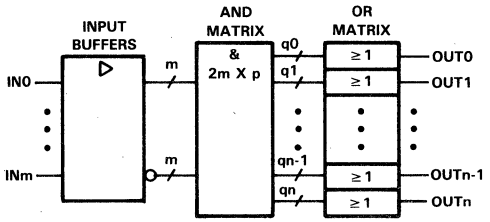
logic symbol



3800

CompilerCell™
PROGRAMMABLE LOGIC ARRAYS (PLA)

logic symbol



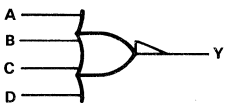
Maximum Parameter Values

INPUTS	PRODUCT TERM	OUTPUTS
m 64	p 128	n 32
Label: Label and cell name are developed as a function of cell design.		

4002

4-INPUT POSITIVE-NOR GATES

logic symbol

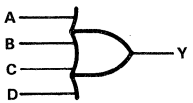


CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
NO410LH	1.4	4.1	0.35
NO420LH	1.2	2.6	0.55
Label: NO4n0LH A,B,C,D,Y;			

4072

4-INPUT POSITIVE-OR GATES

logic symbol



CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
OR410LH	2.2	3.1	0.92
OR420LH	2.6	3.1	1.83
OR440LH	2.4	2.7	3.46
OR460LH	2.4	2.7	5.48
Label: OR4n0LH A,B,C,D,Y;			

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4075

3-INPUT POSITIVE-OR GATES

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
OR310LH	1.8	2.7	0.90
OR320LH	2.2	2.7	1.71
OR340LH	1.9	2.2	3.51
OR360LH	2.0	2.2	5.36
Label: OR3n0LH A,B,C,Y;			

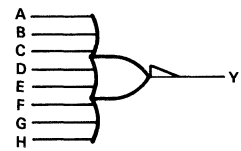
logic symbol

4078

8-INPUT POSITIVE-NOR GATES

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
NO810LH	2.6	3.4	1.54
NO820LH	2.3	4.9	0.65
Label: NO8n0LH A,B,C,D,E,F,G,H,Y;			

logic symbol



5000

CMOS-COMPATIBLE INVERTING INPUT BUFFERS

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
IPE00LH	0.7	1.1	2.00
IPF00LH	0.7	1.1	2.00
Label: IPF00LH A,Y;			

logic symbol

5001

TTL-COMPATIBLE INVERTING INPUT BUFFERS

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
IPE03LH	0.9	2.1	16.5
IPF03LH	0.9	2.1	16.5
Label: IPF03LH A,Y;			

logic symbol

5002

CMOS-COMPATIBLE INVERTING SCHMITT-TRIGGER INPUT BUFFERS

logic symbol

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
IPE06LH	2.8	4.8	1.30
IPF06LH	2.8	4.8	1.30
Label: IPF06LH A,TAP,Y;			

5003

TTL-COMPATIBLE INVERTING SCHMITT-TRIGGER INPUT BUFFERS WITH PULL-UP TAP

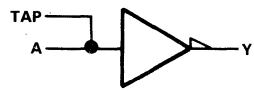
logic symbol

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
IPE08LH	3.7	7.5	19.00
IPF08LH	4.3	8.1	19.00
Label: IPE08LH A,TAP,Y;			

5004

CMOS-COMPATIBLE INVERTING INPUT BUFFERS WITH PULL-UP TAP

logic symbol

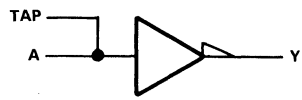


CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
IPF02LH	0.7	1.0	2.00
Label: IPF02LH A,TAP,Y;			

5005

TTL-COMPATIBLE INVERTING INPUT BUFFERS WITH PULL-UP TAP

logic symbol



CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
IPE05LH	0.9	2.1	16.00
IPF05LH	0.9	2.1	16.00
Label: IPF05LH A,TAP,Y;			

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5006

CMOS-COMPATIBLE NONINVERTING INPUT BUFFERS

logic symbol

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
IPE01LH	1.7	1.9	3.00
IPF01LH	0.7	1.1	3.00
Label: IPF01LH A,Y;			

5007

TTL-COMPATIBLE NONINVERTING INPUT BUFFERS

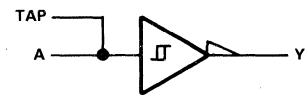
logic symbol

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
IPE04LH	1.8	2.1	18.00
IPF04LH	1.8	2.1	18.00
Label: IPF04LH A,Y;			
IPF12LH	1.4	1.6	18.00
Label: IPF12LH A,Y;			

5010

TTL-COMPATIBLE INVERTING SCHMITT-TRIGGER INPUT BUFFERS WITH PULL-UP TAP

logic symbol



CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
IPE10LH	3.7	7.5	20.00
IPF10LH	3.7	7.5	20.00
Label: IPF10LH A,TAP,Y;			

5013

TTL-COMPATIBLE NONINVERTING BUFFERS WITH PULL-UP TAP

logic symbol

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
IPF13LH	1.8	2.1	18.00
Label: IPF13LH A,TAP,Y;			

5100

TTL-/CMOS-COMPATIBLE OUTPUT BUFFERS

logic symbol

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 15 pF	C_L = 50 pF	
OPE40LH	2.7	4.7	9.10
OPF40LH	2.7	4.7	10.90
Label: OPF40LH A,Y;			

5103

TTL-/CMOS-COMPATIBLE OUTPUT BUFFERS

logic symbol

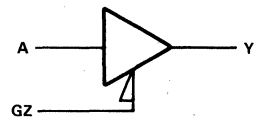
CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 15 pF	C_L = 50 pF	
OPE60LH	2.4	3.5	15.50
OPF60LH	2.4	3.5	17.30
Label: OPF60LH A,Y;			

5104

TTL-/CMOS-COMPATIBLE 3-STATE OUTPUT BUFFERS

logic symbol

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 15 pF	C_L = 50 pF	
OPE63LH	2.7	4.0	17.10
OPF63LH	2.7	4.0	19.40
Label: OPF63LH A,GZ,Y;			



5105

TTL-/CMOS-COMPATIBLE OPEN-DRAIN OUTPUT BUFFERS

logic symbol

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 15 pF	C_L = 50 pF	
OPE61LH	2.0	4.0	3.80
OPF61LH	2.0	4.0	4.00
Label: OPF61LH A,Y;			

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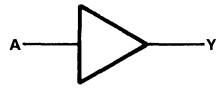
5106

TTL-/CMOS-COMPATIBLE OUTPUT BUFFERS

logic symbol

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 15 pF	C_L = 50 pF	
OPE00LH	2.0	2.8	21.80
OPF00LH	2.0	2.8	20.10
Label: OPF00LH A,Y;			

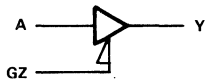


5107

TTL-/CMOS-COMPATIBLE 3-STATE OUTPUT BUFFERS

logic symbol

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 15 pF	C_L = 50 pF	
OPE03LH	2.7	3.7	19.90
OPF03LH	2.7	3.7	23.20
Label: OPF03LH A,GZ,Y;			



5108

TTL-/CMOS-COMPATIBLE OPEN-DRAIN OUTPUT BUFFERS

logic symbol

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 15 pF	C_L = 50 pF	
OPE01LH	1.7	3.0	5.60
OPF01LH	1.7	3.0	5.80
Label: OPF01LH A,Y;			

5109

TTL-/CMOS-COMPATIBLE OPEN-DRAIN OUTPUT BUFFERS

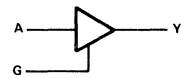
logic symbol

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 15 pF	C_L = 50 pF	
OPE41LH	2.7	6.0	2.40
OPF41LH	2.7	6.0	2.60
Label: OPF41LH A,Y;			

5110

TTL-/CMOS-COMPATIBLE NONINVERTING 3-STATE OUTPUT BUFFERS

logic symbol

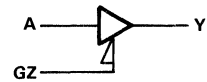


CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 15 pF	C_L = 50 pF	
OPE42LH	3.4	6.2	8.6
OPF42LH	3.4	6.2	10.5
Label: OPF42LH A,G,Y;			

5111

TTL-/CMOS-COMPATIBLE 3-STATE OUTPUT BUFFERS

logic symbol



CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 15 pF	C_L = 50 pF	
OPE43LH	3.5	5.7	10.30
OPF43LH	3.5	5.7	10.90
Label: OPF43LH A,GZ,Y;			

5120

TTL-/CMOS-COMPATIBLE OUTPUT BUFFERS

logic symbol

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 15 pF	C_L = 50 pF	
OPFB0LH	1.7	2.2	32.80
Label: OPFB0LH A,Y;			

5121

TTL-/CMOS-COMPATIBLE OPEN-DRAIN OUTPUT BUFFERS

logic symbol

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 15 pF	C_L = 50 pF	
OPFD1LH	1.7	2.2	10.40
Label: OPFD1LH A,Y;			

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5123

TTL-/CMOS-COMPATIBLE OPEN-DRAIN OUTPUT BUFFERS

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 15 pF	C_L = 50 pF	
OPFE1LH	1.5	1.9	16.20
Label: OPFE1LH A,Y;			

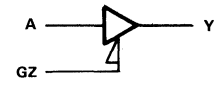
logic symbol

5124

TTL-/CMOS-COMPATIBLE 3-STATE OUTPUT BUFFERS

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 15 pF	C_L = 50 pF	
OPFD3LH	2.5	3.0	49.00
Label: OPFD3LH A,GZ,Y;			

logic symbol

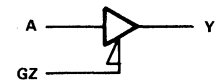


5125

TTL-/CMOS-COMPATIBLE 3-STATE OUTPUT BUFFERS

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 15 pF	C_L = 50 pF	
OPFB3LH	2.8	3.7	29.00
Label: OPFB3LH A,GZ,Y;			

logic symbol

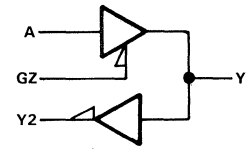


5200

3-STATE I/O BUFFER WITH INVERTING CMOS INPUT AND CMOS/TTL OUTPUT

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 15 pF	C_L = 50 pF	
IOE40LH	3.3	5.9	12.50
IOF40LH	3.3	5.9	12.70
Label: IOF40LH A,GZ,Y2,Y1;			

logic symbol

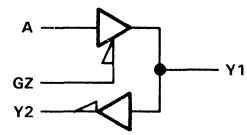


5201

3-STATE I/O BUFFER WITH INVERTING TTL INPUT AND CMOS/TTL OUTPUT

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 15 pF	C_L = 50 pF	
IOE43LH	3.5	5.8	13.20
IOF43LH	3.5	5.8	13.40
Label: IOF43LH A,GZ,Y2,Y1;			

logic symbol

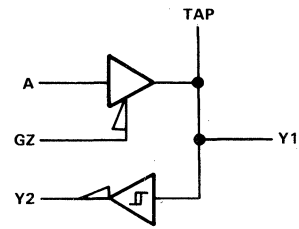


5202

3-STATE I/O BUFFERS WITH INVERTING CMOS INPUT AND CMOS/TTL OUTPUT

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 15 pF	C_L = 50 pF	
IOF47LH	3.6	6.8	13.10
Label: IOF47LH A,GZ,TAP,Y2,Y1;			

logic symbol

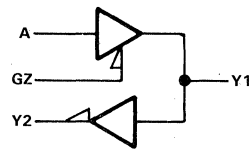


5203

3-STATE I/O BUFFERS WITH INVERTING TTL INPUT AND CMOS/TTL OUTPUT

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 15 pF	C_L = 50 pF	
IOF48LH	3.3	3.5	14.90
Label: IOF48LH A,GZ,Y2,Y1;			

logic symbol

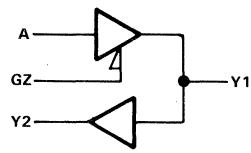


5206

3-STATE I/O BUFFER WITH NONINVERTING CMOS INPUT AND CMOS/TTL OUTPUT

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 15 pF	C_L = 50 pF	
IOE41LH	3.3	5.5	16.70
IOF41LH	3.3	5.5	14.30
Label: IOF41LH A,GZ,Y2,Y1;			

logic symbol



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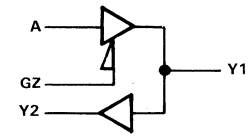
5207

3-STATE I/O BUFFER WITH NONINVERTING TTL INPUT AND CMOS/TTL OUTPUT

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 15 pF	C_L = 50 pF	
IOE44LH	3.5	5.8	14.50
IOF44LH	3.5	5.8	14.30
Label: IOF44LH A,GZ,Y2,Y1;			

logic symbol

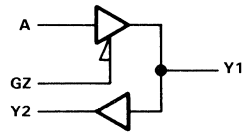


5217

3-STATE I/O BUFFER WITH NONINVERTING TTL INPUT AND CMOS/TTL OUTPUT

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 15 pF	C_L = 50 pF	
IOF64LH	2.7	4.1	22.40
Label: IOF64LH A,GZ,Y2,Y1;			

logic symbol

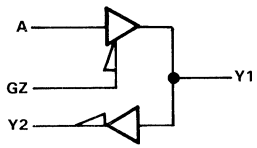


5220

3-STATE I/O BUFFER WITH INVERTING CMOS INPUT AND CMOS/TTL OUTPUT

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 15 pF	C_L = 50 pF	
IOE00LH	2.9	3.8	31.40
IOF00LH	2.9	3.8	25.80
Label: IOF00LH A,GZ,Y2,Y1;			

logic symbol

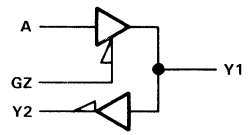


5221

3-STATE I/O BUFFER WITH INVERTING TTL INPUT AND CMOS/TTL OUTPUT

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 15 pF	C_L = 50 pF	
IOF03LH	2.7	3.8	24.40
Label: IOF03LH A,GZ,Y2,Y1;			

logic symbol

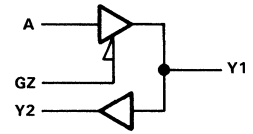


5226

3-STATE I/O BUFFER WITH NONINVERTING CMOS INPUT AND CMOS/TTL OUTPUT

logic symbol

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 15 pF	C_L = 50 pF	
IOF01LH	2.7	3.8	26.60
Label: IOF01LH A,GZ,Y2,Y1;			

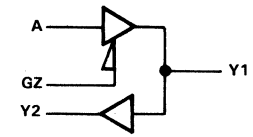


5227

3-STATE I/O BUFFER WITH NONINVERTING TTL INPUT AND CMOS/TTL OUTPUT

logic symbol

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 15 pF	C_L = 50 pF	
IOF04LH	2.7	3.8	25.70
Label: IOF04LH A,GZ,Y2,Y1;			

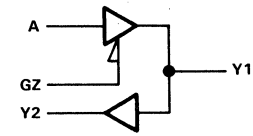


5239

3-STATE I/O BUFFER WITH NONINVERTING TTL INPUT AND CMOS/TTL OUTPUT

logic symbol

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 15 pF	C_L = 50 pF	
IOFB8LH	2.7	3.7	28.20
Label: IOFB8LH A,GZ,Y2,Y1;			

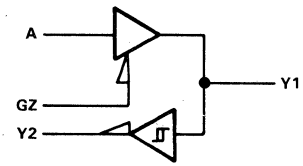


5246

3-STATE I/O BUFFER WITH INVERTING TTL INPUT AND TTL/CMOS OUTPUT

logic symbol

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 15 pF	C_L = 50 pF	
IOFD8LH	2.5	3.0	50.80
Label: IOFD8LH A,GZ,Y2,Y1;			



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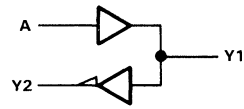
5250

OPEN-DRAIN I/O BUFFER WITH INVERTING CMOS INPUT AND CMOS/TTL OUTPUT

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 15 pF	C_L = 50 pF	
IOFD0LH	1.7	2.3	11.60
Label: IOFD0LH A,Y2,Y1;			

logic symbol

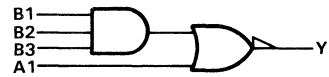


6002

AND-NOR GATES, $Y = \overline{A1 + (B1 \bullet B2 \bullet B3)}$

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
BF002LH	1.1	2.7	0.42
Label: BF002LH A1,B1,B2,B3,Y;			

logic symbol

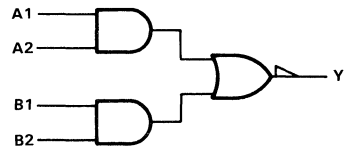


6003

AND-NOR GATES, $Y = \overline{(A1 \bullet A2) + (B1 \bullet B2)}$

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
BF003LH	1.1	2.6	0.51
Label: BF003LH A1,A2,B1,B2,Y;			

logic symbol

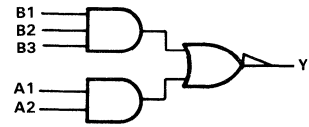


6004

AND-NOR GATES, $Y = \overline{(A1 \bullet A2) + (B1 \bullet B2 \bullet B3)}$

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
BF004LH	1.2	2.8	0.53
Label: BF004LH A1,A2,B1,B2,B3,Y;			

logic symbol

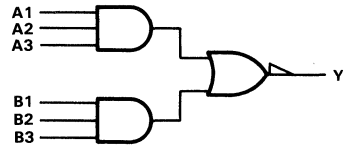


6005

AND-NOR GATES,
$Y = \overline{(A1 \bullet A2 \bullet A3) + (B1 \bullet B2 \bullet B3)}$

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
BF005LH	1.4	3.0	0.64
Label: BF005LH A1,A2,A3,B1,B2,B3,Y;			

logic symbol

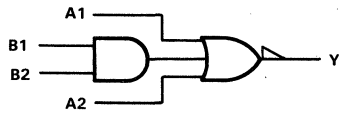


6006

AND-NOR GATES, $Y = \overline{A1 + A2 + (B1 \bullet B2)}$

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
BF006LH	1.3	3.2	0.36
Label: BF006LH A1,A2,B1,B2,Y;			

logic symbol

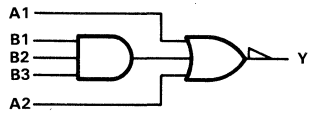


6007

AND-NOR GATES, $Y = \overline{A1 + A2 + (B1 \bullet B2 \bullet B3)}$

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
BF007LH	1.5	3.7	0.36
Label: BF007LH A1,A2,B1,B2,B3,Y;			

logic symbol

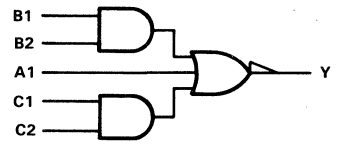


6008

AND-NOR GATES, $Y = \overline{A1 + (B1 \bullet B2) + (C1 \bullet C2)}$

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
BF008LH	1.4	3.4	0.44
Label: BF008LH A1,B1,B2,C1,C2,Y;			

logic symbol



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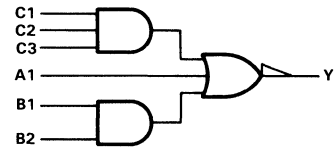
6009

AND-NOR GATES, $Y = \overline{A1+(B1 \bullet B2)+(C1 \bullet C2 \bullet C3)}$

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
BF009LH	1.6	3.7	0.45
Label: BF009LH A1,B1,B2,C1,C2,C3,Y;			

logic symbol

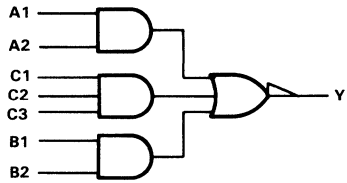


6012

AND-NOR GATES,
$Y = \overline{(A1 \bullet A2)+(B1 \bullet B2)+(C1 \bullet C2 \bullet C3)}$

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
BF012LH	1.7	3.7	0.56
Label: BF012LH A1,A2,B1,B2,C1,C2,C3,Y;			

logic symbol

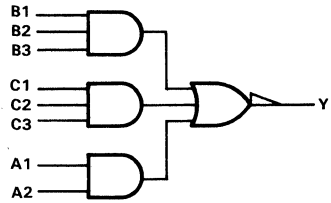


6013

AND-NOR GATES,
$Y = \overline{(A1 \bullet A2)+(B1 \bullet B2 \bullet B3)+(C1 \bullet C2 \bullet C3)}$

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
BF013LH	1.9	4.1	0.57
Label: BF013LH A1,A2,B1,B2,B3,C1,C2,C3,Y;			

logic symbol

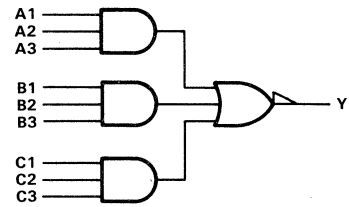


6014

AND-NOR GATES,
$Y = \overline{(A1 \bullet A2 \bullet A3) + (B1 \bullet B2 \bullet B3) + (C1 \bullet C2 \bullet C3)}$

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
BF014LH	2.1	4.3	0.71
Label: BF014LH A1,A2,A3,B1,B2,B3,C1,C2,C3,Y;			

logic symbol

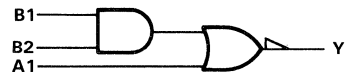


6017

AND-NOR GATES, $Y = \overline{A1 + (B1 \bullet B2)}$

logic symbol

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
BF001LH	1.0	2.5	0.38
Label: BF001LH A1,B1,B2,Y;			

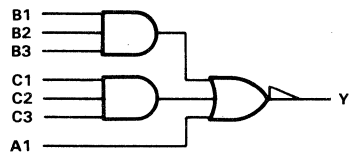


6018

AND-NOR GATES,
$Y = \overline{A1 + (B1 \bullet B2 \bullet B3) + (C1 \bullet C2 \bullet C3)}$

logic symbol

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
BF010LH	1.7	3.9	0.45
Label: BF010LH A1,B1,B2,B3,C1,C2,C3,Y;			

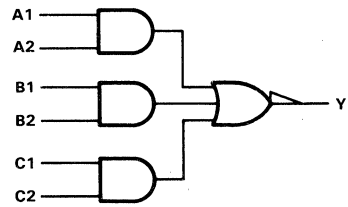


6019

AND-NOR GATES,
$Y = \overline{(A1 \bullet A2) + (B1 \bullet B2) + (C1 \bullet C2)}$

logic symbol

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
BF011LH	1.5	3.5	0.52
Label: BF011LH A1,A2,B1,B2,C1,C2,Y;			

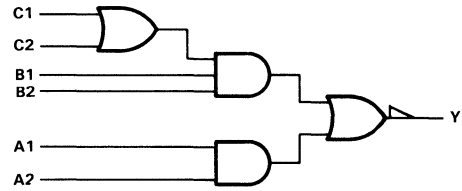


6022

OR-AND-NOR GATES,
$Y = \overline{A1 \bullet A2 + [B1 \bullet B2 \bullet (C1 + C2)]}$

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
BF022LH	1.7	3.9	0.54
Label: BF022LH A1,A2,B1,B2,C1,C2,Y;			

logic symbol

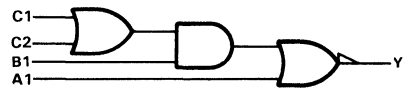


6023

OR-AND-NOR GATES, $Y = \overline{A1 + [B1 \bullet (C1 + C2)]}$

logic symbol

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
BF015LH	1.3	3.2	0.36
Label: BF015LH A1,B1,C1,C2,Y;			

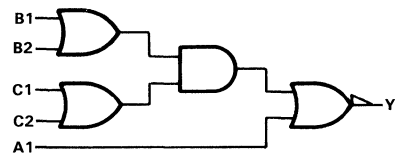


6024

OR-AND-NOR GATES,
$Y = \overline{A1 + [(B1 + B2) \bullet (C1 + C2)]}$

logic symbol

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
BF016LH	1.4	3.4	0.42
Label: BF016LH A1,B1,B2,C1,C2,Y;			

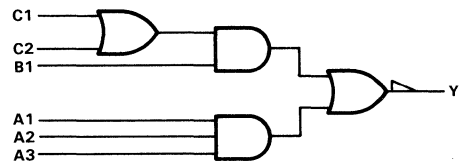


6025

OR-AND-NOR GATES,
$Y = \overline{A1 \bullet A2 \bullet A3 + [B1 \bullet (C1 + C2)]}$

logic symbol

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
BF025LH	1.5	3.5	0.64
Label: BF025LH A1,A2,A3,B1,C1,C2,Y;			

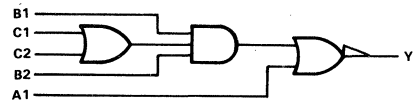


6026

OR-AND-NOR GATES,
$Y = \overline{A1 + [B1 \bullet B2 \bullet (C1 + C2)]}$

logic symbol

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
BF017LH	1.5	3.7	0.40
Label: BF017LH A1,B1,B2,C1,C2,Y;			

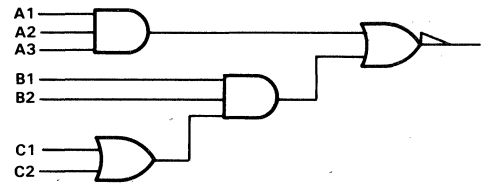


6027

OR-AND-NOR GATES,
$Y = \overline{A1 \bullet A2 \bullet A3 + [B1 \bullet B2 \bullet (C1 + C2)]}$

logic symbol

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
BF027LH	1.8	3.6	0.98
Label: BF027LH A1,A2,A3,B1,B2,C1,C2,Y;			

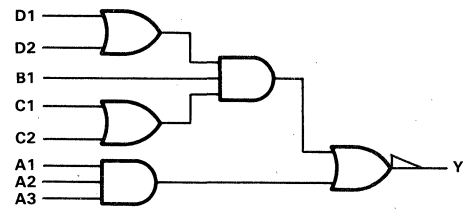


6028

OR-AND-NOR GATES,
$Y = \overline{A1 \bullet A2 \bullet A3 + [B1 \bullet (C1 + C2) \bullet (D1 + D2)]}$

logic symbol

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
BF028LH	1.9	3.6	1.11
Label: BF028LH A1,A2,A3,B1,C1,C2,D1,D2,Y;			

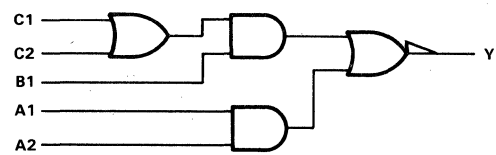


6029

OR-AND-NOR GATES,
$Y = \overline{A1 \bullet A2 + [B1 \bullet (C1 + C2)]}$

logic symbol

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
BF020LH	1.4	3.4	0.47
Label: BF020LH A1,A2,B1,C1,C2,Y;			

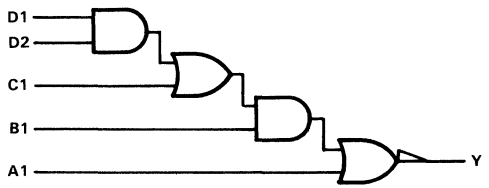


6032

AND-OR-AND-NOR GATES,
$Y = \overline{A1 + \{B1 \bullet [C1 + (D1 \bullet D2)]\}}$

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
BF030LH	1.7	3.9	0.80
Label: BF030LH A1,B1,C1,D1,D2,Y;			

logic symbol

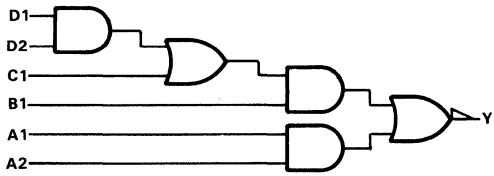


6034

AND-OR-AND-NOR GATES,
$Y = \overline{(A1 \bullet A2) + \{B1 \bullet [C1 + (D1 \bullet D2)]\}}$

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
BF034LH	1.7	3.6	0.86
Label: BF034LH A1,A2,B1,C1,D1,D2,Y;			

logic symbol

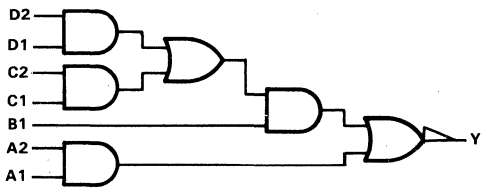


6035

AND-OR-AND-NOR GATES,
$Y = \overline{(A1 \bullet A2) + \{B1 \bullet [(C1 \bullet C2) + (D1 \bullet D2)]\}}$

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
BF035LH	1.7	3.3	0.96
Label: BF035LH A1,A2,B1,C1,C2,D1,D2,Y;			

logic symbol

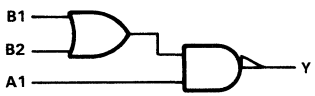


6048

OR-NAND GATES, $Y = \overline{A1 \bullet (B1 + B2)}$

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
BF051LH	1.0	2.4	0.57
Label: BF051LH A1,B1,B2,Y;			

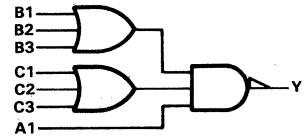
logic symbol



6049

OR-NAND GATES,
$Y = \overline{A1 \bullet (B1 + B2 + B3) \bullet (C1 + C2 + C3)}$

logic symbol

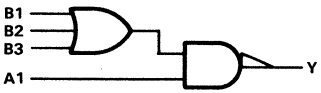


CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
BF060LH	1.7	3.8	0.65
Label: BF060LH A1,B1,B2,B3,C1,C2,C3,Y;			

6052

OR-NAND GATES, $Y = \overline{A1 \bullet (B1 + B2 + B3)}$

logic symbol

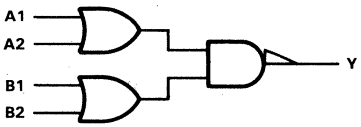


CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
BF052LH	1.2	3.2	0.57
Label: BF052LH A1,B1,B2,B3,Y;			

6053

OR-NAND GATES, $Y = \overline{(A1 + A2) \bullet (B1 + B2)}$

logic symbol

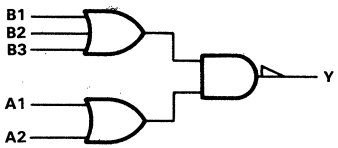


CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
BF053LH	1.1	2.6	0.49
Label: BF053LH A1,A2,B1,B2,Y;			

6054

OR-NAND GATES, $Y = \overline{(A1 + A2) \bullet (B1 + B2 + B3)}$

logic symbol



CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
BF054LH	1.2	3.0	0.47
Label: BF054LH A1,A2,B1,B2,B3,Y;			

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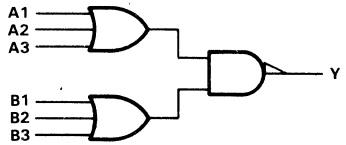
6055

OR-NAND GATES,
$Y = \overline{(A1 + A2 + A3) \bullet (B1 + B2 + B3)}$

logic symbol

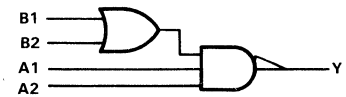


CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
BF055LH	1.3	3.3	0.51
Label: BF055LH A1,A2,A3,B1,B2,B3,Y;			

6056

OR-NAND GATES, Y = $\overline{A1 \bullet A2 \bullet (B1 + B2)}$

logic symbol

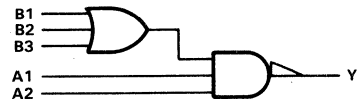


CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
BF056LH	1.2	2.9	0.55
Label: BF056LH A1,A2,B1,B2,Y;			

6057

OR-NAND GATES, Y = $\overline{A1 \bullet A2 \bullet (B1 + B2 + B3)}$

logic symbol

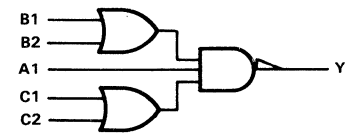


CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
BF057LH	1.5	3.7	0.58
Label: BF057LH A1,A2,B1,B2,B3,Y;			

6058

OR-NAND GATES, Y = $\overline{A1 \bullet (B1 + B2) \bullet (C1 + C2)}$

logic symbol



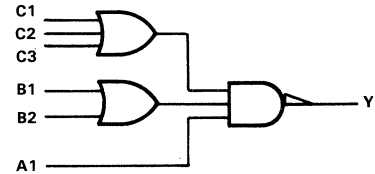
CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
BF058LH	1.3	3.0	0.64
Label: BF058LH A1,B1,B2,C1,C2,Y;			

6059

OR-NAND GATES, $Y = \overline{A1 \bullet (B1 + B2) \bullet (C1 + C2 + C3)}$

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
BF059LH	1.6	3.5	0.65
Label: BF059LH A1,B1,B2,C1,C2,C3,Y;			

logic symbol

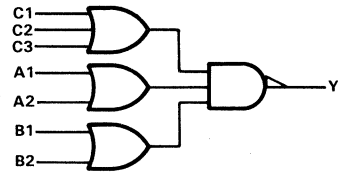


6062

OR-NAND GATES,
$Y = \overline{(A1 + A2) \bullet (B1 + B2) \bullet (C1 + C2 + C3)}$

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
BF062LH	1.9	4.1	0.65
Label: BF062LH A1,A2,B1,B2,C1,C2,C3,Y;			

logic symbol

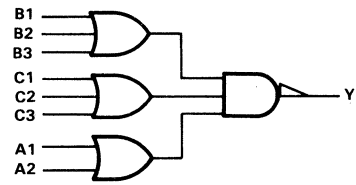


6063

OR-NAND GATES,
$Y = \overline{(A1 + A2) \bullet (B1 + B2 + B3) \bullet (C1 + C2 + C3)}$

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
BF063LH	2.0	4.2	0.64
Label: BF063LH A1,A2,B1,B2,B3,C1,C2,C3,Y;			

logic symbol

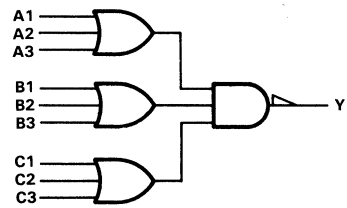


6064

OR-NAND GATES,
$Y = \overline{(A1 + A2 + A3) \bullet (B1 + B2 + B3) \bullet (C1 + C2 + C3)}$

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
BF064LH	1.9	4.1	0.70
Label: BF064LH A1,A2,A3,B1,B2,B3,C1,C2,C3,Y;			

logic symbol



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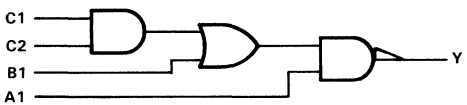
6065

AND-OR-NAND GATES, $Y = \overline{A1 \bullet [B1 + (C1 \bullet C2)]}$

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
BF065LH	1.2	2.8	0.58
Label: BF065LH A1,B1,C1,C2,Y;			

logic symbol

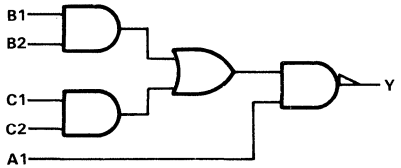


6066

AND-OR-NAND GATES,
$Y = \overline{A1 \bullet [(B1 \bullet B2) + (C1 \bullet C2)]}$

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
BF066LH	1.3	2.9	0.64
Label: BF066LH A1,B1,B2,C1,C2,Y;			

logic symbol

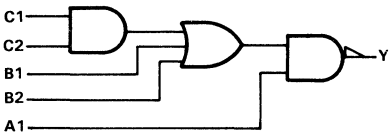


6067

AND-OR-NAND GATES,
$Y = \overline{A1 \bullet [B1 + B2 + (C1 \bullet C2)]}$

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
BF067LH	1.5	3.7	0.57
Label: BF067LH A1,B1,B2,C1,C2,Y;			

logic symbol

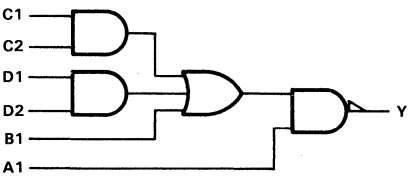


6068

AND-OR-NAND GATES,
$Y = \overline{A1 \bullet [B1 + (C1 \bullet C2) + (D1 \bullet D2)]}$

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
BF068LH	1.8	4.0	0.61
Label: BF068LH A1,B1,C1,C2,D1,D2,Y;			

logic symbol

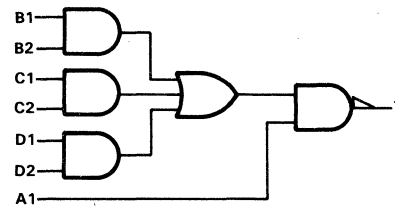


6069

AND-OR-NAND GATES,
$Y = \overline{A1 \bullet [(B1 \bullet B2) + (C1 \bullet C2) + (D1 \bullet D2)]}$

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
BF069LH	1.9	4.2	0.66
Label: BF069LH A1,B1,B2,C1,C2,D1,D2,Y;			

logic symbol

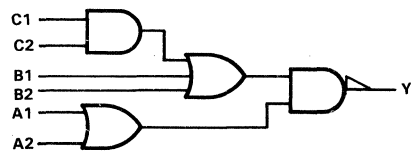


6072

AND-OR-NAND GATES,
$Y = \overline{(A1 + A2) \bullet [B1 + B2 + (C1 \bullet C2)]}$

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
BF072LH	1.8	3.8	0.81
Label: BF072LH A1,A2,B1,B2,C1,C2,Y;			

logic symbol

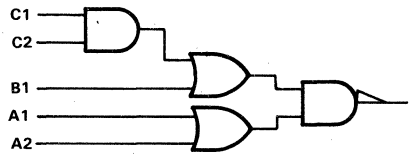


6073

AND-OR-NAND GATES,
$Y = \overline{(A1 + A2) \bullet [B1 + (C1 \bullet C2)]}$

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
BF070LH	1.3	2.9	0.53
Label: BF070LH A1,A2,B1,C1,C2,Y;			

logic symbol

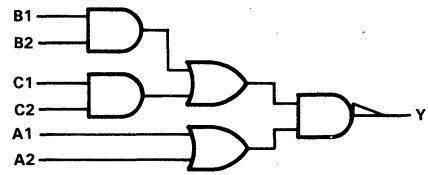


6074

AND-OR-NAND GATES,
$Y = \overline{(A1 + A2) \bullet [(B1 \bullet B2) + (C1 \bullet C2)]}$

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
BF071LH	1.5	3.1	0.64
Label: BF071LH A1,A2,B1,B2,C1,C2,Y;			

logic symbol



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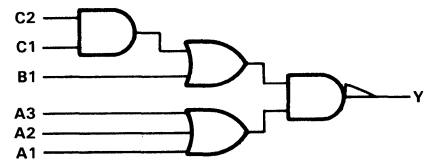
6075

AND-OR-NAND GATES,
$Y = \overline{(A1+A2+A3)\bullet[B1+(C1\bullet C2)]}$

logic symbol

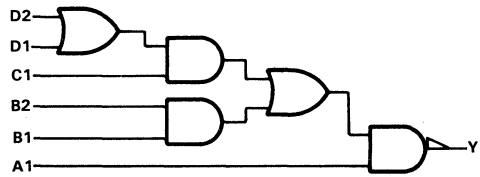


CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
BF075LH	1.1	2.5	0.77
Label: BF075LH A1,A2,A3,B1,C1,C2,Y;			

6082

OR-AND-OR-NAND GATES,
$Y = \overline{A1\bullet\{(B1\bullet B2)+[C1\bullet(D1+D2)]\}}$

logic symbol

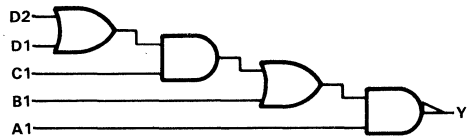


CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
BF082LH	1.9	3.8	0.87
Label: BF082LH A1,B1,B2,C1,D1,D2,Y;			

6083

OR-AND-OR-NAND GATES,
$Y = \overline{A1\bullet\{B1+[C1\bullet(D1+D2)]\}}$

logic symbol

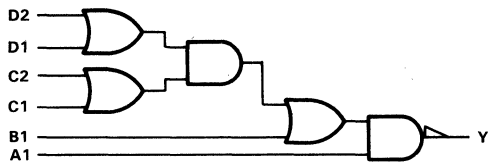


CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
BF080LH	1.6	3.7	0.80
Label: BF080LH A1,B1,C1,D1,D2,Y;			

6084

OR-AND-OR-NAND GATES,
$Y = \overline{A1\bullet\{B1+[(C1+C2)\bullet(D1+D2)]\}}$

logic symbol



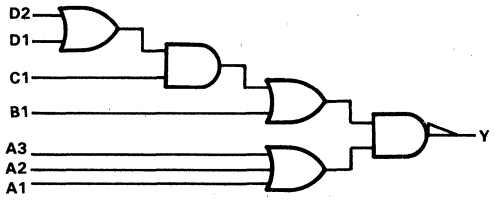
CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
BF081LH	1.9	3.9	0.90
Label: BF081LH A1,B1,C1,C2,D1,D2,Y;			

6088

OR-AND-OR-NAND GATES,
$Y = \overline{(A1+A2+A3)\bullet\{B1+[C1\bullet(D1+D2)]\}}$

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
BF088LH	2.1	4.1	0.99
Label: BF088LH A1,A2,A3,B1,C1,D1,D2,Y;			

logic symbol

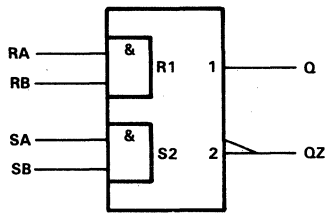


6100

4-INPUT GATED S-R LATCHES

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
GM010LH	1.3	2.8	0.75
Label: GM010LH RA,RB,SA,SB,Q,QZ;			

logic symbol

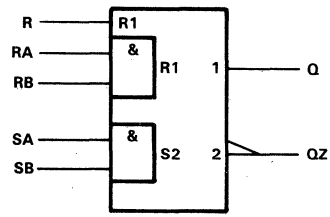


6101

5-INPUT GATED S-R LATCHES INCLUDING SEPARATE RESET

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
GM110LH	1.3	3.6	0.80
Label: GM110LH RA,RB,SA,SB,R,Q,QZ;			

logic symbol



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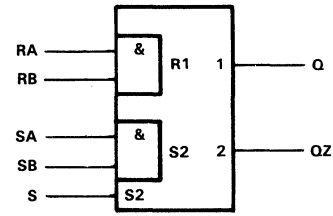
6102

5-INPUT GATED S-R LATCHES INCLUDING SEPARATE SET

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
GMS10LH	1.6	3.6	0.75
Label: GMS10LH RA,RB,SA,SB,S,Q,QZ;			

logic symbol

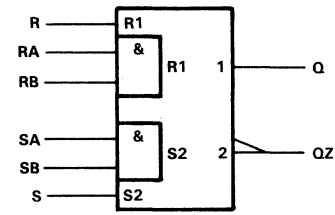


6103

6-INPUT GATED S-R LATCHES INCLUDING SEPARATE SET AND RESET

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
GM210LH	1.6	3.6	0.81
Label: GM210LH RA,RB,SA,SB,R,S,Q,QZ;			

logic symbol

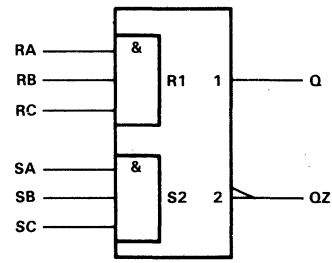


6105

6-INPUT GATED S-R LATCHES

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
GM310LH	1.4	3.0	0.80
Label: GM310LH RA,RB,RC,SA,SB,SC,Q,QZ;			

logic symbol

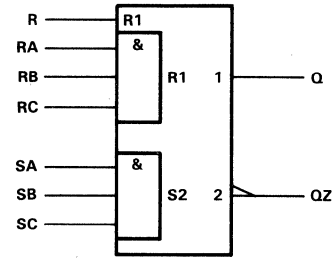


6106

7-INPUT GATED S-R LATCHES INCLUDING SEPARATE RESET

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
GM410LH	1.8	4.0	0.85
Label: GM410LH RA,RB,RC,SA,SB,SC,R,Q,QZ;			

logic symbol

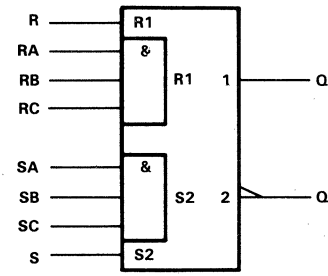


6108

8-INPUT GATED S-R LATCHES INCLUDING SEPARATE SET AND RESET

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
GM510LH	1.8	4.0	0.86
Label: GM510LH RA,RB,RC,SA,SB,SC,R,S,Q,QZ;			

logic symbol

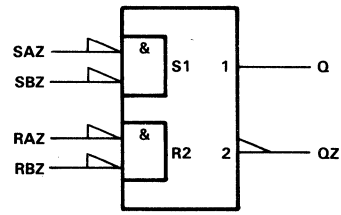


6110

4-INPUT GATED $\overline{S}$-$\overline{R}$ LATCHES

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
GS010LH	1.3	2.7	0.72
Label: GS010LH RAZ,RBZ,SAZ,SBZ,Q,QZ;			

logic symbol

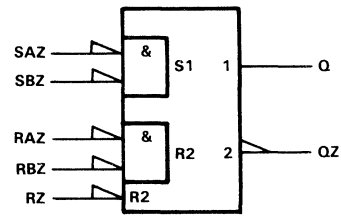


6111

5-INPUT GATED $\overline{S}$-$\overline{R}$ LATCHES INCLUDING SEPARATE RESET

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
GS110LH	1.5	3.1	0.84
Label: GS110LH RAZ,RBZ,SAZ,SBZ,RZ,Q,QZ;			

logic symbol

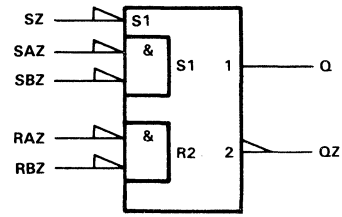


6112

5-INPUT GATED $\overline{S}$-$\overline{R}$ LATCHES INCLUDING SEPARATE SET

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
GSS10LH	1.4	3.1	0.84
Label: GSS10LH RAZ,RBZ,SAZ,SBZ,SZ,Q,QZ;			

logic symbol

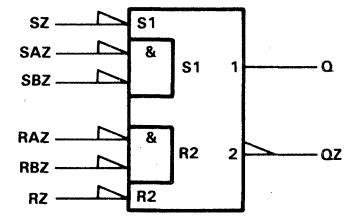


6113

6-INPUT GATED $\overline{S}$-$\overline{R}$ LATCHES INCLUDING SEPARATE SET AND RESET

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
GS210LH	1.5	3.1	0.84
Label: GS210LH RAZ,RBZ,SAZ,SBZ,RZ,SZ,Q,QZ;			

logic symbol

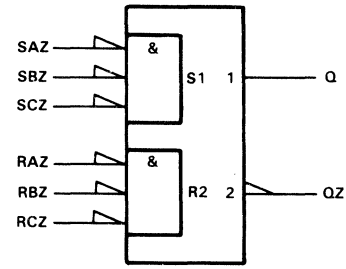


6115

6-INPUT GATED $\overline{S}$-$\overline{R}$ LATCHES

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
GS310LH	1.5	3.4	0.75
Label: GS310LH RAZ,RBZ,RCZ,SAZ,SBZ,SCZ,Q,QZ;			

logic symbol

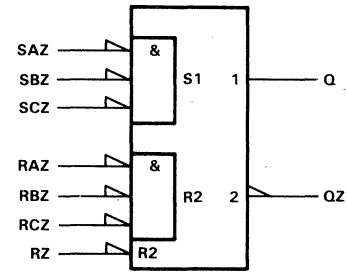


6116

7-INPUT GATED $\overline{S}$-$\overline{R}$ LATCHES INCLUDING SEPARATE RESET

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
GS410LH	1.7	3.8	0.85
Label: GS410LH RAZ,RBZ,RCZ,SAZ,SBZ,SCZ,RZ,Q,QZ;			

logic symbol

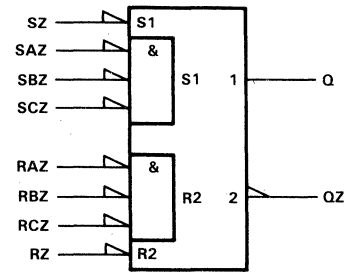


6118

8-INPUT GATED $\overline{S}$-$\overline{R}$ LATCHES INCLUDING SEPARATE SET AND RESET

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
GS510LH	1.9	4.0	0.89
Label: GS510LH RAZ,RBZ,RCZ,SAZ,SBZ,SCZ,RZ,SZ,Q,QZ;			

logic symbol



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6120

NONINVERTING DELAY BUFFERS

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
BU120LH	1.1	1.7	1.29
BU130LH	1.4	1.7	1.73
Label: BU1n0LH A,Y;			

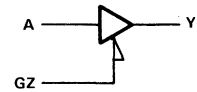
logic symbol

6121

NONINVERTING 3-STATE BUFFERS WITH ACTIVE-LOW ENABLE

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
BU221LH	1.6	2.3	1.62
BU261LH	1.8	2.0	3.29
Label: BU2n1LH A,GZ,Y;			

logic symbol

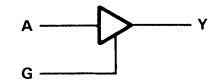


6122

NONINVERTING 3-STATE BUFFERS WITH ACTIVE-HIGH ENABLE

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
BU222LH	1.6	2.3	1.62
BU262LH	1.8	2.0	3.30
Label: BU2n2LH A,G,Y;			

logic symbol

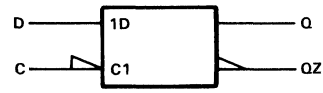


6125

D-TYPE LATCHES WITH ACTIVE-LOW ENABLE

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
LAL20LH	3.2	3.9	4.68
Label: LALn0LH D,C,Q,QZ;			

logic symbol

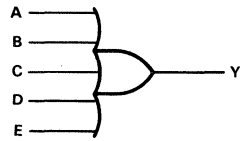


6130

5-INPUT POSITIVE-OR GATES

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
OR510LH	2.5	3.4	1.11
Label: OR510LH A,B,C,D,E,Y;			

logic symbol

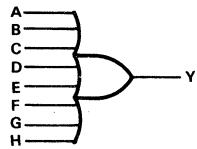


6131

8-INPUT POSITIVE-OR GATES

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
OR810LH	2.3	3.3	1.16
Label: OR810LH A,B,C,D,E,F,G,H,Y;			

logic symbol

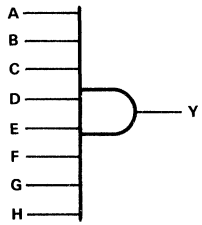


6132

8-INPUT POSITIVE-AND GATES

CELL NAME	t_{pd} (ns)		C_{pd} (pF)
	C_L = 0 pF	C_L = 1 pF	
AN810LH	2.1	3.4	1.22
Label: AN810LH A,B,C,D,E,F,G,H,Y;			

logic symbol



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SystemCell™ 2-μm INTERNAL STANDARD CELL

- Choice of Five Performance Levels
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

positive logic equation

$Y = \overline{A\,B} = \overline{A} + \overline{B}$

description

The SN54ASC00 and SN74ASC00 are 2-input positive-NAND gate CMOS standard-cell functions implementing the equivalent of one-fourth of an SN54LS00 or SN74LS00. The standard-cell library contains five physical implementations providing the custom IC designer a choice between five performance levels for optimizing design. The five options are designated and called from the engineering workstation input using the following cell names to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		TYPICAL DELAY C_L = 1 pF	RELATIVE CELL AREA TO NA210LH
NA210LH	Label: NA2n0LH A,B,Y;	2 ns	1
NA220LH		1.3 ns	1.5
NA230LH		1.1 ns	2
NA240LH		1 ns	2.5
NA260LH		0.8 ns	3.5

The SN54ASC00 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC00 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS		NA210LH TYP	NA210LH MAX	NA220LH TYP	NA220LH MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current	SN54ASC00	V_{CC} = 4.5 V to 5.5 V,	V_I = V_{CC} or 0,		131		196	nA
		SN74ASC00	T_A = MIN to MAX			7.84		11.7	
C_i	Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.12		0.2		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	0.51		1		pF

PARAMETER			TEST CONDITIONS		NA230LH TYP	NA230LH MAX	NA240LH TYP	NA240LH MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current	SN54ASC00	V_{CC} = 4.5 V to 5.5 V,	V_I = V_{CC} or 0,		254		316	nA
		SN74ASC00	T_A = MIN to MAX			15.2		19	
C_i	Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.39		0.54		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	1.51		2.06		pF

PARAMETER			TEST CONDITIONS		NA260LH TYP	NA260LH MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		V
I_{CC}	Supply current	SN54ASC00	V_{CC} = 4.5 V to 5.5 V,	V_I = V_{CC} or 0,		433	nA
		SN74ASC00	T_A = MIN to MAX			26	
C_i	Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.79		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	2.98		pF

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

NA210LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC00			SN74ASC00			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A or B	Y	C_L = 0	0.7	0.8	1.4	0.7	0.8	1.3	ns
t_{PHL}				0.5	1	1.5	0.5	1	1.4	
t_{PLH}	A or B	Y	C_L = 1 pF	1.2	2	4	1.2	2	3.7	ns
t_{PHL}				1	2	4.2	1.1	2	3.7	
Δt_{PLH}	A or B	Y		0.5	1.2	2.7	0.5	1.2	2.5	ns/pF
Δt_{PHL}				0.5	1	2.7	0.5	1	2.3	

NA220LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC00			SN74ASC00			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A or B	Y	C_L = 0	0.5	0.8	1.3	0.6	0.8	1.2	ns
t_{PHL}				0.3	0.7	1.4	0.4	0.7	1.3	
t_{PLH}	A or B	Y	C_L = 1 pF	0.8	1.3	2.4	0.9	1.3	2.2	ns
t_{PHL}				0.6	1.3	2.7	0.7	1.3	2.4	
Δt_{PLH}	A or B	Y		0.3	0.5	1.1	0.3	0.5	1	ns/pF
Δt_{PHL}				0.3	0.6	1.3	0.3	0.6	1.1	

NA230LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC00			SN74ASC00			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A or B	Y	C_L = 0	0.4	0.7	1.3	0.5	0.7	1.3	ns
t_{PHL}				0.2	0.6	1.4	0.3	0.6	1.3	
t_{PLH}	A or B	Y	C_L = 1 pF	0.7	1.1	2	0.7	1.1	1.9	ns
t_{PHL}				0.5	1	2.3	0.5	1	2	
Δt_{PLH}	A or B	Y		0.2	0.4	0.8	0.2	0.4	0.7	ns/pF
Δt_{PHL}				0.3	0.4	0.9	0.2	0.4	0.8	

NA240LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC00			SN74ASC00			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A or B	Y	C_L = 0	0.4	0.7	1.2	0.4	0.7	1.1	ns
t_{PHL}				0.1	0.5	1.2	0.2	0.5	1.1	
t_{PLH}	A or B	Y	C_L = 1 pF	0.6	1	1.8	0.6	1	1.7	ns
t_{PHL}				0.4	0.9	1.9	0.4	0.9	1.7	
Δt_{PLH}	A or B	Y		0.2	0.3	0.6	0.2	0.3	0.6	ns/pF
Δt_{PHL}				0.3	0.4	0.7	0.2	0.4	0.7	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

NA260LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC00			SN74ASC00			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A or B	Y	C_L = 0	0.4	0.6	1.2	0.5	0.6	1.1	ns
t_{PHL}				0.1	0.5	1.2	0.3	0.5	1.1	
t_{PLH}	A or B	Y	C_L = 1 pF	0.5	0.8	1.6	0.6	0.8	1.5	ns
t_{PHL}				0.3	0.7	1.7	0.4	0.7	1.5	
Δt_{PLH}	A or B	Y		0.1	0.2	0.5	0.1	0.2	0.4	ns/pF
Δt_{PHL}				0.1	0.2	0.6	0.1	0.2	0.5	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to Section 7

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

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SystemCell™ 2-μm INTERNAL STANDARD CELL

- **Choice of Four Performance Levels**
- **Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V**
- **Functional Operation Over V_{CC} Range of 2 V to 6 V**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

positive logic equations

$$Y = \overline{A+B} = \overline{A} \cdot \overline{B}$$

description

The SN54ASC02 and SN74ASC02 are 2-input positive-NOR gate CMOS standard-cell functions implementing the equivalent of one-fourth of the SN54LS02 or SN74LS02. The standard-cell library contains four physical implementations providing the custom IC designer a choice between four performance levels for optimizing designs. Each option is designated and called from the engineering workstation input using the following cell names to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		TYPICAL DELAY C_L = 1 pF	RELATIVE CELL AREA TO NA210LH
NO210LH	Label: NO2n0LH A,B,Y;	2.4 ns	1
NO220LH		1.5 ns	1.5
NO230LH		1.3 ns	2
NO240LH		1.1 ns	2.5

The SN54ASC02 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC02 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS		NO210LH TYP	NO210LH MAX	NO220LH TYP	NO220LH MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current	SN54ASC02	V_{CC} = 4.5 V to 5.5 V,	V_I = V_{CC} or 0,		128		185	nA
		SN74ASC02	T_A = MIN to MAX			7.71		11.1	
C_i	Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.11		0.24		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	0.33		0.52		pF

PARAMETER			TEST CONDITIONS		NO230LH TYP	NO230LH MAX	NO240LH TYP	NO240LH MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current	SN54ASC02	V_{CC} = 4.5 V to 5.5 V,	V_I = V_{CC} or 0,		237		292	nA
		SN74ASC02	T_A = MIN to MAX			14.2		17.5	
C_i	Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.36		0.47		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	0.8		0.98		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

NO210LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC02 MIN	SN54ASC02 TYP‡	SN54ASC02 MAX	SN74ASC02 MIN	SN74ASC02 TYP‡	SN74ASC02 MAX	UNIT
t_{PLH}	A or B	Y	C_L = 0	0.6	0.8	1.6	0.6	0.8	1.5	ns
t_{PHL}				0.5	1	1.7	0.6	1	1.7	
t_{PLH}	A or B	Y	C_L = 1 pF	1.5	2.8	6.2	1.6	2.8	5.6	ns
t_{PHL}				1.1	2	4.6	1.1	2	4.1	
Δt_{PLH}	A or B	Y		0.9	2	4.6	1	2	4.2	ns/pF
Δt_{PHL}				0.5	1	2.9	0.5	1	2.5	

NO220LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC02 MIN	SN54ASC02 TYP‡	SN54ASC02 MAX	SN74ASC02 MIN	SN74ASC02 TYP‡	SN74ASC02 MAX	UNIT
t_{PLH}	A or B	Y	C_L = 0	0.6	0.8	1.3	0.6	0.8	1.2	ns
t_{PHL}				0.3	0.8	1.5	0.3	0.8	1.5	
t_{PLH}	A or B	Y	C_L = 1 pF	1	1.7	3.5	1.1	1.7	3.2	ns
t_{PHL}				0.7	1.3	2.6	0.7	1.3	2.4	
Δt_{PLH}	A or B	Y		0.4	0.9	2.3	0.5	0.9	2	ns/pF
Δt_{PHL}				0.3	0.6	1.1	0.4	0.6	1	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

NO230LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC02			SN74ASC02			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A or B	Y	C_L = 0	0.5	0.8	1.4	0.5	0.8	1.2	ns
t_{PHL}				0.3	0.7	1.6	0.3	0.7	1.5	
t_{PLH}	A or B	Y	C_L = 1 pF	0.9	1.4	2.9	0.9	1.4	2.6	ns
t_{PHL}				0.6	1.2	2.4	0.6	1.2	2.2	
Δt_{PLH}	A or B	Y		0.3	0.6	1.5	0.3	0.6	1.4	ns/pF
Δt_{PHL}				0.2	0.5	0.9	0.3	0.5	0.8	

NO240LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC02			SN74ASC02			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A or B	Y	C_L = 0	0.5	0.7	1.3	0.5	0.7	1.2	ns
t_{PHL}				0.2	0.6	1.4	0.2	0.6	1.3	
t_{PLH}	A or B	Y	C_L = 1 pF	0.7	1.2	2.4	0.8	1.2	2.2	ns
t_{PHL}				0.5	1	2.1	0.5	1	1.9	
Δt_{PLH}	A or B	Y		0.2	0.5	1.2	0.3	0.5	1.1	ns/pF
Δt_{PHL}				0.2	0.4	0.7	0.2	0.4	0.6	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to Section 7.

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SystemCell™ 2-μm INTERNAL STANDARD CELL

- **Choice of Seven Performance Levels**
- **Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V**
- **Functional Operation Over V_{CC} Range of 2 V to 6 V**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol

FUNCTION TABLE

INPUT A	OUTPUT Y
H	L
L	H

positive logic equation

$Y = \overline{A}$

description

The SN54ASC04 and SN74ASC04 are CMOS inverter standard cells implementing the equivalent of one-sixth of a SN54LS04 or SN74LS04. The standard-cell library contains seven physical implementations providing the custom IC designer a choice of seven performance levels for optimizing designs. Each of the options are designated and called from the engineering workstation input using the following cell names to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		TYPICAL DELAY C_L = 1 pF	RELATIVE CELL AREA TO NA210LH
IV110LH	Label: IV1n0LH A,Y;	1.7 ns	0.75
IV120LH		1.1 ns	1
IV130LH		0.9 ns	1.25
IV140LH		0.8 ns	1.5
IV160LH		0.7 ns	2
IV180LH		0.6 ns	2.5
IV101LH	Label: IV101LH A,Y;	2.3 ns	4.5

The SN54ASC04 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC04 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS		IV110LH TYP	IV110LH MAX	IV120LH TYP	IV120LH MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current	SN54ASC04	V_{CC} = 4.5 V to 5.5 V,	V_I = V_{CC} or 0,		105		131	nA
		SN74ASC04	T_A = MIN to MAX			6.32		7.85	
C_i	Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.12		0.24		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	0.44		0.8		pF

PARAMETER			TEST CONDITIONS		IV130LH TYP	IV130LH MAX	IV140LH TYP	IV140LH MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current	SN54ASC04	V_{CC} = 4.5 V to 5.5 V,	V_I = V_{CC} or 0,		163		190	nA
		SN74ASC04	T_A = MIN to MAX			9.76		11.4	
C_i	Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.4		0.49		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	1.29		1.61		pF

PARAMETER			TEST CONDITIONS		IV160LH TYP	IV160LH MAX	IV180LH TYP	IV180LH MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current	SN54ASC04	V_{CC} = 4.5 V to 5.5 V,	V_I = V_{CC} or 0,		247		306	nA
		SN74ASC04	T_A = MIN to MAX			14.8		18.4	
C_i	Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.74		1		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	2.39		3.16		pF

PARAMETER			TEST CONDITIONS		IV101LH TYP	IV101LH MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		V
I_{CC}	Supply current	SN54ASC04	V_{CC} = 4.5 V to 5.5 V,	V_I = V_{CC} or 0,		553	nA
		SN74ASC04	T_A = MIN to MAX			33.2	
C_i	Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.13		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	7.22		pF

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

IV110LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC04			SN74ASC04			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	C_L = 0	0.6	0.8	1.1	0.6	0.8	1.1	ns
t_{PHL}				0.4	0.9	1.4	0.5	0.9	1.4	
t_{PLH}	A	Y	C_L = 1 pF	1.1	1.8	3.4	1.2	1.8	3.2	ns
t_{PHL}				0.9	1.6	3.2	1	1.6	2.9	
Δt_{PLH}	A	Y		0.5	1	2.3	0.5	1	2.1	ns/pF
Δt_{PHL}				0.5	0.8	1.8	0.5	0.8	1.6	

IV120LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC04			SN74ASC04			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	C_L = 0	0.4	0.6	1.1	0.4	0.6	1	ns
t_{PHL}				0.2	0.6	1.2	0.2	0.6	1.1	
t_{PLH}	A	Y	C_L = 1 pF	0.8	1.2	2.1	0.8	1.2	2	ns
t_{PHL}				0.5	1	2.1	0.6	1	2	
Δt_{PLH}	A	Y		0.3	0.5	1.1	0.3	0.5	1	ns/pF
Δt_{PHL}				0.3	0.5	0.9	0.3	0.5	0.9	

IV130LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC04			SN74ASC04			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	C_L = 0	0.4	0.6	1.1	0.4	0.6	1	ns
t_{PHL}				0.03	0.3	0.9	0.08	0.3	0.8	
t_{PLH}	A	Y	C_L = 1 pF	0.7	1	1.8	0.7	1	1.7	ns
t_{PHL}				0.2	0.7	1.5	0.3	0.7	1.4	
Δt_{PLH}	A	Y		0.2	0.4	0.8	0.2	0.4	0.7	ns/pF
Δt_{PHL}				0.2	0.4	0.7	0.2	0.4	0.6	

IV140LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC04			SN74ASC04			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	C_L = 0	0.4	0.5	0.9	0.4	0.5	0.9	ns
t_{PHL}				0.1	0.4	0.9	0.1	0.4	0.8	
t_{PLH}	A	Y	C_L = 1 pF	0.6	0.9	1.5	0.6	0.9	1.4	ns
t_{PHL}				0.3	0.7	1.5	0.3	0.7	1.4	
Δt_{PLH}	A	Y		0.2	0.3	0.6	0.2	0.3	0.6	ns/pF
Δt_{PHL}				0.2	0.3	0.6	0.2	0.3	0.6	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

IV160LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC04			SN74ASC04			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	C_L = 0	0.3	0.5	0.8	0.3	0.5	0.8	ns
t_{PHL}				0.09	0.3	0.8	0.1	0.3	0.8	
t_{PLH}	A	Y	C_L = 1 pF	0.5	0.7	1.3	0.5	0.7	1.2	ns
t_{PHL}				0.2	0.6	1.3	0.3	0.6	1.2	
Δt_{PLH}	A	Y		0.1	0.2	0.5	0.1	0.2	0.5	ns/pF
Δt_{PHL}				0.1	0.2	0.5	0.1	0.2	0.5	

IV180LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC04			SN74ASC04			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	C_L = 0	0.3	0.4	0.8	0.3	0.4	0.7	ns
t_{PHL}				0.08	0.3	0.8	0.1	0.3	0.7	
t_{PLH}	A	Y	C_L = 1 pF	0.4	0.6	1.1	0.4	0.6	1.1	ns
t_{PHL}				0.2	0.5	1.1	0.2	0.5	1	
Δt_{PLH}	A	Y		0.1	0.2	0.4	0.1	0.2	0.4	ns/pF
Δt_{PHL}				0.1	0.2	0.4	0.1	0.2	0.4	

IV101LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC04			SN74ASC04			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	C_L = 0	1.3	2.3	5	1.3	2.3	4.5	ns
t_{PHL}				1	2	4.6	1	2	4.1	
t_{PLH}	A	Y	C_L = 1 pF	1.3	2.4	5.2	1.4	2.4	4.7	ns
t_{PHL}				1	2.1	4.9	1.1	2.1	4.4	
Δt_{PLH}	A	Y		60	120	230	60	120	200	ps/pF
Δt_{PHL}				30	110	290	50	110	280	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to Section 7.

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SystemCell™ 2-μm INTERNAL STANDARD CELL

- Choice of Four Performance Levels
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

positive logic equations

$$Y = A \cdot B = \overline{\overline{A} + \overline{B}}$$

description

The SN54ASC08 and SN74ASC08 are 2-input positive-AND gate CMOS standard cells each implementing the equivalent of one-fourth of an SN54LS08 or SN74LS08. The standard-cell library contains four physical implementations providing the custom IC designer a choice between four performance levels for optimizing designs. Each option is designated and called from the engineering workstation input using the following cell names to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		TYPICAL DELAY C_L = 1 pF	RELATIVE CELL AREA TO NA210LH
AN210LH	Label: AN2n0LH A,B,Y;	2.1 ns	1.5
AN220LH		1.9 ns	1.75
AN240LH		2.1 ns	2.25
AN260LH		1.7 ns	3

The SN54ASC08 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC08 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS		AN210LH TYP	AN210LH MAX	AN220LH TYP	AN220LH MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current	SN54ASC08	V_{CC} = 4.5 V to 5.5 V,	V_I = V_{CC} or 0,		194		228	nA
		SN74ASC08	T_A = MIN to MAX			11.6		13.6	
C_i	Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.13		0.13		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	0.9		1.2		pF

PARAMETER			TEST CONDITIONS		AN240LH TYP	AN240LH MAX	AN260LH TYP	AN260LH MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current	SN54ASC08	V_{CC} = 4.5 V to 5.5 V,	V_I = V_{CC} or 0,		286		381	nA
		SN74ASC08	T_A = MIN to MAX			17.2		22.8	
C_i	Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.13		0.26		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	2.32		3.08		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

AN210LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC08 MIN	SN54ASC08 TYP‡	SN54ASC08 MAX	SN74ASC08 MIN	SN74ASC08 TYP‡	SN74ASC08 MAX	UNIT
t_{PLH}	A or B	Y	C_L = 0	0.6	1.2	2.8	0.6	1.2	2.5	ns
t_{PHL}				0.8	1.3	2.8	0.8	1.3	2.6	
t_{PLH}	A or B	Y	C_L = 1 pF	1.1	2.2	5	1.2	2.2	4.6	ns
t_{PHL}				1.1	1.9	4.2	1.1	1.9	3.8	
Δt_{PLH}	A or B	Y		0.5	1	2.3	0.5	1	2.1	ns/pF
Δt_{PHL}				0.2	0.6	1.5	0.3	0.6	1.3	

AN220LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC08 MIN	SN54ASC08 TYP‡	SN54ASC08 MAX	SN74ASC08 MIN	SN74ASC08 TYP‡	SN74ASC08 MAX	UNIT
t_{PLH}	A or B	Y	C_L = 0	0.7	1.4	3.3	0.8	1.4	3	ns
t_{PHL}				0.8	1.5	3.1	0.9	1.5	2.8	
t_{PLH}	A or B	Y	C_L = 1 pF	1	2	4.4	1.1	2	4	ns
t_{PHL}				1	1.8	3.9	1.1	1.8	3.5	
Δt_{PLH}	A or B	Y		0.2	0.5	1.2	0.2	0.5	1.1	ns/pF
Δt_{PHL}				0.1	0.3	0.9	0.2	0.3	0.8	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

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AN240LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC08			SN74ASC08			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A or B	Y	C_L = 0	0.9	1.9	4.3	1	1.9	3.8	ns
t_{PHL}				1	1.8	3.7	1.1	1.8	3.4	
t_{PLH}	A or B	Y	C_L = 1 pF	1.1	2.2	5	1.2	2.2	4.4	ns
t_{PHL}				1.1	2	4.4	1.2	2	4	
Δt_{PLH}	A or B	Y		0.1	0.3	0.7	0.1	0.3	0.7	ns/pF
Δt_{PHL}				0.1	0.2	0.7	0.1	0.2	0.6	

AN260LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC08			SN74ASC08			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A or B	Y	C_L = 0	0.7	1.5	3.5	0.8	1.5	3.1	ns
t_{PHL}				0.9	1.5	3	1	1.5	2.9	
t_{PLH}	A or B	Y	C_L = 1 pF	0.8	1.7	3.9	0.9	1.7	3.5	ns
t_{PHL}				1	1.7	3.4	1	1.7	3.2	
Δt_{PLH}	A or B	Y		0.1	0.2	0.5	0.1	0.2	0.4	ns/pF
Δt_{PHL}				0.03	0.16	0.5	0.04	0.16	0.4	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to Section 7

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

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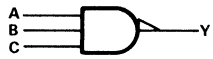
SystemCell™ 2-μm INTERNAL STANDARD CELL

- **Choice of Four Performance Levels**
- **Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V**
- **Functional Operation Over V_{CC} Range of 2 V to 6 V**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol



FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

positive logic equation

$$Y = \overline{ABC} = \overline{A}+\overline{B}+\overline{C}$$

description

The SN54ASC10 and SN74ASC10 are 3-input positive-NAND gate CMOS standard cell, each implementing the equivalent of one-third of an SN54LS10 or SN74LS10. The standard-cell library contains four physical implementations providing the custom IC designer a choice between four performance levels for optimizing design. The four options are designated and called from the engineering workstation input using the following cell names to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		TYPICAL DELAY C_L = 1 pF	RELATIVE CELL AREA TO NA210LH
NA310LH	Label: NA3n0LH A,B,C,Y;	2.2 ns	1.25
NA320LH		1.5 ns	2
NA330LH		1.3 ns	2.5
NA340LH		1.1 ns	3.5

The SN54ASC10 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC10 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS		NA310LH TYP	NA310LH MAX	NA320LH TYP	NA320LH MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current	SN54ASC10	V_{CC} = 4.5 V to 5.5 V,	V_I = V_{CC} or 0,		163		255	nA
		SN74ASC10	T_A = MIN to MAX			9.78		15.3	
C_i	Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.12		0.26		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	0.5		0.94		pF

PARAMETER			TEST CONDITIONS		NA330LH TYP	NA330LH MAX	NA340LH TYP	NA340LH MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current	SN54ASC10	V_{CC} = 4.5 V to 5.5 V,	V_I = V_{CC} or 0,		344		435	nA
		SN74ASC10	T_A = MIN to MAX			20.6		26.1	
C_i	Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.39		0.52		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	1.41		1.86		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

NA310LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC10 MIN	SN54ASC10 TYP‡	SN54ASC10 MAX	SN74ASC10 MIN	SN74ASC10 TYP‡	SN74ASC10 MAX	UNIT
t_{PLH}	A,B,C	Y	C_L = 0	0.7	0.8	1.9	0.6	0.8	1.7	ns
t_{PHL}				0.5	0.7	2.1	0.6	0.7	1.8	
t_{PLH}	A,B,C	Y	C_L = 1 pF	1	2	4.8	1.1	2	4.4	ns
t_{PHL}				1.1	2.4	5.8	1.3	2.4	5.1	
Δt_{PLH}	A,B,C	Y		0.5	1.2	3.1	0.5	1.2	2.9	ns/pF
Δt_{PHL}				0.6	1.4	3.8	0.7	1.4	3.2	

NA320LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC10 MIN	SN54ASC10 TYP‡	SN54ASC10 MAX	SN74ASC10 MIN	SN74ASC10 TYP‡	SN74ASC10 MAX	UNIT
t_{PLH}	A,B,C	Y	C_L = 0	0.5	0.9	1.5	0.6	0.9	1.5	ns
t_{PHL}				0.3	0.8	1.7	0.4	0.8	1.6	
t_{PLH}	A,B,C	Y	C_L = 1 pF	0.8	1.4	2.8	0.9	1.4	2.6	ns
t_{PHL}				0.6	1.5	3.4	0.8	1.5	3.1	
Δt_{PLH}	A,B,C	Y		0.3	0.5	1.3	0.3	0.5	1.1	ns/pF
Δt_{PHL}				0.3	0.7	1.8	0.4	0.7	1.5	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

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NA330LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC10			SN74ASC10			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A,B,C	Y	C_L = 0	0.5	0.8	1.5	0.6	0.8	1.5	ns
t_{PHL}				0.3	0.8	1.7	0.5	0.8	1.6	
t_{PLH}	A,B,C	Y	C_L = 1 pF	0.7	1.2	2.3	0.8	1.2	2.2	ns
t_{PHL}				0.6	1.3	2.9	0.7	1.3	2.6	
Δt_{PLH}	A,B,C	Y		0.2	0.4	0.8	0.2	0.4	0.8	ns/pF
Δt_{PHL}				0.2	0.5	1.2	0.2	0.5	1	

NA340LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC10			SN74ASC10			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A,B,C	Y	C_L = 0	0.5	0.8	1.5	0.5	0.8	1.4	ns
t_{PHL}				0.3	0.7	1.6	0.3	0.7	1.5	
t_{PLH}	A,B,C	Y	C_L = 1 pF	0.6	1.1	2.1	0.7	1.1	2	ns
t_{PHL}				0.4	1.1	2.5	0.5	1.1	2.2	
Δt_{PLH}	A,B,C	Y		0.2	0.3	0.7	0.2	0.3	0.6	ns/pF
Δt_{PHL}				0.2	0.4	0.9	0.2	0.4	0.8	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to Section 7

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

D2939, AUGUST 1986

SystemCell™ 2-μm INTERNAL STANDARD CELL

- **Choice of Four Performance Levels**
- **Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V**
- **Functional Operation Over V_{CC} Range of 2 V to 6 V**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol

FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

positive logic equation

$$Y = A\,B\,C = \overline{\overline{A}+\overline{B}+\overline{C}}$$

description

The SN54ASC11 and SN74ASC11 are 3-input positive-AND gate CMOS standard cells implementing the equivalent of one-third of an SN54LS11 or SN74LS11. The standard-cell library contains four physical implementations providing the custom IC designer a choice between four performance levels for optimizing designs. The four options are designated and called from the engineering workstation input using the following cell names to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		TYPICAL DELAY C_L = 1 pF	RELATIVE CELL AREA TO NA210LH
AN310LH	Label: AN3n0LH A,B,C,Y;	2.4 ns	1.75
AN320LH		2.2 ns	2
AN340LH		2.5 ns	2.5
AN360LH		1.9 ns	3.5

The SN54ASC11 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC11 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS		AN310LH		AN320LH		UNIT
					TYP	MAX	TYP	MAX	
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current	SN54ASC11	V_{CC} = 4.5 V to 5.5 V,	V_I = V_{CC} or 0,		221		249	nA
		SN74ASC11	T_A = MIN to MAX			13.3		15	
C_i	Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.12		0.12		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	1.06		1.56		pF

PARAMETER			TEST CONDITIONS		AN340LH		AN360LH		UNIT
					TYP	MAX	TYP	MAX	
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current	SN54ASC11	V_{CC} = 4.5 V to 5.5 V,	V_I = V_{CC} or 0,		311		438	nA
		SN74ASC11	T_A = MIN to MAX			18.7		26.3	
C_i	Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.12		0.26		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	2.59		4.08		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

AN310LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC11			SN74ASC11			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A,B,C	Y	C_L = 0	0.8	1.6	3.8	0.8	1.6	3.3	ns
t_{PHL}				0.9	1.6	3.3	1	1.6	3	
t_{PLH}	A,B,C	Y	C_L = 1 pF	1.3	2.6	6	1.4	2.6	5.4	ns
t_{PHL}				1.2	2.2	4.7	1.3	2.2	4.3	
Δt_{PLH}	A,B,C	Y		0.5	1	2.3	0.5	1	2.1	ns/pF
Δt_{PHL}				0.2	0.6	1.5	0.3	0.6	1.4	

AN320LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC11			SN74ASC11			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A,B,C	Y	C_L = 0	0.8	1.8	4.2	0.9	1.8	3.8	ns
t_{PHL}				0.9	1.6	3.5	0.9	1.6	3.2	
t_{PLH}	A,B,C	Y	C_L = 1 pF	1.1	2.3	5.4	1.2	2.3	4.8	ns
t_{PHL}				1.1	2	4.4	1.2	2	4	
Δt_{PLH}	A,B,C	Y		0.2	0.5	1.3	0.3	0.5	1.1	ns/pF
Δt_{PHL}				0.1	0.4	0.9	0.1	0.4	0.8	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

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AN340LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC11			SN74ASC11			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A,B,C	Y	C_L = 0	1.1	2.3	5.6	1.1	2.3	4.9	ns
t_{PHL}				1.1	2.1	4.6	1.1	2.1	4.1	
t_{PLH}	A,B,C	Y	C_L = 1 pF	1.2	2.6	6.3	1.3	2.6	5.6	ns
t_{PHL}				1.2	2.3	5.2	1.3	2.3	4.7	
Δt_{PLH}	A,B,C	Y		0.1	0.3	0.8	0.1	0.3	0.7	ns/pF
Δt_{PHL}				0.1	0.2	0.7	0.1	0.2	0.6	

AN360LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC11			SN74ASC11			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A,B,C	Y	C_L = 0	0.8	1.8	4.3	0.9	1.8	3.8	ns
t_{PHL}				0.9	1.6	3.5	0.9	1.6	3.3	
t_{PLH}	A,B,C	Y	C_L = 1 pF	1	2	4.8	1	2	4.3	ns
t_{PHL}				1	1.8	3.9	1	1.8	3.6	
Δt_{PLH}	A,B,C	Y		0.1	0.2	0.5	0.1	0.2	0.5	ns/pF
Δt_{PHL}				0.08	0.2	0.5	0.08	0.2	0.4	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to Section 7

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

D2939, August 1986

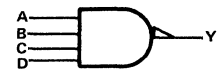
SystemCell™ 2-μm INTERNAL STANDARD CELL

- Choice of Three Performance Levels
- Specified for Operation Over V_{CC} Range of 5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

positive logic equation

$$Y = \overline{A \cdot B \cdot C \cdot D} = \overline{A} + \overline{B} + \overline{C} + \overline{D}$$

logic symbol



FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

description

The SN54ASC20 and SN74ASC20 are four-input positive-NAND gate CMOS standard cells, each implementing the equivalent of one-half of an SN54LS20 or SN74LS20. The standard-cell library contains three physical implementations to provide the custom IC designer a choice from three performance levels for optimizing designs. Each option is designated and called from the engineering workstation input using the following cell names to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		TYPICAL DELAY C_L = 1 pF	RELATIVE CELL AREA TO NA210LH
NA410LH	Label: NA4n0LH A,B,C,D,Y;	2.6 ns	1.5
NA420LH		1.8 ns	2.5
NA430LH		1.5 ns	3.75

The SN54ASC20 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC20 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS	NA410LH TYP	NA410LH MAX	NA420LH TYP	NA420LH MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current	SN54ASC20	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0,		187		312	nA
		SN54ASC20	T_A = MIN to MAX		11.2		18.7	
C_i	Input capacitance		V_{CC} = 5 V, T_A = 25°C	0.12		0.27		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, t_r = t_f = 3 ns, T_A = 25°C	0.5		0.96		pF

PARAMETER			TEST CONDITIONS	NA430LH TYP	NA430LH MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		V
I_{CC}	Supply current	SN54ASC20	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0,		441	nA
		SN74ASC20	T_A = MIN to MAX		26.4	
C_i	Input capacitance		V_{CC} = 5 V, T_A = 25°C	0.4		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, t_r = t_f = 3 ns, T_A = 25°C	1.46		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

NA410LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC20 MIN	SN54ASC20 TYP‡	SN54ASC20 MAX	SN74ASC20 MIN	SN74ASC20 TYP‡	SN74ASC20 MAX	UNIT
t_{PLH}	A,B,C,D	Y	C_L = 0	0.8	1.1	2	0.8	1.1	1.9	ns
t_{PHL}				0.6	1.1	2.7	0.6	1.1	2.4	
t_{PLH}	A,B,C,D	Y	C_L = 1 pF	1.3	2.4	5.7	1.3	2.4	5.2	ns
t_{PHL}				1.4	2.9	7.5	1.5	2.9	6.5	
Δt_{PLH}	A,B,C,D	Y		0.5	1.3	3.9	0.5	1.3	3.5	ns/pF
Δt_{PHL}				0.8	1.8	4.8	0.8	1.8	4.1	

NA420LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC20 MIN	SN54ASC20 TYP‡	SN54ASC20 MAX	SN74ASC20 MIN	SN74ASC20 TYP‡	SN74ASC20 MAX	UNIT
t_{PLH}	A,B,C,D	Y	C_L = 0	0.6	1	1.8	0.7	1	1.7	ns
t_{PHL}				0.5	1	2.4	0.5	1	2.1	
t_{PLH}	A,B,C,D	Y	C_L = 1 pF	0.9	1.6	3.3	1	1.6	3	ns
t_{PHL}				0.8	1.9	4.6	1	1.9	4	
Δt_{PLH}	A,B,C,D	Y		0.3	0.6	1.5	0.3	0.6	1.4	ns/pF
Δt_{PHL}				0.4	0.8	2.3	0.4	0.8	2	

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NA430LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC20			SN74ASC20			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A,B,C,D	Y	C_L = 0	0.6	1	1.9	0.6	1	1.8	ns
t_{PHL}				0.4	1	2.3	0.5	1	2.1	
t_{PLH}	A,B,C,D	Y	C_L = 1 pF	0.8	1.4	2.9	0.9	1.4	2.7	ns
t_{PHL}				0.7	1.6	3.9	0.8	1.6	3.4	
Δt_{PLH}	A,B,C,D	Y		0.2	0.4	1.1	0.2	0.4	1	ns/pF
Δt_{PHL}				0.3	0.6	1.6	0.3	0.6	1.3	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

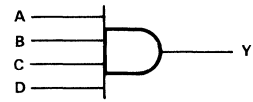
All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

D2939, AUGUST 1986

SystemCell™ 2-μm INTERNAL STANDARD CELL

- **Choice of Four Performance Levels**
- **Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V**
- **Functional Operation Over V_{CC} Range of 2 V to 6 V**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol



FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	H
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L

positive logic equations

$$Y = A \cdot B \cdot C \cdot D = \overline{\overline{A}+\overline{B}+\overline{C}+\overline{D}}$$

description

The SN54ASC21 and SN74ASC21 are 4-input positive-AND gate CMOS standard-cells implementing the equivalent of one-half of an SN54LS21 or SN74LS21. The standard-cell library contains four physical implementations providing the custom IC designer a choice between four performance levels for optimizing designs. The four options are designated and called from the engineering workstation input using the following cell names to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		TYPICAL DELAY C_L = 1 pF	RELATIVE CELL AREA TO NA210LH
AN410LH	Label: AN4n0LH A,B,C,D,Y;	2.6 ns	2
AN420LH		2.5 ns	2.25
AN440LH		2.7 ns	2.75
AN460LH		2.3 ns	4

The SN54ASC21 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC21 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS		AN410LH TYP	AN410LH MAX	AN420LH TYP	AN420LH MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
	Supply current	SN54ASC21	V_{CC} = 4.5 V to 5.5 V,	V_I = V_{CC} or 0,		256		286	nA
		SN74ASC21	T_A = MIN to MAX			20.9		30	
C_i	Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.12		0.12		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	$t_r = t_f$ = 3 ns,	1.18		1.72		pF

PARAMETER			TEST CONDITIONS		AN440LH TYP	AN440LH MAX	AN460LH TYP	AN460LH MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
	Supply current	SN54ASC21	V_{CC} = 4.5 V to 5.5 V,	V_I = V_{CC} or 0,		348		500	nA
		SN74ASC21	T_A = MIN to MAX			20.9		30	
C_i	Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.12		0.27		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	$t_r = t_f$ = 3 ns,	2.77		4.58		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

AN410LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC21 MIN	SN54ASC21 TYP‡	SN54ASC21 MAX	SN74ASC21 MIN	SN74ASC21 TYP‡	SN74ASC21 MAX	UNIT
t_{PLH}	A,B,C,D	Y	C_L = 0	0.9	1.9	4.8	1	1.9	4.2	ns
t_{PHL}				1	1.7	3.8	1	1.7	3.4	
t_{PLH}	A,B,C,D	Y	C_L = 1 pF	1.4	2.9	7.1	1.5	2.9	6.3	ns
t_{PHL}				1.3	2.3	5.3	1.3	2.3	4.7	
Δt_{PLH}	A,B,C,D	Y		0.5	1	2.4	0.5	1	2.2	ns/pF
Δt_{PHL}				0.2	0.6	1.5	0.3	0.6	1.4	

AN420LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC21 MIN	SN54ASC21 TYP‡	SN54ASC21 MAX	SN74ASC21 MIN	SN74ASC21 TYP‡	SN74ASC21 MAX	UNIT
t_{PLH}	A,B,C,D	Y	C_L = 0	1	2.1	5.5	1.1	2.1	4.8	ns
t_{PHL}				1	1.8	4.1	1	1.8	3.7	
t_{PLH}	A,B,C,D	Y	C_L = 1 pF	1.3	2.7	6.7	1.4	2.7	5.9	ns
t_{PHL}				1.2	2.2	5	1.2	2.2	4.5	
Δt_{PLH}	A,B,C,D	Y		0.2	0.6	1.3	0.2	0.6	1.2	ns/pF
Δt_{PHL}				0.1	0.4	1	0.1	0.4	0.9	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

AN440LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC21			SN74ASC21			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A,B,C,D	Y	C_L = 0	1.2	2.7	7.2	1.3	2.7	6.2	ns
t_{PHL}				1.1	2.1	5.1	1.2	2.1	4.6	
t_{PLH}	A,B,C,D	Y	C_L = 1 pF	1.4	3	8	1.5	3	6.9	ns
t_{PHL}				1.2	2.4	5.8	1.3	2.4	5.2	
Δt_{PLH}	A,B,C,D	Y		0.1	0.3	0.8	0.1	0.3	0.7	ns/pF
Δt_{PHL}				0.1	0.3	0.7	0.1	0.3	0.6	

AN460LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC21			SN74ASC21			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A,B,C,D	Y	C_L = 0	1	2.3	5.7	1.1	2.3	5	ns
t_{PHL}				0.9	1.8	4	1	1.8	3.6	
t_{PLH}	A,B,C,D	Y	C_L = 1 pF	1.1	2.5	6.3	1.2	2.5	5.5	ns
t_{PHL}				1.1	2	4.5	1.1	2	4.1	
Δt_{PLH}	A,B,C,D	Y		0.1	0.2	0.6	0.1	0.2	0.5	ns/pF
Δt_{PHL}				0.09	0.2	0.5	0.1	0.2	0.5	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to Section 7

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

D2939, AUGUST 1986

SystemCell™ 2-μm INTERNAL STANDARD CELL

- **Choice of Three Performance Levels**
- **Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V**
- **Functional Operation Over V_{CC} Range of 2 V to 6 V**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol

FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
H	X	X	L
X	H	X	L
X	X	H	L
L	L	L	H

positive logic equation

$$Y = \overline{A+B+C} = \overline{A}\,\overline{B}\,\overline{C}$$

description

The SN54ASC27 and SN74ASC27 are 3-input positive-NOR gate CMOS standard cells, each implementing the equivalent of one-third of an SN54LS27 or SN74LS27. The standard-cell library contains three physical implementations providing the custom IC designer a choice from three performance levels for optimizing designs. The three options are designated and called from the engineering workstation input using the following cell names to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		TYPICAL DELAY C_L = 1 pF	RELATIVE CELL AREA TO NA210LH
NO310LH	Label: NO3n0LH A,B,C,Y;	3.2 ns	1.25
NO320LH		2.1 ns	2
NO330LH		1.8 ns	2.75

The SN54ASC27 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC27 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS	NO310LH		NO320LH		NO330LH		UNIT
				TYP	MAX	TYP	MAX	TYP	MAX	
V_T	Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		2.2		V
I_{CC}	Supply current	SN54ASC27	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0,		156		233		312	nA
		SN74ASC27	T_A = MIN to MAX		9.33		14		18.7	
C_i	Input capacitance		V_{CC} = 5 V, T_A = 25°C	0.11		0.24		0.35		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, t_r = t_f = 3 ns, T_A = 25°C	0.32		0.56		0.85		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

NO310LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC27			SN74ASC27			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A,B,C	Y	C_L = 0	0.6	1	2.6	0.6	1	2.4	ns
t_{PHL}				0.7	1.2	2.1	0.8	1.2	2	
t_{PLH}	A,B,C	Y	C_L = 1 pF	2	4	9.5	2.2	4	8.6	ns
t_{PHL}				1.3	2.4	5.9	1.4	2.4	5.2	
Δt_{PLH}	A,B,C	Y		1.4	3	6.9	1.5	3	6.3	ns/pF
Δt_{PHL}				0.5	1.2	3.9	0.5	1.2	3.3	

NO320LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC27			SN74ASC27			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A,B,C	Y	C_L = 0	0.6	1	2.1	0.7	1	1.9	ns
t_{PHL}				0.5	1.1	2	0.6	1.1	1.9	
t_{PLH}	A,B,C	Y	C_L = 1 pF	1.3	2.4	5.4	1.4	2.4	4.9	ns
t_{PHL}				1	1.7	3.5	1	1.7	3.2	
Δt_{PLH}	A,B,C	Y		0.6	1.4	3.4	0.7	1.4	3.1	ns/pF
Δt_{PHL}				0.4	0.6	1.6	0.4	0.6	1.4	

NO330LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC27			SN74ASC27			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A,B,C	Y	C_L = 0	0.6	1	2	0.6	1	1.8	ns
t_{PHL}				0.4	1	1.9	0.5	1	1.8	
t_{PLH}	A,B,C	Y	C_L = 1 pF	1.1	2	4.3	1.2	2	3.9	ns
t_{PHL}				0.8	1.5	2.9	0.8	1.5	2.7	
Δt_{PLH}	A,B,C	Y		0.4	1	2.3	0.5	1	2.1	ns/pF
Δt_{PHL}				0.3	0.5	1.1	0.3	0.5	0.9	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

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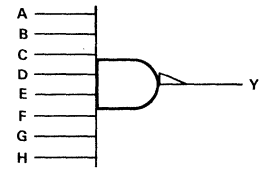
D2939, AUGUST 1986

SystemCell™ 2-μm INTERNAL STANDARD CELL

- Choice of Two Performance Levels
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol



positive logic equation

$$Y = \overline{ABCDEFGH} = \overline{A}+\overline{B}+\overline{C}+\overline{D}+\overline{E}+\overline{F}+\overline{G}+\overline{H}$$

FUNCTION TABLE

INPUTS								OUTPUT
A	B	C	D	E	F	G	H	Y
H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	H
X	X	X	L	X	X	X	X	H
X	X	X	X	L	X	X	X	H
X	X	X	X	X	L	X	X	H
X	X	X	X	X	X	L	X	H
X	X	X	X	X	X	X	L	H

description

The SN54ASC30 and SN74ASC30 are 8-input positive-NAND gate CMOS standard cells each implementing the equivalent of an SN54LS30 or SN74LS30. The standard-cell library contains two physical implementations providing the custom IC designer a choice between two performance levels for optimizing designs. The two options are designated and called from the engineering workstation input using the following cell names to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		TYPICAL DELAY C_L = 1 pF	RELATIVE CELL AREA TO NA210LH
NA810LH	Label: NA8n0LH A,B,C,D,E,F,G,H,Y;	4.5 ns	2.5
NA820LH		3.3 ns	4.75

The SN54ASC30 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC30 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS		NA810LH TYP	NA810LH MAX	NA820LH TYP	NA820LH MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current	SN54ASC30	V_{CC} = 4.5 V to 5.5 V,	V_I = V_{CC} or 0,		290		502	nA
		SN74ASC30	T_A = MIN to MAX			17.4		30.1	
C_i	Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.12		0.22		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	0.61		1.13		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

NA810LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC30 MIN	SN54ASC30 TYP‡	SN54ASC30 MAX	SN74ASC30 MIN	SN74ASC30 TYP‡	SN74ASC30 MAX	UNIT
t_{PLH}	A thru H	Y	C_L = 0	0.9	1.8	4.2	0.9	1.8	3.7	ns
t_{PHL}				0.8	2	6.5	0.9	2	5.6	
t_{PLH}	A thru H	Y	C_L = 1 pF	1.6	3.6	8	1.7	3.6	7.3	ns
t_{PHL}				2.3	5.3	5.2	2.5	5.3	13.1	
Δt_{PLH}	A thru H	Y		0.6	1.8	4.9	0.6	1.8	4.7	ns/pF
Δt_{PHL}				1.4	3.3	8.7	1.6	3.3	7.5	

NA820LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC30 MIN	SN54ASC30 TYP‡	SN54ASC30 MAX	SN74ASC30 MIN	SN74ASC30 TYP‡	SN74ASC30 MAX	UNIT
t_{PLH}	A thru H	Y	C_L = 0	1	1.6	3.6	1	1.6	3.3	ns
t_{PHL}				0.9	2.1	5.8	1	2.1	5	
t_{PLH}	A thru H	Y	C_L = 1 pF	1.5	2.6	5.7	1.6	2.6	5.3	ns
t_{PHL}				1.8	4	10.8	2.1	4	9.3	
Δt_{PLH}	A thru H	Y		0.4	1	2.3	0.5	1	2.1	ns/pF
Δt_{PHL}				0.8	1.9	5.1	0.9	1.9	4.4	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to Section 7

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

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D2939, AUGUST 1986

SystemCell™ 2-μm INTERNAL STANDARD CELL

- **Choice of Four Performance Levels**
- **Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V**
- **Functional Operation Over V_{CC} Range of 2 V to 6 V**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

positive logic equation

$$Y = A + B = \overline{\overline{A}\,\overline{B}}$$

description

The SN54ASC32 and SN74ASC32 are 2-input positive-OR gate CMOS standard cells each implementing the equivalent of one-fourth of an SN54LS32 or SN74LS32. The standard- cell library contains four physical implementations providing the custom IC designer a choice between four performance levels for optimizing design. The four options are designated and called from the engineering workstation input using the following cell names to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		TYPICAL DELAY C_L = 1 pF	RELATIVE CELL AREA TO NA210LH
OR210LH	Label: OR2n0LH A,B,Y;	2.3 ns	1.5
OR220LH		2.1 ns	1.75
OR240LH		1.8 ns	2.6
OR260LH		1.7 ns	3.75

The SN54ASC32 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC32 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS		OR210LH TYP	OR210LH MAX	OR220LH TYP	OR220LH MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current	SN54ASC32	V_{CC} = 4.5 V to 5.5 V,	V_I = V_{CC} or 0,		185		217	nA
		SN74ASC32	T_A = MIN to MAX			11.1		13	
C_i	Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.11		0.11		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	0.86		1.62		pF

PARAMETER			TEST CONDITIONS		OR240LH TYP	OR240LH MAX	OR260LH TYP	OR260LH MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current	SN54ASC32	V_{CC} = 4.5 V to 5.5 V,	V_I = V_{CC} or 0,		305		461	nA
		SN74ASC32	T_A = MIN to MAX			18.3		27.7	
C_i	Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.22		0.36		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	3.09		4.7		pF

4 Data Sheets

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

OR210LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC32 MIN	SN54ASC32 TYP‡	SN54ASC32 MAX	SN74ASC32 MIN	SN74ASC32 TYP‡	SN74ASC32 MAX	UNIT
t_{PLH}	A or B	Y	C_L = 0	0.6	1.3	2.9	0.6	1.3	2.7	ns
t_{PHL}				0.9	1.7	3.6	1	1.7	3.3	
t_{PLH}	A or B	Y	C_L = 1 pF	1.1	2.3	5.2	1.2	2.3	4.8	ns
t_{PHL}				1.2	2.3	5.2	1.3	2.3	4.6	
Δt_{PLH}	A or B	Y		0.5	1	2.3	0.5	1	2.1	ns/pF
Δt_{PHL}				0.2	0.6	1.6	0.3	0.6	1.4	

OR220LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC32 MIN	SN54ASC32 TYP‡	SN54ASC32 MAX	SN74ASC32 MIN	SN74ASC32 TYP‡	SN74ASC32 MAX	UNIT
t_{PLH}	A or B	Y	C_L = 0	0.7	1.5	3.4	0.8	1.5	3.2	ns
t_{PHL}				1	1.8	4.2	1	1.8	3.8	
t_{PLH}	A or B	Y	C_L = 1 pF	1	2	4.6	1	2	4.2	ns
t_{PHL}				1.2	2.2	5.1	1.2	2.2	4.6	
Δt_{PLH}	A or B	Y		0.2	0.5	1.2	0.2	0.5	1.1	ns/pF
Δt_{PHL}				0.1	0.4	1	0.2	0.4	0.9	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

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OR240LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC32			SN74ASC32			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A or B	Y	C_L = 0	0.6	1.4	3.1	0.7	1.4	2.8	ns
t_{PHL}				0.9	1.7	3.6	0.9	1.7	3.4	
t_{PLH}	A or B	Y	C_L = 1 pF	0.8	1.7	3.7	0.9	1.7	3.3	ns
t_{PHL}				1	1.9	4.2	1.1	1.9	3.9	
Δt_{PLH}	A or B	Y		0.1	0.3	0.6	0.1	0.3	0.6	ns/pF
Δt_{PHL}				0.1	0.2	0.6	0.1	0.2	0.6	

OR260LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC32			SN74ASC32			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A or B	Y	C_L = 0	0.6	1.4	3	0.7	1.4	2.8	ns
t_{PHL}				0.9	1.6	3.7	0.9	1.6	3.4	
t_{PLH}	A or B	Y	C_L = 1 pF	0.7	1.6	3.4	0.8	1.6	3.1	ns
t_{PHL}				1	1.8	4.1	1	1.8	3.7	
Δt_{PLH}	A or B	Y		0.1	0.2	0.5	0.1	0.2	0.4	ns/pF
Δt_{PHL}				0.07	0.2	0.5	0.09	0.2	0.4	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to Section 7

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

D2939, AUGUST 1986

SystemCell™ 2-μm HARDWIRED MACRO CELLS

- **All Cells Provide Complementary Q and QZ Outputs**
- **Choice between Two Relative Output Drive Capabilities**
- **Choice of Asynchronous Inputs Provides Custom Cell for Most Applications**
- **Implements High-Speed Registers: Clock Frequencies . . . 46 to 69 MHz**

FLIP-FLOP CELL CONFIGURATIONS OFFERED

CELL NAME	PRESET	CLEAR	DRIVE LEVEL
DFB20LH	Yes	Yes	2X
DFC20LH	No	Yes	2X
DFN20LH	No	No	2X
DFP20LH	Yes	No	2X
DFY20LH	Yes	No	2X
DFZ20LH	Yes	Yes	2X
DTB10LH	Yes	Yes	1X
DTC10LH	No	Yes	1X
DTN10LH	No	No	1X
DTP10LH	Yes	No	1X

description

The SN54ASC74 and SN74ASC74 are dedicated, hardwired standard-cell macros implementing various D-type flip-flops. The 'ASC74 cell selection offers a broad choice of flip-flop configurations, providing the custom IC designer with specific storage elements to embed in ASICs in their most efficient form: as stand-alone bit-storage devices or as additions to larger synchronous functions such as registers or counters. The DFB20LH and DTB10LH flip-flops are identical in function and sequential operation to one-half of the 'LS74, 'S74, or 'F74 packaged flip-flops.

The other nine cells provide the designer with flip-flop versions having either a preset or clear or no asynchronous input.

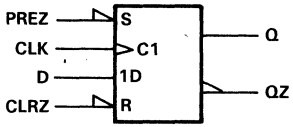
The DFY20LH and DFZ20LH cells feature grounded D inputs meaning that they can simplify implementation of flag registers that can be reset to zero with a system clock. The DFZ20LH offers asynchronous clear and preset inputs providing an option to zero the register with either the system clock or system clear signal, or both.

CELL NAME	NETLIST HDL LABEL	FEATURES	
		MAXIMUM CLOCK FREQUENCY	RELATIVE CELL AREA TO NA210LH
DFB20LH	Label: DFB20LH CLRZ, PREZ, D, CLK, Q, QZ;	46.3 MHz	7.7
DFC20LH	Label: DFC20LH CLRZ, D, CLK, Q, QZ;	52.1 MHz	7.2
DFN20LH	Label: DFN20LH D, CLK, Q, QZ;	64.2 MHz	6.5
DFP20LH	Label: DFP20LH PREZ, D, CLK, Q, QZ;	55.8 MHz	7
DFY20LH	Label: DFY20LH PREZ, CLK, Q, QZ;	69.2 MHz	5.7
DFZ20LH	Label: DFZ20LH CLRZ, PREZ, CLK, Q, QZ;	59.2 MHz	6.5
DTB10LH	Label: DTB10LH CLRZ, PREZ, D, CLK, Q, QZ;	55.8 MHz	6.5
DTC10LH	Label: DTC10LH CLRZ, D, CLK, Q, QZ;	52.1 MHz	6
DTN10LH	Label: DTN10LH D, CLK, Q, QZ;	55.8 MHz	5.2
DTP10LH	Label: DTP10LH PREZ, D, CLK, Q, QZ;	55.8 MHz	6

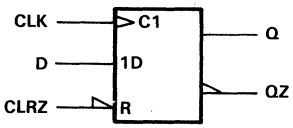
The SN54ASC74 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC74 is characterized for operation from −40°C to 85°C.

logic symbols

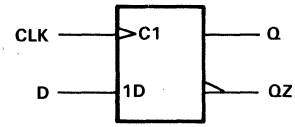
DFB20LH, DTB10LH



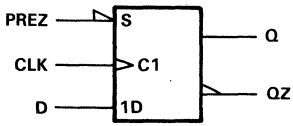
DFC20LH, DTC10LH



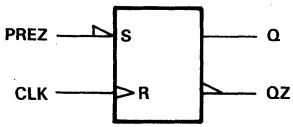
DFN20LH, DTN10LH



DFP20LH, DTP10LH



DFY20LH



FUNCTION TABLES

DFB20LH, DTB10LH

INPUTS				OUTPUTS	
PREZ	CLRZ	CLK	D	Q	QZ
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	L*	L*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

DFC20LH, DTC10LH

INPUTS			OUTPUTS	
CLRZ	CLK	D	Q	QZ
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

DFN20LH, DTN10LH

INPUTS		OUTPUTS	
CLK	D	Q	QZ
↑	H	H	L
↑	L	L	H
L	X	Q_0	$\overline{Q}_0$

DFP20LH, DTP10LH

INPUTS			OUTPUTS	
PREZ	CLK	D	Q	QZ
L	X	X	H	L
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

DFY20LH

INPUTS		OUTPUTS	
PREZ	CLK	Q	QZ
L	X	H	L
H	↑	L	H
H	L	Q_0	$\overline{Q}_0$

* This configuration is nonstable; that is, it will not persist when PREZ or CLRZ returns to its inactive (high) level.

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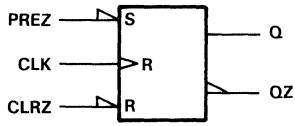
logic symbol

DFZ20LH



FUNCTION TABLE

DFZ20LH

INPUTS			OUTPUTS	
PREZ	CLRZ	CLK	Q	QZ
L	H	X	H	L
H	L	X	L	H
L	L	X	L*	L*
H	H	↑	L	H
H	H	L	Q_0	$\overline{Q}_0$

* This configuration is nonstable; that is, it will not persist when PREZ or CLRZ returns to its inactive (high) level.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			DFB20LH		DFC20LH		DFN20LH		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	46.3	0	52.1	0	64.2	MHz
t_w	Pulse duration	CLRZ low	7.2		6.6				ns
		PREZ low	7.8						
		CLK high or low	10.8		9.6		7.8		
t_{su}	Setup time	CLRZ inactive	7.8		6.6				ns
		PREZ inactive	1.2						
		D high or low	6.6		6.6		4.8		
t_h	Hold time	CLRZ low	1.2		0.6				ns
		PREZ low	3						
		D high or low	2.4		1.8		2.4		

			DFP20LH		DFY20LH		DFZ20LH		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	55.8	0	69.2	0	59.2	MHz
t_w	Pulse duration	CLRZ low					7.2		ns
		PREZ low	7.2		7.2		7.8		
		CLK high or low	9		7.2		8.4		
t_{su}	Setup time	CLRZ inactive							ns
		PREZ inactive	1.2		1.2		1.2		
		D high or low	6						
t_h	Hold time	CLRZ low							ns
		PREZ low	2.4		1.8		3		
		D high or low	3						

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

			DTB10LH		DTC10LH		DTN10LH		DTP10LH		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	55.8	0	52.1	0	55.8	0	55.8	MHz
t_w	Pulse duration	CLRZ low	13.8		10.8						ns
		PREZ low	18.6						20.4		
		CLK high or low	9		9.6		9		9		
t_{su}	Setup time	CLRZ inactive	0.6		0.6						ns
		PREZ inactive	−1.8						−2.4		
		D high or low	3		6		4.8		4.2		
t_h	Hold time	CLRZ low	16.2		12.6						ns
		PREZ low	21						22.2		
		D high or low	3		2.4		2.4		2.4		

electrical characteristics

DFB20LH

PARAMETER			TEST CONDITIONS		SN54ASC74		SN74ASC74		UNIT
					TYP	MAX	TYP	MAX	
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX	V_I = V_{CC} or 0,		934		56	nA
C_i	Input capacitance	CLRZ	V_{CC} = 5 V,	T_A = 25°C	0.36		0.36		pF
		PREZ			0.38		0.38		
		D			0.11		0.11		
		CLK			0.25		0.25		
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	3.76		3.76		pF

DFC20LH

PARAMETER			TEST CONDITIONS		SN54ASC74		SN74ASC74		UNIT
					TYP	MAX	TYP	MAX	
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX	V_I = V_{CC} or 0,		881		52.9	nA
C_i	Input capacitance	CLRZ	V_{CC} = 5 V,	T_A = 25°C	0.36		0.36		pF
		D			0.11		0.11		
		CLK			0.28		0.28		
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	3.39		3.39		pF

DFN20LH

PARAMETER			TEST CONDITIONS		SN54ASC74		SN74ASC74		UNIT
					TYP	MAX	TYP	MAX	
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX	V_I = V_{CC} or 0,		799		47.9	nA
C_i	Input capacitance	D	V_{CC} = 5 V,	T_A = 25°C	0.13		0.13		pF
		CLK			0.27		0.27		
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	2.71		2.71		pF

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electrical characteristics

DFP20LH

PARAMETER			TEST CONDITIONS		SN54ASC74 TYP	SN54ASC74 MAX	SN74ASC74 TYP	SN74ASC74 MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX	V_I = V_{CC} or 0,		845		50.7	nA
C_i	Input capacitance	PREZ	V_{CC} = 5 V,	T_A = 25°C	0.35		0.35		pF
		D			0.13		0.13		
		CLK			0.26		0.26		
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	3.49		3.49		pF

DFY20LH

PARAMETER			TEST CONDITIONS		SN54ASC74 TYP	SN54ASC74 MAX	SN74ASC74 TYP	SN74ASC74 MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX	V_I = V_{CC} or 0,		702		42.1	nA
C_i	Input capacitance	PREZ	V_{CC} = 5 V,	T_A = 25°C	0.35		0.35		pF
		CLK			0.25		0.25		
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	4.63		4.63		pF

DFZ20LH

PARAMETER			TEST CONDITIONS		SN54ASC74 TYP	SN54ASC74 MAX	SN74ASC74 TYP	SN74ASC74 MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX	V_I = V_{CC} or 0,		777		46.6	nA
C_i	Input capacitance	CLRZ	V_{CC} = 5 V,	T_A = 25°C	0.25		0.25		pF
		PREZ			0.23		0.23		
		CLK			0.36		0.36		
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	4.94		4.94		pF

electrical characteristics

DTB10LH

PARAMETER			TEST CONDITIONS		SN54ASC74 TYP	SN54ASC74 MAX	SN74ASC74 TYP	SN74ASC74 MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX	V_I = V_{CC} or 0,		699		41.9	nA
C_i	Input capacitance	CLRZ	V_{CC} = 5 V,	T_A = 25°C	0.12		0.12		pF
		PREZ			0.18		0.18		
		D			0.20		0.20		
		CLK			0.14		0.14		
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	2.12		2.12		pF

DTC10LH

PARAMETER			TEST CONDITIONS		SN54ASC74 TYP	SN54ASC74 MAX	SN74ASC74 TYP	SN74ASC74 MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX	V_I = V_{CC} or 0,		641		38.5	nA
C_i	Input capacitance	CLRZ	V_{CC} = 5 V,	T_A = 25°C	0.11		0.11		pF
		D			0.19		0.19		
		CLK			0.08		0.08		
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	2.1		2.1		pF

DTN10LH

PARAMETER			TEST CONDITIONS		SN54ASC74 TYP	SN54ASC74 MAX	SN74ASC74 TYP	SN74ASC74 MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX	V_I = V_{CC} or 0,		544		32.6	nA
C_i	Input capacitance	D	V_{CC} = 5 V,	T_A = 25°C	0.10		0.10		pF
		CLK			0.11		0.11		
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	2.21		2.21		pF

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DTP10LH

PARAMETER		TEST CONDITIONS	SN54ASC74		SN74ASC74		UNIT
			TYP	MAX	TYP	MAX	
V_T Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC} Supply current		V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		638		38.3	nA
C_i Input capacitance	PREZ	V_{CC} = 5 V, T_A = 25°C	0.19		0.19		pF
	D		0.14		0.14		
	CLK		0.11		0.11		
C_{pd} Equivalent power dissipation capacitance		V_{CC} = 5 V, t_r = t_f = 3 ns, T_A = 25°C	2.5		2.5		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

DFB20LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC74			SN74ASC74			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	CLK	Q,QZ	C_L = 0	2.1	4.9	12.7	2.3	4.9	11.1	ns
t_{PHL}				1.4	3.2	8.2	1.6	3.2	7.2	
t_{PLH}	PREZ,CLRZ	Q,QZ		1.9	3.9	9.3	2	3.9	8.3	ns
t_{PHL}				1.1	2	4.2	1.1	2	3.8	
t_{PLH}	CLK	Q,QZ	C_L = 1 pF	2.4	5.4	13.9	2.6	5.4	12.2	ns
t_{PHL}				1.6	3.6	9.2	1.8	3.6	8.1	
t_{PLH}	PREZ,CLRZ	Q,QZ		2.2	4.4	10.6	2.3	4.4	9.4	ns
t_{PHL}				1.3	2.4	5.2	1.3	2.4	4.7	
Δt_{PLH}	Any	Q,QZ		0.2	0.5	1.3	0.2	0.5	1.2	ns/pF
Δt_{PHL}				0.1	0.4	1	0.1	0.4	0.9	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

DFC20LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC74			SN74ASC74			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	CLK	Q,$\overline{Q}$	C_L = 0	1.9	4.5	12.2	2	4.5	10.7	ns
t_{PHL}				1.4	3	7.9	1.5	3	5.7	
t_{PLH}	CLRZ	$\overline{Q}$		1.8	3.5	8.1	1.9	3.5	7.2	ns
t_{PHL}		Q		1	1.8	3.9	1.1	1.8	3.6	
t_{PLH}	CLK	Q,$\overline{Q}$	C_L = 1 pF	2.1	5	13.4	2.3	5	11.8	ns
t_{PHL}				1.5	3.4	8.8	1.7	3.4	7.7	
t_{PLH}	CLRZ	$\overline{Q}$		2.1	4	9.3	2.2	4	8.3	ns
t_{PHL}		Q		1.2	2.2	4.9	1.3	2.2	4.4	
Δt_{PLH}	Any	Q,$\overline{Q}$		0.2	0.5	1.3	0.2	0.5	1.1	ns/pF
Δt_{PHL}				0.1	0.4	1	0.1	0.4	0.8	

DFN20LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC74			SN74ASC74			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	CLK	Q,$\overline{Q}$	C_L = 0	1.7	3.7	9.5	1.8	3.7	8.4	ns
t_{PHL}				1.2	2.6	6.6	1.3	2.6	5.9	
t_{PLH}	CLK	Q,$\overline{Q}$	C_L = 1 pF	1.9	4.2	10.7	2.1	4.2	9.4	ns
t_{PHL}				1.4	3	7.5	1.5	3	6.7	
Δt_{PLH}	CLK	Q,$\overline{Q}$		0.2	0.5	1.2	0.2	0.5	1.1	ns/pF
Δt_{PHL}				0.1	0.4	0.9	0.1	0.4	0.8	

DFP20LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC74			SN74ASC74			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	CLK	Q,$\overline{Q}$	C_L = 0	1.8	4.3	12	1.9	4.3	9.6	ns
t_{PHL}				1.3	3	7.8	1.4	3	6.9	
t_{PLH}	PREZ	Q		1.7	3.3	7.7	1.8	3.3	6.9	ns
t_{PHL}		$\overline{Q}$		1.1	2	4.1	1.2	2	3.8	
t_{PLH}	CLK	Q,$\overline{Q}$	C_L = 1 pF	2	4.8	13.2	2.2	4.8	11.6	ns
t_{PHL}				1.5	3.4	8.7	1.6	3.4	7.6	
t_{PLH}	PREZ	Q		2	3.8	8.9	2.1	3.8	7.9	ns
t_{PHL}		$\overline{Q}$		1.3	2.4	5	1.3	2.4	4.5	
Δt_{PLH}	Any	Q,$\overline{Q}$		0.2	0.5	1.3	0.2	0.5	1.1	ns/pF
Δt_{PHL}				0.1	0.4	1	0.1	0.4	0.8	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

DFY20LH and DFZ20LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC74			SN74ASC74			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	CLK	Q,QZ	C_L = 0	1.8	4.3	11.7	1.9	4.3	10.3	ns
t_{PHL}				1.2	2.6	6.6	1.2	2.6	5.9	
t_{PLH}	PREZ,CLRZ§	Q,QZ		1.6	3.6	9.7	1.9	3.6	8.5	ns
t_{PHL}				1.1	1.9	4.1	1.1	1.9	3.8	
t_{PLH}	CLK	Q,QZ	C_L = 1 pF	2	4.8	12.8	2.2	4.8	11.3	ns
t_{PHL}				1.3	3	7.6	1.4	3	6.8	
t_{PLH}	PREZ,CLRZ§	Q,QZ		1.8	4.1	10.8	1.9	4.1	9.6	ns
t_{PHL}				1.2	2.3	5.1	1.3	2.3	4.6	
Δt_{PLH}	Any	Q,QZ		0.2	0.5	1.3	0.2	0.5	1.1	ns/pF
Δt_{PHL}				0.1	0.4	1	0.1	0.4	0.9	

DTB10LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC74			SN74ASC74			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	CLK	Q,QZ	C_L = 0	1.5	3.1	7.7	1.6	3.1	6.8	ns
t_{PHL}				1.6	3.5	8.9	1.8	3.5	7.9	
t_{PLH}	PREZ	Q		2.1	4.2	10.1	2.2	4.2	9.1	ns
t_{PHL}		QZ		0.8	1.4	2.9	0.9	1.4	2.7	
t_{PHL}	CLRZ	Q		2	4	9.3	2.1	4	8.3	ns
t_{PLH}		QZ		1.9	3.8	8.9	2	3.8	7.9	
t_{PLH}	CLK	Q,QZ	C_L = 1 pF	2	4.1	9.9	2.2	4.1	8.9	ns
t_{PHL}				2.2	4.8	12	2.4	4.8	10.6	
t_{PLH}	PREZ	Q		2.6	5.2	12.5	2.8	5.2	11.2	ns
t_{PHL}		QZ		1.4	2.7	6.1	1.5	2.7	5.4	
t_{PHL}	CLRZ	Q		2.6	5.3	12.7	2.8	5.3	11.3	ns
t_{PLH}		QZ		2.4	4.8	11.1	2.6	4.8	9.9	
Δt_{PLH}	CLK	Q,QZ		0.4	1	2.5	0.5	1	2.2	ns/pF
Δt_{PHL}				0.5	1.3	3.4	0.6	1.3	2.9	
Δt_{PLH}	PREZ	Q,QZ		0.5	1	2.4	0.5	1	2.2	ns/pF
Δt_{PHL}				0.5	1.3	3.2	0.6	1.3	2.8	
Δt_{PLH}	CLRZ	Q,QZ		0.5	1	2.2	0.5	1	2.1	ns/pF
Δt_{PHL}				0.6	1.3	3.5	0.7	1.3	3.1	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.
§ CLRZ does not apply for the DFY20LH.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

DTC10LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC74			SN74ASC74			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	CLK	Q,$\overline{Q}$	C_L = 0	1.5	3.2	8.4	1.6	3.2	7.5	ns
t_{PHL}				1.5	3.3	8.4	1.7	3.3	7.5	
t_{PLH}	CLRZ	$\overline{Q}$		2.4	4.9	12	2.6	4.9	10.6	ns
t_{PHL}		Q		2.2	4.5	10.6	2.4	4.5	9.4	
t_{PLH}	CLK	Q,$\overline{Q}$	C_L = 1 pF	2	4.2	10.6	2.1	4.2	9.5	ns
t_{PHL}				2.1	4.6	11.5	2.3	4.6	10.2	
t_{PLH}	CLRZ	$\overline{Q}$		2.9	5.9	14.1	3.1	5.9	12.6	ns
t_{PHL}		Q		2.9	6	14.3	3.1	6	12.7	
Δt_{PLH}	CLK	Q,$\overline{Q}$		0.5	1	2.4	0.5	1	2.2	ns/pF
Δt_{PHL}				0.5	1.3	3.3	0.6	1.3	2.9	
Δt_{PLH}	CLRZ	Q,$\overline{Q}$		0.4	1	2.2	0.5	1	2	ns/pF
Δt_{PHL}				0.7	1.5	3.7	0.7	1.5	3.3	

DTN10LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC74			SN74ASC74			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	CLK	Q,$\overline{Q}$	C_L = 0	1.5	3.2	8.1	1.6	3.2	7.2	ns
t_{PHL}				1.5	3.3	8.1	1.7	3.3	7.2	
t_{PLH}	CLK	Q,$\overline{Q}$	C_L = 1 pF	2	4.2	10.3	2.1	4.2	9.2	ns
t_{PHL}				2.1	4.6	11.1	2.3	4.6	9.8	
Δt_{PLH}	CLK	Q,$\overline{Q}$		0.4	1	2.4	0.5	1	2.2	ns/pF
Δt_{PHL}				0.5	1.3	3.3	0.6	1.3	2.9	

DTP10LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC74			SN74ASC74			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	CLK	Q,$\overline{Q}$	C_L = 0	1.5	3.2	7.2	1.6	3.2	6.5	ns
t_{PHL}				1.6	3.5	9.1	1.7	3.5	8.1	
t_{PLH}	PREZ	Q		2.4	4.9	11.7	2.6	4.9	10.4	ns
t_{PHL}		$\overline{Q}$		0.9	1.4	3	0.9	1.4	2.8	
t_{PLH}	CLK	Q,$\overline{Q}$	C_L = 1 pF	2	4.2	9.5	2.2	4.2	8.5	ns
t_{PHL}				2.2	4.8	12.3	2.3	4.8	10.8	
t_{PLH}	PREZ	Q		2.9	5.9	14.1	3.1	5.9	12.6	ns
t_{PHL}		$\overline{Q}$		1.5	2.7	6.2	1.6	2.7	5.5	
Δt_{PLH}	CLK	Q,$\overline{Q}$		0.5	1	2.5	0.5	1	2.3	ns/pF
Δt_{PHL}				0.5	1.3	3.2	0.6	1.3	2.8	
Δt_{PLH}	PREZ	Q,$\overline{Q}$		0.5	1	2.5	0.5	1	2.2	ns/pF
Δt_{PHL}				0.5	1.3	3.2	0.6	1.3	2.8	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

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DESIGN CONSIDERATIONS

interfacing the macro

Inputs and outputs of these dedicated macros are compatible for interfacing directly with cells and macros available in the TI standard cell library. The inputs can be driven by either noninverting or inverting input cells when interfacing off-chip for the input data. The outputs can be interfaced to drive off-chip loads with any of the noninverting output buffers or interfaced to external bidirectional buses through a three-state input/output TTL/CMOS buffer.

designing for testability

Designs employing storage or bistable elements should consider testability of the design in its final form. The need to preset or clear these elements should be assessed throughout the development of custom logic circuits with these considerations extended to the end-equipment application with respect to maintainability. Simple actions on the part of the ASIC designer can result in considerable cost savings allowing the expense of IC testing, system testing, and system maintenance to be reduced significantly.

power-up clear/preset

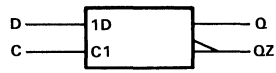
Standard cell storage elements containing the capability to be asynchronously either preset or cleared may be connected to an SN54ASC2320 or SN74ASC2320 power-up clear cell to achieve system initialization. Access to the clear or preset inputs from other system signals in conjunction with the power-up clear can be implemented with an AND gate.

D2939, AUGUST 1986

SystemCell™ 2-μm HARDWIRED MACRO CELL

- **Provides Complementary Q and QZ Outputs**
- **Choice Between Two Relative Output Drive Capabilities**
- **Implements Control/Status Registers**
- **Parallel Latches to Implement Wide Word Widths**

logic symbol



FUNCTION TABLE

INPUTS		OUTPUT	
D	C	Q	QZ
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}_0$

description

The SN54ASC75 and SN74ASC75 are dedicated, hard-wired standard-cell macros implementing D-type latches. The 'ASC75 latches offer two choices of individual latch configurations providing the custom IC designer storage elements to embed in ASICs in their most efficient form. The LAH20LH and LAH10LH latches implement identical function and sequential operation to one-fourth of the 'LS75 packaged latches, except that the 'ASC75 enable (C) input is individually available for custom design. The LAH20LH provides twice the drive capability as the LAH10LH element.

Information present at the data input is transferred to the Q output when the enable input is high, and the Q output will follow the data input as long as enable remains high. When enable goes low, the data that was present at the data input at the time the transition occurred is retained at the Q output until enable is taken high. The cells are designated and called from the engineering workstation input using the following cell names to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
LAH10LH	Label: LAHn0LH D,C,Q,QZ;	5
LAH20LH		4.5

The SN54ASC75 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC75 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

				LAH10LH	LAH20LH	UNIT
				MIN	MIN	
t_w	Pulse duration	C high		6	6	ns
		C low		4.8	4.8	
t_{su}	Setup time, D high or low			6	6	ns
t_h	Hold time, D high or low			0	0	ns

electrical characteristics

LAH10LH

PARAMETER			TEST CONDITIONS		SN54ASC75		SN74ASC75		UNIT
					TYP	MAX	TYP	MAX	
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX	V_I = V_{CC} or 0,		463		27.8	nA
C_i	Input capacitance	C	V_{CC} = 5 V,	T_A = 25°C	0.21		0.21		pF
		D			0.26		0.26		
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	2		2		pF

LAH20LH

PARAMETER			TEST CONDITIONS		SN54ASC75		SN74ASC75		UNIT
					TYP	MAX	TYP	MAX	
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C		2.2		2.2	V
I_{CC}	Supply current		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX	V_I = V_{CC} or 0,		528		31.7	nA
C_i	Input capacitance	C	V_{CC} = 5 V,	T_A = 25°C	0.22		0.22		pF
		D			0.25		0.25		
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	2.81		2.81		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

LAH10LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC75			SN74ASC75			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	C	Q	C_L = 0	1	2.1	4.8	1.1	2.1	4.3	ns
t_{PHL}				0.6	1.6	4	0.7	1.6	3.7	
t_{PLH}	C	QZ		0.9	2.1	5.1	1	2.1	4.6	ns
t_{PHL}				1.4	2.8	6.4	1.5	2.8	5.8	
t_{PLH}	D	Q		0.8	1.6	3.6	0.8	1.6	3.3	ns
t_{PHL}				1	1.6	3.6	1	1.6	3.3	
t_{PLH}	D	QZ		1.2	2.1	4.7	1.2	2.1	4.2	ns
t_{PHL}				1.1	2.3	5.3	1.1	2.3	4.7	
t_{PLH}	C	Q	C_L = 1 pF	1.5	3.1	7	1.7	3.1	6.3	ns
t_{PHL}				0.9	2.2	5.5	1	2.2	4.9	
t_{PLH}	C	QZ		1.4	3.1	7.4	1.5	3.1	6.7	ns
t_{PHL}				1.6	3.4	7.9	1.8	3.4	7	
t_{PLH}	D	Q		1.3	2.6	5.9	1.4	2.6	5.3	ns
t_{PHL}				1.2	2.2	5	1.3	2.2	4.5	
t_{PLH}	D	QZ		1.7	3.1	7	1.8	3.1	6.3	ns
t_{PHL}				1.3	2.9	6.8	1.4	2.9	6	
Δt_{PLH}	Any	Q,QZ		0.4	1	2.3	0.5	1	2.1	ns/pF
Δt_{PHL}				0.2	0.6	1.5	0.2	0.6	1.3	

LAH20LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC75			SN74ASC75			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	C	Q	C_L = 0	0.9	1.9	4.5	1	1.9	4	ns
t_{PHL}				0.6	1.7	4.1	0.7	1.7	3.7	
t_{PLH}	C	QZ		1	2.4	5.9	1.1	2.4	5.3	ns
t_{PHL}				1.3	2.8	6.6	1.4	2.8	5.9	
t_{PLH}	D	Q		0.7	1.5	3.5	0.8	1.5	3.2	ns
t_{PHL}				1	1.7	3.6	1.1	1.7	3.3	
t_{PLH}	D	QZ		1.3	2.4	5.4	1.4	2.4	4.9	ns
t_{PHL}				1.1	2.4	5.6	1.2	2.4	5	
t_{PLH}	C	Q	C_L = 1 pF	1.2	2.4	5.6	1.3	2.4	5.1	ns
t_{PHL}				0.8	2	5	0.9	2	4.5	
t_{PLH}	C	QZ		1.2	2.9	7	1.4	2.9	6.3	ns
t_{PHL}				1.4	3.1	7.4	1.6	3.1	6.7	
t_{PLH}	D	Q		1	2	4.6	1	2	4.2	ns
t_{PHL}				1.2	2	4.5	1.2	2	4.1	
t_{PLH}	D	QZ		1.6	2.9	6.5	1.7	2.9	5.9	ns
t_{PHL}				1.3	2.7	6.4	1.4	2.7	5.8	
Δt_{PLH}	Any	Q,QZ		0.2	0.5	1.2	0.2	0.5	1.1	ns/pF
Δt_{PHL}				0.1	0.3	0.9	0.1	0.3	0.8	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

interfacing the macro

Inputs and outputs of these dedicated macros are compatible for interfacing directly with cells and macros available in the TI standard cell library. The inputs can be driven by either noninverting or inverting input cells. The outputs can be interfaced to drive off-chip loads with any of the noninverting output buffers or interfaced to external bidirectional buses through a three-state input/output TTL/CMOS buffer.

designing for testability

Designers employing storage or bistable elements should consider testability of the design in its final form. The need to preset or clear these elements should be assessed throughout the development of custom logic circuits with these considerations extended to the end equipment application with respect to maintainability. Simple actions on the part of the ASIC designer can result in considerable cost savings, allowing the expense of IC testing, system testing, and system maintenance to be reduced significantly.

power-up clear/preset

Standard cell storage elements containing the capability to be asynchronously preset or cleared may be connected to the SN54ASC2320 or SN74ASC2320 power-up clear cell to achieve system initialization. Control of the clear or preset inputs from another system signal in conjunction with the power-up clear can be achieved with an AND gate.

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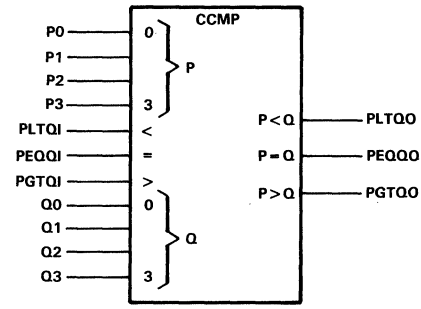
D2939, AUGUST 1986

SystemCell™ 2-μm SOFTWARE MACRO CELL

- **Performs Magnitude Comparison of Binary, BCD, and Monotonic Codes**
- **Weighted Cascading Inputs Accommodate Both Serial and Parallel Expansion**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The SN54ASC85 and SN74ASC85 are standard-cell software macros implementing 4-bit expandable magnitude comparators. The 4-bit configuration provides the custom IC designer a magnitude comparator to embed in ASICs in its most efficient form. The 'ASC85 implements a comparison scheme identical with that performed by packaged 'HC85, 'LS85 and 'F85 comparators.

These 4-bit magnitude comparators perform comparison of straight binary and straight BCD(8-4-2-1) codes. Three fully decoded decisions about two 4-bit words (P, Q) are made and are externally available at three outputs. These devices are fully expandable to any number of bits without external gates. Words of greater length may be compared by connecting comparators in cascade. The PGTQO, PLTQO, and PEQQO outputs of a stage handling less significant bits are connected to the corresponding PGTQI, PLTQI, and PEQQI inputs of the next stage handling more significant bits. The stage handling the least significant bits must have a high-level voltage applied to the PEQQI input. The cascading path of the 'ASC85 is implemented with only a two-gate-level delay to reduce overall comparison times for long words. The 'ASC85 is implemented with the standard cell functions indicated. The HDL netlist label for this software macro is shown on the last line of the following table:

CELL NAME	RELATIVE CELL AREA TO NA210LH	NO. USED	TOTAL RELATIVE CELL AREA	TOTAL C_{pd}‡ (pF)	MAXIMUM I_{CC} (nA)	
					SN54ASC'	SN74ASC'
AO221LH	2.7	4	10.8	2.36	896	53.6
IV120LH	1	3	3	1.32	315	18.96
NA210LH	1	6	6	3.06	786	47.04
NA310LH	1.25	2	2.5	1	326	19.56
NA410LH	1.5	2	3	1	374	22.4
NA510LH	1.75	7	12.25	3.64	1491	89.6
NA810LH	2.5	2	5	1.22	580	34.8
TOTALS		26	42.55	13.6	4768	286
S85LH Label: S85LH P3,P2,P1,P0,Q3,Q2,Q1,Q0,PGTQI,PLTQI,PEQQI,PGTQO,PLTQO,PEQQO;						

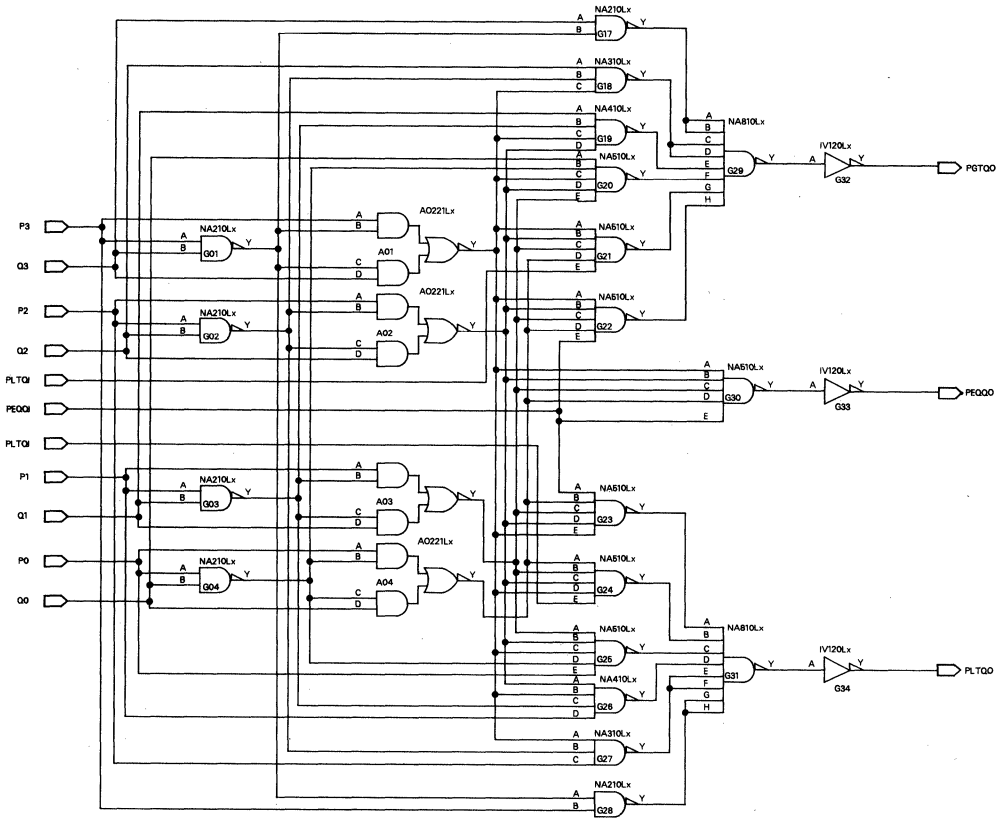
‡The equivalent power dissipation capacitance does not include interconnect capacitance.

The SN54ASC85 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC85 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
P3, Q3	P2, Q2	P1, Q1	P0, Q0	PGTQI	PLTQI	PEQQI	PGTQO	PLTQO	PEQQO
P3 > Q3	X	X	X	X	X	X	H	L	L
P3 < Q3	X	X	X	X	X	X	L	H	L
P3 = Q3	P2 > Q2	X	X	X	X	X	H	L	L
P3 = Q3	P2 < Q2	X	X	X	X	X	L	H	L
P3 = Q3	P2 = Q2	P1 > Q1	X	X	X	X	H	L	L
P3 = Q3	P2 = Q2	P1 < Q1	X	X	X	X	L	H	L
P3 = Q3	P2 = Q2	P1 = Q1	P0 > Q0	X	X	X	H	L	L
P3 = Q3	P2 = Q2	P1 = Q1	P0 < Q0	X	X	X	L	H	L
P3 = Q3	P2 = Q2	P1 = Q1	P0 = Q0	H	L	L	H	L	L
P3 = Q3	P2 = Q2	P1 = Q1	P0 = Q0	L	H	L	L	H	L
P3 = Q3	P2 = Q2	P1 = Q1	P0 = Q0	X	X	H	L	L	H
P3 = Q3	P2 = Q2	P1 = Q1	P0 = Q0	H	H	L	L	L	L
P3 = Q3	P2 = Q2	P1 = Q1	P0 = Q0	L	L	L	H	H	L

logic diagram



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absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER		TEST CONDITIONS	SN54ASC85		SN74ASC85		UNIT
			TYP	MAX	TYP	MAX	
V_T Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC} Supply current		V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN or MAX		4768		286	nA
C_i Input capacitance	PEQQI	V_{CC} = 5 V, T_A = 25°C	0.36		0.36		pF
	PQTQI, PLTQI		0.12		0.12		
	All others		0.37		0.37		
C_{pd} Equivalent power dissipation capacitance‡		V_{CC} = 5 V, T_A = 25°C, t_r = t_f = 3 ns,	13.6		13.6		pF

† The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted) (see Note 1)

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC85			SN74ASC85			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
t_{pd}	Pn, Qn	PGTQO, PLTQO	C_L = 0		12	28		12	25.1	ns
t_{pd}	Pn, Qn	PEQQO			9	21.5		9	19.5	ns
t_{pd}	PLTQI, PEQQI	PGTQO			6	15.9		6	14	ns
t_{pd}	PGTQI, PEQQI	PLTQO			5.5	13.2		5.5	11.7	ns
t_{pd}	PEQQI	PEQQO			3	7.6		3	6.6	ns
Δt_{pd}	Any	Any		0.3	0.5	1.1	0.3	0.5	1	ns/pF

‡ Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{pd} ≡ propagation delay time, low-to-high or high-to-low output
Δt_{pd} ≡ change in t_{pd} with capacitance
§ Typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: These switching characteristics are simulations of the software macro cell using interconnect capacitance values for an array design having 2,000 gates. Post-layout simulation uses actual interconnect capacitance values.

DESIGN CONSIDERATIONS

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

The HDL for this software macro is included as a part of the library supplied for supported engineering workstations so that a single label can be developed to apply the macro as needed. The following printout of the HDL block definition is furnished for reference.

HDL FILE

```
BLOCK S85LH;
P3          @INPUT;
P2          @INPUT;
P1          @INPUT;
P0          @INPUT;
Q3          @INPUT;
Q2          @INPUT;
Q1          @INPUT;
Q0          @INPUT;
PGTQI       @INPUT;
PLTQI       @INPUT;
PEQQI       @INPUT;
PGTQO       @OUTPUT;
PLTQO       @OUTPUT;
PEQQO       @OUTPUT;

STRUCTURE
AO1         :AO221LH        P3,G1O,G1O,Q3,AO1O;
AO2         :AO221LH        P2,G2O,G2O,Q2,AO2O;
AO3         :AO221LH        P1,G3O,G3O,Q1,AO3O;
AO4         :AO221LH        P0,G4O,G4O,Q0,AO4O;
G01         :NA210LH        P3,Q3,G1O;
G02         :NA210LH        P2,Q2,G2O;
G03         :NA210LH        P1,Q1,G3O;
GO4         :NA210LH        P0,Q0,G4O;
G17         :NA210LH        Q3,G1O,G17O;
G18         :NA310LH        Q2,G2O,AO1O,G18O;
G19         :NA410LH        Q1,G3O,AO1O,AO2O,G19O;
G20         :NA510LH        Q0,G4O,AO1O,AO2O,AO3O,G20O;
G21         :NA510LH        AO1O,AO2O,AO3O,AO4O,PLTQI,G21O;
G22         :NA510LH        AO1O,AO2O,AO3O,AO4O,PEQQI,G22O;
G23         :NA510LH        PEQQI,AO4O,AO3O,AO2O,AO1O,G23O;
G24         :NA510LH        AO4O,AO3O,AO2O,AO1O,PGTQI,G24O;
G25         :NA510LH        AO3O,AO2O,AO1O,G4O,P0,G25O;
G26         :NA410LH        AO2O,AO1O,G3O,P1,G26O;
G27         :NA310LH        AO1O,G2O,P2,G27O;
G28         :NA210LH        G1O,P3,G28O;
G29         :NA810LH        G17O,G17O,G18O,G18O,G19O,G20O,G21O,G22O,G29O;
G30         :NA510LH        AO1O,AO2O,AO3O,AO4O,PEQQI,G30O;
G31         :NA810LH        G23O,G24O,G25O,G26O,G27O,G27O,G28O,G28O,G31O;
G32         :IV120LH        G29O,PGTQO;
G33         :IV120LH        G30O,PEQQO;
G34         :IV120LH        G31O,PLTQO;
END S85LH;
```


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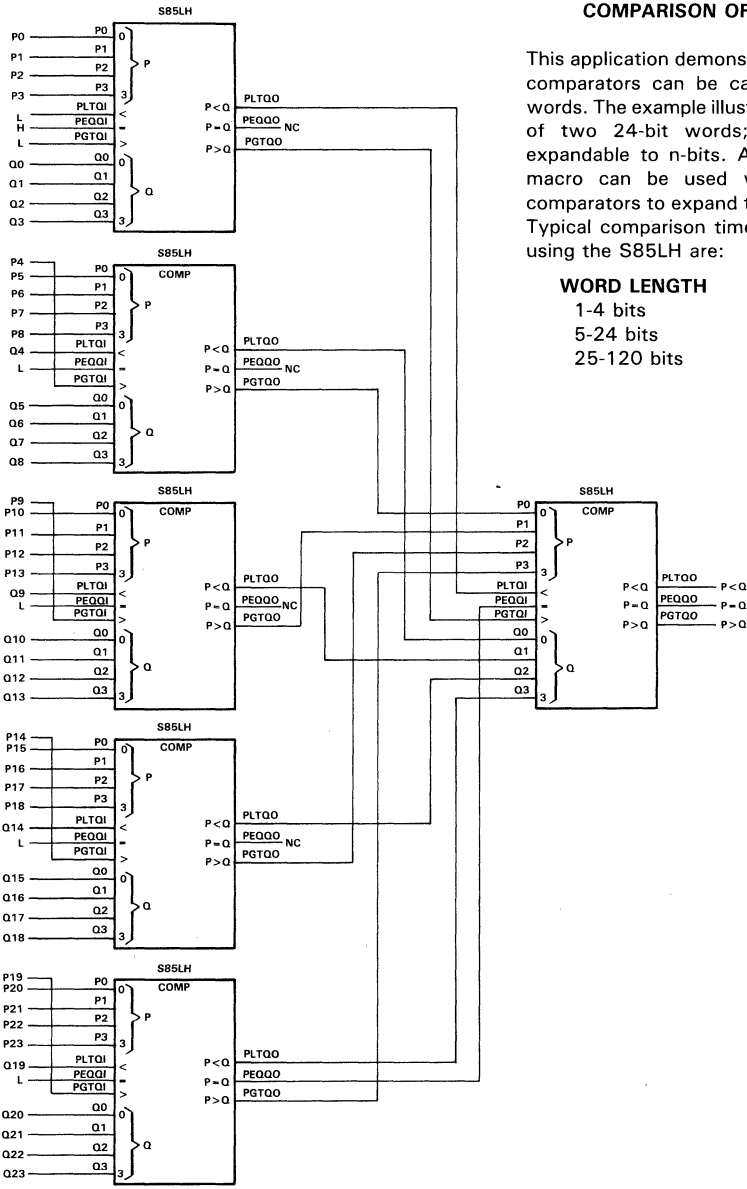
TYPICAL APPLICATION INFORMATION

COMPARISON OF TWO N-BIT WORDS

This application demonstrates how these magnitude comparators can be cascaded to compare longer words. The example illustrated shows the comparison of two 24-bit words; however, the design is expandable to n-bits. As an example, one S85LH macro can be used with five of these 24-bit comparators to expand the word length to 120-bits. Typical comparison times for various word lengths using the S85LH are:

WORD LENGTH	TYPICAL COMPARE TIME
1-4 bits	12.5 ns
5-24 bits	25.0 ns
25-120 bits	37.5 ns



H = To high output of tie-off cell, L = To low output of tie-off cell, NC = no connection.

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SystemCell™ 2-μm INTERNAL STANDARD CELL

- **Choice of Three Performance Levels**
- **Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V**
- **Functional Operation Over V_{CC} Range of 2 V to 6 V**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

positive logic equations

$$Y = A \oplus B = \overline{A}B + A\overline{B}$$

description

The SN54ASC86 and SN74ASC86 are 2-input exclusive-OR gate CMOS standard cells each implementing the equivalent of one-fourth of an SN54LS86 or SN74LS86 device. The standard-cell library contains three physical implementations to provide the custom IC designer a choice between three performance levels for optimizing designs. Each option is designated and called from the engineering workstation input using the following cell names to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		TYPICAL DELAY C_L = 1 pF	RELATIVE CELL AREA TO NA210LH
EX210LH	Label: EX2n0LH A,B,Y;	2.3 ns	2
EX220LH		2 ns	2.25
EX240LH		2 ns	2.5

The SN54ASC86 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC86 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS	EX210LH TYP	EX210LH MAX	EX220LH TYP	EX220LH MAX	EX240LH TYP	EX240LH MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		2.2		V
I_{CC}	Supply current	SN54ASC86	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0,		218		252		287	nA
		SN74ASC86	T_A = MIN to MAX		13.1		15.1		17.2	
C_i	Input capacitance		V_{CC} = 5 V, T_A = 25°C	0.19		0.19		0.19		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, t_r = t_f = 3 ns, T_A = 25°C	1		1.35		2.55		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

EX210LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC86			SN74ASC86			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A or B	Y	C_L = 0	0.8	1.3	2.5	0.8	1.3	2.3	ns
t_{PHL}				0.5	1.3	3.2	0.5	1.3	2.9	
t_{PLH}	A or B	Y	C_L = 1 pF	1.3	2.3	4.8	1.4	2.3	4.4	ns
t_{PHL}				1	2.3	6	1.1	2.3	5.4	
Δt_{PLH}	A or B	Y		0.5	1	2.3	0.5	1	2.1	ns/pF
Δt_{PHL}				0.5	1	2.9	0.5	1	2.5	

EX220LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC86			SN74ASC86			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A or B	Y	C_L = 0	0.7	1.4	2.7	0.8	1.4	2.5	ns
t_{PHL}				0.5	1.4	3.2	0.5	1.4	2.9	
t_{PLH}	A or B	Y	C_L = 1 pF	1	1.9	3.8	1.1	1.9	3.5	ns
t_{PHL}				0.8	2.1	5	0.9	2.1	4.5	
Δt_{PLH}	A or B	Y		0.3	0.5	1.2	0.3	0.5	1.1	ns/pF
Δt_{PHL}				0.3	0.7	1.9	0.3	0.7	1.7	

EX240LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC86			SN74ASC86			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A or B	Y	C_L = 0	0.8	1.6	3.2	0.9	1.6	2.9	ns
t_{PHL}				0.5	1.6	3.8	0.6	1.6	3.5	
t_{PLH}	A or B	Y	C_L = 1 pF	1	1.9	3.8	1.1	1.9	3.5	ns
t_{PHL}				0.7	2	5	0.8	2	4.4	
Δt_{PLH}	A or B	Y		0.1	0.3	0.7	0.1	0.3	0.6	ns/pF
Δt_{PHL}				0.2	0.4	1.2	0.2	0.4	1.1	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to Section 7.

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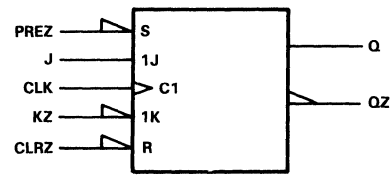
SystemCell™ 2-μm HARDWIRED MACRO CELL

- **Provides Complementary Q and QZ Outputs**
- **Positive-Edge Triggered with J and KZ Data Inputs**
- **CLRZ and PREZ Inputs Provide Asynchronous Initialization**
- **J and KZ Inputs Simplify Implementation of Toggle Flip-Flops**

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The SN54ASC109 and SN74ASC109 are dedicated, hardwired, standard-cell macros implementing positive-edge-triggered flip-flops. A low level at the PREZ or CLRZ input controls the state of the outputs regardless of the levels of the other inputs. When PREZ AND CLRZ are inactive (high), data at the J and KZ inputs meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock transition. Following the hold time interval, data at the J and KZ inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as D-type flip-flops if J and KZ are tied together. The JK20LH flip-flop implements the function and sequential operation identical to one-half of the 'LS109, 'S109, or 'F109 packaged flip-flops. The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		MAXIMUM CLOCK FREQUENCY	RELATIVE CELL AREA TO NA210LH
JKB20LH	Label: JKB20LH CLRZ,PREZ,J,KZ,CLK,Q,QZ;	44.2 MHz	10

The SN54ASC109 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC109 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

INPUTS					OUTPUTS	
PREZ	CLRZ	CLK	J	KZ	Q	QZ
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H‡	H‡
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q_0	$\overline{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$

‡This configuration is nonstable; that is, it will not persist when PREZ or CLRZ return to their inactive (high) level.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			MIN	MAX	UNIT
f_{max}	Clock frequency		0	44.2	MHz
t_w	Pulse duration	CLRZ low	9		ns
		PREZ low	9		
		CK High	11.4		
		CK low	11.4		
t_{su}	Setup time	CLRZ inactive	1.8		ns
		PREZ inactive	−0.4		
t_h	Hold time	J or KZ low	9		ns
		CLRZ low	3		
		PREZ low	9.6		
		J or KZ high or low	0		

electrical characteristics

PARAMETER			TEST CONDITIONS	SN54ASC019 TYP	SN54ASC019 MAX	SN74ASC019 TYP	SN74ASC019 MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current		V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		1181		70.9	nA
C_i	Input capacitance	PREZ or CLRZ	V_{CC} = 5 V, T_A = 25°C	0.25		0.25		pF
		J		0.12		0.12		
		KZ		0.13		0.13		
		CLK		0.13		0.13		
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C, t_r = t_f = 3 ns,	4.81		4.81		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC109 MIN	SN54ASC109 TYP‡	SN54ASC109 MAX	SN74ASC109 MIN	SN74ASC109 TYP‡	SN74ASC109 MAX	UNIT
t_{PLH}	CLK	Q,QZ	C_L = 0	1.8	5	13.5	2	5	11.9	ns
t_{PHL}				1.9	4.5	12.2	2.1	4.5	10.9	
t_{PLH}	PREZ,CLRZ	Q,QZ		2	4.2	11	2.2	4.2	9.8	ns
t_{PHL}				1.1	2.2	5.2	1.2	2.2	4.7	
t_{PLH}	CLK	Q,QZ	C_L = 1 pF	2.1	5.5	14.6	2.3	5.5	13	ns
t_{PHL}				2.1	4.9	13.1	2.2	4.9	11.7	
t_{PLH}	PREZ,CLRZ	Q,QZ		2.3	4.7	12.2	2.5	4.7	10.9	ns
t_{PHL}				1.3	2.6	6.4	1.4	2.6	5.8	
Δt_{PLH}	Any	Q,QZ		0.2	0.5	1.3	0.2	0.5	1.2	ns/pF
Δt_{PHL}				0.1	0.4	1.2	0.1	0.4	1.1	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

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DESIGN CONSIDERATIONS

interfacing the macro

Inputs and outputs of these dedicated macros are compatible for interfacing directly with cells and macros available in the TI standard cell library. The inputs can be driven by either noninverting or inverting input cells. The outputs can be interfaced to drive off-chip loads with any of the noninverting output buffers or interfaced to external bidirectional buses through a 3-state input/output TTL/CMOS buffer.

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

designing for testability

Designs employing storage or bistable elements should consider testability of the design in its final form. The need to preset or clear these elements should be assessed throughout the development of custom logic circuits with these considerations extended to the end equipment application with respect to maintainability. Simple actions on the part of the ASIC designer can result in considerable cost savings, allowing the expense of IC testing, system testing, and system maintenance to be reduced significantly.

power-up clear/preset

Standard cell storage elements containing the capability to be asynchronously preset or cleared may be connected to the SN54ASC109 or SN74ASC109 power-up clear cell to achieve system initialization. Control of the clear or preset inputs from another system signal in conjunction with the power-up clear can be achieved with an AND gate.

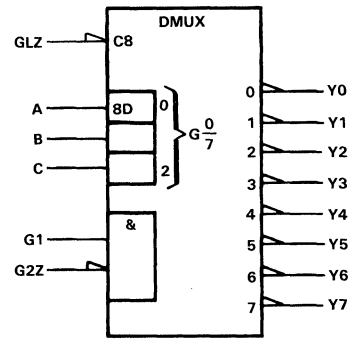
SystemCell™ 2-μm SOFTWARE MACRO CELL

- **Latched Address Lines Ensure Stable Bus Interfaces**
- **Expandable Select Width**
- **Parallel Decoders for Multiple-Bit Words**

description

The SN54ASC137 and SN74ASC137 are standard-cell software macros implementing a 3-line to 8-line decoder/demultiplexer. The 'ASC137 incorporates a 3-bit latch on the three address inputs to simplify system design, as the data selected is stored and is available until replaced by another selection. The 'ASC137 implements the full function table identical with that performed by packaged ICs such as the 'LS137.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

When the latch-enable input (GLZ) is low, the 'ASC137 acts as a decoder/demultiplexer. When GLZ goes from low to high, the address present at the select inputs (A, B, and C) is stored in the latches. Further address changes are ignored as long as GLZ remains high. This latching capability makes the 'ASC137 ideally suited for implementing stable decoders for strobed (stored-address) applications in bus-oriented systems.

Also provided in the macro are output controls, G1 and G2Z, that enable and disable the outputs when G1 is low or G2Z is high. When enabled (G1 high and G2Z low), the selected output is low. These enables permit the 'ASC137 to be cascaded to accommodate wider multiplexers, as only the enabled 8-bit field will contain an active data bit. The 'ASC137 is implemented with standard cell functions indicated. The HDL netlist label for this software macro is shown on the last line of the following table:

CELL NAME	RELATIVE CELL AREA TO NA210LH	NO. USED	TOTAL RELATIVE CELL AREA	TOTAL C_{pd}‡ (pF)	MAXIMUM I_{CC} (nA)	
					SN54ASC'	SN74ASC'
IV110LH	0.75	5	3.75	2.2	525	31.6
AN210LH	1.5	6	9	5.4	1164	69.6
NO210LH	1	7	7	2.31	896	54
NA420LH	2.5	8	20	7.68	290	149.6
TOTALS		26	39.75	17.59	2875	305
Label: S137LH C,B,A,GLZ,G2Z,G1,Y0,Y1,Y2,Y3,Y4,Y5,Y6,Y6;						

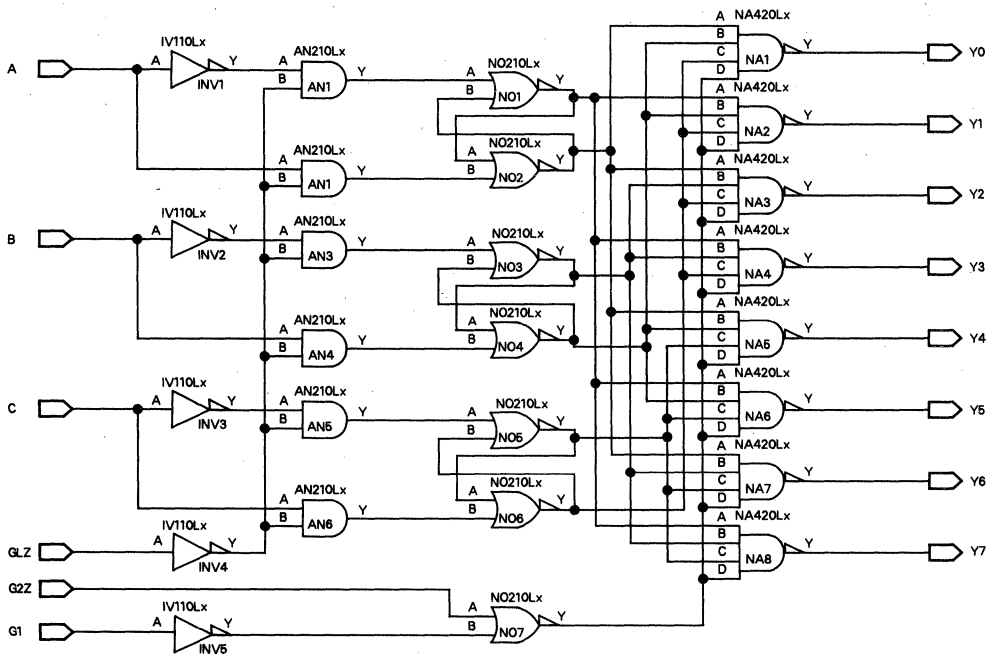
‡The equivalent power dissipation capacitance does not include interconnect capacitance.

The SN54ASC137 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC137 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT										
GLZ	G1	G2Z	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	H	H	L
H	H	L	X	X	X	Output corresponding to stored address = L All others = H							

logic diagram



Lx = LH

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absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS	SN54ASC137		SN74ASC137		UNIT
				TYP	MAX	TYP	MAX	
V_T	Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current		V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		2875		305	nA
C_i	Input capacitance	A,B,C	V_{CC} = 5 V, T_A = 25°C	0.25		0.25		pF
		GLZ,G1		0.12		0.12		
		G2Z		0.11		0.11		
C_{pd}	Equivalent power dissipation capacitance†		V_{CC} = 5 V, t_r = t_f = 3 ns,	17.59		17.59		pF

† The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 1)

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC137			SN74ASC137			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
t_{pd}	A,B,C,GLZ	Any	C_L = 0		12	25.8		12	23.3	ns
t_{pd}	G1 or G2Z	Any			5	12.3		5	11.3	ns
Δt_{pd}	Any	Any		0.3	0.7	2.3	0.3	0.7	2	ns/pF

‡ Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{pd} ≡ propagation delay time, low-to-high-level or high-to-low-level output
Δt_{pd} ≡ change in t_{pd} with load capacitance
§ Typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: These switching characteristics are simulations of the software macro cell using interconnect capacitance values for an array design having 2,000 gates. Post-layout simulation uses actual interconnect capacitance values.

DESIGN CONSIDERATIONS

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design.

The HDL for this software macro is included as a part of the library supplied for supported engineering workstations so that a single label can be developed to apply the macro as needed. The following printout of the HDL block definition is furnished for a reference.

HDL FILE

```
BLOCK S137LH;
C               @INPUT;
B               @INPUT;
A               @INPUT;
GLZ             @INPUT;
G2Z             @INPUT;
G1              @INPUT;
Y0              @OUTPUT;
Y1              @OUTPUT;
Y2              @OUTPUT;
Y3              @OUTPUT;
Y4              @OUTPUT;
Y5              @OUTPUT;
Y6              @OUTPUT;
Y7              @OUTPUT;

STRUCTURE
AN1             :AN210LH        AN,GLP,LIAP;
AN2             :AN210LH        A,GLP,LIAN;
AN3             :AN210LH        BN,GLP,LIBP;
AN4             :AN210LH        B,GLP,LIBN;
AN5             :AN210LH        CN,GLP,LICP;
AN6             :AN210LH        C,GLP,LICN;
INV1            :IV110LH        A,AN;
INV2            :IV110LH        B,BN;
INV3            :IV110LH        C,CN;
INV4            :IV110LH        GLZ,GLP;
INV5            :IV110LH        G1,IV5O;
NA1             :NA420LH        LOAD,LOBN,LOCN,OC,Y0;
NA2             :NA420LH        LOAP,LOBN,LOCN,OC,Y1;
NA3             :NA420LH        LOAN,LOBP,LOCN,OC,Y2;
NA4             :NA420LH        LOAP,LOBP,LOCN,OC,Y3;
NA5             :NA420LH        LOAN,LOBN,LOCP,OC,Y4;
NA6             :NA420LH        LOAP,LOBN,LOCP,OC,Y5;
NA7             :NA420LH        LOAN,LOBP,LOCP,OC,Y6;
NA8             :NA420LH        LOAP,LOBP,LOCP,OC,Y7;
NO1             :NO210LH        LIAP,LOAN,LOAP;
NO2             :NO210LH        LOAP,LIAN,LOAN;
NO3             :NO210LH        LIBP,LOBN,LOBP;
NO4             :NO210LH        LOBP,LIBN,LOBN;
NO5             :NO210LH        LICP,LOCN,LOCP;
NO6             :NO210LH        LOCP,LICN,LOCN;
NO7             :NO210LH        G2Z,IV5O,OC;
END S137LH;
```


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Dedicated 2-line to 4-line decoder cells ('ASC2350) are also available in the standard cell library for implementing small data-path decoders. Two predesigned cells, designated as the DE210LH and the DE212LH, are offered. The DE212LH cell incorporates an enable input that can be used for expanding the word width. Latch cells can be added at the select inputs to facilitate storage. These hardwired cells should be considered if the decoder is in a critical path, as their performance is predetermined as specified in their switching characteristics.

interfacing the macro

Inputs and outputs of the predesigned macro are compatible for interfacing directly with cells and macros available in the TI standard cell library.

The inputs can be driven by either inverting or noninverting input cells. The outputs can be interfaced to drive off-chip loads with any of the noninverting output buffers or interfaced to external bidirectional buses through a 3-state input/output TTL/CMOS buffer.

D2939, AUGUST 1986

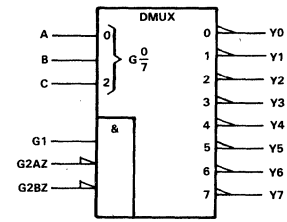
SystemCell™ 2-μm SOFTWARE MACRO CELL

- **Three Enable Inputs for Expandability**
- **Choice of an Active-High or Two Active-Low Enables**
- **Parallel Decoders for Multiple-Bit Words**

description

The SN54ASC138 and SN74ASC138 are standard-cell software macros implementing a 3-line to 8-line decoder/demultiplexer. The 'ASC138 implements the full function table identical with that performed by packaged ICs such as the 'LS138, 'S138, and 'F138.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Also provided in the macro are strobe inputs G1, G2AZ, and G2BZ, which enable and disable the inputs. All of the outputs are high, disabled, unless G1 is high and unless G2AZ and G2BZ are low, enabling the outputs. When enabled the selected output assumes a low-logic level. These strobes also permit the 'ASC138 to be cascaded to accommodate wider multiplexers, as only the enabled 8-bit field will contain an active data bit. The 'ASC138 is implemented with the standard cell functions indicated. The HDL netlist label for this software macro is shown on the last line of the following table:

CELL NAME	RELATIVE CELL AREA TO NA210LH	NO. USED	TOTAL RELATIVE CELL AREA	TOTAL C_{pd}‡ (pF)	MAXIMUM I_{CC} (nA)	
					SN54ASC'	SN74ASC'
IV110LH	0.75	1	1	0.44	105	6.32
IV120LH	1	6	6	4.8	786	47.1
NO330LH	2.75	1	2.75	0.85	312	18.7
NA420LH	2.5	8	20	7.68	2496	149.6
TOTALS		16	29.75	13.77	3699	222
Label: S138LH G1,G2AZ,G2BZ,A,B,C,Y0,Y1,Y2,Y3,Y4,Y5,Y6,Y7;						

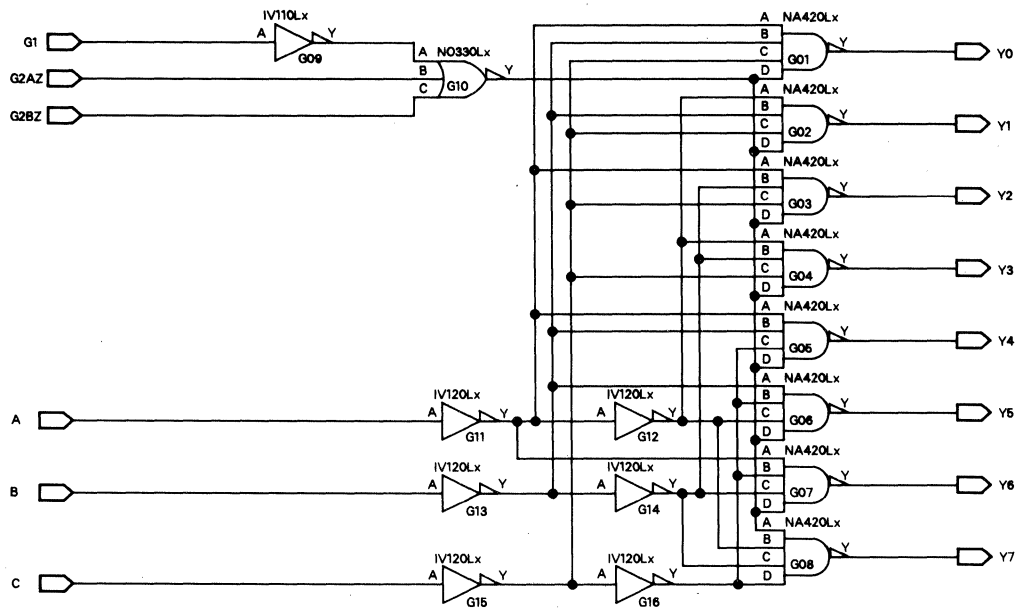
‡The equivalent power dissipation capacitance does not include interconnect capacitance.

The SN54ASC138 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC138 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT										
G1	G2AZ	G2BZ	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

logic diagram (positive logic)



Lx = LH for 2-μm standard cells.

TEXAS INSTRUMENTS
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absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS	SN54ASC138		SN74ASC138		UNIT
				TYP	MAX	TYP	MAX	
V_T	Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current		V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		3699		222	nA
C_i	Input capacitance	A,B,C	V_{CC} = 5 V, T_A = 25°C	0.24		0.24		pF
		G1		0.12		0.12		
		G2AZ,G2BZ		0.35		0.35		
C_{pd}	Equivalent power dissipation capacitance†		V_{CC} = 5 V, T_A = 25°C, t_r = t_f = 3 ns,	13.8		13.8		pF

† The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 1)

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC138			SN74ASC138			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
t_{pd}	A,B,C	Any	C_L = 0		4	8.1		4	7.5	ns
t_{pd}	G1, G2AZ, or G2BZ	Any			7	13.2		7	12.2	ns
Δt_{pd}	Any	Any		0.3	0.7	2.3	0.3	0.7	2	ns/pF

‡ Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{pd} ≡ propagation delay time, low-to-high-level or high-to-low-level output
Δt_{pd} ≡ change in t_{pd} with load capacitance
§ Typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: These switching characteristics are simulations of the software macro cell using interconnect capacitance values for an array design having 2,000 gates. Post-layout simulation uses actual interconnect capacitance values.

DESIGN CONSIDERATIONS

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

The HDL for this software macro is included as a part of the library supplied for supported engineering workstations so that a single label can be developed to apply the macro as needed. The following printout of the HDL block definition is furnished for reference.

HDL FILE

```
BLOCK S138LH;
G1          @INPUT;
G2AZ        @INPUT;
G2BZ        @INPUT;
A           @INPUT;
B           @INPUT;
C           @INPUT;
Y0          @OUTPUT;
Y1          @OUTPUT;
Y2          @OUTPUT;
Y3          @OUTPUT;
Y4          @OUTPUT;
Y5          @OUTPUT;
Y6          @OUTPUT;
Y7          @OUTPUT;

STRUCTURE
G01         :NA420LH        G11O,G13O,G15O,G10O,Y0;
G02         :NA420LH        G12O,G13O,G15O,G10O,Y1;
G03         :NA420LH        G11O,G14O,G15O,G10O,Y2;
G04         :NA420LH        G12O,G14O,G15O,G10O,Y3;
G05         :NA420LH        G11O,G13O,G16O,G10O,Y4;
G06         :NA420LH        G13O,G16O,G12O,G10O,Y5;
G07         :NA420LH        G11O,G16O,G14O,G10O,Y6;
G08         :NA420LH        G10O,G12O,G14O,G16O,Y7;
G09         :IV110LH        G1,G09O;
G10         :NO330LH        G09O,G2AZ,G2BZ,G10O;
G11         :IV120LH        A,G11O;
G12         :IV120LH        G11O,G12O;
G13         :IV120LH        B,G13O;
G14         :IV120LH        G13O,G14O;
G15         :IV120LH        C,G15O;
G16         :IV120LH        G15O,G16O;
END S138LH:
```

Dedicated 2-line to 4-line decoder cells ('ASC2350) are also available in the standard cell library for implementing small, data-path decoders. Two predesigned cells, designated as the DE210LH and the DE212LH, are offered. The DE212LH cell incorporates an enable input that can be used for expanding the word width. Latch cells can be added at the select inputs to implement storage. These hardwired cells should be considered if the decoder is in a critical path, as their performance is predetermined as specified in their switching characteristics.

interfacing the macro

Inputs and outputs of the predesigned macro are compatible for interfacing directly with cells and macros available in the TI standard cell library.

The inputs can be driven by either inverting or noninverting input cells. The outputs can be interfaced to drive off-chip loads with any of the noninverting output buffers or interfaced to external bidirectional buses through a 3-state input/output TTL/CMOS buffer.

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D2939, AUGUST 1986

SystemCell™ 2-μm SOFTWARE MACRO CELL

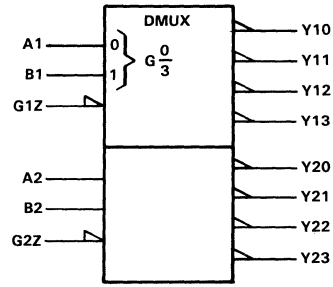
- **Enable Input Permits Expansion of Each Decoder**
- **Parallel Decoders for Multiple Bit Words**

description

The SN54ASC139 and SN74ASC139 are standard-cell software macros implementing dual 2-line to 4-line decoders/demultiplexers. The 'ASC139 implements the full function table identical with that performed by packaged ICs such as the 'LS139A, 'S139, and 'F139.

Also provided in the macro are two strobe inputs G1Z and G2Z that enable and disable the outputs. The four outputs of a decoder are high when its corresponding strobe is high. When the strobe is low, the selected output is low. These strobes, G1Z for decoder 1 and G2Z for decoder 2, permit the 'ASC139 decoders to be cascaded to accommodate wider multiplexers, as only the enabled 4-bit field will contain an active data bit. The 'ASC139 is implemented with the standard cell functions indicated. The HDL netlist label for this software macro is shown on the last line of the following table:

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

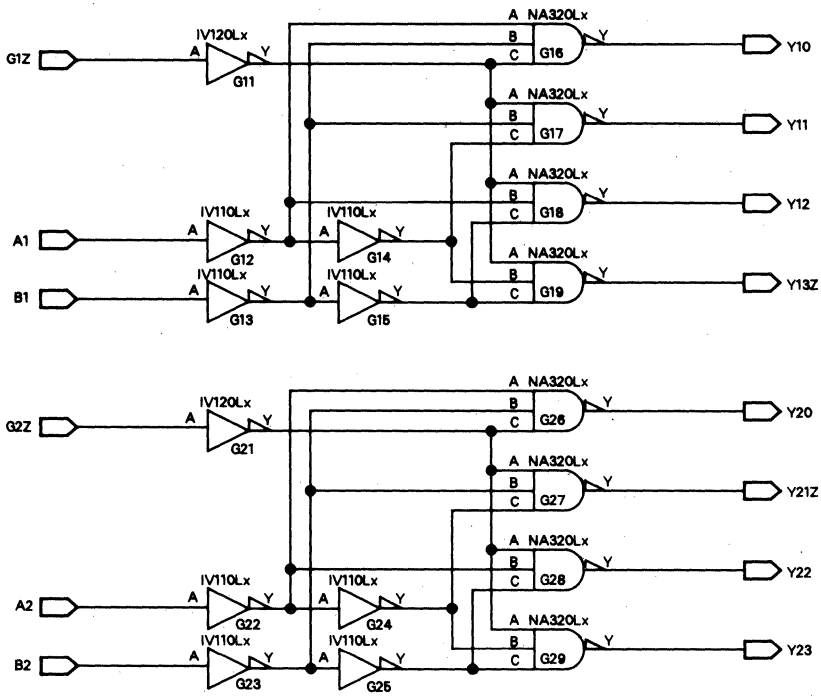
CELL NAME	RELATIVE CELL AREA TO NA210LH	NO. USED	TOTAL RELATIVE CELL AREA	TOTAL C_{pd}‡ (pF)	MAXIMUM I_{CC} (nA)	
					SN54ASC'	SN74ASC'
IV110LH	0.75	8	6	3.52	840	50.56
IV120LH	1	2	2	1.6	262	15.7
NA320LH	2	8	16	7.52	2040	122.4
TOTALS		18	24	12.64	3142	189
Label: S139LH A1,B1,G1Z,A2,B2,G2Z,Y10,Y11,Y12,Y13,Y20,Y21,Y22,Y23;						

‡The equivalent power dissipation capacitance does not include interconnect capacitance.

The SN54ASC139 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC139 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

INPUTS			OUTPUTS			
ENABLE	SELECT					
GnZ	Bn	An	Yn0	Yn1	Yn2	Yn3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L



TEXAS INSTRUMENTS
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absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS	SN54ASC139		SN74ASC139		UNIT
				TYP	MAX	TYP	MAX	
V_T	Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current		V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		3142		189	nA
C_i	Input capacitance	An,Bn	V_{CC} = 5 V, T_A = 25°C	0.12		0.12		pF
		GnZ		0.24		0.24		
C_{pd}	Equivalent power dissipation capacitance†		V_{CC} = 5 V, t_r = t_f = 3 ns,	12.64		12.64		pF

† The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted) (see Note 1)

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC139			SN74ASC139			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
t_{pd}	An or Bn	Any	C_L = 0		4	8.1		4	7.5	ns
t_{pd}	GnZ	Any			3	5.2		3	4.8	ns
Δt_{pd}	Any	Any		0.3	0.6	1.8	0.3	0.6	1.5	ns/pF

‡ Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{pd} ≡ propagation delay time, low-to-high or high-to-low-level output
Δt_{pd} ≡ change in t_{pd} with load capacitance
§ Typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: These switching characteristics are simulations of the software macro cell using interconnect capacitance values for an array design having 2,000 gates. Post-layout simulation uses actual interconnect capacitance values.

DESIGN CONSIDERATIONS

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design.

The HDL for this soft macro is included as a part of the library supplied for supported engineering workstations so that a single label can be developed to apply the macro as needed. The following printout of the HDL block definition is furnished for reference.

HDL FILE

```
BLOCK S139LH;
A1          @INPUT;
B1          @INPUT;
G1Z         @INPUT;
A2          @INPUT;
B2          @INPUT;
G2Z         @INPUT;
Y10         @OUTPUT;
Y11         @OUTPUT;
Y12         @OUTPUT;
Y13         @OUTPUT;
Y20         @OUTPUT;
Y21         @OUTPUT;
Y22         @OUTPUT;
Y23         @OUTPUT;

STRUCTURE
G11         :IV120LH        G1Z,G11O;
G12         :IV110LH        A1,G12O;
G13         :IV110LH        B1,G13O;
G14         :IV110LH        G12O,G14O;
G15         :IV110LH        G13O,G15O;
G16         :NA320LH        G12O,G13O,G11O,Y10;
G17         :NA320LH        G11O,G13O,G14O,Y11;
G18         :NA320LH        G11O,G12O,G15O,Y12;
G19         :NA320LH        G11O,G14O,G15O,Y13;
G21         :IV120LH        G2Z,G21O;
G22         :IV110LH        A2,G22O;
G23         :IV110LH        B2,G23O;
G24         :IV110LH        G22O,G24O;
G25         :IV110LH        G23O,G25O;
G26         :NA320LH        G22O,G23O,G21O,Y2O;
G27         :NA320LH        G21O,G23O,G24O,Y21;
G28         :NA320LH        G21O,G22O,G25O,Y22;
G29         :NA320LH        G21O,G24O,G25O,Y23;
END S139LH;
```

Dedicated 2-line to 4-line decoder cells ('ASC2350) are also available in the standard cell library for implementing small, data-path decoders. Two predesigned cells, designated as the DE210LH and the DE212LH, are offered. The DE212LH cell incorporates an enable input that can be used for expanding the word width. Latch cells can be added at the select inputs to facilitate storage. These hard-wired cells should be considered if the decoder is in a critical path, as their performance is predetermined as specified in their switching characteristics.

interfacing the macro

Inputs and outputs of the predesigned macro are compatible for interfacing directly with cells and macros available in the TI standard cell library.

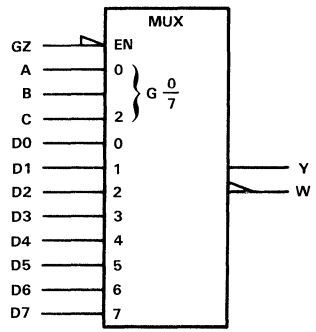
The inputs can be driven by either noninverting or inverting input cells when interfacing off-chip for the input data words. The outputs can be interfaced to drive off-chip loads with any of the noninverting output buffers or interfaced to external bidirectional buses through a 3-state input/output TTL/CMOS buffer.

D2939, AUGUST 1986

SystemCell™ 2-μm SOFTWARE MACRO CELL

- **Active-Low Strobe for Expandability**
- **Use Parallel Multiplexers for Multiple-Bit Words**

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The SN54ASC151 and SN74ASC151 are standard-cell software macros implementing 8-line to 1-line multiplexers. The 'ASC151 implements a function table identical with that performed by packaged 'HC151, 'LS151, 'S151, and 'F151 multiplexers.

The macro has a strobe input, GZ, that enables and disables the inputs. The Y output is low and the W output is high when GZ is high. When GZ is low, the Y output assumes the level of the selected input and the W output assumes the complement of that level. This strobe permits the macro to be employed for designing wider multiplexers, as only the enabled 8-bit field will output an active data bit. The 'ASC151 is implemented with standard cell functions indicated. The HDL netlist label for this software macro is shown on the last line of the following table:

CELL NAME	RELATIVE CELL AREA TO NA210LH	NO. USED	TOTAL RELATIVE CELL AREA	TOTAL C_{pd}‡ (pF)	MAXIMUM I_{CC} (nA)	
					SN54ASC'	SN74ASC'
IV110LH	0.75	3	2.25	1.32	310	19
IV120LH	1	5	5	4	655	39.3
NA510LH	1.75	8	14	4.16	1704	102.4
NA810LH	2.5	1	2.5	0.61	290	17.4
TOTALS		17	23.75	10.09	2964	179
Label: S151LH GZ,A,B,C,D0,D1,D2,D3,D4,D5,D6,D7,Y,W;						

‡The equivalent power dissipation capacitance does not include interconnect capacitance.

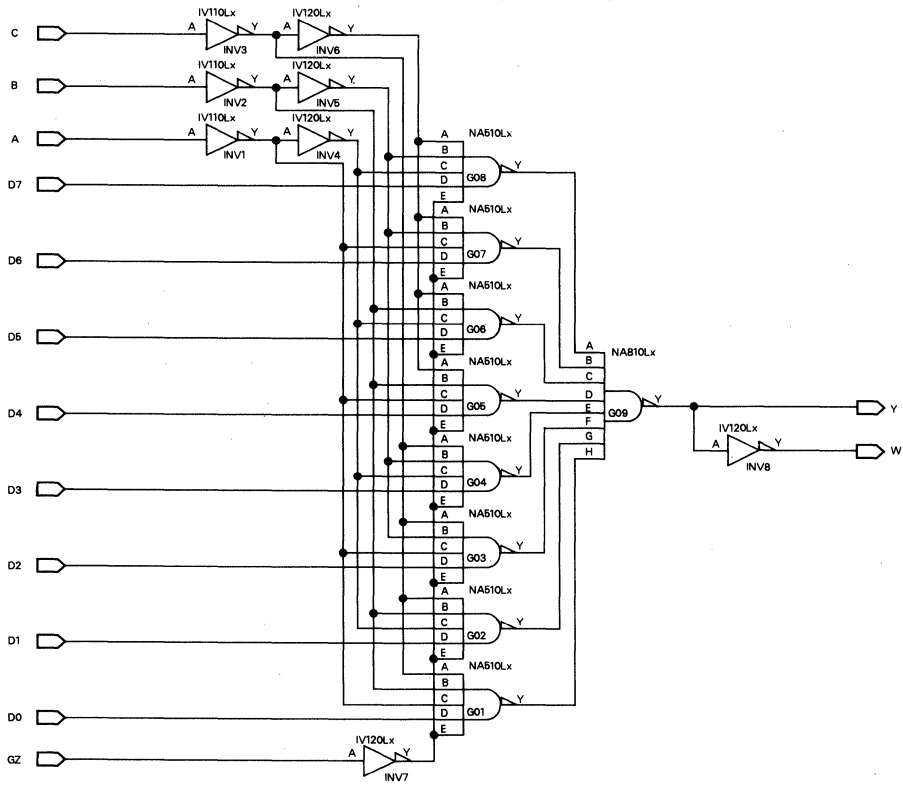
The SN54ASC151 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC151 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

INPUTS				OUTPUTS	
SELECT			STROBE		
C	B	A	GZ	Y	W
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

See explanation of Function Tables in Section 1.
D0, D1. . .D7 = the level of the respective D input.

logic diagram



TEXAS INSTRUMENTS
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absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER		TEST CONDITIONS	SN54ASC151		SN74ASC151		UNIT
			TYP	MAX	TYP	MAX	
V_T Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC} Supply current		V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN or MAX		2964		179	nA
C_i Input capacitance	GZ	V_{CC} = 5 V, T_A = 25°C	0.24		0.24		pF
	All other inputs		0.12		0.12		
C_{pd} Equivalent power dissipation capacitance†		V_{CC} = 5 V, T_A = 25°C, t_r = t_f = 3 ns,	10.09		10.09		pF

† The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 1)

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC151			SN74ASC151			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
t_{pd}	A, B, or C	Y	C_L = 0		7	16.5		7	14.8	ns
t_{pd}		W			8	17.5		8	15.8	
t_{pd}	Any D	Y			4	10.1		4	8.9	ns
t_{pd}		W			4.5	11.1		4.5	9.9	
t_{pd}	GZ	Y			5.5	12.7		5.5	11.3	ns
t_{pd}		W			6	13.7		6	12.3	
Δt_{pd}	Any	Y		0.6	2.6	8.7	0.6	2.6	7.5	ns/pF
Δt_{pd}	Any	W		0.3	0.5	1.1	0.3	0.5	1	

‡ Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{pd} ≡ propagation delay time, low-to-high or high-to-low-level output
Δt_{pd} ≡ change in t_{pd} with load capacitance
§ Typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: These switching characteristics are simulations of the software macro cell using interconnect capacitance values for an array design having 2,000 gates. Post-layout simulation uses actual interconnect capacitance values.

DESIGN CONSIDERATIONS

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

The HDL for this software macro is included as a part of the library supplied for supported engineering workstations so that a single label can be developed to apply the macro as needed. The following printout of the HDL block definition is furnished for reference.

HDL FILE

```
BLOCK S151LH;
GZ          @INPUT;
A           @INPUT;
B           @INPUT;
C           @INPUT;
D0          @INPUT;
D1          @INPUT;
D2          @INPUT;
D3          @INPUT;
D4          @INPUT;
D5          @INPUT;
D6          @INPUT
D7          @INPUT;
Y           @OUTPUT;
W           @OUTPUT;

STRUCTURE
G01         :NA510LH    CZ,BZ,AZ,D0,INV7O,U0;
G02         :NA510LH    CZ,BZ,AT,D1,INV7O,U1;
G03         :NA510LH    CZ,BT,AZ,D2,INV7O,U2;
G04         :NA510LH    CZ,BT,AT,D3,INV7O,U3;
G05         :NA510LH    CT,BZ,AZ,D4,INV7O,U4;
G06         :NA510LH    CT,BZ,AT,D5,INV7O,U5;
G07         :NA510LH    CT,BT,AZ,D6,INV7O,U6;
G08         :NA510LH    CT,BT,AT,D7,INV7O,U7;
G09         :NA810LH    U7,U6,U5,U4,U3,U2,U1,U0,Y;
INV1        :IV110LH    A,AZ;
INV2        :IV110LH    B,BZ;
INV3        :IV110LH    C,CZ;
INV4        :IV120LH    AZ,AT;
INV5        :IV120LH    BZ,BT;
INV6        :IV120LH    CZ,CT;
INV7        :IV120LH    GZ,INV7O;
INV8        :IV120LH    Y,W;
END S151LH;
```

Dedicated 8-line to 1-line multiplexers ('ASC2342) are also available in the standard cell library for implementing data-path multiplexers. The 'ASC2342 cell incorporates an enable input that can be used for expanding the word width. These hardwired cells should be considered if the multiplexer is in a critical path, as their performance is predetermined as specified in their switching characteristics.

interfacing the macro

Inputs and outputs of the predesigned macro are compatible for interfacing directly with cells and macros available in the TI standard cell library.

The outputs can be interfaced to drive off-chip loads with any of the noninverting output buffers or interfaced to external bidirectional buses through a 3-state input/output TTL/CMOS buffer.

If bus interface is needed, the 'ASC251 8-line to 1-line multiplexer incorporates 3-state outputs capable of driving internal data buses.

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D2939, AUGUST 1986

SystemCell™ 2-μm SOFTWARE MACRO CELL

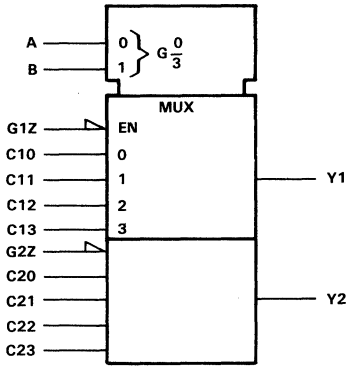
- **Active-Low Strobe for Expandability**
- **Use Parallel Multiplexers for Multiple-Bit Words**

description

The SN54ASC153 and SN74ASC153 are standard-cell software macros implementing dual 4-line to 1-line multiplexers.The 'ASC153 implements a function table identical with that performed by packaged 'HC153, 'LS153, 'S153, and 'F153 multiplexers.

Each 4-bit half of the macro has a strobe input that enables and disables its associated inputs. The Yn output is low when GnZ is high. When GnZ is low, the output assumes the level of the selected input. These strobes permit the macro to be employed for designing wider multiplexers, as only the enabled 4-bit field will output an active data bit. The 'ASC153 is implemented with the standard cell functions indicated. The HDL netlist label for this software macro is shown on the last line of the following table:

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

CELL NAME	RELATIVE CELL AREA TO NA210LH	NO. USED	TOTAL RELATIVE CELL AREA	TOTAL C_{pd}‡ (pF)	MAXIMUM I_{CC} (nA)	
					SN54ASC'	SN74ASC'
IV110LH	0.75	6	4.5	2.64	630	38
NA410LH	1.5	8	12	4	1496	89.6
NA420LH	2.5	2	5	1.92	624	37.4
TOTALS		16	21.5	8.56	2750	165
Label: S153LH G1Z,G2Z,A,B,C10,C11,C12,C13,C20,C21,C22,C23,Y1,Y2;						

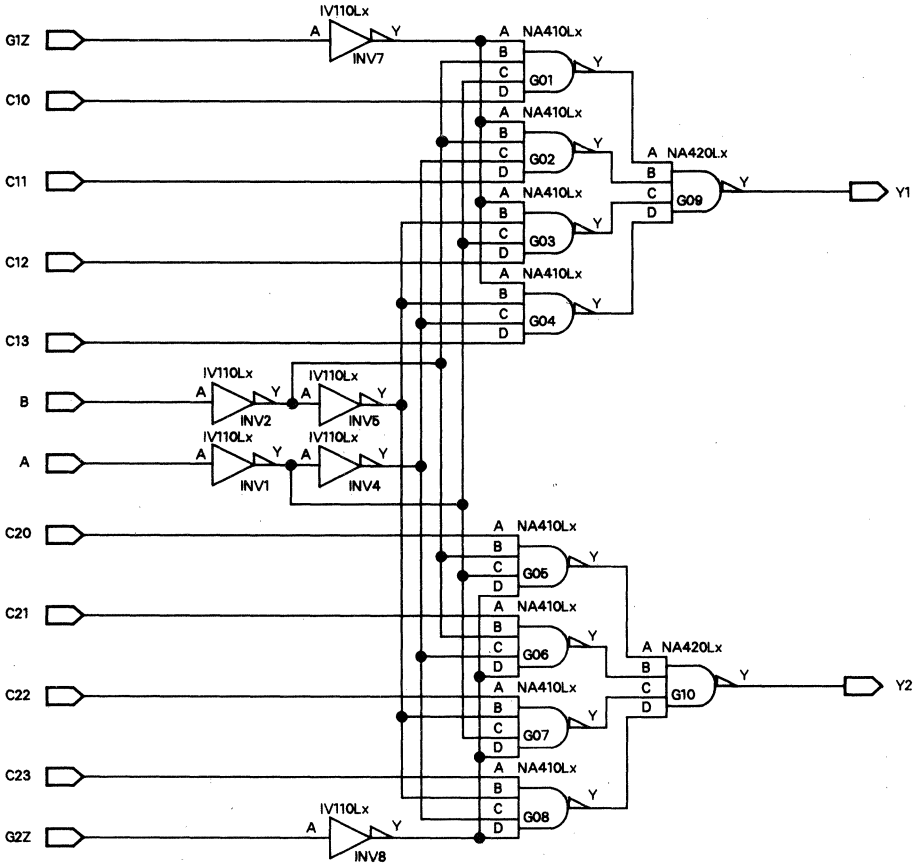
‡The equivalent power dissipation capacitance does not include interconnect capacitance.

The SN54ASC153 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC153 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

INPUTS						STROBE	OUTPUT
SELECT		DATA					
B	A	C0	C1	C2	C3	GnZ	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

logic diagram



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absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER		TEST CONDITIONS	SN54ASC153		SN74ASC153		UNIT
			TYP	MAX	TYP	MAX	
V_T	Input threshold voltage	V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN or MAX		2750		165	nA
C_i	Input capacitance	V_{CC} = 5 V, T_A = 25°C	0.12		0.12		pF
C_{pd}	Equivalent power dissipation capacitance†	V_{CC} = 5 V, T_A = 25°C, t_r = t_f = 3 ns,	8.56		8.56		pF

† The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted) (See Note 1)

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC153			SN74ASC153			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
t_{pd}	A or B	Y	C_L = 0		8	13.7		8	12.4	ns
t_{pd}	Any C	Y			4	7.1		4	6.3	ns
t_{pd}	G1Z or G2Z	Y			6.5	10.4		6.5	9.3	ns
Δt_{pd}	Any	Y		0.3	0.7	2.3	0.3	0.7	2	ns/pF

‡ Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{pd} ≡ propagation delay time, low-to-high or high-to-low-level output
Δt_{pd} ≡ change in t_{pd} with load capacitance
§ Typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: These switching characteristics are simulations of the software macro cell using interconnect capacitance values for an array design having 2,000 gates. Post-layout simulation uses actual interconnect capacitance values.

DESIGN CONSIDERATIONS

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

The HDL for this soft macro is included as a part of the library supplied for supported engineering workstations so that a single label can be developed to apply the macro as needed. The following printout of the HDL block definition is furnished for reference.

HDL FILE

```
BLOCK S153LH;
G1Z          @INPUT;
G2Z          @INPUT;
A            @INPUT;
B            @INPUT;
C10          @INPUT;
C11          @INPUT;
C12          @INPUT;
C13          @INPUT;
C20          @INPUT;
C21          @INPUT;
C22          @INPUT;
C23          @INPUT;
Y1           @OUTPUT;
Y2           @OUTPUT;

STRUCTURE
G01          :NA410LH        STB1Z,BZ,AZ,C10,U10;
G02          :NA410LH        STB1Z,BZ,AT,C11,U11;
G03          :NA410LH        STB1Z,BT,AZ,C12,U12;
G04          :NA410LH        STB1Z,BT,AT,C13,U13;
G05          :NA410LH        C20,BZ,AZ,STB2Z,U20;
G06          :NA410LH        C21,BZ,AT,STB2Z,U21;
G07          :NA410LH        C22,BT,AZ,STB2Z,U22;
G08          :NA410LH        C23,BT,ZT,STB2Z,U23;
G09          :NA420LH        U10,U11,U12,U13,Y1;
G10          :NA420LH        U20,U21,U22,U23,Y2;
INV1         :IV110LH        A,AZ;
INV2         :IV110LH        B,BZ;
INV4         :IV110LH        AZ,AT;
INV5         :IV110LH        BZ,BT;
INV7         :IV110LH        G1Z,STB1Z;
INV8         :IV110LH        G2Z,STB2Z;
END S153LH;
```

Dedicated 4-line to 1-line multiplexers ('SC2341) are also available in the standard cell library for implementing data-path multiplexers. These hardwired cells should be considered if the multiplexer is in a critical path, as their performance is predetermined as specified in their switching characteristics.

interfacing the macro

Inputs and outputs of the predesigned macro are compatible for interfacing directly with cells and macros available in the TI standard cell library.

The inputs can be driven by either inverting or noninverting input cells. The outputs can be interfaced to drive off-chip loads with any of the noninverting output buffers or interfaced to external bidirectional buses through a 3-state input/output TTL/CMOS buffer.

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• SystemCell™ 2-μm SOFTWARE MACRO CELL

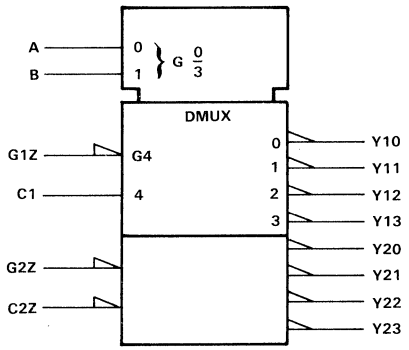
- Enable Input Permits Expansion of Each Decoder
- Individual Data Inputs to Each 4-Line Decoder
- Parallel Decoders for Multiple Bit Words

description

The SN54ASC155 and SN74ASC155 are standard-cell software macros implementing 8-line or dual 4-line decoders/demultiplexers. The 'ASC155 implements the full function table identical with that performed by packaged ICs such as the 'LS155A.

The A and B inputs are common to the two sections of the macro and select one of the four outputs in each section. Each section has a C input ANDed with a G input and for 4-line demultiplexer applications, a choice can be made in the use of these inputs as strobe and data inputs. In Section 1, when C1 is high the selected output assumes the level of G1Z, or to view this another way, when G1Z is low the selected output assumes the complement of the level of C1. In Section 2, C2Z and G2Z are interchangeable. When both are low, the selected output is low. When one of them is high, all outputs are high. Because the active levels of C1 and C2Z are complementary, they can be connected together in 3-line to 8-line decoder or 1-line to 8-line demultiplexer applications to serve as the third (C) select line with A and B. G1Z and G2Z are connected together as the active-low strobe or data line.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

The 'ASC155 is implemented with the standard cell functions indicated. The HDL netlist label for this software macro is shown on the last line of the following table:

CELL NAME	RELATIVE CELL AREA TO NA210LH	NO. USED	TOTAL RELATIVE CELL AREA	TOTAL C_{pd}‡ (pF)	MAXIMUM I_{CC} (nA)	
					SN54ASC'	SN74ASC'
IV110LH	0.75	1	0.75	0.44	105	6.32
IV120LH	1	4	4	3.2	524	31.4
NA320LH	2	8	16	7.52	2040	122.4
NO220LH	1.5	2	3	1.04	370	22.2
TOTALS		15	23.75	12.2	3039	183
Label: S155LH C1,G1Z,C2Z,G2Z,A,B,Y10,Y11,Y12,Y13,Y20,Y21,Y22,Y23;						

‡The equivalent power dissipation capacitance does not include interconnect capacitance.

The SN54ASC155 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC155 is characterized for operation from −40°C to 85°C.

FUNCTION TABLES
2-LINE-TO-4-LINE DECODER
OR 1-LINE-TO-4-LINE DEMULTIPLEXER

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	G1Z	C1	Y10	Y11	Y12	Y13
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	G2Z	C2Z	Y20	Y21	Y22	Y23
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

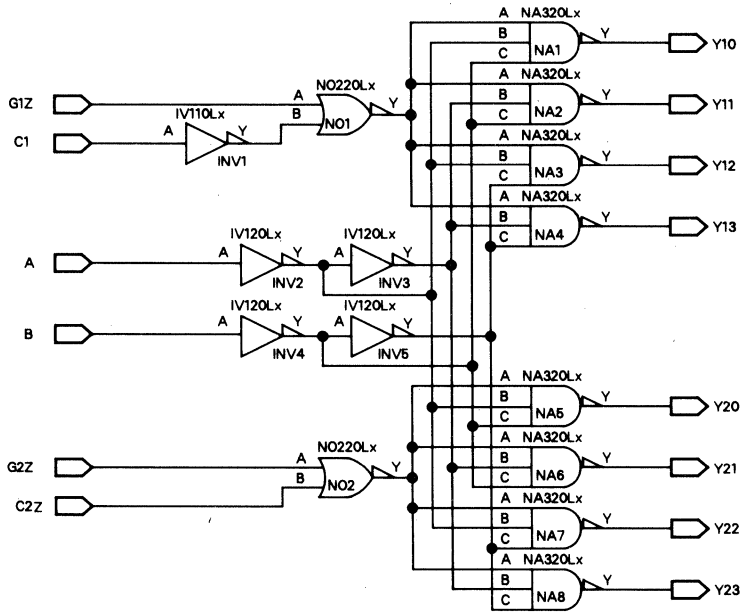
FUNCTION TABLE
3-LINE-TO-8-LINE DECODER
OR 1-LINE-TO-8-LINE DEMULTIPLEXER

INPUTS				OUTPUTS							
SELECT			STROBE OR DATA	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C†	B	A	$\overline{G}$‡	Y20	Y21	Y22	Y23	Y10	Y11	Y12	Y13
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

†C = inputs C1 and C2Z connected together
‡$\overline{G}$ = inputs G1Z and G2Z connected together

4 Data Sheets

logic diagram



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absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER		TEST CONDITIONS	SN54ASC155		SN74ASC155		UNIT
			TYP	MAX	TYP	MAX	
V_T Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC} Supply current		V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		3039		183	nA
C_i Input capacitance	A, B	V_{CC} = 5 V, T_A = 25°C	0.24		0.24		pF
	C1		0.12		0.12		
	C2Z, GnZ		0.24		0.24		
C_{pd} Equivalent power dissipation capacitance†		V_{CC} = 5 V, T_A = 25°C, t_r = t_f = 3 ns,	12.2		12.2		pF

† The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted) (see Note 1)

PARAMETER‡	FROM	TO	TEST CONDITIONS	SN54ASC155			SN74ASC155			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
t_{pd}	A or B	Any	C_L = 0		4	7.5		4	6.9	ns
t_{pd}	GnZ or Cn	Any Yn			5	8.6		5	8.1	ns
Δt_{pd}	Any	Any		0.3	0.6	1.8	0.3	0.6	1.5	ns/pF

‡ Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{pd} ≡ propagation delay time, low-to-high or high-to-low-level output
Δt_{pd} ≡ change in t_{pd} with load capacitance
§ Typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: These switching characteristics are simulations of the software macro cell using interconnect capacitance values for an array design having 2,000 gates. Post-layout simulation uses actual interconnect capacitance values.

DESIGN CONSIDERATIONS

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

The HDL for this software macro is included as a part of the library supplied for supported engineering workstations so that a single label can be developed to apply the macro as needed. The following printout of the HDL block definition is furnished for a reference.

HDL FILE

```
BLOCK S155LH;
C1          @INPUT;
G1Z         @INPUT;
C2Z         @INPUT;
G2Z         @INPUT;
A           @INPUT;
B           @INPUT;
Y10         @OUTPUT;
Y11         @OUTPUT;
Y12         @OUTPUT;
Y13         @OUTPUT;
Y20         @OUTPUT;
Y21         @OUTPUT;
Y22         @OUTPUT;
Y23         @OUTPUT;

STRUCTURE
INV1        :IV110LH        C1,INV1O;
INV2        :IV120LH        A,INV2O;
INV3        :IV120LH        INV2O,INV3O;
INV4        :IV120LH        B,INV4O;
INV5        :IV120LH        INV4O,INV5O;
NA1         :NA320LH        NO1O,INV2O,INV4O,Y10;
NA2         :NA320LH        NO1O,INV3O,INV4O,Y11;
NA3         :NA320LH        NO1O,INV2O,INV5O,Y12;
NA4         :NA320LH        NO1O,INV3O,INV5O,Y13;
NA5         :NA320LH        NO2O,INV2O,INV4O,Y20;
NA6         :NA320LH        NO2O,INV3O,INV4O,Y21;
NA7         :NA320LH        NO2O,INV2O,INV5O,Y22;
NA8         :NA320LH        NO2O,INV3O,INV5O,Y23;
NO1         :NO220LH        G1Z,INV1O,NO1O;
NO2         :NO220LH        G2Z,C2Z,NO2O;
END S155LH;
```

Dedicated 2-line to 4-line decoder cells ('ASC2350) are also available in the standard cell library for implementing small, data-path decoders. Two predesigned cells, designated as the DE210LH and the DE212LH, are offered. The DE212LH cell incorporates an enable input that can be used for expanding the word width. Latch cells can be added at the select inputs to provide storage. These hardwired cells should be considered if the decoder is in a critical path, as their performance is predetermined as specified in their switching characteristics.

interfacing the macro

Inputs and outputs of the predesigned macro are compatible for interfacing directly with cells and macros available in the TI standard cell library.

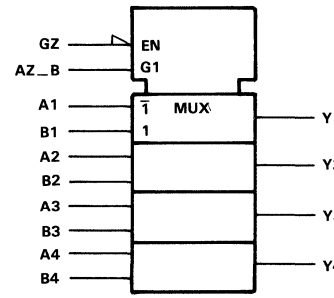
The outputs can be interfaced to drive off-chip loads with any of the noninverting output buffers or interfaced to external bidirectional buses through a 3-state input/output TTL/CMOS buffer.

D2939, AUGUST 1986

SystemCell™ 2-μm SOFTWARE MACRO CELL

- **Active-Low Strobe for Expandability**
- **Use Parallel Multiplexers for Multiple-Bit Words**

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The SN54ASC157 and SN74ASC157 are standard-cell software macros implementing four 2-line to 1-line multiplexers. The 'ASC157 implements a function table identical with that performed by packaged 'HC157, 'LS157, 'S157, and 'F157 multiplexers.

The macro has a strobe input, GZ, that enables and disables the outputs. The Y output is forced low when GZ is high. When GZ is low, the outputs assume the level of the selected inputs. This strobe permits the macro to be employed for designing wider multiplexers, only the enabled 2-bit field will output an active data bit. The 'ASC157 is implemented with standard cell functions indicated. The HDL netlist label for this software macro is shown on the last line of the following table:

CELL NAME	RELATIVE CELL AREA TO NA210LH	NO. USED	TOTAL RELATIVE CELL AREA	TOTAL C_{pd}‡ (pF)	MAXIMUM I_{CC} (nA)	
					SN54ASC'	SN74ASC'
IV110LH	0.75	2	1.5	0.88	210	12.64
NA210LH	1	12	12	6.12	1572	94.08
AN220LH	1.75	2	3.5	2.4	456	27.2
TOTALS		16	17	9.4	2238	134
Label: S157LH A1,A2,A3,A4,B1,B2,B3,B4,AZ_B,GZ,Y1,Y2,Y3,Y4;						

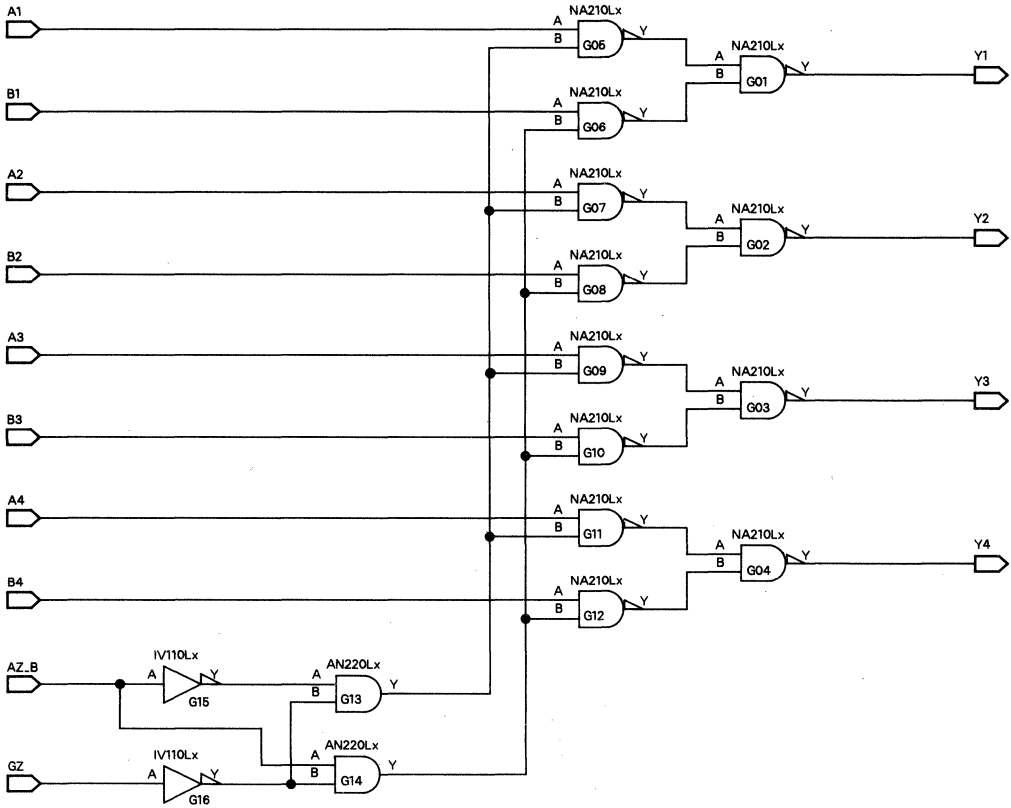
‡The equivalent power dissipation capacitance does not include interconnect capacitance.

The SN54ASC157 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC157 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

INPUTS				OUTPUT
STROBE	SELECT	DATA		
GZ	AZ_B	A	B	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

logic diagram



absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS	SN54ASC157 TYP	SN54ASC157 MAX	SN74ASC157 TYP	SN74ASC157 MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current		V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		2238		134	nA
C_i	Input capacitance	AZ_B	V_{CC} = 5 V, T_A = 25°C	0.25		0.25		pF
		All others		0.12		0.12		
C_{pd}	Equivalent power dissipation capacitance†		V_{CC} = 5 V, T_A = 25°C, t_r = t_f = 3 ns,	9.4		9.4		pF

† The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 1)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC157			SN74ASC157			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{pd}	Any A or B	Y	C_L = 0		2.2	4		2.2	3.7	ns
t_{pd}	GZ or AZ_B	Y			5.5	10.6		5.5	9.9	ns
Δt_{pd}	Any	Y		0.5	1.1	2.7	0.5	1.1	2.5	ns/pF

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f = 3$ ns (10% and 90%).
t_{pd} ≡ propagation delay time, low-to-high or high-to-low-level output
Δt_{pd} ≡ change in t_{pd} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: These switching characteristics are simulations of the software macro cell using interconnect capacitance values for an array design having 2,000 gates. Post-layout simulation uses actual interconnect capacitance values.

DESIGN CONSIDERATIONS

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

The HDL for this software macro is included as a part of the library supplied for supported engineering workstations so that a single label can be developed to apply the macro as needed. The following printout of the HDL block definition is furnished for reference.

HDL FILE

```
BLOCK S157LH;
A1          @INPUT;
A2          @INPUT;
A3          @INPUT;
A4          @INPUT;
B1          @INPUT;
B2          @INPUT;
B3          @INPUT;
B4          @INPUT;
AZ_B        @INPUT;
GZ          @INPUT
Y1          @OUTPUT;
Y2          @OUTPUT;
Y3          @OUTPUT;
Y4          @OUTPUT;

STRUCTURE
G01         :NA210LH        G05O,G06O,Y1;
G02         :NA210LH        G07O,G08O,Y2;
G03         :NA210LH        G09O,G10O,Y3;
G04         :NA210LH        G11O,G12O,Y4;
G05         :NA210LH        A1,G13O,G05O;
G06         :NA210LH        B1,G14O,G06O;
G07         :NA210LH        A2,G13O,G07O;
G08         :NA210LH        B2,G14O,G08O;
G09         :NA210LH        A3,G13O,G09O;
G10         :NA210LH        B3,G14O,G10O;
G11         :NA210LH        A4,G13O,G11O;
G12         :NA210LH        B4,G14O,G12O;
G13         :AN220LH        G15O,G16O,G13O;
G14         :AN220LH        AZ_B,G16O,G14O;
G15         :IV110LH        AZ_B,G15O;
G16         :IV110LH        GZ,G16O;
END S157LH;
```

Dedicated 2-line to 1-line multiplexers are also available in the standard cell library ('SC2340) for implementing data-path multiplexers. These hardwired cells should be considered if the multiplexer is in a critical path, as their performance is predetermined as specified in their switching characteristics.

interfacing the macro

Inputs and outputs of the predesigned macro are compatible for interfacing directly with cells and macros available in the TI standard cell library.

The inputs can be driven by either inverting or noninverting input cells when interfacing off-chip for the input data words. The outputs can be interfaced to drive off-chip loads with any of the noninverting output buffers or interfaced to external bidirectional buses through a 3-state input/output TTL/CMOS buffer.

If bus interface is needed, the 'ASC257A 2-line to 1-line multiplexer incorporates 3-state outputs capable of driving internal data buses.

TEXAS INSTRUMENTS
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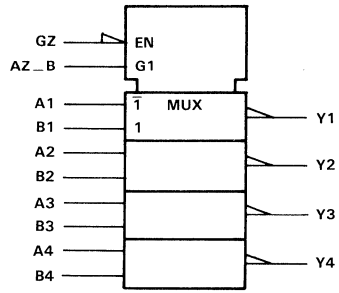
D2939, AUGUST 1986

SystemCell™ 2-μm SOFTWARE MACRO CELL

- **Active-Low Strobe for Expandability**
- **Use Parallel Multiplexers for Multiple-Bit Words**

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The SN54ASC158 and SN74ASC158 are standard-cell software macros implementing four 2-line to 1-line multiplexers. The 'ASC158 implements a function table identical with that performed by packaged 'HC158, 'LS158, 'S158, and 'F158 multiplexers.

The macro has a strobe input, GZ, that enables and disables the outputs. The Y output is forced high when GZ is high. When GZ is low, the output assumes the complement of the level of the selected input. This strobe permits the macro to be employed for designing wider multiplexers, as only the enabled 2-bit field will output an active data bit. The 'ASC158 is implemented with standard cell functions indicated. The HDL netlist label for this software macro is shown on the last line of the following table:

CELL NAME	RELATIVE CELL AREA TO NA210LH	NO. USED	TOTAL RELATIVE CELL AREA	TOTAL C_{pd}‡ (pF)	MAXIMUM I_{CC} (nA)	
					SN54ASC'	SN74ASC'
IV110LH	0.75	2	1.5	0.88	210	12.64
NA210LH	1	8	8	4.08	1048	62.72
AN220LH	1.75	6	10.5	7.2	1368	81.6
TOTALS		16	20	12.16	2626	157
Label: S158LH A1,A2,A3,A4,B1,B2,B3,B4,AZ_B,GZ,Y1,Y2,Y3,Y4;						

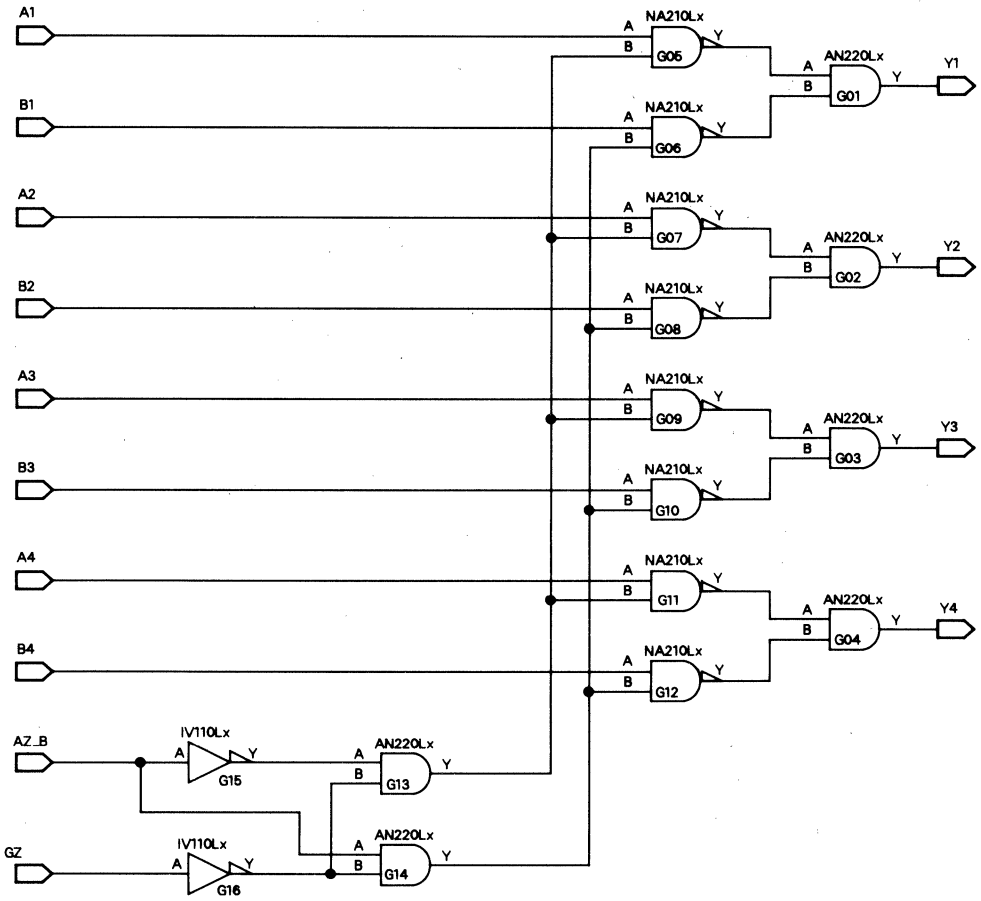
‡The equivalent power dissipation capacitance does not include interconnect capacitance.

The SN54ASC158 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC158 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

INPUTS				OUTPUT
STROBE	SELECT	DATA		
GZ	AZ_B	A	B	Y
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

logic diagram



absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS		SN54ASC158		SN74ASC158		UNIT
					TYP	MAX	TYP	MAX	
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current		V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX			2626		157	nA
C_i	Input capacitance	AZ_B	V_{CC} = 5 V,	T_A = 25°C	0.25		0.25		pF
		All others			0.12		0.12		
C_{pd}	Equivalent power dissipation capacitance†		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	12.16		12.16		pF

† The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 1)

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC158			SN74ASC158			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
t_{pd}	Any A or B	Y	C_L = 0		2.8	5.7		2.8	5.2	ns
t_{pd}	GZ or AZ_B	Y			6.2	12.2		6.2	11.4	ns
Δt_{pd}	Any	Y		0.1	0.4	1.2	0.2	0.4	1.1	ns/pF

‡ Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{pd} ≡ propagation delay time, low-to-high or high-to-low-level output
Δt_{pd} ≡ change in t_{pd} with load capacitance
§ Typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: These switching characteristics are simulations of the software macro cell using interconnect capacitance values for an array design having 2,000 gates. Post-layout simulation uses actual interconnect capacitance values.

DESIGN CONSIDERATIONS

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

The HDL for this software macro is included as a part of the library supplied for supported engineering workstations so that a single label can be developed to apply the macro as needed. The following printout of the HDL block definition is furnished for reference.

HDL FILE

```
BLOCK S158LH;
A1          @INPUT;
A2          @INPUT;
A3          @INPUT;
A4          @INPUT;
B1          @INPUT;
B2          @INPUT;
B3          @INPUT;
B4          @INPUT;
AZ_B        @INPUT;
GZ          @INPUT
Y1          @OUTPUT;
Y2          @OUTPUT;
Y3          @OUTPUT;
Y4          @OUTPUT;

STRUCTURE
G01         :AN220LH        G05O,G06O,Y1;
G02         :AN220LH        G07O,G08O,Y2;
G03         :AN220LH        G09O,G10O,Y3;
G04         :AN220LH        G11O,G12O,Y4;
G05         :NA210LH        A1,G13O,G05O;
G06         :NA210LH        B1,G14O,G06O;
G07         :NA210LH        A2,G13O,G07O;
G08         :NA210LH        B2,G14O,G08O;
G09         :NA210LH        A3,G13O,G09O;
G10         :NA210LH        B3,G14O,G10O;
G11         :NA210LH        A4,G13O,G11O;
G12         :NA210LH        B4,G14O,G12O;
G13         :AN220LH        G15O,G16O,G13O;
G14         :AN220LH        AZ_B,G16O,G14O;
G15         :IV110LH        AZ_B,G15O;
G16         :IV110LH        GZ,G16O;
END S158LH;
```

Dedicated 2-line to 1-line multiplexers ('ASC2340) are also available in the standard cell library for implementing data-path multiplexers. These hardwired cells should be considered if the multiplexer is in a critical path, as their performance is predetermined as specified in their switching characteristics.

interfacing the macro

Inputs and outputs of the predesigned macro are compatible for interfacing directly with cells and macros available in the TI standard cell library.

The inputs can be driven with inverting or noninverting input cells. The outputs can be interfaced to drive off-chip loads with any of the noninverting output buffers or interfaced to external bidirectional buses through a 3-state input/output TTL/CMOS buffer.

If bus interface is needed, the 'ASC258A 2-line to 1-line multiplexer incorporates 3-state outputs capable of driving internal data buses.

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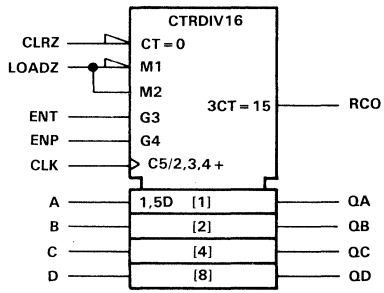
D2939, AUGUST 1986

SystemCell™ 2-μm SOFTWARE MACRO CELL

- **Internal Look-Ahead Enhances Performance of Cascaded Counters**
- **Asynchronous Clear Initializes Sequence Regardless of Mode**
- **Parallel Synchronously Presettable for Full-Cycle Modulo-N Sequences**
- **Gated Enables and RCO Implement Local and Global Carry Status**

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The SN54ASC161A and SN74ASC161A are standard-cell software macros implementing synchronous 4-bit binary counter elements. The 4-bit configuration provides the custom IC designer a synchronous counter to embed in ASICs in its most efficient form, and its 4-bit length means that testability is simplified when constructing large counters. The 'ASC161A implements a count sequence identical with that performed by packaged 'HC161A, 'LS161A, and 'F161A counters.

Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidentally with each other when so instructed by the count-enable inputs and other gating. This mode of operation eliminates output counting spikes associated with asynchronous (ripple) counters. The clear and load inputs are buffered to enhance performance, and clocking of the register occurs on the rising (positive-going) edge of the clock waveform. The 'ASC161A is implemented with the standard cell functions indicated. The HDL netlist label for this software macro is shown on the last line of the following table:

CELL NAME	RELATIVE CELL AREA TO NA210LH	NO. USED	TOTAL RELATIVE CELL AREA	TOTAL C_{pd}‡ (pF)	MAXIMUM I_{CC} (nA)	
					SN54ASC'	SN74ASC'
AN320LH	2	1	2	1.56	249	15
IV110LH	0.75	4	4	1.76	420	25.28
IV120LH	1	4	4	3.2	524	31.4
IV140LH	1.5	2	3	3.22	380	22.8
NA210LH	1	6	6	3.06	786	47.04
NA310LH	1.25	10	12.5	5	1630	97.8
NA410LH	1.5	2	3	1	374	22.4
NA510LH	1.75	2	3.5	1.04	426	25.6
R2406LH	26.25	1	26.25	11.69	2931	176
TOTALS		32	63.25	31.53	7720	464
Label: S161ALH D,C,B,A,CLK,CLRZ,ENP,ENT,LOADZ,QD,QC,QB,QA,RCO;						

‡The equivalent power dissipation capacitance does not include interconnect capacitance.

These counters are fully programmable; that is, they may be preset to any number between 0 and 15. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs.

Clearing is asynchronous. A low level at the clear input sets all outputs low regardless of the levels of the clock, load, or enable.

The carry look-ahead circuitry provides for cascading counters in n-bit synchronous applications without additional gating. Instrumental in achieving this are two count-enable inputs and a ripple carry output. Both count-enable inputs (ENP and ENT) must be high to count. ENP enables the local 4-bits and the ENT is fed forward to globally extend the enable/disable of previous/next 4-bit cascaded counters. The ripple-carry out (RCO), when locally and globally enabled, will output a high-level pulse at maximum count that is used to enable successive stages.

These counters feature a fully independent clock. Changes at control inputs other than the clear will have no effect on the counter until clocking occurs. The functions of the counter are dictated solely by conditions meeting setup, hold, and duration recommendations.

The SN54ASC161A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC161A is characterized for operation from −40°C to 85°C.

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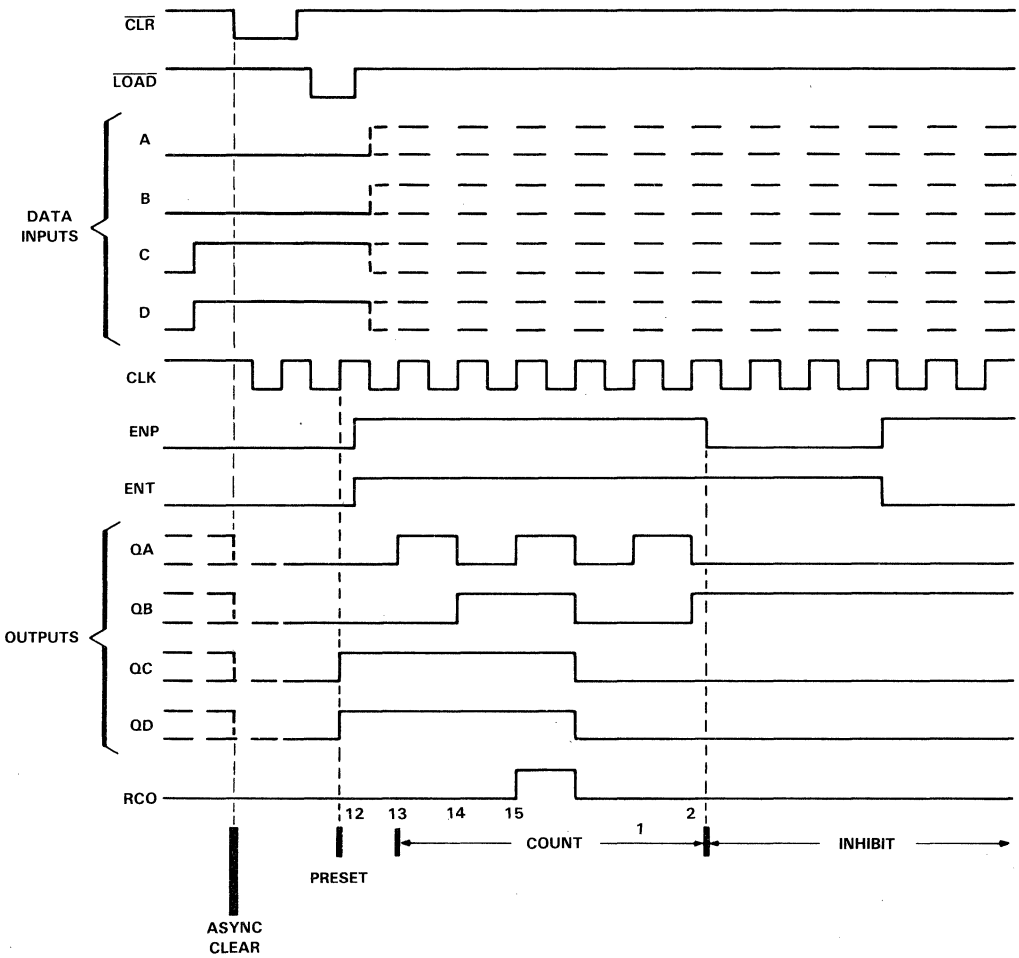
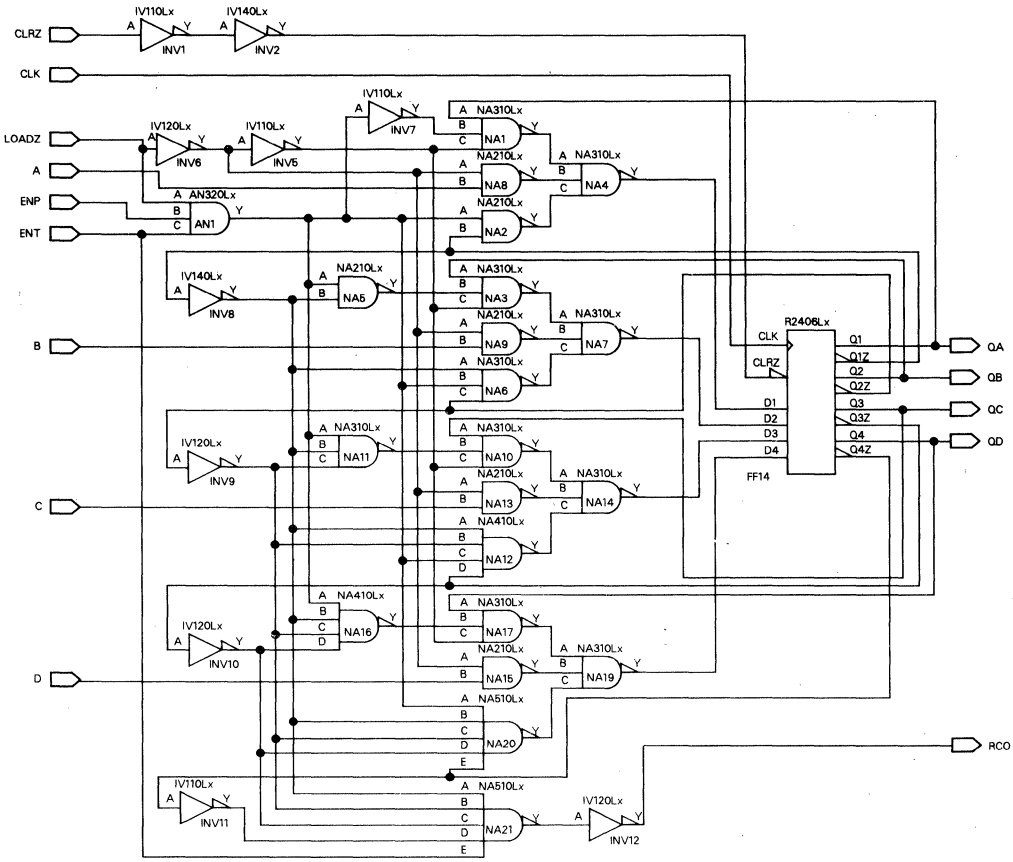
'ASC161A output sequence

Illustrated below is the following sequence:

1. Asynchronously clear outputs to zero
2. Preset to binary twelve
3. Count to thirteen, fourteen, fifteen, zero, one, and two
4. Inhibit



logic diagram



absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

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electrical characteristics

PARAMETER		TEST CONDITIONS	SN54ASC161A TYP	SN54ASC161A MAX	SN74ASC161A TYP	SN74ASC161A MAX	UNIT
V_T Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC} Supply current		V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		7720		464	nA
C_i Input capacitance	A,B,C,D	V_{CC} = 5 V, T_A = 25°C	0.12		0.12		pF
	CLK		0.24		0.24		
	CLRZ		0.12		0.12		
	ENP		0.12		0.12		
	ENT		0.25		0.25		
	LOADZ		0.36		0.36		
C_{pd} Equivalent power dissipation capacitance†		V_{CC} = 5 V, T_A = 25°C, t_r = t_f = 3 ns,	31.54		31.54		pF

† The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted) (see Note 1)

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC161A MIN	SN54ASC161A TYP§	SN54ASC161A MAX	SN74ASC161A MIN	SN74ASC161A TYP§	SN74ASC161A MAX	UNIT
t_{pd}	CLK	RCO	C_L = 0		12	22		12	19.8	ns
t_{pd}	CLK	Any Q			4.5	10.4		4.5	9.4	ns
t_{pd}	ENT	RCO			4	7.6		4	6.6	ns
t_{PHL}	CLRZ	Any Q			5	8.3		5	7.7	ns
t_{PHL}	CLRZ	RCO			12	19.5		12	17.9	ns
Δt_{pd}	Any	Any Q		0.3	1	2.4	0.3	1	2.1	ns/pF
Δt_{pd}	Any	RCO		0.3	0.5	1.1	0.3	0.5	1	ns/pF

‡ Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{pd} ≡ propagation delay time, low-to-high or high-to-low-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{pd} ≡ change in t_{pd} with load capacitance
§ Typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: These switching characteristics are simulations of the software macro cell using interconnect capacitance values for an array design having 2,000 gates. Post-layout simulation uses actual interconnect capacitance values.

DESIGN CONSIDERATIONS

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

The HDL for this software macro is included as a part of the library supplied for supported engineering workstations so that a single label can be developed to apply the macro as needed. The following printout of the HDL block definition is furnished for reference.

HDL FILE

```
BLOCK S161ALH;
D           @INPUT;
C           @INPUT;
B           @INPUT;
A           @INPUT;
CLK         @INPUT;
CLRZ        @INPUT;
ENP         @INPUT;
ENT         @INPUT;
LOADZ       @INPUT;
QD          @OUTPUT;
QC          @OUTPUT;
QB          @OUTPUT;
QA          @OUTPUT;
RCO         @OUTPUT;

STRUCTURE
AN1         :AN320LH        LOADZ,ENP,ENT,AN1O;
FF14        :R2406LH        INV2O,NA4O,NA7O,NA14O,NA19O,CLK,QA,FFA_QZ,
                            QB,FFB_QZ,QC,FFC_QZ,QD,FFD_QZ;
INV1        :IV110LH        CLRZ,INV1O;
INV10       :IV120LH        FFC_QZ,INV10O;
INV11       :IV110LH        FFD_QZ11O;
INV12       :IV120LH        NA21O,RCO;
INV2        :IV140LH        INV1O,INV2O;
INV5        :IV110LH        INV6O,INV5O;
INV6        :IV120LH        LOADZ,INV6O;
INV7        :IV110LH        AN1O,INV7O;
INV8        :IV140LH        FFA_QZ,INV8O;
INV9        :IV120LH        FFB_QZ,INV9O;
NA1         :NA310LH        QA,INV7O,INV5O,NA1O;
NA10        :NA310LH        QC,NA11O,INV5O,NA10O;
NA11        :NA310LH        AN1O,INV8O,INV9O,NA11O;
NA12        :NA410LH        INV8O,INV9O,AN1O,FFC_QZ,NA12O;
NA13        :NA210LH        INV6O,C,NA13O;
NA14        :NA310LH        NA10O,NA13O,NA12O,NA14O;
NA15        :NA210LH        INV6O,D,NA15O;
NA16        :NA410LH        AN1O,INV8O,INV9O,INV10O,NA16O;
NA17        :NA310LH        QD,NA16O,INV5O,NA17O;
NA19        :NA310LH        NA17O,NA15O,NA20O,NA19O;
NA2         :NA210LH        AN1O,FFA_QZ,NA2O;
NA20        :NA510LH        AN1O,INV8O,INV9O,INV10O,FFD_QZ,NA20O;
NA21        :NA510LH        INV8O,INV9O,INV10O,INV11O,ENT,NA21O;
NA3         :NA310LH        QB,NA5O,INV5O,NA3O;
NA4         :NA310LH        NA1O,NA8O,NA2O,NA4O;
NA5         :NA210LH        AN1O,INV8O,NA5O;
NA6         :NA310LH        INV8O,AN1O,FFB_QZ,NA6O;
NA7         :NA310LH        NA3O,NA9O,NA6O,NA7O;
NA8         :NA210LH        INV6O,A,NA8O;
NA9         :NA210LH        INV6O,B,NA9O;
END S161ALH;
```


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count definition

These counters are unidirectional with respect to count operation. Inverting the output levels will produce a down-count sequence. Bidirectional counters are available in software macros or can be constructed using the 'ASC2405 through 'ASC2407 4-bit predesigned registers.

designing for testability

Designs employing storage or bistable elements, especially long counters (ripple or synchronous), should consider testability of the design in its final form. The need to preset or clear and read intermediate stages of these elements should be assessed throughout the development of custom logic circuits with these considerations extended to the end-equipment application with respect to maintainability. Simple actions on the part of the ASIC designer can result in considerable cost savings, allowing the expense of IC testing, system testing, and system maintenance to be reduced significantly.

power-up clear/preset

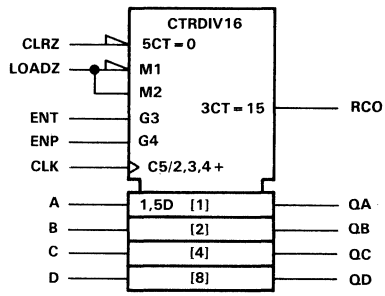
Standard cell storage elements containing the capability to be asynchronously preset or cleared may be connected to the SN54ASC2320 or SN74ASC2320 power-up clear cell to achieve system initialization. Control of the clear or preset inputs from another system signal in conjunction with the power-up clear can be achieved with an AND gate.

D2939, AUGUST 1986

SystemCell™ 2-μm SOFTWARE MACRO CELL

- **Internal Look-Ahead Enhances Performance of Cascaded Counters**
- **Synchronous Clear Initializes Sequence Regardless of Mode**
- **Parallel Synchronously Presettable for Full-Cycle Modulo-N Sequences**
- **Gated Enables and RCO Implement Local and Global Carry Status**

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The SN54ASC163A and SN74ASC163A are standard-cell software macros implementing synchronous 4-bit binary counter elements. The 4-bit configuration provides the custom IC designer a synchronous counter to embed in ASICs in its most efficient form, and its 4-bit length means that testability is simplified when constructing large counters. The 'ASC163A implements a count sequence identical with that performed by packaged 'HC163, 'LS163A, and 'F163A counters.

Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidentally with each other when so instructed by the count-enable inputs and other gating. This mode of operation eliminates output counting spikes associated with asynchronous (ripple) counters. The clear and load inputs are buffered to enhance performance, and clocking of the register occurs on the rising (positive-going) edge of the clock waveform.

The 'ASC163 is implemented with the standard cell functions indicated. The HDL netlist label for this software macro is shown on the last line of the following table:

CELL NAME	RELATIVE CELL AREA TO NA210LH	NO. USED	TOTAL RELATIVE CELL AREA	TOTAL C_{pd}‡ (pF)	MAXIMUM I_{CC} (nA)	
					SN54ASC'	SN74ASC'
AN410LH	2	1	2	1.18	256	15.3
IV110LH	0.75	3	2.25	1.32	315	18.96
IV120LH	1	3	3	2.4	393	23.55
IV140LH	1.5	1	1.5	1.61	190	11.4
NA210LH	1	6	6	3.06	786	47.04
NA310LH	1.25	10	12.5	5	1630	97.8
NA410LH	1.5	2	3	1	374	22.4
NA510LH	1.75	2	3.5	1.04	426	25.6
NO220LH	1.5	1	1.5	0.52	185	11.1
NO240LH	2.5	1	2.5	0.98	292	17.5
R2406LH	41	1	26.25	11.69	2931	176
TO010LH	2	1	2	—	177	10.6
TOTALS		32	66	29.8	7955	478
Label: S163ALH D,C,B,A,CLK,CLRZ,ENP,ENT,LOADZ,QD,QC,QB,QA,RCO;						

‡The equivalent power dissipation capacitance does not include interconnect capacitance.

These counters are fully programmable; that is, they may be preset to any number between 0 and 15. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of the enable inputs.

Clearing is synchronous. A low level at the clear input will set all outputs low on the next positive transition of the clock.

The carry look-ahead circuitry provides for cascading counters in n-bit synchronous applications without additional gating. Instrumental in achieving this are two count-enable inputs and a ripple carry output. Both count-enable inputs (ENP and ENT) must be high to count. ENP enables the local 4-bits and the ENT is fed forward to globally extend the enable/disable of previous/next 4-bit cascaded counters. The ripple-carry out (RCO), when locally and globally enabled, will output a high-level pulse at maximum count that is used to enable successive stages.

These counters feature a fully independent clock. Changes at control inputs, including clear, will have no effect on the counter until clocking occurs. The functions of the counter are dictated solely by conditions meeting setup, hold, and duration recommendations.

The SN54ASC163A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC163A is characterized for operation from −40°C to 85°C.

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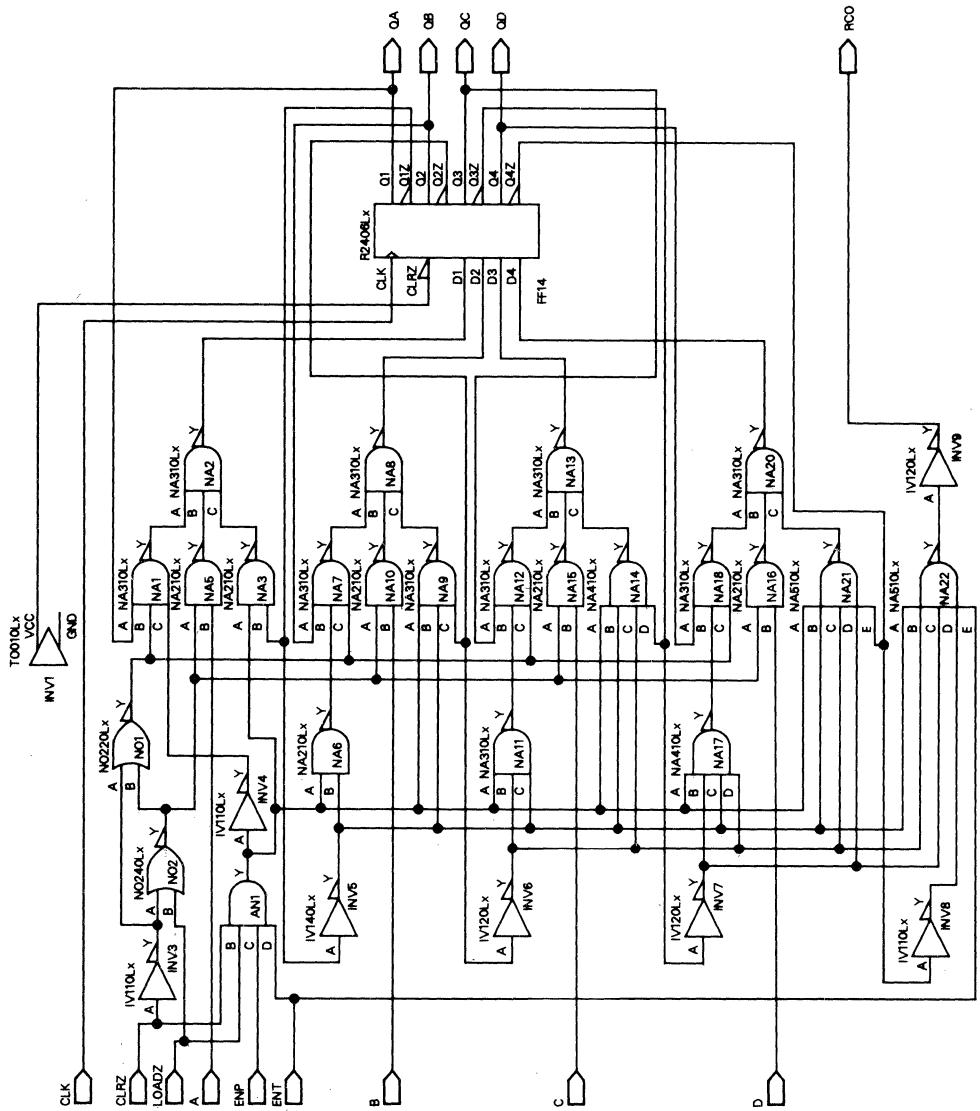
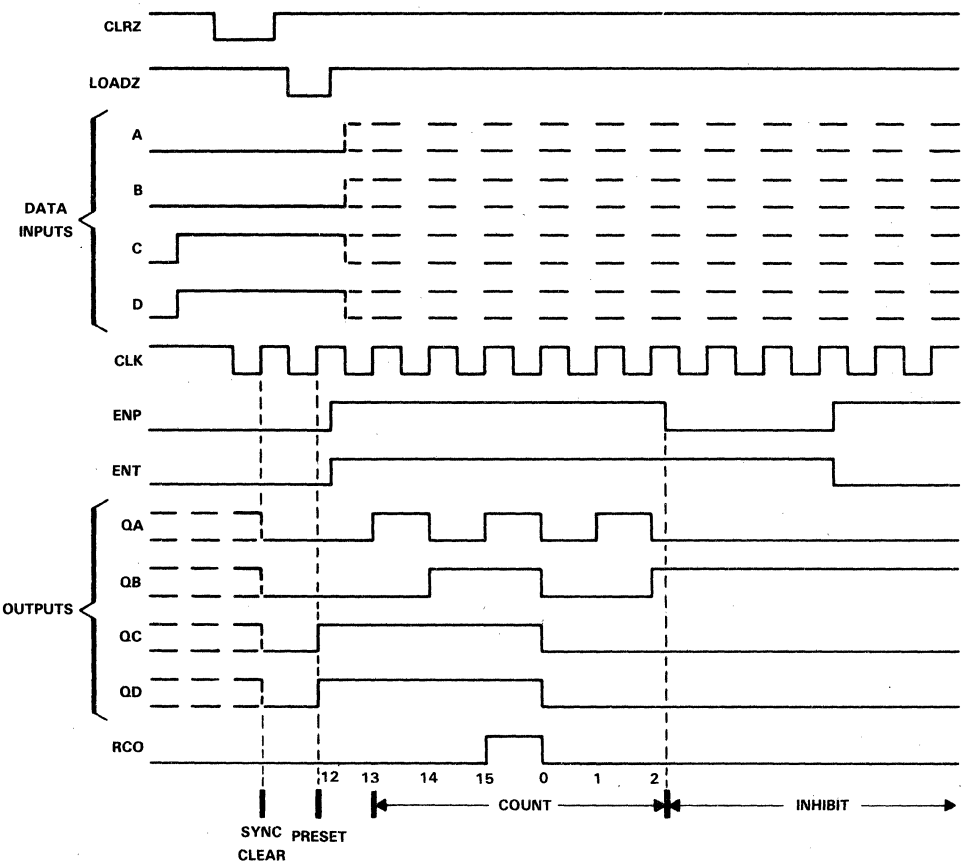
logic diagram (positive logic)



'ASC163A output sequence

Illustrated below is the following sequence:

1. Synchronously clear outputs to zero
2. Preset to binary twelve
3. Count to thirteen, fourteen, fifteen, zero, one, and two
4. Inhibit



absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

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electrical characteristics

PARAMETER			TEST CONDITIONS	SN54ASC163A		SN74ASC163A		UNIT
				TYP	MAX	TYP	MAX	
V_T	Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current		V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		7955		478	nA
C_i	Input capacitance	A,B,C,D	V_{CC} = 5 V, T_A = 25°C	0.12		0.12		pF
		CLK		0.24		0.24		
		CLRZ		0.24		0.24		
		ENP		0.12		0.12		
		ENT		0.24		0.24		
		LOADZ		0.59		0.59		
C_{pd}	Equivalent power dissipation capacitance†		V_{CC} = 5 V, T_A = 25°C, t_r = t_f = 3 ns,	29.8		29.8		pF

† The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (See Note 1)

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC163A			SN74ASC163A			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
t_{pd}	CLK	RCO	C_L = 0		9	22.2		9	20.1	ns
t_{pd}	CLK	Any Q			5	10.6		5	9.6	ns
t_{pd}	ENT	RCO			2	7.6		2	6.6	ns
Δt_{pd}	Any	Any Q		0.3	1	2.4	0.3	1	2.1	ns/pF
Δt_{pd}	Any	RCO		0.3	0.5	1.1	0.3	0.5	1	ns/pF

‡ Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{pd} ≡ propagation delay time, low-to-high or high-to-low-level output
Δt_{pd} ≡ change in t_{pd} with load capacitance
§ Typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: These switching characteristics are simulations of the software macro cell using interconnect capacitance values for an array design having 2,000 gates. Post-layout simulation uses actual interconnect capacitance values.

DESIGN CONSIDERATIONS

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

The HDL for this software macro is included as a part of the library supplied for supported engineering workstations so that a single label can be developed to apply the macro as needed. The following printout of the HDL block definition is furnished for reference.

HDL FILE

```
BLOCK S163ALH;
D           @INPUT;
C           @INPUT;
B           @INPUT;
A           @INPUT;
CLK         @INPUT;
CLRZ        @INPUT;
ENP         @INPUT;
ENT         @INPUT;
LOADZ       @INPUT;
QD          @OUTPUT;
QC          @OUTPUT;
QB          @OUTPUT;
QA          @OUTPUT;
RCO         @OUTPUT;

STRUCTURE
AN1         :AN410LH        CLRZ,LOADZ,ENP,ENT,AN1O;
FF14        :R2406LH        ICLRZ,NA2O,NA8O,NA13O,NA20O,CLK,QA,QAZ,QB,QBZ,
                            QC,QCZ,QD,QDZ;
INV1        :TO010LH        DUM,ICLRZ;
INV3        :IV110LH        CLRZ,INV3O;
INV4        :IV110LH        AN1O,INV4O;
INV5        :IV140LH        QAZ,INV5O;
INV6        :IV120LH        QBZ,INV6O;
INV7        :IV120LH        QCZ,INV7O;
INV8        :IV110LH        QDZ,INV8O;
INV9        :IV120LH        NA22O,RCO;
NA1         :NA310LH        QA,NO1O,INV4O,NA1O;
NA10        :NA210LH        NO2O,B,NA10O;
NA11        :NA310LH        AN1O,INV6O,INV5O,NA11O;
NA12        :NA310LH        QC,NA11O,NO1O,NA12O;
NA13        :NA310LH        NA12O,NA15O,NA14O,NA13O;
NA14        :NA410LH        AN1O,INV5O,INV6O,QCZ,NA14O;
NA15        :NA210LH        NO2O,C,NA15O;
NA16        :NA210LH        NO2O,D,NA16O;
NA17        :NA410LH        AN1O,INV7O,INV5O,INV6O,NA17O;
NA18        :NA310LH        QD,NA17O,NO1O,NA18O;
NA2         :NA310LH        NA1O,NA5O,NA3O,NA2O;
NA20        :NA310LH        NA18O,NA16O,NA21O,NA20O;
NA21        :NA510LH        AN1O,INV5O,INV6O,INV7O,QDZ,NA21O;
NA22        :NA510LH        INV5O,INV6O,INV7O,INV8O,ENT,NA22O;
NA3         :NA210LH        AN1O,QAZ,NA3O;
NA5         :NA210LH        NO2O,A,NA5O;
NA6         :NA210LH        AN1O,INV5O,NA6O;
NA7         :NA310LH        QB,NA6O,NO1O,NA7O;
NA8         :NA310LH        NA7O,NA10O,NA9O,NA8O;
NA9         :NA310LH        AN1O,INV5O,QBZ,NA9O;
NO1         :NO220LH        INV3O,NO2O,NO1O;
NO2         :NO240LH        INV3O,LOADZ,NO2O;
END S163ALH;
```


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count definition

These counters are unidirectional with respect to count operation. Inverting the output levels will produce a down-count sequence. Bidirectional counters are available in software macros or can be constructed using the 'ASC2405 through 'ASC2407 4-bit predesigned registers.

designing for testability

Designs employing storage or bistable elements, especially long counters (ripple or synchronous), should consider testability of the design in its final form. The need to preset or clear and to read intermediate stages of these elements should be assessed throughout the development of custom logic circuits with these considerations extended to the end-equipment application with respect to maintainability. Simple actions on the part of the ASIC designer can result in considerable cost savings, allowing the expense of IC testing, system testing, and system maintenance to be reduced significantly.

power-up clear/preset

Standard cell storage elements containing the capability to be asynchronously preset or cleared may be connected to the SN54ASC2320 or SN74ASC2320 power-up clear cell to achieve system initialization. Control of the clear or preset inputs from another system signal in conjunction with the power-up clear can be achieved with an AND gate.

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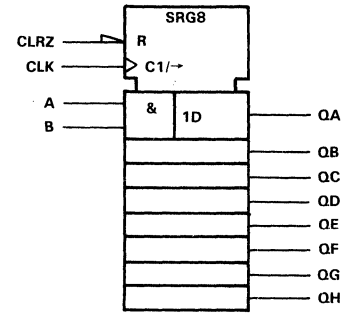
SystemCell™ 2-μm SOFTWARE MACRO CELL

- **AND-Gated (Enable/Disable) Serial Inputs**
- **Buffered Clear and Serial Inputs**
- **Direct Clear**
- **Embedded Clock Drivers Provide Clock Buffering**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The SN54ASC164 and SN74ASC164 are standard-cell software macros implementing 8-bit parallel-out shift registers. The 8-bit configuration provides the custom IC designer a register to embed in ASICs in its most efficient form. Its 8-bit length simplifies construction of large counters. The 'ASC164 implements a shift sequence identical with that performed by packaged 'HC164, 'LS164, and 'F164 registers.

These 8-bit shift registers feature AND-gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data, as a low at either input inhibits entry of new data and resets the first flip-flop to a low level at the next clock pulse. A high-level input enables the other input, which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, provided the minimum setup time requirements are met. Clocking occurs on the low-to-high-level transition of the clock pulse.

The 'ASC164 is implemented with the standard cell functions indicated. The HDL netlist label for this software macro is shown on the last line of the following table:

CELL NAME	RELATIVE CELL AREA TO NA210LH	NO. USED	TOTAL RELATIVE CELL AREA	TOTAL C_{pd}‡ (pF)	MAXIMUM I_{CC} (nA)	
					SN54ASC'	SN74ASC'
AN210LH	1.5	1	1.5	0.9	194	11.6
IV110LH	0.75	1	0.75	0.44	105	6.32
IV140LH	1.5	1	1.5	1.61	190	11.4
R2401LH	39.4	2	50.5	20.6	6142	370
TOTALS		5	54.25	23.55	6631	400
Label: S164LH A,B,CLK,CLRZ,QA,QB,QC,QD,QE,QF,QG,QH;						

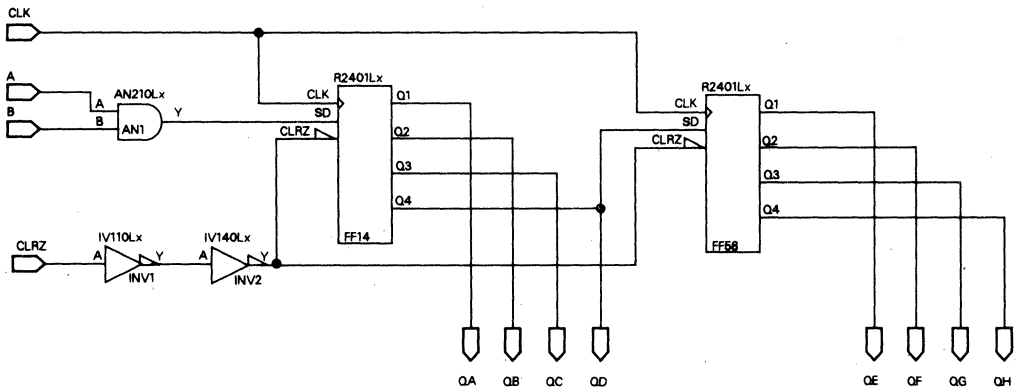
‡The equivalent power dissipation capacitance does not include interconnect capacitance.

The SN54ASC164 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC164 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

INPUTS				OUTPUTS		
CLR	CLK	A	B	QA	QB . . . QH	
L	X	X	X	L	L	L
H	L	X	X	QA_0	QB_0	QH_0
H	↑	H	H	H	QA_n	QG_n
H	↑	L	X	L	QA_n	QG_n
H	↑	X	L	L	QA_n	QG_n

logic diagram



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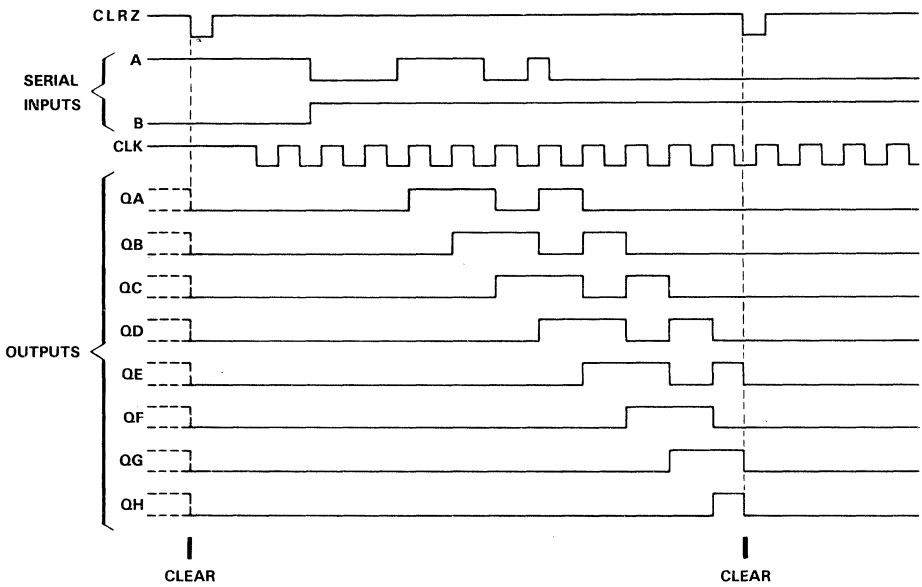
typical clear, shift, and clear sequences



absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

electrical characteristics

PARAMETER			TEST CONDITIONS	SN54ASC164 TYP	SN54ASC164 MAX	SN74ASC164 TYP	SN74ASC164 MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current		V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN or MAX		6631		400	nA
C_i	Input capacitance	A, B	V_{CC} = 5 V, T_A = 25°C	0.13		0.13		pF
		CLK		0.48		0.48		
		CLRZ		0.12		0.12		
C_{pd}	Equivalent power dissipation capacitance†		V_{CC} = 5 V, T_A = 25°C, t_r = t_f = 3 ns,	23.55		23.55		pF

† The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 1)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC164			SN74ASC164			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{pd}	CLK	Qn	C_L = 0		5	11.2		5	10.2	ns
t_{PHL}	CLRZ	Qn			4	7.7		4	7.5	ns
Δt_{pd}	CLK or CLRZ	Qn		0.3	0.5	1.3	0.3	0.5	1.1	ns/pF

†Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{pd} ≡ propagation delay time, low-to-high- or high-to-low-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{pd} ≡ change in t_{pd} with load capacitance
‡Typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: These switching characteristics are simulations of the software macro cell using interconnect capacitance values for an array design having 2,000 gates. Post-layout simulation uses actual interconnect capacitance values.

DESIGN CONSIDERATIONS

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

The HDL for this soft macro is included as a part of the library supplied for supported engineering workstations so that a single label can be developed to apply the macro as needed.The following printout of the HDL block definition is furnished for reference.

HDL FILE

```
BLOCK S164LH;
A           @INPUT;
B           @INPUT;
CLK         @INPUT;
CLRZ        @INPUT;
QA          @OUTPUT;
QB          @OUTPUT;
QC          @OUTPUT;
QD          @OUTPUT;
QE          @OUTPUT;
QF          @OUTPUT;
QG          @OUTPUT;
QH          @OUTPUT;

STRUCTURE
AN1         :AN210LH        A,B,AN1O;
INV1        :IV110LH        CLRZ,INV1O;
INV2        :IV140LH        INV1O,INV2O;
FF14        :R2401LH        INV2O,AN1O,CLK,QA,QB,QC,QD;
FF58        :R2401LH        INV2O,QD,CLK,QE,QF,QG,QH;
END S164LH;
```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shift definition

These registers are unidirectional with respect to shift operations. Bidirectional registers are available in software macros or can be constructed using the 'ASC2405 through 'ASC2407 4-bit predesigned registers.

designing for testability

Designers employing storage or bistable elements, especially long registers (ripple or synchronous), should consider testability of the design in its final form. The need to preset or clear, and read intermediate stages of these elements should be assessed throughout the development of custom logic circuits with these considerations extended to the end-equipment application with respect to maintainability. Simple actions on the part of the ASIC designer can result in considerable cost savings, allowing the expense of IC testing, system testing, and system maintenance to be reduced significantly.

power-up clear/preset

Standard cell storage elements containing the capability to be asynchronously preset or cleared may be connected to the SN54ASC2320 or SN74ASC2320 power-up clear cell to achieve system initialization. Control of the clear or preset inputs from another system signal in conjunction with the power-up clear can be achieved with an AND gate.

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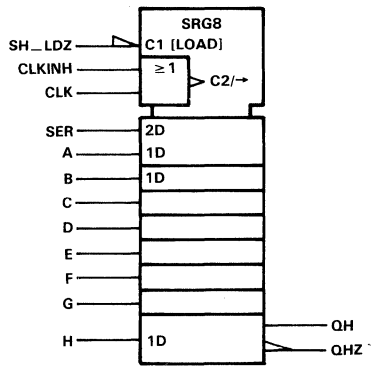
SystemCell™ 2-μm SOFTWARE MACRO CELL

- **Gated (Enable/Inhibit) Clock Inputs**
- **Complementary Outputs**
- **Direct Overriding Load (Data) Inputs**
- **Parallel-to-Serial Data Conversion**
- **Clock Driver Provides Clock Buffering**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The SN54ASC165 and SN74ASC165 are standard-cell software macros implementing 8-bit parallel-in shift registers. The 8-bit configuration provides the custom IC designer a register to embed in ASICs in its most efficient form. Its 8-bit length simplifies construction of large registers. The 'ASC165 implements a shift sequence identical with that performed by packaged 'HC165 and 'LS165 registers.

The 'ASC165 is an 8-bit serial shift register that, when clocked, shifts the data toward serial output QH. Parallel-in access to each stage is provided by eight individual direct data inputs that are enabled by a low level at the SH_LDZ input. The 'ASC165 also features a clock-inhibit function and a complementary serial output QHZ. The 'ASC165 is implemented with the standard cell functions indicated. The HDL netlist label for this software macro is shown on the last line of the following table:

CELL NAME	RELATIVE CELL AREA TO NA210LH	NO. USED	TOTAL RELATIVE CELL AREA	TOTAL C_{pd}‡ (pF)	MAXIMUM I_{CC} (nA)	
					SN54ASC'	SN74ASC'
AO221LH	2.7	1	2.7	0.59	224	13.4
DFB20LH	7.7	8	61.6	30.08	7472	448
IV140LH	1.5	2	3	3.24	380	22.8
NA210LH	1	16	16	8.16	2096	125.44
TOTALS		27	83.3	42.07	10172	610
Label: S165LH A,B,C,D,E,F,G,H,CLK,CLKINH,SH_LDZ,SER,QH,QHZ;						

‡ The equivalent power dissipation capacitance does not include interconnect capacitance.

Clocking is accomplished by a low-to-high transition of the CLK input while SH_LDZ is held high and CLKINH is held low. The functions of the CLK and CLKINH inputs are interchangeable. Since a low CLK input and a low-to-high transition of CLKINH will also accomplish clocking, CLKINH should be changed to the high level only while the CLK input is high. Parallel loading is inhibited when SH_LDZ is held high. The parallel inputs to the register are enabled while SH_LDZ is low independently of the levels of CLK, CLKINH, or SER inputs.

The SN54ASC165 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC165 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

INPUTS			FUNCTION
SH_LDZ	CLK	CLKINH	
L	X	X	Parallel load A thru H
H	H	X	No change
H	X	H	No change
H	L	↑	Shift
H	↑	L	Shift

Shift = Content of each internal register shifts toward serial output QH. Data at serial input is shifted into first register.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

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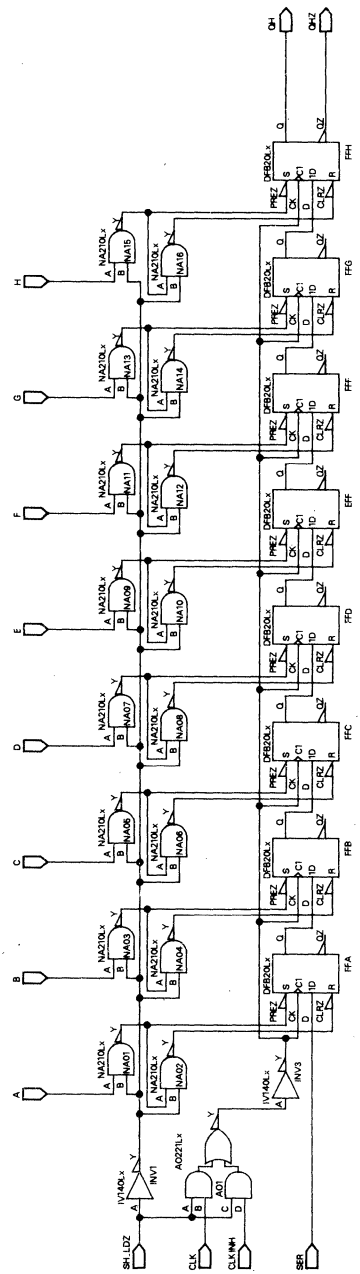
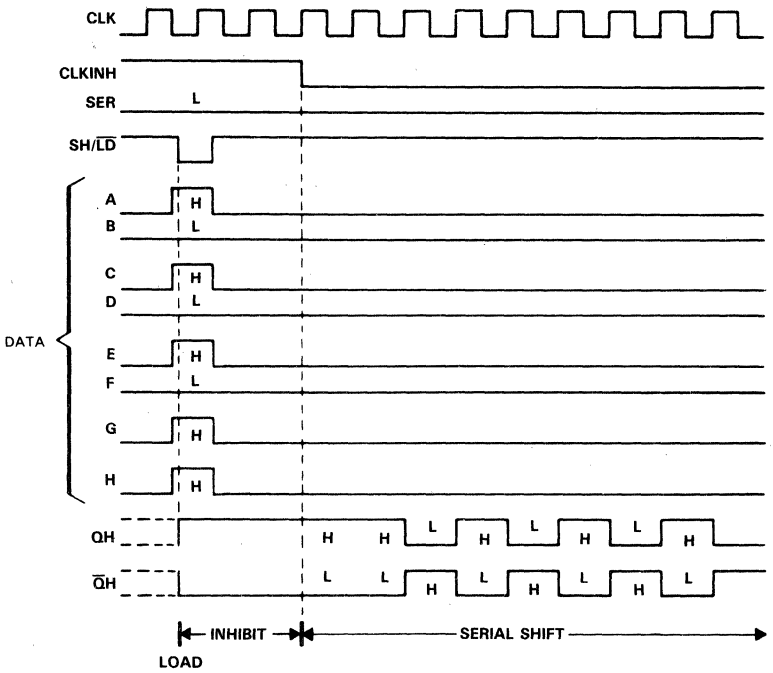
logic diagram



typical shift, load, and inhibit sequences



electrical characteristics

PARAMETER			TEST CONDITIONS	SN54ASC165 TYP	SN54ASC165 MAX	SN74ASC165 TYP	SN74ASC165 MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current		V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		10172		610	nA
C_i	Input capacitance	A thru H	V_{CC} = 5 V, T_A = 25°C	0.12		0.12		pF
		CLK,CLKINH		0.13		0.13		
		SER		0.11		0.11		
		SH_LDZ		0.75		0.75		
C_{pd}	Equivalent power dissipation capacitance†		V_{CC} = 5 V, t_r = t_f = 3 ns, T_A = 25°C	42.07		42.07		pF

† The equivalent power dissipation capacitance does not include interconnect capacitance.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 1)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC165			SN74ASC165			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{pd}	SH_LDZ	QH,QHZ	C_L = 0		7	15.5		7	14.1	ns
t_{pd}	CLK	QH,QHZ			8	19.5		8	17.4	ns
t_{pd}	H	QH,QHZ			4	7.8		4	7.2	ns
Δt_{pd}	Any	Qn		0.1	0.5	1.3	0.1	0.5	1.2	ns/pF

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{pd} ≡ propagation delay time, low-to-high- or high-to-low-level output
Δt_{pd} ≡ change in t_{pd} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: These switching characteristics are simulations of the software macro cell using interconnect capacitance values for an array design having 2,000 gates. Post-layout simulation uses actual interconnect capacitance values.

DESIGN CONSIDERATIONS

All inputs to cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

The HDL for this software macro is included as a part of the library supplied for supported engineering workstations so that a single label can be developed to apply the macro as needed. The following printout of the HDL block definition is furnished for reference.

HDL FILE

```
BLOCK S165LH;
A           @INPUT;
B           @INPUT;
C           @INPUT;
D           @INPUT;
E           @INPUT;
F           @INPUT;
G           @INPUT;
H           @INPUT;
CLK         @INPUT;
CLKINH      @INPUT
SH_LDZ      @INPUT;
SER         @INPUT;
QH          @OUTPUT;
QHZ         @OUTPUT;
```

HDL FILE (Continued)

```
STRUCTURE
A01      :AO221LH    SH_LDZ,CLK,SH_LDZ,CLKINH,AO1O;
FFA      :DFB20LH    NA02O,NA01O,SER,INV3O,FFAQ,DUM;
FFB      :DFB20LH    NA04O,NA03O,FFAQ,INV3O,FFBQ,DUM;
FFC      :DFB20LH    NA06O,NA05O,FFBQ,INV3O,FFCQ,DUM;
FFD      :DFB20LH    NA08O,NA07O,FFCQ,INV3O,FFDQ,DUM;
FFE      :DFB20LH    NA10O,NA09O,FFDQ,INV3O,FFEQ,DUM;
FFF      :DFB20LH    NA12O,NA11O,FFEQ,INV3O,FFFQ,DUM;
FFG      :DFB20LH    NA14O,NA13O,FFFQ,INV3O,FFGQ,DUM;
FFH      :DFB20LH    NA16O,NA15O,FFGQ,INV3O,QH,QHZ;
INV1     :IV140LH    SH_LDZ,INV1O;
INV3     :IV140LH    AO1O,INV3O;
NA01     :NA210LH    A,INV1O,NA01O;
NA02     :NA210LH    NA01O,INV1O,NA02O;
NA03     :NA210LH    B,INV1O,NA03O;
NA04     :NA210LH    NA03O,INV1O,NA04O;
NA05     :NA210LH    C,INV1O,NA05O;
NA06     :NA210LH    NA05O,INV1O,NA06O;
NA07     :NA210LH    D,INV1O,NA07O;
NA08     :NA210LH    NA07O,INV1O,NA08O;
NA09     :NA210LH    E,INV1O,NA09O;
NA10     :NA210LH    NA09O,INV1O,NA10O;
NA11     :NA210LH    F,INV1O,NA11O;
NA12     :NA210LH    NA11O,INV1O,NA12O;
NA13     :NA210LH    G,INV1O,NA13O;
NA14     :NA210LH    NA13O,INV1O,NA14O;
NA15     :NA210LH    H,INV1O,NA15O;
NA16     :NA210LH    NA15O,INV1O,NA16O;
END S165LH;
```


shift definition

These registers are unidirectional with respect to shift operations and the relationship for shifting left or right is defined by the IC designer. Bidirectional registers are available in software macros or can be constructed using the 'ASC2405 through 'ASC2407 4-bit predesigned registers.

designing for testability

Designers employing storage or bistable elements, especially long registers (ripple or synchronous), should consider testability of the design in its final form. The need to preset or clear and read intermediate stages of these elements should be assessed throughout the development of custom logic circuits with these considerations extended to the end-equipment application with respect to maintainability. Simple actions on the part of the ASIC designer can result in considerable cost savings, allowing the expense of IC testing, system testing, and system maintenance to be reduced significantly.

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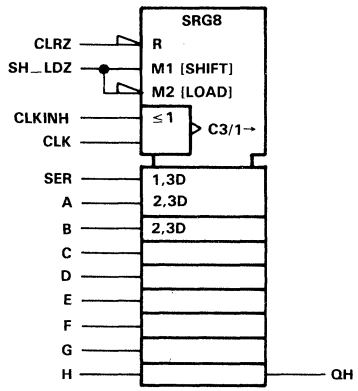
D2939, AUGUST 1986

SystemCell™ 2-μm SOFTWARE MACRO CELL

- **Synchronous Load**
- **Direct Overriding Clear**
- **Parallel-to-Serial Conversion**
- **Direct Clear**
- **Embedded Clock Drivers Provide Clock Buffering**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The SN54ASC166 and SN74ASC166 are standard-cell software macros implementing 8-bit parallel-in shift registers. The 8-bit configuration provides the custom IC designer a register to embed in ASICs in its most efficient form. Its 8-bit length simplifies construction of large counters. The 'ASC166 implements a shift sequence identical with that performed by packaged 'HC166 and 'LS166 registers.

The 'ASC166 is an 8-bit serial shift register that, when clocked, shifts the data toward serial output QH. Parallel-in access to each stage is provided by eight individual direct data inputs that are enabled by a low level at the SH_LDZ input. The 'ASC166 also features a clock inhibit function and a direct clear input. The 'ASC166 is implemented with the standard cell functions indicated. The HDL netlist label for this software macro is shown on the last line of the following table:

CELL NAME	RELATIVE CELL AREA TO NA210LH	NO. USED	TOTAL RELATIVE CELL AREA	TOTAL C_{pd}‡ (pF)	MAXIMUM I_{CC} (nA)	
					SN54ASC'	SN74ASC'
AN221LH	2.7	8	21.6	4.72	1792	107.2
IV110LH	0.75	9	6.75	3.96	945	56.88
IV120LH	1	2	2	1.6	262	15.7
IV140LH	1.5	1	1.5	1.61	190	11.4
OR210LH	1.5	1	1.5	0.86	185	11.1
R2405LH	23.25	2	46.5	20.4	5294	318
TOTALS		23	79.85	33.15	8668	521
Label: S166LH A,B,C,D,E,F,G,H,CLK,CLKINH,SER,SH_LDZ,CLRZ,QH;						

‡The equivalent power dissipation capacitance does not include interconnect capacitance.

The parallel-in-or serial-in modes are established by the shift/load input. When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. When the shift load input is low, the parallel (broadside) data inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high-level edge of the clock pulse through a two-input positive NOR gate permitting one input to be used as a clock-enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This allows the system clock to be free-running and the register can be stopped on command with the other clock input. The clock-inhibit input should be changed to the high level only when the clock input is high. A direct clear input, when taken low, overrides all other inputs, including the clock, and resets all flip-flops to zero.

The SN54ASC166 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC166 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

INPUTS						INTERNAL OUTPUTS		OUTPUT
CLRZ	SH_LDZ	CLKINH	CLK	SER	A. . .H	QA	QB	QH
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	QA_0	QB_0	QH_0
H	L	L	↑	X	a. . .h	a	b	h
H	H	L	↑	H	X	H	QA_n	QG_n
H	H	L	↑	L	X	L	QA_n	QG_n
H	X	H	↑	X	X	QA_0	QB_0	QH_0

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

TEXAS INSTRUMENTS
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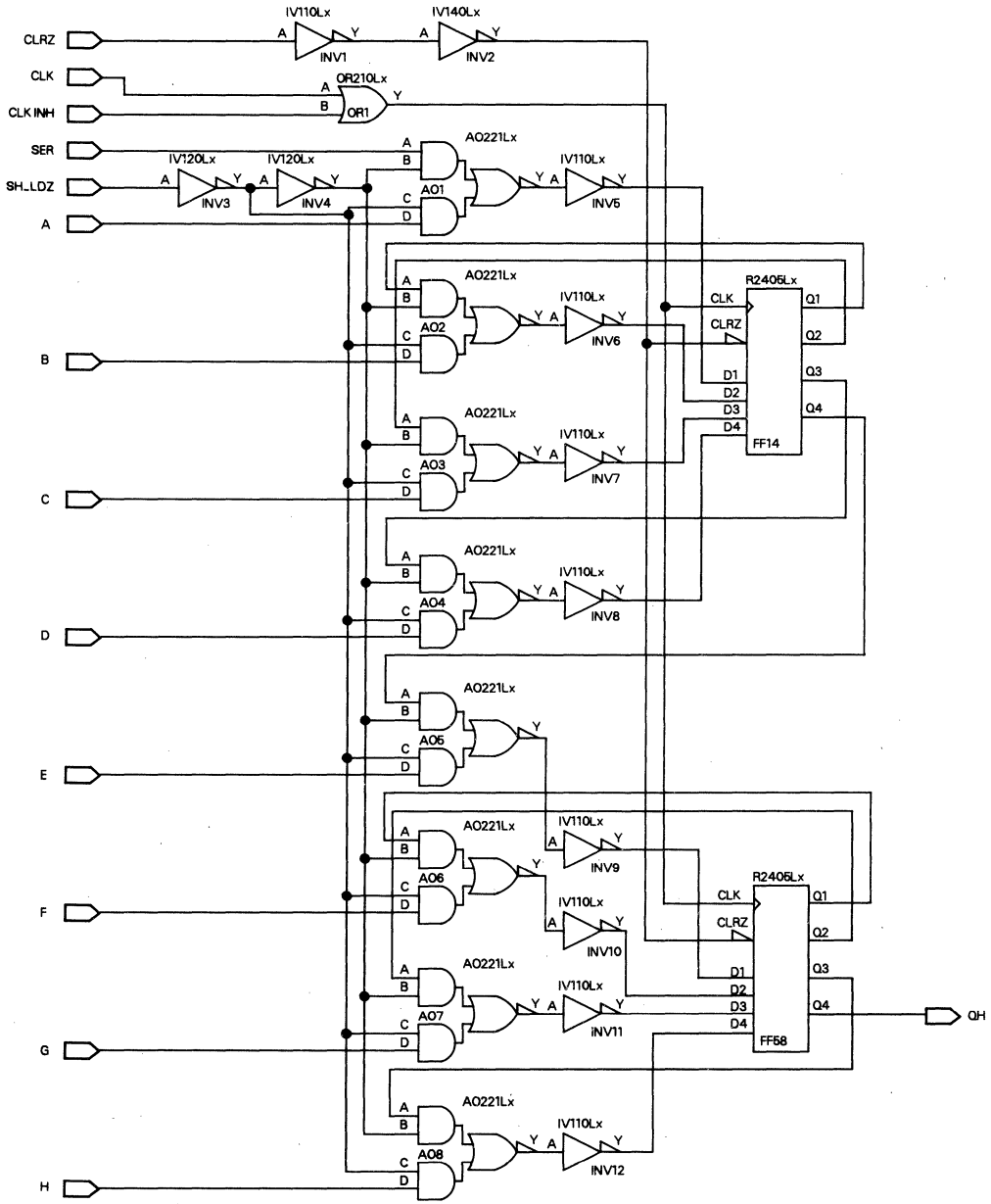
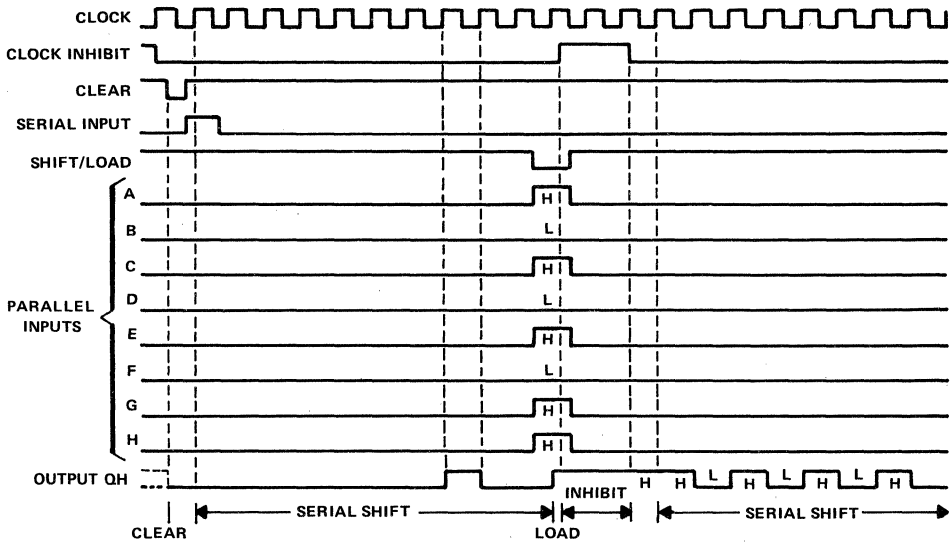
logic diagram



typical clear, shift, load, inhibit, and shift sequences



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electrical characteristics

PARAMETER			TEST CONDITIONS	SN54ASC166		SN74ASC166		UNIT
				TYP	MAX	TYP	MAX	
V_T	Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current		V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		8668		521	nA
C_i	Input capacitance	A thru H	V_{CC} = 5 V, T_A = 25°C	0.13		0.13		pF
		CLK,CLKINH		0.11		0.11		
		SER		0.13		0.13		
		SH_LDZ		0.24		0.24		
C_{pd}	Equivalent power dissipation capacitance†		V_{CC} = 5 V, T_A = 25°C, t_r = t_f = 3 ns,	33.03		33.03		pF

† The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 1)

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC166			SN74ASC166			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
t_{pd}	CLK	QH	C_L = 0			12.5			11.3	ns
t_{PHL}	CLRZ	QH				7.7			7.1	ns
Δt_{pd}	Any	QH		0.3	0.9	2.3	0.3	0.9	2.1	ns/pF
Δt_{PHL}	CLRZ	QH		0.3	0.7	1.9	0.3	0.7	1.6	ns/pF

‡ Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{pd} ≡ propagation delay time, low-to-high or high-to-low-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{pd} ≡ change in t_{pd} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
§ Typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: These switching characteristics are simulations of the software macro cell using interconnect capacitance values for an array design having 2,000 gates. Post-layout simulation uses actual interconnect capacitance values.

DESIGN CONSIDERATIONS

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

The HDL for this software macro is included as a part of the library supplied for supported engineering workstations so that a single label can be developed to apply the macro as needed. The following printout of the HDL block definition is furnished for reference.

HDL FILE

```
BLOCK S166LH;
A           @INPUT;
B           @INPUT;
C           @INPUT;
D           @INPUT;
E           @INPUT;
F           @INPUT;
G           @INPUT;
H           @INPUT;
CLK         @INPUT;
CLKINH      @INPUT;
SER         @INPUT;
SH_LDZ      @INPUT;
CLRZ        @INPUT;
QH          @OUTPUT;

STRUCTURE
AO1         :AO221LH      SER,INV4O,INV3O,A,AO1O;
AO2         :AO221LH      QA,INV4O,INV3O,B,AO2O;
AO3         :AO221LH      QB,INV4O,INV3O,C,AO3O;
AO4         :AO221LH      QC,INV4O,INV3O,D,AO4O;
AO5         :AO221LH      QD,INV4O,INV3O,E,AO5O;
AO6         :AO221LH      QE,INV4O,INV3O,F,AO6O;
AO7         :AO221LH      QF,INV4O,INV3O,G,AO7O;
AO8         :AO221LH      QG,INV4O,INV3O,H,AO8O;
FF14        :R2405LH      INV2O,INV5O,INV6O,INV7O,INV8O,OR1O,QA,QB,QC,QD;
FF58        :R2405LH      INV2O,INV9O,INV10O,INV11O,INV12O,OR1O,QE,QF,QG,QH;
INV1        :IV110LH      CLRZ,INV1O;
INV10       :IV110LH      AO6O,INV10O;
INV11       :IV110LH      AO7O,INV11O;
INV12       :IV110LH      AO8O,INV12O;
INV2        :IV140LH      INV1O,INV2O;
INV3        :IV120LH      SH_LDZ,INV3O;
INV4        :IV120LH      INV3O,INV4O;
INV5        :IV110LH      AO1O,INV5O;
INV6        :IV110LH      AO2O,INV6O;
INV7        :IV110LH      AO3O,INV7O;
INV8        :IV110LH      AO4O,INV8O;
INV9        :IV110LH      AO5O,INV9O;
OR1         :OR210LH      CLK,CLKINH,OR1O;
END S166LH;
```


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shift definition

These registers are unidirectional with respect to shift operations. Bidirectional registers are available in software macros or can be constructed using the 'ASC2405 through 'ASC2407 4-bit predesigned registers.

designing for testability

Designers employing storage or bistable elements, especially long registers (ripple or synchronous), should consider testability of the design in its final form. The need to preset or clear and to read intermediate stages of these elements should be assessed throughout the development of custom logic circuits with these considerations extended to the end-equipment application with respect to maintainability. Simple actions on the part of the ASIC designer can result in considerable cost savings, allowing the expense of IC testing, system testing, and system maintenance to be reduced significantly.

power-up clear

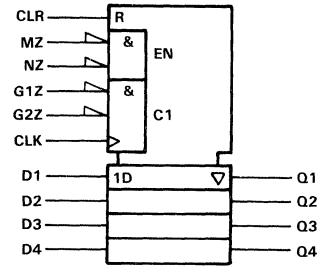
Standard cell storage elements containing the capability to be asynchronously preset or cleared may be connected to the SN54ASC2320 or SN74ASC2320 power-up clear cell to achieve system initialization. Control of the clear or preset inputs from another system signal in conjunction with the power-up clear can be achieved with an AND gate.

D2939, AUGUST 1986

SystemCell™ 2-μm SOFTWARE MACRO CELL

- 3-State Outputs Interface Internal Data Buses Directly
- Direct Clear Input Simplifies Initialization or Pattern Length
- Embedded Clock Driver Provides Symmetrical Performance Across Long Registers
- Parallel Registers for 8-Bit, 16-Bit, 32-Bit Word Widths

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The SN54ASC173 and SN74ASC173 are standard-cell software macros implementing 4-bit D-type register elements designed specifically for interfacing internal bus lines. Their four-bit length means that testability is simplified when constructing large registers. The 'ASC173 implements a function table identical with that performed by packaged 'HC173 and 'LS173 registers.

Gated enable inputs are provided on these macros for controlling the entry of data into the register. When both data enable inputs, GnZ, are low, data at the D inputs are loaded on the next positive transition of the clock input. Buffer output enable inputs, MZ and NZ, are also provided. When both are low, the normal logic states (high or low levels) of the four outputs are impressed on the data bus. The outputs are disabled by a high logic level at either output control input. The outputs then present a high impedance to the internal bus. When the outputs are disabled, sequential operation of the flip-flops is not affected. The 'ASC173 is implemented with the standard cell functions indicated. The HDL netlist label for this software macro is shown on the last line of the following table:

CELL NAME	RELATIVE CELL AREA TO NA210LH	NO. USED	TOTAL RELATIVE CELL AREA	TOTAL C_{pd}‡ (pF)	MAXIMUM I_{CC} (nA)	
					SN54ASC'	SN74ASC'
IV120LH	1	2	2	1.6	262	15.7
IV222LH	2	4	8	3.92	972	58.4
NA210LH	1	12	12	6.12	1572	94.08
NO210PH	1	2	2	0.66	256	15.42
R2406LH	26.25	1	26.25	11.7	2931	176
TOTALS		21	50.25	24	5993	360
Label: S173LH D1,D2,D3,D4,CLK,CLR,G1Z,G2Z,MZ,NZ,Q1,Q2,Q3,Q4;						

‡The equivalent power dissipation capacitance does not include interconnect capacitance.

The SN54ASC173 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC173 is characterized for operation from −40°C to 85°C.

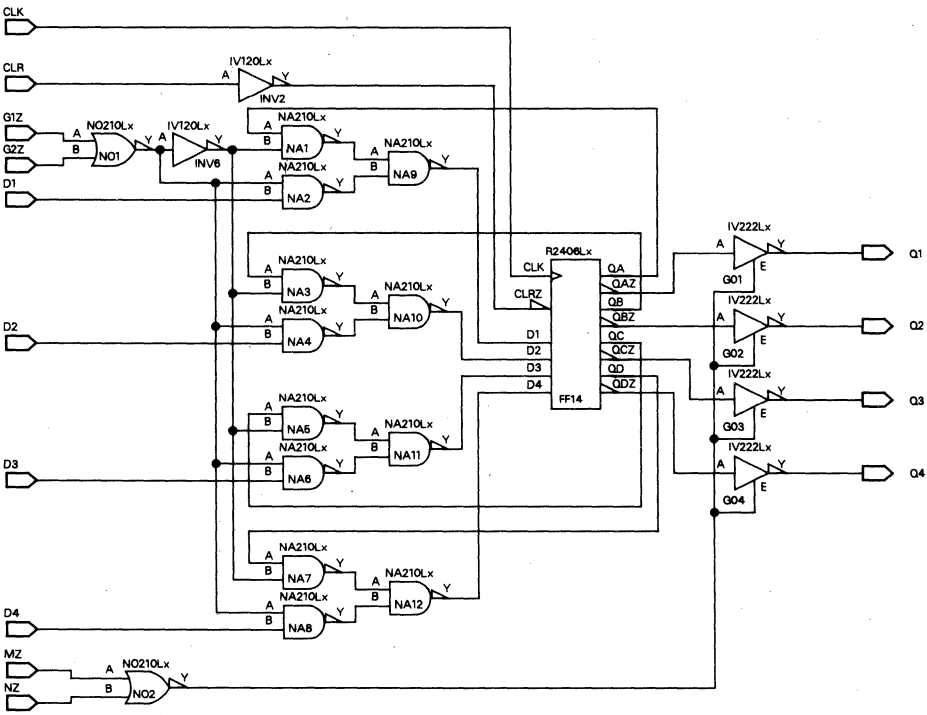
FUNCTION TABLE
(EACH FLIP-FLOP) (see Note 1)

INPUTS					OUTPUT
CLR	CLK	G1Z	G2Z	D	Q
H	X	X	X	X	L
L	L	X	X	X	Q_0
L	↑	H	X	X	Q_0
L	↑	X	H	H	Q_0
L	↑	L	L	L	L
L	↑	L	L	H	H

Q_0 = level of Q before the indicated steady-state input conditions were established.

NOTE 1: When either MZ or NZ (or both) is (are) high, the output is disabled to the high-impedance state; however, sequential operation of the flip-flops is not affected.

logic diagram



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absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements are made during pre-layout simulation that produce workstation output used to identify and resolve each specific timing need.

electrical characteristics

PARAMETER			TEST CONDITIONS	SN54ASC173		SN74ASC173		UNIT
				TYP	MAX	TYP	MAX	
V_T	Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current		V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		5993		360	nA
C_i	Input capacitance	CLR	V_{CC} = 5 V, T_A = 25°C	0.24		0.24		pF
		CLK		0.24		0.24		
		Dn		0.12		0.12		
		GnZ		0.11		0.11		
		MZ, NZ		0.11		0.11		
C_o	Output capacitance		V_{CC} = 5 V, T_A = 25°C	0.33		0.33		pF
C_{pd}	Equivalent power dissipation capacitance†		V_{CC} = 5 V, T_A = 25°C, t_r = t_f = 3 ns,	24		24		pF

† The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Notes 2 and 3)

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC173			SN74ASC173			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
t_{pd}	CLK	Q	C_L = 0		7.1	15.2		7.1	13.8	ns
t_{PHL}	CLR	Q			5.5	11.5		5.5	10.3	ns
t_{en}	MZ, NZ	Q			3.9	8.2		3.9	7.4	ns
Δt_{pd}	Any	Q		0.3	0.9	2.3	0.4	0.9	2.1	ns/pF
Δt_{en}	Any	Q		0.4	0.9	2.3	0.5	0.9	2.1	ns/pF

‡ Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{pd} ≡ propagation delay time, low-to-high or high-to-low output
t_{en} ≡ enable time, high-impedance state to low- or high-logic-level output
t_{PHL} ≡ propagation delay time, high-to-low output
Δt_{pd} ≡ change in t_{pd} with load capacitance
Δt_{en} ≡ change in t_{en} with load capacitance
§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTES: 2. These switching characteristics are simulations of the software macro cell using interconnect capacitance values for an array design having 2,000 gates. Actual performance can be evaluated at post-layout simulation.
3. Enable and delta-enable times are measured using the conditions specified for the 'ASC2311 (IV222LH).

DESIGN CONSIDERATIONS

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

The HDL for this soft macro is included as a part of the library supplied for supported engineering workstations so that a single label can be developed to apply the macro as needed.The following printout of the HDL block definition is furnished for reference.

HDL FILE

```
BLOCK S173LH;
D1          @INPUT;
D2          @INPUT;
D3          @INPUT;
D4          @INPUT;
CLK         @INPUT;
CLR         @INPUT;
G1Z         @INPUT;
G2Z         @INPUT;
MZ          @INPUT;
NZ          @INPUT;
Q1          @OUTPUT;
Q2          @OUTPUT;
Q3          @OUTPUT;
Q4          @OUTPUT;

STRUCTURE
G01         :IV222LH        QAZ,NO2O,Q1;
G02         :IV222LH        QBZ,NO2O,Q2;
G03         :IV222LH        QCZ,NO2O,Q3;
G04         :IV222LH        QDZ,NO2O,Q4;
INV2        :IV120LH        CLR,INV2O;
INV6        :IV120LH        NO1O,INV6O;
NA1         :NA210LH        QA,INV6O,NA1O;
NA10        :NA210LH        NA3O,NA4O,NA10O;
NA11        :NA210LH        NA5O,NA6O,NA11O;
NA12        :NA210LH        NA7O,NA8O,NA12O;
NA2         :NA210LH        NO1O,D1,NA2O;
NA3         :NA210LH        QB,INV6O,NA3O;
NA4         :NA210LH        NO1O,D2,NA4O;
NA5         :NA210LH        QC,INV6O,NA5O;
NA6         :NA210LH        NO1O,D3,NA6O;
NA7         :NA210LH        QD,INV6O,NA7O;
NA8         :NA210LH        NO1O,D4,NA8O;
NA9         :NA210LH        NA1O,NA2O,NA9O;
NO1         :NO210LH        G1Z,G2Z,NO1O;
NO2         :NO210LH        MZ,NZ,NO2O;
FF14        :R2406LH        INV2O,NA9O,NA10O,NA11O,NA12O,CLK,QA,QAZ,QB,QBZ,QC,
                            QCZ,QD,QDZ:

END S173LH;
```


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designing for testability

Designs employing storage or bistable elements, especially long registers (ripple or synchronous), should consider testability of the design in its final form. The need to preset or clear and read intermediate stages of these elements should be assessed throughout the development of custom logic circuits with these considerations extended to the end-equipment application with respect to maintainability. Simple actions on the part of the ASIC designer can result in considerable cost savings, allowing the expense of IC testing, system testing, and system maintenance to be reduced significantly.

power-up clear/preset

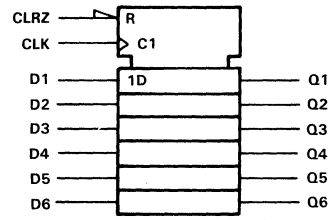
Standard cell storage elements containing the capability to be asynchronously preset or cleared may be connected through an inverter to the SN54ASC2320 or SN74ASC2320 power-up clear cell to achieve system initialization. Control of the clear or preset inputs from another system signal in conjunction with the power-up clear can be achieved with an OR gate.

D2939, AUGUST 1986

SystemCell™ 2-μm SOFTWARE MACRO CELL

- **Six-Bit Register**
- **Direct Clear Input Simplifies Initialization or Pattern Length**
- **Clock Buffer Provides Symmetrical Performance Across Long Registers**

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The SN54ASC174 and SN74ASC174 are standard-cell software macros implementing a 6-bit D-type register element for embedding in ASICs in its most efficient form. Its 6-bit length simplifies construction of large counters. The 'ASC174 implements a function table identical with that performed by packaged 'HC174, 'LS174, and 'F174 registers. It may be customized to meet specific systems requirements.

This software macro reduces the input loading for implementation of larger registers, as standard library cells are used to buffer the clear and clock inputs to further enhance performance across long registers. The 'ASC174 is implemented with the standard cell functions indicated. The HDL netlist label for this software macro is shown on the last line of the following table:

CELL NAME	RELATIVE CELL AREA TO NA210LH	NO. USED	TOTAL RELATIVE CELL AREA	TOTAL C_{pd}‡ (pF)	MAXIMUM I_{CC} (nA)	
					SN54ASC'	SN74ASC'
IV110LH	0.75	2	1.5	0.88	210	12.64
IV140LH	1.5	2	3	3.22	380	22.8
DFC20LH	7.2	6	43.2	20.34	5286	317.4
TOTALS		10	47.7	24.44	5876	353
Label: S174LH D1,D2,D3,D4,D5,D6,CLK,CLRZ,Q1,Q2,Q3,Q4,Q5,Q6;						

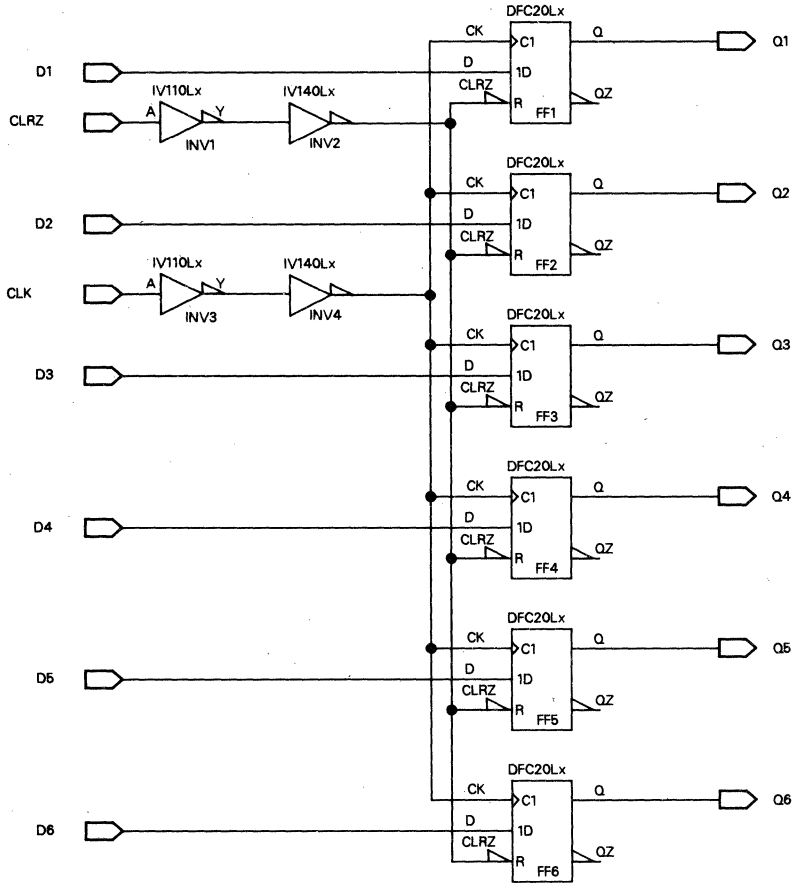
‡The equivalent power dissipation capacitance does not include interconnect capacitance.

The SN54ASC174 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC174 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUT
CLRZ	CLK	Dn	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

logic diagram



absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

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electrical characteristics

PARAMETER		TEST CONDITIONS	SN54ASC174		SN74ASC174		UNIT
			TYP	MAX	TYP	MAX	
V_T Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC} Supply current		V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		5876		353	nA
C_i Input capacitance	CLRZ	V_{CC} = 5 V, T_A = 25°C	0.12		0.12		pF
	Dn		0.11		0.11		
	CLK		0.12		0.12		
C_{pd} Equivalent power dissipation capacitance†		V_{CC} = 5 V, t_r = t_f = 3 ns, T_A = 25°C	24.44		24.44		pF

† The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted) (see Note 1)

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC174			SN74ASC174			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
t_{pd}	CLK	Q	C_L = 0		8	17.4		8	15.6	ns
t_{PHL}	CLRZ	Q			5.1	9.5		5.1	8.8	ns
Δt_{pd}	Any	Q		0.1	0.5	1.1	0.1	0.5	1	ns/pF

‡ Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{pd} ≡ propagation delay time, low-to-high-level or high-to-low-level output
t_{PHL} ≡ propagation delay time, high-to-low output
Δt_{pd} ≡ change in t_{pd} with load capacitance
§ Typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: These switching characteristics are simulations of the software macro cell using interconnect capacitance values for an array design having 2,000 gates. Post-layout simulation uses actual interconnect capacitance values.

DESIGN CONSIDERATIONS

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

The HDL for this software macro is included as a part of the library supplied for supported engineering workstations so that a single label can be developed to apply the macro as needed. The following printout of the HDL block definition is furnished for reference.

HDL FILE

```
BLOCK S174LH;
D1          @INPUT;
D2          @INPUT;
D3          @INPUT;
D4          @INPUT;
D5          @INPUT;
D6          @INPUT;
CLK         @INPUT;
CLRZ        @INPUT;
Q1          @OUTPUT;
Q2          @OUTPUT;
Q3          @OUTPUT;
Q4          @OUTPUT;
Q5          @OUTPUT;
Q6          @OUTPUT;

STRUCTURE
FF1         :DFC20LH        INV2O,D1,INV4O,Q1,DUM:
FF2         :DFC20LH        INV2O,D2,INV4O,Q2,DUM;
FF3         :DFC20LH        INV2O,D3,INV4O,Q3,DUM;
FF4         :DFC20LH        INV2O,D4,INV4O,Q4,DUM;
FF5         :DFC20LH        INV2O,D5,INV4O,Q5,DUM;
FF6         :DFC20LH        INV2O,D6,INV4O,Q6,DUM;
INV1        :IV110LH        CLRZ,INV1O;
INV2        :IV140LH        INV1O,INV2O;
INV3        :IV110LH        CLK,INV3O;
INV4        :IV140LH        INV3O,INV4O;
END S174LH:
```


designing for testability

Designs employing storage or bistable elements, especially long registers (ripple or synchronous), should consider testability of the design in its final form. The need to preset or clear and read intermediate stages of these elements should be assessed throughout the development of custom logic circuits with these considerations extended to the end-equipment application with respect to maintainability. Simple actions on the part of the ASIC designer can result in considerable cost savings, allowing the expense of IC testing, system testing, and system maintenance to be reduced significantly.

power-up clear/preset

Standard cell storage elements containing the capability to be asynchronously preset or cleared may be connected to the SN54ASC2320 or SN74ASC2320 power-up clear cell to achieve system initialization. Control of the clear or preset inputs from another system signal in conjunction with the power-up clear can be achieved with an AND gate.

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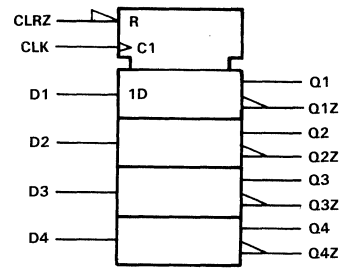
SystemCell™ 2-μm SOFTWARE MACRO CELL

- **Four-Bit Register with Complementary Outputs**
- **Direct Clear Input Simplifies Initialization or Pattern Length**
- **Embedded Clock Driver Provides Clock Buffering**
- **Parallel Latches for 8-Bit, 16-Bit, 32-Bit Word Widths**

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The SN54ASC175 and SN74ASC175 are standard-cell software macros implementing a 4-bit register element for embedding in ASICs. Its 4-bit length simplifies construction of large registers. The 'ASC175 implements a function table identical with that performed by packaged 'HC175, 'LS175, and 'F175 registers.

This macro reduces the input loading for implementation of larger registers, as standard library cells are used to buffer the clear input and the R2406LH register clock input is internally buffered. The 'ASC175 is implemented with the standard cell functions indicated. The HDL netlist label for this software macro is shown on the last line of the following table:

CELL NAME	RELATIVE CELL AREA TO NA210LH	NO. USED	TOTAL RELATIVE CELL AREA	TOTAL C_{pd}‡ (pF)	MAXIMUM I_{CC} (nA)	
					SN54ASC'	SN74ASC'
IV110LH	0.75	1	0.75	0.44	105	6.32
IV140LH	1.5	1	1.5	1.61	190	11.4
R2406LH	26.5	1	26.5	11.69	2931	176
TOTALS		3	28.5	13.74	3226	194
Label: S175LH D1,D2,D3,D4,CLK,CLRZ,Q1,Q1Z,Q2,Q2Z,Q3,Q3Z,Q4,Q4Z;						

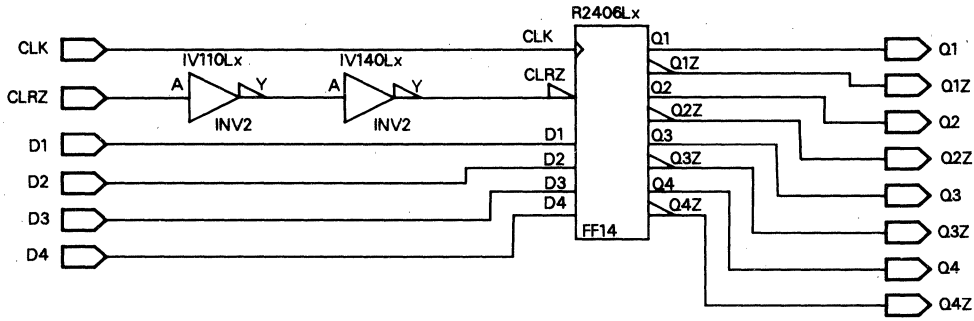
‡ The equivalent power dissipation capacitance does not include interconnect capacitance.

The SN54ASC175 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC175 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUTS	
CLRZ	CLK	Dn	Q	QZ
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

logic diagram



absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

electrical characteristics

PARAMETER		TEST CONDITIONS	SN54ASC175		SN74ASC175		UNIT
			TYP	MAX	TYP	MAX	
V_T Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC} Supply current		V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		3226		194	nA
C_i Input capacitance	CLRZ	V_{CC} = 5 V, T_A = 25°C	0.12		0.12		pF
	Dn		0.13		0.13		
	CLK		0.24		0.24		
C_{pd} Equivalent power dissipation capacitance†		V_{CC} = 5 V, t_r = t_f = 3 ns, T_A = 25°C	13.74		13.74		pF

† The equivalent power dissipation capacitance does not include interconnect capacitance.

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switching characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted) (see Note 1)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC175			SN74ASC175			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{pd}	CLK	Q	C_L = 0		5	10.6		5	9.6	ns
t_{pd}	CLK	$\overline{Q}Z$			5.5	12.5		5.5	11.3	
t_{PLH}	$\overline{CLR}Z$	$\overline{Q}Z$			6	10.4		6	9.4	ns
t_{PHL}	$\overline{CLR}Z$	Q			5.4	8.3		5.4	7.7	
Δt_{pd}	CLK	Q		0.2	0.9	2.3	0.3	0.9	2.1	ns/pF

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{pd} ≡ propagation delay time, low-to-high-level or high-to-low-level output
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{pd} ≡ change in t_{pd} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: These switching characteristics are simulations of the software macro cell using interconnect capacitance values for an array design having 2,000 gates. Post-layout simulation uses actual interconnect capacitance values.

DESIGN CONSIDERATIONS

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

The HDL for this software macro is included as a part of the library supplied for supported engineering workstations so that a single label can be developed to apply the macro as needed. The following printout of the HDL block definition is furnished for reference.

HDL FILE

```
BLOCK S175LH;
D1          @INPUT;
D2          @INPUT;
D3          @INPUT;
D4          @INPUT;
CLK         @INPUT;
CLRZ        @INPUT;
Q1          @OUTPUT;
Q1Z         @OUTPUT;
Q2          @OUTPUT;
Q2Z         @OUTPUT;
Q3          @OUTPUT;
Q3Z         @OUTPUT;
Q4          @OUTPUT;
Q4Z         @OUTPUT;

STRUCTURE
FF14        :R2406LH        INV2O,D1,D2,D3,D4,CLK,Q1,Q1Z,Q2,Q2Z,Q3,Q3Z,Q4,Q4Z;
INV1        :IV110LH        CLRZ,INV1O;
INV2        :IV140LH        INV1O,INV2O;
END S175LH:
```

designing for testability

Designs employing storage or bistable elements, especially long registers (ripple or synchronous), should consider testability of the design in its final form. The need to preset or clear and read intermediate stages of these elements should be assessed throughout the development of custom logic circuits with these considerations extended to the end-equipment application with respect to maintainability. Simple actions on the part of the ASIC designer can result in considerable cost savings, allowing the expense of IC testing, system testing, and system maintenance to be reduced significantly.

power-up clear/preset

Standard cell storage elements containing the capability to be asynchronously preset or cleared may be connected to the SN54ASC2320 or SN74ASC2320 power-up clear cell to achieve system initialization. Control of the clear or preset inputs from another system signal in conjunction with the power-up clear can be achieved with an AND gate.

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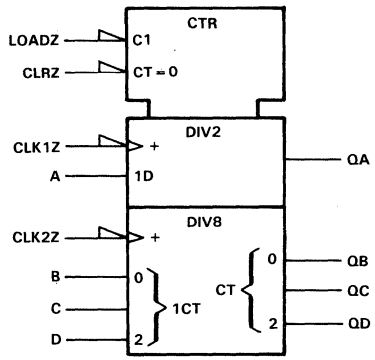
SystemCell™ 2-μm SOFTWARE MACRO CELL

- **Individual 1-Bit and 3-Bit Counters for Implementing Custom Count Sequences**
- **Asynchronous Clear Initializes Sequence Regardless of Mode**
- **Parallel Asynchronously Presettable for Modulo-N Sequences**
- **Performs Ripple-Count or Simple Latching Functions**

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The SN54ASC177 and SN74ASC177 are standard-cell software macros implementing 1-bit and 3-bit ripple counter elements. The overall 4-bit configuration provides the custom IC designer a multifunction counter/latch to embed in ASICs in its most efficient form, and its 4-bit length simplifies construction of large counters. The 'ASC177 implements a count sequence identical with that performed by packaged 'ASC177 counters.

These ripple counters consist of four D-type flip-flops that are interconnected to provide a divide-by-two and a divide-by-eight counter. A divide-by-16 sequence is obtained by connecting the QA output to the CLK2Z input. During the count operation, transfer of information to the outputs occurs on the negative-going edge of the clock pulse. The 'ASC177 is implemented with the standard cell functions indicated. The HDL netlist label for this software macro is shown on the last line of the following table:

CELL NAME	RELATIVE CELL AREA TO NA210LH	NO. USED	TOTAL RELATIVE CELL AREA	TOTAL C_{pd}‡ (pF)	MAXIMUM I_{CC} (nA)	
					SN54ASC'	SN74ASC'
AN220LH	1.75	1	1.75	1.2	228	13.6
DFB20LH	7.7	4	30.8	15.04	3736	224
IV110LH	0.75	3	2.25	1.32	315	18.96
IV140LH	1.5	1	1.5	1.61	190	11.4
NA210LH	1	4	4	2.04	524	31.36
NA310LH	1.25	4	5	2	652	39.12
NO410LH	1.5	1	1.5	0.35	177	10.6
TOTALS		18	46.8	23.56	5822	350
Label: S177LH A,B,C,D,LOADZ,CLRZ,CLK1Z,CLK2Z,QA,QB,QC,QD;						

‡ The equivalent power dissipation capacitance does not include interconnect capacitance.

The counter is fully programmable; that is, it may be preset to any number between 0 and 15. As presetting is asynchronous, a low level at the load input disables the counter and causes the outputs to agree with the setup data independently of the level of the clock input.

These counters may be used as 4-bit latches by using the LOADZ input as the strobe and entering data at the data inputs. The outputs will directly follow the data inputs while LOADZ is low, but will remain unchanged while LOADZ is high and the clock inputs are inactive.

Clearing is asynchronous. A low level at the clear input sets all outputs low regardless of the levels of the clocks or LOADZ.

The SN54ASC177 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC177 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(See Note 1)

INPUTS							OUTPUTS			
CLRZ	LOADZ	D	C	B	A	CLK1Z	QD	QC	QB	QA
L	H	X	X	X	X	X	L	L	L	L
H	L	d	c	b	a	X	d	c	b	a
H	H	X	X	X	X	↑	L	L	L	H
H	H	X	X	X	X	↑	L	L	H	L
H	H	X	X	X	X	↑	L	L	H	H
H	H	X	X	X	X	↑	L	H	L	L
H	H	X	X	X	X	↑	L	H	L	H
H	H	X	X	X	X	↑	L	H	H	L
H	H	X	X	X	X	↑	L	H	H	H
H	H	X	X	X	X	↑	H	L	L	L
H	H	X	X	X	X	↑	H	L	L	H
H	H	X	X	X	X	↑	H	L	H	L
H	H	X	X	X	X	↑	H	L	H	H
H	H	X	X	X	X	↑	H	H	L	L
H	H	X	X	X	X	↑	H	H	L	H
H	H	X	X	X	X	↑	H	H	H	L
H	H	X	X	X	X	↑	H	H	H	H
H	H	X	X	X	X	↑	L	L	L	L
H	H	X	X	X	X	L	Q_0	Q_0	Q_0	Q_0

See Explanation of Function Tables in Section 1.
NOTE 1: Table applies with output QA connectd to CLK2Z input.

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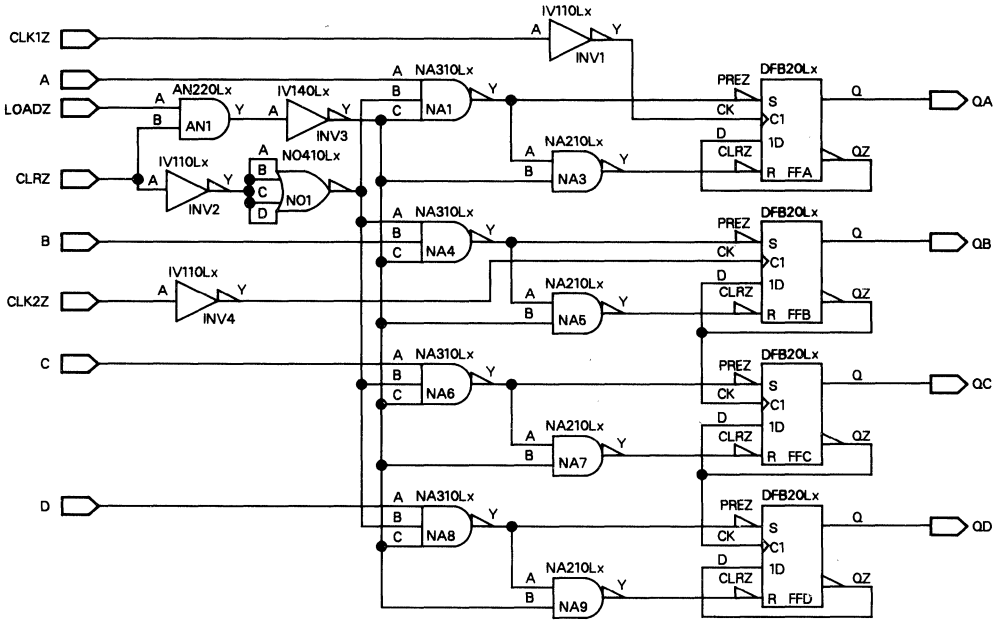
logic diagram



absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

electrical characteristics

PARAMETER			TEST CONDITIONS	SN54ASC177 TYP	SN54ASC177 MAX	SN74ASC177 TYP	SN74ASC177 MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current		V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		5822		350	nA
C_i	Input capacitance	LOADZ	V_{CC} = 5 V, T_A = 25°C	0.13		0.13		pF
		CLRZ		0.25		0.25		
		All others		0.12		0.12		
C_{pd}	Equivalent power dissipation capacitance†		V_{CC} = 5 V, T_A = 25°C, t_r = t_f = 3 ns,	23.56		23.56		pF

† The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 1)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC177			SN74ASC177			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{pd}	CLK1Z	QA	C_L = 0		6	15		6	13.3	ns
t_{pd}	CLK2Z	QB			6	15		6	13.3	ns
t_{pd}		QC			10	28.1		10	24.9	ns
t_{pd}		QD			16	41.2		16	36.5	ns
t_{pd}	A,B,C,D	Any			5	11.5		5	10.6	ns
t_{pd}	LOADZ	Any			7	13.9		7	12.4	ns
t_{pd}	CLRZ	RCO			5.4	21.3		5.4	19.4	ns
Δt_{pd}	Any	Any		0.1	0.5	1.3	0.1	0.5	1.2	ns/pF

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f = 3$ ns (10% and 90%).
t_{pd} ≡ propagation delay time, low-to-high-level or high-to-low-level output
Δt_{pd} ≡ change in t_{pd} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: These switching characteristics are simulations of the software macro cell using interconnect capacitance values for an array design having 2,000 gates. Post-layout simulation uses actual interconnect capacitance values.

DESIGN CONSIDERATIONS

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

The HDL for this software macro is included as a part of the library supplied for supported engineering workstations so that a single label can be developed to apply the macro as needed. The following printout of the HDL block definition is furnished for reference.

HDL FILE

```
BLOCK S177LH;
A           @INPUT;
B           @INPUT;
C           @INPUT;
D           @INPUT;
LOADZ       @INPUT;
CLRZ        @INPUT;
CLK1Z       @INPUT;
CLK2Z       @INPUT;
QA          @OUTPUT;
QB          @OUTPUT;
QC          @OUTPUT;
QD          @OUTPUT;
```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HDL (Continued)

```
STRUCTURE
AN1         :AN220LH        LOADZ,CLRZ,AN1O;
FFA         :DFB20LH        NA3O,NA1O,FFAQZ,INV1O,QA,FFAQZ;
FFB         :DFB20LH        NA5O,NA4O,FFBQZ,INV4O,QB,FFBQZ;
FFC         :DFB20LH        NA7O,NA6O,FFCQZ,FFBQZ,QC,FFCQZ;
FFD         :DFB20LH        NA9O,NA8O,FFDQZ,FFCQZ,QD,FFDQZ;
INV1        :IV110LH        CLK1Z,INV1O;
INV2        :IV110LH        CLRZ,INV2O;
INV3        :IV140LH        AN1O,INV3O;
INV4        :IV110LH        CLK2Z,INV4O;
NA1         :NA310LH        A,NO1O,INV3O,NA1O;
NA3         :NA210LH        NA1O,INV3O,NA3O;
NA4         :NA310LH        NO1O,B,INV3O,NA4O;
NA5         :NA210LH        NA4O,INV3O,NA5O;
NA6         :NA310LH        C,NO1O,INV3O,NA6O;
NA7         :NA210LH        NA6O,INV3O,NA7O;
NA8         :NA310LH        D,NO1O,INV3O,NA8O;
NA9         :NA210LH        NA8O,INV3O,NA9O;
NO1         :NO410LH        INV2O,INV2O,INV2O,INV2O,NO1O;
END S177LH;
```

count definition

These counters are unidirectional with respect to count operation. Inverting the output levels will produce a down-count sequence. Bidirectional counters are available in software macros or can be constructed using the 'ASC2405 through 'ASC2407 4-bit predesigned registers. Additional single bits can be achieved with predesigned flip-flops offered in TI's standard cell family.

designing for testability

Designers employing storage or bistable elements, especially long counters (ripple or synchronous), should consider testability of the design in its final form. The need to preset or clear and read intermediate stages of these elements should be assessed throughout the development of custom logic circuits with these considerations extended to the end-equipment application with respect to maintainability. Simple actions on the part of the ASIC designer can result in considerable cost savings, allowing the expense of IC testing, system testing, and system maintenance to be reduced significantly.

power-up clear/preset

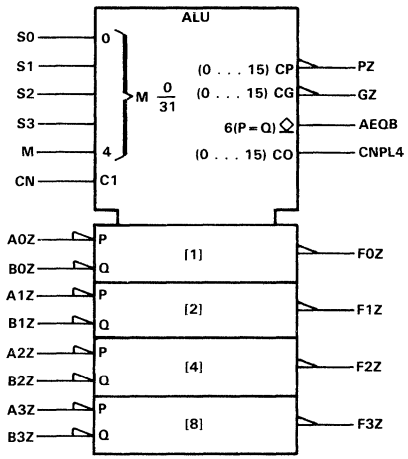
Standard cell storage elements containing the capability to be asynchronously preset or cleared may be connected to the SN54ASC2320 or SN74ASC2320 power-up clear cell to achieve system initialization. Control of the clear or preset inputs from another system signal in conjunction with the power-up clear can be achieved with an AND gate.

D2939, AUGUST 1986

SystemCell™ 2-μm SOFTWARE MACRO CELL

- **Performs Full 16-Function Arithmetic or Boolean Combinations of Two Variables**
- **Arithmetic Operating Modes:**
  - **Addition**
  - **Subtraction**
  - **Shift Operand A One Position**
  - **Magnitude Comparison**
  - **Plus Twelve Other Arithmetic Operations**
- **Logic Function Modes:**
  - **Exclusive-OR**
  - **Comparator**
  - **AND, NAND, OR, NOR**
  - **Plus Ten Other Logic Operations**

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The SN54ASC181 and SN74ASC181 are standard-cell software macro 4-bit arithmetic logic units. The 'ASC181 implements a function table identical with that performed by packaged 'LS181, 'S181, and 'F181 arithmetic logic units/function generators.

The 'ASC181 performs 16 arithmetic or Boolean operations on two 4-bit binary words as shown in Tables 1 and 2. Choice between the two operating modes is established by the mode control, M, and selection of one-of-sixteen operations is accomplished at the select inputs S3, S2, S1, and S0. The 'ASC181 is implemented with the standard cell functions indicated. The HDL netlist label for this software macro is shown on the last line of the following table:

CELL NAME	RELATIVE CELL AREA TO NA210LH	NO. USED	TOTAL RELATIVE CELL AREA	TOTAL C_{pd}‡ (pF)	MAXIMUM I_{CC} (nA)	
					SN54ASC'	SN74ASC'
AN210LH	1.5	9	13.5	8.1	1746	104.4
AN310LH	1.75	9	15.75	9.54	1989	119.7
AN420LH	2.25	1	2.25	1.72	286	17.2
EX210LH	2	4	8	4.48	892	53.6
EX220LH	2.25	4	9	6	1032	62
IV110LH	0.75	8	6	3.52	840	50.56
IV120LH	1	1	1	0.8	131	7.85
NA210LH	1	4	5	2.55	655	39.2
NA220LH	1.5	1	1.5	1	196	11.7
NA310LH	1.25	4	5	2	652	39.12
NA410LH	1.5	6	9	3	1122	67.2
NA510LH	1.75	2	3.5	1.04	426	25.6
NO210LH	1	5	5	1.65	640	38.55
NO310LH	1.25	4	5	1.28	624	37.32
TOTALS		62	89.5	46.68	11231	675
Label: S181LH A3Z,A2Z,A1Z,A0Z,B3Z,B2Z,B1Z,B0Z,CN,M,S3,S2,S1,S0,F3Z,F2Z, F1Z,F0Z,AEQB,GZ,PZ,CNPL4;						

‡The equivalent power dissipation capacitance does not include interconnect capacitance.

When the mode control input is low, the 16 arithmetic operations are accessible via the four select inputs. The 4-bit full adder incorporates both ripple and look-ahead carry circuitry, providing the capability to extend either technique across expanded word widths when multiple 'ASC181s are used in parallel.

The 'ASC181 accommodates both active-high and active-low data simply by redefining the designations used to describe the data inputs and outputs. For use with active-low data, use Table 1 and the input/output designations provided for the label developed above. For use with active-high data, use Table 2.

Note that only the relationships of A, B, and F data with respect to the carry and look-ahead circuitry are affected.

Subtraction is accomplished by 1's complement addition in which the 1's complement of the subtrahend is generated internally. The resultant output is A-B-1, which requires an end-around or forced carry to provide A-B. Arithmetic operations with and without carry are shown in Tables 1 and 2.

The 'ASC181 also performs a comparison of the A and B operands. The AEQB output is decoded from the function outputs (F3, F2, F1, and F0) so that, when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A = B). The ALU must be in the subtract mode with CN = H when performing this comparison. The AEQB output can be AND- or NAND-gated to perform comparisons over expanded ALUs. The CNPL4 carry output can also be used to supply relative magnitude information. Again, the ALU must be in the subtract mode by having the select inputs S3, S2, S1, and S0 at L, H, H, L, respectively.

INPUT CN	OUTPUT CNPL4	ACTIVE-LOW DATA (FIGURE 1)	ACTIVE-HIGH DATA (FIGURE 2)
H	H	A≥B	A≤B
H	L	A<B	A>B
L	H	A>B	A<B
L	L	A≤B	A≥B

The SN54ASC181 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC181 is characterized for operation from −40°C to 85°C.

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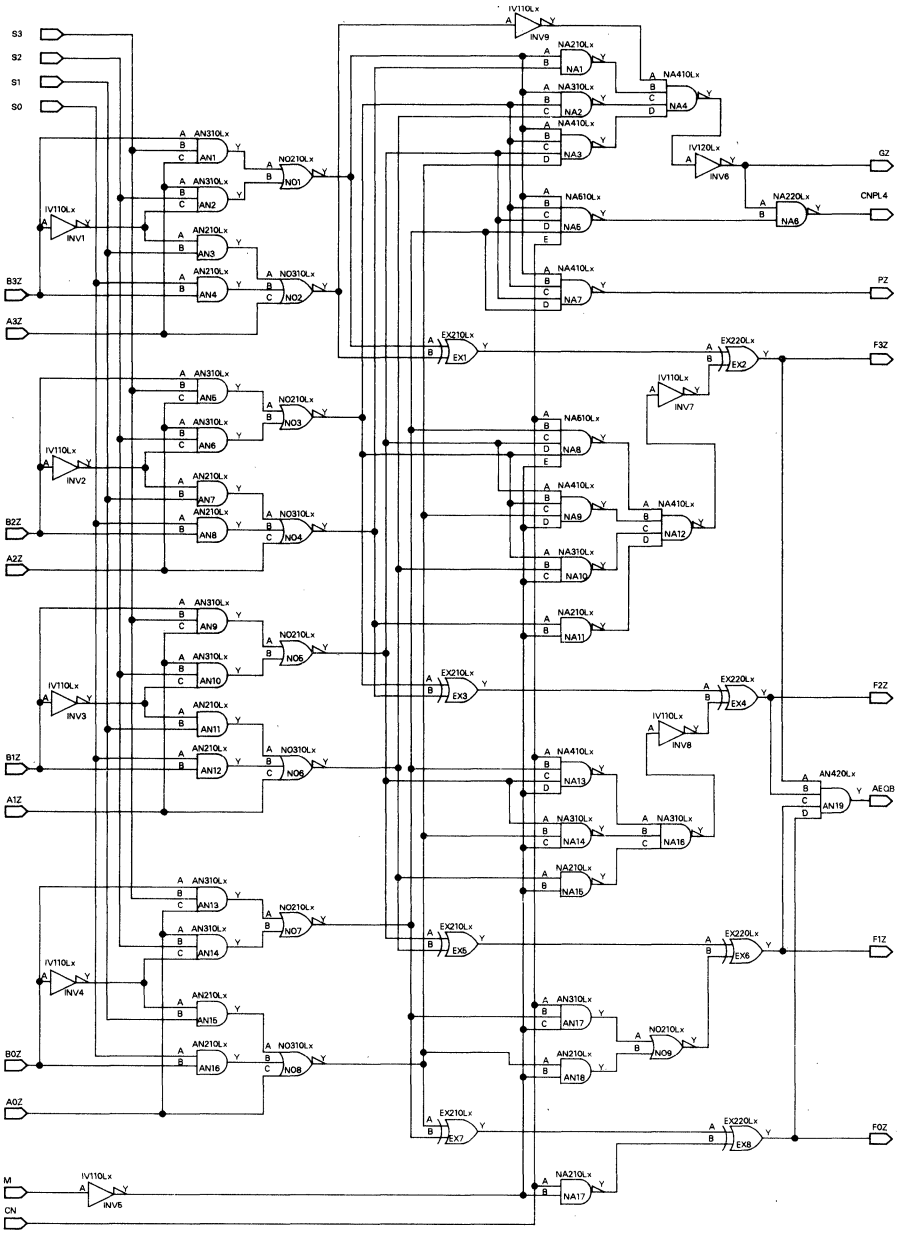
logic diagram



signal designations

The polarity indicators (open arrowheads) in both Figures 1 and 2 indicate that the associated input or output is active-low with respect to the function shown inside the symbol, and the symbols are the same in both figures. The signal designations in Figure 1 agree with the indicated internal functions based on active-low data and are for use with the logic functions and arithmetic operations shown in Table 1. The signal designations used in Figure 2 accommodate the logic functions and arithmetic operations for the active-high data given in Table 2.

FIGURE 1

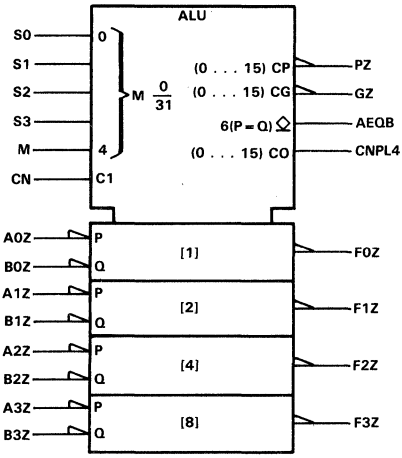


FIGURE 2

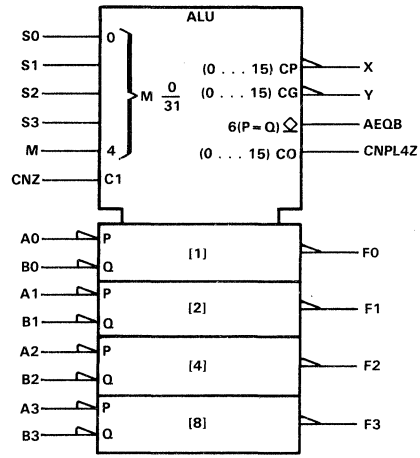


TABLE 1

SELECTION				ACTIVE-LOW DATA		
				M = H	M = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC FUNCTIONS	CN = L (no carry)	CN = H (with carry)
L	L	L	L	F = $\overline{A}$	F = A MINUS 1	F = A
L	L	L	H	F = $\overline{AB}$	F = AB MINUS 1	F = AB
L	L	H	L	F = $\overline{A}$ + B	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
L	L	H	H	F = 1	F = MINUS 1 (2's COMP)	F = ZERO
L	H	L	L	F = $\overline{A + B}$	F = A PLUS (A + $\overline{B}$)	F = A PLUS (A + $\overline{B}$) PLUS 1
L	H	L	H	F = $\overline{B}$	F = AB PLUS (A + $\overline{B}$)	F = AB PLUS (A + $\overline{B}$) PLUS 1
L	H	H	L	F = $\overline{A \oplus B}$	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	F = A + $\overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
H	L	L	L	F = $\overline{A}$B	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1
H	L	L	H	F = A $\oplus$ B	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = A$\overline{B}$ PLUS (A + B)	F = A$\overline{B}$ PLUS (A + B) PLUS 1
H	L	H	H	F = A + B	F = (A + B)	F = (A + B) PLUS 1
H	H	L	L	F = 0	F = A PLUS A*	F = A PLUS A PLUS 1
H	H	L	H	F = A$\overline{B}$	F = AB PLUS A	F = AB PLUS A PLUS 1
H	H	H	L	F = AB	F = A$\overline{B}$ PLUS A	F = A$\overline{B}$ PLUS A PLUS 1
H	H	H	H	F = A	F = A	F = A PLUS 1

*Each bit is shifted to the next more significant position.

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TABLE 2

SELECTION				ACTIVE-HIGH DATA		
				M = H	M = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC FUNCTIONS	CNZ = H (no carry)	CNZ = L (with carry)
L	L	L	L	F = $\overline{A}$	F = A	F = A PLUS 1
L	L	L	H	F = $\overline{A + B}$	F = A + B	F = (A + B) PLUS 1
L	L	H	L	F = $\overline{A}B$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
L	L	H	H	F = 0	F = MINUS 1 (2's COMP)	F = ZERO
L	H	L	L	F = $\overline{AB}$	F = A PLUS A$\overline{B}$	F = A PLUS A$\overline{B}$ PLUS 1
L	H	L	H	F = $\overline{B}$	F = (A + B) PLUS A$\overline{B}$	F = (A + B) PLUS A$\overline{B}$ PLUS 1
L	H	H	L	F = A ⊕ B	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	F = A$\overline{B}$	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
H	L	L	L	F = $\overline{A}$ + B	F = A PLUS AB	F = A PLUS AB PLUS 1
H	L	L	H	F = $\overline{A \oplus B}$	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = (A + $\overline{B}$) PLUS AB	F = (A + $\overline{B}$) PLUS AB PLUS 1
H	L	H	H	F = AB	F = AB MINUS 1	F = AB
H	H	L	L	F = 1	F = A PLUS A*	F = A PLUS A PLUS 1
H	H	L	H	F = A + $\overline{B}$	F = (A + B) PLUS A	A = (A + B) PLUS A PLUS 1
H	H	H	L	F = A + B	F = (A + $\overline{B}$) PLUS A	F = (A + $\overline{B}$) PLUS A PLUS 1
H	H	H	H	F = A	F = A MINUS 1	F = A

*Each bit is shifted to the next more significant position.

maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS	SN54ASC181		SN74ASC181		UNIT
				TYP	MAX	TYP	MAX	
V_T	Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current		V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN or MAX		11231		675	nA
C_i	Input capacitance	An, Bn	V_{CC} = 5 V, T_A = 25°C	0.36		0.36		pF
		Sn		0.5		0.5		
		M		0.12		0.12		
		CN		0.6		0.6		
C_{pd}	Equivalent power dissipation capacitance†		V_{CC} = 5 V, T_A = 25°C, t_r = t_f = 3 ns,	46.68		46.68		pF

† The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 1)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC181			SN74ASC181			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{pd}	CN	CNPL4			3	8		3	7	ns
t_{pd}	AnZ or BnZ	CNPL4	SUM mode		7	15		7	14	ns
t_{pd}			DIFF mode							
t_{pd}	CN	Fn	SUM or DIFF		7	14.4		7	12.9	ns
t_{pd}	AnZ or BnZ	GZ	SUM mode		6	13.8		6	12.8	ns
t_{pd}			DIFF mode							
t_{pd}	AnZ or BnZ	PZ	SUM mode		7	15.4		7	14.1	ns
t_{pd}			DIFF mode							
t_{pd}	AiZ or BiZ	FiZ	SUM mode		12	28		12	25.6	ns
t_{pd}			DIFF mode							
t_{pd}	AnZ or BnZ	AEQB	DIFF mode		13	28.4		13	25.5	ns
Δt_{pd}	Any	CNPL4		0.3	0.6	1.3	0.3	0.6	1.1	ns/pF
Δt_{pd}	AnZ or BnZ	GZ		0.3	0.5	1.1	0.3	0.5	1	ns/pF
Δt_{pd}	AnZ or BnZ	PZ		0.5	1.6	4.8	0.5	1.6	4.1	ns/pF
Δt_{pd}	Any	FiZ		0.3	0.5	1.9	0.3	0.5	1.7	ns/pF
Δt_{pd}	Any	AEQB		0.1	0.5	1.3	0.1	0.5	1.2	ns/pF

†Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f = 3$ ns (10% and 90%).
t_{pd} ≡ propagation delay time, low-to-high or high-to-low-level output
Δt_{pd} ≡ change in t_{pd} with load capacitance
‡Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.
NOTE 1: These switching characteristics are simulations of the software macro cell using interconnect capacitance values for an array design having 2,000 gates. Post-layout simulation uses actual interconnect capacitance values.

DESIGN CONSIDERATIONS

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

The HDL for this soft macro is included as a part of the library supplied for supported engineering workstations so that a single label can be developed to apply the macro as needed. The following printout of the HDL block definition is furnished for reference.

HDL FILE

```
BLOCK S181LH;
A3Z          @INPUT;
A2Z          @INPUT;
A1Z          @INPUT;
A0Z          @INPUT;
B3Z          @INPUT;
B2Z          @INPUT;
B1Z          @INPUT;
B0Z          @INPUT;
CN           @INPUT;
M            @INPUT;
S3           @INPUT;
S2           @INPUT;
S1           @INPUT;
S0           @INPUT;
F3Z          @OUTPUT;
F2Z          @OUTPUT;
F1Z          @OUTPUT;
F0Z          @OUTPUT;
AEQB         @OUTPUT;
GZ           @OUTPUT;
PZ           @OUTPUT;
CNPL4        @OUTPUT;

STRUCTURE
AN1          :AN310LH        B3Z,S3,A3Z,AN1O;
AN10         :AN310LH        A1Z,S2,INV3O,AN10O;
AN11         :AN210LH        INV3O,S1,AN11O;
AN12         :AN210LH        S0,B1Z,AN12O;
AN13         :AN310LH        B0Z,S3,A0Z,AN13O;
AN14         :AN310LH        A0Z,S2,INV4O,AN14O;
AN15         :AN210LH        INV4O,S1,AN15O;
AN16         :AN210LH        S0,B0Z,AN16O;
AN17         :AN310LH        CN,NO7O,INV5O,AN17O;
AN18         :AN210LH        NO8O,INV5O,AN18O;
AN19         :AN420LH        F3Z,F2Z,F1Z,F0Z,AEQB;
AN2          :AN310LH        A3Z,S2,INV1O,AN2O;
AN3          :AN210LH        INV1O,S1,AN3O;
AN4          :AN210LH        S0,B3Z,AN4O;
AN5          :AN310LH        B2Z,S3,A2Z,AN5O;
AN6          :AN310LH        A2Z,S2,INV2O,AN6O;
AN7          :AN210LH        INV2O,S1,AN7O;
AN8          :AN210LH        S0,B2Z,AN8O;
AN9          :AN310LH        B1Z,S3,A1Z,AN9O;
EX1          :EX210LH        NO1O,NO2O,EX1O;
EX2          :EX220LH        EX1O,INV7O,F3Z;
EX3          :EX210LH        NO3O,NO4O,EX3O;
EX4          :EX220LH        EX3O,INV8O,F2Z;
EX5          :EX210LH        NO5O,NO6O,EX5O;
EX6          :EX220LH        EX5O,NO9O,F1Z;
```

HDL FILE (Continued)

STRUCTURE (Continued)

```
EX7         :EX210LH        NO8O,NO7O,EX7O;
EX8         :EX220LH        EX7O,NA17O,F0Z;
INV1        :IV110LH        B3Z,INV1O;
INV2        :IV110LH        B2Z,INV2O;
INV3        :IV110LH        B1Z,INV3O;
INV4        :IV110LH        B0Z,INV4O;
INV5        :IV110LH        M,INV5O;
INV6        :IV120LH        NA4O,GZ;
INV7        :IV110LH        NA12O,INV7O;
INV8        :IV110LH        NA16O,INV8O;
INV9        :IV110LH        NO2O,INV9O;
NA1         :NA210LH        NO1O,NO4O,NA1O;
NA10        :NA310LH        NO3O,NO6O,INV5O,NA10O;
NA11        :NA210LH        NO4O,INV5O,NA11O;
NA12        :NA410LH        NA8O,NA9O,NA10O,NA11O,NA12O;
NA13        :NA410LH        CN,NO7O,NO5O,INV5O,NA13O;
NA14        :NA310LH        NO5O,NO8O,INV5O,NA14O;
NA15        :NA210LH        NO6O,INV5O,NA15O;
NA16        :NA310LH        NA13O,NA14O,NA15O,NA16O;
NA17        :NA210LH        CN,INV5O,NA17O;
NA2         :NA310LH        NO1O,NO3O,NO6O,NA2O;
NA3         :NA410LH        NO1O,NO3O,NO5O,NO8O,NA3O;
NA4         :NA410LH        INV9O,NA1O,NA2O,NA3O,NA4O;
NA5         :NA510LH        NO1O,NO3O,NO5O,NO7O,CN,NA5O;
NA6         :NA220LH        GZ,NA5O,CNPL4;
NA7         :NA410LH        NO1O,NO3O,NO5O,NO7O,PZ;
NA8         :NA510LH        CN,NO7O,NO5O,NO3O,INV5O,NA8O;
NA9         :NA410LH        NO5O,NO3O,NO8O,INV5O,NA9O;
NO1         :NO210LH        AN1O,AN2O,NO1O;
NO2         :NO310LH        AN3O,AN4O,A3Z,NO2O;
NO3         :NO210LH        AN5O,AN6O,NO3O;
NO4         :NO310LH        AN7O,AN8O,A2Z,NO4O;
NO5         :NO210LH        AN9O,AN10O,NO5O;
NO6         :NO310LH        AN11O,AN12O,A1Z,NO6O;
NO7         :NO210LH        AN13O,AN14O,NO7O;
NO8         :NO310LH        AN15O,AN16O,A0Z,NO8O;
NO9         :NO210LH        AN17O,AN18O,NO9O;
END S181LH;
```

intefacing the macro

Inputs and outputs of the predesigned macro are compatible for interfacing directly with cells and macros available in the TI standard cell library.

The inputs can be driven by either noninverting or inverting input cells. The outputs can be interfaced to drive off-chip loads with any of the noninverting output buffers or interfaced to external bidirectional buses through a 3-state input/output TTL/CMOS buffer.

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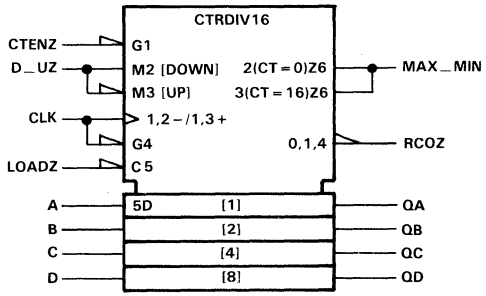
D2939, AUGUST 1986

SystemCell™ 2-μm SOFTWARE MACRO CELL

- **Single Down/Up Control Line**
- **Look-Ahead Circuitry Enhances Performance of Cascaded Counters**
- **Fully Synchronous in Count Mode**
- **Parallel Asynchronous Load for Modulo-N Count Sequences**
- **Count Enable Input for Setting Sequence Start and Stop**

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The SN54ASC191 and SN74ASC191 are standard-cell software macros implementing 4-bit up-down counter elements. The 4-bit configuration provides the custom IC designer a fully designed bidirectional counter to embed in ASICs in its most efficient form, and its 4-bit length means that testability is simplified when constructing large counters. The 'ASC191 implements a count sequence identical with that performed by packaged 'HC191, 'LS191, and 'F191 synchronous counters.

The 'ASC191 is a synchronous, reversible up/down 4-bit binary counter. Synchronous counting operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidentally with each other when so instructed by the steering logic. This mode of operation eliminates output counting spikes normally associated with asynchronous (ripple clock) counters. The 'ASC191 is implemented with the standard cell functions indicated. The HDL netlist label for this software macro is shown on the last line of the following table:

CELL NAME	RELATIVE CELL AREA TO NA210LH	NO. USED	TOTAL RELATIVE CELL AREA	TOTAL C_{pd}‡ (pF)	MAXIMUM I_{CC} (nA)	
					SN54ASC'	SN74ASC'
DFB20LH	7.7	4	30.8	15.04	3736	224
IV110LH	0.75	9	6.75	3.96	945	56.88
IV120LH	1	1	1	0.8	131	7.85
NA210LH	1	26	26	13.26	3406	203.84
NA310LH	1.25	3	3.75	1.5	489	29.34
NA410LH	1.5	2	3	1	374	22.4
NA510LH	1.75	2	3.5	1.04	426	25.6
NO210LH	1	2	2	0.66	256	15.42
TOTALS		49	76.8	37.26	9763	586
Label: S191LH D,C,B,A,CLK,D_UZ,CTENZ,LOADZ,QD,QC,QB,QA,RCOZ,MAX_MIN;						

‡The equivalent power dissipation capacitance does not include interconnect capacitance.

The outputs of the four flip-flops are triggered on a low-to-high-level transition of the clock input if the enable input (CTENZ) is low. A high at CTENZ inhibits counting. The direction of the count is determined by the level of the down/up (D_UZ) input. When D_UZ is low, the counter counts up and when the D_UZ is high, it counts down.

These counters feature a fully-independent clock circuit. Changes at the control inputs (CTENZ and D_UZ) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter will be dictated solely by the conditions meeting the setup and hold times.

These counters are fully programmable, that is, they may be preset to any number between 0 and 15 by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

Two outputs have been made available to perform the cascading function: ripple and maximum/minimum count. The latter output (MAX_MIN) produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock while the count is zero (all outputs low) counting down or maximum (all outputs high) counting up. The ripple clock output (RCOZ) produces a low-level output pulse under those same conditions, but only while the clock input is low. The counters can be easily cascaded by feeding the ripple-clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

The SN54ASC191 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC191 is characterized for operation from −40°C to 85°C.

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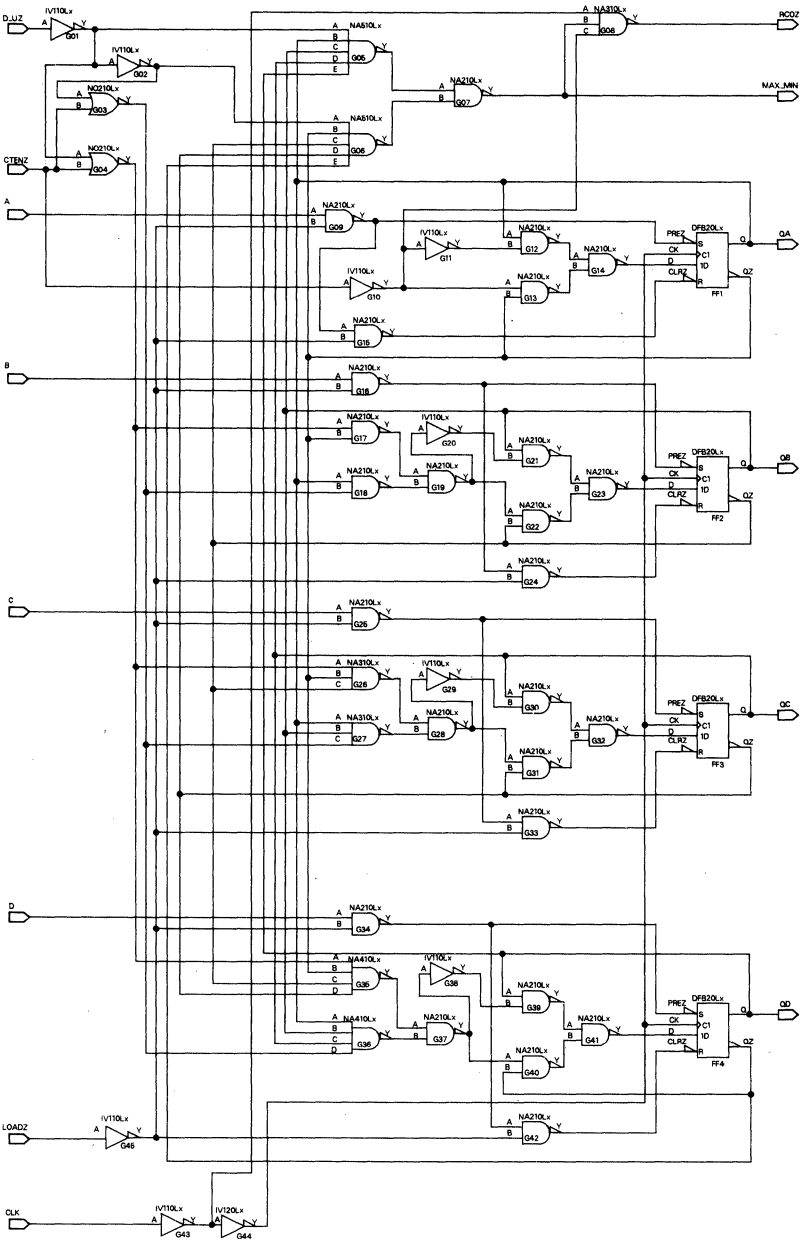
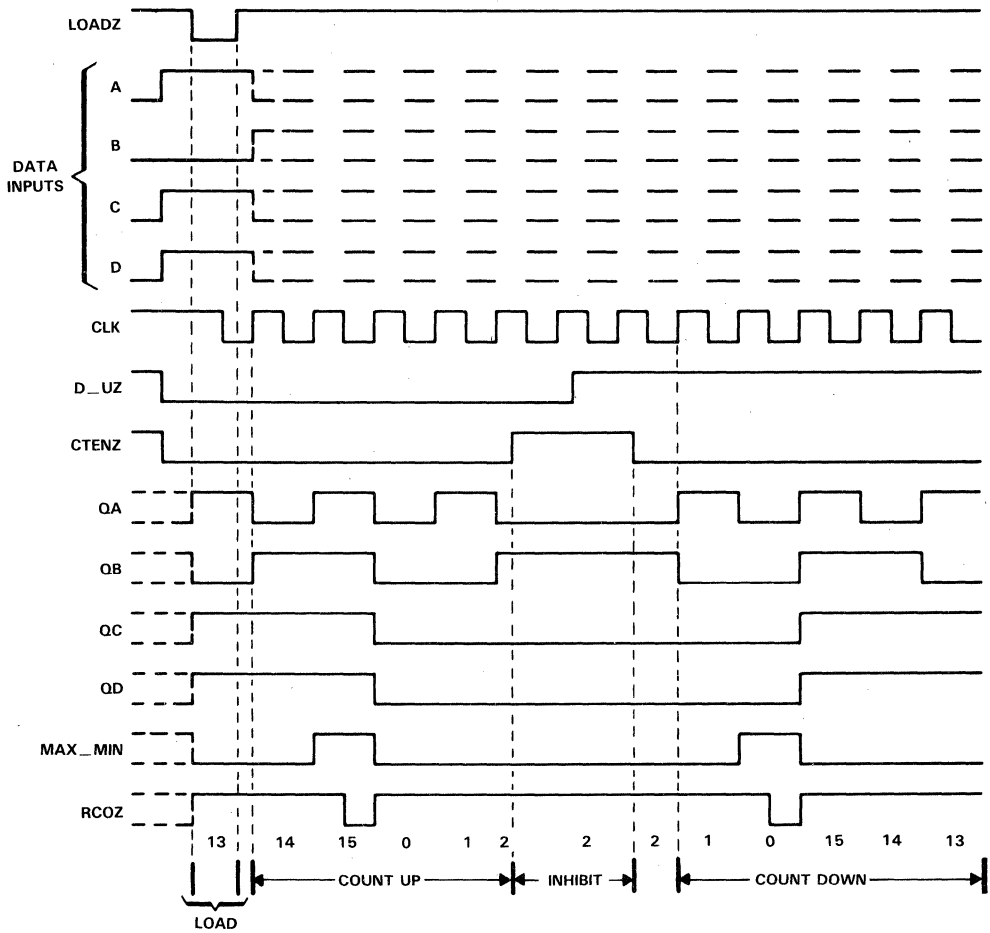
logic diagram



typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to binary thirteen.
2. Count up to fourteen, fifteen (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen.



absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

electrical characteristics

PARAMETER		TEST CONDITIONS	SN54ASC191		SN74ASC191		UNIT
			TYP	MAX	TYP	MAX	
V_T Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC} Supply current		V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		9763		586	nA
C_i Input capacitance	CTENZ	V_{CC} = 5 V, T_A = 25°C	0.34		0.34		pF
	All others		0.12		0.12		
C_{pd} Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25 °C, t_r = t_f = 3 ns,	37.26		37.26		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 1)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC191			SN74ASC191			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{pd}	LOADZ	Q	C_L = 0		7.7	15		7.7	13.0	ns
t_{pd}	A, B, C, D	Q			5.9	11.6		5.9	10.4	ns
t_{pd}	CLK	RCOZ			2.7	4.5		2.7	4.3	ns
t_{pd}	CLK	Q			8	18		8	16	ns
t_{pd}	CLK	MAX_MIN			11.5	25.5		11.5	22.7	ns
t_{pd}	D_UZ	RCOZ			6.9	13.2		6.9	11.9	ns
t_{pd}	D_UZ	MAX_MIN			5.9	11.2		5.9	10.1	ns
t_{pd}	CTENZ	RCOZ			2.6	4.8		2.6	4.5	ns
Δt_{pd}	Any	Q		0.1	0.5	1.3	0.1	0.5	1.2	ns/pF
Δt_{pd}	Any	RCOZ		0.5	1.3	3.8	0.5	1.3	3.2	ns/pF
Δt_{pd}	Any	MAX_MIN		0.5	1.1	2.7	0.5	1.1	2.5	ns/pF

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{pd} ≡ propagation delay time, low-to-high-level or high-to-low-level output
Δt_{pd} ≡ change in t_{pd} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: These switching characteristics are simulations of the software macro cell using interconnect capacitance values for an array design having 2,000 gates. Post-layout simulation uses actual interconnect capacitance values.

DESIGN CONSIDERATIONS

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

The HDL for this software macro is included as a part of the library supplied for supported engineering workstations so that a single label can be developed to apply the macro as needed. The following printout of the HDL block definition is furnished for reference.

HDL FILE

```
BLOCK S191LH;
D               @INPUT;
C               @INPUT;
B               @INPUT;
A               @INPUT;
CLK             @INPUT;
D_UZ            @INPUT;
CTENZ           @INPUT;
LOADZ           @INPUT;
QD              @OUTPUT;
QC              @OUTPUT;
QB              @OUTPUT;
QA              @OUTPUT;
RCOZ            @OUTPUT;
MAX_MIN         @OUTPUT;

STRUCTURE
FF1             :DFB20LH        G15O,G09O,G14O,G44O,QA,FF1QZ;
FF2             :DFB20LH        G24O,G16O,G23O,G44O,QB,FF2QZ;
FF3             :DFB20LH        G33O,G25O,G32O,G44O,QC,FF3QZ;
FF4             :DFB20LH        G42O,G34O,G41O,G44O,QD,FF4QZ;
G01             :IV110LH        D_UZ,G01O;
G02             :IV110LH        G01O,G02O;
G03             :NO210LH        G02O,CTENZ,G03O;
G04             :NO210LH        G01O,CTENZ,G04O;
G05             :NA510LH        G01O,QA,QB,QC,QD,G05O;
G06             :NA510LH        G02O,FF1QZ,FF2QZ,FF3QZ,FF4QZ,G06O;
G07             :NA210LH        G05O,G06O,MAX_MIN;
G08             :NA310LH        G43O,MAX_MIN,G10O,RCOZ;
G09             :NA210LH        A,G45O,G09O;
G10             :IV110LH        CTENZ,G10O;
G11             :IV110LH        G10O,G11O;
G12             :NA210LH        QA,G11O,G12O;
G13             :NA210LH        G10O,FF1QZ,G13O;
G14             :NA210LH        G12O,G13O,G14O;
G15             :NA210LH        G09O,G45O,G15O;
G16             :NA210LH        B,G45O,G16O;
G17             :NA210LH        G04O,FF1QZ,G17O;
G18             :NA210LH        QA,G03O,G18O;
G19             :NA210LH        G17O,G18O,G19O;
G20             :IV110LH        G19O,G20O;
G21             :NA210LH        QB,G20O,G21O;
G22             :NA210LH        G19O,FF2QZ,G22O;
G23             :NA210LH        G21O,G22O,G23O;
G24             :NA210LH        G16O,G45O,G24O;
G25             :NA210LH        C,G45O,G25O;
G26             :NA310LH        G04O,FF1QZ,FF2QZ,G26O;
G27             :NA310LH        QA,QB,G03O,G27O;
G28             :NA210LH        G26O,G27O,G28O;
G29             :IV110LH        G28O,G29O;
G30             :NA210LH        QC,G29O,G30O;
```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HDL FILE (Continued)

```
STRUCTURE (Continued)
G31          :NA210LH        G28O,FF3QZ,G31O;
G32          :NA210LH        G30O,G31O,G32O;
G33          :NA210LH        G25O,G45O,G33O;
G34          :NA210LH        D,G45O,G34O;
G35          :NA410LH        G04O,FF1QZ,FF2QZ,FF3QZ,G35O;
G36          :NA410LH        QA,QB,QC,G03O,G36O;
G37          :NA210LH        G35O,G36O,G37O;
G38          :IV110LH        G37O,G38O;
G39          :NA210LH        QD,G38O,G39O;
G40          :NA210LH        G37O,FF4QZ,G40O;
G41          :NA210LH        G39O,G40O,G41O;
G42          :NA210LH        G34O,G45O,G42O;
G43          :IV110LH        CLK,G43O;
G44          :IV120LH        G43O,G44O;
G45          :IV110LH        LOADZ,G45O;
END S191LH;
```

count definition

These counters are bidirectional with respect to count operations, and the relationship for counting up or down is defined by the D_UZ select input. Unidirectional counters are available in software macros or can be constructed using the 'ASC2405 through 'ASC2407 4-bit predesigned registers. Additional single bits can be achieved with flip-flop cells offered in TI's standard cell family.

designing for testability

Designers employing storage or bistable elements, especially long registers (ripple or synchronous), should consider testability of the design in its final form. The need to preset or clear and read intermediate stages of these elements should be assessed throughout the development of custom logic circuits with these considerations extended to the end-equipment application with respect to maintainability. Simple actions on the part of the ASIC designer can result in considerable cost savings, allowing the expense of IC testing, system testing, and system maintenance to be reduced significantly.

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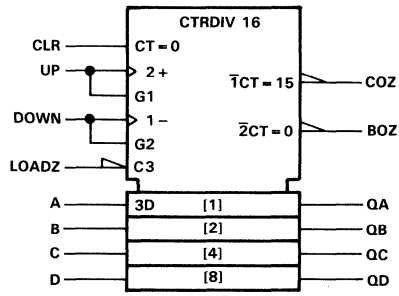
SystemCell™ 2-μm SOFTWARE MACRO CELL

- Dual Clock Inputs for Sourcing Count Direction
- Fully Synchronous in Count Modes
- Parallel Asynchronous Load for Modulo-N Count Sequences
- Asynchronous Clear
- Look-Ahead Circuitry Enhances Performance of Cascaded Counters

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The SN54ASC193 and SN74ASC193 are standard-cell software macros implementing 4-bit up-down binary counters. The 4-bit configuration provides the custom IC designer a bidirectional counter to embed in ASICs in its most efficient form. Its 4-bit length means that testability is simplified when constructing large counters. The 'ASC193 implements a count sequence identical with that performed by packaged 'HC193, 'LS193, and 'F193 counters.

The 'ASC193 is a synchronous, reversible up/down counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidentally with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters. The 'ASC193 is implemented with the standard cell functions indicated. This software macro is identified and called from the engineering workstation input using the cell name and netlist in conjunction with a label developed as shown on the last line of the following table:

CELL NAME	RELATIVE CELL AREA TO NA210LH	NO. USED	TOTAL RELATIVE CELL AREA	TOTAL C_{pd}‡ (pF)	MAXIMUM I_{CC} (nA)	
					SN54ASC'	SN74ASC'
AN210LH	1.5	6	9	5.4	1164	69.6
AN310LH	1.75	2	3.5	2.12	442	26.6
AN410LH	2	2	4	2.36	512	30.6
IV120LH	1	4	4	1.76	420	25.28
NA210LH	1	4	4	2.04	524	31.36
NA310LH	1.25	4	5	2	652	39.12
NA520LH	1.75	2	3.5	1.04	426	25.6
NO210LH	1	4	4	1.32	512	30.84
TAB20LH	7.7	4	30.8	16.8	3756	224.8
TOTALS		32	67.8	34.84	8408	504
Label: S193LH A,B,C,D,UP,DOWN,LOADZ,CLR,BOZ,COZ,QA,QB,QC,QD;						

‡The equivalent power dissipation capacitance does not include interconnect capacitance.

The outputs of the four flip-flops are triggered by a low-to-high-level transition of either count (clock) input (UP or DOWN). The direction of counting is determined by which count input is pulsed while the other count input is high. These counters are fully programmable; that is, they may be preset to any number between 0 and 15 by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided that forces all outputs to the low level when a high level is applied. The clear function is independent of the count and the load inputs.

These counters are designed to be cascaded without the need for additional circuitry. The borrow output (BOZ) produces a low-level pulse while the count is zero (all outputs low) and the count-down is low. Similarly, the carry output (COZ) produces a low-level pulse while the count is maximum (all outputs high) and the count-up input is low. The counters are cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs, respectively, of the succeeding counter.

The SN54ASC193 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC193 is characterized for operation from −40°C to 85°C.

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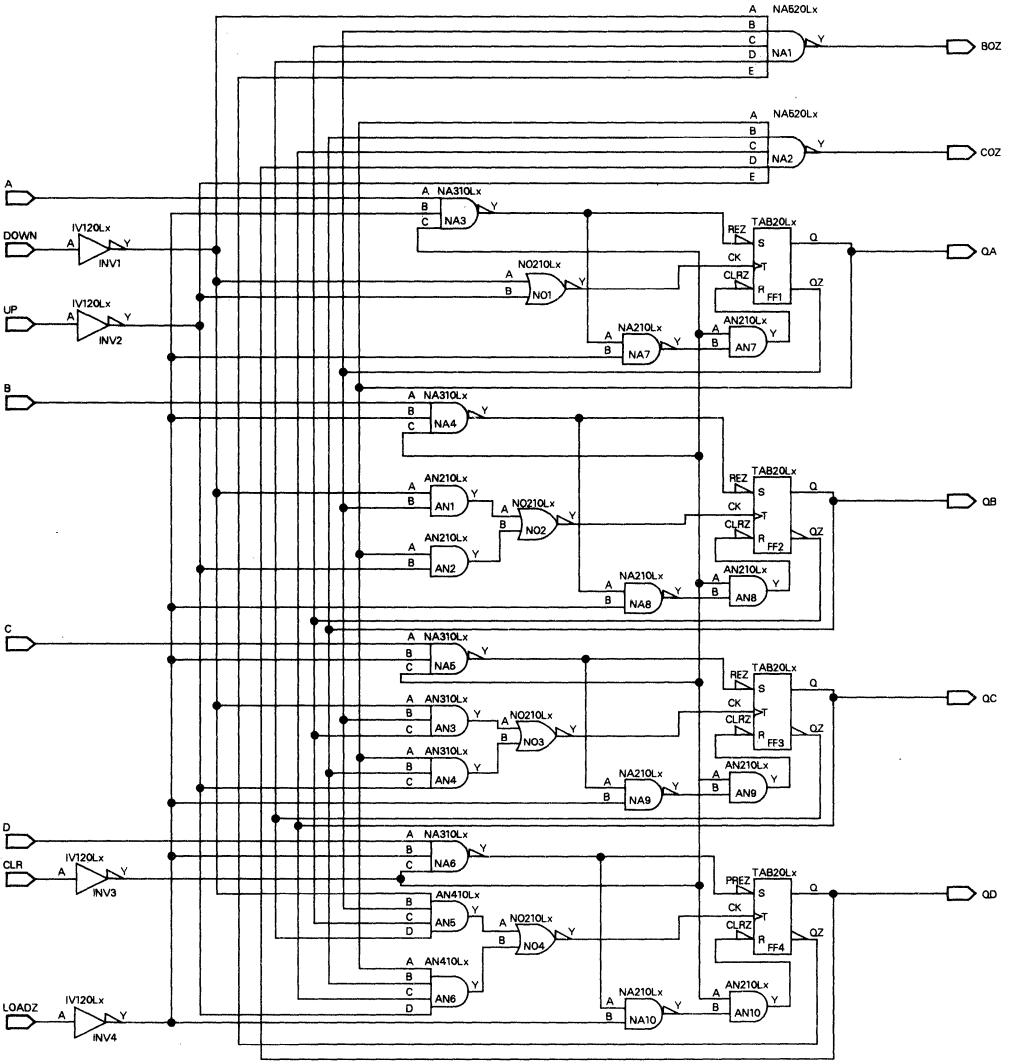
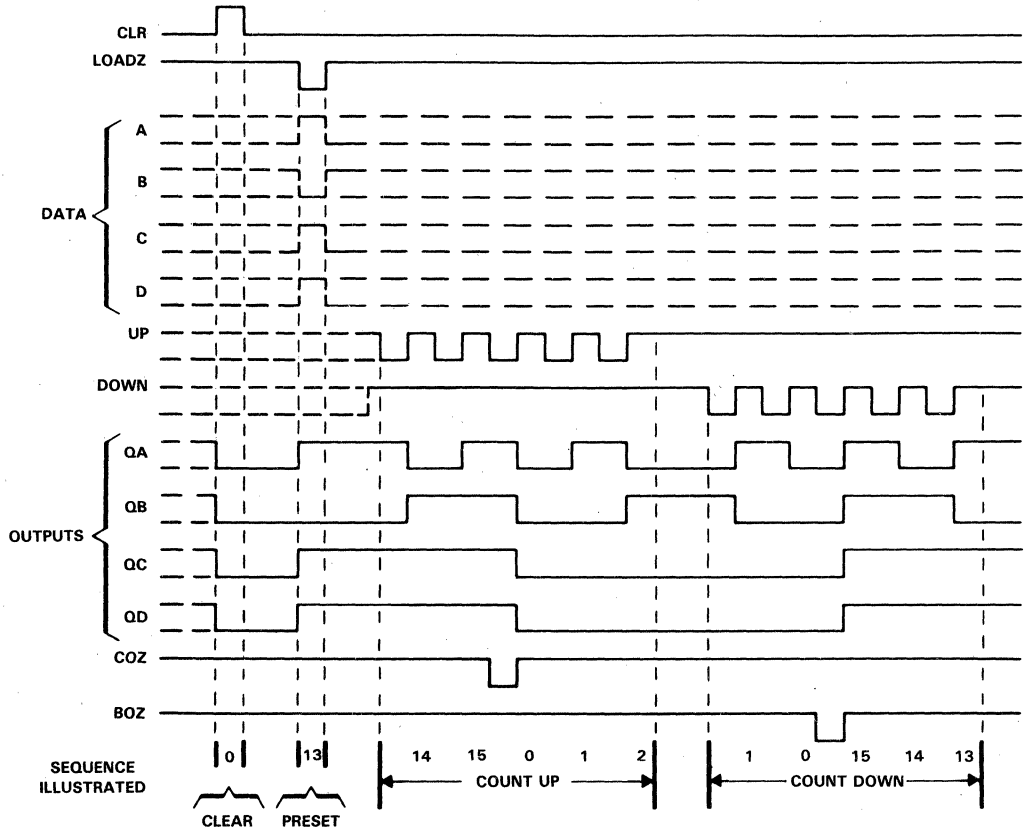
logic diagram



typical clear, load, and count sequences

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to binary thirteen.
3. Count up to fourteen, fifteen, carry, zero, one, and two.
4. Count down to one, zero, borrow, fifteen, fourteen, and thirteen.



NOTES: A. Clear overrides load, data, and count inputs.
B. When counting up, count-down input must be high; when counting down, count-up input must be high.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

electrical characteristics

PARAMETER			TEST CONDITIONS	SN54ASC193		SN74ASC193		UNIT
				TYP	MAX	TYP	MAX	
V_T	Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current		V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		8408		504	nA
C_i	Input capacitance	A,B,C,D	V_{CC} = 5 V, T_A = 25°C	0.12		0.12		pF
		All others		0.24		0.24		
C_{pd}	Equivalent power dissipation capacitance†		V_{CC} = 5 V, T_A = 25°C, t_r = t_f = 3 ns,	34.84		34.84		pF

† The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 1)

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC193			SN74ASC193			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
t_{pd}	UP	COZ	C_L = 0		3	5.1		3	4.7	ns
t_{pd}	DOWN	BOZ			3	5.2		3	4.7	ns
t_{pd}	DOWN, UP	Any Q			11	24.1		11	21.6	ns
t_{pd}	LOADZ	Any Q			7	14.5		7	13.5	ns
t_{PHL}	CLR	Any Q			5	10.5		5	9.6	ns
Δt_{pd}	Any	Any Q		0.1	0.5	1.4	0.1	0.5	1.2	ns/pF
Δt_{pd}	Any	BOZ, COZ		0.3	0.9	2.8	0.3	0.9	2.4	ns/pF

‡ Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{pd} ≡ propagation delay time, low-to-high or high-to-low-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{pd} ≡ change in t_{pd} with load capacitance
§ Typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: These switching characteristics are simulations of the software macro cell using interconnect capacitance values for an array design having 2,000 gates. Post-layout simulation uses actual interconnect capacitance values.

DESIGN CONSIDERATIONS

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

The HDL for this software macro is included as a part of the library supplied for supported engineering workstations so that a single label can be developed to apply the macro as needed. The following printout of the HDL block definition is furnished for reference.

HDL FILE

```
BLOCK S193LH;
A               @INPUT;
B               @INPUT;
C               @INPUT;
D               @INPUT;
UP              @INPUT;
DOWN            @INPUT;
LOADZ           @INPUT;
CLR             @INPUT;
BOZ             @OUTPUT;
COZ             @OUTPUT;
QA              @OUTPUT;
QB              @OUTPUT;
QC              @OUTPUT;
QD              @OUTPUT;

STRUCTURE
AN1             :AN210LH        INV1S,FF1S,AN1S;
AN10            :AN210LH        INV3S,NA10,AN10S;
AN2             :AN210LH        QA,INV2S,AN2S;
AN3             :AN310LH        INV1S,FF1S,FF2S,AN3S;
AN4             :AN310LH        QA,QB,INV2S,AN4S;
AN5             :AN410LH        INV1S,FF1S,FF2S,FF3S,AN5S;
AN6             :AN410LH        QA,QB,QC,INV2S,AN6S;
AN7             :AN210LH        INV3S,NA7S,AN7S;
AN8             :AN210LH        INV3S,NA8S,AN8S;
AN9             :AN210LH        INV3S,NA9S,AN9S;
FF1             :TAB20LH        AN7S,NA3S,NO1S,QA,FF1S;
FF2             :TAB20LH        AN8S,NA4S,NO2S,QB,FF2S;
FF3             :TAB20LH        AN9S,NA5S,NO3S,QC,FF3S;
FF4             :TAB20LH        AN10S,NA6S,NO4S,QD,FF4S;
INV1            :IV120LH        DOWN,INV1S;
INV2            :IV120LH        UP,INV2S;
INV3            :IV120LH        CLR,INV3S;
INV4            :IV120LH        LOADZ,INV4S;
NA1             :NA520LH        INV1S,FF1S,FF2S,FF3S,FF4S,BOZ;
NA10            :NA210LH        NA6S,INV4S,NA10S;
NA2             :NA520LH        QA,QB,QC,QD,INV2S,COZ;
NA3             :NA310LH        A,INV4S,INV3S,NA3S;
NA4             :NA310LH        B,INV4S,INV3S,NA4S;
NA5             :NA310LH        C,INV4S,INV3S,NA5S;
NA6             :NA310LH        D,INV4S,INV3S,NA6S;
NA7             :NA210LH        NA3S,INV4S,NA7S;
NA8             :NA210LH        NA4S,INV4S,NA8S;
NA9             :NA210LH        NA5S,INV4S,NA9S;
NO1             :NO210LH        INV1S,INV2S,NO1S;
NO2             :NO210LH        AN1S,AN2S,NO2S;
NO3             :NO210LH        AN3S,AN4S,NO3S;
NO4             :NO210LH        AN5S,AN6S,NO4S;
END S193LH;
```

count definition

These counters are bidirectional with respect to count operations, and the relationship for counting up or down is defined by the UP and DOWN inputs. Unidirectional counters are available in software macros or can be constructed using the 'ASC2405 through 'ASC2407 4-bit predesigned registers. Additional single bits can be achieved with predesigned flip-flops offered in TI's standard cell family.

designing for testability

Designs employing storage or bistable elements, especially long counters (ripple or synchronous), should consider testability of the design in its final form. The need to preset or clear and to read intermediate stages of these elements should be assessed throughout the development of custom logic circuits with these considerations extended to the end-equipment application with respect to maintainability. Simple actions on the part of the ASIC designer can result in considerable cost savings, allowing the expense of IC testing, system testing, and system maintenance to be reduced significantly.

power-up clear/preset

Standard cell storage elements containing the capability to be asynchronously preset or cleared may be connected to the SN54ASC2320 or SN74ASC2320 power-up clear cell to achieve system initialization. Control of the clear or preset inputs from another system signal in conjunction with the power-up clear can be achieved with an OR gate.

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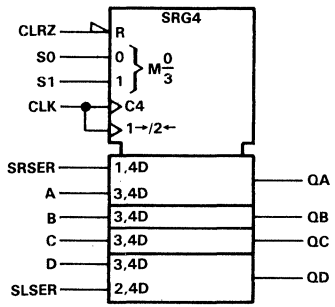
SystemCell™ 2-μm SOFTWARE MACRO CELL

- **Parallel Inputs and Outputs**
- **Four Operating Modes:**
  - **Synchronous Parallel Load**
  - **Right Shift**
  - **Left Shift**
  - **Do Nothing**
- **Positive Edge-Triggered Clocking**
- **Embedded Clock Drivers Provide Clock Buffering**

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The SN54ASC194A and SN74ASC194A are standard-cell software macros implementing 4-bit parallel-in/parallel-out bidirectional, universal shift registers. The 4-bit configuration provides the custom IC designer a register to embed in ASICs in its most efficient form. Its 4-bit length simplifies construction of large registers. The 'ASC194A implements a shift register identical with that performed by packaged 'HC194, 'LS194A, and 'F194 registers.

These bidirectional shift registers are designed to incorporate virtually all of the features a system designer may want in a shift register. The circuit features parallel inputs, parallel outputs, right-shift and left-shift inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

Inhibit clocking (do nothing)
Shift right (in the direction QA toward QD)
Shift left (in the direction QD toward QA)
Parallel (broadside load)

The 'ASC194A is implemented with the standard cell functions indicated. The HDL netlist label for this software macro is shown on the last line of the following table:

CELL NAME	RELATIVE CELL AREA TO NA210LH	NO. USED	TOTAL RELATIVE CELL AREA	TOTAL C_{pd}‡ (pF)	MAXIMUM I_{CC} (nA)	
					SN54ASC'	SN74ASC'
IV110LH	0.75	1	0.75	0.44	105	6.32
IV120LH	1	4	4	3.2	524	31.4
IV140LH	1.5	1	1.5	1.61	190	11.4
NA310LH	1.25	16	20	8	2608	156.48
NA410LH	1.5	4	6	2	748	44.8
R2405LH	23.25	1	23.25	10.2	2647	159
TOTALS		27	55.5	25.45	6822	410
S194ALH	Label: S194ALH A,B,C,D,SRSER,SLSER,CLK,CLRZ,S1,S0,QA,QB,QC,QD;					

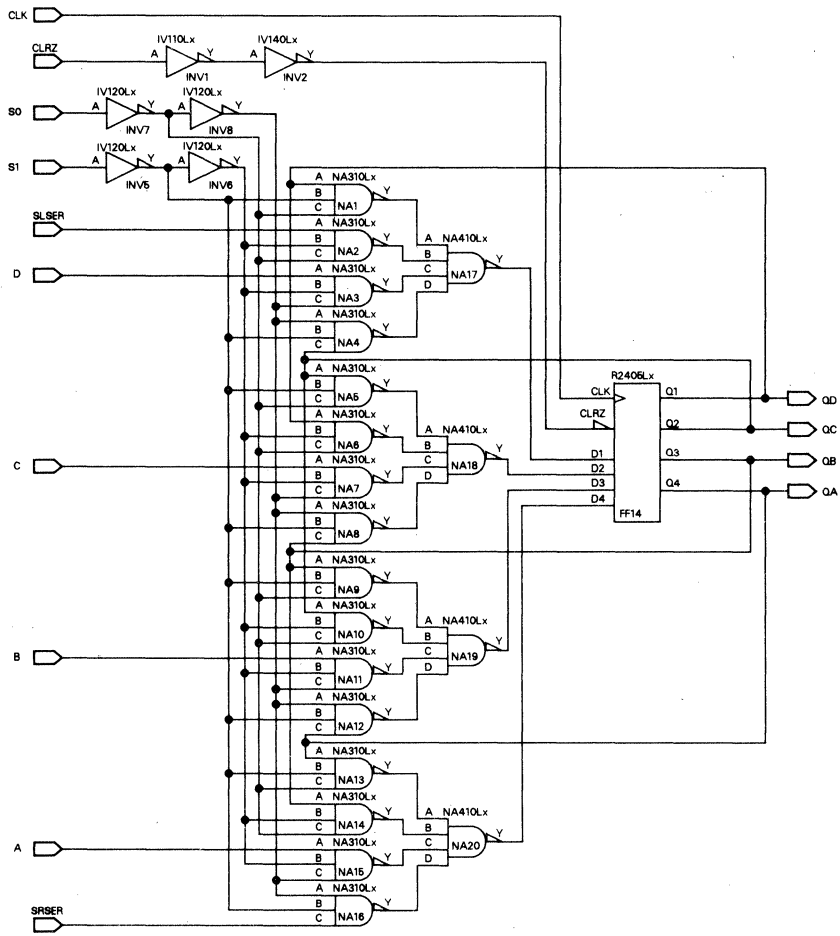
‡The equivalent power dissipation capacitance does not include interconnect capacitance.

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S0 and S1, high. The data are loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode are entered at the shift-right data input. When S0 is low and S1 is high, data shift left synchronously and new data are entered at the shift-left serial input. When both mode control inputs are low, a free-running clock will reload the present state of each flip-flop on each clock transition to implement the do-nothing mode.

The SN54ASC194A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC194A is characterized for operation from −40°C to 85°C.

logic diagram

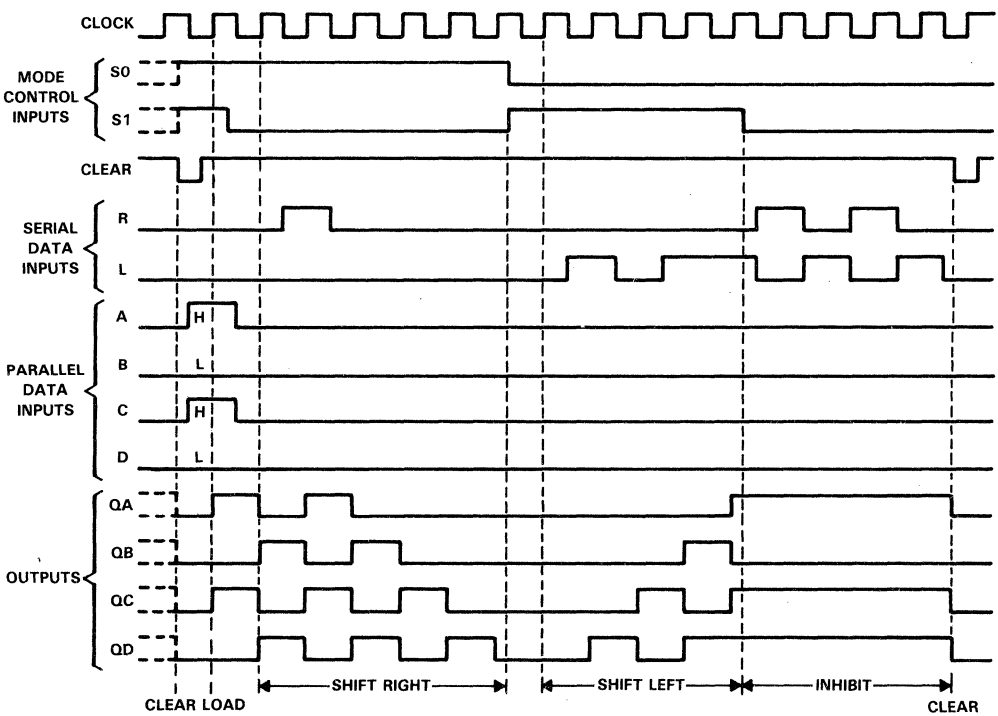


FUNCTION TABLE

INPUTS										OUTPUTS			
CLRZ	MODE		CLK	SERIAL		PARALLEL				QA	QB	QC	QD
	S1	S0		SLSER	SRSER	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	QA_0	QB_0	QC_0	QD_0
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	QA_n	QB_n	QC_n
H	L	H	↑	X	L	X	X	X	X	L	QA_n	QB_n	QC_n
H	H	L	↑	H	X	X	X	X	X	QB_n	QC_n	QD_n	H
H	H	L	↑	L	X	X	X	X	X	QB_n	QC_n	QD_n	L
H	L	L	X	X	X	X	X	X	X	QA_0	QB_0	QC_0	QD_0

See Explanation of Function Tables in Section 1.

typical clear, load, right-shift, left-shift, inhibit, and clear sequences



absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

electrical characteristics

PARAMETER			TEST CONDITIONS	SN54ASC194A TYP	SN54ASC194A MAX	SN74ASC194A TYP	SN74ASC194A MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current		V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		6822		410	nA
C_i	Input capacitance	CLK,S0,S1	V_{CC} = 5 V, T_A = 25°C	0.24		0.24		pF
		All others		0.12		0.12		
C_{pd}	Equivalent power dissipation capacitance†		V_{CC} = 5 V, T_A = 25°C, t_r = t_f = 3 ns,	25.45		25.45		pF

† The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 1)

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC194A MIN	SN54ASC194A TYP§	SN54ASC194A MAX	SN74ASC194A MIN	SN74ASC194A TYP§	SN74ASC194A MAX	UNIT
t_{pd}	CLK	Qn	C_L = 0		5	10.5		5	9.4	ns
t_{PHL}	CLRZ	Qn			5	8.4		5	7.7	ns
Δt_{pd}	CLK	Qn		0.3	0.9	2.3	0.3	0.9	2.1	ns/pF
Δt_{PHL}	CLRZ	Qn		0.3	0.7	1.9	0.3	0.7	1.6	ns/pF

‡ Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{pd} ≡ propagation delay time, low-to-high- or high-to-low-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{pd} ≡ change in t_{pd} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
§ Typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: These switching characteristics are simulations of the software macro cell using interconnect capacitance values for an array design having 2,000 gates. Post-layout simulation uses actual interconnect capacitance values.

DESIGN CONSIDERATIONS

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

The HDL for this software macro is included as a part of the library supplied for supported engineering workstations so that a single label can be developed to apply the macro as needed. The following printout of the HDL block definition is furnished for reference.

TEXAS INSTRUMENTS
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HDL FILE

```
BLOCK S194ALH;
A               @INPUT;
B               @INPUT;
C               @INPUT;
D               @INPUT;
SRSER           @INPUT;
SLSER           @INPUT;
CLK             @INPUT;
CLRZ            @INPUT;
S1              @INPUT;
S0              @INPUT;
QA              @OUTPUT;
QB              @OUTPUT;
QC              @OUTPUT;
QD              @OUTPUT;

STRUCTURE
FF14            :R2405LH        INV2O,NA17O,NA18O,NA19O,NA20O,CLK,QD,QC,QB,QA;
INV1            :IV110LH        CLRZ,INV1O;
INV2            :IV140LH        INV1O,INV2O;
INV5            :IV120LH        S1,INV5O;
INV6            :IV120LH        INV5O,INV6O;
INV7            :IV120LH        S0,INV7O;
INV8            :IV120LH        INV7O,INV8O;
NA1             :NA310LH        QD,INV5O,INV7O,NA1O;
NA10            :NA310LH        QC,INV6O,INV7O,NA10O;
NA11            :NA310LH        B,INV6O,INV8O,NA11O;
NA12            :NA310LH        INV8O,INV5O,QA,NA12O;
NA13            :NA310LH        QA,INV5O,INV7O,NA13O;
NA14            :NA310LH        QB,INV6O,INV7O,NA14O;
NA15            :NA310LH        A,INV6O,INV8O,NA15O;
NA16            :NA310LH        INV8O,INV5O,SRSER,NA16O;
NA17            :NA410LH        NA1O,NA2O,NA3O,NA4O,NA17O;
NA18            :NA410LH        NA5O,NA6O,NA7O,NA8O,NA18O;
NA19            :NA410LH        NA9O,NA1O,NA11O,NA12O,NA19O;
NA2             :NA310LH        SLSER,INV6O,INV7O,NA2O;
NA20            :NA410LH        NA13O,NA14O,NA15O,NA16O,NA2OO;
NA3             :NA310LH        D,INV6O,INV8O,NA3O;
NA4             :NA310LH        INV8O,INV5O,QC,NA4O;
NA5             :NA310LH        QC,INV5O,INV7O,NA5O;
NA6             :NA310LH        QD,INV6OINV7O,NA6O;
NA7             :NA310LH        C,INV6O,INV8O,NA7O;
NA8             :NA310LH        INV8O,INV5O,QB,NA8O;
NA9             :NA310LH        QB,INV5O,INV7O,NA9O;
END S194ALH;
```

shift definition

These registers are bidirectional with respect to shift operations and the relationship for shifting left or right is defined by the S0 and S1 inputs. Unidirectional registers are available in software macros or can be constructed using the 'ASC2405 through 'ASC2407 4-bit predesigned registers. Additional single bits can be achieved with flip-flop cells offered in TI's standard cell family.

designing for testability

Designs employing storage or bistable elements, especially long registers (ripple or synchronous), should consider testability of the design in its final form. The need to preset or clear and read intermediate stages of these elements should be assessed throughout the development of custom logic circuits with these considerations extended to the end-equipment application with respect to maintainability. Simple actions on the part of the ASIC designer can result in considerable cost savings, allowing the expense of IC testing, system testing, and system maintenance to be reduced significantly.

power-up clear preset

Standard cell storage elements containing the capability to be asynchronously preset or cleared may be connected to the SN54ASC2320 or SN74ASC2320 power-up clear cell to achieve system initialization. Control of the clear or preset inputs from another system signal in conjunction with the power-up clear can be achieved with an AND gate.

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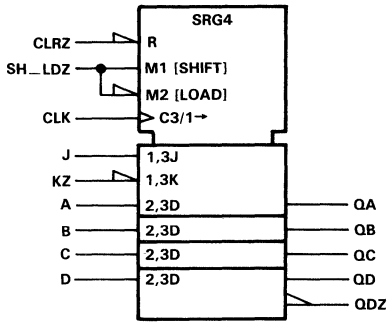
D2939, AUGUST 1986

SystemCell™ 2-μm SOFTWARE MACRO CELL

- **Synchronous Parallel Load**
- **Positive-Edge-Triggered Clocking**
- **J and KZ Inputs to First Stage**
- **Complementary Outputs from Last Stage**
- **Embedded Clock Drivers Provide Clock Buffering**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The SN54ASC195A and SN74ASC195A are standard-cell software macros implementing 4-bit parallel-out shift registers. The 4-bit configuration provides the custom IC designer a register to embed in ASICs in its most efficient form. The 4-bit length simplifies construction of large counters. The 'ASC195A implements a shift sequence identical with that performed by packaged 'HC195, 'LS195A, and 'F195 registers.

These 4-bit shift registers feature parallel inputs, parallel outputs, J-KZ serial inputs, shift/load control input, and a direct overriding clear. The registers have two modes of operation: parallel (broadside) load, and shift (in the direction of QA toward QD).

The 'ASC195A is implemented with the standard cell functions indicated. The HDL netlist label for this software macro is shown on the last line of the following table:

CELL NAME	RELATIVE CELL AREA TO NA210LH	NO. USED	TOTAL RELATIVE CELL AREA	TOTAL C_{pd}‡ (pF)	MAXIMUM I_{CC} (nA)	
					SN54ASC'	SN74ASC'
IV110LH	0.75	1	0.75	0.44	105	6.32
IV120LH	1	2	2	1.6	262	15.7
IV140LH	1.5	1	1.5	1.61	190	11.4
NA210LH	1	10	10	5.1	1310	78.4
NA310LH	1.25	3	3.75	1.5	489	29.34
R2406LH	26.25	1	26.25	11.69	2931	176
TOTALS		18	44.25	21.94	5287	318
S195ALH	Label: S195ALH CLRZ,CLK,SH_LDZ,J,KZ,A,B,C,D,QA,QB,QC,QD,QDZ;					

‡The equivalent power dissipation capacitance does not include interconnect capacitance.

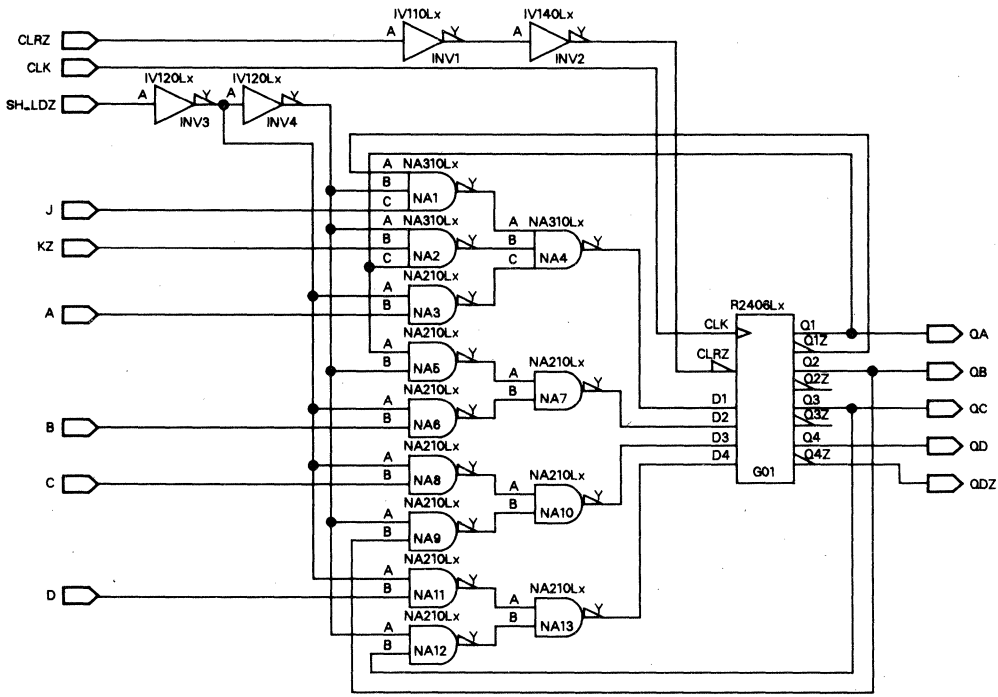
Parallel loading is accomplished by applying the four bits of data and taking the shift/load control (SH_LDZ) input low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock (CLK) input. During loading, serial data flow is inhibited.

description (continued)

Shifting is accomplished synchronously when the shift/load control is high. Serial data for this mode is entered at the J-KZ inputs. These inputs permit the first stage to perform as a J-K, D-, or T-type flip-flop as shown in the function table.

The SN54ASC195A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC195A is characterized for operation from −40°C to 85°C.

logic diagram



TEXAS INSTRUMENTS
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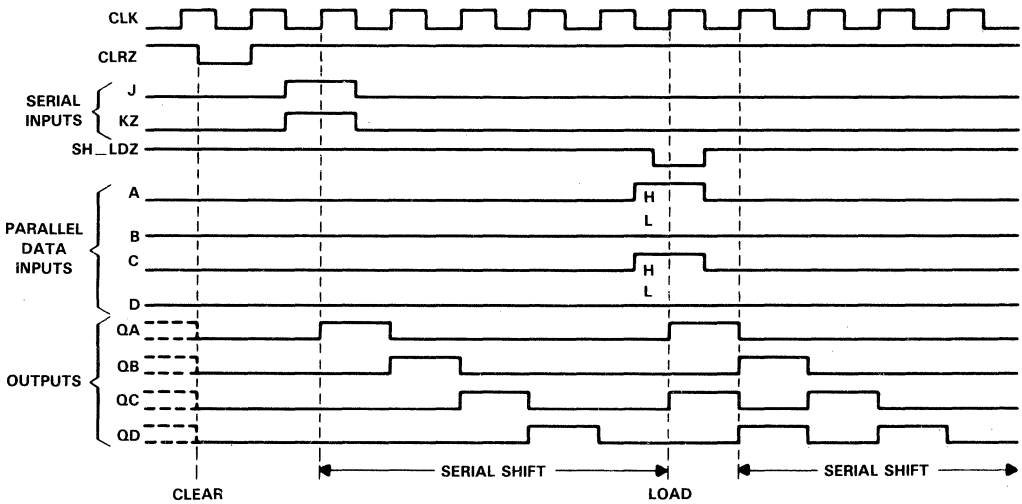
FUNCTION TABLE

INPUTS									OUTPUTS				
CLRZ	SH_LDZ	CLK	SERIAL		PARALLEL				QA	QB	QC	QD	QDZ
			J	KZ	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\overline{d}$Z
H	H	L	X	X	X	X	X	X	QA_0	QB_0	QC_0	QD_0	$\overline{Q}D_0$
H	H	↑	L	H	X	X	X	X	QA_0	QA_0	QB_n	QC_n	$\overline{Q}C_n$
H	H	↑	L	L	X	X	X	X	L	QA_n	QB_n	QC_n	$\overline{Q}C_n$
H	H	↑	H	H	X	X	X	X	H	QA_n	QB_n	QC_n	$\overline{Q}C_n$
H	H	↑	H	L	X	X	X	X	$\overline{Q}A_n$	QA_n	QB_n	QC_n	$\overline{Q}C_n$

typical clear, shift and load sequences



absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

electrical characteristics

PARAMETER			TEST CONDITIONS	SN54ASC195A TYP	SN54ASC195A MAX	SN74ASC195A TYP	SN74ASC195A MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current		V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		5287		318	nA
C_i	Input capacitance	CLK,SH_LDZ	V_{CC} = 5 V, T_A = 25°C	0.24		0.24		pF
		All others		0.12		0.12		
C_{pd}	Equivalent power dissipation capacitance†		V_{CC} = 5 V, T_A = 25°C, t_r = t_f = 3 ns,	21.95		21.95		pF

† The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted) (see Note 1)

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC195A MIN	SN54ASC195A TYP§	SN54ASC195A MAX	SN74ASC195A MIN	SN74ASC195A TYP§	SN74ASC195A MAX	UNIT
t_{pd}	CLK	Qn	C_L = 0		5	10.6		5	9.6	ns
t_{pd}	CLK	QDZ			5.5	12.5		5.5	11.3	ns
t_{PHL}	CLRZ	Qn			5.4	8.3		5.4	7.7	ns
t_{PLH}	CLRZ	QDZ			6.1	10.4		6.1	9.4	ns
Δt_{pd}	Any	Qn,QDZ		0.2	0.9	2.4	0.3	0.9	2.1	ns/pF

‡ Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{pd} ≡ propagation delay time, low-to-high-level or high-to-low-level output
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{pd} ≡ change propagation delay time with capacitance
§ Typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: These switching characteristics are simulations of the software macro cell using interconnect capacitance values for an array design having 2,000 gates. Post-layout simulation uses actual interconnect capacitance values.

DESIGN CONSIDERATIONS

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

The HDL for this software macro is included as a part of the library supplied for supported engineering workstations so that a single label can be developed to apply the macro as needed. The following printout of the HDL block definition is furnished for reference.

TEXAS INSTRUMENTS
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HDL FILE

```
BLOCK S195ALH;
CLRZ        @INPUT;
CLK         @INPUT;
SH_LDZ      @INPUT;
J           @INPUT;
KZ          @INPUT;
A           @INPUT;
B           @INPUT;
C           @INPUT;
D           @INPUT;
QA          @OUTPUT;
QB          @OUTPUT;
QC          @OUTPUT;
QD          @OUTPUT;
QDZ         @OUTPUT;

STRUCTURE
INV1        :IV110LH        CLRZ,CLR;
INV2        :IV140LH        CLR,CLRZ1;
INV3        :IV120LH        SH_LDZ,SHLDZ;
INV4        :IV120LH        SHLDZ,SHLD1;
NA1         :NA310LH        QAZ,SHLD1,J,S1;
NA10        :NA210LH        S8,S9,S10;
NA11        :NA210LH        SHLDZ,D,S11;
NA12        :NA210LH        SHLD1,QC,S12;
NA13        :NA210LH        S11,S12,S13;
NA2         :NA310LH        SHLD1,KZ,QA,S2;
NA3         :NA210LH        SHLDZ,A,S3;
NA4         :NA310LH        S1,S2,S3,S4;
NA5         :NA210LH        QA,SHLD1,S5;
NA6         :NA210LH        SHLDZ,B,S6;
NA7         :NA210LH        S5,S6,S7;
NA8         :NA210LH        SHLDZ,C,S8;
NA9         :NA210LH        SHLD1,QB,S9;
G01         :R2406LH        CLRZ1,S4,S7,S10,S13,CLK,QA,QAZ,QB,DUM,QC,DUM,QD,QDZ;
END S195ALH;
```

shift definition

These registers are unidirectional with respect to shift operations. Bidirectional registers are available in software macros or can be constructed using the 'ASC2405 through 'ASC2407 4-bit predesigned registers. Additional single bits can be achieved with flip-flop cells offered in TI's standard cell family.

designing for testability

Designs employing storage or bistable elements, especially long registers (ripple or synchronous), should consider testability of the design in its final form. The need to preset or clear and read intermediate stages of these elements should be assessed throughout the development of custom logic circuits with these considerations extended to the end-equipment application with respect to maintainability. Simple actions on the part of the ASIC designer can result in considerable cost savings, allowing the expense of IC testing, system testing, and system maintenance to be reduced significantly.

power-up clear/preset

Standard cell storage elements containing the capability to be asynchronously preset or cleared may be connected to the SN54ASC2320 or SN74ASC2320 power-up clear cell to achieve system initialization. Control of the clear or preset inputs from another system signal in conjunction with the power-up clear can be achieved with an AND gate.

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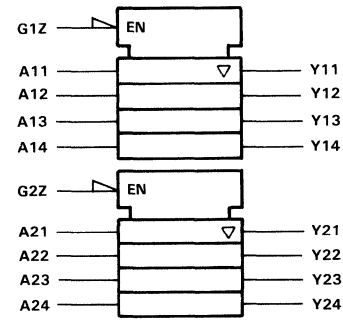
D2939, AUGUST 1986

SystemCell™ 2-μm SOFTWARE MACRO CELL

- **3-State Outputs Interface Internal Data Buses Directly**
- **Active-Low Enables for Expandability**
- **Use Parallel Bus Interfaces for Wide Words**

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The SN54ASC244 and SN74ASC244 are standard-cell software macros implementing octal internal 3-state bus buffers. The 'ASC244 executes a function table identical with that performed by packaged 'HC244, 'LS244, and 'S244 bus drivers.

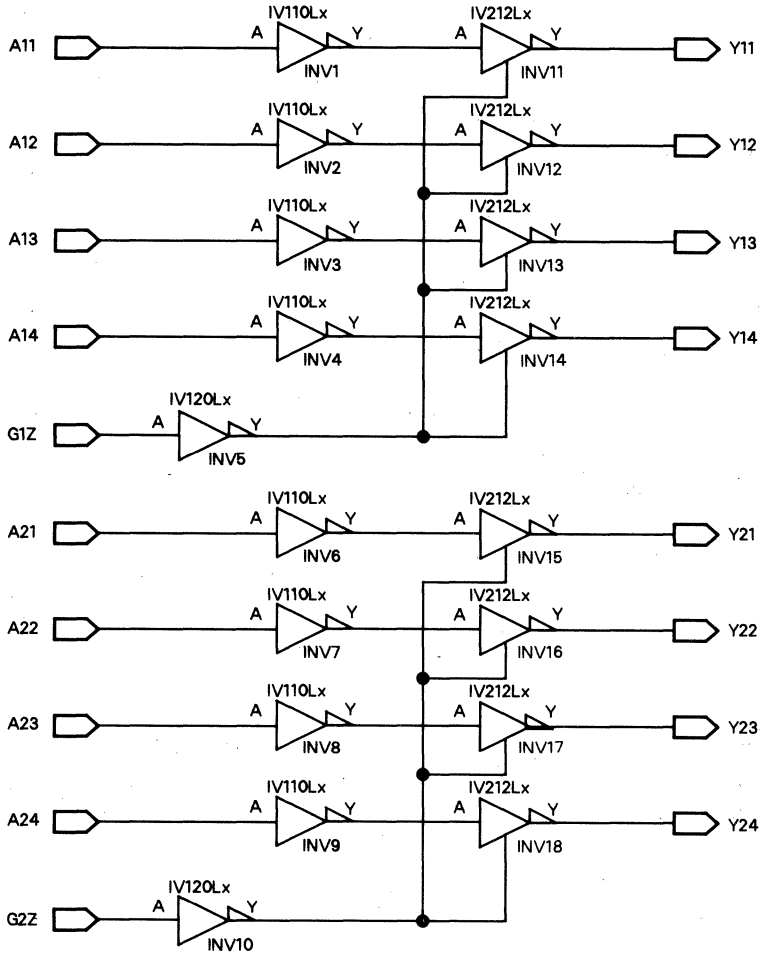
The macro is organized as dual 4-bit drivers with individual enables, G1Z and G2Z, that enable and disable the 3-state outputs to permit interfacing the internal bus directly in either a parallel or word mode. The Y outputs are in a high-impedance state when GnZ is high. When GnZ is low, the outputs drive the bus lines. The 'ASC244 is implemented with standard cell functions indicated. The HDL netlist label for this software macro is shown on the last line of the following table:

CELL NAME	RELATIVE CELL AREA TO NA210LH	NO. USED	TOTAL RELATIVE CELL AREA	TOTAL C_{pd}‡ (pF)	MAXIMUM I_{CC} (nA)	
					SN54ASC'	SN74ASC'
IV110LH	0.75	8	6	3.52	840	50.56
IV120LH	1	2	2	1.6	262	15.7
IV212LH	1.5	8	12	4	1440	86.4
TOTALS		18	20	8.82	2542	153
Label: S244LH A11,A12,A13,A14,G1Z,A21,A22,A23,A24,G2Z,Y11,Y12,Y13,Y14,Y21, Y22,Y23,Y24;						

‡The equivalent power dissipation capacitance does not include interconnect capacitance.

The SN54ASC244 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC244 is characterized for operation from −40°C to 85°C.

logic diagram



absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS		SN54ASC244 TYP	SN54ASC244 MAX	SN74ASC244 TYP	SN74ASC244 MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX	V_I = V_{CC} or 0,		2542		153	nA
C_i	Input capacitance	A inputs	V_{CC} = 5 V,	T_A = 25°C	0.12		0.12		pF
		G1Z, G2Z			0.24		0.24		
C_o	Output capacitance		V_{CC} = 5 V,	T_A = 25°C	0.18		0.18		pF
C_{pd}	Equivalent power dissipation capacitance†		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	8.82		8.82		pF

† The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Notes 1 and 2)

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC244 MIN	SN54ASC244 TYP§	SN54ASC244 MAX	SN74ASC244 MIN	SN74ASC244 TYP§	SN74ASC244 MAX	UNIT
t_{pd}	Any A	Any Y	C_L = 0		2.4	4.4		2.4	4.1	ns
t_{en}	GnZ	Any Y			2.6	5.1		2.6	4.7	
Δt_{pd}	Any	Y		0.6	1.7	4.6	0.6	1.7	4.2	ns/pF
Δt_{en}	Any	Y		0.7	1.7	4.8	0.7	1.7	4.4	ns/pF

‡ Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{pd} ≡ propagation delay time, low-to-high- or high-to-low-level output
t_{en} ≡ enable time, high-impedance state to low- or high-logic-level output
Δt_{pd} ≡ change in t_{pd} with load capacitance
Δt_{en} ≡ change in t_{en} with load capacitance
§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTES 1. These switching characteristics are simulations of the software macro cell using interconnect capacitance values for an array design having 2,000 gates. Post-layout simulation uses actual interconnect capacitance values.
2. Enable and delta-enable times are measured using the conditions specified for the 'ASC2311 (IV212LH).

DESIGN CONSIDERATIONS

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

The HDL for this software macro is included as a part of the library supplied for supported engineering workstations so that a single label can be developed to apply the macro as needed. The following printout of the HDL block definition is furnished for reference.

HDL FILE

```
BLOCK S244LH;
A11         @INPUT;
A12         @INPUT;
A13         @INPUT;
A14         @INPUT;
G1Z         @INPUT;
A21         @INPUT;
A22         @INPUT;
A23         @INPUT;
A24         @INPUT;
G2Z         @INPUT;
Y11         @OUTPUT;
Y12         @OUTPUT;
Y13         @OUTPUT;
Y14         @OUTPUT;
Y21         @OUTPUT;
Y22         @OUTPUT;
Y23         @OUTPUT;
Y24         @OUTPUT;

STRUCTURE
INV1        :IV110LH        A11,INV1O;
INV10       :IV120LH        G2Z,INV10O;
INV11       :IV212LH        INV1O,INV5O,Y11;
INV12       :IV212LH        INV2O,INV5O,Y12;
INV13       :IV212LH        INV3O,INV5O,Y13;
INV14       :IV212LH        INV4O,INV5O,Y14;
INV15       :IV212LH        INV6O,INV10O,Y21;
INV16       :IV212LH        INV7O,INV10O,Y22;
INV17       :IV212LH        INV8O,INV10O,Y23;
INV18       :IV212LH        INV9O,INV10O,Y24;
INV2        :IV110LH        A12,INV2O;
INV3        :IV110LH        A13,INV3O;
INV4        :IV110LH        A14,INV4O;
INV5        :IV120LH        G1Z,INV5O;
INV6        :IV110LH        A21,INV6O;
INV7        :IV110LH        A22,INV7O;
INV8        :IV110LH        A23,INV8O;
INV9        :IV110LH        A24,INV9O;
END S244LH;
```

Hardwired internal cells with 3-state outputs are also available in the standard cell library. These hardwired cells should be considered if the interface is in a critical path, as their performance is predetermined as specified in their switching characteristics.

interfacing the macro

Inputs and outputs of the predesigned macro are compatible for interfacing directly with cells and macros available in the TI standard cell library.

The inputs can be driven by either inverting or noninverting input cells. The outputs can be interfaced to drive off-chip loads with any of the noninverting output buffers or interfaced to external bidirectional buses through a 3-state input/output TTL/CMOS buffer.

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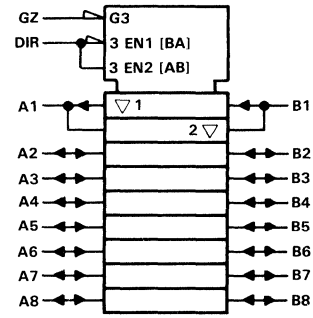
D2939, AUGUST 1986

SystemCell™ 2-μm SOFTWARE MACRO CELL

- **3-State Outputs Interface Internal Data Buses Directly**
- **Active-Low Enables for Expandability**
- **Use Parallel Bus Interfaces for Wide Words**

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The SN54ASC245 and SN74ASC245 are standard-cell software macros implementing octal internal 3-state bidirectional I/O ports. The 'ASC245 executes a function table identical with that performed by packaged 'HC245, 'LS245, and 'F245 bus transceivers.

The macro is organized as an octal transceiver with direction control DIR and an output enable GZ. The GZ input enables and disables the 3-state outputs to permit interfacing or isolating the internal bus directly in a parallel mode. The outputs are in a high-impedance state when GZ is high. When GZ is low, the outputs selected by the DIR control drive the bus lines. The 'ASC245 is implemented with standard cell functions indicated. The HDL netlist label for this software macro is shown on the last line of the following table:

CELL NAME	RELATIVE CELL AREA TO NA210LH	NO. USED	TOTAL RELATIVE CELL AREA	TOTAL C_{pd}‡ (pF)	MAXIMUM I_{CC} (nA)	
					SN54ASC'	SN74ASC'
AN220LH	1.75	1	1.75	1.2	228	13.6
IV110LH	0.75	17	12.75	7.48	1785	107.44
IV212LH	1.5	16	24	8	2880	172.8
NO220LH	1.5	1	1.5	0.52	185	11.1
TOTALS		35	44	22.96	5494	330
Label: S245LH A1,A2,A3,A4,A5,A6,A7,A8,B1,B2,B3,B4,B5,B6,B7,B8,GZ,DIR;						

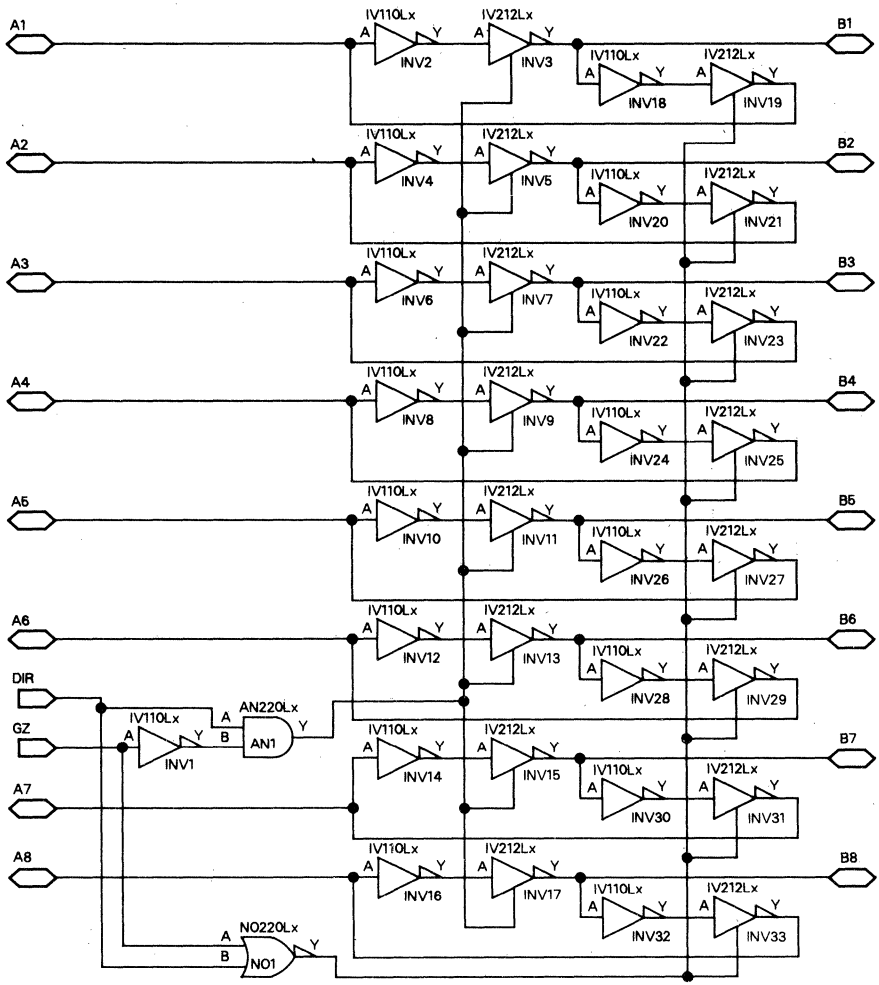
‡The equivalent power dissipation capacitance does not include interconnect capacitance.

The SN54ASC245 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC245 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

CONTROL INPUTS		OPERATION
GZ	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic diagram



absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS		SN54ASC245		SN74ASC245		UNIT
					TYP	MAX	TYP	MAX	
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX	V_I = V_{CC} or 0,		5494		330	nA
C_i	Input capacitance	A or B	V_{CC} = 5 V,	T_A = 25°C	0.30		0.30		pF
		DIR			0.37		0.37		
		GZ			0.36		0.36		
C_o	Output capacitance (reference only, same as A or B)		V_{CC} = 5 V,	T_A = 25°C	0.30		0.30		pF
C_{pd}	Equivalent power dissipation capacitance†		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	22.96		22.96		pF

† The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Notes 1 and 2)

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC245			SN74ASC245			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
t_{pd}	A or B	B or A	C_L = 0		2.4	4.4		2.4	4.4	ns
t_{pd}	DIR	B or A			5	11.3		5	10.3	ns
t_{en}	GZ	A or B			5	11.3		5	10.3	ns
Δt_{pd}	A or B	B or A		0.6	1.7	4.6	0.6	1.7	4.2	ns
Δt_{en}	A or B	B or A		0.7	1.7	4.8	0.7	1.7	4.4	ns/pF

‡ Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{pd} ≡ propagation delay time, low-to-high- or high-to-low-level output
t_{en} ≡ enable time, high impedance state to low- or high-logic-level output
Δt_{pd} ≡ change in t_{pd} with load capacitance
Δt_{en} ≡ change in t_{en} with load capacitance
§ Typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTES 1. These switching characteristics are simulations of the software macro cell using interconnect capacitance values for an array design having 2,000 gates. Post-layout simulation uses actual interconnect capacitance values.
2. Enable and delta-enable times are measured using the conditions specified for the 'ASC2311 (IV212LH).

DESIGN CONSIDERATIONS

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

The HDL for this software macro is included as a part of the library supplied for supported engineering workstations so that a single label can be developed to apply the macro as needed. The following printout of the HDL block definition is furnished for reference.

HDL FILE

```
BLOCK S245LH;
GZ          @INPUT;
DIR         @INPUT;
A1          @INOUT;
A2          @INOUT;
A3          @INOUT;
A4          @INOUT;
A5          @INOUT;
A6          @INOUT;
A7          @INOUT;
A8          @INOUT;
B1          @INOUT;
B2          @INOUT;
B3          @INOUT;
B4          @INOUT;
B5          @INOUT;
B6          @INOUT;
B7          @INOUT;
B8          @INOUT;

STRUCTURE
AN1         :AN220LH        DIR,INV1O,AN1O;
INV1        :IV110LH        GZ,INV1O;
INV10       :IV110LH        A5,INV0O;
INV11       :IV212LH        INV10O,AN1O,B5;
INV12       :IV110LH        A6,INV12O;
INV13       :IV212LH        INV12O,AN1O,B6;
INV14       :IV110LH        A7,INV14O;
INV15       :IV212LH        INV14O,AN1O,B7;
INV16       :IV110LH        A8,INV16O;
INV17       :IV212LH        INV16O,AN1O,B8;
INV18       :IV110LH        B1,INV18O;
INV19       :IV212LH        INV18O,NO1O,A1;
INV2        :IV110LH        A1,INV2O;
INV20       :IV110LH        B2,INV20O;
INV21       :IV212LH        INV20O,NO1O,A2;
INV22       :IV110LH        B3,INV22O;
INV23       :IV212LH        INV22O,NO1O,A3;
INV24       :IV110LH        B4,INV24O;
INV25       :IV212LH        INV24O,NO1O,A4;
INV26       :IV110LH        B5,INV26O;
INV27       :IV212LH        INV26O,NO1O,A5;
INV28       :IV110LH        B6,INV28O;
INV29       :IV212LH        INV28O,NO1O,A6;
INV3        :IV212LH        INV2O,AN1O,B1;
INV30       :IV110LH        B7,INV30O;
INV31       :IV212LH        INV30O,NO1O,A7;
INV32       :IV110LH        B8,INV32O;
INV33       :IV212LH        INV32O,NO1O,A8;
INV4        :IV110LH        A2,INV4O;
```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HDL FILE (Continued)

```
STRUCTURE (Continued)
INV5        :IV212LH        INV4O,AN1O,B2;
INV6        :IV110LH        A3,INV6O;
INV7        :IV212LH        INV6O,AN1O,B3;
INV8        :IV110LH        A4,INV8O;
INV9        :IV212LH        INV8O,AN1O,B4;
NO1         :NO220LH        GZ,DIR,NO1O;
END S245LH;
```

Hardwired internal cells with 3-state outputs are also available in the standard cell library. These hardwired cells should be considered if the interface is in a critical path, as their performance is predetermined as specified in their switching characteristics.

interfacing the macro

Inputs and outputs of the predesigned macro are compatible for interfacing directly with cells and macros available in the TI standard cell library.

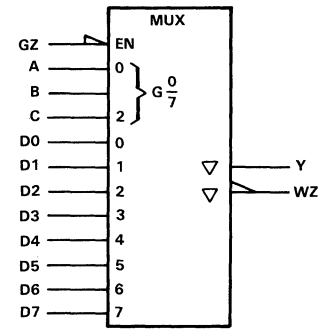
The inputs can be driven by either inverting or noninverting input cells. The outputs can be interfaced to drive off-chip loads with any of the noninverting output buffers or interfaced to external bidirectional buses through a 3-state input/output TTL/CMOS buffer.

D2939, AUGUST 1986

SystemCell™ 2-μm SOFTWARE MACRO CELL

- **3-State Outputs Interface Internal Data Buses Directly**
- **Active-Low Strobe for Expandability**
- **Use Parallel Multiplexers for Multiple-Bit Words**

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The SN54ASC251 and SN74ASC251 are standard-cell software macros implementing 8-line to 1-line multiplexers. The 'ASC251 implements a function table identical with that performed by packaged 'HC251, 'LS251, 'S251, and 'F251 multiplexers.

The macro has a strobe input GZ, that enables and disables the 3-state outputs to facilitate interfacing the multiplexer directly with internal control or data buses. The Y output and the WZ output are in a high-impedance state when GZ is high. When GZ is low, the Y output assumes the level of the selected input and the WZ output assumes the complement of that level. This strobe permits the macro to also be employed for designing wider multiplexers, as only the enabled 8-bit field will output an active data bit. The 'ASC251 is implemented with standard cell functions indicated. The HDL netlist label for this software macro is shown on the last line of the following table:

CELL NAME	RELATIVE CELL AREA TO NA210LH	NO. USED	TOTAL RELATIVE CELL AREA	TOTAL C_{pd}‡ (pF)	MAXIMUM I_{CC} (nA)	
					SN54ASC'	SN74ASC'
IV110LH	0.75	3	2.25	1.32	315	19
IV120LH	1	4	4	3.2	524	31.44
IV212LH	1.5	2	3	3.72	360	21.6
NA410LH	1.5	8	12	4	1496	89.6
NA810LH	2.5	1	2.5	0.61	290	17.4
TOTALS		18	23.75	12.85	2985	180
Label: S251LH GZ,A,B,C,D0,D1,D2,D3,D4,D5,D6,D7,Y,WZ;						

‡ The equivalent power dissipation capacitance does not include interconnect capacitance.

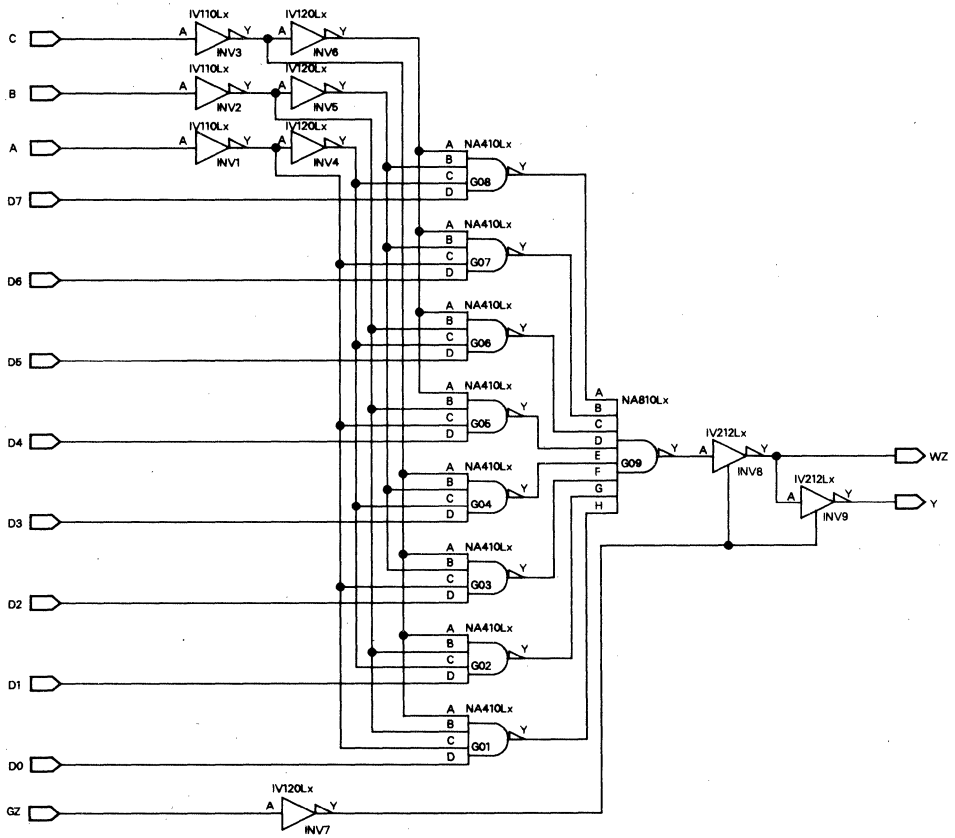
The SN54ASC251 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC251 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

INPUTS				OUTPUTS	
SELECT			STROBE	Y	WZ
C	B	A	GZ		
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

D0,D1 . . . D7 = the level of the respective D input.

logic diagram



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absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS	SN54ASC251		SN74ASC251		UNIT
				TYP	MAX	TYP	MAX	
V_T	Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current		V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} to 0, T_A = MIN to MAX		2985		180	nA
C_i	Input capacitance	GZ	V_{CC} = 5 V, T_A = 25°C	0.24		0.24		pF
		All other inputs		0.12		0.12		
C_{pd}	Equivalent power dissipation capacitance†		V_{CC} = 5 V, T_A = 25°C, t_r = t_f = 3 ns,	12.85		12.85		pF

† The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Notes 1 and 2)

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC251			SN74ASC251			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
t_{pd}	A, B, or C	Y	C_L = 0		9.7	22.2		9.7	19.8	ns
t_{pd}		WZ			8.7	20.3		8.7	18.1	
t_{pd}	Any D	Y			7.7	18.5		7.7	16.4	ns
t_{pd}		WZ			6.8	16.6		6.8	14.7	
t_{en}	GZ	Y			3.1	5.6		3.1	5.2	ns
t_{en}		WZ			2.1	4.2		2.1	3.9	
Δt_{pd}	Any	Y,WZ		0.6	1.7	4.6	0.6	1.7	4.2	ns/pF
Δt_{en}	Any	Y,WZ		0.7	1.7	4.8	0.7	1.7	4.4	

‡ Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{pd} ≡ propagation delay time, low-to-high-level or high-to-low-level output
t_{en} ≡ enable time, high-impedance state to low- or high-logic-level output
Δt_{pd} ≡ change in t_{pd} with load capacitance
Δt_{en} ≡ change in t_{en} with load capacitance
§ Typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTES: 1. These switching characteristics are simulations of the software macro cell using interconnect capacitance values for an array design having 2,000 gates. Post-layout simulation uses actual interconnect capacitance values.
2. Enable and delta-enable times are measured using the conditions specified for the 'ASC2311 (IV212LH).

DESIGN CONSIDERATIONS

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

The HDL for this software macro is included as a part of the library supplied for supported engineering workstations so that a single label can be developed to apply the macro as needed. The following printout of the HDL block definition is furnished for reference.

HDL FILE

```
BLOCK S251LH;
GZ          @INPUT;
A           @INPUT;
B           @INPUT;
C           @INPUT;
D0          @INPUT;
D1          @INPUT;
D2          @INPUT;
D3          @INPUT;
D4          @INPUT;
D5          @INPUT;
D6          @INPUT;
D7          @INPUT;
Y           @OUTPUT;
WZ          @OUTPUT;

STRUCTURE
G01         :NA410LH        CZ,BZ,AZ,D0,U0;
G02         :NA410LH        CZ,BZ,AT,D1,U1;
G03         :NA410LH        CZ,BT,AZ,D2,U2;
G04         :NA410LH        CZ,BT,AT,D3,U3;
G05         :NA410LH        CT,BZ,AZ,D4,U4;
G06         :NA410LH        CT,BZ,AT,D5,U5;
G07         :NA410LH        CT,BT,AZ,D6,U6;
G08         :NA410LH        CT,BT,AT,D7,U7;
G09         :NA810LH        U7,U6,U5,U4,U3,U2,U1,U0,YINT;
INV1        :IV110LH        A,AZ;
INV2        :IV110LH        B,BZ;
INV3        :IV110LH        C,CZ;
INV4        :IV120LH        AZ,AT;
INV5        :IV120LH        BZ,BT;
INV6        :IV120LH        CZ,CT;
INV7        :IV120LH        GZ,INV7O;
INV8        :IV212LH        YINT,INV7O,WZ;
INV9        :IV212LH        WZ,INV7O;Y;
END S251LH;
```

Dedicated 8-line to 1-line multiplexers, 'SC2342, are also available in the standard cell library for implementing data-path multiplexers. The 'SC2342 cell incorporates an enable input that can be used for expanding the word width. These hard-wired cells should be considered if the multiplexer is in a critical path, as their performance is predetermined as specified in their switching characteristics.

interfacing the macro

Inputs and outputs of the predesigned macro are compatible for interfacing directly with cells and macros available in the TI standard cell library. The 3-state outputs can interface internal bidirectional buses.

The inputs can be driven by either inverting or noninverting input cells. The outputs can be interfaced to drive off-chip loads with any of the noninverting output buffers or interfaced to external bidirectional buses through a 3-state input/output TTL/CMOS buffer. If bus interface is not required, the 'ASC151 8-line to 1-line multiplexer provides totem-pole outputs.

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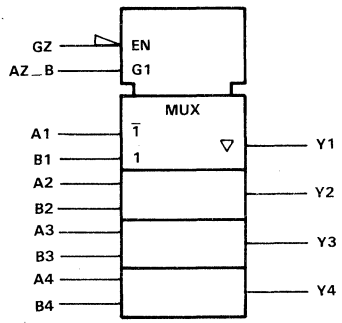
SystemCell™ 2-μm SOFTWARE MACRO CELL

- **3-State Outputs Interface with Internal Data Buses Directly**
- **Active-Low Enable for Expandability**
- **Use Parallel Multiplexers for Multiple-Bit Words**

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The SN54ASC257A and SN74ASC257A are standard-cell software macros implementing 2-line to 1-line multiplexers. The 'ASC257A implements a function table identical with that performed by packaged 'HC257, 'LS257, 'S257, and 'F257 multiplexers.

The macro has an enable input, GZ, that enables and disables the 3-state outputs to facilitate interfacing the multiplexer directly with internal control or data buses. The Y outputs are in a high-impedance state when GZ is high. When GZ is low, the outputs assume the levels of the selected inputs. This enable permits the macro to also be employed for designing wider multiplexers, as only the enabled 2-bit field will output an active data bit. The 'ASC257A is implemented with standard cell functions indicated. The HDL netlist label for this software macro is shown on the last line of the following table:

CELL NAME	RELATIVE CELL AREA TO NA210LH	NO. USED	TOTAL RELATIVE CELL AREA	TOTAL C_{pd}‡ (pF)	MAXIMUM I_{CC} (nA)	
					SN54ASC'	SN74ASC'
IV110LH	0.75	10	7.5	4.4	1050	63.2
IV212LH	1.5	8	12	4	1440	86.4
AN220LH	1.75	2	3.5	2.4	456	27.2
TOTALS		20	23	10.8	2946	177
Label: S257ALH A1,A2,A3,A4,B1,B2,B3,B4,GZ,AZ_B,Y1,Y2,Y3,Y4;						

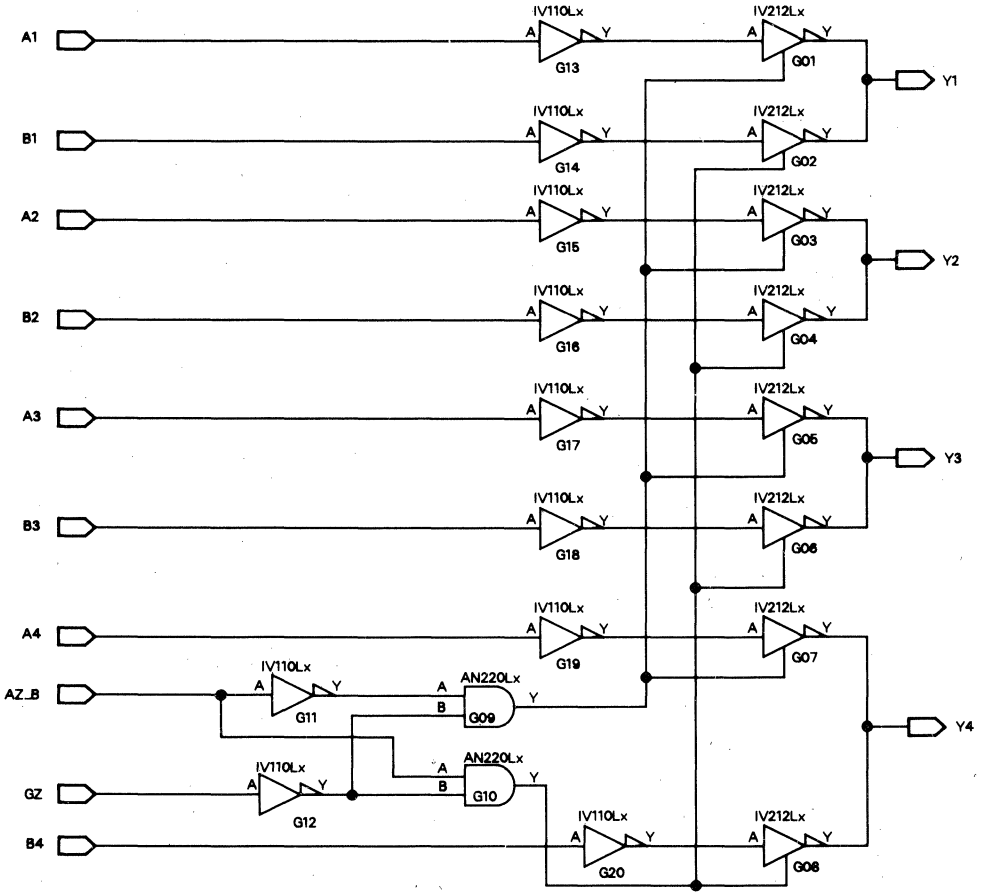
‡The equivalent power dissipation capacitance does not include interconnect capacitance.

The SN54ASC257A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC257A is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

INPUTS				OUTPUT
ENABLE	SELECT	DATA		
GZ	AZ_B	A	B	Y
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

logic diagram



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absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS	SN54ASC257A		SN74ASC257A		UNIT
				TYP	MAX	TYP	MAX	
V_T	Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current		V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		2946		177	nA
C_i	Input capacitance	AZ_B	V_{CC} = 5 V, T_A = 25°C	0.25		0.25		pF
		All other inputs		0.12		0.12		
C_{pd}	Equivalent power dissipation capacitance†		V_{CC} = 5 V, T_A = 25°C, t_r = t_f = 3 ns,	10.8		10.8		pF

† The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Notes 1 and 2)

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC257A			SN74ASC257A			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
t_{pd}	Any A or B	Y	C_L = 0		2.7	5.2		2.7	4.8	ns
t_{pd}	AZ_B	Y			5	10.4		5	9.5	ns
t_{en}	GZ	Y			5	10.7		5	9.8	ns
Δt_{pd}	Any	Y		0.6	1.7	4.6	0.6	1.7	4.2	ns
Δt_{en}	Any	Y		0.7	1.7	4.8	0.7	1.7	4.4	ns/pF

‡ Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{pd} ≡ propagation delay time, low-to-high-level or high-to-low-level output
t_{en} ≡ enable time, high-impedance state to low- or high-logic-level output
Δt_{pd} ≡ change in t_{pd} with load capacitance
Δt_{en} ≡ change in t_{en} with load capacitance
§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTES: 1. These switching characteristics are simulations of the software macro cell using interconnect capacitance values for an array design having 2,000 gates. Post-layout simulation uses actual interconnect capacitance values.
2. Enable and delta-enable times are measured using the conditions specified for the 'ASC2311.

DESIGN CONSIDERATIONS

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

The HDL for this software macro is included as a part of the library supplied for supported engineering workstations so that a single label can be developed to apply the macro as needed. The following printout of the HDL block definition is furnished for reference.

HDL FILE

```
BLOCK S257ALH;
A1          @INPUT;
A2          @INPUT;
A3          @INPUT;
A4          @INPUT;
B1          @INPUT;
B2          @INPUT;
B3          @INPUT;
B4          @INPUT;
GZ          @INPUT;
AZ_B        @INPUT;
Y1          @OUTPUT;
Y2          @OUTPUT;
Y3          @OUTPUT;
Y4          @OUTPUT;

STRUCTURE
G01         :IV212LH        G13O,G09O,Y1;
G02         :IV212LH        G14O,G10O,Y1;
G03         :IV212LH        G15O,G09O,Y2;
G04         :IV212LH        G16O,G10O,Y2;
G05         :IV212LH        G17O,G09O,Y3;
G06         :IV212LH        G18O,G10O,Y3;
G07         :IV212LH        G19O,G09O,Y4;
G08         :IV212LH        G20O,G10O,Y4;
G09         :AN220LH        G11O,G12O,G09O;
G10         :AN220LH        AZ_B,G12O,G10O;
G11         :IV110LH        AZ_B,G11O;
G12         :IV110LH        GZ,G12O;
G13         :IV110LH        A1,G13O;
G14         :IV110LH        B1,G14O;
G15         :IV110LH        A2,G15O;
G16         :IV110LH        B2,G16O;
G17         :IV110LH        A3,G17O;
G18         :IV110LH        B3,G18O;
G19         :IV110LH        A4,G19O;
G20         :IV110LH        B4,G20O;
END S257ALH;
```

Dedicated 2-line to 1-line multiplexers, 'SC2340, are also available in the standard cell library for implementing data-path multiplexers. The 'SC2340 cell incorporates an enable input which can be used for expanding the word width. These hardwired cells should be considered if the multiplexer is in a critical path, as their performance is predetermined as specified in their switching characteristics.

interfacing the macro

Inputs and outputs of the predesigned macro are compatible for interfacing directly with cells and macros available in the TI standard cell library. The 3-state outputs can interface internal bidirectional buses.

The inputs can be driven by either inverting or noninverting input cells. The outputs can be interfaced to drive off-chip loads with any of the noninverting output buffers or interfaced to external bidirectional buses through a 3-state input/output TTL/CMOS buffer. If bus interface is not required, the 'ASC157 2-line to 1-line multiplexer provides totem-pole outputs.

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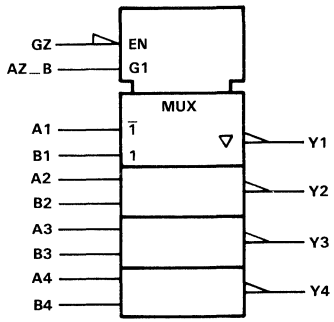
SystemCell™ 2-μm SOFTWARE MACRO CELL

- **3-State Outputs Interface with Internal Data Buses Directly**
- **Active-Low Enable for Expandability**
- **Use Parallel Multiplexers for Multiple-Bit Words**

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The SN54ASC258A and SN74ASC258A are standard-cell software macros implementing 2-line to 1-line multiplexers. The 'ASC258A implements a function table identical with that performed by packaged 'HC258, 'LS258, 'S258, and 'F258 multiplexers.

The macro has an enable input, GZ, that enables and disables the 3-state outputs to facilitate interfacing the multiplexer directly with internal control or data buses. The Yn outputs are in a high-impedance state when GZ is high. When GZ is low, the output assumes the complement of the level of the selected input. This enable permits the macro to also be employed for designing wider multiplexers, as only the enabled 2-bit field will output an active data bit. The 'ASC258A is implemented with standard cell functions indicated. The HDL netlist label for this software macro is shown on the last line of the following table:

CELL NAME	RELATIVE CELL AREA TO NA210LH	NO. USED	TOTAL RELATIVE CELL AREA	TOTAL C_{pd}‡ (pF)	MAXIMUM I_{CC} (nA)	
					SN54ASC'	SN74ASC'
IV110LH	0.75	2	1.5	0.88	210	12.64
IV212LH	1.5	8	12	4	1440	86.4
AN220LH	1.75	2	3.5	2.4	456	27.2
TOTALS		12	17	7.28	2106	127
Label: S258ALH A1,A2,A3,A4,B1,B2,B3,B4,GZ,AZ_B,Y1,Y2,Y3,Y4;						

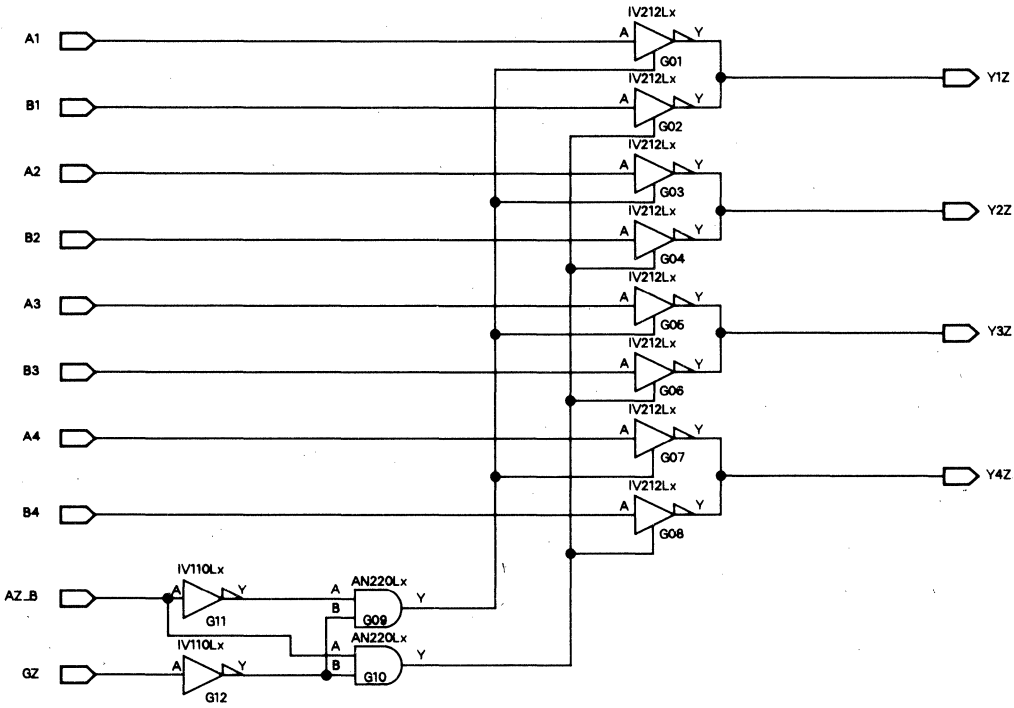
‡ The equivalent power dissipation capacitance does not include interconnect capacitance.

The SN54ASC258A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC258A is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

INPUTS				OUTPUT
ENABLE	SELECT	DATA		
GZ	AZ_B	A	B	Y
H	X	X	X	Z
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

logic diagram



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absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER		TEST CONDITIONS	SN54ASC258A		SN74ASC258A		UNIT
			TYP	MAX	TYP	MAX	
V_T Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC} Supply current		V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		2106		127	nA
C_i Input capacitance	AZ_B	V_{CC} = 5 V, T_A = 25°C	0.25		0.25		pF
	All other inputs		0.12		0.12		
C_{pd} Equivalent power dissipation capacitance†		V_{CC} = 5 V, T_A = 25°C, t_r = t_f = 3 ns,	7.28		7.28		pF

† The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Notes 1 and 2)

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC258A			SN74ASC258A			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
t_{pd}	Any A or B	Y	C_L = 0		1.4	2.8		1.4	2.5	ns
t_{pd}	AZ_B	Y			5	10.4		5	9.5	ns
t_{en}	GZ	Y			5	10.7		5	9.8	ns
Δt_{pd}	Any	Y		0.6	1.7	4.6	0.6	1.7	4.2	ns/pF
Δt_{en}	Any	Y		0.7	1.7	4.8	0.7	1.7	4.4	ns/pF

‡ Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{pd} ≡ propagation delay time, low-to-high-level or high-to-low-level output
t_{en} ≡ enable time, high impedance state to low- or high-logic-level output
Δt_{pd} ≡ change in t_{pd} with load capacitance
Δt_{en} ≡ change in t_{en} with load capacitance
§ Typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTES: 1. These switching characteristics are simulations of the software macro cell using interconnect capacitance values for an array design having 2,000 gates. Post-layout simulation uses actual interconnect capacitance values.
2. Enable and delta-enable times are measured using the conditions specified for the 'ASC2311 (IV212LH).

DESIGN CONSIDERATIONS

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

The HDL for this software macro is included as a part of the library supplied for supported engineering workstations so that a single label can be developed to apply the macro as needed. The following printout of the HDL block definition is furnished for reference.

HDL FILE

```
BLOCK S258ALH;
A1          @INPUT;
A2          @INPUT;
A3          @INPUT;
A4          @INPUT;
B1          @INPUT;
B2          @INPUT;
B3          @INPUT;
B4          @INPUT;
GZ          @INPUT;
AZ_B        @INPUT;
Y1          @OUTPUT;
Y2          @OUTPUT;
Y3          @OUTPUT;
Y4          @OUTPUT;

STRUCTURE
G01         :IV212LH        A1,G09O,Y1;
G02         :IV212LH        B1,G10O,Y1;
G03         :IV212LH        A2,G09O,Y2;
G04         :IV212LH        B2,G10O,Y2;
G05         :IV212LH        A3,G09O,Y3;
G06         :IV212LH        B3,G10O,Y3;
G07         :IV212LH        A4,G09O,Y4;
G08         :IV212LH        B4,G10O,Y4;
G09         :AN220LH        G11O,G12O,G09O;
G10         :AN220LH        AZ_B,G12O,G10O;
G11         :IV110LH        AZ_B,G11O;
G12         :IV110LH        GZ,G12O;
END S258ALH;
```

Dedicated 2-line to 1-line multiplexers are also available in the standard cell library ('SC2340) for implementing data-path multiplexers. The 'SC2340 cell incorporates an enable input which can be used for expanding the word width. These hard-wired cells should be considered if the multiplexer is in a critical path, as their performance is predetermined as specified in their switching characteristics.

interfacing the macro

Inputs and outputs of the predesigned macro are compatible for interfacing directly with cells and macros available in the TI standard cell library. The 3-state outputs can interface internal bidirectional buses.

The inputs can be driven by either inverting or noninverting input cells. The outputs can be interfaced to drive off-chip loads with any of the noninverting output buffers or interfaced to external bidirectional buses through a 3-state I/O TTL/CMOS buffer. If bus interface is not required, the 'ASC158 2-line to 1-line multiplexer provides totem-pole outputs.

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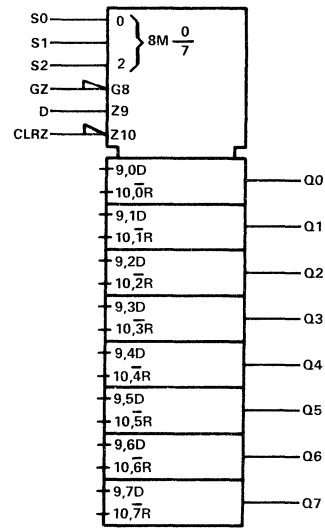
SystemCell™ 2-μm SOFTWARE MACRO CELL

- **Parallel-Out Register Performs Serial-to-Parallel Conversion with Storage**
- **Expandable for N-Bit Applications**
- **Enable/Disable Input Simplifies Expansion**
- **Four Functional Modes:**
  - **Addressable Transparent Latch**
  - **Parallel 8-Bit Storage Latch**
  - **1-of-8 Demultiplexer**
  - **Asynchronous Parallel Clear**

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

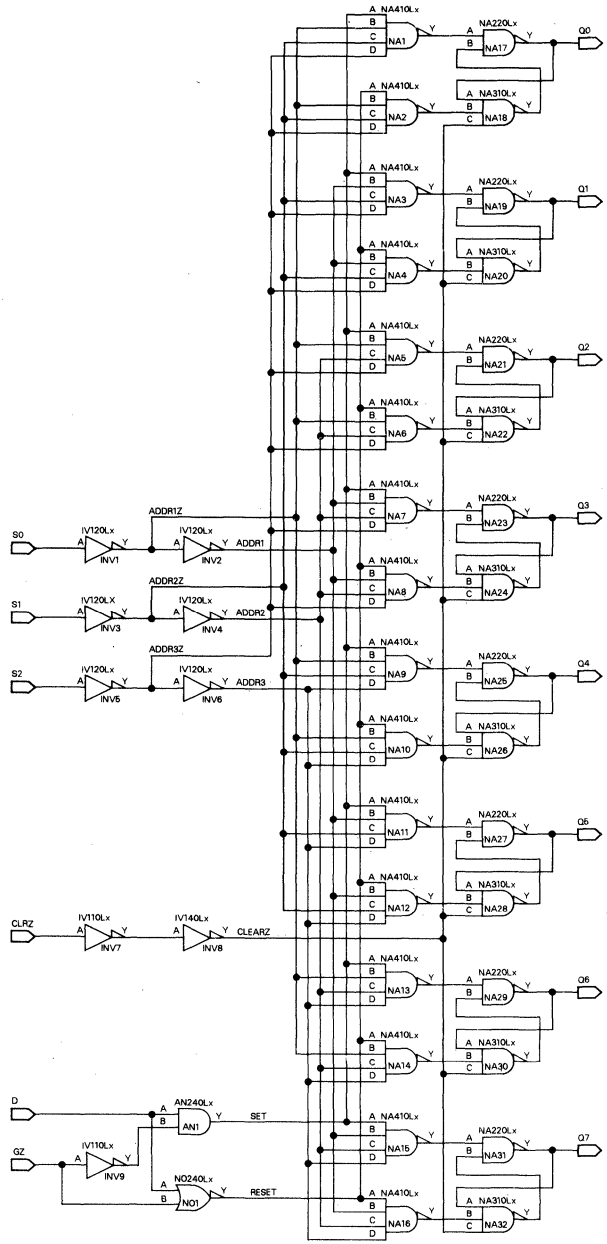
The SN54ASC259 and SN74ASC259 are standard-cell software macros implementing addressable 8-bit parallel latches. The 8-bit configuration provides the custom IC designer a fully designed addressable register/demultiplexer to embed in ASICs in its most efficient form, and its 8-bit length simplifies construction of large latches. The 'ASC259 implements an addressable latch function identical with that performed by packaged 'HC259, 'LS259, and 'F259 latches.

These 8-bit addressable latches are designed for general purpose storage applications where demultiplexing and/or addressable bit storage locations are useful co-functions. Some uses include working registers, serial-holding registers, and active-high decoders or demultiplexers. They are multifunction macros capable of storing single-line data in eight addressable latches or of implementing a 1-of-N line decoder or demultiplexer with active-high outputs. The 'ASC259 is implemented with the standard cell functions indicated. The HDL netlist label for this software macro is shown on the last line of the following table:

CELL NAME	RELATIVE CELL AREA TO NA210LH	NO. USED	TOTAL RELATIVE CELL AREA	TOTAL C_{pd}‡ (pF)	MAXIMUM I_{CC} (nA)	
					SN54ASC'	SN74ASC'
AN240LH	2.25	1	2.25	2.32	286	17.2
IV110LH	0.75	2	1.5	0.88	210	12.64
IV120LH	1	6	6	4.8	786	47.1
IV140LH	1.5	1	1.5	1.61	190	11.4
NA220LH	1.5	8	12	8	1568	93.6
NA310LH	1.25	8	10	4	1304	78.24
NA410LH	1.5	16	24	8	2992	179.2
NO240LH	2.5	1	2.5	0.98	292	17.5
TOTALS		43	59.75	40.59	7528	457
Label: S259LH CLRZ,D,GZ,S0,S1,S2,Q0,Q1,Q2,Q3,Q4,Q5,Q6,Q7;						

‡The equivalent power dissipation capacitance does not include interconnect capacitance.

logic diagram



Four distinct modes of operation are selectable by controlling the clear (CLRZ) and enable (GZ) inputs as shown in the function table. In the addressable-latch mode, data at the data-in input D are written into the addressed latch. The addressed latch will follow the data input with remaining unaddressed latches retaining their previous states. In the memory mode, all latches remain in their previous states and are not affected by changes at the data or address inputs. To preclude entering erroneous data in the latches, enable GZ should be held high (inactive) while the address lines are changed. In the 1-of-8 decoding or demultiplexing mode, the addressed output will follow the level at the D input with the remaining outputs low. In the clear mode, all outputs are set low and are not affected by address and data changes.

The SN54ASC259 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC259 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

INPUTS		OUTPUT OF ADDRESSED LATCH	EACH OTHER OUTPUT	FUNCTION
CLRZ	GZ			
H	L	D	Qi_0	Addressable Latch
H	H	Qi_0	Qi_0	Memory
L	L	D	L	8-Line Demultiplexer
L	H	L	L	Clear

D = the level at the data input
Qi_0 = the level of Qi (i = 0, 1, . . . 7, as appropriate) before the indicated steady-input conditions were established.

LATCH SELECTION TABLE

SELECT INPUTS			LATCH
S0	S1	S2	ADDRESSED
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS	SN54ASC259 TYP	SN54ASC259 MAX	SN74ASC259 TYP	SN74ASC259 MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current		V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		7528		457	nA
C_i	Input capacitance	S0,S1,S2	V_{CC} = 5 V, T_A = 25°C	0.24		0.24		pF
		D		0.13		0.13		
		CLRZ, GZ		0.6		0.6		
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, t_r = t_f = 3 ns, T_A = 25°C	40.59		40.59		pF

switching characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted) (see Note 1)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC259			SN74ASC259			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{pd}	S0, S1, S2	Qn	C_L = 0		6	12		6	11	ns
t_{pd}	D	Qn			5	12.2		5	11.2	ns
t_{pd}	GZ	Qn			6	13.4		6	12	ns
t_{PHL}	CLR				5	9.9		5	9.3	ns
Δt_{pd}	Any	Any		0.3	0.6	1.3	0.3	0.6	1.1	ns/pF

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{pd} ≡ propagation delay time, low-to-high-level or high-to-low-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{pd} ≡ change in t_{pd} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: These switching characteristics are simulations of the software macro cell using interconnect capacitance values for an array design having 2,000 gates. Post-layout simulation uses actual interconnect capacitance values.

DESIGN CONSIDERATIONS

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

The HDL for this software macro is included as a part of the library supplied for supported engineering workstations so that a single label can be developed to apply the macro as needed. The following printout of the HDL block definition is furnished for reference.

HDL FILE

```
BLOCK S259LH;
CLRZ        @INPUT;
D           @INPUT;
GZ          @INPUT;
S0          @INPUT;
S1          @INPUT;
S2          @INPUT;
Q0          @OUTPUT;
Q1          @OUTPUT;
Q2          @OUTPUT;
Q3          @OUTPUT;
Q4          @OUTPUT;
Q5          @OUTPUT;
Q6          @OUTPUT;
Q7          @OUTPUT;

STRUCTURE
AN1         :AN240LH        D,G,SET;
INV1        :IV120LH        S0,ADDR1Z;
INV2        :IV120LH        ADDR1Z,ADDR1;
INV3        :IV120LH        S1,ADDR2Z;
INV4        :IV120LH        ADDR2Z,ADDR2;
INV5        :IV120LH        S2,ADDR3Z;
INV6        :IV120LH        ADDR3Z,ADDR3;
```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HDL FILE (Continued)

```
STRUCTURE (Continued)
INV7        :IV110LH        CLRZ,CLEAR;
INV8        :IV140LH        CLEAR,CLEARZ;
INV9        :IV110LH        GZ,G;
NA1         :NA410LH        SET,ADDR1Z,ADDR2Z,ADDR3Z,SET0Z;
NA2         :NA410LH        RESET,ADDR1Z,ADDR2Z,ADDR3Z,RESET0Z;
NA3         :NA410LH        SET,ADDR1,ADDR2Z,ADDR3Z,SET1Z;
NA4         :NA410LH        RESET,ADDR1,ADDR2Z,ADDR3Z,RESET1Z;
NA5         :NA410LH        SET,ADDR1Z,ADDR2,ADDR3Z,SET2Z;
NA6         :NA410LH        RESET,ADDR1Z,ADDR2,ADDR3Z,RESET2Z;
NA7         :NA410LH        SET,ADDR1,ADDR2,ADDR3Z,SET3Z;
NA8         :NA410LH        RESET,ADDR1,ADDR2,ADDR3Z,RESET3Z;
NA9         :NA410LH        SET,ADDR1Z,ADDR2Z,ADDR3,SET4Z;
NA10        :NA410LH        RESET,ADDR1Z,ADDR2Z,ADDR3,RESET4Z;
NA11        :NA410LH        SET,ADDR1,ADDR2Z,ADDR3,SET5Z;
NA12        :NA410LH        RESET,ADDR1,ADDR2Z,ADDR3,RESET5Z;
NA13        :NA410LH        SET,ADDR1Z,ADDR2,ADDR3,SET6Z;
NA14        :NA410LH        RESET,ADDR1Z,ADDR2,ADDR3,RESET6Z;
NA15        :NA410LH        SET,ADDR1,ADDR2,ADDR3,SET7Z;
NA16        :NA410LH        RESET,ADDR1,ADDR2,ADDR3,RESET7Z;
NA17        :NA220LH        SET0Z,Q0Z,Q0;
NA18        :NA310LH        Q0,RESET0Z,CLEARZ,Q0Z;
NA19        :NA220LH        SET1Z,Q1Z,Q1;
NA20        :NA310LH        Q1,RESET1Z,CLEARZ,Q1Z;
NA21        :NA220LH        SET2Z,Q2Z,Q2;
NA22        :NA310LH        Q2,RESET2Z,CLEARZ,Q2Z;
NA23        :NA220LH        SET3Z,Q3Z,Q3;
NA24        :NA310LH        Q3,RESET3Z,CLEARZ,Q3Z;
NA25        :NA220LH        SET4Z,Q4Z,Q4;
NA26        :NA310LH        Q4,RESET4Z,CLEARZ,Q4Z;
NA27        :NA220LH        SET5Z,Q5Z,Q5;
NA28        :NA310LH        Q5,RESET5Z,CLEARZ,Q5Z;
NA29        :NA220LH        SET6Z,Q6Z,Q6;
NA30        :NA310LH        Q6,RESET6Z,CLEARZ,Q6Z;
NA31        :NA220LH        SET7Z,Q7Z,Q7;
NA32        :NA310LH        Q7,RESET7Z,CLEARZ,Q7Z;
NO1         :NO240LH        D,GZ,RESET;
END S259LH;
```

designing for testability

Designs employing storage or bistable elements, especially long counters (ripple or synchronous), should consider testability of the design in its final form. The need to preset or clear and read intermediate stages of these elements should be assessed throughout the development of custom logic circuits with these considerations extended to the end-equipment application with respect to maintainability. Simple actions on the part of the ASIC designer can result in considerable cost savings, allowing the expense of IC testing, system testing, and system maintenance to be reduced significantly.

power-up clear/preset

Standard cell storage elements containing the capability to be asynchronously either preset or cleared may be connected to the SN54ASC2320 or SN74ASC2320 power-up clear cell to achieve system initialization. Access to the clear inputs from other system signals in conjunction with the power-up clear can be facilitated with an AND gate.

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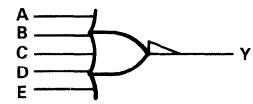
SystemCell™ 2-μm INTERNAL STANDARD CELL

- **Choice of Two Performance Levels**
- **Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V**
- **Functional Operation Over V_{CC} Range of 2 V to 6 V**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol



positive logic equations

$$Y = \overline{A+B+C+D+E} = \overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \overline{D} \cdot \overline{E}$$

FUNCTION TABLE

INPUTS					OUTPUT
A	B	C	D	E	Y
H	X	X	X	X	L
X	H	X	X	X	L
X	X	H	X	X	L
X	X	X	H	X	L
X	X	X	X	H	L
L	L	L	L	L	H

description

The SN54ASC260 and SN74ASC260 are five-input positive-NOR gate CMOS standard cells implementing the equivalent of one-half of an SN54LS260 or SN74LS260. The standard-cell library contains two physical implementations providing the custom IC designer a choice between two performance levels for optimizing a design. Each option is designated and called from the engineering workstation input using the following cell names to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		TYPICAL DELAY C_L = 1 pF	RELATIVE CELL AREA TO NA210LH
NO510LH	Label: NO5n0LH A,B,C,D,E,Y;	5 ns	1.75
NO520LH		3.2 ns	3

The SN54ASC260 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC260 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS		NO510LH TYP	NO510LH MAX	NO520LH TYP	NO520LH MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current	SN54ASC260	V_{CC} = 4.5 V to 5.5 V,	V_I = V_{CC} or 0,		200		318	nA
		SN74ASC260	T_A = MIN to MAX			12		19.1	
C_i	Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.11		0.23		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	$t_r = t_f$ = 3 ns,	0.37		0.64		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

NO510LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC260			SN74ASC260			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A thru E	Y	C_L = 0	0.7	1.8	5.7	0.7	1.8	5.2	ns
t_{PHL}				1	1.5	3	1	1.5	2.7	
t_{PLH}	A thru E	Y	C_L = 1 pF	3.1	6.8	17.3	3.3	6.8	15.6	ns
t_{PHL}				1.7	3.2	7.8	1.8	3.2	6.8	
Δt_{PLH}	A thru E	Y		2.4	5	11.6	2.6	5	10.5	ns/pF
Δt_{PHL}				0.6	1.7	5.3	0.7	1.7	4.6	

NO520LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC260			SN74ASC260			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A thru E	Y	C_L = 0	0.8	1.6	4.2	0.8	1.6	3.8	ns
t_{PHL}				0.8	1.5	2.9	0.9	1.5	2.6	
t_{PLH}	A thru E	Y	C_L = 1 pF	2	4.2	10.2	2.2	4.2	9.2	ns
t_{PHL}				1.4	2.4	5.3	1.4	2.4	4.6	
Δt_{PLH}	A thru E	Y		1.2	2.6	6	1.3	2.6	5.4	ns/pF
Δt_{PHL}				0.4	0.9	2.5	0.5	0.9	2.2	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to Section 7.

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

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D2939, AUGUST 1986

SystemCell™ 2-μm INTERNAL STANDARD CELL

- 2.4 ns Typical Propagation Delay with 1-pF Load
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H

positive logic equations

$Y = \overline{A \oplus B} = AB + \overline{A}\,\overline{B}$

description

The SN54ASC266 and SN74ASC266 are 2-input exclusive-NOR gate CMOS standard-cell functions implementing the equivalent of one-fourth of an 'LS266 or 'HC266. The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		TYPICAL DELAY C_L = 1 pF	RELATIVE CELL AREA TO NA210LH
EN210LH	Label: EN210LH A,B,Y;	2.4 ns	2.25

The SN54ASC266 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC266 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS		TYP	MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		V
I_{CC}	Supply current	SN54ASC266	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0,			272	nA
		SN74ASC266	T_A = MIN to MAX			16.3	
C_i	Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.28		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	$t_r = t_f$ = 3 ns,	1.09		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC266			SN74ASC266			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A or B	Y	C_L = 0	0.5	1.3	2.9	0.6	1.3	2.6	ns
t_{PHL}				0.9	1.5	3.3	0.9	1.5	3	
t_{PLH}	A or B	Y	C_L = 1 pF	1.1	2.3	5.2	1.1	2.3	4.7	ns
t_{PHL}				1.3	2.4	5.7	1.4	2.4	5	
Δt_{PLH}	A or B	Y		0.5	1	2.3	0.5	1	2.1	ns/pF
Δt_{PHL}				0.4	0.9	2.5	0.4	0.9	2.1	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to Section 7.

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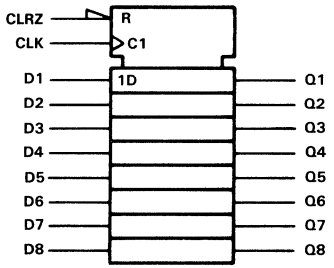
D2939, AUGUST 1986

SystemCell™ 2-μm SOFTWARE MACRO CELL

- 8-Bit Software Register
- Direct Clear Input Simplifies Initialization or Pattern Length
- Buffered Clear Simplifies System Design
- Cascadable and Expandable for Full Customization

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The SN54ASC273 and SN74ASC273 are standard-cell software macros implementing 8-bit register elements for embedding in ASICs in their most efficient form. The 8-bit length simplifies construction of large registers. The 'ASC273 implements a function table identical with that performed by packaged 'HC273, 'LS273, and 'F273 registers.

The software macro reduces the input loading for implementation of larger registers, as standard library cells are used to buffer the clear input. The 'ASC273 is implemented with the standard cell functions indicated. The HDL netlist label for this software macro is shown on the last line of the following table:

CELL NAME	RELATIVE CELL AREA TO NA210LH	NO. USED	TOTAL RELATIVE CELL AREA	TOTAL C_{pd}‡ (pF)	MAXIMUM I_{CC} (nA)	
					SN54ASC'	SN74ASC'
IV110LH	0.75	1	0.75	0.44	105	6.32
IV140LH	1.5	1	1.5	1.61	190	11.4
R2405LH	23.25	2	46.5	20.4	5294	318
TOTALS		4	48.75	22.4	5589	336
Label: S273LH D1,D2,D3,D4,D5,D6,D7,D8,CLK,CLRZ,Q1,Q2,Q3,Q4,Q5,Q6,Q7,Q8;						

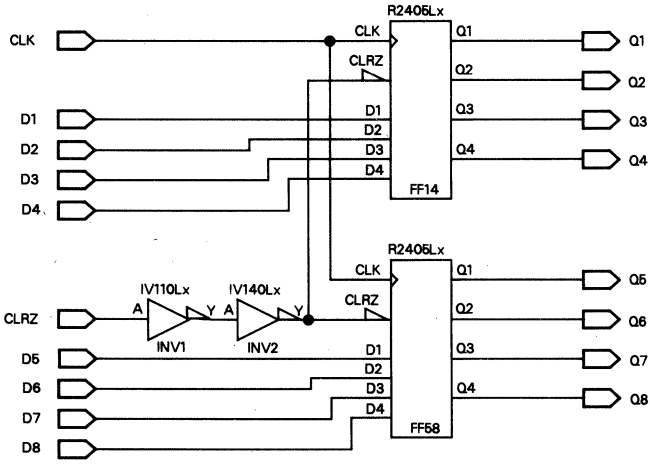
‡ The equivalent power dissipation capacitance does not include interconnect capacitance.

The SN54ASC273 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC273 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUT
CLRZ	CLK	Dn	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

logic diagram



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absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements, made during pre-layout simulation, produce workstation output used to identify and resolve each specific timing need.

electrical characteristics

PARAMETER			TEST CONDITIONS	SN54ASC273		SN74ASC273		UNIT
				TYP	MAX	TYP	MAX	
V_T	Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current		V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} to 0, T_A = MIN to MAX		5589		336	nA
C_i	Input capacitance	CLRZ	V_{CC} = 5 V, T_A = 25°C	0.12		0.12		pF
		Dn		0.13		0.13		
		CLK		0.48		0.48		
C_{pd}	Equivalent power dissipation capacitance†		V_{CC} = 5 V, T_A = 25°C, t_r = t_f = 3 ns,	22.45		22.45		pF

† The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted) (see Note 1)

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC273			SN74ASC273			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
t_{pd}	CLK	Q	C_L = 0		5	10.5		5	9.4	ns
t_{PHL}	CLRZ	Q			5	9.3		5	8.6	ns
Δt_{pd}	Any	Q		0.3	0.8	2.3	0.3	0.8	2.1	ns/pF

‡ Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{pd} ≡ propagation delay time, low-to-high-level or high-to-low-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{pd} ≡ change in t_{pd} with load capacitance
§ Typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: These switching characteristics are simulations of the software macro cell using interconnect capacitance values for an array design having 2,000 gates. Post-layout simulation uses actual interconnect capacitance values.

DESIGN CONSIDERATIONS

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

The HDL for this software macro is included as a part of the library supplied for supported engineering workstations so that a single label can be developed to apply the macro as needed. The following printout of the HDL block definition is furnished for reference.

HDL FILE

```
BLOCK S273LH;
D1          @INPUT;
D2          @INPUT;
D3          @INPUT;
D4          @INPUT;
D5          @INPUT;
D6          @INPUT;
D7          @INPUT;
D8          @INPUT;
CLK         @INPUT;
CLRZ        @INPUT;
Q1          @OUTPUT;
Q2          @OUTPUT;
Q3          @OUTPUT;
Q4          @OUTPUT;
Q5          @OUTPUT;
Q6          @OUTPUT;
Q7          @OUTPUT;
Q8          @OUTPUT;

STRUCTURE
FF14        :R2405LH    INV2O,D1,D2,D3,D4,CLK,Q1,Q2,Q3,Q4;
FF58        :R2405LH    INV2O,D5,D6,D7,D8,CLK,Q5,Q6,Q7,Q8;
INV1        :IV110LH    CLRZ,INV1O;
INV2        :IV140LH    INV1O,INV2O;
END S273LH;
```

designing for testability

Designs employing storage or bistable elements, especially long registers (ripple or synchronous), should consider testability of the design in its final form. The need to preset or clear and read intermediate stages of these elements should be assessed throughout the development of custom logic circuits with these considerations extended to the end-equipment application with respect to maintainability. Simple actions on the part of the ASIC designer can result in considerable cost savings, allowing the expense of IC testing, system testing, and system maintenance to be reduced significantly.

power-up clear/preset

Standard cell storage elements containing the capability to be asynchronously preset or cleared may be connected to the SN54ASC2320 or SN74ASC2320 power-up clear cell to achieve system initialization. Control of the clear or preset inputs from another system signal in conjunction with the power-up clear can be achieved with an AND gate.

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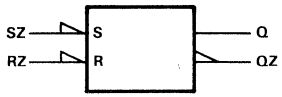
D2939, AUGUST 1986

SystemCell™ 2-μm HARDWIRED MACRO CELLS

- **Provides Complementary Q and QZ Outputs**
- **Choice Between Two Relative Output Drive Capabilities**
- **Implements Control/Status Registers**
- **Parallel Latches to Implement Wide Word Widths**

logic symbol



FUNCTION TABLE

INPUTS		OUTPUTS	
SZ	RZ	Q	QZ
H	H	Q_0	$\overline{Q}_0$
L	H	H	L
H	L	L	H
L	L	H*	H*

*This configuration is nonstable; that is, it will not persist when either SZ or RZ returns to its inactive (H) level.

description

The SN54ASC279 and SN74ASC279 are dedicated, hardwired standard-cell macros implementing S-R latch elements. The 'ASC279 latches offer two choices of individual latch configurations providing the custom IC designer a storage element to embed in ASICs in its most efficient form: as stand-alone bit-storage devices or as additions to larger latched functions. The LAB10LH and LAB20LH latches implement identical function and sequential operation to one-fourth of the 'LS279A packaged latches except both Q and QZ outputs are available on these standard-cell latches. The LAB20LH provides twice the drive capability as the LAB10LH element.

The cells are designated and called from the engineering workstation input using the following cell names to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
LAB10LH	Label: LABn0LH SZ,RZ,Q,QZ;	2.5
LAB20LH		3

The SN54ASC279 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC279 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS	SN54ASC279		SN74ASC279		UNIT
				TYP	MAX	TYP	MAX	
V_T	Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current	LAB10LH	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		311		18.6	nA
		LAB20LH			373		22.4	
C_i	Input capacitance	RZ	V_{CC} = 5 V, T_A = 25°C	0.13		0.13		pF
		SZ		0.12		0.12		
C_{pd}	Equivalent power dissipation capacitance	LAB10LH	V_{CC} = 5 V, t_r = t_f = 3 ns, T_A = 25°C	2.11		2.11		pF
		LAB20LH		3.2		3.2		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

LAB10LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC279			SN74ASC279			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	RZ, SZ	QZ, Q	C_L = 0	1.3	2.4	5.4	1.4	2.4	4.9	ns
t_{PHL}				1	1.6	3.4	1	1.6	3.1	
t_{PLH}	RZ, SZ	QZ, Q	C_L = 1 pF	1.8	3.4	7.6	1.9	3.4	6.9	ns
t_{PHL}				1.3	2.2	4.9	1.3	2.2	4.4	
Δt_{PLH}	RZ, SZ	QZ, Q		0.4	1	2.4	0.5	1	2.1	ns/pF
Δt_{PHL}				0.2	0.6	1.5	0.2	0.6	1.3	

LAB20LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC279			SN74ASC279			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	RZ, SZ	QZ, Q	C_L = 0	1.4	2.7	6.4	1.5	2.7	5.7	ns
t_{PHL}				0.9	1.7	3.6	1	1.7	3.3	
t_{PLH}	RZ, SZ	QZ, Q	C_L = 1 pF	1.6	3.2	7.5	1.7	3.2	6.8	ns
t_{PHL}				1.1	2.1	4.5	1.2	2.1	4.1	
Δt_{PLH}	RZ, SZ	QZ, Q		0.2	0.5	1.2	0.2	0.5	1.1	ns/pF
Δt_{PHL}				0.1	0.4	0.9	0.1	0.4	0.8	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

interfacing the macro

Inputs and outputs of these dedicated macros are compatible for interfacing directly with cells and macros available in the TI standard cell library. The inputs can be driven by either noninverting or inverting input cells. The outputs can be interfaced to drive off-chip loads with any of the noninverting output buffers or interfaced to external bidirectional buses through a 3-state input/output TTL/CMOS buffer.

designing for testability

Designs employing storage or bistable elements should consider testability of the design in its final form. The need to preset or clear these elements should be assessed throughout the development of custom logic circuits with these considerations extended to the end-equipment application with respect to maintainability. Simple actions on the part of the ASIC designer can result in considerable cost savings, allowing the expense of IC testing, system testing, and system maintenance to be reduced significantly.

power-up clear preset

Standard cell storage elements containing the capability to be asynchronously preset or cleared may be connected to the SN54ASC2320 or SN74ASC2320 power-up clear cell to achieve system initialization. Control of the clear or preset inputs from another system signal in conjunction with the power-up clear can be achieved with an AND gate.

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D2939, AUGUST 1986

SystemCell™ 2-μm SOFTWARE MACRO CELL

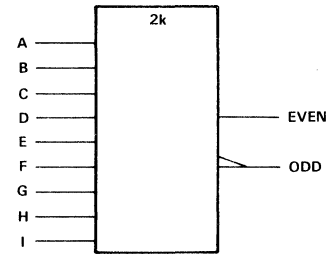
- **Generates Either Odd or Even Parity for Nine Data Lines**
- **Cascadable for n-Bits**
- **Dependable Texas Instruments Quality and Reliability**

description

The SN54ASC280 and SN74ASC280 are standard-cell software macros implementing parallel 9-bit parity generators. The 9-bit configuration provides the custom IC designer a fully designed parity generator to embed in ASICs in its most efficient form, and the 9-bit length simplifies construction of large parity generators. The 'ASC280 implements a parity tree identical with that performed by packaged 'H280, 'LS280, and 'F280 generators.

These universal 9-bit parity generators/checkers feature odd and even outputs to facilitate operation in either odd- or even-parity applications. The word-length capability is easily expanded by cascading. The 'ASC280 is implemented with the standard cell functions indicated. The HDL netlist label for this software macro is shown on the last line of the following table:

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE

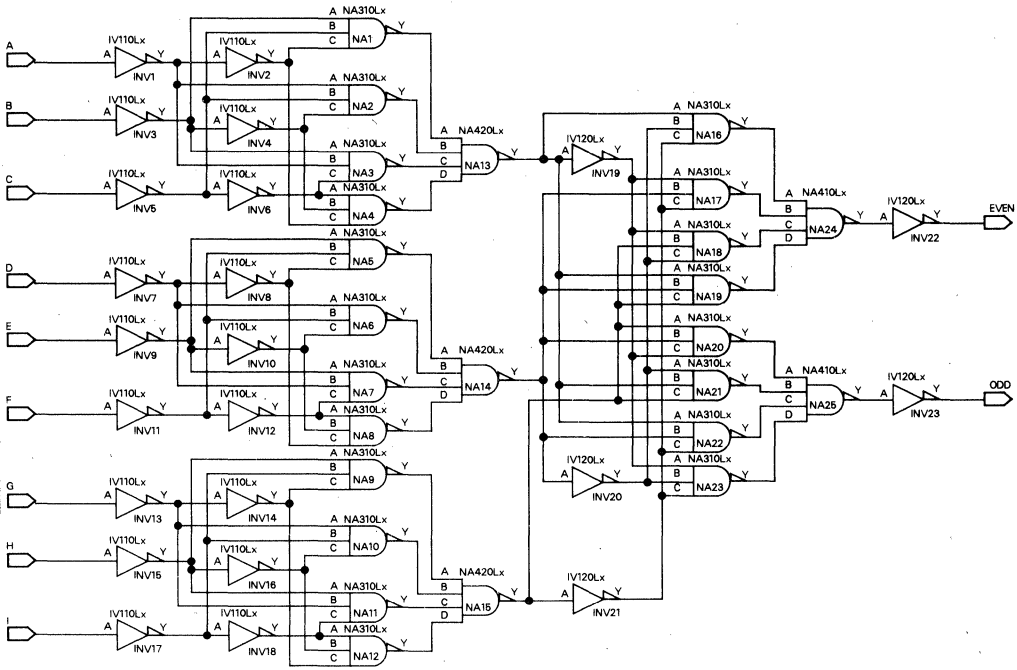
NUMBER OF INPUTS A THRU I THAT ARE HIGH	OUTPUTS	
	EVEN	ODD
0,2,4,6,8	H	L
1,3,5,7,9	L	H

CELL NAME	RELATIVE CELL AREA TO NA210LH	NO. USED	TOTAL RELATIVE CELL AREA	TOTAL C_{pd}‡ (pF)	MAXIMUM I_{CC} (nA)	
					SN54ASC'	SN74ASC'
IV110LH	0.75	18	13.5	7.92	1890	113.76
IV120LH	1	5	5	4	655	39.25
NA310LH	1.25	20	25	10	3260	195.6
NA410LH	1.5	2	3	1	374	22.4
NA420LH	2.5	3	7.5	2.88	936	56.1
TOTALS		48	54	25.8	7115	428
Label: S280LH A,B,C,D,E,F,G,H,I,EVEN,ODD;						

‡The equivalent power dissipation capacitance does not include interconnect capacitance.

The SN54ASC280 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC280 is characterized for operation from −40°C to 85°C.

logic diagram



absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER		TEST CONDITIONS	SN54ASC280		SN74ASC280		UNIT
			TYP	MAX	TYP	MAX	
V_T	Input threshold voltage	V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		7115		428	nA
C_i	Input capacitance	V_{CC} = 5 V, T_A = 25°C	0.12		0.12		pF
C_{pd}	Equivalent power dissipation capacitance†	V_{CC} = 5 V, t_r = t_f = 3 ns, T_A = 25°C	25.8		25.8		pF

† The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted) (see Note 1)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC280			SN74ASC280			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{pd}	Any	EVEN	C_L = 0		11	23.4		11	21.6	ns
t_{pd}	Any	ODD			11	24.4		11	21.9	ns
Δt_{pd}	Any	Any		0.3	0.5	1.1	0.3	0.5	1	ns/pF

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{pd} ≡ propagation delay time, low-to-high- or high-to-low-level output
Δt_{pd} ≡ change in t_{pd} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: These switching characteristics are simulations of the software macro cell using interconnect capacitance values for an array design having 2,000 gates. Post-layout simulation uses actual interconnect capacitance values.

DESIGN CONSIDERATIONS

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

The HDL for this software macro is included as a part of the library supplied for supported engineering workstations so that a single label can be developed to apply the macro as needed. The following printout of the HDL block definition is furnished for reference.

HDL FILE

```
BLOCK S280LH;
A           @INPUT;
B           @INPUT;
C           @INPUT;
D           @INPUT;
E           @INPUT;
F           @INPUT;
G           @INPUT;
H           @INPUT;
I           @INPUT;
EVEN        @OUTPUT;
ODD         @OUTPUT;
```

HDL FILE (Continued)

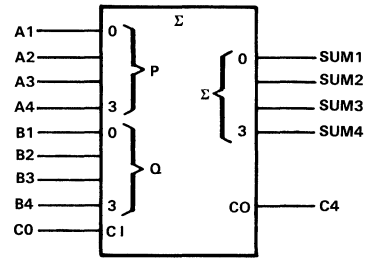
```
STRUCTURE
INV1        :IV110LH        A,INV1O;
INV10       :IV110LH        INV9O,INV10O;
INV11       :IV110LH        F,INV11O;
INV12       :IV110LH        INV11O,INV12O;
INV13       :IV110LH        G,INV13O;
INV14       :IV110LH        INV13O,INV14O;
INV15       :IV110LH        H,INV15O;
INV16       :IV110LH        INV15O,INV16O;
INV17       :IV110LH        I,INV17O;
INV18       :IV110LH        INV17O,INV18O;
INV19       :IV120LH        SNA13,SIV19;
INV2        :IV110LH        INV1O,INV2O;
INV20       :IV120LH        SNA14,SIV20;
INV21       :IV120LH        SNA15,SIV21;
INV22       :IV120LH        SNA24,EVEN;
INV23       :IV120LH        SNA25,ODD;
INV3        :IV110LH        B,INV3O;
INV4        :IV110LH        INV3O,INV4O;
INV5        :IV110LH        C,INV5O;
INV6        :IV110LH        INV5O,INV6O;
INV7        :IV110LH        D,INV7O;
INV8        :IV110LH        INV7O,INV8O;
INV9        :IV110LH        E,INV9O;
NA1         :NA310LH        INV3O,INV5O,INV2O,SNA1;
NA10        :NA310LH        INV13O,INV17O,INV16O,SNA10;
NA11        :NA310LH        INV15O,INV13O,INV18O,SNA11;
NA12        :NA310LH        INV18O,INV16O,INV14O,SNA12;
NA13        :NA420LH        SNA1,SNA2,SNA3,SNA4,SNA13;
NA14        :NA420LH        SNA5,SNA6,SNA7,SNA8,SNA14;
NA15        :NA420LH        SNA9,SNA10,SNA11,SNA12,SNA15;
NA16        :NA310LH        SNA13,SIV20,SIV21,SNA16;
NA17        :NA310LH        SIV19,SNA14,SIV21,SNA17;
NA18        :NA310LH        SIV19,SNA15,SIV20,SNA18;
NA19        :NA310LH        SNA13,SNA14,SNA15,SNA19;
NA2         :NA310LH        INV1O,INV5O,INV4O,SNA2;
NA20        :NA310LH        SNA15,SNA14,SIV19,SNA20;
NA21        :NA310LH        SIV20,SNA13,SNA15,SNA21;
NA22        :NA310LH        SNA13,SNA14,SIV21,SNA22;
NA23        :NA310LH        SIV19,SIV20,SIV21,SNA23;
NA24        :NA410LH        SNA16,SNA17,SNA18,SNA19,SNA24;
NA25        :NA410LH        SNA20,SNA21,SNA22,SNA23,SNA25;
NA3         :NA310LH        INV3O,INV1O,INV6O,SNA3;
NA4         :NA310LH        INV6O,INV4O,INV2O,SNA4;
NA5         :NA310LH        INV9O,INV11O,INV8O,SNA5;
NA6         :NA310LH        INV7O,INV11O,INV10O,SNA6;
NA7         :NA310LH        INV9O,INV7O,INV12O,SNA7;
NA8         :NA310LH        INV12O,INV10O,INV8O,SNA8;
NA9         :NA310LH        INV15O,INV17O,INV14O,SNA9;
END S280LH;
```

D2939, AUGUST 1986

SystemCell™ 2-μm SOFTWARE MACRO CELL

- **Full-Carry Look-Ahead Across the Four Bits**
- **Systems Achieve Partial Look-Ahead Performance with the Economy of Ripple Carry**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The SN54ASC283 and SN74ASC283 are standard-cell software macros implementing 4-bit binary full adders. The 4-bit configuration provides the custom IC designer a fully designed, fast-carry adder to embed in ASICs in its most efficient form, and the 4-bit length simplifies construction of large adders. The 'ASC283 implements an adder identical with that performed by packaged 'LS283, and 'F283 adders.

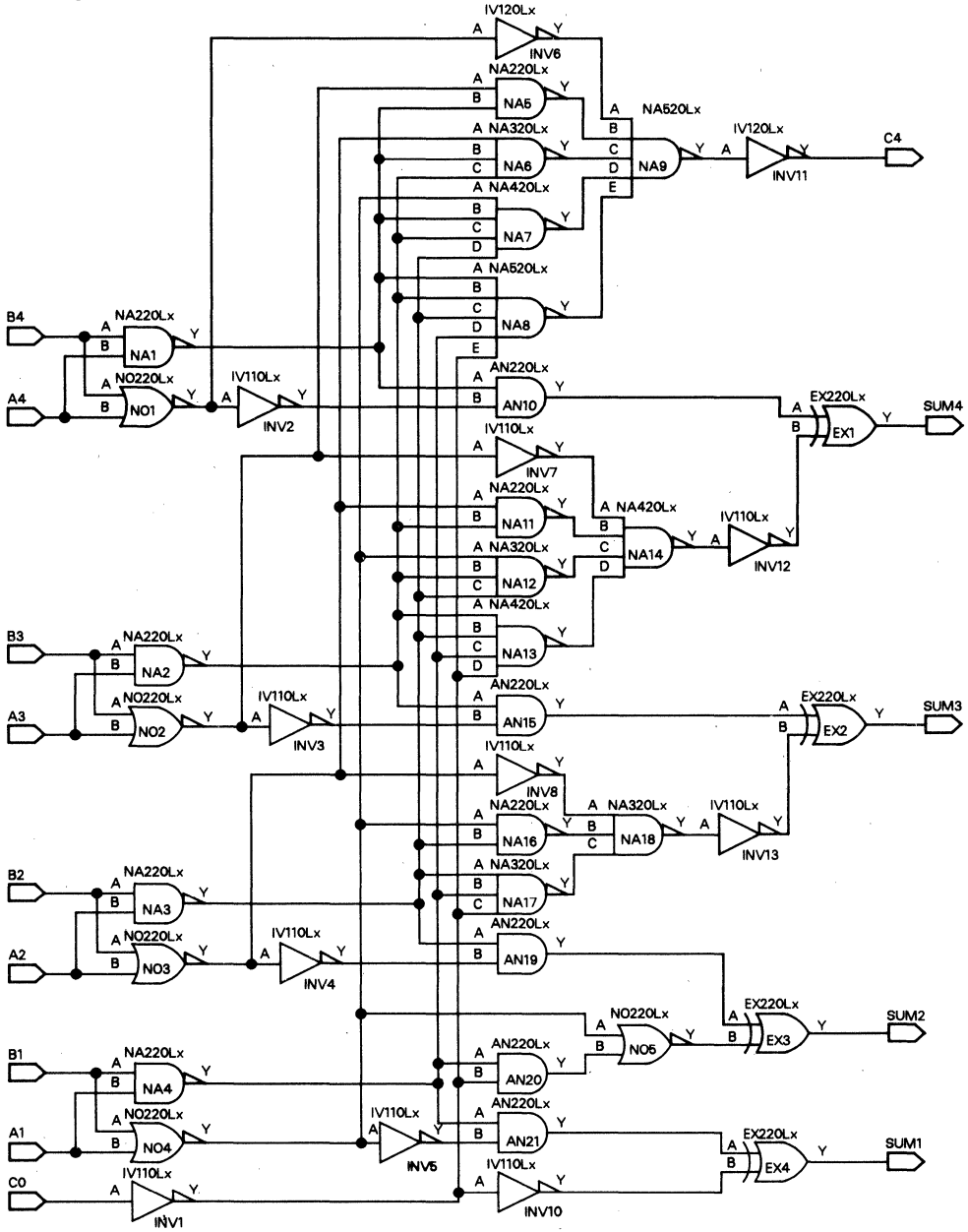
These full adders perform the addition of two 4-bit binary words. The sum outputs are provided for each bit and the resultant carry (C4) is generated in parallel from the four bits. These adders feature full carry look-ahead across all four bits, providing the system designer with built-in partial look-ahead. The adder logic, including the carry, is implemented in its true form. End around carry can be accomplished without the need for logic or level inversion. The 'ASC283 is implemented with the standard cell functions indicated. The HDL netlist label for this software macro is shown on the last line of the following table:

CELL NAME	RELATIVE CELL AREA TO NA210LH	NO. USED	TOTAL RELATIVE CELL AREA	TOTAL C_{pd}‡ (pF)	MAXIMUM I_{CC} (nA)	
					SN54ASC'	SN74ASC'
AN220LH	1.75	5	8.75	6	1140	68
EX220LH	2.25	4	9	6	1032	62
IV110LH	0.75	10	7.5	4.4	1050	63.2
IV120LH	1	2	2	1.6	262	15.7
NA220LH	1.5	7	10.5	7	1372	81.9
NA320LH	2	4	8	3.76	1020	61.2
NA420LH	2.5	3	7.5	2.88	936	56.1
NA520LH	3	2	6	2.04	720	43.8
NO220LH	1.5	5	7.5	2.6	925	55.5
TOTALS		42	66.75	36.28	8457	508
Label: S283LH A4,A3,A2,A1,B4,B3,B2,B1,C0,SUM4,SUM3,SUM2,SUM1,C4;						

‡ The equivalent power dissipation capacitance does not include interconnect capacitance.

The SN54ASC283 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC283 is characterized for operation from −40°C to 85°C.

logic diagram



FUNCTION TABLE

INPUT				OUTPUT					
				WHEN C0 = L			WHEN C0 = H		
				WHEN C2 = L			WHEN C2 = H		
A1 / A3	B1 / B3	A2 / A4	B2 / B4	SUM1 / SUM3	SUM2 / SUM4	C2 / C4	SUM1 / SUM3	SUM2 / SUM4	C2 / C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

NOTE: Input conditions at A1, B1, A2, B2, and C0 are used to determine outputs SUM1 and SUM2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs SUM3, SUM4, and C4.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS	SN54ASC283 TYP	SN54ASC283 MAX	SN74ASC283 TYP	SN74ASC283 MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current		V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		8457		508	nA
C_i	Input capacitance	An,Bn	V_{CC} = 5 V, T_A = 25°C	0.5		0.5		pF
		C0		0.12		0.12		
C_{pd}	Equivalent power dissipation capacitance†		V_{CC} = 5 V, T_A = 25°C, t_r = t_f = 3 ns,	36.28		36.28		pF

† The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted) (see Note 1)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC283			SN74ASC283			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{pd}	C0	SUMn	C_L = 0		8.5	16.5		8.5	15	ns
t_{pd}	An, Bn	SUMn			7.5	15.5		7.5	14.3	ns
t_{pd}	C0	C4			6	12.6		6	11.7	ns
t_{pd}	An, Bn	C4			6	12.8		6	11.6	ns
Δt_{pd}	Any	Any		0.3	0.6	1.9	0.3	0.6	1.7	ns/pF

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f = 3$ ns (10% and 90%).
t_{pd} ≡ propagation delay time, low-to-high-level or high-to-low-level output
Δt_{pd} ≡ change in t_{pd} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: These switching characteristics are simulations of the software macro cell using interconnect capacitance values for an array design having 2,000 gates. Post-layout simulation uses actual interconnect capacitance values.

DESIGN CONSIDERATIONS

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

The HDL for this software macro is included as a part of the library supplied for supported engineering workstations so that a single label can be developed to apply the macro as needed. The following printout of the HDL block definition is furnished for reference.

HDL FILE

```
BLOCK S283LH;
A4          @INPUT;
A3          @INPUT;
A2          @INPUT;
A1          @INPUT;
B4          @INPUT;
B3          @INPUT;
B2          @INPUT;
B1          @INPUT;
C0          @INPUT;
SUM4        @OUTPUT;
SUM3        @OUTPUT;
SUM2        @OUTPUT;
SUM1        @OUTPUT;
C4          @OUTPUT;
```

HDL FILE (Continued)

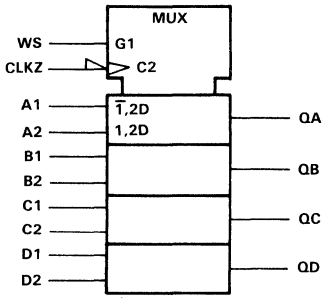
```
STRUCTURE
EX1          :EX220LH      AN10O,INV12O,SUM4;
EX2          :EX220LH      AN15O,INV13O,SUM3;
EX3          :EX220LH      AN19O,NO5O,SUM2;
EX4          :EX220LH      AN21O,INV10O,SUM1;
INV1         :IV110LH      CO,INV1O;
INV10        :IV110LH      INV1O,INV10O;
INV11        :IV120LH      NA9O,C4;
INV12        :IV110LH      NA14O,INV12O;
INV13        :IV110LH      NA18O,INV13O;
INV2         :IV110LH      NO1O,INV2O;
INV3         :IV110LH      NO2O,INV3O;
INV4         :IV110LH      NO3O,INV4O;
INV5         :IV110LH      NO4O,INV5O;
INV6         :IV120LH      NO1O,INV6O;
INV7         :IV110LH      NO2O,INV7O;
INV8         :IV110LH      NO3O,INV8O;
NA1          :NA220LH      B4,A4,NA1O;
AN10         :AN220LH      NA1O,INV2O,AN10O;
NA11         :NA220LH      NO3O,NA2O,NA11O;
NA12         :NA320LH      NO4O,NA2O,NA3O,NA12O;
NA13         :NA420LH      NA2O,NA3O,NA4O,INV1O,NA13O;
NA14         :NA420LH      INV7O,NA11O,NA12O,NA13O,NA14O;
AN15         :AN220LH      NA2O,INV3O,AN15O;
NA16         :NA220LH      NO4O,NA3O,NA16O;
NA17         :NA320LH      NA3O,NA4O,INV1O,NA17O;
NA18         :NA320LH      INV8O,NA16O,NA17O,NA18O;
AN19         :AN220LH      NA3O,INV4O,AN19O;
NA2          :NA220LH      B3,A3,NA2O;
NA20         :AN220LH      NA4O,INV1O,NA20O;
AN21         :AN220LH      NA4O,INV5O,AN21O;
NA3          :NA220LH      B2,A2,NA3O;
NA4          :NA220LH      B1,A1,NA4O;
NA5          :NA220LH      NO2O,NA1O,NA5O;
NA6          :NA320LH      NO3O,NA1O,NA2O,NA6O;
NA7          :NA420LH      NO4O,NA1O,NA2O,NA3O,NA7O;
NA8          :NA520LH      NA1O,NA2O,NA3O,NA4O,INV1O,NA8O;
NA9          :NA520LH      INV6O,NA5O,NA6O,NA7O,NA8O,NA9O;
NO1          :NO220LH      B4,A4,NO1O;
NO2          :NO220LH      B3,A3,NO2O;
NO3          :NO220LH      B2,A2,NO3O;
NO4          :NO220LH      B1,A1,NO4O;
NO5          :NO220LH      NO4O,AN20O,NO5O;
END S283LH;
```

D2939, AUGUST 1986

SystemCell™ 2-μm SOFTWARE MACRO CELL

- **Selects One of Two 4-Bit Data Sources and Stores Data Synchronously with System Clock**
- **Storage Register Loads New Data on Negative-Going Transition**
- **Implements Hexadecimal/BCD Shifter**
- **Parallel Multiplexers for Wider Words**

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The SN54ASC298 and SN74ASC298 are standard-cell software macros implementing four 2-line to 1-line multiplexers with storage. The 'ASC298 implements a function table identical with that performed by packaged 'HC298, 'LS298, and 'F298 multiplexers.

When the Word-Select (WS) input is low, word one (A1, B1,C1, D1) is applied to the flip-flops. A high WS input causes word two (A2, B2, C2, D2) to be selected. The selected word is clocked to the output terminals on the negative-going edge of the clock pulse. The 'ASC298 is implemented with standard cell functions indicated. The HDL netlist label for this software macro is shown on the last line of the following table:

CELL NAME	RELATIVE CELL AREA TO NA210LH	NO. USED	TOTAL RELATIVE CELL AREA	TOTAL C_{pd}‡ (pF)	MAXIMUM I_{CC} (nA)	
					SN54ASC'	SN74ASC'
IV120LH	1	3	3	2.4	393	23.55
NA210LH	1	12	12	6.12	1572	94.2
R2405LH	23.25	1	23.25	10.2	2647	159
TO010LH	1.5	1	1.5	–	177	10.6
TOTALS		17	39.75	18.72	4789	288
Label: S298LH A1,A2,B1,B2,C1,C2,D1,D2,CLKZ,WS,QA,QB,QC,QD;						

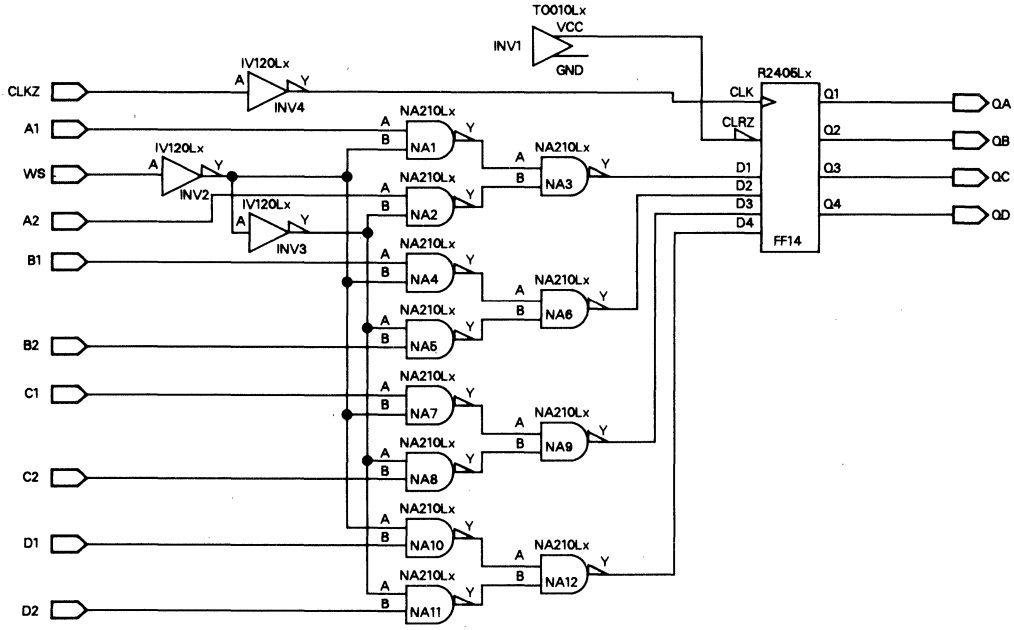
‡The equivalent power dissipation capacitance does not include interconnect capacitance.

The SN54ASC298 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC298 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

INPUTS		OUTPUTS			
WS	CLKZ	QA	QB	QC	QD
L	↓	a1	b1	c1	d1
H	↓	a2	b2	c2	d2
X	H	QA_0	QB_0	QC_0	QD_0

logic diagram



TEXAS INSTRUMENTS
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absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

electrical characteristics

PARAMETER		TEST CONDITIONS	SN54ASC298		SN74ASC298		UNIT
			TYP	MAX	TYP	MAX	
V_T Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC} Supply current		V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		4789		288	nA
C_i Input capacitance	CLKZ	V_{CC} = 5 V, T_A = 25°C	0.24		0.24		pF
	WS		0.24		0.24		
	All others		0.12		0.12		
C_{pd} Equivalent power dissipation capacitance†		V_{CC} = 5 V, T_A = 25°C, t_r = t_f = 3 ns,	18.72		18.72		pF

† The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 1)

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC298			SN74ASC298			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
t_{pd}	CLKZ	Qn	C_L = 0		6	12		6	11	ns
Δt_{pd}	Any	Qn		0.3	0.8	2.3	0.3	0.8	2.1	ns/pF

‡ Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{pd} ≡ propagation delay time, low-to-high or high-to-low-level output
Δt_{pd} ≡ change in t_{pd} with load capacitance
§ Typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: These switching characteristics are simulations of the software macro cell using interconnect capacitance values for an array design having 2,000 gates. Post-layout simulation uses actual interconnect capacitance values.

DESIGN CONSIDERATIONS

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

The HDL for this software macro is included as a part of the library supplied for supported engineering workstations so that a single label can be developed to apply the macro as needed. The following printout of the HDL block definition is furnished for reference.

HDL FILE

```
BLOCK S298LH;
A1          @INPUT;
A2          @INPUT;
B1          @INPUT;
B2          @INPUT;
C1          @INPUT;
C2          @INPUT;
D1          @INPUT;
D2          @INPUT;
CLKZ        @INPUT;
WS          @INPUT
QA          @OUTPUT;
QB          @OUTPUT;
QC          @OUTPUT;
QD          @OUTPUT;

STRUCTURE
FF14        :R2405LH        INV1O,NA3O,INV4O,NA6O,NA9O,NA12O,QA,QB,QC,QD;
INV1        :TO010LH        DUM,INV1O;
INV2        :IV120LH        WS,INV2O;
INV3        :IV120LH        INV2O,INV3O;
INV4        :IV120LH        CLKZ,INV4O;
NA1         :NA210LH        A1,INV2O,NA1O;
NA10        :NA210LH        INV2O,D1,NA10O;
NA11        :NA210LH        INV3O,D2,NA11O;
NA12        :NA210LH        NA10O,NA11O,NA12O;
NA2         :NA210LH        A2,INV3O,NA2O;
NA3         :NA210LH        NA1O,NA2O,NA3O;
NA4         :NA210LH        B1,INV2O,NA4O;
NA5         :NA210LH        INV3O,B2,NA5O;
NA6         :NA210LH        NA4O,NA5O,NA6O;
NA7         :NA210LH        C1,INV2O,NA7O;
NA8         :NA210LH        INV3O,C2,NA8O;
NA9         :NA210LH        NA7O,NA8O,NA9O;
END S298LH;
```

Dedicated 2-line to 1-line multiplexers ('ASC2340) are also available in the standard cell library for implementing data-path multiplexers. These hard-wired multiplexers in conjunction with hard-wired registers should be considered if the multiplexer is in a critical path, as their performance is predetermined as specified in their switching characteristics.

interfacing the macro

Inputs and outputs of the predesigned macro are compatible for interfacing directly with cells and macros available in the TI standard cell library.

The inputs can be driven by either inverting or noninverting input cells. The outputs can be interfaced to drive off-chip loads with any of the noninverting output buffers or interfaced to external bidirectional buses through a 3-state input/output TTL/CMOS buffer.

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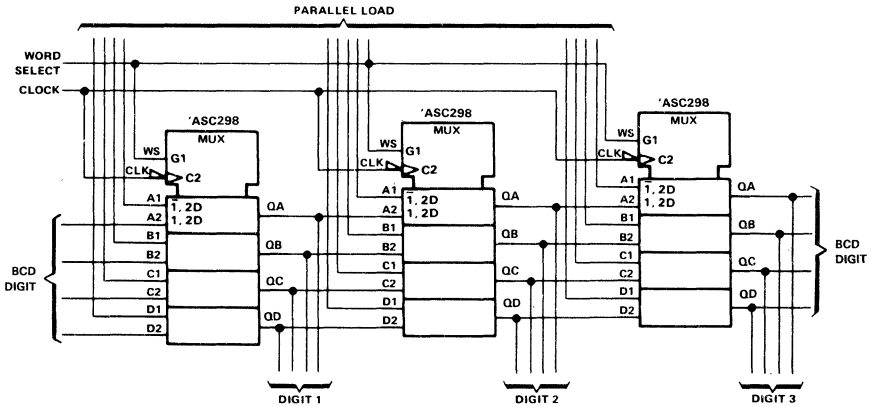
TYPICAL APPLICATION DATA

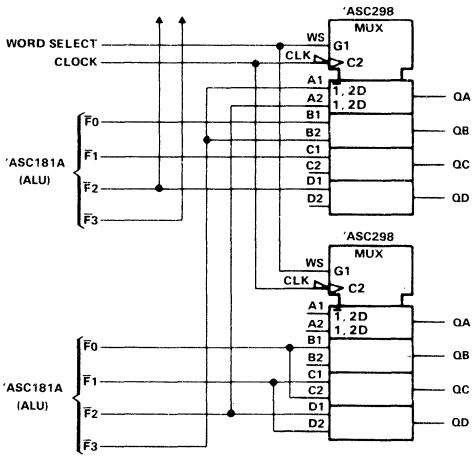
This versatile multiplexer/register can be connected to operate as a shift register that can shift N-places in a single clock pulse.

The following figure illustrates a BCD shift register that will shift an entire 4-bit BCD digit in one clock pulse.



When the word-select input is high and the registers are clocked, the contents of register 1 is transferred (shifted) to register 2, etc. In effect, the BCD digits are shifted one position. In addition, this application retains a parallel-load capability which means that new BCD data can be entered in the entire register with one clock pulse. This arrangement can be modified to perform the shifting of binary data for any number of bit locations.

Another function that can be implemented with the 'ASC298 is a rgister that can be designed specifically for supporting multiplier or division operations. The example below is a one-place/two-place shift register.



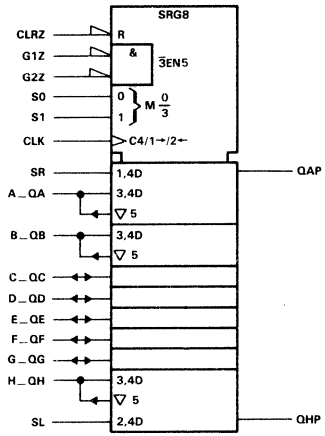
When word select is low and the register is clocked, the outputs of the arithmetic/logic units (ALUs) are shifted one place. When word select is high and the registers are clocked, the data is shifted two places.

D2939, AUGUST 1986

SystemCell™ 2-μm SOFTWARE MACRO CELLS

- Ported 3-State Inputs/Outputs Simplify Implementation of:
  - Single/Multiple Push/Pop Stack
  - Multiple/Supplementary Accumulator
  - Bus Storage/Shift Register
- Four Operating Modes:
  - Synchronous Parallel Load
  - Right Shift
  - Left Shift
  - Do Nothing
- Positive-Edge-Triggered Clocking
- Embedded Clock Drivers Provide Clock Buffering

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The SN54ASC299 and SN74ASC299 are standard-cell software macros implementing 8-bit parallel-in/parallel-out bidirectional, universal shift/storage registers. The 8-bit configuration provides the custom IC designer a register to embed in ASICs in its most efficient form. The 8-bit length simplifies construction of large registers. The 'ASC299 implements an 8-bit shift sequence identical with that performed by packaged 'HC299, 'LS299, and 'F299 4-bit shift registers.

These bidirectional shift registers are designed to incorporate virtually all of the features a system designer may want in a shift register. The circuit features parallel inputs, parallel outputs, right-shift and left-shift inputs, operating-mode-control inputs, and a direct overriding clear line. The 'ASC299 is implemented with the standard cell functions indicated. The HDL netlist label for this software macro is shown on the last line of the following table:

CELL NAME	RELATIVE CELL AREA TO NA210LH	NO. USED	TOTAL RELATIVE CELL AREA	TOTAL C_{pd}‡ (pF)	MAXIMUM I_{CC} (nA)	
					SN54ASC'	SN74ASC'
AN210LH	1.5	1	15	0.9	194	11.6
IV110LH	0.75	1	0.75	0.44	210	12.64
IV140LH	1.5	5	6	8.05	760	45.6
IV222LH	1.5	8	16	7.84	1944	116.8
NA310LH	1.25	32	40	16	5216	312.96
NA410LH	1.5	8	12	4	1496	89.6
NO310LH	1.25	1	1.25	.32	312	18.66
R2406LH	26.25	2	52.5	23.4	5862	352
TOTALS		58	181.5	60.02	15915	956
Label: S299LH S0,S1,G1Z,G2Z,SL,SR,CLK,CLRZ,QAP,QHP,A_QA,B_QB,C_QC, D_QD,E_QE,F_QF,G_QG,H_QH;						

‡The equivalent power dissipation capacitance does not include interconnect capacitance.

The 'ASC299 register has four distinct modes of operation, namely:

Parallel (broadside load)
Shift right (in the direction QA toward QH)
Shift left (in the direction QH toward QA)
Inhibit clocking (do nothing).

Synchronous parallel loading is accomplished by taking either output control input, G1Z or G2Z, high and applying the eight bits of data while both mode control inputs, S0 and S1, are high. The data are loaded into the associated flip-flops on the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial input. When both mode control inputs are low, a free-running clock will reload the present state of each flip-flop on each clock transition to implement the do-nothing mode.

The SN54ASC299 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC299 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

INPUTS								I/O PORTS								OUTPUTS	
CLRZ	MODE		OUTPUT CONTROLS		CLK	SERIAL											
	S1	S0	G1Z†	G2Z†		SL	SR	A_QA	B_QB	C_QC	D_QD	E_QE	F_QF	G_QG	H_QH	QAP	QHP
L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
L	H	H	X	X	X	X	X	X	X	X	X	X	X	X	X	L	L
H	L	L	L	L	X	X	X	QA_0	QB_0	QC_0	QD_0	QE_0	QF_0	QG_0	QH_0	QA_0	QH_0
H	X	X	L	L	L	X	X	QA_0	QB_0	QC_0	QD_0	QE_0	QF_0	QG_0	QH_0	QA_0	QH_0
H	L	H	L	L	↑	X	H	H	QA_n	QB_n	QC_n	QD_n	QE_n	QF_n	QG_n	H	QG_n
H	L	H	L	L	↑	X	L	L	QA_n	QB_n	QC_n	QD_n	QE_n	QF_n	QG_n	L	QG_n
H	H	L	L	L	↑	H	X	QB_n	QC_n	QD_n	QE_n	QF_n	QG_n	QH_n	H	QB_n	H
H	H	L	L	L	↑	L	X	QB_n	QC_n	QD_n	QE_n	QF_n	QG_n	QH_n	L	QB_n	L
H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

† When one or both output controls are high, the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected. a . . . h = the level of the steady-state input at inputs A through H, respectively. These data are loaded into the flip-flops while the flip-flop outputs are isolated from the input/output terminals.

See explanation of Function Tables in Section 1.

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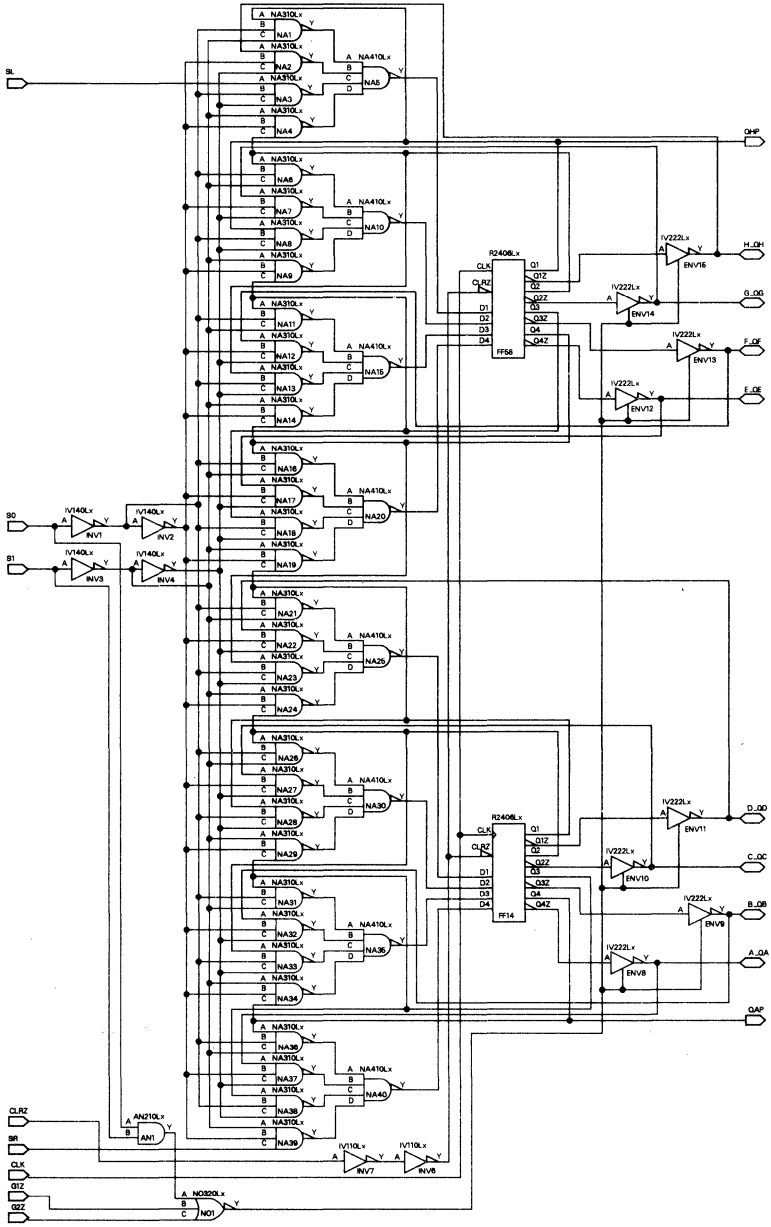
logic diagram



absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

electrical characteristics

PARAMETER			TEST CONDITIONS		SN54ASC299		SN74ASC299		UNIT
					TYP	MAX	TYP	MAX	
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX	V_I = V_{CC} or 0,		15915		956	nA
C_i	Input capacitance	CLK	V_{CC} = 5 V,	T_A = 25°C	0.48		0.48		pF
		G1Z, G2Z			0.24		0.24		
		S0, S1			0.62		0.62		
		A_QA...H_QH			0.45		0.45		
		All others			0.12		0.12		
C_o	Output capacitance		V_{CC} = 5 V,	T_A = 25°C	0.33		0.33		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	60.02		60.02		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 1)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC299			SN74ASC299			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{pd}	CLK	Qn	C_L = 0		7.1	15.2		7.1	13.8	ns
t_{PHL}	CLRZ	Qn			8.4	17		8.4	15.3	ns
t_{pd}	CLK	QAP, QHP			5	10.3		5	9.4	ns
t_{PHL}	CLRZ	QAP, QHP			6	11.4		6	10.4	ns
t_{en}	GnZ	Qn			6.1	13.5		6.1	12.2	ns
Δt_{pd}	Any	Any		0.2	0.9	2.3	0.3	0.9	2.1	ns/pF
Δt_{en}	GnZ	Qn		0.4	0.8	2.3	0.5	0.8	2.1	ns/pF

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{pd} ≡ propagation delay time, low-to-high or high-to-low-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{en} ≡ enable time, high-impedance state to low- or high-logic-level output
Δt_{pd} ≡ change in t_{pd} with load capacitance
Δt_{en} ≡ change in t_{en} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: These switching characteristics are simulations of the software macro cell using interconnect capacitance values for an array design having 2,000 gates. Post-layout simulation uses actual interconnect capacitance values.

DESIGN CONSIDERATIONS

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

The HDL for this software macro is included as a part of the library supplied for supported engineering workstations so that a single label can be developed to apply the macro as needed. The following printout of the HDL block definition is furnished for a reference.

TEXAS INSTRUMENTS
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HDL FILE

```
BLOCK S299LH;
S0          @INPUT;
S1          @INPUT;
G1Z         @INPUT;
G2Z         @INPUT;
SL          @INPUT;
SR          @INPUT;
CLK         @INPUT;
CLRZ        @INPUT;
QAP         @OUTPUT;
QHP         @OUTPUT;
A_QA        @INOUT;
B_QB        @INOUT;
C_QC        @INOUT;
D_QD        @INOUT;
E_QE        @INOUT;
F_QF        @INOUT;
G_QG        @INOUT
H_QH        @INOUT;

STRUCTURE
AN1         :AN210LH        S0,S1,AN1O;
INV1        :IV140LH        S0,INV1O;
INV10       :IV222LH        CN,NO1O,C_QC;
INV11       :IV222LH        DN,NO1O,D_QD;
INV12       :IV222LH        EN,NO1O,E_QE;
INV13       :IV222LH        FN,NO1O,F_QF;
INV14       :IV222LH        GN,NO1O,G_QG;
INV15       :IV222LH        HN,NO1O,H_QH;
INV2        :IV140LH        INV1O,INV2O;
INV3        :IV140LH        S1,INV3O;
INV4        :IV140LH        INV3O,INV4O;
INV6        :IV110LH        INV7O,INV6O;
INV7        :IV110LH        CLRZ,INV7O;
INV8        :IV222LH        AN,NO1O,A_QA;
INV9        :IV222LH        BN,NO1O,B_QB;
NA1         :NA310LH        QHP,INV1O,INV3O,NA1O;
NA10        :NA410LH        NA6O,NA7O,NA8O,NA9O,NA10O;
NA11        :NA310LH        FP,INV1O,INV3O,NA11O;
NA12        :NA310LH        F_QF,INV2O,INV4O,NA12O;
NA13        :NA310LH        GP,INV1O,INV4O,NA13O;
NA14        :NA310LH        INV3O,INV2O,EP,NA14O;
NA15        :NA410LH        NA11O,NA12O,NA13O,NA14O,NA15O;
NA16        :NA310LH        EP,INV1O,INV3O,NA16O;
NA17        :NA310LH        E_QE,INV2O,INV4O,NA17O;
NA18        :NA310LH        FP,INV1O,INV4O,NA18O;
NA19        :NA310LH        INV3O,INV2O,DP,NA19O;
NA2         :NA310LH        H_QH,INV2O,INV4O,NA2O;
NA20        :NA410LH        NA16O,NA17O,NA18O,NA19O,NA20O;
NA21        :NA310LH        DP,INV1O,INV3O,NA21O;
NA22        :NA310LH        D_QD,INV2O,INV4O,NA22O;
```

HDL FILE (Continued)

```
STRUCTURE (Continued)
NA23        :NA310LH        EP,INV1O,INV4O,NA23O;
NA24        :NA310LH        INV3O,INV2O,CP,NA24O;
NA25        :NA410LH        NA21O,NA22O,NA23O,NA24O,NA25O;
NA26        :NA310LH        CP,INV1O,INV3O,NA26O;
NA27        :NA310LH        C_QC,INV2O,INV4O,NA27O;
NA28        :NA310LH        DP,INV1O,INV4O,NA28O;
NA29        :NA310LH        INV3O,INV2O,BP,NA29O;
NA3         :NA310LH        SL,INV1O,INV4O,NA3O;
NA30        :NA410LH        NA26O,NA27O,NA28O,NA29O,NA30O;
NA31        :NA310LH        BP,INV1O,INV3O,NA31O;
NA32        :NA310LH        B_QB,INV2O,INV4O,NA32O;
NA33        :NA310LH        CP,INV1O,INV4O,NA33O;
NA34        :NA310LH        INV3O,INV2O,QAP,NA34O;
NA35        :NA410LH        NA31O,NA32O,NA33O,NA34O,NA35O;
NA36        :NA310LH        QAP,INV1O,INV3O,NA36O;
NA37        :NA310LH        A_QA,INV2O,INV4O,NA37O;
NA38        :NA310LH        BP,INV1O,INV4O,NA38O;
NA39        :NA310LH        INV3O,INV2O,SR,NA39O;
NA4         :NA310LH        INV3O,INV2O,GP,NA4O;
NA40        :NA410LH        NA36O,NA37O,NA38O,NA39O,NA40O;
NA5         :NA410LH        NA1O,NA2O,NA3O,NA4O,NA5O;
NA6         :NA310LH        GP,INV1O,INV3O,NA6O;
NA7         :NA310LH        G_QG,INV2O,INV4O,NA7O;
NA8         :NA310LH        QHP,INV1O,INV4O,NA8O;
NA9         :NA310LH        INV3O,INV2O,FP,NA9O;
NO1         :NO310LH        AN1O,G1Z,G2Z,NO1O;
FF14        :R2406LH        INV6O,NA25O,NA30O,NA35O,NA40O,CLK,DP,DN,CP,CN,BP,
                            BN,QAP,AN;
FF58        :R2406LH        INV6O,NA5O,NA10O,NA15O,NA20O,CLK,QHP,HN,GP,GN,FP,
                            FN,EP,EN;

END S299LH;
```

shift definition

These registers are bidirectional with respect to shift operations, and the relationship for shifting left or right is defined by the S0 and S1 inputs. Unidirectional registers are available in software macros or can be constructed using the 'ASC2405 through 'ASC2407 8-bit predesigned registers. Additional single bits can be achieved with flip-flop cells offered in TI's standard cell family.

designing for testability

Designers employing storage or bistable elements, especially long registers (ripple or synchronous), should consider testability of the design in its final form. The need to preset or clear and read intermediate stages of these elements should be assessed throughout the development of custom logic circuits with these considerations extended to the end equipment application with respect to maintainability. Simple actions on the part of the ASIC designer can result in considerable cost savings, allowing the expense of IC testing, system testing, and system maintenance to be reduced significantly.

power-up clear/preset

Standard cell storage elements containing the capability to be asynchronously preset or cleared may be connected to the SN54ASC2320 or SN74ASC2320 power-up clear cell to achieve system initialization. Control of the clear or preset inputs from another system signal in conjunction with the power-up clear can be achieved with an AND gate.

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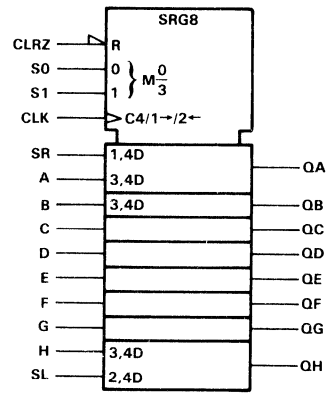
D2939, AUGUST 1986

SystemCell™ 2-μm SOFTWARE MACRO CELL

- **Parallel Inputs and Outputs**
- **Four Operating Modes:**
  - **Synchronous Parallel Load**
  - **Right Shift**
  - **Left Shift**
  - **Do Nothing**
- **Positive Edge-Triggered Clocking**
- **Embedded Clock Drivers Provide Clock Buffering**

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The SN54ASC299X and SN74ASC299X are standard-cell software macros implementing 8-bit parallel-in/parallel-out bidirectional, universal shift registers. The 8-bit configuration provides the custom IC designer a register to embed in ASICs in their most efficient form. The 8-bit length simplifies construction of large registers. The 'ASC299X implements an 8-bit shift sequence identical with that performed by packaged 'HC194A, 'LS194A, and 'F194 4-bit shift registers.

These bidirectional shift registers are designed to incorporate virtually all of the features a system designer may want in a shift register. The circuit features parallel inputs, parallel outputs, right-shift and left-shift inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

Parallel (broadside load)
Shift right (in the direction QA toward QH)
Shift left (in the direction QH toward QA)
Inhibit clocking (do nothing)

The 'ASC299X is implemented with the standard cell functions indicated. The HDL netlist label for this software macro is shown on the last line of the following table:

CELL NAME	RELATIVE CELL AREA TO NA210LH	NO. USED	TOTAL RELATIVE CELL AREA	TOTAL C_{pd}‡ (pF)	MAXIMUM I_{CC} (nA)	
					SN54ASC'	SN74ASC'
IV110LH	0.75	1	0.75	0.44	105	6.32
IV140LH	1.5	5	7.5	8.05	950	57
NA310LH	1.25	32	40	16	5216	312.96
NA410LH	1.5	8	12	4	1496	89.6
R2405LH	23.25	2	46.5	20.4	5294	318
TOTALS		48	106.75	48.89	13061	784
Label: S299XLH A,B,C,D,E,F,G,H,S0,S1,SL,SR,CLK,CLRZ,QA,QB,QC,QD,QE,QF,QG,QH;						

‡The equivalent power dissipation capacitance does not include interconnect capacitance.

description (continued)

Synchronous parallel loading is accomplished by applying the eight bits of data and taking both mode control inputs, S0 and S1, high. The data are loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial input. When both mode control inputs are low, a free-running clock will reload the present state of each flip-flop on each clock transition to implement the do-nothing mode.

The SN54ASC299X is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC299X is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

INPUTS														OUTPUTS							
	MODE			SERIAL		PARALLEL															
CLRZ	S1	S0	CLK	SL	SR	A	B	C	D	E	F	G	H	QA	QB	QC	QD	QE	QF	QG	QH
L	X	X	X	X	X	X	X	X	X	X	X	X	X	L	L	L	L	L	L	L	L
H	X	X	L	X	X	X	X	X	X	X	X	X	X	QA_0	QB_0	QC_0	QD_0	QE_0	QF_0	QG_0	QH_0
H	H	H	↑	X	X	a	b	c	d	e	f	g	h	a	b	c	d	e	f	g	h
H	L	H	↑	X	H	X	X	X	X	X	X	X	X	H	QAn	QBn	QCn	QDn	QEn	QFn	QGn
H	L	H	↑	X	L	X	X	X	X	X	X	X	X	L	QAn	QBn	QCn	QDn	QEn	QFn	QGn
H	H	L	↑	H	X	X	X	X	X	X	X	X	X	QBn	QCn	QDn	QEn	QFn	QGn	QHn	H
H	H	L	↑	L	X	X	X	X	X	X	X	X	X	QBn	QCn	QDn	QEn	QFn	QGn	QHn	L
H	L	L	X	X	X	X	X	X	X	X	X	X	X	QA_0	QB_0	QC_0	QD_0	QE_0	QF_0	QG_0	QH_0

typical clear, load, right-shift, left-shift, inhibit, and clear sequences

The 4-bit sequences illustrated on the 'ASC194 data sheet are applicable for similar 8-bit functions performed by the 'ASC299X.

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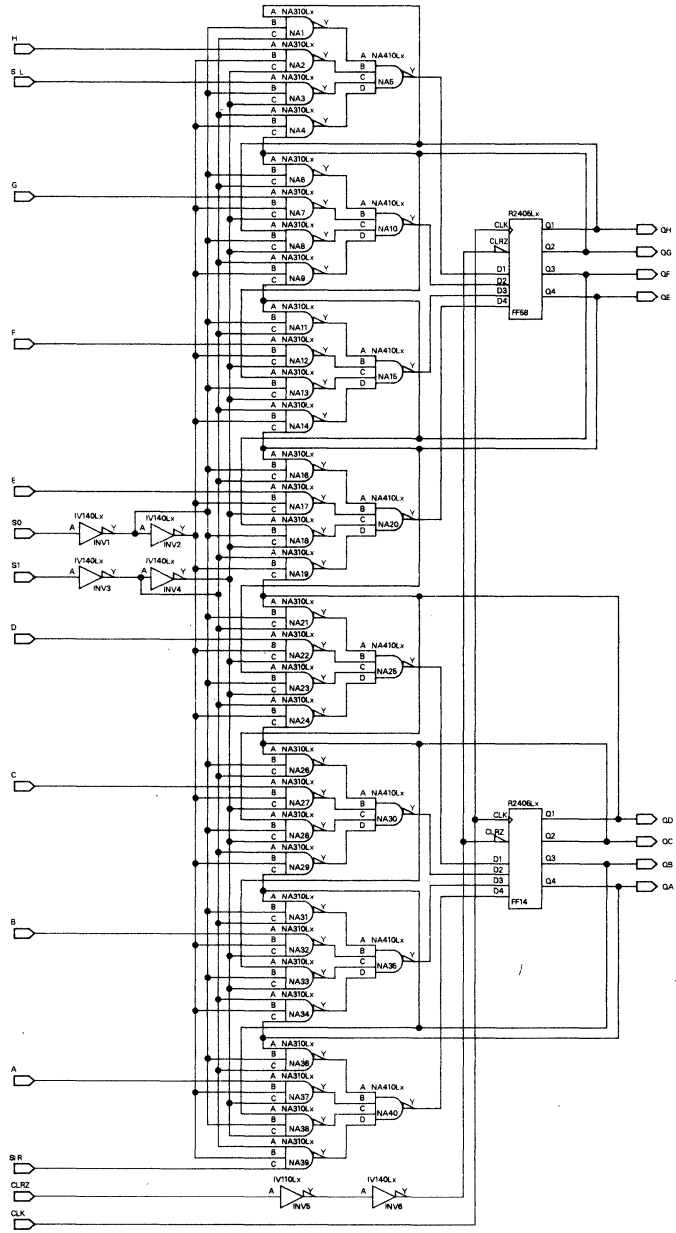
logic diagram



absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

electrical characteristics

PARAMETER		TEST CONDITIONS	SN54ASC299X		SN74ASC299X		UNIT
			TYP	MAX	TYP	MAX	
V_T Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC} Supply current		V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		13061		784	nA
C_i Input capacitance	CLK	V_{CC} = 5 V, T_A = 25°C	0.48		0.48		pF
	S0,S1		0.49		0.49		
	All others		0.12		0.12		
C_{pd} Equivalent power dissipation capacitance†		V_{CC} = 5 V, T_A = 25°C, t_r = t_f = 3 ns,	48.89		48.89		pF

† The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted) (see Note 1)

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC299X			SN74ASC299X			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
t_{pd}	CLK	Qn	C_L = 0		5	10.5		5	9.4	ns
t_{PHL}	CLRZ	Qn			5	9.3		6.1	8.6	ns
Δt_{pd}	CLK	Qn		0.3	0.9	2.3	0.3	0.9	2.1	ns/pF
Δt_{PHL}	CLRZ	Qn		0.3	0.7	1.9	0.3	0.7	1.6	ns/pF

‡ Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{pd} ≡ propagation delay time, low-to-high-level or high-to-low-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{pd} ≡ change in t_{pd} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
§ Typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: These switching characteristics are simulations of the software macro cell using interconnect capacitance values for an array design having 2,000 gates. Post-layout simulation uses actual interconnect capacitance values.

DESIGN CONSIDERATIONS

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

The HDL for this software macro is included as a part of the library supplied for supported engineering workstations so that a single label can be developed to apply the macro as needed. The following printout of the HDL block definition is furnished for reference.

TEXAS INSTRUMENTS
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HDL FILE

```
BLOCK S299XLH;
A           @INPUT;
B           @INPUT;
C           @INPUT;
D           @INPUT;
E           @INPUT;
F           @INPUT;
G           @INPUT;
H           @INPUT;
S0          @INPUT;
S1          @INPUT;
SL          @INPUT;
SR          @INPUT;
CLK         @INPUT;
CLRZ        @INPUT;
QA          @OUTPUT;
QB          @OUTPUT;
QC          @OUTPUT;
QD          @OUTPUT;
QE          @OUTPUT;
QF          @OUTPUT;
QG          @OUTPUT;
QH          @OUTPUT;

STRUCTURE
INV1        :IV140LH        S0,INV1O;
INV2        :IV140LH        INV1O,INV2O;
INV3        :IV140LH        S1,INV3O;
INV4        :IV140LH        INV3O,INV4O;
INV5        :IV110LH        CLRZ,INV5O;
INV6        :IV140LH        INV5O,INV6O;
NA1         :NA310LH        QH,INV1O,INV3O,NA1O;
NA10        :NA410LH        NA6O,NA7O,NA8O,NA9O,NA10O;
NA11        :NA310LH        QF,INV1O,INV3O,NA11O;
NA12        :NA310LH        F,INV2O,INV4O,NA12O;
NA13        :NA310LH        QG,INV1O,INV4O,NA13O;
NA14        :NA310LH        INV3O,INV2O,QE,NA14O;
NA15        :NA410LH        NA11O,NA12O,NA13O,NA14O,NA15O;
NA16        :NA310LH        QE,INV1O,INV3O,NA16O;
NA17        :NA310Lh        E,INV2O,INV4O,NA17O;
NA18        :NA310LH        QF,INV1O,INV4O,NA18O;
NA19        :NA310LH        INV3O,INV2O,QD,NA19O;
NA2         :NA310LH        H,INV2O,INV4O,NA2O;
NA20        :NA410LH        NA16O,NA17O,NA18O,NA19O,NA20O;
NA21        :NA310LH        QD,INV1O,INV3O,NA21O;
NA22        :NA310LH        D,INV2O,INV4O,NA22O;
NA23        :NA310LH        QE,INV1O,INV4O,NA23O;
NA24        :NA310LH        INV3O,INV2O,QC,NA24O;
NA25        :NA410LH        NA21O,NA22O,NA23O,NA24O,NA25O;
NA26        :NA310LH        QC,INV1O,INV3O,NA26O;
NA27        :NA310LH        C,INV2O,INV4O,NA27O;
```

HDL FILE (continued)

```
STRUCTURE (continued)
NA28        :NA310LH        QD,INV1O,INV4O,NA28O;
NA29        :NA310LH        INV3O,INV2O,QB,NA29O;
NA3         :NA310LH        SL,INV1O,INV4O,NA3O;
NA30        :NA410LH        NA26O,NA27O,NA28O,NA29O,NA30O;
NA31        :NA310LH        QB,INV1O,INV3O,NA31O;
NA32        :NA310LH        B,INV2O,INV4O,NA32O;
NA33        :NA310LH        QC,INV1O,INV4O,NA33O;
NA34        :NA310LH        INV3O,INV2O,QA,NA34O;
NA35        :NA410LH        NA31O,NA32O,NA33O,NA34O,NA35O;
NA36        :NA310LH        QA,INV1O,INV3O,NA36O;
NA37        :NA310LH        A,INV2O,INV4O,NA37O;
NA38        :NA310LH        QB,INV1O,INV4O,NA38O;
NA39        :NA310LH        INV3O,INV2O,SR,NA39O;
NA4         :NA310LH        INV3O,INV2O,QG,NA4O;
NA40        :NA410LH        NA36O,NA37O,NA38O,NA39O,NA40O;
NA5         :NA410LH        NA1O,NA2O,NA3O,NA4O,NA5O;
NA6         :NA310LH        QG,INV1O,INV3O,NA6O;
NA7         :NA310LH        G,INV2O,INV4O,NA7O;
NA8         :NA310LH        QH,INV1O,INV4O,NA8O;
NA9         :NA310LH        INV3O,INV2O,QF,NA9O;
FF14        :R2405LH        INV6O,NA25O,NA30O,NA35O,NA40O,CLK,QD,QC,QB,QA;
FF58        :R2405LH        INV6O,NA5O,NA10O,NA15O,NA20O,CLK,QH,QG,QF,QE;
END S299XLH;
```

shift definition

These registers are bidirectional with respect to shift operations and the relationship for shifting left or right is defined by the S0 and S1 inputs. Unidirectional registers are available in software macros or can be constructed using the 'ASC2405 through 'ASC2407 8-bit predesigned registers. Additional single bits can be achieved with flip-flop cells offered in TI's standard cell family.

designing for testability

Designs employing storage or bistable elements, especially long registers (ripple or synchronous), should consider testability of the design in its final form. The need to preset or clear and read intermediate stages of these elements should be assessed throughout the development of custom logic circuits with these considerations extended to the end-equipment application with respect to maintainability. Simple actions on the part of the ASIC designer can result in considerable cost savings, allowing the expense of IC testing, system testing, and system maintenance to be reduced significantly.

power-up clear/preset

Standard cell storage elements containing the capability to be asychronously preset or cleared may be connected to the SN54ASC2320 or SN74ASC2320 power-up clear cell to achieve system initialization. Control of the clear or preset inputs from another system signal in conjunction with the power-up clear can be achieved with an AND gate.

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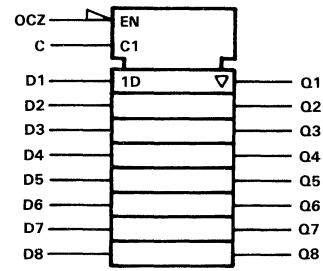
D2939, AUGUST 1986

SystemCell™ 2-μm SOFTWARE MACRO CELL

- **3-State Outputs Interface with Internal Data Buses Directly**
- **Buffered Output Enable Simplifies System Design**
- **Full Parallel Access for Loading**
- **Parallel Latches for 16-Bit, 32-Bit, 64-Bit Word Widths**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The SN54ASC373 and SN74ASC373 are standard-cell software macros implementing 8-bit D-type latch elements designed specifically for interfacing internal bus lines. The 8-bit length means that testability is simplified when constructing large latches. The 'ASC373 implements a function table identical with that performed by packaged 'HC373, 'LS373, and 'F373 latches.

The eight latches of the 'HC373 are transparent D-type latches. While the enable (C) is high, the Q outputs will follow the data (D) inputs. When the enable is taken low, the Q outputs will be latched at the levels that were set up at the D inputs. The output-control input OCZ can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. When the outputs are enabled with OCZ low, the logic level at each of the eight outputs is impressed on the data bus. The outputs are disabled by a high logic level at OCZ. The outputs then present a high impedance to the internal bus. The output control does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off. The 'ASC373 is implemented with standard cell functions indicated. The HDL netlist label for this software macro is shown on the last line of the following table:

CELL NAME	RELATIVE CELL AREA TO NA210LH	NO. USED	TOTAL RELATIVE CELL AREA	TOTAL C_{pd}‡ (pF)	MAXIMUM I_{CC} (nA)	
					SN54ASC'	SN74ASC'
IV110LH	0.75	8	6	3.52	840	50.56
IV140LH	1.5	3	4.5	4.83	570	34.2
IV212LH	1.5	8	12	4	1440	86.4
AO221LH	2.7	8	21.6	4.72	1792	107.2
TOTALS		27	44.1	17.07	4642	279
Label: S373LH D1,D2,D3,D4,D5,D6,D7,D8,C,OCZ,Q1,Q2,Q3,Q4,Q5,Q6,Q7,Q8;						

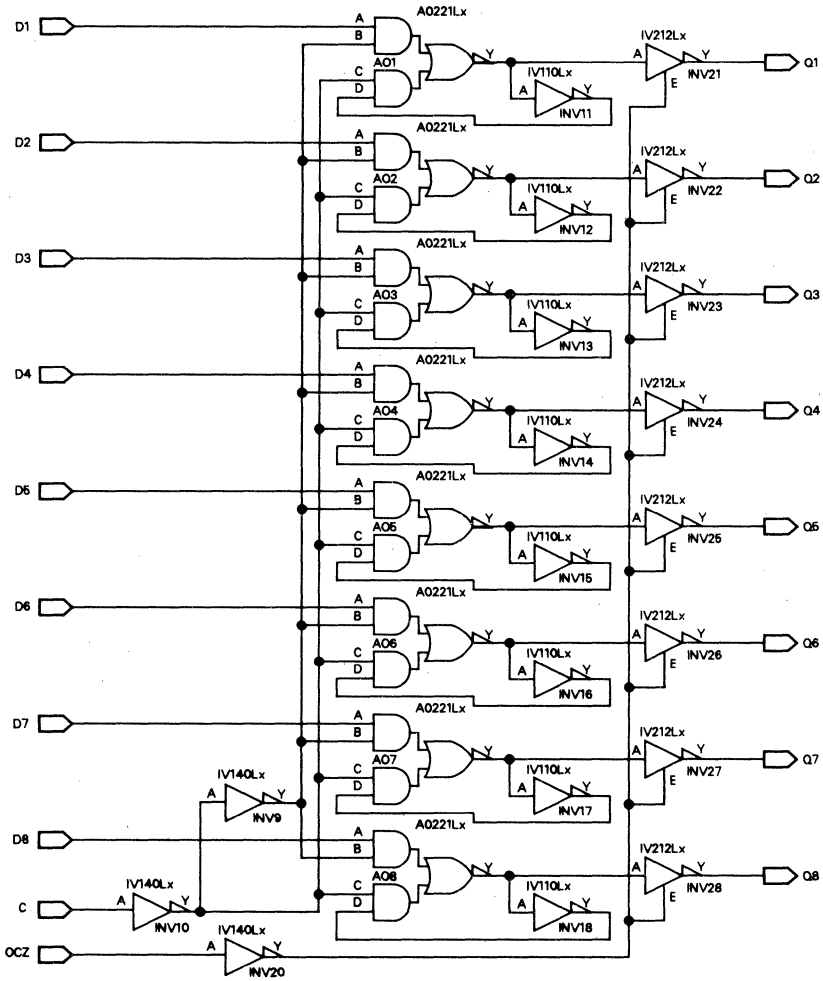
‡ The equivalent power dissipation capacitance does not include interconnect capacitance.

The SN54ASC373 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC373 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(EACH LATCH)

INPUTS			OUTPUT
OCZ	C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic diagram



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

electrical characteristics

PARAMETER		TEST CONDITIONS		SN54ASC373		SN74ASC373		UNIT
				TYP	MAX	TYP	MAX	
V_T Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC} Supply current		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX	V_I = V_{CC} or 0,		4642		279	nA
C_i Input capacitance	C	V_{CC} = 5 V,	T_A = 25°C	0.49		0.49		pF
	Dn			0.13		0.13		
	OCZ			0.49		0.49		
C_o Output capacitance		V_{CC} = 5 V,	T_A = 25°C	0.18		0.18		pF
C_{pd} Equivalent power dissipation capacitance†		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	17.07		17.07		pF

† The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Notes 1 and 2)

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC373			SN74ASC373			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
t_{pd}	D	Q	C_L = 0		3	7.5		3	6.7	ns
t_{en}	OCZ	Q			5	10.2		5	9.2	ns
Δt_{pd}	D	Q		0.6	1.7	4.6	0.6	1.7	4.2	ns/pF
Δt_{en}	Any	Q		0.7	1.7	4.8	0.7	1.7	4.4	ns/pF

‡ Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{pd} ≡ propagation delay time, low-to-high-level or high-to-low-level output
t_{en} ≡ enable time, high-impedance state to low- or high-logic-level output
Δt_{pd} ≡ change in t_{pd} with load capacitance
Δt_{en} ≡ change in t_{en} with load capacitance
§ Typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTES: 1. These switching characteristics are simulations of the software macro cell using interconnect capacitance values for an array design having 2,000 gates. Post-layout simulation uses actual interconnect capacitance values.
2. Enable and delta-enable times are measured using the conditions specified for the 'ASC2407.

DESIGN CONSIDERATIONS

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

The HDL for this software macro is included as a part of the library supplied for supported engineering workstations so that a single label can be developed to apply the macro as needed. The following printout of the HDL block definition is furnished for reference.

HDL FILE

```
BLOCK S373LH;
D1              @INPUT;
D2              @INPUT;
D3              @INPUT;
D4              @INPUT;
D5              @INPUT;
D6              @INPUT;
D7              @INPUT;
D8              @INPUT;
C               @INPUT;
OCZ             @INPUT;
Q1              @OUTPUT;
Q2              @OUTPUT;
Q3              @OUTPUT;
Q4              @OUTPUT;
Q5              @OUTPUT;
Q6              @OUTPUT;
Q7              @OUTPUT;
Q8              @OUTPUT;

STRUCTURE
AO1             :AO221LH        D1,INV9O,INV10O,INV11O,AO1O;
AO2             :AO221LH        D2,INV9O,INV10O,INV12O,AO2O;
AO3             :AO221LH        D3,INV9O,INV10O,INV13O,AO3O;
AO4             :AO221LH        D4,INV9O,INV10O,INV14O,AO4O;
AO5             :AO221LH        D5,INV9O,INV10O,INV15O,AO5O;
AO6             :AO221LH        D6,INV9O,INV10O,INV16O,AO6O;
AO7             :AO221LH        D7,INV9O,INV10O,INV17O,AO7O;
AO8             :AO221LH        D8,INV9O,INV10O,INV18O,AO8O;
INV10           :IV140LH        C,INV10O;
INV11           :IV110LH        AO1O,INV11O;
INV12           :IV110LH        AO2O,INV12O;
INV13           :IV110LH        AO3O,INV13O;
INV14           :IV110LH        AO4O,INV14O;
INV15           :IV110LH        AO5O,INV15O;
INV16           :IV110LH        AO6O,INV16O;
INV17           :IV110LH        AO7O,INV17O;
INV18           :IV110LH        AO8O,INV18O;
INV20           :IV140LH        OCZ,INV20O;
INV21           :IV212LH        AO1O,INV20O,Q1;
INV22           :IV212LH        AO2O,INV20O,Q2;
INV23           :IV212LH        AO3O,INV20O,Q3;
INV24           :IV212LH        AO4O,INV20O,Q4;
INV25           :IV212LH        AO5O,INV20O,Q5;
INV26           :IV212LH        AO6O,INV20O,Q6;
INV27           :IV212LH        AO7O,INV20O,Q7;
INV28           :IV212LH        AO8O,INV20O,Q8;
INV9            :IV140LH        INV10O,INV9O;
END S373LH;
```


TEXAS INSTRUMENTS
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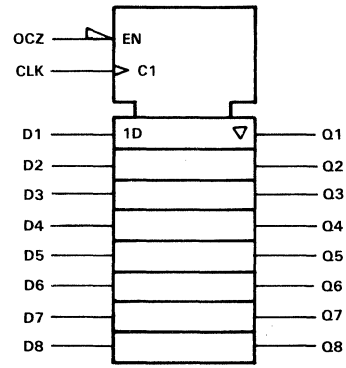
D2939, AUGUST 1986

SystemCell™ 2-μm SOFTWARE MACRO CELL

- **3-State Outputs Interface with Internal Data Buses Directly**
- **Buffered Output Control Simplifies System Design**
- **Embedded Clock Drivers Provide Symmetrical Performance Across Long Registers**
- **Parallel Latches for 16-Bit, 32-Bit, 64-Bit Word Widths**

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The SN54ASC374 and SN74ASC374 are standard-cell software macros implementing 8-bit D-type register elements designed specifically for interfacing internal bus lines. The 8-bit length simplifies construction of large registers. The 'ASC374 implements a function table identical with that performed by packaged 'HC374, 'LS374, and 'F374 latches.

The Output-Control input OCZ can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. When the outputs are enabled with OCZ low, the logic level at each of the eight outputs is impressed on the data bus. The outputs are disabled by a high logic level at OCZ. The outputs then present a high impedance to the internal bus. When the outputs are disabled, sequential operation of the flip-flops is not affected. The 'ASC374 is implemented with the standard cell functions indicated. The HDL netlist label for this software macro is shown on the last line of the following table:

CELL NAME	RELATIVE CELL AREA TO NA210LH	NO. USED	TOTAL RELATIVE CELL AREA	TOTAL C_{pd}‡ (pF)	MAXIMUM I_{CC} (nA)	
					SN54ASC'	SN74ASC'
IV120LH	1	1	1	0.8	131	7.85
R2407LH	26.25	2	52.5	22	6062	384
TO010LH	1.5	1	1.5	—	177	10.6
TOTALS		4	55	22.80	6370	403
Label: S374LH D1,D2,D3,D4,D5,D6,D7,D8,CLK,OCZ,Q1,Q2,Q3,Q4,Q5,Q6,Q7,Q8;						

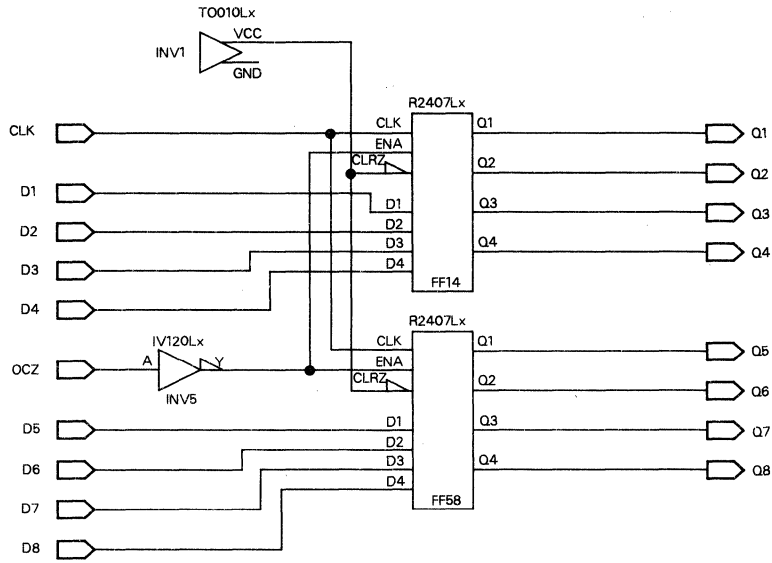
‡The equivalent power dissipation capacitance does not include interconnect capacitance.

The SN54ASC374 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC374 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUT
OCZ	CLK	Dn	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

logic diagram



TEXAS INSTRUMENTS
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absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

electrical characteristics

PARAMETER			TEST CONDITIONS		SN54ASC374		SN74ASC374		UNIT
					TYP	MAX	TYP	MAX	
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX	V_I = V_{CC} or 0,		6370		403	nA
C_i	Input capacitance	CLK	V_{CC} = 5 V,	T_A = 25°C	0.48		0.48		pF
		Dn			0.25		0.25		
		OCZ			0.24		0.24		
C_o	Output capacitance		V_{CC} = 5 V,	T_A = 25°C	0.24		0.24		pF
C_{pd}	Equivalent power dissipation capacitance†		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	22.8		22.8		pF

† The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted) (see Notes 1 and 2)

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC374			SN74ASC374			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
t_{pd}	CLK	Q	C_L = 0		5	11.4		5	10.4	ns
t_{en}	OCZ	Q			4	7.1		4	6.6	ns
Δt_{pd}	CLK	Q		0.6	1.7	4.6	0.6	1.7	4.2	ns
Δt_{en}	Any	Q		0.8	1.7	4.8	0.8	1.7	4.3	ns/pF

‡ Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{pd} ≡ propagation delay time, low-to-high-level or high-to-low-level output
t_{en} ≡ enable time, high-impedance state to low- or high-logic-level output
Δt_{pd} ≡ change in t_{pd} with load capacitance
Δt_{en} ≡ change in t_{en} with load capacitance
§ Typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTES: 1. These switching characteristics are simulations of the software macro cell using interconnect capacitance values for an array design having 2,000 gates. Actual performance can be evaluated at post-layout simulation.
2. Enable and delta-enable times are measured using the conditions specified for the 'ASC2407.

DESIGN CONSIDERATIONS

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

The HDL for this software macro is included as a part of the library supplied for supported engineering workstations so that a single label can be developed to apply the macro as needed. The following printout of the HDL block definition is furnished for reference.

HDL FILE

```
BLOCK S374LH;
D1          @INPUT;
D2          @INPUT;
D3          @INPUT;
D4          @INPUT;
D5          @INPUT;
D6          @INPUT;
D7          @INPUT;
D8          @INPUT;
CLK         @INPUT;
OCZ         @INPUT;
Q1          @OUTPUT;
Q2          @OUTPUT;
Q3          @OUTPUT;
Q4          @OUTPUT;
Q5          @OUTPUT;
Q6          @OUTPUT;
Q7          @OUTPUT;
Q8          @OUTPUT;

STRUCTURE
INV1        :TO010LH        DUM,ICLRZ;
INV5        :IV120LH        OCZ,INV5O;
FF14        :R2407LH        ICLRZ,D1,D2,D3,D4,CLK,INV5O,Q1,Q2,Q3,Q4;
FF58        :R2407LH        ICLRZ,D5,D6,D7,D8,CLK,INV5O,Q5,Q6,Q7,Q8;
END S374LH;
```

designing for testability

Designers employing storage or bistable elements, especially long registers (ripple or synchronous), should consider testability of the design in its final form. The need to preset or clear and read intermediate stages of these elements should be assessed throughout the development of custom logic circuits with these considerations extended to the end-equipment application with respect to maintainability. Simple actions on the part of the ASIC designer can result in considerable cost savings, allowing the expense of IC testing, system testing, and system maintenance to be reduced significantly.

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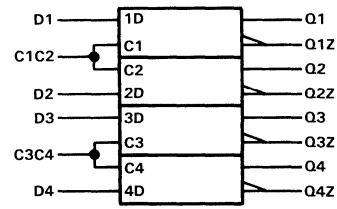
D2939, AUGUST 1986

SystemCell™ 2-μm SOFTWARE MACRO CELL

- **Four-Bit Software Latches with Complementary Outputs**
- **Eliminates Skew and Mismatch of Long versus Short Data Paths**
- **Parallel Latches for 8-Bit, 16-Bit, 32-Bit Word Widths**

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The SN54ASC375 and SN74ASC375 are standard-cell software macros implementing 4-bit bistable latch elements for embedding in ASICs. The 4-bit length simplifies construction of large registers. The 'ASC375 implements a function table identical with that performed by packaged 'HC375 and 'LS375 registers.

Information present at a Dn input is transferred to the Qn output when the Cn input is high, and the Qn output will follow the data input as long as Cn remains high. When Cn goes low, the data (that was present at the Dn input at the time the transition occurred) is retained at the Qn output until CnCn is taken high. The 'ASC375 is implemented with the standard cell functions indicated. The HDL netlist label for this software is shown on the last line of the following table:

CELL NAME	RELATIVE CELL AREA TO NA210LH	NO. USED	TOTAL RELATIVE CELL AREA	TOTAL C_{pd}‡ (pF)	MAXIMUM I_{CC} (nA)	
					SN54ASC'	SN74ASC'
AO221LH	2.7	4	10.8	2.36	896	53.6
IV110LH	0.75	4	3	1.76	420	25.28
IV120LH	1	4	4	3.2	524	31.4
TOTALS		12	17.8	7.32	1840	111
Label: S375LH D1,D2,D3,D4,C1C2,C3C4,Q1,Q1Z,Q2,Q2Z,Q3,Q3Z,Q4,Q4Z;						

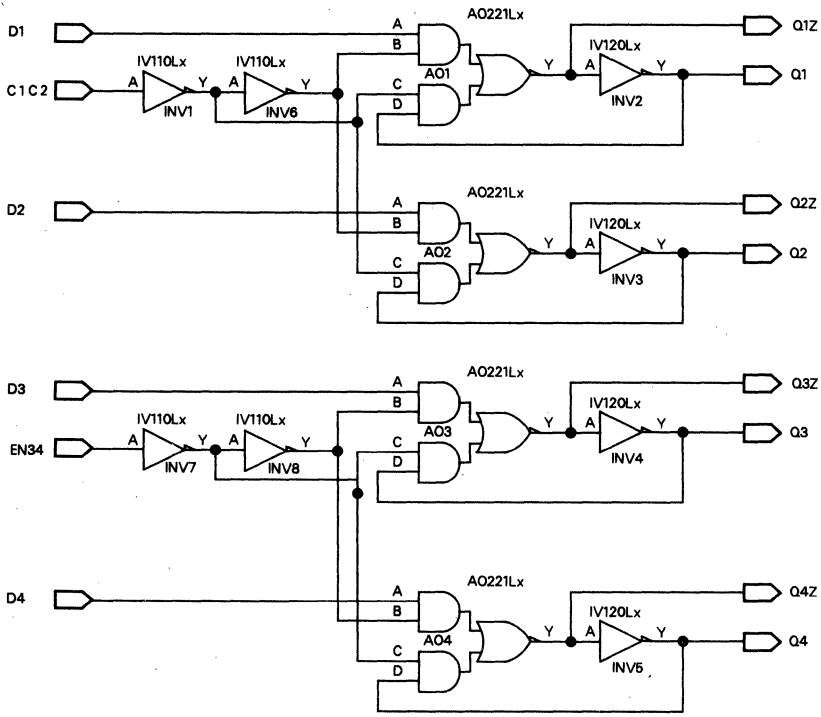
‡The equivalent power dissipation capacitance does not include interconnect capacitance.

The SN54ASC375 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC375 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS		OUTPUTS	
Dn	Cn	Qn	QnZ
L	H	L	H
H	H	H	L
X	L	Qn_0	$\overline{Qn_0}$

logic diagram



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absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation, produce workstation output used to identify and resolve each specific timing need.

electrical characteristics

PARAMETER		TEST CONDITIONS	SN54ASC375		SN74ASC375		UNIT
			TYP	MAX	TYP	MAX	
V_T Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC} Supply current		V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} to 0, T_A = MIN to MAX		1840		111	nA
C_i Input capacitance	Dn	V_{CC} = 5 V, T_A = 25°C	0.13		0.13		pF
	CnCm		0.12		0.12		
C_{pd} Equivalent power dissipation capacitance†		V_{CC} = 5 V, T_A = 25°C, t_r = t_f = 3 ns,	7.32		7.32		pF

† The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 1)

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC375			SN74ASC375			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
t_{pd}	Dn	Qn	C_L = 0		3	6.4		3	5.8	ns
t_{pd}	Dn	QnZ			2	4.8		2	4.8	
t_{pd}	Cn	Qn			5	10.2		5	9.5	ns
t_{pd}	Cn	QnZ			4.5	8.7		4.5	8	
Δt_{pd}	Any	Qn		0.3	0.5	1.1	0.3	0.5	1	ns/pF
Δt_{pd}	Any	Qnz		0.5	1.5	4.6	0.5	1.5	4.1	

‡ Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{pd} ≡ propagation delay time, low-to-high-level or high-to-low-level output
Δt_{pd} ≡ change in t_{pd} with load capacitance
§ Typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: These switching characteristics are simulations of the software macro cell using interconnect capacitance values for an array design having 2,000 gates. Post-layout simulation uses actual interconnect capacitance values.

DESIGN CONSIDERATIONS

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

The HDL for this software macro is included as a part of the library supplied for supported engineering workstations so that a single label can be developed to apply the macro as needed. The following printout of the HDL block definition is furnished for reference.

HDL FILE

```
BLOCK S375LH;
D1              @INPUT;
D2              @INPUT;
D3              @INPUT;
D4              @INPUT;
C1C2            @INPUT;
C3C4            @INPUT;
Q1              @OUTPUT;
Q1Z             @OUTPUT;
Q2              @OUTPUT;
Q2Z             @OUTPUT;
Q3              @OUTPUT;
Q3Z             @OUTPUT;
Q4              @OUTPUT;
Q4Z             @OUTPUT;

STRUCTURE
AO1             :AO221LH        D1,INV6O,INV1O,Q1,Q1Z;
AO2             :AO221LH        D2,INV6O,INV1O,Q2,Q2Z;
AO3             :AO221LH        D3,INV8O,INV7O,Q3,Q3Z;
AO4             :AO221LH        D4,INV8O,INV7O,Q4,Q4Z;
INV1            :IV110LH        C1C2,INV1O;
INV2            :IV120LH        Q1Z,Q1;
INV3            :IV120LH        Q2Z,Q2;
INV4            :IV120LH        Q3Z,Q3;
INV5            :IV120LH        Q4Z,Q4;
INV6            :IV110LH        INV1O,INV6O;
INV7            :IV110LH        C3C4,INV7O;
INV8            :IV110LH        INV7O,INV8O;
END S375LH;
```


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designing for testability

Designs employing storage or bistable elements, especially long registers (ripple or synchronous), should consider testability of the design in its final form. The need to preset or clear and read intermediate stages of these elements should be assessed throughout the development of custom logic circuits with these considerations extended to the end-equipment application with respect to maintainability. Simple actions on the part of the ASIC designer can result in considerable cost savings, allowing the expense of IC testing, system testing, and system maintenance to be reduced significantly.

power-up clear/preset

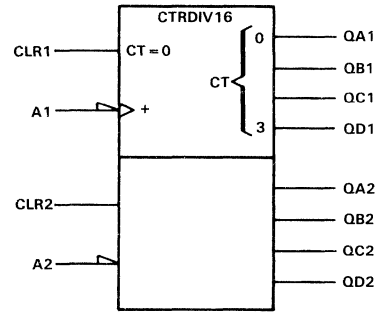
Standard cell storage elements containing the capability to be asynchronously preset or cleared may be connected to the SN54ASC2320 or SN74ASC2320 power-up clear cell to achieve system initialization. Control of the clear or preset inputs from another system signal in conjunction with the power-up clear can be achieved with an AND gate.

D2939, AUGUST 1986

SystemCell™ 2-μm SOFTWARE MACRO CELL

- **Software Dual Four-Bit Counter for Custom IC Applications**
- **Direct Clear Input Simplifies Initialization or Cycle Length**
- **Embedded Clock Drivers Provide Symmetrical Performance Across Long Counters**
- **Cascadable and Expandable for Full Customization**

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The SN54ASC393 and SN74ASC393 are standard-cell software macros implementing dual 4-bit binary counter elements. The dual 4-bit configuration provides the custom IC designer a fully designed counter element to embed in ASICs in its most efficient form, and the 4-bit length simplifies construction of large counters. The 'ASC393 implements a count sequence identical with that performed by packaged 'HC393 and 'LS393 counters.

This software macro reduces the input loading for implementation of larger counters, as standard library buffer cells are used to buffer each clock and clear input to further enhance the performance across long counters. The 'ASC393 is implemented with standard cell functions indicated. The HDL netlist label for this software is shown on the last line of the following table:

CELL NAME	RELATIVE CELL AREA TO NA210LH	NO. USED	TOTAL RELATIVE CELL AREA	TOTAL C_{pd}‡ (pF)	MAXIMUM I_{CC} (nA)	
					SN54ASC'	SN74ASC'
IV110LH	0.75	2	1.5	0.88	210	12.64
IV120LH	1	2	2	1.6	262	15.7
R2408LH	28.25	2	56.5	14.44	6926	416
TOTALS		6	60	16.92	7398	445
Label: S393LH A1,CLR1,A2,CLR2,QA1,QB1,QC1,QD1,QA2,QB2,QC2,QD2;						

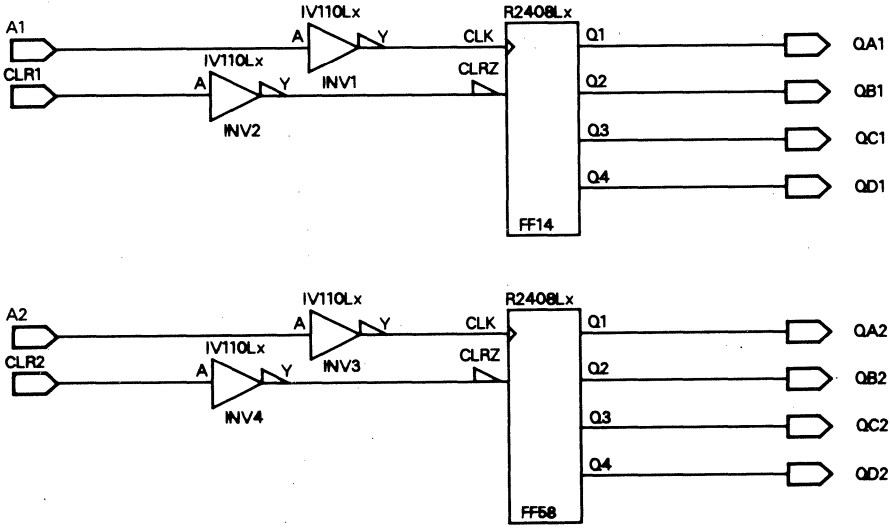
‡The equivalent power dissipation capacitance does not include interconnect capacitance.

The SN54ASC393 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC393 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(EACH COUNTER)

INPUTS		OUTPUTS			
CLRn	An	QDn	QCn	QBn	QAn
H	X	L	L	L	L
L	↓	L	L	L	H
L	↓	L	L	H	L
L	↓	L	L	H	H
L	↓	L	H	L	L
L	↓	L	H	L	H
L	↓	L	H	H	L
L	↓	L	H	H	H
L	↓	H	L	L	L
L	↓	H	L	L	H
L	↓	H	L	H	L
L	↓	H	L	H	H
L	↓	H	H	L	L
L	↓	H	H	L	H
L	↓	H	H	H	L
L	↓	H	H	H	H
L	↓	L	L	L	L

logic diagram



TEXAS INSTRUMENTS
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absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

electrical characteristics

PARAMETER			TEST CONDITIONS	SN54ASC393		SN74ASC393		UNIT
				TYP	MAX	TYP	MAX	
V_T	Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current		V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		7398		445	nA
C_i	Input capacitance	CLRn	V_{CC} = 5 V, T_A = 25°C	0.24		0.24		pF
		An		0.12		0.12		
C_{pd}	Equivalent power dissipation capacitance†		V_{CC} = 5 V, T_A = 25°C, t_r = t_f = 3 ns,	16.92		16.92		pF

† The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 1)

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC393			SN74ASC393			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
t_{pd}	Any	QA	C_L = 0		7	14.9		7	13.6	ns
t_{pd}		QD			14	31.5		14	28.5	ns
t_{PHL}	CLRn	Q			4.5	8.7		4.5	8.1	ns
Δt_{pd}	Any	Any Q		0.3	0.5	1.3	0.3	0.5	1.1	ns/pF

‡ Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{pd} ≡ propagation delay time, low-to-high-level or high-to-low-level output
t_{PHL} ≡ propagation delay time, high-to-low level output
Δt_{pd} ≡ change in t_{pd} with load capacitance
§ Typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: These switching characteristics are simulations of the software macro cell using interconnect capacitance values for an array design having 2,000 gates. Actual performance can be evaluated at post-layout simulation.

DESIGN CONSIDERATIONS

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

The HDL for this software macro is included as a part of the library supplied for supported engineering workstations so that a single label can be developed to apply the macro as needed. The following printout of the HDL block definition is furnished for reference.

HDL FILE

```
BLOCK S393LH;
A1          @INPUT;
CLR1        @INPUT;
A2          @INPUT;
CLR2        @INPUT;
QA1         @OUTPUT;
QB1         @OUTPUT;
QC1         @OUTPUT;
QD1         @OUTPUT;
QA2         @OUTPUT;
QB2         @OUTPUT;
QC2         @OUTPUT;
QD2         @OUTPUT;

STRUCTURE
INV1        :IV110LH        A1,INV1O;
INV2        :IV110LH        CLR1,INV2O;
INV3        :IV110LH        A2,INV3O;
INV4        :IV110LH        CLR2,INV4O;
FF14        :R2408LH        INV1O,INV2O,QA1,QB1,QC1,QD1;
FF58        :R2408LH        INV3O,INV4O,QA2,QB2,QC2,QD2;
END S393LH;
```

count definition

These counters are unidirectional with respect to count operations. Inverting the output levels will produce a down-count sequence. Bidirectional counters are available in software macros or can be constructed using the 'ASC2405 through 'ASC2407 4-bit predesigned registers.

designing for testability

Designs employing storage or bistable elements, especially long counters (ripple or synchronous), should consider testability of the design in its final form. The need to preset or clear and read intermediate stages of these elements should be assessed throughout the development of custom logic circuits, with these considerations extended to the end-equipment application with respect to maintainability. Simple actions on the part of the ASIC designer can result in considerable cost savings, allowing the expense of IC testing, system testing, and system maintenance to be reduced significantly.

power-up-clear/preset

Standard cell storage elements containing the capability to be asynchronously either preset or cleared may be connected through an inverter to the SN54ASC2320 or SN74ASC2320 power-up clear cell to achieve system initialization. Access to the clear inputs from other system signals in conjunction with power-up clear can be implemented with an OR gate.

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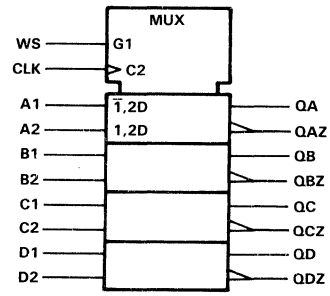
SystemCell™ 2-μm SOFTWARE MACRO CELL

- **Selects One of Two 4-Bit Data Sources and Stores Data Synchronously with System Clock**
- **Storage Register Loads New Data on Positive-Going Transition**
- **Implements Hexadecimal/BCD Shifter**
- **Use Parallel Multiplexers for Multiple-Bit Words**

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The SN54ASC398 and SN74ASC398 are standard-cell software macros implementing four 2-line to 1-line multiplexers with storage. The 'ASC398 implements a function table identical with that performed by packaged 'LS398 and 'F398 multiplexers.

When the word-select (WS) input is low, word 1 (A1, B1,C1, D1) is applied to the flip-flops. A high WS input causes word 2 (A2, B2, C2, D2) to be selected. The selected word is clocked to the output terminals on the positive-going edge of the clock pulse. The 'ASC398 is implemented with standard cell functions indicated. The HDL netlist label for this software macro is shown on the last line of the following table:

CELL NAME	RELATIVE CELL AREA TO NA210LH	NO. USED	TOTAL RELATIVE CELL AREA	TOTAL C_{pd}‡ (pF)	MAXIMUM I_{CC} (nA)	
					SN54ASC'	SN74ASC'
IV120LH	1	2	2	1.6	262	15.7
NA210LH	1	12	12	6.12	1572	94.2
R2405LH	26.25	1	26.25	11.7	2931	176
TO010LH	1.5	1	1.5	—	177	10.6
TOTALS		16	41.75	19.42	4942	297
Label: S398LH A1,A2,B1,B2,C1,C2,D1,D2,CLK,WS,QA,QAZ,QB,QBZ,QC,QCZ,QD,QDZ;						

‡The equivalent power dissipation capacitance does not include interconnect capacitance.

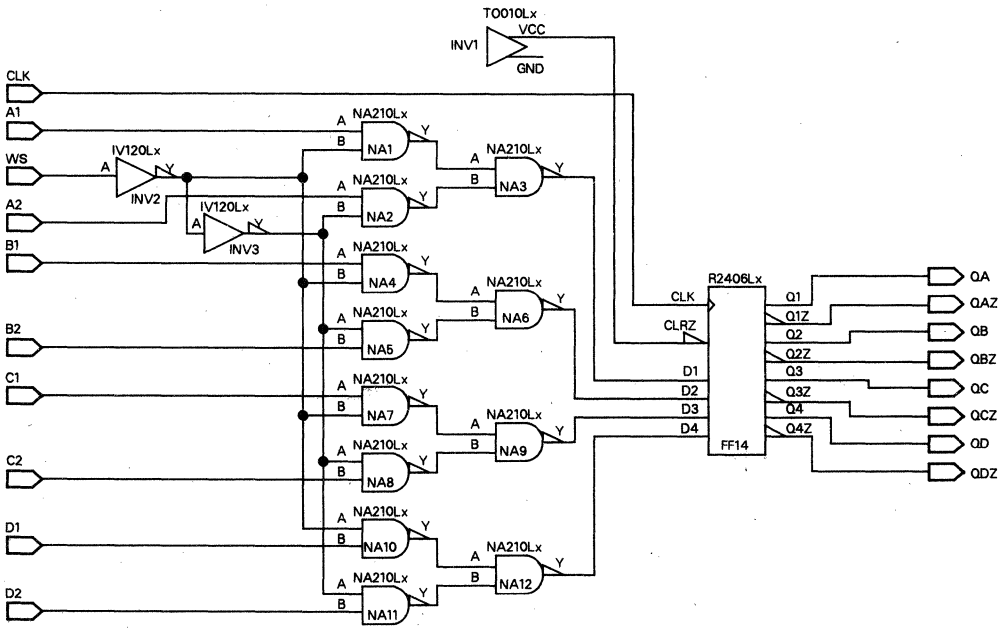
The SN54ASC398 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC398 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

INPUTS		OUTPUTS§			
WORD SELECT	CLK	QA	QB	QC	QD
L	↑	a1	b1	c1	d1
H	↑	a2	b2	c2	d2
X	L	QA_0	QB_0	QC_0	QD_0

§Corresponding QnZ output is the complement of Qn (shown).

logic diagram



timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements are made during pre-layout simulation that produce workstation output used to identify and resolve each specific timing need.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS	SN54ASC398 TYP	SN54ASC398 MAX	SN74ASC398 TYP	SN74ASC398 MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current		V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		4942		297	nA
C_i	Input capacitance	CLK	V_{CC} = 5 V, T_A = 25°C	0.24		0.24		pF
		WS		0.24		0.24		
		All others		0.12		0.12		
C_{pd}	Equivalent power dissipation capacitance†		V_{CC} = 5 V, T_A = 25°C, t_r = t_f = 3 ns,	19.42		19.42		pF

† The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 1)

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC398			SN74ASC398			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
t_{pd}	CLK	Qn	C_L = 0		5	10.6		5	9.6	ns
t_{pd}	CLK	QnZ			5.5	12.5		5.5	11.3	ns
Δt_{pd}	Any	Qn		0.2	0.9	2.4	0.3	0.9	2.1	ns/pF

‡ Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{pd} ≡ propagation delay time, low-to-high-level or high-to-low-level output
Δt_{pd} ≡ change in t_{pd} with load capacitance
§ Typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: These switching characteristics are simulations of the software macro cell using interconnect capacitance values for an array design having 2,000 gates. Post-layout simulation uses actual interconnect capacitance values.

DESIGN CONSIDERATIONS

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

The HDL for this software macro is included as a part of the library supplied for supported engineering workstations so that a single label can be developed to apply the macro as needed. The following printout of the HDL block definition is furnished for reference.

HDL FILE

```
BLOCK S398LH;
A1          @INPUT;
A2          @INPUT;
B1          @INPUT;
B2          @INPUT;
C1          @INPUT;
C2          @INPUT;
D1          @INPUT;
D2          @INPUT;
CLK         @INPUT;
WS          @INPUT
QA          @OUTPUT;
QAZ         @OUTPUT;
QB          @OUTPUT;
QBZ         @OUTPUT;
QC          @OUTPUT;
QCZ         @OUTPUT;
QD          @OUTPUT;
QDZ         @OUTPUT;
```

HDL FILE (Continued)

```
STRUCTURE
FF14        :R2406LH      INV1O,NA3O,NA6O,NA9O,NA12O,CLK,QA,QAZ,QB,QBZ,
                          QC,QCZ,QD,QDZ;
INV1        :TO010LH      DUM,INV1O;
INV2        :IV120LH      WS,INV2O;
INV3        :IV120LH      INV2O,INV3O;
NA1         :NA210LH      A1,INV2O,NA1O;
NA10        :NA210LH      INV2O,D1,NA10O;
NA11        :NA210LH      INV3O,D2,NA11O;
NA12        :NA210LH      NA10O,NA11O,NA12O;
NA2         :NA210LH      A3,INV3O,NA2O;
NA3         :NA210LH      NA1O,NA2O,NA3O;
NA4         :NA210LH      B1,INV2O,NA4O;
NA5         :NA210LH      INV3O,B2,NA5O;
NA6         :NA210LH      NA4O,NA5O,NA6O;
NA7         :NA210LH      C1,INV2O,NA7O;
NA8         :NA210LH      INV3O,C2,NA8O;
NA9         :NA210LH      NA7O,NA8O,NA9O;
END S398LH;
```

Dedicated 2-line to 1-line multiplexers ('ASC2340) are also available in the standard cell library for implementing data-path multiplexers. These hardwired multiplexers in conjunction with hardwired registers should be considered if the multiplexer is in a critical path, as their performance is predetermined as specified in their switching characteristics.

interfacing the macro

Inputs and outputs of the predesigned macro are compatible for interfacing directly with cells and macros available in the TI standard cell library.

The inputs can be driven by either inverting or noninverting input cells. The outputs can be interfaced to drive off-chip loads with noninverting output buffers or interfaced to external bidirectional buses through a 3-state input/output TTL/CMOS buffer.

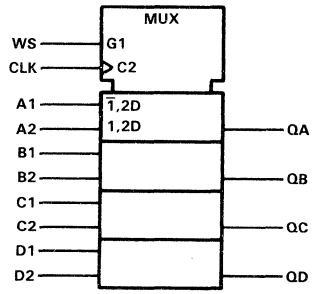
implementing 4-bit (digit) shifter

Implementation of a digit shifter is illustrated on the 'ASC298 data sheet.

SystemCell™ 2-μm SOFTWARE MACRO CELL

- **Selects One of Two 4-Bit Data Sources and Stores Data Synchronously with System Clock**
- **Storage Register Loads New Data on Positive-Going Transition**
- **Implements Hexadecimal/BCD Shifter**
- **Use Parallel Multiplexers for Multiple-Bit Words**

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The SN54ASC399 and SN74ASC399 are standard-cell software macros implementing four 2-line to 1-line multiplexers with storage. The 'ASC399 implements a function table identical with that performed by packaged 'LS399 and 'F399 multiplexers.

When the word-select (WS) input is low, word one (A1, B1, C1, D1) is applied to the flip-flops. A high WS input causes word two (A2, B2, C2, D2) to be selected. The selected word is clocked to the output terminals on the positive-going edge of the clock pulse. The 'ASC399 is implemented with standard cell functions indicated. The HDL netlist label for this software macro is shown on the last line of the following table:

CELL NAME	RELATIVE CELL AREA TO NA210LH	NO. USED	TOTAL RELATIVE CELL AREA	TOTAL C_{pd}‡ (pF)	MAXIMUM I_{CC} (nA)	
					SN54ASC'	SN74ASC'
IV120LF1	1	2	2	1.6	262	15.7
NA210LF1	1	12	12	6.12	1572	94.2
R2405LF1	23.25	1	23.25	10.2	2647	159
TO010LF1	1.5	1	1.5	–	177	10.6
TOTALS		16	38.75	17.92	4658	280
Label: S399LH A1,A2,B1,B2,C1,C2,D1,D2,CLK,WS,QA,QB,QC,QD;						

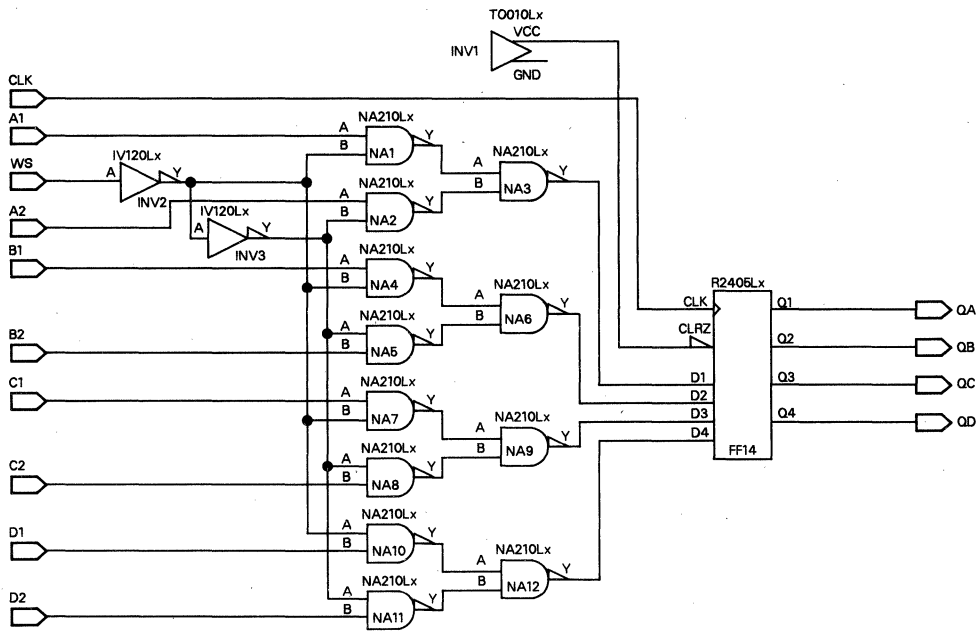
‡The equivalent power dissipation capacitance does not include interconnect capacitance.

The SN54ASC399 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC399 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

INPUTS		OUTPUTS			
WORD SELECT	CLK	QA	QB	QC	QD
L	↑	a1	b1	c1	d1
H	↑	a2	b2	c2	d2
X	L	QA_0	QB_0	QC_0	QD_0

logic diagram



timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation that produce workstation output are used to identify and resolve each specific timing need.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS		SN54ASC399 TYP	SN54ASC399 MAX	SN74ASC399 TYP	SN74ASC399 MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX	V_I = V_{CC} or 0,		4658		280	nA
C_i	Input capacitance	CLK	V_{CC} = 5 V,	T_A = 25°C	0.24		0.24		pF
		WS			0.24		0.24		
		All others			0.12		0.12		
C_{pd}	Equivalent power dissipation capacitance†		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	17.92		17.92		pF

† The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted) (see Note 1)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC399			SN74ASC399			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{pd}	CLK	Qn	C_L = 0		5	10.7		5	9.6	ns
Δt_{pd}	CLK	Qn		0.3	0.8	2.3	0.3	0.8	2.1	ns/pF

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{pd} ≡ propagation delay time, low-to-high-level or high-to-low-level output
Δt_{pd} ≡ change in t_{pd} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: These switching characteristics are simulations of the software macro cell using interconnect capacitance values for an array design having 2,000 gates. Post-layout simulation uses actual interconnect capacitance values.

DESIGN CONSIDERATIONS

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

The HDL for this software macro is included as a part of the library supplied for supported engineering workstations so that a single label can be developed to apply the macro as needed. The following printout of the HDL block definition is furnished for reference.

HDL FILE

```
BLOCK S399LH;
A1          @INPUT;
A2          @INPUT;
B1          @INPUT;
B2          @INPUT;
C1          @INPUT;
C2          @INPUT;
D1          @INPUT;
D2          @INPUT;
CLK         @INPUT;
WS          @INPUT
QA          @OUTPUT;
QB          @OUTPUT;
QC          @OUTPUT;
QD          @OUTPUT;
```

HDL FILE (Continued)

```
STRUCTURE
FF14        :R2405LH      INV1O,NA3O,NA6O,NA9O,NA12O,CLK,QA,QB,QC,QD;
INV1        :TO010LH      DUM,INV1O;
INV2        :IV120LH      WS,INV2O;
INV3        :IV120LH      INV2O,INV3O;
NA1         :NA210LH      A1,INV2O,NA1O;
NA10        :NA210LH      INV2O,D1,NA10O;
NA11        :NA210LH      INV3O,D2,NA11O;
NA12        :NA210LH      NA10O,NA11O,NA12O;
NA2         :NA210LH      A2,INV3O,NA2O;
NA3         :NA210LH      NA1O,NA2O,NA3O;
NA4         :NA210LH      B1,INV2O,NA4O;
NA5         :NA210LH      INV3O,B2,NA5O;
NA6         :NA210LH      NA4O,NA5O,NA6O;
NA7         :NA210LH      C1,INV2O,NA7O;
NA8         :NA210LH      INV3O,C2,NA8O;
NA9         :NA210LH      NA7O,NA8O,NA9O;
END S399LH;
```


Dedicated 2-line to 1-line multiplexers ('ASC2340) are also available in the standard cell library for implementing data-path multiplexers. These hardwired multiplexers in conjunction with hardwired registers should be considered if the multiplexer is in a critical path, as their performance is predetermined as specified in their switching characteristics.

interfacing the macro

Inputs and outputs of the predesigned macro are compatible for interfacing directly with cells and macros available in the TI standard cell library.

The inputs can be driven by either inverting or noninverting input cells. The outputs can be interfaced to drive off-chip loads with noninverting output buffers or interfaced to external bidirectional buses through a 3-state input/output TTL/CMOS buffer.

implementing 4-bit (digit) shifter

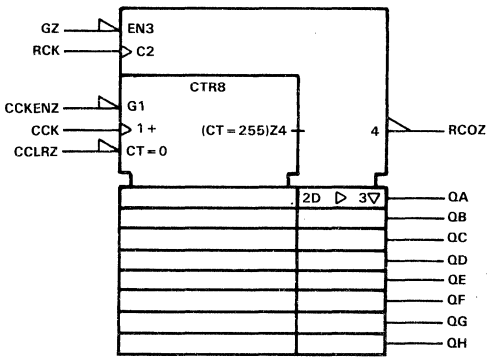
Implementation of a digit shifter is illustrated on the 'ASC298 data sheet.

D2939, AUGUST 1986

SystemCell™ 2-μm SOFTWARE MACRO CELL

- 8-Bit Counter with Register
- Individual Positive-Edge-Triggered Clocks for Counter and Register
- 3-State Output Register Provides Parallel Bus Interface
- Counter Has Direct Clear and Clock Enable
- Ripple-Carry Output Simplifies Expansion

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The SN54ASC590 and SN74ASC590 are standard-cell software macros implementing synchronous 8-bit binary counter elements. The 8-bit configuration provides the custom IC designer a counter to embed in ASICs in its most efficient form, and the 8-bit length simplifies construction of large counters. The 'ASC590 implements a function table identical with that performed by packaged 'HC590 and 'LS590 counters.

The 'ASC590 implements an 8-bit binary counter that feeds an 8-bit storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for both the binary counter and storage register. The binary counter features a direct clear input CCLRZ and a count enable input CCKENZ. For cascading, a ripple-carry output RCOZ is provided. Expansion is easily accomplished by tying RCOZ of the lower stage to CCKENZ of the higher stage, etc. The 'ASC590 is implemented with the standard cell functions indicated. The HDL netlist label for this software macro is shown on the last line of the following table:

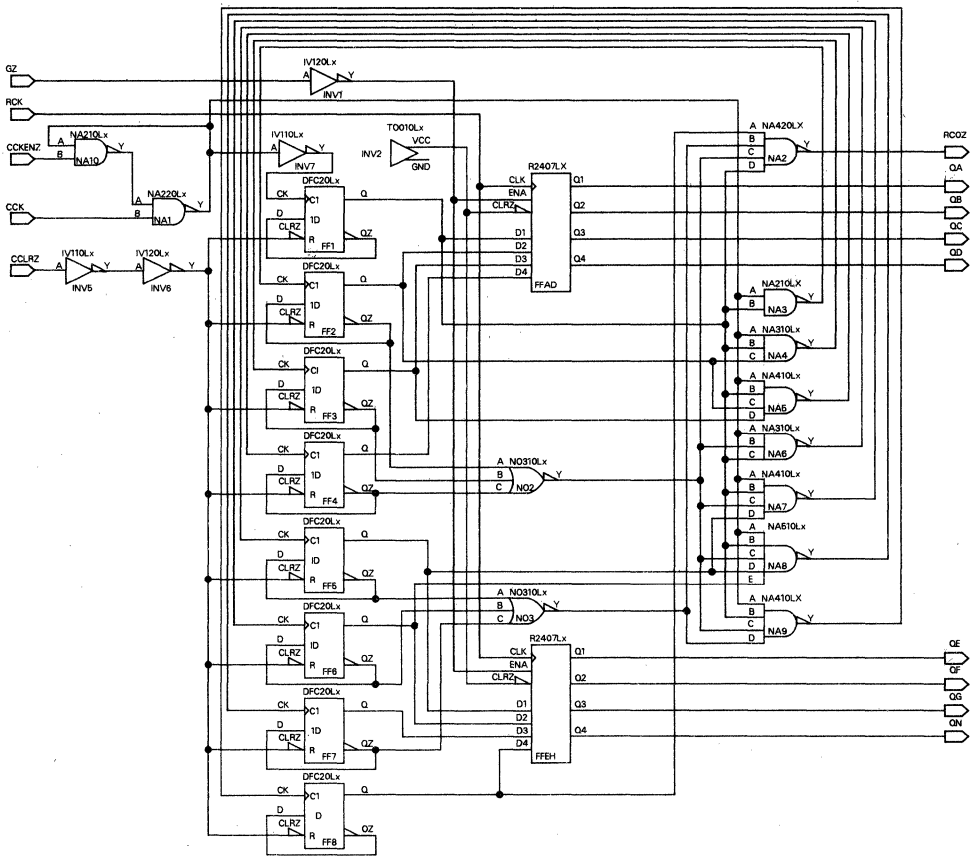
CELL NAME	RELATIVE CELL AREA TO NA210LH	NO. USED	TOTAL RELATIVE CELL AREA	TOTAL C_{pd}‡ (pF)	MAXIMUM I_{CC} (nA)	
					SN54ASC'	SN74ASC'
DFC20LH	7.2	8	57.6	27.12	7048	423.2
IV110LH	0.75	2	1.5	0.88	210	12.64
IV120LH	1	2	2	1.6	262	15.7
NA210LH	1	2	2	1.02	262	15.68
NA220LH	1.5	1	1.5	1	196	11.7
NA310LH	1.25	2	2.5	1	326	19.56
NA410LH	1.5	3	4.5	1.5	561	33.6
NA420LH	2.5	1	2.5	0.96	312	18.7
NA510LH	1.75	1	1.75	0.52	213	12.8
NO310LH	1.25	2	2.5	0.64	312	18.66
R2407LH	26.25	2	52.5	22	6062	384
TO010LH	1.5	1	1.5	—	177	10.6
TOTALS		27	132.35	58.24	15941	977
Label: S590LH CCK,CCKENZ,RCK,CCLRZ,GZ,QA,QB,QC,QD,QE,QF,QG,QH,RCOZ;						

‡The equivalent power dissipation capacitance does not include interconnect capacitance.

Both the counter and register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the counter state will always be one count ahead of the register. Internal circuitry prevents clocking from the clock enable.

The SN54ASC590 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC590 is characterized for operation from −40°C to 85°C.

logic diagram



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absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements are made during pre-layout simulation that produce workstation output used to identify and resolve each specific timing need.

electrical characteristics

PARAMETER			TEST CONDITIONS	SN54ASC590		SN74ASC590		UNIT
				TYP	MAX	TYP	MAX	
V_T	Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current		V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		15941		977	nA
C_i	Input capacitance	CCK	V_{CC} = 5 V, T_A = 25°C	0.26		0.26		pF
		CCKENZ,CCLRZ		0.12		0.12		
		GZ		0.24		0.24		
		RCK		0.48		0.48		
C_{pd}	Equivalent power dissipation capacitance†		V_{CC} = 5 V, t_r = t_f = 3 ns, T_A = 25°C	58.24		58.24		pF

† The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted) (see Notes 1 and 2)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC590			SN74ASC590			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{pd}	CCK↑	RCOZ	C_L = 0		10.4	22.8		10.4	20.4	ns
t_{pd}	CCLRZ↓	RCOZ			7.4	13.5		7.4	12.3	ns
t_{pd}	RCK↑	Qn			5.7	11.6		5.7	10.6	ns
t_{en}	GZ↓	Qn			3.1	6		3.1	5.6	ns
Δt_{pd}	Any	Qn		0.6	1.6	4.6	0.6	1.6	4.2	ns/pF
Δt_{pd}	Any	RCOZ		0.3	0.7	2.3	0.3	0.7	2	ns/pF
Δt_{en}	Any	Qn		0.8	1.7	4.8	0.8	1.7	4.3	ns/pF

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{pd} ≡ propagation delay time, low-to-high-level or high-to-low-level output
t_{en} ≡ enable time, high-impedance state to low- or high-logic-level output
Δt_{pd} ≡ change in t_{pd} with load capacitance
Δt_{en} ≡ change in t_{en} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTES: 1. These switching characteristics are simulations of the software macro cell using interconnect capacitance values for an array design having 2,000 gates. Actual performance can be evaluated at post-layout simulation.
2. Enable and delta-enable times are measured using the conditions specified for the 'ASC2407.

DESIGN CONSIDERATIONS

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

The HDL for this software macro is included as a part of the library supplied for supported engineering workstations so that a single label can be developed to apply the macro as needed. The following printout of the HDL block definition is furnished for reference.

HDL FILE

```
BLOCK S590LH;
CCK          @INPUT;
CCKENZ       @INPUT;
RCK          @INPUT;
CCLRZ        @INPUT;
GZ           @INPUT;
QA           @OUTPUT;
QB           @OUTPUT;
QC           @OUTPUT;
QD           @OUTPUT;
QE           @OUTPUT
QF           @OUTPUT;
QG           @OUTPUT;
QH           @OUTPUT;
RCOZ         @OUTPUT;

STRUCTURE
FF1          :DFC20LH        INV6O,FF1QZ,INV7O,FF1Q,FF1QZ;
FF2          :DFC20LH        INV6O,FF2QZ,NA3O,FF2Q,FF2QZ;
FF3          :DFC20LH        INV6O,FF3QZ,NA4O,FF3Q,FF3QZ;
FF4          :DFC20LH        INV6O,FF4QZ,NA5O,FF4Q,FF4QZ;
FF5          :DFC20LH        INV6O,FF5QZ,NA6O,FF5Q,FF5QZ;
FF6          :DFC20LH        INV6O,FF6QZ,NA7O,FF6Q,FF6QZ;
FF7          :DFC20LH        INV6O,FF7QZ,NA8O,FF7Q,FF7QZ;
FF8          :DFC20LH        INV6O,FF8QZ,NA9O,FF8Q,FF8QZ;
INV1         :IV120LH        GZ,INV1O;
INV2         :TO010LH        DUM,INV2O;
INV5         :IV110LH        CCLRZ,INV5O;
INV6         :IV120LH        INV5O,INV6O;
INV7         :IV110LH        NA1O,INV7O;
```


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HDL FILE (Continued)

```
STRUCTURE (Continued)
NA1      :NA220LH    NA100,CCK,NA1O;
NA10     :NA210LH    NA1O,CCKENZ,NA10O;
NA2      :NA420LH    FF8Q,NO3O,NO2O,FF1Q,RCOZ;
NA3      :NA210LH    NA1O,FF1Q,NA3O;
NA4      :NA310LH    NA1O,FF1Q,FF2Q,NA4O;
NA5      :NA410LH    NA1O,FF1Q,FF2Q,FF3Q,NA5O;
NA6      :NA310LH    NA1O,NO2O,FF1Q,NA6O;
NA7      :NA410LH    NA1O,FF1Q,NO2O,FF5Q,NA7O;
NA8      :NA510LH    NA1O,FF1Q,NO2O,FF5Q,FF6Q,NA8O;
NA9      :NA410LH    NA1O,FF1Q,NO2O,NO3O,NA9O;
NO2      :NO310LH    FF2QZ,FF3QZ,FF4QZ,NO2O;
NO3      :NO310LH    FF5QZ,FF6QZ,FF7QZ,NO3O;
FFAD     :R2407LH    INV2O,FF1Q,FF2Q,FF3Q,FF4Q,RCK,INV1O,QA,QB,QC,QD;
FFEH     :R2407LH    INV2O,FF5Q,FF6Q,FF7Q,FF8Q,RCK,INV1O,QE,QF,QG,QH;
END S590LH;
```

count defintion

These counters are unidirectional with respect to count operation. Inverting the output levels will produce a down-count sequence. Bidirectional counters are available in software macros or can be constructed using the 'ASC2405 through 'ASC2407 4-bit predesigned registers. Additional single bits can be achieved with predesigned flip-flops offered in TI's standard cell family.

designing for testability

Designs employing storage or bistable elements, especially long counters (ripple or synchronous), should consider testability of the design in its final form. The need to preset or clear and read intermediate stages of these elements should be assessed throughout the development of custom logic circuits, with these considerations extended to the end-equipment application with respect to maintainability. Simple actions on the part of the ASIC designer can result in considerable cost savings, allowing the expense of IC testing, system testing, and system maintenance to be reduced significantly.

power-up-clear/preset

Standard cell storage elements containing the capability to be asynchronously either preset or cleared may be connected to the SN54ASC2320 or SN74ASC2320 power-up clear cell to achieve system initialization. Access to the clear inputs from other system signals in conjunction with the power-up clear can be accomplished with an AND gate.

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SystemCell™ 2-μm SOFTWARE MACRO CELL

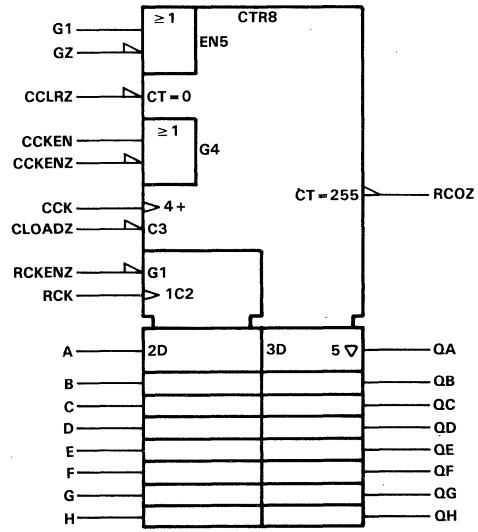
- 8-Bit Counter with Input Registers
- Individual Positive-Edge-Triggered Clocks for Counter and Register
- 3-State Counter Outputs Provide Parallel Bus Interface
- Counter Has Direct Clear and Clock Enable
- Ripple-Carry Output Simplifies Expansion

description

The SN54ASC593X and SN74ASC593X are standard-cell software macros implementing synchronous 8-bit binary counter elements. The 8-bit configuration provides the custom IC designer a counter to embed in ASICs in its most efficient form, and the 8-bit length simplifies construction of large counters. The 'ASC593X implements a count sequence identical with that performed by packaged 'HC593 and 'LS593 counters, but the common data input/output terminals have been separated to provide individual data inputs to the register and 3-state outputs from the counter.

The 'ASC593X implements an 8-bit storage register that feeds an 8-bit binary counter.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

The counter has parallel 3-state outputs. Separate clocks are provided for both the binary counter and storage register. The 'ASC593X is implemented with the standard cell functions indicated. The HDL netlist label for this software macro is shown on the last line of the table on the following page.

CELL NAME	RELATIVE CELL AREA TO NA210LH	NO. USED	TOTAL RELATIVE CELL AREA	TOTAL C_{pd}† (pF)	MAXIMUM I_{CC} (nA)	
					SN54ASC′	SN74ASC′
AN210LH	1.5	8	12	7.2	1552	92.8
DFB20LH	7.7	8	61.6	30.08	7472	448
IV110LH	0.75	4	3	1.76	420	25.28
IV120LH	1	2	2	1.6	262	15.7
IV140LH	1.5	1	1.5	1.61	190	11.4
IV212LH	1.5	8	12	4	720	86.4
NA210LH	1	19	19	9.69	2489	148.96
NA220LH	1.5	1	1.5	1	131	7.84
NA310LH	1.25	3	3.75	1.5	489	29.34
NA410LH	1.5	3	4.5	1.5	561	33.6
NA420LH	2.5	1	2.5	0.96	312	18.7
NA510LH	1.75	1	1.75	0.52	213	12.8
NO310LH	1.25	2	2.5	0.64	312	18.66
OR210LH	1.5	1	1.5	0.86	185	11.1
R2406LH	26.25	2	52.5	23.4	5862	352
TO010LH	1.5	1	1.5	–	177	10.6
TOTALS		65	183.1	86.32	21347	1324
Label: S593XLH A,B,C,D,E,F,G,H,CCK,CCKEN,CCKENZ,RCK,RCKENZ,CCLRZ,CLOADZ,G1,GZ,QA,QB, QC,QD,QE,QF,QG,QH,RCOZ;						

†The equivalent power dissipation capacitance does not include interconnect capacitance.

The binary counter features a direct clear input CCLRZ and a count enable input CCKENZ. For cascading, a ripple-carry output RCOZ is provided. Expansion is easily accomplished by tying RCOZ of the lower stage to CCKENZ of the higher stage, etc. Both the counter and register clocks are positive-edge-triggered. If the user wishes to connect both clocks together, the counter state will equal the previous register contents plus one. Internal circuitry prevents clocking from the clock enable.

The SN54ASC593X is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC593X is characterized for operation from −40°C to 85°C.

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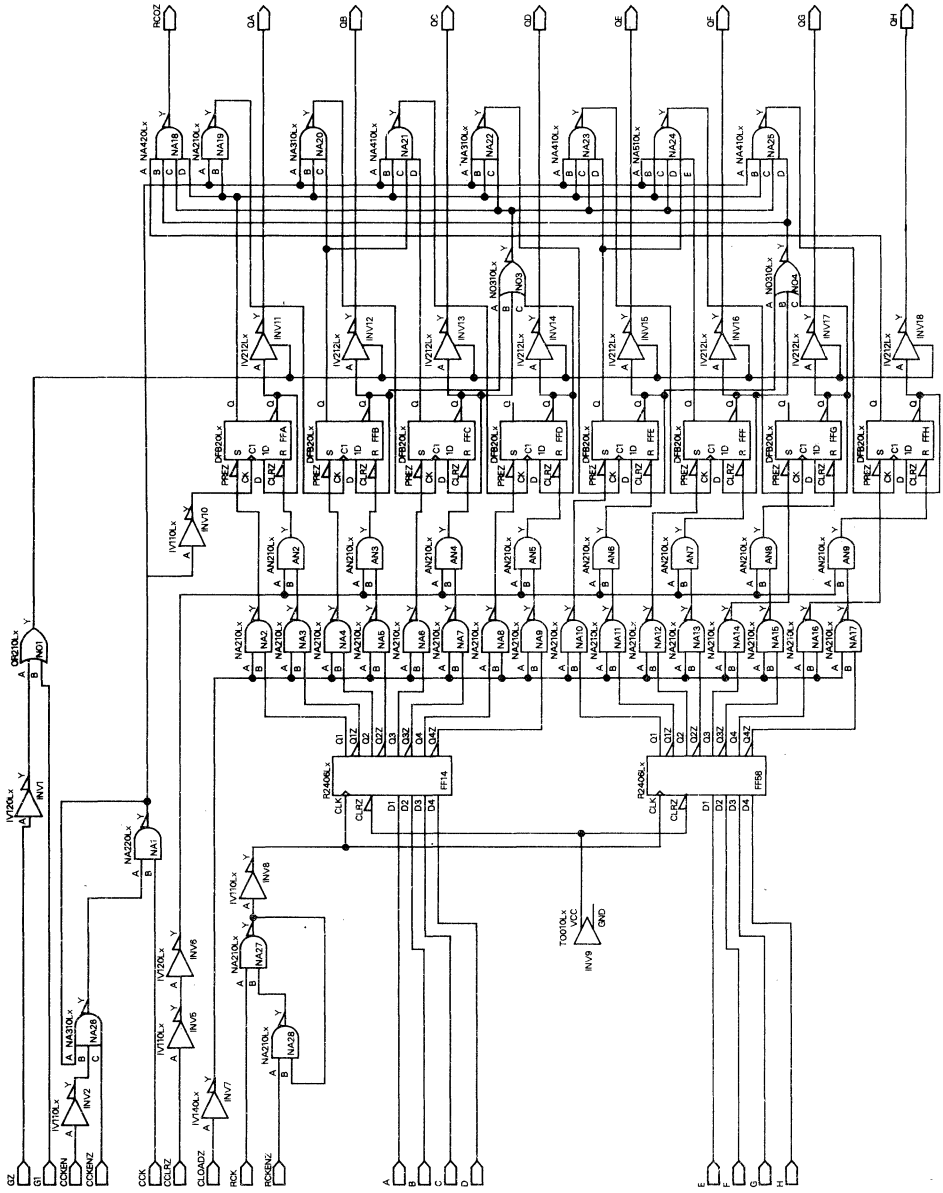
logic diagram



absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements, made during pre-layout simulation, produce workstation output used to identify and resolve each specific timing need.

electrical characteristics

PARAMETER		TEST CONDITIONS	SN54ASC593X TYP	SN54ASC593X MAX	SN74ASC593X TYP	SN74ASC593X MAX	UNIT
V_T Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC} Supply current		V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		21347		1324	nA
C_i Input capacitance	A thru H	V_{CC} = 5 V, T_A = 25°C	0.13		0.13		pF
	CCK		0.26		0.26		
	CLOADZ		0.49		0.49		
	G1		0.11		0.11		
	GZ		0.24		0.24		
	All others		0.12		0.12		
C_{pd} Equivalent power dissipation capacitance†		V_{CC} = 5 V, T_A = 25°C, t_r = t_f = 3 ns,	86.32		86.32		pF

† The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Notes 1 and 2)

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC593X MIN	SN54ASC593X TYP§	SN54ASC593X MAX	SN74ASC593X MIN	SN74ASC593X TYP§	SN74ASC593X MAX	UNIT
t_{pd}	CCK↑	RCOZ	C_L = 0		9	23.2		9	20.7	ns
t_{pd}	CCLRZ↓	RCOZ			8	15		8	13.8	ns
t_{pd}	CCLRZ↓	Qn			10	21.1		10	19	ns
t_{pd}	CCK↑	Qn			9	23.1		9	20.7	ns
t_{pd}	CLOADZ	Qn			9	21.6		9	19.4	ns
t_{pd}	CLOADZ	RCOZ			10	24.4		10	22.1	ns
t_{en}	G1 or GZ↑	Qn			4	8.8		4	8.1	ns
Δt_{pd}	Any	Qn		0.6	1.6	4.6	0.6	1.6	4.2	ns/pF
Δt_{pd}	Any	RCOZ		0.3	0.7	2.3	0.3	0.7	2	ns/pF
Δt_{en}	Any	Qn		0.8	1.7	4.8	0.8	1.7	4.4	ns/pF

‡ Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{pd} ≡ propagation delay time, low-to-high-level or high-to-low-level output
t_{en} ≡ enable time, low-to-high-level or high-to-low-level output
Δt_{pd} ≡ change in t_{pd} with load capacitance
Δt_{en} ≡ change in t_{en} with load capacitance
§ Typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTES: 1. These switching characteristics are simulations of the software macro cell using interconnect capacitance values for an array design having 2,000 gates. Actual performance can be evaluated at post-layout simulation.
2. Enable and delta-enable times are measured using the conditions specified for the 'ASC2407.

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DESIGN CONSIDERATIONS

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

The HDL for this software macro is included as a part of the library supplied for supported engineering workstations so that a single label can be developed to apply the macro as needed. The following printout of the HDL block definition is furnished for reference.

HDL FILE

```
BLOCK S593XLH;
A           @INPUT;
B           @INPUT;
C           @INPUT;
D           @INPUT;
E           @INPUT;
F           @INPUT;
G           @INPUT;
H           @INPUT;
CCK         @INPUT;
CCKEN       @INPUT;
CCKENZ      @INPUT;
RCK         @INPUT;
RCKENZ      @INPUT;
CCLRZ       @INPUT;
CLOADZ      @INPUT;
G1          @INPUT;
GZ          @INPUT;
QA          @OUTPUT;
QB          @OUTPUT;
QC          @OUTPUT;
QD          @OUTPUT;
QE          @OUTPUT
QF          @OUTPUT;
QG          @OUTPUT;
QH          @OUTPUT;
RCOZ        @OUTPUT;

STRUCTURE
AN2         :AN210LH        INV6O,NA3O,AN2O;
AN3         :AN210LH        INV6O,NA5O,AN3O;
AN4         :AN210LH        INV6O,NA7O,AN4O;
AN5         :AN210LH        INV6O,NA9O,AN5O;
AN6         :AN210LH        INV6O,NA11O,AN6O;
AN7         :AN210LH        INV6O,NA13O,AN7O;
AN8         :AN210LH        INV6O,NA15O,AN8O;
AN9         :AN210LH        INV6O,NA17O,AN9O;
FFA         :DFB20LH        AN2O,NA2O,FFAQZ,INV10O,FFAQ,FFAQZ;
FFB         :DFB20LH        AN3O,NA4O,FFBQZ,NA19O,FFBQ,FFBQZ;
FFC         :DFB20LH        AN4O,NA6O,FFCQZ,NA20O,FFCQ,FFCQZ;
FFD         :DFB20LH        AN5O,NA8O,FFDQZ,NA21O,DUM,FFDQZ;
FFE         :DFB20LH        AN6O,NA10O,FFEQZ,NA22O,FFEQ,FFEQZ;
```

HDL FILE (Continued)

```
STRUCTURE (Continued)
FFF          :DFB20LH        AN7O,NA12O,FFFQZ,NA23O,FFFQ,FFFQZ;
FFG          :DFB20LH        AN8O,NA14O,FFGQZ,NA24O,DUM,FFGQZ;
FFH          :DFB20LH        AN9O,NA16O,FFHQZ,NA25O,FFHQ,FFHQZ;
INV1         :IV120LH        GZ,INV1O;
INV1O        :IV110LH        NA1O,INV10O;
INV11        :IV212LH        FFAQZ,NO1O,QA;
INV12        :IV212LH        FFBQZ,NO1O,QB;
INV13        :IV212LH        FFCQZ,NO1O,QC;
INV14        :IV212LH        FFDQZ,NO1O,QD;
INV15        :IV212LH        FFEQZ,NO1O,QE;
INV16        :IV212LH        FFFQZ,NO1O,QF;
INV17        :IV212LH        FFGQZ,NO1O,QG;
INV18        :IV212LH        FFHQZ,NO1O,QH;
INV2         :IV110LH        CCKEN,INV2O;
INV5         :IV110LH        CCLRZ,INV5O;
INV6         :IV120LH        INV5O,INV6O;
INV7         :IV140LH        CLOADZ,INV7O;
INV8         :IV110LH        NA27O,RCFQZ;
INV9         :TO010LH        DUM,CLR;
NA1          :NA220LH        NA26O,CCK,NA1O;
NA10         :NA210LH        INV7O,F5Q,NA10O;
NA11         :NA210LH        INV7O,F5QZ,NA11O;
NA12         :NA210LH        INV7O,F6Q,NA12O;
NA13         :NA210LH        INV7O,F6QZ,NA13O;
NA14         :NA210LH        INV7O,F7Q,NA14O;
NA15         :NA210LH        INV7O,F7QZ,NA15O;
NA16         :NA210LH        F8Q,INV7O,NA16O;
NA17         :NA210LH        INV7O,F8QZ,NA17O;
NA18         :NA420LH        FFHQ,NO4O,NO3O,FFQA,RCOZ;
NA19         :NA210LH        NA1O,FFAQ,NA19O;
NA2          :NA210LH        INV7O,F1Q,NA2O;
NA20         :NA310LH        NA1O,FFQA,FFBQ,NA20O;
NA21         :NA410LH        NA1O,FFAQ,FFBQ,FFCQ,NA21O;
NA22         :NA310LH        NA1O,FFAQ,NO3O,NA22O;
NA23         :NA410LH        NA1O,FFAQ,NO3O,FFEQ,NA23O;
NA24         :NA510LH        NA1O,FFAQ,NO3O,FFEQ,FFFQ,NA24O;
NA25         :NA410LH        NA1O,FFAQ,NO3O,NO4O,NA25O;
NA26         :NA310LH        NA1O,INV2O,CCKENZ,NA26O;
NA27         :NA210LH        RCK,NA28O,NA27O;
NA28         :NA210LH        RCKENZ,NA27O,NA28O;
NA3          :NA210LH        INV7O,F1QZ,NA3O;
NA4          :NA210LH        INV7O,F2Q,NA4O;
NA5          :NA210LH        INV7O,F2QZ,NA5O;
NA6          :NA210LH        INV7O,F3Q,NA6O;
NA7          :NA210LH        INV7O,F3QZ,NA7O;
NA8          :NA210LH        F4Q,INV7O,NA8O;
NA9          :NA210LH        INV7O,F4QZ,NA9O;
NO1          :OR210LH        INV1O,G1,NO1O;
NO3          :NO310LH        FFBQZ,FFCQZ,FFDQZ,NO3O;
NO4          :NO310LH        FFEQZ,FFFQZ,FFGQZ,NO4O;
```


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HDL FILE (Continued)

```
STRUCTURE (Continued)
FF14          :R2406LH        CLR,A,B,C,D,RCFQZ,F1Q,F1QZ,F2Q,F2QZ,F3Q,F3QZ,F4Q,F4QZ;
FF58          :R2406LH        CLR,E,F,G,H,RCFQZ,F5Q,F5QZ,F6Q,F6QZ,F7Q,F7QZ,F8Q,F8QZ;
END S593XLH;
```

count definition

These counters are unidirectional with respect to count operation. Inverting the output levels will produce a down-count sequence. Bidirectional counters are available in software macros or can be constructed using the 'ASC2405 through 'ASC2407 4-bit predesigned registers.

designing for testability

Designs employing storage or bistable elements, especially long counters (ripple or synchronous), should consider testability of the design in its final form. The need to preset or clear and read intermediate stages of these elements should be assessed throughout the development of custom logic circuits, with these considerations extended to the end-equipment application with respect to maintainability. Simple actions on the part of the ASIC designer can result in considerable cost savings, allowing the expense of IC testing, system testing, and system maintenance to be reduced significantly.

power-up-clear/preset

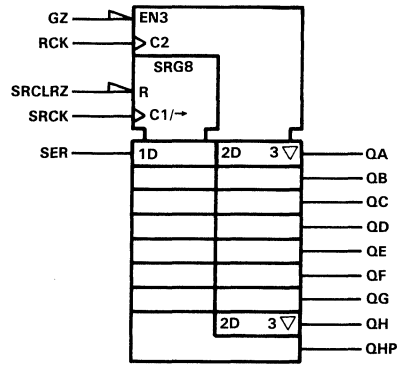
Standard cell storage elements containing the capability to be asynchronously either preset or cleared may be connected to the SN54ASC2320 or SN74ASC2320 power-up clear cell to achieve system initialization. Access to the clear inputs from other system signals in conjunction with the power-up clear can be accomplished with an AND gate.

D2939, AUGUST 1986

SystemCell™ 2-μm SOFTWARE MACRO CELL

- 8-Bit Serial-In, Parallel-Out Shift Registers with Output Storage
- Buffered Clear and Output-Enable Inputs
- Shift Register has Direct Clear
- Embedded Clock Drivers Provide Clock Buffering
- Dependable Texas Instruments Quality and Reliability

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The SN54ASC595 and SN74ASC595 are standard-cell software macros implementing synchronous 8-bit parallel-out shift registers with output storage registers. The 8-bit configuration provides the custom IC designer a multifunction register to embed in ASICs in its most efficient form. The 8-bit length simplifies construction of large registers. The 'ASC595 implements a shift sequence identical with that performed by packaged 'HC595 and 'LS595 registers.

These macros each contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for both the shift register and the storage register. The shift register has a direct-overriding clear, serial input, and serial output pins for cascading. Both the shift register and storage register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the shift-register state will always be one clock pulse ahead of the storage register. The 'ASC595 is implemented with the standard cell functions indicated. The HDL netlist label for this software macro is shown on the last line of the following table:

CELL NAME	RELATIVE CELL AREA TO NA210LH	NO. USED	TOTAL RELATIVE CELL AREA	TOTAL C_{pd}‡ (pF)	MAXIMUM I_{CC} (nA)	
					SN54ASC'	SN74ASC'
IV110LH	0.75	1	0.75	0.44	105	6.32
IV120LH	1	2	2	1.6	262	15.70
R2401LH	25.25	2	50.5	20.6	6142	370
R2407LH	26.25	2	52.5	22	6062	384
TO010LH		1		—	177	10.6
TOTALS		8	105.75	44.64	12748	787
Label: S595LH SER,SRCK,SRCLRZ,RCK,GZ,QA,QB,QC,QD,QE,QF,QG,QH,QHP;						

‡The equivalent power dissipation capacitance does not include interconnect capacitance.

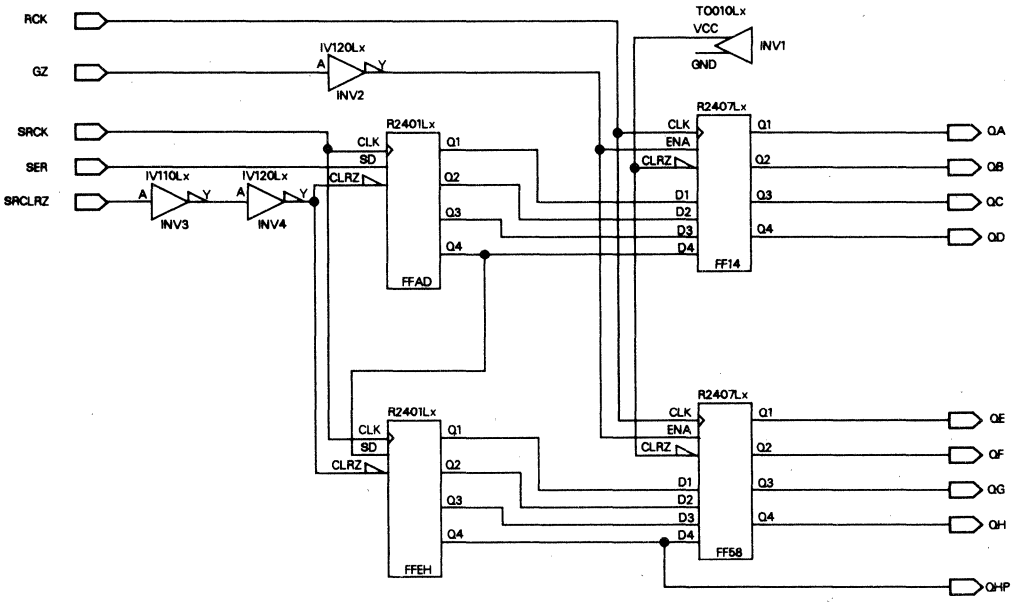
The SN54ASC595 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC595 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

SHIFT REGISTER							OUTPUT REGISTER				
INPUTS			OUTPUTS				INPUTS		OUTPUTS		
SRCLRZ	SRCK	SER	sQA	sQB . . .	sQH	sQHP	RCK	GZ	QA	QB . . .	QH
X	X	X	X	X	X	X	X	H	Z	Z	Z
X	X	X	X	X	X	X	L	L	QA_0	QB_0	QH_0
L	X	X	L	L	L	L	↑	L	L	L	L
H	↑	H	H	sQA_n	sQG_n	sQG_n	L	L	rQA_0	rQB_0	rQH_0
H	↑	L	L	sQA_n	sQG_n	sQG_n	L	L	rQA_0	rQB_0	rQH_0
H	↑	H	H	sQA_n	sQG_n	sQG_n	↑	L	sQA	sQB	sQH
H	↑	L	L	sQA_n	sQG_n	sQG_n	↑	L	sQA	sQB	sQH
H	L	X	sQA_0	sQB_0	sQH_0	sQH_0	↑	L	sQA	sQB	sQH

H = high level (steady state)
L = low level (steady state)
sQ = shift register output,
x = irrelevant (any input, including transitions)
↑ = transition from low to high level.
QA_0, QB_0, QH_0 = the level of QA, QB, or QH, respectively, before the indicated steady-state input conditions were established.
QA_n, QG_n = the level of QA or QG before the most-recent ↑ transition of the clock; indicates a one-bit shift.

logic diagram



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absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements, made during pre-layout simulation, produce workstation output used to identify and resolve each specific timing need.

electrical characteristics

PARAMETER		TEST CONDITIONS	SN54ASC595		SN74ASC595		UNIT
			TYP	MAX	TYP	MAX	
V_T Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC} Supply current		V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		12748		787	nA
C_i Input capacitance	GZ	V_{CC} = 5 V, T_A = 25°C	0.24		0.24		pF
	RCK,SRCK		0.48		0.48		
	SRCLRZ		0.12		0.12		
	SER		0.13		0.13		
C_{pd} Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C, t_r = t_f = 3 ns,	44.64		44.64		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Notes 1 and 2)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC595			SN74ASC595			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{pd}	SRCK↑	QHP	C_L = 0		5.5	11.3		5.5	10.4	ns
t_{pd}	RCK↑	Qn			5.5	11.6		5.5	10.6	ns
t_{PHL}	SRCLRZ	QHP			3.6	7		3.6	6.6	ns
t_{en}	GZ↓	Qn			3.1	5.6		3.1	4.8	ns
Δt_{pd}	Any	Qn		0.6	1.7	4.6	0.6	1.7	4.2	ns/pF
Δt_{en}	GZ↓	Qn		0.8	1.7	4.8	0.8	1.7	4.3	ns/pF

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{pd} ≡ propagation delay time, low-to-high-level or high-to-low-level output
t_{PHL} ≡ propagation delay time, high-to-low level output
t_{en} ≡ enable time, high-impedance state to high- or low-level output
Δt_{pd} ≡ change in t_{pd} with load capacitance
Δt_{en} ≡ change in t_{en} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTES: 1. These switching characteristics are simulations of the software macro cell using interconnect capacitance values for an array design having 2,000 gates. Actual performance can be evaluated at post-layout simulation.
2. Enable and delta-enable times are measured using the conditions specified for the 'ASC2407.

DESIGN CONSIDERATIONS

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

The HDL for this software macro is included as a part of the library supplied for supported engineering workstations so that a single label can be developed to apply the macro as needed. The following printout of the HDL block definition is furnished for reference.

HDL FILE

```
BLOCK S595LH;
SER         @INPUT;
SRCK        @INPUT;
SRCLRZ      @INPUT;
RCK         @INPUT;
GZ          @INPUT;
QA          @OUTPUT;
QB          @OUTPUT;
QC          @OUTPUT;
QD          @OUTPUT;
QE          @OUTPUT
QF          @OUTPUT;
QG          @OUTPUT;
QH          @OUTPUT;
QHP         @OUTPUT;

STRUCTURE
INV1        :TO010LH        DUM,INV1O;
INV2        :IV120LH        GZ,INV2O;
INV3        :IV110LH        SRCLRZ,INV3O;
INV4        :IV120LH        INV3O,INV4O;
FF14        :R2407LH        INV1O,FFAQ,FFBQ,FFCQ,FFDQ,RCK,INV2O,QA,QB,QC,QD;
FF58        :R2407LH        INV1O,FFEQ,FFFQ,FFGQ,QHP,RCK,INV2O,QE,QF,QG,QH;
FFAD        :R2401LH        INV4O,SER,SRCK,FFAQ,FFBQ,FFCQ,FFDQ;
FFEH        :R2401LH        INV4O,FFDQ,SRCK,FFEQ,FFFQ,FFGQ,QHP;
END S595LH;
```

shift defintion

These registers are unidirectional with respect to shift operations and the relationship for shifting left or right is defined by the IC designer. Bidirectional registers are available in software macros or can be constructed using the 'ASC2405 through 'ASC2407 4-bit predesigned registers.

designing for testability

Designs employing storage or bistable elements, especially long registers (ripple or synchronous), should consider testability of the design in its final form. The need to preset or clear and to read intermediate stages of these elements should be assessed throughout the development of custom logic circuits, with these considerations extended to the end-equipment application with respect to maintainability. Simple actions on the part of the ASIC designer can result in considerable cost savings, allowing the expense of IC testing, system testing, and system maintenance to be reduced significantly.

power-up-clear/preset

Standard cell storage elements containing the capability to be asynchronously preset or cleared may be connected to the SN54ASC2320 or SN74ASC2320 power-up clear cell to achieve system initialization. Control of the clear or preset inputs from other system signal in conjunction with the power-up clear can be accomplished with an AND gate.

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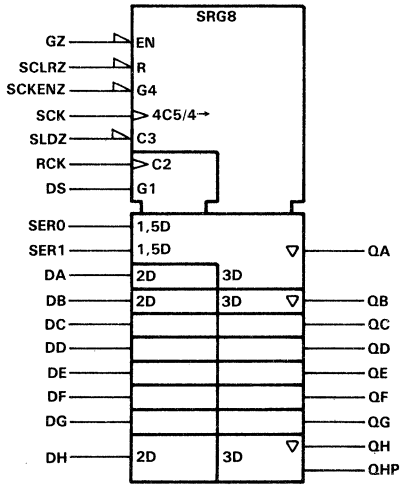
D2939, AUGUST 1986

SystemCell™ 2-μm SOFTWARE MACRO CELL

- 8-Bit Serial-In, Parallel-Out Shift Registers with Input Storage
- Buffered Clear and Output-Enable Inputs
- Shift Register Has Direct Clear
- Embedded Clock Drivers Provide Clock Buffering
- Dependable Texas Instruments Quality and Reliability

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The SN54ASC598X and SN74ASC598X are standard-cell software macros implementing 8-bit parallel-out shift registers with input storage registers. The 8-bit configuration provides the custom IC designer a multifunction register to embed in ASICs in its most efficient form. The 8-bit length simplifies construction of large registers. The 'ASC598X implements a count sequence identical with that performed by packaged 'HC598 and 'LS598 registers.

These macros each contain an 8-bit serial-in, parallel-out shift register fed by an 8-bit D-type input register. The shift register has parallel 3-state outputs. Separate clocks are provided for the shift register and the input register. The 'ASC598X is implemented with the standard cell functions indicated. The HDL netlist label for this software macro is shown on the last line of the following table:

CELL NAME	RELATIVE CELL AREA TO NA210LH	NO. USED	TOTAL RELATIVE CELL AREA	TOTAL C_{pd}‡ (pF)	MAXIMUM I_{CC} (nA)	
					SN54ASC'	SN74ASC'
AN210LH	1.5	10	15	9	1940	116.0
DFB20LH	7.7	8	61.6	30.08	7472	448
IV110LH	0.75	3	2.25	1.32	315	18.96
IV120LH	1	4	4	3.2	524	31.4
IV140LH	1.5	1	1.5	1.61	190	11.4
IV212LH	1.5	8	12	4	1440	86.4
NA210LH	1	18	18	9.18	2358	141.12
OR210LH	1.5	1	1.5	0.86	185	11.1
R2406LH	41	2	50.5	23.38	5862	352
TO010LH	–	1	–	–	177	10.6
TOTALS		56	166.35	82.63	20463	1227
Label: S598XLH DA,DB,DC,DD,DE,DF,DG,DH,RCK,SCK,SCKENZ,SLDZ,SCLRZ,SER0,SER1,DS,GZ,QA, QB,QC,QD,QE,QF,QG,QH,QHP;						

‡The equivalent power dissipation capacitance does not include interconnect capacitance.

The shift register has a direct overriding clear, multiplexed dual serial inputs, and dual serial outputs to simplify cascading. Both the shift register and input register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the shift-register output will be half or double the previous value of the storage register. The shift register has a clock enable associated with internal circuitry that prevents it from triggering the clock.

The SN54ASC598X is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC598X is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

INPUT REGISTER					SHIFT REGISTER											
					INPUTS								OUTPUTS			
RCK	INPUTS		OUTPUTS		SCLRZ	GZ	CLOCK		LOAD	SERIAL						
	DA...DH		RA...RH				SCKENZ	SCK	SLDZ	DS	SER0	SER1	QA	QB...QH		QHP
X	X	X	X	X	X	H	X	X	X	X	X	X	Z	Z	Z	QH
X	X	X	X	X	L	L	X	X	X	X	X	X	L	L	L	L
↑	a	h	a	h	H	L	H	X	X	X	X	X	QA_0	QB_0	QH_0	QH_0
L	X	X	RA_0	RH_0	H	L	L	↑	L	X	X	X	RA	RB	RH	RH
↑	a	h	a	h	H	L	L	↑	H	L	H	X	H	QA_n	QG_n	QG_n
X	X	X	X	X	H	L	L	↑	H	L	H	X	H	QA_n	QG_n	QG_n
X	X	X	X	X	H	L	L	↑	H	L	L	X	L	QA_n	QG_n	QG_n
X	X	X	X	X	H	L	L	↑	H	H	X	H	H	QA_n	QG_n	QG_n
X	X	X	X	X	H	L	L	↑	H	H	X	L	L	QA_n	QG_n	QG_n
X	X	X	X	X	H	L	X	L	X	X	X	X	QA_0	QB_0	QH_0	QH_0

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

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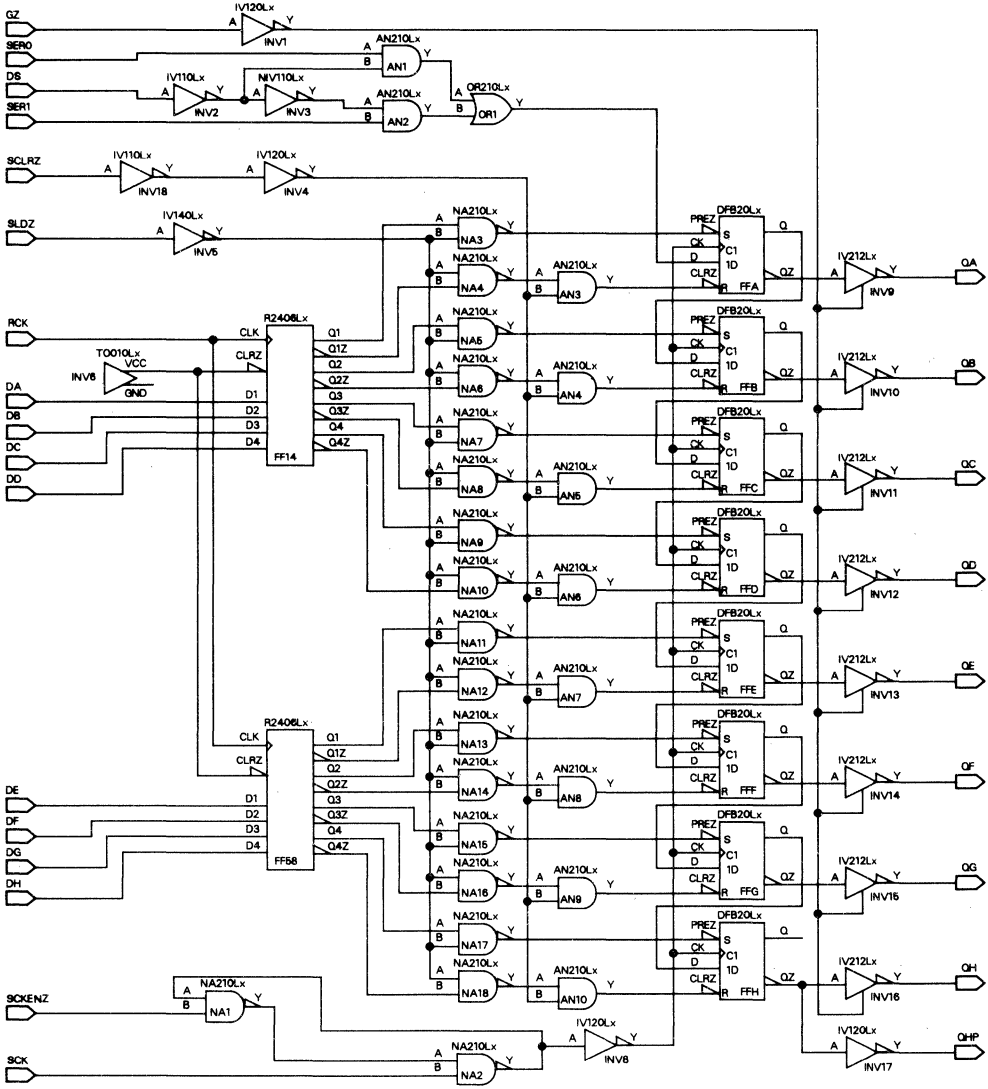
logic diagram



electrical characteristics

PARAMETER			TEST CONDITIONS	SN54ASC598X		SN74ASC598X		UNIT
				TYP	MAX	TYP	MAX	
V_T	Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current		V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		20463		1227	nA
C_i	Input capacitance	Dn, SERn	V_{CC} = 5 V, T_A = 25°C	0.13		0.13		pF
		GZ		0.24		0.24		
		RCK, SLDZ		0.49		0.49		
		Any other		0.12		0.12		
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C, t_r = t_f = 3 ns,	82.63		82.63		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Notes 1 and 2)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC598X			SN74ASC598X			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{pd}	SCK↑	QHP	C_L = 0		9.8	21.9		9.8	19.7	ns
t_{PHL}	SCLRZ	QHP			8	15.5		8	14.2	ns
t_{PHL}	SCLRZ	Qn			9.9	20.8		9.9	18.7	ns
t_{pd}	SCK↑	Qn			9.9	22.2		9.9	20	ns
t_{pd}	SLDZ	QHP			8.1	15.8		8.1	14.5	ns
t_{pd}	SLDZ	Qn			10	21.1		10	19	ns
t_{en}	GZ↑	Qn			3.5	6.7		3.5	6.2	ns
Δt_{pd}	Any	Qn		0.6	1.7	4.6	0.6	1.7	4.2	ns/pF
Δt_{en}	GZ↑	Qn		0.7	1.7	4.8	0.7	1.7	4.4	ns/pF
Δt_{pd}	Any	QHP		0.3	0.5	1.1	0.3	0.5	1	ns/pF

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{pd} ≡ propagation delay time, low-to-high-level or high-to-low-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{en} ≡ enable time, low-to-high-level or high-to-low-level output
Δt_{pd} ≡ change in t_{pd} with load capacitance
Δt_{en} ≡ change in t_{en} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTES: 1. These switching characteristics are simulations of the software macro cell using interconnect capacitance values for an array design having 2,000 gates. Actual performance can be evaluated at post-layout simulation.
2. Enable and delta enable times given apply for the conditions specified for the 'ASC2406 and 'ASC2311 (IV212LH).

DESIGN CONSIDERATIONS

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

The HDL for this software macro is included as a part of the library supplied for supported engineering workstations so that a single label can be developed to apply the macro as needed. The following printout of the HDL block definition is furnished for reference.

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HDL FILE

```
BLOCK S598XLH;
DA          @INPUT;
DB          @INPUT;
DC          @INPUT;
DD          @INPUT;
DE          @INPUT;
DF          @INPUT;
DG          @INPUT;
DH          @INPUT;
RCK         @INPUT;
SCK         @INPUT;
SCKENZ      @INPUT;
SLDZ        @INPUT;
SCLRZ       @INPUT;
SER0        @INPUT;
SER1        @INPUT;
DS          @INPUT;
GZ          @INPUT;
QA          @OUTPUT;
QB          @OUTPUT;
QC          @OUTPUT;
QD          @OUTPUT;
QE          @OUTPUT
QF          @OUTPUT;
QG          @OUTPUT;
QH          @OUTPUT;
QHP         @OUTPUT;

STRUCTURE
AN1         :AN210LH        SER0,INV2O,AN1O;
AN10        :AN210LH        NA18O,INV4O,AN10O;
AN2         :AN210LH        INV3O,SER1,AN2O;
AN3         :AN210LH        NA4O,INV4O,AN4O;
AN4         :AN210LH        NA6O,INV4O,AN4O;
AN5         :AN210LH        NA8O,INV4O,AN5O;
AN6         :AN210LH        NA10O,INV4O,AN6O;
AN7         :AN210LH        NA12O,INV4O,AN7O;
AN8         :AN210LH        NA14O,INV4O,AN8O;
AN9         :AN210LH        NA16O,INV4O,AN9O;
FFA         :DFB20LH        AN3O,NA3O,OR1O,INV8O,FFAQ,FFAQZ;
FFB         :DFB20LH        AN4O,NA5O,FFAQ,INV8O,FFBQ,FFBQZ;
FFC         :DFB20LH        AN5O,NA7O,FFBQ,INV8O,FFCQ,FFCQZ;
FFD         :DFB20LH        AN6O,NA9O,FFCQ,INV8O,FFDQ,FFDQZ;
FFE         :DFB20LH        AN7O,NA10O,FFDQ,INV8O,FFEQ,FFEQZ;
FFF         :DFB20LH        AN8O,NA13O,FFEQ,INV8O,FFFQ,FFFQZ;
FFG         :DFB20LH        AN9O,NA15O,FFFQ,INV8O,FFGQ,FFGQZ;
FFH         :DFB20LH        AN10O,NA17O,FFGQ,INV8O,DUM,FFHQZ;
```

HDL FILE (Continued)

```
STRUCTURE (Continued)
INV1        :IV120LH        GZ,INV1O;
INV1O       :IV212LH        FFBQZ,INV1O,QB;
INV11       :IV212LH        FFCQZ,INV1O,QC;
INV12       :IV212LH        FFDQZ,INV1O,QD;
INV13       :IV212LH        FFEQZ,INV1O,QE;
INV14       :IV212LH        FFFQZ,INV1O,QF;
INV15       :IV212LH        FFGQZ,INV1O,QG;
INV16       :IV212LH        FFHQZ,INV1O,QH;
INV17       :IV210LH        FFHQZ,QHP;
INV18       :IV110LH        SCLRZ,INV18O;
INV2        :IV110LH        DS,INV20;
INV3        :IV110LH        INV20,INV30;
INV4        :IV120LH        INV180,INV40;
INV5        :IV140LH        SLDZ,INV5O;
INV6        :TO010LH        DUM,INV60;
INV8        :IV120LH        NA20,INV80;
INV9        :IV212LH        FFAQZ,INV1O,QA;
NA1         :NA210LH        NA2O,SCKENZ,NA1O;
NA10        :NA210LH        INV5O,FF4QZ,NA10O;
NA11        :NA210LH        FF5Q,INV5O,NA11O;
NA12        :NA210LH        INV5O,FF5QZ,NA12O;
NA13        :NA210LH        FF6Q,INV5O,NA13O;
NA14        :NA210LH        INV5O,FF6QZ,NA14O;
NA15        :NA210LH        FF7Q,INV5O,NA15O;
NA16        :NA210LH        INV5O,FF7QZ,NA16O;
NA17        :NA210LH        FF8Q,INV5O,NA17O;
NA18        :NA210LH        INV5O,FF8QZ,NA18O;
NA2         :NA210LH        NA1O,SCK,NA2O;
NA3         :NA210LH        FF1Q,INV5O,NA3O;
NA4         :NA210LH        INV5O,FF1QZ,NA4O;
NA5         :NA210LH        FF2Q,INV5O,NA5O;
NA6         :NA210LH        INV5O,FF2QZ,NA6O;
NA7         :NA210LH        FF3Q,INV5O,NA7O;
NA8         :NA210LH        INV5O,FF3QZ,NA8O;
NA9         :NA210LH        FF4Q,INV5O,NA9O;
OR1         :OR210LH        AN1O,AN2O,OR1O;
FF14        :R2406LH        INV6O,DA,DB,DC,DD,RCK,FF1Q,FF1QZ,FF2Q,FF2QZ,FF3Q,
                            FF3QZ,FF4Q,FF4QZ;
FF58        :R2406LH        INV6O,DE,DF,DG,DH,RCK,FF5Q,FF5QZ,FF6Q,FF6QZ,FF7Q,
                            FF7QZ,FF8Q,FF8QZ;

END S598XLH;
```


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shift definition

These registers are unidirectional with respect to shift operations and the relationship for shifting left or right is defined by the IC designer. Bidirectional registers are available in software macros or can be constructed using the 'ASC2405 through 'ASC2407 4-bit predesigned registers. Additional single bits can be achieved with flip-flops offered in TI's standard cell family.

designing for testability

Designs employing storage or bistable elements, especially long counters (ripple or synchronous), should consider testability of the design in its final form. The need to preset or clear and read intermediate stages of these elements should be assessed throughout the development of custom logic circuits, with these considerations extended to the end-equipment application with respect to maintainability. Simple actions on the part of the ASIC designer can result in considerable cost savings, allowing the expense of IC testing, system testing, and system maintenance to be reduced significantly.

power-up-clear/preset

Standard cell storage elements containing the capability to be asynchronously either preset or cleared may be connected to the SN54ASC2320 or SN74ASC2320 power-up clear cell to achieve system initialization. Control of the clear or preset inputs from another system signal in conjunction with the power-up clear can be achieved with an AND gate.

D2939, AUGUST 1986

SystemCell™ 2-μm SOFTWARE MACRO CELL

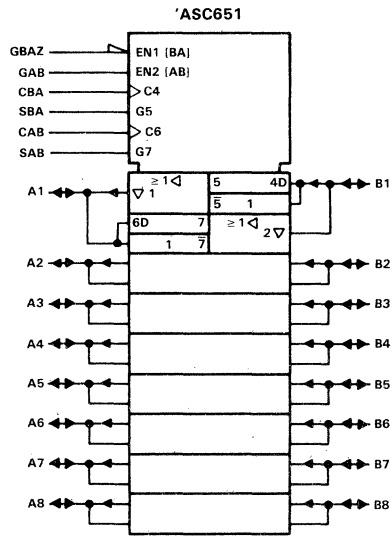
- **Independent Registers and Enables for A and B Buses**
- **Multiplexed Real-Time and Stored Data**
- **Choice of Data Paths:**
  'ASC651 is Inverting
  'ASC652 is Noninverting
- **Positive Edge-Triggered Clocking**
- **Embedded Clock Drivers Provide Clock Buffering**

description

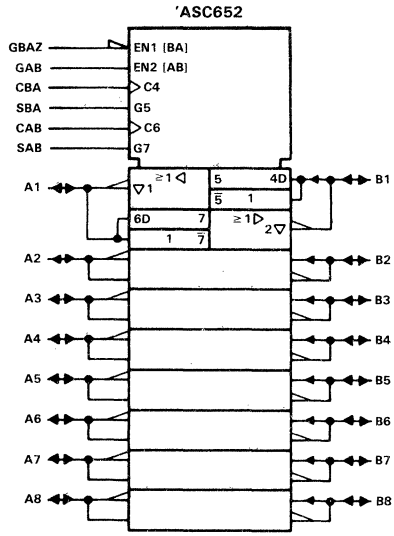
The SN54ASC651, SN54ASC652, SN74ASC651, and SN74ASC652 are standard-cell software macros that implement 8-bit parallel-in/parallel-out bidirectional, universal transceiver registers. The 8-bit configuration provides the custom IC designer a register to embed in ASICs in its most efficient form. The 8-bit length simplifies construction of large registers. The 'ASC651 and 'ASC652 implement an 8-bit port control sequence identical with that performed by packaged 'HC651, 'HC652, and 'LS651, 'LS652 8-bit transceivers.

logic symbols†

'ASC651



'ASC652



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

4 Data Sheets

These bidirectional transceivers are designed to incorporate virtually all of the features a system designer may want in a transceiver. The circuit features parallel inputs, parallel outputs, direction control, and source-control inputs. The 'ASC651 is implemented with the standard cell functions indicated. The HDL netlist label for this software macro is shown on the last line of the following table:

CELL NAME	RELATIVE CELL AREA TO NA210LH	NO. USED	TOTAL RELATIVE CELL AREA	TOTAL C_{pd}† (pF)	MAXIMUM I_{CC} (nA)	
					SN54ASC'	SN74ASC'
IV110LH	0.75	1	0.75	0.44	105	6.32
IV140LH	1.5	6	9	9.66	1140	68.4
IV222LH	2	16	32	15.68	3888	233.6
NA210LH	1	48	48	24.48	6288	376.32
R2405LH	23.25	4	93	40.8	10588	636
TO010LH	1.5	1	1.5	–	177	10.6
TOTALS 'ASC651		76	184.25	91.06	22186	1332
IV110LH	0.75	17	12.75	7.48	1785	107.44
IV140LH	1.5	6	9	9.66	1140	68.4
IV222LH	2	16	32	15.68	3888	233.6
NA210LH	1	48	48	24.48	6288	376.32
R2406LH	26.25	4	105	46.8	11724	704
TO010LH	1.5	1	1.5	–	177	10.6
TOTALS 'ASC652		92	208.25	104.1	25002	1501
Label: S651LH or S652LH GBAZ,GAB,SBA,SAB,CBA,CAB,A1,A2,A3,A4,A5,A6,A7,A8,B1,B2,B3, B4,B5,B6,B7,B8;						

†The equivalent power dissipation capacitance does not include interconnect capacitance.

The 'ASC651 and 'ASC652 consist of bus interface circuits, D-type registers, and control circuitry arranged for multiplexed transmission of data directly to or from an internal data bus or from the embedded storage registers. Enable GAB and GBAZ are provided to control the transceiver functions. SAB and SBA control inputs are provided to select whether real-time or stored data are transferred. A low input level selects real time data, and a high selects stored data. The examples on the following page demonstrates the four fundamental bus-management functions that can be performed with the 'ASC651 and ASC652.

Data on the A or B data bus, or both, can be stored in the internal D registers by low-to-high transitions at the appropriate clock inputs (CAB and CBA) regardless of the select or enable control inputs. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type registers by simultaneously enabling GAB and GBAZ. In this configuration each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain as its last state.

The SN54ASC651 and SN54ASC652 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC651 and SN74ASC652 are characterized for operation from −40°C to 85°C.

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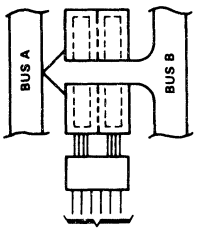
FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION	
GAB	GBAZ	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	'ASC651	'ASC652
L	H	H or L	H or L	X	X	Input	Input	Isolation	Isolation
L	H	↑	↑	X	X			Store A and B Data	Store A and B Data
X	H	↑	H or L	X	X	Input	Not specified	Store A, Hold B	Store A, Hold B
H	H	↑	↑	X	X	Input	Output	Store A in both registers	Store A in both registers
L	X	H or L	↑	X	X	Not specified	Input	Hold A, Store B	Hold A, Store B
L	L	↑	↑	X	X	Output	Input	Store B in both registers	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-Time $\overline{B}$ Data to A Bus	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Stored $\overline{B}$ Data to A Bus	Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time $\overline{A}$ Data to B Bus	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored $\overline{A}$ Data to B Bus	Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{A}$ Data to B Bus and Stored $\overline{B}$ Data to A Bus	Stored A Data to B Bus and Stored B Data to A Bus

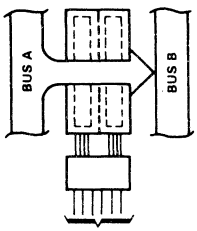
† The data output functions may be enabled or disabled by various signals at the GAB and GBAZ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

typical bus management functions



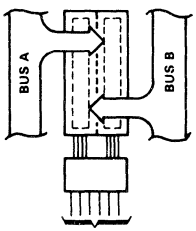
GAB	GBAZ	CAB	CBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER BUS B TO BUS A



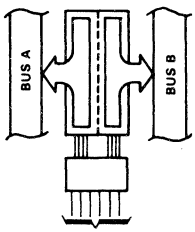
GAB	GBAZ	CAB	CBA	SAB	SBA
H	H	X	X	L	X

REAL-TIME TRANSFER BUS A TO BUS B



GAB	GBAZ	CAB	CBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

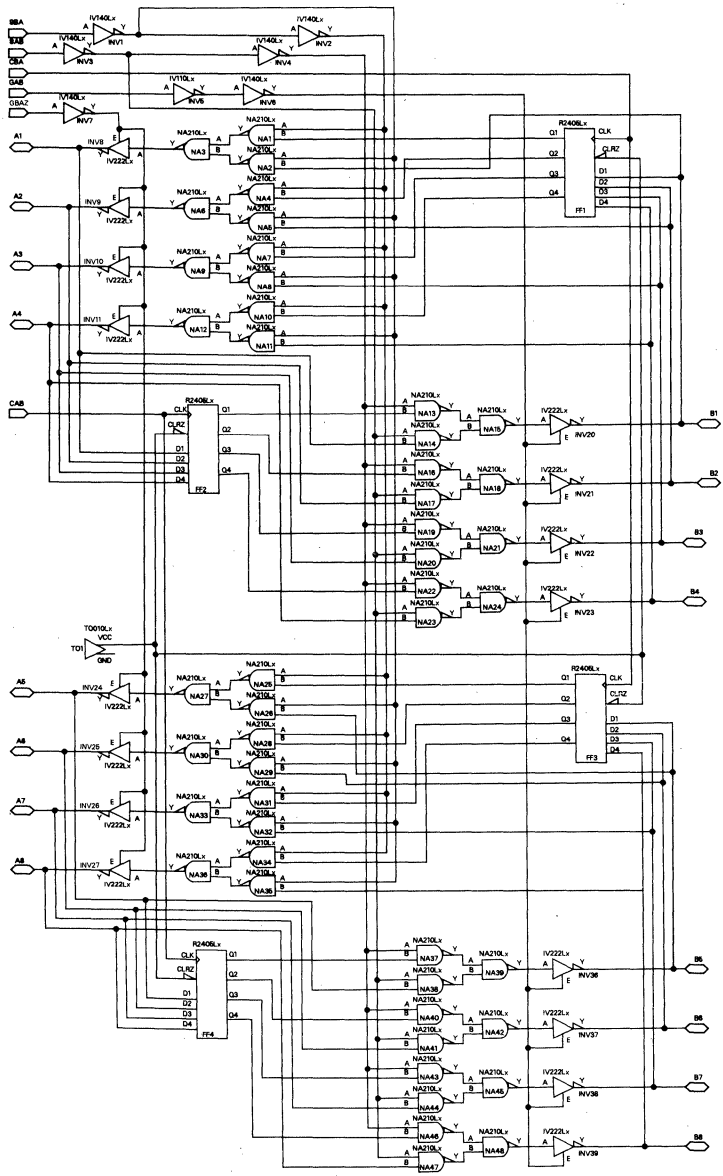
STORAGE FROM A AND/OR B



GAB	GBAZ	CAB	CBA	SAB	SBA
H	L	H or L	H or L	H	H

TRANSFER STORED DATA TO A AND/OR B

logic diagram 'ASC651



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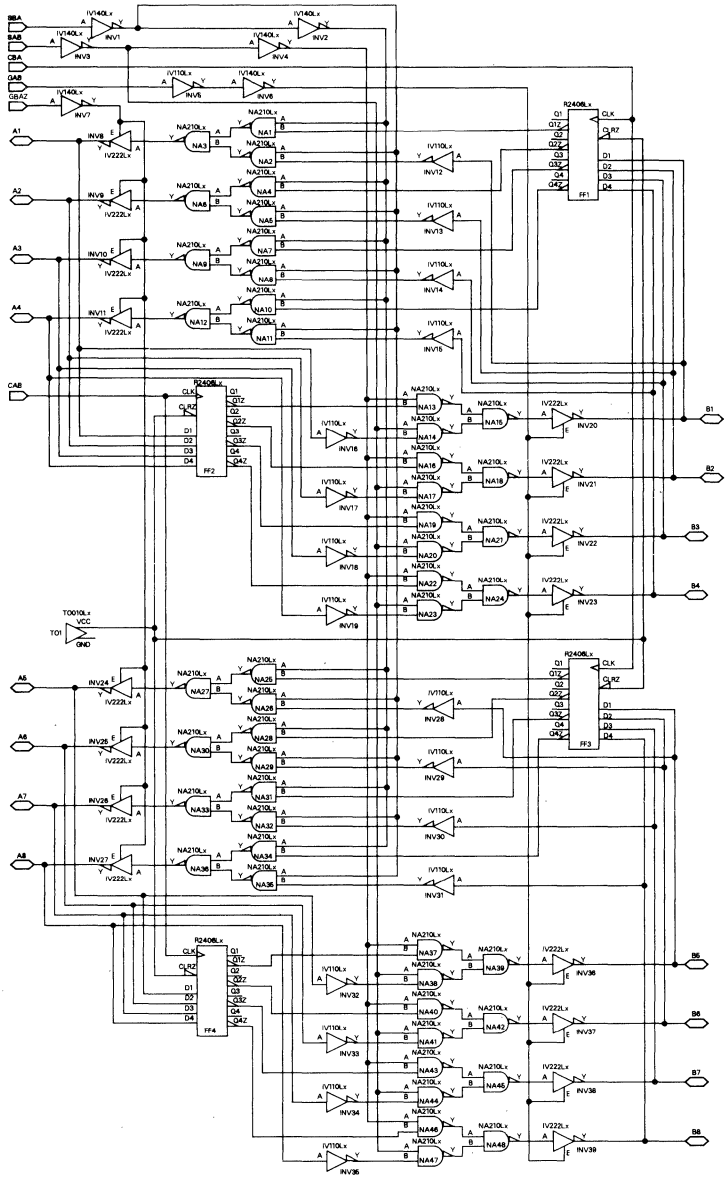
logic diagram 'ASC652



absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

electrical characteristics

PARAMETER			TEST CONDITIONS		SN54ASC651 SN54ASC652		SN74ASC651 SN74ASC652		UNIT
					TYP	MAX	TYP	MAX	
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current	S651LH	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0,			22186		1332	nA
		S652LH	T_A = MIN to MAX			25002		1501	
C_i	Input capacitance	An or Bn	V_{CC} = 5 V,	T_A = 25°C	0.58		0.58		pF
		CAB, CBA			0.48		0.48		
		GAB			0.12		0.12		
		GBAZ, SAB, SBA			0.49		0.49		
C_o	Output capacitance		V_{CC} = 5 V,	T_A = 25°C	0.58		0.58		pF
C_{pd}	Equivalent power dissipation capacitance†	S651LH	V_{CC} = 5 V,	t_r = t_f = 3 ns,	91.06		91.06		pF
		S652LH	T_A = 25°C		104.1		104.1		

† The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Notes 1 and 2)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC651 SN54ASC652			SN74ASC651 SN74ASC652			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{pd}	CAB, CBA	A, B	C_L = 0		10.4	20.9		10.4	19.1	ns
t_{pd}	A, B	B, A			5.4	10.1		5.4	9.4	
t_{pd}	SAB, SBA	A, B			6.6	12.3		6.6	11.8	ns
t_{en}	GAB, GBAZ	A, B			4.7	8.7		4.7	8.3	
Δt_{pd}	Any	Any		0.3	0.9	2.3	0.4	0.9	2.1	ns/pF
Δt_{en}	GAB, GBAZ	Any		0.4	0.9	2.3	0.5	0.9	2.1	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{pd} ≡ propagation delay time, low-to-high-level or high-to-low-level output
t_{en} ≡ enable time, high-impedance state to low- or high-logic-level output
Δt_{pd} ≡ change in t_{pd} with load capacitance
Δt_{en} ≡ change in t_{en} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTES: 1. These switching characteristics are simulations of the software macro cell using interconnect capacitance values for an array design having 2,000 gates. Post-layout simulation uses actual interconnect capacitance values.
2. Enable and delta-enable times are measured using the conditions specified for the SN54ASC2311 and SN74ASC2311 (IV222LH).

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DESIGN CONSIDERATIONS

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

The HDL for this software macro is included as a part of the library supplied for supported engineering workstations so that a single label can be developed to apply the macro as needed. The following printout of the HDL block definition is furnished for reference.

HDL FILE

```
BLOCK S651LH;
GBAZ        @INPUT;
GAB         @INPUT;
SBA         @INPUT;
SAB         @INPUT;
CBA         @INPUT;
CAB         @INPUT;
A1          @INOUT;
A2          @INOUT;
A3          @INOUT;
A4          @INOUT
A5          @INOUT;
A6          @INOUT;
A7          @INOUT;
A8          @INOUT;
B1          @INOUT;
B2          @INOUT;
B3          @INOUT;
B4          @INOUT;
B5          @INOUT;
B6          @INOUT;
B7          @INOUT;
B8          @INOUT;

STRUCTURE
INV1        :IV140LH        SBA,SBAZ;
INV10       :IV222LH        SNA9,GBA,A3;
INV11       :IV222LH        SNA12,GBA,A4;
INV2        :IV140LH        SBAZ,SBA1;
INV20       :IV222LH        SNA15,GAB1,B1;
INV21       :IV222LH        SNA18,GAB1,B2;
INV22       :IV222LH        SNA21,GAB1,B3;
INV23       :IV222LH        SNA24,GAB1,B4;
INV24       :IV222LH        SNA27,GBA,A5;
INV25       :IV222LH        SNA30,GBA,A6;
INV26       :IV222LH        SNA33,GBA,A7;
INV27       :IV222LH        SNA36,GBA,A8;
INV3        :IV140LH        SAB,SABZ;
INV36       :IV222LH        SNA39,GAB1,B5;
INV37       :IV222LH        SNA42,GAB1,B6;
INV38       :IV222LH        SNA45,GAB1,B7;
INV39       :IV222LH        SNA48,GAB1,B8;
```

HDL FILE (Continued)

```
STRUCTURE (Continued)
INV4        :IV140LH        SABZ,SAB1;
INV5        :IV110LH        GAB,GABZ;
INV6        :IV140LH        GABZ,GAB1;
INV7        :IV140LH        GBAZ,GBA;
INV8        :IV222LH        SNA3,GBA,A1;
INV9        :IV222LH        SNA6,GBA,A2;
NA1         :NA210LH        SBA1,FF1A,SNA1;
NA10        :NA210LH        SBA1,FF1D,SNA10;
NA11        :NA210LH        SBAZ,B4,SNA11;
NA12        :NA210LH        SNA10,SNA11,SNA12;
NA13        :NA210LH        SAB1,FF2A,SNA13;
NA14        :NA210LH        SABZ,A1,SNA14;
NA15        :NA210LH        SNA13,SNA14,SNA15;
NA16        :NA210LH        SAB1,FF2B,SNA16;
NA17        :NA210LH        SABZ,A2,SNA17;
NA18        :NA210LH        SNA16,SNA17,SNA18;
NA19        :NA210LH        SAB1,FF2C,SNA19;
NA2         :NA210LH        SBAZ,B1,SNA2;
NA20        :NA210LH        SABZ,A3,SNA20;
NA21        :NA210LH        SNA19,SNA20,SNA21;
NA22        :NA210LH        SAB1,FF2D,SNA22;
NA23        :NA210LH        SABZ,A4,SNA23;
NA24        :NA210LH        SNA22,SNA23,SNA24;
NA25        :NA210LH        SBA1,FF3A,SNA25;
NA26        :NA210LH        SBAZ,B5,SNA26;
NA27        :NA210LH        SNA25,SNA26,SNA27;
NA28        :NA210LH        SBA1,FF3B,SNA28;
NA29        :NA210LH        SBAZ,B6,SNA29;
NA3         :NA210LH        SNA1,SNA2,SNA3;
NA30        :NA210LH        SNA28,SNA29,SNA30;
NA31        :NA210LH        SBA1,FF3C,SNA31;
NA32        :NA210LH        SBAZ,B7,SNA32;
NA33        :NA210LH        SNA31,SNA32,SNA33;
NA34        :NA210LH        SBA1,FF3D,SNA34;
NA35        :NA210LH        SBAZ,B8,SNA35;
NA36        :NA210LH        SNA34,SNA35,SNA36;
NA37        :NA210LH        SAB1,FF4A,SNA37;
NA38        :NA210LH        SABZ,A5,SNA38;
NA39        :NA210LH        SNA37,SNA38,SNA39;
NA4         :NA210LH        SBA1,FF1B,SNA4;
```

HDL FILE (Continued)

```
    STRUCTURE (Continued)
    NA40        :NA210LH        SAB1,FF4B,SNA40;
    NA41        :NA210LH        SABZ,A6,SNA41;
    NA42        :NA210LH        SNA40,SNA41,SNA42;
    NA43        :NA210LH        SAB1,FF4C,SNA43;
    NA44        :NA210LH        SABZ,A7,SNA44;
    NA45        :NA210LH        SNA43,SNA44,SNA45;
    NA46        :NA210LH        SAB1,FF4D,SNA46;
    NA47        :NA210LH        SABZ,A8,SNA47;
    NA48        :NA210LH        SNA46,SNA47,SNA48;
    NA5         :NA210LH        SBAZ,B2,SNA5;
    NA6         :NA210LH        SNA4,SNA5,SNA6;
    NA7         :NA210LH        SBA1,FF1C,SNA7;
    NA8         :NA210LH        SBAZ,B3,SNA8;
    NA9         :NA210LH        SNA7,SNA8,SNA9;
    TO1         :TO010LH        DUM,STO1:
    FF1         :R2405LH        STO1,B1,B2,B3,B4,CBA,FF1A,FF1B,FF1C,FF1D;
    FF2         :R2405LH        STO1,A1,A2,A3,A4,CAB,FF2A,FF2B,FF2C,FF2D;
    FF3         :R2405LH        STO1,B5,B6,B7,B8,CBA,FF3A,FF3B,FF3C,FF3D;
    FF4         :R2405LH        STO1,A5,A6,A7,A8,CAB,FF4A,FF4B,FF4C,FF4D;
END S651LH

    BLOCK S652LH;
    GBAZ        @INPUT;
    GAB         @INPUT;
    SBA         @INPUT;
    SAB         @INPUT;
    CBA         @INPUT;
    CAB         @INPUT;
    A1          @INOUT;
    A2          @INOUT;
    A3          @INOUT;
    A4          @INOUT
    A5          @INOUT;
    A6          @INOUT;
    A7          @INOUT;
    A8          @INOUT;
    B1          @INOUT;
    B2          @INOUT;
    B3          @INOUT;
    B4          @INOUT;
    B5          @INOUT;
    B6          @INOUT;
    B7          @INOUT;
    B8          @INOUT;
```

HDL FILE (Continued)

```
STRUCTURE (Continued)
INV1        :IV140LH        SBA,SBAZ;
INV10       :IV222LH        SNA9,GBA,A3;
INV11       :IV222LH        SNA12,GBA,A4;
INV12       :IV110LH        B1,SIV12;
INV13       :IV110LH        B2,SIV13;
INV14       :IV110LH        B3,SIV14;
INV15       :IV110LH        B4,SIV15;
INV16       :IV110LH        A1,SIV16;
INV17       :IV110LH        A2,SIV17;
INV18       :IV110LH        A3,SIV18;
INV19       :IV110LH        A4,SIV19;
INV2        :IV140LH        SBAZ,SBA1;
INV20       :IV222LH        SNA15,GAB1,B1;
INV21       :IV222LH        SNA18,GAB1,B2;
INV22       :IV222LH        SNA21,GAB1,B3;
INV23       :IV222LH        SNA24,GAB1,B4;
INV24       :IV222LH        SNA27,GBA,A5;
INV25       :IV222LH        SNA30,GBA,A6;
INV26       :IV222LH        SNA33,GBA,A7;
INV27       :IV222LH        SNA36,GBA,A8;
INV28       :IV110LH        B5,SIV28;
INV29       :IV110LH        B6,SIV29;
INV3        :IV140LH        SAB,SABZ;
INV30       :IV110LH        B7,SIV30;
INV31       :IV110LH        B8,SIV31;
INV32       :IV110LH        A5,SIV32;
INV33       :IV110LH        A6,SIV33;
INV34       :IV110LH        A7,SIV34;
INV35       :IV110LH        A8,SIV35;
INV36       :IV222LH        SNA39,GAB1,B5;
INV37       :IV222LH        SNA42,GAB1,B6;
INV38       :IV222LH        SNA45,GAB1,B7;
INV39       :IV222LH        SNA48,GAB1,B8;
INV4        :IV140LH        SABZ,SAB1;
INV5        :IV110LH        GAB,GABZ;
INV6        :IV140LH        GABZ,GAB1;
INV7        :IV140LH        GBAZ,GBA;
INV8        :IV222LH        SNA3,GBA,A1;
INV9        :IV222LH        SNA6,GBA,A2;
NA1         :NA210LH        SBA1,FF1AZ,SNA1;
NA10        :NA210LH        SBA1,FF1DZ,SNA10;
NA11        :NA210LH        SBAZ,SIV15,SNA11;
NA12        :NA210LH        SNA10,SNA11,SNA12;
NA13        :NA210LH        SAB1,FF2AZ,SNA13;
NA14        :NA210LH        SABZ,SIV16,SNA14;
NA15        :NA210LH        SNA13,SNA14,SNA15;
NA16        :NA210LH        SAB1,FF2BZ,SNA16;
NA17        :NA210LH        SABZ,SIV17,SNA17;
NA18        :NA210LH        SNA16,SNA17,SNA18;
NA19        :NA210LH        SAB1,FF2CZ,SNA19;
```


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HDL FILE (Continued)

```
    STRUCTURE (Continued)
    NA2         :NA210LH        SBAZ,SIV12,SNA2;
    NA20        :NA210LH        SABZ,SIV18,SNA20;
    NA21        :NA210LH        SNA19,SNA20,SNA21;
    NA22        :NA210LH        SAB1,FF2DZ,SNA22;
    NA23        :NA210LH        SABZ,SIV19,SNA23;
    NA24        :NA210LH        SNA22,SNA23,SNA24;
    NA25        :NA210LH        SBA1,FF3AZ,SNA25;
    NA26        :NA210LH        SBAZ,SIV28,SNA26;
    NA27        :NA210LH        SNA25,SNA26,SNA27;
    NA28        :NA210LH        SBA1,FF3BZ,SNA28;
    NA29        :NA210LH        SBAZ,SIV29,SNA29;
    NA3         :NA210LH        SNA1,SNA2,SNA3;
    NA30        :NA210LH        SNA28,SNA29,SNA30;
    NA31        :NA210LH        SBA1,FF3CZ,SNA31;
    NA32        :NA210LH        SBAZ,SIV30,SNA32;
    NA33        :NA210LH        SNA31,SNA32,SNA33;
    NA34        :NA210LH        SBA1,FF3DZ,SNA34;
    NA35        :NA210LH        SBAZ,SIV31,SNA35;
    NA36        :NA210LH        SNA34,SNA35,SNA36;
    NA37        :NA210LH        SAB1,FF4AZ,SNA37;
    NA38        :NA210LH        SABZ,SIV32,SNA38;
    NA39        :NA210LH        SNA37,SNA38,SNA39;
    NA4         :NA210LH        SBA1,FF1BZ,SNA4;
    NA40        :NA210LH        SAB1,FF4BZ,SNA40;
    NA41        :NA210LH        SABZ,SIV33,SNA41;
    NA42        :NA210LH        SNA40,SNA41,SNA42;
    NA43        :NA210LH        SAB1,FF4CZ,SNA43;
    NA44        :NA210LH        SABZ,SIV34,SNA44;
    NA45        :NA210LH        SNA43,SNA44,SNA45;
    NA46        :NA210LH        SAB1,FF4DZ,SNA46;
    NA47        :NA210LH        SABZ,SIV35,SNA47;
    NA48        :NA210LH        SNA46,SNA47,SNA48;
    NA5         :NA210LH        SBAZ,SIV13,SNA5;
    NA6         :NA210LH        SNA4,SNA5,SNA6;
    NA7         :NA210LH        SBA1,FF1CZ,SNA7;
    NA8         :NA210LH        SBAZ,SIV14,SNA8;
    NA9         :NA210LH        SNA7,SNA8,SNA9;
    TO1         :TO010LH        DUM,STO1:
    FF1         :R2406LH        STO1,B1,B2,B3,B4,CBA,DUM,FF1AZ,DUM,FF1BZ,DUM,FF1CZ,
                                DUM,FF1DZ;
    FF2         :R2406LH        STO1,A1,A2,A3,A4,CAB,DUM,FF2AZ,DUM,FF2BZ,DUM,FF2CZ,
                                DUM,FF2DZ;
    FF3         :R2406LH        STO1,B5,B6,B7,B8,CBA,DUM,FF3AZ,DUM,FF3BZ,DUM,FF3CZ,
                                DUM,FF3DZ;
    FF4         :R2406LH        STO1,A5,A6,A7,A8,CAB,DUM,FF4AZ,DUM,FF4BZ,DUM,FF4CZ,
                                DUM,FF4DZ;
END S652LH
```

D2939, AUGUST 1986

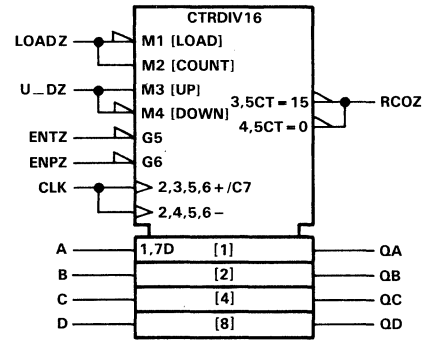
SystemCell™ 2-μm SOFTWARE MACRO CELL

- **Fully Synchronous Operation for Counting and Programming**
- **Internal Look-Ahead for Fast Counting**
- **Carry Output for n-Bit Cascading**
- **Fully Independent Clock Circuit**
- **Buffered Outputs**

description

The SN54ASC669 and SN74ASC669 are standard-cell software macros implementing synchronous 4-bit up-down binary counter elements. The four-bit configuration provides the custom IC designer a fully designed bidirectional counter to embed in ASICs in its most efficient form, and the 4-bit length simplifies construction of large counters. The 'ASC669 implements a count sequence identical with that performed by packaged 'LS669 counters.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

These synchronous presettable counters feature an internal carry look-ahead for cascading in high-speed counting applications. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidentally with each other when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple-clock) counters. A buffered clock input triggers the four master-slave flip-flops on the rising (positive-going) edge of the clock waveform. The 'ASC669 is implemented with the standard cell functions indicated. The HDL netlist label for this software macro is shown on the last line of the following table:

CELL NAME	RELATIVE CELL AREA TO NA210LH	NO. USED	TOTAL RELATIVE CELL AREA	TOTAL C_{pd}† (pF)	MAXIMUM I_{CC} SN54ASC' (nA)	MAXIMUM I_{CC} SN74ASC' (nA)
AN320LH	2	1	2	1.06	221	13.3
AO221LH	2.7	4	10.8	2.36	896	53.6
IV110LH	0.75	7	5.25	3.08	735	44.24
IV120LH	1	3	3	2.4	393	23.55
NA210LH	1	6	6	3.06	786	47.04
NA310LH	1.25	10	12.5	5	1630	97.8
NA410LH	1.5	2	3	1	374	11.4
NA510LH	1.75	2	3.5	1.04	426	25.6
R2406LH	26.25	1	26.25	11.7	2931	176
TO010LH	1.5	1	1.5	–	177	10.6
TOTALS		37	73.75	30.7	8569	504
Label: S669LH D,C,B,A,CLK,U_DZ,ENPZ,ENTZ,LOADZ,QD,QC,QB,QA,RCOZ;						

†The equivalent power dissipation capacitance does not include interconnect capacitance.

description (continued)

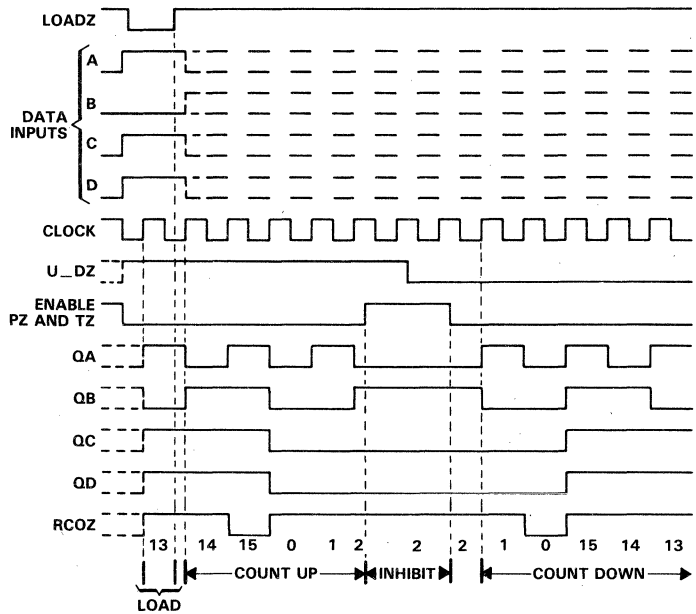
These counters are fully programmable; that is, they may be preset to any number between 0 and 15. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the output to agree with the data inputs after the next clock pulse.

The carry look-ahead circuitry provides for cascading counters in n-bit synchronous applications without additional gating. Instrumental in achieving this are two count-enable inputs and a ripple carry output. Both count-enable inputs (ENPZ and ENTZ) must be low to count. ENPZ enables the local 4-bits and the ENTZ is fed forward to globally extend the enable/disable of previous/next 4-bit cascaded counters. The ripple-carry out RCOZ, when locally and globally enabled, will output a low-level pulse that is used to enable successive stages. Transitions at the ENPZ and ENTZ inputs are allowed regardless of the level of the clock input.

These counters feature a fully independent clock circuit. Changes at control inputs (ENPZ, ENTZ, LOADZ, U_DZ) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enable, disable, load, or count) will be dictated solely by the conditions meeting the setup and hold times.

The SN54ASC669 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC669 is characterized for operation from −40°C to 85°C.

typical load, count, and inhibit sequences



Note 1: This sequence shows the following characteristics:
Load (preset) to binary thirteen
Count up to fourteen, fifteen (maximum), zero, one, and two
Inhibit
Count down to one, zero, (minimum), fifteen, fourteen, and thirteen

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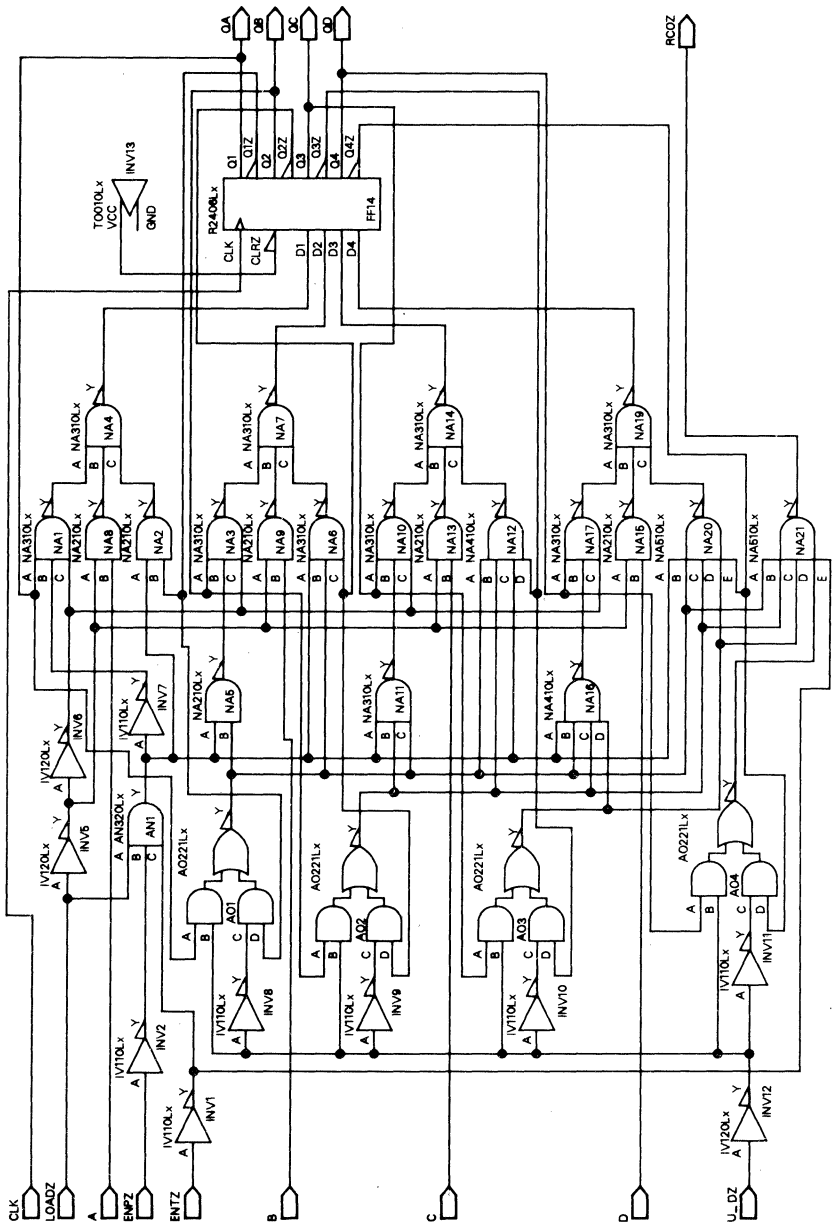
logic diagram



absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of the timing requirements, are made during pre-layout simulation, produce workstation output used to identify and resolve each specific timing need.

electrical characteristics

PARAMETER			TEST CONDITIONS	SN54ASC669		SN74ASC669		UNIT
				TYP	MAX	TYP	MAX	
V_T	Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current		V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		8569		504	nA
C_i	Input capacitance	CLK,LOADZ, and U_DZ	V_{CC} = 5 V, T_A = 25°C	0.24		0.24		pF
		All others		0.12		0.12		
C_{pd}	Equivalent power dissipation capacitance†		V_{CC} = 5 V, t_r = t_f = 3 ns, T_A = 25°C	30.7		30.7		pF

† The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 1)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC669			SN74ASC669			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{pd}	CLK	RCOZ	C_L = 0		10	24.2		10	22	ns
t_{pd}	CLK	Qn			5	10.4		5	9.4	
t_{pd}	ENTZ	RCOZ			3	5.9		3	5.3	ns
t_{pd}	U_DZ	RCOZ			6	14.2		6	13	
Δt_{pd}	Any	Qn		0.2	0.9	2.4	0.3	0.9	2.1	ns/pF
Δt_{pd}	Any	RCOZ		0.5	1.8	5.8	0.5	1.8	5	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{pd} ≡ propagation delay time, low-to-high or high-to-low output
Δt_{pd} ≡ change in t_{pd} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These switching characteristics are simulations of the software macro cell using interconnect capacitance values for an array design having 2,000 gates. Post-layout simulation uses actual interconnect capacitance values.

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DESIGN CONSIDERATIONS

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

The HDL for this software macro is included as a part of the library supplied for supported engineering workstations so that a single label can be developed to apply the macro as needed. The following printout of the HDL block definition is furnished for reference.

HDL FILE

```
BLOCK S669LH;
D           @INPUT;
C           @INPUT;
B           @INPUT;
A           @INPUT;
CLK         @INPUT;
U_DZ        @INPUT;
ENPZ        @INPUT;
ENTZ        @INPUT;
LOADZ       @INPUT;
QD          @OUTPUT;
QC          @OUTPUT;
QB          @OUTPUT;
QA          @OUTPUT;
RCOZ        @OUTPUT;

STRUCTURE
AN1         :AN320LH      LOADZ,INV2O,INV1O,AN1O;
AO12        :AO221LH      QA,INV12O,INV8O,FFAQZ,AO1O;
AO2         :AO221LH      QB,INV12O,INV9O,FFBQZ,AO2O;
AO3         :AO221LH      QC,INV2O,INV10O,FFCQZ,AO3O;
AO4         :AO221LH      QD,INV12O,INV11O,FFDQZ,AO4O;
INV1        :IV110LH      ENTZ,INV1O;
INV10       :IN110LH      INV12O,INV10O;
INV11       :IV110LH      INV12O,INV11O;
INV12       :INV120LH     U_DZ,INV12O;
INV13       :TO010LH      DUM,CLRZ;
INV2        :IV110LH      ENPZ,INV2O;
INV5        :IV120LH      LOADZ,INV5O;
INV6        :IV120LH      INV5O,INV6O;
INV7        :IV110LH      AN1O,INV7O;
INV8        :IV110LH      INV12O,INV8O;
INV9        :IV11OLH      INV12O,INV9O;
NA1         :NA310LH      QA,INV7O,INV6O,NA1O;
NA10        :NA310LH      QC,NA11O,INV6O,NA10O;
NA11        :NA310LH      AN1O,AO2O,AO1O,NA11O;
NA12        :NA410LH      AO1O,AO2O,AN1O,FFCQZ,NA12O;
NA13        :NA210LH      INV5O,C,NA13O;
NA14        :NA310LH      NA10O,NA13O,NA12O,NA14O;
NA15        :NA210LH      INV5O,D,NA15O;
NA16        :NA410LH      AN1O,AO1O,AO2O,AO3O,NA16O;
NA17        :NA31OLH      QD,NA16O,INV6O,NA17O;
```

HDL FILE (Continued)

```
STRUCTURE (Continued)
NA19        :NA310LH        NA17O,NA15O,NA20O,NA19O;
NA2         :NA210LH        AN1O,FFAQZ,NA2O;
NA20        :NA510LH        AN1O,AO1O,AO2O,AO3O,FFDQZ,NA20O;
NA21        :NA510LH        AO1O,AO2O,AO3O,AO4O,INV1O,RCOZ;
NA3         :NA310LH        QB,NA5O,INV6O,NA3O;
NA4         :NA310LH        NA1O,NA8O,NA2O,NA4O;
NA5         :NA210LH        AN1O,AO1O,NA5O;
NA6         :NA310LH        AN1O,AO1O,FFBQZ,NA6O;
NA7         :NA310LH        NA3O,NA9O,NA6O,NA7O;
NA8         :NA210LH        INV5O,A,NA8O;
NA9         :NA210LH        INV5O,B,NA9O;
FF14        :R2406ZLH       CLRZ,NA4O,NA7O,NA14O,NA19O,CLK,QA,FFAQZ,QB,FFBQZ,
                            QC,FFCQZ,QD,FFDQZ;

END S669LH
```

count definition

These counters are bidirectional with respect to count operations and the relationship for counting up or down is defined by the U_DZ input. Unidirectional counters are available in software macros or can be contructed using the 'ASC2405 through 'ASC2407 4-bit predesigned registers. Additional single bits can be achieved with predesigned flip-flops offered in TI's standard cell family.

designing for testability

Designers employing storage or bistable elements, especially long counters (ripple or synchronous), should consider testability of the design in its final form. The need to preset or clear, and read intermediate stages of these elements, should be assessed throughout the development of custom logic circuits with these considerations extended to the end equipment application with respect to maintainability. Simple actions on the part of the ASIC designer can result in considerable costs savings as the expense of IC testing, system testing, and system maintenance can be reduced significantly.

power-up-clear/preset

Standard cell storage elements containing the capability to be asynchronously either preset or cleared may be connected to the SN54ASC2320 or SN74ASC2320 power-up clear cell to achieve system initialization. Access to the clear inputs from other system signals in conjunction with the power-up clear can be facilitated with an AND gate.

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D2939, AUGUST 1986

SystemCell™ 2-μm SOFTWARE MACRO CELL

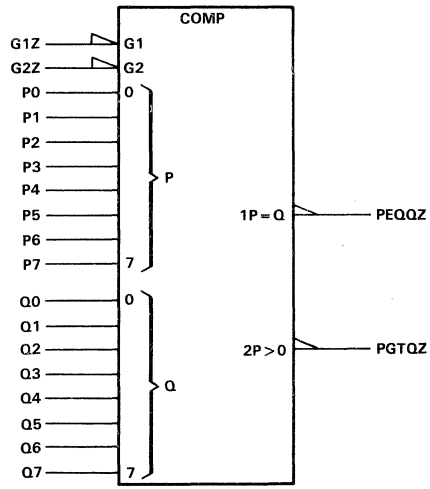
- **Performs Magnitude Comparison of Binary, BCD, and Monotonic Codes**
- **Weighted Cascaded Inputs Accomodate Both Serial and Parallel Expansion**
- **Dependable Texas Instruments Quality and Reliability**

description

The SN54ASC686 and SN74ASC686 are standard-cell software macros implementing 8-bit expandable magnitude comparators. The 8-bit configuration provides the custom IC designer a magnitude comparator to embed in ASICs in its most efficient form, and the 8 bit width simplifies construction of wider comparators. The 'ASC686 implements a comparison scheme identical with that performed by packaged 'HC686 and 'LS686 comparators.

These 8-bit magnitude comparators perform comparison of straight binary and straight BCD (8-4-2-1), codes. Two fully decoded decisions, P>Q or P = Q, about two eight-bit words (P,Q) are made and are externally available at two outputs that can be decoded with a NAND gate to provide the P<Q decision. These devices are fully expandable to any number of bits. Words of greater length may be compared by connecting comparators in cascade. The PEQQZ and PGTQZ outputs of a stage handling less-significant bits are connected to the corresponding G1Z and G2Z inputs of the next stage handling more-significant bits. The 'ASC686 is implemented with the standard cell functions indicated. The HDL netlist label for this software macro is shown on the last line of the following table:

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

CELL NAME	RELATIVE CELL AREA TO NA210LH	NO. USED	TOTAL RELATIVE CELL AREA	TOTAL C_{pd}‡ (pF)	MAXIMUM I_{CC} SN54ASC' (nA)	MAXIMUM I_{CC} SN74ASC' (nA)
AN210LH	1.5	4	6	3.6	776	46.4
AN310LH	1.75	7	12.25	7.42	1547	93.1
AN410LH	2	6	12	7.08	1536	91.8
EX210LH	2	8	16	8.96	1784	107.2
IV110LH	0.75	13	9.75	5.72	1365	82.16
IV120LH	1	5	5	4	655	39.25
NA210LH	1	4	4	2.04	524	31.36
NA310LH	1.25	3	3.75	1.5	489	29.34
NA410LH	1.5	3	4.5	1.5	561	33.6
NA420LH	2.5	1	2.5	0.96	312	18.7
NO220LH	1.5	1	1.5	0.52	185	11.1
TOTALS		55	77.25	43.3	9734	585
Label: S686LH P0,P1,P2,P3,P4,P5,P6,P7,Q0,Q1,Q2,Q3,Q4,Q5,Q6,Q7,G1Z,G2Z,PEQQZ,PGTQZ;						

‡Does not include interconnect capacitance.

The SN54ASC688 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC688 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

INPUTS			OUTPUTS‡	
DATA	ENABLES†		PEQQZ	PGTQZ
P,Q	G1Z	G2Z		
P=Q	L	X	L	H
P>Q	X	L	H	L
P<Q	X	X	H	H
P=Q	H	X	H	H
P>Q	X	H	H	H
X	H	H	H	H

† G1Z enables PEQQZ, and G2Z enables PGTQZ.
‡ The $\overline{P<Q}$ function can be generated by applying the PEQQZ and PGTQZ outputs to a 2-input NAND gate.

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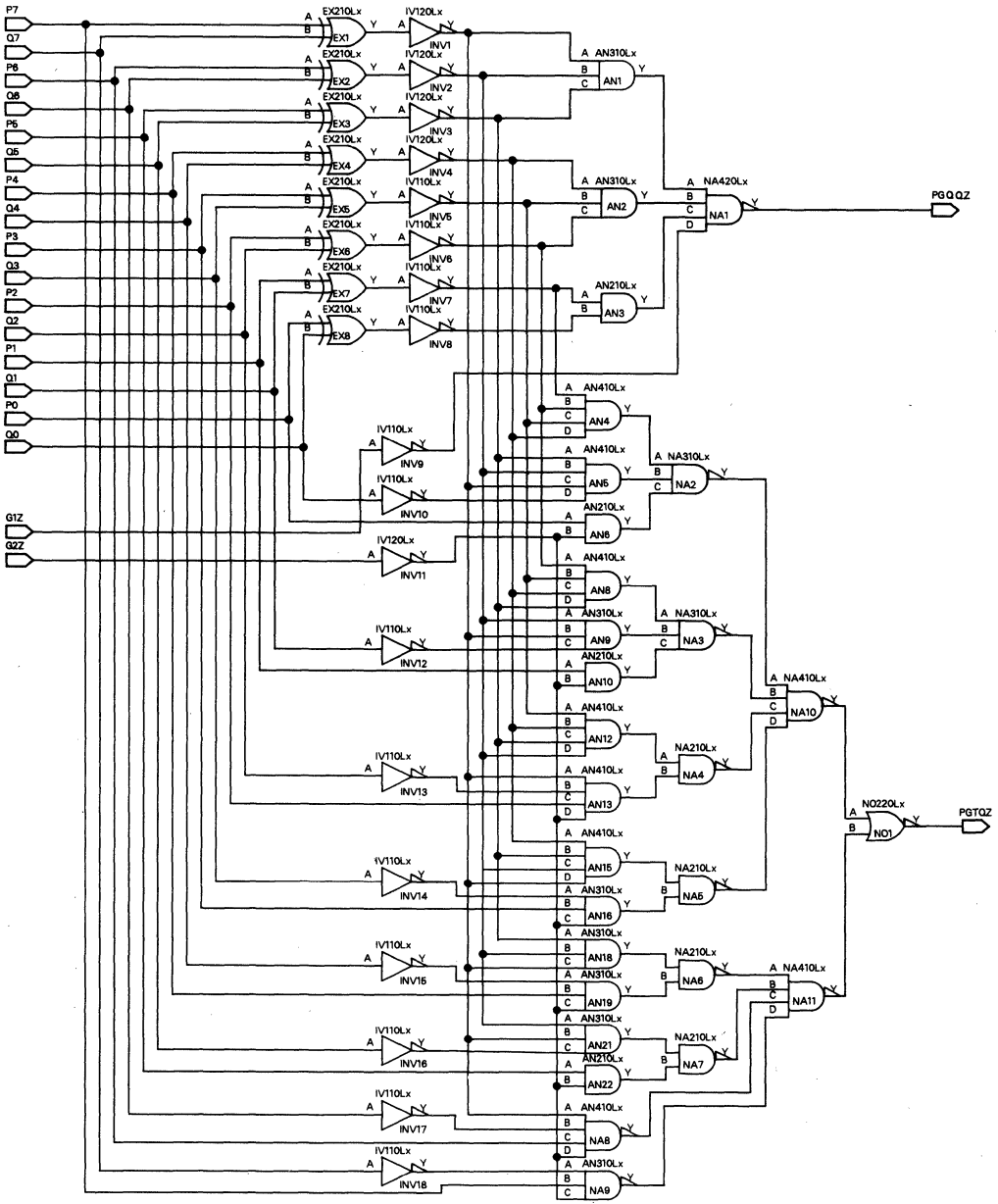
logic diagram



absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER		TEST CONDITIONS	SN54ASC686		SN74ASC686		UNIT
			TYP	MAX	TYP	MAX	
V_T Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC} Supply current		V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		9734		585	nA
C_i Input capacitance	G1Z	V_{CC} = 5 V, T_A = 25°C	0.12		0.12		pF
	G2Z		0.24		0.24		
	Any P or Q		0.34		0.34		
C_{pd} Equivalent power dissipation capacitance†		V_{CC} = 5 V, t_r = t_f = 3 ns, T_A = 25°C	43.3		43.3		pF

† The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 1)

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC686			SN74ASC686			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
t_{pd}	Pn, Qn	Any	C_L = 0		9	20.6		9	19.1	ns
t_{pd}	G1Z,G2Z	Any			7	15.4		7	14.1	
Δt_{pd}	Any	Any		0.3	0.8	2.3	0.3	0.8	2	ns/pF

‡ Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{pd} ≡ propagation delay time, low-to-high or high-to-low output
Δt_{pd} ≡ change in t_{pd} with load capacitance
§ Typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: These switching characteristics are simulations of the software macro cell using interconnect capacitance values for an array design having 2,000 gates. Post-layout simulation uses actual interconnect capacitance values.

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DESIGN CONSIDERATIONS

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

The HDL for this software macro is included as a part of the library supplied for supported engineering workstations so that a single label can be developed to apply the macro as needed. The following printout of the HDL block definition is furnished for reference.

HDL FILE

```
BLOCK S686LH;
P0          @INPUT;
P1          @INPUT;
P2          @INPUT;
P3          @INPUT;
P4          @INPUT;
P5          @INPUT;
P6          @INPUT;
P7          @INPUT;
Q0          @INPUT;
Q1          @INPUT;
Q2          @INPUT;
Q3          @INPUT;
Q4          @INPUT;
Q5          @INPUT;
Q6          @INPUT;
Q7          @INPUT;
G1Z         @INPUT;
G2Z         @INPUT;
PEQQZ       @OUTPUT;
PGTQZ       @OUTPUT;

STRUCTURE
AN1         :AN310LH        INV1O,INV2O,INV3O,AN1O;
AN10        :AN210LH        P1,INV11O,INV10O;
AN12        :AN410LH        INV5O,INV4O,INV3O,INV2O,AN12O;
AN13        :AN410LH        INV1O,INV13O,P2,INV11O,AN13O;
AN15        :AN410LH        INV4O,INV3O,INV2O,INV1O,AN15O;
AN16        :AN310LH        INV14O,P3,INV11O,AN16O;
AN18        :AN310LH        INV3O,INV2O,INV1O,AN18O;
AN19        :AN310LH        INV15O,P4,INV11O,AN19O;
AN2         :AN310LH        INV4O,INV5O,INV6O,AN2O;
AN21        :AN310LH        INV2O,INV1O,INV16O,AN21O;
AN22        :AN210LH        P5,INV11O,AN22O;
AN3         :AN210LH        INV7O,INV8O,AN3O;
AN4         :AN410LH        INV7O,INV6O,INV5O,INV4O,AN4O;
AN5         :AN410LH        INV3O,INV2O,INV1O,INV10O,AN5O;
AN6         :AN210LH        PO,INV11O,AN6O;
AN8         :AN410LH        INV6O,INV5O,INV4O,INV3O,AN8O;
AN9         :AN310LH        INV2O,INV1O,INV12O,AN9O;
```

HDL (Continued)

```
STRUCTURE (Continued)
EX1          :EX210LH        P7,Q7,EX1O;
EX2          :EX210LH        P6,Q6,EX2O;
EX3          :EX210LH        P5,Q5,EX3O;
EX4          :EX210LH        P4,Q4,EX4O;
EX5          :EX210LH        P3,Q3,EX5O;
EX6          :EX210LH        P2,Q2,EX6O;
EX7          :EX210LH        P1,Q1,EX7O;
EX8          :EX210LH        P0,Q0,EX8O;
INV1         :IV120LH        EX1O,INV1O;
INV10        :INV110LH       Q0,INV10O;
INV11        :INV120LH       G2Z,INV11O;
INV12        :IV110LH        Q1,INV12O;
INV13        :IV110LH        Q2,INV13O;
INV14        :IV110LH        Q3,INV14O;
INV15        :IV110LH        Q4,INV15O;
INV16        :IV110LH        Q5,INV16O;
INV17        :IV110LH        Q6,INV17O;
INV18        :IV110LH        Q7,INV18O;
INV2         :IV120LH        EX2O,INV2O;
INV3         :IV120LH        EX3O,INV3O;
INV4         :IV120LH        EX4O,INV4O;
INV5         :IV110LH        EX5O,INV5O;
INV6         :IV110LH        EX6O,INV6O;
INV7         :IV110LH        EX7O,INV7O;
INV8         :IV110LH        EX8O,INV8O;
INV9         :IV110LH        G1Z,INV9O;
NA1          :NA420LH        AN1O,AN2O,AN3O,INV9O,PEQQZ;
NA10         :NA410LH        NA2O,NA3O,NA4O,NA5O,NA10O;
NA11         :NA410LH        NA6O,NA7O,NA8O,NA9O,NA11O;
NA2          :NA310LH        AN4O,AN5O,AN6O,NA2O;
NA3          :NA310LH        AN8O,AN9O,AN10O,NA3O;
NA4          :NA210LH        AN12O,NA13O,NA4O;
NA5          :NA210LH        AN15O,AN16O,NA5O;
NA6          :NA210LH        AN18O,AN19O,NA6O;
NA7          :NA210LH        AN21O,AN22O,NA7O;
NA8          :NA410LH        INV1O,INV17O,P6,INV11O,NA8O;
NA9          :NA310LH        INV18O,P7,INV11O,NA9O;
NO1          :NO220LH        NA10O,NA11O,PGTQZ;
END S686LH;
```


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D2939, AUGUST 1986

SystemCell™ 2-μm SOFTWARE MACRO CELL

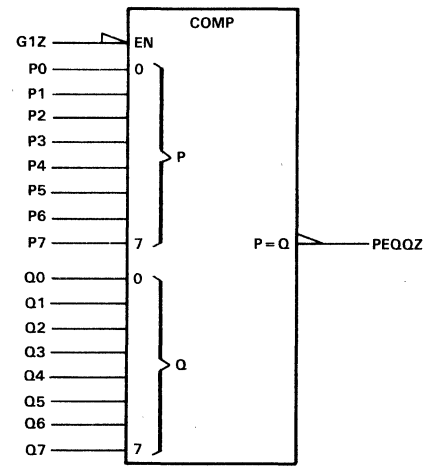
- **Performs Identity Comparison of Binary, BCD, and Monotonic Codes**
- **Cascading Input Accomodates Expansion**
- **Dependable Texas Instruments Quality and Reliability**

description

The SN54ASC688 and SN74ASC688 are standard-cell software macros that implement 8-bit expandable identity comparators. The 8-bit configuration provides the custom IC designer an identity comparator to embed in ASICs in its most efficient form, and the 8-bit width simplifies construction of wider comparators. The 'ASC688 implements a comparison scheme identical with that performed by packaged 'HC688 and 'LS688 comparators.

These 8-bit identity comparators perform bit-by-bit comparison of binary, straight BCD (8-4-2-1), or random codes. The fully decoded equality decision (P = Q?) on 8-bit words (P,Q) is made. These devices are expandable to any number of bits. Words of greater length may be compared by connecting comparators in cascade. The PEQQZ output of a stage handling less-significant bits is connected to the corresponding G1Z input of the next stage handling more-significant bits. The 'ASC688 is implemented with the standard-cell functions indicated. The HDL netlist label for this software macro is shown on the last line of the following table:

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE

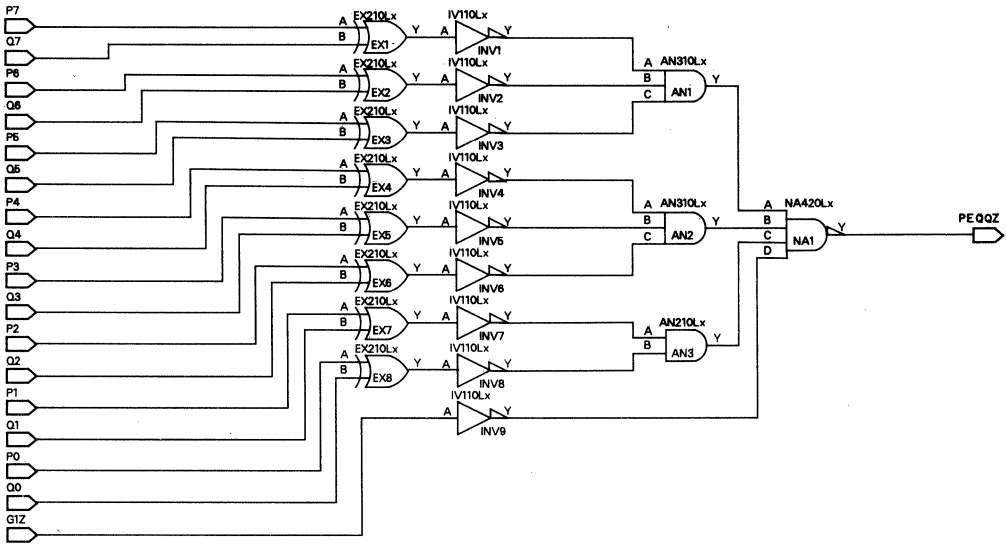
INPUTS		OUTPUT
DATA P,Q	ENABLE G1Z	PEQQZ
P=Q	L	L
P>Q	X	H
P<Q	X	H
X	H	H

CELL NAME	RELATIVE CELL AREA TO NA210LH	NO. USED	TOTAL RELATIVE CELL AREA	TOTAL C_{pd}‡ (pF)	MAXIMUM I_{CC} SN54ASC' (nA)	MAXIMUM I_{CC} SN74ASC' (nA)
AN210LH	1.5	1	1.5	0.9	194	11.6
AN310LH	1.75	2	3.5	2.12	442	26.6
EX210LH	2.0	8	16	8.0	1784	107.2
IV110LH	0.75	9	6.75	3.96	945	56.88
NA420LH	2.5	1	2.5	0.96	312	18.7
TOTALS		21	30.25	15.94	3677	221
Label: S688LH P0,P1,P2,P3,P4,P5,P6,P7,Q0,Q1,Q2,Q3,Q4,Q5,Q6,Q7,G1Z,PEQQZ;						

‡Does not include interconnect capacitance.

The SN54ASC688 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC688 is characterized for operation from −40°C to 85°C.

logic diagram



absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER		TEST CONDITIONS	SN54ASC688 TYP	SN54ASC688 MAX	SN74ASC688 TYP	SN74ASC688 MAX	UNIT
V_T Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC} Supply current		V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		3677		221	nA
C_i Input capacitance	G1Z	V_{CC} = 5 V, T_A = 25°C	0.12		0.12		pF
	Any P or Q		0.22		0.22		
C_{pd} Equivalent power dissipation capacitance†		V_{CC} = 5 V, T_A = 25°C, t_r = t_f = 3 ns	15.94		15.94		pF

† The equivalent power dissipation capacitance does not include interconnect capacitance.

TEXAS INSTRUMENTS
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switching characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted) (see Note 1)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC688			SN74ASC688			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{pd}	Pn, Qn	PEQQZ	C_L = 0		7.5	13.6		7.5	12.3	ns
t_{pd}	G1Z	PEQQZ			3	4.7		3	4.4	ns
Δt_{pd}	Any	PEQQZ		0.3	0.7	2.3	0.3	0.7	2	ns/pF

†Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{pd} ≡ propagation delay time, low-to-high or high-to-low output
Δt_{pd} ≡ change in t_{pd} with capacitance
‡Typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: These switching characteristics are simulations of the software macro cell using interconnect capacitance values for an array design having 2,000 gates. Post-layout simulation uses actual interconnect capacitance values.

DESIGN CONSIDERATIONS

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

The HDL for this software macro is included as a part of the library supplied for supported engineering workstations so that a single label can be developed to apply the macro as needed. The following printout of the HDL block definition is furnished for reference.

HDL FILE

```
BLOCK S688LH;
P0          @INPUT;
P1          @INPUT;
P2          @INPUT;
P3          @INPUT;
P4          @INPUT;
P5          @INPUT;
P6          @INPUT;
P7          @INPUT;
Q0          @INPUT;
Q1          @INPUT;
Q2          @INPUT;
Q3          @INPUT;
Q4          @INPUT;
Q5          @INPUT;
Q6          @INPUT;
Q7          @INPUT;
G1Z         @INPUT;
PEQQZ       @OUTPUT;
```

```
STRUCTURE
AN1         :AN310LH        INV1O,INV2O,INV3O,AN1O;
AN2         :AN310LH        INV4O,INV5O,INV6O,AN2O;
AN3         :AN210LH        INV7O,INV8O,AN3O;
EX1         :EX210LH        P7,Q7,EX1O;
EX2         :EX210LH        P6,Q6,EX2O;
EX3         :EX210LH        P5,Q5,EX3O;
EX4         :EX210LH        P4,Q4,EX4O;
EX5         :EX210LH        P3,Q3,EX5O;
EX6         :EX210LH        P2,Q2,EX6O;
EX7         :EX210LH        P1,Q1,EX7O;
EX8         :EX210LH        P0,Q0,EX8O;
INV1        :IV110LH        EX1O,INV1O;
INV2        :IV110LH        EX2O,INV2O;
INV3        :IV110LH        EX3O,INV3O;
INV4        :IV110LH        EX4O,INV4O;
INV5        :IV110LH        EX5O,INV5O;
INV6        :IV110LH        EX6O,INV6O;
INV7        :IV110LH        EX7O,INV7O;
INV8        :IV110LH        EX8O,INV8O;
INV9        :IV110LH        G1Z,INV9O;
NA1         :NA420LH        AN1O,AN2O,AN3O,INV9O,PEQQZ;
END S688LH;
```

SN54ASC888, SN74ASC888 8-BIT PROCESSOR SLICES

D2939, AUGUST 1986

SystemCell™ COMPATIBLE MegaModule™

- Parallel 8-Bit ALU with Expansion Nodes
- 13 Arithmetic and Logic Functions
- 8 Conditional Shifts (Single and Double Length)
- 9 Instructions that Manipulate Bytes
- 4 Instructions that Manipulate Bits
- Add and Subtract Immediate Instructions
- Absolute Value Instruction
- Signed Magnitude to/from Two's Complement Conversion
- Single- and Double-Length Normalize
- Select Functions
- Signed and Unsigned Divides with Overflow Detection; Input Does Not Need to be Prescaled
- Signed, Mixed, and Unsigned Multiplies
- Three-Operand, 16-Word Register File
- Full Carry Look Ahead Support
- Sign, Carry Out, Overflow, and Zero-Detect Status Capabilities
- Excess-3 BCD Arithmetic
- ALU Bypass Path Increases Speeds of Multiply, Divide, and Normalize Instructions and Provides New Instructions such as Bit Set, Bit Reset, Bit Test, Byte Subtract, Byte Add, and Byte Logical
- 3-Operand Register Files Allow an Operation and a Move Instruction to be Combined
- Bit and Byte Masks are Shared with Register Address Fields to Minimize Control Store Word Width
- 3 Data Input/Output Ports Maximize Data Throughput

description

These 8-bit Advanced CMOS SystemCell™ compatible standard cells implement high-performance digital computer or controller data-paths. An architecture and instruction set has been chosen that supports a fast system clock, a narrow micro-code word width, and a high system throughput. The powerful instruction set allows high-speed system architecture to be implemented and also allows an existing system's performance to be upgraded while protecting software investments. These processors are designed to be cascadable, in increments of eight bits, to any word width of 16 bits or greater.

The SN54ASC888 will be characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC888 will be characterized for operation from −40°C to 85°C.

TEXAS INSTRUMENTS
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node descriptions

NODE NAME	I/O	DESCRIPTION
A0	I	Register file A port read address select (LSB = 0)
A1	I	
A2	I	
A3	I	
B0	I	Register file B port read address select (LSB = 0)
B1	I	
B2	I	
B3	I	
C0	I	Register file address select
C1	I	
C2	I	
C3	I	
CLK	I	Clocks all synchronous registers on positive edge
C_n	I	ALU carry input
CNPL8	O	ALU ripple carry output
DA0	I/O	A port data bus. Outputs register data if EAZ is low, or inputs data if EAZ is high.
DA1	I/O	
DA2	I/O	
DA3	I/O	
DA4	I/O	
DA5	I/O	
DA6	I/O	
DA7	I/O	
DB0	I/O	B port data bus. Outputs register data if OEBZ is low, or input data if OEBZ is high.
DB1	I/O	
DB2	I/O	
DB3	I/O	
DB4	I/O	
DB5	I/O	
DB6	I/O	
DB7	I/O	
EAZ	I	ALU input operand select. High state selects DA bus, and low state selects register file.
EB0	I	ALU input operand select. EB0 and EB1 select the source of data that the S multiplexer provides for the S bus. Independent control of the DB bus and data-path selection allows the user to isolate the DB bus while the ALU continues to process data.
EB1	I	
GZ_N	O	ALU generate/negative result for most significant 8-bit slice, active low
I0	I	Instruction input
I1	I	
I2	I	
I3	I	
I4	I	
I5	I	
I6	I	
I7	I	
LSC	I	Package position inputs
MSC		
OEAZ	I	DA bus enable, active low
OEBZ	I	DB bus enable, active low
OEYZ	I	Y bus output enable, active low

TEXAS INSTRUMENTS
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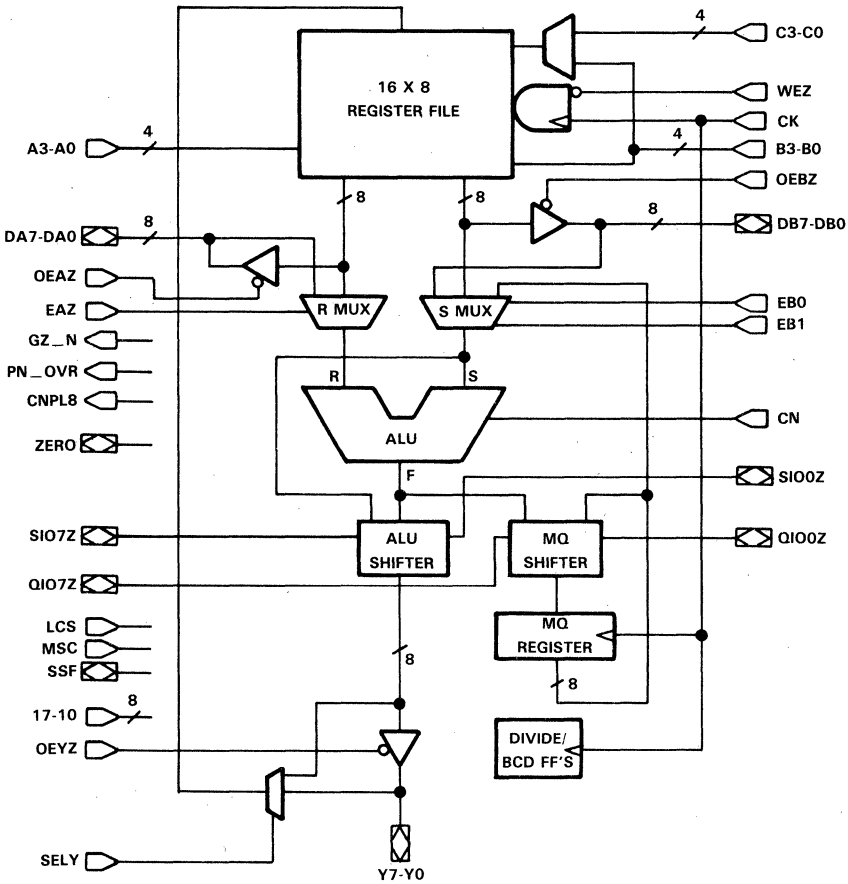
node descriptions (continued)

NODE NAME	I/O	DESCRIPTION
PZ_OVR	O	ALU propagate/instruction overflow for most significant 8-bit slice, active low
SIO7Z	I/O	Bidirectional shift pin, active low
QIO7Z	I/O	
QIO0Z	I/O	
SIO0Z	I/O	
SELY	I	Y bus select, active high
SSF	I/O	Expandable shift function. Used to transfer information between 8-bit slices during special instruction execution in expanded (16-bit, 32-bit) systems
WEZ	I	Register file (RF) write enable. Data is written into RF when WEZ is low and a low-to-high clock transition occurs. RF write is inhibited when WEZ is high.
Y0	I/O	Y port data bus. Outputs instruction results if OEYZ is low or input data register file if OEYZ is high.
Y1	I/O	
Y2	I/O	
Y3	I/O	
Y4	I/O	
Y5	I/O	
Y6	I/O	
Y7	I/O	
ZERO	I/O	ALU shifter zero detection, open drain. Input during certain special instructions

functional block diagram



For additional detailed information refer to the SN54AS888 and the SN74AS888 data sheet, SDBS001B, and the Bit-Slice Processor User's Guide, SDBU001A.

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SN54ASC890, SN74ASC890 MICROSEQUENCERS

D2939, AUGUST 1986

SystemCell™ COMPATIBLE MegaModule™

- **14 Bits Wide — Addresses Up to 16,384 Words of Microcode with One Megacell**
- **Selects Address from One of Eight Sources**
- **Independent Read Pointer for Aid in Microcode Diagnostics**
- **Supports Real-Time Interrupts**
- **Two Independent Loop Counters**
- **Supports 64 Powerful Instructions**
- **Dependable Texas Instruments Quality and Reliability**

description

The SN54ASC890 and SN74ASC890 are Advanced CMOS standard cell microseqencers supporting traditional bit-slice data-path implementations.

The microsequencers select a 14-bit microaddress from one of eight sources to provide the proper microinstruction sequence for bit-slice processor megacells or other microcode-based data paths. These high-performance megacells are capable of addressing 16,384 control store memory locations either sequentially or via conditional branching algorithms. This multiway branching capability, coupled with a nine-word-deep FILO (first in, last out) stack, allows the microprogrammer to arrange his code in blocks so that microprograms may be structured in the same fashion as such high-level languages as ALGOL, Pascal, or Ada.

node descriptions

NODE NAME	I/O	FUNCTION
RAOEZ	I	Enables DRA output, active low
DRA6-DRA0	I/O	Seven LSBs of the A direct data I/O port
OSEL	I	MUX control for the source to DRA. Low selects RA, high selects stack.
MUX2-MUX0	I	MUX control for Y output bus
RC2-RC0	I	Register/counter controls
S2-S0	I	Stack control
CCZ	I	Condition code
CLK	I	Clock
ZERO	O	Zero detect flag for register A and B
STKWRN/RER	O	Stack overflow, underflow/read error flag
DRB6-DRB0	I/O	Seven LSBs of the B direct data I/O port (0 = LSB)
RBOEZ	I	Enables DRB output, active low
DRB13-DRB7	I/O	Seven MSBs of the B direct data I/O port
INTZ	I	When low selects INT RT register to stack
Y13-Y8	I/O	Six MSBs of bidirectional Y port
Y7	I/O	Seventh bit of bidirectional Y port
YOEZ	I	Enables Y output bus, active low
Y6-Y0	I/O	Seven LSBs of bidirectional Y port (0 = LSB)
INC	I	Incrementer control
DRA13-DRA7	I/O	Seven MSBs of direct B data I/O port
B3-B0	I	16-way branch inputs

Both polled and real-time interrupt routines are supported by the 'ASC890 to enhance system throughput capability. Vectored interrupts may occur during any instruction, including PUSHes and POPs.

The SN54ASC890 will be characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC890 will be characterized for operation from −40°C to 85°C.

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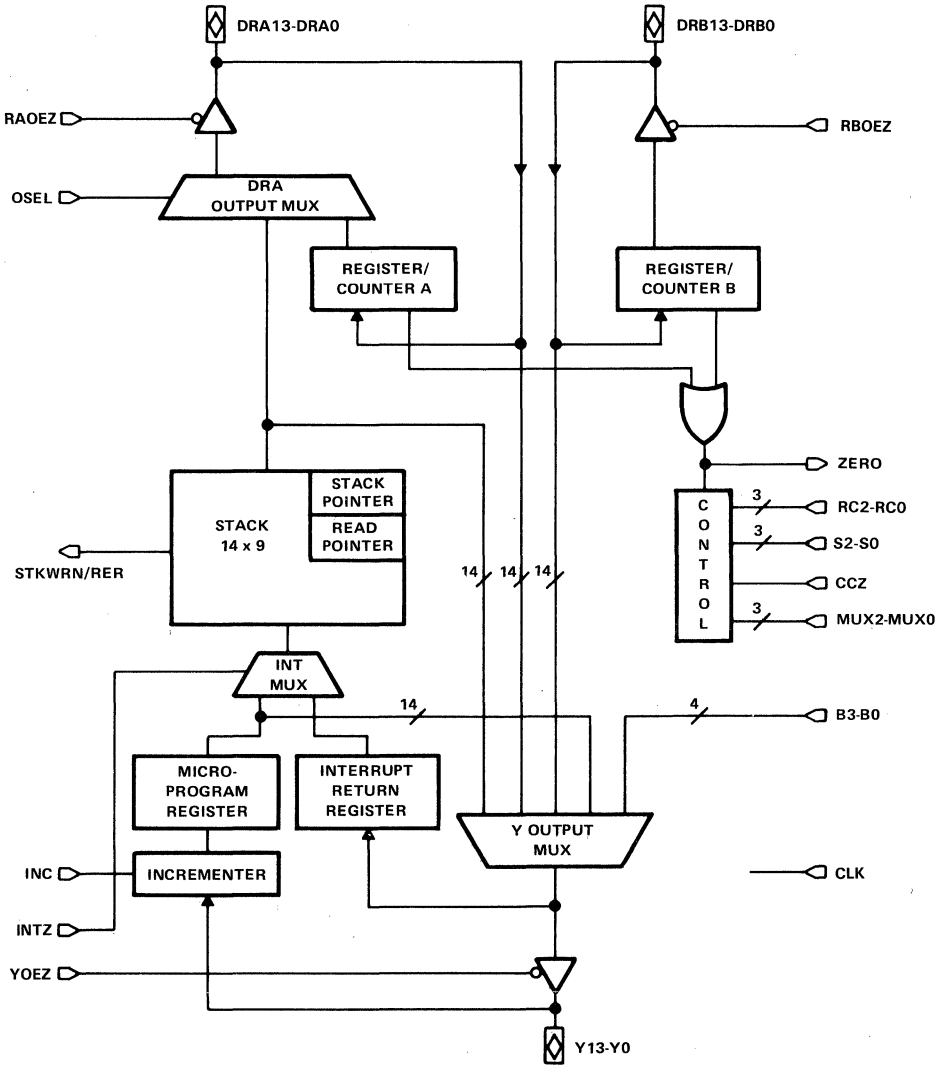
functional block diagram



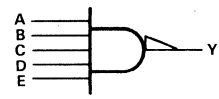
For additional detailed information refer to the SN54AS890 and SN74AS890 data sheet, SDBS002, and the Bit-Slice Processor User's Guide, SDBU001A.

D2939, AUGUST 1986

SystemCell™ 2-μm INTERNAL STANDARD CELL

- **Choice of Two Performance Levels**
- **Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V**
- **Functional Operation Over V_{CC} Range of 2 V to 6 V**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol



positive logic equation

$$Y = \overline{A \cdot B \cdot C \cdot D \cdot E} = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E}$$

FUNCTION TABLE

INPUTS					OUTPUT
A	B	C	D	E	Y
H	H	H	H	H	L
L	X	X	X	X	H
X	L	X	X	X	H
X	X	L	X	X	H
X	X	X	L	X	H
X	X	X	X	L	H

description

The SN54ASC2022 and SN74ASC2022 are 5-input positive-NAND gate CMOS standard cells. The standard-cell library contains two physical implementations providing the custom IC designer a choice between two performance levels for optimizing designs. Each option is designated and called from the engineering workstation input using the following cell names to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		TYPICAL DELAY C_L = 1 pF	RELATIVE CELL AREA TO NA210LH
NA510LH	Label: NA5n0LH A,B,C,D,E,Y;	2.7 ns	1.75
NA520LH		2.1 ns	3

The SN54ASC2022 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC2022 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS		NA510LH		NA520LH		UNIT
					TYP	MAX	TYP	MAX	
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current	SN54ASC2022	V_{CC} = 4.5 V to 5.5 V,	V_I = V_{CC} or 0,		213		365	nA
		SN74ASC2022	T_A = MIN to MAX			12.8		21.9	
C_i	Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.12		0.25		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	$t_r = t_f$ = 3 ns,	0.52		1.02		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

NA510LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC2022			SN74ASC2022			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A thru E	Y	C_L = 0	0.8	1.2	2.4	0.8	1.2	2.2	ns
t_{PHL}				0.6	1.3	3.5	0.7	1.3	3	
t_{PLH}	A thru E	Y	C_L = 1 pF	1.3	2.6	6.3	1.4	2.6	5.8	ns
t_{PHL}				1.6	2.7	9.2	1.7	2.7	8	
Δt_{PLH}	A thru E	Y		0.5	1.4	4.3	0.5	1.4	3.9	ns/pF
Δt_{PHL}				0.9	2.2	5.8	1	2.2	5	

NA520LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC2022			SN74ASC2022			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A thru E	Y	C_L = 0	0.7	1.2	2.4	0.7	1.2	2.2	ns
t_{PHL}				0.6	1.2	2.9	0.6	1.2	2.6	
t_{PLH}	A thru E	Y	C_L = 1 pF	1	1.9	3.9	1.1	1.9	3.5	ns
t_{PHL}				1.1	2.2	5.7	1.2	2.2	5	
Δt_{PLH}	A thru E	Y		0.3	0.7	1.6	0.3	0.7	1.4	ns/pF
Δt_{PHL}				0.4	1	2.8	0.5	1	2.4	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to Section 7.

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

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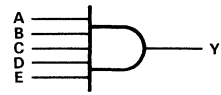
D2939, AUGUST 1986

SystemCell™ 2-μm INTERNAL STANDARD CELL

- **2.9 ns Typical Propagation Delay with 1-pF Load**
- **Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V**
- **Functional Operation Over V_{CC} Range of 2 V to 6 V**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol



FUNCTION TABLE

OUTPUT					INPUTS
A	B	C	D	E	Y
H	H	H	H	H	H
L	X	X	X	X	L
X	L	X	X	X	L
X	X	L	X	X	L
X	X	X	L	X	L
X	X	X	X	L	L

positive logic equation

$$Y = ABCDE = \overline{\overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E}}$$

description

The SN54ASC2024 and SN74ASC2024 are 5-input positive-AND gate CMOS standard cells. Each cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		TYPICAL DELAY C_L = 1 pF	RELATIVE CELL AREA TO NA210LH
AN510LH	Label: AN510LH A,B,C,D,E,Y;	2.9 ns	2.25

The SN54ASC2024 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC2024 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS		TYP	MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		V
I_{CC}	Supply current	SN54ASC2024	V_{CC} = 4.5 V to 5.5 V,	V_I = V_{CC} or 0,		286	nA
		SN74ASC2024	T_A = MIN to MAX			17.2	
C_i	Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.13		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	1.12		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC2024			SN74ASC2024			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A thru E	Y	C_L = 0	1	2.4	6.1	1.1	2.4	5.3	ns
t_{PHL}				0.7	1.7	3.9	0.8	1.7	3.5	
t_{PLH}	A thru E	Y	C_L = 1 pF	1.6	3.4	8.6	1.7	3.4	7.5	ns
t_{PHL}				1.1	2.3	5.5	1.1	2.3	4.9	
Δt_{PLH}	A thru E	Y		0.5	1	2.5	0.5	1	2.2	ns/pF
Δt_{PHL}				0.2	0.6	1.6	0.3	0.6	1.4	

† Propagation delay times are measured from V_I = 44% to V_O = 44% of V_{CC} with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to Section 7.

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

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D2939, AUGUST 1986

SystemCell™ 2-μm HARDWIRED MACRO CELL

- **Provides Complementary Q and QZ Outputs**
- **Choice Between Three Clocked Toggle Flip-Flop Configurations**
- **Cascadable for Implementing Ripple Counters**
- **Implements High-Speed Counters: Clock Frequencies . . . 54 to 65 MHz**

latch cells offered

CELL NAME	PRESET	CLEAR
TAB20LH	yes	yes
TAC20LH	no	yes
TAP20LH	yes	no

description

The SN54ASC2102 and SN74ASC2102 are dedicated, hardwired standard-cell macros implementing toggle flip-flops with clear and/or preset. The 'ASC2102 latches offer three choices of individual flip-flop configurations providing the custom IC designer a clocked storage element to embed in ASICs in its most efficient form: as stand-alone bit-control devices or as additions to larger latched function.

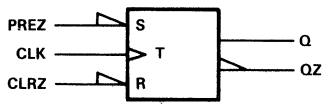
A low level at the preset or clear input controls the state of the outputs regardless of the levels at other inputs. When preset and clear inputs are inactive (high) and the clock input makes a low-to-high transition, each of the complementary outputs will toggle to its opposite state. While the clock remains high or transitions to the low level and remains low, the outputs will remain stable. The cells are designated and called from the engineering workstation input using the following cell names to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		MAXIMUM CLOCK FREQUENCY	RELATIVE CELL AREA TO NA210LH
TAB20LH	Label: TAB20LH CLRZ,PREZ,CLK,Q,QZ;	54.2 MHz	7.7
TAC20LH	Label: TAC20LH CLRZ,CLK,Q,QZ;	61.7 MHz	7.2
TAP20LH	Label: TAP20LH PREZ,CLK,Q,QZ;	65.8 MHz	7

The SN54ASC2102 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC2102 is characterized for operation from −40°C to 85°C.

logic symbol†

TAB20LH



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE

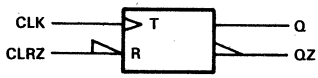
TAB20LH

INPUTS			OUTPUTS	
PREZ	CLRZ	CLK	Q	QZ
L	H	X	H	L
H	L	X	L	H
L	L	X	L‡	L‡
H	H	↑	$\overline{Q}_0$	Q_0
H	H	L	Q_0	$\overline{Q}_0$

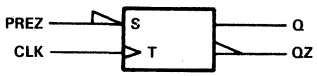
‡ This configuration is nonstable; that is, it will not persist when the PREZ and CLRZ inputs return to their inactive (H) level.

logic symbols†

TAC20LH



TAP20LH



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLES

TAC20LH

INPUTS		OUTPUT	
CLRZ	CLK	Q	QZ
L	X	L	H
H	↑	$\overline{Q}_0$	Q_0
H	L	Q_0	$\overline{Q}_0$

TAP20LH

INPUTS		OUTPUT	
PREZ	CLK	Q	QZ
L	X	H	L
H	↑	$\overline{Q}_0$	Q_0
H	L	Q_0	$\overline{Q}_0$

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			TAB20LH				TAC20LH				UNIT
			SN54′		SN74′		SN54′		SN74′		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			50.8		54.2		54.2		61.7	MHz
t_w	Pulse duration	CLRZ low	8.8		7.6		7.6		7.6		ns
		PREZ low	7.6		7.6						
		CLK high or low	9.8		9.2		9.2		8.2		
t_{su}	Setup time before clock	CLRZ inactive	7.2		6		4.8		4.8		ns
		PREZ inactive	7.2		4.8						
t_h	Hold time after clock	CLRZ low	0		0		0		0		ns
		PREZ low	0		−0.8						

			TAP20LH				UNIT
			SN54′		SN74′		
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			58.3		65.8	MHz
t_w	Pulse duration	PREZ low	7.6		7.6		ns
		CLK high or low	8.5		7.6		
t_{su}	Setup time before clock	PREZ inactive	2.4		2.4		ns
t_h	Hold time after clock	PREZ low	2.4		2.4		ns

TEXAS INSTRUMENTS
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electrical characteristics

TAB20LH

PARAMETER			TEST CONDITIONS	SN54ASC2102 TYP	SN54ASC2102 MAX	SN74ASC2102 TYP	SN74ASC2102 MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current		V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		939		56.2	nA
C_i	Input capacitance	CLRZ	V_{CC} = 5 V, T_A = 25°C	0.25		0.25		pF
		PREZ		0.36		0.36		
		CLK		0.29		0.29		
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, t_r = t_f = 3 ns, T_A = 25°C	4.2		4.2		pF

TAC20LH

PARAMETER			TEST CONDITIONS	SN54ASC2102 TYP	SN54ASC2102 MAX	SN74ASC2102 TYP	SN74ASC2102 MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current		V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		884		53	nA
C_i	Input capacitance	CLRZ	V_{CC} = 5 V, T_A = 25°C	0.36		0.36		pF
		CLK		0.25		0.25		
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, t_r = t_f = 3 ns, T_A = 25°C	3.79		3.79		pF

TAP20LH

PARAMETER			TEST CONDITIONS	SN54ASC2102 TYP	SN54ASC2102 MAX	SN74ASC2102 TYP	SN74ASC2102 MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current		V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		846		50.8	nA
C_i	Input capacitance	PREZ	V_{CC} = 5 V, T_A = 25°C	0.35		0.35		pF
		CLK		0.26		0.26		
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, t_r = t_f = 3 ns, T_A = 25°C	3.59		3.59		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TAB20LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC2102			SN74ASC2102			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	CLK	Q,QZ	C_L = 0	2.2	5.1	13.4	2.4	5.1	11.8	ns
t_{PHL}				1.5	3.3	8.4	1.6	3.3	7.4	
t_{PLH}	PREZ	Q		2	4	9.7	2.1	4	8.6	ns
	CLRZ	QZ		2	4	9.7	2.1	4	8.6	
t_{PHL}	PREZ	QZ		1.1	2	4.4	1.2	2	4	
	CLRZ	Q		1.1	2	4.4	1.2	2	4	
t_{PLH}	CLK	Q,QZ	C_L = 1 pF	2.4	5.6	14.7	2.6	5.6	12.9	ns
t_{PHL}				1.7	3.7	9.4	1.8	3.7	8.3	
t_{PLH}	PREZ	Q		2.3	4.5	11	2.4	4.5	9.8	
	CLRZ	QZ		2.3	4.5	11	2.4	4.5	9.8	
t_{PHL}	PREZ	QZ		1.3	2.4	5.4	1.4	2.4	4.9	
	CLRZ	Q		1.3	2.4	5.4	1.4	2.4	4.9	
Δt_{PLH}	Any	Q,QZ		0.2	0.5	1.4	0.2	0.5	1.2	ns/pF
Δt_{PHL}				0.1	0.4	1.1	0.1	0.4	0.9	

TAC20LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC2102			SN74ASC2102			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	CLK	Q,QZ	C_L = 0	1.9	4.6	13	2.1	4.6	11.3	ns
t_{PHL}				1.4	3.1	7.9	1.6	3.1	7	
t_{PLH}	CLRZ	QZ		1.8	3.5	8.3	2	3.5	7.4	
t_{PHL}	CLRZ	Q		1.1	2	4.3	1.2	2	3.9	
t_{PLH}	CLK	Q,QZ	C_L = 1 pF	2.2	5.1	14.2	2.3	5.1	12.5	ns
t_{PHL}				1.6	3.5	8.8	1.7	3.5	7.7	
t_{PLH}	CLRZ	QZ		2.1	4	9.4	2.2	4	8.4	
t_{PHL}	CLRZ	Q		1.3	2.4	5.3	1.4	2.4	4.8	
Δt_{PLH}	Any	Q,QZ		0.2	0.5	1.3	0.2	0.5	1.2	ns/pF
Δt_{PHL}				0.1	0.4	1	0.1	0.4	0.9	

TAP20LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC2102			SN74ASC2102			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	CLK	Q,QZ	C_L = 0	1.9	4.5	12.5	2	4.5	10.9	ns
t_{PHL}				1.3	3	8.2	1.4	3	7.2	
t_{PLH}	PREZ	Q		1.8	3.4	8	1.9	3.4	7.1	
t_{PHL}	PREZ	QZ		1.1	2	4.1	1.2	2	3.8	
t_{PLH}	CLK	Q,QZ	C_L = 1 pF	2.1	5	13.7	2.3	5	12	ns
t_{PHL}				1.5	3.4	9.1	1.6	3.4	8	
t_{PLH}	PREZ	Q		2	3.9	9.2	2.2	3.9	8.2	
t_{PHL}	PREZ	QZ		1.3	2.4	5	1.3	2.4	4.6	
Δt_{PLH}	Any	Q,QZ		0.2	0.5	1.3	0.2	0.5	1.1	ns/pF
Δt_{PHL}				0.1	0.4	1	0.1	0.4	0.9	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
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DESIGN CONSIDERATIONS

interfacing the macro

Inputs and outputs of these dedicated macros are compatible for interfacing directly with cells and macros available in the TI standard-cell library. The inputs can be driven by either noninverting or inverting input cells. The outputs can be interfaced to drive off-chip loads with any of the noninverting output buffers or interfaced to external bidirectional buses through a 3-state input/output TTL/CMOS buffer.

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered for managing unused inputs.

designing for testability

Designers employing storage or bistable elements should consider testability of the design in its final form. The need to preset or clear these elements should be assessed throughout the development of custom logic circuits with these considerations extended to the end equipment application with respect to maintainability. Simple actions on the part of the ASIC designer can result in considerable cost savings, allowing the expense of IC testing, system testing, and system maintenance to be reduced significantly.

power-up clear/preset

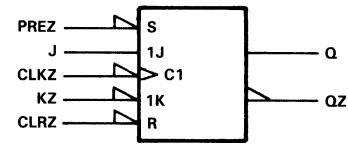
Standard-cell storage elements containing the capability to be asynchronously preset or cleared may be connected to the SN54ASC2320 or SN74ASC2320 power-up/clear cells to achieve system initialization. Control of the clear or preset inputs from another system signal in conjunction with the power-up clear can be achieved with an AND gate.

D2939, AUGUST 1986

SystemCell™ 2-μm HARDWIRED MACRO CELL

- **Provides Complementary Q and QZ Outputs**
- **Negative-Edge Triggered with J and KZ Data Inputs**
- **CLRZ and PREZ Inputs Provide Asynchronous Initialization**
- **J and KZ Inputs Simplify Implementation of Toggle Flip-Flops**

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The SN54ASC2108 and SN74ASC2108 are dedicated, hardwired standard-cell macros implementing negative-edge-triggered flip-flops. A low level at the Preset or Clear input controls the state of the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the J and KZ inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the fall time of the clock transition. Following the hold time interval, data at the J and KZ inputs may be changed wihout affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J high and KZ low. They also can perform as D-type flip-flops if J and KZ are tied together. The JKB21LH flip-flop implements the identical function and sequential operation to one-half of the 'LS109, 'S109, or 'F109 packaged flip-flops except the JKB21LH is negative-edge triggered rather than positive-edge triggered. The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

FUNCTION TABLE

INPUTS					OUTPUTS	
PREZ	CLRZ	CLKZ	J	KZ	Q	QZ
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	L‡	L‡
H	H	↓	L	L	L	H
H	H	↓	H	L	TOGGLE	
H	H	↓	L	H	Q_0	QZ_0
H	H	↓	H	H	H	L
H	H	L	X	X	Q_0	QZ_0

‡ This configuration is nonstable; that is, it will not persist when PREZ or CLRZ returns to its inactive (high) level.

CELL NAME	NETLLIST HDL LABEL	FEATURES	
		MAXIMUM CLOCK FREQUENCY	RELATIVE CELL AREA TO NA210LH
JKB21LH	Label: JKB21LH CLRZ,PREZ,J,KZ,CLKZ,Q,QZ;	44.2 MHz	13.3

The SN54ASC2108 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC2108 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			MIN	MAX	UNIT
f_{clock}	Clock frequency			44.2	MHz
t_w	Pulse duration	PREZ or CLRZ low	9		ns
		CLKZ high or low	11.4		
t_{su}	Setup time	CLRZ inactive	1.8		ns
		PREZ inactive	−0.4		
		J or KZ high or low	9		
t_h	Hold time	CLRZ low	3		ns
		PREZ low	9.6		
		J or KZ high or low	0		

electrical characteristics

PARAMETER			TEST CONDITIONS	SN54ASC2108		SN74ASC2108		UNIT
				TYP	MAX	TYP	MAX	
V_T	Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current		V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		1194		71.6	nA
C_i	Input capacitance	PREZ or CLRZ	V_{CC} = 5 V, T_A = 25°C	0.25		0.25		pF
		J		0.12		0.12		
		KZ or CLKZ		0.13		0.13		
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, t_r = t_f = 3 ns, T_A = 25°C	4.97		4.97		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC2108			SN74ASC2108			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	CLKZ	Q,QZ	C_L = 0	1.8	5	12.9	2.2	5	11.4	ns
t_{PHL}				1.9	4.5	13.4	2	4.5	11.1	
t_{PLH}	PREZ,CLRZ	Q,QZ		2	4.3	11.1	2.2	4.3	9.8	ns
t_{PHL}				1.1	2.1	5.2	1.2	2.1	4.8	
t_{PLH}	CLKZ	Q,QZ	C_L = 1 pF	2.3	5.5	14	2.5	5.5	12.5	ns
t_{PHL}				2.1	4.9	12.5	2.3	4.9	11.9	
t_{PLH}	PREZ,CLRZ	Q,QZ		2.3	4.8	12.2	2.5	4.8	10.9	ns
t_{PHL}				1.3	2.5	6.4	1.4	2.5	5.8	
Δt_{PLH}	Any	Q,QZ		0.2	0.5	1.3	0.2	0.5	1.2	ns/pF
Δt_{PHL}				0.1	0.4	1.2	0.1	0.4	1.1	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are V_{CC} = 5 V, T_A = 25°C.

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DESIGN CONSIDERATIONS

interfacing the macro

Inputs and outputs of these dedicated macros are compatible for interfacing directly with cells and macros available in the TI standard cell library. The inputs can be driven by either noninverting or inverting input cells. The outputs can be interfaced to drive off-chip loads with any of the noninverting output buffers or interfaced to external bidirectional buses through a 3-state input/output TTL/CMOS buffer.

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

designing for testability

Designs employing storage or bistable elements should consider testability of the design in its final form. The need to preset or clear these elements should be assessed throughout the development of custom logic circuits with these considerations extended to the end equipment application with respect to maintainability. Simple actions on the part of the ASIC designer can result in considerable cost savings, allowing the expense of IC testing, system testing, and system maintenance to be reduced significantly.

power-up clear/preset

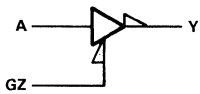
Standard cell storage elements containing the capability to be asynchronously preset or cleared may be connected to the SN54ASC2320 or SN74ASC2320 power-up clear cell to achieve system initialization. Control of the clear or preset inputs from another system signal in conjunction with the power-up clear can be achieved with an AND gate.

D2939, AUGUST 1986

SystemCell™ 2-μm INTERNAL STANDARD CELL

- **Choice of Three Performance Levels**
- **Active-Low Enable**
- **Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V**
- **Functional Operation Over V_{CC} Range of 2 V to 6 V**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol



FUNCTION TABLE

INPUTS		OUTPUT
GZ	A	Y
L	H	L
L	L	H
H	X	Z

positive logic equation

$Y = \overline{A}$ when GZ is L

description

The SN54ASC2310 and SN74ASC2310 are inverting 3-state internal buffer standard cells that interface internal cells with internal buses. The standard-cell library contains three physical implementations providing the custom IC designer a choice between three performance levels for optimizing designs. Each option is designated and called from the engineering workstation input using the following cell names to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		TYPICAL DELAY C_L = 1 pF	RELATIVE CELL AREA TO NA210LH
IV211LH	Label: IV2n1LH A,GZ,Y;	2.6 ns	1.5
IV221LH		1.7 ns	2
IV241LH		1.3 ns	3

The SN54ASC2310 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC2310 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS	IV211LH TYP	IV211LH MAX	IV221LH TYP	IV221LH MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current	SN54ASC2310	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0,		180		244	nA
		SN74ASC2310	T_A = MIN to MAX		10.8		14.6	
C_i	Input capacitance	A	V_{CC} = 5 V, T_A = 25°C	0.22		0.47		pF
		GZ		0.4		0.55		
C_o	Output capacitance		V_{CC} = 5 V, T_A = 25°C	0.22		0.39		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, t_r = t_f = 3 ns, T_A = 25°C	0.49		1		pF

PARAMETER			TEST CONDITIONS	IV241LH TYP	IV241LH MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		V
I_{CC}	Supply current	SN54ASC2310	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0,		359	nA
		SN74ASC2310	T_A = MIN to MAX		21.5	
C_i	Input capacitance	A	V_{CC} = 5 V, T_A = 25°C	1		pF
		GZ		0.85		
C_o	Output capacitance		V_{CC} = 5 V, T_A = 25°C	0.59		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, t_r = t_f = 3 ns, T_A = 25°C	1.88		pF

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

IV211LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC2310			SN74ASC2310			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	C_L = 0	0.6	0.9	2	0.6	0.9	1.8	ns
t_{PHL}				0.5	0.9	2.3	0.6	0.9	2	
t_{PLH}	A	Y	C_L = 1 pF	1.6	2.9	6.5	1.7	2.9	5.9	ns
t_{PHL}				1.1	2.2	5.3	1.2	2.2	4.6	
t_{PZH}	GZ	Y	C_L = 1 pF, R_L = 40 kΩ to GND	1.4	2.7	5.9	1.5	2.7	5.3	ns
t_{PZL}	GZ	Y	C_L = 1 pF, R_L = 20 kΩ to V_{CC}	1.3	2.5	5.9	1.4	2.5	5.1	ns
t_{PHZ}	GZ	Y	C_L = 1 pF, R_L = 40 kΩ to GND		7.5			7.5		ns
t_{PLZ}	GZ	Y	C_L = 1 pF, R_L = 20 kΩ to V_{CC}		4			4		ns
Δt_{PLH}	A	Y		0.9	2	4.6	1	2	4.2	ns/pF
Δt_{PHL}				0.6	1.3	3	0.6	1.3	2.7	
Δt_{PZH}	GZ	Y		1	2.1	4.8	1	2.1	4.4	ns/pF
Δt_{PZL}				0.5	1.3	3.6	0.6	1.3	3.1	

IV221LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC2310			SN74ASC2310			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	C_L = 0	0.6	0.9	1.9	0.6	0.9	1.7	ns
t_{PHL}				0.4	0.9	1.9	0.4	0.9	1.7	
t_{PLH}	A	Y	C_L = 1 pF	1.1	1.9	4.1	1.1	1.9	3.8	ns
t_{PHL}				0.8	1.5	3.5	0.8	1.5	3.1	
t_{PZH}	GZ	Y	C_L = 1 pF, R_L = 40 kΩ to GND	0.7	1.5	3.2	0.8	1.5	3	ns
t_{PZL}	GZ	Y	C_L = 1 pF, R_L = 20 kΩ to V_{CC}	1	1.8	4	1.1	1.8	3.5	ns
t_{PHZ}	GZ	Y	C_L = 1 pF, R_L = 40 kΩ to GND		8.9			8.9		ns
t_{PLZ}	GZ	Y	C_L = 1 pF, R_L = 20 kΩ to V_{CC}		4.5			4.5		ns
Δt_{PLH}	A	Y		0.4	1	2.3	0.5	1	2.1	ns/pF
Δt_{PHL}				0.3	0.7	1.7	0.4	0.7	1.5	
Δt_{PZH}	GZ	Y		0.6	1	2.3	0.6	1	2.1	ns/pF
Δt_{PZL}				0.2	0.7	1.8	0.3	0.7	1.5	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
t_{PHZ} ≡ output disable time from high level
t_{PLZ} ≡ output disable time from low level
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
Δt_{PZH} ≡ change in t_{PZH} with load capacitance
Δt_{PZL} ≡ change in t_{PZL} with load capacitance
‡ Typical values are V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

IV241LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC2310			SN74ASC2310			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	C_L = 0	0.6	0.9	1.7	0.6	0.9	1.6	ns
t_{PHL}				0.3	0.7	1.8	0.3	0.7	1.6	
t_{PLH}	A	Y	C_L = 1 pF	0.8	1.4	2.9	0.8	1.4	2.6	ns
t_{PHL}				0.5	1.1	2.6	0.5	1.1	2.3	
t_{PZH}	GZ	Y	C_L = 1 pF, R_L = 40 kΩ to GND	0.2	0.9	2.1	0.3	0.9	1.9	ns
t_{PZL}	GZ	Y	C_L = 1 pF, R_L = 20 kΩ to V_{CC}	0.9	1.5	3.3	0.9	1.5	2.9	ns
t_{PHZ}	GZ	Y	C_L = 1 pF, R_L = 40 kΩ to GND		9.8			9.8		ns
t_{PLZ}	GZ	Y	C_L = 1 pF, R_L = 20 kΩ to V_{CC}		4.9			4.9		ns
Δt_{PLH}	A	Y		0.2	0.5	1.2	0.2	0.5	1.1	ns/pF
Δt_{PHL}				0.2	0.4	0.9	0.2	0.4	0.8	
Δt_{PZH}	GZ	Y		0.4	0.6	1.1	0.4	0.6	1	ns/pF
Δt_{PZL}				0.1	0.4	1	0.1	0.4	0.8	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
t_{PHZ} ≡ output disable time from high level
t_{PLZ} ≡ output disable time from low level
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
Δt_{PZH} ≡ change in t_{PZH} with load capacitance
Δt_{PZL} ≡ change in t_{PZL} with load capacitance
‡ Typical values are V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to Section 7.

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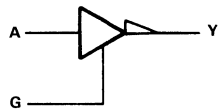
D2939, AUGUST 1986

SystemCell™ 2-μm INTERNAL STANDARD CELL

- Choice of Three Performance Levels
- Active-High Enable
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol



FUNCTION TABLE

INPUTS		OUTPUT
G	A	Y
H	H	L
H	L	H
L	X	Z

positive logic equation

$Y = \overline{A}$

description

The SN54ASC2311 and SN74ASC2311 are inverting 3-state internal buffer standard cells that interface internal cells with internal buses. The standard-cell library contains three physical implementations to provide the custom IC designer a choice between three performance levels for optimizing designs. Each option is designated and called from the engineering workstation input using the following cell names to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		TYPICAL DELAY C_L = 1 pF	RELATIVE CELL AREA TO NA210LH
IV212LH	Label: IV2n2LH A,G,Y;	2.6 ns	1.5
IV222LH		1.8 ns	2
IV242LH		1.3 ns	3

The SN54ASC2311 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC2311 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS	IV212LH TYP	IV212LH MAX	IV222LH TYP	IV222LH MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current	SN54ASC2311	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0,		180		243	nA
		SN54ASC2311	T_A = MIN to MAX		10.8		14.6	
C_i	Input capacitance	A	V_{CC} = 5 V, T_A = 25°C	0.24		0.47		pF
		G		0.31		0.42		
C_o	Output capacitance		V_{CC} = 5 V, T_A = 25°C	0.18		0.33		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, t_r = t_f = 3 ns, T_A = 25°C	0.5		0.98		pF

PARAMETER			TEST CONDITIONS	IV242LH TYP	IV242LH MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		V
I_{CC}	Supply current	SN54ASC2311	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0,		358	nA
		SN74ASC2311	T_A = MIN to MAX		21.5	
C_i	Input capacitance	A	V_{CC} = 5 V, T_A = 25°C	1		pF
		G		0.58		
C_o	Output capacitance		V_{CC} = 5 V, T_A = 25°C	0.48		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, t_r = t_f = 3 ns, T_A = 25°C	1.86		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

IV212LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC2311 MIN	SN54ASC2311 TYP‡	SN54ASC2311 MAX	SN74ASC2311 MIN	SN74ASC2311 TYP‡	SN74ASC2311 MAX	UNIT
t_{PLH}	A	Y	C_L = 0	0.6	1	2	0.6	1	1.8	ns
t_{PHL}				0.5	0.9	1.9	0.6	0.9	1.7	
t_{PLH}	A	Y	C_L = 1 pF	1.6	3	6.6	1.7	3	6	ns
t_{PHL}				1.1	2.2	5.2	1.2	2.2	4.6	
t_{PZH}	G	Y	C_L = 1 pF, R_L = 40 kΩ to GND	1.4	3	6.9	1.5	3	6.2	ns
t_{PZL}	G	Y	C_L = 1 pF, R_L = 20 kΩ to V_{CC}	1.2	2.3	5.1	1.3	2.3	4.5	ns
t_{PHZ}	G	Y	C_L = 1 pF, R_L = 40 kΩ to GND		8.2			8.2		ns
t_{PLZ}	G	Y	C_L = 1 pF, R_L = 20 kΩ to V_{CC}		3.5			3.5		ns
Δt_{PLH}	A	Y		0.9	2	4.6	1	2	4.2	ns/pF
Δt_{PHL}				0.6	1.3	3.3	0.6	1.3	2.9	
Δt_{PZH}	G	Y		1	2.1	4.8	1	2.1	4.4	ns/pF
Δt_{PZL}				0.7	1.3	3.6	0.7	1.3	3.1	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
t_{PHZ} ≡ output disable time from high level
t_{PLZ} ≡ output disable time from low level
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
Δt_{PZH} ≡ change in t_{PZH} with load capacitance
Δt_{PZL} ≡ change in t_{PZL} with load capacitance
‡ Typical values are V_{CC} = 5 V, T_A = 25°C.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

IV222LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC2311			SN74ASC2311			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	C_L = 0	0.6	1	2	0.6	1	1.8	ns
t_{PHL}				0.4	0.9	1.8	0.4	0.9	1.7	
t_{PLH}	A	Y	C_L = 1 pF	1.1	2	4.2	1.1	2	3.8	ns
t_{PHL}				0.8	1.5	3.5	0.8	1.5	3.1	
t_{PZH}	G	Y	C_L = 1 pF, R_L = 40 kΩ to GND	0.9	2	4.4	1	2	4	ns
t_{PZL}	G	Y	C_L = 1 pF, R_L = 20 kΩ to V_{CC}	0.6	1.4	3.1	0.7	1.4	2.8	ns
t_{PHZ}	G	Y	C_L = 1 pF, R_L = 40 kΩ to GND		10			10		ns
t_{PLZ}	G	Y	C_L = 1 pF, R_L = 20 kΩ to V_{CC}		3.8			3.8		ns
Δt_{PLH}	A	Y		0.4	1	2.3	0.5	1	2.1	ns/pF
Δt_{PHL}				0.3	0.7	1.7	0.4	0.7	1.4	
Δt_{PZH}	G	Y		0.4	1	2.3	0.5	1	2.1	ns/pF
Δt_{PZL}				0.5	0.7	1.7	0.5	0.7	1.5	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
t_{PHZ} ≡ output disable time from high level
t_{PLZ} ≡ output disable time from low level
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
Δt_{PZH} ≡ change in t_{PZH} with load capacitance
Δt_{PZL} ≡ change in t_{PZL} with load capacitance
‡ Typical values are V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

IV242LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC2311			SN74ASC2311			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	C_L = 0	0.6	0.9	1.8	0.6	0.9	1.7	ns
t_{PHL}				0.2	0.7	1.7	0.3	0.7	1.5	
t_{PLH}	A	Y	C_L = 1 pF	0.8	1.4	3	0.8	1.4	2.7	ns
t_{PHL}				0.5	1.1	2.5	0.5	1.1	2.2	
t_{PZH}	G	Y	C_L = 1 pF, R_L = 40 kΩ to GND	0.7	1.6	3.4	0.8	1.6	3.1	ns
t_{PZL}	G	Y	C_L = 1 pF, R_L = 20 kΩ to V_{CC}	0.2	0.8	2	0.2	0.8	1.8	ns
t_{PHZ}	G	Y	C_L = 1 pF, R_L = 40 kΩ to GND		12			12		ns
t_{PLZ}	G	Y	C_L = 1 pF, R_L = 20 kΩ to V_{CC}		3.7			3.7		ns
Δt_{PLH}	A	Y		0.2	0.5	1.2	0.2	0.5	1.1	ns/pF
Δt_{PHL}				0.2	0.4	0.9	0.2	0.4	0.8	
Δt_{PZH}	G	Y		0.2	0.5	1.2	0.2	0.5	1.1	ns/pF
Δt_{PZL}				0.3	0.5	0.9	0.3	0.5	0.8	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
t_{PHZ} ≡ output disable time from high level
t_{PLZ} ≡ output disable time from low level
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
Δt_{PZH} ≡ change in t_{PZH} with load capacitance
Δt_{PZL} ≡ change in t_{PZL} with load capacitance
‡ Typical values are V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to Section 7.

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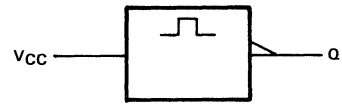
D2939, AUGUST 1986

SystemCell™ 2-μm HARDWIRED STANDARD CELL

- **Provides Initialization Pulse for Clearing/Presetting Registers**
- **Embedded Function — Requires No External Package Connection**
- **Automatically Triggered by Rising Edge of the 5-V Power-Up Supply Voltage**

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The SN54ASC2320 and SN74ASC2320 are dedicated, hardwired standard-cell macros implementing a positive-edge-triggered one-shot.

When the 'ASC2320 is embedded in a standard-cell design, its output rises with V_{CC}, then falls to a low level when V_{CC} reaches the trigger level V_1. As V_{CC} continues to rise, the pulse terminates and the output goes high when V_{CC} reaches V_2. Another pulse will be initiated only if V_{CC} falls below V_1. The duration of the low-level pulse is dependent on the rise time of the supply voltage. The output of the 'ASC2320 is used to initialize storage elements that can be preset or cleared asynchronously. For most applications, a single 'ASC2320 is adequate to execute the power-up initialization. The cell is designated and called from the engineering workstation using the following cell name and netlist label:

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
PUC00LH	Label: PUC00LH Q;	13.3

The SN54ASC2320 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC2320 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54ASC2320		SN74ASC2320		UNIT
			MIN	MAX	MIN	MAX	
V_1	Level of V_{CC} to initiate pulse	V_{CC} rising from 0 V to 4.5 V		2		2	V
V_2	Level of V_{CC} to terminate pulse	V_{CC} rising from 0 V to 4.5 V		4		4	V
I_{CC}	Supply current	V_{CC} = 4.5 V to 5.5 V		756		45.4	nA

output pulse characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS†	SN54ASC2320			SN74ASC2320			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{wQ}	V_{CC}	Q	t_r = 1 μs		0.5			0.5		μs
			t_r = 1 ms		0.28			0.28		ms
			t_r = 100 ms		26			26		ms

† Rise times are measured between the 0.5-V and 4.5-V points of V_{CC}.

D2939, AUGUST 1986

SystemCell™ 2-μm INTERNAL STANDARD CELL

- Symmetrical Delay Buffers ($t_{PLH} \approx t_{PHL}$)
- Choice of Inverting or Noninverting Delay Lines
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbols

BU110LH, BU112LH

BU111LH

positive logic equations

BU110LH, BU112LH: $Y = A$

BU111LH: $Y = \overline{A}$

description

The SN54ASC2321 and SN74ASC2321 are three internal delay buffer standard cells that provide the ASIC designer with symmetrical delay elements. Each option is designated and called from the engineering workstation input using the following cell names to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		TYPICAL DELAY C_L = 1 pF	RELATIVE CELL AREA TO NA210LH
BU110LH	Label: BU11nLH A,Y;	3 ns	2
BU111LH		4 ns	2
BU112LH		3 ns	2

The SN54ASC2321 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC2321 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS	BU110LH TYP	BU110LH MAX	BU111LH TYP	BU111LH MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current	SN54ASC2321	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0,		150		212	nA
		SN74ASC2321	T_A = MIN to MAX		9		12.7	
C_i	Input capacitance		V_{CC} = 5 V, T_A = 25°C	0.05		0.05		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, t_r = t_f = 3 ns, T_A = 25°C	0.74		0.83		pF

PARAMETER			TEST CONDITIONS	BU112LH TYP	BU112LH MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		V
I_{CC}	Supply current	SN54ASC2321	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0,		151	nA
		SN74ASC2321	T_A = MIN to MAX		9.1	
C_i	Input capacitance		V_{CC} = 5 V, T_A = 25°C	0.06		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, t_r = t_f = 3 ns, T_A = 25°C	0.56		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

BU110LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC2321 MIN	SN54ASC2321 TYP‡	SN54ASC2321 MAX	SN74ASC2321 MIN	SN74ASC2321 TYP‡	SN74ASC2321 MAX	UNIT
t_{PLH}	A	Y	C_L = 0	1	2	4.1	1.1	2	3.7	ns
t_{PHL}				1.4	2.4	5.1	1.4	2.4	4.6	
t_{PLH}	A	Y	C_L = 1 pF	1.5	3	6.4	1.7	3	5.8	ns
t_{PHL}				1.7	3.1	6.8	1.8	3.1	6.2	
Δt_{PLH}	A	Y		0.5	1	2.4	0.5	1	2.1	ns/pF
Δt_{PHL}				0.3	0.7	1.8	0.3	0.7	1.6	

BU111LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC2321 MIN	SN54ASC2321 TYP‡	SN54ASC2321 MAX	SN74ASC2321 MIN	SN74ASC2321 TYP‡	SN74ASC2321 MAX	UNIT
t_{PLH}	A	Y	C_L = 0	1.5	2.8	6.1	1.6	2.8	5.5	ns
t_{PHL}				1.5	3.1	7.2	1.6	3.1	6.5	
t_{PLH}	A	Y	C_L = 1 pF	2	3.8	8.4	2.2	3.8	7.6	ns
t_{PHL}				2	4.2	9.8	2.1	4.2	8.7	
Δt_{PLH}	A	Y		0.5	1	2.4	0.5	1	2.1	ns/pF
Δt_{PHL}				0.4	1	2.6	0.5	1	2.3	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are V_{CC} = 5 V, T_A = 25°C.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

BU112LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC2321			SN74ASC2321			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	C_L = 0	1	1.9	3.8	1.1	1.9	3.5	ns
t_{PHL}				1.1	2	4	1.1	2	3.7	
t_{PLH}	A	Y	C_L = 1 pF	1.5	2.9	6.2	1.7	2.9	5.6	ns
t_{PHL}				1.6	3	6.7	1.7	3	6	
Δt_{PLH}	A	Y		0.5	1	2.4	0.5	1	2.1	ns/pF
Δt_{PHL}				0.5	1	2.7	0.5	1	2.3	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to Section 7.

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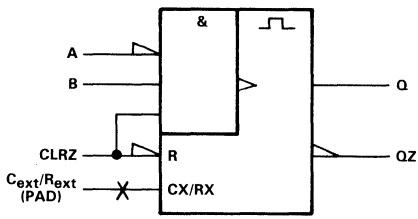
SystemCell™ 2-μm HARDWIRED STANDARD CELL

- **DC-Triggered from Active-High or Active-Low Logic Inputs**
- **Retriggerable for Very Long Output Pulses, Up to 100% Duty Cycle**
- **Overriding Clear Terminates Output Pulse**
- **Compensated for V_{CC} and Temperature Variations**
- **Incorporates Circuitry with C_{ext}/R_{ext} Pad to Protect against ESD and Latch-Up**

logic symbol



description

The SN54ASC2322 and SN74ASC2322 are hardwired standard cells implementing retriggerable monostable multivibrators similar to one-half of the 'LS123. The dc-triggered multivibrator features output pulse-duration control by any of the three following methods.

1. Pulse duration can be determined by external RC values following a trigger pulse at either A or B input.
2. Pulse duration can be extended by retriggering the A or B input.
3. Pulse duration can be determined (shortened) by triggering the clear input.

FUNCTION TABLE

INPUTS			OUTPUTS	
A	B	CLRZ	Q	QZ
X	X	L	L	H
H	X	X	L	H
X	L	X	L	H
L	↑	H	⎍	⎎
↓	H	H	⎍	⎎
L	H	↑	⎍	⎎

The C_{ext}/R_{ext} input pad incorporates circuit elements designed specifically to actively bypass and dissipate electrostatic discharges of potentials ranging up to 4 kilovolts. Guard-ring structures are employed that provide current management techniques for the cell to recover from exposure to large currents up to 400 milliamperes, thereby negating most common sources that can produce a latch-up condition.

The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist.

CELL NAME	NETLIST HDL LABEL	FEATURES	
		TYPICAL DELAY C_L = 1 pF	RELATIVE CELL AREA TO NA210LH
MVF00LH	Label: MVF00LH A,B,CLRZ,Q,QZ;	9 ns	100

C_{ext}/R_{ext} is a dedicated bonding pad for connection to an external package pin and is not available for netlist use.

The SN54ASC2322 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC2322 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

		SN54ASC2322		SN74ASC2322		UNIT
		MIN	MAX	MIN	MAX	
Input pulse duration, t_w	A low	9.4		7		ns
	B high	7.2		5.8		
	CLRZ low	7.2		5.8		
External timing resistance, R_{ext}		20		20		kΩ
External capacitance, C_{ext}		No restriction		No restriction		
Wiring capacitance at C_{ext}/R_{ext} terminal			50		50	pF

Also see Table 1 in Section 2

electrical characteristics

PARAMETER			TEST CONDITIONS		TYP	MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		V
I_{CC}	Supply current	SN54ASC2322	V_{CC} = 4.5 V to 5.5 V,			4419	nA
		SN74ASC2322	V_I = V_{CC} or 0,	T_A = MIN to MAX		265	
C_i	Input capacitance	A or B	V_{CC} = 5 V,	T_A = 25°C	0.16		pF
		CLRZ			0.2		
		C_{ext}/R_{ext}			5		
C_{pd}	Equivalent power dissapation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	20.5		pF

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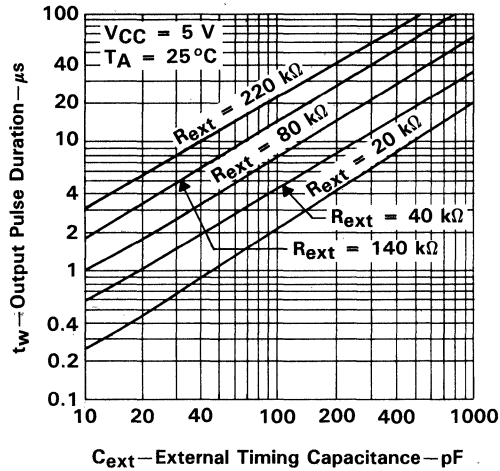
switching characteristics over recommended ranges of operating free-air temperature and supply voltage, C_{ext} = 0, and R_{ext} = 20 kΩ

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC2322			SN74ASC2322			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Q	C_L = 0	3.9	8.3	20.8	4.2	8.3	18.3	ns
t_{PHL}		QZ		3.8	8	20.1	4	8	17.7	
t_{PLH}	B	Q		3.6	7.7	19.3	3.9	7.7	17	ns
t_{PHL}		QZ		3.5	7.5	18.7	3.7	7.5	16.5	
t_{PHL}	CLRZ	Q		2.3	4.7	11.2	2.5	4.7	9.9	ns
t_{PLH}		QZ		2.1	4.2	10	2.2	4.2	8.9	
t_{PLH}	CLRZ	Q		4.2	9.5	24.2	4.6	9.5	21.3	ns
t_{PHL}		QZ		4.1	9.3	23.6	4.5	9.3	20.8	
t_{wQ}	A,B, or CLRZ	Q(H), QZ(L)	C_L = 1 pF	58	70	120	62	70	107	ns
t_{PLH}	A	Q		4.4	9.3	23.1	4.7	9.3	20.4	ns
t_{PHL}		QZ		4.1	8.7	22	4.4	8.7	19.4	
t_{PLH}	B	Q		4.1	8.7	21.6	4.4	8.7	19.1	ns
t_{PHL}		QZ		3.8	8.2	20.5	4.1	8.2	18.1	
t_{PHL}	CLRZ	Q		2.6	5.4	13	2.8	5.4	11.5	ns
t_{PLH}		QZ		2.6	5.2	12.3	2.8	5.2	11	
t_{PLH}	CLRZ	Q		4.7	10.5	26.5	5.2	10.5	23.4	ns
t_{PHL}		QZ		4.4	10	26.5	4.9	10	22.4	
Δt_{PLH}	Any	Q or		0.5	1	2.4	0.5	1	2.2	ns/pF
Δt_{PHL}		QZ		0.3	0.7	2	0.3	0.7	1.7	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
t_{wQ} ≡ output pulse duration
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TYPICAL OUTPUT PULSE DURATION
vs
EXTERNAL TIMING CAPACITANCE



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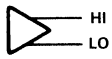
SystemCell™ 2-μm INTERNAL STANDARD CELL

- **Provides dc Termination for High- and Low-Level Unused Inputs**
- **Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V**
- **Provides Termination Over V_{CC} Range of 2 V to 6 V**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol



description

The SN54ASC2325 and SN74ASC2325 CMOS standard cell tie-off gates are offered specifically for managing unused inputs. The 'ASC2325 tie-off cells feature both high-logic-level HI and low-logic-level LO outputs each capable of handling all unused inputs encountered in virtually any ASIC design. Each cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
TO010LH	Label: TO010LH LO,HI;	1.5

The SN54ASC2325 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC2325 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
I_{CC} Supply current	SN54ASC2325	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0,		177	nA
	SN74ASC2325	T_A = MIN to MAX		10.6	
C_{pd} Equivalent power dissapation capacitance		V_{CC} = 5 V, t_r = t_f = 3 ns,	Nil		pF

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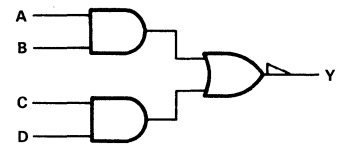
SystemCell™ 2-μm INTERNAL STANDARD CELL

- **Typical Propagation Delay: 2.6 ns with 1-pF Load**
- **Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V**
- **Functional Operation Over V_{CC} Range of 2 V to 6 V**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol



FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	Y
H	H	X	X	L
X	X	H	H	L
Any other combination				H

positive logic equation

$$Y = \overline{(A \cdot B) + (C \cdot D)}$$

description

The SN54ASC2330 and SN74ASC2330 are 2-wide, 2-input AND-NOR gate CMOS standard cells. Each cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		TYPICAL DELAY C_L = 1 pF	RELATIVE CELL AREA TO NA210LH
AO221LH	Label: AO221LH A,B,C,D,Y;	2.6 ns	2.7

The SN54ASC2330 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC2330 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS		TYP	MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		V
I_{CC}	Supply current	SN54ASC2330	V_{CC} = 4.5 V to 5.5 V,	V_I = V_{CC} or 0,		224	nA
		SN74ASC2330	T_A = MIN to MAX			13.4	
C_i	Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.13		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	0.59		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC2330			SN74ASC2330			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Any	Y	C_L = 0	0.7	1.2	2.9	0.8	1.2	2.6	ns
t_{PHL}				0.4	1.1	2.2	0.4	1.1	2	
t_{PLH}	Any	Y	C_L = 1 pF	1.7	3.2	7.3	1.8	3.2	6.7	ns
t_{PHL}				0.9	2	4.6	0.9	2	4.1	
Δt_{PLH}	Any	Y		0.9	2	4.6	1	2	4.1	ns/pF
Δt_{PHL}				0.5	0.9	2.5	0.5	0.9	2.2	

† Propagation delay times are measured from 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to Section 7.

All inputs to this cell, as well as all cells, must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

This Boolean function is a member of a series of multifunction cells designed specifically to simplify the implementation of a broad class of higher-level logic equations such as:

- Sum of products
- Exclusive-OR and exclusive-NOR functions
- Majority decoders
- Modulo adders
- Carry-save adders
- Function generators
- Random logic

Other members of this class of standard-cell functions are grouped in the 'ASC6000 series of type numbers. The selection consists of four primary architectures with expandable versions offered in each:

- Dedicated and expandable AND-NOR gates
- Dedicated and expandable OR-AND-NOR gates
- Expandable AND-OR-NOR gates
- Expandable OR-NAND gates
- Expandable AND-OR-NAND gates
- Expandable OR-AND-OR-NAND gates

Options are offered in each architecture from basic 2-wide functions up to expandable 3-wide functions providing single-macro solution to most design requirements. The expandable functions can be combined with basic gating cells and/or other Boolean cells offered in Texas Instruments SystemCell™ family to implement application-specific solutions.

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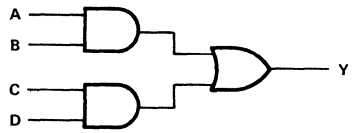
SystemCell™ 2-μm INTERNAL STANDARD CELL

- **Typical Propagation Delay: 2.6 ns with 1-pF Load**
- **Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V**
- **Functional Operation Over V_{CC} Range of 2 V to 6 V**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol



FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	Y
H	H	X	X	H
X	X	H	H	H
Any other combination				L

positive logic equation

$Y = (A \cdot B) + (C \cdot D)$

description

The SN54ASC2331 and SN74ASC2331 are 2-wide, 2-input AND-OR gate CMOS standard cells. Each cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		TYPICAL DELAY C_L = 1 pF	RELATIVE CELL AREA TO NA210LH
AO220LH	Label: AO220LH A,B,C,D,Y;	2.6 ns	3.1

The SN54ASC2331 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC2331 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS		TYP	MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		V
I_{CC}	Supply current	SN54ASC2331	V_{CC} = 4.5 V to 5.5 V,	V_I = V_{CC} or 0,		255	nA
		SN74ASC2331	T_A = MIN to MAX			15.3	
C_i	Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.13		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	0.9		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC2331			SN74ASC2331			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Any	Y	C_L = 0	0.4	1.3	3.2	0.5	1.3	2.9	ns
t_{PHL}				1	2	4.9	1	2	4.4	
t_{PLH}	Any	Y	C_L = 1 pF	1	2.3	5.6	1.1	2.3	5	ns
t_{PHL}				1.4	2.8	6.9	1.4	2.8	6.2	
Δt_{PLH}	Any	Y		0.5	1	2.4	0.5	1	2.1	ns/pF
Δt_{PHL}				0.3	0.8	2	0.4	0.8	1.8	

† Propagation delay times are measured from 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATION

Refer to Section 7 and the ASC2330 data sheet.

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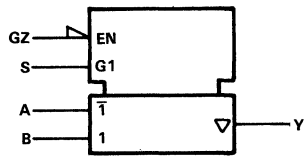
SystemCell™ 2-μm HARDWIRED MACRO CELL

- **3.7 ns Typical Propagation Delay with 1-pF Load**
- **Active-Low Enable for Expandability**
- **Use Parallel Decoders for Multiple-Bit Words**
- **High Density for Use in Cost-Efficient VLSI ASICs**

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The SN54ASC2340 and SN74ASC2340 are standard-cell dedicated macros that are implemented as 2-line to 1-line multiplexers. The 'ASC2340 implements a function table similar to packaged ICs such as one-fourth of the 'LS157, 'S157, and 'F157.

The macro has an enable input, GZ, that enables and disables the output. The output is at a high impedance when GZ is high. When GZ is low, the output assumes the level of the selected input. This enable permits the macro to be employed for designing wider multiplexers as only the enabled 2-bit field will output an active data bit. Each cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

FUNCTION TABLE

INPUTS		OUTPUT
S	GZ	Y
X	H	Z
L	L	A
H	L	B

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
MU110LH	Label: MU110LH A,B,S,GZ,Y;	3.7

The SN54ASC2340 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC2340 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS		SN54ASC2340		SN74ASC2340		UNIT
					TYP	MAX	TYP	MAX	
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX	V_I = V_{CC} or 0,		435		26.1	nA
C_i	Input capacitance	A, B	V_{CC} = 5 V,	T_A = 25°C	0.24		0.24		pF
		S			0.21		0.21		
		GZ			0.21		0.21		
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	0.92		0.92		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC2340			SN74ASC2340			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A or B	Y	C_L = 0	0.7	1.7	4.1	0.8	1.7	3.8	ns
t_{PHL}				0.8	1.5	3.6	0.9	1.5	3.2	
t_{PLH}	A or B	Y	C_L = 1 pF	1.7	3.6	8.5	1.8	3.6	7.7	ns
t_{PHL}				1.2	2.4	5.7	1.3	2.4	5.1	
t_{PLH}	S	Y	C_L = 0	1.1	2.4	5.3	1.2	2.4	4.8	ns
t_{PHL}				1.1	2.1	5	1.2	2.1	4.4	
t_{PLH}	S	Y	C_L = 1 pF	2	4.3	9.7	2.2	4.3	8.8	ns
t_{PHL}				1.5	3	7.1	1.7	3	6.4	
t_{PZH}	GZ	Y	C_L = 1 pF, R_L = 1 kΩ to GND	1.3	2.5	5.5	1.4	2.5	5	ns
t_{PZL}	GZ	Y	C_L = 1 pF, R_L = 1 kΩ to V_{CC}	1	2	4.6	1.1	2	4.3	ns
t_{PHZ}	GZ	Y	C_L = 1 pF, R_L = 40 kΩ to GND		7.6			7.6		ns
t_{PLZ}	GZ	Y	C_L = 1 pF, R_L = 20 kΩ to V_{CC}		4.5			4.5		ns
Δt_{PLH}	A or B	Y		0.9	1.9	4.4	1	1.9	4	ns/pF
Δt_{PHL}				0.3	0.9	2.2	0.4	0.9	2	
Δt_{PLH}	S	Y		0.9	1.9	4.4	1	1.9	4	ns/pF
Δt_{PHL}				0.5	0.9	2.2	0.5	0.9	2	
Δt_{PZH}	GZ	Y		0.9	2	4.6	1	2	4.1	ns/pF
Δt_{PZL}				0.3	0.9	2.8	0.3	0.9	2.4	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
t_{PHZ} ≡ output disable time from high level
t_{PLZ} ≡ output disable time from low level
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
Δt_{PZH} ≡ change in t_{PZH} with load capacitance
Δt_{PZL} ≡ change in t_{PZL} with load capacitance
‡ Typical values are V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to Section 7.

interfacing the macro

Inputs and outputs of the predesigned macro are compatible for interfacing directly with cells and macros available in the TI standard-cell library. The inputs can be driven by either inverting or noninverting input cells. The outputs can be interfaced to drive off-chip loads with any of the noninverting output buffers or interfaced to external bidirectional buses through a 3-state input/output TTL/CMOS standard-cell buffer.

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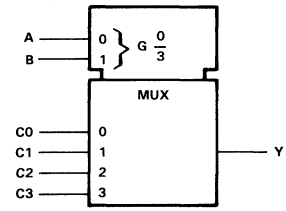
D2939, AUGUST 1986

SystemCell™ 2-μm HARDWIRED MACRO CELL

- **Typical Propagation Delay: 2.9 ns with 1-pF Load**
- **Use Parallel Decoders for Multiple-Bit Words**
- **High Density for Use In Cost-Efficient VLSI ASIC's**

logic symbol†



† This symbol is in accordance with IEEE ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE

INPUTS		OUTPUT
B	A	Y
L	L	C0
L	H	C1
H	L	C2
H	H	C3

description

The SN54ASC2341 and SN74ASC2341 are standard-cell dedicated macros implementing 4-line to 1-line multiplexers. The 'ASC2341 implements a function table similar to that performed by packaged ICs such as one-half of the 'LS153, 'S153, and 'F153. Each cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
MU210LH	Label: MU210LH A,B,C0,C1,C2,C3,Y;	5

The SN54ASC2341 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC2341 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER		TEST CONDITIONS	SN54ASC2341		SN74ASC2341		UNIT
			TYP	MAX	TYP	MAX	
V_T Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC} Supply current		V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		586		35.2	nA
C_i Input capacitance	A or B	V_{CC} = 5 V, T_A = 25°C	0.28		0.28		pF
	C0,C1,C2,C3		0.22		0.22		
C_{pd} Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C, t_r = t_f = 3 ns,	1.28		1.28		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC2341			SN74ASC2341			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	C0,C1,C2,C3	Y	C_L = 0	1	2	4.4	1	2	3.9	ns
t_{PHL}				1.1	2.1	4.6	1.2	2.1	4.2	
t_{PLH}	C0,C1,C2,C3	Y	C_L = 1 pF	1.5	3	6.7	1.6	3	6	ns
t_{PHL}				1.5	2.8	6.3	1.6	2.8	5.6	
t_{PLH}	A, B	Y	C_L = 0	0.5	1.8	5.6	0.5	1.8	5.1	ns
t_{PHL}				1	2.1	6.3	1	2.1	5.6	
t_{PLH}	A, B	Y	C_L = 1 pF	1	2.8	7.9	1.1	2.8	7.1	ns
t_{PHL}				1.3	2.8	7.9	1.3	2.8	7.1	
Δt_{PLH}	C0,C1,C2,C3	Y		0.5	1	2.3	0.5	1	2.1	ns/pF
Δt_{PHL}				0.3	0.7	1.7	0.3	0.7	1.5	
Δt_{PLH}	A, B	Y		0.5	1	2.3	0.5	1	2.1	ns/pF
Δt_{PHL}				0.3	0.7	1.7	0.3	0.7	1.5	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to Section 7.

interfacing the macro

Inputs and outputs of the predesigned macro are compatible for interfacing directly with cells and macros available in the TI standard-cell library. The inputs can be driven by either noninverting or inverting input cells. The outputs can be interfaced to drive off-chip loads with any of the noninverting output buffers or interfaced to external bidirectional buses through a 3-state input/output TTL/CMOS standard cell buffer.

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D2939, AUGUST 1986

SystemCell™ 2-μm HARDWIRED MACRO CELL

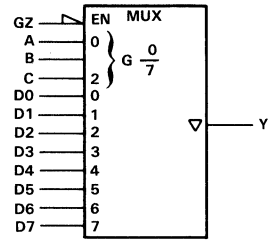
- **4.7 ns Typical Propagation Delay with 1-pF Load**
- **Active-Low Enable for Expandability**
- **Uses Parallel Decoders for Multiple-Bit Words**
- **High Density for Use in Cost-Efficient VLSI ASICs**

description

The SN54ASC2342 and SN74ASC2342 are standard-cell dedicated macros that are implemented as 8-line to 1-line multiplexers. The ASC2342 implements a function table similar to packaged ICs such as the 'LS151, 'S151, and 'F151.

The macro has an enable input, GZ, that enables and disables the output. The output is at a high impedance when GZ is high. When GZ is low, the output assumes the level of the selected bit. This enable permits the macro to be employed for designing wider multiplexers, as only the enabled 8-bit field will output an active data bit. Each cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE

INPUTS				OUTPUT
C	B	A	GZ	Y
X	X	X	H	Z
L	L	L	L	D0
L	L	H	L	D1
L	H	L	L	D2
L	H	H	L	D3
H	L	L	L	D4
H	L	H	L	D5
H	H	L	L	D6
H	H	H	L	D7

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
MU310LH	Label: MU310LH A,B,C,D0,D1,D2,D3,D4,D5,D6,D7,GZ,Y;	15.7

The SN54ASC2342 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC2342 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS		SN54ASC2342		SN74ASC2342		UNIT
					TYP	MAX	TYP	MAX	
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX	V_I = V_{CC} or 0,		1748		105	nA
C_i	Input capacitance	D0 thru D7	V_{CC} = 5 V,	T_A = 25°C	0.2		0.2		pF
		A or C			0.25		0.25		
		B			0.12		0.12		
		GZ			0.21		0.21		
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	1.68		1.68		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC2342			SN74ASC2342			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	D0 thru D7	Y	C_L = 0	1.5	3	7.5	1.6	3	6.7	ns
t_{PHL}				1.6	3.2	8	1.7	3.2	7.1	
t_{PLH}	D0 thru D7	Y	C_L = 1 pF	2.5	5	12	2.7	5	10.7	ns
t_{PHL}				2.2	4.4	10.7	2.3	4.4	9.5	
t_{PLH}	A, B, or C	Y	C_L = 0	0.7	3	9.8	0.8	3	8.7	ns
t_{PHL}				1.1	3.3	10.2	1.1	3.3	9.1	
t_{PLH}	A, B, or C	Y	C_L = 1 pF	1.7	5	14.3	1.8	5	12.8	ns
t_{PHL}				1.6	4.4	12.9	1.7	4.4	11.5	
t_{PZH}	GZ	Y	C_L = 1 pF, R_L = 1 kΩ to GND	1.2	2.6	6.1	1.3	2.6	5.5	ns
t_{PZL}	GZ	Y	C_L = 1 pF, R_L = 1 kΩ to V_{CC}	1	2	5	1.1	2	4.4	ns
t_{PHZ}	GZ	Y	C_L = 1 pF, R_L = 40 kΩ to GND		8.3			8.3		ns
t_{PLZ}	GZ	Y	C_L = 1 pF, R_L = 20 kΩ to V_{CC}		4.6			4.6		ns
Δt_{PLH}	D0 thru D7	Y		0.9	2	4.5	1	2	4.1	ns/pF
Δt_{PHL}				0.5	1.2	2.8	0.5	1.2	2.5	
Δt_{PLH}	A, B, or C	Y		0.9	2	4.5	1	2	4.1	ns/pF
Δt_{PHL}				0.5	1.1	2.7	0.5	1.1	2.4	
Δt_{PZH}	GZ	Y		0.9	2	4.7	1	2	4.2	ns/pF
Δt_{PZL}				0.3	1	2.9	0.3	1	2.6	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
t_{PHZ} ≡ output disable time from high level
t_{PLZ} ≡ output disable time from low level
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
Δt_{PZH} ≡ change in t_{PZH} with load capacitance
Δt_{PZL} ≡ change in t_{PZL} with load capacitance
‡ Typical values are V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to Section 7.

interfacing the macro

Inputs and outputs of the predesigned macro are compatible for interfacing directly with cells and macros available in the TI standard-cell library. The inputs can be driven by either inverting or noninverting input cells. The outputs can be interfaced to drive off-chip loads with any of the noninverting output buffers or interfaced to external bidirectional buses through a 3-state input/output TTL/CMOS standard-cell buffer.

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

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D2939, AUGUST 1986

SystemCell™ 2-μm HARDWIRED MACRO CELL

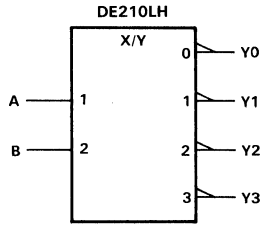
- **Macro DE212LH Features Active-Low Enable for Expandability**
- **Use Parallel Decoders for Multiple-Bit Words**
- **High Density for Use in Cost-Efficient VLSI ASICs**

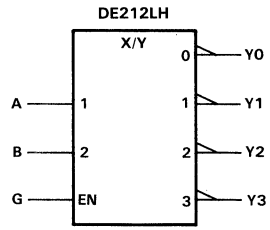
description

The SN54ASC2350 and SN74ASC2350 are standard-cell dedicated macros implementing 2-line to 4-line decoders/demultiplexers. The DE212LH implements a function table similiar to that performed by packaged ICs such as the 'LS139A, 'S139, and 'F139.

The DE212LH macro has an output control, G, that enables and disables the outputs. All of the outputs are high when G is low. When G is high, the selected output assumes a low-logic level. This enable permits the DE212LH macro to be employed for designing wider multiplexers, as only the enabled 4-bit field will contain an active data bit. Each macro is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

logic symbols†





† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

CELL NAME	NETLIST HDL LABEL	FEATURES	
		TYPICAL DELAY C_L = 1 pF	RELATIVE CELL AREA TO NA210LH
DE210LH	Label: DE210LH A,B,Y0,Y1,Y2,Y3;	2 ns	4.25
DE212LH	Label: DE212LH A,B,G,Y0,Y1,Y2,Y3;	2.5 ns	5.25

The SN54ASC2350 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC2350 is characterized for operation from −40°C to 85°C.

FUNCTION TABLES

DE210LH

INPUTS		OUTPUTS			
A	B	Y0	Y1	Y2	Y3
L	L	L	H	H	H
H	L	H	L	H	H
L	H	H	H	L	H
H	H	H	H	H	L

DE212LH

INPUTS			OUTPUTS			
A	B	G	Y0	Y1	Y2	Y3
X	X	L	H	H	H	H
L	L	H	L	H	H	H
H	L	H	H	L	H	H
L	H	H	H	H	L	H
H	H	H	H	H	H	L

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

DE210LH

PARAMETER		TEST CONDITIONS		SN54ASC2350		SN74ASC2350		UNIT
				TYP	MAX	TYP	MAX	
V_T	Input threshold voltage	V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current	V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX	V_I = V_{CC} or 0,		464		27.9	nA
C_i	Input capacitance	V_{CC} = 5 V,	T_A = 25°C	0.37		0.37		pF
C_{pd}	Equivalent power dissipation capacitance	V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	2.91		2.91		pF

DE212LH

PARAMETER			TEST CONDITIONS		SN54ASC2350		SN74ASC2350		UNIT
					TYP	MAX	TYP	MAX	
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX	V_I = V_{CC} or 0,		582		34.9	nA
C_i	Input capacitance	A, B	V_{CC} = 5 V,	T_A = 25°C	0.37		0.37		pF
		G			0.5		0.5		
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	2.81		2.81		pF

TEXAS INSTRUMENTS
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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

DE210LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC2350			SN74ASC2350			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A or B	Yn	C_L = 0	0.6	1	3.2	0.7	1	2.9	ns
t_{PHL}				0.5	1	3.3	0.5	1	3	
t_{PLH}	A or B	Yn	C_L = 1 pF	1.1	2	5.4	1.2	2	5	ns
t_{PHL}				1	2	6	1.1	2	5.3	
Δt_{PLH}	A or B	Yn		0.4	1	2.7	0.5	1	2.4	ns/pF
Δt_{PHL}				0.4	1	2.7	0.4	1	2.4	

DE212LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC2350			SN74ASC2350			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A or B	Yn	C_L = 0	0.7	1.3	3.3	0.7	1.3	3	ns
t_{PHL}				0.6	1.1	4.1	0.7	1.1	3.6	
t_{PLH}	G	Yn		0.7	1	1.9	0.8	1	1.8	ns
t_{PHL}				0.5	1	2.2	0.6	1	2	
t_{PLH}	A or B	Yn	C_L = 1 pF	1.2	2.4	5.6	1.3	2.4	5.1	ns
t_{PHL}				1.3	2.5	7.8	1.4	2.5	6.8	
t_{PLH}	G	Yn		1.2	2	4.1	1.3	2	3.8	ns
t_{PHL}				1.2	2.4	6	1.3	2.4	5.2	
Δt_{PLH}	A or B	Yn		0.5	1.1	3	0.5	1.1	2.8	ns/pF
Δt_{PHL}				0.6	1.4	3.8	0.7	1.4	3.3	
Δt_{PLH}	G	Yn		0.4	1	2.2	0.5	1	2	ns/pF
Δt_{PHL}				0.6	1.4	3.8	0.7	1.4	3.3	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

interfacing the macro

Inputs and outputs of the predesigned macro are compatible for interfacing directly with cells and macros available in the TI standard cell library. For the input data words, the inputs can be driven by either inverting or noninverting input cells.

The outputs can be interfaced to drive off-chip loads with any of the noninverting output buffers or interfaced to external bidirectional buses through a 3-state input/output TTL/CMOS buffer.

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design.

TEXAS INSTRUMENTS
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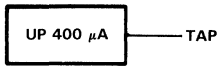
D2939, AUGUST 1986

SystemCell™ 2-μm INTERNAL MACRO CELL

- Provides Active Termination for Inputs or I/Os
- Embedded Function — Requires No External Connection
- Prevents Inputs or I/Os from "Floating"
- ESD and Latch-Up Protected by Input or I/O Cell

logic symbol



description

The SN54ASC2370 and SN74ASC2370 are dedicated, hardwired, standard-cell pull-up terminators that can be incorporated into an ASIC design on input or I/O cells having a pull-up tap. The input or I/O tap enables connection of this active pull-up terminator. When the terminator is used, it ensures the input or I/O will be driven to a high logic level, thereby avoiding exposure to a high-impedance or floating condition. Each cell is designated and called from the engineering workstation input using the following cell name to develop a label for the design netlist:

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
PR400LH	Label: PR400LH TAP;	4.7

The SN54ASC2370 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC2370 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54ASC2370			SN74ASC2370			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
I_O	Output current	V_O = 4 V	−75	−272	−730	−84	−272	−675	μA
		V_O = 2.5 V	−225	−515	−1114	−250	−515	−1032	
		V_O = 0	−283	−612	−1289	−313	−612	−1194	
I_{CC}	Supply current	V_I = V_{CC} or 0			147			8.85	nA

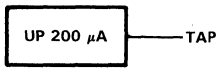
† Typical values are at V_{CC} = 5 V, T_A = 25°C.

D2939, AUGUST 1986

SystemCell™ 2-μm INTERNAL MACRO CELL

- **Provides Active Termination for Inputs or I/Os**
- **Embedded Function — Requires No External Connection**
- **Prevents Inputs or I/Os from "Floating"**
- **ESD and Latch-Up Protected by Input or I/O Cell**

logic symbol



description

The SN54ASC2371 and SN74ASC2371 are dedicated, hardwired, standard-cell pull-up terminators that can be incorporated into an ASIC design on input or I/O cells having a pull-up tap. The input or I/O tap enables connection of this active pull-up terminator. When the terminator is used, it ensures the input or I/O will be driven to a high-logic level, thereby avoiding exposure to a high-impedance or floating condition. Each cell is designated and called from the engineering workstation input using the following cell name to develop a label for the design netlist:

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
PR250LH	Label: PR250LH TAP;	5

The SN54ASC2371 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC75 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54ASC2371			SN74ASC2371			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
I_O	Output current	V_O = 4 V	−36	−125	−322	−40	−125	−297	μA
		V_O = 2.5 V	−107	−235	−489	−118	−235	−452	
		V_O = 0	−134	−279	−565	−148	−279	−523	
I_{CC}	Supply current	V_I = V_{CC} or 0			158			9.48	nA

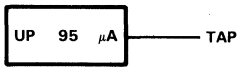
† Typical values are at V_{CC} = 5 V, T_A = 25°C.

D2939, AUGUST 1986

SystemCell™ 2-μm INTERNAL MACRO CELL

- **Provides Active Termination for Inputs or I/Os**
- **Embedded Function — Requires No External Connection**
- **Prevents Inputs or I/Os from "Floating"**
- **ESD and Latch-Up Protected by Input or I/O Cell**

logic symbol



description

The SN54ASC2372 and SN74ASC2372 are dedicated, hardwired, standard-cell pull-up terminators that can be incorporated into an ASIC design on input or I/O cells having a pull-up tap. The input or I/O tap enables connection of this active pull-up terminator. When the terminator is used, it ensures the input or I/O will be driven to a high logic level, thereby avoiding exposure to a high-impedance or floating condition. Each cell is designated and called from the engineering workstation input using the following cell name to develop a label for the design netlist:

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
PR095LH	Label: PR095LH TAP;	5.5

The SN54ASC2372 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC2372 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54ASC2372			SN74ASC2372			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
I_O	Output current	V_O = 4 V	−17	−60	−152	−19	−60	−140	μA
		V_O = 2.5 V	−52	−113	−230	−58	−113	−213	
		V_O = 0	−65	−134	−266	−72	−134	−246	
I_{CC}	Supply current	V_I = V_{CC} or 0			183			11	nA

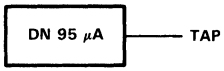
† Typical values are at V_{CC} = 5 V, T_A = 25°C.

D2939, AUGUST 1986

SystemCell™ 2-μm INTERNAL MACRO CELL

- **Provides Active Termination for Inputs or I/Os**
- **Embedded Function — Requires No External Connection**
- **Prevents Inputs or I/Os from "Floating"**
- **ESD and Latch-Up Protected by Input or I/O Cell**

logic symbol



description

The SN54ASC2373 and SN74ASC2373 are dedicated, hardwired, standard-cell pull-down terminators that can be incorporated into an ASIC design on input or I/O cells having a tap. The input or I/O tap enables connection of this active pull-down terminator. When the terminator is used, it ensures the input or I/O will be driven to a low-logic level, thereby avoiding exposure to a high-impedance or floating condition. Each cell is designated and called from the engineering workstation input using the following cell name to develop a label for the design netlist:

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
PD095LH	Label: PD095LH TAP;	4.7

The SN54ASC2373 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC2373 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54ASC2373			SN74ASC2373			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
I_O	Output current	V_O = 1 V	37	79	163	43	79	147	μA
		V_O = 2.5 V	57	126	275	66	126	247	
		V_O = 4.5	61	137	297	71	137	267	
I_{CC}	Supply current	V_I = V_{CC} or 0			194			11.7	nA

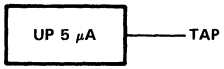
† Typical values are at V_{CC} = 5 V, T_A = 25°C.

D2939, AUGUST 1986

SystemCell™ 2-μm INTERNAL MACRO CELL

- **Provides Active Termination for Inputs or I/Os**
- **Embedded Function — Requires No External Connection**
- **Prevents Inputs or I/Os from "Floating"**
- **ESD and Latch-Up Protected by Input or I/O Cell**

logic symbol



description

The SN54ASC2374 and SN74ASC2374 are dedicated, hardwired, standard-cell pull-up terminators that can be incorporated into an ASIC design on input or I/O cells having a pull-up tap. The input or I/O tap enables connection of this active pull-up terminator. When the terminator is used, it ensures the input or I/O will be driven to a high-logic level, thereby avoiding exposure to a high-impedance or floating condition. Each cell is designated and called from the engineering workstation input using the following cell name to develop a label for the design netlist:

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
PR005LH	Label: PR005LH TAP;	6.2

The SN54ASC2374 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC2374 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54ASC2374			SN74ASC2374			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
I_O	Output current	V_O = 4 V	−0.4	−1.5	−4.1	−0.4	−1.5	−3.8	μA
		V_O = 2.5 V	−1.1	−2.8	−6.4	−1.3	−2.8	−5.9	
		V_O = 0	−1.4	−3.2	−7.1	−1.5	−3.2	−6.6	
I_{CC}	Supply current	V_I = V_{CC} or 0			208			12.5	nA

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

SystemCell™ 2-μm HARDWIRED MACRO CELL

- **Designed for Implementing Serial/Parallel Registers**
- **Choice of Four Versions to Achieve Best Design Density**
- **Embedded Clock Drivers Provide Clock Buffering**

SHIFT REGISTER CONFIGURATIONS

CELL TYPE	INPUTS		COMPLEMENTARY OUTPUTS	ASYNCHRONOUS CLEAR
	SERIAL	PARALLEL		
'ASC2401	yes	no	no	yes
'ASC2402	yes	no	yes	yes
'ASC2403	yes	yes	no	no
'ASC2404	yes	yes	yes	no

description

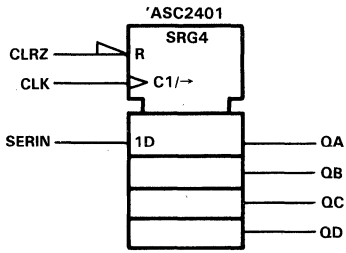
The 'ASC2401 thru 'ASC2404 are dedicated, hardwired standard-cell macros implementing four 4-bit shift register cells. The four register configurations provide the custom IC designer register elements to embed in ASICs in their most efficient form. Their 4-bit length means that larger blocks of custom logic can be handled efficiently to construct large registers.

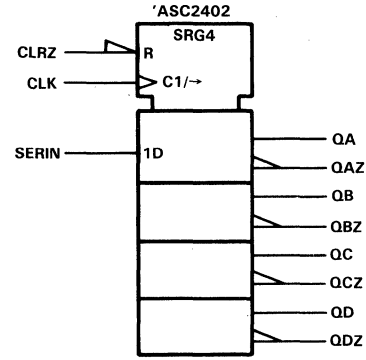
The macros each contain an embedded clock driver that buffers the clock input to a single 2-line input. This further simplifies implementaion of longer registers, as standard library buffer cells can be used to drive multiple clock inputs, which are used in the longer registers. The macro cells are identified and called from the engineering workstation input using the cell names and netlists in conjunction with labels developed as shown in the following table:

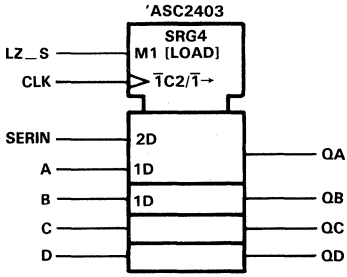
CELL NAME	NETLIST HDL LABEL	FEATURES	
		MAXIMUM CLOCK FREQUENCY	RELATIVE CELL AREA TO NA210LH
R2401LH	Label: R2401LH CLRZ,SERIN,CLK,QA,QB,QC,QD;	59.6 MHz	25.25
R2402LH	Label: R2402LH CLRZ,SERIN,CLK,QA,QAZ,QB,QBZ,QC,QCZ,QD,QDZ;	59.6 MHz	28.25
R2403LH	Label: R2403LH SERIN,LZ_S,CLK,A,B,C,D,QA,QB,QC,QD;	59.6 MHz	31.25
R2404LH	Label: R2404LH SERIN,LZ_S,CLK,A,B,C,D,QA,QAZ,QB,QBZ,QC,QCZ,QD,QDZ;	59.6 MHz	34.25

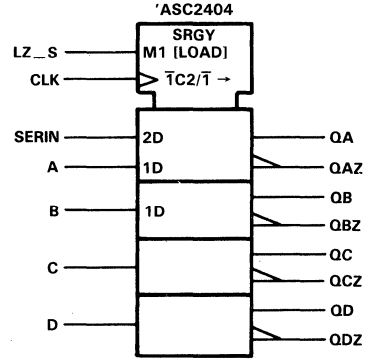
The SN54ASC' cells are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC' cells are characterized for operation from −40°C to 85°C.

logic symbols†









† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLES

'ASC2401, 'ASC2402

INPUTS			OUTPUTS			
CLRZ	CLK	SERIN	QA‡	QB‡	QC‡	QD‡
L	X	X	L	L	L	L
H	↑	H	H	QA_n	QB_n	QC_n
H	↑	L	L	QA_n	QB_n	QC_n
H	L	X	Q_0	Q_0	Q_0	Q_0

'ASC2403,'ASC2404

INPUTS							OUTPUTS			
			DATA							
LZ_S	CLK	SERIN	A	B	C	D	QA‡	QB‡	QC‡	QD‡
L	↑	X	a	b	c	d	a	b	c	d
H	↑	H	X	X	X	X	H	QA_n	QB_n	QC_n
H	↑	L	X	X	X	X	L	QA_n	QB_n	QC_n
X	L	X	X	X	X	X	Q_0	Q_0	Q_0	Q_0

‡ The 'ASC2402 and 'ASC2404 QxZ output is the complement of Qx.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			R2401LH				R2402LH				UNIT
			SN54'		SN74'		SN54'		SN74'		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	59.6	0	59.6	0	59.6	0	59.6	MHz
t_w	Pulse duration	CLRZ low	5.4		5.4		6.6		6.6		ns
		CLK high	8.4		8.4		8.4		8.4		
		CLK low	8.4		8.4		8.4		8.4		
t_{su}	Setup time before clock	SERIN (H or L)	5.8		5.8		5.8		5.8		ns
		CLRZ inactive	−3		−3		−3		−3		
t_h	Hold time after clock	SERIN (H or L)	0.2		0.2		0.2		0.3		ns
		CLRZ active	5.4		5.4		5.4		5.4		

			R2403LH				R2404LH				UNIT
			SN54'		SN74'		SN54'		SN74'		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	59.6	0	59.6	0	59.6	0	59.6	MHz
t_w	Pulse duration	CLK high	8.4		8.4		8.4		8.4		ns
		CLK low	8.4		8.4		8.4		8.4		
t_{su}	Setup time before clock	SERIN (H or L)	5.8		5.8		5.8		5.7		ns
		LZ_S (H or L)	0		0		0		0		
		A..D (H or L)	5.8		5.8		5.8		5.7		
t_h	Hold time after clock	SERIN (H or L)	−0.4		−0.3		−0.4		−0.3		ns
		LZ_S (H or L)	0		0		0		0		
		A..D (H or L)	−0.3		−0.3		−0.4		−0.3		

electrical characteristics

R2401LH

PARAMETER			TEST CONDITIONS		SN54ASC2401 TYP	SN54ASC2401 MAX	SN74ASC2401 TYP	SN74ASC2401 MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX	V_I = V_{CC} or 0,		3071		184	nA
C_i	Input capacitance	CLRZ	V_{CC} = 5 V,	T_A = 25°C	1.04		1.04		pF
		SERIN			0.13		0.13		
		CLK			0.24		0.24		
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	10.3		10.3		pF

R2402LH

PARAMETER			TEST CONDITIONS		SN54ASC2402 TYP	SN54ASC2402 MAX	SN74ASC2402 TYP	SN74ASC2402 MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX	V_I = V_{CC} or 0,		3355		202	nA
C_i	Input capacitance	CLRZ	V_{CC} = 5 V,	T_A = 25°C	1.04		1.04		pF
		SERIN			0.13		0.13		
		CLK			0.24		0.24		
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	12.1		12.1		pF

R2403LH

PARAMETER			TEST CONDITIONS		SN54ASC2403 TYP	SN54ASC2403 MAX	SN74ASC2403 TYP	SN74ASC2403 MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX	V_I = V_{CC} or 0,		3711		223	nA
C_i	Input capacitance	SERIN	V_{CC} = 5 V,	T_A = 25°C	0.19		0.19		pF
		LZ_S			0.8		0.8		
		CLK			0.24		0.24		
		Dn			0.19		0.19		
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	11.1		11.1		pF

R2404LH

PARAMETER			TEST CONDITIONS		SN54ASC2404 TYP	SN54ASC2404 MAX	SN74ASC2404 TYP	SN74ASC2404 MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX	V_I = V_{CC} or 0,		3995		240	nA
C_i	Input capacitance	SERIN	V_{CC} = 5 V,	T_A = 25°C	0.19		0.19		pF
		LZ_S			0.8		0.8		
		CLK			0.24		0.24		
		Dn			0.19		0.19		
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	12.1		12.1		pF

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

R2401LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC2401			SN74ASC2401			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	CLK	Q	C_L = 0	3.6	5.7	11.1	4.1	5.7	10.1	ns
t_{PHL}				2.4	4.7	10.2	2.8	4.7	9.3	
t_{PHL}	CLRZ	Q		1.2	1.9	3.9	1.5	1.9	3.6	ns
t_{PLH}	CLK	Q	C_L = 1 pF	3.9	6.2	12.3	4.4	6.2	11.2	ns
t_{PHL}				2.7	5.2	11.1	3.1	5.2	10	
t_{PHL}	CLRZ	Q		1.5	2.4	4.7	1.8	2.4	4.4	ns
Δt_{PLH}	CLK	Q		0.3	0.5	1.3	0.3	0.5	1.1	ns/pF
Δt_{PHL}				0.3	0.5	0.9	0.3	0.5	0.8	
Δt_{PHL}	CLRZ	Q		0.3	0.5	0.9	0.3	0.5	0.8	ns/pF

R2402LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC2402			SN74ASC2402			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	CLK	Q	C_L = 0	3.7	5.9	11.6	3.9	5.9	10.5	ns
t_{PHL}				2.5	4.9	10.5	2.6	4.9	9.5	
t_{PLH}	CLK	QZ		2.7	5.3	11.1	2.9	5.3	10.1	ns
t_{PHL}				3.8	6.1	12.2	4.1	6.1	11.1	
t_{PLH}	CLRZ	QZ		1.5	2.5	4.7	1.6	2.5	4.5	ns
t_{PHL}	CLRZ	Q		1.3	2.1	4.1	1.3	2.1	3.9	ns
t_{PLH}	CLK	Q	C_L = 1 pF	4	6.4	12.8	4.2	6.4	11.6	ns
t_{PHL}				2.7	5.3	11.3	2.9	5.3	10.2	
t_{PLH}	CLK	QZ		3.3	6.3	13.5	3.5	6.3	12.1	ns
t_{PHL}				4.3	7.2	14.8	4.7	7.2	13.4	
t_{PLH}	CLRZ	QZ		2.1	3.5	6.9	2.2	3.5	6.5	ns
t_{PHL}	CLRZ	Q		1.5	2.5	4.9	1.6	2.5	4.6	ns
Δt_{PLH}	CLK	Q		0.3	0.5	1.2	0.3	0.5	1.1	ns/pF
Δt_{PHL}				0.2	0.4	0.8	0.3	0.4	0.8	
Δt_{PLH}	CLK	QZ		0.6	1	2.3	0.6	1	2	ns/pF
Δt_{PHL}				0.5	1.1	2.7	0.6	1.1	2.4	
Δt_{PLH}	CLRZ	QZ		0.6	1	2.3	0.6	1	2	ns/pF
Δt_{PHL}	CLRZ	Q		0.2	0.4	0.8	0.3	0.4	0.8	ns/pF

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t = t_f = 3$ ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

R2403LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC2403			SN74ASC2403			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	CLK	Q	C_L = 0	3.5	5.4	10.2	3.6	5.4	9.4	ns
t_{PHL}				2.3	4.6	10	2.5	4.6	9	
t_{PLH}	CLK	Q	C_L = 1 pF	3.8	6	11.5	3.9	6	10.5	ns
t_{PHL}				2.6	5	10.8	2.8	5	9.8	
Δt_{PLH}	CLK	Q		0.3	0.5	1.3	0.3	0.5	1.1	ns/pF
Δt_{PHL}				0.3	0.5	0.9	0.3	0.5	0.8	

R2404LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC2404			SN74ASC2404			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	CLK	Q	C_L = 0	3.6	5.6	10.7	3.7	5.6	9.8	ns
t_{PHL}				2.4	4.8	10.2	2.6	4.8	9.3	
t_{PLH}	CLK	QZ		2.6	5.2	10.8	2.7	5.2	9.9	ns
t_{PHL}				3.7	5.8	11.3	3.9	5.8	10.4	
t_{PLH}	CLK	Q	C_L = 1 pF	3.9	6.1	11.9	4	6.1	10.8	ns
t_{PHL}				2.6	5.2	11	2.9	5.2	10	
t_{PLH}	CLK	QZ		3.2	6.2	13.1	3.4	6.2	11.9	ns
t_{PHL}				4.2	6.9	13.9	4.5	6.9	12.7	
Δt_{PLH}	CLK	Q		0.3	0.5	1.2	0.3	0.5	1.1	ns/pF
Δt_{PHL}				0.2	0.4	0.8	0.3	0.4	0.8	
Δt_{PLH}	CLK	QZ		0.6	1	2.3	0.7	1	2	ns/pF
Δt_{PHL}				0.5	1.1	2.7	0.6	1.1	2.4	

†Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

designing for testability

Designers employing storage or bistable elements should consider testability of the design in its final form. The need to preset or clear these elements should be assessed throughout the development of custom logic circuits with these considerations extended to the end equipment application with respect to maintainability. Simple action on the part of the ASIC designer can result in considerable cost savings, allowing the expense of IC testing, system testing, and system maintenance to be reduced significantly.

power-up clear/preset

Standard cell storage elements containing the capability to be asynchronously preset or cleared may be connected to the SN54ASC2320 or SN74ASC2320 power-up clear cell to achieve system initialization. Control of the clear or preset inputs from another system signal in conjunction with the power-up clear can be achieved with an AND gate.

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SystemCell™ 2-μm HARDWIRED MACRO CELL

- **Designed for Implementing Synchronous Registers**
- **Choice of Three Versions to Achieve Best Design Density**
- **Embedded Clock Drivers Provide Symmetrical Performance Across Long Registers**
- **Cascable and Expandable for Full Customization**

REGISTER CONFIGURATIONS OFFERED

CELL NAME	OUTPUTS	ASYNCHRONOUS CLEAR
'ASC2405	Q	Yes
'ASC2406	Q and $\overline{Q}$	Yes
'ASC2407	Q (3-State)	Yes

description

The 'ASC2405 thru 'ASC2407 are dedicated, hard-wired standard-cell macros implementing a three 4-bit flip-flop register elements. The three register configurations provide the custom IC designer with 4-bit registers to embed in ASICs in their most efficient form. Their 4-bit length means that larger blocks of custom logic can be handled efficiently to construct large registers.

The macros each contain an embedded clock driver that buffers the clock input to a single 2-line input. This further simplifies implementaion of longer registers, as standard library buffer cells can be used to drive multiple clock inputs, which are used in the longer registers. The macro cells are identified and called from the engineering workstation input using the cell names and netlist in conjunction with labels developed as shown in the following table:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		MAXIMUM CLOCK FREQUENCY (SN74ASC')	RELATIVE CELL AREA TO NA210LH
R2405LH	Label: R2405LH CLRZ,D1,D2,D3,D4,CLK,Q1,Q2,Q3,Q4;	64.2 MHz	23.25
R2406LH	Label: R2406LH CLRZ,D1,D2,D3,D4,CLK,Q1,Q1Z,Q2,Q2Z,Q3,Q3Z,Q4,Q4Z;	64.2 MHz	26.25
R2407LH	Label: R2407LH CLRZ,D1,D2,D3,D4,CLK,G,Q1,Q2,Q3,Q4;	36.3 MHz	26.25

The R2407LH incorporates 3-state outputs for interfacing internal buses directly. When enable G is high, the normal logic states (high or low levels) of the four outputs are impressed on the data bus. The outputs are disabled by a low logic level at enable G. The outputs then present a high impedance to the internal bus. While the outputs are disabled, sequential operation of the flip-flops is not affected.

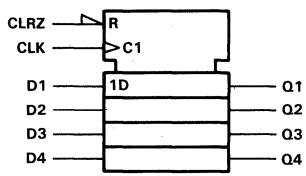
The SN54ASC' cells are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC' cells are characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

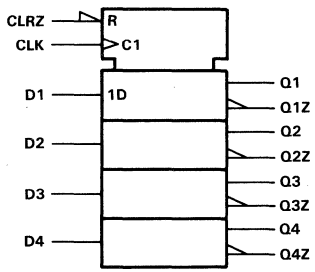
See Table 1 in Section 2.

logic symbols†

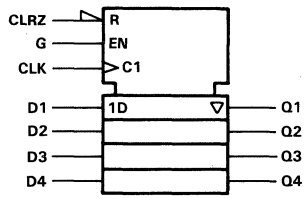
'ASC2405



'ASC2406



'ASC2407



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE
'ASC2405, 'ASC2406
(EACH FLIP-FLOP)

INPUTS			OUTPUTS	
CLRZ	CLK	D	Q	QZ‡
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q_0}$

‡'ASC2406 only

FUNCTION TABLE
'ASC2407
(EACH FLIP-FLOP)

INPUTS				OUTPUT
G	CLRZ	CLK	D	Q
H	L	X	X	L
H	H	↑	H	H
H	H	↑	L	L
H	H	L	X	Q_0
L	X	X	X	Z

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			R2405LH				R2406LH				UNIT
			SN54ASC'		SN74ASC'		SN54ASC'		SN74ASC'		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			64.2		64.2		64.2		64.2	MHz
t_w	Pulse duration	CLRZ low	6		6		7.8		7.8		ns
		CLK high or low	7.8		7.8		7.8		7.8		
t_{su}	Setup time before clock	Dn (high or low)	5.8		5.7		5.8		5.7		ns
		CLRZ inactive	−3		−3		−3		−3		
t_h	Hold time after clock	Dn (high or low)	0.2		0.3		−0.4		−0.3		ns
		CLRZ active	5.4		5.4		5.4		5.4		

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			R2407LH				UNIT
			SN54ASC'		SN74ASC'		
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			36.3		36.3	MHz
t_w	Pulse duration	CLRZ low	6.6		6.6		ns
		CLK high or low	13.8		13.8		
t_{su}	Setup time before clock	Dn (high or low)	7.6		7.5		ns
		CLRZ inactive	−3.6		−3.6		
t_h	Hold time after clock	Dn (high or low)	−0.4		−0.3		ns
		CLRZ active	6.6		6.6		

electrical characteristics

R2405LH

PARAMETER			TEST CONDITIONS		SN54ASC'		SN74ASC'		UNIT
					TYP	MAX	TYP	MAX	
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX	V_I = V_{CC} or 0,		2647		159	nA
C_i	Input capacitance	CLRZ	V_{CC} = 5 V,	T_A = 25°C	1.08		1.08		pF
		Dn			0.13		0.13		
		CLK			0.24		0.24		
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	10.2		10.2		pF

R2406LH

PARAMETER			TEST CONDITIONS		SN54ASC'		SN74ASC'		UNIT
					TYP	MAX	TYP	MAX	
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX	V_I = V_{CC} or 0,		2931		176	nA
C_i	Input capacitance	CLRZ	V_{CC} = 5 V,	T_A = 25°C	1.04		1.04		pF
		Dn			0.13		0.13		
		CLK			0.24		0.24		
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	11.7		11.7		pF

R2407LH

PARAMETER			TEST CONDITIONS		SN54ASC'		SN74ASC'		UNIT
					TYP	MAX	TYP	MAX	
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX	V_I = V_{CC} or 0,		3031		192	nA
C_i	Input capacitance	CLRZ	V_{CC} = 5 V,	T_A = 25°C	2.08		2.08		pF
		Dn			0.25		0.25		
		CLK			0.24		0.24		
		G			1.4		1.4		
C_o	Output capacitance		V_{CC} = 5 V,	T_A = 25°C	0.24		0.24		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	11		11		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

R2405LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC2405			SN74ASC2405			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	CLK	Q	C_L = 0	3.1	5.1	10.5	3.3	5.1	9.4	ns
t_{PHL}				2.3	4.4	10	2.5	4.4	8.9	
t_{PHL}	CLRZ	Q		1	1.7	3.5	1.1	1.7	3.2	ns
t_{PLH}	CLK	Q	C_L = 1 pF	3.5	6.1	12.8	3.8	6.1	11.5	ns
t_{PHL}				2.6	5.1	11.8	2.8	5.1	10.5	
t_{PHL}	CLRZ	Q		1.3	2.4	5.3	1.4	2.4	4.7	ns
Δt_{PLH}	CLK	Q		0.4	1	2.3	0.5	1	2.1	ns/pF
Δt_{PHL}				0.3	0.7	1.8	0.3	0.7	1.6	
Δt_{PHL}	CLRZ	Q		0.3	0.7	1.9	0.3	0.7	1.6	ns/pF

R2406LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC2406			SN74ASC2406			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	CLK	Q	C_L = 0	3.1	5.1	10.5	3.3	5.1	9.4	ns
t_{PHL}				2.3	4.5	9.9	2.5	4.5	8.9	
t_{PLH}	CLK	QZ		2.4	4.8	11	2.6	4.8	9.9	ns
t_{PHL}				3.4	5.8	12.3	3.6	5.8	11.1	
t_{PLH}	CLRZ	QZ		1.4	2.4	5.4	1.5	2.4	4.8	ns
t_{PHL}		Q		1	1.7	3.4	1.1	1.7	3.2	
t_{PLH}	CLK	Q	C_L = 1 pF	3.6	6.1	12.8	3.8	6.1	11.5	ns
t_{PHL}				2.6	5.2	11.8	2.8	5.2	10.5	
t_{PLH}	CLK	QZ		2.9	5.8	13.2	3.1	5.8	11.9	ns
t_{PHL}				3.6	6.4	13.8	3.9	6.4	12.3	
t_{PLH}	CLRZ	QZ		1.8	3.4	7.7	2	3.4	6.9	ns
t_{PHL}		Q		1.3	2.4	5.3	1.4	2.4	4.8	
Δt_{PLH}	CLK	Q		0.5	1	2.4	0.5	1	2.1	ns/pF
Δt_{PHL}				0.3	0.7	1.9	0.3	0.7	1.7	
Δt_{PLH}	CLK	QZ		0.5	1	2.3	0.5	1	2.1	ns/pF
Δt_{PHL}				0.2	0.6	1.5	0.3	0.6	1.3	
Δt_{PLH}	CLRZ	QZ		0.4	1	2.3	0.5	1	2.1	ns/pF
Δt_{PHL}		Q		0.3	0.7	1.9	0.3	0.7	1.6	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

R2407LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC2407			SN74ASC2407			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	CLK	Q	C_L = 0	3.3	5.5	11.6	3.5	5.5	10.5	ns
t_{PHL}				2.4	4.8	11.1	2.6	4.8	9.8	
t_{PHL}	CLRZ	Q		1.1	2	4.4	1.2	2	4	ns
t_{PLH}	CLK	Q	C_L = 1 pF	4.3	7.5	16.1	4.5	7.5	14.6	ns
t_{PHL}				3	6.2	14.4	3.2	6.2	12.7	
t_{PHL}	CLRZ	Q		1.7	3.4	7.9	1.9	3.4	7	ns
t_{PZH}	G	Q	C_L = 1 pF, R_L = 1 kΩ to GND	9.4	10.5	14.7	9.4	10.5	14.4	ns
t_{PZL}	G	Q	C_L = 1 pF, R_L = 1 kΩ to V_{CC}	4.3	5	8.1	4.4	4	7.7	ns
t_{PHZ}	G	Q	C_L = 1 pF, R_L = 40 kΩ to GND		9.8			9.8		ns
t_{PLZ}	G	Q	C_L = 1 pF, R_L = 20 kΩ to V_{CC}		5.6			5.6		ns
Δt_{PLH}	CLK	Q		1	2	4.6	1	2	4.2	ns/pF
Δt_{PHL}				0.6	1.4	3.4	0.6	1.4	3	
Δt_{PHL}	CLRZ	Q		0.6	1.4	3.5	0.7	1.4	3.1	ns/pF
Δt_{PZH}	G	Q		0.9	2	4.8	1	2	4.3	ns/pF
Δt_{PZL}				0.8	1.4	3.9	0.8	1.4	3.3	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
t_{PHZ} ≡ output disable time from high level
t_{PLZ} ≡ output disable time from low level
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
Δt_{PZH} ≡ change in t_{PZH} with load capacitance
Δt_{PZL} ≡ change in t_{PZL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

interfacing the macro

Inputs and outputs of these dedicated macros are compatible for interfacing directly with cells and macros available in the TI standard cell library. The inputs can be driven by either noninverting or inverting input cells. The outputs can be interfaced to drive off-chip loads with any of the noninverting output buffers or interfaced to external bidirectional buses through a 3-state input/output TTL/CMOS buffer.

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

designing for testability

Designers employing storage or bistable elements should consider testability of the design in its final form. The need to preset or clear these elements should be assessed throughout the development of custom logic circuits with these considerations extended to the end equipment application with respect to maintainability. Simple actions on the part of the ASIC designer can result in considerable cost savings, allowing the expense of IC testing, system testing, and system maintenance to be reduced significantly.

power-up clear/preset

Standard cell storage elements containing the capability to be asynchronously preset or cleared may be connected to the SN54ASC2320 or SN74ASC2320 power-up clear cell to achieve system initialization. Control of the clear or preset inputs from another system signal in conjunction with the power-up clear can be achieved with an AND gate.

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D2939, AUGUST 1986

SystemCell™ 2-μm HARDWIRED MACRO CELL

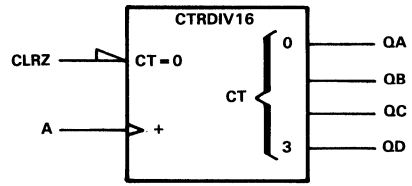
- **Predesigned for Implementing Custom Counters**
- **Direct Clear Input Simplifies Initialization or Cycle Length**
- **Embedded Clock Drivers Provide Clock Buffering**

description

The SN54ASC2408 and SN74ASC2408 are dedicated, hardwired standard-cell macros implementing a 4-bit binary counter element. The 4-bit configuration provides the custom IC designer a counter element to embed in ASICs in its most efficient form. Its 4-bit length means that larger blocks of custom logic can be handled efficiently to construct large counters. The 'ASC2408 implements a count sequence identical with that performed by one-half of packaged 'HC393 and 'LS393 counters with the exceptions that the 'AS2408 clock, A, triggers on the positive-going edge, and the clear is active low.

The macros each contain an embedded clock driver that buffers the clock input to a single 2-line input. This further simplifies implementaion of longer counters, as standard library buffer cells can be used to drive multiple clock inputs that are used in the longer counters. The macro cell is identified and called from the engineering workstation input using the cell name and netlist in conjunction with a label developed as shown in the following table:

logic symbol†



†This symbol is in accordance with ANSI/IEEE std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE

INPUTS		OUTPUTS			
CLRZ	A	QD	QC	QB	QA
L	X	L	L	L	L
H	↑	L	L	L	H
H	↑	L	L	H	L
H	↑	L	L	H	H
H	↑	L	H	L	L
H	↑	L	H	L	H
H	↑	L	H	H	L
H	↑	L	H	H	H
H	↑	H	L	L	L
H	↑	H	L	L	H
H	↑	H	L	H	L
H	↑	H	L	H	H
H	↑	H	H	L	L
H	↑	H	H	L	H
H	↑	H	H	H	L
H	↑	H	H	H	H
H	↑	L	L	L	L

CELL NAME	NETLIST HDL LABEL	FEATURES	
		MAXIMUM CLOCK FREQUENCY (SN74ASC)	RELATIVE CELL AREA TO NA210LH
R2408LH	Label: R2408LH CLRZ,A,QA,QB,QC,QD;	59.6	28.25

The SN54ASC2408 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC2408 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			SN54ASC2408		SN74ASC2408		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	59.6	0	59.6	MHz
t_w	Pulse duration	CLRZ low	7.8		7.8		ns
		A high or low	8.4		8.4		
t_{su}	Setup time	CLRZ inactive	−1.2		−1.2		ns
t_h	Hold time	CLRZ active	4.2		4.2		ns

electrical characteristics

PARAMETER			TEST CONDITIONS		SN54ASC2408		SN74ASC2408		UNIT
					TYP	MAX	TYP	MAX	
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX	V_I = V_{CC} or 0,		3463		208	nA
C_i	Input capacitance	CLRZ	V_{CC} = 5 V,	T_A = 25°C	1.04		1.04		pF
		A			0.24		0.24		
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	7.22		7.22		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC2408			SN74ASC2408			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{pd}	A	QA	C_L = 0	2.6	5.5	12.3	2.8	5.5	11.1	ns
		QB		3.7	8	17.7	4	8	15.9	
		QC		4.8	10.2	23.1	5.2	10.2	20.7	
		QD		5.9	12.5	28.5	6.4	12.5	25.5	
t_{PHL}	CLRZ	Q		1.3	2.2	4.6	1.4	2.2	4.2	ns
t_{pd}	A	QA	C_L = 1 pF	2.9	6	13.5	3.1	6	12.2	ns
		QB		4	8.5	18.9	4.3	8.5	17	
		QC		5.1	10.7	24.3	5.5	10.7	21.8	
		QD		6.2	13	29.7	6.7	13	26.6	
t_{PHL}	CLRZ	Q		1.6	2.7	5.4	1.7	2.7	5	ns
Δt_{PLH}	A	Any Q		0.3	0.5	1.3	0.3	0.5	1.1	ns/pF
Δt_{PHL}	Any	Any		0.3	0.5	0.9	0.3	0.5	0.8	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{pd} ≡ propagation delay time, low-to-high- or high-to-low-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

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DESIGN CONSIDERATIONS

interfacing the macro

Inputs and outputs of these dedicated macros are compatible for interfacing directly with cells and macros available in the TI standard cell library. The inputs can be driven by either noninverting or inverting input cells. The outputs can be interfaced to drive off-chip loads with any of the noninverting output buffers or interfaced to external bidirectional buses through a 3-state input/output TTL/CMOS buffer.

count definition

Bidirectional counters are available in software macros or can be constructed using the 'ASC2405 through 'ASC2407 4-bit registers.

designing for testability

Designers employing storage or bistable elements should consider testability of the design in its final form. The need to preset or clear these elements should be assessed throughout the development of custom logic circuits with these considerations extended to the end equipment application with respect to maintainability. Simple actions on the part of the ASIC designer can result in considerable cost savings, allowing the expense of IC testing, system testing, and system maintainence to be reduced significantly.

power-up clear/preset

Standard cell storage elements containing the capability to be asynchronously preset or cleared may be connected to the SN54ASC2320 or SN74ASC2320 power-up clear cell to achieve system initialization. Control of the clear or preset inputs from another system signal in conjunction with the power-up clear can be achieved with an AND gate.

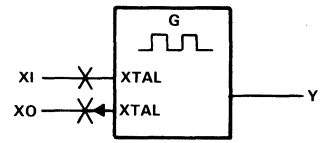
SN54ASC2500, SN74ASC2500 CRYSTAL-CONTROLLED OSCILLATORS

D2939, AUGUST 1986

SystemCell™ 2-μm HARDWIRED STANDARD CELL

- Crystal-Controlled Oscillator for Generating On-Chip Clock Signals Up to 20 MHz
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol



description

The SN54ASC2500 and SN74ASC2500 are crystal-controlled CMOS oscillators for use in SystemCell™ designs. The input XI and the feedback output XO provide the connections for use with an external series resonant fundamental crystal. The 'ASC2500 provides three cells supporting frequencies up to 20 MHz. Driving on-chip binary frequency dividers, a single oscillator can generate multiple system clocks and/or control functions. Each option is designated and called from the engineering workstation input using the following cell name and netlist label.

CELL NAME	NETLIST HDL LABEL	FEATURES	
		MAXIMUM FREQUENCY	RELATIVE CELL AREA TO NA210LH
OSE00LH	Label: OSx0nLH XI,Y,XO;	5 MHz	129
OSF02LH		20 MHz	150
OSE06LH		800 kHz	128

The SN54ASC2500 will be characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC2500 will be characterized for operation from −40°C to 85°C.

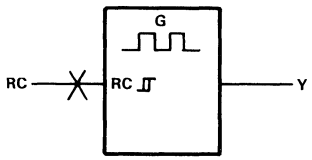
SN54ASC2502, SN74ASC2502 RC OSCILLATORS

D2939, AUGUST 1986

SystemCell™ 2-μm HARDWIRED STANDARD CELL

- **Single-Pin RC-Controlled Oscillator for Generating On-Chip Clock Signals**
- **Input Hysteresis Improves Response to Analog Input Levels**
- **Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol



description

The SN54ASC2502 and SN74ASC2502 are single-input RC-controllable CMOS oscillators for use in SystemCell™ IC designs. Input RC serves as the external connection point for the RC frequency-determining network. The ASC2502 has a bandwidth of 10 kHz to 1 MHz with the actual frequency dependent on the RC time constant. The oscillator incorporates hysteresis in the RC input threshold to sharpen the oscillator response. The cell is designated and called from the engineering workstation input using the following cell name and netlist label.

CELL NAME	NETLIST HDL LABEL	FEATURES	
		MAX OUTPUT FREQUENCY RANGE	RELATIVE CELL AREA TO NA210LH
OSE03LH	Label: OSE03LH RC,Y;	1 MHz	42.2

The SN54ASC2502 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC2502 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operated conditions

		SN54ASC2502		SN74ASC2502		UNIT
		MIN	MAX	MIN	MAX	
C_{ext}	External RC capacitor	10		10		pF
R_{ext}	External RC resistor	10	100	10	100	kΩ
f_{out}	Output frequency		1		1	MHz

Also, see Table 1 in Section 2.

electrical characteristics

PARAMETER		TEST CONDITIONS		SN54ASC2502		SN74ASC2502		UNIT
				TYP	MAX	TYP	MAX	
V_{t+}	Positive-going threshold voltage	V_{CC} = 5 V,	T_A = 25°C	3.6		3.6		V
V_{t-}	Negative-going threshold voltage	V_{CC} = 5 V	T_A = 25°C	1.3		1.3		V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = 5 V,	T_A = 25°C	2.3		2.3		V
I_{CC}	Supply current	V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX,	V_I = V_{CC} or 0		1026		61.5	nA
C_i	Input capacitance	V_{CC} = 5 V,	T_A = 25°C	2.34		2.34		pF
C_{pd}	Equivalent power dissipation capacitance	V_{CC} = 5 V, T_A = 25°C	$t_r = t_f$ = 3 ns,	2.44		2.44		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

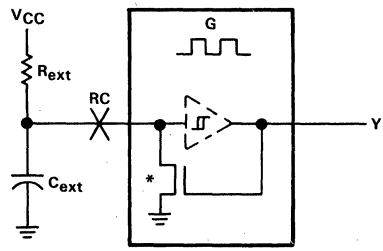
PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC2502			SN74ASC2502			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	RC	Y	C_L = 0	3.9	6.8	14.7	4.2	6.8	13.6	ns
t_{PHL}				3.3	5.8	12.9	3.5	5.8	11.5	
t_{PLH}	RC	Y	C_L = 1 pF	4.3	7.6	16.7	4.6	7.6	14.9	ns
t_{PHL}				3.9	7.2	16.3	4.2	7.2	14.4	
Δt_{PLH}	RC	Y		0.4	0.8	2	0.4	0.8	1.8	ns/pF
Δt_{PHL}				0.6	1.4	3.4	0.7	1.4	2.9	

† Propagation delay times are measured from the 50% point of V_I to the 50% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with capacitance
Δt_{PHL} ≡ change in t_{PHL} with capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

An RC network is used to drive the oscillator input. Oscillator output stability is primarily a function of the temperature coefficients of the components in the RC network.

TYPICAL OUTPUT FREQUENCIES		
R_{ext} (kΩ)	C_{ext}	f_{out}
100	0.1 μF	100 Hz
100	0.001 μF	10 kHz
100	10 pF	700 kHz



*On resistance ≈ 150 Ω

SN54ASC2503, SN74ASC2503 DIFFERENTIAL COMPARATORS

D2939, AUGUST 1986

SystemCell™ COMPATIBLE ANALOG CELL

- **Single 5-V Supply with ±10% Tolerance**
- **Very Low Power Consumption . . . 60 μW Typical**
- **Wide Range of Common-Mode Input Voltage Includes Ground on P-Channel Inputs and V_{CC} on N-Channel Inputs**
- **External Voltage Reference**

logic symbol

description

The CO212LH and CO213LH standard cells are medium-speed comparators and operate from a single 5-volt supply. The CO212LH standard cell is a P-channel comparator, and the CO213LH is an N-channel comparator. The inputs are connected to ESD-protected bond pads, which are connected to an external voltage reference and the analog input. The comparators can be configured as either inverting or noninverting functions and are designed to drive the inputs of logic cells or buffers. The CO212LH P-channel comparator can be used with input voltages between (ground) and 3.5 volts. The CO213LH N-channel comparator can operate with input voltages between 1.5 volts and V_{CC}. Each cell is designated and called from the engineering workstation input using the following cell name and netlist label:

CELL NAME	DESCRIPTION	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
CO212LH	P-Channel Comparator	CO212LH INZ,IN,OUT;	5
CO213LH	N-Channel Comparator	CO213LH INZ,IN,OUT;	5

The SN54ASC2503 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC2503 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 1 pF

PARAMETER		CO213LH			CO212LH			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage			50			50	mV
V_{ICR}	Common-mode input voltage	1.5		V_{CC}	0		3.5	V
A_{VD}	Large-signal differential voltage amplification		116			116		dB
CMRR	Common-mode rejection ratio at f = 1 kHz		94			97		dB
k_{SVR}	Supply voltage rejection ratio at f = 1 kHz		100			104		dB
I_{CC}	Supply current		11			11.7		μA

switching characteristics at V_{CC} = 5 V, T_A = 25 °C

PARAMETER	TEST CONDITION	CO213LH			CO212LH			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	100-mV input step with 5 mV of overdrive, $V_{ref} = V_{CC}/2$		1.9			1.71		ns
t_{PHL}			1.5			2.14		
Δt_{PLH}			8			6		ns/pF
Δt_{PHL}			6			7		
t_{PLH}	TTL-level input step 0.2 to 3 V, V_{ref} = 1.6 V					1.71		μs
t_{PHL}						2.06		
Δt_{PLH}						3		ns/pF
Δt_{PHL}						7		

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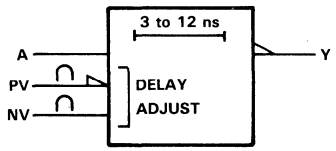
SN54ASC2507, SN74ASC2507 DYNAMIC DELAY ELEMENT

D2939, AUGUST 1986

SystemCell™ COMPATIBLE MACRO CELL

- Provides Dynamic Delay for Custom Delay Lines
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Dependable Texas Instruments Quality and Reliability

logic symbol



description

The SN54ASC2507 and SN74ASC2507 are hardwired standard cells implementing an inverting delay buffer preceded by a transmission gate and driven by an SN54ASC2508/SN74ASC2508 control element. This provides a custom delay line with a typical delay tolerance range of ±5%.

The 'ASC2508 control element uses a reference clock signal as a time-base for generating the complimentary reference voltages, NV and PV, for controlling the data path delay output of the 'ASC2507. The reference clock signal can be supplied from either an on-chip oscillator or an external source.

CELL NAME	NETLIST HDL LABEL	TYPICAL DELAY C_L = 1 pF	RELATIVE CELL AREA TO NA210LH
DLE10LH	Label: DLE10LH A,PV,NV,Y;	3 to 12 ns	7.41

The SN54ASC2507 will be characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC2507 will be characterized for operation from −40°C to 85°C.

design considerations

Data path delays are dependent on the accuracy of the time-base reference and the control block. The custom delay line can be broken into two sections: 1) the control section and 2) the delay section. The control section provides the NV and PV voltages for controlling the delay time through the data delay paths (see Figure 1).

design considerations (continued)

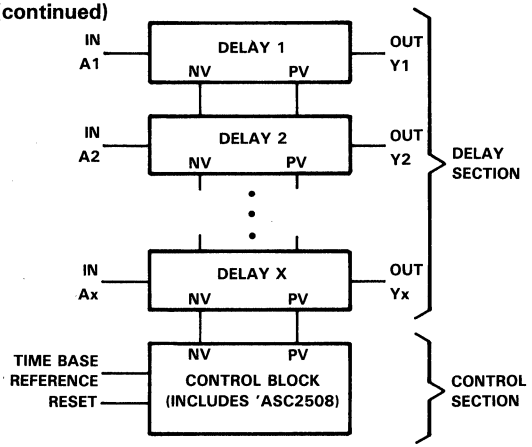


FIGURE 1. BLOCK DIAGRAM OF CUSTOM DELAY LINE

The delay section offers two methods to program line delays, either by the number of delay elements in the data path or, by the voltage to the PV and NV lines. In Figure 2, the delay ratio between the delay 1, delay 2, and delay 3 data paths is set with the number of delay elements in each data line. Actual delay times through the delay elements can be determined and changed with the PV and NV voltages that are governed by the control block and the 'ASC2508.

Figure 2 shows the basic method of providing three different delay times using six 'ASC2507s controlled by a single 'ASC2708.

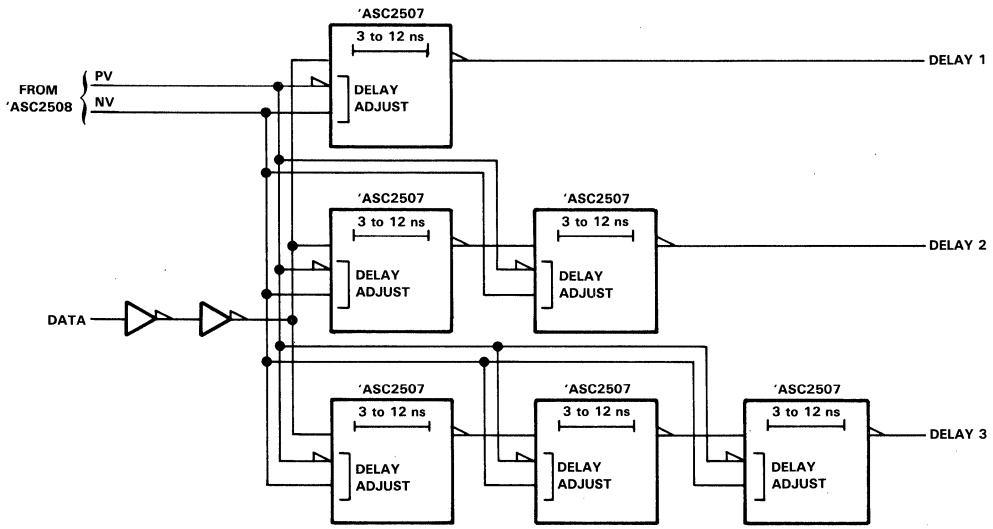


FIGURE 2. THREE DELAY PATHS CONTROLLED BY A SINGLE CONTROL ELEMENT

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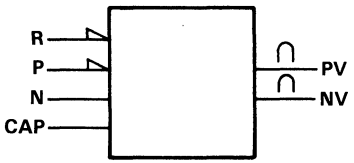
SN54ASC2508, SN74ASC2508
CONTROL ELEMENT FOR DYNAMIC DELAY ELEMENT

D2939, AUGUST 1986

SystemCell™ COMPATIBLE MACRO CELL

- **Provides Dynamic Control for Custom Delay Lines**
- **Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol



description

The SN54ASC2508 and SN74ASC2508 are hardwired standard cell analog voltage control blocks for the 'ASC2507 dynamic delay elements, providing control voltages for the PV and NV inputs of the delay element.

The 'ASC2508 control element uses a reference clock signal as a time-base for generating the complimentary reference voltages, NV and PV, to control the 'ASC2507 element data path delays. The reference clock signal can be supplied from either an on-chip oscillator or an external oscillator. A single control element can control several delay paths and each path can have a different delay time. Typical time-base reference frequency range is from 5 MHz to 25 MHz.

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
DLC10LH	Label: DLC10LH P,N,R,CAP,PV,NV;	7.41

The SN54ASC2508 will be characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC2508 will be characterized for operation from −40°C to 85°C.

DESIGN CONSIDERATIONS

The timing reference, shown in Figure 1, is implemented with SystemCell™ components to provide temperature and voltage-compensated digital reference inputs that activate the 'ASC2508, which generates the NV and PV control voltages for the 'ASC2507 delay element. The timing reference is unique for each application. Specific timing design information is made available in conjunction with the completion of a customer's ASIC specification.

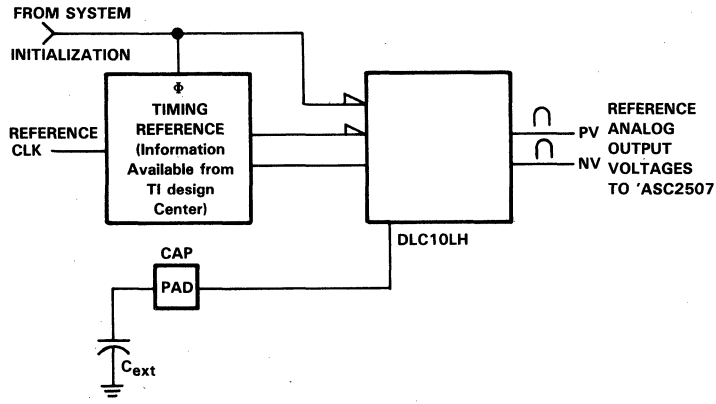


FIGURE 1. BLOCK DIAGRAM OF TIMING REFERENCE AND CONTROL ELEMENT FOR GENERATING ANALOG VOLTAGES, PV AND NV

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SN54ASC2519, SN74ASC2519
MEDIUM-DRIVE OPERATIONAL AMPLIFIER

D2939, AUGUST 1986

SystemCell™ COMPATIBLE ANALOG CELL

- Single 5-Volt Supply
- Internally Frequency Compensated
- Inputs are ESD and Latch-Up Protected
- Medium Output Drive Capability: 10 kΩ and 50-pF External Load

logic symbol

description

The SN54ASC2519 and SN74ASC2519 standard cells are medium-speed operational amplifiers that operate from a single 5-V supply. Their inputs and outputs are connected to ESD-protected bond pads for connection to external circuitry. The operational amplifiers can be configured as either inverting or noninverting amplifiers. For precision applications, a separate V_{CC} and ground should be included in the design specification. The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL
AMC12NH	AMC12NH IN,INZ,OUT;

The SN54ASC2519 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC2519 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

		MIN	MAX	UNIT
C_L	External load capacitance		50	pF
R_L	External load resistance	10		kΩ

Also, see Table 1 in Section 2.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 1 pF

	PARAMETER	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage		±10		mV
V_{ICR}	Common-mode input voltage	1		$V_{CC}-1$	V
V_{OM}	Maximum peak output voltage swing	1		4.5	V
A_{VD}	Large-signal differential amplification		15		V/mV
B_1	Unity-gain bandwidth		2		MHz
ϕ_m	Phase margin		90°		
r_o	Output resistance		5		Ω
CMRR	Common-mode rejection ratio at 1 kHz		80		dB
k_{svr}	Supply voltage rejection ratio at 1 KHz		100		dB
I_{CC}	Supply current		1		mA

operating characteristics at V_{CC} = 4.5 V to 5.5 V, T_A = 25°C

	PARAMETER	MIN	TYP	MAX	UNIT
SR	Slew rate		2		V/μs

SystemCell™ COMPATIBLE MegaModule™

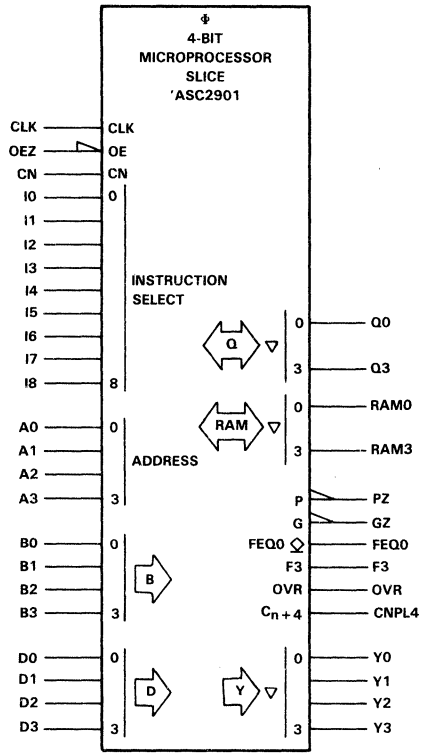
description

The SN54ASC2901 and SN74ASC2901 standard cells are compatible with TI's SystemCell™ library and have been developed to achieve maximum design efficiency on silicon. This library function allows for complete system implementation on chip by reducing the industry standard AM2901 4-bit microprocessor slice function to a single cell, thus allowing space for additional logic functions.

The cell consists of a 16-word by 4-bit two-port RAM, a high-performance ALU, and the associated circuitry to achieve the necessary decoding, shifting, and multiplexing. The microprocessor cell can be cascaded for greater design flexibility, and is a valuable tool when used in conjunction with other members of the 'ASC2900 family of standard cells, including the 'ASC2902 look-ahead carry generator, the 'ASC2904 status and shift control unit, and the 'ASC2910 microprogram controller.

The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

logic symbol



CELL NAME	NETLIST HDL LABEL
M01MPLH	Label: M01MPLH CLK,QEZ,CN,I8. . . I0,B3 . . . B0,A3 . . . A0,D3 . . . D0,Q3,Q0, RAM3,RAM0,GZ,PZ,F3,FEQ0,OVR,CNPL4,Y3 . . . Y0;

The SN54ASC2901 will be characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC2901 will be characterized for operation from −40°C to 85°C.

signal description

NODE NAME	FUNCTION
A0 . . . A3	Address inputs to A port of register stacks
B0 . . . B3	Address inputs to B port
I0 . . . I8	Instruction control lines
Q3/RAM3	Shift line at MSB of the Q register
Q0/RAM0	Shift line at LSB of the Q register
D0 . . . D3	Direct data inputs
Y0 . . . Y3	Data outputs
OEZ	Output enable. When high, the Y outputs are off.
GZ,PZ	Carry generate and propagate outputs of the ALU
OVR	Overflow
FEQ0	Open-collector output. A high indicates ALU outputs are low
F3	Most significant ALU output bit
CN	Carry-in to internal ALU
CNPL4	Carry-out of internal ALU
CLK	Clock input

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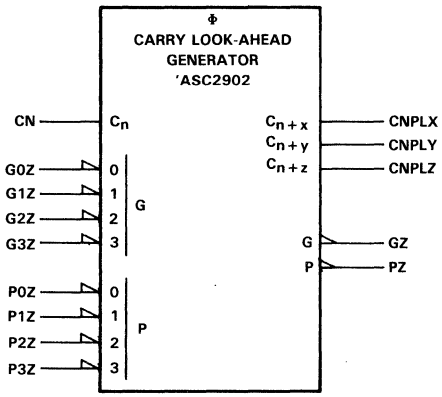
SN54ASC2902, SN74ASC2902 LOOK-AHEAD CARRY GENERATOR

D2939, AUGUST 1986

SystemCell™ COMPATIBLE MegaModule™

logic symbol



description

The SN54ASC2902 and SN74ASC2902 standard cells are compatible with the TI SystemCell™ library and are functionally equivalent to the standard AM2902. The cell is a high-speed, look-ahead carry generator designed to accept up to four pairs of carry propagate and carry generate signals, and a carry input. Anticipated carries are provided across four groups of binary ALUs. Along with these features, the carry propagate and carry generate outputs can be used with further levels of look-ahead.

The 'ASC2902 offers extensive design value when used in conjunction with TI's 'ASC2901 and related family members. The 'ASC2902 cell can be used to create full system functionality on a custom or a standard cell chip.

The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL
M02CGLH	Label: M02CGLH CN,G3Z,P3Z,G2Z,P2Z,G1Z,P1Z,G0Z,P0Z,CNPLX,CNPLY,CNPLZ,GZ,PZ;

The SN54ASC2902 will be characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC2902 will be characterized for operation from −40°C to 85°C.

signal description

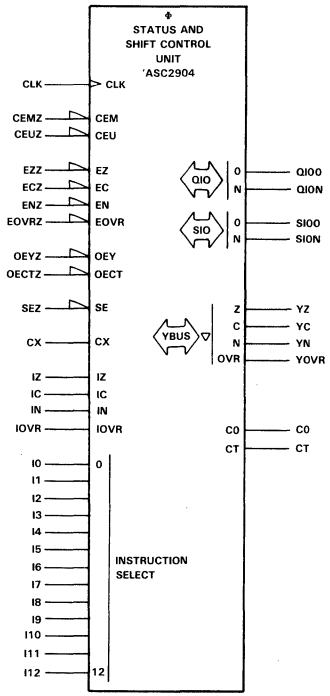
NODE NAME	FUNCTION
CN	Carry-in inputs
CNPLj	Carry-out outputs (j = X, Y, Z)
G0Z . . . G3Z	Carry generate inputs
P0Z . . . P3Z	Carry propagate inputs
GZ	Generate output
PZ	Propagate output

SN54ASC2904, SN74ASC2904 STATUS AND SHIFT CONTROLLER

D2939, AUGUST 1986

SystemCell™ COMPATIBLE MegaModule™

logic symbol



description

The SN54ASC2904 and SN74ASC2904 standard cells are compatible with the TI SystemCell™ library and are functionally equivalent to the standard AM2904. The cell was developed to work with the 'ASC2901 to allow for complete system development. The 'ASC2904 includes generation of the carry-in signal to the ALU and carry look-ahead unit. It also accounts for the interconnection of the data path, auxiliary operations, and the testing of ALU status flags. This cell, when used with other 'ASC2900 family cells provides complete ALU capability and offers full system implementation on a single chip.

The 'ASC2904 cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL
M04SSLH	Label: M04SSLH CLK,CEMZ,CEUZ,EZZ,ECZ,ENZ,EOVRZ,OEYZ,OECTZ,SEZ,CX,IZ,IC,IN, IOVR,I12 . . . I0,YZ,YC,YN,YOVR,SI00,SIOn,QI00,QIOn,C0,CT;

The SN54ASC2904 will be characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC2904 will be characterized for operation from −40°C to 85°C.

signal description

NODE NAME	FUNCTION
IZ	Zero status input
IC	Carry status input
IN	Sign status input
IOVR	Overflow status input
I0 . . . I12	Instruction select inputs
CEMZ	Overall enable for machine status register. When high, MSR bits retain their present state.
EZZ/ECZ/ENZ/EOVRZ	Enable for corresponding bits in machine status register
CEUZ	When low, enables all four bits in micro status register (USR)
YZ/YC/YN/YOVR	Form a bidirectional bus over which MSR and USR status can be read or the MSR bits can be loaded in parallel.
OEYZ	When low, enables Y signals as outputs
CT	Conditional test output
OECTZ	When low, activates CT
SIO0/SIOn/QIO0/QIOn	Linking for various shift and rotate conditions
SEZ	Controls the state of shift outputs
C0	Carry-in control MUX output
CX	Carry-in control MUX input
CLK	Clock input

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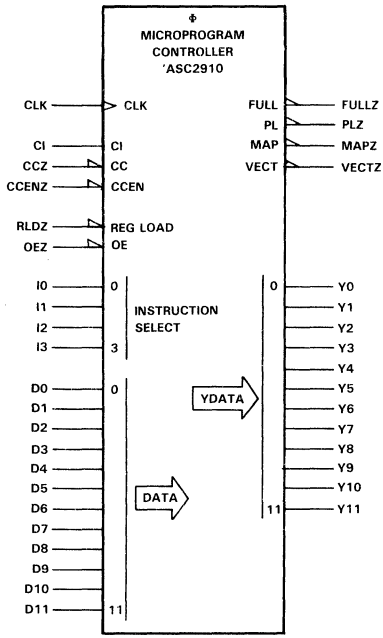
SN54ASC2910, SN74ASC2910 MICROPROGRAM CONTROLLER

D2939, AUGUST 1986

SystemCell™ COMPATIBLE MegaModule™

logic symbol



description

The SN54ASC2910 and SN74ASC2910 standard cells are compatible with the TI SystemCell™ library. The 'ASC2910 supports the function of an address sequencer in controlling the sequence of execution of microinstructions stored in the microprogram memory. Both sequential stepping and conditional branching to microinstructions within its microword range are allowed. Nine levels of nesting of microsubroutines, accessed through the return linkage and looping capabilities, are provided for by a last-in, first-out stack.

The 'ASC2910 cell has been designed as a companion to the other members of TI's 'ASC2900 standard cell family, which offers a total system design solution for single-chip implementation. The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL
M10MCLH	Label: M10MCLH CLK,CI,CCZ,CCENZ,RLDZ,OEZ,I3 . . . I0,D11 . . . D0, FULLZ,PLZ,MAPZ,VECTZ,Y11 . . . Y0;

The SN54ASC2910 will be characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC2910 will be characterized for operation from −40°C to 85°C.

signal description

NODE NAME	FUNCTION
D0 . . . D11	Input to register/counter and MUX
I0 . . . I3	Instruction select
CCZ	Test criterion. Low level indicates test passed.
CCENZ	When high, CCZ is ignored.
C1	Carry input to incrementer
RLDZ	When low, forces loading of register/counter.
OEZ	Output enable for Y outputs
CLK	Trigger for internal state changes
Y0 . . . Y11	Address to microprogram memory
FULLZ	Indicates that nine items are on stack
PLZ	When low, selects #1 source as direct input (usually pipeline register).
MAPZ	When low, selects #2 source as direct input (usually mapping PROM or PLA).
VECTZ	When low, selects #3 source as direct input (for example, interrupt starting address).

4 Data Sheets

SystemCell™ 2-μm COMPATIBLE MACRO CELLS

- **Typical Access Time . . . 41 ns at C_L = 1 pF**
- **Full Parallel Access with Separate Input and Output Ports**
- **Low Standby Power in Power-Down Mode**
- **Data Retention at V_{CC} Down to 2 V**

RAM SUMMARY

TYPE	ORGANIZATION	
	WORDS	BITS
'ASC3003	16	16
'ASC3004	64	8
'ASC3005	256	4
'ASC3006	128	8

description

The 'ASC3003 through 'ASC3006 are dedicated, hardwired standard-cell macros implementing four static RAM organization configurations that provide the custom IC designer with small and medium-complexity memory macros to embed in ASICs in their most efficient form. Their structured architecture permits the use of multiple memory macros to implement custom on-chip local storage memories.

The memory macros contain embedded buffers to reduce input loading. This further simplifies implementation of larger memories as standard library cells can be used to interface the memory control inputs. The macro cells are identified and called from the engineering workstation input using the cell name and netlist in conjunction with a label developed as shown in the following:

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
RA416LH	Label: RA416LH D0,D1,D2,D3,D4,D5,D6,D7,D8,D9,D10,D11,D12,D13, D14,D15,A0,A1,A2,A3,EZ,WZ,GZ,Q0,Q1,Q2,Q3,Q4,Q5,Q6,Q7, Q8,Q9,Q10,Q11,Q12,Q13,Q14,Q15,TIE;	473
RA608LH	Label: RA608LH D0,D1,D2,D3,D4,D5,D6,D7,A0,A1,A2,A3,A4,A5,EZ,WZ GZ,Q0,Q1,Q2,Q3,Q4,Q5,Q6,Q7,TIE;	712
RA804LH	Label: RA804LH D0,D1,D2,D3,A0,A1,A2,A3,A4,A5,A6,A7,EZ,WZ,GZ, Q0,Q1,Q2,Q3,TIE;	1243
RA708LH	Label: RA708LH D0,D1,D2,D3,D4,D5,D6,D7,A0,A1,A2,A3,A4,A5,A6, EZ,WZ,GZ,Q0,Q1,Q2,Q3,Q4,Q5,Q6,Q7,TIE;	1214

Separate inputs and outputs not only simplify control circuitry design but also enhance memory access for both read and write. The read and write modes are independent and can occur in the same machine cycle, if desired.

TABLE 1. FUNCTION TABLE (ALL RAM TYPES)

ENABLE INPUTS			DATA INPUTS	OUTPUTS		MEMORY MODE
WZ	EZ	GZ†	D0 THRU Dn	Q0 THRU Qn	TIE†	
L	L	L	Data in	Data out	H	Write, outputs enabled
L	L	H	Data in	Hi-Z	H	Write, outputs disabled
X	H	L	Inhibited	L	X	Power-down
X	H	H	Inhibited	Hi-Z	X	Power-down
H	L	L	Inhibited	Data out	L	Read, outputs enabled
H	L	H	Inhibited	Hi-Z	L	Outputs disabled
L	L	TIE	Data in	Hi-Z	H	Write, outputs disabled
L	H	TIE	Not active	Hi-Z	H	Power-down
H	L	TIE	Inhibited	Data out	L	Read, outputs enabled
H	H	TIE	Not active	Hi-Z	H	Power-down

†The TIE output can be connected directly to the output enable, GZ, to implement a common input/output, I/O, memory. If common I/O is not used, the TIE output is not connected in the netlist.

An independent output enable, GZ, is provided for the three-state output to facilitate interfacing the memory with internal data-buses. Also, a separate input, EZ, is provided for enabling or disabling the entire memory macro. When disabled, the memory assumes a powered-down state. The active levels for these two enables are compatible for utilizing a single control mode to effect both output disable and simultaneous power-down. An individual input controlling the write mode, WZ, enters new data into the addressed word location when WZ is low.

The TIE output, provided as a design option, offers the designer a simple method for implementing a common input/output (I/O) memory. The TIE output can be connected directly to the 3-state output-control input, GZ, to implement a common I/O RAM. If common I/O is not desired, the TIE output can be omitted from connections in the design netlist.

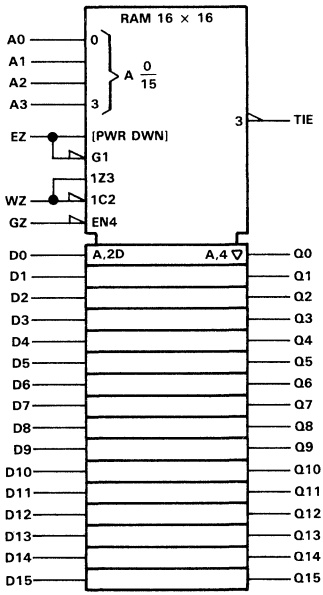
SN54ASC' RAMs are characterized for operation over the full military temperature range of −55°C to 125°C. SN74ASC' RAMs are characterized for operation from −40°C to 85°C.

SIGNAL DESCRIPTIONS

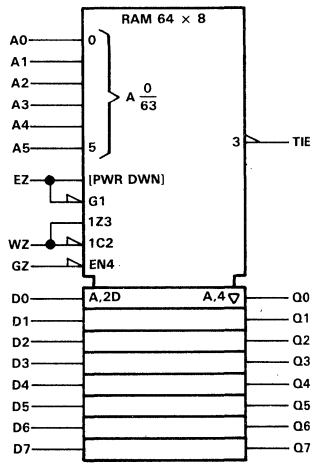
NODE		FUNCTION
NAME(S)	TITLE	
A0−An	Address	Address inputs
D0−Dn	Data	Data inputs
EZ	Memory Enable	When low, the memory is enabled. When high, the memory is placed in a power-down mode and disabled.
GZ	Output Enable	When low, data appears at the memory output. If EZ is high when GZ is low, output will be low. When high, the outputs assume a high-impedance state, Hi-Z.
Q0−Qn	Output	Data outputs
TIE	Output	When WZ is high and EZ is low, the TIE output goes low. For any other write/chip enable combination, the TIE output remains high. TIE implements a common I/O RAM by connecting it directly to the output enable, GZ.
WZ	Write	When low, data is written into the addressed locations. When high, writing is inhibited.

logic symbols†

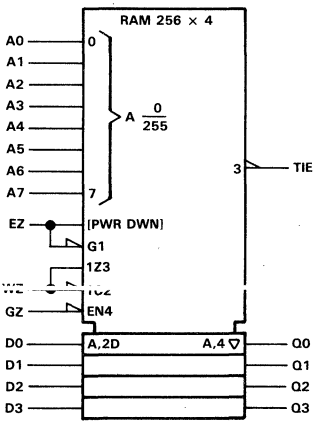
RA416LH



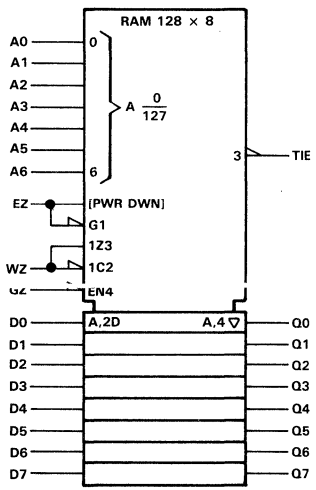
RA608LH



RA804LH



RA708LH



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings and recommended operating conditions

See Table 1, Section 2. Data stored in the memory will be retained if the supply voltage is above the 2-volt minimum. Functional characteristics other than data retention are not specified when V_{CC} is between 2 volts and 4.5 volts.

timing requirements over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

		RA416LH RA804LH		RA608LH		RA708LH		UNIT
		SN54'	SN74'	SN54'	SN74'	SN54'	SN74'	
		MIN	MIN	MIN	MIN	MIN	MIN	
$t_{su(A)}$	Address setup time	0	0	0	0	0	0	ns
$t_{h(A)}$	Address hold time	0	0	0	0	0	0	ns
$t_{su(D)}$	Data setup time	30	28	22	20	30	28	ns
$t_{h(D)}$	Data hold time	0	0	0	0	0	0	ns
$t_{w(W)}$	Write pulse duration	22	20	22	20	24	22	ns
$t_{c(W)}$	Write cycle time	80	77	80	77	80	77	ns

electrical characteristics over recommended ranges of supply voltage and temperature (unless otherwise noted)

RA416LH

PARAMETER			TEST CONDITIONS	SN54ASC3003		SN74ASC3003		UNIT
				TYP	MAX	TYP	MAX	
V_T	Input threshold voltage	D0-D15	V_{CC} = 5 V, T_A = 25°C	2.1		2.1		V
		All others		2		2		
I_{CC}	Supply current	EZ = H	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN or MAX		19.8		1.2	μA
		EZ = L			31.8		29.5	mA
C_i	Input capacitance	A0	V_{CC} = 5 V, T_A = 25°C	0.6		0.6		pF
		A1 to A3		0.18		0.18		
		Dn		0.13		0.13		
		EZ		0.15		0.15		
		GZ		0.26		0.26		
		WZ		0.29		0.29		
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C, t_r = t_f = 3 ns,	110		110		pF

RA608LH

PARAMETER			TEST CONDITIONS	SN54ASC3004		SN74ASC3004		UNIT
				TYP	MAX	TYP	MAX	
V_T	Input threshold voltage	D0-D7	V_{CC} = 5 V, T_A = 25°C	2.1		2.1		V
		All others		2		2		
I_{CC}	Supply current	EZ = H	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN or MAX		24.9		1.5	μA
		EZ = L			29.7		27.6	mA
C_i	Input capacitance	A0	V_{CC} = 5 V, T_A = 25°C	0.6		0.6		pF
		A1 to A5		0.18		0.18		
		Dn		0.13		0.13		
		EZ		0.15		0.15		
		GZ		0.26		0.26		
		WZ		0.29		0.29		
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C, t_r = t_f = 3 ns,	110		110		pF

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electrical characteristics over recommended ranges of supply voltage and temperature (unless otherwise noted) (continued)

RA804LH

PARAMETER			TEST CONDITIONS	SN54ASC3005		SN74ASC3005		UNIT
				TYP	MAX	TYP	MAX	
V_T	Input threshold voltage	D0-D3	V_{CC} = 5 V, T_A = 25°C	2.1		2.1		V
		All others		2		2		
I_{CC}	Supply current	EZ = H	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0,		51.9		3.1	μA
		EZ = L	T_A = MIN or MAX		31.8		29.5	mA
C_i	Input capacitance	A0 to A2	V_{CC} = 5 V, T_A = 25°C	0.6		0.6		pF
		A3 to A7		0.18		0.18		
		Dn		0.13		0.13		
		EZ		0.15		0.15		
		GZ		0.26		0.26		
		WZ		0.29		0.29		
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C, $t_r = t_f$ = 3 ns,	110		110		pF

RA708LH

PARAMETER			TEST CONDITIONS	SN54ASC3006		SN74ASC3006		UNIT
				TYP	MAX	TYP	MAX	
V_T	Input threshold voltage	D0-D7	V_{CC} = 5 V, T_A = 25°C	2.1		2.1		V
		All others		2		2		
I_{CC}	Supply current	EZ = H	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0,		51.9		3.1	μA
		EZ = L	T_A = MIN or MAX		31.8		29.5	mA
C_i	Input capacitance	A0,A1	V_{CC} = 5 V, T_A = 25°C	0.6		0.6		pF
		A2 to A6		0.18		0.18		
		Dn		0.13		0.13		
		EZ		0.15		0.15		
		GZ		0.26		0.26		
		WZ		0.29		0.29		
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C, $t_r = t_f$ = 3 ns,	110		110		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

RA416LH, RA608LH, RA804LH, and RA708LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54'			SN74'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$t_{a(A)}$	An	Qn	C_L = 1 pF		41	80		41	77	ns
$t_{a(E)}$	EZ	Qn			41	80		41	77	
t_{PZH}	GZ	Qn	C_L = 1 pF to V_{CC}, R_L = 40 kΩ to GND	1.7	4.5	12.4	2.1	4.5	11.1	ns
t_{PZL}	GZ	Qn	C_L = 1 pF to GND, R_L = 20 kΩ to V_{CC}	1.5	3.4	8.7	1.7	3.4	7.7	ns
t_{PHZ}	GZ	Qn	C_L = 1 pF to GND, R_L = 40 kΩ to GND	7.6	9.2	15.4	7.6	9.2	14.4	ns
t_{PLZ}	GZ	Qn	C_L = 1 pF to GND, R_L = 20 kΩ to V_{CC}	3.9	4.6	9.4	3.9	4.6	8.6	ns
Δt_{PLH}	Any	Qn		0.2	0.7	1.7	0.3	0.7	1.5	ns/pF
Δt_{PHL}				0.3	0.7	1.7	0.3	0.7	1.6	
Δt_{PZH}	GZ	Qn		0.3	0.7	1.8	0.3	0.7	1.7	ns/pF
Δt_{PZL}				0.3	0.7	1.8	0.3	0.7	1.6	

†Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
$t_{a(A)}$ ≡ access time from address, low-to-high-level or high-to-low-level output
$t_{a(E)}$ ≡ access time from enable (power up), low-to-high-level or low-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} = output enable time to low level
t_{PHZ} ≡ output disable time from high level
t_{PLZ} ≡ output disable time from low level
Δt_{PLH} ≡ change in t_a with load capacitance, low-to-high-level output
Δt_{PHL} ≡ change in t_a with load capacitance, high-to-low-level output
Δt_{PZH} ≡ change in Δt_{PZH} with laod capacitance
Δt_{PZL} ≡ change in Δt_{PZL} with load capacitance
‡Typical values are at V_{CC} = 5 V, T_A = 25°C.

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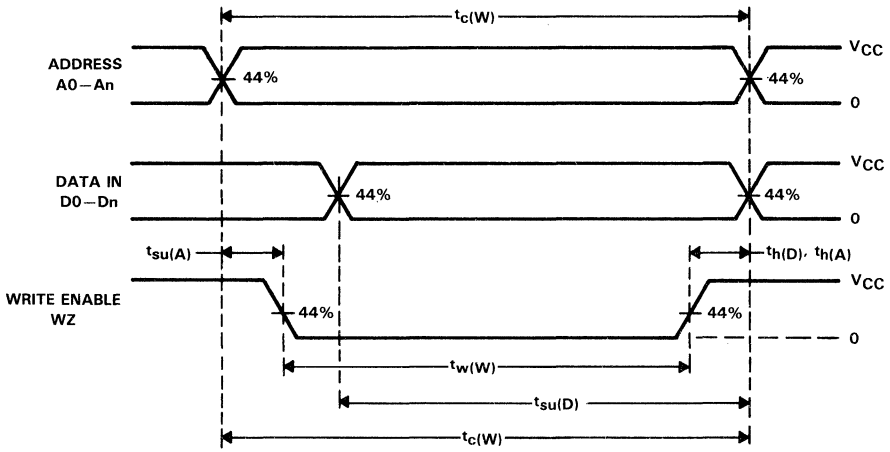
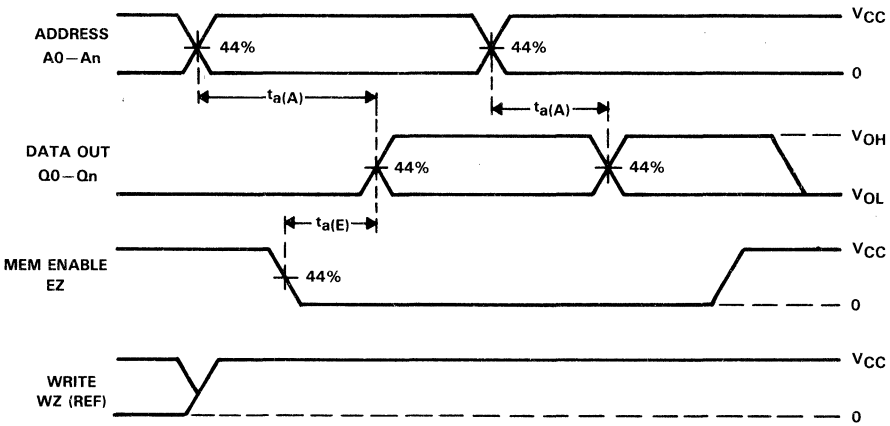
PARAMETER MEASUREMENT INFORMATION

write cycle 1 (see Notes 1 and 2)



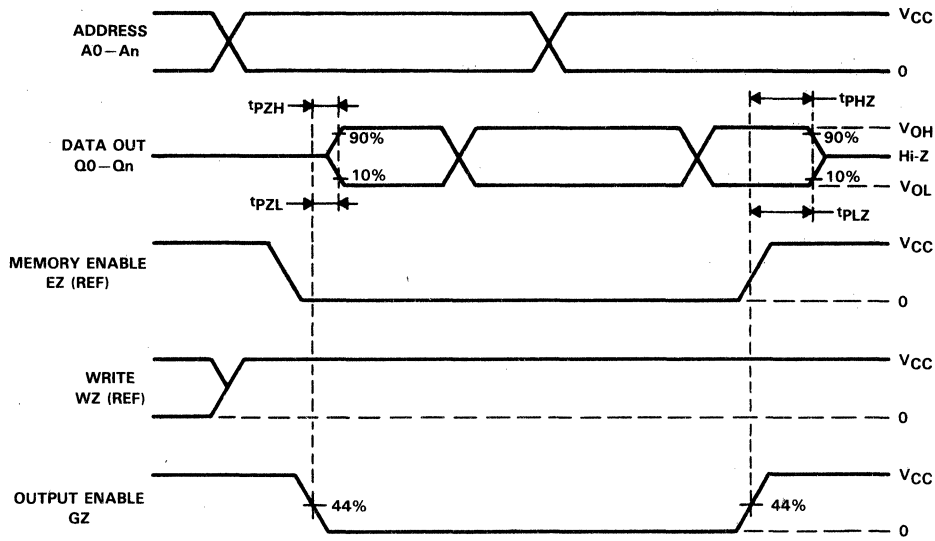
NOTES: 1. Write cycle 1 is used when the RAM has separate DATA IN and DATA OUT buses.
2. EZ = GZ = LOW

read cycle 1 (see Notes 3 and 4)



NOTES: 3. This read cycle is used when the RAM has separate DATA IN and DATA OUT buses.
4. GZ = LOW

read cycle 2 (see Note 5)



NOTE 5: This read cycle is used when the RAM is interfaced with a bidirectional data bus.

DESIGN CONSIDERATIONS

interfacing the macro

Inputs and outputs of these dedicated macros are compatible for interfacing directly with cells and macros available in the TI standard cell library. The inputs can be driven by either noninverting or inverting input cells. The outputs can be interfaced to drive off-chip loads with any of the noninverting output buffers or interfaced to external bidirectional buses through a 3-state input/output TTL/CMOS buffer.

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

designing for testability

Testability of the design in its final form should be considered when memory elements are used in the design. Testing at the device level and troubleshooting under field maintenance conditions can be enhanced by providing either direct or multiplexed input pins for controlling the memory. Simple actions on the part of the ASIC designer can result in considerable costs savings and the expense of IC testing, system testing, and system maintenance can be reduced significantly.

TEXAS INSTRUMENTS
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SystemCell™ COMPATIBLE 2-μm CompilerCell™ SRAMs

description

The SN54ASC3010 and SN74ASC3010 CompilerCell™ SRAMs are compatible with the TI SystemCell™ library and are structured to simplify the design of logic systems. The static storage element is a conventional 6-transistor cell. Operation using two clock signals permits the use of internal timing strobes, which results in optimum use of silicon, reduced power consumption, and speeds up both read and write cycles.

A comprehensive software package is used by the factory to generate a schematic, HDL description, and a simulation model. The timing performance of the RAM is a function of the number of bits and the geometrical configuration used. The user specifies the number of words and the word length for use by the factory RAM compiler software. Table 1 shows the range of RAM configurations that can be generated using the 'ASC3010.

logic symbol

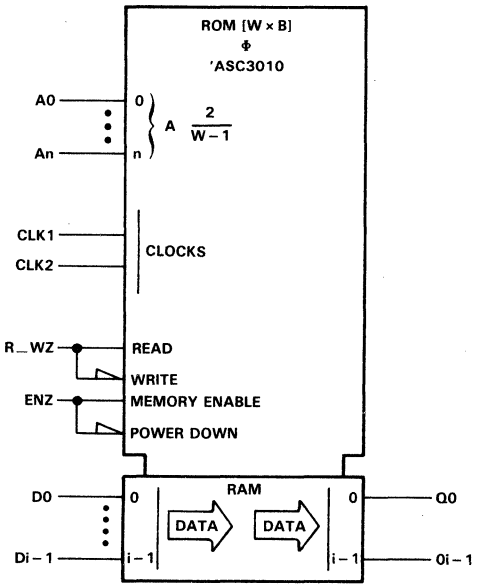


TABLE 1. SRAM ARRAY LIMITS

PARAMETERS	MIN	MAX	COMMENTS
Number of words ($W \leq 2^n$)	4	1024	Any even number
Word length in bits (B = i)	4	32	Number of data inputs = number of data outputs = word length
Total number of bits (W x B)	16	16384	

The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL
AZRMLB†	LABEL: AZRMLB D0,D1, D2,...Di-1, A0...An,CLK1,CLK2,ENZ,R_WZ,Q0...Qi-1

Cell names and labels are developed as a function of cell design.
†AZ: Identifying symbol
LB: Wordlength in bits. Topology dependent value
M: Number of columns multiplexed onto one output. A = 1:1, B = 2:1, C = 4:1, and D = 8:1. Topology dependent value
R: Number of rows. Topology dependent value

The SN54ASC3010 will be characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC3010 will be characterized for operation from −40°C to 85°C.

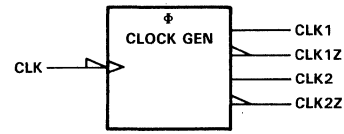
SN54ASC3011, SN74ASC3011
2-PHASE CLOCK GENERATOR WITH COMPLEMENTARY OUTPUTS

D2939, AUGUST 1986

SystemCell™ 2-μm COMPATIBLE MACRO CELL

- **Generates 2-Phase Clock for Compiler Cell Functions**
- **Embedded Function — Requires No External Connection**
- **Can Be Operated from Single-Phase of System On-Chip Clock**

logic symbol



description

The SN54ASC3011 and SN74ASC3011 are dedicated, hardwired standard-cell 2-phase clock generators that provide complementary outputs for driving the clock inputs of compiler cells used in a SystemCell™ design. The compiler cells employ clocked circuitry to reduce power requirements, and a synchronous clock ensures that state changes occur on the trailing edge of the clock, thus ensuring that state conditions are stable during the next clock period. The clock generator cell is designated and called from the engineering workstation input using the following cell name to develop a label for the design netlist:

CELL NAME	NETLIST HDL LABEL
CK4X0LH	Label: CK4X0LH CLK,CLK1,CLK1Z,CLK2,CLK2Z;

The SN54ASC3011 will be characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC3011 will be characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 2 in Section 2.

D2939, AUGUST 1986

SystemCell™ COMPATIBLE MegaModule

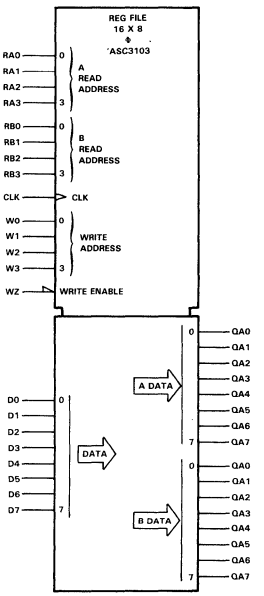
- **Full Parallel Access with One Write and Two Read Ports**
- **Typical Access Times:**
  Write-then-Read Cycle Time . . . 11 ns
  Address Access Time . . . 8 ns
- **Data Retention at V_{CC} > 2 V**

description

The SN54ASC3103 and SN74ASC3103 are dedicated, hard-wired standard-cell macros implementing a 3-port, high-speed register file organized as 16 words of 8 bits each. These devices provide cost-effective, closely coupled working registers to support high-performance, bus-structured processors embedded in ASICs. Multiple 8-bit-wide register files can be used to implement wide-word, scratch-pad memories.

The register macros contain embedded buffers to reduce input loading. This further simplifies implementation of larger registers as standard library cells can be used to interface the register control inputs. The macro cells are designated and called from the engineering workstation input using the cell name and netlist in conjuction with a label developed as shown in the following table:

logic symbol



CELL NAME	NETLIST HDL LABEL
RF408LH	Label: RF408LH CLK,WZ,W0,W1,W2,W3,RA0,RA1,RA2,RA3,RB0,RB1,RB2,RB3, D0,D1,D2,D3,D4,D5,D6,D7,QA0,QA1,QA2,QA3,QA4,QA5,QA6,QA7, QB0,QB1,QB2,QB3,QB4,QB5,QB6,QB7;

The 16-word-by-8-bit register organization is provided with a data-input port and two read ports that incorporate dedicated address inputs. As the read mode is asynchronous at both output ports, data entry and retrieval can occur simultaneously at all three ports. The dedicated address inputs permit full access to any of the 16-word locations from each port.

An independent write enable, WZ, is provided to simplify implementation of the write cycle. When high, the write enable inhibits new data entry. When low, the write function is enabled, and a positive transition at the clock input will store data applied at the data inputs in the register word addressed by the write-address inputs, W0 thru W3.

The SN54ASC3103 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC3103 is characterized for operation from −40°C to 85°C.

WRITE FUNCTION TABLE

		WRITE ADDRESS				DATA INPUTS	OUTPUTS OF REGISTER	FUNCTION
CLK	WZ	W0	W1	W2	W3	D0 . . D7	ADDRESSED	
X	H	X	X	X	X	X . . X	$Q0_0$ . . $Q7_0$	No change
↑	L	L	L	L	L	a . . h	a . . h	Write word 0
↑	L	H	L	L	L	a . . h	a . . h	Write word 1
↑	L	L	H	L	L	a . . h	a . . h	Write word 2
↑	L	H	H	L	L	a . . h	a . . h	Write word 3
.	.					.	. .	.
.	.					.	. .	.
.	.					.	. .	.
↑	L	H	H	H	H	a . . h	a . . h	Write word 15
L	X	X	X	X	X	X . . X	$Q0_0$ . . $Q7_0$	No change

READ FUNCTION TABLE

A PORT READ ADDRESS				A PORT DATA OUTPUTS	B PORT READ ADDRESS				B PORT DATA OUTPUTS
RA0	RA1	RA2	RA3	QA0 . . QA7	RB0	RB1	RB2	RB3	QB0 . . QB7
L	L	L	L	Read word 0	H	H	H	H	Read word 15
H	L	L	L	Read word 1	L	H	H	H	Read word 14
L	H	L	L	Read word 2	H	L	H	H	Read word 13
H	H	L	L	Read word 3	L	L	H	H	Read word 12
	.			.		.			.
	.			.		.			.
	.			.		.			.
H	L	L	L	Read word 7	H	L	L	L	Read word 7
	.			.		.			.
	.			.		.			.
H	H	H	H	Read word 15	L	L	L	L	Read word 0

SIGNAL DESCRIPTIONS

NODE		FUNCTION
NAME(S)	TITLE	
CLK	Clock input	Data present at the data inputs are stored in the addressed locations during a positive transition at the clock input. During steady-state (high or low) the clock is inactive.
D0,Dn	Data input	Data inputs
QA0,QAn	Data output	Data outputs for A port
QB0,QBn	Data output	Data outputs for B port
RA0,RAn	Read address input	Read address inputs for A port
RB0,RBn	Read address input	Read address inputs for B port
W0,Wn	Write address	Write address inputs
WZ	Write input	When low, data can be clocked into the addressed locations. When high, writing is inhibited.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2. Data stored in the register are retained if the supply voltage is not permitted to go below 2 volts minimum. Functional characteristics other than data retention are not specified when V_{CC} = 2 V to 4.5 V.

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electrical characteristics

PARAMETER		TEST CONDITIONS	SN54ASC3103		SN74ASC3103		UNIT
			TYP	MAX	TYP	MAX	
V_T Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC} Supply current		V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		69.6		4.2	μA
C_i Input capacitance	CLK	V_{CC} = 5 V, T_A = 25°C	0.1		0.1		pF
	Dn		0.16		0.16		
	RAn		0.14		0.14		
	RBn		0.14		0.14		
	Wn		0.14		0.14		
	WZ		0.23		0.23		
C_{pd} Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C, t_r = t_f = 3 ns,	289		289		pF

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		MIN	MAX	UNIT
t_w Clock pulse duration	High	10.5		ns
	Low	10		
t_{su} Setup time before CLK↑	Write address	8.5		ns
	Data	3.5		
	Write enable	10		
t_h Hold time after CLK↑	Write address	0		ns
	Data	6		
	Write enable	1		

switching characteristics over recommended ranges of supply voltge and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC3103			SN74ASC3103			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	RAn, RBn	Any	C_L = 0	3.3	6.3	13.4	3.6	6.3	11.8	ns
t_{PHL}				3.7	6.2	13.6	3.9	6.2	12.1	
t_{PLH}	CLK	Any		4.7	10.3	22.4	5.1	10.3	19.9	ns
t_{PHL}				4.2	10.2	20.6	4.6	10.2	18.3	
t_{PLH}	RAn, RBn	Any	C_L = 1 pF	3.6	7	14.7	3.9	7	13	ns
t_{PHL}				4	7	15.1	4.2	7	13.5	
t_{PLH}	CLK	Any		5.1	11	23.7	5.5	11	21.1	ns
t_{PHL}				4.6	11	22.1	5	11	19.7	
Δt_{PLH}	Any	Any		0.3	0.7	1.4	0.3	0.7	1.3	ns/pF
Δt_{PHL}				0.3	0.8	1.6	0.3	0.8	1.5	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

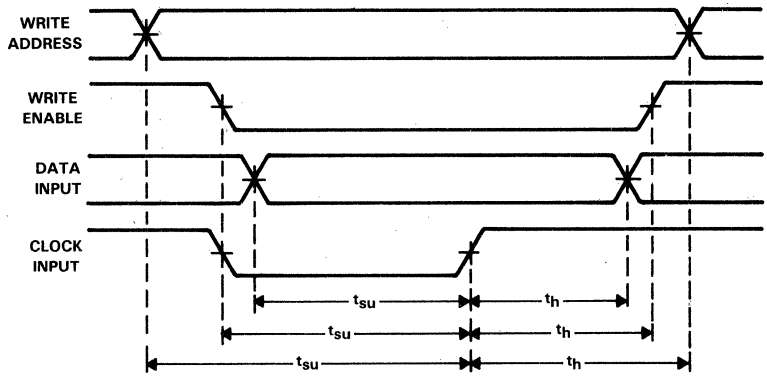
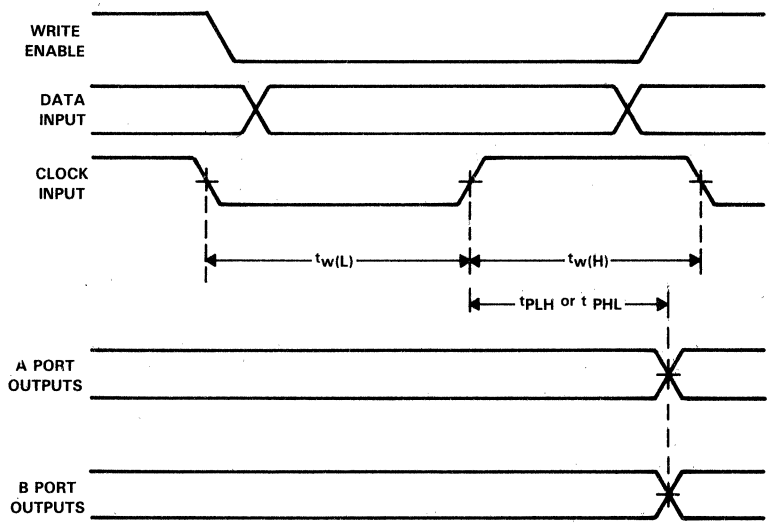


FIGURE 1. SETUP AND HOLD TIMES



Addresses for write and both reads are the same.

FIGURE 2. CLOCK PULSE DURATION, PROPAGATION DELAY TIMES FROM CLOCK

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PARAMETER MEASUREMENT INFORMATION

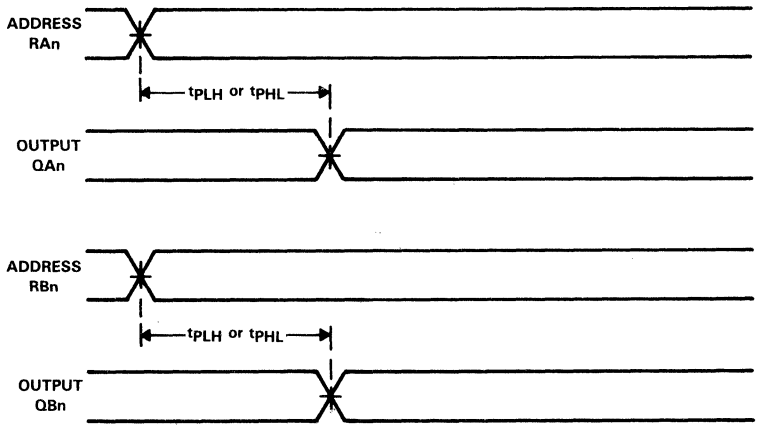


FIGURE 3. PROPAGATION DELAY TIMES FROM READ ADDRESS

DESIGN CONSIDERATIONS

interfacing the macro

Inputs and outputs of these dedicated macros are compatible for interfacing directly with cells and macros available in the TI standard cell library. The inputs can be driven by either noninverting or inverting input cells. The outputs can be interfaced to drive off-chip loads with any of the noninverting output buffers or interfaced to external bidirectional buses through a 3-state input/output TTL/CMOS buffer.

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

designing for testability

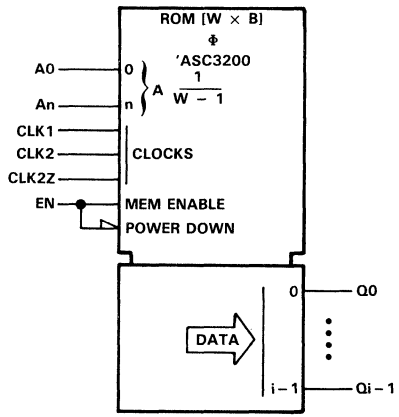
Designers employing register elements should consider testability of the design in its final form. The need to provide either direct or multiplexed input pins for controlling the register will enhance both testing at the device level and troubleshooting under field maintenance conditions. Simple actions on the part of the ASIC designer can result in considerable cost savings, allowing the expense of IC testing, system testing, and system maintenance to be reduced significantly.

SN54ASC3200, SN74ASC3200 CompilerCell™ READ-ONLY MEMORIES

D2639, AUGUST 1986

SystemCell™ COMPATIBLE 2-μm CompilerCell™ ROMs

logic symbol



HDL CALL

LABEL: ROM ADO . . . ADn,PHI1B,PHI2,PHI2B,POWD,
OUTO . . . OUTn;

description

The SN54ASC3200 and SN74ASC3200 are read-only memory (ROM) CompilerCell™. They are compatible with TI's SystemCell™ library and can be a powerful aid to the solution of cell design problems. They can be selected with bit capacities between 512 and 65,536.

These ROMs are clock controlled, which permits pre-charging of some circuit regions resulting in speed advantages, lower power dissipation, and optimum use of silicon. The 'ASC3200 is a nonvolatile memory whose bit contents are determined by the presence or absence of transistors in the rows and columns of the ROM matrix. The transistors are formed during the custom patterning process defined by the user.

For bit capacities up to 16K, a single array is used. For greater capacities, a double array offers 64K-bit capacity for only 70% more silicon area. A choice of multiplexing ratios is offered between the array columns and the output word, which allows greater flexibility in the layout of the cell.

TI Compiler Software permits rapid programmation and verification of the chosen pattern, as well as rapid generation of the desired ROM bit organization. The possible combination of ROM organizations are shown in Tables 1 and 2.

TABLE 1. SINGLE ARRAY PARAMETER LIMITS

PARAMETERS	MIN	MAX	COMMENTS
Number of Words ($W \geq 2^n$)	8	2048	Must be multiple of 4
Word Length (B = i)	4	32	Even or Odd
Total Number of Bits (W × B)	512	16384	

TABLE 2. DOUBLE ARRAY PARAMETER LIMITS

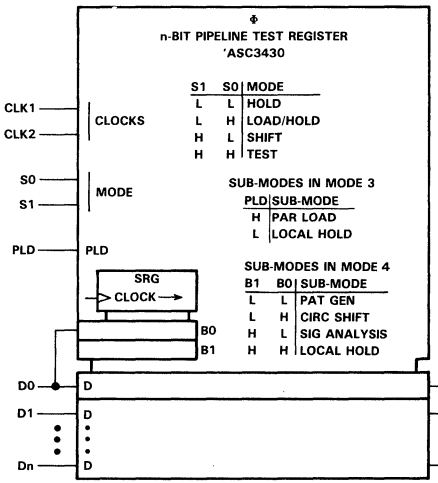
PARAMETERS	MIN	MAX	COMMENTS
Number of Words ($W \geq 2^n$)	8	4096	Must be multiple of 4
Word Length (B = i)	4	64	Must be Even
Total Number of Bits (W × B)	512	65536	

SN54ASC3430, SN74ASC3430
CompilerCell™ PIPELINE TEST REGISTERS

D2939, AUGUST 1986

SystemCell™ COMPATIBLE 2-μm INTERNAL STANDARD CELL

logic symbol



description

The SN54ASC3430 and SN74ASC3430 CompilerCell™ Pipeline Test Registers assist the designer in solving the problem of testing VLSI cell designs. The large gate counts and circuit complexities permitted by 2-μm technologies result in functional blocks so embedded within the circuit that their inputs/outputs can neither be monitored or initialized without the use of very large test pattern sets of I/O cells assigned specifically for test purpose.

The PTR is an n-bit register whose size is determined by the user in the design phase (n = 4 to 32). The principal modes of operation are as a parallel master-slave latch for holding and latching data buses or as a serially-loaded unidirectional register that allows test stimuli and results to be shifted around the circuit.

Sections of a logic circuit may be self tested using a pair of PTRs. The first PTR is configured as a pseudo-random pattern generator that delivers random values at a number of outputs over a time period. The second PTR, arranged as a signature analyzer, takes the outputs from the circuit under the test over a number of clock cycles and condenses them into a test signature whose value depends totally on the tested outputs over the specified time period. At the end of the period, the signature is serially down-loaded from the PTR and compared with a known "fault free" value in order to arrive at a pass/fail decision. The modes of operation are listed in Table 1 and described in the following paragraphs.

TABLE 1. MODES OF OPERATION

MAIN MODE			SUB-MODE			
	S1	S0		PLD	B1	B0
HOLD	L	L	NONE			
USER FUNCTIONAL	L	H	LOCAL HOLD	L	X	X
			PARALLEL LOAD	H	X	X
SHIFT	H	L	NONE			
TEST	H	H	PATTERN GENERATE	X	L	L
			CIRCULAR SHIFT	X	L	H
			SIGNATURE ANALYZE	X	H	L
			LOCAL HOLD	X	H	H

Hold	All data is retained in the registers. If all PTRs in the system have common pins, then all data is held in all registers.
Shift	Data may be serially loaded into the register via pin DO. The data passes through a two-bit control register whose ouputs BO and B1 determine the sub-mode.
User Functional	Data is parallel loaded into the register or held according to the setting of input PLD. In this mode, each element of the register is isolated from its neighbor and acts as an independent data latch. In sub-mode "Local Hold", data may be held in just a single register while the remaining PTRs may be performing other tasks.
Test	In this mode, there are four available sub-modes.

Sub-mode 0. Pseudo-Random Pattern Generation

The outputs from the register are fed back to the input via a selected number of Exclusive-OR gates. This is a well-documented method of producing a sequence of pseudo-random signals from a register for use as test signals for a logic circuit. A four-bit example is shown in Figure 1.

Sub-mode 1. Circular Shift

Connection in the circular shift mode causes the last output of the PTR to be connected to the first.

Sub-mode 2. Signature Analysis

As with Pattern Generation, the Signal Analyzer has data fed back to its first input as indicated in Figure 2. The input of each section of the register is determined by both the preceding output and the output from the circuit under test. A characteristic data signature is built up on the register outputs. This signature is dependent on all of the previous output states of the circuit under test. After a number of clock cycles, the signature of a faulty circuit will be different from that of a good one.

Sub-mode 3. Local Hold

This sub-mode permits a user to command one or more PTRs in a system to hold its data.

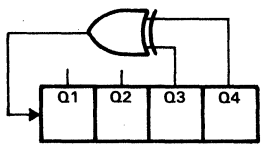


FIGURE 1. PTR AS A PSEUDO-RANDOM PATTERN GENERATOR

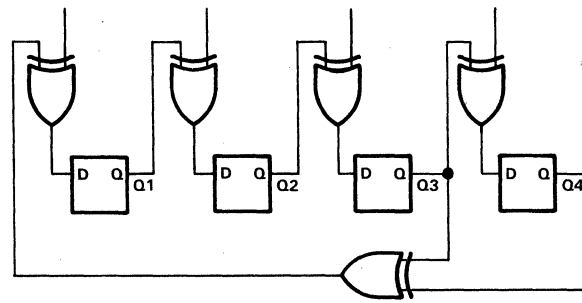


FIGURE 2. 4-BIT PTR AS A SIGNATURE ANALYZER

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SN54ASC3800, SN74ASC3800
CompilerCell™ PROGRAMMABLE LOGIC ARRAYS

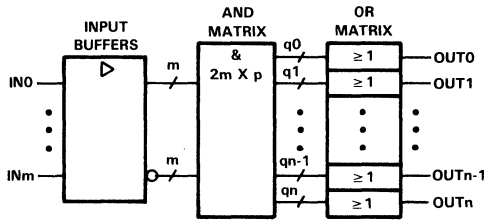
D2939, AUGUST 1986

SystemCell™ COMPATIBLE 2-μm INTERNAL STANDARD CELL

description

The SN54ASC3800 and SN74ASC3800 **CompilerCell™** logic arrays are semicustom PLAs having many of the features of the current packaged PLAs. The cells operate dynamically from a system-derived clock and offer significant power savings compared to the packaged devices. Cell complexity is decided at the design stage and can be tailored for the application resulting in economical use of silicon. Texas Instruments software generates the PLA automatically from a library of primitive cells according to the user's function tables or Boolean equations. The software will also produce an HDL description, a simulation model, timing diagrams, and an individual data sheet.

functional block diagram



m = number of inputs
n = number of outputs
p = number of product terms = q0 + q1 + . . . qn − 1 + qn
qx = number of inputs to OR gate x (x = 0 . . . n)

The cells are specified by number of inputs, m, number of product terms, p, and number of outputs, n. The internal matrix follows the usual arrangement of an AND matrix and an OR matrix. Each product term ANDs together a specified number of inputs, and each output comes from a specified number of product terms via an OR gate. Maximum values for the parameters are shown below:

INPUTS	PRODUCT TERMS	OUTPUTS
m	p	n
64	128	32

- Circuit design is optimized around a 32-input X 64-product term X 32-output design that will run at a speed of 20 MHz.

The SN54ASC3800 will be characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC3800 will be characterized for operation from 0°C to 70°C.

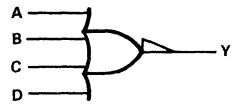
4 Data Sheets

D2939, AUGUST 1986

SystemCell™ 2-μm INTERNAL STANDARD CELL

- **Choice of Two Performance Levels**
- **Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V**
- **Functional Operation Over V_{CC} Range of 2 V to 6 V**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol



FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	Y
H	X	X	X	L
X	H	X	X	L
X	X	H	X	L
X	X	X	H	L
L	L	L	L	H

positive logic equation

$$Y = \overline{A+B+C+D} = \overline{A}\,\overline{B}\,\overline{C}\,\overline{D}$$

description

The SN54ASC4002 and SN74ASC4002 are 4-input positive-NOR gate CMOS standard cells that implement the equivalent of one-half of the SN54HC4002 or SN74HC4002. The standard-cell library contains two physical implementations to provide the custom IC designer a choice between two performance levels for optimizing designs. Each option is designated and called from the engineering workstation input using the following cell names to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		TYPICAL DELAY C_L = 1 pF	RELATIVE CELL AREA TO NA210LH
NO410LH	Label: NO4n0LH A,B,C,D,Y;	4.1 ns	1.5
NO420LH		2.6 ns	2.5

The SN54ASC4002 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC4002 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS	NO410LH		NO420LH		UNIT
				TYP	MAX	TYP	MAX	
V_T	Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current	SN54ASC4002	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0,		177		277	nA
		SN74ASC4002	T_A = MIN to MAX		10.6		16.6	
C_i	Input capacitance		V_{CC} = 5 V, T_A = 25°C	0.11		0.22		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, t_r = t_f = 3 ns, T_A = 25°C	0.35		0.55		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

NO410LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC4002			SN74ASC4002			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A,B,C,D	Y	C_L = 0	0.7	1.4	4.1	0.7	1.4	3.7	ns
t_{PHL}				0.8	1.3	2.6	0.9	1.3	2.3	
t_{PLH}	A,B,C,D	Y	C_L = 1 pF	2.6	5.4	13.3	2.8	5.4	12	ns
t_{PHL}				1.4	2.8	7	1.5	2.8	6.2	
Δt_{PLH}	A,B,C,D	Y		1.9	4	9.2	2	4	8.4	ns/pF
Δt_{PHL}				0.5	1.5	4.7	0.6	1.5	4.1	

NO420LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC4002			SN74ASC4002			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A,B,C,D	Y	C_L = 0	0.7	1.1	2.8	0.7	1.1	2.5	ns
t_{PHL}				0.6	1.2	2.3	0.7	1.2	2.2	
t_{PLH}	A,B,C,D	Y	C_L = 1 pF	1.6	3.1	7.4	1.7	3.1	6.7	ns
t_{PHL}				1.1	2	4.3	1.2	2	3.8	
Δt_{PLH}	A,B,C,D	Y		0.9	2	4.6	1	2	4.2	ns/pF
Δt_{PHL}				0.4	0.8	2.1	0.4	0.8	1.8	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to Section 7.

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

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D2939, AUGUST 1986

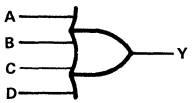
SystemCell™ 2-μm INTERNAL STANDARD CELL

- Choice of Four Performance Levels
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

positive logic equation

$$Y = A+B+C+D = \overline{\overline{A}\,\overline{B}\,\overline{C}\,\overline{D}}$$

logic symbol



FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	Y
H	X	X	X	H
X	H	X	X	H
X	X	H	X	H
X	X	X	H	H
L	L	L	L	L

description

The SN54ASC4072 and SN74ASC4072 are four-input positive-OR gate CMOS standard cells that implement the equivalent of one-half of the SN54HC4072/SN74HC4072. The standard-cell library contains four physical implementations to provide the custom IC designer a choice between four performance levels for optimizing designs. Each option is designated and called from the engineering workstation input using the following cell names to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		TYPICAL DELAY C_L = 1 pF	RELATIVE CELL AREA TO NA210LH
OR410LH	Label: OR4n0LH A,B,C,D,Y;	3.1 ns	2
OR420LH		3.1 ns	2.25
OR440LH		2.7 ns	3.55
OR460LH		2.7 ns	5.25

The SN54ASC4072 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC4072 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS	OR410LH TYP	OR410LH MAX	OR420LH TYP	OR420LH MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current	SN54ASC4072	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0,		225		270	nA
		SN74ASC4072	T_A = MIN to MAX		13.5		16.2	
C_i	Input capacitance		V_{CC} = 5 V, T_A = 25°C	0.11		0.11		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, t_r = t_f = 5 ns, T_A = 25°C	0.92		1.83		pF

PARAMETER			TEST CONDITIONS	OR440LH TYP	OR440LH MAX	OR460LH TYP	OR460LH MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current	SN54ASC4072	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0,		404		597	nA
		SN74ASC4072	T_A = MIN to MAX		24.2		35.8	
C_i	Input capacitance		V_{CC} = 5 V, T_A = 25°C	0.22		0.33		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, t_r = t_f = 5 ns, T_A = 25°C	3.46		5.48		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

OR410LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC4072 MIN	SN54ASC4072 TYP‡	SN54ASC4072 MAX	SN74ASC4072 MIN	SN74ASC4072 TYP‡	SN74ASC4072 MAX	UNIT
t_{PLH}	A,B,C,D	Y	C_L = 0	0.9	1.9	4.1	0.9	1.9	3.7	ns
t_{PHL}				1.2	2.5	7	1.3	2.5	6.2	
t_{PLH}	A,B,C,D	Y	C_L = 1 pF	1.4	2.9	6.4	1.5	2.9	5.8	ns
t_{PHL}				1.6	3.3	8.9	1.7	3.3	7.9	
Δt_{PLH}	A,B,C,D	Y		0.5	1	2.4	0.5	1	2.2	ns/pF
Δt_{PHL}				0.3	0.8	2	0.4	0.8	1.8	

OR420LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC4072 MIN	SN54ASC4072 TYP‡	SN54ASC4072 MAX	SN74ASC4072 MIN	SN74ASC4072 TYP‡	SN74ASC4072 MAX	UNIT
t_{PLH}	A,B,C,D	Y	C_L = 0	1.1	2.2	5.3	1.2	2.2	4.7	ns
t_{PHL}				1.4	3	8.3	1.5	3	7.4	
t_{PLH}	A,B,C,D	Y	C_L = 1 pF	1.4	2.7	6.5	1.5	2.7	5.8	ns
t_{PHL}				1.6	3.5	9.6	1.7	3.5	8.5	
Δt_{PLH}	A,B,C,D	Y		0.2	0.5	1.2	0.2	0.5	1.1	ns/pF
Δt_{PHL}				0.2	0.5	1.4	0.2	0.5	1.2	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are V_{CC} = 5 V, T_A = 25°C.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

OR440LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC4072			SN74ASC4072			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A,B,C,D	Y	C_L = 0	1.1	2	4.4	1.2	2	4	ns
t_{PHL}				1.3	2.8	6.9	1.4	2.8	6.1	
t_{PLH}	A,B,C,D	Y	C_L = 1 pF	1.2	2.3	5	1.3	2.3	4.5	ns
t_{PHL}				1.4	3.1	7.7	1.5	3.1	6.8	
Δt_{PLH}	A,B,C,D	Y		0.1	0.3	0.7	0.1	0.3	0.6	ns/pF
Δt_{PHL}				0.1	0.3	0.8	0.1	0.3	0.8	

OR460LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC4072			SN74ASC4072			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A,B,C,D	Y	C_L = 0	1	2	4.4	1.1	2	3.9	ns
t_{PHL}				1.3	2.8	7.1	1.4	2.8	6.4	
t_{PLH}	A,B,C,D	Y	C_L = 1 pF	1.1	2.2	4.8	1.2	2.2	4.3	ns
t_{PHL}				1.4	3	7.7	1.5	3	6.9	
Δt_{PLH}	A,B,C,D	Y		0.1	0.2	0.5	0.1	0.2	0.5	ns/pF
Δt_{PHL}				0.1	0.2	0.7	0.1	0.2	0.6	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to Section 7.

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

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SystemCell™ 2-μm INTERNAL STANDARD CELL

- **Choice of Four Performance Levels**
- **Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V**
- **Functional Operation Over V_{CC} Range of 2 V to 6 V**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol

FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
H	X	X	H
X	H	X	H
X	X	H	H
L	L	L	L

positive logic equation

$$Y = A+B+C = \overline{\overline{A}\,\overline{B}\,\overline{C}}$$

description

The SN54ASC4075 and SN74ASC4075 are 3-input positive-OR gate CMOS standard cells that implement the equivalent of one-third of the SN54HC4075 or SN74HC4075. The standard-cell library contains four physical implementations to provide the custom IC designer a choice between four performance levels for optimizing designs. Each option is designated and called from the engineering workstation input using the following cell names to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		TYPICAL DELAY C_L = 1 pF	RELATIVE CELL AREA TO NA210LH
OR310LH	Label: OR3n0LH A,B,C,Y;	2.7 ns	2
OR320LH		2.7 ns	2.25
OR340LH		2.2 ns	3.5
OR360LH		2.2 ns	5.25

The SN54ASC4075 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC4075 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS	OR310LH TYP	OR310LH MAX	OR320LH TYP	OR320LH MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current	SN54ASC4075	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0,		201		234	nA
		SN74ASC4075	T_A = MIN to MAX		12.1		14	
C_i	Input capacitance		V_{CC} = 5 V, T_A = 25°C	0.11		0.11		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, t_r = t_f = 3 ns, T_A = 25°C	0.9		1.71		pF

PARAMETER			TEST CONDITIONS	OR340LH TYP	OR340LH MAX	OR360LH TYP	OR360LH MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current	SN54ASC4075	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0,		362		526	nA
		SN74ASC4075	T_A = MIN to MAX		21.7		31.6	
C_i	Input capacitance		V_{CC} = 5 V, T_A = 25°C	0.21		0.33		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, t_r = t_f = 3 ns, T_A = 25°C	3.51		5.36		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

OR310LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC4075 MIN	SN54ASC4075 TYP‡	SN54ASC4075 MAX	SN74ASC4075 MIN	SN74ASC4075 TYP‡	SN74ASC4075 MAX	UNIT
t_{PLH}	A,B,C	Y	C_L = 0	0.8	1.6	3.5	0.8	1.6	3.2	ns
t_{PHL}				1	2	5	1.1	2	4.5	
t_{PLH}	A,B,C	Y	C_L = 1 pF	1.3	2.6	5.8	1.4	2.6	5.2	ns
t_{PHL}				1.4	2.7	6.8	1.5	2.7	6.1	
Δt_{PLH}	A,B,C	Y		0.5	1	2.3	0.5	1	2.1	ns/pF
Δt_{PHL}				0.3	0.7	1.8	0.3	0.7	1.6	

OR320LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC4075 MIN	SN54ASC4075 TYP‡	SN54ASC4075 MAX	SN74ASC4075 MIN	SN74ASC4075 TYP‡	SN74ASC4075 MAX	UNIT
t_{PLH}	A,B,C	Y	C_L = 0	0.8	1.9	4.2	0.9	1.9	3.8	ns
t_{PHL}				1.2	2.4	6	1.2	2.4	5.4	
t_{PLH}	A,B,C	Y	C_L = 1 pF	1.1	2.4	5.3	1.2	2.4	4.8	ns
t_{PHL}				1.4	2.9	7.2	1.5	2.9	6.4	
Δt_{PLH}	A,B,C	Y		0.2	0.5	1.2	0.2	0.5	1.1	ns/pF
Δt_{PHL}				0.2	0.5	1.2	0.2	0.5	1.1	

† Propagation delay times are measured from 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are V_{CC} = 5 V, T_A = 25°C.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

OR340LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC4075			SN74ASC4075			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A,B,C	Y	C_L = 0	0.9	1.7	3.7	1	1.7	3.4	ns
t_{PHL}				1.1	2.1	5.3	1.2	2.1	4.7	
t_{PLH}	A,B,C	Y	C_L = 1 pF	1	2	4.3	1.1	2	3.9	ns
t_{PHL}				1.2	2.4	6	1.3	2.4	5.2	
Δt_{PLH}	A,B,C	Y		0.1	0.3	0.7	0.1	0.3	0.6	ns/pF
Δt_{PHL}				0.1	0.3	0.7	0.1	0.3	0.7	

OR360LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC4075			SN74ASC4075			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A,B,C	Y	C_L = 0	0.9	1.7	3.5	1	1.7	3.2	ns
t_{PHL}				1.1	2.2	5	1.2	2.2	4.5	
t_{PLH}	A,B,C	Y	C_L = 1 pF	1	1.9	4	1.1	1.9	3.6	ns
t_{PHL}				1.2	2.4	5.6	1.3	2.4	5	
Δt_{PLH}	A,B,C	Y		0.08	0.2	0.5	0.09	0.2	0.5	ns/pF
Δt_{PHL}				0.06	0.2	0.6	0.08	0.2	0.5	

† Propagation delay times are measured from 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to Section 7.

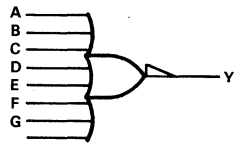
All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

D2939, AUGUST 1986

SystemCell™ 2-μm INTERNAL STANDARD CELL

- Choice of Two Performance Levels
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol



positive logic equation

$$Y = \overline{A+B+C+D+E+F+G+H}$$

$$= \overline{A}\,\overline{B}\,\overline{C}\,\overline{D}\,\overline{E}\,\overline{F}\,\overline{G}\,\overline{H}$$

FUNCTION TABLE

INPUTS								OUTPUT
A	B	C	D	E	F	G	H	Y
H	X	X	X	X	X	X	X	L
X	H	X	X	X	X	X	X	L
X	X	H	X	X	X	X	X	L
X	X	X	H	X	X	X	X	L
X	X	X	X	H	X	X	X	L
X	X	X	X	X	H	X	X	L
X	X	X	X	X	X	H	X	L
X	X	X	X	X	X	X	H	L
L	L	L	L	L	L	L	L	H

description

The SN54ASC4078 and SN74ASC4078 are eight-input positive-NOR gate CMOS standard cells that implement the equivalent of one HC4078. The standard-cell library contains two physical implementations to provide the custom IC designer a choice between two performance levels for optimizing designs. Each option is designated and called from the engineering workstation input using the following cell names to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		TYPICAL DELAY C_L = 1 pF	RELATIVE CELL AREA TO NA210LH
NO810LH	Label: NO8n0LH A,B,C,D,E,F,G,H,Y;	3.4 ns	3.5
NO820LH		4.9 ns	4.5

The SN54ASC4078 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC4078 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS	NO810LH		NO820LH		UNIT
				TYP	MAX	TYP	MAX	
V_T	Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current	SN54ASC4078	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0,		409		465	nA
		SN74ASC4078	T_A = MIN to MAX		24.5		27.9	
C_i	Input capacitance		V_{CC} = 5 V, T_A = 25°C	0.11		0.2		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, t_r = t_f = 3 ns, T_A = 25°C	1.54		0.65		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

NO810LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC4078			SN74ASC4078			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A thru H	Y	C_L = 0	1.4	3	8.3	1.5	3	7.4	ns
t_{PHL}				1	2.1	5	1.1	2.1	4.5	
t_{PLH}	A thru H	Y	C_L = 1 pF	1.9	4	10.5	2.1	4	9.3	ns
t_{PHL}				1.2	2.7	6.3	1.4	2.7	5.6	
Δt_{PLH}	A thru H	Y		0.4	1	2.2	0.5	1	2	ns/pF
Δt_{PHL}				0.2	0.6	1.4	0.2	0.6	1.2	

NO820LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC4078			SN74ASC4078			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A thru H	Y	C_L = 0	1.1	2.7	7.8	1.1	2.7	7	ns
t_{PHL}				1.1	1.8	4.1	1.2	1.8	3.6	
t_{PLH}	A thru H	Y	C_L = 1 pF	3	6.7	17.2	3.2	6.7	15.5	ns
t_{PHL}				1.8	3.1	7.4	1.9	3.1	6.5	
Δt_{PLH}	A thru H	Y		1.9	4	9.4	2	4	8.6	ns/pF
Δt_{PHL}				0.5	1.3	3.7	0.6	1.3	3.1	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to Section 7.

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

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SystemCell™ 2-μm INPUT STANDARD CELL

- 1.1 ns Typical Propagation Delay with 1-pF Load
- Incorporates Circuitry to Protect Against ESD and Latch-Up
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol

FUNCTION TABLE

INPUT A	OUTPUT Y
H	L
L	H

positive logic equation

$Y = \overline{A}$

description

The SN54ASC5000 and SN74ASC5000 are inverting input buffer CMOS standard-cell functions that interface external inputs with CMOS internal cells. This cell function exists in two versions (''E'' and ''F'') with different physical implementations to allow the final IC area to be optimized. Since the electrical performance of each version is identical, for simplicity only one version (the ''F'' cell) will be contained in the engineering workstation cell libraries. Determination of the most appropriate cell version will be made during the layout stage. The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		CELL LAYOUT ASPECT RATIO	RELATIVE CELL AREA TO NA210LH
IPE00LH IPF00LH	Label: IPF00LH A,Y;	minimum height minimum width	29.4 31.5

Each cell incorporates circuit elements designed specifically to actively bypass and dissipate electrostatic discharges with potentials ranging up to 4 kilovolts. Guard-ring structures are employed that provide current management techniques for the cell to recover from exposure to high currents up to 400 milliamperes, thereby negating most common sources that can produce a latch-up condition.

The SN54ASC5000 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC5000 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		SN54ASC5000		SN74ASC5000		UNIT
					TYP	MAX	TYP	MAX	
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.5		2.5		V
I_{IH}	High-level input current		$V_{IH} = V_{CC}$			±1		±1	μA
I_{IL}	Low-level input current		V_{IL} = 0			±1		±1	μA
I_{CC}	Supply current	IPA06LH	$V_I = V_{CC}$ or 0			1000		60	nA
			V_I = 2 V or 0.8 V			4.4		4.2	mA
		IPC00LH	$V_I = V_{CC}$ or 0			1253		75.2	nA
			V_I = 2 V or 0.8 V			4.4		4.2	mA
C_i	Intrinsic input capacitance†		V_{CC} = 5 V,	T_A = 25°C	2.3		2.3		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	$t_r = t_f$ = 3 ns,	2		2		pF

† Total input capacitance is dependent on the package type and is equal to the sum of package capacitance and intrinsic input capacitance.

switching characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5000			SN74ASC5000			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
t_{PLH}	A	Y	C_L = 0	0.5	0.7	1.3	0.5	0.7	1.2	ns
t_{PHL}				0.2	0.7	1.6	0.3	0.7	1.4	
t_{PLH}	A	Y	C_L = 1 pF	0.7	1.1	1.9	0.7	1.1	1.8	ns
t_{PHL}				0.5	1.1	2.4	0.6	1.1	2.1	
Δt_{PLH}	A	Y		0.2	0.4	0.7	0.2	0.4	0.6	ns/pF
Δt_{PHL}				0.2	0.4	0.9	0.2	0.4	0.8	

‡ Propagation delay times are measured from the 50% point of V_I to the 44% point of V_O with $t_r = t_f$ = 4 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to Section 7.

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SystemCell™ 2-μm INPUT STANDARD CELL

- 2.1 ns Typical Propagation Delay with 1-pF Load
- Incorporates Circuitry to Protect Against ESD and Latch-Up
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol

FUNCTION TABLE

INPUT A	OUTPUT Y
H	L
L	H

positive logic equation

$Y = \overline{A}$

description

The SN54ASC5001 and SN74ASC5001 are inverting input buffer CMOS standard cells that translate TTL input voltage levels to CMOS internal-cell voltage levels. This cell function exists in two versions (''E'' and ''F'') with different physical implementations to allow the final IC area to be optimized. Since the electrical performance of each version is identical, for simplicity only one version (the ''F'' cell) will be contained in the engineering workstation cell libraries. Determination of the most appropriate cell version will be made during the layout stage. The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		CELL LAYOUT ASPECT RATIO	RELATIVE CELL AREA TO NA210LH
IPE03LH IPF03LH	Label: IPF03LH A,Y;	minimum height minimum width	28.6 31.5

The cells incorporate circuit elements designed to actively bypass and dissipate electrostatic discharges with potentials ranging up to 4 kilovolts. Guard-ring structures are employed that provide current management techniques for the cell to recover from exposure to high currents of up to 400 milliamperes, thereby negating most common sources that can produce a latch-up condition.

The SN54ASC5001 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC5001 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 2 in Section 2.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		SN54ASC5001		SN74ASC5001		UNIT
					TYP	MAX	TYP	MAX	
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	1.3		1.3		V
I_I	Input current		V_I = 0 to V_{CC}			±1		±1	μA
I_{CC}	Supply current	IPE03LH	V_I = V_{CC} or 0			910		54.6	nA
			V_I = 2 V or 0.8 V			1.21		1.13	mA
		IPF03LH	V_I = V_{CC} or 0			1223		73.4	nA
			V_I = 2 V or 0.8 V			1.21		1.13	mA
C_i	Intrinsic input capacitance†		V_{CC} = 5 V,	T_A = 25°C	2.1		2.1		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	16.5		16.5		pF

† Total input capacitance is dependent on the package type and is equal to the sum of package capacitance and intrinsic input capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5001			SN74ASC5001			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
t_{PLH}	A	Y	C_L = 0	0.6	1	2.2	0.7	1	2	ns
t_{PHL}				0.5	0.8	1.4	0.5	0.8	1.3	
t_{PLH}	A	Y	C_L = 1 pF	1.6	2.9	6.3	1.8	2.9	5.7	ns
t_{PHL}				0.8	1.3	2.2	0.8	1.3	2.1	
Δt_{PLH}	A	Y		1	1.9	4.2	1	1.9	3.8	ns/pF
Δt_{PHL}				0.3	0.5	0.9	0.3	0.5	0.8	

‡ Propagation delay times are measured from the 1.3 V point of V_I (0 to 3 V) to the 44% point of V_O with t_r = t_f = 2 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
§ Typical values are at V_{CC} = V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to Section 7.

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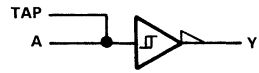
D2939, AUGUST 1986

SystemCell™ 2-μm INPUT STANDARD CELL

- 4.8 ns Typical Propagation Delay with 1-pF Load
- Incorporates Circuitry to Protect Against ESD and Latch-Up
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol



FUNCTION TABLE

INPUT A	OUTPUT Y
H	L
L	H

positive logic equation

$Y = \overline{A}$

description

The SN54ASC5002 and SN74ASC5002 are inverting Schmitt-trigger input buffer CMOS standard cells that interface CMOS inputs with CMOS internal cells. This cell function exists in two versions (''E'' and ''F'') with different physical implementations to allow the final IC area to be optimized. Since the electrical performance of each version is identical, for simplicity only one version (the ''F'' cell) will be contained in the engineering workstation cell libraries. Determination of the most appropriate cell version will be made during the layout stage. The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		CELL LAYOUT ASPECT RATIO	RELATIVE CELL AREA TO NA210LH
IPE06LH IPF06LH	Label: IPF06LH A,TAP,Y;	minimum height minimum width	29.4 33

The cell incorporates a pull-up tap to simplify termination of the input. This tap may be used in conjunction with an active pull-up/pull-down terminator in the SNASC237x group or the pull-up tap may be left unconnected. When the terminator is used it ensures that the input will be driven to a high- or low-logic level thereby avoiding exposure to a high-impedance or floating condition. Refer to Section 7 for implementation of the pull-up.

The cells incorporate circuit elements designed to actively bypass and dissipate electrostatic discharges with potentials ranging up to 4 kilovolts. Guard-ring structures are employed that provide current management techniques for the cell to recover from exposure to high currents of up to 400 milliamperes, thereby negating most common sources that can produce a latch-up condition.

The SN54ASC5002 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC5002 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 2 in Section 2.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	SN54ASC5002			SN74ASC5002			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{T+}	Positive-going threshold level			2.9	3.2	3.5	2.9	3.2	3.5	V
V_{T-}	Negative-going threshold level			1.5	1.7	1.9	1.5	1.7	1.9	V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)‡				1.5			1.5		V
I_I	Input current		V_I = 0 to V_{CC}			±1			±1	μA
I_{CC}	Supply current	IPE06LH	V_I = V_{CC} or 0			1022			61.3	nA
			V_I = 3.15 V or 0.9 V			2.44			1.21	mA
		IPF06LH	V_I = V_{CC} or 0			1351			81	nA
			V_I = 3.15 V or 0.9 V			1.23			1.17	mA
C_i	Intrinsic input capacitance§		V_{CC} = 5 V, T_A = 25°C		2.1			2.1		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, $t_r = t_f$ = 3 ns, T_A = 25°C		1.3			1.3		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5002			SN74ASC5002			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 0	2.1	2.7	4.7	2.1	2.7	4.4	ns
t_{PHL}				2.1	2.9	5.9	2.1	2.9	5.3	
t_{PLH}	A	Y	C_L = 1 pF	3	4.5	8.8	3.1	4.5	8.1	ns
t_{PHL}				3.1	5	11.3	3.2	5	10	
Δt_{PLH}	A	Y		0.9	1.8	4.1	0.9	1.8	3.7	ns/pF
Δt_{PHL}				1	2.1	5.5	1.1	2.1	4.7	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}.
§ Total input capacitance is dependent on the package type and is equal to the sum of package capacitance and intrinsic input capacitance. The value shown includes the pull-up tap.
¶ Propagation delay times times are measured from the 50% point of V_I to the 44% point of V_O with $t_r = t_f$ = 4 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance

DESIGN CONSIDERATIONS

Refer to Section 7.

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SystemCell™ 2-μm INPUT STANDARD CELL

- 8 ns Typical Propagation Delay with 1-pF Load
- Incorporates Circuitry to Protect Against ESD and Latch-Up
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol

FUNCTION TABLE

INPUT A	OUTPUT Y
H	L
L	H

positive logic equation

$Y = \overline{A}$

description

The SN54ASC5003 and SN74ASC5003 are inverting Schmitt-trigger input buffer CMOS standard cells that translate TTL input voltage levels to CMOS internal cell voltage levels. This cell function exists in two versions ("E" and "F") with different physical implementations to allow the final IC area to be optimized. Since the electrical performance of each version is identical, for simplicity only one version (the "F" cell) will be contained in the engineering workstation cell libraries. Determination of the most appropriate cell version will be made during the layout stage. The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		CELL LAYOUT ASPECT RATIO	RELATIVE CELL AREA TO NA210LH
IPE08LH IPF08LH	Label: IPE08LH A,TAP,Y;	minimum height minimum width	29.4 37.5

The cell incorporates a pull-up tap to simplify termination of the input. This tap may be used in conjunction with an active pull-up/pull-down terminator in the SNASC237x group or the pull-up tap may be left unconnected. When the terminator is used it ensures that the input will be driven to a high- or low-logic level thereby avoiding exposure to a high-impedance or floating condition.

The cells incorporate circuit elements designed to actively bypass and dissipate electrostatic discharges with potentials ranging up to 4 kilovolts. Guard-ring structures are employed that provide current management techniques for the cell to recover from exposure to high currents of up to 400 milliamperes, thereby negating most common sources that can produce a latch-up condition.

The SN54ASC5003 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC5003 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 2 in Section 2.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	SN54ASC5003			SN74ASC5003			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{T+}	Positive-going threshold level			1.5	1.8	2	1.5	1.8	2	V
V_{T-}	Negative-going threshold level			0.6	0.9	1.1	0.6	0.9	1.1	V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)				900			900		mV
I_I	Input current		V_I = 0 to V_{CC}			±1			±1	μA
I_{CC}	Supply current	IPE08LH	V_I = V_{CC} or 0			1125			67.5	nA
			V_I = 2 V or 0.8 V			1.47			1.37	mA
		IPF08LH	V_I = V_{CC} or 0			1549			92.9	nA
			V_I = 2 V or 0.8 V			1.45			1.35	mA
C_i	Intrinsic input capacitance‡		V_{CC} = 5 V, T_A = 25°C		2.3			2.3		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C, $t_r = t_f$ = 3 ns,		19			19		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

IPE08LH

PARAMETER§	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5003			SN74ASC5003			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 0	3	6	19	3.1	6	17	ns
t_{PHL}				1.1	1.4	2.3	1.1	1.4	2.2	
t_{PLH}	A	Y	C_L = 1 pF	6.3	13	35	6.8	13	32	ns
t_{PHL}				1.3	2	3.8	1.4	2	3.5	
Δt_{PLH}	A	Y		3.4	7	17	3.7	7	15	ns/pF
Δt_{PHL}				0.2	0.6	1.5	0.2	0.6	1.3	

IPF08LH

PARAMETER§	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5003			SN74ASC5003			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 0	3.5	7	18	3.7	7	17	ns
t_{PHL}				1.1	1.5	2.3	1.1	1.5	2.2	
t_{PLH}	A	Y	C_L = 1 pF	7	14	35	7.5	14	32	ns
t_{PHL}				1.3	2.1	3.8	1.4	2.1	3.5	
Δt_{PLH}	A	Y		3.5	7	17	3.8	7	15	ns/pF
Δt_{PHL}				0.2	0.6	1.5	0.2	0.6	1.3	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Total input capacitance is dependent on the package type and is equal to the sum of package capacitance and intrinsic input capacitance. The value shown includes the pull-up tap.
§ Propagation delay times times are measured from the 1.3 V point of V_I (0 to 3 V) to the 44% point of V_O with $t_r = t_f$ = 2 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance

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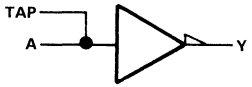
SystemCell™ 2-μm INPUT STANDARD CELL

- 1 ns Typical Propagation Delay with 1-pF Load
- Incorporates Circuitry to Protect Against ESD and Latch-Up
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol



FUNCTION TABLE

INPUT A	OUTPUT Y
H	L
L	H

positive logic equation

$Y = \overline{A}$

description

The SN54ASC5004 and SN74ASC5004 are inverting input buffer CMOS standard cells that interface external CMOS inputs with CMOS internal cells. The cell is designated and called from the engineering workstation input using the following cell name and netlist label:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		CELL LAYOUT ASPECT RATIO	RELATIVE CELL AREA TO NA210LH
IPF02LH	Label: IPF02LH A,TAP,Y;	minimum width	35

The cell incorporates a pull-up tap to simplify termination of the input. This tap may be used in conjunction with an active pull-up/pull-down terminator in the 'ASC237x group or the pull-up tap may be left unconnected. When the terminator is used it ensures that the input will be driven to a high or low logic level, thereby avoiding exposure to a high-impedance or floating condition. Refer to Section 7 for implementation of the pull-up.

The cell incorporates circuit elements designed to actively bypass and dissipate electrostatic discharges with potentials ranging up to 4 kilovolts. Guard-ring structures are employed that provide current management techniques for the cell to recover from exposure to high currents of up to 400 milliamperes, thereby negating most common sources that can produce a latch-up condition.

The SN54ASC5004 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC5004 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 2 in Section 2.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ASC5004		SN74ASC5004		UNIT
				TYP	MAX	TYP	MAX	
V_T	Input threshold voltage	V_{CC} = 5 V,	T_A = 25°C	2.5		2.5		V
I_I	Input current	V_I = 0 to V_{CC}			±1		±1	μA
I_{CC}	Supply current	V_I = V_{CC} or 0			999		60	nA
		V_I = 3.15 V or 0.9 V			4.37		4.14	mA
C_i	Intrinsic input capacitance†	V_{CC} = 5 V,	T_A = 25°C	2.3		2.3		pF
C_{pd}	Equivalent power dissipation capacitance	V_{CC} = 5 V, T_A = 25°C	$t_r = t_f$ = 3 ns,	2		2		pF

† Total input capacitance is dependent on the package type and is equal to the sum of package capacitance and intrinsic input capacitance. The value shown includes the pull-up tap.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5004			SN74ASC5004			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
t_{PLH}	A	Y	C_L = 0	0.4	0.7	1.2	0.5	0.7	1.2	ns
t_{PHL}				0.3	0.6	1.5	0.3	0.6	1.3	
t_{PLH}	A	Y	C_L = 1 pF	0.7	1	1.8	0.7	1	1.8	ns
t_{PHL}				0.5	1	2.3	0.6	1	2.1	
Δt_{PLH}	A	Y		0.2	0.3	0.7	0.2	0.3	0.6	ns/pF
Δt_{PHL}				0.2	0.4	0.9	0.2	0.4	0.8	

‡ Propagation delay times are measured from the 50% point of V_I to the 44% point of V_O with $t_r = t_f$ = 4 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to Section 7.

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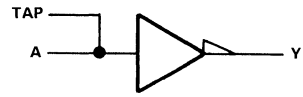
D2939, AUGUST 1986

SystemCell™ 2-μm INPUT STANDARD CELL

- 2.1 ns Typical Propagation Delay with 1-pF Load
- Incorporates Circuitry to Protect Against ESD and Latch-Up
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol



FUNCTION TABLE

INPUT A	OUTPUT Y
H	L
L	H

positive logic equation

$Y = \overline{A}$

description

The SN54ASC5005 and SN74ASC5005 are inverting input buffer CMOS standard cells that translate TTL input voltage levels to CMOS internal-cell voltage levels. This cell function exists in two versions (''E'' and ''F'') with different physical implementations to allow the final IC area to be optimized. Since the electrical performance of each version is identical, for simplicity only one version (the ''F'' cell) will be contained in the engineering workstation cell libraries. Determination of the most appropriate cell version will be made during the layout stage. The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		CELL LAYOUT ASPECT RATIO	RELATIVE CELL AREA TO NA210LH
IPE05LH IPF05LH	Label: IPF05LH A,TAP,Y;	minimum height minimum width	28.6 31.5

These input cells incorporate a pull-up tap to simplify termination of the input. This tap may be used in conjunction with an active pull-up/pull-down terminator from the 'ASC2370 through 'ASC2374 group, otherwise the pull-up tap may be left unconnected. When the terminator is used it ensures that the input will be driven to a high or low logic level thereby avoiding exposure to a high-impedance or floating condition.

The cells incorporate circuit elements designed to actively bypass and dissipate electrostatic discharges with potentials ranging up to 4 kilovolts. Guard-ring structures are employed that provide current management techniques for the cell to recover from exposure to high currents of up to 400 milliamperes, thereby negating most common sources that can produce a latch-up condition.

The SN54ASC5005 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC5005 is characterized for operation from −40°C to 85°C.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	SN54ASC5005		SN74ASC5005		UNIT
				TYP	MAX	TYP	MAX	
V_T	Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	1.3		1.3		V
I_I	Input current		V_I = V_{CC} or 0		±1		±1	μA
I_{CC}	Supply current	IPE05LH	V_I = V_{CC} or 0		905		54.3	nA
			V_I = 2 V or 0.8 V		1.21		1.13	mA
		IPF05LH	V_I = V_{CC} or 0		758		45.5	nA
			V_I = 2 V or 0.8 V		1.21		1.13	mA
C_i	Intrinsic input capacitance†		V_{CC} = 5 V, T_A = 25°C	2.1		2.1		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, t_r = t_f = 3 ns, T_A = 25°C	16		16		pF

†Total input capacitance is dependent on the package type and is equal to the sum of package capacitance and intrinsic input capacitance. The value shown includes the pull-up tap.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5005			SN74ASC5005			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
t_{PLH}	A	Y	C_L = 0	0.6	0.9	2	0.6	0.9	2	ns
t_{PHL}				0.4	0.9	1.3	0.5	0.9	1.3	
t_{PLH}	A	Y	C_L = 1 pF	1.6	2.8	6.2	1.7	2.8	5.5	ns
t_{PHL}				0.8	1.3	2.2	0.8	1.3	2	
Δt_{PLH}	A	Y		1	1.9	4.2	1	1.9	3.8	ns/pF
Δt_{PHL}				0.3	0.4	0.9	0.3	0.4	0.8	

‡Propagation delay times are measured from the 1.3 V point of V_I (0 to 3 V) to the 44% point of V_O with t_r = t_f = 2 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
§Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to Section 7.

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D2939, AUGUST 1986

SystemCell™ 2-μm INPUT STANDARD CELL

- Typical Propagation Delay with 1-pF Load
  1.9 ns for the IPE01LH
  1.1 ns for the IPF01LH
- Incorporates Circuitry to Protect Against ESD and Latch-Up
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol

FUNCTION TABLE

INPUT A	OUTPUT Y
H	H
L	L

positive logic equation

$Y = A$

description

The SN54ASC5006 and SN74ASC5006 are noninverting input buffer CMOS standard cells that buffer CMOS input voltage levels to CMOS internal-cell voltage levels. This cell function eixsts in two versions (''E'' and ''F'') with different physical implementations to allow the final IC area to be optimized. Since the electrical performance of each version is identical, for simplicity only one version (the ''F'' cell) will be contained in the engineering workstation cell libraries. Determination of the most appropriate cell version will be made during the layout stage. The cell is designated and called from the engineering workstation input using the following cell names to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		CELL LAYOUT ASPECT RATIO	RELATIVE CELL AREA TO NA210LH
IPE01LH IPF01LH	Label: IPF01LH A,Y;	minimum height minimum width	31 31.5

The cells incorporate circuit elements designed to actively bypass and dissipate electrostatic discharges with potentials ranging up to 4 kilovolts. Guard-ring structures are employed that provide current management techniques for the cell to recover from exposure to high currents of up to 400 milliamperes, thereby negating most common sources that can produce a latch-up condition.

The SN54ASC5006 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC5006 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 2 in Section 2.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		SN54ASC5006		SN74ASC5006		UNIT
					TYP	MAX	TYP	MAX	
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.5		2.5		V
I_I	Input current		V_I = V_{CC} or 0			±1		±1	μA
I_{CC}	Supply current	IPE01LH	V_I = V_{CC} or 0			1218		73.1	nA
			V_I = 3.15 V or 0.9 V			2.93		2.62	mA
		IPF01LH	V_I = V_{CC} or 0			1353		81.2	nA
			V_I = 3.15 V or 0.9 V			2.95		2.62	mA
C_i	Intrinsic input capacitance†		V_{CC} = 5 V,	T_A = 25°C	2		2		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	3		3		pF

† Total input capacitance is dependent on the package type and is equal to the sum of package capacitance and intrinsic input capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

IPE01LH

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5006			SN74ASC5006			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
t_{PLH}	A	Y	C_L = 0	0.9	1.7	3.7	1	1.7	3.4	ns
t_{PHL}				1	1.7	3.3	1	1.7	3.1	
t_{PLH}	A	Y	C_L = 1 pF	1	1.9	4.1	1.1	1.9	3.8	ns
t_{PHL}				1.1	1.9	3.7	1.1	1.9	3.4	
Δt_{PLH}	A	Y		0.07	0.2	0.5	0.09	0.2	0.4	ns/pF
Δt_{PHL}				0.1	0.2	0.5	0.1	0.2	0.4	

IPF01LH

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5006			SN74ASC5006			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
t_{PLH}	A	Y	C_L = 0	0.5	0.7	1.2	0.5	0.7	1.2	ns
t_{PHL}				0.2	0.7	1.5	0.3	0.7	1.4	
t_{PLH}	A	Y	C_L = 1 pF	0.7	1.1	1.9	0.7	1.1	1.8	ns
t_{PHL}				0.5	1.1	2.3	0.6	1.1	2.1	
Δt_{PLH}	A	Y		0.2	0.4	0.7	0.2	0.4	0.6	ns/pF
Δt_{PHL}				0.2	0.4	0.9	0.2	0.4	0.8	

‡ Propagation delay times are measured from the 50% point of V_I to the 44% point of V_O with t_r = t_f = 4 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
§ Typical values are at V_{CC} = V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to Section 7.

TEXAS INSTRUMENTS
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D2939, AUGUST 1986

SystemCell™ 2-μm INPUT STANDARD CELL

- **Typical Propagation Delay with 1-pF Load**
  2.1 ns for the IPE04LH and IPF04LH
  1.6 ns for the IPF12LH
- **Incorporates Circuitry to Protect Against ESD and Latch-Up**
- **Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V**
- **Functional Operation Over V_{CC} Range of 2 V to 6 V**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol

FUNCTION TABLE

INPUT A	OUTPUT Y
H	H
L	L

positive logic equation

$Y = A$

description

The SN54ASC5007 and SN74ASC5007 are noninverting input buffer CMOS standard cells that translate TTL input voltage levels to CMOS internal-cell voltage levels. This cell function exists in two versions (''E'' and ''F'') with different physical implementations to allow the final IC area to be optimized. Since the electrical performance of each version is identical, for simplicity only one version (the ''F'' cell) will be contained in the engineering workstation cell libraries. Determination of the most appropriate cell version will be made during the layout stage. The options are designated and called from the engineering workstation input using the following cell names to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		CELL LAYOUT ASPECT RATIO	RELATIVE CELL AREA TO NA210LH
IPE04LH IPF04LH	Label: IPF04LH A,Y;	minimum height minimum width	28.6 31.5
IPF12LH	Label: IPF12LH A,Y;	minimum width	37.5

The cells incorporate circuit elements designed to actively bypass and dissipate electrostatic discharges with potentials ranging up to 4 kilovolts. Guard-ring structures are employed that provide current management techniques for the cell to recover from exposure to high currents of up to 400 milliamperes, thereby negating most common sources that can produce a latch-up condition.

The SN54ASC5007 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC5007 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 2 in Section 2.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	SN54ASC5007 TYP	SN54ASC5007 MAX	SN74ASC5007 TYP	SN74ASC5007 MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	1.3		1.3		V
I_I	Input current		V_I = V_{CC} or 0		±1		±1	μA
I_{CC}	Supply current	IPE04LH	V_I = V_{CC} or 0		1040		62.4	nA
			V_I = 2 V or 0.8 V		1.21		1.13	mA
		IPF04LH	V_I = V_{CC} or 0		1307		78.4	nA
			V_I = 2 V or 0.8 V		1.2		1.13	mA
		IPF12LH	V_I = V_{CC} or 0		1303		78.2	nA
			V_I = 2 V or 0.8 V		3		2.81	mA
C_i	Intrinsic input capacitance†	IPE04LH	V_{CC} = 5 V, T_A = 25°C	1.9		1.9		pF
		IPF04LH		2.2		2.2		
		IPF12LH		2.8		2.8		
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, t_r = t_f = 3 ns, T_A = 25°C	18		18		pF

† Total input capacitance is dependent on the package type and is equal to the sum of package capacitance and intrinsic input capacitance.

4 Data Sheets

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

IPE04LH and IPF04LH

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5007 MIN	SN54ASC5007 TYP§	SN54ASC5007 MAX	SN74ASC5007 MIN	SN74ASC5007 TYP§	SN74ASC5007 MAX	UNIT
t_{PLH}	A	Y	C_L = 0	0.8	1.3	2.5	0.8	1.3	2.3	ns
t_{PHL}				1.2	2.3	5.4	1.3	2.3	4.8	
t_{PLH}	A	Y	C_L = 1 pF	1	1.6	3.2	1	1.6	3	ns
t_{PHL}				1.4	2.6	6.2	1.5	2.6	5.5	
Δt_{PLH}	A	Y		0.1	0.3	0.8	0.1	0.3	0.7	ns/pF
Δt_{PHL}				0.1	0.3	0.8	0.1	0.3	0.8	

IPF12LH

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5007 MIN	SN54ASC5007 TYP§	SN54ASC5007 MAX	SN74ASC5007 MIN	SN74ASC5007 TYP§	SN74ASC5007 MAX	UNIT
t_{PLH}	A	Y	C_L = 0	0.5	1.1	2	0.6	1.1	1.9	ns
t_{PHL}				0.8	1.6	3.5	0.9	1.6	3.1	
t_{PLH}	A	Y	C_L = 1 pF	0.7	1.4	2.7	0.7	1.4	2.5	ns
t_{PHL}				1	1.8	4.2	1	1.8	3.7	
Δt_{PLH}	A	Y		0.1	0.3	0.7	0.1	0.3	0.7	ns/pF
Δt_{PHL}				0.1	0.2	0.7	0.1	0.2	0.6	

‡ Propagation delay times are measured from the 1.3 V point of V_I (0 to 3 V) to the 44% point of V_O with t_r = t_f = 2 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
§ Typical values are at V_{CC} = V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to Section 7.

TEXAS INSTRUMENTS
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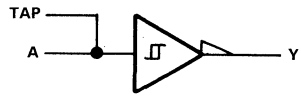
SystemCell™ 2-μm INPUT STANDARD CELL

- 7.5 ns Typical Propagation Delay with 1-pF Load
- Incorporates Circuitry to Protect Against ESD and Latch-Up
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol



FUNCTION TABLE

INPUT A	OUTPUT Y
H	L
L	H

positive logic equation

$Y = \overline{A}$

description

The SN54ASC5010 and SN74ASC5010 are inverting Schmitt-trigger input buffer CMOS standard cells that translate TTL input voltage levels to CMOS internal-cell voltage levels. This cell function exists in two versions (''E'' and ''F'') with different physical implementations to allow the final IC area to be optimized. Since the electrical performance of each version is identical, for simplicity only one version (the ''F'' cell) will be contained in the engineering workstation cell libraries. Determination of the most appropriate cell version will be made during the layout stage. The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		CELL LAYOUT ASPECT RATIO	RELATIVE CELL AREA TO NA210LH
IPE10LH IPF10LH	Label: IPF10LH A,TAP,Y;	minimum height minimum width	29.4 37.5

These input cells incorporate a pull-up tap to simplify termination of the input. This tap may be used in conjunction with an active pull-up/pull-down terminator from the 'ASC2370 through 'ASC2374 group, otherwise the pull-up tap may be left unconnected. When the terminator is used it ensures that the input will be driven to a high or low logic level thereby avoiding exposure to a high-impedance or floating condition.

The cells incorporate circuit elements designed to actively bypass and dissipate electrostatic discharges with potentials ranging up to 4 kilovolts. Guard-ring structures are employed that provide current management techniques for the cell to recover from exposure to high currents of up to 400 milliamperes, thereby negating most common sources that can produce a latch-up condition.

The SN54ASC5010 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC5010 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	SN54ASC5010			SN74ASC5010			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{T+}	Positive-going threshold level			1.5	1.8	2	1.5	1.8	2	V
V_{T-}	Negative-going threshold level			0.6	0.9	1.1	0.6	0.9	1.1	V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)				900			900		mV
I_I	Input current		$V_I = V_{CC}$ or 0			±1			±1	μA
I_{CC}	Supply current	IPE10LH	$V_I = V_{CC}$ or 0			1125			67.5	nA
			V_I = 2 V or 0.8 V			1.47			1.37	mA
		IPF10LH	$V_I = V_{CC}$ or 0			1548			92.9	nA
			V_I = 2 V or 0.8 V			1.45			1.37	mA
C_i	Intrinsic input capacitance†		V_{CC} = 5 V, T_A = 25°C		2.1			2.1		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, $t_r = t_f$ = 3 ns, T_A = 25°C		20			20		pF

†Total input capacitance is dependent on the package type and is equal to the sum of package capacitance and intrinsic input capacitance. The value shown includes the pull-up tap.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5010			SN74ASC5010			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
t_{PLH}	A	Y	C_L = 0	2.9	6	16	3.1	6	14	ns
t_{PHL}				1.1	1.4	2.2	1.1	1.4	2	
t_{PLH}	A	Y	C_L = 1 pF	6.3	13	33	6.8	13	29	ns
t_{PHL}				1.3	2	3.6	1.4	2	3.3	
Δt_{PLH}	A	Y		3.4	7	18	3.7	7	16	ns/pF
Δt_{PHL}				0.2	0.6	1.5	0.2	0.6	1.3	

‡Propagation delay times are measured from the 1.3 V point of V_I (0 to 3 V) to the 44% point of V_O with $t_r = t_f$ = 2 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
§Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

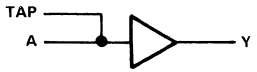
Refer to Section 7.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SystemCell™ 2-μm INPUT STANDARD CELL

- 2.1 ns Typical Propagation Delay With 1-pF Load
- Incorporates Circuitry to Protect Against ESD and Latch-Up
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol



FUNCTION TABLE

INPUT A	OUTPUT Y
H	H
L	L

positive logic equation

Y = A

description

The SN54ASC5013 and SN74ASC5013 are noninverting input buffer CMOS standard cells that translate TTL input voltage levels to CMOS internal-cell voltage levels. The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		CELL LAYOUT ASPECT RATIO	RELATIVE CELL AREA TO NA210LH
IPF13LH	Label: IPF13LH A,TAP,Y;	minimum height	29.4

This input cell incorporates a pull-up tap to simplify termination of the input. This tap may be used in conjunction with either an active pull-up/pull-down terminator from the 'ASC2370 through 'ASC2374 group, otherwise the pull-up tap may be left unconnected. When the terminator is used it ensures that the input will be driven to a high or low logic level thereby avoiding exposure to a high-impedance or floating condition.

The cell incorporates circuit elements designed to actively bypass and dissipate electrostatic discharges with potentials ranging up to 4 kilovolts. Guard-ring structures are employed that provide current management techniques for the cell to recover from exposure to high currents of up to 400 milliamperes, thereby negating most common sources that can produce a latch-up condition.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ASC5013		SN74ASC5013		UNIT
				TYP	MAX	TYP	MAX	
V_T	Input threshold voltage	V_{CC} = 5 V,	T_A = 25°C	1.3		1.3		V
I_I	Input current	$V_I = V_{CC}$ or 0			±1		±1	μA
I_{CC}	Supply current	$V_I = V_{CC}$ or 0			1037		62.2	nA
		V_I = 2 V or 0.8 V			1.21		1.13	mA
C_i	Input capacitance†	V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		pF
C_{pd}	Equivalent power dissipation capacitance	V_{CC} = 5 V, T_A = 25°C	$t_r = t_f$ = 3 ns,	18		18		pF

†Total input capacitance is dependent on the package type and is equal to the sum of package capacitance and intrinsic input capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5013			SN74ASC5013			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
t_{PLH}	A	Y	C_L = 0	0.8	1.3	2.4	0.8	1.3	2.3	ns
t_{PHL}				1.3	2.3	5.3	1.3	2.3	4.7	
t_{PLH}	A	Y	C_L = 1 pF	1	1.6	3.2	1	1.6	2.9	ns
t_{PHL}				1.4	2.6	6.1	1.5	2.6	5.4	
Δt_{PLH}	A	Y		0.1	0.3	0.8	0.1	0.3	0.7	ns/pF
Δt_{PHL}				0.1	0.3	0.8	0.1	0.3	0.8	

‡Propagation delay times are measured from V_I = 1.3 V to the 44% point of V_O with $t_r = t_f$ = 2 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
§Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to Section 7.

TEXAS INSTRUMENTS
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D2939, AUGUST 1986

SystemCell™ 2-μm OUTPUT STANDARD CELL

- **Typical Propagation Delays**
  2.7 ns with 15-pF Load
  4.7 ns with 50-pF Load
- **Output Current Ratings**
  SN54ASC5100 I_{OL} = 3.4 mA
  I_{OH} = −3.4 mA
  SN74ASC5100 I_{OL} = 4 mA
  I_{OH} = −4 mA
- **Incorporates Circuitry to Protect Against ESD and Latch-Up**
- **Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V**
- **Functional Operation Over V_{CC} Range of 2 V to 6 V**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol

FUNCTION TABLE

INPUT A	OUTPUT Y
H	H
L	L

positive logic equation

$Y = A$

description

The SN54ASC5100 and SN74ASC5100 are noninverting output buffer standard cells that interface internal cells with TTL or CMOS external loads. This cell function exists in two versions (''E'' and ''F'') with different physical implementations to allow the final IC area to be optimized. Since the electrical performance of each version is identical, for simplicity only one version (the ''F'' cell) will be contained in the engineering workstation cell libraries. Determination of the most appropriate cell version will be made during the layout stage. The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		CELL LAYOUT ASPECT RATIO	RELATIVE CELL AREA TO NA210LH
OPE40LH OPF40LH	Label: OPF40LH A,Y;	minimum height minimum width	31.8 39

The cells incorporate circuit elements designed to actively bypass and dissipate electrostatic discharges with potentials ranging up to 4 kilovolts. Guard-ring structures are employed that provide current management techniques for the cell to recover from exposure to high currents of up to 400 milliamperes, thereby negating most common sources that can produce a latch-up condition.

These output cells have been designed to provide low-impedance drive levels for both the high- and low-logic-level states. As a result, passive resistance has been omitted in series with the output transistors. Shorting a high-level output to ground or a low-level output to V_{CC} will cause current flow above that recommended for normal opeation. Therefore, it is recommended that outputs not be shorted directly to ground or V_{CC}.

The dynamic drive capability of each output is specified by the delta propagation delay time parameter included with the switching characteristics. The delta delay times provide a means for making direct comparisons of the various output responses with changes in capacitive loading.

The SN54ASC5100 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC5100 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 3 in Section 2. The maximum high-level or low-level output current is 3.4 milliamperes for the SN54ASC5100 and 4 milliamperes for the SN74ASC5100.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	SN54ASC5100			SN74ASC5100			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_T	Input threshold voltage		V_{CC} = 5 V, T_A = 25°C		2.2			2.2		V
V_{OH}	High-level output voltage		I_{OH} = −4 mA				3.7			V
			I_{OH} = −3.4 mA	3.7						
			I_{OH} = −20 μA, See Note 1	V_{CC}−0.1			V_{CC}−0.1			
V_{OL}	Low-level output voltage		I_{OL} = 4 mA						0.5	V
			I_{OL} = 3.4 mA			0.5				
			I_{OL} = 20 μA, See Note 1			0.1			0.1	
I_{CC}	Supply current	OPE40LH	V_{CC} = 4.5 V to 5.5 V,			1563			93.8	nA
		OPF40LH	V_I = V_{CC} or 0, T_A = Min to Max			1988			119	
C_i	Input capacitance		V_{CC} = 5 V, T_A = 25°C		0.7			0.7		pF
C_{pd}	Equivalent power dissipation capacitance	OPE40LH	V_{CC} = 5 V, t_r = t_f = 3 ns,		9.1			9.1		pF
		OPF40LH	T_A = 25°C		10.9			10.9		

NOTE 1: These limits apply when all other outputs are open.

TEXAS INSTRUMENTS
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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5100			SN74ASC5100			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	C_L = 15 pF,	1	1.9	4.1	1.1	1.9	3.7	ns
t_{PHL}			R_L = ∞	1.8	3.7	8.7	1.9	3.7	7.8	
t_{PLH}	A	Y	C_L = 50 pF,	1.5	2.9	6.6	1.7	2.9	5.9	ns
t_{PHL}			R_L = ∞	3.3	6.9	16.2	3.7	6.9	14.3	
Δt_{PLH}	A	Y		10	30	80	10	30	70	ps/pF
Δt_{PHL}				40	90	210	50	90	190	

CMOS loads

PARAMETER†	FROM INPUT	TO OUTPUT	TEST CONDITIONS	SN54ASC5100			SN74ASC5100			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	C_L = 15 pF,	1.2	2.4	5.3	1.3	2.4	4.8	ns
t_{PHL}			R_L = ∞	1.6	3	7.1	1.7	3	6.3	
t_{PLH}	A	Y	C_L = 50 pF,	2.2	4.4	9.9	2.4	4.4	9	ns
t_{PHL}			R_L = ∞	2.5	5.1	12.2	2.7	5.1	10.7	
Δt_{PLH}	A	Y		30	60	130	30	60	120	ps/pF
Δt_{PHL}				30	60	150	30	60	130	

† Propagation delay times are measured from the 44% point of V_I with $t_r = t_f$ = 3 ns (10% and 90%). For TTL loads, the times end at V_O = 1.3 V. For CMOS loads, the times end at the 50% point of V_O.
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to Section 7.

D2939, AUGUST 1986

SystemCell™ 2-μm OUTPUT STANDARD CELL

- Typical Propagation Delay
  2.4 ns with 15-pF Load
  3.5 ns with 50-pF Load
- Output Current Ratings
  SN54ASC5103 I_{OL} = 5.1 mA
  I_{OH} = −5.1 mA
  SN74ASC5103 I_{OL} = 6 mA
  I_{OH} = −6 mA
- Incorporates Circuitry to Protect Against ESD and Latch-Up
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol

FUNCTION TABLE

INPUT A	OUTPUT Y
H	H
L	L

positive logic equation

$Y = A$

description

The SN54ASC5103 and SN74ASC5103 are noninverting output buffer standard cells that interface CMOS internal cells with TTL or CMOS external loads. This cell function exists in two versions (''E'' and ''F'') with different physical implementations to allow the final IC area to be optimized. Since the electrical performance of each version is identical, for simplicity only one version (the ''F'' cell) will be contained in the engineering workstation cell libraries. Determination of the most appropriate cell version will be made during the layout stage. The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		CELL LAYOUT ASPECT RATIO	RELATIVE CELL AREA TO NA210LH
OPE60LH OPF60LH	Label: OPF60LH A,Y;	minimum height minimum width	43 40.5

The cells incorporate circuit elements designed to actively bypass and dissipate electrostatic discharges with potentials ranging up to 4 kilovolts. Guard-ring structures are employed that provide current management techniques for the cell to recover from exposure to high currents of up to 400 milliamperes, thereby negating most common sources that can produce a latch-up condition.

These output cells have been designed to provide low-impedance drive levels for both the high- and low-logic-level states. As a result, passive resistance has been omitted in series with the output transistors. Shorting a high-level output to ground or a low-level output to V_{CC} will cause current flow in excess of that recommended for normal operation. Therefore, it is recommended that outputs not be shorted directly to ground or V_{CC}.

description (continued)

The dynamic drive capability of each output is specified by the delta propagation delay time parameter included with the switching characteristics. The delta propagation delay times provide a means for making direct comparisons of the various output responses with change in capacitive loading.

The SN54ASC5103 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC5103 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 3 in Section 2, and the I_O test conditions shown in the electrical characteristics. The maximum low-level or high-level output current is 5.1 milliamperes for the SN54ASC5103 and 6 milliamperes for the SN74ASC5103.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		SN54ASC5103			SN74ASC5103			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C		2.2			2.2		V
V_{OH}	High-level output voltage		I_{OH} = −6 mA					3.7			V
			I_{OH} = −5.1 mA		3.7						
			I_{OH} = −20 μA,	See Note 1	V_{CC}−0.1			V_{CC}−0.1			
V_{OL}	Low-level output voltage		I_{OL} = 6 mA							0.5	V
			I_{OL} = 5.1 mA				0.5				
			I_{OL} = 20 μA,	See Note 1			0.1			0.1	
I_{CC}	Supply current	OPE60LH	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0,				2629			158	nA
		OPF60LH	T_A = MIN to MAX				2404			144	
C_i	Input capacitance		V_{CC} = 5 V,	T_A = 25°C		1			1		pF
C_{pd}	Equivalent power dissipation capacitance	OPE60LH	V_{CC} = 5 V,	t_r = t_f = 3 ns,		15.5			15.5		pF
		OPF60LH	T_A = 25°C			17.3			17.3		

NOTE 1: These limits apply when all other outputs are open.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5103			SN74ASC5103			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	C_L = 15 pF,	0.9	1.6	3.5	1	1.6	3.2	ns
t_{PHL}			R_L = ∞	1.6	3.2	7.3	1.7	3.2	6.5	
t_{PLH}	A	Y	C_L = 50 pF,	1.2	2.3	4.9	1.3	2.3	4.4	ns
t_{PHL}			R_L = ∞	2.5	5	11.9	2.7	5	10.5	
Δt_{PLH}	A	Y		10	20	40	10	20	30	ps/pF
Δt_{PHL}				20	51	140	30	51	120	

CMOS loads

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5103			SN74ASC5103			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	C_L = 15 pF,	1	2	4.4	1.1	2	4	ns
t_{PHL}			R_L = ∞	1.5	2.7	6.1	1.6	2.7	5.5	
t_{PLH}	A	Y	C_L = 50 pF,	1.6	3	6.7	1.7	3	6	ns
t_{PHL}			R_L = ∞	2.1	4	9.2	2.2	4	8.2	
Δt_{PLH}	A	Y		10	29	60	20	29	60	ps/pF
Δt_{PHL}				20	37	90	20	37	80	

† Propagation delay times are measured from the 44% point of V_I with $t_r = t_f$ = 3 ns (10% and 90%). For TTL loads, the times end at V_O = 1.3 V. For CMOS loads, the times end at the 50% point of V_O.
t_{PLH} ≡ propagation delay time, low-to-high level output
t_{PHL} ≡ propagation delay time, high-to-low level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to Section 7.

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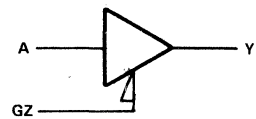
SystemCell™ 2-μm OUTPUT STANDARD CELL

- Typical Propagation Delays
  2.7 ns with 15-pF Load
  4 ns with 50-pF Load
- Output Current Ratings
  SN54ASC5104 I_{OL} = 5.1 mA
  I_{OH} = −5.1 mA
  SN74ASC5104 I_{OL} = 6 mA
  I_{OH} = −6 mA
- Incorporates Circuitry to Protect Against ESD and Latch-Up
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol



FUNCTION TABLE

INPUTS		OUTPUT
GZ	A	Y
L	H	H
L	L	L
H	X	Z

positive logic equation

Y = A (when GZ is L)

description

The SN54ASC5104 and SN74ASC5104 are noninverting 3-state output buffer standard-cells that interface internal cells with TTL or CMOS external buses. This cell function exists in two versions (''E'' and ''F'') with different physical implementations to allow the final IC area to be optimized. Since the electrical performance of each version is identical, for simplicity only one version (the ''F'' cell) will be contained in the engineering workstation cell libraries. Determination of the most appropriate cell version will be made during the layout stage. The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		CELL LAYOUT ASPECT RATIO	RELATIVE CELL AREA TO NA210LH
OPE63LH OPF63LH	Label: OPF63LH A,GZ,Y;	minimum height minimum width	51 49.2

The cells incorporate circuit elements designed to actively bypass and dissipate electrostatic discharges with potentials ranging up to 4 kilovolts. Guard-ring structures are employed that provide current management techniques for the cell to recover from exposure to high currents of up to 400 milliamperes, thereby negating most common sources that can produce a latch-up condition.

These output cells have been designed to provide low-impedance drive levels for both the high- and low-logic-level states; therefore, passive resistance has been omitted in series with the output transistors. Shorting a high-level output to ground or a low-level output to V_{CC} will cause current flow in excess of that recommended for normal operation. Therefore, it is recommended that outputs not be shorted directly to ground or V_{CC}.

description (continued)

The dynamic drive capability of each output is specified by the delta propagation delay time parameter that is included with the switching characteristics. The delta propagation delay times provide a means for making direct comparisons of the various output responses with change in capacitive loading.

The SN54ASC5104 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC5104 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 3 in Section 2 and the I_O test conditions shown in the electrical characteristics. The maximum low-level or high-level output current is 5.1 milliamperes for the SN54ASC5104 and 6 milliamperes for the SN74ASC5104.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	SN54ASC5104			SN74ASC5104			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_T	Input threshold voltage		V_{CC} = 5 V, T_A = 25°C		2.2		2.2			V
V_{OH}	High-level output voltage		I_{OH} = −6 mA				3.7			V
			I_{OH} = −5.1 mA	3.7						
			I_{OH} = −20 μA, See Note 1	V_{CC}−0.1			V_{CC}−0.1			
V_{OL}	Low-level output voltage		I_{OL} = 6 mA						0.5	V
			I_{OL} = 5.1 mA			0.5				
			I_{OL} = 20 μA, See Note 1			0.1			0.1	
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	μA
I_{CC}	Supply current	OPE63LH	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX			3145			189	nA
		OPF63LH				3039			182	
C_i	Input capacitance	A	V_{CC} = 5 V, T_A = 25°C		1			1		pF
		GZ			0.7			0.7		
C_{pd}	Equivalent power dissipation capacitance	OPE63LH	V_{CC} = 5 V, t_r = t_f = 3 ns, T_A = 25°C		17.1			17.1		pF
		OPF63LH			19.4			19.4		

NOTE 1: These limits apply when all other outputs are open.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, C_L = 15 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5104			SN74ASC5104			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	R_L = ∞	1	2	4.5	1.1	2	4	ns
t_{PHL}				1.6	3.3	7.8	1.7	3.3	6.9	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	1.2	2.8	6.6	1.3	2.8	6	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.5	3	7.1	1.6	3	6.4	

TTL loads, C_L = 50 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5104			SN74ASC5104			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	R_L = ∞	1.4	2.7	6.3	1.5	2.7	5.6	ns
t_{PHL}				2.4	5.2	12.7	2.6	5.2	11.1	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	1.5	3.5	8.4	1.7	3.5	7.6	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.4	5.2	12.6	2.6	5.2	11	
t_{PHZ}	GZ	Y	R_L = 1 kΩ to GND		10			10		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		9			9		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5104			SN74ASC5104			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
Δt_{PLH}	A	Y		10	23	50	10	23	50	ps/pF
Δt_{PHL}				20	54	140	30	54	120	
Δt_{PZH}	GZ	Y		10	20	50	10	20	50	ps/pF
Δt_{PZL}				30	63	160	30	63	130	

† Propagation delay times are measured from the 44% point of V_I with $t_r = t_f$ = 3 ns (10% and 90%). For TTL loads, the times end at V_O = 1.3 V.

t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
t_{PHZ} ≡ output disable time from high level
t_{PLZ} ≡ output disable time from low level

Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
Δt_{PZH} ≡ change in t_{PZH} with load capacitance
Δt_{PZL} ≡ change in t_{PZL} with load capacitance

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

CMOS loads, C_L = 15 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5104			SN74ASC5104			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	$R_L = \infty$	1.2	2.4	5.6	1.3	2.4	5	ns
t_{PHL}				1.5	2.8	6.6	1.6	2.8	5.8	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	1.7	3.2	7.3	1.8	3.2	6.6	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.3	2.5	5.7	1.4	2.5	5.2	

CMOS loads, C_L = 50 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5104			SN74ASC5104			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	$R_L = \infty$	1.7	3.6	8.4	1.9	3.6	7.5	ns
t_{PHL}				2	4	9.9	2.2	4	8.7	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	2.2	4.4	10.3	2.4	4.4	9.2	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2	4	9.5	2.2	4	8.4	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

CMOS loads

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5104			SN74ASC5104			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
Δt_{PLH}	A	Y		20	34	80	20	34	70	ps/pF
Δt_{PHL}				20	34	100	20	34	80	
Δt_{PZH}	GZ	Y		20	34	80	20	34	70	ps/pF
Δt_{PZL}				20	43	110	20	43	90	

† Propagation delay times are measured from the 44% point of V_I with $t_r = t_f$ = 3 ns (10% and 90%). CMOS times are specified at the 50% point of V_O.

t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
Δt_{PZH} ≡ change in t_{PZH} with load capacitance
Δt_{PZL} ≡ change in t_{PZL} with load capacitance

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to Section 7.

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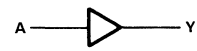
SystemCell™ 2-μm OUTPUT STANDARD CELL

- Typical Propagation Delays
  2 ns with 15-pF Load
  4 ns with 50-pF Load
- Output Current Ratings
  SN54ASC5105 I_{OL} = 5.1 mA
  SN74ASC5105 I_{OL} = 6 mA
- Incorporates Circuitry to Protect Against ESD and Latch-Up
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol



FUNCTION TABLE

INPUT A	OUTPUT Y
H	H
L	L

positive logic equation

$Y = A$

description

The SN54ASC5105 and SN74ASC5105 are noninverting output buffer standard cells that interface CMOS internal cells with a passive pull-up external load. This cell function exists in two versions (''E'' and ''F'') with different physical implementations to allow the final IC area to be optimized. Since the electrical performance of each version is identical, for simplicity only one version (the ''F'' cell) will be contained in the engineering workstation cell libraries. Determination of the most appropriate cell version will be made during the layout stage. The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		CELL LAYOUT ASPECT RATIO	RELATIVE CELL AREA TO NA210LH
OPE61LH OPF61LH	Label: OPF61LH A,Y;	minimum height minimum width	31 40

The cells incorporate circuit elements designed to actively bypass and dissipate electrostatic discharges with potentials ranging up to 4 kilovolts. Guard-ring structures are employed that provide current management techniques for the cell to recover from exposure to high currents of up to 400 milliamperes, thereby negating most common sources that can produce a latch-up condition.

These output cells have been designed to provide low-impedance drive levels for low-logic-level outputs interfacing a bus having a terminated high-level drive source. As a result, passive resistance has been omitted in series with the output transistor. Shorting the low-level output to V_{CC} will cause current flow in excess of that recommended for normal operation. Therefore, it is recommended that outputs not be shorted directly to V_{CC}.

The dynamic drive capability of each output is specified by the delta propagation delay time parameter included with the switching characteristics. The delta delay times provide a means for making direct comparisons of the various output responses to increased capacitive loading.

description (continued)

The SN54ASC5105 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC5105 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 3 in Section 2. Maximum low-level output current is 5.1 milliamperes for the SN54ASC5105 and 6 milliamperes for the SN74ASC5105.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ASC5105			SN74ASC5105			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_T Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C		2.2			2.2		V
V_{OL} Low-level output voltage		I_{OL} = 6 mA							0.5	V
		I_{OL} = 5.1 mA				0.5				
		I_{OL} = 20 μA,	See Note 1			0.1			0.1	
I_{OZ} Off-state output current		V_O = V_{CC} or 0				±10			±5	μA
I_{CC} Supply current	OPE61LH	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0,				1192			71.5	nA
	OPF61LH	T_A = MIN to MAX				1063			63.8	
C_i Input capacitance		V_{CC} = 5 V,	T_A = 25°C		1			1		pF
C_{pd} Equivalent power dissipation capacitance	OPE61LH	V_{CC} = 5 V,	t_r = t_f = 3 ns,		3.8			3.8		pF
	OPF61LH	T_A = 25°C			4			4		

NOTE 1: These limits apply when all other outputs are open.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5105			SN74ASC5105			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PZL}	A	Y	C_L = 15 pF, R_L = 1 kΩ to V_{CC}	1	2	4.7	1.1	2	4.2	ns
t_{PZL}	A	Y	C_L = 50 pF, R_L = 1 kΩ to V_{CC}	1.9	4	9.8	2.1	4	8.6	ns
t_{PLZ}	A	Y	R_L = 1 kΩ to V_{CC}		8			8		ns
Δt_{PZL}	A	Y		30	60	150	30	60	130	ps/pF

CMOS loads

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5105			SN74ASC5105			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PZL}	A	Y	C_L = 15 pF, R_L = 1 kΩ to V_{CC}	0.9	1.6	3.5	1	1.6	3.2	ns
t_{PZL}	A	Y	C_L = 50 pF, R_L = 1 kΩ to V_{CC}	1.5	2.9	7	1.6	2.9	6.1	ns
Δt_{PZL}	A	Y		20	37	100	20	37	80	ps/pF

† Propagation delay times are measured from the 44% point of V_I with t_r = t_f = 3 ns (10% and 90%). For TTL loads, the times end at V_O = 1.3 V. For CMOS loads, the times end at the 50% point of V_O.
t_{PZL} ≡ output enable time to low level
t_{PLZ} ≡ output disable time from low level
Δt_{PZL} ≡ change in t_{PZL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

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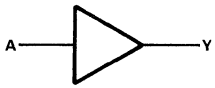
SystemCell™ 2-μm OUTPUT STANDARD CELL

- Typical Propagation Delays
  2 ns with 15-pF Load
  2.8 ns with 50-pF Load
- Output Current Ratings
  SN54ASC5106 I_{OL} = 8.5 mA
  I_{OH} = −8.5 mA
  SN74ASC5106 I_{OL} = 10 mA
  I_{OH} = −10 mA
- Incorporates Circuitry to Protect Against ESD and Latch-Up
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol



FUNCTION TABLE

INPUT A	OUTPUT Y
H	H
L	L

positive logic equation

$Y = A$

description

The SN54ASC5106 and SN74ASC5106 are noninverting output buffer standard-cells that interface CMOS internal cells with TTL or CMOS external loads. This cell function exists in two versions (''E'' and ''F'') with different physical implementations to allow the final IC area to be optimized. Since the electrical performance of each version is identical, for simplicity only one version (the ''F'' cell) will be contained in the engineering workstation cell libraries. Determination of the most appropriate cell version will be made during the layout stage. The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		CELL LAYOUT ASPECT RATIO	RELATIVE CELL AREA TO NA210LH
OPE00LH OPF00LH	Label: OPF00LH A,Y;	minimum height minimum width	47.7 42

The cells incorporates circuit elements designed to actively bypass and dissipate electrostatic discharges with potentials ranging up to 4 kilovolts. Guard-ring structures are employed that provide current management techniques for the cell to recover from exposure to high currents of up to 400 milliamperes, thereby negating most common sources that can produce a latch-up condition.

These output cells have been designed to provide low-impedance drive levels for both the high- and low-logic-level states. As a result, passive resistance has been omitted in series with the output transistors. Shorting a high-level output to ground or a low-level output to V_{CC} will cause current flow in excess of that recommended for normal operation. Therefore, it is recommended that outputs not be shorted directly to ground or V_{CC}.

The dynamic drive capability of each output is specified by the delta propagation delay time parameter included with the switching characteristics. The delta propagation delay times provide a means for making direct comparisons of the various output responses with change in capacitive loading.

The SN54ASC5106 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC5106 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 3 in Section 2 and the I_O test conditions shown in the electrical characteristics. The maximum low-level or high-level output current is 8.5 milliamperes for the SN54ASC5106 and 10 milliamperes for the SN74ASC5106.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54ASC5106			SN74ASC5106			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_T Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2			2.2			V
V_{OH} High-level output voltage		I_{OH} = −10 mA				3.7			V
		I_{OH} = −8.5 mA	3.7						
		I_{OH} = −20 μA, See Note 1	V_{CC}−0.1			V_{CC}−0.1			
V_{OL} Low-level output voltage		I_{OL} = 10 mA						0.5	V
		I_{OL} = 8.5 mA			0.5				
		I_{OL} = 20 μA, See Note 1			0.1			0.1	
I_{CC} Supply current	OPE00LH	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0,			2933			176	nA
	OPF00LH	T_A = MIN to MAX			2590			155	
C_i Input capacitance		V_{CC} = 5 V, T_A = 25°C		1.4			1.4		pF
C_{pd} Equivalent power dissipation capacitance	OPE00LH	V_{CC} = 5 V, t_r = t_f = 3 ns,		21.8			21.8		pF
	OPF00LH	T_A = 25°C		20.1			20.1		

NOTE 1: These limits apply when all other outputs are open.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5106			SN74ASC5106			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	C_L = 15 pF,	0.8	1.5	3.2	0.9	1.5	2.9	ns
t_{PHL}			R_L = ∞	1.2	2.6	5.7	1.3	2.6	5.1	
t_{PLH}	A	Y	C_L = 50 pF	1.1	2	4.4	1.2	2	4	ns
t_{PHL}			R_L = ∞	1.8	3.7	8.5	1.9	3.7	7.6	
Δt_{PLH}	A	Y		10	14	40	10	14	30	ps/pF
Δt_{PHL}				20	31	80	20	31	70	

CMOS loads

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5106			SN74ASC5106			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	C_L = 15 pF,	0.9	1.9	4	1	1.9	3.6	ns
t_{PHL}			R_L = ∞	1.2	2.2	4.8	1.3	2.2	4.4	
t_{PLH}	A	Y	C_L = 50 pF,	1.4	2.7	6.2	1.5	2.7	5.6	ns
t_{PHL}			R_L = ∞	1.6	3	6.8	1.7	3	6.1	
Δt_{PLH}	A	Y		10	23	60	10	23	60	ps/pF
Δt_{PHL}				10	23	60	10	23	50	

† Propagation delay times are measured from the 44% point of V_I with $t_r = t_f$ = 3 ns (10% and 90%). For TTL loads, the times end at V_O = 1.3 V. For CMOS loads, the times end at 50% point of V_O.
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to Section 7.

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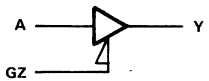
SystemCell™ 2-μm OUTPUT STANDARD CELL

- Typical Propagation Delays
  2.7 ns with 15-pF Load
  3.7 ns with 50-pF Load
- Output Current Ratings
  SN54ASC5107 I_{OL} = 8.5 mA
  I_{OH} = −8.5 mA
  SN74ASC5107 I_{OL} = 10 mA
  I_{OH} = −10 mA
- Incorporates Circuitry to Protect Against ESD and Latch-Up
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol



FUNCTION TABLE

INPUTS		OUTPUT
GZ	A	Y
L	H	H
L	L	L
H	X	Z

positive logic equation

Y = A (when GZ is L)

description

The SN54ASC5107 and SN74ASC5107 are noninverting 3-state output buffer standard cells that interface CMOS internal cells with TTL or CMOS external buses. This cell function exists in two versions (''E'' and ''F'') with different physical implementations to allow the final IC area to be optimized. Since the electrical performance of each version is identical, for simplicity only one version (the ''F'' cell) will be contained in the engineering workstation cell libraries. Determination of the most appropriate cell version will be made during the layout stage. The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		CELL LAYOUT ASPECT RATIO	RELATIVE CELL AREA TO NA210LH
OPE03LH OPF03LH	Label: OPF03LH A,GZ,Y;	minimum height minimum width	54 52.4

The cells incorporate circuit elements designed to actively bypass and dissipate electrostatic discharges with potentials ranging up to 4 kilovolts. Guard-ring structures are employed that provide current management techniques for the cell to recover from exposure to high currents of up to 400 milliamperes, thereby negating most common sources that can produce a latch-up condition.

These output cells have been designed to provide low-impedance drive levels for both the high- and low-logic-level states. As a result, passive resistance has been omitted in series with the output transistors. Shorting a high-level output to ground or a low-level output to V_{CC} will cause current flow in excess of that recommended for normal operation. Therefore, it is recommended that outputs not be shorted directly to ground or V_{CC}.

description (continued)

The dynamic drive capability of each output is specified by the delta propagation delay time parameter included with the switching characteristics. The delta propagation delay times provide a means for making direct comparisons of the various output responses with change in capacitive loading.

The SN54ASC5107 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC5107 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 3 in Section 2. The maximum low-level or high-level output current is 8.5 milliamperes for the SN54ASC5107 and 10 milliamperes for the SN74ASC5107.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		SN54ASC5107			SN74ASC5107			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C		2.2			2.2		V
V_{OH}	High-level output voltage		I_{OH} = −10 mA					3.7			V
			I_{OH} = −8.5 mA		3.7						
			I_{OH} = −20 μA,	See Note 1	V_{CC}−0.1			V_{CC}−0.1			
V_{OL}	Low-level output voltage		I_{OL} = 10 mA							0.5	V
			I_{OL} = 8.5 mA				0.5				
			I_{OL} = 20 μA,	See Note 1			0.1			0.1	
I_{OZ}	Off-state output current		V_O = V_{CC} or 0				±10			±5	μA
I_{CC}	Supply current	OPE03LH	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0,				3483			209	nA
		OPF03LH	T_A = MIN to MAX				3318			199	
C_i	Input capacitance	A	V_{CC} = 5 V,	T_A = 25°C		1.1			1.1		pF
		GZ				0.7			0.7		
C_{pd}	Equivalent power dissipation capacitance	OPE03LH	V_{CC} = 5 V,	t_r = t_f = 3 ns,		19.9			19.9		pF
		OPF03LH	T_A = 25°C			23.2			23.2		

NOTE 1: These limits apply when all other outputs are open.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, C_L = 15 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5107			SN74ASC5107			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	R_L = ∞	1.1	2.1	4.8	1.2	2.1	4.3	ns
t_{PHL}				1.5	3.3	8.2	1.6	3.3	7.3	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	1.2	2.8	6.8	1.3	2.8	6.2	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.4	3.1	7.3	1.5	3.1	6.5	

† Propagation delay times are measured from the 44% point of V_I with t_r = t_f = 3 ns (10% and 90%). For TTL loads, the times end at V_O = 1.3 V.
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PLZ} ≡ output disable time from low level
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

TTL loads, C_L = 50 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5107			SN74ASC5107			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	R_L = ∞	1.4	2.7	6.5	1.5	2.7	5.7	ns
t_{PHL}				2.2	4.7	11.6	2.4	4.7	10.3	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	1.5	3.5	8.5	1.7	3.5	7.6	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.2	4.7	11.2	2.4	4.7	10	
t_{PHZ}	GZ	Y	R_L = 1 kΩ to GND		10			10		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		8			8		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5107			SN74ASC5107			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
Δt_{PLH}	A	Y		10	17	50	10	17	40	ps/pF
Δt_{PHL}				20	40	100	20	40	90	
Δt_{PZH}	GZ	Y		10	20	50	10	20	40	ps/pF
Δt_{PZL}				20	46	110	20	46	100	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

CMOS loads, C_L = 15 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5107			SN74ASC5107			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	R_L = ∞	1.2	2.5	5.9	1.3	2.5	5.3	ns
t_{PHL}				1.5	2.9	7.1	1.5	2.9	6.3	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	1.7	3.3	7.6	1.8	3.3	6.8	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.3	2.6	6.1	1.4	2.6	5.5	

CMOS loads, C_L = 50 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5107			SN74ASC5107			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	R_L = ∞	1.7	3.5	8.3	1.9	3.5	7.4	ns
t_{PHL}				1.9	3.9	9.6	2	3.9	8.5	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	2.2	4.3	10.1	2.3	4.3	9.1	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.9	3.8	9	2	3.8	8	

†Propagation delay times are measured from the 44% point of V_I with $t_r = t_f$ = 3 ns (10% and 90%). For TTL loads, the times end at V_O = 1.3 V. For CMOS loads, the times end at the 50% point of V_O.

t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
t_{PHZ} ≡ output disable time from high level
t_{PLZ} ≡ output disable time from low level

Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
Δt_{PZH} ≡ change in t_{PZH} with load capacitance
Δt_{PZL} ≡ change in t_{PZL} with load capacitance

‡Typical values are at V_{CC} = 5 V, T_A = 25°C.

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

CMOS loads

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5107			SN74ASC5107			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
Δt_{PLH}	A	Y		10	29	70	10	29	70	ps/pF
Δt_{PHL}				10	29	70	10	29	60	
Δt_{PZH}	GZ	Y		10	29	70	10	29	70	ps/pF
Δt_{PZL}				20	34	80	20	34	70	

† Propagation delay times are measured from the 44% point of V_I with $t_r = t_f = 3$ ns (10% and 90%). For CMOS loads, the times end at the 50% point of V_O.
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
Δt_{PZH} ≡ change in t_{PZH} with load capacitance
Δt_{PZL} ≡ change in t_{PZL} with load capacitance
‡ Typical values are at $V_{CC} = 25°C$, $T_A = 25°C$.

DESIGN CONSIDERATIONS

Refer to Section 7.

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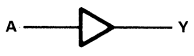
SystemCell™ 2-μm OUTPUT STANDARD CELL

- Typical Propagation Delays
  1.7 ns with 15-pF Load
  3 ns with 50-pF Load
- Output Current Ratings
  SN54ASC5108 I_{OL} = 8.5 mA
  SN74ASC5108 I_{OL} = 10 mA
- Incorporates Circuitry to Protect Against ESD and Latch-Up
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol



FUNCTION TABLE

INPUT A	OUTPUT Y
H	H
L	L

positive logic equation

$Y = A$

description

The SN54ASC5108 and SN74ASC5108 are noninverting output buffer standard-cells that interface CMOS internal cells with a passive pull-up external load. This cell function exists in two versions (''E'' and ''F'') with different physical implementations to allow the final IC area to be optimized. Since the electrical performance of each version is identical, for simplicity only one version (the ''F'' cell) will be contained in the engineering workstation cell libraries. Determination of the most appropriate cell version will be made during the layout stage. The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		CELL LAYOUT ASPECT RATIO	RELATIVE CELL AREA TO NA210LH
OPE01LH OPF01LH	Label: OPF01LH A,Y;	minimum height minimum width	31.8 42

The cells incorporate circuit elements designed to actively bypass and dissipate electrostatic discharges with potentials ranging up to 4 kilovolts. Guard ring structures are employed that provide current management techniques for the cell to recover from exposure to high currents of up to 400 milliamperes, thereby negating most common sources that can produce a latch-up condition.

These output cells have been designed to provide low-impedance drive levels for low-logic-level outputs interfacing a bus having a terminated high-level drive source. As a result, passive resistance has been omitted in series with the output transistor. Shorting the low-level output to V_{CC} will cause current flow in excess of that recommended for normal operation. Therefore, it is recommended that outputs not be shorted directly to V_{CC}.

The dynamic drive capability of each output is specified by the delta propagation delay time parameter included with the switching characteristics. The delta propagation delay times provide a means for making direct comparisons of the various output responses with change in capacitive loading.

The SN54ASC5108 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC5108 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 3 in Section 2 and the I_O test conditions shown in the electrical characteristics. Maximum low-level output current is 8.5 milliamperes for the SN54ASC5108 and 10 milliamperes for the SN74ASC5108.

electrical characteristics over recommended ranges of suply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		SN54ASC5108			SN74ASC5108			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C		2.2			2.2		V
V_{OL}	Low-level output voltage		I_{OL} = 10 mA							0.5	V
			I_{OL} = 8.5 mA				0.5				
			I_{OL} = 20 μA,	See Note 1			0.1			0.1	
I_{OZ}	Off-state output current		V_O = V_{CC} or 0				±10			±5	μA
I_{CC}	Supply current	OPE01LH	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0,				1302			78.1	nA
		OPF01LH	T_A = MIN to MAX				1193			71.6	
C_i	Input capacitance		V_{CC} = 5 V,	T_A = 25°C		1.4			1.4		pF
C_{pd}	Equivalent power dissipation capacitance	OPE01LH	V_{CC} = 5 V,	t_r = t_f = 3 ns,		5.6			5.6		pF
		OPF01LH	T_A = 25°C			5.8			5.8		

NOTE 1: These limits apply when all other outputs are open.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5108			SN74ASC5108			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PZL}	A	Y	C_L = 15 pF, R_L = 1 kΩ to V_{CC}	0.9	1.7	3.7	0.9	1.7	3.3	ns
t_{PZL}	A	Y	C_L = 50 pF, R_L = 1 kΩ to V_{CC}	1.4	3	6.8	1.5	3	6	ns
t_{PLZ}	A	Y	R_L = 1 kΩ to V_{CC}		7.2			7.2		ns
Δt_{PZL}	A	Y		10	37	90	20	37	80	ps/pF

CMOS loads

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5108			SN74ASC5108			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PZL}	A	Y	C_L = 15 pF, R_L = 1 kΩ to V_{CC}	0.8	1.4	2.9	0.8	1.4	2.6	ns
t_{PZL}	A	Y	C_L = 50 pF, R_L = 1 kΩ to V_{CC}	1.2	2.2	5	1.3	2.2	4.5	ns
Δt_{PZL}	A	Y		10	23	60	10	23	50	ps/pF

† Propagation delay times are measured from the 44% point of V_I with t_r = t_f = 3 ns (10% and 90%). For TTL loads, the times end at V_O = 1.3 V. For CMOS loads, the times end at the 50% point of V_O.
t_{PZL} ≡ output enable time to low level
t_{PLZ} ≡ output disable time from low level
Δt_{PZL} ≡ change in t_{PZL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

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SystemCell™ 2-μm OUTPUT STANDARD CELL

- Typical Propagation Delay
  2.7 ns with 15-pF Load
  6 ns with 50-pF Load
- Output Current Ratings
  SN54ASC5109 I_{OL} = 3.4 mA
  SN74ASC5109 I_{OL} = 4 mA
- Incorporates Circuitry to Protect Against ESD and Latch-Up
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol

FUNCTION TABLE

INPUT A	OUTPUT Y
H	H
L	L

positive logic equation

$Y = A$

description

The SN54ASC5109 and SN74ASC5109 are noninverting output buffer standard cells that interface CMOS internal cells with a passive pull-up external load. This cell function exists in two versions (''E'' and ''F'') with different physical implementations to allow the final IC area to be optimized. Since the electrical performance of each version is identical, for simplicity only one version (the ''F'' cell) will be contained in the engineering workstation cell libraries. Determination of the most appropriate cell version will be made during the layout stage. The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		CELL LAYOUT ASPECT RATIO	RELATIVE CELL AREA TO NA210LH
OPE41LH OPF41LH	Label: OPF41LH A,Y;	minimum height minimum width	27.8 39

The cells incorporate circuit elements designed to actively bypass and dissipate electrostatic discharges with potentials ranging up to 4 kilovolts. Guard-ring structures are employed that provide current management techniques for the cell to recover from exposure to high currents of up to 400 milliamperes, thereby negating most common sources that can produce a latch-up condition.

These output cells have been designed to provide low-impedance drive levels for low-logic-level outputs interfacing a bus having a terminated high-level drive source. As a result, passive resistance has been omitted in series with the output transistor. Shorting the low-level output to V_{CC} will cause current flow in excess of that recommended for normal operation. Therefore, it is recommended that outputs not be shorted directly to V_{CC}.

The dynamic drive capability of each output is specified by the delta propagation delay time parameter included with the switching characteristics. The delta propagation delay times provide a means for making direct comparisons of the various output responses with change in capacitive loading.

description (continued)

The SN54ASC5109 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC5109 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 3 in Section 2. Maximum low-level output current is 3.4 milliamperes for the SN54ASC5109 and 4 milliamperes for the SN74ASC5109.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		SN54ASC5109			SN74ASC5109			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C		2.2			2.2		V
V_{OL}	Low-level output voltage		I_{OL} = 4 mA							0.5	V
			I_{OL} = 3.4 mA				0.5				
			I_{OL} = 20 μA,	See Note 1			0.1			0.1	
I_{OZ}	Off-state output current		V_O = V_{CC} or 0				±10			±5	μA
I_{CC}	Supply current	OPE41LH	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0,				1052			63.1	nA
		OPF41LH	T_A = MIN to MAX				1037			62.2	
C_i	Input capacitance		V_{CC} = 5 V,	T_A = 25°C		0.7			0.7		pF
C_{pd}	Equivalent power dissipation capacitance	OPE41LH	V_{CC} = 5 V,	t_r = t_f = 3 ns,		2.4			2.4		pF
		OPF41LH	T_A = 25°C			2.6			2.6		

NOTE 1: These limits apply when all other outputs are open.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5109			SN74ASC5109			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PZL}	A	Y	C_L = 15 pF, R_L = 1 kΩ to V_{CC}	1.3	2.7	6.5	1.4	2.7	5.7	ns
t_{PZL}	A	Y	C_L = 50 pF, R_L = 1 kΩ to V_{CC}	2.8	6	14.5	3.1	6	12.5	ns
t_{PLZ}					9.6			9.6		
Δt_{PZL}	A	Y		40	90	230	50	90	200	ps/pF

CMOS loads

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5109			SN74ASC5109			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PZL}	A	Y	C_L = 15 pF, R_L = 1 kΩ to V_{CC}	1.1	2	4.8	1.2	2	4.3	ns
t_{PZL}	A	Y	C_L = 50 pF, R_L = 1 kΩ to V_{CC}	2.1	4	10	2.2	4	8.7	ns
Δt_{PZL}	A	Y		30	57	150	30	57	130	ps/pF

† Propagation delay times are measured from the 44% point of V_I with t_r = t_f = 3 ns (10% and 90%). For TTL loads, the times end at V_O = 1.3 V. For CMOS loads, the times end at the 50% point of V_O.
t_{PZL} ≡ output enable time to low level
t_{PLZ} ≡ output disable time from low level
Δt_{PZL} ≡ change in t_{PZL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

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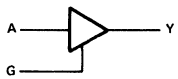
SystemCell™ 2-μm OUTPUT STANDARD CELL

- **Typical Propagation Delay**
  3.4 ns with 15-pF Load
  6.2 ns with 50-pF Load
- **Incorporates Circuitry to Protect Against ESD and Latch-Up**
- **Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V**
- **Functional Operation Over V_{CC} Range of 2 V to 6 V**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol



FUNCTION TABLE

INPUTS		OUTPUT
G	A	Y
H	H	H
H	L	L
L	X	Z

positive logic equation

Y = A (when G is H)
Y is at a high impedance when G is low.

description

The SN54ASC5110 and SN74ASC5110 are noninverting 3-state output buffer standard cells that interface internal cells with TTL or CMOS external loads. This cell function exists in two versions (''E'' and ''F'') with different physical implementations to allow the final IC area to be optimized. Since the electrical performance of each version is identical, for simplicity only one version (the ''F'' cell) will be contained in the engineering workstation cell libraries. Determination of the most appropriate cell version will be made during the layout stage. The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		CELL LAYOUT ASPECT RATIO	RELATIVE CELL AREA TO NA210LH
OPE42LH OPF42LH	Label: OPF42LH A,G,Y;	minimum height minimum width	38.1 45

The cell incorporates circuit elements designed to actively bypass and dissipate electrostatic discharges with potentials ranging up to 4 kilovolts. Guard-ring structures are employed that provide current management techniques for the cell to recover from exposure to high currents of up to 400 milliamperes, thereby negating most common sources that can produce a latch-up condition.

These output cells have been designed specifically to provide low-impedance drive levels for both the high- and low-logic-level states. Therefore, passive resistance has been omitted in series with the output transistors. Shorting of a high-level output to ground or a low-level output to V_{CC} will cause current flow in excess of that recommended for normal operation. Therefore, it is recommended that outputs not be shorted directly to ground or V_{CC}.

The dynamic drive capability of each output is specified by the delta propagation delay time parameter included with the switching characteristics. The delta delay times provide a means for making direct comparisons of the various output responses with change in capacitive loading.

The SN54ASC5110 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC5110 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 3 in Section 2 and the I_O test conditions shown in the electrical characteristics. The maximum high-level or low-level output current is 3.2 milliamperes for the SN54ASC5110 and 4 milliamperes for the SN74ASC5110.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	SN54ASC5110			SN74ASC5110			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_T	Input threshold voltage		V_{CC} = 5 V, T_A = 25°C		2.2			2.2		V
V_{OH}	High-level output voltage		I_{OH} = −4 mA				3.7			V
			I_{OH} = −3.2 mA	3.7						
			I_{OH} = −20 μA, See Note 1	V_{CC}−0.1			V_{CC}−0.1			
V_{OL}	Low-level output voltage		I_{OL} = 4 mA						0.4	V
			I_{OL} = 3.2 mA			0.4				
			I_{OL} = 20 μA, See Note 1			0.1			0.1	
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	μA
I_{CC}	Supply current	OPE42LH	V_I = V_{CC} or 0			1962			118	nA
		OPF42LH				2317			139	
C_i	Input capacitance	A	V_{CC} = 5 V, T_A = 25°C		0.6			0.6		pF
		G			0.5			0.5		
C_{pd}	Equivalent power dissipation capacitance	OPE42LH	V_{CC} = 5 V, t_r = t_f = 3 ns, T_A = 25°C		8.6			8.6		ns
		OPF42LH			10.5			10.5		

NOTE 1: These limits apply when all other outputs are open.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, C_L = 15 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5110			SN74ASC5110			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	$R_L = \infty$	1.3	2.3	4.4	1.4	2.3	4	ns
t_{PHL}				2.2	4.5	8.8	2.4	4.5	7.8	
t_{PZH}	G	Y	R_L = 1 kΩ to GND	1.3	2.4	4.5	1.4	2.4	4.1	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.7	5.2	10.4	2.9	5.2	9	

TTL loads, C_L = 50 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5110			SN74ASC5110			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	$R_L = \infty$	1.9	3.7	7.2	2	3.7	6.5	ns
t_{PHL}				4.3	8.8	17.2	4.7	8.8	15	
t_{PZH}	G	Y	R_L = 1 kΩ to GND	1.9	3.8	7.4	2	3.8	6.6	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.8	9.8	20	5.3	9.8	17.2	
t_{PHZ}	G	Y	R_L = 1 kΩ to GND		10			10		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		10			10		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5110			SN74ASC5110			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
Δt_{PLH}	A	Y		20	40	80	20	40	70	ps/pF
Δt_{PHL}				60	123	240	70	123	212	
Δt_{PZH}	G	Y		20	40	80	20	40	70	ps/pF
Δt_{PZL}				60	131	270	70	131	230	

† Propagation delay times are measured from the 44% point of V_I with $t_r = t_f$ = 3 ns (10% and 90%). For TTL loads, the times end at V_O = 1.3 V.

t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
t_{PHZ} ≡ output disable time from high level
t_{PLZ} ≡ output disable time from low level

Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
Δt_{PZH} ≡ change in t_{PZH} with load capacitance
Δt_{PZL} ≡ change in t_{PZL} with load capacitance

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

CMOS loads, C_L = 15 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5110			SN74ASC5110			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	$R_L = \infty$	1.5	3	5.8	1.6	3	5.2	ns
t_{PHL}				1.9	3.8	7.9	2	3.8	7	
t_{PZH}	G	Y	R_L = 1 kΩ to GND	1.6	3.2	6	1.7	3.2	5.4	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2	4.4	9.3	2.1	4.4	8.2	

CMOS loads, C_L = 50 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5110			SN74ASC5110			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	$R_L = \infty$	2.5	5.3	10.5	3	5.3	9.4	ns
t_{PHL}				3.2	6.5	13.4	3.5	6.5	11.7	
t_{PZH}	G	Y	R_L = 1 kΩ to GND	2.6	5.5	11	2.8	5.5	9.9	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.3	7.2	15.2	3.6	7.2	13.3	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5110			SN74ASC5110			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
Δt_{PLH}	A	Y		30	66	130	30	66	120	ps/pF
Δt_{PHL}				30	77	160	40	77	140	
Δt_{PZH}	G	Y		30	66	140	30	66	130	ps/pF
Δt_{PZL}				40	80	180	40	80	150	

† Propagation delay times are measured from the 44% point of V_I with $t_r = t_f = 3$ ns (10% and 90%). For CMOS loads, the times end at 50% point of V_O.

t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level

Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
Δt_{PZH} ≡ change in t_{PZH} with load capacitance
Δt_{PZL} ≡ change in t_{PZL} with load capacitance

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to Section 7.

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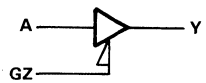
SystemCell™ 2-μm OUTPUT STANDARD CELL

- Typical Propagation Delay
  3.5 ns with 15-pF Load
  5.7 ns with 50-pF Load
- Output Current Ratings
  SN54ASC5111 I_{OL} = 3.4 mA
  I_{OH} = −3.4 mA
  SN74ASC5111 I_{OL} = 4 mA
  I_{OH} = −4 mA
- Incorporates Circuitry to Protect Against ESD and Latch-Up
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol



FUNCTION TABLE

INPUTS		OUTPUT
GZ	A	Y
L	H	H
L	L	L
H	X	Z

positive logic equation

Y = A (when GZ is L)

description

The SN54ASC5111 and SN74ASC5111 are noninverting 3-state output buffer standard cells that interface CMOS internal cells with TTL or CMOS external buses. This cell function exists in two versions (''E'' and ''F'') with different physical implementations to allow the final IC area to be optimized. Since the electrical performance of each version is identical, for simplicity only one version (the ''F'' cell) will be contained in the engineering workstation cell libraries. Determination of the most appropriate cell version will be made during layout stage. The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		CELL LAYOUT ASPECT RATIO	RELATIVE CELL AREA TO NA210LH
OPE43LH OPF43LH	Label: OPF43LH A, GZ, Y;	minimum height minimum width	38 45

The cells incorporate circuit elements designed to actively bypass and dissipate electrostatic discharges with potentials ranging up to 4 kilovolts. Guard-ring structures are employed that provide current management techniques for the cell to recover from exposure to high currents of up to 400 milliamperes, thereby negating most common sources that can produce a latch-up condition.

These output cells have been designed to provide low-impedance drive levels for both the high- and low-logic-level states; therefore, passive resistance has been omitted in series with the output transistors. Shorting a high-level output to ground or a low-level output to V_{CC} will cause current flow in excess of that recommended for normal operation. Therefore, it is recommended that outputs not be shorted directly to ground or V_{CC}.

description (continued)

The dynamic drive capability of each output is specified by the delta propagation delay time parameter included with the switching characteristics. The delta propagation delay times provide a means for making direct comparisons of the various output responses with change in capacitive loading.

The SN54ASC5111 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC5111 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 3 in Section 2 and the I_O test conditions shown in the electrical characteristics. The maximum low-level or high-level output current is 3.4 milliamperes for the SN54ASC5111 and 4 milliamperes for the SN74ASC5111.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ASC5111			SN74ASC5111			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_T Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C		2.2			2.2		V
V_{OH} High-level output voltage		I_{OH} = −4 mA					3.7			V
		I_{OH} = −3.4 mA		3.7						
		I_{OH} = −20 μA,	See Note 1	V_{CC}−0.1			V_{CC}−0.1			
V_{OL} Low-level output voltage		I_{OL} = 4 mA							0.5	V
		I_{OL} = 3.4 mA				0.5				
		I_{OL} = 20 μA,	See Note 1			0.1			0.1	
I_{OZ} Off-state output current		V_O = V_{CC} or 0				±10			±5	μA
I_{CC} Supply current	OPE43LH	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0,				1982			119	nA
	OPF43LH	T_A = MIN to MAX				2334			140	
C_i Input capacitance	A	V_{CC} = 5 V,	T_A = 25°C		0.6			0.6		pF
	GZ				0.4			0.4		
C_{pd} Equivalent power dissipation capacitance	OPE43LH	V_{CC} = 5 V,	t_r = t_f = 3 ns,		10.3			10.3		pF
	OPF43LH	T_A = 25°C			10.9			10.9		

NOTE 1: These limits apply when all other outputs are open.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, C_L = 15 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5111			SN74ASC5111			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	R_L = ∞	1.3	2.4	5.6	1.4	2.4	5	ns
t_{PHL}				2.1	4.5	11.3	2.2	4.5	10	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	1.5	3.3	8	1.6	3.3	7.2	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2	4.5	11.6	2.2	4.5	10.2	

TTL loads, C_L = 50 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5111			SN74ASC5111			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	R_L = ∞	1.8	3.5	8.5	1.9	3.5	7.6	ns
t_{PHL}				3.8	8	19.7	4.2	8	17.3	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	2	4.4	10.9	2.1	4.4	9.8	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.9	8.3	21	4.2	8.3	18.2	
t_{PHZ}	GZ	Y	R_L = 1 kΩ to GND		11			11		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		10			10		

change in propagation delay times with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5111			SN74ASC5111			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
Δt_{PLH}	A	Y		10	31	80	20	31	70	ps/pF
Δt_{PHL}				50	100	240	50	100	210	
Δt_{PZH}	GZ	Y		10	31	80	20	31	70	ps/pF
Δt_{PZL}				50	109	280	60	109	230	

† Propagation delay times are measured from the 44% point of V_I with $t_r = t_f$ = 3 ns (10% and 90%). For TTL loads, the times end at V_O = 1.3 V.

t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
t_{PHZ} ≡ output disable time from high level
t_{PLZ} ≡ output disable time from low level

Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
Δt_{PZH} ≡ change in t_{PZH} with load capacitance
Δt_{PZL} ≡ change in t_{PZL} with load capacitance

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

CMOS loads, C_L = 15 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5111			SN74ASC5111			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	R_L = ∞	1.5	3	7.1	1.6	3	6.3	ns
t_{PHL}				1.8	3.7	9.3	1.9	3.7	8.3	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	2	4	9.3	2.2	4	8.3	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.7	3.6	9.2	1.9	3.6	8.2	

CMOS loads, C_L = 50 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5111			SN74ASC5111			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	R_L = ∞	2.5	5	11.9	2.7	5	10.6	ns
t_{PHL}				2.9	6	15.3	3.1	6	13.4	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	3	6	14.2	3.2	6	12.7	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.9	6	15.6	3.1	6	13.7	

change in propagation delay times with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5111			SN74ASC5111			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
Δt_{PLH}	A	Y		30	57	130	30	57	120	ps/pF
Δt_{PHL}				30	66	170	30	66	150	
Δt_{PZH}	GZ	Y		30	57	130	30	57	130	ps/pF
Δt_{PZL}				30	69	180	40	69	160	

† Propagation delay times are measured from the 44% point of V_I with $t_r = t_f$ = 3 ns (10% and 90%). For CMOS loads, the times end at 50% point of V_O.

t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level

Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
Δt_{PZH} ≡ change in t_{PZH} with load capacitance
Δt_{PZL} ≡ change in t_{PZL} with load capacitance

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to Section 7.

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SN54ASC5120, SN74ASC5120 TTL-/CMOS-COMPATIBLE OUTPUT BUFFERS

D2939, AUGUST 1986

SystemCell™ 2-μm OUTPUT STANDARD CELL

- Typical Propagation Delay
  1.7 ns with 15-pF Load
  2.2 ns with 50-pF Load
- Output Current Ratings
  SN54ASC5120 I_{OL} = 20.4 mA
  I_{OH} = −10.2 mA
  SN74ASC5120 I_{OL} = 24 mA
  I_{OH} = −12 mA
- Incorporates Circuitry to Protect Against ESD and Latch-Up
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol

FUNCTION TABLE

INPUT A	OUTPUT Y
H	H
L	L

positive logic equation

$Y = A$

description

The SN54ASC5120 and SN74ASC5120 are noninverting output buffer standard cells that interface CMOS internal cells with TTL or CMOS external loads. The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		CELL LAYOUT ASPECT RATIO	RELATIVE CELL AREA TO NA210LH
OPFB0LH	Label: OPFB0LH A,Y;	minimum width	63

The cell incorporates circuit elements designed to actively bypass and dissipate electrostatic discharges with potentials ranging up to 4 kilovolts. Guard-ring structures are employed that provide current management techniques for the cell to recover from exposure to high currents of up to 400 milliamperes, thereby negating most common sources that can produce a latch-up condition.

These output cells have been designed to provide low-impedance drive levels for both the high- and low-logic-level states. As a result, passive resistance has been omitted in series with the output transistors. Shorting a high-level output to ground or a low-level output to V_{CC} will cause current flow in excess of that recommended for normal operation. Therefore, it is recommended that outputs not be shorted directly to ground or V_{CC}.

description (continued)

The dynamic drive capability of each output is specified by the delta propagation delay time parameter included with the switching characteristics. The delta propagation delay times provide a means for making direct comparisons of the various output responses with change in capacitive loading.

The SN54ASC5120 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC5120 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 3 in Section 2. The maximum high-level output current is −10.2 milliamperes for the SN54ASC5120 and −12 milliamperes for the SN74ASC5120. The maximum low-level output current is 20.4 milliamperes for the SN54ASC5120 and 24 milliamperes for the SN74ASC5120.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ASC5120			SN74ASC5120			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_T	Input threshold voltage	V_{CC} = 5 V,	T_A = 25°C		2.2			2.2		V
V_{OH}	High-level output voltage	I_{OH} = −12 mA					3.7			V
		I_{OH} = −10.2 mA		3.7						
		I_{OH} = −20 μA,	See Note 1	V_{CC}−0.1			V_{CC}−0.1			
V_{OL}	Low-level output voltage	I_{OL} = 24 mA							0.5	V
		I_{OL} = 20.4 mA				0.5				
		I_{OL} = 20 μA,	See Note 1			0.1			0.1	
I_{CC}	Supply current	V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX	V_I = V_{CC} or 0,			4207			252	nA
C_i	Input capacitance	V_{CC} = 5 V,	T_A = 25°C		2.7			2.7		pF
C_{pd}	Equivalent power dissipation capacitance	V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,		32.8			32.8		pF

NOTE 1: These limits apply when all other outputs are open.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5120			SN74ASC5120			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	C_L = 15 pF, R_L = ∞		1.3			1.3		ns
t_{PHL}					2			2		
t_{PLH}	A	Y	C_L = 50 pF, R_L = ∞		1.7			1.7		ns
t_{PHL}					2.6			2.6		
Δt_{PLH}	A	Y			11			11		ps/pF
Δt_{PHL}					17			17		

CMOS loads

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5120			SN74ASC5120			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	C_L = 15 pF, R_L = ∞		1.6			1.6		ns
t_{PHL}					1.8			1.8		
t_{PLH}	A	Y	C_L = 50 pF, R_L = ∞		2.1			2.1		ns
t_{PHL}					2.2			2.2		
Δt_{PLH}	A	Y			14			14		ps/pF
Δt_{PHL}					11			11		

† Propagation delay times are measured from the 44% point of V_I with $t_r = t_f$ = 3 ns (10% and 90%). For TTL loads, the times end at V_O = 1.3 V. For CMOS loads, the times end at the 50% point of V_O.
t_{PLH} ≡ propagation delay time, low-to-high level output
t_{PHL} ≡ propagation delay time, high-to-low level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to Section 7.

4 Data Sheets

SN54ASC5121, SN74ASC5121
TTL-/CMOS-COMPATIBLE OPEN-DRAIN OUTPUT BUFFERS

D2939, AUGUST 1986

SystemCell™ 2-μm OUTPUT STANDARD CELL

- Typical Propagation Delays
  1.7 ns with 15-pF Load
  2.2 ns with 50-pF Load
- Output Current Ratings
  SN54ASC5121 I_{OL} = 37.4 mA
  SN74ASC5121 I_{OL} = 44 mA
- Incorporates Circuitry to Protect Against ESD and Latch-Up
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol

FUNCTION TABLE

INPUT A	OUTPUT Y
H	H
L	L

positive logic equation

$Y = A$

description

The SN54ASC5121 and SN74ASC5121 are noninverting output buffer standard cells that interface CMOS internal cells with a passive pull-up external load. The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		CELL LAYOUT ASPECT RATIO	RELATIVE CELL AREA TO NA210LH
OPFD1LH	Label: OPFD1LH A,Y;	minimum width	54

The cell incorporates circuit elements designed to actively bypass and dissipate electrostatic discharges with potentials ranging up to 4 kilovolts. Guard-ring structures are employed that provide current management techniques for the cell to recover from exposure to high currents of up to 400 milliamperes, thereby negating most common sources that can produce a latch-up condition.

These output cells have been designed to provide low-impedance drive levels for low-logic-level outputs interfacing a bus having a terminated high-level drive source. As a result, passive resistance has been omitted in series with the output transistor. Shorting the low-level output to V_{CC} will cause current flow in excess of that recommended for normal operation. Therefore, it is recommended that outputs not be shorted directly to V_{CC}.

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description (continued)

The dynamic drive capability of each output is specified by the delta propagation delay time parameter included with the switching characteristics. The delta propagation delay times provide a means for making direct comparisons of the various output responses with change in capacitive loading.

The SN54ASC5121 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC5121 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 3 in Section 2. The maximum low-level output current is 37.4 milliamperes for the SN54ASC5121 and 44 milliamperes for the SN74ASC5121.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ASC5121			SN74ASC5121			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_T	Input threshold voltage	V_{CC} = 5 V,	T_A = 25°C		2.2			2.2		V
V_{OL}	Low-level output voltage	I_{OL} = 44 mA							0.5	V
		I_{OL} = 37.4 mA				0.5				
		I_{OL} = 20 μA,	See Note 1			0.1			0.1	
I_{OZ}	Off-state output current	V_O = V_{CC} or 0				±10			±5	μA
I_{CC}	Supply current	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX				2203			132	nA
C_i	Input capacitance	V_{CC} = 5 V,	T_A = 25°C		1.2			1.2		pF
C_{pd}	Equivalent power dissipation capacitance	V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,		10.4			10.4		pF

NOTE 1: These limits apply when all other outputs are open.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5121			SN74ASC5121			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PZL}	A	Y	C_L = 15 pF, R_L = 1 kΩ to V_{CC}		1.7			1.7		ns
t_{PZL}	A	Y	C_L = 50 pF, R_L = 1 kΩ to V_{CC}		2.2			2.2		ns
t_{PLZ}	A	Y	R_L = 1 kΩ to V_{CC}		8.3			8.3		ns
Δt_{PZL}	A	Y			14			14		ps/pF

CMOS loads

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5121			SN74ASC5121			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PZL}	A	Y	C_L = 15 pF, R_L = 1 kΩ to V_{CC}		1.5			1.5		ns
t_{PZL}	A	Y	C_L = 50 pF, R_L = 1 kΩ to V_{CC}		2			2		ns
Δt_{PZL}	A	Y			14			14		ps/pF

† Propagation delay times are measured from the 44% point of V_I with $t_r = t_f$ = 3 ns (10% and 90%). For TTL loads, the times end at V_O = 1.3 V. For CMOS loads, the times end at the 50% point of V_O.
t_{PZL} ≡ output enable time to low level
t_{PLZ} ≡ output disable time from low level
Δt_{PZL} ≡ change in t_{PZL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to Section 7.

SN54ASC5123, SN74ASC5123
TTL-/CMOS-COMPATIBLE OPEN-DRAIN OUTPUT BUFFERS

D2939, AUGUST 1986

SystemCell™ 2-μm OUTPUT STANDARD CELL

- Typical Propagation Delays
  1.5 ns with 15-pF Load
  1.9 ns with 50-pF Load
- Output Current Ratings
  SN54ASC5123 I_{OL} = 40.8 mA
  SN74ASC5123 I_{OL} = 48 mA
- Incorporates Circuitry to Protect Against ESD and Latch-Up
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol

FUNCTION TABLE

INPUT A	OUTPUT Y
H	H
L	L

positive logic equation

$Y = A$

description

The SN54ASC5123 and SN74ASC5123 are noninverting output buffer standard-cells that interface CMOS internal cells with a passive pull-up external load. The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		CELL LAYOUT ASPECT RATIO	RELATIVE CELL AREA TO NA210LH
OPFE1LH	Label: OPFE1LH A,Y;	minimum width	69

The cell incorporates circuit elements designed to actively bypass and dissipate electrostatic discharges with potentials ranging up to 4 kilovolts. Guard-ring structures are employed that provide current management techniques for the cell to recover from exposure to high currents of up to 400 milliamperes, thereby negating most common sources that can produce a latch-up condition.

These output cells have been designed to provide low-impedance drive levels for the low-logic-level outputs interfacing a bus having a terminated high-level drive source. As a result, passive resistance has been omitted in series with the output transistor. Shorting the low-level output to V_{CC} will cause current flow in excess of that recommended for normal operation. Therefore, it is recommended that outputs not be shorted directly to V_{CC}.

The dynamic drive capability of each output is specified by the delta propagation delay time parameter included with the switching characteristics. The delta propagation delay times provide a means for making direct comparisons of the various output responses with change in capacitive loading.

The SN54ASC5123 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC5123 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 3 in Section 2. The maximum low-level output current is 40.8 milliamperes for the SN54ASC5123 and 48 milliamperes for the SN74ASC5123.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54ASC5123			SN74ASC5123			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_T	Input threshold voltage	V_{CC} = 5 V, T_A = 25°C		2.2			2.2		V
V_{OL}	Low-level output voltage	I_{OL} = 48 mA,						0.5	V
		I_{OL} = 40.8 μA,			0.5				
		I_{OL} = 20 μA, See Note 1			0.1			0.1	
I_{OZ}	Off-state output current	V_O = V_{CC} or 0			±10			±5	μA
I_{CC}	Supply current	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX			3171			190	nA
C_i	Input capacitance	V_{CC} = 5 V, T_A = 25°C		1.8			1.8		pF
C_{pd}	Equivalent power dissipation capacitance	V_{CC} = 5 V, t_r = t_f = 3 ns, T_A = 25°C		16.2			16.2		pF

NOTE 1: These limits apply when all other outputs are open.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5123			SN74ASC5123			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PZL}	A	Y	C_L = 15 pF, R_L = 1 kΩ to V_{CC}		1.5			1.5		ns
t_{PZL}	A	Y	C_L = 50 pF, R_L = 1 kΩ to V_{CC}		1.9			1.9		ns
t_{PLZ}	A	Y	R_L = 1 kΩ to V_{CC}		9			9		ns
Δt_{PZL}	A	Y			11			11		ps/pF

CMOS loads

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5123			SN74ASC5123			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PZL}	A	Y	C_L = 15 pF, R_L = 1 kΩ to V_{CC}		1.3			1.3		ns
t_{PZL}	A	Y	C_L = 50 pF, R_L = 1 kΩ to V_{CC}		1.7			1.7		ns
Δt_{PZL}	A	Y			11			11		ps/pF

† Propagation delay times are measured from the 44% point of V_I with t_r = t_f = 3 ns (10% and 90%). For TTL loads, the times end at V_O = 1.3 V. For CMOS loads, the times end at 50% point of V_O.
t_{PZL} ≡ output enable time to low level
t_{PLZ} ≡ output disable time from low level
Δt_{PZL} ≡ change in t_{PZL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to Section 7.

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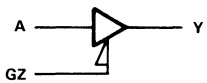
SN54ASC5124, SN74ASC5124
TTL-/CMOS-COMPATIBLE 3-STATE OUTPUT BUFFERS

D2939, AUGUST 1986

SystemCell™ 2-μm OUTPUT STANDARD CELL

- Typical Propagation Delays
  2.5 ns with 15-pF Load
  3 ns with 50-pF Load
- Output Current Ratings
  SN54ASC5124 I_{OL} = 37.4 mA
  I_{OH} = −10.2 mA
  SN74ASC5124 I_{OL} = 44 mA
  I_{OH} = −12 mA
- Incorporates Circuitry to Protect Against ESD and Latch-Up
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol



FUNCTION TABLE

INPUTS		OUTPUT
GZ	A	Y
L	H	H
L	L	L
H	X	Z

positive logic equation

Y = A (when GZ is L)

description

The SN54ASC5124 and SN74ASC5124 are noninverting 3-state output buffer standard cells that interface CMOS internal cells with TTL or CMOS external buses. The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		CELL LAYOUT ASPECT RATIO	RELATIVE CELL AREA TO NA210LH
OPFD3LH	Label: OPFD3LH A,GZ,Y;	minimum width	93

The cell incorporates circuit elements designed to actively bypass and dissipate electrostatic discharges with potentials ranging up to 4 kilovolts. Guard-ring structures are employed that provide current management techniques for the cell to recover from exposure to high currents of up to 400 milliamperes, thereby negating most common sources that can produce a latch-up condition.

These output cells have been designed to provide low-impedance drive levels for both the high-and low-logic-level states. As a result, passive resistance has been omitted in series with the output transistors. Shorting a high-level output to ground or a low-level output to V_{CC} will cause current flow in excess of that recommended for normal operation. Therefore, it is recommended that outputs not be shorted directly to ground or V_{CC}.

The dynamic drive capability of each output is specified by the delta propagation delay time parameter included with the switching characteristics. The delta propagation delay times provide a means for making direct comparisons of the various output responses with change in capacitive loading.

The SN54ASC5124 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC5124 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 3 in Section 2. The maximum high-level output current is 10.2 milliamperes for the SN54ASC5124 and 12 milliamperes for the SN74ASC5124. The maximum low-level output current is 37.4 milliamperes for the SN54ASC5124 and 44 milliamperes for the SN74ASC5124.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		SN54ASC5124			SN74ASC5124			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C		2.2			2.2		V
V_{OH}	High-level output voltage		I_{OH} = −12 mA					3.7			V
			I_{OH} = −10.2 mA		3.7						
			I_{OH} = −20 μA,	See Note 1	V_{CC}−0.1			V_{CC}−0.1			
V_{OL}	Low-level output voltage		I_{OL} = 44 mA							0.5	V
			I_{OL} = 37.4 mA				0.5				
			I_{OL} = 20 μA,	See Note 1			0.1			0.1	
I_{OZ}	Off-state output current		V_O = V_{CC} or 0				±10			±5	μA
I_{CC}	Supply current		V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX				6320			379	nA
C_i	Input capacitance	A	V_{CC} = 5 V,	T_A = 25°C		1.8			1.8		pF
		GZ				1.4			1.4		
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	$t_r = t_f$ = 3 ns,		49			49		pF

NOTE 1: These limits apply when all other outputs are open.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, C_L = 15 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5124			SN74ASC5124			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	R_L = ∞		2.2			2.2		ns
t_{PHL}					2.5			2.5		
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND		3			3		ns
t_{PZL}			R_L = 1 kΩ to V_{CC}		2.1			2.1		

† Propagation delay times are measured from the 44% point of V_I with $t_r = t_f$ = 3 ns (10% and 90%). For TTL loads, the times end at V_O = 1.3 V.
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output disable time from low level
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

TTL loads, C_L = 50 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5124			SN74ASC5124			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	$R_L = \infty$		2.8			2.8		ns
t_{PHL}					3			3		
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND		3.6			3.6		ns
t_{PZL}			R_L = 1 kΩ to V_{CC}		2.8			2.8		
t_{PHZ}	GZ	Y	R_L = 1 kΩ to GND		10			10		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		9			9		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5124			SN74ASC5124			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
Δt_{PLH}	A	Y			17			17		ps/pF
Δt_{PHL}					14			14		
Δt_{PZH}	GZ	Y			17			17		ps/pF
Δt_{PZL}					20			20		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

CMOS loads, C_L = 15 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5124			SN74ASC5124			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	$R_L = \infty$		2.7			2.7		ns
t_{PHL}					2.2			2.2		
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND		3.4			3.4		ns
t_{PZL}			R_L = 1 kΩ to V_{CC}		1.8			1.8		

CMOS loads, C_L = 50 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5124			SN74ASC5124			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	$R_L = \infty$		3.6			3.6		ns
t_{PHL}					2.6			2.6		
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND		4.4			4.4		ns
t_{PZL}			R_L = 1 kΩ to V_{CC}		2.4			2.4		

†Propagation delay times are measured from the 44% point of V_I with $t_r = t_f$ = 3 ns (10% and 90%). For TTL loads, the times end at V_O = 1.3 V. For CMOS loads, the times end at the 50% point of V_O.

t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
t_{PHZ} ≡ output disable time from high level
t_{PLZ} ≡ output disable time from low level

Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
Δt_{PZH} ≡ change in t_{PZH} with load capacitance
Δt_{PZL} ≡ change in t_{PZL} with load capacitance

‡Typical values are at V_{CC} = 5 V, T_A = 25°C.

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

CMOS loads

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5124			SN74ASC5124			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
Δt_{PLH}	A	Y			26			26		ps/pF
Δt_{PHL}					11			11		
Δt_{PZH}	GZ	Y			29			29		ps/pF
Δt_{PZL}					17			17		

† Propagation delay times are measured from the 44% point of V_I with $t_r = t_f = 3$ ns (10% and 90%). For CMOS loads, the times end at the 50% point of V_O.
$\Delta t_{PLH} \equiv$ change in t_{PLH} with load capacitance
$\Delta t_{PHL} \equiv$ change in t_{PHL} with load capacitance
$\Delta t_{PZH} \equiv$ change in t_{PZH} with load capacitance
$\Delta t_{PZL} \equiv$ change in t_{PZL} with load capacitance
‡ Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

DESIGN CONSIDERATIONS

Refer to Section 7.

TEXAS INSTRUMENTS
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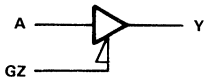
SN54ASC5125, SN74ASC5125
TTL-/CMOS-COMPATIBLE 3-STATE OUTPUT BUFFERS

D2939, AUGUST 1986

SystemCell™ 2-μm OUTPUT STANDARD CELL

- Typical Propagation Delays
  2.8 ns with 15-pF Load
  3.7 ns with 50-pF Load
- Output Current Ratings
  SN54ASC5125 I_{OL} = 20.4 mA
  I_{OH} = −10.2 mA
  SN74ASC5125 I_{OL} = 24 mA
  I_{OH} = −12 mA
- Incorporates Circuitry to Protect Against ESD and Latch-Up
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol



FUNCTION TABLE

INPUTS		OUTPUT
GZ	A	Y
L	H	H
L	L	L
H	X	Z

positive logic equation

Y = A (when GZ is L)

description

The SN54ASC5125 and SN74ASC5125 are noninverting 3-state output buffer standard cells that interface CMOS internal cells with TTL or CMOS external buses. The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		CELL LAYOUT ASPECT RATIO	RELATIVE CELL AREA TO NA210LH
OPFB3LH	Label: OPFB3LH A,GZ,Y;	minimum width	64

The cell incorporates circuit elements designed to actively bypass and dissipate electrostatic discharges with potentials ranging up to 4 kilovolts. Guard-ring structures are employed that provide current management techniques for the cell to recover from exposure to high currents of up to 400 milliamperes, thereby negating most common sources that can produce a latch-up condition.

These output cells have been designed to provide low-impedance drive levels for both the high- and low-logic-level states. As a result, passive resistance has been omitted in series with the output transistors. Shorting a high-level output to ground or a low-level output to V_{CC} will cause current flow in excess of that recommended for normal operation. Therefore, it is recommended that outputs not be shorted directly to ground or V_{CC}.

The dynamic drive capability of each output is specified by the delta propagation delay time parameter included with the switching characteristics. The delta propagation delay times provide a means for making direct comparisons of the various output responses with change in capacitive loading.

The SN54ASC5125 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC5125 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 3 in Section 2. The maximum high-level output current is 10.2 milliamperes for the SN54ASC5125 and 12 milliamperes for the SN74ASC5125. The maximum low-level output current is 20.4 milliamperes for the SN54ASC5125 and 24 milliamperes for the SN74ASC5125.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ASC5125			SN74ASC5125			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_T	Input threshold voltage	V_{CC} = 5 V,	T_A = 25°C		2.2			2.2		V
V_{OH}	High-level output voltage	I_{OH} = −12 mA					3.7			V
		I_{OH} = −10.2 mA		3.7						
		I_{OH} = −20 μA,	See Note 1	V_{CC}−0.1			V_{CC}−0.1			
V_{OL}	Low-level output voltage	I_{OL} = 24 mA							0.5	V
		I_{OL} = 20.4 mA				0.5				
		I_{OL} = 20 μA,	See Note 1			0.1			0.1	
I_{OZ}	Off-state output current	V_O = V_{CC} or 0				±10			±5	μA
I_{CC}	Supply current	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX				4009			241	nA
C_i	Input capacitance	V_{CC} = 5 V,	T_A = 25°C		1.1			1.1		pF
C_{pd}	Equivalent power dissipation capacitance	V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,		29			29		pF

NOTE 1: These limits apply when all other outputs are open.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, C_L = 15 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5125			SN74ASC5125			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	R_L = ∞		2.3			2.3		ns
t_{PHL}					3.2			3.2		
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND		2.7			2.7		ns
t_{PZL}			R_L = 1 kΩ to V_{CC}		3			3		

† Propagation delay times are measured from the 44% point of V_I with t_r = t_f = 3 ns (10% and 90%). For TTL loads, the times end at V_O = 1.3 V.
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output disable time from low level
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

TTL loads, C_L = 50 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5125			SN74ASC5125			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	R_L = ∞		2.9			2.9		ns
t_{PHL}					4.3			4.3		
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND		3.4			3.4		ns
t_{PZL}			R_L = 1 kΩ to V_{CC}		4.2			4.2		
t_{PHZ}	GZ	Y	R_L = 1 kΩ to GND		8.5			8.5		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		8.2			8.2		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5125			SN74ASC5125			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
Δt_{PLH}	A	Y			17			17		ps/pF
Δt_{PHL}					31			31		
Δt_{PZH}	GZ	Y			20			20		ps/pF
Δt_{PZL}					34			34		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

CMOS loads, C_L = 15 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5125			SN74ASC5125			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	R_L = ∞		2.7			2.7		ns
t_{PHL}					2.9			2.9		
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND		3.2			3.2		ns
t_{PZL}			R_L = 1 kΩ to V_{CC}		2.6			2.6		

CMOS loads, C_L = 50 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5125			SN74ASC5125			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	R_L = ∞		3.7			3.7		ns
t_{PHL}					3.7			3.7		
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND		4.2			4.2		ns
t_{PZL}			R_L = 1 kΩ to V_{CC}		3.5			3.5		

†Propagation delay times are measured from the 44% point of V_I with $t_r = t_f$ = 3 ns (10% and 90%). For TTL loads, the times end at V_O = 1.3 V. For CMOS loads, the times end at the 50% point of V_O.

t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
t_{PHZ} ≡ output disable time from high level
t_{PLZ} ≡ output disable time from low level

Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
Δt_{PZH} ≡ change in t_{PZH} with load capacitance
Δt_{PZL} ≡ change in t_{PZL} with load capacitance

‡Typical values are at V_{CC} = 5 V, T_A = 25°C.

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

CMOS loads

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5125			SN74ASC5125			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
Δt_{PLH}	A	Y			29			29		ps/pF
Δt_{PHL}					23			23		
Δt_{PZH}	GZ	Y			29			29		ps/pF
Δt_{PZL}					26			26		

† Propagation delay times are measured from the 44% point of V_I with $t_r = t_f = 3$ ns (10% and 90%). For TTL loads, the times end at the 50% point of V_O.
$\Delta t_{PLH} \equiv$ change in t_{PLH} with load capacitance
$\Delta t_{PHL} \equiv$ change in t_{PHL} with load capacitance
$\Delta t_{PZH} \equiv$ change in t_{PZH} with load capacitance
$\Delta t_{PZL} \equiv$ change in t_{PZL} with load capacitance
‡ Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

DESIGN CONSIDERATIONS

Refer to Section 7.

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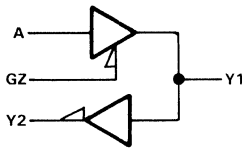
SystemCell™ 2-μm OUTPUT STANDARD CELL

- Typical Propagation Delays
  3.3 ns with 15-pF Load
  5.9 ns with 50-pF Load
- Output Current Ratings:
  SN54ASC5200 I_{OL} = 3.4 mA
  I_{OH} = −3.4 mA
  SN74ASC5200 I_{OL} = 4 mA
  I_{OH} = −4 mA
- Incorporates Circuitry to Protect Against ESD and Latch-Up
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol



FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	H
H	L	H	H	L
X	H	L	Z	H
X	H	H	Z	L

positive logic equations

$Y1 = A \qquad Y2 = \overline{Y1}$

description

The SN54ASC5200 and SN74ASC5200 are three-state input/output buffer standard cells that interface CMOS internal cells with TTL or CMOS bidirectional bus lines. The input buffer responds to CMOS threshold levels imposed on the I/O bus regardless of the state of the internal 3-state control GZ. This cell function exists in two versions (''E'' and ''F'') with different physical implementations to allow the final IC area to be optimized. Since the electrical performance of each version is identical, for simplicity only one version (the ''F'' cell) will be contained in the engineering workstation cell libraries. Determination of the most appropriate cell version will be made during the layout stage. The cell is designated and called from the engineering workstation input using the following cell name and netlist label:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		CELL LAYOUT ASPECT RATIO	RELATIVE CELL AREA TO NA210LH
IOE40LH IOF40LH	Label: IOF40LH A,GZ,Y2,Y1;	minimum height minimum width	44.5 49.5

The cells incorporate circuit elements designed to actively bypass and dissipate electrostatic discharges with potentials ranging up to 4 kilovolts. Guard-ring structures are employed that provide current management techniques for the cell to recover from exposure to high currents of up to 400 milliamperes, thereby negating most common sources that can produce a latch-up condition.

These output cells have been designed to provide low-impedance drive levels for both the high- and low-logic-level states. As a result, shorting a high-level output to ground or a low-level output to V_{CC} will cause current flow in excess of that recommended for normal operation. Therefore, it is recommended that outputs not be shorted directly to ground or V_{CC}.

description (continued)

The dynamic drive capability of each output is specified by the delta propagation delay time parameter included with the switching characteristics. The delta propagation delay times provide a means for making direct comparisons of the various outputs response with change in capacitive loading.

The SN54ASC5200 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC5200 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 4 in Section 2. The maximum high-level or maximum low-level output current is 3.4 milliamperes for the SN54ASC5200 and 4 milliamperes for the SN74ASC5200.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54ASC5200			SN74ASC5200			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_T Input threshold voltage	A,GZ	V_{CC} = 5 V, T_A = 25°C		2.2			2.2		V
	Y1			2.5			2.5		
V_{OH} High-level output voltage		I_{OH} = −4 mA				3.7			V
		I_{OH} = −3.4 mA	3.7						
		I_{OH} = −20 μA, See Note 1	V_{CC}−0.1			V_{CC}−0.1			
V_{OL} Low-level output voltage		I_{OL} = 4 mA						0.5	V
		I_{OL} = 3.4 mA			0.5				
		I_{OL} = 20 μA, See Note 1			0.1			0.1	
I_{OZ} Off-state output current		V_O = V_{CC} or 0			±10			±5	μA

NOTE 1: These limits apply when all other outputs are open.

IOE40LH

PARAMETER		TEST CONDITIONS	SN54ASC5200		SN74ASC5200		UNIT
			TYP	MAX	TYP	MAX	
I_{CC} Supply current		V_I = V_{CC} or 0		2373		142	nA
		V_I = 3.15 V or 0.9 V		4.33		4.1	mA
C_i Input capacitance	A	V_{CC} = 5 V, T_A = 25°C	0.61		0.61		pF
	GZ		0.4		0.4		
	Y1†		3.84		3.84		
C_{pd} Equivalent power dissipation capacitance		V_{CC} = 5 V, t_r = t_f = 3 ns, T_A = 25°C	12.5		12.5		pF

IOF40LH

PARAMETER		TEST CONDITIONS	SN54ASC5200		SN74ASC5200		UNIT
			TYP	MAX	TYP	MAX	
I_{CC} Supply current		V_I = V_{CC} or 0		2592		155	nA
		V_I = 3.15 V or 0.9 V		4.29		4.06	mA
C_i Input capacitance	A	V_{CC} = 5 V, T_A = 25°C	0.59		0.59		pF
	GZ		0.47		0.47		
	Y1†		4.38		4.38		
C_{pd} Equivalent power dissipation capacitance		V_{CC} = 5 V, t_r = t_f = 3 ns, T_A = 25°C	12.7		12.7		pF

†Total input capacitance is dependent on the package type and is equal to the sum of package capacitance and intrinsic input capacitance.

TEXAS INSTRUMENTS
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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, C_L = 15 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5200			SN74ASC5200			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y1	R_L = ∞	1.3	2.5	5.9	1.4	2.5	5.3	ns
t_{PHL}				2.1	4.5	11.6	2.3	4.5	10.4	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.5	3.4	8.4	1.6	3.4	7.6	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.1	4.6	11.8	2.2	4.6	10.5	

TTL loads, C_L = 50 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5200			SN74ASC5200			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y1	R_L = ∞	1.8	3.6	8.8	2	3.6	7.8	ns
t_{PHL}				3.9	8.2	19.8	4.3	8.2	17.4	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2	4.5	11.3	2.1	4.5	10.2	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4	8.5	20.8	4.3	8.5	18.1	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		11			11		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		10			10		

change in propagation delay times with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5200			SN74ASC5200			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
Δt_{PLH}	A	Y1		10	31	80	20	31	80	ps/pF
Δt_{PHL}				50	106	230	50	106	210	
Δt_{PZH}	GZ	Y1		10	31	80	20	31	60	ps/pF
Δt_{PZL}				50	111	260	60	111	240	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

CMOS loads, C_L = 15 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5200			SN74ASC5200			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y1	R_L = ∞	1.5	3.1	7.5	1.7	3.1	6.7	ns
t_{PHL}				1.8	3.7	9.7	2	3.7	8.6	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2	4	9.8	2.2	4	8.8	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.8	3.7	9.4	1.9	3.7	8.4	

† Propagation delay times are measured from the 44% point of V_I with t_r = t_f = 3 ns (10% and 90%). For TTL loads, the times end at V_O = 1.3 V. For CMOS loads, the times end at the 50% point of V_O.

t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
t_{PHZ} ≡ output disable time from high level
t_{PLZ} ≡ output disable time from low level

Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
Δt_{PZH} ≡ change in t_{PZH} with load capacitance
Δt_{PZL} ≡ change in t_{PZL} with load capacitance

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

CMOS loads, C_L = 50 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5200			SN74ASC5200			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.6	5.2	12.1	2.8	5.2	10.8	ns
t_{PHL}				2.9	6.2	15.5	3.2	6.2	13.7	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	3.1	6.2	14.6	3.3	6.2	13	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.9	6.2	15.7	3.2	6.2	13.8	

change in propagation delay times with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5200			SN74ASC52000			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
Δt_{PLH}	A	Y1		30	60	140	30	60	120	ps/pF
Δt_{PHL}				30	69	170	30	69	150	
Δt_{PZH}	GZ	Y1		30	63	140	30	63	130	ps/pF
Δt_{PZL}				30	71	190	40	71	160	

input buffer switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER§	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5200			SN74ASC52000			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Y1	Y2	C_L = 0	0.4	0.7	1.2	0.4	0.7	1.2	ns
t_{PHL}				0.2	0.7	1.5	0.3	0.7	1.3	
t_{PLH}	Y1	Y2	C_L = 1 pF	0.7	1	1.8	0.7	1	1.8	ns
t_{PHL}				0.5	1.1	2.3	0.6	1.1	2.1	
Δt_{PLH}	Y1	Y2		0.2	0.3	0.7	0.2	0.3	0.7	ns/pF
Δt_{PHL}				0.2	0.4	0.9	0.2	0.4	0.8	

† Propagation delay times are measured from the 44% point of V_I with $t_r = t_f$ = 3 ns (10% and 90%). For CMOS loads, the times end at the 50% point of V_O.

t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
Δt_{PZH} ≡ change in t_{PZH} with load capacitance
Δt_{PZL} ≡ change in t_{PZL} with load capacitance

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Input propagation delay times are measured from the 50% point of V_I to the 44% point of V_O with $t_r = t_f$ = 4 ns.

DESIGN CONSIDERATIONS

Refer to Section 7.

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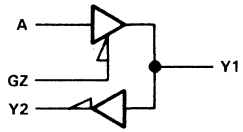
SystemCell™ 2-μm OUTPUT STANDARD CELL

- Typical Propagation Delays
  3.5 ns with 15-pF Load
  5.8 ns with 50-pF Load
- Output Current Ratings
  SN54ASC5201 I_{OL} = 3.4 mA
  I_{OH} = −3.4 mA
  SN74ASC5201 I_{OL} = 4 mA
  I_{OH} = −4 mA
- Incorporates Circuitry to Protect Against ESD and Latch-Up
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol



FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	H
H	L	H	H	L
X	H	L	Z	H
X	H	H	Z	L

positive logic equations

$Y1 = A \qquad Y2 = \overline{Y1}$

description

The SN54ASC5201 and SN74ASC5201 are 3-state input/output buffer standard-cells that interface CMOS internal cells with TTL or CMOS bidirectional bus lines. The input buffer responds to TTL threshold levels imposed on the I/O bus regardless of the state of the internal 3-state control GZ. This cell function exists in two versions (''E'' and ''F'') with different physical implementations to allow the final IC area to be optimized. Since the electrical performance of each version is identical, for simplicity only one version (the ''F'' cell) will be contained in the engineering workstation cell libraries. Determination of the most appropriate cell version will be made during the layout stage. The cell is designated and called from the engineering workstation input using the following cell name and netlist label:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		CELL LAYOUT ASPECT RATIO	RELATIVE CELL AREA TO NA210LH
IOE43LH IOF43LH	Label: IOF43LH A,GZ,Y2,Y1;	minimum height minimum width	47.7 50.9

The cells incorporate circuit elements designed to actively bypass and dissipate electrostatic discharges with potentials ranging up to 4 kilovolts. Guard-ring structures are employed that provide current management techniques for the cell to recover from exposure to high currents of up to 400 milliamperes, thereby negating most common sources that can produce a latch-up condition.

These output cells have been designed to provide low-impedance drive levels for both the high- and low-logic-level states. As a result, passive resistance has been omitted in series with the output transistors. Shorting a high-level output to ground or a low-level output to V_{CC} will cause current flow in excess of that recommended for normal operation. Therefore, it is recommended that outputs not be shorted directly to ground or V_{CC}.

description (continued)

The dynamic drive capability of each output is specified by the delta propagation delay time parameter included with the switching characteristics. The delta propagation delay times provide a means for making direct comparisons of the various output responses to change in capacitive loading.

The SN54ASC5201 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC5201 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 4 in Section 2. The maximum high-level or maximum low-level output current is 3.4 milliamperes for the SN54ASC5201 and 4 milliamperes for the SN74ASC5201.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54ASC5201			SN74ASC5201			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_T Input threshold voltage	A,GZ	V_{CC} = 5 V, T_A = 25°C		2.2			2.2		V
	Y1			1.3			1.3		
V_{OH} High-level output voltage		I_{OH} = −4 mA				3.7			V
		I_{OH} = −3.4 mA	3.7						
		I_{OH} = −20 μA, See Note 1	V_{CC}−0.1			V_{CC}−0.1			
V_{OL} Low-level output voltage		I_{OL} = 4 mA						0.5	V
		I_{OL} = 3.4 mA			0.5				
		I_{OL} = 20 μA, See Note 1			0.1			0.1	
I_{OZ} Off-state output current		V_O = V_{CC} or 0			±10			±5	μA

NOTE 1: These limits apply when all other outputs are open.

IOE43LH

PARAMETER		TEST CONDITIONS	SN54ASC5201		SN74ASC5201		UNIT
			TYP	MAX	TYP	MAX	
I_{CC} Supply current		V_I = V_{CC} or 0		2500		150	nA
		V_I = 2 V or 0.8 V		1.2		1.12	mA
C_i Input capacitance	A	V_{CC} = 5 V, T_A = 25°C	0.62		0.62		pF
	GZ		0.41		0.41		
	Y1†		4.34		4.34		
C_{pd} Equivalent power dissipation capacitance		V_{CC} = 5 V, t_r = t_f = 3 ns, T_A = 25°C	13.2		13.2		pF

IOF43LH

PARAMETER		TEST CONDITIONS	SN54ASC5201		SN74ASC5201		UNIT
			TYP	MAX	TYP	MAX	
I_{CC} Supply current		V_I = V_{CC} or 0		2588		155	nA
		V_I = 2 V or 0.8 V		1.21		1.13	mA
C_i Input capacitance	A	V_{CC} = 5 V, T_A = 25°C	0.59		0.59		pF
	GZ		0.47		0.47		
	Y1†		4.26		4.26		
C_{pd} Equivalent power dissipation capacitance		V_{CC} = 5 V, t_r = t_f = 3 ns, T_A = 25°C	13.4		13.4		pF

†Total input capacitance is dependent on the package type and is equal to the sum of package capacitance and intrinsic input capacitance.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, C_L = 15 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5201			SN74ASC5201			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y1	R_L = ∞	1.3	2.5	6	1.4	2.5	5.4	ns
t_{PHL}				2.1	4.5	11.2	2.2	4.5	9.9	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.5	3.5	8.5	1.6	3.5	7.8	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2	4.4	11.2	2.2	4.4	9.8	

TTL loads, C_L = 50 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5201			SN74ASC5201			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y1	R_L = ∞	1.8	3.6	9	2	3.6	8	ns
t_{PHL}				3.7	8	20.2	4	8	17.7	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2	4.6	11.4	2.2	4.6	10.4	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.7	8	21.7	4	8	18.7	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		11			11		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		10			10		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5201			SN74ASC5201			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
Δt_{PLH}	A	Y1		10	31	80	20	31	70	ps/pF
Δt_{PHL}				50	100	260	50	100	220	
Δt_{PZH}	GZ	Y1		10	31	90	20	31	80	ps/pF
Δt_{PZL}				50	103	300	50	103	250	

† Propagation delay times are measured from the 44% point of V_I with $t_r = t_f$ = 3 ns (10% and 90%). For TTL loads, the times end at V_O = 1.3 V.

t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
t_{PHZ} ≡ output disable time from high level
t_{PLZ} ≡ output disable time from low level

Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
Δt_{PZH} ≡ change in t_{PZH} with load capacitance
Δt_{PZL} ≡ change in t_{PZL} with load capacitance

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

CMOS loads, C_L = 15 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5201			SN74ASC5201			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y1	R_L = ∞	1.5	3.1	7.7	1.7	3.1	6.8	ns
t_{PHL}				1.8	3.5	9.2	1.9	3.5	8.1	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.1	4	10	2.2	4	8.9	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.7	3.3	8.7	1.8	3.3	7.7	

CMOS loads, C_L = 50 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5201			SN74ASC5201			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y1	R_L = ∞	2.5	5.2	12.3	2.7	5.2	11	ns
t_{PHL}				2.8	5.6	15.4	3	5.6	13.4	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	3.1	6.1	14.8	3.3	6.1	13.2	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.8	5.6	15.6	3	5.6	13.6	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5201			SN74ASC5201			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
Δt_{PLH}	A	Y1		30	60	130	30	60	120	ps/pF
Δt_{PHL}				30	60	180	30	60	150	
Δt_{PZH}	GZ	Y1		30	60	140	30	60	120	ps/pF
Δt_{PZL}				30	66	200	30	66	170	

input buffer switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER§	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5201			SN74ASC5201			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Y1	Y2	C_L = 0	0.6	1	2.2	0.6	1	1.9	ns
t_{PHL}				0.5	0.9	1.4	0.5	0.9	1.4	
t_{PLH}	Y1	Y2	C_L = 1 pF	1.6	2.9	6.2	1.7	2.9	5.6	ns
t_{PHL}				0.8	1.3	2.2	0.8	1.3	2.1	
Δt_{PLH}	Y1	Y2		0.9	1.9	4.1	1	1.9	3.7	ns/pF
Δt_{PHL}				0.3	0.4	0.9	0.3	0.4	0.8	

† Propagation delay times are measured from the 44% point of V_I with $t_r = t_f$ = 3 ns (10% and 90%). For CMOS loads, the times end at the 50% point of V_O.

t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
Δt_{PZH} ≡ change in t_{PZH} with load capacitance
Δt_{PZL} ≡ change in t_{PZL} with load capacitance

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Input propagation delay times are measured from the 1.3 V point of V_I to the 44% point of V_O with $t_r = t_f$ = 2 ns.

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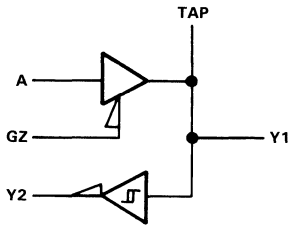
SystemCell™ 2-μm OUTPUT STANDARD CELL

- Typical Propagation Delays
  3.6 ns with 15-pF Load
  6.8 ns with 50-pF Load
- Output Current Ratings
  SN54ASC5202 I_{OL} = 3.4 mA
  I_{OH} = −3.4 mA
  SN74ASC5202 I_{OL} = 4 mA
  I_{OH} = −4 mA
- Incorporates Circuitry to Protect Against ESD and Latch-Up
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol



FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	H
H	L	H	H	L
X	H	L	Z	H
X	H	H	Z	L

positive logic equations

$Y = A \qquad Y2 = \overline{Y1}$

description

The SN54ASC5202 and SN74ASC5202 are 3-state input/output buffer standard cells that interface CMOS internal cells with TTL or CMOS bidirectional bus lines. The Schmitt-trigger input buffer, providing additional noise-rejection with its hysteresis loop, responds to CMOS threshold levels imposed on the I/O bus regardless of the state of the internal 3-state control GZ. The cell is designated and called from the engineering workstation input using the following cell name and netlist label:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		CELL LAYOUT ASPECT RATIO	RELATIVE CELL AREA TO NA210LH
IOF47LH	Label: IOF47LH A,GZ,TAP,Y2,Y1;	minimum width	55.4

The cell incorporates circuit elements designed to actively bypass and dissipate electrostatic discharges with potentials ranging up to 4 kilovolts. Guard-ring structures are employed that provide current management techniques for the cell to recover from exposure to high currents of up to 400 milliamperes, thereby negating most common sources that can produce a latch-up condition.

The IOF47LH incorporates a pull-up tap to simplify termination of the I/O. This tap may be used in conjunction with an active pull-up/pull-down terminator in the 'ASC237x group or the pull-up tap may be left unconnected. When the terminator is used it ensures that the input will be driven to a high or low logic level thereby avoiding exposure to a high-impedance or floating condition. Refer to Section 7 for implementation of the pull-up.

description (continued)

These output cells have been designed to provide low-impedance drive levels for both the high- and low-logic-level states. As a result, passive resistance has been omitted in series with the output transistors. Shorting a high-level output to ground or a low-level output to V_{CC} will cause current flow in excess of that recommended for normal operation. Therefore, it is recommended that outputs not be shorted directly to ground or V_{CC}.

The dynamic drive capability of each output is specified by the delta propagation delay time parameter included with the switching characteristics. The delta propogation delay times provide a means for making direct comparisons of the various output responses with change in capacitive loading.

The SN54ASC5202 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC5202 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 4 in Section 2. The maximum high-level or maximum low-level output current is 3.4 milliamperes for the SN54ASC5202 and 4 milliamperes for the SN74ASC5202.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	SN54ASC5202			SN74ASC5202			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_T	Input threshold voltage at A, GZ		V_{CC} = 5 V, T_A = 25°C		2.2			2.2		V
V_{T+}	Positive-going threshold level (Y1)			2.9	3.2	3.5	2.9	3.2	3.5	V
V_{T-}	Negative-going threshold level (Y1)			1.5	1.7	1.9	1.5	1.7	1.9	V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$) at Y1				1.5			1.5		V
V_{OH}	High-level output voltage		I_{OH} = −4 mA				3.7			V
			I_{OH} = −3.4 mA	3.7						
			I_{OH} = −20 μA, See Note 1	V_{CC}−0.1			V_{CC}−0.1			
V_{OL}	Low-level output voltage		I_{OL} = 4 mA						0.5	V
			I_{OL} = 3.4 mA			0.5				
			I_{OL} = 20 μA, See Note 1			0.1			0.1	
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	μA
I_{CC}	Supply current		V_I = V_{CC} or 0			3005			180	nA
			V_I = 3.5 V or 0.9 V			2.44			1.23	mA
C_i	Input capacitance	A	V_{CC} = 5 V, T_A = 25°C		0.55			0.55		pF
		GZ			0.44			0.44		
		TAP or Y1†			4.5			4.5		
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C, t_r = t_f = 3 ns,		13.1			13.1		pF

†Total input capacitance is dependent on the package type and is equal to the sum of package capacitance and intrinsic input capacitance.
NOTE 1: These limits apply when all other outputs are open.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, C_L = 15 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5202			SN74ASC5202			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y1	R_L = ∞	1.3	2.5	5.7	1.4	2.5	5	ns
t_{PHL}				2.3	4.8	11.3	2.5	4.8	10	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.5	3.4	8.2	1.6	3.4	7.4	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.3	4.8	11.4	2.5	4.8	10.1	

TTL loads, C_L = 50 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5202			SN74ASC5202			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y1	R_L = ∞	1.8	3.6	8.5	1.9	3.6	7.5	ns
t_{PHL}				3.9	8.1	19.1	4.2	8.1	16.8	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2	4.5	11	2.2	4.5	9.9	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4	8.3	20.1	4.3	8.3	17.5	
t_{PHZ}			R_L = 1 kΩ to GND		11			11		
t_{PLZ}			R_L = 1 kΩ to V_{CC}		10			10		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5202			SN74ASC5202			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
Δt_{PLH}	A	Y1		10	31	80	10	31	70	ps/pF
Δt_{PHL}				50	94	230	50	94	200	
Δt_{PZH}	GZ	Y1		10	31	80	20	31	70	ps/pF
Δt_{PZL}				50	100	250	50	100	210	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

CMOS loads, C_L = 15 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5202			SN74ASC5202			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y1	R_L = ∞	1.6	3.1	7.2	1.7	3.1	6.4	ns
t_{PHL}				2	4	9.4	2.2	4	8.4	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.1	4	9.5	2.2	4	8.5	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2	3.9	9.2	2.2	3.9	8.2	

† Propagation delay times are measured from the 44% point of V_I with $t_r = t_f$ = 3 ns (10% and 90%). For TTL loads, the times end at V_O = 1.3 V. For CMOS loads, the times end at the 50% point of V_O.

t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
t_{PHZ} ≡ output disable time from high level
t_{PLZ} ≡ output disable time from low level

Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
Δt_{PZH} ≡ change in t_{PZH} with load capacitance
Δt_{PZL} ≡ change in t_{PZL} with load capacitance

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

CMOS loads, C_L = 50 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5202			SN74ASC5202			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.5	5.1	11.7	2.7	5.1	10.4	ns
t_{PHL}				3.1	6.3	15	3.3	6.3	13.3	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	3	6.1	14.1	3.3	6.1	12.6	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.1	6.3	15.2	3.4	6.3	13.4	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

CMOS loads

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5202			SN74ASC5202			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
Δt_{PLH}	A	Y1		30	57	130	30	57	110	ps/pF
Δt_{PHL}				30	66	160	30	66	140	
Δt_{PZH}	GZ	Y1		30	60	130	30	60	120	ps/pF
Δt_{PZL}				30	69	170	30	69	150	

input buffer switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETERS§	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5202			SN74ASC5202			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Y1	Y2	C_L = 0	2.1	2.6	4.3	2.1	2.6	4.1	ns
t_{PHL}				2.1	2.9	5.4	2.1	2.9	4.9	
t_{PLH}	Y1	Y2	C_L = 1 pF	3	4.4	8.4	3.1	4.4	7.8	ns
t_{PHL}				3.1	5	10.9	3.2	5	9.6	
Δt_{PLH}	Y1	Y2		0.9	1.8	4.1	0.9	1.8	3.7	ns/pF
Δt_{PHL}				0.9	2.1	5.5	1.1	2.1	4.7	

†Propagation delay times are measured from the 44% point of V_I with $t_r = t_f$ = 3 ns (10% and 90%). For CMOS loads, the times end at the 50% point of V_O.

t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
Δt_{PZH} ≡ change in t_{PZH} with load capacitance
Δt_{PZL} ≡ change in t_{PZL} with load capacitance

‡Typical values are at V_{CC} = 5 V, T_A = 25°C.

§Input propagation delay times are measured from the 50% point of V_I to the 44% point of V_O with $t_r = t_f$ = 4 ns.

DESIGN CONSIDERATIONS

Refer to Section 7.

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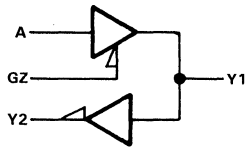
SystemCell™ 2-μm OUTPUT STANDARD CELL

- Typical Propagation Delays
  3.3 ns with 15-pF Load
  5.5 ns with 50-pF Load
- Output Current Ratings
  SN54ASC5203 I_{OL} = 3.4 mA
  I_{OH} = −3.4 mA
  SN74ASC5203 I_{OL} = 4 mA
  I_{OH} = −4 mA
- Incorporates Circuitry to Protect Against ESD and Latch-Up
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol



FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	H
H	L	H	H	L
X	H	L	Z	H
X	H	H	Z	L

positive logic equations

$Y1 = A \qquad Y2 = \overline{Y1}$

description

The SN54ASC5203 and SN74ASC5203 are three-state input/output buffer standard-cells that interface CMOS internal cells with TTL or CMOS bidirectional bus lines. The input buffer responds to TTL threshold levels imposed on the I/O bus regardless of the state of the internal 3-state control GZ. The cell is designated and called from the engineering workstation input using the following cell name and netlist label:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		CELL LAYOUT ASPECT RATIO	RELATIVE CELL AREA TO NA210LH
IOF48LH	Label: IOF48LH A,GZ,Y2,Y1;	minimum width	45.2

The cell incorporates circuit elements designed to actively bypass and dissipate electrostatic discharges with potentials ranging up to 4 kilovolts. Guard-ring structures are employed that provide current management techniques for the cell to recover from exposure to high currents of up to 400 milliamperes, thereby negating most common sources that can produce a latch-up condition.

These output cells have been designed to provide low-impedance drive levels for both the high- and low-logic-level states. As a result, passive resistance has been purposely omitted in series with the output transistors. Shorting a high-level output to ground or a low-level output to V_{CC} will cause current flow in excess of that recommended for normal operation. Therefore, it is recommended that outputs not be shorted directly to ground or V_{CC}.

The dynamic drive capability of each output is specified by the delta delay propagation time parameter included with the switching characteristics. The delta delay times provide a means for making direct comparisons of the various outputs response to change in capacitive loading.

The SN54ASC5203 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC5203 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 4 in Section 2. Maximum high-level or maximum low-level output current is 3.4 milliamperes for the SN54ASC5203 and 4 milliamperes for the SN74ASC5203.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54ASC5203			SN74ASC5203			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_T Input threshold voltage	A,GZ	V_{CC} = 5 V, T_A = 25°C		2.2			2.2		V
	Y1			1.3			1.3		
V_{OH} High-level output voltage		I_{OH} = −4 mA				3.7			V
		I_{OH} = −3.4 mA	3.7						
		I_{OH} = −20 μA, See Note 1	V_{CC}−0.1			V_{CC}−0.1			
V_{OL} Low-level output voltage		I_{OL} = 4 mA						0.5	V
		I_{OL} = 3.4 mA			0.5				
		I_{OL} = 20 μA, See Note 1			0.1			0.1	
I_{OZ} Off-state output current		V_O = V_{CC} or 0			±10			±5	μA

NOTE 1: These limits apply when all other outputs are open.

IOF48LH

PARAMETER		TEST CONDITIONS	SN54ASC5203		SN74ASC5203		UNIT
			TYP	MAX	TYP	MAX	
I_{CC} Supply current		V_I = V_{CC} or 0 V		2795		168	nA
		V_I = 2 V or 0.8 V		1.43		1.32	mA
C_i Input capacitance	A	V_{CC} = 5 V, T_A = 25°C	0.63		0.63		pF
	GZ		0.41		0.41		
	Y1†		4.5		4.5		
C_{pd} Equivalent power dissipation capacitance		V_{CC} = 5 V, t_r = t_f = 3 ns, T_A = 25°C	14.9		14.9		pF

†Total input capacitance for Y1 is dependent on the package type and is equal to the sum of package capacitance and intrinsic input capacitance.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, C_L = 15 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5203			SN74ASC5203			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y1	R_L = ∞	1.3	2.4	5.7	1.4	2.4	5.1	ns
t_{PHL}				2.1	4.2	10	2.2	4.2	8.9	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.5	3.3	8.1	1.6	3.3	7.3	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2	4.2	9.9	2.2	4.2	8.7	

TTL loads, C_L = 50 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5203			SN74ASC5203			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y1	R_L = ∞	1.8	3.6	8.5	1.9	3.6	7.6	ns
t_{PHL}				3.7	7.5	18	4	7.5	16	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2	4.5	11	2.2	4.5	9.9	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.7	7.7	19	4	7.7	16.3	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		11			11		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		10			10		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5203			SN74ASC5203			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
Δt_{PLH}	A	Y1		10	34	80	20	34	70	ps/pF
Δt_{PHL}				50	94	220	50	94	190	
Δt_{PZH}	GZ	Y1		10	54	80	20	54	70	ps/pF
Δt_{PZL}				50	100	250	50	100	210	

† Propagation delay times are measured from the 44% point of V_I with $t_r = t_f$ = 3 ns (10% and 90%). For TTL loads, the times end at V_O = 1.3 V.

t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
t_{PHZ} ≡ output disable time from high level
t_{PLZ} ≡ output disable time from low level

Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
Δt_{PZH} ≡ change in t_{PZH} with load capacitance
Δt_{PZL} ≡ change in t_{PZL} with load capacitance

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

CMOS loads, C_L = 15 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5203			SN74ASC5203			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.5	3.1	7.3	1.6	3.1	6.5	ns
t_{PHL}				1.8	3.5	8.2	1.9	3.5	7.3	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.1	4	9.5	2.2	4	8.4	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.7	3.3	7.8	1.8	3.3	6.9	

CMOS loads, C_L = 50 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5203			SN74ASC5203			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.5	5.1	11.8	2.7	5.1	10.6	ns
t_{PHL}				2.8	5.6	13.6	3	5.6	12	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	3	6.1	14.2	3.3	6.1	12.7	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.8	5.6	13.7	3	5.6	12	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5203			SN74ASC5203			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
Δt_{PLH}	A	Y1		30	57	130	30	57	120	ps/pF
Δt_{PHL}				30	60	150	30	60	130	
Δt_{PZH}	GZ	Y1		30	60	130	30	60	120	ps/pF
Δt_{PZL}				30	65	170	30	65	150	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER§	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5203			SN74ASC5203			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Y1	Y2	C_L = 0	3	6	14.6	3.2	6	13.6	ns
t_{PHL}				1.1	1.4	2.2	1.1	1.4	2.1	
t_{PLH}	Y1	Y2	C_L = 1 pF	6.5	13	32	7	13	29	ns
t_{PHL}				1.3	2	3.7	1.4	2	3.4	
Δt_{PLH}	Y1	Y2		3.4	7	17.3	3.7	7	15.2	ns/pF
Δt_{PHL}				0.2	0.6	1.5	0.2	0.6	1.4	

† Propagation delay times are measured from the 44% point of V_I with $t_r = t_f$ = 3 ns (10% and 90%). For CMOS loads, the times end at the 50% point of V_O.

t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
Δt_{PZH} ≡ change in t_{PZH} with load capacitance
Δt_{PZL} ≡ change in t_{PZL} with load capacitance

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Input propagation delay times are measured from the 1.3 V point of V_I and the times end at the 44% point of V_O with $t_r = t_f$ = 2 ns.

DESIGN CONSIDERATIONS

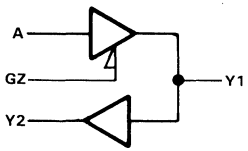
Refer to Section 7.

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

SystemCell™ 2-μm OUTPUT STANDARD CELL

- Typical Propagation Delays
  3.3 ns with 15-pF Load
  5.5 ns with 50-pF Load
- Output Current Ratings
  SN54ASC5206 I_{OL} = 3.4 mA
  I_{OH} = −3.4 mA
  SN74ASC5206 I_{OL} = 4 mA
  I_{OH} = −4 mA
- Incorporates Circuitry to Protect Against ESD and Latch-Up
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol



FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

positive logic equations

Y1 = A Y2 = Y1

description

The SN54ASC5206 and SN74ASC5206 are three-state input/output buffer standard-cells that interface CMOS internal cells with TTL or CMOS bidirectional bus lines. The input buffer responds to CMOS threshold levels imposed on the I/O bus regardless of the state of the internal 3-state control GZ. This cell function exists in two versions (''E'' and ''F'') with different physical implementations to allow the final IC area to be optimized. Since the electrical performance of each version is identical, for simplicity only one version (the ''F'' cell) will be contained in the engineering workstation cell libraries. Determination of the most appropriate cell version will be made during the layout stage. The cell is designated and called from the engineering workstation input using the following cell name and netlist label:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		CELL LAYOUT ASPECT RATIO	RELATIVE CELL AREA TO NA210LH
IOE41LH IOF41LH	Label: IOF41LH A,GZ,Y2,Y1;	minimum height minimum width	49.2 49.4

The cells incorporate circuit elements designed to actively bypass and dissipate electrostatic discharges with potentials ranging up to 4 kilovolts. Guard-ring structures are employed that provide current management techniques for the cell to recover from exposure to high currents of up to 400 milliamperes, thereby negating most common sources that can produce a latch-up condition.

These output cells have been designed to provide low-impedance drive levels for both the high- and low-logic-level states. As a result, passive resistance has been omitted in series with the output transistors. Shorting a high-level output to ground or a low-level output to V_{CC} will cause current flow in excess of that recommended for normal operation. Therefore, it is recommended that outputs not be shorted directly to ground or V_{CC}.

description (continued)

The dynamic drive capability of each output is specified by the delta propagation delay time parameter included with the switching characteristics. The delta propagation delay times provide a means for making direct comparisons of the various outputs response to change in capacitive loading.

The SN54ASC5206 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC5206 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 4 in Section 2. The maximum high-level or maximum low-level output current is 3.4 milliamperes for the SN54ASC5206 and 4 milliamperes for the SN74ASC5206.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54ASC5206			SN74ASC5206			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_T Input threshold voltage	A,GZ	V_{CC} = 5 V, T_A = 25°C		2.2			2.2		V
	Y1			2.5			2.5		
V_{OH} High-level output voltage		I_{OH} = −4 mA				3.7			V
		I_{OH} = −3.4 mA	3.7						
		I_{OH} = −20 μA, See Note 1	V_{CC}−0.1			V_{CC}−0.1			
V_{OL} Low-level output voltage		I_{OL} = 4 mA						0.5	V
		I_{OL} = 3.4 mA			0.5				
		I_{OL} = 20 μA, See Note 1			0.1			0.1	
I_{OZ} Off-state output current		V_O = V_{CC} or 0			±10			±5	μA

NOTE 1: These limits apply when all other outputs are open.

IOE41LH

PARAMETER		TEST CONDITIONS	SN54ASC5206		SN74ASC5206		UNIT
			TYP	MAX	TYP	MAX	
I_{CC} Supply current		V_I = V_{CC} or 0		2755		165	nA
		V_I = 3.5 V or 0.9 V		3.26		2.86	mA
C_i Input capacitance	A	V_{CC} = 5 V, T_A = 25°C	0.6		0.6		pF
	GZ		0.42		0.42		
	Y1†		4.09		4.09		
C_{pd} Equivalent power dissipation capacitance		V_{CC} = 5 V, t_r = t_f = 3 ns, T_A = 25°C	16.7		16.7		pF

IOF41LH

PARAMETER		TEST CONDITIONS	SN54ASC5206		SN74ASC5206		UNIT
			TYP	MAX	TYP	MAX	
I_{CC} Supply current		V_I = V_{CC} or 0		2579		155	nA
		V_I = 3.15 V or 0.9 V		2.96		2.58	mA
C_i Input capacitance	A	V_{CC} = 5 V, T_A = 25°C	0.62		0.62		pF
	GZ		0.44		0.44		
	Y1†		3.83		3.86		
C_{pd} Equivalent power dissipation capacitance		V_{CC} = 5 V, t_r = t_f = 3 ns, T_A = 25°C	14.3		14.3		pF

†Total input capacitance for Y1 is dependent on the package type and is equal to the sum of package capacitance and intrinsic input capacitance.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, C_L = 15 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5206			SN74ASC5206			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y1	R_L = ∞	1.3	2.5	6	1.4	2.5	5.3	ns
t_{PHL}				2.1	4.3	10.2	2.3	4.3	9.1	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.5	3.5	8.4	1.6	3.5	7.6	ns
t_{PZL}	GZ	Y1	R_L = 1 kΩ to V_{CC}	2	4.2	10.4	2.2	4.2	9.2	

TTL loads, C_L = 50 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5206			SN74ASC5206			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y1	R_L = ∞	1.9	3.7	8.9	2	3.7	7.9	ns
t_{PHL}				3.7	7.6	18.4	4	7.6	16.1	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.1	4.6	11.4	2.2	4.6	10.3	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.7	7.8	19.6	4	7.8	17	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		11			11		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		10			10		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5206			SN74ASC5206			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
Δt_{PLH}	A	Y1		20	33	90	20	33	80	ps/pF
Δt_{PHL}				50	98	230	50	98	200	
Δt_{PZH}	GZ	Y1		10	31	90	20	31	80	ps/pF
Δt_{PZL}				50	105	260	50	105	220	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

CMOS loads, C_L = 15 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5206			SN74ASC5206			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y1	R_L = ∞	1.6	3.3	7.6	1.7	3.3	6.8	ns
t_{PHL}				1.8	3.5	8.4	1.9	3.5	7.4	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.1	4.2	9.8	2.3	4.2	8.8	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.7	3.4	8.2	1.8	3.4	7.3	

†Propagation delay times are measured from the 44% point of V_I with $t_r = t_f$ = 3 ns (10% and 90%). For TTL loads, the times end AT V_O = 1.3 V. For CMOS loads, the times end at the 50% point of V_O.

t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
t_{PHZ} ≡ output disable time from high level
t_{PLZ} ≡ output disable time from low level

Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
Δt_{PZH} ≡ change in t_{PZH} with load capacitance
Δt_{PZL} ≡ change in t_{PZL} with load capacitance

‡Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

CMOS loads, C_L = 50 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5206			SN74ASC5206			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y1	R_L = ∞	2.6	5.3	12.5	2.8	5.3	11.2	ns
t_{PHL}				2.8	5.8	14.1	3	5.8	12.4	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	3.1	6.3	15.1	3.3	6.3	13.5	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.8	5.8	14.3	3	5.8	12.5	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5206			SN74ASC5206			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
Δt_{PLH}	A	Y1		30	57	150	30	57	130	ps/pF
Δt_{PHL}				30	66	160	30	66	140	
Δt_{PZH}	GZ	Y1		30	60	160	30	60	140	ps/pF
Δt_{PZL}				30	69	180	30	69	150	

input buffer switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER§	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5206			SN74ASC5206			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Y1	Y2	C_L = 0	0.9	1.8	4.1	1	1.8	3.7	ns
t_{PHL}				1	1.8	3.4	1.1	1.8	3.2	
t_{PLH}	Y1	Y2	C_L = 1 pF	1	2	4.5	1.1	2	4	ns
t_{PHL}				1.1	2	3.8	1.2	2	3.6	
Δt_{PLH}	Y1	Y2		0.1	0.2	0.5	0.1	0.2	0.4	ns/pF
Δt_{PHL}				0.1	0.2	0.5	0.1	0.2	0.4	

† Propagation delay times are measured from the 44% point of V_I with $t_r = t_f$ = 3 ns (10% and 90%). For CMOS loads, the times end at the 50% point of V_O.

t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
Δt_{PZH} ≡ change in t_{PZH} with load capacitance
Δt_{PZL} ≡ change in t_{PZL} with load capacitance

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Input propagation delay times are measured from the 50% point of V_I to the 44% point of V_O with $t_r = t_f$ = 4 ns.

DESIGN CONSIDERATIONS

Refer to Section 7.

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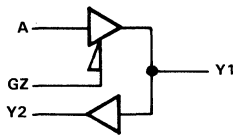
SystemCell™ 2-μm OUTPUT STANDARD CELL

- Typical Propagation Delays
  3.5 ns with 15-pF Load
  5.8 ns with 50-pF Load
- Output Current Ratings
  SN54ASC5207 I_{OL} = 3.4 mA
  I_{OH} = −3.4 mA
  SN74ASC5207 I_{OL} = 4 mA
  I_{OH} = −4 mA
- Incorporates Circuitry to Protect Against ESD and Latch-Up
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol



FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

positive logic equations

Y1 = A Y2 = Y1

description

The SN54ASC5207 and SN74ASC5207 are three-state input/output buffer standard-cells that interface CMOS internal cells with TTL or CMOS bidirectional bus lines. The input buffer responds to TTL threshold levels imposed on the I/O bus regardless of the state of the internal 3-state control GZ. This cell function exists in two versions (''E'' and ''F'') with different physical implementations to allow the final IC area to be optimized. Since the electrical performance of each version is identical, for simplicity only one version (the ''F'' cell) will be contained in the engineering workstation cell libraries. Determination of the most appropriate cell version will be made during the layout stage. The cell is designated and called from the engineering workstation input using the following cell name and netlist label:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		CELL LAYOUT ASPECT RATIO	RELATIVE CELL AREA TO NA210LH
IOE44LH IOF44LH	Label: IOF44LH A,GZ,Y2,Y1;	minimum height minimum width	49.2 52.4

The cells incorporate circuit elements designed to actively bypass and dissipate electrostatic discharges with potentials ranging up to 4 kilovolts. Guard-ring structures are employed that provide current management techniques for the cell to recover from exposure to high currents of up to 400 milliamperes, thereby negating most common sources that can produce a latch-up condition.

These output cells have been designed to provide low-impedance drive levels for both the high- and low-logic-level states. As a result, passive resistance has been omitted in series with the output transistors. Shorting a high-level output to ground or a low-level output to V_{CC} will cause current flow in excess of that recommended for normal operation. Therefore, it is recommended that outputs not be shorted directly to ground or V_{CC}.

description (continued)

The dynamic drive capability of each output is specified by the delta propagation delay time parameter included with the switching characteristics. The delta propagation delay times provide a means for making direct comparisons of the various outputs response to change in capacitive loading.

The SN54ASC5207 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC5207 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 4 in Section 2. The maximum high-level or maximum low-level output current is 3.4 milliamperes for the SN54ASC5207 and 4 milliamperes for the SN74ASC5207.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54ASC5207			SN74ASC5207			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_T Input threshold voltage	A,GZ	V_{CC} = 5 V, T_A = 25°C		2.2			2.2		V
	Y1			1.3			1.3		
V_{OH} High-level output voltage		I_{OH} = −4 mA				3.7			V
		I_{OH} = −3.4 mA	3.7						
		I_{OH} = −20 μA, See Note 1	V_{CC}−0.1			V_{CC}−0.1			
V_{OL} Low-level output voltage		I_{OL} = 4 mA						0.5	V
		I_{OL} = 3.4 mA			0.5				
		I_{OL} = 20 μA, See Note 1			0.1			0.1	
I_{OZ} Off-state output current		V_O = V_{CC} or 0			±10			±5	μA

NOTE 1: These limits apply when all other outputs are open.

IOE44LH

PARAMETER		TEST CONDITIONS	SN54ASC5207		SN74ASC5207		UNIT
			TYP	MAX	TYP	MAX	
I_{CC} Supply current		V_I = V_{CC} or 0		2611		157	nA
		V_I = 2 V or 0.8 V		1.17		1.1	mA
C_i Input capacitance	A	V_{CC} = 5 V, T_A = 25°C	0.6		0.6		pF
	GZ		0.42		0.42		
	Y1†		4.17		4.17		
C_{pd} Equivalent power dissipation capacitance		V_{CC} = 5 V, t_r = t_f = 3 ns, T_A = 25°C	14.5		14.5		pF

IOF44LH

PARAMETER		TEST CONDITIONS	SN54ASC5207		SN74ASC5207		UNIT
			TYP	MAX	TYP	MAX	
I_{CC} Supply current		V_I = V_{CC} or 0		2725		163	nA
		V_I = 2 V or 0.8 V		1.2		1.12	mA
C_i Input capacitance	A	V_{CC} = 5 V, T_A = 25°C	0.6		0.6		pF
	GZ		0.48		0.48		
	Y1†		4.23		4.23		
C_{pd} Equivalent power dissipation capacitance		V_{CC} = 5 V, t_r = t_f = 3 ns, T_A = 25°C	14.3		14.3		pF

†Total input capaciatance for the Y1 input is dependent on the package type and is equal to the sum of package capacitance and intrinsic input capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, C_L = 15 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5207			SN74ASC5207			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y1	R_L = ∞	1.3	2.5	5.9	1.4	2.5	5.2	ns
t_{PHL}				2.1	4.5	11.1	2.2	4.5	9.9	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.5	3.4	8.4	1.7	3.4	7.6	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2	4.4	11.3	2.2	4.4	9.9	

TTL loads, C_L = 50 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5207			SN74ASC5207			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y1	R_L = ∞	1.9	3.7	8.9	2	3.7	7.9	ns
t_{PHL}				3.7	8	20.3	4	8	17.7	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.1	4.6	11.4	2.2	4.6	10.2	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.7	8	21.8	4.1	8	18.8	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		11			11		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		10			10		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5207			SN74ASC5207			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
Δt_{PLH}	A	Y1		10	34	80	20	34	70	ps/pF
Δt_{PHL}				50	100	260	60	100	220	
Δt_{PZH}	GZ	Y1		10	34	80	20	34	80	ps/pF
Δt_{PZL}				50	103	300	50	103	250	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

CMOS loads, C_L = 15 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5207			SN74ASC5207			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y1	R_L = ∞	1.6	3.2	7.5	1.7	3.2	6.7	ns
t_{PHL}				1.8	3.6	9.1	1.9	3.6	8.1	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.1	4.2	9.8	2.3	4.2	8.7	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.7	3.5	8.8	1.8	3.5	7.8	

† Propagation delay times are measured from the 44% point of V_I with $t_r = t_f$ = 3 ns (10% and 90%). For TTL loads, the times end at V_O = 1.3 V. For CMOS loads, the times end at the 50% point of V_O.

t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
Δt_{PZH} ≡ change in t_{PZH} with load capacitance
Δt_{PZL} ≡ change in t_{PZL} with load capacitance

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

CMOS loads, C_L = 50 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5207			SN74ASC5207			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.6	5.3	12.3	2.6	5.3	11	ns
t_{PHL}				2.8	6	15.4	3	6	13.5	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	3.1	6.2	14.5	3.4	6.2	13.2	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.8	6.1	15.7	3	6.1	13.7	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5207			SN74ASC5207			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
Δt_{PLH}	A	Y1		30	60	140	30	60	120	ps/pF
Δt_{PHL}				30	57	180	30	57	150	
Δt_{PZH}	GZ	Y1		30	57	140	30	57	120	ps/pF
Δt_{PZL}				30	74	200	30	74	170	

input buffer switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER§	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5207			SN74ASC5207			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Y1	Y2	C_L = 0	0.8	1.4	2.5	0.8	1.4	2.4	ns
t_{PHL}				1.2	2.4	5.5	1.2	2.4	4.9	
t_{PLH}	Y1	Y2	C_L = 1 pF	0.9	1.7	3.3	1	1.7	3	ns
t_{PHL}				1.3	2.7	6.3	1.4	2.7	5.6	
Δt_{PLH}	Y1	Y2		0.1	0.3	0.8	0.1	0.3	0.7	ns/pF
Δt_{PHL}				0.1	0.3	0.9	0.1	0.3	0.8	

† Propagation delay times are measured from the 44% point of V_I with $t_r = t_f$ = 3 ns (10% and 90%). For CMOS loads, the times end at the 50% point of V_O.

t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
Δt_{PZH} ≡ change in t_{PZH} with load capacitance
Δt_{PZL} ≡ change in t_{PZL} with load capacitance

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Input propagation delay times are measured from the 1.3 V point of V_I to the 44% point of V_O with $t_r = t_f$ = 2 ns.

DESIGN CONSIDERATIONS

Refer to Section 7.

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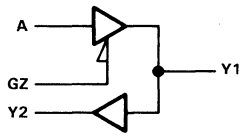
SystemCell™ 2-μm OUTPUT STANDARD CELL

- Typical Propagation Delays
  2.7 ns with 15-pF Load
  4.1 ns with 50-pF Load
- Output Current Ratings
  SN54ASC5217 I_{OL} = 5.1 mA
  I_{OH} = −5.1 mA
  SN74ASC5217 I_{OL} = 6 mA
  I_{OH} = −6 mA
- Incorporates Circuitry to Protect Against ESD and Latch-Up
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol



FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

positive logic equations

Y1 = A Y2 = Y1

description

The SN54ASC5217 and SN74ASC5217 are 3-state input/output buffer standard cells that interface CMOS internal cells with TTL or CMOS bidirectional bus lines. The input buffer responds to TTL threshold levels imposed on the I/O bus regardless of the state of the internal 3-state control GZ. The cell is designated and called from the engineering workstation input using the following cell name and netlist label:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		CELL LAYOUT ASPECT RATIO	RELATIVE CELL AREA TO NA210LH
IOF64LH	Label: IOF64LH A,GZ,Y2,Y1;	minimum width	58.4

The cell incorporates circuit elements designed to actively bypass and dissipate electrostatic discharges with potentials ranging up to 4 kilovolts. Guard-ring structures are employed that provide current management techniques for the cell to recover from exposure to high currents of up to 400 milliamperes, thereby negating most common sources that can produce a latch-up condition.

These output cells have been designed to provide low-impedance drive levels for both the high- and low-logic-level states. As a result, passive resistance has been omitted in series with the output transistors. Shorting a high-level output to ground or a low-level output to V_{CC} will cause current flow in excess of that recommended for normal operation. Therefore, it is recommended that outputs not be shorted directly to ground or V_{CC}.

The dynamic drive capability of each output is specified by the delta propagation delay time parameter included with the switching characteristics. The delta propagation delay times provide a means for making direct comparisons of the various outputs response to change in capacitive loading.

description (continued)

The SN54ASC5217 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC5217 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 4 in Section 2. The maximum high-level or maximum low-level output current is 5.1 milliamperes for the SN54ASC5217 and 6 milliamperes for the SN74ASC5217.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	SN54ASC5217			SN74ASC5217			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_T	Input threshold voltage	A, GZ	V_{CC} = 5 V, T_A = 25°C		2.2			2.2		V
		Y1			1.3			1.3		
V_{OH}	High-level output voltage		I_{OH} = −6 mA				3.7			V
			I_{OH} = −5.1 mA	3.7						
			I_{OH} = −20 μA, See Note 1	V_{CC}−0.1			V_{CC}−0.1			
V_{OL}	Low-level output voltage		I_{OL} = 6 mA						0.5	V
			I_{OL} = 5.1 mA			0.5				
			I_{OL} = 20 μA, See Note 1			0.1			0.1	
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	μA
I_{CC}	Supply current		V_I = V_{CC} or 0			3466			208	nA
			V_I = 2 V or 0.8 V			1.21			1.13	mA
C_i	Input capacitance	A	V_{CC} = 5 V, T_A = 25°C		1.03			1.03		pF
		GZ			0.72			0.72		
		Y1†			5.94			5.94		
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, t_r = t_f = 3 ns, T_A = 25°C		22.4			22.4		pF

†Total input capacitance is dependent on the package type and is equal to the sum of package capacitance and intrinsic input capacitance.
NOTE 1: These limits apply when all other outputs are open.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, C_L = 15 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5217			SN74ASC5217			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y1	R_L = ∞	1.1	2	4.5	1.1	2	4	ns
t_{PHL}				1.7	3.5	8.3	1.9	3.5	7.3	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.2	2.8	6.6	1.3	2.8	6	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.6	3.3	7.7	1.8	3.3	6.9	

TTL loads, C_L = 50 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5217			SN74ASC5217			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y1	R_L = ∞	1.4	2.7	6.3	1.5	2.7	5.6	ns
t_{PHL}				2.7	5.6	13.2	2.9	5.6	11.6	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.5	3.5	8.4	1.7	3.5	7.6	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.7	5.5	13.1	2.9	5.5	11.5	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		11			11		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		9			9		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5217			SN74ASC5217			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
Δt_{PLH}	A	Y1		10	20	50	10	20	40	ps/pF
Δt_{PHL}				30	60	140	30	60	120	
Δt_{PZH}	GZ	Y1		10	20	50	10	20	50	ps/pF
Δt_{PZL}				30	63	160	30	63	130	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

CMOS loads, C_L = 15 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5217			SN74ASC5217			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y1	R_L = ∞	1.2	2.5	5.6	1.3	2.5	5.1	ns
t_{PHL}				1.6	3	5.9	1.7	3	6.2	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.7	3.3	7.4	1.8	3.3	6.7	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.5	2.7	6.2	1.5	2.7	5.5	

† Propagation delay times are measured from the 44% point of V_I with t_r = t_f = 3 ns (10% and 90%). For TTL loads, the times end at V_O = 1.3 V. For CMOS loads, the times end at the 50% point of V_O.

t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
t_{PHZ} ≡ output disable time from high level
t_{PLZ} ≡ output disable time from low level

Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
Δt_{PZH} ≡ change in t_{PZH} with load capacitance
Δt_{PZL} ≡ change in t_{PZL} with load capacitance

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

CMOS loads, C_L = 50 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5217			SN74ASC5217			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.8	3.6	8.3	1.9	3.6	7.4	ns
t_{PHL}				2.2	4.4	10.4	2.4	4.4	9.1	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.2	4.4	10.2	2.4	4.4	9.1	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.2	4.2	10	2.3	4.2	8.8	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5217			SN74ASC5217			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
Δt_{PLH}	A	Y1		20	30	80	20	30	70	ps/pF
Δt_{PHL}				20	40	100	20	40	80	
Δt_{PZH}	GZ	Y1		20	30	80	20	30	70	ps/pF
Δt_{PZL}				20	40	110	20	40	90	

input buffer switching characteristics over recommended ranges of supply voltage and free-air temperature (unless otherwise noted)

PARAMETER§	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5217			SN74ASC5217			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Y1	Y2	C_L = 0	0.8	1.4	2.4	0.8	1.4	2.4	ns
t_{PHL}				1.3	2.4	5.5	1.3	2.4	4.9	
t_{PLH}	Y1	Y2	C_L = 1 pF	1	1.7	3.3	1	1.7	3	ns
t_{PHL}				1.4	2.7	6.4	1.5	2.7	5.6	
Δt_{PLH}	Y1	Y2		0.1	0.3	0.8	0.1	0.3	0.7	ns/pF
Δt_{PHL}				0.1	0.3	0.9	0.1	0.3	0.8	

†Propagation delay times are measured from the 44% point of V_I with $t_r = t_f$ = 3 ns (10% and 90%). For CMOS loads, the times end at the 50% point of V_O.

t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
Δt_{PZH} ≡ change in t_{PZH} with load capacitance
Δt_{PZL} ≡ change in t_{PZL} with load capacitance

‡Typical values are at V_{CC} = 5 V, T_A = 25°C.

§Input propagation delay times are measured from the 1.3 V point of V_I and the times end at the 44% point of V_O with $t_r = t_f$ = 2 ns.

DESIGN CONSIDERATIONS

Refer to Section 7.

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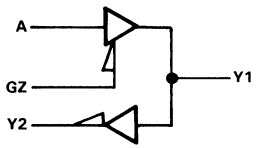
SystemCell™ 2-μm OUTPUT STANDARD CELL

- **Typical Propagation Delays**
  2.9 ns with 15-pF Load
  3.8 ns with 50-pF Load
- **Output Current Ratings**
  SN54ASC5220 I_{OL} = 8.5 mA
  I_{OH} = −8.5 mA
  SN74ASC5220 I_{OL} = 10 mA
  I_{OH} = −10 mA
- **Incorporates Circuitry to Protect Against ESD and Latch-Up**
- **Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V**
- **Functional Operation Over V_{CC} Range of 2 V to 6 V**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol



FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	H
H	L	H	H	L
X	H	L	Z	H
X	H	H	Z	L

positive logic equations

$Y1 = A \qquad Y2 = \overline{Y1}$

description

The SN54ASC5220 and SN74ASC5220 are 3-state input/output buffer standard-cells that interface CMOS internal cells with TTL or CMOS bidirectional bus lines. The input buffer responds to CMOS threshold levels imposed on the I/O bus regardless of the state of the internal 3-state control GZ. This cell function exists in two versions ("E" and "F") with different physical implementations to allow the final IC area to be optimized. Since the electrical performance of each version is identical, for simplicity only one version (the "F" cell) will be contained in the engineering workstation cell libraries. Determination of the most appropriate cell version will be made during the layout stage. The cell is designated and called from the engineering workstation input using the following cell name and netlist label:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		CELL LAYOUT ASPECT RATIO	RELATIVE CELL AREA TO NA210LH
IOE00LH IOF00LH	Label: IOF00LH A,GZ,Y2,Y1;	minimum height minimum width	69 62.9

The cells incorporate circuit elements designed to actively bypass and dissipate electrostatic discharges with potentials ranging up to 4 kilovolts. Guard-ring structures are employed that provide current management techniques for the cell to recover from exposure to high currents of up to 400 milliamperes, thereby negating most common sources that can produce a latch-up condition.

These output cells have been designed to provide low-impedance drive levels for both the high- and low-logic-level states. As a result, passive resistance has been omitted in series with the output transistors. Shorting a high-level output to ground or a low-level output to V_{CC} will cause current flow in excess of that recommended for normal operation. Therefore, it is recommended that outputs not be shorted directly to ground or V_{CC}.

description (continued)

The dynamic drive capability of each output is specified by the delta propagation delay time parameter included with the switching characteristics. The delta propagation delay times provide a means for making direct comparisons of the various outputs response to change in capacitive loading.

The SN54ASC5220 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC5220 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 4 in Section 2. The maximum high-level or maximum low-level output current is 8.5 milliamperes for the SN54ASC5220 and 10 milliamperes for the SN74ASC5220.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54ASC5220			SN74ASC5220			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_T Input threshold voltage	A,GZ	V_{CC} = 5 V, T_A = 25°C		2.2			2.2		V
	Y1			2.5			2.5		
V_{OH} High-level output voltage		I_{OH} = −10 mA				3.7			V
		I_{OH} = −8.5 mA	3.7						
		I_{OH} = −20 μA, See Note 1	V_{CC}−0.1			V_{CC}−0.1			
V_{OL} Low-level output voltage		I_{OL} = 10 mA						0.5	V
		I_{OL} = 8.5 mA			0.5				
		I_{OL} = 20 μA, See Note 1			0.1			0.1	
I_{OZ} Off-state output current		V_O = V_{CC} or 0			±10			±5	μA

NOTE 1: These limits apply when all other outputs are open.

IOE00LH

PARAMETER		TEST CONDITIONS	SN54ASC5220		SN74ASC5220		UNIT
			TYP	MAX	TYP	MAX	
I_{CC} Supply current		V_I = V_{CC} or 0		4660		280	nA
		V_I = 3.15 V pr 0.9 V	4.33		4.09		mA
C_i Input capacitance	A	V_{CC} = 5 V, T_A = 25°C	1.24		1.24		pF
	GZ		0.73		0.73		
	Y1†		7.53		7.53		
C_{pd} Equivalent power dissipation capacitance		V_{CC} = 5 V, t_r = t_f = 3 ns, T_A = 25°C	31.4		31.4		pF

IOF00LH

PARAMETER		TEST CONDITIONS	SN54ASC5220		SN74ASC5220		UNIT
			TYP	MAX	TYP	MAX	
I_{CC} Supply current		V_I = V_{CC} or 0		3724		233	nA
		V_I = 3.15 V or 0.9 V	4.37		4.14		mA
C_i Input capacitance	A	V_{CC} = 5 V, T_A = 25°C	1.03		1.03		pF
	GZ		0.77		0.77		
	Y1†		7.11		7.11		
C_{pd} Equivalent power dissipation capacitance		V_{CC} = 5 V, t_r = t_f = 3 ns, T_A = 25°C	25.8		25.8		pF

†Total input capacitance for Y1 is dependent on the package type and is equal to the sum of package capacitance and intrinsic input capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, C_L = 15 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5220			SN74ASC5220			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y1	R_L = ∞	1.2	2.2	5.1	1.2	2.2	4.6	ns
t_{PHL}				1.7	3.6	8.5	1.8	3.6	7.6	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.3	3	7.3	1.4	3	6.6	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.6	3.3	7.4	1.7	3.3	6.8	

TTL loads, C_L = 50 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5220			SN74ASC5220			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y1	R_L = ∞	1.5	2.8	6.7	1.6	2.8	6	ns
t_{PHL}				2.3	4.8	11.3	2.5	4.8	10.1	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.6	3.7	8.9	1.7	3.7	8	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.2	4.6	11.1	2.4	4.6	9.8	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		10			10		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		9			9		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5220			SN74ASC5220			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
Δt_{PLH}	A	Y1		10	20	50	10	20	40	ps/pF
Δt_{PHL}				10	35	90	20	35	80	
Δt_{PZH}	GZ	Y1		10	20	50	10	20	40	ps/pF
Δt_{PZL}				20	40	100	20	40	90	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

CMOS loads, C_L = 15 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5220			SN74ASC5220			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y1	R_L = ∞	1.3	2.6	6.2	1.4	2.6	5.6	ns
t_{PHL}				1.5	3.1	7.4	1.6	3.1	6.6	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.7	3.4	8.1	1.8	3.4	7.3	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.5	2.8	6.2	1.5	2.8	5.6	

† Propagation delay times are measured from the 44% point of V_I with $t_r = t_f$ = 3 ns (10% and 90%). For TTL loads, the times end at V_O = 1.3 V. For CMOS loads, the times end at the 50% point of V_O.

t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
t_{PHZ} ≡ output disable time from high level
t_{PLZ} ≡ output disable time from low level

Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
Δt_{PZH} ≡ change in t_{PZH} with load capacitance
Δt_{PZL} ≡ change in t_{PZL} with load capacitance

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

CMOS loads, C_L = 50 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5220			SN74ASC5220			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.8	3.6	8.5	1.9	3.6	7.6	ns
t_{PHL}				2	4	9.5	2.1	4	8.4	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.2	4.5	10.4	2.4	4.5	9.3	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2	3.8	8.9	2.1	3.8	7.9	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5220			SN74ASC5220			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
Δt_{PLH}	A	Y1		10	30	70	10	30	60	ps/pF
Δt_{PHL}				10	25	70	10	25	60	
Δt_{PZH}	GZ	Y1		10	30	70	10	30	70	ps/pF
Δt_{PZL}				10	30	80	20	30	70	

input buffer switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER§	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5220			SN74ASC5220			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Y1	Y2	C_L = 0	0.5	0.8	1.3	0.5	0.8	1.3	ns
t_{PHL}				0.2	0.7	1.6	0.3	0.7	1.5	
t_{PLH}	Y1	Y2	C_L = 1 pF	0.7	1.1	2	0.7	1.1	1.9	ns
t_{PHL}				0.5	1.1	2.4	0.6	1.1	2.8	
Δt_{PLH}	Y1	Y2		0.2	0.3	0.7	0.2	0.3	0.6	ns/pF
Δt_{PHL}				0.2	0.4	0.8	0.2	0.4	0.8	

† Propagation delay times are measured from the 44% point of V_I with $t_r = t_f$ = 3 ns (10% and 90%). For CMOS loads, the times end at the 50% point of V_O.

t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level

Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
Δt_{PZH} ≡ change in t_{PZH} with load capacitance
Δt_{PZL} ≡ change in t_{PZL} with load capacitance

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Input propagation delay times are measured from the 50% point of V_I to the 44% point of V_O with $t_r = t_f$ = 4 ns.

DESIGN CONSIDERATIONS

Refer to Section 7.

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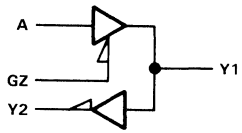
SystemCell™ 2-μm OUTPUT STANDARD CELL

- Typical Propagation Delays
  2.7 ns with 15-pF Load
  3.8 ns with 50-pF Load
- Output Current Ratings
  SN54ASC5221 I_{OL} = 8.5 mA
  I_{OH} = −8.5 mA
  SN74ASC5221 I_{OL} = 10 mA
  I_{OH} = −10 mA
- Incorporates Circuitry to Protect Against ESD and Latch-Up
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol



FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	H
H	L	H	H	L
X	H	L	Z	H
X	H	H	Z	L

positive logic equations

$Y1 = A \qquad Y2 = \overline{Y1}$

description

The SN54ASC5221 and SN74ASC5221 are 3-state input/output buffer standard-cells that interface CMOS internal cells with TTL or CMOS bidirectional bus lines. The input buffer responds to CMOS threshold levels imposed on the I/O bus regardless of the state of the internal 3-state control GZ. The cell is designated and called from the engineering workstation input using the following cell name and netlist label:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		CELL LAYOUT ASPECT RATIO	RELATIVE CELL AREA TO NA210LH
IOF03LH	Label: IOF03LH A,GZ,Y2,Y1;	minimum width	62.9

The cell incorporates circuit elements designed to actively bypass and dissipate electrostatic discharges with potentials ranging up to 4 kilovolts. Guard-ring structures are employed that provide current management techniques for the cell to recover from exposure to high currents of up to 400 milliamperes, thereby negating most common sources that can produce a latch-up condition.

These output cells have been designed to provide low-impedance drive levels for both the high- and low-logic-level states. As a result, passive resistance has been purposely omitted in series with the output transistors. Shorting a high-level output to ground or a low-level output to V_{CC} will cause current flow in excess of that recommended for normal operation. Therefore, it is recommended that outputs not be shorted directly to ground or V_{CC}.

The dynamic drive capability of each output is specified by the delta propagation delay time parameter included with the switching characteristics. The delta propagation delay times provide a means for making direct comparisons of the outputs response to change in capacitive loading.

The SN54ASC5221 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC5221 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 4 in Section 2 and the I_O test conditions shown in the electrical characteristics. Maximum high-level or maximum low-level output current is 8.5 milliamperes for the SN54ASC5221 and 10 milliamperes for the SN74ASC5221.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54ASC5221			SN74ASC5221			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_T Input threshold voltage	A,GZ	V_{CC} = 5 V, T_A = 25°C		2.2			2.2		V
	Y1			2.5			2.5		
V_{OH} High-level output voltage		I_{OH} = −10 mA				3.7			V
		I_{OH} = −8.5 mA	3.7						
		I_{OH} = −20 μA, See Note 1	V_{CC}−0.1			V_{CC}−0.1			
V_{OL} Low-level output voltage		I_{OL} = 10 mA						0.5	V
		I_{OL} = 8.5 mA			0.5				
		I_{OL} = 20 μA, See Note 1			0.1			0.1	
I_{OZ} Off-state output current		V_O = V_{CC} or 0			±10			±5	μA
I_{CC} Supply current		V_I = 2 V or 0.8 V			3658			219	nA
		V_I = V_{CC} or 0			1.21			1.13	mA
C_i Input capacitance	A	V_{CC} = 5 V, T_A = 25°C		1			1		pF
	GZ			0.77			0.77		
	Y1†			6.46			6.46		
C_{pd} Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C, t_r = t_f = 3 ns,		24.4			24.4		pF

†Total input capacitance is dependent on the package type and is equal to the sum of package capacitance and intrinsic input capacitance.
NOTE 1: These limits apply when all other outputs are open.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, C_L = 15 pF

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5221			SN74ASC5221			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
t_{PLH}	A	Y1	R_L = ∞	1.1	2.1	4.8	1.2	2.1	4.3	ns
t_{PHL}				1.7	3.4	8	1.8	3.4	7.1	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.3	2.8	6.8	1.4	2.8	6.2	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.6	3.2	7.4	1.7	3.2	6.7	

‡Propagation delay times are measured from the 44% point of V_I with t_r = t_f = 3 ns (10% and 90%). For TTL loads, the times end at V_O = 1.3 V.
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
§Typical values are at V_{CC} = 5 V, T_A = 25°C.

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switching characteristics over recommended ranges of suply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, C_L = 50 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5221			SN74ASC5221			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y1	R_L = ∞	1.5	2.7	6.4	1.6	2.7	5.7	ns
t_{PHL}				2.3	4.8	11.4	2.5	4.8	10.1	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.6	3.5	8.6	1.7	3.5	7.7	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.3	4.8	11.1	2.5	4.8	9.9	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		10			10		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		9			9		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5221			SN74ASC5221			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
Δt_{PLH}	A	Y1		10	20	50	10	20	40	ps/pF
Δt_{PHL}				20	40	100	20	40	80	
Δt_{PZH}	GZ	Y1		10	20	50	10	20	40	ps/pF
Δt_{PZL}				20	46	110	20	46	90	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

CMOS loads, C_L = 15 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5221			SN74ASC5221			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y1	R_L = ∞	1.3	2.5	5.9	1.4	2.5	5.3	ns
t_{PHL}				1.5	3	6.9	1.6	3	6.1	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.7	3.3	7.6	1.8	3.3	6.8	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.5	2.7	6.1	1.5	2.7	5.5	

CMOS loads, C_L = 50 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5221			SN74ASC5221			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y1	R_L = ∞	1.8	3.6	8.4	1.9	3.6	7.5	ns
t_{PHL}				2	4	9.4	2.1	4	8.3	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.2	4.4	10.2	2.4	4.4	9.2	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2	3.9	9	2.1	3.9	8	

† Propagation delay times are measured from the 44% point of V_I with $t_r = t_f$ = 3 ns (10% and 90%). For TTL loads, the times end at V_O = 1.3 V. For CMOS loads, the times end at 50% point of V_O.

t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
t_{PHZ} ≡ output disable time from high level
t_{PLZ} ≡ output disable time from low level

Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
Δt_{PZH} ≡ change in t_{PZH} with load capacitance
Δt_{PZL} ≡ change in t_{PZL} with load capacitance

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5221			SN74ASC5221			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
Δt_{PLH}	A	Y1		10	31	70	20	31	60	ps/pF
Δt_{PHL}				10	29	70	10	29	60	
Δt_{PZH}	GZ	Y1		10	31	70	20	31	70	ps/pF
Δt_{PZL}				20	34	80	20	34	70	

input buffer switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER§	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5221			SN74ASC5221			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Y1	Y2	C_L = 0	0.7	1	2.3	0.7	1	2	ns
t_{PHL}				0.5	0.9	1.4	0.5	0.9	1.4	
t_{PLH}	Y1	Y2	C_L = 1 pF	1.7	2.9	6.4	1.8	2.9	5.7	ns
t_{PHL}				0.8	1.3	2.2	0.8	1.3	2.1	
Δt_{PLH}	Y1	Y2		1	1.9	4.1	1	1.9	3.8	ns/pF
Δt_{PHL}				0.3	0.4	0.9	0.3	0.4	0.8	

† Propagation delay times are measured from the 44% point of V_I with $t_r = t_f$ = 3 ns (10% and 90%). For CMOS loads, the times end at the 50% point of V_O.
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
Δt_{PZH} ≡ change in t_{PZH} with load capacitance
Δt_{PZL} ≡ change in t_{PZL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Input propagation delay times are measured from the 50% point of V_I to the 44% point of V_O with $t_r = t_f$ = 4 ns.

DESIGN CONSIDERATIONS

Refer to Section 7.

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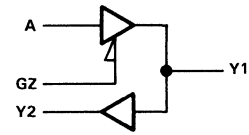
SystemCell™ 2-μm OUTPUT STANDARD CELL

- **Typical Propagation Delays**
  2.7 ns with 15-pF Load
  3.8 ns with 50-pF Load
- **Output Current Ratings**
  SN54ASC5226 I_{OL} = 8.5 mA
  I_{OH} = −8.5 mA
  SN74ASC5226 I_{OL} = 10 mA
  I_{OH} = −10 mA
- **Incorporates Circuitry to Protect Against ESD and Latch-Up**
- **Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V**
- **Functional Operation Over V_{CC} Range of 2 V to 6 V**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol



FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

positive logic equations

$Y1 = A \qquad Y2 = Y1$

description

The SN54ASC5226 and SN74ASC5226 are three-state input/output buffer standard-cells that interface CMOS internal cells with TTL or CMOS bidirectional bus lines. The input buffer responds to CMOS threshold levels imposed on the I/O bus regardless of the state of the internal 3-state control GZ. This cell is designated and called from the engineering workstation input using the following cell name and netlist label:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		CELL LAYOUT ASPECT RATIO	RELATIVE CELL AREA TO NA210LH
IOF01LH	Label: IOF01LH A,GZ,Y2,Y1;	minimum width	64.4

The cells incorporate circuit elements designed to actively bypass and dissipate electrostatic discharges with potentials ranging up to 4 kilovolts. Guard-ring structures are employed that provide current management techniques for the cell to recover from exposure to high currents of up to 400 milliamperes, thereby negating most common sources that can produce a latch-up condition.

These output cells have been designed to provide low-impedance drive levels for both the high- and low-logic-level states. As a result, passive resistance has been omitted in series with the output transistors. Shorting a high-level output to ground or a low-level output to V_{CC} will cause current flow in excess of that recommended for normal operation. Therefore, it is recommended that outputs not be shorted directly to ground or V_{CC}.

The dynamic drive capability of each output is specified by the delta propagation delay time parameter included with the switching characteristics. The delta propagation delay times provide a means for making direct comparisons of the various outputs response to change in capacitive loading.

The SN54ASC5226 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC5226 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 4 in Section 2. The maximum high-level or maximum low-level output current is 8.5 milliamperes for the SN54ASC5226 and 10 milliamperes for the SN74ASC5226.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54ASC5226			SN74ASC5226			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_T Input threshold voltage	A,GZ	V_{CC} = 5 V, T_A = 25°C		2.2			2.2		V
	Y1			2.5			2.5		
V_{OH} High-level output voltage		I_{OH} = −10 mA				3.7			V
		I_{OH} = −8.5 mA	3.7						
		I_{OH} = −20 μA, See Note 1	V_{CC}−0.1			V_{CC}−0.1			
V_{OL} Low-level output voltage		I_{OL} = 10 mA						0.5	V
		I_{OL} = 8.5 mA			0.5				
		I_{OL} = 20 μA, See Note 1			0.1			0.1	
I_{OZ} Off-state output current		V_O = V_{CC} or 0			±10			±5	μA
I_{CC} Supply current		V_I = V_{CC} or 0			3843			231	nA
		V_I = 3.15 V or 0.9 V			2.92			2.51	mA
C_i Input capacitance	A	V_{CC} = 5 V, T_A = 25°C		1.04			1.04		pF
	GZ			0.76			0.76		
	Y1†			6.07			6.07		
C_{pd} Equivalent power dissipation capacitance		V_{CC} = 5 V, t_r = t_f = 3 ns, T_A = 25°C		26.6			26.6		pF

†Total input capaciatance for the Y1 input is dependent on the package type and is equal to the sum of package capacitance and intrinsic input capacitance.

NOTE 1: These limits apply when all other outputs are open.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, C_L = 15 pF

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5226			SN74ASC5226			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
t_{PLH}	A	Y1	R_L = ∞	1.1	2.1	4.7	1.2	2.1	4.2	ns
t_{PHL}				1.7	3.4	7.9	1.8	3.4	7.1	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.3	2.8	6.8	1.4	2.8	6.1	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.6	3.2	7.3	1.7	3.2	6.6	

‡Propagation delay times are measured from the 44% point of V_I with t_r = t_f = 3 ns (10% and 90%). For TTL loads, the times end at V_O = 1.3 V.

t_{PLH} ≡ propagation delay time, low-to-high-level output

t_{PHL} ≡ propagation delay time, high-to-low-level output

t_{PZH} ≡ output enable time to high level

t_{PZL} ≡ output enable time to low level

§Typical values are at V_{CC} = 5 V, T_A = 25°C.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, C_L = 50 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5226			SN74ASC5226			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y1	R_L = ∞	1.4	2.7	6.4	1.5	2.7	5.7	ns
t_{PHL}				2.3	4.8	11.3	2.5	4.8	10.1	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.6	3.5	8.5	1.7	3.5	7.7	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.3	4.8	11.1	2.5	4.8	9.9	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		10			10		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		9			9		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5226			SN74ASC5226			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
Δt_{PLH}	A	Y1		10	17	50	10	17	40	ps/pF
Δt_{PHL}				20	40	100	20	40	80	
Δt_{PZH}	GZ	Y1		10	20	50	10	20	40	ps/pF
Δt_{PZL}				20	46	110	20	46	90	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

CMOS loads, C_L = 15 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5226			SN74ASC5226			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y1	R_L = ∞	1.3	2.5	5.8	1.4	2.5	5.2	ns
t_{PHL}				1.5	3	6.8	1.6	3	6.1	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.7	3.3	7.5	1.8	3.3	6.8	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.4	2.7	6.1	1.5	2.7	5.5	

† Propagation delay times are measured from the 44% point of V_I with $t_r = t_f$ = 3 ns (10% and 90%). For TTL loads, the times end at V_O = 1.3 V. For CMOS loads, the times end at the 50% point of V_O.

t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
t_{PHZ} ≡ output disable time from high level
t_{PLZ} ≡ output disable time from low level

Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
Δt_{PZH} ≡ change in t_{PZH} with load capacitance
Δt_{PZL} ≡ change in t_{PZL} with load capacitance

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

CMOS loads, CL = 50 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5226			SN74ASC5226			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.8	3.6	8.3	1.9	3.6	7.5	ns
t_{PHL}				2	4	9.3	2.1	4	8.3	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.2	4.4	10.1	2.4	4.4	9.1	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2	3.9	8.9	2.1	3.9	8	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5226			SN74ASC5226			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
Δt_{PLH}	A	Y1		10	31	70	20	31	60	ps/pF
Δt_{PHL}				10	29	70	10	29	60	
Δt_{PZH}	GZ	Y1		10	31	80	20	31	70	ps/pF
Δt_{PZL}				20	34	80	20	34	70	

input buffer switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER§	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5226			SN74ASC5226			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Y1	Y2	$C_L = 0$	0.9	1.8	3.8	1	1.8	3.5	ns
t_{PHL}				1.1	1.8	3.5	1.1	1.8	3.2	
t_{PLH}	Y1	Y2	C_L = 1 pF	1	2	4.2	1.1	2	3.8	ns
t_{PHL}				1.2	2	3.8	1.2	2	3.6	
Δt_{PLH}	Y1	Y2		0.1	0.2	0.5	0.1	0.2	0.4	ns/pF
Δt_{PHL}				0.1	0.2	0.5	0.1	0.2	0.4	

† Propagation delay times are measured from the 44% point of V_I with $t_r = t_f$ = 3 ns (10% and 90%). For CMOS loads, the times end at the 50% point of V_O.

t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level

Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
Δt_{PZH} ≡ change in t_{PZH} with load capacitance
Δt_{PZL} ≡ change in t_{PZL} with load capacitance

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Input propagation delay times are measured from the 50% point of V_I to the 44% point of V_O with $t_r = t_f$ = 4 ns.

DESIGN CONSIDERATIONS

Refer to Section 7.

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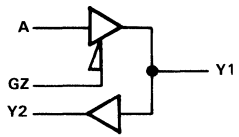
SystemCell™ 2-μm OUTPUT STANDARD CELL

- Typical Propagation Delays
  2.7 ns with 15-pF Load
  3.8 ns with 50-pF Load
- Output Current Ratings
  SN54ASC5227 I_{OL} = 8.5 mA
  I_{OH} = −8.5 mA
  SN74ASC5227 I_{OL} = 10 mA
  I_{OH} = −10 mA
- Incorporates Circuitry to Protect Against ESD and Latch-Up
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol



FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

positive logic equations

Y1 = A Y2 = Y1

description

The SN54ASC5227 and SN74ASC5227 are three-state input/output buffer standard-cells that interface CMOS internal cells with TTL or CMOS bidirectional bus lines. The input buffer responds to TTL threshold levels imposed on the I/O bus regardless of the state of the internal 3-state control GZ. This cell is designated and called from the engineering workstation input using the following cell name and netlist label.

CELL NAME	NETLIST HDL LABEL	FEATURES	
		CELL LAYOUT ASPECT RATIO	RELATIVE CELL AREA TO NA210LH
IOF04LH	Label: IOF04LH A,GZ,Y2,Y1;	minimum width	62.9

The cells incorporate circuit elements designed to actively bypass and dissipate electrostatic discharges with potentials ranging up to 4 kilovolts. Guard-ring structures are employed that provide current management techniques for the cell to recover from exposure to high currents of up to 400 milliamperes, thereby negating most common sources that can produce a latch-up condition.

These output cells have been designed to provide low-impedance drive levels for both the high- and low-logic-level states. As a result, passive resistance has been omitted in series with the output transistors. Shorting a high-level output to ground or a low-level output to V_{CC} will cause current flow in excess of that recommended for normal operation. Therefore, it is recommended that outputs not be shorted directly to ground or V_{CC}.

The dynamic drive capability of each output is specified by the delta propagation delay time parameter included with the switching characteristics. The delta propagation delay times provide a means for making direct comparisons of the various outputs response to change in capacitive loading.

The SN54ASC5227 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC5227 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 4 in Section 2. The maximum high-level or maximum low-level output current is 8.5 milliamperes for the SN54ASC5227 and 10 milliamperes for the SN74ASC5227.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54ASC5227			SN74ASC5227			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_T Input threshold voltage	A,GZ	V_{CC} = 5 V, T_A = 25°C		2.2			2.2		V
	Y1			1.3			1.3		
V_{OH} High-level output voltage		I_{OH} = −10 mA				3.7			V
		I_{OH} = −8.5 mA	3.7						
		I_{OH} = −20 μA, See Note 1	V_{CC}−0.1			V_{CC}−0.1			
V_{OL} Low-level output voltage		I_{OL} = 10 mA						0.5	V
		I_{OL} = 8.5 mA			0.5				
		I_{OL} = 20 μA, See Note 1			0.1			0.1	
I_{OZ} Off-state output current		V_O = V_{CC} or 0			±10			±5	μA
I_{CC} Supply current		V_I = V_{CC} or 0			3794			228	nA
		V_I = 2 V or 0.8 V			1.19			1.11	mA
C_i Input capacitance	A	V_{CC} = 5 V, T_A = 25°C		1			1		pF
	GZ			0.76			0.76		
	Y1†			6.44			6.44		
C_{pd} Equivalent power dissipation capacitance		V_{CC} = 5 V, t_r = t_f = 3 ns, T_A = 25°C		25.7			25.7		pF

†Total input capaciatance for the Y1 input is dependent on the package type and is equal to the sum of package capacitance and intrinsic input capacitance.

NOTE 1: These limits apply when all other outputs are open.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, C_L = 15 pF

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5227			SN74ASC5227			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
t_{PLH}	A	Y1	R_L = ∞	1.1	2.1	4.8	1.2	2.1	4.2	ns
t_{PHL}				1.7	3.4	7.9	1.8	3.4	7.1	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.3	2.8	6.8	1.4	2.8	6.1	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.6	3.2	7.3	1.7	3.2	6.6	

‡Propagation delay times are measured from the 44% point of V_I with t_r = t_f = 3 ns (10% and 90%). For TTL loads, the times end at V_O = 1.3 V.

t_{PLH} ≡ propagation delay time, low-to-high-level output

t_{PHL} ≡ propagation delay time, high-to-low-level output

t_{PZH} ≡ output enable time to high level

t_{PZL} ≡ output enable time to low level

§Typical values are at V_{CC} = 5 V, T_A = 25°C.

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switching characteristics over recommended ranges of supply voltge and operating free-air temperature (unless otherwise noted)

TTL loads, C_L = 50 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5227			SN74ASC5227			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y1	R_L = ∞	1.5	2.7	6.4	1.5	2.7	5.7	ns
t_{PHL}				2.3	4.8	11.3	2.5	4.8	10.1	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.6	3.5	8.5	1.7	3.5	7.7	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.3	4.7	11.1	2.5	4.7	9.8	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		10			10		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		9			9		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5227			SN74ASC5227			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
Δt_{PLH}	A	Y1		10	17	50	10	17	40	ps/pF
Δt_{PHL}				20	40	100	20	40	80	
Δt_{PZH}	GZ	Y1		10	20	50	10	20	40	ps/pF
Δt_{PZL}				20	43	110	20	43	90	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

CMOS loads, C_L = 15 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5227			SN74ASC5227			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y1	R_L = ∞	1.3	2.5	5.9	1.4	2.5	5.2	ns
t_{PHL}				1.5	3	6.8	1.6	3	6.1	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.7	3.3	7.6	1.8	3.3	6.8	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.4	2.7	6.1	1.5	2.7	5.5	

CMOS loads, CL = 50 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5227			SN74ASC5227			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y1	R_L = ∞	1.8	3.6	8.3	1.9	3.6	7.5	ns
t_{PHL}				2	4	9.3	2.1	4	8.3	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.2	4.4	10.2	2.4	4.4	9.1	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2	3.8	8.9	2.1	3.8	8	

† Propagation delay times are measured from the 44% point of V_I with $t_r = t_f$ = 3 ns (10% and 90%). For TTL loads, the times end at V_O = 1.3 V. For CMOS loads, the times end at the 50% point of V_O.

t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
t_{PHZ} ≡ output disable time from high level
t_{PLZ} ≡ output disable time from low level

Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
Δt_{PZH} ≡ change in t_{PZH} with load capacitance
Δt_{PZL} ≡ change in t_{PZL} with load capacitance

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5227			SN74ASC5227			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
Δt_{PLH}	A	Y1		10	31	70	20	31	60	ps/pF
Δt_{PHL}				10	29	70	10	29	60	
Δt_{PZH}	GZ	Y1		10	31	70	20	31	70	ps/pF
Δt_{PZL}				20	31	80	20	31	70	

input buffer switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER§	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5227			SN74ASC5227			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Y1	Y2	C_L = 0	0.8	1.4	2.6	0.9	1.4	2.4	ns
t_{PHL}				1.3	2.6	5.9	1.4	2.6	5.3	
t_{PLH}	Y1	Y2	C_L = 1 pF	1	1.7	3.3	1	1.7	3.1	ns
t_{PHL}				1.5	2.9	6.8	1.6	2.9	6	
Δt_{PLH}	Y1	Y2		0.1	0.3	0.8	0.1	0.3	0.7	ns/pF
Δt_{PHL}				0.2	0.3	0.9	0.2	0.3	0.8	

† Propagation delay times are measured from the 44% point of V_I with $t_r = t_f$ = 3 ns (10% and 90%). For CMOS loads, the times end at the 50% point of V_O.

t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
Δt_{PZH} ≡ change in t_{PZH} with load capacitance
Δt_{PZL} ≡ change in t_{PZL} with load capacitance

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Input propagation delay times are measured from the 1.3 V point of V_I to the 44% point of V_O with $t_r = t_f$ = 2 ns.

DESIGN CONSIDERATIONS

Refer to Section 7.

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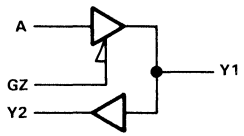
SN54ASC5239, SN74ASC5239
3-STATE I/O BUFFER WITH NONINVERTING TTL INPUT AND CMOS/TTL OUTPUT

D2939, AUGUST 1986

SystemCell™ 2-μm OUTPUT STANDARD CELL

- Typical Propagation Delays
  2.7 ns with 15-pF Load
  3.7 ns with 50-pF Load
- Output Current Ratings
  SN54ASC5239 I_{OL} = 20.4 mA
  I_{OH} = −10.2 mA
  SN74ASC5239 I_{OL} = 24 mA
  I_{OH} = −12 mA
- Incorporates Circuitry to Protect Against ESD and Latch-Up
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol



FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

positive logic equations

$Y1 = A \qquad Y2 = Y1$

description

The SN54ASC5239 and SN74ASC5239 are 3-state input/output buffer standard-cell functions that interface CMOS internal cells with TTL or CMOS bidirectional bus lines. The input buffer responds to TTL threshold levels imposed on the I/O bus regardless of the state of the internal 3-state control GZ. The cell is designated and called from the engineering workstation input using the following cell name and netlist label:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		CELL LAYOUT ASPECT RATIO	RELATIVE CELL AREA TO NA210LH
IOFB8LH	Label: IOFB8LH A,GZ,Y2,Y1;	minimum width	73.4

The cell incorporates circuit elements designed to actively bypass and dissipate electrostatic discharges with potentials ranging up to 4 kilovolts. Guard-ring structures are employed that provide current management techniques for the cell to recover from exposure to high currents of up to 400 milliamperes, thereby negating most common sources that can produce a latch-up condition.

These output cells have been designed to provide low-impedance drive levels for both the high- and low-logic-level states. As a result, passive resistance has been omitted in series with the output transistors. Shorting a high-level output to ground or a low-level output to V_{CC} will cause current flow in excess of that recommended for normal operation. Therefore, it is recommended that outputs not be shorted directly to ground or V_{CC}.

The dynamic drive capability of each output is specified by the delta propagation delay time parameter included with the switching characteristics. The delta propagation delay times provide a means for making direct comparisons of the various output responses with change in capacitive loading.

description (continued)

The SN54ASC5239 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC5239 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 4 in Section 2. The maximum high-level output current is 10.2 milliamperes for the SN54ASC5239 and 12 milliamperes for the SN74ASC5239. The maximum low-level output current is 20.4 milliamperes for the SN54ASC5239 and 24 milliamperes for the SN74ASC5239.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	SN54ASC5239			SN74ASC5239			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_T	Input threshold voltage	A,GZ	V_{CC} = 5 V, T_A = 25°C		2.2			2.2		V
		Y1			1.3			1.3		
V_{OH}	High-level output voltage		I_{OH} = −12 mA				3.7			V
			I_{OH} = −10.2 mA	3.7						
			I_{OH} = −20 μA, See Note 1	V_{CC}−0.1			V_{CC}−0.1			
V_{OL}	Low-level output voltage		I_{OL} = 24 mA						0.5	V
			I_{OL} = 20.4 mA			0.5				
			I_{OL} = 20 μA, See Note 1			0.1			0.1	
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	μA
I_{CC}	Supply current		V_I = V_{CC} or 0			4538			272	nA
			V_I = 2 V or 0.8 V			1.2			1.12	mA
C_i	Input capacitance	A	V_{CC} = 5 V, T_A = 25°C		1.18			1.18		pF
		GZ			0.89			0.89		
		Y1†			7.39			7.39		
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, t_r = t_f = 3 ns, T_A = 25°C		28.2			28.2		pF

†Total input capacitance is dependent on the package type and is equal to the sum of package capacitance and intrinsic input capacitance.
NOTE 1: These limits apply when all other outputs are open.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, C_L = 15 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5239			SN74ASC5239			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y1	R_L = ∞		2.3			2.3		ns
t_{PHL}					3.2			3.2		
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND		2.7			2.7		ns
t_{PZL}			R_L = 1 kΩ to V_{CC}		3			3		

TTL loads, C_L = 50 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5239			SN74ASC5239			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y1	R_L = ∞		2.9			2.9		ns
t_{PHL}					4.2			4.2		
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND		3.4			3.4		ns
t_{PZL}			R_L = 1 kΩ to V_{CC}		4.2			4.2		
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		10			10		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		9			9		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5239			SN74ASC5239			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
Δt_{PLH}	A	Y1			17			17		ps/pF
Δt_{PHL}					29			29		
Δt_{PZH}	GZ	Y1			20			20		ps/pF
Δt_{PZL}					34			34		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

CMOS loads, C_L = 15 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5239			SN74ASC5239			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y1	R_L = ∞		2.7			2.7		ns
t_{PHL}					2.8			2.8		
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND		3.2			3.2		ns
t_{PZL}			R_L = 1 kΩ to V_{CC}		2.6			2.6		

† Propagation delay times are measured from the 44% point of V_I with $t_r = t_f = 3$ ns (10% and 90%). For TTL loads, the times end at V_O = 1.3 V. For CMOS loads, the times end at the 50% point of V_O.

t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
t_{PHZ} ≡ output disable time from high level
t_{PLZ} ≡ output disable time from low level

Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
Δt_{PZH} ≡ change in t_{PZH} with load capacitance
Δt_{PZL} ≡ change in t_{PZL} with load capacitance

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

CMOS loads, C_L = 50 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5239			SN74ASC5239			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y1	$R_L = \infty$		3.7			3.7		ns
t_{PHL}					3.6			3.6		
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND		4.2			4.2		ns
t_{PZL}			R_L = 1 kΩ to V_{CC}		3.5			3.5		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5239			SN74ASC5239			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
Δt_{PLH}	A	Y1			29			29		ps/pF
Δt_{PHL}					23			23		
Δt_{PZH}	GZ	Y1			29			29		ps/pF
Δt_{PZL}					26			26		

input buffer switching characteristics over recommended ranges of supply voltage and free-air temperature (unless otherwise noted)

PARAMETER§	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5239			SN74ASC5239			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Y1	Y2	C_L = 0		1.3			1.3		ns
t_{PHL}					2.4			2.4		
t_{PLH}	Y1	Y2	C_L = 1 pF		1.6			1.6		ns
t_{PHL}					2.7			2.7		
Δt_{PLH}	Y1	Y2			0.3			0.3		ns/pF
Δt_{PHL}					0.3			0.3		

†Propagation delay times are measured from the 44% point of V_I with $t_r = t_f$ = 3 ns (10% and 90%). For CMOS loads, the times end at the 50% point of V_O.

t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
Δt_{PZH} ≡ change in t_{PZH} with load capacitance
Δt_{PZL} ≡ change in t_{PZL} with load capacitance

‡Typical values are at V_{CC} = 5 V, T_A = 25°C.

§Input propagation delay times are measured from the 1.3 V point of V_I to the 44% point of V_O with $t_r = t_f$ = 2 ns.

DESIGN CONSIDERATIONS

Refer to Section 7.

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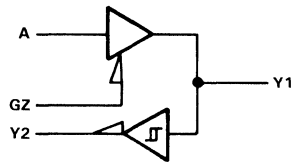
SN54ASC5246, SN74ASC5246 3-STATE I/O BUFFER WITH INVERTING TTL INPUT AND TTL/CMOS OUTPUT

D2939, AUGUST 1986

SystemCell™ 2-μm OUTPUT STANDARD CELL

- Typical Propagation Delays
  2.5 ns with 15-pF Load
  3 ns with 50-pF Load
- Output Current Ratings
  SN54ASC5246 I_{OL} = 37.4 mA
  I_{OH} = −10.2 mA
  SN74ASC5246 I_{OL} = 44 mA
  I_{OH} = −12 mA
- Incorporates Circuitry to Protect Against ESD and Latch-Up
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol



FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	H
H	L	H	H	L
X	H	L	Z	H
X	H	H	Z	L

positive logic equations

$Y = A \qquad Y2 = \overline{Y1}$

description

The SN54ASC5246 and SN74ASC5246 are 3-state input/output buffer standard cells that interface CMOS internal cells with TTL or CMOS bidirectional bus lines. The Schmitt-trigger input buffer, providing additional noise-rejection with its hysteresis loop, responds to TTL threshold levels imposed on the I/O bus regardless of the state of the internal 3-state control GZ. The cell is designated and called from the engineering workstation input using the following cell name and netlist label:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		CELL LAYOUT ASPECT RATIO	RELATIVE CELL AREA TO NA210LH
IOFD8LH	Label: IOFD8LH A,GZ,Y2,Y1;	minimum width	54

The cell incorporates circuit elements designed to actively bypass and dissipate electrostatic discharges with potentials ranging up to 4 kilovolts. Guard-ring structures are employed that provide current management techniques for the cell to recover from exposure to high currents of up to 400 milliamperes, thereby negating most common sources that can produce a latch-up condition.

These output cells have been designed to provide low-impedance drive levels for both the high- and low-logic-level states. As a result, passive resistance has been omitted in series with the output transistors. Shorting a high-level output to ground or a low-level output to V_{CC} will cause current flow in excess of that recommended for normal operation. Therefore, it is recommended that outputs not be shorted directly to ground or V_{CC}.

The dynamic drive capability of each output is specified by the delta propagation delay time parameter included with the switching characteristics. The delta delay times provide a means for making direct comparisons of the various output responses to change in capacitive loading.

description (continued)

The SN54ASC5246 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC5246 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 4 in Section 2. The maximum high-level output current is 10.2 milliamperes for the SN54ASC5246 and 12 milliamperes for the SN74ASC5246. The maximum low-level output current is 37.4 milliamperes for the SN54ASC5246 and 44 milliamperes for the SN74ASC5246.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	SN54ASC5246			SN74ASC5246			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_T	Input threshold voltage at A, GZ		V_{CC} = 5 V, T_A = 25°C	2.2			2.2			V
V_{T+}	Positive-going threshold level (Y1)			1.5	1.7	2	1.5	1.7	2	V
V_{T-}	Negative-going threshold level (Y1)			0.6	0.9	1.1	0.6	0.9	1.1	V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)				0.8			0.8		V
V_{OH}	High-level output voltage		I_{OH} = −12 mA				3.7			V
			I_{OH} = −10.2 mA	3.7						
			I_{OH} = −20 μA, See Note 1	V_{CC}−0.1			V_{CC}−0.1			
V_{OL}	Low-level output voltage		I_{OL} = 44 mA						0.5	V
			I_{OL} = 37.4 mA			0.5				
			I_{OL} = 20 μA, See Note 1			0.1			0.1	
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	μA
I_{CC}	Supply current		V_I = 2 V or 0.6 V			1.45			1.35	mA
			V_I = V_{CC} or 0			6300			378	nA
C_i	Input capacitance	A	V_{CC} = 5 V, T_A = 25°C		1.84			1.84		pF
		GZ			1.51			1.51		
		Y1†			8.79			8.79		
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, t_r = t_f = 3 ns, T_A = 25°C		50.8			50.8		pF

†Total input capacitance for Y1 is dependent on the package type and is equal to the sum of package capacitance and intrinsic input capacitance.

NOTE 1: These limits apply when all other outputs are open.

TEXAS INSTRUMENTS
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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, C_L = 15 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5246			SN74ASC5246			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y1	R_L = ∞		2.3			2.3		ns
t_{PHL}					2.5			2.5		
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND		3			3		ns
t_{PZL}			R_L = 1 kΩ to V_{CC}		2.2			2.2		

TTL loads, C_L = 50 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5246			SN74ASC5246			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y1	R_L = ∞		2.8			2.8		ns
t_{PHL}					3			3		
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND		3.6			3.6		ns
t_{PZL}			R_L = 1 kΩ to V_{CC}		2.8			2.8		
t_{PHZ}			R_L = 1 kΩ to GND		10			10		
t_{PLZ}			R_L = 1 kΩ to V_{CC}		9			9		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5246			SN74ASC5246			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
Δt_{PLH}	A	Y1			15			15		ps/pF
Δt_{PHL}					15			15		
Δt_{PZH}	GZ	Y1			9			9		ps/pF
Δt_{PZL}					17			17		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

CMOS loads, C_L = 15 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5246			SN74ASC5246			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y1	R_L = ∞		2.7			2.7		ns
t_{PHL}					2.2			2.2		
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND		3.5			3.5		ns
t_{PZL}			R_L = 1 kΩ to V_{CC}		2			2		

†Propagation delay times are measured from the 44% point of V_I with $t_r = t_f = 3$ ns (10% and 90%). For TTL loads, the times end at V_O = 1.3 V. For CMOS loads, the times end at the 50% point of V_O.

t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
t_{PHZ} ≡ output disable time from high level
t_{PLZ} ≡ output disable time from low level

Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
Δt_{PZH} ≡ change in t_{PZH} with load capacitance
Δt_{PZL} ≡ change in t_{PZL} with load capacitance

‡Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

CMOS loads, C_L = 50 pF

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5246			SN74ASC5246			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y1	$R_L = \infty$		3.7			3.7		ns
t_{PHL}					2.6			2.6		
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND		4.5			4.5		ns
t_{PZL}			R_L = 1 kΩ to V_{CC}		2.4			2.4		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5246			SN74ASC5246			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
Δt_{PLH}	A	Y1			29			29		ps/pF
Δt_{PHL}					11			11		
Δt_{PZH}	GZ	Y1			29			29		ps/pF
Δt_{PZL}					11			11		

input buffer switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER§	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5246			SN74ASC5246			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Y1	Y2	C_L = 0		7			7		ns
t_{PHL}					1.4			1.4		
t_{PLH}	Y1	Y2	C_L = 1 pF		14			14		ns
t_{PHL}					2			2		
Δt_{PLH}	Y1	Y2			7			7		ns/pF
Δt_{PHL}					0.6			0.6		

†Propagation delay times are measured from the 44% point of V_I with $t_r = t_f$ = 3 ns (10% and 90%). For CMOS loads, the times end at the 50% point of V_O.

t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
Δt_{PZH} ≡ change in t_{PZH} with load capacitance
Δt_{PZL} ≡ change in t_{PZL} with load capacitance

‡Typical values are at V_{CC} = 5 V, T_A = 25°C.

§Input propagation delay times are measured from the 1.3 V point of V_I to the 44% point of V_O with $t_r = t_f$ = 2 ns.

DESIGN CONSIDERATIONS

Refer to Section 7.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

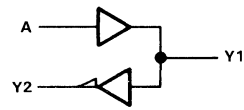
SN54ASC5250, SN74ASC5250
OPEN-DRAIN I/O BUFFER WITH INVERTING CMOS INPUT AND CMOS/TTL OUTPUT

D2939, AUGUST 1986

SystemCell™ 2-μm OUTPUT STANDARD CELL

- Typical Propagation Delays
  1.7 ns with 15-pF Load
  2.3 ns with 50-pF Load
- Output Current Ratings
  SN54ASC5250 I_{OL} = 37.4 mA
  SN74ASC5250 I_{OL} = −44 mA
- Incorporates Circuitry to Protect Against ESD and Latch-Up
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol



FUNCTION TABLE

INPUTS		OUTPUTS	
A	Y1	Y1	Y2
L	L	L	H
H	H	Z	L
H	L	Z	H

positive logic equations

$Y1 = A \qquad Y2 = \overline{Y1}$

description

The SN54ASC5250 and SN74ASC5250 are three-state input/output buffer standard-cells that interface CMOS internal cells with terminated TTL or CMOS bidirectional bus lines. The input buffer responds to CMOS threshold levels imposed on the I/O bus when the internal input A is at a high logic level. The cell is designated and called from the engineering workstation input using the following cell name and netlist label:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		CELL LAYOUT ASPECT RATIO	RELATIVE CELL AREA TO NA210LH
IOFD0LH	Label: IOFD0LH A,Y2,Y1;	minimum width	54

The cell incorporates circuit elements designed to actively bypass and dissipate electrostatic discharges with potentials ranging up to 4 kilovolts. Guard-ring structures are employed that provide current management techniques for the cell to recover from exposure to high currents of up to 400 milliamperes, thereby negating most common sources that can produce a latch-up condition.

These output cells have been designed to provide low-impedance drive levels for low-logic-level outputs interfacing a bus having a terminated high-level drive source. As a result, passive resistance has been omitted in series with the output transistor. Shorting the low-level output to V_{CC} will cause current flow in excess of that recommended for normal operation. Therefore, it is recommended that outputs not be shorted directly to V_{CC}.

The dynamic drive capability of each output is specified by the delta propagation delay time parameter included with the switching characteristics. The delta delay times provide a means for making direct comparisons of the various outputs response to change in capacitive loading.

The SN54ASC5250 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC5250 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 4 in Section 2. The maximum low-level output current is 37.4 milliamperes for SN54ASC5250 and 44 milliamperes for SN74ASC5250.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54ASC5250			SN74ASC5250			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_T Input threshold voltage	A	V_{CC} = 5 V, T_A = 25°C		2.2			2.2		V
	Y1			2.5			2.5		
V_{OL} Low-level output voltage		I_{OL} = 44 mA						0.5	V
		I_{OL} = 37.4 mA			0.5				
		I_{OL} = 20 μA, See Note 1			0.1			0.1	
I_{OZ} Off-state output current		V_O = V_{CC} or 0			±10			±5	μA
I_{CC} Supply current		V_I = V_{CC} or 0			2847			171	nA
		V_I = 3.15 V or 0.9 V			4.3			4.07	mA
C_i Input capacitance	A	V_{CC} = 5 V, T_A = 25°C		0.61			1.19		pF
	Y1†			6			6		
C_{pd} Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C, t_r = t_f = 3 ns		11.6			11.6		pF

†Total input capacitance for Y1 is dependent on the package type and is equal to the sum of package capacitance and intrinsic input capacitance.

NOTE 1: These limits apply when all other outputs are open.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5250			SN74ASC5250			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
t_{PHL}	A	Y1	C_L = 15 pF, R_L = 1 kΩ to V_{CC}		1.7			1.7		ns
t_{PLH}	A	Y1	C_L = 50 pF, R_L = 1 kΩ to V_{CC}		8.5			8.5		ns
t_{PHL}					2.3			2.3		
Δt_{PHL}	A	Y1			17			17		ps/pF

‡Propagation delay times are measured from the 44% point of V_I with t_r = t_f = 3 ns (10% and 90%). For TTL loads the times end at V_O = 1.3 V.

t_{PLH} ≡ propagation delay time, low-to-high-level output

t_{PHL} ≡ propagation delay time, high-to-low-level output

Δt_{PHL} ≡ change in t_{PHL} with load capacitance

§Typical values are at V_{CC} = 5 V, T_A = 25°C.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

CMOS loads

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5250			SN74ASC5250			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PHL}	A	Y1	C_L = 15 pF, R_L = 1 kΩ to V_{CC}		1.5			1.5		ns
t_{PHL}	A	Y1	C_L = 50 pF, R_L = 1 kΩ to V_{CC}		2			2		ns
Δt_{PHL}	A	Y1			14			14		ps/pF

input buffer switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER§	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC5250			SN74ASC5250			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Y1	Y2	C_L = 0		0.6			0.6		ns
t_{PHL}					0.5			0.5		
t_{PLH}	Y1	Y2	C_L = 1 pF		1			1		ns
t_{PHL}					1			1		
Δt_{PLH}	Y1	Y2			0.4			0.4		ns/pF
Δt_{PHL}					0.5			0.5		

† Propagation delay times are measured from the 44% point of V_I with $t_r = t_f$ = 3 ns (10% and 90%). For CMOS loads, the times end at the 50% point of V_O.
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Input propagation delay times are measured from the 50% point of V_I to the 44% point of V_O with $t_r = t_f$ = 4 ns.

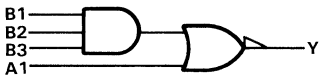
DESIGN CONSIDERATIONS

Refer to Section 7.

SystemCell™ 2-μm INTERNAL STANDARD CELL

- 2.7 ns Typical Propagation Delay with 1-pF Load
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol



FUNCTION TABLE

INPUTS				OUTPUT
A1	B1	B2	B3	Y
H	X	X	X	L
X	H	H	H	L
L	L	X	X	H
L	X	L	X	H
L	X	X	L	H

positive logic equation

$$Y = \overline{A1 + (B1 \cdot B2 \cdot B3)}$$

description

The SN54ASC6002 and SN74ASC6002 are expandable 1-3-input AND-NOR gate CMOS standard cells. The cells are designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		TYPICAL DELAY C_L = 1 pF	RELATIVE CELL AREA TO NA210LH
BF002LH	Label: BF002LH A1,B1,B2,B3,Y;	2.7 ns	1.5

The SN54ASC6002 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6002 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		V
I_{CC} Supply current	SN54ASC6002	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		204	nA
	SN74ASC6002			12.3	
C_i Input capacitance		V_{CC} = 5 V, T_A = 25°C	0.13		pF
C_{pd} Equivalent power dissipation capacitance		V_{CC} = 5 V, t_r = t_f = 3 ns, T_A = 25°C	0.42		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6002			SN74ASC6002			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Any	Y	C_L = 0	0.6	1.2	2.9	0.6	1.2	2.6	ns
t_{PHL}				0.3	1	2.3	0.3	1	2	
t_{PLH}	Any	Y	C_L = 1 pF	1.5	3.2	7.4	1.6	3.2	6.8	ns
t_{PHL}				0.7	2.2	5.7	0.8	2.2	5	
Δt_{PLH}	Any	Y		0.9	2	4.6	1	2	4.1	ns/pF
Δt_{PHL}				0.4	1.2	3.5	0.4	1.2	3	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to the 'ASC6017 data sheet and Section 7.

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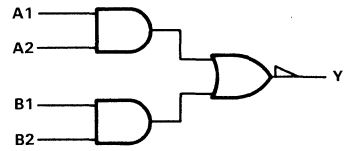
SystemCell™ 2-μm INTERNAL STANDARD CELL

- 2.6 ns Typical Propagation Delay with 1-pF Load
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol



positive logic equation

$$Y = \overline{(A1 \cdot A2) + (B1 \cdot B2)}$$

FUNCTION TABLE

INPUTS				OUTPUT
A1	A2	B1	B2	Y
H	H	X	X	L
X	X	H	H	L
Any other combination				H

description

The SN54ASC6003 and SN74ASC6003 are 2-wide, 2-input AND-OR gate CMOS standard cells. The cells are designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		TYPICAL DELAY C_L = 1 pF	RELATIVE CELL AREA TO NA210LH
BF003LH	Label: BF003LH A1,A2,B1,B2,Y;	2.6 ns	1.75

The SN54ASC6003 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6003 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS		TYP	MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		V
I_{CC}	Supply current	SN54ASC6003	V_{CC} = 4.5 V to 5.5 V,	V_I = V_{CC} or 0,		220	nA
		SN74ASC6003	T_A = MIN to MAX			13.2	
C_i	Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.13		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	$t_r = t_f$ = 3 ns,	0.51		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6003			SN74ASC6003			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Any	Y	C_L = 0	0.7	1.2	2.7	0.7	1.2	2.5	ns
t_{PHL}				0.3	1	2	0.4	1	1.9	
t_{PLH}	Any	Y	C_L = 1 pF	1.6	3.2	7.2	1.7	3.2	6.6	ns
t_{PHL}				0.9	2	4.5	0.9	2	4	
Δt_{PLH}	Any	Y		0.9	2	4.6	1	2	4.2	ns/pF
Δt_{PHL}				0.5	0.9	2.5	0.5	0.9	2.2	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to the 'ASC6017 data sheet and Section 7.

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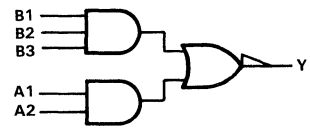
SystemCell™ 2-μm INTERNAL STANDARD CELL

- 2.8 ns Typical Propagation Delay with 1-pF Load
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol



positive logic equation

$$Y = \overline{(A1 \cdot A2) + (B1 \cdot B2 \cdot B3)}$$

FUNCTION TABLE

INPUTS					OUTPUT
A1	A2	B1	B2	B3	Y
H	H	X	X	X	L
X	X	H	H	H	L
Any other combination					H

description

The SN54ASC6004 and SN74ASC6004 are 2-wide, 2-3-input AND-NOR gate CMOS standard cells. The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		TYPICAL DELAY C_L = 1 pF	RELATIVE CELL AREA TO NA210LH
BF004LH	Label: BF004LH A1,A2,B1,B2,B3,Y;	2.8 ns	1.75

The SN54ASC6004 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6004 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		V
I_{CC}	Supply current	SN54ASC6004	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		237	nA
		SN74ASC6004			14.2	
C_i	Input capacitance		V_{CC} = 5 V, T_A = 25°C	0.13		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, $t_r = t_f$ = 3 ns, T_A = 25°C	0.53		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6004			SN74ASC6004			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Any	Y	C_L = 0	0.6	1.3	2.7	0.7	1.3	2.5	ns
t_{PHL}				0.4	1	2.1	0.4	1	1.9	
t_{PLH}	Any	Y	C_L = 1 pF	1.6	3.3	6.4	1.7	3.3	5.9	ns
t_{PHL}				0.9	2.2	5	1	2.2	4.4	
Δt_{PLH}	Any	Y		0.9	2	3.8	1	2	3.5	ns/pF
Δt_{PHL}				0.5	1.2	3	0.5	1.2	2.6	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to the 'ASC6017 data sheet and Section 7.

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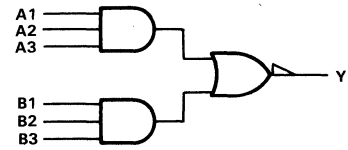
SystemCell™ 2-μm INTERNAL STANDARD CELL

- 3 ns Typical Propagation Delay with 1-pF Load
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol



FUNCTION TABLE

INPUTS						OUTPUT
A1	A2	A3	B1	B2	B3	Y
H	H	H	X	X	X	L
X	X	X	H	H	H	L
Any other combination						H

positive logic equation

$$Y = \overline{(A1 \cdot A2 \cdot A3) + (B1 \cdot B2 \cdot B3)}$$

description

The SN54ASC6005 and SN74ASC6005 are 2-wide, 3-input AND-NOR gate CMOS standard cells. The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		TYPICAL DELAY C_L = 1 pF	RELATIVE CELL AREA TO NA210LH
BF005LH	Label: BF005LH A1,A2,A3,B1,B2,B3,Y;	3 ns	2

The SN54ASC6005 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6005 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER		TEST CONDITIONS		TYP	MAX	UNIT
V_T Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		V
I_{CC} Supply current	SN54ASC6005	V_{CC} = 4.5 V to 5.5 V,	V_I = V_{CC} or 0,		266	nA
	SN74ASC6005	T_A = MIN to MAX			15.9	
C_i Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.13		pF
C_{pd} Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	$t_r = t_f$ = 3 ns,	0.64		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6005			SN74ASC6005			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Any	Y	C_L = 0	0.7	1.5	3.3	0.7	1.5	3.1	ns
t_{PHL}				0.5	1.2	2.4	0.5	1.2	2.1	
t_{PLH}	Any	Y	C_L = 1 pF	1.6	3.5	7.1	1.7	3.5	6.5	ns
t_{PHL}				1.1	2.5	5.2	1.2	2.5	4.5	
Δt_{PLH}	Any	Y		0.9	2	3.8	1	2	3.5	ns/pF
Δt_{PHL}				0.6	1.3	3	0.6	1.3	2.5	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to the 'ASC6017 data sheet and Section 7.

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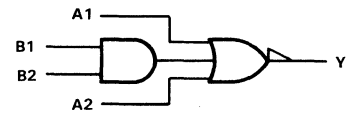
SystemCell™ 2-μm INTERNAL STANDARD CELL

- **Typical Propagation Delay with 1-pF Load**
  3 ns from Any A
  3.2 ns from Any B
- **Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V**
- **Functional Operation Over V_{CC} Range of 2 V to 6 V**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol



FUNCTION TABLE

INPUTS				OUTPUT
A1	A2	B1	B2	Y
H	X	X	X	L
X	H	X	X	L
X	X	H	H	L
L	L	L	X	H
L	L	X	L	H

positive logic equation

$$Y = \overline{A1 + A2 + (B1 \cdot B2)}$$

description

The SN54ASC6006 and SN74ASC6006 are expandable 1-1-2-input AND-NOR gate CMOS standard cells. The cells are designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
BF006LH	Label: BF006LH A1,A2,B1,B2,Y;	1.75

The SN54ASC6006 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6006 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		V
I_{CC} Supply current	SN54ASC6006	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0,		222	nA
	SN74ASC6006	T_A = MIN to MAX		13.3	
C_I Input capacitance		V_{CC} = 5 V, T_A = 25°C	0.13		pF
C_{pd} Equivalent power dissipation capacitance		V_{CC} = 5 V, $t_r = t_f$ = 3 ns, T_A = 25°C	0.36		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6006			SN74ASC6006			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Any	Y	C_L = 0	0.8	1.5	4.1	0.8	1.5	3.7	ns
t_{PHL}	Any A	Y		0.2	0.8	1.6	0.3	0.8	1.6	
t_{PHL}	Any B	Y		0.4	1	2	0.5	1	1.9	
t_{PLH}	Any	Y	C_L = 1 pF	2.2	4.5	11	2.3	4.5	9.9	ns
t_{PHL}	Any A	Y		0.7	1.4	3	0.8	1.4	2.8	
t_{PHL}	Any B	Y		0.9	1.9	4.6	1	1.9	4	
Δt_{PLH}	Any	Y		1.4	3	7	1.5	3	6.3	ns/pF
Δt_{PHL}	Any A	Y		0.4	0.6	1.4	0.4	0.6	1.2	
Δt_{PHL}	Any B	Y		0.5	0.9	2.6	0.5	0.9	2.2	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to the 'ASC6017 data sheet and Section 7.

TEXAS INSTRUMENTS
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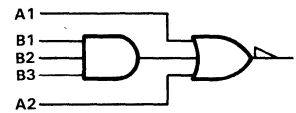
SystemCell™ 2-μm INTERNAL STANDARD CELL

- **Typical Propagation Delay with 1-pF Load**
  3.2 ns from Any A
  3.7 ns from Any B
- **Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V**
- **Functional Operation Over V_{CC} Range of 2 V to 6 V**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol



FUNCTION TABLE

INPUTS					OUTPUT
A1	A2	B1	B2	B3	Y
H	X	X	X	X	L
X	H	X	X	X	L
X	X	H	H	H	L
L	L	L	X	X	H
L	L	X	L	X	H
L	L	X	X	L	H

positive logic equation

$$Y = \overline{A1 + A2 + (B1 \cdot B2 \cdot B3)}$$

description

The SN54ASC6007 and SN74ASC6007 are expandable 1-1-3-input AND-NOR gate CMOS standard cells. The cells are designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
BF007LH	Label: BF007LH A1,A2,B1,B2,B3,Y;	1.75

The SN54ASC6007 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6007 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER		TEST CONDITIONS		TYP	MAX	UNIT
V_T Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		V
I_{CC} Supply current	SN54ASC6007	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0			240	nA
	SN74ASC6007	T_A = MIN to MAX			14.4	
C_i Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.13		pF
C_{pd} Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	$t_r = t_f$ = 3 ns,	0.36		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6007			SN74ASC6007			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Any	Y	C_L = 0	0.7	1.8	5	0.7	1.8	4.5	ns
t_{PHL}	Any A	Y		0.3	0.9	1.6	0.3	0.9	1.6	
t_{PHL}	Any B	Y		0.4	1.2	2.7	0.5	1.2	2.4	
t_{PLH}	Any	Y	C_L = 1 pF	2.2	4.8	11.8	2.3	4.8	10.7	ns
t_{PHL}	Any A	Y		0.7	1.5	3.1	0.8	1.5	2.8	
t_{PHL}	Any B	Y		1.1	2.5	6.2	1.2	2.5	5.4	
Δt_{PLH}	Any	Y		1.4	3	6.9	1.5	3	6.3	ns/pF
Δt_{PHL}	Any A	Y		0.4	0.6	1.5	0.4	0.6	1.2	
Δt_{PHL}	Any B	Y		0.6	1.3	3.6	0.7	1.3	3.1	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

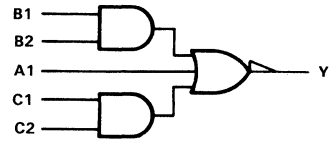
Refer to the 'ASC6017 data sheet and Section 7.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SystemCell™ 2-μm INTERNAL STANDARD CELL

- 3.4 ns Typical Propagation Delay with 1-pF Load
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol



FUNCTION TABLE

INPUTS					OUTPUT
A1	B1	B2	C1	C2	Y
H	X	X	X	X	L
X	H	H	X	X	L
X	X	X	H	H	L
Any other combination					H

positive logic equation

$$Y = \overline{A1 + (B1 \cdot B2) + (C1 \cdot C2)}$$

description

The SN54ASC6008 and SN74ASC6008 are expandable 1-2-2 input AND-NOR gate CMOS standard cells. The cells are designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		TYPICAL DELAY C_L = 1 pF	RELATIVE CELL AREA TO NA210LH
BF008LH	Label: BF008LH A1,B1,B2,C1,C2,Y;	3.4 ns	2

The SN54ASC6008 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6008 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER		TEST CONDITIONS		TYP	MAX	UNIT
V_T Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		V
I_{CC} Supply current	SN54ASC6008	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0,			210	nA
	SN74ASC6008	T_A = MIN to MAX			14.9	
C_i Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.13		pF
C_{pd} Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	$t_r = t_f$ = 3 ns,	0.44		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6008			SN74ASC6008			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Any	Y	C_L = 0	0.9	1.8	5.3	0.9	1.8	4.7	ns
t_{PHL}	A1			0.4	1	1.7	0.4	1	1.7	
t_{PHL}	Any B, C			0.3	1	2.3	0.4	1	2.1	
t_{PLH}	Any	Y	C_L = 1 pF	2.3	4.8	12.1	2.5	4.8	10.9	ns
t_{PHL}	A1			0.8	1.6	3.2	0.9	1.6	2.9	
t_{PHL}	Any B, C			0.8	2	4.8	0.9	2	4.2	
Δt_{PLH}	Any	Y		1.4	3	6.9	1.5	3	6.3	ns/pF
Δt_{PHL}	A1			0.4	0.6	1.5	0.4	0.6	1.3	
Δt_{PHL}	Any B, C			0.5	1	2.6	0.5	1	2.2	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

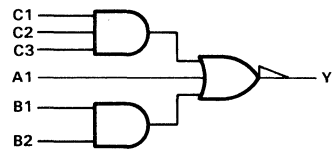
Refer to the 'ASC6017 data sheet and Section 7.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SystemCell™ 2-μm INTERNAL STANDARD CELL

- 3.7 ns Typical Propagation Delay with 1-pF Load
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol



positive logic equation

$$Y = \overline{A1 + (B1 \cdot B2) + (C1 \cdot C2 \cdot C3)}$$

FUNCTION TABLE

INPUTS						OUTPUT
A1	B1	B2	C1	C2	C3	Y
H	X	X	X	X	X	L
X	H	H	X	X	X	L
X	X	X	H	H	H	L
Any other combination						H

description

The SN54ASC6009 and SN74ASC6009 are expandable 1-2-3-input AND-NOR gate CMOS standard cells. The cells are designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		TYPICAL DELAY C_L = 1 pF	RELATIVE CELL AREA TO NA210LH
BF009LH	Label: BF009LH A1,B1,B2,C1,C2,C3,Y;	3.7 ns	2

The SN54ASC6009 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6009 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		V
I_{CC}	Supply current	SN54ASC6009	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		266	nA
		SN74ASC6009			15.9	
C_i	Input capacitance		V_{CC} = 5 V, T_A = 25°C	0.13		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, t_r = t_f = 3 ns, T_A = 25°C	0.45		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6009			SN74ASC6009			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Any	Y	C_L = 0	0.9	2	6.1	0.9	2	5.5	ns
t_{PHL}	A1	Y		0.4	1	1.8	0.5	1	1.7	
t_{PHL}	Any B, C	Y		0.3	1.2	3	0.4	1.2	2.7	
t_{PLH}	Any	Y	C_L = 1 pF	2.3	5	12.9	2.5	5	11.7	ns
t_{PHL}	A1	Y		0.8	1.6	3.2	0.9	1.6	2.9	
t_{PHL}	Any B, C	Y		0.9	2.4	6.6	1	2.4	5.7	
Δt_{PLH}	Any	Y		1.4	3	6.9	1.5	3	6.3	ns/pF
Δt_{PHL}	A1	Y		0.4	0.6	1.5	0.4	0.6	1.3	
Δt_{PHL}	Any B, C	Y		0.5	1.2	3.6	0.5	1.2	3.1	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

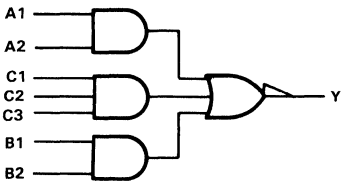
Refer to the 'ASC6017 data sheet and Section 7.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SystemCell™ 2-μm INTERNAL STANDARD CELL

- 3.7 ns Typical Propagation Delay with 1-pF Load
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol



positive logic equation

$$Y = \overline{(A1 \cdot A2) + (B1 \cdot B2) + (C1 \cdot C2 \cdot C3)}$$

FUNCTION TABLE

INPUTS							OUTPUT
A1	A2	B1	B2	C1	C2	C3	Y
H	H	X	X	X	X	X	L
X	X	H	H	X	X	X	L
X	X	X	X	H	H	H	L
Any other combination							H

description

The SN54ASC6012 and SN74ASC6012 are 3-wide, 2-2-3-input AND-NOR gate CMOS standard cells. The cells are designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		TYPICAL DELAY C_L = 1 pF	RELATIVE CELL AREA TO NA210LH
BF012LH	Label: BF012LH A1,A2,B1,B2,C1,C2,C3,Y;	3.7 ns	2.5

The SN54ASC6012 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6012 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS		TYP	MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		V
I_{CC}	Supply current	SN54ASC6012	V_{CC} = 4.5 V to 5.5 V,	V_I = V_{CC} or 0,		312	nA
		SN74ASC6012	T_A = MIN to MAX			18.7	
C_i	Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.13		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	$t_r = t_f$ = 3 ns,	0.56		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6012			SN74ASC6012			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Any	Y	C_L = 0	0.9	2.1	7	0.9	2.1	6.3	ns
t_{PHL}				0.3	1.2	3.2	0.4	1.2	2.8	
t_{PLH}	Any	Y	C_L = 1 pF	2.3	5.1	13.8	2.5	5.1	12.5	ns
t_{PHL}				0.9	2.3	6.7	0.9	2.3	5.8	
Δt_{PLH}	Any	Y		1.4	3	6.9	1.5	3	6.2	ns/pF
Δt_{PHL}				0.5	1.1	3.5	0.5	1.1	3.1	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

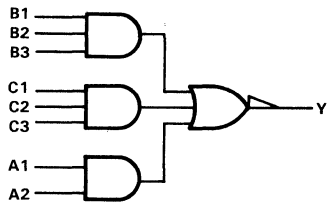
Refer to the 'ASC6017 data sheet and Section 7.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SystemCell™ 2-μm INTERNAL STANDARD CELL

- 4.1 ns Typical Propagation Delay with 1-pF Load
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol



positive logic equation

$$Y = \overline{(A1 \cdot A2) + (B1 \cdot B2 \cdot B3) + (C1 \cdot C2 \cdot C3)}$$

FUNCTION TABLE

INPUTS								OUTPUT
A1	A2	B1	B2	B3	C1	C2	C3	Y
H	H	X	X	X	X	X	X	L
X	X	H	H	H	X	X	X	L
X	X	X	X	X	H	H	H	L
Any other combination								H

description

The SN54ASC6013 and SN74ASC6013 are 3-wide, 2-3-3-input AND-NOR gate CMOS standard cells. The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		TYPICAL DELAY C_L = 1 pF	RELATIVE CELL AREA TO NA210LH
BF013LH	Label: BF013LH A1,A2,B1,B2,B3,C1,C2,C3,Y;	4.1 ns	2.5

The SN54ASC6013 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6013 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS		TYP	MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		V
I_{CC}	Supply current	SN54ASC6013	V_{CC} = 4.5 V to 5.5 V,	V_I = V_{CC} or 0,		330	nA
		SN74ASC6013	T_A = MIN to MAX			19.8	
C_i	Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.13		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	0.57		pF

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6013			SN74ASC6013			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Any	Y	C_L = 0	1	2.5	7.9	1.1	2.5	7.1	ns
t_{PHL}				0.4	1.3	3.4	0.4	1.3	3	
t_{PLH}	Any	Y	C_L = 1 pF	2.5	5.5	14.6	2.6	5.5	13.2	ns
t_{PHL}				0.9	2.6	7	1	2.6	6	
Δt_{PLH}	Any	Y		1.4	3	6.9	1.5	3	6.3	ns/pF
Δt_{PHL}				0.5	1.3	3.7	0.5	1.3	3.2	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

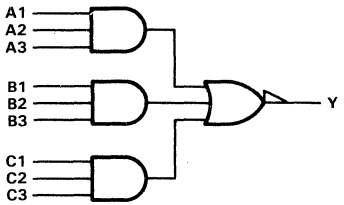
Refer to the 'ASC6017 data sheet and Section 7.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SystemCell™ 2-μm INTERNAL STANDARD CELL

- 4.3 ns Typical Propagation Delay with 1-pF Load
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol



positive logic equation

$$Y = \overline{(A1 \cdot A2 \cdot A3) + (B1 \cdot B2 \cdot B3) + (C1 \cdot C2 \cdot C3)}$$

FUNCTION TABLE

INPUTS									OUTPUT
A1	A2	A3	B1	B2	B3	C1	C2	C3	Y
H	H	H	X	X	X	X	X	X	L
X	X	X	H	H	H	X	X	X	L
X	X	X	X	X	X	H	H	H	L
Any other combination									H

description

The SN54ASC6014 and SN74ASC6014 are 3-wide, 3-input AND-NOR gate CMOS standard cells. The cells are designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		TYPICAL DELAY C_L = 1 pF	RELATIVE CELL AREA TO NA210LH
BF014LH	Label: BF014LH A1,A2,A3,B1,B2,B3,C1,C2,C3,Y;	4.3 ns	2.75

The SN54ASC6014 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6014 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER		TEST CONDITIONS		TYP	MAX	UNIT
V_T Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		V
I_{CC} Supply current	SN54ASC6014	V_{CC} = 4.5 V to 5.5 V,	$V_I = V_{CC}$ or 0,		363	nA
	SN74ASC6014	T_A = MIN to MAX			21.8	
C_i Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.13		pF
C_{pd} Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	$t_r = t_f$ = 3 ns,	0.71		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6014			SN74ASC6014			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Any	Y	C_L = 0	1.1	2.8	9.4	1.1	2.8	8.4	ns
t_{PHL}				0.4	1.4	3.9	0.5	1.4	3.4	
t_{PLH}	Any	Y	C_L = 1 pF	2.5	5.8	16	2.6	5.8	14.5	ns
t_{PHL}				1.1	2.8	7.5	1.2	2.8	6.5	
Δt_{PLH}	Any	Y		1.4	3	6.8	1.5	3	6.2	ns/pF
Δt_{PHL}				0.6	1.4	3.7	0.6	1.4	3.1	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

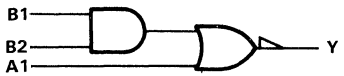
Refer to the 'ASC6017 data sheet and Section 7.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SystemCell™ 2-μm INTERNAL STANDARD CELL

- 2.5 ns Typical Propagation Delay with 1-pF Load
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol



FUNCTION TABLE

INPUTS			OUTPUT
A1	B2	B1	Y
H	X	X	L
X	H	H	L
L	L	X	H
L	X	L	H

positive logic equation

$$Y = \overline{A1 + (B1 \cdot B2)}$$

description

The SN54ASC6017 and SN74ASC6017 are expandable 1-2-input AND-NOR gate CMOS standard cells. The cells are designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		TYPICAL DELAY C_L = 1 pF	RELATIVE CELL AREA TO NA210LH
BF001LH	Label: BF001LH A1,B1,B2,Y;	2.5 ns	1.5

The SN54ASC6017 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6017 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS		TYP	MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		V
I_{CC}	Supply current	SN54ASC6017	V_{CC} = 4.5 V to 5.5 V,	V_I = V_{CC} or 0,		187	nA
		SN74ASC6017	T_A = MIN to MAX			11.2	
C_i	Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.13		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	$t_r = t_f$ = 2 ns,	0.38		pF

4 Data Sheets

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6017			SN74ASC6017			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Any	Y	C_L = 0	0.6	1.1	2.4	0.6	1.1	2.2	ns
t_{PHL}				0.2	0.9	1.9	0.3	0.9	1.7	
t_{PLH}	Any	Y	C_L = 1 pF	1.6	3.1	6.9	1.7	3.1	6.3	ns
t_{PHL}				0.7	1.8	4.3	0.8	1.8	3.8	
Δt_{PLH}	Any	Y		0.9	2	4.6	1	2	4.2	ns/pF
Δt_{PHL}				0.4	0.9	2.5	0.4	0.9	2.1	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to Section 7.

All inputs to this cell, as well as all cells, must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

This Boolean function is a member of a series of multifunction cells designed to simplify the implementation of a broad class of higher-level logic equations such as:

- Sum of products
- Exclusive-OR and exclusive-NOR functions
- Majority decoders
- Modulo adders
- Carry-save adders
- Function generators
- Random logic

The members of this class of standard-cell functions are grouped in the 'ASC6000 series of type numbers. The selection consists of four primary architectures with expandable versions offered in each:

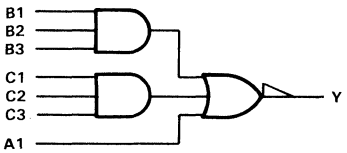
- Dedicated and expandable AND-NOR gates
- Dedicated and expandable OR-AND-NOR gates
- Expandable AND-OR-NOR gates
- Expandable OR-NAND gates
- Expandable AND-OR-NAND gates
- Expandable OR-AND-OR-NAND gates

Options are offered in each architecture from basic 2-wide functions up to expandable 3-wide functions providing single-macro solutions to most design requirements. The expandable functions can be combined with basic gating cells and/or other Boolean cells offered in Texas Instruments standard-cell family to implement the application-specific solutions.

SystemCell™ 2-μm INTERNAL STANDARD CELL

- 3.9 ns Typical Propagation Delay with 1-pF Load
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol



positive logic equation

$$Y = \overline{A1 + (B1 \cdot B2 \cdot B3) + (C1 \cdot C2 \cdot C3)}$$

FUNCTION TABLE

INPUTS							OUTPUT
A1	B1	B2	B3	C1	C2	C3	Y
H	X	X	X	X	X	X	L
X	H	H	H	X	X	X	L
X	X	X	X	H	H	H	L
Any other combination							H

description

The SN54ASC6018 and SN74ASC6018 are expandable 1-3-3-input AND-NOR gate CMOS standard cells. The cells are designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		TYPICAL DELAY C_L = 1 pF	RELATIVE CELL AREA TO NA210LH
BF010LH	Label: BF010LH A1,B1,B2,B3,C1,C2,C3,Y;	3.9 ns	2

The SN54ASC6018 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6018 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS		TYP	MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		V
I_{CC}	Supply current	SN54ASC6018	V_{CC} = 4.5 V to 5.5 V,	$V_I = V_{CC}$ or 0,		301	nA
		SN74ASC6018	T_A = MIN to MAX			18.1	
C_i	Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.13		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	$t_r = t_f$ = 3 ns,	0.45		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6018			SN74ASC6018			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Any	Y	C_L = 0	0.8	2.1	6.6	0.9	2.1	6	ns
t_{PHL}	A1			0.3	0.8	1.5	0.3	0.8	1.5	
t_{PHL}	Any B, C			0.5	1.3	3	0.5	1.3	2.6	
t_{PLH}	Any	Y	C_L = 1 pF	2.3	5.1	13.4	2.4	5.1	12.2	ns
t_{PHL}	A1			0.7	1.4	2.9	0.8	1.4	2.7	
t_{PHL}	Any B, C			1.1	2.6	6.6	1.3	2.6	5.7	
Δt_{PLH}	Any	Y		1.4	3	6.7	1.5	3	6.3	ns/pF
Δt_{PHL}	A1			0.4	0.6	1.4	0.4	0.6	1.2	
Δt_{PHL}	Any B, C			0.6	1.3	3.7	0.6	1.3	3.2	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to the 'ASC6017 data sheet and Section 7.

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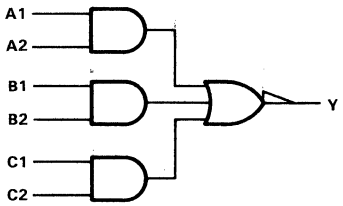
SystemCell™ 2-μm INTERNAL STANDARD CELL

- 3.5 ns Typical Propagation Delay with 1-pF Load
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol



positive logic equation

$$Y = \overline{(A1 \cdot A2) + (B1 \cdot B2) + (C1 \cdot C2)}$$

FUNCTION TABLE

INPUTS						OUTPUT
A1	A2	B1	B2	C1	C2	Y
H	H	X	X	X	X	L
X	X	H	H	X	X	L
X	X	X	X	H	H	L
Any other combination						H

description

The SN54ASC6019 and SN74ASC6019 are 3-wide, 2-input AND-NOR gate CMOS standard cells. The cells are designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		TYPICAL DELAY C_L = 1 pF	RELATIVE CELL AREA TO NA210LH
BF011LH	Label: BF011LH A1,A2,B1,B2,C1,C2,Y;	3.5 ns	2.75

The SN54ASC6019 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6019 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER		TEST CONDITIONS		TYP	MAX	UNIT
V_T Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		V
I_{CC} Supply current	SN54ASC6019	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0,			319	nA
	SN74ASC6019	T_A = MIN to MAX			19.1	
C_i Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.13		pF
C_{pd} Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	$t_r = t_f$ = 3 ns,	0.52		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6019			SN74ASC6019			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Any	Y	C_L = 0	0.9	2	6	1	2	5.4	ns
t_{PHL}				0.3	1	2.4	0.4	1	2.2	
t_{PLH}	Any	Y	C_L = 1 pF	2.4	5	12.8	2.5	5	11.6	ns
t_{PHL}				0.9	2	5	0.9	2	4.4	
Δt_{PLH}	Any	Y		1.4	3	6.9	1.5	3	6.3	ns/pF
Δt_{PHL}				0.5	1	2.6	0.5	1	2.3	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to the 'ASC6017 data sheet and Section 7.

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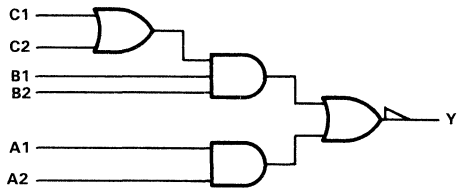
SystemCell™ 2-μm INTERNAL STANDARD CELL

- Typical Propagation Delay with 1-pF Load
  - 3.3 ns from Any A
  - 3 ns from Any B
  - 3.9 ns from Any C
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol



positive logic equation

$$Y = \overline{A1 \cdot A2 + [B1 \cdot B2 \cdot (C1 + C2)]}$$

FUNCTION TABLE

INPUTS						OUTPUT
A1	A2	B1	B2	C1	C2	Y
H	H	X	X	X	X	L
X	X	H	H	H	X	L
X	X	H	H	X	H	L
Any other combination						H

description

The SN54ASC6022 and SN74ASC6022 CMOS standard-cell Boolean macros are 2-wide 2-3-input sum-of-products AND-NOR gates with a dedicated 2-input OR, 3-input AND product term. Two available inputs to the 3-input AND gate and two to the other 2-input AND gate provide expandability for implementing customized product terms. The cells are designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
BF022LH	Label: BF022LH A1,A2,B1,B2,C1,C2,Y;	2.25

The SN54ASC6022 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6022 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS		TYP	MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		V
I_{CC}	Supply current	SN54ASC6022	V_{CC} = 4.5 V to 5.5 V,	V_I = V_{CC} or 0,		282	nA
		SN74ASC6022	T_A = MIN to MAX			16.9	
C_i	Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.13		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	$t_r = t_f$ = 3 ns,	0.54		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6022			SN74ASC6022			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Any A	Y	C_L = 0	1.1	1.9	4.4	1.1	1.9	4	ns
t_{PHL}				0.4	0.9	1.7	0.4	0.9	1.7	
t_{PLH}	Any A	Y	C_L = 1 pF	2.5	4.9	11.2	2.7	4.9	10.2	ns
t_{PHL}				0.9	1.8	4.2	1	1.8	3.8	
t_{PLH}	Any B	Y	C_L = 0	0.7	1.3	3.2	0.7	1.3	2.9	ns
t_{PHL}				0.7	1.3	2.8	0.8	1.3	2.5	
t_{PLH}	Any B	Y	C_L = 1 pF	1.7	3.3	7.7	1.8	3.3	7	ns
t_{PHL}				1.3	2.7	6.5	1.4	2.7	5.6	
t_{PLH}	Any C	Y	C_L = 0	1.1	2.2	5.4	1.1	2.2	4.9	ns
t_{PHL}				0.5	1.2	2.9	0.5	1.2	2.5	
t_{PLH}	Any C	Y	C_L = 1 pF	2.5	5.2	12.2	2.7	5.2	11	ns
t_{PHL}				1.1	2.5	6.5	1.2	2.5	5.6	
Δt_{PLH}	Any A	Y		1.4	3	6.9	1.5	3	6.3	ns/pF
Δt_{PHL}				0.5	0.9	2.5	0.5	0.9	2.2	
Δt_{PLH}	Any B	Y		0.9	2	4.6	1	2	4.2	ns/pF
Δt_{PHL}				0.6	1.4	3.6	0.6	1.4	3.1	
Δt_{PLH}	Any C	Y		1.4	3	6.9	1.5	3	6.2	ns/pF
Δt_{PHL}				0.6	1.3	3.6	0.6	1.3	3.1	

†Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to the 'ASC6017 data sheet and Section 7.

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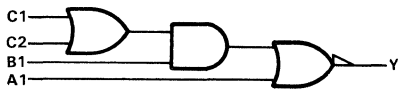
SystemCell™ 2-μm INTERNAL STANDARD CELL

- **Typical Propagation Delay with 1-pF Load**
  2.9 ns from A1
  2.5 ns from B1
  3.2 ns from Any C
- **Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V**
- **Functional Operation Over V_{CC} Range of 2 V to 6 V**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol



FUNCTION TABLE

INPUTS				OUTPUT
A1	B1	C1	C2	Y
H	X	X	X	L
X	H	H	X	L
X	H	X	H	L
L	L	X	X	H
L	X	L	L	H

positive logic equation

$$Y = \overline{A1 + [B1 \cdot (C1 + C2)]}$$

description

The SN54ASC6023 and SN74ASC6023 CMOS standard-cell Boolean macros are 2-input sum-of-products NOR gates with a dedicated 2-input OR, 2-input AND product term. One available input to the 2-input AND gate and the 2-input NOR gate provides expandability for implementing customized product terms. The cells are designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
BF015LH	Label: BF015LH A1,B1,C1,C2,Y;	1.75

The SN54ASC6023 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6023 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS		TYP	MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		V
I_{CC}	Supply current	SN54ASC6023	V_{CC} = 4.5 V to 5.5 V,	V_I = V_{CC} or 0,		218	μA
		SN74ASC6023	T_A = MIN to MAX			13.1	
C_i	Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.13		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	0.36		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6023			SN74ASC6023			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A1	Y	C_L = 0	1	1.4	2.7	1.1	1.4	2.5	ns
t_{PHL}				0.2	0.8	1.4	0.3	0.8	1.4	
t_{PLH}	A1	Y	C_L = 1 pF	2.4	4.4	9.5	2.6	4.4	8.7	ns
t_{PHL}				0.7	1.4	2.8	0.8	1.4	2.6	
t_{PLH}	B1	Y	C_L = 0	0.6	0.9	1.9	0.6	0.9	1.7	ns
t_{PHL}				0.5	1	1.8	0.6	1	1.7	
t_{PLH}	B1	Y	C_L = 1 pF	1.6	2.9	6.4	1.7	2.9	5.8	ns
t_{PHL}				1.1	2	4.3	1.2	2	3.8	
t_{PLH}	Any C	Y	C_L = 0	0.9	1.7	4.1	0.9	1.7	3.7	ns
t_{PHL}				0.4	0.9	1.9	0.4	0.9	1.7	
t_{PLH}	Any C	Y	C_L = 1 pF	2.3	4.7	10.9	2.5	4.7	9.9	ns
t_{PHL}				0.9	1.9	4.4	1	1.9	3.9	
Δt_{PLH}	A1	Y		1.4	3	6.4	1.5	3	6.2	ns/pF
Δt_{PHL}				0.4	0.6	1.4	0.4	0.6	1.2	
Δt_{PLH}	B1	Y		0.9	2	4.6	1	2	2.4	ns/pF
Δt_{PHL}				0.5	1	2.5	0.5	1	2.1	
Δt_{PLH}	Any C	Y		1.4	3	6.9	1.5	3	6.2	ns/pF
Δt_{PHL}				0.5	1	2.6	0.5	1	2.2	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to the 'ASC6017 data sheet and Section 7.

TEXAS INSTRUMENTS
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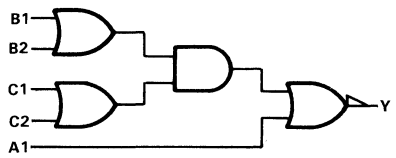
SystemCell™ 2-μm INTERNAL STANDARD CELL

- **Typical Propagation Delay with 1-pF Load**
  - **3.2 ns from A1**
  - **3.6 ns from Any B**
  - **3.4 ns from Any C**
- **Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V**
- **Functional Operation Over V_{CC} Range of 2 V to 6 V**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol



FUNCTION TABLE

INPUTS					OUTPUT
A1	B1	B2	C1	C2	Y
H	X	X	X	X	L
X	H	X	H	X	L
X	X	H	H	X	L
X	H	X	X	H	L
X	X	H	X	H	L
L	L	L	X	X	H
L	X	X	L	L	H

positive logic equation

$$Y = \overline{A1 + [(B1 + B2) \cdot (C1 + C2)]}$$

description

The SN54ASC6024 and SN74ASC6024 CMOS standard-cell Boolean macros are 2-input sum-of-products NOR gates with a dedicated 2-wide, 2-input OR-AND product term. The available NOR input can be used to combine other custom product terms with the 2-wide, 2-input OR-AND term. The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
BF016LH	Label: BF016LH A1,B1,B2,C1,C2,Y;	2.5

The SN54ASC6024 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6024 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		V
I_{CC} Supply current	SN54ASC6024	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		289	nA
	SN74ASC6024			17.4	
C_i Input capacitance		V_{CC} = 5 V, T_A = 25°C	0.13		pF
C_{pd} Equivalent power dissipation capacitance		V_{CC} = 5 V, $t_r = t_f$ = 3 ns, T_A = 25°C	0.42		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6024			SN74ASC6024			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A1	Y	C_L = 0	1.2	1.9	4	1.3	1.9	3.6	ns
t_{PHL}				0.3	0.9	1.6	0.4	0.9	1.5	
t_{PLH}	A1	Y	C_L = 1 pF	2.6	4.9	10.8	2.8	4.9	9.8	ns
t_{PHL}				0.8	1.5	3	0.8	1.5	2.7	
t_{PLH}	Any B	Y	C_L = 0	1.1	2.2	5.3	1.1	2.2	4.8	ns
t_{PHL}				0.5	1	2.2	0.5	1	2	
t_{PLH}	Any B	Y	C_L = 1 pF	2.5	5.2	12.2	2.7	5.2	11	ns
t_{PHL}				1	2	4.8	1.1	2	4.2	
t_{PLH}	Any C	Y	C_L = 0	0.8	1.6	3.9	0.9	1.6	3.5	ns
t_{PHL}				0.6	1.2	2.2	0.7	1.2	2	
t_{PLH}	Any C	Y	C_L = 1 pF	2.3	4.6	10.8	2.4	4.6	9.8	ns
t_{PHL}				1.1	2.2	4.8	1.2	2.2	4.2	
Δt_{PLH}	A1	Y		1.4	3	6.9	1.5	3	6.2	ns/pF
Δt_{PHL}				0.4	0.6	1.4	0.4	0.6	1.2	
Δt_{PLH}	Any B	Y		1.4	3	6.9	1.5	3	6.2	ns/pF
Δt_{PHL}				0.5	1	2.6	0.5	1	2.2	
Δt_{PLH}	Any C	Y		1.4	3	6.9	1.5	3	6.3	ns/pF
Δt_{PHL}				0.5	1	2.6	0.5	1	2.2	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

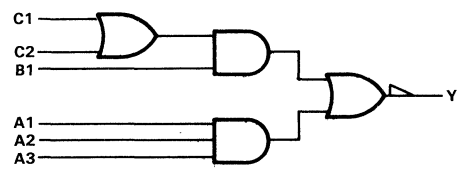
Refer to the 'ASC6017 data sheet and Section 7.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SystemCell™ 2-μm INTERNAL STANDARD CELL

- **Typical Propagation Delay with 1-pF Load**
  - **3.6 ns from Any A**
  - **2.7 ns from B1**
  - **3.5 ns from Any C**
- **Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V**
- **Functional Operation Over V_{CC} Range of 2 V to 6 V**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol



positive logic equation

$$Y = \overline{A1 \cdot A2 \cdot A3 + [B1 \cdot (C1 + C2)]}$$

FUNCTION TABLE

INPUTS						OUTPUT
A1	A2	A3	B1	C1	C2	Y
H	H	H	X	X	X	L
X	X	X	H	H	X	L
X	X	X	H	X	H	L
Any other combination						H

description

The SN54ASC6025 and SN74ASC6025 CMOS standard-cell Boolean macros are 2-wide 3-2-input sum-of-products AND-NOR gates with a dedicated 2-input OR, 2-input AND product term. One available input to the 2-input AND gate and three to the 3-input AND gate provide expandability for implementing customized product terms. The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
BF025LH	Label: BF025LH A1,A2,A3,B1,C1,C2,Y;	2.25

The SN54ASC6025 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6025 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS		TYP	MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		V
I_{CC}	Supply current	SN54ASC6025	V_{CC} = 4.5 V to 5.5 V,	V_I = V_{CC} or 0,		281	nA
		SN74ASC6025	T_A = MIN to MAX			16.9	
C_i	Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.13		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	0.64		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6025			SN74ASC6025			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Any A	Y	C_L = 0	1	1.9	4.8	1	1.9	4.3	ns
t_{PHL}				0.4	1.1	2.4	0.5	1.1	2.1	
t_{PLH}	Any A	Y	C_L = 1 pF	2.4	4.9	11.5	2.6	4.9	10.5	ns
t_{PHL}				1.1	2.4	5.8	1.2	2.4	5.1	
t_{PLH}	B1	Y	C_L = 0	0.7	1.1	2.5	0.8	1.1	2.3	ns
t_{PHL}				0.7	1.2	2.2	0.7	1.2	2	
t_{PLH}	B1	Y	C_L = 1 pF	1.7	3.1	7	1.8	3.1	6.4	ns
t_{PHL}				1.2	2.2	4.7	1.3	2.2	4.2	
t_{PLH}	Any C	Y	C_L = 0	1	2	4.9	1.1	2	4.4	ns
t_{PHL}				0.5	1	2.3	0.5	1	2	
t_{PLH}	Any C	Y	C_L = 1 pF	2.5	5	11.7	2.6	5	10.6	ns
t_{PHL}				1	2	4.8	1.1	2	4.2	
Δt_{PLH}	Any A	Y		1.4	3	6.8	1.5	3	6.2	ns/pF
Δt_{PHL}				0.6	1.3	3.5	0.6	1.3	3	
Δt_{PLH}	B1	Y		0.9	2	4.6	1	2	4.2	ns/pF
Δt_{PHL}				0.5	1	2.5	0.5	1	2.2	
Δt_{PLH}	Any C	Y		1.4	3	6.9	1.5	3	6.2	ns/pF
Δt_{PHL}				0.5	1	2.6	0.5	1	2.2	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

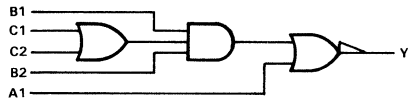
Refer to the 'ASC6017 data sheet and Section 7.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SystemCell™ 2-μm INTERNAL STANDARD CELL

- **Typical Propagation Delay with 1-pF Load**
  3 ns from A1
  2.9 ns from Any B
  3.7 ns from Any C
- **Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V**
- **Functional Operation Over V_{CC} Range of 2 V to 6 V**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol



FUNCTION TABLE

INPUTS					OUTPUT
A1	B1	B2	C1	C2	Y
L	L	X	X	X	H
L	X	L	X	X	H
L	X	X	L	L	H
L	L	X	L	L	H
L	X	L	L	L	H
X	H	H	H	X	L
X	H	H	X	H	L
H	X	X	X	X	L

positive logic equation

$$Y = \overline{A1 + [B1 \cdot B2 \cdot (C1 + C2)]}$$

description

The SN54ASC6026 and SN74ASC6026 CMOS standard-cell Boolean macros are 2-input sum-of-products NOR gates with a dedicated 2-input OR, 3-input AND product term. Two available inputs to the 3-input AND gate and one to the other 2-input NOR gate provide expandability for implementing customized product terms. The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
BF017LH	Label: BF017LH A1,B1,B2,C1,C2,Y;	2

The SN54ASC6026 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6026 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS		TYP	MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		V
I_{CC}	Supply current	SN54ASC6026	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0,			248	nA
		SN74ASC6026	T_A = MIN to MAX			14.9	
C_i	Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.13		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	$t_r = t_f$ = 3 ns,	0.4		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6026			SN74ASC6026			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A1	Y	C_L = 0	1.2	1.7	3	1.2	1.7	2.8	ns
t_{PHL}				0.3	0.8	1.2	0.3	0.8	1.2	
t_{PLH}	A1	Y	C_L = 1 pF	2.6	4.7	8.7	2.7	4.7	7.9	ns
t_{PHL}				0.7	1.4	2.4	0.8	1.4	2.2	
t_{PLH}	Any B	Y	C_L = 0	0.7	1.2	2.5	0.7	1.2	2.2	ns
t_{PHL}				0.7	1.2	2.2	0.7	1.2	1.9	
t_{PLH}	Any B	Y	C_L = 1 pF	1.6	3.2	6.2	1.7	3.2	5.6	ns
t_{PHL}				1.3	2.5	5.1	1.4	2.5	4.5	
t_{PLH}	Any C	Y	C_L = 0	1	2	4.1	1	2	3.7	ns
t_{PHL}				0.4	1	2.2	0.5	1	1.9	
t_{PLH}	Any C	Y	C_L = 1 pF	2.4	5	9.8	2.6	5	8.9	ns
t_{PHL}				1.1	2.3	5.1	1.2	2.3	4.5	
Δt_{PLH}	A1	Y		1.4	3	5.7	1.5	3	5.2	ns/pF
Δt_{PHL}				0.4	0.6	1.2	0.4	0.6	1	
Δt_{PLH}	Any B	Y		0.9	2	3.8	1	2	3.5	ns/pF
Δt_{PHL}				0.6	1.3	3	0.7	1.3	2.6	
Δt_{PLH}	Any C	Y		1.4	3	5.7	1.5	3	5.2	ns/pF
Δt_{PHL}				0.6	1.3	3	0.7	1.3	2.6	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

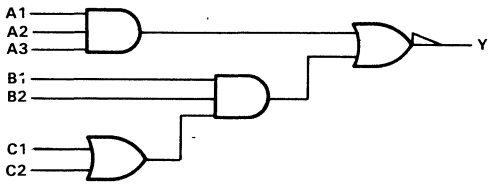
Refer to the 'ASC6017 data sheet and Section 7.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SystemCell™ 2-μm INTERNAL STANDARD CELL

- **Typical Propagation Delay with 1-pF Load**
  2.4 ns from Any A
  2.6 ns from Any B
  3.6 ns from Any C
- **Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V**
- **Functional Operation Over V_{CC} Range of 2 V to 6 V**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol



FUNCTION TABLE

INPUTS							OUTPUT
A1	A2	A3	B1	B2	C1	C2	Y
H	H	H	X	X	X	X	L
X	X	X	H	H	H	X	L
X	X	X	H	H	X	H	L
Any other combination							H

positive logic equation

$$Y = \overline{A1 \cdot A2 \cdot A3 + [B1 \cdot B2 \cdot (C1 + C2)]}$$

description

The SN54ASC6027 and SN74ASC6027 CMOS standard-cell Boolean macros are 2-wide OR-AND-NOR gates with an OR gate comprising an input to the second AND gate. The first AND gate has 3 available inputs. The second AND gate has 2 available inputs plus the 2 ORed inputs. This combination provides expandability for implementing customized product terms. The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
BF027LH	Label: BF027LH A1,A2,A3,B1,B2,C1,C2,Y;	2.5

The SN54ASC6027 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6027 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER		TEST CONDITIONS		TYP	MAX	UNIT
V_T Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		V
I_{CC} Supply current	SN54ASC6027	V_{CC} = 4.5 V to 5.5 V,	V_I = V_{CC} or 0,		334	nA
	SN74ASC6027	T_A = MIN to MAX			18.3	
C_i Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.13		pF
C_{pd} Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	$t_r = t_f$ = 3 ns,	0.98		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6027			SN74ASC6027			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Any A	Y	C_L = 0	0.7	1.1	2.2	0.7	1.1	2	ns
t_{PHL}				0.4	1	2	0.4	1	1.8	
t_{PLH}	Any A	Y	C_L = 1 pF	1.4	2.4	5.2	1.4	2.4	4.8	ns
t_{PHL}				1	2.3	5.4	1.1	2.3	4.7	
t_{PLH}	Any B	Y	C_L = 0	0.7	1.2	2.6	0.8	1.2	2.4	ns
t_{PHL}				0.7	1.5	3.1	0.8	1.5	2.8	
t_{PLH}	Any B	Y	C_L = 1 pF	1.3	2.5	5.6	1.4	2.5	5.1	ns
t_{PHL}				1.2	2.6	6	1.3	2.6	5.2	
t_{PLH}	Any C	Y	C_L = 0	1	2.1	5	1.1	2.1	4.5	ns
t_{PHL}				0.6	1.5	4	0.7	1.5	3.5	
t_{PLH}	Any C	Y	C_L = 1 pF	2.1	4.4	10.1	2.2	4.4	9.2	ns
t_{PHL}				1.2	2.8	7.4	1.3	2.8	6.4	
Δt_{PLH}	Any A	Y		0.6	1.3	3.1	0.6	1.3	2.8	ns/pF
Δt_{PHL}				0.6	1.3	3.4	0.6	1.3	2.9	
Δt_{PLH}	Any B	Y		0.6	1.3	3	0.6	1.3	2.8	ns/pF
Δt_{PHL}				0.5	1.1	2.9	0.5	1.1	2.5	
Δt_{PLH}	Any C	Y		1	2.3	5.2	1.1	2.3	4.8	ns/pF
Δt_{PHL}				0.5	1.3	3.4	0.6	1.3	3	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f = 3$ ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

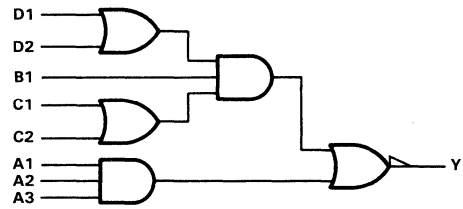
Refer to the 'ASC6017 data sheet and Section 7.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SystemCell™ 2-μm INTERNAL STANDARD CELL

- **Typical Propagation Delay With 1-pF Load**
  5.7 ns from Any A or B1
  3.6 ns from Any C or D
- **Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V**
- **Functional Operation Over V_{CC} Range of 2 V to 6 V**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol



positive logic equation

$$Y = \overline{A1 \cdot A2 \cdot A3 + [B1 \cdot (C1 + C2) \cdot (D1 + D2)]}$$

description

The SN54ASC6028 and SN74ASC6028 CMOS standard-cell Boolean macros are 2-wide AND-NOR gates with OR gates comprising 2 inputs to the second AND gate. The first AND gate has 3 available inputs. The second AND gate has 1 available input plus the 4 ORed inputs. This combination provides expandability for implementing customized product terms. The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

FUNCTION TABLE

INPUTS								OUTPUT
A1	A2	A3	B1	C1	C2	D1	D2	Y
H	H	H	X	X	X	X	X	L
X	X	X	H	H	X	H	X	L
X	X	X	H	H	X	X	H	L
X	X	X	H	X	H	H	X	L
X	X	X	H	X	H	X	H	L
Any other combination								H

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
BF028LH	Label: BF028LH A1,A2,A3,B1,C1,C2,D1,D2,Y;	2.75

The SN54ASC6028 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6028 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		V
I_{CC} Supply current	SN54ASC6028	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		341	nA
	SN74ASC6028			20.5	
C_i Input capacitance		V_{CC} = 5 V, T_A = 25°C	0.13		pF
C_{pd} Equivalent power dissipation capacitance		V_{CC} = 5 V, t_r = t_f = 3 ns, T_A = 25°C	1.11		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6028			SN74ASC6028			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Any A,B	Y	C_L = 0	0.8	1.2	2.5	0.8	1.2	2.2	ns
t_{PHL}				0.4	1.1	2.8	0.4	1.1	2.5	
t_{PLH}	Any A,B	Y	C_L = 1 pF	1.5	2.6	5.8	1.5	2.6	5.3	ns
t_{PHL}				1	2.4	5.6	1.1	2.4	4.9	
t_{PLH}	Any C,D	Y	C_L = 0	1	2.2	6	1	2.2	5.4	ns
t_{PHL}				0.7	1.5	3.9	0.8	1.5	3.4	
t_{PLH}	Any C,D	Y	C_L = 1 pF	2.1	4.5	11.3	2.2	4.5	10.2	ns
t_{PHL}				1.2	2.6	6.9	1.3	2.6	6.1	
Δt_{PLH}	Any A,B	Y		0.6	1.4	3.4	0.7	1.4	3.1	ns/pF
Δt_{PHL}				0.4	1.3	3.5	0.5	1.3	3	
Δt_{PLH}	Any C,D	Y		1.1	2.3	5.4	1.2	2.3	4.9	ns/pF
Δt_{PHL}				0.4	1.1	3.2	0.4	1.1	2.8	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

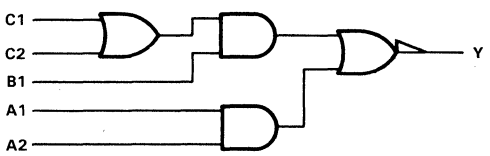
Refer to the 'ASC6017 data sheet and Section 7.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SystemCell™ 2-μm INTERNAL STANDARD CELL

- **Typical Propagation Delay with 1-pF Load**
  3.2 ns from Any A
  2.5 ns from B1
  3.4 ns from Any C
- **Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V**
- **Functional Operation Over V_{CC} Range of 2 V to 6 V**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol



FUNCTION TABLE

INPUTS					OUTPUT
A1	A2	B1	C1	C2	Y
H	H	X	X	X	L
X	X	H	H	X	L
X	X	H	X	H	L
Any other combination					H

positive logic equation

$$Y = \overline{A1 \cdot A2 + [B1 \cdot (C1 + C2)]}$$

description

The SN54ASC6029 and SN74ASC6029 CMOS standard-cell Boolean macros are 2-wide 2-input sum-of-products OR-AND-NOR gates with a dedicated 2-input OR, 2-input AND product term. One available input to one 2-input-AND gate and two to the other 2-input-AND gate provide expandability for implementing customized product terms. The cells are designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
BF020LH	Label: BF020LH A1,A2,B1,C1,C2,Y;	2

The SN54ASC6029 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6029 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS		TYP	MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		V
I_{CC}	Supply current	SN54ASC6029	V_{CC} = 4.5 V to 5.5 V,	V_I = V_{CC} or 0,		247	nA
		SN74ASC6029	T_A = MIN to MAX			14.8	
C_i	Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.13		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	$t_r = t_f$ = 3 ns,	0.47		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6029			SN74ASC6029			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Any A	Y	C_L = 0	1	1.5	3.3	1	1.5	3.1	ns
t_{PHL}				0.3	0.9	1.7	0.4	0.9	1.6	
t_{PLH}	Any A	Y	C_L = 1 pF	2.4	4.5	10.1	2.5	4.5	9.2	ns
t_{PHL}				0.8	1.8	4.1	0.9	1.8	3.6	
t_{PLH}	B1	Y	C_L = 0	0.7	1	2.1	0.7	1	1.9	ns
t_{PHL}				0.6	1.1	1.9	0.6	1.1	1.8	
t_{PLH}	B1	Y	C_L = 1 pF	1.6	3	6.6	1.7	3	6	ns
t_{PHL}				1.1	2	4.4	1.2	2	3.9	
t_{PLH}	Any C	Y	C_L = 0	0.9	1.8	4.3	1	1.8	3.9	ns
t_{PHL}				0.4	0.9	2	0.5	0.9	1.8	
t_{PLH}	Any C	Y	C_L = 1 pF	2.3	4.8	11.2	2.5	4.8	10.1	ns
t_{PHL}				0.9	1.9	4.5	1	1.9	4	
Δt_{PLH}	Any A	Y		1.4	3	6.9	1.5	3	6.2	ns/pF
Δt_{PHL}				0.5	0.9	2.5	0.5	0.9	2.1	
Δt_{PLH}	B1	Y		0.9	2	4.6	1	2	4.2	ns/pF
Δt_{PHL}				0.5	0.9	2.5	0.5	0.9	2.2	
Δt_{PLH}	Any C	Y		1.4	3	6.9	1.5	3	6.2	ns/pF
Δt_{PHL}				0.5	1	2.6	0.5	1	2.2	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

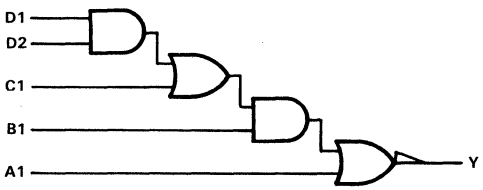
Refer to the 'ASC6017 data sheet and Section 7.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SystemCell™ 2-μm INTERNAL STANDARD CELL

- **Typical Propagation Delay with 1-pF Load**
  - **2 ns from A1**
  - **2.5 ns from B1**
  - **3 ns from C1**
  - **3.9 ns from Any D**
- **Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V**
- **Functional Operation Over V_{CC} Range of 2 V to 6 V**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol



FUNCTION TABLE

INPUTS					OUTPUT
A1	B1	C1	D1	D2	Y
H	X	X	X	X	L
X	H	H	X	X	L
X	H	X	H	H	L
Any other combination					H

positive logic equation

$$Y = \overline{A1 + \{B1 \cdot [C1 + (D1 \cdot D2)]\}}$$

description

The SN54ASC6032 and SN74ASC6032 CMOS standard-cell Boolean macros are 2-wide 1-2-input sum-of-products AND-NOR gates with 2-input AND and one available input each to the 2-input AND and OR gates to provide expandability for implementing customized product terms. The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
BF030LH	Label: BF030LH A1,B1,C1,D1,D2,Y;	2

The SN54ASC6032 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6032 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		V
I_{CC}	Supply current	SN54ASC6032	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0,		254	nA
		SN74ASC6032	T_A = MIN to MAX		15.2	
C_i	Input capacitance		V_{CC} = 5 V, T_A = 25°C	0.13		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, $t_r = t_f$ = 3 ns, T_A = 25°C	0.8		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6032			SN74ASC6032			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A1	Y	C_L = 0	0.8	1	1.6	0.8	1	1.5	ns
t_{PHL}				0.3	0.8	1.4	0.3	0.8	1.4	
t_{PLH}	A1	Y	C_L = 1 pF	1.6	2.6	5.2	1.6	2.6	4.8	ns
t_{PHL}				0.7	1.4	2.8	0.8	1.4	2.6	
t_{PLH}	B1	Y	C_L = 0	0.7	1	2.2	0.7	1	2	ns
t_{PHL}				0.5	1.1	1.8	0.6	1.1	1.8	
t_{PLH}	B1	Y	C_L = 1 pF	1.7	3	6.8	1.8	3	6.2	ns
t_{PHL}				1	1.9	3.9	1.1	1.9	3.5	
t_{PLH}	C1	Y	C_L = 0	0.9	1.5	3.6	1	1.5	3.3	ns
t_{PHL}				0.4	0.9	2	0.5	0.9	1.8	
t_{PLH}	C1	Y	C_L = 1 pF	2.1	4	9.3	2.3	4	8.4	ns
t_{PHL}				0.9	1.9	4.4	1	1.9	3.9	
t_{PLH}	Any D	Y	C_L = 0	1	2.2	5.6	1	2.2	5	ns
t_{PHL}				0.5	1.2	2.9	0.5	1.2	2.6	
t_{PLH}	Any D	Y	C_L = 1 pF	2.4	5.2	12.4	2.6	5.2	11.2	ns
t_{PHL}				1.1	2.6	6.5	1.2	2.6	5.6	
Δt_{PLH}	A1	Y		0.7	1.6	3.7	0.8	1.6	3.3	ns/pF
Δt_{PHL}				0.4	0.6	1.4	0.4	0.6	1.2	
Δt_{PLH}	B1	Y		0.9	2	4.7	1	2	4.2	ns/pF
Δt_{PHL}				0.5	0.8	2.1	0.5	0.8	1.8	
Δt_{PLH}	C1	Y		1.1	2.5	5.8	1.2	2.5	5.2	ns/pF
Δt_{PHL}				0.5	1	2.5	0.5	1	2.2	
Δt_{PLH}	Any D	Y		1.4	3	6.9	1.5	3	6.3	ns/pF
Δt_{PHL}				0.6	1.4	3.6	0.7	1.4	3.1	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

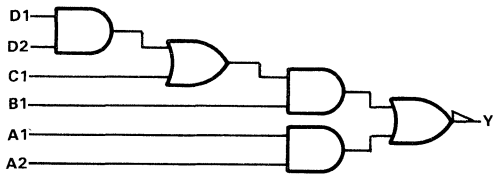
Refer to the 'ASC6017 data sheet and Section 7.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SystemCell™ 2-μm INTERNAL STANDARD CELL

- Typical Propagation Delay with 1-pF Load
  - 2.3 ns from Any A or B1
  - 3 ns from C1
  - 3.6 ns from Any D
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol



positive logic equation

$$Y = \overline{(A1 \cdot A2) + \{B1 \cdot [C1 + (D1 \cdot D2)]\}}$$

FUNCTION TABLE

INPUTS						OUTPUT
A1	A2	B1	C1	D1	D2	Y
H	H	X	X	X	X	L
X	X	H	H	X	X	L
X	X	H	X	H	H	L
Any other combination						H

description

The SN54ASC6034 and SN74ASC6034 CMOS standard-cell Boolean macros are 2-wide 2-2-input sum-of-products AND-NOR gates with 2-input AND and one available input each to the 2-input AND and OR gates to provide expandability for implementing customized product terms. The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
BF034LH	Label: BF034LH A1,A2,B1,C1,D1,D2,Y;	2.25

The SN54ASC6034 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6034 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		V
I_{CC}	Supply current	SN54ASC6034	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		280	nA
		SN74ASC6034			16.8	
C_i	Input capacitance		V_{CC} = 5 V, T_A = 25°C	0.13		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, t_r = t_f = 3 ns, T_A = 25°C	0.86		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6034			SN74ASC6034			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Any A	Y	C_L = 0	0.8	0.9	1.7	0.8	0.9	1.6	ns
t_{PHL}				0.3	0.9	1.5	0.3	0.9	1.5	
t_{PLH}	Any A	Y	C_L = 1 pF	1.5	2.5	5.3	1.6	2.5	4.9	ns
t_{PHL}				0.8	1.8	3.9	0.9	1.8	3.5	
t_{PLH}	B1	Y	C_L = 0	0.7	1	2	0.7	1	1.8	ns
t_{PHL}				0.6	1.2	2.1	0.7	1.2	2	
t_{PLH}	B1	Y	C_L = 1 pF	1.4	2.5	5.5	1.5	2.5	5	ns
t_{PHL}				1.1	2	4.2	1.2	2	3.8	
t_{PLH}	C1	Y	C_L = 0	0.9	1.7	3.8	0.9	1.7	3.5	ns
t_{PHL}				0.6	1.2	2.6	0.6	1.2	2.3	
t_{PLH}	C1	Y	C_L = 1 pF	1.9	3.7	8.4	2	3.7	7.7	ns
t_{PHL}				1.1	2.2	5.2	1.2	2.2	4.5	
t_{PLH}	Any D	Y	C_L = 0	1	1.9	4.4	1	1.9	4	ns
t_{PHL}				0.5	1.4	3.1	0.6	1.4	2.7	
t_{PLH}	Any D	Y	C_L = 1 pF	2.2	4.4	10.1	2.3	4.4	9.2	ns
t_{PHL}				1.2	2.7	6.7	1.3	2.7	5.8	
Δt_{PLH}	Any A	Y		0.7	1.6	3.7	0.8	1.6	3.3	ns/pF
Δt_{PHL}				0.5	0.9	2.4	0.5	0.9	2	
Δt_{PLH}	B1	Y		0.7	1.5	3.5	0.7	1.5	3.2	ns/pF
Δt_{PHL}				0.5	0.8	2.2	0.5	0.8	1.9	
Δt_{PLH}	C1	Y		0.9	2	4.6	1	2	4.2	ns/pF
Δt_{PHL}				0.5	1	2.6	0.5	1	2.3	
Δt_{PLH}	Any D	Y		1.2	2.5	5.8	1.3	2.5	5.3	ns/pF
Δt_{PHL}				0.6	1.3	3.6	0.6	1.3	3.1	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to the 'ASC6017 data sheet and Section 7.

TEXAS INSTRUMENTS
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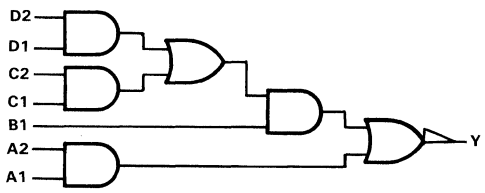
SystemCell™ 2-μm INTERNAL STANDARD CELL

- **Typical Propagation Delay with 1-pF Load**
  - **2.1 ns from Any A**
  - **2.3 ns from B1**
  - **3.3 ns from Any C or D**
- **Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V**
- **Functional Operation Over V_{CC} Range of 2 V to 6 V**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol



FUNCTION TABLE

INPUTS							OUTPUT
A1	A2	B1	C1	C2	D1	D2	Y
H	H	X	X	X	X	X	L
X	X	H	H	H	X	X	L
X	X	H	X	X	H	H	L
Any other combination							H

positive logic equation

$$Y = \overline{(A1 \cdot A2) + \{B1 \cdot [(C1 \cdot C2) + (D1 \cdot D2)]\}}$$

description

The SN54ASC6035 and SN74ASC6035 CMOS standard-cell Boolean macros are expandable sum-of-products AND-OR-AND-NOR gates for implementing customized product terms. The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
BF035LH	Label: BF035LH A1,A2,B1,C1,C2,D1,D2,Y;	2.25

The SN54ASC6035 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6035 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER		TEST CONDITIONS		TYP	MAX	UNIT
V_T Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		V
I_{CC} Supply current	SN54ASC6035	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0,			282	nA
	SN74ASC6035	T_A = MIN to MAX			16.9	
C_i Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.13		pF
C_{pd} Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	$t_r = t_f$ = 3 ns,	0.96		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6035			SN74ASC6035			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Any A	Y	C_L = 0	0.7	1	1.7	0.7	1	1.6	ns
t_{PHL}				0.3	0.8	1.6	0.3	0.8	1.5	
t_{PLH}	Any A	Y	C_L = 1 pF	1.4	2.4	5	1.5	2.4	4.6	ns
t_{PHL}				0.8	1.8	3.9	0.9	1.8	3.5	
t_{PLH}	B1	Y	C_L = 0	0.7	1	2	0.7	1	1.8	ns
t_{PHL}				0.7	1.2	2.3	0.7	1.2	2.1	
t_{PLH}	B1	Y	C_L = 1 pF	1.4	2.4	5.3	1.4	2.4	4.8	ns
t_{PHL}				1.2	2.1	4.6	1.3	2.1	4.1	
t_{PLH}	Any C or D	Y	C_L = 0	0.9	1.8	4.5	0.9	1.8	4.1	ns
t_{PHL}				0.5	1.5	3.8	0.6	1.5	3.3	
t_{PLH}	Any C or D	Y	C_L = 1 pF	1.8	3.8	9.1	2	3.8	8.3	ns
t_{PHL}				1.2	2.8	7.3	1.3	2.8	6.3	
Δt_{PLH}	Any A	Y		0.6	1.4	3.4	0.7	1.4	3	ns/pF
Δt_{PHL}				0.5	1	2.4	0.5	1	2	
Δt_{PLH}	B1	Y		0.6	1.4	3.3	0.7	1.4	3	ns/pF
Δt_{PHL}				0.5	0.9	2.4	0.5	0.9	2.1	
Δt_{PLH}	Any C or D	Y		0.9	2	4.6	1	2	4.2	ns/pF
Δt_{PHL}				0.6	1.3	3.6	0.6	1.3	3.1	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

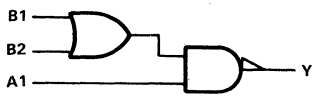
Refer to the 'ASC6017 data sheet and Section 7.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SystemCell™ 2-μm INTERNAL STANDARD CELL

- **Typical Propagation Delay with 1-pF Load**
  1.9 ns from A1
  2.4 ns from Either B
- **Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V**
- **Functional Operation Over V_{CC} Range of 2 V to 6 V**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol



FUNCTION TABLE

INPUTS			OUTPUT
A1	B1	B2	Y
H	H	X	L
H	X	H	L
L	X	X	H
X	L	L	H

positive logic equation

$$Y = \overline{A1 \cdot (B1 + B2)}$$

description

The SN54ASC6048 and SN74ASC6048 are 2-wide, 1-2-input OR-NAND gate CMOS standard-cell functions. The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
BF051LH	Label: BF051LH A1,B1,B2,Y;	1.5

The SN54ASC6048 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6048 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS		TYP	MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		V
I_{CC}	Supply current	SN54ASC6048	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0,			187	nA
		SN74ASC6048	T_A = MIN to MAX			11.2	
C_i	Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.13		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	$t_r = t_f$ = 3 ns,	0.57		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6048			SN74ASC6048			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A1	Y	C_L = 0	0.6	0.8	1.2	0.7	0.8	1.2	ns
t_{PHL}				0.6	1.1	1.8	0.6	1.1	1.7	
t_{PLH}	A1	Y	C_L = 1 pF	1.1	1.8	3.5	1.2	1.8	3.2	ns
t_{PHL}				1.1	2	4.2	1.2	2	3.8	
t_{PLH}	Any B	Y	C_L = 0	0.7	1.1	2.4	0.8	1.1	2.2	ns
t_{PHL}				0.3	0.8	1.7	0.3	0.8	1.5	
t_{PLH}	Any B	Y	C_L = 1 pF	1.7	3.1	6.9	1.8	3.1	6.3	ns
t_{PHL}				0.8	1.7	4.1	0.9	1.7	3.6	
Δt_{PLH}	A1	Y		0.5	1	2.3	0.5	1	2.1	ns/pF
Δt_{PHL}				0.5	0.9	3.5	0.5	0.9	2.1	
Δt_{PLH}	Any B	Y		0.9	2	4.6	1	2	4.1	ns/pF
Δt_{PHL}				0.5	0.9	2.5	0.5	0.9	2.1	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to the 'ASC6017 data sheet and Section 7.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

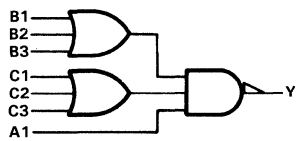
SystemCell™ 2-μm INTERNAL STANDARD CELL

- Typical Propagation Delay with 1-pF Load
  2.3 ns from A1
  3.8 ns from Any B or C
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

positive logic equation

$$Y = \overline{A1 \cdot (B1 + B2 + B3) \cdot (C1 + C2 + C3)}$$

logic symbol



FUNCTION TABLE

INPUTS							OUTPUT
A1	B1	B2	B3	C1	C2	C3	Y
H	H	X	X	H	X	X	L
H	X	H	X	X	H	X	L
H	X	X	H	X	X	H	L
H	(Any H)			(Any H)			L
Any other combination							H

description

The SN54ASC6049 and SN74ASC6049 are 3-wide 1-3-3-input OR-NAND gate CMOS standard-cell functions.The cells are designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
BF060LH	Label: BF060LH A1,B1,B2,B3,C1,C2,C3,Y;	2.25

The SN54ASC6049 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6049 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER		TEST CONDITIONS		TYP	MAX	UNIT
V_T Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		V
I_{CC} Supply current	SN54ASC6049	V_{CC} = 4.5 V to 5.5 V,	V_I = V_{CC} or 0		301	nA
	SN74ASC6049	T_A = MIN to MAX			18	
C_i Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.13		pF
C_{pd} Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	$t_r = t_f$ = 3 ns,	0.65		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6049			SN74ASC6049			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A1	Y	C_L = 0	0.6	0.8	1.4	0.6	0.8	1.3	ns
t_{PHL}				0.9	1.4	2.7	0.9	1.4	2.4	
t_{PLH}	A1	Y	C_L = 1 pF	1.1	1.8	3.6	1.2	1.8	3.3	ns
t_{PHL}				1.5	2.7	6.2	1.6	2.7	5.4	
t_{PLH}	Any B or C	Y	C_L = 0	1	2	5.8	1	2	5.2	ns
t_{PHL}				0.4	1.3	3.8	0.5	1.3	3.3	
t_{PLH}	Any B or C	Y	C_L = 1 pF	2.4	5	12.6	2.6	5	11.4	ns
t_{PHL}				1	2.6	7.3	1.1	2.6	6.4	
Δt_{PLH}	A1	Y		0.5	1	2.3	0.5	1	2.1	ns/pF
Δt_{PHL}				0.6	1.3	3.5	0.6	1.3	3.1	
Δt_{PLH}	Any B or C	Y		1.4	3	6.9	1.5	3	6.2	ns/pF
Δt_{PHL}				0.6	1.3	3.6	0.6	1.3	3.1	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

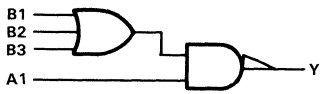
Refer to the 'ASC6017 data sheet and Section 7.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SystemCell™ 2-μm INTERNAL STANDARD CELL

- Typical Propagation Delay with 1-pF Load
  1.9 ns from A1
  3.2 ns from Any B
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol



FUNCTION TABLE

INPUTS				OUTPUT
A1	B1	B2	B3	Y
H	H	X	X	L
H	X	H	X	L
H	X	X	H	L
L	X	X	X	H
X	L	L	L	H

positive logic equation

$$Y = \overline{A \cdot (B1 + B2 + B3)}$$

description

The SN54ASC6052 and SN74ASC6052 are 2-wide, 1-3-input OR-NAND gate CMOS standard-cell functions. The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
BF052LH	Label: BF052LH A1,B1,B2,B3,Y;	1.5

The SN54ASC6052 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6052 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER		TEST CONDITIONS		TYP	MAX	UNIT
V_T Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		V
I_{CC} Supply current	SN54ASC6052	V_{CC} = 4.5 V to 5.5 V,	V_I = V_{CC} or 0,		204	nA
	SN74ASC6052	T_A = MIN to MAX			12.3	
C_i Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.13		pF
C_{pd} Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	$t_r = t_f$ = 3 ns,	3.57		pF

4 Data Sheets

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6052			SN74ASC6052			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A1	Y	C_L = 0	0.6	0.8	1.2	0.7	0.8	1.2	ns
t_{PHL}				0.6	1.1	2	0.7	1.1	1.8	
t_{PLH}	A1	Y	C_L = 1 pF	1.1	1.8	3.5	1.2	1.8	3.2	ns
t_{PHL}				1.2	2	4.4	1.2	2	4	
t_{PLH}	Any B	Y	C_L = 0	0.9	1.6	3.8	0.9	1.6	3.4	ns
t_{PHL}				0.3	0.8	1.8	0.3	0.8	1.7	
t_{PLH}	Any B	Y	C_L = 1 pF	2.3	4.6	10.6	2.4	4.6	9.6	ns
t_{PHL}				0.8	1.8	4.3	0.9	1.8	3.8	
Δt_{PLH}	A1	Y		0.5	1	2.3	0.5	1	2.1	ns/pF
Δt_{PHL}				0.5	0.9	2.5	0.5	0.9	2.2	
Δt_{PLH}	Any B	Y		1.4	3	6.9	1.5	3	6.2	ns/pF
Δt_{PHL}				0.5	1	2.5	0.5	1	2.2	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

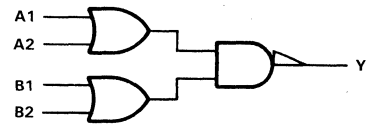
Refer to the 'ASC6017 data sheet and Section 7.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SystemCell™ 2-μm INTERNAL STANDARD CELL

- **2.6 ns Typical Propagation Delay with 1-pF Load**
- **Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V**
- **Functional Operation Over V_{CC} Range of 2 V to 6 V**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol



FUNCTION TABLE

INPUTS				OUTPUT
A1	A2	B1	B2	Y
H	X	H	X	L
H	X	X	H	L
X	H	H	X	L
X	H	X	H	L
L	L	X	X	H
X	X	L	L	H

positive logic equation

$$Y = \overline{(A1 + A2) \cdot (B1 + B2)}$$

description

The SN54ASC6053 and SN74ASC6053 are 2-wide, 2-input OR-NAND gate CMOS standard-cell functions. The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		TYPICAL DELAY C_L = 1 pF	RELATIVE CELL AREA TO NA210LH
BF053LH	Label: BF053LH A1,A2,B1,B2,Y;	2.6 ns	1.75

The SN54ASC6053 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6053 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER		TEST CONDITIONS		TYP	MAX	UNIT
V_T Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		V
I_{CC} Supply current	SN54ASC6053	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0			220	nA
	SN74ASC6053	T_A = MIN to MAX			13.2	
C_i Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.13		pF
C_{pd} Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	$t_r = t_f$ = 3 ns,	0.49		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6053			SN74ASC6053			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Any	Y	C_L = 0	0.7	1.1	2.7	0.7	1.1	2.4	ns
t_{PHL}				0.5	1	2.1	0.5	1	2	
t_{PLH}	Any	Y	C_L = 1 pF	1.6	3.1	7.2	1.7	3.1	6.5	ns
t_{PHL}				0.8	2	4.6	0.9	2	4.1	
Δt_{PLH}	Any	Y		0.9	2	4.6	1	2	4.2	ns/pF
Δt_{PHL}				0.5	1	2.5	0.5	1	2.1	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

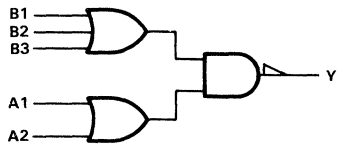
Refer to the 'ASC6017 data sheet and Section 7.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SystemCell™ 2-μm INTERNAL STANDARD CELL

- 3 ns Typical Propagation Delay with 1-pF Load
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol



positive logic equation

$$Y = \overline{(A1 + A2) \cdot (B1 + B2 + B3)}$$

description

The SN54ASC6054 and SN74ASC6054 are 2-wide, 2-3-input OR-NAND gate CMOS standard-cell functions. The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

FUNCTION TABLE

INPUTS					OUTPUT
A1	A2	B1	B2	B3	Y
H	X	H	X	X	L
H	X	X	H	X	L
H	X	X	X	H	L
X	H	H	X	X	L
X	H	X	H	X	L
X	H	X	X	H	L
Any other combination					H

CELL NAME	NETLIST HDL LABEL	FEATURES	
		TYPICAL DELAY C_L = 1 pF	RELATIVE CELL AREA TO NA210LH
BF054LH	Label: BF054LH A1,A2,B1,B2,B3,Y;	3 ns	1.75

The SN54ASC6054 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6054 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER		TEST CONDITIONS		TYP	MAX	UNIT
V_T Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		V
I_{CC} Supply current	SN54ASC6054	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0,			237	nA
	SN74ASC6054	T_A = MIN to MAX			14.2	
C_i Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.13		pF
C_{pd} Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	$t_r = t_f$ = 3 ns,	0.47		pF

4 Data Sheets

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6054			SN74ASC6054			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Any	Y	C_L = 0	0.7	1.4	4.2	0.7	1.4	3.8	ns
t_{PHL}				0.3	1	2.4	0.3	1	2.1	
t_{PLH}	Any	Y	C_L = 1 pF	1.6	4	11	1.7	4	10	ns
t_{PHL}				0.8	2	4.8	0.9	2	4.3	
Δt_{PLH}	Any	Y		0.9	2.6	6.9	1	2.6	6.2	ns/pF
Δt_{PHL}				0.5	1	2.5	0.5	1	2.2	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

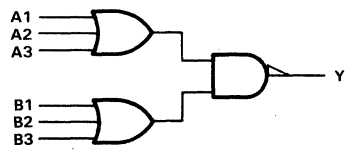
Refer to the 'ASC6017 data sheet and Section 7.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SystemCell™ 2-μm INTERNAL STANDARD CELL

- 3.3 ns Typical Propagation Delay with 1-pF Load
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol



positive logic equation

$$Y = \overline{(A1 + A2 + A3) \cdot (B1 + B2 + B3)}$$

description

The SN54ASC6055 and SN74ASC6055 are 2-wide, 3-input OR-NAND gate CMOS standard-cell functions. The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

FUNCTION TABLE

INPUTS						OUTPUT
A1	A2	A3	B1	B2	B3	Y
H	X	X	H	X	X	L
H	X	X	X	H	X	L
H	X	X	X	X	H	L
X	H	X	H	X	X	L
X	H	X	X	H	X	L
X	H	X	X	X	H	L
X	X	H	H	X	X	L
X	X	H	X	H	X	L
X	X	H	X	X	H	L
Any other combination						H

CELL NAME	NETLIST HDL LABEL	FEATURES	
		TYPICAL DELAY C_L = 1 pF	RELATIVE CELL AREA TO NA210LH
BF055LH	Label: BF055LH A1,A2,A3,B1,B2,B3,Y;	3.3 ns	2

The SN54ASC6055 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6055 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS		TYP	MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		V
I_{CC}	Supply current	SN54ASC6055	V_{CC} = 4.5 V to 5.5 V,	V_I = V_{CC} or 0,		266	nA
		SN74ASC6055	T_A = MIN to MAX			15.9	
C_i	Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.13		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	$t_r = t_f$ = 3 ns,	0.51		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6055			SN74ASC6055			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Any	Y	C_L = 0	0.8	1.6	4.5	0.8	1.6	4.1	ns
t_{PHL}				0.3	1	2.6	0.4	1	2.4	
t_{PLH}	Any	Y	C_L = 1 pF	2.2	4.6	11.3	2.4	4.6	10.3	ns
t_{PHL}				0.8	2	5.1	0.9	2	4.5	
Δt_{PLH}	Any	Y		1.4	3	7	1.5	3	6.3	ns/pF
Δt_{PHL}				0.5	1	2.6	0.5	1	2.2	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to the 'ASC6017 data sheet and Section 7.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

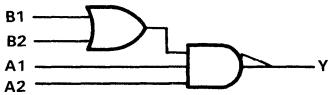
SystemCell™ 2-μm INTERNAL STANDARD CELL

- Typical Propagation Delay with 1-pF Load
  2.2 ns from Any A
  2.9 ns from Any B
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

positive logic equation

$$Y = \overline{A1 \cdot A2 \cdot (B1 + B2)}$$

logic symbol



FUNCTION TABLE

INPUTS				OUTPUT
A1	A2	B1	B2	Y
H	H	H	X	L
H	H	X	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	L	H

description

The SN54ASC6056 and SN74ASC6056 are 3-wide, 1-1-2-input OR-NAND gate CMOS standard-cell functions. The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
BF056LH	Label: BF056LH A1,A2,B1,B2,Y;	1.75

The SN54ASC6056 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6056 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS		TYP	MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		V
I_{CC}	Supply current	SN54ASC6056	V_{CC} = 4.5 V to 5.5 V,	$V_I = V_{CC}$ or 0,		220	nA
		SN74ASC6056	T_A = MIN to MAX			13.2	
C_i	Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.13		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	$t_r = t_f$ = 3 ns,	0.55		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6056			SN74ASC6056			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Any A	Y	C_L = 0	0.6	0.9	1.6	0.6	0.9	1.5	ns
t_{PHL}				0.7	1.2	2.4	0.7	1.2	2.2	
t_{PLH}	Any A	Y	C_L = 1 pF	1.1	1.9	3.8	1.2	1.9	3.5	ns
t_{PHL}				1.3	2.5	5.9	1.4	2.5	5.1	
t_{PLH}	Any B	Y	C_L = 0	0.8	1.4	3.2	0.9	1.4	2.9	ns
t_{PHL}				0.4	1	2.4	0.4	1	2.2	
t_{PLH}	Any B	Y	C_L = 1 pF	1.8	3.4	7.7	1.9	3.4	7	ns
t_{PHL}				1	2.3	5.9	1.1	2.3	5.1	
Δt_{PLH}	Any A	Y		0.5	1	2.3	0.5	1	2.1	ns/pF
Δt_{PHL}				0.6	1.3	3.5	0.6	1.3	3	
Δt_{PLH}	Any B	Y		0.9	2	4.6	1	2	4.1	ns/pF
Δt_{PHL}				0.6	1.3	3.5	0.6	1.3	3	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

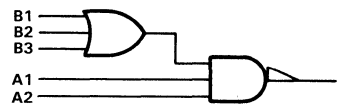
Refer to the 'ASC6017 data sheet and Section 7.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SystemCell™ 2-μm INTERNAL STANDARD CELL

- **Typical Propagation Delay with 1-pF Load**
  2.8 ns from Any A
  3.7 ns from Any B
- **Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V**
- **Functional Operation Over V_{CC} Range of 2 V to 6 V**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol



FUNCTION TABLE

INPUTS					OUTPUT
A1	A2	B1	B2	B3	Y
H	H	H	X	X	L
H	H	X	H	X	L
H	H	X	X	H	L
L	X	X	X	X	H
X	L	X	X	X	H
X	X	L	L	L	H

positive logic equation

$$Y = \overline{A1 \cdot A2 \cdot (B1 + B2 + B3)}$$

description

The SN54ASC6057 and SN74ASC6057 are 3-wide, 1-1-3-input OR-NAND gate CMOS standard-cell functions. The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
BF057LH	Label: BF057LH A1,A2,B1,B2,B3,Y;	1.75

The SN54ASC6057 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6057 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER		TEST CONDITIONS		TYP	MAX	UNIT
V_T Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		V
I_{CC} Supply current	SN54ASC6057	V_{CC} = 4.5 V to 5.5 V,	V_I = V_{CC} or 0,		237	nA
	SN74ASC6057	T_A = MIN to MAX			14.2	
C_i Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.13		pF
C_{pd} Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	0.58		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6057			SN74ASC6057			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Any A	Y	C_L = 0	0.6	0.9	1.6	0.6	0.9	1.5	ns
t_{PHL}				0.7	1.3	2.8	0.8	1.3	2.5	
t_{PLH}	Any A	Y	C_L = 1 pF	1.1	1.9	3.8	1.2	1.9	3.5	ns
t_{PHL}				1.3	2.6	6.3	1.4	2.6	5.5	
t_{PLH}	Any B	Y	C_L = 0	1	2	5	1.1	2	4.5	ns
t_{PHL}				0.4	1	2.8	0.4	1	2.4	
t_{PLH}	Any B	Y	C_L = 1 pF	2.4	5	11.9	2.6	5	10.7	ns
t_{PHL}				1	2.3	6.3	1.1	2.3	5.4	
Δt_{PLH}	Any A	Y		0.5	1	2.3	0.5	1	2.1	ns/pF
Δt_{PHL}				0.6	1.3	3.6	0.6	1.3	3.1	
Δt_{PLH}	Any B	Y		1.4	3	6.9	1.5	3	6.2	ns/pF
Δt_{PHL}				0.6	1.3	3.5	0.6	1.3	3.1	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

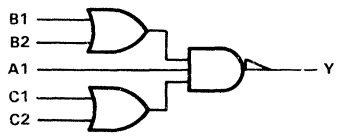
Refer to the 'ASC6017 data sheet and Section 7.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SystemCell™ 2-μm INTERNAL STANDARD CELL

- Typical Propagation Delay with 1-pF Load
  2.3 ns from A1
  3 ns from Any B or C
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol



FUNCTION TABLE

INPUTS					OUTPUT
A1	B1	B2	C1	C2	Y
H	H	X	H	X	L
H	H	X	X	H	L
H	X	H	H	X	L
H	X	H	X	H	L
L	X	X	X	X	H
X	L	L	X	X	H
X	X	X	L	L	H

positive logic equation

$$Y = \overline{A1 \cdot (B1 + B2) \cdot (C1 + C2)}$$

description

The SN54ASC6058 and SN74ASC6058 are 3-wide, 1-2-2-input OR-NAND gate CMOS standard-cell functions. The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
BF058LH	Label: BF058LH A1,B1,B2,C1,C2,Y;	2

The SN54ASC6058 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6058 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER		TEST CONDITIONS		TYP	MAX	UNIT
V_t Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		V
I_{CC} Supply current	SN54ASC6058	V_{CC} = 4.5 V to 5.5 V,	$V_I = V_{CC}$ or 0,		250	nA
	SN74ASC6058	T_A = MIN to MAX			15	
C_i Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.13		pF
C_{pd} Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	$t_r = t_f$ = 3 ns,	0.64		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6058			SN74ASC6058			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A1	Y	C_L = 0	0.8	1	1.8	0.8	1	1.7	ns
t_{PHL}				0.8	1.3	3.1	0.8	1.3	2.7	
t_{PLH}	A1	Y	C_L = 1 pF	1.3	2	4	1.3	2	3.7	ns
t_{PHL}				1.4	2.6	6.5	1.5	2.6	5.7	
t_{PLH}	Any B or C	Y	C_L = 0	0.7	1.3	3.5	0.7	1.3	3.2	ns
t_{PHL}				0.5	1.3	2.8	0.5	1.3	2.7	
t_{PLH}	Any B or C	Y	C_L = 1 pF	1.6	3.3	8	1.7	3.3	7.3	ns
t_{PHL}				1.1	2.6	6.3	1.2	2.6	5.7	
Δt_{PLH}	A1	Y		0.4	1	2.3	0.5	1	2.1	ns/pF
Δt_{PHL}				0.6	1.3	3.5	0.6	1.3	3	
Δt_{PLH}	Any B or C	Y		0.9	2	4.6	1	2	4.2	ns/pF
Δt_{PHL}				0.6	1.3	3.5	0.6	1.3	3	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

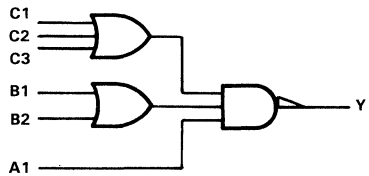
Refer to the 'ASC6017 data sheet and Section 7.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SystemCell™ 2-μm INTERNAL STANDARD CELL

- **Typical Propagation Delay with 1-pF Load**
  2.3 ns from A1
  3.5 ns from Any B or C
- **Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V**
- **Functional Operation Over V_{CC} Range of 2 V to 6 V**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol



positive logic equation

$$Y = \overline{A1 \cdot (B1 + B2) \cdot (C1 + C2 + C3)}$$

description

The SN54ASC6059 and SN74ASC6059 are 3-wide, 1-2-3-input OR-NAND gate CMOS standard-cell functions. The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

FUNCTION TABLE

INPUTS						OUTPUT
A1	B1	B2	C1	C2	C3	Y
H	H	X	H	X	X	L
H	H	X	X	H	X	L
H	H	X	X	X	H	L
H	X	H	H	X	X	L
H	X	H	X	H	X	L
H	X	H	X	X	H	L
L	X	X	X	X	X	H
X	L	L	X	X	X	H
X	X	X	L	L	L	H

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
BF059LH	Label: BF059LH A1,B1,B2,C1,C2,C3,Y;	2.25

The SN54ASC6059 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6059 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER		TEST CONDITIONS		TYP	MAX	UNIT
V_T Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		V
I_{CC} Supply current	SN54ASC6059	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0,			284	nA
	SN74ASC6059	T_A = MIN to MAX			17	
C_i Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.13		pF
C_{pd} Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	$t_r = t_f$ = 3 ns,	0.65		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6059			SN74ASC6059			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A1	Y	C_L = 0	0.6	0.8	1.4	0.6	0.8	1.3	ns
t_{PHL}				0.8	1.3	2.3	0.8	1.3	2.1	
t_{PLH}	A1	Y	C_L = 1 pF	1.1	1.8	3.6	1.2	1.8	3.3	ns
t_{PHL}				1.4	2.6	5.8	1.5	2.6	5.1	
t_{PLH}	Any B or C	Y	C_L = 0	0.9	1.8	4.8	1	1.8	4.3	ns
t_{PHL}				0.4	1.3	3.4	0.5	1.3	3	
t_{PLH}	Any B or C	Y	C_L = 1 pF	1.9	4.4	11.6	2	4.4	10.5	ns
t_{PHL}				1.1	2.6	6.9	1.2	2.6	6	
Δt_{PLH}	A1	Y		0.5	1	2.3	0.5	1	2.1	ns/pF
Δt_{PHL}				0.6	1.3	3.5	0.6	1.3	3	
Δt_{PLH}	Any B or C	Y		0.9	2.6	6.9	1	2.6	6.2	ns/pF
Δt_{PHL}				0.6	1.3	3.6	0.6	1.3	3.1	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to the 'ASC6017 data sheet and Section 7.

TEXAS INSTRUMENTS
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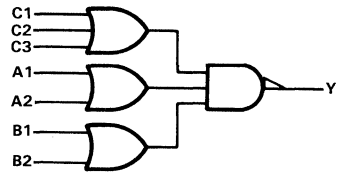
$$Y = \overline{(A1 + A2) \cdot (B1 + B2) \cdot (C1 + C2 + C3)}$$

D2939, AUGUST 1986

SystemCell™ 2-μm INTERNAL STANDARD CELL

- 4.1 ns Typical Propagation Delay with 1-pF Load
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol



positive logic equation

$$Y = \overline{(A1 + A2) \cdot (B1 + B2) \cdot (C1 + C2 + C3)}$$

FUNCTION TABLE

INPUTS							OUTPUT
A1	A2	B1	B2	C1	C2	C3	Y
H	X	H	X	H	X	X	L
X	H	X	H	X	H	X	L
H	X	H	X	X	X	H	L
(Any H)		(Any H)		(Any H)			L
Any other combination							H

description

The SN54ASC6062 and SN74ASC6062 are 3-wide, 2-2-3-input OR-NAND gate CMOS standard cell functions. The cells are designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		TYPICAL DELAY C_L = 1 pF	RELATIVE CELL AREA TO NA210LH
BF062LH	Label: BF062LH A1,A2,B1,B2,C1,C2,C3,Y;	4.1 ns	2.5

The SN54ASC6062 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6062 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER		TEST CONDITIONS		TYP	MAX	UNIT
V_T Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		V
I_{CC} Supply current	SN54ASC6062	V_{CC} = 4.5 V to 5.5 V,	V_I = V_{CC} or 0,		312	nA
	SN74ASC6062	T_A = MIN to MAX			18.7	
C_i Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.13		pF
C_{pd} Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	$t_r = t_f$ = 3 ns,	0.65		pF

4 Data Sheets

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6062			SN74ASC6062			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Any A or B	Y	C_L = 0	0.6	1.4	4	0.7	1.4	3.6	ns
t_{PHL}				0.5	1.3	3.3	0.6	1.3	2.9	
t_{PLH}	Any A or B	Y	C_L = 1 pF	1.6	3.3	8.5	1.7	3.3	7.7	ns
t_{PHL}				1.1	2.6	6.7	1.3	2.6	5.8	
t_{PLH}	Any C	Y	C_L = 0	1.1	2.1	5.3	1.1	2.1	4.7	ns
t_{PHL}				0.7	1.6	4	0.8	1.6	3.5	
t_{PLH}	Any C	Y	C_L = 1 pF	2.5	5.1	12.2	2.7	5.1	11	ns
t_{PHL}				1.4	3	7.6	1.5	3	6.5	
Δt_{PLH}	Any A or B	Y		0.9	2	4.6	1	2	4.2	ns/pF
Δt_{PHL}				0.6	1.3	3.5	0.6	1.3	3	
Δt_{PLH}	Any C	Y		1.4	3	6.9	1.5	3	6.3	ns/pF
Δt_{PHL}				0.6	1.4	3.6	0.6	1.4	3.1	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

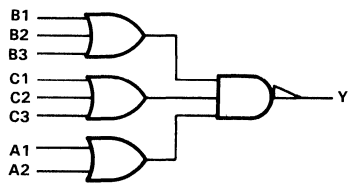
Refer to the 'ASC6017 data sheet and Section 7.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SystemCell™ 2-μm INTERNAL STANDARD CELL

- 4.2 ns Typical Propagation Delay with 1-pF Load
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol



positive logic equation

$$Y = \overline{(A1 + A2) \cdot (B1 + B2 + B3) \cdot (C1 + C2 + C3)}$$

FUNCTION TABLE

INPUTS								OUTPUT
A1	A2	B1	B2	B3	C1	C2	C3	Y
H	X	H	X	X	H	X	X	L
X	H	X	H	X	X	H	X	L
H	X	X	X	H	X	X	H	L
(Any H)		(Any H)			(Any H)			L
Any other combination								H

description

The SN54ASC6063 and SN74ASC6063 are 3-wide, 2-3-3-input OR-NAND gate CMOS standard cell functions. The cells are designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		TYPICAL DELAY C_L = 1 pF	RELATIVE CELL AREA TO NA210LH
BF063LH	Label: BF063LH A1,A2,B1,B2,B3,C1,C2,C3,Y;	4.2 ns	2.5

The SN54ASC6063 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6063 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS		TYP	MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		V
I_{CC}	Supply current	SN54ASC6063	V_{CC} = 4.5 V to 5.5 V,	V_I = V_{CC} or 0,		330	nA
		SN74ASC6063	T_A = MIN to MAX			19.8	
C_i	Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.13		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	$t_r = t_f$ = 3 ns,	0.64		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6063			SN74ASC6063			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Any A	Y	C_L = 0	0.6	1	2.2	0.7	1	2	ns
t_{PHL}				0.8	1.4	3.1	0.9	1.4	2.8	
t_{PLH}	Any A	Y	C_L = 1 pF	1.6	3	6.7	1.7	3	6.1	ns
t_{PHL}				1.5	2.7	6.6	1.6	2.7	5.8	
t_{PLH}	Any B or C	Y	C_L = 0	1.1	2.4	6.3	1.1	2.4	5.7	ns
t_{PHL}				0.6	1.6	4.4	0.6	1.6	3.8	
t_{PLH}	Any B or C	Y	C_L = 1 pF	2.5	5.4	13.1	2.7	5.4	11.9	ns
t_{PHL}				1.1	3	8	1.2	3	6.9	
Δt_{PLH}	Any A	Y		0.9	2	4.6	1	2	4.2	ns/pF
Δt_{PHL}				0.6	1.3	3.6	0.6	1.3	3.1	
Δt_{PLH}	Any B or C	Y		1.4	3	6.9	1.5	3	6.3	ns/pF
Δt_{PHL}				0.6	1.4	3.6	0.6	1.4	3.1	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to the 'ASC6017 data sheet and Section 7.

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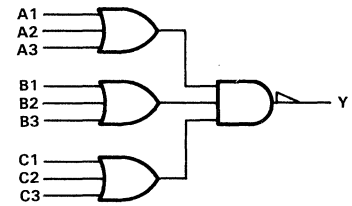
$$Y = \overline{(A1 + A2 + A3) \cdot (B1 + B2 + B3) \cdot (C1 + C2 + C3)}$$

D2939, AUGUST 1986

SystemCell™ 2-μm INTERNAL STANDARD CELL

- 4.1 ns Typical Propagation Delay with 1-pF Load
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol



positive logic equation

$$Y = \overline{(A1 + A2 + A3) \cdot (B1 + B2 + B3) \cdot (C1 + C2 + C3)}$$

description

The SN54ASC6064 and SN74ASC6064 are 3-wide, 3-input OR-NAND gate CMOS standard-cell functions. The cells are designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

FUNCTION TABLE

INPUTS									OUTPUT
A1	A2	A3	B1	B2	B3	C1	C2	C3	Y
H	X	X	H	X	X	H	X	X	L
X	H	X	X	H	X	X	H	X	L
X	X	H	X	X	H	X	X	H	L
(Any H)			(Any H)			(Any H)			L
Any other combination									H

CELL NAME	NETLIST HDL LABEL	FEATURES	
		TYPICAL DELAY C_L = 1 pF	RELATIVE CELL AREA TO NA210LH
BF064LH	Label: BF064LH A1,A2,A3,B1,B2,B3,C1,C2,C3,Y;	4.1 ns	2.75

The SN54ASC6064 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6064 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS		TYP	MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		V
I_{CC}	Supply current	SN54ASC6064	V_{CC} = 4.5 V to 5.5 V,	V_I = V_{CC} or 0,		363	nA
		SN74ASC6064	T_A = MIN to MAX			21.8	
C_i	Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.13		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	$t_r = t_f$ = 3 ns,	0.7		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6064			SN74ASC6064			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Any	Y	C_L = 0	0.8	2.2	6.8	0.8	2.2	6.1	ns
t_{PHL}				0.6	1.6	5	0.7	1.6	4.4	
t_{PLH}	Any	Y	C_L = 1 pF	2.2	5.2	13.6	2.4	5.2	12.3	ns
t_{PHL}				1.2	3	8.6	1.3	3	7.4	
Δt_{PLH}	Any	Y		1.4	3	6.9	1.5	3	6.3	ns/pF
Δt_{PHL}				0.6	1.4	3.6	0.6	1.4	3.1	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to the 'ASC6017 data sheet and Section 7.

TEXAS INSTRUMENTS
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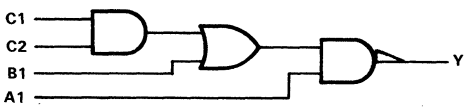
SystemCell™ 2-μm INTERNAL STANDARD CELL

- **Typical Propagation Delay with 1-pF Load**
  - **2.2 ns from A1**
  - **2.4 ns from B1**
  - **2.8 ns from Any C**
- **Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V**
- **Functional Operation Over V_{CC} Range of 2 V to 6 V**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol



FUNCTION TABLE

INPUTS				OUTPUT
A1	B1	C1	C2	Y
H	H	X	X	L
H	X	H	H	L
L	X	X	X	H
X	L	L	X	H
X	L	X	L	H

positive logic equation

$$Y = \overline{A1 \cdot [B1 + (C1 \cdot C2)]}$$

description

The SN54ASC6065 and SN74ASC6065 CMOS standard-cell Boolean macros are 2-input sum-of-products NAND gates with a dedicated 2-input OR, 2-input AND product term. One available input to the 2-input OR gate and the available input to the 2-input NAND gate provides expandability for implementing customized product terms. The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
BF065LH	Label: BF065LH A1,B1,C1,C2,Y;	1.75

The SN54ASC6065 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6065 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER		TEST CONDITIONS		TYP	MAX	UNIT
V_T Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		V
I_{CC} Supply current	SN54ASC6065	V_{CC} = 4.5 V to 5.5 V,	V_I = V_{CC} or 0		219	nA
	SN74ASC6065	T_A = MIN to MAX			13.1	
C_i Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.13		pF
C_{pd} Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	$t_r = t_f$ = 3 ns,	0.58		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6065			SN74ASC6065			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A1	Y	C_L = 0	0.6	0.8	1.2	0.6	0.8	1.2	ns
t_{PHL}				0.8	1.2	2.3	0.8	1.2	2.1	
t_{PLH}	A1	Y	C_L = 1 pF	1.1	1.8	3.5	1.2	1.8	3.2	ns
t_{PHL}				1.4	2.5	5.7	1.5	2.5	5	
t_{PLH}	B1	Y	C_L = 0	0.9	1.2	2.1	0.9	1.2	2	ns
t_{PHL}				0.3	0.7	1.4	0.3	0.7	1.3	
t_{PLH}	B1	Y	C_L = 1 pF	1.8	3.1	6.6	1.9	3.1	6.1	ns
t_{PHL}				0.8	1.7	3.8	0.9	1.7	3.4	
t_{PLH}	Any C	Y	C_L = 0	0.7	1.3	3.1	0.8	1.3	2.8	ns
t_{PHL}				0.4	1	2.4	0.5	1	2.1	
t_{PLH}	Any C	Y	C_L = 1 pF	1.7	3.3	7.7	1.8	3.3	6.9	ns
t_{PHL}				1.1	2.3	5.9	1.2	2.3	5.1	
Δt_{PLH}	A1	Y		0.5	1	2.3	0.5	1	2.1	ns/pF
Δt_{PHL}				0.6	1.3	3.5	0.6	1.3	3	
Δt_{PLH}	B1	Y		0.9	1.9	4.5	1	1.9	4.1	ns/pF
Δt_{PHL}				0.5	1	2.5	0.5	1	2.1	
Δt_{PLH}	Any C	Y		0.9	2	4.6	1	2	4.1	ns/pF
Δt_{PHL}				0.6	1.3	3.5	0.6	1.3	3	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

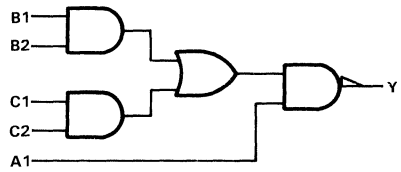
Refer to the 'ASC6017 data sheet and Section 7.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SystemCell™ 2-μm INTERNAL STANDARD CELL

- **Typical Propagation Delay with 1-pF Load**
  2.3 ns from A1
  3.2 ns from Any B
  2.9 ns from Any C
- **Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V**
- **Functional Operation Over V_{CC} Range of 2 V to 6 V**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol



FUNCTION TABLE

INPUTS					OUTPUT
A1	B1	B2	C1	C2	Y
H	H	H	X	X	L
H	X	X	H	H	L
Any other combination					H

positive logic equation

$$Y = \overline{A1 \cdot [(B1 \cdot B2) + (C1 \cdot C2)]}$$

description

The SN54ASC6066 and SN74ASC6066 CMOS standard-cell Boolean macros are 2-input sum-of-products NAND gates with a dedicated 2-wide, 2-input AND-OR product term. The available NAND input can be used to combine other custom product terms with the 2-wide, 2-input AND-OR term. The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
BF066LH	Label: BF066LH A1,B1,B2,C1,C2,Y;	2.5

The SN54ASC6066 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6066 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER		TEST CONDITIONS		TYP	MAX	UNIT
V_T Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		V
I_{CC} Supply current	SN54ASC6066	V_{CC} = 4.5 V to 5.5 V,	V_I = V_{CC} or 0,		291	nA
	SN74ASC6066	T_A = MIN to MAX			17.4	
C_i Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.13		pF
C_{pd} Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	0.64		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6066			SN74ASC6066			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A1	Y	C_L = 0	0.7	0.9	1.4	0.7	0.9	1.4	ns
t_{PHL}				0.9	1.5	3.1	1	1.5	2.8	
t_{PLH}	A1	Y	C_L = 1 pF	1.2	1.9	3.7	1.2	1.9	3.4	ns
t_{PHL}				1.6	2.8	6.6	1.7	2.8	5.8	
t_{PLH}	Any B	Y	C_L = 0	0.9	1.7	4.2	0.9	1.7	3.8	ns
t_{PHL}				0.6	0.3	3.8	0.6	1.3	3.1	
t_{PLH}	Any B	Y	C_L = 1 pF	1.9	3.7	8.8	2	3.7	8	ns
t_{PHL}				1.2	2.6	6.6	1.3	2.6	5.8	
t_{PLH}	Any C	Y	C_L = 0	1	1.5	3.4	1	1.5	3.1	ns
t_{PHL}				0.4	1	2.8	0.5	1	2.4	
t_{PLH}	Any C	Y	C_L = 1 pF	1.9	3.5	7.9	2	3.5	7.2	ns
t_{PHL}				1.1	2.3	5.8	1.2	2.3	5	
Δt_{PLH}	A1	Y		0.5	1	2.3	0.5	1	2.1	ns/pF
Δt_{PHL}				0.6	1.3	3.5	0.6	1.3	3	
Δt_{PLH}	Any B	Y		0.9	2	4.6	0.9	2	4.2	ns/pF
Δt_{PHL}				0.6	1.3	2.9	0.6	1.3	2.7	
Δt_{PLH}	Any C	Y		0.9	2	4.6	1	2	4.1	ns/pF
Δt_{PHL}				0.6	1.3	3	0.6	1.3	2.7	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

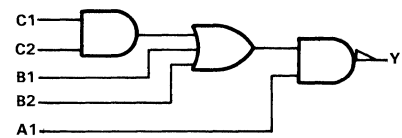
Refer to the 'ASC6017 data sheet and Section 7.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SystemCell™ 2-μm INTERNAL STANDARD CELL

- Typical Propagation Delay with 1-pF Load
  - 2.2 ns from A1
  - 3.3 ns from Any B
  - 3.7 ns from Any C
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol



FUNCTION TABLE

INPUTS					OUTPUT
A1	B1	B2	C1	C2	Y
H	H	X	X	X	L
H	X	H	X	X	L
H	X	X	H	H	L
L	X	X	X	X	H
X	L	L	L	X	H
X	L	L	X	L	H

positive logic equation

$$Y = \overline{A1 \cdot [B1 + B2 + (C1 \cdot C2)]}$$

description

The SN54ASC6067 and SN74ASC6067 CMOS standard-cell Boolean macros are 2-input sum-of-products NAND gates with a dedicated 2-input AND, 3-input OR product term. Two available inputs to the 3-input OR gate and one to the 2-input NAND gate provide expandability for implementing customized product terms. The cells are designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
BF067LH	Label: BF067LH A1,B1,B2,C1,C2,Y;	2

The SN54ASC6067 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6067 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER		TEST CONDITIONS		TYP	MAX	UNIT
V_T Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		V
I_{CC} Supply current	SN54ASC6067	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0,			248	nA
	SN74ASC6067	T_A = MIN to MAX			14.9	
C_i Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.13		pF
C_{pd} Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	$t_r = t_f$ = 3 ns,	0.57		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6067			SN74ASC6067			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A1	Y	C_L = 0	0.6	0.8	1.2	0.6	0.8	1.2	ns
t_{PHL}				0.9	1.3	2.5	0.9	1.3	2.3	
t_{PLH}	A1	Y	C_L = 1 pF	1.1	1.8	3.5	1.2	1.8	3.2	ns
t_{PHL}				1.5	2.6	6.1	1.6	2.6	5.3	
t_{PLH}	Any B	Y	C_L = 0	1.1	1.8	4.4	1.1	1.8	4	ns
t_{PHL}				0.3	0.9	2	0.4	0.9	1.8	
t_{PLH}	Any B	Y	C_L = 1 pF	2.5	4.8	11.2	2.7	4.8	10.2	ns
t_{PHL}				0.9	1.8	4.4	0.9	1.8	3.8	
t_{PLH}	Any C	Y	C_L = 0	0.8	1.9	5	0.9	1.9	4.5	ns
t_{PHL}				0.4	1.1	2.6	0.5	1.1	2.3	
t_{PLH}	Any C	Y	C_L = 1 pF	2.3	4.9	11.8	2.4	4.9	10.7	ns
t_{PHL}				1.1	2.4	6.2	1.2	2.4	5.4	
Δt_{PLH}	A1	Y		0.5	1	2.3	0.5	1	2.1	ns/pF
Δt_{PHL}				0.6	1.3	3.6	0.6	1.3	3.1	
Δt_{PLH}	Any B	Y		1.4	3	6.9	1.5	3	6.2	ns/pF
Δt_{PHL}				0.5	0.9	2.5	0.5	0.9	2.1	
Δt_{PLH}	Any C	Y		1.4	3	6.9	1.5	3	6.2	ns/pF
Δt_{PHL}				0.6	1.3	3.6	0.7	1.3	3.1	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

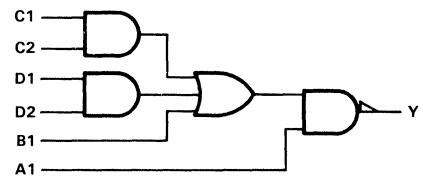
Refer to the 'ASC6017 data sheet and Section 7.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SystemCell™ 2-μm INTERNAL STANDARD CELL

- Typical Propagation Delay With (1-pF Load)
  - 2.8 ns from A1
  - 3.2 ns from B1
  - 4.0 ns from Any C or D
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol



FUNCTION TABLE

INPUTS						OUTPUT
A1	B1	C1	C2	D1	D2	Y
H	H	X	X	X	X	L
H	X	H	H	X	X	L
H	X	X	X	H	H	L
L	X	X	X	X	X	H
X	L	L	X	L	X	H
X	L	X	L	X	L	H

positive logic equation

$$Y = \overline{A1 \cdot [B1 + (C1 \cdot C2) + (D1 \cdot D2)]}$$

description

The SN54ASC6068 and SN74ASC6068 CMOS standard-cell Boolean macros are 2-input sum-of-products NAND gates with dedicated 2-wide-AND and 3-input-OR product term. The available NAND and OR inputs can be used to combine other custom product terms with the 2-wide, 2-input AND-OR term. The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
BF068LH	Label: BF068LH A1,B1,C1,C2,D1,D2,Y;	2.75

The SN54ASC6068 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6068 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS		TYP	MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		V
I_{CC}	Supply current	SN54ASC6068	V_{CC} = 4.5 V to 5.5 V,	V_I = V_{CC} or 0,		317	nA
		SN74ASC6068	T_A = MIN to MAX			19	
C_i	Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.13		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	$t_r = t_f$ = 3 ns,	0.61		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6068			SN74ASC6068			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A1	Y	C_L = 0	0.6	0.8	1.2	0.6	0.8	1.2	ns
t_{PHL}				0.9	1.4	2.9	1	1.4	2.6	
t_{PLH}	A1	Y	C_L = 1 pF	1.1	1.8	3.5	1.2	1.8	3.2	ns
t_{PHL}				1.6	2.8	6.5	1.7	2.8	5.7	
t_{PLH}	B1	Y	C_L = 0	1.1	1.7	3.3	1.1	1.7	3.1	ns
t_{PHL}				0.3	0.8	1.6	0.4	0.8	1.5	
t_{PLH}	B1	Y	C_L = 1 pF	2.5	4.6	10.1	2.7	4.6	9.2	ns
t_{PHL}				0.9	1.8	4	0.9	1.8	3.6	
t_{PLH}	Any C or D	Y	C_L = 0	0.9	2.3	5.5	1	2.3	5	ns
t_{PHL}				0.4	1.3	2.9	0.5	1.3	2.5	
t_{PLH}	Any C or D	Y	C_L = 1 pF	2.4	5.3	12.4	2.6	5.3	11.2	ns
t_{PHL}				1.1	2.6	6.5	1.2	2.6	5.6	
Δt_{PLH}	A1	Y		0.5	1	2.3	0.5	1	2.1	ns/pF
Δt_{PHL}				0.6	1.4	3.7	0.6	1.4	3.2	
Δt_{PLH}	B1	Y		1.4	2.9	6.9	1.5	2.9	6.2	ns/pF
Δt_{PHL}				0.5	1	2.5	0.5	1	2.1	
Δt_{PLH}	Any C or D	Y		1.4	3	6.9	1.5	3	6.2	ns/pF
Δt_{PHL}				0.6	1.3	3.7	0.6	1.3	3.2	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

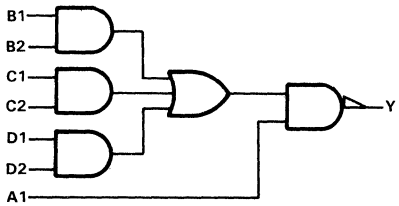
DESIGN CONSIDERATIONS

Refer to the 'ASC6017 data sheet and Section 7.

SystemCell™ 2-μm INTERNAL STANDARD CELL

- **Typical Propagation Delay with 1-pF Load**
  2.5 ns from A1
  4.2 ns from Any B, C, or D
- **Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V**
- **Functional Operation Over V_{CC} Range of 2 V to 6 V**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol



positive logic equation

$$Y = \overline{A1 \cdot [(B1 \cdot B2) + (C1 \cdot C2) + (D1 \cdot D2)]}$$

FUNCTION TABLE

INPUTS							OUTPUT
A1	B1	B2	C1	C2	D1	D2	Y
H	H	H	X	X	X	X	L
H	X	X	H	H	X	X	L
H	X	X	X	X	H	H	L
Any other combination							H

description

The SN54ASC6069 and SN74ASC6069 CMOS standard-cell Boolean macros are 2-input sum-of-products NAND gates with a dedicated 3-wide-AND-OR product term. The available NAND input can be used to combine other custom product terms with the 3-wide, 2-input AND-OR term. The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
BF069LH	Label: BF069LH A1,B1,B2,C1,C2,D1,D2,Y;	3

The SN54ASC6069 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6069 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS		TYP	MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		V
I_{CC}	Supply current	SN54ASC6069	V_{CC} = 4.5 V to 5.5 V,	V_I = V_{CC} or 0,		350	nA
		SN74ASC6069	T_A = MIN to MAX			21	
C_i	Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.13		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	$t_r = t_f$ = 3 ns,	0.66		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6069			SN74ASC6069			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A1	Y	C_L = 0	0.6	0.9	1.4	0.7	0.9	1.4	ns
t_{PHL}				1.1	1.7	3.8	1.1	1.7	3.4	
t_{PLH}	A1	Y	C_L = 1 pF	1.2	1.9	3.7	1.2	1.9	3.4	ns
t_{PHL}				1.7	3.1	7.4	1.8	3.1	6.4	
t_{PLH}	Any B, C, or D	Y	C_L = 0	1.1	2.4	6.9	1.2	2.4	6.2	ns
t_{PHL}				0.4	1.4	4	0.5	1.4	3.3	
t_{PLH}	Any B, C, or D	Y	C_L = 1 pF	2.5	5.7	13.8	2.7	5.7	12.5	ns
t_{PHL}				1.1	2.7	7.1	1.2	2.7	6.2	
Δt_{PLH}	A1	Y		0.5	1	2.3	0.5	1	2.1	ns/pF
Δt_{PHL}				0.6	1.4	3.6	0.6	1.4	3.1	
Δt_{PLH}	Any B, C, or D	Y		1.4	3	6.9	1.5	3	6.3	ns/pF
Δt_{PHL}				0.6	1.3	3.1	0.6	1.3	2.9	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

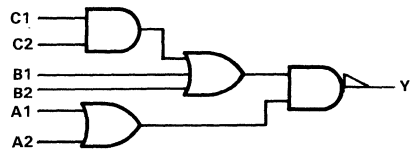
Refer to the 'ASC6017 data sheet and Section 7.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SystemCell™ 2-μm INTERNAL STANDARD CELL

- **Typical Propagation Delay with 1-pF Load**
  2.3 ns from Any A
  3 ns from Any B
  3.8 ns from Any C
- **Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V**
- **Functional Operation Over V_{CC} Range of 2 V to 6 V**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol



FUNCTION TABLE

INPUTS						OUTPUT
A1	A2	B1	B2	C1	C2	Y
H	X	H	X	X	X	L
X	H	H	X	X	X	L
H	X	X	H	X	X	L
X	H	X	H	X	X	L
H	X	X	X	H	H	L
X	H	X	X	H	H	L
L	L	X	X	X	X	H
X	X	L	L	L	X	H
X	X	L	L	X	L	H

positive logic equation

$$Y = \overline{(A1 + A2) \cdot [B1 + B2 + (C1 \cdot C2)]}$$

description

The SN54ASC6072 and SN74ASC6072 CMOS standard-cell Boolean macros are 2-wide 2-3-input sum-of-products OR-NAND gates with a dedicated 2-input AND, 2-input OR product term. Two available inputs to the 3-input OR gate and two to the 2-input OR gate provide expandability for implementing customized product terms. The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
BF072LH	Label: BF072LH A1,A2,B1,B2,C1,C2,Y;	2

The SN54ASC6072 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6072 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER		TEST CONDITIONS		TYP	MAX	UNIT
V_T Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		V
I_{CC} Supply current	SN54ASC6072	V_{CC} = 4.5 V to 5.5 V,	V_I = V_{CC} or 0,		252	nA
	SN74ASC6072	T_A = MIN to MAX			15.1	
C_i Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.13		pF
C_{pd} Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	$t_r = t_f$ = 3 ns,	0.81		pF

switching characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6072			SN74ASC6072			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Any A	Y	C_L = 0	0.7	1	1.8	0.7	1	1.6	ns
t_{PHL}				0.3	0.9	1.6	0.4	0.9	1.6	
t_{PLH}	Any A	Y	C_L = 1 pF	1.6	2.9	6.2	1.6	2.9	5.6	ns
t_{PHL}				0.9	1.6	3.4	0.9	1.6	3.1	
t_{PLH}	Any B	Y	C_L = 0	1	1.7	3.9	1.1	1.7	3.5	ns
t_{PHL}				0.3	1	1.8	0.4	1	1.7	
t_{PLH}	Any B	Y	C_L = 1 pF	2.2	4.2	9.6	2.3	4.2	8.7	ns
t_{PHL}				0.8	1.7	3.6	0.9	1.7	3.2	
t_{PLH}	Any C	Y	C_L = 0	1.1	2.3	6	1.1	2.3	5.4	ns
t_{PHL}				0.5	1.2	2.6	0.5	1.2	2.3	
t_{PLH}	Any C	Y	C_L = 1 pF	2.5	5.3	12.9	2.7	5.3	11.6	ns
t_{PHL}				1	2.3	5.5	1.1	2.3	4.8	
Δt_{PLH}	Any A	Y		0.9	1.9	4.5	0.9	1.9	4	ns/pF
Δt_{PHL}				0.4	0.7	1.8	0.5	0.7	1.6	
Δt_{PLH}	Any B	Y		1.1	2.5	5.8	1.2	2.5	5.2	ns/pF
Δt_{PHL}				0.4	0.7	1.9	0.4	0.7	1.6	
Δt_{PLH}	Any C	Y		1.4	3	7	1.5	3	6.3	ns/pF
Δt_{PHL}				0.5	1.1	3	0.5	1.1	2.6	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

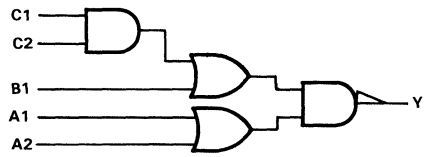
Refer to the 'ASC6017 data sheet and Section 7.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SystemCell™ 2-μm INTERNAL STANDARD CELL

- **Typical Propagation Delay with 1-pF Load**
  - **2.3 ns from Any A**
  - **2.2 ns from B1**
  - **2.9 ns from Any C**
- **Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V**
- **Functional Operation Over V_{CC} Range of 2 V to 6 V**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol



FUNCTION TABLE

INPUTS					OUTPUT
A1	A2	B1	C1	C2	Y
H	X	H	X	X	L
X	H	H	X	X	L
H	X	X	H	H	L
X	H	X	H	H	L
L	L	X	X	X	H
X	X	L	L	X	H
X	X	L	X	L	H

positive logic equation

$$Y = \overline{(A1 + A2) \cdot [B1 + (C1 \cdot C2)]}$$

description

The SN54ASC6073 and SN74ASC6073 CMOS standard-cell Boolean macros are 2-wide 2-input sum-of-products OR-NAND gates with a dedicated 2-input AND, 2-input OR product term. One available input to one 2-input OR gate and two to the other provide expandability for implementing customized product terms. The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
BF070LH	Label: BF070LH A1,A2,B1,C1,C2,Y;	2

The SN54ASC6073 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6073 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS		TYP	MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		V
I_{CC}	Supply current	SN54ASC6073	V_{CC} = 4.5 V to 5.5 V,	V_I = V_{CC} or 0,		249	nA
		SN74ASC6073	T_A = MIN to MAX			14.9	
C_i	Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.13		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	$t_r = t_f$ = 3 ns,	0.53		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6073			SN74ASC6073			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Any A	Y	C_L = 0	0.6	1	2	0.6	1	1.8	ns
t_{PHL}				0.8	1.3	2.8	0.8	1.3	2.5	
t_{PLH}	Any A	Y	C_L = 1 pF	1.6	3	6.5	1.7	3	5.9	ns
t_{PHL}				1.4	2.6	6.2	1.5	2.6	5.5	
t_{PLH}	B1	Y	C_L = 0	0.9	1.1	2.1	0.9	1.1	1.9	ns
t_{PHL}				0.3	0.8	1.5	0.4	0.8	1.4	
t_{PLH}	B1	Y	C_L = 1 pF	1.6	2.6	5.4	1.6	2.6	5	ns
t_{PHL}				0.9	1.7	4	0.9	1.7	3.5	
t_{PLH}	Any C	Y	C_L = 0	0.8	1.4	3.4	0.8	1.4	3.1	ns
t_{PHL}				0.5	1.1	2.5	0.5	1.1	2.3	
t_{PLH}	Any C	Y	C_L = 1 pF	1.7	3.4	7.9	1.8	3.4	7.2	ns
t_{PHL}				1.1	2.4	6	1.2	2.4	5.3	
Δt_{PLH}	Any A	Y		0.9	2	4.6	1	2	4.2	ns/pF
Δt_{PHL}				0.6	1.3	3.5	0.6	1.3	3	
Δt_{PLH}	B1	Y		0.6	1.5	3.4	0.7	1.5	3.1	ns/pF
Δt_{PHL}				0.5	0.9	2.5	0.5	0.9	2.1	
Δt_{PLH}	Any C	Y		0.9	2	4.6	1	2	4.1	ns/pF
Δt_{PHL}				0.6	1.3	3.5	0.6	1.3	3	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

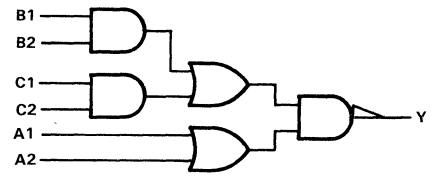
Refer to the 'ASC6017 data sheet and Section 7.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SystemCell™ 2-μm INTERNAL STANDARD CELL

- **Typical Propagation Delay with 1-pF Load**
  2.9 ns from Any A
  3.1 ns from Any B or C
- **Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V**
- **Functional Operation Over V_{CC} Range of 2 V to 6 V**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol



positive logic equation

$$Y = \overline{(A1 + A2) \cdot [(B1 \cdot B2) + (C1 \cdot C2)]}$$

FUNCTION TABLE

INPUTS						OUTPUT
A1	A2	B1	B2	C1	C2	Y
H	X	H	H	X	X	L
X	H	H	H	X	X	L
H	X	X	X	H	H	L
X	H	X	X	H	H	L
Any other combination						H

description

The SN54ASC6074 and SN74ASC6074 CMOS standard-cell Boolean macros are 2-wide 2-input sum-of-products OR-NAND gates with a dedicated 2-wide, 2-input, AND-OR product term. The available 2-input OR gate provides expandability for implementing customized product terms. The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
BF071LH	Label: BF071LH A1,A2,B1,B2,C1,C2,Y;	2.5

The SN54ASC6074 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6074 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS		TYP	MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		V
I_{CC}	Supply current	SN54ASC6074	V_{CC} = 4.5 V to 5.5 V,	V_I = V_{CC} or 0,		304	nA
		SN74ASC6074	T_A = MIN to MAX			18.2	
C_i	Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.13		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	$t_r = t_f$ = 3 ns,	0.64		pF

4 Data Sheets

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6074			SN74ASC6074			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Any A	Y	C_L = 0	0.7	1.1	2.3	0.7	1.1	2.1	ns
t_{PHL}				0.9	1.5	3.9	0.9	1.5	3.3	
t_{PLH}	Any A	Y	C_L = 1 pF	1.6	3.1	6.9	1.7	3.1	6.2	ns
t_{PHL}				1.5	2.8	6.7	1.6	2.8	5.9	
t_{PLH}	Any B or C	Y	C_L = 0	0.9	1.7	4.2	0.9	1.7	3.8	ns
t_{PHL}				0.5	1.2	3.9	0.5	1.2	3.3	
t_{PLH}	Any B or C	Y	C_L = 1 pF	1.9	3.7	8.7	2	3.7	7.9	ns
t_{PHL}				1.1	2.5	6.7	1.2	2.5	5.9	
Δt_{PLH}	Any A	Y		0.9	2	4.6	1	2	4.2	ns/pF
Δt_{PHL}				0.6	1.3	2.8	0.6	1.3	2.6	
Δt_{PLH}	Any B or C	Y		0.9	2	4.6	1	2	4.2	ns/pF
Δt_{PHL}				0.6	1.3	3	0.6	1.3	2.7	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to the 'ASC6017 data sheet and Section 7.

TEXAS INSTRUMENTS
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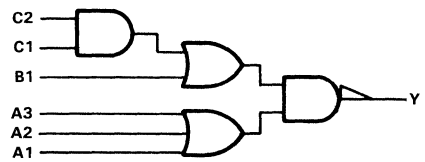
SystemCell™ 2-μm INTERNAL STANDARD CELL

- **Typical Propagation Delay with 1-pF Load**
  - **3.6 ns from Any A**
  - **1.9 ns from B1**
  - **2.5 ns from Any C**
- **Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V**
- **Functional Operation Over V_{CC} Range of 2 V to 6 V**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol



positive logic equation

$$Y = \overline{(A1 + A2 + A3) \cdot [B1 + (C1 \cdot C2)]}$$

FUNCTION TABLE

(SUMMARIZED) INPUTS						OUTPUT
A1	A2	A3	B1	C1	C2	Y
H	X	X	H	X	X	L
X	H	X	H	X	X	L
X	X	H	H	X	X	L
H	X	X	X	H	H	L
X	H	X	X	H	H	L
X	X	H	X	H	H	L
L	L	L	X	X	X	H
X	X	X	L	L	X	H
X	X	X	L	X	L	H

description

The SN54ASC6075 and SN74ASC6075 CMOS standard-cell Boolean macros are 2-wide 2-3-input sum-of-products OR-NAND gates with a dedicated 2-input AND, 2-input OR product term. One available input to the 2-input OR gate and three to the 3-input OR gate provide expandability for implementing customized product terms. The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
BF075LH	Label: BF075LH A1,A2,A3,B1,C1,C2,Y;	2

The SN54ASC6075 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6075 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS		TYP	MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		V
I_{CC}	Supply current	SN54ASC6075	V_{CC} = 4.5 V to 5.5 V,	V_I = V_{CC} or 0,		252	nA
		SN74ASC6075	T_A = MIN to MAX			15.1	
C_i	Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.13		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	$t_r = t_f$ = 3 ns,	0.77		pF

4 Data Sheets

switching characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6075			SN74ASC6075			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Any A	Y	C_L = 0	1.2	2.3	5.7	1.2	2.3	5.2	ns
t_{PHL}				0.3	1.1	2.8	0.4	1.1	2.6	
t_{PLH}	Any A	Y	C_L = 1 pF	2.6	5.3	12.6	2.8	5.3	11.4	ns
t_{PHL}				0.8	1.8	4.4	0.9	1.8	3.9	
t_{PLH}	B1	Y	C_L = 0	0.8	0.8	1.3	0.7	0.8	1.3	ns
t_{PHL}				0.4	0.9	1.4	0.4	0.9	1.4	
t_{PLH}	B1	Y	C_L = 1 pF	1.4	2.2	4.5	1.4	2.2	4.1	ns
t_{PHL}				0.9	1.6	3.2	0.9	1.6	2.9	
t_{PLH}	Any C	Y	C_L = 0	0.7	1	2.4	0.7	1	2.2	ns
t_{PHL}				0.5	1.1	2	0.5	1.1	1.9	
t_{PLH}	Any C	Y	C_L = 1 pF	1.5	2.9	6.6	1.6	2.9	6	ns
t_{PHL}				1	2.1	4.7	1.1	2.1	4.2	
Δt_{PLH}	Any A	Y		1.4	3	6.9	1.5	3	6.3	ns/pF
Δt_{PHL}				0.4	0.7	2	0.5	0.7	1.7	
Δt_{PLH}	B1	Y		0.6	1.4	3.2	0.7	1.4	2.9	ns/pF
Δt_{PHL}				0.4	0.7	1.8	0.5	0.7	1.5	
Δt_{PLH}	Any C	Y		0.8	1.9	4.4	0.9	1.9	4	ns/pF
Δt_{PHL}				0.5	1	2.7	0.5	1	2.3	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

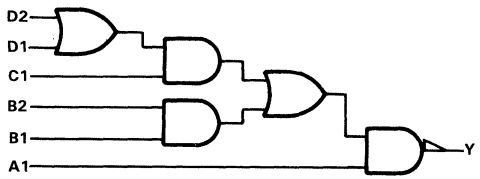
DESIGN CONSIDERATIONS

Refer to the 'ASC6017 data sheet and Section 7.

SystemCell™ 2-μm INTERNAL STANDARD CELL

- **Typical Propagation Delay with 1-pF Load**
  - **2.1 ns from A1**
  - **2.8 ns from Any B or C**
  - **3.8 ns from Any D**
- **Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V**
- **Functional Operation Over V_{CC} Range of 2 V to 6 V**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol



FUNCTION TABLE

INPUTS						OUTPUT
A1	B1	B2	C1	D1	D2	Y
H	H	H	X	X	X	L
H	X	X	H	H	X	L
H	X	X	H	X	H	L
Any other combination						H

positive logic equation

$$Y = \overline{A1 \cdot \{(B1 \cdot B2) + [C1 \cdot (D1 + D2)]\}}$$

description

The SN54ASC6082 and SN74ASC6082 CMOS standard-cell Boolean macros are 2-wide 1-2-input sum-of-products OR-NAND gates with 2-input OR, 2-input AND, and one available input to the 2-input AND gate to provide expandability for implementing customized product terms. The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
BF082LH	Label: BF082LH A1,B1,B2,C1,D1,D2,Y;	2.25

The SN54ASC6082 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6082 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS		TYP	MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		V
I_{CC}	Supply current	SN54ASC6082	V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX	V_I = V_{CC} or 0,		283	nA
		SN74ASC6082				17	
C_i	Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.13		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	0.87		pF

switching characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6082			SN74ASC6082			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A1	Y	C_L = 0	0.7	1.1	1.5	0.8	1.1	1.5	ns
t_{PHL}				0.6	1.2	2	0.7	1.2	2	
t_{PLH}	A1	Y	C_L = 1 pF	1.3	2	3.6	1.3	2	3.4	ns
t_{PHL}				1.2	2.1	4.2	1.3	2.1	3.8	
t_{PLH}	Any B, C	Y	C_L = 0	1	1.5	2.8	1	1.5	2.7	ns
t_{PHL}				0.4	1.2	2.9	0.4	1.2	2.6	
t_{PLH}	Any B, C	Y	C_L = 1 pF	1.7	3.1	6.6	1.8	3.1	6.1	ns
t_{PHL}				1	2.5	5.9	1.1	2.5	5.2	
t_{PLH}	Any D	Y	C_L = 0	1.2	2.2	5.1	1.2	2.2	4.6	ns
t_{PHL}				0.5	1.5	3.5	0.6	1.5	3.1	
t_{PLH}	Any D	Y	C_L = 1 pF	2.4	4.7	10.8	2.5	4.7	9.8	ns
t_{PHL}				1.2	2.8	7.1	1.3	2.8	6.2	
Δt_{PLH}	A1	Y		0.5	0.9	2.2	0.5	0.9	2	ns/pF
Δt_{PHL}				0.5	0.9	2.3	0.6	0.9	1.9	
Δt_{PLH}	Any B, C	Y		0.7	1.6	3.8	0.7	1.6	3.4	ns/pF
Δt_{PHL}				0.6	1.3	3.5	0.6	1.3	3	
Δt_{PLH}	Any D	Y		1.1	2.5	5.8	1.2	2.5	5.2	ns/pF
Δt_{PHL}				0.6	1.3	3.6	0.7	1.3	3.1	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

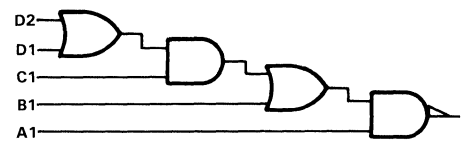
DESIGN CONSIDERATIONS

Refer to the 'ASC6017 data sheet and Section 7.

SystemCell™ 2-μm INTERNAL STANDARD CELL

- **Typical Propagation Delay with 1-pF Load**
  - **1.8 ns from A1**
  - **2.3 ns from B1**
  - **3 ns from C1**
  - **3.7 ns from Any D**
- **Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V**
- **Functional Operation Over V_{CC} Range of 2 V to 6 V**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol



FUNCTION TABLE

INPUTS					OUTPUT
A1	B1	C1	D1	D2	Y
H	H	X	X	X	L
H	X	H	H	X	L
H	X	H	X	H	L
Any other combination					H

positive logic equation

$$Y = \overline{A1 \cdot \{B1 + [C1 \cdot (D1 + D2)]\}}$$

description

The SN54ASC6083 and SN74ASC6083 CMOS standard-cell Boolean macros are 2-wide 1-2-input sum-of-products OR-NAND gates with 2-input OR, and one available input each to the 2-input AND and OR gates to provide expandability for implementing customized product terms. The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
BF080LH	Label: BF080LH A1,B1,C1,D1,D2,Y;	2

The SN54ASC6083 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6083 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS		TYP	MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		V
I_{CC}	Supply current	SN54ASC6083	V_{CC} = 4.5 V to 5.5 V,	V_I = V_{CC} or 0,		252	nA
		SN74ASC6083	T_A = MIN to MAX			15.1	
C_i	Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.13		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	0.8		pF

switching characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6083			SN74ASC6083			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A1	Y	C_L = 0	0.6	0.9	1.2	0.6	0.9	1.2	ns
t_{PHL}				0.4	0.9	1.5	0.5	0.9	1.4	
t_{PLH}	A1	Y	C_L = 1 pF	1.1	1.8	3.4	1.2	1.8	3.1	ns
t_{PHL}				0.9	1.7	3.4	1	1.7	3	
t_{PLH}	B1	Y	C_L = 0	0.9	1.2	2.1	0.9	1.2	2	ns
t_{PHL}				0.3	0.8	1.5	0.4	0.8	1.4	
t_{PLH}	B1	Y	C_L = 1 pF	1.7	2.8	5.9	1.7	2.8	5.4	ns
t_{PHL}				0.8	1.7	3.8	0.9	1.7	3.4	
t_{PLH}	C1	Y	C_L = 0	1	1.7	3.9	1	1.7	3.5	ns
t_{PHL}				0.5	1.1	2.5	0.6	1.1	2.2	
t_{PLH}	C1	Y	C_L = 1 pF	1.9	3.7	8.4	2	3.7	7.7	ns
t_{PHL}				1	2.2	5.4	1.1	2.2	4.7	
t_{PLH}	Any D	Y	C_L = 0	0.9	1.9	4.6	1	1.9	4.1	ns
t_{PHL}				0.6	1.2	2.8	0.7	1.2	2.4	
t_{PLH}	Any D	Y	C_L = 1 pF	2.4	4.9	11.5	2.5	4.9	10.4	ns
t_{PHL}				1.3	2.5	6.3	1.3	2.5	5.5	
Δt_{PLH}	A1	Y		0.5	0.9	2.2	0.5	0.9	2	ns/pF
Δt_{PHL}				0.5	0.8	1.9	0.5	0.8	1.7	
Δt_{PLH}	B1	Y		0.7	1.6	3.8	0.8	1.6	3.5	ns/pF
Δt_{PHL}				0.5	0.9	2.4	0.5	0.9	2	
Δt_{PLH}	C1	Y		0.9	2	4.6	1	2	4.2	ns/pF
Δt_{PHL}				0.5	1.1	2.9	0.5	1.1	2.5	
Δt_{PLH}	Any D	Y		1.4	3	7	1.5	3	6.3	ns/pF
Δt_{PHL}				0.6	1.3	3.5	0.6	1.3	3.1	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to the 'ASC6017 data sheet and Section 7.

TEXAS INSTRUMENTS
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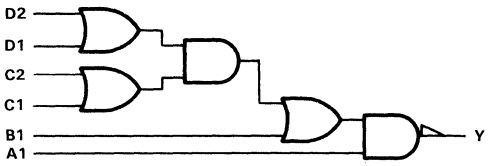
SystemCell™ 2-μm INTERNAL STANDARD CELL

- **Typical Propagation Delay with 1-pF Load**
  - **1.7 ns from A1**
  - **2.5 ns from B1**
  - **3.9 ns from Any C or D**
- **Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V**
- **Functional Operation Over V_{CC} Range of 2 V to 6 V**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol



FUNCTION TABLE

INPUTS						OUTPUT
A1	B1	C1	C2	D1	D2	Y
H	H	X	X	X	X	L
H	X	H	X	H	X	L
H	X	H	X	X	H	L
H	X	X	H	H	X	L
H	X	X	H	X	H	L
Any other combination						H

positive logic equation

$$Y = \overline{A1 \cdot \{B1 + [(C1 + C2) \cdot (D1 + D2)]\}}$$

description

The SN54ASC6084 and SN74ASC6084 CMOS standard-cell Boolean macros are 2-wide 1-2-input sum-of-products OR-NAND gates with 2-input OR, dual 2-input OR, and one available input to the 2-input OR gate to provide expandability for implementing customized product terms. The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
BF081LH	Label: BF081LH A1,B1,C1,C2,D1,D2,Y;	2.5

The SN54ASC6084 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6084 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER		TEST CONDITIONS		TYP	MAX	UNIT
V_T Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		V
I_{CC} Supply current	SN54ASC6084	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0,			314	nA
	SN74ASC6084	T_A = MIN to MAX			18.9	
C_i Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.13		pF
C_{pd} Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	$t_r = t_f$ = 3 ns,	0.9		pF

switching characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6084			SN74ASC6084			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A1	Y	C_L = 0	0.7	0.8	1.3	0.7	0.8	1.2	ns
t_{PHL}				0.4	0.8	1.5	0.5	0.8	1.4	
t_{PLH}	A1	Y	C_L = 1 pF	1.2	1.8	3.5	1.2	1.8	3.3	ns
t_{PHL}				0.9	1.6	3.3	1	1.6	3	
t_{PLH}	B1	Y	C_L = 0	1	1.3	2.4	1	1.3	2.3	ns
t_{PHL}				0.3	0.8	1.6	0.4	0.8	1.5	
t_{PLH}	B1	Y	C_L = 1 pF	1.9	3.2	6.9	2	3.2	6.3	ns
t_{PHL}				0.8	1.7	4	0.9	1.7	3.5	
t_{PLH}	Any C, D	Y	C_L = 0	1	2.5	6.7	1.1	2.5	6	ns
t_{PHL}				0.5	1.2	2.9	0.6	1.2	2.6	
t_{PLH}	Any C, D	Y	C_L = 1 pF	2.6	5.5	13.4	2.7	5.5	12.1	ns
t_{PHL}				1.1	2.3	5.9	1.2	2.3	5.1	
Δt_{PLH}	A1	Y		0.5	1	2.3	0.5	1	2.1	ns/pF
Δt_{PHL}				0.4	0.8	1.9	0.6	0.8	1.6	
Δt_{PLH}	B1	Y		0.9	1.9	4.5	0.9	1.9	4.1	ns/pF
Δt_{PHL}				0.5	0.9	2.4	0.5	0.9	2.1	
Δt_{PLH}	Any C, D	Y		1.4	3	6.9	1.5	3	6.2	ns/pF
Δt_{PHL}				0.5	1.1	3.1	0.6	1.1	2.6	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

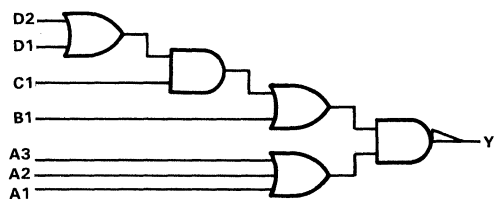
DESIGN CONSIDERATIONS

Refer to the 'ASC6017 data sheet and Section 7.

SystemCell™ 2-μm INTERNAL STANDARD CELL

- **Typical Propagation Delay with 1-pF Load**
  - **3.1 ns from Any A or C1**
  - **2.3 ns from B1**
  - **4.1 ns from Any D**
- **Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V**
- **Functional Operation Over V_{CC} Range of 2 V to 6 V**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol



positive logic equation

$$Y = \overline{(A1 + A2 + A3) \cdot \{B1 + [C1 \cdot (D1 + D2)]\}}$$

FUNCTION TABLE

INPUTS							OUTPUT
A1	A2	A3	B1	C1	D1	D2	Y
H	X	X	H	X	X	X	L
X	H	X	H	X	X	X	L
X	X	H	H	X	X	X	L
(Any H)			X	H	H	X	L
(Any H)			X	H	X	H	L
Any other combination							H

description

The SN54ASC6088 and SN74ASC6088 CMOS standard-cell Boolean macros are 2-wide 2-3-input sum-of-products OR-NAND gates with 2-input OR and one available input each to the 2-input AND and OR gate to provide expandability for implementing customized product terms. The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
BF088LH	Label: BF088LH A1,A2,A3,B1,C1,D1,D2,Y;	2.5

The SN54ASC6088 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6088 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER		TEST CONDITIONS		TYP	MAX	UNIT
V_T Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		V
I_{CC} Supply current	SN54ASC6088	V_{CC} = 4.5 V to 5.5 V,	V_I = V_{CC} or 0,		318	nA
	SN74ASC6088	T_A = MIN to MAX			19.1	
C_i Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.13		pF
C_{pd} Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	$t_r = t_f$ = 3 ns,	0.99		pF

switching characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6088			SN74ASC6088			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Any A, C1	Y	C_L = 0	0.8	1.4	3.9	0.8	1.4	3.6	ns
t_{PHL}				0.4	1	2.2	0.4	1	2.1	
t_{PLH}	Any A, C1	Y	C_L = 1 pF	1.8	4.4	10.3	1.9	4.4	9.3	ns
t_{PHL}				0.9	1.8	4.3	1	1.8	3.8	
t_{PLH}	B1	Y	C_L = 0	1	1.5	2.9	1	1.5	2.7	ns
t_{PHL}				0.4	0.9	1.7	0.4	0.9	1.7	
t_{PLH}	B1	Y	C_L = 1 pF	1.7	3	6.5	1.8	3	5.9	ns
t_{PHL}				0.8	1.6	3.3	0.9	1.6	3	
t_{PLH}	Any D	Y	C_L = 0	1.4	3	7.3	1.5	3	6.6	ns
t_{PHL}				0.6	1.2	2.7	0.6	1.2	2.4	
t_{PLH}	Any D	Y	C_L = 1 pF	2.8	5.9	14	3	5.9	12.6	ns
t_{PHL}				1	2.2	5.5	1.1	2.2	4.8	
Δt_{PLH}	Any A, C1	Y		0.8	3	7	0.9	3	6.4	ns/pF
Δt_{PHL}				0.4	0.8	2.1	0.4	0.8	1.8	
Δt_{PLH}	B1	Y		0.7	1.5	3.6	0.7	1.5	3.2	ns/pF
Δt_{PHL}				0.4	0.7	1.6	0.4	0.7	1.4	
Δt_{PLH}	Any D	Y		1.4	2.9	6.7	1.5	2.9	6.1	ns/pF
Δt_{PHL}				0.4	1	2.9	0.4	1	2.5	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to the 'ASC6017 data sheet and Section 7.

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SystemCell™ 2-μm HARDWIRED MACRO CELL

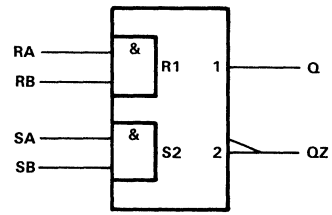
- **Provides Complementary Q and QZ Outputs**
- **Contains 2-Input Gated Set and Reset Lines**
- **Implements Summing/Decoding Registers**
- **Parallel Latches to Implement Wide Word Widths**

description

The SN54ASC6100 and SN74ASC6100 are dedicated, hardwired standard-cell macros implementing 4-input S-R latches. Setting is accomplished by taking SA and SB high; resetting is accomplished by taking RA and RB high. A full range of gated latches is offered in the 'ASC6100 and 'ASC6110 series of standard cells to provide the custom IC designer a latch element to embed in ASICs in its most efficient form. These gated latches are designed to simplify implementing summing, decoding, and other decision-making registers.

The 'ASC6100 gated latch is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE

INPUTS		OUTPUTS	
SA,SB	RA,RB	Q	QZ
Any L	Any L	Q_0	QZ_0
Both H	Any L	H	L
Any L	Both H	L	H
Both H	Both H	L‡	L‡

‡ This configuration is nonstable; that is, it will not persist when the set and reset inputs return to their inactive (L) levels.

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
GM010LH	Label: GM010LH RA,RB,SA,SB,Q,QZ;	3

The SN54ASC6100 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6100 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		MIN	MAX	UNIT
t_w Pulse duration	Any Rn or Sn low	13.8		ns
	Any Rn or Sn high	6		

electrical characteristics

PARAMETER	TEST CONDITIONS	SN54ASC6100		SN74ASC6100		UNIT
		TYP	MAX	TYP	MAX	
V_T Input threshold voltage	V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC} Supply current	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		354		21.3	nA
C_i Input capacitance	V_{CC} = 5 V, T_A = 25°C	0.13		0.13		pF
C_{pd} Equivalent power dissipation capacitance	V_{CC} = 5 V, T_A = 25°C, t_r = t_f = 3 ns,	0.75		0.75		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6100			SN74ASC6100			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Rn	$\overline{Q}$	C_L = 0	1.1	2.4	5.5	1.2	2.4	5	ns
t_{PHL}		Q		0.5	1.2	2.4	0.6	1.2	2.2	
t_{PLH}	Sn	Q		1.1	2.4	5.5	1.2	2.4	5	ns
t_{PHL}		$\overline{Q}$		0.5	1.2	2.4	0.6	1.2	2.2	
t_{PLH}	Rn	$\overline{Q}$§	C_L = 1 pF	2.7	5.8	13.5	2.9	5.8	12.1	ns
t_{PHL}		Q		1	2.2	4.9	1.1	2.2	4.4	
t_{PLH}	Sn	Q¶		2.7	5.8	13.5	2.9	5.8	12.1	ns
t_{PHL}		$\overline{Q}$		1	2.2	4.9	1.1	2.2	4.4	
Δt_{PLH}	Rn	$\overline{Q}$§		1.1	2.4	5.5	1.2	2.4	5	ns/pF
Δt_{PHL}		Q		0.5	1	2.5	0.5	1	2.2	
Δt_{PLH}	Sn	Q¶		1.1	2.4	5.5	1.2	2.4	5	ns/pF
Δt_{PHL}		$\overline{Q}$		0.5	1	2.5	0.5	1	2.2	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.
§ The internal cross coupling of gates that make up the latch is not buffered from the Q and $\overline{Q}$ outputs. Therefore, the Δt for the Q output must be added to the Δt for the $\overline{Q}$ output when calculating delays from the reset inputs to $\overline{Q}$.
¶ The internal cross coupling of gates that make up the latch is not buffered from the Q and $\overline{Q}$ outputs. Therefore, the Δt for the $\overline{Q}$ output must be added to the Δt for the Q output when calculating delays from the set inputs to Q.

DESIGN CONSIDERATIONS

designing for testability

Designers employing storage or bistable elements should consider testability of the design in its final form. The need to preset or clear these elements should be assessed throughout the development of custom logic circuits with these considerations extended to the end equipment application with respect to maintainability. Simple actions on the part of the ASIC designer can result in considerable cost savings, allowing the expense of IC testing, system testing, and system maintenance to be reduced significantly.

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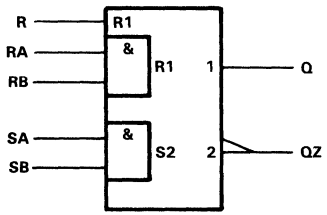
- **Provides Complementary Q and QZ Outputs**
- **Contains 2-Input Gated Set and Reset Lines Plus Separate Reset**
- **Implements Summing/Decoding Registers**
- **Parallel Latches to Implement Wide Word Widths**

description

The SN54ASC6101 and SN74ASC6101 are dedicated, hardwired standard-cell macros implementing 5-input S-R latches. Setting is accomplished by taking SA and SB high; resetting is accomplished by taking RA and RB high or R high by itself. A full range of gated latches is offered in the 'ASC6100 and 'ASC6110 series of standard cells to provide the custom IC designer a latch element to embed in ASICs in its most efficient form. These gated latches are designed to simplify implementing summing, decoding, and other decision-making registers.

The 'ASC6101 gated latch is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE

INPUTS			OUTPUTS	
SA,SB	RA,RB	R	Q	QZ
Any L	Any L	L	Q_0	QZ_0
Both H	Any L	X	H	L
Any L	Both H	X	L	H
Any L	Both X	H	L	H
Both H	Both H	X	L‡	L‡
Both H	Both X	H	L‡	L‡

‡ This configuration is nonstable; that is, it will not persist when the set and reset inputs return to their inactive (L) levels.

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
GM110LH	Label: GM110LH RA,RB,SA,SB,R,Q,QZ;	3

The SN54ASC6101 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6101 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		MIN	MAX	UNIT
t_w Pulse duration	R low	15		ns
	R high	4.8		
	RA or RB low	18.6		
	RA or RB high	6.6		
	SA or SB low	12.6		
	SA or SB high	6		

electrical characteristics

PARAMETER		TEST CONDITIONS		SN54ASC6101		SN74ASC6101		UNIT
				TYP	MAX	TYP	MAX	
V_T	Input threshold voltage	V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX			359		21.6	nA
C_i	Input capacitance	V_{CC} = 5 V,	T_A = 25°C	0.13		0.13		pF
C_{pd}	Equivalent power dissipation capacitance	V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	0.8		0.8		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6101			SN74ASC6101			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	R	QZ	C_L = 0	1	2.2	4.8	1.1	2.2	4.4	ns
t_{PHL}		Q		0.4	1	1.8	0.5	1	1.8	
t_{PLH}	Rn	QZ		0.9	2.3	5.2	1	2.3	4.7	ns
t_{PHL}		Q		0.5	1.2	2.6	0.5	1.2	2.5	
t_{PLH}	Sn	Q		1.2	2.5	5.7	1.2	2.5	5.1	ns
t_{PHL}		QZ		0.5	1.2	2.6	0.6	1.2	2.2	
t_{PLH}	R	QZ§	C_L = 1 pF	2.4	5	11.2	2.7	5	10.1	ns
t_{PHL}		Q		0.8	1.6	3.2	0.9	1.6	2.9	
t_{PLH}	Rn	QZ§		2.6	5.5	13.1	2.9	5.6	11.7	ns
t_{PHL}		Q		1	2.2	5.1	1.1	2.2	4.5	
t_{PLH}	Sn	Q¶		3	6.4	14.8	3.1	6.4	13.2	ns
t_{PHL}		QZ		1	2.2	4.9	1.1	2.2	4.3	
Δt_{PLH}	R	QZ§		1	2.2	5.1	1.1	2.2	4.6	ns/pF
Δt_{PHL}		Q		0.4	0.6	1.5	0.4	0.6	1.2	
Δt_{PLH}	Rn	QZ§		1	2.2	5.1	1.1	2.2	4.6	ns/pF
Δt_{PHL}		Q		0.5	1	2.6	0.5	1	2.2	
Δt_{PLH}	Sn	Q¶		1.4	2.9	6.7	1.5	2.9	6	ns/pF
Δt_{PHL}		QZ		0.4	1	2.5	0.5	1	2.1	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.
§ The internal cross coupling of gates that make up the latch is not buffered from the Q and QZ outputs. Therefore, the Δt for the Q output must be added to the Δt for the QZ output when calculating delays from the reset inputs to QZ.
¶ The internal cross coupling of gates that make up the latch is not buffered from the Q and QZ outputs. Therefore, the Δt for the QZ output must be added to the Δt for the Q output when calculating delays from the set inputs to Q.

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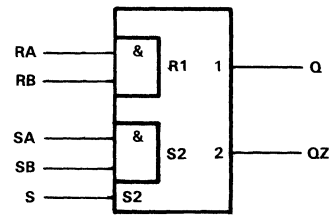
- **Contains 2-Input Gated Set and Reset Lines Plus Separate Set**
- **Implements Summing/Decoding Registers**
- **Parallel Latches to Implement Wide Word Widths**

description

The SN54ASC6102 and SN74ASC6102 are dedicated, hardwired standard-cell macros implementing 5-input S-R latches. Setting is accomplished by taking SA and SB high or S high by itself; resetting is accomplished by taking RA and RB high. A full range of gated latches is offered in the 'ASC6100 and 'ASC6110 series of standard cells to provide the custom IC designer a latch element to embed in ASICs in its most efficient form. These gated latches are designed to simplify implementing summing, decoding, and other decision-making registers.

The 'ASC6102 gated latch is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE

INPUTS			OUTPUTS	
SA,SB	RA,RB	S	Q	QZ
Any L	Any L	L	Q_0	QZ_0
Both H	Any L	X	H	L
Any L	Both H	X	L	H
Both X	Any L	H	H	L
Both H	Both H	X	L‡	L‡
Both X	Both H	H	L‡	L‡

‡ This configuration is nonstable; that is, it will not persist when the set and reset inputs return to their inactive (L) levels.

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
GMS10LH	Label: GMS10LH RA,RB,SA,SB,S,Q,QZ;	3

The SN54ASC6102 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6102 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		MIN	MAX	UNIT
t_w Pulse duration	RA or RB low	13.2		ns
	RA or RB high	6		
	S low	15		
	S high	4.8		
	SA or SB low	19.8		
	SA or SB high	6.6		

electrical characteristics

PARAMETER		TEST CONDITIONS	SN54ASC6102		SN74ASC6102		UNIT
			TYP	MAX	TYP	MAX	
V_T	Input threshold voltage	V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		355		21.3	nA
C_i	Input capacitance	V_{CC} = 5 V, T_A = 25°C	0.13		0.13		pF
C_{pd}	Equivalent power dissipation capacitance	V_{CC} = 5 V, T_A = 25°C, t_r = t_f = 3 ns,	0.79		0.79		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6102			SN74ASC6102			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Rn	QZ	C_L = 0	1.4	2.5	5.5	1.4	2.5	5	ns
t_{PHL}		Q		0.5	1.2	2.4	0.6	1.2	2.2	
t_{PLH}	S	Q		1	2.2	4.6	1.2	2.2	4.3	ns
t_{PHL}		QZ		0.4	1	1.7	0.5	1	1.7	
t_{PLH}	Sn	Q		1.1	2.5	5.3	1.2	2.5	4.8	ns
t_{PHL}		QZ		0.5	1.3	2.4	0.6	1.3	2.2	
t_{PLH}	Rn	QZ§	C_L = 1 pF	3.2	6.4	14.7	3.4	6.4	13.1	ns
t_{PHL}		Q		1	2.2	4.9	1.1	2.2	4.3	
t_{PLH}	S	Q¶		2.4	5	11.2	2.7	5	10.1	ns
t_{PHL}		QZ		0.8	1.6	3.2	0.9	1.6	2.9	
t_{PLH}	Sn	Q¶		2.6	5.6	12.9	2.9	5.6	11.5	ns
t_{PHL}		QZ		1	2.2	4.9	1.1	2.2	4.3	
Δt_{PLH}	Rn	QZ§		1.3	2.9	6.7	1.5	2.9	6	ns/pF
Δt_{PHL}		Q		0.5	1	2.5	0.5	1	2.1	
Δt_{PLH}	S	Q¶		1	2.2	5.1	1.1	2.2	4.6	ns/pF
Δt_{PHL}		QZ		0.4	0.6	1.5	0.4	0.6	1.2	
Δt_{PLH}	Sn	Q¶		1	2.2	5.1	1.1	2.2	4.6	ns/pF
Δt_{PHL}		QZ		0.5	0.9	2.5	0.5	0.9	2.1	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.
§ The internal cross coupling of gates that make up the latch is not buffered from the Q and QZ outputs. Therefore, the Δt for the Q output must be added to the Δt for the QZ output when calculating delays from the reset inputs to QZ.
¶ The internal cross coupling of gates that make up the latch is not buffered from the Q and QZ outputs. Therefore, the Δt for the QZ output must be added to the Δt for the Q output when calculating delays from the set inputs to Q.

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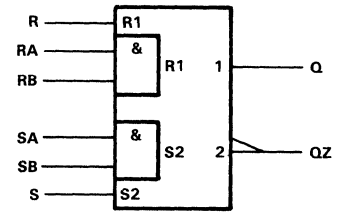
- **Contains 2-Input Gated Set and Reset Lines Plus Separate Set and Reset**
- **Implements Summing/Decoding Registers**
- **Parallel Latches to Implement Wide Word Widths**

description

The SN54ASC6103 and SN74ASC6103 are dedicated, hardwired standard-cell macros implementing 6-input S-R latches. Setting is accomplished by taking SA and SB high or S high by itself; resetting is accomplished by taking RA and RB high or R high by itself. A full range of gated latches is offered in the 'ASC6100 and 'ASC6110 series of standard cells to provide the custom IC designer a latch element to embed in ASICs in its most efficient form. These gated latches are designed to simplify implementing summing, decoding, and other decision-making registers.

The 'ASC6103 gated latch is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE

INPUTS				OUTPUTS	
SA,SB	RA,RB	S	R	Q	QZ
Any L	Any L	L	L	Q_0	QZ_0
Both H	Any L	X	X	H	L
Any L	Both H	X	X	L	H
Both X	Any L	H	L	H	L
Any L	Both X	L	H	L	H
Both H	Both H	X	X	L‡	L‡
Both X	Both X	H	H	L‡	L‡
Both H	Both X	X	H	L‡	L‡
Both X	Both H	H	X	L‡	L‡

‡ This configuration is nonstable; that is, it will not persist when the set and reset inputs return to their inactive (L) levels.

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
GM210LH	Label: GM210LH RA,RB,SA,SB,R,S,Q,QZ;	3.25

The SN54ASC6103 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6103 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		MIN	MAX	UNIT
t_w Pulse duration	R or S low	19.8		ns
	R or S high	7.2		
	RA or SA low	15		
	RA or SA high	4.8		
	RB or SB low	19.8		
	RB or SB high	7.2		

electrical characteristics

PARAMETER		TEST CONDITIONS		SN54ASC6103		SN74ASC6103		UNIT
				TYP	MAX	TYP	MAX	
V_T	Input threshold voltage	V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX			387		23.2	nA
C_i	Input capacitance	V_{CC} = 5 V,	T_A = 25°C	0.13		0.13		pF
C_{pd}	Equivalent power dissipation capacitance	V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	0.81		0.81		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6103			SN74ASC6103			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	R	QZ	C_L = 0	1	2.2	4.9	1.1	2.2	4.4	ns
t_{PHL}		Q		0.4	1	1.8	0.4	1	1.7	
t_{PLH}	Rn	QZ		1.1	2.4	5.6	1.2	2.4	5	ns
t_{PHL}		Q		0.5	1.2	2.5	0.5	1.2	2.2	
t_{PLH}	S	Q		1	2.2	4.7	1.1	2.2	4.3	ns
t_{PHL}		QZ		0.4	1	1.8	0.5	1	1.7	
t_{PLH}	Sn	Q		1.1	2.4	5.5	1.2	2.4	4.9	ns
t_{PHL}		QZ		0.5	1.2	2.6	0.6	1.2	2.3	
t_{PLH}	R	QZ§	C_L = 1 pF	2.7	5.5	12.4	2.9	5.5	11.1	ns
t_{PHL}		Q		0.8	1.6	3.2	0.9	1.6	2.8	
t_{PLH}	Rn	QZ§		2.9	6.1	14.2	3.1	6.1	12.6	ns
t_{PHL}		Q		1	2.2	4.9	1.1	2.2	4.3	
t_{PLH}	S	Q¶		2.7	5.5	12.4	2.9	5.5	11.1	ns
t_{PHL}		QZ		0.8	1.6	3.2	0.9	1.6	2.8	
t_{PLH}	Sn	Q¶		2.9	6.1	14.2	3.1	6.1	12.6	ns
t_{PHL}		QZ		1	2.2	4.9	1.1	2.2	4.3	
Δt_{PLH}	R	QZ§		1.3	2.7	6.2	1.3	2.7	5.6	ns/pF
Δt_{PHL}		Q		0.4	0.6	1.4	0.4	0.6	1.2	
Δt_{PLH}	Rn	QZ§		1.3	2.7	6.2	1.3	2.7	5.6	ns/pF
Δt_{PHL}		Q		0.5	1	2.5	0.5	1	2.1	
Δt_{PLH}	S	Q¶		1.3	2.7	6.2	1.3	2.7	5.6	ns/pF
Δt_{PHL}		QZ		0.4	0.6	1.4	0.4	0.6	1.2	
Δt_{PLH}	Sn	Q¶		1.3	2.7	6.2	1.3	2.7	5.6	ns/pF
Δt_{PHL}		QZ		0.5	1	2.5	0.5	1	2.1	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.
§ The internal cross coupling of gates that make up the latch is not buffered from the Q and QZ outputs. Therefore, the Δt for the Q output must be added to the Δt for the QZ output when calculating delays from the reset inputs to QZ.
¶ The internal cross coupling of gates that make up the latch is not buffered from the Q and QZ outputs. Therefore, the Δt for the QZ output must be added to the Δt for the Q output when calculating delays from the set inputs to Q.

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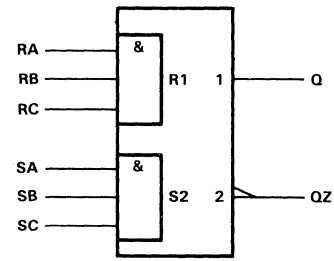
- **Provides Complementary Q and QZ Outputs**
- **Contains 3-Input Gated Set and Reset Lines**
- **Implements Summing/Decoding Registers**
- **Parallel Latches to Implement Wide Word Widths**

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The SN54ASC6105 and SN74ASC6105 are dedicated, hardwired standard-cell macros implementing 6-input S-R latches. Setting is accomplished by taking SA, SB, and SC high; resetting is accomplished by taking RA, RB, and RC high. A full range of gated latches is offered in the 'ASC6100 and 'ASC6110 series of standard cells to provide the custom IC designer a latch element to embed in ASICs in its most efficient form. These gated latches are designed to simplify implementing summing, decoding, and other decision-making registers.

The 'ASC6105 gated latch is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

FUNCTION TABLE

INPUTS		OUTPUTS	
SA,SB,SC	RA,RB,RC	Q	QZ
Any L	Any L	Q_0	QZ_0
All H	Any L	H	L
Any L	All H	L	H
All H	All H	L‡	L‡

‡ This configuration is nonstable; that is, it will not persist when the set and reset inputs return to their inactive (L) level.

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
GM310LH	Label: GM310LH RA,RB,RC,SA,SB,SC,Q,QZ;	2.75

The SN54ASC6105 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6105 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2

timing requirements over recommended ranges of supply voltage and operating free-air temperature

			MIN	MAX	UNIT
t_w	Pulse duration	Any Rn or Sn low	13.8		ns
		Any Rn or Sn high	6.6		

electrical characteristics

PARAMETER		TEST CONDITIONS	SN54ASC6105		SN74ASC6105		UNIT
			TYP	MAX	TYP	MAX	
V_T	Input threshold voltage	V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		334		20	nA
C_i	Input capacitance	V_{CC} = 5 V, T_A = 25°C	0.13		0.13		pF
C_{pd}	Equivalent power dissipation capacitance	V_{CC} = 5 V, T_A = 25°C, t_r = t_f = 3 ns,	0.8		0.8		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6105			SN74ASC6105			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Rn	QZ	C_L = 0	1	2.3	5.5	1.1	2.3	4.8	ns
t_{PHL}		Q		0.5	1.3	3	0.6	1.3	2.6	
t_{PLH}	Sn	Q		1	2.3	5.5	1.1	2.3	4.8	ns
t_{PHL}		QZ		0.5	1.3	2.9	0.6	1.3	2.6	
t_{PLH}	Rn	QZ§	C_L = 1 pF	2.8	6.2	14.9	3	6.2	13.2	ns
t_{PHL}		Q		1.1	2.6	6.4	1.2	2.6	5.6	
t_{PLH}	Sn	Q¶		2.8	6.2	14.9	3	6.2	13.2	ns
t_{PHL}		QZ		1.1	2.6	6.4	1.2	2.6	5.6	
Δt_{PLH}	Rn	QZ§		1.2	2.6	5.9	1.3	2.6	5.3	ns/pF
Δt_{PHL}		Q		0.6	1.3	3.4	0.6	1.3	2.9	
Δt_{PLH}	Sn	Q¶		1.2	2.6	5.9	1.3	2.6	5.3	ns/pF
Δt_{PHL}		QZ		0.6	1.3	3.4	0.6	1.3	2.9	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.
§ The internal cross coupling of gates that make up the latch is not buffered from the Q and QZ outputs. Therefore, the Δt for the Q output must be added to the Δt for the QZ output when calculating delays from the reset inputs to QZ.
¶ The internal cross coupling of gates that make up the latch is not buffered from the Q and QZ outputs. Therefore, the Δt for the QZ output must be added to the Δt for the Q output when calculating delays from the set inputs to Q.

DESIGN CONSIDERATIONS

designing for testability

Designers employing storage or bistable elements should consider testability of the design in its final form. The need to preset or clear these elements should be assessed throughout the development of custom logic circuits with these considerations extended to the end equipment application with respect to maintainability. Simple actions on the part of the ASIC designer can result in considerable cost savings, allowing the expense of IC testing, system testing, and system maintenance to be reduced significantly.

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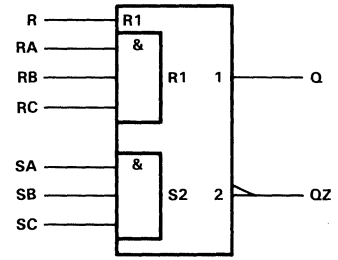
- **Contains 3-Input Gated Set and Reset Lines Plus Separate Reset**
- **Implements Summing/Decoding Registers**
- **Parallel Latches to Implement Wide Word Widths**

description

The SN54ASC6106 and SN74ASC6106 are dedicated, hardwired standard-cell macros implementing 7-input S-R latches. Setting is accomplished by taking SA, SB, and SC high; resetting is accomplished by taking RA, RB, and RC high or R high by itself. A full range of gated latches is offered in the 'ASC6100 and 'ASC6110 series of standard cells to provide the custom IC designer a latch element to embed in ASICs in its most efficient form. These gated latches are designed to simplify implementing summing, decoding, and other decision-making registers.

The 'ASC6106 gated latch is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE

INPUTS			OUTPUTS	
SA,SB,SC	RA,RB,RC	R	Q	QZ
Any L	Any L	L	Q_0	QZ_0
All H	Any L	X	H	L
Any L	All H	X	L	H
Any L	All X	H	L	H
All H	All H	X	L‡	L‡
All H	All X	H	L‡	L‡

‡This configuration is nonstable; that is, it will not persist when the set and reset inputs return to their inactive (L) levels.

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
GM410LH	Label: GM410LH RA,RB,RC,SA,SB,SC,R,Q,QZ;	3

The SN54ASC6106 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6106 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		MIN	MAX	UNIT
t_w Pulse duration	R low	13.2		ns
	R high	4.8		
	RA, RB, or RC low	21		
	RA, RB, or RC high	7.8		
	SA, SB, or SC low	12.6		
	SA, SB, or SC high	6.6		

electrical characteristics

PARAMETER		TEST CONDITIONS	SN54ASC6106		SN74ASC6106		UNIT
			TYP	MAX	TYP	MAX	
V_T	Input threshold voltage	V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		359		21.5	nA
C_i	Input capacitance	V_{CC} = 5 V, T_A = 25°C	0.13		0.13		pF
C_{pd}	Equivalent power dissipation capacitance	V_{CC} = 5 V, t_r = t_f = 3 ns, T_A = 25°C	0.85		0.85		pF

4 Data Sheets

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6106			SN74ASC6106			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	R	QZ	C_L = 0	0.9	1.8	4	0.9	1.8	3.6	ns
t_{PHL}		Q		0.4	1	1.8	0.4	1	1.7	
t_{PLH}	Rn	QZ		1	2.3	5.7	1.1	2.3	4.8	ns
t_{PHL}		Q		0.5	1.4	3.5	0.6	1.4	3	
PLH	Sn	Q		1.1	2.5	5.9	1.2	2.5	5.2	ns
t_{PHL}		QZ		0.5	1.3	2.9	0.6	1.3	2.5	
t_{PLH}	R	QZ§	C_L = 1 pF	2.3	4.6	10.2	2.5	4.6	9.3	ns
t_{PHL}		Q		0.8	1.6	3.1	0.9	1.6	2.9	
t_{PLH}	Rn	QZ§		2.7	5.8	13.9	2.9	5.8	11.8	ns
t_{PHL}		Q		1.2	2.8	6.8	1.3	2.8	5.9	
t_{PLH}	Sn	Q¶		3	6.6	16	3.3	6.6	14.1	ns
t_{PHL}		QZ		1.1	2.6	6.3	1.2	2.6	5.5	
Δt_{PLH}	R	QZ§		1	2.2	5	1.1	2.2	4.5	ns/pF
Δt_{PHL}		Q		0.4	0.6	1.4	0.4	0.6	1.2	
Δt_{PLH}	Rn	QZ§		1	2.1	5	1.1	2.1	4.5	ns/pF
Δt_{PHL}		Q		0.6	1.4	3.6	0.6	1.4	3.1	
Δt_{PLH}	Sn	Q¶		1.3	2.8	6.6	1.4	2.8	5.9	ns/pF
Δt_{PHL}		QZ		0.6	1.3	3.5	0.6	1.3	3	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.
§ The internal cross coupling of gates that make up the latch is not buffered from the Q and QZ outputs. Therefore, the Δt for the Q output must be added to the Δt for the QZ output when calculating delays from the reset inputs to QZ.
¶ The internal cross coupling of gates that make up the latch is not buffered from the Q and QZ outputs. Therefore, the Δt for the QZ output must be added to the Δt for the Q output when calculating delays from the set inputs to Q.

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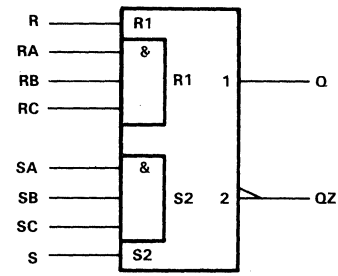
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The SN54ASC6108 and SN74ASC6108 are dedicated, hardwired standard-cell macros implementing 8-input S-R latches. Setting is accomplished by taking SA, SB, and SC high or S high by itself; resetting is accomplished by taking RA, RB, and RC high or R high by itself. A full range of gated latches is offered in the 'ASC6100 and 'ASC6110 series of standard cells to provide the custom IC designer a latch element to embed in ASICs in its most efficient form. These gated latches are designed to simplify implementing summing, decoding, and other decision-making registers.

The 'ASC6108 gated latch is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

FUNCTION TABLE

INPUTS				OUTPUTS	
SA,SB,SC	RA,RB,RC	S	R	Q	QZ
Any L	Any L	L	L	Q_0	QZ_0
All H	Any L	X	X	H	L
Any L	All H	X	X	L	H
All X	Any L	H	L	H	L
Any L	All X	L	H	L	H
All H	All H	X	X	L‡	L‡
All X	All X	H	H	L‡	L‡
All H	All X	X	H	L‡	L‡
All X	All H	H	X	L‡	L‡

‡ This configuration is nonstable; that is, it will not persist when the set and reset inputs return to their inactive (L) levels.

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
GM510LH	Label: GM510LH RA,RB,RC,SA,SB,SC,R,S,Q,QZ;	3.25

The SN54ASC6108 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6108 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		MIN	MAX	UNIT
t_w Pulse duration	R or S low	13.8		ns
	R or S high	4.8		
	Any Rn or Sn low	21		
	Any Rn or Sn high	8.4		

electrical characteristics

PARAMETER		TEST CONDITIONS	SN54ASC6108		SN74ASC6108		UNIT
			TYP	MAX	TYP	MAX	
V_T	Input threshold voltage	V_{CC} = 5 V, T_A = 25°C	2.2		2.2.		V
I_{CC}	Supply current	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		395		23.7	nA
C_i	Input capacitance	V_{CC} = 5 V, T_A = 25°C	0.13		0.13		pF
C_{pd}	Equivalent power dissipation capacitance	V_{CC} = 5 V, t_r = t_f = 3 ns, T_A = 25°C	0.86		0.86		pF

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6108			SN74ASC6108			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	R	$\overline{Q}Z$	C_L = 0	1	2.1	4.5	1.1	2.1	4.1	ns
t_{PHL}		Q		0.4	1	1.7	0.4	1	1.7	
t_{PLH}	Rn	$\overline{Q}Z$		1.1	2.5	6	1.2	2.5	5.3	ns
t_{PHL}		Q		0.5	1.4	3.3	0.6	1.4	2.9	
t_{PLH}	S	Q		1	2.1	4.5	1.1	2.1	4.1	ns
t_{PHL}		$\overline{Q}Z$		0.4	1	1.7	0.4	1	1.7	
t_{PLH}	Sn	Q		1.1	2.5	6	1.2	2.5	5.3	ns
t_{PHL}		$\overline{Q}Z$		0.5	1.4	3.3	0.6	1.4	2.9	
t_{PLH}	R	$\overline{Q}Z$§	C_L = 1 pF	2.6	5.2	11.6	2.8	5.2	10.6	ns
t_{PHL}		Q		0.8	1.6	3.1	0.9	1.6	2.9	
t_{PLH}	Rn	$\overline{Q}Z$§		3	6.4	15.3	3.2	6.4	13.6	ns
t_{PHL}		Q		1.2	2.8	6.8	1.3	2.8	5.9	
t_{PLH}	S	Q¶		2.6	5.2	11.6	2.8	5.2	10.6	ns
t_{PHL}		$\overline{Q}Z$		0.8	1.6	3.1	0.9	1.6	2.9	
t_{PLH}	Sn	Q¶		3	6.4	15.3	3.2	6.4	13.6	ns
t_{PHL}		$\overline{Q}Z$		1.2	2.8	6.8	1.3	2.8	5.9	
Δt_{PLH}	R	$\overline{Q}Z$§		1.2	2.5	5.8	1.3	2.5	5.2	ns/pF
Δt_{PHL}		Q		0.4	0.6	1.4	0.4	0.6	1.2	
Δt_{PLH}	Rn	$\overline{Q}Z$§		1.2	2.5	5.8	1.3	2.5	5.2	ns/pF
Δt_{PHL}		Q		0.6	1.4	3.6	0.6	1.4	3.1	
Δt_{PLH}	S	Q¶		1.2	2.5	5.8	1.3	2.5	5.2	ns/pF
Δt_{PHL}		$\overline{Q}Z$		0.4	0.6	1.4	0.4	0.6	1.2	
Δt_{PLH}	Sn	Q¶		1.2	2.5	5.8	1.3	2.5	5.2	ns/pF
Δt_{PHL}		$\overline{Q}Z$		0.6	1.4	3.6	0.6	1.4	3.1	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.
§ The internal cross coupling of gates that make up the latch is not buffered from the Q and $\overline{Q}Z$ outputs. Therefore, the Δt for the Q output must be added to the Δt for the $\overline{Q}Z$ output when calculating delays from the reset inputs to $\overline{Q}Z$.
¶ The internal cross coupling of gates that make up the latch is not buffered from the Q and $\overline{Q}Z$ outputs. Therefore, the Δt for the $\overline{Q}Z$ output must be added to the Δt for the Q output when calculating delays from the set inputs to Q.

DESIGN CONSIDERATIONS

designing for testability

Designers employing storage or bistable elements should consider testability of the design in its final form. The need to preset or clear these elements should be assessed throughout the development of custom logic circuits with these considerations extended to the end equipment application with respect to maintainability. Simple actions on the part of the ASIC designer can result in considerable cost savings, allowing the expense of IC testing, system testing, and system maintenance to be reduced significantly.

power-up clear/preset

These standard cell latch elements can be asynchronously set or reset. They can be connected through an inverter to the SN54ASC2320 or SN74ASC2320 power-up clear cell to achieve system initialization. Control of the set or reset inputs from another system signal in conjunction with the power-up clear can be achieved with an OR gate.

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SystemCell™ 2-μm HARDWIRED MACRO CELL

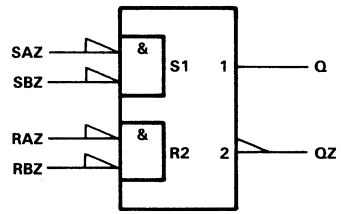
- **Provides Complementary Q and QZ Outputs**
- **Contains 2-Input Gated Set and Reset Lines**
- **Implements Summing/Decoding Registers**
- **Parallel Latches to Implement Wide Word Widths**

description

The SN54ASC6110 and SN74ASC6110 are dedicated, hardwired standard-cell macros implementing 4-input S̄-R̄ latches. Setting is accomplished by taking SAZ and SBZ low; resetting is accomplished by taking RAZ and RBZ low. A full range of gated latches is offered in the 'ASC6100 and 'ASC6110 series of standard cells to provide the custom IC designer a latch element to embed in ASICs in its most efficient form. These gated latches are designed to simplify implementing summing, decoding, and other decision-making registers.

The 'ASC6110 gated latch is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE

INPUTS		OUTPUTS	
SAZ,SBZ	RAZ,RBZ	Q	QZ
Any H	Any H	Q_0	QZ_0
Both L	Any H	H	L
Any H	Both L	L	H
Both L	Both L	H‡	H‡

‡ This configuration is nonstable; that is, it will not persist when the set and reset inputs return to their inactive (H) levels.

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
GS010LH	Label: GS010LH RAZ,RBZ,SAZ,SBZ,Q,QZ;	2.75

The SN54ASC6110 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6110 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		MIN	MAX	UNIT
t_w Pulse duration	Any RnZ or SnZ low	11.4		ns
	Any RnZ or SnZ high	4.5		

electrical characteristics

PARAMETER		TEST CONDITIONS	SN54ASC6110		SN74ASC6110		UNIT
			TYP	MAX	TYP	MAX	
V_T	Input threshold voltage	V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		323		19.4	nA
C_i	Input capacitance	V_{CC} = 5 V, T_A = 25°C	0.13		0.13		pF
C_{pd}	Equivalent power dissipation capacitance	V_{CC} = 5 V, t_r = t_f = 3 ns, T_A = 25°C	0.72		0.72		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6110			SN74ASC6110			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	RnZ	QZ	C_L = 0	0.9	1.5	3.1	0.9	1.5	2.8	ns
t_{PHL}		Q		1.2	2.3	5.2	1.3	2.3	4.7	
t_{PLH}	SnZ	Q		0.9	1.5	3.2	0.9	1.5	2.9	ns
t_{PHL}		QZ		1.2	2.3	5.3	1.3	2.3	4.7	
t_{PLH}	RnZ	QZ	C_L = 1 pF	1.8	3.5	7.7	1.9	3.5	7	ns
t_{PHL}		Q§		2.9	6.2	14.5	3.1	6.2	13	
t_{PLH}	SnZ	Q		1.8	3.5	7.7	1.9	3.5	7	ns
t_{PHL}		QZ¶		2.9	6.2	14.5	3.1	6.2	13	
Δt_{PLH}	RnZ	QZ		0.9	2	4.6	1	2	4.2	ns/pF
Δt_{PHL}		Q§		0.8	1.9	4.7	0.9	1.9	4.1	
Δt_{PLH}	SnZ	Q		0.9	2	4.6	1	2	4.2	ns/pF
Δt_{PHL}		QZ		0.8	1.9	4.7	0.9	1.9	4.1	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.
§ The internal cross coupling of gates that make up the latch is not buffered from the Q and QZ outputs. Therefore, the Δt for the QZ output must be added to the Δt for the Q output when calculating delays from the reset inputs to Q.
¶ The internal cross coupling of gates that make up the latch is not buffered from the Q and QZ outputs. Therefore, the Δt for the Q output must be added to the Δt for the QZ output when calculating delays from the set inputs to QZ.

DESIGN CONSIDERATIONS

designing for testability

Designers employing storage or bistable elements should consider testability of the design in its final form. The need to preset or clear these elements should be assessed throughout the development of custom logic circuits with these considerations extended to the end equipment application with respect to maintainability. Simple actions on the part of the ASIC designer can result in considerable cost savings, allowing the expense of IC testing, system testing, and system maintenance to be reduced significantly.

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SystemCell™ 2-μm HARDWIRED MACRO CELL

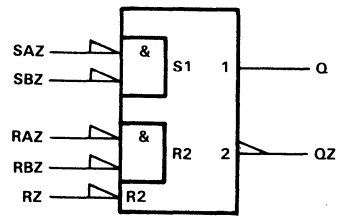
- Provides Complementary Q and QZ Outputs
- Contains 2-Input Gated Set and Reset Lines Plus Separate Reset
- Implements Summing/Decoding Registers
- Parallel Latches to Implement Wide Word Widths

description

The SN54ASC6111 and SN74ASC6111 are dedicated, hardwired standard-cell macros implementing 5-input $\overline{S}$-$\overline{R}$ latches. Setting is accomplished by taking SAZ and SBZ low; resetting is accomplished by taking RAZ and RBZ low or RZ low by itself. A full range of gated latches is offered in the 'ASC6100 and 'ASC6110 series of standard cells to provide the custom IC designer a latch element to embed in ASICs in its most efficient form. These gated latches are designed to simplify implementing summing, decoding, and other decision-making registers.

The 'ASC6111 gated latch is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE

INPUTS			OUTPUTS	
SAZ,SBZ	RAZ,RBZ	RZ	Q	QZ
Any H	Any H	H	Q_0	QZ_0
Both L	Any H	H	H	L
Any H	Both L	X	L	H
Any H	Both X	L	L	H
Both L	Both L	X	H‡	H‡
Both L	Both X	L	H‡	H‡

‡ This configuration is nonstable; that is, it will not persist when the set and reset inputs return to their inactive (L) levels.

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
GS110LH	Label: GS110LH RAZ,RBZ,SAZ,SBZ,RZ,Q,QZ;	3

The SN54ASC6111 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6111 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		MIN	MAX	UNIT
t_w Pulse duration	RZ low	7.2		ns
	RZ high	6.6		
	Any RnZ low	13.8		
	Any RnZ high	8.4		
	Any SnZ low	13.8		
	Any SnZ high	6		

electrical characteristics

PARAMETER		TEST CONDITIONS		SN54ASC6111		SN74ASC6111		UNIT
				TYP	MAX	TYP	MAX	
V_T	Input threshold voltage	V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current	V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX	V_I = V_{CC} or 0,		355		21.3	nA
C_i	Input capacitance	V_{CC} = 5 V,	T_A = 25°C	0.13		0.13		pF
C_{pd}	Equivalent power dissipation capacitance	V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	0.84		0.84		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6111			SN74ASC6111			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	RZ	QZ	C_L = 0	0.8	1.1	1.9	0.8	1.1	1.8	ns
t_{PHL}		Q		1.1	1.9	4	1.2	1.9	3.6	
t_{PLH}	RnZ	QZ		0.9	1.7	3.9	1	1.7	3.5	ns
t_{PHL}		Q		1.2	2.5	5.9	1.3	2.5	5.3	
t_{PLH}	SnZ	Q		0.9	1.6	3.5	1	1.6	3.2	ns
t_{PHL}		QZ		1.4	2.7	6.4	1.4	2.7	5.7	
t_{PLH}	RZ	QZ	C_L = 1 pF	1.3	2.1	4.2	1.3	2.1	3.9	ns
t_{PHL}		Q§		2.3	4.4	10.1	2.4	4.4	9	
t_{PLH}	RnZ	QZ		1.9	3.7	8.3	2	3.7	7.6	ns
t_{PHL}		Q§		2.9	6	14.2	3.1	6	12.7	
t_{PLH}	SnZ	Q		1.9	3.6	8	2	3.6	7.3	ns
t_{PHL}		QZ¶		3.3	6.8	16.3	3.5	6.8	14.5	
Δt_{PLH}	RZ	QZ		0.5	1	2.3	0.5	1	2.1	ns/pF
Δt_{PHL}		Q§		0.7	1.5	3.8	0.7	1.5	3.4	
Δt_{PLH}	RnZ	QZ		0.9	2	4.5	1	2	4.1	ns/pF
Δt_{PHL}		Q§		0.7	1.5	3.8	0.7	1.5	3.4	
Δt_{PLH}	SnZ	Q		0.9	2	4.5	1	2	4.1	ns/pF
Δt_{PHL}		QZ§		0.9	2.1	5.3	1	2.1	4.7	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.
§ The internal cross coupling of gates that make up the latch is not buffered from the Q and QZ outputs. Therefore, the Δt for the QZ output must be added to the Δt for the Q output when calculating delays from the reset inputs to Q.
¶ The internal cross coupling of gates that make up the latch is not buffered from the Q and QZ outputs. Therefore, the Δt for the Q output must be added to the Δt for the QZ output when caclulating delays from the set inputs to QZ.

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DESIGN CONSIDERATIONS

designing for testability

Designers employing storage or bistable elements should consider testability of the design in its final form. The need to preset or clear these elements should be assessed throughout the development of custom logic circuits with these considerations extended to the end equipment application with respect to maintainability. Simple actions on the part of the ASIC designer can result in considerable cost savings, allowing the expense of IC testing, system testing, and system maintenance to be reduced significantly.

power-up clear/preset

These standard cell latch elements can be asynchronously reset. They can be connected to the SN54ASC2320 or SN74ASC2320 power-up clear cell to achieve system initialization. Control of the reset input from another system signal in conjunction with the power-up clear can be achieved with an AND gate.

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SystemCell™ 2-μm HARDWIRED MACRO CELL

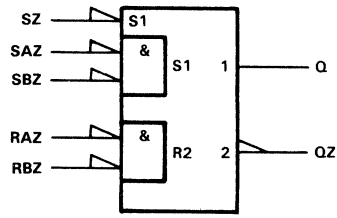
- **Provides Complementary Q and QZ Outputs**
- **Contains 2-Input Gated Set and Reset Lines Plus Separate Set**
- **Implements Summing/Decoding Registers**
- **Parallel Latches to Implement Wide Word Widths**

description

The SN54ASC6112 and SN74ASC6112 are dedicated, hardwired standard-cell macros implementing 5-input S̄-R̄ latches. Setting is accomplished by taking SAZ and SBZ low or SZ low by itself; resetting is accomplished by taking RAZ and RBZ low. A full range of gated latches is offered in the 'ASC6100 and 'ASC6110 series of standard cells to provide the custom IC designer a latch element to embed in ASICs in its most efficient form. These gated latches are designed to simplify implementing summing, decoding, and other decision-making registers.

The 'ASC6112 gated latch is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE

INPUTS			OUTPUTS	
SAZ,SBZ	RAZ,RBZ	SZ	Q	QZ
Any H	Any H	H	Q_0	QZ_0
Both L	Any H	X	H	L
Any H	Both L	H	L	H
Both X	Any H	L	H	L
Both L	Both L	X	H‡	H‡
Both X	Both L	L	H‡	H‡

‡ This configuration is nonstable; that is, it will not persist when the set and reset inputs return to their inactive (H) levels.

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
GSS10LH	Label: GSS10LH RAZ,RBZ,SAZ,SBZ,SZ,Q,QZ;	3

The SN54ASC6112 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6112 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		MIN	MAX	UNIT
t_w Pulse duration	RAZ or RBZ low	13.2		ns
	RAZ or RBZ high	6		
	SZ low	7.8		
	SZ high	6.6		
	SAZ or SBZ low	13.8		
	SAZ or SBZ high	8.4		

electrical characteristics

PARAMETER		TEST CONDITIONS	SN54ASC6112		SN74ASC6112		UNIT
			TYP	MAX	TYP	MAX	
V_T	Input threshold voltage	V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		355		21.3	nA
C_i	Input capacitance	V_{CC} = 5 V, T_A = 25°C	0.13		0.13		pF
C_{pd}	Equivalent power dissipation capacitance	V_{CC} = 5 V, t_r = t_f = 3 ns, T_A = 25°C	0.84		0.84		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6112			SN74ASC6112			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	RnZ	QZ	C_L = 0	0.9	1.6	3.5	1	1.6	3.2	ns
t_{PHL}		Q		1.4	2.7	6.4	1.4	2.7	5.7	
t_{PLH}	SZ	Q		0.8	1.1	1.9	0.8	1.1	1.8	ns
t_{PHL}		QZ		1.1	1.9	4	1.2	1.9	3.6	
t_{PLH}	SnZ	Q		0.9	1.7	3.9	1	1.7	3.5	ns
t_{PHL}		QZ		1.2	2.5	5.9	1.3	2.5	5.3	
t_{PLH}	RnZ	QZ	C_L = 1 pF	1.9	3.6	8	2	3.6	7.3	ns
t_{PHL}		Q§		3.3	6.8	16.3	3.5	6.8	14.5	
t_{PLH}	SZ	Q		1.3	2.1	4.2	1.3	2.1	3.9	ns
t_{PHL}		QZ¶		2.3	4.4	10.1	2.4	4.4	9	
t_{PLH}	SnZ	Q		1.9	3.7	8.3	2	3.7	7.6	ns
t_{PHL}		QZ¶		2.9	6	14.2	3.1	6	12.7	
Δt_{PLH}	RnZ	QZ		0.9	2	4.5	1	2	4.1	ns/pF
Δt_{PHL}		Q§		0.9	2.1	5.3	1	2.1	4.7	
Δt_{PLH}	SZ	Q		0.5	1	2.3	0.5	1	2.1	ns/pF
Δt_{PHL}		QZ¶		0.7	1.5	3.8	0.7	1.5	3.4	
Δt_{PLH}	SnZ	Q		0.9	2	4.5	1	2	4.1	ns/pF
Δt_{PHL}		QZ¶		0.7	1.5	3.8	0.7	1.5	3.4	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.
§ The internal cross coupling of gates that make up the latch is not buffered from the Q and QZ outputs. Therefore, the Δt for the QZ output must be added to the Δt for the Q output when calculating delays from the reset inputs to Q.
¶ The internal cross coupling of gates that make up the latch is not buffered from the Q and QZ outputs. Therefore, the Δt for the Q output must be added to the Δt for the QZ output when calculating delays from the set inputs to QZ.

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SystemCell™ 2-μm HARDWIRED MACRO CELL

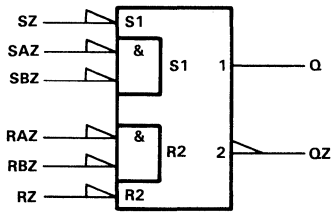
- **Provides Complementary Q and QZ Outputs**
- **Contains 2-Input Gated Set and Reset Lines Plus Separate Set and Reset**
- **Implements Summing/Decoding Registers**
- **Parallel Latches to Implement Wide Word Widths**

description

The SN54ASC6113 and SN74ASC6113 are dedicated, hardwired standard-cell macros implementing 6-input S̄-R̄ latches. Setting is accomplished by taking SAZ and SBZ low or SZ low by itself; resetting is accomplished by taking RAZ and RBZ low or RZ low by itself. A full range of gated latches is offered in the 'ASC6100 and 'ASC6110 series of standard cells to provide the custom IC designer a latch element to embed in ASICs in its most efficient form. These gated latches are designed to simplify implementing summing, decoding, and other decision-making registers.

The 'ASC6113 gated latch is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE

INPUTS				OUTPUTS	
SAZ,SBZ	RAZ,RBZ	SZ	RZ	Q	QZ
Any H	Any H	H	H	Q_0	QZ_0
Both L	Any H	X	H	H	L
Any H	Both L	H	X	L	H
Both X	Any H	L	H	H	L
Any H	Both X	H	L	L	H
Both L	Both L	X	X	H‡	H‡
Both X	Both X	L	L	H‡	H‡
Both L	Both X	X	L	H‡	H‡
Both X	Both L	L	X	H‡	H‡

‡ This configuration is nonstable; that is, it will not persist when the set and reset inputs return to their inactive (H) levels.

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
GS210LH	Label: GS210LH RAZ,RBZ,SAZ,SBZ,RZ,SZ,Q,QZ;	3

The SN54ASC6113 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6113 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		MIN	MAX	UNIT
t_w Pulse duration	RZ or SZ low	7.2		ns
	RZ or SZ high	6.6		
	RAZ or RBZ low	12.6		
	RAZ or RBZ high	7.8		
	SAZ or SBZ low	13.8		
	SAZ or SBZ high	7.8		

electrical characteristics

PARAMETER		TEST CONDITIONS	SN54ASC6113		SN74ASC6113		UNIT
			TYP	MAX	TYP	MAX	
V_T	Input threshold voltage	V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		359		21.5	nA
C_i	Input capacitance	V_{CC} = 5 V, T_A = 25°C	0.13		0.13		pF
C_{pd}	Equivalent power dissipation capacitance	V_{CC} = 5 V, t_r = t_f = 3 ns, T_A = 25°C	0.84		0.84		pF

TEXAS INSTRUMENTS
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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6113			SN74ASC6113			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	RZ	QZ	C_L = 0	0.8	1.1	1.9	0.8	1.1	1.8	ns
t_{PHL}		Q		1.2	1.9	4.2	1.2	1.9	3.8	
t_{PLH}	RnZ	QZ		0.9	1.7	3.6	0.9	1.7	3.3	ns
t_{PHL}		Q		1.3	2.5	6	1.3	2.5	5.3	
t_{PLH}	SZ	Q		0.8	1.1	1.9	0.8	1.1	1.8	ns
t_{PHL}		QZ		1.2	1.9	4.2	1.2	1.9	3.8	
t_{PLH}	SnZ	Q		0.9	1.7	3.9	1	1.7	3.5	ns
t_{PHL}		QZ		1.3	2.5	6.2	1.4	2.5	5.5	
t_{PLH}	RZ	QZ	C_L = 1 pF	1.3	2.1	4.1	1.3	2.1	3.8	ns
t_{PHL}		Q§		2.4	4.7	10.9	2.5	4.7	9.7	
t_{PLH}	RnZ	QZ		1.8	3.5	7.8	1.9	3.5	7.1	ns
t_{PHL}		Q§		2.9	6.1	14.6	3.1	6.1	13	
t_{PLH}	SZ	Q		1.3	2.1	4.1	1.3	2.1	3.8	ns
t_{PHL}		QZ¶		2.4	4.7	10.9	2.5	4.7	9.7	
t_{PLH}	SnZ	Q		1.8	3.5	7.8	1.9	3.5	7.1	ns
t_{PHL}		QZ¶		2.9	6.1	14.6	3.1	6.1	13	
Δt_{PLH}	RZ	QZ		0.4	1	2.3	0.5	1	2.1	ns/pF
Δt_{PHL}		Q§		0.7	1.8	4.4	0.8	1.8	3.8	
Δt_{PLH}	RnZ	QZ		0.8	1.8	4.3	0.9	1.8	3.8	ns/pF
Δt_{PHL}		Q§		0.7	1.8	4.4	0.8	1.8	3.8	
Δt_{PLH}	SZ	Q		0.4	1	2.3	0.5	1	2.1	ns/pF
Δt_{PHL}		QZ¶		0.7	1.8	4.4	0.8	1.8	3.8	
Δt_{PLH}	SnZ	Q		0.8	1.8	4.3	0.9	1.8	3.8	ns/pF
Δt_{PHL}		QZ¶		0.7	1.8	4.4	0.8	1.8	3.8	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f = 3$ ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.
§ The internal cross coupling of gates that make up the latch is not buffered from the Q and QZ outputs. Therefore, the Δt for the QZ output must be added to the Δt for the Q output when calculating delays from the reset inputs to Q.
¶ The internal cross coupling of gates that make up the latch is not buffered from the Q and QZ outputs. Therefore, the Δt for the Q output must be added to the Δt for the QZ output when calculating delays from the set inputs to QZ.

DESIGN CONSIDERATIONS

designing for testability

Designers employing storage or bistable elements should consider testability of the design in its final form. The need to preset or clear these elements should be assessed throughout the development of custom logic circuits with these considerations extended to the end equipment application with respect to maintainability. Simple actions on the part of the ASIC designer can result in considerable cost savings, allowing the expense of IC testing, system testing, and system maintenance to be reduced significantly.

power-up clear/preset

These standard cell latch elements can be asynchronously set or reset. They can be connected to the SN54ASC2320 or SN74ASC2320 power-up clear cell to achieve system initialization. Control of the set or reset inputs from another system signal in conjunction with the power-up clear can be achieved with an AND gate.

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SystemCell™ 2-μm HARDWIRED MACRO CELL

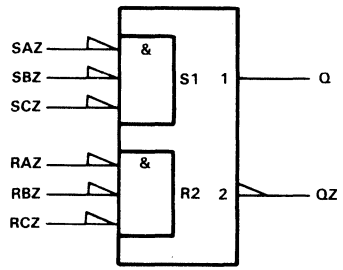
- **Provides Complementary Q and QZ Outputs**
- **Contains 3-Input Gated Set and Reset Lines**
- **Implements Summing/Decoding Registers**
- **Parallel Latches to Implement Wide Word Widths**

description

The SN54ASC6115 and SN74ASC6115 are dedicated, hardwired standard-cell macros implementing 6-input S-R latches. Setting is accomplished by taking SAZ, SBZ, and SCZ low; resetting is accomplished by taking RAZ, RBZ, and RCZ low. A full range of gated latches is offered in the 'ASC6100 and 'ASC6110 series of standard cells to provide the custom IC designer a latch element to embed in ASICs in its most efficient form. These gated latches are designed to simplify implementing summing, decoding, and other decision-making registers.

The 'ASC6115 gated latch is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE

INPUTS		OUTPUTS	
SAZ,SBZ,SCZ	RAZ,RBZ,RCZ	Q	QZ
Any H	Any H	Q_0	QZ_0
Both L	Any H	H	L
Any H	Both L	L	H
Both L	Both L	H‡	H‡

‡ This configuration is nonstable; that is, it will not persist when the set and reset inputs return to their inactive (H) levels.

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
GS310LH	Label: GS310LH RAZ,RBZ,RCZ,SAZ,SBZ,SCZ,Q,QZ;	2.75

The SN54ASC6115 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6115 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

timing requirements over recommended ranges of operating free-air temperature and supply voltage

		MIN	MAX	UNIT
t_w Pulse duration	Any RnZ or SnZ low	17.4		ns
	Any RnZ or SnZ high	6		

electrical characteristics

PARAMETER	TEST CONDITIONS	SN54ASC6115		SN74ASC6115		UNIT
		TYP	MAX	TYP	MAX	
V_T Input threshold voltage	V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC} Supply current	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		332		19.9	nA
C_i Input capacitance	V_{CC} = 5 V, T_A = 25°C	0.13		0.13		pF
C_{pd} Equivalent power dissipation capacitance	V_{CC} = 5 V, T_A = 25°C, $t_r = t_f$ = 3 ns,	0.75		0.75		pF

switching characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6115			SN74ASC6115			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	RnZ	QZ	C_L = 0	1	2	4.9	1.1	2	4.4	ns
t_{PHL}		Q		1.4	2.9	7.3	1.4	2.9	6.5	
t_{PLH}	SnZ	Q		1	1.9	4.9	1.1	1.9	4.4	ns
t_{PHL}		QZ		1.3	2.8	7.3	1.4	2.8	6.5	
t_{PLH}	RnZ	QZ	C_L = 1 pF	2.4	4.8	11.5	2.5	4.8	10.4	ns
t_{PHL}		Q§		3.6	7.8	19.2	3.9	7.8	17.2	
t_{PLH}	SnZ	Q		2.4	4.8	11.5	2.5	4.8	10.4	ns
t_{PHL}		QZ¶		3.6	7.8	19.2	3.9	7.8	17.2	
Δt_{PLH}	RnZ	QZ		1.3	2.8	6.6	1.4	2.8	6	ns/pF
Δt_{PHL}		Q§		0.9	2.1	5.3	1	2.1	4.7	
Δt_{PLH}	SnZ	Q		1.3	2.9	6.6	1.4	2.9	6	ns/pF
Δt_{PHL}		QZ¶		0.9	2.1	5.3	1	2.1	4.7	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ RnZ/SnZ to QZ/Q = RnZ to QZ and SnZ to Q.
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.
§ The internal cross coupling of gates that make up the latch is not buffered from the Q and QZ outputs. Therefore, the Δt for the QZ output must be added to the Δt for the Q output when calculating delays from the reset inputs to Q.
¶ The internal cross coupling of gates that make up the latch is not buffered from the Q and QZ outputs. Therefore, the Δt for the Q output must be added to the Δt for the QZ output when calculating delays from the set inputs to QZ.

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SystemCell™ 2-μm HARDWIRED MACRO CELL

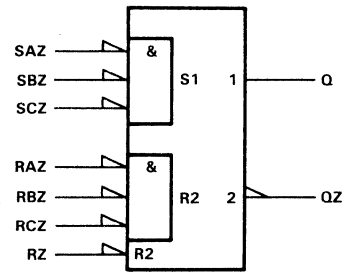
- **Provides Complementary Q and QZ Outputs**
- **Contains 3-Input Gated Set and Reset Lines Plus Separate Reset**
- **Implements Summing/Decoding Registers**
- **Parallel Latches to Implement Wide Word Widths**

description

The SN54ASC6116 and SN74ASC6116 are dedicated, hardwired standard-cell macros implementing 7-input S̄-R̄ latches. Setting is accomplished by taking SAZ, SBZ, and SCZ low; resetting is accomplished by taking RAZ, RBZ, and RCZ low or RZ low by itself. A full range of gated latches is offered in the 'ASC6100 and 'ASC6110 series of standard cells to provide the custom IC designer a latch element to embed in ASICs in its most efficient form. These gated latches are designed to simplify implementing summing, decoding, and other decision-making registers.

The 'ASC6116 gated latch is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12

FUNCTION TABLE

INPUTS			OUTPUTS	
SAZ,SBZ,SCZ	RAZ,RBZ,RCZ	RZ	Q	QZ
Any H	Any H	H	Q_0	QZ_0
All L	Any H	H	H	L
Any H	All L	X	L	H
Any H	All X	L	L	H
All L	All L	X	H‡	H‡
All L	All X	L	H‡	H‡

‡This configuration is nonstable; that is, it will not persist when the set and reset inputs return to their inactive (H) levels.

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
GS410LH	Label: GS410LH RAZ,RBZ,RCZ,SAZ,SBZ,SCZ,RZ,Q,QZ;	3.25

The SN54ASC6116 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6116 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		MIN	MAX	UNIT
t_w Pulse duration	RZ low	7.2		ns
	RZ high	6.6		
	Any RnZ low	22.2		
	Any RnZ high	9		
	Any SnZ low	21		
	Any SnZ high	6.6		

electrical characteristics

PARAMETER		TEST CONDITIONS	SN54ASC6116		SN74ASC6116		UNIT
			TYP	MAX	TYP	MAX	
V_T	Input threshold voltage	V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		384		23.1	nA
C_i	Input capacitance	V_{CC} = 5 V, T_A = 25°C	0.13		0.13		pF
C_{pd}	Equivalent power dissipation capacitance	V_{CC} = 5 V, T_A = 25°C, t_r = t_f = 3 ns,	0.85		0.85		pF

switching characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6116			SN74ASC6116			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	RZ	QZ	C_L = 0	0.8	1.1	1.8	0.8	1.1	1.7	ns
t_{PHL}		Q		1.1	1.7	3.7	1.1	1.7	3.3	
t_{PLH}	RnZ	QZ		1.2	2.4	6	1.2	2.4	5.4	ns
t_{PHL}		Q		1.5	3.1	7.9	1.5	3.1	7	
t_{PLH}	SnZ	Q		1.1	2.1	5.2	1.1	2.1	4.7	ns
t_{PHL}		QZ		1.5	3.2	8.3	1.6	3.2	7.3	
t_{PLH}	RZ	QZ	C_L = 1 pF	1.3	2	4	1.3	2	3.8	ns
t_{PHL}		Q§		2.3	4.2	9.7	2.4	4.2	8.8	
t_{PLH}	RnZ	QZ		2.6	5.4	12.9	2.8	5.4	11.6	ns
t_{PHL}		Q§		3.6	7.6	18.6	3.9	7.6	16.6	
t_{PLH}	SnZ	Q		2.5	5.1	12.1	2.7	5.1	10.9	ns
t_{PHL}		QZ¶		3.9	8.5	21	4.3	8.5	18.7	
Δt_{PLH}	RZ	QZ		0.4	1	2.3	0.5	1	2	ns/pF
Δt_{PHL}		Q§		0.6	1.5	3.8	0.7	1.5	3.4	
Δt_{PLH}	RnZ	QZ		1.4	3	6.9	1.5	3	6.2	ns/pF
Δt_{PHL}		Q§		0.6	1.5	3.8	0.7	1.5	3.4	
Δt_{PLH}	SnZ	Q		1.4	3	6.9	1.5	3	6.2	ns/pF
Δt_{PHL}		QZ¶		1	2.3	5.9	1.1	2.3	5.1	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.
§ The internal cross coupling of gates that make up the latch is not buffered from the Q and QZ outputs. Therefore, the Δt for the QZ output must be added to the Δt for the Q output when calculating delays from the reset inputs to Q.
¶ The internal cross coupling of gates that make up the latch is not buffered from the Q and QZ outputs. Therefore, the Δt for the Q output must be added to the Δt for the QZ output when calculating delays from the set inputs to QZ.

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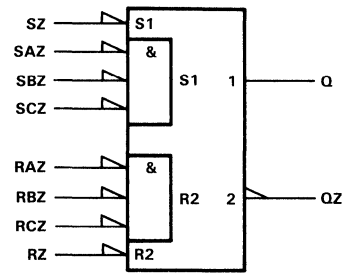
SystemCell™ 2-μm HARDWIRED MACRO CELL

- **Provides Complementary Q and QZ Outputs**
- **Contains 3-Input Gated Set and Reset Lines Plus Separate Set and Reset**
- **Implements Summing/Decoding Registers**
- **Parallel Latches to Implement Wide Word Widths**

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The SN54ASC6118 and SN74ASC6118 are dedicated, hardwired standard-cell macros implementing 8-input S̄-R̄ latches. Setting is accomplished by taking SAZ, SBZ, and SCZ low or SZ low by itself; resetting is accomplished by taking RAZ, RBZ, and RCZ low or RZ low by itself. A full range of gated latches is offered in the 'ASC6100 and 'ASC6110 series of standard cells to provide the custom IC designer a latch element to embed in ASICs in its most efficient form. These gated latches are designed to simplify implementing summing, decoding, and other decision-making registers.

The 'ASC6118 gated latch is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
GS510LH	Label: GS510LH RAZ,RBZ,RCZ,SAZ,SBZ,SCZ,RZ,SZ,Q,QZ;	3.25

The SN54ASC6118 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6118 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

INPUTS				OUTPUTS	
SAZ,SBZ,SCZ	RAZ,RBZ,RCZ	SZ	RZ	Q	QZ
Any H	Any H	H	H	Q_0	QZ_0
All L	Any H	X	H	H	L
Any H	All L	H	X	L	H
All X	Any H	L	H	H	L
Any H	All X	H	L	L	H
All L	All L	X	X	H‡	H‡
All X	All X	L	L	H‡	H‡
All L	All X	X	L	H‡	H‡
All X	All L	L	X	H‡	H‡

‡ This configuration is nonstable; that is, it will not persist when the set and reset inputs return to their inactive (H) levels.

timing requirements over recommended ranges of operating free-air temperature and supply voltage

		MIN	MAX	UNIT
t_w Pulse duration	RZ or SZ low	7.8		ns
	RZ or SZ high	6		
	Any RnZ or SnZ low	22.2		
	Any RnZ or SnZ high	9		

electrical characteristics

PARAMETER		TEST CONDITIONS	SN54ASC6118		SN74ASC6118		UNIT
			TYP	MAX	TYP	MAX	
V_T	Input threshold voltage	V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		395		23.7	nA
C_i	Input capacitance	V_{CC} = 5 V, T_A = 25°C	0.13		0.13		pF
C_{pd}	Equivalent power dissipation capacitance	V_{CC} = 5 V, t_r = t_f = 3 ns, T_A = 25°C	0.89		0.89		pF

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6118			SN74ASC6118			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	RZ	QZ	C_L = 0	0.8	1.1	1.9	0.8	1.1	1.8	ns
t_{PHL}		Q		1.1	1.9	4.1	1.2	1.9	3.7	
t_{PLH}	RnZ	QZ		1.2	2.4	6.1	1.2	2.4	5.5	ns
t_{PHL}		Q		1.5	3.2	8.4	1.6	3.2	7.5	
t_{PLH}	SZ	Q		0.8	1.1	1.9	0.8	1.1	1.8	ns
t_{PHL}		QZ		1.2	1.9	4.2	1.2	1.9	3.7	
t_{PLH}	SnZ	Q		1.2	2.5	6.3	1.3	2.5	5.7	ns
t_{PHL}		QZ		1.6	3.3	8.3	1.7	3.3	7.7	
t_{PLH}	RZ	QZ	C_L = 1 pF	1.3	2.1	4.1	1.3	2.1	3.8	ns
t_{PHL}		Q§		2.4	4.6	10.6	2.5	4.6	9.4	
t_{PLH}	RnZ	QZ		2.6	5.4	12.9	2.8	5.4	11.7	ns
t_{PHL}		Q§		3.7	7.9	19.3	4	7.9	17.3	
t_{PLH}	SZ	Q		1.3	2.1	4.1	1.3	2.1	3.8	ns
t_{PHL}		QZ¶		2.4	4.6	10.6	2.5	4.6	9.5	
t_{PLH}	SnZ	Q		2.7	5.5	13.2	2.8	5.5	11.9	ns
t_{PHL}		QZ¶		3.7	8	19.7	4	8	17.5	
Δt_{PLH}	RZ	QZ		0.4	1	2.3	0.5	1	2	ns/pF
Δt_{PHL}		Q§		0.7	1.7	4.2	0.8	1.7	3.7	
Δt_{PLH}	RnZ	QZ		1.4	3	6.9	1.5	3	6.2	ns/pF
Δt_{PHL}		Q§		0.7	1.7	4.2	0.8	1.7	3.7	
Δt_{PLH}	SZ	Q		0.4	1	2.3	0.5	1	2	ns/pF
Δt_{PHL}		QZ¶		0.7	1.7	4.2	0.8	1.7	3.7	
Δt_{PLH}	SnZ	Q		1.4	3	6.9	1.5	3	6.2	ns/pF
Δt_{PHL}		QZ¶		0.7	1.7	4.2	0.8	1.7	3.7	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.
§ The internal cross coupling of gates that make up the latch is not buffered from the Q and QZ outputs. Therefore, the Δt for the QZ output must be added to the Δt for the Q output when calculating delays from the reset inputs to Q.
¶ The internal cross coupling of gates that make up the latch is not buffered from the Q and QZ outputs. Therefore, the Δt for the Q output must be added to the Δt for the QZ output when calculating delays from the set inputs to QZ.

DESIGN CONSIDERATIONS

designing for testability

Designers employing storage or bistable elements should consider testability of the design in its final form. The need to preset or clear these elements should be assessed throughout the development of custom logic circuits with these considerations extended to the end equipment application with respect to maintainability. Simple actions on the part of the ASIC designer can result in considerable cost savings, allowing the expense of IC testing, system testing, and system maintenance to be reduced significantly.

power-up clear/preset

These standard cell latch elements can be asynchronously set or reset. They can be connected to the SN54ASC2320 or SN74ASC2320 power-up clear cell to achieve system initialization. Control of the set or reset inputs from another system signal in conjunction with the power-up clear can be achieved with an AND gate.

TEXAS INSTRUMENTS
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D2939, AUGUST 1986

SystemCell™ 2-μm INTERNAL STANDARD CELL

- **Symmetrical Delay Buffers ($t_{PLH} \approx t_{PHL}$)**
- **Choice of Two Performance Levels of Delay Lines**
- **Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V**
- **Functional Operation Over V_{CC} Range of 2 V to 6 V**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol

positive logic equation

$Y = A$

description

The SN54ASC6120 and SN74ASC6120 are two internal delay buffer standard cells that provide the ASIC designer with symmetrical delay elements that can be used to implement signal path delay-line management techniques needed to ensure timing integrity. Each option is designated and called from the engineering workstation input using the following cell names to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		TYPICAL DELAY C_L = 1 pF	RELATIVE CELL AREA TO NA210LH
BU120LH	Label: BU1n0LH A,Y;	1.7 ns	1.5
BU130LH		1.7 ns	1.75

The SN54ASC6120 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6120 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS		BU120LH TYP	BU120LH MAX	BU130LH TYP	BU130LH MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current	SN54ASC6120	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0,			187		214	nA
		SN74ASC6120	T_A = MIN to MAX			11.2		12.9	
C_i	Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.13		0.13		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	$t_r = t_f$ = 3 ns,	1.29		1.73		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

BU120LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6120			SN74ASC6120			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	C_L = 0	0.4	0.9	2.3	0.5	0.9	2.1	ns
t_{PHL}				0.8	1.2	2.8	0.9	1.2	2.6	
t_{PLH}	A	Y	C_L = 1 pF	0.7	1.6	3.4	0.8	1.6	3.1	ns
t_{PHL}				1	1.7	3.6	1.1	1.7	3.3	
Δt_{PLH}	A	Y		0.2	0.5	1.2	0.2	0.5	1.1	ns/pF
Δt_{PHL}				0.1	0.3	0.8	0.1	0.3	0.7	

BU130LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6120			SN74ASC6120			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	C_L = 0	0.6	1.3	2.6	0.6	1.3	2.4	ns
t_{PHL}				0.9	1.5	3.2	0.9	1.5	2.9	
t_{PLH}	A	Y	C_L = 1 pF	0.8	1.6	3.4	0.8	1.6	3.1	ns
t_{PHL}				1	1.8	3.8	1.1	1.8	3.5	
Δt_{PLH}	A	Y		0.1	0.3	0.8	0.2	0.3	0.8	ns/pF
Δt_{PHL}				0.1	0.3	0.7	0.1	0.3	0.6	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to Section 7.

TEXAS INSTRUMENTS
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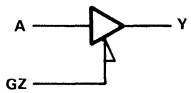
SystemCell™ 2-μm INTERNAL STANDARD CELL

- Choice of Two Performance Levels
- Active Low Enable
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol



FUNCTION TABLE

INPUTS		OUTPUT
GZ	A	Y
L	H	H
L	L	L
H	X	Z

positive logic equation

$Y = A$

description

The SN54ASC6121 and SN74ASC6121 are noninverting 3-state internal buffer standard cells that interface internal cells with internal buses. The standard-cell library contains two physical implementations providing the custom IC designer a choice from two performance levels for optimizing designs. Each option is designated and called from the engineering workstation input using the following cell names to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		TYPICAL DELAY C_L = 1 pF	RELATIVE CELL AREA TO NA210LH
BU221LH	Label: BU2n1LH A,GZ,Y;	2.3 ns	2.75
BU261LH		2 ns	4.75

The SN54ASC6121 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6121 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS	BU221LH TYP	BU221LH MAX	BU261LH TYP	BU261LH MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current	SN54ASC6121	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0,		328		562	nA
		SN74ASC6121	T_A = MIN to MAX		19.7		33.7	
C_i	Input capacitance	A	V_{CC} = 5 V, T_A = 25°C	0.14		0.28		pF
		GZ		0.32		0.28		
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C, t_r = t_f = 3 ns,	1.62		3.29		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

BU221LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6121			SN74ASC6121			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	C_L = 0	0.6	1.5	3.6	0.7	1.5	3.2	ns
t_{PHL}				1	1.6	3.4	1	1.6	3.1	
t_{PLH}	A	Y	C_L = 1 pF	1.1	2.5	5.8	1.2	2.5	5.3	ns
t_{PHL}				1.2	2.1	4.6	1.2	2.1	4.2	
t_{PZH}	GZ	Y	C_L = 1 pF, R_L = 40 kΩ to GND	0.7	1.4	2.9	0.7	1.4	2.7	ns
t_{PZL}	GZ	Y	C_L = 1 pF, R_L = 20 kΩ to V_{CC}	1	1.6	3.4	1	1.6	3.1	ns
t_{PHZ}	GZ	Y	C_L = 1 pF, R_L = 40 kΩ to GND		10			10		ns
t_{PLZ}	GZ	Y	C_L = 1 pF, R_L = 20 kΩ to V_{CC}		5.3			5.3		ns
Δt_{PLH}	A	Y		0.5	1	2.3	0.5	1	2.1	ns/pF
Δt_{PHL}				0.2	0.5	1.3	0.2	0.5	1.1	
Δt_{PZH}	GZ	Y		0.5	0.9	2.2	0.5	0.9	2	ns/pF
Δt_{PZL}				0.2	0.5	1.3	0.2	0.5	1.2	

BU261LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6121			SN74ASC6121			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	C_L = 0	0.7	1.5	3.3	0.8	1.5	2.9	ns
t_{PHL}				1.2	2	4.1	1.2	2	3.8	
t_{PLH}	A	Y	C_L = 1 pF	0.8	1.7	3.8	0.9	1.7	3.4	ns
t_{PHL}				1.3	2.2	4.6	1.3	2.2	4.2	
t_{PZH}	GZ	Y	C_L = 1 pF, R_L = 40 kΩ to GND	1.2	2.2	4.8	1.2	2.2	4.3	ns
t_{PZL}	GZ	Y	C_L = 1 pF, R_L = 20 kΩ to V_{CC}	1.1	2	4.4	1.1	2	4	ns
t_{PHZ}	GZ	Y	C_L = 1 pF, R_L = 40 kΩ to GND		16			16		ns
t_{PLZ}	GZ	Y	C_L = 1 pF, R_L = 20 kΩ to V_{CC}		7.4			7.4		ns
Δt_{PLH}	A	Y		0.1	0.2	0.5	0.1	0.2	0.5	ns/pF
Δt_{PHL}				0.1	0.2	0.6	0.1	0.2	0.5	
Δt_{PZH}	GZ	Y		0.1	0.2	0.5	0.1	0.2	0.5	ns/pF
Δt_{PZL}				0.1	0.2	0.7	0.1	0.2	0.6	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
t_{PHZ} ≡ output disable time from high level
t_{PLZ} ≡ output disable time from low level
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
Δt_{PZH} ≡ change in Δt_{PZH} with load capacitance
Δt_{PZL} ≡ change in Δt_{PZL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to Section 7.

TEXAS INSTRUMENTS
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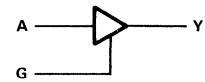
SystemCell™ 2-μm INTERNAL STANDARD CELL

- Choice of Two Performance Levels
- Active-High Enable
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol



FUNCTION TABLE

INPUTS		OUTPUT
G	A	Y
H	H	H
H	L	L
L	X	Z

positive logic equation

$Y = A$

description

The SN54ASC6122 and SN74ASC6122 are noninverting 3-state internal buffer standard cells that interface internal cells with internal buses. The standard-cell library contains two physical implementations providing the custom IC designer a choice from two performance levels for optimizing designs. Each option is designated and called from the engineering workstation input using the following cell names to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		TYPICAL DELAY C_L = 1 pF	RELATIVE CELL AREA TO NA210LH
BU222LH	Label: BU2n2LH A,G,Y;	2.3 ns	2.75
BU262LH		2 ns	4.75

The SN54ASC6122 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6122 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER		TEST CONDITIONS		BU222LH TYP	BU222LH MAX	BU262LH TYP	BU262LH MAX	UNIT
V_I Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC} Supply current	SN54ASC6122	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0,			328		562	nA
	SN74ASC6122	T_A = MIN to MAX			19.7		33.7	
C_i Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.14		0.28		pF
C_{pd} Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	$t_r = t_f$ = 3 ns,	1.62		3.3		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

BU222LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6122			SN74ASC6122			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	C_L = 0	0.6	1.6	3.6	0.7	1.6	3.3	ns
t_{PHL}				1	1.5	3.3	1	1.5	3	
t_{PLH}	A	Y	C_L = 1 pF	1.1	2.6	5.9	1.2	2.6	5.3	ns
t_{PHL}				1.2	2	4.5	1.2	2	4.1	
t_{PZH}	G	Y	C_L = 1 pF, R_L = 40 kΩ to GND	0.8	1.8	4.2	0.9	1.8	3.8	ns
t_{PZL}	G	Y	C_L = 1 pF, R_L = 20 kΩ to V_{CC}	0.4	1.1	2.5	0.4	1.1	2.3	ns
t_{PHZ}	G	Y	C_L = 1 pF, R_L = 40 kΩ to GND		11			11		ns
t_{PLZ}	G	Y	C_L = 1 pF, R_L = 20 kΩ to V_{CC}		4.5			4.5		ns
Δt_{PLH}	A	Y		0.5	1	2.3	0.5	1	2.1	ns/pF
Δt_{PHL}				0.2	0.5	1.3	0.2	0.5	1.1	
Δt_{PZH}	G	Y		0.4	1.1	2.4	0.5	1.1	2.2	ns/pF
Δt_{PZL}				0.4	0.6	1.3	0.4	0.6	1.1	

BU262LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6122			SN74ASC6122			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	C_L = 0	0.7	1.5	3.3	0.8	1.5	3	ns
t_{PHL}				1.2	2	4.1	1.2	2	3.8	
t_{PLH}	A	Y	C_L = 1 pF	0.8	1.7	3.8	0.9	1.7	3.4	ns
t_{PHL}				1.3	2.2	4.6	1.3	2.2	4.2	
t_{PZH}	G	Y	C_L = 1 pF, R_L = 40 kΩ to GND	0.6	1.5	3.4	0.7	1.5	3	ns
t_{PZL}	G	Y	C_L = 1 pF, R_L = 20 kΩ to V_{CC}	0.9	2.3	5.6	1	2.3	5	ns
t_{PHZ}	G	Y	C_L = 1 pF, R_L = 40 kΩ to GND		16			16		ns
t_{PLZ}	G	Y	C_L = 1 pF, R_L = 20 kΩ to V_{CC}		8			8		ns
Δt_{PLH}	A	Y		0.1	0.2	0.5	0.1	0.2	0.5	ns/pF
Δt_{PHL}				0.1	0.2	0.6	0.1	0.2	0.5	
Δt_{PZH}	G	Y		0.1	0.2	0.6	0.1	0.2	0.5	ns/pF
Δt_{PZL}				0.1	0.2	0.7	0.1	0.2	0.6	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
t_{PHZ} ≡ output disable time from high level
t_{PLZ} ≡ output disable time from low level
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
Δt_{PZH} ≡ change in Δt_{PZH} with load capacitance
Δt_{PZL} ≡ change in Δt_{PZL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

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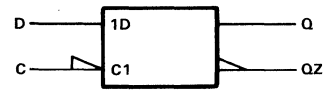
D2939, AUGUST 1986

SystemCell™ 2-μm HARDWIRED MACRO CELL

- **Provides Complementary Q and QZ Outputs**
- **Transparent When Enable Is Low**
- **Implements Control/Status Registers**
- **Parallel Latches to Implement Wide Word Widths**

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The SN54ASC6125 and SN74ASC6125 are dedicated, hardwired standard-cell macros implementing bistable latches. The 'ASC6125 latches provide an active-low enable, C, with a transparent storage element to embed in ASICs in its most efficient form. The 'ASC6125 latches implement identical function and sequential operation to one-fourth of the 'LS75 packaged latches except the 'ASC125 enable is active-low and available on each individual latch.

FUNCTION TABLE

INPUTS		OUTPUT	
D	C	Q	QZ
L	L	L	H
H	L	H	L
X	H	Q_0	QZ_0

Information present at the data (D) input is transferred to the Q output when the enable input is low, and the Q output will follow the data input as long as enable remains low. When enable goes high, the data (that was present at the data input at the time the transition occurred) are retained at the Q output until the enable is again taken low. The cells are designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	RELATIVE CELL AREA TO NA210LH
LAL20LH	Label: LALn0LH D,C,Q,QZ;	4.25

The SN54ASC6125 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6125 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			MIN	MAX	UNIT
t_w	Pulse duration	C low	9		ns
t_{su}	Setup time	D high or low	10.8		
t_h	Hold time	D high or low	0		

electrical characteristics

PARAMETER		TEST CONDITIONS	SN54ASC6125		SN74ASC6125		UNIT
			TYP	MAX	TYP	MAX	
V_T Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC} Supply current		V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		505		30.3	nA
C_i Input Capacitance	D	V_{CC} = 5 V, TA = 25°C	0.27		0.27		pF
	C		0.28		0.28		
C_{pd} Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C, t_r = t_f = 3 ns,	4.68		4.68		pF

switching characteristics over recommended ranges of supply volatge and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6125			SN74ASC6125			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	D	Q	C_L = 0	1.8	4.2	10.7	1.9	4.2	9.5	ns
t_{PHL}				1.3	2.5	5.9	1.4	2.5	5.3	
t_{PLH}	D	QZ		2	4	10	2.1	4	8.9	ns
t_{PHL}				1.1	2.8	6.9	1.2	2.8	6.2	
t_{PLH}	C	Q		2.1	4	9.4	2.2	4	8.4	ns
t_{PHL}				1.5	2.6	5.7	1.6	2.6	5.2	
t_{PLH}	C	QZ		2.1	4.1	9.7	2.3	4.1	8.7	ns
t_{PHL}				1.5	2.5	5.8	1.6	2.5	5.2	
t_{PLH}	D	Q	C_L = 1 pF	2	4.7	11.8	2.2	4.7	10.5	ns
t_{PHL}				1.5	3	7	1.6	3	6.3	
t_{PLH}	D	QZ		2.2	4.5	11.1	2.4	4.5	9.9	ns
t_{PHL}				1.3	3.2	8	1.5	3.2	7.2	
t_{PLH}	C	Q		2.3	4.5	10.5	2.4	4.5	9.4	ns
t_{PHL}				1.7	3	6.8	1.8	3	6.2	
t_{PLH}	C	QZ		2.4	4.6	10.8	2.5	4.6	9.6	ns
t_{PHL}				1.7	3	6.9	1.8	3	6.2	
Δt_{PLH}	Any	Q,QZ		0.2	0.5	1.1	0.2	0.5	1	ns/pF
Δt_{PHL}				0.1	0.5	1.1	0.2	0.5	1	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with t_r = t_f = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V. T_A = 25°C.

TEXAS INSTRUMENTS
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DESIGN CONSIDERATIONS

interfacing the macro

Inputs and outputs of these dedicated macros are compatible for interfacing directly with cells and macros available in the TI standard cell library. The inputs can be driven by either noninverting or inverting input cells. The outputs can be interfaced to drive off-chip loads with any of the noninverting output buffers or interfaced to external bidirectional buses through a 3-state input/output TTL/CMOS buffer.

designing for testability

Designers employing storage or bistable elements should consider testability of the design in its final form. The need to preset or clear these elements should be assessed throughout the development of custom logic circuits with these considerations extended to the end equipment application with respect to maintainability. Simple actions on the part of the ASIC designer can result in considerable cost savings, allowing the expense of IC testing, system testing, and system maintenance to be reduced significantly.

power-up clear/preset

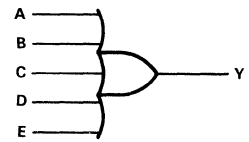
Standard cell storage elements containing the capability to be asynchronously preset or cleared may be connected to the SN54ASC2320 or SN74ASC2320 power-up clear cell to achieve system initialization. Control of the clear or preset inputs from another system signal in conjunction with the power-up clear can be achieved with an AND gate.

D2939, AUGUST 1986

SystemCell™ 2-μm INTERNAL STANDARD CELL

- **3.4 ns Typical Propagation Delay With 1-pF Load**
- **Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V**
- **Functional Operation Over V_{CC} Range of 2 V to 6 V**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

positive logic equation

$$Y = A+B+C+D+E = \overline{\overline{A}\cdot\overline{B}\cdot\overline{C}\cdot\overline{D}\cdot\overline{E}}$$

FUNCTION TABLE

INPUTS					OUTPUT
A	B	C	D	E	Y
H	X	X	X	X	H
X	H	X	X	X	H
X	X	H	X	X	H
X	X	X	H	X	H
X	X	X	X	H	H
L	L	L	L	L	L

description

The SN54ASC6130 and SN74ASC6130 are 5-input positive-OR gate CMOS standard cells. Each cell is designated and called from the engineering workstation input using the following cell names to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		TYPICAL DELAY C_L = 1 pF	RELATIVE CELL AREA TO NA210LH
OR510LH	Label: OR510LH A,B,C,D,E,Y;	3.4 ns	2.25

The SN54ASC6130 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6130 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER		TEST CONDITIONS		TYP	MAX	UNIT
V_T Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		V
I_{CC} Supply current	SN54ASC6130	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0,			255	nA
	SN74ASC6130	T_A = MIN to MAX			15.3	
C_i Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.11		pF
C_{pd} Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	$t_r = t_f$ = 3 ns,	1.11		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6130			SN74ASC6130			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A thru E	Y	C_L = 0	0.9	1.8	4	1	1.8	3.6	ns
t_{PHL}				1.4	3.1	9.1	1.4	3.1	8.2	
t_{PLH}	A thru E	Y	C_L = 1 pF	1.4	2.8	6.3	1.5	2.8	5.7	ns
t_{PHL}				1.7	4	11.3	1.9	4	10	
Δt_{PLH}	A thru E	Y		0.4	1	2.4	0.5	1	2.2	ns/pF
Δt_{PHL}				0.3	0.9	2.2	0.4	0.9	1.9	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to Section 7.

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

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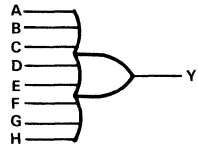
D2939, AUGUST 1986

SystemCell™ 2-μm INTERNAL STANDARD CELL

- **3.3 ns Typical Propagation Delay with 1-pF Load**
- **Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V**
- **Functional Operation Over V_{CC} Range of 2 V to 6 V**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol



positive logic equation

$Y = A+B+C+D+E+F+G+H = \overline{\overline{A}\,\overline{B}\,\overline{C}\,\overline{D}\,\overline{E}\,\overline{F}\,\overline{G}\,\overline{H}}$

FUNCTION TABLE

INPUTS								OUTPUTS
A	B	C	D	E	F	G	H	Y
H	X	X	X	X	X	X	X	H
X	H	X	X	X	X	X	X	H
X	X	H	X	X	X	X	X	H
X	X	X	H	X	X	X	X	H
X	X	X	X	H	X	X	X	H
X	X	X	X	X	H	X	X	H
X	X	X	X	X	X	H	X	H
X	X	X	X	X	X	X	H	H
L	L	L	L	L	L	L	L	L

description

The SN54ASC6131 and SN74ASC6131 are 8-input positive-OR gate CMOS standard cells. Each cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		TYPICAL DELAY C_L = 1 pF	RELATIVE CELL AREA TO NA210LH
OR810LH	Label: OR810LH A,B,C,D,E,F,G,H,Y;	3.3 ns	3.25

The SN54ASC6131 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6131 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS		TYP	MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		V
I_{CC}	Supply current	SN54ASC6131	V_{CC} = 4.5 V to 5.5 V,	V_I = V_{CC} or 0,		384	nA
		SN74ASC6131	T_A = MIN to MAX			23.1	
C_i	Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.11		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	1.16		pF

switching characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6131			SN74ASC6131			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A thru H	Y	C_L = 0	0.8	1.7	3.9	0.8	1.7	3.5	ns
t_{PHL}				1.3	2.9	7.4	1.4	2.9	6.6	
t_{PLH}	A thru H	Y	C_L = 1 pF	1.3	2.7	6.1	1.4	2.7	5.5	ns
t_{PHL}				1.8	3.9	10.2	1.9	3.9	9	
Δt_{PLH}	A thru H	Y		0.4	1	2.3	0.5	1	2.1	ns/pF
Δt_{PHL}				0.4	1	2.8	0.5	1	2.4	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f = 3$ ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to Section 7.

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

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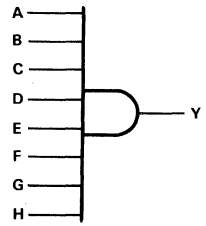
D2939, AUGUST 1986

SystemCell™ 2-μm INTERNAL STANDARD CELL

- 3.4 ns Typical Propagation Delay
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

logic symbol



positive logic equations

$$Y = A\,B\,C\,D\,E\,F\,G\,H = \overline{\overline{A}+\overline{B}+\overline{C}+\overline{D}+\overline{E}+\overline{F}+\overline{G}+\overline{H}}$$

FUNCTION TABLE

INPUTS								OUTPUT
A	B	C	D	E	F	G	H	Y
H	H	H	H	H	H	H	H	H
Any other combination								L

description

The SN54ASC6132 and SN74ASC6132 are 8-input positive-AND gate CMOS standard cells. Each cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		TYPICAL DELAY C_L = 1 pF	RELATIVE CELL AREA TO NA210LH
AN810LH	Label: AN810LH A,B,C,D,E,F,G,H,Y;	3.4 ns	3.25

The SN54ASC6132 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC6132 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		V
I_{CC}	Supply current	SN54ASC6132	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		403	nA
		SN74ASC6132			24.2	
C_i	Input capacitance		V_{CC} = 5 V, T_A = 25°C	0.13		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, t_r = t_f = 3 ns, T_A = 25°C	1.22		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC6132			SN74ASC6132			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A thru H	Y	C_L = 0	0.9	2.2	5.3	1	2.2	4.7	ns
t_{PHL}				0.8	1.9	3.9	0.8	1.9	3.6	
t_{PLH}	A thru H	Y	C_L = 1 pF	1.9	4.2	9.8	2	4.2	8.8	ns
t_{PHL}				1.1	2.5	5.4	1.1	2.5	4.9	
Δt_{PLH}	A thru H	Y		0.9	2	4.6	1	2	4.2	ns/pF
Δt_{PHL}				0.2	0.6	1.6	0.3	0.6	1.4	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
Δt_{PLH} ≡ change in t_{PLH} with load capacitance
Δt_{PHL} ≡ change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to Section 7.

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

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TEXAS INSTRUMENTS MILITARY-QUALIFIED STANDARD CELL PRODUCTS

The SystemCell™ product family offered by Texas Instruments has been designed to operate over the full military temperature range of −55°C to +125°C. All cells have been characterized for this extended temperature range performance and the military TI software library contains this information, allowing for engineering workstation simulation at both temperature extremes. For military and other high-reliability applications, these standard cells are manufactured in compliance with the requirements of JEDEC Publication 111 (JEDEC's rewrite of Method 5010 of MIL-STD-883). When required, full qualification processing is available in accordance with the standards set forth in MIL-STD-883.

The extensive Texas Instruments military semiconductor experience and resources are utilized to supply high-reliability military-qualified standard cell devices. All wafers are processed in facilities that have DESC-certified product flows. Prototypes are available in JEDEC-Standard ceramic packages and may be supplied after testing over the full military temperature range. When production devices are required, TI offers complete capabilities to fabricate, assemble, and test standard cell devices within the continental United States, allowing for compliance with complete-domestic program requirements. TI's offshore production facilities are also available to provide cost-effective military-processed devices.

MILITARY HIGH-RELIABILITY STANDARD CELL INTEGRATED CIRCUITS

The Texas Instruments military standard cell program offers several production options designed to meet system cost, reliability, leadtime, and contract requirements. The following are the key features of the options available for MIL-M-38510 and MIL-STD-883 Class B applications and can be produced either on- or offshore.

MIL-STD-883, Level B Screening

- Produced under MIL-STD-883 guidelines with all chips manufactured in facilities with DESC-certified product flows
- All production devices assembled and tested in a certified facility
- Fully tested as per MIL-STD-883 Method 5004/5005
- Electrical specification limits to be jointly agreed upon by the customer and TI
- Each lot shipment includes a Certificate of Conformance and Group A summary report

883/JEDEC Custom/Semicustom Screening

- Produced under MIL-STD-883 guidelines with all chips manufactured in facilities with DESC-certified product flows
- All production devices assembled and tested in a certified facility
- Fully tested as per MIL-STD-883 Method 5010 or JEDEC Publication 111
- Electrical specification limits to be jointly agreed upon by the customer and TI
- Each lot shipment includes a Certificate of Conformance and Group A summary report

MILITARY SCREENING AND LOT CONFORMANCE—CLASS B

SCREEN	METHOD	REQUIREMENT	
		METHOD 5004/5005	METHOD 5010 or JEDEC 111
Internal Visual (Precap)	2010, Note 1	100%	100%
Backside Symbol	Diffusion lot identified by code year and week of seal	100%	100%
Stabilization Bake	1008, 24 Hr Min, 150°C Max, Condition C	100%	100%
Temperature Cycle	1010, Condition C, Note 1	100%	100%
Constant Acceleration	2001, Y1 Only, Condition E, Note 2	100%	100%
Overvoltage Test	As per device specification at manufacturer's option, may be performed at Probe, Note 1	100%	100%
Pre-Burn-In Test	As per device specification, 25°C	100%	100%
Burn-In	1015, 160 Hr at 125°C (Min), Condition A, Note 5	100%	100%
Post-Burn-In Test	As per device specification, 25°C, DC	100%	100%
Final Electrical Test	As per device specification, −55°C, 125°C, and 25°C switching	100%	100%
Seal (A) Fine (B) Gross	 1014, Note 2 Condition B Limit = 5×10^{-8} Condition C	100%	100%
Quality Conformance Inspection Group A (Note 4)	5005, Class B	LTPD	(Note 6)
(A) Static			
(1) 25°C	(Subgroup 1)	2	5
(2) Temp	(Subgroups 2 and 3)	3	7
(B) Switching 25°C	(Subgroup 9)	2	5
(C) Functional 25°C	(Subgroup 7)	2	5
Groups B, C, D, and E	(Note 3)	Customer Option	Customer Option (Note 7)
External Visual Inspection	2009	100%	100%

NOTES:
1. Overvoltage test conditions, limits, and application will be identified by Texas Instruments upon completion of design characterization and will apply when the alternate screening procedure of Method 5004, Paragraph 3.3, is performed.
2. For device packages with 84 pins or less. For larger packages, test condition may require modification.
3. Available options depend on package type and size. Details of Groups B, C, D, and E testing and sampling plan to be negotiated.
4. If lot size is too small to meet LTPD requirements, 100% testing is acceptable.
5. T_A may need to be reduced to prevent maximum junction temperature from being exceeded.
6. Group A may be performed on QA in-line monitor program.
7. Extensive use of process control and test circuits for reduced cost.

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Explanation of Logic Symbols

F. A. Mann

Contents

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Telephone (214) 995-2659

IEEE Standards may be purchased from:

Institute of Electrical and Electronics Engineers, Inc.
IEEE Standards Office
345 East 47th Street
New York, N.Y. 10017

International Electrotechnical Commission (IEC) publications may be purchased from:

American National Standards Institute, Inc.
1430 Broadway
New York, N.Y. 10018

List of Tables

List of Illustrations

1.0 INTRODUCTION

The International Electrotechnical Commission (IEC) has been developing a very powerful symbolic language that can show the relationship of each input of a digital logic circuit to each output without showing explicitly the internal logic. At the heart of the system is dependency notation, which will be explained in Section 4.

The system was introduced in the USA in a rudimentary form in IEEE/ANSI Standard Y32.14-1973. Lacking at that time a complete development of dependency notation, it offered little more than a substitution of rectangular shapes for the familiar distinctive shapes for representing the basic functions of AND, OR, negation, etc. This is no longer the case.

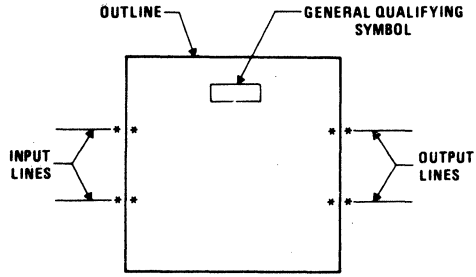
Internationally, Working Group 2 of IEC Technical Committee TC-3 has prepared a new document (Publication 617-12) that consolidates the original work started in the mid 1960's and published in 1972 (Publication 117-15) and the amendments and supplements that have followed. Similarly for the USA, IEEE Committee SCC 11.9 has revised the publication IEEE Std 91/ANSI Y32.14. Now numbered simply IEEE Std 91-1984, the IEEE standard contains all of the IEC work that has been approved, and also a small amount of material still under international consideration. Texas Instruments is participating in the work of both organizations and this document introduces new logic symbols in accordance with the new standards. When changes are made as the standards develop, future editions will take those changes into account.

The following explanation of the new symbolic language is necessarily brief and greatly condensed from what the standards publications now contain. This is not intended to be sufficient for those people who will be developing symbols for new devices. It is primarily intended to make possible the understanding of the symbols used in various data books and the comparison of the symbols with logic diagrams, functional block diagrams, and/or function tables to further help that understanding.

2.0 SYMBOL COMPOSITION

A symbol comprises an outline or a combination of outlines together with one or more qualifying symbols. The shape of the symbol is not significant. As shown in Figure 1, general qualifying symbols are used to tell exactly what logical operation is performed by the elements. Table I shows general qualifying symbols defined in the new standards. Input lines are placed on the left and output lines are placed on the right. When an exception is made to that convention, the direction of signal flow is indicated by an arrow as shown in Figure 11.

All outputs of a single, unsubdivided element always have identical internal logic states determined by the function of the element except when otherwise indicated by an associated qualifying symbol or label inside the element.



*Possible positions for qualifying symbols relating to inputs and outputs

Figure 1. Symbol Composition

The outlines of elements may be abutted or embedded in which case the following conventions apply. There is no logic connection between the elements when the line common to their outlines is in the direction of signal flow. There is at least one logic connection between the elements when the line common to their outlines is perpendicular to the direction of signal flow. The number of logic connections between elements will be clarified by the use of qualifying symbols and this is discussed further under that topic. If no indications are shown on either side of the common line, it is assumed there is only one connection.

When a circuit has one or more inputs that are common to more than one element of the circuit, the common-control block may be used. This is the only distinctively shaped outline used in the IEC system. Figure 2 shows that unless otherwise qualified by dependency notation, an input to the common-control block is an input to each of the elements below the common-control block.

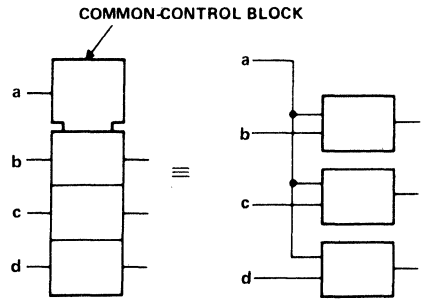


Figure 2. Common-Control Block

A common output depending on all elements of the array can be shown as the output of a common-output element. Its distinctive visual feature is the double line at its top. In addition the common-output element may have other inputs as shown in Figure 3. The function of the common-output element must be shown by use of a general qualifying symbol.

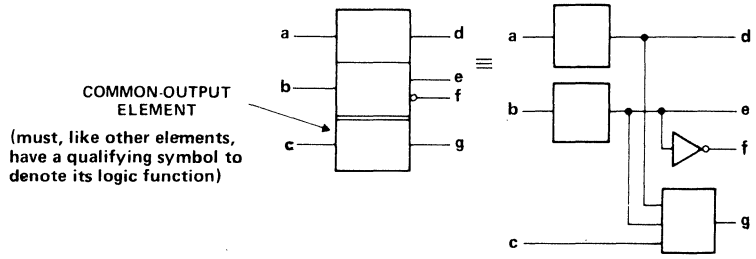


Figure 3. Common-Output Element

3.0 QUALIFYING SYMBOLS

3.1 General Qualifying Symbols

Table I shows general qualifying symbols defined by IEEE Standard 91. These characters are placed near the top center or the geometric center of a symbol or symbol element to define the basic function of the device represented by the symbol or of the element.

3.2 General Qualifying Symbols for Inputs and Outputs

Qualifying symbols for inputs and outputs are shown in Table II and many will be familiar to most users, with the possible exception of the logic polarity and analog signal indicators. The older logic negation indicator means that the external 0 state produces the internal 1 state. The internal 1 state means the active state. Logic negation may be used in pure logic diagrams; in order to tie the external 1 and 0 logic states to the levels H (high) and L (low), a statement of whether positive logic (1 = H, 0 = L) or negative logic (1 = L, 0 = H) is being used, is required or must be assumed. Logic polarity indicators eliminate the need for calling out the logic convention and are used in various data books in the symbology for actual devices. The presence of the triangular polarity indicator indicates that the L logic level will produce the internal 1 state (the active state) or that, in the case of an output, the internal 1 state will produce the external L level. Note how the active direction of transition for a dynamic input is indicated in positive logic, negative logic, and with polarity indication.

The internal connections between logic elements abutted together in a symbol may be indicated by the symbols shown in Table II. Each logic connection may be shown by the presence of qualifying symbols at one or both sides of the common line and if confusion can arise about the number of connections, use can be made of one of the internal connection symbols.

Table I. General Qualifying Symbols

SYMBOL	DESCRIPTION	CMOS EXAMPLE	TTL EXAMPLE
&	AND gate or function.	'HC00	SN7400
≥1	OR gate or function. The symbol was chosen to indicate that at least one active input is needed to activate the output.	'HC02	SN7402
=1	Exclusive OR. One and only one input must be active to activate the output.	'HC86	SN7486
=	Logic identity. All inputs must stand at the same state.	'HC86	SN74180
2k	An even number of inputs must be active.	'HC280	SN74180
2k + 1	An odd number of inputs must be active.	'HC86	SN74ALS86
1	The one input must be active.	'HC04	SN7404
▷ or ◁	A buffer or element with more than usual output capability (symbol is oriented in the direction of signal flow).	'HC240	SN74S436
⎍	Schmitt trigger; element with hysteresis.	'HC132	SN74LS18
X/Y	Coder, code converter (DEC/BCD, BIN/OCT, BIN/7-SEG, etc.).	'HC42	SN74LS347
MUX	Multiplexer/data selector.	'HC151	SN74150
DMUX or DX	Demultiplexer.	'HC138	SN74138
Σ	Adder.	'HC283	SN74LS385
P−Q	Subtracter.	*	SN74LS385
CPG	Look-ahead carry generator.	'HC182	SN74182
π	Multiplier.	*	SN74LS384
COMP	Magnitude comparator.	'HC85	SN74LS682
ALU	Arithmetic logic unit.	'HC181	SN74LS381
⎍	Retriggerable monostable.	'HC123	SN74LS422
1⎍	Nonretriggerable monostable (one-shot).	'HC221	SN74121
G ⎍	Astable element. Showing waveform is optional.	*	SN74LS320
!G ⎍	Synchronously starting astable.	*	SN74LS624
G! ⎍	Astable element that stops with a completed pulse.	*	*
SRGm	Shift register. m = number of bits.	'HC164	SN74LS595
CTRm	Counter. m = number of bits; cycle length = 2^m.	'HC590	SN54LS590
CTR DIVm	Counter with cycle length = m.	'HC160	SN74LS668
RCTRm	Asynchronous (ripple-carry) counter; cycle length = 2^m.	'HC4020	*
ROM	Read-only memory.	*	SN74187
RAM	Random-access read/write memory.	'HC189	SN74170
FIFO	First-in, first-out memory.	*	SN74LS22
I=0	Element powers up cleared to 0 state.	*	SN74AS877
I=1	Element powers up set to 1 state.	'HC7022	SN74AS877
Φ	Highly complex function; "gray box" symbol with limited detail shown under special rules.	*	SN74LS608

*Not all of the general qualifying symbols have been used in TI's CMOS and TTL data books, but they are included here for the sake of completeness.

Table II. Qualifying Symbols for Inputs and Outputs

Logic negation at input. External 0 produces internal 1.

Logic negation at output. Internal 1 produces external 0.

Active-low input. Equivalent to  in positive logic.

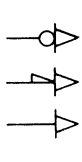
Active-low output. Equivalent to  in positive logic.

Active-low input in the case of right-to-left signal flow.

Active-low output in the case of right-to-left signal flow.

Signal flow from right to left. If not otherwise indicated, signal flow is from left to right.

Bidirectional signal flow.



Nonlogic connection. A label inside the symbol will usually define the nature of this pin.

Input for analog signals (on a digital symbol) (see Figure 14).

Input for digital signals (on an analog symbol) (see Figure 14).

Internal connection. 1 state on left produces 1 state on right.

Negated internal connection. 1 state on left produces 0 state on right.

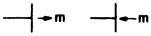
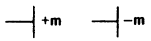
Dynamic internal connection. Transition from 0 to 1 on left produces transitory 1 state on right.

Internal input (virtual input). It always stands at its internal 1 state unless affected by an overriding dependency relationship.

Internal output (virtual output). Its effect on an internal input to which it is connected is indicated by dependency notation.

The internal (virtual) input is an input originating somewhere else in the circuit and is not connected directly to a terminal. The internal (virtual) output is likewise not connected directly to a terminal. The application of internal inputs and outputs requires an understanding of dependency notation, which is explained in Section 4.

Table III. Symbols Inside the Outline

	Postponed output (of a pulse-triggered flip-flop). The output changes when input initiating change (e.g., a C input) returns to its initial external state or level. See § 5.
	Bi-threshold input (input with hysteresis)
	N-P-N open-collector or similar output that can supply a relatively low-impedance L level when not turned off. Requires external pull-up. Capable of positive-logic wired-AND connection.
	Passive-pull-up output is similar to N-P-N open-collector output but is supplemented with a built-in passive pull-up.
	N-P-N open-emitter or similar output that can supply a relatively low-impedance H level when not turned off. Requires external pull-down. Capable of positive-logic wired-OR connection.
	Passive-pull-down output is similar to N-P-N open-emitter output but is supplemented with a built-in passive pull-down.
	3-state output.
	Output with more than usual output capability (symbol is oriented in the direction of signal flow).
	Enable input When at its internal 1-state, all outputs are enabled. When at its internal 0-state, open-collector and open-emitter outputs are off, three-state outputs are in the high-impedance state, and all other outputs (i.e., totem-poles) are at the internal 0-state.
J, K, R, S	Usual meanings associated with flip-flops (e.g., R = reset to 0, S = set to 1).
	Toggle input causes internal state of output to change to its complement.
	Data input to a storage element equivalent to: 
	Shift right (left) inputs, m = 1, 2, 3, etc. If m = 1, it is usually not shown.
	Counting up (down) inputs, m = 1, 2, 3, etc. If m = 1, it is usually not shown.
	Binary grouping. m is highest power of 2.
	The contents-setting input, when active, causes the content of a register to take on the indicated value.
	The content output is active if the content of the register is as indicated.
	Input line grouping . . . indicates two or more terminals used to implement a single logic input. e.g., The paired expander inputs of SN7450. 
	Fixed-state output always stands at its internal 1 state. For example, see SN74185.

In an array of elements, if the same general qualifying symbol and the same qualifying symbols associated with inputs and outputs would appear inside each of the elements of the array, then these qualifying symbols are usually shown only in the first element. This is done to reduce clutter and to save time in recognition. Similarly, large identical elements that are subdivided into smaller elements may each be represented by an unsubdivided outline. The SN54HC242 or SN54LS440 symbol illustrates this principle.

3.3 Symbols Inside the Outline

Table III shows some symbols used inside the outline. Note particularly that open-collector (open-drain), open-emitter (open-source), and 3-state outputs have distinctive symbols. An EN input affects all the external outputs of the element in which it is placed, plus the external outputs of any elements shown to be influenced by that element. It has no effect on inputs. When an enable input affects only certain outputs, affects outputs located outside the indicated influence of the element in which the enable input is placed, and/or affects one or more inputs, a form of dependency notation will indicate this (see 4.10). The effects of the EN input on the various types of outputs are shown.

It is particularly important to note that a D input is always the data input of a storage element. At its internal 1 state, the D input sets the storage element to its 1 state, and at its internal 0 state it resets the storage element to its 0 state.

The binary grouping symbol will be explained more fully in Section 8. Binary-weighted inputs are arranged in order and the binary weights of the least-significant and the most-significant lines are indicated by numbers. In this document weights of input and output lines will be represented by powers of two usually only when the binary grouping symbol is used, otherwise decimal numbers will be used. The grouped inputs generate an internal number on which a mathematical function can be performed or that can be an identifying number for dependency notation (Figure 28). A frequent use is in addresses for memories.

Reversed in direction, the binary grouping symbol can be used with outputs. The concept is analogous to that for the inputs and the weighted outputs will indicate the internal number assumed to be developed within the circuit.

Other symbols are used inside the outlines in accordance with the IEC/IEEE standards but are not shown here. Generally these are associated with arithmetic operations and are self-explanatory.

When nonstandardized information is shown inside an outline, it is usually enclosed in square brackets [like these]. The square brackets are omitted when associated with a nonlogic input, which is indicated by an X superimposed on the connection line outside the symbol.

4.0 DEPENDENCY NOTATION

4.1 General Explanation

Dependency notation is the powerful tool that sets the IEC symbols apart from previous systems and makes compact, meaningful, symbols possible. It provides the means of denoting the relationship between inputs, outputs, or inputs and outputs without actually showing all the

elements and interconnections involved. The information provided by dependency notation supplements that provided by the qualifying symbols for an element's function.

In the convention for the dependency notation, use will be made of the terms "affecting" and "affected." In cases where it is not evident which inputs must be considered as being the affecting or the affected ones (e.g., if they stand in an AND relationship), the choice may be made in any convenient way.

So far, eleven types of dependency have been defined and all of these are used in various TI data books. X dependency is used mainly with CMOS circuits. They are listed below in the order in which they are presented and are summarized in Table IV following 4.12.

Section	Dependency Type or Other Subject
4.2	G, AND
4.3	General Rules for Dependency Notation
4.4	V, OR
4.5	N, Negate (Exclusive-OR)
4.6	Z, Interconnection
4.7	X, Transmission
4.8	C, Control
4.9	S, Set and R, Reset
4.10	EN, Enable
4.11	M, Mode
4.12	A, Address

4.2 G (AND) Dependency

A common relationship between two signals is to have them ANDed together. This has traditionally been shown by explicitly drawing an AND gate with the signals connected to the inputs of the gate. The 1972 IEC publication and the 1973 IEEE/ANSI standard showed several ways to show this AND relationship using dependency notation. While ten other forms of dependency have since been defined, the ways to invoke AND dependency are now reduced to one.

In Figure 4 input **b** is ANDed with input **a** and the complement of **b** is ANDed with **c**. The letter G has been chosen to indicate AND relationships and is placed at input **b**, inside the symbol. A number considered appropriate by the symbol designer (1 has been used here) is placed after the letter G and also at each affected input. Note the bar over the 1 at input **c**.

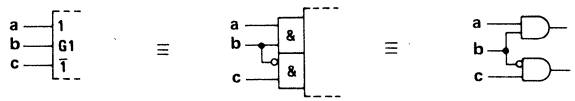


Figure 4. G Dependency Between Inputs

In Figure 5, output **b** affects input **a** with an AND relationship. The lower example shows that it is the internal logic state of **b**, unaffected by the negation sign, that is ANDed. Figure 6 shows input **a** to be ANDed with a dynamic input **b**.

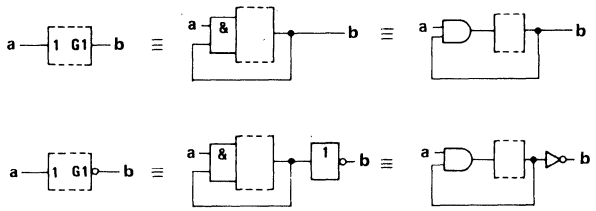


Figure 5. G Dependency Between Outputs and Inputs

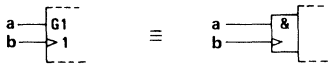


Figure 6. G Dependency with a Dynamic Input

The rules for G dependency can be summarized thus:

> When a G*m* input or output (*m* is a number) stands at its internal 1 state, all inputs and outputs affected by G*m* stand at their normally defined internal logic states. When the G*m* input or output stands at its 0 state, all inputs and outputs affected by G*m* stand at their internal 0 states.

4.3 Conventions for the Application of Dependency Notation in General

The rules for applying dependency relationships in general follow the same pattern as was illustrated for G dependency.

Application of dependency notation is accomplished by:

1) labeling the input (or output) *affecting* other inputs or outputs with the letter symbol indicating the relationship involved (e.g., G for AND) followed by an identifying number, appropriately chosen, and
2) labeling each input or output *affected* by that affecting input (or output) with that same number.

If it is the complement of the internal logic state of the affecting input or output that does the affecting, then a bar is placed over the identifying numbers at the affected inputs or outputs (Figure 4).

If two affecting inputs or outputs have the same letter and the same identifying number, they stand in an OR relationship to each other (Figure 7).

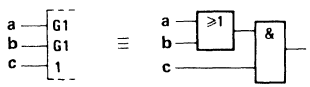


Figure 7. ORed Affecting Inputs

If the affected input or output requires a label to denote its function (e.g., "D"), this label will be *prefixed* by the identifying number of the affecting input (Figure 15).

If an input or output is affected by more than one affecting input, the identifying numbers of each of the affecting inputs will appear in the label of the affected one, separated by commas. The normal reading order of these numbers is the same as the sequence of the affecting relationships (Figure 15).

If the labels denoting the functions of affected inputs or outputs must be numbers (e.g., outputs of a coder), the identifying numbers to be associated with both affecting inputs and affected inputs or outputs will be replaced by another character selected to avoid ambiguity, e.g., Greek letters (Figure 8).

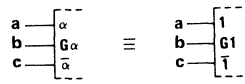


Figure 8. Substitution for Numbers

4.4 V (OR) Dependency

The symbol denoting OR dependency is the letter V (Figure 9).

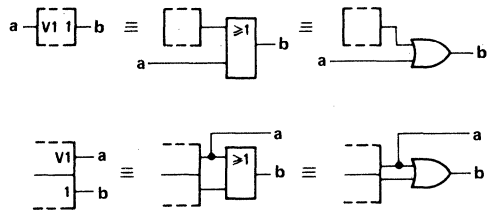
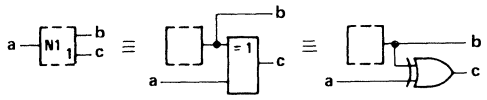


Figure 9. V (OR) Dependency

When a V*m* input or output stands at its internal 1 state, all inputs and outputs affected by V*m* stand at their internal 1 states. When the V*m* input or output stands at its internal 0 state, all inputs and outputs affected by V*m* stand at their normally defined internal logic states.

4.5 N (Negate) (Exclusive-OR) Dependency

The symbol denoting negate dependency is the letter N (Figure 10). Each input or output affected by an N*m* input or output stands in an Exclusive-OR relationship with the N*m* input or output.



If a = 0, then c = b
If a = 1, then c = $\overline{b}$

Figure 10. N (Negate) (Exclusive-OR) Dependency

When an N*m* input or output stands at its internal 1 state, the internal logic state of each input and each output affected by N*m* is the complement of what it would otherwise be. When an N*m* input or output stands at its internal 0 state, all inputs and outputs affected by N*m* stand at their normally defined internal logic states.

4.6 Z (Interconnection) Dependency

The symbol denoting interconnection dependency is the letter Z.

Interconnection dependency is used to indicate the existence of internal logic connections between inputs, outputs, internal inputs, and/or internal outputs.

The internal logic state of an input or output affected by a Z*m* input or output will be the same as the internal logic state of the Z*m* input or output, unless modified by additional dependency notation (Figure 11).

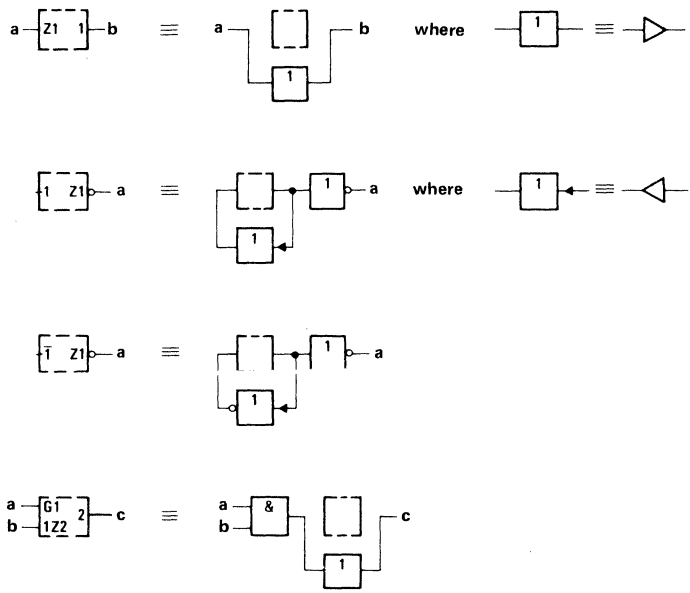
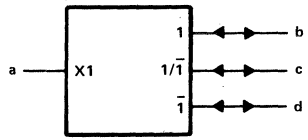


Figure 11. Z (Interconnection) Dependency

4.7 X (Transmission) Dependency

The symbol denoting transmission dependency is the letter X.

Transmission dependency is used to indicate controlled bidirectional connections between affected input/output ports (Figure 12).



If a = 1, there is a bidirectional connection between b and c.

If a = 0, there is a bidirectional connection between c and d.

Figure 12. X (Transmission) Dependency

When an X*m* input or output stands at its internal 1 state, all input-output ports affected by this X*m* input or output are bidirectionally connected together and stand at the same internal logic state or analog signal level. When an X*m* input or output stands at its internal 0 state, the connection associated with this set of dependency notation does not exist.

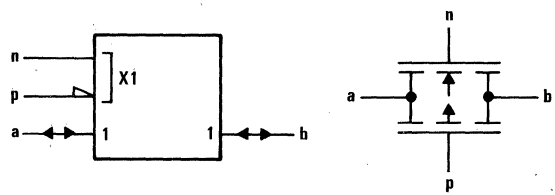


Figure 13. CMOS Transmission Gate Symbol and Schematic

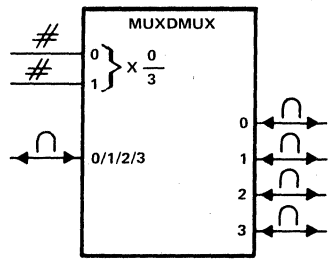


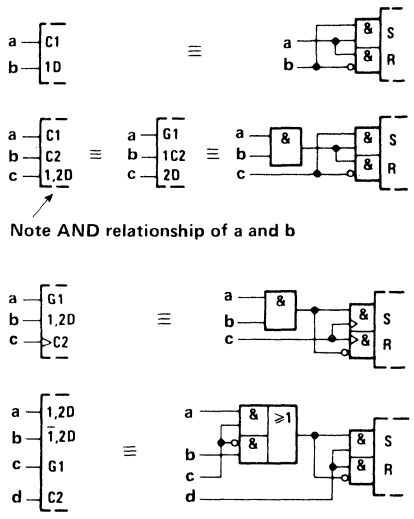
Figure 14. Analog Data Selector (Multiplexer/Demultiplexer)

Although the transmission paths represented by X dependency are inherently bidirectional, use is not always made of this property. This is analogous to a piece of wire, which may be constrained to carry current in only one direction. If this is the case in a particular application, then the directional arrows shown in Figures 12, 13, and 14 are omitted.

4.8 C (Control) Dependency

The symbol denoting control dependency is the letter C.

Control inputs are usually used to enable or disable the data (D, J, K, R, or S) inputs of storage elements. They may take on their internal 1 states (be active) either statically or dynamically. In the latter case the dynamic input symbol is used as shown in the third example of Figure 15.



Input c selects which of a or b is stored when d goes low.

Figure 15. C (Control) Dependency

When a C*m* input or output stands at its internal 1 state, the inputs affected by C*m* have their normally defined effect on the function of the element, i.e., these inputs are enabled. When a C*m* input or output stands at its internal 0 state, the inputs affected by C*m* are disabled and have no effect on the function of the element.

4.9 S (Set) and R (Reset) Dependencies

The symbol denoting set dependency is the letter S. The symbol denoting reset dependency is the letter R.

Set and reset dependencies are used if it is necessary to specify the effect of the combination R = S = 1 on a bistable element. Case 1 in Figure 16 does not use S or R dependency.

When an S*m* input is at its internal 1 state, outputs affected by the S*m* input will react, regardless of the state of an R input, as they normally would react to the combination S = 1, R = 0. See cases 2, 4, and 5 in Figure 16.

When an R*m* input is at its internal 1 state, outputs affected by the R*m* input will react, regardless of the state of an S input, as they normally would react to the combination S = 0, R = 1. See cases 3, 4, and 5 in Figure 16.

When an S*m* or R*m* input is at its internal 0 state, it has no effect.

Note that the noncomplementary output patterns in cases 4 and 5 are only pseudo stable. The simultaneous return of the inputs to S = R = 0 produces an unforeseeable stable and complementary output pattern.

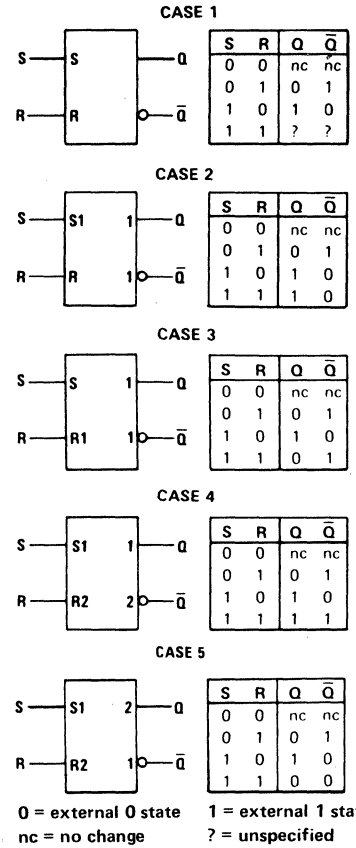


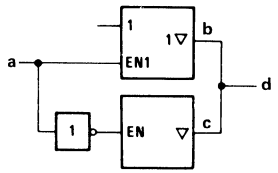
Figure 16. S (Set) and R (Reset) Dependencies

4.10 EN (Enable) Dependency

The symbol denoting enable dependency is the combination of letters EN.

An EN*m* input has the same effect on outputs as an EN input, see 3.3, but it affects only those outputs labeled with the identifying number *m*. It also affects those inputs labeled with the identifying number *m*. By contrast, an EN input affects all outputs and no inputs. The effect of an EN*m* input on an affected input is identical to that of a C*m* input (Figure 17).

When an EN*m* input stands at its internal 1 state, the inputs affected by EN*m* have their normally defined effect on the function of the element and the outputs affected by this input stand at their normally defined internal logic states, i.e., these inputs and outputs are enabled.



If a = 0, b is disabled and d = c
If a = 1, c is disabled and d = b

Figure 17. EN (Enable) Dependency

When an EN*m* input stands at its internal 0 state, the inputs affected by EN*m* are disabled and have no effect on the function of the element, and the outputs affected by EN*m* are also disabled. Open-collector outputs are turned off, three-state outputs stand at their normally defined internal logic states by externally exhibit high impedance, and all other outputs (e.g., totem-pole outputs) stand at their internal 0 states.

4.11 M (MODE) Dependency

The symbol denoting mode dependency is the letter M.

Mode dependency is used to indicate that the effects of particular inputs and outputs of an element depend on the mode in which the element is operating.

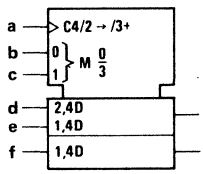
If an input or output has the same effect in different modes of operation, the identifying numbers of the relevant affecting M*m* inputs will appear in the label of that affected input or output between parentheses and separated by solidi (Figure 22).

4.11.1 M Dependency Affecting Inputs

M dependency affects inputs the same as C dependency. When an M*m* input or M*m* output stands at its internal 1 state, the inputs affected by this M*m* input or M*m* output have their normally defined effect on the function of the element, i.e., the inputs are enabled.

When an M*m* input or M*m* output stands at its internal 0 state, the inputs affected by this M*m* input or M*m* output have no effect on the function of the element. When an affected input has several sets of labels separated by solidi (e.g., C4/2→/3+), any set in which the identifying number of the M*m* input or M*m* output appears has no effect and is to be ignored. This represents disabling of some of the functions of a multifunction input.

The circuit in Figure 18 has two inputs, **b** and **c**, that control which one of four modes (0, 1, 2, or 3) will exist at any time. Inputs **d**, **e**, and **f** are D inputs subject to dynamic control (clocking) by the **a** input. The numbers 1 and 2 are in the series chosen to indicate the modes so inputs **e** and **f** are only enabled in mode 1 (for parallel loading) and input **d** is only enabled in mode 2 (for serial loading). Note that input **a** has three functions. It is the clock for entering data. In mode 2, it causes right shifting of data, which means a shift away from the control block. In mode 3, it causes the contents of the register to be incremented by one count.



Note that all operations are synchronous.

In MODE 0 (b = 0, c = 0), the outputs remain at their existing states as none of the inputs has an effect.

In MODE 1 (b = 1, c = 0), parallel loading takes place thru inputs e and f.

In MODE 2 (b = 0, c = 1), shifting down and serial loading thru input d take place.

In MODE 3 (b = c = 1), counting up by increment of 1 per clock pulse takes place.

Figure 18. M (Mode) Dependency Affecting Inputs

4.11.2 M Dependency Affecting Outputs

When an M*m* input or M*m* output stands at its internal 1 state, the affected outputs stand at their normally defined internal logic states, i.e., the outputs are enabled.

When an M*m* input or M*m* output stands at its internal 0 state, at each affected output any set of labels containing the identifying number of that M*m* input or M*m* output has no effect and is to be ignored. When an output has several different sets of labels separated by solidi (e.g., 2,4/3,5), only those sets in which the identifying number of this M*m* input or M*m* output appears are to be ignored.

Figure 19 shows a symbol for a device whose output can behave as either a 3-state output or an open-collector output depending on the signal applied to input **a**. Mode 1 exists when input **a** stands at its internal 1 state and, in that case, the three-state symbol applies and the open-element symbol has no effect. When **a** = 0, mode 1 does not exist so the three-state symbol has no effect and the open-element symbol applies.

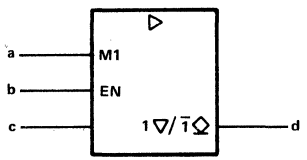


Figure 19. Type of Output Determined by Mode

In Figure 20, if input **a** stands at its internal 1 state establishing mode 1, output **b** will stand at its internal 1 state only when the content of the register equals 9. Since output **b** is located in the common-control block with no defined function outside of mode 1, the state of this output outside of mode 1 is not defined by the symbol.

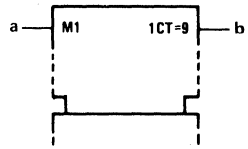


Figure 20. An Output of the Common-Control Block

In Figure 21, if input **a** stands at its internal 1 state establishing mode 1, output **b** will stand at its internal 1 state only when the content of the register equals 15. If input **a** stands at its internal 0 state, output **b** will stand at its internal 1 state only when the content of the register equals 0.

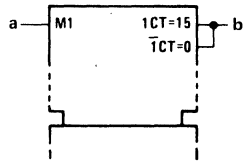


Figure 21. Determining an Output's Function

In Figure 22 inputs **a** and **b** are binary weighted to generate the numbers 0, 1, 2, or 3. This determines which one of the four modes exists.

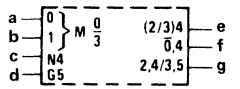


Figure 22. Dependent Relationships Affected by Mode

At output **e** the label set causing negation (if **c** = 1) is effective only in modes 2 and 3. In modes 0 and 1 this output stands at its normally defined state as if it had no labels. At output **f** the label set has effect when the mode is not 0 so output **e** is negated (if **c** = 1) in modes 1, 2, and 3. In mode 0 the label set has no effect so the output stands at its normally defined state. In this example $\overline{0}$,4 is equivalent to (1/2/3)4. At output **g** there are two label sets. The first set, causing negation (if **c** = 1), is effective only in mode 2. The second set, subjecting **g** to AND dependency on **d**, has effect only in mode 3.

Note that in mode 0 none of the dependency relationships has any effect on the outputs, so **e**, **f**, and **g** will all stand at the same state.

4.12 A (Address) Dependency

The symbol denoting address dependency is the letter A.

Address dependency provides a clear representation of those elements, particularly memories, that use address control inputs to select specified sections of a multildimensional array. Such a section of a memory array is usually called a word. The purpose of address dependency is to allow a symbolic presentation of the entire array. An input of the array shown at a particular

element of this general section is common to the corresponding elements of all selected sections of the array. An output of the array shown at a particular element of this general section is the result of the OR function of the outputs of the corresponding elements of selected sections.

Inputs that are not affected by any affecting address input have their normally defined effect on all sections of the array, whereas inputs affected by an address input have their normally defined effect only on the section selected by that address input.

An affecting address input is labeled with the letter A followed by an identifying number that corresponds with the address of the particular section of the array selected by this input. Within the general section presented by the symbol, inputs and outputs affected by an A*m* input are labeled with the letter A, which stands for the identifying numbers, i.e., the addresses, of the particular sections.

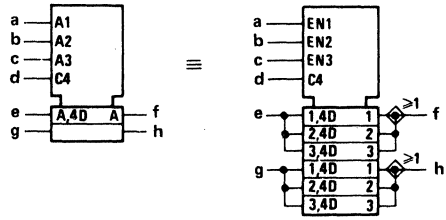


Figure 23. A (Address) Dependency

Figure 23 shows a 3-word by 2-bit memory having a separate address line for each word and uses EN dependency to explain the operation. To select word 1, input **a** is taken to its 1 state, which establishes mode 1. Data can now be clocked into the inputs marked "1,4D." Unless words 2 and 3 are also selected, data cannot be clocked in at the inputs marked "2,4D" and "3,4D." The outputs will be the OR functions of the selected outputs, i.e., only those enabled by the active EN functions.

The identifying numbers of affecting address inputs correspond with the addresses of the sections selected by these inputs. They need not necessarily differ from those of other affecting dependency-inputs (e.g., G, V, N, . . .), because in the general section presented by the symbol they are replaced by the letter A.

If there are several sets of affecting A*m* inputs for the purpose of independent and possibly simultaneous access to sections of the array, then the letter A is modified to 1A, 2A, ... Since they have access to the same sections of the array, these sets of A inputs may have the same identifying numbers. The symbols for 'HC170 or SN74LS170 make use of this.

Figure 24 is another illustration of the concept.

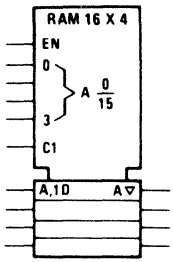


Figure 24. Array of 16 Sections of Four Transparent Latches with 3-State Outputs Comprising a 16-Word × 4-Bit Random-Access Memory

Table IV. Summary of Dependency Notation

TYPE OF DEPENDENCY	LETTER SYMBOL*	AFFECTING INPUT AT ITS 1-STATE	AFFECTING INPUT AT ITS 0-STATE
Address	A	Permits action (address selected)	Prevents action (address not selected)
Control	C	Permits action	Prevents action
Enable	EN	Permits action	Prevents action of inputs ◇ outputs off ▽ outputs at external high impedance, no change in internal logic state Other outputs at internal 0 state
AND	G	Permits action	Imposes 0 state
Mode	M	Permits action (mode selected)	Prevents action (mode not selected)
Negate (Ex-OR)	N	Complements state	No effect
Reset	R	Affected output reacts as it would to S = 0, R = 1	No effect
Set	S	Affected output reacts as it would to S = 1, R = 0	No effect
OR	V	Imposes 1 state	Permits action
Transmission	X	Bidirectional connection exists	Bidirectional connection does not exist
Interconnection	Z	Imposes 1 state	Imposes 0 state

* These letter symbols appear at the AFFECTING input (or output) and are followed by a number. Each input (or output) AFFECTED by that input is labeled with that same number. When the labels EN, R, and S appear at inputs without the following numbers, the descriptions above do not apply. The action of these inputs is described under "Symbols Inside the Outline," see 3.3.

5.0 BISTABLE ELEMENTS

The dynamic input symbol, the postponed output symbol, and dependency notation provide the tools to differentiate four main types of bistable elements and make synchronous and asynchronous inputs easily recognizable (Figure 25). The first column shows the essential distinguishing features; the other columns show examples.

Transparent latches have a level-operated control input. The D input is active as long as the C input is at its internal 1 state. The outputs respond immediately. Edge-triggered elements accept data from D, J, K, R, or S inputs on the active transition of C. Pulse-triggered elements

require the setup of data before the start of the control pulse; the C input is considered static since the data must be maintained as long as C is at its 1 state. The output is postponed until C returns to its 0 state. The data-lock-out element is similar to the pulse-triggered version except that the C input is considered dynamic in that shortly after C goes through its active transition, the data inputs are disabled and data does not have to be held. However, the output is still postponed until the C input returns to its initial external level.

Notice that synchronous inputs can be readily recognized by their dependency labels (1D, 1J, 1K, 1S, 1R) compared to the asynchronous inputs (S, R), which are not dependent on the C inputs.

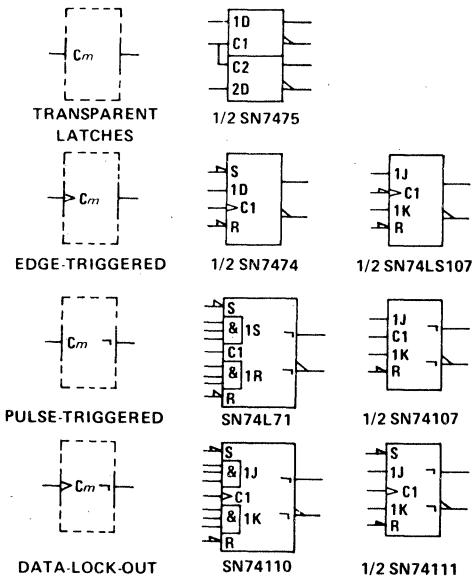


Figure 25. Four Types of Bistable Circuits

6.0 CODERS

The general symbol for a coder or code converter is shown in Figure 26. X and Y may be replaced by appropriate indications of the code used to represent the information at the inputs and at the outputs, respectively.

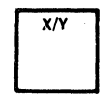


Figure 26. Coder General Symbol

Indication of code conversion is based on the following rule:

Depending on the input code, the internal logic states of the inputs determine an internal value. This value is reproduced by the internal logic states of the outputs, depending on the output code.

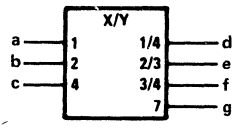
The indication of the relationships between the internal logic states of the inputs and the internal value is accomplished by:

1) labeling the inputs with numbers. In this case the internal value equals the sum of the weights associated with those inputs that stand at their internal 1-state, or by
2) replacing X by an appropriate indication of the input code and labeling the inputs with characters that refer to this code.

The relationships between the internal value and the internal logic states of the outputs are indicated by:

1) labeling each output with a list of numbers representing those internal values that lead to the internal 1-state of that output. These numbers shall be separated by solidi as in Figure 27. This labeling may also be applied when Y is replaced by a letter denoting a type of dependency (see Section 7). If a continuous range of internal values produces the internal 1 state of an output, this can be indicated by two numbers that are inclusively the beginning and the end of the range, with these two numbers separated by three dots (e.g., 4 . . . 9 = 4/5/6/7/8/9) or by
2) replacing Y by an appropriate indiction of the output code and labeling the outputs with characters that refer to this code as in Figure 28.

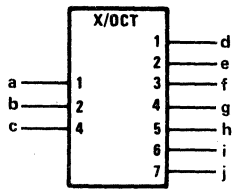
Alternatively, the general symbol may be used together with an appropriate reference to a table in which the relationship between the inputs and outputs is indicated. This is a recommended way to symbolize a PROM after it has been programmed.



TRUTH TABLE

INPUTS			OUTPUTS			
c	b	a	g	f	e	d
0	0	0	0	0	0	0
0	0	1	0	0	0	1
0	1	0	0	0	1	0
0	1	1	0	1	1	0
1	0	0	0	1	0	1
1	0	1	0	0	0	0
ı	ı	U	U	U	0	0
1	1	1	1	0	0	0

Figure 27. An X/Y Code Converter



TRUTH TABLE

INPUTS			OUTPUTS						
c	b	a	j	i	h	g	f	e	d
0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	1
0	1	0	0	0	0	0	0	1	0
0	1	1	0	0	0	0	1	0	0
1	0	0	0	0	0	1	0	0	0
1	0	1	0	0	1	0	0	0	0
1	1	0	0	1	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0

Figure 28. An X/Octal Code Converter

7.0 USE OF A CODER TO PRODUCE AFFECTING INPUTS

It often occurs that a set of affecting inputs for dependency notation is produced by decoding the signals on certain inputs to an element. In such a case use can be made of the symbol for a coder as an embedded symbol (Figure 29).

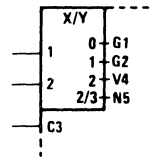


Figure 29. Producing Various Types of Dependencies

If all affecting inputs produced by a coder are of the same type as their identifying numbers shown at the outputs of the coder, Y (in the qualifying symbol X/Y) may be replaced by the letter denoting the type of dependency. The indications of the affecting inputs should then be omitted (Figure 30).

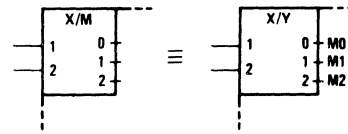


Figure 30. Producing One Type of Dependency

8.0 USE OF BINARY GROUPING TO PRODUCE AFFECTING INPUTS

If all affecting inputs produced by a coder are of the same type and have consecutive identifying numbers not necessarily corresponding with the numbers that would have been shown at the outputs of the coder, use can be made of the binary grouping symbol. *k* external lines effectively generate 2^k internal inputs. The bracket is followed by the letter denoting the type of dependency followed by m1/m2. The m1 is to be replaced by the smallest identifying number and the m2 by the largest one, as shown in Figure 31.

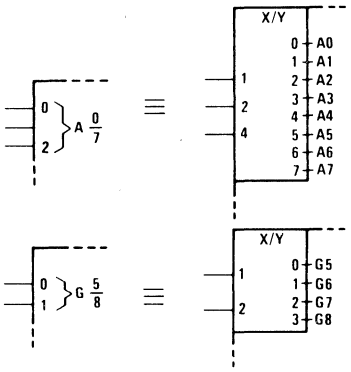


Figure 31. Use of the Binary Grouping Symbol

9.0 SEQUENCE OF INPUT LABELS

If an input having a single functional effect is affected by other inputs, the qualifying symbol (if there is any) for that functional effect is preceded by the labels corresponding to the affecting inputs. The left-to-right order of these preceding labels is the order in which the effects or modifications must be applied. The affected input has no functional effect on the element if the logic state of any one of the affecting inputs, considered separately, would cause the affected input to have no effect, regardless of the logic states of other affecting inputs.

If an input has several different functional effects or has several different sets of affecting inputs, depending on the mode of action, the input may be shown as often as required. However, there are cases in which this method of presentation is not advantageous. In those cases the input may be shown once with the different sets of labels separated by solidi (Figure 32). No meaning is attached to the order of these sets of labels. If one of the functional effects of an input is that of an unlabeled input to the element, a solidus will precede the first set of labels shown.

If all inputs of a combinational element are disabled (caused to have no effect on the function of the element), the internal logic states of the outputs of the element are not specified by the symbol. If all inputs of a sequential element are disabled, the content of this element is not changed and the outputs remain at their existing internal logic states.

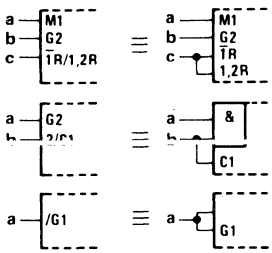


Figure 32. Input Labels

Labels may be factored using algebraic techniques (Figure 33).

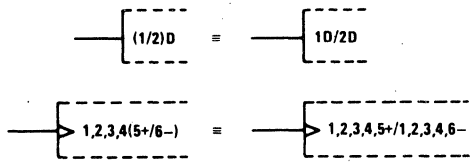


Figure 33. Factoring Input Labels

10.0 SEQUENCE OF OUTPUT LABELS

If an output has a number of different labels, regardless of whether they are identifying numbers of affecting inputs or outputs or not, these labels are shown in the following order:

1) If the postponed output symbol has to be shown, this comes first, if necessary preceded by the indications of the inputs to which it must be applied
2) Followed by the labels indicating modifications of the internal logic state of the output, such that the left-to-right order of these labels corresponds with the order in which their effects must be applied
3) Followed by the label indicating the effect of the output on inputs and other outputs of the element.

Symbols for open-circuit or 3-state outputs, where applicable, are placed just inside the outside boundary of the symbol adjacent to the output line (Figure 34).

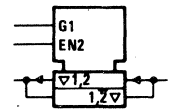


Figure 34. Placement of 3-State Symbols

If an output needs several different sets of labels that represent alternative functions (e.g., depending on the mode of action), these sets may be shown on different output lines that must be connected outside the outline. However, there are cases in which this method of presentation is not advantageous. In those cases the output may be shown once with the different sets of labels separated by solidi (Figure 35).

Two adjacent identifying numbers of affecting inputs in a set of labels that are not already separated by a nonnumeric character should be separated by a comma.

If a set of labels of an output not containing a solidus contains the identifying number of an affecting M*m* input standing at its internal 0 state, this set of labels has no effect on that output.

Labels may be factored using algebraic techniques (Figure 36).

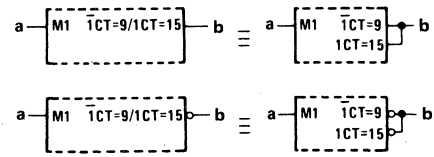


Figure 35. Output Labels

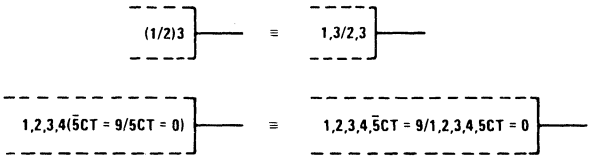


Figure 36. Factoring Output Labels

If you have questions on this Explanation of Logic Symbols, please contact:

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F.A. Mann, MS 49
P.O. Box 655012
Dallas, Texas 75265

Telephone (214) 995-2659

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IEEE Standards Office
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New York, N.Y. 10017

International Electrotechnical Commission (IEC) publications may be purchased from:

American National Standards Institute, Inc.
1430 Broadway
New York, N.Y. 10018

DESIGN CONSIDERATIONS

Logic Evaluation

To begin your standard cell IC design, you should prepare a functional description, a timing diagram, and a logic design. A complete definition of the circuit performance must be specified. Waveform diagrams or test vectors may be adequate; however, precise and detailed specifications simplify the implementation. Once you have these items, you are ready to examine the circuit and choose those portions to be included in the standard cell design.

Logic Partitioning

Logic partitioning is the act of examining a logic design and deciding which components will be in your standard cell implementation. Sometimes the choice is obvious; other times it involves compromises. Here are some factors to consider:

Complexity of the Circuit

Although a semicustom IC may contain thousands of gates, there is a practical limit to its size. If the circuit is too large, it must be partitioned into several smaller blocks. These may then be implemented as separate standard cell designs.

As part of the initial evaluation and specification of your present schematic, you must define boundaries as to what will be integrated. This step must be done whether adapting an existing logic system or designing a new one. As you evaluate your design, you may find some functions for which no standard cells exist. TI invites your requests for new cell development and will work with you to implement special cells for your design.

Type of Package to be Used

You have a choice of more than 40 different IC packages, including plastic dual-in-lines, plastic-leaded-chip carriers, and pin-grid arrays. A circuit should be partitioned so as to include the greatest number of gates, while minimizing the number of connections to external circuitry.

Examine the Logic to be Partitioned

If the circuit is separated into functional blocks, this may make things easier. Cross out any elements which cannot be included in the IC. Look at the logic, and draw a border around as much of the circuitry as possible while crossing as few conductors (which will become input, output, or I/O pins) as necessary. This is the first pass.

Schematic Evaluation

You may wish to partition your schematic several different ways in order to choose the best standard cell implementation. In each case, examine the tradeoffs between pin count, the number of ICs replaced, and the number of gates integrated.

You can use the following table to simplify evaluation. It should list the system's current parts and functions as well as those that are offered in the cell library.

Table 1. Component Identification

1 UNIT NUMBER	2 DEVICE NUMBER	3 FUNCTION	4 STANDARD CELL CANDIDATE	5 PIN COUNT	6 EQUIV GATES	7 COMMENTS

Column 1 lists the component designator on your schematic.

Column 2 is the component's normal TTL or equivalent part number.

Column 3 lists the function of the IC.

Column 4 usually has a yes/no entry. Use the standard cell library functional index in Section 1. Some standard cell candidates may be dependent on the final decision based on pin count or package size.

Column 5 has the number of pins on the device crossing the borders drawn on the logic diagram (do not count V_{CC} and ground pins). These will be the package signal pins required for the standard cell design (inputs, outputs, and bidirectionals). Remember, some devices might not be fully utilized. The unused circuitry can be excluded from the standard cell IC. Evaluate the possible combinations of components and IC package pin counts to determine cost and functionality.

Column 6 lists the number of equivalent 2-input NAND gates of the standard cell function. This allows the total number of gates required for each partitioning option to be examined.

Use Column 7 to indicate functional features you are considering for standard cell implementation. TI will consider developing special cells specifically for your design. Contact a TI ASIC product specialist for details.

Critical Path Considerations

As a rule, SystemCell™ standard cells meet or exceed the corresponding HC, AHC, and most bipolar logic switching speeds. However, as with any CMOS semiconductor process, standard cells are sensitive to loading. Critical path requirements should be evaluated for propagation delay specifications and output loading. An example of this is in the propagation delay analysis in this section.

Standard cell implementations also offer a significant advantage over conventional discrete logic designs. Because all the cells are on the same chip, the delays of similar cells are well matched. It is not necessary to calculate performance based on combinations of min/max or best/worst assumptions; one calculation assuming minimum speed and another calculation assuming maximum speed will encompass all the possibilities.

Standard Cell Selection

Cell Selection Guidelines

The standard cell library contains over 300 cells, 50 of which are functional equivalents to familiar TTL and CMOS devices. Most SSI cell types are available in several sizes. The different sizes represent variations in physical size, drive capability, power dissipation, and propagation delay. For example, the SN54ASC00 and SN74ASC00 2-input NAND gate is offered with five options. These are listed in Table 2.

Table 2. Options Available for 2-Input NAND Gate

CELL VERSION	RELATIVE DRIVE CAPABILITY	TYPICAL DELAY† (ns)	TYPICAL PWR DISP‡ C_{pd} (pF)	RELATIVE CELL SIZE
NA210LH	1X	2.0	0.51	1
NA220LH	2X	1.3	1	1.5
NA230LH	3X	1.1	1.51	2.0
NA240LH	4X	1.0	2.06	2.5
NA260LH	6X	0.8	2.98	3.5

†$(t_{PLH} + t_{PHL})/2$, C_L = 1 pF
‡Equivalent power dissipation capacitance

As a first-pass rule of thumb, select the cell according to the "Minimum Cell Rule":

"Use the smallest cell size that provides the required circuit performance."

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For the initial layout you should select all 1X cells. Simulations will show where the critical timing paths are located. When timing problems occur during simulation, you can improve your design by using faster and higher fan-out cells in critical locations.

Once you have identified a path failing to meet timing requirements, replace smaller cells with larger cells beginning at the output and working backwards. Additional simulation runs will show when you have solved the problem.

The "Second-Pass Rule of Thumb":

> "Replace gates in a critical path with larger ones, starting from the last element in the critical path and working backward."

There are two additional guidelines that may be applied to cell selection: The "One-Third X Rule" and the "Two-Nanosecond Rule."

One-Third X Rule

Drive a larger cell (say 6X) with a cell one-third as large (say 2X). This simple rule yields optimum speed for a string of gates of the same logical function type. It may not be valid for other configurations.

Two-Nanosecond Rule

Pick the smallest cell such that the product of its Δt_{pd} (change in propagation delay time with capacitance) and the driven node capacitance is less than 2 ns, where Δt_{pd} is defined as the average of the typical values shown for Δt_{PLH} and Δt_{PHL}.

Influence of Capacitive Loading on Cell Choice

When your design includes cells with high drive capabilities, the additional capacitive load represented by these cells and its effect on critical path timing must be accounted for. Although dc fan-out is practically unlimited, CMOS is sensitive to capacitive loading. Evaluate timing requirements carefully and select the best cell option.

Temptations to use large cells throughout your design can result in unnecessarily large input capacitance that imposes unnecessary loading on the driving cell. Use the "First-Pass Rule" explained above.

Propagation Delay Example

In order to estimate the node loading resulting from the metal interconnect capacitance, C_{int}, use the following formula:

$$C_{int}(pF) = (0.088 + 0.104K)(0.83 + 0.136F)$$

K = Circuit total gate count (in thousands of equivalent 2-input NAND gates).
F = Fan-out (number of cell inputs connected to the node).

The change in propagation delay, Δt_{pd}, due to interconnect resistance, I_R, can be estimated using the following formula:

$$\Delta t_{pd}[IR](ns) = 0.002 + (0.1065 + 0.0018K)\, C_{node}$$

C_{node} = total node capacitance in pF = $C_{int} + C_{in}$
C_{in} = combined input capacitance of driven cells.

These are estimations. Actual values will depend on chip layout. Additional examples are given in the appropriate workstation "Standard Cell Design Manual."

Choosing I/O Cells

As part of the evaluation and selection process, input and output buffers are normally selected based on the type of external circuitry that surrounds your standard cell IC. The TI library contains a family of 39 input, output, and bidirectional buffers.

Evaluation of I/Os for a design begins with an identification of the three main interface parameters common to any design. These parameters are:

Input and output logic levels
Output current requirements
Load characteristics, i.e., capacitance, resistive, inductive.

Take into account the added propagation delay imposed by I/O buffers when evaluating timing requirements for a standard cell implementation. You can make this analysis when the output buffer is selected.

The following paragraphs discuss the different types of buffers available from the cell library. Refer to the cell data sheets for more details.

Input Buffers

There are both TTL-compatible and CMOS-compatible input buffers. "Compatible" means no additional interface circuits are required to provide voltage level translation from standard TTL and CMOS (SN54HC and SN74HC) devices. The threshold voltages for the devices are:

CMOS typical threshold = 2.5 V
TTL typical threshold = 1.3 V

Table 3 lists the variety of input cells available for your design.

Table 3. TTL/CMOS Input Cells Available

CELL NUMBER	THRESHOLD	INPUT LOGIC	FEATURES
'ASC5001	TTL	INVERTING	
'ASC5003	TTL	INVERTING	W/HYSTERESIS
'ASC5005	TTL	INVERTING	W/PULL-UP TAP
'ASC5007	TTL	NONINVERTING	
'ASC5010	TTL	NONINVERTING	W/HYSTERESIS AND PULL-UP TAP
'ASC5013	TTL	NONINVERTING	W/PULL-UP TAP
'ASC5006	CMOS	NONINVERTING	
'ASC5002	CMOS	INVERTING	W/HYSTERESIS
'ASC5000	CMOS	NONINVERTING	
'ASC5004	CMOS	INVERTING	W/PULL-UP TAP

Bidirectional Cells and Output Buffers

All output buffers, including the output sections of bidirectional buffer cells are compatible with either TTL or CMOS. Open drain outputs can sink from 4 mA to as much as 48 mA. All output cells and output sections of bidirectional cells are noninverting. Tables 4, 5, and 6 list the variety of cells available.

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Table 4. Output Buffer Availability

LOGIC	OUTPUT BUFFERS	(54/74ASC xxxx) SINK CURRENT CAPACITY					
		4 mA	6 mA	10 mA	24 mA	44 mA	48 mA
NONINVERTING	OPEN DRAIN	'ASC5109	'ASC5105	'ASC5108	-	'ASC5121	'ASC5123
NONINVERTING	PUSH-PULL	'ASC5100	'ASC5103	'ASC5106	'ASC5120	-	-
NONINVERTING	3-STATE ACTIVE	'ASC5110	'ASC5104	'ASC5107	'ASC5125	'ASC5124	-
	LOW-ENABLE	'ASC5111	-	-	-	-	-

Table 5. TTL I/O Buffer Availability (Input)

LOGIC		TTL-INPUT	(54/74SC xxxx) SINK CURRENT CAPACITY				
INPUT	OUTPUT	I/O BUFFERS	4 mA	6 mA	10 mA	24 mA	44 mA
NONINVERTING	NONINVERTING	3-STATE OUTPUT	'ASC5207	'ASC5217	'ASC5227	'ASC5239	-
INVERTING	NONINVERTING	3-STATE OUTPUT	'ASC5201	-	'ASC5221	-	-
INVERTING	NONINVERTING	W/HYSTERESIS	'ASC5203	-	-	-	'ASC5246

Table 6. CMOS I/O Buffer Availability (Input)

LOGIC		CMOS-INPUT	(54/74ASC xxxx) SINK CURRENT CAPACITY			
INPUT	OUTPUT	I/O BUFFERS	4 mA	10 mA	24 mA	44 mA
NONINVERTING	NONINVERTING	3-STATE OUTPUT	'ASC5206	'ASC5226	-	-
INVERTING	NONINVERTING	3-STATE OUTPUT	'ASC5200	'ASC5220	-	-
INVERTING	NONINVERTING	W/HYSTERESIS	'ASC5202	-	-	-
INVERTING	NONINVERTING	W/OPEN DRAIN	-	-	-	'ASC5250

Setup and Hold Times (Timing Requirements)

TI supplied standard cell libraries contain specific information regarding the setup and hold time requirements for hardware macro synchronous elements such as registers and flip-flops. Logic simulators, resident on most workstations, perform pre-layout and post-layout evaluations on the integrity of the design for meeting setup and hold times. Any failure to meet the timing requirements specified in the library is flagged on the workstation, permitting you to evaluate solution alternatives. Additional information is provided in the appropriate workstation *Standard Cell Design Manual*.

Designs submitted to Texas Instruments are evaluated by the design automation system at post-layout prior to device fabrication.

Designing for Testability

Importance of Chip Testability

After functional integrity, the most important design element to incorporate into an integrated circuit is "testability." A common mistake is failing to provide a means for adequate testing of the circuit. Replacing a board with an integrated circuit does not remove the need for control or test points within the IC circuitry. The replacement only compresses the circuitry into a smaller area.

Device testing, field service, and on-board diagnosis are issues that should be considered as you design the IC. Test provisions must be built into the design. The following guidelines will make the design tests more efficient.

Test Design Guidelines

Avoid circuits that require a large number of clock cycles to initialize. In this case, initialization is the "total" absence of unknown or "don't care" conditions.

Signal paths controlling critical sequential state machines or memory elements should be brought out to external pins whenever possible so they can be monitored and controlled externally. Break up long chains of counters into smaller modules with connecting signal paths brought to external pins.

Avoid asynchronous logic whenever possible. Asynchronous logic can be more difficult to test than synchronous logic.

Provide a way to inhibit and examine free-running oscillators. When an oscillator is used on a chip, provision should be made within the design to disable it so an external signal generator can be used. This will allow verification of oscillator performance and the substitution of clocks to simplify testing the remainder of the chip design.

Support Cells and Their Use

The Tie-Off Cell

All internal inputs to each cell must be accounted for in the netlist used to generate the next level of an ASIC design. The common technique of tying unused inputs to a used input is acceptable; however, the associated capacitance is added to the path being developed. Also, terminating internal cell inputs directly to V_{CC} and ground will potentially expose the internal cell input to electrostatic discharge (ESD) and unbuffered noise impulses. The tie-off cell, 'ASC2325, provides ESD-protected high level and low level logic termination for unused inputs. As the termination is static, the cell can provide reference high and low voltages for a large number of inputs.

The internal schematic of the tie-off cell is shown in Figure 1. In operation, output HI will always be high and output LO will be low. Rules governing use of the tie-off cell are

1. Use only one tie-off cell per schematic-capture block. The netlist signal names, replacing HI and LO, should be unique for each tie-off cell used.

2. Designs using the power-up clear cell should have no more than 100 inputs terminated to each tie-off cell output.

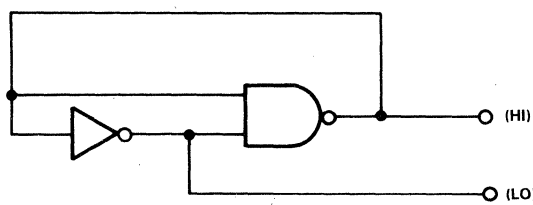

Figure 1. ESD-Protected Tie-Off Cell, 'ASC2325

Power-Up-Clear Cell

The 'ASC2320 power-up-clear cell is used to initialize, preset, or clear bistable elements. As V_{CC} increases upon power-up shown in Figure 2, the power-up-clear output is driven to a low logic level when the "clear initiate" or V1 threshold is reached. As the supply voltage increases further, the "clear release" or CR threshold is reached,

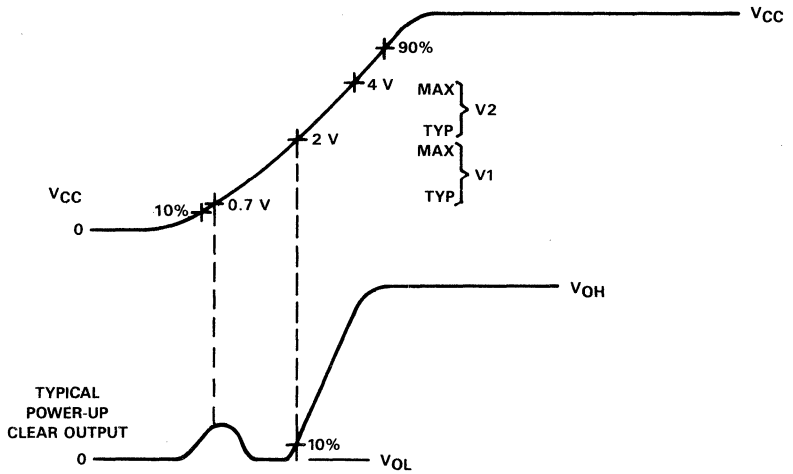

Figure 2. Power-Up-Clear Timing Sequence

and the output returns to a high logic level. This output can be tied to preset or clear lines of counters, registers, flip-flops, latches, or other cells containing bistable functions and serves to initialize them to a known state.

The relationship between V_{CC} rise time and the output pulse width of the power-up-clear signal follows.

V_{CC} RAMPING TIME V_{CC} = 0 V TO V_{CC} = 5 V	TYPICAL RESET PULSE WIDTH
90 ns	45 ns
1 μs	500 ns
1000 μs	280 μs
100 ms	26 ms

The maximum voltage thresholds are as follows:

Clear Initiate (V1) 2 V
Clear Terminate (V2) 4 V.

If voltage spikes occur on the V_{CC} pin, the power-up-clear cell is guaranteed not to be reactivated unless the voltage goes below the V1 threshold of 2 V. If V_{CC} falls below 2 V, the power-up-clear cell could retrigger.

INTERFACING WITH OTHER TECHNOLOGIES

StandardCell™ Packaging and Pin-Out Guidelines

Package Availability

Select the package that has the minimum number of pins required to implement your design. Fewer signal pins typically mean a lower component cost for the standard cell IC and a higher ratio of integration. Table 7 illustrates

some of the packaging options now available and planned. Contact your nearest TI office for the latest availability information.

Table 7. Package Options

PACKAGE DESCRIPTION	DESIGNATOR	PINS																
		8	16	20	24	28	40	44	48	64	68	84	100	108	132	144	164	180	208
Dual-in-line (DIP)	N or (P)	(*)	*	*	*	*	*		*										
	J or (JG)	(*)	*	*	*														
	JD			*	*	*	*		*	*									
Ceramic pin-grid array (PGA)	GB										*	*	*	*	P	*		P	P
Small-outline (SOIC)	D	*	*																
	DW			*	*	*													
Plastic leaded chip carrier (PLCC)	FN			*		*		*			*	*							
Ceramic leadless chip carrier (LCC)	FK			*		*		*			*	*							
Quad plastic flatpack	PQ											P	P		P		P		
Quad ceramic flatpack	HQ											P	P		P		P		

* = Available, P = Planned

NOTE: For packaging needs beyond that shown above, and for applications (military versus commercial) information, contact your local TI field sales representative.

Pin Assignment Techniques

In some cases, the assignment of each package pin to an I/O signal, power, or ground is predetermined by the user. An example would be an application where a standard cell design replaces an existing logic array device. If the pin-out selection is not fixed in advance, certain guidelines are recommended during the selection process.

Select Power and Ground Pins for Minimum Inductance

This will reduce transient voltages. For most chip-carrier-style packages, there is little difference in inductance between package pins. However, for dual-in-line and pin-grid-array packages, there is a significant difference in inductance between some pins. The corner pins of DIP packages may have as much as four times the inductance of center pins.

Do Not Position Power Pins Opposite Each Other

Incorrect insertion of the IC should not reverse power and ground voltages. Proper placement can preclude possible damage to the IC.

Position I/O Clocks and Strobes Near the Ground Pin

All I/O signals that control a path leading to a clock, preset, or clear of a flip-flop, or the enable input of a latch, should be located as near a ground pin as possible. This will minimize the possibility of having a storage element disturbed by ground noise.

Position High Current Pins Near the Appropriate Power Pin

Position outputs with high sink current requirements close to the ground pin(s). Position outputs with high source current requirements near the V_{CC} pin(s). These placements will minimize voltage drops due to chip metalization. Placement of outputs with high sink current requirements take precedence over placement of outputs with high current source requirements, since the noise level tolerated by high level signals is greater.

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INTRODUCTION TO TI HARDWARE DESCRIPTION LANGUAGE (HDL)

The Hardware Description Language (HDL) is a hierarchical listing describing each cell and all cell connections that comprise a standard cell design. HDL is used for simulation, test programs, and final chip layout. Understanding HDL and how it is derived can help you find common errors during schematic capture. The standard cell design shown in Figure 3 will be used as an example. The design has been given the name COUNT.SYM. Figure 4 shows the complete HDL listing for the design.

HDL Hierarchy

An HDL listing is divided into blocks, and each block is divided into sections. The first part of an HDL listing is called the Design Block. There is only one Design Block for a given hierarchy of a design. The Design Block contains the name of the overall circuit, in this case COUNT, and lists all input and output connections you have assigned during the schematic capture phase. Global variables are also defined within this block, such as V_{CC}, V_{DD}, and GND (ground).

The second section is called the Environment. It is very short and appears only in the Design Block. It names the CMOS technology and the global signals for the circuit.

The second major block within HDL is the Structure Block. It describes the circuit's cells and their interconnections using individual HDL statements for each cell.

Individual HDL Statements

Each HDL statement within a Structure Block consists of three parts: the label, the cell name, and the input/output default net names. As each cell is called and placed into a design, assign a unique component identifier to each cell. This name becomes the "label" portion of the cell's HDL statement. As the input and output connections are made, the cell's HDL I/O default names are replaced by the net names you have assigned. Labels and net names are limited to 15 characters. Try to keep them short to improve schematic readability.

Refer to Figures 3 and 4 for the following discussion. The DFB20LH flip-flop, used in the COUNT circuit, is shown in Figure 3 as it appears in the datasheet. The HDL statement for the example circuit's HDL listing is generated by schematic capture and is shown in Figure 4.

Every input and output must be connected to preserve the correct order. The example in Figures 3 and 4 shows that the CLRZ input of the flip-flop FF1 is connected to a net with the name S3; the PREZ input is connected to net PREZ; the D input is connected to net F0Z; the CLK input is connected to net S1; the Q output is connected to net F0; and the QZ output is connected to net F0Z.

Additional HDL statements describe the remaining cells in the same manner. If soft macros are used, additional structure blocks will appear in the HDL listing describing the macro's internal cells and interconnections.

TEST PATTERN GENERATION AND TDL

Correctness of the logic diagram is verified through the use of the workstation's test simulator. Although each simulator may operate differently, the results are similar. Initial conditions are described, the inputs are stimulated, and after a specified period of time the outputs are measured for expected conditions. If the measured test conditions match expected conditions, the design has passed, and the next set of conditions is applied. This combination—initial conditions, input stimulus, and expected outputs—is called a test pattern.

Test patterns can be made up of many smaller patterns, each describing a different input stimulus. A test pattern may use the previous pattern's internal states and output conditions as its initial conditions before new input

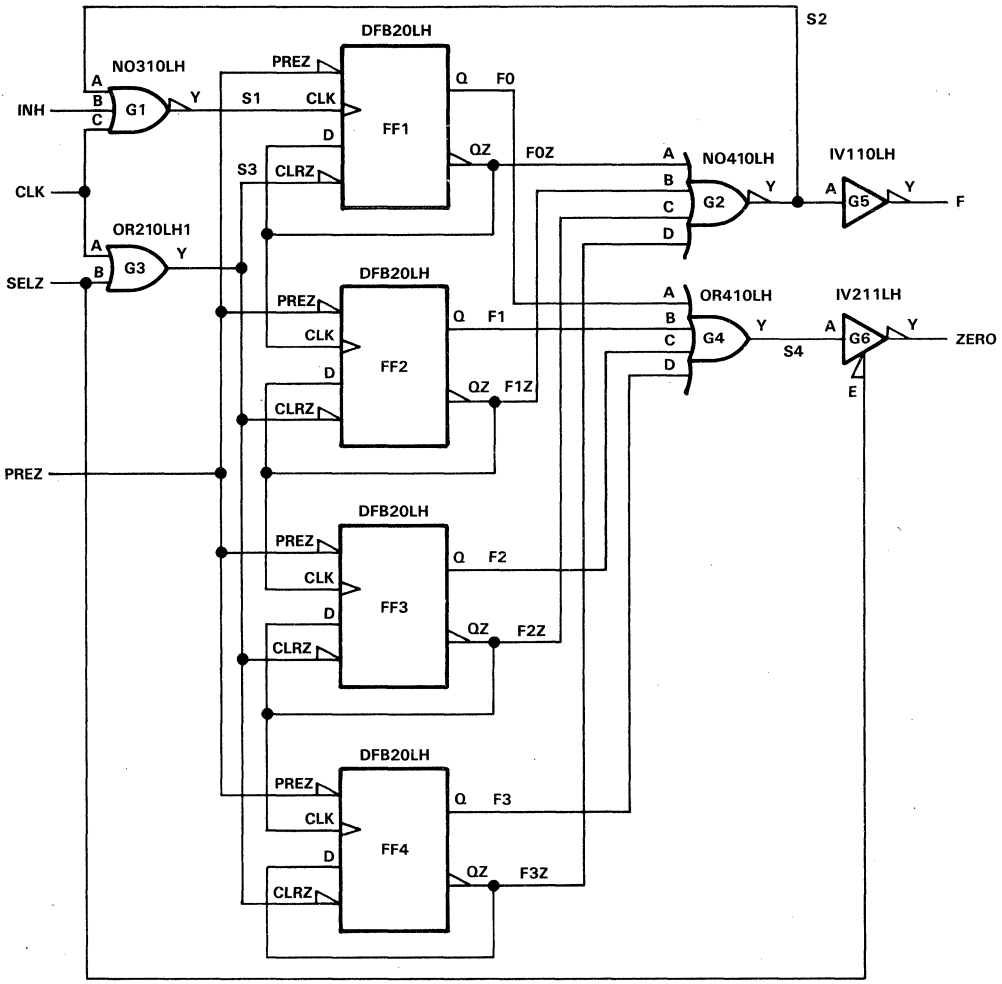

Figure 3. Circuit Schematic for HDL Example

conditions are applied. This cycle, continuing until all logic states are tested, accommodates testing of counters, registers, and other sequential-type circuitry.

A Test Description Language (TDL) pattern set is created from the workstation's simulation patterns by the TDL extraction program. Your simulation patterns may need to be modified in order to obtain a complete test routine. TI uses the TDL database to program integrated circuit test equipment.

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```
BLOCK COUNT     DESIGN;
SELZ            @INPUT;
CLK             @INPUT;
INH             @INPUT;
PREZ            @INPUT;
ZERO            @OUTPUT;                                    } DESIGN BLOCK
F               @OUTPUT;

DUM             @(GLOBAL,DUMMY);
VCC             @(GLOBAL,LOCAL,VOLTAGE,TIEOFF = L'1');
VDD             @(GLOBAL,LOCAL,VOLTAGE,TIEOFF = L'1');
GND             @(GLOBAL,LOCAL,VOLTAGE,TIEOFF = L'0');

ENVIRONMENT

TECHNOLOGY CMOS, PROCESS = CMOS;                            } ENVIRONMENT
VOLTAGE VCC,VDD,GND;                                        } BLOCK
GLOBAL DUM;

STRUCTURE

FF1             :DFB20LH        S3,PREZ,F0Z,S1,F0,F0Z;
FF2             :DFB20LH        S3,PREZ,F1Z,F0Z,F1,F1Z;
FF3             :DFB20LH        S3,PREZ,F2Z,F1Z,F2,F2Z;
FF4             :DFB20LH        S3,PREZ,F3Z,F2Z,F3,F3Z;     } STRUCTURE BLOCK
G1              :NO310LH        S2,INH,CLK,S1;
G2              :NO410LH        F0Z,F1Z,F2Z,F3Z,S2;
G3              :OR210LH        CLK,SELZ,S3;
G4              :OR410LH        F0,F1,F2,F3,S4;
G5              :IV110LH        S2,F;
G6              :IV211LH        S4, SELZ,ZERO;

END COUNT;
```

Figure 4. HDL Listing

Some TDL Guidelines

TDL applies input changes at fixed intervals to conditioning test vectors by selectively sequencing inputs to meet setup and hold time requirements. It is not possible to test for asynchronous conditions.

Clock signals should occur after the beginning of a test cycle. The test cycle should be a multiple of the clock rate.

Only inputs, outputs, and nodes brought out to package pins are testable.

Logic levels at internal nodes must be preset by providing specific input conditions.

For more information on test pattern generation, refer to the appropriate workstation design manual, as well as to the workstation operating manuals.

Power Dissipation in Standard Cells

Quiescent Power (P_q)

Under dc conditions, when an ideal CMOS device is not switching, supply current should not flow. In reality, CMOS devices do have small leakage currents flowing across the reverse-biased junction diodes. This leakage,

or quiescent current, is due to thermally generated charge carriers near the junction, and it characteristically increases with increasing temperature. For standard cells, the total current is dependent on the total active area of gates and elements used in a design.

Table 8 shows the maximum quiescent current for designs of up to 20,000 gates.

Table 8. Maximum Quiescent Current for CMOS Devices

NO. GATES	I_{CCQ} (nA)	NO. GATES	I_{CCQ} (nA)
500	100	10500	1100
1000	150	11000	1150
2000	250	12000	1250
3000	350	13000	1350
4000	450	14000	1450
5000	550	15000	1550
6000	650	16000	1650
7000	750	17000	1750
8000	850	18000	1850
9000	950	19000	1950
10000	1050	20000	2050

Intracell Transient Power (P_t)

Transient power dissipation occurs due to current flowing when the CMOS transistor is switching logic levels. The magnitude of intracell transient power is a function of cell capacitance (intrinsic and parasitic), as well as transient energy required to change states.

Intercell Transient Power (P_C)

Intercell transient power dissipation is a function of frequency and the cell interconnect scheme. Independent of the frequency of operation it consists of two major elements: the external load capacitance and external parasitic capacitance.

Typically, CMOS draws two orders of magnitude less quiescent power than equivalent LS functions. When the CMOS function is switching, the transient power dissipation is efficiently consumed to achieve only the performance level desired, as dynamic dissipation is directly proportional to the operating frequency. Consider the components above (P_q, P_t, and P_C) when determining total power dissipation for CMOS standard cells.

Latch-Up Protection

There are two parasitic bipolar (NPN and PNP) transistors within all standard CMOS structures. These parasitic transistors begin to conduct when one or more of the PN junctions becomes forward-biased. If the current gain of the parasitic transistors is large a Silicon Controlled Rectifier (SCR) action can be achieved. This produces latchup, which can be destructive if steps are not taken to limit latchup currents to safe values.

The TI CMOS designs, including standard cell inputs and outputs, incorporate guard rings designed to protect against latch-up resulting from exposure to currents with magnitudes up to 400 mA.

Electrostatic Discharge Protection

Electrostatic discharge (ESD) occurs when a build-up of electrostatic charge on a surface "jumps" or "arcs" through a dielectric to another surface. Electrostatic charge is generated and stored on the surfaces of ordinary materials such as common textile garments and plastics. The passage of this charge through an electrostatic-sensitive part may result in catastrophic damage or performance degradation of the device.

TI has developed unique circuitry that can identify and control the safe discharge of relatively large electrostatic charges. This circuitry is designed to protect inputs and outputs from the effects of ESD.

The primary protection element for an input is a large lateral NPN transistor, shown in Figure 5, placed at the input pad. It shunts ESD current directly to the ground bus. It is also effective in clamping both negative- and positive-going transient voltage. Diodes to both V_{CC} and ground offer additional output protection as shown in Figure 6.

Observe appropriate precautions when handling CMOS devices.

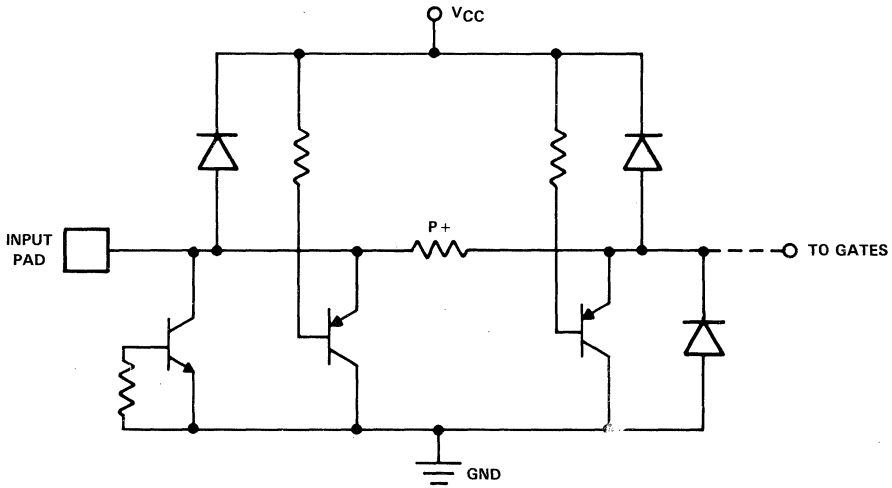

Figure 5. Schematic of Input Protection

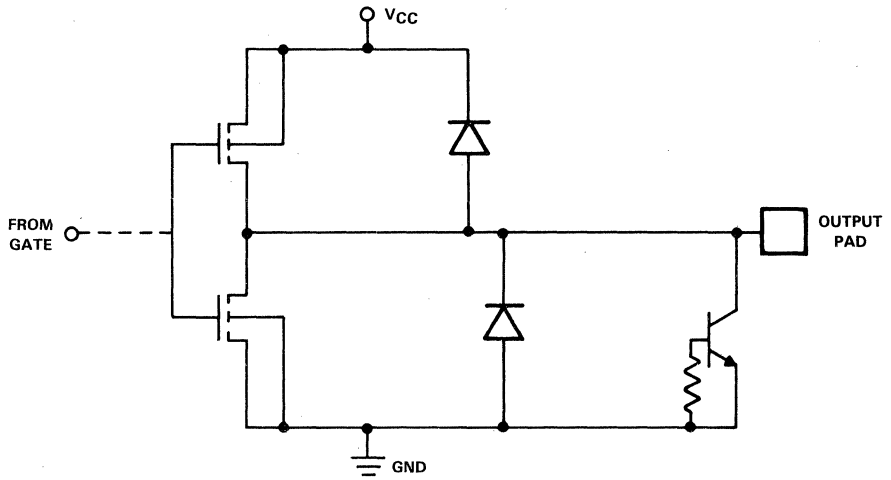

Figure 6. Schematic of Output Protection

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Electrical characteristics presented in this data book, unless otherwise noted, apply to standard cells prior to interconnect routing and packaging. Characteristics and effects of routing, cell layout, and interconnection of a completed ASIC design are covered in the post-layout simulation software. The capacitive loading effects of the package bond wire(s) and terminals(s) are assumed to be a portion of the 15 pF or 50 pF switching-characteristics load shown for the output and I/O cells. Typically, the packaging bond-wire and terminal capacitance values range from 1 to 2 pF. Consult TI's design-center personnel for further assistance in choosing and specifying ASIC packaging options.

package selection

Outline drawings presented in this section are for both conventional through-hole and surface-mount packages. The following classes of packages are covered.

Dual-in-line (DIP), plastic and ceramic
Pin-grid-array (PGA), ceramic
Small-outline (SO), plastic
Ceramic leadless chip carriers (LCC)
Plastic leaded chip carriers (PLCC)
Ceramic quad flatpacks

These packages are recommended as a representative selection which satisfies a wide range of ASIC applications. TI will review and consider supplying package requirements other than those shown.

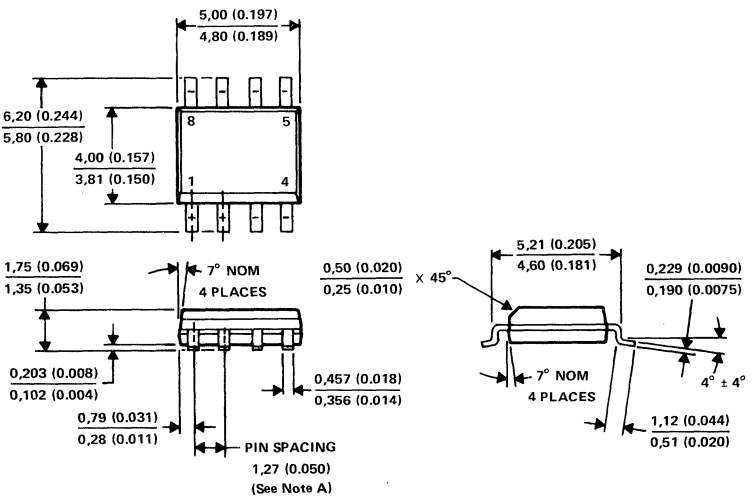
ordering instructions

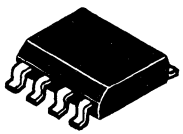
Implementation of semiconductor solutions using **SystemCell™** components normally results in an application-specific integrated circuit. Total specifications, including packaging and ordering instructions, are developed as a part of this Design Specification described in Section 1. Contact your TI representative for further information on getting started with an ASIC design.

D plastic "small outline" packages

Each of these "small outline" packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

8-PIN D PACKAGE





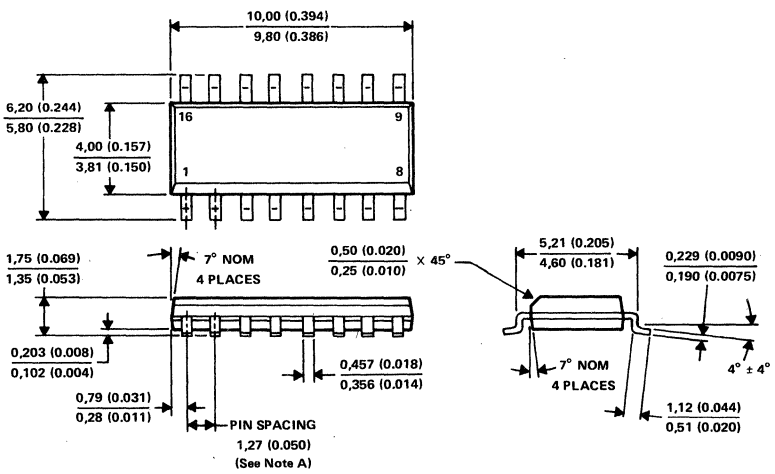
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

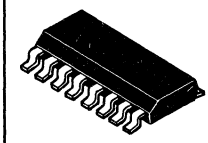
NOTES: A. Body dimensions do not include mold flash or protrusion.
B. Mold flash or protrusion shall not exceed 0,15 (0.006).
C. Leads are within 0,25 (0.010) radius of true position at maximum material dimension.
D. Lead tips to be planar within ±0,051 (0.002) exclusive of solder.

D plastic "small outline" packages

Each of these "small outline" packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

16-PIN D PACKAGE





ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Body dimensions do not include mold flash or protrusion.
B. Mold flash or protrusion shall not exceed 0,15 (0.006).
C. Leads are within 0,25 (0.010) radius of true position at maximum material dimension.
D. Lead tips to be planar within ±0,051 (0.002) exclusive of solder.

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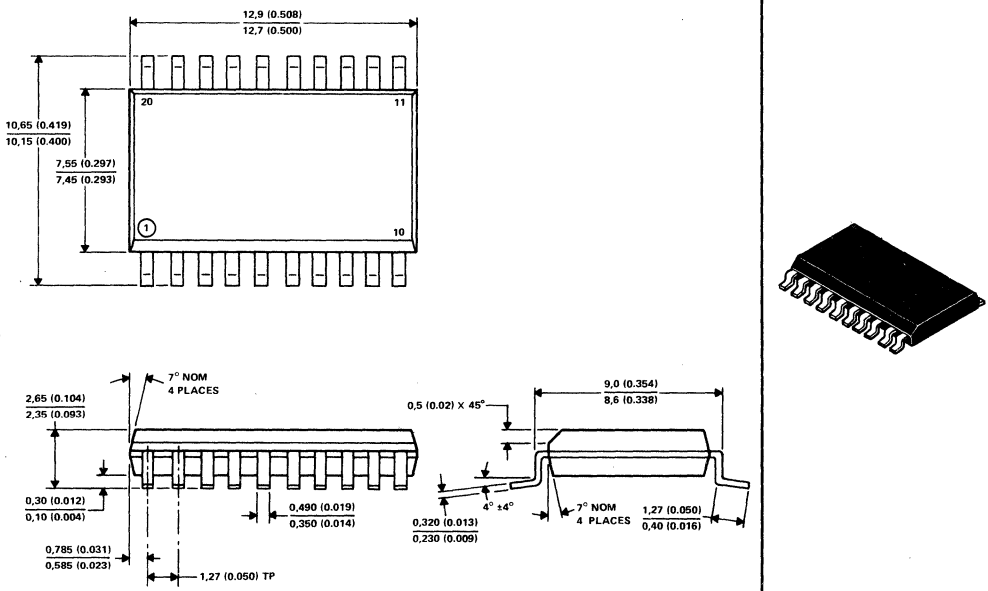
DW plastic "small outline" packages

Each of these "small outline" packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

20-PIN DW PACKAGE



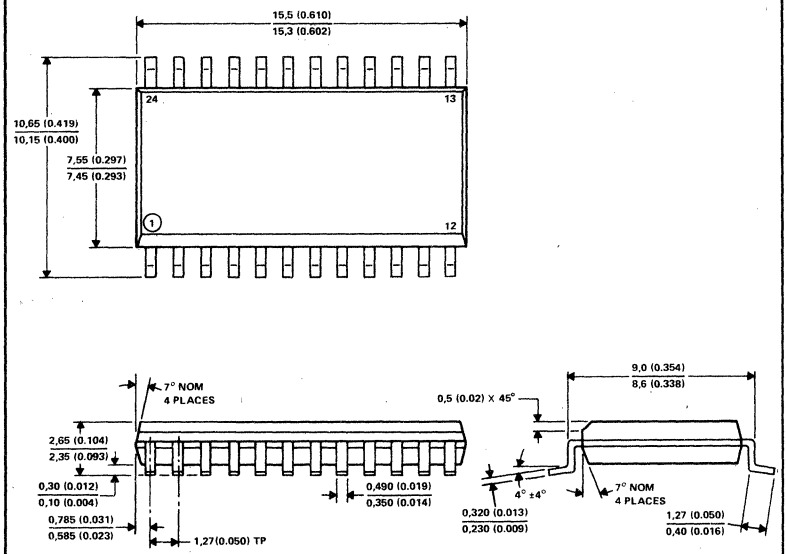
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

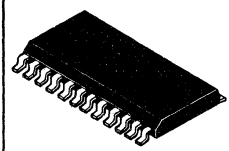
NOTES: A. Body dimensions do not include mold flash or protrusion.
B. Mold flash or protrusion shall not exceed 0,15 (0.006).
C. Leads are within 0,25 (0.010) radius of true position at maximum material dimension.
D. Lead tips to be planar within ±0,051 (0.002) exclusive of solder.

DW plastic "small outline" packages

Each of these "small outline" packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

24-PIN DW PACKAGE





ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Body dimensions do not include mold flash or protrusion.
B. Mold flash or protrusion shall not exceed 0,15 (0.006).
C. Leads are within 0,25 (0.010) radius of true position at maximum material dimension.
D. Lead tips to be planar within ±0,051 (0.002) exclusive of solder.

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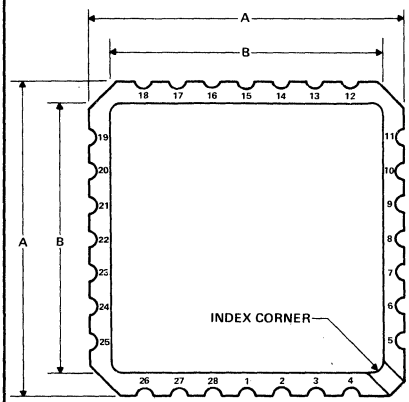
FK ceramic chip carrier packages

Each of these hermetically sealed chip carrier packages has a three-layer ceramic base with a metal lid and braze seal. The packages are intended for surface mounting on solder lands on 1,27 (0.050-inch) centers. Terminals require no additional cleaning or processing when used in soldered assembly.

FK package terminal assignments conform to JEDEC Standards 1, 2, and 11.

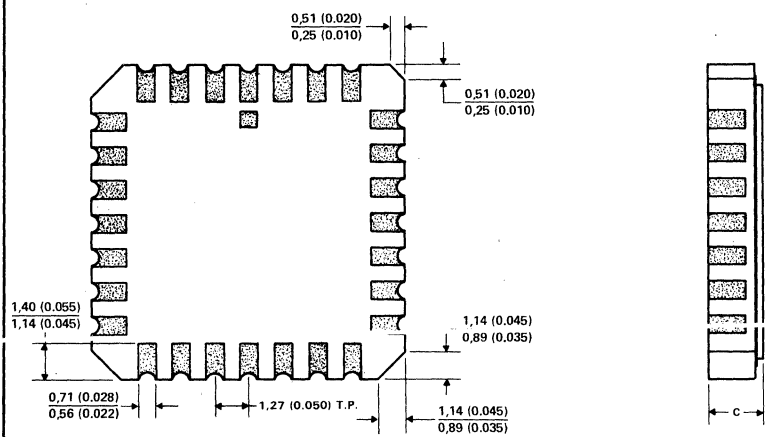
FK CERAMIC CHIP CARRIER
(28-terminal package shown)



CERAMIC CHIP CARRIERS

JEDEC OUTLINE DESIGNATION*	NO. OF TERMINALS	A MIN	A MAX	B MAX	C MIN	C MAX
MS004CB	20	8,69 (0.342)	9,09 (0.358)	9,09 (0.358)	1,63 (0.064)	2,03 (0.080)
MS004CC	28	11,23 (0.422)	11,63 (0.458)	11,63 (0.458)	1,63 (0.064)	2,03 (0.080)
MS004CD	44	16,26 (0.640)	16,76 (0.660)	14,22 (0.560)	1,75 (0.069)	3,05 (0.120)
MS004CF	68	28,83 (0.938)	24,43 (0.962)	21,89 (0.862)	2,08 (0.082)	3,05 (0.120)
MS004CG	84	28,83 (1.135)	29,59 (1.165)	27,05 (1.065)	2,08 (0.082)	3,05 (0.120)

*All dimensions and notes for the specified JEDEC outline apply.

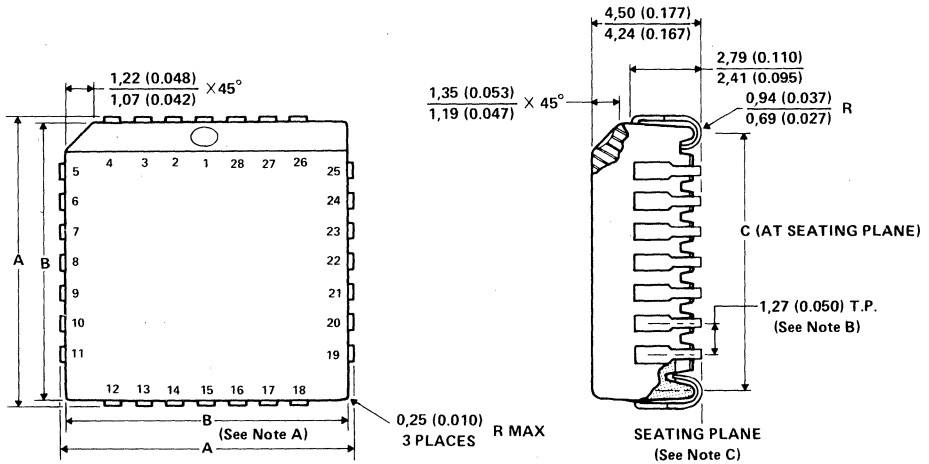


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

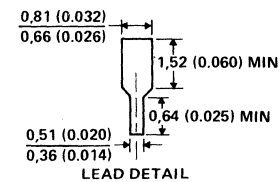
FN plastic chip carrier package

Each of these chip carrier packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound withstands soldering temperatures with no deformation, and circuit performance characteristics remain stable when the devices are operated in high-humidity conditions. The packages are intended for surface mounting on solder lands on 1,27 (0.050) centers. Leads require no additional cleaning or processing when used in soldered assembly.

FN PLASTIC CHIP CARRIER
(28-terminal package used for illustration)



JEDEC OUTLINE	NO. OF TERMINALS	A MIN	A MAX	B MIN	B MAX	C MIN	C MAX
MO-047AA	20	9,78 (0.385)	10,03 (0.395)	8,89 (0.350)	9,04 (0.356)	7,87 (0.310)	8,38 (0.330)
MO-047AB	28	12,32 (0.485)	12,57 (0.495)	11,43 (0.450)	11,58 (0.456)	10,41 (0.410)	10,92 (0.430)
MO-047AC	44	17,40 (0.685)	17,65 (0.695)	16,51 (0.650)	16,66 (0.656)	15,49 (0.610)	16,00 (0.630)
MO-047AE	68	25,02 (0.985)	25,27 (0.995)	24,13 (0.950)	24,33 (0.956)	23,11 (0.910)	23,62 (0.930)
MO-047AF	84	30,10 (1.185)	30,35 (1.195)	29,21 (1.150)	29,41 (1.158)	27,69 (1.090)	28,70 (1.130)



All dimensions and notes for the specified JEDEC outline apply.

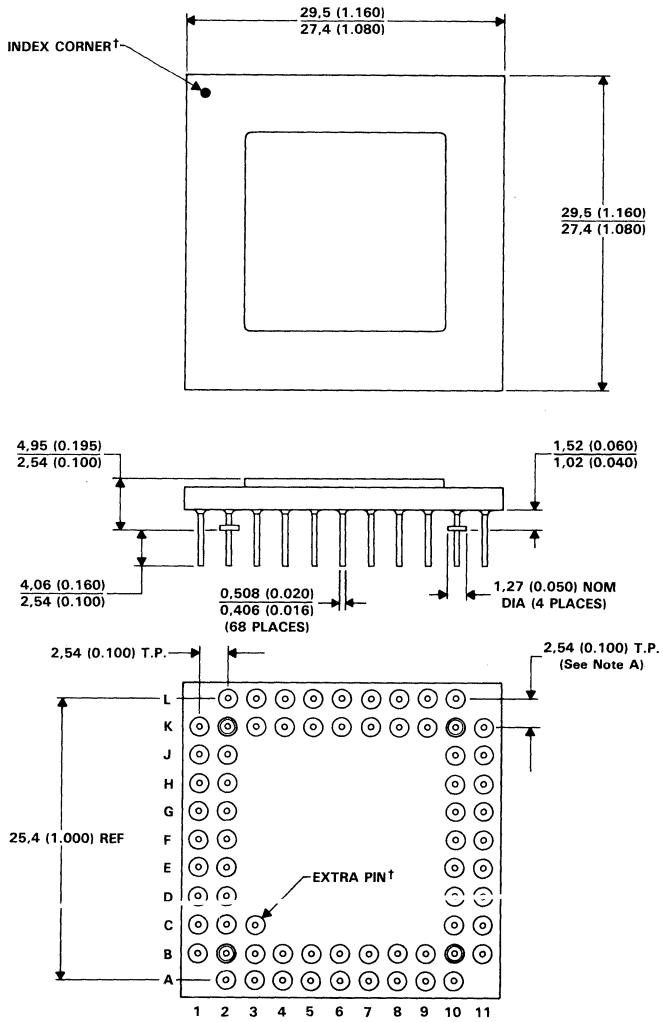
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Centerline of center pin each side is within 0,10 (0.004) of package centerline as determined by dimension B.
B. Location of each pin is within 0,127 (0.005) of true position with respect to center pin on each side.
C. The lead contact points are planar within 0,10 (0.004).

GB pin-grid-array ceramic package

This is a hermetically sealed package with metal cap and gold-plated pins.

68-PIN GB



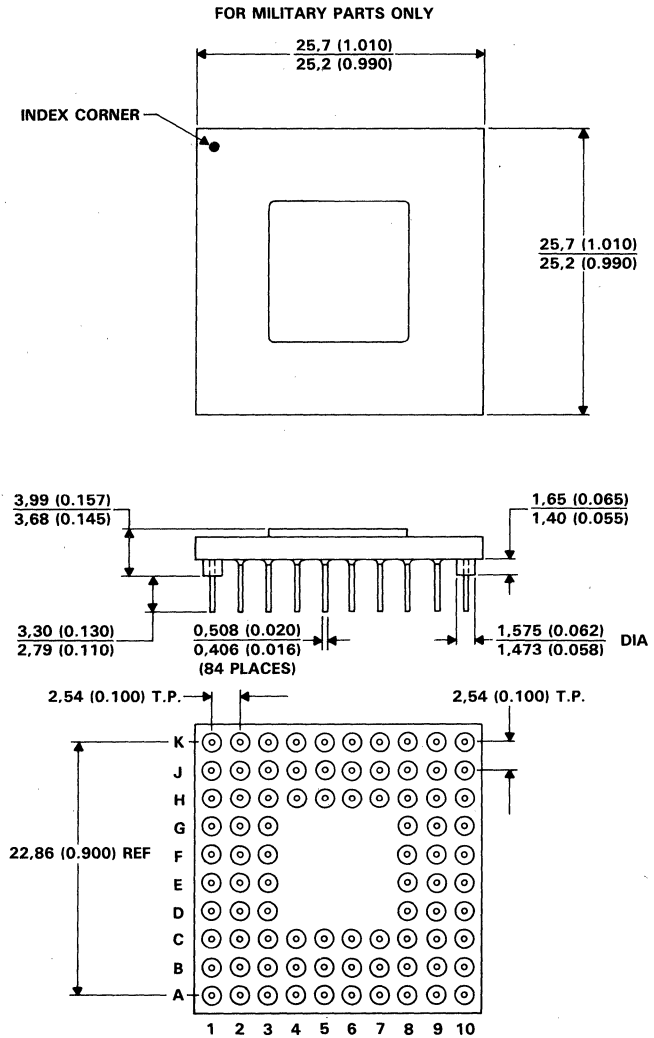
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

† Index mark may appear on top or bottom depending on package vendor.
‡ Not featured on single level ceramic packages.
NOTE A: Pins are located within 0,13 (0.005) radius of true position relative to each other at maximum material condition and within 0,25 (0.010) radius relative to the center of the ceramic.

GB pin-grid-array ceramic package (Form 1)

This is a hermetically sealed package with metal cap and gold-plated pins.

84-PIN GB (FORM 1)



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Pins are located within 0,13 (0.005) radius of true position relative to each other at maximum material condition and within 0,25 (0.010) radius relative to the center of the ceramic.

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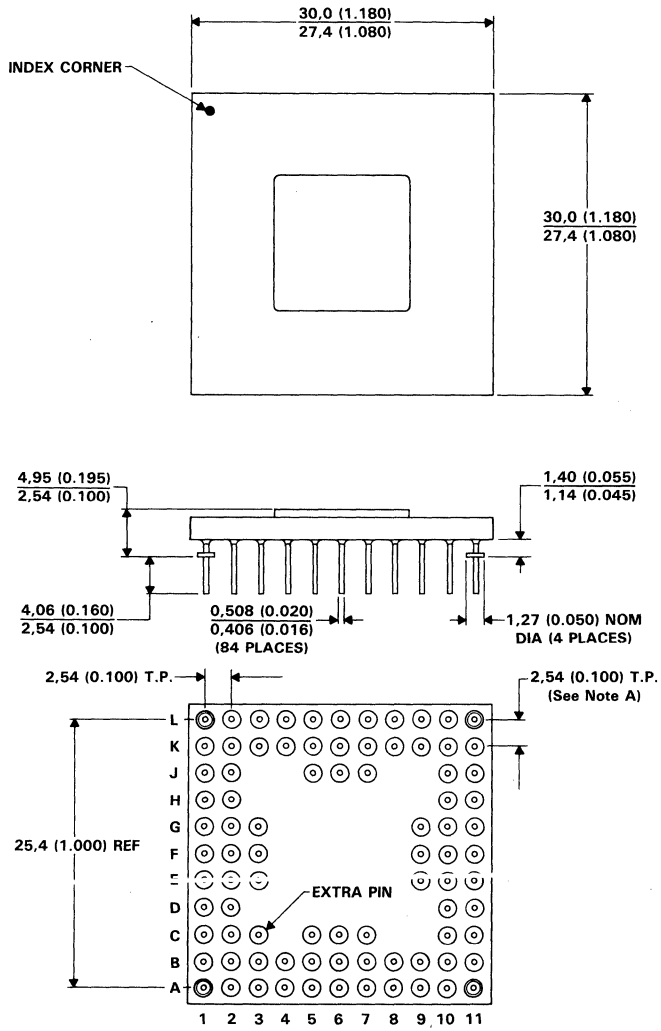
GB pin-grid-array ceramic package (Form 2)

This is a hermetically sealed package with metal cap and gold-plated pins.

84-PIN GB (FORM 2)



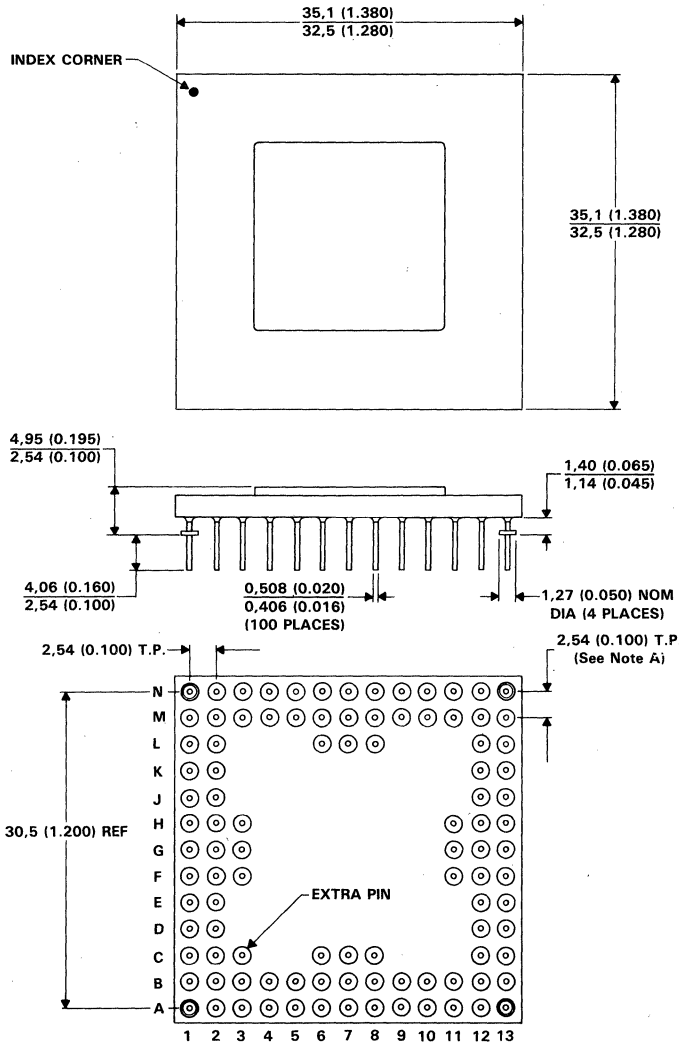
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Pins are located within 0,13 (0.005) radius of true position relative to each other at maximum material condition and within 0,25 (0.010) radius relative to the center of the ceramic.

GB pin-grid-array ceramic package

This is a hermetically sealed package with metal cap and gold-plated pins.

100-PIN GB



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Pins are located within 0,13 (0.005) radius of true position relative to each other at maximum material condition and within 0,25 (0.010) radius relative to the center of the ceramic.

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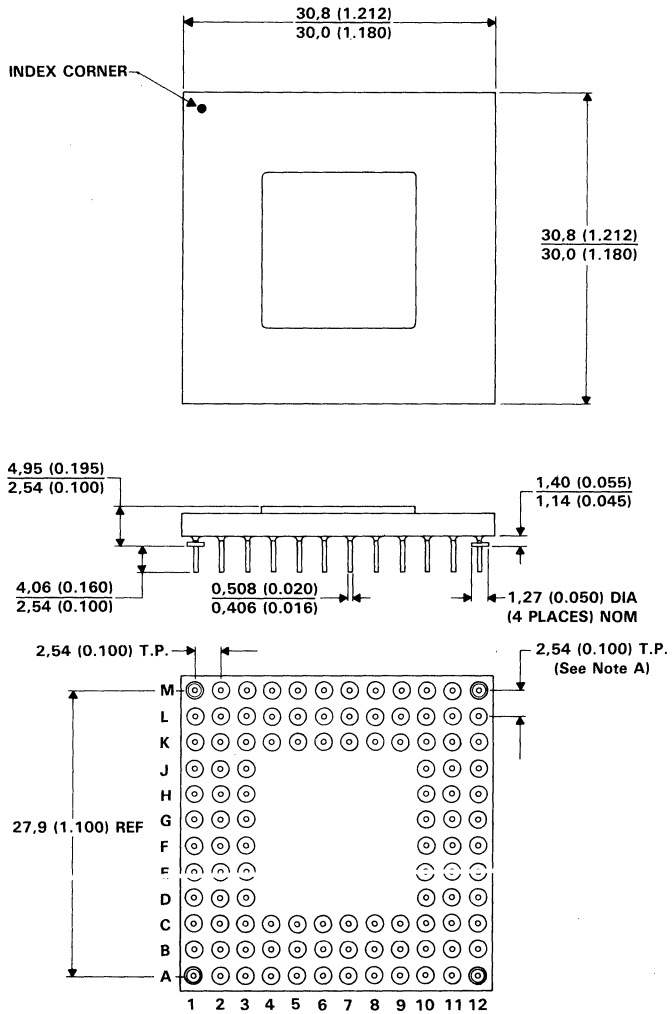
GB pin-grid-array ceramic package

This is a hermetically sealed package with metal cap and gold-plated pins.

108-PIN GB



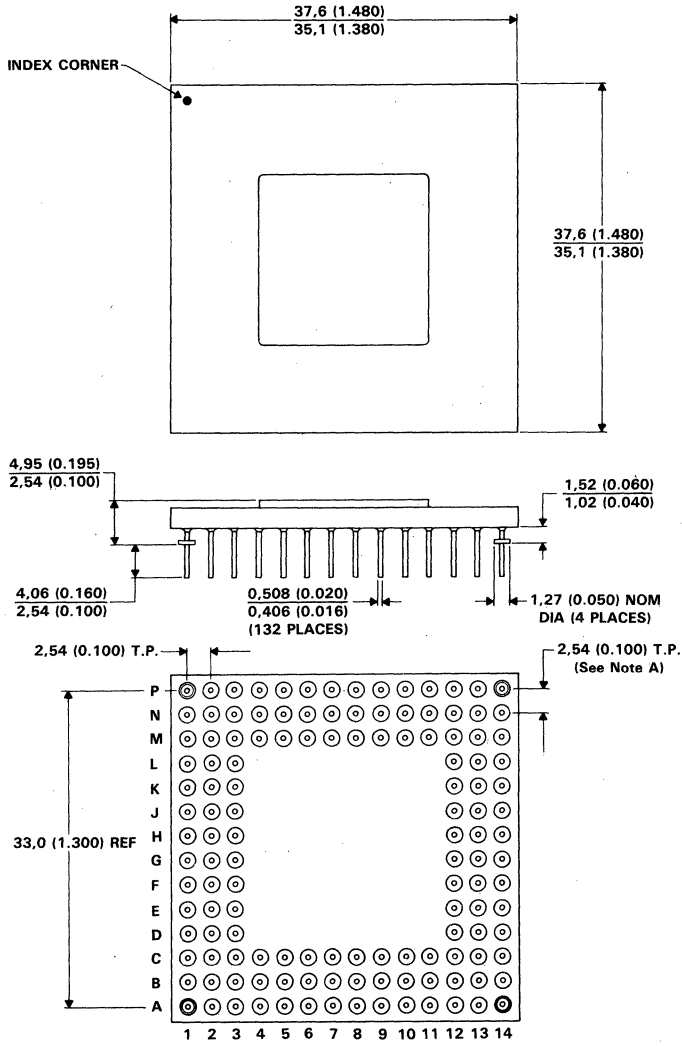
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Pins are located within 0,13 (0.005) radius of true position relative to each other at maximum material condition and within 0,25 (0.010) radius relative to the center of the ceramic.

GB pin-grid-array ceramic package

This is a hermetically sealed package with metal cap and gold-plated pins.

132-PIN GB



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Pins are located within 0,13 (0.005) radius of true position relative to each other at maximum material condition and within 0,25 (0.010) radius relative to the center of the ceramic.

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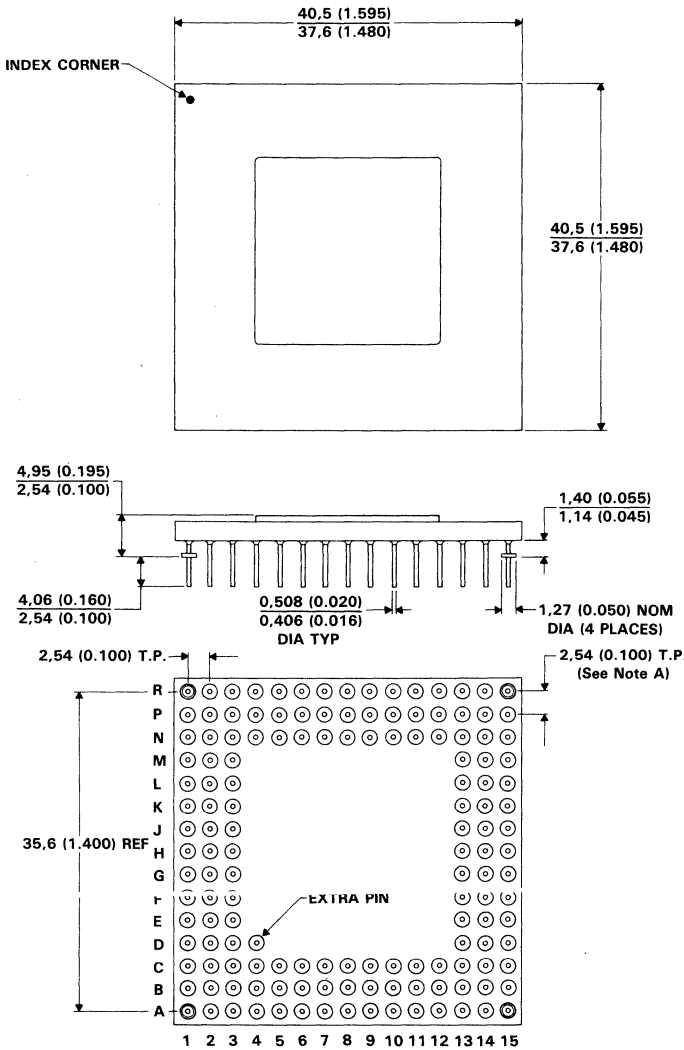
GB pin-grid-array ceramic package

This is a hermetically sealed package with metal cap and gold-plated pins.

144-PIN GB



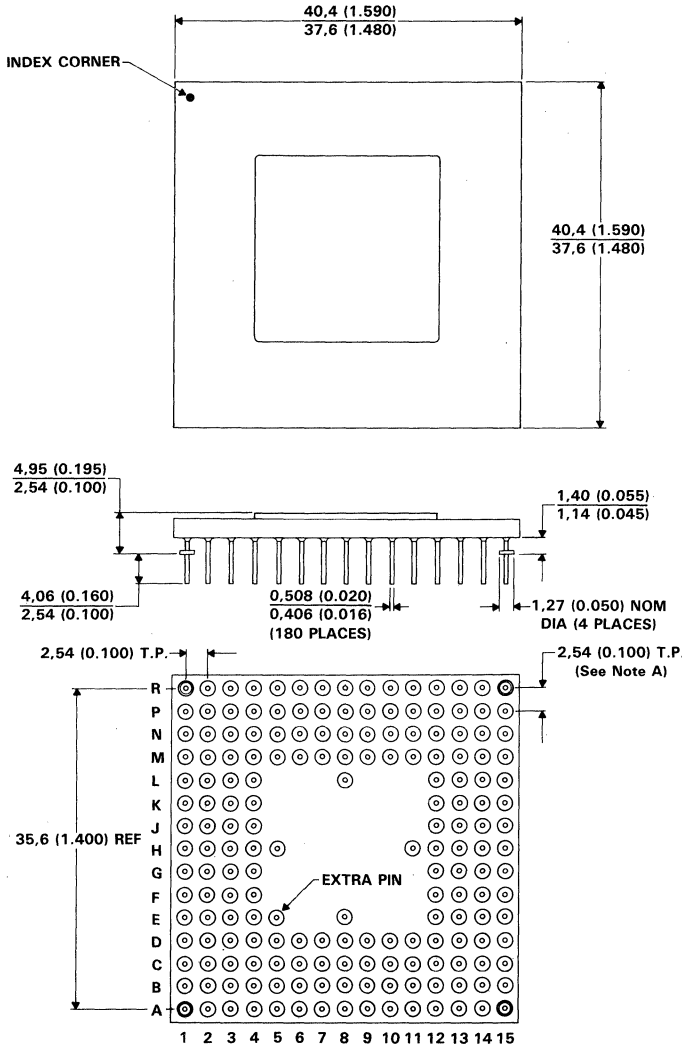
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Pins are located within 0,13 (0.005) radius of true position relative to each other at maximum material condition and within 0,25 (0.010) radius relative to the center of the ceramic.

GB pin-grid-array ceramic package

This is a hermetically sealed package with metal cap and gold-plated pins.

180-PIN GB



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Pins are located within 0,13 (0.005) radius of true position relative to each other at maximum material condition and within 0,25 (0.010) radius relative to the center of the ceramic.

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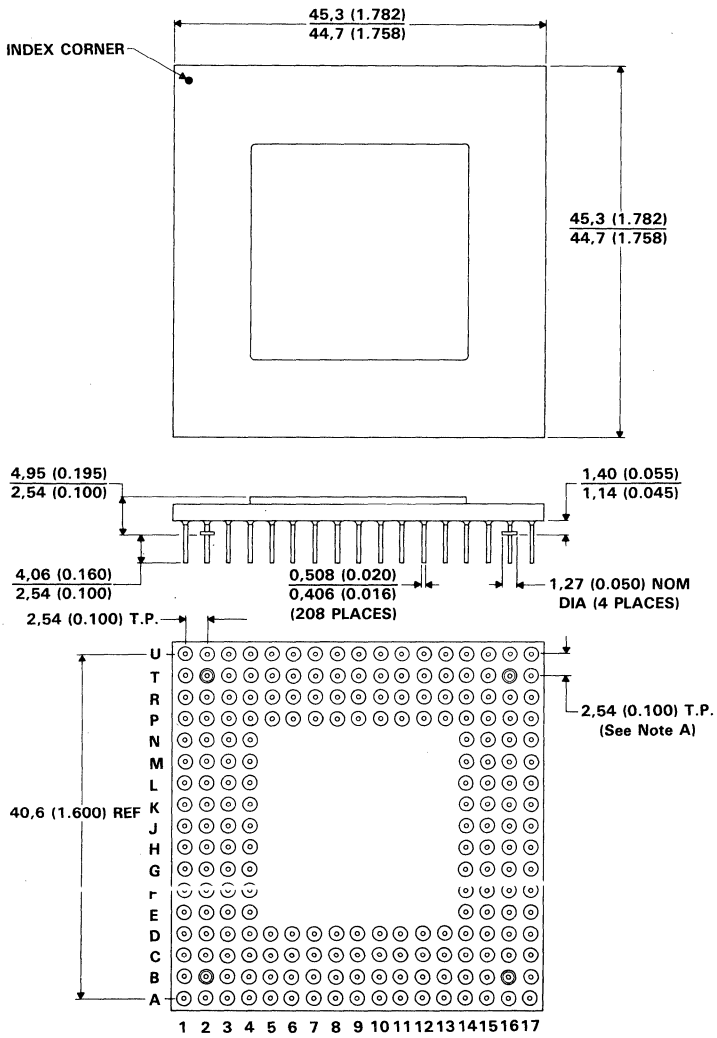
GB pin-grid-array ceramic package

This is a hermetically sealed package with metal cap and gold-plated pins.

208-PIN GB



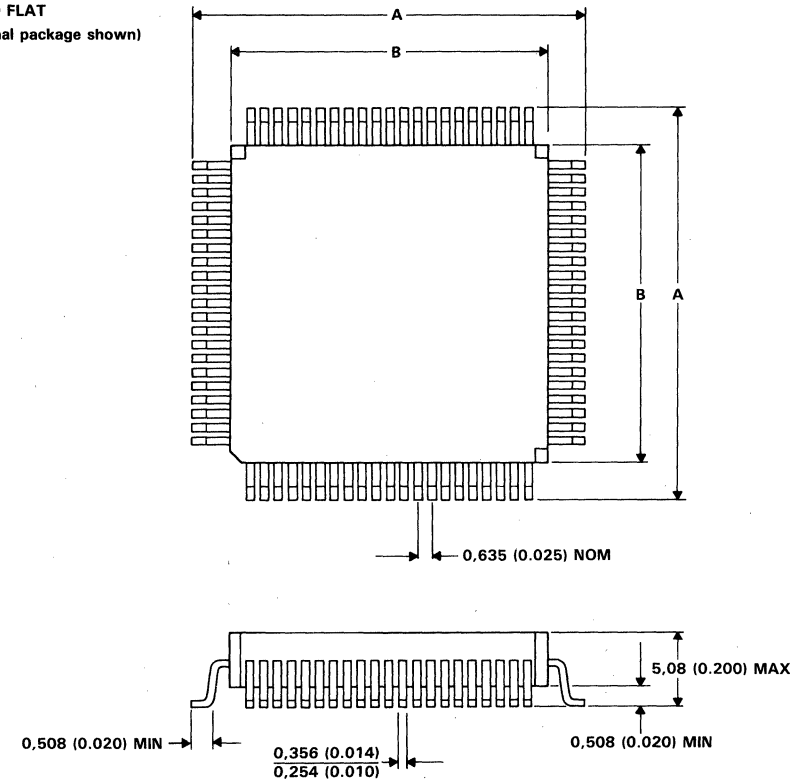
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Pins are located within 0,13 (0.005) radius of true position relative to each other at maximum material condition and within 0,25 (0.010) radius relative to the center of the ceramic.

HQ quad flat packages

The members of this family of hermetically sealed quad flat packs have 0.025-inch-lead spacing and have gull-wing bent leads suitable for surface-mounting. A plastic version is proposed for introduction at a future date.

HQ QUAD FLAT
(84-terminal package shown)



NUMBER OF TERMINALS	A		B	
	MIN	MAX	MIN	MAX
84	22,81 (0.898)	23,42 (0.922)	14,48 (0.570)	18,54 (0.730)
100	25,35 (0.998)	25,96 (1.022)	18,80 (0.740)	19,30 (0.760)
132	28,45 (1.120)	29,06 (1.144)	21,90 (0.862)	22,40 (0.882)
164	35,51 (1,398)	36,12 (1.422)	28,96 (1.140)	29,45 (1.160)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

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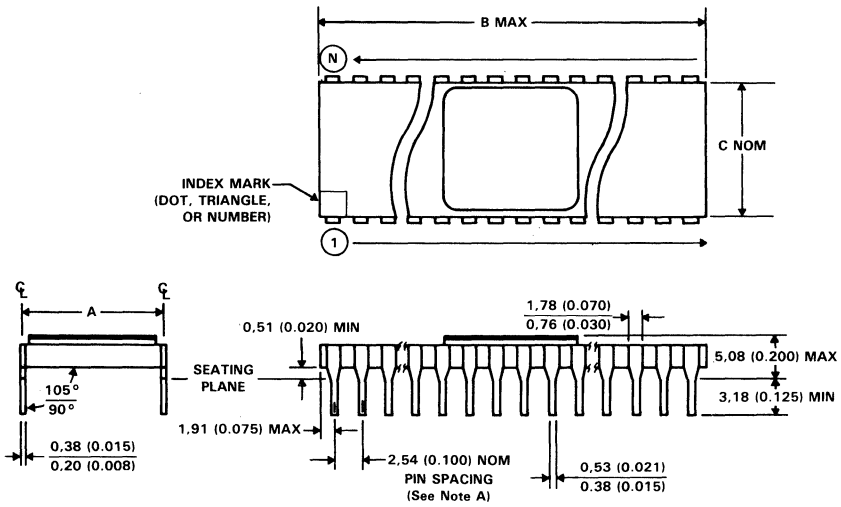
JD ceramic dual-in-line packages

This is a hermetically sealed ceramic package with a metal cap and side-brazed tin-plated leads.

NOTE: For the 24-pin packages, the letters JDT must be specified for 7,62 (0.300) row spacing or JDW for 15,24 (0.600) row spacing.

JD CERAMIC—SIDE BRAZE



300-mil PACKAGES

DIM \ PINS (N)	20	24
A +0.51 (+0.020) −0,25 (−0.010)	7.62 (0.300)	7.62 (0.300)
B (MAX)	25,65 (1.010)	30,86 (1.215)
C (NOM)	7,37 (0.290)	7,37 (0.290)

600-mil PACKAGES

DIM \ PINS (N)	24	28	40	48	64
A +0.51 (+0.020) −0,25 (−0.010)	15,24 (0,600)	15,24 (0.600)	15,24 (0.600)	15,24 (0.600)	22,86 (0.900)
B (MAX)	31,8 (1.250)	36,8 (1,450)	52,1 (2.050)	62,2 (2.450)	82,6 (3.250)
C (NOM)	15,0 (0.590)	15,0 (0.590)	15,0 (0.590)	15,0 (0.590)	22,6 (0.890)

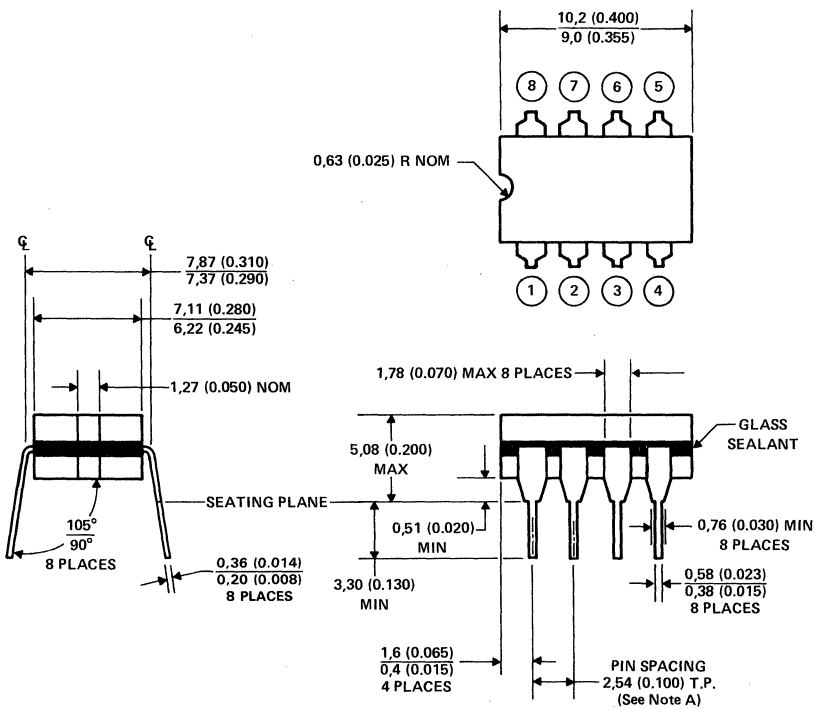
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

JG ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and 8-lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers (see Note A). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Non-shiny tin-plated leads require no additional cleaning or processing when used in soldered assembly.

8-PIN JG CERAMIC



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

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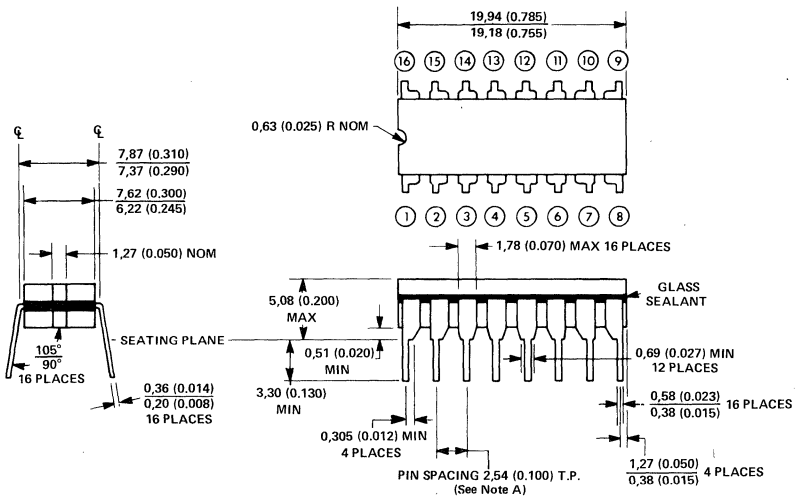
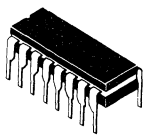
J ceramic packages

Each of these hermetically sealed dual-in-line packages consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The packages are intended for insertion in mounting-hole rows on 7,62 (0.300) or 15,24 (0.600) centers. Once the leads are compressed and inserted sufficient tension is provided to secure the package in the board during soldering. Tin-plated (''bright-dipped'') leads require no additional cleaning or processing when used in soldered assembly.

NOTE: For the 16-, and 20-pin packages, the letter J is used by itself since these packages are available only in the 7,62 (0.300) row spacing. For the 24-pin packages, if no second letter or row spacing is specified, the package is assumed to have 15,24 (0.600) row spacing.

16-PIN J CERAMIC

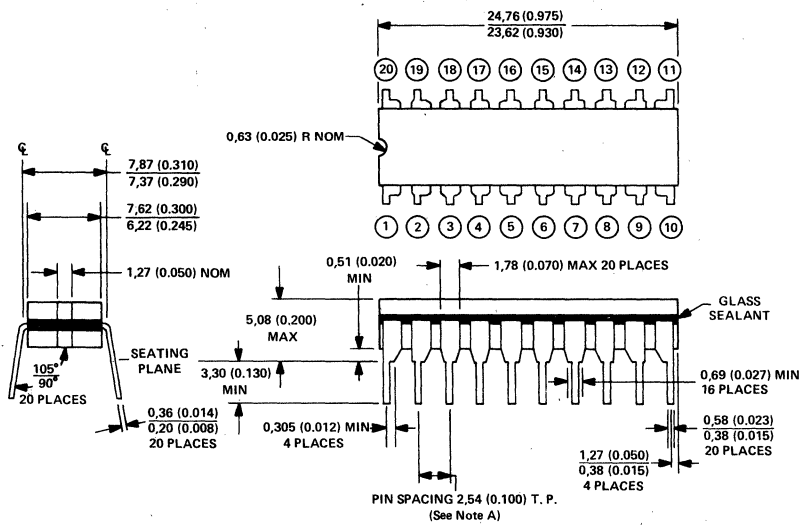


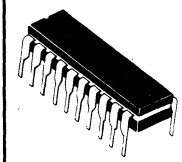


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

20-PIN J CERAMIC

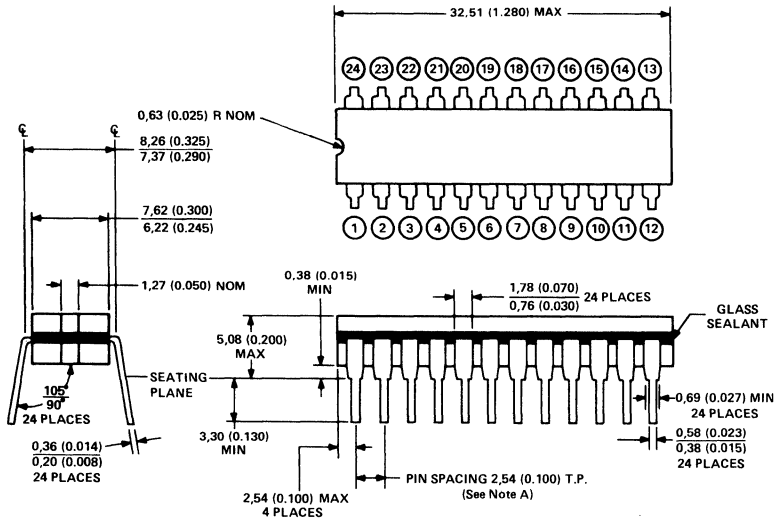




ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Each pin centerline is located with 0,25 (0.010) of its true longitudinal position.

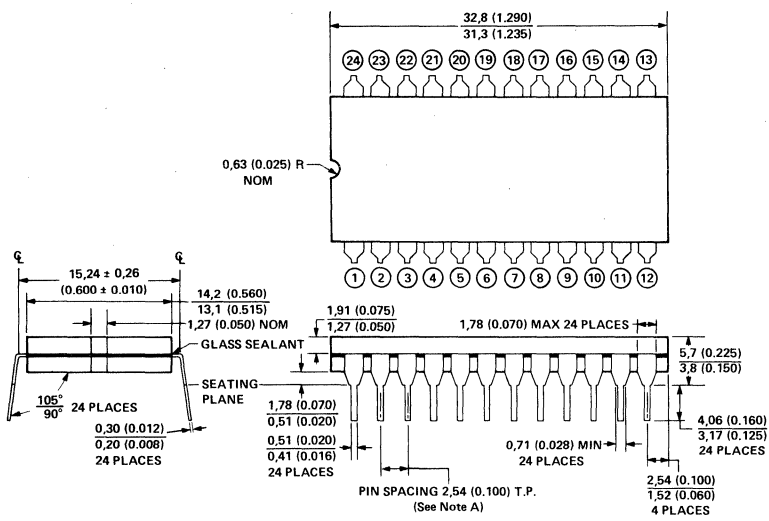
24-PIN JT CERAMIC, 0.300-INCH ROW SPACING

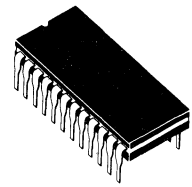


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

24-PIN JW CERAMIC





Falls within JEDEC MO-015AA dimensions

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

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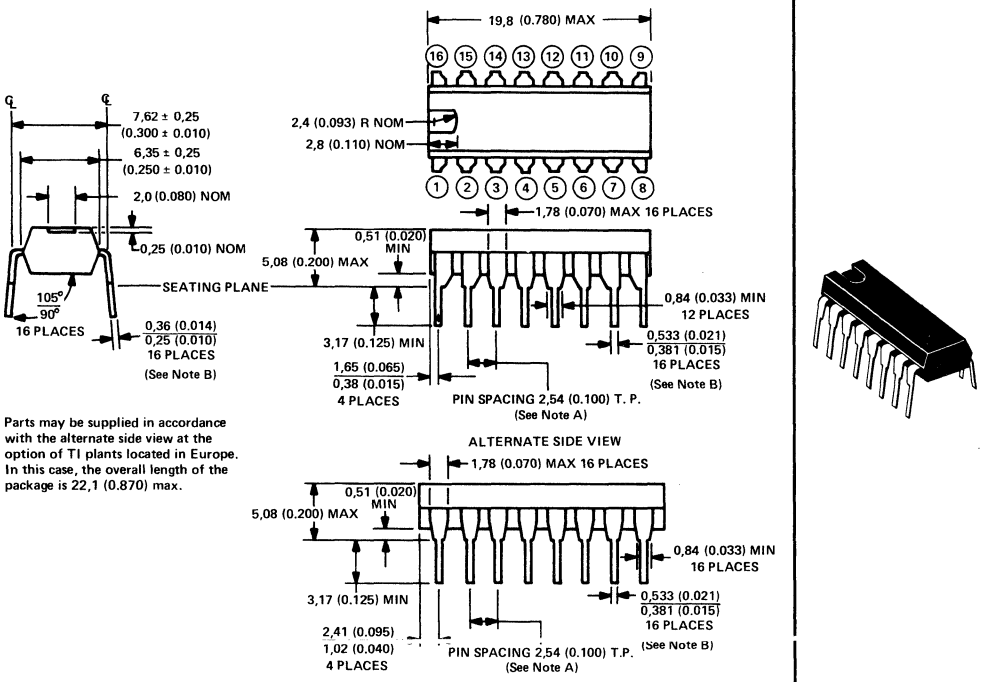
N plastic packages (including NT and NW dual-in-line packages)

Each of these dual-in-line packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remaining stable when operated in high-humidity conditions. The packages are intended for insertion in mounting-hole rows on 7,62 (0.300) centers for the N and NT packages and on 15,24 (0.600) centers for the NW packages. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

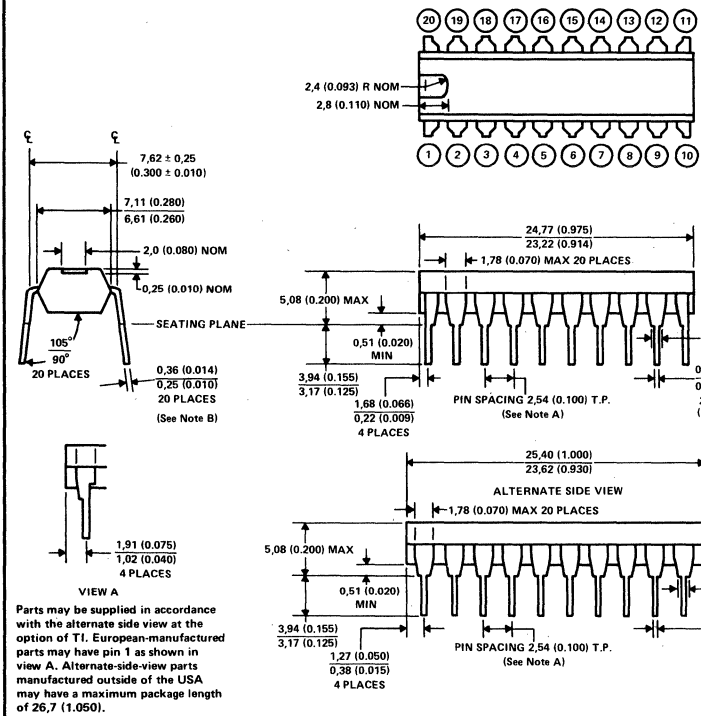
NOTE: For the 16- and 20- pin packages, the letter N is used by itself since these packages are available in only one row-spacing width — 7,63 (0.300). For 24-pin packages, the letters NT must be specified for 7,62 (0.300) row spacing or NW for 15,24 (0.600) row spacing. For the 28-pin thru 48-pin (NW) packages, if no second letter is specified, the package is assumed to have 15,24 (0.600) row spacing.

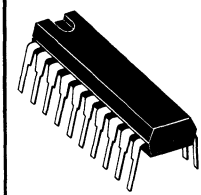
16-PIN N PLASTIC



NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

20-PIN N PLASTIC





Parts may be supplied in accordance with the alternate side view at the option of TI. European-manufactured parts may have pin 1 as shown in view A. Alternate-side-view parts manufactured outside of the USA may have a maximum package length of 26,7 (1.050).

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

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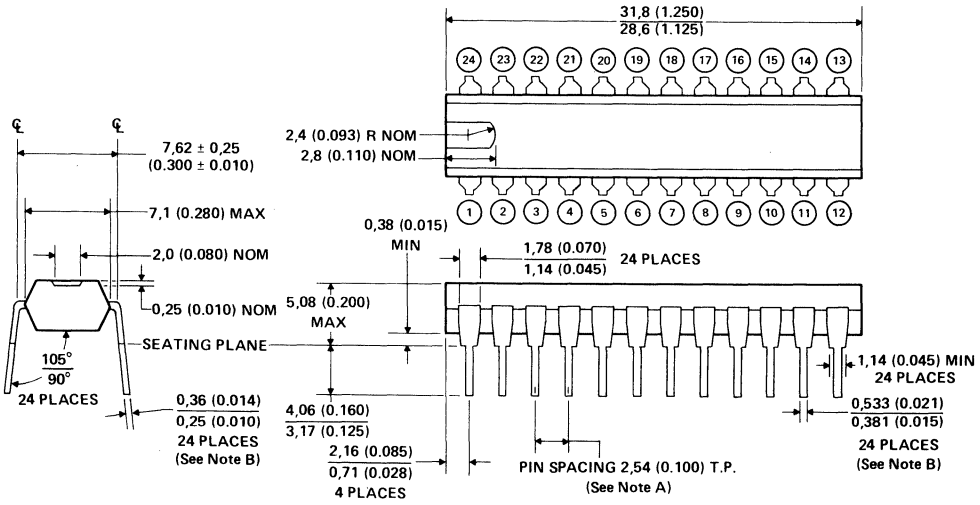
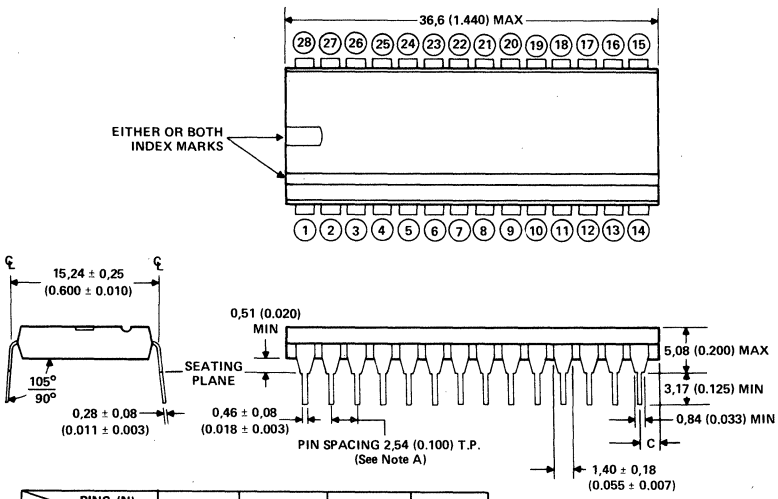
24-PIN NT PLASTIC, 0.300-INCH ROW SPACING

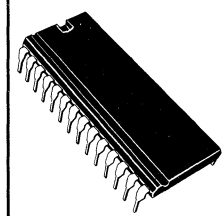


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

NW PLASTIC
(28-PIN PACKAGE SHOWN)





DIM \ PINS (N)	24	28	40	48
A ±0,25 (0.010)	15,24 (0.600)	15,24 (0.600)	15,24 (0.600)	15,24 0.600)
B (MAX)	32,8 (1.290)	36,6 (1.440)	53,1 (2.090)	62,2 (2.45)
C ±0,51 (0.020)	1,91 (0.075)	1,27 (0.050)	1,91 (0.075)	1,40 (0.055)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

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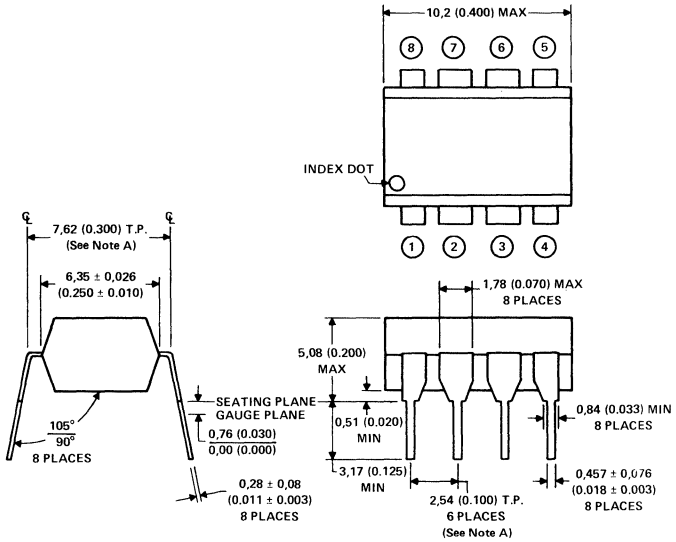
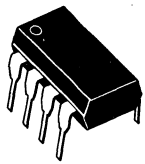
P plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on an 8-lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62-mm (0.300) centers (see Note A). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Solder-plated leads require no additional cleaning or processing when used in soldered assembly.

8-PIN P PLASTIC





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NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

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