SDAD001B

ALS/AS Logic Data Book

1986

Advanced Low-Power Schottky
Advanced Schottky

TEXAS INSTRUMENTS

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Specifications contained in this data book supersede all data for these products published by TI in the United States before May 1986.

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INTRODUCTION

The ALS/AS Logic Data Book presents pertinent technical information on Texas Instruments advanced families of TTL integrated circuits, Advanced Low-Power Schottky† (ALS), and Advanced Schottky† (AS). TI's ALS or AS functions provide the system design engineer with management tools to optimize system performance. Aggressive design goals can be achieved by utilizing ALS in noncritical paths and high-performance AS in speed critical paths.

The use of pin-for-pin compatible devices with the most popular LSTTL and STTL functions, existing TTL-based systems may be easily upgraded to ALS/AS to reduce system power requirements, enhance system performance, and improve overall system reliability. New system designs can capitalize on both the improved efficiency of the pin-compatible devices and the higher densities of the MSI/LSI series of devices unique to the ALS/AS family.

ALS and AS devices utilize an advanced wafer fabrication process that includes walled emitters, ion-implanted transistors, oxide isolations, and composed masks. This process is coupled with circuit design techniques to implement the following:

- improve input threshold and noise margins
- improve line driving and receiving
- maintain or increase drive capability
- tolerate ± 10% supply voltage swings
- take advantage of new packaging
  - 24-pin 300-mil DIP
  - plastic "Small Outline"
- specify ac parameters over the full operating temperature range

The ALS/AS family will grow to well over 400 devices through the end of 1986. Included among the new functions are:

- the fastest stand-alone 32-bit error detection and correction circuit (EDAC)
- high-performance 16 × 4 and 16 × 5 "zero-fall-through" FIFO (first in, first out) memory devices with 24-nanosecond fall through
- edge-triggered octal, 9-bit, and 10-bit read-back latches
- high-speed and low-power bus-transceivers with internal registers
- many additional pin-compatible ALS and AS devices

Also included in this book are several linear interface circuits that utilize the Advanced Low-Power Schottky† technology to provide a new linear interface family of devices with improved speed-power characteristics. The leadership functions are as follows:

- IBM 360/370 I/O Line Drivers
- IEEE-488 (GPIB) Octal Bus Transceivers
- RS-422-A Quad Line Drivers
- RS-422-A, RS-423-A, and RS-485 Quad Line Receivers

This data book provides a functional index of all bipolar digital, as well as, selected linear interface device types available or under development. Package dimensions given in the Mechanical Data section of this book are in metric measurement (and parenthetically in inches), which should simplify board layout for designers involved in metric conversion and new designs. The General Information section includes an explanation of the function tables, parameter measurement information, thermal information, D flip-flop and latch signal conventions, and typical characteristics related to the products listed in this volume.

Complete technical data for any Texas Instruments semiconductor/component product is available from your nearest TI field sales office, local authorized TI distributor, or by writing direct to:

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P.O. Box 655012, MS 308
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We sincerely believe that you will find the new ALS/AS Logic Data Book a meaningfull addition to your technical library.

†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U.S. Patent Number 3,463,975.

NUMERICAL INDEX

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INTRODUCTION

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

PART I — OPERATING CONDITIONS AND CHARACTERISTICS (IN SEQUENCE BY LETTER SYMBOLS)

f_{max} **Maximum clock frequency**
The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.

I_{CC} **Supply current**
The current into* the V_{CC} supply terminal of an integrated circuit.

I_{CCH} **Supply current, outputs high**
The current into* the V_{CC} supply terminal of an integrated circuit when all (or a specified number) of the outputs are at the high level.

I_{CCL} **Supply current, outputs low**
The current into* the V_{CC} supply terminal of an integrated circuit when all (or a specified number) of the outputs are at the low level.

I_{IH} **High-level input current**
The current into* an input when a high-level voltage is applied to that input.

I_{IL} **Low-level input current**
The current into* an input when a low-level voltage is applied to that input.

I_{OH} **High-level output current**
The current into* an output with input conditions applied that, according to the product specification, will establish a high level at the output.

I_{OL} **Low-level output current**
The current into* an output with input conditions applied that, according to the product specification, will establish a low level at the output.

I_{OS} **Short-circuit output current**
The current into* an output when that output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potential).

I_{OZH} **Off-state (high-impedance-state) output current (of a three-state output) with high-level voltage applied**
The current flowing into* an output having three-state capability with input conditions established that, according to the product specification, will establish the high-impedance state at the output and with a high-level voltage applied to the output.
NOTE: This parameter is measured with other input conditions established that would cause the output to be at a low level if it were enabled.

*Current out of a terminal is given as a negative value.

I_{OZL} **Off-state (high-impedance-state) output current (of a three-state output) with low-level voltage applied**
The current flowing into* an output having three-state capability with input conditions established that, according to the product specification, will establish the high-impedance state at the output and with a low-level voltage applied to the output.
NOTE: This parameter is measured with other input conditions established that would cause the output to be at a high level if it were enabled.

V_{IH} **High-level input voltage**
An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.
NOTE: A minimum is specified that is the least-positive value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{IK} **Input clamp voltage**
An input voltage in a region of relatively low differential resistance that serves to limit the input voltage swing.

V_{IL} **Low-level input voltage**
An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables.
NOTE: A maximum is specified that is the most-positive value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{OH} **High-level output voltage**
The voltage at an output terminal with input conditions applied that, according to the product specification, will establish a high level at the output.

V_{OL} **Low-level output voltage**
The voltage at an output terminal with input conditions applied that, according to the product specification, will establish a low level at the output.

t_a **Access time**
The time interval between the application of a specified input pulse and the availability of valid signals at an output.

t_{dis} **Disable time (of a three-state or open-collector output)**
The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from either of the defined active levels (high or low) to a high-impedance (off) state.
NOTE: For 3-state outputs, $t_{dis} = t_{PHZ}$ or t_{PLZ}. Open-collector outputs will change only if they are low at the time of disabling so $t_{dis} = t_{PLH}$.

t_{en} **Enable time (of a three-state or open-collector output)**
The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from a high-impedance (off) state to either of the defined active levels (high or low).
NOTE: In the case of memories, this is the access time from an enable input (e.g., $\overline{G}$). For 3-state outputs, $t_{en} = t_{PZH}$ or t_{PZL}. Open-collector outputs will change only if they are responding to data that would cause the output to go low so $t_{en} = t_{PHL}$.

*Current out of a terminal is given as a negative value.

t_h **Hold time**
The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.
NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is guaranteed.

t_{pd} **Propagation delay time**
The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level. (t_{pd} = t_{PHL} or t_{PLH}).

t_{PHL} **Propagation delay time, high-to-low-level output**
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

t_{PHZ} **Disable time (of a three-state output) from high level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined high level to a high-impedance (off) state.

t_{PLH} **Propagation delay time, low-to-high-level output**
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.

t_{PLZ} **Disable time (of a three-state output) from low level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined low level to a high-impedance (off) state.

t_{PZH} **Enable time (of a three-state output) to high level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined high level.

t_{PZL} **Enable time (of a three-state output) to low level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined low level.

t_{sr} **Sense recovery time**
The time interval needed to switch a memory from a write mode to a read mode and to obtain valid data signals at the output.

t_{su} **Setup time**
The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal.
NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

2. The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is guaranteed.

t_w **Pulse duration (width)**
The time interval between specified reference points on the leading and trailing edges of the pulse waveform.

PART II — CLASSIFICATION OF CIRCUIT COMPLEXITY

Gate Equivalent Circuit

A basic unit-of-measure of relative digital-circuit complexity. The number of gate equivalent circuits is that number of individual logic gates that would have to be interconnected to perform the same function.

Large-Scale Integration, LSI

A concept whereby a complete major subsystem or system function is fabricated as a single microcircuit. In this context a major subsystem or system, whether digital or linear, is considered to be one that contains 100 or more equivalent gates or circuitry of similar complexity.

Medium-Scale Integration, MSI

A concept whereby a complete subsystem or system function is fabricated as a single microcircuit. The subsystem or system is smaller than for LSI, but whether digital or linear, is considered to be one that contains 12 or more equivalent gates or circuitry of similar complexity.

Small-Scale Integration, SSI

Integrated circuits of less complexity than medium-scale integration (MSI).

Very-Large-Scale Integration, VLSI

The description of any IC technology that is much more complex than large-scale integration (LSI), and involves a much higher equivalent gate count. At this time an exact definition including a minimum gate count has not been standardized by JEDEC or the IEEE.

PART III — STRESS

Stress beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

The following symbols are used in function tables on TI data sheets:

H	=	high level (steady state)
L	=	low level (steady state)
↑	=	transition from low to high level
↓	=	transition from high to low level
→	=	value/level or resulting value/level is routed to indicated destination
↶	=	value/level is re-entered
X	=	irrelevant (any input, including transitions)
Z	=	off (high-impedance) state of a 3-state-output
a . . h	=	the level of steady-state inputs at inputs A through H respectively
Q_0	=	level of Q before the indicated steady-state input conditions were established
$\overline{Q}_0$	=	complement of Q_0 or level of $\overline{Q}$ before the indicated steady-state input conditions were established
Q_n	=	level of Q before the most recent active transition indicated by ↓ or ↑
⎍	=	one high-level pulse
⎏	=	one low-level pulse
TOGGLE	=	each output changes to the complement of its previous level on each active transition indicated by ↓ or ↑.

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with ↑ and/or ↓, this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, Q_0, or $\overline{Q}_0$), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output. (If the output is shown as a pulse, ⎍ or ⎏, the pulse follows the indicated input transition and persists for an interval dependent on the circuit.)

Among the most complex function tables in this book are those of the shift registers. These embody most of the symbols used in any of the function tables, plus more. Below is the function table of a 4-bit bidirectional universal shift register, e.g., type SN74194.

FUNCTION TABLE

INPUTS										OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D
	S1	S0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

The first line of the table represents a synchronous clearing of the register and says that if clear is low, all four outputs will be reset low regardless of the other inputs. In the following lines, clear is inactive (high) and so has no effect.

The second line shows that so long as the clock input remains low (while clear is high), no other input has any effect and the outputs maintain the levels they assumed before the steady-state combination of clear high and clock low was established. Since on other lines of the table only the rising transition of the clock is shown to be active, the second line implicitly shows that no further change in the outputs will occur while the clock remains high or on the high-to-low transition of the clock.

The third line of the table represents synchronous parallel loading of the register and says that if S1 and S0 are both high then, without regard to the serial input, the data entered at A will be at output Q_A, data entered at B will be at Q_B, and so forth, following a low-to-high clock transition.

The fourth and fifth lines represent the loading of high- and low-level data, respectively, from the shift-right serial input and the shifting of previously entered data one bit; data previously at Q_A is now at Q_B, the previous levels of Q_B and Q_C are now at Q_C and Q_D respectively, and the data previously at Q_D is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is low and S0 is high and the levels at inputs A through D have no effect.

The sixth and seventh lines represent the loading of high- and low-level data, respectively, from the shift-left serial input and the shifting of previously entered data one bit; data previously at Q_B is now at Q_A, the previous levels of Q_C and Q_D are now at Q_B and Q_C, respectively, and the data previously at Q_A is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is high and S0 is low and the levels at inputs A through D have no effect.

The last line shows that as long as both mode inputs are low, no other input has any effect and, as in the second line, the outputs maintain the levels they assumed before the steady-state combination of clear high and both mode inputs low was established.

The truth table functional tests do not reflect all possible combinations or sequential modes.

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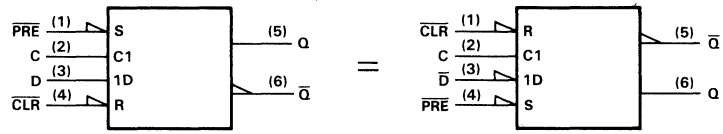
D flip-flop and latch signal conventions

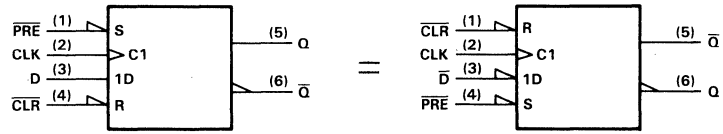
It is normal TI practice to name the outputs and other inputs of a D-type flip-flop or latch and to draw its logic symbol based on the assumption of true data (D) inputs. Outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called $\overline{Q}$. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called Preset (PRE). An input that causes a $\overline{Q}$ output to go high or a Q output to go low is called Clear (CLR). Bars are used over these pin names (PRE and CLR) if they are active-low.

The devices on several data sheets are second-source designs, and the pin-name conventions used by the original manufacturers have been retained. That makes it necessary to designate the inputs and outputs of the inverting circuits $\overline{D}$ and Q.

In some applications, it may be advantageous to redesignate the data input from D to $\overline{D}$ or vice versa. In that case, all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbols. Arbitrary pin numbers are shown in parentheses.



LATCH LATCH



FLIP-FLOP FLIP-FLOP

The figures show that when Q and $\overline{Q}$ exchange names, the Preset and Clear pins also exchange names. The polarity indicators (▷) on $\overline{PRE}$ and $\overline{CLR}$ remain, as these inputs are still active-low, but the presence or absence of the polarity indicator changes at D (or $\overline{D}$), Q, and $\overline{Q}$. Pin 5 (Q or $\overline{Q}$) is still in phase with the data input (D or $\overline{D}$); their active levels change together.

In digital system design, consideration must be given to thermal management of components. The small size of the "small outline" package makes this even more critical. Figure 1 shows the thermal resistance of these packages for various rates of air flow.

The thermal resistances in Figure 1 can be used to approximate typical and maximum virtual junction temperatures for the Advanced Low-Power Schottky (ALS) and Advanced Schottky (AS) families. In general, junction temperature for any device can be calculated using Equation 1.

JUNCTION-TO-AMBIENT THERMAL RESISTANCE
vs
AIR VELOCITY

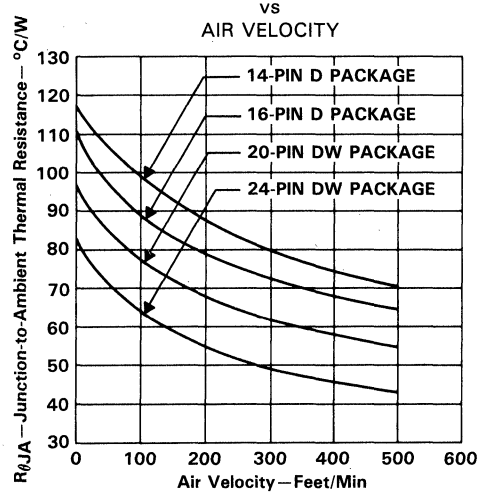


FIGURE 1

$$T_J = R_{\theta JA} (V_{CC} \cdot I_{CC} + N \cdot I_{OL} \cdot V_{OL}) + T_A \quad (1)$$

where

T_J = virtual junction temperature
$R_{\theta JA}$ = thermal resistance, junction to ambient air
V_{CC} = supply voltage (5 V for typical, 5.5 V for maximum)
I_{CC} = supply current
N = the number of outputs
I_{OL} = the low-level output current
V_{OL} = the low-level output voltage
T_A = the ambient air temperature

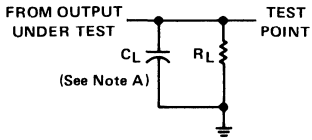
Typical junction temperature can be calculated using Equation 1 directly with typical values of I_{CC} taken from the data sheets and V_{CC} = 5 volts. To calculate maximum junction temperature, it is necessary to take into account the spread of I_{CC} values for a population. Due to different specification practices that have been followed, it is sometimes useful to use slightly different calculation procedures for the ALS and AS families.

Maximum junction temperature for all 54ALS, 54AS, and some 74ALS parts can be calculated using Equation 1 with I_{CC} being the maximum value specified on the data sheet and V_{CC} = 5.5 volts. In fact, I_{CC} for Series 54 devices at the temperature extremes of −55 °C to 125 °C will be higher than for a Series 74 device at the temperature extremes of 0 °C to 70 °C. This is reflected in the limits specified for some 74ALS devices, which are less than those specified for 54ALS devices. The AS family and most ALS family data sheets give a single maximum value for I_{CC}. If that value is used to calculate maximum junction temperature for series 74 devices, an unrealistically high value will result. Instead, Equation 2 can be used. This uses the factor 1.31 to scale the typical value of I_{CC} up to a practical maximum value for process variations and thermal effects.

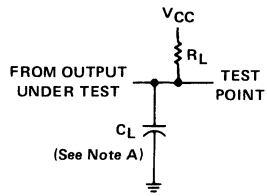
Thus, for 74AS and 74ALS devices if a lowered maximum I_{CC} has not been specified:

$$T_{Jmax} = R_{\theta JA} (5.5 \cdot 1.31 \cdot I_{CCtyp} + N \cdot I_{OL} \cdot V_{OL}) + T_A \quad (2)$$

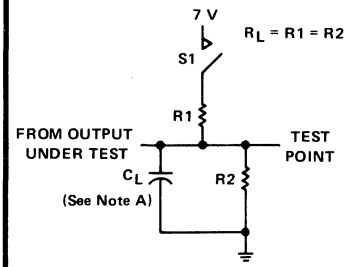
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



LOAD CIRCUIT FOR
BI-STATE
TOTEM-POLE OUTPUTS

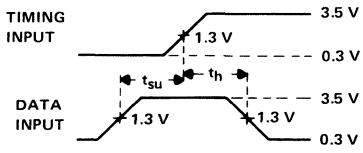


LOAD CIRCUIT FOR
OPEN-COLLECTOR OUTPUTS

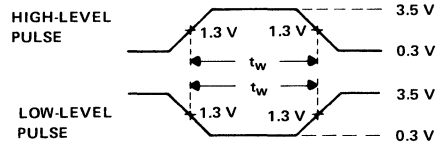


LOAD CIRCUIT FOR
THREE-STATE OUTPUTS

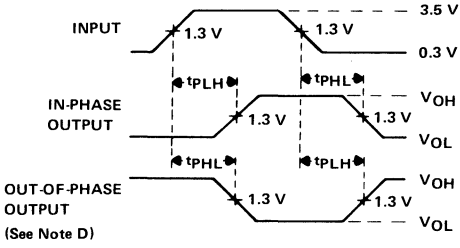
NOTE A: C_L includes probe and jig capacitance.



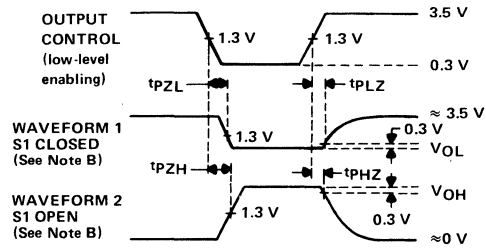
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f$ = 2 ns, duty cycle = 50%.
D. When measuring propagation delay items of 3-state outputs, switch S1 is open.
E. The outputs are measured one at a time with one input transition per measurement.

GATES AND INVERTERS

POSITIVE-NAND GATES AND INVERTERS

DESCRIPTION	TYPE	TECHNOLOGY							VOLUME
		STD TTL	ALS	AS	H	L	LS	S	
Hex 2-Input Gates	'804		A	B					3
Hex Inverters	'04	●			●	●	●	●	2
			A	●					3
	'1004		●	●					
Quadruple 2-Input Gates	'00	●			●	●	●	●	2
			A	●					3
	'1000		A	A					
Triple 3-Input Gates	'10	●			●	●	●	●	2
			A	●					3
	'1010		A						3
Dual 4-Input Gates	'20	●			●	●	●	●	2
			A	●					3
	'1020		A						
8-Input Gates	'30	●			●	●	●	●	2
			A	●					3
13-Input Gates	'133							●	2
			●						3
Dual 2-Input Gates	'8003		●						

POSITIVE-NAND GATES AND INVERTERS WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY							VOLUME
		STD TTL	ALS	AS	H	L	LS	S	
Hex Inverters	'05	●			●		●	●	2
			A						3
	'1005		●						
Quadruple 2-Input Gates	'01	●			●		●		2
			●						3
	'03	●				●	●	●	2
			B						3
	'1003		A						
Triple 3-Input Gates	'12	●					●		2
			A						3
Dual 4-Input Gates	'22	●			●		●	●	2
			B						3

POSITIVE-AND GATES

DESCRIPTION	TYPE	TECHNOLOGY							VOLUME
		STD TTL	ALS	AS	H	LS	S		
Hex 2-Input Gates	'808		A	B					3
Quadruple 2-Input Gates	'08	●				●	●		2
			●	●					3
	'1008		A	●					
Triple 3-Input Gates	'11				●	●	●		2
			A	●					3
	'1011		A						3
Dual 4-Input Gates	'21				●	●			2
			●	●					3

POSITIVE-AND GATES WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY						VOLUME
		STD TTL	ALS	AS	H	LS	S	
Quadruple 2-Input Gates	'09	●				●	●	2
			●					3
Triple 3-Input Gates	'15				●	●	●	2
			A					3

POSITIVE-OR GATES

DESCRIPTION	TYPE	TECHNOLOGY					VOLUME
		STD TTL	ALS	AS	LS	S	
Hex 2-Input Gates	'832		A	B			3
Quadruple 2-Input Gates	'32	●			●	●	2
			●	●			3
	'1032		A	●			

POSITIVE-NOR GATES

DESCRIPTION	TYPE	TECHNOLOGY						VOLUME
		STD TTL	ALS	AS	L	LS	S	
Hex 2-Input Gates	'805		A	B				3
Quadruple 2-Input Gates	'02	●			●	●	●	2
			●	●				3
	'1002		A					
Triple 3-Input Gates	'27	●				●		2
			●	●				3
Dual 4-Input Gates with Strobe	'25	●						2
Dual 5-Input Gates	'260						●	

SCHMITT-TRIGGER POSITIVE-NAND GATES AND INVERTERS

DESCRIPTION	TYPE	TECHNOLOGY					VOLUME
		STD TTL	ALS	AS	LS	S	
Hex Inverters	'14	●			●		2
	'19				●		
Octal Inverters	'619				●		
Dual 4-Input Positive-NAND	'13	●			●		
	'18				●		
Triple 4-Input Positive-NAND	'618				●		
Quadruple 2-Input Positive-NAND	'24				●		
	'132	●			●	●	

CURRENT-SENSING GATES

DESCRIPTION	TYPE	TECHNOLOGY			VOLUME
		ALS	AS	LS	
Hex	'63			●	2

DELAY ELEMENTS

DESCRIPTION	TYP	TECHNOLOGY			VOLUME
		ALS	AS	LS	
Inverting and Noninverting Elements, 2-Input NAND Buffers	'31			●	2

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GATES, EXPANDERS, BUFFERS, DRIVERS, AND TRANSCEIVERS

AND-OR-INVERT GATES

DESCRIPTION	TYPE	TECHNOLOGY							VOLUME
		STD TTL	ALS	AS	H	L	LS	S	
2-Wide 4-Input	'55				●	●	●		2
4-Wide 4-2-3-2 Input	'64							●	
4-Wide 2-2-3-2 Input	'54				●				
4-Wide 2-Input	'54	●							
4-Wide 2-3-3-2 Input	'54					●	●		
Dual 2-Wide 2-Input	'51	●			●	●	●	●	

AND-OR-INVERT GATES WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY				VOLUME
		STD TTL	ALS	AS	S	
4-Wide 4-2-3-2 Input	'65				●	2

EXPANDABLE GATES

DESCRIPTION	TYPE	TECHNOLOGY						VOLUME
		STD TTL	ALS	AS	H	L	LS	
Dual 4-Input Positive-NOR with Strobe	'23	●						2
4-Wide AND-OR	'52				●			
4-Wide AND-OR-INVERT	'53	●			●			
2-Wide AND-OR-INVERT	'55				●	●	●	
Dual 2-Wide AND-OR-INVERT	'50	●			●			

EXPANDERS

DESCRIPTION	TYPE	TECHNOLOGY				VOLUME
		STD TTL	ALS	AS	H	
Dual 4-Input	'60	●			●	2
Triple 3-Input	'61				●	
3-2-2-3 Input AND-OR	'62				●	

BUFFER AND INTERFACE GATES WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY					VOLUME
		STD TTL	ALS	AS	LS	S	
Hex	'07	●					2
	'17	●					
	'35		●				3
	'1035		●				3
Hex Inverter	'06	●					2
	'16	●					
	'1005		●				3
Quad 2-Input Positive-NAND	'26	●			●		2
	'38	●			●	●	2
			A				3
	'39	●					2
	'1003		A				3
Quad 2-Input Positive-NOR	'33	●			●		2
			A				3

BUFFERS, DRIVERS, AND BUS TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY					VOLUME
		STD TTL	ALS	AS	LS	S	
Noninverting	'757			●			3
Octal Buffers/Drivers	'760			●			
Inverting Octal Buffers/Drivers	'756			●			
	'763		●	●			
Inverting and Non-Inverting Octal Buffers/Drivers	'762		●	●			
Non-Inverting Quad Transceivers	'759			●			
Inverting Quad Transceivers	'758		●	●			

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GATES, EXPANDERS, BUFFERS, DRIVERS, AND TRANSCEIVERS

GATES, BUFFERS, DRIVERS, AND BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY					VOLUME
		STD TTL	ALS	AS	LS	S	
Noninverting 10-Bit Buffers/Drivers	'29827		●				LSI
Inverting 10-Bit Buffers/Drivers	'29828		●				
Noninverting 10-Bit Transceivers	'29861		●				
Inverting 10-Bit Transceivers	'29862		●				
Noninverting 9-Bit Transceivers	'29863		●				
Inverting 9-Bit Transceivers	'29864		●				
Noninverting Octal Buffers/Drivers	'241				●	●	2
			A	●			3
	'244				●	●	2
			A	●			3
	'465				●		2
			A				3
	'467				●		2
			A				3
	'541				●		2
			●				
	'1244¶		A				3
Inverting Octal Buffers/Drivers	'231		●	●			
	'240				●	●	2
			A	●			3
	'466				●		2
			A				3
	'468				●		2
			A				3
	'540				●		2
			●				3
	'1240¶		●				
Inverting and Noninverting Octal Buffers/Drivers	'230			●			3
Octal Transceivers	'245				●		2
			A	●			3
	'1245		A				
Noninverting Hex Buffers/Drivers	'365	A			A		2
	'367	A			A		2
Inverting Hex Buffers/Drivers	'366	A			A		2
	'368	A			A		2
Quad Buffers/Drivers with Independent Output Controls	'125	●			A		2
	'126	●			A		
	'425	●					
	'426	●					
Noninverting Quad Transceivers	'243				●		3
			A	●			
Inverting Quad Transceivers	'242				●		2
			A	●			3
	'1242¶		●				
Quad Transceivers with Storage	'226					●	2
12-Input NAND Gate	'134					●	

50-OHM/75-OHM LINE DRIVERS

DESCRIPTION	TYPE	TECHNOLOGY				VOLUME
		STD TTL	ALS	AS	S	
Hex 2-Input Positive-NAND	'804		A	B		3
Hex 2-Input Positive-NOR	'805		A	B		
Hex 2-Input Positive-AND	'808		A	B		
Hex 2-Input Positive-OR	'832		A	B		
Quad 2-Input Positive-NOR	'128	●				2
Dual 4-Input Positive-NAND	'140				●	

● Denotes available technology.
¶ Denotes very low power.
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BUFFERS, DRIVERS, TRANSCEIVERS, AND CLOCK GENERATORS

BUFFERS, CLOCK/MEMORY DRIVERS

DESCRIPTION	TYPE	TECHNOLOGY						VOLUME
		STD TTL	ALS	AS	H	LS	S	
Hex 2-Input Positive-NAND	'804		A	B				3
Hex 2-Input Positive-NOR	'805		A	B				
Hex 2-Input Positive-AND	'808		A	B				
Hex 2-Input Positive-OR	'832		A	B				
Hex Inverter	'1004		●	●				
Hex Buffer	'34		●	●				
	'1034		●	A				
Quad 2-Input Positive-NAND	'37	●				●	●	2
			A					3
	'1000		A	●				
Quad 2-Input Positive-NOR	'28	●				●		2
			A					3
	'1002		A					
	'1036			A				
Quad 2-Input Positive-AND	'1008		A	●				
Quad 2-Input Positive-OR	'1032		A	●				
Triple 3-Input Positive-NAND	'1010		A					
Triple 3-Input Positive-AND	'1011		A					
Dual 4-Input Positive-NAND	'40	●			●	●	●	2
			A					3
	'1020		A					
Line Driver/Memory Driver with Series Damping Resistor	'436						●	2
Line Driver/Memory Driver	'437						●	

BI-/TRI-DIRECTIONAL BUS TRANSCEIVERS AND DRIVERS

DESCRIPTION	TYPE OF OUTPUT	TYPE	TECHNOLOGY				VOLUME
			ALS	AS	LS	S	
Quad with Bit Direction	3-State	'446			●		2
Controls	3-State	'449			●		
Quad Tridirection	OC	'440			●		
	OC	'441			●		
	3-State	'442			●		
	3-State	'443			●		
	3-State	'444			●		
	OC	'448			●		
4-Bit with Storage	3-State	'226				●	

OCTAL BUS TRANSCEIVERS/MOS DRIVERS

DESCRIPTION	TYPE	TECHNOLOGY					VOLUME
		STD TTL	ALS	AS	LS	S	
Inverting Outputs, 3-State	'2620			●			3
	'2640			●			
True Outputs, 3-State	'2623			●			
	'2645			●			

OCTAL BUFFERS AND LINE DRIVERS WITH INPUT/OUTPUT RESISTORS

DESCRIPTION		TYPE	TECHNOLOGY					VOLUME
			STD TTL	ALS	AS	LS	S	
Input Resistors	Inverting Outputs	'746		●				3
	Noninverting Outputs	'747		●				
Output Resistors	Inverting Outputs	'2540		●				
	Noninverting Outputs	'2541		●				

OCTAL BI-/TRI-DIRECTIONAL BUS TRANSCEIVERS

DESCRIPTION		TYPE OF OUTPUT	TYPE	TECHNOLOGY			VOLUME
				ALS	AS	LS	
12 mA/24 mA/48 mA/64 mA Sink, True Outputs	Low Power	3-State	'245	A	●		3
						●	2
		OC	'621	A	●		3
						●	2
		3-State	'623	A	●		3
						●	2
		OC, 3-State	'639	A	●		3
						●	2
		3-State	'652	●	●		3 & LSI
						●	2
		OC, 3-State	'654	▲			3
						●	2
12 mA/24 mA/48 mA/64 mA Sink, Inverting Outputs	Low Power	3-State	'620	A	●		3
						●	2
		OC	'622	A	●		3
						●	2
		OC, 3-State	'638	A	●		3
						●	2
		3-State	'651	●	●		3 & LSI
						●	2
		OC, 3-State	'653	▲			3
						●	2
12 mA/24 mA/48 mA/64 mA Sink, True Outputs	Low Power	OC	'641	A	●		
						●	2
		3-State	'645	A	●		3
						●	2
	Very Low Power	3-State	'1645	A			3
12 mA/24 mA/48 mA/64 mA Sink, Inverting Outputs	Low Power	3-State	'640	A	●		
						●	2
		OC	'642	A	●		3
						●	2
	Very Low Power	3-State	'1640	A			3
12 mA/24 mA/48 mA/64 mA Sink, True and Inverting Outputs	Low Power	3-State	'643	A	●		
						●	2
		OC	'644	A	●		3
						●	2
Registered with Multiplex 12 mA/24 mA/48 mA/64 mA True Outputs		3-State	'646	●	●		3 & LSI
						●	2
		OC	'647	●			3
						●	2
Registered with Multiplexed 12 mA/24 mA/48 mA/64 mA Inverting Outputs		3-State	'648	●	●		3 & LSI
						●	2
		OC	'649	●			3 & LSI
						●	2
Universal Transceiver/ Port Controllers		3-State	'877		●		3 & LSI
			'852		●		
			'856		●		

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FLIP-FLOPS

DUAL AND SINGLE FLIP-FLOPS

DESCRIPTION	TYPE	TECHNOLOGY							VOLUME
		STD TTL	ALS	AS	H	L	LS	S	
Dual J-K Edge-Triggered	'73	●			●	●	A		2
	'76						A		
	'78				●	●	A		
	'103				●				
	'106				●				
	'107	●					A		
	'108				●				
	'109	●					A		
			A	●					3
	'112						A	●	2
			A						3
	'113						A	●	2
			A						3
	'114						A	●	2
			A						3
Single J-K Edge-Triggered	'70	●							2
	'101				●				
	'102				●				
Dual Pulse-Triggered	'73	●			●	●			
	'76	●			●				
	'78				●	●			
	'107	●							
Single Pulse-Triggered	'71				●	●			
	'72	●			●	●			
	'104	●							
	'105	●							
Dual J-K with Data Lockout	'111	●							
Single J-K with Data Lockout	'110	●							
Dual D-Type	'74	●			●	●	A	●	
			A	●					3

QUAD AND HEX FLIP-FLOPS

DESCRIPTION	NO. OF FFs	OUTPUTS	TYPE	TECHNOLOGY					VOLUME
				STD TTL	ALS	AS	LS	S	
D Type	6	Q	'174	●			●	●	2
					●	●			3
			'378				●		
	4	Q, $\overline{Q}$	'171				●		2
			'175	●			●	●	
					●	A			3
			'379				●		2
J-K	4	Q	'276	●					
			'376	●					

OCTAL, 9-BIT, AND 10-BIT D-TYPE FLIP-FLOPS

DESCRIPTION	NO. OF BITS	OUTPUT	TYPE	TECHNOLOGY					VOLUME
				STD TTL	ALS	AS	LS	S	
True Data	Octal	3-State	'374		●	●			3
							●	●	2
		3-State	'574		B	●			3
True Data with Clear	Octal	2-State	'273		●				
				●			●		2
		3-State	'575		●	●			3
		3-State	'874		●	●			
		3-State	'878		●	●			
True with Enable	Octal	2-State	'377				●		2
Inverting	Octal	3-State	'534		●	●			3
		3-State	'564		A				
		3-State	'576		A	●			
Inverting with Clear	Octal	3-State	'577		A	●			
		3-State	'879		A	●			
Inverting with Preset	Octal	3-State	'876		A	●			
True	Octal	3-State	'825			●			3 & LSI
Inverting	Octal	3-State	'826			●			
True	9-Bit	3-State	'823			●			
Inverting	9-Bit	3-State	'824			●			
True	10-Bit	3-State	'821			●			
Inverting	10-Bit	3-State	'822			●			
True	Octal	3-State	'29825		▲	▲			
Inverting	Octal	3-State	'29826		▲	▲			
True	9-Bit	3-State	'29823		▲	▲			
Inverting	9-Bit	3-State	'29824		▲	▲			
True	10-Bit	3-State	'29821		▲	▲			
Inverting	10-Bit	3-State	'29822		▲	▲			

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LATCHES AND MULTIVIBRATORS

QUAD LATCHES

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY					VOLUME
			STD TTL	ALS	AS	L	LS	
Dual 2-Bit Transparent	2-State	'75	●			●	●	2
	2-State	'77	●			●	●	
	2-State	'375					●	
S-R	2-State	'279	●				A	

RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

DESCRIPTION	TYPE	TECHNOLOGY					VOLUME
		STD TTL	ALS	AS	LS	L	
Single	'122	●			●	●	2
	'130	●					
	'422				●		
Dual	'123	●			●	●	
	'423				●		

D-TYPE OCTAL, 9-BIT, AND 10-BIT READ-BACK LATCHES

DESCRIPTION	NO. OF BITS	TYPE	TECHNOLOGY					VOLUME
			STD TTL	ALS	AS	LS	S	
Edge-Triggered Inverting and Noninverting	Octal	'996		●				3 & LSI
Transparent True	Octal	'990		●				
	9-Bit	'992		●				
	10-Bit	'994		●				
Transparent Noninverting	Octal	'991		●				
	9-Bit	'992		●				
	10-Bit	'994		●				
Transparent with Clear True Outputs	Octal	'666		●				
Transparent with Clear Inverting Outputs	Octal	'667		●				

OCTAL, 9-BIT, AND 10-BIT LATCHES

DESCRIPTION	NO. OF BITS	OUTPUT	TYPE	TECHNOLOGY					VOLUME
				STD TTL	ALS	AS	LS	S	
Transparent	Octal	3-State	'268					●	2
			'373				●	●	
					●	●			3
		3-State	'573		●	●			
Dual 4-Bit Transparent	Octal	2-State	'100	●					2
		2-State	'116	●					
		3-State	'873		B	●			3
Inverting Transparent	Octal	3-State	'533		●	●			
		3-State	'563		A				
		3-State	'580		A	●			
Dual 4-Bit Inverting Transparent	Octal	3-State	'880		A	●			
2-Input Multiplexed	Octal	3-State	'604				●		2
		OC	'605				●		
		3-State	'606				●		
		OC	'607				●		
Addressable	Octal	2-State	'259	●			●		
					●				3
Multi-Mode Buffered	Octal	3-State	'412					●	2
True	Octal	3-State	'845		●	●			3 & LSI
Inverting	Octal	3-State	'846		●	●			
True	9-Bit	3-State	'843		●	●			
Inverting	9-Bit	3-State	'844		●	●			
True	10-Bit	3-State	'841		●	●			
Inverting	10-Bit	3-State	'842		●	●			
True	Octal	3-State	'29845		●	●			3
Inverting	Octal	3-State	'29846		●	●			
True	9-Bit	3-State	'29843		●	●			
Inverting	9-Bit	3-State	'29844		●	●			
True	10-Bit	3-State	'29841		●	●			
Inverting	10-Bit	3-State	'29842		●	●			

MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

DESCRIPTION	TYPE	TECHNOLOGY						VOLUME
		STD TTL	ALS	AS	LS	S	L	
Single	'121	●					●	2
Dual	'221	●			●			

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REGISTERS

SHIFT REGISTERS

DESCRIPTION	NO. OF BITS	MODES				TYPE	TECHNOLOGY						VOLUME
		S-R	S-L	LOAD	HOLD		STD TTL	ALS	AS	L	LS	S	
Sign-Protected		X		X	X	'322					A		2
Parallel-In Parallel-Out	8	X	X	X	X	'198	●				●	●	2
		X	X	X	X	'299		●	▲				3
Bidirectional		X	X	X	X	'323					●		2
								●	▲				3
	4	X	X	X	X	'194	●				A	●	2
									▲				3
Parallel-In, Parallel-Out, Registered Outputs	4	X	X	X	X	'671					●		2
		X	X	X	X	'672					●		
Parallel-In, Parallel-Out	8	X		X	X	'199	●						2
	5	X		X		'96	●			●	●		
	4	X		X		'95	A			●	B		2
									▲				3
		X		X		'99				●			2
		X		X	X	'178	●						
		X		X	X	'179	●						
		X		X		'195	●				A	●	2
									▲				3
		X		X		'295					B		2
		X		X		'395					A		2
Serial-In Parallel-Out	16	X		X	X	'673					●		2
	8	X				'164	●			●	●		2
								▲					3
Parallel-In, Serial-Out	16	X		X	X	'674					●		2
	8	X		X	X	'165	●				A		2
								▲					3
		X		X	X	'166	●				A		2
								▲					3
Serial-In, Serial-Out	8	X				'91	A			●	●		2
	4	X		X		'94	●						

SHIFT REGISTERS WITH LATCHES

DESCRIPTION	NO. OF BITS	OUTPUTS	TYPE	TECHNOLOGY			VOLUME
				ALS	AS	LS	
Parallel-In, Parallel-Out with Output Latches	4	3-State	'671			●	2
		3-State	'672			●	
Serial-In, Parallel-Out with Output Latches	16	2-State	'673			●	
	8	Buffered	'594			●	
		3-State	'595			●	
		OC	'596			●	
		OC	'599			●	
Parallel-In, Serial-Out, with Input Latches	8	2-State	'597			●	
		3-State	'599			●	
Parallel I/O Ports with Input Latches, Multiplexed Serial Inputs	8	3-State	'598			●	

SIGN-PROTECTED REGISTERS

DESCRIPTION	NO. OF BITS	MODES				TYPE	TECHNOLOGY			VOLUME
		S-R	S-L	LOAD	HOLD		ALS	AS	LS	
Sign-Protected Register	8	X		X	X	'322			A	2

REGISTER FILES

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY				VOLUME
			STD TTL	ALS	AS	LS	
8 Words × 2 Bits	3-State	'172	●				2
4 Words × 4 Bits	OC	'170	●			●	
	3-State	'670				●	
Dual 16 Words × 4 Bits	3-State	'870			●		3 & LSI
	3-State	'871			●		
64 Words × 40 Bits	3-State	'8834			▲		LSI

OTHER REGISTERS

DESCRIPTION	TYPE	TECHNOLOGY						VOLUME
		STD TTL	ALS	AS	L	LS	S	
Quadruple Multiplexers with Storage	'98				●			2
	'298	●				●		
	'398			●				3
	'399				●			2
8-Bit Universal Shift Registers	'299					●	●	
			●	▲				3
Quadruple Bus-Buffer Registers	'173	●				A		2
Octal Storage Register	'396					●		
Dual-Rank 8-Bit Shift Registers	'963		▲					3 & LSI
	'964		▲					
8-Bit Diagnostics/ Pipeline Registers	'29818		●					
	'819		▲					

● Denotes available technology.
▲ Denotes planned new products.
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B Denotes "B" suffix version available in the technology indicated.

COUNTERS

SYNCHRONOUS COUNTERS — POSITIVE-EDGE TRIGGERED

DESCRIPTION	PARALLEL LOAD	TYPE	TECHNOLOGY						VOLUME
			STD TTL	ALS	AS	L	LS	S	
Decade	Sync	'160	●				A		2
				B	●				3
	Sync	'162	●				A	●	2
				B	●				3
	Sync	'560		A					
	Sync	'668					●		2
	Sync	'690					●		
	Sync	'692					●		
Decade Up/Down	Sync	'168					B	●	2
				B	●				3
	Async	'190	●				●		2
				●					3
	Async	'192	●			●	●		2
				●					3
	Sync	'568		A					
	Sync	'696					●		2
	Sync	'698					●		
Decade Rate Multipler, $\frac{1}{N10}$	Async Set-to-9	'167	●						2
4-Bit Binary	Sync	'161	●				A		2
				B	●				3
	Sync	'163	●				A	●	2
				B	●				3
	Sync	'561		A					
	Sync	'669					●		2
	Sync	'691					●		
	Sync	'693					●		
4-Bit Binary Up/Down	Sync	'169					B	●	2
				B	●				3
	Async	'191	●				●		2
				●					3
	Async	'193	●			●	●		2
				●					3
	Sync	'569		A					
	Sync	'697					●		2
	Sync	'699					●		
6-Bit Binary Rate Multipler, $\frac{1}{N2}$		'97	●						2
8-Bit Up/Down	Async CLR	'867			●				3 & LSI
	Sync CLR	'869			●				

ASYNCHRONOUS COUNTERS (RIPPLE CLOCK) — NEGATIVE-EDGE TRIGGERED

DESCRIPTION	PARALLEL LOAD	TYPE	TECHNOLOGY						VOLUME
			STD TTL	ALS	AS	L	LS	S	
Decade	Set-to-9	'90	A			●	●		2
		'68					●		
	Yes	'176	●						
	Yes	'196	●				●	●	
	Set-to-9	'290	●				●		
4-Bit Binary	None	'93	A			●	●		
		'69					●		
	Yes	'177	●						
	Yes	'197	●				●	●	
	None	'293	●				●		
Divide-by-12	None	'92	A				●		
Dual Decade	None	'390	●				●		
	Set-to-9	'490	●				●		
Dual 4-Bit Binary	None	'393	●				●		

8-BIT BINARY COUNTERS WITH REGISTERS

DESCRIPTION	TYPE OF OUTPUT	TYPE	TECHNOLOGY			VOLUME
			ALS	AS	LS	
Parallel Register	3-State	'590			●	2
Outputs	OC	'591			●	
Parallel Register Inputs	2-State	'592			●	
Parallel I/O	3-State	'593			●	

FREQUENCY DIVIDERS, RATE MULTIPLIERS

DESCRIPTION	TYPE	TECHNOLOGY				VOLUME
		STD TTL	ALS	AS	LS	
50-to-1 Frequency Divider	'56				●	2
60-to-1 Frequency Divider	'57				●	
60-Bit Binary Rate Multiplier	'97	●				
Decade Rate Multiplier	'167	●				

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TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

DECODERS, ENCODERS, DATA SELECTORS/MULTIPLEXERS AND SHIFTERS

DATA SELECTORS/MULTIPLEXERS

DESCRIPTION	TYPE OF OUTPUT	TYPE	TECHNOLOGY						VOLUME
			STD TTL	ALS	AS	L	LS	S	
16-to-1	2-State	'150	●						2
	3-State	'250			●				3 & LSI
	3-State	'850			●				
	3-State	'851			●				
Dual 8-to-1	3-State	'351	●						2
8-to-1	2-State	'151	A				●	●	
				●	●				3
	2-State	'152	A				●		2
	3-State	'251	●				●	●	
				●	▲				3
	3-State	'354					●		2
	2-State	'355					●		
	3-State	'356					●		
	OC	'357					●		
Dual 4-to-1	2-State	'153	●			●	●	●	
				●	●				3
	3-State	'253					●	●	2
				●	●				3
	2-State	'352					●		2
				●	●				3
	3-State	'353					●		2
				●	A				3
Octal 2-to-1 with Storage	3-State	'604					●		2
	OC	'605					●		
	3-State	'606					●		
	OC	'607					●		
Quad 2-to-1 with Storage	2-State	'98				●			2
	2-State	'298	●				●		
					●				3
	2-State	'398					●		2
	2-State	'399					●		
Quad 2-to-1	2-State	'157	●			●	●	●	
				●	●				3
	2-State	'158					●	●	2
				●	●				3
	3-State	'257					B	●	2
				A	●				3
	3-State	'258					B	●	2
				A	●				3
6-to-1 Universal Multiplexer	3-State	'857		●	●				3

DECODERS/DEMULTIPLEXERS

DESCRIPTION	TYPE OF OUTPUT	TYPE	TECHNOLOGY						VOLUME
			STD TTL	ALS	AS	L	LS	S	
4-to-16	3-State	'154	●			●			2
	OC	'159	●						
4-to-10 BCD-to-Decimal	2-State	'42	A			●	●		
4-to-10 Excess 3-to-Decimal	2-State	'43	A			●			
4-to-10 Excess 3-Gray-to-Decimal	2-State	'44	A			●			
3-to-8 with Address Latches	2-State	'131		●	A				3
		'137		●	●				
3-to-8	2-State	'138		●	●		●		2
							●	●	3
Dual 2-to-4	2-State	'139		●	▲				
							A	●	2
	2-State	'155	●				A		
	OC	'156	●				●		

CODE CONVERTERS

DESCRIPTION	TYPE	TECHNOLOGY		VOLUME
		STD TTL	S	
6-Line-BCD to 6-Line Binary, or 4-Line to 4-Line BCD 9's/BCD 10's Converters	'184	●		2
6-Bit-Binary to 6-Bit BCD Converters	'185	A		
BCD-to-Binary Converters	'484		A	4
Binary-to-BCD Converters	'485		A	

PRIORITY ENCODERS/REGISTERS

DESCRIPTION	TYPE	TECHNOLOGY				VOLUME
		STD TTL	ALS	AS	LS	
Full BCD	'147	●			●	2
Cascadable Octal	'148	●			●	
Cascadable Octal with 3-State Outputs	'348				●	
4-Bit Cascadable with Registers	'278	●				

SHIFTERS

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY						VOLUME
			STD TTL	ALS	AS	L	LS	S	
4-Bit Shifter	3-State	'350						●	2
Parallel 16-Bit Multi-Mode Barrel Shifter	3-State	'897			●				LSI
32-Bit Barrel Shifter	3-State	'8838			●				

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DISPLAY DECODERS/DRIVERS, MEMODRY/MICROPROCESSOR CONTROLLERS, AND VOLTAGE-CONTROLLED OSCILLATORS

OPEN-COLLECTOR DISPLAY DECODERS/DRIVERS

DESCRIPTION	OFF-STATE OUTPUT VOLTAGE	TYPE	TECHNOLOGY					VOLUME
			STD TTL	ALS	AS	L	LS	
BCD-to-Decimal	30 V	'45	●					2
	60 V	'141	●					
	15 V	'145	●				●	
	7 V	'445					●	
BCD-to-Seven-Segment	30 V	'46	A			●		
	15 V	'47	A			●	●	
	5.5 V	'48	●				●	
	5.5 V	'49	●				●	
	30 V	'246	●					
	15 V	'247	●				●	
	7 V	'347					●	
	7 V	'447					●	
	5.5 V	'248	●				●	
	5.5 V	'249	●				●	

MEMORY/MICROPROCESSOR CONTROLLERS

DESCRIPTION			TYPE	TECHNOLOGY				VOLUME
				ALS	AS	LS	S	
System Controllers (Universal or for '888)			'890		●			LSI
Memory Refresh Controllers	Transparent, Burst Modes	4K, 16K	'600			A		2
		64K	'601			A		
	Cycle Steal, Burst Modes	4K, 16K	'602			A		
		64K	'603			A		
Memory Cycle Controller			'608			●		
Memory Mappers		3-State	'612			●		LSI
		OC	'613			●		
Memory Mappers with Output Latches		3-State	'610			●		
		OC	'611			●		
Multi-Mode Latches (8080A Applications)			'412				●	2
Dynamic Memory Controllers		16K, 64K, 256K	2967	▲				LSI
			'2968	▲				
		16K, 64K	'6301	▲				
		256K, 1 MEG	'6302	▲				

OPEN COLLECTOR DISPLAY DECODERS/DRIVERS WITH COUNTERS/LATCH

DESCRIPTION	TYPE	TECHNOLOGY			VOLUME
		STD TTL	ALS	AS	
BCD Counter/4-Bit Latch/BCD-to-Decimal Decoder/Driver	'142	●			2
BCD Counter/4-Bit Latch/BCD-to-Seven-Segment Decoder/LED Driver	'143	●			
BCD Counter/4-Bit Latch/BCD-to-Seven-Segment Decoder/Lamp Driver	'144	●			

CLOCK GENERATOR CIRCUITS

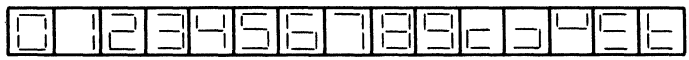
DESCRIPTION	TYPE	TECHNOLOGY					VOLUME
		STD TTL	ALS	AS	LS	S	
Quadruple Complementary-Output Logic Elements	'265	●					2
Dual Pulse Synchronizers/Drivers	'120	●					
Crystal-Controlled Oscillators	'320				●		
	'321				●		
Digital Phase-Lock Loop	'297				●		
Programmable Frequency Dividers/Digital Timers	'292				●		
	'294				●		
Dual VCO	'124					●	2

VOLTAGE-CONTROLLED OSCILLATORS

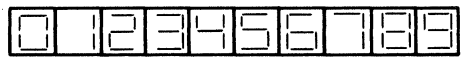
DESCRIPTION						TYPE	TECHNOLOGY		VOLUME
No. VCOs	COMP'L Z_{OUT}	ENABLE	RANGE INPUT	R_{ext}	f_{max} MHz		LS	S	
Single	Yes	Yes	Yes	No	20	'624	●		2
Single	Yes	Yes	Yes	Yes	20	'628	●		
Dual	No	Yes	Yes	No	60	'124		●	
Dual	Yes	Yes	No	No	20	'626	●		
Dual	No	No	No	No	20	'627	●		
Dual	No	Yes	Yes	No	20	'629	●		

RESULTANT DISPLAYS USING '46A, '47A, '48, '49, 'L46, 'L47, 'LS47, 'LS48, 'LS49, 'LS347

RESULTANT DISPLAYS USING '246, '247, '248, '249, 'LS247, 'LS248, 'LS249, 'LS447



RESULTANT DISPLAYS USING '143, '144



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TEXAS INSTRUMENTS
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COMPARATORS AND ERROR DETECTION CIRCUITS

4-BIT COMPARATORS

DESCRIPTION					TYPE	TECHNOLOGY						VOLUME
P=Q	P>Q	P<Q	OUTPUT	OUTPUT ENABLE		STD TTL	ALS	AS	L	LS	S	
Yes	Yes	No	2-State	No	'85	●			●	●	●	2

8-BIT COMPARATORS

DESCRIPTION								TYPE	TECHNOLOGY			VOLUME
INPUTS	P=Q	$\overline{P=Q}$	P>Q	$\overline{P>Q}$	P<Q	OUTPUT	OUTPUT ENABLE		ALS	AS	LS	
20-kΩ Pull-Up	Yes	No	No	No	No	OC	Yes	'518	●			3
	No	Yes	No	No	No	2-S	Yes	'520	●			
	No	Yes	No	No	No	OC	Yes	'522	●			
	No	Yes	No	Yes	No	2-S	No	'682			●	2
	No	Yes	No	Yes	No	OC	No	'683			●	
Standard	Yes	No	No	No	No	OC	Yes	'519	●			3
	No	Yes	No	No	No	2-S	Yes	'521	●			
	No	Yes	No	Yes	No	2-S	No	'684			●	2
	No	Yes	No	Yes	No	OC	No	'685			●	
	No	Yes	No	Yes	No	2-S	Yes	'686			●	
	No	Yes	No	Yes	No	OC	Yes	'687			●	
	No	Yes	No	No	No	2-S	Yes	'688	●			3
											●	2
	No	Yes	No	No	No	OC	Yes	'689	●			3
											●	2
Latched P Logic & Arith	No	No	Yes	No	Yes	2-S	Yes	'885		●		3 & LSI
Latched P&Q Logic & Arith	Yes	No	Yes	No	Yes	Latched	Yes	'866		●		3

ADDRESS COMPARATORS

DESCRIPTION	OUTPUT ENABLE	LATCHED OUTPUT	TYPE	TECHNOLOGY		VOLUME
				ALS	AS	
16-Bit to 4-Bit	Yes		'677	●		3
		Yes	'678	●		
12-Bit to 4-Bit	Yes		'679	●		
		Yes	'680	●		

PARITY GENERATORS/CHECKERS, ERROR DETECTION AND CORRECTION CIRCUITS

DESCRIPTION		NO. OF BITS	TYPE	TECHNOLOGY					VOLUME
				STD TTL	ALS	AS	LS	S	
Odd/Even Parity Generators/Checkers		8	'180	●					2
		9	'280				●	●	
					●	●			3 & LSI
		9	'286			●			
Parallel Error Detection/Correction Circuits	3-State	8	'636				●		2
	OC	8	'637				●		
	3-State	16	'616			●			3 & LSI
	OC	16	'617			▲			
	3-State	16	'630				●		2
	OC	16	'631				●		
	3-State	16	'8400		▲				LSI
	3-State	32	'632		A	▲			3 & LSI
	OC	32	'633		▲	▲			
	3-State	32	'634		●	▲			
	OC	32	'635		▲	▲			

FUSE-PROGRAMMABLE COMPARATORS

DESCRIPTION	TYPE	TECHNOLOGY					VOLUME
		STD TTL	ALS	AS	LS	S	
16-Bit Identity Comparator	'526		●				3
12-Bit identity Comparator	'528		●				
8-Bit Identity Comparator and 4-Bit Comparator	'527		●				

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ARITHMETIC CIRCUITS AND PROCESSOR ELEMENTS

PARALLEL BINARY ADDERS

DESCRIPTION	TYPE	TECHNOLOGY						VOLUME
		STD TTL	ALS	AS	H	LS	S	
1-Bit Gated	'80	●						2
2-Bit	'82	●						
4-Bit	'83	A				A		
	'283	●				●	●	
Dual 1-Bit Carry-Save	'183				●	●		

ACCUMULATORS, ARITHMETIC LOGIC UNITS, LOOK-AHEAD CARRY GENERATORS

DESCRIPTION		TYPE	TECHNOLOGY					VOLUME
			STD TTL	ALS	AS	LS	S	
4-Bit Parallel Binary Accumulators		'281					●	2
		'681				●		
4-Bit Arithmetic Logic Units/ Function Generators		'181	●			●	●	3 & LSI
					A			
		'1181			●			
		'381				A		2
							●	
		'881			A			3 & LSI
4-Bit Arithmetic Logic Unit with Ripple Carry		'382				●		2
Look-Ahead Carry Generators	16-Bit	'182	●				●	2
					▲			3
		'282			▲			
	32-Bit	'882			A			3 & LSI
Quad Serial Adder/Subtractor		'385				●		2

MULTIPLIERS

DESCRIPTION	TYPE	TECHNOLOGY					VOLUME
		STD TTL	ALS	AS	LS	S	
2-Bit-by-4-Bit Parallel Binary Multipliers	'261				●		2
4-Bit-by-4-Bit Parallel Binary Multipliers	'284	●					
	'285	●					
25-MHz 6-Bit Binary Rate Multipliers	'97	●					
25-MHz Decade Rate Multipliers	'167	●					
8-Bit × 1-Bit 2's Complement Multipliers	'384				●		

OTHER ARITHMETIC OPERATORS

DESCRIPTION	TYPE	TECHNOLOGY						VOLUME
		STD TTL	ALS	AS	H	L	LS	S	
Quad 2-Input Exclusive-OR Gates with Totem-Pole Outputs	'86	●				●	A	●	2
			●						3
	'386						A		2
Quad 2-Input Exclusive-OR Gates with Open-Collector Outputs	'136	●						●	
			●						3
Quad 2-Input Exclusive-NOR Gates	'266						●		2
	'810		●	▲					3
Quad 2-Input Exclusive-NOR Gates with Open-Collector Outputs	'811		●	▲					3
Quad Exclusive OR/NOR Gates	'135							●	2
4-Bit True/Complement Element	'87				●				

BIPOLAR BIT-SLICE PROCESSOR ELEMENTS

DESCRIPTION	CASCADABLE TO N-BITS	TYPE	TECHNOLOGY				VOLUME
			ALS	AS	LS	S	
8-Bit Slice	No	'887		●			LSI
	Yes	'888		●			
	Yes	'895		●			

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INTERFACE ALS CIRCUITS

All type numbers on this page refer to devices in the SN55ALS and SN75ALS families.

IBM 360/370 I/O LINE DRIVERS

DESCRIPTION	TYPE	TECHNOLOGY ALS	VOLUME
Quadruple Line Driver	'126	●	ALS/AS
Quadruple Line Driver	'130	●	ALS/AS

IEEE-488 (GPIB) INTERFACE BUS TRANSCEIVERS

DESCRIPTION	TYPE	TECHNOLOGY ALS	VOLUME
Octal Transceiver	'160	▲	ALS/AS
	'161	▲	
	'162	▲	
	'163	▲	
	'164	▲	
	'165	▲	

RS-422-A, RS-423-A, AND RS-485 LINE RECEIVERS

DESCRIPTION	TYPE	TECHNOLOGY ALS	VOLUME
Quad Differential with 3-State Outputs	'193	●	ALS/AS
Quad Differential with 3-State Outputs (TTL Comp.)	'195	●	ALS/AS

RS-422-A LINE DRIVERS

DESCRIPTION	TYPE	TECHNOLOGY ALS	VOLUME
Quad Differential	'192	●	ALS/AS
Quad Differential with 3-State Outputs	'194	●	ALS/AS

● Denotes available technology.
▲ Denotes planned new products.

MEMORIES

USER-PROGRAMMABLE READ-ONLY MEMORIES (PROMs)
STANDARD PROMs

DESCRIPTION	TYPE	ORGANIZATION	TYPE OUTPUT	S	VOLUME
16K-Bit Arrays	TBP28S166	2048W × 8B	3-State	●	4
	TBP38S165	2048W × 8B	3-State	●	
	TBP38S166	2048W × 8B	3-State	●	
	TBP38SA165	2048W × 8B	OC	●	
	TBP38SA166	2048W × 8B	OC	●	
	TBP34S162	4096W × 4B	3-State	●	
	TBP34SA162	4096W × 4B	OC	▲	
8K-Bit Arrays	TBP24S81	2048W × 4B	3-State	●	
	TBP24SA81	2048W × 4B	OC	●	
	TBP28S85A	1024W × 8B	3-State	▲	
	TBP28S86A	1024W × 8B	3-State	●	
	TBP28SA86A	1024W × 8B	OC	●	
	TBP38S85	1024W × 8B	3-State	▲	
	TBP38S86	1024W × 8B	3-State	▲	
	TBP38SA85	1024W × 8B	OC	▲	
	TBP38SA86	1024W × 8B	OC	▲	
4K-Bit Arrays	TBP24S41	1024W × 4B	3-State	●	
	TBP24SA41	1024W × 4B	OC	●	
	TBP28S42	512W × 8B	3-State	●	
	TBP28SA42	512W × 8B	OC	●	
	TBP28S46	512W × 8B	3-State	●	
	TBP28SA46	512W × 8B	OC	●	
2K-Bit Arrays	TBP38S22	256W × 8B	3-State	●	
	TBP38SA22	256W × 8B	OC	●	
1K-Bit Arrays	TBP24S10	256W × 4B	3-State	●	
	TBP24SA10	256W × 4B	OC	●	
	TBP34S10	256W × 4B	3-State	●	
	TBP34SA10	256W × 4B	OC	●	
256-Bit Arrays	TBP18S030	32W × 8B	3-State	●	
	TBP18SA030	32W × 8B	OC	●	
	TBP38S030	32W × 8B	3-State	●	
	TBP38SA030	32W × 8B	OC	●	

LOW-POWER PROMs

DESCRIPTION	TYPE	ORGANIZATION	TYPE OUTPUT	S	VOLUME
16K-Bit Arrays	TBP28L166	2048W × 8B	3-State	●	4
	TBP38L165	2048W × 8B	3-State	●	
	TBP38L166	2048W × 8B	3-State	●	
	TBP34L162	4096W × 4B	3-State	▲	
8K-Bit Arrays	TBP28L85A	1024W × 8B	3-State	▲	
	TBP28L86A	1024W × 8B	3-State	●	
	TBP38L85	1024W × 8B	3-State	▲	
	TBP38L86	1024W × 8B	3-State	▲	
4K-Bit Arrays	TBP28L42	512W × 8B	3-State	●	
	TBP28L46	512W × 8B	3-State	●	
2K-Bit Arrays	TBP28L22	256W × 8B	3-State	●	
	TBP28LA22	256W × 8B	OC	●	
	TBP38L22	256W × 8B	3-State	●	
1K-Bit Arrays	TBP34L10	256W × 4B	3-State	●	
256-Bit Arrays	TBP38L030	32W × 8B	3-State	●	

REGISTERED PROMs

DESCRIPTION	TYPE	ORGANIZATION	TYPE OUTPUT	S	VOLUME
16K-Bit Arrays	TBP34R162	4096W × 4B	3-State	●	4
	TBP34SR165	4096W × 4B	3-State	●	
	TBP38R165	2048W × 8B	3-State	●	

RANDOM-ACCESS READ-WRITE MEMORIES (RAMs)

DESCRIPTION	ORGANIZATION	TYPE OF OUTPUT	TYPE	TECHNOLOGY					VOLUME
				STD TTL	ALS	AS	LS	S	
256-Bit Arrays	256 × 1	3-State	'201					●	4
		OC	'301					●	
64-Bit Arrays	16 × 4	OC	'89	●					
		3-State	'189				A	B	
		3-State	'219				A		
		OC	'289				A	B	
		OC	'319				A		
16-Bit Multiple-Port Register File	8 × 2	3-State	'172	●					2
16-Bit Register File	4 × 4	OC	'170	●			●		
		3-State	'670				●		
Dual 64-Bit Register Files	16 × 4	3-State	'870			●			3
			'871			●			

FIRST-IN FIRST-OUT MEMORIES (FIFOs)

DESCRIPTION	TYPE OF OUTPUT	TYPE	TECHNOLOGY				VOLUME
			ALS	AS	LS	S	
16 × 4	3-State	222			●		LSI
	3-State	224			●		
	3-State	227			●		
	3-State	228			●		
	3-State	232	A				3 & LSI
16 × 5	3-State	225			●	●	LSI
	3-State	229	A				3 & LSI
	3-State	233	A				

● Denotes available technology.
▲ Denotes planned new products.
A Denotes "A" suffix version available in the technology indicated.
B Denotes "B" suffix version available in the technology indicated.

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PROGRAMMABLE LOGIC ARRAYS

PROGRAMMABLE LOGIC ARRAYS

DESCRIPTION	INPUTS	NO.	OUTPUTS TYPE	TYPE NO	ALS	NO. OF PINS	VOLUME
High-Performance PAL*	16	8	Active-Low	*PAL16L8A	•	20	
		4	Registered	*PAL16R4A	•		
		6		*PAL16R6A	•		
		8		*PAL16R8A	•		
Half-Power PAL*	16	8	Active-Low	*PAL16L8A-2	•	20	
		4	Registered	*PAL16R4A-2	•		
		6		*PAL16R6A-2	•		
		8		*PAL16R8A-2	•		
High-Performance PAL*	20	8	Active-Low	*PAL20L8A	•	24	
		4	Registered	*PAL20R4A	•		
		6		*PAL20R6A	•		
		8		*PAL20R8A	•		
Half-Power PAL*	20	8	Active-Low	*PAL20L8A-2	•	24	
		4	Registered	*PAL20R4A-2	•		
		6		*PAL20R6A-2	•		
		8		*PAL20R8A-2	•		
Impact PAL*	16	8	Active-Low	*TIBPAL16L8-12	•	20	
		4	Registered	*TIBPAL16R4-12	•		
		6		*TIBPAL16R6-12	•		
		8		*TIBPAL16R8-12	•		
Impact PAL*	16	8	Active-Low	*TIBPAL16L8-15	•	20	
		4	Registered	*TIBPAL16R4-15	•		
		6		*TIBPAL16R6-15	•		
		8		*TIBPAL16R8-15	•		
Impact PAL*	20	8	Active-Low	*TIBPAL20L8-15	•	24	
		4	Registered	*TIBPAL20R4-15	•		
		6		*TIBPAL20R6-15	•		
		8		*TIBPAL20R8-15	•		
Exclusive-OR PAL*	20	10	Active-Low	*TIBPAL20L10-20	•	24	4
		4	Registered	*TIBPAL20X4-20	•		
		8		*TIBPAL20X8-20	•		
		10		*TIBPAL20X10-20	•		
Exclusive-OR PAL*	20	8	Active-Low	*TIBPAL20L10-35	•	24	
		4	Registered	*TIBPAL20X4-35	•		
		8		*TIBPAL20X8-35	•		
		10		*TIBPAL20X10-35	•		
Registered-Input PAL*	19	8	Active-Low	*TIBPALR19L8-25	•	24	
		4	Registered	*TIBPALR19R4-25	•		
		6		*TIBPALR19R6-25	•		
		8		*TIBPALR19R8-25	•		
Registered-Input PAL*	19	8	Active-Low	*TIBPALR19L8-40	•	24	
		4	Registered	*TIBPALR19R4-40	•		
		6		*TIBPALR19R6-40	•		
		8		*TIBPALR19R8-40	•		
Latched-Input PAL*	19	8	Active-Low	*TIBPALT19L8-25	•	24	
		4	Registered	*TIBPALT19R4-25	•		
		6		*TIBPALT19R6-25	•		
		8		*TIBPALT19R8-25	•		
Latched-Input PAL*	19	8	Active-Low	*TIBPALT19L8-40	•	24	
		4	Registered	*TIBPALT19R4-40	•		
		6		*TIBPALT19R6-40	•		
		8		*TIBPALT19R8-40	•		
Field-Programmable 14 × 32 × 6 Logic Arrays	14	6	3-State	*TIFPLA839	•	24	
			OC	*TIFPLA840	•		

* PAL is a registered trademark of Monolithic Memories Incorporated.

• Denotes available technology.

D2661, APRIL 1982—REVISED MAY 1986

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

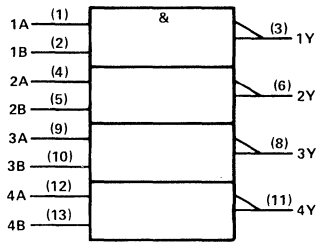
These devices contain four independent 2-input NAND gates. They perform the Boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The SN54ALS00A and SN54AS00 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS00A and SN74AS00 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

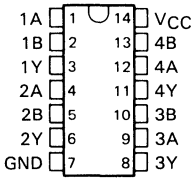
INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol†

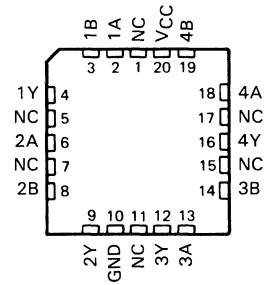


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54ALS00A, SN54AS00 . . . J PACKAGE
SN74ALS00A, SN74AS00 . . . D OR N PACKAGE
(TOP VIEW)

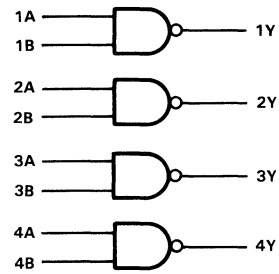


SN54ALS00A, SN54AS00 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



2

ALS and AS Circuits

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS00A . . . . . −55°C to 125°C
SN74ALS00A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS00A			SN74ALS00A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS00A			SN74ALS00A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.5	0.85		0.5	0.85	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		1.5	3		1.5	3	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS00A	SN54ALS00A		SN74ALS00A		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	7	3	16	3	11	ns
t_{PHL}	A or B	Y	5	2	13	2	8	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS00 . . . . . −55°C to 125°C
SN74AS00 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS00			SN74AS00			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS00			SN74AS00			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		2	3.2		2	3.2	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		10.8	17.4		10.8	17.4	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 50 Ω, T_A = MIN to MAX				UNIT
			SN54AS00		SN74AS00		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1	5	1	4.5	ns
t_{PHL}	A or B	Y	1	5	1	4	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

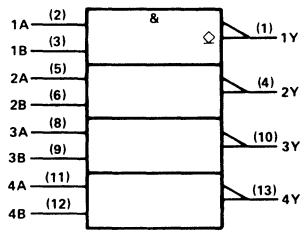
These devices contain four independent 2-input NAND gates. They perform the Boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN54ALS01 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS01 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

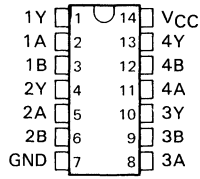
INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol†

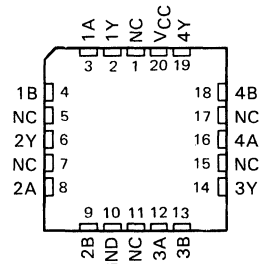


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54ALS01 . . . J PACKAGE
SN74ALS01 . . . D OR N PACKAGE
(TOP VIEW)

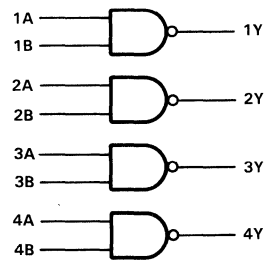


SN54ALS01 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS01 . . . . . −55°C to 125°C
SN74ALS01 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS01			SN74ALS01			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS01			SN74ALS01			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.43	0.85		0.43	0.85	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		1.62	3		1.62	3	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 2 kΩ, T_A = MIN to MAX				UNIT
			SN54ALS01		SN74ALS01		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	23	66	23	54	ns
t_{PHL}	A or B	Y	8	39	8	28	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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D2661, APRIL 1982—REVISED MAY 1986

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

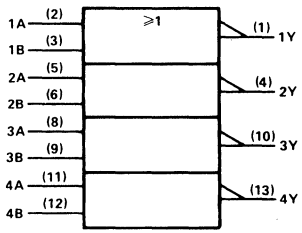
These devices contain four independent 2-input NOR gates. They perform the Boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The SN54ALS02 and SN54AS02 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS02 and SN74AS02 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

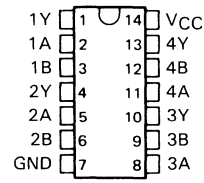
INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

logic symbol†

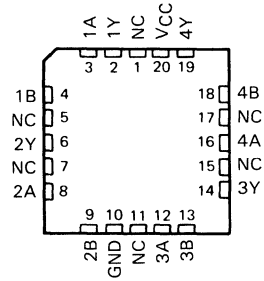


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54ALS02, SN54AS02 . . . J PACKAGE
SN74ALS02, SN74AS02 . . . D OR N PACKAGE
(TOP VIEW)

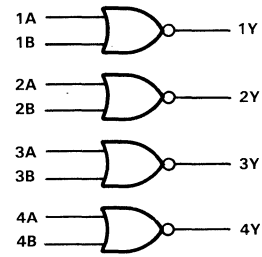


SN54ALS02, SN54AS02 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS02 . . . . . −55°C to 125°C
SN74ALS02 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS02			SN74ALS02			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating-free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS02			SN74ALS02			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.86	2.2		0.86	2.2	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		2.16	4		2.16	4	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS02	SN54ALS02		SN74ALS02		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	7	1	18	3	12	ns
t_{PHL}	A or B	Y	5	1	11	3	10	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS02 . . . . . −55°C to 125°C
SN74AS02 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS02			SN74AS02			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating-free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS02			SN74AS02			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		3.7	5.9		3.7	5.9	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		12.5	20.1		12.5	20.1	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS02		SN74AS02		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1	5	1	4.5	ns
t_{PHL}	A or B	Y	1	5	1	4.5	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

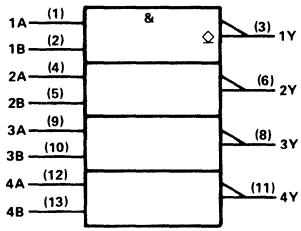
These devices contain four independent 2-input NAND buffers. They perform the Boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN54ALS03B is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS03B is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

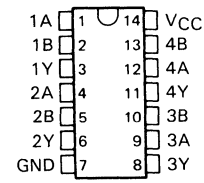
INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol†

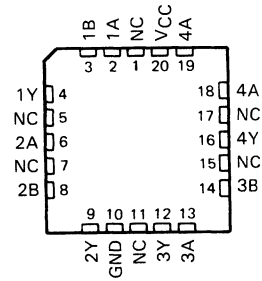


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54ALS03B . . . J PACKAGE
SN74ALS03B . . . D OR N PACKAGE
(TOP VIEW)

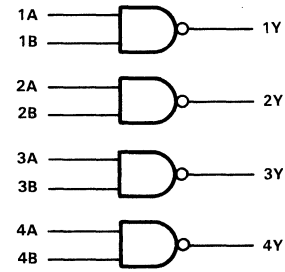


SN54ALS03B . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS03B . . . . . −55°C to 125°C
SN74ALS03B . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS03B			SN74ALS03B			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating-free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS03B			SN74ALS03B			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.43	0.85		0.43	0.85	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		1.62	3		1.62	4	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 2 kΩ, T_A = MIN to MAX				UNIT
			'ALS03B	SN54ALS03B		SN74ALS03B		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	35	20	59	20	50	ns
t_{PHL}	A or B	Y	8	3	23	3	13	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

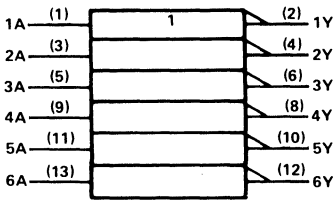
These devices contain six independent inverters. They perform the Boolean function $Y = \overline{A}$.

The SN54ALS04B and SN54AS04 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS04B and SN74AS04 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each inverter)

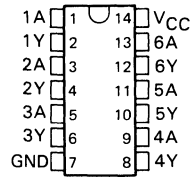
INPUT A	OUTPUT Y
H	L
L	H

logic symbol†

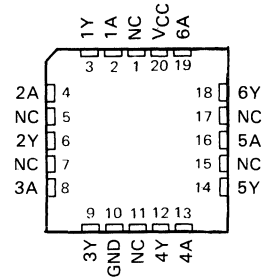


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54ALS04B, SN54AS04 . . . J PACKAGE
SN74ALS04B, SN74AS04 . . . D OR N PACKAGE
(TOP VIEW)

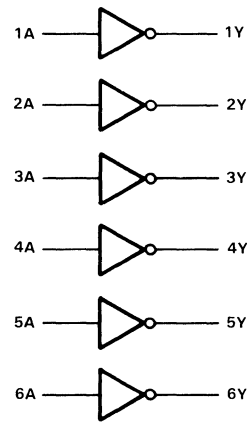


SN54ALS04B, SN54AS04 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



2 ALS and AS Circuits

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS04B . . . . . −55°C to 125°C
SN74ALS04B . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS04B			SN74ALS04B			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS04B			SN74ALS04B			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.65	1.1		0.65	1.1	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		2.9	4.2		2.9	4.2	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS04B		SN74ALS04B		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	3	14	3	11	ns
t_{PHL}	A	Y	2	12	2	8	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS04 . . . . . −55°C to 125°C
SN74AS04 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS04			SN74AS04			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS04			SN74AS04			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		3	4.8		3	4.8	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		14	26.3		14	26.3	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS04		SN74AS04		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1	6	1	5	ns
t_{PHL}	A	Y	1	4.5	1	4	ns

NOTE 1. Load circuit and voltage waveforms are shown in Section 1.

D2661, APRIL 1982—REVISED MAY 1986

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

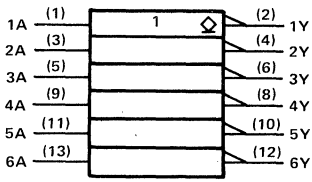
These devices contain six independent inverters. They perform the Boolean function $Y = \overline{A}$. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN54ALS05A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS05A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each inverter)

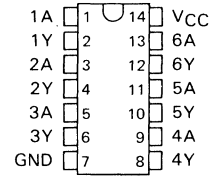
INPUT A	OUTPUT Y
H	L
L	H

logic symbol†

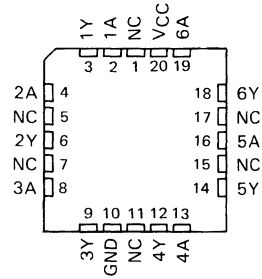


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54ALS05A . . . J PACKAGE
SN74ALS05A . . . D OR N PACKAGE
(TOP VIEW)

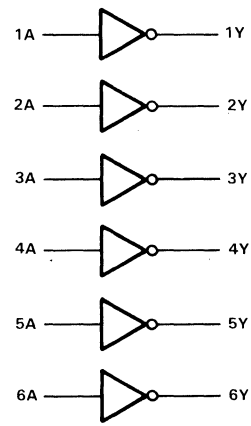


SN54ALS05A . . . FK PACKAGE
(TOP VIEW)



NC — No internal connection

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS05A . . . . . −55°C to 125°C
SN74ALS05A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS05A			SN74ALS05A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS05A			SN74ALS05A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.65	1.1		0.65	1.1	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		2.9	4.2		2.9	4.2	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS05A	SN54ALS05A		SN74ALS05A		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	45	23	84	23	54	ns
t_{PHL}	A	Y	9	4	24	4	14	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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D2661, APRIL 1982—REVISED MAY 1986

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

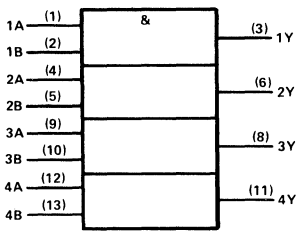
These devices contain four independent 2-input AND gates. They perform the Boolean functions $Y = A \cdot B$ or $Y = \overline{\overline{A} + \overline{B}}$ in positive logic.

The SN54ALS08 and SN54AS08 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS08 and SN74AS08 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each gate)

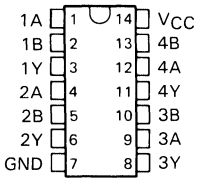
INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

logic symbol†

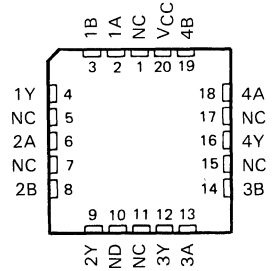


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54ALS08, SN54AS08 . . . J PACKAGE
SN74ALS08, SN74AS08 . . . D OR N PACKAGE
(TOP VIEW)

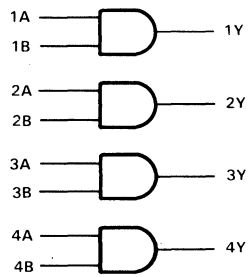


SN54ALS08, SN54AS08 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS08 . . . . . −55°C to 125°C
SN74ALS08 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS08			SN74ALS08			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	mA
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low--level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS08			SN74ALS08			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2						V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		1.3	2.4		1.3	2.4	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		2.2	4		2.2	4	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS08	SN54ALS08		SN74ALS08		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	8	4	18	4	14	ns
t_{PHL}	A or B	Y	6.5	3	15	3	10	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS08 . . . . . −55°C to 125°C
SN74AS08 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS08			SN74AS08			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	mA
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS08			SN74AS08			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		5.8	9.3		5.8	9.3	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		14.9	24		14.9	24	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions hav been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 50 Ω, T_A = MIN to MAX				UNIT
			SN54AS08		SN74AS08		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1	6.5	1	5.5	ns
t_{PHL}	A or B	Y	1	6.5	1	5.5	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2661, APRIL 1982—REVISED MAY 1986

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

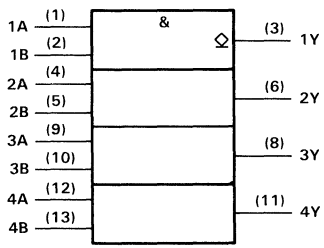
These devices contain four independent 2-input AND gates. They perform the Boolean functions $Y = A \cdot B$ or $Y = \overline{\overline{A} + \overline{B}}$ in positive logic. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN54ALS09 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS09 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

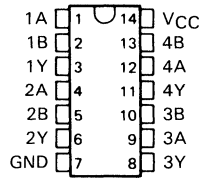
INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

logic symbol†

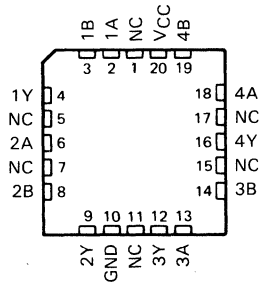


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54ALS09 . . . J PACKAGE
SN74ALS09 . . . D OR N PACKAGE
(TOP VIEW)

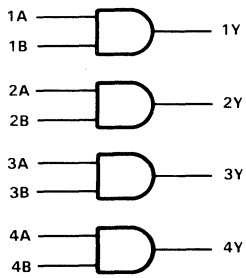


SN54ALS09 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS09 . . . . . −55°C to 125°C
SN74ALS09 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS09			SN74ALS09			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS09			SN74ALS09			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		1.35	2.4		1.35	2.4	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		2.2	4		2.2	4	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 2 kΩ, T_A = MIN to MAX				UNIT
			SN54ALS09		SN74ALS09		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	20	69	23	54	ns
t_{PHL}	A or B	Y	5	23	5	15	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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MARCH 1984—REVISED MAY 1986

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

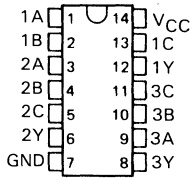
These devices contain three independent 3-input NAND gates. They perform the Boolean functions $Y = \overline{A \cdot B \cdot C}$ or $Y = \overline{A} + \overline{B} + \overline{C}$ in positive logic.

The SN54ALS10A and SN54AS10 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS10A and SN74AS10 are characterized for operation from 0°C to 70°C.

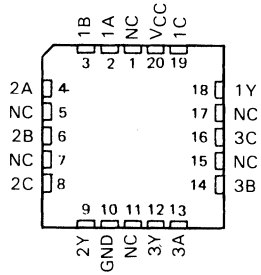
FUNCTION TABLE (each gate)

INPUTS			OUTPUT
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

SN54ALS10A, SN54AS10 . . . J PACKAGE
SN74ALS10A, SN74AS10 . . . D OR N PACKAGE
(TOP VIEW)

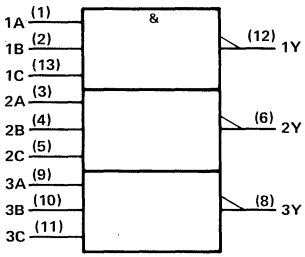


SN54ALS10A, SN54AS10 . . . FK PACKAGE
(TOP VIEW)



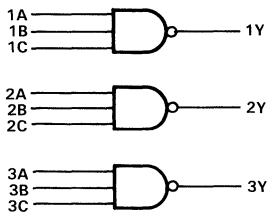
NC—No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS10A . . . . . −55 °C to 125 °C
SN74ALS10A . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS10A			SN74ALS10A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS10A			SN74ALS10A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.32	0.6		0.32	0.6	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		1.2	2.2		1.2	2.2	mA

†All typical values are at V_{CC} = 5 V, T_A = 25 °C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS10A		SN74ALS10A		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	2	16	2	11	ns
t_{PHL}	Any	Y	2	12	2	10	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS10 . . . . . −55 °C to 125 °C
SN74AS10 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54AS10			SN74AS10			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS10			SN74AS10			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		1.5	2.4		1.5	2.4	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		8.1	13		8.1	13	mA

†All typical values are at V_{CC} = 5 V, T_A = 25 °C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS10		SN74AS10		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	1	5	1	4.5	ns
t_{PHL}	Any	Y	1	5	1	4.5	ns

NOTE 1. Load circuit and voltage waveforms are shown in Section 1.

MARCH 1984—REVISED MAY 1986

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

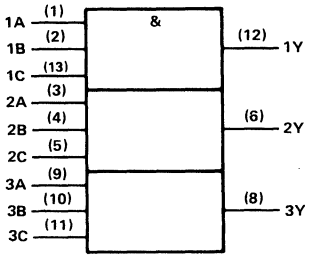
These devices contain three independent 3-input AND gates. They perform the Boolean functions $Y = A \cdot B \cdot C$ or $Y = \overline{\overline{A}+\overline{B}+\overline{C}}$ in positive logic.

The SN54ALS11A and SN54AS11 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS11A and SN74AS11 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

INPUTS			OUTPUT
A	B	C	Y
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

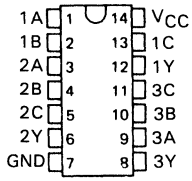
logic symbol†



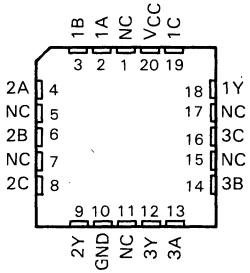
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

SN54ALS11A, SN54AS11 . . . J PACKAGE
SN74ALS11A, SN74AS11 . . . D OR N PACKAGE
(TOP VIEW)

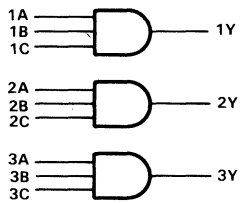


SN54ALS11A, SN54AS11 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS11A . . . . . −55°C to 125°C
SN74ALS11A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS11A			SN74ALS11A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS11A			SN74ALS11A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		1	1.8		1	1.8	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		1.6	3		1.6	3	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS11A		SN74ALS11A		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	2	17	2	13	ns
t_{PHL}	Any	Y	2	14	2	10	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS11 . . . . . −55°C to 125°C
SN74AS11 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS11			SN74AS11			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS11			SN74AS11			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		4.3	7		4.3	7	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		11.2	18		11.2	18	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS11		SN74AS11		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	1	6.5	1	6	ns
t_{PHL}	Any	Y	1	6.5	1	5.5	ns

NOTE 1. Load circuit and voltage waveforms are shown in Section 1.

MARCH 1984—REVISED MAY 1986

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

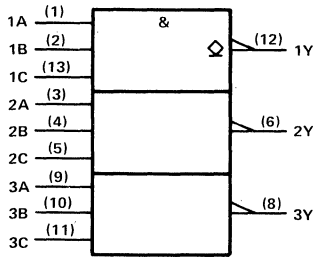
These devices contain three independent 3-input NAND gates with open-collector outputs. These gates perform the Boolean functions $Y = \overline{A \cdot B \cdot C}$ or $Y = \overline{A} + \overline{B} + \overline{C}$ in positive logic. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN54ALS12A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS12A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

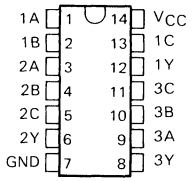
INPUTS			OUTPUT
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

logic symbol†

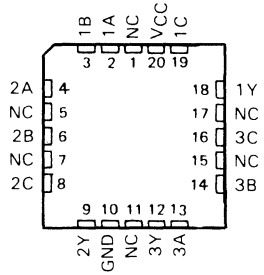


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54ALS12A . . . J PACKAGE
SN74ALS12A . . . D OR N PACKAGE
(TOP VIEW)

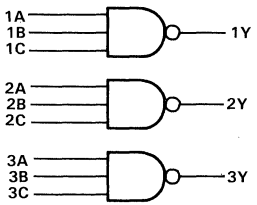


SN54ALS12A . . . FK PACKAGE
(TOP VIEW)



NC No internal connection

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS12A . . . . . −55°C to 125°C
SN74ALS12A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS12A			SN74ALS12A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS12A			SN74ALS12A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.32	0.6		0.32	0.6	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		1.2	2.2		1.2	2.2	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 2 kΩ, T_A = MIN to MAX				UNIT
			SN54ALS12A		SN74ALS12A		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	23	59	23	54	ns
t_{PHL}	Any	Y	5	26	5	18	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

MARCH 1984—REVISED MAY 1986

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

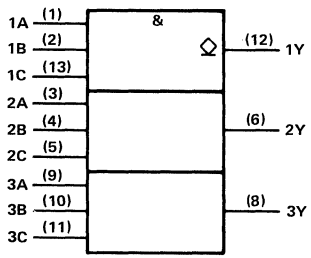
These devices contain three independent 3-input AND gates with open-collector outputs. These gates perform the Boolean functions $Y = A \cdot B \cdot C$ or $Y = \overline{\overline{A}+\overline{B}+\overline{C}}$ in positive logic. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN54ALS15A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS15A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

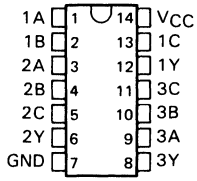
INPUTS			OUTPUT
A	B	C	Y
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

logic symbol†

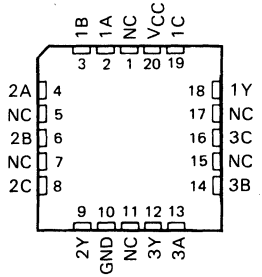


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54ALS15A . . . J PACKAGE
SN74ALS15A . . . D OR N PACKAGE
(TOP VIEW)

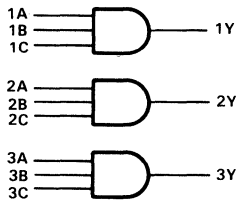


SN54ALS15A . . . FK PACKAGE
(TOP VIEW)



NC — No internal connection

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS15A . . . . . −55°C to 125°C
SN74ALS15A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS15A			SN74ALS15A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS15A			SN74ALS15A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		1	1.8		1	1.8	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		1.66	3		1.66	3	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 2 kΩ, T_A = MIN to MAX				UNIT
			SN54ALS15A		SN74ALS15A		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	20	59	20	45	ns
t_{PHL}	Any	Y	6	25	6	20	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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D2661, APRIL 1982—REVISED MAY 1986

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

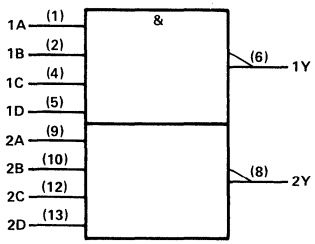
These devices contain two independent 4-input NAND gates. They perform the Boolean functions $Y = \overline{A \cdot B \cdot C \cdot D}$ or $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D}$ in positive logic.

The SN54ALS20A and SN54AS20 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS20A and SN74AS20 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

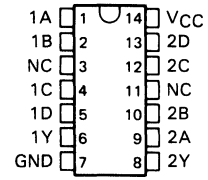
INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

logic symbol†

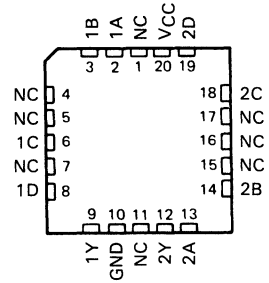


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54ALS20A, SN54AS20 . . . J PACKAGE
SN74ALS20A, SN74AS20 . . . D OR N PACKAGE
(TOP VIEW)

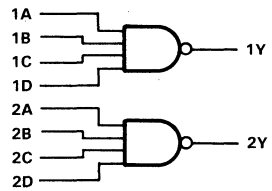


SN54ALS20A, SN54AS20 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS20A . . . . . −55°C to 125°C
SN74ALS20A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS20A			SN74ALS20A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating-free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS20A			SN74ALS20A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.22	0.4		0.22	0.4	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		0.81	1.5		0.81	1.5	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS20A	SN54ALS20A		SN74ALS20A		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	7	1	18	3	11	ns
t_{PHL}	Any	Y	6	1	15	3	10	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS20 . . . . . −55°C to 125°C
SN74AS20 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS20			SN74AS20			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating-free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS20			SN74AS20			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		1	1.6		1	1.6	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		5.4	8.7		5.4	8.7	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS20		SN74AS20		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	1	5.5	1	5	ns
t_{PHL}	Any	Y	1	5	1	4.5	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2661, APRIL 1982—REVISED MAY 1986

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

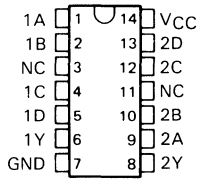
These devices contain two independent 4-input AND gates. They perform the Boolean functions $Y = A \cdot B \cdot C \cdot D$ or $Y = \overline{\overline{A}+\overline{B}+\overline{C}+\overline{D}}$ in positive logic.

The SN54ALS21A and SN54AS21 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS21A and SN74AS21 are characterized for operation from 0°C to 70°C.

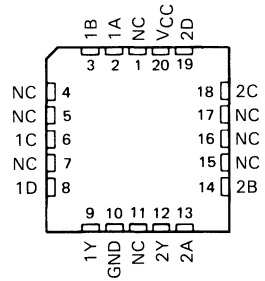
FUNCTION TABLE (each gate)

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	H
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L

SN54ALS21A, SN54AS21 . . . J PACKAGE
SN74ALS21A, SN74AS21 . . . D OR N PACKAGE
(TOP VIEW)

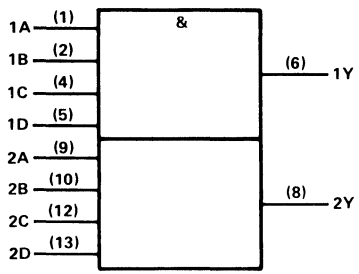


SN54ALS21A, SN54AS21 . . . FK PACKAGE
(TOP VIEW)



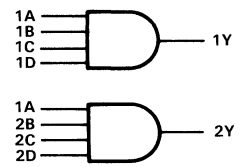
NC—No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS21A . . . . . −55°C to 125°C
SN74ALS21A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS21A			SN74ALS21A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS21A			SN74ALS21A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		0.85	1.4		0.85	1.4	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		1.4	2.3		1.4	2.3	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS21A	SN54ALS21A		SN74ALS21A		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	8.3	4	18	4	15	ns
t_{PHL}			6.5	2	12	2	10	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS21 . . . . . −55°C to 125°C
SN74AS21 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS21			SN74AS21			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS21			SN74AS21			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		2.9	4.6		2.9	4.6	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		7.4	12		7.4	12	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS21		SN74AS21		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	1	6.5	1	6	ns
t_{PHL}	Any	Y	1	6.5	1	6	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

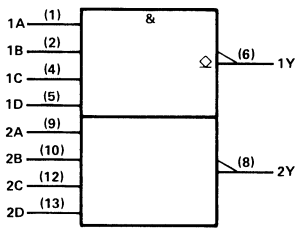
These devices contain two independent 4-input NAND gates. They perform the Boolean functions $Y = \overline{A \cdot B \cdot C \cdot D}$ or $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D}$ in positive logic. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN54ALS22B is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS22B is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

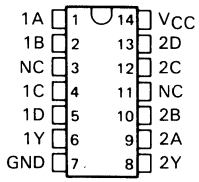
INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

logic symbol†

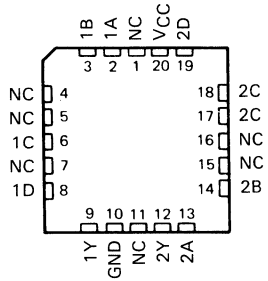


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54ALS22B . . . J PACKAGE
SN74ALS22B . . . D OR N PACKAGE
(TOP VIEW)

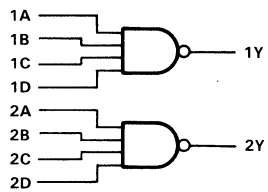


SN54ALS22B . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



2 ALS and AS Circuits

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS22B . . . . . −55°C to 125°C
SN74ALS22B . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS22B			SN74ALS22B			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating-free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS22B			SN74ALS22B			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.22	0.4		0.22	0.4	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		0.8	1.5		0.8	1.5	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 2 kΩ, T_A = MIN to MAX			UNIT
			'ALS22B	SN54ALS22B		SN74ALS22B	
			TYP	MIN	MAX	MIN	MAX
t_{PLH}	Any	Y	35	23	65	23	45	ns
t_{PHL}	Any	Y	8	4	32	4	18	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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D2661, APRIL 1982—REVISED MAY 1986

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

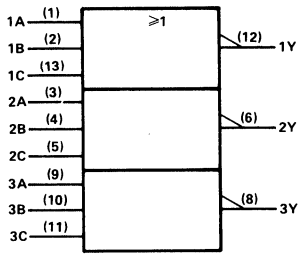
These devices contain three independent 3-input NOR gates. They perform the Boolean functions $Y = \overline{A+B+C}$ or $Y = \overline{A}\cdot\overline{B}\cdot\overline{C}$ in positive logic.

The SN54ALS27 and SN54AS27 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS27 and SN74AS27 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

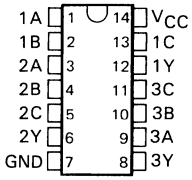
INPUTS			OUTPUT
A	B	C	Y
H	X	X	L
X	H	X	L
X	X	H	L
L	L	L	H

logic symbol†

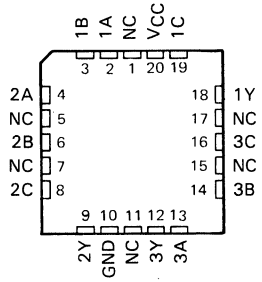


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54ALS27, SN54AS27 . . . J PACKAGE
SN74ALS27, SN74AS27 . . . D OR N PACKAGE
(TOP VIEW)

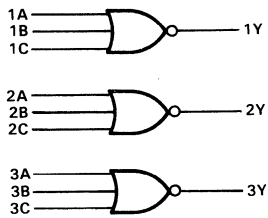


SN54ALS27, SN54AS27 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS27 . . . . . −55 °C to 125 °C
SN74ALS27 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS27			SN74ALS27			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS27			SN74ALS27			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.97	1.8		0.97	1.8	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		2	4		2	4	mA

†All typical values are at V_{CC} = 5 V, T_A = 25 °C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS27		SN74ALS27		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	4	26	4	15	ns
t_{PHL}	Any	Y	1	11	3	9	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS27 . . . . . −55°C to 125°C
SN74AS27 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS27			SN74AS27			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS27			SN74AS27			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		4	6.4		4	6.4	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		10.6	17.1		10.6	17.1	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS27		SN74AS27		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	1	6.5	1	5.5	ns
t_{PHL}	Any	Y	1	5	1	4.5	ns

NOTE 1. Load circuit and voltage waveforms are shown in Section 1.

D2661, APRIL 1982—REVISED MAY 1986

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

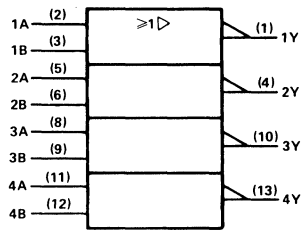
These devices contain four independent 2-input NOR buffer gates. They perform the Boolean functions $Y = \overline{A+B}$ or $Y = \overline{A} \cdot \overline{B}$ in positive logic.

The SN54ALS28A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS28A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

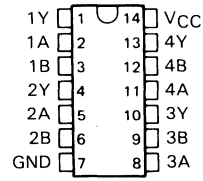
INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

logic symbol†

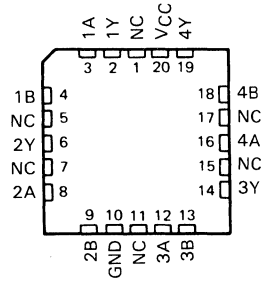


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54ALS28A . . . J PACKAGE
SN74ALS28A . . . D OR N PACKAGE
(TOP VIEW)

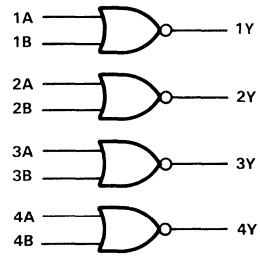


SN54ALS28A . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS28A . . . . . −55°C to 125°C
SN74ALS28A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS28A			SN74ALS28A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS28A			SN74ALS28A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.3		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		1.7	2.8		1.7	2.8	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		5.6	9		5.6	9	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS28A	SN54ALS28A		SN74ALS28A		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	4	1	16	2	8	ns
t_{PHL}	A or B	Y	4	1	10	2	7	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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MARCH 1984—REVISED MAY 1986

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These devices contain a single 8-input NAND gate and perform the following Boolean functions in positive logic:

$$Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H} \text{ OR}$$

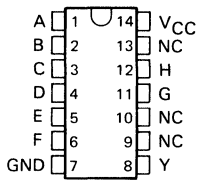
$$Y = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F} + \overline{G} + \overline{H}$$

The SN54ALS30A and SN54AS30 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS30A and SN74AS30 are characterized for operation from 0°C to 70°C.

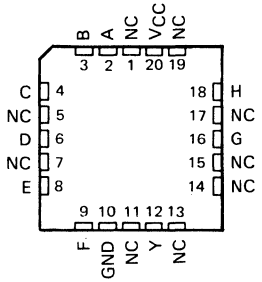
FUNCTION TABLE

INPUTS A THRU H	OUTPUT Y
All inputs H	L
One or more inputs L	H

SN54ALS30A, SN54AS30 . . . J PACKAGE
SN74ALS30A, SN74AS30 . . . D OR N PACKAGE
(TOP VIEW)

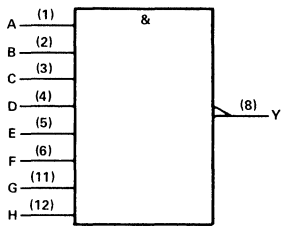


SN54ALS30A, SN54AS30 . . . FK PACKAGE
(TOP VIEW)



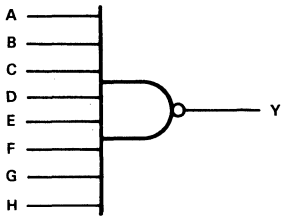
NC—No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS30A . . . . . −55°C to 125°C
SN74ALS30A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS30A			SN74ALS30A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS30A			SN74ALS30A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.22	0.36		0.22	0.36	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		0.54	0.9		0.54	0.9	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS30A		SN74ALS30A		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	3	15	3	10	ns
t_{PHL}	Any	Y	3	15	3	12	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS30 . . . . . −55 °C to 125 °C
SN74AS30 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54AS30			SN74AS30			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS30			SN74AS30			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.9	1.5		0.9	1.5	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		3	4.9		3	4.9	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS30		SN74AS30		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	1	5.5	1	5	ns
t_{PHL}	Any	Y	1	5	1	4.5	ns

NOTE 1. Load circuit and voltage waveforms are shown in Section 1.

ALS and AS Circuits

D2661, APRIL 1982—REVISED MAY 1986

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

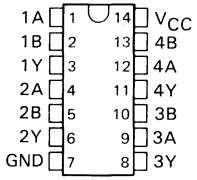
These devices contain four independent 2-input OR gates. They perform the Boolean functions $Y = A+B$ or $Y = \overline{\overline{A}\cdot\overline{B}}$ in positive logic.

The SN54ALS32 and SN54AS32 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS32 and SN74AS32 are characterized for operation from 0°C to 70°C.

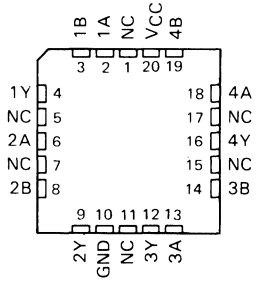
FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

SN54ALS32, SN54AS32 . . . J PACKAGE
SN74ALS32, SN74AS32 . . . D OR N PACKAGE
(TOP VIEW)

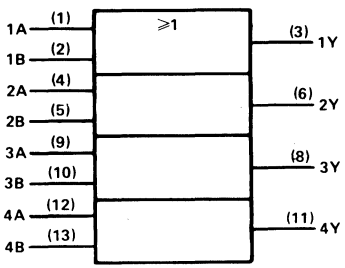


SN54ALS32, SN54AS32 . . . FK PACKAGE
(TOP VIEW)



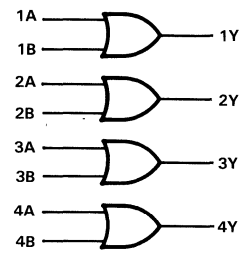
NC—No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS32 . . . . . −55°C to 125°C
SN74ALS32 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS32			SN74ALS32			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	mA
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low--level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS32			SN74ALS32			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		1.9	4		1.9	4	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		2.6	4.9		2.6	4.9	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS32	SN54ALS32		SN74ALS32		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	8.8	3	18	3	14	ns
t_{PHL}	A or B	Y	6.8	3	16	3	12	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS32 . . . . . −55°C to 125°C
SN74AS32 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS32			SN74AS32			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	mA
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low--level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS32			SN74AS32			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		7.3	12		7.3	12	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		16.5	26.6		16.5	26.6	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 50 Ω, T_A = MIN to MAX				UNIT
			SN54AS32		SN74AS32		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1	7.5	1	5.8	ns
t_{PHL}	A or B	Y	1	6.5	1	5.8	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2661, APRIL 1982—REVISED MAY 1986

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

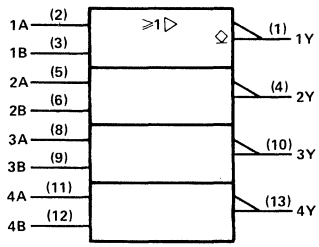
These devices contain four independent 2-input NOR buffer gates with open-collector outputs. Open-collector outputs require resistive pull-up to perform logically but can deliver higher V_{OH} levels and are commonly used in wired-AND applications. These devices perform the Boolean functions $Y = A+B$ or $Y = A \cdot B$ in positive logic.

The SN54ALS33A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS33A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

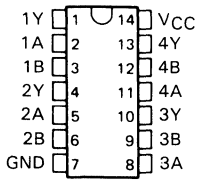
INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

logic symbol†

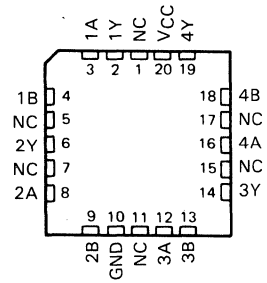


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54ALS33A . . . J PACKAGE
SN74ALS33A . . . D OR N PACKAGE
(TOP VIEW)

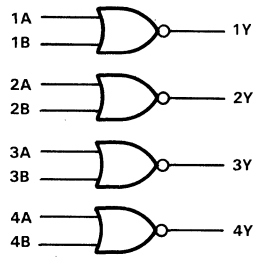


SN54ALS33A . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS33A . . . . . −55°C to 125°C
SN74ALS33A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS33A			SN74ALS33A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating-free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS33A			SN74ALS33A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		1.7	2.8		1.7	2.8	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		5.6	9		5.6	9	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 680 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX				UNIT
			'ALS33A			SN54ALS33A		SN74ALS33A		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y		18	24	10	59	10	33	ns
t_{PHL}	A or B	Y		7	10	2	18	2	12	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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D2261, DECEMBER 1983—REVISED MAY 1986

- **Noninverters**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

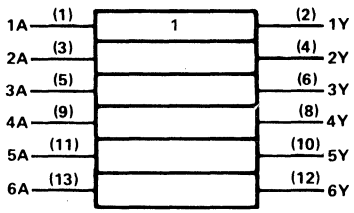
These devices contain six independent noninverters. They perform the Boolean function Y = A.

The SN54ALS34 and SN54AS34 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS34 and SN74AS34 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each buffer)

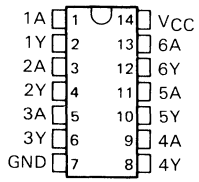
INPUT A	OUTPUT Y
H	H
L	L

logic symbol†

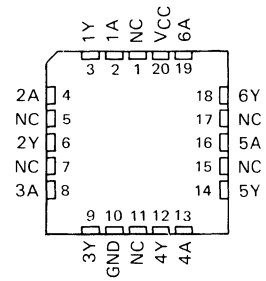


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54ALS34, SN54AS34 . . . J PACKAGE
SN74ALS34, SN74AS34 . . . D OR N PACKAGE
(TOP VIEW)

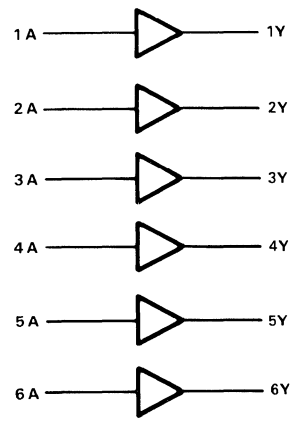


SN54ALS34, SN54AS34 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS34 . . . . . −55°C to 125°C
SN74ALS34 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS34			SN74ALS34			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS34			SN74ALS34			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		3.1	5		3.1	5	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		5	8		5	8	mA

†All typical values are at V_{CC} = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS34	SN54ALS34		SN74ALS34		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	9.4	4	18	4	15	ns
t_{PHL}			5	1	12	1	10	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted),

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS34 . . . . . −55°C to 125°C
SN74AS34 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS34			SN74AS34			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS34			SN74AS34			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		7.4	12		7.4	12	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		21.3	34.6		21.3	34.6	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS34		SN74AS34		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1	6.5	1	5.5	ns
t_{PHL}			1	7	1	6	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2661, DECEMBER 1983—REVISED MAY 1986

- **Noninverters with Open-Collector Outputs**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

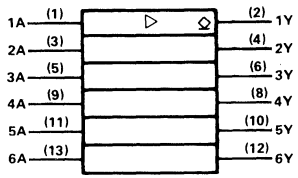
These devices contain six independent noninverters. They perform the Boolean functions Y = A. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN54ALS35A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS35A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each buffer)

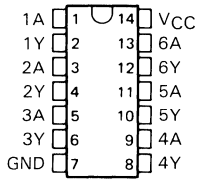
INPUT A	OUTPUT Y
H	H
L	L

logic symbol†

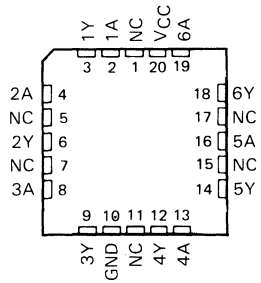


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J and N packages.

SN54ALS35A . . . J PACKAGE
SN74ALS35A . . . D OR N PACKAGE
(TOP VIEW)

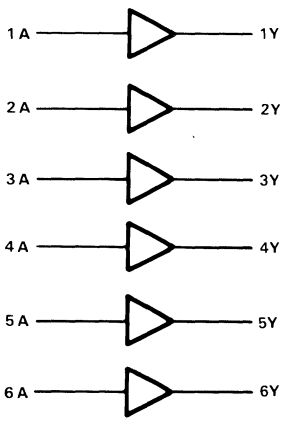


SN54ALS35A . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS35A . . . . . −55°C to 125°C
SN74ALS35A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS35A			SN74ALS35A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS35A			SN74ALS35A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		2.7	4.7		2.7	4.7	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		4.1	6.3		4.1	6.3	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 2 kΩ, T_A = MIN to MAX				UNIT
			'ALS35A	SN54ALS35A		SN74ALS35A		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	34	20	60	20	50	ns
t_{PHL}			9	2	17	2	14	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

D2661, APRIL 1982—REVISED MAY 1986

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

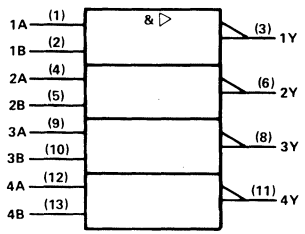
These devices contain four independent 2-input NAND buffer gates. They perform the Boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The SN54ALS37A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS37A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

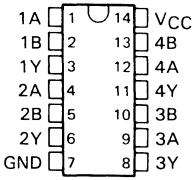
INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol†

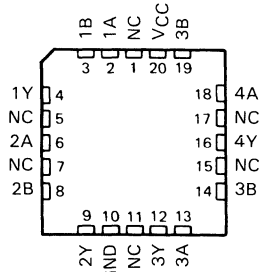


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54ALS37A . . . J PACKAGE
SN74ALS37A . . . D OR N PACKAGE
(TOP VIEW)

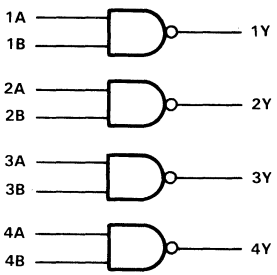


SN54ALS37A . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS37A . . . . . −55°C to 125°C
SN74ALS37A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS37A			SN74ALS37A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating-free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS37A			SN74ALS37A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.86	1.6		0.86	1.6	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		4.8	7.8		4.8	7.8	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS37A	SN54ALS37A		SN74ALS37A		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	4	2	17	2	8	ns
t_{PHL}	A or B	Y	5	2	10	2	7	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

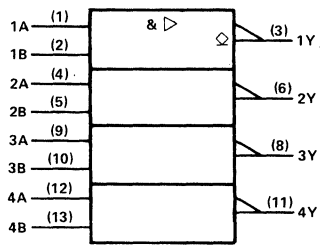
These devices contain four independent 2-input NAND buffer gates with open-collector outputs. These NAND buffers perform the Boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN54ALS38A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS38A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

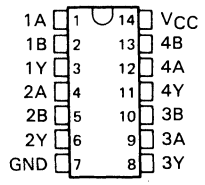
INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol†

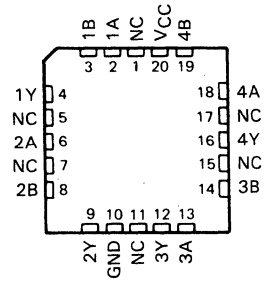


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54ALS38A . . . J PACKAGE
SN74ALS38A . . . D OR N PACKAGE
(TOP VIEW)

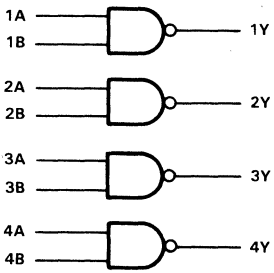


SN54ALS38A . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS38A . . . . . −55°C to 125°C
SN74ALS38A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS38A			SN74ALS38A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating-free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS38A			SN74ALS38A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.86	1.6		0.86	1.6	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		4.8	7.8		4.8	7.8	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 680 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX				UNIT
			'ALS38A	SN54ALS38A		SN74ALS38A		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	18	10	59	10	33	ns
t_{PHL}	A or B	Y	7	2	18	2	12	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2661, APRIL 1984—REVISED MAY 1986

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

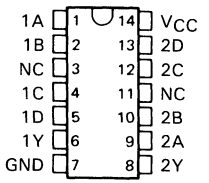
These devices contain two independent 4-input NAND buffer gates. They perform the Boolean functions $Y = \overline{A \cdot B \cdot C \cdot D}$ or $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D}$ in positive logic.

The SN54ALS40A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS40A is characterized for operation from 0°C to 70°C.

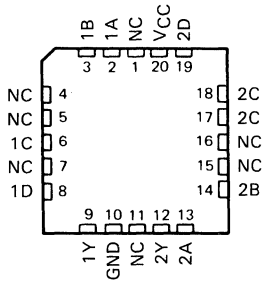
FUNCTION TABLE (each gate)

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

SN54ALS40A . . . J PACKAGE
SN74ALS40A . . . D OR N PACKAGE
(TOP VIEW)

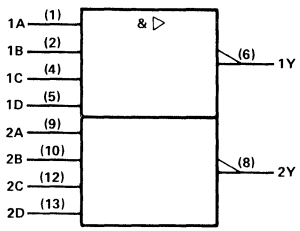


SN54ALS40A . . . FK PACKAGE
(TOP VIEW)



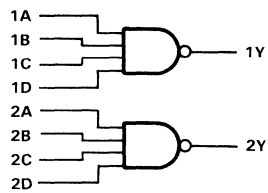
NC—No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS40A . . . . . −55°C to 125°C
SN74ALS40A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS40A			SN74ALS40A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating-free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS40A			SN74ALS40A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.43	0.8		0.43	0.8	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		2.4	3.9		2.4	3.9	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS40A	SN54ALS40A		SN74ALS40A		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	5	2	10	2	8	ns
t_{PHL}	Any	Y	5	2	10	2	7	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

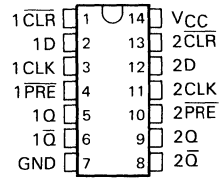
SN54ALS74A, SN54AS74, SN74ALS74A, SN74AS74
DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

D2661, APRIL 1982 – REVISED MAY 1986

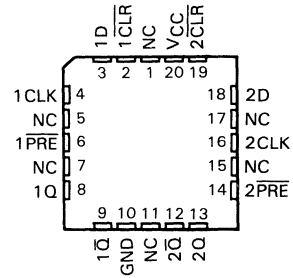
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY (C_L = 50 pF)	TYPICAL POWER DISSIPATION PER FLIP-FLOP
'ALS74A	50 MHz	6 mW
'AS74	134 MHz	26 mW

SN54ALS74A, SN54AS74 . . . J PACKAGE
SN74ALS74A, SN74AS74 . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS74A, SN54AS74 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These devices contain two independent D-type positive-edge-triggered flip-flops. A low level at the Preset or Clear inputs sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the D input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

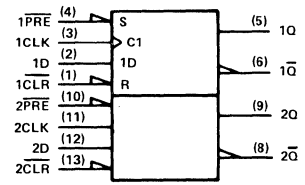
The SN54ALS74A and SN54AS74 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS74A and SN74AS74 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

* The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} if the lows at Preset and Clear are near V_{IL} maximum. Furthermore, this configuration is nonstable; that is, it will not persist when either Preset or Clear returns to its inactive (high) level.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS74A, SN54AS74 . . . . . −55°C to 125°C
SN74ALS74A, SN74AS74 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS74A			SN74ALS74A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		30	0		34	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	15			15			ns
		CLK high	17.5			14.5			
		CLK low	17.5			14.5			
t_{su}	Setup time before CLK↑	Data	16			15			ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	10			10			
t_h	Hold time, data after CLK↑		2			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS74A			SN74ALS74A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	CLK or D	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	$\overline{PRE}$ or $\overline{CLR}$					0.2			0.2	
I_{IH}	CLK or D	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	$\overline{PRE}$ or $\overline{CLR}$					40			40	
I_{IL}	CLK or D	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
	$\overline{PRE}$ or $\overline{CLR}$					−0.4			−0.4	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		2.4	4		2.4	4	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with D, CLK, and $\overline{PRE}$ grounded, then with D, CLK, and $\overline{CLR}$ grounded.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS74A		SN74ALS74A		
			MIN	MAX	MIN	MAX	
f_{max}			30		34		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	3	18	3	13	ns
t_{PHL}			5	17	5	15	
t_{PLH}	CLK	Q or $\overline{Q}$	5	23	5	16	ns
t_{PHL}			5	20	5	18	

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

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recommended operating conditions

			SN54AS74			SN74AS74			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−2	mA
I_{OL}	Low-level output current				20			20	mA
f_{clock}	Clock frequency		0		90	0		105	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	4			4			ns
		CLK high	4			4			
		CLK low	5.5			5.5			
t_{su}	Setup time before CLK↑	Data	4.5			4.5			ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	2			2			
t_h	Hold time, data after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS74			SN74AS74			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.25	0.5		0.25	0.5	V
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	CLK or D	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	$\overline{PRE}$ or $\overline{CLR}$					40			40	
I_{IL}	CLK or D	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	$\overline{PRE}$ or $\overline{CLR}$					−1.8			−1.8	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	See Note 1		10.5	16		10.5	16	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-current output current, I_{OS}.
NOTE 1: I_{CC} is measured with D, CLK, and $\overline{PRE}$ grounded, then with D, CLK, and $\overline{CLR}$ grounded.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS74		SN74AS74		
			MIN	MAX	MIN	MAX	
f_{max}			90		105		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	3	8.5	3	7.5	ns
t_{PHL}			3.5	11.5	3.5	10.5	
t_{PLH}	CLK	Q or $\overline{Q}$	3.5	9	3.5	8	ns
t_{PHL}			4.5	10.5	4.5	9	

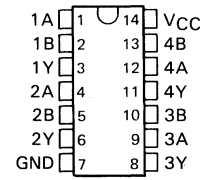
NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

ALS and AS Circuits

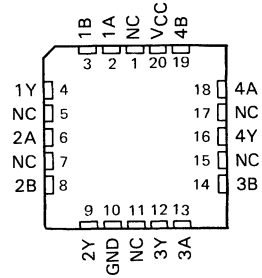
D2661, APRIL 1982—REVISED MAY 1986

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS86, SN54AS86 . . . J PACKAGE
SN74ALS86, SN74AS86 . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS86, SN54AS86 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

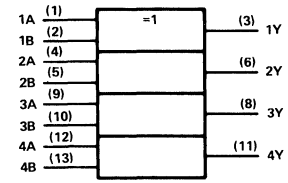
description

These devices contain four independent 2-input Exclusive-OR gates. They perform the Boolean functions $Y = A \oplus B = \overline{A}B + A\overline{B}$ in positive logic.

A common application is as a true/complement element. If one of the inputs is low, the other input will be reproduced in true form at the output. If one of the inputs is high, the signal on the other input will be reproduced inverted at the output.

The SN54ALS86 and SN54AS86 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS86 and SN74AS86 are characterized for operation from 0°C to 70°C.

logic symbol†



FUNCTION TABLE
(each gate)

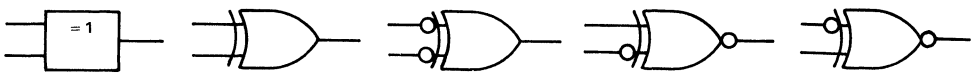
INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

exclusive-OR logic

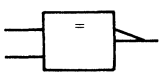
An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.

EXCLUSIVE-OR



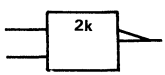
These are five equivalent Exclusive-OR symbols valid for an 'ALS86 gate in positive logic; negation may be shown at any two ports.

LOGIC IDENTITY ELEMENT



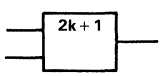
The output is active (low) if all inputs stand at the same logic level (i.e., A = B).

EVEN-PARITY



The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

ODD-PARITY ELEMENT



The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS86 . . . . . −55 °C to 125 °C
SN74ALS86 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS86			SN74ALS86			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS86			SN74ALS86			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V,	All inputs at 4.5 V		3.9	5.9		3.9	5.9	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS86		SN74ALS86		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	3	22	3	17	ns
t_{PHL}	(other input low)		2	14	2	12	
t_{PLH}	A or B	Y	3	22	3	17	ns
t_{PHL}	(other input high)		2	12	2	10	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS86 . . . . . −55°C to 125°C
SN74AS86 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS86			SN74AS86			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS86			SN74AS86			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		18			18		mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		15			15		mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

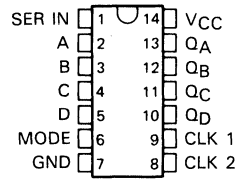
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			SN54AS86			SN74AS86			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A or B (other input low)	Y		3.6			3.6		ns
t_{PHL}				3.5			3.5		
t_{PLH}	A or B (other input high)	Y		3.6			3.6		ns
t_{PHL}				3.5			3.5		

† All typical valves are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

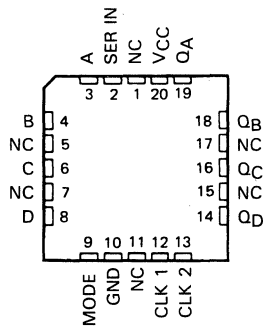
D2661, DECEMBER 1983—REVISED MAY 1986

- **Serial-to-Parallel Conversions**
- **Parallel Synchronous Loading**
- **Right or Left Shifts**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54AS95 . . . J PACKAGE
SN74AS95 . . . D OR N PACKAGE
(TOP VIEW)



SN54AS95 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

These four-bit registers feature parallel and serial inputs, parallel outputs, mode control, and two clock inputs. The registers have three modes of operation:

Parallel (broadside) load
Shift right (the direction Q_A toward Q_D)
Shift left (the direction Q_D toward Q_A)

Parallel loading is accomplished by applying the four bits and taking the mode control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the Clock-2 input. During loading, the entry of serial data is inhibited.

Shift right is accomplished on the high-to-low transition of Clock 1 when the mode control is low; shift left is accomplished on the high-to-low transition of Clock 2 when the mode control is high by connecting the output of each flip-flop to the parallel input of the previous flip-flop (Q_D to input C, etc.); and serial data is entered at input D. The clock input may be applied commonly to Clock 1 and Clock 2 if both modes can be clocked from the same source. Changes at the mode control input should normally be made while both clock inputs are low. However, conditions described in the last three lines of the function table will also ensure that the register contents are protected.

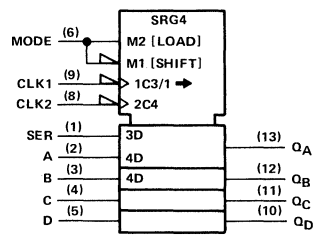
The SN54AS95 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS95 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS								OUTPUTS			
MODE	CLOCKS		SERIAL	PARALLEL							
CONTROL	2 (L)	1 (R)		A	B	C	D	Q_A	Q_B	Q_C	Q_D
H	H	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	↓	X	X	a	b	c	d	a	b	c	d
H	↓	X	X	Q_B†	Q_C†	Q_D†	d	Q_{Bn}	Q_{Cn}	Q_{Dn}	d.
L	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	X	↓	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
L	X	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
↑	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

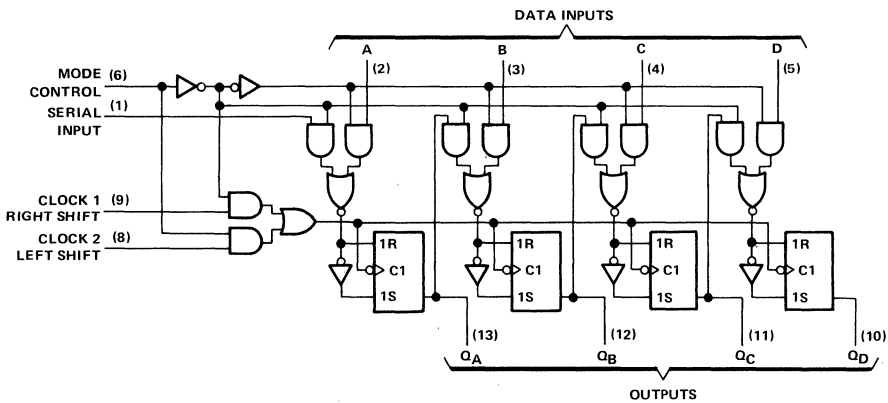
†Shifting left requires external connection of Q_B to A, Q_C to B, and Q_D to C. Serial data is entered at input D.
H = high level (steady state), L = low level (steady state), X = irrelevant (any input, including transitions).
↓ = transition from high to low level, ↑ = transition from low to high level.
a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the most-recent ↓ transition of the clock.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS95 . . . . . −55°C to 125°C
SN74AS95 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54AS95			SN74AS85			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−2			−2	mA
I_{OL}	Low-level output current				20			20	mA
f_{clock}	Clock frequency		0		80	0		100	MHz
t_w	Pulse duration, CLK high or low		6.5			5			ns
t_{su}	Setup time, data before CLK↓		2.5			2			ns
t_h	Hold time after CLK↓ (see Figure 1)	Data	2.5			2.5			ns
		CLK 1 to Mode	3.5			3			
		CLK 2 to Mode	1			0			
t_{en}	Clock enable time (see Figure 1)	CLK 1	13			12			ns
		CLK 2	13			12			
t_{in}	Clock inhibit time (see Figure 1)	CLK 1	3			2.5			ns
		CLK 2	1			0			
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS95			SN74AS95			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	Mode	V_{CC} = 5.5 V,	V_{IL} = 0.4 V			−1			−1	mA
	All other					−0.5			−0.5	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.35 V	−30		−112	−30		−112	mA
I_{CCH}		V_{CC} = 5.5 V			21	34		21	34	mA
I_{CCL}		V_{CC} = 5.5 V			26	39		26	39	mA

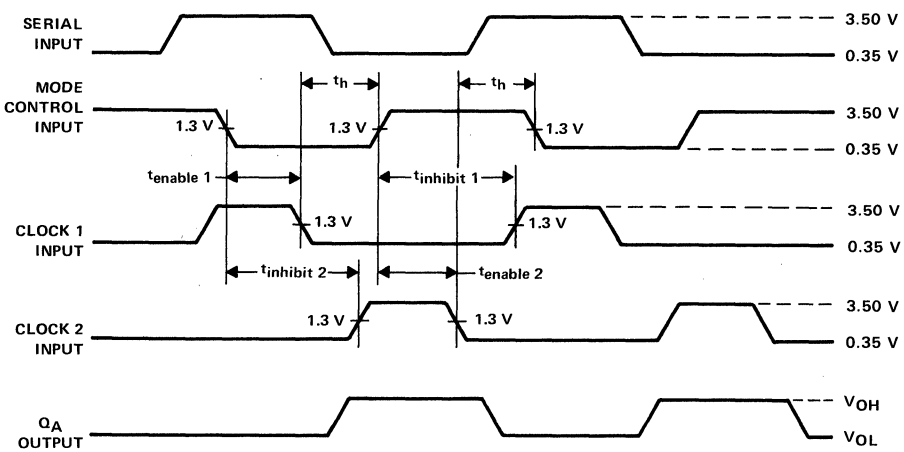
†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristice (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS95		SN74AS95		
			MIN	MAX	MIN	MAX	
f_{max}			80		100		MHz
t_{PLH}	CLK	Q	2	11	2	10	ns
t_{PHL}			2	10.5	2	9.5	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

FIGURE 1–CLOCK ENABLE, INHIBIT, AND HOLD TIMES

TEXAS INSTRUMENTS
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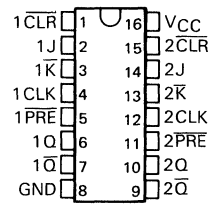
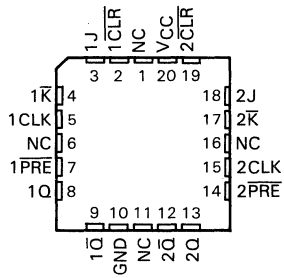
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION PER FLIP-FLOP
'ALS109A	50 MHz	6 mW
'AS109	129 MHz	29 mW

SN54ALS109A, SN54AS109 . . . J PACKAGE
SN74ALS109A, SN74AS109 . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS109A, SN54AS109 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

These devices contain two independent J-$\overline{K}$ positive-edge-triggered flip-flops. A low level at the Preset or Clear inputs sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the J and $\overline{K}$ input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and $\overline{K}$ inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by grounding $\overline{K}$ and trying J high. They also can perform as D-type flip-flops if J and $\overline{K}$ are tied together.

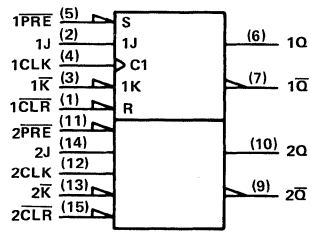
The SN54ALS109A and SN54AS109 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS109A and SN74AS109 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q_0	$\overline{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$

* The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} if the lows at Preset and Clear are near V_{IL} maximum. Furthermore, this configuration is nonstable; that is, it will not persist when either Preset or Clear returns to its inactive (high) level.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS109A, SN54AS109 . . . . . −55°C to 125°C
SN74ALS109A, SN74AS109 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS109A			SN74ALS109A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		30	0		34	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	15			15			ns
		CLK high	16.5			14.5			
		CLK low	16.5			14.5			
t_{su}	Setup time before CLK↑	Data	15			15			ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	10			10			
t_h	Hold time, data after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS109A			SN74ALS109A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	CLK, J, or $\overline{K}$	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	$\overline{PRE}$ or $\overline{CLR}$					0.2			0.2	
I_{IH}	CLK, J, or $\overline{K}$	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	$\overline{PRE}$ or $\overline{CLR}$					40			40	
I_{IL}	CLK, J or $\overline{K}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
	$\overline{PRE}$ or $\overline{CLR}$					−0.4			−0.4	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		2.4	4		2.4	4	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with J, $\overline{K}$, CLK, and $\overline{PRE}$ grounded, then with J, $\overline{K}$, CLK, and $\overline{CLR}$ grounded.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS109A		SN74ALS109A		
			MIN	MAX	MIN	MAX	
f_{max}			30		34		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	3	17	3	13	ns
t_{PHL}			5	17	5	15	
t_{PLH}	CLK	Q or $\overline{Q}$	5	21	5	16	ns
t_{PHL}			5	20	5	18	

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

recommended operating conditions

			SN54AS109			SN74AS109			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−2	mA
I_{OL}	Low-level output current				20			20	mA
f_{clock}	Clock frequency		0		90	0		105	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	4			4			ns
		CLK high	4			4			
		CLK low	5.5			5.5			
t_{su}	Setup time before CLK↑	Data	5.5			5.5			ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	2			2			
t_h	Hold time, data after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS109			SN74AS109			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.25	0.5		0.25	0.5	V
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	CLK, J or $\overline{K}$	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	$\overline{PRE}$ or $\overline{CLR}$					40			40	
I_{IL}	CLK, J or $\overline{K}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			0.5	mA
	$\overline{PRE}$ or $\overline{CLR}$					−1.8			−1.8	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		11.5	17		11.5	17	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with J, $\overline{K}$, CLK, and $\overline{PRE}$ grounded, then with J, $\overline{K}$, CLK, and $\overline{CLR}$ grounded.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS109		SN74AS109		
			MIN	MAX	MIN	MAX	
f_{max}			90		105		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	3	9	3	8	ns
t_{PHL}			3.5	11.5	3.5	10.5	
t_{PLH}	CLK	Q or $\overline{Q}$	3.5	10	3.5	9	ns
t_{PHL}			4.5	10.5	4.5	9	

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

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- **Fully Buffered to Offer Maximum Isolation from External Disturbance**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION PER FLIP-FLOP
'ALS112A	50 MHz	6 mW

description

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the Preset or Clear inputs sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the fall time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

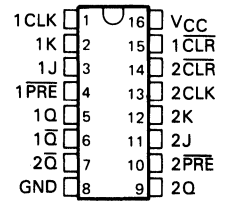
The SN54ALS112A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS112A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

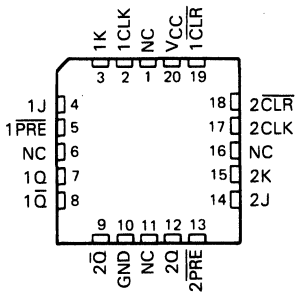
INPUTS					OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H†	H†
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q}_0$

†The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH}. Furthermore, this configuration is nonstable; that is, it will not persist when either Preset or Clear returns to its inactive (high) level.

SN54ALS112A . . . J PACKAGE
SN74ALS112A . . . D OR N PACKAGE
(TOP VIEW)

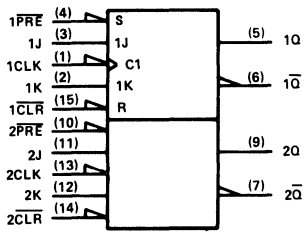


SN54ALS112A . . . FK PACKAGE
(TOP VIEW)



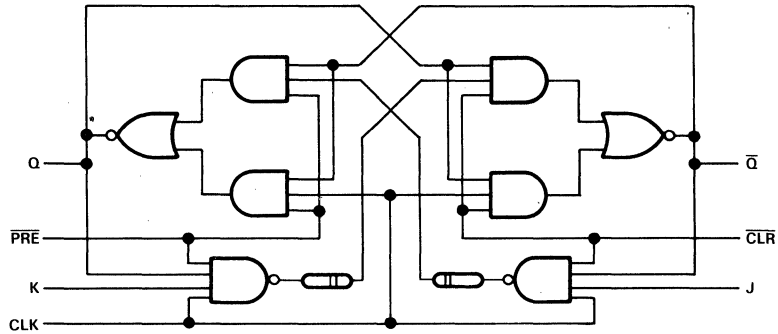
NC—No internal connection

logic symbol‡



‡This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS112A . . . . . −55°C to 125°C
SN74ALS112A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS112A			SN74ALS112A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		25	0		30	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	15			10			ns
		CLK high	20			16.5			
		CLK low	20			16.5			
t_{su}	Setup time before CLK↓	Data	25			22			ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	22			20			
t_h	Hold time, data after CLK↓		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

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electrical characteristice over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS112A			SN74ALS112A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V	I_{OL} = 8 mA					0.35	0.5	
I_I	J, K, or CLK	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	$\overline{PRE}$ or $\overline{CLR}$					0.2			0.2	
I_{IH}	J, K, or CLK	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	$\overline{PRE}$ or $\overline{CLR}$					40			40	
I_{IL}	J, K, or CLK	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
	$\overline{PRE}$ or $\overline{CLR}$					−0.4			−0.4	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		2.5	4.5		2.5	4.5	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with J, K, CLK, and $\overline{PRE}$ grounded, then with J, K, CLK, and $\overline{CLR}$ grounded.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS112A		SN74ALS112A		
			MIN	MAX	MIN	MAX	
f_{max}			25		30		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	3	26	3	15	ns
t_{PHL}			4	23	4	18	
t_{PLH}	CLK	Q or $\overline{Q}$	3	23	3	15	ns
t_{PHL}			5	24	5	19	

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

D2261, APRIL 1982—REVISED MAY 1986

- **Fully Buffered to Offer Maximum Isolation from External Disturbance**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION PER FLIP-FLOP
'ALS113A	40 MHz (C_L = 15 pF)	6 mW

description

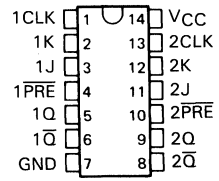
These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the Preset input sets the outputs regardless of the levels of the other inputs. When Preset ($\overline{PRE}$) is inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the fall time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

The SN54ALS113A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS113A is characterized for operation from 0°C to 70°C.

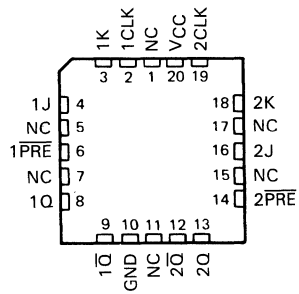
FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{PRE}$	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	H	L
H	↓	L	L	Q_0	$\overline{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\overline{Q}_0$

SN54ALS113A . . . J PACKAGE
SN74ALS113A . . . D OR N PACKAGE
(TOP VIEW)

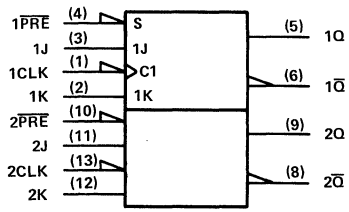


SN54ALS113A . . . FK PACKAGE
(TOP VIEW)



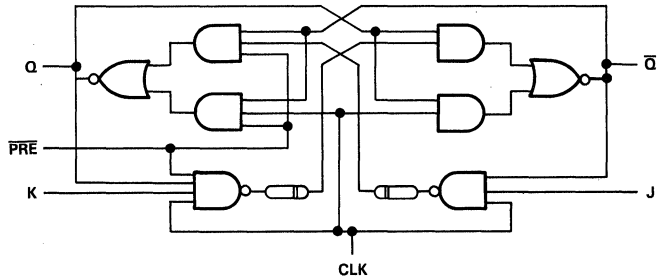
NC—No internal connection

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS113A . . . . . −55°C to 125°C
SN74ALS113A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS113A			SN74ALS113A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		25	0		30	MHz
t_w	Pulse duration	$\overline{PRE}$ low	20			10			ns
		CLK high	20			16.5			
		CLK low	20			16.5			
t_{su}	Setup time before CLK↓	Data	25			22			ns
		$\overline{PRE}$ inactive	25			20			
t_h	Hold time, data after CLK↓		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS113A			SN74ALS113A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = 0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	J, K, or CLK	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	$\overline{PRE}$					0.2			0.2	
I_{IH}	J, K, or CLK	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	$\overline{PRE}$					40			40	
I_{IL}	J, K, or CLK	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
	$\overline{PRE}$					−0.4			−0.4	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		2.5	4.5		2.5	4.5	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with J, K, CLK, and $\overline{PRE}$ grounded, then with J, K, CLK, and $\overline{CLR}$ grounded.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS113A		SN74ALS113A		
			MIN	MAX	MIN	MAX	
f_{max}			25		30		MHz
t_{PLH}	$\overline{PRE}$	Q or $\overline{Q}$	3	23	3	14	ns
t_{PHL}			4	26	4	16	
t_{PLH}	CLK	Q or $\overline{Q}$	3	22	3	15	ns
t_{PHL}			5	23	5	19	

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

D2661, DECEMBER 1982—REVISED MAY 1986

- **Fully Buffered to Offer Maximum Isolation from External Disturbance**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Typical Maximum Clock Frequency . . . 40 MHz**
- **Typical Power Dissipation per Flip-Flop . . . 6 mW**
- **Dependable Texas Instruments Quality and Reliability**

description

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the Preset or Clear inputs sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the fall time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

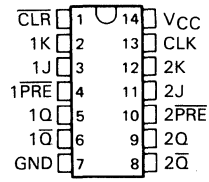
The SN54ALS114A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS114A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

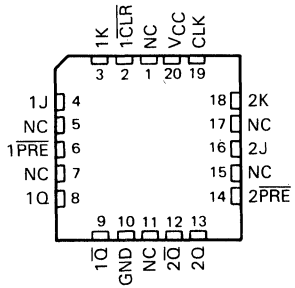
INPUTS					OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q}_0$

* The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} if the lows at Preset and Clear are near V_{IL} maximum. Furthermore, this configuration is nonstable; that is, it will not persist when either Preset or Clear returns to its inactive (high) level.

SN54ALS114A . . . J PACKAGE
SN74ALS114A . . . D OR N PACKAGE
(TOP VIEW)

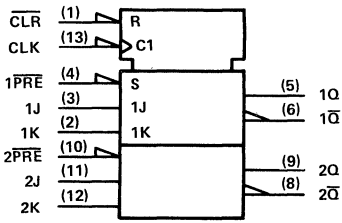


SN54ALS114A . . . FK PACKAGE
(TOP VIEW)



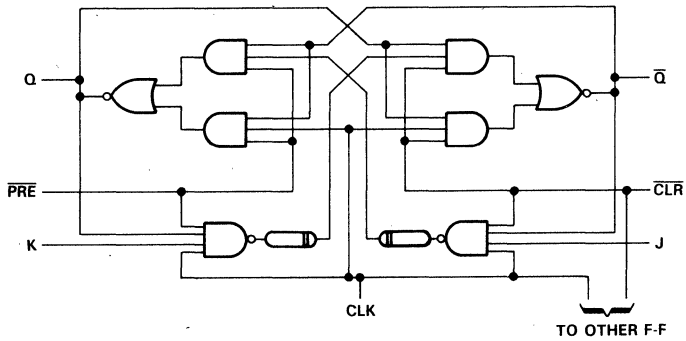
NC—No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers are for D, J, and N packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS114A . . . . . −55°C to 125°C
SN74ALS114A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS114A			SN74ALS114A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		25	0		30	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	20			10			ns
		CLK high	20			16.5			
		CLK low	20			16.5			
t_{su}	Setup time before CLK↓	Data	25			22			ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	25			20			
t_h	Hold time, data after CLK↓		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS114A			SN74ALS114A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4				V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	J, K, or CLK	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	$\overline{PRE}$ or $\overline{CLR}$					0.2			0.2	
I_{IH}	J, K, or CLK	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	$\overline{PRE}$ or $\overline{CLR}$					40			40	
I_{IL}	J, K, or CLK	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
	$\overline{PRE}$ or $\overline{CLR}$					−0.4			−0.4	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		2.5	4.5		2.5	4.5	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with J, K, CLK, and $\overline{PRE}$ grounded, then with J, K, CLK, and $\overline{CLR}$ grounded.

switching characteristics (see Note 2)

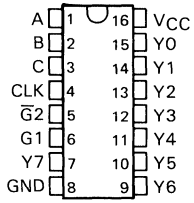
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS114A		SN74ALS114A		
			MIN	MAX	MIN	MAX	
f_{max}			25		30		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	3	29	3	15	ns
t_{PHL}			4	30	4	18	
t_{PLH}	CLK	Q or $\overline{Q}$	3	28	3	15	ns
t_{PHL}			5	31	5	19	

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

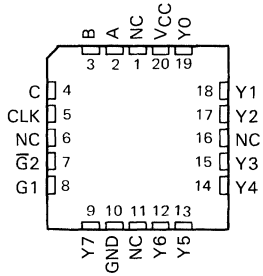
D2661, APRIL 1982—REVISED MAY 1986

- **Combines Decoder and 3-Bit Address Register**
- **Incorporates 2 Enable Inputs to Simplify Cascading**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS131, SN54AS131A . . . J PACKAGE
SN74ALS131, SN74AS131A . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS131, SN54AS131A . . . FK PACKAGE
(TOP VIEW)



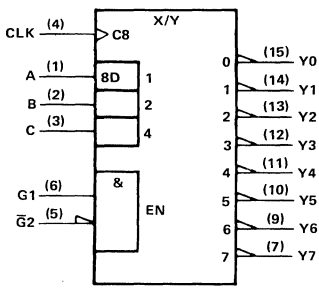
NC—No internal connection

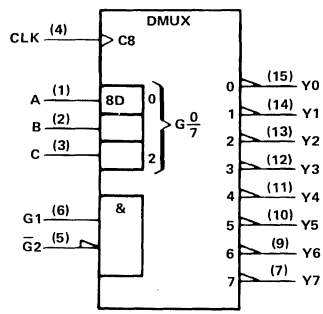
description

The 'ALS131 and 'AS131A are three-line to eight-line decoder/demultiplexer with registers on the three address inputs. When the clock input (CLK) goes from low to high, the 'ALS131 and 'AS131A act as decoders/demultiplexers and the address present at the select inputs (A, B, and C) is stored in the registers. Further address changes are ignored until the next rising transition of CLK. The output enable controls, G1 and $\overline{G}2$, control the state of the outputs independently of the select or CLK inputs. All of the outputs are high unless G1 is high and $\overline{G}2$ is low. The 'ALS131 and 'ALS131A are ideally suited for implementing glitch-free decoders in strobed (stored-address) applications in bus-oriented systems.

The SN54ALS131 and SN54AS131A are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS131 and SN74AS131A are characterized for operation from 0°C to 70°C.

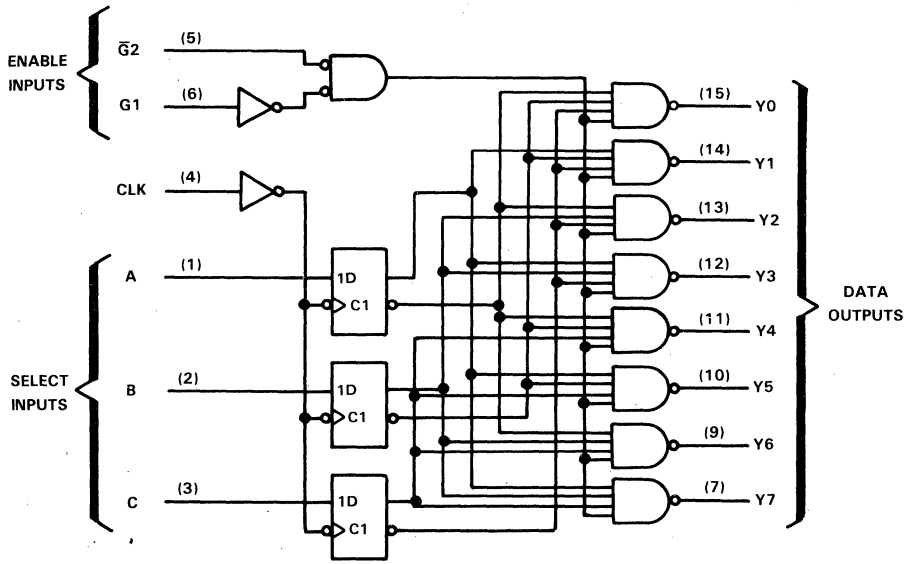
logic symbols† (alternatives)





†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

FUNCTION TABLE

INPUTS						OUTPUTS							
CLK	ENABLE		SELECT										
	G1	$\overline{G2}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
↑	H	L	L	L	L	L	H	H	H	H	H	H	H
↑	H	L	L	L	H	H	L	H	H	H	H	H	H
↑	H	L	L	H	L	H	H	L	H	H	H	H	H
↑	H	L	L	H	H	H	H	H	L	H	H	H	H
↑	H	L	H	L	L	H	H	H	H	L	H	H	H
↑	H	L	H	L	H	H	H	H	H	H	L	H	H
↑	H	L	H	H	L	H	H	H	H	H	H	L	H
↑	H	L	H	H	H	H	H	H	H	H	H	H	L
L or H	H	L	X	X	X	OUTPUTS CORRESPONDING TO STORED ADDRESS, L; ALL OTHERS, H							

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS131, SN54AS131A . . . . . −55°C to 125°C
SN74ALS131, SN74AS131A . . . . . 0°C to 70°C
Storage temperature . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS131			SN74ALS131			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		40	0		50	MHz
t_w	Pulse duration	CLK high	12.5			10			ns
		CLK low	12.5			10			
t_{su}	Setup time at A, B, and C before CLK↑		15			10			ns
t_h	Hold time at A, B, and C after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS131			SN74ALS131			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V			5	11		5	11	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS131		SN74ALS131		
			MIN	MAX	MIN	MAX	
f_{max}			40		50		MHz
t_{PLH}	CLK	Y	8	28	8	25	ns
t_{PHL}			7	24	7	20	
t_{PLH}	G1	Y	7	24	7	20	ns
t_{PHL}			6	20	6	17	
t_{PLH}	$\overline{G2}$	Y	5	18	5	15	ns
t_{PHL}			5	18	5	15	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

recommended operating conditions

			SN54AS131A			SN74AS131A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−2	mA
I_{OL}	Low-level output current				20			20	mA
f_{clock}	Clock frequency		0		90	0		100	MHz
t_w	Pulse duration	CLK high	5.5			5			ns
		CLK low	5.5			5			
t_{su}	Setup time at A, B, and C before CLK↑		3.5			3.5			ns
t_h	Hold time at A, B, and C after CLK↑		1			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS131A			SN74AS131A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V			15	29		15	29	mA
I_{CCL}	V_{CC} = 5.5 V			16	30		16	30	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS131A		SN74AS131A		
			MIN	MAX	MIN	MAX	
f_{max}			90		100		MHz
t_{PLH}	CLK	Y	2	15	2	14.5	ns
t_{PHL}			2	10	2	9.5	
t_{PLH}	G1	Y	2	10.5	2	10	ns
t_{PHL}			2	9	2	9	
t_{PLH}	$\overline{G2}$	Y	2	7.5	2	7	ns
t_{PHL}			2	8.5	2	8.5	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

D2661, APRIL 1982—REVISED MAY 1986

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These devices contain a single 13-input NAND gate. They perform the Boolean functions in positive logic:

$$Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H \cdot I \cdot J \cdot K \cdot L \cdot M}$$

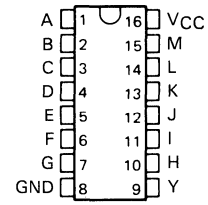
$$Y = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F} + \overline{G} + \overline{H} + \overline{I} + \overline{J} + \overline{K} + \overline{L} + \overline{M}$$

The SN54ALS133 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS133 is characterized for operation from 0°C to 70°C.

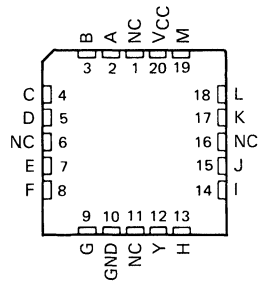
FUNCTION TABLE

INPUTS A THRU M	OUTPUT Y
All inputs H	L
One or more inputs L	H

SN54ALS133 . . . J PACKAGE
SN74ALS133 . . . D OR N PACKAGE
(TOP VIEW)

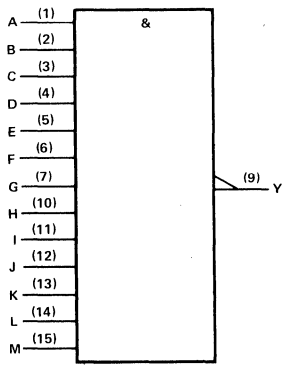


SN54ALS133 . . . FK PACKAGE
(TOP VIEW)



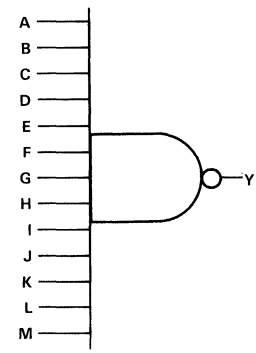
NC—No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS133 . . . . . −55°C to 125°C
SN74ALS133 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS133			SN74ALS133			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating-free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS133			SN74ALS133			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.24	0.34		0.24	0.34	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		0.56	0.8		0.56	0.8	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS133	SN54ALS133		SN74ALS133		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	8	1	16	3	11	ns
t_{PHL}	Any	Y	17	5	47	5	25	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
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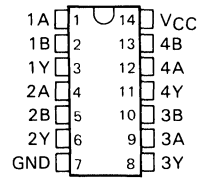
SN54ALS136, SN54AS136, SN74ALS136, SN74AS136
QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES
WITH OPEN-COLLECTOR OUTPUTS

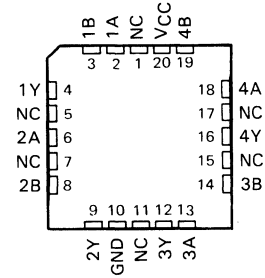
D2837, MARCH 1984—REVISED MAY 1986

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS136, SN54AS136 . . . J PACKAGE
SN74ALS136, SN74AS136 . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS136, SN54AS136 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

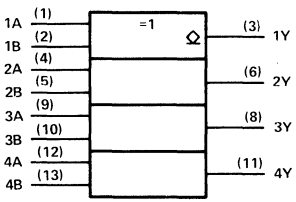
description

These devices contain four independent Exclusive-OR gates with open-collector outputs. They perform the Boolean functions $Y = A \oplus B = \overline{A}B + A\overline{B}$ in positive logic.

A common application is a true/complement element. If one of the inputs is low, the other input will be reproduced in true form at the output. If one of the inputs is high, the signal on the other input will be reproduced inverted at the output.

The SN54ALS136 and SN54AS136 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS136 and SN74AS136 are characterized for operation from 0°C to 70°C.

logic symbol†



FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

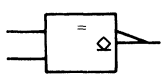
exclusive-OR logic

An Exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.

EXCLUSIVE-OR

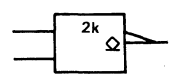
These are five equivalent Exclusive-OR symbols valid for an 'ALS136 gate in positive logic; negation may be shown at any two ports.

LOGIC IDENTITY ELEMENT



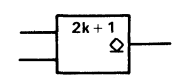
The output is active (low) if all inputs stand at the same logic level (i.e., A = B).

EVEN-PARITY



The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

ODD-PARITY ELEMENT



The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS136 . . . . . −55°C to 125°C
SN74ALS136 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS136			SN74ALS136			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS136			SN74ALS136			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_{CC}	V_{CC} = 5.5 V,	All inputs at 4.5 V		3.9	5.9		3.9	5.9	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 2 kΩ, T_A = MIN to MAX				UNIT
			SN54ALS136		SN74ALS136		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	20	55	20	50	ns
t_{PHL}	(other input low)		3	18	3	15	
t_{PLH}	A or B	Y	20	55	20	50	ns
t_{PHL}	(other input high)		3	15	3	12	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
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SN54AS136, SN74AS136 QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES WITH OPEN-COLLECTOR OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54AS136 . . . . . −55°C to 125°C
SN74AS136 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS136			SN74AS136			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS86			SN74AS86			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			2			2	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−01			−0.1	mA
I_{CCH}	V_{CC} = 5.5 V			18			18		mA
I_{CCL}	V_{CC} = 5.5 V			15			15		mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics (see Note 1)

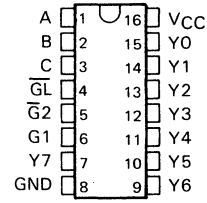
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 2 kΩ, T_A = MIN to MAX						UNIT
			SN54AS136			SN74AS136			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A or B (other input low)	Y		10.5			10.5		ns
t_{PHL}				4.3			4.3		
t_{PLH}	A or B (other input high)	Y		10.5			10.5		ns
t_{PHL}				4.3			4.3		

† All typical valves are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

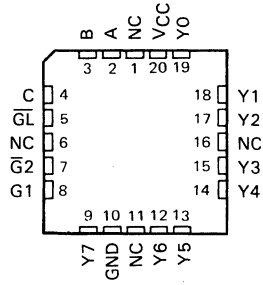
D2661, APRIL 1982—REVISED MAY 1986

- **Combines Decoder and 3-Bit Address Latch**
- **Incorporates 2 Output Enables to Simplify Cascading**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS137, SN54AS137 . . . J PACKAGE
SN74ALS137, SN74AS137 . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS137, SN54AS137 . . . FK PACKAGE
(TOP VIEW)



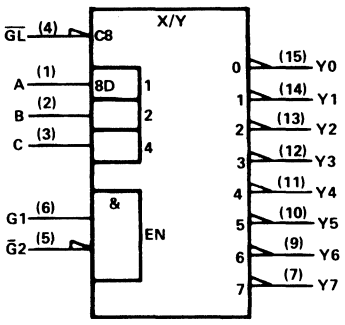
NC—No internal connection

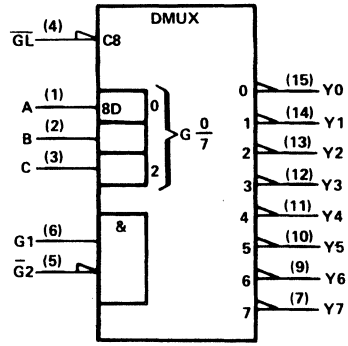
description

The 'ALS137 and 'AS137 are three-line to eight-line decoder/demultiplexer with latches on the three address inputs. When the latch-enable input ($\overline{GL}$) is low, the 'ALS137 and 'AS137 acts as a decoder/demultiplexer. When $\overline{GL}$ goes from low to high, the address present at the select inputs (A, B, and C) is stored in the latches. Further address changes are ignored as long as $\overline{GL}$ remains high. The output enable controls, G1 and $\overline{G2}$, control the outputs independently of the select or latch-enable inputs. All of the outputs are forced high if G1 is low or $\overline{G2}$ is high. The 'ALS137 and 'AS137 are ideally suited for implementing glitch-free decoders in strobed (stored-address) applications in bus-oriented systems.

The SN54ALS137 and SN54AS137 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS137 and SN74AS137 are characterized for operation from 0°C to 70°C.

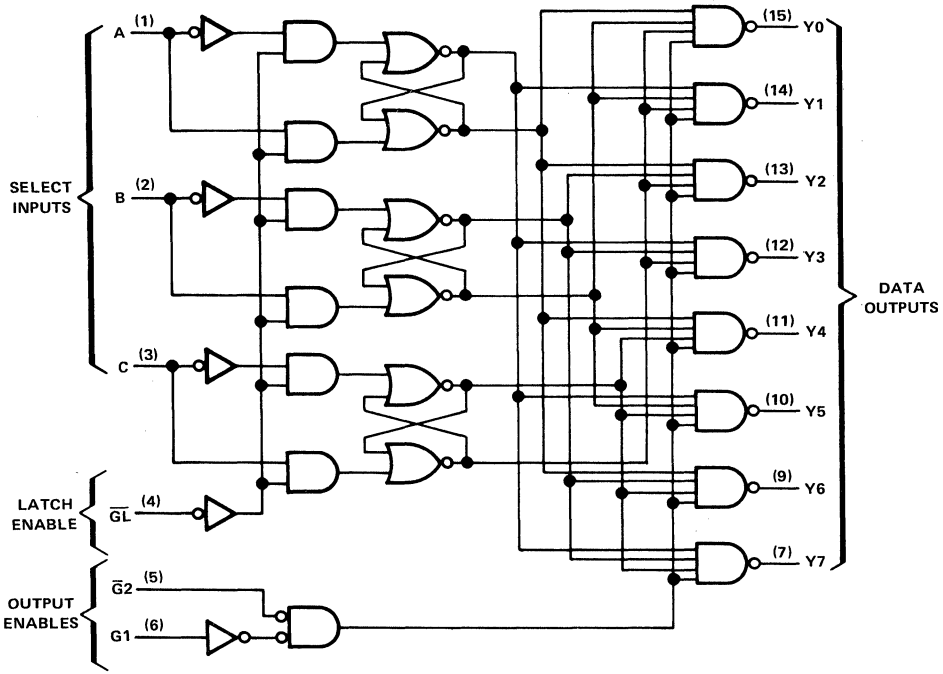
logic symbols (alternatives)†





†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

FUNCTION TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT										
$\overline{G}L$	G1	$\overline{G}2$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	H	H	L
H	H	L	X	X	X	Output corresponding to stored address, L; all others, H							

TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS137, SN54AS137 . . . . . −55°C to 125°C
SN74ALS137, SN74AS137 . . . . . 0°C to 70°C
Storage temperature . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS137			SN74ALS137			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
t_w	Pulse duration, $\overline{GL}$ low	15			10			ns
t_{su}	Setup time at A, B, and C before $\overline{GL}$↑	15			10			ns
t_h	Hold time at A, B, and C after $\overline{GL}$↑	5			5			ns
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS137			SN74ALS137			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V			5	11		5	11	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS137		SN74ALS137		
			MIN	MAX	MIN	MAX	
t_{PLH}	A, B, C	Y	5	25	5	20	ns
t_{PHL}			6	25	6	20	
t_{PLH}	$\overline{G2}$	Y	4	15	4	12	ns
t_{PHL}			5	18	5	15	
t_{PLH}	G1	Y	5	21	5	17	ns
t_{PHL}			5	19	5	15	
t_{PLH}	$\overline{GL}$	Y	7	27	7	22	ns
t_{PHL}			7	25	7	20	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

recommended operating conditions

		SN54AS137			SN74AS137			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
t_w	Pulse duration, $\overline{GL}$ low	5			4.5			ns
t_{su}	Setup times at A, B, and C before $\overline{GL}$↑	4.5			4			ns
t_h	Hold time at A, B, and C after $\overline{GL}$↑	1			1			ns
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS137			SN74AS137			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC} −2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−1			−1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V			15	24		15	24	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

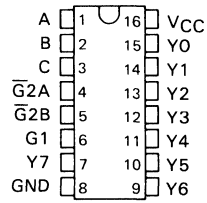
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS137		SN74AS137		
			MIN	MAX	MIN	MAX	
t_{PLH}	A, B, C	Y	2	14	2	12.5	ns
t_{PHL}			2	14	2	12.5	
t_{PLH}	$\overline{G2}$	Y	2	9	2	8	ns
t_{PHL}			2	9	2	8.5	
t_{PLH}	G1	Y	2	11	2	10	ns
t_{PHL}			2	10	2	9	
t_{PLH}	$\overline{GL}$	Y	2	14.5	3	13.5	ns
t_{PHL}			2	15	3	14	

NOTE 1. Load circuit and voltage waveforms are shown in Section 1.

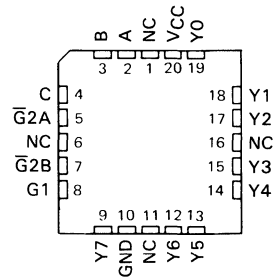
D2661, APRIL 1982—REVISED MAY 1986

- **Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems**
- **Incorporates 3 Enable Inputs to Simplify Cascading and/or Data Reception**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS138, SN54AS138 . . . J PACKAGE
SN74ALS138, SN74AS138 . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS138, SN54AS138 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

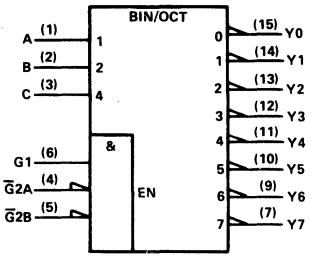
description

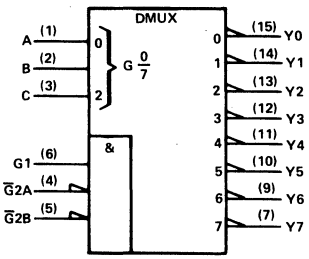
The 'ALS138 and 'AS138 circuits are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems this decoder can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the Schottky-clamped system decoder is negligible.

The conditions at the binary select inputs and the three enable inputs select one of eight input lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

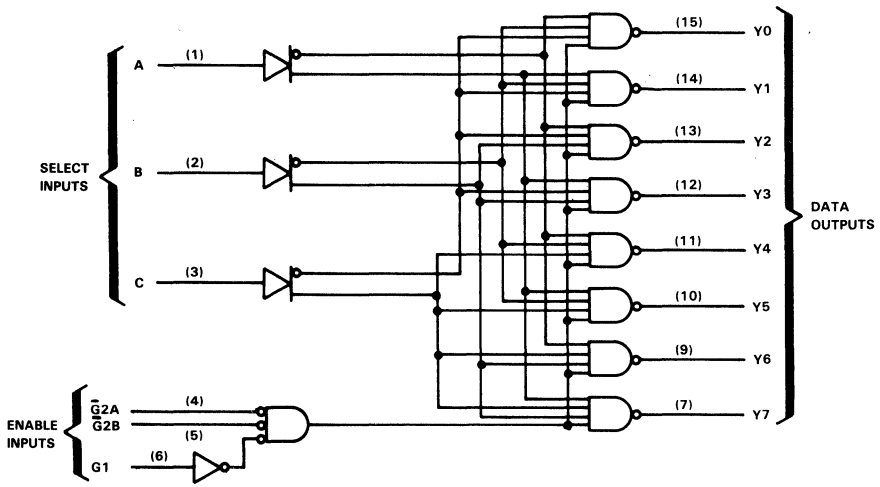
The SN54ALS138 and SN54AS138 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS138 and SN74AS138 are characterized for operation from 0°C to 70°C.

logic symbols (alternatives)†





logic diagram (positive logic)



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

FUNCTION TABLE

ENABLE INPUTS			SELECT INPUTS			OUTPUTS							
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range; SN54ALS138, SN54AS138 . . . . . −55°C to 125°C
SN74ALS138, SN74AS138 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS138			SN74ALS138			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS138			SN74ALS138			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V			5	10		5	10	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS138		SN74ALS138		
			MIN	MAX	MIN	MAX	
t_{PLH}	A, B, C	Any Y	2	28	6	22	ns
t_{PHL}			6	22	6	18	
t_{PLH}	Enable	Any Y	2	22	4	17	ns
t_{PHL}			4	21	5	17	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

recommended operating conditions

		SN54AS138			SN74AS138			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS138			SN74AS138			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V			12	17.5		12	17.5	mA
I_{CCL}	V_{CC} = 5.5 V			14	20		14	20	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

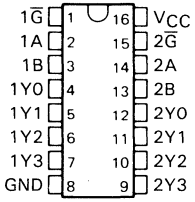
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS138		SN74AS138		
			MIN	MAX	MIN	MAX	
t_{PLH}	A, B, C	Any Y	2	11	2	10	ns
t_{PHL}			2	11	2	9.5	
t_{PLH}	G1	Any Y	2	11.5	2	10	ns
t_{PHL}			2	11	2	10	
t_{PLH}	$\overline{G2}$	Any Y	2	9	2	7.5	
t_{PHL}			2	10	2	8.5	

NOTE 1. Load circuit and voltage waveforms are shown in Section 1.

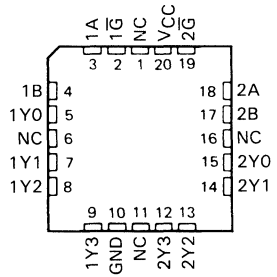
D2661, APRIL 1982—REVISED MAY 1986

- **Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems**
- **Incorporates 2 Enable Inputs to Simplify Cascading and/or Data Reception**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS139, SN54AS139 . . . J PACKAGE
SN74ALS139, SN74AS139 . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS139, SN54AS139 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

The 'ALS139 and 'AS139 circuits are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast-enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the Schottky-clamped system decoder is negligible.

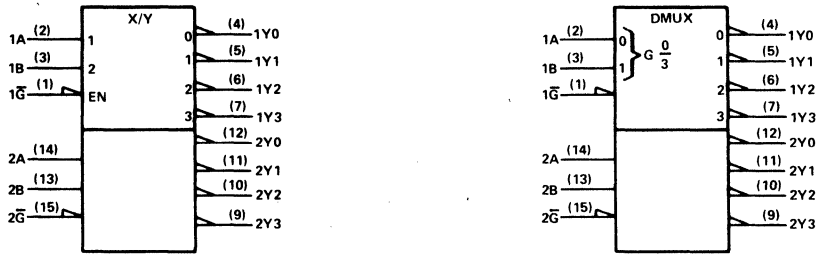
The 'ALS139 and 'AS139 are comprised of two individual two-line to four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications. These decoders/demultiplexers feature fully buffered inputs, each of which represents only one normalized load to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and simplify system design.

The SN54ALS139 and SN54AS139 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS139 and SN74AS139 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

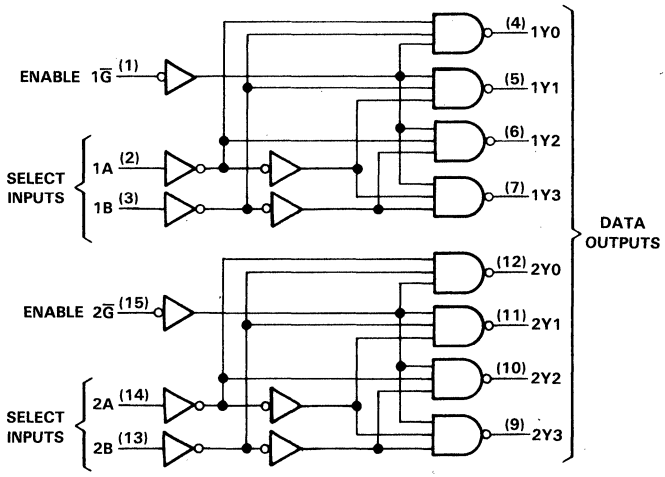
INPUTS			OUTPUTS			
ENABLE	SELECT					
$\overline{G}$	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

logic symbols† (alternatives)



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pins numbers shown are for D, J, and N packages.

functional block diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS139, SN54AS139 . . . . . −55°C to 125°C
SN74ALS139, SN74AS139 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

TEXAS INSTRUMENTS
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recommended operating conditions

		SN54ALS139			SN74ALS139			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS139			SN74ALS139			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V			8	13		8	13	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS139	SN54ALS139		SN74ALS139		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	9	3	17	3	14	ns
t_{PHL}			9	3	17	3	14	
t_{PLH}	$\overline{G}$	Y	9	3	17	3	14	ns
t_{PHL}			9	3	18	3	15	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

recommended operating conditions

		SN54AS139			SN74AS139			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS139			SN74AS139			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V			13			13		mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L1 = 50 Ω, T_A = MIN to MAX						UNIT
			SN54AS139			SN74AS139			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A or B	Y		5.5			5.5		ns
t_{PHL}				6			6		
t_{PLH}	$\overline{G}$	Y		5.5			5.5		ns
t_{PHL}				5			5		

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

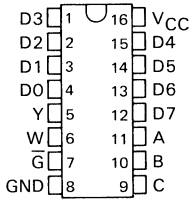
Additional information on these products can be obtained from the factory as it becomes available.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

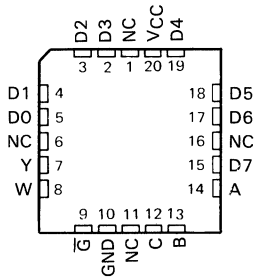
D2661, APRIL 1982—REVISED MAY 1986

- 8-Line to 1-Line Multiplexers Can Perform As:
  - Boolean Function Generators
  - Parallel-to-Serial Converters
  - Data Source Selectors
- Input Clamping Diodes Simplify System Design
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS151, SN54AS151 . . . J PACKAGE
SN74ALS151, SN74AS151 . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS151, SN54AS151 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

These monolithic data selectors/multiplexers provide full binary decoding to select one of eight data sources. The strobe input ($\overline{G}$) must be at a low logic level to enable the inputs. A high level at the strobe terminal forces the W output high and the Y output low.

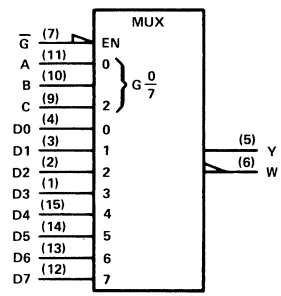
The SN54ALS151 and SN54AS151 are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS151 and SN74AS151 are characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE

INPUTS				OUTPUTS	
SELECT			STROBE		
C	B	A	$\overline{G}$	Y	W
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

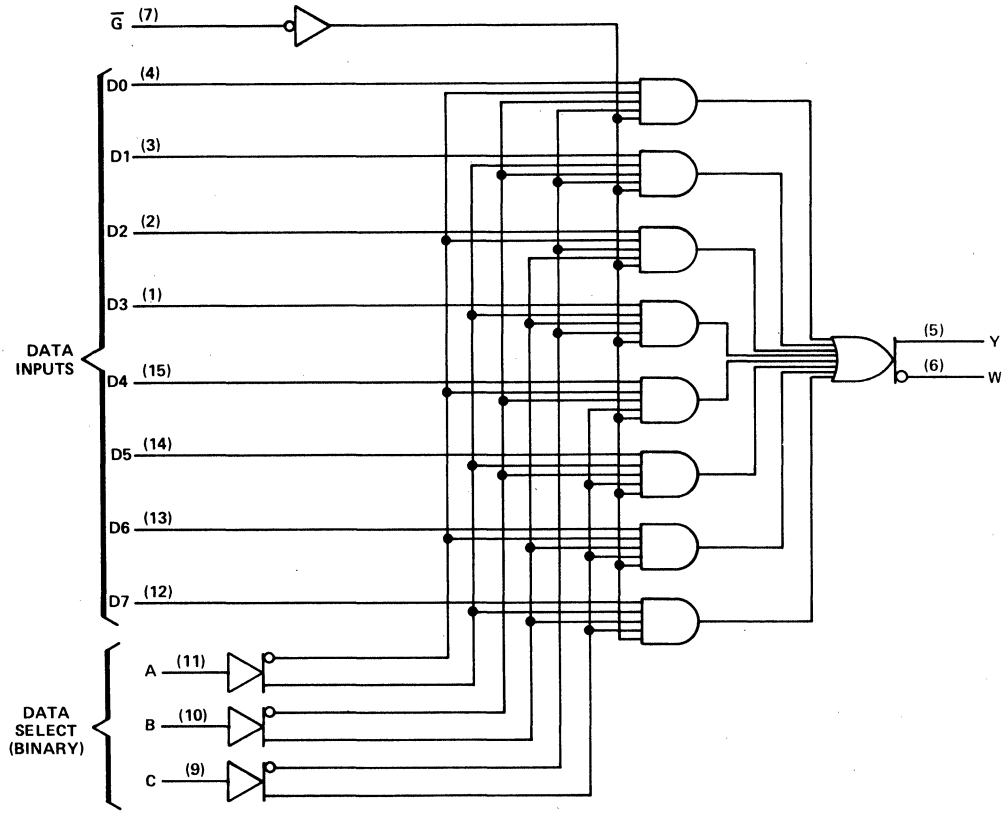
H = high level, L = low level, X = irrelevant
D0, D1 . . . D7 = the level of the D respective input

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS151, SN54AS151 . . . . . −55 °C to 125 °C
SN74ALS151, SN74AS151 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150°C

recommended operating conditions

		SN54ALS151			SN74ALS151			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS151			SN74ALS151			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V,	Inputs at 4.5 V		7.5	12		7.5	12	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS151		SN74ALS151		
			MIN	MAX	MIN	MAX	
t_{PLH}	A, B, or C	Y	4	21	4	18	ns
t_{PHL}			8	35	8	24	
t_{PLH}	A, B, or C	W	7	36	7	24	ns
t_{PHL}			7	26	7	23	
t_{PLH}	Any D	Y	3	14	3	10	ns
t_{PHL}			5	21	5	15	
t_{PLH}	Any D	W	3	23	3	15	ns
t_{PHL}			4	20	4	15	
t_{PLH}	$\overline{G}$	Y	4	21	4	18	ns
t_{PHL}			4	25	4	19	
t_{PLH}	$\overline{G}$	W	5	27	5	19	ns
t_{PHL}			5	26	5	23	

NOTE 1. Load circuit and voltage waveforms are shown in Section 1.

recommended operating conditions

		SN54AS151			SN74AS151			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			32			48	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS151			SN74AS151			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2					
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4	3.3		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_I	A, B, or C	V_{CC} = 5.5 V,	V_I = 7 V			0.2			0.2	mA
	All others					0.1			0.1	
I_{IH}	A, B, or C	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	μA
	All others					20			20	
I_{IL}	A, B, or C	V_{CC} = 5.5 V,	V_I = 0.4 V			−1			−1	mA
	All others					−0.5			−0.5	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,			18.6	30		18.6	30	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS151		SN74AS151		
			MIN	MAX	MIN	MAX	
t_{PLH}	A, B, or C	Y	4.5	16	4.5	14.5	ns
t_{PHL}			4.5	16	4.5	15	
t_{PLH}	A, B, or C	W	4	14.5	4	12	ns
t_{PHL}			4	14.5	4	12	
t_{PLH}	Any D	Y	3	11.5	3	10.5	ns
t_{PHL}			3	12	3	11	
t_{PLH}	Any D	W	2	8	2	6.5	ns
t_{PHL}			1	5.5	1	4.5	
t_{PLH}	$\overline{G}$	Y	4.5	16	4.5	14	ns
t_{PHL}			3	12.5	3	11	
t_{PLH}	$\overline{G}$	W	1.5	7	1.5	6	ns
t_{PHL}			3	11	3	10	

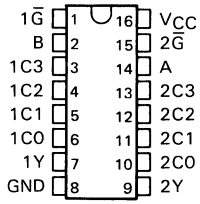
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

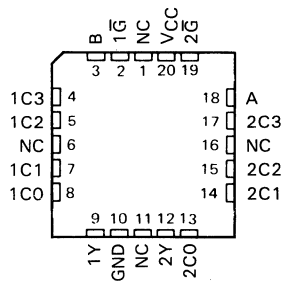
D2661, APRIL 1982—REVISED MAY 1986

- **Permits Multiplexing from N Lines to 1 Line**
- **Performs Parallel-to-Serial Conversion**
- **Strobe (Enable) Line Provided for Cascading (N lines to n lines)**
- **'ALS253 and 'AS253 Are 3-State Versions of These Parts**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS153, SN54AS153 . . . J PACKAGE
SN74ALS153, SN74AS153 . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS153, SN54AS153 . . . FK PACKAGE
(TOP VIEW)



NC — No internal connection

description

Each of these data selectors/multiplexers contains inverters and drivers to supply full binary decoding data selection to the AND-OR gates. Separate strobe inputs (G) are provided for each of the two four-line sections.

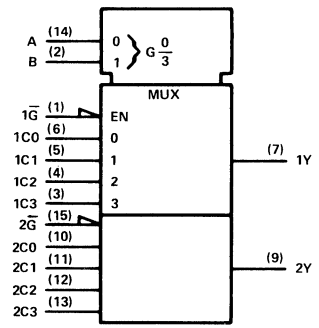
The SN54ALS153 and SN54AS153 are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS153 and SN74AS153 are characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	$\overline{G}$	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

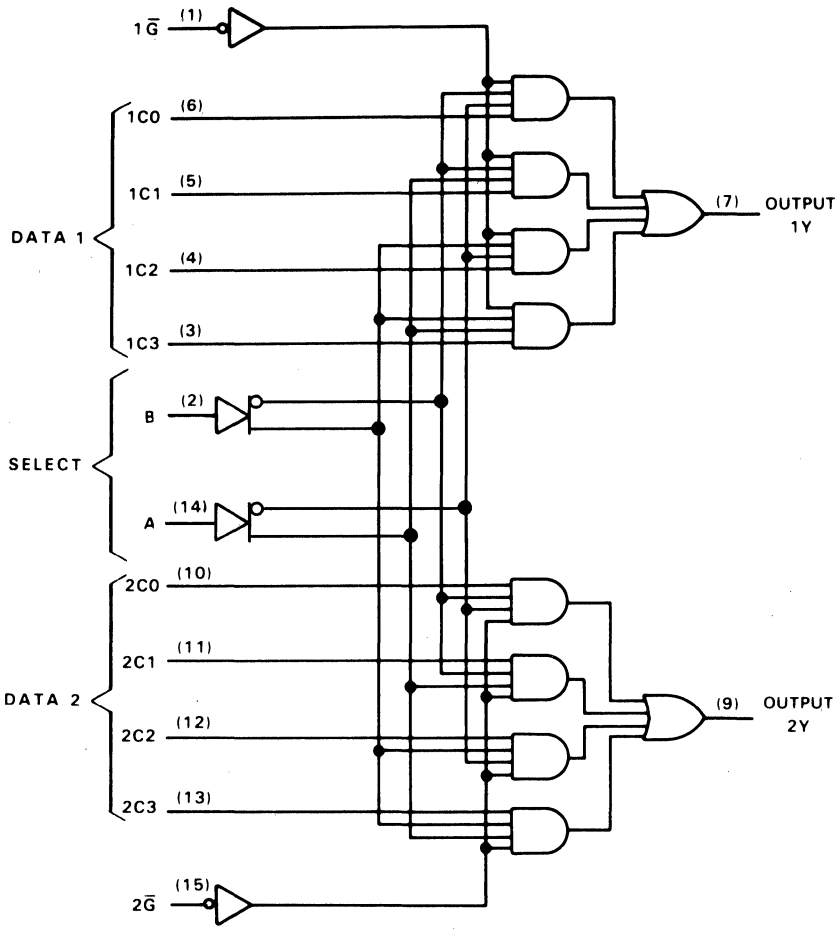
Select inputs A and B are common to both sections.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS153, SN54AS153 . . . . . −55 °C to 125 °C
SN74ALS153, SN74AS153 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS153			SN74ALS153			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS153			SN74ALS153			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V,	All inputs at 4.5 V		7.5	14		7.5	14	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS153		SN74ALS153		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	5	29	5	21	ns
t_{PHL}			5	27	5	21	
t_{PLH}	Data (Any C)	Y	3	15	3	10	ns
t_{PHL}			2	18	4	15	
t_{PLH}	G	Y	5	27	5	18	ns
t_{PHL}			3	22	5	18	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

recommended operating conditions

		SN54AS153			SN74AS153			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			32			48	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS153			SN74AS153			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2					
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4	3.3		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5				V
		V_{CC} = 4.5 V	I_{OL} = 48 mA					0.35	0.5	
I_I	A, B	V_{CC} = 5.5 V,	V_I = 7 V			0.2			0.2	mA
	All others					0.1			0.1	
I_{IH}	A, B	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	μA
	All others					20			20	
I_{IL}	A, B	V_{CC} = 5.5 V,	V_I = 0.4 V			−1			−1	mA
	All others					−0.5			−0.5	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	Outputs high		16	26		16	26	mA
			Outputs low		21	33		21	33	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS153		SN74AS153		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	3	14	3	12.5	ns
t_{PHL}			3	12.5	3	11	
t_{PLH}	Data (Any C)	Y	2	8	2	7	ns
t_{PHL}			2	8.5	2	8	
t_{PLH}	$\overline{G}$	Y	3	13	3	11.5	ns
t_{PHL}			2	10	2	9	

NOTE 1. Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

- **Applications:**
  Dual 2-Line to 4-Line Decoder
  Dual 1-Line to 4-Line Demultiplexer
  3-Line to 8-Line Decoder
  1-Line to 8-Line Demultiplexer
- **Individual Strobes Simplify Cascading for Decoding or Demultiplexing Larger Words**

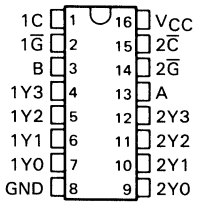
description

The 'ALS156 circuits feature dual 1-line to 4-line demultiplexers with individual strobes and common binary-address inputs in a single 16-pin package. When both sections are enabled, the common binary-address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit enabling or disabling each of the 4-bit sections as desired.

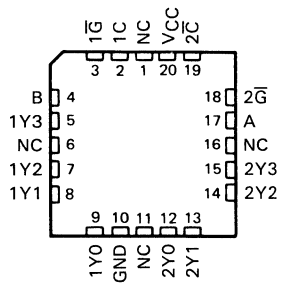
Data applied to input 1C is inverted at its outputs and data applied at input $2\overline{C}$ is not inverted through its outputs. The inverter following the 1C data input permits use of the 'ALS156 as a 3-line to 8-line demultiplexer without external gating. All inputs are clamped with high-performance Schottky diodes to suppress line ringing and simplify system design.

The SN74ALS156 is characterized for operation from 0°C to 70°C.

D OR N PACKAGE
(TOP VIEW)

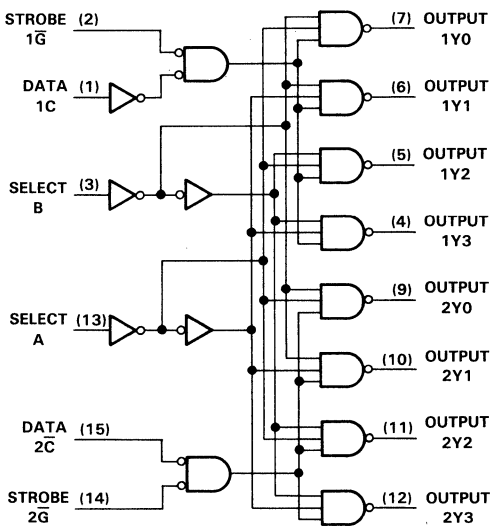


FN PACKAGE
(TOP VIEW)



NC—No internal connection

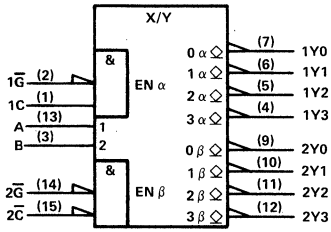
logic diagram (positive logic)



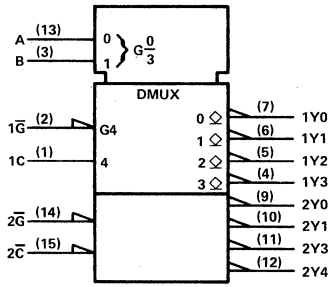
SN74ALS156
DUAL 2-LINE TO 4-LINE DECODER/DEMULTIPLEXER WITH OPEN-COLLECTOR OUTPUTS

logic symbols† (alternatives)

2-LINE TO 4-LINE DECODER



1-LINE TO 4-LINE DEMULTIPLEXER



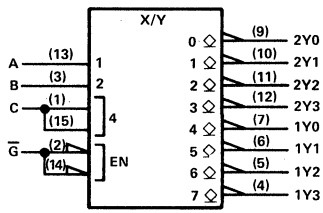
FUNCTION TABLE

2-LINE TO 4-LINE DECODER
OR
1-LINE TO 4-LINE DEMULTIPLEXER

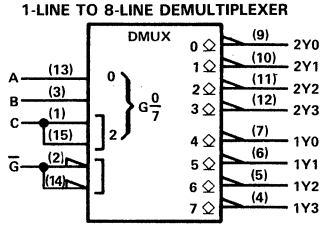
INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	$1\overline{G}$	1C	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	$2\overline{G}$	$2\overline{C}$	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

3-LINE TO 8-LINE DECODER



1-LINE TO 8-LINE DEMULTIPLEXER



FUNCTION TABLE

3-LINE TO 8-LINE DECODER
OR
1-LINE TO 8-LINE DEMULTIPLEXER

INPUTS				OUTPUTS							
SELECT			STROBE OR DATA	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C‡	B	A	$\overline{G}$§	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

‡ C = inputs 1C and $2\overline{C}$ connected together
§ $\overline{G}$ = inputs $1\overline{G}$ and $2\overline{G}$ connected together

† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown on logic symbols are for D and N packages only.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_{OH}	High-level output voltage			5.5	V
I_{OL}	Low-level output current			8	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5	V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.35	0.5	
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1	mA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1	μA
I_{CCL}	V_{CC} = 5.5 V			5	9	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics‡

PARAMETER	FROM	TO	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 0°C to 70°C		UNIT
			TYP	MIN	MAX	
t_{PLH}	A, B	1Y, 2Y	30	13	55	ns
t_{PHL}			12	6	25	
t_{PLH}	1C	1Y	38	18	50	ns
t_{PHL}			12	6	23	
t_{PLH}	$1\overline{G}$	1Y	24	13	38	ns
t_{PHL}			13	6	22	
t_{PLH}	$2\overline{C}$, $2\overline{G}$	2Y	24	13	38	ns
t_{PHL}			13	6	22	

‡ For load circuits and voltage waveforms see Section 1.

- **Buffered Inputs and Outputs**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

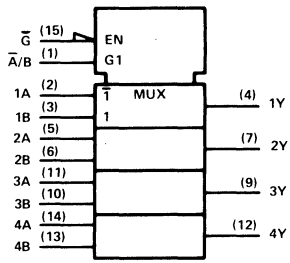
description

These monolithic data selectors/multiplexers contain inverters and drivers to supply full data selection to the four output gates. A separate strobe input ($\overline{G}$) is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. The 'ALS157 and 'AS157 present true data whereas the 'ALS158 and 'AS158 present inverted data to minimize propagation delay time.

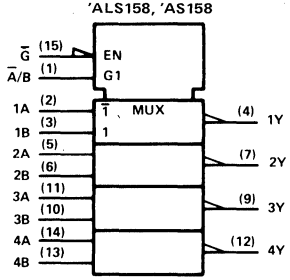
The SN54' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

logic symbols†

'ALS157,'AS157

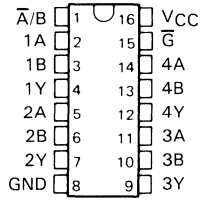


'ALS158, 'AS158

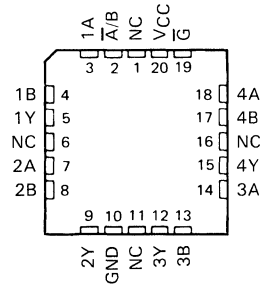


†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54ALS', SN54AS' . . . J PACKAGE
SN74ALS', SN74AS' . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS', SN54AS' . . . FK PACKAGE
(TOP VIEW)



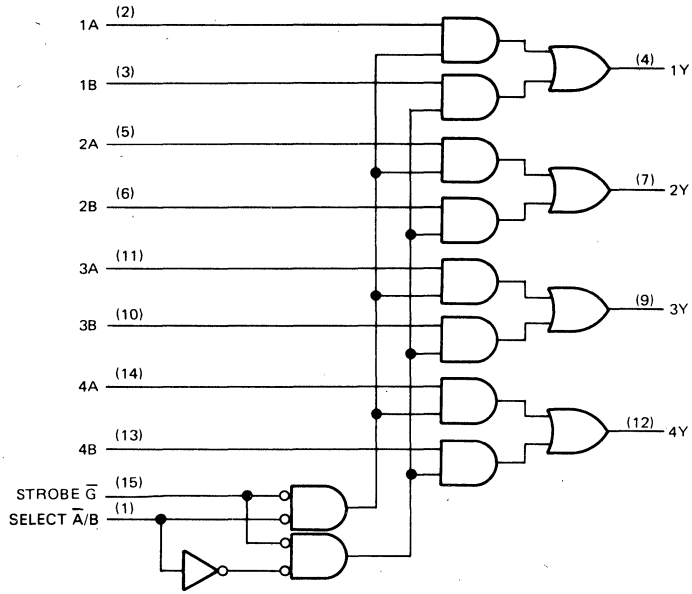
NC—No internal connection

FUNCTION TABLE

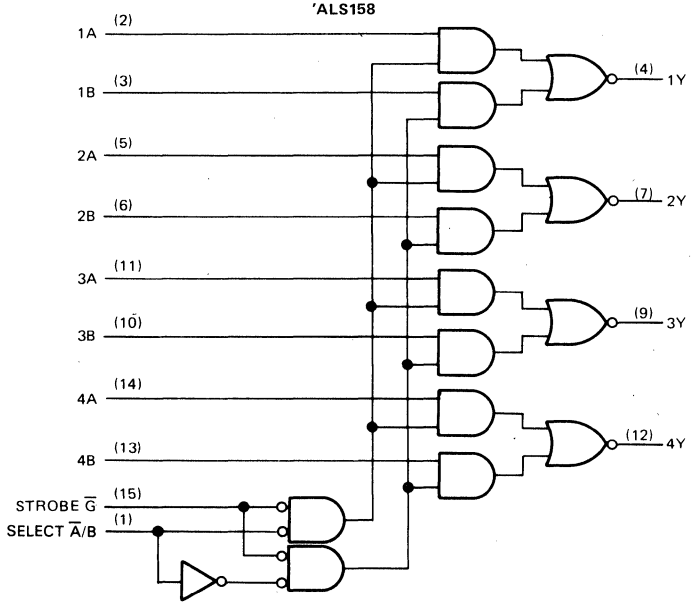
INPUTS				OUTPUT Y	
STROBE	SELECT	DATA			
$\overline{G}$	$\overline{A}$/B	A	B	'ALS157 'AS157	'ALS158 'AS158
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

logic diagrams (positive logic)

'ALS157



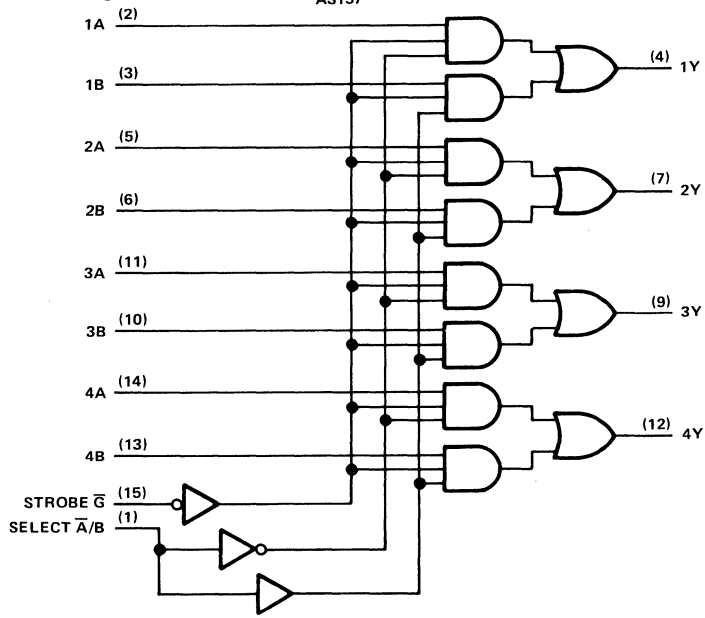
'ALS158



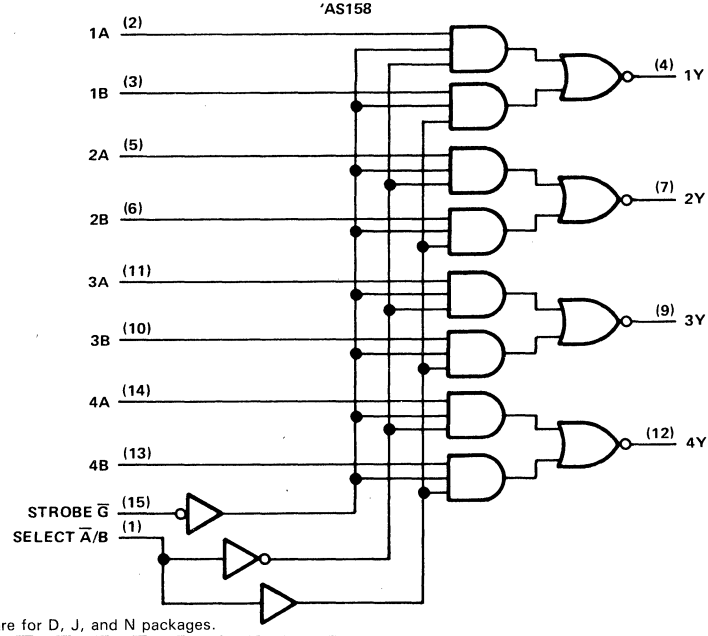
Pin numbers shown are for D, J, and N packages.

logic diagrams (positive logic)

'AS157



'AS158



Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS157, SN54ALS158 . . . . . −55°C to 125°C
SN74ALS157, SN74ALS158 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS157 SN54ALS158			SN74ALS157 SN74ALS158			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS157 SN54ALS158			SN74ALS157 SN74ALS158			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS157	V_{CC} = 5.5 V,	See Note 1		6	11		6	11	mA
	'ALS158				5	10		5	10	

†All typical values ae at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit current, I_{OS}.
NOTE 1: I_{CC} is measured with 4.5 V applied to all inputs and all outputs open.

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'ALS157 switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS157	SN54ALS157		SN74ALS157		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	9	4	17	4	14	ns
t_{PHL}			6	2	15	2	12	
t_{PLH}	$\overline{A}$/B	Y	15	7	28	7	24	ns
t_{PHL}			9	4	16	4	13	
t_{PLH}	$\overline{G}$	Y	14	7	25	7	20	ns
t_{PHL}			10	4	18	4	13	

'ALS158 switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS158	SN54ALS158		SN74ALS158		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	9	4	18	4	15	ns
t_{PHL}			5	2	12	2	8	
t_{PLH}	$\overline{A}$/B	Y	13	5	22	5	18	ns
t_{PHL}			13	5	22	5	18	
t_{PLH}	$\overline{G}$	Y	13	5	22	5	18	ns
t_{PHL}			13	5	22	5	18	

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS157, SN54AS158 . . . . . −55°C to 125°C
SN74AS157, SN74AS158 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS157 SN54AS158			SN74AS157 SN74AS158			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS157 SN54AS158			SN74AS157 SN74AS158			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	$\overline{A}$/B	V_{CC} = 5.5 V,	V_I = 7 V			0.2			0.2	mA
	A, B, or $\overline{G}$					0.1			0.1	
I_{IH}	$\overline{A}$/B	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	μA
	A, B, or $\overline{G}$					20			20	
I_{IL}	$\overline{A}$/B	V_{CC} = 5.5 V,	V_I = 0.4 V			−1			−1	mA
	A, B or $\overline{G}$					−0.5			−0.5	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'AS157	V_{CC} = 5.5 V			17.5	28		17.5	28	mA
	'AS158				15.6	22.5		15.6	22.5	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit current, I_{OS}.

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'AS157 switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS157		SN74AS157		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1	7.5	1	6	ns
t_{PHL}			1	6.5	1	5.5	
t_{PLH}	$\overline{A}$/B	Y	2	12	2	11	ns
t_{PHL}			2	12	2	10	
t_{PLH}	$\overline{G}$	Y	2	12.5	2	10.5	ns
t_{PHL}			2	8.5	2	7.5	

'AS158 switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS158		SN74AS158		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1	6	1	5	ns
t_{PHL}			1	5.5	1	4.5	
t_{PLH}	$\overline{A}$/B	Y	2	11	2	9.5	ns
t_{PHL}			2	11.5	2	10.5	
t_{PLH}	$\overline{G}$	Y	2	8	2	6.5	ns
t_{PHL}			2	11.5	2	10	

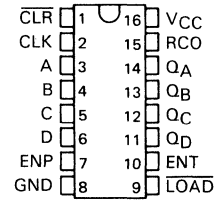
NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

SN54ALS160B THRU SN54ALS163B, SN54AS160 THRU SN54AS163
SN74ALS160B THRU SN74ALS163B, SN74AS160 THRU SN74AS163
SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS

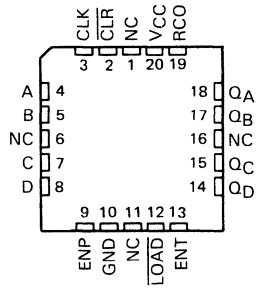
D2661, APRIL 1982—REVISED MAY 1986

- **Internal Look-Ahead for Fast Counting**
- **Carry Output for n-Bit Cascading**
- **Synchronous Counting**
- **Synchronously Programmable**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS', SN54AS' . . . J PACKAGE
SN74ALS', SN74AS' . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS', SN54AS' . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The 'ALS160B, 'ALS162B, 'AS160, and 'AS162 are decade counters, and the 'ALS161B, 'ALS163B, 'AS161, and 'AS163 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, they may be preset to any number between 0 and 9, or 15. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs.

The clear function for the 'ALS160B, 'ALS161B, 'AS160, and 'AS161 is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of the clock, load, or enable inputs.

The clear function for the 'ALS162B, 'ALS163B, 'AS162, and 'AS163 is synchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily by decoding the Q outputs for the maximum count desired. The active-low output of the gate used for decoding is connected to the clear input to synchronously clear the counter to 0000 (LLLL).

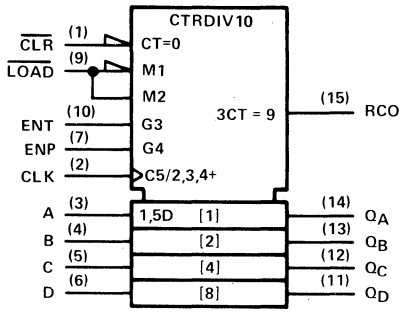
The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (ENP and ENT) must be high to count, and ENT is fed forward to enable the ripple carry output. The ripple carry output (RCO) thus enabled will produce a high-level pulse while the count is maximum (9 or 15 with Q_A high). This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. Transitions at the ENP or ENT are allowed regardless of the level of the clock input.

These counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, or $\overline{\text{LOAD}}$) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

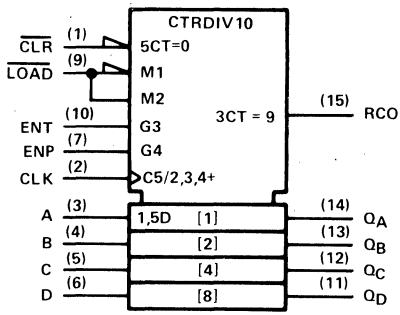
The SN54ALS160B through SN54ALS163B and SN54AS160 through SN54AS163 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS160B through SN74ALS163B and SN74AS160 through SN74AS163 are characterized for operation from 0°C to 70°C.

logic symbols†

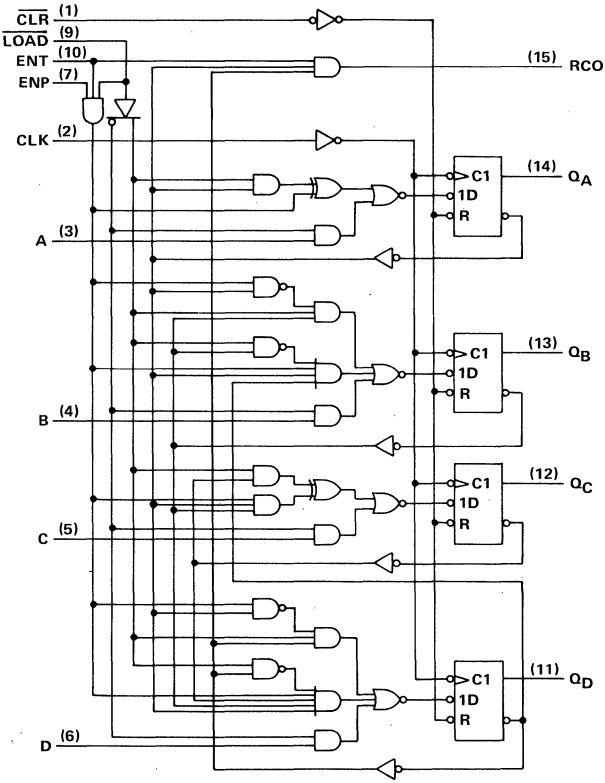
'ALS160B AND 'AS160 DECADE COUNTERS WITH DIRECT CLEAR



'ALS162B AND 'AS162 DECADE COUNTERS WITH SYNCHRONOUS CLEAR



'ALS160B and 'AS160 logic diagram (positive logic)



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.
'ALS162B and 'AS162 decade counters are similar; however the clear is synchronous as shown for the 'ALS163B and 'AS163 binary counters.

TEXAS INSTRUMENTS
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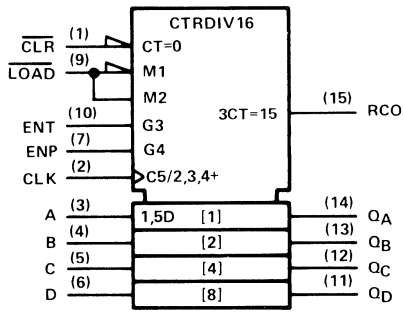
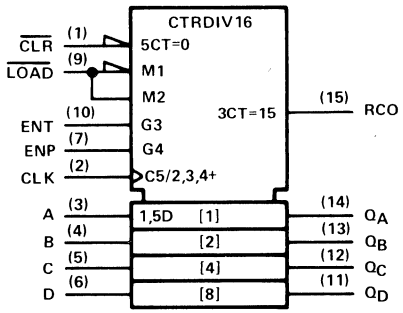
logic symbols†

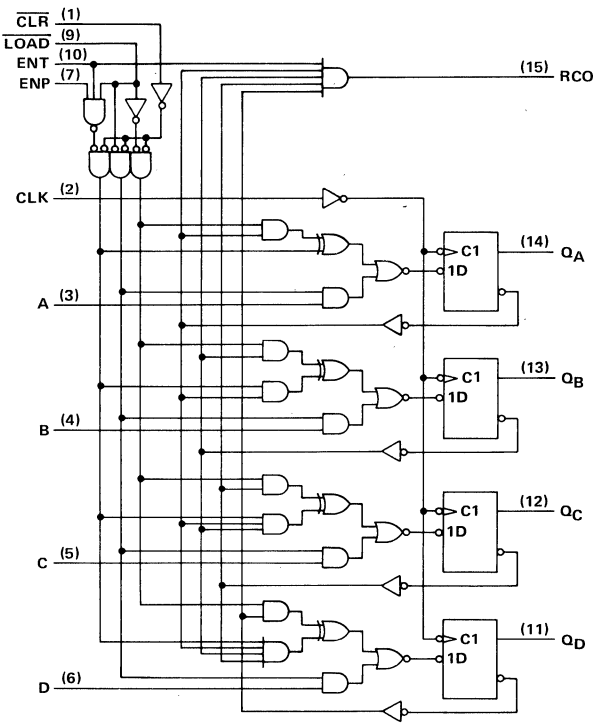
'ALS161B and 'AS161 BINARY COUNTERS WITH DIRECT CLEAR



'ALS163B AND 'AS163 BINARY COUNTERS WITH SYNCHRONOUS CLEAR



'ALS163B and 'AS163 logic diagram (positive logic)



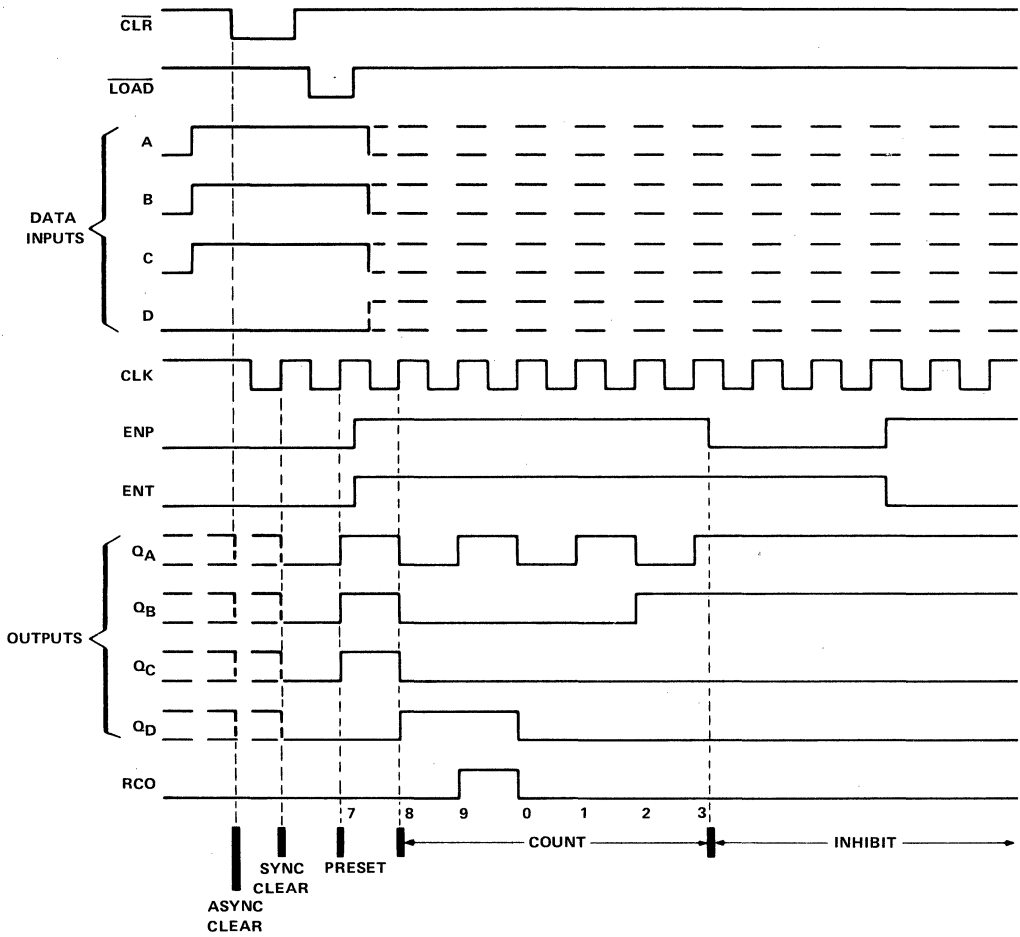
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.
'ALS161B and 'AS161 synchronous binary counters are similar; however the clear is asynchronous as shown for the 'ALS160B and 'AS160 decade counters.

typical clear, preset, count, and inhibit sequences

'ALS160B, 'AS160, 'ALS162B, 'AS162

Illustrated below is the following sequence:

1. Clear outputs to zero ('ALS160B and 'AS160 are asynchronous; 'ALS162B and 'AS162 are synchronous)
2. Preset to BCD seven
3. Count to eight, nine, zero, one, two, and three
4. Inhibit



TEXAS INSTRUMENTS
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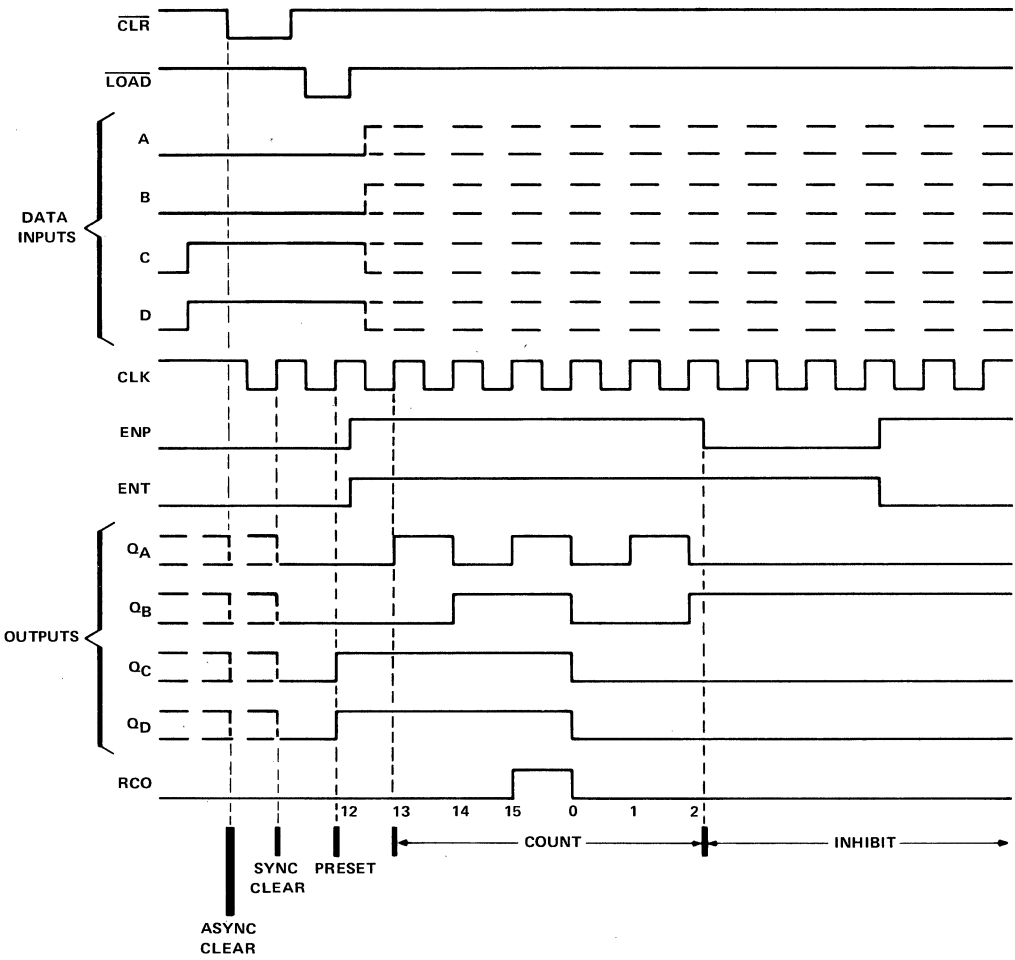
typical clear, preset, count, and inhibit sequences

'ALS161B, 'AS161, 'ALS163B, 'AS163

Illustrated below is the following sequence:

1. Clear outputs to zero ('ALS161B and 'AS161 are asynchronous; 'ALS163B and 'AS163 are synchronous)
2. Preset to binary twelve
3. Count to thirteen, fourteen, fifteen, zero, one, and two
4. Inhibit



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS160B thru SN54ALS163B . . . . . −55°C to 125°C
SN74ALS160B thru SN74ALS163B . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

				SN54ALS160B THRU SN54ALS163B			SN74ALS160B THRU SN74ALS163B			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
I_{OH}	High-level output current					−0.4			−0.4	mA
I_{OL}	Low-level output current					4			8	mA
f_{clock}	Clock frequency			0		22	0		40	MHz
t_w	Pulse duration	CLK high or low		20			12.5			ns
		'ALS160B, 'ALS161B $\overline{CLR}$ low		20			15			
t_{su}	Setup time before CLK↑	A, B, C, D		20			15			ns
		$\overline{LOAD}$		20			15			
		ENP, ENT	'ALS160B, 'ALS161B	25			15			
			'ALS162B, 'ALS163B	20			15			
		'ALS160B, 'ALS161B	$\overline{CLR}$ inactive	10			10			
		'ALS162B, 'ALS163B	$\overline{CLR}$ low	20			15			
			$\overline{CLR}$ high (inactive)	10			10			
t_h	Hold time, all synchronous inputs after CLK↑			0			0			ns
T_A	Operating free-air temperature			−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS160B THRU SN54ALS163B			SN74ALS160B THRU SN74ALS163B			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V			12	21		12	21	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

TEXAS INSTRUMENTS
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'ALS160B, 'ALS161B switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS160B SN54ALS161B		SN74ALS160B SN74ALS161B		
			MIN	MAX	MIN	MAX	
f_{max}			22		40		MHz
t_{PLH}	CLK	RCO	5	34	5	20	ns
t_{PHL}			5	27	5	20	
t_{PLH}	CLK	Any Q	4	19	4	15	ns
t_{PHL}			6	25	6	20	
t_{PLH}	ENT	RCO	3	18	3	13	ns
t_{PHL}			3	17	3	13	
t_{PHL}	$\overline{CLR}$	Any Q	8	27	8	24	ns
t_{PHL}	$\overline{CLR}$	RCO	11	32	11	23	ns

'ALS162B, 'ALS163B switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS162B SN54ALS163B		SN74ALS162B SN74ALS163B		
			MIN	MAX	MIN	MAX	
f_{max}			35		40		MHz
t_{PLH}	CLK	RCO	5	25	5	20	ns
t_{PHL}			5	25	5	20	
t_{PLH}	CLK	Any Q	4	18	4	15	ns
t_{PHL}			6	25	6	20	
t_{PLH}	ENT	RCO	3	16	3	13	ns
t_{PHL}			3	16	3	13	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS160 thru SN54AS163 . . . . . −55°C to 125°C
SN74AS160 thru SN74AS163 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

				SN54AS160 THRU SN54AS163			SN74AS160 THRU SN74AS163			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
I_{OH}	High-level output current					−2			−2	mA
I_{OL}	Low-level output current					20			20	mA
f_{clock}	Clock frequency			0		65	0		75	MHz
t_w	Pulse duration	CLK high or low		7.7			6.7			ns
		'AS160, 'AS161 $\overline{CLR}$ low		10			8			
t_{su}	Setup time before CLK↑	A, B, C, D		10			8			ns
		$\overline{LOAD}$		10			8			
		ENP, ENT		10			8			
		'AS160, 'AS161 $\overline{CLR}$ inactive		10			8			
		'AS162, 'AS163	$\overline{CLR}$ low	14			12			
			$\overline{CLR}$ high (inactive)	10			9			
t_h	Hold time, all synchronous inputs after CLK↑			2			0			ns
T_A	Operating free-air temperature			−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS160 THRU SN54AS163			SN74AS160 THRU SN74AS163			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.25	0.5		0.25	0.5	V
I_I	$\overline{LOAD}$	V_{CC} = 5.5 V,	V_I = 7 V			0.3			0.3	mA
	ENT					0.2			0.2	
	All other					0.1			0.1	
I_{IH}	$\overline{LOAD}$	V_{CC} = 5.5 V,	V_I = 2.7 V			60			60	μA
	ENT					40			40	
	All other					20			20	
I_{IL}	$\overline{LOAD}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−1.5			−1.5	mA
	ENT					−1			−1	
	All other					−0.5			−0.5	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V			35	53		35	53	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

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'AS160, 'AS161 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS160 SN54AS161		SN74AS160 SN74AS161		
			MIN	MAX	MIN	MAX	
f_{max}			65		75		MHz
t_{PHL}	CLK	RCO	2	14	2	12.5	ns
t_{PLH}		RCO (with $\overline{LOAD}$ high)	1	8.5	1	8	
t_{PLH}		RCO (with $\overline{LOAD}$ low)	3	17.5	3	16.5	
t_{PLH}	CLK	Any Q	1	7.5	1	7	ns
t_{PHL}			2	14	2	13	
t_{PLH}	ENT	RCO	1.5	10	1.5	9	ns
t_{PHL}			1	9.5	1	8.5	
t_{PHL}	$\overline{CLR}$	Any Q	2	14	2	13	ns
t_{PHL}	$\overline{CLR}$	RCO	2	14	2	12.5	ns

'AS162, 'AS163 switching characteristics (see Note 1)

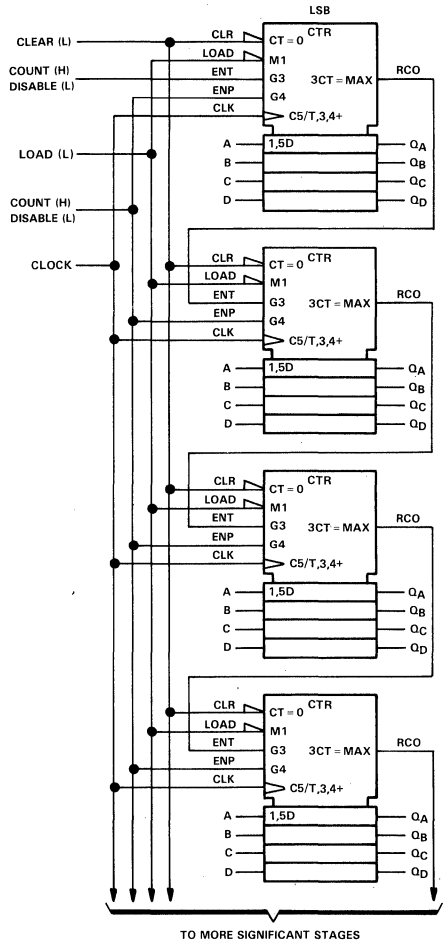
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS162 SN54AS163		SN74AS162 SN74AS163		
			MIN	MAX	MIN	MAX	
f_{max}			65		75		MHz
t_{PHL}	CLK	RCO	2	14	2	12.5	ns
t_{PLH}		RCO (with $\overline{LOAD}$ high)	1	8.5	1	8	
t_{PLH}		RCO (with $\overline{LOAD}$ low)	3	17.5	3	16.5	
t_{PLH}	CLK	Any Q	1	7.5	1	7	ns
t_{PHL}			2	14	2	13	
t_{PLH}	ENT	RCO	1.5	10	1.5	9	ns
t_{PHL}			1	9.5	1	8.5	

NOTE 1. Load circuit and voltage waveforms are shown in Section 1.

TYPICAL APPLICATION DATA

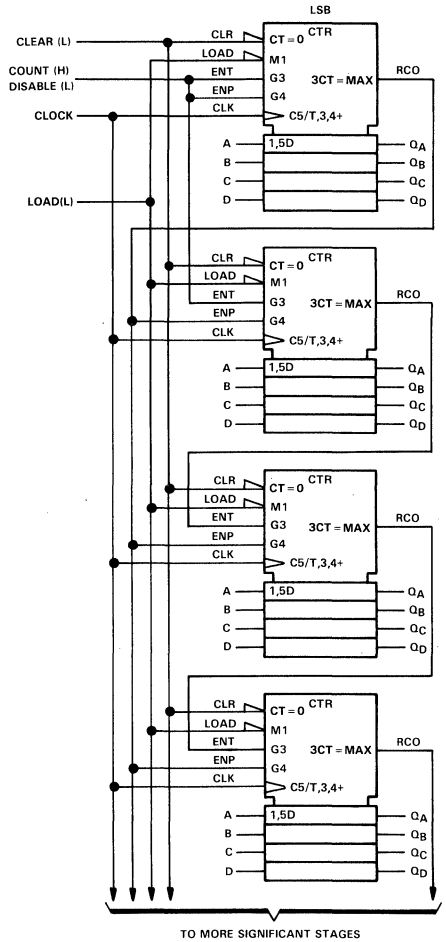
N-BIT SYNCHRONOUS COUNTERS

This application demonstrates how the ripple mode carry circuit (Figure 1) and the carry-look-ahead circuit (Figure 2) can be used to implement a high-speed N-bit counter. The 'ALS160B, 'AS160, 'ALS162B, and 'AS162 will count in BCD and the 'ALS161B, 'AS161, 'ALS163B, and 'AS163 will count in binary. When additional stages are added, the f_{MAX} decreases in Figure 1, but remains unchanged in Figure 2.



$f_{MAX} = 1/(\text{CLK to RCO } t_{PLH}) + (\text{ENT to RCO } t_{PLH})(N-2) + (\text{ENT } t_{su})$

FIGURE 1



$f_{MAX} = 1/\text{CLK to RCO } t_{PLH} + (\text{ENP } t_{su})$

FIGURE 2

TEXAS INSTRUMENTS
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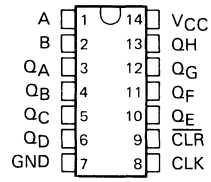
SN54ALS164, SN74ALS164
8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

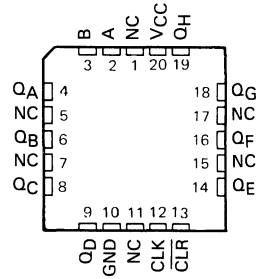
D2661, APRIL 1982—REVISED MAY 1986

- **AND-Gated (Enable/Disable) Serial Inputs**
- **Fully Buffered Clock and Serial Inputs**
- **Direct Clear**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS164 . . . J PACKAGE
SN74ALS164 . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS164 . . . FK PACKAGE
(TOP VIEW)



NC—No Internal connection

description

These 8-bit shift registers feature AND-gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data as a low at either input inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input, which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, provided the minimum setup time requirements are met. Clocking occurs on the low-to-high-level transition of the clock input. All inputs are diode-clamped to minimize transmission-line effects.

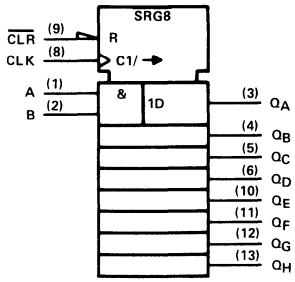
The SN54ALS164 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS164 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS				OUTPUTS		
CLEAR	CLOCK	A	B	Q_A	Q_B . . . Q_H	
L	X	X	X	L	L	L
H	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	↑	H	H	H	Q_{An}	Q_{Gn}
H	↑	L	X	L	Q_{An}	Q_{Gn}
H	↑	X	L	L	Q_{An}	Q_{Gn}

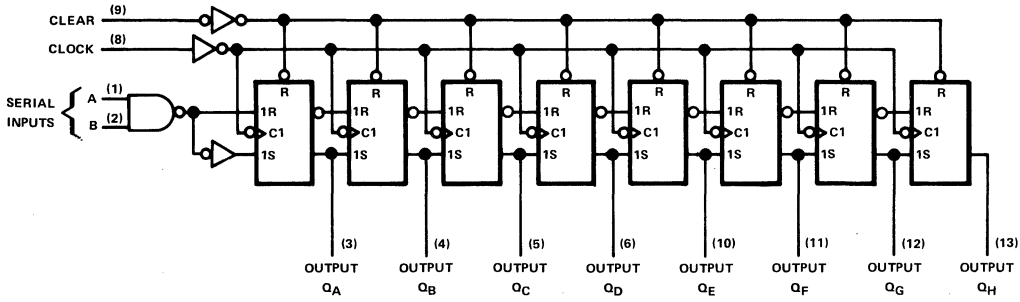
H = high level (steady state), L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level.
Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Gn} = the level of Q_A or Q_G before the most-recent ↑ transition of the clock; indicates a one-bit shift.

logic symbol†



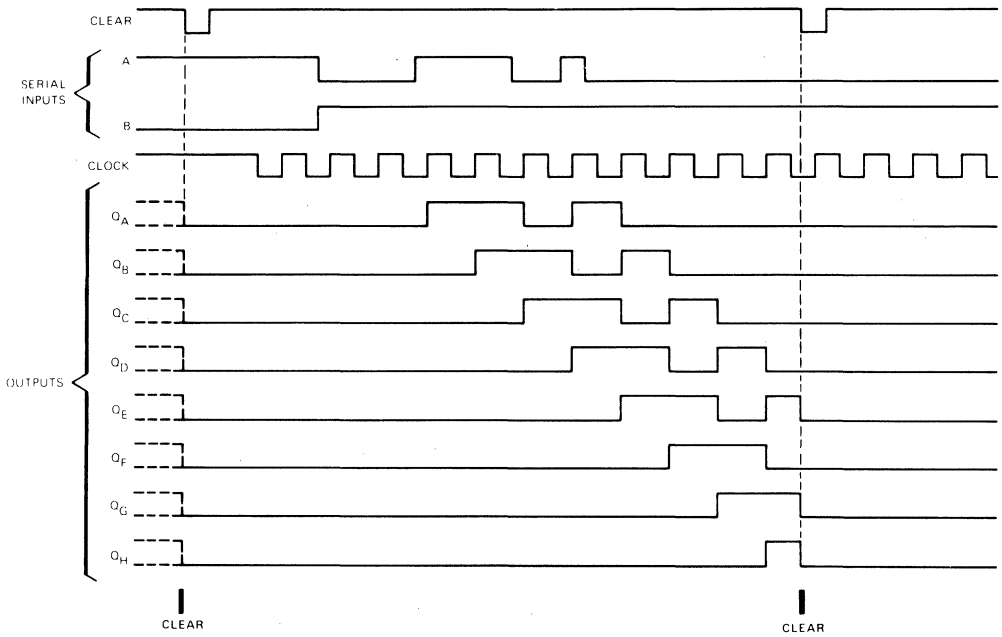
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J and N packages.

logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

typical clear, shift, and clear sequences



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS164 . . . . . −55 °C to 125 °C
SN74ALS164 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

recommended operating conditions

			SN54ALS164			SN74ALS164			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency								MHz
t_w	Pulse duration	$\overline{CLR}$ low							ns
		CLK high							
		CLK low							
t_{su}	Setup time before CLK↑	SH/LD							ns
		Data							
		$\overline{CLR}$ inactive							
t_h	Hold time, data after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS164			SN74ALS164			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	See Note 1		10			10		mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: With 4.5 Volts applied to the serial input and all other inputs except the clock grounded, I_{CC} is measured after a clock transition from 0 to 4.5 volts.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS164			SN74ALS164			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}				60			60		MHz
t_{PHL}	$\overline{CLR}$	Any Q		12			12		ns
t_{PLH}	CLK	Any Q		10			10		ns
t_{PHL}				11			11		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

Additional information on these products can be obtained from the factory as it becomes available.

SN54ALS165, SN74ALS165
PARALLEL-LOAD 8-BIT SHIFT REGISTERS

D2661, JUNE 1982—REVISED MAY 1986

- **Complementary Outputs**
- **Direct Overriding Load (Data) Inputs**
- **Gated Clock Inputs**
- **Parallel-to-Serial Data Conversion**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

The 'ALS165 is an 8-bit serial shift register that, when clocked, shifts the data toward serial output $\overline{Q}_H$. Parallel-in access to each stage is provided by eight individual direct data inputs that are enabled by a low level at the SH/LD input. The 'ALS165 also features a clock inhibit function and a complemented serial output $\overline{Q}_H$.

Clocking is accomplished by a low-to-high transition of the CLK input while SH/$\overline{LD}$ is held high and CLK INH is held low. The functions of the CLK and CLK INH (clock inhibit) inputs are interchangeable. Since a low CLK input and a low-to-high transition of CLK INH will also accomplish clocking, CLK INH should be changed to the high level only while the CLK input is high. Parallel loading is inhibited when SH/$\overline{LD}$ is held high. The parallel inputs to the register are enabled while SH/$\overline{LD}$ is low independently of the levels of CLK, CLK INH, or SER inputs.

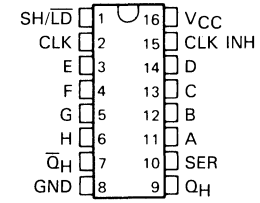
The SN54ALS165 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS165 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

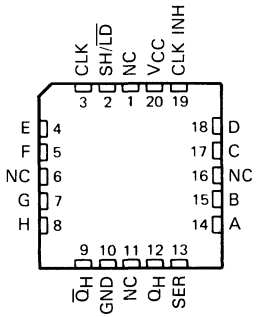
INPUTS			FUNCTION
SH/LD	CLK	CLK INH	
L	X	X	PARALLEL LOAD
H	H	X	NO CHANGE
H	X	H	NO CHANGE
H	L	↑	SHIFT
H	↑	L	SHIFT

SHIFT—content of each internal register shifts toward serial output Q_H. Data at serial input is shifted into first register.

SN54ALS165 . . . J PACKAGE
SN74ALS165 . . . D OR N PACKAGE
(TOP VIEW)

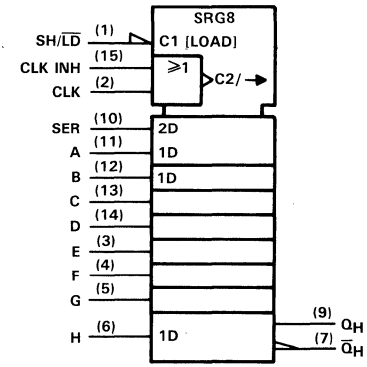


SN54ALS165 . . . FK PACKAGE
(TOP VIEW)



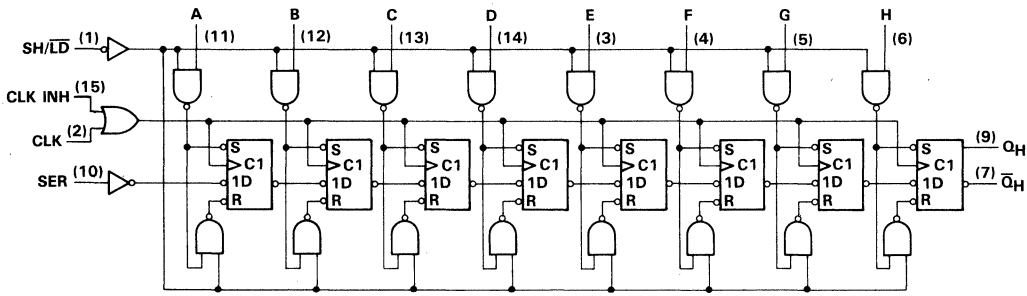
NC—No internal connection

logic symbol†



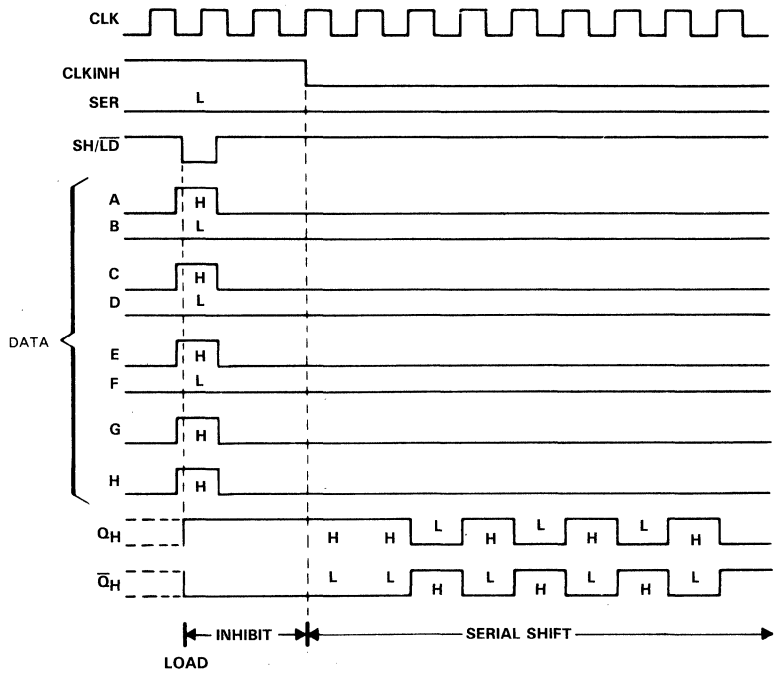
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers are for D, J, and N packages.

logic diagram (positive logic)



Pin numbers are for D, J, and N packages.

typical shift, load, and inhibit sequences



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS165 . . . . . −55°C to 125°C
SN74ALS165 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS165			SN74ALS165			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	55	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency								MHz
t_w	Pulse duration	$\overline{CLR}$ low							ns
		CLK high							
		CLK low							
t_{su}	Setup time before CLK↑	SH/$\overline{LD}$							ns
		Data							
		$\overline{CLR}$ inactive							
t_h	Hold time, data after CLK↑								ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS165			SN74ALS165			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	See Note 1		16			16		mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I_{OS}.
NOTE 1: With the outputs open, CLK INH and CLK at 4.5 V, and a clock pulse applied to the SH/$\overline{LD}$ input, I_{CC} is measured first with the parallel inputs at 4.5 V, then with the parallel inputs grounded.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 50 Ω, T_A = MIN to MAX						UNIT
			SN54ALS165			SN74ALS165			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}			25			25			MHz
t_{PLH}	SH/$\overline{LD}$	Any		21			21		ns
t_{PHL}				26			26		
t_{PLH}	CLK	Any		14			14		ns
t_{PHL}				16			16		
t_{PLH}	H	Q_H		13			13		ns
t_{PHL}				24			24		
t_{PLH}	H	$\overline{Q}_H$		19			19		ns
t_{PHL}				17			17		

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

Additional information on these products can be obtained from the factory as it becomes available.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SN54ALS166, SN74ALS166
PARALLEL-LOAD 8-BIT SHIFT REGISTERS

D2661, APRIL 1982—REVISED MAY 1986

- **Synchronous Load**
- **Direct Overriding Clear**
- **Parallel to Serial Conversion**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

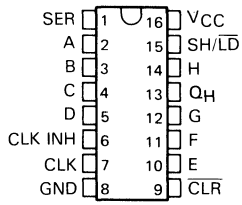
description

The 'ALS166 8-bit shift register is compatible with most other TTL logic families. All inputs are buffered to lower the drive requirements. Input clamping diodes minimize switching transients and simplify system design.

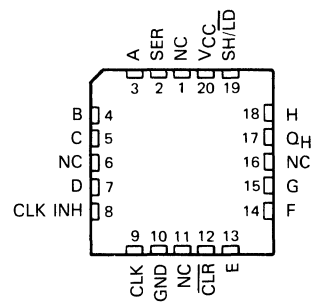
These parallel-in or serial-in, serial-out registers have a complexity of 77 equivalent gates on a monolithic chip. They feature gated clock inputs and an overriding clear input. The parallel-in or serial-in modes are established by the shift/load input. When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. When low, the parallel (broadside) data inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high-level edge of the clock pulse through a two-input positive NOR gate permitting one input to be used as a clock-enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This, of course, allows the system clock to be free-running and the register can be stopped on command with the clock input. The clock-inhibit input should be changed to the high level only when the clock input is high. A buffered, direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero.

The SN54ALS166 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS166 is characterized for operation from 0°C to 70°C.

SN54ALS166 . . . J PACKAGE
SN74ALS166 . . . D OR N PACKAGE
(TOP VIEW)

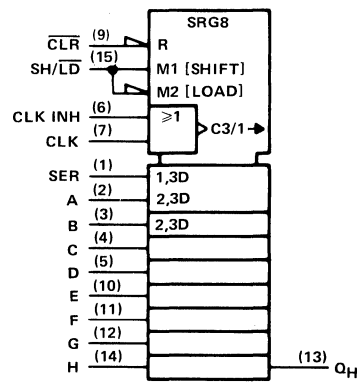


SN54ALS166 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic symbol†

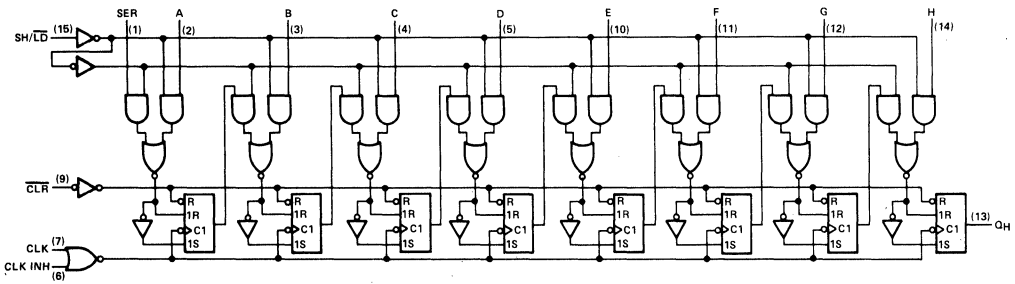


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers are for D, J, and N packages.

FUNCTION TABLE

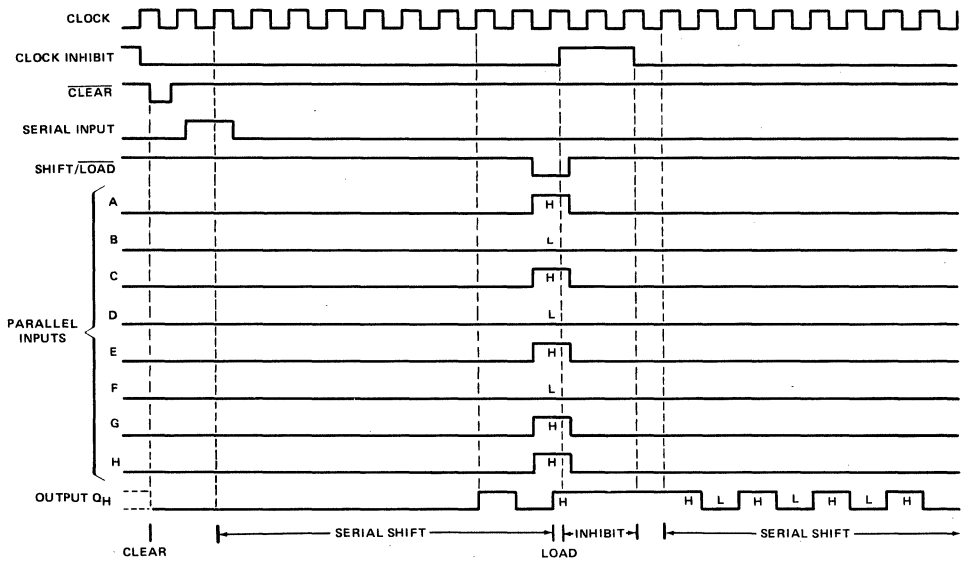
INPUTS						INTERNAL OUTPUTS		OUTPUT
CLEAR	SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A . . . H	Q_A	Q_B	Q_H
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	L	↑	X	a . . . h	a	b	h
H	H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	X	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

logic diagram (positive logic)



Pin numbers are for D, J, and N packages.

typical clear, shift, load, inhibit, and shift sequences



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS166 . . . . . −55°C to 125°C
SN74ALS166 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS166			SN74ALS166			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency								MHz
t_w	Pulse duration	$\overline{CLR}$ low							ns
		CLK high							
		CLK low							
t_{su}	Setup time before CLK↑	SH/$\overline{LD}$							ns
		Data							
		$\overline{CLR}$ inactive							
t_h	Hold time, data after CLK↑								ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS166			SN74ALS166			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	See Note 1		16			16		mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: With 4.5 volts applied to the serial input and all other inputs except the clock grounded, I_{CC} is measured after a clock transition from 0 to 4.5 volts.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS166			SN74ALS166			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}				60			60		MHz
t_{PHL}	$\overline{CLR}$	Q_H		10			10		ns
t_{PLH}	CLK	Q_H		12			12		ns
t_{PHL}				13			13		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

Additional information on these products can be obtained from the factory as it becomes available.

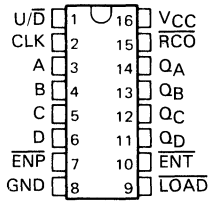
TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SYNCHRONOUS 4-BIT UP/DOWN DECADE AND BINARY COUNTERS

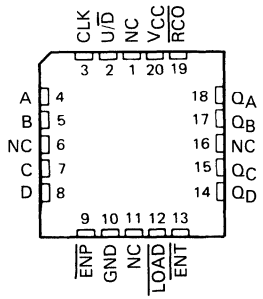
MARCH 1984 – REVISED MAY 1986

- **Fully Synchronous Operation for Counting and Programming**
- **Internal Look-Ahead for Fast Counting**
- **Carry Output for n-Bit Cascading**
- **Fully Independent Clock Circuit**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS', SN54AS' . . . J PACKAGE
SN74ALS', SN74AS' . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS', SN54AS' . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These synchronous presettable counters feature an internal carry look-ahead for cascading in high-speed counting applications. The 'ALS168B and 'AS168 are decade counters and the 'ALS169B and 'AS169 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock waveform.

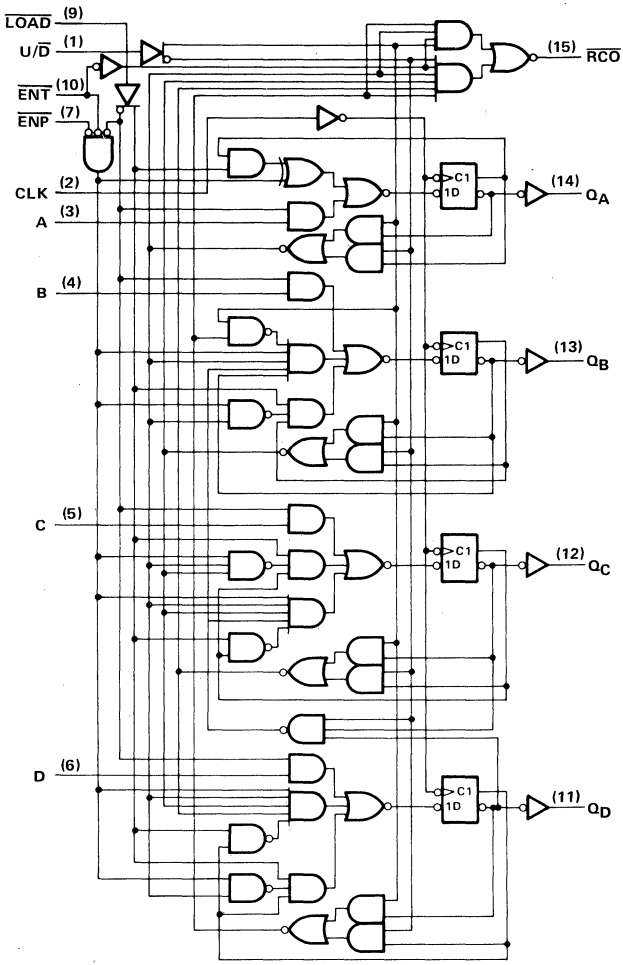
These counters are fully programmable; that is, the outputs may each be preset to either level. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous application without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count enable inputs ($\overline{ENP}$ and $\overline{ENT}$) must be low to count. The direction of the count is determined by the level of the U/$\overline{D}$ input. When U/$\overline{D}$ is high, the counter counts up; when low, it counts down. Input $\overline{ENT}$ is fed forward to enable the carry output. The riple carry output ($\overline{RCO}$) thus enabled will produce a low-level pulse while the count is zero (all inputs low) counting down or maximum (9 or 15) counting up. This low-level overflow carry pulse can be used to enable successive cascaded stages. Transistions at $\overline{ENP}$ or $\overline{ENT}$ are allowed regardless of the level of the clock input. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design.

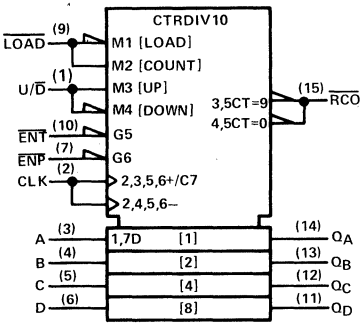
These counters feature a fully independent clock circuit. Changes at control inputs ($\overline{ENP}$, $\overline{ENT}$, $\overline{LOAD}$, U/$\overline{D}$) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

The SN54ALS168B, SN54AS168, SN54ALS169B, and SN54AS169 are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS168B, SN74AS168, SN74ALS169B, and SN74AS169 are characterized for operation from 0 °C to 70 °C.

'ALS168B, 'AS168 logic diagram (positive logic)



'ALS168B, 'AS168 logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

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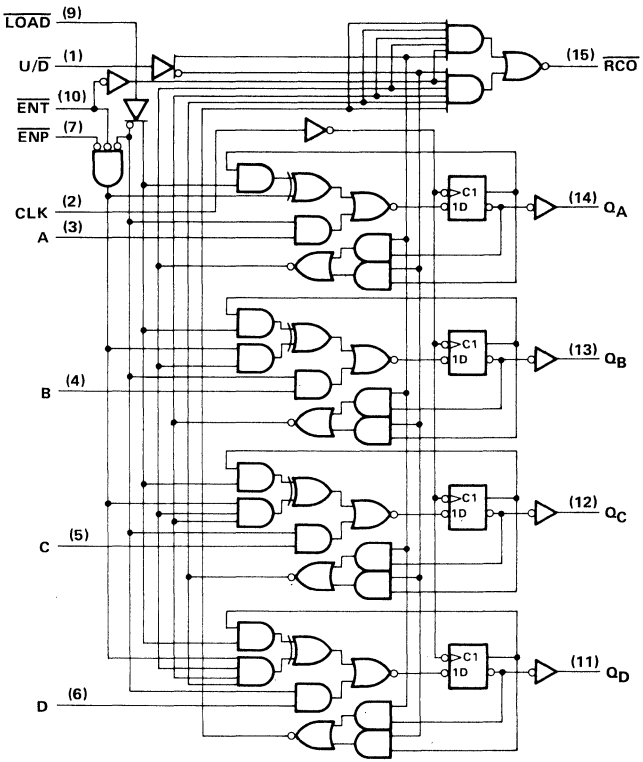
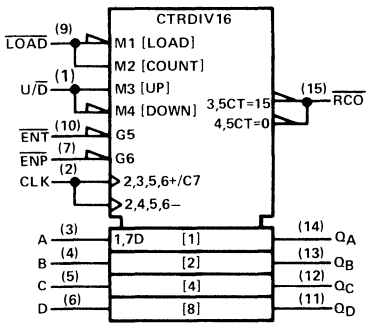
'ALS169B, 'AS169 logic diagram (positive logic)



'ALS169B, 'AS169 logic symbol†

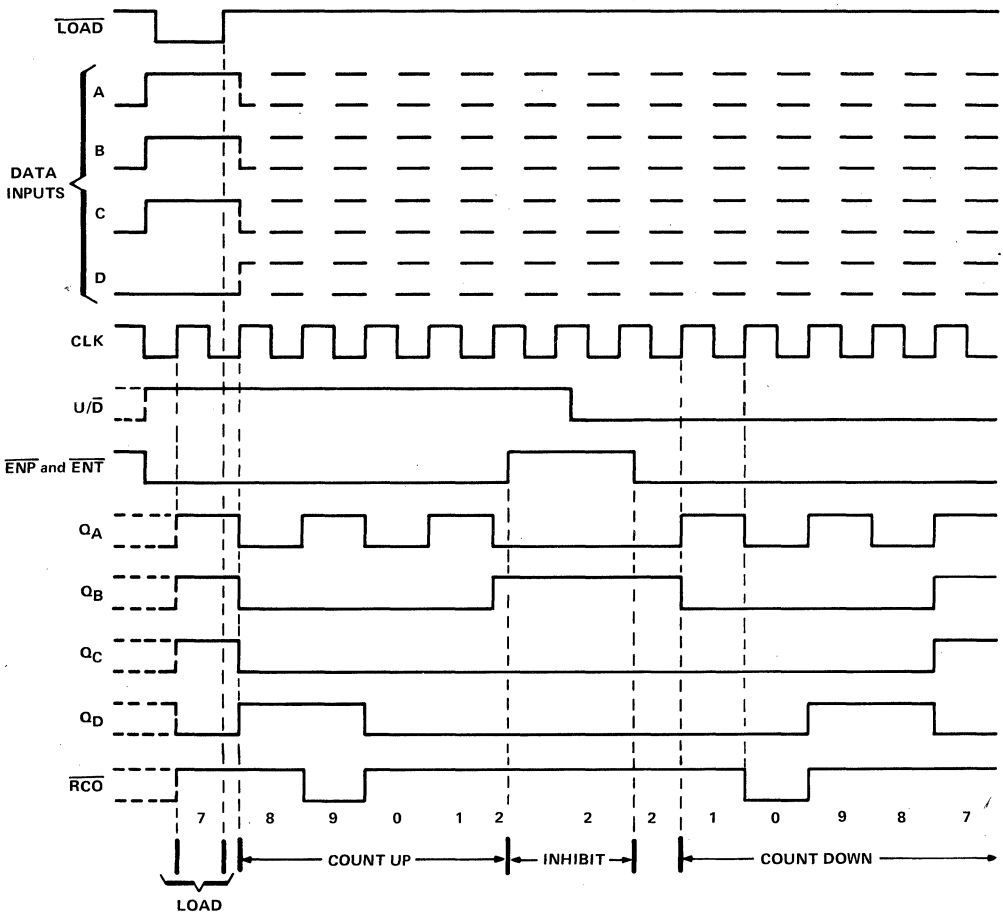


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

'ALS168B, 'AS168 typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to BCD seven
2. Count up to eight, nine (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), nine, eight, and seven



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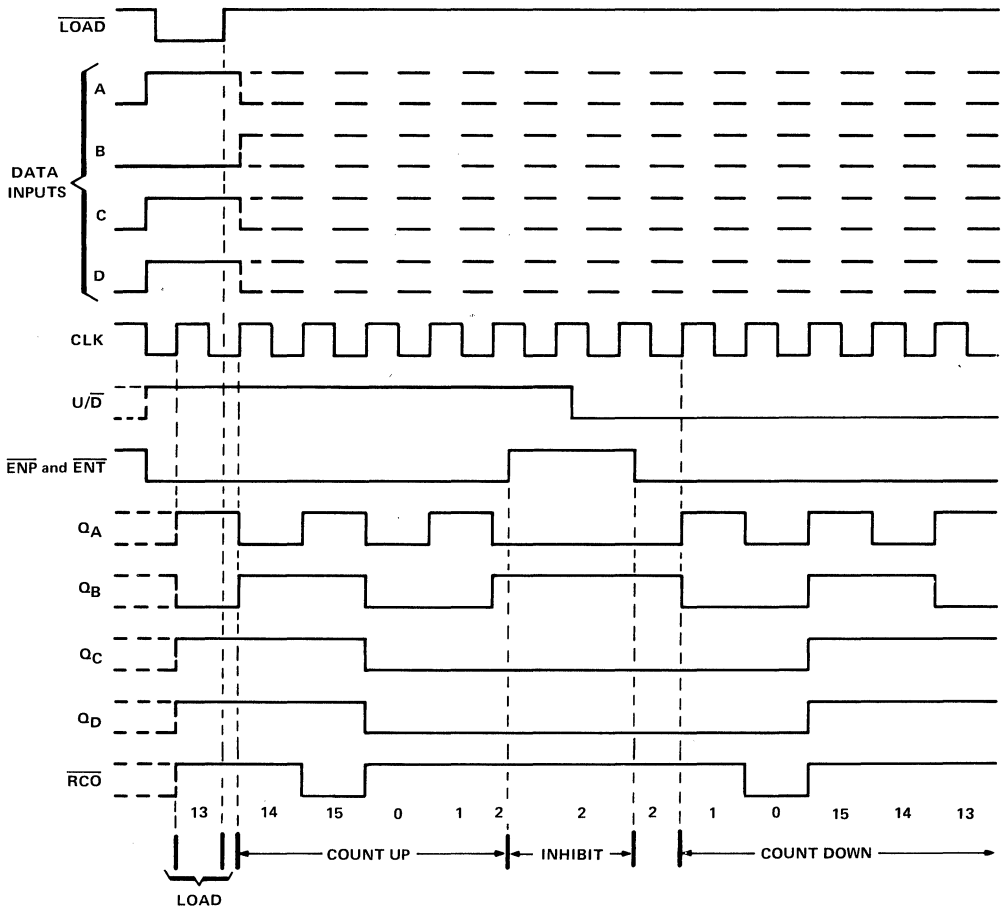
'ALS169B, 'AS169 typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to binary thirteen
2. Count up to fourteen, fifteen (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS168B, SN54ALS169B . . . . . −55°C to 125°C
SN74ALS168B, SN74ALS169B . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS168B SN54ALS169B			SN74ALS168B SN74ALS169B			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		22	0		40	MHz
t_w	Pulse duration	CLK high or low	14			12.5			ns
t_{su}	Setup time before CLK↑	A, B, C, or D	20			15			ns
		$\overline{ENP}$ or $\overline{ENT}$	25			15			
		$\overline{LOAD}$	20			15			
		U/$\overline{D}$	28			15			
t_h	Hold time, data after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS168B SN54ALS169B			SN74ALS168B SN74ALS169B			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V			15	25		15	25	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

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'ALS168B, 'ALS169B switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, RL = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS168B SN54ALS169B		SN74ALS168B SN74ALS169B		
			MIN	MAX	MIN	MAX	
f_{max}			22		40		MHz
t_{PLH}	CLK	$\overline{RCO}$	3	25	3	20	ns
t_{PHL}			6	25	6	20	
t_{PLH}	CLK	Any Q	2	20	2	15	ns
t_{PHL}			5	23	5	20	
t_{PLH}	$\overline{ENT}$	$\overline{RCO}$	2	16	2	13	ns
t_{PHL}			3	24	3	16	
t_{PLH}	U/$\overline{D}$	$\overline{RCO}$	5	22	5	19	ns
t_{PHL}			5	22	5	19	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS168, SN54AS169 . . . . . −55°C to 125°C
SN74AS168, SN74AS169 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54AS168 SN54AS169			SN74AS168 SN74AS169			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−2	mA
I_{OL}	Low-level output current				20			20	mA
f_{clock}	Clock frequency		0		65	0		75	MHz
t_w	Pulse duration	CLK high or low	7.7			6.7			ns
t_{su}	Setup time before CLK↑	A, B, C, or D	10			8			ns
		$\overline{ENP}$ or $\overline{ENT}$	10			8			
		$\overline{LOAD}$	10			8			
		U/$\overline{D}$	10			8			
t_h	Hold time, data after CLK↑		2			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS168 SN54AS169			SN74AS168 SN74AS169			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.25	0.5		0.25	0.5	V
I_I	$\overline{LOAD}$, $\overline{ENT}$, U/$\overline{D}$	V_{CC} = 5.5 V,	V_I = 7 V			0.2			0.2	mA
	All others					0.1			0.1	
I_{IH}	$\overline{LOAD}$, $\overline{ENT}$, U/$\overline{D}$	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	μA
	All others					20			20	
I_{IL}	$\overline{LOAD}$, $\overline{ENT}$, U/$\overline{D}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−1			−1	mA
	All others,					−0.5			−0.5	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V			41	63		41	63	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

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'AS168, 'AS169 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, RL = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS168 SN54AS169		SN74AS168 SN74AS169		
			MIN	MAX	MIN	MAX	
f_{max}			65		75		MHz
t_{PLH}	CLK	$\overline{RCO}$	3	17.5	3	16.5	ns
t_{PHL}		($\overline{LOAD}$ high or low)	2	14	2	13	
t_{PLH}	CLK	Any Q	1	7.5	1	7	ns
t_{PHL}			2	14	2	13	
t_{PLH}	$\overline{ENT}$	$\overline{RCO}$	1.5	10	1.5	9	ns
t_{PHL}			1.5	10	1.5	9	
t_{PLH}	U/$\overline{D}$	$\overline{RCO}$	2	14	2	12	ns
t_{PHL}			2	14.5	2	13	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2661, APRIL 1982 – REVISED MAY 1986

- 'ALS174 and 'AS174 Contain Six Flip-Flops with Single-Rail Outputs
- 'ALS175 and 'AS175A Contain Four Flip-Flops with Double-Rail Outputs
- Buffered Clock and Direct Clear Inputs
- Applications Include:
  Buffer/Storage Registers
  Shift Registers
  Pattern Generators
- Fully Buffered Outputs for Maximum Isolation from External Disturbances ('AS only)
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input and the 'ALS175 and 'AS175A feature complementary outputs from each flip-flop.

Information at the D inputs meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

These circuits are fully compatible for use with most TTL circuits.

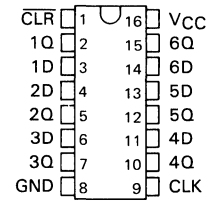
The SN54ALS174, SN54ALS175, SN54AS174, and SN54AS175A are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS174, SN74ALS175, SN74AS174, and SN74AS175A are characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(EACH FLIP-FLOP)

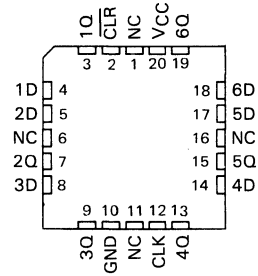
INPUTS			OUTPUTS	
$\overline{CLR}$	CLK	D	Q	$\overline{Q}$†
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

†'ALS175 and 'AS175A only

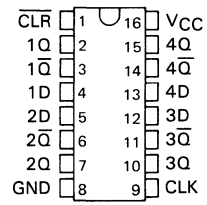
SN54ALS174, SN54AS174 . . . J PACKAGE
SN74ALS174, SN74AS174 . . . D OR N PACKAGE
(TOP VIEW)



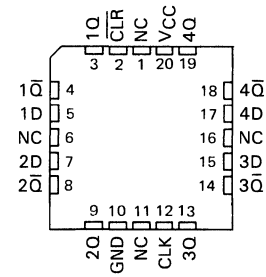
SN54ALS174, SN54AS174 . . . FK PACKAGE
(TOP VIEW)



SN54ALS175, SN54AS175A . . . J PACKAGE
SN74ALS175, SN74AS175A . . . D OR N PACKAGE
(TOP VIEW)



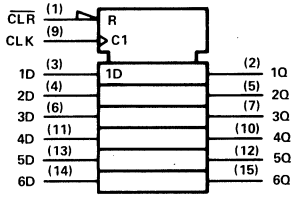
SN54ALS175, SN54AS175A . . . FK PACKAGE
(TOP VIEW)



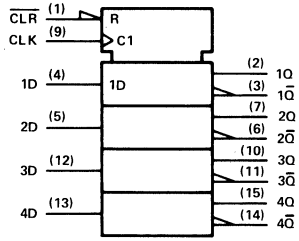
NC – No internal connection.

logic symbols†

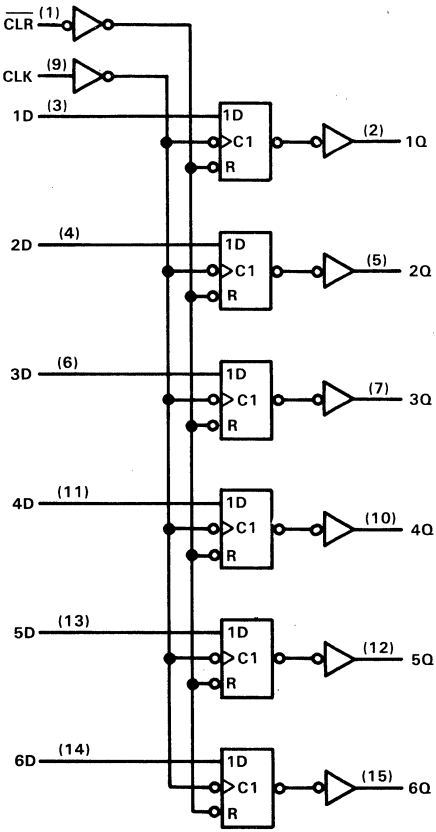
'ALS174, 'AS174

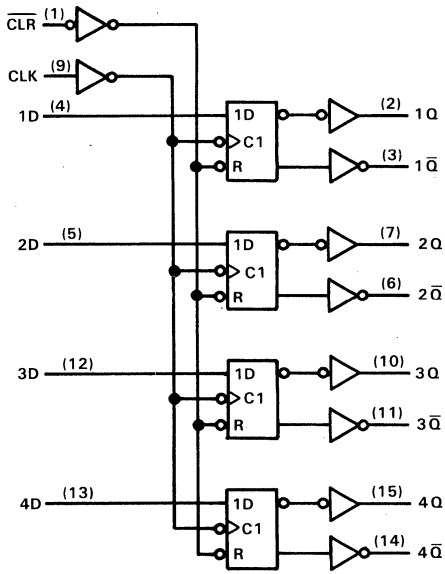


'ALS175, 'AS175A



logic diagrams (positive logic)





†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS174, SN54ALS175 . . . . . −55°C to 125°C
SN74ALS174, SN74ALS175 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS174 SN54ALS175			SN74ALS174 SN74ALS175			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		40	0		50	MHz
t_w	Pulse duration	$\overline{CLR}$ low	15			10			ns
		CLK high	12.5			10			
		CLK low	12.5			10			
t_{su}	Setup time before CLK↑	Data	15			10			ns
		$\overline{CLR}$ inactive	8			6			
t_h	Hold time, data after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS174 SN54ALS175			SN74ALS174 SN74ALS175			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V	I_{OL} = 8 mA					0.35	0.5	
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS174	V_{CC} = 5.5 V,	See Note 1		11	19		11	19	mA
	'ALS175				8	14		9	14	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with D inputs and $\overline{CLR}$ grounded, and CLK at 4.5 V.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS174 SN54ALS175		SN74ALS174 SN74ALS175		
			MIN	MAX	MIN	MAX	
f_{max}			40		50		MHz
t_{PLH}	$\overline{CLR}$	Any $\overline{Q}$ ('ALS175)	5	20	5	18	ns
t_{PHL}		Any Q	8	30	8	23	
t_{PLH}	CLK	Any Q	3	20	3	15	ns
t_{PHL}		(or $\overline{Q}$, 'ALS175)	5	24	5	17	

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS174, SN54AS175A . . . . . −55°C to 125°C
SN74AS174, SN74AS175A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

				SN54AS174 SN54AS175A			SN74AS174 SN74AS175A			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
I_{OH}	High-level output current					−2			−2	mA
I_{OL}	Low-level output current					20			20	mA
f_{clock}	Clock frequency			0		100	0		100	MHz
t_w	Pulse duration	$\overline{CLR}$ low		5.5			5			ns
		CLK high		4			4			
		CLK low	'AS174	6			6			
			'AS175A	5			5			
t_{su}	Setup time before CLK↑	Data	'AS174	4			4			ns
			'AS175A	3			3			
		$\overline{CLR}$ inactive		6			6			
t_h	Hold time, data after CLK↑			1			1			ns
T_A	Operating free-air temperature			−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS174 SN54AS175A			SN74AS174 SN74AS175A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'AS174	V_{CC} = 5.5 V,	See Note 1		30	45		30	45	mA
	'AS175				22.5	34		22.5	34	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with D inputs and $\overline{CLR}$ grounded, and CLK at 4.5 V.

'AS174 switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS174		SN74AS174		
			MIN	MAX	MIN	MAX	
f_{max}			100		100		MHz
t_{PHL}	$\overline{CLR}$	Any Q	5	15	5	14	ns
t_{PLH}	CLK	Any Q	3.5	9.5	3.5	8	ns
t_{PHL}			4.5	11.5	4.5	10	

'AS175A switching characteristics (see Note 2)

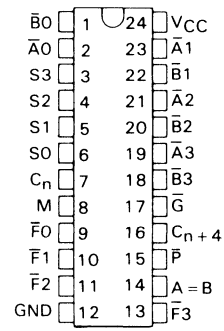
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS175A		SN74AS175A		
			MIN	MAX	MIN	MAX	
f_{max}			100		100		MHz
t_{PLH}	$\overline{CLR}$	Any Q or $\overline{Q}$	4	10	4	9	ns
t_{PHL}			4.5	15	4.5	13	
t_{PLH}	CLK	Any Q or $\overline{Q}$	4	8.5	4	7.5	ns
t_{PHL}			4	11	4	10	

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

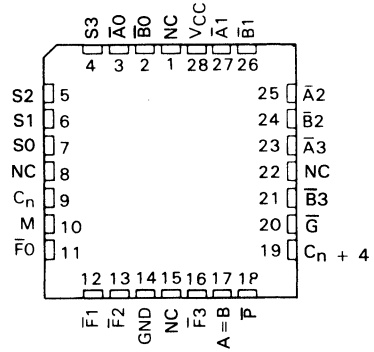
D2661, DECEMBER 1982—REVISED MAY 1986

- Package Options Include the 'AS181A in Compact 300-mil or Standard 600-mil Packages. The 'AS881A is Offered in 300-mil Packages. Both Devices are Available in Both Plastic and Ceramic Chip Carriers.
- Full Look-Ahead for High-Speed Operations on Long Words
- Arithmetic Operating Modes:
  - Addition
  - Subtraction
  - Shift Operand A One Position
  - Magnitude Comparison
  - Plus Twelve Other Arithmetic Operations
- Logic Function Modes
  - Exclusive-OR
  - Comparator
  - AND, NAND, OR, NOR
  - 'AS881A Provides Status Register Checks
  - Plus Ten Other Logic Operations
- Dependable Texas Instruments Quality and Reliability

SN54AS181A . . . JT OR JW PACKAGE
SN54AS881A . . . JT PACKAGE
SN74AS181A . . . DW, NT OR NW PACKAGE
SN74AS881A . . . DW OR NT PACKAGE
(TOP VIEW)

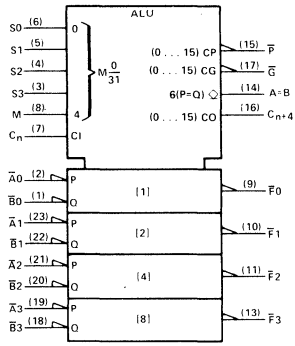


SN54AS181A, SN54AS881A . . . FK PACKAGE
SN74AS181A, SN74AS881A . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, JW, NT, and NW packages.

TYPICAL ADDITION TIMES (C_L = 15 pF, R_L = 280 Ω, T_A = 25°C)

NUMBER OF BITS	ADDITION TIMES			PACKAGE COUNT		CARRY METHOD BETWEEN ALUs
	USING 'AS881A AND 'AS882	USING 'AS181A AND 'AS882	USING 'S181 AND 'S182	ARITHMETIC LOGIC UNITS	LOOK-AHEAD CARRY GENERATORS	
1 to 4	5 ns	5 ns	11 ns	1		NONE
5 to 8	10 ns	10 ns	18 ns	2		RIPPLE
9 to 16	14 ns	14 ns	19 ns	3 or 4	1	FULL LOOK-AHEAD
17 to 64	19 ns	19 ns	28 ns	5 to 16	2 to 5	FULL LOOK-AHEAD

description

The 'AS181A and 'AS881A are arithmetic logic units (ALU)/function generators that have a complexity of 75 and 77 equivalent gates, respectively, on a monolithic chip. These circuits perform 16 binary arithmetic operations on two 4-bit words as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of two cascade-outputs (pins 15 and 17) for the four bits in the package. When used in conjunction with the SN54AS882 or SN74AS882 full carry look-ahead circuits, high-speed arithmetic operations can be performed. The typical addition times shown previously illustrate the little additional time required for addition of longer words when full carry look-ahead is employed. The method of cascading 'AS882 circuits with these ALUs to provide multilevel full carry look-ahead is illustrated under signal designations.

If high speed is not of importance, a ripple-carry input (C_n) and a ripple-carry output ($C_n + 4$) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

The 'AS181A and 'AS881A will accommodate active-high or active-low data if the pin designations are interpreted as follows:

PIN NUMBER	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-low data (Table 1)	$\overline{A}0$	$\overline{B}0$	$\overline{A}1$	$\overline{B}1$	$\overline{A}2$	$\overline{B}2$	$\overline{A}3$	$\overline{B}3$	$\overline{F}0$	$\overline{F}1$	$\overline{F}2$	$\overline{F}3$	C_n	C_{n+4}	$\overline{P}$	$\overline{G}$
Active-high data (Table 2)	A0	B0	A1	B1	A2	B2	A3	B3	F0	F1	F2	F3	$\overline{C}_n$	$\overline{C}_{n+4}$	X	Y

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A−B−1, which requires an end-around or forced carry to provide A−B.

The 'AS181A and 'AS881A can also be utilized as a comparator. The A = B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A = B). The ALU must be in the subtract mode with C_n = H when performing this comparison. The A = B output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output ($C_n + 4$) can also be used to supply relative magnitude information. Again, the ALU must be placed in the subtract mode by placing the function select input S3, S2, S1, S0 at L, H, H, L, respectively.

INPUT C_n	OUTPUT C_{n+4}	ACTIVE-LOW DATA (FIGURE 1)	ACTIVE-HIGH DATA (FIGURE 2)
H	H	A ≥ B	A ≤ B
H	L	A < B	A > B
L	H	A > B	A < B
L	L	A ≤ B	A ≥ B

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR, and OR functions.

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description (continued)

The 'AS881A has the same pinout and same functionality as the 'AS181A except for the $\overline{P}$, $\overline{G}$, and C_{n+4} outputs when the device is in the logic mode (M = H).

In the logic mode the 'AS881A provides the user with a status check on the input words A and B, and the ouput word F. While in the logic mode the $\overline{P}$, $\overline{G}$, and C_{n+4} outputs supply status information based upon the following logical combinations:

$\overline{P} = F0 + F1 + F2 + F3$
$\overline{G} = H$
$C_{n+4} = PC_n$

FUNCTION TABLE FOR INPUT BITS EQUAL/NOT EQUAL

S0 = S3 = H, S1 = S2 = L, and M = H

C_n	DATA INPUTS				OUTPUTS		
					$\overline{G}$	$\overline{P}$	C_{n+4}
H	$\overline{A}0 = \overline{B}0$	$\overline{A}1 = \overline{B}1$	$\overline{A}2 = \overline{B}2$	$\overline{A}3 = \overline{B}3$	H	L	H
L	$\overline{A}0 = \overline{B}0$	$\overline{A}1 = \overline{B}1$	$\overline{A}2 = \overline{B}2$	$\overline{A}3 = \overline{B}3$	H	L	L
X	$\overline{A}0 \neq \overline{B}0$	X	X	X	H	H	L
X	X	$\overline{A}1 \neq \overline{B}1$	X	X	H	H	L
X	X	X	$\overline{A}2 \neq \overline{B}2$	X	H	H	L
X	X	X	X	$\overline{A}3 \neq \overline{B}3$	H	H	L

FUNCTION TABLE FOR INPUT PAIRS HIGH/NOT HIGH

S0 = S1 = S3 = L, S2 = H, and M = H

C_n	DATA INPUTS				OUTPUTS		
					$\overline{G}$	$\overline{P}$	C_{n+4}
H	$\overline{A}0$ or $\overline{B}0$ = L	$\overline{A}1$ or $\overline{B}1$ = L	$\overline{A}2$ or $\overline{B}2$ = L	$\overline{A}3$ or $\overline{B}3$ = L	H	L	H
L	$\overline{A}0$ or $\overline{B}0$ = L	$\overline{A}1$ or $\overline{B}1$ = L	$\overline{A}2$ or $\overline{B}2$ = L	$\overline{A}3$ or $\overline{B}3$ = L	H	L	L
X	$\overline{A}0 = \overline{B}0$ = H	X	X	X	H	H	L
X	X	$\overline{A}1 = \overline{B}1$ = H	X	X	H	H	L
X	X	X	$\overline{A}2 = \overline{B}2$ = H	X	H	H	L
X	X	X	X	$\overline{A}3 = \overline{B}3$ = H	H	H	L

The combination of signals on the S3 through S0 control lines determine the operation performed on the data words to generate the output bits $\overline{F}i$. By monitoring the $\overline{P}$ and C_{n+4} outputs, the user can determine if all pairs of input bits are equal (see table above) or if any pair of inputs are both high (see table above). The 'AS881A has the unique feature of providing an A = B status while the exclusive-OR($\oplus$) function is being utilized. When the control inputs (S3, S2, S1, S0) equal H, L, L, H; a status check is generated to determine whether all pairs ($\overline{A}i$, $\overline{B}i$) are equal in the following manner: $\overline{P}$ = (A0 $\oplus$ B0) + (A1 $\oplus$ B1) + (A2 $\oplus$ B2) + (A3 $\oplus$ B3). This unique bit-by-bit comparison of the data words, which is available on the totem-pole $\overline{P}$ output, is particularly useful when cascading 'AS881s. As the A = B condition is sensed in the first stage, the signal is propagated through the same ports used for carry generation in the arithmetic mode ($\overline{P}$ and $\overline{G}$). Thus the A = B status is transmitted to the second stage more quickly without the need for external multiplexing logic. The A = B open-collector output allows the user to check the validity of the bit-by-bit result by comparing the two signals for parity.

If the user wishes to check for any pair of data inputs ($\overline{A}i$, $\overline{B}i$) being high, it is necessary to set the control lines (S3,S2,S1,S0) to L, H, L, L. The data pairs will then be ANDed together and the results ORed in the following manner: $\overline{P} = \overline{A}0\overline{B}0 + \overline{A}1\overline{B}1 + \overline{A}2\overline{B}2 + \overline{A}3\overline{B}3$.

S3	S2	S1	S0	M	$\overline{P}$ =
L	H	L	L	H	$\overline{A}0\overline{B}0 + \overline{A}1\overline{B}1 + \overline{A}2\overline{B}2 + \overline{A}3\overline{B}3$
H	L	L	H	H	(A0 $\oplus$ B0) + (A1 $\oplus$ B1) + (A2 $\oplus$ B2) + (A3 $\oplus$ B3)

signal designations

In both Figures 1 and 2, the polarity indicators (◺) indicate that the associated input or output is active-low with respect to the function shown inside the symbol and the symbols are the same in both figures. The signal designations in Figure 1 agree with the indicated internal functions based on active-low data, and are for use with the logic functions and arithmetic operations shown in Table 1. The signal designations have been changed in Figure 2 to accommodate the logic functions and arithmetic operations for the active-high data given in Table 2. The 'AS181A and 'AS881A together with 'AS882 and 'S182 can be used with the signal designation of either Figure 1 or Figure 2.

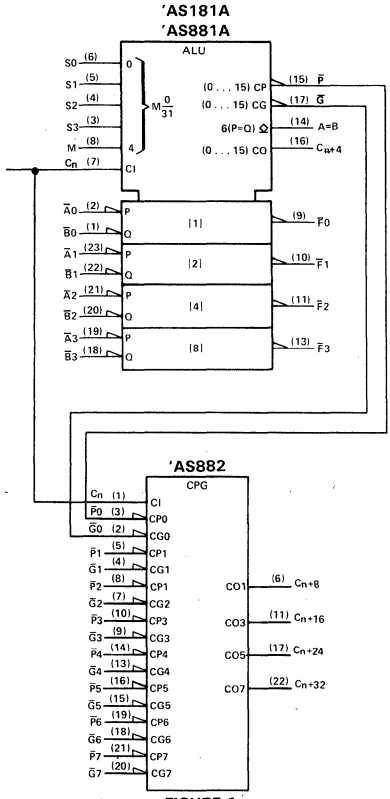

FIGURE 1
(USE WITH TABLE 1)

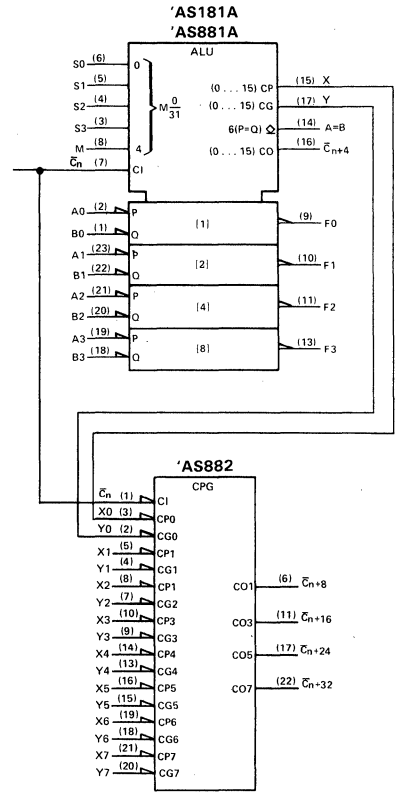

FIGURE 2
(USE WITH TABLE 2)

TABLE 1

SELECTION				ACTIVE-LOW DATA		
				M = H	M = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC FUNCTIONS	C_n = L (no carry)	C_n = H (with carry)
L	L	L	L	F = $\overline{A}$	F = A MINUS 1	F = A
L	L	L	H	F = $\overline{AB}$	F = AB MINUS 1	F = AB
L	L	H	L	F = $\overline{A}$ + B	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
L	L	H	H	F = 1	F = MINUS 1 (2's COMP)	F = ZERO
L	H	L	L	F = $\overline{A + B}$	F = A PLUS (A + $\overline{B}$)	F = A PLUS (A + $\overline{B}$) PLUS 1
L	H	L	H	F = $\overline{B}$	F = AB PLUS (A + $\overline{B}$)	F = AB PLUS (A + $\overline{B}$) PLUS 1
L	H	H	L	F = A $\oplus$ B	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	F = A + $\overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
H	L	L	L	F = $\overline{A}$B	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1
H	L	L	H	F = A $\oplus$ B	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = A$\overline{B}$ PLUS (A + B)	F = A$\overline{B}$ PLUS (A + B) PLUS 1
H	L	H	H	F = A + B	F = (A + B) PLUS 1	F = (A + B) PLUS 1
H	H	L	L	F = 0	F = A PLUS A†	F = A PLUS A PLUS 1
H	H	L	H	F = A$\overline{B}$	F = AB PLUS A	F = AB PLUS A PLUS 1
H	H	H	L	F = AB	F = A$\overline{B}$ PLUS A	F = A$\overline{B}$ PLUS A PLUS 1
H	H	H	H	F = A	F = A	F = A PLUS 1

TABLE 2

SELECTION				ACTIVE-HIGH DATA		
				M = H	M = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC FUNCTIONS	$\overline{C}_n$ = H (no carry)	$\overline{C}_n$ = L (with carry)
L	L	L	L	F = $\overline{A}$	F = A	F = A PLUS 1
L	L	L	H	F = $\overline{A + B}$	F = A + B	F = (A + B) PLUS 1
L	L	H	L	F = $\overline{AB}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
L	L	H	H	F = 0	F = MINUS 1 (2's COMPL)	F = ZERO
L	H	L	L	F = $\overline{AB}$	F = A PLUS A$\overline{B}$	F = A PLUS A$\overline{B}$ PLUS 1
L	H	L	H	F = $\overline{B}$	F = (A + B) PLUS A$\overline{B}$	F = (A + B) PLUS A$\overline{B}$ PLUS 1
L	H	H	L	F = A $\oplus$ B	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	F = A$\overline{B}$	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
H	L	L	L	F = $\overline{A}$ + B	F = A PLUS AB	F = A PLUS AB PLUS 1
H	L	L	H	F = A $\oplus$ B	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = (A + $\overline{B}$) PLUS AB	F = (A + $\overline{B}$) PLUS AB PLUS 1
H	L	H	H	F = AB	F = AB MINUS 1	F = AB
H	H	L	L	F = 1	F = A PLUS A†	F = A PLUS A PLUS 1
H	H	L	H	F = A + $\overline{B}$	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1
H	H	H	L	F = A + B	F = (A + $\overline{B}$) PLUS A	F = (A + $\overline{B}$) PLUS A PLUS 1
H	H	H	H	F = A	F = A MINUS 1	F = A

†Each bit is shifted to the next more significant position.

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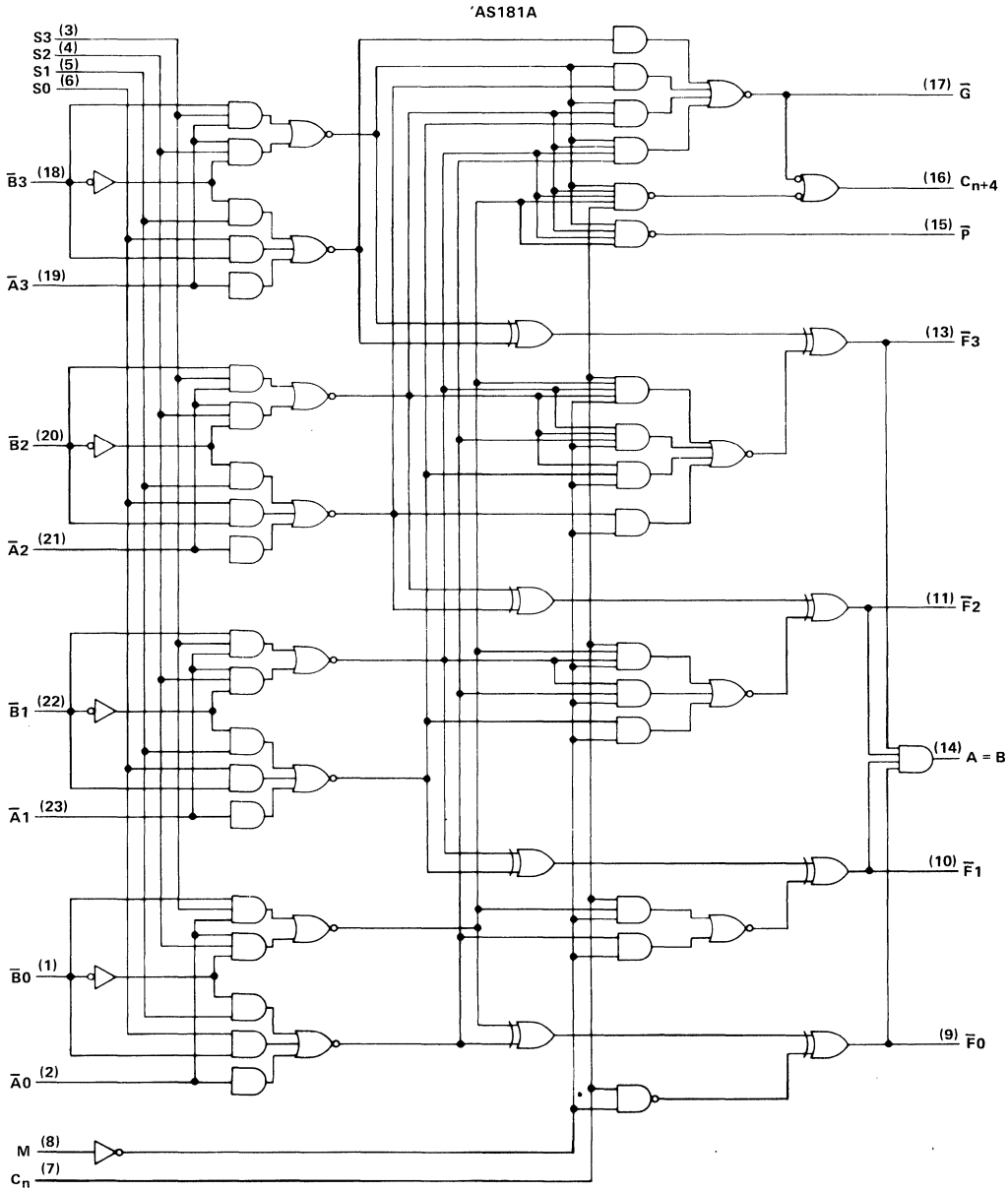
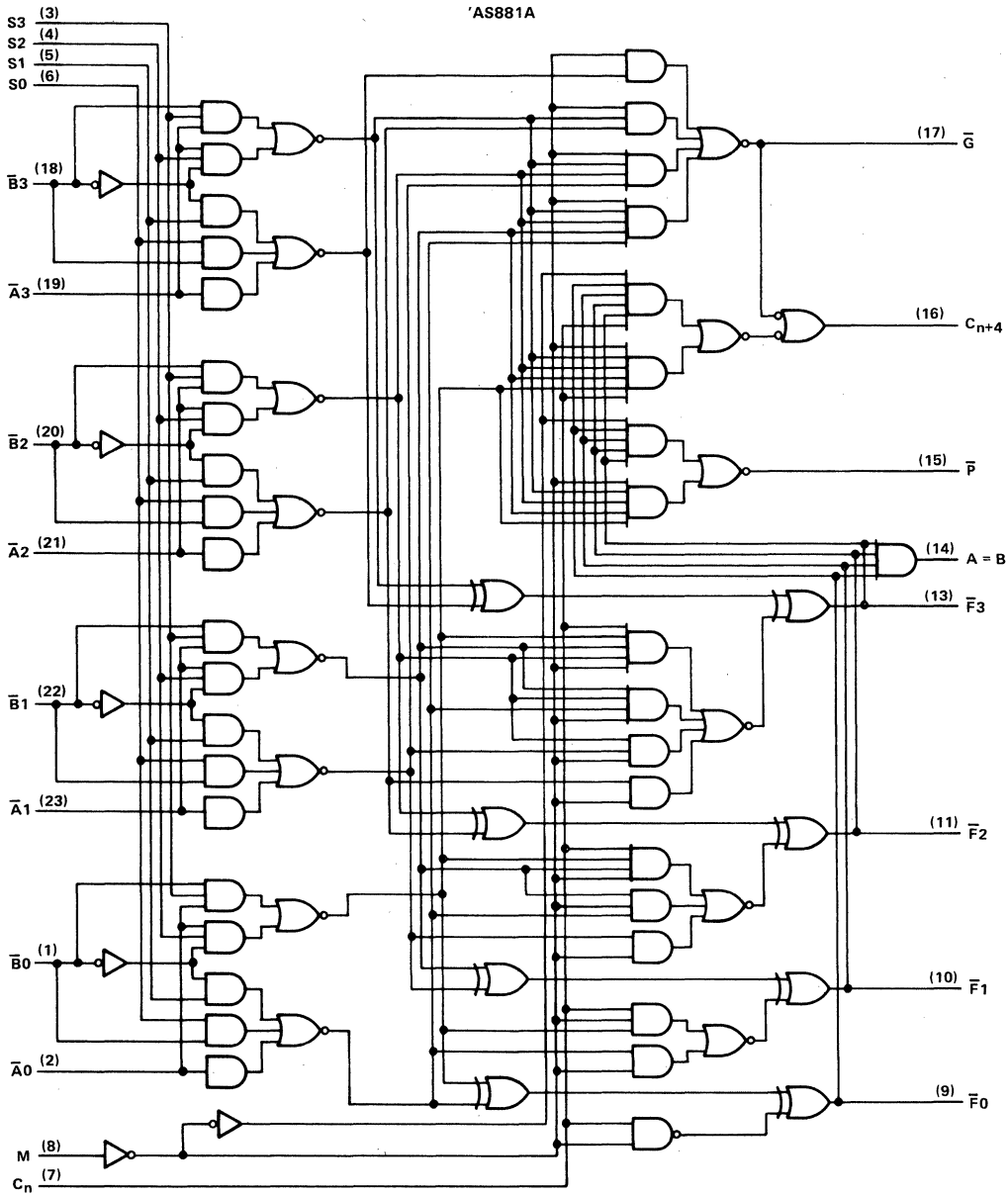
logic diagram (positive logic)



Pin numbers shown are for DW, JT, JW, NT, and NW packages.

logic diagram (positive logic)



Pin numbers shown are for DW, JT, JW, NT, and NW packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage (A = B output only) . . . . . 7 V
Operating free-air temperature range: SN54AS181A, SN54AS881A . . . . . −55°C to 125°C
SN74AS181A, SN74AS881A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54AS'			SN74AS'			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{OH}	High-level output voltage	A = B output only			5.5			5.5	V
I_{OH}	High-level output current	All outputs except A = B and $\overline{G}$			−2			−2	mA
		$\overline{G}$			−3			−3	mA
I_{OL}	Low-level output current	All outputs except $\overline{G}$			20			20	mA
		$\overline{G}$			48			48	mA
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS'			SN74AS'			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	Any output except A = B	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
	$\overline{G}$	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.4		2.4	3.4		V
I_{OH}	A = B	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	Any output except $\overline{G}$	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.3	0.5		0.3	0.5	V
	$\overline{G}$	V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.4	0.5		0.4	0.5	V
I_I	M input	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	Any A or B input					0.3			0.3	
	Any S input					0.4			0.4	
	Carry input					0.6			0.6	
I_{IH}	M input	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	Any A or B input					60			60	
	Any S input					80			80	
	Carry input					120			120	
I_{IL}	M input	V_{CC} = 5.5 V,	V_I = 0.4 V			−2			−2	mA
	Any A or B input					−6			−6	
	Any S input					−8			−8	
	Carry input					−12			−12	
I_O‡	All outputs except A = B and $\overline{G}$	V_{CC} = 5.5 V,	V_O = 2.25 V	−30	−45	−112	−30	−45	−112	mA
	$\overline{G}$				−165			−165		
I_{CC}		V_{CC} = 5.5 V	'AS181A		135	200		135	200	mA
			'AS881A		135	210		135	210	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit current, I_{OS}.

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switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC} = 5 V, C_L = 15 pF, R_L = 500 Ω (280 Ω for A = B), T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF (15 pF for A = B), R_L = 500 Ω (280 Ω for A = B), T_A = MIN to MAX						UNIT
				'AS181A 'AS881A	SN54AS181A SN54AS881A			SN74AS181A SN74AS881A			
				MIN TYP† MAX	MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{pd}	C_n	C_{n+4}		5	2	7	11	2	7	9	ns
t_{pd}	Any $\overline{A}$ or $\overline{B}$	C_{n+4}	M = 0 V, S1 = S2 = 0 V, S0 = S3 = 4.5 V ($\overline{SUM}$ mode)	6	2	8	14	2	8	12	ns
t_{pd}	Any $\overline{A}$ or $\overline{B}$	C_{n+4}	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)	7	2	8	20	2	8	16	ns
t_{pd}	C_n	Any $\overline{F}$	M = 0 V ($\overline{SUM}$ or $\overline{DIFF}$ mode)	5	3	6	11	3	6	9	ns
t_{pd}	Any $\overline{A}$ or $\overline{B}$	$\overline{G}$	M = 0 V, S1 = S2 = 0 V, S0 = S3 = 4.5 V ($\overline{SUM}$ mode)	4	2	5	9	2	5	7	ns
t_{pd}	Any $\overline{A}$ or $\overline{B}$	$\overline{G}$	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)	5	2	6	12	2	6	9	ns
t_{pd}	Any $\overline{A}$ or $\overline{B}$	$\overline{P}$	M = 0 V, S1 = S2 = 0 V, S0 = S3 = 4.5 V ($\overline{SUM}$ mode)	5	2	6	11	2	6	8	ns
t_{pd}	Any $\overline{A}$ or $\overline{B}$	$\overline{P}$	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)	5	2	6	13	2	6	10	ns
t_{pd}	$\overline{A}i$ or $\overline{B}i$	$\overline{F}i$	M = 0 V, S1 = S2 = 0 V, S0 = S3 = 4.5 V ($\overline{SUM}$ mode)	5	2	5	11	2	5	8	ns
t_{pd}	$\overline{A}i$ or $\overline{B}i$	$\overline{F}i$	M = 0 V, S0 = S1 = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)	5	2	6	12	2	6	10	ns
t_{pd}	$\overline{A}i$ or $\overline{B}i$	$\overline{F}i$	M = 4.5 V (LOGIC mode)	6	2	6	16	2	6	11	ns
t_{pd}	Any $\overline{A}$ or $\overline{B}$	A = B	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)	12	4	14	26	4	14	21	ns

additional 'AS881A switching characteristics involving status checks (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC} = 5 V, C_L = 15 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
				'AS881A	SN54AS881A			SN74AS881A			
				MIN TYP† MAX	MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{pd}	Any $\overline{A}$ or $\overline{B}$	$\overline{P}$	C_n = 4.5V, M = 4.5 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V, Equality ($\overline{A}i = \overline{B}i$ or $\overline{A}i \neq \overline{B}i$)	8	2	10	19	2	10	15	ns
t_{pd}	Any $\overline{A}$ or $\overline{B}$	C_{n+4}	C_n = 4.5 V, M = 4.5 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V, Equality ($\overline{A}i = \overline{B}i$ or $\overline{A}i \neq \overline{B}i$)	10	2	12	24	2	12	18	ns
t_{pd}	Any $\overline{A}$ or $\overline{B}$	$\overline{P}$	C_n = 4.5 V, M = 4.5 V, S2 = 4.5 V, S0 = S1 = S3 = 0 V, ($\overline{A}i = \overline{B}i$ = H or $\overline{A}i$ or $\overline{B}i$ = L)	8	2	10	19	2	10	15	ns
t_{pd}	Any $\overline{A}$ or $\overline{B}$	C_{n+4}	C_n = 4.5 V, M = 4.5 V, S2 = 4.5 V, S0 = S1 = S3 = 0 V, ($\overline{A}i = \overline{B}i$ = H or $\overline{A}i$ or $\overline{B}i$ = L)	11	2	13	25	2	13	19	ns

t_{pd} = t_{PHL} or t_{PLH}
†All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

PARAMETER MEASUREMENT INFORMATION

$\overline{\text{SUM}}$ MODE TEST TABLE

FUNCTION INPUTS: S0 = S3 = 4.5 V, S1 = S2 = M = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (SEE NOTE 1)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} / t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}i$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}i$	In-Phase
t_{PLH} / t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}i$	None	$\overline{A}i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	In-Phase
t_{PLH} / t_{PHL}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_{n+4}	In-Phase
t_{PLH} / t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{B}i$	None	$\overline{A}i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}	Out-of-Phase

$\overline{\text{DIFF}}$ MODE TEST TABLE

FUNCTION INPUTS: S1 = S2 = 4.5 V, S0 = S3 = M = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (SEE NOTE 1)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} / t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{A}$	Remaining B, C_n	$\overline{F}i$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{A}$	Remaining B, C_n	$\overline{F}i$	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}i$	None	$\overline{A}i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{A}$	remaining $\overline{B}$, C_n	A = B	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B	Out-of-Phase
t_{PLH} / t_{PHL}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	C_{n+4} or any $\overline{F}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	None	Remaining $\overline{A}$, $\overline{B}$, C_n	C_{n+4}	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{B}i$	None	$\overline{A}i$	None	Remaining $\overline{A}$, $\overline{B}$, C_n	C_{n+4}	In-Phase

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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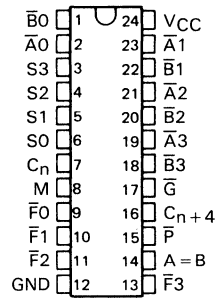
SN54AS181B, SN74AS181B
ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

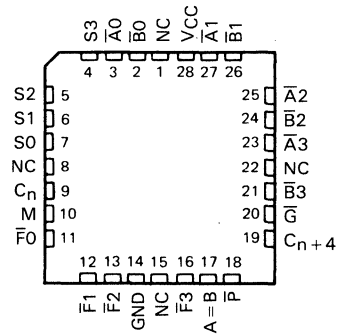
D2661, DECEMBER 1985—REVISED MAY 1986

- Package Options Include Compact 300-mil or Standard 600-mil DIPs and Both Plastic and Ceramic Chip Carriers
- Full Look-Ahead for High-Speed Operations on Long Words
- Arithmetic Operating Modes:
  - Addition
  - Subtraction
  - Shift Operand A One Position
  - Magnitude Comparison
  - Plus Twelve Other Arithmetic Operations
- Logic Function Modes
  - Exclusive-OR
  - Comparator
  - AND, NAND, OR, NOR
- Dependable Texas Instruments Quality and Reliability

SN54AS181B . . . JT OR JW PACKAGE
SN74AS181B . . . N OR NT PACKAGE
(TOP VIEW)

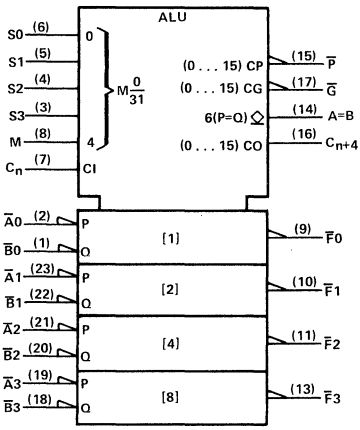


SN54AS181B . . . FK PACKAGE
SN74AS181B . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for J, JT, N, and NT packages.

TYPICAL ADDITION TIMES (C_L = 15 pF, R_L = 280 Ω, T_A = 25°C)

NUMBER OF BITS	ADDITION TIMES			PACKAGE COUNT		CARRY METHOD BETWEEN ALUs
	USING 'AS181B AND 'AS882	USING 'AS881B AND 'AS882	USING 'S181 AND 'S182	ARITHMETIC LOGIC UNITS	LOOK-AHEAD CARRY GENERATORS	
1 to 4	5 ns	5 ns	11 ns	1		NONE
5 to 8	10 ns	10 ns	18 ns	2		RIPPLE
9 to 16	14 ns	14 ns	19 ns	3 or 4	1	FULL LOOK-AHEAD
17 to 64	19 ns	19 ns	28 ns	5 to 16	2 to 5	FULL LOOK-AHEAD

description

The 'AS181B arithmetic logic units (ALU)/function generators have a complexity of 75 equivalent gates on a monolithic chip. These circuits perform 16 binary arithmetic operations on two 4-bit words as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of two cascade-outputs, $\overline{G}$ and $\overline{P}$, for the four bits in the package. When used in conjunction with the SN54AS882 or SN74AS882 full carry look-ahead circuits, high-speed arithmetic operations can be performed. The typical addition times shown previously illustrate the little additional time required for addition of longer words when full carry look-ahead is employed. The method of cascading 'AS882 circuits with these ALUs to provide multilevel full carry look-ahead is illustrated under signal designations.

If high speed is not of importance, a ripple-carry input (C_n) and a ripple-carry output ($C_n + 4$) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

The 'AS181B will accommodate active-high or active-low data if the pin designations are interpreted as follows:

PIN NUMBER	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-low data (Table 1)	$\overline{A}0$	$\overline{B}0$	$\overline{A}1$	$\overline{B}1$	$\overline{A}2$	$\overline{B}2$	$\overline{A}3$	$\overline{B}3$	$\overline{F}0$	$\overline{F}1$	$\overline{F}2$	$\overline{F}3$	C_n	C_{n+4}	$\overline{P}$	$\overline{G}$
Active-high data (Table 2)	A0	B0	A1	B1	A2	B2	A3	B3	F0	F1	F2	F3	$\overline{C}_n$	$\overline{C}_{n+4}$	X	Y

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A−B−1, which requires an end-around or forced carry to provide A−B.

The 'AS181B can also be utilized as a comparator. The A = B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A = B). The ALU must be in the subtract mode with C_n = H when performing this comparison. The A = B output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output ($C_n + 4$) can also be used to supply relative magnitude information. Again, the ALU must be placed in the subtract mode by placing the function select input S3, S2, S1, S0 at L, H, H, L, respectively.

INPUT C_n	OUTPUT C_{n+4}	ACTIVE-LOW DATA (FIGURE 1)	ACTIVE-HIGH DATA (FIGURE 2)
H	H	A≥B	A≤B
H	L	A<B	A>B
L	H	A>B	A<B
L	L	A≤B	A≥B

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR, and OR functions.

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signal designations

In both Figures 1 and 2, the polarity indicators (▷) indicate that the associated input or output is active-low with respect to the function shown inside the symbol and the symbols are the same in both figures. The signal designations in Figure 1 agree with the indicated internal functions based on active-low data, and are for use with the logic functions and arithmetic operations shown in Table 1. The signal designations have been changed in Figure 2 to accommodate the logic functions and arithmetic operations for the active-high data given in Table 2. The 'AS181B together with 'AS882 and 'S182 can be used with the signal designation of either Figure 1 or Figure 2.

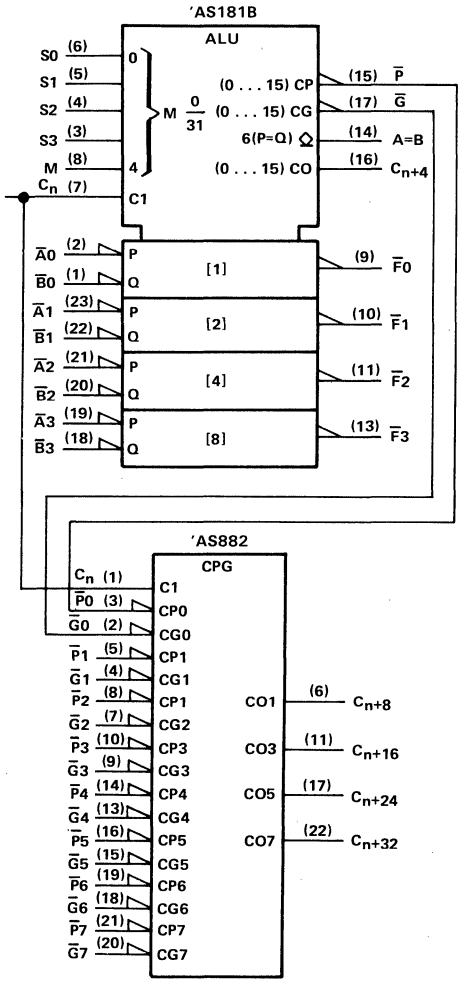

FIGURE 1
(USE WITH TABLE I)

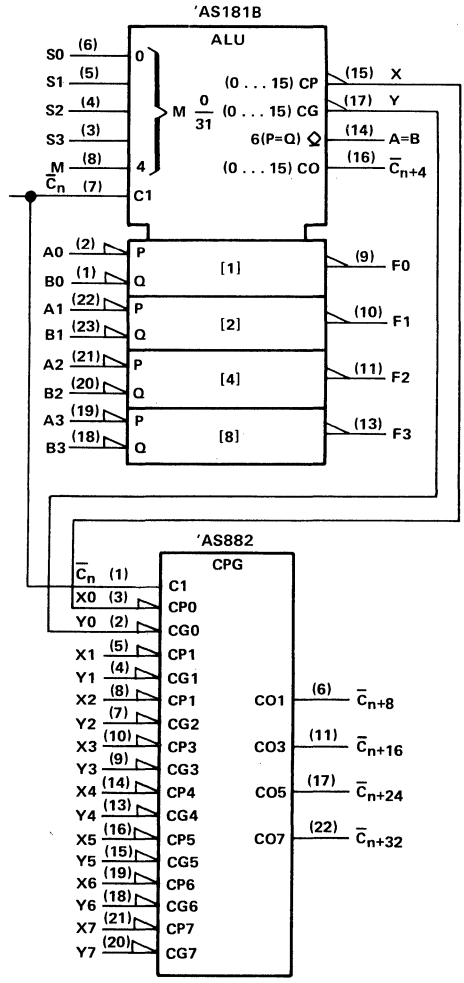

FIGURE 2
(USE WITH TABLE II)

TABLE I

SELECTION				ACTIVE-LOW DATA		
				M = H	M = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC FUNCTIONS	C_n = L (no carry)	C_n = H (with carry)
L	L	L	L	F = $\overline{A}$	F = A MINUS 1	F = A
L	L	L	H	F = $\overline{AB}$	F = AB MINUS 1	F = AB
L	L	H	L	F = $\overline{A}$ + B	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
L	L	H	H	F = 1	F = MINUS 1 (2's COMP)	F = ZERO
L	H	L	L	F = $\overline{A + B}$	F = A PLUS (A + $\overline{B}$)	F = A PLUS (A + $\overline{B}$) PLUS 1
L	H	L	H	F = $\overline{B}$	F = AB PLUS (A + $\overline{B}$)	F = AB PLUS (A + $\overline{B}$) PLUS 1
L	H	H	L	F = $\overline{A \oplus B}$	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	F = A + $\overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
H	L	L	L	F = $\overline{A}$B	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1
H	L	L	H	F = A $\oplus$ B	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = A$\overline{B}$ PLUS (A + B)	F = A$\overline{B}$ PLUS (A + B) PLUS 1
H	L	H	H	F = A + B	F = (A + B)	F = (A + B) PLUS 1
H	H	L	L	F = 0	F = A PLUS A*	F = A PLUS A PLUS 1
H	H	L	H	F = A$\overline{B}$	F = AB PLUS A	F = AB PLUS A PLUS 1
H	H	H	L	F = AB	F = A$\overline{B}$ PLUS A	F = A$\overline{B}$ PLUS A PLUS 1
H	H	H	H	F = A	F = A	F = A PLUS 1

TABLE II

SELECTION				ACTIVE-HIGH DATA		
				M = H	M = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC FUNCTIONS	$\overline{C}_n$ = H (no carry)	$\overline{C}_n$ = L (with carry)
L	L	L	L	F = $\overline{A}$	F = A	F = A PLUS 1
L	L	L	H	F = $\overline{A + B}$	F = A + B	F = (A + B) PLUS 1
L	L	H	L	F = $\overline{A}$B	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
L	L	H	H	F = 0	F = MINUS 1 (2's COMP)	F = ZERO
L	H	L	L	F = $\overline{AB}$	F = A PLUS A$\overline{B}$	F = A PLUS A$\overline{B}$ PLUS 1
L	H	L	H	F = $\overline{B}$	F = (A + B) PLUS A$\overline{B}$	F = (A + B) PLUS A$\overline{B}$ PLUS 1
L	H	H	L	F = A $\oplus$ B	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	F = A$\overline{B}$	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
H	L	L	L	F = $\overline{A}$ + B	F = A PLUS AB	F = A PLUS AB PLUS 1
H	L	L	H	F = $\overline{A \oplus B}$	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = (A + $\overline{B}$) PLUS AB	F = (A + $\overline{B}$) PLUS AB PLUS 1
H	L	H	H	F = AB	F = AB MINUS 1	F = AB
H	H	L	L	F = 1	F = A PLUS A*	F = A PLUS A PLUS 1
H	H	L	H	F = A + $\overline{B}$	F = (A + B) PLUS A	A = (A + B) PLUS A PLUS 1
H	H	H	L	F = A + B	F = (A + $\overline{B}$) PLUS A	F = (A + $\overline{B}$) PLUS A PLUS 1
H	H	H	H	F = A	F = A MINUS 1	F = A

*Each bit is shifted to the next more significant position.

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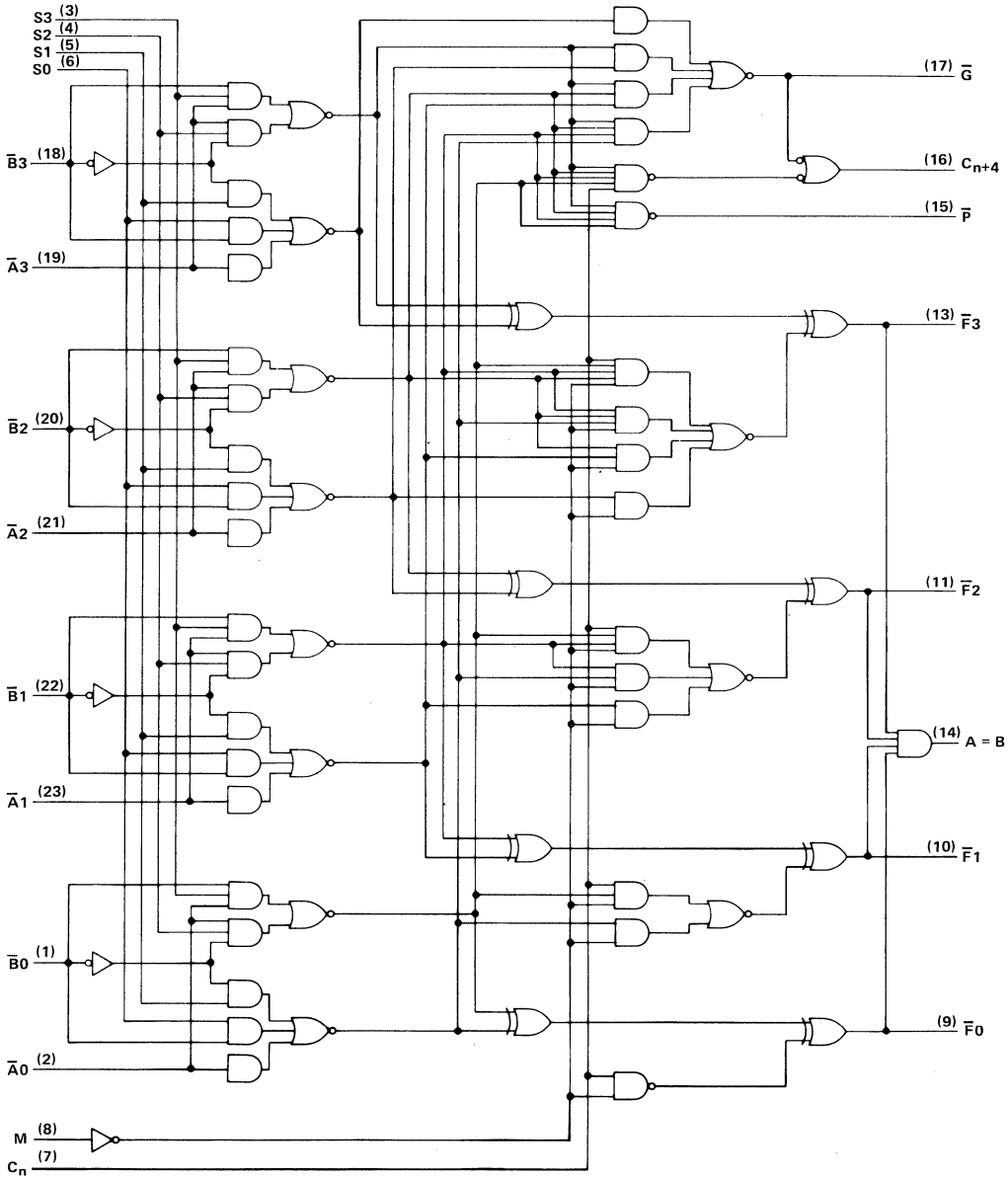
logic diagram (positive logic)



Pin numbers shown are for J, JT, N, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage (A = B output only) . . . . . 7 V
Operating free-air temperature range: SN54AS181B . . . . . −55°C to 125°C
SN74AS181B . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54AS181B			SN74AS181B			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{OH}	High-level output voltage	A = B output only			5.5			5.5	V
I_{OH}	High-level output current	All outputs except A = B and $\overline{G}$			−2			−2	mA
		$\overline{G}$			−3			−3	mA
I_{OL}	Low-level output current	All outputs except $\overline{G}$			20			20	mA
		$\overline{G}$			48			48	mA
T_A	Operating free-air temperature		−55		125	0		70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS181B			SN74AS181B			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	Any output except A = B	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
	$\overline{G}$	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.4		2.4	3.4		V
I_{OH}	A = B	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	Any output except $\overline{G}$	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.3	0.5		0.3	0.5	V
	$\overline{G}$	V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.4	0.5		0.4	0.5	V
I_I	M input	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	Any A or B input					0.3			0.3	
	Any S input					0.4			0.4	
	Carry input					0.6			0.6	
I_{IH}	M input	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	Any A or B input					60			60	
	Any S input					80			80	
	Carry input					120			120	
I_{IL}	M input	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	Any A or B input					−1.5			−1.5	
	Any S input					−2			−2	
	Carry input					−3			−3	
I_O‡	All outputs except A = B and $\overline{G}$	V_{CC} = 5.5 V,	V_O = 2.25 V	−30	−45	−112	−30	−45	−112	mA
	$\overline{G}$			−30		−125	−30		−125	
I_{CC}		V_{CC} = 5.5 V			74	117		74	117	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
				SN54AS181B		SN74AS181B		
				MIN	MAX	MIN	MAX	
t_{PLH}	C_n	C_{n+4}		3	9	3	8.5	ns
t_{PHL}				2	7	2	6.5	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	C_{n+4}	M = 0 V, S1 = S2 = 0 V, S0 = S3 = 4.5 V (SUM mode)	3.5	13	5	12	ns
t_{PHL}				3.5	12.5	5	12	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	C_{n+4}	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V (DIFF mode)	5	14.5	5	13	ns
t_{PHL}				5	13.5	5	12.5	
t_{PLH}	C_n	Any $\overline{F}$	M = 0 V (SUM or DIFF mode)	3	10.5	3	9	ns
t_{PHL}				3	8	3	7.5	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	$\overline{G}$	M = 0 V, S1 = S2 = 0 V, S0 = S3 = 4.5 V (SUM mode)	3	8.5	3	8	ns
t_{PHL}				2	7	2	6	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	$\overline{G}$	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V (DIFF mode)	3	10.5	3	9.5	ns
t_{PHL}				2	9	2	7	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	$\overline{P}$	M = 0 V, S1 = S2 = 0 V, S0 = S3 = 4.5 V (SUM mode)	3	8.5	3	7.5	ns
t_{PHL}				2	7.5	2	6	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	$\overline{P}$	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V (DIFF mode)	3	10.5	3	9	ns
t_{PHL}				3	8.5	3	8	
t_{PLH}	$\overline{A}i$ or $\overline{B}i$	$\overline{F}i$	M = 0 V, S1 = S2 = 0 V, S0 = S3 = 4.5 V (SUM mode)	3	11	3	9.5	ns
t_{PHL}				3	9	3	7.5	
t_{PLH}	$\overline{A}i$ or $\overline{B}i$	$\overline{F}i$	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V (DIFF mode)	3	12	3	10.5	ns
t_{PHL}				3	11	3	9.5	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	Any $\overline{F}$	M = 0 V, S1 = S2 = 0 V, S0 = S3 = 4.5 V (SUM mode)	3	13.5	3	12	ns
t_{PHL}				3	13	3	11.5	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	Any $\overline{F}$	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V (DIFF mode)	3	16	3	14.5	ns
t_{PHL}				3	13	3	12.5	
t_{PLH}	$\overline{A}i$ or $\overline{B}i$	$\overline{F}i$	M = 4.5 V (LOGIC mode)	3	12.5	3	11	ns
t_{PHL}				3	10	3	9.5	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	A = B	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V (DIFF mode)	4	19	4	17	ns
t_{PHL}				5	18.5	5	15	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

PARAMETER MEASUREMENT INFORMATION

SUM MODE TEST TABLE

FUNCTION INPUTS: S0 = S3 = 4.5 V, S1 = S2 = M = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (SEE NOTE 1)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}i$	In-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}i$	In-Phase
t_{PLH} t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PLH} t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	In-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	None	$\overline{A}i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	In-Phase
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_{n+4}	In-Phase
t_{PLH} t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}	Out-of-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	None	$\overline{A}i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}	Out-of-Phase

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

PARAMETER MEASUREMENT INFORMATION

DIFF MODE TEST TABLE
FUNCTION INPUTS: S1 = S2 = 4.5 V, S0 = S3 = M = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (SEE NOTE 1)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}i$	In-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}i$	Out-of-Phase
t_{PLH} t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	Out-of-Phase
t_{PLH} t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	In-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	None	$\overline{A}i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	Out-of-Phase
t_{PLH} t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B	In-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B	Out-of-Phase
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	C_n+4 or any $\overline{F}$	In-Phase
t_{PLH} t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	None	Remaining $\overline{A}$, $\overline{B}$, C_n	C_n+4	Out-of-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	None	$\overline{A}i$	None	Remaining $\overline{A}$, $\overline{B}$, C_n	C_n+4	In-Phase

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

PARAMETER MEASUREMENT INFORMATION

LOGIC MODE TEST TABLE

FUNCTION INPUTS: S1 = S2 = M = 4.5 V, S0 = S3 = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (SEE NOTE 1)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} / t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}i$	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}i$	Out-of-Phase

INPUT BITS EQUAL/NOT EQUAL TEST TABLE

FUNCTION INPUTS: S0 = S3 = M = 4.5 V, S1 = S2 = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (SEE NOTE 1)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} / t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	$\overline{P}$	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	$\overline{P}$	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	$\overline{P}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}i$	None	$\overline{A}i$	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	$\overline{P}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	C_{n+4}	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	C_{n+4}	In-Phase
t_{PLH} / t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	C_{n+4}	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{B}i$	None	$\overline{A}i$	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	C_{n+4}	Out-of-Phase

INPUT PAIRS HIGH/NOT HIGH TEST TABLE

FUNCTION INPUTS: S2 = M = 4.5 V, S0 = S1 = S3 = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (SEE NOTE 1)
		APPLY 4.5 V	APPLY GND	APPLY 4.5V	APPLY GND		
t_{PLH} / t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	Remaining $\overline{A}$, C_n	Remaining $\overline{B}$	$\overline{P}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	$\overline{P}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	Remaining $\overline{A}$, C_n	Remaining $\overline{B}$	C_{n+4}	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	C_{n+4}	Out-of-Phase

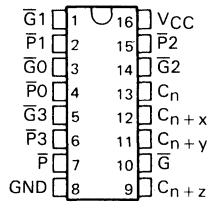
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54AS182, SN74AS182
LOOK-AHEAD CARRY GENERATOR

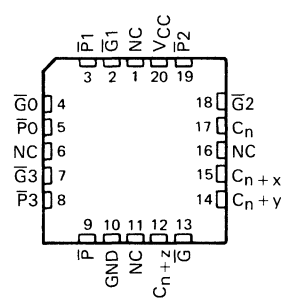
D2661, DECEMBER 1983—REVISED MAY 1986

- **High-Speed Replacement for the 'S182**
- **Offers Carry Functions in a Compatible Form for Direct Connections to the ALU**
- **Cascadable to Perform Look-Ahead Across n-Bit Adders**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54AS182 . . . J PACKAGE
SN74AS182 . . . D OR N PACKAGE
(TOP VIEW)



SN54AS182 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

PIN DESIGNATIONS

ALTERNATIVE	DESIGNATIONS†	FUNCTION
$\overline{G}0$, $\overline{G}1$, $\overline{G}2$, $\overline{G}3$	G0, G1, G2, G3	Carry Generate Inputs
$\overline{P}0$, $\overline{P}1$, $\overline{P}2$, $\overline{P}3$	P0, P1, P2, P3	Carry Propagate Inputs
C_n	$\overline{C}_n$	Carry Input
C_{n+x}, C_{n+y}, C_{n+z}	$\overline{C}_{n+x}$, $\overline{C}_{n+y}$, $\overline{C}_{n+z}$	Carry Outputs
$\overline{G}$	Y	Carry Generate Output
$\overline{P}$	X	Carry Propagate Output
V_{CC}		Supply Voltage
GND		Ground

† Interpretations are illustrated in connection with the Function Tables for the 'AS181B and 'AS881A.

description

The 'AS182 look-ahead carry generators are capable of anticipating a carry across four binary adders or group of adders. They are cascadable to perform full look-ahead across n-bit adders.

This generator, when used in conjunction with the 'AS181B or 'AS881A Arithmetic Logic Unit ALU, provides high-speed carry look-ahead capability for any word length. The 'AS182 generates the look-ahead (anticipated carry) across a group of four ALUs. In addition, other carry look-ahead circuits may be employed to anticipate carry-across sections of four look-ahead packages up to n-bits. The method of cascading 'AS182 circuits to perform multilevel look-ahead is illustrated under the typical application data.

The carry functions (inputs, outputs, generate, and propagate) of the look-ahead generators are implemented in the compatible forms for direct connections to the ALU. Reinterpretations of carry functions as explained on the 'AS181B and 'AS881A data sheet are also applicable to and compatible with the look-ahead generator. Logic equations for the 'AS182 are:

$$C_{n+x} = G0 + P0\,C_n$$
$$C_{n+y} = G1 + P1\,G0 + P1\,P0\,C_n$$
$$C_{n+z} = G2 + P2\,G1 + P2\,P1\,G0 + P2\,P1\,P0\,C_n$$
$$\overline{G} = \overline{G3 + P3\,G2 + P3\,P2\,G1 + P3\,P2\,P1\,G0}$$
$$\overline{P} = \overline{P3\,P2\,P1\,P0}$$

or

$$\overline{C}_{n+x} = \overline{Y0\,(X0 + C_n)}$$
$$\overline{C}_{n+y} = \overline{Y1\,[X1 + Y0\,(X0 + C_n)]}$$
$$\overline{C}_{n+z} = \overline{Y2\,\{X2 + Y1\,[X1 + Y0\,(X0 + C_n)]\}}$$
$$Y = Y3\,(X3 + Y2)\,(X3 + X2 + Y1)\,(X3 + X2 + X1 + Y0)$$
$$X = X3 + X2 + X1 + X0$$

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FUNCTION TABLE FOR $\overline{G}$ OUTPUT

INPUTS							OUTPUT
$\overline{G}3$	$\overline{G}2$	$\overline{G}1$	$\overline{G}0$	$\overline{P}3$	$\overline{P}2$	$\overline{P}1$	$\overline{G}$
L	X	X	X	X	X	X	L
X	L	X	X	L	X	X	L
X	X	L	X	L	L	X	L
X	X	X	L	L	L	L	L
All other combinations							H

FUNCTION TABLE FOR $\overline{P}$ OUTPUT

INPUTS				OUTPUT
$\overline{P}3$	$\overline{P}2$	$\overline{P}1$	$\overline{P}0$	$\overline{P}$
L	L	L	L	L
All other combinations				H

FUNCTION TABLE FOR C_{n+x} OUTPUT

INPUTS			OUTPUT
$\overline{G}0$	$\overline{P}0$	C_n	C_{n+x}
L	X	X	H
X	L	H	H
All other combinations			L

FUNCTION TABLE C_{n+y} OUTPUT

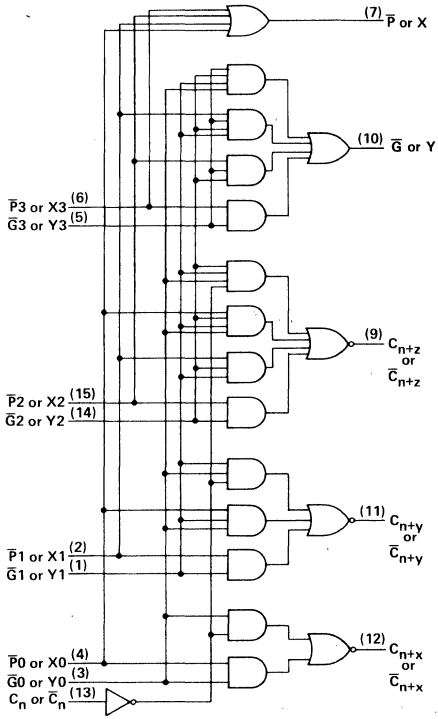
INPUTS					OUTPUT
$\overline{G}1$	$\overline{G}0$	$\overline{P}1$	$\overline{P}0$	C_n	C_{n+y}
L	X	X	X	X	H
X	L	L	X	X	H
X	X	L	L	H	H
All other combinations					L

FUNCTION TABLE FOR C_{n+z} OUTPUT

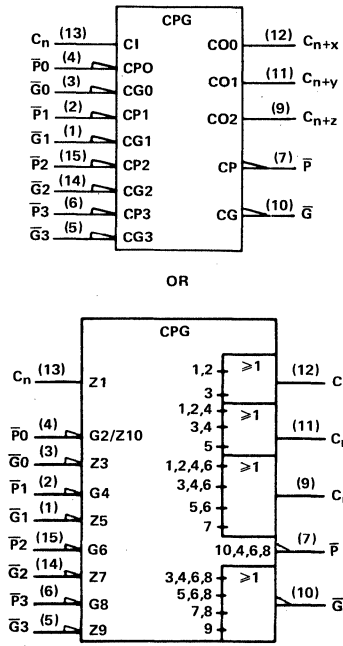
INPUTS							OUTPUT
$\overline{G}2$	$\overline{G}1$	$\overline{G}0$	$\overline{P}2$	$\overline{P}1$	$\overline{P}0$	C_n	C_{n+z}
L	X	X	X	X	X	X	H
X	L	X	L	X	X	X	H
X	X	L	L	L	X	X	H
X	X	X	L	L	L	H	H
All other combinations							L

H = high-level, L = low level, X = irrelevant.
Any inputs not shown in a given table are irrelevant with respect to that output.

logic diagram (positive logic)



logic symbols†



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers are for D, J, and N packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS182 . . . . . −55°C to 125°C
SN74AS182 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS182			SN74AS182			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS182			SN74AS182			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.3	0.5		0.3	0.5	V
I_I	C_n	V_{CC} = 5.5 V,	V_I = 7.0 V			0.1			0.1	mA
	$\overline{P}3$					0.2			0.2	
	$\overline{P}2$					0.3			0.3	
	$\overline{P}0$, $\overline{P}1$, $\overline{G}3$					0.4			0.4	
	$\overline{G}0$, $\overline{G}2$					0.7			0.7	
	$\overline{G}1$					0.8			0.8	
I_{IH}	C_n	V_{CC} = 5.5 V,	V_I = 2.7 V			0.02			0.02	mA
	$\overline{P}3$					0.04			0.04	
	$\overline{P}2$					0.06			0.06	
	$\overline{P}0$, $\overline{P}1$, $\overline{G}3$					0.08			0.08	
	$\overline{G}0$, $\overline{G}2$					0.14			0.14	
	$\overline{G}1$					0.16			0.16	
I_{IL}	C_n	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	$\overline{P}3$					−1			−1	
	$\overline{P}2$					−1.5			−1.5	
	P0, $\overline{P}1$, $\overline{G}3$					−2			−2	
	$\overline{G}0$, $\overline{G}2$					−3.5			−3.5	
	$\overline{G}1$					−4			−4	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}		V_{CC} = 5.5 V			17			17		mA
I_{CCL}					23			23		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit current, I_{OS}.

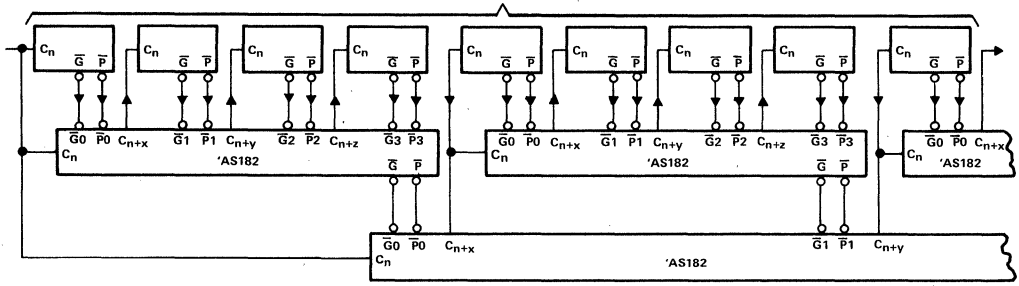
switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			SN54AS182			SN74AS182			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	C_n	C_{n+x}, C_{n+y}		5			5		ns
t_{PHL}		C_{n+z}		5			5		
t_{PLH}	Any $\overline{P}$ or $\overline{G}$	C_{n+x}, C_{n+y}		5			5		ns
t_{PHL}		C_{n+z}		5			5		
t_{PLH}	Any $\overline{P}$ or $\overline{G}$	$\overline{G}$		6			6		ns
t_{PHL}				5			5		
t_{PLH}	Any $\overline{P}$	$\overline{P}$		5			5		ns
t_{PHL}				5			5		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TYPICAL APPLICATION DATA

'AS181B, 'AS881A



NOTE: Remaining inputs and outputs of 'AS181B or 'AS881A are not shown.

FIGURE 1. THE 'AS182 IN A 64-BIT LOOK-AHEAD CARRY CIRCUIT

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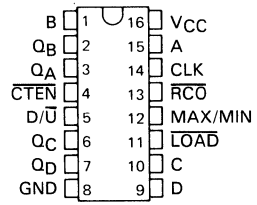
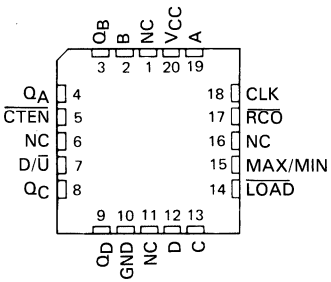
D2661, DECEMBER 1982—REVISED MAY 1986

- **Single Down/Up Count Control Line**
- **Look-Ahead Circuitry Enhances Speed of Cascaded Counters**
- **Fully Synchronous in Count Modes**
- **Asynchronously Presettable with Load Control**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS190, SN54ALS191 . . . J PACKAGE
SN74ALS190, SN74ALS191 . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS190, SN54ALS191 . . . FK PACKAGE
(TOP VIEW)



NC — no internal connection.

descriptions

The 'ALS190 and 'ALS191 are synchronous, reversible up/down counters. The 'ALS190 is a 4-bit decade counter and the 'ALS191 is a 4-bit binary counter. Synchronous counting operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered on a low-to-high-level transition of the clock input if the enable input ($\overline{CTEN}$) is low. A high at $\overline{CTEN}$ inhibits counting. The direction of the count is determined by the level of the down/up (D/$\overline{U}$) input. When D/$\overline{U}$ is low, the counter counts up and when D/$\overline{U}$ is high, it counts down.

These counters feature a fully independent clock circuit. Changes at the control inputs ($\overline{CTEN}$ and D/$\overline{U}$) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter will be dictated solely by the condition meeting the stable setup and hold times.

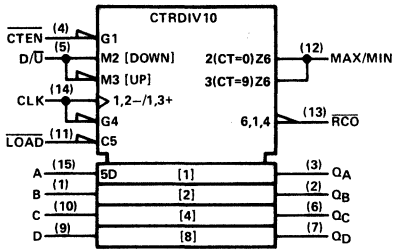
These counters are fully programmable; that is, the outputs may each be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

The CLK, D/$\overline{U}$, and LOAD inputs are buffered to lower the drive requirement, which significantly reduces the loading on, or current required by, clock drivers, etc., for long parallel words.

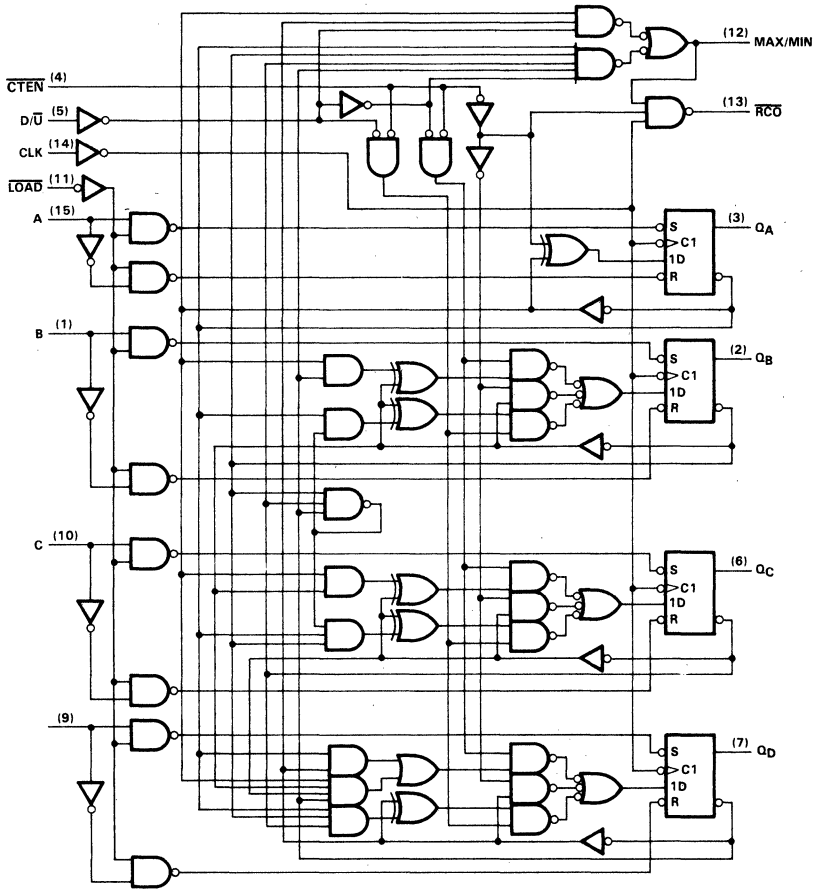
Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock while the count is zero (all outputs low) counting down or maximum (9 or 15) counting up. The ripple clock output produces a low-level output pulse under those same conditions but only while the clock input is low. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

The SN54ALS190 and SN54ALS191 are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS190 and SN74ALS191 are characterized for operation from 0 °C to 70 °C.

'ALS190 logic symbol†

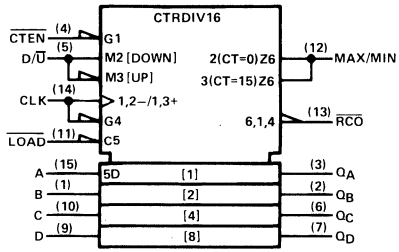


'ALS190 logic diagram (positive logic)

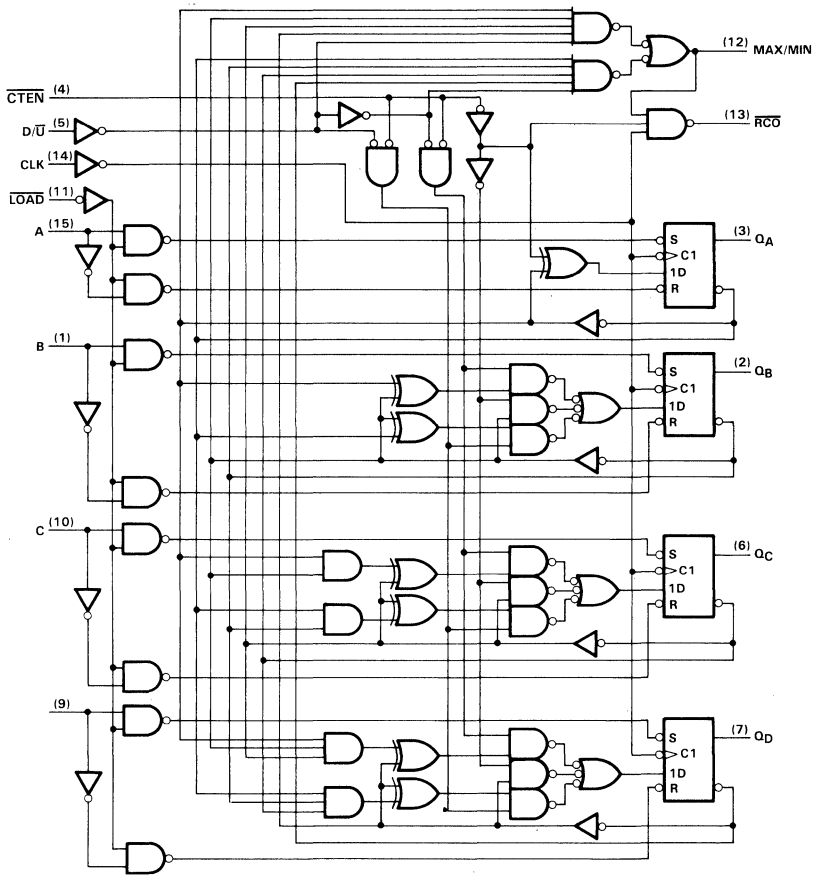


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

'ALS191 logic symbol†



'ALS191 logic diagram (positive logic)



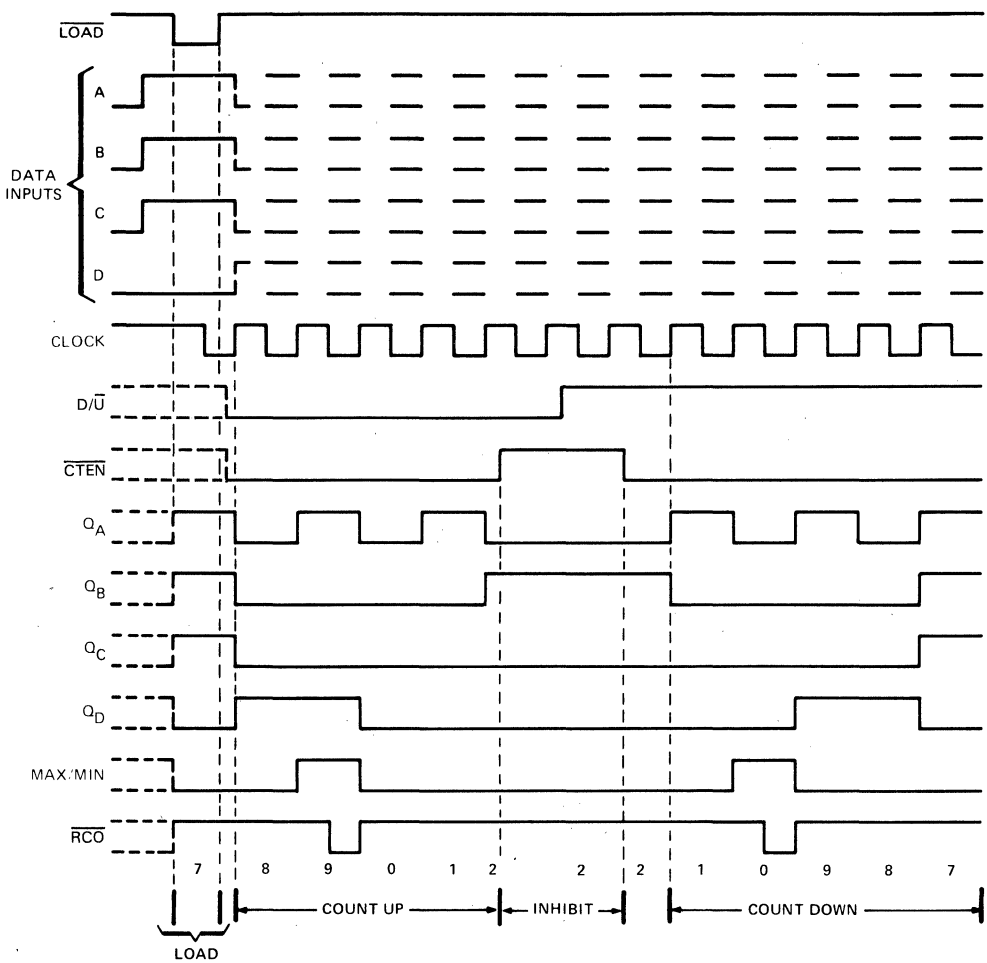
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

typical load, count, and inhibit sequences

'ALS190

Illustrated below is the following sequence:

1. Load (preset) to BCD seven.
2. Count up to eight, nine (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), nine, eight, and seven.

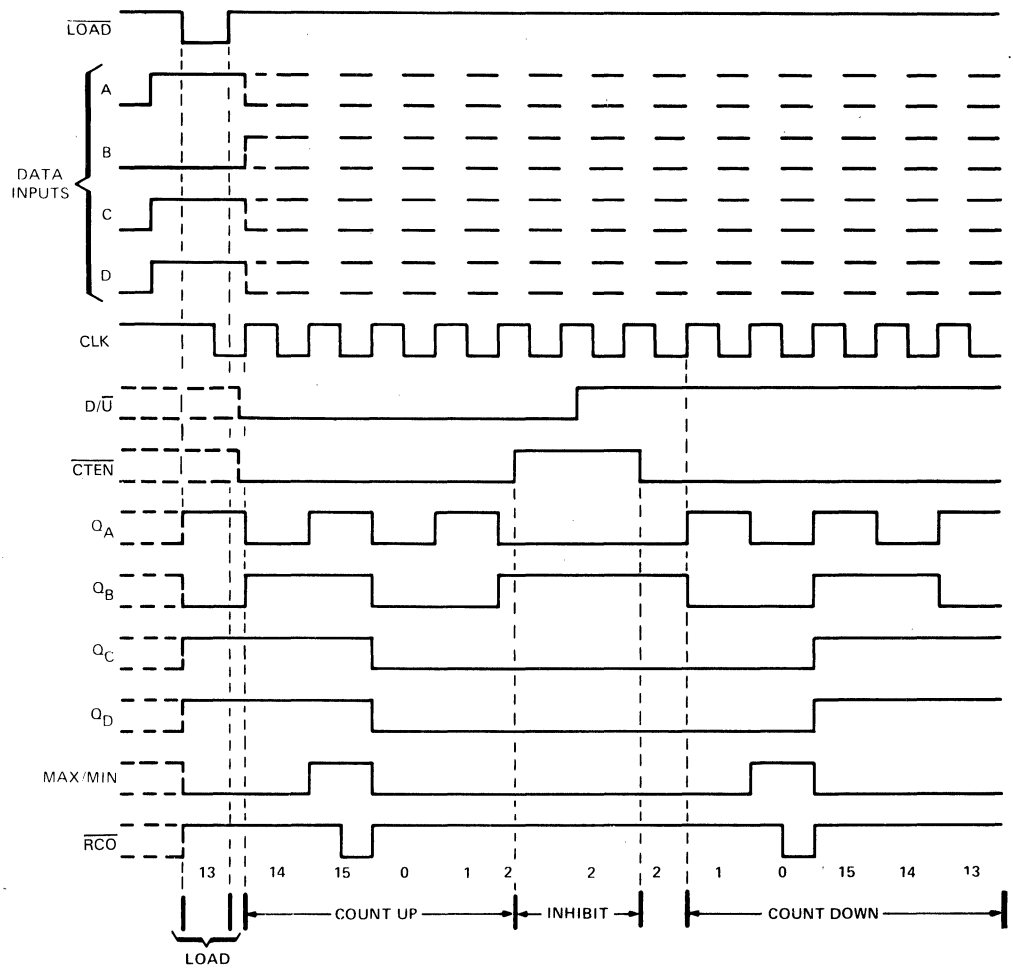


typical load, count, and inhibit sequences

'ALS191

Illustrated below is the following sequence:

1. Load (preset) to binary thirteen.
2. Count up to fourteen, fifteen (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS190, SN54ALS191 . . . . . −55 °C to 125 °C
SN74ALS190, SN74ALS191 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

				SN54ALS190 SN54ALS191			SN74ALS190 SN74ALS191			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
I_{OH}	High-level output current					−0.4			−0.4	mA
I_{OL}	Low-level output current					4			8	mA
f_{clock}	Clock frequency	'ALS190		0		20	0		25	MHz
		'ALS191		0		20	0		30	
t_w	Pulse duration	CLK high or low	'ALS190	25			20			ns
			'ALS191	20			16.5			
		$\overline{LOAD}$ low		25			20			
t_{su}	Setup time	Data before $\overline{LOAD}$↑		25			20			ns
		$\overline{CTEN}$ before CLK↑		45			20			
		D/$\overline{U}$ before CLK↑		45			20			
		$\overline{LOAD}$ inactive before CLK↑		20			20			
t_h	Hold time	Data after $\overline{LOAD}$↑		5			5			ns
		$\overline{CTEN}$ after CLK↑		0			0			
		D/$\overline{U}$ after CLK↑		0			0			
T_A	Operating free-air temperature			−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS190 SN54ALS191			SN74ALS190 SN74ALS191			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V	I_{OL} = 8 mA					0.35	0.5	
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	$\overline{CTEN}$ or CLK	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
	All others					−0.1			−0.1	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	All inputs at 0 V		12	22		12	22	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

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switching characteristics (see Note 1)

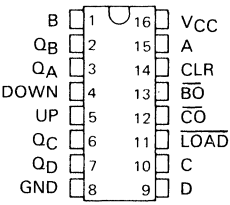
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS190 SN54ALS191		SN74ALS190 SN74ALS191		
			MIN	MAX	MIN	MAX	
f_{max}	'ALS190		20		25		MHz
	'ALS191		20		30		
t_{PLH}	$\overline{LOAD}$	Any Q	7	37	8	30	ns
t_{PHL}			8	34	8	30	
t_{PLH}	A, B, C, D	Any Q	4	25	4	21	ns
t_{PHL}			4	25	4	21	
t_{PLH}	CLK	$\overline{RCO}$	5	24	5	20	ns
t_{PHL}			5	25	5	20	
t_{PLH}	CLK	Any Q	3	26	3	18	ns
t_{PHL}			3	22	3	18	
t_{PLH}	CLK	MAX/MIN	8	37	8	31	ns
t_{PHL}			8	34	8	31	
t_{PLH}	D/$\overline{U}$	$\overline{RCO}$	12	45	15	37	ns
t_{PHL}			10	36	10	28	
t_{PLH}	D/$\overline{U}$	MAX/MIN	8	35	8	25	ns
t_{PHL}			8	30	8	25	
t_{PLH}	$\overline{CTEN}$	$\overline{RCO}$	4	21	4	18	ns
t_{PHL}			4	23	4	18	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

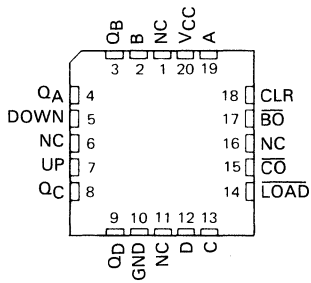
D2661, DECEMBER 1982—REVISED MAY 1986

- **Look-Ahead Circuitry Enhances Cascaded Counters**
- **Fully Synchronous in Count Modes**
- **Parallel Asynchronous Load for Modulo-N Count Lengths**
- **Asynchronous Clear**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS192, SN54AS193 . . . J PACKAGE
SN74ALS192, SN74ALS193 . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS192, SN54ALS193 . . . FK PACKAGE
(TOP VIEW)



NC — no internal connection.

description

The 'ALS192 and 'ALS193 are synchronous, reversible up/down counters. The 'ALS192 is a 4-bit decade counter and the 'ALS193 is a 4-bit binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered by a low-to-high-level transition of either count (clock) input (Up or Down). The direction of counting is determined by which count input is pulsed while the other count input is high.

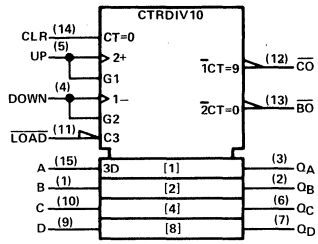
All four counters are fully programmable; that is, each output may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided that forces all outputs to the low level when a high level is applied. The clear function is independent of the count and the load inputs. The clock, count, and load inputs are buffered to lower the drive requirements. This significantly reduces the loading on clock drivers, etc., for long parallel words.

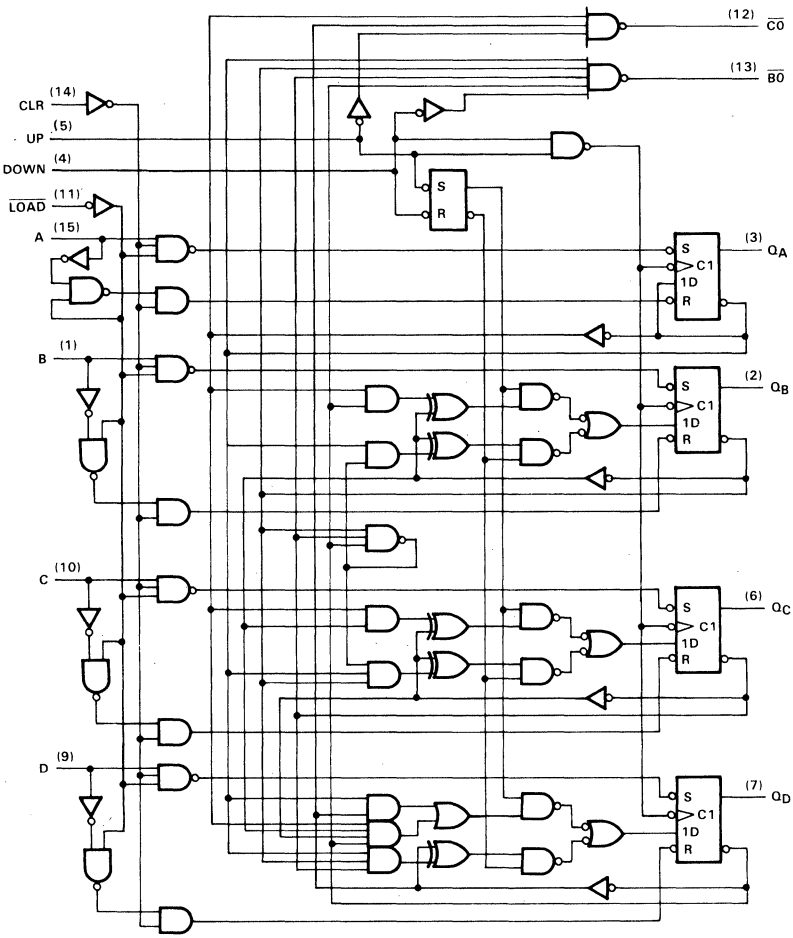
These counters were designed to be cascaded without the need for external circuitry. The borrow output (BO) produces a low-level pulse while the count is zero (all outputs low) and the count-down input is low. Similarly, the carry output ($\overline{CO}$) produces a low-level pulse while the count is maximum (9 or 15) and the count-up input is low. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs, respectively, of the succeeding counter.

The SN54ALS192 and SN54ALS193 are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS192 and SN74ALS193 are characterized for operation from 0 °C to 70 °C.

'ALS192 logic symbol†



'ALS192 logic diagram (positive logic)



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

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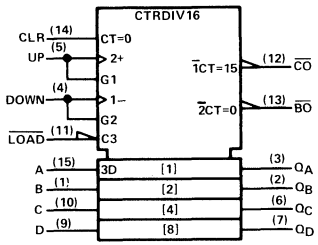
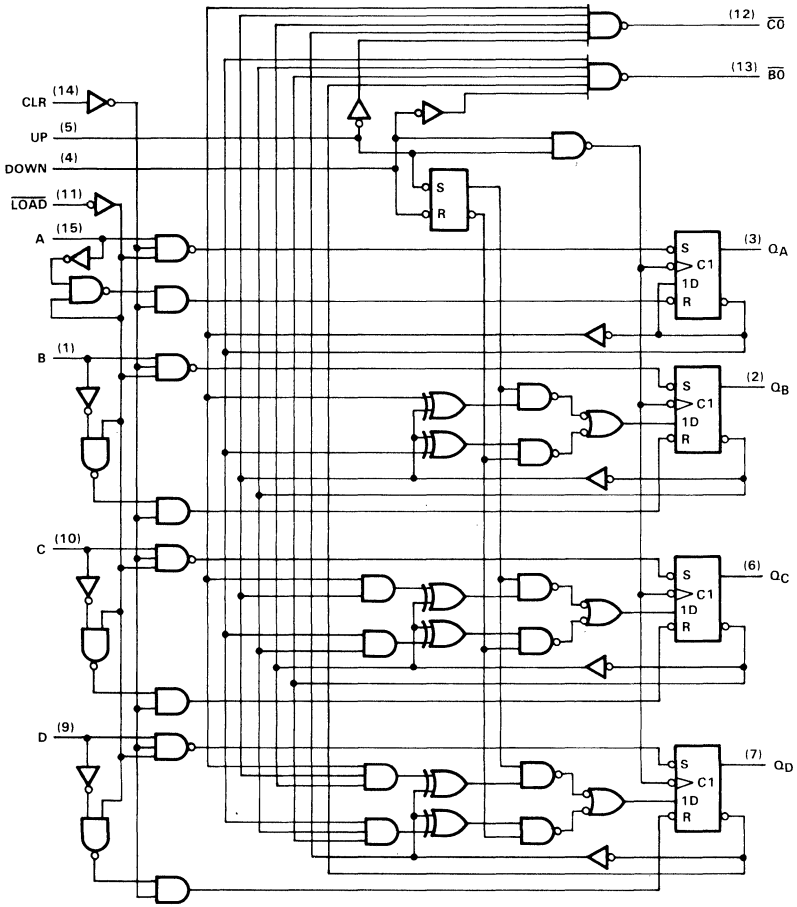
'ALS193 logic symbol†



'ALS193 logic diagrams (positive logic)



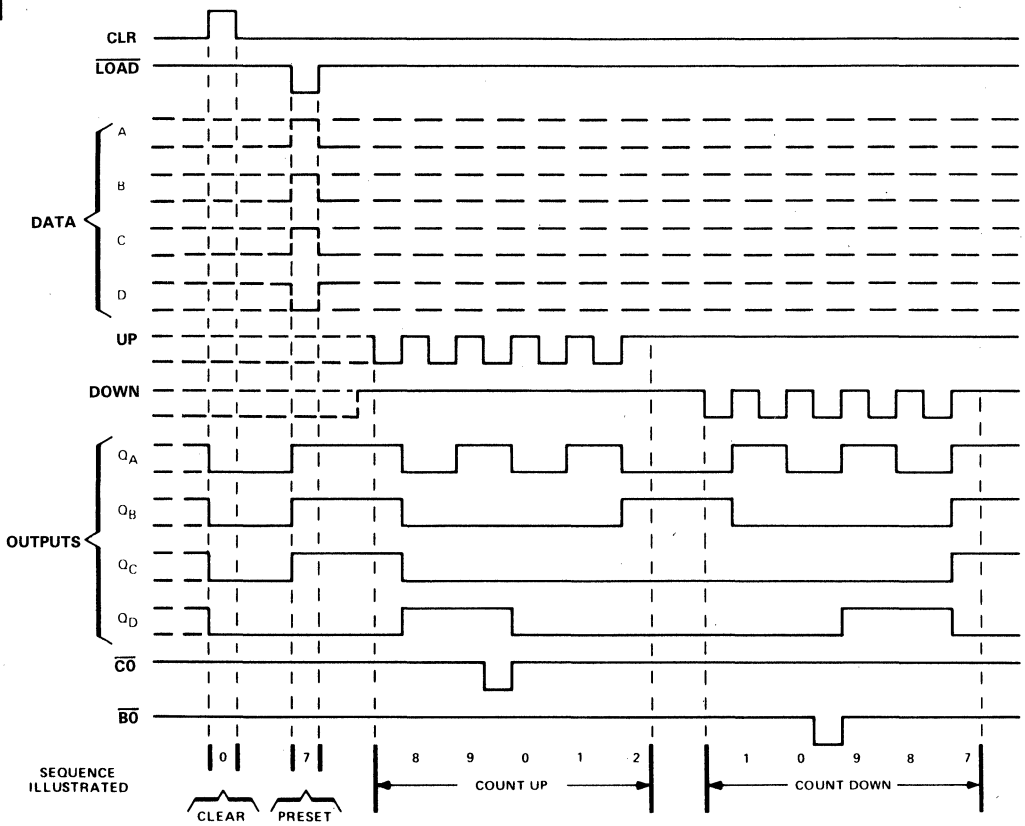
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

typical clear, load, and count sequence

'ALS192

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to BCD seven.
3. Count up to eight, nine, carry, zero, one, and two.
4. Count down to one, zero, borrow, nine, eight, and seven.



NOTES: A. Clear overrides load, data, and count inputs.
B. When counting up, count-down input must be high; when counting down, count-up input must be high.

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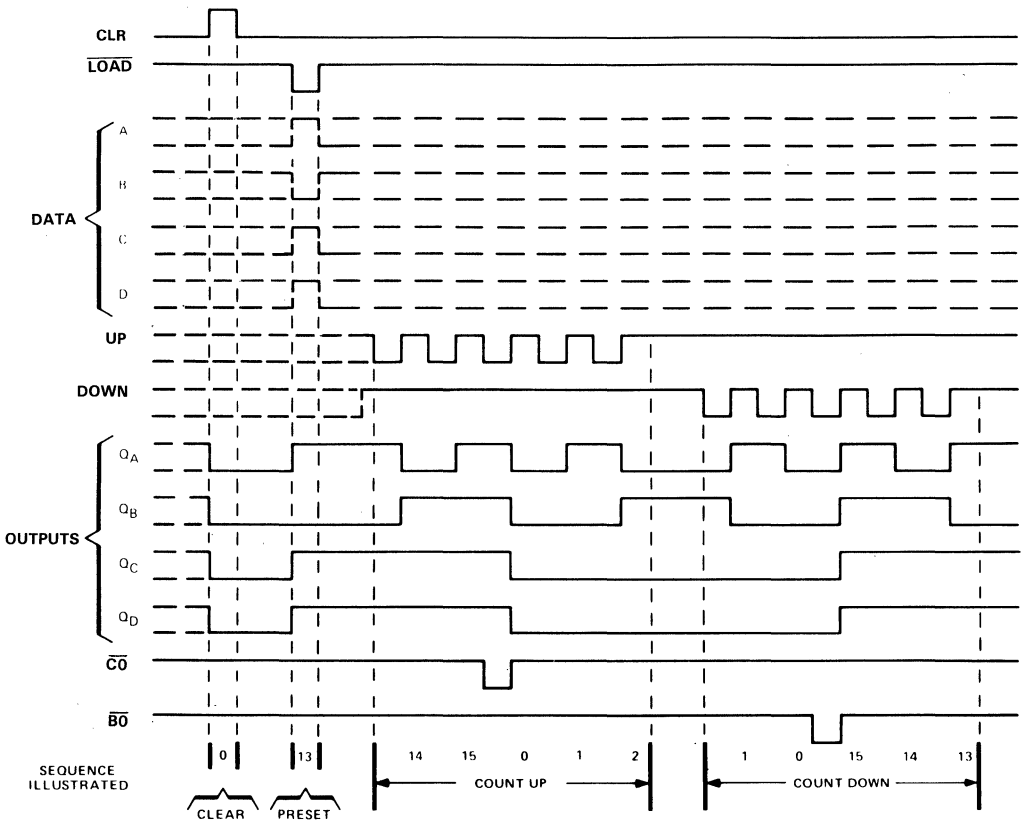
typical clear, load, and count sequences

'ALS193

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to binary thirteen.
3. Count up to fourteen, fifteen, carry, zero, one, and two.
4. Count down to one, zero, borrow, fifteen, fourteen, and thirteen.



NOTES: A. Clear overrides load, data, and count inputs.

B. When counting up, count-down input must be high; when counting down, count-up input must be high.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS192, SN54ALS193 . . . . . −55 °C to 125 °C
SN74ALS192, SN74ALS193 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

				SN54ALS192 SN54ALS193			SN74ALS192 SN74ALS193			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
I_{OH}	High-level output current					−0.4			−0.4	mA
I_{OL}	Low-level output current					4			8	mA
f_{clock}	Clock frequency	'ALS192		0		20	0		25	MHz
		'ALS193		0		20	0		30	
t_w	Pulse duration	CLR high		10			10			ns
		$\overline{LOAD}$ low		25			20			
		UP or DOWN high or low	'ALS192	25			20			ns
			'ALS193	30			16.5			
t_{su}	Setup time	Data before $\overline{LOAD}$↑		25			20			ns
		CLR inactive before UP↑ or DOWN↑		20			20			
		$\overline{LOAD}$ inactive before UP↑ or DOWN↑		20			20			
t_h	Hold time	Data after $\overline{LOAD}$↑		5			5			ns
		UP high after DOWN↑		0			0			
		DOWN high after UP↑		0			0			
T_A	Operating free-air temperature			−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS192 SN54ALS193			SN74ALS192 SN74ALS193			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V	I_{OL} = 8 mA					0.35	0.5	
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	UP, DOWN	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
	All others					−0.1			−0.1	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		12	22		12	22	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with the clear and load inputs grounded, and all other inputs at 4.5 V.

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switching characteristics (see Note 2)

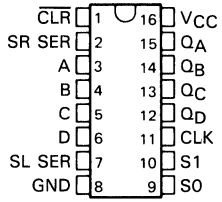
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS192 SN54ALS193		SN74ALS192 SN74ALS193		
			MIN	MAX	MIN	MAX	
f_{max}	'ALS192		20		25		MHz
	'ALS193		25		30		
t_{PLH}	Up	CO	3	20	4	16	ns
t_{PHL}			3	21	5	18	
t_{PLH}	Down	BO	4	20	4	16	ns
t_{PHL}			5	22	5	18	
t_{PLH}	Up or Down	Any Q	4	27	4	19	ns
t_{PHL}			4	23	4	17	
t_{PLH}	$\overline{\text{LOAD}}$	Any Q	8	38	8	30	ns
t_{PHL}			8	37	8	28	
t_{PHL}	CLR	Any Q	5	20	5	17	ns

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

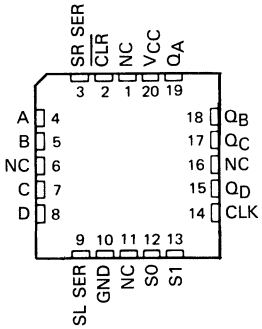
D2661, DECEMBER 1983—REVISED MAY 1986

- **Parallel-to-Serial, Serial-to-Parallel Conversions**
- **Left or Right Shifts**
- **Parallel Synchronous Loading**
- **Direct Overriding Clear**
- **Temporary Data Latching Capability**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54AS194 . . . J PACKAGE
SN74AS194 . . . D OR N PACKAGE
(TOP VIEW)



SN54AS194 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

These bidirectional shift registers feature parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

Inhibit clock (temporary data latch/do nothing)
Shift-right (in the direction Q_A toward Q_D)
Shift-left (in the direction Q_D toward Q_A)
Parallel (broadside) load

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S0 and S1, high. The data are loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift-right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial inputs. Clocking of the flip-flop is inhibited when both mode control inputs are low.

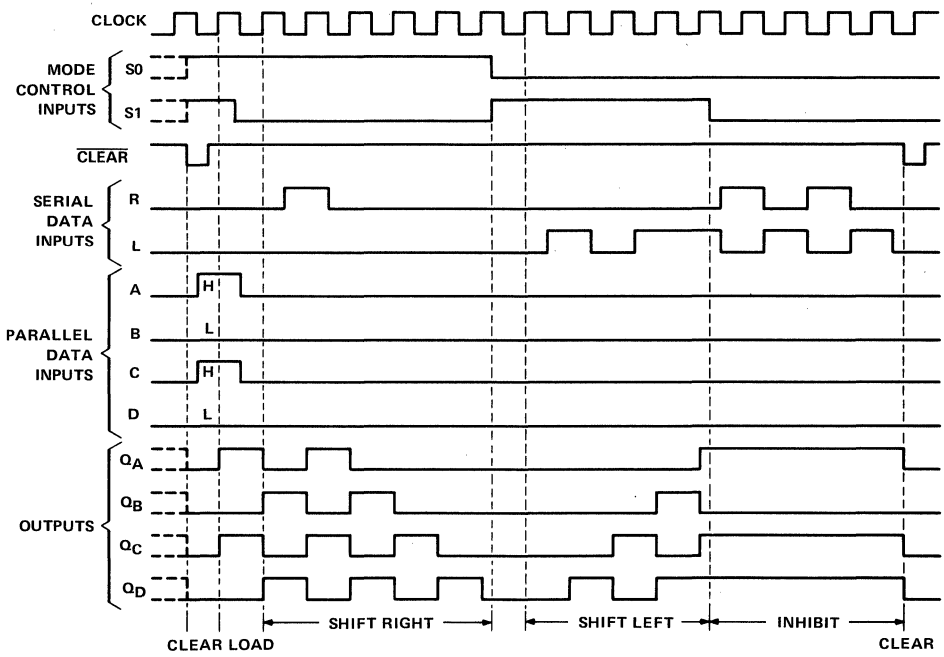
The SN54AS194 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS194 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS										OUTPUTS			
$\overline{\text{CLEAR}}$	MODE		CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D
	S1	S0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

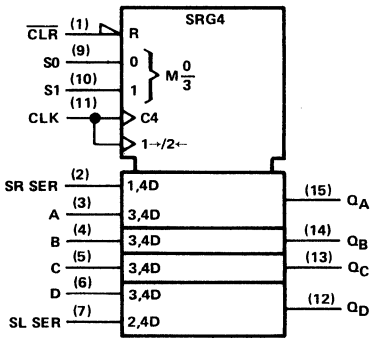
H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, respectively, before the most-recent ↑ transition of the clock.

typical clear, load, right-shift, inhibit, and clear sequences

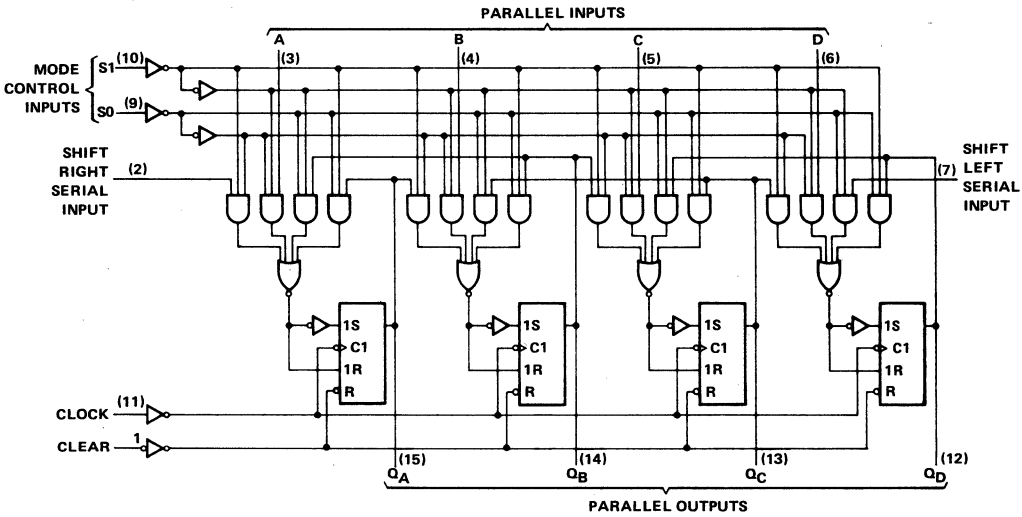


TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

logic symbol†



logic diagram (positive logic)



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS194 . . . . . −55°C to 125°C
SN74AS194 . . . . . 0°C to 150°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54AS194			SN74AS194			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−2	mA
I_{OL}	Low-level output current				20			20	mA
f_{clock}	Clock frequency		0		75	0		80	MHz
t_w	Pulse duration	$\overline{CLR}$	4			4			ns
		CLK high	4			2			
		CLK low	6			6			
t_{su}	Set-up time before CLK↑	Select	9			8			ns
		Data	3.5			3			
t_{wr}	Recovery time	$\overline{CLR}$	6			6			ns
t_h	Hold time, data after CLK↑		0.5			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS194			SN74AS194			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	Data, CLK, $\overline{CLR}$	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	Mode, SL, SR					0.2			0.2	
I_{IH}	Data, CLK, $\overline{CLR}$	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	Mode, SL,SR					40			40	
I_{IL}	Data, CLK, $\overline{CLR}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	Mode, SL, SR					−1			−1	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	Outputs high		30	49		30	43	mA
			Outputs low		38	60		38	53	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

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switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS194		SN74AS194		
			MIN	MAX	MIN	MAX	
f_{max}			75		80		MHz
t_{PLH}	CLK	Any Q	2.5	8	3	7	ns
t_{PHL}			2.5	8	3	7	
t_{PHL}	$\overline{CLR}$	Any Q	3.5	13	4	12	ns

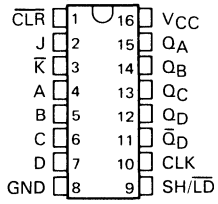
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54AS195, SN74AS195
4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

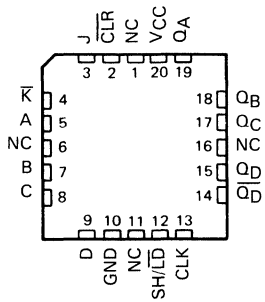
D2661, DECEMBER 1983—REVISED MAY 1986

- **Parallel-to-Serial, Serial-to-Parallel Conversions**
- **Parallel Synchronous Loading**
- **J and $\overline{K}$ Inputs to First Stage**
- **Right-Shift Only with Complementary Outputs on Last Stage**
- **Direct Overriding Clear**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54AS195 . . . J PACKAGE
SN74AS195 . . . D OR N PACKAGE
(TOP VIEW)



SN54AS195 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

These 4-bit registers feature parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, shift/load control input, and a direct overriding clear. The registers have two modes of operation:

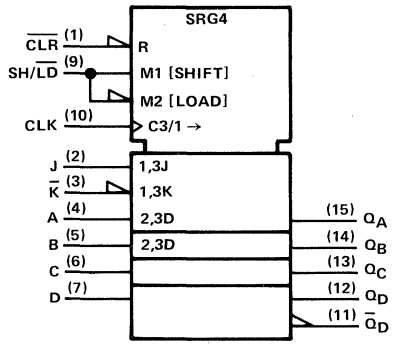
Parallel (broadside) load
Shift (in the direction Q_A toward Q_D)

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data are loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading serial data flow is inhibited.

Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-$\overline{K}$ inputs. These inputs permit the first stage to perform as a J-$\overline{K}$, D-, or T-type flip-flop as shown in the function table.

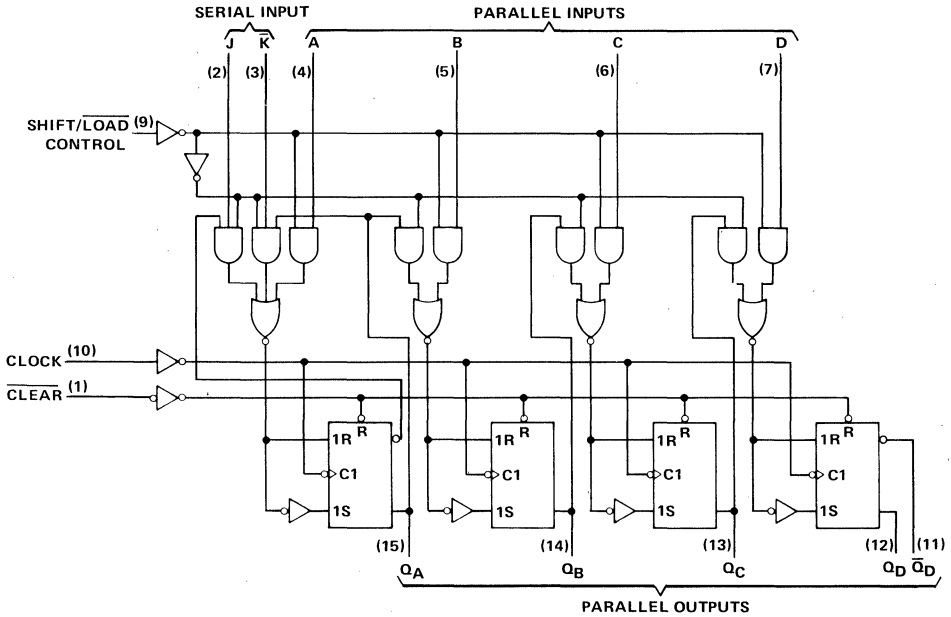
The SN54AS195 is characterized for operation over the full military range of −55°C to 125°C. The SN74AS195 is characterized for operation from 0°C to 70°C.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



TEXAS INSTRUMENTS
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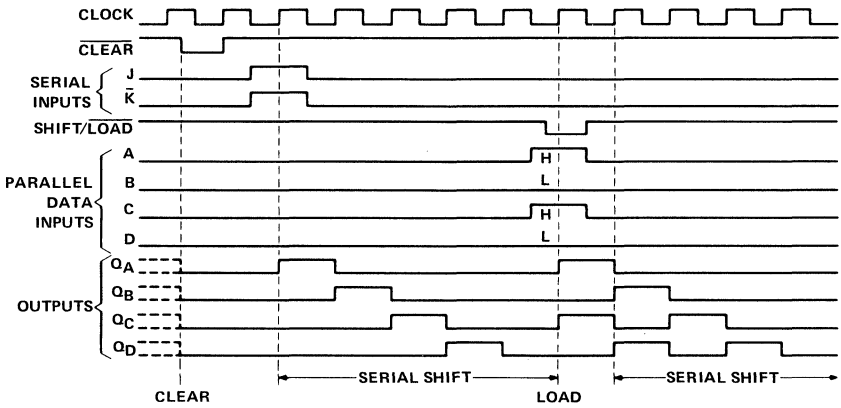
FUNCTION TABLE

INPUTS									OUTPUTS				
$\overline{CLEAR}$	SHIFT/$\overline{LOAD}$	CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
			J	$\overline{K}$	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

typical clear, shift, and load sequences



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS195 . . . . . −55°C to 125°C
SN74AS195 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54AS195			SN74AS195			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−2	mA
I_{OL}	Low-level output current				20			20	mA
f_{clock}	Clock frequency		0		60	0		70	MHz
t_w	Pulse duration	CLK high	4			4			ns
		$\overline{CLR}$ low	4			4			
t_{su}	Setup time	Data before CLK↑	4			3.5			ns
		SH/$\overline{LD}$ before CLK↑	9			8			
		$\overline{CLR}$ high before CLK↑	6.5			6			
t_h	Hold time	Data after CLK↑	1			0.5			ns
		SH/$\overline{LD}$ after CLK↑	0			0			
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS195			SN74AS195			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	SH/$\overline{LD}$	V_{CC} = 5.5 V,	V_I = 7 V			0.2			0.2	mA
	All others					0.1			0.1	
I_{IH}	SH/$\overline{LD}$	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	μA
	All others					20			20	
I_{IL}	SH/$\overline{LD}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−1			−1	mA
	All others					−0.5			−0.5	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}		V_{CC} = 5.5 V			32	51		32	51	mA
I_{CCL}		V_{CC} = 5.5 V			36	57		36	57	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

TEXAS INSTRUMENTS
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switching characteristics (see Note 1)

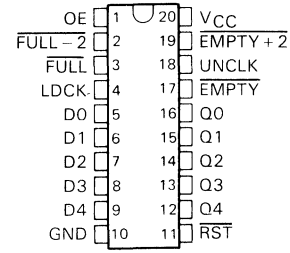
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS195		SN74AS195		
			MIN	MAX	MIN	MAX	
f_{max}			60		70		MHz
t_{PLH}	CLK	Any Q	3	10	3	8.5	ns
t_{PHL}			2.5	11.5	2.5	10.5	
t_{PLH}	$\overline{CLR}$	$\overline{Q}_D$	4	9.5	4	8	ns
t_{PHL}		Q_A thru Q_D	5	13	5	11.5	

NOTE 1: Load circuits and voltage waveforms are shown in Section 1.

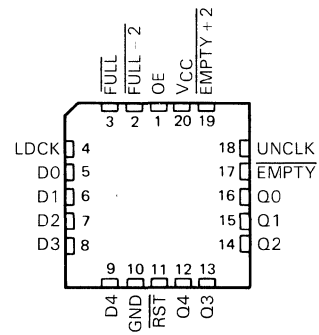
D2876, MARCH 1986–REVISED MAY 1986

- **Independent Asychronous Inputs and Outputs**
- **16 Words by 5 Bits Each**
- **Data Rates from 0 to 30 MHz**
- **Fall-Through Time . . . 24 ns Typ**
- **3-State Outputs**

SN54ALS229A . . . J PACKAGE
SN74ALS229A . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS229A . . . FK PACKAGE
SN74ALS229A . . . FN PACKAGE
(TOP VIEW)



description

These 80-bit memories utilize Advanced Low-Power Schottky technology and feature high speed and fast fall-through times. They are organized as 16 words by 5 bits each.

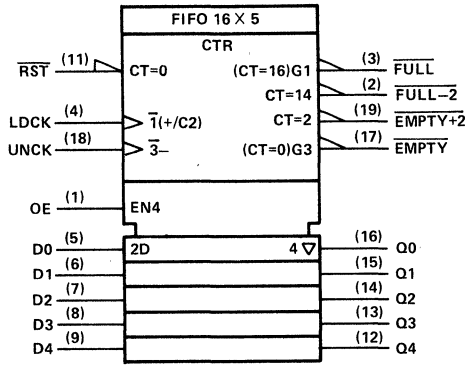
A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. These FIFOs are designed to process data at rates from 0 to 30 megahertz in a bit-parallel format, word by word.

Data is written into memory on a low-to-high transition at the load clock input (LDCK) and is read out on a low-to-high transition at the unload clock input (UNCK). The memory is full when the number of words clocked in exceeds by 16 the number of words clocked out. When the memory is full, LDCK signals will have no effect. When the memory is empty, UNCK signals have no effect.

Status of the FIFO memory is monitored by the $\overline{\text{FULL}}$, $\overline{\text{EMPTY}}$, $\overline{\text{FULL}-2}$, and $\overline{\text{EMPTY}+2}$ output flags. The $\overline{\text{FULL}}$ output will be low whenever the memory is full, and high whenever not full. The $\overline{\text{FULL}-2}$ output will be low whenever the memory contains 14 data words. The $\overline{\text{EMPTY}}$ output will be low whenever the memory is empty, and high whenever it is not empty. The $\overline{\text{EMPTY}+2}$ output will be low whenever 2 words remain in memory.

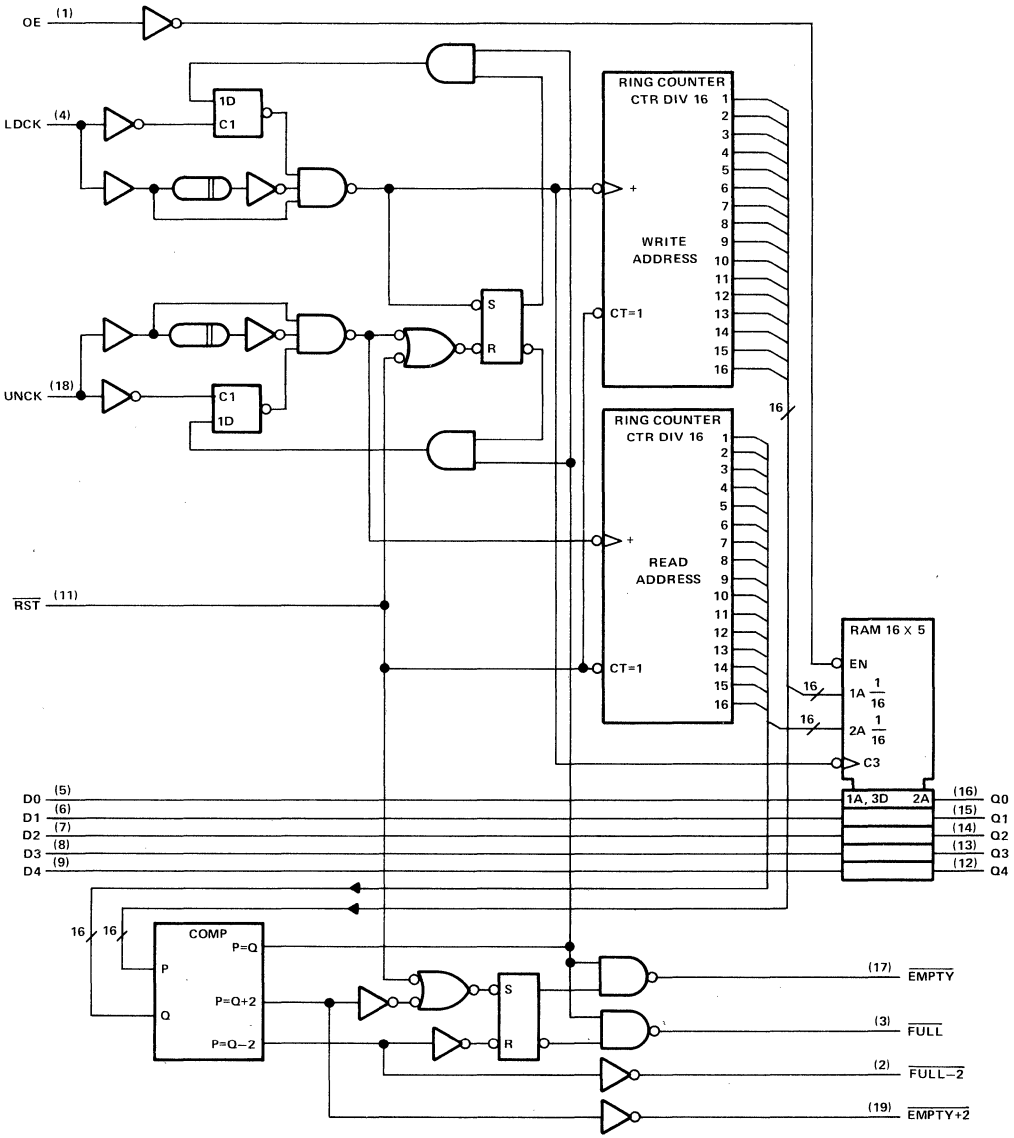
A low level on the reset input ($\overline{\text{RST}}$) resets the internal stack control pointers and also sets $\overline{\text{EMPTY}}$ low and sets $\overline{\text{FULL}}$, $\overline{\text{FULL}-2}$, and $\overline{\text{EMPTY}+2}$ high. The Q outputs are not reset to any specific logic level. The first low-to-high transition on LDCK, after either a $\overline{\text{RST}}$ pulse or from an empty condition, will cause $\overline{\text{EMPTY}}$ to go high and the data to appear on the Q outputs. It is important to note that the first word does not have to be unloaded. Data outputs are noninverting with respect to the data inputs and are at high impedance when the output enable input (OE) is low. OE does not affect the output flags. Cascading is easily accomplished in the word-width direction, but is not possible in the word-depth direction.

logic symbol†

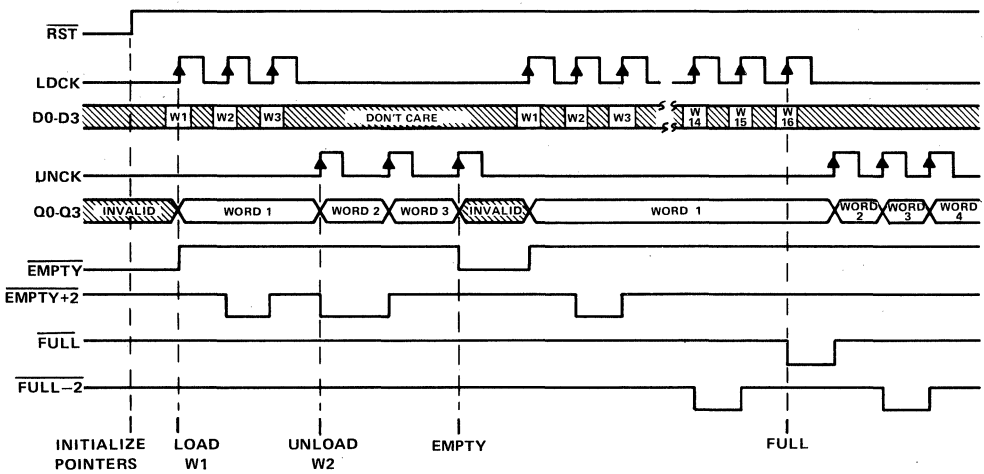


† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12. The symbol is functionally accurate but does not show the details of implementation; for these, see the logic diagram. The symbol represents the memory as if it were controlled by a single counter whose content is the number of words stored at the time. Output data is invalid when the counter content (CT) is 0.

logic diagram (positive logic)



timing diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS229A . . . . . −55°C to 125°C
SN74ALS229A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS229A			SN74ALS229A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current	Q outputs			−1.0			−1.6	mA
		Status flags			−0.4			−0.4	
I_{OL}	Low-level output current	Q outputs			12			24	mA
		Status flags			4			8	
f_{clock}	Clock frequency	LDCK	0		25	0		30	MHz
		UNCK	0		25	0		30	
t_w	Pulse duration	$\overline{RST}$ low	20			15			ns
		LDCK low	15			10			
		LDCK high	25			20			
		UNCK low	15			10			
		UNCK high	25			20			
t_{su}	Setup time	Data before LDCK↑	10			10			ns
		$\overline{RST}$ (inactive) before LDCK↑	5			5			
t_h	Hold time	Data after LDCK↑	5			5			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS229A			SN74ALS229A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	Status flags	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
	Q outputs	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	Q outputs	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
	Status flags	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V			95	150		95	140	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS229A			SN54ALS229A		SN74ALS229A		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	LDCK					25		30		MHz
	UNCK					25		30		
t_{pd}	LDCK↑	Any Q		24	47	7	54	7	50	ns
t_{pd}	UNCK↑	Any Q		19	29	9	35	9	33	ns
t_{PLH}	LDCK↑	$\overline{EMPTY}$		18	26	9	32	9	30	ns
t_{PHL}	UNCK↑	$\overline{EMPTY}$		18	25	9	32	9	29	ns
t_{PHL}	$\overline{RST}$↓	$\overline{EMPTY}$		15	21	6	26	6	24	ns
t_{pd}	LDCK↑	$\overline{EMPTY+2}$		23	33	10	40	10	38	ns
t_{pd}	UNCK↑	$\overline{EMPTY+2}$		20	29	9	38	9	35	ns
t_{PLH}	$\overline{RST}$↓	$\overline{EMPTY+2}$		20	28	9	35	9	33	ns
t_{pd}	LDCK↑	$\overline{FULL-2}$		23	33	10	40	10	38	ns
t_{pd}	UNCK↑	$\overline{FULL-2}$		20	29	9	38	9	35	ns
t_{PLH}	$\overline{RST}$↓	$\overline{FULL-2}$		20	28	9	35	9	33	ns
t_{PHL}	LDCK↑	$\overline{FULL}$		21	28	10	35	10	33	ns
t_{PLH}	UNCK↑	$\overline{FULL}$		17	23	8	29	8	27	ns
t_{PLH}	$\overline{RST}$↓	$\overline{FULL}$		18	27	8	33	8	31	ns
t_{en}	OE↑	Q		8	13	1	16	2	15	ns
t_{dis}	OE↓	Q		8	14	2	20	2	17	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

D2661, DECEMBER 1982—REVISED MAY 1986

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- 'ALS230 and 'AS230 have True and Complementary Outputs
- 'ALS231 and 'AS231 have Complementary G and $\overline{G}$ Inputs
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- High Capacitive Drive Capability
- Current Sinking Capability Up to 64 mA
- Dependable Texas Instruments Quality and Reliability

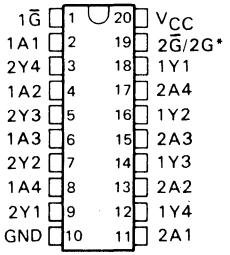
description

These octal buffers and line drivers are designed specifically to improve the performance of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs.

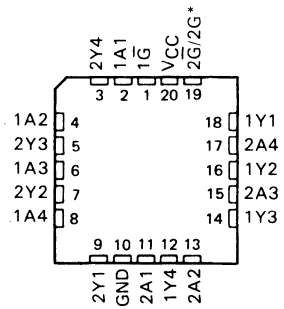
The -1 versions of the SN74ALS' parts are identical to their standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes. There are no -1 versions of the SN54ALS' parts.

The SN54' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

SN54ALS', SN54AS' . . . J PACKAGE
SN74ALS', SN74AS' . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS', SN54AS' . . . FK PACKAGE
(TOP VIEW)

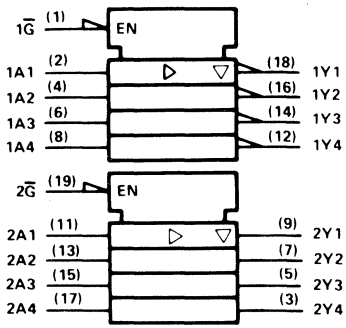


*$2\overline{G}$ for 'AS230 or 2G for 'ALS231, 'AS231

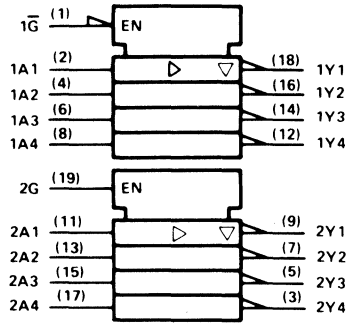
2 ALS and AS Circuits

logic symbols†

'ALS230, 'AS230

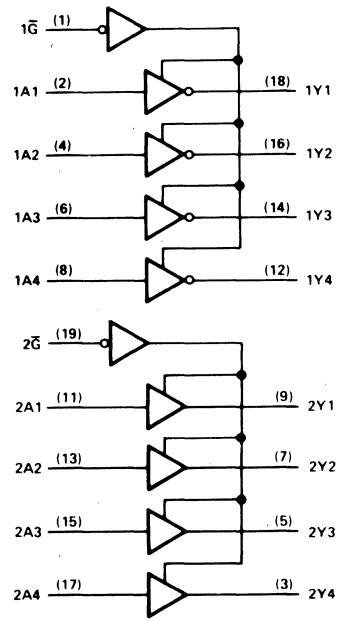


'ALS231, 'AS231

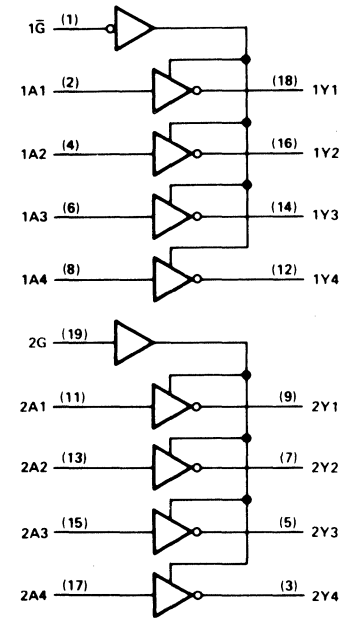


logic diagrams (positive logic)

'ALS230, 'AS230



'ALS231, 'AS231



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS230 . . . . . −55°C to 125°C
SN74ALS230 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS230			SN74ALS230			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
							48†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The 48 mA limit applies only to the −1 versions and only if V_{CC} is maintained between 4.75 V and 5.25 V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS230			SN74ALS230			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
		V_{CC} = 4.75 V,	I_{OL} = 48 mA (−1 versions)					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS230	V_{CC} = 5.5 V,	Outputs high		7			7		mA
			Outputs low		15			15		
			Outputs disabled		12			12		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS230 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS230			SN54ALS230		SN74ALS230		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y		5						ns
t_{PHL}				5						
t_{PZH}	$\overline{G}$	Y		9						ns
t_{PZL}				10						
t_{PHZ}	$\overline{G}$	Y		5						ns
t_{PLZ}				6						

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS231 . . . . . −55°C to 125°C
SN74ALS231 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS231			SN74ALS231			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
							48†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The 48 mA limit applies only to the −1 versions and only if V_{CC} is maintained between 4.75 V and 5.25 V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS231			SN74ALS231			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
		V_{CC} = 4.75 V,	I_{OL} = 48 mA (−1 versions)					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS231	V_{CC} = 5.5 V,	Outputs high		7	11		7	11	mA
			Outputs low		15	22		15	22	
			Outputs disabled		12	19		12	19	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS231 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS231	SN54ALS231		SN74ALS231		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	5	2	12	2	9	ns
t_{PHL}			5	2	11	2	9	
t_{PZH}	$1\overline{G}$	Y	9	4	17	4	14	ns
t_{PZL}			10	5	21	5	18	
t_{PHZ}	$1\overline{G}$	Y	5	2	12	2	10	ns
t_{PLZ}			6	3	18	3	12	
t_{PZH}	2G	Y	11	5	18	5	16	ns
t_{PZL}			12	5	22	5	19	
t_{PHZ}	2G	Y	6	2	12	2	10	ns
t_{PLZ}			7	3	19	3	13	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54AS230, SN54AS231 . . . . . −55°C to 125°C
SN74AS230, SN74AS231 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS230 SN54AS231			SN74AS230 SN74AS231			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS230 SN54AS231			SN74AS230 SN74AS231			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.4		2.4	3.4		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.27	0.55				V
		V_{CC} = 4.5 V	I_{OL} = 64 mA					0.31	0.55	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	'AS230 2A	V_{CC} = 5.5 V,	V_I = 0.4 V			−1			−1	mA
	All others					−0.5			−0.5	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−50		−150	−50		−150	mA
I_{CC}	'AS230	V_{CC} = 5.5 V	Outputs high		16	25		16	25	mA
			Outputs low		55	87		55	87	
			Outputs disabled		29	46		29	46	
	'AS231	V_{CC} = 5.5 V	Outputs high		12	18		12	18	mA
			Outputs low		52	82		52	82	
			Outputs disabled		25	39		25	39	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'AS230 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS230		SN74AS230		
			MIN	MAX	MIN	MAX	
t_{PLH}	1A	1Y	2.5	7	2.5	6.5	ns
t_{PHL}			2	6	2	5.7	
t_{PLH}	2A	2Y	2.5	9	2.5	6.2	ns
t_{PHL}			2	7	2	6.2	
t_{PZH}	$1\overline{G}$	1Y	2	7	2	6.4	ns
t_{PZL}			2	9	2	8.5	
t_{PHZ}			2	5.5	2	5	
t_{PLZ}			2	12.5	2	9.5	
t_{PZH}	$2\overline{G}$	2Y	2	10	2	9	ns
t_{PZL}			2	8	2	7.5	
t_{PHZ}			2	6.5	2	6	
t_{PLZ}			2	10.5	2	9	

'AS231 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS231		SN74AS231		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	2	7	2	6.5	ns
t_{PHL}			2	6	2	5.7	
t_{PZH}	$\overline{G}$	Y	2	7	2	6.4	ns
t_{PZL}			2	9	2	8.5	
t_{PHZ}			2	5.5	2	5	
t_{PLZ}			2	12.5	2	9.5	
t_{PZH}	G	Y	3	7	3	6	ns
t_{PZL}			3	10	3	9	
t_{PHZ}			3	6.5	3	6	
t_{PLZ}			3	13.5	3	7	

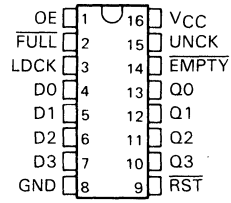
NOTE 1. Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

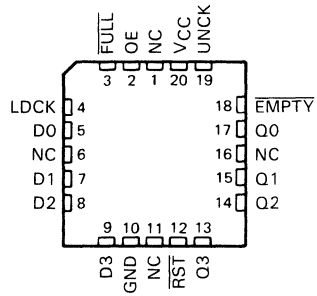
D2876, OCTOBER 1985 – REVISED MAY 1986

- **Independent Asynchronous Inputs and Outputs**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **16 Words by 4 Bits Each**
- **Data Rates from 0 to 30 MHz**
- **Fall-Through Time . . . 24 ns Typ**
- **3-State Outputs**

SN54ALS232A . . . J PACKAGE
SN74ALS232A . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS232A . . . FK PACKAGE
SN74ALS232A . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection.

description

These 64-bit memories use Advanced Low-Power Schottky technology and feature high speed and fast fall-through times. They are organized as 16 words by 4 bits each.

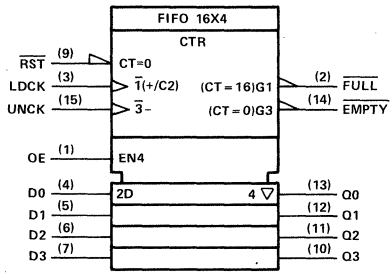
A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. These FIFOs are designed to process data at rates from 0 to 30 megahertz in a bit-parallel format, word by word.

Data is written into memory on a low-to-high transition at the load clock input (LDCK) and is read out on a low-to-high transition at the unload clock input (UNCK). The memory is full when the number of words clocked in exceeds by 16 the number of words clocked out. When the memory is full, LDCK signals have no effect on the data residing in memory. When the memory is empty, UNCK signals have no effect.

Status of the FIFO memory is monitored by the $\overline{\text{FULL}}$ and $\overline{\text{EMPTY}}$ output flags. The $\overline{\text{FULL}}$ output will be low when the memory is full, and high when the memory is not full. The $\overline{\text{EMPTY}}$ output will be low when the memory is empty, and high when it is not empty.

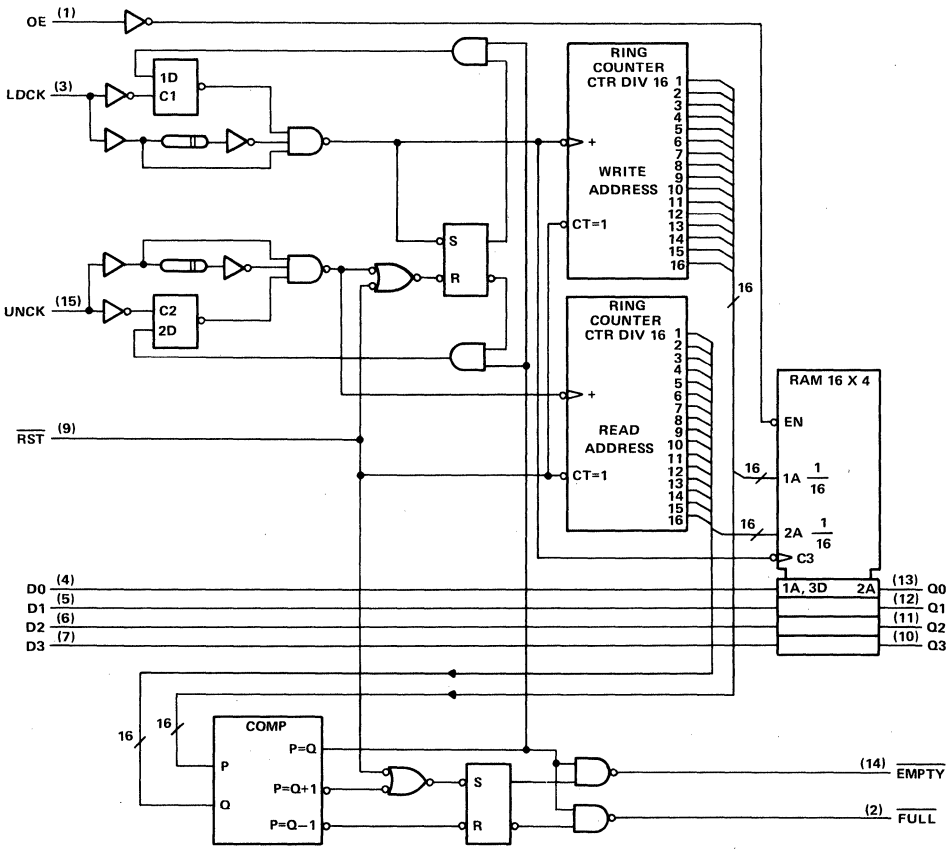
A low level on the reset input ($\overline{\text{RST}}$) resets the internal stack control pointers and also sets $\overline{\text{EMPTY}}$ low and sets $\overline{\text{FULL}}$ high. The outputs are not reset to any specific logic levels. The first low-to-high transition on LDCK, either after a $\overline{\text{RST}}$ pulse or from an empty condition, will cause $\overline{\text{EMPTY}}$ to go high and the data to appear on the Q outputs. It is important to note that the first word does not have to be unloaded. Data outputs are noninverting with respect to the data inputs and are at high impedance when the output-enable input (OE) is low. OE does not affect either the $\overline{\text{FULL}}$ or $\overline{\text{EMPTY}}$ output flags. Cascading is easily accomplished in the word-width direction, but is not possible in the word-depth direction.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12. The symbol is functionally accurate but does not show the details of implementation; for these, see the logic diagram. The symbol represents the memory as if it were controlled by a single counter whose content is the number of words stored at the time. Output data is invalid when the counter content (CT) is 0.

logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

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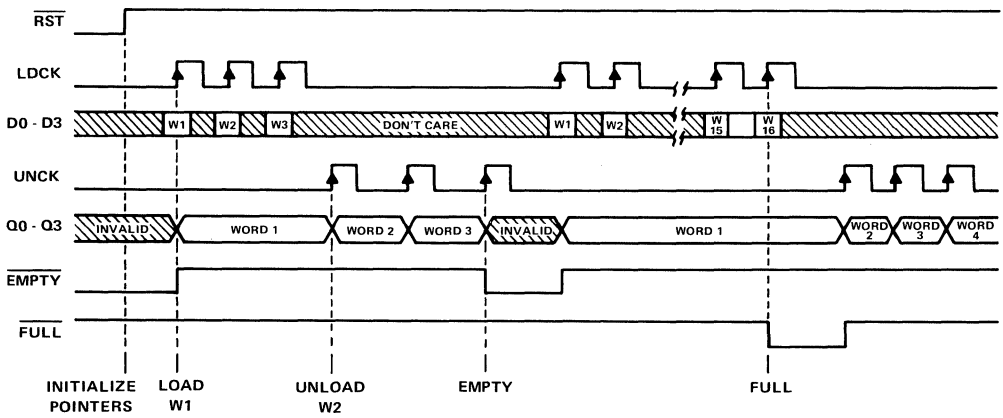
timing diagram



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS232A . . . . . −55°C to 125°C
SN74ALS232A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS232A			SN74ALS232A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current	Q outputs			−1			−1.6	mA
		$\overline{FULL}$, $\overline{EMPTY}$			−0.4			−0.4	
I_{OL}	Low-level output current	Q outputs			12			24	mA
		$\overline{FULL}$, $\overline{EMPTY}$			4			8	
f_{clock}	Clock frequency	LDCK	0		25	0		30	MHz
		UNCK	0		25	0		30	
t_w	Pulse duration	$\overline{RST}$ low	20			15			ns
		LDCK low	15			10			
		LDCK high	25			20			
		UNCK low	15			10			
		UNCK high	25			20			
t_{su}	Setup time	Data before LDCK↑	10			10			ns
		$\overline{RST}$ (inactive) before LDCK↑	5			5			
t_h	Hold time	Data after LDCK↑	5			5			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS232A			SN74ALS232A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	$\overline{FULL}$, $\overline{EMPTY}$	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	Q outputs	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	Q outputs	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
	$\overline{FULL}$, $\overline{EMPTY}$	V_{CC} = 4.5 V,	I_{OH} = 4 mA		0.25	0.4		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V			75	125		75	125	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

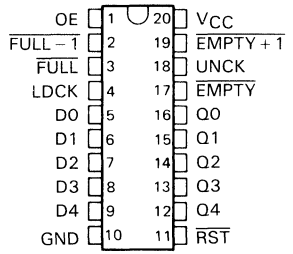
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS232A			SN54ALS232A		SN74ALS232A		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	LDCK			40		25		30		MHz
	UNCK			40		25		30		
t_{pd}	LDCK↑	Any Q		30	40	4	50	4	46	ns
t_{pd}	UNCK↑	Any Q		20	27	7	35	7	31	ns
t_{PLH}	LDCK↑	$\overline{EMPTY}$		17	23	8	29	8	26	ns
t_{PHL}	UNCK↑	$\overline{EMPTY}$		19	24	10	36	10	29	ns
t_{PHL}	$\overline{RST}$↓	$\overline{EMPTY}$		13	18	5	23	5	20	ns
t_{PHL}	LDCK↑	$\overline{FULL}$		21	26	10	35	10	31	ns
t_{PLH}	UNCK↑	$\overline{FULL}$		17	23	8	28	8	25	ns
t_{PLH}	$\overline{RST}$↓	$\overline{FULL}$		18	24	8	31	8	28	ns
t_{en}	OE↑	Q		7	12	1	16	1	14	ns
t_{dis}	OE↓	Q		10	16	2	23	2	21	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

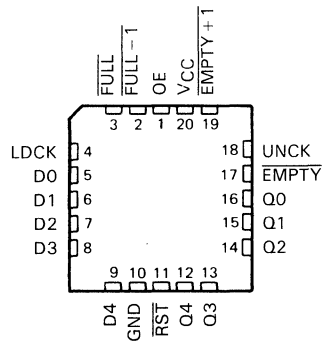
D2876, JANUARY 1986 – REVISED MAY 1986

- **Independent Asynchronous Inputs and Outputs**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **16 Words by 5 Bits Each**
- **Data Rates from 0 to 30 MHz**
- **Fall-Through Time . . . 24 ns Typ**
- **3-State Outputs**

SN54ALS233A . . . J PACKAGE
SN74ALS233A . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS233A . . . FK PACKAGE
SN74ALS233A . . . FN PACKAGE
(TOP VIEW)



description

These 80-bit memories utilize Advanced Low-Power Schottky technology and feature high speed and fast fall-through times. They are organized as 16 words by 5 bits each.

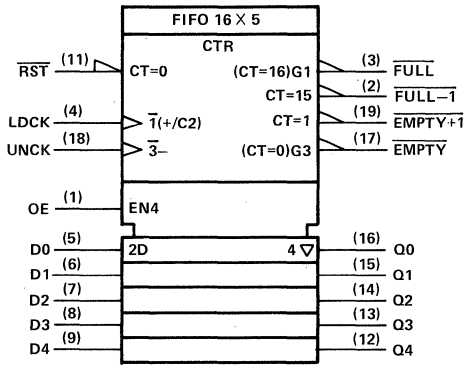
A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. These FIFOs are designed to process data at rates from 0 to 30 megahertz in a bit-parallel format, word by word.

Data is written into memory on a low-to-high transition at the load clock input (LDCK) and is read out on a low-to-high transition at the unload clock input (UNCK). The memory is full when the number of words clocked in exceeds by 16 the number of words clocked out. When the memory is full, LDCK signals will have no effect. When the memory is empty, UNCK signals have no effect.

Status of the FIFO memory is monitored by the $\overline{\text{FULL}}$, $\overline{\text{EMPTY}}$, $\overline{\text{FULL}-1}$, and $\overline{\text{EMPTY}+1}$ output flags. The FULL output will be low whenever the memory is full, and high whenever not full. The $\overline{\text{FULL}-1}$ output will be low whenever the memory contains 15 data words. The $\overline{\text{EMPTY}}$ output will be low whenever the memory is empty, and high whenever it is not empty. The $\overline{\text{EMPTY}+1}$ output will be low whenever one word remains in memory.

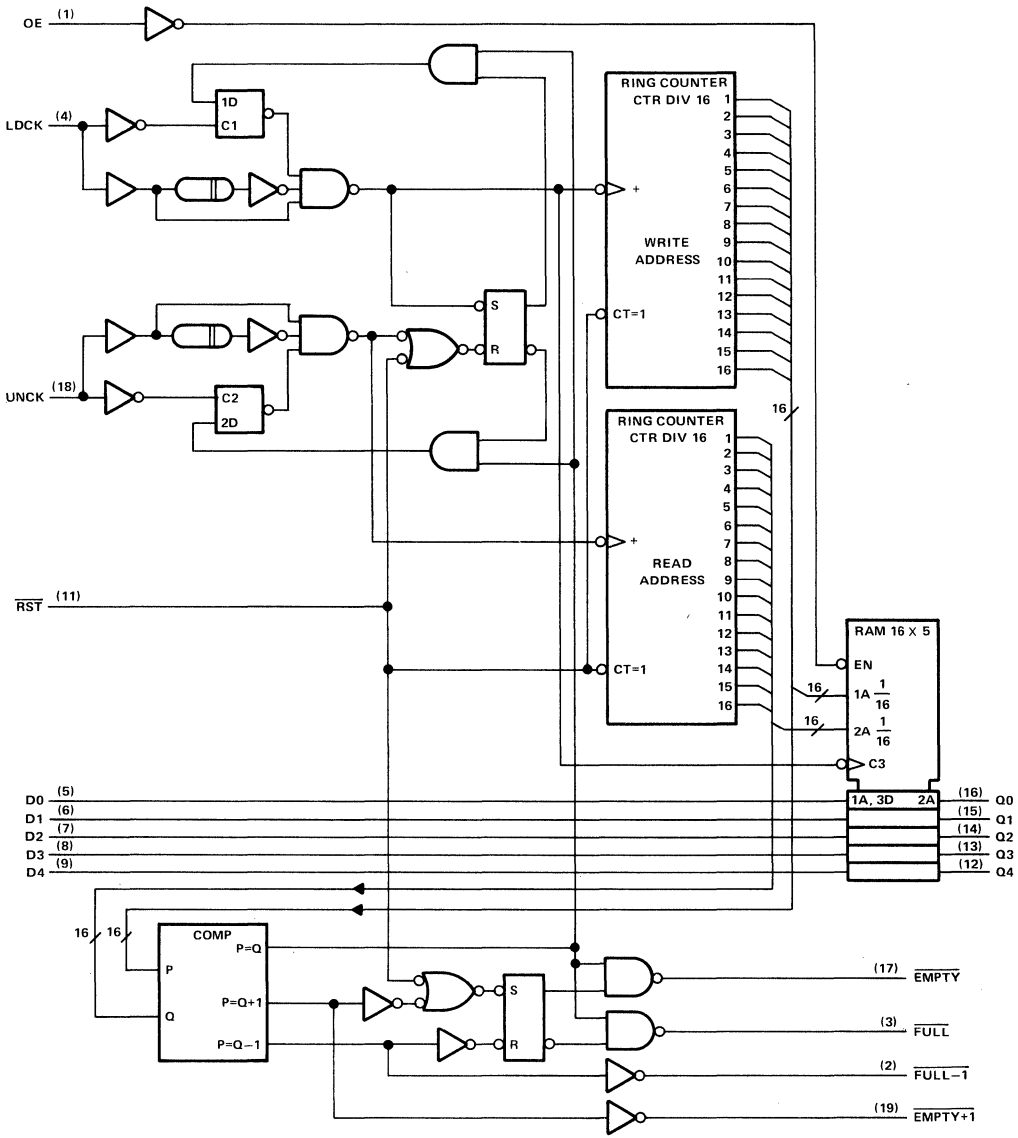
A low level on the reset input ($\overline{\text{RST}}$) resets the internal stack control pointers and also sets $\overline{\text{EMPTY}}$ low and sets $\overline{\text{FULL}}$, $\overline{\text{FULL}-1}$, and $\overline{\text{EMPTY}+1}$ high. The Q outputs are not reset to any specific logic level. The first low-to-high transition on LDCK, after either a $\overline{\text{RST}}$ pulse or from an empty condition, will cause $\overline{\text{EMPTY}}$ to go high and the data to appear on the Q outputs. It is important to note that the first word does not have to be unloaded. Data outputs are noninverting with respect to the data inputs and are at high impedance when the output enable input (OE) is low. OE does not affect the output flags. Cascading is easily accomplished in the word-width direction, but is not possible in the word-depth direction.

logic symbol†



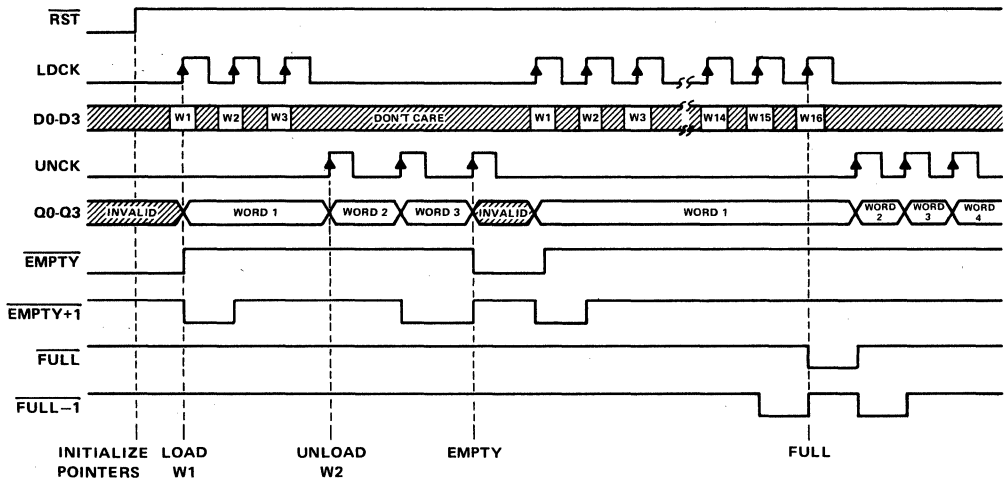
† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12. The symbol is functionally accurate but does not show the details of implementation; for these, see the logic diagram. The symbol represents the memory as if it were controlled by a single counter whose content is the number of words stored at the time. Output data is invalid when the counter content (CT) is 0.

logic diagram (positive logic)



Pin numbers are for D, J, and N packages.

timing diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS233A . . . . . −55°C to 125°C
SN74ALS233A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS233A			SN74ALS233A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current	Q outputs			−1			−1.6	mA
		Status flags			−0.4			−0.4	
I_{OL}	Low-level output current	Q outputs			12			24	mA
		Status flags			4			8	
f_{clock}	Clock frequency	LDCK	0		25	0		30	MHz
		UNCK	0		25	0		30	
t_w	Pulse duration	$\overline{RST}$ low	20			15			ns
		LDCK low	15			10			
		LDCK high	25			20			
		UNCK low	15			10			
		UNCK high	25			20			
t_{su}	Setup time	Data before LDCK↑	10			10			ns
		$\overline{RST}$ inactive before LDCK↑	5			5			
t_h	Hold time	Data after LDCK↑	5			5			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS233A			SN74ALS233A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	Status flags	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	Q outputs	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	Q outputs	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
	Status flags	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V			88	143		88	133	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = −MIN to MAX				UNIT
			'ALS233A			SN54ALS233A		SN74ALS233A		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	LDCK			40		25		30		MHz
	UNCK			40		25		30		
t_{pd}	LDCK↑	Any Q		24	44	7	52	7	48	ns
t_{pd}	UNCK↑	Any Q		19	29	9	35	9	33	ns
t_{PLH}	LDCK↑	$\overline{EMPTY}$		18	25	9	30	9	28	ns
t_{PHL}	UNCK↑	$\overline{EMPTY}$		18	25	9	33	10	30	ns
t_{PHL}	$\overline{RST}$↓	$\overline{EMPTY}$		13	19	6	24	6	22	ns
t_{pd}	LDCK↑	$\overline{EMPTY+1}$		22	31	10	40	10	37	ns
t_{pd}	UNCK↑	$\overline{EMPTY+1}$		22	31	9	40	10	37	ns
t_{PLH}	$\overline{RST}$↓	$\overline{EMPTY+1}$		19	27	8	32	8	31	ns
t_{pd}	LDCK↑	$\overline{FULL-1}$		23	32	11	38	12	36	ns
t_{pd}	UNCK↑	$\overline{FULL-1}$		23	32	11	39	12	36	ns
t_{PLH}	$\overline{RST}$↓	$\overline{FULL-1}$		20	28	10	34	11	32	ns
t_{PHL}	LDCK↑	$\overline{FULL}$		21	28	10	35	12	33	ns
t_{PLH}	UNCK↑	$\overline{FULL}$		17	24	8	29	9	27	ns
t_{PLH}	$\overline{RST}$↓	$\overline{FULL}$		18	27	8	32	9	30	ns
t_{en}	OE↑	Q		8	13	1	16	2	15	ns
t_{dis}	OE↓	Q		8	12	2	20	2	17	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
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OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

D2661, DECEMBER 1982—REVISED MAY 1986

- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **P-N-P Inputs Reduce DC Loading**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

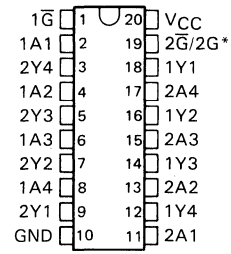
description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs. These devices feature high fan-out and improved fan-in.

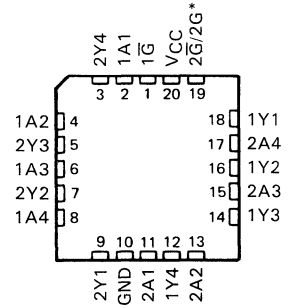
The -1 versions of the SN74ALS' parts are identical to their standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes. There are no -1 versions of the SN54ALS' parts.

The SN54' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

SN54ALS', SN54AS' . . . J PACKAGE
SN74ALS', SN74AS' . . . DW or N PACKAGE
(TOP VIEW)



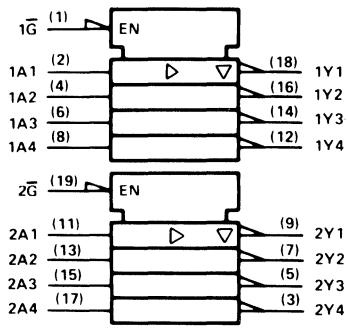
SN54ALS', SN54AS' . . . FK PACKAGE
(TOP VIEW)



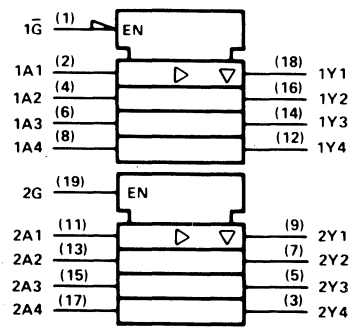
*$2\overline{G}$ for 'ALS240A, 'AS240 or 2G for 'ALS241A, 'AS241

logic symbols†

'ALS240A, 'AS240



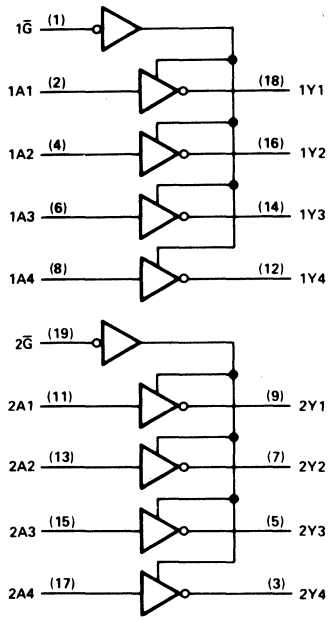
'ALS241A, 'AS241



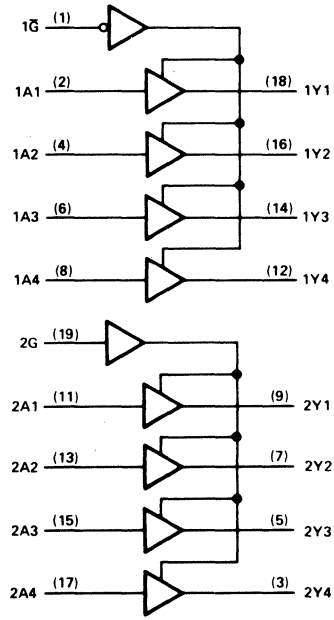
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers are for DW, J, and N packages.

logic diagrams (positive logic)

'ALS240A, 'AS240



'ALS241A, 'AS241



Pin numbers are for DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS240A, SN54ALS241A . . . . . −55°C to 125°C
SN74ALS240A, SN74ALS241A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS240A SN54ALS241A			SN74ALS240A SN74ALS241A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
							48†	
T_A	Operating free-air temperature	−55		125	0		70	°C

† The 48 mA limit applies only to the -1 versions and only if the V_{CC} is maintained between 4.75 V and 5.25 V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS240A SN54ALS241A			SN74ALS240A SN74ALS241A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
		V_{CC} = 4.75 V,	I_{OL} = 48 mA (-1 versions)							
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS240A	V_{CC} = 5.5 V	Outputs high		4	11		4	11	mA
			Outputs low		13	23		13	23	
			Outputs disabled		14	25		14	25	
	'ALS241A		Outputs high		9	17		9	15	
			Outputs low		15	28		15	26	
			Outputs disabled		17	32		17	30	

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS240A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS240A	SN54ALS240A		SN74ALS240A		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	6	2	22	2	9	ns
t_{PHL}			5	2	11	2	9	
t_{PZH}	$\overline{G}$	Y	9	4	34	5	13	ns
t_{PZL}			10	5	26	5	18	
t_{PHZ}	$\overline{G}$	Y	6	1	15	2	10	ns
t_{PLZ}			7	3	24	3	12	

'ALS241A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS241A		SN74ALS241A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	3	31	3	11	ns
t_{PHL}			1	14	3	10	
t_{PZH}	$1\overline{G}$	Y	5	33	7	21	ns
t_{PZL}			7	27	7	21	
t_{PHZ}	$1\overline{G}$	Y	2	13	2	10	ns
t_{PLZ}			2	32	3	15	
t_{PZH}	2G	Y	7	38	7	21	ns
t_{PZL}			7	30	7	21	
t_{PHZ}	2G	Y	2	17	2	10	ns
t_{PLZ}			3	35	3	15	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54AS240, SN54AS241 . . . . . −55°C to 125°C
SN74AS240, SN74AS241 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS240 SN54AS241			SN74AS240 SN74AS241			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS240 SN54AS241			SN74AS240 SN74AS241			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V, I_I = −18 mA				−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V, I_{OH} = −2 mA		V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V to 5.5 V, I_{OH} = −3 mA		2.4	3.4		2.4	3.4		
		V_{CC} = 4.5 V, I_{OH} = −12 mA		2.4						
		V_{CC} = 4.5 V, I_{OH} = −15 mA					2.4			
V_{OL}		V_{CC} = 4.5 V, I_{OL} = 48 mA			0.27	0.55				V
		V_{CC} = 4.75 V, I_{OL} = 64 mA						0.31	0.55	
I_{OZH}		V_{CC} = 5.5 V, V_O = 2.7 V				50			50	μA
I_{OZL}		V_{CC} = 5.5 V, V_O = 0.4 V				−50			−50	μA
I_I		V_{CC} = 5.5 V, V_I = 7 V				0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V, V_I = 2.7 V				20			20	μA
I_{IL}	'AS241A inputs	V_{CC} = 5.5 V, V_I = 0.4 V				−1			−1	mA
	All others					−0.5			−0.5	
I_O‡		V_{CC} = 5.5 V, V_O = 2.25 V		−50		−150	−50		−150	mA
I_{CC}	'AS240	V_{CC} = 5.5 V	Outputs high		11	17		11	17	mA
			Outputs low		51	75		51	75	
			Outputs disabled		24	38		24	38	
	'AS241		Outputs high		22	35		22	35	
			Outputs low		61	90		61	90	
			Outputs disabled		35	56		35	56	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'AS240 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS240		SN74AS240		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	2	7	2	6.5	ns
t_{PHL}			2	6	2	5.7	
t_{PZH}	$1\overline{G}$	Y	2	7	2	6.4	ns
t_{PZL}			2	9.5	2	9	
t_{PHZ}	$\overline{G}$	Y	2	5.5	2	5	ns
t_{PLZ}			2	12.5	2	9.5	

'AS241 switching characteristics (see Note 1)

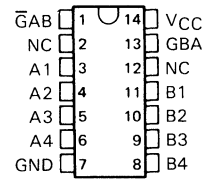
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS241		SN74AS241		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	2	9	2	6.2	ns
t_{PHL}			2	7	2	6.2	
t_{PZH}	$1\overline{G}$	Y	2	10	2	9	ns
t_{PZL}			2	8	2	7.5	
t_{PHZ}	$1\overline{G}$	Y	2	6.5	2	6	ns
t_{PLZ}			2	10.5	2	9	
t_{PZH}	2G	Y	2	11	3	10.5	ns
t_{PZL}			3	9.5	3	8.5	
t_{PHZ}	2G	Y	3	7	3	7	ns
t_{PLZ}			3	12	3	12	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

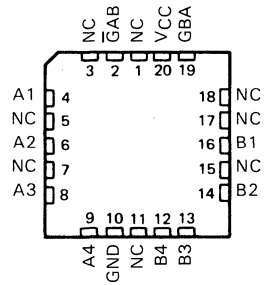
D2661, DECEMBER 1982—REVISED MAY 1986

- **2-Way Asynchronous Communication Between Data Buses**
- **P-N-P Inputs Reduce Loading**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54' . . . J PACKAGE
SN74' . . . D OR N PACKAGE
(TOP VIEW)



SN54' . . . FK PACKAGE
(TOP VIEW)



NC-No internal connection

description

These quadruple bus transceivers are designed for asynchronous two-way communications between data buses. The control function implementation allows for maximum flexibility in timing. These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs (GBA and $\overline{G}AB$). The enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives the quadruple bus transceivers the capability to store data by simultaneous enabling of GBA and $\overline{G}AB$. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (8 in all) will retain their states. The 4-bit codes appearing on the two sets of buses will be complimentary for the 'ALS242 and 'AS242 or identical for the 'ALS243 and 'AS243.

The -1 versions of the SN74ALS' parts are identical to the standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes. There are no -1 versions of the SN54ALS' parts.

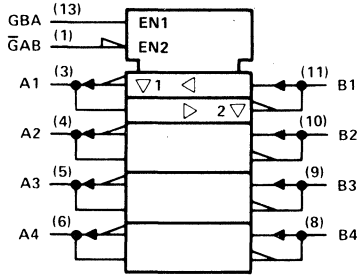
The SN54' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

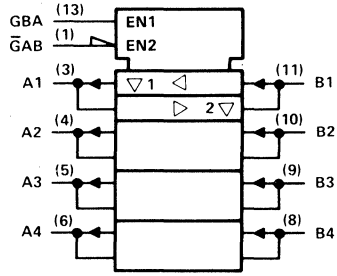
INPUTS		'ALS242B	'ALS243A
$\overline{G}AB$	GBA	'AS242	'AS243
L	L	$\overline{A}$ to B	A to B
H	H	$\overline{B}$ to A	B to A
H	L	Isolation	Isolation
L	H	Latch A and B ($A=\overline{B}$)	Latch A and B ($A=B$)

logic symbols†

'ALS242B, 'AS242



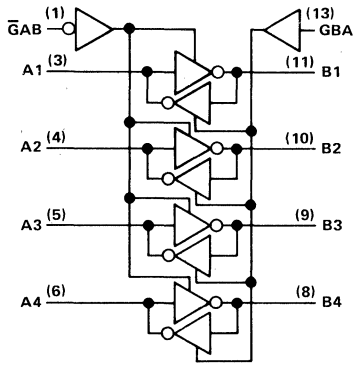
'ALS243A, 'AS243



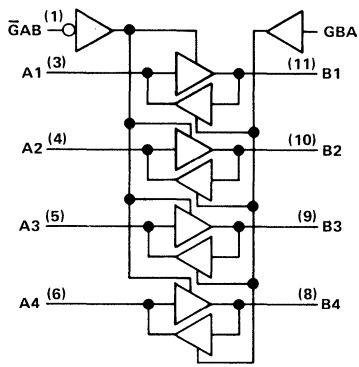
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagrams (positive logic)

'ALS242B, 'AS242



'ALS243A, 'AS243



Pin numbers are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS242B, SN54ALS243A . . . . . −55°C to 125°C
SN74ALS242B, SN74ALS243A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS242B SN54ALS243A			SN74ALS242B SN74ALS243A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
							48†	
T_A	Operating free-air temperature	−55		125	0		70	°C

† The 48-mA limit applies only to the -1 versions, and only if V_{CC} is maintained between 4.75 V and 5.25 V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS242B SN54ALS243A			SN74ALS242B SN74ALS243A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
		V_{CC} = 4.75 V,	I_{OL} = 48 mA (−1 versions)					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports‡					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	A or B ports‡					−0.1			−0.1	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS242B	V_{CC} = 5.5 V	Outputs high		10	20		10	16	mA
			Outputs low		14	26		14	21	
			Outputs disabled		12	24		12	19	
	'ALS243A		Oututs high		15	30		15	25	
			Outputs low		20	35		20	30	
			Outputs disabled		21	37		21	32	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS242B switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS242B	SN54ALS242B		SN74ALS242B		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	5	2	15	2	11	ns
t_{PHL}			5	2	14	2	10	
t_{PZH}	GAB	B	10	4	22	4	18	ns
t_{PZL}			11	7	25	7	21	
t_{PHZ}	GAB	B	6	2	16	2	14	ns
t_{PLZ}			5	2	18	2	12	
t_{PZH}	GBA	A	10	4	22	4	18	ns
t_{PZL}			11	7	25	7	21	
t_{PHZ}	GBA	A	6	2	16	2	14	ns
t_{PLZ}			5	2	18	2	12	

'ALS243A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS243A		SN74ALS243A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	4	15	4	11	ns
t_{PHL}			4	15	4	11	
t_{PZH}	$\overline{G}$AB	B	7	25	7	20	ns
t_{PZL}			7	25	7	20	
t_{PHZ}	$\overline{G}$AB	B	2	16	2	14	ns
t_{PLZ}			3	27	3	22	
t_{PZH}	GBA	A	7	25	7	20	ns
t_{PZL}			7	25	7	20	
t_{PHZ}	GBA	A	2	16	2	14	ns
t_{PLZ}			3	27	3	22	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54AS242, SN54AS243 . . . . . −55°C to 125°C
SN74AS242, SN74AS243 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS242 SN54AS243			SN74AS242 SN74AS243			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS242 SN54AS243			SN74AS242 SN74AS243			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC} − 2			V_{CC} − 2			V
		V_{CC} = 4.5 V	I_{OH} = −3 mA	2.4	3.4		2.4	3.4		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA			0.55				V
		V_{CC} = 4.5 V,	I_{OL} = 64 mA						0.55	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports‡					70			70	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	'AS242 A or B ports‡					−0.5			−0.5	
	'AS243 A or B ports‡					−1			−1	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−50		−150	−50		−150	mA
I_{CC}	'AS242	V_{CC} = 5.5 V	Outputs high		18	28		18	28	mA
			Outputs low		38	60		38	60	
			Outputs disabled		25	39		25	39	
	'AS243		Outputs high		28	44		28	44	
			Outputs low		47	74		47	74	
			Outputs disabled		35	56		35	56	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'AS242 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS242		SN74AS242		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	2	7	2	6.5	ns
t_{PHL}			2	6	2	5.7	
t_{PZH}	$\overline{G}$AB	B	2	9	2	5.5	ns
t_{PZL}			2	8.5	2	7.5	
t_{PHZ}	$\overline{G}$AB	B	2	7	2	6.5	ns
t_{PLZ}			2	12.5	2	9.5	
t_{PZH}	GBA	A	3	7	3	6	ns
t_{PZL}			3	9	3	8	
t_{PHZ}	GBA	A	3	8.5	3	6	ns
t_{PLZ}			3	13.5	3	10.5	

'AS243 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS243		SN74AS243		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	3	9	3	7.5	ns
t_{PHL}			3	8	3	6.5	
t_{PZH}	$\overline{G}$AB	B	2	10	2	9	ns
t_{PZL}			2	9	2	7.5	
t_{PHZ}	$\overline{G}$AB	B	2	7	2	6.5	ns
t_{PLZ}			2	11	2	9	
t_{PZH}	GBA	A	3	11	3	10.5	ns
t_{PZL}			3	9.5	3	8.5	
t_{PHZ}	GBA	A	3	7.5	3	7	ns
t_{PLZ}			3	14	3	11	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

D2661, DECEMBER 1982—REVISED MAY 1986

- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **P-N-P Inputs Reduce DC Loading**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

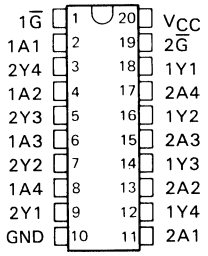
description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'ALS240A, 'ALS241A, 'AS240, and 'AS241, these devices provide the choice of selected combinations of inverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs.

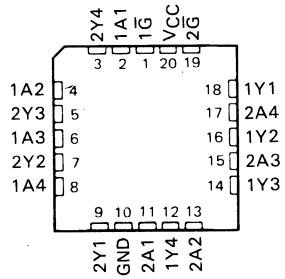
The −1 version of the SN74ALS244A is identical to the standard version except that the recommended maximum I_{OL} is increased to 48 milliamperes. There is no −1 version of the SN54ALS244A.

The SN54ALS244A and SN54AS244 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS244A and SN74AS244 are characterized for operation from 0°C to 70°C.

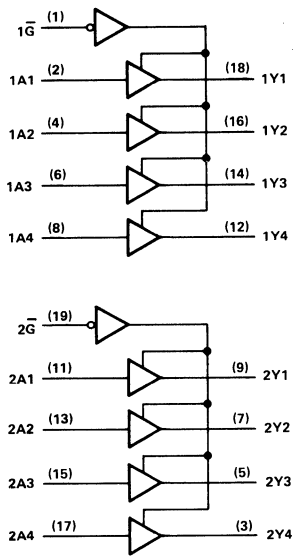
SN54ALS244A, SN54AS244 . . . J PACKAGE
SN74ALS244A, SN74AS244 . . . DW OR N PACKAGE
(TOP VIEW)



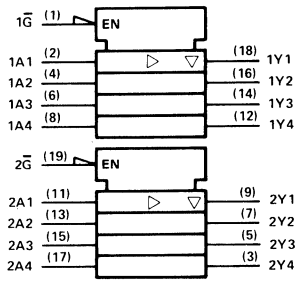
SN54ALS244A, SN54AS244 . . . FK PACKAGE
(TOP VIEW)



logic diagram (positive logic)



logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS244A . . . . . −55°C to 125°C
SN74ALS244A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS244A			SN74ALS244A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
							48†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48-mA limit applies for the SN74ALS244A-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS244A			SN74ALS244A			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V (I_{OL} = 48 mA for −1 version)	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		9	15		9	15	mA
		Outputs low		15	24		15	24	
		Outputs disabled		17	27		17	27	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS244A		SN74ALS244A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1	18	3	10	ns
t_{PHL}			3	13	3	10	
t_{PZH}	$\overline{G}$	Y	1	29	7	20	ns
t_{PZL}			1	27	7	20	
t_{PHZ}	$\overline{G}$	Y	2	12	2	10	ns
t_{PLZ}			1	21	3	13	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54AS244 . . . . . −55 °C to 125 °C
SN74AS244 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54AS244			SN74AS244			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS244			SN74AS244			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.4		2.4	3.4		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA			0.55				V
		V_{CC} = 4.5 V	I_{OL} = 64 mA						0.55	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	$\overline{G}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	A					−1			−1	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−50		−150	−50		−150	mA
I_{CC}		V_{CC} = 5.5 V	Outputs high		22	34		22	34	mA
			Outputs low		60	90		60	90	
			Outputs disabled		34	54		34	54	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

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switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS244		SN74AS244		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	2	9	2	6.2	ns
t_{PHL}			2	7	2	6.2	
t_{PZH}	$\overline{G}$	Y	2	10	2	9	ns
t_{PZL}			2	8	2	7.5	
t_{PHZ}	$\overline{G}$	Y	2	6.5	2	6	ns
t_{PLZ}			2	10.5	2	9	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2661, DECEMBER 1982—REVISED MAY 1986

- **3-State Outputs Drive Bus Lines Directly**
- **P-N-P Inputs Reduce DC Loading**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

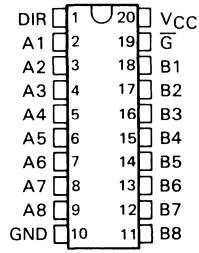
These octal bus transceivers are designed for asynchronous two-way communication between data buses The control function implementation minimizes external timing requirements.

The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated.

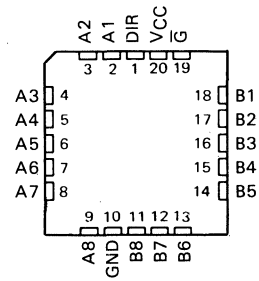
The –1 version of the SN74ALS245A is identical to the standard version except that the recommended maximum I_{OL} is increased to 48 milliamperes. There is no –1 version of the SN54ALS245A.

The SN54ALS245A and SN54AS245 are characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ALS245A and SN74AS245 are characterized for operation from 0°C to 70°C.

SN54ALS245A, SN54AS245 . . . J PACKAGE
SN74ALS245A, SN74AS245 . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS245A, SN54AS245 . . . FK PACKAGE
(TOP VIEW)

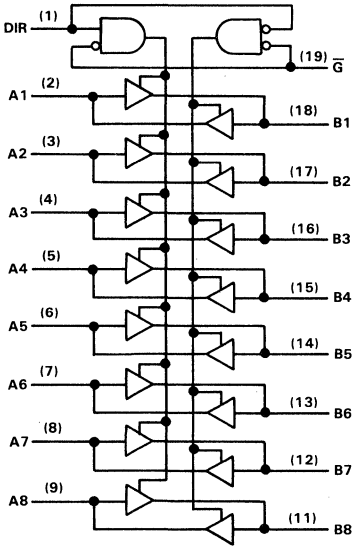


FUNCTION TABLE

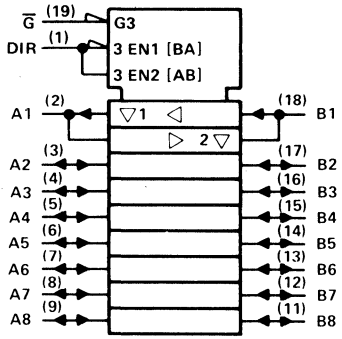
ENABLE $\overline{G}$	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

2 ALS and AS Circuits

logic diagram (positive logic)



logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS245A . . . . . −55°C to 125°C
SN74ALS245A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS245A			SN74ALS245A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
							48‡	
T_A	Operating free-air temperature	−55		125	0		70	°C

‡The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48-mA limit applies for the SN74ALS245A-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS245A			SN74ALS245A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} −2			V_{CC} −2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, (I_{OL} = 48 mA for −1 versions)	I_{OL} = 24 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports‡					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	A or B ports‡					−0.1			−0.1	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	Outputs high		30	48		30	45	mA
			Outputs low		36	60		36	55	
			Outputs disabled		38	63		38	58	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS245A		SN74ALS245A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1	19	3	10	ns
t_{PHL}			1	14	3	10	
t_{PZH}	$\overline{G}$	A or B	2	30	5	20	ns
t_{PZL}			2	29	5	20	
t_{PHZ}	$\overline{G}$	A or B	2	14	2	10	ns
t_{PLZ}			2	30	4	15	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54AS245 . . . . . −55°C to 125°C
SN74AS245 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS245			SN74AS245			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS245			SN74AS245			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.3	0.55				V
		V_{CC} = 4.5 V,	I_{OL} = 64 mA					0.35	0.55	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.4 V			50			20	μA
	A or B ports‡					70			70	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	A or B ports‡					−0.75			−0.75	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−50		−150	−50		−150	mA
I_{CC}		V_{CC} = 5.5 V	Outputs high		62	97		62	97	mA
			Outputs low		95	143		95	143	
			Outputs disabled		79	123		79	123	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡For I/O ports (Q_A through Q_H), the parameters I_{IH} and I_{IL} include the off-state output current.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

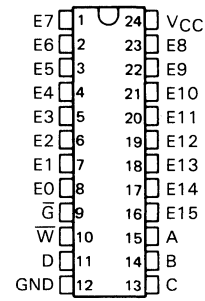
switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS245		SN74AS245		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	2	9.5	2	7.5	ns
t_{PHL}			2	9	2	7	
t_{PZH}	$\overline{G}$	A or B	2	11	2	9	ns
t_{PZL}			2	10.5	2	8.5	
t_{PHZ}	$\overline{G}$	A or B	2	7.5	2	5.5	ns
t_{PLZ}			2	12	2	9.5	

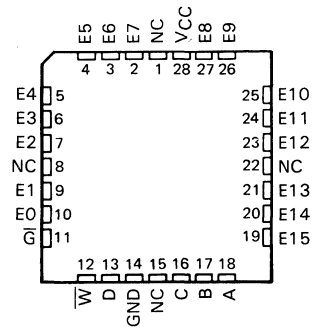
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

- 4-Line to 1-Line Multiplexer that can Select 1 and 16 Data Inputs
- Applications:
  Boolean Function Generator
  Parallel-to-Serial Converter
  Data Source Selector
- Buffered 3-State Bus Driver Inputs Permit Multiplexing from N Lines to One Line
- Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

SN74AS250 . . . DW OR NT PACKAGE
(TOP VIEW)



SN74AS250 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

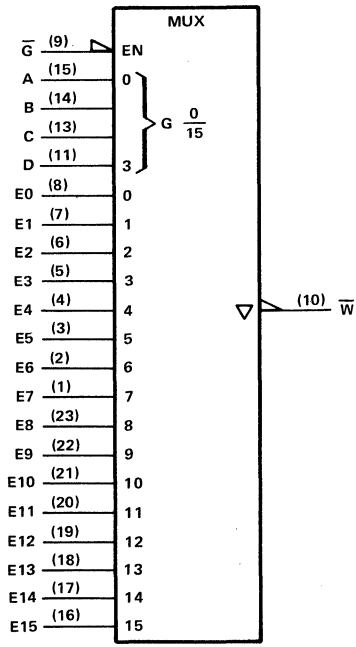
The 'AS250 provides full binary decoding to select one of sixteen data sources with an inverting $\overline{W}$ output. The selected sources are buffered with symmetrical propagation delay times. This reduces the possibility of transients occurring at the output.

A buffered enable output ($\overline{G}$) may be used for n-line-to-one-line cascading. Taking the $\overline{G}$ high will place the output in a high-impedance state. In the high-impedance state, the output neither loads nor drives the bus lines significantly.

The enable ($\overline{G}$) does not affect the internal operations of the data selector/multiplexer. New data can be set up while the outputs are disabled.

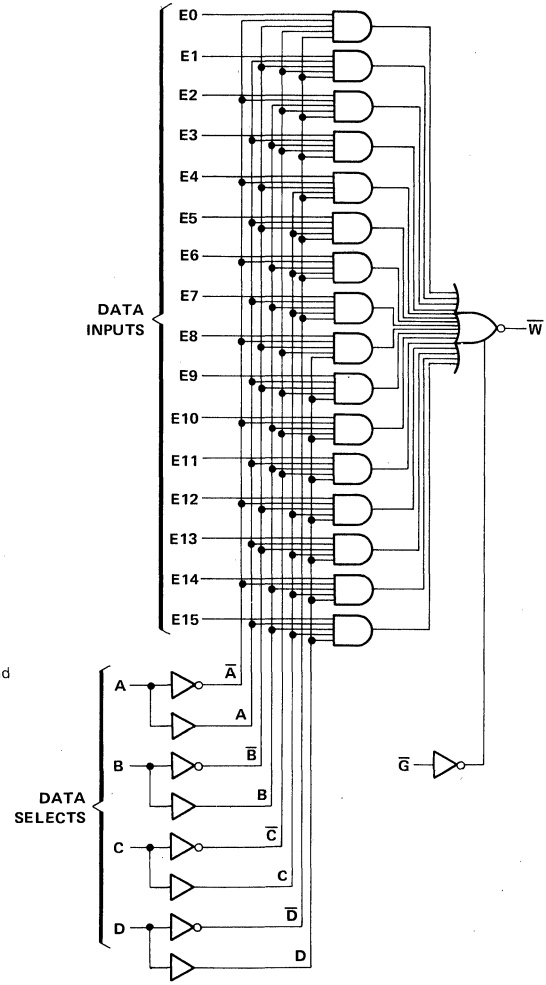
The SN74AS250 is characterized for operation from 0°C to 70°C.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publicatin 617-12.
Pin numbers shown are for DW or NT packages.

logic diagram (positive logic)



TEXAS INSTRUMENTS
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FUNCTION TABLE

INPUT						OUTPUT
$\overline{G}$	A	B	C	D	Ei	$\overline{W}$
L	L	L	L	L	E0	E0
L	H	L	L	L	E1	E1
L	L	H	L	L	E2	E2
L	H	H	L	L	E3	E3
L	L	L	H	L	E4	E4
L	H	L	H	L	E5	E5
L	L	H	H	L	E6	E6
L	H	H	H	L	E7	E7
L	L	L	L	H	E8	E8
L	H	L	L	H	E9	E9
L	L	H	L	H	E10	E10
L	H	H	L	H	E11	E11
L	L	L	H	H	E12	E12
L	H	L	H	H	E13	E13
L	L	H	H	H	E14	E14
L	H	H	H	H	E15	E15
H	X	X	X	X	X	Z

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−15	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −15 mA	2.4	3.3		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.35	0.5	V
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−50	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		26	42	mA
		Outputs low		31	50	
		Outputs disabled		30	48	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 0°C to 70°C			UNIT
			MIN	TYP†	MAX	
t_{PLH}	DATA	$\overline{W}$	3		8	ns
t_{PHL}			2		6	
t_{PLH}	SELECT	$\overline{W}$	4		13	ns
t_{PHL}			4		10	
t_{PZH}	$\overline{G}$	$\overline{W}$	2		7	ns
t_{PZL}			4		20	
t_{PHZ}	$\overline{G}$	$\overline{W}$	2		6	ns
t_{PLZ}			2		6	

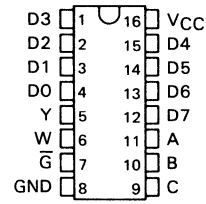
†All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54ALS251, SN54AS251, SN74ALS251, SN74AS251
1-OF-8 DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

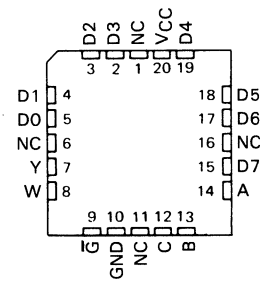
D2661, APRIL 1982—REVISED MAY 1986

- **Three-State Versions of 'ALS151 and 'AS151**
- **Three-State Outputs Interface Directly with System Bus**
- **Performs Parallel-to-Serial Conversion**
- **Complementary Outputs Provide True and Inverted Data**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS251, SN54AS251 . . . J PACKAGE
SN74ALS251, SN74AS251 . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS251, SN54AS251 . . . FK PACKAGE
(TOP VIEW)



NC — No internal connection.

description

These data selectors/multiplexers contain full binary decoding to select one-of-eight data sources and feature strobe-controlled complementary three-state outputs.

The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state), the low-impedance of the signal enabled output will drive the bus line to a high or low logic level. Both outputs are controlled by the strobe ($\overline{G}$). The outputs are disabled when $\overline{G}$ is high.

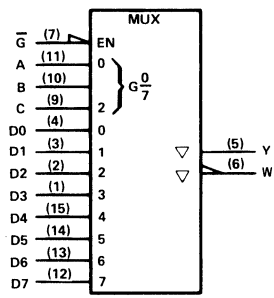
The SN54ALS251 and SN54AS251 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS251 and SN74AS251 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS				OUTPUTS	
SELECT			STROBE		
C	B	A	$\overline{G}$	Y	W
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

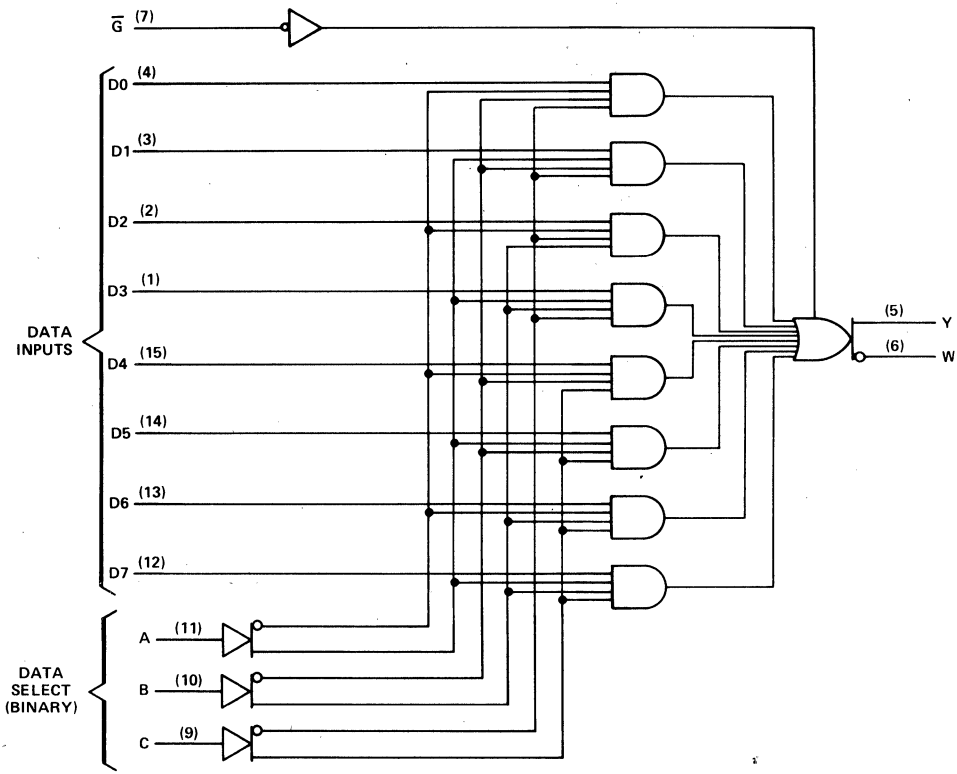
D0, D1 . . . D7 = the level of the respective D input

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS251, SN54AS251 . . . . . −55 °C to 125 °C
SN74ALS251, SN74AS251 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

recommended operating conditions

		SN54ALS251			SN74ALS251			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS251			SN74ALS251			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	Enabled	V_{CC} = 5.5 V,	Inputs at Gnd.		7	10		7	10	mA
	Disabled	V_{CC} = 5.5 V,	Inputs at 4.5 V		9.4	14		9.4	14	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS251		SN74ALS251		
			MIN	MAX	MIN	MAX	
t_{PLH}	A, B or C	Y	1	21	5	18	ns
t_{PHL}			8	34	8	24	
t_{PLH}	A, B or C	W	8	38	8	24	ns
t_{PHL}			7	26	7	23	
t_{PLH}	Any D	Y	2	15	2	10	ns
t_{PHL}			3	23	3	15	
t_{PLH}	Any D	W	3	25	3	15	ns
t_{PHL}			3	20	3	15	
t_{PZH}	$\overline{G}$	Y	3	21	3	15	ns
t_{PZL}			3	19	3	15	
t_{PZH}	$\overline{G}$	W	3	21	3	15	ns
t_{PZL}			3	19	3	15	
t_{PHZ}	$\overline{G}$	Y	2	12	2	10	ns
t_{PLZ}			1	18	1	10	
t_{PHZ}	$\overline{G}$	W	2	12	2	10	ns
t_{PLZ}			1	18	1	10	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

recommended operating conditions

		SN54AS251			SN74AS251			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			32			48	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS251			SN74AS251			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2					
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4	3.3		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−50			−50	μA
I_I	A, B, C	V_{CC} = 5.5 V,	V_I = 7 V			0.2			0.2	mA
	All other					0.1			0.1	
I_{IH}	A, B, C	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	μA
	All other					20			20	
I_{IL}	A, B, C	V_{CC} = 5.5 V,	V_I = 0.4 V		−0.6			−0.6		mA
	All other				−0.3			−0.3		
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,			28			28		mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54AS251			SN74AS251			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A, B,or C	Y		5			5		ns
t_{PHL}				5			5		
t_{PLH}	A, B, or C	W		4.5			4.5		ns
t_{PHL}				4.5			4.5		
t_{PLH}	Any D	Y		3			3		ns
t_{PHL}				4			4		
t_{PLH}	Any D	W		3			3		ns
t_{PHL}				2.5			2.5		
t_{PZH}	$\overline{G}$	Y		5			5		ns
t_{PZL}				6			6		
t_{PZH}	$\overline{G}$	W		5			5		ns
t_{PZL}				6			6		
t_{PHZ}	$\overline{G}$	Y		3			3		ns
t_{PLZ}				4			4		
t_{PHZ}	$\overline{G}$	W		3			3		ns
t_{PLZ}				4			4		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1. Load circuit and voltage waveforms are shown in Section 1.

Additional information on these products can be obtained from the factory as it becomes available.

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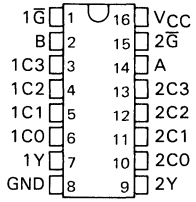
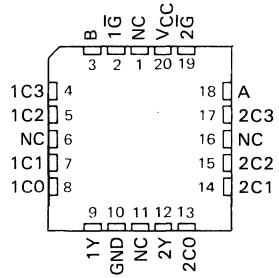
D2661, APRIL 1982—REVISED MAY 1986

- **Three-State Versions of 'ALS153 and 'AS153**
- **Permits Multiplexing from N Lines to 1 Line**
- **Performs Parallel-to-Serial Conversion**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS253, SN54AS253 . . . J PACKAGE
SN74ALS253, SN74AS253 . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS253, SN54AS253 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

Each of these data selectors/multiplexers contains inverters and drivers to supply full binary decoding data selection to the AND-OR gates. Separate output control inputs are provided for each of the two four-line sections.

The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low-impedance of the single enabled output will drive the bus line to a high or low logic level. Each output has its own strobe ($\overline{G}$). The output is disabled when its strobe is high.

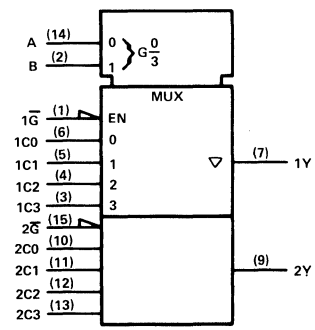
The SN54ALS253 and SN54AS253 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS253 and SN74AS253 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT CONTROL	OUTPUT
B	A	C0	C1	C2	C3	$\overline{G}$	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

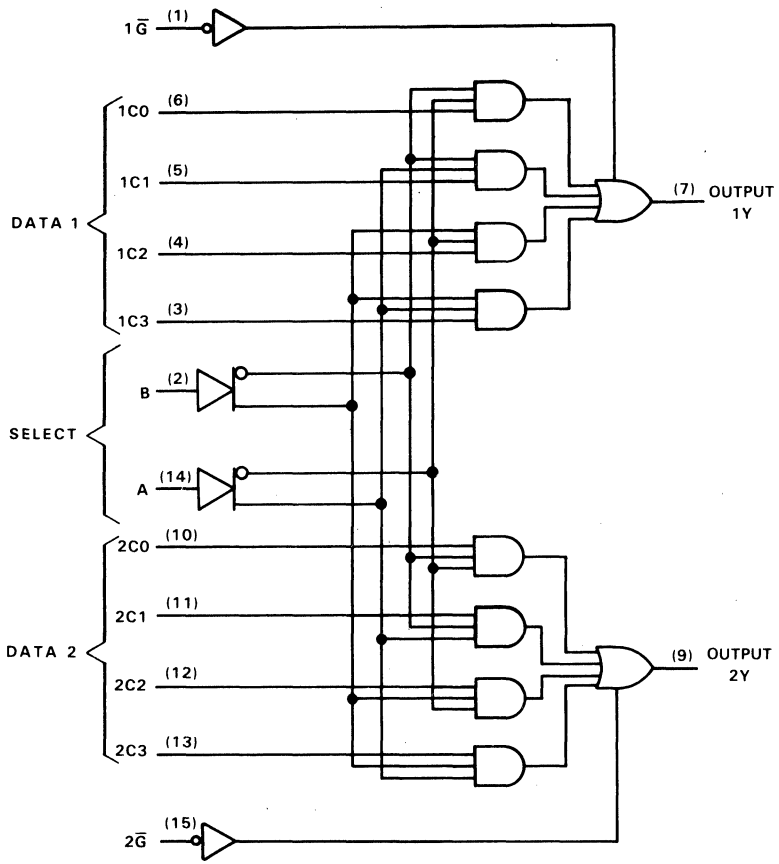
Address inputs A and B are common to both sections.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS253, SN54AS253 . . . . . −55 °C to 125 °C
SN74ALS253, SN74AS253 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS253			SN74ALS253			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS253			SN74ALS253			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs enabled		6.5	12		6.5	12	mA
		Outputs disabled		7.5	14		7.5	14	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS253		SN74ALS253		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Any Y	5	30	5	21	ns
t_{PHL}			5	27	5	21	
t_{PLH}	Data (Any C)	Any Y	2	15	2	10	ns
t_{PHL}			3	18	3	14	
t_{PZH}	$\overline{G}$	Any Y	3	20	3	14	ns
t_{PZL}			2	19	4	16	
t_{PHZ}	$\overline{G}$	Any Y	2	12	2	10	ns
t_{PLZ}			2	18	2	14	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

recommended operating conditions

		SN54AS253			SN74AS253			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			32			48	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS253			SN74AS253			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC} −2			V_{CC} −2			V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2					
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I	A, B	V_{CC} = 5.5 V,	V_I = 7 V			0.2			0.2	mA
	All others					0.1			0.1	
I_{IH}	A, B	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	μA
	All others					20			20	
I_{IL}	A, B	V_{CC} = 5.5 V,	V_I = 0.4 V			−1			−1	mA
	All others					−0.5			−0.5	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	Outputs high		18	29		18	29	mA
			Outputs low		20	32		20	32	
			Outputs disabled		21	33		21	33	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS253		SN74AS253		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	4	14.5	4	13.5	ns
t_{PHL}			4	12	4	11.5	
t_{PLH}	Data (Any C)	Y	3	8.5	3	7.5	ns
t_{PHL}			3	8.5	3	8	
t_{PZH}	G	Any Y	4	13	4	12.5	ns
t_{PZL}			4	12	4	11.5	
t_{PHZ}	G	Any Y	2	6.5	2	6	ns
t_{PLZ}			2	8	2	7	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

D2661, APRIL 1982—REVISED MAY 1986

- **Three-State Outputs Interface Directly with System Bus**
- **Provides Bus Interface from Multiple Sources in High-Performance Systems**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

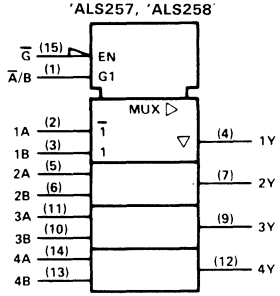
description

These devices are designed to multiplex signals from four-bit data sources to four-output data lines in bus-organized systems. The 3-state outputs will not load the data lines when the output control pin ($\overline{G}$) is at a high-logic level.

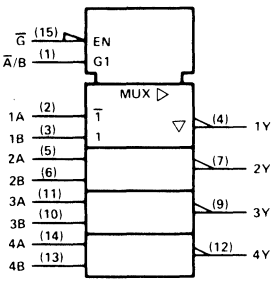
The SN54' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

logic symbol†

'ALS257, 'ALS258



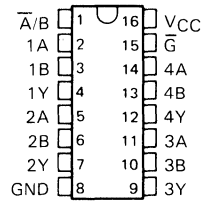
'AS257, 'AS258



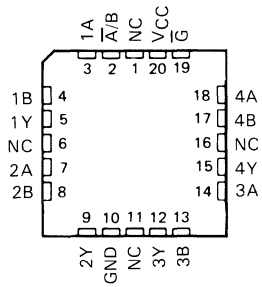
† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

SN54ALS', SN54AS' . . . J PACKAGE
SN74ALS', SN74AS' . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS', SN54AS' . . . FK PACKAGE
(TOP VIEW)

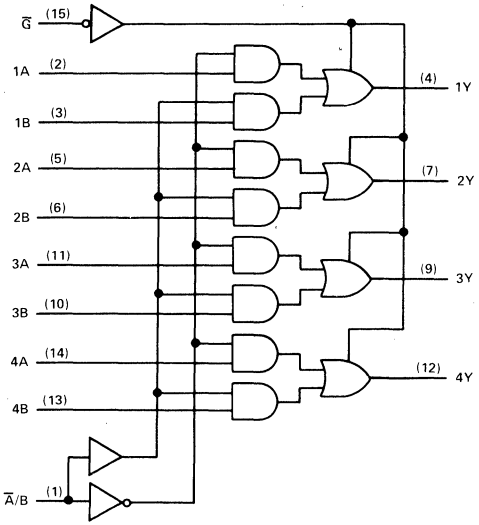


FUNCTION TABLE

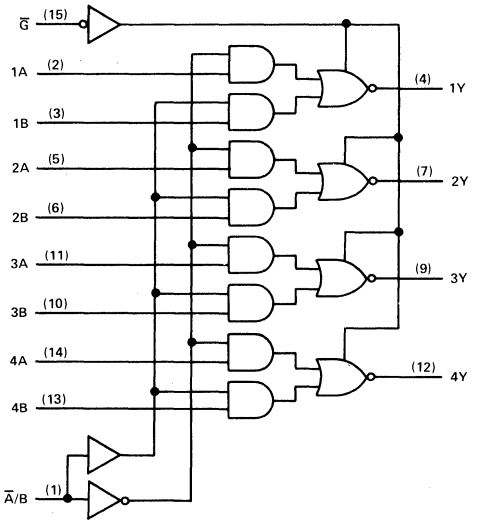
INPUTS				OUTPUT Y	
OUTPUT CONTROL $\overline{G}$	SELECT $\overline{A}/B$	DATA A	DATA B	'ALS257 'AS257	'ALS258 'AS258
H	X	X	X	Z	Z
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

logic diagram (positive logic)

'ALS257, 'AS257



'ALS258, 'AS258



Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS', SN54AS' . . . . . −55°C to 125°C
SN74ALS', SN74AS' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS257 SN54ALS258			SN74ALS257 SN74ALS258			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS257 SN54ALS258			SN74ALS257 SN74ALS258			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS257	V_{CC} = 5.5 V	Outputs high		3	6		3	6	mA
			Outputs low		8	12		8	12	
			Outputs disabled		9	14		9	14	
	'ALS258	V_{CC} = 5.5 V	Outputs high		2.5	4		2.5	4	
			Outputs low		7	11		7	11	
			Outputs disabled		8	13		8	13	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS257 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS257		SN74ALS257		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Any Y	2	12	2	10	ns
t_{PHL}			2	14	2	12	
t_{PLH}	$\overline{A}$/B	Any Y	7	21	7	18	ns
t_{PHL}			6	25	6	22	
t_{PZH}	$\overline{G}$	Any Y	4	20	4	16	ns
t_{PZL}			5	22	5	18	
t_{PHZ}	$\overline{G}$	Any Y	2	12	2	10	ns
t_{PLZ}			4	35	4	15	

'ALS258 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS258		SN74ALS258		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Any Y	1	12	2	8	ns
t_{PHL}			2	9	2	7	
t_{PLH}	$\overline{A}$/B	Any Y	5	28	8	20	ns
t_{PHL}			8	25	5	25	
t_{PZH}	$\overline{G}$	Any Y	5	20	5	18	ns
t_{PZL}			5	21	5	18	
t_{PHZ}	$\overline{G}$	Any Y	2	12	2	10	ns
t_{PLZ}			5	37	5	18	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

recommended operating conditions

		SN54AS257 SN54AS258			SN74AS257 SN74AS258			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			32			48	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS257 SN54AS258			SN74AS257 SN74AS258			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I	A, B or $\overline{G}$	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	$\overline{A}$/B					0.2			0.2	
I_{IH}	A, B, or $\overline{G}$	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	$\overline{A}$/B					40			40	
I_{IL}	A, B, or $\overline{G}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	$\overline{A}$/B					−1			−1	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'AS257	V_{CC} = 5.5 V	Outputs high		12.1	19.7		12.1	19.7	mA
			Outputs low		19	30.6		19	30.6	
			Outputs disabled		19.7	31.9		19.7	31.9	
	'AS258	V_{CC} = 5.5 V	Outputs high		8.4	13.5		8.4	13.5	
			Outputs low		15.2	24.6		15.2	24.6	
			Outputs disabled		15.5	25.2		15.5	25.2	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'AS257 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS257		SN74AS257		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Any Y	1	6.5	1	5.5	ns
t_{PHL}			1	7	1	6	
t_{PLH}	$\overline{A}$/B	Any Y	2	12	2	11	ns
t_{PHL}			2	10.5	2	10	
t_{PZH}	$\overline{G}$	Any Y	2	8.5	2	7.5	ns
t_{PZL}			2	10.5	2	9.5	
t_{PHZ}	$\overline{G}$	Any Y	1.5	8	1.5	6.5	ns
t_{PLZ}			2	8	2	7	

'AS258 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS258		SN74AS258		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Any Y	1	5.5	1	5	ns
t_{PHL}			1	5	1	4	
t_{PLH}	$\overline{A}$/B	Any Y	2	11	2	9.5	ns
t_{PHL}			2	11	2	10	
t_{PZH}	$\overline{G}$	Any Y	2	8.5	2	8	ns
t_{PZL}			2	11	2	10	
t_{PHZ}	$\overline{G}$	Any Y	1.5	7	1.5	6	ns
t_{PLZ}			2	8.5	2	6.5	

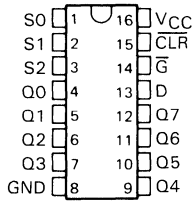
NOTE 1. Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

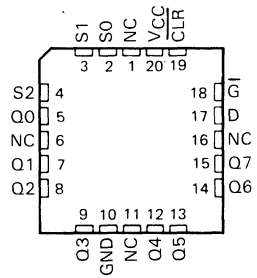
D2661, DECEMBER 1982—REVISED MAY 1986

- **8-Bit Parallel-Out Storage Register Performs Serial-to-Parallel Conversion with Storage**
- **Asynchronous Parallel Clear**
- **Active High Decoder**
- **Enable/Disable Input Simplifies Expansion**
- **Expandable for N-Bit Applications**
- **Four Distinct Functional Modes**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS259 . . . J PACKAGE
SN74ALS259 . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS259 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

These 8-bit addressable latches are designed for general purpose storage applications in digital systems. Specific uses include working registers, serial-holding registers, and active-high decoders or demultiplexers. They are multifunctional devices capable of storing single-line data in eight addressable latches, and being a 1-of-8 decoder or demultiplexer with active-high outputs.

Four distinct modes of operation are selectable by controlling the clear ($\overline{CLR}$) and enable ($\overline{G}$) inputs as enumerated in the function table. In the addressable-latch mode, data at the data-in terminal is written into the addressed latch. The addressed latch will follow the data input with all unaddressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data in the latches, enable $\overline{G}$ should be held high (inactive) while the address lines are changing. In the 1-of-8 decoding or demultiplexing mode, the addressed output will follow the level of the D input with all other outputs low. In the clear mode, all outputs are low and unaffected by the address and data inputs.

The SN54ALS259 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS259 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS $\overline{CLR}$	INPUTS $\overline{G}$	OUTPUT OF ADDRESSED LATCH	EACH OTHER OUTPUT	FUNCTION
H	L	D	Q_{i0}	Addressable Latch
H	H	Q_{i0}	Q_{i0}	Memory
L	L	D	L	8-Line Demultiplexer
L	H	L	L	Clear

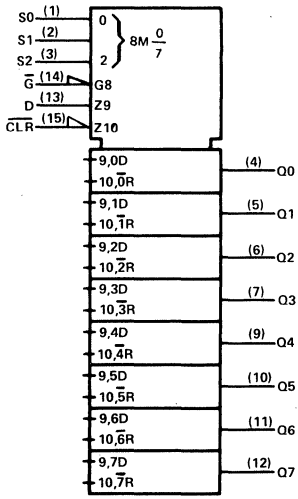
D = the level at the data input.
Q_{i0} = the level of Q_i (i = Q, 1, . . . 7, as appropriate) before the indicated steady-state input conditions were established.

LATCH SELECTION TABLE

SELECT INPUTS S2	S1	S0	LATCH ADDRESSED
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

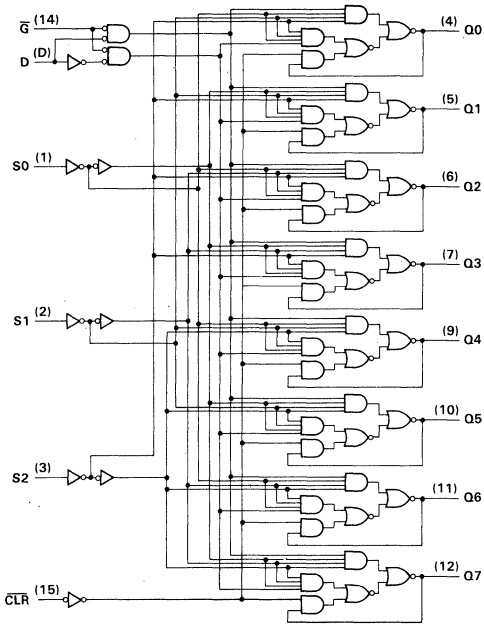
TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS259 . . . . . −55°C to 125°C
SN74ALS259 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS259			SN74ALS259			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
t_w	Pulse duration	$\overline{G}$ low	20			15			ns
		$\overline{CLR}$ low	10			10			
t_{su}	Setup time	Data before $\overline{G}$↑	20			15			ns
		Address before $\overline{G}$↑	20			15			
t_h	Hold time	Data after $\overline{G}$↑	0			0			ns
		Address after $\overline{G}$↑	0			0			
T_A	Operating free-air temperature		−55		125	0		70	°C

TEXAS INSTRUMENTS
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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS259			SN74ALS259			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V			14	22		14	22	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS259 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS259	SN54ALS259		SN74ALS259		
			TYP	MIN	MAX	MIN	MAX	
t_{PHL}	Clear	Any Q	8	2	15	2	12	ns
t_{PLH}	Data	Any Q	10	4	22	4	19	ns
t_{PHL}			8	2	15	2	12	
t_{PLH}	Address	Any Q	15	4	26	4	22	ns
t_{PHL}			8	2	15	2	12	
t_{PLH}	Enable	Any Q	13	4	22	4	20	ns
t_{PHL}			8	2	16	2	13	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

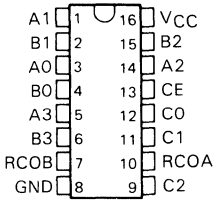
2 ALS and AS Circuits

SN54AS264, SN74AS264
LOOK-AHEAD CARRY GENERATORS FOR COUNTERS

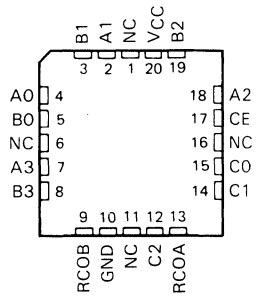
D2824, DECEMBER 1983—REVISED MAY 1986

- **Performs Look-Ahead Carry Across n-Bit Counters**
- **Accommodates Active-High or Active-Low Carry**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Improves Cascaded Counters System Performance**
- **Dependable Texas Instruments Quality and Reliability**

SN54AS264 . . . J PACKAGE
SN74AS264 . . . D OR N PACKAGE
(TOP VIEW)



SN54AS264 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

This look-ahead generator was designed specifically to perform a carry-anticipate across any number of n-bit counters,thus increasing system clock frequency. A carry enable CE, and carry outputs RCOA and RCOB are provided for n-bit cascading.

The counter can be used with either active-high-carry or active-low-carry counters. For active-high-carry counters, CE is active high, the A set of inputs and output RCOA are used, and the B set of inputs are connected to a low logic level. For active-low-carry counters, CE is active low, the B set of inputs and output RCOB are used, and the A set of inputs are connected to a high logic level. See Figures 1 and 2 for typical applications.

The SN54AS264 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS264 is characterized for operation in the temperature range of 0°C to 70°C.

positive logic equations

ACTIVE-HIGH-CARRY COUNTERS
(CE is high, all B inputs are low)

$C0 = A0$
$C1 = A0 \cdot A1$
$C2 = A0 \cdot A1 \cdot A2$
$RCOA = A0 \cdot A1 \cdot A2 \cdot A3$
RCOB is high

ACTIVE-LOW-CARRY COUNTERS
(CE is low, all A inputs are high)

$C0 = \overline{B0}$
$C1 = \overline{B0 \cdot B1}$
$C2 = \overline{B0 \cdot B1 \cdot B2}$
$RCOA = \overline{B1 \cdot B2 \cdot B3}$
$RCOB = \overline{B0 \cdot B1 \cdot B2 \cdot B3}$

FUNCTION TABLE FOR C0 OUTPUT

INPUTS			OUTPUT
A0	B0	CE	C0
H	H	X	H
H	X	H	H
L	X	X	L
X	L	L	L

FUNCTION TABLE FOR C1 OUTPUT

INPUTS					OUTPUT
A1	A0	B1	B0	CE	C1
H	X	H	X	X	H
H	H	X	H	X	H
H	H	X	X	H	H
L	X	X	X	X	L
X	L	L	X	X	L
X	X	L	L	L	L

FUNCTION TABLE FOR C2 OUTPUT

INPUTS							OUTPUT
A2	A1	A0	B2	B1	B0	CE	C2
H	X	X	H	X	X	X	H
H	H	X	X	H	X	X	H
H	H	H	X	X	H	X	H
H	H	H	X	X	X	H	H
L	X	X	X	X	X	X	L
X	L	X	L	X	X	X	L
X	X	L	L	L	X	X	L
X	X	X	L	L	L	L	L

FUNCTION TABLE FOR RCOA OUTPUT

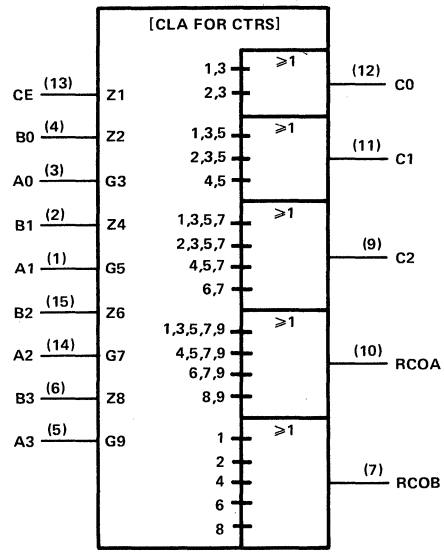
INPUTS								OUTPUT
A3	A2	A1	A0	B3	B2	B1	CE	RCOA
H	X	X	X	H	X	X	X	H
H	H	X	X	X	H	X	X	H
H	H	H	X	X	X	H	X	H
H	H	H	H	X	X	X	H	H
L	X	X	X	X	X	X	X	L
X	L	X	X	L	X	X	X	L
X	X	L	X	L	L	X	X	L
X	X	X	L	L	L	L	X	L
X	X	X	X	L	L	L	L	L

FUNCTION TABLE FOR RCOB OUTPUT

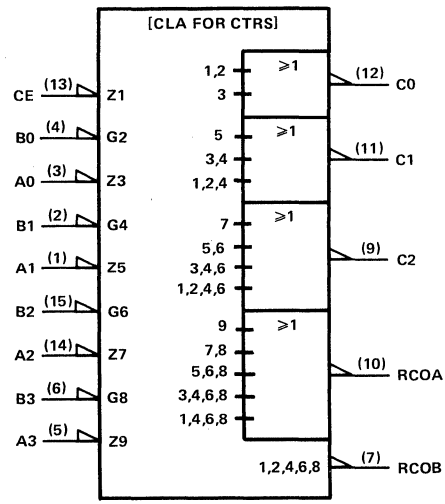
INPUTS					OUTPUT
B3	B2	B1	B0	CE	RCOB
H	X	X	X	X	H
X	H	X	X	X	H
X	X	H	X	X	H
X	X	X	H	X	H
X	X	X	X	H	H
L	L	L	L	L	L

logic symbols†

ACTIVE-HIGH INPUTS



ACTIVE-LOW INPUTS



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

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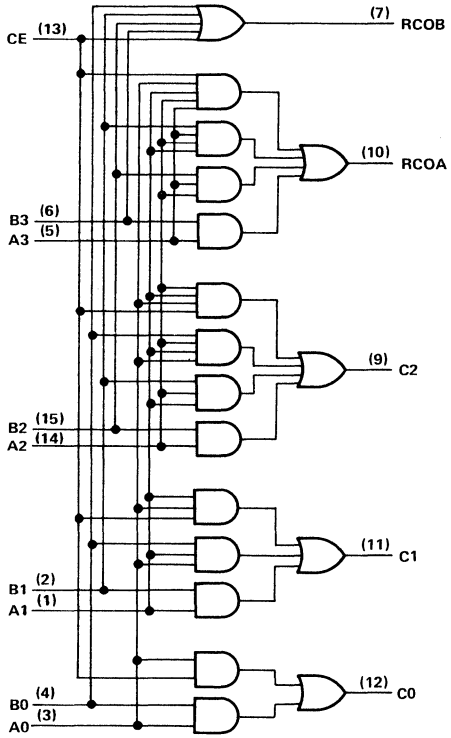
logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over free-air temperature (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS264 . . . . . −55°C to 125°C
SN74AS264 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS264			SN74AS264			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS264			SN74AS264			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.3	0.5		0.3	0.5	V
I_I	CE	V_{CC} = 5.5 V,	V_I = 7 V			500			500	μA
	A0, A2					700			700	
	A1					800			800	
	A3, B0, B1					400			400	
	B2					300			300	
	B3					200			200	
I_{IH}	CE	V_{CC} = 5.5 V,	V_I = 2.7 V			100			100	μA
	A0, A2					140			140	
	A1					160			160	
	A3, B0, B1					80			80	
	B2					60			60	
	B3					40			40	
I_{IL}	CE	V_{CC} = 5.5 V,	V_I = 0.4 V			−2.5			−2.5	mA
	A0					−3.5			−3.5	
	A1, A2					−4			−4	
	A3, B0, B1					−2			−2	
	B2					−1			−1	
	B3					−1.5			−1.5	
I_O‡		V_{CC} = 5.5 V	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}		V_{CC} = 5.5 V			26			26		mA
I_{CCL}					28			28		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 50 Ω, T_A = MIN to MAX						UNIT
			SN54AS264			SN74AS264			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	CE	C0, C1, C2		6			6		ns
t_{PHL}				5			5		
t_{PLH}	An or Bn	C0, C1, C2		5			5		ns
t_{PHL}				5			5		
t_{PLH}	An, Bn, or CE	RCOA		5			5		ns
t_{PHL}				5			5		
t_{PLH}	Bn or CE	RCOB		5			5		ns
t_{PHL}				5			5		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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TYPICAL APPLICATION INFORMATION

The circuit shown in Figure 1 illustrates how the 'AS264 can implement look-ahead carry for the active-high-carry 'AS163, while Figure 2 shows the look-ahead carry for the active-low-carry 'AS169.

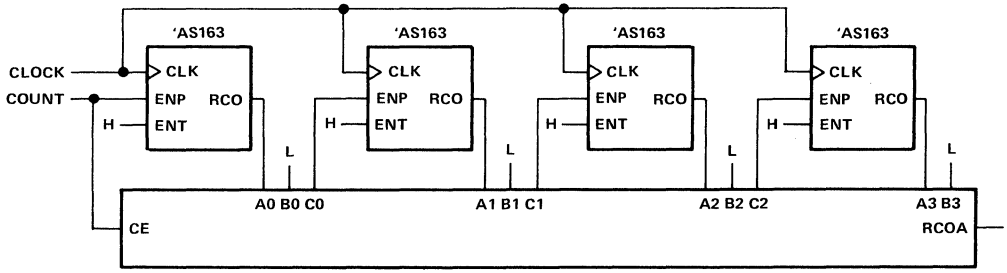


FIGURE 1–ACTIVE-HIGH-CARRY

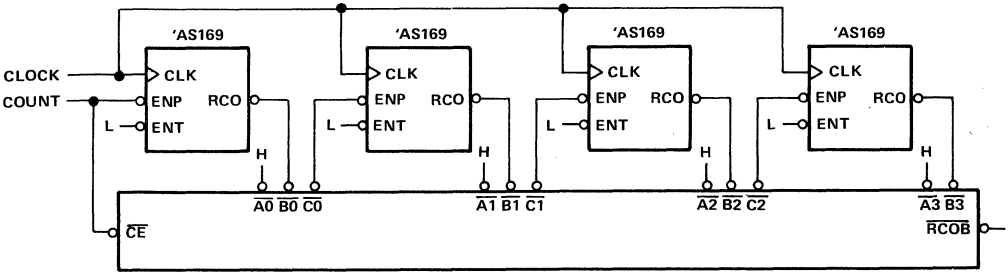
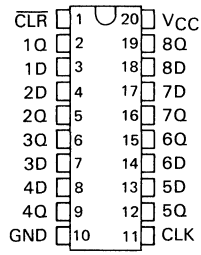


FIGURE 2–ACTIVE-LOW-CARRY

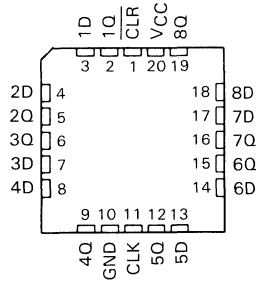
D2661, APRIL 1982—REVISED MAY 1986

- Contains Eight Flip-Flops with Single-Rail Outputs
- Buffered Clock and Direct Clear Inputs
- Individual Data Input to Each Flip-FLop
- Applications Include:
  - Buffer/Storage Registers
  - Shift Registers
  - Pattern Generators
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS273 . . . J PACKAGE
SN74ALS273 . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS273 . . . FK PACKAGE
(TOP VIEW)



description

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic with a direct clear input.

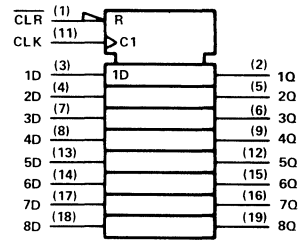
Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

The SN54ALS273 is characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS273 is characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE
(EACH FLIP-FLOP)

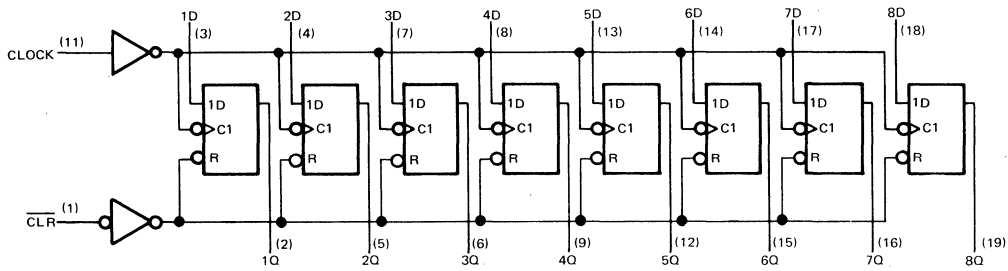
INPUTS			OUTPUT
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS273 . . . . . −55 °C to 125 °C
SN74ALS273 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

			SN54ALS273			SN74ALS273			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−1			−2.6	mA
I_{OL}	Low-level output current				12			24	mA
f_{clock}	Clock frequency		0		30	0		35	MHz
t_w	Pulse duration	$\overline{CLR}$ low	10			10			ns
		CLK high	16.5			14			
		CLK low	16.5			14			
t_{su}	Setup time before CLK↑	Data	10			10			ns
		Clear inactive state	15			15			
t_h	Hold time, data after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS273			SN74ALS273			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V			11	20		11	20	mA
I_{CCL}	V_{CC} = 5.5 V			19	29		19	29	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

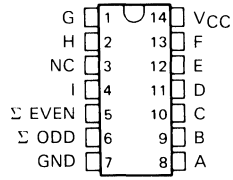
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS273		SN74ALS273		
			MIN	MAX	MIN	MAX	
f_{max}			30		35		MHz
t_{PHL}	$\overline{CLR}$	Any Q	4	24	4	18	ns
t_{PLH}	CLK	Any Q	2	20	2	12	ns
t_{PHL}			3	17	3	15	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

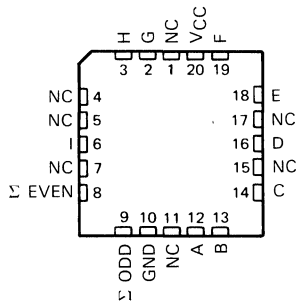
D2661, DECEMBER 1982 – REVISED MAY 1986

- **Generates Either Odd or Even Parity for Nine Data Lines**
- **Cascadable for n-Bits Parity**
- **Can Be Used to Upgrade Existing Systems Using MSI Parity Circuits**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS280, SN54AS280 . . . J PACKAGE
SN74ALS280, SN74AS280 . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS280, SN54AS280 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These universal, monolithic, nine-bit parity generators/checkers utilize Advanced Schottky high-performance circuitry and feature odd and even outputs to facilitate operation of either odd or even parity application. The word-length capability is easily expanded by cascading.

These devices can be used to upgrade the performance of most systems utilizing the '180 parity generator/checker. Although the 'ALS280 and 'AS280 are implemented without expander inputs, the corresponding function is provided by the availability of an input at pin 4 and the absence of any internal connection at pin 3. This permits the 'ALS280 and 'AS280 to be substituted for the '180 in existing designs to produce an identical function even if the devices are mixed with existing '180's.

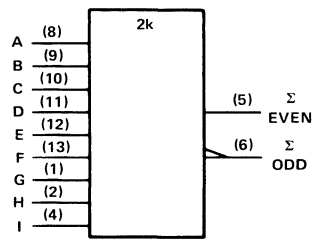
All 'AS280 inputs are buffered to lower the drive requirements.

The SN54' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

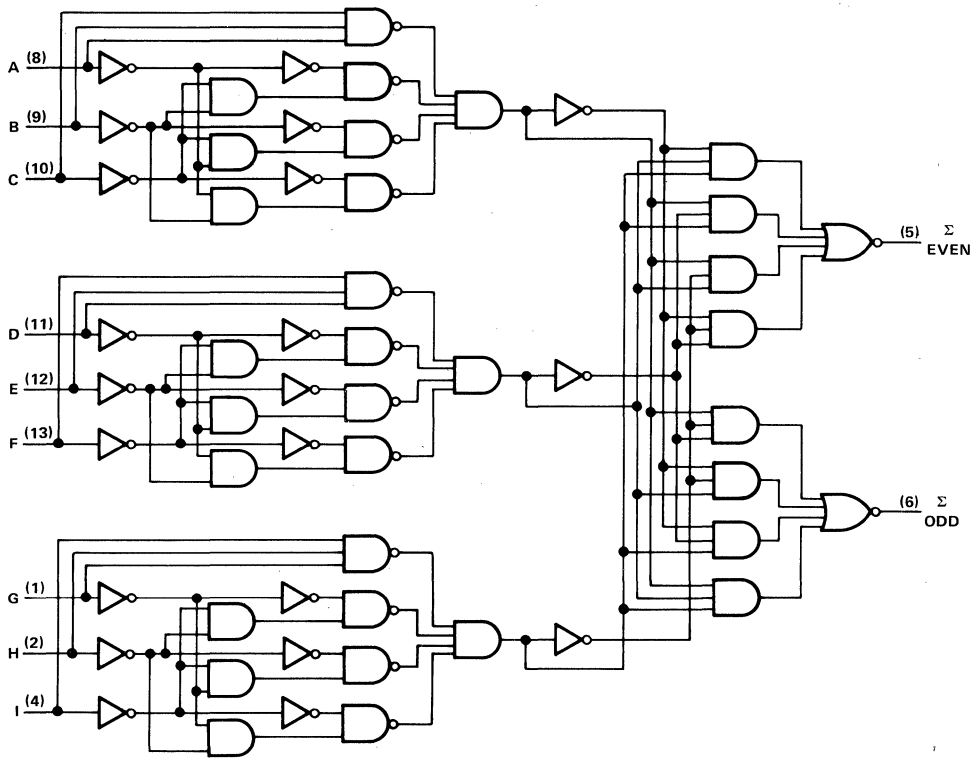
NUMBER OF INPUTS A THRU I THAT ARE HIGH	OUTPUTS	
	Σ EVEN	Σ ODD
0,2,4,6,8	H	L
1,3,5,7,9	L	H

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS280 . . . . . −55°C to 125°C
SN74ALS280 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS280			SN74ALS280			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

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POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS280			SN74ALS280			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V			10	16		10	16	mA

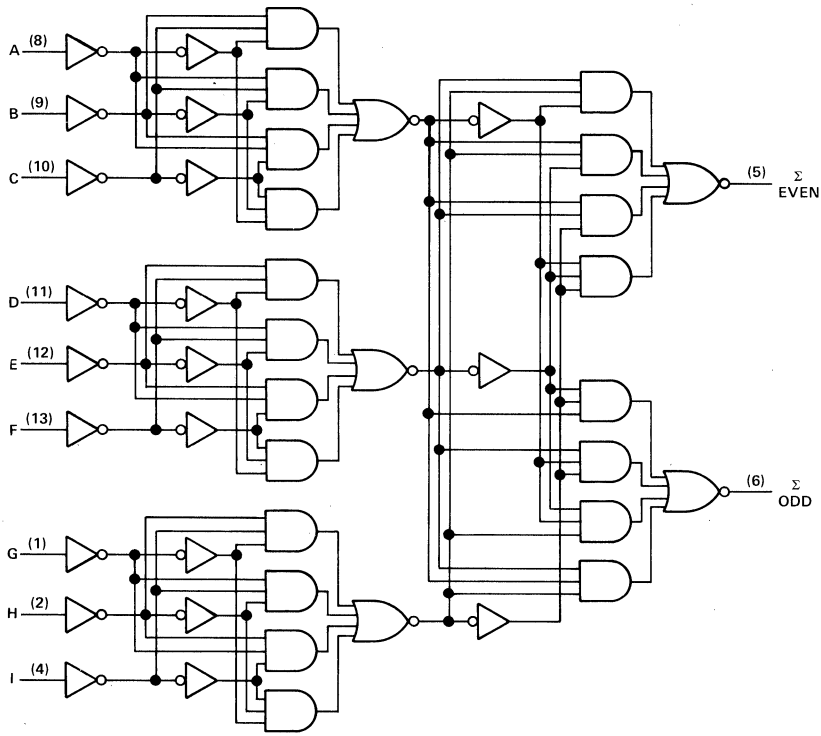
†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS280	SN54ALS280		SN74ALS280		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	Any	Σ Even	12	3	24	3	20	ns
t_{PHL}			12	3	24	3	20	
t_{PLH}	Any	Σ Odd	12	3	24	3	20	ns
t_{PHL}			13	4	26	4	22	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

logic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS280 . . . . . −55°C to 125°C
SN74AS280 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS280			SN74AS280			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS280			SN74AS280			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V			25	40		25	35	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

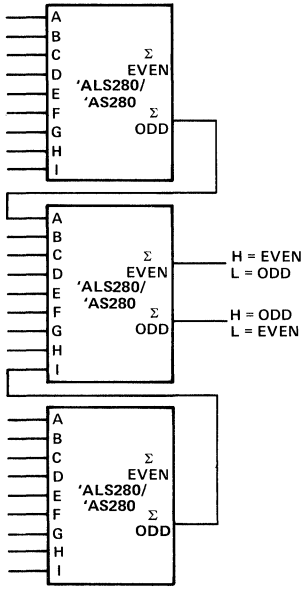
switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS280		SN74AS280		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any	Σ Even	3	13	3	12	ns
t_{PHL}			3	12.5	3	11	
t_{PLH}	Any	Σ Odd	3	13	3	12	ns
t_{PHL}			3	12.5	3	11.5	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TYPICAL APPLICATION DATA

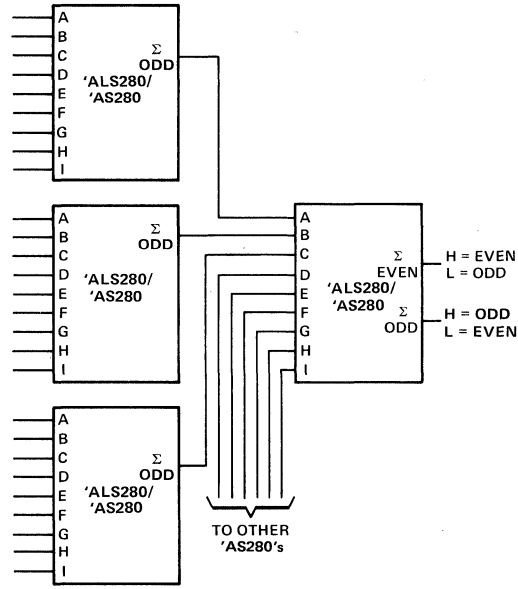
25-LINE PARITY/GENERATOR CHECKER



Three 'ALS280/'AS280 can be used to implement a 25-line parity generator/checker.

As an alternative, the Σ ODD outputs of two or three parity generators/checkers can be decoded with a 2-input ('S86 or 'LS86) or 3-input ('S135) exclusive-OR gate for 18- or 27-line parity applications.

81-LINE PARITY/GENERATOR CHECKER



Longer word lengths can be implemented by cascading 'ALS280/'AS280. As shown here, parity can be generated for word lengths up to 81 bits.

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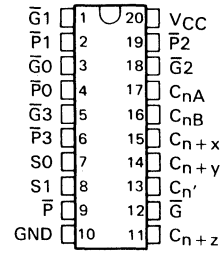
SN54AS282, SN74AS282
LOOK-AHEAD CARRY GENERATOR WITH SELECTABLE CARRY INPUTS

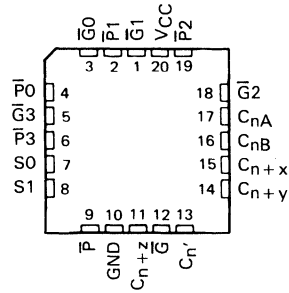
D2811, DECEMBER 1983—REVISED MAY 1986

- **Selectable Carry Inputs Version of the Popular 'S182 Allows Double Precision Carry**
- **Offers Carry Functions in a Compatible Form for Direct Connection to the ALU**
- **Cascadable to Perform Look-Ahead Across n-Bit Adders**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54AS282 . . . J PACKAGE
SN74AS282 . . . DW OR N PACKAGE
(TOP VIEW)



SN54AS282 . . . FK PACKAGE
(TOP VIEW)



PIN DESIGNATIONS

ALTERNATIVE DESIGNATIONS†		FUNCTION
$\overline{G}0$, $\overline{G}1$, $\overline{G}2$, $\overline{G}3$	G0, G1, G2, G3	Carry Generate Inputs
$\overline{P}0$, $\overline{P}1$, $\overline{P}2$, $\overline{P}3$	P0, P1, P2, P3	Carry Propagate Inputs
C_{nA}, C_{nB}	$\overline{C}_{nA}$, $\overline{C}_{nB}$	Carry Inputs
$C_{n'}$	$\overline{C}_{n'}$	Selected Carry
C_{n+x}, C_{n+y}, C_{n+z}	$\overline{C}_{n+x}$, $\overline{C}_{n+y}$, $\overline{C}_{n+z}$	Carry Outputs
$\overline{G}$	Y	Carry Generate Outputs
$\overline{P}$	X	Carry Propagate Outputs
S0, S1		Carry Select Inputs
V_{CC}		Supply Voltage
GND		Ground

† Interpretations are illustrated in connection with the Function Tables for the 'AS181A and 'AS881A.

description

The 'AS282 look-ahead carry generator is capable of anticipating a carry across four binary adders or group of adders. They are cascadable to perform full look-ahead across n-bit adders. The 'AS282 is functionally the same as the SN54AS182/SN74AS182 except that the carry input (C_n) is selected from C_{nA}, C_{nB}, and their complements $\overline{C}_{nA}$ and $\overline{C}_{nB}$. The logic equations are written in terms of the selected carry C_n. This signal is also available as an output at $C_{n'}$.

When used in conjunction with the 'AS181A, 'AS881A, or 'AS888 arithmetic logic unit (ALU), this generator provides high-speed carry look-ahead capability for any word length. The 'AS282 generates the look-ahead (anticipated carry) across a group of four ALU's and, in addition, other carry across sections of four look-ahead circuits may be employed to anticipated carry across sections of four look-ahead packages up to n-bits. The method of cascading 'AS282 circuits to perform multi-level look-ahead is illustrated under typical application data.

logic equations

$$C_{n+x} = G0 + P0\,C_n$$
$$C_{n+y} = G1 + P1\,G0 + P1\,P0\,C_n$$
$$C_{n+z} = G2 + P2\,G1 + P2\,P1\,G0 + P2\,P1\,P0\,C_n$$
$$\overline{G} = \overline{G3 + P3\,G2 + P3\,P2\,G1 + P3\,P2\,P1\,G0}$$
$$\overline{P} = \overline{P3\,P2\,P1\,P0}$$

or

$$\overline{C}_{n+x} = \overline{Y0\,(X0 + C_n)}$$
$$\overline{C}_{n+y} = \overline{Y1\,[X1 + Y0\,(X0 + C_n)]}$$
$$\overline{C}_{n+z} = \overline{Y2\,\{X2 + Y1\,[X1 + Y0\,(X0 + C_n)]\}}$$
$$Y = Y3\,(X3 + Y2)\,(X3 + X2 + Y1)\,(X3 + X2 + X1 + Y0)$$
$$X = X3 + X2 + X1 + X0$$

FUNCTION TABLE FOR $\overline{G}$ OUTPUT

INPUTS							OUTPUT
$\overline{G3}$	$\overline{G2}$	$\overline{G1}$	$\overline{G0}$	$\overline{P3}$	$\overline{P2}$	$\overline{P1}$	$\overline{G}$
L	X	X	X	X	X	X	L
X	L	X	X	L	X	X	L
X	X	L	X	L	L	X	L
X	X	X	L	L	L	L	L
All other combinations							H

FUNCTION TABLE FOR $\overline{P}$ OUTPUT

INPUTS				OUTPUT
$\overline{P3}$	$\overline{P2}$	$\overline{P1}$	$\overline{P0}$	$\overline{P}$
L	L	L	L	L
All other combinations				H

FUNCTION TABLE FOR $C_{n'}$ OUTPUT

INPUTS		OUTPUT
S1	S0	$C_{n'}$
L	L	C_{nA}
L	H	$\overline{C}_{nA}$
H	L	C_{nB}
H	H	$\overline{C}_{nB}$

FUNCTION TABLE FOR C_{n+x} OUTPUT

INPUTS			OUTPUT
$\overline{G0}$	$\overline{P0}$	Cn'	C_{n+x}
L	X	X	H
X	L	H	H
All other combinations			L

FUNCTION TABLE C_{n+y} OUTPUT

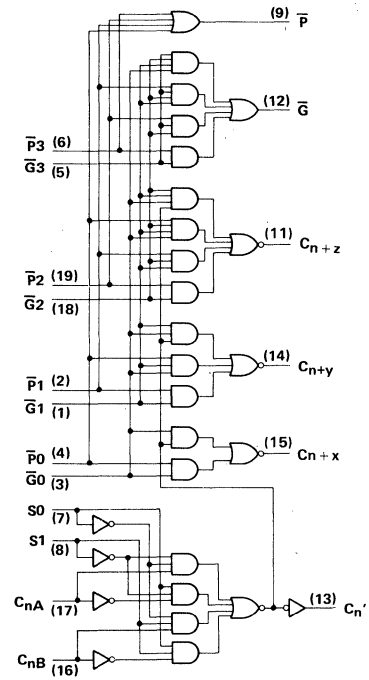
INPUTS					OUTPUT
$\overline{G1}$	$\overline{G0}$	$\overline{P1}$	$\overline{P0}$	$C_{n'}$	C_{n+y}
L	X	X	X	X	H
X	L	L	X	X	H
X	X	L	L	H	H
All other combinations					L

FUNCTION TABLE FOR C_{n+z} OUTPUT

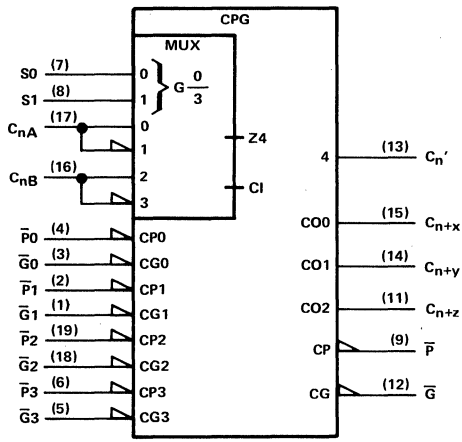
INPUTS							OUTPUT
$\overline{G2}$	$\overline{G1}$	$\overline{G0}$	$\overline{P2}$	$\overline{P1}$	$\overline{P0}$	$C_{n'}$	C_{n+z}
L	X	X	X	X	X	X	H
X	L	X	L	X	X	X	H
X	X	L	L	L	X	X	H
X	X	X	L	L	L	H	H
All other combinations							L

H = high-level, L = low level, X = irrelevant.
Any inputs not shown in a given table are irrelevant with respect to that output.

logic diagram (positive logic)



logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS282 . . . . . −55°C to 125°C
SN74AS282 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS282			SN74AS282			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS282			SN74AS282			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.3	0.5		0.3	0.5	V
I_I	C_{nA}, C_{nB}	V_{CC} = 5.5 V,	V_I = 7 V			200			200	μA
	S0, S1, $\overline{P}3$					200			200	
	$\overline{P}2$					300			300	
	$\overline{P}0$, $\overline{P}1$, $\overline{G}3$					400			400	
	$\overline{G}0$, $\overline{G}2$					700			700	
	$\overline{G}1$					800			800	
I_{IH}	C_{nA}, C_{nB}	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	μA
	S0, S1, $\overline{P}3$					40			40	
	$\overline{P}2$					60			60	
	$\overline{P}0$, $\overline{P}1$, $\overline{G}3$					80			80	
	$\overline{G}0$, $\overline{G}2$					140			140	
	$\overline{G}1$					160			160	
I_{IL}	C_{nA}, C_{nB}	V_{CC} = 5.5 V,	V_I = 0.4 V			−1			−1	mA
	S0, S1, $\overline{P}3$					−1			−1	
	$\overline{P}2$					−1.5			−1.5	
	$\overline{P}0$, $\overline{P}1$, $\overline{G}3$					−2			−2	
	$\overline{G}0$, $\overline{G}2$					−3.5			−3.5	
	$\overline{G}1$					−4			−4	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}		V_{CC} = 5.5 V			22			22		mA
I_{CCL}					26			26		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			SN54AS282			SN74AS282			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	S0, S1, C_{nA}, or C_{nB}	$C_{n'}$		6			6		ns
t_{PHL}				6			6		
t_{PLH}	S0, S1, C_{nA}, or C_{nB}	C_{n+x}, C_{n+y}, C_{n+z}		6			6		ns
t_{PHL}				6			6		
t_{PLH}	$\overline{P}$ or $\overline{G}$	C_{n+x}, C_{n+y}, C_{n+z}		5			5		ns
t_{PHL}				5			5		
t_{PLH}	$\overline{P}$ or $\overline{G}$	$\overline{G}$		6			6		ns
t_{PHL}				5			5		
t_{PLH}	$\overline{P}$	$\overline{P}$		5			5		ns
t_{PHL}				5			5		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TYPICAL APPLICATION DATA

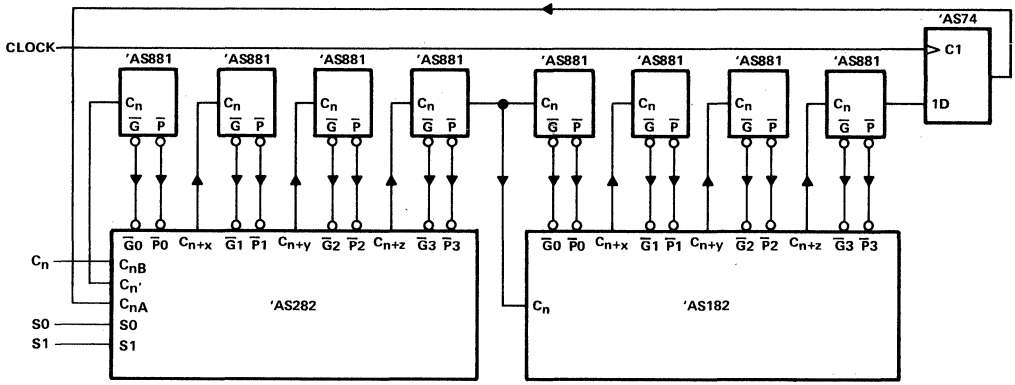
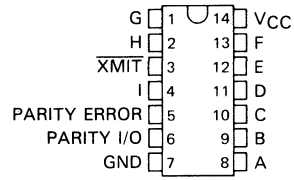


FIGURE 1–32-BIT LOOK-AHEAD CARRY WITH DOUBLE-PRECISION CARRY IN 'AS282 AND 'AS182

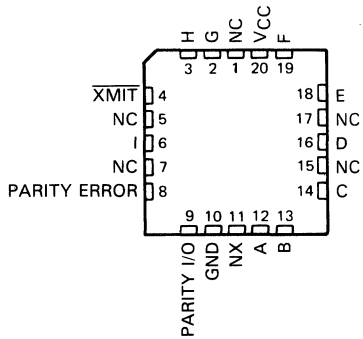
TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

- **Generates Either Odd or Even Parity for Nine Data Lines**
- **Cascadable for n-Bits Parity**
- **Direct Bus Connection for Parity Generation or for Checking by Using the Parity I/O Port**
- **Glitch-Free Bus During Power Up/Down**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54AS286 . . . J PACKAGE
SN74AS286 . . . D OR N PACKAGE
(TOP VIEW)



SN54AS286 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN54AS286 and SN74AS286 universal nine-bit parity generators/checkers feature a local output for parity checking and a 48-milliampere bus-driving parity I/O port for parity generation/checking. The word-length capability is easily expanded by cascading.

The $\overline{\text{XMIT}}$ control input is implemented specifically to accommodate cascading. When $\overline{\text{XMIT}}$ is low the parity tree is disabled and PE will remain at a high logic level regardless of the input levels. When $\overline{\text{XMIT}}$ is high the parity tree is enabled. The Parity Error output will indicate a parity error when either an even number of inputs (A through I) are high and Parity I/O is forced to a low logic level, or when an odd number of inputs are high and Parity I/O is forced to a high logic level.

The I/O control circuitry was designed so that the I/O port will remain in the high-impedance state during power-up or power-down to prevent bus glitches.

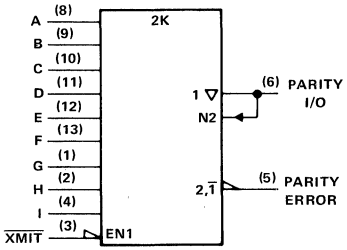
The SN54AS286 is characterized for operation over the full military range of −55°C to 125°C. The SN74AS286 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

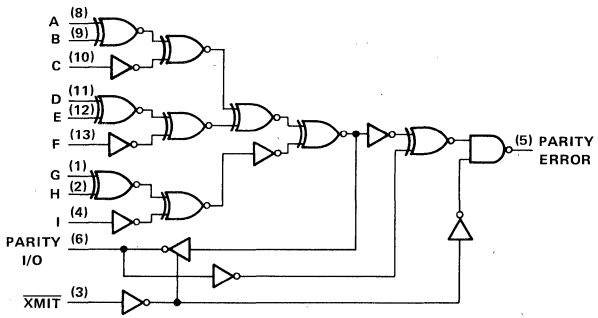
NUMBER OF INPUTS (A THRU I) THAT ARE HIGH	$\overline{XMIT}$	PARITY I/O	PARITY ERROR
0, 2, 4, 6, 8	l	H	H
1, 3, 5, 7, 9	l	L	H
0, 2, 4, 6, 8	h	h	H
	h	l	L
1, 3, 5, 7, 9	h	h	L
	h	l	H

h — high input level l — low input level
H — high output level L — low output level

logic symbol†



logic diagram (positive logic)



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54AS286 . . . . . −55°C to 125°C
SN74AS286 . . . . . 0°C to 70°C
Storage temperature . . . . . −65°C to 140°C

recommended operating conditions

			SN54AS286			SN74AS286			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current	Parity error			−2			−2	mA
		Parity I/O			−12			−15	
I_{OL}	Low-level output current	Parity error			20			20	mA
		Parity I/O			32			48	
T_A	Operating free-air temperature		−55		125	0		70	°C

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics over recommended free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS286			SN74AS286			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	All outputs	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
	Parity I/O	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	2.9		2.4	3		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4			
V_{OL}	Parity error	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
	Parity I/O	V_{CC} = 4.5 V,	I_{OL} = 32 mA			0.5				
		V_{CC} = 4.5 V,	I_{OL} = 48 mA						0.5	
I_I	Parity I/O	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	mA
	All other inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	
I_{IH}	Parity I/O‡	V_{CC} = 5.5 V,	V_I = 2.7 V			50			50	μA
	All other inputs					20			20	
I_{IL}	Parity I/O‡	V_{CC} = 5.5 V,	V_I = 0.4 V			0.5			-0.5	mA
	All other inputs					0.5			-0.5	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	Transmit	V_{CC} = 5.5 V			30	43		30	43	mA
	Receive				35	50		35	50	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡For I/O ports, the parameters I_{IH} and I_{IL} include the off-state current.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS286		SN74AS286		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any A thru I	Parity I/O	3	17	3	15	ns
t_{PHL}			3	15	3	14	
t_{PLH}	Any A thru I	Parity error	3	20	3	16.5	ns
t_{PHL}			3	18	3	16.5	
t_{PLH}	Parity I/O	Parity error	3	10	3	9	ns
t_{PHL}			3	10	3	9	
t_{PZH}	$\overline{XMIT}$	Parity I/O	3	14	3	13	ns
t_{PZL}			3	17	3	16	
t_{PHZ}			3	13	3	11.5	
t_{PLZ}			3	11	3	10	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TYPICAL APPLICATION DATA

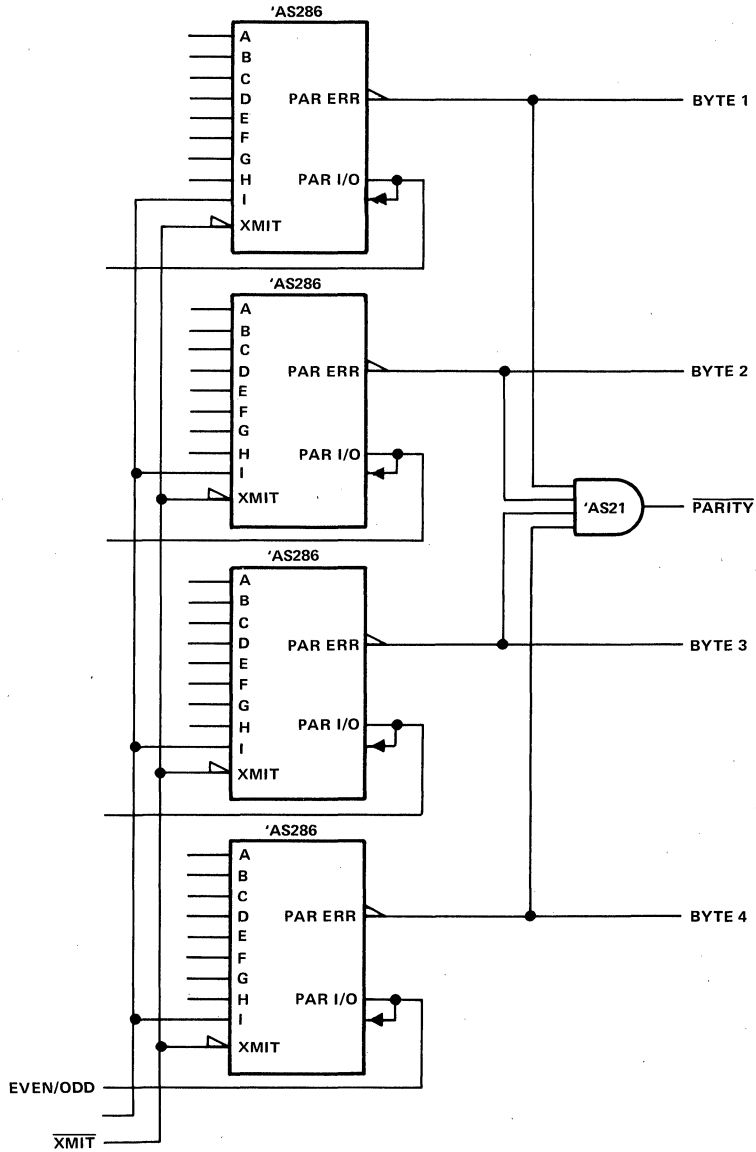


FIGURE 1. 32-BIT PARITY GENERATOR/CHECKER

Figure 1 shows a 32-bit parity generator/checker with output polarity-switching, parity error detection, and parity on every byte.

TEXAS INSTRUMENTS
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TYPICAL APPLICATION DATA

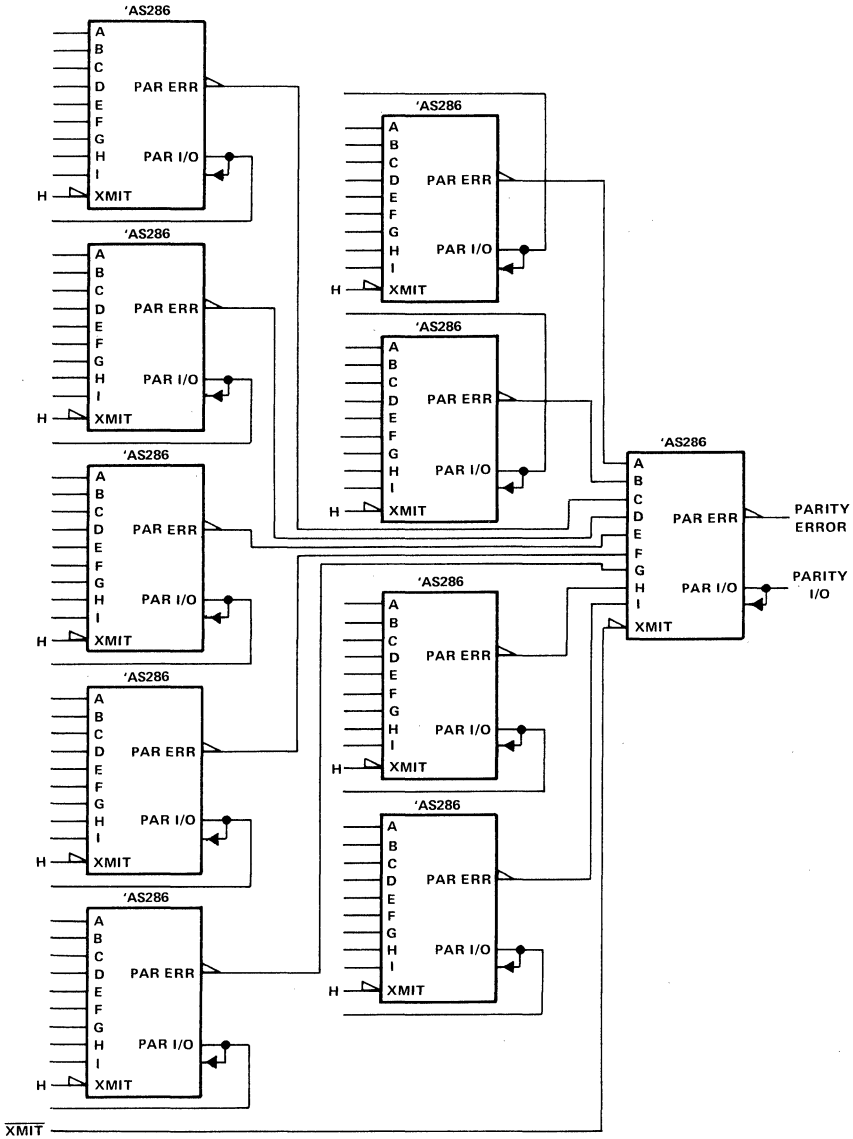


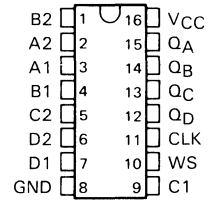
FIGURE 2. 90-BIT PARITY GENERATOR/CHECKER WITH PARITY ERROR DETECTION

In Figure 2, a 90-bit parity generator/checker with the $\overline{\text{XMIT}}$ on the last stage is available for use with parity detection.

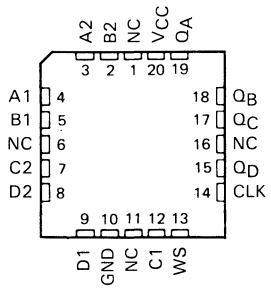
D2661, DECEMBER 1983—REVISED MAY 1986

- Selects One of Two 4-Bit Data Sources and Stores Data Synchronously with System Clock
- Applications:
  - Dual Source for Operands and Constants in Arithmetic Processor; Can Release Processor Register Files for Acquiring New Data
  - Implements Separate Registers Capable of Parallel Exchange of Contents, yet Retains External Load Capability
  - Has Universal-Type Register for Implementing Various Shift Patterns, including Compound Left-Right Capability
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

SN54AS298 . . . J PACKAGE
SN74AS298 . . . D OR N PACKAGE
(TOP VIEW)



SN54AS298 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

This quadruple two-input multiplexer with storage provides essentially the equivalent functional capabilities of two separate MSI functions (SN54AS157/SN74AS157 and SN54AS175/SN74AS175) in a single 16-pin package.

When the word-select (WS) input is low, Word 1 (A1, B1, C1, D1 is applied to the flip-flops. A high input to the word-select (WS) will cause the selection of Word 2 (A2, B2, C2, D2). The selected word is clocked to the output terminals on the negative-going edge of the clock pulse.

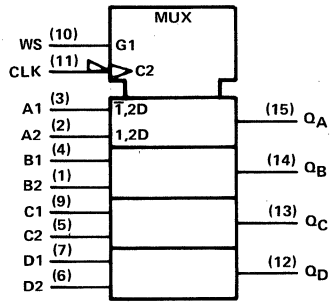
The SN54AS298 is characterized for operation over the full military range of −55°C to 125°C. The SN74AS298 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

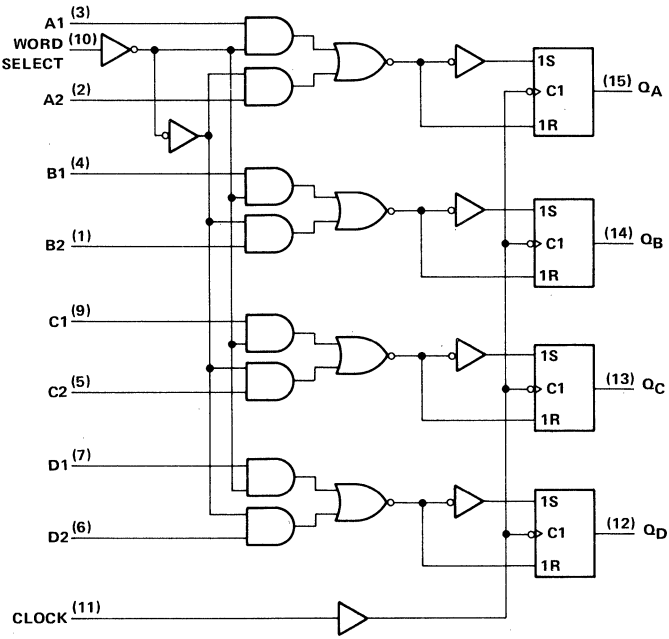
INPUTS		OUTPUTS			
WORD SELECT	CLOCK	Q_A	Q_B	Q_C	Q_D
L	↓	a1	b1	c1	d1
H	↓	a2	b2	c2	d2
X	H	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↓ = transition from high to low level
a1, a2, etc. = the level of steady-state input at A1, A2, etc.
Q_{A0}, Q_{B0}, etc. = the level of Q_A, Q_B, etc. entered on the most-recent ↓ transition of the clock input.

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS298 . . . . . −55°C to 125°C
SN74AS298 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54AS298			SN74AS298			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−2	mA
I_{OL}	Low-level output current				20			20	mA
f_{clock}	Clock frequency		0		100	0		100	MHz
t_w	Pulse duration, CLK high or low		5			5			ns
t_{su}	Setup time before CLK ↓	Data	4.5			4.5			ns
		Word Select	13			13			
t_h	Hold time after CLK ↓	Data	3.5			3.5			ns
		Word Select	1			1			
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS298			SN74AS298			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1			−1	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	WS	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	μA
	All other					20			20	
I_{IL}	WS	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.75			−0.75	mA
	All other					−0.5			−0.5	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}		V_{CC} = 5.5 V			21	33		21	33	mA
I_{CCL}		V_{CC} = 5.5 V			22	36		22	36	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characterisitcs (see Note 1)

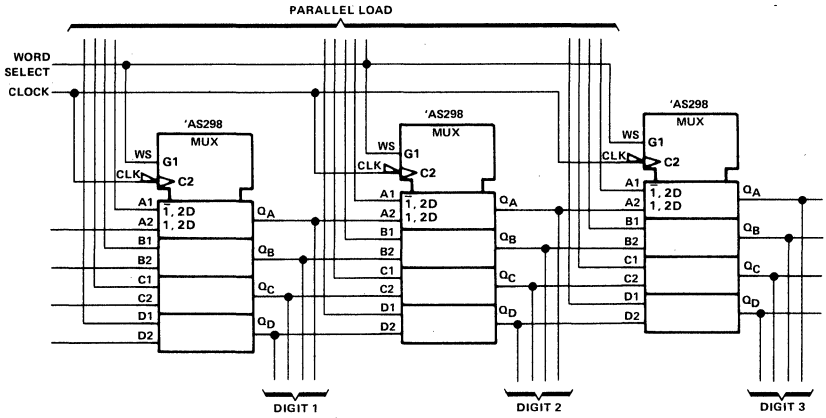
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS298		SN74AS298		
			MIN	MAX	MIN	MAX	
f_{max}			100		100		MHz
t_{PLH}	CLK	Q	2	16	2	9	ns
t_{PHL}			1	12	1	11	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TYPICAL APPLICATION DATA

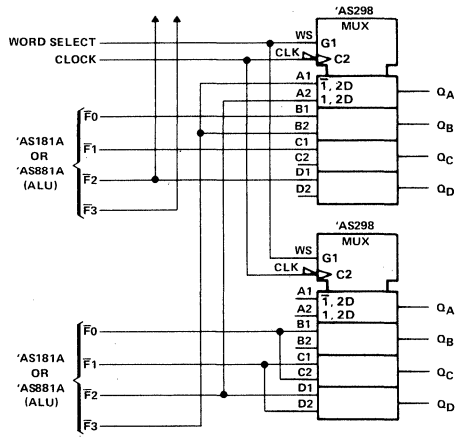
This versatile multiplexer/register can be connected to operate as a shift register that can shift N-places in a single clock pulse.

The following figure illustrates a BCD shift register that will shift an entire 4-bit BCD digit in one clock pulse.



When the word-select input is high and the registers are clocked, the contents of register 1 is transferred (shifted) to register 2, etc. In effect, the BCD digits are shifted one position. In addition, this application retains a parallel-load capability which means that new BCD data can be entered in the entire register with one clock pulse. This arrangement can be modified to perform the shifting of binary data for any number of bit locations.

Another function that can be implemented with the 'AS298 is a register that can be designed specifically for supporting multiplier or division operations. The example below is a one-place/two-place shift register.



When word select is low and the register is clocked, the outputs of the arithmetic/logic units (ALUs) are shifted one place. When word select is high and the registers are clocked, the data is shifted two places.

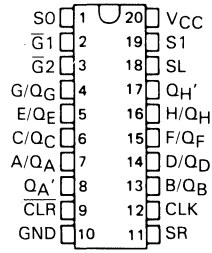
TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH 3-STATE OUTPUTS

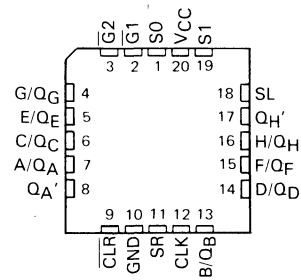
D2661, DECEMBER 1982—REVISED MAY 1986

- Multiplexed I/O Ports Provides Improved Bit Density
- Four Modes of Operation: Hold (Store), Shift Right, Shift Left, and Load Data
- Operates with Outputs Enabled or at High Impedance
- 3-State Outputs Drive Bus Lines Directly
- Can Be Cascaded for N-Bit Word Lengths
- 'ALS299 and AS299 Have Direct Overriding Clear
- 'ALS323 and AS323 Have Synchronous Clear
- Application:
  Stacked or Push-Down Registers, Buffer Storage, and Accumulator Registers
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS', SN54AS' . . . J PACKAGE
SN74ALS', SN74AS' . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS', SN54AS' . . . FK PACKAGE
(TOP VIEW)



description

These eight-bit universal registers feature multiplexed I/O ports to achieve full eight-bit data handling in a single 20-pin package. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table.

Synchronous parallel loading is accomplished by taking both function-select lines S0 and S1 high. This places the three-state outputs in a high-impedance state and permits data that is applied on the I/O ports to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. Clearing occurs asynchronously on 'ALS299, 'AS299 and synchronously on 'ALS323, 'AS323 when $\overline{CLR}$ is low. Taking either of the output controls, $\overline{G}1$ or $\overline{G}2$, high disables the outputs but this has no effect on clearing, shifting, or storage of data.

The SN54' family is characterized for operation over the full military range of −55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

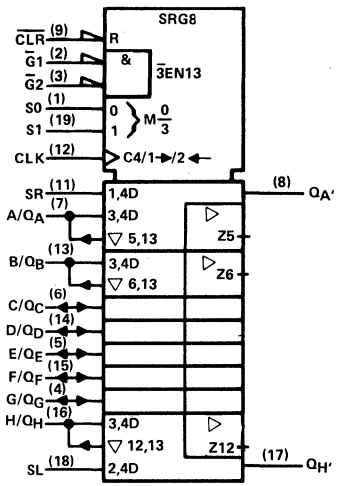
FUNCTION TABLE

MODE	INPUTS								I/O PORTS								OUTPUTS	
	$\overline{CLR}$	S1	S0	OUTPUT CONTROL $\overline{G1}$	OUTPUT CONTROL $\overline{G2}$	CLK	SL	SR	A/Q_A	B/Q_B	C/Q_C	D/Q_D	E/Q_E	F/Q_F	G/Q_G	H/Q_H	Q_A'	Q_H'
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
('ALS299)	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
('AS299)	L	H	H	X	X	X	X	X	X	X	X	X	X	X	X	X	L	L
Clear	L	X	L	L	L	↑	X	X	L	L	L	L	L	L	L	L	L	L
('ALS323)	L	L	X	L	L	↑	X	X	L	L	L	L	L	L	L	L	L	L
('AS323)	L	H	H	X	X	↑	X	X	X	X	X	X	X	X	X	X	L	L
Hold	H	L	L	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
	H	X	X	L	L	L	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
Shift Right	H	L	H	L	L	↑	X	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	H	Q_{Gn}
	H	L	H	L	L	↑	X	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	L	Q_{Gn}
Shift Left	H	H	L	L	L	↑	H	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	H	Q_{Bn}	H
	H	H	L	L	L	↑	L	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	L	Q_{Bn}	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

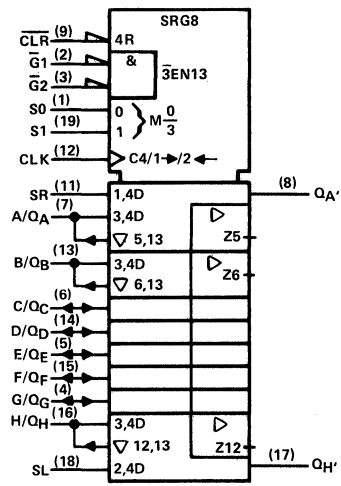
When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

logic symbols†

'ALS299, 'AS299



'ALS323, 'AS323



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

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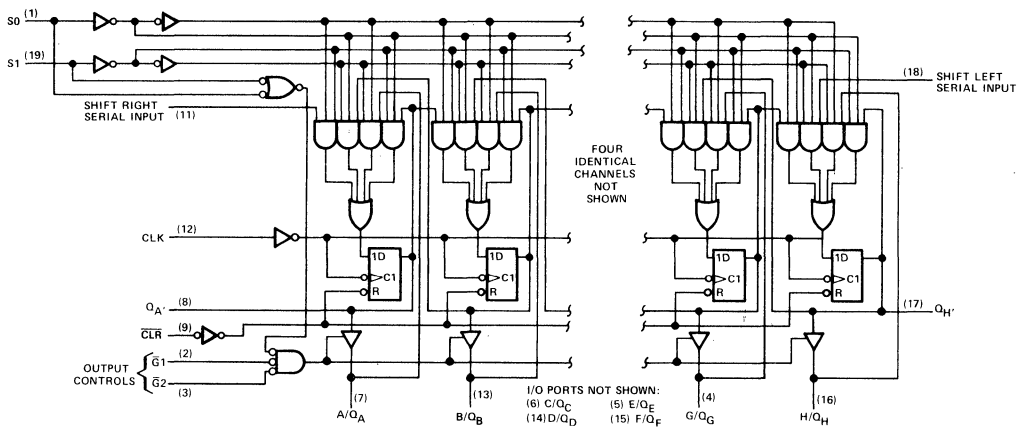
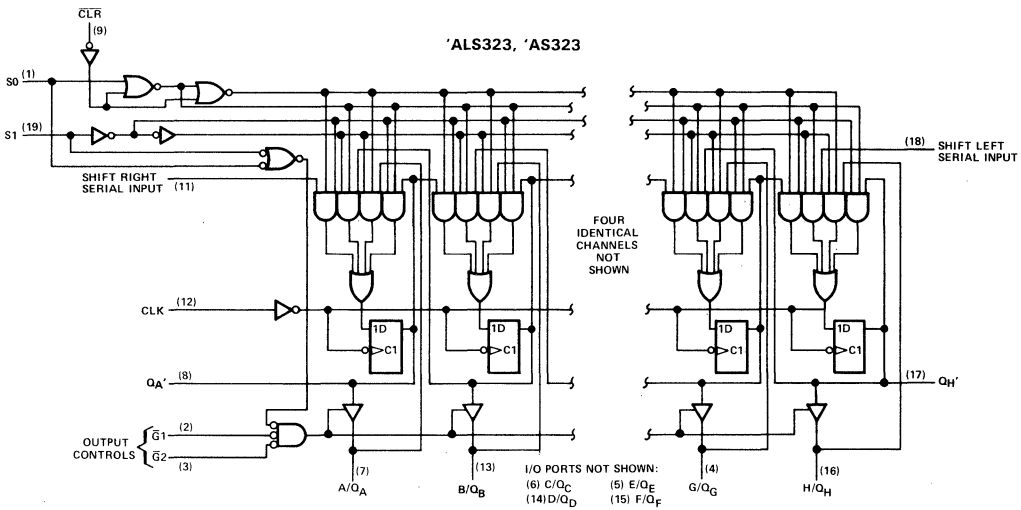
logic diagrams (positive logic)

'ALS299, 'AS299



'ALS323, 'AS323



Pin numbers shown are for DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS', SN54AS' . . . . . −55°C to 125°C
SN74ALS', SN74AS' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

				SN54ALS299 SN54ALS323			SN74ALS299 SN74ALS323			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
I_{OH}	High-level output current	$Q_{A'}$ or $Q_{H'}$				−0.4			−0.4	mA
		Q_A thru Q_H				−1			−2.6	
I_{OL}	Low-level output current	$Q_{A'}$ or $Q_{H'}$				4			8	mA
		Q_A thru Q_H				12			24	
f_{clock}	Clock frequency (at 50% duty cycle)			0		17	0		30	MHz
t_w	Pulse duration	CLK high or low		22			16.5			ns
		$\overline{CLR}$ low ('ALS299)		12			10			
t_{su}	Setup time before CLK↑	Select		25			20			ns
		Serial or Parallel data	High level	18			16			
			Low level	15			6			
		$\overline{CLR}$ inactive ('ALS299)		15			15			
		$\overline{CLR}$ active ('ALS323)		25			20			
		$\overline{CLR}$ inactive ('ALS323)		18			16			
t_h	Hold time after CLK↑	Select		0			0			ns
		Serial or parallel data		0			0			
T_A	Operating free-air temperature			−55		125	0		70°	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS299 SN54ALS323			SN74ALS299 SN74ALS323			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	All outputs	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	Q_A thru Q_H	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	$Q_{A'}$ or $Q_{H'}$	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
	Q_A thru Q_H	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	A thru H	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	mA
	Any other	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	
I_{IH}‡		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}‡	S0, S1, SR, SL	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
	All others					−0.1			−0.1	
I_O§	$Q_{A'}$, $Q_{H'}$	V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
	Q_A thru Q_H			−30		−112	−30		−112	
I_{CC}		V_{CC} = 5.5 V	Outputs high		15	28		15	28	mA
			Outputs low		22	38		22	38	
			Outputs disabled		23	40		23	40	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡For I/O ports (Q_A through Q_H), the parameters I_{IH} and I_{IL} include the off-state output current.

§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

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switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS299 SN54ALS323		SN74ALS299 SN74ALS323		
			MIN	MAX	MIN	MAX	
f_{max}			17		30		MHz
t_{PLH}	CLK	Q_A thru Q_H	2	19	4	13	ns
t_{PHL}			4	25	7	19	
t_{PLH}	CLK	Q_A' or Q_H'	2	21	5	15	ns
t_{PHL}			4	22	8	18	
t_{PHL}	$\overline{CLR}$ ('ALS299 only)	Q_A thru Q_H	6	29	6	22	ns
		Q_A' or Q_H'	6	29	6	22	
t_{PZH}	$\overline{G}1$, $\overline{G}2$	Q_A thru Q_H	5	22	6	16	ns
t_{PZL}			6	26	8	22	
t_{PZH}	S0, S1	Q_A thru Q_H	5	21	7	17	ns
t_{PZL}			6	26	8	22	
t_{PHZ}	$\overline{G}1$, $\overline{G}2$	Q_A thru Q_H	1	15	1	8	ns
t_{PLZ}			5	38	5	15	
t_{PHZ}	S0, S1	Q_A thru Q_H	1	16	1	12	ns
t_{PLZ}			8	34	8	25	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

recommended operating conditions

				SN54AS299 SN54AS323			SN74AS299 SN74AS323			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
I_{OH}	High-level output current	Q_A' or Q_H'				−2			−2	mA
		Q_A thru Q_H				−12			−15	
I_{OL}	Low-level output current	Q_A' or Q_H'				20			20	mA
		Q_A thru Q_H				32			48	
f_{clock}	Clock frequency (at 50% duty cycle)									MHz
t_w	Pulse duration	CLK high or low								ns
		$\overline{CLR}$ low ('AS299)								
t_{su}	Setup time before CLK↑	Select								ns
		Serial or Parallel data	High level							
			Low level							
		$\overline{CLR}$ inactive ('AS299)								
		$\overline{CLR}$ active ('AS323)								
		$\overline{CLR}$ inactive ('AS323)								
t_h	Hold time after CLK↑	Select								ns
		Serial or parallel data								
T_A	Operating free-air temperature			−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS299 SN54AS323			SN74AS299 SN74AS323			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	All outputs	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
	Q_A thru Q_H	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2					
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4	3.2		
V_{OL}	Q_A' or Q_H'	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.25	0.5		0.25	0.5	V
	Q_A thru Q_H	V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5				
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_I	A thru H	V_{CC} = 5.5 V,	V_I = 5.5 V							mA
	Any other	V_{CC} = 5.5 V,	V_I = 7 V							
I_{IH}‡		V_{CC} = 5.5 V,	V_I = 2.7 V							μA
I_{IL}‡		V_{CC} = 5.5 V,	V_I = 0.4 V							mA
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	Outputs high							mA
			Outputs low							
			Outputs disabled		95			95		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡For I/O ports (Q_A through Q_H), the parameters I_{IH} and I_{IL} include the off-state output current.

§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

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switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54AS299 SN54AS323			SN74AS299 SN74AS323			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}									MHz
t_{PLH}	CLK	Q_A thru Q_H			10			10	ns
t_{PHL}					10			10	
t_{PLH}	CLK	Q_A' or Q_H'			10			10	
t_{PHL}					10			10	
t_{PHL}	$\overline{CLR}$	Q_A thru Q_H			12			12	ns
		Q_A' or Q_H'			12			12	
t_{PZH}	$\overline{G}1$, $\overline{G}2$	Q_A thru Q_H			10			10	ns
t_{PZL}					10			10	
t_{PZH}	S0, S1	Q_A thru Q_H			10			10	ns
t_{PZL}					10			10	
t_{PHZ}	$\overline{G}1$, $\overline{G}2$	Q_A thru Q_H			7			7	ns
t_{PLZ}					7			7	
t_{PHZ}	S0, S1	Q_A thru Q_H			7			7	ns
t_{PLZ}					7			7	

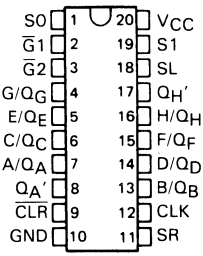
†All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH 3-STATE OUTPUTS

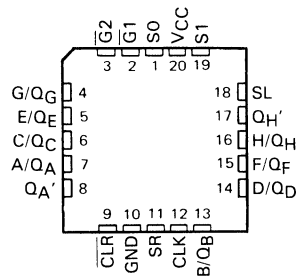
D2661, DECEMBER 1982—REVISED MAY 1986

- Multiplexed I/O Ports Provide Improved Bit Density
- Four Modes of Operation: Hold (Store), Shift Right, Shift Left, and Load Data
- Operates with Outputs Enabled or at High Impedance
- 3-State Outputs Drive Bus Lines Directly
- Can Be Cascaded for N-Bit Word Lengths
- 'ALS323 and 'AS323 Have Synchronous Clear
- Application:
  Stacked or Push-Down Registers, Buffer Storage, and Accumulator Registers
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS', SN54AS' . . . J PACKAGE
SN74ALS', SN74AS' . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS', SN54AS' . . . FK PACKAGE
(TOP VIEW)

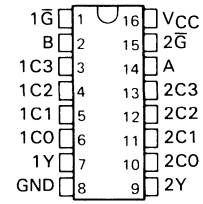


For complete information on the SN54ALS323, SN54AS323, SN74ALS323, SN74AS323, see page 2-343.

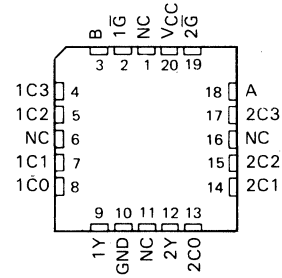
D2661, APRIL 1982—REVISED MAY 1986

- Inverting Versions of 'ALS153 and 'AS153
- Permits Multiplexing from N Lines to 1 Line
- Performs Parallel-to-Serial Conversion
- Strobe (Enable) Line Provided for Cascading (N Lines to n Lines)
- Typical 'ALS352 Power per Multiplexer . . . 16 mW
- Typical 'AS352 Average Propagation Delay Times
  Data Input to Output . . . 2.7 ns
  Strobe Input to Output . . . 4.5 ns
  Select Input to Output . . . 4.5 ns
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS352, SN54AS352 . . . J PACKAGE
SN74ALS352, SN74AS352 . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS352, SN54AS352 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

Each of these data selectors/multiplexers contains inverters and drivers to supply fully complementary binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs ($\overline{G}$) are provided for each of the two four-line sections.

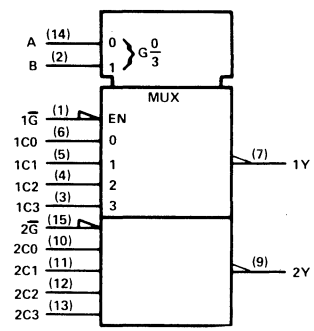
The SN54ALS352 and SN54AS352 are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS352 and SN74AS352 are characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	$\overline{G}$	Y
X	X	X	X	X	X	H	H
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
L	H	X	L	X	X	L	H
L	H	X	H	X	X	L	L
H	L	X	X	L	X	L	H
H	L	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

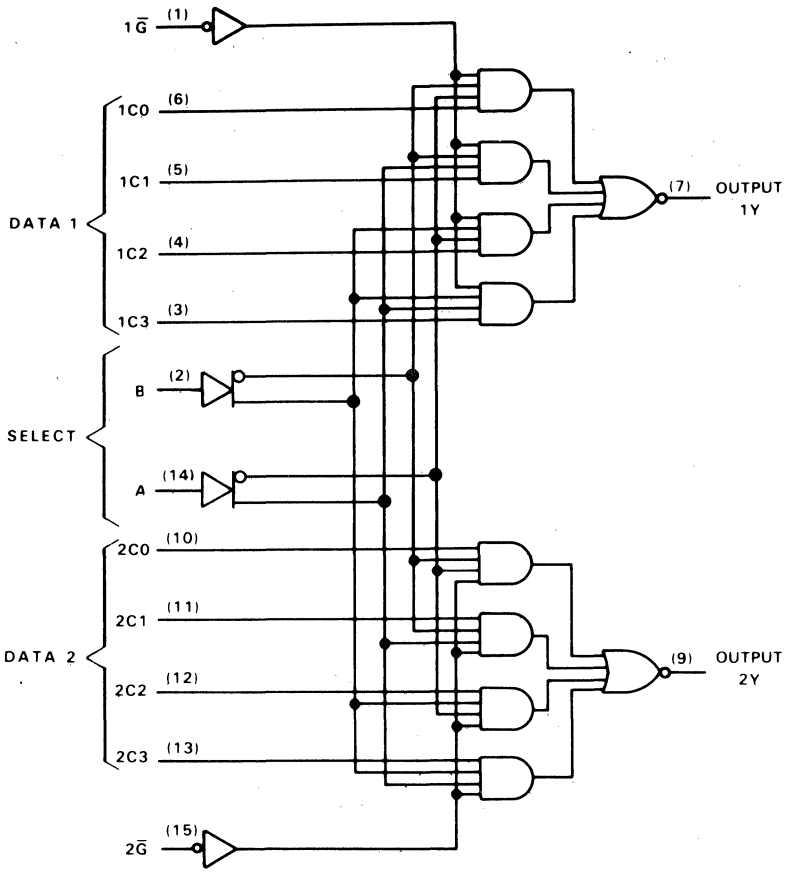
Select inputs A and B are common to both sections.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS352, SN54AS352 . . . . . −55 °C to 125 °C
SN74ALS352, SN74AS352 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS352			SN74ALS352			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS352			SN74ALS352			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V,	See Note 1		6.5	10		6.5	10	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with data and select inputs at 4.5 V, and G inputs grounded.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS352		SN74ALS352		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	5	32	5	24	ns
t_{PHL}			5	24	5	21	
t_{PLH}	Data (Any C)	Y	3	24	3	18	ns
t_{PHL}			2	15	2	13	
t_{PLH}	$\overline{G}$	Y	4	26	4	18	ns
t_{PHL}			4	24	4	20	

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

recommended operating conditions

		SN54AS352			SN74AS352			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			32			48	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS352			SN74AS352			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2					
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4	3.3		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_I	A, B	V_{CC} = 5.5 V,	V_I = 7 V			0.2			0.2	mA
	All others					0.1			0.1	
I_{IH}	A, B	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	μA
	All others					20			20	
I_{IL}	A, B	V_{CC} = 5.5 V,	V_I = 0.4 V			−1			−1	mA
	All others					−0.5			−0.5	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	Outputs high		15.5	25		15.5	25	mA
			Outputs low		17.5	28		17.5	28	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS352		SN74AS352		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	4	12.5	4	11	ns
t_{PHL}			4	14	4	13	
t_{PLH}	Data (Any C)	Y	2	7.5	2	6.5	ns
t_{PHL}			2	7	2	6	
t_{PLH}	$\overline{G}$	Y	3	8	3	7	ns
t_{PHL}			4	13.5	4	12	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

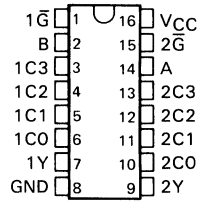
TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SN54ALS353, SN54AS353A, SN74ALS353, SN74AS353A
DUAL 1-OF-4 DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

D2661, APRIL 1982—REVISED MAY 1986

- Inverting Versions of 'ALS253 and 'AS253
- Permits Multiplexing from N Lines to 1 Line
- Performs Parallel-to-Serial Conversion
- Typical 'ALS353 Power per Multiplexer . . . 20 mW
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS353, SN54AS353A . . . J PACKAGE
SN74ALS353, SN74AS353A . . . D OR N PACKAGE
(TOP VIEW)



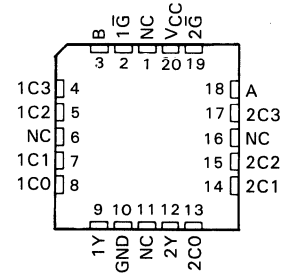
description

Each of these data selectors/multiplexers contains inverters and drivers to supply full binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs ($\overline{G}$) are provided for each of the two four-line sections.

The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low-impedance of the single enabled output will drive the bus line to a high or low logic level. Each output has its own strobe ($\overline{G}$). The output is disabled when its strobe is high.

The SN54ALS353 and SN54AS353A are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS353 and SN74AS353A are characterized for operation from 0°C to 70°C.

SN54ALS353, SN54AS353A . . . FK PACKAGE
(TOP VIEW)



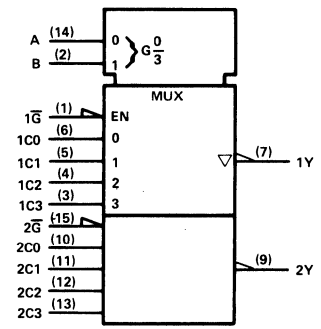
NC—No internal connection

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT CONTROL	OUTPUT
B	A	C0	C1	C2	C3	$\overline{G}$	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
L	H	X	L	X	X	L	H
L	H	X	H	X	X	L	L
H	L	X	X	L	X	L	H
H	L	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

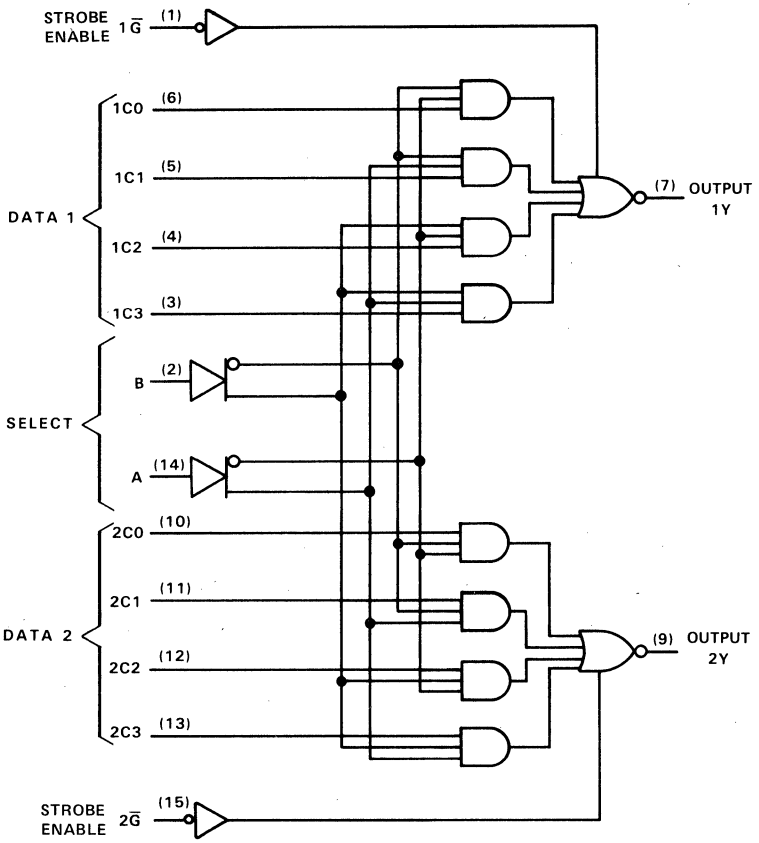
Select inputs A and B are common to both sections.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS353, SN54AS353A . . . . . −55 °C to 125 °C
SN74ALS353, SN74AS353A . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS353			SN74ALS353			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS353			SN74ALS353			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V,			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	disabled	V_{CC} = 5.5 V,	All inputs, at 4.5 V		8	13		8	13	mA
	enabled		All inputs at Gnd		7	12		7	12	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS353		SN74ALS353		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	5	32	5	24	ns
t_{PHL}			5	24	5	21	
t_{PLH}	Data (Any C)	Y	4	24	4	18	ns
t_{PHL}			3	15	3	13	
t_{PZH}	$\overline{G}$	Y	3	18	3	13	ns
t_{PZL}			3	20	2	16	
t_{PHZ}	$\overline{G}$	Y	2	12	2	10	ns
t_{PLZ}			2	22	2	14	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

recommended operating conditions

		SN54AS353A			SN74AS353A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			32			48	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS353A			SN74AS353A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2					
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4	3.3		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V,			−50			−50	μA
I_I	A, B	V_{CC} = 5.5 V,	V_I = 7 V			0.2			0.2	mA
	All others					0.1			0.1	
I_{IH}	A, B	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	μA
	All others					20			20	
I_{IL}	A, B	V_{CC} = 5.5 V,	V_I = 0.4 V			−1			−1	mA
	All others					−0.5			−0.5	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	Outputs high		15	24		15	24	mA
			Outputs low		19	31		19	31	
			Outputs disabled		18	30		18	30	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS353A		SN74AS353A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	3	10	3	9	ns
t_{PHL}			4	14	4	12	
t_{PLH}	Data (Any C)	Y	3	8.5	3	7.5	ns
t_{PHL}			2	6.5	2	6	
t_{PZH}	Strobe	Y	3	8.5	3	7.5	ns
t_{PZL}			4	13.5	4	12.5	
t_{PHZ}	Strobe	Y	2	6.5	2	5.5	ns
t_{PLZ}			3	9	3	7.5	

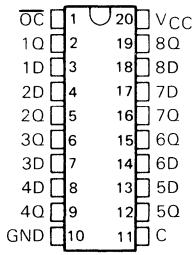
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

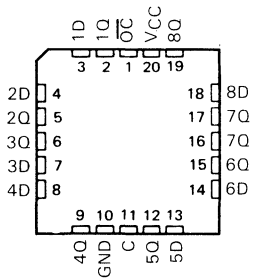
D2661, APRIL 1982—REVISED MAY 1986

- **8 Latches in a Single Package**
- **3-State Bus-Driving True Outputs**
- **Full Parallel Access for Loading**
- **Buffered Control Inputs**
- **P-N-P Inputs Reduce D-C Loading on Data Lines**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS373, SN54AS373 . . . J PACKAGE
SN74ALS373, SN74AS373 . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS373, SN54AS373 . . . FK PACKAGE
(TOP VIEW)



description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'ALS373 and 'AS373 are transparent D-type latches. While the enable (C) is high the Q outputs will follow the data (D) inputs. When the enable is taken low, the Q outputs will be latched at the levels that were set up at the D inputs.

A buffered output-control input ($\overline{OC}$) can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

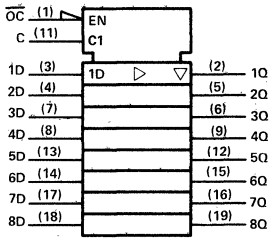
The output control $\overline{OC}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

The SN54ALS373 and SN54AS373 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS373 and SN74AS373 are characterized for operation from 0°C to 70°C.

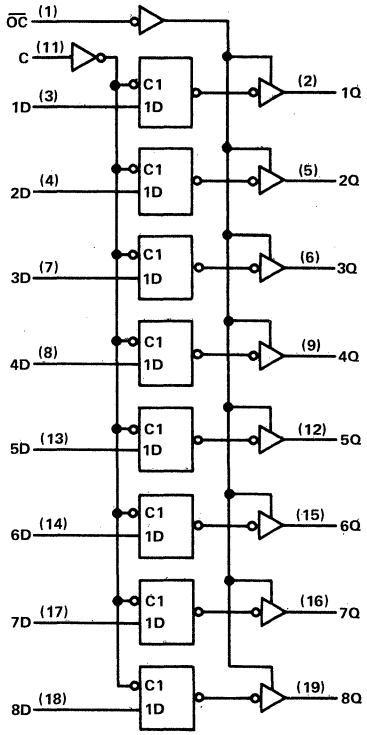
FUNCTION TABLE (EACH LATCH)

INPUTS			OUTPUT
$\overline{OC}$	ENABLE C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



logic diagram (positive logic)



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

absolute maximum ratings over free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS373, SN54AS373 . . . . . −55°C to 125°C
SN74ALS373, SN74AS373 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS373			SN74ALS373			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
t_w	Pulse duration, enable C high	10			10			ns
t_{su}	Setup time, data before enable C↓	10			10			ns
t_h	Hold time, data after enable C↓	7			7			ns
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS373			SN74ALS373			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		9	16		9	16	mA
		Outputs low		16	25		16	25	
		Outputs disabled		17	27		17	27	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS373		SN74ALS373		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	2	17	2	12	ns
t_{PHL}			1	19	4	16	
t_{PLH}	C	Any Q	6	29	6	22	ns
t_{PHL}			1	27	7	23	
t_{PZH}	$\overline{OC}$	Any Q	3	33	6	18	ns
t_{PZL}			3	24	5	20	
t_{PHZ}	$\overline{OC}$	Any Q	2	24	2	10	ns
t_{PLZ}			2	16	2	12	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
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recommended operating conditions

		SN54AS373			SN74AS373			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			32			48	mA
t_w	Pulse duration, enable C high	5.5			4.5			ns
t_{su}	Setup time, data before enable C↓	2			2			ns
t_h	Hold time, data after enable C↓	3			3			ns
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS373			SN74AS373			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC} − 2			V_{CC} − 2			V
	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2					
	V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4	3.3		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.27	0.5				V
	V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.32	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−50			−50	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V		−0.02	−0.5		−0.02	−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		55	90		55	90	mA
		Outputs low		55	85		55	85	
		Outputs disabled		65	100		65	100	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS373		SN74AS373		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	3	8	3.5	6	ns
t_{PHL}			3	7	3.5	6	
t_{PLH}	C	Any Q	6.5	14	6.5	11.5	ns
t_{PHL}			5	8	5	7.5	
t_{PZH}	$\overline{OC}$	Any Q	2	7.5	2	6.5	ns
t_{PZL}			4.5	10.5	4.5	9.5	
t_{PHZ}	$\overline{OC}$	Any Q	3	7.5	3	6.5	ns
t_{PLZ}			3	8	3	7	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

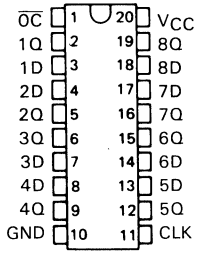
TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SN54ALS374, SN54AS374, SN74ALS374, SN74AS374
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

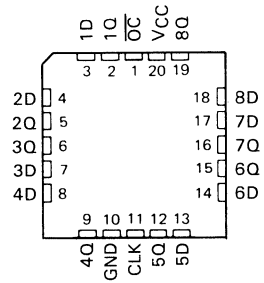
D2661, APRIL 1982 REVISED MAY 1986

- D-Type Flip-Flops In a Single Package
- 3-State Bus-Driving True Outputs
- Full Parallel Access for Loading
- Buffered Control Inputs
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS374, SN54AS374 . . . J PACKAGE
SN74ALS374, SN74AS374 . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS374, SN54AS374 . . . FK PACKAGE
(TOP VIEW)



description

These 8-bit flip-flops feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the 'ALS374 and 'AS374 are edge-triggered D-type flip-flops. On the positive transition of the clock the Q outputs will be set to the logic levels that were set up at the D inputs.

A buffered output-control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

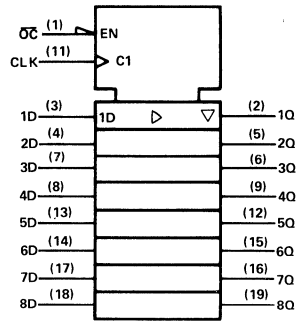
The output control ($\overline{OC}$) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54ALS374 and SN54AS374 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS374 and SN74AS374 are characterized for operation from 0°C to 70°C.

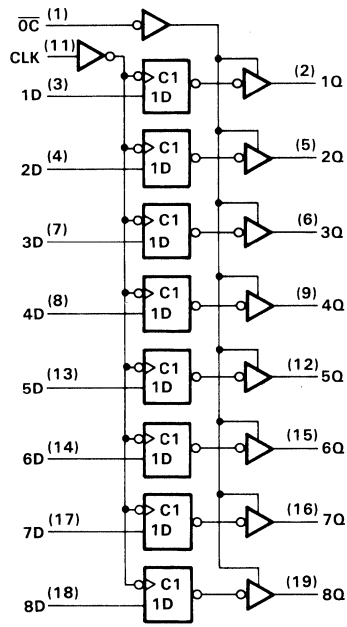
FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS			OUTPUT
$\overline{OC}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



logic diagram (positive logic)



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS374, SN54AS374 . . . . . −55 °C to 125 °C
SN74ALS374, SN74AS374 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

			SN54ALS374			SN74ALS374			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	high-level output current				−1			−2.6	mA
I_{OL}	Low-level output current				12			24	mA
f_{clock}	Clock frequency		0		30	0		35	MHz
t_w	Pulse duration	CLK high	16.5			14			ns
		CLK low	16.5			14			
t_{su}	Setup time, data before CLK↑		10			10			ns
t_h	Hold time, data after CLK↑		4			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS374			SN74ALS374			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		11	19		11	19	mA
		Outputs low		19	28		19	28	
		Outputs disabled		20	31		20	31	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

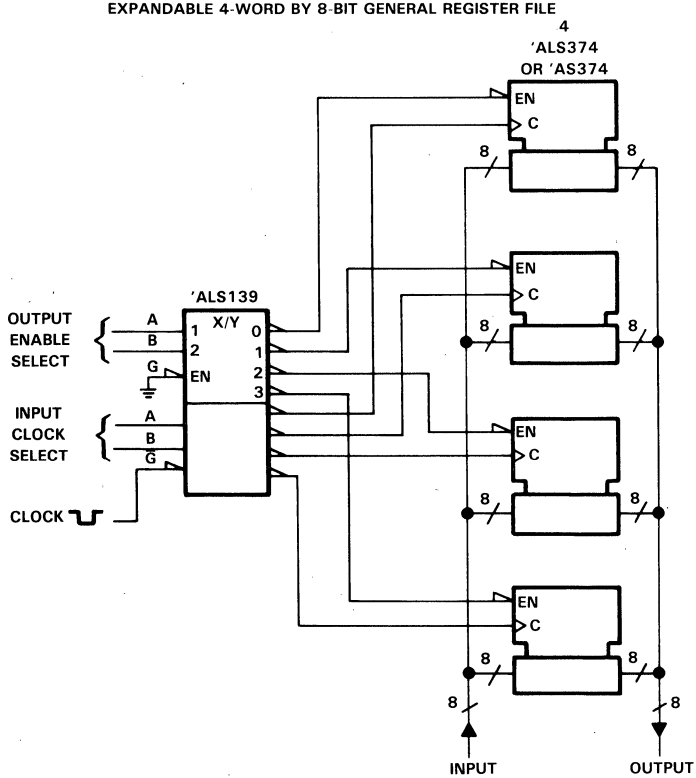
switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS374		SN74ALS374		
			MIN	MAX	MIN	MAX	
f_{max}			30		35		MHz
t_{PLH}	CLK	Q	3	21	3	12	ns
t_{PHL}			5	19	5	16	
t_{PZH}	$\overline{OC}$	Q	5	27	5	17	ns
t_{PZL}			6	23	7	18	
t_{PHZ}	$\overline{OC}$	Q	2	12	2	10	ns
t_{PLZ}			3	33	3	18	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TYPICAL APPLICATION DATA

EXPANDABLE 4-WORD BY 8-BIT GENERAL REGISTER FILE



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

recommended operating conditions

			SN54AS374			SN74AS374			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−12			−15	mA
I_{OL}	Low-level output current				32			48	mA
f_{clock}	Clock frequency		0		100	0		125	MHz
t_w	Pulse duration	CLK high	5.5			4			ns
		CLK low	5			3			
t_{su}	Setup time data before CLK↑		3			2			ns
t_h	Hold time, data after CLK↑		3			2			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS374			SN74AS374			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2					
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4	3.3		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.29	0.5				V
		V_{CC} = 4.5 V	I_{OL} = 48 mA					0.34	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	OC, CLK	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	Data					−3			−2	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	Outputs high		77	120		77	120	mA
			Outputs low		84	128		84	128	
			Outputs disabled		84	128		84	128	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

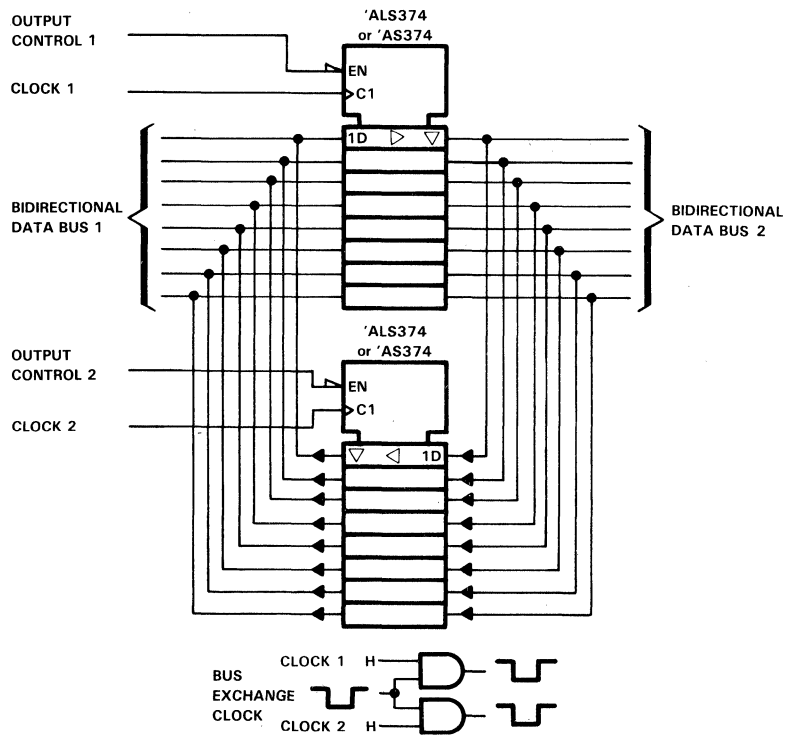
switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS374		SN74AS374		
			MIN	MAX	MIN	MAX	
f_{max}			100		125		MHz
t_{PLH}	CLK	Q	3	11	3	8	ns
t_{PHL}			4	11.5	4	9	
t_{PZH}	$\overline{OC}$	Q	2	7	2	6	ns
t_{PZL}			3	11	3	10	
t_{PHZ}	$\overline{OC}$	Q	2	7	2	6	ns
t_{PLZ}			2	7	2	6	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TYPICAL APPLICATION DATA

BIDIRECTIONAL BUS DRIVER



CLOCK CIRCUIT FOR BUS EXCHANGE

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

D2661, APRIL 1982 – REVISED MAY 1986

- **Mechanically and Functionally Interchangeable with DM71/81LS97 and DM71/81LS98**
- **P-N-P Inputs Reduce Bus Loading**
- **3-State Outputs Rated at I_{OL} of 12 mA and 24 mA for SN54ALS' and SN74ALS', Respectively**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

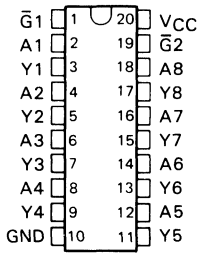
DEVICE	DATA PATH
'ALS465A	True
'ALS466A	Inverting
'ALS467A	True
'ALS468A	Inverting

description

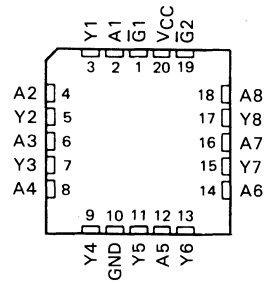
These octal buffers utilize the latest advanced low-power Schottky technology. The 'ALS465A and 'ALS466A have a two-input active-low AND enable gate controlling all eight data buffers. The 'ALS467A and 'ALS468A have two separate active-low enable inputs each controlling four data buffers. In each case, a high level on any $\overline{G}$ places the affected outputs at high impedance.

The SN54ALS465A, SN54ALS466A, SN54ALS467A, and SN54ALS468A are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS465A, SN74ALS466A, SN74ALS467A, and SN74ALS468A are characterized for operation from 0°C to 70°C.

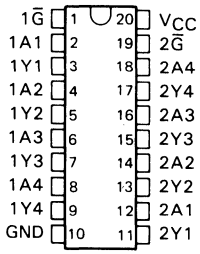
SN54ALS465A, SN54ALS466A . . . J PACKAGE
SN74ALS465A, SN74ALS466A . . . DW OR N PACKAGE
(TOP VIEW)



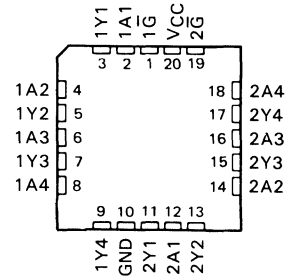
SN54ALS465A, SN54ALS466A . . . FK PACKAGE
(TOP VIEW)



SN54ALS467A, SN54ALS468A . . . J PACKAGE
SN74ALS467A, SN74ALS468A . . . DW OR N PACKAGE
(TOP VIEW)

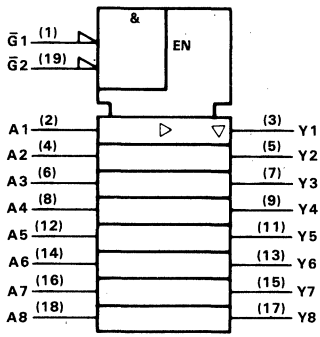


SN54ALS467A, SN54ALS468A . . . FK PACKAGE
(TOP VIEW)

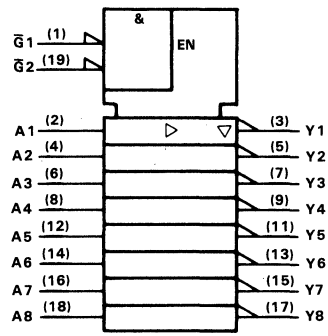


logic symbols†

'ALS465A

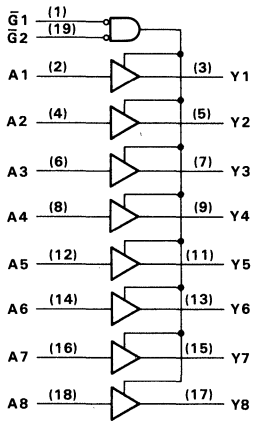


'ALS466A

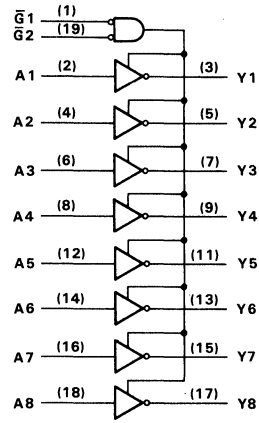


logic diagrams (positive logic)

'ALS465A

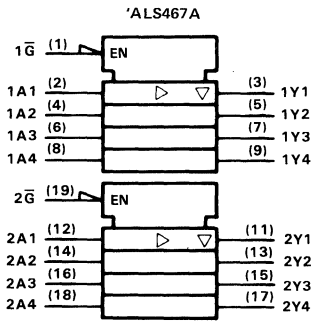


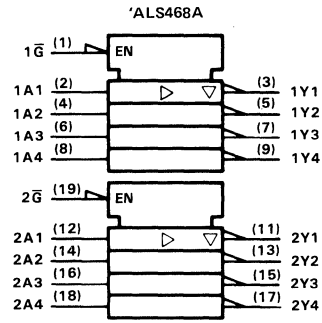
'ALS466A



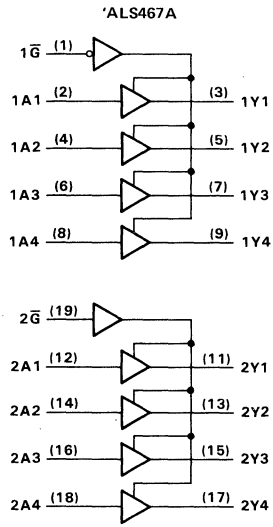
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

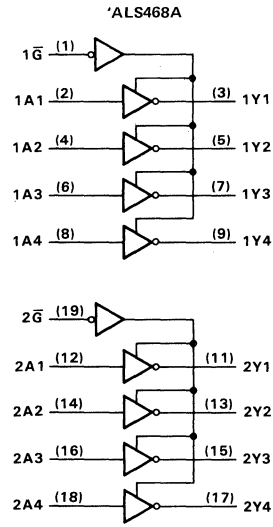
logic symbols†





logic diagrams (positive logic)





†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS465A THRU SN54ALS468A . . . . . −55°C to 125°C
SN74ALS465A THRU SN74ALS468A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS465A THRU SN54ALS468A			SN74ALS465A THRU SN74ALS468A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
							48†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limit applies only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48 mA limit applies for SN74ALS465A-1, SN74ALS466A-1, SN74ALS467A-1, and SN74ALS468A-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS465A THRU SN54ALS468A			SN74ALS465A THRU SN74ALS468A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, (I_{OL} = 48 mA for −1 versions)	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS465A 'ALS467A	V_{CC} = 5.5 V	Outputs high		11	21		11	16	mA
			Outputs low		19	33		19	28	
			Outputs disabled		23	38		23	33	
	'ALS466A 'ALS468A	V_{CC} = 5.5 V	Outputs high		7	15		7	10	mA
			Outputs low		16	29		16	24	
			Outputs disabled		19	32		19	27	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

'ALS465A, 'ALS467A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS465A SN54ALS467A		SN74ALS465A SN74ALS467A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	2	16	2	13	ns
t_{PHL}			4	15	4	12	
t_{PZH}	$\overline{G}$	Any Y	4	27	4	23	ns
t_{PZL}			5	30	5	25	
t_{PHZ}	$\overline{G}$	Any Y	2	12	2	10	ns
t_{PLZ}			3	21	3	18	

'ALS466A, 'ALS468A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS466A SN54ALS468A		SN74ALS466A SN74ALS468A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	3	14	3	12	ns
t_{PHL}			2	11	2	9	
t_{PZH}	$\overline{G}$	Any Y	4	21	4	16	ns
t_{PZL}			7	25	7	23	
t_{PHZ}	$\overline{G}$	Any Y	2	12	2	10	ns
t_{PLZ}			2	20	2	17	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

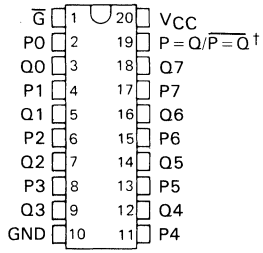
D2661, JUNE 1982 – REVISED MAY 1986

- **Compares Two 8-Bit Words**
- **Choice of Totem-Pole or Open-Collector Outputs**
- **'ALS518, 'ALS520, and 'ALS522 Have 20-kΩ Pull-up Resistors on Q Inputs**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

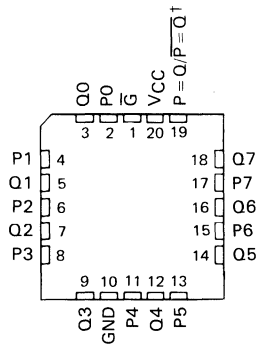
TYPE	INPUT PULL-UP RESISTOR	OUTPUT FUNCTION AND CONFIGURATION
'ALS518	Yes	P = Q open-collector
'ALS519	No	P = Q open-collector
'ALS520	Yes	$\overline{P=Q}$ totem-pole
'ALS521†	No	$\overline{P=Q}$ totem-pole
'ALS522	Yes	$\overline{P=Q}$ open-collector

†'ALS521 is identical to 'ALS688

SN54ALS' . . . J PACKAGE
SN74ALS' . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS' . . . FK PACKAGE
(TOP VIEW)



† P = Q for 'ALS518 and 'ALS519, and $\overline{P=Q}$ for 'ALS520, 'ALS521, and 'ALS522.

description

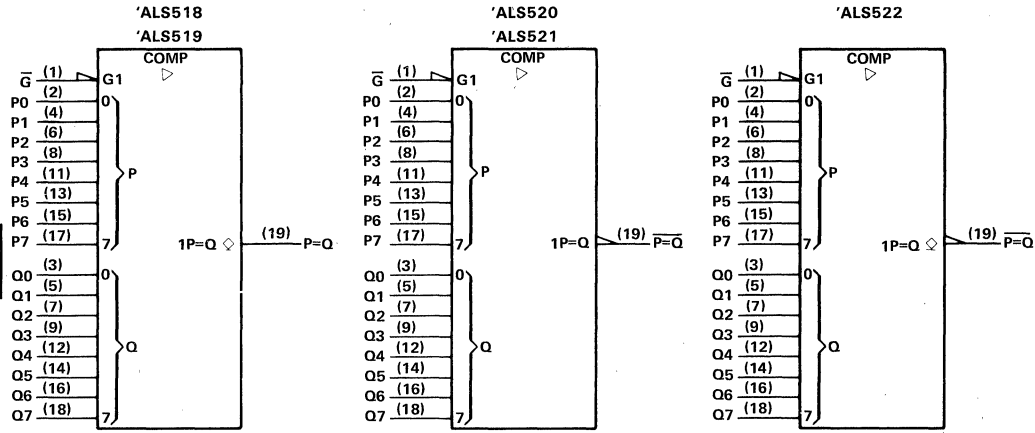
These identity comparators perform comparisons on two eight-bit binary or BCD words. The 'ALS518 and 'ALS519 provide P = Q outputs, while the 'ALS520, 'ALS521, and 'ALS522 provide $\overline{P=Q}$ outputs. The 'ALS518, 'ALS519, and 'ALS522 have open-collector outputs. The 'ALS518, 'ALS520, and 'ALS522 feature 20-kΩ pull-up termination resistors on the Q inputs for analog or switch data.

The SN54ALS518 through SN54ALS522 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS518 through SN74ALS522 are characterized for operation from 0°C to 70°C.

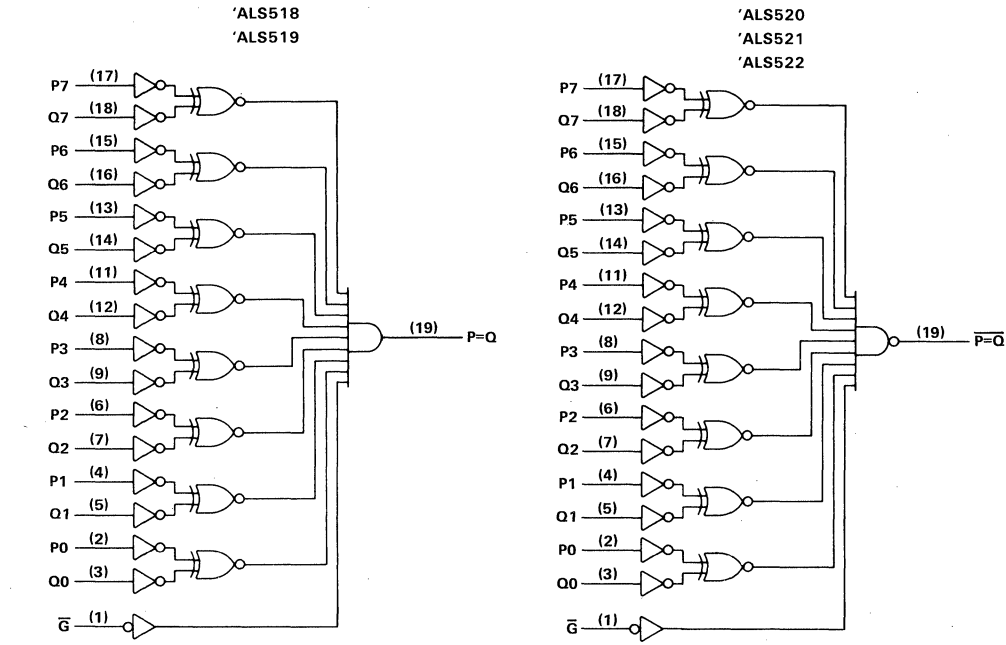
FUNCTION TABLE

INPUTS		OUTPUTS	
DATA P, Q	ENABLE G	P = Q	$\overline{P=Q}$
P = Q	L	H	L
P > Q	L	L	H
P < Q	L	L	H
X	H	L	H

logic symbols†



logic diagrams (positive logic)



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: Q inputs of 'ALS518, 'ALS522 . . . . . V_{CC} + 0.5 V or 5.5 V, whichever is less
All other inputs . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS518, SN54ALS519, SN54ALS522 . . . . . −55 °C to 125 °C
SN74ALS518, SN74ALS519, SN74ALS522 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS518 SN54ALS519 SN54ALS522			SN74ALS518 SN74ALS519 SN74ALS522			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS518 SN54ALS519 SN54ALS522			SN74ALS518 SN74ALS519 SN74ALS522			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}		V_{CC} = 5.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	'ALS518, 'ALS522 Q inputs	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	mA
	All other inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	
I_{IH}	'ALS518, 'ALS522 Q inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			−0.2			−0.2	mA
	All other inputs					20			20	μA
I_{IL}	'ALS518, 'ALS522 Q inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.6			−0.6	mA
	All other inputs					−0.1			−0.1	
I_{CC}	'ALS518	V_{CC} = 5.5 V,	See Note 1		11	17		11	17	mA
	'ALS519				11	17		11	17	
	'ALS522				11	17		11	17	

†All typical values are at V_{CC} = 5 V, T_A = 25 °C.
NOTE 1: I_{CC} is measured with $\overline{G}$ grounded, P and Q at 4.5 V.

'ALS518, 'ALS519 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX				UNIT
			SN54ALS518 SN54ALS519		SN74ALS518 SN74ALS519		
			MIN	MAX	MIN	MAX	
t_{PLH}	P or Q	P=Q	15	37	15	33	ns
t_{PHL}			3	18	3	15	
t_{PLH}	$\overline{G}$	P=Q	15	37	15	33	ns
t_{PHL}			3	18	3	15	

'ALS522 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX				UNIT
			SN54ALS522		SN74ALS522		
			MIN	MAX	MIN	MAX	
t_{PLH}	P or Q	$\overline{P=Q}$	10	30	10	25	ns
t_{PHL}			5	25	5	23	
t_{PLH}	$\overline{G}$	$\overline{P=Q}$	8	30	8	25	ns
t_{PHL}			8	30	8	23	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: Q inputs of 'ALS520 . . . . . V_{CC} + 0.5 V or 5.5 V, whichever is less
All other inputs . . . . . 7 V
Operating free-air temperature range: SN54ALS520, SN54ALS521 . . . . . −55°C to 125°C
SN74ALS520, SN74ALS521 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS520 SN54ALS521			SN74ALS520 SN74ALS521			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS520 SN54ALS521			SN74ALS520 SN74ALS521			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_I	'ALS520 Q inputs	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	mA
	All other inputs	V_{CC} = 5.5 V	V_I = 7 V			0.1			0.1	
I_{IH}	'ALS520 Q inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			−0.2			−0.2	mA
	All other inputs					20			20	μA
I_{IL}	'ALS520 Q inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.6			−0.6	mA
	All other inputs					−0.1			−0.1	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS520	V_{CC} = 5.5 V,	See Note 1		12	19		12	19	mA
	'ALS521				12	19		12	19	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with $\overline{G}$ grounded and P and Q inputs at 4.5 V.

'ALS520, 'ALS521 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS520 SN54ALS521		SN74ALS520 SN74ALS521		
			MIN	MAX	MIN	MAX	
t_{PLH}	P or Q	$\overline{P=Q}$	3	19	3	12	ns
t_{PHL}			3	25	5	20	
t_{PLH}	$\overline{G}$	$\overline{P=Q}$	2	18	2	12	ns
t_{PHL}			5	23	5	22	

NOTE 1. Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

FUSE-PROGRAMMABLE IDENTITY COMPARATORS

D2826, JUNE 1984 – REVISED MAY 1986

- Can Be Programmed and Verified on Most Incoming Test Equipment
- Reduces Board and Package Size for Similar Fixed Comparator Functions
- High-Speed Address Recognition
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

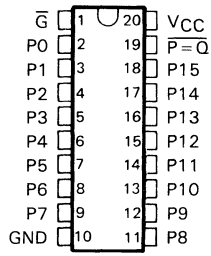
Programming Capabilities

'ALS526 – Fuse Programmable 16-Bit Identity Comparator

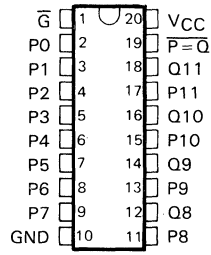
'ALS527 – Fuse Programmable 8-Bit Identity Comparator and 4-Bit Comparator

'ALS528 – Fuse Programmable 12-Bit Identity Comparator

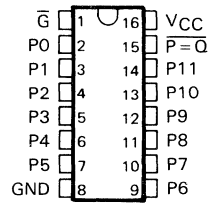
SN54ALS526 . . . J PACKAGE
SN74ALS526 . . . DW OR N PACKAGE
(TOP VIEW)



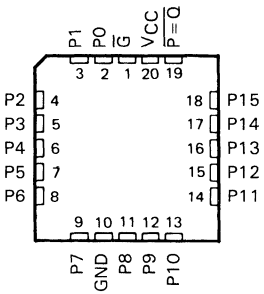
SN54ALS527 . . . J PACKAGE
SN74ALS527 . . . DW OR N PACKAGE
(TOP VIEW)



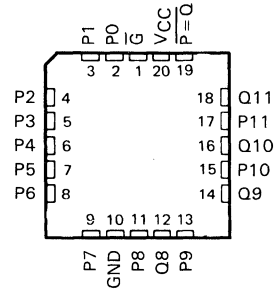
SN54ALS528 . . . J PACKAGE
SN54ALS528 . . . DW OR N PACKAGE
(TOP VIEW)



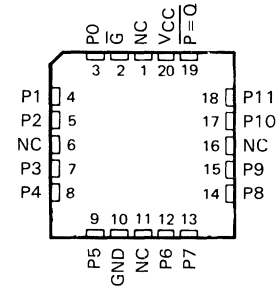
SN54ALS526 . . . FK PACKAGE
(TOP VIEW)



SN54ALS527 . . . FK PACKAGE
(TOP VIEW)



SN54ALS528 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

The 'ALS526 and 'ALS528 are fuse-programmable identity comparators designed for easy programming in fixed-comparator applications. The 'ALS526 compares a 16-bit data word against a preprogrammed 16-bit data word while the 'ALS528 compares a 12-bit data word against a preprogrammed 12-bit data word. The $\overline{P=Q}$ output will go low when the applied data word (P inputs) matches the preprogrammed data word (Q represents the preprogrammed data word). Programming is easily accomplished on the bench or with conventional automatic test equipment. Special equipment such as PROM-programmers are not required.

The 'ALS527 is a combination of an 8-bit fuse-programmable comparator and a conventional 4-bit comparator. For the $\overline{P=Q}$ output to go low, the applied data word P0 through P7 must match the preprogrammed data word Q0 through Q7, and the applied data word P8 through P11 must match the applied data word Q8 through Q11.

The SN54ALS526, SN54ALS527, and SN54ALS528 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS526, SN74ALS527, and SN74ALS528 are characterized for operation from 0°C to 70°C.

programming procedure

Before any fuses are blown, the inputs will recognize a low logic level. Therefore, only the bits that are to recognize a high logic level require programming. A fuse is blown by applying 12 volts (V_{IHH}) to the desired P input and also to the $\overline{G}$ input. This permanently programs the pin to recognize a high. Only one input pin should be programmed at a time.

Step 1. Take $\overline{G}$ to V_{IL} and apply V_{IH} to all P inputs†.
Step 2. Take desired P input to V_{IHH}, output will be low if the fuse is intact.
Step 3. Pulse $\overline{G}$ to V_{IHH}. After $\overline{G}$ has returned to V_{IL}, the output will be high indicating that the fuse is blown.
Step 4. Take P input back to V_{IH}. Repeat steps 2 through 4 to program additional inputs.

verification procedure

These devices can be checked to determine which fuses if any are blown. Figure 1 shows how verification can be accomplished during programming.

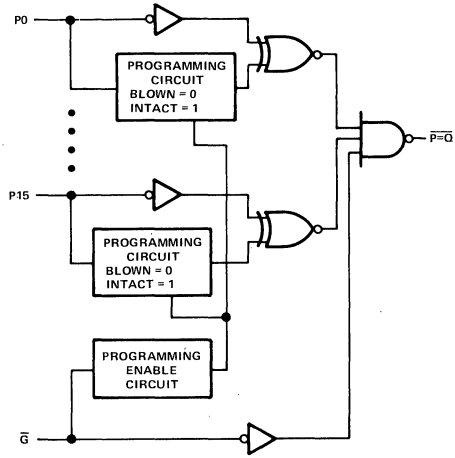
Step 1. Take $\overline{G}$ and all P inputs† to V_{IL}. If the output is low, all fuses are intact.
Step 2. Take all P inputs† to V_{IH}. The output should be high except when all fuses are blown. If all fuses are blown then the output will be low.
Step 3. Take test input to V_{IHH}, leaving other inputs at V_{IH}. If the output goes low, the fuse is intact. If the output goes high, the fuse is blown.
Step 4. Take test input back to V_{IH}. Repeat steps 3 and 4 to test additional inputs.

†For the 'ALS527, P8 through P11 inputs must match the Q8 through Q11 inputs.

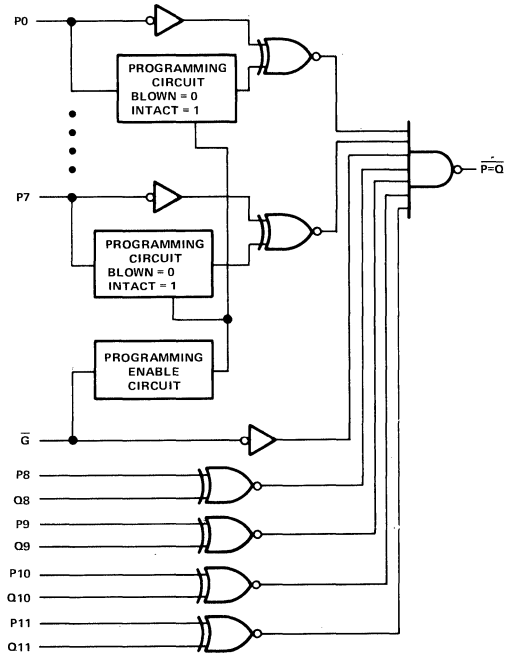
TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

logic diagrams (positive logic)

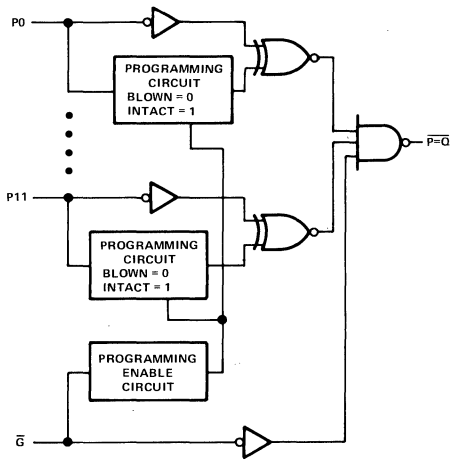
'ALS526



'ALS527

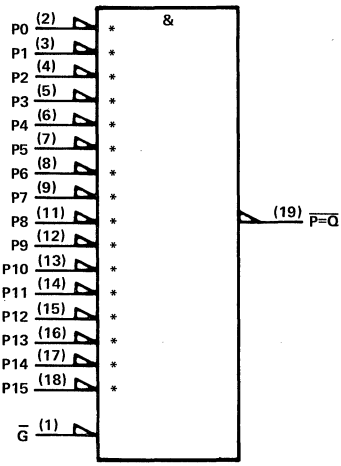


'ALS528

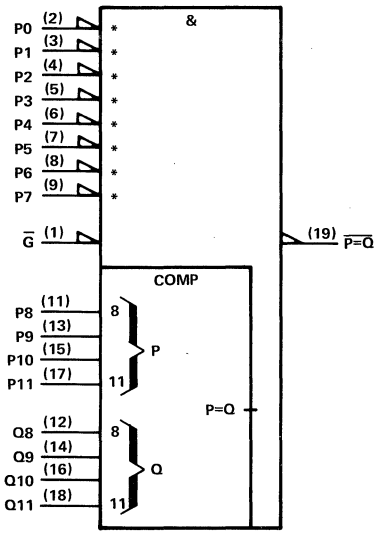


logic symbols†

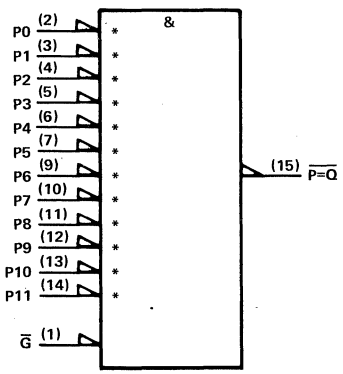
'ALS526



'ALS527



'ALS528



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.
*These inputs can be programmed to be active high. The asterisk is not a part of the symbol. For a correct symbol for the programmed device, delete the polarity symbol (▷) at any input whose programming fuse has been blown.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: SN54ALS' . . . . . −55°C to 125°C
SN74ALS' . . . . . 0°CC to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

		SN54ALS'			SN74ALS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2		5.5	2		5.5	V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS'			SN74ALS'			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	2.9		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.36	0.5	
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_{IL} = 0.4 V			−0.2			−0.2	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−130	−30		−130	mA
I_{CC}	'ALS526	V_{CC} = 5.5 V,	All inputs at 4.5 V		16	27		16	27	mA
	'ALS527				15	24		15	24	
	'ALS528				13	21		13	21	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximtes one half of the true short-circuit output current, I_{OS}.

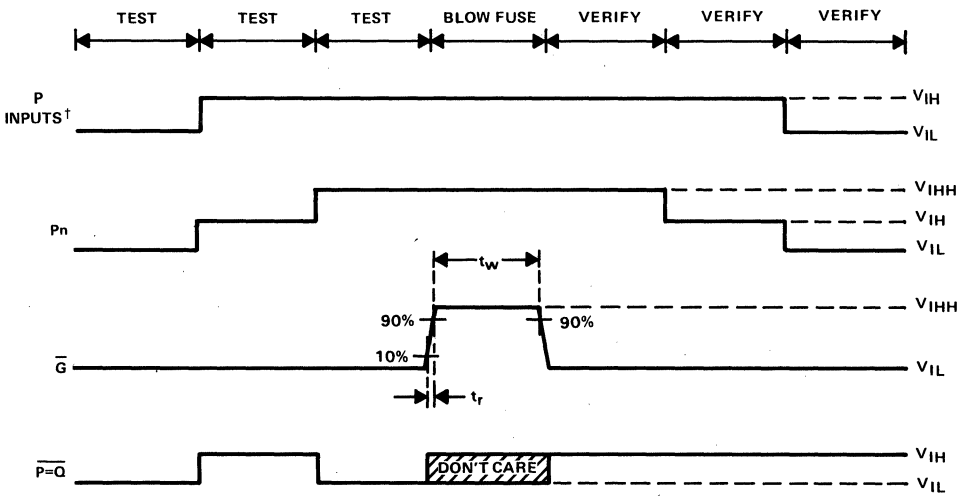
switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS'		SN74ALS'		
			MIN	MAX	MIN	MAX	
t_{PLH}	P or Q	$\overline{P=Q}$	3	18	3	15	ns
t_{PHL}			2	15	2	12	
t_{PLH}	$\overline{G}$	$\overline{P=Q}$	2	18	2	15	ns
t_{PHL}			2	15	2	12	

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

programming parameters

PARAMETER			MIN	MAX	UNIT
V_{IH}	High-level input voltage		2	5.5	V
V_{IL}	Low-level input voltage			0.8	V
V_{IHH}	Program-pulse input voltage		11.5	12.5	V
V_{CC}	Supply voltage		6.5	7.5	V
I_{IHH}	Program-pulse input current	Pn ($\overline{G}$ low)		10	mA
		$\overline{G}$		1.24	
I_{CCHH}	Supply current with V_{IHH} applied	'ALS526		31	mA
		'ALS527		29	
		'ALS528		26	
t_w	Pulse duration, program		10	50	μs
t_r	Rise time, program voltage			10	μs



Illustrated above is the following sequence:

NOTES: A. It is desired to program a particular input to recognize a high level input. With $\overline{G}$ low and all P inputs† at V_{IL}, the output is low if no fuses are blown.
B. With $\overline{G}$ low all P inputs† at V_{IH}, the output is high unless all fuses are blown.
C. The desired input is taken to V_{IHH}, the output goes low if the fuse is intact.
D. $\overline{G}$ is pulsed to V_{IHH} blowing the desired fuse.
E. After $\overline{G}$ is low output will be high indicating that the fuse is blown.
F. The programmed input returns to V_{IH}, the output is high unless all fuses have been blown.
G. All P inputs† are taken to V_{IL}, the output is high if a fuse has been blown.

†For the 'ALS527, P8 through P11 inputs must match the Q8 through Q11 inputs.

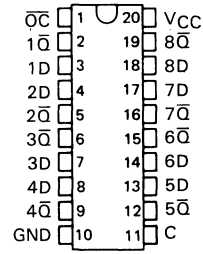
FIGURE 1. PROGRAMMING WAVEFORMS

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

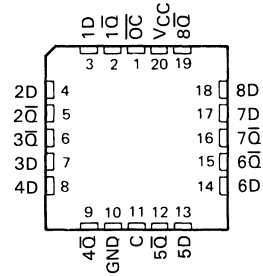
D2661, APRIL 1982 – REVISED MAY 1986

- 8-Latches In a Single Package
- 3-State Bus-Driving Inverting Outputs
- Full Parallel Access for Loading
- Buffered Control Inputs
- P-N-P Inputs Reduce D-C Loading on Data Lines
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS533, SN54AS533 . . . J PACKAGE
SN74ALS533, SN74AS533 . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS533, SN54AS533 . . . FK PACKAGE
(TOP VIEW)



description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'ALS533 and 'AS533 are transparent D-type latches. While the enable (C) is high, the $\overline{Q}$ outputs will follow the complements of the D inputs. When the enable is taken low, the $\overline{Q}$ outputs will be latched at the inverses of the levels that were set up at the D inputs. The 'ALS533 and 'AS533 are functionally equivalent to the 'ALS373 and 'AS373 except for having inverted outputs.

A buffered output-control ($\overline{OC}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

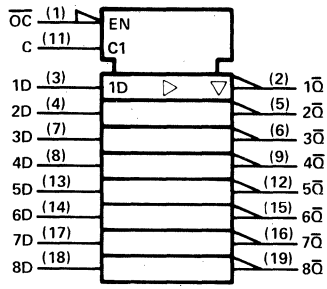
The output control does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are off.

The SN54ALS533 and SN54AS533 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS533 and SN74AS533 are characterized for operation from 0°C to 70°C.

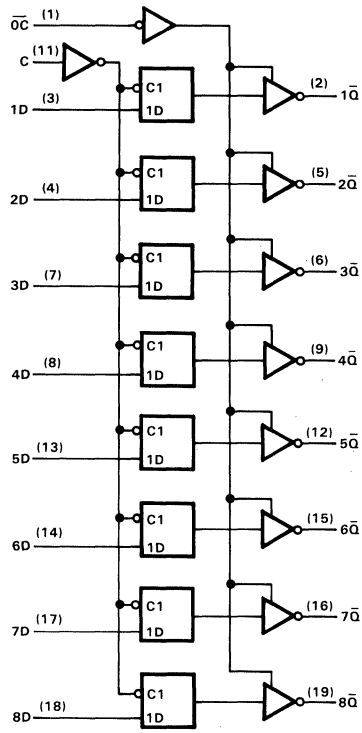
FUNCTION TABLE (EACH LATCH)

INPUTS			OUTPUT
$\overline{OC}$	ENABLE C	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

logic symbol†



logic diagram (positive logic)



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS533, SN54AS533 . . . . . −55 °C to 125 °C
SN74ALS533, SN74AS533 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS533			SN74ALS533			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
t_w	Pulse duration, enable C high	15			15			ns
t_{su}	Setup time, data before enable C↓	15			15			ns
t_h	Hold time, data after enable C↓	7			7			ns
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS533			SN74ALS533			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		10	17		10	17	mA
		Outputs low		17	26		17	26	
		Outputs disabled		18.5	28		18.5	28	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS533		SN74ALS533		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	$\overline{Q}$	4	24	4	19	ns
t_{PHL}			4	14	4	13	
t_{PLH}	C	Any $\overline{Q}$	5	28	5	23	ns
t_{PHL}			4	21	4	18	
t_{PZH}	$\overline{OC}$	Any $\overline{Q}$	4	19	4	17	ns
t_{PZL}			4	20	4	18	
t_{PHZ}	$\overline{OC}$	Any $\overline{Q}$	2	12	2	10	ns
t_{PLZ}			3	22	3	16	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

recommended operating conditions

		SN54AS533			SN74AS533			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			32			48	mA
t_w	Pulse duration, enable C high	3			2			ns
t_{su}	Setup time, data before enable C↓	2			2			ns
t_h	Hold time, data after enable C↓	3			3			ns
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS533			SN74AS533			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2					
	V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4	3.3		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.29	0.5				V
	V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.34	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−50			−50	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V		−0.02	−0.5		−0.02	−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		62	100		62	100	mA
		Outputs low		64	100		64	100	
		Outputs disabled		71	110		71	110	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS533		SN74AS533		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	$\overline{Q}$	4	10	4	7.5	ns
t_{PHL}			4	8	4	7	
t_{PLH}	C	Any $\overline{Q}$	5	11	5	9	ns
t_{PHL}			4.5	8.5	4.5	8	
t_{PZH}	$\overline{OC}$	Any $\overline{Q}$	2	7.5	2	6.5	ns
t_{PZL}			4.5	10.5	4.5	9.5	
t_{PHZ}	$\overline{OC}$	Any $\overline{Q}$	3	7.5	3	6.5	ns
t_{PLZ}			3	8	3	7	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

D2661, APRIL 1982 – REVISED MAY 1986

- **3-State Bus-Driving Inverting Outputs**
- **Buffered Control Inputs**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These 8-bit flip-flops feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

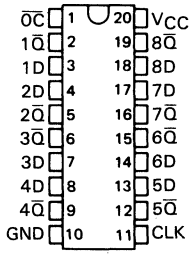
The eight flip-flops of the 'ALS534 and 'AS534 are edge-triggered D-type flip-flops. On the positive transition of the clock, the $\overline{Q}$ outputs will be set to the complement of the logic states that were set up at the D inputs. The 'ALS534 and 'AS534 are functionally equivalent to the 'ALS374 and 'AS374 except for having inverted outputs.

A buffered output-control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

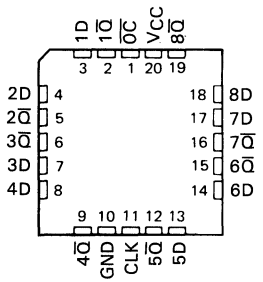
The output control does not affect the internal operatin of the flip-flops. Old data can be retained or new data can be entered while the outputs are off.

The SN54ALS534 and SN54AS534 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ALS534 and SN74AS534 are characterized for operation from 0°C to 70°C.

SN54ALS534, SN54AS534 . . . J PACKAGE
SN74ALS534, SN74AS534 . . . DW OR N PACKAGE
(TOP VIEW)



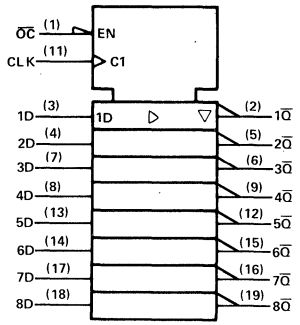
SN54ALS534, SN54AS534 . . . FK PACKAGE
(TOP VIEW)



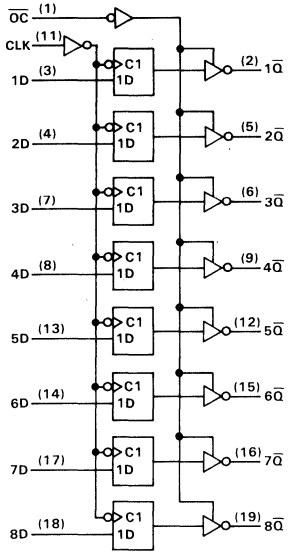
FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS			OUTPUT
$\overline{OC}$	CLK	D	$\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

logic symbol†



logic diagram (positive logic)



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS534, SN54AS534 . . . . . −55 °C to 125 °C
SN74ALS534, SN74AS534 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

recommended operating conditions

			SN54ALS534			SN74ALS534			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−1			−2.6	mA
I_{OL}	Low-level output current				12			24	mA
f_{clock}	Clock frequency		0		30	0		35	MHz
t_w	Pulse duration	CLK high	16.5			14			ns
		CLK low	16.5			14			
t_{su}	Setup time, data before CLK↑		10			10			ns
t_h	Hold time, data after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS534			SN74ALS534			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	CLK, $\overline{OC}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	D					−0.2			−0.2	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	Outputs high		11	19		11	19	mA
			Outputs low		19	28		19	28	
			Outputs disabled		10	31		20	31	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS534		SN74ALS534		
			MIN	MAX	MIN	MAX	
f_{max}			30		35		MHz
t_{PLH}	CLK	Any $\overline{Q}$	3	15	3	12	ns
t_{PHL}			5	18	5	16	
t_{PZH}	$\overline{OC}$	Any $\overline{Q}$	5	19	5	17	ns
t_{PZL}			7	20	7	18	
t_{PHZ}	$\overline{OC}$	Any $\overline{Q}$	2	12	2	10	ns
t_{PLZ}			2	16	2	14	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

recommended operating conditions

			SN54AS534			SN74AS534			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−12			−15	mA
I_{OL}	Low-level output current				32			48	mA
f_{clock}	Clock frequency		0		100	0		125	MHz
t_w	Pulse duration	CLK high	5.5			4			ns
		CLK low	5			3			
t_{su}	Setup time, data before CLK↑		3			2			ns
t_h	Hold time, data after CLK↑		3			2			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS534			SN74AS534			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2					
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4	3.3		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.29	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.34	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−50			−50	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	$\overline{OC}$, CLK	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	D					−3			−2	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC} mA		V_{CC} = 5.5 V	Outputs high		77	120		77	120	mA
			Outputs low		84	128		84	128	
			Outputs disabled		84	128		84	128	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS534		SN74AS534		
			MIN	MAX	MIN	MAX	
f_{max}			100		125		MHz
t_{PLH}	CLK	Any $\overline{Q}$	3	11	3	8	ns
t_{PHL}			4	11.5	4	9	
t_{PZH}	$\overline{OC}$	Any $\overline{Q}$	2	7	2	6	ns
t_{PZL}			3	11	3	10	
t_{PHZ}	$\overline{OC}$	Any $\overline{Q}$	2	7	2	6	ns
t_{PLZ}			2	7	2	6	

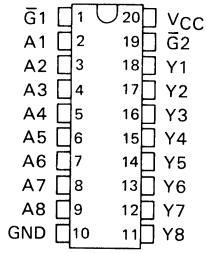
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

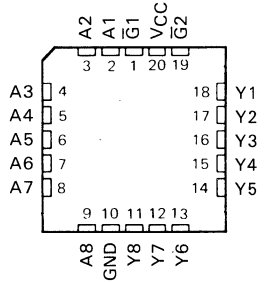
D2661, APRIL 1982 – REVISED MAY 1986

- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **P-N-P Inputs Reduce D-C Loading**
- **Data Flow-Thru Pinout (All Inputs on Opposite Side from Outputs)**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS540, SN54ALS541 . . . J PACKAGE
SN74ALS540, SN74ALS541 . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS540, SN54ALS541 . . . FK PACKAGE
(TOP VIEW)



description

These octal buffers and line drivers are designed to have the performance of the popular SN54ALS240/SN74ALS240 series and, at the same time, offer a pinout with inputs and outputs on opposite sides of the package. This arrangement greatly enhances printed circuit board layout.

The three-state control gate is a 2-input NOR such that if either $\overline{G}1$ or $\overline{G}2$ is high, all eight outputs are in the high-impedance state.

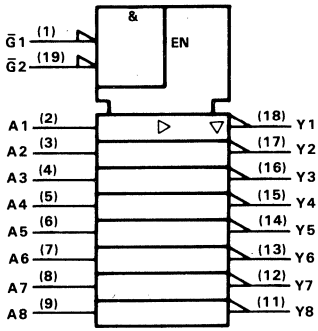
The 'ALS540 provides inverted data and the 'ALS541 provides true data at the outputs.

The -1 versions of the SN74ALS540 and SN74ALS541 parts are identical to the standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes. There are no -1 versions of the SN54ALS540 and SN54ALS541.

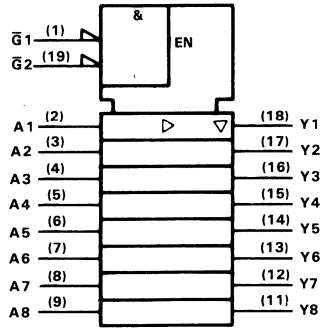
The SN54ALS540 and SN54ALS541 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS540 and SN74ALS541 are characterized for operation from 0°C to 70°C.

logic symbols†

'ALS540

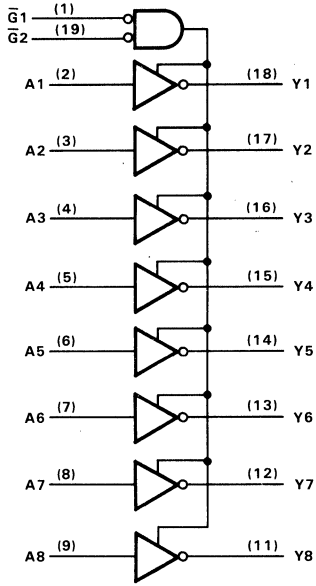


'ALS541

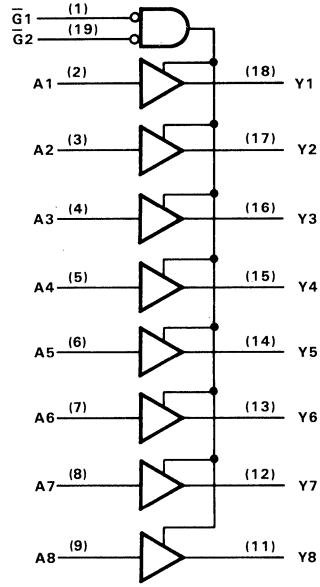


logic diagrams (positive logic)

'ALS540



'ALS541



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS540, SN54ALS541 . . . . . −55°C to 125°C
SN74ALS540, SN74ALS541 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS540 SN54ALS541			SN74ALS540 SN74ALS541			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
							48†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limit applies only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48 mA limit applies for the SN74ALS540-1 and SN74ALS541-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS540 SN54ALS541			SN74ALS540 SN74ALS541			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA¶					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS540	V_{CC} = 5.5 V	Outputs high		5	10		5	10	mA
			Outputs low		13	22		13	22	
			Outputs disabled		11	19		11	19	
	'ALS541	V_{CC} = 5.5 V	Outputs high		6	14		6	14	mA
			Outputs low		15	25		15	25	
			Outputs disabled		13.5	22		13.5	22	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
¶I_{OL} = 48 mA for −1 versions.

'ALS540 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS540	SN54ALS540		SN74ALS540		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	7.5	2	14	2	12	ns
t_{PHL}			5.6	2	11	2	9	
t_{PZH}	$\overline{G}$	Y	9	5	18	5	15	ns
t_{PZL}			12.5	8	24	8	20	
t_{PHZ}	$\overline{G}$	Y	4	1	12	1	10	ns
t_{PLZ}			7	2	14	2	12	

'ALS541 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS541	SN54ALS541		SN74ALS541		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	8.7	4	17	4	14	ns
t_{PHL}			7	2	12	2	10	
t_{PZH}	$\overline{G}$	Y	9	5	18	5	15	ns
t_{PZL}			12.5	8	24	8	20	
t_{PHZ}	$\overline{G}$	Y	4	1	12	1	10	ns
t_{PLZ}			7	2	14	2	12	

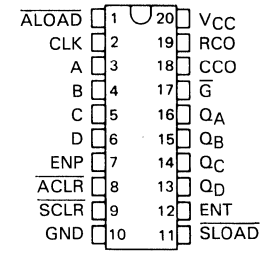
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

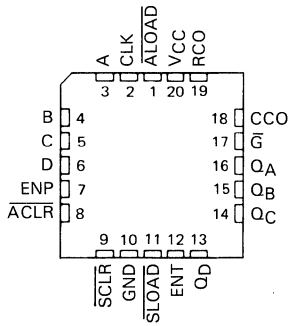
D2661, DECEMBER 1982—REVISED MAY 1986

- **Carry Output for n-Bit Cascading**
- **Buffer-Type Outputs Drive Bus Lines Directly**
- **Choice of Asynchronous or Synchronous Load or Clear**
- **Internal Look-Ahead for Fast Cascading**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS560A, SN54ALS561A . . . J PACKAGE
SN74ALS560A, SN74ALS561A . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS560A, SN54ALS561A . . . FK PACKAGE
(TOP VIEW)



description

The 'ALS560A decade counters and 'ALS561A binary counters are programmable and offer synchronous and asynchronous clearing as well as synchronous and asynchronous loading. All synchronous functions are executed on the positive-going edge of the clock.

The clear function is initiated by applying a low level to either Asynchronous Clear ($\overline{ACLR}$) or Synchronous Clear ($\overline{SCLR}$). Asynchronous (direct) clearing overrides all other functions of the device, while synchronous clearing overrides only the other synchronous functions. Data is loaded from the A, B, C, and D inputs by applying a low level to Asynchronous Load ($\overline{ALOAD}$) or by the combination of a low level at Synchronous Load ($\overline{SLOAD}$) and a positive-going clock transition. The counting function is enabled only when Enable P (ENP), Enable T (ENT), $\overline{ACLR}$, $\overline{ALOAD}$, $\overline{SCLR}$, and $\overline{SLOAD}$ are all high.

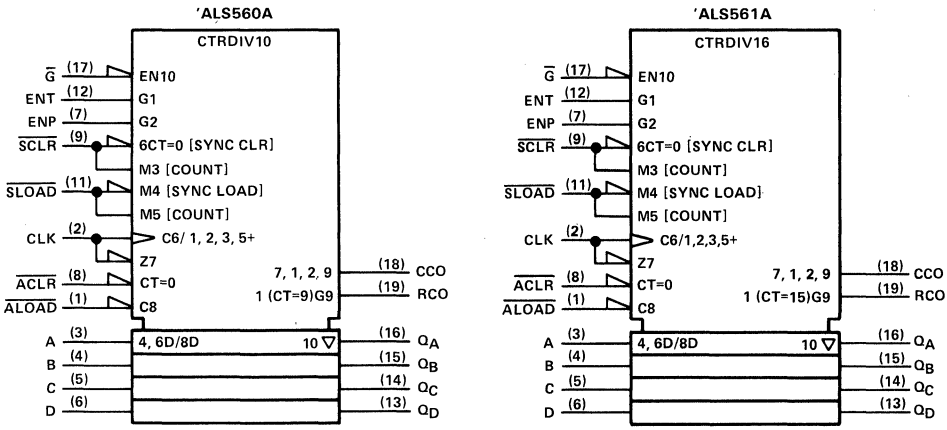
A high level at the Output Enable ($\overline{G}$) forces the Q outputs into the high-impedance state, and a low level enables those outputs. Counting is independent of $\overline{G}$. ENT is fed forward to enable the Ripple Carry Output (RCO) to produce a high-level pulse while the count is maximum (9 or 15). The Clocked Carry Output (CCO) produces a high-level pulse for a duration equal to that of the low level of the clock when RCO is high and the counter is enabled (both ENP and ENT are high); otherwise, CCO is low. CCO does not have the glitches commonly associated with a ripple-carry output. Cascading is normally accomplished by connecting RCO or CCO of the first counter to ENT of the next counter. However, for very-high-speed counting, RCO should be used for cascading since CCO does not become active until the clock returns to the low level.

The SN54ALS560A and SN54ALS561A are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS560A and SN74ALS561A are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS								OPERATION
$\overline{G}$	$\overline{ACLR}$	$\overline{ALOAD}$	$\overline{SCLR}$	$\overline{SLOAD}$	ENT	ENP	CLK	
H	X	X	X	X	X	X	X	Q Outputs Disabled
L	L	X	X	X	X	X	X	Asynchronous Clear
L	H	L	X	X	X	X	X	Asynchronous Load
L	H	H	L	X	X	X	↑	Synchronous Clear
L	H	H	H	L	X	X	↑	Synchronous Load
L	H	H	H	H	H	H	↑	Count
L	H	H	H	H	L	X	X	Inhibit Counting
L	H	H	H	H	X	L	X	Inhibit Counting

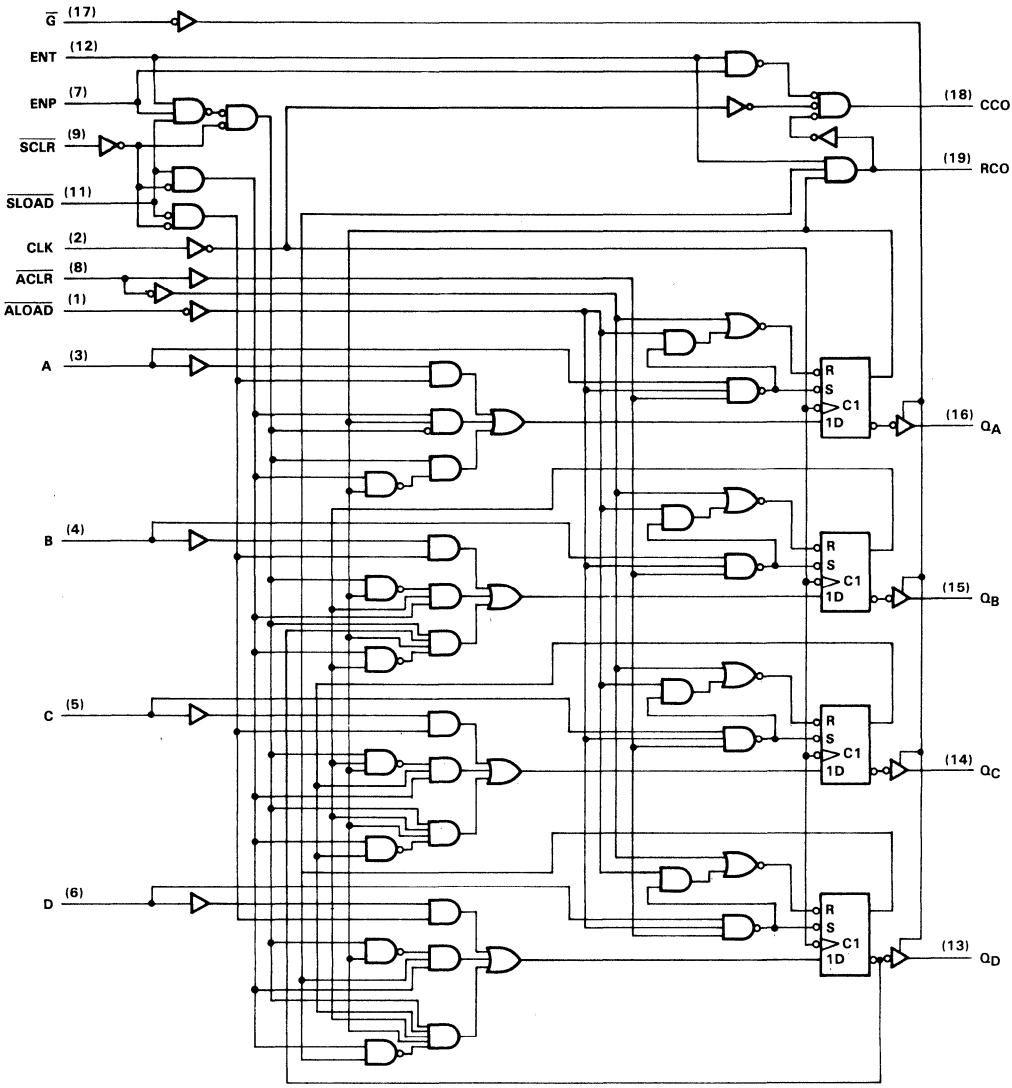
logic symbols†



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

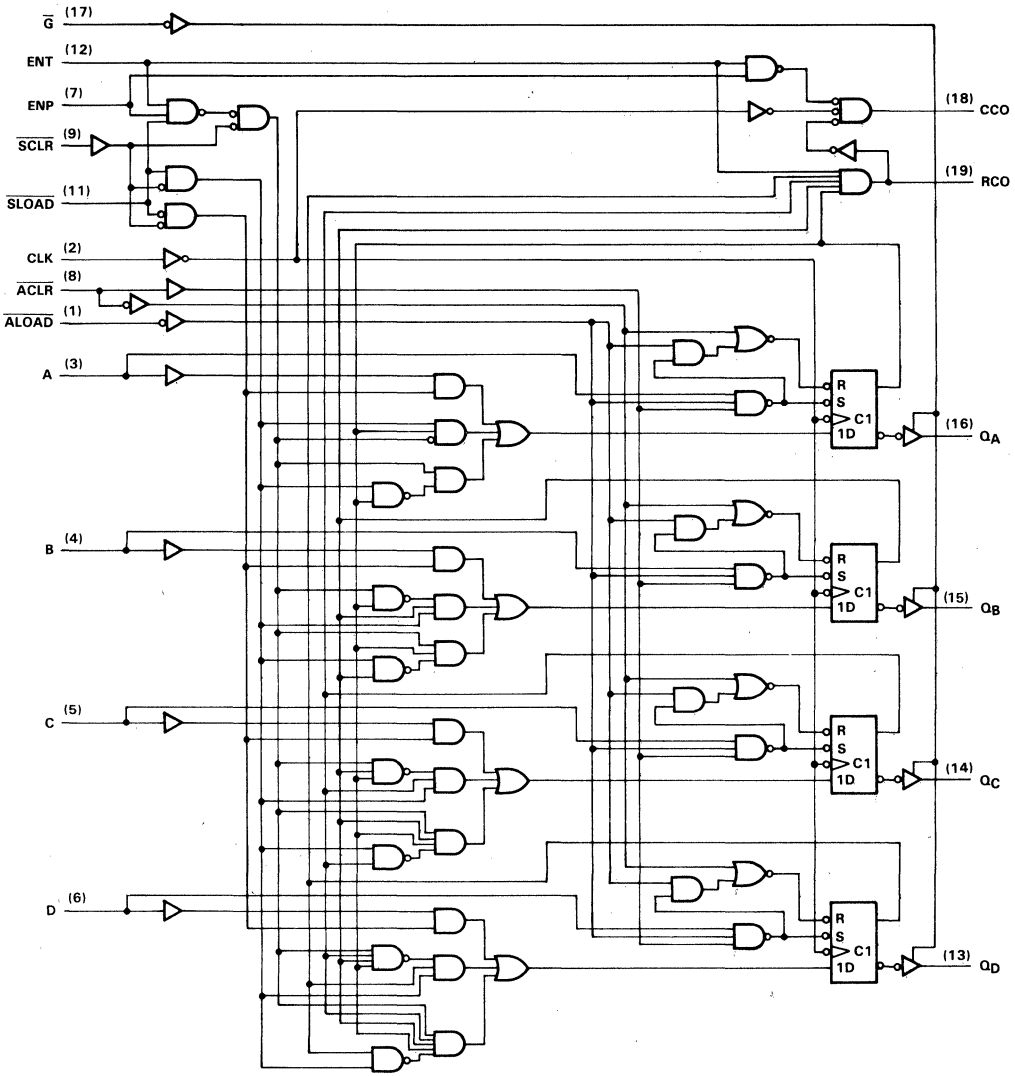
TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

'ALS560A logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

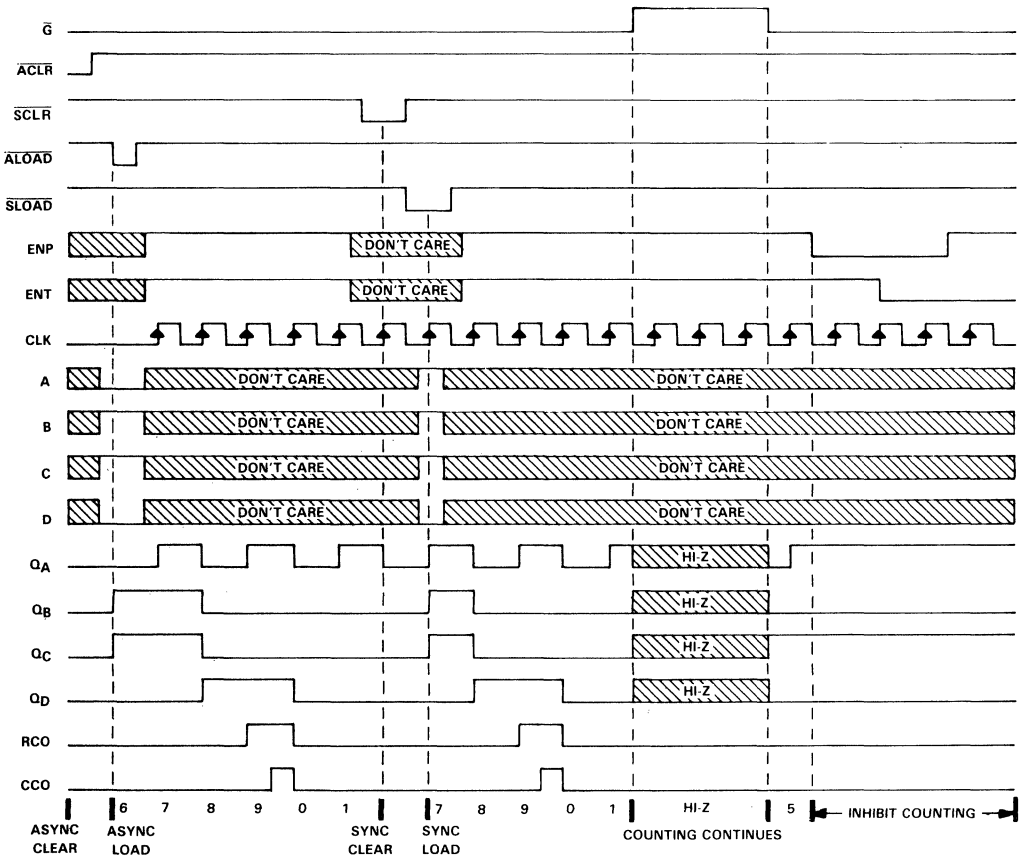
'ALS561A logic diagram (positive logic)



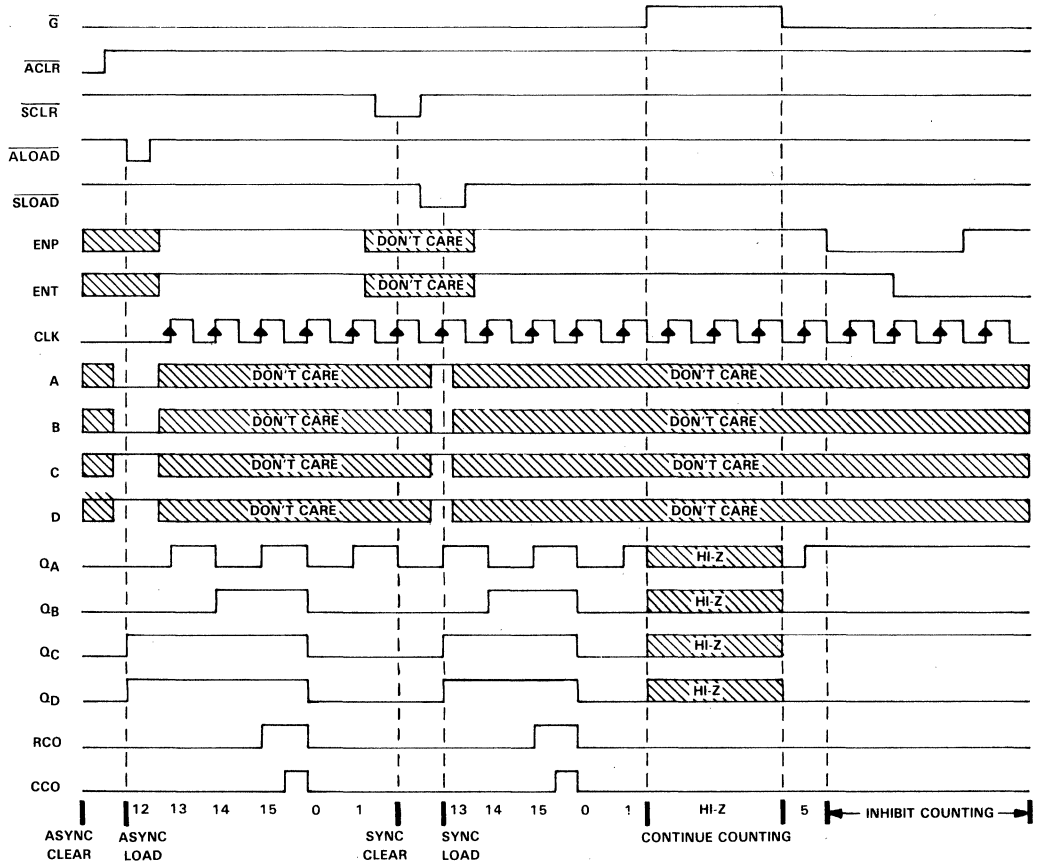
Pin numbers shown are for D, J, and N packages.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

'ALS560A typical load, count, and inhibit sequences



'ALS561A typical load, count, and inhibit sequences



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS560A, SN54ALS561A . . . . . −55°C to 125°C
SN74ALS560A, SN74ALS561A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

				SN54ALS560A SN54ALS561A			SN74ALS560A SN74ALS561A			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
I_{OH}	High-level output current	Q outputs				−1			−2.6	mA
		CCO and RCO				−0.4			−0.4	
I_{OL}	Low-level output current	Q outputs				12			24	mA
		CCO and RCO				4			8	
f_{clock}	Clock frequency	'ALS560A		0		18	0		20	MHz
		'ALS561A		0		25	0		30	
t_w	Pulse duration	$\overline{ACLR}$ or $\overline{ALOAD}$ low		20			15			ns
		'ALS560A	CLK high	27.5			25			
			CLK low	27.5			25			
		'ALS561A	CLK high	20			16.5			
			CLK low	20			16.5			
t_{su}	Setup time before CLK↑	ENP, ENT	High	25			20			ns
			Low	25			20			
		Data at A, B, C, D		25			20			
		$\overline{SCLR}$	Low	21			15			
			High (inactive)	35			30			
		$\overline{SLOAD}$	Low	20			15			
			High (inactive)	35			30			
		$\overline{ACLR}$ or $\overline{ALOAD}$ inactive		10			10			
t_h	Hold time after CLK↑ for data, ENP, ENT, $\overline{SCLR}$, or $\overline{SLOAD}$			0			0			ns
T_A	Operating free-air temperature			−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS560A SN54ALS561A			SN74ALS560A SN74ALS561A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	All outputs	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	Q outputs	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	Q outputs	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
	CCO and RCO	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	ENT and ENP	V_{CC} = 5.5 V,	V_I = 7 V			0.2			0.2	mA
	Other inputs					0.1			0.1	
I_{IH}	ENT and ENP	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	μA
	Other inputs					20			20	
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O‡	CCO and RCO	V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
	Q			−30		−112	−30		−112	
I_{CC}		V_{CC} = 5.5 V	Outputs high		17	27		17	27	mA
			Outputs low		21	33		21	33	
			Outputs disabled		22	36		22	36	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS560A SN54ALS561A		SN74ALS560A SN74ALS561A		
			MIN	MAX	MIN	MAX	
f_{max}	'ALS560A		18		20		MHz
	'ALS561A		25		30		
t_{PLH}	CLK	Any Q	4	15	4	12	ns
t_{PHL}			5	21	5	18	
t_{PLH}	CLK	RCO	9	35	9	29	ns
t_{PHL}			8	29	8	24	
t_{PLH}	CLK	CCO	8	31	8	26	ns
t_{PHL}			5	20	5	16	
t_{PLH}	$\overline{ALOAD}$	Any Q	10	38	10	35	ns
t_{PHL}			7	27	7	23	
t_{PLH}	$\overline{ALOAD}$	RCO	15	50	15	40	ns
t_{PHL}			12	35	12	30	
t_{PLH}	$\overline{ALOAD}$	CCO	25	65	25	55	ns
t_{PHL}			12	42	12	33	
t_{PLH}	A, B, C, or D	Any Q	8	35	8	30	ns
t_{PHL}			7	27	7	22	
t_{PLH}	ENT	RCO	5	20	5	16	ns
t_{PHL}			4	18	4	14	
t_{PLH}	ENT	CCO	12	35	12	32	ns
t_{PHL}			4	15	4	12	
t_{PLH}	ENP	CCO	5	22	5	18	ns
t_{PHL}			4	14	4	12	
t_{PHL}	$\overline{ACLR}$	Any Q	7	28	7	22	ns
t_{PZH}	$\overline{G}$	Any Q	5	24	5	19	ns
t_{PZL}			8	28	8	23	
t_{PHZ}	$\overline{G}$	Any Q	2	12	2	10	ns
t_{PLZ}			4	20	4	15	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

ALS and AS Circuits

D2661, DECEMBER 1982 – REVISED MAY 1986

- **3-State Buffer-Type Outputs Drive Bus-Lines Directly**
- **Bus Structured Pinout**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

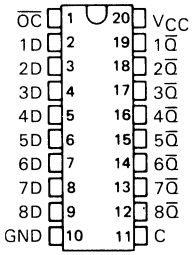
The eight latches are transparent D-type latches. When the enable (C) is high the $\overline{Q}$ outputs will follow the complements of data (D) inputs. When the enable is taken low the output will be latched at the inverses of the levels that were set up at the D inputs.

A buffered output-control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased high-logic level provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

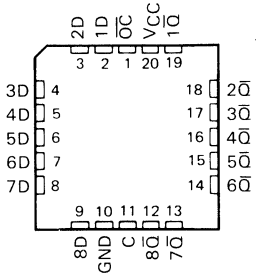
The output control ($\overline{OC}$) does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54ALS563A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS563A is characterized for operation from 0°C to 70°C.

SN54ALS563A . . . J PACKAGE
SN74ALS563A . . . DW OR N PACKAGE
(TOP VIEW)



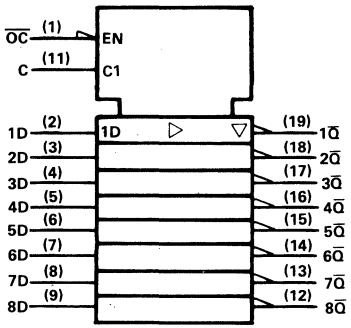
SN54ALS563A . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE
(EACH LATCH)

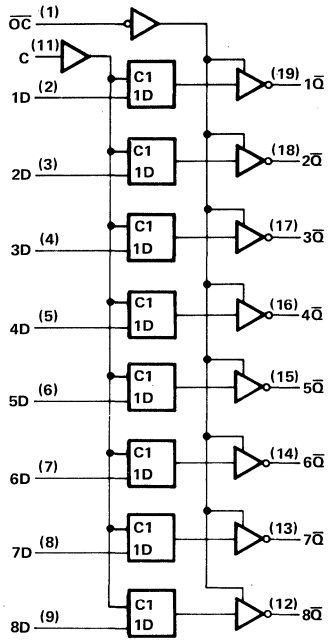
INPUTS			OUTPUT
ENABLE			
$\overline{OC}$	C	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS563A . . . . . −55°C to 125°C
SN74ALS563A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS563A			SN74ALS563A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
t_w	Pulse duration, enable C high	15			15			ns
t_{su}	Setup time, data before enable C↓	10			10			ns
t_h	Hold time, data after enable C↓	10			10			ns
T_A	Operating free-air temperature	−55		125	0		70	°C

TEXAS INSTRUMENTS
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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted

PARAMETER	TEST CONDITIONS		SN54ALS563A			SN74ALS563A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OL} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		10	17		10	17	mA
		Outputs low		16	26		16	26	
		Outputs disabled		17	29		17	29	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

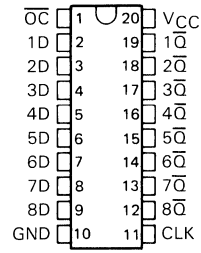
switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS563A	SN54ALS563A		SN74ALS563A		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	D	$\overline{Q}$	10	3	21	3	18	ns
t_{PHL}			8	3	15	3	14	
t_{PLH}	C	$\overline{Q}$	8	8	29	8	22	ns
t_{PHL}			14	8	22	8	21	
t_{PZH}	OC	$\overline{Q}$	8	4	21	4	18	ns
t_{PZL}			10	4	21	4	18	
t_{PHZ}	OC	$\overline{Q}$	5	2	12	2	10	ns
t_{PLZ}			7	3	18	3	15	

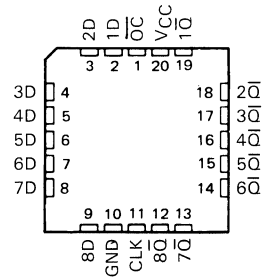
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

- **3-State Buffer-Type Inverting Outputs Drive Bus-Lines Directly**
- **Bus-Structured Pinout**
- **Buffered Control Inputs**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS564A . . . J PACKAGE
SN74ALS564A . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS564A . . . FK PACKAGE
(TOP VIEW)



description

These 8-bit registers feature inverting three-state outputs designed specifically for bus driving. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight-bit edge-triggered D-type flip-flops enter data on the low-to-high transition of the clock.

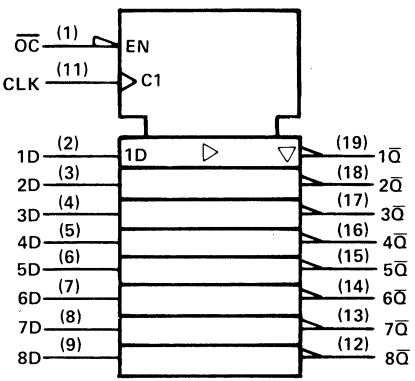
The output control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54ALS564A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS564A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(EACH FLIP-FLOP)

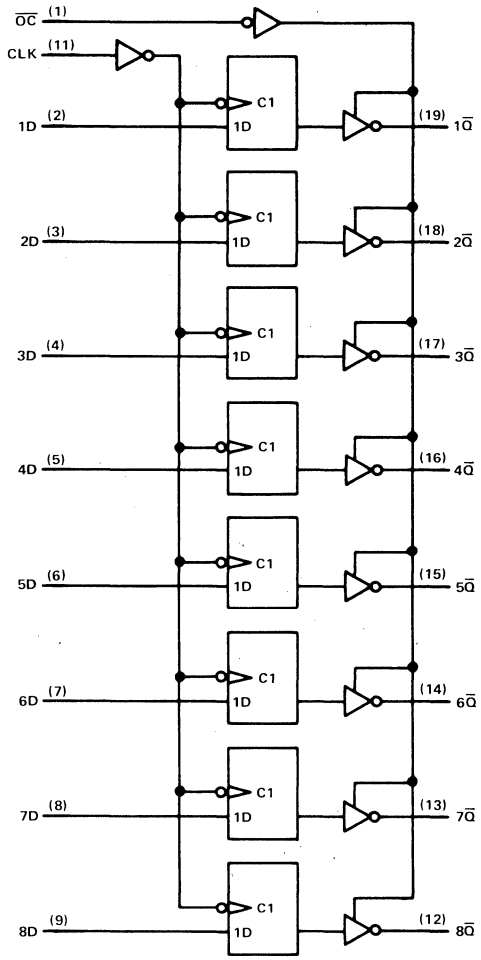
INPUTS			OUTPUT
$\overline{OC}$	CLK	D	$\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_O$
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS564A . . . . . −55°C to 125°C
SN74ALS564A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS564A			SN74ALS564A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−1			−2.6	mA
I_{OL}	Low-level output current				12			24	mA
f_{clock}	Clock frequency		0		25	0		30	MHz
t_w	Pulse duration	CLK high	16.5			14			ns
		CLK low	16.5			14			
t_{su}	Setup time, data before CLK↑		15			15			ns
t_h	Hold time, data after CLK↑		4			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS564A			SN74ALS564A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		10	18		10	18	mA
		Outputs low		15	24		15	24	
		Outputs disabled		16	30		16	30	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25° C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS564A	SN54ALS564A		SN74ALS564A		
			TYP	MIN	MAX	MIN	MAX	
f_{max}			50	25		30		MHz
t_{PLH}	CLK	Any $\overline{Q}$	9	4	15	4	14	ns
t_{PHL}			9	4	15	4	14	
t_{PZH}	$\overline{OC}$	Any $\overline{Q}$	11	4	21	4	18	ns
t_{PZL}			11	4	21	4	18	
t_{PHZ}	$\overline{OC}$	Any $\overline{Q}$	6	2	12	2	10	ns
t_{PLZ}			8	3	17	3	15	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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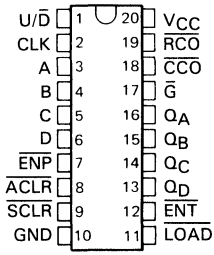
SN54ALS568A, SN54ALS569A, SN74ALS568A, SN74ALS569A
SYNCHRONOUS 4-BIT UP/DOWN DECADE AND BINARY COUNTERS WITH 3-STATE OUTPUTS

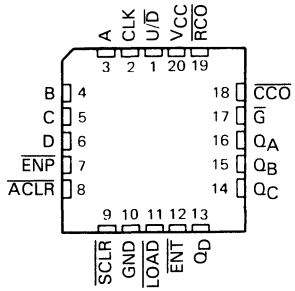
D2661, APRIL 1982–REVISED MAY 1986

- **3-State Q Outputs Drive Bus Lines Directly**
- **Counter Operation Independent of 3-State Output**
- **Fully Synchronous Clear, Count, and Load**
- **Asynchronous Clear Also Provided**
- **Fully Cascadable**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS568A, SN54ALS569A . . . J PACKAGE
SN74ALS568A, SN74ALS569A . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS568A, SN54ALS569A . . . FK PACKAGE
(TOP VIEW)



description

The 'ALS568A decade counters and 'ALS569A binary counters are programmable, count up or down, and offer both synchronous and asynchronous clearing. All synchronous functions are executed on the positive-going edge of the clock.

The clear function is initiated by applying a low level to either Asynchronous Clear ($\overline{ACLR}$) or Synchronous Clear ($\overline{SCLR}$). Asynchronous (direct) clearing overrides all other functions of the device, while synchronous clearing overrides only the other synchronous functions. Data is loaded from the A, B, C, and D inputs by holding Load ($\overline{LOAD}$) low during a positive-going clock transition. The counting function is enabled only when Enable P ($\overline{ENP}$) and Enable T ($\overline{ENT}$) are low and $\overline{ACLR}$, $\overline{SCLR}$, and $\overline{LOAD}$ are high. The Up/Down (U/$\overline{D}$) input controls the direction of the count. These counters count up when U/$\overline{D}$ is high and count down when U/$\overline{D}$ is low.

A high level at the Output Enable ($\overline{G}$) forces the Q outputs into the high-impedance state, and a low level enables those outputs. Counting is independent of of $\overline{G}$. $\overline{ENT}$ is fed forward to enable the Ripple Carry Output ($\overline{RCO}$) to produce a low-level pulse while the count is zero (all Q outputs low) when counting down or maximum (9 or 15) when counting up. The Clocked Carry Output ($\overline{CCO}$) produces a low level pulse for a duration equal to that of the low level of the clock when $\overline{RCO}$ is low and the counter is enabled (both $\overline{ENP}$ and $\overline{ENT}$ are low); otherwise, $\overline{CCO}$ is high. $\overline{CCO}$ does not have the glitches commonly associated with a ripple-carry output. Cascading is normally accomplished by connecting $\overline{RCO}$ or $\overline{CCO}$ of the first counter to $\overline{ENT}$ of the next counter. However, for very-high-speed counting, $\overline{RCO}$ should be used for cascading since $\overline{CCO}$ does not become active until the clock returns to the low level.

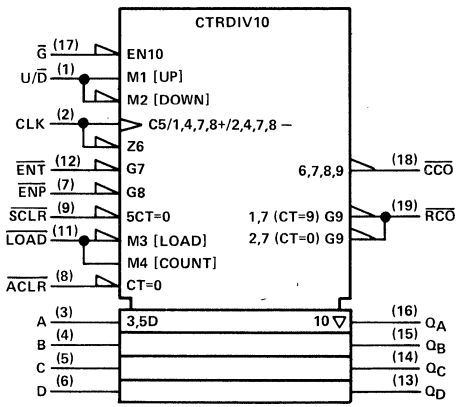
The SN54ALS568A and SN54ALS569A are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS568A and SN74ALS569A are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

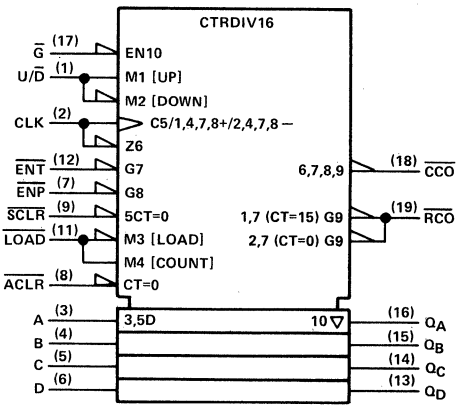
INPUTS								OPERATION
$\overline{G}$	$\overline{ACLR}$	$\overline{SCLR}$	$\overline{LOAD}$	$\overline{ENT}$	$\overline{ENP}$	U/$\overline{D}$	CLK	
H	X	X	X	X	X	X	X	Q Outputs Disabled
L	L	X	X	X	X	X	X	Asynchronous Clear
L	H	L	X	X	X	X	↑	Synchronous Clear
L	H	H	L	X	X	X	↑	Load
L	H	H	H	L	L	H	↑	Count Up
L	H	H	H	L	L	L	↑	Count Down
L	H	H	H	H	X	X	X	Inhibit Count
L	H	H	H	X	H	X	X	Inhibit Count

logic symbols†

'ALS568A



'ALS569A



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

TEXAS INSTRUMENTS
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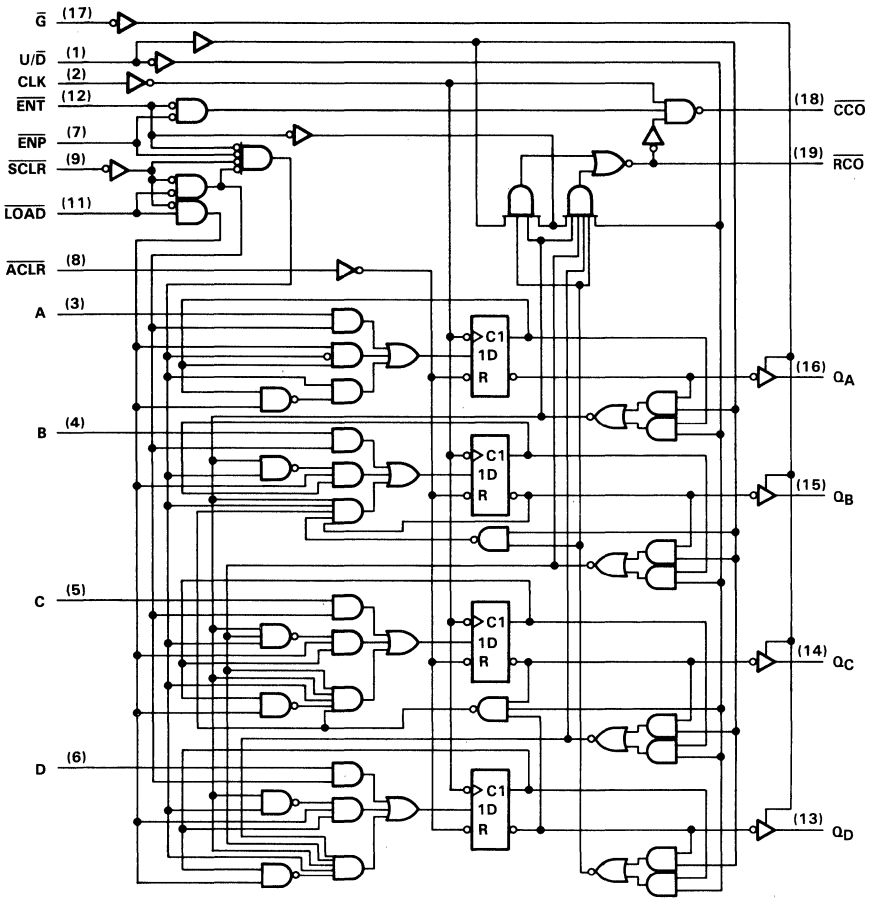
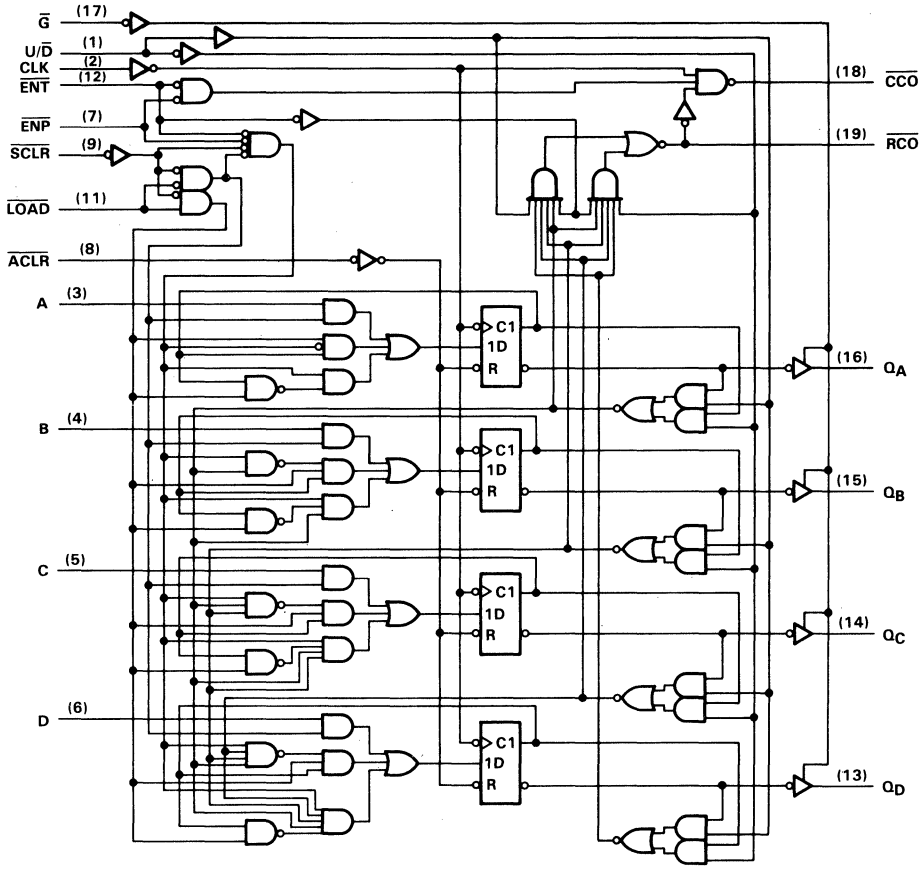
'ALS568A logic diagram (positive logic)



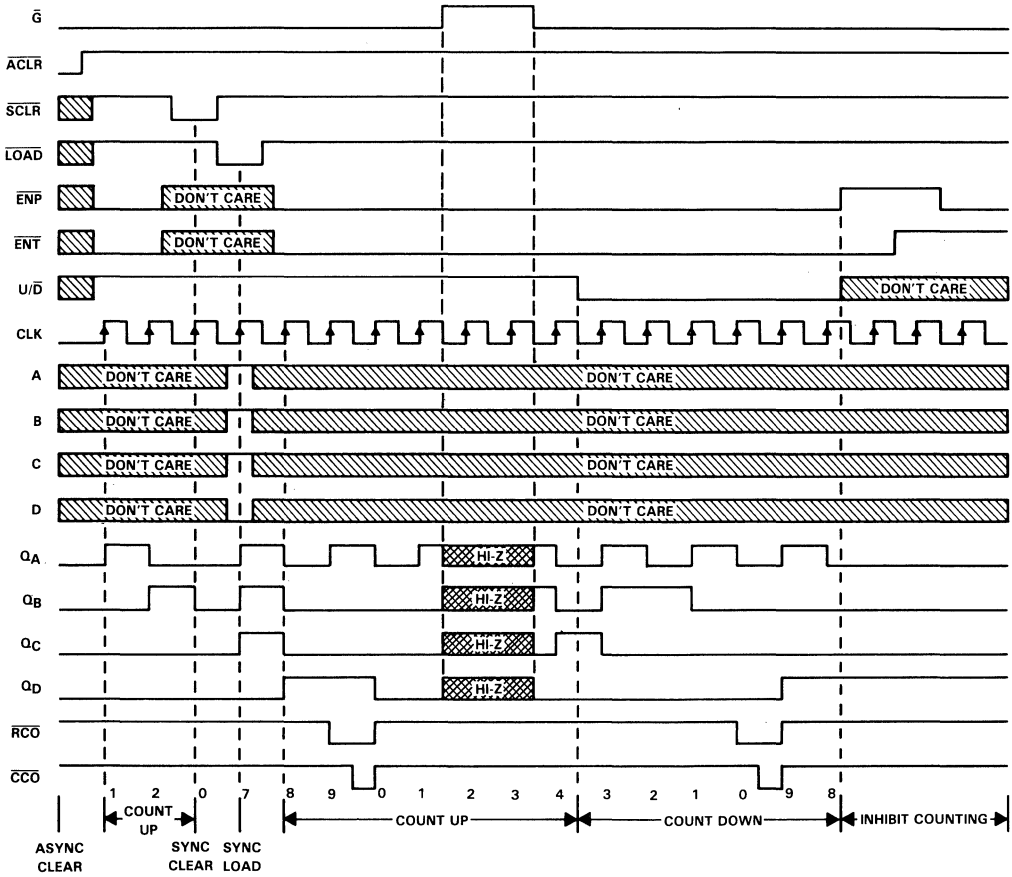
Pin numbers shown are for DW, J, and N packages.

'ALS569A logic diagram (positive logic)

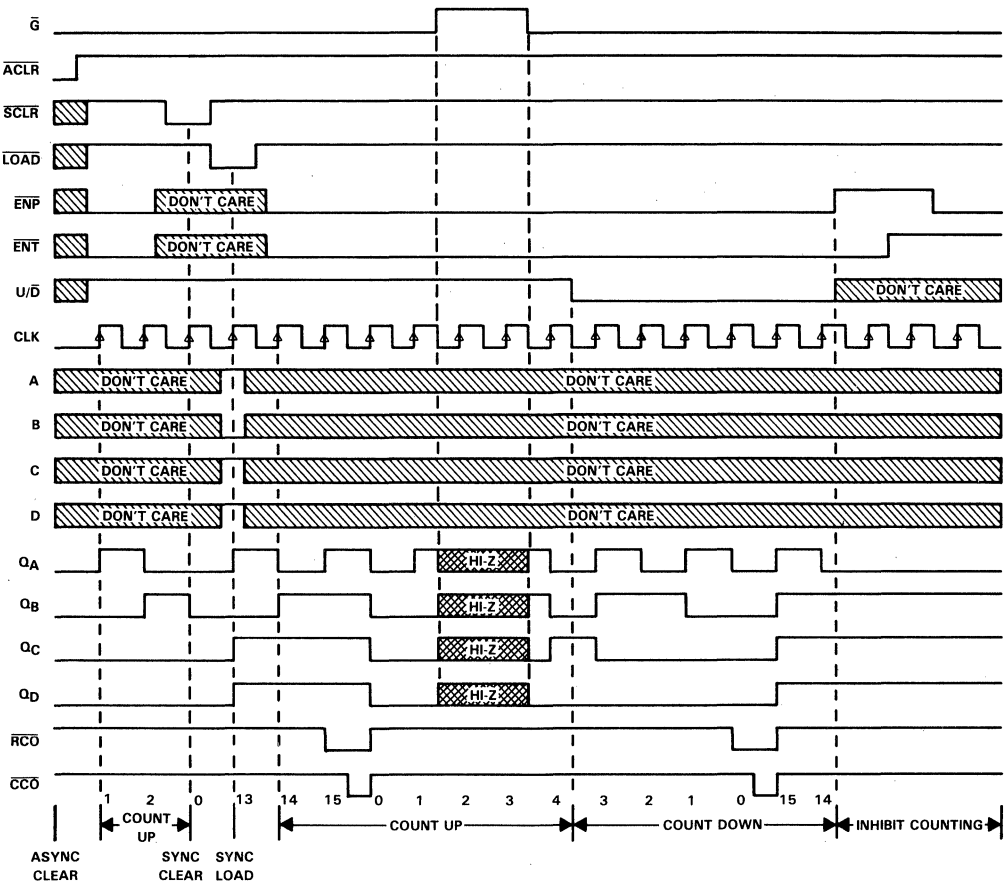


Pin numbers shown are for DW, J, and N packages.

'ALS568A typical load, count, and inhibit sequences



'ALS569A typical load, count, and inhibit sequences



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS568A, SN54ALS569A . . . . . −55 °C to 125 °C
SN74ALS568A, SN74ALS569A . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

				SN54ALS568A SN54ALS569A			SN74ALS568A SN74ALS569A			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltge					0.7			0.8	C
I_{OH}	High-level output current	Q outputs				−1			−2.6	mA
		$\overline{CCO}$ and $\overline{RCO}$				−0.4			−0.4	
I_{OL}	Low-level output current	Q outputs				12			24	mA
		$\overline{CCO}$ and $\overline{RCO}$				4			8	
f_{clock}	Clock frequency	'ALS568A		0		18	0		20	MHz
		'ALS569A		0		22	0		30	
t_w	Pulse duration	$\overline{ALCR}$ or $\overline{LOAD}$ low		20			15			ns
		'ALS568A	CLK high	27.5			25			
			CLK low	27.5			25			
		'ALS569A	CLK high	20			16.5			
			CLK low	20			16.5			
t_{su}	Setup time before CLK ↑	Data at A, B, C, D		25			20			ns
		$\overline{ENP}$, $\overline{ENT}$	High	35			30			
			Low	25			20			
		$\overline{SCLR}$	Low	20			15			
			High (inactive)	35			30			
		$\overline{LOAD}$	Low	20			15			
			High (inactive)	35			30			
		U/$\overline{D}$		35			30			
		$\overline{ACLR}$ inactive		10			10			
t_h	Hold time after CLK↑ for any input			0			0			ns
T_A	Operating free-air temperature			−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS568A SN54ALS569A			SN74ALS568A SN74ALS569A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	All outputs	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
	Q outputs	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	Q outputs	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
	$\overline{CCO}$ and $\overline{RCO}$	V_{CC} = 4.5 V,	I_{OH} = 4 mA		0.25	0.4		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O‡	$\overline{CCO}$ and $\overline{RCO}$	V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
	Q outputs			−30		−112	−30		−112	
I_{CC}		V_{CC} = 5.5 V	Outputs high		16	26		16	26	mA
			Outputs low		20	32		20	32	
			Outputs disabled		20	32		20	32	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

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switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS568A SN54ALS569A		SN74ALS568A SN74ALS569A		
			MIN	MAX	MIN	MAX	
f_{max}	'ALS568A		18		20		MHz
	'ALS569A		22		30		
t_{PLH}	CLK	Any Q	4	21	4	13	ns
t_{PHL}			7	19	7	16	
t_{PLH}	CLK	$\overline{RCO}$	12	37	12	28	ns
t_{PHL}			10	28	10	19	
t_{PLH}	CLK	$\overline{CCO}$	5	17	5	13	ns
t_{PHL}			6	30	6	25	
t_{PLH}	U/$\overline{D}$	$\overline{RCO}$	9	31	9	23	ns
t_{PHL}			9	33	9	19	
t_{PLH}	$\overline{ENT}$	$\overline{RCO}$	6	21	6	15	ns
t_{PHL}			4	20	4	13	
t_{PLH}	$\overline{ENT}$	$\overline{CCO}$	5	18	5	13	ns
t_{PHL}			9	32	9	23	
t_{PLH}	$\overline{ENP}$	$\overline{CCO}$	4	18	4	12	ns
t_{PHL}			5	18	5	14	
t_{PHL}	$\overline{ACLR}$	Any Q	9	25	9	20	ns
t_{PZH}	$\overline{G}$	Any Q	6	23	6	18	ns
t_{PZL}			6	29	6	24	
t_{PHZ}	$\overline{G}$	Any Q	1	12	1	10	ns
t_{PLZ}			3	29	3	13	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54ALS573B, SN54ALS580A, SN54AS573, SN54AS580
SN74ALS573B, SN74ALS580A, SN74AS573, SN74AS580
OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

D2661, DECEMBER 1982 – REVISED MAY 1986

- **3-State Buffer-Type Outputs Drive Bus-Lines Directly**
- **Bus-Structured Pinout**
- **Choice of True or Inverting Logic**
  'ALS573B, 'AS573 True Outputs
  'ALS580A, 'AS580 Inverting Outputs
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

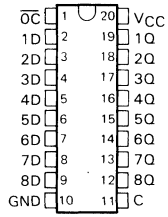
The eight latches are transparent D-type latches. While the enable (C) is high the outputs (Q or $\overline{Q}$) will respond to the data (D) inputs. When the enable is taken low the outputs will be latched to retain the data that was set up.

A buffered output-control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

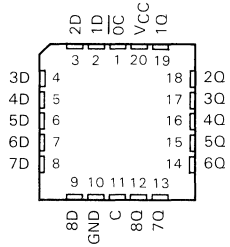
The output control ($\overline{OC}$) does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are at high impedance.

The SN54ALS' and SN54AS' devices are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS' and SN74AS' devices are characterized for operation from 0°C to 70°C.

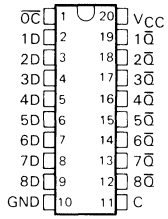
SN54ALS573B, SN54AS573 . . . J PACKAGE
SN74ALS573B, SN74AS573 . . . DW OR N PACKAGE
(TOP VIEW)



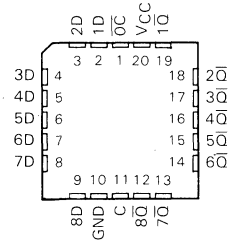
SN54ALS573B, SN54AS573 . . . FK PACKAGE
(TOP VIEW)



SN54ALS580A, SN54AS580 . . . J PACKAGE
SN74ALS580A, SN74AS580 . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS580A, SN54AS580 . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLES

'ALS573B, 'AS573
(EACH LATCH)

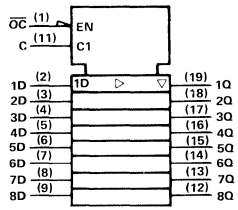
INPUTS			OUTPUT
ENABLE			
$\overline{OC}$	C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_O
H	X	X	Z

'ALS580A, 'AS580
(EACH LATCH)

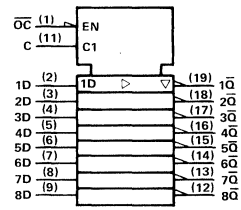
INPUTS			OUTPUT
ENABLE			
$\overline{OC}$	C	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}_O$
H	X	X	Z

logic symbols†

'ALS573B, 'AS573



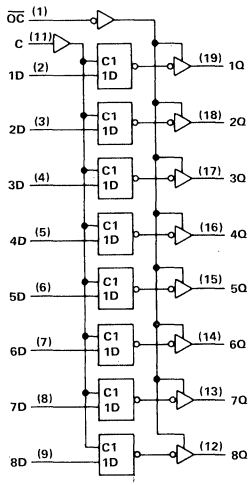
'ALS580A, 'AS580



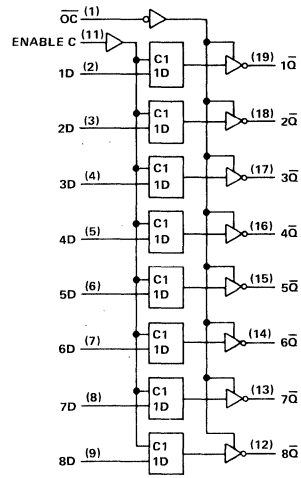
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

'ALS573B, 'AS573



'ALS580A, 'AS580



Pin numbers shown are for DW, J, and N packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range; SN54ALS573B, SN54ALS580A . . . . . −55°C to 125°C
SN74ALS573B, SN74ALS580A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS573B SN54ALS580A			SN74ALS573B SN74ALS580A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−1			−2.6	mA
I_{OL}	Low-level output current				12			−24	mA
t_w	Pulse duration, enable C high	'ALS573B	10			10			ns
		'ALS580A	15			15			
t_{su}	Setup time, data before enable C↓		10			10			ns
t_h	Hold time, data after enable C↓	'ALS573B	7			7			ns
		'ALS580A	10			10			
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS573B SN54ALS580A			SN74ALS573B SN74ALS580A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V,			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS573B	V_{CC} = 5.5 V	Outputs high		10	17		10	17	mA
			Outputs low		15	24		15	24	
			Outputs disabled		16	27		16	27	
	'ALS580A		Outputs high		10	17		10	17	
			Outputs low		16	26		16	26	
			Outputs disabled		17	29		17	29	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS573B switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS573B	SN54ALS573B		SN74ALS573B		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	7	2	15	2	14	ns
t_{PHL}			7	2	15	2	14	
t_{PLH}	C	Q	12	8	25	8	20	ns
t_{PHL}			12	8	20	8	19	
t_{PZH}	$\overline{OC}$	Q	9	4	21	4	18	ns
t_{PZL}			11	4	21	4	18	
t_{PHZ}	$\overline{OC}$	Q	5	2	12	2	10	ns
t_{PLZ}			7	3	18	3	15	

'ALS580A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS580A	SN54ALS580A		SN74ALS580A		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	D	$\overline{Q}$	10	3	21	3	18	ns
t_{PHL}			8	3	15	3	14	
t_{PLH}	C	$\overline{Q}$	8	8	29	8	22	ns
t_{PHL}			14	8	22	8	21	
t_{PZH}	$\overline{OC}$	$\overline{Q}$	8	4	21	4	18	ns
t_{PZL}			10	4	21	4	18	
t_{PHZ}	$\overline{OC}$	$\overline{Q}$	5	2	12	2	10	ns
t_{PLZ}			7	3	18	3	15	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54AS573, SN54AS580 . . . . . −55°C to 125°C
SN74AS573, SN74AS580 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54AS573 SN54AS580			SN74AS573 SN74AS580			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−12			−15	mA
I_{OL}	Low-level output current				32			−48	mA
t_w	Pulse duration, enable C high	'AS573	5.5			4.5			ns
		'AS580	3			2			
t_{su}	Setup time, data before enable C↓		2			2			ns
t_h	Hold time, data after enable C↓		3			3			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS573 SN54AS580			SN74AS573 SN74AS580			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.3		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.28	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.33	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V,			−50			−50	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'AS573	V_{CC} = 5.5 V	Outputs high		56	93		56	93	mA
			Outputs low		55	90		55	90	
			Outputs disabled		65	106		65	106	
	'AS580		Outputs high		62	100		62	100	
			Outputs low		65	106		65	106	
			Outputs disabled		71	115		71	115	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'AS573 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS573		SN74AS573		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	3	9	3	6	ns
t_{PHL}			3	7	3	6	
t_{PLH}	C	Q	6	14	6	11.5	ns
t_{PHL}			4	9	4	7.5	
t_{PZH}	$\overline{OC}$	Q	2	8	2	6.5	ns
t_{PZL}			4	11	4	9.5	
t_{PHZ}	$\overline{OC}$	Q	2	8	2	6.5	ns
t_{PLZ}			2	8	2	7	

'AS580 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS580		SN74AS580		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	$\overline{Q}$	3	10	3	7.5	ns
t_{PHL}			3	7.5	3	7	
t_{PLH}	C	$\overline{Q}$	5	12	5	9	ns
t_{PHL}			4	8.5	4	8	
t_{PZH}	$\overline{OC}$	$\overline{Q}$	2	7.5	2	6.5	ns
t_{PZL}			4	10.5	4	9.5	
t_{PHZ}	$\overline{OC}$	$\overline{Q}$	2	7.5	2	6.5	ns
t_{PLZ}			2	8	2	7	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

D2661, JUNE 1982 – REVISED MAY 1986

- **3-State Buffer-Type Noninverting Outputs Drive Bus-Lines Directly**
- **Bus-Structured Pinout**
- **Buffered Control Inputs**
- **'ALS575A and 'AS575 Have Synchronous Clear**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These 8-bit registers feature three-state outputs designed specifically for bus driving. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight edge-triggered D-type flip-flops enter data on the low-to-high transition of the clock. The 'ALS575A and 'AS575 may be synchronously cleared by taking the $\overline{CLR}$ input low.

The output-control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54ALS' and SN54AS' devices are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS' and SN74AS' devices are characterized for operation from 0°C to 70°C.

FUNCTION TABLES

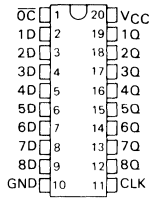
'ALS574A, 'AS574
(EACH FLIP-FLOP)

INPUTS			OUTPUT
$\overline{OC}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

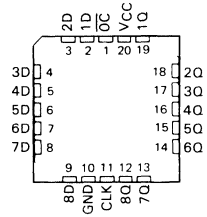
'ALS575A, 'AS575
(EACH FLIP-FLOP)

INPUTS				OUTPUT
$\overline{OC}$	$\overline{CLR}$	CLK	D	Q
L	L	↑	X	L
L	H	↑	H	H
L	H	↑	L	L
L	H	L	X	Q_0
H	X	X	X	Z

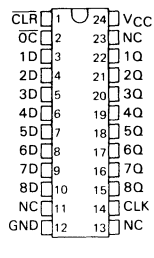
SN54ALS574A, SN54AS574 . . . J PACKAGE
SN74ALS574A, SN74AS574 . . . DW OR N PACKAGE
(TOP VIEW)



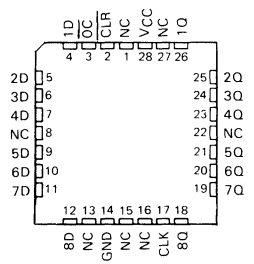
SN54ALS574A, SN54AS574 . . . FK PACKAGE
(TOP VIEW)



SN54ALS575A, SN54AS575 . . . JT PACKAGE
SN74ALS575A, SN74AS575 . . . DW OR NT PACKAGE
(TOP VIEW)



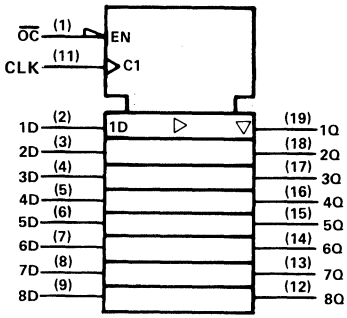
SN54ALS575A, SN54AS575 . . . FK PACKAGE
SN74ALS575A, SN74AS575 . . . FN PACKAGE
(TOP VIEW)



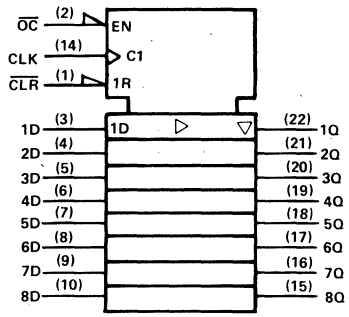
NC—No internal connection

logic symbols†

'ALS574A, 'AS574



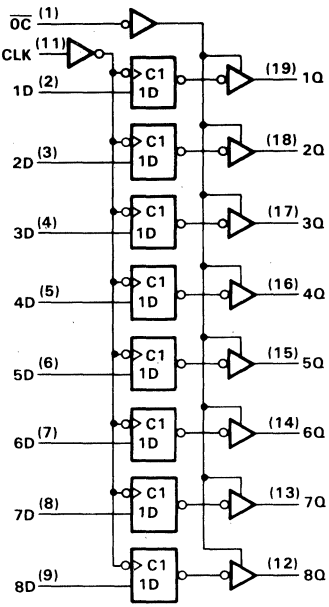
'ALS575A, 'AS575



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

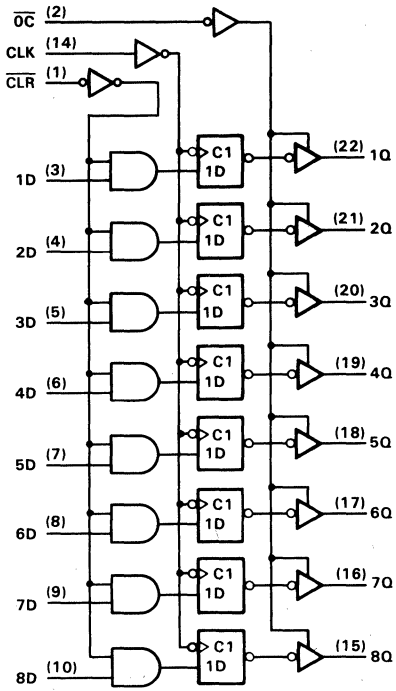
logic diagrams (positive logic)

'ALS574A, 'AS574



Pin numbers shown are for DW, J, and N packages.

'ALS575A, 'AS575



Pin numbers shown are for DW, JT, and NT packages.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS574A, SN54ALS575A . . . . . −55°C to 125°C
SN74ALS574A, SN74ALS575A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS574A SN54ALS575A			SN74ALS574A SN74ALS575A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−1			−2.6	mA
I_{OL}	Low-level output current				12			24	mA
f_{clock}	Clock frequency	'ALS574A	0		28	0		35	MHz
		'ALS575A	0		25	0		30	
t_w	Pulse duration	'ALS574A CLK high or low	16.5			14			ns
		'ALS575A CLK high or low	20			16.5			
t_{su}	Setup time before CLK↑	Data	15			15			ns
		'ALS575A $\overline{CLR}$	15			15			
t_h	Hold time after CLK↑	Data	4			0			ns
		'ALS575A $\overline{CLR}$	0			0			
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS574A SN54ALS575A			SN74ALS574A SN74ALS575A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS574A	V_{CC} = 5.5 V	Outputs high		11	18		11	18	mA
			Outputs low		17	27		17	27	
			Outputs disabled		17	28		17	28	
	'ALS575A		Outputs high		10	17		10	17	
			Outputs low		15	24		15	24	
			Outputs disabled		16	30		16	30	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS574A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C, 'ALS574A	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX, SN54ALS574A		SN74ALS574A		UNIT
			TYP	MIN	MAX	MIN	MAX	
f_{max}			50	28		35		MHz
t_{PLH}	CLK	Q	8	4	22	4	14	ns
t_{PHL}			8	4	17	4	14	
t_{PZH}	$\overline{OC}$	Q	9	4	21	4	18	ns
t_{PZL}			12	4	26	4	18	
t_{PHZ}	$\overline{OC}$	Q	5	2	16	2	10	ns
t_{PLZ}			5	2	25	2	12	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

'ALS575A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS575A			SN54ALS575A		SN74ALS575A		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			40	50		25		30		MHz
t_{PLH}	CLK	Q		8	11	4	15	4	14	ns
t_{PHL}				9	11.5	4	15	4	14	
t_{PZH}	$\overline{OC}$	Q		11	14	4	21	4	18	ns
t_{PZL}				12	15	4	21	4	18	
t_{PHZ}	$\overline{OC}$	Q		6	8	2	12	2	10	ns
t_{PLZ}				8	11	3	15	3	13	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54AS574, SN54AS575 . . . . . −55°C to 125°C
SN74AS574, SN74AS575 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

				SN54AS574 SN54AS575			SN74AS574 SN74AS575			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
I_{OH}	High-level output current					−12			−15	mA
I_{OL}	Low-level output current					32			48	mA
f_{clock}	Clock frequency			0		100	0		125	MHz
t_w	Pulse duration	CLK high		5			4			ns
		CLK low		4			2			
t_{su}	Setup time before CLK↑	Data		3			2			ns
		'AS575	$\overline{CLR}$ high or low	6.5			5.5			
t_h	Hold time after CLK↑	Data		3			2			ns
		'AS575	$\overline{CLR}$	0			0			
T_A	Operating free-air temperature			−55		125	0		70	°C

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS574 SN54AS575			SN74AS574 SN74AS575			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC} − 2			V_{CC} − 2			V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2					
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4	3.3		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.29	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.34	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	$\overline{OC}$, CLK, $\overline{CLR}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	D					−3			−2	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'AS574	V_{CC} = 5.5 V	Outputs high		73	116		73	116	mA
			Outputs low		85	134		85	134	
			Outputs disabled		84	134		84	134	
	'AS575		Outputs high		78	126		78	126	
			Outputs low		89	142		89	142	
			Outputs disabled		88	142		88	142	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS574 SN54AS575		SN74AS574 SN74AS575		
			MIN	MAX	MIN	MAX	
f_{max}			100		125		MHz
t_{PLH}	CLK	Any Q	3	11	3	8	ns
t_{PHL}			4	11	4	9	
t_{PZH}	$\overline{OC}$	Any Q	2	7	2	6	ns
t_{PZL}			3	11	3	10	
t_{PHZ}	$\overline{OC}$	Any Q	2	7	2	6	ns
t_{PLZ}			2	7	2	6	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

ALS and AS Circuits

OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

D2661, DECEMBER 1982 – REVISED MAY 1986

- **3-State Buffer-Type Inverting Outputs Drive Bus-Lines Directly**
- **Bus-Structured Pinout**
- **Buffered Control Inputs**
- **'ALS577A and 'AS577 Have Synchronous Clear**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

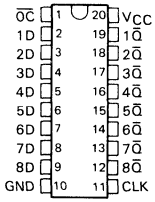
These 8-bit registers feature three-state outputs designed specifically for bus driving. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight-bit edge-triggered D-type flip-flops enter data on the low-to-high transition of the clock.

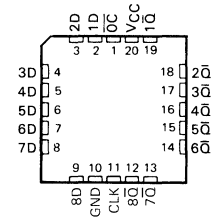
The output control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are off.

The SN54ALS' and SN54AS' devices are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS' and SN74AS' devices are characterized for operation from 0°C to 70°C.

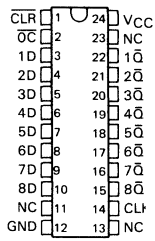
SN54ALS576A, SN54AS576 . . . J PACKAGE
SN74ALS576A, SN74AS576 . . . DW OR N PACKAGE
(TOP VIEW)



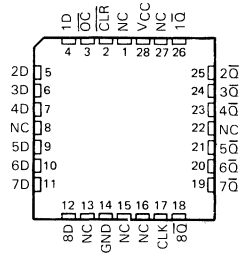
SN54ALS576A, SN54AS576 . . . FK PACKAGE
(TOP VIEW)



SN54ALS577A, SN54AS577 . . . JT PACKAGE
SN74ALS577A, SN74AS577 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54ALS577A, SN54AS577 . . . FK PACKAGE
SN74ALS577A, SN74AS577 . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLES

ALS576A, AS576

(Each Flip-Flop)

INPUTS			OUTPUT
$\overline{OC}$	CLK	D	$\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

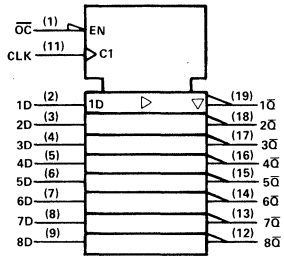
ALS577A, AS577

(Each Flip-Flop)

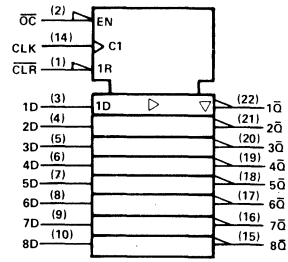
INPUTS				OUTPUT
$\overline{OC}$	$\overline{CLR}$	CLK	D	$\overline{Q}$
L	L	↑	X	H
L	H	↑	H	L
L	H	↑	L	H
L	H	L	X	$\overline{Q}_0$
H	X	X	X	Z

logic symbols†

'ALS576A, AS576



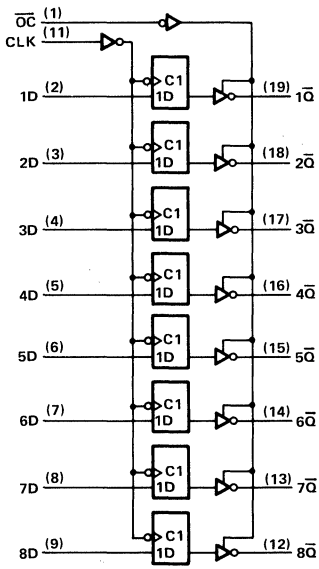
'ALS577A, 'AS577



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

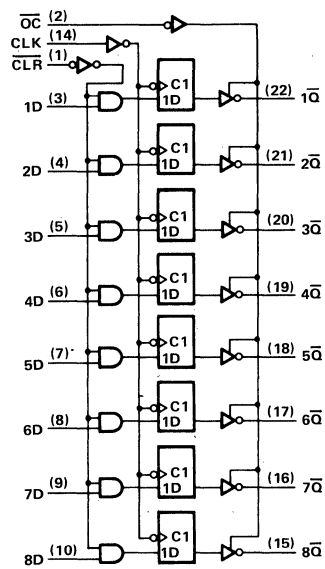
logic diagrams (positive logic)

'ALS576A, 'AS576



Pin numbers shown are for DW, J, and N packages.

'ALS577A, 'AS577



Pin numbers shown are for DW, JT and NT packages.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS', SN54AS' . . . . . −55°C to 125°C
SN74ALS', SN74AS' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS576A SN54ALS577A			SN74ALS576A SN74ALS577A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−1			−2.6	mA
I_{OL}	Low-level output current				12			24	mA
f_{clock}	Clock frequency	'ALS576A	0		25	0		30	MHz
		'ALS577A	0		25	0		30	
t_w	Pulse duration	CLK high or low 'ALS576A	20			16.5			ns
		CLK high or low 'ALS577A	20			16.5			
t_{su}	Setup time before CLK↑	Data	15			15			ns
		$\overline{CLR}$ ('ALS577A)	15			15			
t_h	Hold time after CLK↑	Data	4			0			ns
		$\overline{CLR}$ ('ALS577A)	4			0			
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS576A SN54ALS577A			SN74ALS576A SN74ALS577A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		10	18		10	18	mA
		Outputs low		15	24		15	24	
		Outputs disabled		16	30		16	30	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS576A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS576A			SN54ALS576A		SN74ALS576A		
			TYP			MIN	MAX	MIN	MAX	
f_{max}			50			25		30		MHz
t_{PLH}	CLK	Any $\overline{Q}$	9			4	15	4	14	ns
t_{PHL}			9			4	15	4	14	
t_{PZH}	$\overline{OC}$	Any $\overline{Q}$	11			4	21	4	18	ns
t_{PZL}			11			4	21	4	18	
t_{PHZ}	$\overline{OC}$	Any $\overline{Q}$ 'ALS576	6			2	12	2	10	ns
t_{PLZ}		Any $\overline{Q}$	8			3	17	3	15	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

'ALS577A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS577A			SN54ALS577A		SN74ALS577A		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			40	50		25		30		MHz
t_{PLH}	CLK	Any $\overline{Q}$		9	11	4	15	4	14	ns
t_{PHL}				9	11.5	4	15	4	14	
t_{PZH}	$\overline{OC}$	Any $\overline{Q}$		11	15	4	21	4	18	ns
t_{PZL}				11	15	4	21	4	18	
t_{PHZ}	$\overline{OC}$	Any $\overline{Q}$ 'ALS577		6	8	2	12	2	10	ns
t_{PLZ}		Any $\overline{Q}$		8	12	3	17	3	15	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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recommended operating conditions

			SN54AS576 SN54AS577			SN74AS576 SN74AS577			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−12			−15	mA
I_{OL}	Low-level output current				32			48	mA
f_{clock}	Clock frequency		0		100	0		125	MHz
t_w	Pulse duration	CLK high	5			4			ns
		CLK low	4			2			
t_{su}	Setup time before CLK↑	Data	3			2			ns
		$\overline{CLR}$ ('AS577)	6.5			5.5			
t_h	Hold time after CLK↑	Data	3			2			ns
		$\overline{CLR}$ ('AS577)	0			0			
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS576 SN54AS577			SN74AS576 SN74AS577			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC} − 2			V_{CC} − 2			V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2					
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4	3.3		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.29	0.5				V
		V_{CC} = 4.5 V	I_{OL} = 48 mA					0.33	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	D	V_{CC} = 5.5 V,	V_I = 0.4 V			−3			−2	mA
	All other					−0.5			−0.5	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'AS576	V_{CC} = 5.5 V	Outputs high		77	125		77	125	mA
			Outputs low		84	135		84	135	
			Outputs disabled		84	135		84	135	
	'AS577		Outputs high		78	126		78	126	
			Outputs low		76	123		76	123	
			Outputs disabled		88	142		88	142	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS576 SN54AS577		SN74AS576 SN74AS577		
			MIN	MAX	MIN	MAX	
f_{max}			100		125		MHz
t_{PLH}	CLK	Any $\overline{Q}$	3	11	3	8	ns
t_{PHL}			4	11	4	9	
t_{PZH}	$\overline{OC}$	Any $\overline{Q}$	2	7	2	6	ns
t_{PZL}			3	11	3	10	
t_{PHZ}	$\overline{OC}$	Any $\overline{Q}$	2	7	2	6	ns
t_{PLZ}			2	7	2	6	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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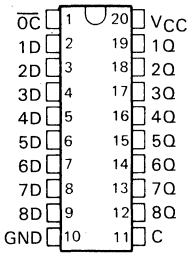
D2661, DECEMBER 1982 – REVISED MAY 1986

- 3-State Buffer-Type Outputs Drive Bus-Lines Directly
- Bus-Structured Pinout
- Choice of True or Inverting Logic

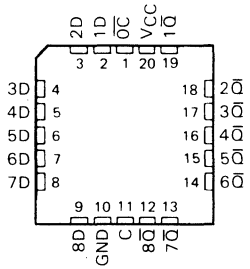
'ALS573, 'AS573	True Outputs
'ALS580, 'AS580	Inverting Outputs

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS580, SN54AS580 . . . J PACKAGE
SN74ALS580, SN74AS580 . . . DW OR N PACKAGE
(TOP VIEW)



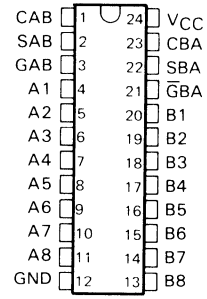
SN54ALS580, SN54AS580 . . . FK PACKAGE
(TOP VIEW)



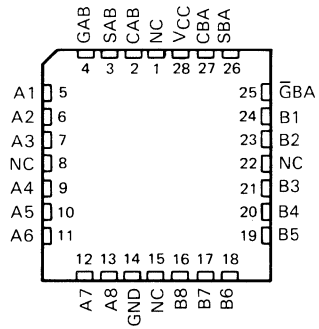
For complete information on the SN54ALS580, SN54AS580, SN74ALS580 and SN74AS580, see page 2-435.

- **Bus Transceivers/Registers**
- **Independent Registers and Enables for A and B Buses**
- **Multiplexed Real-Time and Stored Data**
- **Choice of True and Inverting Data Paths**
  'ALS614 . . . Inverting logic
  'ALS615 . . . True logic
- **Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

DW OR NT PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NC—No internal connection

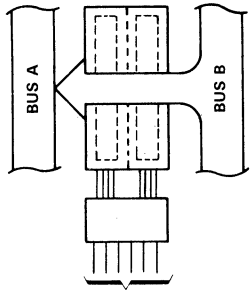
description

These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Enable GAB and $\overline{G}$BA are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether real-time or stored data is transferred. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input level selects real-time data, and a high selects stored data. The following examples demonstrate the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and $\overline{G}$BA. In this configuration each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

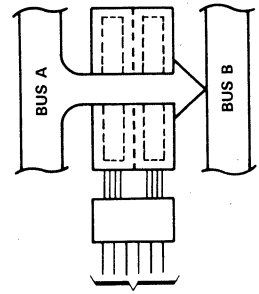
The -1 versions of the SN74ALS614 and SN74ALS615 are identical to the standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes.

The SN74ALS614 and SN74ALS615 are characterized for operation from 0°C to 70°C.



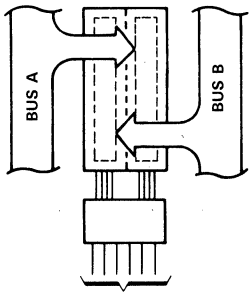
GAB	$\overline{G}$BA	CAB	CBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



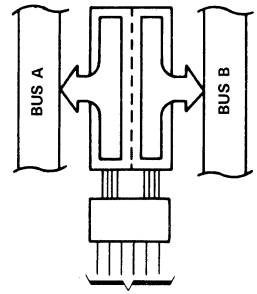
GAB	$\overline{G}$BA	CAB	CBA	SAB	SBA
H	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



GAB	$\overline{G}$BA	CAB	CBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

STORAGE FROM
A AND/OR B



GAB	$\overline{G}$BA	CAB	CBA	SAB	SBA
H	L	H or L	H or L	H	H

TRANSFER
STORED DATA
TO A AND/OR B

FUNCTION TABLE

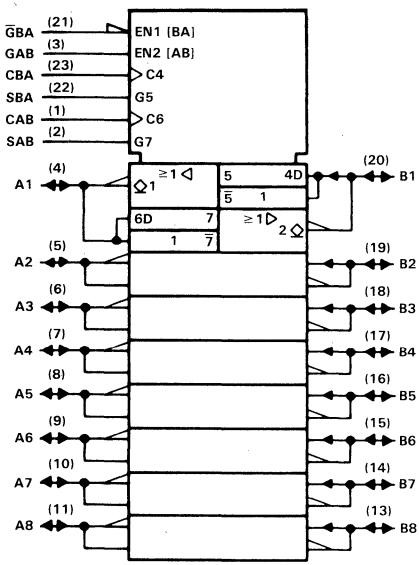
INPUTS						DATA I/O		OPERATION OR FUNCTION	
GAB	$\overline{GBA}$	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	SN74ALS614	SN74ALS615
L	H	H or L	H or L	X	X	Input	Input	Isolation	Isolation
L	H	↑	↑	X	X			Store A and B Data	Store A and B Data
X	H	↑	H or L	X	X	Input	Unspecified†	Store A, Hold B	Store A, Hold B
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers	Store A in both registers
L	X	H or L	↑	X	X	Unspecified†	Input	Hold A, Store B	Hold A, Store B
L	L	↑	↑	X	X‡	Output	Input	Store B in both registers	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-Time $\overline{B}$ Data to A Bus	Real-Time B Data to A bus
L	L	X	H or L	X	H			Stored $\overline{B}$ Data to A Bus	Stored B data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time $\overline{A}$ Data to B Bus	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored $\overline{A}$ Data to B Bus	Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{A}$ Data to B Bus and Stored $\overline{B}$ Data to A Bus	Stored A Data to B Bus and Stored B Data to A Bus

† The data output functions may be enabled or disabled by various signals at the GAB or $\overline{GBA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

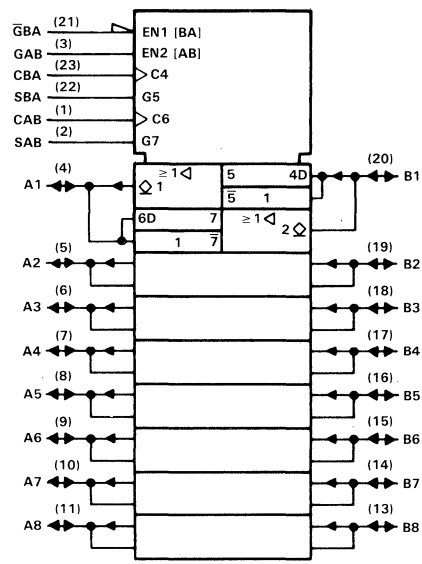
‡ Select control = L: clocks can occur simultaneously.
Select control = H: clocks must be staggered in order to load both registers.

logic symbols†

SN74ALS614



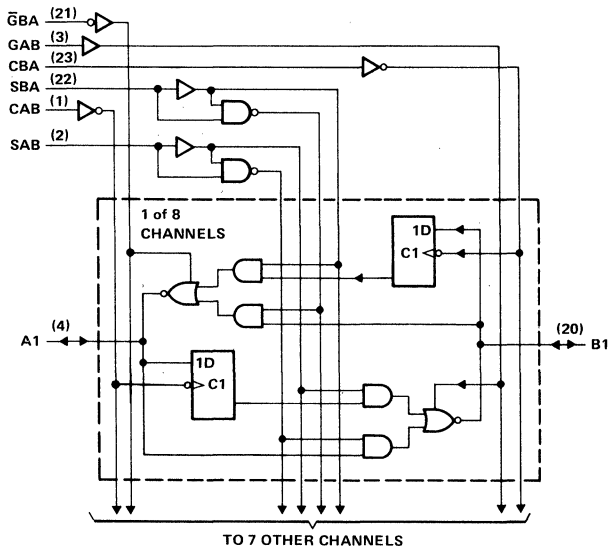
SN74ALS615



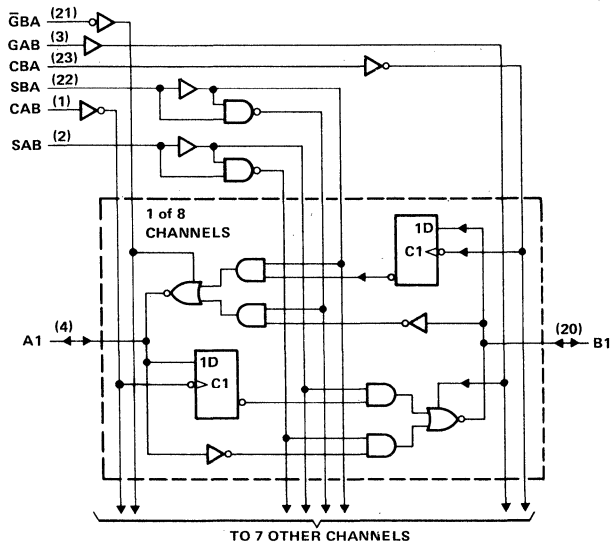
† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW and NT packages.

logic diagrams (positive logic)

SN74ALS614



SN74ALS615



Pin numbers shown are for DW and NT packages.

TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{OH}	High-level output voltage				5.5	V
I_{OL}	Low-level output current				24	mA
					48†	
t_w	Pulse duration	CBA or CAB high	16.5			ns
		CBA or CAB low	16.5			
t_{su}	Setup time before CAB↑ or CBA↑	A or B	10			ns
t_h	Hold time after CAB↑ or CBA↑	A or B	0			ns
T_A	Operating free-air temperature		0		70	°C

†The extended condition applies if V_{CC} is maintained between 4.75 V and 5.25 V. The 48-mA limit applies for the SN74ALS614-1 and SN74ALS615-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
I_{OH}		V_{CC} = 4.5 V,	V_{OH} = 5.5 V				0.1	mA
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA			0.25	0.4	V
		V_{CC} = 4.75 V, (I_{OL} = 48 mA for -1 versions)	I_{OL} = 24 mA			0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V				0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V				0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V				20	μA
	A or B ports§						20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V				−0.2	mA
	A or B ports§						−0.2	
I_{CC}	'ALS614	V_{CC} = 5.5 V		Outputs high		52	60	mA
				Outputs low		57	70	
	'ALS615			Output high		40	60	mA
				Output low		48	72	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

SN74ALS614 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 680 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = 0°C to 70°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	CBA or CAB	A or B		37	52	20	64	ns
t_{PHL}				14	19	6	20	
t_{PLH}	A or B	B or A		31	42	14	51	ns
t_{PHL}				6	10	2	12	
t_{PLH}	$\overline{SBA}$ or $\overline{SAB}$† (with A or B high)	A or B		35	47	19	58	ns
t_{PHL}				12	20	5	22	
t_{PLH}	$\overline{SBA}$ or $\overline{SAB}$† (with A or B low)	A or B		35	47	19	58	ns
t_{PHL}				12	20	5	22	
t_{PLH}	$\overline{G}$BA or GAB	A or B		16	22	9	27	ns
t_{PHL}				12	18	6	22	

SN74ALS615 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 680 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = 0°C to 70°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	CBA or CAB	A or B		33	50	19	64	ns
t_{PHL}				14	20	6	22	
t_{PLH}	A or B	B or A		28	44	12	56	ns
t_{PHL}				11	17	4	20	
t_{PLH}	$\overline{SBA}$ or $\overline{SAB}$† (with A or B high)	A or B		35	50	19	62	ns
t_{PHL}				15	22	5	25	
t_{PLH}	$\overline{SBA}$ or $\overline{SAB}$† (with A or B low)	A or B		35	50	19	62	ns
t_{PHL}				15	22	5	25	
t_{PLH}	$\overline{G}$BA or GAB	A or B		17	23	6	27	ns
t_{PHL}				14	20	6	24	

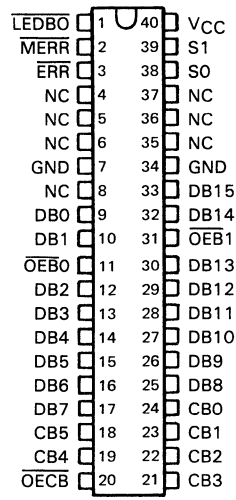
†These parameters are measured with the internal output state of the storage register opposite to that of the bus input.
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2840, APRIL 1984—REVISED MAY 1986

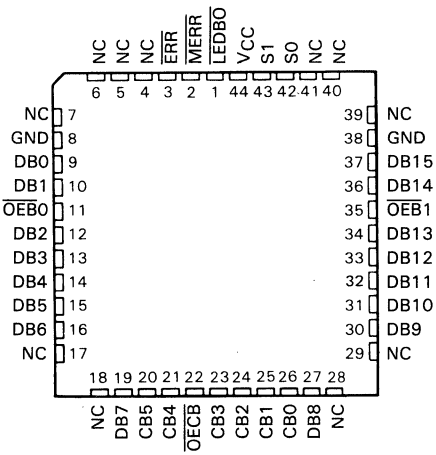
- **Detects and Corrects Single-Bit Errors**
- **Detects and Flags Dual-Bit Errors**
- **Built-In Diagnostic Capability**
- **Fast Write and Read Cycle Processing Times**
- **Byte-Write Capability**
- **Dependable Texas Instruments Quality and Reliability**

DEVICE	OUTPUT
'ALS616	3-State
'ALS617	Open-Collector

SN54ALS616, SN54ALS617 . . . JD PACKAGE
SN74ALS616, SN74ALS617 . . . JD OR N PACKAGE
(TOP VIEW)



SN74ALS616, SN74ALS617 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

The 'ALS616 and 'ALS617 are 16-bit parallel error detection and correction circuits in 40-pin, 600-mil packages. The EDACs use a modified Hamming code to generate a 6-bit check word from a 16-bit data word. This check word is stored along with the data word during the memory write cycle. During memory read cycles, the 22-bit words from memory are processed by the EDACs to determine if errors have occurred in memory.

Single-bit errors in the 16-bit data word are flagged and corrected. Single-bit errors in the 6-bit check word are flagged, but the data word will remain unaltered. The 6-bit error syndrome code will pinpoint the error-generating location.

Dual-bit errors are flagged but not corrected. These errors may occur in any two bits of the 22-bit word from memory. The gross-error condition of all lows or all highs from memory will be detected. Otherwise, errors in three or more bits of the 22-bit word are beyond the capabilities of these devices to detect.

Read-modify-write (byte-control) operations can be performed with the 'ALS616 and 'ALS617 EDACs by using output latch enable, $\overline{\text{LEDBO}}$, and individual $\overline{\text{OEB0}}$ and $\overline{\text{OEB1}}$ byte control pins.

Diagnostics are performed on the EDACs by controls and internal paths that allow the user to read the contents of the DB and CB input latches. These will determine if the failure occurred in memory or in the EDAC.

The SN54ALS616 and SN54ALS617 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS616 and SN74ALS617 are characterized for operation from 0°C to 70°C.

TABLE 1. WRITE CONTROL FUNCTION

MEMORY CYCLE	EDAC FUNCTION	CONTROL S1	CONTROL S0	DATA I/O	DB CONTROL $\overline{OEB0}$ & $\overline{OEB1}$	DB OUTPUT LATCH $\overline{LEDBO}$	CHECK I/O	CB CONTROL $\overline{OECB}$	ERROR FLAGS $\overline{ERR}$	ERROR FLAGS $\overline{MERR}$
Write	Generate check word	L	L	Input	H	X	Output check bits†	L	H	H

†See Table 2 for details on check bit generation.

memory write cycle details

During a memory write cycle, the check bits (CB0 thru CB5) are generated internally in the EDAC by six 8-input parity generators using the 16-bit data word as defined in Table 2. These six check bits are stored in memory along with the original 16-bit data word. This 22-bit word will later be used in the memory read cycle for error detection and correction.

TABLE 2. PARITY ALGORITHM

CHECK WORD BIT	16-BIT DATA WORD 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CB0			X		X	X	X			X			X		X	X
CB1		X		X		X	X	X				X		X		X
CB2	X			X	X			X	X		X			X	X	
CB3	X	X	X				X	X			X	X	X			
CB4	X	X	X	X	X	X			X	X						
CB5									X	X	X	X	X	X	X	X

The six check bits are parity bits derived from the matrix of data bits as indicated by "X" for each bit.

error detection and correction details

During a memory read cycle, the 6-bit check word is retrieved along with the actual data. In order to be able to determine whether the data from memory is acceptable to use as presented to the bus, the error flags must be tested to determine if they are at the high level.

The first case in Table 3 represents the normal, no-error conditions. The EDAC presents highs on both flags. The next two cases of single-bit errors give a high on $\overline{MERR}$ and a low on $\overline{ERR}$, which is the signal for a correctable error, and the EDAC should be sent through the correction cycle. The last three cases of double-bit errors will cause the EDAC to signal lows on both $\overline{ERR}$ and $\overline{MERR}$, which is the interrupt indication for the CPU.

TABLE 3. ERROR FUNCTION

TOTAL NUMBER OF ERRORS 16-BIT DATA WORD	6-BIT CHECK WORD	ERROR FLAGS $\overline{ERR}$	ERROR FLAGS $\overline{MERR}$	DATA CORRECTION
0	0	H	H	Not applicable
1	0	L	H	Correction
0	1	L	H	Correction
1	1	L	L	Interrupt
2	0	L	L	Interrupt
0	2	L	L	Interrupt

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TABLE 4. READ, FLAG, AND CORRECT FUNCTION

MEMORY CYCLE	EDAC FUNCTION	CONTROL S1	CONTROL S0	DATA I/O	DB CONTROL $\overline{OEB0}$ & $\overline{OEB1}$	DB OUTPUT LATCH $\overline{LEDB0}$	CHECK I/O	CB CONTROL $\overline{OECB}$	ERROR FLAGS $\overline{ERR}$ $\overline{MERR}$
Read	Read & flag	H	L	Input	H	X	Input	H	Enabled†
Read	Latch input data & check bits	H	H	Latched input data	H	L	Latched input check word	H	Enabled†
Read	Output corrected data and syndrome bits	H	H	Output corrected data word	L	X	Output syndrome bits‡	L	Enabled†

†See Table 3 for error description.
‡See Table 5 for error location.

Error detection is accomplished as the 6-bit check word and the 16-bit data word from memory are applied to the internal parity generators/checkers. If the parity of all six groupings of data and check bits are correct, it is assumed that no error has occurred and both error flags will be high.

If the parity of one or more of the check groups is incorrect, an error has occurred and the proper error flag or flags will be set low. The two-bit error is not correctable since the parity tree can only identify single-bit errors. Both error flags are set low when any two-bit error is detected.

Three or more simultaneous bit errors can cause the EDAC to believe that no error, a correctable error, or an uncorrectable error has occurred and will produce erroneous results in all three cases. It should be noted that the gross-error conditions of all highs will be detected.

As the corrected word is made available on the data I/O port (DB0 thru DB15), the check word I/O port (CB0 thru CB5) presents a 6-bit syndrome error code. This syndrome code can be used to locate the bad memory chip. See Table 5 for syndrome decoding.

TABLE 5. SYNDROME DECODING

SYNDROME BITS						ERROR
5	4	3	2	1	0	
L	L	L	L	L	L	2-bit
L	L	L	L	L	H	unc
L	L	L	L	H	L	unc
L	L	L	L	H	H	2-bit
L	L	L	H	L	L	unc
L	L	L	H	L	H	2-bit
L	L	L	H	H	L	2-bit
L	L	L	H	H	H	unc
L	L	H	L	L	L	unc
L	L	H	L	L	H	2-bit
L	L	H	L	H	L	2-bit
L	L	H	L	H	H	DB7
L	L	H	H	L	L	2-bit
L	L	H	H	L	H	unc
L	L	H	H	H	L	DB6
L	L	H	H	H	H	2-bit

SYNDROME BITS						ERROR
5	4	3	2	1	0	
L	H	L	L	L	L	unc
L	H	L	L	L	H	2-bit
L	H	L	L	H	L	2-bit
L	H	L	L	H	H	DB5
L	H	L	H	L	L	2-bit
L	H	L	H	L	H	DB4
L	H	L	H	H	L	DB3
L	H	L	H	H	H	2-bit
L	H	H	L	L	L	2-bit
L	H	H	L	L	H	DB2
L	H	H	L	H	L	DB1
L	H	H	L	H	H	2-bit
L	H	H	H	L	L	DB0
L	H	H	H	L	H	2-bit
L	H	H	H	H	L	2-bit
L	H	H	H	H	H	CB5

SYNDROME BITS						ERROR
5	4	3	2	1	0	
H	L	L	L	L	L	unc
H	L	L	L	L	H	2-bit
H	L	L	L	H	L	2-bit
H	L	L	L	H	H	DB15
H	L	L	H	L	L	2-bit
H	L	L	H	L	H	DB14
H	L	L	H	H	L	DB13
H	L	L	H	H	H	2-bit
H	L	H	L	L	L	2-bit
H	L	H	L	L	H	DB12
H	L	H	L	H	L	DB11
H	L	H	L	H	H	2-bit
H	L	H	H	L	L	DB10
H	L	H	H	L	H	2-bit
H	L	H	H	H	L	2-bit
H	L	H	H	H	H	CB4

SYNDORME BITS						ERROR
5	4	3	2	1	0	
H	H	L	L	L	L	2-bit
H	H	L	L	L	H	DB8
H	H	L	L	H	L	unc
H	H	L	L	H	H	2-bit
H	H	L	H	L	L	DB9
H	H	L	H	L	H	2-bit
H	H	L	H	H	L	2-bit
H	H	L	H	H	H	CB3
H	H	H	L	L	L	unc
H	H	H	L	L	H	2-bit
H	H	H	L	H	L	2-bit
H	H	H	L	H	H	CB2
H	H	H	H	L	L	2-bit
H	H	H	H	L	H	CB1
H	H	H	H	H	L	CB0
H	H	H	H	H	H	none

CB X = error in check bit X
DB Y = error in data bit Y
2-bit = double-bit error
unc = uncorrectable multibit error

read-modify-write (byte control) operations

The 'ALS616 and 'ALS617 devices are capable of byte-write operations. The 22-bit word from memory must first be latched into the DB and CB input latches. This is easily accomplished by switching from the read and flag mode (S1 = H, S0 = L) to the latch input mode (S1 = H, S0 = H). The EDAC will then make any corrections, if necessary, to the data word and place it at the input of the output data latch. This data word must then be latched into the output data latch by taking $\overline{\text{LEDBO}}$ from a low to a high.

Byte control can now be employed on the data word through the $\overline{\text{OEB0}}$ or $\overline{\text{OEB1}}$ controls. $\overline{\text{OEB0}}$ controls DB0-DB7 (byte 0), $\overline{\text{OEB1}}$ controls DB8-DB15 (byte 1).

Placing a high on the byte control will disable the output and the user can modify the byte. If a low is placed on the byte control, then the original byte is allowed to pass onto the data bus unchanged. If the original data word is altered through byte control, a new check word must be generated before it is written back into memory. This is easily accomplished by taking control S1 and S0 low. Table 6 lists the read-modify-write functions.

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TABLE 6. READ-MODIFY-WRITE FUNCTION

MEMORY CYCLE	EDAC FUNCTION	CONTROL S1	CONTROL S0	BYTEn†	$\overline{OEBn}$†	DB OUTPUT LATCH $\overline{LEDBO}$	CHECK I/O	CB CONTROL	ERROR FLAG $\overline{ERR}$	ERROR FLAG $\overline{MERR}$
Read	Read & Flag	H	L	Input	H	X	Input	H	Enabled	
Read	Latch input data & check bits	H	H	Latched Input data	H	L	Latched input check word	H	Enabled	
Read	Latch corrected data word into output latch	H	H	Latched output data word	H	H	Hi-Z Output Syndrome bits	H L	Enabled	
Modify/ write	Modify appropriate byte or bytes & generate new check word	L	L	Input modified $\overline{BYTE0}$ Output unchanged BYTE0	H L	H	Output check word	L	H	H

†$\overline{OEB0}$ controls DB0-DB7 (BYTE0), $\overline{OEB1}$ controls DB8-DB15 (BYTE1)

diagnostic operations

The 'ALS616 and 'ALS617 are capable of diagnostics that allow the user to determine whether the EDAC or the memory is failing. The diagnostic function tables will help the user to see the possibilities for diagnostic control.

In the diagnostic mode (S1 = L, S0 = H), the checkword is latched into the input latch while the data input latch remains transparent. This lets the user apply various data words against a fixed known checkword. If the user applies a diagnostic data word with an error in any bit location, the $\overline{ERR}$ flag should be low. If a diagnostic data word with two errors in any bit location is applied, the $\overline{MERR}$ flag should be low. After the checkword is latched into the input latch, it can be verified by taking $\overline{OECB}$ low. This outputs the latched checkword. The diagnostic data word can be latched into the output data latch and verified via the $\overline{LEDBO}$ control pin. By changing from the diagnostic mode (S1 = L, S0 = H), the user can verify that the EDAC will correct the diagnostic data word. Also, the syndrome bits can be produced to verify that the EDAC pinpoints the error location. Table 7 lists the diagnostic functions.

TABLE 7. DIAGNOSTIC FUNCTION

EDAC FUNCTION	CONTROL S1	CONTROL S0	DATA I/O	DB BYTE CONTROL $\overline{OEBn}$	DB OUTPUT LATCH $\overline{LEDBO}$	CHECK I/O	CB CONTROL $\overline{OECB}$	ERROR FLAGS $\overline{ERR}$	ERROR FLAGS $\overline{MERR}$
Read & flag	H	L	Input correct data word	H	X	Input correct check bits	H	H	H
Latch input check word while data input latch remains transparent	L	H	Input diagnostic data word†	H	L	Latched input check bits	H	Enabled	
Latch diagnostic data word into output latch	L	H	Input diagnostic data word†	H	H	Output latched check bits	L	Enabled	
						Hi-Z	H		
Latch diagnostic data word into input latch	H	H	Latched input diagnostic data word	H	H	Output syndrome bits	L	Enabled	
						Hi-Z	H		
Output diagnostic data word & syndrome bits	H	H	Output diagnostic data word	L	H	Output syndrome bits	L	Enabled	
						Hi-Z	H		
Output corrected diagnostic data word & output syndrome bits	H	H	Output corrected diagnostic data word	L	L	Output syndrome bits	L	Enabled	
						Hi-Z	H		

†Diagnostic data is a data word with an error in one bit location except when testing the $\overline{MERR}$ error flag. In this case, the diagnostic data word will contain errors in two bit locations.

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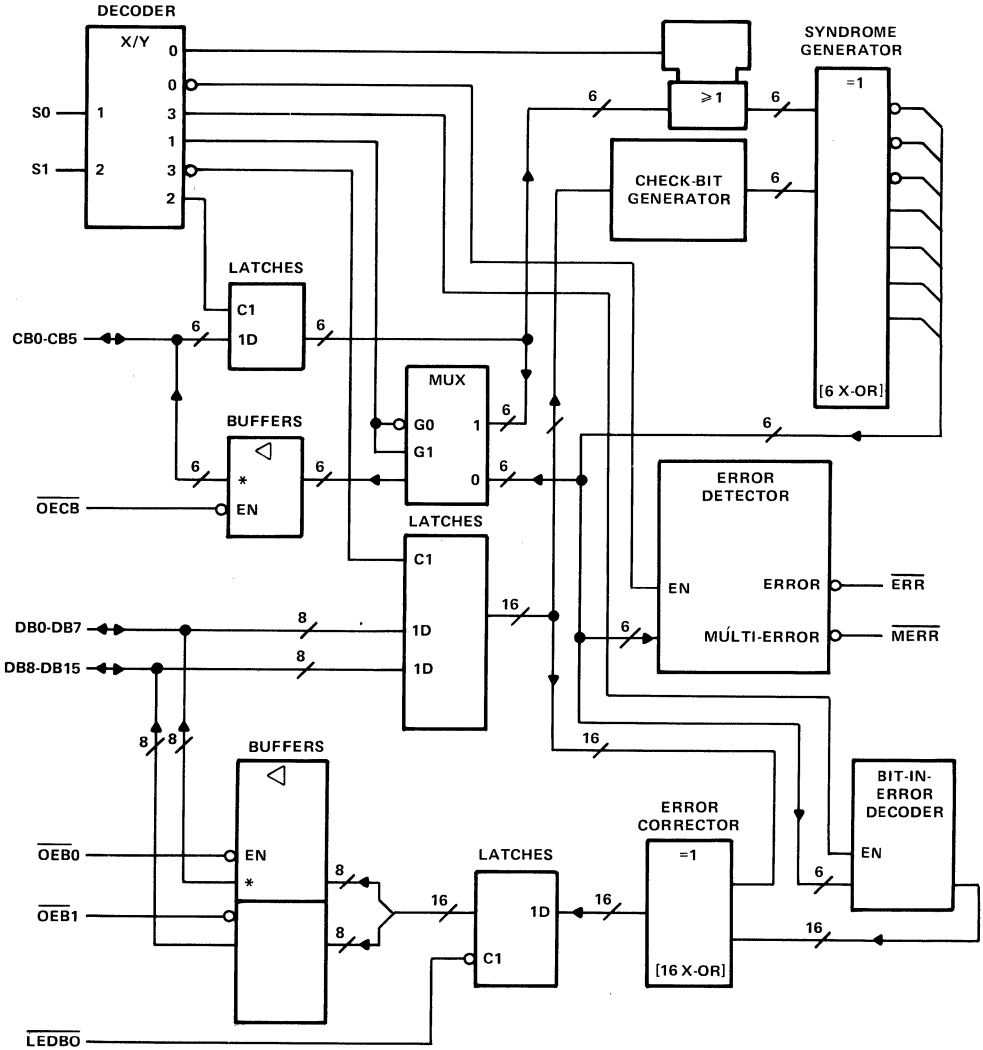
logic diagram (positive logic)



*'ALS616 has 3-state (▽) check-bit and data outputs.
'ALS617 has open-collector(◇) check-bit and data outputs.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: CB and DB . . . . . 5.5 V
All others . . . . . 7 V
Operating case temperature range SN54ALS616, SN54ALS617, ... −55°C to 125°C
Operating free-air temperature range, SN74ALS616, SN74ALS617 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

				SN54ALS616 SN54ALS617			SN74ALS616 SN74ALS617			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{OH}	High-level output voltage	DB or CB	'ALS617			5.5			5.5	V
I_{OH}	High-level output current	$\overline{ERR}$ or $\overline{MERR}$				−0.4			−0.4	mA
		DB or CB	'ALS616			−1			−2.6	
I_{OL}	Low-level output current	$\overline{ERR}$ or $\overline{MERR}$				4			8	mA
		DB or CB				12			24	
t_w	Pulse duration	$\overline{LEDBO}$ low		45			25			ns
t_{su}	Setup time	(1) Data and check word before S0↑ (S1 = H)		15			12			ns
		(2) S0 high before $\overline{LEDBO}$↑ (S1 = H)†		45			45			
		(3) $\overline{LEDBO}$ high before the earlier of S0↓ or S1↓†		0			0			
		(4) $\overline{LEDBO}$ high before S1↑ (S0 = H)		0			0			
		(5) Diagnostic data word before S1↑ (S0 = H)		28			12			
		(6) Diagnostic check word before the later of S1↓ or S0↑		15			12			
		(7) Diagnostic data word before $\overline{LEDBO}$↑ (S1 = L and S0 = H)†		35			20			
t_h	Hold time	(8) Read-mode, S0 low and S1 high		35			30			ns
		(9) Data and check word after S0↑ (S1 = H)		20			15			
		(10) Data word after S1↑ (S0 = H)		20			15			
		(11) Check word after the later of S1↓ or S0↑		20			15			
		(12) Diagnostic data word after $\overline{LEDBO}$↑ (S1 = L, S0 = H)‡		0			0			
t_{corr}	Correction time (see Figure 1)			70			65			ns
T_C	Operating case temperature			−55		125				°C
T_A	Operating free-air temperature						0		70	°C

†These times ensure that corrected data is saved in the output data latch.
‡These times ensure that the diagnostic data word is saved in the output data latch.

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'ALS616 electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS616			SN74ALS616			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	All outputs	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	DB or CB	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	$\overline{ERR}$ or $\overline{MERR}$	V_{CC} = 4.5 V,	I_{OH} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
	DB or CB	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	S0 or S1	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	DB or CB	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	S0 or S1	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	DB or CB‡					20			20	
I_{IL}	S0 or S1	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.4			−0.4	mA
	DB or CB‡					−0.1			−0.1	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	See Note 1		110	190		110	170	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with S0 and S1 at 4.5 V and all CB and DB pins grounded.

'ALS616 switching characteristics, V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, T_C = −55°C to 125°C for SN54ALS616, T_A = 0°C to 70°C for SN74ALS616

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ALS616		SN74ALS616		UNIT
				MIN	MAX	MIN	MAX	
t_{pd}	DB and CB	$\overline{ERR}$	S1 = H, S0 = L, R_L = 500 Ω	10	43	10	40	ns
	DB	$\overline{ERR}$	S1 = L, S0 = H, R_L = 500 Ω	10	43	10	40	
t_{pd}	DB and CB	$\overline{MERR}$	S1 = H, S0 = L, R_L = 500 Ω	15	65	15	55	ns
	DB	$\overline{MERR}$	S1 = L, S0 = H, R_L = 500 Ω	15	65	15	55	
t_{pd}	S0↓ and S1↓	CB	R1 = R2 = 500 Ω	10	60	10	49	ns
t_{pd}	DB	CB	S1 = L, S0 = L, R1 = R2 = 500 Ω	10	60	10	49	ns
t_{pd}	$\overline{LEDBO}$↓	DB	S1 = X, S0 = H, R1 = R2 = 500 Ω	7	35	7	30	ns
t_{pd}	S1↑	CB	S0 = H, R1 = R2 = 500 Ω	10	50	10	50	ns
t_{en}	$\overline{OECB}$↓	CB	S0 = H, S1 = X, R1 = R2 = 500 Ω	2	30	2	27	ns
t_{dis}	$\overline{OECB}$↑	CB	S0 = H, S1 = X, R1 = R2 = 500 Ω	2	30	2	27	ns
t_{en}	$\overline{OEB0}$ and $\overline{OEB1}$↓	DB	S0 = H, S1 = X, R1 = R2 = 500 Ω	2	30	2	27	ns
t_{dis}	$\overline{OEB0}$ and $\overline{OEB1}$↑	DB	S0 = H, S1 = X, R1 = R2 = 500 Ω	2	30	2	27	ns

'ALS617 electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS617			SN74ALS617			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	$\overline{ERR}$ or $\overline{MERR}$	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
I_{OH}	DB or CB	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	$\overline{ERR}$ or $\overline{MERR}$	V_{CC} = 4.5 V,	I_{OH} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
	DB or CB	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	S0 or S1	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	DB or CB	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	S0 or S1	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	DB or CB‡					20			20	
I_{IL}	S0 or S1	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.4			−0.4	mA
	DB or CB‡					−0.1			−0.1	
I_O§	$\overline{ERR}$ or $\overline{MERR}$	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	See Note 1		110			110		mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with S0 and S1 at 4.5 V and all CB and DB pins grounded.

'ALS617 switching characteristics, V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, T_C = −55°C to 125°C for SN54ALS617, T_A = 0°C to 70°C for SN74ALS617

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ALS617			SN74ALS617			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{pd}	DB and CB	$\overline{ERR}$	S1 = H, S0 = L, R_L = 500 Ω		26			26		ns
	DB	$\overline{ERR}$	S1 = L, S0 = H, R_L = 500 Ω		26			26		
t_{pd}	DB and CB	$\overline{MERR}$	S1 = H, S0 = L, R_L = 500 Ω		40			40		ns
			S1 = L, S0 = H, R_L = 500 Ω		40			40		
t_{pd}	S0↓ and S1↓	CB	R_L = 680 Ω		40			40		ns
t_{pd}	DB	CB	S1 = L, S0 = L, R_L = 680 Ω		40			40		ns
t_{pd}	$\overline{LEDBO}$↓	DB	S1 = X, S0 = H, R_L = 680 Ω		26			26		ns
t_{pd}	S1↑	CB	S0 = H, R_L = 680 Ω		40			40		ns
t_{PLH}	$\overline{OECB}$↑	CB	S1 = X, S0 = H, R_L = 680 Ω		24			24		ns
t_{PHL}	$\overline{OECB}$↓	CB	S1 = X, S0 = H, R_L = 680 Ω		24			24		ns
t_{PLH}	$\overline{OEB0}$ and $\overline{OEB1}$↑	DB	S1 = X, S0 = H, R_L = 680 Ω		24			24		ns
t_{PHL}	$\overline{OEB0}$ and $\overline{OEB1}$↓	DB	S1 = X, S0 = H, R_L = 680 Ω		24			24		ns

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

Additional information on these products can be obtained from the factory as it becomes available.

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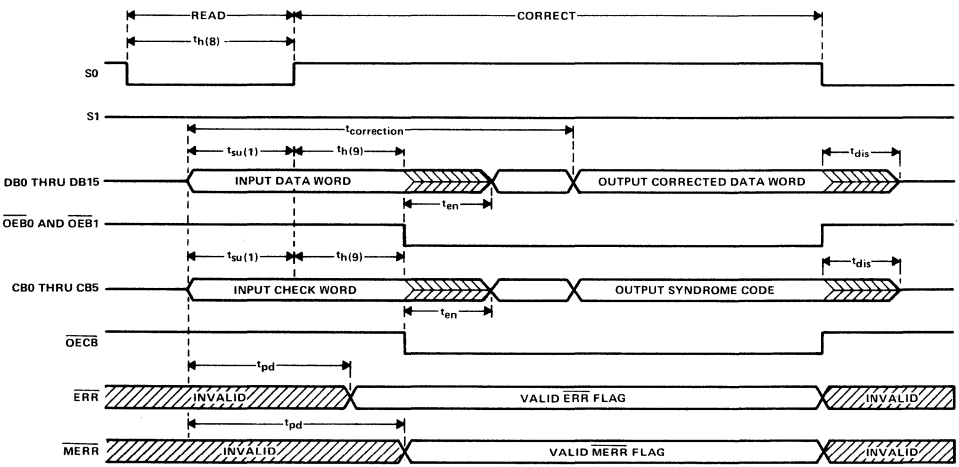

FIGURE 1. READ, FLAG, AND CORRECT MODE SWITCHING WAVEFORMS

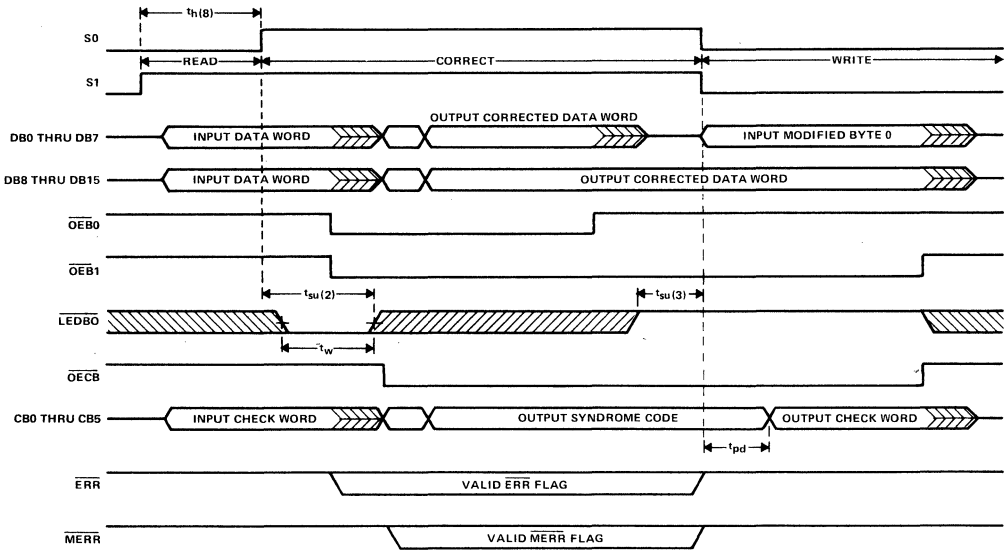

FIGURE 2. READ, CORRECT, MODIFY MODE SWITCHING WAVEFORMS

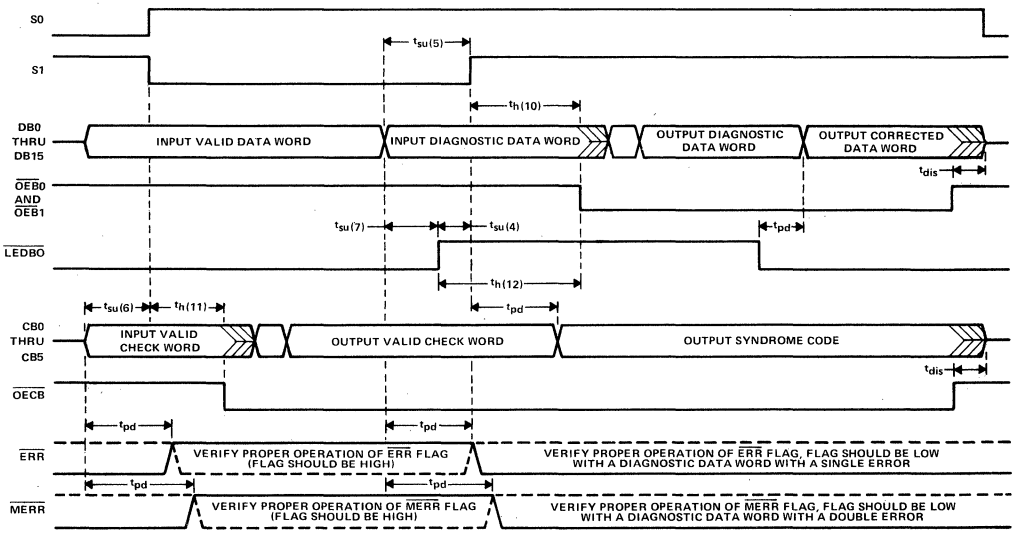

FIGURE 3. DIAGNOSTIC MODE SWITCHING WAVEFORM

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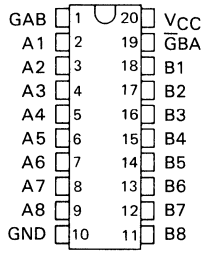
D2661, DECEMBER 1982 – REVISED MAY 1986

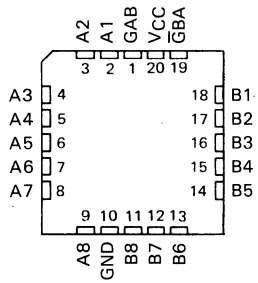
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Local Bus-Latch Capability**
- **Choice of True or Inverting Logic**
- **Choice of 3-State or Open-Collector Outputs**
- **Dependable Texas Instruments Quality and Reliability**

DEVICE	OUTPUT	LOGIC
'ALS620A, 'AS620	3-State	Inverting
'ALS621A, 'AS621	Open-Collector	True
'ALS622A, 'AS622	Open-Collector	Inverting
'ALS623A, 'AS623	3-State	True

SN54ALS', SN54AS' . . . J PACKAGE
SN74ALS', SN74AS' . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS', SN54AS' . . . FK PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs ($\overline{G}$BA and GAB).

The enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives the octal bus transceivers the capability to store data by simultaneous enabling of $\overline{G}$BA and GAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states. The 8-bit codes appearing on the two sets of buses will be identical for the 'ALS621A, 'AS621 and 'ALS623A, 'AS623 or complementary for the 'ALS620A, 'AS620 and 'ALS622A, 'AS622.

The -1 versions of the SN74ALS' parts are identical to their standard versions except that the recommended maximum I_{OL} is increased to 48 mA. There are no -1 versions of the SN54ALS' parts.

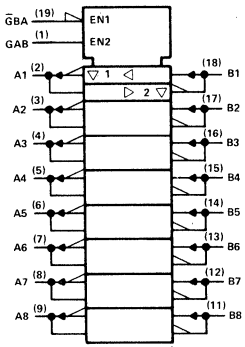
The SN54' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

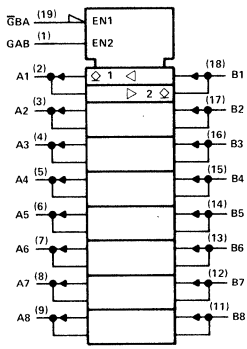
ENABLE INPUTS		OPERATION	
$\overline{G}$BA	GAB	'ALS620A, 'ALS622A 'AS620, 'AS622	'ALS621A, 'ALS623A 'AS621, 'AS623
L	L	$\overline{B}$ data to A bus	B data to A bus
H	H	$\overline{A}$ data to B bus	A data to B bus
H	L	Isolation	Isolation
L	H	$\overline{B}$ data to A bus, $\overline{A}$ data to B bus	B data to A bus, A data to B bus

logic symbols†

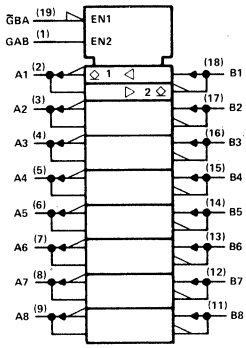
'ALS620A, 'AS620



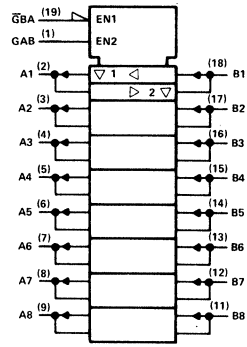
'ALS621A, 'AS621



'ALS622A, 'AS622



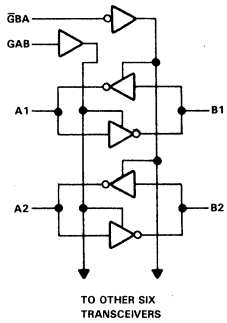
'ALS623A, 'AS623



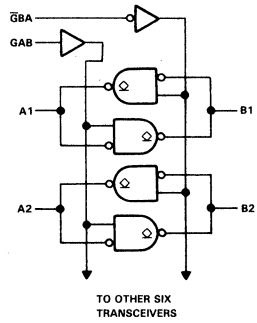
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

logic diagrams (positive logic)

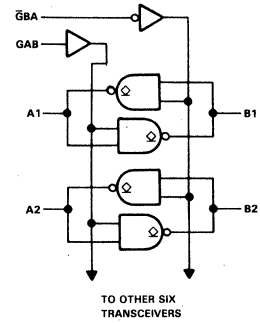
'ALS620A, 'AS620



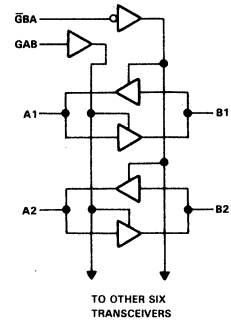
'ALS621A, 'AS621



'ALS622A, 'AS622



'ALS623A, 'AS623



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS620A, SN54ALS623A . . . . . −55°C to 125°C
SN74ALS620A, SN74ALS623A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS620A SN54ALS623A			SN74ALS620A SN74ALS623A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
							48†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48-mA limit applies for the SN74ALS620A-1 and SN74ALS623A-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS620A SN54ALS623A			SN74ALS620A SN74ALS623A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, (I_{OL} = 48 mA for −1 versions)	I_{OL} = 24 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports§					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	A or B ports§					−0.1			−0.1	
I_O¶		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS620A	V_{CC} = 5.5 V	Outputs high		24	39		24	34	mA
			Outputs low		31	49		31	44	
			Outputs disabled		33	52		33	47	
	'ALS623A	V_{CC} = 5.5 V	Outputs high		32	48		32	43	
			Outputs low		39	55		39	50	
			Outputs disabled		42	60		42	55	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C
§For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
¶The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS620A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS620A		SN74ALS620A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2	12	2	10	ns
t_{PHL}			2	12	2	10	
t_{PLH}	B	A	2	12	2	10	ns
t_{PHL}			2	12	2	10	
t_{PZH}	$\overline{G}$BA	A	3	23	3	17	ns
t_{PZL}			5	31	5	25	
t_{PHZ}	$\overline{G}$BA	A	2	14	2	12	ns
t_{PLZ}			3	22	3	18	
t_{PZH}	GAB	B	3	23	3	18	ns
t_{PZL}			5	31	5	25	
t_{PHZ}	GAB	B	2	14	2	12	ns
t_{PLZ}			3	22	3	18	

'ALS623A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS623A		SN74ALS623A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2	15	2	13	ns
t_{PHL}			3	13	3	11	
t_{PLH}	B	A	2	15	2	13	ns
t_{PHL}			3	13	3	11	
t_{PZH}	$\overline{G}$BA	A	5	25	5	22	ns
t_{PZL}			5	25	5	22	
t_{PHZ}	$\overline{G}$BA	A	2	19	2	16	ns
t_{PLZ}			2	23	2	19	
t_{PZH}	GAB	B	5	25	5	22	ns
t_{PZL}			5	25	5	22	
t_{PHZ}	GAB	B	2	19	2	16	ns
t_{PLZ}			2	23	2	19	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs and I/O ports . . . . . 7 V
Operating free-air temperature range: SN54ALS621A, SN54ALS622A . . . . . −55°C to 125°C
SN74ALS621A, SN74ALS622A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS621A SN54ALS622A			SN74ALS621A SN74ALS622A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			12			24	mA
							48†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48-mA limit applies for the SN74ALS621A-1 and SN74ALS622A-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS621A SN54ALS622A			SN74ALS621A SN74ALS622A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V, I_I = −18 mA				−1.5			−1.5	V
I_{OH}		V_{CC} = 4.5 V, V_{OH} = 5.5 V				0.1			0.1	mA
V_{OL}		V_{CC} = 4.5 V, I_{OL} = 12 mA			0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, I_{OL} = 24 mA (I_{OL} = 48 mA for -1 versions)						0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V, V_I = 7 V				0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V, V_I = 5.5 V				0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V, V_I = 2.7 V				20			20	µA
	A or B ports§					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V, V_I = 0.4 V				−0.1			−0.1	mA
	A or B ports§					−0.1			−0.1	
I_{CC}	'ALS621A	V_{CC} = 5.5 V	Outputs high		29	45		29	40	mA
			Outputs low		35	53		35	48	
	'ALS622A	V_{CC} = 5.5 V	Outputs high		11	20		11	15	
			Outputs low		20	33		20	28	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

'ALS621A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX				UNIT
			SN54ALS621A		SN74ALS621A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	10	45	10	33	ns
t_{PHL}			5	24	5	20	
t_{PLH}	B	A	10	45	10	33	ns
t_{PHL}			5	24	5	20	
t_{PLH}	$\overline{G}$BA	A	10	47	10	39	ns
t_{PHL}			12	40	12	35	
t_{PLH}	GAB	B	10	47	10	39	ns
t_{PHL}			12	40	12	35	

'ALS622A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX				UNIT
			SN54ALS622A		SN74ALS622A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	8	42	8	35	ns
t_{PHL}			5	23	5	19	
t_{PLH}	B	A	8	42	8	35	ns
t_{PHL}			5	23	5	19	
t_{PLH}	$\overline{G}$BA	A	8	45	8	38	ns
t_{PHL}			10	40	10	35	
t_{PLH}	GAB	B	8	45	8	38	ns
t_{PHL}			10	40	10	35	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54AS620, SN54AS623 . . . . . −55°C to 125°C
SN74AS620, SN74AS623 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS620 SN54AS623			SN74AS620 SN74AS623			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS620 SN54AS623			SN74AS620 SN74AS623			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.30	0.55				V
		V_{CC} = 4.5 V,	I_{OL} = 64 mA					0.35	0.55	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports‡					70			70	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	A or B ports‡					−0.75			−0.75	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−50		−150	−50		−150	mA
I_{CC}	'AS620	V_{CC} = 5.5 V	Outputs high		35	57		35	57	mA
			Outputs low		74	122		74	122	
			Outputs disabled		48	77		48	77	
	'AS623	V_{CC} = 5.5 V	Outputs high		57	93		57	93	
			Outputs low		116	189		116	189	
			Outputs disabled		71	116		71	116	

†All typical values are at V_{CC2} = 5 V, T_A = 25°C.
‡For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'AS620 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS620		SN74AS620		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	1	8	1	7	ns
t_{PHL}			2	7	2	6	
t_{PLH}	B	A	1	8	1	7	ns
t_{PHL}			2	7	2	6	
t_{PZH}	$\overline{G}$BA	A	2	8.5	2	8	ns
t_{PZL}			2	10	2	9	
t_{PHZ}	$\overline{G}$BA	A	1	7.5	1	6	ns
t_{PLZ}			2	15	2	12	
t_{PZH}	GAB	B	2	9	2	8	ns
t_{PZL}			2	10.5	2	9	
t_{PHZ}	GAB	B	1	6.5	1	6	ns
t_{PLZ}			2	16	2	13	

'AS623 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS623		SN74AS623		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	1	10	1	9	ns
t_{PHL}			1	9	1	8	
t_{PLH}	B	A	1	10	1	9	ns
t_{PHL}			1	9.5	1	8.5	
t_{PZH}	$\overline{G}$BA	A	2	11.5	2	11	ns
t_{PZL}			2	11	2	10	
t_{PHZ}	$\overline{G}$BA	A	1	8.5	1	7.5	ns
t_{PLZ}			1	13.5	1	11.5	
t_{PZH}	GAB	B	2	13	2	11.5	ns
t_{PZL}			2	12	2	11	
t_{PHZ}	GAB	B	1	8	1	7	ns
t_{PLZ}			1	10.5	1	9	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs and I/O ports . . . . . 7 V
Operating free-air temperature range: SN54AS621, SN54AS622 . . . . . −55°C to 125°C
SN74AS621, SN74AS622 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS621 SN54AS622			SN74AS621 SN74AS622			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS621 SN54AS622			SN74AS621 SN74AS622			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
I_{OH}		V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.30	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 64 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports‡					70			70	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	A or B ports‡					−0.75			−0.75	
I_{CC}	'AS621	V_{CC} = 5.5 V	Outputs high		48	79		48	79	mA
			Outputs low		116	189		116	189	
	'AS622	V_{CC} = 5.5 V	Outputs high		24	39		24	39	
			Outputs low		63	103		63	103	

†All typical values are at V_{CC} = 5 V, T_A = 25°C
‡For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

'AS621 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS621		SN74AS621		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	5	28.5	5	24	ns
t_{PHL}			1	8.5	1	7.5	
t_{PLH}	B	A	5	23	5	21	ns
t_{PHL}			1	8.5	1	7.5	
t_{PLH}	$\overline{G}BA$	A	5	24	5	21	ns
t_{PHL}			1	10	1	9	
t_{PLH}	GAB	B	5	26	5	22	ns
t_{PHL}			1	11	1	10	

'AS622 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS622		SN74AS622		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	5	28.5	5	24.5	ns
t_{PHL}			1	8.5	1	8	
t_{PLH}	B	A	5	30	5	25	ns
t_{PHL}			1	8.5	1	8	
t_{PLH}	$\overline{G}BA$	A	5	26	5	22	ns
t_{PHL}			1	11.5	1	10	
t_{PLH}	GAB	B	5	26	5	23	ns
t_{PHL}			1	11.5	1	10.5	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

32-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

D2661, DECEMBER 1982 – REVISED MAY 1986

- **Detects and Corrects Single-Bit Errors**
- **Detects and Flags Dual-Bit Errors**
- **Built-In Diagnostic Capability**
- **Fast Write and Read Cycle Processing Times**
- **Byte-Write Capability . . . 'ALS632A and 'ALS633**
- **Dependable Texas Instruments Quality and Reliability**

DEVICE	PACKAGE	BYTE-WRITE	OUTPUT
'ALS632A	52-pin	yes	3-State
'ALS633	52-pin	yes	Open-Collector
'ALS634	48-pin	no	3-State
'ALS635	48-pin	no	Open-Collector

description

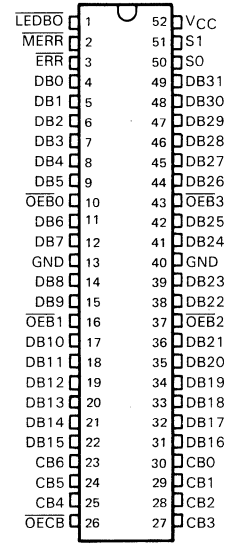
The 'ALS632A and 'ALS633 through 'ALS635 devices are 32-bit parallel error detection and correction circuits (EDACs) in 52-pin ('ALS632A and 'ALS633) or 48-pin ('ALS634 and 'ALS635) 600-mil packages. The EDACs use a modified Hamming code to generate a 7-bit check word from a 32-bit data word. This check word is stored along with the data word during the memory write cycle. During the memory read cycle, the 39-bit words from memory are processed by the EDACs to determine if errors have occurred in memory.

Single-bit errors in the 32-bit data word are flagged and corrected.

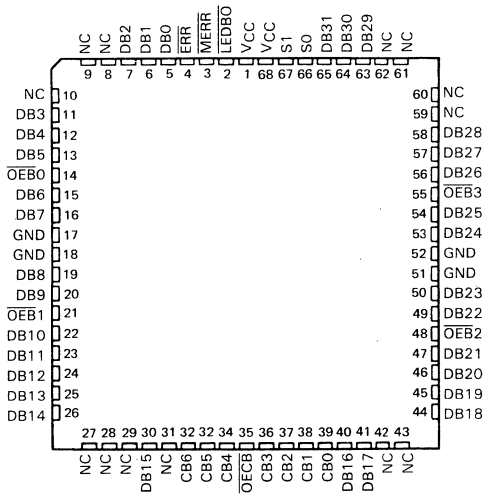
Single-bit errors in the 7-bit check word are flagged, and the CPU sends the EDAC through the correction cycle even though the 32-bit data word is not in error. The correction cycle will simply pass along the original 32-bit data word in this case and produce error syndrome bits to pinpoint the error-generating location.

Dual-bit errors are flagged but not corrected. These errors may occur in any two bits of the 39-bit data word from memory (two errors in the 32-bit data word, two errors in the 7-bit check word, or one error in each word). The gross-error condition of all lows or all highs from memory will be detected. Otherwise, errors in three or more bits of the 39-bit word are beyond the capabilities of these devices to detect.

'ALS632A, 'ALS633 . . . JD PACKAGE
(TOP VIEW)



'ALS632A, 'ALS633 . . . FN PACKAGE
(TOP VIEW)

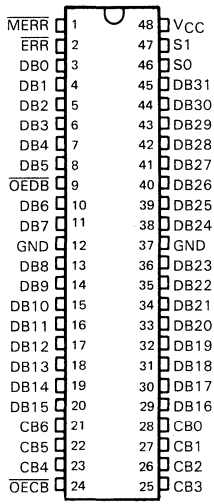


NC – No internal connection

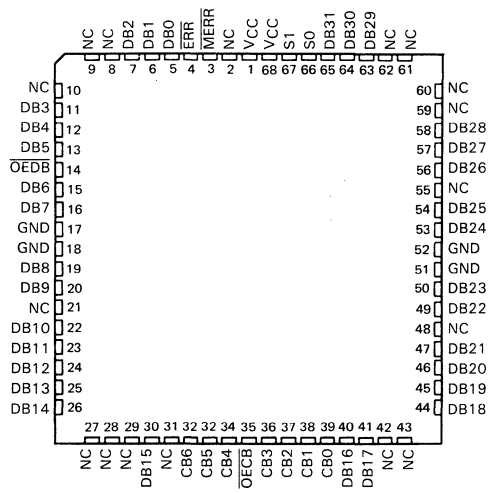
Read-modify-write (byte-control) operations can be performed with the 'ALS632A and 'ALS633 EDACs by using output latch enable, $\overline{\text{LEDBO}}$, and the individual $\overline{\text{OEB0}}$ thru $\overline{\text{OEB3}}$ byte control pins.

Diagnostics are performed on the EDACs by controls and internal paths that allow the user to read the contents of the DB and CB input latches. These will determine if the failure occurred in memory or in the EDAC.

'ALS634, 'ALS635 . . . JD PACKAGE
(TOP VIEW)



'ALS634, 'ALS635 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

TABLE 1. WRITE CONTROL FUNCTION

MEMORY CYCLE	EDAC FUNCTION	CONTROL S1	CONTROL S0	DATA I/O	DB CONTROL $\overline{\text{OEBn}}$ OR $\overline{\text{OEDB}}$	DB OUTPUT LATCH ('ALS632A, 'ALS633) $\overline{\text{LEDBO}}$	CHECK I/O	CB CONTROL $\overline{\text{OECB}}$	ERROR FLAGS $\overline{\text{ERR}}$	ERROR FLAGS $\overline{\text{MERR}}$
Write	Generate check word	L	L	Input	H	X	Output check bits†	L	H	H

†See Table 2 for details on check bit generation.

memory write cycle details

During a memory write cycle, the check bits (CB0 thru CB6) are generated internally in the EDAC by seven 16-input parity generators using the 32-bit data word as defined in Table 2. These seven check bits are stored in memory along with the original 32-bit data word. This 32-bit word will later be used in the memory read cycle for error detection and correction.

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TABLE 2. PARITY ALGORITHM

CHECK WORD	32-BIT DATA WORD																												
BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CB0	X		X	X		X					X		X	X	X			X			X		X	X	X	X		X				X
CB1				X		X		X		X		X		X	X	X				X		X		X		X		X		X	X	X
CB2	X		X			X	X		X			X	X			X	X		X			X	X		X			X	X			X
CB3			X	X	X				X	X	X				X	X			X	X	X				X	X	X				X	X
CB4	X	X							X	X	X	X	X	X			X	X							X	X	X	X	X	X		
CB5	X	X	X	X	X	X	X	X									X	X	X	X	X	X	X	X								
CB6	X	X	X	X	X	X	X	X																	X	X	X	X	X	X	X	X

The seven check bits are parity bits derived from the matrix of data bits as indicated by "X" for each bit.

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ALS and AS Circuits

error detection and correction details

During a memory read cycle, the 7-bit check word is retrieved along with the actual data. In order to be able to determine whether the data from memory is acceptable to use as presented to the bus, the error flags must be tested to determine if they are at the high level.

The first case in Table 3 represents the normal, no-error conditions. The EDAC presents highs on both flags. The next two cases of single-bit errors give a high on $\overline{\text{MERR}}$ and a low on $\overline{\text{ERR}}$, which is the signal for a correctable error, and the EDAC should be sent through the correction cycle. The last three cases of double-bit errors will cause the EDAC to signal lows on both $\overline{\text{ERR}}$ and $\overline{\text{MERR}}$, which is the interrupt indication for the CPU.

TABLE 3. ERROR FUNCTION

TOTAL NUMBER OF ERRORS		ERROR FLAGS		DATA CORRECTION
32-BIT DATA WORD	7-BIT CHECK WORD	$\overline{\text{ERR}}$	$\overline{\text{MERR}}$	
0	0	H	H	Not applicable
1	0	L	H	Correction
0	1	L	H	Correction
1	1	L	L	Interrupt
2	0	L	L	Interrupt
0	2	L	L	Interrupt

Error detection is accomplished as the 7-bit check word and the 32-bit data word from memory are applied to internal parity generators/checkers. If the parity of all seven groupings of data and check bits are correct, it is assumed that no error has occurred and both error flags will be high.

If the parity of one or more of the check groups is incorrect, an error has occurred and the proper error flag or flags will be set low. Any single error in the 32-bit data word will change the state of either three or five bits of the 7-bit check word. Any single error in the 7-bit check word changes the state of only that one bit. In either case, the single error flag ($\overline{\text{ERR}}$) will be set low while the dual error flag ($\overline{\text{MERR}}$) will remain high.

Any two-bit error will change the state of an even number of check bits. The two-bit error is not correctable since the parity tree can only identify single-bit errors. Both error flags are set low when any two-bit error is detected.

Three or more simultaneous bit errors can cause the EDAC to believe that no error, a correctable error, or an uncorrectable error has occurred and will produce erroneous results in all three cases. It should be noted that the gross-error conditions of all lows and all highs will be detected.

TABLE 4. READ, FLAG, AND CORRECT FUNCTION

MEMORY CYCLE	EDAC FUNCTION	CONTROL S1	CONTROL S0	DATA I/O	DB CONTROL $\overline{OEBn}$ OR $\overline{OEDB}$	DB OUTPUT LATCH ('ALS632A, 'ALS633) $\overline{LEDBO}$	CHECK I/O	CB CONTROL $\overline{OECB}$	ERROR FLAGS $\overline{ERR}$ $\overline{MERR}$
Read	Read & flag	H	L	Input	H	X	Input	H	Enabled†
Read	Latch input data & check bits	H	H	Latched input data	H	L	Latched input check word	H	Enabled†
Read	Output corrected data & syndrome bits	H	H	Output corrected data word	L	X	Output syndrome bits‡	L	Enabled†

†See Table 3 for error description.
‡See Table 5 for error location.

As the corrected word is made available on the data I/O port (DB0 thru DB31), the check word I/O port (CB0 thru CB6) presents a 7-bit syndrome error code. This syndrome error code can be used to locate the bad memory chip. See Table 5 for syndrome decoding.

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TABLE 5. SYNDROME DECODING

SYNDROME BITS							ERROR
6	5	4	3	2	1	0	
L	L	L	L	L	L	L	unc
L	L	L	L	L	L	H	2-bit
L	L	L	L	L	H	L	2-bit
L	L	L	L	L	H	H	unc
L	L	L	L	H	L	L	2-bit
L	L	L	L	H	L	H	unc
L	L	L	L	H	H	L	unc
L	L	L	L	H	H	H	2-bit
L	L	L	H	L	L	L	2-bit
L	L	L	H	L	L	H	unc
L	L	L	H	L	H	L	DB31
L	L	L	H	L	H	H	2-bit
L	L	L	H	H	L	L	unc
L	L	L	H	H	L	H	2-bit
L	L	L	H	H	H	L	DB30
L	L	H	L	L	L	L	2-bit
L	L	H	L	L	L	H	unc
L	L	H	L	L	H	L	DB29
L	L	H	L	L	H	H	2-bit
L	L	H	L	H	L	L	DB28
L	L	H	L	H	L	H	2-bit
L	L	H	L	H	H	L	2-bit
L	L	H	L	H	H	H	DB27
L	L	H	H	L	L	L	DB26
L	L	H	H	L	L	H	2-bit
L	L	H	H	L	H	L	2-bit
L	L	H	H	L	H	H	DB25
L	L	H	H	H	L	L	2-bit
L	L	H	H	H	L	H	DB24
L	L	H	H	H	H	L	unc
L	L	H	H	H	H	H	2-bit

SYNDROME BITS							ERROR
6	5	4	3	2	1	0	
L	H	L	L	L	L	L	2-bit
L	H	L	L	L	L	H	unc
L	H	L	L	L	H	L	DB7
L	H	L	L	L	H	H	2-bit
L	H	L	L	H	L	L	DB6
L	H	L	L	H	L	H	2-bit
L	H	L	L	H	H	L	2-bit
L	H	L	L	H	H	H	DB5
L	H	L	H	L	L	L	DB4
L	H	L	H	L	L	H	2-bit
L	H	L	H	L	H	L	2-bit
L	H	L	H	L	H	H	DB3
L	H	L	H	H	L	L	2-bit
L	H	L	H	H	L	H	DB2
L	H	L	H	H	H	L	unc
L	H	L	H	H	H	H	2-bit
L	H	H	L	L	L	L	DB0
L	H	H	L	L	L	H	2-bit
L	H	H	L	L	H	L	2-bit
L	H	H	L	L	H	H	unc
L	H	H	L	H	L	L	2-bit
L	H	H	L	H	L	H	DB1
L	H	H	L	H	H	L	unc
L	H	H	L	H	H	H	2-bit
L	H	H	H	L	L	L	2-bit
L	H	H	H	L	L	H	unc
L	H	H	H	L	H	L	unc
L	H	H	H	L	H	H	2-bit
L	H	H	H	H	L	L	unc
L	H	H	H	H	L	H	2-bit
L	H	H	H	H	H	L	2-bit
L	H	H	H	H	H	H	CB6

SYNDROME BITS							ERROR
6	5	4	3	2	1	0	
H	L	L	L	L	L	L	2-bit
H	L	L	L	L	L	H	unc
H	L	L	L	L	H	L	unc
H	L	L	L	L	H	H	2-bit
H	L	L	L	H	L	L	unc
H	L	L	L	H	L	H	2-bit
H	L	L	L	H	H	L	2-bit
H	L	L	L	H	H	H	unc
H	L	L	H	L	L	L	unc
H	L	L	H	L	L	H	2-bit
H	L	L	H	L	H	L	2-bit
H	L	L	H	L	H	H	DB15
H	L	L	H	H	L	L	2-bit
H	L	L	H	H	L	H	unc
H	L	L	H	H	H	L	DB14
H	L	L	H	H	H	H	2-bit
H	L	H	L	L	L	L	unc
H	L	H	L	L	L	H	2-bit
H	L	H	L	L	H	L	2-bit
H	L	H	L	L	H	H	DB13
H	L	H	L	H	L	L	2-bit
H	L	H	L	H	L	H	DB12
H	L	H	L	H	H	L	DB11
H	L	H	L	H	H	H	2-bit
H	L	H	H	L	L	L	2-bit
H	L	H	H	L	L	H	DB10
H	L	H	H	L	H	L	DB9
H	L	H	H	L	H	H	2-bit
H	L	H	H	H	L	L	DB8
H	L	H	H	H	L	H	2-bit
H	L	H	H	H	H	L	2-bit
H	L	H	H	H	H	H	CB5

SYNDROME BITS							ERROR
6	5	4	3	2	1	0	
H	H	L	L	L	L	L	unc
H	H	L	L	L	L	H	2-bit
H	H	L	L	L	H	L	2-bit
H	H	L	L	L	H	H	DB23
H	H	L	L	H	L	L	2-bit
H	H	L	L	H	L	H	DB22
H	H	L	L	H	H	L	DB21
H	H	L	L	H	H	H	2-bit
H	H	L	H	L	L	L	2-bit
H	H	L	H	L	L	H	DB20
H	H	L	H	L	H	L	DB19
H	H	L	H	L	H	H	2-bit
H	H	L	H	H	L	L	DB18
H	H	L	H	H	L	H	2-bit
H	H	L	H	H	H	L	2-bit
H	H	L	H	H	H	H	CB4
H	H	H	L	L	L	L	2-bit
H	H	H	L	L	L	H	DB16
H	H	H	L	L	H	L	unc
H	H	H	L	L	H	H	2-bit
H	H	H	L	H	L	L	DB17
H	H	H	L	H	L	H	2-bit
H	H	H	L	H	H	L	2-bit
H	H	H	L	H	H	H	CB3
H	H	H	H	L	L	L	unc
H	H	H	H	L	L	H	2-bit
H	H	H	H	L	H	L	2-bit
H	H	H	H	L	H	H	CB2
H	H	H	H	H	L	L	2-bit
H	H	H	H	H	L	H	CB1
H	H	H	H	H	H	L	CB0
H	H	H	H	H	H	H	none

CB X= error in check bit X
DB Y= error in data bit Y
2-bit = double-bit error
unc = uncorrectable multibit error

read-modify-write (byte control) operations

The 'ALS632A and 'ALS633 devices are capable of byte-write operations. The 39-bit word from memory must first be latched into the DB and CB input latches. This is easily accomplished by switching from the read and flag mode (S1 = H, S0 = L) to the latch input mode (S1 = H, S0 = H). The EDAC will then make any corrections, if necessary, to the data word and place it at the input of the output data latch. This data word must then be latched into the output data latch by taking $\overline{\text{LEDBO}}$ from a low to a high.

Byte control can now be employed on the data word through the $\overline{\text{OEB0}}$ through $\overline{\text{OEB3}}$ controls. $\overline{\text{OEB0}}$ controls DB0-DB7 (byte 0), $\overline{\text{OEB1}}$ controls DB8-DB15 (byte 1), $\overline{\text{OEB2}}$ controls DB16-DB23 (byte 2), and $\overline{\text{OEB3}}$ controls DB24-DB31 (byte 3). Placing a high on the byte control will disable the output and the user can modify the byte. If a low is placed on the byte control, then the original byte is allowed to pass onto the data bus unchanged. If the original data word is altered through byte control, a new check word must be generated before it is written back into memory. This is easily accomplished by taking control S1 and S0 low. Table 6 lists the read-modify-write functions.

TABLE 6. READ-MODIFY-WRITE FUNCTION

MEMORY CYCLE	EDAC FUNCTION	CONTROL S1	CONTROL S0	BYTEn†	$\overline{OEB}$n†	DB OUTPUT LATCH $\overline{LEDBO}$	CHECK I/O	CB CONTROL	ERROR FLAG $\overline{ERR}$ $\overline{MERR}$
Read	Read & Flag	H	L	Input	H	X	Input	H	Enabled
Read	Latch input data & check bits	H	H	Latched Input data	H	L	Latched input check word	H	Enabled
Read	Latch corrected data word into output latch	H	H	Latched output data word	H	H	Hi-Z	H	Enabled
							Output Syndrome bits	L	
Modify /write	Modify appropriate byte or bytes & generate new check word	L	L	Input modified BYTE0	H	H	Output check word	L	H H
				Output unchanged BYTE0	L				

†$\overline{OEB}$0 controls DB0-DB7 (BYTE0), $\overline{OEB}$1 controls DB8-DB15 (BYTE1), $\overline{OEB}$3 controls DB16-DB23 (BYTE2), $\overline{OEB}$3 controls DB24-DB31 (BYTE3).

diagnostic operations

The 'ALS632A and 'ALS633 thru 'ALS635 are capable of diagnostics that allow the user to determine whether the EDAC or the memory is failing. The diagnostic function tables will help the user to see the possibilities for diagnostic control.

In the diagnostic mode (S1 = L, S0 = H), the checkword is latched into the input latch while the data input latch remains transparent. This lets the user apply various data words against a fixed known checkword. If the user applies a diagnostic data word with an error in any bit location, the $\overline{ERR}$ flag should be low. If a diagnostic data word with two errors in any bit location is applied, the $\overline{MERR}$ flag should be low. After the checkword is latched into the input latch, it can be verified by taking $\overline{OECB}$ low. This outputs the latched checkword. With the 'ALS632A and 'ALS633, the diagnostic data word can be latched into the output data latch and verified. It should be noted that the 'ALS634 and 'ALS635 do not have this pass-through capability because they do not contain an output data latch. By changing from the diagnostic mode (S1 = L, S0 = H) to the correction mode (S1 = H, S0 = H), the user can verify that the EDAC will correct the diagnostic data word. Also, the syndrome bits can be produced to verify that the EDAC pinpoints the error location. Table 7 ('ALS632A and 'ALS633) and Table 8 ('ALS634 and 'ALS635) list the diagnostic functions.

TABLE 7. 'ALS632A, 'ALS633 DIAGNOSTIC FUNCTION

EDAC FUNCTION	CONTROL S1	CONTROL S0	DATA I/O	DB BYTE CONTROL $\overline{OEBn}$	DB OUTPUT LATCH $\overline{LEDBO}$	CHECK I/O	CB CONTROL $\overline{OECB}$	ERROR FLAGS $\overline{ERR}$	ERROR FLAGS $\overline{MERR}$
Read & flag	H	L	Input correct data word	H	X	Input correct check bits	H	H	H
Latch input check word while data input latch remains transparent	L	H	Input diagnostic data word†	H	L	Latched input check bits	H	Enabled	
Latch diagnostic data word into output latch	L	H	Input diagnostic data word†	H	H	Output latched check bits	L	Enabled	
						Hi-Z	H		
Latch diagnostic data word into input latch	H	H	Latched input diagnostic data word	H	H	Output syndrome bits	L	Enabled	
						Hi-Z	H		
Output diagnostic data word & syndrome bits	H	H	Output diagnostic data word	L	H	Output syndrome bits	L	Enabled	
						Hi-Z	H		
Output corrected diagnostic data word & output syndrome bits	H	H	Output corrected diagnostic data word	L	L	Output syndrome bits	L	Enabled	
						Hi-Z	H		

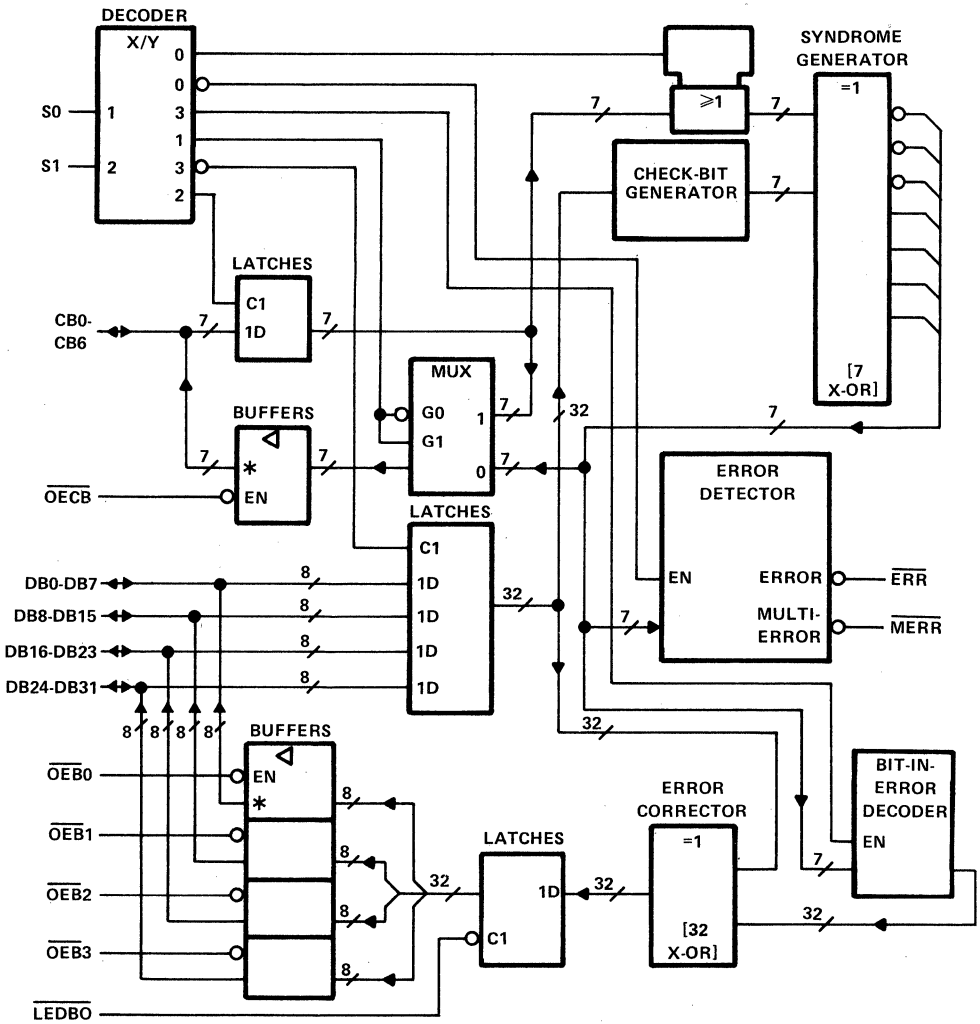
†Diagnostic data is a data word with an error in one bit location except when testing the $\overline{MERR}$ error flag. In this case, the diagnostic data word will contain errors in two bit locations.

TABLE 8. 'ALS634, 'ALS635 DIAGNOSTIC FUNCTION

EDAC FUNCTION	CONTROL S1	CONTROL S0	DATA I/O	DB CONTROL $\overline{OEDB}$	CHECK I/O	CB CONTROL $\overline{OECB}$	ERROR FLAGS $\overline{ERR}$	ERROR FLAGS $\overline{MERR}$
Read & flag	H	L	Input correct data word	H	Input correct check bits	H	H	H
Latch input check bits while data input latch remains transparent	L	H	Input diagnostic data word†	H	Latched input check bits	H	Enabled	
Output input check bits	L	H	Input diagnostic data word†	H	Output input check bits	L	Enabled	
Latch diagnostic data into input latch	H	H	Latched input diagnostic data word	H	Output syndrome bits	L	Enabled	
					Hi-Z	H		
Output corrected diagnostic data word	H	H	Output corrected diagnostic data word	L	Output syndrome bits	L	Enabled	
					Hi-Z	H		

†Diagnostic data is a data word with an error in one bit location except when testing the $\overline{MERR}$ error flag. In this case, the diagnostic data word will contain errors in two bit locations.

'ALS632A, 'ALS633 logic diagram (positive logic)



*'ALS632A has 3-state (▽) check-bit and data outputs.
'ALS633 has open-collector (⟐) check-bit and data outputs.

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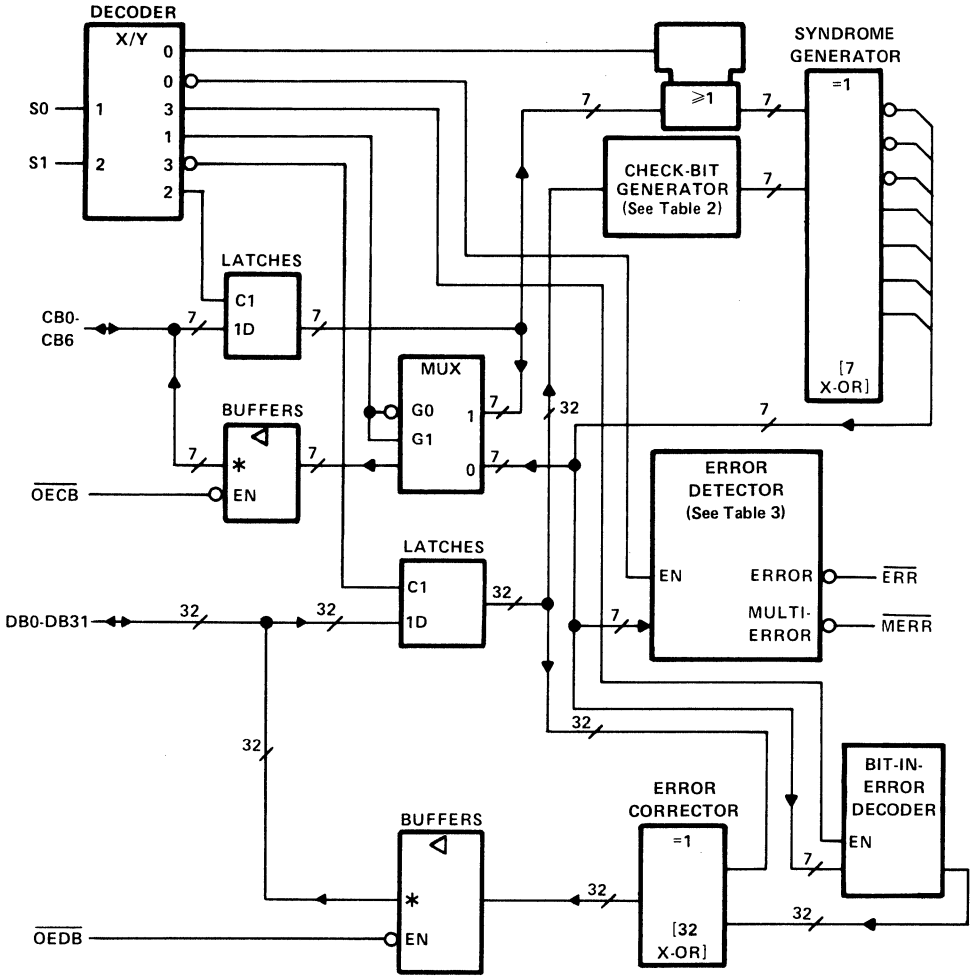
'ALS634, 'ALS635 logic diagram (positive logic)



*'ALS634 has 3-state (▽) check-bit and data outputs.
'ALS635 has open-collector (⏀) check-bit and data outputs.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: CB and DB . . . . . 5.5 V
All others . . . . . 7 V
Operating free-air temperature range:
SN74ALS632A, SN74ALS633 thru SN74ALS635 . . . . . 0°C to 70°C
Operating case temperature range:
SN54ALS632A, SN54ALS633 thru SN54ALS635 . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS632A SN54ALS633 THRU SN54ALS635			SN74ALS632A SN74ALS633 THRU SN74ALS635			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.6			0.8	V
I_{OH}	High-level output current	$\overline{ERR}$ or $\overline{MERR}$			−0.4			−0.4	mA
		DB or CB ‘ALS632A, ‘ALS634			−1			−2.6	
I_{OL}	Low-level output current	$\overline{ERR}$ or $\overline{MERR}$			4			8	mA
		DB or CB			12			24	
t_w	Pulse duration	$\overline{LEDBO}$ low	45			25			ns
t_{su}	Setup time	(1) Data and check word before S0↑ (S1 = H)	15			10			ns
		(2) S0 high before $\overline{LEDBO}$↑ (S1 = H)†	45			45			
		(3) $\overline{LEDBO}$ high before the earlier of S0↓ or S1↓†	0			0			
		(4) $\overline{LEDBO}$ high before S1↑ (S0 = H)	0			0			
		(5) Diagnostic data word before S1↑ (S0 = H)	28			10			
		(6) Diagnostic check word before the later of S1↓ or S0↑	15			10			
		(7) Diagnostic data word before $\overline{LEDBO}$↑ (S1 = L and S0 = H)‡	35			20			
t_h	Hold time	(8) Read-mode, S0 low and S1 high	35			30			ns
		(9) Data and check word after S0↑ (S1 = H)	20			15			
		(10) Data word after S1↑ (S0 = H)	20			15			
		(11) Check word after the later of S1↓ or S0↑	20			15			
		(12) Diagnostic data word after $\overline{LEDBO}$↑ (S1 = L, S0 = H)‡	0			0			
t_{corr}	Correction time (see Figure 1)			65			58		ns
T_C	Operating case temperature		−55		125				°C
T_A	Operating free-air temperature					0		70	°C

†These times ensure that corrected data is saved in the output data latch.
‡These times ensure that the diagnostic data word is saved in the output data latch.

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'ALS632A, 'ALS634 electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS632A SN54ALS634			SN74ALS632A SN74ALS634			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	All outputs	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} −2			V_{CC} −2			V
	DB or CB	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	$\overline{ERR}$ or $\overline{MERR}$	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
	DB or CB	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	S0 or S1	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	All others	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	S0 or S1	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	All others‡					20			20	
I_{IL}	S0 or S1	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.4			−0.4	mA
	All others‡					−0.1			−0.1	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		150	250		150	250	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with S0 and S1 at 4.5 V and all CB and DB pins grounded.

'ALS632A switching characteristics, V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, T_C = −55°C to 125°C for SN54ALS632A, T_A = 0°C to 70°C for SN74ALS632A

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ALS632A		SN74ALS632A		UNIT
				MIN	MAX	MIN	MAX	
t_{pd}	DB and CB	$\overline{ERR}$	S1 = H, S0 = L, R_L = 500 Ω	10	50	10	40	ns
	DB	$\overline{ERR}$	S1 = L, S0 = H, R_L = 500 Ω	10	43	10	40	
t_{pd}	DB and CB	$\overline{MERR}$	S1 = H, S0 = L, R_L = 500 Ω	15	67	15	55	ns
	DB	$\overline{MERR}$	S1 = L, S0 = H, R_L = 500 Ω	15	67	15	55	
t_{pd}	S0↓ and S1↓	CB	R1 = R2 = 500 Ω	10	60	10	48	ns
t_{PLH}	S0↓ and S1↓	$\overline{ERR}$	R_L = 500 Ω	5	30	5	25	ns
t_{pd}	DB	CB	S1 = L, S0 = L, R1 = R2 = 500 Ω	10	60	10	48	ns
t_{pd}	$\overline{LEDBO}$↓	DB	S1 = X, S0 = H, R1 = R2 = 500 Ω	7	35	7	30	ns
t_{pd}	S1↑	CB	S0 = H, R1 = R2 = 500 Ω	10	60	10	50	ns
t_{en}	$\overline{OECB}$↓	CB	S0 = H, S1 = X, R1 = R2 = 500 Ω	2	40	2	25	ns
t_{dis}	$\overline{OECB}$↑	CB	S0 = H, S1 = X, R1 = R2 = 500 Ω	2	40	2	25	ns
t_{en}	$\overline{OEB0}$ thru $\overline{OEB3}$↓	DB	S0 = H, S1 = X, R1 = R2 = 500 Ω	2	40	2	25	ns
t_{dis}	$\overline{OEB0}$ thru $\overline{OEB3}$↑	DB	S0 = H, S1 = X, R1 = R2 = 500 Ω	2	40	2	25	ns

'ALS634 switching characteristics, V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, T_C = −55°C to 125°C for SN54ALS634, T_A = 0°C to 70°C for SN74ALS634

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ALS634		SN74ALS634		UNIT
				MIN	MAX	MIN	MAX	
t_{pd}	DB and CB	$\overline{ERR}$	S1 = H, S0 = L, R_L = 500 Ω	10	43	10	40	ns
			S1 = L, S0 = H, R_L = 500 Ω	10	43	10	40	
t_{pd}	DB and CB	$\overline{MERR}$	S1 = H, S0 = L, R_L = 500 Ω	15	67	15	55	ns
			S1 = L, S0 = H, R_L = 500 Ω	15	67	15	55	
t_{pd}	S0↓ and S1↓	CB	R1 = R2 = 500 Ω	10	60	10	48	ns
t_{PLH}	S0↓ and S1↓	$\overline{ERR}$	R_L = 500 Ω	5	30	5	25	ns
t_{pd}	DB	CB	S1 = L, S0 = L, R1 = R2 = 500 Ω	10	60	10	48	ns
t_{pd}	S1↑	CB	S0 = H, R1 = R2 = 500 Ω	7	35	7	30	ns
t_{en}	$\overline{OECB}$↓	CB	S1 = X, S0 = H, R1 = R2 = 500 Ω	2	30	2	25	ns
t_{dis}	$\overline{OECB}$↑	CB	S1 = X, S0 = H, R1 = R2 = 500 Ω	2	30	2	25	ns
t_{en}	$\overline{OEDB}$↓	DB	S1 = X, S0 = H, R1 = R2 = 500 Ω	2	30	2	30	ns
t_{dis}	$\overline{OEDB}$↑	DB	S1 = X, S0 = H, R1 = R2 = 500 Ω	2	30	2	25	ns

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'ALS633 electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS633			SN74ALS633			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	$\overline{ERR}$ or $\overline{MERR}$	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
I_{OH}	DB or CB	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	$\overline{ERR}$ or $\overline{MERR}$	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
	DB or CB	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	S0 or S1	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	All others	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	S0 or S1	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	All others‡					20			20	
I_{IL}	S0 or S1	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.4			−0.4	mA
	All others‡					−0.1			−0.1	
I_O§	$\overline{ERR}$ or $\overline{MERR}$	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		150	250		150	250	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with S0 and S1 at 4.5 V and all CB and DB pins grounded.

'ALS633 switching characteristics, V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, T_C = −55°C to 125°C for SN54ALS633, T_A = 0°C to 70°C for SN74ALS633

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ALS633		SN74ALS633		UNIT
				MIN	MAX	MIN	MAX	
t_{pd}	DB and CB	$\overline{ERR}$	S1 = H, S0 = L, R_L = 500 Ω	10	43	10	40	ns
	DB	$\overline{ERR}$	S1 = L, S0 = H, R_L = 500 Ω	10	43	10	40	
t_{pd}	DB and CB	$\overline{MERR}$	S1 = H, S0 = L, R_L = 500 Ω	15	67	15	55	ns
			S1 = L, S0 = H, R_L = 500 Ω	15	67	15	55	
t_{pd}	S0↓ and S1↓	CB	R_L = 680 Ω	10	75	10	60	ns
t_{PLH}	S0↓ and S1↓	$\overline{ERR}$	R_L = 500 Ω	5	30	5	25	ns
t_{pd}	DB	CB	S1 = L, S0 = L, R_L = 680 Ω	10	70	10	60	ns
t_{pd}	$\overline{LEDBO}$↓	DB	S1 = X, S0 = H, R_L = 680 Ω	15	70	15	50	ns
t_{pd}	S1↑	CB	S0 = H, R_L = 680 Ω	10	60	10	45	ns
t_{PLH}	$\overline{OECB}$↑	CB	S1 = X, S0 = H, R_L = 680 Ω	2	35	2	30	ns
t_{PHL}	$\overline{OECB}$↓	CB	S1 = X, S0 = H, R_L = 680 Ω	2	35	2	30	ns
t_{PLH}	$\overline{OEB0}$ thru $\overline{OEB3}$↑	DB	S1 = X, S0 = H, R_L = 680 Ω	2	35	2	30	ns
t_{PHL}	$\overline{OEB0}$ thru $\overline{OEB3}$↓	DB	S1 = X, S0 = H, R_L = 680 Ω	2	35	2	30	ns

'ALS635 electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS635			SN74ALS635			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	$\overline{ERR}$ or $\overline{MERR}$	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
I_{OH}	DB or CB	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	$\overline{ERR}$ or $\overline{MERR}$	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
	DB or CB	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	S0 or S1	V_{CC} = 5.5 V,	V_I = 7 V							mA
	All others	V_{CC} = 5.5 V,	V_I = 5.5 V							
I_{IH}	S0 or S1	V_{CC} = 5.5 V,	V_I = 2.7 V							μA
	All others‡									
I_{IL}	S0 or S1	V_{CC} = 5.5 V,	V_I = 0.4 V							mA
	All others‡									
I_O§	$\overline{ERR}$ or $\overline{MERR}$	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		150			150		mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with S0 and S1 at 4.5 V and all CB and DB pins grounded.

'ALS635 switching characteristics, V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, T_C = −55°C to 125°C for SN54ALS635, T_A = 0°C to 70°C for SN74ALS635

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ALS635			SN74ALS635			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{pd}	DB and CB	$\overline{ERR}$	S1 = H, S0 = L, R_L = 500 Ω		26			26		ns
	DB	$\overline{ERR}$	S1 = L, S0 = H, R_L = 500 Ω		26			26		
t_{pd}	DB and CB	$\overline{MERR}$	S1 = H, S0 = L, R_L = 500 Ω		40			40		ns
			S1 = L, S0 = H, R_L = 500 Ω		40			40		
t_{pd}	S0↓ and S1↓	CB	R_L = 680 Ω		40			40		ns
t_{PLH}	S0↓ and S1↓	$\overline{ERR}$	R_L = 500 Ω		14			14		ns
t_{pd}	DB	CB	S1 = L, S0 = L, R_L = 680 Ω		40			40		ns
t_{pd}	S1↑	DB	S0 = H, R_L = 680 Ω		40			40		ns
t_{PLH}	$\overline{OECB}$↑	CB	S1 = X, S0 = H, R_L = 680 Ω		24			24		ns
t_{PHL}	$\overline{OECB}$↓	CB	S1 = X, S0 = H, R_L = 680 Ω		24			24		ns
t_{PLH}	$\overline{OEDB}$↑	DB	S1 = X, S0 = H, R_L = 680 Ω		24			24		ns
t_{PHL}	$\overline{OEDB}$↓	DB	S1 = X, S0 = H, R_L = 680 Ω		24			24		ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

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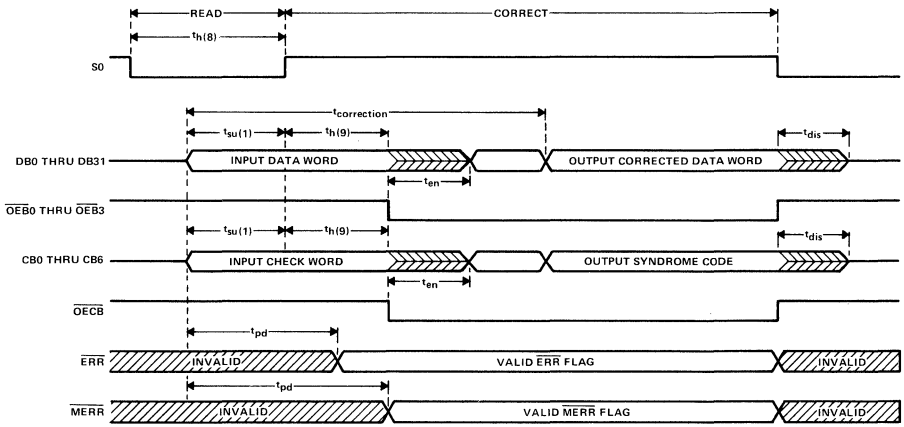

FIGURE 1. READ, FLAG, AND CORRECT MODE SWITCHING WAVEFORMS

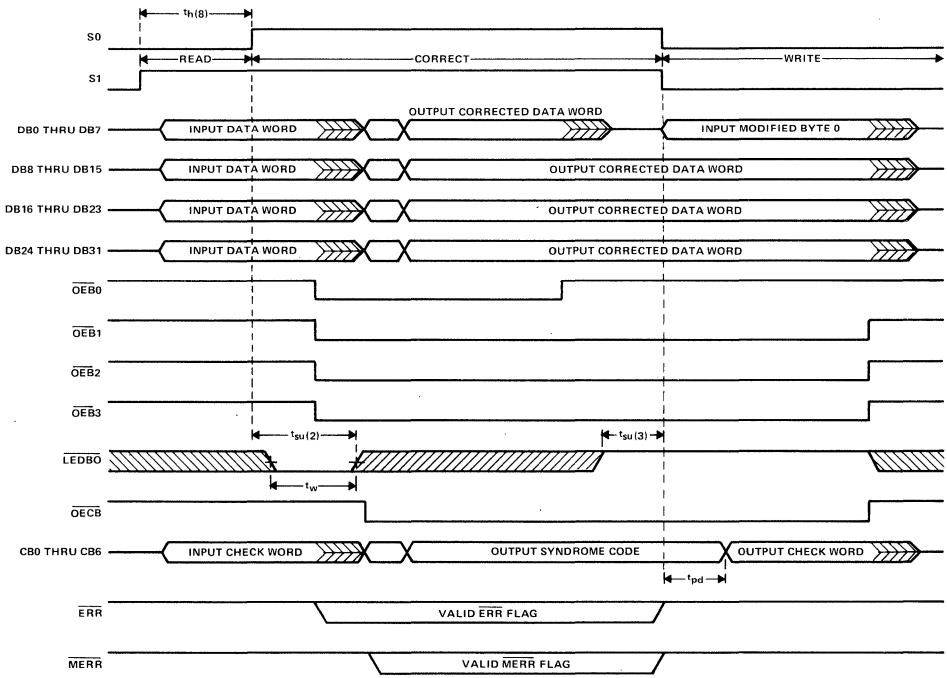

FIGURE 2. READ, CORRECT, MODIFY MODE SWITCHING WAVEFORMS

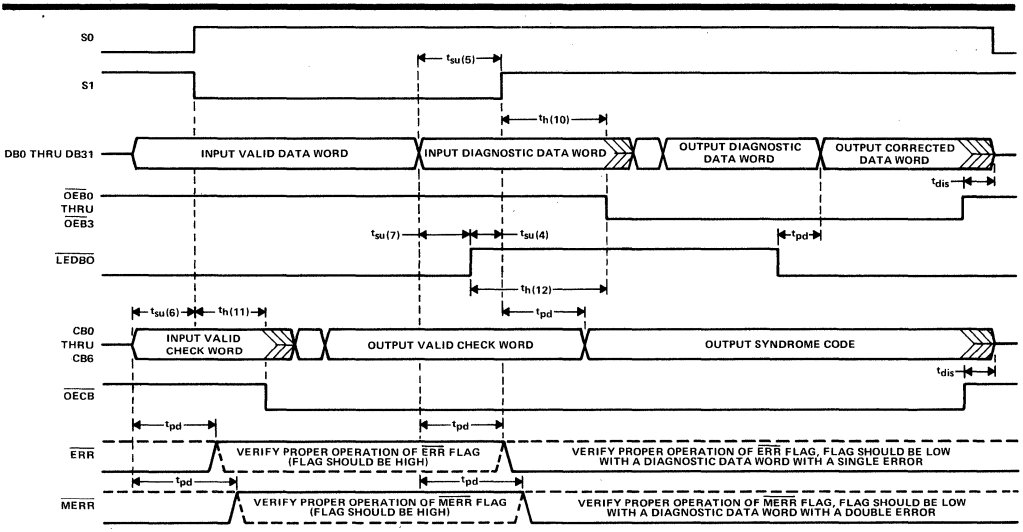

FIGURE 3. DIAGNOSTIC MODE SWITCHING WAVEFORM

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SN54AS632, SN54AS634
SN74AS632, SN74AS634
32-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

D2661, JANUARY 1986

- **Detects and Corrects Single-Bit Errors**
- **Detects and Flags Dual-Bit Errors**
- **Built-In Diagnostic Capability**
- **Fast Write and Read Cycle Processing Times**
- **Byte-Write Capability . . . 'AS632**
- **Dependable Texas Instruments Quality and Reliability**

DEVICE	PACKAGE	BYTE-WRITE	OUTPUT
'AS632	52-pin	yes	3-State
'AS634	48-pin	no	3-State

description

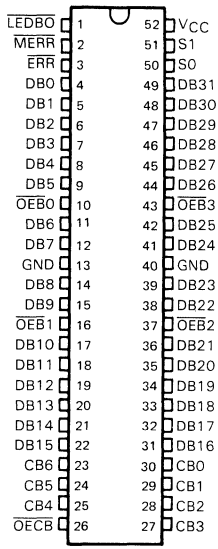
The 'AS632 and 'AS634 devices are 32-bit parallel error detection and correction circuits (EDACs) in 52-pin ('AS632) or 48-pin ('AS634) 600-mil packages. The EDACs use a modified Hamming code to generate a 7-bit check word from a 32-bit data word. This check word is stored along with the data word during the memory write cycle. During the memory read cycle, the 39-bit words from memory are processed by the EDACs to determine if errors have occurred in memory.

Single-bit errors in the 32-bit data word are flagged and corrected.

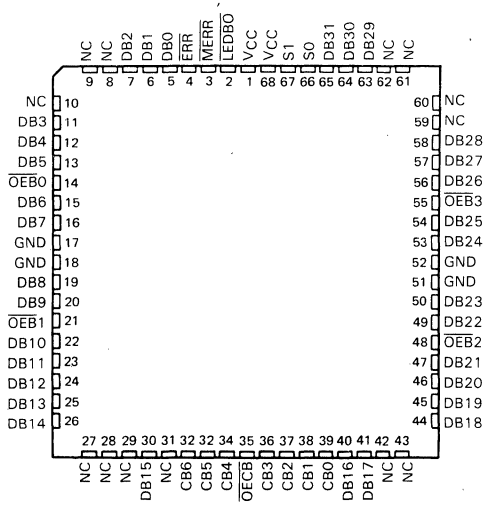
Single-bit errors in the 7-bit check word are flagged, and the CPU sends the EDAC through the correction cycle even though the 32-bit data word is not in error. The correction cycle will simply pass along the original 32-bit data word in this case and produce error syndrome bits to pinpoint the error-generating location.

Dual-bit errors are flagged but not corrected. These errors may occur in any two bits of the 39-bit data word from memory (two errors in the 32-bit data word, two errors in the 7-bit check word, or one error in each word). The gross-error condition of all lows or all highs from memory will be detected. Otherwise, errors in three or more bits of the 39-bit word are beyond the capabilities of these devices to detect.

'AS632 . . . JD PACKAGE
(TOP VIEW)



'AS632 . . . FN PACKAGE
(TOP VIEW)

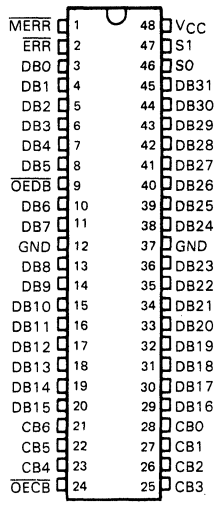


NC—No internal connection

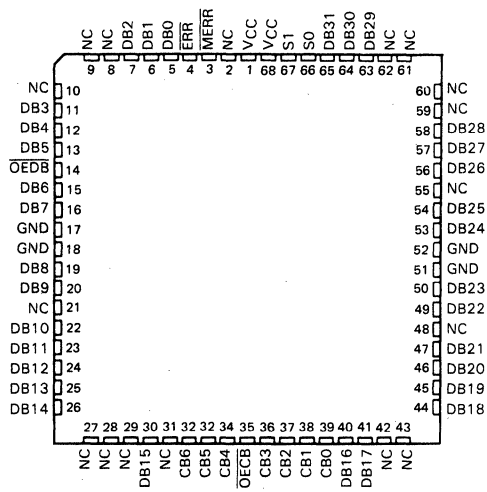
Read-modify-write (byte-control) operations can be performed with the 'AS632 EDAC by using output latch enable, $\overline{\text{LEDBO}}$, and the individual $\overline{\text{OEB0}}$ thru $\overline{\text{OEB3}}$ byte control pins.

Diagnostics are performed on the EDACs by controls and internal paths that allow the user to read the contents of the DB and CB input latches. These will determine if the failure occurred in memory or in the EDAC.

'AS634 . . . JD PACKAGE
(TOP VIEW)



'AS634 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

TABLE 1. WRITE CONTROL FUNCTION

MEMORY CYCLE	EDAC FUNCTION	CONTROL S1	CONTROL S0	DATA I/O	DB CONTROL $\overline{\text{OEBn}}$ OR $\overline{\text{OEDB}}$	DB OUTPUT LATCH ('AS632) $\overline{\text{LEDBO}}$	CHECK I/O	CB CONTROL $\overline{\text{OECB}}$	ERROR FLAGS $\overline{\text{ERR}}$	ERROR FLAGS $\overline{\text{MERR}}$
Write	Generate check word	L	L	Input	H	X	Output check bits†	L	H	H

†See Table 2 for details on check bit generation.

memory write cycle details

During a memory write cycle, the check bits (CB0 thru CB6) are generated internally in the EDAC by seven 16-input parity generators using the 32-bit data word as defined in Table 2. These seven check bits are stored in memory along with the original 32-bit data word. This 32-bit word will later be used in the memory read cycle for error detection and correction.

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TABLE 2. PARITY ALGORITHM

CHECK WORD	32-BIT DATA WORD																													
BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CB0	X		X	X		X					X		X	X	X			X			X		X	X	X	X		X				X
CB1				X		X		X		X		X		X	X	X				X		X		X		X		X		X	X	X
CB2	X		X			X	X		X			X	X			X	X		X			X	X		X			X	X			X
CB3			X	X	X				X	X	X				X	X			X	X	X				X	X	X				X	X
CB4	X	X							X	X	X	X	X	X			X	X							X	X	X	X	X	X		
CB5	X	X	X	X	X	X	X	X									X	X	X	X	X	X	X	X								
CB6	X	X	X	X	X	X	X	X																	X	X	X	X	X	X	X	X

The seven check bits are parity bits derived from the matrix of data bits as indicated by "X" for each bit.

error detection and correction details

During a memory read cycle, the 7-bit check word is retrieved along with the actual data. In order to be able to determine whether the data from memory is acceptable to use as presented to the bus, the error flags must be tested to determine if they are at the high level.

The first case in Table 3 represents the normal, no-error conditions. The EDAC presents highs on both flags. The next two cases of single-bit errors give a high on $\overline{\text{MERR}}$ and a low on $\overline{\text{ERR}}$, which is the signal for a correctable error, and the EDAC should be sent through the correction cycle. The last three cases of double-bit errors will cause the EDAC to signal lows on both $\overline{\text{ERR}}$ and $\overline{\text{MERR}}$, which is the interrupt indication for the CPU.

TABLE 3. ERROR FUNCTION

TOTAL NUMBER OF ERRORS		ERROR FLAGS		DATA CORRECTION
32-BIT DATA WORD	7-BIT CHECK WORD	$\overline{\text{ERR}}$	$\overline{\text{MERR}}$	
0	0	H	H	Not applicable
1	0	L	H	Correction
0	1	L	H	Correction
1	1	L	L	Interrupt
2	0	L	L	Interrupt
0	2	L	L	Interrupt

Error detection is accomplished as the 7-bit check word and the 32-bit data word from memory are applied to internal parity generators/checkers. If the parity of all seven groupings of data and check bits are correct, it is assumed that no error has occurred and both error flags will be high.

If the parity of one or more of the check groups is incorrect, an error has occurred and the proper error flag or flags will be set low. Any single error in the 32-bit data word will change the state of either three or five bits of the 7-bit check word. Any single error in the 7-bit check word changes the state of only that one bit. In either case, the single error flag ($\overline{\text{ERR}}$) will be set low while the dual error flag ($\overline{\text{MERR}}$) will remain high.

Any two-bit error will change the state of an even number of check bits. The two-bit error is not correctable since the parity tree can only identify single-bit errors. Both error flags are set low when any two-bit error is detected.

Three or more simultaneous bit errors can cause the EDAC to believe that no error, a correctable error, or an uncorrectable error has occurred and will produce erroneous results in all three cases. It should be noted that the gross-error conditions of all lows and all highs will be detected.

TABLE 4. READ, FLAG, AND CORRECT FUNCTION

MEMORY CYCLE	EDAC FUNCTION	CONTROL S1	CONTROL S0	DATA I/O	DB CONTROL $\overline{OEBn}$ OR $\overline{OEDB}$	DB OUTPUT LATCH ('AS632) $\overline{LEDBO}$	CHECK I/O	CB CONTROL $\overline{OECB}$	ERROR FLAGS $\overline{ERR}$ $\overline{MERR}$
Read	Read & flag	H	L	Input	H	X	Input	H	Enabled†
Read	Latch input data & check bits	H	H	Latched input data	H	L	Latched input check word	H	Enabled†
Read	Output corrected data & syndrome bits	H	H	Output corrected data word	L	X	Output syndrome bits‡	L	Enabled†

†See Table 3 for error description.
‡See Table 5 for error location.

As the corrected word is made available on the data I/O port (DB0 thru DB31), the check word I/O port (CB0 thru CB6) presents a 7-bit syndrome error code. This syndrome error code can be used to locate the bad memory chip. See Table 5 for syndrome decoding.

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TABLE 5. SYNDROME DECODING

SYNDROME BITS							ERROR
6	5	4	3	2	1	0	
L	L	L	L	L	L	L	unc
L	L	L	L	L	L	H	2-bit
L	L	L	L	L	H	L	2-bit
L	L	L	L	L	H	H	unc
L	L	L	L	H	L	L	2-bit
L	L	L	L	H	L	H	unc
L	L	L	L	H	H	L	unc
L	L	L	L	H	H	H	2-bit
L	L	L	H	L	L	L	2-bit
L	L	L	H	L	L	H	unc
L	L	L	H	L	H	L	DB31
L	L	L	H	L	H	H	2-bit
L	L	L	H	H	L	L	unc
L	L	L	H	H	L	H	2-bit
L	L	L	H	H	H	L	2-bit
L	L	L	H	H	H	H	DB30
L	L	H	L	L	L	L	2-bit
L	L	H	L	L	L	H	unc
L	L	H	L	L	H	L	DB29
L	L	H	L	L	H	H	2-bit
L	L	H	L	H	L	L	DB28
L	L	H	L	H	L	H	2-bit
L	L	H	L	H	H	L	2-bit
L	L	H	L	H	H	H	DB27
L	L	H	H	L	L	L	DB26
L	L	H	H	L	L	H	2-bit
L	L	H	H	L	H	L	2-bit
L	L	H	H	L	H	H	DB25
L	L	H	H	H	L	L	2-bit
L	L	H	H	H	L	H	DB24
L	L	H	H	H	H	L	unc
L	L	H	H	H	H	H	2-bit

SYNDROME BITS							ERROR
6	5	4	3	2	1	0	
L	H	L	L	L	L	L	2-bit
L	H	L	L	L	L	H	unc
L	H	L	L	L	H	L	DB7
L	H	L	L	L	H	H	2-bit
L	H	L	L	H	L	L	DB6
L	H	L	L	H	L	H	2-bit
L	H	L	L	H	H	L	2-bit
L	H	L	L	H	H	H	DB5
L	H	L	H	L	L	L	DB4
L	H	L	H	L	L	H	2-bit
L	H	L	H	L	H	L	2-bit
L	H	L	H	L	H	H	DB3
L	H	L	H	H	L	L	2-bit
L	H	L	H	H	L	H	DB2
L	H	L	H	H	H	L	unc
L	H	L	H	H	H	H	2-bit
L	H	H	L	L	L	L	DB0
L	H	H	L	L	L	H	2-bit
L	H	H	L	L	H	L	2-bit
L	H	H	L	L	H	H	unc
L	H	H	L	H	L	L	2-bit
L	H	H	L	H	L	H	DB1
L	H	H	L	H	H	L	unc
L	H	H	L	H	H	H	2-bit
L	H	H	H	L	L	L	unc
L	H	H	H	L	L	H	unc
L	H	H	H	L	H	L	unc
L	H	H	H	L	H	H	2-bit
L	H	H	H	H	L	L	unc
L	H	H	H	H	L	H	2-bit
L	H	H	H	H	H	L	2-bit
L	H	H	H	H	H	H	CB6

SYNDROME BITS							ERROR
6	5	4	3	2	1	0	
H	L	L	L	L	L	L	2-bit
H	L	L	L	L	L	H	unc
H	L	L	L	L	H	L	unc
H	L	L	L	L	H	H	2-bit
H	L	L	L	H	L	L	unc
H	L	L	L	H	L	H	2-bit
H	L	L	L	H	H	L	2-bit
H	L	L	L	H	H	H	unc
H	L	L	H	L	L	L	unc
H	L	L	H	L	L	H	2-bit
H	L	L	H	L	H	L	2-bit
H	L	L	H	L	H	H	DB15
H	L	L	H	H	L	L	2-bit
H	L	L	H	H	L	H	unc
H	L	L	H	H	H	L	DB14
H	L	L	H	H	H	H	2-bit
H	L	H	L	L	L	L	unc
H	L	H	L	L	L	H	2-bit
H	L	H	L	L	H	L	2-bit
H	L	H	L	L	H	H	DB13
H	L	H	L	H	L	L	2-bit
H	L	H	L	H	L	H	DB12
H	L	H	L	H	H	L	DB11
H	L	H	L	H	H	H	2-bit
H	L	H	H	L	L	L	2-bit
H	L	H	H	L	L	H	DB10
H	L	H	H	L	H	L	DB9
H	L	H	H	L	H	H	2-bit
H	L	H	H	H	L	L	DB8
H	L	H	H	H	L	H	DB1
H	L	H	H	H	H	L	2-bit
H	L	H	H	H	H	H	CB5

SYNDROME BITS							ERROR
6	5	4	3	2	1	0	
H	H	L	L	L	L	L	unc
H	H	L	L	L	L	H	2-bit
H	H	L	L	L	H	L	2-bit
H	H	L	L	L	H	H	DB23
H	H	L	L	H	L	L	2-bit
H	H	L	L	H	L	H	DB22
H	H	L	L	H	H	L	DB21
H	H	L	L	H	H	H	2-bit
H	H	L	H	L	L	L	2-bit
H	H	L	H	L	L	H	DB20
H	H	L	H	L	H	L	DB19
H	H	L	H	L	H	H	2-bit
H	H	L	H	H	L	L	DB18
H	H	L	H	H	L	H	2-bit
H	H	L	H	H	H	L	2-bit
H	H	L	H	H	H	H	CB4
H	H	H	L	L	L	L	2-bit
H	H	H	L	L	L	H	DB16
H	H	H	L	L	H	L	unc
H	H	H	L	L	H	H	2-bit
H	H	H	L	H	L	L	DB17
H	H	H	L	H	L	H	2-bit
H	H	H	L	H	H	L	2-bit
H	H	H	L	H	H	H	CB3
H	H	H	H	L	L	L	unc
H	H	H	H	L	L	H	2-bit
H	H	H	H	L	H	L	2-bit
H	H	H	H	L	H	H	CB2
H	H	H	H	H	L	L	2-bit
H	H	H	H	H	L	H	CB1
H	H	H	H	H	H	L	CB0
H	H	H	H	H	H	H	none

CB X= error in check bit X
DB Y= error in data bit Y
2-bit = double-bit error
unc = uncorrectable multibit error

read-modify-write (byte control) operations

The 'AS632 is capable of byte-write operations. The 39-bit word from memory must first be latched into the DB and CB input latches. This is easily accomplished by switching from the read and flag mode (S1 = H, S0 = L) to the latch input mode (S1 = H, S0 = H). The EDAC will then make any corrections, if necessary, to the data word and place it at the input of the output data latch. This data word must then be latched into the output data latch by taking $\overline{\text{LEDBO}}$ from a low to a high.

Byte control can now be employed on the data word through the $\overline{\text{OEB0}}$ through $\overline{\text{OEB3}}$ controls. $\overline{\text{OEB0}}$ controls DB0-DB7 (byte 0), $\overline{\text{OEB1}}$ controls DB8-DB15 (byte 1), $\overline{\text{OEB2}}$ controls DB16-DB23 (byte 2), and $\overline{\text{OEB3}}$ controls DB24-DB31 (byte 3). Placing a high on the byte control will disable the output and the user can modify the byte. If a low is placed on the byte control, then the original byte is allowed to pass onto the data bus unchanged. If the original data word is altered through byte control, a new check word must be generated before it is written back into memory. This is easily accomplished by taking control S1 and S0 low. Table 6 lists the read-modify-write functions.

TABLE 6. READ-MODIFY-WRITE FUNCTION

MEMORY CYCLE	EDAC FUNCTION	CONTROL S1	CONTROL S0	BYTEn†	$\overline{OEB}$n†	DB OUTPUT LATCH $\overline{LEDBO}$	CHECK I/O	CB CONTROL	ERROR FLAG $\overline{ERR}$	ERROR FLAG $\overline{MERR}$
Read	Read & Flag	H	L	Input	H	X	Input	H	Enabled	
Read	Latch input data & check bits	H	H	Latched Input data	H	L	Latched input check word	H	Enabled	
Read	Latch corrected data word into output latch	H	H	Latched output data word	H	H	Hi-Z	H	Enabled	
							Output Syndrome bits	L		
Modify /write	Modify appropriate byte or bytes & generate new check word	L	L	Input modified BYTE0	H	H	Output check word	L	H	H
				Output unchanged BYTE0	L					

†$\overline{OEB}$0 controls DB0-DB7 (BYTE0), $\overline{OEB}$1 controls DB8-DB15 (BYTE1), $\overline{OEB}$3 controls DB16-DB23 (BYTE2), $\overline{OEB}$3 controls DB24-DB31 (BYTE3).

diagnostic operations

The 'AS632 and 'AS634 are capable of diagnostics that allow the user to determine whether the EDAC or the memory is failing. The diagnostic function tables will help the user to see the possibilities for diagnostic control.

In the diagnostic mode (S1 = L, S0 = H), the checkword is latched into the input latch while the data input latch remains transparent. This lets the user apply various data words against a fixed known checkword. If the user applies a diagnostic data word with an error in any bit location, the $\overline{ERR}$ flag should be low. If a diagnostic data word with two errors in any bit location is applied, the $\overline{MERR}$ flag should be low. After the checkword is latched into the input latch, it can be verified by taking $\overline{OECB}$ low. This outputs the latched checkword. With the 'AS632, the diagnostic data word can be latched into the output data latch and verified. It should be noted that the 'AS634 does not have this pass-through capability because they do not contain an output data latch. By changing from the diagnostic mode (S1 = L, S0 = H) to the correction mode (S1 = H, S0 = H), the user can verify that the EDAC will correct the diagnostic data word. Also, the syndrome bits can be produced to verify that the EDAC pinpoints the error location. Table 7 ('AS632) and Table 8 ('AS634) list the diagnostic functions.

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TABLE 7. 'AS632 DIAGNOSTIC FUNCTION

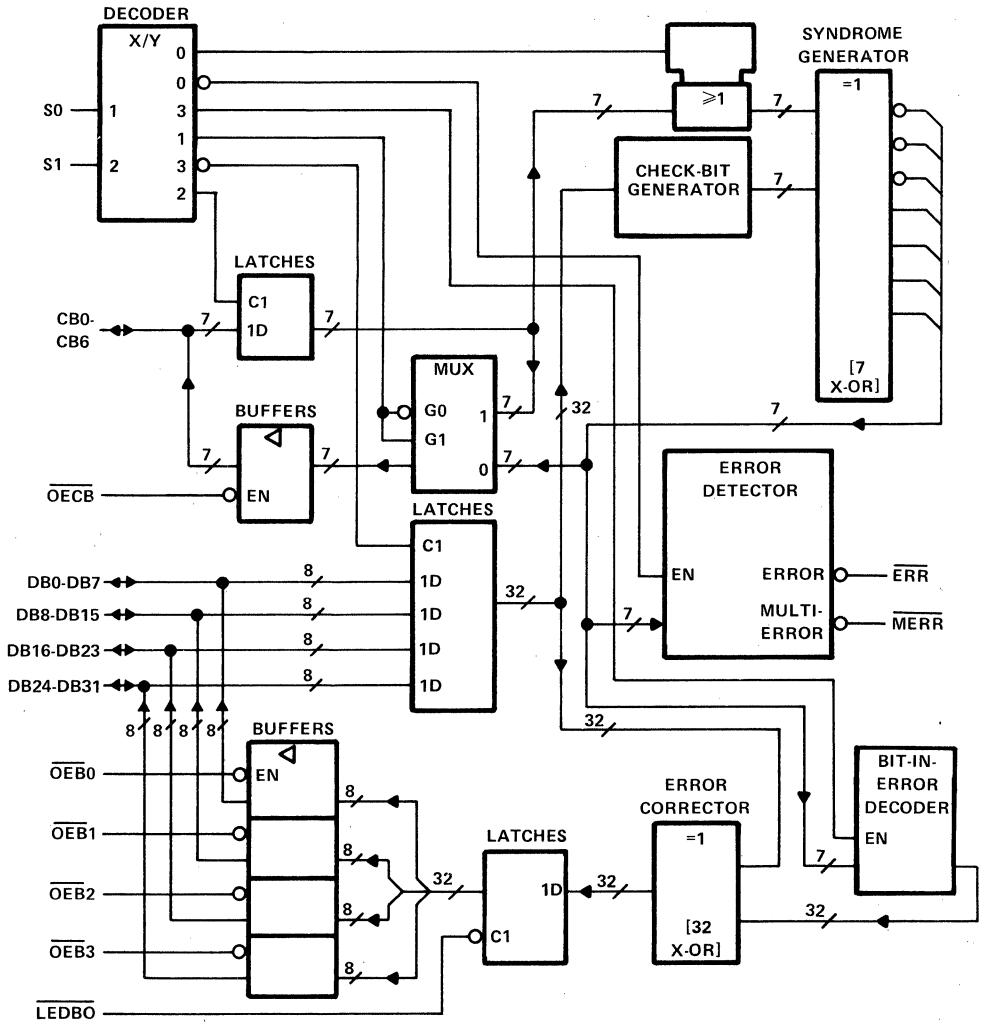
EDAC FUNCTION	CONTROL S1	CONTROL S0	DATA I/O	DB BYTE CONTROL $\overline{OEBn}$	DB OUTPUT LATCH $\overline{LEDBO}$	CHECK I/O	CB CONTROL $\overline{OECB}$	ERROR FLAGS $\overline{ERR}$	ERROR FLAGS $\overline{MERR}$
Read & flag	H	L	Input correct data word	H	X	Input correct check bits	H	H	H
Latch input check word while data input latch remains transparent	L	H	Input diagnostic data word†	H	L	Latched input check bits	H	Enabled	
Latch diagnostic data word into output latch	L	H	Input diagnostic data word†	H	H	Output latched check bits	L	Enabled	
						Hi-Z	H		
Latch diagnostic data word into input latch	H	H	Latched input diagnostic data word	H	H	Output syndrome bits	L	Enabled	
						Hi-Z	H		
Output diagnostic data word & syndrome bits	H	H	Output diagnostic data word	L	H	Output syndrome bits	L	Enabled	
						Hi-Z	H		
Output corrected diagnostic data word & output syndrome bits	H	H	Output corrected diagnostic data word	L	L	Output syndrome bits	L	Enabled	
						Hi-Z	H		

TABLE 8. 'AS634 DIAGNOSTIC FUNCTION

EDAC FUNCTION	CONTROL S1	CONTROL S0	DATA I/O	DB CONTROL $\overline{OEDB}$	CHECK I/O	CB CONTROL $\overline{OECB}$	ERROR FLAGS $\overline{ERR}$	ERROR FLAGS $\overline{MERR}$
Read & flag	H	L	Input correct data word	H	Input correct check bits	H	H	H
Latch input check bits while data input latch remains transparent	L	H	Input diagnostic data word†	H	Latched input check bits	H	Enabled	
Output input check bits	L	H	Input diagnostic data word†	H	Output input check bits	L	Enabled	
Latch diagnostic data into input latch	H	H	Latched input diagnostic data word	H	Output syndrome bits	L	Enabled	
					Hi-Z	H		
Output corrected diagnostic data word	H	H	Output corrected diagnostic data word	L	Output syndrome bits	L	Enabled	
					Hi-Z	H		

†Diagnostic data is a data word with an error in one bit location except when testing the $\overline{MERR}$ error flag. In this case, the diagnostic data word will contain errors in two bit locations.

'AS632 logic diagram (positive logic)



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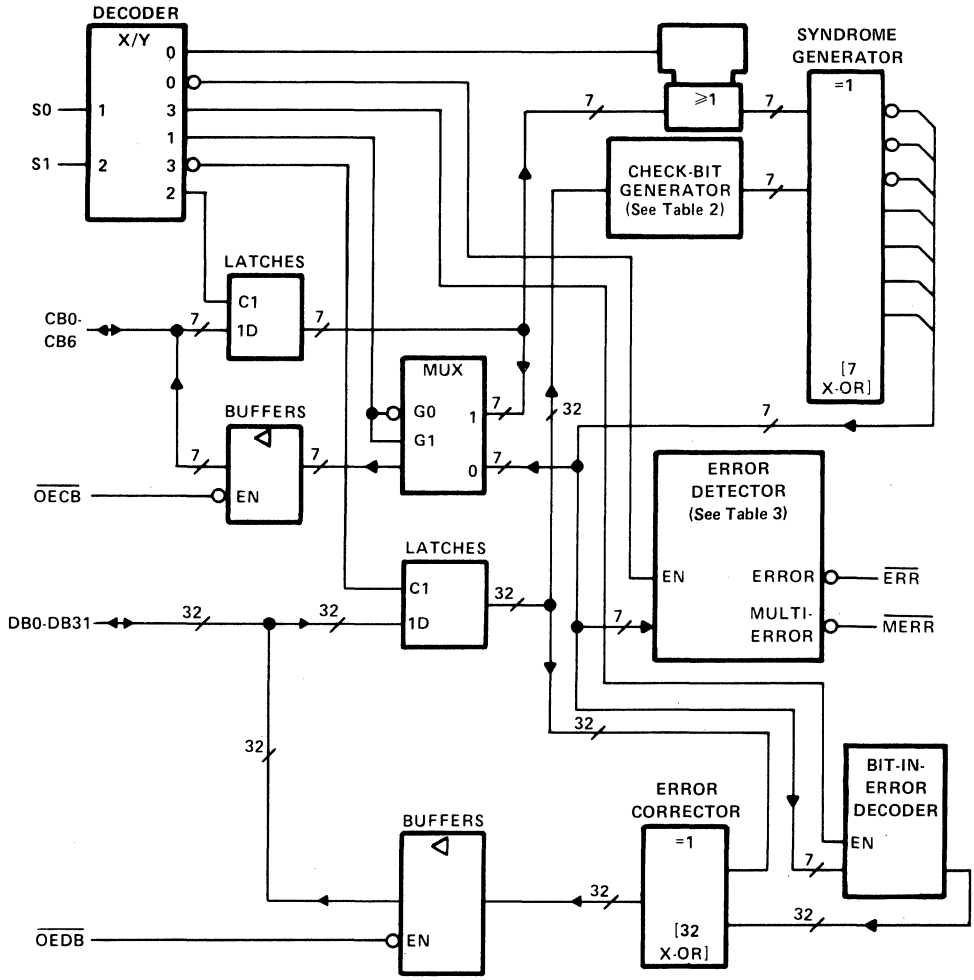
'AS634 logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: CB and DB . . . . . 5.5 V
All others . . . . . 7 V
Operating free-air temperature range:
SN74AS632, SN74AS634 . . . . . 0°C to 70°C
Operating case temperature range:
SN54AS632, SN54AS634 . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54AS632 SN54AS634			SN74AS632 SN74AS634			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current	$\overline{ERR}$ or $\overline{MERR}$			−0.4			−0.4	mA
		DB or CB			−1			−2.6	
I_{OL}	Low-level output current	$\overline{ERR}$ or $\overline{MERR}$			4			8	mA
		DB or CB			12			24	
t_w	Pulse duration	$\overline{LEDBO}$ low							ns
t_{su}	Setup time	(1) Data and check word before S0↑ (S1 = H)							ns
		(2) S0 high before $\overline{LEDBO}$↑ (S1 = H)†							
		(3) $\overline{LEDBO}$ high before the earlier of S0↓ or S1↓†							
		(4) $\overline{LEDBO}$ high before S1↑ (S0 = H)							
		(5) Diagnostic data word before S1↑ (S0 = H)							
		(6) Diagnostic check word before the later of S1↓ or S0↑							
		(7) Diagnostic data word before $\overline{LEDBO}$↑ (S1 = L and S0 = H)‡							
t_h	Hold time	(8) Read-mode, S0 low and S1 high							ns
		(9) Data and check word after S0↑ (S1 = H)							
		(10) Data word after S1↑ (S0 = H)							
		(11) Check word after the later of S1↓ or S0↑							
		(12) Diagnostic data word after $\overline{LEDBO}$↑ (S1 = L, S0 = H)‡							
t_{corr}	Correction time (see Figure 1)								ns
T_C	Operating case temperature		−55		125				°C
T_A	Operating free-air temperature					0		70	°C

† These times ensure that corrected data is saved in the output data latch.
‡ These times ensure that the diagnostic data word is saved in the output data latch.

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'AS632, 'AS634 electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS632 SN54AS634			SN74AS632 SN74AS634			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	All outputs	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	DB or CB	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	$\overline{ERR}$ or $\overline{MERR}$	V_{CC} = 4.5 V,	I_{OH} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
	DB or CB	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	S0 or S1	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	All others	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	DB or CB‡	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	All others‡					20			20	
I_{IL}	S0 or S1	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.4			−0.4	mA
	All others‡					−0.1			−0.1	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		150			150		mA

NOTE 1: I_{CC} is measured with S0 and S1 at 4.5 V and all CB and DB pins grounded.

'AS632 switching characteristics, V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, T_C = −55°C to 125°C for SN54AS632, T_A = 0°C to 70°C for SN74AS632

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54AS632			SN74AS632			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{pd}	DB and CB	$\overline{ERR}$	S1 = H, S0 = L, R_L = 500 Ω		17			17		ns
	DB	$\overline{ERR}$	S1 = L, S0 = H, R_L = 500 Ω		17			17		
t_{pd}	DB and CB	$\overline{MERR}$	S1 = H, S0 = L, R_L = 500 Ω		26			26		ns
	DB	$\overline{MERR}$	S1 = L, S0 = H, R_L = 500 Ω		26			26		
t_{pd}	S0↓ and S1↓	CB	R1 = R2 = 500 Ω		26			26		ns
t_{PLH}	S0↓ and S1↓	$\overline{ERR}$	R_L = 500 Ω		9			9		ns
t_{pd}	DB	CB	S1 = L, S0 = L, R1 = R2 = 500 Ω		26			26		ns
t_{pd}	$\overline{LEDBO}$↓	DB	S1 = X, S0 = H, R1 = R2 = 500 Ω		17			17		ns
t_{pd}	S1↑	CB	S0 = H, R1 = R2 = 500 Ω		26			26		ns
t_{en}	$\overline{OECB}$↓	CB	S0 = H, S1 = X, R1 = R2 = 500 Ω		12			12		ns
t_{dis}	$\overline{OECB}$↑	CB	S0 = H, S1 = X, R1 = R2 = 500 Ω		12			12		ns
t_{en}	$\overline{OEB0}$ thru $\overline{OEB3}$↓	DB	S0 = H, S1 = X, R1 = R2 = 500 Ω		12			12		ns
t_{dis}	$\overline{OEB0}$ thru $\overline{OEB3}$↑	DB	S0 = H, S1 = X, R1 = R2 = 500 Ω		12			12		ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'AS634 switching characteristics, V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, T_C = −55°C to 125°C for SN54AS634, T_A = 0°C to 70°C for SN74AS634

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54AS634			SN74AS634			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{pd}	DB and CB	$\overline{ERR}$	S1 = H, S0 = L, R_L = 500 Ω		17			17		ns
			S1 = L, S0 = H, R_L = 500 Ω		17			17		
t_{pd}	DB and CB	$\overline{MERR}$	S1 = H, S0 = L, R_L = 500 Ω		26			26		ns
			S1 = L, S0 = H, R_L = 500 Ω		26			26		
t_{pd}	S0↓ and S1↓	CB	R1 = R2 = 500 Ω		23			23		ns
t_{PLH}	S0↓ and S1↓	$\overline{ERR}$	R_L = 500 Ω		9			9		ns
t_{pd}	DB	CB	S1 = L, S0 = L, R1 = R2 = 500 Ω		23			23		ns
t_{pd}	S1↑	CB	S0 = H, R1 = R2 = 500 Ω		23			23		ns
t_{en}	$\overline{OECB}$↓	CB	S1 = X, S0 = H, R1 = R2 = 500 Ω		12			12		ns
t_{dis}	$\overline{OECB}$↑	CB	S1 = X, S0 = H, R1 = R2 = 500 Ω		12			12		ns
t_{en}	$\overline{OEDB}$↓	DB	S1 = X, S0 = H, R1 = R2 = 500 Ω		12			12		ns
t_{dis}	$\overline{OEDB}$↑	DB	S1 = X, S0 = H, R1 = R2 = 500 Ω		12			12		ns

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

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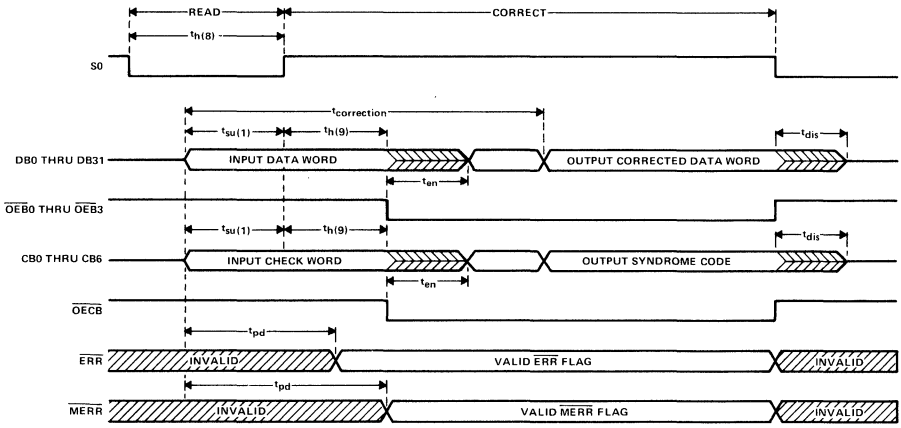

FIGURE 1. READ, FLAG, AND CORRECT MODE SWITCHING WAVEFORMS

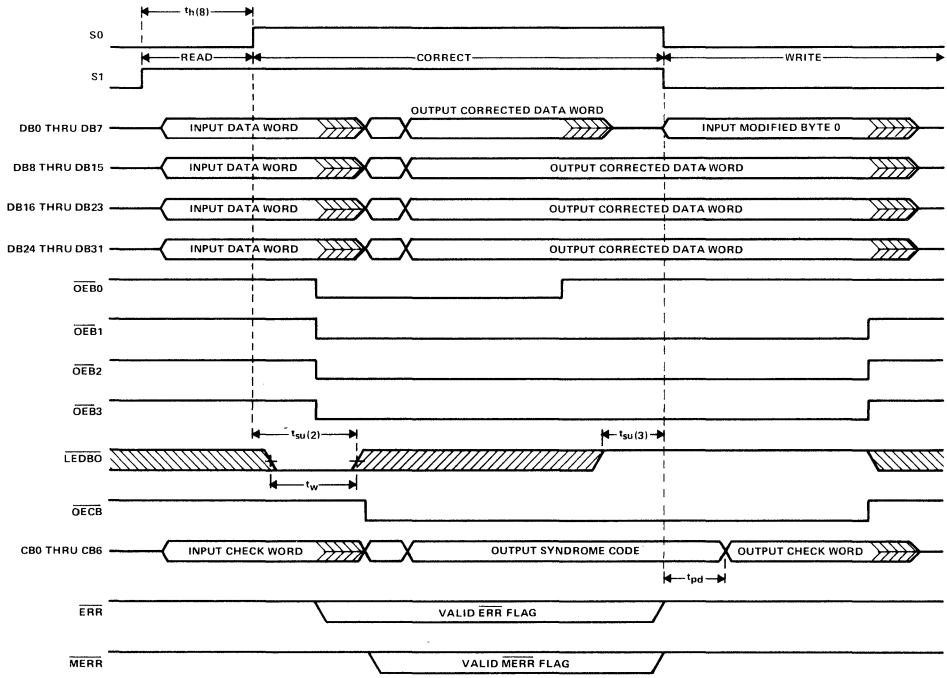

FIGURE 2. READ, CORRECT, MODIFY MODE SWITCHING WAVEFORMS

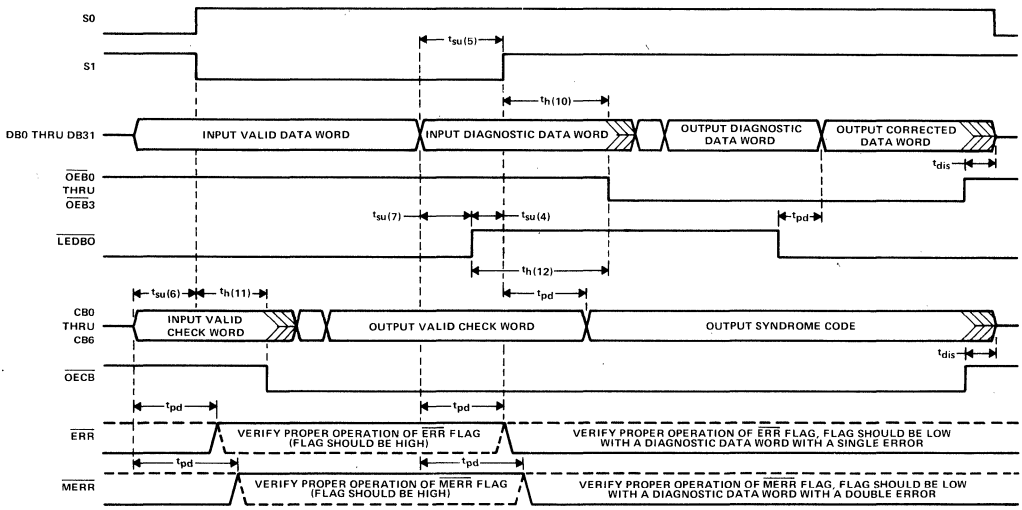

FIGURE 3. DIAGNOSTIC MODE SWITCHING WAVEFORM

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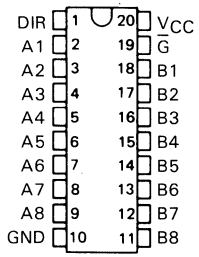
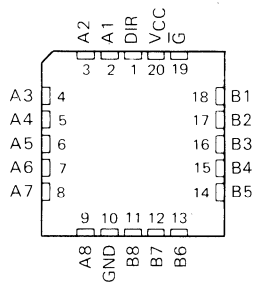
D2261, DECEMBER 1983 – REVISED MAY 1986

- **Bidirectional Bus Transceivers in High-Density 20-Pin Packages**
- **Choice of True or Inverting Logic**
- **A Bus Outputs are Open-Collector; B Bus Outputs are 3-State**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS', SN54AS' . . . J PACKAGE
SN74ALS', SN74AS' . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS', SN54AS' . . . FK PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed for asynchronous two-way communication between open-collector and 3-state buses. The devices transmit data from the A bus (open-collector) to the B bus (3-state) or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so the buses are isolated.

DEVICE	A OUTPUT	B OUTPUT	LOGIC
'ALS638A, 'AS638	Open-Collector	3-State	Inverting
'ALS639A, 'AS639	Open-Collector	3-State	True

The –1 versions of the SN74ALS' parts are identical to the standard versions except that recommended maximum of I_{OL} is increased to 48 milliamperes. There are no –1 versions of the SN54ALS' parts.

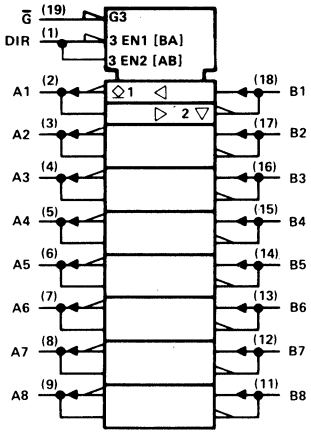
The SN54' family is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

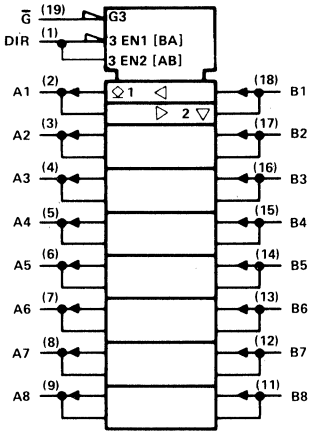
CONTROL INPUTS		OPERATION	
$\overline{G}$	DIR	'ALS638A 'AS638	'ALS639A 'AS639
L	L	$\overline{B}$ data to A bus	B data to A bus
L	H	$\overline{A}$ data to B bus	A data to B bus
H	X	Isolation	Isolation

logic symbols†

'ALS638A, 'AS638

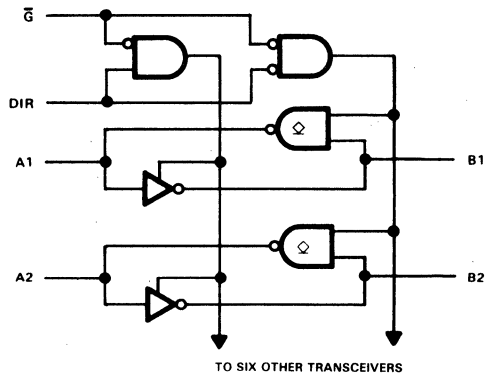


'ALS639A, 'AS639

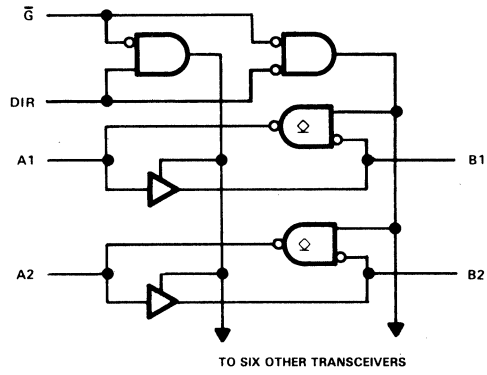


logic diagrams (positive logic)

'ALS638A, 'AS638



'ALS639A, 'AS639



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
A bus I/O ports . . . . . 7 V
B bus I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS638A, SN54ALS639A . . . . . −55°C to 125°C
SN74ALS638A, SN74ALS639A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS638A SN54ALS639A			SN74ALS638A SN74ALS639A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
V_{OH}	High-level output voltage	A ports			5.5			5.5	V
I_{OH}	High-level output current	B ports			−12			−15	mA
I_{OL}	Low-level output current	A or B ports			12			24	mA
								48†	
T_A	Operating free-air temperature		−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48-mA limit applies for the SN74ALS638A-1 and SN74ALS639A-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS638A SN54ALS639A			SN74ALS638A SN74ALS639A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	A ports	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OH}	B ports	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}	A or B ports	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, (I_{OL} = 48 mA for −1 versions)	I_{OL} = 24 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports§					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	A or B ports§					−0.1			−0.1	
I_O¶	B ports	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS638A	V_{CC} = 5.5 V	Outputs high		18	36		18	30	mA
			Outputs low		25	48		26	41	
			Outputs disabled		16	35		16	30	
	'ALS639A		Outputs high		25	45		25	40	
			Outputs low		30	55		30	50	
			Outputs disabled		33	60		33	54	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C
§For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
¶The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS638A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω (A outputs), R1 = R2 = 500 Ω (B outputs), T_A = MIN to MAX				UNIT
			SN54ALS638A		SN74ALS638A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2	15	2	12	ns
t_{PHL}			2	15	2	12	
t_{PLH}	B	A	8	30	8	25	ns
t_{PHL}			8	35	8	30	
t_{PLH}	$\overline{G}$	A	5	30	5	25	ns
t_{PHL}			10	50	10	45	
t_{PZH}	$\overline{G}$	B	5	25	5	20	ns
t_{PZL}			5	28	5	22	
t_{PHZ}	$\overline{G}$	B	2	12	2	10	ns
t_{PLZ}			3	18	3	15	

'ALS639A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω (A outputs), R1 = R2 = 500 Ω (B outputs), T_A = MIN to MAX				UNIT
			SN54ALS639A		SN74ALS639A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2	15	2	12	ns
t_{PHL}			2	15	2	12	
t_{PLH}	B	A	10	35	10	30	ns
t_{PHL}			5	28	5	22	
t_{PLH}	$\overline{G}$	A	10	35	10	30	ns
t_{PHL}			10	40	10	35	
t_{PZH}	$\overline{G}$	B	6	28	6	21	ns
t_{PZL}			8	30	8	25	
t_{PHZ}	$\overline{G}$	B	2	12	2	10	ns
t_{PLZ}			3	19	3	16	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
A bus I/O ports . . . . . 7 V
B bus I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54AS638, SN54AS639 . . . . . −55°C to 125°C
SN74AS638, SN74AS639 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54AS638 SN54AS639			SN74AS638 SN74AS639			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{OH}	High-level output voltage	A ports			5.5			5.5	V
I_{OH}	High-level output current	B ports			−12			−15	mA
I_{OL}	Low-level output current	A or B ports			48			64	mA
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS638 SN54AS639			SN74AS638 SN74AS639			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
I_{OH}	A ports	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OH}	B ports	V_{CC} = 4.5 V, to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4			
V_{OL}	A or B ports	V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.3	0.55				V
		V_{CC} = 4.5 V,	I_{OL} = 64 mA					0.35	0.55	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports‡					70			70	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	A or B ports‡					−0.75			−0.75	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−50		−150	−50		−150	mA
I_{CC}	'AS638	V_{CC} = 5.5 V	Outputs high		24	40		24	40	mA
			Outputs low		75	122		75	122	
			Outputs disabled		37	61		37	61	
	'AS639		Outputs high		56	92		56	92	
			Outputs low		95	154		95	154	
			Outputs disabled		62	100		62	100	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'AS638 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω (A outputs), R1 = R2 = 500 Ω (B outputs), T_A = MIN to MAX				UNIT
			SN54AS638		SN74AS638		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2	8	2	7	ns
t_{PHL}			2	7.5	2	6.5	
t_{PLH}	B	A	5	23	5	20	ns
t_{PHL}			2	8	2	7	
t_{PLH}	$\overline{G}$	A	5	20	5	19	ns
t_{PHL}			2	10	2	9	
t_{PZH}	$\overline{G}$	B	2	10	2	8	ns
t_{PZL}			2	12	2	10	
t_{PHZ}	$\overline{G}$	B	2	8	2	7	ns
t_{PLZ}			2	12	2	10	

'AS639 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω (A outputs), R1 = R2 = 500 Ω (B outputs), T_A = MIN to MAX				UNIT
			SN54AS639		SN74AS639		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2	11	2	9.5	ns
t_{PHL}			2	10.5	2	9	
t_{PLH}	B	A	5	25	5	22	ns
t_{PHL}			2	10	2	9	
t_{PLH}	$\overline{G}$	A	5	23	5	21.5	ns
t_{PHL}			2	12.5	2	11.5	
t_{PZH}	$\overline{G}$	B	2	12	2	10.5	ns
t_{PZL}			2	12	2	10.5	
t_{PHZ}	$\overline{G}$	B	2	7.5	2	7	ns
t_{PLZ}			2	12	2	10.5	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

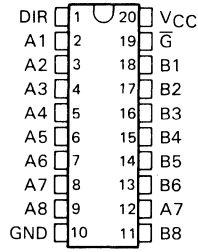
OCTAL BUS TRANSCEIVERS

D2661, DECEMBER 1983—REVISED MAY 1986

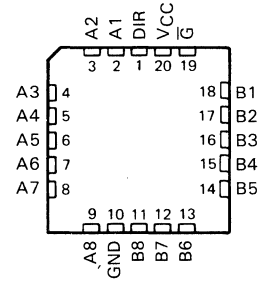
- **Bidirectional Bus Transceivers in High-Density 20-Pin Packages**
- **Choice of True or Inverting Logic**
- **Choice of 3-State or Open-Collector Outputs**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

DEVICE	OUTPUT	LOGIC
'ALS640A, 'AS640	3-State	Inverting
'ALS641A, 'AS641	Open-Collector	True
'ALS642A, 'AS642	Open-Collector	Inverting
'ALS643A, 'AS643	3-State	True and Inverting
'ALS644A, 'AS644	Open-Collector	True and Inverting
'ALS645A, 'AS645	3-State	True

SN54ALS', SN54AS' . . . J PACKAGE
SN74ALS', SN74AS' . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS', SN54AS' . . . FK PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so the buses are effectively isolated.

The -1 versions of the SN74ALS' parts are identical to the standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes. There are no -1 versions of the SN54ALS' parts.

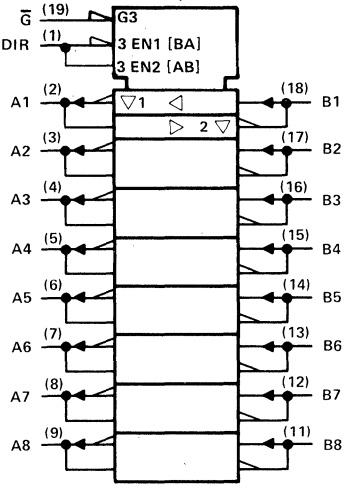
The SN54' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

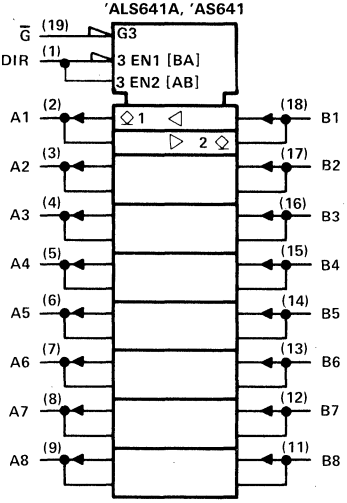
CONTROL INPUTS		OPERATION		
$\overline{G}$	DIR	'ALS640A, 'AS640 'ALS642A, 'AS642	'ALS641A, 'AS641 'ALS645A, 'AS645	'ALS643A, 'AS643 'ALS644A, 'AS644
L	L	$\overline{B}$ data to A bus	B data to A bus	B data to A bus
L	H	$\overline{A}$ data to B bus	A data to B bus	$\overline{A}$ data to B bus
H	X	Isolation	Isolation	Isolation

logic symbols†

'ALS640A, 'AS640

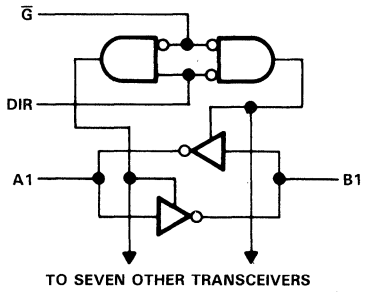


'ALS641A, 'AS641

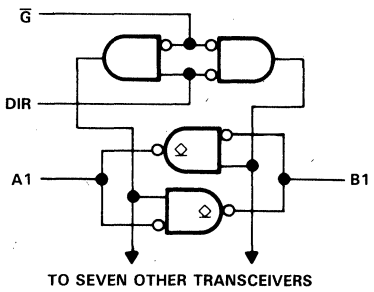


logic diagrams (positive logic)

'ALS640A, 'AS640



'ALS641A, 'AS641



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

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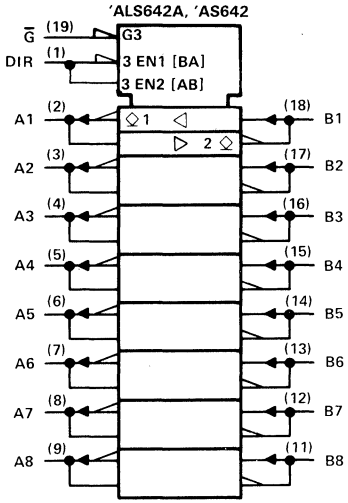
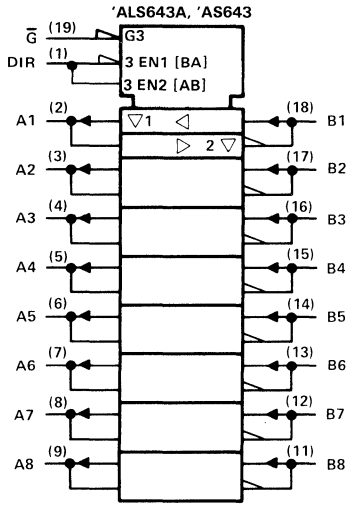
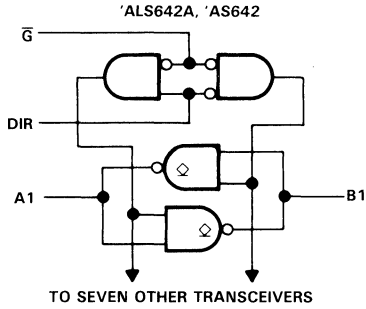
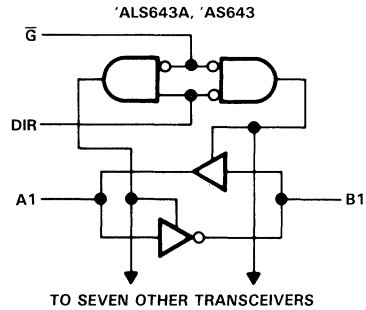
logic symbols†





logic diagrams (positive logic)

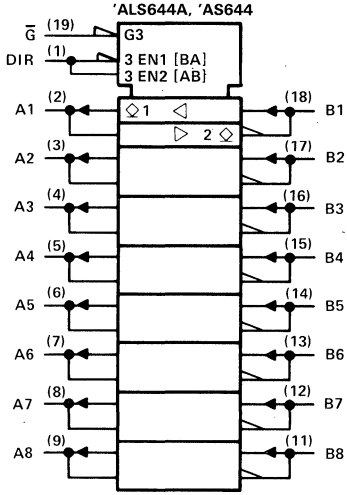




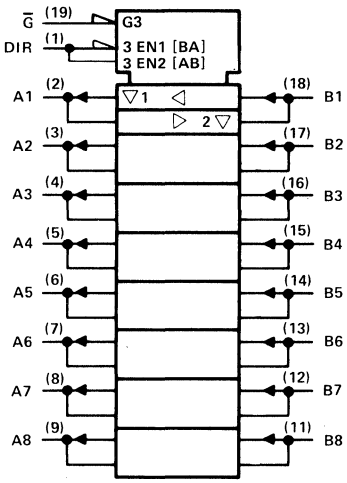
† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

logic symbols†

'ALS644A, 'AS644

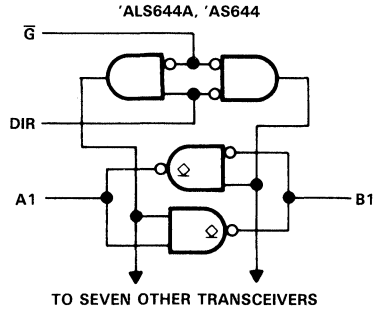


'ALS645A, 'AS645

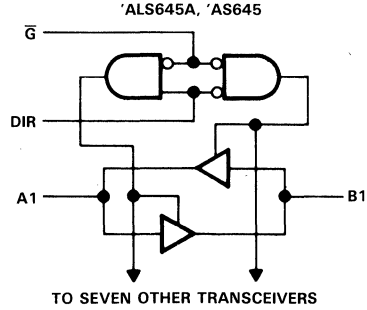


logic diagrams (positive logic)

'ALS644A, 'AS644



'ALS645A, 'AS645



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS640A, SN54ALS643A, SN54ALS645A . . . . . −55 °C to 125 °C
SN74ALS640A, SN74ALS643A, SN74ALS645A . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS640A SN54ALS643A SN54ALS645A			SN74ALS640A SN74ALS643A SN74ALS645A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
							48†	
T_A	Operating free-air temperature	−55		125	0		70	°C

† The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48-mA limit applies for the SN74ALS640A-1, SN74ALS643A-1, and SN74ALS645A-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS'			SN74ALS'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, (I_{OL} = 48 mA for −1 versions)	I_{OL} = 24 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports§					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	A or B ports§					−0.1			−0.1	
I_O¶		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS640A	V_{CC} = 5.5 V	Outputs high		19	35		19	30	mA
			Outputs low		27	45		27	40	
			Outputs disabled		28	48		28	43	
	'ALS643A		Outputs high		25	37		25	35	
			Outputs low		33	47		33	45	
			Outputs disabled		35	50		35	48	
	'ALS645A		Outputs high		30	48		30	45	
			Outputs low		36	60		36	55	
			Outputs disabled		38	63		38	58	

‡ All typical values are at V_{CC} = 5 V, T_A = 25 °C.
§ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
¶ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS640A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS640A		SN74ALS640A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	2	14	2	11	ns
t_{PHL}			2	13	2	10	
t_{PZH}	$\overline{G}$	A or B	5	25	5	21	ns
t_{PZL}			8	27	8	24	
t_{PHZ}	$\overline{G}$	A or B	2	12	2	10	ns
t_{PLZ}			3	20	3	15	

'ALS643A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS643A		SN74ALS643A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2	15	2	13	ns
t_{PHL}			2	13	2	11	
t_{PLH}	B	A	2	15	2	13	ns
t_{PHL}			2	13	2	11	
t_{PZH}	$\overline{G}$	A	5	28	5	25	ns
t_{PZL}			5	28	5	25	
t_{PHZ}	$\overline{G}$	A	2	12	2	10	ns
t_{PLZ}			3	22	3	17	
t_{PZH}	$\overline{G}$	B	5	28	5	25	ns
t_{PZL}			5	28	5	25	
t_{PHZ}	$\overline{G}$	B	2	12	2	10	ns
t_{PLZ}			3	22	3	17	

'ALS645A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS645A		SN74ALS645A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1	19	3	10	ns
t_{PHL}			1	14	3	10	
t_{PZH}	$\overline{G}$	A or B	2	30	5	20	ns
t_{PZL}			2	29	5	20	
t_{PHZ}	$\overline{G}$	A or B	2	14	2	10	ns
t_{PLZ}			2	30	4	15	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs and I/O ports . . . . . 7 V
Operating free-air temperature range:
SN54ALS641A, SN54ALS642A, SN54ALS644A . . . . . −55°C to 125°C
SN74ALS641A, SN74ALS642A, SN74ALS644A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS641A SN54ALS642A SN54ALS644A			SN74ALS641A SN74ALS642A SN74ALS644A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
V_{OH}	High-level output current			5.5			5.5	V
I_{OL}	Low-level output current			12			24	mA
							48†	
T_A	Operating free-air temperature	−55		125	0		70	°C

† The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48-mA limit applies for the SN74ALS641A-1, SN74ALS642A-1, and SN74ALS644A-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			SN54ALS641A SN54ALS642A SN54ALS644A			SN74ALS641A SN74ALS642A SN74ALS644A			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.5			−1.5	V
I_{OH}		V_{CC} = 4.5 V,	V_{OH} = 5.5 V				0.1			0.1	mA
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA			0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, (I_{OL} = 48 mA for -1 versions)	I_{OL} = 24 mA						0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V				0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V				0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V				20			20	μA
	A or B ports§						20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V				−0.1			−0.1	mA
	A or B ports§						−0.1			−0.1	
I_{CC}	'ALS641A	V_{CC} = 5.5 V		Outputs high		25	40		25	37	mA
				Outputs low		33	50		33	47	
	'ALS642A			Outputs high		8	15		8	15	
				Outputs low		18	28		18	28	
	'ALS644A			Outputs high		16	32		16	29	
				Outputs low		25	44		25	40	

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

'ALS641A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX				UNIT
			SN54ALS641A		SN74ALS641A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	5	30	5	25	ns
t_{PHL}			3	23	3	18	
t_{PLH}	$\overline{G}$	A or B	8	35	8	30	ns
t_{PHL}			8	35	8	30	
t_{PLH}	DIR	A or B	8	37	8	32	ns
t_{PHL}			8	37	8	32	

'ALS642A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX				UNIT
			SN54ALS642A		SN74ALS642A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	10	35	10	30	ns
t_{PHL}			5	25	5	22	
t_{PLH}	$\overline{G}$ or DIR	A or B	10	35	10	30	ns
t_{PHL}			15	43	15	38	

'ALS644A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX				UNIT
			SN54ALS644A		SN74ALS644A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	10	35	10	30	ns
t_{PHL}			5	25	5	22	
t_{PLH}	B	A	10	35	10	30	ns
t_{PHL}			5	23	5	21	
t_{PLH}	$\overline{G}$	A	8	35	8	30	ns
t_{PHL}			10	38	10	35	
t_{PLH}	$\overline{G}$	B	8	31	8	26	ns
t_{PHL}			15	40	15	35	
t_{PLH}	DIR	A	8	31	8	26	ns
t_{PHL}			10	40	10	35	
t_{PLH}	DIR	B	10	35	10	30	ns
t_{PHL}			15	40	15	35	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range:
SN54AS640, SN54AS643, SN54AS645 . . . . . −55°C to 125°C
SN74AS640, SN74AS643, SN74AS645 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS640 SN54AS643 SN54AS645			SN74AS640 SN74AS643 SN74AS645			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS'			SN74AS'			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.30	0.55				V
		V_{CC} = 4.5 V,	I_{OL} = 64 mA					0.35	0.55	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports‡					70			70	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	A or B ports‡					−0.75			−0.75	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−50		−150	−50		−150	mA
I_{CC}	'AS640	V_{CC} = 5.5 V	Outputs high		37	58		37	58	mA
			Outputs low		78	123		78	123	
			Outputs disabled		51	80		51	80	
	'AS643		Outputs high		48	79		48	79	
			Outputs low		88	143		88	143	
			Outputs disabled		61	100		61	100	
	'AS645		Outputs high		62	97		62	97	
			Outputs low		95	149		95	149	
			Outputs disabled		79	123		79	123	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'AS640 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS640		SN74AS640		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	2	8	2	7	ns
t_{PHL}			2	7	2	6	
t_{PZH}	$\overline{G}$	A or B	2	10	2	8	ns
t_{PZL}			2	12	2	10	
t_{PHZ}	$\overline{G}$	A or B	2	9	2	8	ns
t_{PLZ}			2	16	2	13	

'AS643 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS643		SN74AS643		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2	10	2	8	ns
t_{PHL}			2	7.5	2	7	
t_{PLH}	B	A	2	11.5	2	10	ns
t_{PHL}			2	10	2	9	
t_{PZH}	$\overline{G}$	A	2	13	2	11	ns
t_{PZL}			2	13	2	11	
t_{PHZ}	$\overline{G}$	A	2	8.5	2	7.5	ns
t_{PLZ}			2	12	2	10.5	
t_{PZH}	$\overline{G}$	B	2	11.5	2	10	ns
t_{PZL}			2	12	2	10	
t_{PHZ}	$\overline{G}$	B	2	8	2	7	ns
t_{PLZ}			2	12	2	10	

'AS645 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS645		SN74AS645		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	2	11	2	9.5	ns
t_{PHL}			2	10.5	2	9	
t_{PZH}	$\overline{G}$	A or B	2	12	2	11	ns
t_{PZL}			2	12	2	10	
t_{PHZ}	$\overline{G}$	A or B	2	8	2	7	ns
t_{PLZ}			2	13	2	12	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs and I/O ports . . . . . 7 V
Operating free-air temperature range:
SN54AS641, SN54AS642, SN54AS644 . . . . . −55°C to 125°C
SN74AS641, SN74AS642, SN74AS644 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS641 SN54AS642 SN54AS644			SN74AS641 SN74AS642 SN74AS644			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output current			5.5			5.5	V
I_{OL}	Low-level output current			48			64	V
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS641 SN54AS642 SN54AS644			SN74AS641 SN74AS642 SN74AS644			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
I_{OH}		V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.3	0.55				V
		V_{CC} = 4.5 V,	I_{OL} = 64 mA					0.35	0.55	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports‡					70			70	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	A or B ports‡					−0.75			−0.75	
I_{CC}	'AS641		Outputs high		50	82		50	82	mA
			Outputs low		84	136		84	136	
	'AS642	V_{CC} = 5.5 V	Outputs high		25	42		25	42	
			Outputs low		64	104		64	104	
	'AS644		Outputs high		38	62		38	62	
			Outputs low		76	124		76	124	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

'AS641 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS641		SN74AS641		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	5	23	5	21	ns
t_{PHL}			1	8.5	1	7.5	
t_{PLH}	$\overline{G}$	A or B	5	24	5	21	ns
t_{PHL}			1	10	1	9	
t_{PLH}	DIR	A or B	5	26	5	22	ns
t_{PHL}			1	11	1	10	

'AS642 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS642		SN74AS642		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	5	28.5	5	24	ns
t_{PHL}			1	8.5	1	7.5	
t_{PLH}	$\overline{G}$	A or B	5	25	5	22	ns
t_{PHL}			1	11	1	10	
t_{PLH}	DIR	A or B	5	26.5	5	23.5	ns
t_{PHL}			1	12.5	1	11.5	

'AS644 switching characteristics (see Note 1)

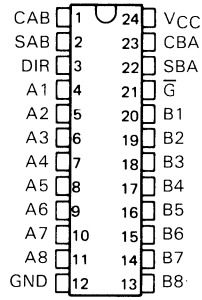
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS644		SN74AS644		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	5	28.5	5	24	ns
t_{PHL}			1	8.5	1	7.5	
t_{PLH}	B	A	5	23	5	21	ns
t_{PHL}			1	8.5	1	7.5	
t_{PLH}	$\overline{G}$	A or B	5	24	5	21	ns
t_{PHL}			1	10	1	9	
t_{PLH}	DIR	A or B	5	26	5	22	ns
t_{PHL}			1	11	1	10	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

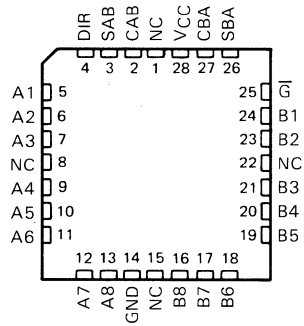
- Independent Registers for A and B Buses
- Multiplexed Real-Time and Stored Data
- Choice of True or Inverting Data Paths
- Choice of 3-State or Open-Collector Outputs
- Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

DEVICE	OUTPUT	LOGIC
'ALS646, 'AS646	3-State	True
'ALS647	Open-Collector	True
'ALS648, 'AS648	3-State	Inverting
'ALS649	Open-Collector	Inverting

SN54ALS', SN54AS' . . . JT PACKAGE
SN74ALS', SN74AS' . . . DW OR NT PACKAGE
(TOP VIEW)



SN54ALS', SN54AS' . . . FK PACKAGE
SN74ALS', SN74AS' . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

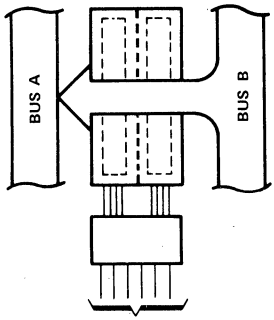
These devices consist of bus transceiver circuits, with 3-state or open-collector outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Data on the A or B bus will be clocked into the registers on the low-to-high transition of the appropriate clock pin (CAB or CBA). The following examples demonstrate the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

Enable ($\overline{G}$) and direction (DIR) pins are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select controls (SAB and SBA) can multiplex stored and real-time (transparent mode) data. The circuitry used for select control will eliminate the typical decoding glitch which occurs in a multiplexer during the transition between stored and real-time data. The direction control determines which bus will receive data when enable $\overline{G}$ is active (low). In the isolation mode (control $\overline{G}$ high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

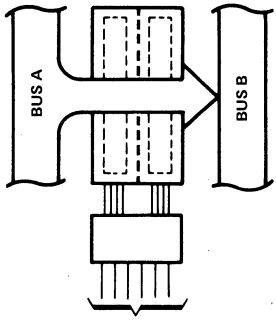
The -1 versions of the SN74ALS' parts are identical to the standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes. There are no -1 versions of the SN54ALS' parts.

The SN54' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.



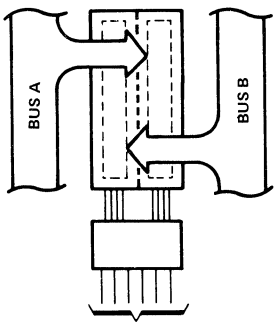
(21) G	(3) DIR	(1) CAB	(23) CBA	(2) SAB	(22) SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



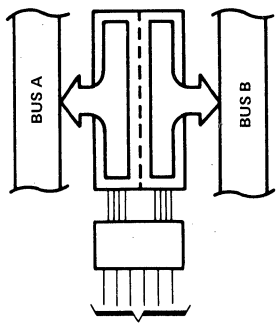
(21) G	(3) DIR	(1) CAB	(23) CBA	(2) SAB	(22) SBA
L	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



(21) G	(3) DIR	(1) CAB	(23) CBA	(2) SAB	(22) SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B



(21) G	(3) DIR	(1) CAB	(23) CBA	(2) SAB	(22) SBA
L	L	X	HorL	X	H
L	H	HorL	X	H	X

TRANSFER
STORED DATA
TO A OR B

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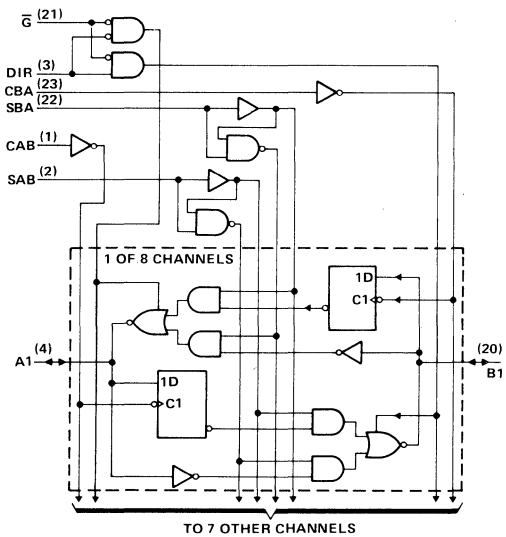
FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION	
G	DIR	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	'ALS646, 'ALS647 'AS646	'ALS648, 'ALS649 'AS648
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B Data	Store A and B Data
H	X	H or L	H or L	X	X			Isolation, hold storage	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus	Real-Time $\overline{B}$ Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus	Stored $\overline{B}$ Data to A Bus
L	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus	Real-Time $\overline{A}$ Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus	Store $\overline{A}$ Data to B Bus

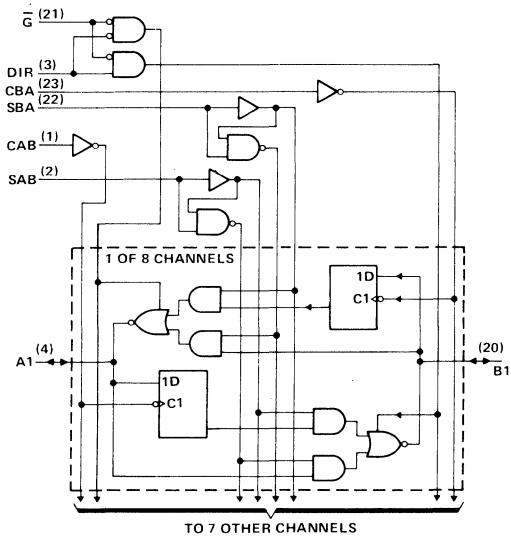
†The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

functional block diagrams (positive logic)

'ALS646, 'AS646, 'ALS647



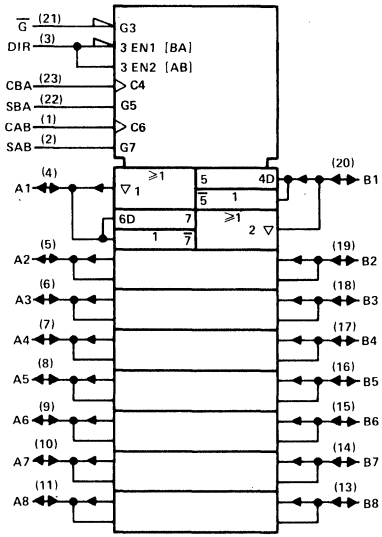
'ALS648, 'AS648, 'ALS649



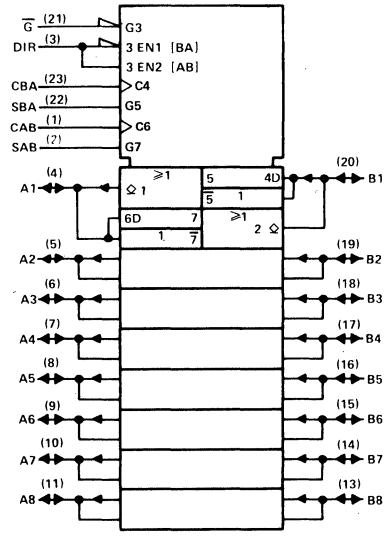
Pin numbers shown are for DW, JT, and NT packages.

logic symbols†

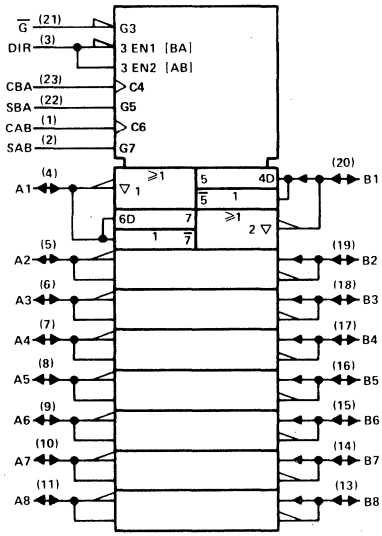
'ALS646, 'AS646



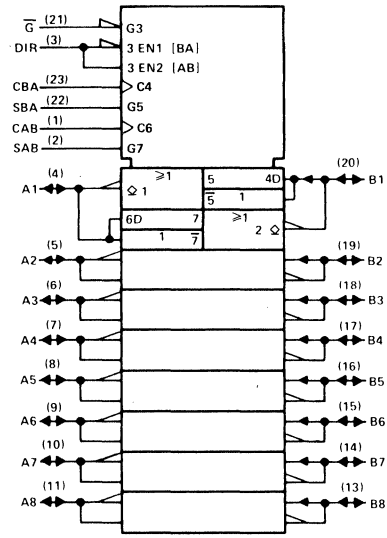
'ALS647



'ALS648, 'AS648



'ALS649



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: Control inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS646 . . . . . −55°C to 125°C
SN74ALS646 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS646			SN74ALS646			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
							48†	
f_{clock}	Clock frequency	0		35	0		40	MHz
t_w	Pulse duration, clocks high or low	14.5			12.5			ns
t_{su}	Setup time, A before CAB↑ or B before CBA↑	15			10			ns
t_h	Hold time, A after CAB↑ or B after CBA↑	0			0			ns
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended condition applies if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48-mA limit applies for the SN74ALS646-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS646			SN74ALS646			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, (I_{OL} = 48 mA for −1 version)	I_{OL} = 24 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports§					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
	A or B ports§					−0.2			−0.2	
I_O¶		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	Outputs high		47	76		47	76	mA
			Outputs low		55	88		55	88	
			Outputs disabled		55	88		55	88	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C
§For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
¶The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS646 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS646			SN54ALS646		SN74ALS646		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}				50		35		40		MHz
t_{PLH}	CBA or CAB	A or B		20	25	10	35	10	30	ns
t_{PHL}				11	15	5	20	5	17	
t_{PLH}	A or B	B or A		11	17	5	22	5	20	ns
t_{PHL}				7.5	10	3	15	3	12	
t_{PLH}	SBA or SAB† (with A or B low)	A or B		24	32	15	40	15	35	ns
t_{PHL}				13	17	5	23	5	20	
t_{PLH}	SBA or SAB† (with A or B high)	A or B		17	22	8	30	8	25	ns
t_{PHL}				13	17	5	24	5	20	
t_{PZH}	$\overline{G}$	A or B		10	15	3	20	3	17	ns
t_{PZL}				10	15	5	22	5	20	
t_{PHZ}	$\overline{G}$	A or B		6	8	1	12	1	10	ns
t_{PLZ}				10	13	2	20	2	16	
t_{PZH}	DIR	A or B		22	28	10	38	10	30	ns
t_{PZL}				14.5	20	5	30	5	25	
t_{PHZ}	DIR	A or B		6	8	1	12	1	10	ns
t_{PLZ}				10	13	2	21	2	16	

† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS647 . . . . . −55°C to 125°C
SN74ALS647 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS647			SN74ALS647			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			12			24	mA
							48†	
f_{clock}	Clock frequency	0		25	0		30	MHz
t_w	Pulse duration, clocks high or low	20			16.5			ns
t_{su}	Setup time, A before CAB↑ or B before CBA↑	15			10			ns
t_h	Hold time, A after CAB↑ or B after CBA↑	0			0			ns
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended condition applies if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48-mA limit applies for the SN74ALS647-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS647			SN74ALS647			UNIT
				MIN	TYP‡	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
I_{OH}		V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4				V
		V_{CC} = 4.5 V, (I_{OL} = 48 mA for −1 versions)	I_{OL} = 24 mA					0.35	0.5	
I_I	A or B ports	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	
I_{IH}	A or ports§	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	Control inputs					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
	A or B ports§					−0.2			−0.2	
I_{CC}		V_{CC} = 5.5 V	Outputs high		35	60		35	60	mA
			Outputs low		40	65		40	65	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C
§For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

'ALS647 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 680 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX				UNIT
			'ALS647			SN54ALS647		SN74ALS647		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}				40		25		30		MHz
t_{PLH}	CBA or CAB	A or B		38	50	19	72	19	58	ns
t_{PHL}				12	20	6	24	6	22	
t_{PLH}	A or B	B or A		35	39	17	70	17	54	ns
t_{PHL}				10	13	4	19	4	16	
t_{PLH}	SBA or SAB† (with A or B low)	A or B		40	51	20	72	20	60	ns
t_{PHL}				12	17	6	26	6	22	
t_{PLH}	SBA or SAB† (with A or B high)	A or B		40	51	20	72	20	60	ns
t_{PHL}				12	17	6	26	6	22	
t_{PLH}	$\overline{G}$	A or B		20	27	10	37	10	31	ns
t_{PHL}				10	15	2	20	2	17	
t_{PLH}	DIR	A or B		20	25	9	34	9	29	ns
t_{PHL}				13	17	2	22	2	19	

†These parameters are measured with the internal output state of the storage register opposite to that of the bus input.
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: Control inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS648 . . . . . −55°C to 125°C
SN74ALS648 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS648			SN74ALS648			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
							48†	
f_{clock}	Clock frequency	0		35	0		40	MHz
t_w	Pulse duration, clocks high or low	14.5			12.5			ns
t_{su}	Setup time, A before CAB↑ or B before CBA↑	15			10			ns
t_h	Hold time, A after CAB↑ or B after CBA↑	0			0			ns
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended conditon applies if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48-mA limit applies for the SN74ALS648-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS648			SN74ALS648			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, (I_{OL} = 48 mA for −1 version)	I_{OL} = 24 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports§					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
	A or B ports§					−0.2			−0.2	
I_O¶		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	Outputs high		47	76		47	76	mA
			Outputs low		57	88		57	88	
			Outputs disabled		57	88		57	88	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C
§For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
¶The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS648 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS648			SN54ALS648		SN74ALS648		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}				50		35		40		MHz
t_{PLH}	CBA or CAB	A or B		21	29	8	39	8	33	ns
t_{PHL}				13	18	5	23	5	20	
t_{PLH}	A or B	B or A		10	15	3	20	3	17	ns
t_{PHL}				6	8	2	12	2	10	
t_{PLH}	SBA or SAB† (with A or B low)	A or B		24	32	5	44	5	39	ns
t_{PHL}				15	21	4	26	4	22	
t_{PLH}	SBA or SAB† (with A or B high)	A or B		16	22	6	30	6	25	ns
t_{PHL}				14	19	6	25	6	21	
t_{PZH}	$\overline{G}$	A or B		12	18	4	25	4	22	ns
t_{PZL}				12	18	4	25	4	22	
t_{PHZ}	$\overline{G}$	A or B		5	8	1	12	1	10	ns
t_{PLZ}				7	12	2	21	2	15	
t_{PZH}	DIR	A or B		14	22	4	35	4	27	ns
t_{PZL}				10	17	3	25	3	19	
t_{PHZ}	DIR	A or B		7	12	1	17	1	14	ns
t_{PLZ}				7	13	2	22	2	15	

† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS649 . . . . . −55°C to 125°C
SN74ALS649 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS649			SN74ALS649			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			12			24	mA
							48†	
f_{clock}	Clock frequency	0		25	0		30	MHz
t_w	Pulse duration, clocks high or low	20			16.5			ns
t_{su}	Setup time, A before CAB↑ or B before CBA↑	15			10			ns
t_h	Hold time, A after CAB↑ or B after CBA↑	0			0			ns
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended condition applies if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48-mA limit applies for the SN74ALS649-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS649			SN74ALS649			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
I_{OH}		V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4				V
		V_{CC} = 4.5 V, (I_{OL} = 48 mA for −1 versions)	I_{OL} = 24 mA					0.35	0.5	
I_I	A or B ports	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	
I_{IH}	A or ports§	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	Control inputs					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
	A or B ports§					−0.2			−0.2	
I_{CC}		V_{CC} = 5.5 V	Outputs high		40	60		40	60	mA
			Outputs low		45	70		45	70	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C
§For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

'ALS649 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 680 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX				UNIT
			'ALS649			SN54ALS649		SN74ALS649		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}				40		25		30		MHz
t_{PLH}	CBA or CAB	A or B		40	52	19	77	19	62	ns
t_{PHL}				12	18	6	22	6	20	
t_{PLH}	A or B	B or A		30	41	13	65	13	50	ns
t_{PHL}				6	9	2	11	2	10	
t_{PLH}	SBA or SAB† (with A or B low)	A or B		35	46	20	72	20	55	ns
t_{PHL}				15	21	6	26	6	22	
t_{PLH}	SBA or SAB† (with A or B high)	A or B		35	46	20	72	20	55	ns
t_{PHL}				15	21	6	26	6	22	
t_{PLH}	$\overline{G}$	A or B		16	22	8	28	8	25	ns
t_{PHL}				13	18	2	23	2	20	
t_{PLH}	DIR	A or B		16	22	8	28	8	25	ns
t_{PHL}				13	17	2	23	2	20	

† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: Control inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54AS646, SN54AS648 . . . . . −55°C to 125°C
SN74AS646, SN74AS648 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54AS646 SN54AS648			SN74AS646 SN74AS648			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−12			−15	mA
I_{OL}	Low-level output current				32			48	mA
f_{clock}	Clock frequency		0		75	0		90	MHz
t_w	Pulse duration	Clock high	6			5			ns
		Clock high	7			6			
t_{su}	Setup time, A before CAB↑ or B before CBA↑		7			6			ns
t_h	Hold time, A after CAB↑ or B after CBA↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS646, SN54AS648			SN74AS646 SN74AS648			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC} − 2			V_{CC} − 2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.50				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.50	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports‡					70			70	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	A or B ports§					−0.75			−0.75	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'AS646	V_{CC} = 5.5 V	Outputs high		120	195		120	195	mA
			Outputs low		130	211		130	211	
			Outputs disabled		130	211		130	211	
	'AS648		Outputs high		110	185		110	185	
			Outputs low		120	195		120	195	
			Outputs disabled		120	195		120	195	

†All typical values are at V_{CC} = 5 V, T_A = 25°C
‡For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'AS646 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS646		SN74AS646		
			MIN	MAX	MIN	MAX	
f_{max}			75		90		MHz
t_{PLH}	CBA or CAB	A or B	2	9.5	2	8.5	ns
t_{PHL}			2	10	2	9	
t_{PLH}	A or B	B or A	2	11	2	9	ns
t_{PHL}			1	8	1	7	
t_{PLH}	SBA or SAB†	A or B	2	12	2	11	ns
t_{PHL}			2	10	2	9	
t_{PZH}	$\overline{G}$	A or B	2	10	2	9	ns
t_{PZL}			3	15	3	14	
t_{PHZ}	$\overline{G}$	A or B	2	11	2	9	ns
t_{PLZ}			2	11	2	9	
t_{PZH}	DIR	A or B	3	19	3	16	ns
t_{PZL}			3	21	3	18	
t_{PHZ}	DIR	A or B	2	12	2	10	ns
t_{PLZ}			2	12	2	10	

'AS648 switching characteristics (see Note 1)

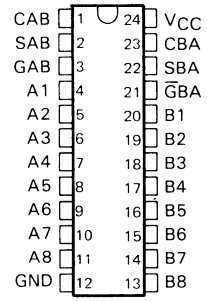
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS648		SN74AS648		
			MIN	MAX	MIN	MAX	
f_{max}			75		90		MHz
t_{PLH}	CBA or CAB	A or B	2	9.5	2	8.5	ns
t_{PHL}			2	10	2	9	
t_{PLH}	A or B	B or A	2	9	2	8	ns
t_{PHL}			1	8	1	7	
t_{PLH}	SBA or SAB†	A or B	2	12	2	11	ns
t_{PHL}			2	10	2	9	
t_{PZH}	$\overline{G}$	A or B	2	10	2	9	ns
t_{PZL}			3	18	3	15	
t_{PHZ}	$\overline{G}$	A or B	2	11	2	9	ns
t_{PLZ}			2	11	2	9	
t_{PZH}	DIR	A or B	3	19	3	16	ns
t_{PZL}			3	21	3	18	
t_{PHZ}	DIR	A or B	2	12	2	10	ns
t_{PLZ}			2	12	2	10	

† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

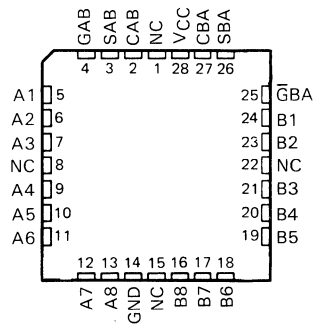
- **Bus Transceivers/Registers**
- **Independent Registers and Enables for A and B Buses**
- **Multiplexed Real-Time and Stored Data**
- **Choice of True and Inverting Data Paths**
- **Choice of 3-State or Open-Collector Outputs to A Bus**
- **Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

DEVICE	A OUTPUT	B OUTPUT	LOGIC
'ALS651, 'AS651	3-State	3-State	Inverting
'ALS652, 'AS652	3-State	3-State	True
'ALS653	Open-Collector	3-State	Inverting
'ALS654	Open-Collector	3-State	True

SN54ALS', SN54AS' . . . JT PACKAGE
SN74ALS', SN74AS' . . . DW OR NT PACKAGE
(TOP VIEW)



SN54ALS', SN54AS' . . . FK PACKAGE
SN74ALS', SN74AS' . . . FN PACKAGE
(TOP VIEW)



NC No internal connection

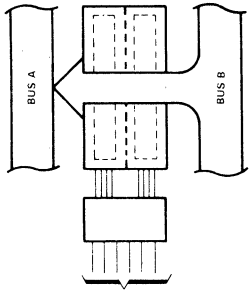
description

These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Enable GAB and $\overline{G}$BA are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether real-time or stored data is transferred. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input level selects real-time data, and a high selects stored data. The following examples demonstrate the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and $\overline{G}$BA. In this configuration each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

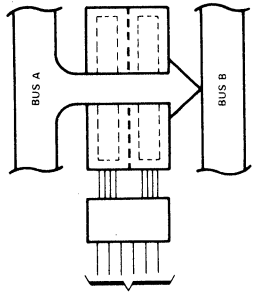
The -1 versions of the SN74ALS651 through SN74ALS654 are identical to the standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes. There are no -1 versions of the SN54ALS651 through SN54ALS654.

The SN54' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.



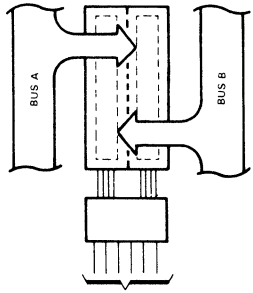
GAB	$\overline{G}$BA	CAB	CBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



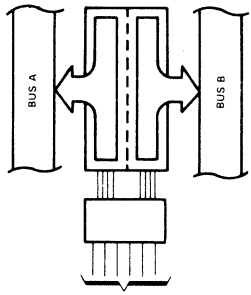
GAB	$\overline{G}$BA	CAB	CBA	SAB	SBA
H	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



GAB	$\overline{G}$BA	CAB	CBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

STORAGE FROM
A AND/OR B



GAB	$\overline{G}$BA	CAB	CBA	SAB	SBA
H	L	H or L	H or L	H	H

TRANSFER
STORED DATA
TO A AND/OR B

TEXAS INSTRUMENTS
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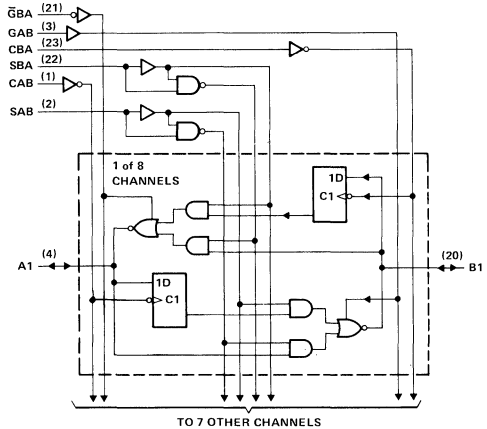
FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION	
GAB	$\overline{GBA}$	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	'ALS651, 'ALS653 'AS651	'ALS652, 'ALS654 'AS652
L	H	H or L	H or L	X	X	Input	Input	Isolation	Isolation
L	H	↑	↑	X	X			Store A and B Data	Store A and B Data
X	H	↑	H or L	X	X	Input	Unspecified†	Store A, Hold B	Store A, Hold B
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers	Store A in both registers
L	X	H or L	↑	X	X	Unspecified†	Input	Hold A, Store B	Hold A, Store B
L	L	↑	↑	X	X‡	Output	Input	Store B in both registers	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-Time $\overline{B}$ Data to A Bus	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Stored $\overline{B}$ Data to A Bus	Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time $\overline{A}$ Data to B Bus	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored $\overline{A}$ Data to B Bus	Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{A}$ Data to B Bus and Stored $\overline{B}$ Data to A Bus	Stored A Data to B Bus and Stored B Data to A Bus

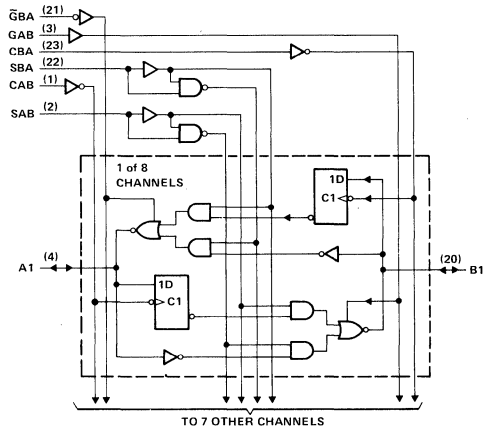
†The data output functions may be enabled or disabled by various signals at the GAB or $\overline{GBA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.
‡Select control = L: clocks can occur simultaneously.
Select control = H: clocks must be staggered in order to load both registers.

logic diagram (positive logic)

'ALS651, 'AS651, 'ALS653



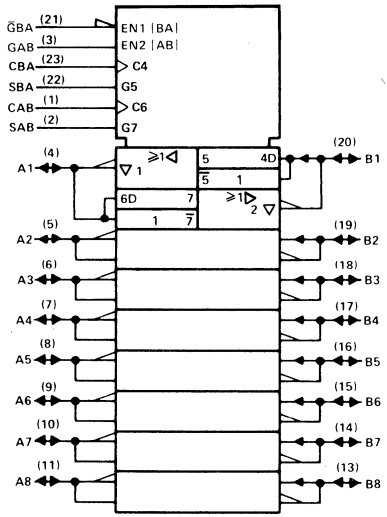
'ALS652, 'AS652, 'ALS654



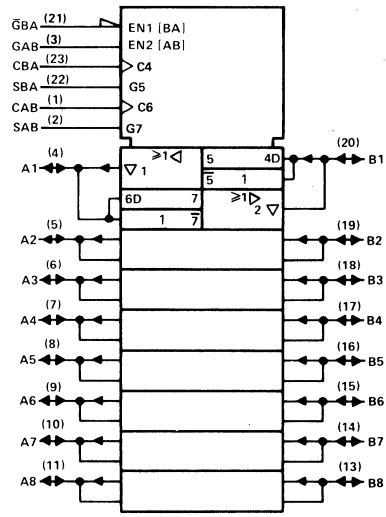
Pin numbers shown are for DW, JT, and NT packages.

logic symbols†

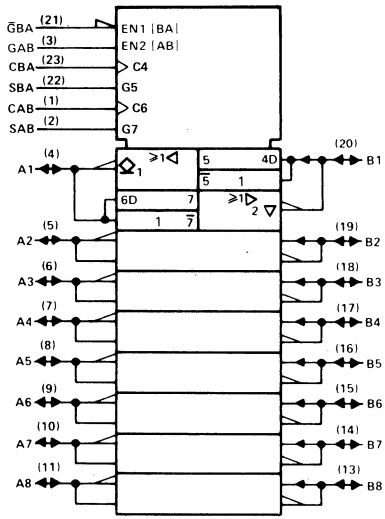
'ALS651, 'AS651



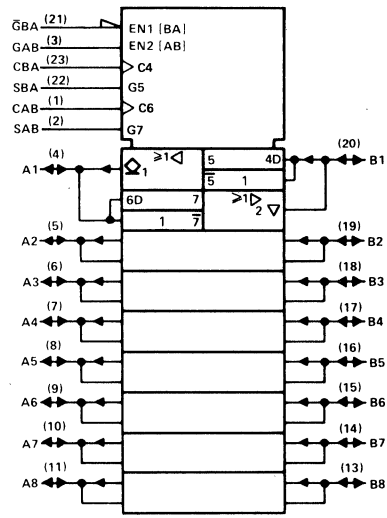
'ALS652, 'AS652



'ALS653



'ALS654



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: Control inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS651, SN54ALS652 . . . . . −55°C to 125°C
SN74ALS651, SN74ALS652 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS651 SN54ALS652			SN74ALS651 SN74ALS652			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−12			−15	mA
I_{OL}	Low-level output current				12			24	mA
								48†	
f_{clock}	Clock frequency		0		35	0		40	MHz
t_w	Pulse duration	CBA or CAB high	14.5			12.5			ns
		CBA or CAB low	14.5			12.5			
t_{su}	Setup time before CAB↑ or CBA↑	A or B	15			10			ns
t_h	Hold time after CAB↑ or CBA↑	A or B	5			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

†The 48-mA limit applies for the SN74ALS651-1 and SN74ALS652-1 and if V_{CC} is maintained between 4.75 V and 5.25 V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS651 SN54ALS652			SN74ALS651 SN74ALS652			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
		V_{CC} = 4.75 V,	I_{OL} = 48 mA (−1 versions)							
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports‡					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
	A or B ports‡					−0.2			−0.2	
I_O§	B ports	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS651	V_{CC} = 5.5 V	Outputs high		42	68		42	68	mA
			Outputs low		52	82		52	82	
			Outputs disabled		52	82		52	82	
	'ALS652		Outputs high		47	76		47	76	
			Outputs low		55	88		55	88	
			Outputs disabled		55	88		55	88	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS651 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS651			SN54ALS651		SN74ALS651		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}				50		35		40		MHz
t_{PLH}	CBA or CAB	A or B		20	27	10	38	10	32	ns
t_{PHL}				11	15	5	21	5	17	
t_{PLH}	A or B	B or A		9	13	4	20	4	18	ns
t_{PHL}				5	8	2	12	2	10	
t_{PLH}	SBA or SAB† (with A or B low)	A or B		24	31	13	45	13	38	ns
t_{PHL}				13	18	7	25	7	21	
t_{PLH}	SBA or SAB† (with A or B high)	A or B		15	20	8	30	8	25	ns
t_{PHL}				13	18	7	25	7	21	
t_{PZH}	$\overline{G}$BA	A		12	16	5	22	5	20	ns
t_{PZL}				11	15	5	21	5	18	
t_{PHZ}	$\overline{G}$BA	A		4	7	2	10	2	9	ns
t_{PLZ}				7	10	3	16	3	12	
t_{PZH}	GAB	B		14	19	7	25	7	22	ns
t_{PZL}				13	18	7	25	7	21	
t_{PHZ}	GAB	B		5	10	2	14	2	12	ns
t_{PLZ}				7	10	2	20	2	14	

'ALS652 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS652			SN54ALS652		SN74ALS652		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}				50		35		40		MHz
t_{PLH}	CBA or CAB	A or B		20	25	10	35	10	30	ns
t_{PHL}				11	15	5	20	5	17	
t_{PLH}	A or B	B or A		11	15	5	20	5	18	ns
t_{PHL}				8	10	3	15	3	12	
t_{PLH}	SBA or SAB† (with A or B low)	A or B		24	32	15	40	15	35	ns
t_{PHL}				13	17	6	23	6	20	
t_{PLH}	SBA or SAB† (with A or B high)	A or B		17	22	8	30	8	25	ns
t_{PHL}				13	17	5	24	5	20	
t_{PZH}	$\overline{G}$BA	A		10	15	3	20	3	17	ns
t_{PZL}				10	14	5	22	5	18	
t_{PHZ}	$\overline{G}$BA	A		6	8	1	12	1	10	ns
t_{PLZ}				10	13	2	20	2	16	
t_{PZH}	GAB	B		15	20	8	25	8	22	ns
t_{PZL}				12	16	6	21	6	18	
t_{PHZ}	GAB	B		6	8	1	12	1	10	ns
t_{PLZ}				10	13	2	21	2	16	

† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs and A I/O ports . . . . . 7 V
B I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS653, SN54ALS654 . . . . . −55°C to 125°C
SN74ALS653, SN74ALS654 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS653 SN54ALS654			SN74ALS653 SN74ALS654			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
V_{OH}	High-level output voltage	A ports			5.5			5.5	V
I_{OH}	High-level output current	B ports			−12			−15	mA
I_{OL}	Low-level output current				12			24	mA
								48†	
f_{clock}	Clock frequency		0		25	0		35	MHz
t_w	Pulse duration	CBA or CAB high	20			14.5			ns
		CBA or CAB low	20			14.5			
t_{su}	Setup time before CAB↑ or CBA↑	A or B	15			10			ns
t_h	Hold time after CAB↑ or CBA↑	A or B	5			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

†The 48-mA limit applies only for the SN74ALS653-1 and SN74ALS654-1 and if V_{CC} is maintained between 4.75 V and 5.25 V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS653 SN54ALS654			SN74ALS653 SN74ALS654			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	B ports	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
I_{OH}	A ports	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
		V_{CC} = 4.75 V, I_{OL} = 48 mA (−1 versions)								
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports‡					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
	A or B ports‡					−0.2			−0.2	
I_O§	B ports	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS653	V_{CC} = 5.5 V	Outputs high		47	76		47	76	mA
			Outputs low		55	88		55	88	
			Outputs disabled		55	88		55	88	
	'ALS654		Outputs high		47	76		47	76	
			Outputs low		55	88		55	88	
			Outputs disabled		55	88		55	88	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 680 Ω (A outputs), R1 = R2 = 500 Ω (B outputs), T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω (A outputs), R2 = R2 = 500 Ω (B outputs), T_A = MIN to MAX				UNIT
			'ALS653 'ALS654			SN54ALS653 SN54ALS654		SN74ALS653 SN74ALS654		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}				40		25		35		MHz
t_{PLH}	CBA	A		30	50	16	71	16	64	ns
t_{PHL}				11	15	6	24	6	22	
t_{PLH}	CAB	B		20	25	10	35	10	30	ns
t_{PHL}				11	15	5	20	5	17	
t_{PLH}	A	B		11	15	5	20	5	18	ns
t_{PHL}				10	13	2	18	2	15	
t_{PLH}	B	A		20	44	12	63	12	56	ns
t_{PHL}				10	13	2	18	2	15	
t_{PLH}	SBA† (with B low)	A		35	50	19	68	19	62	ns
t_{PHL}				15	22	5	27	5	25	
t_{PLH}	SBA† (with B high)	A		35	50	19	68	19	62	ns
t_{PHL}				15	22	5	27	5	25	
t_{PLH}	SAB† (with A low)	B		24	32	12	40	15	35	ns
t_{PHL}				13	18	6	25	6	22	
t_{PLH}	SAB† (with A high)	B		18	22	8	30	8	25	ns
t_{PHL}				13	19	6	25	6	22	
t_{PLH}	$\overline{G}$BA	A		17	23	6	35	6	30	ns
t_{PHL}				14	20	6	27	6	24	
t_{PZH}	GAB	B		15	20	8	25	8	22	ns
t_{PZL}				13	17	6	25	6	22	
t_{PHZ}	GAB	B		8	12	1	16	1	14	ns
t_{PLZ}				10	13	2	21	2	16	

† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: Control inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54AS651, SN54AS652 . . . . . −55°C C to 125°C
SN74AS651, SN74AS652 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54AS651 SN54AS652			SN74AS651 SN74AS652			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−12			−15	mA
I_{OL}	Low-level output current				32			48	mA
f_{clock}	Clock frequency		0		75	0		90	MHz
t_w	Pulse duration	CBA or CAB high	6			5			ns
		CBA or CAB low	7			6			
t_{su}	Setup time before CAB↑ or CBA↑	A or B	7			6			ns
t_h	Hold time after CAB↑ or CBA↑	A or B	0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS651 SN54AS652			SN74AS651 SN74AS652			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.50				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.50	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports‡					70			70	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	A or B ports‡					−0.75			−0.75	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'AS651	V_{CC} = 5.5 V	Outputs high		110	185		110	185	mA
			Outputs low		120	195		120	195	
			Outputs disabled		130	195		130	195	
	'AS652		Outputs high		120	195		120	195	
			Outputs low		130	211		130	211	
			Outputs disabled		130	211		130	211	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'AS651 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS651		SN74AS651		
			MIN	MAX	MIN	MAX	
f_{max}			75		90		MHz
t_{PLH}	CBA or CAB	A or B	2	9.5	2	8.5	ns
t_{PHL}			2	10	2	9	
t_{PLH}	A or B	B or A	2	9	2	8	ns
t_{PHL}			1	8	1	7	
t_{PLH}	SBA or SAB†	A or B	2	12	2	11	ns
t_{PHL}			2	10	2	9	
t_{PZH}	$\overline{G}$BA	A	2	11	2	10	ns
t_{PZL}			3	18	3	16	
t_{PHZ}	$\overline{G}$BA	A	2	10	2	9	ns
t_{PLZ}			2	10	2	9	
t_{PZH}	GAB	B	3	12	3	11	ns
t_{PZL}			3	20	3	16	
t_{PHZ}	GAB	B	2	11	2	10	ns
t_{PLZ}			2	12	2	11	

'AS652 switching characteristics (see Note 1)

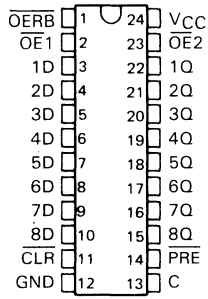
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS652		SN74AS652		
			MIN	MAX	MIN	MAX	
f_{max}			75		90		MHz
t_{PLH}	CBA or CAB	A or B	2	9.5	2	8.5	ns
t_{PHL}			2	10	2	9	
t_{PLH}	A or B	B or A	2	11	2	9	ns
t_{PHL}			1	8	1	7	
t_{PLH}	SBA or SAB†	A or B	2	12	2	11	ns
t_{PHL}			2	10	2	9	
t_{PZH}	$\overline{G}$BA	A	2	11	2	10	ns
t_{PZL}			3	18	3	16	
t_{PHZ}	$\overline{G}$BA	A	2	10	2	9	ns
t_{PLZ}			2	10	2	9	
t_{PZH}	GAB	B	3	12	3	11	ns
t_{PZL}			3	20	3	16	
t_{PHZ}	GAB	B	2	11	2	10	ns
t_{PLZ}			2	12	2	11	

† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

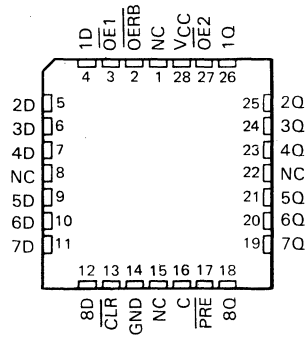
TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

- **3-State I/O-Type Read-Back Inputs**
- **Bus-Structured Pinout**
- **Choice of True or Inverting Logic**
  'ALS666 . . . True Outputs
  'ALS667 . . . Inverting Outputs
- **Preset and Clear Inputs**
- **Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS666 . . . JT PACKAGE
SN74ALS666 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54ALS666 . . . FK PACKAGE
SN74ALS666 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection.

description

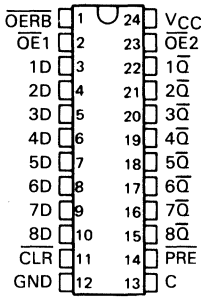
These 8-bit latches are designed specifically for storing the contents of the input data bus plus providing the capability of reading-back the stored data onto the input data bus. In addition, they provide a 3-state buffer type output and are easily utilized in bus-structured applications.

The eight latches of the 'ALS666 and 'ALS667 are transparent D-type. While the enable (C) is high, the Q outputs of the 'ALS666 will follow the data (D) inputs. On the 'ALS667, the $\overline{Q}$ outputs will provide the inverse of what is applied to its data (D) inputs. On both devices, the Q or $\overline{Q}$ output will be in the high-impedance state if either output control, $\overline{OE}1$ or $\overline{OE}2$, is at a high logic level.

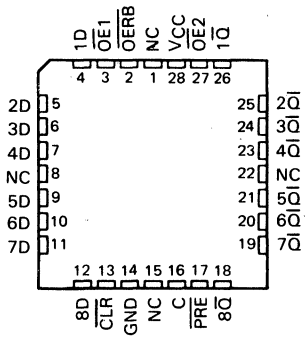
Read-back is provided thru the read-back control input ($\overline{OERB}$). When $\overline{OERB}$ is taken low, the data present at the output of the data latches will be allowed to pass back onto the input data bus. When it is taken high, the output of the data latches will be isolated from the data (D) inputs. The read-back control does not affect the internal operation of the latches; however, caution should be exercised not to create a bus-conflict situation.

The SN54ALS666 and SN54ALS667 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS666 and SN75ALS667 are characterized for operation from 0°C to 70°C.

SN54ALS667 . . . JT PACKAGE
SN74ALS667 . . . DW OR NT PACKAGE
(TOP VIEW)



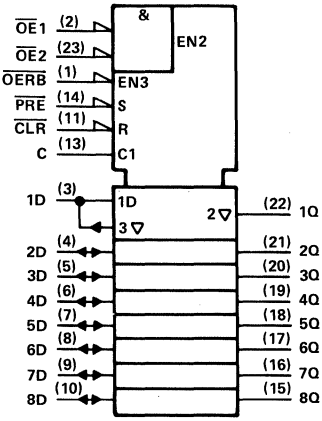
SN54ALS667 . . . FK PACKAGE
SN74ALS667 . . . FN PACKAGE
(TOP VIEW)



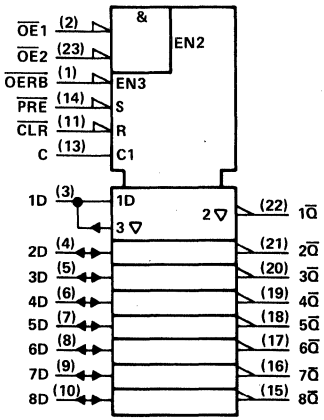
NC—No internal connection.

logic symbols†

'ALS666



'ALS667



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12
Pin numbers shown are for DW, JT, and NT packages.

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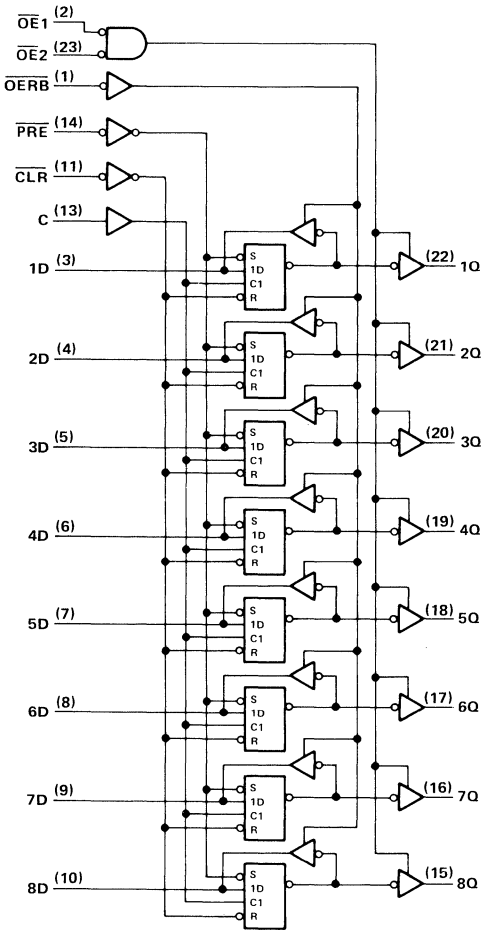
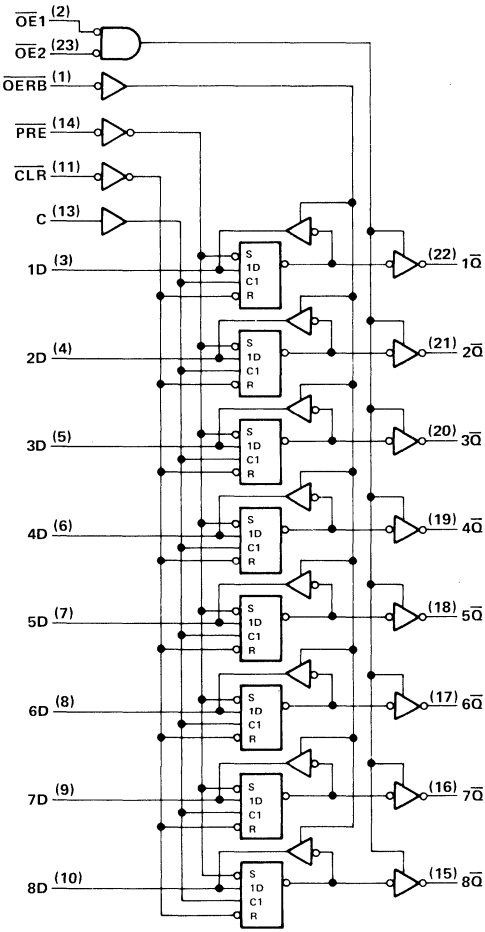
logic diagrams (positive logic)

'ALS666

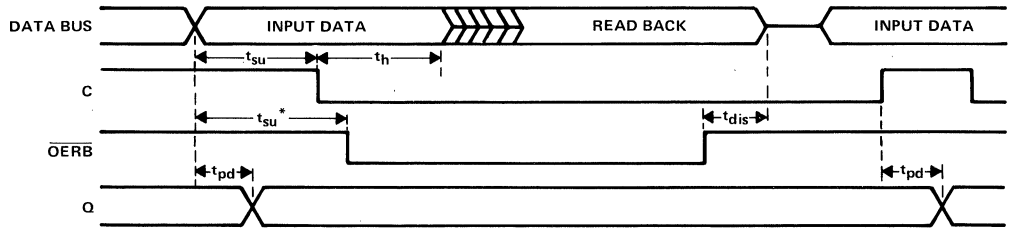


'ALS667



Pin numbers shown are for DW, JT, and NT packages.

timing diagram



$\overline{CLR}$ = H, $\overline{PRE}$ = H, $\overline{OE1}$ = L, $\overline{OE2}$ = L

*This setup time ensures the readback circuit will not create a conflict on the input data bus.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage (all inputs except D input) . . . . . 7 V
Voltage applied to D inputs and to disabled 3-state outputs . . . . . 5.5 V
Operating free-air temperature range: SN54ALS666, SN54ALS667 . . . . . −55°C to 125°C
SN74ALS666, SN74ALS667 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS666 SN54ALS667			SN74ALS666 SN74ALS667			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current	Q			−1			−2.6	mA
		D			−0.4			−0.4	
I_{OL}	Load-level output current	Q			12			24	mA
		D			4			8	
t_w	Pulse duration	Enable C high	15			10			ns
		$\overline{CLR}$ low	10			10			
		$\overline{PRE}$ low	10			10			
t_{su}	Setup time	Data before C↓	15			10			ns
		Data before $\overline{OERB}$↓	15			10			
t_h	Hold time	Data after C↓	10			5			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS666 SN54ALS667			SN74ALS666 SN74ALS667			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	All outputs	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	Q or $\overline{Q}$	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	D	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
	Q or $\overline{Q}$	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	Q or $\overline{Q}$	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	
I_I	D inputs	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	mA
	All others	V_{CC} = 5.5 V,	V = 7 V			0.1			0.1	
I_{IH}	D inputs‡	V_{CC} = 5.5 V,	V = 2,7 V			20			20	μA
	All others					20			20	
I_{IL}	D inputs‡	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	All others					−0.1			−0.1	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS666	V_{CC} = 5.5 V, $\overline{OERB}$ high	Q outputs high		25	50		25	50	mA
			Q outputs low		40	73		40	73	
			Q outputs disabled		30	55		30	55	
	'ALS667		$\overline{Q}$ outputs high		25	50		25	50	
			$\overline{Q}$ outputs low		45	79		45	79	
			$\overline{Q}$ outputs disabled		30	60		30	60	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ The output conditions have been chosen to produce a current that closely approximates one half the true short-circuit output currents, I_{OS}.

'ALS666 switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, T_A = MIN to MAX				UNIT
			'ALS666			SN54ALS666		SN74ALS666		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q		7	10	3	18	3	14	ns
t_{PHL}				11	15	4	22	4	18	
t_{PLH}	C	Q		12	16	6	25	6	21	ns
t_{PHL}				16	21	8	32	8	27	
t_{PHL}	$\overline{CLR}$	Q		17	22	9	32	9	29	ns
t_{PHL}		D		17	24	11	36	11	32	
t_{PLH}	$\overline{PRE}$	Q		13	18	7	28	7	22	ns
t_{PHL}		D		17	22	9	35	9	28	
t_{en}	$\overline{OERB}$	D		11	17	4	25	4	21	ns
t_{dis}				6	11	1	18	1	14	
t_{en}	$\overline{OE}1$, $\overline{OE}2$	Q		11	17	4	25	4	21	ns
t_{dis}				6	11	1	18	1	14	

'ALS667 switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, T_A = MIN to MAX				UNIT
			'ALS667			SN54ALS667		SN74ALS667		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	$\overline{Q}$		13	17	6	24	6	20	ns
t_{PHL}				9	13	4	18	4	15	
t_{PLH}	C	$\overline{Q}$		18	23	9	35	9	28	ns
t_{PHL}				14	19	7	27	7	22	
t_{PLH}	$\overline{CLR}$	$\overline{Q}$		14	19	7	28	7	24	ns
t_{PHL}		D		17	23	8	30	8	26	
t_{PHL}	$\overline{PRE}$	$\overline{Q}$		17	23	8	30	8	25	ns
t_{PLH}		D		18	25	9	35	9	28	
t_{en}	$\overline{OERB}$	D		11	17	4	25	4	21	ns
t_{dis}				6	11	1	20	1	14	
t_{en}	$\overline{OE}1$, $\overline{OE}2$	$\overline{Q}$		11	17	4	25	4	21	ns
t_{dis}				6	11	1	20	1	14	

t_{en} = t_{PZH} or t_{PZL}
t_{dis} = t_{PHZ} or t_{PLZ}

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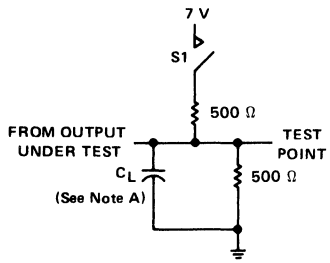
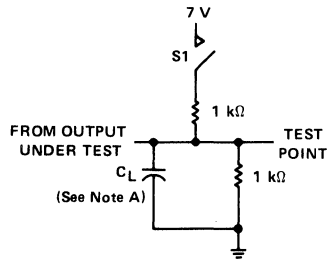
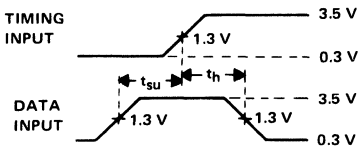
PARAMETER MEASUREMENT INFORMATION



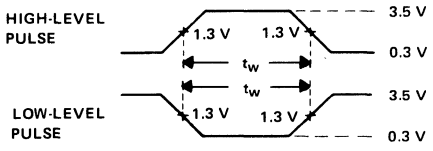
LOAD CIRCUIT FOR
Q OR $\overline{Q}$ OUTPUTS



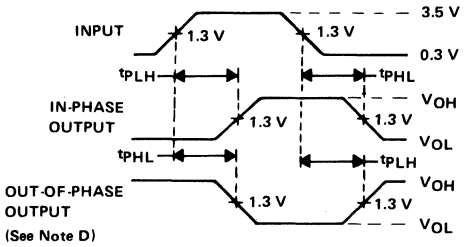
LOAD CIRCUIT FOR D OUTPUTS



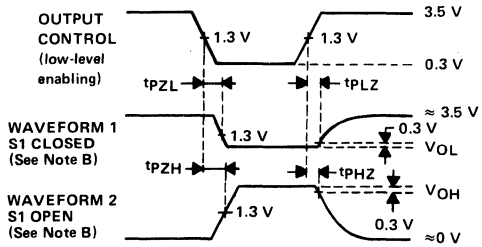
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE WIDTHS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is open.

FIGURE 1

D2661, JUNE 1982—REVISED MAY 1986

- **'ALS677A is a 16-bit Address Comparator with Enable**
- **'ALS678 is a 16-bit Address Comparator with Latch**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

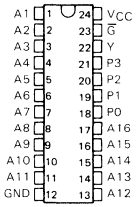
description

The 'ALS677A and 'ALS678 address comparators simplify addressing of memory boards and/or other peripheral devices. The four P inputs are normally hard wired with a preprogrammed address. An internal decoder determines what input information applied to the 16 A inputs must be low or high to cause a low state at the output (Y). For example, a positive-logic bit combination of 0111 (decimal 7) at the P input determines that inputs A1 through A7 must be low and that inputs A8 through A16 must be high to cause the output to go low. Equality of the address applied at the A inputs to the preprogrammed address is indicated by the output being low.

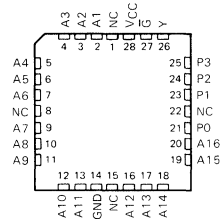
The 'ALS677A features an enable input ($\overline{G}$). When $\overline{G}$ is low, the device is enabled. When $\overline{G}$ is high, the device is disabled and the output is high regardless of the A and P inputs. The 'ALS678 features a transparent latch and a latch enable input (C). When C is high, the device is in the transparent mode. When C is low, the previous logic state of Y is latched.

The SN54ALS677A and SN54ALS678 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN54ALS677A and SN74ALS678 are characterized for operation from 0°C to 70°C.

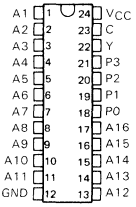
SN54ALS677A . . . JT PACKAGE
SN74ALS677A . . . DW OR NT PACKAGE
(TOP VIEW)



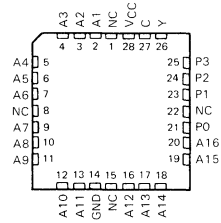
SN54ALS677A . . . FK PACKAGE
SN74ALS677A . . . FN PACKAGE
(TOP VIEW)



SN54ALS678 . . . JT PACKAGE
SN74ALS678 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54ALS678 . . . FK PACKAGE
SN74ALS678 . . . FN PACKAGE
(TOP VIEW)



NC No internal connection

FUNCTION TABLE

'ALS677A	'ALS678	INPUTS COMMON TO 'ALS677A AND 'ALS678																				OUTPUT
$\overline{G}$	C	P3	P2	P1	P0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	Y
L	H	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	H	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	L	H	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	H	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	L
L	H	H	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	L
L	H	H	L	L	H	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	L
L	H	H	L	H	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	L
L	H	H	L	H	H	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	L
L	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	L
L	H	H	H	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	L
L	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	L
L	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L
L	H	All other combinations																				H
H		**'ALS677A: Any combination**																				H
	L	'ALS678: Any combination																				Latched

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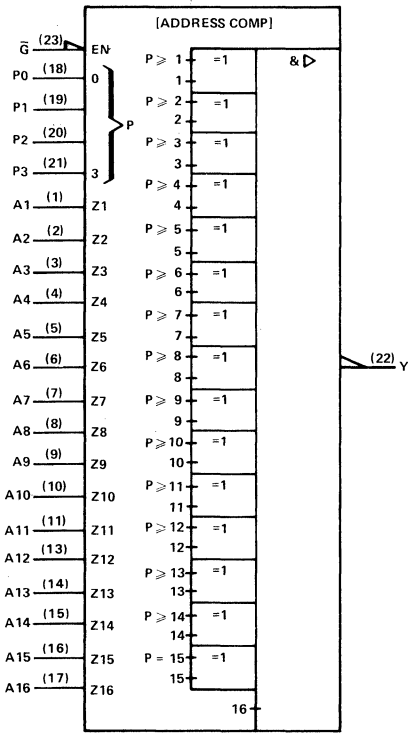
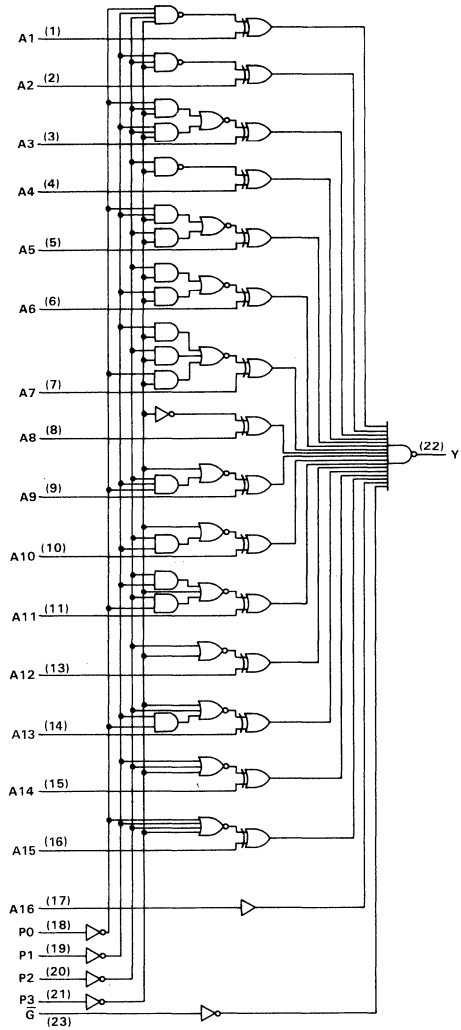
'ALS677A logic symbol†

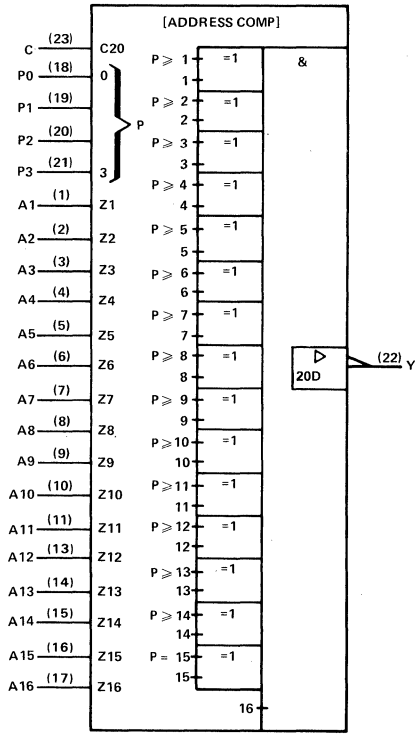


'ALS677A logic diagram (positive logic)

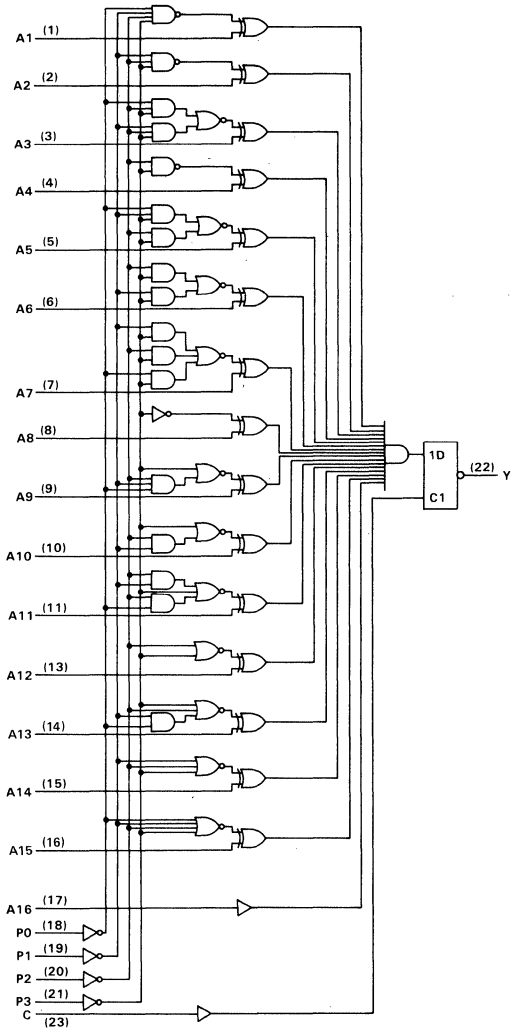


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

'ALS678 logic symbol†



'ALS678 logic diagram (positive logic)



†This symbol is in accordance with ANSI/IEEE STD 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

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POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS677A, SN54ALS678 . . . . . −55°C to 125°C
SN74ALS677A, SN74ALS678 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS677A SN54ALS678			SN74ALS677A SN74ALS678			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−1			−2.6	mA
I_{OL}	Low-level output current				12			24	mA
t_w	Pulse duration, enable C high	'ALS678	45			40			ns
t_{su}	Setup time, data before C↓	'ALS678	50			45			ns
t_h	Hold time, data after C↓	'ALS678	10			5			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS677A SN54ALS678			SN74ALS677A SN74ALS678			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS677A	V_{CC} = 5.5 V			21	33		21	33	mA
	'ALS678				21	35		21	35	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS677A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS677A			SN54ALS677A		SN74ALS677A		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Any P	Y		11	18	4	28	4	25	ns
t_{PHL}				22	32	8	43	8	38	
t_{PLH}	Any A	Y		10	17	5	26	5	22	ns
t_{PHL}				16	25	5	35	5	30	
t_{PLH}	$\overline{G}$	Y		6	10	3	15	3	13	ns
t_{PHL}				16	30	5	40	5	35	

'ALS678 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS678		SN74ALS678		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any P	Y	6	27	6	22	ns
t_{PHL}			10	52	10	43	
t_{PLH}	Any A	Y	5	25	5	21	ns
t_{PHL}			5	40	5	35	
t_{PLH}	C	Y	3	25	3	20	ns
t_{PHL}			15	54	15	48	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TYPICAL APPLICATION INFORMATION

The 'ALS677A and 'ALS678 can be wired to recognize any one of 2^{16} addresses. The number of "lows" in the address determines the input pattern for the P inputs. Then those system address lines that are low in the address to be recognized are connected to the lowest numbered A inputs of the address comparator and the system address lines that are high are connected to the highest numbered A inputs.

For example, assume the comparator is to enable a device when the 16-bit system address is:

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
H	H	L	L	H	H	L	L	H	H	L	L	H	H	H	H

Since the address contains 6 lows and 10 highs, the following connections are made:

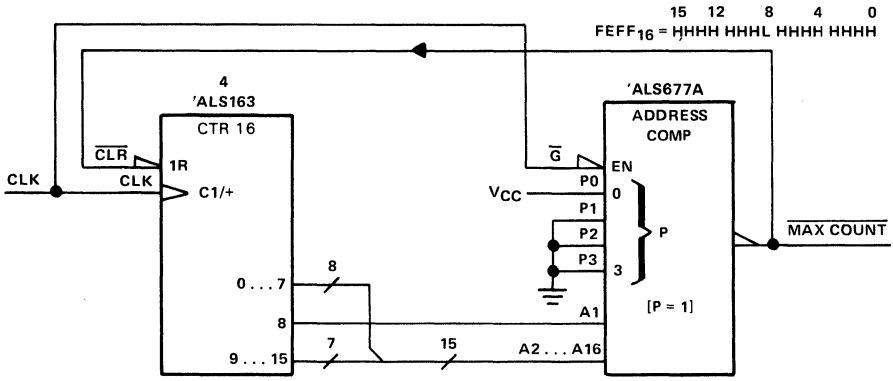
P3 to 0 V, P2 to V_{CC}, P1 to V_{CC}, and P0 to 0 V.

System address lines A13, A12, A9, A8, A5, and A4 to comparator inputs A1 through A6 in any convenient order.

The remaining ten system address lines to comparator inputs A7 through A16 in any convenient order.

The output provides an active-low enabling signal.

The following circuit is a modulo-N synchronous counter. The 'ALS163 is connected to provide a low-level clear signal when N = $FEFF_{16}$.



MODULO-N SYNCHRONOUS COUNTER

SN54ALS679, SN54ALS680, SN74ALS679, SN74ALS680
12-BIT ADDRESS COMPARATORS

D2661, JUNE 1982 – REVISED MAY 1986

- **'ALS679 is a 12-Bit Address Comparator with Enable**
- **'ALS680 is a 12-Bit Address Comparator with Latch**
- **Package Options Include "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

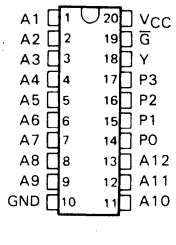
description

The 'ALS679 and 'ALS680 address comparators simplify addressing of memory boards and/or other peripheral devices. The four P inputs are normally hard wired with a preprogrammed address. An internal decoder determines what input information applied to the 12 A inputs must be low or high to cause a low state at the output (Y). For example, a positive-logic bit combination of 0111 (decimal 7) at the P input determines that inputs A1 through A7 must be low and that inputs A8 through A12 must be high-to cause the output to go low. Equality of the address applied at the A inputs to the preprogrammed address is indicated by the output being low.

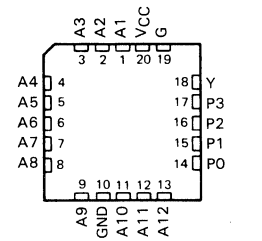
The 'ALS679 features an enable input ($\overline{G}$). When $\overline{G}$ is low, the device is enabled. When $\overline{G}$ is high, the device is disabled and the output is high regardless of the A and P inputs. The 'ALS680 features a transparent latch and a latch enable input (C). When C is high, the device is in the transparent mode. When C is low, the previous logic state of Y is latched.

The SN54ALS679 and SN54ALS680 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS679 and SN74ALS680 are characterized for operation from 0°C to 70°C.

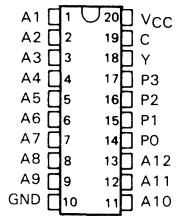
SN54ALS679 . . . J PACKAGE
SN74ALS679 . . . DW OR N PACKAGE
(TOP VIEW)



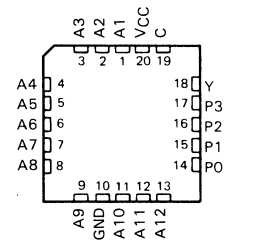
SN54ALS679 . . . FK PACKAGE
(TOP VIEW)



SN54ALS680 . . . J PACKAGE
SN74ALS680 . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS680 . . . FK PACKAGE
(TOP VIEW)



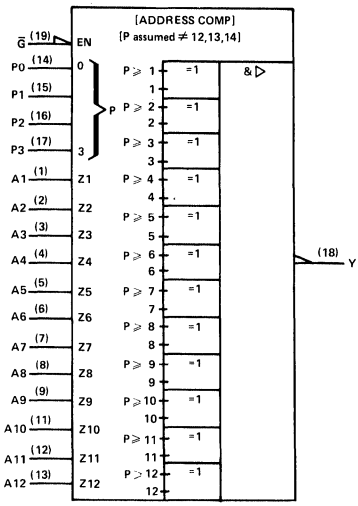
FUNCTION TABLE

'ALS679	'ALS680	INPUTS COMMON TO 'ALS679 AND 'ALS680																OUTPUT
$\overline{G}$	C	P3	P2	P1	P0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	Y
L	H	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	H	H	L	L	L	H	H	H	H	H	H	H	H	H	L
L	H	L	H	L	L	L	L	L	L	H	H	H	H	H	H	H	H	L
L	H	L	H	L	H	L	L	L	L	L	H	H	H	H	H	H	H	L
L	H	L	H	H	L	L	L	L	L	L	L	H	H	H	H	H	H	L
L	H	L	H	H	H	L	L	L	L	L	L	L	H	H	H	H	H	L
L	H	H	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	L
L	H	H	L	L	H	L	L	L	L	L	L	L	L	L	H	H	H	L
L	H	H	L	H	L	L	L	L	L	L	L	L	L	L	L	H	H	L
L	H	H	L	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L
L	H	H	H	L	L	L	L	L	L	L	L	L	L	H	H	H	L	L†
L	H	H	H	L	H	L	L	L	L	L	L	L	L	L	H	H	L	L†
L	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	H	L	L†
L	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L
L	H	All other combinations																H
H		'ALS679: Any combination																H
	L	'ALS680: Any combination																Latched

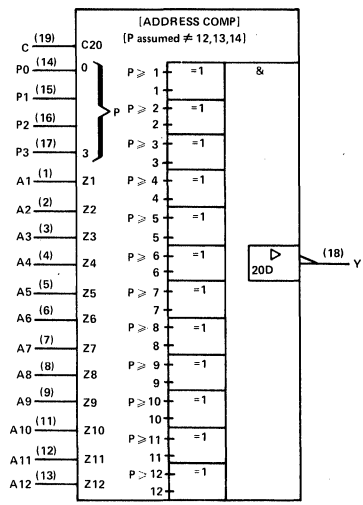
†The three shaded rows of the function table show combinations that would normally not be used in address comparator applications. The logic symbols above are not valid for these combinations in which P = 12, 13, and 14. If symbols valid for all combinations are required, starting with the fourth Exclusive-OR from the bottom, change P ≥ 9 to P = 9 . . . 11/13 . . . 15, P ≥ 10 to P = 10/11/14/15, and P ≥ 11 to P = 11/15.

logic symbols‡

'ALS679



'ALS680



‡These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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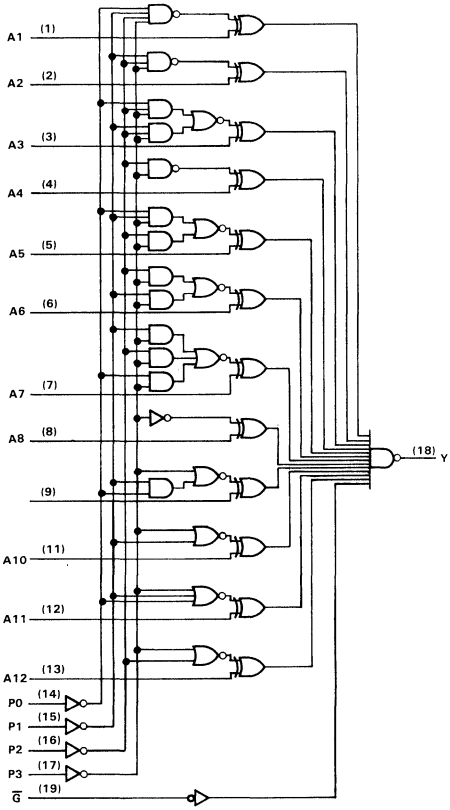
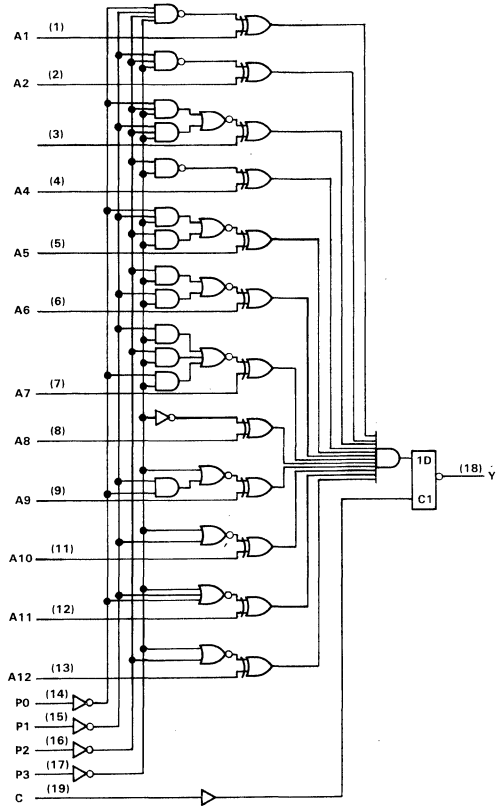
logic diagrams (positive logic)

'ALS679



'ALS680



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS679, SN54ALS680 . . . . . −55°C to 125°C
SN74ALS679, SN74ALS680 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS679 SN54ALS680			SN74ALS679 SN74ALS680			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−1			−2.6	mA
I_{OL}	Low-level output current				12			24	mA
t_w	Pulse duration, Enable C high	'ALS680	45			40			ns
t_{su}	Setup time, Data before C↓	'ALS680	50			45			ns
t_h	Hold time, Data after C↓	'ALS680	10			5			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS679 SN54ALS680			SN74ALS679 SN74ALS680			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS679	V_{CC} = 5.5 V			17	28		17	28	mA
	'ALS680				18	27		18	27	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

TEXAS INSTRUMENTS
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'ALS679 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS679		SN74ALS679		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any P	Y	4	28	4	25	ns
t_{PHL}			8	40	8	35	
t_{PLH}	Any A	Y	5	26	5	22	ns
t_{PHL}			5	35	5	30	
t_{PLH}	$\overline{G}$	Y	3	15	3	13	ns
t_{PHL}			5	30	5	25	

'ALS680 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V C_L = 50 pF R_L = 500 Ω T_A = MIN to MAX				UNIT
			SN54ALS680		SN74ALS680		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any P	Y	6	27	6	22	ns
t_{PHL}			10	43	10	38	ns
t_{PLH}	Any A	Y	5	25	5	21	ns
t_{PHL}			5	28	5	25	
t_{PLH}	C	Y	3	25	3	20	ns
t_{PHL}			15	48	15	42	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TYPICAL APPLICATION INFORMATION

The 'ALS679 and 'ALS680 can be wired to recognize any one of 2^{12} addresses. The number of "lows" in the address determines the input pattern for the P inputs. Then those system address lines that are low in the address to be recognized are connected to the lowest numbered A inputs of the address comparator and the system address lines that are high are connected to the highest numbered A inputs.

For example, assume the comparator is to enable a device when the 12-bit system address is:

A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
H	H	L	L	H	H	L	L	H	H	H	H

Since the address contains 4 lows and 8 highs, the following connections are made:

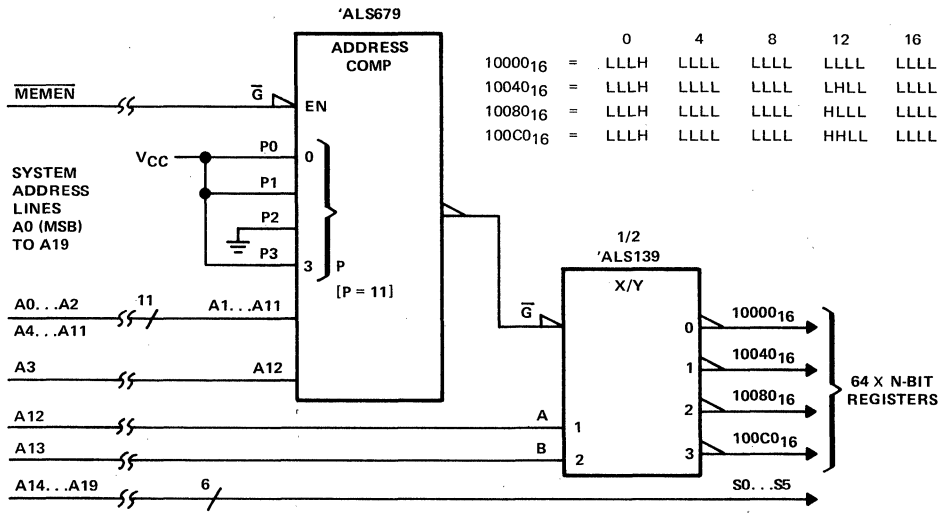
P3 to 0 V, P2 to V_{CC}, P1 to 0 V, and P0 to 0 V.

System address lines A9, A8, A5, and A4 to comparator inputs A1 through A4 in any convenient order.

The remaining eight system address lines to comparator inputs A5 through A12 in any convenient order.

The output provides an active-low enabling signal.

The following circuit is a register bank decoder that examines the 14 most significant bits (A0 through A13) of a 20-bit address to select banks corresponding to the hex addresses 10000, 10040, 10080, and 100C0.



REGISTER BANK DECODER

TEXAS INSTRUMENTS
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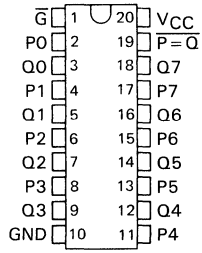
D2661, JUNE 1982 – REVISED MAY 1986

- **Compares Two Eight-Bit Words**
- **Choice of Totem-Pole or Open-Collector Outputs**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

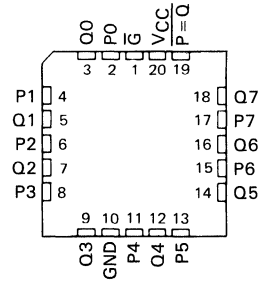
TYPE	OUTPUT FUNCTION AND CONFIGURATION
'ALS688†	$\overline{P=Q}$ totem pole
'ALS689	$\overline{P=Q}$ open-collector

†'ALS688 is identical to 'ALS521

SN54ALS688, SN54ALS689 . . . J PACKAGE
SN74ALS688, SN74ALS689 . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS688, SN54ALS689 . . . FK PACKAGE
(TOP VIEW)



description

These identity comparators perform comparisons of two eight-bit binary or BCD words. The 'ALS688 and 'ALS689 provide $\overline{P=Q}$ outputs. The 'ALS688 has totem-pole outputs, while 'ALS689 has open-collector outputs.

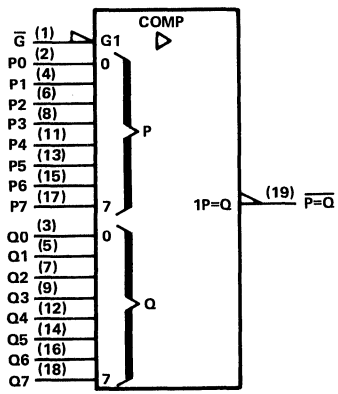
The SN54ALS688 and SN54ALS689 are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS688 and SN74ALS689 are characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE

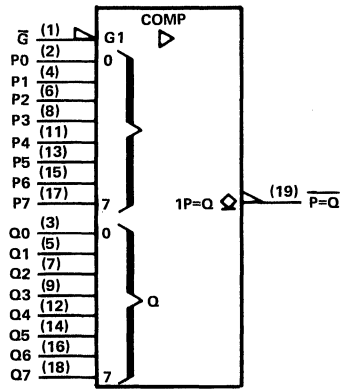
INPUTS		OUTPUT
DATA P,Q	ENABLE $\overline{G}$	$\overline{P=Q}$
P=Q	L	L
P>Q	L	H
P<Q	L	H
X	H	H

logic symbols‡

'ALS688

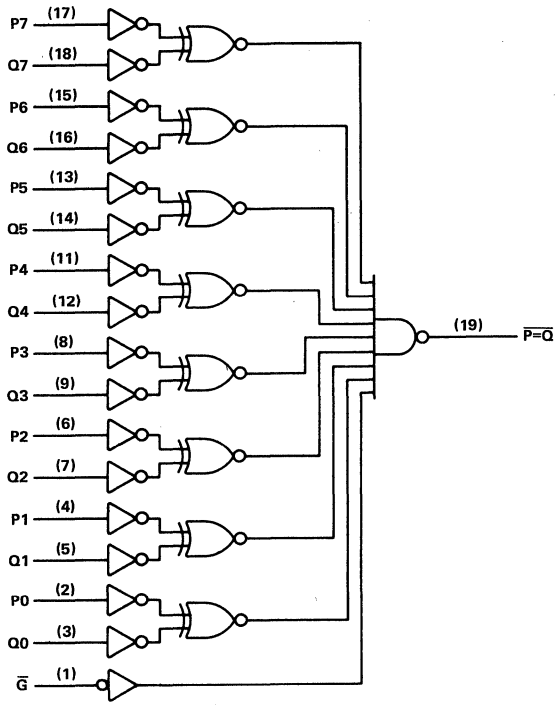


'ALS689



‡These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: . . . . . 7 V
Off-state output voltage: 'ALS689 . . . . . 7 V
Operating free-air temperature range: SN54ALS688, SN54AS689 . . . . . −55 °C to 125 °C
SN74ALS688, SN74AS689 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS688			SN74ALS688			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS688			SN74ALS688			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} −2			V_{CC} −2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	See Note 1		12	19		12	19	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with G grounded, P and Q at 4.5 V.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS688		SN74ALS688		
			MIN	MAX	MIN	MAX	
t_{PLH}	P	$\overline{P=Q}$	3	16	3	12	ns
t_{PHL}			5	25	5	20	
t_{PLH}	Q	$\overline{P=Q}$	3	16	3	12	ns
t_{PHL}			5	25	5	20	
t_{PLH}	$\overline{G}$	$\overline{P=Q}$	3	15	3	12	ns
t_{PHL}			5	25	5	22	

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

recommended operating conditions

		SN54ALS689			SN74ALS689			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			5.5			5.5	V
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS689			SN74ALS689			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = 5.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_{CC}	V_{CC} = 5.5 V,	See Note 1		12	19		12	19	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: I_{CC} is measured with G grounded, P and Q at 4.5 V.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX				UNIT
			SN54ALS689		SN74ALS689		
			MIN	MAX	MIN	MAX	
t_{PLH}	P	$\overline{P=Q}$	10	30	10	25	ns
t_{PHL}			5	25	5	23	
t_{PLH}	Q	$\overline{P=Q}$	10	30	10	25	ns
t_{PHL}			5	25	5	23	
t_{PLH}	$\overline{G}$	$\overline{P=Q}$	8	30	8	25	ns
t_{PHL}			8	30	8	25	

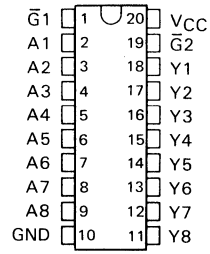
NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

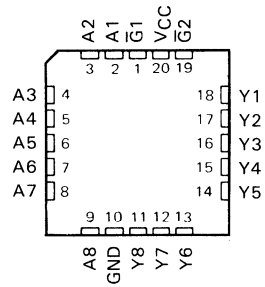
AUGUST 1984 – REVISED MAY 1986

- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Input Pull-Up Resistors Added for Data Bus Termination**
- **Data Flow-Thru Pinout (All Inputs on Opposite Side from Outputs)**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS746, SN54ALS747 . . . J PACKAGE
SN74ALS746, SN74ALS747 . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS746, SN54ALS747 . . . FK PACKAGE
(TOP VIEW)



description

These octal buffers and line drivers are designed to have the performance of the popular SN54ALS240A/SN74ALS240A series and, at the same time, offer a pinout with inputs and outputs on opposite sides of the package. This arrangement greatly enhances printed circuit board layout. In addition, 20 kilohm resistors have been added between all inputs and V_{CC}. This eliminates adding external resistors in applications where the data bus must be at a high level whenever all other connecting devices are at a high impedance state.

The three-state control gate is a 2-input NOR such that if either $\overline{G}1$ or $\overline{G}2$ is high, all eight outputs are in the high-impedance state.

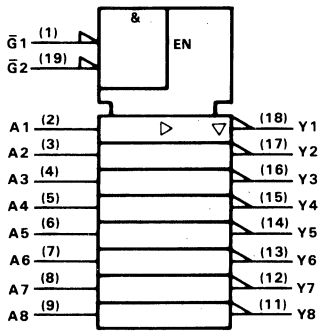
The 'ALS746 provides inverted data and the 'ALS747 provides true data at the outputs.

The -1 versions of the SN74ALS746 and SN74ALS747 parts are identical to the standard versions except that the recommended maximum I_{OL} is increased to 48 milliampers. There are no -1 versions of the SN54ALS746 and SN54ALS747.

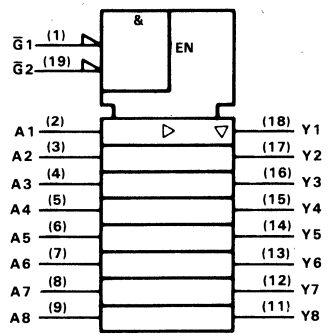
The SN54ALS746 and SN54ALS747 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN54ALS746 and SN74ALS747 are characterized for operation from 0°C to 70°C.

logic symbols†

'ALS746



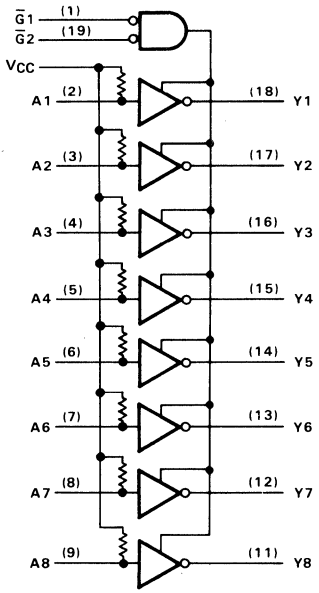
'ALS747



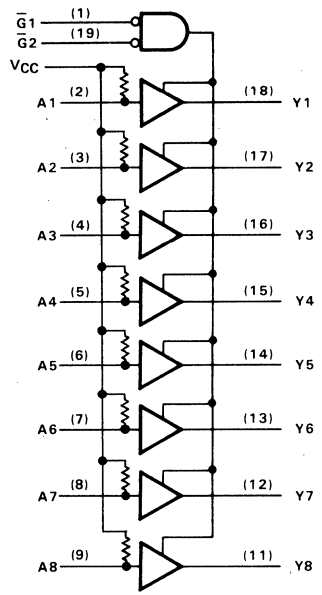
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)

'ALS746



'ALS747



All input pull-up resistors are 20 kΩ

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS746, SN54ALS747 . . . . . −55°C to 125°C
SN74ALS746, SN74ALS747 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS746 SN54ALS747			SN74ALS746 SN74ALS747			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
							48†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limit applies only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48 mA limit applies for the SN74ALS746-1 and SN74ALS747-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS746 SN54ALS747			SN74ALS746 SN74ALS747			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA¶					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	A	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	mA
	$\overline{G}1$, $\overline{G}2$	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	
I_{IH}	A	V_{CC} = 5.5 V,	V_I = 2.7 V			−0.2			−0.2	mA
	$\overline{G}1$, $\overline{G}2$					20			20	μA
I_{IL}	A	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.6			−0.6	mA
	$\overline{G}1$, $\overline{G}2$					−0.1			−0.1	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS746	V_{CC} = 5.5 V,	Outputs high		7	12		7	12	mA
			Outputs low		13	22		13	22	
			Outputs disabled		11	19		11	19	
	'ALS747	V_{CC} = 5.5 V,	Outputs high		6	14		6	14	mA
			Outputs low		18	30		18	30	
			Outputs disabled		12.5	22		12.5	22	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely aproximates one half of the true short-circuit output current, I_{OS}.
¶I_{OL} = 48 mA for -1 versions.

'ALS746 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS746	SN54ALS746		SN74ALS746		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	7.5	3	14	3	12	ns
t_{PHL}			5.6	2	11	2	9	
t_{PZH}	$\overline{G}$	Y	9	5	18	5	15	ns
t_{PZL}			12.5	8	24	8	20	
t_{PHZ}	$\overline{G}$	Y	4	1	12	1	10	ns
t_{PLZ}			7	2	14	2	12	

'ALS747 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS747	SN54ALS747		SN74ALS747		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	8.7	4	17	4	14	ns
t_{PHL}			7.4	2	12	2	10	
t_{PZH}	$\overline{G}$	Y	9	5	18	5	15	ns
t_{PZL}			12.5	8	24	8	20	
t_{PHZ}	$\overline{G}$	Y	4	1	12	1	10	ns
t_{PLZ}			7	2	14	2	12	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

OCTAL BUFFERS AND LINE DRIVERS WITH OPEN-COLLECTOR OUTPUTS

D2661, DECEMBER 1983—REVISED MAY 1986

- **Open-Collector Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Eliminates the Need for 3-State Overlap Protection**
- **P-N-P Inputs Reduce DC Loading**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Open-Collector Versions of 'ALS240A, 'ALS241A, and 'AS240, 'AS241**
- **Dependable Texas Instruments Quality and Reliability**

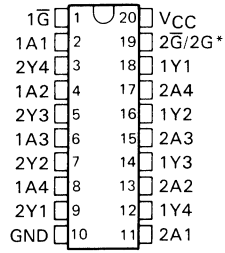
description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters by eliminating the need for three-state overlap protection. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs. These devices feature high fan-out and improved fan-in.

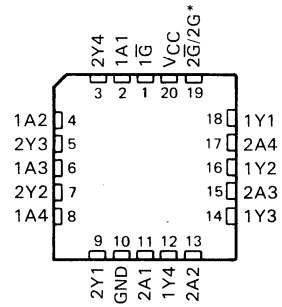
The -1 version of the SN74ALS756 is identical to the standard version except that the recommended maximum I_{OL} is increased to 48 milliamperes. There is no -1 version of the SN54ALS756.

The SN54' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

SN54ALS', SN54AS' . . . J PACKAGE
SN74ALS', SN74AS' . . . DW OR N PACKAGE
(TOP VIEW)



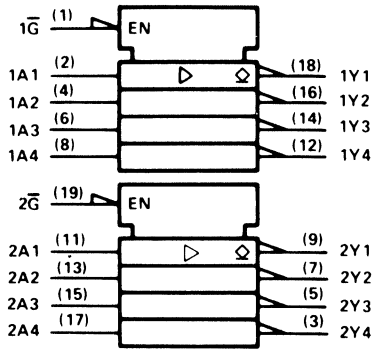
SN54ALS', SN54AS' . . . FK PACKAGE
(TOP VIEW)



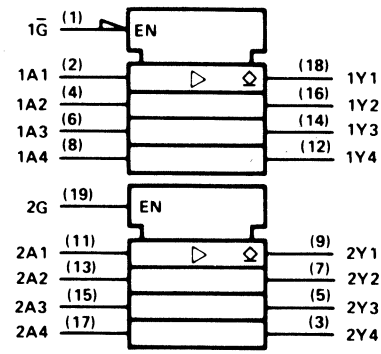
*$2\overline{G}$ for 'ALS756, 'AS756 or 2G for 'AS757.

logic symbols†

'ALS756, 'AS756



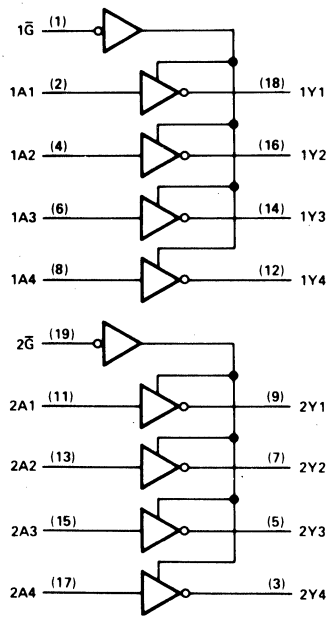
'AS757



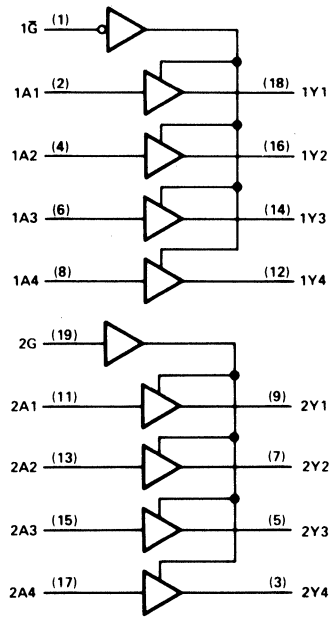
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)

'ALS756, 'AS756



'AS757



TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS756 . . . . . −55°C to 125°C
SN74ALS756 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS756			SN74ALS756			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			12			24	mA
							48†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The 48-mA limit applies only to the −1 versions and only if V_{CC} is maintained between 4.75 V and 5.25 V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS756			SN74ALS756			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA§					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_{CC}	V_{CC} = 5.5 V	Output high		7	11		7	11	mA
		Output low		13	22		13	22	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§V_{CC} = 4.75 V and I_{OL} = 48 mA for -1 versions.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS756	SN54ALS756		SN74ALS756		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	14	8	29	8	24	ns
t_{PHL}			5	2	12	2	10	
t_{PLH}	$\overline{G}$	Y	16	8	29	8	24	ns
t_{PHL}			12	6	23	6	20	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54AS756, SN54AS757 . . . . . −55°C to 125°C
SN74AS756, SN74AS757 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS756 SN54AS757			SN74AS756 SN74AS757			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			SN54AS756 SN54AS757			SN74AS756 SN74AS757			UNIT
					MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2			−1.2	V
I_{OH}		V_{CC} = 4.5 V,	V_{OH} = 5.5 V				0.1			0.1	mA
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA			0.55					V
		V_{CC} = 4.5 V,	I_{OL} = 64 mA							0.55	
I_I		V_{CC} = 5.5 V,	V_I = 7 V				0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V				20			20	μA
I_{IL}	A inputs of 'AS757 only	V_{CC} = 5.5 V,	V_I = 0.4 V				−1			−1	mA
	All other inputs						−0.5			−0.5	
I_{CC}	'AS756	V_{CC} = 5.5 V,		Output high		9	15		9	15	mA
				Output low		51	80		51	80	
	'AS757			Output high		21	33		21	33	
				Output low		61	95		61	95	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

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'AS756 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS756		SN74AS756		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	3	20	3	19	ns
t_{PHL}			1	7	1	6	
t_{PLH}	$\overline{G}$	Y	3	22	3	19.5	ns
t_{PHL}			1	8.5	1	7.5	

'AS757 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS757		SN74AS757		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	3	19.5	3	18.5	ns
t_{PHL}			1	7	1	6	
t_{PLH}	$1\overline{G}$	Y	3	21	3	20	ns
t_{PHL}			1	8	1	7	
t_{PLH}	2G	Y	3	22.5	3	21	ns
t_{PHL}			1	8.5	1	7.5	

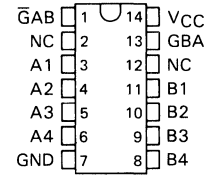
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

QUADRUPLE BUS TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS

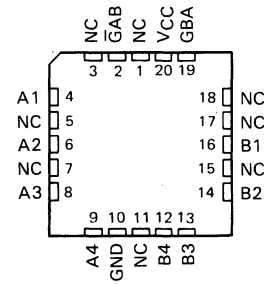
D2910, DECEMBER 1983—REVISED MAY 1986

- **2-Way Asynchronous Communication Between Data Buses**
- **P-N-P Inputs Reduce Loading**
- **Open-Collector Versions of 'ALS242A, 'ALS243A and 'AS242, 'AS243**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54' . . . J PACKAGE
SN74' . . . D OR N PACKAGE
(TOP VIEW)



SN54' . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

These four-data-line transceivers are designed for asynchronous two-way communications between data buses.

The -1 versions of the SN74ALS' parts are identical to their standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes. There are no -1 versions of the SN54ALS' parts.

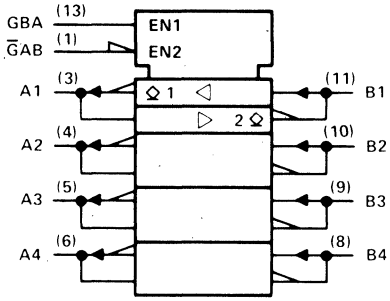
The SN54' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

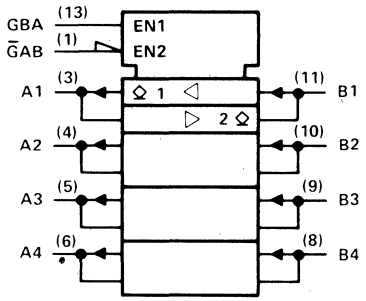
INPUTS		'ALS758 'AS758	'AS759
$\overline{G}AB$	GBA		
L	L	$\overline{A}$ to B	A to B
H	H	$\overline{B}$ to A	B to A
H	L	Isolation	Isolation
L	H	Latch A and B ($A = \overline{B}$)	Latch A and B ($A = B$)

logic symbols†

'ALS758, 'AS758

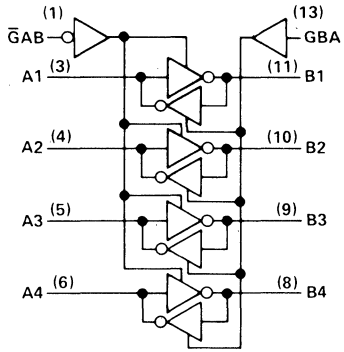


'AS759

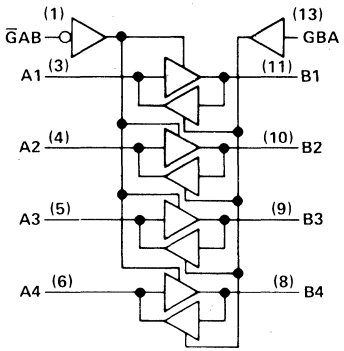


logic diagrams (positive logic)

'ALS758, 'AS758



'AS759



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs and I/O ports . . . . . 7 V
Operating free-air temperature range: SN54' . . . . . −55°C to 125°C
SN74' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

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recommended operating conditions

		SN54ALS758			SN74ALS758			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			12			24	mA
							48†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limit applies only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48 mA limit applies for the SN74ALS758-1.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS758			SN74ALS758			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
I_{OH}		V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA§					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports¶					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	A or B ports¶					−0.1			−0.1	
I_{CC}		V_{CC} = 5.5 V	Outputs high		6	10		6	10	mA
			Outputs low		10	16		10	16	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§I_{OL} = 48 mA for -1 versions.
¶For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 680 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX				UNIT
			'ALS758	SN54ALS758		SN74ALS758		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	20	10	33	10	28	ns
t_{PHL}			5	2	15	2	12	
t_{PLH}	GBA	A	18	10	33	10	28	ns
t_{PHL}			13	6	25	6	21	
t_{PLH}	$\overline{G}AB$	B	18	10	33	10	28	ns
t_{PHL}			13	6	25	6	21	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

recommended operating conditions

		SN54AS758			SN74AS758			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS758			SN74AS758			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
I_{OH}		V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA			0.55				V
		V_{CC} = 4.5 V,	I_{OL} = 64 mA						0.55	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports					50			50	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	A or B ports‡					−0.5			−0.5	
I_{CC}		V_{CC} = 5.5 V	Outputs high		17	27		17	27	mA
			Outputs low		38	60		38	60	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS758		SN74AS758		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	3	20.5	3	19.5	ns
t_{PHL}			1	7	1	6	
t_{PLH}	GBA	A	3	22	3	19.5	ns
t_{PHL}			1	8.5	1	7.5	
t_{PLH}	$\overline{G}AB$	B	3	22	3	21	ns
t_{PHL}			1	8.5	1	8	

NOTE 1. Load circuit and voltage waveforms are shown in Section 1.

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recommended operating conditions

		SN54AS759			SN74AS759			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS759			SN74AS759			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
I_{OH}		V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA			0.55				V
		V_{CC} = 4.5 V,	I_{OL} = 64 mA						0.55	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports					50			50	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	A or B ports‡					−1			−1	
I_{CC}		V_{CC} = 5.5 V	Outputs high		27	43		27	43	mA
			Outputs low		47	74		47	74	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS759		SN74AS759		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	3	21	3	20	ns
t_{PHL}			1	7	1	6	
t_{PLH}	GBA	A	3	21	3	20	ns
t_{PHL}			1	8	1	7	
t_{PLH}	$\overline{G}AB$	B	3	22.5	3	21	ns
t_{PHL}			1	8.5	1	7.5	

NOTE 1. Load circuit and voltage waveforms are shown in Section 1.

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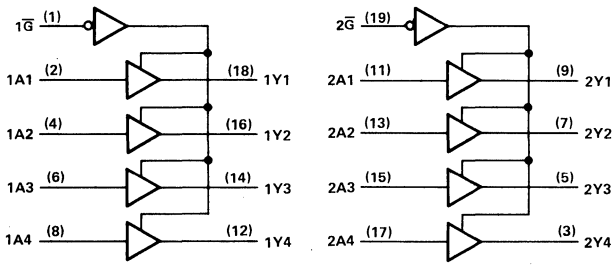
- **Open-Collector Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Eliminates the Need for 3-State Overlap Protection**
- **P-N-P Inputs Reduce DC Loading**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Open-Collector Versions of 'ALS244 and 'AS244**
- **Dependable Texas Instruments Quality and Reliability**

description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters by eliminating the need for 3-state overlap protection. Taken together with the 'ALS756, 'AS756, and 'AS757, these devices provide the choice of selected combinations of inverting outputs, symmetrical $\overline{G}$ (active-low input control) inputs, and complimentary G and $\overline{G}$ inputs.

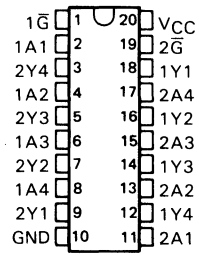
The SN54ALS760 and SN54AS760 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS760 and SN74AS760 are characterized for operation from 0°C to 70°C.

logic diagram (positive logic)

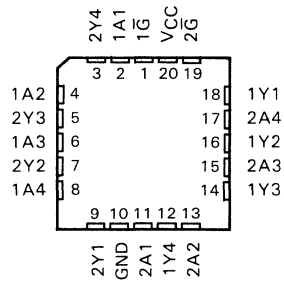


Pin numbers shown are for DW, J, and N packages.

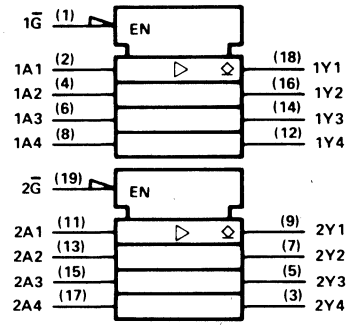
SN54ALS760, SN54AS760 . . . J PACKAGE
SN74ALS760, SN74AS760 . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS760, SN54AS760 . . . FK PACKAGE
(TOP VIEW)



logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS760 . . . . . −55°C to 125°C
SN74ALS760 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS760			SN74ALS760			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS760			SN74ALS760			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.5		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		9			9		mA
		Outputs low		15			15		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS760			SN74ALS760			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y		22			22		ns
t_{PHL}				13			13		
t_{PLH}	$\overline{G}$	Y		25			25		ns
t_{PHL}				24			24		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54AS760 . . . . . −55°C to 125°C
SN74AS760 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS760			SN74AS760			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS760			SN74AS760			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
I_{OH}		V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA			0.55				V
		V_{CC} = 4.5 V,	I_{OL} = 64 mA						0.55	
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	$\overline{G}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	A					−1			−1	
I_{CC}		V_{CC} = 5.5 V	Outputs high		20	32		20	32	mA
			Outputs low		60	94		60	94	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS760		SN74AS760		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	3	19.5	3	18.5	ns
t_{PHL}			1	7	1	6	
t_{PLH}	$\overline{G}$	Y	3	19.5	3	18.5	ns
t_{PHL}			1	8	1	7	

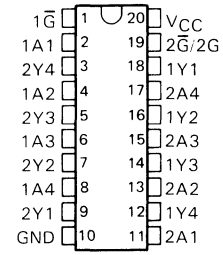
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

OCTAL BUFFERS AND LINE DRIVERS WITH OPEN-COLLECTOR OUTPUTS

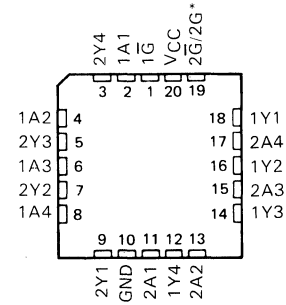
DECEMBER 1983—REVISED MAY 1986

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **'ALS762 and 'AS762 Have True and Complementary Outputs**
- **'ALS763 and 'AS763 Have Complementary G and $\overline{G}$ Inputs**
- **Open-Collector Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Eliminates the Need for 3-State Overlap Protection**
- **Current Sinking Capability Up to 64 mA**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS', SN54AS' . . . J PACKAGE
SN74ALS', SN74AS' . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS', SN54AS' . . . FK PACKAGE
(TOP VIEW)



*2$\overline{G}$ for 'ALS762, 'AS762 and 2G 'ALS763, 'AS763

description

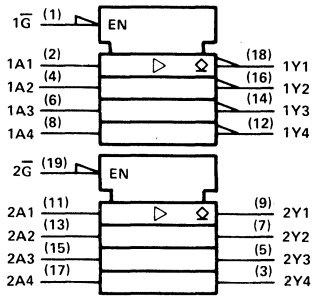
These octal buffers and line drivers are designed specifically to improve the performance of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters by eliminating the need for 3-state overlap protection. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs.

The -1 versions of the SN74ALS' parts are identical to their standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes. There are no -1 versions of the SN54ALS' parts.

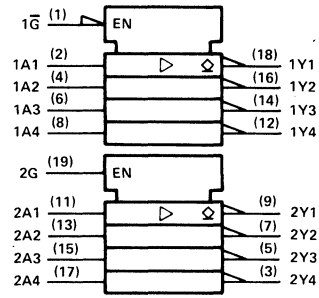
The SN54' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

logic symbols†

'ALS762, 'AS762



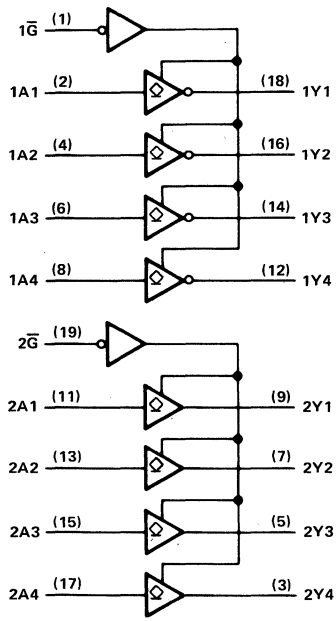
'ALS763, 'AS763



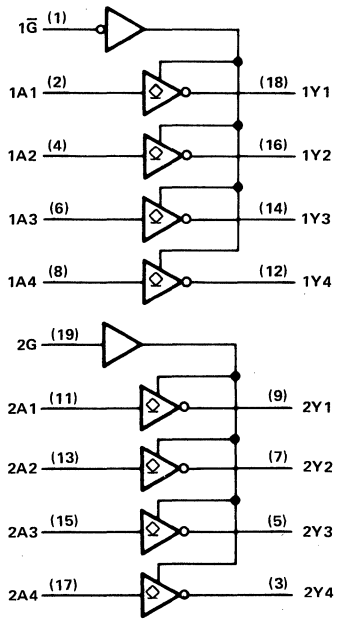
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)

'ALS762, 'AS762



'ALS763, 'AS763



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS762 . . . . . −55°C to 125°C
SN74ALS762 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS762			SN74ALS762			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			12			24	mA
							48†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48-mA limit applies for the SN74ALS762-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS762			SN74ALS762			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V, I_I = −18 mA				−1.2			−1.2	V
I_{OH}		V_{CC} = 4.5 V, V_{OH} = 5.5 V				0.1			0.1	mA
V_{OL}		V_{CC} = 4.5 V, I_{OL} = 12 mA			0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, I_{OL} = 24 mA (I_{OL} = 48 mA for -1 versions)						0.35	0.5	
I_I		V_{CC} = 5.5 V, V_I = 7 V				0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V, V_I = 2.7 V				20			20	μA
I_{IL}		V_{CC} = 5.5 V, V_I = 0.4 V				−0.1			−0.1	mA
I_{CC}	'ALS762	V_{CC} = 5.5 V	Outputs high		11			11		mA
			Outputs low		18			18		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

'ALS762 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 680 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX		UNIT
			'ALS762	SN54ALS762	SN74ALS762	
			TYP	MIN MAX	MIN MAX	
t_{PLH}	A	Y	17			ns
t_{PHL}			6			
t_{PLH}	$\overline{G}$	Y	14			ns
t_{PHL}			18			

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS763 . . . . . −55°C to 125°C
SN74ALS763 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS763			SN74ALS763			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			12			24	mA
							48†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48-mA limit applies for the SN74ALS763-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS763			SN74ALS763			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
I_{OH}		V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, (I_{OL} = 48 mA for -1 versions)	I_{OL} = 24 mA					0.35	0.5	
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_{CC}	'ALS763	V_{CC} = 5.5 V	Outputs high		7	11		7	11	mA
			Outputs low		14	22		14	22	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

'ALS763 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 680 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX				UNIT
			'ALS763	SN54ALS763		SN74ALS763		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	16	7	28	7	25	ns
t_{PHL}			5	2	11	2	9	
t_{PLH}	$\overline{G}$	Y	18	8	28	9	25	ns
t_{PHL}			13	5	25	5	21	
t_{PLH}	G	Y	18	8	28	9	25	ns
t_{PHL}			13	5	25	5	21	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54AS762, SN54AS763 . . . . . −55°C to 125°C
SN74AS762, SN74AS763 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS762 SN54AS763			SN74AS762 SN74AS763			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS762 SN54AS763			SN74AS762 SN74AS763			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
I_{OH}		V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA			0.55				V
		V_{CC} = 4.5 V,	I_{OL} = 64 mA						0.55	
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	'AS762 2A inputs only	V_{CC} = 5.5 V,	V_I = 0.4 V			−1			−1	mA
	All others					−0.5			−0.5	
I_{CC}	'AS762	V_{CC} = 5.5 V	Output high		15	23		15	23	mA
			Output low		55	87		55	87	
	'AS763	V_{CC} = 5.5 V	Output high		10	16		10	16	
			Output low		52	82		52	82	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

'AS762 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS762		SN74AS762		
			MIN	MAX	MIN	MAX	
t_{PLH}	1A	1Y	3	20	3	19	ns
t_{PHL}			1	7	1	6	
t_{PLH}	2A	2Y	3	19.5	3	18.5	ns
t_{PHL}			1	7	1	6	
t_{PLH}	$\overline{G}$	1Y	3	22	3	19.5	ns
t_{PHL}			1	8	1	7.5	
t_{PLH}	$\overline{G}$	2Y	3	20	3	19	ns
t_{PHL}			1	8	1	7	

'AS763 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS763		SN74AS763		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	3	20	3	19	ns
t_{PHL}			1	7	1	6	
t_{PLH}	$\overline{G}$	Y	3	22	3	19.5	ns
t_{PHL}			1	8.5	1	7.5	
t_{PLH}	G	Y	3	22	3	20	ns
t_{PHL}			1	8.5	1	8	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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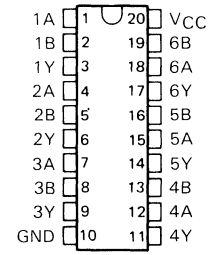
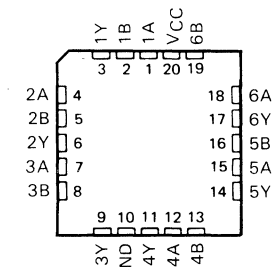
D2661, DECEMBER 1982 – REVISED MAY 1986

- **High Capacitive Drive Capability**
- **'ALS804A has Typical Delay Time of 4 ns (C_L = 50 pF) and Typical Power Dissipation of 3.4 mW per Gate**
- **'AS804B has Typical Delay Time of 2.6 ns (C_L = 50 pF) and Typical Power Dissipation of Less than 9 mW per Gate**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS804A, SN54AS804B . . . J PACKAGE
SN74ALS804A, SN74AS804B . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS804A, SN54AS804B . . . FK PACKAGE
(TOP VIEW)



description

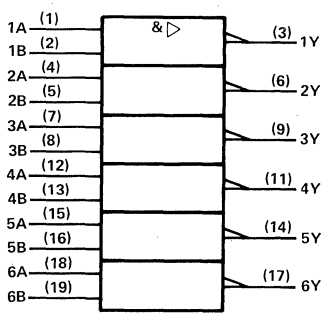
These devices contain six independent 2-input NAND drivers. They perform the Boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The SN54ALS804A and SN54AS804B are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS804A and SN74AS804B are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each driver)

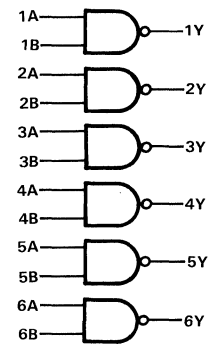
INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS804A . . . . . −55°C to 125°C
SN74ALS804A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 50°C

recommended operating conditions

		SN54ALS804A			SN74ALS804A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS804A			SN74ALS804A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.9	2.5		0.9	2.5	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		7	12		7	12	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS804A	SN54ALS804A		SN74ALS804A		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	4	2	9	2	7	ns
t_{PHL}			4	2	9	2	8	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS804B . . . . . −55°C to 125°C
SN74AS804B . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 50°C

recommended operating conditions

		SN54AS804B			SN74AS804B			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−40			−48	mA
I_{OL}	Low-level output current			40			48	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS804B			SN74AS804B			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −40 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −48 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 40 mA		0.25	0.5				V
	V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25	−50		−200	−50		−200	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		3.5	5		3.5	5	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		16	27		16	27	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

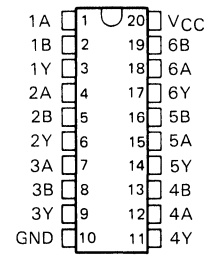
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS804B		SN74AS804B		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1	5	1	4	ns
t_{PHL}			1	5	1	4	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

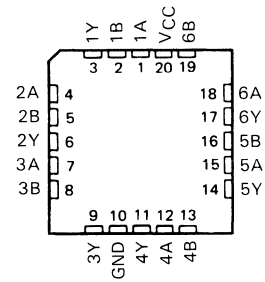
D2661, DECEMBER 1982 – REVISED MAY 1986

- **High Capacitive Drive Capability**
- **'ALS805A has Typical Delay Time of 4.2 ns (C_L = 50 pF) and Typical Power Dissipation of 4.2 mW per Gate**
- **'AS805B has Typical Delay Time of 2.6 ns (C_L = 50 pF) and Typical Power Dissipation of 12 mW per Gate**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS805A, SN54AS805B . . . J PACKAGE
SN74ALS805A, SN74AS805B . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS805A, SN54AS805B . . . FK PACKAGE
(TOP VIEW)



description

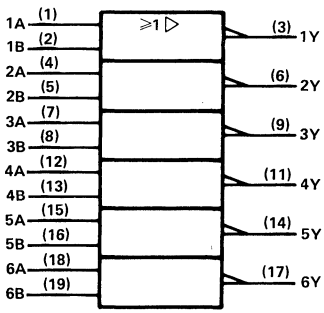
These devices contain six independent 2-input NOR drivers. They perform the Boolean functions $Y = \overline{A+B}$ or $Y = \overline{A} \cdot \overline{B}$ in positive logic.

The SN54ALS805A and SN54AS805B are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS805A and SN74AS805B are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each driver)

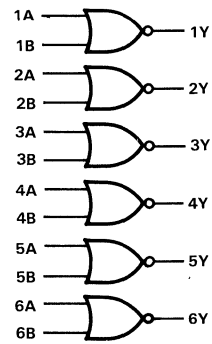
INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS805A . . . . . −55°C to 125°C
SN74ALS805A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS805A			SN74ALS805A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS805A			SN74ALS805A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		2	4		2	4	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		8	14		8	14	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS805A	SN54ALS805A		SN74ALS805A		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	4	2	9	2	7	ns
t_{PHL}			4	2	9	2	8	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS805B . . . . . −55°C to 125°C
SN74AS805B . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS805B			SN74AS805B			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−40			−48	mA
I_{OL}	Low-level output current			40			48	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS805B			SN74AS805B			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −40 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −48 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 40 mA		0.25	0.5				V
	V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−50		−200	−50		−200	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		6.5	10		6.5	10	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		20	32		20	32	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

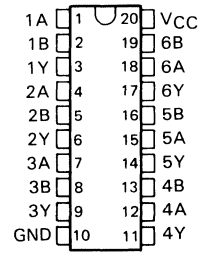
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS805B		SN74AS805B		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1	4.8	1	4.3	ns
t_{PHL}			1	4.8	1	4.3	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

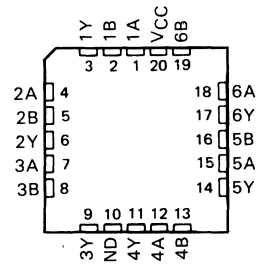
D2661, DECEMBER 1982 – REVISED MAY 1986

- **High Capacitive Drive Capability**
- **'ALS808A has Typical Delay Time of 4.8 ns (C_L = 50 pF) and Typical Power Dissipation of 4.5 mW per Gate**
- **'AS808B has Typical Delay Time of 3.2 ns (C_L = 50 pF) and Typical Power Dissipation of Less than 13 mW per Gate**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS808A, SN54AS808B . . . J PACKAGE
SN74ALS808A, SN74AS808B . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS808A, SN54AS808B . . . FK PACKAGE
(TOP VIEW)



description

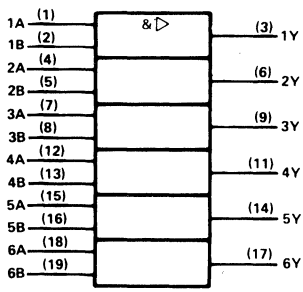
These devices contain six independent 2-input AND drivers. They perform the Boolean functions $Y = A \cdot B$ or $Y = \overline{\overline{A} + \overline{B}}$ in positive logic.

The SN54ALS808A and SN54AS808B are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS808A and SN74AS808B are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each driver)

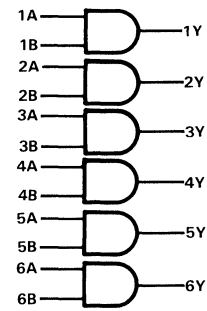
INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS808A . . . . . −55°C to 125°C
SN74ALS808A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS808A			SN74ALS808A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS808A			SN74ALS808A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
	V_{CC} = 4.5 V,	I_{OL} = −15 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		4.5	7		4.5	7	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		8	16		8	16	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS808A	SN54ALS808A		SN74ALS808A		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	6	2	11	2	9	ns
t_{PHL}			4	1	10	1	8	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS808B . . . . . −55°C to 125°C
SN74AS808B . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS808B			SN74AS808B			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−40			−48	mA
I_{OL}	Low-level output current			40			48	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS808B			SN74AS808B			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −40 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −48 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 40 mA		0.25	0.5				V
	V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−50		−200	−50		−200	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		8	13		8	13	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		20	33		20	33	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS808B		SN74AS808B		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1	6.5	1	6	ns
t_{PHL}			1	6.5	1	6	

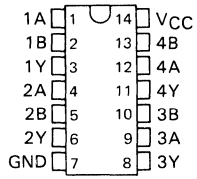
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

ALS and AS Circuits

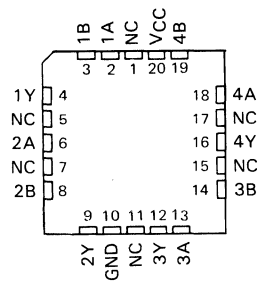
D2837, MARCH 1984—REVISED MAY 1986

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS810, SN54AS810 . . . J PACKAGE
SN74ALS810, SN74AS810 . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS810, SN54AS810 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

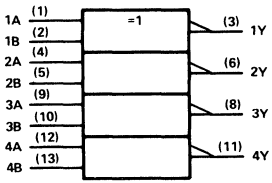
description

These devices contain four independent Exclusive-NOR gates. They perform the Boolean functions $Y = \overline{A \oplus B} = (A+\overline{B})\cdot(\overline{A}+B)$ in positive logic.

A common application is a true/complement element. If one of the inputs is high, the other input will be reproduced in true form at the output. If one of the inputs is low, the signal on the other input will be reproduced inverted at the output.

The SN54ALS810 and SN54AS810 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS810 and SN74AS810 are characterized for operation from 0° to 70°C.

logic symbol†



FUNCTION TABLE
(each gate)

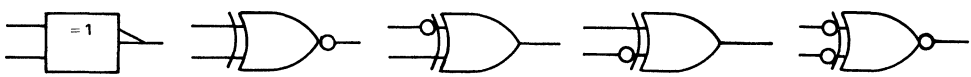
INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H

†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

exclusive-NOR logic

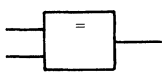
An exclusive-NOR gate has many applications, some of which can be represented better by alternative logic symbols.

EXCLUSIVE-NOR



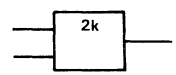
These are five equivalent Exclusive-NOR symbols valid for an 'ALS810 gate in positive logic; negation may be shown at any one port, or at all three of them.

LOGIC IDENTITY ELEMENT



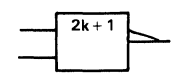
The output is active (High) if all inputs stand at the same logic level (i.e., A = B).

EVEN-PARITY



The output is active (High) if an even number of inputs (i.e., 0 or 2) are active.

ODD-PARITY ELEMENT



The output is active (Low) if an odd number of inputs (i.e., only 1 of the 2) are active.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS810 . . . . . −55°C to 125°C
SN74ALS810 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS810			SN74ALS810			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS810			SN74ALS810			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V,	A at 4.5 V, B at 0 V		5	7.5		5	7.5	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS810		SN74ALS810		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	5	23	5	20	ns
t_{PHL}	(other input low)		3	17	3	14	
t_{PLH}	A or B	Y	5	21	5	18	ns
t_{PHL}	(other input high)		3	17	3	14	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS810 . . . . . −55°C to 125°C
SN74AS810 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS810			SN74AS810			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS810			SN74AS810			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V			18			18		mA
I_{CCL}	V_{CC} = 5.5 V			15			15		mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			SN54AS810			SN74AS810			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A or B	Y		3.4			3.4		ns
t_{PHL}	(other input low)			5.3			5.3		
t_{PLH}	A or B	Y		3.4			3.4		ns
t_{PHL}	(other input high)			5.3			5.3		

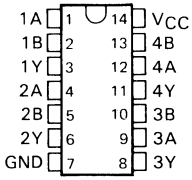
†All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

ALS and AS Circuits

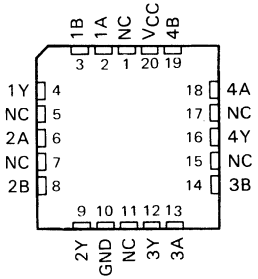
D2837, MARCH 1984—REVISED MAY 1986

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS811, SN54AS811 . . . J PACKAGE
SN74ALS811, SN74AS811 . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS811, SN54AS811 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

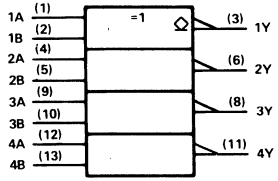
description

These devices contain four independent Exclusive-NOR gates with open-collector outputs. They perform the Boolean functions $Y = \overline{A \oplus B} = (A + \overline{B}) \cdot (\overline{A} + B)$ in positive logic.

A common application is a true/complement element. If one of the inputs is high, the other input will be reproduced in true form at the output. If one of the inputs is low, the signal on the other input will be reproduced inverted at the output.

The SN54ALS811 and SN54AS811 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS811 and SN74AS811 are characterized for operation from 0°C to 70°C.

logic symbol†



FUNCTION TABLE
(each gate)

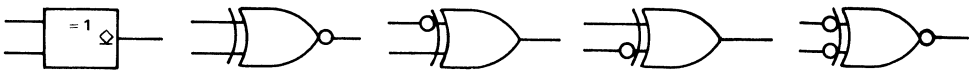
INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H

†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

exclusive-NOR logic

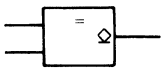
An exclusive-NOR gate has many applications, some of which can be represented better by alternative logic symbols.

EXCLUSIVE-NOR



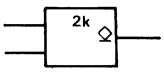
These are five equivalent Exclusive-NOR symbols valid for an 'ALS811 gate in positive logic; negation may be shown at any one port, or at all three of them.

LOGIC IDENTITY ELEMENT



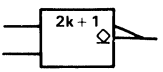
The output is active (high) if all inputs stand at the same logic level (i.e., A = B).

EVEN-PARITY



The output is active (high) if an even number of inputs (i.e., 0 or 2) are active.

ODD-PARITY ELEMENT



The output is active (low) if an odd number of inputs (i.e., only 1 of the 2) are active.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS811 . . . . . −55°C to 125°C
SN74ALS811 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS811			SN74ALS811			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS811			SN74ALS811			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_{CC}	V_{CC} = 5.5 V,	A at 4.5 V, B at 0 V		5	7.5		5	7.5	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 2 kΩ, T_A = MIN to MAX				UNIT
			SN54ALS811		SN74ALS811		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	25	60	25	55	ns
t_{PHL}	(other input low)		5	30	5	28	
t_{PLH}	A or B	Y	20	55	20	50	ns
t_{PHL}	(other input high)		5	28	5	23	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54AS811 . . . . . −55°C to 125°C
SN74AS811 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS811			SN74AS811			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS811			SN74AS811			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = 4.5 V	V_{OH} = 5.5 V			2			2	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_{CCH}	V_{CC} = 5.5 V			18			18		mA
I_{CCL}	V_{CC} = 5.5 V			15			15		mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, RL = 2 kΩ, T_A = MIN to MAX						UNIT
			SN54AS811			SN74AS811			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A or B	Y		10.0			10.0		ns
t_{PHL}	(other input low)			5.7			5.7		
t_{PLH}	A or B	Y		10.0			10.0		ns
t_{PHL}	(other input high)			5.7			5.7		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2825, DECEMBER 1983—REVISED JANUARY 1986

- **Functionally Equivalent to AMD's AM29821 and AM29822**
- **Provides Extra Data Width Necessary for Wider Address/Data Paths or Buses with Parity**
- **Outputs Have Undershoot Protection Circuitry**
- **Power-Up High-Impedance State**
- **Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Buffered Control Inputs to Reduce DC Loading Effects**
- **Dependable Texas Instruments Quality and Reliability**

description

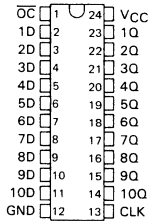
These 10-bit flip-flops feature three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

The ten flip-flops are edge-triggered D-type flip-flops. On the positive transition of the clock the Q outputs on the 'AS821 will be true, and on the 'AS822 will be complementary to the data input.

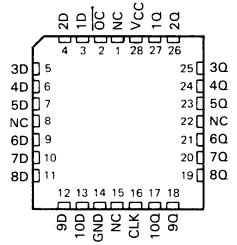
A buffered output-control input can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output control ($\overline{OC}$) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54AS' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS' family is characterized for operation from 0°C to 70°C.

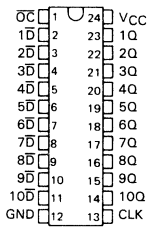
SN54AS821 . . . JT PACKAGE
SN74AS821 . . . DW OR NT PACKAGE
(TOP VIEW)



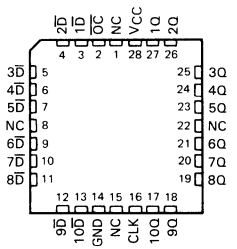
SN54AS821 . . . FK PACKAGE
SN74AS821 . . . FN PACKAGE
(TOP VIEW)



SN54AS822 . . . JT PACKAGE
SN74AS822 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54AS822 . . . FK PACKAGE
SN74AS822 . . . FN PACKAGE
(TOP VIEW)

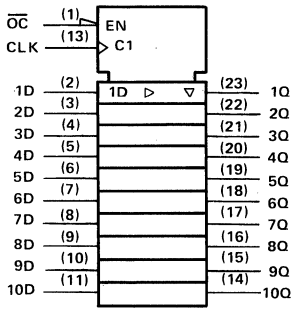


NC—No internal connection

'AS821 FUNCTION TABLE (EACH FLIP-FLOP)

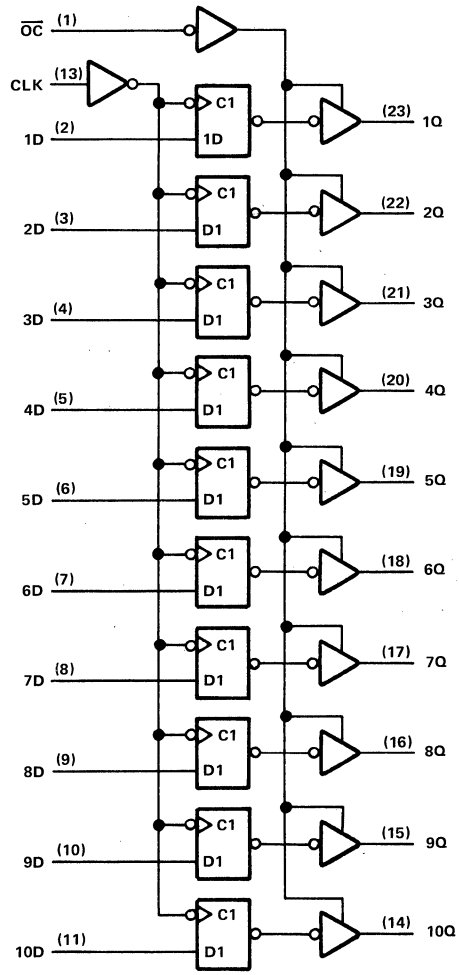
INPUTS			OUTPUT
$\overline{OC}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

'AS821 logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

'AS821 logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

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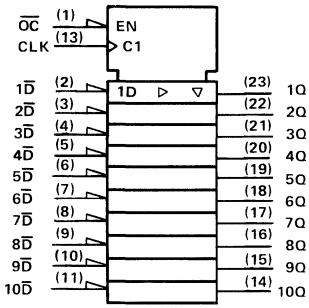
'AS822 FUNCTION TABLE (EACH FLIP-FLOP)

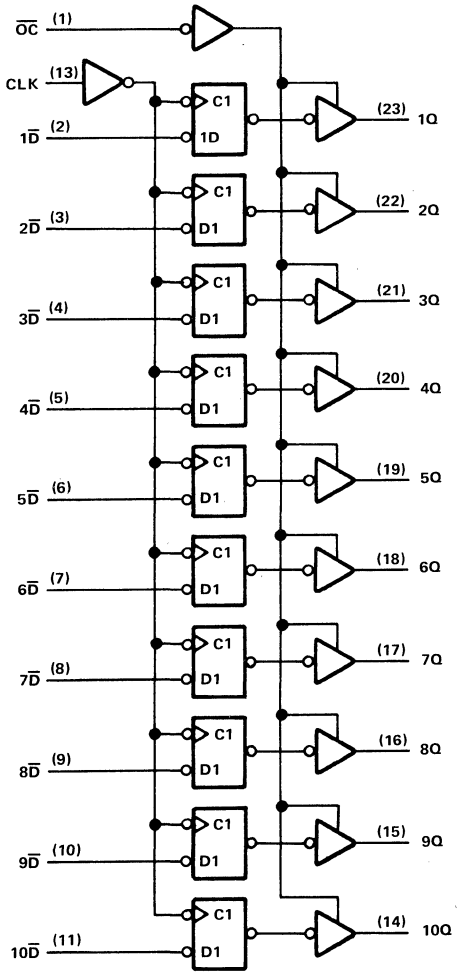
INPUTS			OUTPUT
$\overline{OC}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

'AS822 logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

'AS822 logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54AS821, SN54AS822 . . . . . −55°C to 125°C
SN74AS821, SN74AS822 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS821 SN54AS822			SN74AS821 SN74AS822			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−24			−24	mA
I_{OL}	Low-level output currrent			32			48	mA
t_w	Pulse duration, CLK high or low	9			8			ns
t_{su}	Setup time, data before CLK↑	7			6			ns
t_h	Hold time, data after CLK↑	0			0			ns
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS821 SN54AS822			SN74AS821 SN74AS822			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −15 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −24 mA	2			2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'AS821	V_{CC} = 5.5 V	Outputs high		55	88		55	88	mA
			Outputs low		68	109		68	109	
			Outputs disabled		70	113		70	113	
	'AS822		Outputs high		55	88		55	88	
			Outputs low		68	109		68	109	
			Outputs disabled		70	113		70	113	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

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switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS821 SN54AS822		SN74AS821 SN74AS822		
			MIN	MAX	MIN	MAX	
t_{PLH}	CLK	Any Q	3.5	9	3.5	7.5	ns
t_{PHL}			3.5	11.5	3.5	10.5	
t_{PZH}	$\overline{OC}$	Any Q	4	12	4	11	ns
t_{PZL}			4	13	4	12	
t_{PHZ}	$\overline{OC}$	Any Q	2	10	2	8	ns
t_{PZL}			2	10	2	8	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

9-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

D2825, JUNE 1984—REVISED JANUARY 1986

- **Functionally Equivalent to AMD's AM29823 and AM29824**
- **Provides Extra Data Width Necessary for Wider Address/Data Paths or Buses with Parity**
- **Outputs Have Undershoot Protection Circuitry**
- **Power-Up High-Impedance State**
- **Buffered Control Inputs to Reduce DC Loading Effects**
- **Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

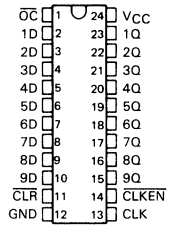
description

These 9-bit flip-flops feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers, parity bus interfacing and working registers.

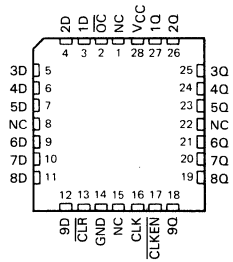
With the clock enable ($\overline{CLKEN}$) low, the nine D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock. Taking $\overline{CLKEN}$ high will disable the clock buffer, thus latching the outputs. The 'AS823 has noninverting D inputs and the 'AS824 has inverting D inputs. Taking the $\overline{CLR}$ input low causes the nine Q outputs to go low independently of the clock.

A buffered output-control input ($\overline{OC}$)can be used to place the nine outputs in either normal logic state (high or low level) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

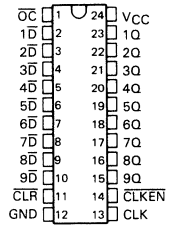
SN54AS823 . . . JT PACKAGE
SN74AS823 . . . DW OR NT PACKAGE
(TOP VIEW)



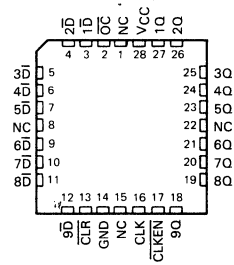
SN54AS823 . . . FK PACKAGE
SN74AS823 . . . FN PACKAGE
(TOP VIEW)



SN54AS824 . . . JT PACKAGE
SN74AS824 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54AS824 . . . FK PACKAGE
SN74AS824 . . . FN PACKAGE
(TOP VIEW)

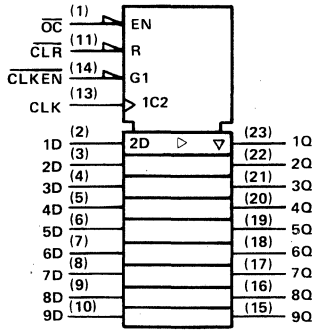


The SN54AS' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS' family is characterized for operation from 0°C to 70°C.

'AS823 FUNCTION TABLE

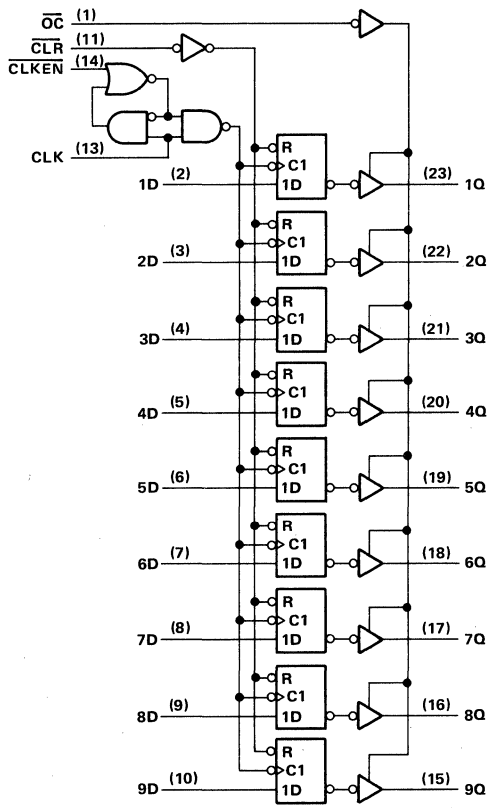
INPUTS					OUTPUT
$\overline{OC}$	$\overline{CLR}$	$\overline{CLKEN}$	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	H	X	X	Q_0
H	X	X	X	X	Z

'AS823 logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12
Pin numbers shown are for DW, JT, and NT packages.

'AS823 logic diagram (positive logic)



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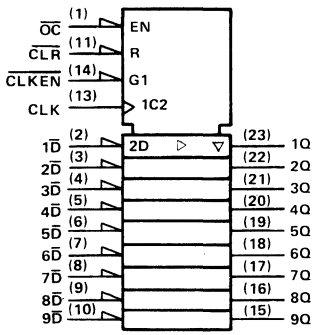
'AS824 FUNCTION TABLE

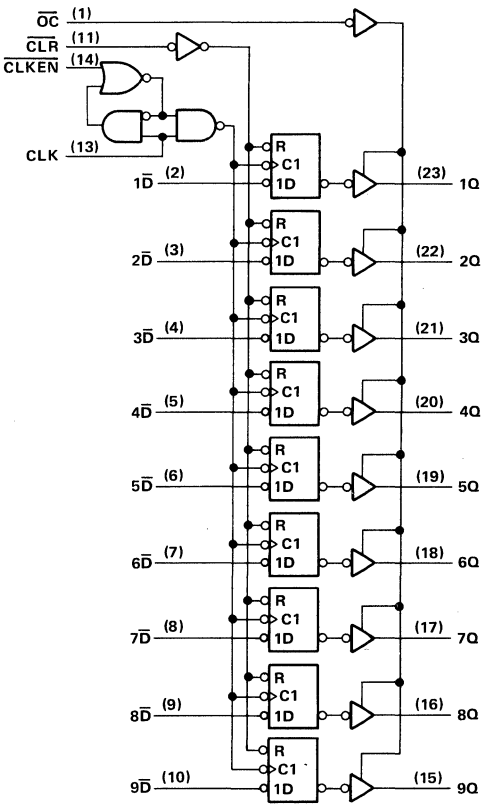
INPUTS					OUTPUT
$\overline{OC}$	$\overline{CLR}$	$\overline{CLKEN}$	CLK	$\overline{D}$	Q
L	L	X	X	X	L
L	H	L	↑	H	L
L	H	L	↑	L	H
L	H	H	X	X	Q_0
H	X	X	X	X	Z

'AS824 logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

'AS824 logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54AS823, SN54AS824 . . . . . −55°C to 125°C
SN74AS823, SN74AS824 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54AS823 SN54AS824			SN74AS823 SN74AS824			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−24			−24	mA
I_{OL}	Low-level output current				32			48	mA
t_w	Pulse duration	$\overline{CLR}$ low	5			4			ns
		CLK high or low	9			8			
t_{su}	Setup time before CLK↑	$\overline{CLR}$ inactive	8			8			ns
		Data	7			6			
		$\overline{CLKEN}$ high or low	7			6			
t_h	Hold time, $\overline{CLKEN}$ or data after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS823 SN54AS824			SN74AS823 SN74AS824			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −15 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −24 mA	2			2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.3	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'AS823	V_{CC} = 5.5 V	Outputs high		49	80		49	80	mA
			Outputs low		61	100		61	100	
			Outputs disabled		64	103		64	103	
	'AS824	V_{CC} = 5.5 V	Outputs high		49	80		49	80	mA
			Outputs low		61	100		61	100	
			Outputs disabled		64	103		64	103	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

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switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS823 SN54AS824		SN74AS823 SN74AS824		
			MIN	MAX	MIN	MAX	
t_{PLH}	CLK	Any Q	3.5	9	3.5	7.5	ns
t_{PHL}			3.5	12	3.5	11	
t_{PHL}	$\overline{CLR}$	Any Q	3.5	14	3.5	13	ns
t_{PZH}	$\overline{OC}$	Any Q	4	12	4	11	ns
t_{PZL}			4	13	4	12	
t_{PHZ}	$\overline{OC}$	Any Q	2	10	2	8	ns
t_{PLZ}			2	10	2	8	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

8-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

D2825, JUNE 1984—REVISED JANUARY 1986

- **Functionally Equivalent to AMD's AM29825 and AM29826**
- **Improved I_{OH} Specifications**
- **Multiple Output Enables Allow Multiuser Control of the Interface**
- **Outputs Have Undershoot Protection Circuitry**
- **Power-Up High-Impedance State**
- **Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Buffered Control Inputs to Reduce DC Loading Effect**
- **Dependable Texas Instruments Quality and Reliability**

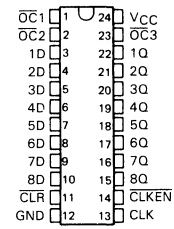
description

These 8-bit flip-flops feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing multiuser registers, I/O ports, bidirectional bus drivers, and working registers.

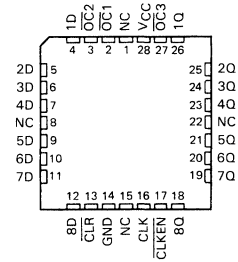
With the clock enable ($\overline{CLKEN}$) low, the eight D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock. Taking $\overline{CLKEN}$ high will disable the clock buffer, thus latching the outputs. The 'AS825 has non-inverting D inputs and the 'AS826 has inverting $\overline{D}$ inputs. Taking the $\overline{CLR}$ input low causes the eight Q outputs to go low independently of the clock.

Multiuser buffered output-control inputs ($\overline{OC}1$, $\overline{OC}2$, and $\overline{OC}3$) can be used to place the eight outputs in either a normal logic state (high or low level) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output controls do not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

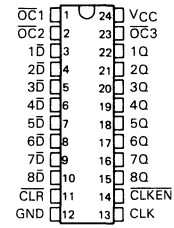
SN54AS825 . . . JT PACKAGE
SN74AS825 . . . DW OR NT PACKAGE
(TOP VIEW)



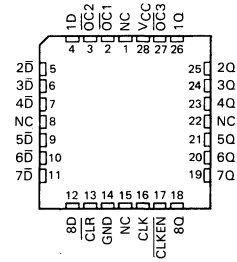
SN54AS825 . . . FK PACKAGE
SN74AS825 . . . FN PACKAGE
(TOP VIEW)



SN54AS826 . . . JT PACKAGE
SN74AS826 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54AS826 . . . FK PACKAGE
SN74AS826 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

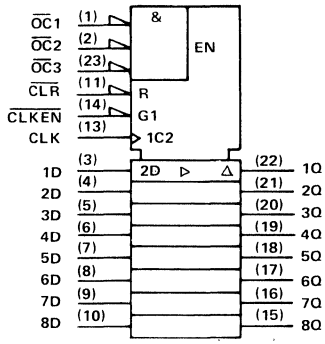
The SN54AS' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS' family is characterized for operation from 0°C to 70°C.

'AS825 FUNCTION TABLE

INPUTS					OUTPUT
$\overline{OC}$*	$\overline{CLR}$	$\overline{CLKEN}$	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	H	X	X	Q_0
H	X	X	X	X	Z

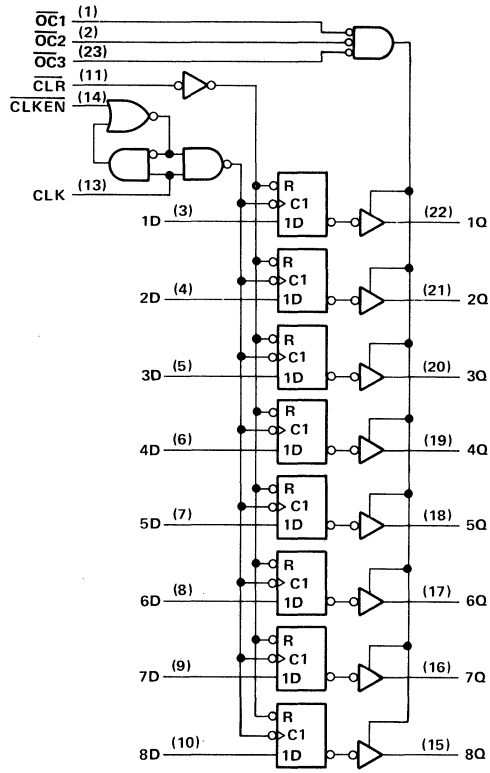
$\overline{OC}$* = H if any of $\overline{OC}$1, $\overline{OC}$2, or $\overline{OC}$3 are high.
$\overline{OC}$* = L if all of $\overline{OC}$1, $\overline{OC}$2, and $\overline{OC}$3 are low.

'AS825 logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

'AS825 logic diagram (positive logic)



Pin numbers are for DW, JT, and NT packages.

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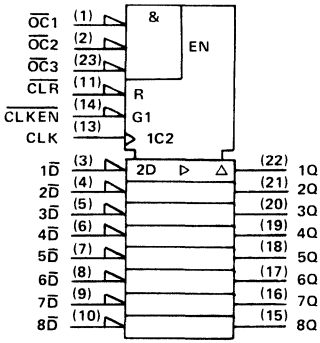
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

'AS826 FUNCTION TABLE

INPUTS					OUTPUT
$\overline{OC}$*	$\overline{CLR}$	$\overline{CLKEN}$	CLK	$\overline{D}$	Q
L	L	X	X	X	L
L	H	L	↑	H	L
L	H	L	↑	L	H
L	H	H	X	X	Q_0
H	X	X	X	X	Z

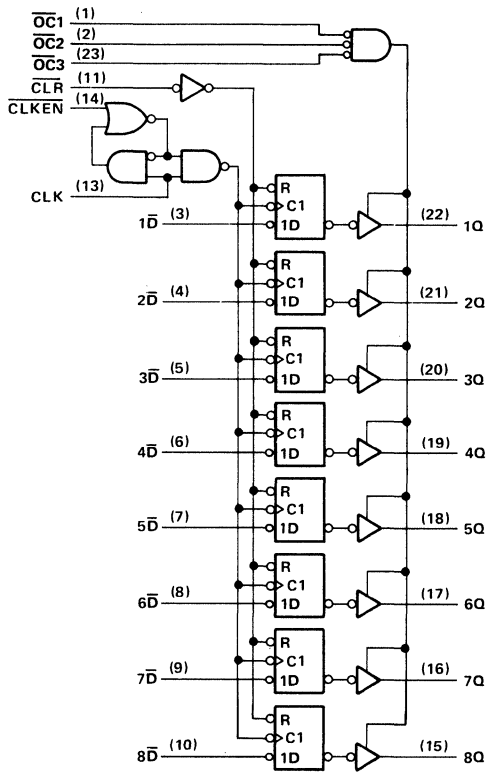
$\overline{OC}$* = H if any of $\overline{OC}$1, $\overline{OC}$2, or $\overline{OC}$3 are high.
$\overline{OC}$* = L if all of $\overline{OC}$1, $\overline{OC}$2, and $\overline{OC}$3 are low.

'AS826 logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12

'AS826 logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range:
SN54AS825, SN54AS826 . . . . . −55°C to 125°C
SN74AS825, SN74AS826 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65 to 150°C

recommended operating conditions

			SN54AS825 SN54AS826			SN74AS825 SN74AS826			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−24			−24	mA
I_{OL}	Low-level output current				32			48	mA
t_w	Pulse duration	$\overline{CLR}$ low	5			4			ns
		CLK high or low	9			8			
t_{su}	Setup time before CLK↑	$\overline{CLR}$ inactive	8			8			ns
		Data	7			6			
		$\overline{CLKEN}$ high or low	7			6			
t_h	Hold time, $\overline{CLKEN}$ or data after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS825 SN54AS826			SN74AS825 SN74AS826			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −15 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −24 mA	2			2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.3	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'AS825	V_{CC} = 5.5 V	Outputs high		45	73		45	73	mA
			Outputs low		56	90		56	90	
			Outputs disabled		59	95		59	95	
	'AS826	V_{CC} = 5.5 V	Outputs high		45	73		45	73	mA
			Outputs low		56	90		56	90	
			Outputs disabled		59	95		59	95	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

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switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS825 SN54AS826		SN74AS825 SN74AS826		
			MIN	MAX	MIN	MAX	
t_{PLH}	CLK	Any Q	3.5	9	3.5	7.5	ns
t_{PHL}			3.5	11.5	3.5	11	
t_{PHL}	$\overline{CLR}$	Any Q	3.5	14	3.5	13	ns
t_{PZH}	$\overline{OC}$	Any Q	4	12	4	11	ns
t_{PZL}			4	13	4	12	
t_{PHZ}	$\overline{OC}$	Any Q	2	10	2	8	ns
t_{PLZ}			2	10	2	8	

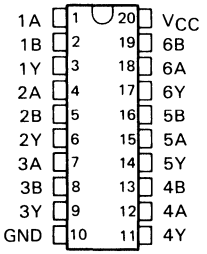
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54ALS832A, SN54AS832B, SN74ALS832A, SN74AS832B
HEX 2-INPUT OR DRIVERS

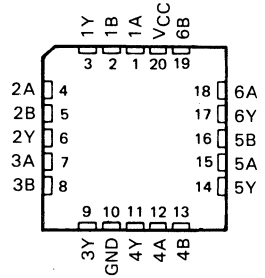
D2661, DECEMBER 1982 – REVISED MAY 1986

- **High Capacitive Drive Capability**
- **'ALS832A has Typical Delay Time of 4.8 ns (C_L = 50 pF) and Typical Power Dissipation of 4.5 mW per Gate**
- **'AS832B has Typical Delay Time of 3.2 ns (C_L = 50 pF) and Typical Power Dissipation of Less than 13 mW per Gate**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS832A, SN54AS832B . . . J PACKAGE
SN74ALS832A, SN74AS832B . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS832A, SN54AS832B . . . FK PACKAGE
(TOP VIEW)



description

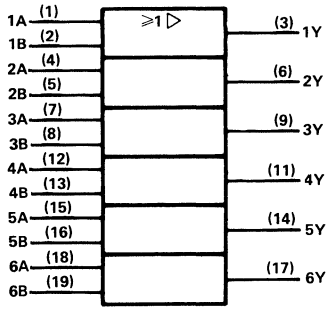
These devices contain six independent 2-input OR drivers. They perform the Boolean functions $Y = A + B$ or $Y = \overline{A \cdot B}$ in positive logic.

The SN54ALS832A and SN54AS832B are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS832A and SN74AS832B are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each driver)

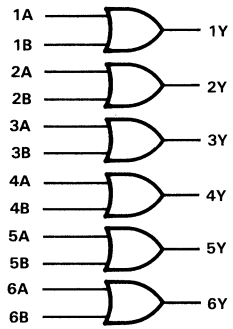
INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS832A . . . . . −55°C to 125°C
SN74ALS832A . . . . . °C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS832A			SN74ALS832A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS832A			SN74ALS832A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		6	9		6	9	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		9.5	16		9.5	16	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX			UNIT
			'ALS832A	SN54ALS832A		SN74ALS832A	
			TYP	MIN	MAX	MIN	MAX
t_{PLH}	A or B	Y	6	2	11	2	9	ns
t_{PHL}			4	1	10	1	8	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS832B . . . . . −55°C to 125°C
SN74AS832B . . . . . °C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS832B			SN74AS832B			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−40			−48	mA
I_{OL}	Low-level output current			40			48	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS832B			SN74AS832B			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −40 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −48 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 40 mA		0.25	0.5				V
	V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−50		−200	−50		−200	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		11	17		11	17	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		22	36		22	36	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS832B		SN74AS832B		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1	7	1	6.3	ns
t_{PHL}			1	7	1	6.3	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

10-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

D2910, DECEMBER 1983 – REVISED MAY 1986

- **3-State Buffer-Type Outputs Drive Bus-Lines Directly**
- **Bus-Structured Pinout**
- **Provide Extra Bus Driving Latches Necessary for Wider Address/Data Paths or Buses with Parity**
- **Buffered Control Inputs to Reduce DC Loading**
- **Power-Up High-Impedance State**
- **Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These 10-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

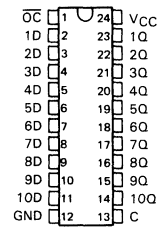
The ten latches are transparent D-type. The 'ALS841 and 'AS841 have noninverting data (D) inputs. The 'ALS842 and 'AS842 have inverting $\overline{D}$ inputs.

A buffered output control ($\overline{OC}$) input can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

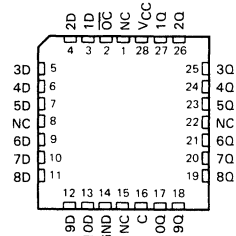
The output control does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are off.

The -1 versions of the SN74ALS841 and SN74ALS842 parts are identical to the standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes. There are no -1 versions of the SN54ALS841 and SN54ALS842.

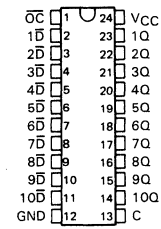
SN54ALS841, SN54AS841 . . . JT PACKAGE
SN74ALS841, SN74AS841 . . . DW OR NT PACKAGE
(TOP VIEW)



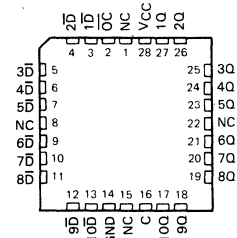
SN54ALS841, SN54AS841 . . . FK PACKAGE
SN74ALS841, SN74AS841 . . . FN PACKAGE
(TOP VIEW)



SN54ALS842, SN54AS842 . . . JT PACKAGE
SN74ALS842, SN74AS842 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54ALS842, SN54AS842 . . . FK PACKAGE
SN74ALS842, SN74AS842 . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

The SN54ALS841, SN54AS841, SN54ALS842, and SN54AS842 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS841, SN74AS841, SN74ALS842, and SN74AS842 are characterized for operation from 0°C to 70°C.

FUNCTION TABLES

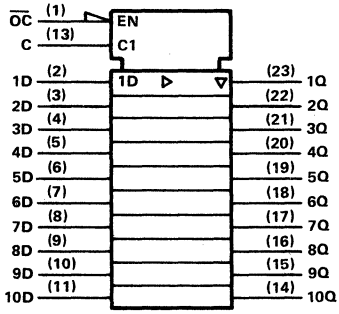
'ALS841, 'AS841

INPUTS			OUTPUT
$\overline{OC}$	C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

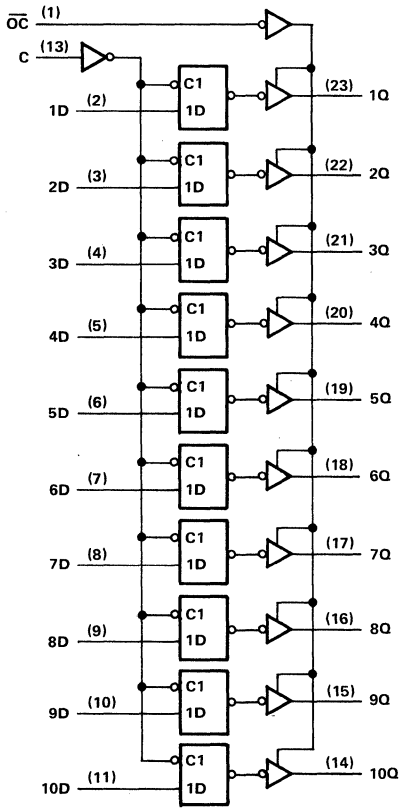
'ALS842, 'AS842

INPUTS			OUTPUT
$\overline{OC}$	C	$\overline{D}$	Q
L	H	H	L
L	H	L	H
L	L	X	Q_0
H	X	X	Z

'ALS841, 'AS841 logic symbol†



'ALS841, 'AS841 logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, and NT packages.

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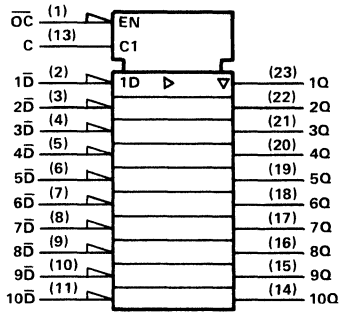
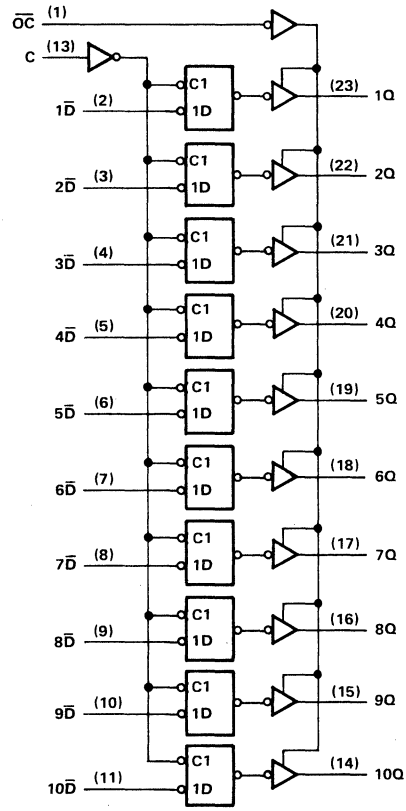
'ALS842, 'AS842 logic symbol†



'ALS842, 'AS842 logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range:
SN54ALS841, SN54AS841, SN54ALS842, SN54AS842 . . . . . −55°C to 125°C
SN74ALS841, SN74AS841, SN74ALS842, SN74AS842 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS841			SN74ALS841			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
							48†	
t_w	Pulse duration, enable C high	25			20			ns
t_{su}	Setup time, data before enable C↓	16			10			ns
t_h	Hold time, data after enable C↓	7			5			ns
T_A	Operating free-air temperature	−55		125	0		70	°C

†The 48-mA limit applies only to the -1 versions and only if V_{CC} is maintained between 4.75 V and 5.25 V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS841			SN74ALS841			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
	V_{CC} = 4.75 V,	I_{OL} = 48 mA (−1 versions)					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		19	30		19	30	mA
		Outputs low		38	62		38	62	
		Outputs disabled		23	40		23	40	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

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'ALS841 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54/74ALS841			SN54ALS841			SN74ALS841			
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	D	Q		8.5	11	2		15	2		13	ns
t_{PHL}				8.5	11	2		15	2		13	
t_{PLH}	C	Q		14	18	7		25	7		21	ns
t_{PHL}				17	23	8		30	8		26	
t_{PZH}	$\overline{OC}$	Q		7.5	10	2		14	2		12	ns
t_{PZL}				7.5	10	2		14	2		12	
t_{PHZ}	$\overline{OC}$	Q		6	8	2		12	2		10	ns
t_{PLZ}				7	9	2		14	2		12	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

recommended operating conditions

		SN54ALS842			SN74ALS842			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
							48†	
t_w	Pulse duration, enable C high	25			20			ns
t_{su}	Setup time, data before enable C↓	16			10			ns
t_h	Hold time, data after enable C↓	7			5			ns
T_A	Operating free-air temperature	−55		125	0		70	°C

†The 48-mA limit applies only to the -1 versions and only if V_{CC} is maintained between 4.75 V and 5.25 V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS842			SN74ALS842			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
	V_{CC} = 4.75 V,	I_{OL} = 48 mA (−1 versions)					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		20	35		20	35	mA
		Outputs low		48	74		48	74	
		Outputs disabled		27	44		27	44	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

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'ALS842 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS842			SN54ALS842		SN74ALS842		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	$\overline{D}$	Q		11	15	4	22	4	18	ns
t_{PHL}				8	11	3	17	3	13	
t_{PLH}	C	Q		17	23	8	31	8	27	ns
t_{PHL}				13	18	6	24	6	20	
t_{PZH}	$\overline{OC}$	Q		8	10	2	14	2	12	ns
t_{PZL}				8	11	2	14	2	12	
t_{PHZ}	$\overline{OC}$	Q		6	8	1	12	1	10	ns
t_{PLZ}				7	9	2	14	2	12	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

recommended operating conditions

		SN54AS841 SN54AS842			SN74AS841 SN74AS842			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−24			−24	mA
I_{OL}	Low-level output current			32			48	mA
t_w	Pulse duration, enable C high	5			4			ns
t_{su}	Setup time, data before enable C↓	3.5			2.5			ns
t_h	Hold time, data after enable C↓	3.5			2.5			ns
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS841 SN54AS842			SN74AS841 SN74AS842			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC} − 2			V_{CC} − 2			V
		V_{CC} = 4.5 V,	I_{OH} = −15 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −24 mA	2			2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'AS841	V_{CC} = 5.5 V	Outputs high		36	60		36	60	mA
			Outputs low		58	94		58	94	
			Outputs disabled		56	92		56	92	
	'AS842		Outputs high		38	62		38	62	
			Outputs low		60	97		60	97	
			Outputs disabled		58	95		58	95	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'AS841 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS841		SN74AS841		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	1	8.5	1	6.5	ns
t_{PHL}			1	10	1	9	
t_{PLH}	C	Q	2	13	2	12	ns
t_{PHL}			2	13	2	12	
t_{PZH}	$\overline{OC}$	Q	2	13.5	2	10.5	ns
t_{PZL}			2	15	2	13.5	
t_{PHZ}	$\overline{OC}$	Q	1	10	1	8	ns
t_{PLZ}			1	10	1	8	

'AS842 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS842		SN74AS842		
			MIN	MAX	MIN	MAX	
t_{PLH}	$\overline{D}$	Q	1	11	1	8.5	ns
t_{PHL}			1	10	1	9	
t_{PLH}	C	Q	2	13	2	12	ns
t_{PHL}			2	13	2	12	
t_{PZH}	$\overline{OC}$	Q	2	14.5	2	12	ns
t_{PZL}			2	15	2	12.5	
t_{PHZ}	$\overline{OC}$	Q	1	10	1	8	ns
t_{PLZ}			1	10	1	8	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

ALS and AS Circuits

9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

D2910, DECEMBER 1983 – REVISED MAY 1986

- **3-State Buffer-Type Outputs Drive Bus-Lines Directly**
- **Bus-Structured Pinout**
- **Provide Extra Bus Driving Latches Necessary for Wider Address/Data Paths or Buses with Parity**
- **Buffered Control Inputs to Reduce DC Loading**
- **Power-Up High Impedance**
- **Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These 9-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

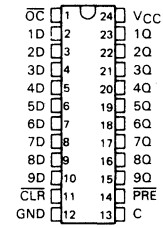
The nine latches are transparent D-type. The 'ALS843 and 'AS843 have noninverting data (D) inputs. The 'ALS844 and 'AS844 have inverting D inputs.

A buffered output control ($\overline{OC}$) input can be used to place the nine outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

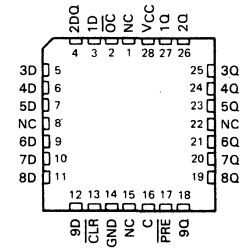
The output control ($\overline{OC}$) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are off.

The -1 versions of the SN74ALS843 and SN74ALS844 parts are identical to the standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes. There are no -1 versions of the SN54ALS843 and SN54ALS844.

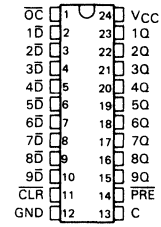
SN54ALS843, SN54AS843 . . . JT PACKAGE
SN74ALS843, SN74AS843 . . . DW OR NT PACKAGE
(TOP VIEW)



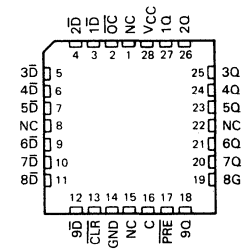
SN54ALS843, SN54AS843. . . FK PACKAGE
SN74ALS843, SN74AS843 . . . FN PACKAGE
(TOP VIEW)



SN54ALS844, SN54AS844 . . . JT PACKAGE
SN74ALS844, SN74AS844 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54ALS844, SN54AS844 . . . FK PACKAGE
SN74ALS844, SN74AS844 . . . FN PACKAGE
(TOP VIEW)



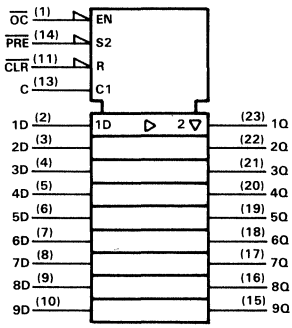
NC – No internal connection

The SN54ALS843, SN54AS843, SN54ALS844, and SN54AS844 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS843, SN74AS843, SN74ALS844, and SN74AS844 are characterized for operation from 0°C to 70°C.

'ALS843, 'AS843 FUNCTION TABLE

INPUTS					OUTPUT
$\overline{PRE}$	$\overline{CLR}$	$\overline{OC}$	C	D	Q
L	X	L	X	X	H
H	L	L	X	X	L
H	H	L	H	L	L
H	H	L	H	H	H
H	H	L	L	X	Q_O
X	X	H	X	X	Z

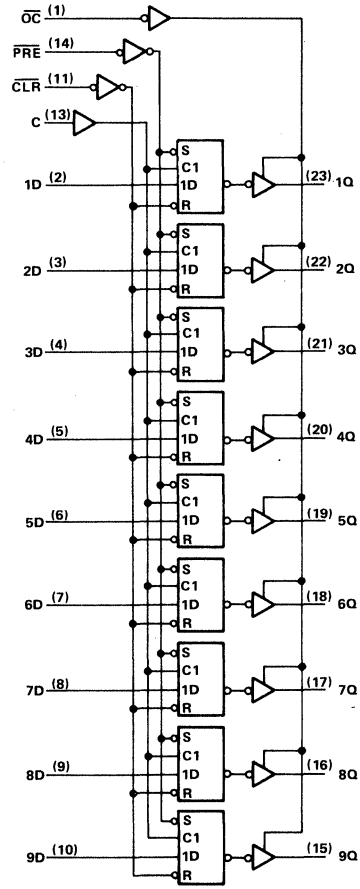
'ALS843, 'AS843 logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, and NT packages.

'ALS843, 'AS843 logic diagram (positive logic)



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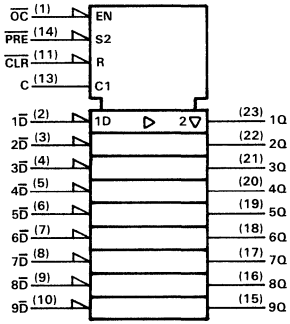
'ALS844, 'AS844 FUNCTION TABLE

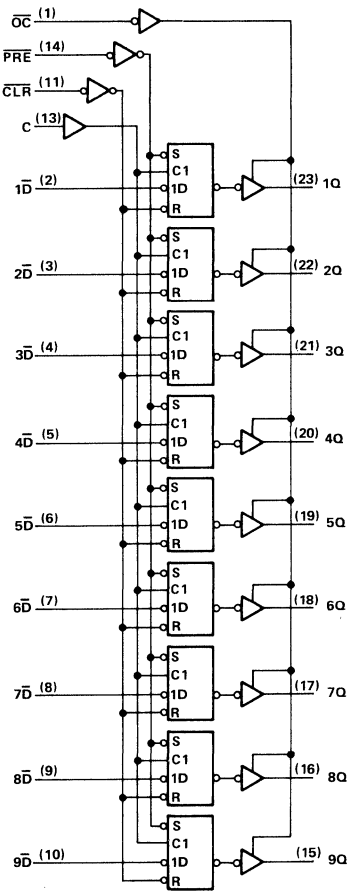
INPUTS					OUTPUT
$\overline{PRE}$	$\overline{CLR}$	$\overline{OC}$	C	$\overline{D}$	Q
L	X	L	X	X	H
H	L	L	X	X	L
H	H	L	H	L	H
H	H	L	H	H	L
H	H	L	L	X	Q_O
X	X	H	X	X	Z

'ALS844, 'AS844 logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

'ALS844, 'AS844 logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS', SN54AS' . . . . . −55°C to 125°C
SN74ALS', SN74AS' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS843 SN54ALS844			SN74ALS843 SN74ALS844			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	55	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0. 7			0.8	V
I_{OH}	High-level output current				−1			−2.6	mA
I_{OL}	Low-level output current				12			24	mA
								48†	
t_w	Pulse duration	$\overline{CLR}$ or $\overline{PRE}$ low	40			35			ns
		C high	25			20			
t_{su}	Setup time, data before enable C↓		16			10			ns
t_h	Hold time, data after enable C↓		7			5			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

†The 48-mA limit applies only to the -1 versions and only if V_{CC} is maintained between 4.75 V and 5.25 V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS843 SN54ALS844			SN74ALS843 SN74ALS844			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	.3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
		V_{CC} = 4.75 V,	I_{OL} = 48 mA (−1 versions)					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS843	V_{CC} = 5.5 V	Outputs high		21	36		21	36	mA
			Outputs low		41	67		41	67	
			Outputs disabled		25	42		25	42	
	'ALS844		Outputs high		21	36		21	36	
			Outputs low		41	72		41	72	
			Outputs disabled		28	48		28	48	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

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'ALS843 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS843			SN54ALS843		SN74ALS843		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q		7	11	2	15	2	13	ns
t_{PHL}				11	15	4	20	4	18	
t_{PLH}	C	Q		12	18	5	25	5	21	ns
t_{PHL}				16	23	8	30	8	26	
t_{PLH}	$\overline{PRE}$	Q		13	19	5	25	5	22	ns
t_{PHL}				19	26	4	35	6	30	
t_{PLH}	$\overline{CLR}$	Q		19	26	4	35	6	30	ns
t_{PHL}				14	21	6	27	6	23	
t_{PZH}	$\overline{OC}$	Q		7	10	2	14	2	12	ns
t_{PZL}				9	12	4	16	4	14	
t_{PHZ}	$\overline{OC}$	Q		6	9	2	12	2	10	ns
t_{PLZ}				7	10	2	14	2	12	

'ALS844 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS844			SN54ALS844		SN74ALS844		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	$\overline{D}$	Q		11	16	4	22	4	20	ns
t_{PHL}				9	13	3	17	3	15	
t_{PLH}	C	Q		17	24	8	32	8	29	ns
t_{PHL}				14	19	6	26	6	22	
t_{PLH}	$\overline{PRE}$	Q		13	19	5	25	5	22	ns
t_{PHL}				19	26	4	35	6	30	
t_{PLH}	$\overline{CLR}$	Q		19	26	4	35	6	30	ns
t_{PHL}				16	23	8	29	8	25	
t_{PZH}	$\overline{OC}$	Q		10	15	2	19	4	17	ns
t_{PZL}				12	18	3	22	5	20	
t_{PHZ}	$\overline{OC}$	Q		7	10	1	12	1	11	ns
t_{PLZ}				5	9	1	14	1	12	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

recommended operating conditions

			SN54AS843 SN54AS844			SN74AS843 SN74AS844			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	55	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−24			−24	mA
I_{OL}	Low-level output current				32			48	mA
t_w	Pulse duration, enable C high	$\overline{CLR}$ or $\overline{PRE}$ low	5			4			ns
		C high	5			4			
t_{su}	Setup time, data before enable C↓		3.5			2.5			ns
t_h	Hold time, data after enable C↓		3.5			2.5			ns
t_r	Recovery time	$\overline{PRE}$	17			15			ns
		$\overline{CLR}$	16			14			
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS843 SN54AS844			SN74AS843 SN74AS844			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −15 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −24 mA	2			2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'AS843	V_{CC} = 5.5 V,	Outputs high		37	62		37	62	mA
			Outputs low		56	92		56	92	
			Outputs disabled		56	92		56	92	
	'AS844		Outputs high		39	64		39	64	
			Outputs low		58	95		58	95	
			Outputs disabled		58	95		58	95	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

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'AS843 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS843		SN74AS843		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	1	8.5	1	6.5	ns
t_{PHL}			1	10	1	9	
t_{PLH}	C	O	2	13	2	12	ns
t_{PHL}			2	13	2	12	
t_{PLH}	$\overline{PRE}$	Q	2	12	2	10	ns
t_{PHL}	$\overline{CLR}$	Q	2	14	2	13	ns
t_{PZH}	$\overline{OC}$	Q	2	13.5	2	10.5	ns
t_{PZL}			2	15	2	13.5	
t_{PHZ}	$\overline{OC}$	Q	1	10	1	8	ns
t_{PLZ}			1	10	1	8	

'AS844 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS844		SN74AS844		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	1	11	1	8.5	ns
t_{PHL}			1	11	1	10	
t_{PLH}	C	O	2	14	2	12.5	ns
t_{PHL}			2	14	2	13	
t_{PLH}	$\overline{PRE}$	Q	2	12	2	10	ns
t_{PHL}	$\overline{CLR}$	Q	2	14.5	2	13.5	ns
t_{PZH}	$\overline{OC}$	Q	2	14.5	2	12	ns
t_{PZL}			2	15	2	13.5	
t_{PHZ}	$\overline{OC}$	Q	1	10	1	8	ns
t_{PLZ}			1	10	1	8	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

8-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

D2825, DECEMBER 1983—REVISED APRIL 1986

- **3-State Buffer-Type Outputs Drive Bus-Lines Directly**
- **Bus-Structured Pinout**
- **Provides Extra Bus Driving Latches Necessary for Wider Address/Data Paths or Buses with Parity**
- **Buffered Control Inputs to Reduce DC Loading**
- **Power-Up High-Impedance State**
- **Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

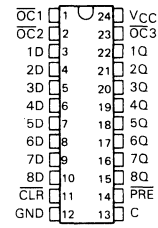
description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

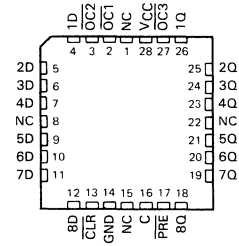
The eight latches are transparent D-type. The 'ALS845 and 'AS845 have noninverting data (D) inputs. The 'ALS846 and 'AS846 have inverting $\overline{D}$ inputs. Since $\overline{CLR}$ and $\overline{PRE}$ are independent of the clock, taking the $\overline{CLR}$ input low will cause the eight Q outputs to go low. Taking the $\overline{PRE}$ input low will cause the eight Q outputs to go high. When both $\overline{PRE}$ and $\overline{CLR}$ are taken low, the outputs will follow the preset condition.

The buffered output control inputs ($\overline{OC}1$, $\overline{OC}2$, and $\overline{OC}3$) can be used to place the eight outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output controls do not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

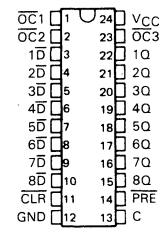
SN54ALS845, SN54AS845 . . . JT PACKAGE
SN74ALS845, SN74AS845 . . . DW OR NT PACKAGE
(TOP VIEW)



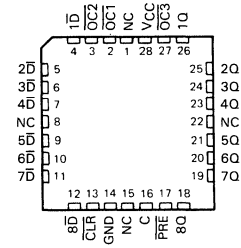
SN54ALS845, SN54AS845 . . . FK PACKAGE
SN74ALS845, SN74AS845 . . . FN PACKAGE
(TOP VIEW)



SN54ALS846, SN54AS846 . . . JT PACKAGE
SN74ALS846, SN74AS846 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54ALS846, SN54AS846 . . . FK PACKAGE
SN74ALS846, SN74AS846 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

The -1 versions of the SN74ALS845 and SN74ALS846 parts are identical to the standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes. There are no -1 versions of the SN54ALS845 and SN54ALS846.

The SN54ALS845, SN54AS845, SN54ALS846, and SN54AS846 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS845, SN74AS845, SN74ALS846, and SN74AS846 are characterized for operation from 0°C to 70°C.

FUNCTION TABLES

'ALS845, 'AS845

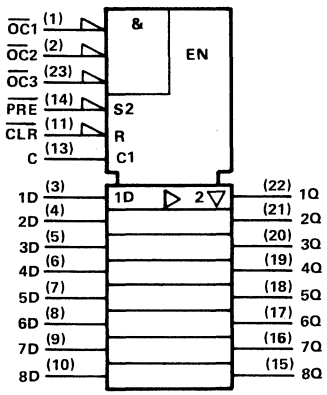
INPUTS							OUTPUT
$\overline{PRE}$	$\overline{CLR}$	$\overline{OC1}$	$\overline{OC2}$	$\overline{OC3}$	C	D	Q
L	H	L	L	L	X	X	H
H	L	L	L	L	X	X	L
L	L	L	L	L	X	X	H
H	H	L	L	L	H	L	L
H	H	L	L	L	H	H	H
H	H	L	L	L	L	X	Q_0
X	X	X	X	H	X	X	Z
X	X	X	H	X	X	X	Z
X	X	H	X	X	X	X	Z

'ALS846, 'AS846

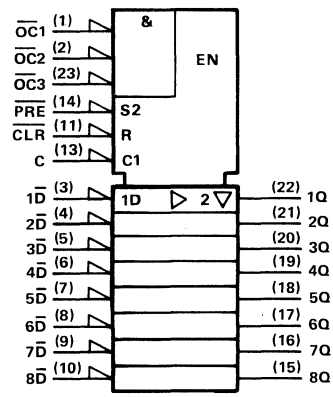
INPUTS							OUTPUT
$\overline{PRE}$	$\overline{CLR}$	$\overline{OC1}$	$\overline{OC2}$	$\overline{OC3}$	C	$\overline{D}$	Q
L	H	L	L	L	X	X	H
H	L	L	L	L	X	X	L
L	L	L	L	L	X	X	H
H	H	L	L	L	H	L	H
H	H	L	L	L	H	H	L
H	H	L	L	L	L	X	Q_0
X	X	X	X	H	X	X	Z
X	X	X	H	X	X	X	Z
X	X	H	X	X	X	X	Z

logic symbols†

'ALS845, 'AS845



'ALS846, 'AS846



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

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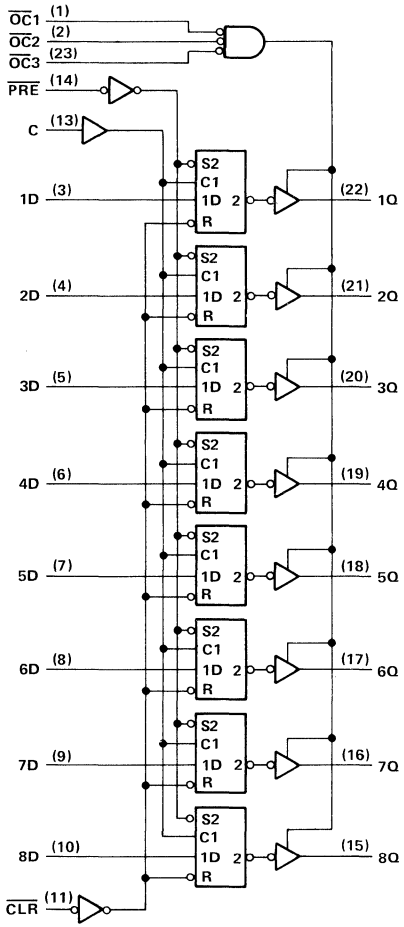
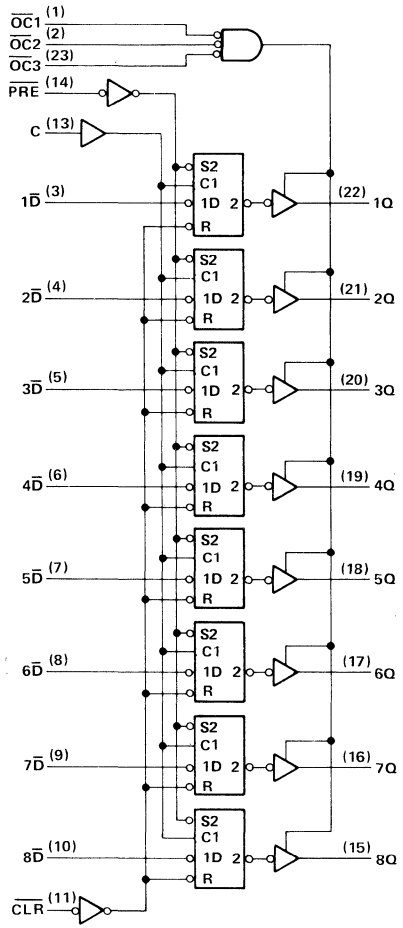
logic diagrams (positive logic)

'ALS845, 'AS845



'ALS846, 'AS846



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range:
SN54ALS845, SN54AS845, SN54ALS846, SN54AS846 . . . . . −55°C to 125°C
SN74ALS845, SN74AS845, SN74ALS846, SN74AS846 . . . . . −0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS845			SN74ALS845			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−1			−2.6	mA
I_{OL}	Low-level output current				12			24	mA
								48†	
t_w	Pulse duration	$\overline{CLR}$ or $\overline{PRE}$ low	40			35			ns
		C high	25			20			
t_{su}	Setup time, data before enable C↓		16			10			ns
t_h	Hold time, data after enable C↓		7			5			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

†The extended limit applies only if V_{CC} is maintained between 4.75 V and 5.25 V. The 48 mA limit applies for SN74ALS845-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS845			SN74ALS845			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V, (I_{OL} = 48 mA for -1 versions)	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		21	36		21	36	mA
		Outputs low		41	67		41	67	
		Outputs disabled		25	42		25	42	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

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switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS845			SN54ALS845		SN74ALS845		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q		7	11	2	15	2	13	ns
t_{PHL}				11	15	4	20	4	18	
t_{PLH}	C	Q		12	18	5	25	5	21	ns
t_{PHL}				16	23	8	30	8	26	
t_{PLH}	$\overline{PRE}$	Q		13	19	5	25	6	22	ns
t_{PHL}				19	26	4	35	6	30	ns
t_{PLH}	$\overline{CLR}$	Q		19	26	4	35	6	30	ns
t_{PHL}				16	22	6	28	6	24	ns
t_{PZH}	$\overline{OC}$	Q		9	14	2	18	3	16	ns
t_{PZL}				12	17	4	20	5	18	
t_{PHZ}	$\overline{OC}$	Q		4	9	1	12	1	11	ns
t_{PLZ}				6	11	2	14	2	12	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

recommended operating conditions

			SN54ALS846			SN74ALS846			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−1			−2.6	mA
I_{OL}	Low-level output current				12			24	mA
								48†	
t_w	Pulse duration	$\overline{CLR}$ or $\overline{PRE}$ low	40			35			ns
		C high	25			20			
t_{su}	Setup time, data before enable C↓		16			10			ns
t_h	Hold time, data after enable C↓		7			5			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

† The extended limit applies only if V_{CC} is maintained between 4.75 V and 5.25 V. The 48 mA limit applies for SN74ALS846-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS846			SN74ALS846			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3,2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4				V
	V_{CC} = 4.5 V, (I_{OL} = 48 mA for -1 versions)	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		22	36		22	36	mA
		Outputs low		43	72		43	72	
		Outputs disabled		28	48		28	48	

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

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switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS846			SN54ALS846		SN74ALS846		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q		11	16	4	22	4	20	ns
t_{PHL}				9	13	3	17	3	15	
t_{PLH}	C	Q		17	23	8	31	8	27	ns
t_{PHL}				14	19	6	26	6	22	
t_{PLH}	$\overline{PRE}$	Q		13	17	5	24	5	20	ns
t_{PHL}				18	24	9	36	9	26	
t_{PLH}	$\overline{CLR}$	Q		14	19	6	23	6	21	ns
t_{PHL}				16	21	9	25	9	23	
t_{PZH}	$\overline{OC}$	Q		10	13	3	17	3	15	ns
t_{PZL}				13	17	5	20	5	18	
t_{PHZ}	$\overline{OC}$	Q		7	10	1	12	1	11	ns
t_{PLZ}				7	11	2	14	2	12	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

recommended operating conditions

			SN54AS845 SN54AS846			SN74AS845 SN74AS846			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−24			−24	mA
I_{OL}	Low-level output current				32			48	mA
t_w	Pulse duration	$\overline{CLR}$ or $\overline{PRE}$ low	5			4			ns
		C high	5			4			
t_{su}	Setup time, data before enable C↓		3.5			2.5			ns
t_h	Hold time, data after enable C↓		3.5			2.5			ns
t_r	Recovery time	$\overline{PRE}$	17			15			ns
		$\overline{CLR}$	16			14			
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS845 SN54AS846			SN74AS845 SN74AS846			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −15 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −24 mA	2			2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'AS845	V_{CC} = 5.5 V	Outputs high		35	58		35	58	mA
			Outputs low		52	85		52	85	
			Outputs disabled		52	85		52	85	
	'AS846		Outputs high		36	59		36	59	
			Outputs low		53	87		53	87	
			Outputs disabled		53	87		53	87	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

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'AS845 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS845		SN74AS845		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	1	8.5	1	6.5	ns
t_{PHL}			1	10	1	9	
t_{PLH}	C	Q	2	13	2	12	ns
t_{PHL}			2	13	2	12	
t_{PLH}	$\overline{PRE}$	Q	2	12	2	10	ns
t_{PHL}	$\overline{CLR}$	Q	2	14	2	13	ns
t_{PHL}	$\overline{OC}$	Q	2	13.5	2	10.5	ns
t_{PZL}			2	15	2	13.5	
t_{PHZ}	$\overline{OC}$	Q	1	10	1	8	ns
t_{PLZ}			1	10	1	8	

'AS846 switching characteristics (see Note 1)

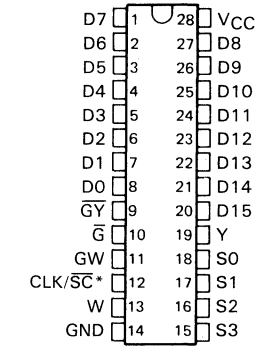
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS846		SN74AS846		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	1	11	1	8.5	ns
t_{PHL}			1	11	1	10	
t_{PLH}	C	Q	2	14	2	12.5	ns
t_{PHL}			2	14	2	13	
t_{PLH}	$\overline{PRE}$	Q	2	12	2	10	ns
t_{PHL}	$\overline{CLR}$	Q	2	14.5	2	13.5	ns
t_{PHL}	$\overline{OC}$	Q	2	14.5	2	12	ns
t_{PZL}			2	15	2	13.5	
t_{PHZ}	$\overline{OC}$	Q	1	10	1	8	ns
t_{PLZ}			1	10	1	8	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

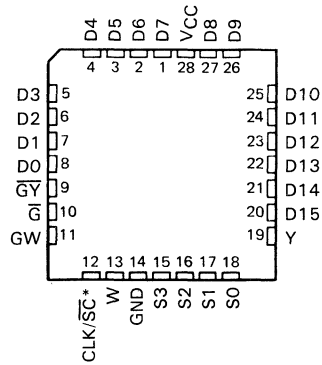
D2822, DECEMBER 1983—REVISED JANUARY 1986

- 4-Line to 1-Line Data Selectors/Multiplexers That Can Select 1 of 16 Data Inputs. Typical Applications:
  - Boolean Function Generators
  - Parallel-to-Serial Converters
  - Data Source Selectors
- Cascadable to n-Bits
- 3-State Bus Driver Outputs
- 'AS850 Offers Clocked Selects; 'AS851 Offers Enable-Controlled Selects
- Has a Master Output Control ($\overline{G}$) for Cascading and Individual Output Controls ($\overline{GY}$, GW) for Each Output
- Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

SN74AS850, SN74AS851 . . . N PACKAGE
(TOP VIEW)



SN74AS850, SN74AS851 . . . FN PACKAGE
(TOP VIEW)



*CLK for 'AS850 or $\overline{SC}$ for 'AS851

description

These four-line to one-line data selectors/multiplexers provide full binary decoding to select one-of-sixteen data sources with complementary Y and W outputs. The 'AS850 has a clock-controlled select register allowing for a symmetrical presentation of the select inputs to the decoder while the 'AS851 has an enable-controlled select register allowing the user to select and hold one particular data line.

A buffered group of output controls ($\overline{G}$, $\overline{GY}$, GW) can be used to place the two-outputs in either a normal logic (high or low logic level) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without the need for interface or pull-up components.

The output controls do not affect the internal operations of the data selector/multiplexer. New data can be setup while the outputs are in the high-impedance state.

The SN74AS850 and SN74AS851 are characterized for operation from 0°C to 70°C.

INPUT SELECTION TABLE

SELECT INPUTS				'AS850	'AS851	INPUT
S3	S2	S1	S0	CLK	$\overline{SC}$	SELECTED
L	L	L	L	↑	L	D0
L	L	L	H	↑	L	D1
L	L	H	L	↑	L	D2
L	L	H	H	↑	L	D3
L	H	L	L	↑	L	D4
L	H	L	H	↑	L	D5
L	H	H	L	↑	L	D6
L	H	H	H	↑	L	D7
H	L	L	L	↑	L	D8
H	L	L	H	↑	L	D9
H	L	H	L	↑	L	D10
H	L	H	H	↑	L	D11
H	H	L	L	↑	L	D12
H	H	L	H	↑	L	D13
H	H	H	L	↑	L	D14
H	H	H	H	↑	L	D15
X	X	X	X	H or L	H	Dn

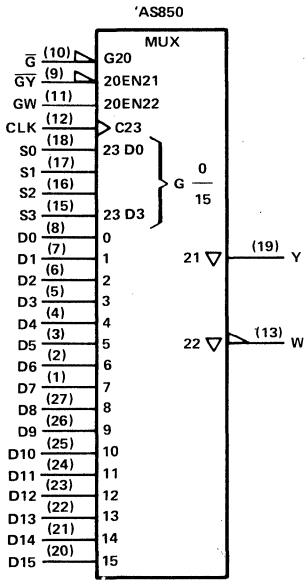
Dn = the input selected before the most-recent low-to-high transition of CLK or $\overline{SC}$.

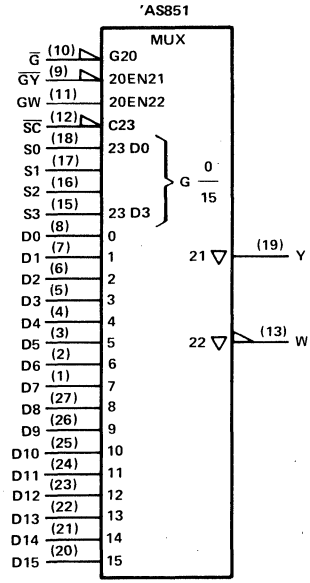
OUTPUT FUNCTION TABLE

$\overline{G}$	$\overline{GY}$	GW	OUTPUTS	
			Y	W
H	X	X	Z	Z
L	H	L	Z	Z
L	L	L	D	Z
L	H	H	Z	$\overline{D}$
L	L	H	D	$\overline{D}$

D = level of selected input D0—D15

logic symbols†





† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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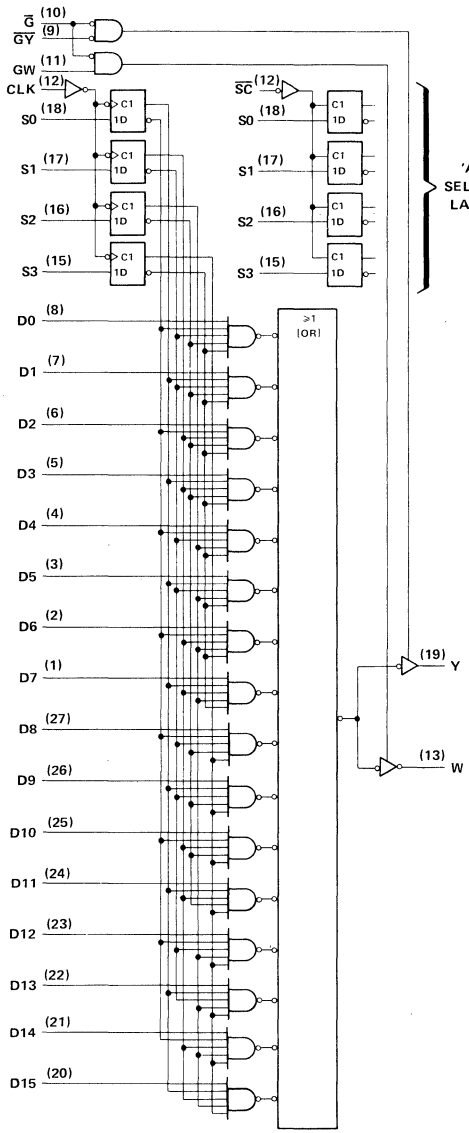
'AS850 logic diagrams (positive logic) (see inset for 'AS851)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

SN74AS850 recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−15	mA
I_{OL}	Low-level output current				48	mA
f_{clock}	Clock frequency		0		60	MHz
t_w	Pulse duration	CLK high	8			ns
		CLK low	8			
t_{su}	Setup time, select inputs before CLK↑		10			ns
t_h	Hold time, select inputs after CLK↑		0			ns
T_A	Operating free-air temperature		0		70	°C

SN74AS850 electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −15 mA	2	3.3		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.35	0.5	V
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}	D, $\overline{G}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−1	mA
	All others					−0.5	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	Outputs active		50	81	mA
			Outputs disabled		52	85	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit current, I_{OS}.

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SN74AS850 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 0°C to 70°C		UNIT
			MIN	MAX	
f_{max}			60		MHz
t_{PLH}	Any D	Y	3	10.5	ns
t_{PHL}			3	11	
t_{PLH}	Any D	W	3	8	ns
t_{PHL}			1	6	
t_{PLH}	CLK	Y	3	14.5	ns
t_{PHL}			3	17.5	
t_{PLH}	CLK	W	3	15	ns
t_{PHL}			3.5	13	
t_{PZH}	$\overline{G}$	Y	2	8	ns
t_{PZL}			3	11	
t_{PHZ}	$\overline{G}$	Y	1	6	ns
t_{PLZ}			2	8	
t_{PZH}	$\overline{G}$	W	2	8	ns
t_{PZL}			3	21	
t_{PHZ}	$\overline{G}$	W	1	6	ns
t_{PLZ}			2	8	
t_{PZH}	$\overline{GY}$	Y	2	8	ns
t_{PZL}			3	11	
t_{PHZ}	$\overline{GY}$	Y	1	6	ns
t_{PLZ}			2	8	
t_{PZH}	GW	W	2	10	ns
t_{PZL}			3	25	
t_{PHZ}	GW	W	1	6	ns
t_{PLZ}			2	11	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN74AS851 recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−15	mA
I_{OL}	Low-level output current			48	mA
t_w	Pulse duration, $\overline{SC}$ low	10			ns
t_{su}	Setup time, select inputs before $\overline{SC}$↑	4.5			ns
t_h	Hold time, select inputs after $\overline{SC}$↑	0			ns
T_A	Operating free-air temperature	0		70	°C

SN74AS851 electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	C
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −15 mA	2	3.3		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.35	0.5	V
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}	D, $\overline{G}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−1	mA
	All others					−0.5	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	Outputs active		50	81	mA
			Outputs disabled		52	85	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit current, I_{OS}.

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SN74AS851 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 0°C to 70°C		UNIT
			MIN	MAX	
t_{PLH}	Any D	Y	3	10.5	ns
t_{PHL}			3	11	
t_{PLH}	Any D	W	3	8	ns
t_{PHL}			1	6	
t_{PLH}	S0, S1, S2, S3	Y	3	18	ns
t_{PHL}			3	19	
t_{PLH}	S0, S1, S2, S3	W	3	16	ns
t_{PHL}			3	15	
t_{PLH}	$\overline{SC}$	Y	3	18	ns
t_{PHL}			3	20	
t_{PLH}	$\overline{SC}$	W	3	16	ns
t_{PHL}			3	15	
t_{PZH}	$\overline{G}$	Y	2	8	ns
t_{PZL}			3	11	
t_{PHZ}	$\overline{G}$	Y	1	6	ns
t_{PLZ}			2	8	
t_{PZH}	$\overline{G}$	W	2	8	ns
t_{PZL}			3	21	
t_{PHZ}	$\overline{G}$	W	1	6	ns
t_{PLZ}			2	8	
t_{PZH}	$\overline{GY}$	Y	2	8	ns
t_{PZL}			3	11	
t_{PHZ}	$\overline{GY}$	Y	1	6	ns
t_{PLL}			2	8	
t_{PZH}	GW	W	2	10	ns
t_{PZL}			3	25	
t_{PHZ}	GW	W	1	6	ns
t_{PLZ}			2	11	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TYPICAL APPLICATION DATA

The 'AS850 or 'AS851 can be used as a 1-of-16 Boolean function generator. Figure 1 shows the 'AS850 in one example.

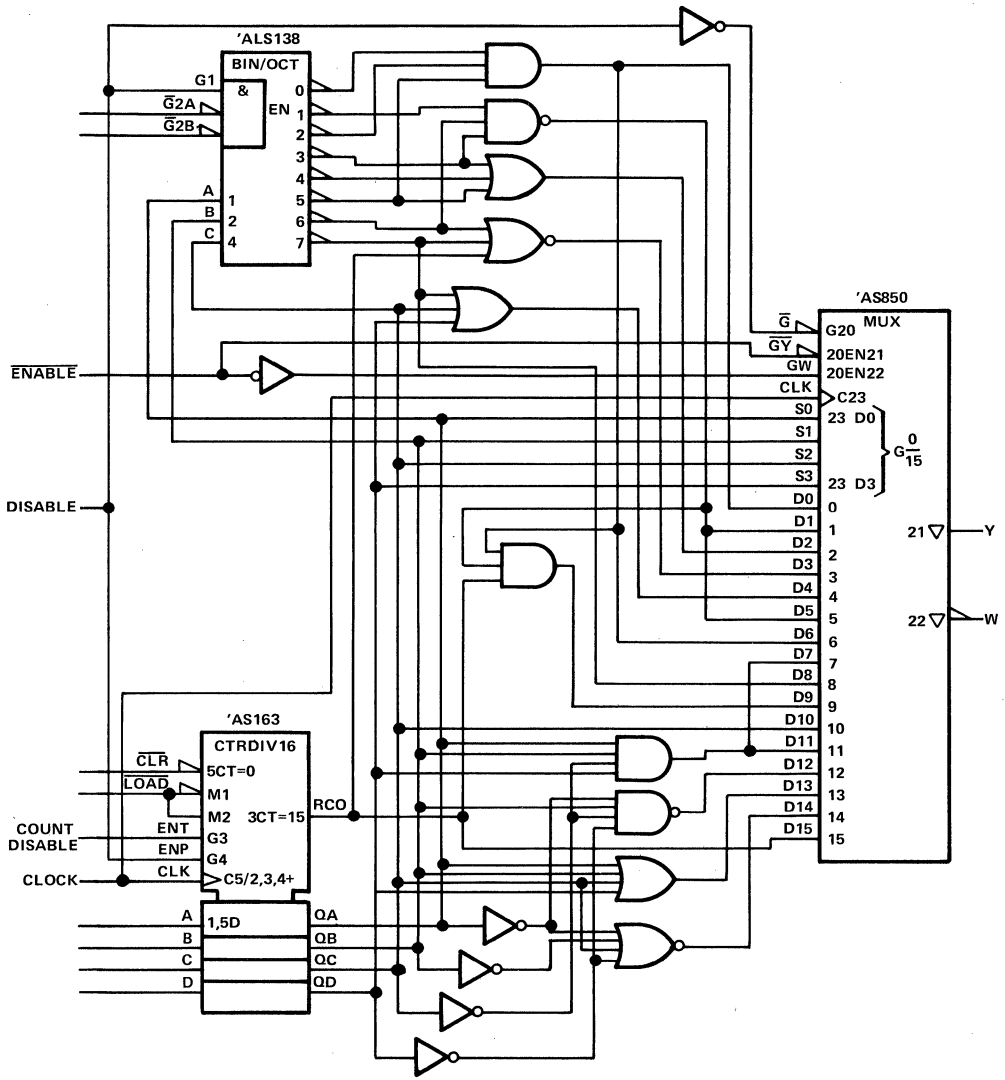

FIGURE 1. 1-of-16 BOOLEAN FUNCTION GENERATOR

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POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

TYPICAL APPLICATION DATA

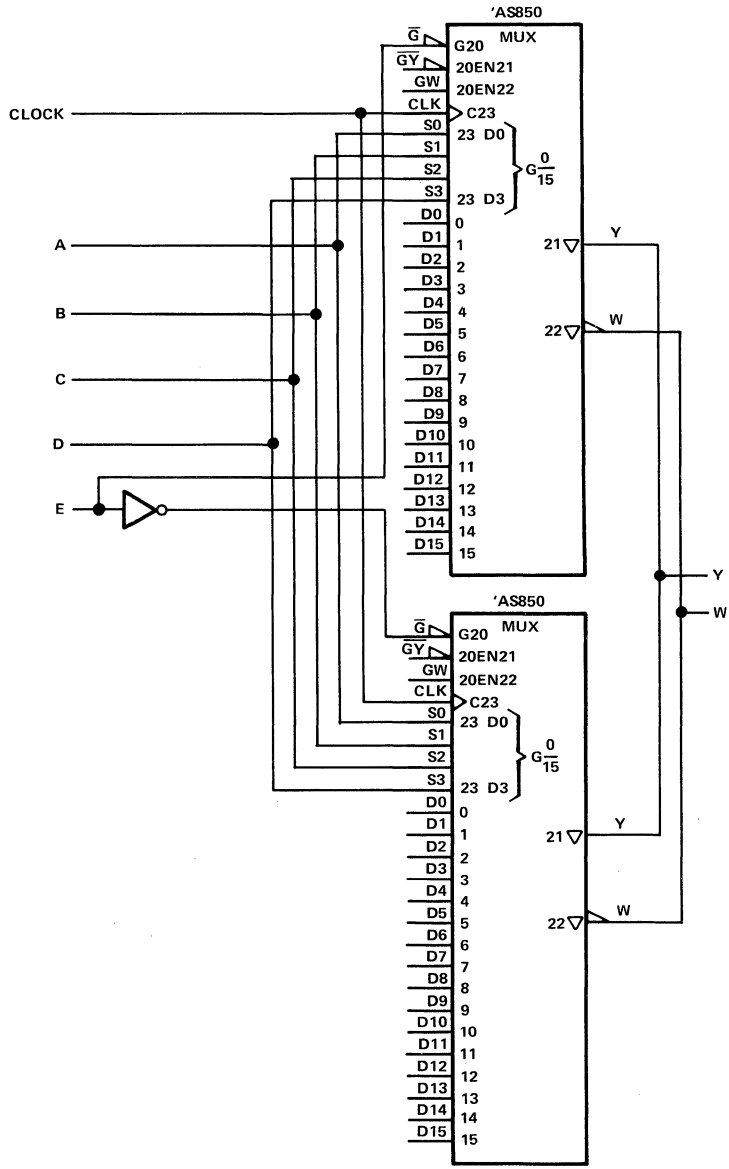


FIGURE 2. 1-of-32 DATA SELECTOR/MULTIPLEXER

TYPICAL APPLICATION DATA

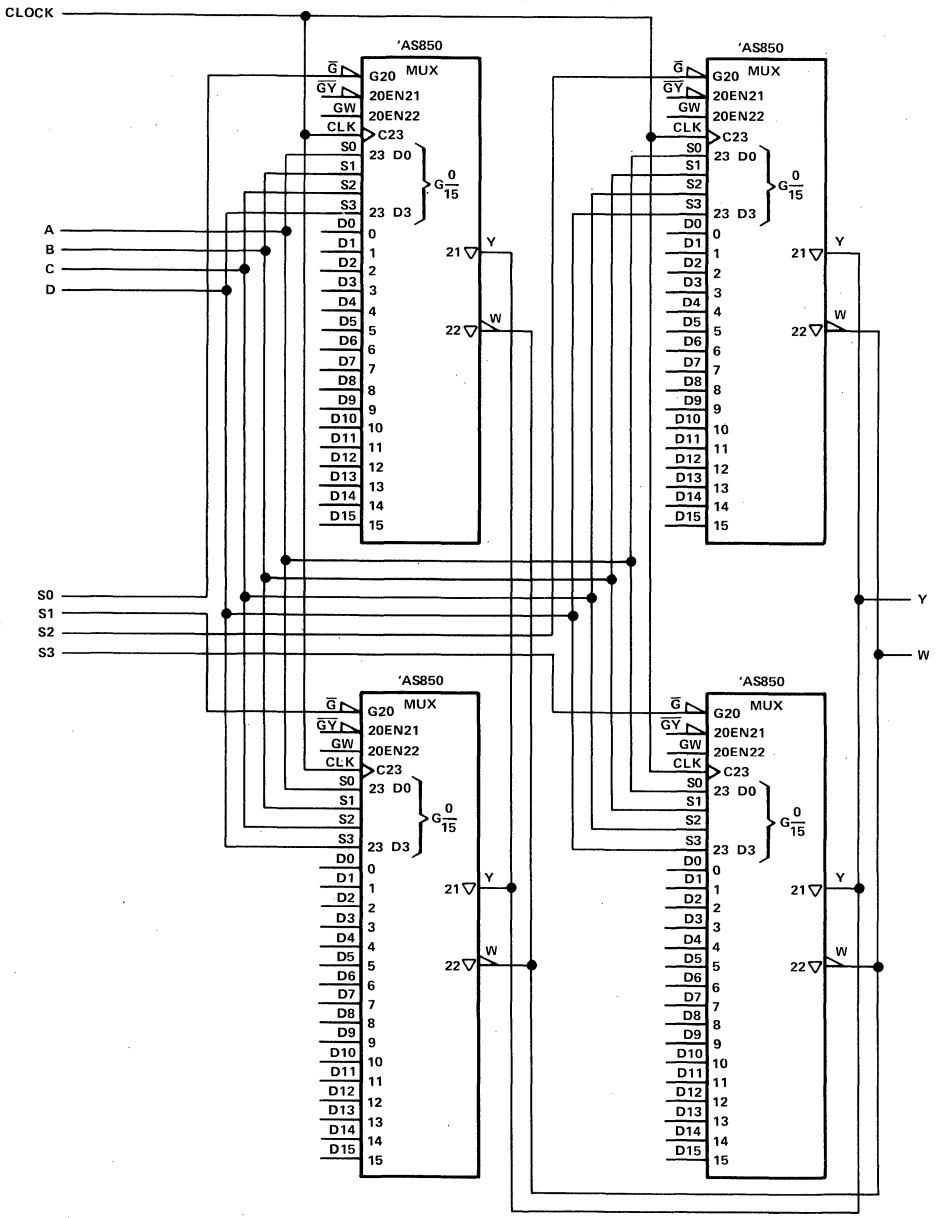


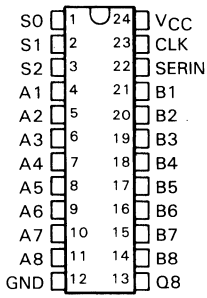
FIGURE 3. 1-of-64 DATA SELECTOR/MULTIPLEXER

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

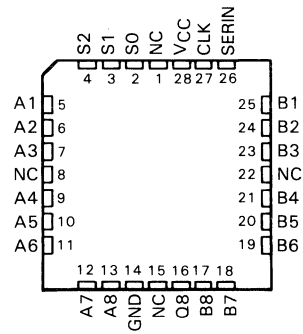
D2810, JUNE 1984—REVISED JANUARY 1986

- Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Buffered 3-State Outputs Drive Bus Lines Directly
- Cascadable to n-Bits
- Eight Selectable Transceiver/Port Functions:
  - A to B or B to A
  - Register to A or B
  - Shifted to A from B or Shifted to B from A
  - Off-Line Shifts (A and B Ports Transceiving or in High-Impedance State)
  - Register Clear
- Particularly Suitable for Use in Diagnostics Circuitry
- Serial Register Provides:
  - — Parallel Storage of Either A or B Input Data
  - — Serial Transmission of Data from Either A or B Port
- Dependable Texas Instruments Quality and Reliability

SN54AS852 . . . JT PACKAGE
SN74AS852 . . . DW or NT PACKAGE
(TOP VIEW)



SN54AS852 . . . FK PACKAGE
SN74AS852 . . . FN PACKAGE
(TOP VIEW)



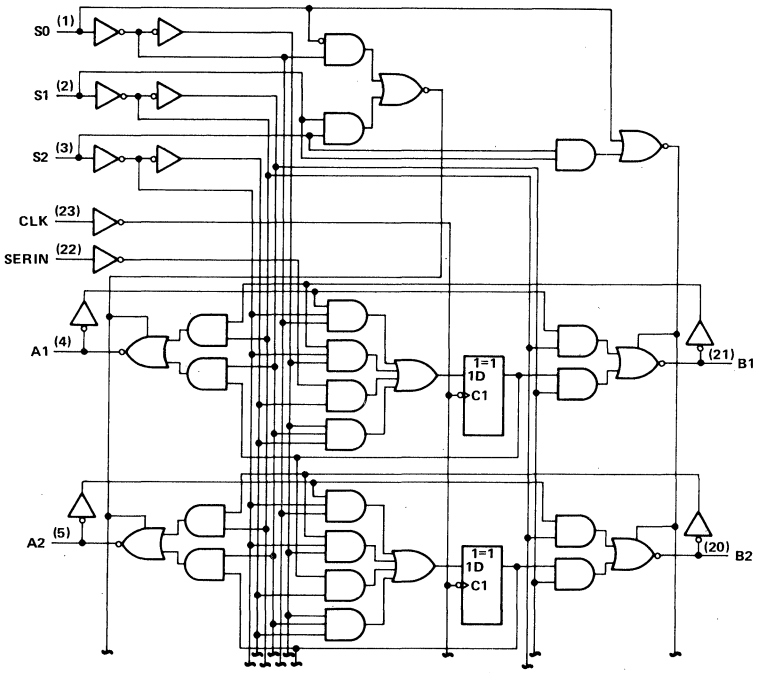
NC—No internal connection

description

The 'AS852 features two 8-bit I/O ports (A1-A8 and B1-B8), and 8-bit parallel-load, serial-in, parallel-out shift register, and control logic. With these features, this device is capable of performing eight selectable transceiver or port functions, depending on the state of the three select lines S0, S1, and S2. These functions include: transferring data from port A to port B or vice versa (i.e., the transceiver function), transferring data from the register to either port, serial shifting data to either port from the opposite port, performing off-line shifts (with A and B ports in high-impedance state), and clearing the register. The 'AS852 can simultaneously transfer data from A to B or B to A and perform an off-line serial shift of data in the register. Synchronous parallel loading of the internal register can be accomplished from either port on the positive transition of the clock while serially shifting data in via the SERIN input. The 'AS852 is ideally suited for applications implementing diagnostic circuitry to enhance system verification and/or fault analysis. All serial data is shifted right. All outputs are buffer-type outputs designed specifically to drive bus lines directly and all are 3-state except for Q8, which is a totem-pole output.

The SN54AS852 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS852 is characterized for operation from 0°C to 70°C.

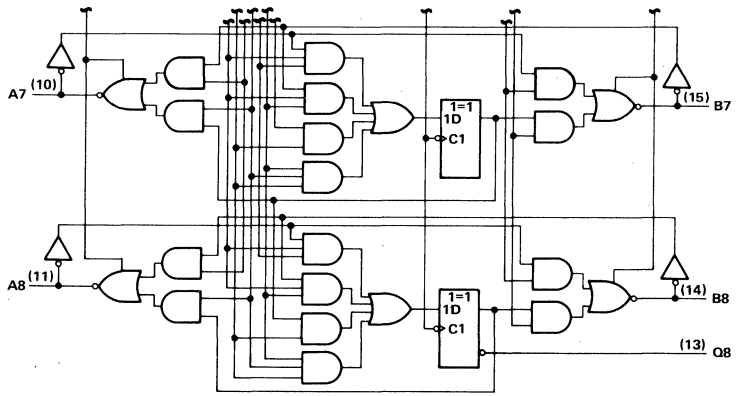
logic diagram (positive logic)



FOUR IDENTICAL CHANNELS NOT SHOWN

INPUTS/OUTPUTS NOT SHOWN:

(6) A3	(19) B3
(7) A4	(18) B4
(8) A5	(17) B5
(9) A6	(16) B6



Pin numbers shown are for DW, JT, and NT packages.

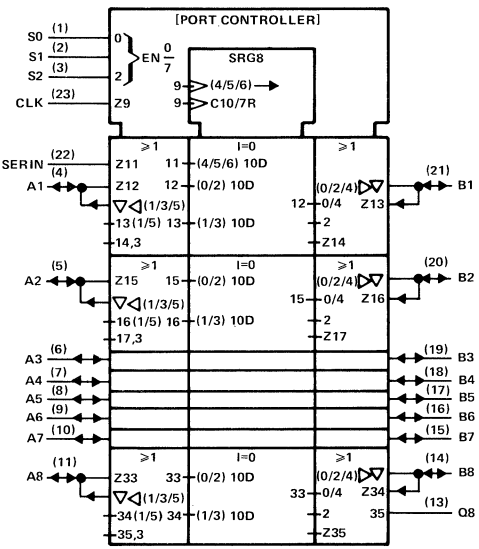
TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

FUNCTION TABLE

MODE S2 S1 S0	CLOCK	SERIN	A1 Q1 B1	A2 Q2 B2	A3 Q3 B3	A4 Q4 B4	A5 Q5 B5	A6 Q6 B6	A7 Q7 B7	A8 Q8 B8	PORT FUNCTION
L L L	H or L	X	Z Q_n A1	Z Q_n A2	Z Q_n A3	Z Q_n A4	Z Q_n A5	Z Q_n A6	Z Q_n A7	Z Q_n A8	A TO B
L L L	↑	X	Z A1 A1	Z A2 A2	A A3 A3	Z A4 A4	Z A5 A5	Z A6 A6	Z A7 A7	Z A8 A8	
L L H	H or L	X	B1 Q_n Z	B2 Q_n Z	B3 Q_n Z	B4 Q_n Z	B5 Q_n Z	B6 Q_n Z	B7 Q_n Z	B8 Q_n Z	B TO A
L L H	↑	X	B1 B1 Z	B2 B2 Z	B3 B3 Z	B4 B4 Z	B5 B5 Z	B6 B6 Z	B7 B7 Z	B8 B8 Z	
L H L	H or L	X	X Q_n Q1	X Q_n Q2	X Q_n Q3	X Q_n Q4	X Q_n Q5	X Q_n Q6	X Q_n Q7	X Q_n Q8	Q_N TO B_N
L H L	↑	X	Z A1 A1	Z A2 A2	Z A3 A3	Z A4 A4	Z A5 A5	Z A6 A6	Z A7 A7	Z A8 A8	
L H H	H or L	X	Q1 Q_n X	Q2 Q_n X	Q3 Q_n X	Q4 Q_n X	Q5 Q_n X	Q6 Q_n X	Q7 Q_n X	Q8 Q_n X	Q_N TO A_N
L H H	↑	X	B1 B1 Z	B2 B2 Z	B3 B3 Z	B4 B4 Z	B5 B5 Z	B6 B6 Z	B7 B7 Z	B8 B8 Z	
H L L	H or L	X	Z Q_n A1	Z Q_n A2	Z Q_n A3	Z Q_n A4	Z Q_n A5	Z Q_n A6	Z Q_n A7	Z Q_n A8	SHIFT
H L L	↑	H	Z H A1	Z Q1 A2	Z Q2 A3	Z Q3 A4	Z Q4 A5	Z Q5 A6	Z Q6 A7	Z Q7 A8	AND
H L L	↑	L	Z L A1	Z Q1 A2	Z Q2 A3	Z Q3 A4	Z Q4 A5	Z Q5 A6	Z Q6 A7	Z Q7 A8	A TO B
H L H	H or L	X	B1 Q_n Z	B2 Q_n Z	B3 Q_n Z	B4 Q_n Z	B5 Q_n Z	B6 Q_n Z	B7 Q_n Z	B8 Q_n Z	SHIFT
H L H	↑	H	B1 H Z	B2 Q1 Z	B3 Q2 Z	B4 Q3 Z	B5 Q4 Z	B6 Q5 Z	B7 Q6 Z	B8 Q7 Z	AND
H L H	↑	L	B1 L Z	B2 Q1 Z	B3 Q2 Z	B4 Q3 Z	B5 Q4 Z	B6 Q5 Z	B7 Q6 Z	B8 Q7 Z	B TO A
H H L	H or L	X	Z Q_n Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	SHIFT
H H L	↑	H	Z H Z	Z Q1 Z	Z Q2 Z	Z Q3 Z	Z Q4 Z	Z Q5 Z	Z Q6 Z	Z Q7 Z	
H H L	↑	L	Z L Z	Z Q1 Z	Z Q2 Z	Z Q3 Z	Z Q4 Z	Z Q5 Z	Z Q6 Z	Z Q7 Z	
H H H	H or L	X	Z Q_n Z	Z Q_n	Z Q_n Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	CLEAR
H H H	↑	X	Z L Z	Z L Z	Z L Z	Z L Z	Z L Z	Z L Z	Z L Z	Z L Z	

n = level of Q_n(n = 1,2, . . . 8) established on the most recent ↑ transition of CLK. Q1 through Q8 are the shift register outputs; only Q8 is available externally. The double inversions that take place as data travels from port to port are ignored in this table.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over free-air temperature range

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54AS852 . . . . . −55°C to 125°C
SN74AS852 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54AS852			SN74AS852			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current	A1-A8, B1-B8			−12			−15	mA
		Q8			−2			−2	
I_{OL}	Low-level output current	A1-A8, B1-B8			32			48	mA
		Q8			20			20	
f_{clock}	Clock frequency		0		45	0		50	MHz
t_w	Duration of clock pulse		11			10			ns
t_{su}	Setup time before CLK↑	A1-A8, B1-B8, SERIN	5.5			5.5			ns
		S0, S1, S2	5.5			5.5			
t_h	Hold-time, data after CLK↑	A1-A8, B1-B8, SERIN	0			0			ns
		S0, S1, S2	0			0			
T_A	Operating free-air temperture		−55		125	0		70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS852			SN74AS852			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	A1-A8, B1-B8	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2					V
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4	3.3		
	All outputs	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			
V_{OL}	All outputs except Q8	V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.3	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
	Q8	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.25	0.5		0.25	0.5	
I_I	S0, S1, S2	V_{CC} = 5.5 V,	V_I = 7 V			0.3			0.3	mA
	CLK and SERIN					0.1			0.1	
	A1-A8, B1-B8	V_{CC} = 5.5 V,	V_I = 5.5 V			0.2			0.2	
I_{IH}	S0, S1, S2	V_{CC} = 5.5 V,	V_I = 2.7 V			60			60	μA
	CLK and SERIN					20			20	
	A1-A8, B1-B8‡					70			70	
I_{IL}	S0, S1, S2	V_{CC} = 5.5 V,	V_I = 0.4 V			−1			−1	mA
	CLK and SERIN					−0.5			−0.5	
	A1-A8, B1-B8‡					−0.5			−0.5	
I_O§	Except Q8	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
	Q8			−20		−112	−20		−112	
I_{CC}		V_{CC} = 5.5 V			136	220		136	220	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡For I/O ports, the parameters I_{IH} and I_{IL} include the output currents I_{OZH} and I_{OZL}, respectively.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

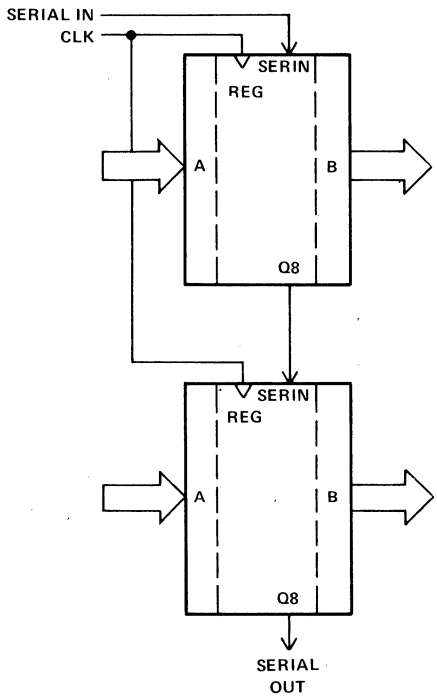
switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	R_L = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS852		SN74AS852		
			MIN	MAX	MIN	MAX	
f_{max}			45		50		MHz
t_{PLH}	Any A port	Any B port	2	9	2	7.5	ns
t_{PHL}			3	12.5	3	11	
t_{PLH}	Any B port	Any A port	2	9	2	7.5	ns
t_{PHL}			3	12.5	3	11	
t_{PLH}	S0, S1, S2¶	Any A or B port	3	11.5	3	10	ns
t_{PHL}			3	12	3	10.5	
t_{PLH}	CLK	Any A or B port	2	11	2	9	ns
t_{PHL}			3	14	3	12.5	
t_{PLH}	CLK	Q8	2	10.5	2	8	ns
t_{PHL}			3	11.5	3	10	
t_{PHZ}	S0, S1, S2	Any A or B port	2	9	2	7	ns
t_{PLZ}			3	13	3	10.5	
t_{PZH}			2	9	2	7	ns
t_{PZL}			3	13	3	10.5	

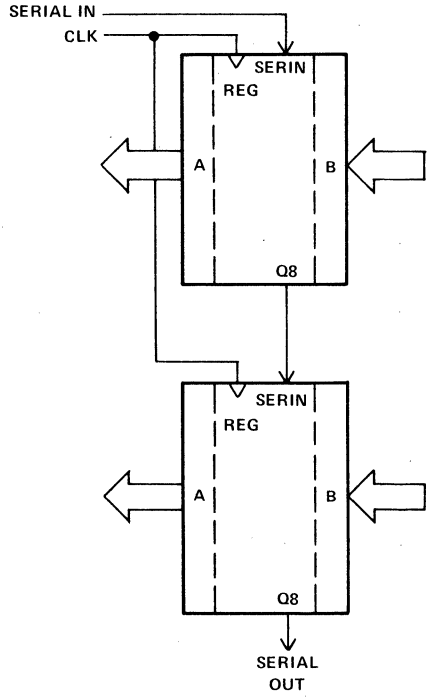
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.
¶ The positive transition of S1 control pin will cause low-level data on the A or B bus to be invalid for 17.5 ns.

TYPICAL APPLICATION DATA

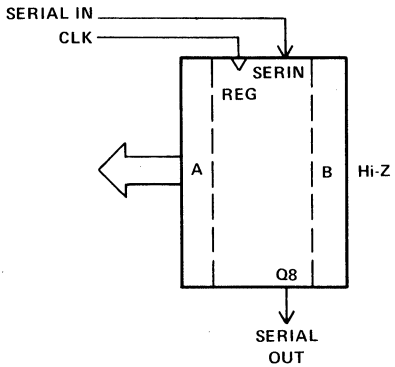
BUS A TO BUS B OR
SERIAL TRANSMISSION



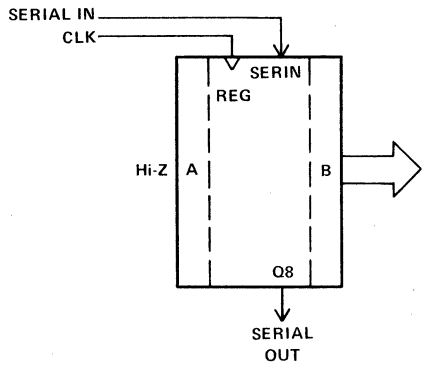
BUS B TO BUS A OR
SERIAL TRANSMISSION



SERIAL IN TO A PORT



SERIAL IN TO B PORT

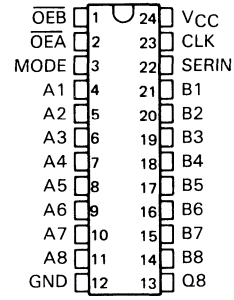


TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

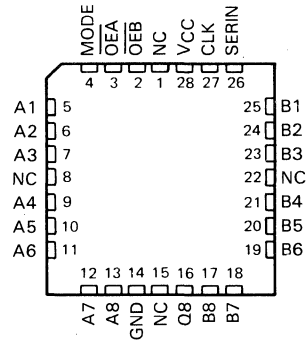
D2814, DECEMBER 1983—REVISED MARCH 1985

- Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Buffered 3-State Outputs Drive Bus Lines Directly
- Cascadable to n-Bits
- Eight Selectable Transceiver/Port Functions:
  - B to A
  - Register to A and/or B
  - Off-Line Shifts (A and B Ports in High-Impedance State)
  - Shifted to A and/or B
- Particularly Suitable for Use in Diagnostics Analysis Circuitry
- Serial Register Provides:
  - Parallel Storage of Either A or B Input Data
  - Serial Transmission of Data from Either A or B Port
  - Readback Mode B to A
- Dependable Texas Instruments Quality and Reliability

SN54AS856 . . . JT PACKAGE
SN74AS856 . . . DW or NT PACKAGE
(TOP VIEW)



SN54AS856 . . . FK PACKAGE
SN74AS856 . . . FN PACKAGE
(TOP VIEW)



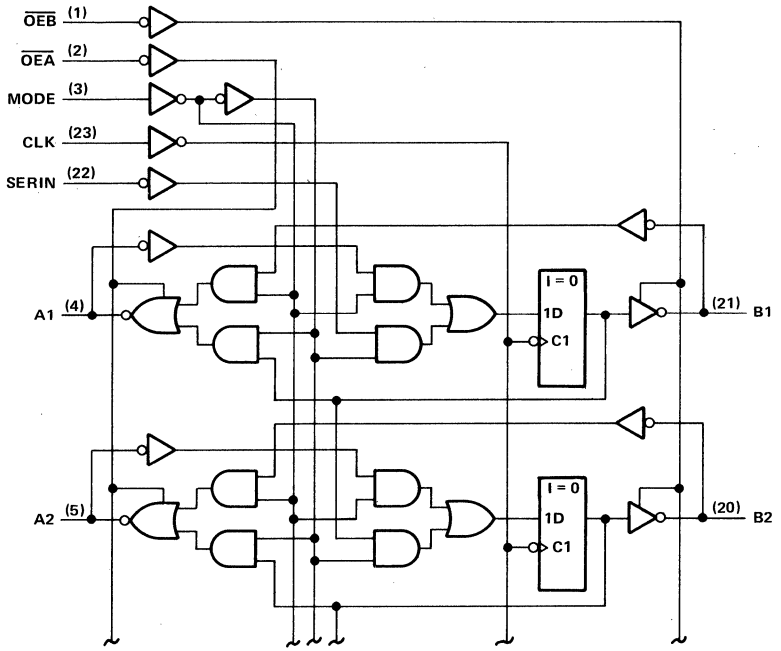
NC – No internal connection

description

The 'AS856 features two 8-bit I/O ports (A1-A8 and B1-B8), an 8-bit parallel-load, serial-in, parallel-out shift register, and control logic. With these features, this device is capable of performing eight selectable transceiver or port functions, depending on the state of the three control lines $\overline{OEA}$, $\overline{OEB}$, and MODE. These functions include: transferring data from port A to port B or vice versa (i.e., the transceiver function), serial shifting data to either or both ports, and performing off-line shifts (with A and B ports active as transceivers in a high-impedance state). Synchronous parallel loading of the internal register can be accomplished from either port on the positive transition of the clock while serially shifting data in via the SERIN input. The 'AS856 is ideally suited for applications needing signature-analysis circuitry to enhance system verification and/or fault analysis. All serial data is shifted right. All outputs are buffer-type outputs designed specifically to drive bus lines directly and all are 3-state except for Q8, which is a totem-pole output.

The SN54AS856 is characterized for operation over the full military temperaure range of −55°C to 125°C. The SN74AS856 is characterized for operation from 0°C to 70°C.

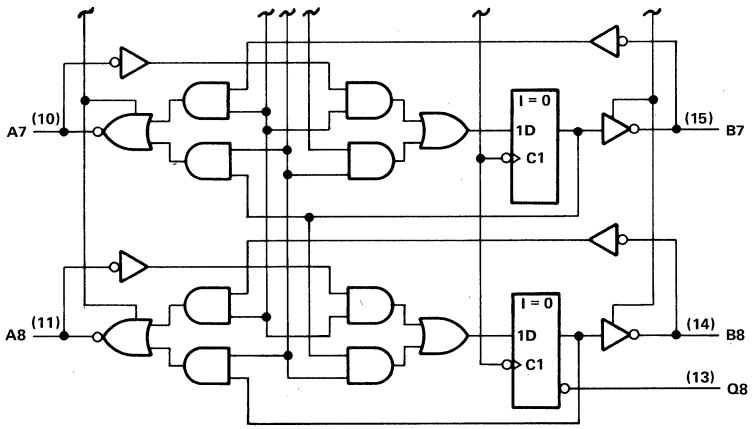
logic diagram (positive logic)



FOUR IDENTICAL CHANNELS NOT SHOWN

INPUTS/OUTPUTS NOT SHOWN:

(6) A3	(19) B3
(7) A4	(18) B4
(8) A5	(17) B5
(9) A6	(16) B6



Pin numbers shown are for DW, JT, and NT packages.

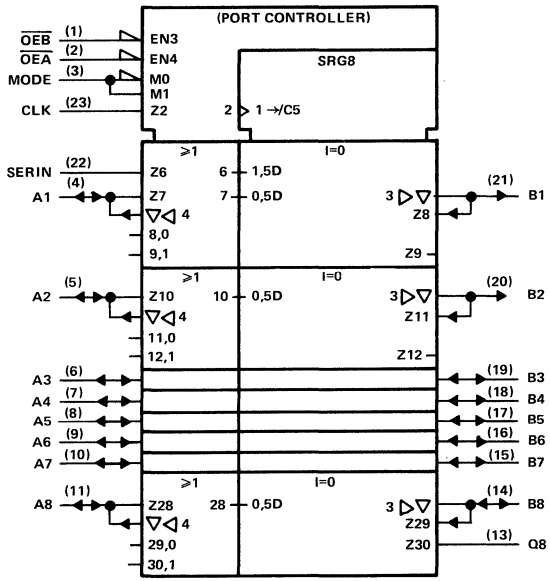
TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

FUNCTION TABLE

MODE	$\overline{OEA}$	$\overline{OEB}$	CLOCK	SERIN	A1 Q1 B1	A2 Q2 B2	A3 Q3 B3	A4 Q4 B4	A5 Q5 B5	A6 Q6 B6	A7 Q7 B7	A8 Q8 B8	FUNCTION
L	L	L	H or L	X	Q1 Q1 Q1	Q2 Q2 Q2	Q3 Q3 Q3	Q4 Q4 Q4	Q5 Q5 Q5	Q6 Q6 Q6	Q7 Q7 Q7	Q8 Q8 Q8	FEEDBACK
L	L	L	↑	X	Q1 Q1 Q1	Q2 Q2 Q2	Q3 Q3 Q3	Q4 Q4 Q4	Q5 Q5 Q5	Q6 Q6 Q6	Q7 Q7 Q7	Q8 Q8 Q8	
L	L	H	H or L	X	B1 Q1 Z	B2 Q2 Z	B3 Q3 Z	B4 Q4 Z	B5 Q5 Z	B6 Q6 Z	B7 Q7 Z	B8 Q8 Z	B to A
L	L	H	↑	X	B1 B1 Z	B2 B2 Z	B3 B3 Z	B4 B4 Z	B5 B5 Z	B6 B6 Z	B7 B7 Z	B8 B8 Z	A to Q
L	H	L	H or L	X	Z Q1 Q1	Z Q2 Q2	Z Q3 Q3	Z Q4 Q4	Z Q5 Q5	Z Q6 Q6	Z Q7 Q7	Z Q8 Q8	A to Q
L	H	L	↑	X	Z A1 A1	Z A2 A2	Z A3 A3	Z A4 A4	Z A5 A5	Z A6 A6	Z A7 A7	Z A8 A8	Q to B
L	H	H	H or L	X	Z Q1 Z	Z Q2 Z	Z Q3 Z	Z Q4 Z	Z Q5 Z	Z Q6 Z	Z Q7 Z	Z Q8 Z	A to Q
L	H	H	↑	X	Z A1 Z	Z A2 Z	Z A3 Z	Z A4 Z	Z A5 Z	Z A6 Z	Z A7 Z	Z A8 Z	
H	L	L	H or L	X	Q1 Q_n Q1	Q2 Q_n Q2	Q3 Q_n Q3	Q4 Q_n Q4	Q5 Q_n Q5	Q6 Q_n Q6	Q7 Q_n Q7	Q8 Q_n Q8	SHIFT
H	L	L	↑	H	H H H	Q1 Q1 Q1	Q2 Q2 Q2	Q3 Q3 Q3	Q4 Q4 Q4	Q5 Q5 Q5	Q6 Q6 Q6	Q7 Q7 Q7	TO
H	L	L	↑	L	L L L	Q1 Q1 Q1	Q2 Q2 Q2	Q3 Q3 Q3	Q4 Q4 Q4	Q5 Q5 Q5	Q6 Q6 Q6	Q7 Q7 Q7	A and B
H	L	H	H or L	X	Q1 Q_n Z	Q2 Q_n Z	Q3 Q_n Z	Q4 Q_n Z	Q5 Q_n Z	Q6 Q_n Z	Q7 Q_n Z	Q8 Q_n Z	SHIFT
H	L	H	↑	H	H H Z	Q1 Q1 Z	Q2 Q2 Z	Q3 Q3 Z	Q4 Q4 Z	Q5 Q5 Z	Q6 Q6 Z	Q7 Q7 Z	TO
H	L	H	↑	L	L L Z	Q1 Q1 Z	Q2 Q2 Z	Q3 Q3 Z	Q4 Q4 Z	Q5 Q5 Z	Q6 Q6 Z	Q7 Q7 Z	A
H	H	L	H or L	X	Z Q_n Q1	Z Q_n Q2	Z Q_n Q3	Z Q_n Q4	Z Q_n Q5	Z Q_n Q6	Z Q_n Q7	Z Q_n Q8	SHIFT
H	H	L	↑	H	Z H H	Z Q1 Q1	Z Q2 Q2	Z Q3 Q3	Z Q4 Q4	Z Q5 Q5	Z Q6 Q6	Z Q7 Q7	TO
H	H	L	↑	L	Z L L	Z Q1 Q1	Z Q2 Q2	Z Q3 Q3	Z Q4 Q4	Z Q5 Q5	Z Q6 Q6	Z Q7 Q7	B
H	H	H	H or L	X	Z Q_n Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	SHIFT
H	H	H	↑	H	Z H Z	Z Q1 Z	Z Q2 Z	Z Q3 Z	Z Q4 Z	Z Q5 Z	Z Q6 Z	Z Q7 Z	
H	H	H	↑	L	Z L H	Z Q1 Z	Z Q2 Z	Z Q3 Z	Z Q4 Z	Z Q5 Z	Z Q6 Z	Z Q7 Z	

n = level of Q_n(n = 1, 2 . . . 8) established on most recent ↑ transition of CLK. Q1 through Q8 are the shift register outputs; only Q8 is available externally. The double inversions that take place as data travels from port to port are ignored in this table.

logic symbol†



Pin numbers shown are for DW, JT, and NT packages.

†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over free-air temperature range

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54AS856 . . . . . −55°C to 125°C
SN74AS856 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54AS856			SN74AS856			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current	A1-A8, B1-B8			−12			−15	mA
		Q8			−2			−2	
I_{OL}	Low-level output current	A1-A8, B1-B8			32			48	mA
		Q8			20			20	
f_{clock}	Clock frequency		0		45	0		50	MHz
t_w	Duration of clock pulse		11			10			ns
t_{su}	Setup time before CLK↑	A1-A8, B1-B8 SERIN	5.5			5.5			ns
		$\overline{OEB}$, $\overline{OEA}$, MODE	5.5			5.5			
t_h	Hold-time, data after CLK↑	A1-A8, B1-B8 SERIN	0			0			ns
		$\overline{OEB}$, $\overline{OEA}$, MODE	0			0			
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS856			SN74AS856			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	A1-A8	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2	3.2					V
	B1-B8	V_{CC} = 4.5 V,	I_{OH} = −15 mA				2	3.3		
	All outputs	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			
V_{OL}	All outputs except Q8	V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
	Q8	V_{CC} = 4.5 V,	I_{OL} = 20 mA			0.5			0.5	
I_I	$\overline{OEB}$, $\overline{OEA}$, MODE	V_{CC} = 5.5 V,	V_I = 7 V			0.2			0.2	mA
	CLK and SERIN					0.1			0.1	
	A1-A8, B1-B8	V_{CC} = 5.5 V,	V_I = 5.5 V			0.2			0.2	
I_{IH}	$\overline{OEB}$, $\overline{OEA}$, MODE	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	μA
	CLK and SERIN					20			20	
	A1-A8, B1-B8‡					70			70	
I_{IL}	$\overline{OEB}$, $\overline{OEA}$, MODE	V_{CC} = 5.5 V,	V_I = 0.4 V			−1			−1	mA
	CLK and SERIN					−0.5			−0.5	
	A1-A8, B1-B8‡					−0.5			−0.5	
I_O§	Except Q8	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
	Q8			−20		−112	−20		−112	
I_{CC}		V_{CC} = 5.5 V			118	200		118	200	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡For I/O ports, the parameters I_{IH} and I_{IL} include the output currents I_{OZH} and I_{OZL}, respectively.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS856		SN74AS856		
			MIN	MAX	MIN	MAX	
f_{max}			45		50		MHz
t_{PLH}	Any B port	Any A port	2	8	2	7	ns
t_{PHL}			2	10.5	2	9.5	
t_{PLH}	↑MODE¶	Any A or B port	2	8.5	2	7.5	ns
t_{PHL}			5	20	5	19	
t_{PLH}	↓MODE	Any A or B port	2	8.5	2	7.5	ns
t_{PHL}			2	9.5	2	8	
t_{PLH}	CLK	Any A or B port	3	12	3	9	ns
t_{PHL}			3	12	3	11	
t_{PLH}	CLK	Q8	2	9	2	7.5	ns
t_{PHL}			2	10	2	9	
t_{PHZ}	$\overline{OEA}$ or $\overline{OEB}$	Any A or B port	2	9	2	7	ns
t_{PLZ}			2	12	2	9.5	
t_{PZH}			2	8	2	7	ns
t_{PZL}			2	11	2	10	

¶The positive transition of the MODE control will cause low-level data at the A output Bus or stored in Q to be invalid for 12 ns.
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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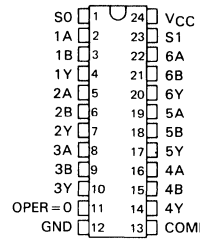
- Selects True or Complementary Data
- Performs AND/NAND (masking) of A or B Operand
- Cascadable to Expand Number of Operands
- Detects Zeros on A or B Operands
- 3-State Outputs Interface Directly with System Bus
- Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS857, SN54AS857 . . . JT PACKAGE
SN74ALS857, SN74AS857 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54ALS857, SN54AS857 . . . FK PACKAGE
SN74ALS857, SN74AS857 . . . FN PACKAGE

For chip carrier information
contact factory

description

The 'ALS857 and 'AS857 are hextuple 2-line to 1-line multiplexers with three-state outputs. The devices can provide either true (COMP low) or inverted (COMP high) data at the Y outputs. In addition, the 'ALS857 and 'AS857 perform the logical AND function (A·B) and the clear function as well. The four modes of operation are:

Select A data inputs,
Select B data inputs,
AND A inputs with B inputs,
Clear

In either of the first two modes, OPER = 0 is high if all the selected A or B inputs are low.

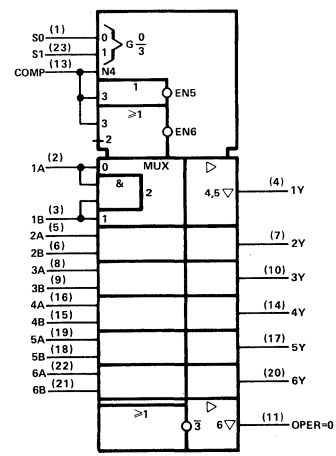
The six Y outputs and the OPER = 0 output are all three-state and rated at 12 mA and 24 mA I_{OL} for the SN54ALS857 and SN74ALS857, respectively, and at 32 mA and 48 mA I_{OL} for the SN54AS857 and SN74AS857, respectively. All outputs can be placed into the high-impedance state by applying a high level to the COMP, S0, and S1 inputs simultaneously. The complete function table is shown below.

The SN54ALS857 and SN54AS857 are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS857 and SN74AS857 are characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE

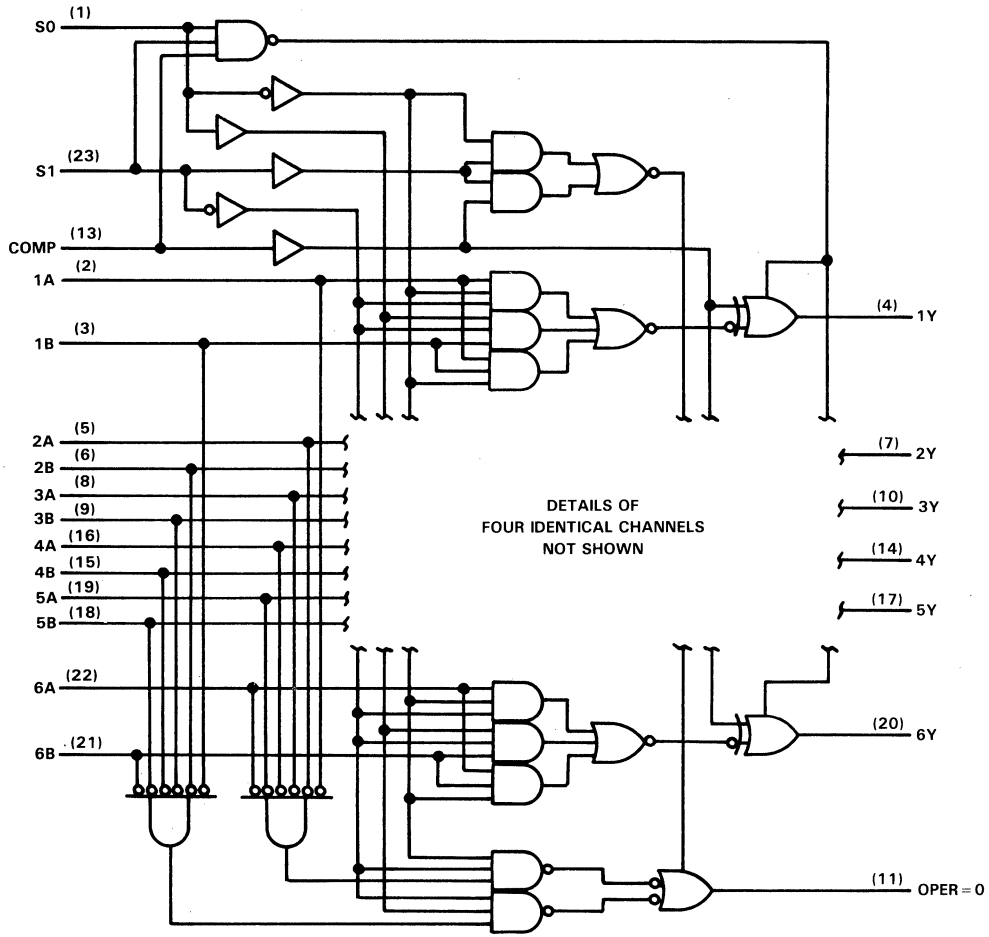
COMP	S1	S0	Y OUTPUTS	OPER = ZERO
L	L	L	A	H = all A inputs L
L	L	H	B	H = all B inputs L
L	H	L	A·B	Z
L	H	H	L	L
H	L	L	$\overline{A}$	H = all A inputs L
H	L	H	$\overline{B}$	H = all B inputs L
H	H	L	$\overline{A \cdot B}$	Z
H	H	H	Z	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

'ALS857 logic diagram (positive logic)



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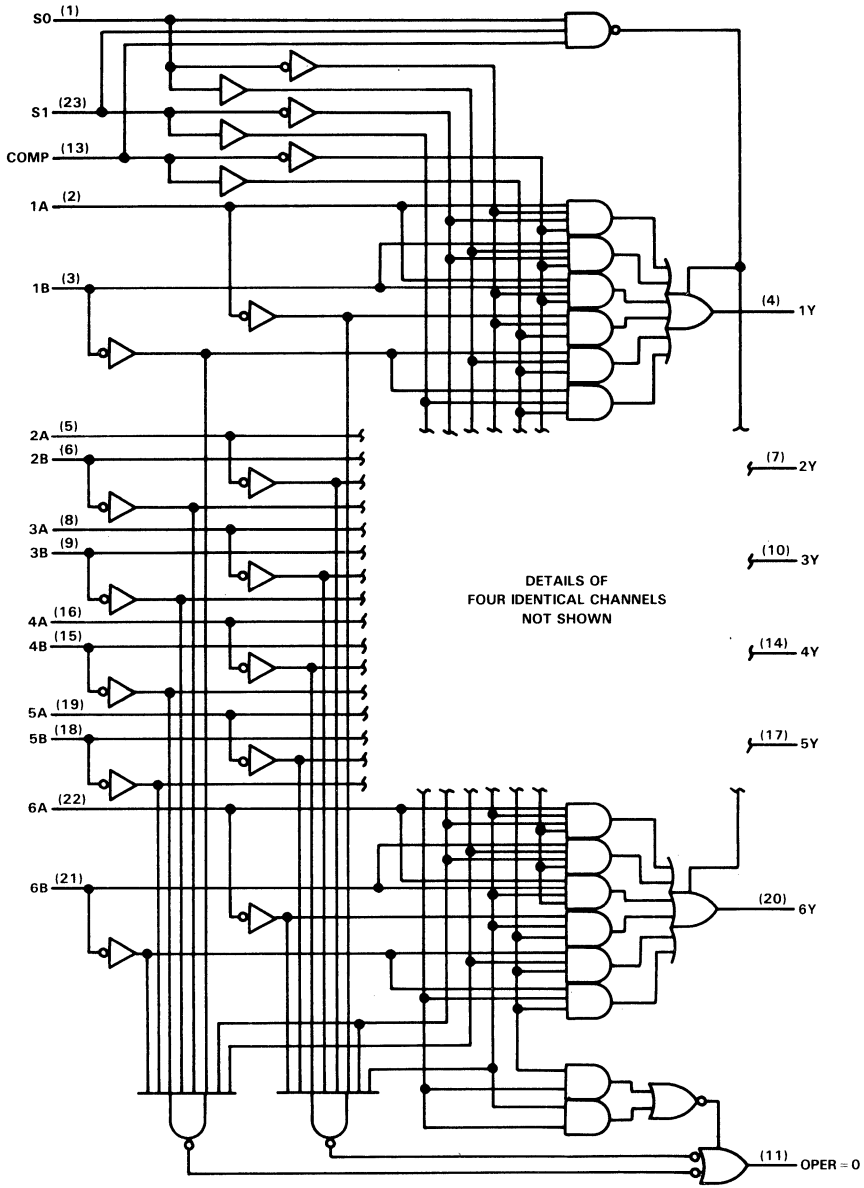
'AS857 logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS857 . . . . . −55 °C to 125 °C
SN74ALS857 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS857			SN74ALS857			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			−24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS857			SN74ALS857			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
I_{CC}	V_{CC} = 5.5 V, See Note 1	Outputs high		11	24		11	24	mA
		Outputs low		16	33		16	33	
		Outputs disabled		18	36		18	36	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with all possible inputs grounded while achieving the stated output conditions.

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switching characterisitcs (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS857		SN74ALS857		
			MIN	MAX	MIN	MAX	
t_{pd}	A or B (COMP high)	Y (Inverting)	4	28	4	25	ns
t_{pd}	A or B (COMP low)	Y (Noninverting)	4	21	4	18	ns
t_{pd}	S0 or S1	Y	7	37	7	33	ns
t_{pd}	COMP	Y	6	22	6	18	
t_{pd}	A or B	OPER = 0	5	45	5	37	
t_{pd}	S0 or S1	OPER = 0	5	30	5	23	
t_{en}	S0 or S1	Y	7	38	7	35	ns
t_{dis}			2	29	2	23	
t_{en}	COMP	Y	8	27	8	24	ns
t_{dis}			6	27	6	21	
t_{en}	S0	OPER = 0	6	24	6	20	ns
t_{dis}			11	34	11	27	
t_{en}	S1	OPER = 0	6	28	6	25	ns
t_{dis}			3	23	3	19	
t_{en}	COMP	OPER = 0	9	30	9	25	ns
t_{dis}			6	24	6	20	

$t_{pd} = t_{PLH}$ or t_{PHL}
$t_{en} = t_{PZH}$ or t_{PZL}
$t_{dis} = t_{PHZ}$ or t_{PLZ}
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54AS857 . . . . . −55°C to 125°C
SN74AS857 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54AS857			SN74AS857			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current	Y Outputs			−12			−15	mA
		OPER = 0			−2			−2	
I_{OL}	Low-level output current	Y Outputs			32			48	mA
		OPER = 0			20			20	
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS857			SN74AS857			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	Y Outputs	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2					V
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4	3.3		
	All Outputs	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			
V_{OL}	Y Outputs	V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.35	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
	OPER = 0	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.25	0.5		0.25	0.5	
I_{OZH}		V_{CC} = 5.5 V,	I_{OL} = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−2			−2	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−50		−150	−50		−150	mA
I_{CC}		V_{CC} = 5.5 V, See Note 1	Outputs high		97	140		97	140	mA
			Outputs low		127	175		127	175	
			Outputs disabled		92	135		92	135	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with all possible inputs grounded while achieving the stated output conditions.

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switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V, to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS857		SN74AS857		
			MIN	MAX	MIN	MAX	
t_{pd}	A or B (COMP high)	Y (Inverting)	2	15	2	12	ns
t_{pd}	A or B (COMP low)	Y (Noninverting)	2	12	2	10	ns
t_{pd}	S0 or S1	Y	2	15	2	13	ns
t_{pd}	COMP	Y	2	15	2	13	
t_{pd}	A or B	OPER = 0	2	16	2	14	
t_{pd}	S0 to S1	OPER = 0	2	20	2	18	
t_{en}	S0 to S1	Y	2	14	2	12	ns
t_{dis}			2	13	2	11	
t_{en}	COMP	Y	2	14	2	12	ns
t_{dis}			2	10	2	9	
t_{en}	S0	OPER = 0	2	14	2	12	ns
t_{dis}			2	10	2	9	
t_{en}	S1	OPER = 0	2	14	2	12	ns
t_{dis}			2	10	2	9	
t_{en}	COMP	OPER = 0	2	15	2	13	ns
t_{dis}			2	10	2	9	

$t_{pd} = t_{PLH}$ or t_{PHL}
$t_{en} = t_{PZH}$ or t_{PAL}
$t_{dis} = t_{PHZ}$ or t_{PLZ}
NOTE 1. Load circuit and voltage waveforms are shown in Section 1.

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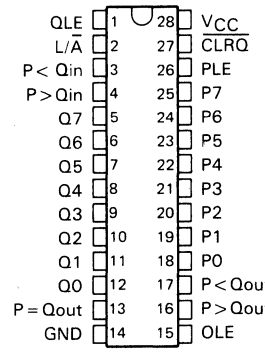
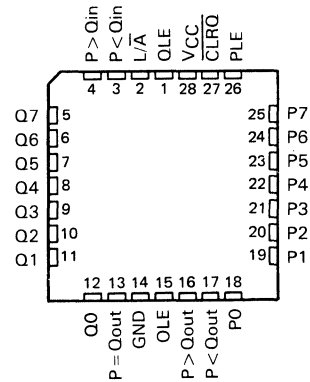
- **Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Input and Output Latches with Active-High Enables**
- **Fast Compare to Zero**
- **Arithmetic and Logical Comparison**
- **Open-Collector P = Q Output**
- **Dependable Texas Instruments Quality and Reliability**

SN54AS866 . . . JD PACKAGE
SN74AS866 . . . N PACKAGE
(TOP VIEW)



SN54AS866 . . . FK PACKAGE
SN74AS866 . . . FN PACKAGE
(TOP VIEW)



description

These Advanced Schottky devices are capable of performing high-speed arithmetic or logical comparisons on two 8-bit binary or two's complement words. Three fully decoded decisions about words P and Q are externally available at the outputs. These devices are fully expandable to any word length by connecting the totem pole P>Q and P<Q outputs of each stage to the P>Q and P<Q inputs of the next higher-order stage. The cascading paths are implemented with only a two-gate-level delay to reduce overall comparison times for long words. The open-collector P=Q output may be wire-ANDed together.

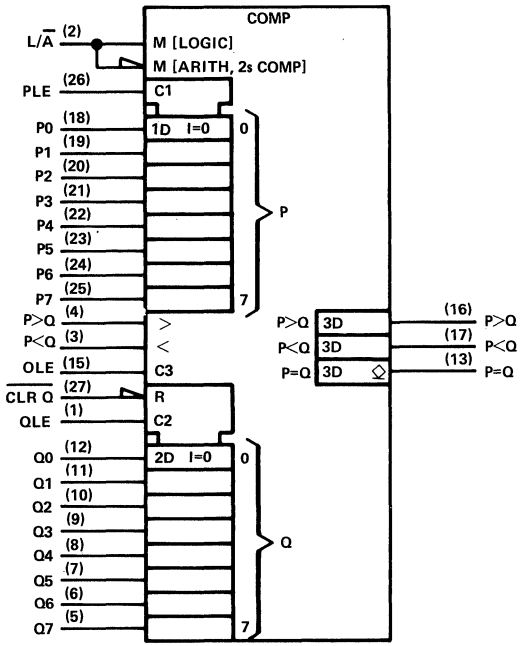
Both input words P and Q plus all three outputs (P>Q, P<Q, and P=Q) are equipped with latches to provide the designer with temporary data storage for avoiding race conditions. The enable circuitry is implemented with minimal delay times to enhance performance when the devices are cascaded for longer word lengths. Each latch is transparent when the appropriate latch enable, PLE, QLE, or OLE is high.

The enable inputs PLE and QLE and data inputs P and Q utilize p-n-p input transistors to reduce the low-level input current requirement to typically −0.25 mA, which minimizes loading effects.

The Q register may be cleared to zero for a fast comparison of the P word to zero.

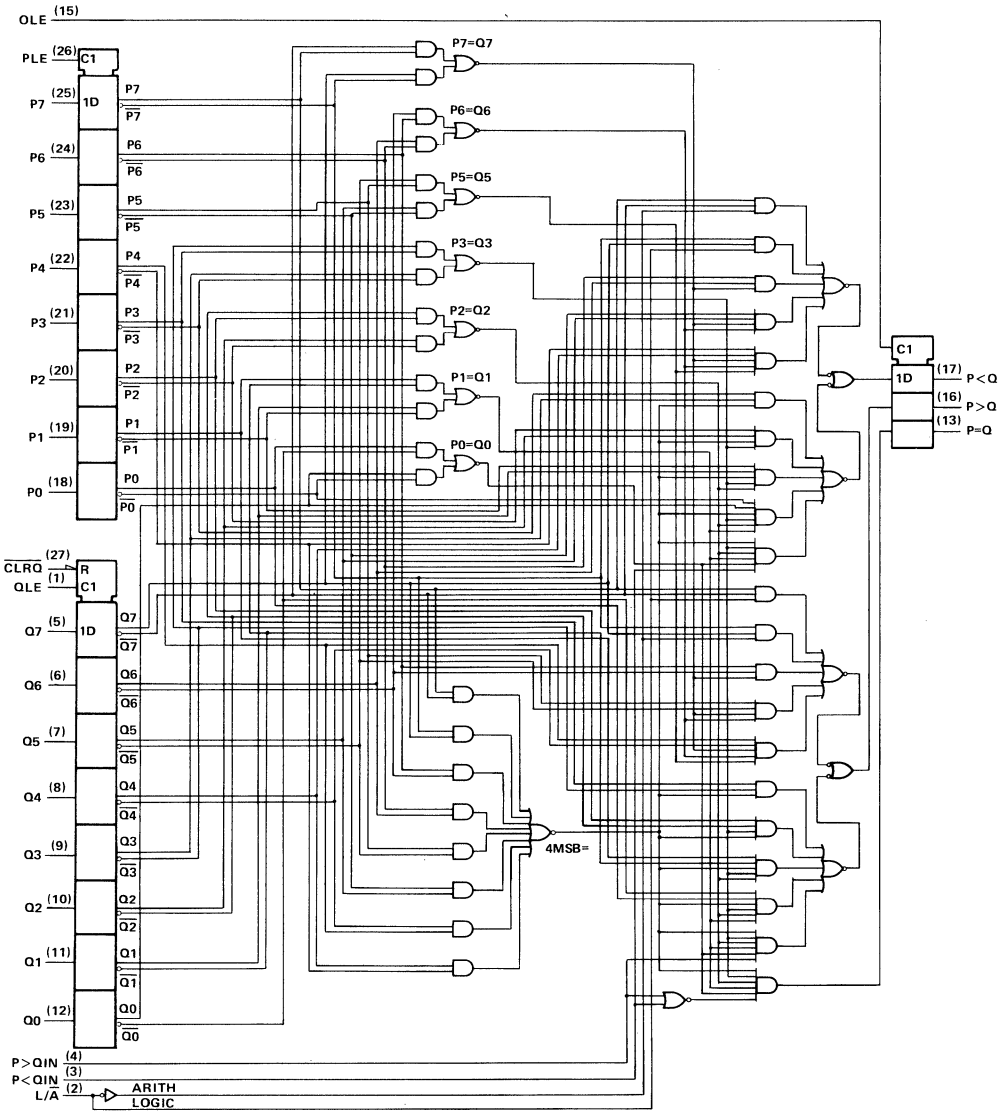
The SN54AS866 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS866 is characterized for operation from 0°C to 70°C.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



FUNCTION TABLE

COMPARISON	L/$\overline{A}$	DATA INPUTS P0-P7, Q0-Q7	INPUTS		OUTPUTS		
			P > Q	P < Q	P > Q	P < Q	P = Q
Logical	H	P > Q	X	X	H	L	L
Logical	H	P < Q	X	X	L	H	L
Logical	H	P = Q	L	L	L	L	H
Logical	H	P = Q	L	H	L	H	L
Logical	H	P = Q	H	L	H	L	L
Logical	H	P = Q	H	H	H	H	L
Arithmetic	L	P AG Q	X	X	H	L	L
Arithmetic	L	Q AG P	X	X	L	H	L
Arithmetic	L	P = Q	L	L	L	L	H
Arithmetic	L	P = Q	L	H	L	H	L
Arithmetic	L	P = Q	H	L	H	L	L
Arithmetic	L	P = Q	H	H	H	H	L

AG = arithmetically greater than

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage, P = Q output . . . . . 7 V
Operating free-air temperature range: SN54AS866 . . . . . −55°C to 125°C
SN74AS866 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

PARAMETER		SN54AS866			SN74AS866			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current, all outputs except P = Q			−2			−2	mA
V_{OH}	High-level output voltage, P = Q output			5.5			5.5	V
I_{OL}	Low-level output current			20			20	mA
t_{su}	Setup time to PLE, QLE, OLE↓	2			2			ns
t_h	Hold time after PLE, QLE, OLE↓	4			4			ns
T_A	Operating free-air temperature	−55		125	0		70	°C

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POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS866			SN74AS866			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	P > Q, P < Q	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC} −2			V_{CC} −2			
I_{OH}	P = Q only	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.25			0.25	mA
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	L/$\overline{A}$, OLE	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	μA
	Others					20			20	
I_{IL}	L/$\overline{A}$, OLE, P > Qin, P < Qin	V_{CC} = 5.5 V,	V_I = 0.4 V			−4			−4	mA
	$\overline{CLRQ}$					−2			−2	
	P, Q, PLE, QLE				−0.25	−1		−0.25	−1	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−20		−112	−20		−112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		160	240		160	240	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit, I_{OS}.
NOTE 1: I_{CC} is measured with all inputs high except L/A, which is low.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			SN54AS866			SN74AS866			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	L/$\overline{A}$	P < Q, P > Q	1	8.5	14	1	8.5	13	ns
t_{PHL}			1	7.5	14	1	7.5	13	
t_{PLH}	P < Q, P > Q		1	5	10	1	5	8	ns
t_{PHL}			1	5.5	10	1	5.5	8	
t_{PLH}	Any P or Q Data Input		1	13.5	21	1	13.5	17.5	ns
t_{PHL}			1	10	17	1	10	15	
t_{PLH}	$\overline{CLRQ}$		1	16	21	1	16	20	ns
t_{PHL}			1	12	17	1	12	16	

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, T_A = 280 Ω, T_A = MIN to MAX						UNIT
			SN54AS866			SN74AS866			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	P < Q, P > Q	P = Q	1	6.5	12	1	6.5	11	ns
t_{PHL}			1	8	14	1	8	13	
t_{PLH}	Any P or Q Data Input	P = Q	1	10	15	1	10	14	ns
t_{PHL}			1	9	14	1	9	13	
t_{PLH}	$\overline{CLRQ}$	P = Q	1	12	17	1	12	16	ns
t_{PHL}			1	13	18	1	13	17	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

TYPICAL APPLICATION DATA

This sequence of comparisons illustrates how the $\overline{CLRQ}$ function can be used to perform dual comparisons of the varying P terms (P0, P1, etc.). When $\overline{CLRQ}$ is high, the P term is compared to the Q term. When $\overline{CLRQ}$ is taken low, the P term is compared to zero. This or similar sequences can enhance performance and reduce package count to perform value range checks.

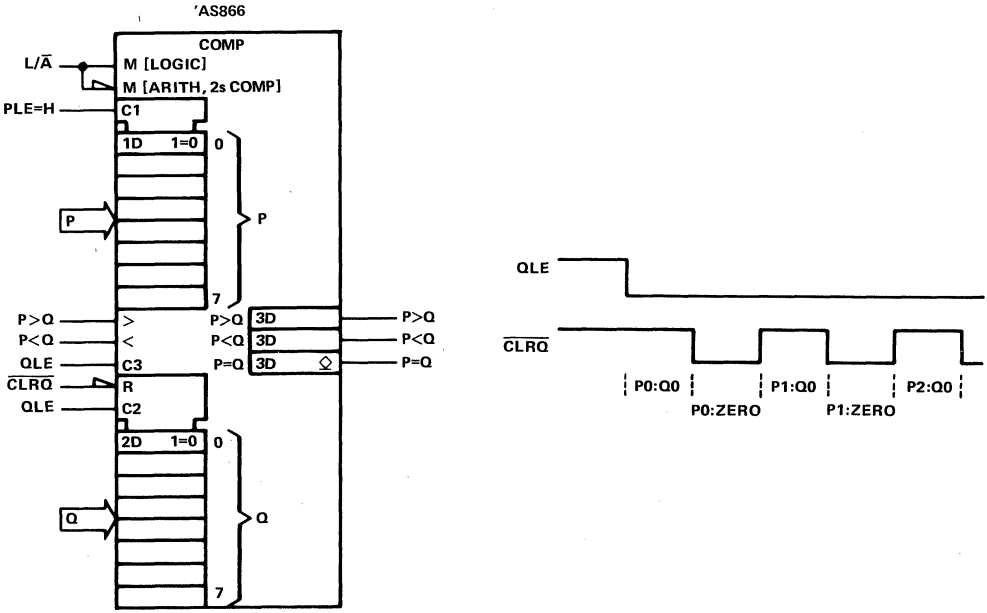

FIGURE 1. MAGNITUDE COMPARISONS COMBINED WITH QUICK COMPARISONS TO ZERO (RANGE VERIFICATIONS)

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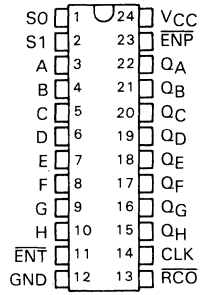
SYNCHRONOUS 8-BIT UP/DOWN COUNTERS

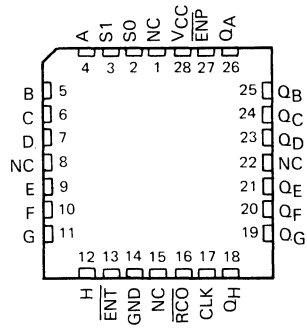
D2661, DECEMBER 1982 – REVISED MAY 1986

- **Fully Programmable with Synchronous Counting and Loading**
- **'867 Has Asynchronous Clear, '869 Has Synchronous Clear**
- **Fully Independent Clock Circuit Simplifies Use**
- **Ripple Carry Output for n-Bit Cascading**
- **Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54' . . . JT PACKAGE
SN74' . . . DW OR NT PACKAGE
(TOP VIEW)



SN54' . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

These synchronous presettable counters feature an internal carry look-ahead for cascading in high-speed counting applications. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple-clock) counters. A buffered clock input triggers the eight flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; that is, the outputs may each be preset to either level. The load mode circuitry allows parallel loading of the cascaded counters. As loading is synchronous, selecting the load mode disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

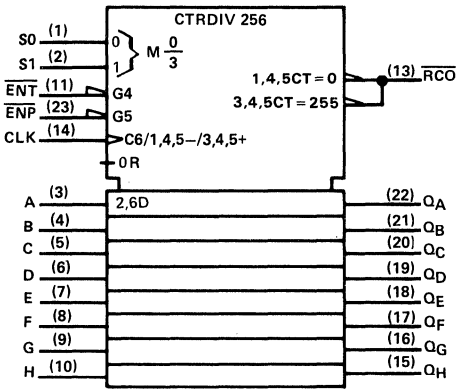
The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count enable inputs ($\overline{ENP}$ and $\overline{ENT}$) must be low to count. The direction of the count is determined by the levels of the select inputs (see Function Table). Input $\overline{ENT}$ is fed forward to enable the carry output. The ripple carry output thus enabled will produce a low-level pulse while the count is zero (all outputs low) counting down or 255 counting up (all outputs high). This low-level overflow carry pulse can be used to enable successive cascaded stages. Transitions at the enable $\overline{ENP}$ and $\overline{ENT}$ inputs are allowed regardless of the level of the clock input. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design.

These counters feature a fully independent clock circuit. With the exception of the asynchronous clear on the '867, changes at control inputs (S0, S1) that will modify the operating mode have no effect on the Q outputs until clocking occurs. Anytime the $\overline{ENP}$ and/or $\overline{ENT}$ is taken high, $\overline{RCO}$ will either go or remain high. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

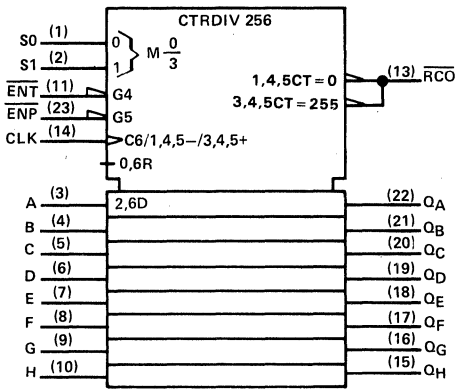
The SN54ALS' and SN54AS' families are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS' and SN74AS' families are characterized for operation from 0°C to 70°C.

logic symbols†

'ALS, 'AS867



'ALS, 'AS869



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

FUNCTION TABLE

S1	S0	FUNCTION
L	L	Clear
L	H	Count down
H	L	Load
H	H	Count up

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS', SN54AS' . . . . . −55°C to 125°C
SN74ALS', SN74AS' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

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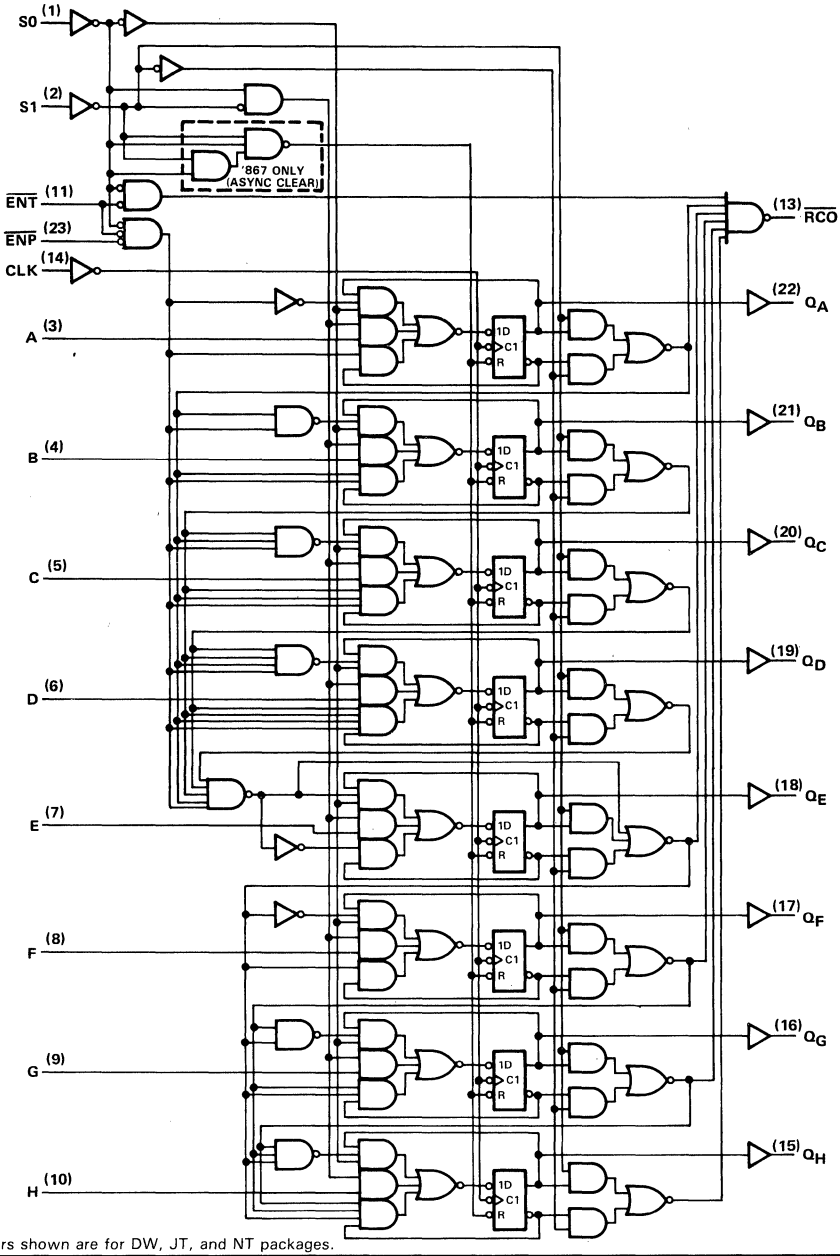
logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

recommended operating conditions

			SN54ALS867			SN74ALS867			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				8.0			8.0	mA
f_{clock}	Clock frequency		0		45	0		45	MHz
$t_{w(clock)}$	Duration								ns
$t_{w(clear)}$	Duration of clear pulse (S0 and S1 low)								ns
t_{su}	Setup time†	Data inputs A-H							ns
		Enable P ($\overline{ENP}$) or Enable T ($\overline{ENT}$)							ns
		S0 or S1 (load)							ns
		S0 or S1 (clear)							ns
		S0 or S1 (count down)							ns
		S0 or S1 (count up)							ns
t_h	Hold time at any input with respect to clock†								ns
t_{skew}	Skew time between S0 and S1 (maximum to avoid inadvertent clear)								ns
T_A	Operating free-air temperature		−55		125	0		70	°C

†This setup time is required to ensure stable data.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS867			SN74ALS867			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	$\overline{ENT}$	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	μA
	Other Inputs					20			20	
I_{IL}	$\overline{ENT}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.4			−0.4	mA
	Other inputs					−0.2			−0.2	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,			28.5			28.5		mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

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recommended operating conditions

			SN54ALS869			SN74ALS869			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−2			−2	mA
I_{OL}	Low-level output current				20			20	mA
f_{clock}	Clock frequency				40			45	MHz
$t_{w(clock)}$	Duration								ns
t_{su}	Setup time†	Data inputs A-H							ns
		Enable P ($\overline{ENP}$) or Enable T ($\overline{ENT}$)							ns
		S0 or S1 (load)							ns
		S0 or S1 (clear)							ns
		S0 or S1 (count down)							ns
		S0 or S1 (count up)							ns
t_h	Hold time at any input with respect to clock†								ns
T_A	Operating free-air temperature		−55		125	0		70	°C

†This setup time is required to ensure stable data.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS869			SN74ALS869			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	$\overline{ENT}$	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	μA
	Other Inputs					20			20	
I_{IL}	$\overline{ENT}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.4			−0.4	mA
	Other inputs					−0.2			−0.2	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,			28.5			28.5		mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS867 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 500 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS867			SN74ALS867			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}			45			45			MHz
t_{PLH}	CLK	$\overline{RCO}$		14			14		ns
t_{PHL}				13			13		
t_{PLH}	CLK	Any Q		10			10		ns
t_{PHL}				12			12		
t_{PLH}	$\overline{ENT}$	$\overline{RCO}$		7.5			7.5		ns
t_{PHL}				8.5			8.5		
t_{PLH}	$\overline{ENP}$	$\overline{RCO}$		11.5			11.5		ns
t_{PHL}				8.5			8.5		
t_{PHL}	Clear (S0, S1 low)	Any Q		17			17		ns
t_{PLH}	S0, S1 (count up/down)	$\overline{RCO}$		12			12		ns
t_{PHL}				13			13		
t_{PHL}	Clear (S0, S1 low)	$\overline{RCO}$		22			22		ns

'ALS869 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 500 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS869			SN74ALS869			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}			45			45			MHz
t_{PLH}	CLK	$\overline{RCO}$		14			14		ns
t_{PHL}				13			13		
t_{PLH}	CLK	Any Q		10			10		ns
t_{PHL}				12			12		
t_{PLH}	$\overline{ENT}$	$\overline{RCO}$		7.5			7.5		ns
t_{PHL}				8.5			8.5		
t_{PLH}	$\overline{ENP}$	$\overline{RCO}$		11.5			11.5		ns
t_{PHL}				8.5			8.5		
t_{PLH}	S0, S1 (count up/down)	$\overline{RCO}$		12			12		ns
t_{PHL}				13			13		
t_{PHL}	Clear (S0, S1 low)	$\overline{RCO}$		22			22		ns
t_{PHL}	Clear (S0, S1 low)	Any Q		17			17		ns

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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recommended operating conditions

			SN54AS867			SN74AS867			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−2	mA
I_{OL}	Low-level output current				20			20	mA
f_{clock}	Clock frequency		0		40	0		50	MHz
$t_{w(clock)}$	Duration		12.5			10			ns
$t_{w(clear)}$	Duration of clear pulse (S0 and S1 low)		12.5			10			ns
t_{su}	Setup time†	Data inputs A-H	5			4			ns
		Enable P ($\overline{ENP}$) or Enable T ($\overline{ENT}$)	9			8			ns
		S0 or S1 (load)	11			10			ns
		S0 or S1 (clear)	11			10			ns
		S0 or S1 (count down)	42			40			ns
		S0 or S1 (count up)	42			40			ns
t_h	Hold time at any input with respect to clock†		0			0			ns
t_{skew}	Skew time between S0 and S1 (maximum to avoid inadvertent clear)		8			7			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

†This setup time is required to ensure stable data.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS867			SN74AS867			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.34	0.5		0.34	0.5	V
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	$\overline{ENT}$	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	μA
	Other inputs					20			20	
I_{IL}	$\overline{ENT}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−4			−4	mA
	Other inputs					−2			−2	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V			134	195		134	195	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

recommended operating conditions

			SN54AS869			SN74AS869			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−2	mA
I_{OL}	Low-level output current				20			20	mA
f_{clock}	Clock frequency		0		40	0		45	MHz
$t_{w(clock)}$	Duration		12.5			11			ns
t_{su}	Setup time†	Data inputs A-H	6			5			ns
		Enable P ($\overline{ENP}$) or Enable T ($\overline{ENT}$)	10			9			ns
		S0 or S1 (load)	13			11			ns
		S0 or S1 (clear)	13			11			ns
		S0 or S1 (count down)	52			50			ns
		S0 or S1 (count up)	52			50			ns
t_h	Hold time at any input with respect to clock†		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

†This setup time is required to ensure stable data.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS869			SN74AS869			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC} 2			V_{CC} 2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.34	0.5		0.34	0.5	V
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	$\overline{ENT}$	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	μA
	Other inputs					20			20	
I_{IL}	$\overline{ENT}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−4			−4	mA
	Other inputs					−2			−2	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V			125	180		125	180	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

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'AS867 switching characteristics (see note 1)

PARAMETER	FROM (INPUT	TO OUTPUT	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS867		SN74AS867		
			MIN	MAX	MIN	MAX	
f_{max}			40		50		MHz
t_{PLH}	CLK	$\overline{RCO}$	5	31	5	22	ns
t_{PHL}			6	19	6	16	
t_{PLH}	CLK	Any Q	3	12	3	11	ns
t_{PHL}			4	16	4	15	
t_{PLH}	$\overline{ENT}$	$\overline{RCO}$	3	19	3	10	ns
t_{PHL}			5	21	5	17	
t_{PLH}	$\overline{ENP}$	$\overline{RCO}$	5	14	5	14	ns
t_{PHL}			5	21	5	17	
t_{PHL}	Clear (S0, S1 low)	Any Q	7	23	7	21	ns

'AS869 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω T_A = MIN to MAX				UNIT
			SN54AS869		SN74AS869		
			MIN	MAX	MIN	MAX	
f_{max}			40		45		MHz
t_{PLH}	CLK	$\overline{RCO}$	6	35	6	35	ns
t_{PHL}			6	20	6	18	
t_{PLH}	CLK	Any Q	3	12	3	11	ns
t_{PHL}			4	16	4	15	
t_{PLH}	$\overline{ENT}$	$\overline{RCO}$	3	25	3	15	ns
t_{PHL}			6	21	6	17	
t_{PLH}	$\overline{ENP}$	$\overline{RCO}$	5	27	5	19	ns
t_{PHL}			6	21	6	18	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

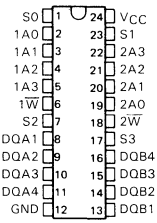
- **'ALS870 and 'AS870 in 24-Pin Small Outline, 300-mil DIP and Both Plastic and Ceramic 28-Pin Chip Carriers**
- **'ALS871 and 'AS871 in 28-Pin 600-mil DIP and Both Plastic and Ceramic Chip Carriers**
- **3-State Buffer-Type Outputs Drive Bus Lines Directly**
- **Typical Access Time:**
  'ALS is 16 ns
  'AS is 11 ns
- **Each Register File Has Individual Write Enable Controls and Address Lines**
- **Designed Specifically for Multibus Architecture and Overlapping File Operations**
- **Prioritized B Input Port Prevents Write Conflicts During Dual Input Mode**
- **Dependable Texas Instruments Quality and Reliability**

description

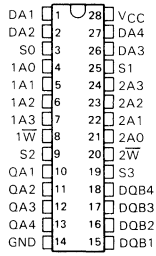
These devices feature two 16-word by 4-bit register files. Each register file has individual write-enable controls and address lines. The 'AS870 has two 4-bit data I/O ports (DQA1-DQA4 and DQB1-DQB4). The 'AS871 has one 4-bit data I/O port (DQB1-DQB4) with the other data port having individual data inputs (DA1-DA4) and data outputs (QA1-QA4). The data I/O ports can output to Bus A and Bus B, receive input from Bus A and Bus B, receive input from Bus A and output to Bus B, or output to Bus A and receive input from Bus B. To prevent writing conflicts in the dual-input mode, the B input port takes priority. Two select lines, S0 and S1, control which port has access to which register. S2 determines whether the A ports are in the input or the output modes and S3 does likewise for the B ports. The address lines (1A0-1A3 or 2A0-2A3) are decoded by an internal 1-of-16 decoder to select which register word is to be accessed. All outputs are 3-state buffer-type outputs designed specifically to drive bus lines directly.

The SN54ALS' and SN54AS' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS' and SN74AS' family is characterized for operation from 0°C to 70°C.

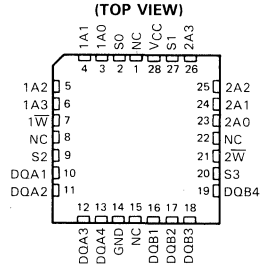
SN54ALS870, SN54AS870 . . . JT PACKAGE
SN74ALS870, SN74AS870 . . . DW OR NT PACKAGE
(TOP VIEW)



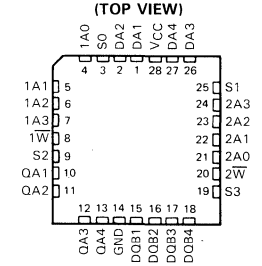
SN54ALS871, SN54AS871 . . . JD PACKAGE
SN74ALS871, SN74AS871 . . . N PACKAGE
(TOP VIEW)



SN54ALS870, SN54AS870 . . . FK PACKAGE
SN74ALS870, SN74AS870 . . . FN PACKAGE
(TOP VIEW)



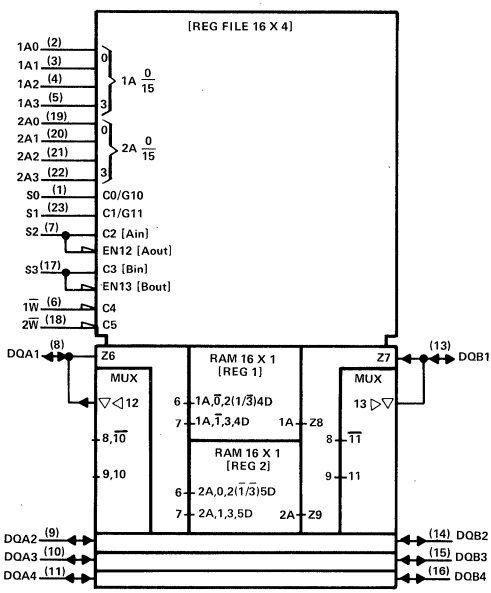
SN54ALS871, SN54AS871 . . . FK PACKAGE
SN74ALS871, SN74AS871 . . . FN PACKAGE
(TOP VIEW)



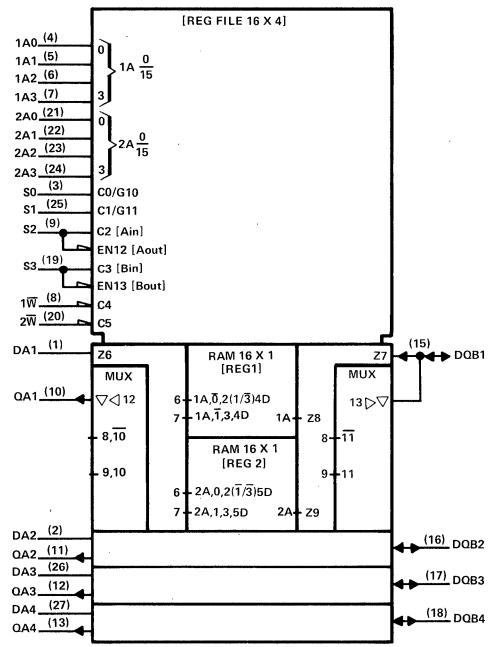
NC – No internal connection

logic symbols†

'ALS870, 'AS870

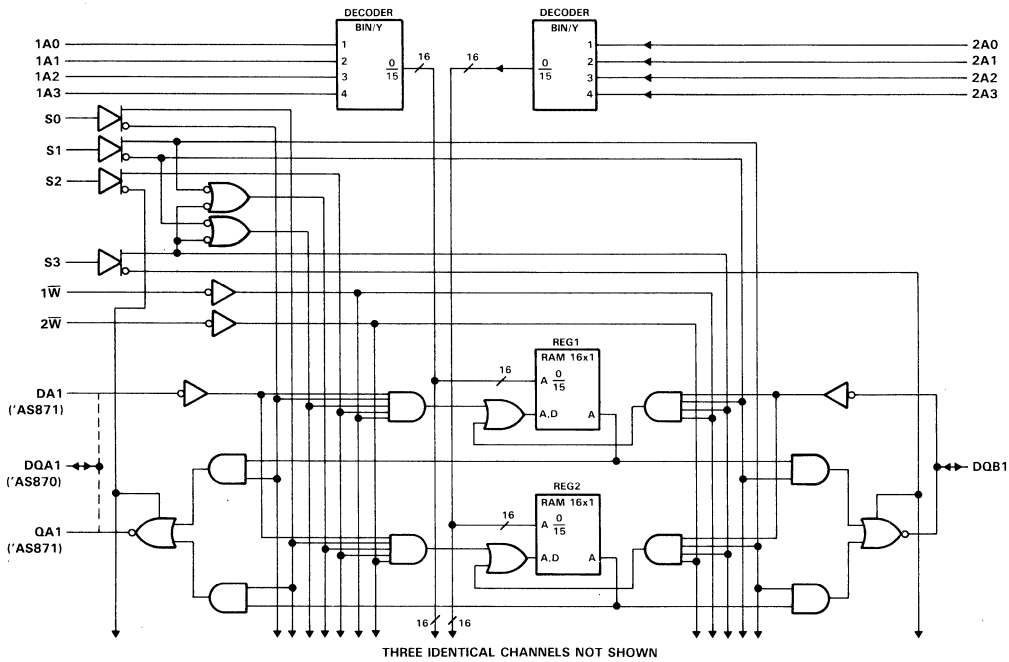


'ALS871, 'AS871



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

logic diagram (positive logic)



FUNCTION TABLE

FILE SELECT			INPUT/OUTPUT		
S0	S1	FILE SEL	S2	S3	I/O SEL
L	L	1R TO A, 1R TO B	L	L	A OUT, B OUT
H	L	2R TO A, 1R TO B			
L	H	1R TO A, 2R TO B			
H	H	2R TO A, 2R TO B			
L	L	A TO 1R, 1R TO B	H	L	A IN, B OUT
H	L	A TO 2R, 1R TO B			
L	H	A TO 1R, 2R TO B			
H	H	A TO 2R, 2R TO B			
L	L	1R TO A, B TO 1R	L	H	A OUT, B IN
H	L	2R TO A, B TO 1R			
L	H	1R TO A, B TO 2R			
H	H	2R TO A, B TO 2R			
L	L	B TO 1R	H	H	A IN, B IN
H	L	A TO 2R, B TO 1R			
L	H	A TO 1R, B TO 2R			
H	H	B TO 2R			

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS870, SN54ALS871 . . . . . −55°C to 125°C
SN74ALS870, SN74ALS871 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS870 SN54ALS871			SN74ALS870 SN74ALS871			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−1			−2.6	mA
I_{OL}	Low-level output current				12			24	mA
t_w	Duration of write pulse			10			10		ns
t_{su}	Setup times	Address before write↓		2			2		ns
		Data before write↑		4			4		
		Select before write↓		3.5			3.5		
t_h	Hold times	Address after write↑		0			0		ns
		Data after write↑		0			0		
		Select after write↓		0			0		
T_A	Operating free-air temperature		−55		125	0		70	°C

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'ALS870 electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS870			SN74ALS870			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.2					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	DQA and DQB ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.2			0.2	
I_{IH}	1$\overline{W}$ and 2$\overline{W}$	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
	Other control inputs					40			40	
	DQA and DQB ports‡					50			50	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
	DQA and DQB ports‡					−0.2			−0.2	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V			70.5			70.5		mA

'ALS871 electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS871			SN74ALS871			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.2					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	QA outputs	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	µA
I_{OZL}	QA outputs	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	µA
I_I	Control and DA inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	DQB ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.2			0.2	
I_{IH}	1$\overline{W}$, 2$\overline{W}$, and DA inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
	Other control inputs					40			40	
	DQB ports‡					50			50	
I_{IL}	Control and DA inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
	DQB ports‡					−0.2			−0.2	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V			70.5			70.5		mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit current, I_{OS}.

'ALS870 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 500 pF, R_1 = 500 Ω, R_2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS870			SN74ALS870			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
$t_{a(A)}$	Any A	Any DQ		11.5			11.5		ns
$t_{a(S)}$	S0	Any DQA		16			16		ns
	S1	Any DQB		16			16		
t_{dis}	S2	Any DQA		9.5			9.5		ns
	S3	Any DQB		9.5			9.5		
t_{en}	S2	Any DQA		7.5			7.5		ns
	S3	Any DQB		7.5			7.5		
t_{pd}	$\overline{W}$	Any DQ		12.5			12.5		ns
	DQA	DQB		16.5			16.5		
	DQB	DQA		16.5			16.5		

'ALS871 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 500 pF, R_1 = 500 Ω, R_2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS871			SN74ALS871			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
$t_{a(A)}$	Any A	Any QA or DQB		11.5			11.5		ns
$t_{a(S)}$	S0	Any QA		16			16		ns
	S1	Any DQB		16			16		
t_{dis}	S2	Any QA		9.5			9.5		ns
	S3	Any DQB		9.5			9.5		
t_{en}	S2	Any QA		7.5			7.5		ns
	S3	Any DQB		7.5			7.5		
t_{pd}	$\overline{W}$	Any QA or DQB		12.5			12.5		ns
	DA	DQB		16.5			16.5		
	DQB	QA		16.5			16.5		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54AS870, SN54AS871 . . . . . −55°C to 125°C
SN74AS870, SN74AS871 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54AS870 SN54AS871			SN74AS870 SN74AS871			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−12			−15	mA
I_{OL}	Low-level output current				32			48	mA
t_w	Duration of write pulse		12			12			ns
t_{su}	Setup times	Address before write↓	5			5			ns
		Data before write↑	15			15			
		Select before write↓	12			12			
t_h	Hold times	Address after write↑	0			0			ns
		Data after write↑	0			0			
		Select after write↑	12			12			
T_A	Operating free-air temperature		−55		125	0		70	°C

'AS870 electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS870			SN74AS870			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC} − 2			V_{CC} − 2			V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2					
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	DQA and DQB ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.2			0.2	
I_{IH}	$1\overline{W}$ and $2\overline{W}$	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	Other control inputs					40			40	
	DQA and DQB ports‡					50			50	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−2			−2	mA
	DQA and DQB ports‡					−2			−2	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V			120	190		120	190	mA

'AS871 electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS871			SN74AS871			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC} − 2			V_{CC} 2			V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2					
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}	QA outputs	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}	QA outputs	V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I	Control and DA inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	DQB ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.2			0.2	
I_{IH}	$1\overline{W}$, $2\overline{W}$, and DA inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	Other control inputs					40			40	
	DQB ports‡					50			50	
I_{IL}	Control and DA inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−2			−2	mA
	DQB ports‡					−2			−2	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V			120	190		120	190	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit current, I_{OS}.

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'AS870 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS870		SN74AS870		
			MIN	MAX	MIN	MAX	
$t_{a(A)}$	Any A	Any DQ	5	20	5	15	ns
$t_{a(S)}$	S0	Any DQA	3	15	3	13	ns
	S1	Any DQB	3	15	3	13	
t_{dis}	S2	Any DQA	3	12	3	11	ns
	S3	Any DQB	3	12	3	11	
t_{en}	S2	Any DQA	3	15	3	12	ns
	S3	Any DQB	3	15	3	12	
t_{pd}	$\overline{W}$	Any DQ	5	23	5	19	ns
	DQA	DQB	5	25	5	22	
	DQB	DQA	5	25	5	22	

'AS871 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS871		SN74AS871		
			MIN	MAX	MIN	MAX	
$t_{a(A)}$	Any A	Any QA or DQB	5	20	5	16	ns
$t_{a(S)}$	S0	Any QA	3	15	3	13	ns
	S1	Any DQB	3	15	3	13	
t_{dis}	S2	Any QA	3	12	3	11	ns
	S3	Any DQB	3	12	3	11	
t_{en}	S2	Any QA	3	15	3	12	ns
	S3	Any DQB	3	15	3	12	
t_{pd}	$\overline{W}$	Any QA or DQB	5	23	5	19	ns
	DA	DQB	5	26	5	23	
	DQB	QA	5	26	5	23	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2661, APRIL 1982 – REVISED MAY 1986

- **3-State Buffer-Type Outputs Drive Bus-Lines Directly**
- **Bus-Structured Pinout**
- **'ALS880A and 'AS880 are Alternative Versions with Inverting Outputs**
- **Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These dual 4-bit registers feature three-state outputs designed specifically for bus driving. This makes these devices particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

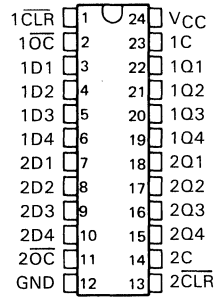
The dual 4-bit latches are transparent D-type. When the latch enable input (1C or 2C) is high, the Q outputs will follow the data (D) inputs in true form, according to the function table. When the latch enable input is taken low, the outputs will be latched. When $\overline{CLR}$ goes low, the Q outputs go low independently of enable C. The outputs are in a high-impedance state when $\overline{OC}$ (output control) is at a high logic level.

The SN54ALS873B and SN54AS873 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS873B and SN74AS873 are characterized for operation from 0°C to 70°C.

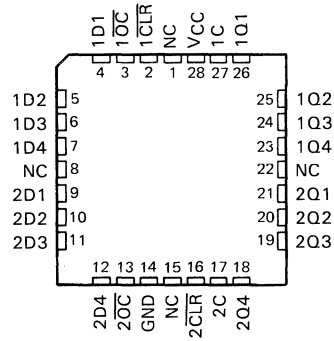
FUNCTION TABLE (EACH LATCH)

INPUTS				OUTPUT
$\overline{OC}$	$\overline{CLR}$	ENABLE C	D	Q
L	L	X	X	L
L	H	H	H	H
L	H	H	L	L
L	H	L	X	Q_0
H	X	X	X	Z

SN54ALS873B, SN54AS873 . . . JT PACKAGE
SN74ALS873B, SN74AS873 . . . DW OR NT PACKAGE
(TOP VIEW)

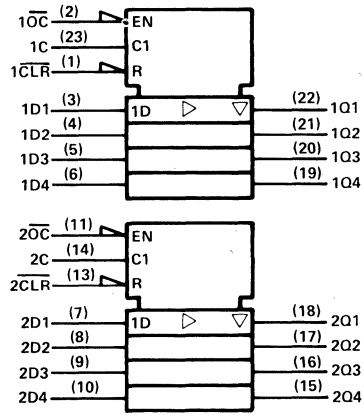


SN54ALS873B, SN54AS873 . . . FK PACKAGE
SN74ALS873B, SN74AS873 . . . FN PACKAGE
(TOP VIEW)



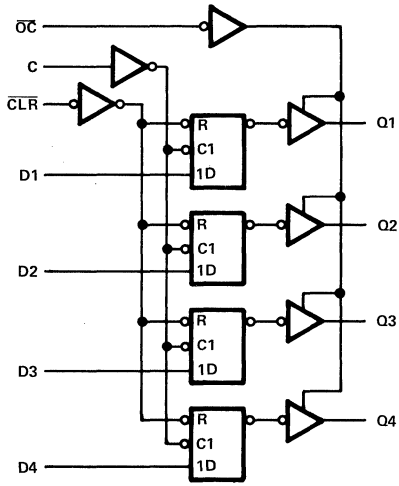
NC—No internal connection

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

logic diagram (each quad latch, positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS873B, SN54AS873 . . . . . −55°C to 125°C
SN74ALS873B, SN74AS873 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS873B			SN74ALS873B			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−1			−2.6	mA
I_{OL}	Low-level output current				12			24	mA
t_w	Pulse duration	$\overline{CLR}$ low	15			15			ns
		Enable C high	10			10			
t_{su}	Setup time, data before enable C↓		10			10			ns
t_h	Hold time, data after enable C↓		7			7			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS873B			SN74ALS873B			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		11	21		11	21	mA
		Outputs low		16	29		16	29	
		Outputs disabled		20	31		20	31	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS873B			SN54ALS873B		SN74ALS873B		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q		7	11	2	17	2	14	ns
t_{PHL}				7	10	2	15	2	14	
t_{PLH}	C	Q		13	17	8	29	8	22	ns
t_{PHL}				14	18	8	26	8	21	
t_{PHL}	$\overline{CLR}$	Q		12	16	6	24	6	20	ns
t_{PZH}	$\overline{OC}$	Q		11	14	4	22	4	18	ns
t_{PZL}				11	15	4	23	4	18	
t_{PHZ}	$\overline{OC}$	Q		7	9	2	12	2	10	ns
t_{PLZ}				7	11	2	21	2	15	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

recommended operating conditions

			SN54AS873			SN74AS873			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−12			−15	mA
I_{OL}	Low-level output current				32			48	mA
t_w	Pulse duration	$\overline{CLR}$ low	4.5			3.5			ns
		Enable C high	5.5			4.5			
t_{su}	Setup time, data before enable C↓		2			2			ns
t_h	Hold time, data after enable C↓		3			3			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS873			SN74AS873			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2					
	V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4	3.3		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5				V
	V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		68	110		68	110	mA
		Outputs low		67	109		67	109	
		Outputs disabled		80	129		80	129	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS873		SN74AS873		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	3	9	3	6	ns
t_{PHL}			3	7	3	6	
t_{PLH}	C	Q	6	14	6	11.5	ns
t_{PHL}			4	9	4	7.5	
t_{PHL}	$\overline{CLR}$	Q	3	8.5	3	7.5	ns
t_{PZH}	$\overline{OC}$	Q	2	8	2	6.5	ns
t_{PZL}			4	11	4	9.5	
t_{PHZ}	$\overline{OC}$	Q	2	8	2	6.5	ns
t_{PLZ}			2	8.5	2	7.5	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

- **3-State Buffer-Type Outputs Drive Bus-Lines Directly**
- **Bus-Structured Pinout**
- **Choice of True or Inverting Logic**
  'ALS874B, 'AS874 True Outputs
  'ALS876A, 'AS876 Inverting Outputs
- **Asynchronous Clear**
- **Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

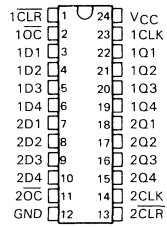
description

These dual four-bit registers feature three-state outputs designed specifically for bus driving. This makes these devices paricularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

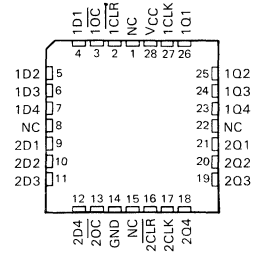
The edge-triggered flip-flops enter data on the low-to-high transition of the clock. The 'ALS874B and 'AS874 have $\overline{CLR}$ inputs and noninverting Q outputs; the 'ALS876A and 'AS876 have $\overline{PRE}$ inputs and inverting Q outputs. In each case, taking this input low causes the four Q or $\overline{Q}$ outputs to go low independently of the clock.

The SN54ALS' and SN54AS' devices are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS' and SN74AS' devices are characterized for operation from 0°C to 70°C.

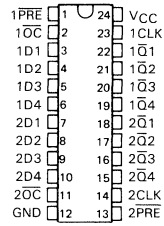
SN54ALS874B, SN54AS874 . . . JT PACKAGE
SN74ALS874B, SN74AS874 . . . DW OR NT PACKAGE
(TOP VIEW)



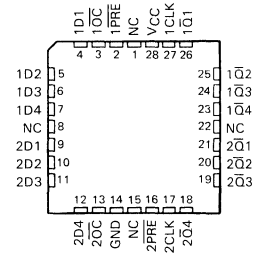
SN54ALS874B, SN54AS874 . . . FK PACKAGE
SN74ALS874B, SN74AS874 . . . FN PACKAGE
(TOP VIEW)



SN54ALS876A, SN54AS876 . . . JT PACKAGE
SN74ALS876A, SN74AS876 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54ALS876A, SN54AS876 . . . FK PACKAGE
SN74ALS876A, SN74AS876 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

FUNCTION TABLES

'ALS874B, 'AS874 (EACH FLIP-FLOP)

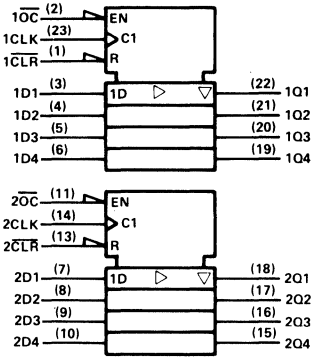
INPUTS				OUTPUT
$\overline{OC}$	$\overline{CLR}$	CLK	D	Q
L	L	X	X	L
L	H	↑	H	H
L	H	↑	L	L
L	H	L	X	Q_0
H	X	X	X	Z

'ALS876A, 'AS876 (EACH FLIP-FLOP)

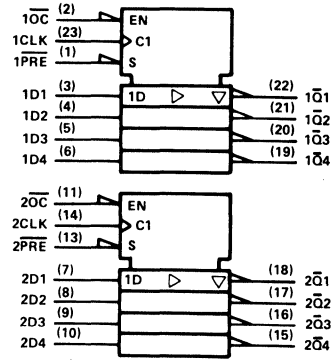
INPUTS				OUTPUT
OC	$\overline{PRE}$	CLK	D	$\overline{Q}$
L	L	X	X	L
L	H	↑	H	L
L	H	↑	L	H
L	H	L	X	$\overline{Q}_0$
H	X	X	X	Z

logic symbols†

'ALS874B, 'AS874



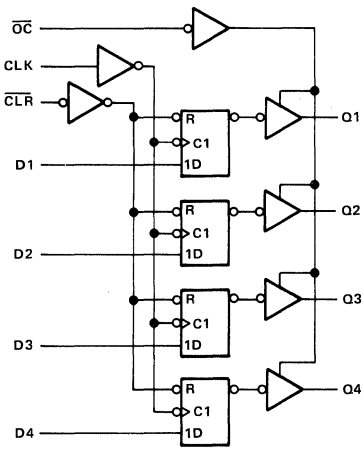
'ALS876A, 'AS876



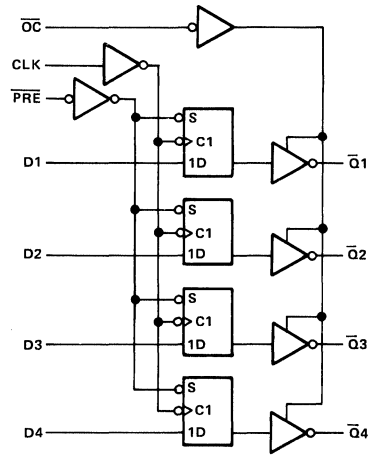
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617.12.

logic diagrams (positive logic)

'ALS874B, 'AS874 (EACH QUAD FLIP-FLOP)



'ALS876A, 'AS876 (EACH QUAD FLIP-FLOP)



Pin numbers shown are for DW, JT, and NT packages.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS874B, SN54ALS876A . . . . . −55°C to 125°C
SN74ALS874B, SN74ALS876A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS874B SN54ALS876A			SN74ALS874B SN74ALS876A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−1			−2.6	mA
I_{OL}	Low-level output current				12			24	mA
f_{clock}	Clock frequency		0		25	0		30	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	10			10			ns
		CLK high	20			16.5			
		CLK low	20			16.5			
t_{su}	Setup time before CLK↑	Data	15			15			ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	10			10			
t_h	Hold time, data after CLK↑		4			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS874B SN54ALS876A			SN74ALS874B SN74ALS876A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS874B	V_{CC} = 5.5 V	Output high		14	21		14	21	mA
			Outputs low		19	30		19	30	
			Outputs disabled		20	32		20	32	
	'ALS876A		Outputs high		14	21		14	21	
			Outputs low		18	29		18	29	
			Outputs disabled		20	31		20	31	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS874B switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS874B			SN54ALS874B		SN74ALS874B		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			40	50		25		30		MHz
t_{PLH}	CLK	Any Q		8	10	4	15	4	14	ns
t_{PHL}				8	13	4	15	4	14	
t_{PHL}	$\overline{CLR}$	Any Q		11	14	5	20	5	17	ns
t_{PZH}	$\overline{OC}$	Any Q		9	12	4	21	4	18	ns
t_{PZL}				11	15	4	21	4	18	
t_{PHZ}	$\overline{OC}$	Any Q		6	8	2	12	2	10	ns
t_{PLZ}				5.7	8	3	15	3	12	

'ALS876A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_1 = 500 Ω, R_2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 C to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS876A			SN54ALS876A		SN74ALS876A		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			40	50		25		30		MHz
t_{PLH}	CLK	Any $\overline{Q}$		8	11	4	15	4	14	ns
t_{PHL}				9	12	4	15	4	14	
t_{PHL}	$\overline{PRE}$	Any $\overline{Q}$		10	16	6	22	6	19	ns
t_{PZH}	$\overline{OC}$	Any $\overline{Q}$		10	13	4	21	4	18	ns
t_{PZL}				11	15	4	21	4	18	
t_{PHZ}	$\overline{OC}$	Any $\overline{Q}$		6	8	2	12	2	10	ns
t_{PLZ}				7	10	3	15	3	13	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS874, SN54AS876 . . . . . −55°C to 125°C
SN74AS874, SN74AS876 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54AS874 SN54AS876			SN74AS874 SN74AS876			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−12			−15	mA
I_{OL}	Low-level output current				32			48	mA
f_{clock}	Clock frequency		0		100	0		125	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	4			2			ns
		CLK high	4			3			
		CLK low	5			4			
t_{su}	Setup time before CLK↑	Data	2.5			2			ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	5			4			
t_h	Hold time, data after CLK↑		1			1			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS874 SN54AS876			SN74AS874 SN74AS876			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2					
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4	3.3		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.4				V
		V_{CC} = 4.5 V	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			10	μA
I_{IL}	D	V_{CC} = 5.5 V,	V_I = 0.4 V			−3			−2	mA
	All other					−0.5			−0.5	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'AS874	V_{CC} = 5.5 V	Output high		82	133		82	133	mA
			Outputs low		92	149		92	149	
			Outputs disabled		100	160		100	160	
	'AS876		Outputs high		88	142		88	142	
			Outputs low		94	150		94	150	
			Outputs disabled		100	160		100	160	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'AS874 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS874		SN74AS874		
			MIN	MAX	MIN	MAX	
f_{max}			100		125		MHz
t_{PLH}	CLK	Any Q	3	11.5	3	8.5	ns
t_{PHL}			4	12.5	4	10.5	
t_{PHL}	$\overline{CLR}$	Any Q	4	11	4	9.5	ns
t_{PZH}	$\overline{OC}$	Any Q	2	8	2	7	ns
t_{PZL}			3	11.5	3	10.5	
t_{PHZ}	$\overline{OC}$	Any Q	2	7	2	6	ns
t_{PLZ}			2	8.5	2	7.5	

'AS876 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS876		SN74AS876		
			MIN	MAX	MIN	MAX	
f_{max}			100		125		MHz
t_{PLH}	CLK	Any $\overline{Q}$	3	11.5	3	8.5	ns
t_{PHL}			4	12.5	4	10.5	
t_{PHL}	$\overline{PRE}$	Any $\overline{Q}$	4	11	4	9.5	ns
t_{PZH}	$\overline{OC}$	Any $\overline{Q}$	2	8	2	7	ns
t_{PZL}			3	11.5	3	10.5	
t_{PHZ}	$\overline{OC}$	Any $\overline{Q}$	2	7	2	6	ns
t_{PLZ}			2	7	2	6	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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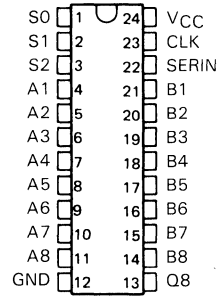
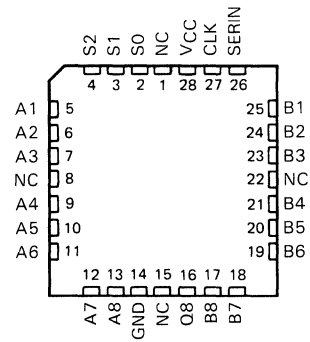
D2661, DECEMBER 1982—REVISED AUGUST 1985

- **Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Buffered 3-State Outputs Drive Bus Lines Directly**
- **Cascaded to n-Bits**
- **Eight Selectable Transceiver/Port Functions:**
  - **A to B or B to A**
  - **Register to A or Register to B**
  - **Shifted to A or Shifted to B**
  - **Off-Line Shifts (A and B Ports in High-Impedance State)**
  - **Register Clear**
- **Particularly Suitable for Use in Signature-Analysis Circuitry**
- **Serial Register Provides:**
  - **Parallel Storage of Either A or B Input Data**
  - **Serial Transmission of Data from Either A or B Port**
- **Dependable Texas Instruments Quality and Reliability**

SN54AS877 . . . JT PACKAGE
SN74AS877 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54AS877....FK PACKAGE
SN74AS877....FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

The 'AS877 features two 8-bit I/O ports (A1-A8 and B1-B8), an 8-bit parallel-load, serial-in, parallel-out shift register, and control logic. With these features, this device is capable of performing eight selectable transceiver or port functions, depending on the state of the three select lines S0, S1, and S2. These functions include: transferring data from port A to port B or vice versa (i.e., the transceiver function), transferring data from the register to either port, serial shifting data to either port, performing off-line shifts (with A and B ports in high-impedance state), and clearing the register. Synchronous parallel loading of the internal register can be accomplished from either port on the positive transition of the clock while serially shifting data in via the SERIN input. The 'AS877 is ideally suited for applications needing signature-analysis circuitry to enhance system verification and/or fault analysis. All serial data is shifted right. All outputs are buffer-type outputs designed specifically to drive bus lines directly and all are 3-state except for Q8, which is a totem-pole output.

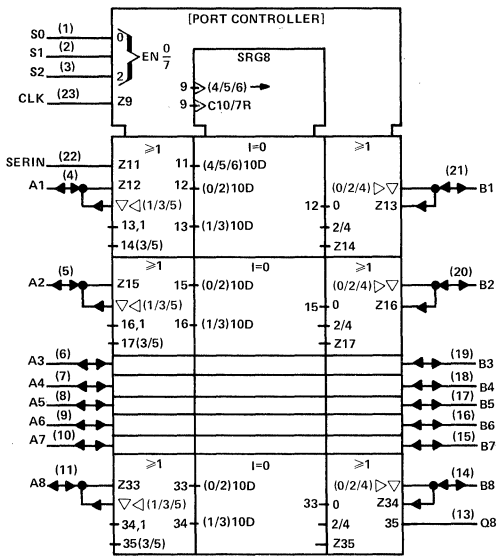
The SN54AS877 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS877 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

MODE S2 S1 S0	CLOCK	SERIN	A1 Q1 B1	A2 Q2 B2	A3 Q3 B3	A4 Q4 B4	A5 Q5 B5	A6 Q6 B6	A7 Q7 B7	A8 Q8 B8	PORT FUNCTION
L L L	H or L	X	Z Q_n A1	Z Q_n A2	Z Q_n A3	Z Q_n A4	Z Q_n A5	Z Q_n A6	Z Q_n A7	Z Q_n A8	A TO B
L L L	↑	X	Z A1 A1	Z A2 A2	Z A3 A3	Z A4 A4	Z A5 A5	Z A6 A6	Z A7 A7	Z A8 A8	
L L H	H or L	X	B1 Q_n Z	B2 Q_n Z	B3 Q_n Z	B4 Q_n Z	B5 Q_n Z	B6 Q_n Z	B7 Q_n Z	B8 Q_n Z	B TO A
L L H	↑	X	B1 B1 Z	B2 B2 Z	B3 B3 Z	B4 B4 Z	B5 B5 Z	B6 B6 Z	B7 B7 Z	B8 B8 Z	
L H L	H or L	X	X Q_n Q1	X Q_n Q2	X Q_n Q3	X Q_n Q4	X Q_n Q5	X Q_n Q6	X Q_n Q7	X Q_n Q8	Q_N TO B_N
L H L	↑	X	Z A1 A1	Z A2 A2	Z A3 A3	Z A4 A4	Z A5 A5	Z A6 A6	Z A7 A7	Z A8 A8	
L H H	H or L	X	Q1 Q_n X	Q2 Q_n X	Q3 Q_n X	Q4 Q_n X	Q5 Q_n X	Q6 Q_n X	Q7 Q_n X	Q8 Q_n X	Q_N TO A_N
L H H	↑	X	B1 B1 Z	B2 B2 Z	B3 B3 Z	B4 B4 Z	B5 B5 Z	B6 B6 Z	B7 B7 Z	B8 B8 Z	
H L L	H or L	X	Z Q_n Q1	Z Q_n Q2	Z Q_n Q3	Z Q_n Q4	Z Q_n Q5	Z Q_n Q6	Z Q_n Q7	Z Q_n Q8	SHIFT
H L L	↑	H	Z H H	Z Q1 Q1	Z Q2 Q2	Z Q3 Q3	Z Q4 Q4	Z Q5 Q5	Z Q6 Q6	Z Q7 Q7	TO
H L L	↑	L	Z L L	Z Q1 Q1	Z Q2 Q2	Z Q3 Q3	Z Q4 Q4	Z Q5 Q5	Z Q6 Q6	Z Q7 Q7	B
H L H	H or L	X	Q1 Q_n Z	Q2 Q_n Z	Q3 Q_n Z	Q4 Q_n Z	Q5 Q_n Z	Q6 Q_n Z	Q7 Q_n Z	Q8 Q_n Z	SHIFT
H L H	↑	H	H H Z	Q1 Q1 Z	Q2 Q2 Z	Q3 Q3 Z	Q4 Q4 Z	Q5 Q5 Z	Q6 Q6 Z	Q7 Q7 Z	TO
H L H	↑	L	L L Z	Q1 Q1 Z	Q2 Q2 Z	Q3 Q3 Z	Q4 Q4 Z	Q5 Q5 Z	Q6 Q6 Z	Q7 Q7 Z	A
H H L	H or L	X	Z Q_n Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	
H H L	↑	H	Z H Z	Z Q1 Z	Z Q2 Z	Z Q3 Z	Z Q4 Z	Z Q5 Z	Z Q6 Z	Z Q7 Z	SHIFT
H H L	↑	L	Z L Z	Z Q1 Z	Z Q2 Z	Z Q3 Z	Z Q4 Z	Z Q5 Z	Z Q6 Z	Z Q7 Z	
H H H	H or L	X	Z Q_n Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	CLEAR
H H H	↑	X	Z L Z	Z L Z	Z L Z	Z L Z	Z L Z	Z L Z	Z L Z	Z L Z	

n = level of Q_n(n = 1, 2...8) established on most recent ↑ transition of CLK. Q1 thru Q8 are the shift register outputs; only Q8 is available externally. The double inversions that take place as data travels from port to port are ignored in this table.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

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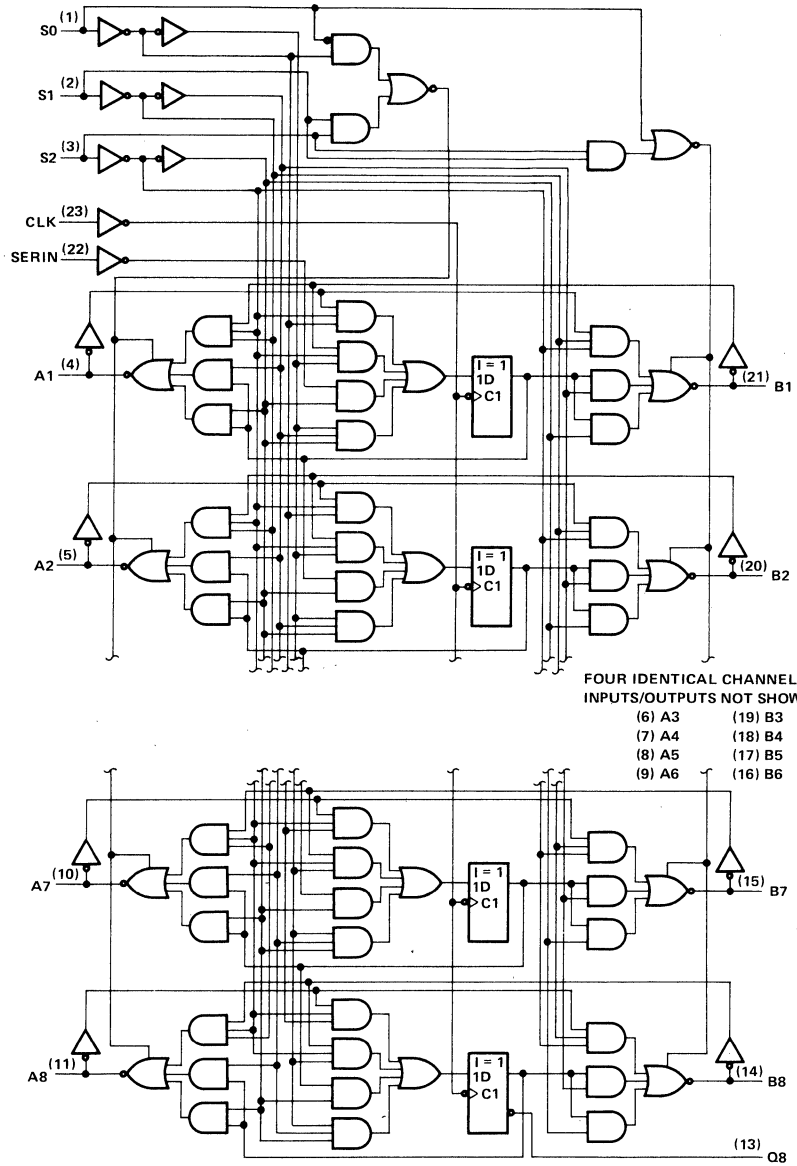
logic diagram (positive logic)



FOUR IDENTICAL CHANNELS NOT SHOWN
INPUTS/OUTPUTS NOT SHOWN:

(6) A3	(19) B3
(7) A4	(18) B4
(8) A5	(17) B5
(9) A6	(16) B6

Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over free-air temperature range

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54AS877 . . . . . −55°C to 125°C
SN74AS877 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54AS877			SN74AS877			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current	A1-A8, B1-B8			−12			−15	mA
		Q8			−2			−2	
I_{OL}	Low-level output current	A1-A8, B1-B8			32			48	mA
		Q8			20			20	
f_{clock}	Clock frequency		0		45	0		50	MHz
t_w	Duration of clock pulse		11			10			ns
t_{su}	Setup time before CLK↑	A1-A8, B1-B8 SERIN	5.5			5.5			ns
		S0, S1, S2	5.5			5.5			
t_h	Hold time, data after CLK↑	A1-A8, B1-B8 SERIN	0			0			ns
		S0, S1, S2	0			0			
T_A	Operating free-air temperature		−55		125	0		70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS877			SN74AS877			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	A1-A8	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2	3.2					V
	B1-B8	V_{CC} = 4.5 V,	I_{OH} = −15 mA				2	3.3		
	All outputs	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC} − 2			V_{CC} − 2			
V_{OL}	All outputs except Q8	V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
	Q8	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.25	0.5		0.25	0.5	
I_I	S0, S1, S2	V_{CC} = 5.5 V,	V_I = 7 V			0.3			0.3	mA
	CLK and SERIN					0.1			0.1	
	A1-A8, B1-B8	V_{CC} = 5.5 V,	V_I = 5.5 V			0.2			0.2	
I_{IH}	S0, S1, S2	V_{CC} = 5.5 V,	V_I = 2.7 V			60			60	μA
	CLK and SERIN					20			20	
	A1-A8, B1-B8‡					70			70	
I_{IL}	S0, S1, S2	V_{CC} = 5.5 V,	V_I = 0.4 V			−1			−1	mA
	CLK and SERIN					−0.5			−0.5	
	A1-A8, B1-B8‡					−0.75			−0.75	
I_O§	Except Q8	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
	Q8			−20		−112	−20		−112	
I_{CC}		V_{CC} = 5.5 V			136	220		136	220	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡For I/O ports, the parameters I_{IH} and I_{IL} include the output currents I_{OZH} and I_{OZL}, respectively.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

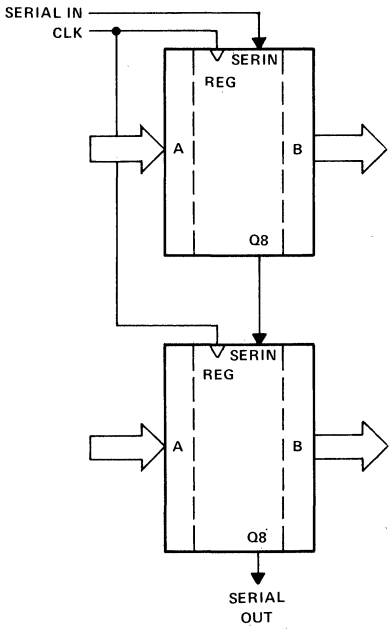
switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS877		SN74AS877		
			MIN	MAX	MIN	MAX	
f_{max}			45		50		MHz
t_{PLH}	Any A port	Any B port	2	8.5	2	7	ns
t_{PHL}			3	10.5	3	9	
t_{PLH}	Any B port	Any A port	2	9	2	7.5	ns
t_{PHL}			3	10.5	3	9	
t_{PLH}	S0, S1, S2¶	Any A or B port	3	11.5	3	10	ns
t_{PHL}			2	9.5	2	8	
t_{PLH}	CLK	Any A or B port	2	11	2	9	ns
t_{PHL}			3	13	3	11.5	
t_{PLH}	CLK	QB	2	10.5	2	8	ns
t_{PHL}			3	10	3	8.5	
t_{PHZ}	S0, S1, S2	Any A or B port	2	7.5	2	6.5	ns
t_{PLZ}			3	13	3	10.5	
t_{PZH}			2	9	2	7	ns
t_{PZL}			3	11.5	3	9.5	

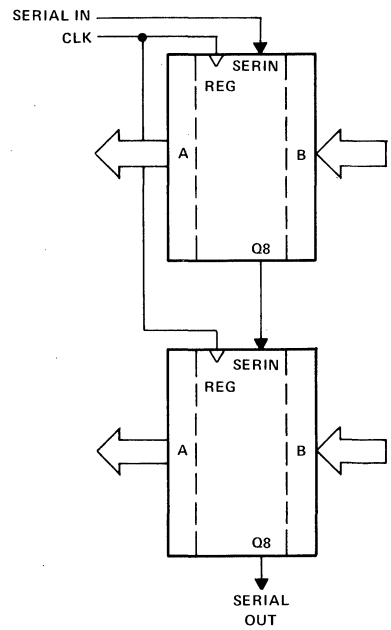
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.
¶The positive transition of S2 will cause low-level data at the A output Bus or stored in the shift register to be invalid for 12 ns.

TYPICAL APPLICATION DATA

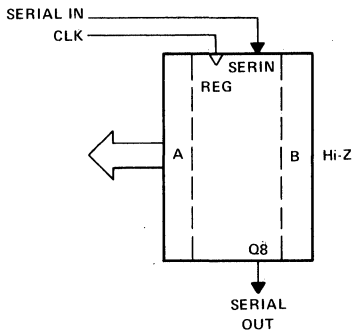
BUS A TO BUS B OR
SERIAL TRANSMISSION



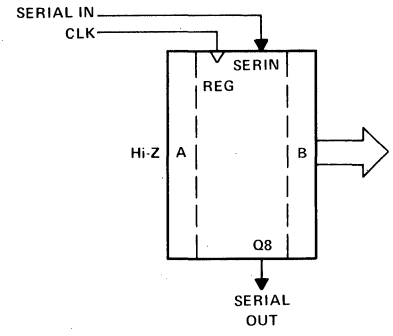
BUS B TO BUS A OR
SERIAL TRANSMISSION



SERIAL IN TO A PORT



SERIAL IN TO B PORT



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SN54ALS878A, SN54ALS879A, SN54AS878, SN54AS879
SN74ALS878A, SN74ALS879A, SN74AS878, SN74AS879
DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

D2661, APRIL 1982 REVISED MAY 1986

- **3-State Bus Driving Outputs**
- **Full Parallel-Access for Loading**
- **Buffered Control Inputs**
- **Choice of True or Inverting Logic**
  'ALS878A, 'AS878 True Outputs
  'ALS879A, 'AS879 Inverting Outputs
- **Synchronous Clear**
- **Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

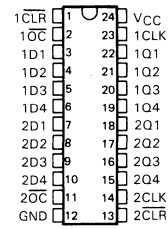
description

These dual 4-bit registers feature three-state outputs designed specifically for bus driving. This makes these devices particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

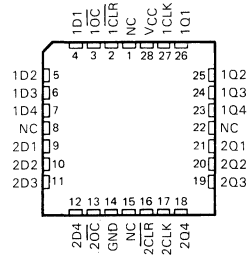
The dual 4-bit edge-triggered flip-flops enter data on the low-to-high transition of the clock (1CLK and 2CLK). All types have individual synchronous clear inputs and output control pins for each group of 4-bit registers.

The SN54ALS' and SN54AS' devices are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS' and SN74AS' devices are characterized for operation from 0°C to 70°C.

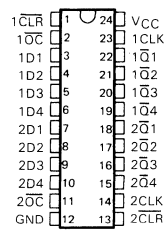
SN54ALS878A, SN54AS878 . . . JT PACKAGE
SN74ALS878A, SN74AS878 . . . DW OR NT PACKAGE
(TOP VIEW)



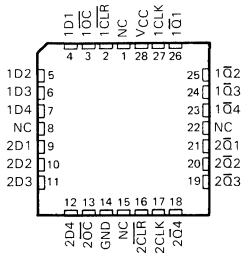
SN54ALS878A, SN54AS878 . . . FK PACKAGE
SN74ALS878A, SN74AS878 . . . FN PACKAGE
(TOP VIEW)



SN54ALS879A, SN54AS879 . . . JT PACKAGE
SN74ALS879A, SN74AS879 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54ALS879A, SN54AS879 . . . FK PACKAGE
SN74ALS879A, SN74AS879 . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLES

'ALS878A, 'AS878
(EACH FLIP-FLOP)

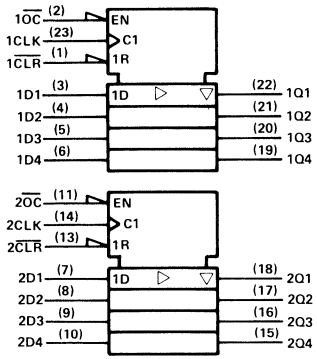
INPUTS				OUTPUT
$\overline{OC}$	$\overline{CLR}$	CLK	D	Q
L	L	↑	X	L
L	H	↑	H	H
L	H	↑	L	L
L	H	L	X	Q_0
H	X	X	X	Z

'ALS879A, 'AS879
(EACH FLIP-FLOP)

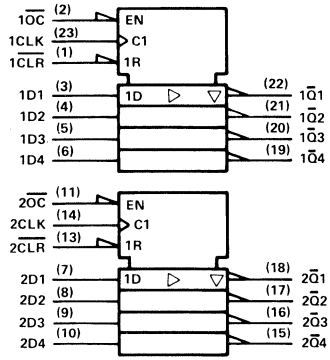
INPUTS				OUTPUT
$\overline{OC}$	$\overline{CLR}$	CLK	D	$\overline{Q}$
L	L	↑	X	H
L	H	↑	H	L
L	H	↑	L	H
L	H	L	X	Q_0
H	X	X	X	Z

logic symbols†

'ALS878A, 'AS878

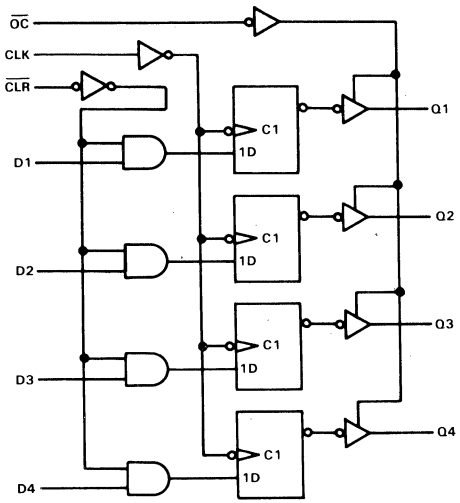


'ALS879A, 'AS879

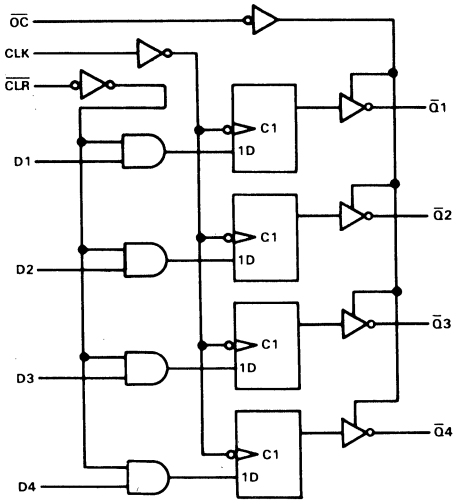


logic diagrams (positive logic)

'ALS878A, AS878 (EACH QUAD FLIP-FLOP)



'ALS879A, 'AS879 (EACH QUAD FLIP-FLOP)



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS878A, SN54ALS879A . . . . . −55°C to 125°C
SN74ALS878A, SN74ALS879A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS878A SN54ALS879A			SN74ALS878A SN74ALS879A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−1			−2.6	mA
I_{OL}	Low-level output current				12			24	mA
f_{clock}	Clock frequency	'ALS878A	0		25	0		30	MHz
		'ALS879A	0		20	0		25	
t_w	Pulse duration	'ALS878A CLK high or low	20			16.5			ns
		'ALS879A CLK high or low	25			20			
t_{su}	Setup time before CLK↑	Data	15			15			ns
		$\overline{CLR}$	20			20			
t_h	Hold time after CLK↑	Data	4			4			ns
		$\overline{CLR}$	0			0			
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS878A SN54ALS879A			SN74ALS878A SN74ALS879A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		14	23		14	23	mA
		Outputs low		18	31		18	31	
		Outputs disabled		20	33		20	33	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS878A 'ALS879A			SN54ALS878A SN54ALS879A		SN74ALS878A SN74ALS879A		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	'ALS878A		40	50		25		30		MHz
	'ALS879A		40	50		20		25		
t_{PLH}	CLK	Q or $\overline{Q}$		8	10	4	15	4	14	ns
t_{PHL}				9	13	4	17	4	16	
t_{PZH}	$\overline{OC}$	Q or $\overline{Q}$		9	13	4	22	4	20	ns
t_{PZL}				11	15	4	22	4	20	
t_{PHZ}	$\overline{OC}$	Q or $\overline{Q}$		6	8	2	12	2	10	ns
t_{PLZ}				7	10	3	18	3	15	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range SN54AS878, SN54AS879 . . . . . −55°C to 125°C
SN74AS878, SN74AS879 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54AS878 SN54AS879			SN74AS878 SN74AS879			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−12			−15	mA
I_{OL}	Low-level output current				32			48	mA
f_{clock}	Clock frequency		0		100	0		125	MHz
t_w	Pulse duration	CLK low	4			2			ns
		CLK high	5			4			
t_{su}	Setup time before CLK↑	Data	3			2			ns
		$\overline{CLR}$	6.5			5.5			
t_h	Hold time after CLK↑	Data	3			2			ns
		$\overline{CLR}$	0			0			
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS878 SN54AS879			SN74AS878 SN74AS879			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2					
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4	3.3		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.29	0.5				V
		V_{CC} = 4.5 V	I_{OL} = 48 mA					0.33	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	D	V_{CC} = 5.5 V,	V_I = 0.4 V			−3			−2	mA
	All other					−0.5			−0.5	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'AS878	V_{CC} = 5.5 V, See Note 1	Outputs high		82	132		82	132	mA
			Outputs low		96	155		96	155	
			Outputs disabled		100	160		100	160	
	'AS879		Outputs high		88	142		88	142	
			Outputs low		94	150		94	150	
			Outputs disabled		100	160		100	160	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with $\overline{CLR}$ and all D inputs grounded, and CLK and $\overline{OC}$ at 4.5 V.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS878 SN54AS879		SN74AS878 SN74AS879		
			MIN	MAX	MIN	MAX	
f_{max}			100		125		MHz
t_{PLH}	CLK	Q or $\overline{Q}$	3	11.5	3	8.5	ns
t_{PHL}			4	12.5	4	10.5	
t_{PZH}	$\overline{OC}$	Q or $\overline{Q}$	2	8	2	7	ns
t_{PZL}			3	11.5	3	10.5	
t_{PHZ}	$\overline{OC}$	Q or $\overline{Q}$	2	7	2	6	ns
t_{PLZ}			2	7	2	6	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

D2661, DECEMBER 1982 – REVISED MAY 1986

- **3-State Buffer-Type Outputs Drive Bus-Lines Directly**
- **Bus-Structured Pinout**
- **'ALS873B is Alternative Version with Noninverting Outputs**
- **Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

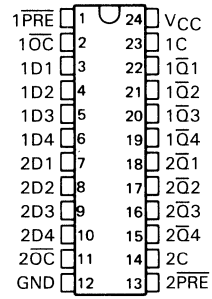
description

These dual 4-bit registers feature three-state outputs designed specifically for bus driving. This makes these devices particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

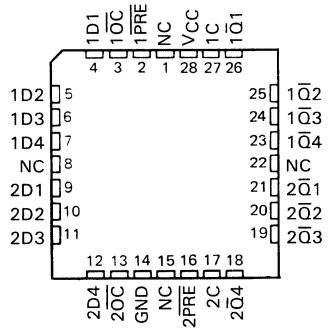
The dual 4-bit latches are transparent D-type. When the latch enable input (1C or 2C) is high, the $\overline{Q}$ outputs will follow the data (D) inputs in inverted form, according to the function table. When the latch enable input is taken low, the outputs will be latched. When $\overline{PRE}$ goes low, the $\overline{Q}$ outputs go low independently of the clock. The outputs are in a high-impedance state when $\overline{OC}$ (output control) is at a high logic level.

The SN54ALS880A and SN54AS880 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS880A and SN74AS880 are characterized for operation from 0°C to 70°C.

SN54ALS880A, SN54AS880 . . . JT PACKAGE
SN74ALS880A, SN74AS880 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54ALS880A, SN54AS880 . . . FK PACKAGE
SN74ALS880A, SN74AS880 . . . FN PACKAGE
(TOP VIEW)

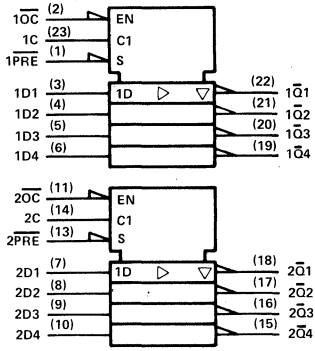


NC—No internal connection

FUNCTION TABLES (EACH LATCH)

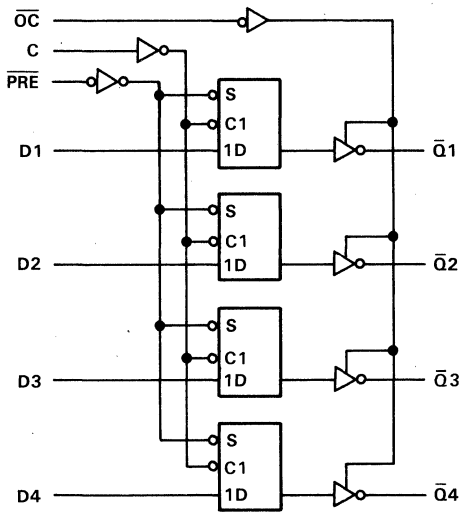
INPUTS				OUTPUT
$\overline{OC}$	$\overline{PRE}$	ENABLE C	D	$\overline{Q}$
L	L	X	X	L
L	H	H	H	L
L	H	H	L	H
L	H	L	X	$\overline{Q}_0$
H	X	X	X	Z

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

logic diagram (each quad latch, positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS880A, SN54AS880 . . . . . −55°C to 125°C
SN74ALS880A, SN74AS880 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

recommended operating conditions

			SN54ALS880A			SN74ALS880A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−1			−2.6	mA
I_{OL}	Low-level output current				12			24	mA
t_w	Pulse duration	$\overline{PRE}$ low	15			15			ns
		Enable C high	15			15			
t_{su}	Setup time, data before enable C↓		10			10			ns
t_h	Hold time, data after enable C↓		10			10			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS880A			SN74ALS880A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		14	21		14	21	mA
		Outputs low		19	29		19	29	
		Outputs disabled		20	31		20	31	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS880A			SN54ALS880A		SN74ALS880A		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	$\overline{Q}$		14	19	3	23	3	20	ns
t_{PHL}				9	12	3	15	3	14	
t_{PLH}	C	$\overline{Q}$		17	22	8	31	8	24	ns
t_{PHL}				14	18	8	22	8	21	
t_{PHL}	$\overline{PRE}$	$\overline{Q}$		12	16	6	24	6	21	ns
t_{PZH}	$\overline{OC}$	$\overline{Q}$		12	15	4	21	4	18	ns
t_{PZL}				13	17	4	21	4	18	
t_{PHZ}	$\overline{OC}$	$\overline{Q}$		6	9	2	12	2	10	ns
t_{PLZ}				8	11	3	21	3	17	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

recommended operating conditions

			SN54AS880			SN74AS880			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−12			−15	mA
I_{OL}	Low-level output current				32			48	mA
t_w	Pulse duration	$\overline{PRE}$ low	4.5			3.5			ns
		Enable C high	4			2.5			
t_{su}	Setup time, data before enable C↓		2			2			ns
t_h	Hold time, data after enable C↓		1			1			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS880			SN74AS880			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2					
	V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4	3.3		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.30	0.5				V
	V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		73	118		73	118	mA
		Outputs low		76	122		76	122	
		Outputs disabled		86	137		86	137	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS880		SN74AS880		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	$\overline{Q}$	4	11	4	9.5	ns
t_{PHL}			4	9	4	8.5	
t_{PLH}	C	$\overline{Q}$	6	14	6	11.5	ns
t_{PHL}			4	10	4	8	
t_{PHL}	$\overline{PRE}$	$\overline{Q}$	4	11.5	4	10	ns
t_{PZH}	$\overline{OC}$	$\overline{Q}$	2	8	2	7.5	ns
t_{PZL}			4	11	4	10	
t_{PHZ}	$\overline{OC}$	$\overline{Q}$	2	8	2	6.5	ns
t_{PLZ}			2	9	2	8	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

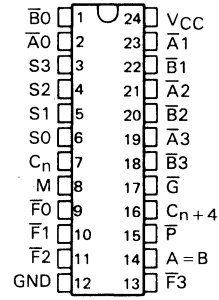
TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SN54AS881A, SN74AS881A
ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

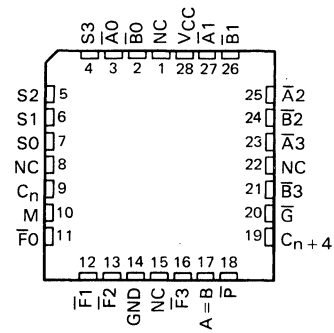
D2661, DECEMBER 1982 – REVISED MAY 1986

- Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Full Look-Ahead for High-Speed Operations on Long Words
- Arithmetic Operating Modes:
  - Addition
  - Subtraction
  - Shift Operand A One Position
  - Magnitude Comparison
  - Plus Twelve Other Arithmetic Operations
- Logic Function Modes
  - Exclusive-OR
  - Comparator
  - AND, NAND, OR, NOR
  - 'AS881A Provides Status Register Checks
  - Plus Ten Other Logic Operations
- Dependable Texas Instruments Quality and Reliability

SN54AS181A . . . J OR JT PACKAGE
SN54AS881A . . . JT PACKAGE
SN74AS181A . . . N OR NT PACKAGE
SN74AS881A . . . DW OR NT PACKAGE
(TOP VIEW)

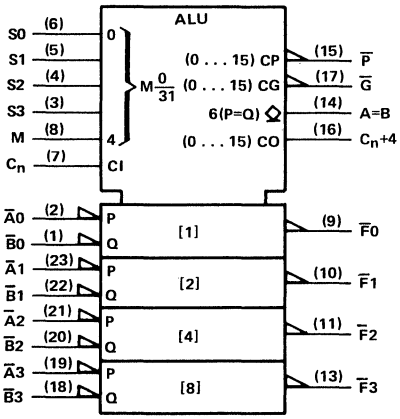


SN54AS181A, SN54AS881A . . . FK PACKAGE
SN74AS181A, SN74AS881A . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

logic symbol†



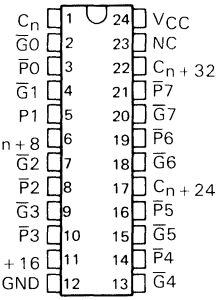
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers are for DW, JT, and NT packages.

For complete information on the SN54AS881A and the SN74AS881A, see page 2-187.

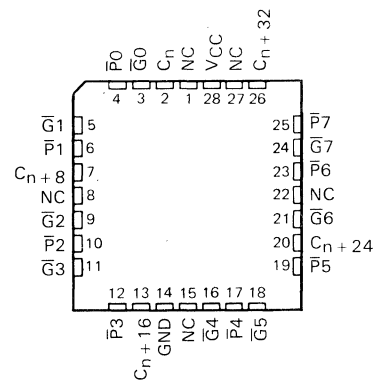
D2661, DECEMBER 1982 - REVISED NOVEMBER 1985

- **Directly Compatible with 'AS181B, 'AS1181, 'AS881B, and 'AS1881 ALUs**
- **Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Capable of Anticipating the Carry Across a Group of Eight 4-Bit Binary Adders**
- **Cascadable to Perform Look-Ahead Across n-Bit Adders**
- **Typical Carry Time, C_n to Any C_{n+i}, is Less Than 6 ns**
- **Dependable Texas Instruments Quality and Reliability**

SN54AS882A . . . JT PACKAGE
SN74AS882A . . . DW OR NT PACKAGE
(TOP VIEW)



SN54AS882A . . . FK PACKAGE
SN74AS882A . . . FN PACKAGE
(TOP VIEW)



NC No internal connection

description

The 'AS882A is a high-speed look-ahead carry generator capable of anticipating the carry across a group of eight 4-bit adders permitting the designer to implement look-ahead for a 32-bit ALU with a single package or, by cascading 'AS882A's, full look-ahead is possible across n-bit adders.

The SN54AS882A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS882A is characterized for operation from 0°C to 70°C.

'AS882A LOGIC EQUATIONS

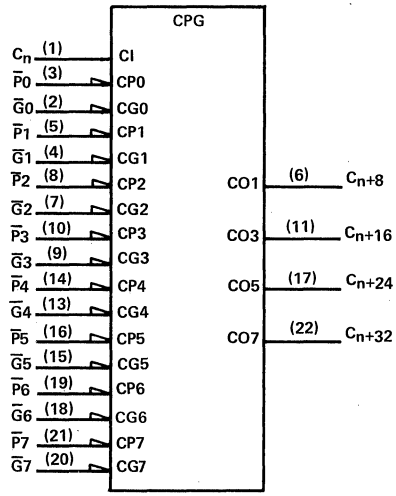
$$C_{n+8} = G1 + P1G0 + P1P0C_n$$

$$C_{n+16} = G3 + P3G2 + P3P2G1 + P3P2P1G0 + P3P2P1P0C_n$$

$$C_{n+24} = G5 + P5G4 + P5P4G3 + P5P4P3G2 + P5P4P3P2G1 + P5P4P3P2P1G0 + P5P4P3P2P1P0C_n$$

$$C_{n+32} = G7 + P7G6 + P7P6G5 + P7P6P5G4 + P7P6P5P4G3 + P7P6P5P4P3G2 + P7P6P5P4P3P2G1 + P7P6P5P4P3P2P1G0 + P7P6P5P4P3P2P1P0C_n$$

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

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FUNCTION TABLE
FOR C_{n+32} OUTPUT

INPUTS																OUTPUT
$\overline{G}7$	$\overline{G}6$	$\overline{G}5$	$\overline{G}4$	$\overline{G}3$	$\overline{G}2$	$\overline{G}1$	$\overline{G}0$	$\overline{P}7$	$\overline{P}6$	$\overline{P}5$	$\overline{P}4$	$\overline{P}3$	$\overline{P}2$	$\overline{P}1$	$\overline{P}0$	C_n	C_{n+32}
L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	L	X	X	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	L	L	X	X	X	X	X	X	X	H
X	X	X	L	X	X	X	X	L	L	L	X	X	X	X	X	X	H
X	X	X	X	L	X	X	X	L	L	L	L	X	X	X	X	X	H
X	X	X	X	X	L	X	X	L	L	L	L	L	X	X	X	X	H
X	X	X	X	X	X	L	X	L	L	L	L	L	L	X	X	X	H
X	X	X	X	X	X	X	L	L	L	L	L	L	L	L	X	X	H
X	X	X	X	X	X	X	X	L	L	L	L	L	L	L	L	H	H
All other combinations																	L

FUNCTION TABLE
FOR C_{n+24} OUTPUT

INPUTS												OUTPUT
$\overline{G}5$	$\overline{G}4$	$\overline{G}3$	$\overline{G}2$	$\overline{G}1$	$\overline{G}0$	$\overline{P}5$	$\overline{P}4$	$\overline{P}3$	$\overline{P}2$	$\overline{P}1$	$\overline{P}0$	C_n	C_{n+24}
L	X	X	X	X	X	X	X	X	X	X	X	X	H
X	L	X	X	X	X	L	X	X	X	X	X	X	H
X	X	L	X	X	X	L	L	X	X	X	X	X	H
X	X	X	L	X	X	L	L	L	X	X	X	X	H
X	X	X	X	L	X	L	L	L	L	X	X	X	H
X	X	X	X	X	L	L	L	L	L	L	X	X	H
X	X	X	X	X	X	L	L	L	L	L	L	H	H
All other combinations													L

FUNCTION TABLE
FOR C_{n+16} OUTPUT

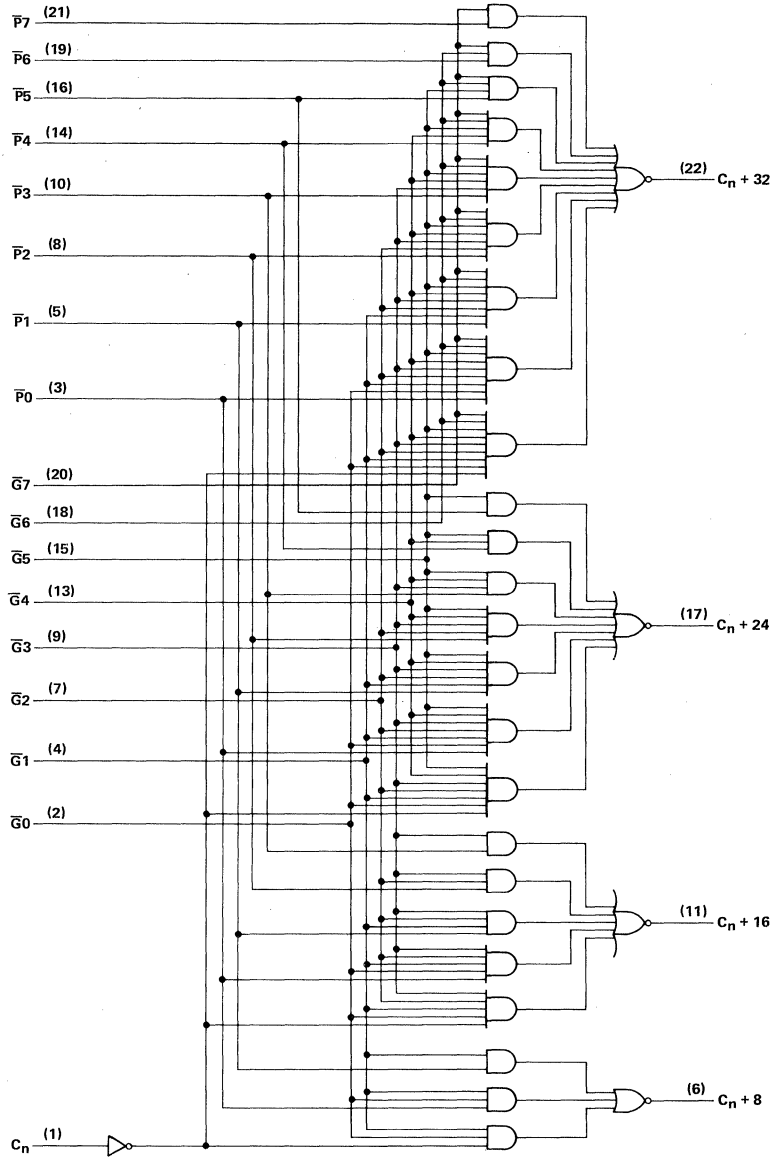
INPUTS									OUTPUT
$\overline{G}3$	$\overline{G}2$	$\overline{G}1$	$\overline{G}0$	$\overline{P}3$	$\overline{P}2$	$\overline{P}1$	$\overline{P}0$	C_n	C_{n+16}
L	X	X	X	X	X	X	X	X	H
X	L	X	X	L	X	X	X	X	H
X	X	L	X	L	L	X	X	X	H
X	X	X	L	L	L	L	X	X	H
X	X	X	X	L	L	L	L	H	H
All other combinations									L

FUNCTION TABLE
FOR C_{n+8} OUTPUT

INPUTS					OUTPUT
$\overline{G}1$	$\overline{G}0$	$\overline{P}1$	$\overline{P}0$	C_n	C_{n+8}
L	X	X	X	X	H
X	L	L	X	X	H
X	X	L	L	H	H
All other combinations					L

Any inputs not shown in a given table are irrelevant with respect to that output.

logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS882A . . . . . −55°C to 125°C
SN74AS822A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS882A			SN74AS882A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS882A			SN74AS882A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V, to 5.5 V,	I_{OH} = −2 mA	V_{CC} − 2			V_{CC} − 2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.3	0.5		0.3	0.5	V
I_I	C_n, $\overline{P}0$, $\overline{P}1$	V_{CC} = 5.5 V,	V_I = 7 V			0.4			0.4	mA
	$\overline{G}0$, $\overline{G}6$					0.8			0.8	
	$\overline{G}1$, $\overline{G}2$, $\overline{G}4$					1.2			1.2	
	$\overline{G}3$, $\overline{G}5$					1.5			1.5	
	$\overline{G}7$					0.9			0.9	
	$\overline{P}2$, $\overline{P}3$					0.3			0.3	
	$\overline{P}4$, $\overline{P}5$					0.2			0.2	
	$\overline{P}6$, $\overline{P}7$					0.1			0.1	
I_{IH}	C_n, $\overline{P}0$, $\overline{P}1$	V_{CC} = 5.5 V,	V_I = 2.7 V			80			80	μA
	$\overline{G}0$, $\overline{G}6$					160			160	
	$\overline{G}1$, $\overline{G}2$, $\overline{G}4$					240			240	
	$\overline{G}3$, $\overline{G}5$					300			300	
	$\overline{G}7$					180			180	
	$\overline{P}2$, $\overline{P}3$					60			60	
	$\overline{P}4$, $\overline{P}5$					40			40	
	$\overline{P}6$, $\overline{P}7$					20			20	
I_{IL}	C_n, $\overline{P}0$, $\overline{P}1$	V_{CC} = 5.5 V,	V_I = 0.4 V			−2			−2	mA
	$\overline{G}0$, $\overline{G}6$					−4			−4	
	$\overline{G}1$, $\overline{G}2$, $\overline{G}4$					−6			−6	
	$\overline{G}3$, $\overline{G}5$					−7.5			−7.5	
	$\overline{G}7$					−4.5			−4.5	
	$\overline{P}2$, $\overline{P}3$					−1.5			−1.5	
	$\overline{P}4$, $\overline{P}5$					−1			−1	
	$\overline{P}6$, $\overline{P}7$					−0.5			−0.5	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−130	−30		−130	mA
I_{CC}		V_{CC} = 5.5 V			44	70		44	70	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

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switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS822A		SN74AS882A		
			MIN	MAX	MIN	MAX	
t_{PLH}	C_n	Any output	2	10	2	9	ns
t_{PHL}			3	15	3	14	
t_{PLH}	$\overline{P}$ or $\overline{G}$	C_{n+8}	2	8	2	7	
t_{PHL}			2	8	2	7	
t_{PLH}	$\overline{P}$ or $\overline{G}$	C_{n+16}	2	8	2	7	
t_{PHL}			2	8	2	7	
t_{PLH}	$\overline{P}$ or $\overline{G}$	C_{n+24}	2	8	2	7	
t_{PHL}			2	11	2	10	
t_{PLH}	$\overline{P}$ or $\overline{G}$	C_{n+32}	1.5	9	2	8	
t_{PHL}			2	13	2	12	

NOTE 1: Load circuits and voltage waveforms are shown in Section 1.

TYPICAL APPLICATION DATA

The application given in Figure 1 illustrates how the 'AS882A can implement look-ahead carry for a 32-bit ALU (in this case, the popular 'AS881A) with a single package. Typical carry times shown are derived using the standard Advanced Schottky load circuit.

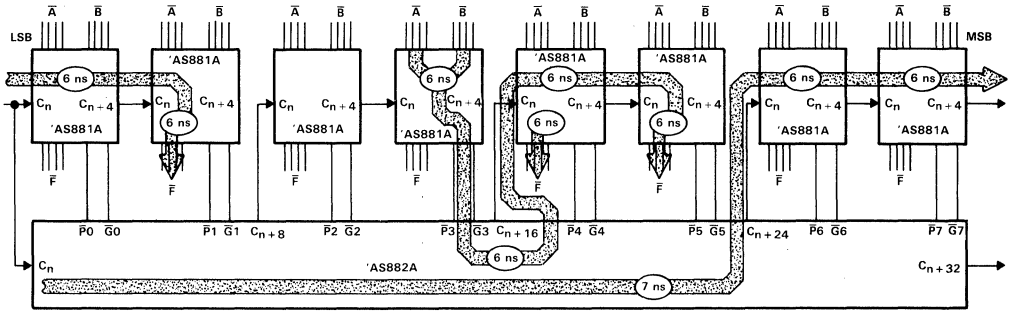

FIGURE 1

Likewise, Figure 2 illustrates the same 32-bit ALU using two 'AS882s. This shows the worst-case delay from LSB to MSB to be 19 ns as opposed to 25 ns in Figure 1.

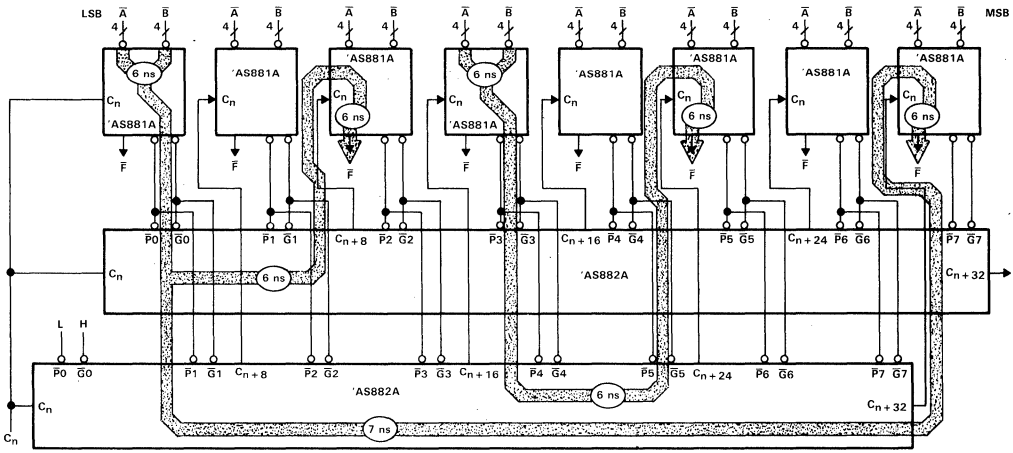

FIGURE 2

TEXAS INSTRUMENTS
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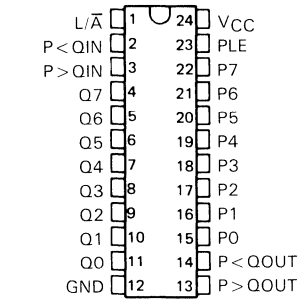
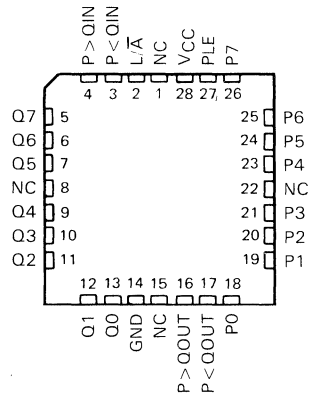
D2661, DECEMBER 1982 REVISED MARCH 1985

- **Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Latchable P Input Ports with Power-Up Clear**
- **Choice of Logical or Arithmetic (2's Complement) Comparison**
- **Data and PLE Inputs Utilize P-N-P Input Transistors to Reduce DC Loading Effects**
- **Approximately 35% Improvement in AC Performance Over Schottky TTL while Performing More Functions**
- **Cascadable to n-Bits while Maintaining High Performance**
- **10% Less Power than STTL for an 8-Bit Comparison**
- **Dependable Texas Instruments Quality and Reliability**

SN54AS885 . . . . JT PACKAGE
SN74AS885 . . . . DW OR NT PACKAGE
(TOP VIEW)



SN54AS885 . . . . FK PACKAGE
SN74AS885 . . . . FN PACKAGE
(TOP VIEW)



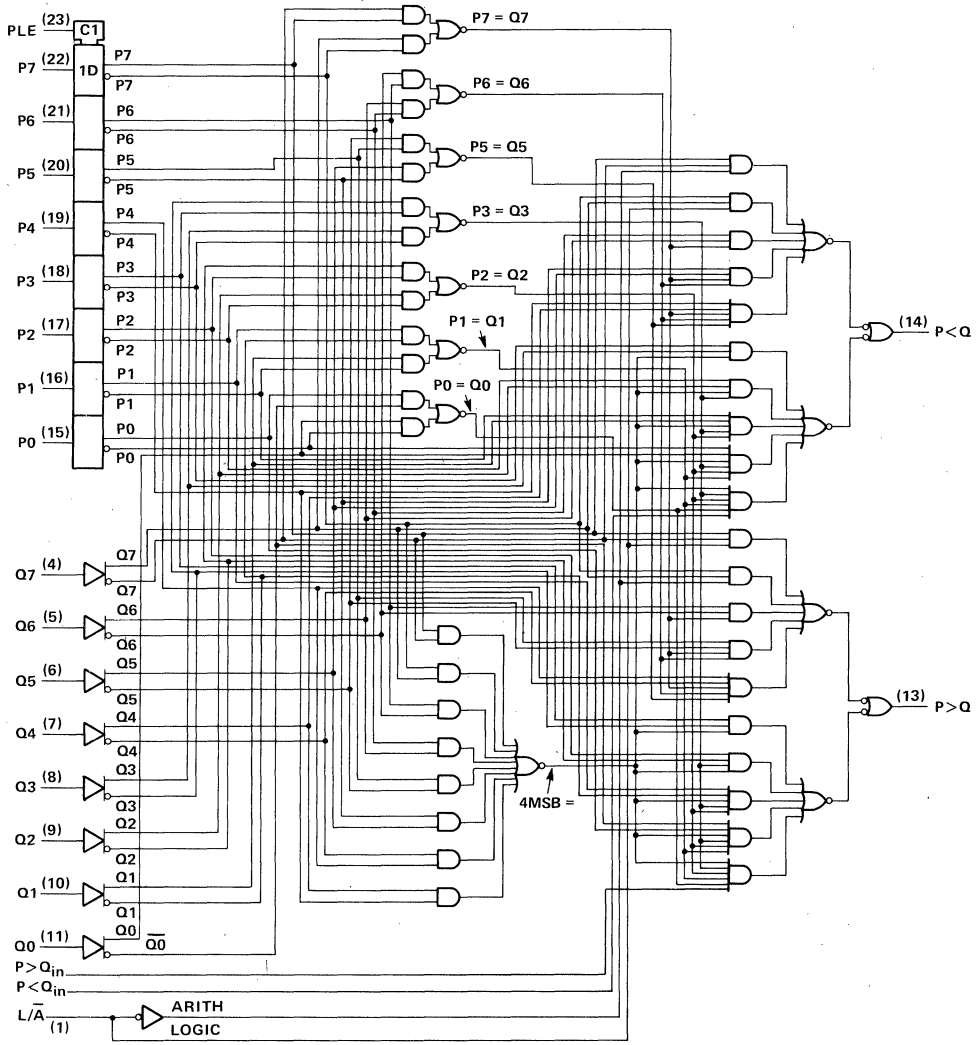
description

These advanced Schottky devices are capable of performing high-speed arithmetic or logic comparisons on two 8-bit binary or two's complement words. Two fully decoded decisions about words P and Q are externally available at two outputs. These devices are fully expandable to any number of bits without external gates. The P > Q and P < Q outputs of a stage handling less-significant bits may be connected to the P > Q and P < Q inputs of the next stage handling more-significant bits to obtain comparisons of words of longer lengths. The cascading paths are implemented with only a two-gate-level delay to reduce overall comparison times for long words. Two alternative methods of cascading are shown in the typical application data.

The latch is transparent when P Latch Enable (PLE) is high; the P input port is latched when PLE is low. This provides the designer with temporary storage for the P data word. The enable circuitry is implemented with minimal delay times to enhance performance when cascaded for longer words. The PLE and P and Q data inputs utilize p-n-p input transistors to reduce the low-level current input requirement to typically −0.25 mA, which minimizes dc loading effects.

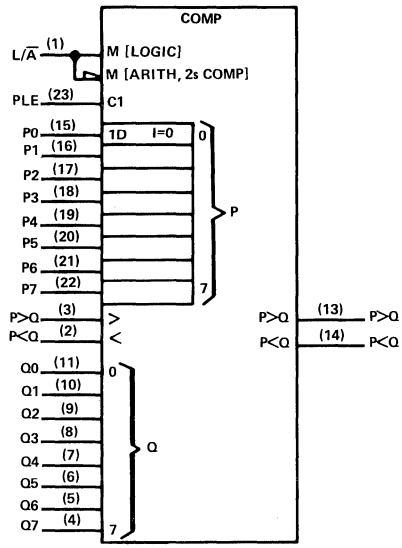
The SN54AS885 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS885 is characterized for operation from 0°C to 70°C.

logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

FUNCTION TABLE

COMPARISON	L/Ā	DATA INPUTS P0-P7, Q0-Q7	INPUT P>Q	INPUT P<Q	OUTPUTS P>Q	OUTPUTS P<Q
LOGICAL	H	P>Q	X	X	H	L
LOGICAL	H	P<Q	X	X	L	H
LOGICAL‡	H	P=Q	H OR L	H OR L	H OR L	H OR L
ARITHMETIC	L	P AG Q	X	X	H	L
ARITHMETIC	L	Q AG P	X	X	L	H
ARITHMETIC‡	L	P=Q	H OR L	H OR L	H OR L	H OR L

‡In these cases the P>Q output will follow the P>Q input, and the P<Q output will follow the P<Q input.
AG — arithmetically greater than

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS885 . . . . . −55°C to 125°C
SN74AS885 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

PARAMETER		SN54AS885			SN74AS885			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
t_{su}	Setup time to PLE↓	2			2			ns
t_h	Hold time after PLE↓	4			4			
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS885			SN74AS885			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 to 5.5 V,	I_{OH} = −2 mA	V_{CC} − 2			V_{CC} − 2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	μA
I_{IH}	L/$\overline{A}$	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	μA
	Others					20			20	
I_{IL}	L/$\overline{A}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−4			−4	mA
	P > Q_{in} P < Q_{in}					−2			−2	
	P, Q, PLE					−1			−1	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−20		−112	−20		−112	mA
I_{CC}		V_{CC} = 5.5 V	See Note 1		130	210		130	210	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit current, I_{OS}.
NOTE 1: I_{CC} is measured with all inputs high except L/$\overline{A}$, which is low.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			SN54AS885			SN74AS885			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	L A	P < Q_{in} P > Q_{in}		8.5	14		8.5	13	ns
t_{PHL}				7.5	14		7.5	13	
t_{PLH}	P < Q_{in}	P < Q, P > Q		5	10		5	8	ns
t_{PHL}	P > Q_{in}			5.5	10		5.5	8	
t_{PLH}	Any P or Q			13.5	21		13.5	17.5	ns
t_{PHL}	Data Input			10	17		10	15	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

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TYPICAL APPLICATION DATA

The 'AS885 can be cascaded to compare words longer than 8-bits. Figure 1 shows the comparison of two 32-bit words; however, the design is expandable to n-bits. Figure 1 shows the optimum cascading arrangement for comparing words of 32 bits or greater. Typical delay times shown are at V_{CC} = 5 V, T_A = 25°C, and use the standard Advanced Schottky load of R_L = 500 Ω, C_L = 50 pF.

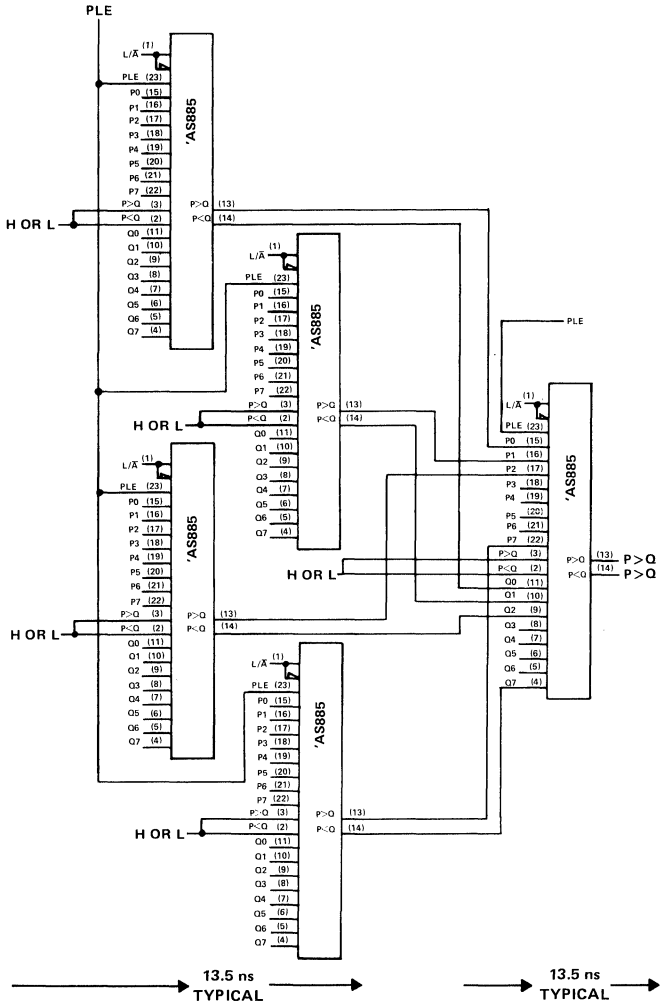


FIGURE 1. 32-BIT TO 72 (N)-BIT MAGNITUDE COMPARATOR

TYPICAL APPLICATION DATA

The method shown in Figure 2 is the fastest cascading arrangement for comparing 16-bit or 24-bit words. Typical delay times shown are at V_{CC} = 5 V, T_A = 25°C, and use the standard Advanced Schottky load of R_L = 500 Ω, C_L = 50 pF.

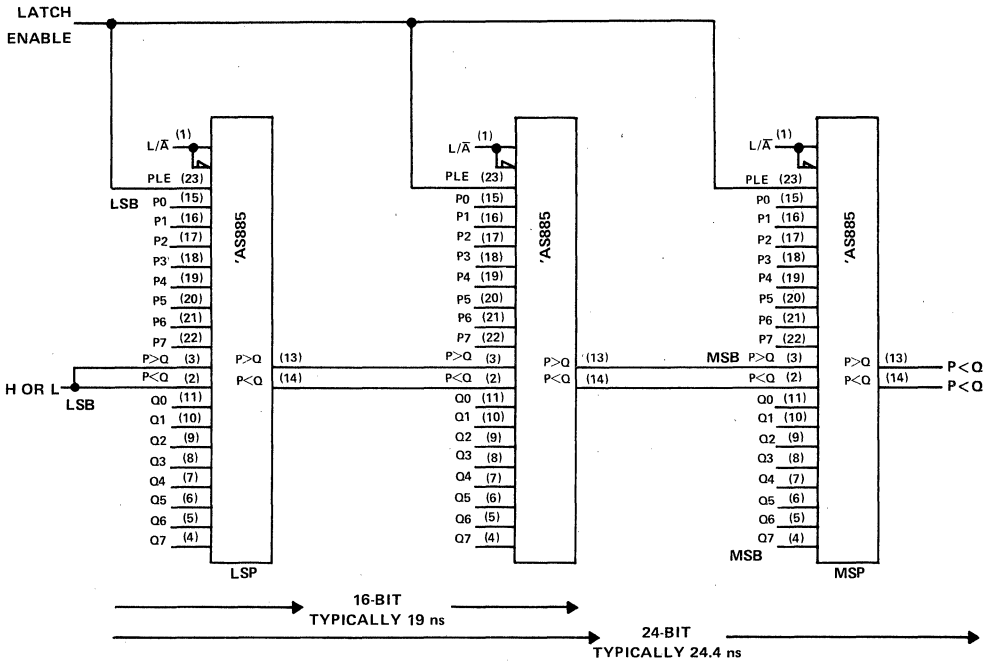


FIGURE 2

SN54ALS963, SN54ALS964, SN74ALS963, SN74ALS964
DUAL-RANK 8-BIT SHIFT REGISTERS WITH 3-STATE OUTPUTS

D2881, NOVEMBER 1985—REVISED MAY 1986

- **Serial-to-Parallel and Parallel-to-Serial Conversions**
- **Parallel I/O Registers**
- **Data Exchangeable Between I/O Register and Shift Register**
- **Choice of Synchronous and/or Asynchronous Clear**
- **Independent or Dual Register Clocking**
- **Functionally Similar to National Semiconductor DM74LS962**
- **Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

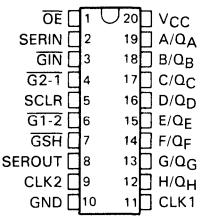
The 'ALS963 and 'ALS964 each contain an 8-bit shift register in parallel with an 8-bit I/O register. In addition to serial-to-parallel and parallel-to-serial conversions, these devices are capable of exchanging data between the shift and I/O registers. Control lines determine the mode of operation as shown in the function table.

The 'ALS963 features individual shift and I/O register clock inputs whereas the 'ALS964 features simultaneous register clocking through a single clock input. Clocking in both cases is achieved by positive transitions at the clock inputs.

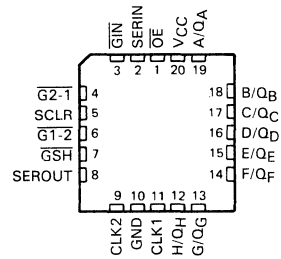
The clear function for the 'ALS963 is synchronous (active high). The 'ALS964 features active-high synchronous and asynchronous clearing.

The SN54ALS963 and SN54ALS964 are characterized for operation over the full military of −55°C to 125°C. The SN74ALS963 and SN74ALS964 are characterized for operation from 0°C to 70°C.

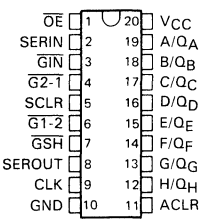
SN54ALS963 . . . JT PACKAGE
SN74ALS963 . . . DW OR NT PACKAGE
(TOP VIEW)



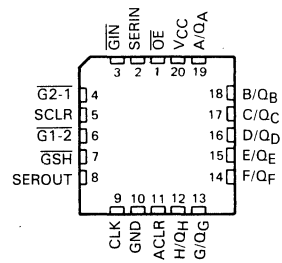
SN54ALS963 . . . FK PACKAGE
(TOP VIEW)



SN54ALS964 . . . JT PACKAGE
SN74ALS964 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54ALS964 . . . FK PACKAGE
(TOP VIEW)



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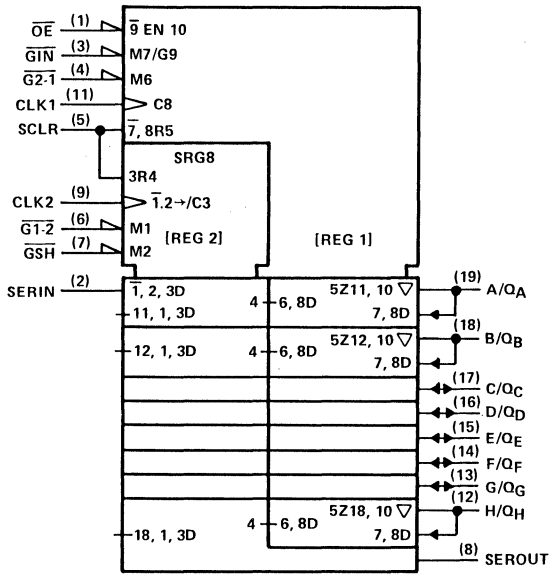
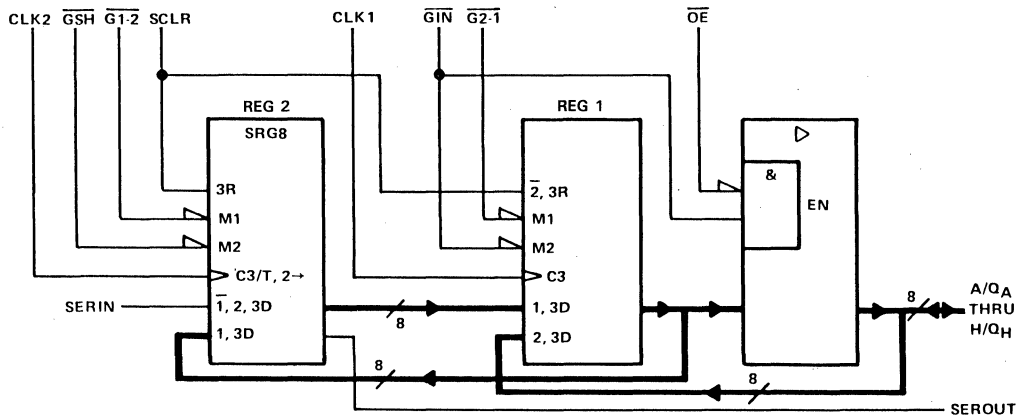
'ALS963 logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

'ALS963 register-level logic diagram



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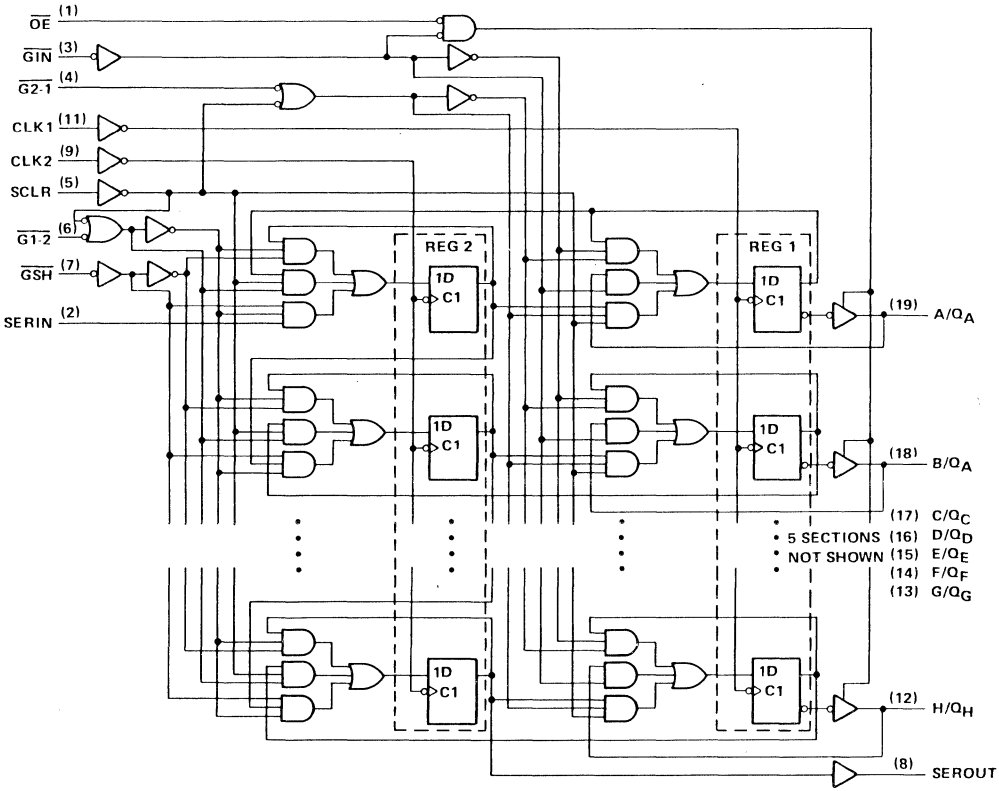
'ALS963 gate-level logic diagram (positive logic)



'ALS963
FUNCTION TABLE

INPUTS								A/QA THROUGH H/QH	OPERATION OR FUNCTION
$\overline{OE}$	$\overline{GIN}$	$\overline{GE\text{-}1}$	$\overline{G1\text{-}2}$	$\overline{GSH}$	CLK1	CLK2	SCLR		
H	H	H	H	H	X	X	L	HI-Z	All data stable
L	H	H	H	H	X	X	L	OUTPUT	All data stable
X	L	H	H	H	↑	X	L	INPUT	Enter data from I/O into Reg 1
H	H	L	H	H	↑	X	L	HI-Z	Copy data from Reg 2 to Reg 1
L	H	L	H	H	↑	X	L	OUTPUT	Copy data from Reg 2 to Reg 1
X	L	L	H	H	↑	↑	L	INPUT	Reg 1 ORs data from Reg 2 and I/O
H	H	H	L	X	X	↑	L	HI-Z	Copy data from Reg 1 to Reg 2
L	H	H	L	X	X	↑	L	OUTPUT	Copy data from Reg 1 to Reg 2
X	L	H	L	X	↑	↑	L	INPUT	Copy data from Reg 1 to Reg 2, enter new data from I/O into Reg 1
H	H	L	L	X	↑	↑	L	HI-Z	Exchange data between registers
L	H	L	L	X	↑	↑	L	OUTPUT	Exchange data between registers
X	L	L	L	X	↑	↑	L	INPUT	Copy data from Reg 1 to Reg 2, Reg 1 ORs data from Reg 2 and I/O
H	H	H	H	L	X	↑	L	HI-Z	Shift data in Reg 2
L	H	H	H	L	X	↑	L	OUTPUT	Shift data in Reg 2
X	L	H	H	L	↑	↑	L	INPUT	Shift data in Reg 2, enter new data from I/O into Reg 1
H	H	L	H	L	↑	↑	L	HI-Z	Copy data from Reg 2 to Reg 1, shift data in Reg 2
L	H	L	H	L	↑	↑	L	OUTPUT	Copy data from Reg 2 to Reg 1, shift data in Reg 2
X	L	L	H	L	↑	↑	L	INPUT	Reg 1 ORs data from Reg 2 and I/O, shift data in Reg 2
X	H	X	X	X	↑	X	H		Synchronously clear Reg 1
X	X	X	X	X	X	↑	H		Synchronously clear Reg 2
X	H	X	X	X	↑	↑	H		Synchronously clear both registers
X	L	X	X	X	↑	↑	H	INPUT	Enter data from I/O into Reg 1 and synchronously clear Reg 2
X	L	X	X	X	↑	X	H	INPUT	Enter data from I/O into Reg 1

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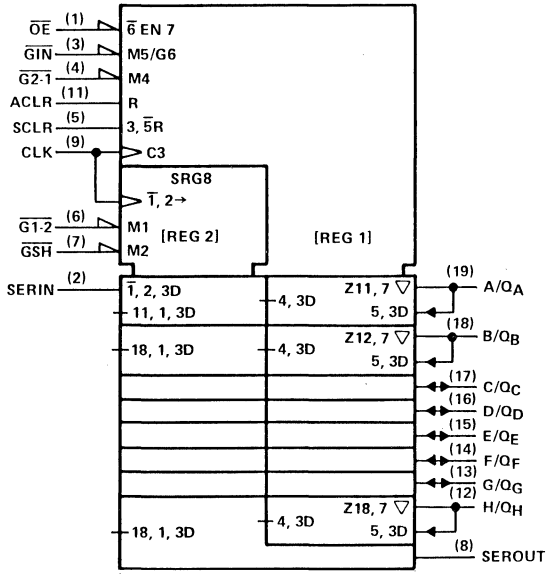
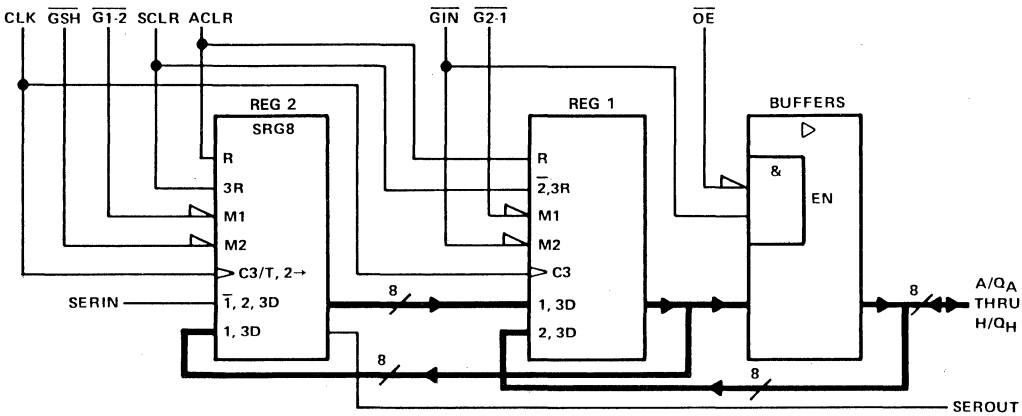
'ALS964 logic symbol†

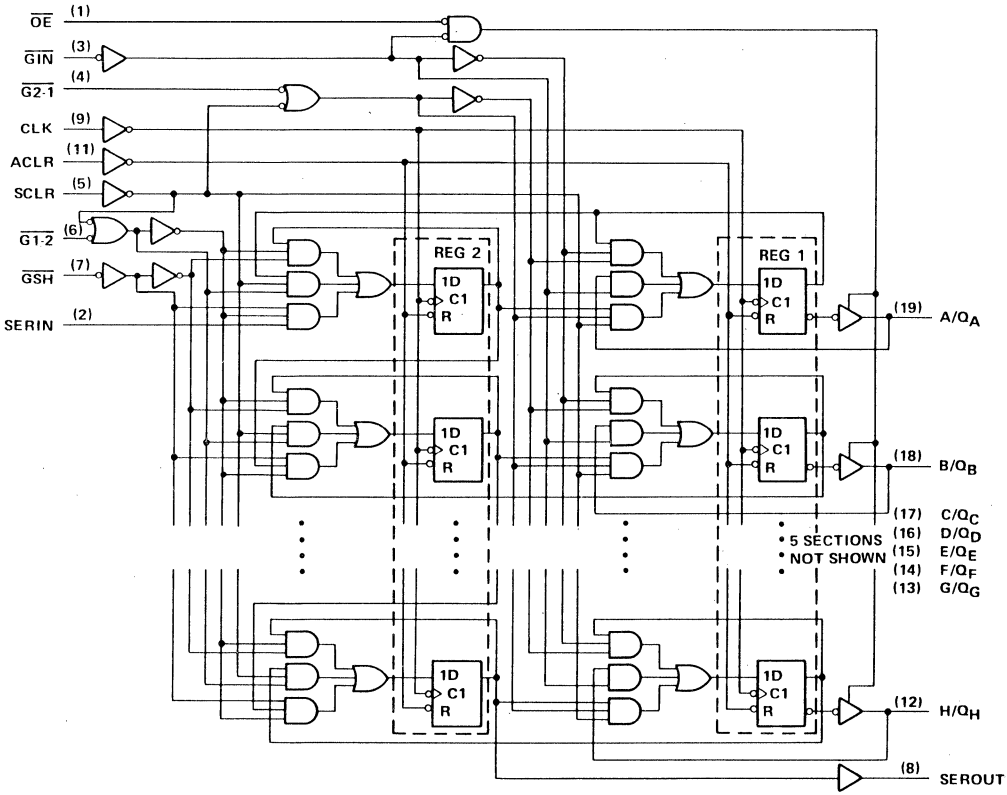


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

'ALS964 register-level logic diagram



'ALS964 gate-level logic diagram (positive logic)



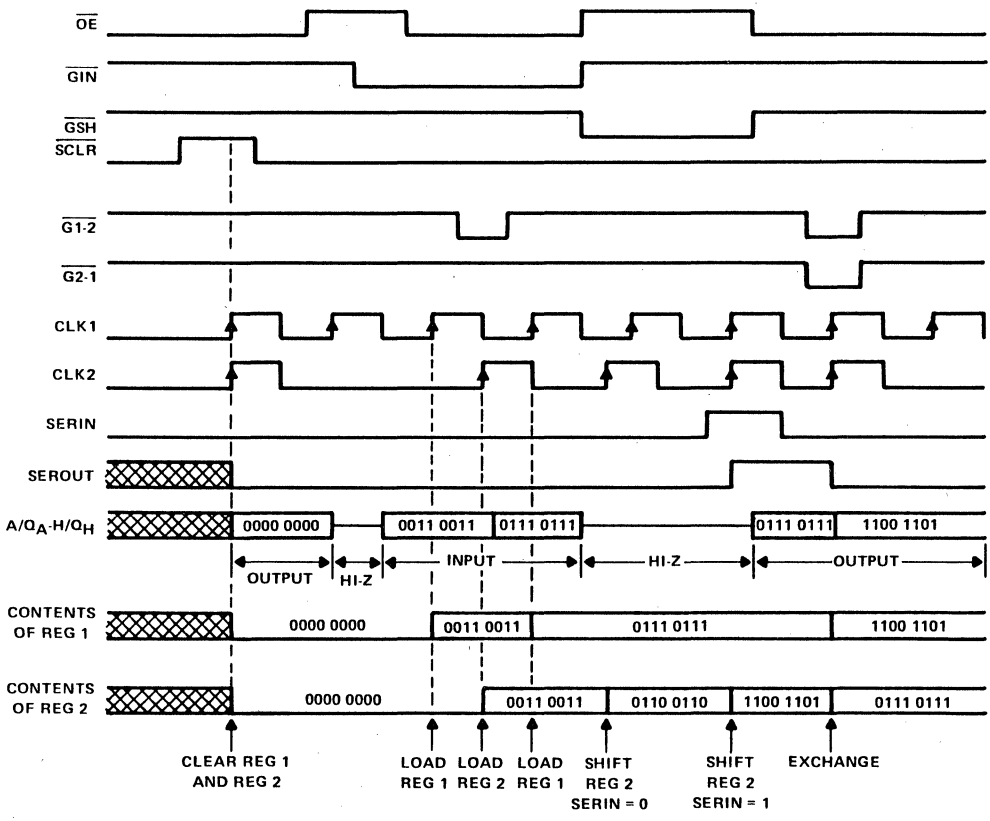
'ALS964
FUNCTION TABLE

INPUTS								A/QA THROUGH H/QH	OPERATION OR FUNCTION
$\overline{OE}$	$\overline{GIN}$	$\overline{G2\text{-}1}$	$\overline{G1\text{-}2}$	$\overline{GSH}$	CLK	ACLR	SCLR		
H	H	H	H	H	X	L	L	HI-Z	All data stable
L	H	H	H	H	X	L	L	OUTPUT	All data stable
X	L	H	H	H	↑	L	L	INPUT	Enter data from I/O into Reg 1
H	H	L	H	H	↑	L	L	HI-Z	Copy data from Reg 2 to Reg 1
L	H	L	H	H	↑	L	L	OUTPUT	Copy data from Reg 2 to Reg 1
X	L	L	H	H	↑	L	L	INPUT	Reg 1 ORs data from Reg 2 and I/O
H	H	H	L	X	↑	L	L	HI-Z	Copy data from Reg 1 to Reg 2
L	H	H	L	X	↑	L	L	OUTPUT	Copy data from Reg 1 to Reg 2
X	L	H	L	X	↑	L	L	INPUT	Copy data from Reg 1 to Reg 2, enter new data from I/O into Reg 1
H	H	L	L	X	↑	L	L	HI-Z	Exchange data between registers
L	H	L	L	X	↑	L	L	OUTPUT	Exchange data between registers
X	L	L	L	X	↑	L	L	INPUT	Copy data from Reg 1 to Reg 2, Reg 1 ORs data from Reg 2 and I/O
H	H	H	H	L	↑	L	L	HI-Z	Shift data in Reg 2
L	H	H	H	L	↑	L	L	OUTPUT	Shift data in Reg 2
X	L	H	H	L	↑	L	L	INPUT	Shift data in Reg 2, enter new data from I/O into Reg 1
H	H	L	H	L	↑	L	L	HI-Z	Copy data from Reg 2 to Reg 1, shift data in Reg 2
L	H	L	H	L	↑	L	L	OUTPUT	Copy data from Reg 2 to Reg 1, shift data in Reg 2
X	L	L	H	L	↑	L	L	INPUT	Reg 1 ORs data from Reg 2 and I/O, shift data in Reg 2
X	H	X	X	X	↑	L	H		Synchronously clear Reg 1 and Reg 2
X	X	X	X	X	X	H	X		Asynchronously clear Reg 1 and Reg 2
X	L	X	X	X	↑	L	H	INPUT	Enter data from I/O into Reg 1 and synchronously clear Reg 2

'ALS963 typical sequence

Illustrated below is the following sequence:

1. Clear both registers to zero.
2. Input 0011 0011 in Reg 1.
3. Transfer 0011 0011 from Reg 1 to Reg 2.
4. Input 0111 0111 into Reg 1.
5. Shift contents of Reg 2, SERIN = 0
6. Shift contents of Reg 2, SERIN = 1
7. Exchange contents of Reg 1 with Reg 2.



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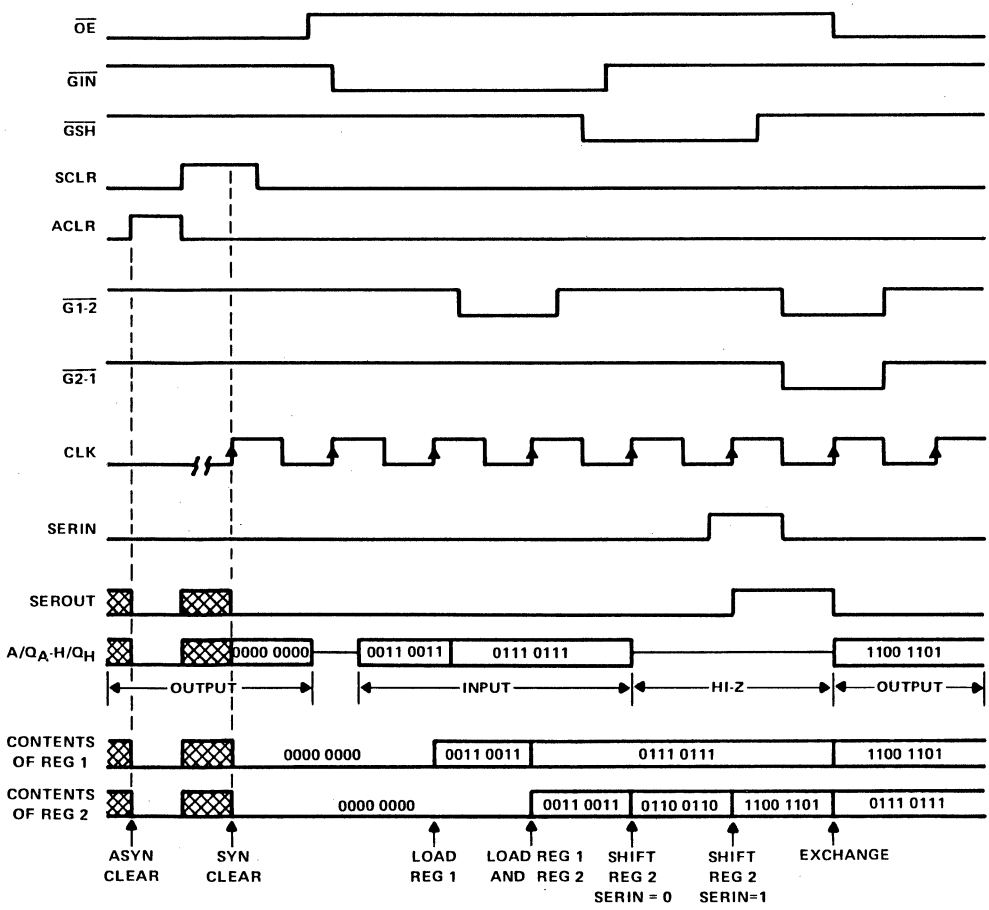
'ALS964 typical sequence

Illustrated below is the following sequence:

1. Asynchronously clear Reg 1 and Reg 2 to zero, operate, then synchronously clear.
2. Input 0011 0011 into Reg 1.
3. Transfer 0011 0011 from Reg 1 to Reg 2 and input 0111 0111 into Reg 1.
4. Shift contents of Reg 2, SERIN = 0
5. Shift contents of Reg 2, SERIN = 1
6. Exchange contents of Reg 1 with Reg 2.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS963, SN54ALS964 . . . . . −55°C to 125°C
SN74ALS963, SN74ALS964 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

'ALS963 recommended operating conditions

			SN54ALS963			SN74ALS963			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−1			−2.6	mA
I_{OL}	Low-level output current	SEROUT			8			16	mA
		Q_A thru Q_H			12			24	
f_{clock}	Clock frequency (at 50% duty cycle)		0		25	0		25	MHz
t_w	Pulse duration	CLK1 high or low	20			20			ns
		CLK2 high or low	20			20			
t_{su}	Setup time	Data before CLK1↑							ns
		$\overline{GIN}$ before CLK1↑							
		$\overline{G1\text{-}2}$ before CLK2↑							
		$\overline{G2\text{-}1}$ before CLK1↑							
		$\overline{GSH}$ before CLK2↑							
		SCLR before CLK1↑ or CLK2↑							
t_h	Hold time after CLK1↑ or CLK2↑								ns
T_A	Operating free-air temperature		−55		125	0		70	°C

'ALS964 recommended operating conditions

			SN54ALS964			SN74ALS964			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−1			−2.6	mA
I_{OL}	Low-level output current	SEROUT			8			16	mA
		Q_A thru Q_H			12			24	
f_{clock}	Clock frequency (at 50% duty cycle)		0		25	0		25	MHz
t_w	Pulse duration	CLK high or low	20			20			ns
		ACLR low							
t_{su}	Setup time	Data before CLK↑							ns
		$\overline{GIN}$ before CLK↑							
		$\overline{G1\text{-}2}$ before CLK↑							
		$\overline{G2\text{-}1}$ before CLK↑							
		$\overline{GSH}$ before CLK↑							
		SCLR before CLK↑							
t_h	Hold time after CLK↑								ns
T_A	Operating free-air temperature		−55		125	0		70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS963 SN54ALS964			SN74ALS963 SN74ALS964			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	SEROUT	V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 16 mA					0.35	0.5	
	Q_A thru Q_H	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	A thru H	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	mA
	Any other	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	
I_{IH}‡		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}‡		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS963	V_{CC} = 5.5 V	Outputs high							mA
			Outputs low							
			Outputs disabled							
	'ALS964	V_{CC} = 5.5 V	Outputs high							mA
			Outputs low							
			Outputs disabled							

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡For I/O ports (Q_A throuh Q_H), the parameters I_{IH} and I_{IL} include the off-state output current.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS963 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS963		SN74ALS963		
			MIN	TYP† MAX	MIN	TYP† MAX	
f_{max}	CLK1 or CLK2	Any Q	25	30	25	30	MHz
t_{PLH}	CLK1	Any Q		10		10	ns
t_{PHL}				14		14	
t_{PLH}	CLK2	SEROUT		10		10	ns
t_{PHL}				14		14	
t_{PHZ}	$\overline{OE}$	Any Q		15		15	ns
t_{PLZ}				18		18	
t_{PZH}	$\overline{OE}$	Any Q		12		12	ns
t_{PZL}				12		12	

'ALS964 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS964		SN74ALS964		
			MIN	TYP† MAX	MIN	TYP† MAX	
f_{max}	CLK	Any Q	25	30	25	30	MHz
t_{PLH}	CLK	Any Q		10		10	ns
t_{PHL}				14		14	
t_{PLH}	CLK	SEROUT		10		10	ns
t_{PHL}				14		14	
t_{PHZ}	ACLR	Any Q or SEROUT		14		14	ns
t_{PHZ}	$\overline{OE}$	Any Q		15		15	ns
t_{PLZ}				18		18	
t_{PZH}	$\overline{OE}$	Any Q		12		12	ns
t_{PZL}				12		12	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2835, APRIL 1984—REVISED MAY 1986

- **3-State I/O-Type Read-Back Inputs**
- **Bus-Structured Pinout**
- **Choice of True or Inverting Logic**
  'ALS990 . . . True Outputs
  'ALS991 . . . Inverting Outputs
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

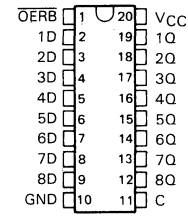
These 8-bit latches are designed specifically for storing the contents of the input data bus plus providing the capability of reading-back the stored data onto the input data bus.

The eight latches of the 'ALS990 and 'ALS991 are transparent D-type. While the enable (C) is high, the Q outputs of the 'ALS990 will follow the data (D) inputs. For the 'ALS991, the Q outputs will provide the complement of what is applied to its data (D) inputs.

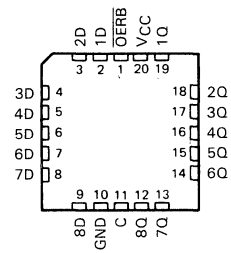
Read-back is provided through the read-back control input ($\overline{OERB}$). When the control is taken low, the data present at the output of the data latches will be allowed to pass back onto the input data bus. When it is taken high, the output of the data latches will be isolated from the data (D) inputs. The read-back control does not affect the internal operation of the latches; however, precautions should be taken not to create a bus-conflict situation.

The SN74ALS990 and SN74ALS991 are characterized for operation from 0°C to 70°C.

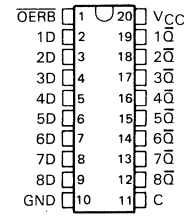
SN74ALS990 . . . DW OR N PACKAGE
(TOP VIEW)



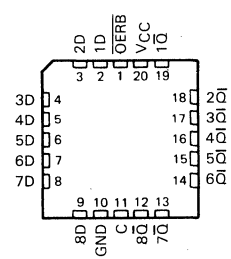
SN74ALS990 . . . FN PACKAGE
(TOP VIEW)



SN74ALS991 . . . DW OR N PACKAGE
(TOP VIEW)

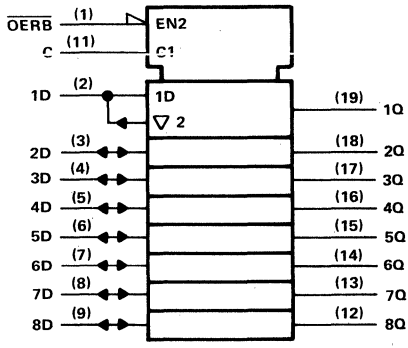


SN74ALS991 . . . FN PACKAGE
(TOP VIEW)

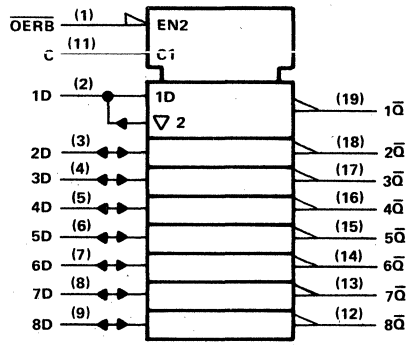


logic symbols†

'ALS990



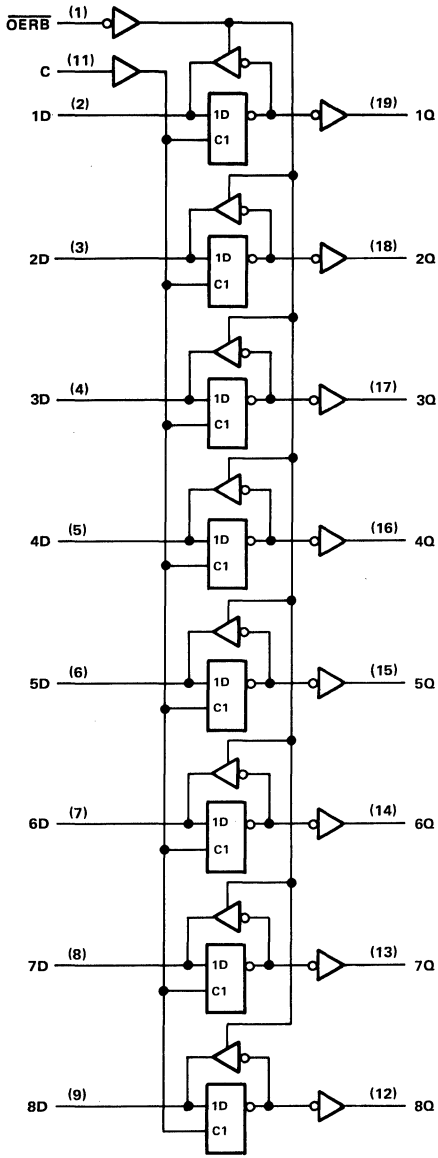
'ALS991



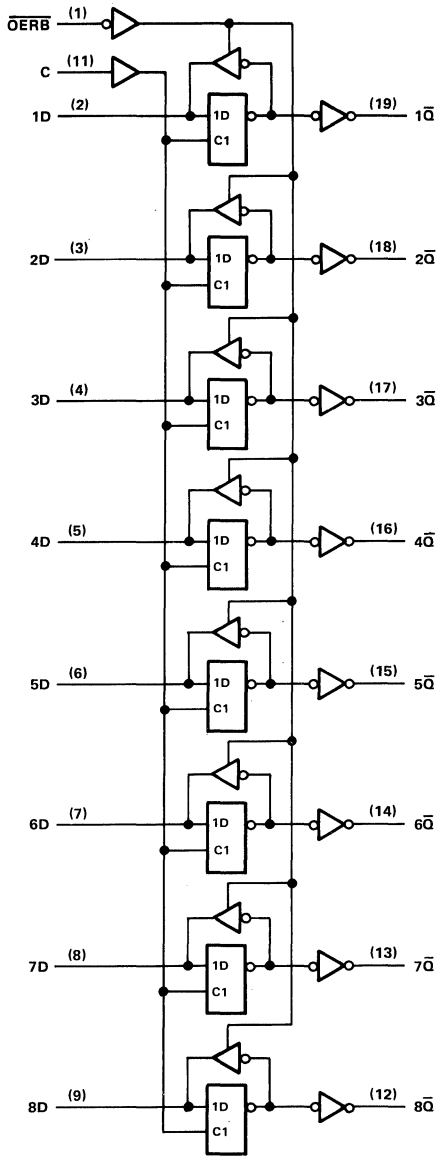
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)

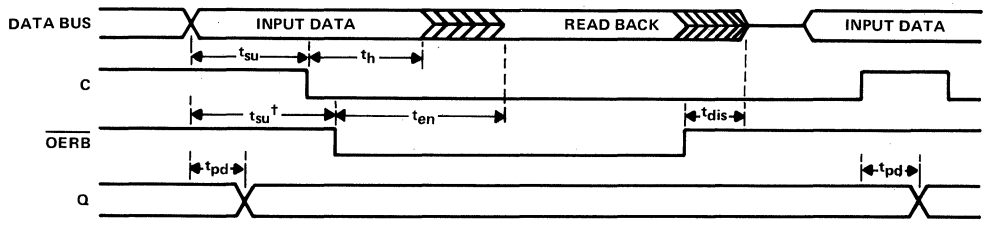
'ALS990



'ALS991



timing diagram



† This setup time ensures the readback circuit will not create a conflict on the input data bus.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, ($\overline{OERB}$ and C inputs) . . . . . 7 V
Voltage applied to D inputs . . . . . 5.5 V
Operating free-air temperature range SN74ALS990, SN74ALS991 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

				MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage			4.5	5	5.5	V
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
I_{OH}	High-level output current		Q			−2.6	mA
			D			−0.4	
I_{OL}	Low-level output current		Q			24	mA
			D			8	
t_w	Pulse duration, enable C high			10			ns
t_{su}	Setup time	Data before C↓		10			ns
		Data before $\overline{OERB}$↓		10			
t_h	Hold time	Data after C↓		5			ns
T_A	Operating free-air temperature			0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	All outputs	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V
	Q or $\overline{Q}$	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA	2.4	3.2		
V_{OL}	D	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.35	0.5	
	Q or $\overline{Q}$	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 24 mA		0.35	0.5	
I_I	$\overline{OERB}$, C	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
	D inputs	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1	
I_{IH}	$\overline{OERB}$, C	V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
	D inputs‡					20	
I_{IL}	$\overline{OERB}$, C	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1	mA
	D inputs‡					−0.1	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}	'ALS990	V_{CC} = 5.5 V, $\overline{OERB}$ high	Q outputs high		27	50	mA
			Q outputs low		40	70	
	'ALS991		$\overline{Q}$ outputs high		25	45	
			$\overline{Q}$ outputs low		45	75	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§The output conditions have been chosen to produce a current that closely approximates one half the true short-circuit output current, I_{OS}.

'ALS990 switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C, See Figures 1 and 2			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, T_A = 0°C to 70°C, See Figures 1 and 2		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	D	Q		8	14	4	17	ns
t_{PHL}				11	22	5	24	
t_{PLH}	C	Q		13	22	6	26	ns
t_{PHL}				16	23	8	26	
t_{en}	$\overline{OERB}$	D		12	18	4	21	ns
t_{dis}				10	18	4	19	

t_{en} = t_{PZL} or t_{PZH}
t_{dis} = t_{PLZ} or t_{PHZ}

'ALS991 switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C, See Figures 1 and 2			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, T_A = 0°C to 70°C, See Figures 1 and 2		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	D	$\overline{Q}$		12	15	4	20	ns
t_{PHL}				9	12	4	15	
t_{PLH}	C	$\overline{Q}$		17	21	9	28	ns
t_{PHL}				14	18	7	23	
t_{en}	$\overline{OERB}$	D		12	17	4	22	ns
t_{dis}				8	12	4	17	

t_{en} = t_{PZL} or t_{PZH}
t_{dis} = t_{PLZ} or t_{PHZ}

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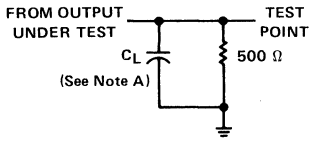
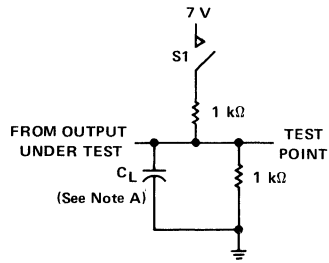
PARAMETER MEASUREMENT INFORMATION

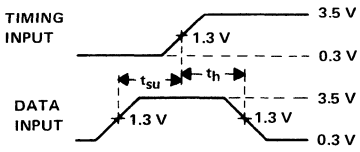


LOAD CIRCUIT FOR
Q OR $\overline{Q}$ OUTPUTS

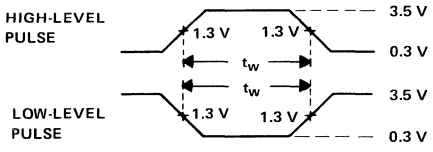


LOAD CIRCUIT FOR D OUTPUTS

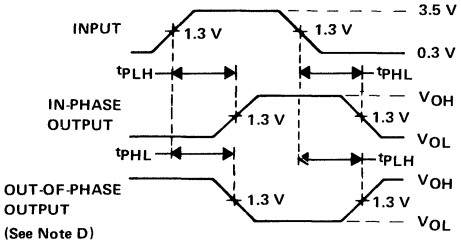
NOTE A: C_L includes probe and jig capacitance.



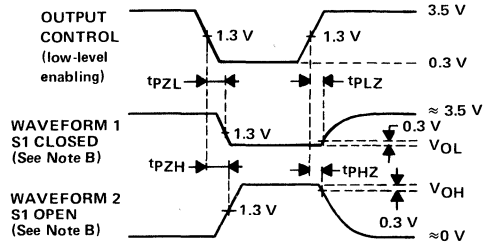
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE WIDTHS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is open.

FIGURE 1

D2836, APRIL 1984 REVISED JANUARY 1986

- **3-State I/O-Type Read-Back Inputs**
- **Bus-Structured Pinout**
- **Choice of True or Inverting Logic**
  'ALS992 . . . True Outputs
  'ALS993 . . . Inverting Outputs
- **Designed with 9 Bits for Parity Applications**
- **Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

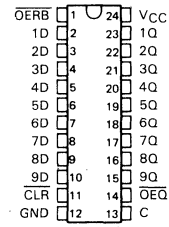
These 9-bit latches are designed specifically for storing the contents of the input data bus plus providing the capability of reading-back the stored data onto the input data bus. In addition, they provide a 3-state buffer-type output and are easily implemented in parity applications.

The nine latches of the 'ALS992 and 'ALS993 are transparent D-type. While the enable (C) is high, the Q outputs of the 'ALS992 will follow the data (D) inputs. For the 'ALS993, the $\overline{Q}$ outputs will provide the complement of what is applied to its data (D) inputs. On both devices, the Q or $\overline{Q}$ outputs will be in the 3-state condition when output enable $\overline{OEQ}$ is high.

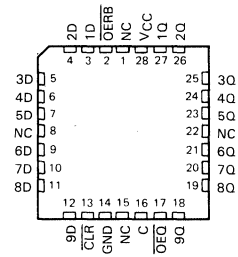
Read-back is provided through the read-back control input ($\overline{OERB}$). When the control is taken low, the data present at the output of the data latches will be allowed to pass back onto the input data bus. When it is taken high, the output of the data latches will be isolated from the data (D) inputs. The read-back control does not affect the internal operation of the latches; however, precautions should be taken not to create a bus-conflict situation.

The SN74ALS992 and SN74ALS993 are characterized for operation from 0°C to 70°C.

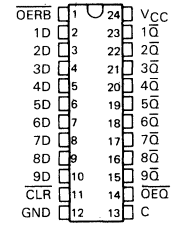
SN74ALS992 . . . DW OR NT PACKAGE
(TOP VIEW)



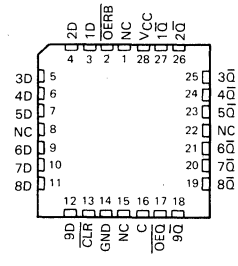
SN74ALS992 . . . FN PACKAGE
(TOP VIEW)



SN74ALS993 . . . DW OR NT PACKAGE
(TOP VIEW)



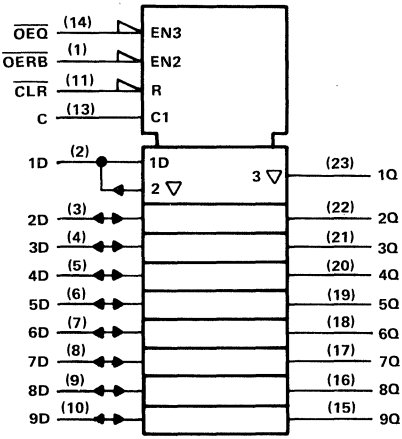
SN74ALS993 . . . FN PACKAGE
(TOP VIEW)



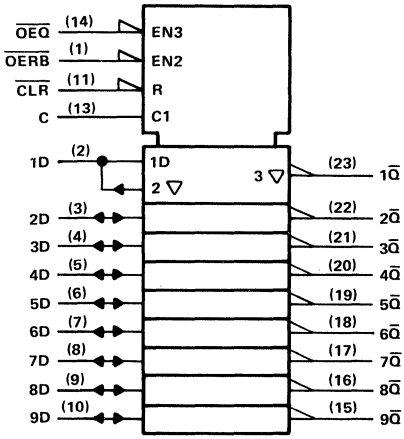
NC—No internal connection

logic symbols†

'ALS992



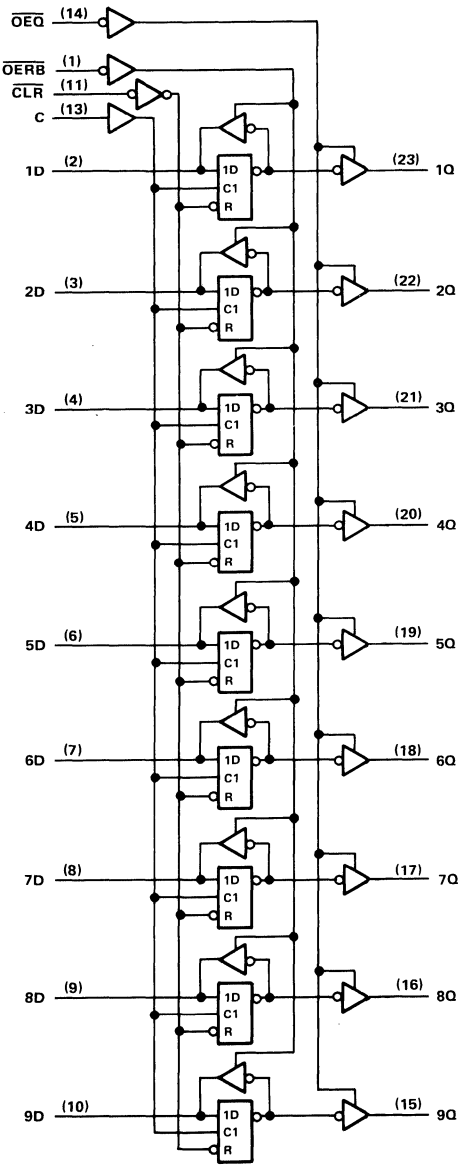
'ALS993



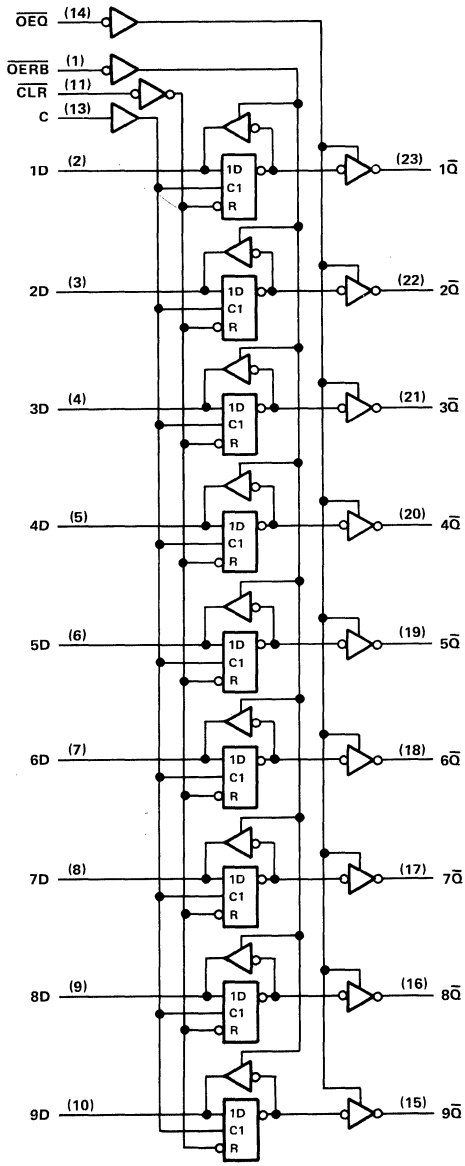
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers are for DW and NT packages.

logic diagrams (positive logic)

'ALS992

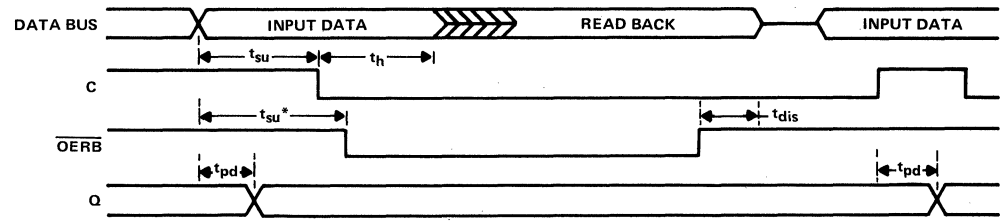


'ALS993



Pin numbers are for DW and NT packages.

timing diagram



$\overline{CLR}$ = H, $\overline{OEQ}$ = L

*This setup time ensures the readback circuit will not create a conflict on the input data bus.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, ($\overline{OERB}$, $\overline{OE}$, $\overline{CLR}$, and C inputs) . . . . . 7 V
Voltage applied to D inputs and to disabled 3-state outputs . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	Q or $\overline{Q}$			−2.6	mA
		D			−0.4	
I_{OL}	Low-level output current	Q or $\overline{Q}$			24	mA
		D			8	
t_w	Pulse duration	Enable C high	10			ns
		$\overline{CLR}$ low	10			
t_{su}	Setup time	Data before C↓	10			ns
		Data before $\overline{OERB}$↓	10			
t_h	Hold time	Data after C↓	5			ns
T_A	Operating free-air temperature		0		70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	All outputs	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V
	Q or $\overline{Q}$	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA	2.4	3.2		
V_{OL}	D	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.35	0.5	
	Q or $\overline{Q}$	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 24 mA		0.35	0.5	
I_{OZH}	Q or $\overline{Q}$	V_{CC} = 5.5 V,	V_O = 2.7 V			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20	
I_I	D inputs	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1	mA
	All other	V_{CC} = 5.5 V,	V_I = 7 V			0.1	
I_{IH}	D inputs‡	V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
	All other					20	
I_{IL}	D inputs‡	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1	mA
	All other					−0.1	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}	'ALS992	V_{CC} = 5.5 V, $\overline{OERB}$ high	Q outputs high		30	50	mA
			Q outputs low		50	80	
			Q outputs disabled		35	55	
	'ALS993	V_{CC} = 5.5 V, $\overline{OERB}$ high	$\overline{Q}$ outputs high		30	50	mA
			$\overline{Q}$ outputs low		52	82	
			$\overline{Q}$outputs disabled		40	60	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ The output conditions have been chosen to produce a current that closely approximates one half the true short-circuit output current, I_{OS}.

'ALS992 switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, T_A = 0°C to 70°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	D	Q		7	10	3	14	ns
t_{PHL}				9	13	4	16	
t_{PLH}	C	Q		12	15	6	20	ns
t_{PHL}				15	19	8	25	
t_{PHL}	$\overline{CLR}$	Q		12	16	6	20	ns
t_{PHL}		D		15	22	8	26	
t_{en}	$\overline{OERB}$	D		11	17	4	21	ns
t_{dis}				6	11	2	14	
t_{en}	$\overline{OEQ}$	Q		11	16	4	18	ns
t_{dis}				6	10	1	14	

'ALS993 switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, T_A = 0°C to 70°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	D	$\overline{Q}$		11	14	6	20	ns
t_{PHL}				8	11	4	15	
t_{PLH}	C	$\overline{Q}$		16	20	9	28	ns
t_{PHL}				13	16	7	22	
t_{PLH}	$\overline{CLR}$	$\overline{Q}$		10	13	5	17	ns
t_{PLH}		D		15	22	8	26	
t_{en}	$\overline{OERB}$	D		11	17	4	21	ns
t_{dis}				6	11	2	14	
t_{en}	$\overline{OEQ}$	$\overline{Q}$		11	16	4	20	ns
t_{dis}				6	10	1	12	

$t_{en} = t_{PZH}$ or t_{PZL}
$t_{dis} = t_{PHZ}$ or t_{PLZ}

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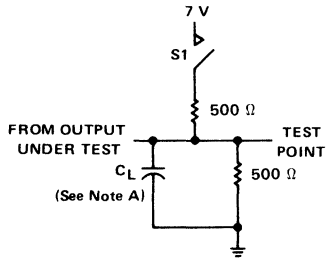
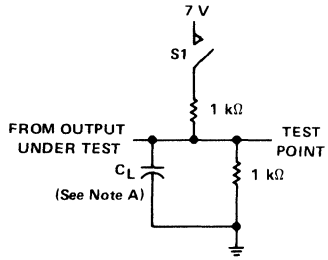
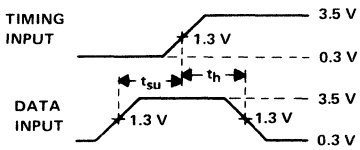
PARAMETER MEASUREMENT INFORMATION



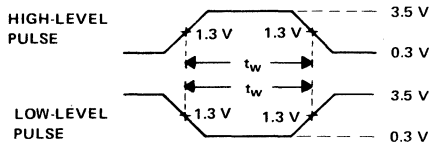
LOAD CIRCUIT FOR
Q OR $\overline{Q}$ OUTPUTS



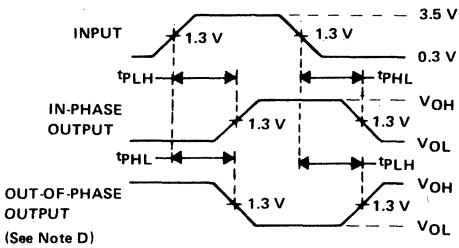
LOAD CIRCUIT FOR D OUTPUTS



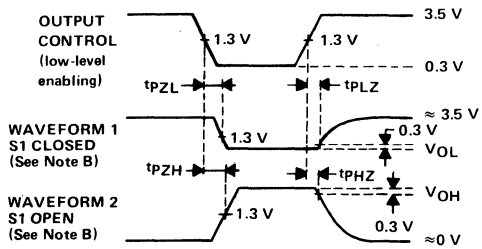
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE WIDTHS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f$ = 2 ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is open.

FIGURE 1

ALS and AS Circuits

D2856, OCTOBER 1984—REVISED JANUARY 1986

- **3-State I/O-Type Read-Back Inputs**
- **Bus-Structured Pinout**
- **Choice of True or Inverting Logic**
  'ALS994 . . . True Outputs
  'ALS995 . . . Inverting Outputs
- **Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

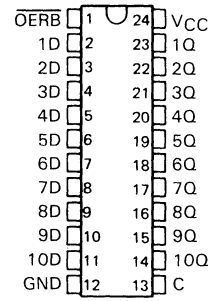
These 10-bit latches are designed specifically for storing the contents of the input data bus plus providing the capability of reading-back the stored data onto the input data bus.

The ten latches of the 'ALS994 and 'ALS995 are transparent D-type. While the enable (C) is high, the Q outputs of the 'ALS994 will follow the data (D) inputs. For the 'ALS995, the Q outputs will provide the inverse of what is applied to its data (D) inputs.

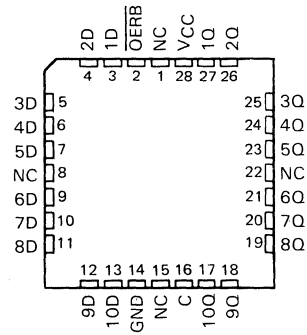
Read-back is provided through the read-back control input ($\overline{OERB}$). When the control is taken low, the data present at the output of the data latches will be allowed to pass back onto the input data bus. When it is taken high, the output of the data latches will be isolated from the data (D) inputs. The read-back control does not affect the internal operation of the latches; however, precautions should be taken not to create a bus-conflict situation.

The SN74ALS994 and SN74ALS995 are characterized for operation from 0°C to 70°C.

SN74ALS994 . . . DW OR NT PACKAGE
(TOP VIEW)

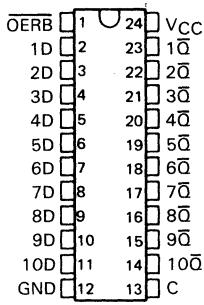


SN74ALS994 . . . FN PACKAGE
(TOP VIEW)



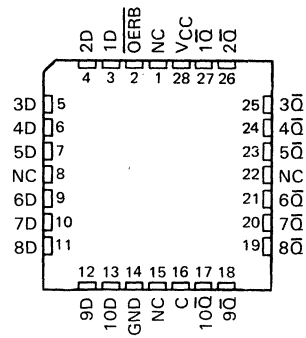
NC—No internal connection.

SN74ALS995 . . . DW OR NT PACKAGE
(TOP VIEW)



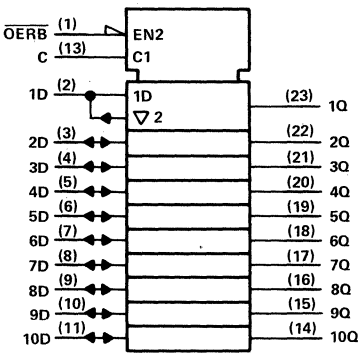
NC—No internal connection

SN74ALS995 . . . FN PACKAGE
(TOP VIEW)

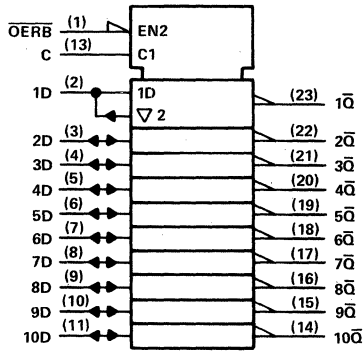


logic symbols†

'ALS994



'ALS995



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW and NT packages.

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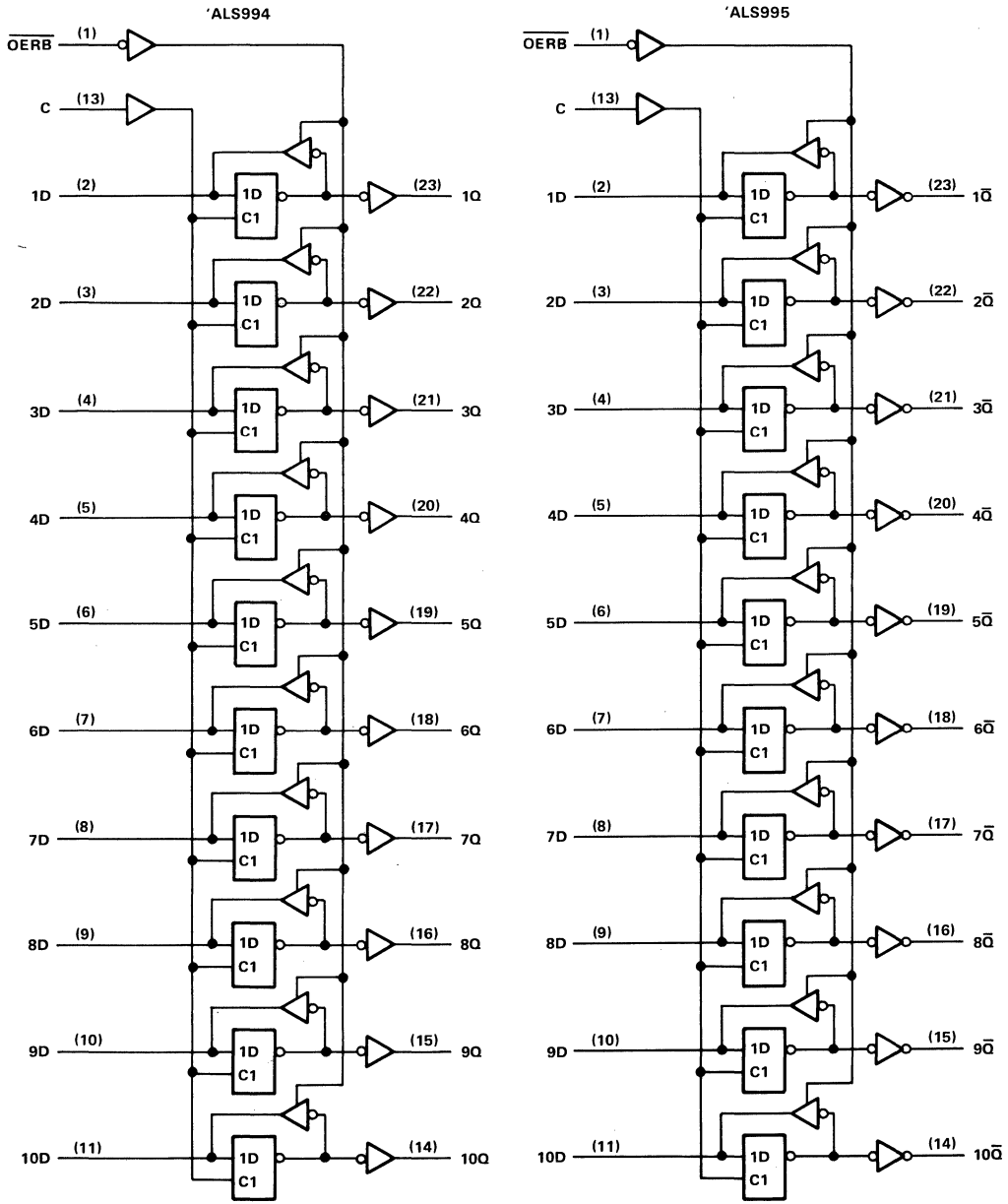
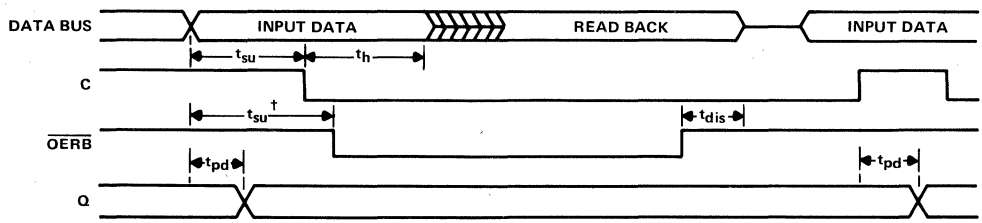
logic diagrams (positive logic)



Pin numbers shown are for DW and NT packages.

timing diagram



†This setup time ensures the readback circuit will not create a conflict on the input data bus.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage ($\overline{OERB}$ and C) . . . . . 7 V
Voltage applied to D inputs . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	Q or $\overline{Q}$			−2.6	mA
		D			−0.4	
I_{OL}	Low-level output current	Q or $\overline{Q}$			24	mA
		D			8	
t_w	Pulse duration, enable C high		10			ns
t_{su}	Setup time	Data before C↓	10			ns
		Data before $\overline{OERB}$↓†	10			
t_h	Hold time	Input data after C↓	5			ns
T_A	Operating free-air temperature		0		70	°C

† This setup time ensures the readback circuit will not create a conflict on the input data bus.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	All outputs	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V
	Q or $\overline{Q}$	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA	2.4	3.2		
V_{OL}	D	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.35	0.5	
	Q or $\overline{Q}$	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 24 mA		0.35	0.5	
I_I	$\overline{OERB}$, C	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
	D inputs	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1	
I_{IH}	$\overline{OERB}$, C	V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
	D inputs‡					20	
I_{IL}	$\overline{OERB}$, C	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1	mA
	D inputs‡					−0.1	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}	'ALS994	V_{CC} = 5.5 V, $\overline{OERB}$ high	Q outputs high		30	50	mA
			Q outputs low		52	82	
	'ALS995		$\overline{Q}$ outputs high		30	50	
			$\overline{Q}$ outputs low		55	85	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ The output conditions have been chosen to produce a current that closely approximates one-half the true short-circuit output current, I_{OS}.

'ALS994 switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, T_A = 0°C to 70°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	D	Q		7	10	3	14	ns
t_{PHL}				11	15	4	18	
t_{PLH}	C	Q		12	16	6	21	ns
t_{PHL}				16	21	8	27	
t_{en}	$\overline{OERB}$	D		11	17	4	21	ns
t_{dis}				9	13	2	16	

'ALS995 switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, T_A = 0°C to 70°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	D	$\overline{Q}$		12	16	6	20	ns
t_{PHL}				9	12	4	15	
t_{PLH}	C	$\overline{Q}$		17	23	9	28	ns
t_{PHL}				14	19	7	22	
t_{en}	$\overline{OERB}$	D		12	18	4	21	ns
t_{dis}				8	12	2	15	

$t_{en} = t_{PZH}$ or t_{PZL}
$t_{dis} = t_{PHZ}$ or t_{PLZ}

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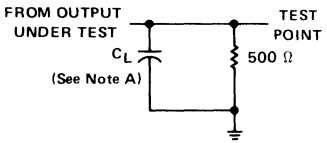
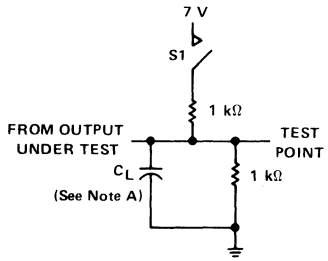
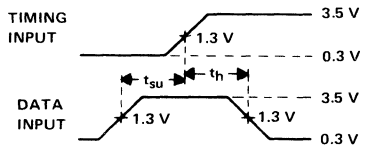
PARAMETER MEASUREMENT INFORMATION



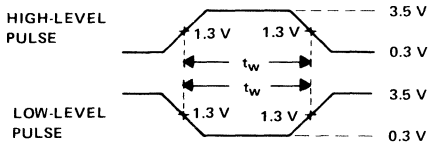
LOAD CIRCUIT FOR
Q OR $\overline{Q}$ OUTPUTS



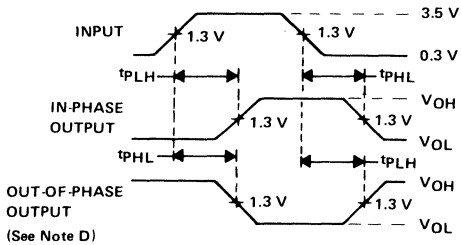
LOAD CIRCUIT FOR D OUTPUTS



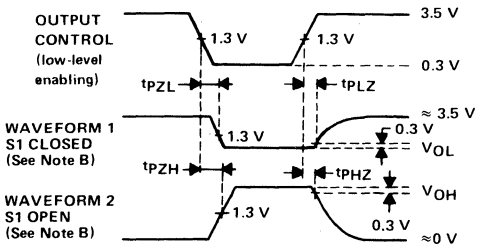
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE WIDTHS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

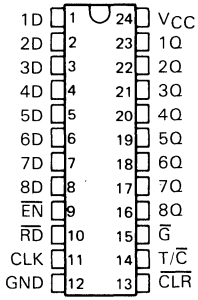
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, t_r = t_f = 2 ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is open.

FIGURE 1

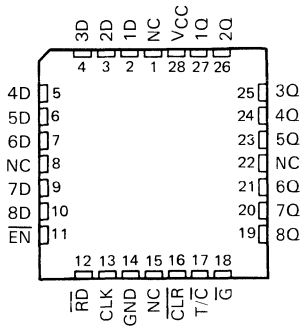
D2854, OCTOBER 1984—REVISED JUNE 1986

- 3-State I/O-Type Read-Back Inputs
- Bus-Structured Pinout
- T/$\overline{C}$ Determines True or Complementary Data at Q Outputs
- Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

DW OR NT PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NC—No internal connection.

description

These 8-bit registers are designed specifically for storing the contents of the input data bus plus providing the capability of reading-back the stored data onto that bus. The Q outputs are designed with bus-driving capability.

The edge-triggered flip-flops enter the data on the low-to-high transition of the clock (CLK) when enable ($\overline{EN}$) is low. Data can be read-back onto the data inputs by taking the read input ($\overline{RD}$) low, in addition to having $\overline{EN}$ low. Whenever $\overline{EN}$ is high, both the read-back and write modes are disabled. Transitions on $\overline{EN}$ should only be made with CLK high in order to prevent false clocking.

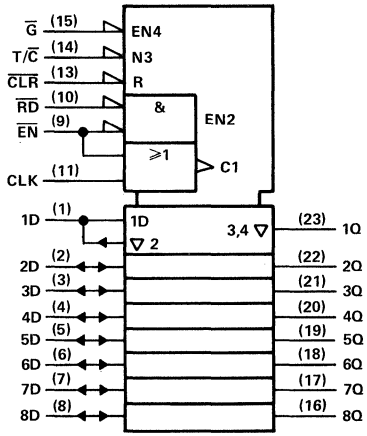
The polarity of the Q outputs can be controlled by the polarity input T/$\overline{C}$. When T/$\overline{C}$ is high, Q will be the same as is stored in the flip-flops. When T/$\overline{C}$ is low, the output data will be inverted. The Q outputs can be placed in a high-impedance state by taking the output control ($\overline{G}$) high. The output control $\overline{G}$ does not affect the internal operations of the register. Old data can be retained or new data can be entered while the outputs are off.

A low level at the clear input ($\overline{CLR}$) resets the internal registers low. The clear function is asynchronous and overrides all other register functions.

The -1 version of the SN74ALS996 is identical to the standard version except that the recommended maximum I_{OL} is increased to 48 milliamperes.

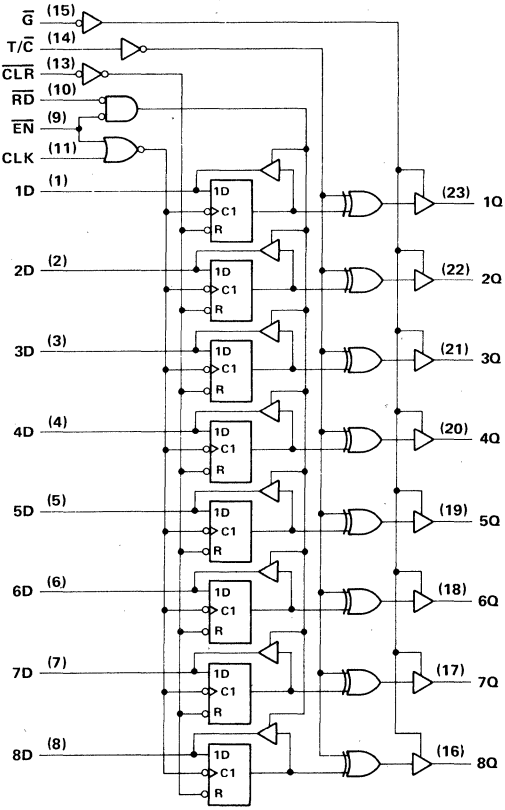
The SN74ALS996 is characterized for operation from 0°C to 70°C.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

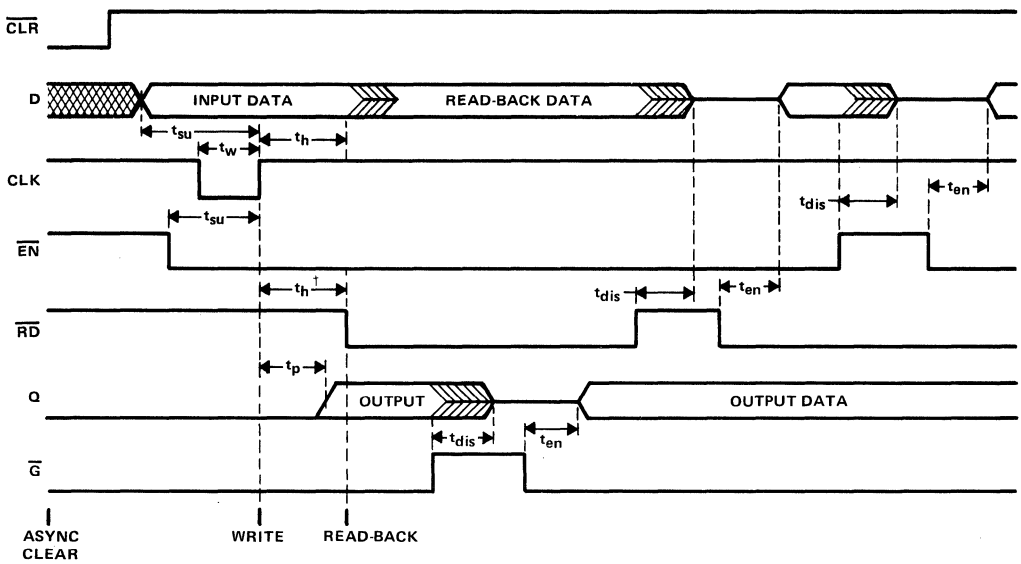


Pin numbers shown are for DW and NT packages.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

timing diagram

($T/\overline{C}$ = H)



†This hold time ensures the readback circuit will not create a conflict on the input data bus.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage ($\overline{G}$, $\overline{RD}$, $\overline{EN}$, CLK, $\overline{CLR}$, and $T/\overline{C}$) . . . . . 7 V
Voltage applied to D inputs and to disabled 3-state outputs . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	Q			−2.6	mA
		D			−0.4	
I_{OL}	Low-level output current	Q			24	mA
					48†	
		D			8	
f_{clock}	Clock frequency		0		35	MHz
t_w	Pulse duration	$\overline{CLR}$ low	10			ns
		CLK low	14.5			
		CLK high	14.5			
t_{su}	Setup time	Data before CLK↑	15			ns
		$\overline{EN}$ low before CLK↑	10			
		CLK high before $\overline{EN}$↑‡	15			
		$\overline{CLR}$ high (inactive) before CLK↑	10			
t_h	Hold time	Data after CLK↑	0			ns
		$\overline{EN}$ low after CLK↑	5			
		$\overline{RD}$ high after CLK↑§	5			
T_A	Operating free-air temperature		0		70	°C

†The 48-mA limit applies only to the -1 versions and only if V_{CC} is maintained between 4.75 V and 5.25 V.
‡This setup time guarantees that $\overline{EN}$ will not false clock the data register.
§This hold time ensures there will be no conflict on the input data bus.

TEXAS INSTRUMENTS
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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	All outputs	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V
	Q	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA	2.4	3.2		
V_{OL}	D	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.35	0.5	
	Q	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 24 mA		0.35	0.5	
		V_{CC} = 4.75 V,	I_{OL} = 48 mA (-1 versions)		0.35	0.5	
I_{OZH}	Q	V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−20	
I_I	D inputs	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1	mA
	All others	V_{CC} = 5.5 V,	V_I = 7 V			0.1	
I_{IH}	D inputs‡	V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
	All others					20	
I_{IL}	D inputs‡	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1	mA
	All others					−0.1	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V, EN, RD low	Q outputs high		35	55	mA
			Q outputs low		55	85	
			Q outputs disabled		42	65	

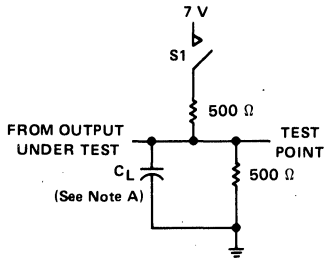
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ The output conditions have been chosen to produce current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 1)

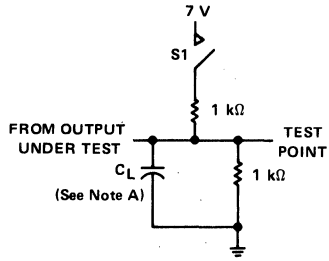
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, T_A = 0°C to 70°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
f_{max}				40		35		MHz
t_{PLH}	CLK ($T/\overline{C}$ = H or L)	Q		16	24	5	28	ns
t_{PHL}				16	24	5	28	
t_{PLH}	$\overline{CLR}$ ($T/\overline{C}$ = L)	Q		15	23	7	27	ns
t_{PHL}	$\overline{CLR}$ ($T/\overline{C}$ = H)			13	19	7	23	
t_{PLH}	$T/\overline{C}$	Q		13	20	5	23	ns
t_{PHL}				13	20	5	23	
t_{PHL}	$\overline{CLR}$	D		19	25	8	30	ns
t_{en}	$\overline{RD}$	D		9	15	3	16	ns
t_{dis}				10	16	3	19	
t_{en}	$\overline{EN}$	D		9	14	3	16	ns
t_{dis}				10	16	3	19	
t_{en}	$\overline{G}$	Q		8	13	4	15	ns
t_{dis}				4	8	1	10	

t_{en} = t_{PZH} or t_{PZL}
t_{dis} = t_{PHZ} or t_{PLZ}

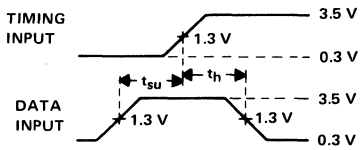
PARAMETER MEASUREMENT INFORMATION



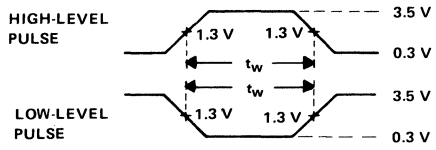
LOAD CIRCUIT FOR Q OUTPUTS



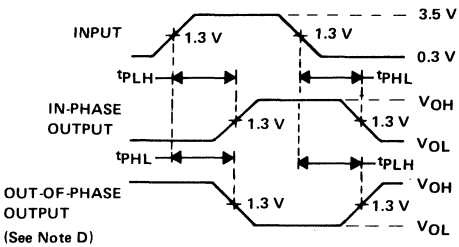
LOAD CIRCUIT FOR D OUTPUTS



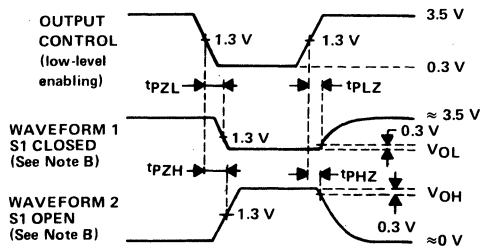
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE WIDTHS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f$ = 2 ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is open.

FIGURE 1

TEXAS INSTRUMENTS
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D2661, APRIL 1984—REVISED MAY 1986

- **'ALS1000A is a Buffer Version of 'ALS00B**
- **'AS1000A is a Driver Version of 'AS00**
- **'AS1000A Offers High Capacitive-Driver Capability**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

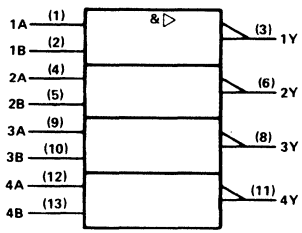
These devices contain four independent 2-input NAND buffers/drivers. They perform the Boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The SN54ALS1000A and SN54AS1000A are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS1000A and SN74AS1000A are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

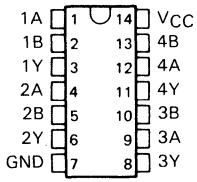
INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol†

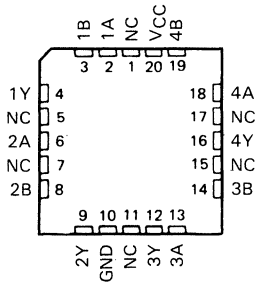


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54ALS1000A, SN54AS1000A . . . J PACKAGE
SN74ALS1000A, SN74AS1000A . . . D OR N PACKAGE
(TOP VIEW)

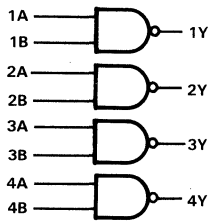


SN54ALS1000A, SN54AS1000A . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



2 ALS and AS Circuits

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS1000A . . . . . −55°C to 125°C
SN74ALS1000A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS1000A			SN74ALS1000A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating-free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS1000A			SN74ALS1000A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.86	1.6		0.86	1.6	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		4.8	7.8		4.8	7.8	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX			UNIT
			'ALS1000A	SN54ALS1000A		SN74ALS1000A	
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	4	2	10	2	8	ns
t_{PHL}	A or B	Y	5	2	10	2	7	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS1000A . . . . . −55°C to 125°C
SN74AS1000A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS1000A			SN74AS1000A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−40			−48	mA
I_{OL}	Low-level output current			40			48	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating-free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS1000A			SN74AS1000A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −40 mA	2						
	V_{CC} = 4.5 V,	I_{OL} = −48 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 40 mA		0.25	0.5				V
	V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−50		−200	−50		−200	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		2.2	3.5		2.2	3.5	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		12	19		12	19	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

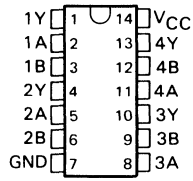
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L1 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS1000A		SN74AS1000A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1	5	1	4	ns
t_{PHL}	A or B	Y	1	5	1	4	ns

NOTE 1. Load circuit and voltage waveforms are shown in Section 1.

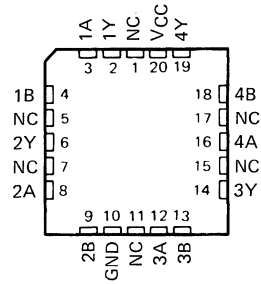
D2661, DECEMBER 1983—REVISED MAY 1986

- **Quad Versions of 'ALS805A**
- **Buffer Version of 'ALS02**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS1002A . . . J PACKAGE
SN74ALS1002A . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS1002A . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

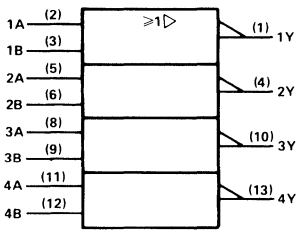
These devices contain four independent 2-input NOR buffers. They perform the Boolean functions $Y = \overline{A+B}$ or $Y = \overline{A} \cdot \overline{B}$ in positive logic.

The SN54ALS1002A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS1002A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

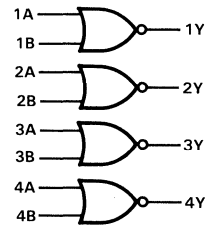
INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS1002A . . . . . −55°C to 125°C
SN74ALS1002A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS1002A			SN74ALS1002A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating-free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS1002A			SN74ALS1002A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		1.7	2.8		1.7	2.8	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		5.6	9		5.6	9	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS1002A	SN54ALS1002A		SN74ALS1002A		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	4	2	10	2	8	ns
t_{PHL}	A or B	Y	4	2	10	2	7	ns

NOTE 1. Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

- **Buffer Version of 'ALS03B**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

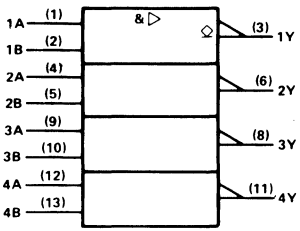
These devices contain four independent 2-input NAND buffers. They perform the Boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN54ALS1003A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS1003A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

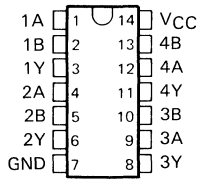
INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol†

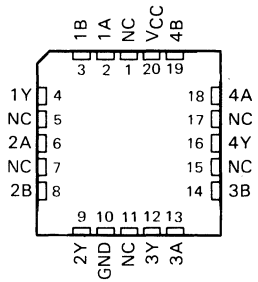


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54ALS1003A . . . J PACKAGE
SN74ALS1003A . . . D OR N PACKAGE
(TOP VIEW)

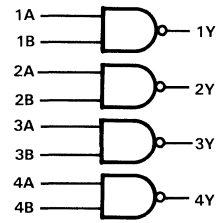


SN54ALS1003A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

logic diagram (positive logic)



2 ALS and AS Circuits

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS1003A . . . . . −55°C to 125°C
SN74ALS1003A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS1003A			SN74ALS1003A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating-free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS1003A			SN74ALS1003A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.86	1.6		0.86	1.6	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		4.8	7.8		4.8	7.8	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 680 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX				UNIT
			'ALS1003A	SN54ALS1003A		SN74ALS1003A		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	18	10	40	10	33	ns
t_{PHL}	A or B	Y	7	2	18	2	12	ns

NOTE 1. Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

D2661, APRIL 1982 – REVISED MAY 1986

- **'AS1004A Offers High Capacitive-Drive Capability**
- **Driver Version of 'ALS04 and 'AS04**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

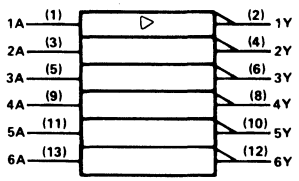
These devices contain six independent inverting drivers. They perform the Boolean function $Y = \overline{A}$.

The SN54ALS1004 and SN54AS1004A are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS1004 and SN74AS1004A are characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each inverter)

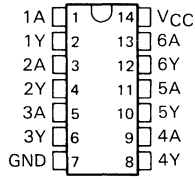
INPUT A	OUTPUT Y
H	L
L	H

logic symbol†

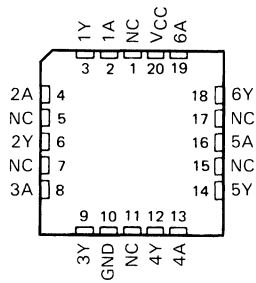


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54ALS1004, SN54AS1004A . . . J PACKAGE
SN74ALS1004, SN74AS1004A . . . D OR N PACKAGE
(TOP VIEW)

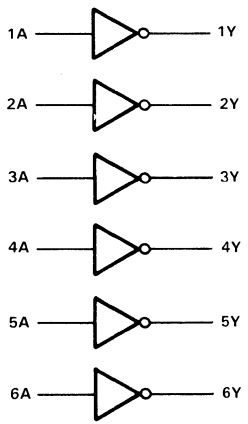


SN54ALS1004, SN54AS1004A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS1004 . . . . . −55°C to 125°C
SN74ALS1004 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS1004			SN74ALS1004			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS1004			SN74ALS1004			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.84	3		0.84	3	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		7	12		7	12	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS1004		SN74ALS1004		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1	9	1	7	ns
t_{PHL}			1	8	1	6	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS1004A . . . . . −55°C to 125°C
SN74AS1004A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS1004A			SN74AS1004A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−40			−48	mA
I_{OL}	Low-level output current			40			48	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS1004A			SN74AS1004A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 to 5.5 V,	I_{OH} = −2 mA	V_{CC} − 2			V_{CC} − 2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −40 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −48 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 40 mA		0.25	0.5				V
	V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−50		−200	−50		−200	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		3.5	5		3.5	5	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		16	27		16	27	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS1004A		SN74AS1004A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1	5	1	4	ns
t_{PHL}			1	5	1	4	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

D2661, APRIL 1982–REVISED MAY 1986

- **Buffer Version of 'ALS05**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

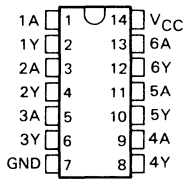
These devices contain six independent inverting buffers. They perform the Boolean function $Y = \overline{A}$. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN54ALS1005 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS1005 is characterized for operation from 0°C to 70°C.

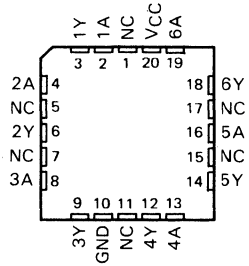
FUNCTION TABLE (each inverter)

INPUT A	OUTPUT Y
H	L
L	H

SN54ALS1005 . . . J PACKAGE
SN74ALS1005 . . . D OR N PACKAGE
(TOP VIEW)

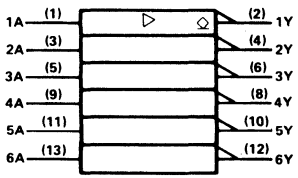


SN54ALS1005 . . . FK PACKAGE
(TOP VIEW)



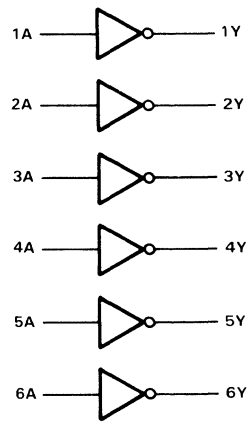
NC – No internal connection

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS1005 . . . . . −55 °C to 125 °C
SN74ALS1005 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS1005			SN74ALS1005			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS1005			SN74ALS1005			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.9	3		0.9	3	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		7	12		7	12	mA

†All typical values are at V_{CC} = 5 V, T_A = 25 °C

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX				UNIT
			SN54ALS1005		SN74ALS1005		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	5	35	5	30	ns
t_{PHL}			2	12	2	10	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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D2661, DECEMBER 1982—REVISED MAY 1986

- **'ALS1008A is a Buffer Version of 'ALS08**
- **'AS1008A is a Driver Version of 'AS08**
- **'AS1008A Offers High Capacitive Drive Capability**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

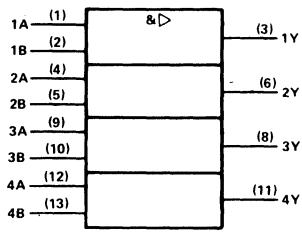
These devices contain four independent 2-input AND buffers/drivers. They perform the Boolean functions $Y = A \cdot B$ or $Y = \overline{\overline{A} + \overline{B}}$ in positive logic.

The SN54ALS1008A and SN54AS1008A are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS1008A and SN74AS1008A are characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each gate)

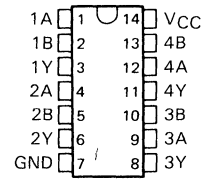
INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

logic symbol†

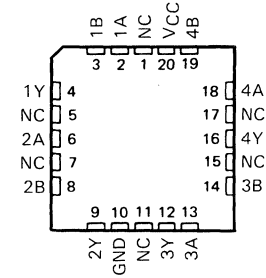


Pin numbers shown are for D, J, and N packages.
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN54ALS1008A, SN54AS1008A . . . J PACKAGE
SN74ALS1008A, SN74AS1008A . . . D OR N PACKAGE
(TOP VIEW)

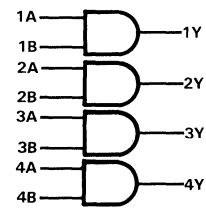


SN54ALS1008A, SN54AS1008A . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS1008A . . . . . −55°C to 125°C
SN74ALS1008A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS1008A			SN74ALS1008A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS1008A			SN74ALS1008A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4				V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		1.8	3		1.8	3	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		5.7	9.3		5.7	9.3	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS1008A		SN74ALS1008A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	2	11	2	9	ns
t_{PHL}			3	11	3	9	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS1008A . . . . . −55°C to 125°C
SN74AS1008A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS1008A			SN74AS1008A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−40			−48	mA
I_{OL}	Low-level output current			40			48	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS1008A			SN74AS1008A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC} − 2			V_{CC} − 2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −40 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −48 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 40 mA		0.25	0.5				V
	V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−50		−200	−50		−200	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		5.6	9.5		5.6	9.5	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		13.5	22		13.5	22	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS1008A		SN74AS1008A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1	6.5	1	6	ns
t_{PHL}			1	6.5	1	6	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2661, APRIL 1982—REVISED MAY 1986

- **Buffer Version of 'ALS10A**
- **Package Options Include Plastic "Small Outline" DIPs and Ceramic Chip Carriers in Addition to the Standard 300-mil Plastic and Ceramic DIPs.**
- **Dependable Texas Instruments Quality and Reliability**

description

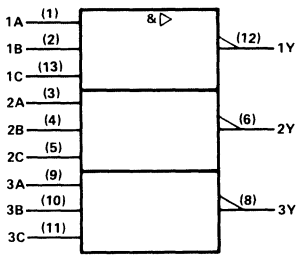
These devices contain three independent 3-input NAND buffers. They perform the Boolean functions $Y = \overline{A \cdot B \cdot C}$ or $Y = \overline{A} + \overline{B} + \overline{C}$ in positive logic.

The SN54ALS1010A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS1010A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (EACH GATE)

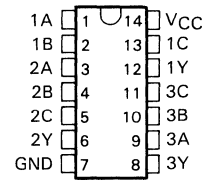
INPUTS			OUTPUT
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

logic symbol†

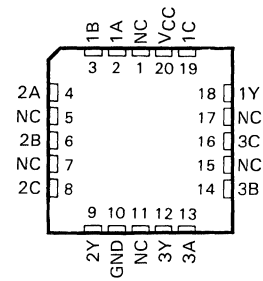


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54ALS1010A . . . J PACKAGE
SN74ALS1010A . . . D OR N PACKAGE
(TOP VIEW)

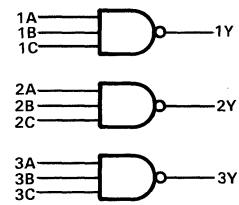


SN54ALS1010A . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



2 ALS and AS Circuits

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS1010A . . . . . −55°C to 125°C
SN74ALS1010A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS1010A			SN74ALS1010A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS1010A			SN74ALS1010A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.65	1.2		0.65	1.2	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		3.6	5.8		3.6	5.8	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX			UNIT
			'ALS1010A	SN54ALS1010A		SN74ALS1010A	
			TYP	MIN	MAX	MIN	MAX
t_{PLH}	Any	Y	5	2	12	2	8	ns
t_{PHL}			5	2	12	2	8	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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D2661, APRIL 1982—REVISED MAY 1986

- **Buffer Version of 'ALS11**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

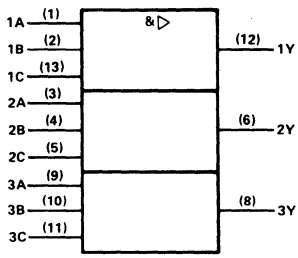
These devices contain three independent 3-input AND buffers. They perform the Boolean functions $Y = A \cdot B \cdot C$ or $Y = \overline{\overline{A}+\overline{B}+\overline{C}}$ in positive logic.

The SN54ALS1011A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS1011A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

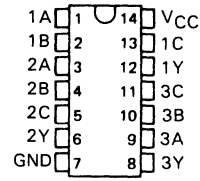
INPUTS			OUTPUT
A	B	C	Y
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

logic symbol†

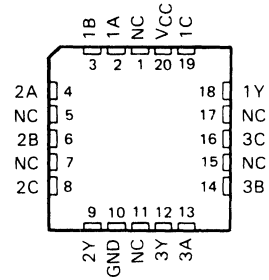


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54ALS1011A . . . J PACKAGE
SN74ALS1011A . . . D OR N PACKAGE
(TOP VIEW)

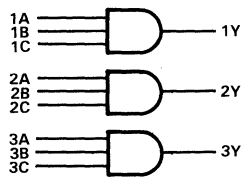


SN54ALS1011A . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS1011A . . . . . −55°C to 125°C
SN74ALS1011A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS1011A			SN74ALS1011A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS1011A			SN74ALS1011A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		1.4	2.3		1.4	2.3	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		4.3	7		4.3	7	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS1011A		SN74ALS1011A		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	2	12	2	10	ns
t_{PHL}			3	11	3	9	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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D2661, APRIL 1982—REVISED MAY 1986

- **Buffer Version of 'ALS20B**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

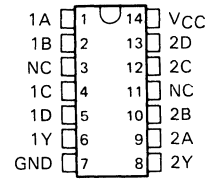
These devices contain two independent 4-input NAND buffers. They perform the Boolean functions $Y = \overline{A \cdot B \cdot C \cdot D}$ or $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D}$ in positive logic.

The SN54ALS1020A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS1020A is characterized for operation from 0°C to 70°C.

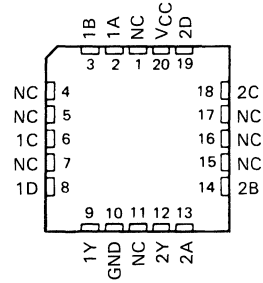
FUNCTION TABLE (each gate)

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

SN54ALS1020A . . . J PACKAGE
SN74ALS1020A . . . D OR N PACKAGE
(TOP VIEW)

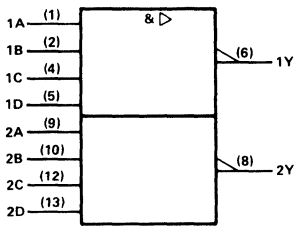


SN54ALS1020A . . . FK PACKAGE
(TOP VIEW)



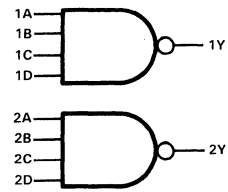
NC—No internal connection

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS1020A . . . . . −55°C to 125°C
SN74ALS1020A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS1020A			SN74ALS1020A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS1020A			SN74ALS1020A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA,	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.3		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.5	0.8		0.5	0.8	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		2.4	3.9		2.4	3.9	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX		UNIT
			'ALS1020A	SN54ALS1020A	SN74ALS1020A	
			TYP	MIN MAX	MIN MAX	
t_{PLH}	Any	Y	5	2 10	2 8	ns
t_{PHL}			5	2 10	2 7	

NOTE 1. Load circuit and voltage waveforms are shown in Section 1.

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D2661, DECEMBER 1982—REVISED MAY 1986

- **'ALS1032A is a Buffer Version of 'ALS32**
- **'AS1032A is a Driver Version of 'AS32**
- **'AS1032A Offers High Capacitive Drive Capability**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

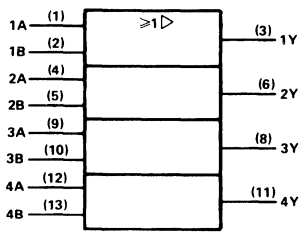
These devices contain four independent 2-input OR buffers/drivers. They perform the Boolean functions $Y = A + B$ or $Y = \overline{\overline{A} \cdot \overline{B}}$ in positive logic.

The SN54ALS1032A and SN54AS1032A are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS1032A and SN74AS1032A are characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each gate)

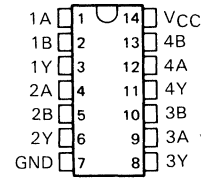
INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

logic symbol†

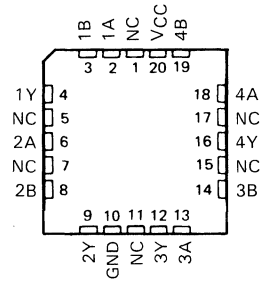


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54ALS1032A, SN54AS1032A . . . J PACKAGE
SN74ALS1032A, SN74AS1032A . . . D or N PACKAGE
(TOP VIEW)

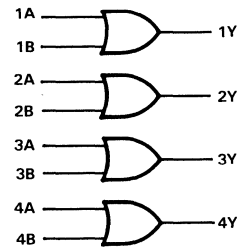


SN54ALS1032A, SN54AS1032A . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



2 ALS and AS Circuits

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS1032A . . . . . −55°C to 125°C
SN74ALS1032A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS1032A			SN74ALS1032A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS1032A			SN74ALS1032A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		2.5	5		2.5	5	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		6.6	10.6		6.6	10.6	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX			UNIT
			'ALS1032A	SN54ALS1032A		SN74ALS1032A	
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	6	2	12	2	9	ns
t_{PHL}			7	3	15	3	12	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS1032A . . . . . −55°C to 125°C
SN74AS1032A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS1032A			SN74AS1032A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−40			−48	mA
I_{OL}	Low-level output current			40			48	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS1032A			SN74AS1032A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −40 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −48 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 40 mA		0.25	0.5				V
	V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−50		−200	−50		−200	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		7.7	11.5		7.7	11.5	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		14.7	24		14.7	24	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

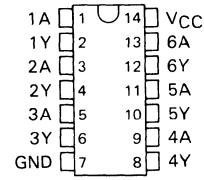
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS1032A		SN74AS1032A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1	7	1	6.3	ns
t_{PHL}			1	7	1	6.3	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

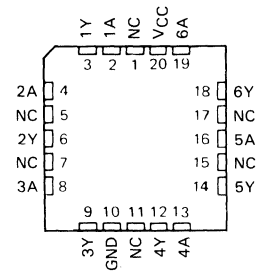
D2661, APRIL 1982—REVISED MAY 1986

- **'AS1034A Offers High Capacitive-Drive Capability**
- **Noninverting Drivers**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS1034, SN54AS1034A . . . J PACKAGE
SN74ALS1034, SN74AS1034A . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS1034, SN54AS1034A . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

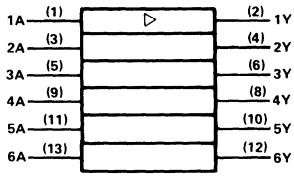
These devices contain six independent noninverting drivers. They perform the Boolean functions Y = A.

The SN54ALS1034 and SN54AS1034A are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS1034 and SN74AS1034A are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each buffer)

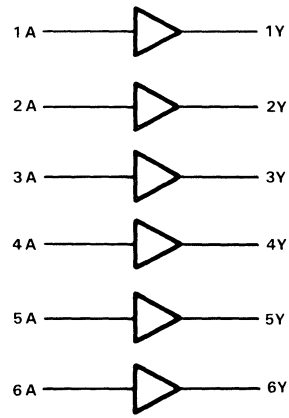
INPUT A	OUTPUT Y
H	H
L	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



2 ALS and AS Circuits

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS1034 . . . . . −55°C to 125°C
SN74ALS1034 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS1034			SN74ALS1034			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output curent			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS1034			SN74ALS1034			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4				V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		3	6		3	6	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		8	14		8	14	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS1034		SN74ALS1034		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1	11	1	8	ns
t_{PHL}			1	13	1	8	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS1034A . . . . . −55°C to 125°C
SN74AS1034A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS1034A			SN74AS1034A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−40			−48	mA
I_{OL}	Low-level output current			40			48	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS1034A			SN74AS1034A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −40 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −48 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 40 mA		0.25	0.5				V
	V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−50		−200	−50		−200	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		9	15		9	15	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		21	35		21	35	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

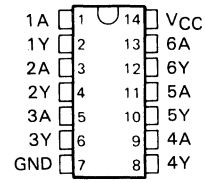
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS1034A		SN74AS1034A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1	6.5	1	6	ns
t_{PHL}			1	6.5	1	6	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

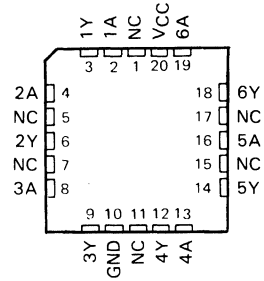
D2661, APRIL 1982—REVISED MAY 1986

- **Noninverting Buffers with Open-Collector Outputs**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS1035 . . . J PACKAGE
SN74ALS1035 . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS1035 . . . FK PACKAGE
(TOP VIEW)



NC–No internal connection

description

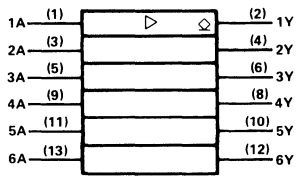
These devices contain six independent noninverting buffers. They perform the boolean functions Y = A. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN54ALS1035 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS1035 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each buffer)

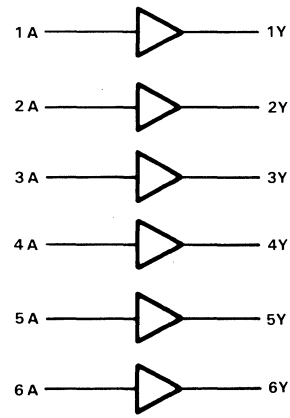
INPUT A	OUTPUT Y
H	H
L	L

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS1035 . . . . . −55°C to 125°C
SN74ALS1035 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS1035			SN74ALS1035			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS1035			SN74ALS1035			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		3	6		3	6	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		8	14		8	14	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX				UNIT
			SN54ALS1035		SN74ALS1035		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	5	35	5	30	ns
t_{PHL}			2	14	2	12	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
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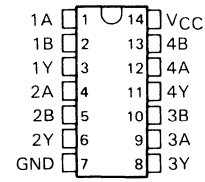
D2661, DECEMBER 1983—REVISED MAY 1986

- Quad Versions of AS805B
- Offers High Capacitive-Drive Capability
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

SN54AS1036A . . . J PACKAGE
SN74AS1036A . . . D OR N PACKAGE
(TOP VIEW)



description

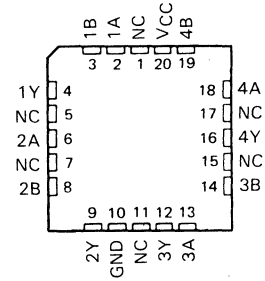
These devices contain four independent 2-input NOR drivers. They perform the Boolean functions $Y = \overline{A+B}$ or $Y = \overline{A} \cdot \overline{B}$ in positive logic.

The SN54AS1036A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS1036A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

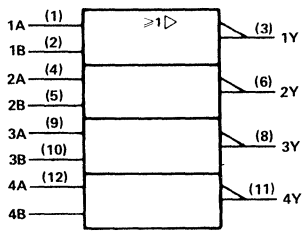
INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

SN54AS1036A . . . FK PACKAGE
(TOP VIEW)



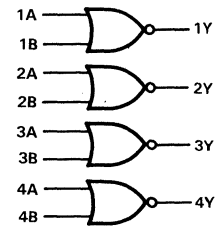
NC—No internal connection

logic symbol



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS1036A . . . . . −55°C to 125°C
SN74AS1036A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS1036A			SN74AS1036A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−40			−48	mA
I_{OL}	Low-level output current			40			48	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS1036A			SN74AS1036A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −40 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −48 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 40 mA		0.25	0.5				V
	V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−50		−200	−50		−200	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		4.3	7		4.3	7	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		14	23		14	23	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS1036A		SN74AS1036A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1	4.8	1	4.3	ns
t_{PHL}			1	4.8	1	4.3	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

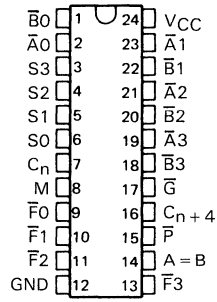
TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SN54AS1181, SN74AS1181
ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

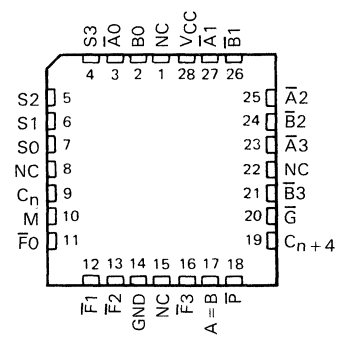
D1915, MAY 1985—REVISED MAY 1986

- Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Full Look-Ahead for High-Speed Operations on Long Words
- Arithmetic Operating Modes:
  - Addition
  - Subtraction
  - Shift Operand A One Position
  - Magnitude Comparison
  - Plus Twelve Other Arithmetic Operations
- Logic Function Modes
  - Exclusive-OR
  - Comparator
  - AND, NAND, OR, NOR
- Dependable Texas Instruments Quality and Reliability

SN54AS1181 . . . JT OR JW PACKAGE
SN74AS1181 . . . DW, NT, OR NW PACKAGE
(TOP VIEW)

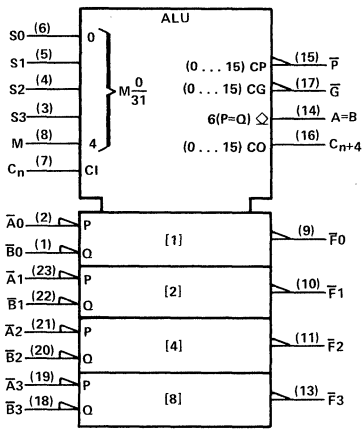


SN54AS1181 . . . FK PACKAGE
SN74AS1181 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, JW, NT, and NW packages.

TYPICAL ADDITION TIMES (C_L = 15 pF, R_L = 280 Ω, T_A = 25°C

NUMBER OF BITS	ADDITION TIMES USING 'AS1181 AND 'AS882	ADDITION TIMES USING 'AS181A AND 'AS882	ADDITION TIMES USING 'S181 AND 'S182	PACKAGE COUNT ARITHMETIC LOGIC UNITS	PACKAGE COUNT LOOK-AHEAD CARRY GENERATORS	CARRY METHOD BETWEEN ALUs
1 to 4	5 ns	5 ns	11 ns	1		NONE
5 to 8	10 ns	10 ns	18 ns	2		RIPPLE
9 to 16	14 ns	14 ns	19 ns	3 or 4	1	FULL LOOK-AHEAD
17 to 64	19 ns	19 ns	28 ns	5 to 16	2 to 5	FULL LOOK-AHEAD

TEXAS INSTRUMENTS
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description

The 'AS1181 arithmetic logic units (ALU)/function generators have a complexity of 75 equivalent gates on a monolithic chip. These circuits perform 16 binary arithmetic operations on two 4-bit words as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of two cascade-outputs (pins 15 and 17) for the four bits in the package. When used in conjunction with the SN54AS882 or SN74AS882 full carry look-ahead circuits, high-speed arithmetic operations can be performed. The typical addition times shown previously illustrate the little additional time required for addition of longer words when full carry look-ahead is employed. The method of cascading 'AS882 circuits with these ALUs to provide multilevel full carry look-ahead is illustrated under signal designations.

If high speed is not of importance, a ripple-carry input (C_n) and a ripple-carry output (C_{n+4}) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

The 'AS1181 will accommodate active-high or active-low data if the pin designations are interpreted as follows:

PIN NUMBER	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-low data (Table 1)	$\overline{A}0$	$\overline{B}0$	$\overline{A}1$	$\overline{B}1$	$\overline{A}2$	$\overline{B}2$	$\overline{A}3$	$\overline{B}3$	$\overline{F}0$	$\overline{F}1$	$\overline{F}2$	$\overline{F}3$	C_n	C_{n+4}	$\overline{P}$	$\overline{G}$
Active-high data (Table 2)	A0	B0	A1	B1	A2	B2	A3	B3	F0	F1	F2	F3	$\overline{C}_n$	$\overline{C}_{n+4}$	X	Y

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A − B − 1, which requires an end-around or forced carry to provide A − B.

The 'AS1181 can also be utilized as a comparator. The A = B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A = B). The ALU must be in the subtract mode with C_n = H when performing this comparison. The A = B output is open-collector so that it can be wired-AND connected to give a comparison for more than four bits. The carry output ($C_n + 4$) can also be used to supply relative magnitude information. Again, the ALU must be placed in the subtract mode by placing the function select input S3, S2, S1, S0 at L, H, H, L, respectively.

INPUT C_n	OUTPUT C_{n+4}	ACTIVE-LOW DATA (FIGURE 1)	ACTIVE-HIGH DATA (FIGURE 2)
H	H	A ≥ B	A ≤ B
H	L	A < B	A > B
L	H	A > B	A < B
L	L	A ≤ B	A ≥ B

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR, and OR functions.

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signal designations

In both Figures 1 and 2, the polarity indicators (▷) indicate that the associated input or output is active-low with respect to the function shown inside the symbol and the symbols are the same in both figures. The signal designations in Figure 1 agree with the indicated internal functions based on active-low data, and are for use with the logic functions and arithmetic operations shown in Table 1. The signal designations have been changed in Figure 2 to accommodate the logic functions and arithmetic operations for the active-high data given in Table 2. The 'AS1181 together with 'AS882 and 'S182 can be used with the signal designation of either Figure 1 or Figure 2.

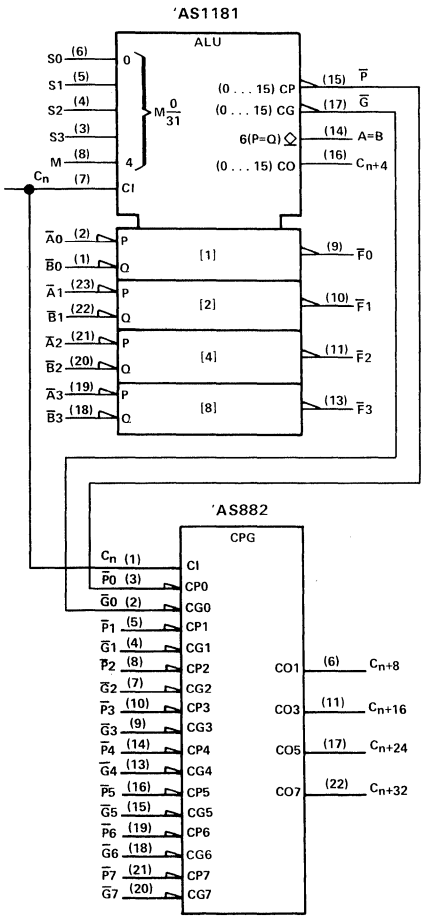

FIGURE 1
(USE WITH TABLE 1)

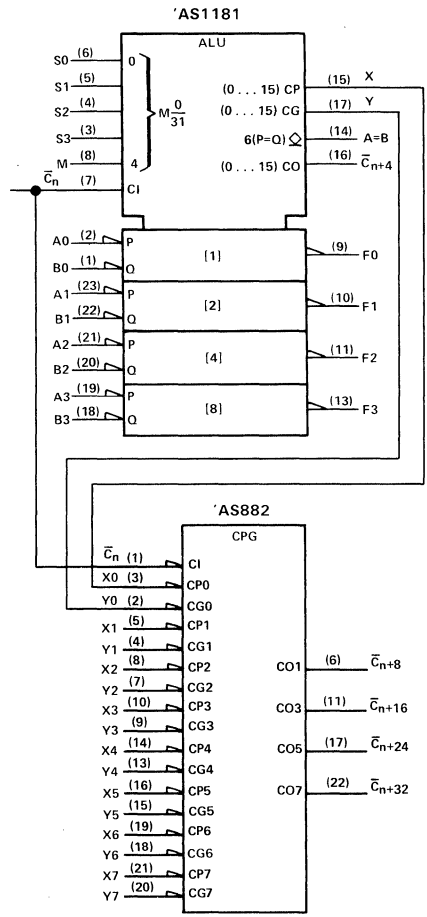

FIGURE 2
(USE WITH TABLE 2)

Pin numbers shown for the 'AS1181 are for DW, JT, JW, NT, and NW packages.

TABLE 1

SELECTION				ACTIVE-LOW DATA		
				M = H	M = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC FUNCTIONS	C_n = L (no carry)	C_n = H (with carry)
L	L	L	L	F = $\overline{A}$	F = A MINUS 1	F = A
L	L	L	H	F = $\overline{A\overline{B}}$	F = AB MINUS 1	F = AB
L	L	H	L	F = $\overline{A}$ + B	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
L	L	H	H	F = 1	F = MINUS 1 (2's COMP)	F = ZERO
L	H	L	L	F = $\overline{A + B}$	F = A PLUS (A + $\overline{B}$)	F = A PLUS (A + $\overline{B}$) PLUS 1
L	H	L	H	F = $\overline{B}$	F = AB PLUS (A + $\overline{B}$)	F = AB PLUS (A + $\overline{B}$) PLUS 1
L	H	H	L	F = $\overline{A \oplus B}$	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	F = A + $\overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
H	L	L	L	F = $\overline{A}$B	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1
H	L	L	H	F = $\overline{A \oplus B}$	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = A$\overline{B}$ PLUS (A + B)	F = A$\overline{B}$ PLUS (A + B) PLUS 1
H	L	H	H	F = A + B	F = (A + B)	F = (A + B) PLUS 1
H	H	L	L	F = 0	F = A PLUS A†	F = A PLUS A PLUS 1
H	H	L	H	F = A$\overline{B}$	F = AB PLUS A	F = AB PLUS A PLUS 1
H	H	H	L	F = AB	F = A$\overline{B}$ PLUS A	F = A$\overline{B}$ PLUS A PLUS 1
H	H	H	H	F = A	F = A	F = A PLUS 1

TABLE 2

SELECTION				ACTIVE-HIGH DATA		
				M = H	M = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC FUNCTIONS	$\overline{C}_n$ = H (no carry)	$\overline{C}_n$ = L (with carry)
L	L	L	L	F = $\overline{A}$	F = A	F = A PLUS 1
L	L	L	H	F = $\overline{A + B}$	F = A + B	F = (A + B) PLUS 1
L	L	H	L	F = $\overline{A}$B	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
L	L	H	H	F = 0	F = MINUS 1 (2's COMPL)	F = ZERO
L	H	L	L	F = $\overline{A\overline{B}}$	F = A PLUS A$\overline{B}$	F = A PLUS A$\overline{B}$ PLUS 1
L	H	L	H	F = $\overline{B}$	F = (A + B) PLUS A$\overline{B}$	F = (A + B) PLUS A$\overline{B}$ PLUS 1
L	H	H	L	F = $\overline{A \oplus B}$	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	F = A$\overline{B}$	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
H	L	L	L	F = $\overline{A}$ + B	F = A PLUS AB	F = A PLUS AB PLUS 1
H	L	L	H	F = $\overline{A \oplus B}$	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = (A + $\overline{B}$) PLUS AB	F = (A + $\overline{B}$) PLUS AB PLUS 1
H	L	H	H	F = AB	F = AB MINUS 1	F = AB
H	H	L	L	F = 1	F = A PLUS A†	F = A PLUS A PLUS 1
H	H	L	H	F = A + $\overline{B}$	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1
H	H	H	L	F = A + B	F = (A + $\overline{B}$) PLUS A	F = (A + $\overline{B}$) PLUS A PLUS 1
H	H	H	H	F = A	F = A MINUS 1	F = A

†Each bit is shifted to the next more significant position.

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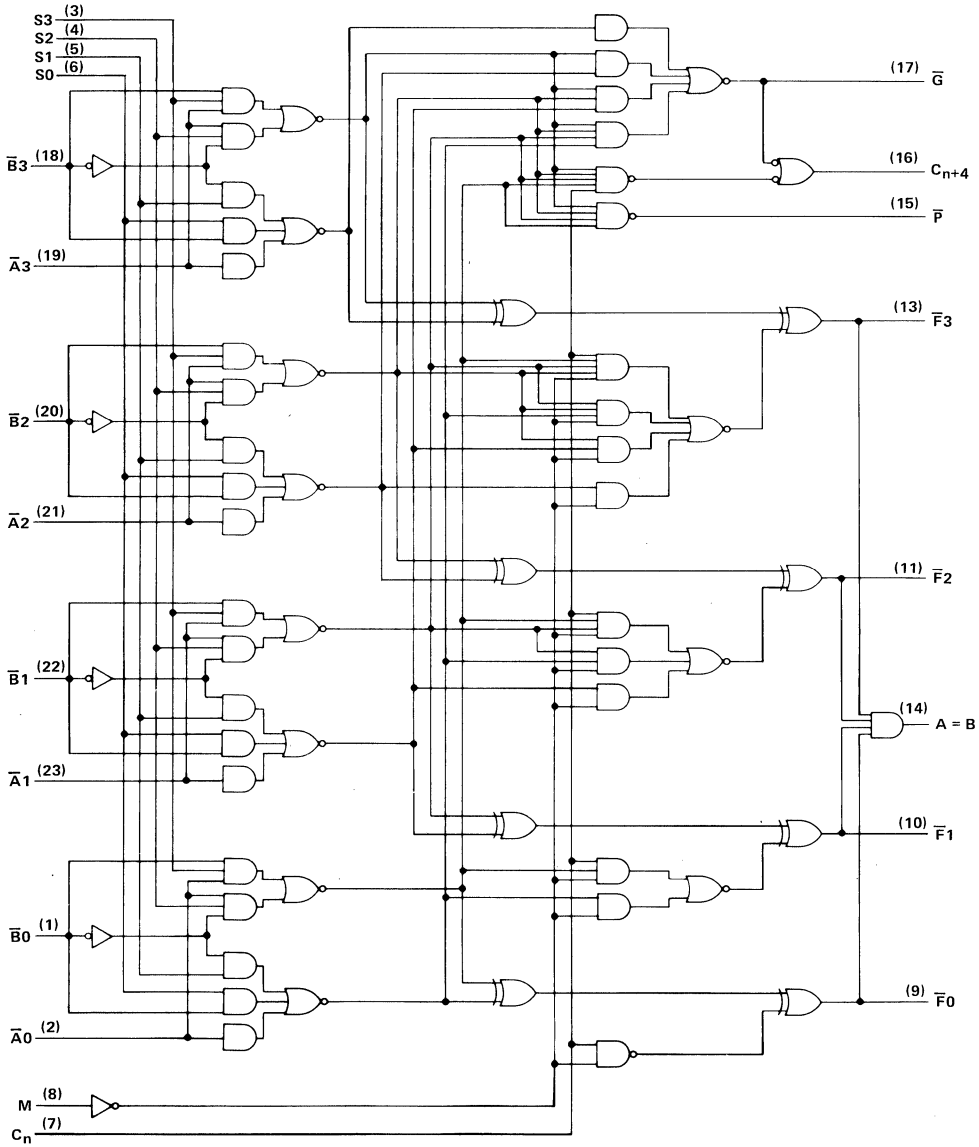
logic diagram (positive logic)

'AS1181



Pin numbers shown are for DW, JT, JW, NT, and NW packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltge (A = B output only) . . . . . 7 V
Operating free-air temperature range: SN54AS1181 . . . . . −55°C to 125°C
SN74AS1181 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54AS1181			SN74AS1181			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{OH}	High-level output voltage	A = B output only			5.5			5.5	V
I_{OH}	High-level output current	All outputs except A = B and $\overline{G}$			−2			−2	mA
		$\overline{G}$ output			−3			−3	mA
I_{OL}	Low-level output current	All outputs except $\overline{G}$			20			20	mA
		$\overline{G}$ output			48			48	mA
T_A	Operating free-air temperature		−55		125	0		70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS1181			SN74AS1181			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	Any output except A = B	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC} − 2			V_{CC} − 2			V
	$\overline{G}$	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3		2.4	3		V
I_{OH}	A = B	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	Any output except $\overline{G}$	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.3	0.5		0.3	0.5	V
	$\overline{G}$	V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.4	0.5		0.4	0.5	V
I_I	M input	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	Any A or B input					0.3			0.3	
	Any S input					0.4			0.4	
	Carry input					0.6			0.6	
I_{IH}	M input	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	Any A or B input					60			60	
	Any S input					80			80	
	Carry input					120			120	
I_{IL}	M input	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	Any A or B input					−1.5			−1.5	
	Any S input					−2			−2	
	Carry input					−3			−3	
I_O‡	All outputs except A=B and $\overline{G}$	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
	$\overline{G}$			−30		−125	−30		−125	
I_{CC}		V_{CC} = 5.5 V			74	117		74	117	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
				SN54AS1181		SN74AS1181		
				MIN	MAX	MIN	MAX	
t_{PLH}	C_n	C_{n+4}		3	9	3	8.5	ns
t_{PHL}				2	7	2	6.5	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	C_{n+4}	M = 0 V, S1 = S2 = 0 V, S0 = S3 = 4.5 V ($\overline{SUM}$ mode)	3.5	13	5	12	ns
t_{PHL}				3.5	12.5	5	12	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	C_{n+4}	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)	5	14.5	5	13	ns
t_{PHL}				5	13.5	5	12.5	
t_{PLH}	C_n	Any $\overline{F}$	M = 0 V ($\overline{SUM}$ or $\overline{DIFF}$ mode)	3	10.5	3	9	ns
t_{PHL}				3	8	3	7.5	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	$\overline{G}$	M = 0 V, S1 = S2 = 0 V, S0 = S3 = 4.5 V ($\overline{SUM}$ mode)	3	8.5	3	8	ns
t_{PHL}				2	7	2	6	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	$\overline{G}$	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)	3	10.5	3	9.5	ns
t_{PHL}				2	9	2	7	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	$\overline{P}$	M = 0 V, S1 = S2 = 0 V, S0 = S3 = 4.5 V ($\overline{SUM}$ mode)	3	8.5	3	7.5	ns
t_{PHL}				2	7.5	2	6	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	$\overline{P}$	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)	3	10.5	3	9	ns
t_{PHL}				3	8.5	3	8	
t_{PLH}	$\overline{A}$i or $\overline{B}$i	$\overline{F}$i	M = 0 V, S1 = S2 = 0 V, S0 = S3 = 4.5 V ($\overline{SUM}$ mode)	3	11	3	9.5	ns
t_{PHL}				3	9	3	7.5	
t_{PLH}	$\overline{A}$i or $\overline{B}$i	$\overline{F}$i	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)	3	12	3	10.5	ns
t_{PHL}				3	11	3	9.5	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	Any $\overline{F}$	M = 0 V, S1 = S2 = 0 V, S0 = S3 = 4.5 V ($\overline{SUM}$ mode)	3	13.5	3	12	ns
t_{PHL}				3	13	3	11.5	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	Any $\overline{F}$	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)	3	16	3	14.5	ns
t_{PHL}				3	13	3	12.5	
t_{PLH}	$\overline{A}$i or $\overline{B}$i	$\overline{F}$i	M = 4.5 V (LOGIC mode)	3	12.5	3	11	ns
t_{PHL}				3	10	3	9.5	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	A = B	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)	4	19	4	17	ns
t_{PHL}				5	18.5	5	15	
t_{PLH}	Any S	Any $\overline{F}$	M = 0 V ($\overline{ARITH}$ mode)	3	12.5	3	11	ns
t_{PHL}				3	11.5	3	11	
t_{PLH}	Any S	A = B	M = 0 V ($\overline{ARITH}$ mode)	5	20	5	18	ns
t_{PHL}				5	21	5	18	
t_{PLH}	Any S	C_{n+4}	M = 4.5 V (LOGIC mode)	2	16.5	4.5	15.5	ns
t_{PHL}				3	12.5	3	12	
t_{PLH}	Any S	$\overline{G}$	M = 0 V ($\overline{ARITH}$ mode)	3	9.5	3	9	ns
t_{PHL}				2	6.5	2	6	
t_{PLH}	Any S	$\overline{P}$	M = 4.5 V (LOGIC mode)	3	8.5	3	7.5	ns
t_{PHL}				2	6.5	2	6.5	
t_{PLH}	M	Any $\overline{F}$	S1 = S2 = 0 V, S0 = S3 = 4.5 V ($\overline{SUM}$ mode)	5	12	5	11.5	ns
t_{PHL}				5	12	5	11.5	
t_{PLH}	M	A = B	S1 = S2 = 0 V, S0 = S3 = 4.5 V ($\overline{SUM}$ mode)	7	19	7	17.5	ns
t_{PHL}				8	21	8	17.5	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

PARAMETER MEASUREMENT INFORMATION

SUM MODE TEST TABLE

FUNCTION INPUTS: S0 = S3 = 4.5 V, S1 = S2 = M = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (SEE NOTE 1)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} / t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}i$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}i$	In-Phase
t_{PLH} / t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}i$	None	$\overline{A}i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	In-Phase
t_{PLH} / t_{PHL}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_{n+4}	In-Phase
t_{PLH} / t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{B}i$	None	$\overline{A}i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}	Out-of-Phase
t_{PLH} / t_{PHL}	Any $\overline{A}$	None	$\overline{B}i$	Remaining $\overline{B}$, $\overline{A}3$	Remaining $\overline{A}$, C_n	Any $\overline{F}$	In-Phase
t_{PLH} / t_{PHL}	Any $\overline{B}$	None	$\overline{A}i$	Remaining $\overline{A}$, $\overline{B}3$	Remaining $\overline{B}$, C_n	Any $\overline{F}$	In-Phase

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

PARAMETER MEASUREMENT INFORMATION

$\overline{\text{DIFF}}$ MODE TEST TABLE

FUNCTION INPUTS: S1 = S2 = 4.5 V, S0 = S3 = M = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (SEE NOTE 1)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}i$	In-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}i$	Out-of-Phase
t_{PLH} t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	Out-of-Phase
t_{PLH} t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	In-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	None	$\overline{A}i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	Out-of-Phase
t_{PLH} t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B	In-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B	Out-of-Phase
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	C_{n+4} or any $\overline{F}$	In-Phase
t_{PLH} t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	None	Remaining $\overline{A}$, $\overline{B}$, C_n	C_{n+4}	Out-of-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	None	$\overline{A}i$	None	Remaining $\overline{A}$, $\overline{B}$, C_n	C_{n+4}	In-Phase
t_{PLH} t_{PHL}	Any $\overline{A}$	$\overline{B}i$	None	$\overline{A}3$	Remaining $\overline{A}$, $\overline{B}$, C_n	Any $\overline{F}$	In-Phase
t_{PLH} t_{PHL}	Any $\overline{B}$	None	$\overline{A}i$	$\overline{A}3$	Remaining $\overline{A}$, $\overline{B}$, C_n	Any $\overline{F}$	Out-of-Phase

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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PARAMETER MEASUREMENT INFORMATION

LOGIC MODE TEST TABLE
FUNCTION INPUTS: S1 = S2 = M = 4.5 V, S0 = S3 = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (SEE NOTE 1)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} t_{PHL}	$\overline{A}i$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}i$	Out-of-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}i$	Out-ot-Phase

INPUT BITS EQUAL/NOT EQUAL TEST TABLE
FUNCTION INPUTS: S0 = S3 = M = 4.5 V, S1 = S2 = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (SEE NOTE 1)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	$\overline{P}$	Out-of-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	$\overline{P}$	Out-of-Phase
t_{PLH} t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	$\overline{P}$	In-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	None	$\overline{A}i$	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	$\overline{P}$	In-Phase
t_{PLH} t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	C_{n+4}	In-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	C_{n+4}	In-Phase
t_{PLH} t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	C_{n+4}	Out-of-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	None	$\overline{A}i$	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	C_{n+4}	Out-of-Phase

INPUT PAIRS HIGH/NOT HIGH TEST TABLE
FUNCTION INPUTS: S2 = M = 4.5 V, S0 = S1 = S3 = 0V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (SEE NOTE 1)
		APPLY 4.5 V	APPLY GND	APPLY 4.5V	APPLY GND		
t_{PLH} t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	Remaining $\overline{A}$, C_n	Remaining $\overline{B}$	$\overline{P}$	In-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	$\overline{P}$	In-Phase
t_{PLH} t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	Remaining $\overline{A}$, C_n	Remaining $\overline{B}$	C_{n+4}	Out-of-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	C_{n+4}	Out-of-Phase

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

PARAMETER MEASUREMENT INFORMATION

SELECT INPUT/LOGIC MODE TEST TABLE
FUNCTION INPUTS: M = 4.5 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (SEE NOTE 1)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH}	Any S	—	—	Remaining $\overline{B}$	$\overline{A}$, $\overline{B}0$, C_n	C_{n+4}	Out-of-Phase
t_{PHL}							
t_{PLH}	Any S	—	—	$\overline{B}$, $\overline{A}2$	Remaining $\overline{A}$, C_n	$\overline{P}$	In-Phase
t_{PHL}							

SELECT INPUT/ARITH MODE TEST TABLE
FUNCTION INPUTS: M = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (SEE NOTE 1)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH}	Any S	—	—	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{A}0$, $\overline{B}0$	Any $\overline{F}$	In-Phase
t_{PHL}							
t_{PLH}	Any S	—	—	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{A}0$, $\overline{B}0$	A = B	In-Phase
t_{PHL}							
t_{PLH}	Any S	—	—	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{A}0$, $\overline{B}0$	$\overline{G}$	In-Phase
t_{PHL}							

MODE INPUT/$\overline{\text{SUM}}$ MODE TEST TABLE
FUNCTION INPUTS: S0 = S3 = 4.5 V, S1 = S2 = 0 V

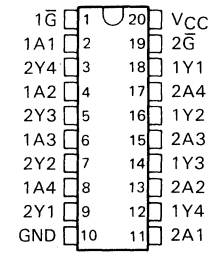
PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (SEE NOTE 1)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH}	M	—	—	Remaining $\overline{A}$ and $\overline{B}$	$\overline{B}2$, $\overline{A}2$, C_n	Any $\overline{F}$	In-Phase
t_{PHL}							
t_{PLH}	M	—	—	Remaining $\overline{A}$ and $\overline{B}$	$\overline{B}1$, $\overline{A}1$, C_n	A = B	In-Phase
t_{PHL}							

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

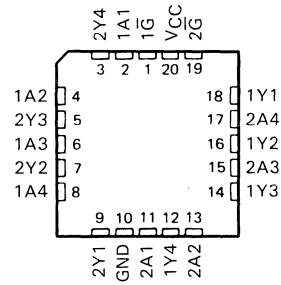
D2661, DECEMBER 1982 – REVISED MAY 1986

- **Low-Power Version of 'ALS240A**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **P-N-P Inputs Reduce DC Loading**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS1240 . . . J PACKAGE
SN74ALS1240 . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS1240 . . . FK PACKAGE
(TOP VIEW)



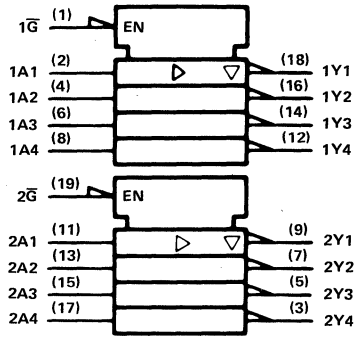
description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs. These devices feature high fan-out and improved fan-in.

The -1 versions of the SN74ALS' parts are identical to the standard versions except that the recommended maximum I_{OL} is increased to 24 milliamperes. There are no -1 versions of the SN54ALS' parts.

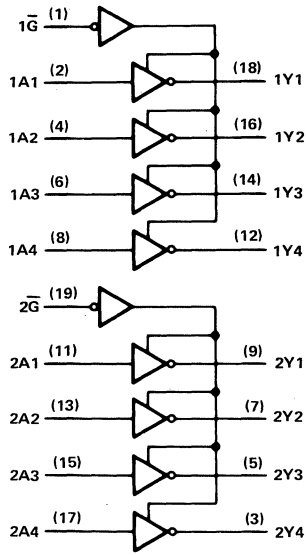
The SN54ALS1240 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS1240 is characterized for operation from 0°C to 70°C.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS1240 . . . . . −55°C to 125°C
SN74ALS1240 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS1240			SN74ALS1240			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			8			16	mA
							24†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 24-mA limit applies for the SN74ALS1240-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS1240			SN74ALS1240			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2		3	V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V, (I_{OL} = 24 mA for -1 versions)	I_{OL} = 16 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}§	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}§	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O¶	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		5	8		5	8	mA
		Outputs low		8.5	14		8.5	14	
		Outputs disabled		8.1	13		8.1	13	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
¶The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS1240	SN54ALS1240		SN74ALS1240		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	7.5	2	16	2	13	ns
t_{PHL}			6.5	2	16	2	13	
t_{PZH}	$\overline{G}$	Y	11.5	4	23	4	20	ns
t_{PZL}			14	6	28	6	22	
t_{PHZ}	$\overline{G}$	Y	7.5	2	12	2	10	ns
t_{PLZ}			8	3	18	3	13	

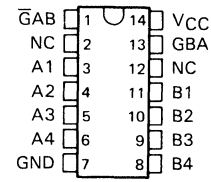
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

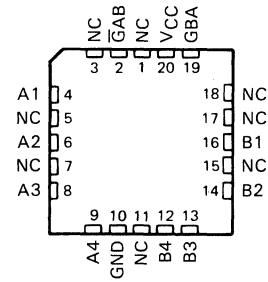
D2661, DECEMBER 1982—REVISED MAY 1986

- **2-Way Asynchonous Communication Between Data Buses**
- **P-N-P Inputs Reduce DC Loading**
- **Low-Power Version of 'ALS242**
- **Three-State Outputs**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS1242 . . . J PACKAGE
SN74ALS1242 . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS1242 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

These quadruple bus transceivers are designed for two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs (GBA and $\overline{GAB}$).

The enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives the 'ALS1242 the capability to store data by simultaneous enabling of $\overline{GAB}$ and GBA. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (8 in all) will remain at their last states. The 4-bit codes appearing on the two sets of buses will be complementary for the 'ALS1242.

The -1 versions of the SN74ALS' parts are identical to the standard versions except that the recommended maximum I_{OL} is increased to 24 milliamperes. There are no -1 versions of the SN54ALS' parts.

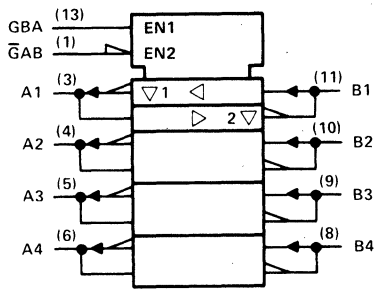
The SN54ALS1242 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS1242 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

$\overline{GAB}$	GBA	OPERATION
L	L	$\overline{A}$ to B
H	H	$\overline{B}$ to A
H	L	Isolation
L	H	Latch A and B ($A = \overline{B}$)

logic symbol†

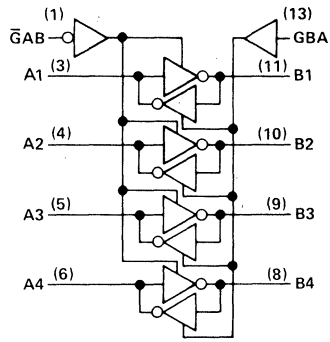
'ALS1242



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)

'ALS1242



Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS1242 . . . . . −55°C to 125°C
SN74ALS1242 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS1242			SN74ALS1242			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			8			16	mA
							24†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The 24-mA limit applies only to the −1 versions and only if V_{CC} is maintained between 4.75 V and 5.25 V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS1242			SN74ALS1242			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = −8 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 16 mA					0.35	0.5	
		V_{CC} = 4.75 V,	I_{OL} = 24 mA (−1 Versions)					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports§					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	A or B ports§					−0.1			−0.1	
I_O¶		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	Outputs high		8	14		8	12	mA
			Outputs low		10	17		10	15	
			Outputs disabled		9	16		9	14	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
¶The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS1242	SN54ALS1242		SN74ALS1242		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	6	2	14	2	12	ns
t_{PHL}			5	2	12	2	10	
t_{PZH}	$\overline{G}$AB	B	10	4	20	4	17	ns
t_{PZL}			13	5	23	5	21	
t_{PHZ}	$\overline{G}$AB	B	6	2	12	2	10	ns
t_{PLZ}			5	2	12	2	10	
t_{PZH}	GBA	A	12	5	23	5	20	ns
t_{PZL}			14	6	25	6	23	
t_{PHZ}	GBA	A	6	2	12	2	10	ns
t_{PLZ}			6	2	15	2	12	

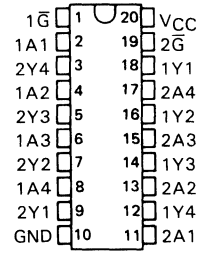
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

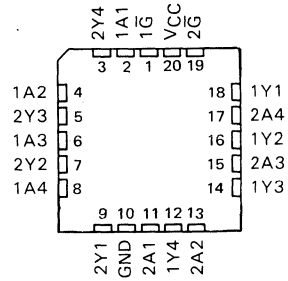
D2661, DECEMBER 1982–REVISED MAY 1986

- **Low-Power Version of 'ALS244A**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **P-N-P Inputs Reduce DC Loading**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS1244A . . . J PACKAGE
SN74ALS1244A . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS1244A . . . FK PACKAGE
(TOP VIEW)



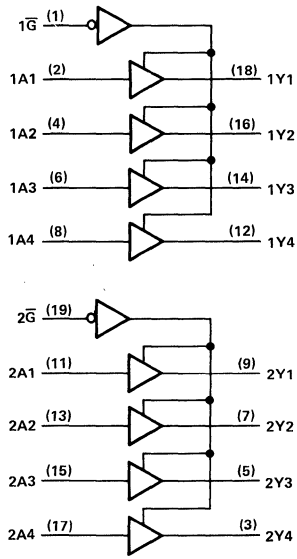
description

This octal buffer and line driver is designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'ALS1240 this device provides the choice of selected combinations of inverting and noninverting outputs symmetrical $\overline{G}$ (active-low input control) inputs, and complementary G and $\overline{G}$ inputs.

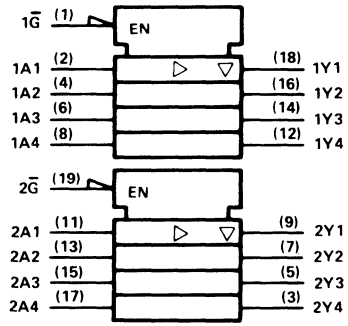
The -1 version of the SN74ALS1244A is identical to the standard version except that the recommended maximum I_{OL} is increased to 24 milliamperes. There is no -1 version of the SN54ALS1244A.

The SN54ALS1244A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS1244A is characterized for operation from 0°C to 70°C.

logic diagram (positive logic)



logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS1244A . . . . . −55°C to 125°C
SN74ALS1244A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS1244A			SN74ALS1244A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			8			16	mA
							24†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 24-mA limit applies for the SN74ALS1244A-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS1244A			SN74ALS1244A			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V, (I_{OL} = 24 mA for −1 versions)	I_{OL} = 16 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		6	15		6	11	mA
		Outputs low		10	20		10	17	
		Outputs disabled		11	25		11	20	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

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switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS1244A		SN74ALS1244A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	3	21	3	14	ns
t_{PHL}			3	16	3	14	
t_{PZH}	$\overline{G}$	Y	6	28	6	22	ns
t_{PZL}			6	26	6	22	
t_{PHZ}	$\overline{G}$	Y	2	15	2	10	ns
t_{PLZ}			3	25	3	13	

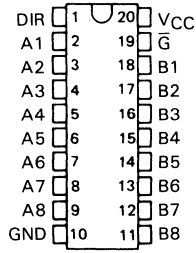
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

ALS and AS Circuits

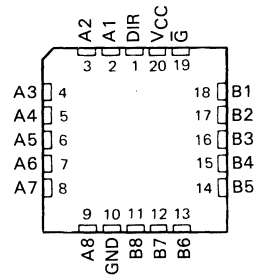
D2661, DECEMBER 1982 – REVISED MAY 1986

- 'Bidirectional Bus Transceivers in High-Density 20-Pin Packages
- Lower-Power Version of 'ALS245A
- 'ALS1245A is Identical to 'ALS1645A
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS1245A . . . J PACKAGE
SN74ALS1245A . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS1245A . . . FK PACKAGE
(TOP VIEW)



description

This octal bus transceiver is designed for asynchronous two-way communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input (G) can be used to disable the device so the buses are effectively isolated.

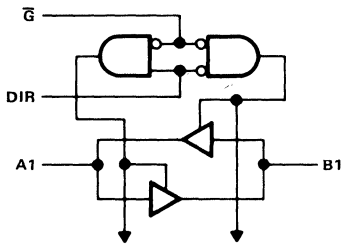
The -1 version of the SN74ALS1245A is identical to the standard versions except that the recommended maximum I_{OL} is increased to 24 milliamperes. There is no -1 version of the SN54ALS1245A.

The SN54ALS1245A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS1245A is characterized for operation from 0°C to 70°C.

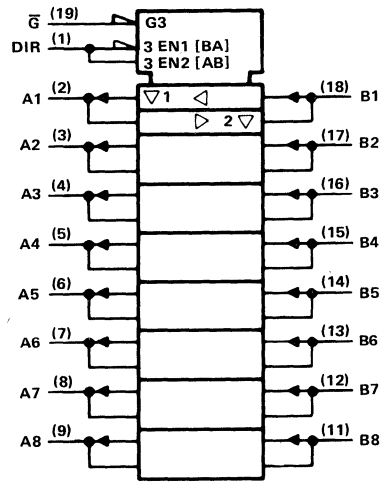
FUNCTION TABLE

CONTROL INPUTS		OPERATION
$\overline{G}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic diagram (positive logic)



logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS1245A . . . . . −55°C to 125°C
SN74ALS1245A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS1245A			SN74ALS1245A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			8			16	mA
							24†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limit applies only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 24-mA limit applies for the SN74ALS1245A-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS1245A			SN74ALS1245A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, (I_{OL} = 24 mA for −1 version)	I_{OL} = 16 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A, B ports§	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A, B ports§					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	A, B ports§					−0.1			−0.1	
I_O¶		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	Output high		21	33		21	30	mA
			Output low		23	36		23	33	
			Output disabled		25	40		25	36	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
¶The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

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switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS1245A		SN74ALS1245A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	2	19	2	13	ns
t_{PHL}			2	15	2	13	
t_{PZH}	$\overline{G}$	A or B	8	30	8	25	ns
t_{PZL}			8	29	8	25	
t_{PHZ}	$\overline{G}$	A or B	2	14	2	12	ns
t_{PLZ}			3	30	3	18	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2661, DECEMBER 1982—REVISED MAY 1986

- **Bidirectinal Bus Transceivers in High-Density 20-Pin Packages**
- **Lower-Power Versions of 'ALS640 Series**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so the buses are effectively isolated. The 'ALS1640A features inverting logic, while the 'ALS1645A features noninverting logic.

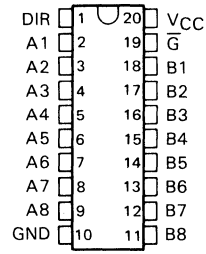
The -1 versions of the SN74ALS' parts are identical to the standard versions except that the recommended maximum I_{OL} is increased to 24 milliamperes. There are no -1 versions of the SN54ALS' parts.

The SN54ALS' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS' family is characterized for operation from 0°C to 70°C.

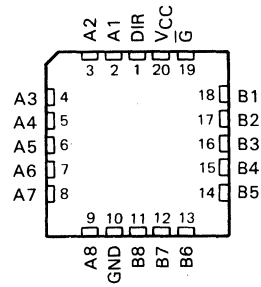
FUNCTION TABLE

CONTROL INPUTS		OPERATION	
$\overline{G}$	DIR	'ALS1640A	'ALS1645A
L	L	$\overline{B}$ data to A bus	B data to A Bus
L	H	$\overline{A}$ data to B bus	A data to Bus
H	X	Isolation	Isolation

SN54ALS' . . . J PACKAGE
SN74ALS' . . . DW OR N PACKAGE
(TOP VIEW)



SN54' . . . FK PACKAGE
(TOP VIEW)

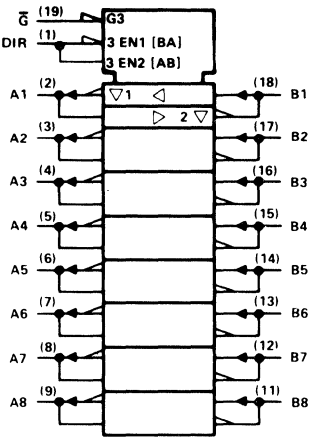


2

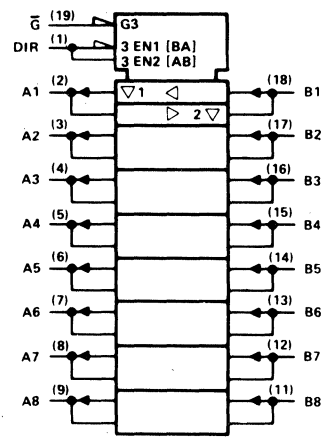
ALS and AS Circuits

logic symbols†

'ALS1640A



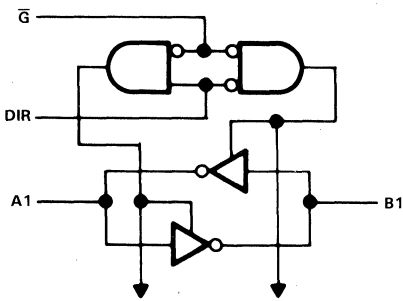
'ALS1645A



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

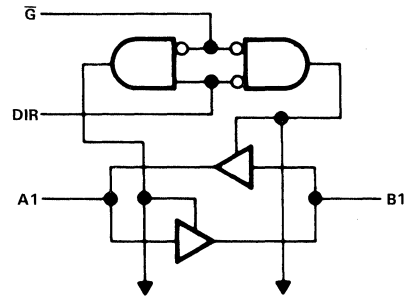
logic diagrams (positive logic)

'ALS1640A



TO SEVEN OTHER TRANSCEIVERS

'ALS1645A



TO SEVEN OTHER TRANSCEIVERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS1640A, SN54ALS1645A . . . . . −55°C to 125°C
SN74ALS1640A, SN74ALS1645A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS1640A SN54ALS1645A			SN74ALS1640A SN74ALS1645A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			8			16	mA
							24†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The 24-mA limit applies only to the −1 versions and only if V_{CC} is maintained between 4.75 V and 5.25 V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS1640A SN54ALS1645A			SN74ALS1640A SN74ALS1645A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 16 mA					0.35	0.5	
		V_{CC} = 4.75 V,	I_{OL} = 24 mA (−1 Versions)					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports§					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	A or B ports§					−0.1			−0.1	
I_O¶		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS1640A	V_{CC} = 5.5 V			18	35		18	32	mA
	'ALS1645A				25	40		25	36	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
¶The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS1640A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS1640A		SN74ALS1640A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	5	17	5	15	ns
t_{PHL}			2	13	2	10	
t_{PZH}	$\overline{G}$	A or B	5	23	5	20	ns
t_{PZL}			5	25	5	22	
t_{PHZ}	$\overline{G}$	A or B	2	12	2	10	ns
t_{PLZ}			5	16	5	13	

'ALS1645A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS1645A		SN74ALS1645A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	2	15	2	13	ns
t_{PHL}			2	15	2	13	
t_{PZH}	$\overline{G}$	A or B	8	28	8	25	ns
t_{PZL}			8	28	8	25	
t_{PHZ}	$\overline{G}$	A or B	2	14	2	12	ns
t_{PLZ}			3	22	3	18	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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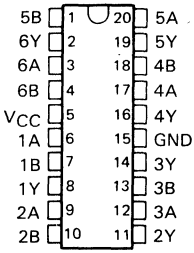
- **High Capacitive Drive Capability**
- **'ALS1804A Has Typical Delay Time of 4 ns (C_L = 50 pF) and Typical Power Dissipation of 3.4 mW per Gate**
- **'AS1804 Has Typical Delay Time of 2.6 ns (C_L = 50 pF) and Typical Power Dissipation of Less than 9 mW per Gate**
- **Center V_{CC} and GND Configuration Provides Minimum Lead Inductance in High Current Switching Applications**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS1804A, SN54AS1804 . . . J PACKAGE
SN74ALS1804A, SN74AS1804 . . . DW OR N PACKAGE
(TOP VIEW)



Use 'ALS804A or 'AS804B for chip carrier option.

description

These devices contain six independent 2-input NAND drivers. They perform the Boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

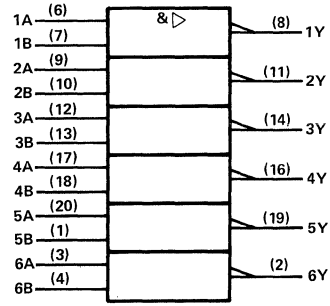
The center pin configuration used in the 'ALS1804A and 'AS1804 provides a reduction of lead inductance when compared to the 'ALS804A and 'AS804B. This reduction of lead inductance will minimize noise generated onto either the V_{CC} or GND bus. This reduction is significant in high current switching applications.

The SN54ALS1804A and SN54AS1804 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS1804A and SN74AS1804 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each driver)

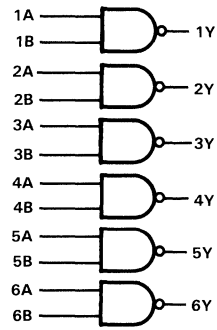
INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS1804A . . . . . −55°C to 125°C
SN74ALS1804A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS1804A			SN74ALS1804A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS1804A			SN74ALS1804A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} −12 mA	2						
	V_{CC} = 4.5 V,	I_{OH} −15 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.9	2.5		0.9	2.5	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		7	12		7	12	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS1804A	SN54ALS1804A		SN74ALS1804A		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	4	2	9	2	7	ns
t_{PHL}			4	2	9	2	8	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS1804 . . . . . −55°C to 125°C
SN74AS1804 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS1804			SN74AS1804			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−40			−48	mA
I_{OL}	Low-level output current			40			48	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS1804			SN74AS1804			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −40 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −48 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 40 mA		0.25	0.5				V
	V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−50		−200	−50		−200	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		3.5	5		3.5	5	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		16	27		16	27	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

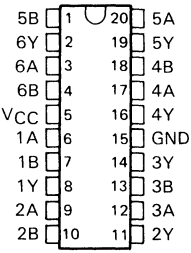
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS1804		SN74AS1804		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1	5	1	4	ns
t_{PHL}			1	5	1	4	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

AUGUST 1984—REVISED MAY 1986

- **High Capacitive Drive Capability**
- **'ALS1805A Has Typical Delay Time of 4.2 ns (C_L = 50 pF) and Typical Power Dissipation of 4.2 mW per Gate**
- **'AS1805 Has Typical Delay Time of 2.6 ns (C_L = 50 pF) and Typical Power Dissipation of Less than 12 mW per Gate**
- **Center V_{CC} and GND Configuration Provides Minimum Lead Inductance in High Current Switching Applications**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS1805A, SN54AS1805 . . . J PACKAGE
SN74ALS1805A, SN74AS1805 . . . N PACKAGE
(TOP VIEW)



Use 'ALS805A or 'AS805B for chip carrier option.

description

These devices contain six independent 2-input NOR drivers. They perform the Boolean functions $Y = \overline{A+B}$ or $Y = \overline{A} \cdot \overline{B}$ in positive logic.

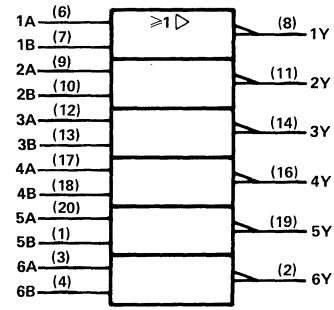
The center pin configuration used in the 'ALS1805A and 'AS1805 provides a reduction of lead inductance when compared to the 'ALS805A and 'AS805B. This reduction of lead inductance will minimize noise generated onto either the V_{CC} or GND bus. This reduction is significant in high current switching applications.

The SN54ALS1805A and SN54AS1805 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS1805A and SN74AS1805 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each driver)

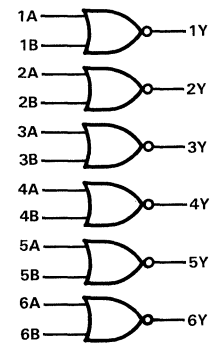
INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS1805A . . . . . −55°C to 125°C
SN74ALS1805A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS1805A			SN74ALS1805A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS1805A			SN74ALS1805A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		2	4		2	4	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		8	14		8	14	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX			UNIT
			'ALS1805A	SN54ALS1805A		SN74ALS1805A	
			TYP	MIN	MAX	MIN	MAX
t_{PLH}	A or B	Y	4	2	9	2	7	ns
t_{PHL}			5	2	10	2	8	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS1805 . . . . . −55°C to 125°C
SN74AS1805 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS1805			SN74AS1805			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−40			−48	mA
I_{OL}	Low-level output current			40			48	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS1805			SN74AS1805			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −40 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −48 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 40 mA		0.25	0.5				V
	V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−50		−200	−50		−200	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		6.5	10		6.5	10	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		20	32		20	32	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS1805		SN74AS1805		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1	4.8	1	4.3	ns
t_{PHL}			1	4.8	1	4.3	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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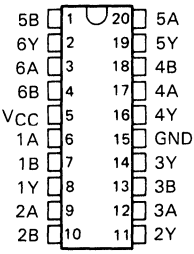
- **High Capacitive Drive Capability**
- **'ALS1808A Has Typical Delay Time of 4.8 ns (C_L = 50 pF) and Typical Power Dissipation of 4.5 mW per Gate**
- **'AS1808 Has Typical Delay Time of 3.2 ns (C_L = 50 pF) and Typical Power Dissipation of Less than 13 mW per Gate**
- **Center V_{CC} and GND Configuration Provides Minimum Lead Inductance in High Current Switching Applications**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS1808A, SN54AS1808 . . . J PACKAGE
SN74ALS1808A, SN74AS1805 . . . N PACKAGE
(TOP VIEW)



Use 'ALS808A or 'AS808B for chip carrier option.

description

These devices contain six independent 2-input AND drivers. They perform the Boolean functions $Y = A \cdot B$ or $Y = \overline{\overline{A}+\overline{B}}$ in positive logic.

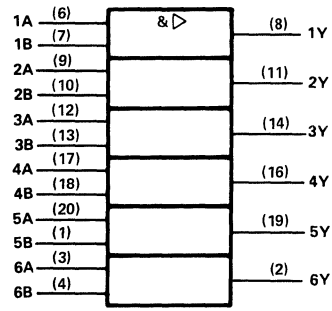
The center pin configuration used in the 'ALS1808A and 'AS1808 provides a reduction of lead inductance when compared to the 'ALS808A and 'AS808B. This reduction of lead inductance will minimize noise generated onto either the V_{CC} or GND bus. This reduction is significant in high current switching applications.

The SN54ALS1808A and SN54AS1808 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS1808A and SN74AS1808 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each driver)

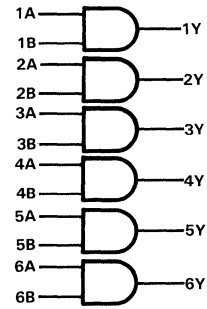
INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS1808A . . . . . −55°C to 125°C
SN74ALS1808A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS1808A			SN74ALS1808A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS1808A			SN74ALS1808A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		4.5	7		4.5	7	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		8	16		8	16	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS1808A	SN54ALS1808A		SN74ALS1808A		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	6	2	11	2	9	ns
t_{PHL}			4	1	10	1	8	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS1808 . . . . . −55°C to 125°C
SN74AS1808 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS1808			SN74AS1808			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−40			−48	mA
I_{OL}	Low-level output current			40			48	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS1808			SN74AS1808			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −40 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −48 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 40 mA		0.25	0.5				V
	V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−50		−200	−50		−200	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		8	13		8	13	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		20	33		20	33	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS1808		SN74AS1808		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1	6.5	1	6	ns
t_{PHL}			1	6.5	1	6	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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- **High Capacitive Drive Capability**
- **'ALS1832A Has Typical Delay Time of 5 ns (C_L = 50 pF) and Typical Power Dissipation of 5.3 mW per Gate**
- **'AS1832 Has Typical Delay Time of 3.9 ns (C_L = 50 pF) and Typical Power Dissipation of Less than 17 mW per Gate**
- **Center V_{CC} and GND Configuration Provides Minimum Lead Inductance in High Current Switching Applications**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These devices contain six independent 2-input OR drivers. They perform the Boolean functions $Y = A+B$ or $Y = \overline{\overline{A} \cdot \overline{B}}$ in positive logic.

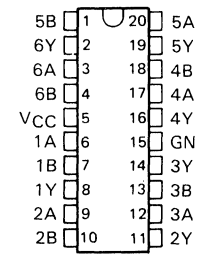
The center pin configuration used in the 'ALS1832A and 'AS1832 provides a reduction of lead inductance when compared to the 'ALS832A and 'AS832B. This reduction of lead inductance will minimize noise generated onto either the V_{CC} or GND bus. This reduction is significant in high current switching applications.

The SN54ALS1832A and SN54AS1832 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS1832A and SN74AS1832 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each driver)

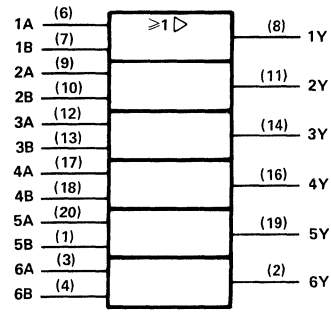
INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

SN54ALS1832A, SN54AS1832 . . . J PACKAGE
SN74ALS1832A, SN74AS1832 . . . N PACKAGE
(TOP VIEW)



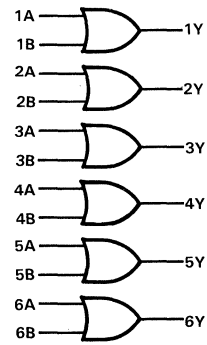
Use 'ALS832A or 'AS832B for chip carrier option.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS1832A . . . . . −55°C to 125°C
SN74ALS1832A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS1832A			SN74ALS1832A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS1832A			SN74ALS1832A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		6	9		6	9	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		9.5	16		9.5	16	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS1832A	SN54ALS1832A		SN74ALS1832A		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	6	2	11	2	9	ns
t_{PHL}			4	1	10	1	8	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS1832 . . . . . −55°C to 125°C
SN74AS1832 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS1832			SN74AS1832			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−40			−48	mA
I_{OL}	Low-level output current			40			48	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS1832			SN74AS1832			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −40 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −48 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 40 mA		0.25	0.5				V
	V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−50		−200	−50		−200	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		11	17		11	17	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		22	36		22	36	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

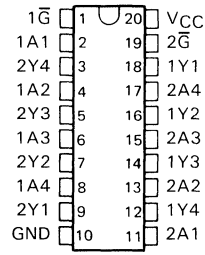
switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS1832		SN74AS1832		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1	7	1	6.3	ns
t_{PHL}			1	7	1	6.3	

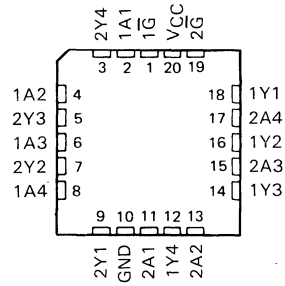
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

- **Bidirectional Quadruple Bus Transceivers for Driving MOS Devices**
- **I/O Ports have 25 Ohm Series Resistors so No External Resistors are Required**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS2240 . . . J PACKAGE
SN74ALS2240 . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS2240 . . . FK PACKAGE
(TOP VIEW)

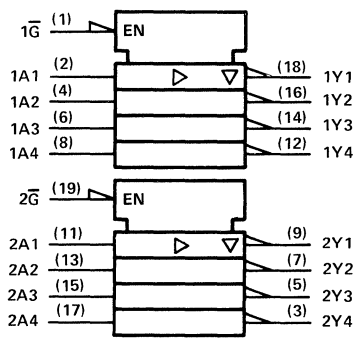


description

These octal buffers and line drivers are designed to drive the capacitive inputs of MOS devices and to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. These devices feature high fan-out and improved fan-in.

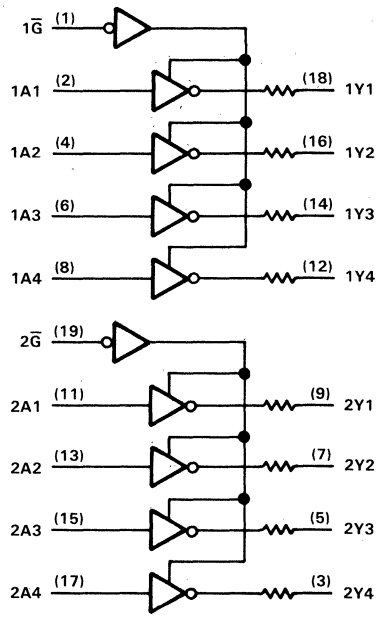
The SN54ALS2240 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS2240 is characterized for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS2240 . . . . . −55°C to 125°C
SN74ALS2240 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS2240			SN74ALS2240			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
T_A	Operating free-air temperature	−55		125	0		70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS2240			SN74ALS2240			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 1 mA		0.15	0.5		0.15	0.5	V
	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.35	0.8		0.35	0.8	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{OH}	V_{CC} = 4.5 V,	V_O = 2 V	−15			−15			mA
I_{OL}	V_{CC} = 4.5 V,	V_O = 2 V	15			15			mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		6	11		6	11	mA
		Outputs low		13	23		13	23	
		Outputs disabled		12	20		12	20	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS2240	SN54ALS2240		SN74ALS2240		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	6	2	14	2	10	ns
t_{PHL}			6	2	14	2	10	
t_{PZH}	$\overline{G}$	Y	10	5	20	5	17	ns
t_{PZL}			12	7	25	7	20	
t_{PHZ}	$\overline{G}$	Y	7	2	12	2	10	ns
t_{PLZ}			9	4	20	4	15	

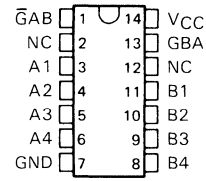
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

2 ALS and AS Circuits

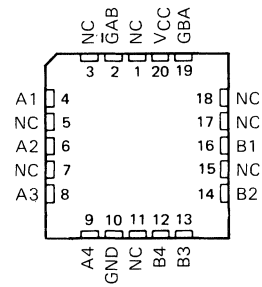
MAY 1985—REVISED MAY 1986

- **Bidirectional Quadruple Bus Transceivers For Driving MOS Devices**
- **I/O Ports Have 25 Ohm Series Resistors so No External Resistors are Required**
- **Package Options Include Plastic "Small Outline" Packages, Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS2242 . . . J PACKAGE
SN74ALS2242 . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS2242 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

These quadruple bus transceivers are designed to drive the capacitive input characteristics of MOS devices and allow asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

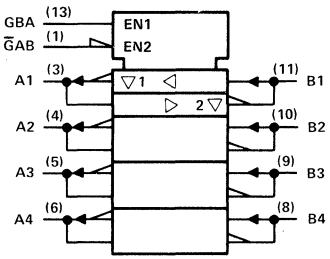
These devices allow data transmission from A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the the enable inputs (GBA and $\overline{G}AB$).

The enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives the 'ALS2242 the capability to store data by simultaneous enabling of GBA and $\overline{G}AB$. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states. The 8-bit codes appearing on the two sets of buses will be complementary.

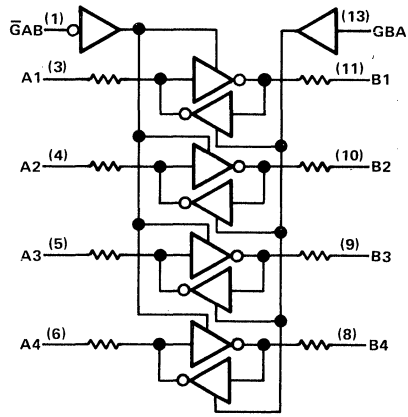
The SN54ALS2242 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS2242 is characterized for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagrams (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS2242 . . . . . −55°C to 125°C
SN74ALS2242 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS2242			SN74ALS2242			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
T_A	Operating free-air temperature	−55		125	0		70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS2242			SN74ALS2242			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} −2			V_{CC} −2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 1 mA		0.15	0.5		0.15	0.5	V
		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.35	0.8		0.35	0.8	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports‡					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	A or B ports‡					−0.1			−0.1	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{OH}		V_{CC} = 4.5 V,	V_O = 2 V	−15			−15			mA
I_{OL}		V_{CC} = 4.5 V,	V_O = 2 V	30			30			mA
I_{CC}		V_{CC} = 5.5 V	Outputs high		10	20		10	16	mA
			Outputs low		14	26		14	21	
			Outputs disabled		13	24		13	19	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_1 = 500 Ω, R_2 = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_1 = 500 Ω, R_2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS2242	SN54ALS2242		SN74ALS2242		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	5	2	15	2	11	ns
t_{PHL}			5	2	14	2	10	
t_{PZH}	$\overline{G}AB$	B	8	3	18	3	16	ns
t_{PZL}			11	5	22	5	20	
t_{PHZ}	$\overline{G}AB$	B	6	2	12	2	10	ns
t_{PLZ}			6	2	18	2	12	
t_{PZH}	GBA	A	10	3	18	3	16	ns
t_{PZL}			12	5	22	5	20	
t_{PHZ}	GBA	A	6	2	12	2	10	ns
t_{PLZ}			6	2	18	2	14	

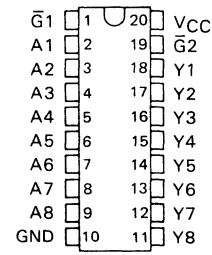
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54ALS2540, SN54ALS2541, SN74ALS2540, SN74ALS2541
OCTAL LINE DRIVERS/MOS DRIVERS WITH 3-STATE OUTPUTS

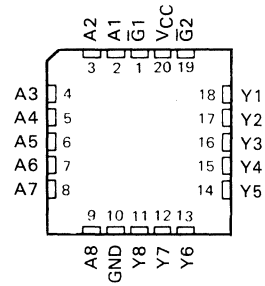
JUNE 1984—REVISED MAY 1986

- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **P-N-P Inputs Reduce D-C Loading**
- **Outputs have 25 Ω Series Resistor, No External Resistors are Required**
- **Package Options Include Plastic "Small Outline" Packages, Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS2540, SN54ALS2541 . . . J PACKAGE
SN74ALS2540, SN74ALS2541 . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS2540, SN54ALS2541 . . . FK PACKAGE
(TOP VIEW)



description

These octal buffers and line drivers are designed to drive capacitive input characteristics of MOS devices and have the performance of the popular SN54ALS240A/SN74ALS240A series. At the same time, they offer a pinout with inputs and outputs on opposite sides of the package. This arrangement greatly enhances printed circuit board layout.

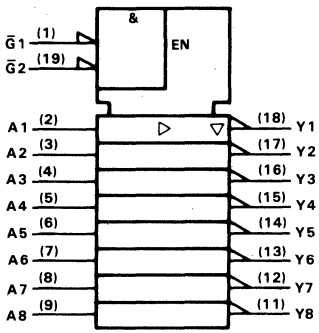
The three-state control gate is a 2-input NOR such that if either $\overline{G}1$ or $\overline{G}2$ is high, all eight outputs are in the high-impedance state.

The 'ALS2540 offers inverting data and the 'ALS2541 offers true data at the outputs.

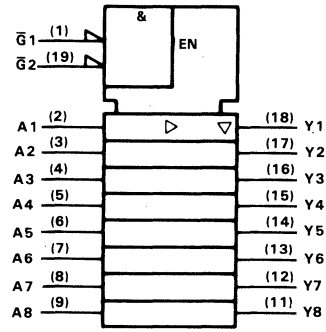
The SN54ALS' is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS' is characterized for operation from 0°C to 70°C.

logic symbols†

'ALS2540



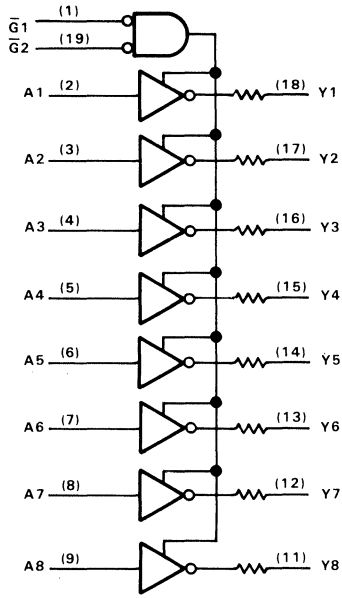
'ALS2541



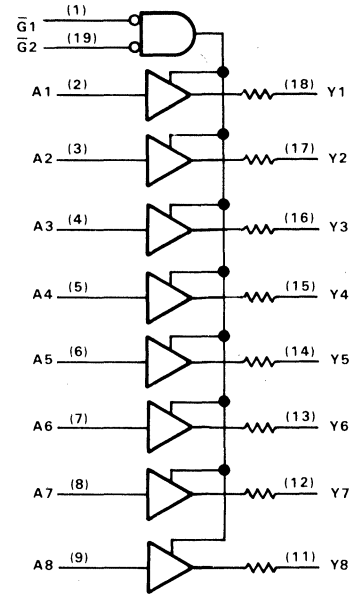
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)

'ALS2540



'ALS2541



All output resistors are 25 Ω.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS2540, SN54ALS2541 . . . . . −55°C to 125°C
SN74ALS2540, SN74ALS2541 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS2540 SN54ALS2541			SN74ALS2540 SN74ALS2541			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			12			12	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS2540 SN54ALS2541			SN74ALS2540 SN74ALS2541			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 1 mA		0.15	0.5		0.15	0.5	V
		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.35	0.8		0.35	0.8	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_{OH}		V_{CC} = 4.5 V,	V_O = 2 V	−15			−15			mA
I_{OL}		V_{CC} = 4.5 V,	V_O = 2 V	30			30			mA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
I_{CC}	'ALS2540	V_{CC} = 5.5 V	Outputs high		5	10		5	10	mA
			Outputs low		13	22		13	22	
			Outputs disabled		11	19		11	19	
	'ALS2541	V_{CC} = 5.5 V	Outputs high		6	14		6	14	mA
			Outputs low		15	25		15	25	
			Outputs disabled		13.5	22		13.5	22	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS2540 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS2540	SN54ALS2540		SN74ALS2540		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	7.5	2	14	2	12	ns
t_{PHL}			5.6	2	13	2	11	
t_{PZH}	$\overline{G}$	Y	9	5	18	5	15	ns
t_{PZL}			12.6	8	24	8	20	
t_{PHZ}	$\overline{G}$	Y	4	1	12	1	10	ns
t_{PLZ}			7	2	14	2	12	

'ALS2541 switching characteristics (see Note 1)

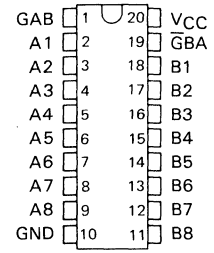
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS2541	SN54ALS2541		SN74ALS2541		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	8.7	2	17	2	15	ns
t_{PHL}			7	2	14	2	12	
t_{PZH}	$\overline{G}$	Y	9	5	18	5	15	ns
t_{PZL}			12.6	8	24	8	20	
t_{PHZ}	$\overline{G}$	Y	4	1	12	1	10	ns
t_{PLZ}			7	2	14	2	12	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

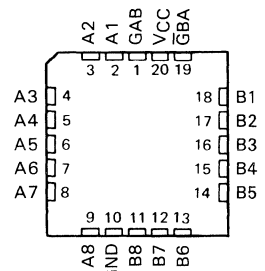
DECEMBER 1983 – REVISED MAY 1986

- **Bidirectional Octal Bus Transceivers For Driving MOS Devices**
- **I/O Ports Have 25 Ohm Series Resistors So No External Resistors Are Required**
- **Local Bus-Latch Capability**
- **Choice of True or Inverting Logic**
- **Package Options Include Plastic "Small Outline" Packages, Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54AS' . . . J PACKAGE
SN74AS' . . . DW OR N PACKAGE
(TOP VIEW)



SN54AS' . . . FK PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed to drive the capacitive input characteristics of MOS devices and allow asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs ($\overline{G}$BA and GAB).

The enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives the 'AS2620 or 'AS2623 the capability to store data by simultaneous enabling of $\overline{G}$BA and GAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states. The 8-bit codes appearing on the two sets of buses will be identical for the 'AS2623 or complementary for the 'AS2620.

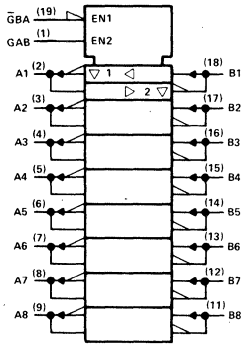
The SN54AS2620 and SN54AS2623 are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74AS2620 and SN74AS2623 are characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE

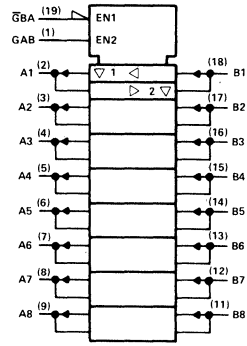
ENABLE INPUTS		OPERATION	
$\overline{G}$BA	GAB	'AS2620	'AS2623
L	L	$\overline{B}$ data to A bus	B data to A bus
H	H	$\overline{A}$ data to B bus	A data to B bus
H	L	Isolation	Isolation
L	H	$\overline{B}$ data to A bus, $\overline{A}$ data to B bus	B data to A bus, A data to B bus

logic symbols†

'AS2620



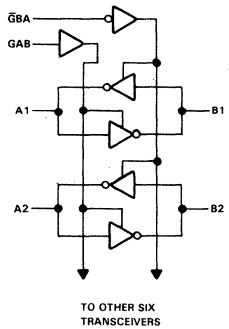
'AS2623



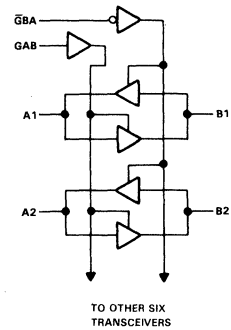
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)

'AS2620



'AS2623



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54AS2620, SN54AS2623 . . . . . −55°C to 125°C
SN74AS2620, SN74AS2623 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS2620 SN54AS2623			SN74AS2620 SN74AS2623			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS2620 SN54AS2623			SN74AS2620 SN74AS2623			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 1 mA		0.15	0.4		0.15	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.35	0.7		0.35	0.7	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports‡					70			70	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	A or B ports‡					−0.75			−0.75	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−50		−150	−50		−150	mA
I_{OH}		V_{CC} = 4.5 V,	V_O = 2 V	−35			−35			mA
I_{OL}		V_{CC} = 4.5 V,	V_O = 2 V	35			35			mA
I_{CC}	'AS2620	V_{CC} = 5.5 V	Outputs high		62	100		62	100	mA
			Outputs low		74	121		74	121	
			Outputs disabled		48	77		48	77	
	'AS2623	V_{CC} = 5.5 V	Outputs high		57	93		57	93	
			Outputs low		116	189		116	189	
			Outputs disabled		72	116		72	116	

†All typical values are at V_{CC} = 5 V, T_A = 25°C
‡For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'AS2620 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS2620		SN74AS2620		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	1	9.5	1	8	ns
t_{PHL}			1	7.5	1	6.5	
t_{PLH}	B	A	1	9.5	1	8	ns
t_{PHL}			1	7.5	1	6.5	
t_{PZH}	$\overline{G}$BA	A	1	11	1	10	ns
t_{PZL}			1	12	1	11	
t_{PHZ}	$\overline{G}$BA	A	1	7.5	1	6	ns
t_{PLZ}			1	15	1	12	
t_{PZH}	GAB	B	1	9	1	8	ns
t_{PZL}			1	9	1	8	
t_{PHZ}	GAB	B	1	12	1	11	ns
t_{PLZ}			1	12	1	11	

'AS2623 switching characteristics (see Note 1)

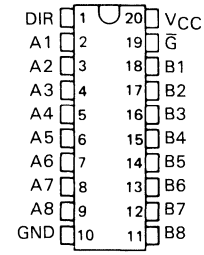
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS2623		SN74AS2623		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	1	9.5	1	8.5	ns
t_{PHL}			1	8.5	1	7.5	
t_{PLH}	B	A	1	10	1	9	ns
t_{PHL}			1	9	1	7.5	
t_{PZH}	$\overline{G}$BA	A	1	12.5	1	11	ns
t_{PZL}			1	12	1	11	
t_{PHZ}	$\overline{G}$BA	A	1	8.5	1	7.5	ns
t_{PLZ}			1	13	1	12	
t_{PZH}	GAB	B	1	13	1	12	ns
t_{PZL}			1	13.5	1	12	
t_{PHZ}	GAB	B	1	7.5	1	7	ns
t_{PLZ}			1	14.5	1	12.5	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

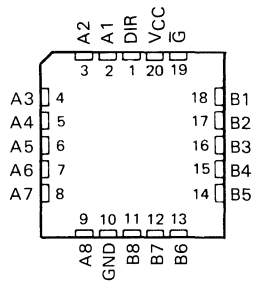
DECEMBER 1983—REVISED MAY 1986

- **Bidirectional Octal Bus Transceivers For Driving MOS Devices**
- **I/O Ports Have 25 Ohm Series Resistors So No External Resistors Are Required**
- **Choice of True or Inverting Logic**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54AS' . . . J PACKAGE
SN74AS' . . . DW or N PACKAGE
(TOP VIEW)



SN54AS' . . . FK PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed to drive the capacitive input characteristics of MOS devices and allow asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so the buses are effectively isolated.

The SN54AS' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS' family is characterized for operation from 0°C to 70°C.

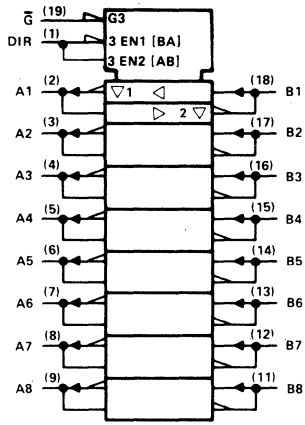
FUNCTION TABLE

CONTROL INPUTS		OPERATION	
$\overline{G}$	DIR	'AS2640	'AS2645
L	L	$\overline{B}$ data to A bus	B data to A bus
L	H	$\overline{A}$ data to B bus	A data to B bus
H	X	Isolation	Isolation

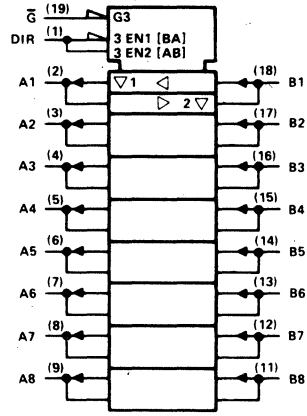
2 ALS and AS Circuits

logic symbols†

'AS2640



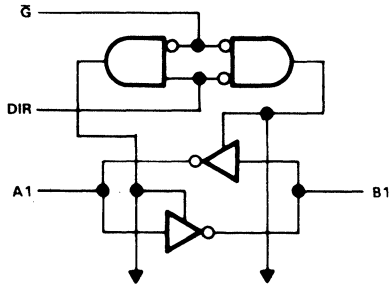
'AS2645



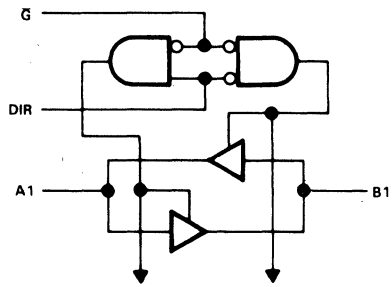
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagrams (positive logic)

'AS2640



'AS2645



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54AS2640, SN54AS2645 . . . . . −55°C to 125°C
SN74AS2640, SN74AS2645 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS2640 SN54AS2645			SN74AS2640 SN74AS2645			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-lvel input voltage			0.8			0.8	V
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS'			SN74AS'			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 1 mA		0.15	0.4		0.15	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.35	0.7		0.35	0.7	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports‡					70			70	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	A or B ports‡					−0.75			−0.75	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−50		−150	−50		−150	mA
I_{OH}		V_{CC} = 4.5 V,	V_O = 2 V	−35			−35			mA
I_{OL}		V_{CC} = 4.5 V,	V_{OL} = 2 V	35			35			mA
I_{CC}	'AS2640	V_{CC} = 5.5 V	Outputs high		37	58		37	58	mA
			Outputs low		78	123		78	123	
			Outputs disabled		51	80		51	80	
	'AS2645		Outputs high		58	95		58	95	
			Outputs low		95	155		95	155	
			Outputs disabled		73	119		73	119	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡For I/O ports, the parametes I_{IH} and I_{IL} include the off-state output current.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'AS2640 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS2640		SN74AS2640		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1	9.5	1	7.5	ns
t_{PHL}			1	7	1	6.5	
t_{PZH}	$\overline{G}$	A or B	2	11	2	9	ns
t_{PZL}			2	12	2	10	
t_{PHZ}	$\overline{G}$	A or B	1	8	1	7	ns
t_{PLZ}			2	15	2	13	

'AS2645 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS2645		SN74AS2645		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1	12	1	10	ns
t_{PHL}			1	11	1	9.5	
t_{PZH}	$\overline{G}$	A or B	1	13	1	11.5	ns
t_{PZL}			1	13	1	10.5	
t_{PHZ}	$\overline{G}$	A or B	1	9	1	8	ns
t_{PLZ}			1	13	1	12	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
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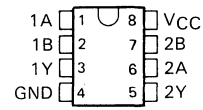
D2746, JULY 1983—REVISED MAY 1986

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs.**
- **Dependable Texas Instruments Quality and Reliability.**

SN54ALS8003 . . . JG PACKAGE
SN74ALS8003 . . . D OR P PACKAGE
(TOP VIEW)



description

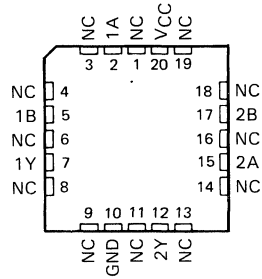
These devices contain two independent 2-input NAND gates. They perform the Boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The SN54ALS8003 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS8003 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

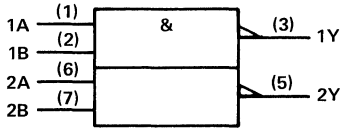
INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

SN54ALS8003 . . . FK PACKAGE
(TOP VIEW)



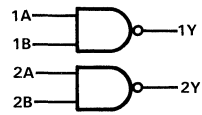
NC—No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, JG and P packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS8003 . . . . . −55°C to 125°C
SN74ALS8003 . . . . . 0°C to 70°C
Storage temperature . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS8003			SN74ALS8003			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS8003			SN74ALS8003			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.22	0.43		0.22	0.43	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		0.81	1.5		0.81	1.5	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximats one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS8003		SN74ALS8003		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	3	14	3	11	ns
t_{PHL}			2	10	2	8	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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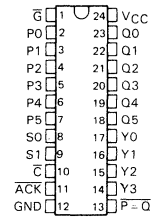
- **'ALS29806 is a 6-Bit Identity Comparator Controlling a 2- to 4-Bit Decoder**
- **'ALS29809 is a 9-Bit Identity Comparator**
- **Low Power Dissipation . . . 50 mW Typical**
- **'ALS29806 and 'ALS29809 are Functionally Equivalent to AM29806 and AM29809**
- **Internal Pull-Up Resistor on Q Inputs**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

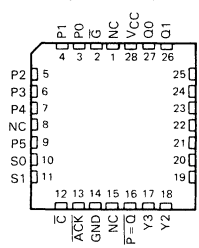
The 'ALS29806 and 'ALS29809 are 6-bit and 9-bit comparators, respectively. The 'ALS29806 and 'ALS29809 compare two data words applied to the P and Q inputs. When the two words are identical, the $\overline{P=Q}$ output goes low. Both devices feature an open-collector acknowledge ($\overline{ACK}$) output that goes low when $\overline{P=Q}$ and the controlling input ($\overline{C}$) are low. The 'ALS29806 features a 2- to 4-bit decoder whose selected output goes low when the $\overline{P=Q}$ output is low. The 'ALS29806 and 'ALS29809 can be cascaded by tying the $\overline{P=Q}$ output to the enable $\overline{G}$ of the next device. If the $\overline{G}$ input is high, all the outputs will be inactive (high).

The SN54ALS29806 and SN54ALS29809 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS29806 and SN74ALS29809 are characterized for operation from 0°C to 70°C.

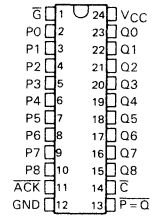
SN54ALS29806 . . . JT PACKAGE
SN74ALS29806 . . . DW OR NT PACKAGE
(TOP VIEW)



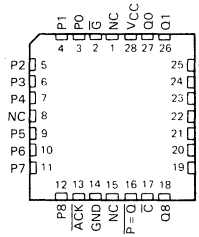
SN54ALS29806 . . . FK PACKAGE
SN74ALS29806 . . . FN PACKAGE
(TOP VIEW)



SN54ALS29809 . . . JT PACKAGE
SN74ALS29809 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54ALS29809 . . . FK PACKAGE
SN74ALS29809 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

FUNCTION TABLE
FOR $\overline{P=Q}$ AND $\overline{ACK}$ OUTPUTS

INPUTS			OUTPUTS	
$\overline{G}$	P,Q	$\overline{C}$	$\overline{P=Q}$	$\overline{ACK}$
H	X	X	H	H
X	P≠Q	X	H	H
L	P=Q	L	L	L
L	P=Q	H	L	H

FUNCTION TABLE
FOR DECODER OUTPUTS

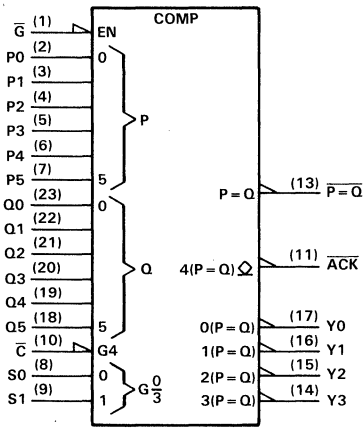
INPUTS				OUTPUTS			
$\overline{G}$	P,Q	S1	S0	Y3	Y2	Y1	Y0
H	X	X	X	H	H	H	H
X	P≠Q	X	X	H	H	H	H
L	P=Q	L	L	H	H	H	L
L	P=Q	L	H	H	H	L	H
L	P=Q	H	L	H	L	H	H
L	P=Q	H	H	L	H	H	H

2

ALS and AS Circuits

logic symbol†

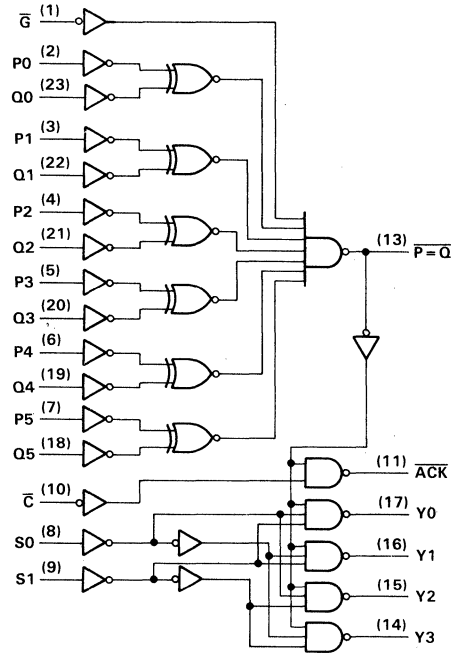
'ALS29806



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT and NT packages.

logic diagram (positive logic)

'ALS29806



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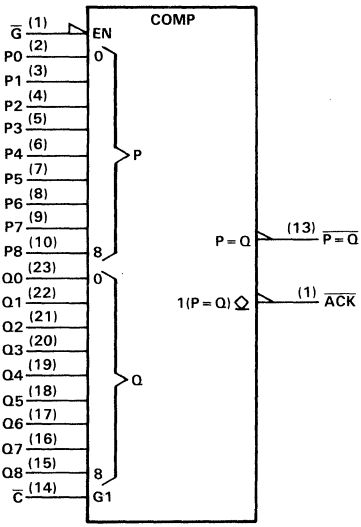
FUNCTION TABLE

INPUTS			OUTPUTS	
$\overline{G}$	P,Q	$\overline{C}$	$\overline{P=Q}$	$\overline{ACK}$
H	X	X	H	H
X	P≠Q	X	H	H
L	P=Q	L	L	L
L	P=Q	H	L	H

logic symbol†

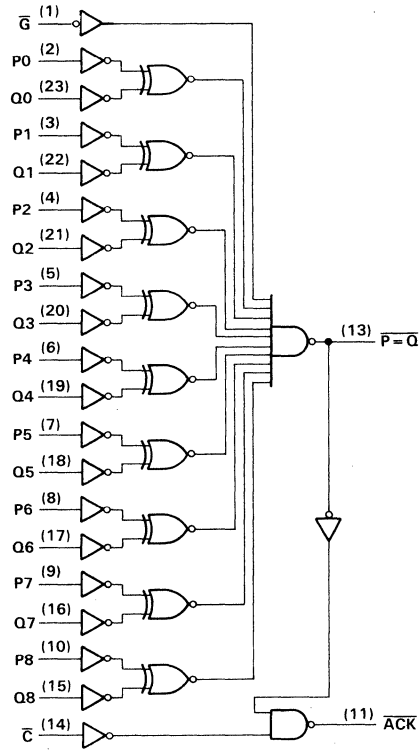
'ALS29809



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT and NT packages.

logic diagram (positive logic)

'ALS29809



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, V_I . . . . . 5.5 V
Operating free-air temperature range: SN54' . . . . . −55°C to 125°C
SN74' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS29806 SN54ALS29809			SN74ALS29806 SN74ALS29809			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
V_{OH}	High-level output voltage	$\overline{ACK}$			5.5			5.5	V
I_{OH}	High-level output current	$\overline{P=Q}$, Y			−3			−3	mA
I_{OL}	Low-level output current	$\overline{ACK}$			32			32	mA
		$\overline{P=Q}$, Y			12			24	
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS29806 SN54ALS29809			SN74ALS29806 SN74ALS29809			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2.2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
I_{OH}	$\overline{ACK}$	V_{CC} = 5.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	$\overline{P=Q}$, Y	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.32	0.5	
	$\overline{ACK}$	V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.34	0.5		0.34	0.5	
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	mA
I_{IH}	Q‡	V_{CC} = 5.5 V,	V_I = 2.4 V			−250			−250	μA
	All other					20			20	
I_{IL}	Q‡	V_{CC} = 5.5 V,	V_I = 0.5 V			−2			−1	mA
	All other					−0.6			−0.6	
I_{OS}§		V_{CC} = 5.5 V,	V_O = 0 V	−60		−150	−60		−150	mA
I_{CC}	'ALS29806	V_{CC} = 5.5 V,	See Note 1		14	22		14	22	mA
	'ALS29809				10	20		10	20	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ All Q inputs have internal pull-up resistors of 27 kΩ nominal.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 1: I_{CC} is measured with $\overline{G}$ grounded and P and Q at 4.5 V.

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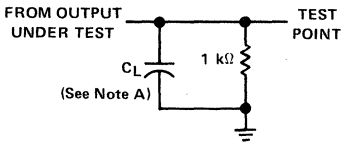
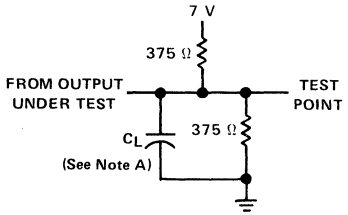
switching characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = (see Figure 1), T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = (see Figure 1), T_A = MIN to MAX				UNIT
			'ALS29806 'ALS29809			SN54ALS29806 SN54ALS29809		SN74ALS29806 SN74ALS29809		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	P or Q	$\overline{P=Q}$		8	11	3	15	3	13	ns
t_{PHL}				7	10	2	13	2	11	
t_{PLH}	P or Q	Y		9	11	3	17	3	13	ns
t_{PHL}				9	12	5	17	5	14	
t_{PLH}	$\overline{G}$	$\overline{P=Q}$		9	12	3	15	3	14	ns
t_{PHL}				7	10	2	14	2	12	
t_{PLH}	$\overline{G}$	Y		8	11	3	17	3	15	ns
t_{PHL}				10	13	5	19	5	16	
t_{PLH}	S0 or S1	Y		6	10	2	15	2	13	ns
t_{PHL}				8	11	2	15	2	13	
t_{PLH}	P or Q	$\overline{ACK}$		11	14	5	22	5	17	ns
t_{PHL}				10	13	4	18	4	16	
t_{PLH}	$\overline{G}$	$\overline{ACK}$		10	14	5	22	5	17	ns
t_{PHL}				10	14	4	19	4	17	
t_{PLH}	$\overline{C}$	$\overline{ACK}$		8	11	3	21	3	18	ns
t_{PHL}				7	11	3	17	3	15	

PARAMETER MEASUREMENT INFORMATION

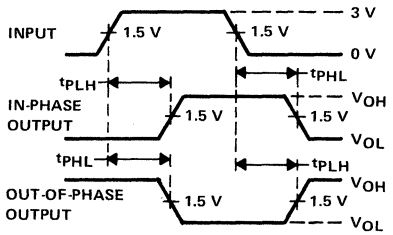


LOAD CIRCUIT FOR
$\overline{P=Q}$ AND Y OUTPUTS



LOAD CIRCUIT FOR
$\overline{ACK}$ OUTPUT

NOTE A: C_L includes probe and jig capacitance.



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

FIGURE 1

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TYPICAL APPLICATION

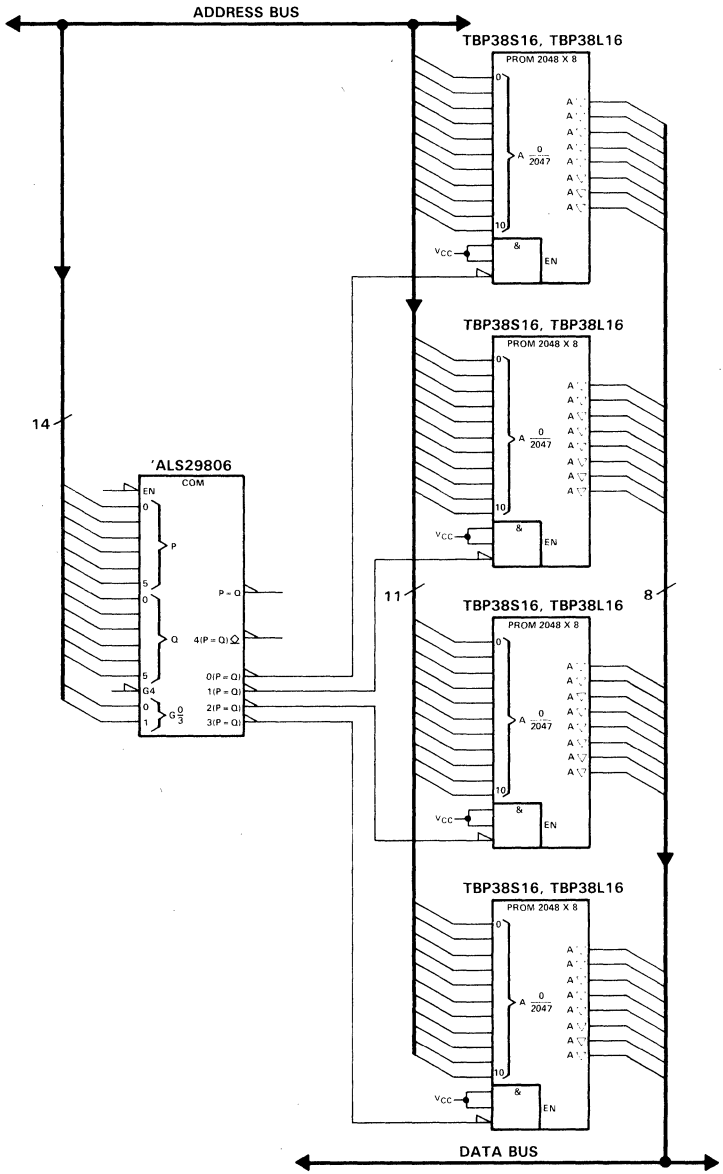


FIGURE 2. MEMORY BANK DECODER

SN54ALS29821, SN54ALS29822
SN74ALS29821, SN74ALS29822
10-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

D2825, JANUARY 1986

- **Functionally Equivalent to AMD's AM29821 and AM29822**
- **Provides Extra Data Width Necessary for Wider Address/Data Paths or Buses with Parity**
- **Outputs Have Undershoot Protection Circuitry**
- **Power-Up High-Impedance State**
- **Package Options Include Both Plastic and Ceramic Carriers in Addition to Plastic and Ceramic DIPs**
- **Buffered Control Inputs to Reduce DC Loading Effects**
- **Dependable Texas Instruments Quality and Reliability**

description

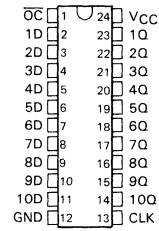
These 10-bit flip-flops feature three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

The ten flip-flops are edge-triggered D-type flip-flops. On the positive transition of the clock the Q outputs on the 'ALS29821 will be true, and on the 'ALS29822 will be complementary to the data input.

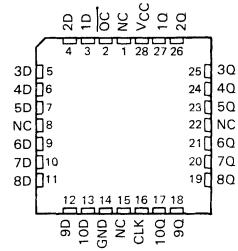
A buffered output-control ($\overline{OC}$)input can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54'family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

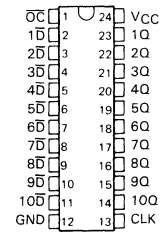
SN54ALS29821 . . . JT PACKAGE
SN74ALS29821 . . . DW OR NT PACKAGE
(TOP VIEW)



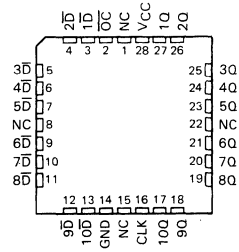
SN54ALS29821 . . . FK PACKAGE
SN74ALS29821 . . . FN PACKAGE
(TOP VIEW)



SN54ALS29822 . . . JT PACKAGE
SN74ALS29822 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54ALS29822 . . . FK PACKAGE
SN74ALS29822 . . . FN PACKAGE
(TOP VIEW)

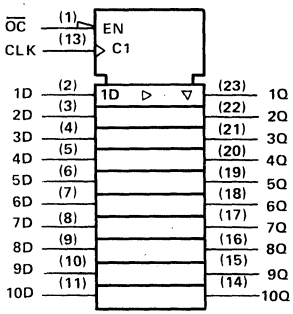


NC—No internal connection

'ALS29821 FUNCTION TABLE (EACH FLIP-FLOP)

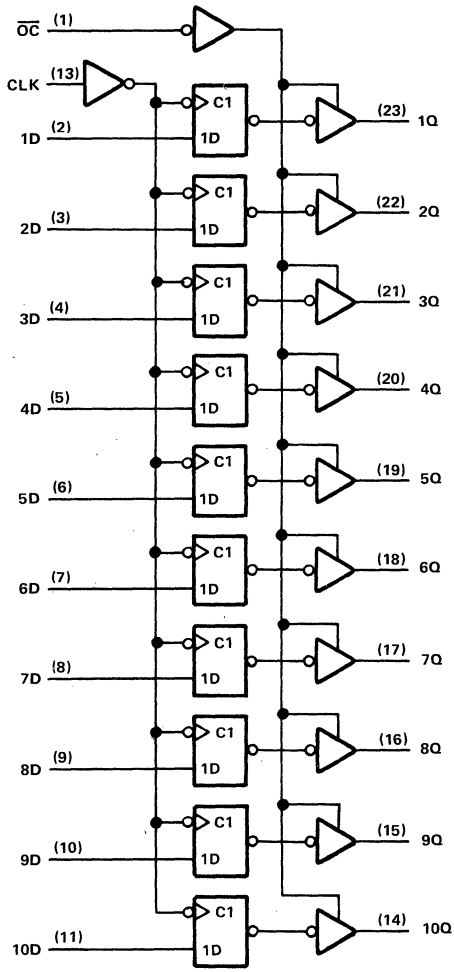
INPUTS			OUTPUT
$\overline{OC}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

'ALS29821 logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

'ALS29821 logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

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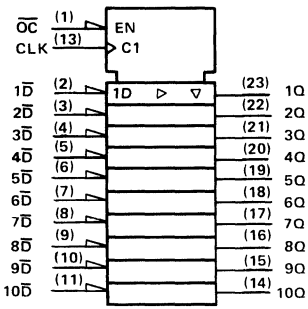
'ALS29822 FUNCTION TABLE (EACH FLIP-FLOP)

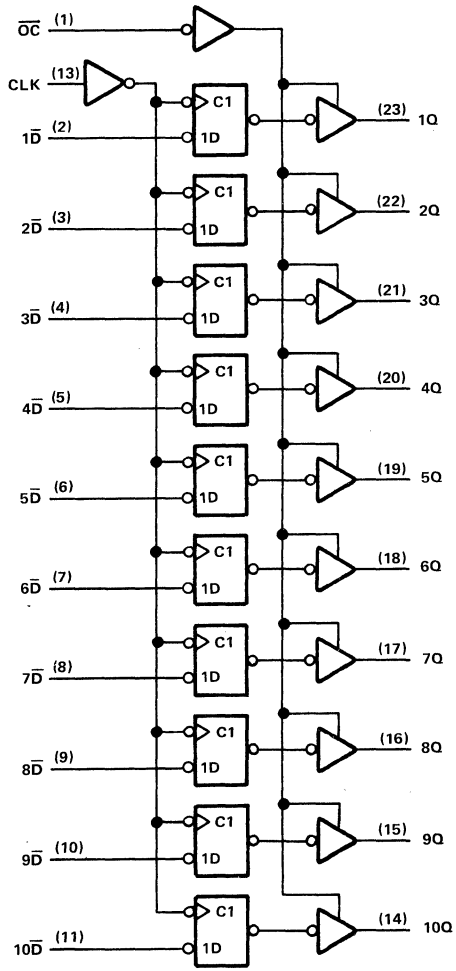
INPUTS			OUTPUT
$\overline{OC}$	CLK	$\overline{D}$	Q
L	↑	H	L
L	↑	L	H
L	L	X	Q_0
H	X	X	Z

'ALS29822 logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

'ALS29822 logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 5.5 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Input current . . . . . 100 mA
Output current . . . . . −30 mA to 5 mA
Operating free-air temperature range: SN54ALS29821, SN54ALS29822 . . . . . −55°C to 125°C
SN74ALS29821, SN74ALS29822 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS29821 SN54ALS29822			SN74ALS29821 SN74ALS29822			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−15			−24	mA
I_{OL}	Low-level output currrent			32			48	mA
t_w	Pulse duration, CLK high or low							ns
t_{su}	Setup time, data before CLK↑							ns
t_h	Hold time, data after CLK↑							ns
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54ALS29821 SN54ALS29822			SN74ALS29821 SN74ALS29822			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = MIN to MAX,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = MIN,	I_{OH} = −15 mA	2.4	3.3					
		V_{CC} = MIN,	I_{OH} = −24 mA				2.4	3.2		
V_{OL}		V_{CC} = MIN,	I_{OL} = 32 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = MIN,	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}		V_{CC} = MAX,	V_O = 2.4 V			20			20	μA
I_{OZL}		V_{CC} = MAX,	V_O = 0.4 V			−20			−20	μA
I_I		V_{CC} = MAX,	V_I = 5.5 V			0.1			0.1	mA
I_{IH}		V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = MAX,	V_I = 0.4 V			−0.1			−0.1	mA
I_{OS}§		V_{CC} = MAX,	V_O = 0 V	−75		−250	−75		−250	mA
I_{CC}	'ALS29821	V_{CC} = MAX	Outputs high							mA
			Outputs low							
			Outputs disabled		48			48		
	'ALS29822		Outputs high							
			Outputs low							
			Outputs disabled		48			48		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Additional information on these products can be obtained from the factory as it becomes available.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

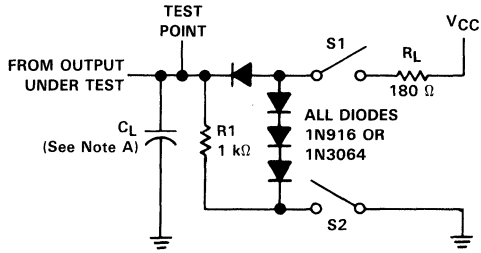
switching characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS See Figure 1	V_{CC} = 5 V, T_A = 25°C 'ALS29821 'ALS29822			V_{CC} = MIN TO MAX,† T_A = MIN TO MAX† SN54ALS29821 SN54ALS29822		SN74ALS29821 SN74ALS29822		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	CLK	Any Q	C_L = 300 pF								ns
t_{PHL}											
t_{PLH}			C_L = 50 pF		6						
t_{PHL}					7						
t_{PZH}	$\overline{OC}$	Any Q	C_L = 300 pF								ns
t_{PZL}											
t_{PZH}			C_L = 50 pF		12						
t_{PZL}					11						
t_{PHZ}	$\overline{OC}$	Any Q	C_L = 50 pF								ns
t_{PLZ}											
t_{PHZ}			C_L = 5 pF		5						
t_{PLZ}					6						

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

Additional information on these products can be obtained from the factory as it becomes available.

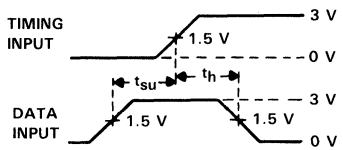
PARAMETER MEASUREMENT INFORMATION



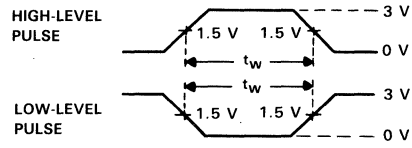
LOAD CIRCUIT

SWITCH POSITION TABLE

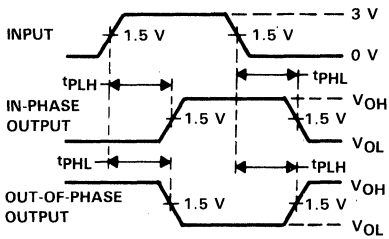
TEST	S1	S2
t_{PLH}	Closed	Closed
t_{PHL}	Closed	Closed
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed



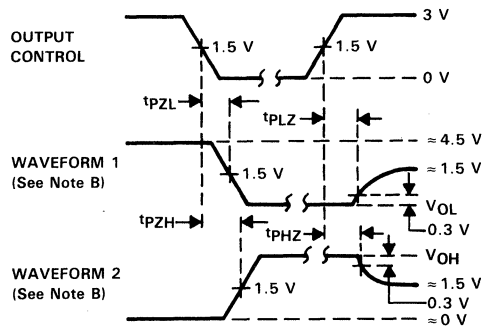
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

FIGURE 1

SN54AS29821, SN54AS29822, SN74AS29821, SN74AS29822
10-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

D2825, MAY 1986

- **Designed to be Interchangeable with AMD AM29821 and AM29822**
- **Ideal for Data Synchronization of Wider Data Paths**
- **Provide Extra Data Width Necessary for Wider Address/Data Paths or Buses with Parity**
- **Outputs Have Undershoot Production Circuitry**
- **Power-Up High Impedance State**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Buffered Control Inputs to Reduce DC Loading Effects**
- **Dependable Texas Instruments Quality and Reliability**

description

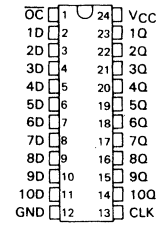
These 10-bit flip-flops feature three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

The ten flip-flops are edge-triggered D-type flip-flops. On the positive transition of the clock the Q outputs on the 'AS29821 will be true, and on the 'AS29822 will be complementary, to the data input.

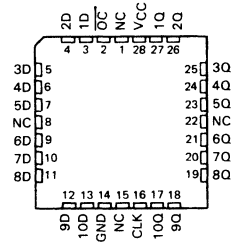
A buffered output control input can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control ($\overline{OC}$) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

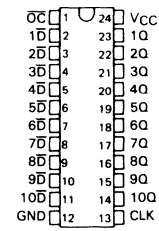
SN54AS29821 . . . JT PACKAGE
SN74AS29821 . . . DW OR NT PACKAGE
(TOP VIEW)



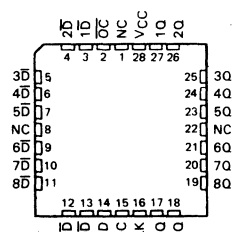
SN54AS29821 . . . FK PACKAGE
SN74AS29821 . . . FN PACKAGE
(TOP VIEW)



SN54AS29822 . . . JT PACKAGE
SN74AS29822 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54AS29822 . . . FK PACKAGE
SN74AS29822 . . . FN PACKAGE
(TOP VIEW)



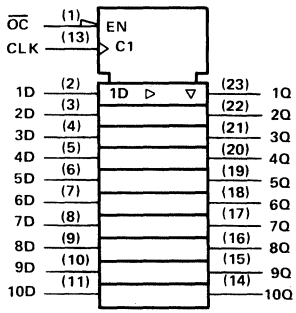
NC—No internal connection

The SN54AS29821 and SN54AS29822 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS29821 and SN74AS29822 are characterized for operation from 0°C to 70°C.

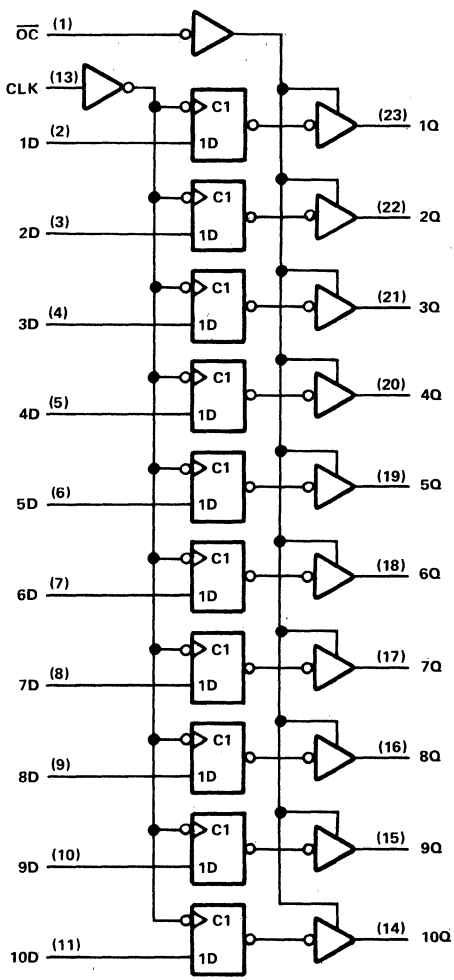
'AS29821 FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS			OUTPUT
$\overline{OC}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_O
H	X	X	Z

'AS29821 logic symbol†



'AS29821 logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

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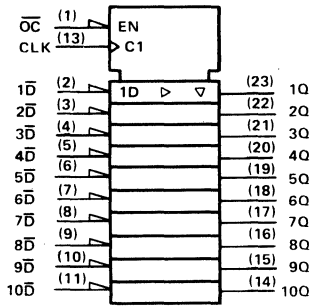
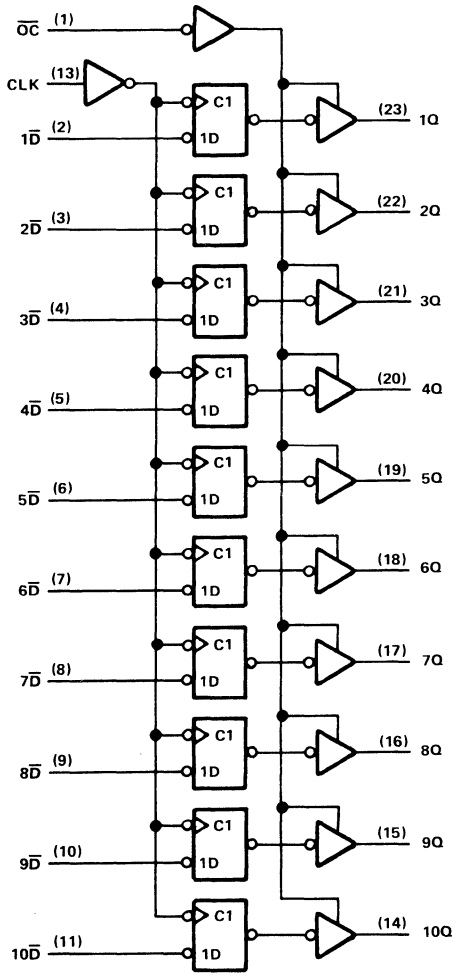
'AS29822 FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS			OUTPUT
$\overline{OC}$	CLK	$\overline{D}$	Q
L	↑	H	L
L	↑	L	H
L	L	X	Q_0
H	X	X	Z

'AS29822 logic symbol†



'AS29822 logic diagram (positive logic)



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

SN54ALS29823, SN54ALS29824
SN74ALS29823, SN74ALS29824
9-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

D2825, JANUARY 1986

- **Functionally Equivalent to AMD's AM29823 and AM29824**
- **Provides Extra Data Width Necessary for Wider Address/Data Paths or Buses with Parity**
- **Outputs Have Undershoot Protection Circuitry**
- **Power-Up High-Impedance State**
- **Buffered Control Inputs to Reduce DC Loading Effects**
- **Package Options Include both Plastic and Ceramic Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

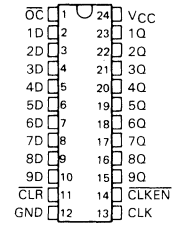
description

These 9-bit flip-flops feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers, parity bus interfacing and working registers.

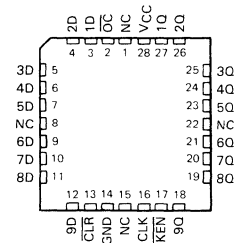
With the clock enable ($\overline{CLKEN}$) low, the nine D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock. Taking $\overline{CLKEN}$ high will disable the clock buffer, thus latching the outputs. The 'ALS29823 has noninverting D inputs and the 'ALS29824 has inverting D inputs. Taking the $\overline{CLR}$ input low causes the nine Q outputs to go low independently of the clock.

A buffered output-control input ($\overline{OC}$)can be used to place the nine outputs in either normal logic state (high or low level) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

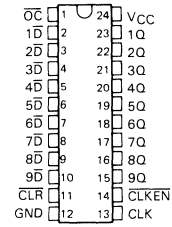
SN54ALS29823 . . . JT PACKAGE
SN74ALS29823 . . . DW OR NT PACKAGE
(TOP VIEW)



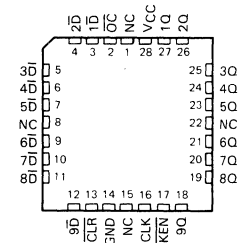
SN54ALS29823 . . . FK PACKAGE
SN74ALS29823 . . . FN PACKAGE
(TOP VIEW)



SN54ALS29824 . . . JT PACKAGE
SN74ALS29824 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54ALS29824 . . . FK PACKAGE
SN74ALS29824 . . . FN PACKAGE
(TOP VIEW)

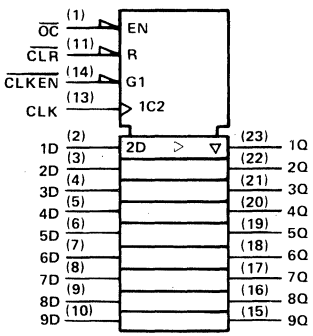


The SN54AS' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS' family is characterized for operation from 0°C to 70°C.

'ALS29823 FUNCTION TABLE

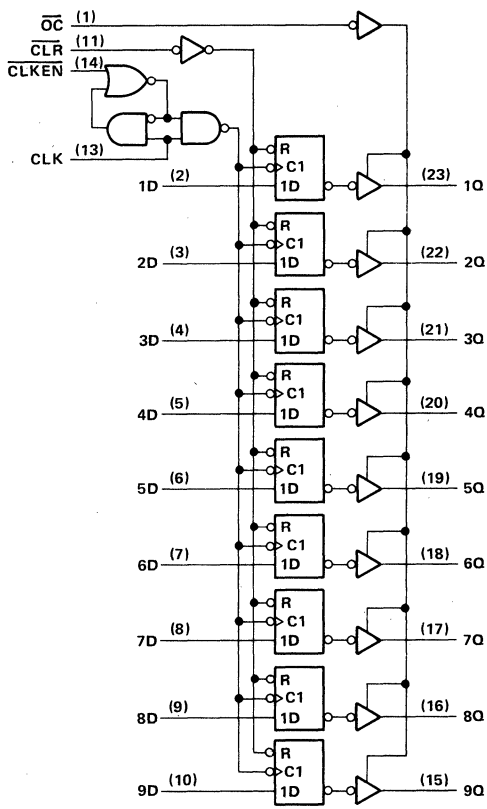
INPUTS					OUTPUT
$\overline{OC}$	$\overline{CLR}$	$\overline{CLKEN}$	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	H	X	X	Q_0
H	X	X	X	X	Z

'ALS29823 logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12

'ALS29823 logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

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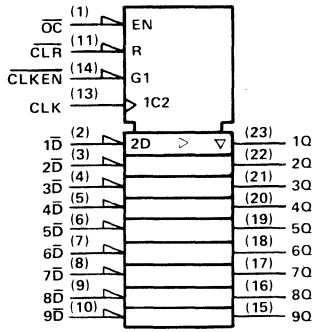
'ALS29824 FUNCTION TABLE

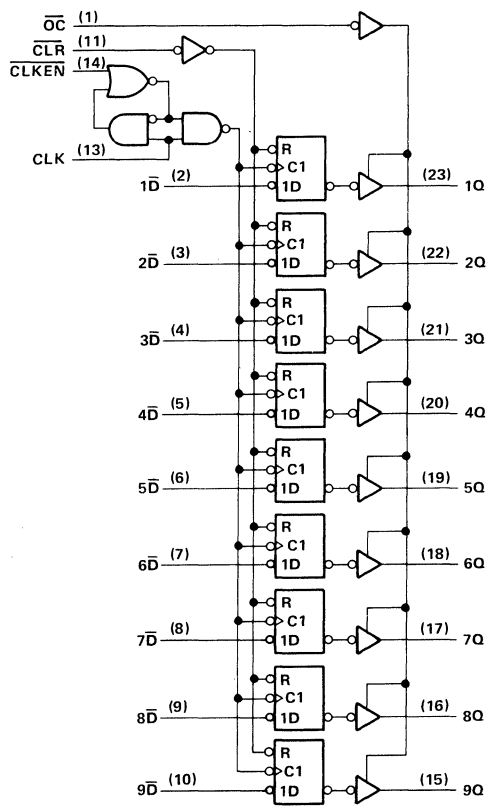
INPUTS					OUTPUT
$\overline{OC}$	$\overline{CLR}$	$\overline{CLKEN}$	CLK	$\overline{D}$	Q
L	L	X	X	X	L
L	H	L	↑	H	L
L	H	L	↑	L	H
L	H	H	X	X	Q_0
H	X	X	X	X	Z

'ALS29824 logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

'ALS29824 logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 5.5 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Input current . . . . . 100 mA
Output current . . . . . −30 mA to 5 mA
Operating free-air temperature range: SN54ALS29823, SN54ALS29824 . . . . . −55°C to 125°C
SN74ALS29823, SN74ALS29824 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS29823 SN54ALS29824			SN74ALS29823 SN74ALS29824			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−15			−24	mA
I_{OL}	Low-level output current				32			48	mA
t_w	Pulse duration	$\overline{CLR}$ low							ns
		CLK high or low							
t_{su}	Setup time before CLK↑	$\overline{CLR}$ inactive							ns
		Data							
		$\overline{CLKEN}$ high or low							
t_h	Hold time, $\overline{CLKEN}$ or data after CLK↑								ns
T_A	Operating free-air temperature		−55		125	0		70	°C

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POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54ALS29823 SN54ALS29824			SN74ALS29823 SN74ALS29824			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = MIN to MAX,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = MIN,	I_{OH} = −15 mA	2.4	3.3					
		V_{CC} = MIN,	I_{OH} = −24 mA				2.4	3.2		
V_{OL}		V_{CC} = MIN,	I_{OL} = 32 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = MIN,	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}		V_{CC} = MAX,	V_O = 2.4 V			20			20	μA
I_{OZL}		V_{CC} = MAX,	V_O = 0.4 V			−20			−20	μA
I_I		V_{CC} = MAX,	V_I = 5.5 V			0.1			0.1	mA
I_{IH}		V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = MAX,	V_I = 0.4 V			−0.1			−0.1	mA
I_{OS}§		V_{CC} = MAX,	V_O = 0 V	−75		−250	−75		−250	mA
I_{CC}	'ALS29823	V_{CC} = MAX	Outputs high							mA
			Outputs low							
			Outputs disabled		48			48		
	'ALS29824		Outputs high							
			Outputs low							
			Outputs disabled		48			48		

† For conditions shown as MIN or MAX, use appropriate value specificed under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Additional Information on these products can be obtained from the factory as it becomes available.

switching characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS See Figure 1	V_{CC} = 5 V, T_A = 25°C 'ALS29823 'ALS29824			V_{CC} = MIN TO MAX,† T_A = MIN TO MAX† SN54ALS29823 SN54ALS29824		SN74ALS29823 SN74ALS29824		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	CLK	Any Q	C_L = 300 pF								ns
t_{PHL}											
t_{PLH}			C_L = 50 pF		5.5						
t_{PHL}					6.5						
t_{PHL}	$\overline{CLR}$	Any Q	C_L = 50 pF		13						ns
t_{PZH}	$\overline{OC}$	Any Q	C_L = 300 pF								ns
t_{PZL}											
t_{PZH}			C_L = 50 pF		12						
t_{PZL}					11						
t_{PHZ}	$\overline{OC}$	Any Q	C_L = 50 pF								ns
t_{PLZ}											
t_{PHZ}			C_L = 5 pF		5						
t_{PLZ}					5.5						

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

Additional information on these products can be obtained from the factory as it becomes available.

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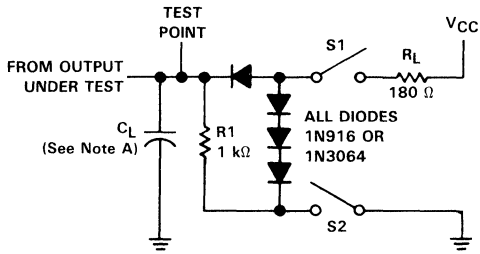
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

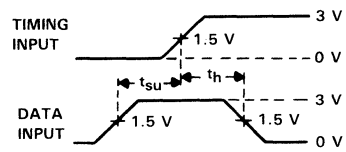
PARAMETER MEASUREMENT INFORMATION



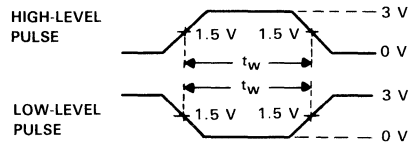
LOAD CIRCUIT

SWITCH POSITION TABLE

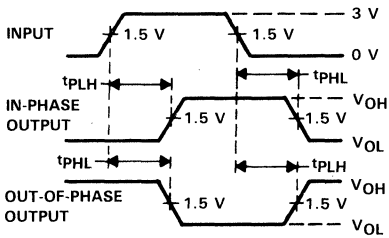
TEST	S1	S2
t_{PLH}	Closed	Closed
t_{PHL}	Closed	Closed
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed



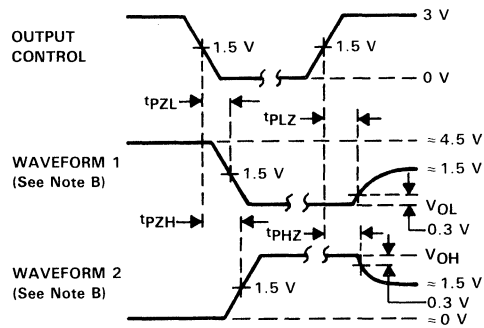
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

FIGURE 1

SN54AS29823, SN54AS29824, SN74AS29823, SN74AS29824
9-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

D2910, MAY 1986

- **Designed to be Interchangeable with AMD AM29823 and AM29824**
- **Ideal for Data Synchronization of Wider Data Paths**
- **Provides Extra Data Width Necessary for Wider Address/Data Paths or Buses with Parity**
- **Outputs Have Undershoot Protection Circuitry**
- **Power-Up High-Impedance State**
- **Buffered Control Inputs to Reduce DC Loading Effects**
- **Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

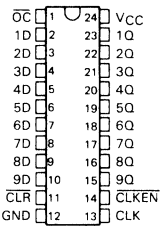
description

These 9-bit flip-flops feature three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers, parity bus interfacing and working registers.

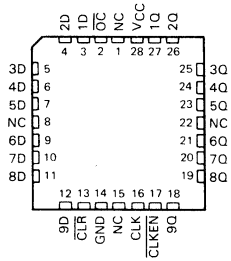
With the clock enable ($\overline{CLKEN}$) low, the nine D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock. Taking $\overline{CLKEN}$ high will disable the clock buffer, thus latching the outputs. The 'AS29823 has noninverting D inputs and the 'AS29824 has inverting $\overline{D}$ inputs. Taking the $\overline{CLR}$ input low causes the nine Q outputs to go low independently of the clock.

The buffered output-control input ($\overline{OC}$) can be used to place the nine outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

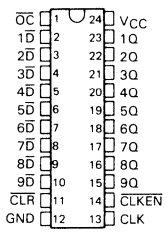
SN54AS29823 . . . JT PACKAGE
SN74AS29823 . . . DW or NT PACKAGE
(TOP VIEW)



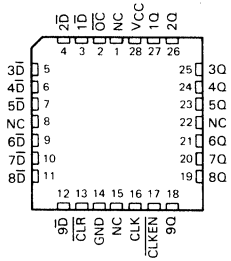
SN54AS29823 . . . FK PACKAGE
SN74AS29823 . . . FN PACKAGE
(TOP VIEW)



SN54AS29824 . . . JT PACKAGE
SN74AS29824 . . . DW or NT PACKAGE
(TOP VIEW)



SN54AS29824 . . . FK PACKAGE
SN74AS29824 . . . FN PACKAGE
(TOP VIEW)



NC - No internal connection

The SN54AS29823 and SN54AS29824 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS29823 and SN74AS29824 are characterized for operation from 0°C to 70°C.

FUNCTION TABLES

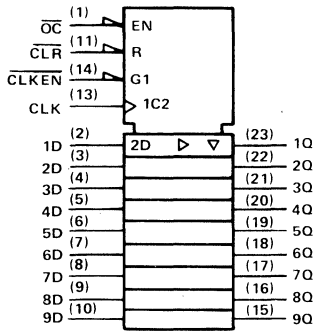
'AS29823

INPUTS					OUTPUT
$\overline{OC}$	$\overline{CLR}$	$\overline{CLKEN}$	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	H	X	X	Q_0
H	X	X	X	X	Z

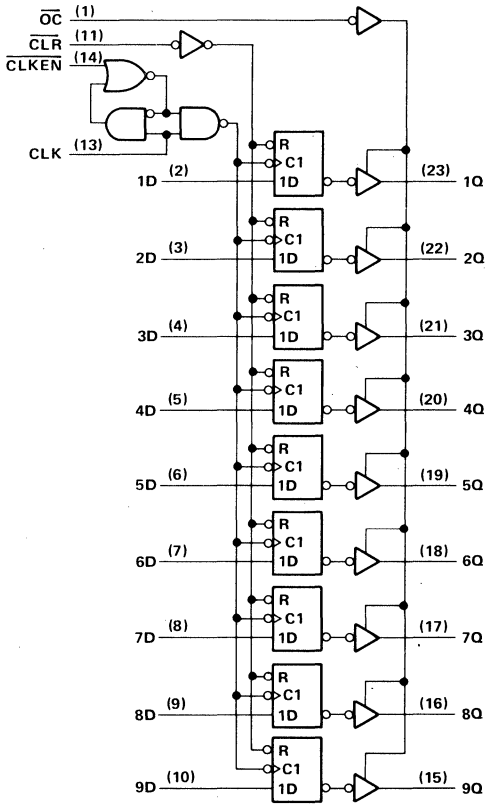
'AS24824

INPUTS					OUTPUT
$\overline{OC}$	$\overline{CLR}$	$\overline{CLKEN}$	CLK	$\overline{D}$	Q
L	L	X	X	X	L
L	H	L	↑	H	L
L	H	L	↑	L	H
L	H	H	X	X	Q_0
H	X	X	X	X	Z

'AS29823 logic symbol†



'AS29823 logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

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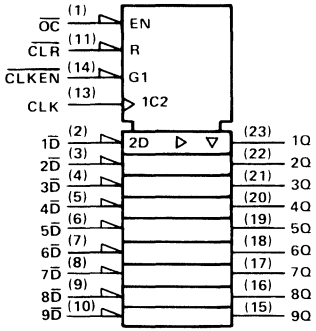
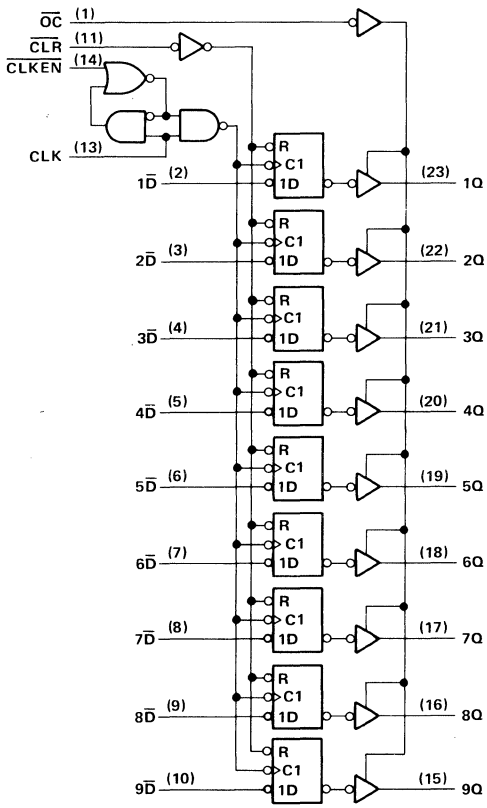
'AS29824 logic symbol†



'AS29824 logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, and NT packages.

SN54ALS29825, SN54ALS29826
SN74ALS29825, SN74ALS29826
8-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

D2829, JANUARY 1986

- **Functionally Equivalent to AMD's AM29825 and AM29826**
- **Improved I_{OH} Specifications**
- **Multiple Output Enables Allow Multiuser Control of the Interface**
- **Outputs Have Undershoot Protection Circuitry**
- **Power-Up High-Impedance State**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Buffered Control Inputs to Reduce DC Loading Effect**
- **Dependable Texas Instruments Quality and Reliability**

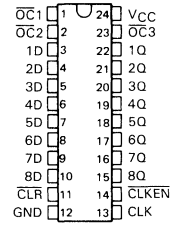
description

These 8-bit flip-flops feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing multiuser registers, I/O ports, bidirectional bus drivers, and working registers.

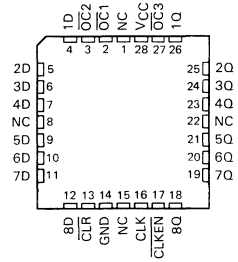
With the clock enable ($\overline{CLKEN}$) low, the eight D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock. Taking $\overline{CLKEN}$ high will disable the clock buffer, thus latching the outputs. The 'ALS29825 has non-inverting D inputs and the 'ALS29826 has inverting $\overline{D}$ inputs. Taking the $\overline{CLR}$ input low causes the eight Q outputs to go low independently of the clock.

Multiuser buffered output-control inputs ($\overline{OC}1$, $\overline{OC}2$, and $\overline{OC}3$) can be used to place the eight outputs in either a normal logic state (high or low level) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output controls do not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

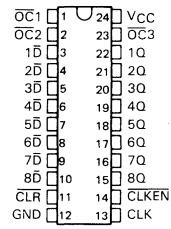
SN54ALS29825 . . . JT PACKAGE
SN74ALS29825 . . . DW OR NT PACKAGE
(TOP VIEW)



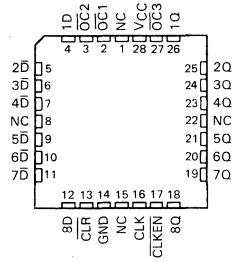
SN54ALS29825 . . . FK PACKAGE
SN74ALS29825 . . . FN PACKAGE
(TOP VIEW)



SN54ALS29826 . . . JT PACKAGE
SN74ALS29826 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54ALS29826 . . . FK PACKAGE
SN74ALS29826 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

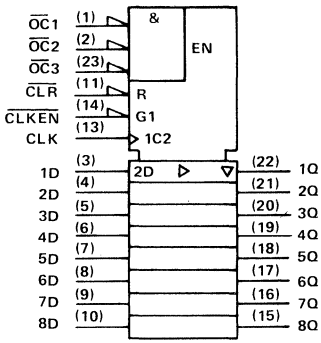
The SN54'family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

'ALS29825 FUNCTION TABLE

INPUTS					OUTPUT
$\overline{OC}$*	$\overline{CLR}$	$\overline{CLKEN}$	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	H	X	X	Q_0
H	X	X	X	X	Z

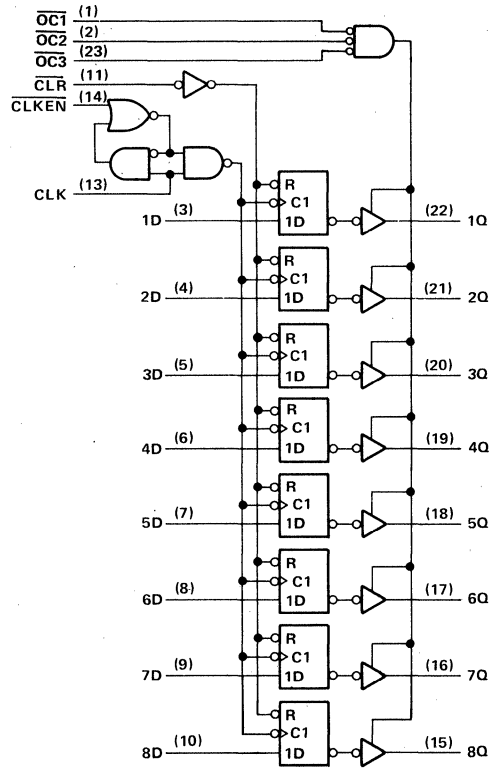
$\overline{OC}$* = H if any of $\overline{OC}$1, $\overline{OC}$2, or $\overline{OC}$3 is high.
$\overline{OC}$* = L if all of $\overline{OC}$1, $\overline{OC}$2, and $\overline{OC}$3 are low.

'ALS29825 logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12
Pin numbers shown are for DW, JT, and NT packages.

'ALS29825 logic diagram (positive logic)



Pin numbers are for DW, JT, and NT packages.

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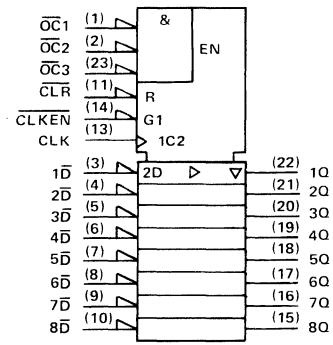
'ALS29826 FUNCTION TABLE

INPUTS					OUTPUT
$\overline{OC}$*	$\overline{CLR}$	$\overline{CLKEN}$	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	L
L	H	L	↑	L	H
L	H	H	X	X	Q_0
H	X	X	X	X	Z

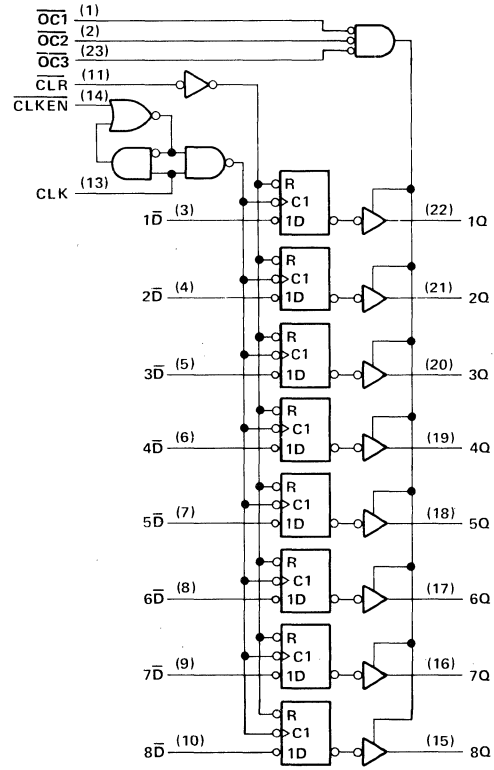
$\overline{OC}$* = H if any of $\overline{OC}$1, $\overline{OC}$2, or $\overline{OC}$3 is high.
$\overline{OC}$* = L if all of $\overline{OC}$1, $\overline{OC}$2, and $\overline{OC}$3 are low.

'ALS29826 logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers are for DW, JT, and NT packages.

'ALS29826 logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Input current . . . . . 100 mA
Output current . . . . . −30 mA to 5 mA
Operating free-air temperature range:
SN54ALS29825, SN54ALS29826 . . . . . −55°C to 125°C
SN74ALS29825, SN74ALS29826 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65 to 150°C

recommended operating conditions

			SN54ALS29825 SN54ALS29826			SN74ALS29825 SN74ALS29826			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−15			−24	mA
I_{OL}	Low-level output current				32			48	mA
t_w	Pulse duration	$\overline{CLR}$ low							ns
		CLK high							
		CLK low							
t_{su}	Setup time before CLK↑	$\overline{CLR}$ inactive							ns
		Data							
		$\overline{CLKEN}$ high or low							
t_h	Hold time, data after CLK↑	Data							ns
		$\overline{CLKEN}$							
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54ALS29825 SN54ALS29826			SN74ALS29825 SN74ALS29826			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = MIN to MAX,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = MIN,	I_{OH} = −15 mA	2.4	3.3					
		V_{CC} = MIN,	I_{OH} = −24 mA				2.4	3.2		
V_{OL}		V_{CC} = MIN,	I_{OL} = 32 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = MIN,	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}		V_{CC} = MAX,	V_O = 2.4 V			20			20	μA
I_{OZL}		V_{CC} = MAX,	V_O = 0.4 V			−20			−20	μA
I_I		V_{CC} = MAX,	V_I = 5.5 V			0.1			0.1	mA
I_{IH}		V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = MAX,	V_I = 0.4 V			−0.1			−0.1	mA
I_{OS}§		V_{CC} = MAX,	V_O = 0 V	−75		−250	−75		−250	mA
I_{CC}	'ALS29825	V_{CC} = MAX	Outputs high							mA
			Outputs low							
			Outputs disabled		48			48		
	'ALS29826		Outputs high							
			Outputs low							
			Outputs disabled		48			48		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Additional information on these products can be obtained from the factory as it becomes available.

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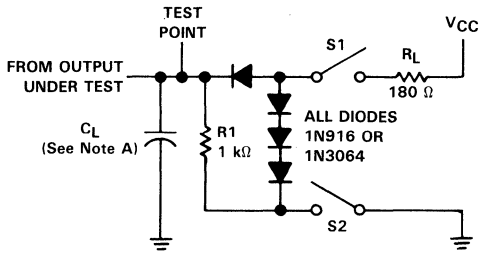
switching characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS See Figure 1	V_{CC} = 5 V, T_A = 25°C			V_{CC} = MIN TO MAX,† T_A = MIN TO MAX†				UNIT
				'ALS29825 'ALS29826			SN54ALS29825 SN54ALS29826		SN74ALS29825 SN74ALS29826		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	CLK	Any Q	C_L = 300 pF								ns
t_{PHL}											
t_{PLH}			C_L = 50 pF		6						
t_{PHL}					7						
t_{PHL}	$\overline{CLR}$	Any Q	C_L = 50 pF		13						ns
t_{PZH}	$\overline{OC}$	Any Q	C_L = 300 pF								ns
t_{PZL}											
t_{PZH}			C_L = 50 pF		12						
t_{PZL}					11						
t_{PHZ}	$\overline{OC}$	Any Q	C_L = 50 pF								ns
t_{PLZ}											
t_{PHZ}			C_L = 5 pF		5						
t_{PLZ}					6						

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

Additional information on these products can be obtained from the factory as it becomes available.

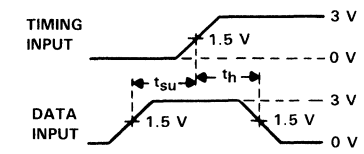
PARAMETER MEASUREMENT INFORMATION



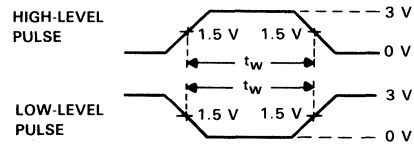
LOAD CIRCUIT

SWITCH POSITION TABLE

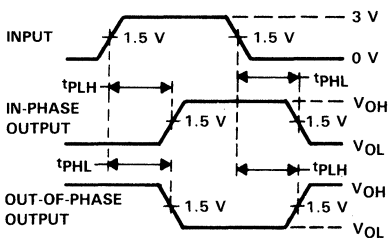
TEST	S1	S2
t_{PLH}	Closed	Closed
t_{PHL}	Closed	Closed
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed



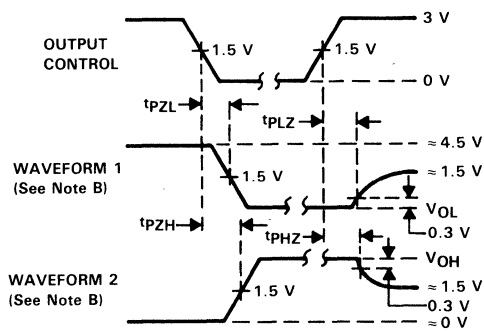
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_o = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

FIGURE 1

SN54AS29825, SN54AS29826, SN74AS29825, SN74AS29826
8-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

D2825, MAY 1986

- **Designed to be Interchangeable with AMD's AM29825 and AM29826**
- **Improved I_{OH} Specifications**
- **Multiple Output Enables Allow Multiuser Control of the Interface**
- **Outputs Have Undershoot Production Circuitry**
- **Power-Up High Impedance State**
- **Package Options Include Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Buffered Control Inputs to Reduce DC Loading Effects**
- **Dependable Texas Instruments Quality and Reliability**

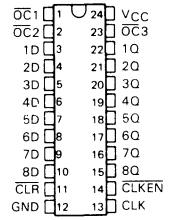
description

These 8-bit flip-flops feature three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. They are particularly suitable for implementing multiuser registers, I/O ports, bidirectional bus drivers, and working registers.

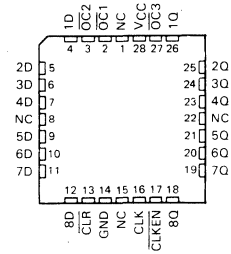
With the clock enable ($\overline{CLKEN}$) low, the eight D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock. Taking CLKEN high will disable the clock buffer, thus latching the outputs. The 'AS29825 has noninverting D inputs and the 'AS29826 has inverting D inputs. Taking the $\overline{CLR}$ input low causes the eight Q outputs to go low independently of the clock.

The buffered output-control inputs ($\overline{OC}1$, $\overline{OC}2$, and $\overline{OC}3$) can be used to place the eight outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output controls do not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

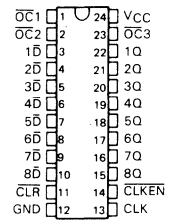
SN54AS29825 . . . JT PACKAGE
SN74AS29825 . . . DW OR NT PACKAGE
(TOP VIEW)



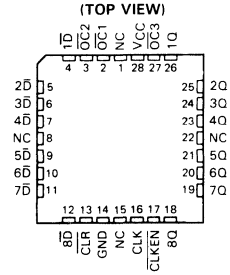
SN54AS29825 . . . FK PACKAGE
SN74AS29825 . . . FN PACKAGE
(TOP VIEW)



SN54AS29826 . . . JT PACKAGE
SN74AS29826 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54AS29826 . . . FK PACKAGE
SN74AS29826 . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

The SN54AS29825 and SN54AS29826 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS29825 and SN74AS29826 are characterized for operation from 0°C to 70°C.

FUNCTION TABLES

'AS29825

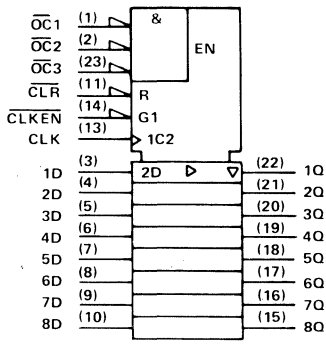
INPUTS					OUTPUT
$\overline{OC}$*	$\overline{CLR}$	$\overline{CLKEN}$	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	H	X	X	Q_0
H	X	X	X	X	Z

'AS29826

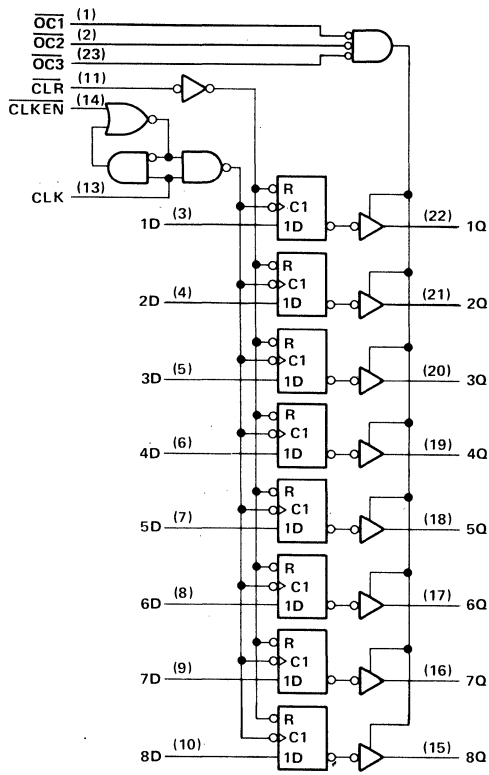
INPUTS					OUTPUT
$\overline{OC}$*	$\overline{CLR}$	$\overline{CLKEN}$	CLK	$\overline{D}$	Q
L	L	X	X	X	L
L	H	L	↑	H	L
L	H	L	↑	L	H
L	H	H	X	X	Q_0
H	X	X	X	X	Z

$\overline{OC}$* = H if any of $\overline{OC}$1, $\overline{OC}$2, or $\overline{OC}$3 is high.
$\overline{OC}$* = L if all of $\overline{OC}$1, $\overline{OC}$2, and $\overline{OC}$3 are low.

'AS29825 logic symbol†

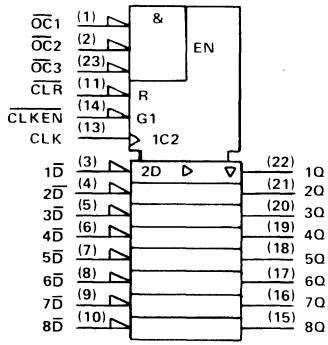


'AS29825 logic diagram (positive logic)

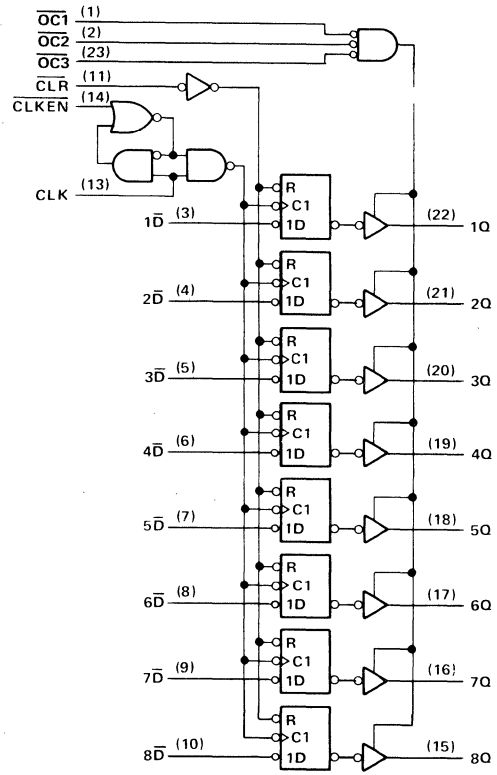


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

'AS29826 logic symbol†



'AS29826 logic diagram (positive logic)



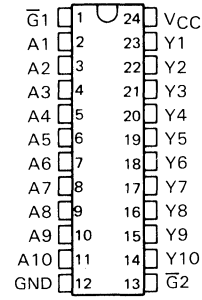
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, and NT packages.

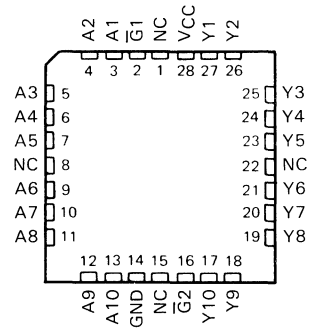
D2912, JANUARY 1986—REVISED MAY 1986

- **Functionally Equivalent to AM29827 and AM29828**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **P-N-P Inputs Reduce D-C Loading**
- **Data Flow-Thru Pinout (All Inputs on Opposite Side from Outputs)**
- **Power-Up High-Impedance State**
- **Package Options Include Plastic "Small Outline" Packages, Plastic Chip Carriers, and Standard Plastic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

DW OR NT PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



description

These 10-bit buffers and bus drivers provide high-performance bus interface for wide data paths or busses carrying parity.

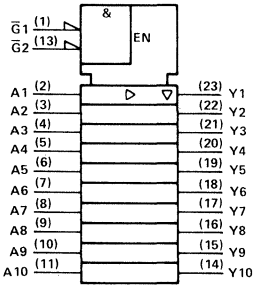
The three-state control gate is a 2-input NOR such that if either $\overline{G1}$ or $\overline{G2}$ is high, all ten outputs are in the high-impedance state.

The SN74ALS29827 provides true data and the SN74ALS29828 provides inverted data at the outputs.

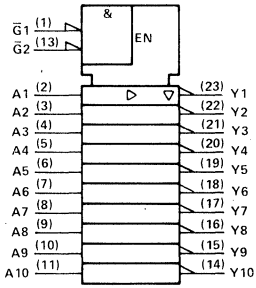
The SN74' family is characterized for operation from 0°C to 70°C.

logic symbols†

'ALS29827



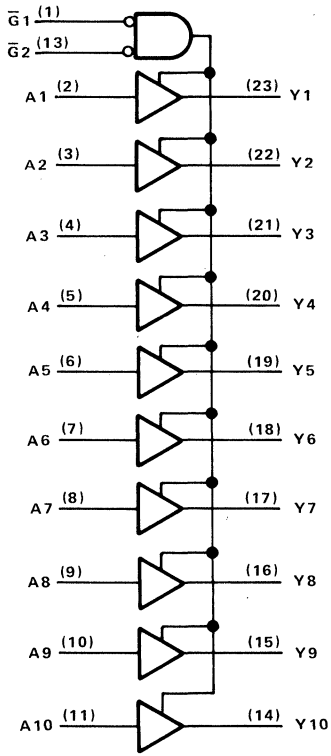
'ALS29828



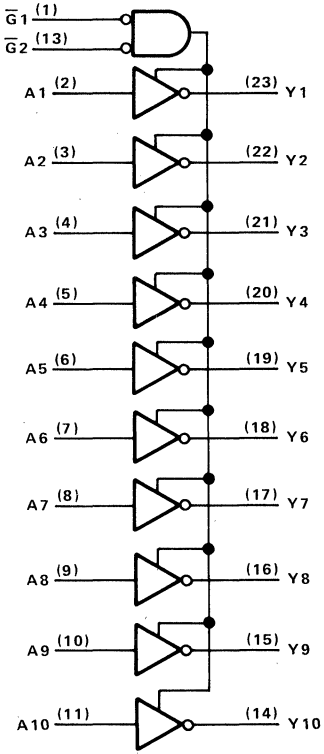
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)

'ALS29827



'ALS29828



Pin numbers shown are DW and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 5.5 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V, I_I = −18 mA			−1.2	V
V_{OH}		V_{CC} = 4.75 V, I_{OH} = −15 mA	2.4			V
		V_{CC} = 4.75 V, I_{OH} = −24 mA	2			
V_{OL}		V_{CC} = 4.75 V, I_{OL} = 48 mA		0.35	0.5	V
I_{OZH}		V_{CC} = 5.25 V, V_O = 2.4 V			20	μA
I_{OZL}		V_{CC} = 5.25 V, V_O = 0.4 V			−20	μA
I_I		V_{CC} = 5.25 V, V_I = 5.5 V			0.1	mA
I_{IH}		V_{CC} = 5.25 V, V_I = 2.7 V			20	μA
I_{IL}		V_{CC} = 5.25 V, V_I = 0.4 V			−0.1	mA
I_{OS}‡		V_{CC} = 5.25 V, V_O = 0 V	−75		−250	mA
I_{CC}	'ALS29827	V_{CC} = 5.25 V		25	40	mA
	'ALS29828	V_{CC} = 5.25 V		25	40	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

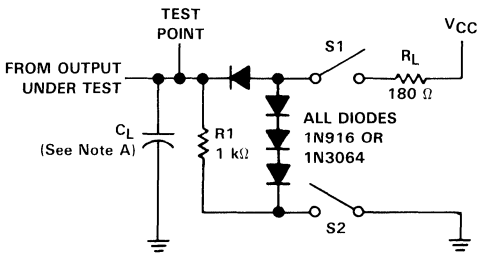
SN74ALS29827 switching characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS See Figure 1	V_{CC} = 5 V, T_A = 25°C			V_{CC} = 4.75 V to 5.25 V, T_A = 0°C to 70°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A	Y	C_L = 300 pF		7.5	11		15	ns
t_{PHL}					11	16		18	
t_{PLH}			C_L = 50 pF		3.5	6		8	
t_{PHL}					6.5	8		10	
t_{PZH}	$\overline{G}$	Y	C_L = 300 pF		13	17		20	ns
t_{PZL}					16	21		23	
t_{PZH}			C_L = 50 pF		6.5	12		15	
t_{PZL}					9.5	12		15	
t_{PHZ}	$\overline{G}$	Y	C_L = 50 pF		10	16		17	ns
t_{PLZ}					4	9		12	
t_{PHZ}			C_L = 5 pF		4.5	8		9	
t_{PLZ}					4.5	8		9	

SN74ALS29828 switching characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS See Figure 1	V_{CC} = 5 V, T_A = 25°C			V_{CC} = 4.75 V to 5.25 V, T_A = 0°C to 70°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A	Y	C_L = 300 pF		7.3	10		14	ns
t_{PHL}					8.5	12.9		14	
t_{PLH}			C_L = 50 pF		4	5.2		7	
t_{PHL}					3	5.9		7.5	
t_{PZH}	$\overline{G}$	Y	C_L = 300 pF		13	17		20	ns
t_{PZL}					16	21		23	
t_{PZH}			C_L = 50 pF		6.5	12		15	
t_{PZL}					9.5	12		15	
t_{PHZ}	$\overline{G}$	Y	C_L = 50 pF		10	16		17	ns
t_{PLZ}					4	9		12	
t_{PHZ}			C_L = 5 pF		4.5	8		9	
t_{PLZ}					4.5	8		9	

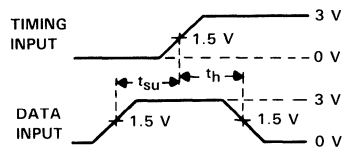
PARAMETER MEASUREMENT INFORMATION



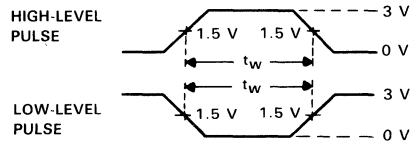
LOAD CIRCUIT

SWITCH POSITION TABLE

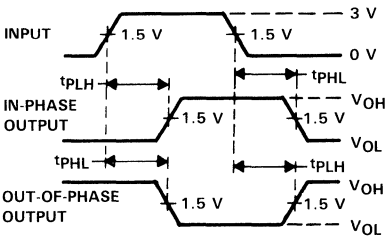
TEST	S1	S2
t_{PLH}	Closed	Closed
t_{PHL}	Closed	Closed
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed



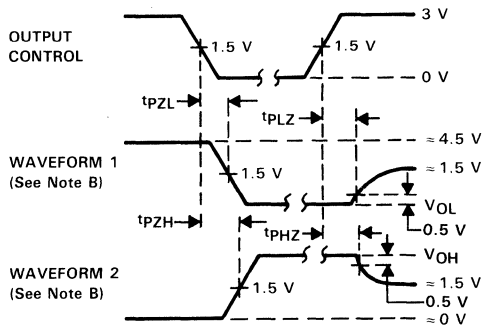
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

FIGURE 1

SN54AS29841, SN54AS29842, SN74AS29841, SN74AS29842
10-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

D2910, MAY 1986

- **Designed to be Interchangeable with AMD AM29841 and AM29842**
- **Bus-Structured Pinout**
- **Provide Extra Bus-Driving Latches Necessary for Wider Address/Data Paths or Buses with Parity**
- **Buffered Control Inputs to Reduce DC Loading**
- **Power-Up High-Impedance State**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These 10-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

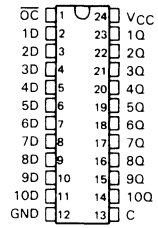
The ten latches are transparent D-type. The 'AS29841 has noninverting data (D) inputs. The 'AS29842 has inverting $\overline{D}$ inputs.

A buffered output control ($\overline{OC}$) input can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

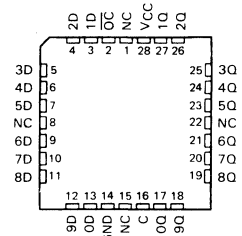
The output control ($\overline{OC}$) does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are off.

The SN54AS29841 and SN54AS29842 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS29841 and SN74AS29842 are characterized for operation from 0°C to 70°C.

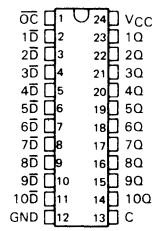
SN54AS29841 . . . JT PACKAGE
SN74AS29841 . . . DW OR NT PACKAGE
(TOP VIEW)



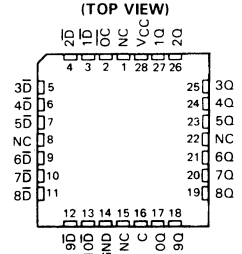
SN54AS29841 . . . FK PACKAGE
SN74AS29841 . . . FN PACKAGE
(TOP VIEW)



SN54AS29842 . . . JT PACKAGE
SN74AS29842 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54AS29842 . . . FK PACKAGE
SN74AS29842 . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLES

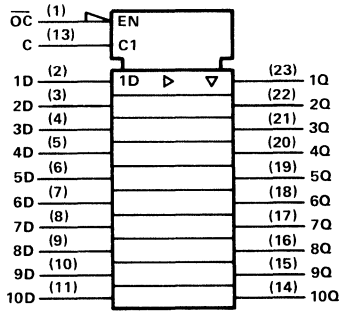
'AS29841

INPUTS			OUTPUT
$\overline{OC}$	C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_O
H	X	X	Z

'AS29842

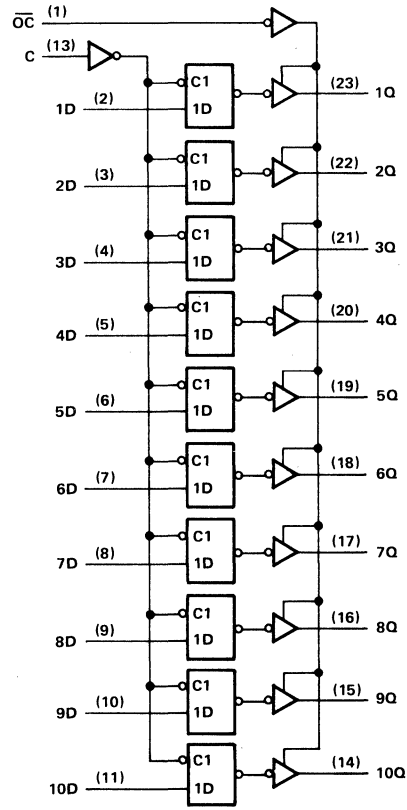
INPUTS			OUTPUT
$\overline{OC}$	C	$\overline{D}$	Q
L	H	H	L
L	H	L	H
L	L	X	Q_O
H	X	X	Z

'AS29841 logic symbol†



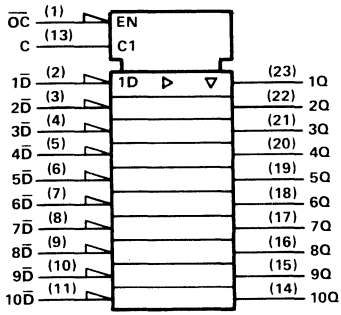
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

'AS29841 logic diagram (positive logic)



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

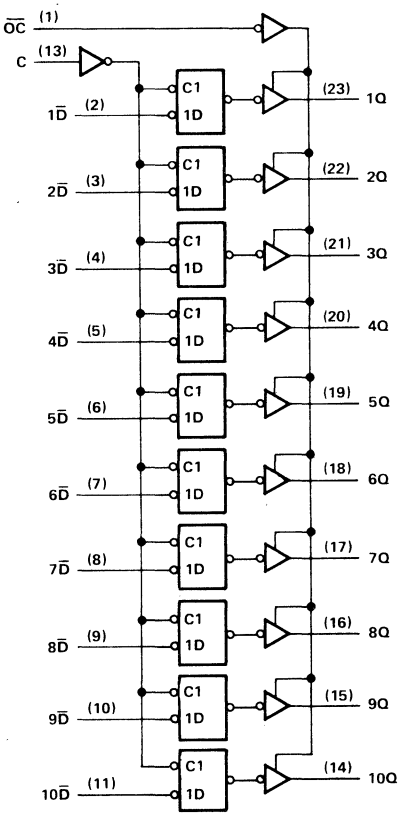
'AS29842 logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, and NT packages.

'AS29842 logic diagram (positive logic)



SN54AS29843, SN54AS29844, SN74AS29843, SN74AS29844
9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

D2910, MAY 1986

- Designed to be Interchangeable with AMD AM29843 and AM29844
- Bus-Structured Pinout
- Provide Extra Bus-Driving Latches Necessary for Wider Address/Data Paths or Buses with Parity
- Buffered Control Inputs to Reduce DC Loading
- Power-Up High-Impedance State
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

These 9-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

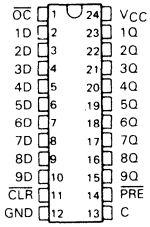
The nine latches are transparent D-type. The 'AS29843 has noninverting data (D) inputs. The 'AS29844 has inverting $\overline{D}$ inputs.

A buffered output control ($\overline{OC}$) input can be used to place the nine outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

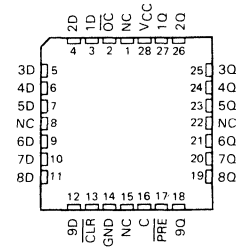
The output control ($\overline{OC}$) does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are off.

The SN54AS29843 and SN54AS29844 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS29843 and SN74AS29844 are characterized for operation from 0°C to 70°C.

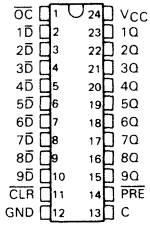
SN54AS29843 . . . JT PACKAGE
SN74AS29843 . . . DW OR NT PACKAGE
(TOP VIEW)



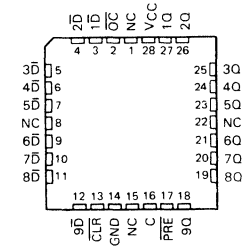
SN54AS29843 . . . FK PACKAGE
SN74AS29843 . . . FN PACKAGE
(TOP VIEW)



SN54AS29844 . . . JT PACKAGE
SN74AS29844 . . . DW or NT PACKAGE
(TOP VIEW)



SN54AS29844 . . . FK PACKAGE
SN74AS29844 . . . FN PACKAGE
(TOP VIEW)



NC No internal connection

FUNCTION TABLES

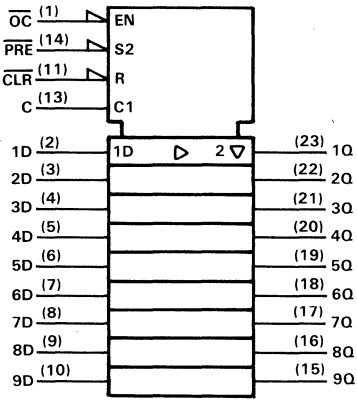
'AS29843

INPUTS					OUTPUT
PRE	CLR	OC	C	D	Q
L	X	L	X	X	H
H	L	L	X	X	L
H	H	L	H	L	L
H	H	L	H	H	H
H	H	L	L	X	Q_O
X	X	H	X	X	Z

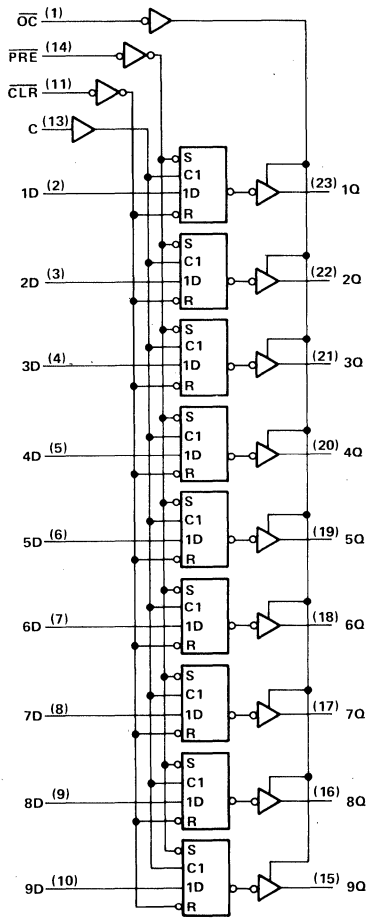
'AS29844

INPUTS					OUTPUT
PRE	CLR	OC	C	D	Q
L	X	L	X	X	H
H	L	L	X	X	L
H	H	L	H	L	H
H	H	L	H	H	L
H	H	L	L	X	Q_O
X	X	H	X	X	Z

'AS29843 logic symbol†



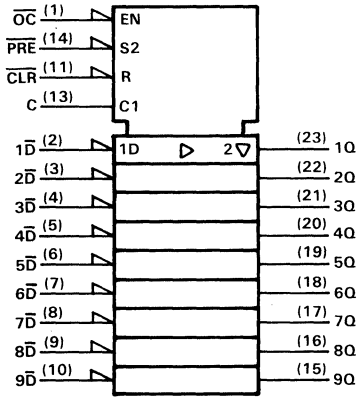
'AS29843 logic diagram (positive logic)



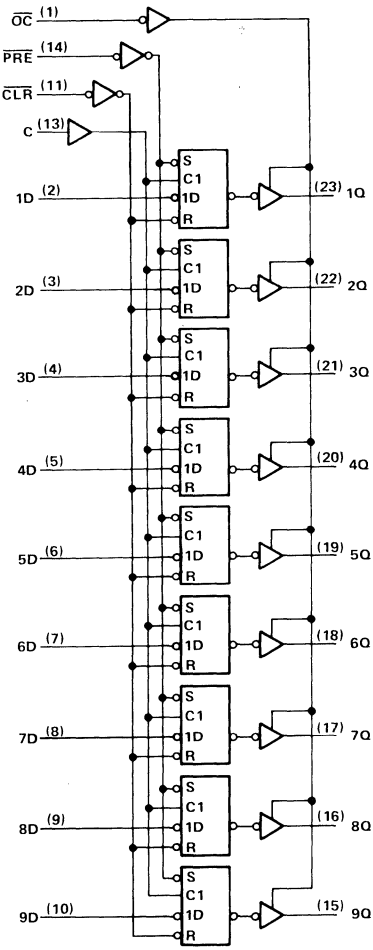
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, and NT packages.

'AS29844 logic symbol†



'AS29844 logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

SN54AS29845, SN54AS29846, SN74AS29845, SN74AS29846
8-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

D2910, MAY, 1986

- **Designed to be Interchangeable with AMD AM29845 and AM29846**
- **Bus-Structured Pinout**
- **Provides Extra Bus-Driving Latches Necessary for Wider Address/Data Paths or Buses with Parity**
- **Buffered Control Inputs to Reduce DC Loading**
- **Power-Up High-Impedance State**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

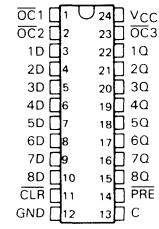
description

These 8-bit latches feature three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

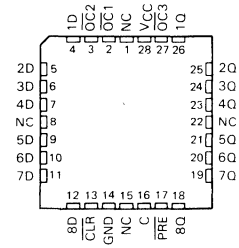
The eight latches are transparent D-type. The 'AS29845 has noninverting data (D) inputs. The 'AS29846 has inverting $\overline{D}$ inputs. Since $\overline{CLR}$ and $\overline{PRE}$ are independent of the clock, taking the $\overline{CLR}$ input low will cause the eight Q outputs to go low. Taking the $\overline{PRE}$ input low will cause the eight Q outputs to go high. When both $\overline{PRE}$ and $\overline{CLR}$ are taken low, the outputs will follow the preset condition.

The buffered output controls input ($\overline{OC}1$, $\overline{OC}2$, and $\overline{OC}3$) can be used to place the eight outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output controls do not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

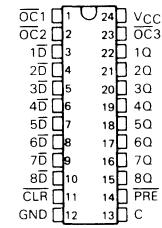
SN54AS29845 . . . JT PACKAGE
SN74AS29845 . . . DW OR NT PACKAGE
(TOP VIEW)



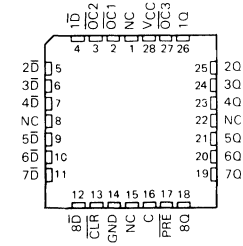
SN54AS29845 . . . FK PACKAGE
SN74AS29845 . . . FN PACKAGE
(TOP VIEW)



SN54AS29846 . . . JT PACKAGE
SN74AS29846 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54AS29846 . . . FK PACKAGE
SN74AS29846 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection.

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The SN54AS29845 and SN54AS29846 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS29845 and SN74AS29846 are characterized for operation from 0°C to 70°C.

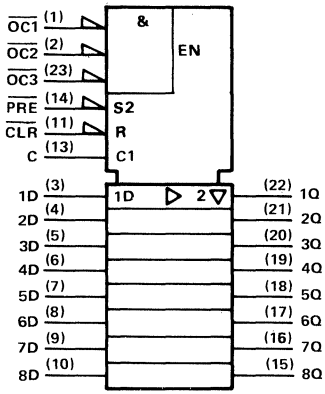
FUNCTION TABLES

INPUTS							OUTPUT
$\overline{PRE}$	$\overline{CLR}$	$\overline{OC1}$	$\overline{OC2}$	$\overline{OC3}$	C	D	Q
L	H	L	L	L	X	X	H
H	L	L	L	L	X	X	L
L	L	L	L	L	X	X	H
H	H	L	L	L	H	L	L
H	H	L	L	L	H	H	H
H	H	L	L	L	L	X	Q_0
X	X	X	X	H	X	X	Z
X	X	X	H	X	X	X	Z
X	X	H	X	X	X	X	Z

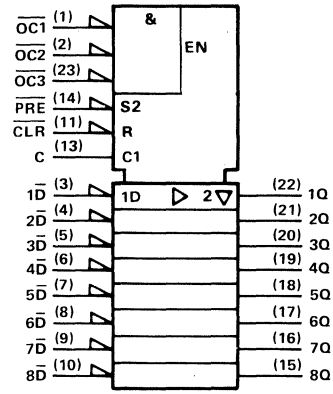
INPUTS							OUTPUT
$\overline{PRE}$	$\overline{CLR}$	$\overline{OC1}$	$\overline{OC2}$	$\overline{OC3}$	C	$\overline{D}$	Q
L	H	L	L	L	X	X	H
H	L	L	L	L	X	X	H
L	L	L	L	L	X	X	H
H	H	L	L	L	H	L	H
H	H	L	L	L	H	H	L
H	H	L	L	L	L	X	Q_0
X	X	X	X	H	X	X	Z
X	X	X	H	X	X	X	Z
X	X	H	X	X	X	X	Z

logic symbols†

'AS29845



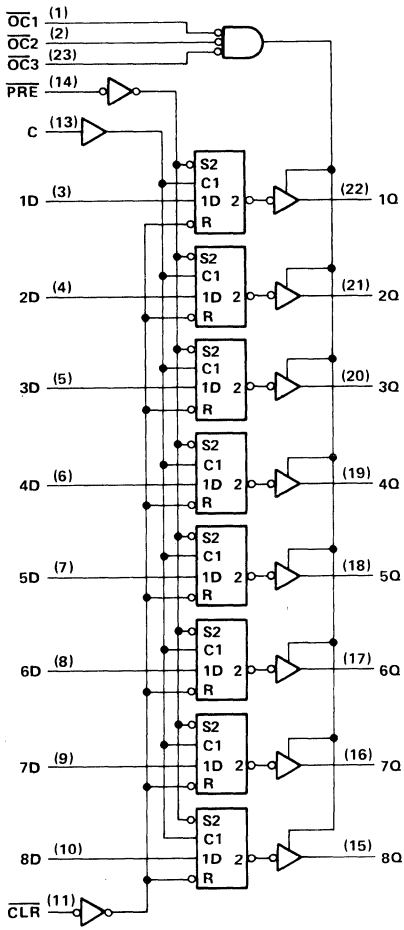
'AS29846



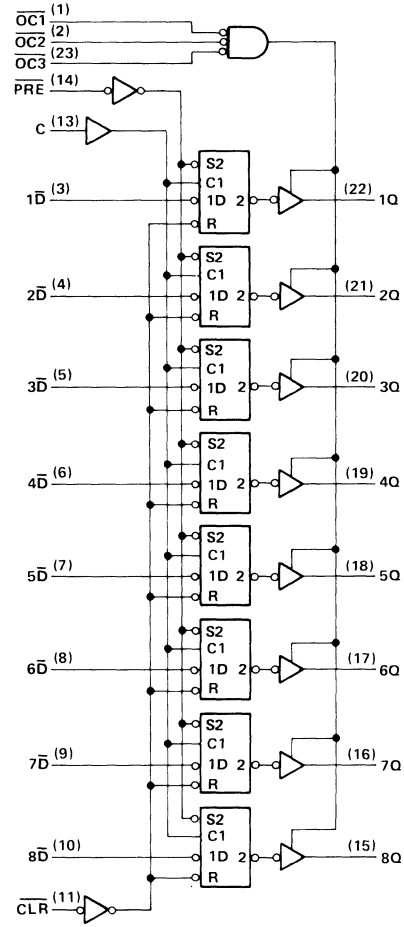
† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

logic diagrams (positive logic)

'AS29845



'AS29846



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54AS' . . . . . −55°C to 125°C
SN74AS' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

2 ALS and AS Circuits

D2915, JANUARY 1986—REVISED MAY 1986

- **Functionally Equivalent to AM29861 and AM29862**
- **Choice of True or Inverting Logic**
- **Power-Up High-Impedance State**
- **Package Options Include Plastic "Small Outline" Packages, Plastic Chip Carriers, and Standard Plastic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These 10-bit bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs ($\overline{G}$BA and $\overline{G}$AB).

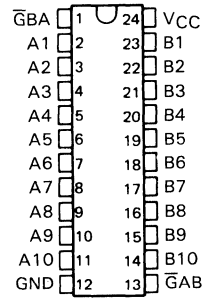
The enable inputs can be used to disable the device so that the buses are effectively isolated.

The SN74' family is characterized for operation from 0°C to 70°C.

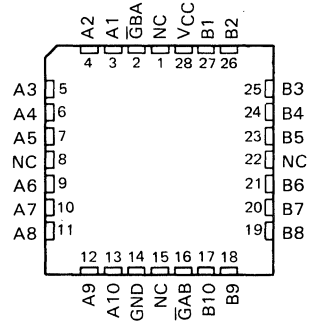
FUNCTION TABLE

INPUTS		OPERATION	
$\overline{G}$AB	$\overline{G}$BA	ALS29861	ALS29862
L	H	A to B	$\overline{A}$ to B
H	L	B to A	$\overline{B}$ to A
H	H	Isolation	Isolation
L	L	Latch A and B (A = B)	Latch A and B (A = $\overline{B}$)

DW OR NT PACKAGE
(TOP VIEW)



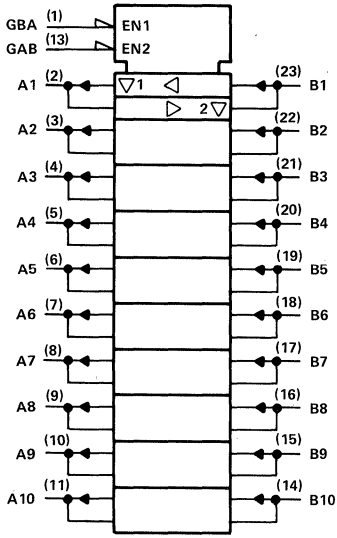
FN PACKAGE
(TOP VIEW)



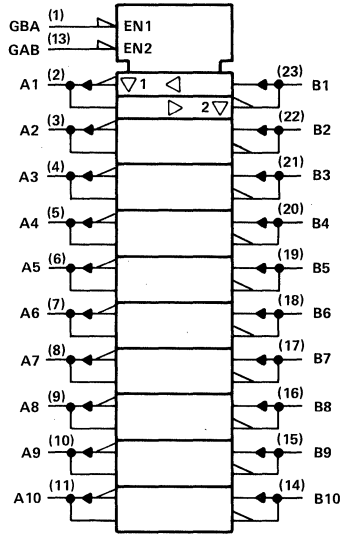
NC—No internal connection

logic symbols†

'ALS29861



'ALS29862



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW and NT packages.

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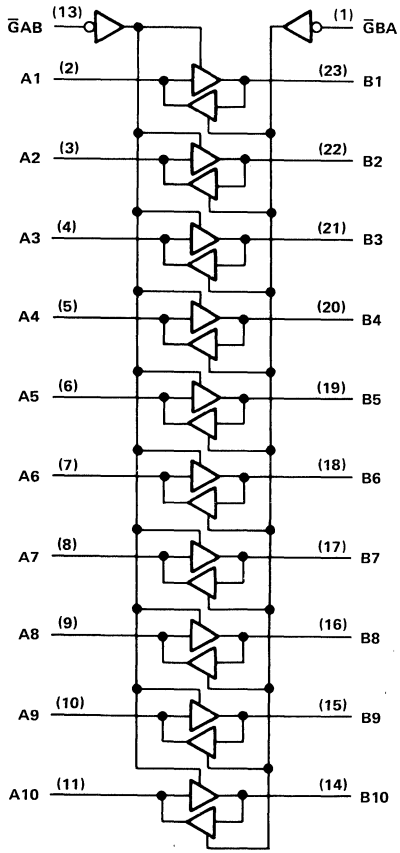
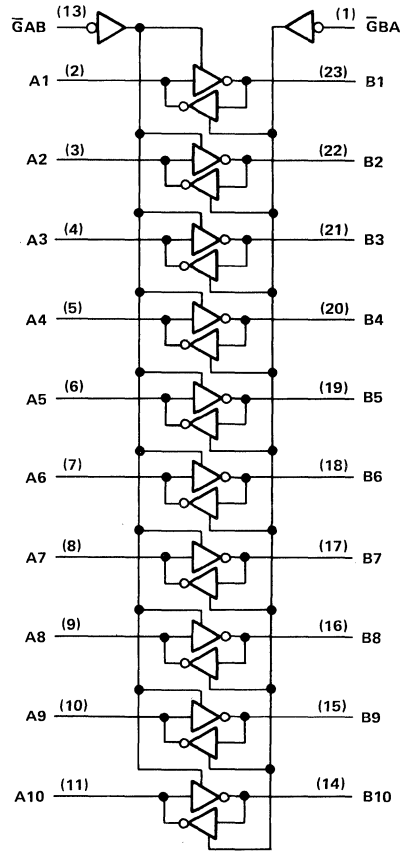
logic diagrams

'ALS29861



'ALS29862



Pin numbers shown are for DW and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs and I/O ports . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V, I_I = −18 mA			−1.2	V
V_{OH}		V_{CC} = 4.75 V, I_{OH} = −15 mA	2.4			V
		V_{CC} = 4.75 V, I_{OH} = −24 mA	2			
V_{OL}		V_{CC} = 4.75 V, I_{OL} = 48 mA		0.35	0.5	V
I_I		V_{CC} = 5.25 V, V_I = 5.5 V			0.1	mA
I_{IH}	Control inputs	V_{CC} = 5.25 V, V_I = 2.7 V			20	μA
	A or B ports‡				20	
I_{IL}	Control inputs	V_{CC} = 5.25 V, V_I = 0.4 V			−0.1	mA
	A or B ports‡				−0.1	
I_{OS}§		V_{CC} = 5.25 V, V_O = 0 V	−75		−250	mA
I_{CC}	'ALS29861	V_{CC} = 5.25 V		40	65	mA
	'ALS29862			40	65	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

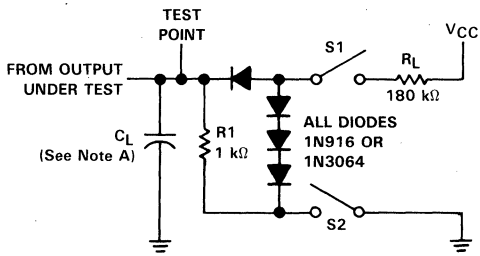
SN74ALS29861 switching characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS See Figure 1	V_{CC} = 5 V, T_A = 25°C			V_{CC} = 4.75 V to 5.25 V, T_A = 0°C to 70°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	C_L = 300 pF		8	11		15	ns
t_{PHL}					11	14		15	
t_{PLH}			C_L = 50 pF		4.8	6		8	
t_{PHL}					5.2	6.2		8	
t_{PZH}	$\overline{G}$AB or $\overline{G}$BA	A or B	C_L = 300 pF		11	17		20	ns
t_{PZL}					17	21		23	
t_{PZH}			C_L = 50 pF		6.5	12		15	
t_{PZL}					9.5	12		15	
t_{PHZ}	$\overline{G}$AB or $\overline{G}$BA	A or B	C_L = 50 pF		10	16		17	ns
t_{PLZ}					4.5	9		12	
t_{PHZ}			C_L = 5 pF		3.5	8		9	
t_{PLZ}					3.5	8		9	

SN74ALS29862 switching characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS See Figure 1	V_{CC} = 5 V, T_A = 25°C			V_{CC} = 4.75 V to 5.25 V, T_A = 0°C to 70°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	C_L = 300 pF		8	10		14	ns
t_{PHL}					9	12.9		14	
t_{PLH}			C_L = 50 pF		4	5.2		7	
t_{PHL}					3	5.9		7.5	
t_{PZH}	$\overline{G}$AB or $\overline{G}$BA	A or B	C_L = 300 pF		11	17		20	ns
t_{PZL}					17	21		23	
t_{PZH}			C_L = 50 pF		6.5	12		15	
t_{PZL}					9.5	12		15	
t_{PHZ}	$\overline{G}$AB or $\overline{G}$BA	A or B	C_L = 50 pF		10	16		17	ns
t_{PLZ}					4.5	9		12	
t_{PHZ}			C_L = 5 pF		3.5	8		9	
t_{PLZ}					3.5	8		9	

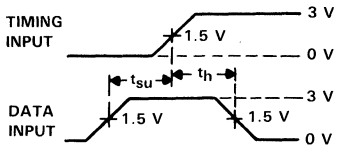
PARAMETER MEASUREMENT INFORMATION



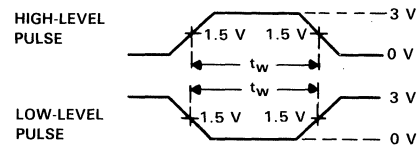
LOAD CIRCUIT

SWITCH POSITION TABLE

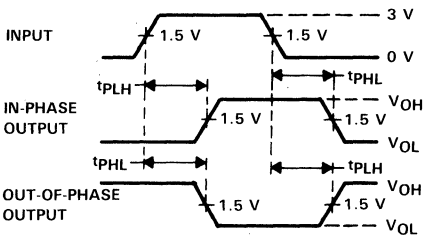
TEST	S1	S2
t_{PLH}	Closed	Closed
t_{PHL}	Closed	Closed
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed



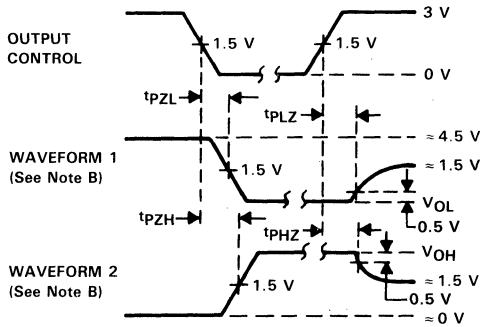
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

FIGURE 1

D2915, JANUARY 1986–REVISED MAY 1986

- **Functionally Equivalent to AM29863 and AM29864**
- **Choice of True or Inverting Logic**
- **Power-Up High-Impedance State**
- **Package Options Include Plastic "Small Outline" Packages, Plastic Chip Carriers, and Standard Plastic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

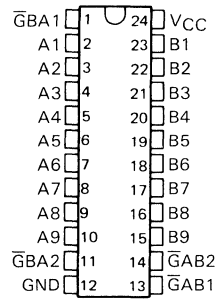
description

These 9-bit bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

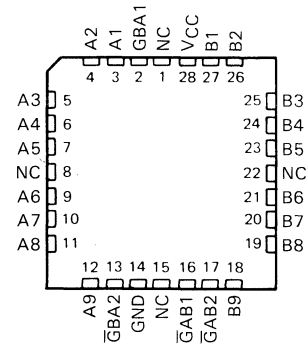
These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs ($\overline{G}$BA1, $\overline{G}$BA2, $\overline{G}$AB1, and $\overline{G}$AB2).

The SN74' family is characterized for operation from 0°C to 70°C.

DW OR NT PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



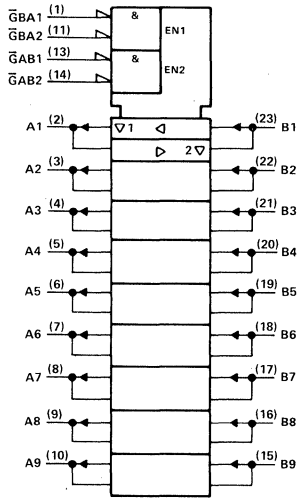
NC – No internal connection

FUNCTION TABLE

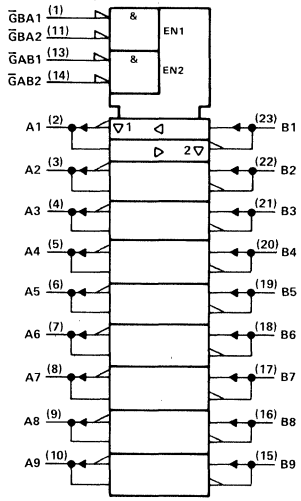
ENABLE INPUTS				OPERATION	
$\overline{G}$AB1	$\overline{G}$AB2	$\overline{G}$BA1	$\overline{G}$BA2	'ALS29863	'ALS29864
L	L	L	L	Latch A and B	Latch A and B
L	L	H	X	A to B	A to $\overline{B}$
L	L	X	H		
H	X	L	L	B to A	B to $\overline{A}$
X	H	L	L		
H	X	H	X	Isolation	Isolation
H	X	X	H		
X	H	X	H		
X	H	H	X		

logic symbols†

'ALS29863



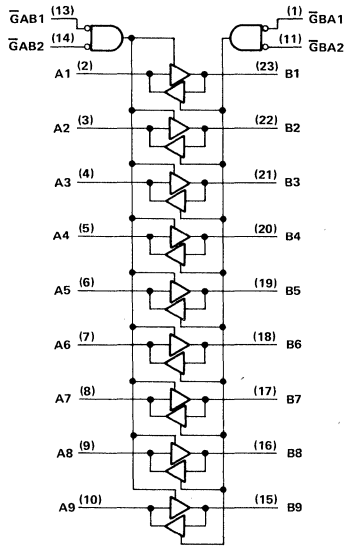
'ALS29864



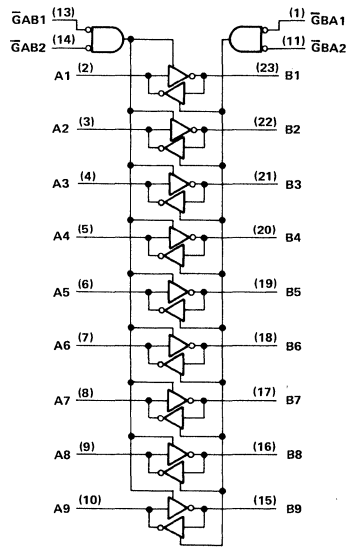
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams

'ALS29863



'ALS29864



Pin numbers shown are for DW and NT packages.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs and I/O ports . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V, I_I = −18 mA			−1.2	V
V_{OH}		V_{CC} = 4.75 V, I_{OH} = −15 mA	2.4			V
		V_{CC} = 4.75 V, I_{OH} = −24 mA	2			
V_{OL}		V_{CC} = 4.75 V, I_{OL} = 48 mA		0.35	0.5	V
I_I		V_{CC} = 5.25 V, V_I = 5.5 V			0.1	mA
I_{IH}	Control inputs	V_{CC} = 5.25 V, V_I = 2.7 V			20	μA
	A or B ports‡				20	
I_{IL}	Control inputs	V_{CC} = 5.25 V, V_I = 0.4 V			−0.1	mA
	A or B ports‡				−0.1	
I_{OS}§		V_{CC} = 5.25 V, V_O = 0 V	−75		−250	mA
I_{CC}	'ALS29863	V_{CC} = 5.25 V		40	65	mA
	'ALS29864			40	65	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

SN74ALS29863 switching characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS See Figure 1	V_{CC} = 5 V, T_A = 25°C			V_{CC} = 4.75 V to 5.25 V, T_A = 0°C to 70°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	C_L = 300 pF		7.5	11		15	ns
t_{PHL}					11	16		18	
t_{PLH}			C_L = 50 pF		3.5	6		8	
t_{PHL}					6.5	8		10	
t_{PZH}	$\overline{G}$AB or $\overline{G}$BA	A or B	C_L = 300 pF		13	17		20	ns
t_{PZL}					16	21		23	
t_{PZH}			C_L = 50 pF		6.5	12		15	
t_{PZL}					9.5	12		15	
t_{PHZ}	$\overline{G}$AB or $\overline{G}$BA	A or B	C_L = 50 pF		10	16		17	ns
t_{PLZ}					4	9		12	
t_{PHZ}			C_L = 5 pF		4.5	8		9	
t_{PLZ}					4.5	8		9	

SN74ALS29864 switching characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS See Figure 1	V_{CC} = 5 V, T_A = 25°C			V_{CC} = 4.75 V to 5.25 V, T_A = 0°C to 70°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	C_L = 300 pF		8	11		14	ns
t_{PHL}					10	12.9		14	
t_{PLH}			C_L = 50 pF		5	7		8	
t_{PHL}					3	5.9		7.5	
t_{PZH}	$\overline{G}$AB or $\overline{G}$BA	A or B	C_L = 300 pF		11	17		20	ns
t_{PZL}					19	23		24	
t_{PZH}			C_L = 50 pF		6.5	12		15	
t_{PZL}					9.5	12		15	
t_{PHZ}	$\overline{G}$AB or $\overline{G}$BA	A or B	C_L = 50 pF		10	16		17	ns
t_{PLZ}					4	9		12	
t_{PHZ}			C_L = 5 pF		6	8		9	
t_{PLZ}					3.5	8		9	

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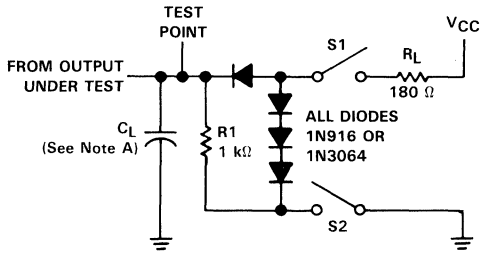
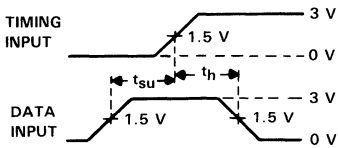
PARAMETER MEASUREMENT INFORMATION



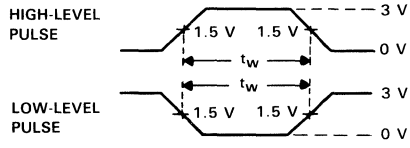
LOAD CIRCUIT

SWITCH POSITION TABLE

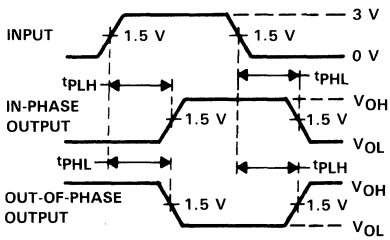
TEST	S1	S2
t_{PLH}	Closed	Closed
t_{PHL}	Closed	Closed
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed



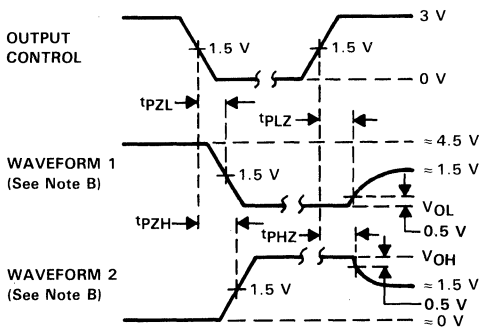
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

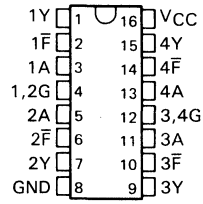
FIGURE 1

SN75ALS126 QUADRUPLE LINE DRIVER

D2299, FEBRUARY 1986

- Meets IBM 360/370 I/O Interface Specification GA22-6974-3 (Also see SN75ALS130)
- Minimum Output Voltage of 3.11 V at I_{OH} = −60 mA
- Fault Flag Circuit Output Signals Driver Output Fault
- Fault-Detection Current Limit Circuit Minimizes Power Dissipation During a Fault Condition
- Advanced Low-Power Schottky Circuitry
- Dual Common Enable
- Individual Fault Flags
- Designed to be an Improved Replacement for the MC3481

SN75ALS126 . . . D, J, OR N PACKAGE
(TOP VIEW)



FUNCTION TABLE

INPUTS		OUTPUTS	
G	A	Y	F̄
L	X	L	H
H	H	H	H
H	H	S	L

H = high level, L = low level,
X = irrelevant, S = shorted to ground

description

The SN75ALS126 quadruple line driver is designed to meet the IBM360/370 I/O specifications GA22-6974-3. The output voltage is 3.11 volts minimum (at I_{OH} = −59.3 milliamperes) over the recommended ranges of supply voltage (4.5 volts to 5.5 volts) and temperature (0°C to 70°C). Driver outputs use a fault-detection current-limit circuit to allow high drive current but still minimize power dissipation when the output is shorted to ground. The SN75ALS126 is compatible with standard TTL logic and supply voltages.

The SN75ALS126 employs the IMPACT™ process to achieve fast switching speeds and low power dissipation. Fault-flag circuitry is designed to sense and signal a line short on any Y line. Upon detecting an output fault condition, the fault-flag circuit forces the driver output into a low state and signals a fault condition by causing the fault-flag output to go low.

The SN75ALS126 will drive a 50-ohm load as required in the IBM GA22-6974-3 specification or a 90-ohm load as used in many I/O systems. Optimum performance can be achieved when the device is used with either the SN75125, SN75127, SN75128, or SN75129 line receivers.

The SN75ALS126 is characterized for operation from 0°C to 70°C.

IMPACT is a trademark of Texas Instruments Incorporated

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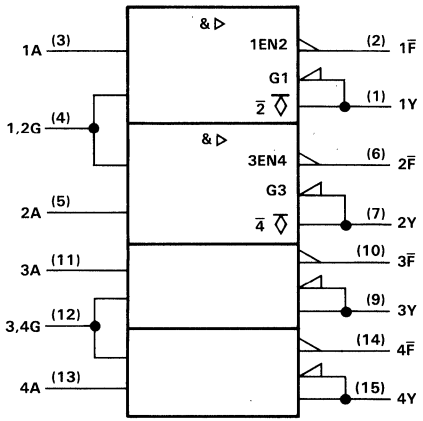
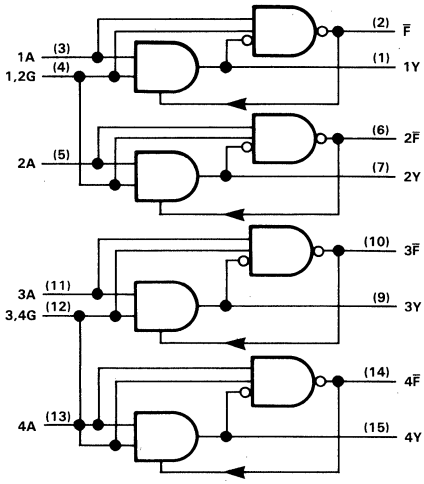
logic symbol†

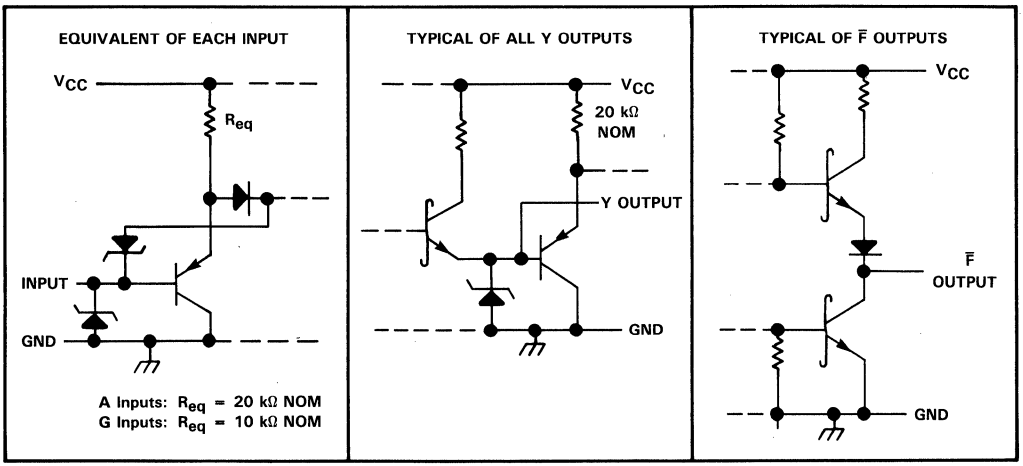


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 1):
D package . . . . . 950 mW
J package . . . . . 1025 mW
N package . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

NOTE 1: For operation above 25°C free-air temperature, derate the D package to 608 mW at 70°C at the rate of 7.6 mW/°C, the J package to 656 mW at 70°C at the rate of 8.2 mW/°C, and the N package to 736 mW at 70°C at the rate of 9.2 mW/°C.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.95	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			−59.3	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{IK}	Input clamp voltage	A,G	I_I = −18 mA		−1.5	V
V_{OH}	High-level output voltage	Y	V_{CC} = 4.5 V, I_{OH} = −59.3 mA, V_{IH} = 2 V	3.11		V
		Y	V_{CC} = 5.25 V, I_{OH} = −41 mA, V_{IH} = 2 V	3.9		
		$\overline{F}$	V_{CC} = 4.5 V, I_{OH} = −400 μA, V_{IH} = 2 V	2.5		
V_{OL}	Low-level output voltage	Y	V_{CC} = 5.5 V, I_{OL} = −240 μA, V_{IL} = 0.8 V		0.15	V
		Y	V_{CC} = 5.95 V, I_{OL} = −1 mA, V_{IL} = 0.8 V		0.15	
		$\overline{F}$	V_{CC} = 4.5 V, I_{OL} = 8 mA, Y at 0 V		0.5	
$I_{O(off)}$	Off-state output current	Y	V_{CC} = 4.5 V, V_{IL} = 0, V_O = 3.11 V		100	μA
		Y	V_{CC} = 0, V_{IL} = 0, V_O = 3.11 V		200	
I_I	Input current	A	V_{CC} = 4.5 V, V_{IH} = 5.5 V		100	μA
		G			400	
I_{IH}	High-level input current	A	V_{CC} = 4.5 V, V_{IH} = 2.7 V		20	μA
		G			80	
I_{IL}	Low-level input current	A	V_{CC} = 5.95 V, V_{IL} = 0.4 V		250	μA
		G			−1000	
I_{OS}	Short-circuit output	Y	V_{CC} = 5.5 V, V_O = 0		−5	mA
		$\overline{F}$		−15	−100	
		Y	V_{CC} = 5.95 V, V_O = 0		−5	
		$\overline{F}$		−15	−110	
I_{CCH}	Supply current, all outputs high		V_{CC} = 5.5 V, No load		25	mA
			V_{CC} = 5.95 V, No load		27	
I_{CCL}	Supply current, Y outputs low		V_{CC} = 5.5 V, No load		45	mA
			V_{CC} = 5.95 V, No load		47	

switching characteristics over recommended operating free-air temperature range

PARAMETER		FROM	TO	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	A	Y	V_{CC} = 4.5 V to 5.5 V, R_L = 50 Ω, C_L = 50 pF, $V_{H(ref)}$ = 3.11 V, See Figures 1 and 2		30	ns
t_{PHL}	Propagation delay time, high-to-low-level output					28	ns
$\frac{t_{PLH}}{t_{PHL}}$	Ratio of propagation delay times				0.3	3	
t_{PLH}	Propagation delay time, low-to-high-level output	A	Y	V_{CC} = 5.25 V to 5.95 V, R_L = 90 Ω, C_L = 50 pF, $V_{H(ref)}$ = 3.9 V See Figures 1 and 2		34	ns
t_{PHL}	Propagation delay time, high-to-low-level output					34	ns
t_{PLH}	Propagation delay time, low-to-high-level output	A	$\overline{F}$	V_{CC} = 5 V, R_L = 2 kΩ, C_L = 15 pF, See Figures 1 and 2		45	ns
t_{PHL}	Propagation delay time, high-to-low-level output					75	ns

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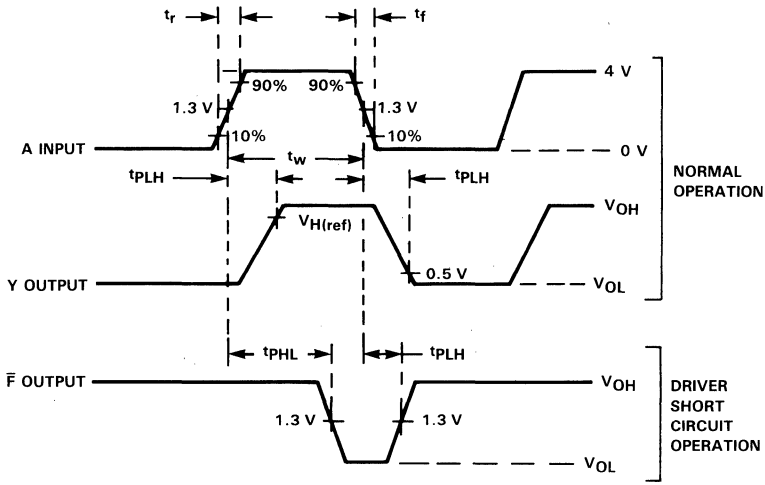
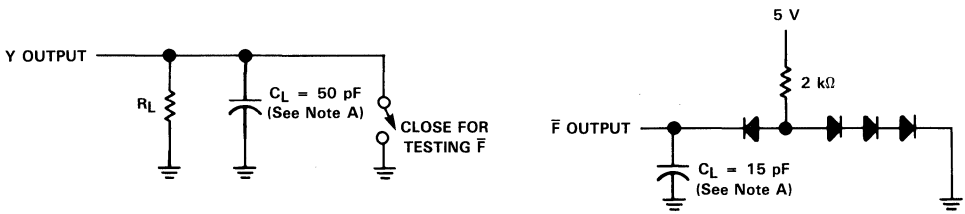
PARAMETER MEASUREMENT INFORMATION



NOTE A: The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_{out} = 50\ \Omega$.

FIGURE 1. INPUT AND OUTPUT VOLTAGE WAVEFORMS



NOTE A: C_L includes probe and stray capacitance.

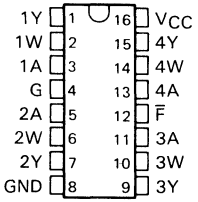
FIGURE 2. SWITCHING CHARACTERISTICS LOAD CIRCUITS

SN75ALS130
QUADRUPLE LINE DRIVER

D2299, FEBRUARY 1986

- **Meets IBM 360/370 I/O Interface Specification GA22-6974-3 (Also see SN75ALS126)**
- **Minimum Output Voltage of 3.11 V at I_{OH} = −60 mA**
- **Fault-Flag Circuit Output Signals Driver Output Fault**
- **Fault-Detection Current Limit Circuit Minimizes Power Dissipation During a Fault Condition**
- **Advanced Low-Power Schottky Circuitry**
- **Common Enable and Common Fault Flag**
- **Designed to be an Improved Replacement for the MC3485**

D, J, OR N PACKAGE
(TOP VIEW)



FUNCTION TABLE

INPUTS		OUTPUTS		
G†	A	Y	F̄†	W
L	X	L	H	H
X	L	L	H	H
H	H	H	H	L
H	H	S	L	H

H = high level, L = low level, X = irrelevant, S = shorted to ground

† G and F̄ are common to the four drivers. If any of the four Y outputs is shorted, the Fault-Flag will respond.

description

The SN75ALS130 quadruple line driver is designed to meet the IBM 360/370 I/O specifications GA22-6974-3. The output voltage is 3.11 volts minimum (at I_{OH} = −59.3 milliamperes) over the recommended ranges of supply voltage (4.5 volts to 5.5 volts) and temperature (0°C to 70°C). Driver outputs use a fault-detection current limit circuit to allow high drive current but still minimize power dissipation when the output is shorted to ground. The SN75ALS130 is compatible with standard TTL logic and supply voltages.

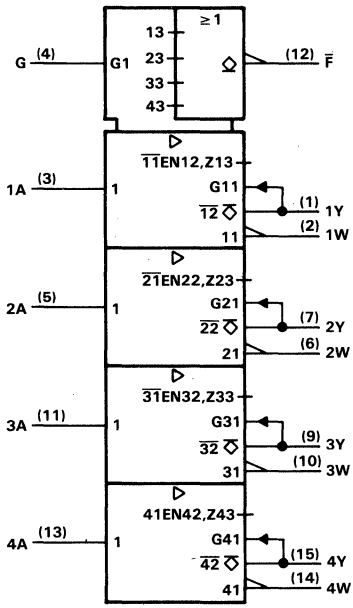
The SN75ALS130 employs the IMPACT™ process to achieve fast switching speeds and low power dissipation. Fault-flag circuitry is designed to sense and signal a line short on any Y line. Upon detecting an output fault condition, the fault-flag circuit forces the driver output into the off (low) state and signals a fault condition by causing the fault-flag output to go low.

The SN75ALS130 will drive a 50-ohm load as required in the IBM GA22-6974-3 specification or a 90-ohm load as used in many I/O systems. Optimum performance can be achieved when the device is used with either the SN75125, SN75127, SN75128, or SN75129 line receivers.

The SN75ALS130 is characterized for operation from 0°C to 70°C.

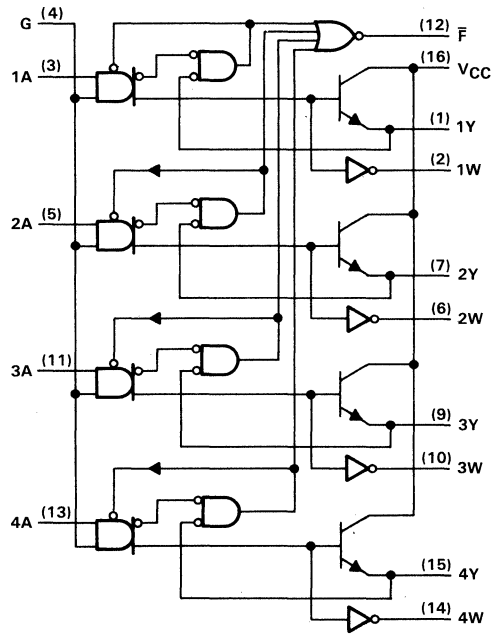
IMPACT is a trademark of Texas Instruments Incorporated

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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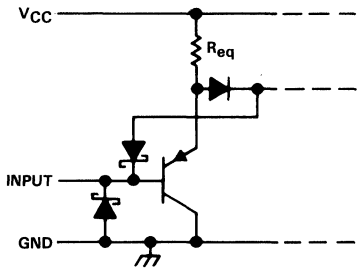
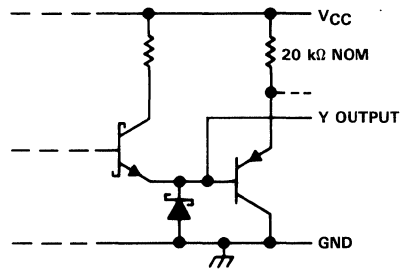
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT

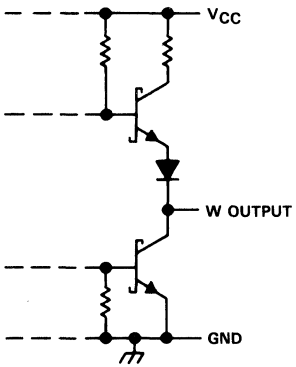


A Inputs: R_{eq} = 20 kΩ NOM
G Inputs: R_{eq} = 10 kΩ NOM

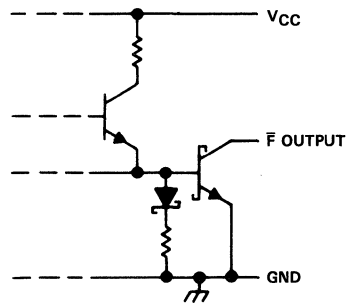
TYPICAL OF ALL Y OUTPUTS



TYPICAL OF ALL W OUTPUTS



TYPICAL OF $\overline{F}$ OUTPUT



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Continuous total dissipation at (or below)
25 °C free-air temperature (see Note 1): D package . . . . . 950 mW
J package . . . . . 1025 mW
N package . . . . . 1150 mW
Operating free-air temperature range . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N package . . . . . 260 °C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300 °C

NOTE 1: For operation above 25 °C free-air temperature, derate the D package to 608 mW at 70 °C at the rate of 7.6 mW/ °C, the J package to 656 mW at 70 °C at the rate of 8.2 mW/ °C, and the N package to 736 mW at 70 °C at the rate of 9.2 mW/ °C.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.95	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			−59.3	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature and supply voltage range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{IK}	Input clamp voltage	A,G	I_I = −18 mA		−1.5	V
V_{OH}	High-level output voltage	Y	V_{CC} = 4.5 V, I_{OH} = −59.3 mA, V_{IH} = 2 V	3.11		V
		Y	V_{CC} = 5.25 V, I_{OH} = −41 mA, V_{IH} = 2 V	3.9		
		W	V_{CC} = 4.5 V, I_{OH} = −400 μA, V_{IH} = 2 V	2.5		
V_{OL}	Low-level output voltage	Y	V_{CC} = 5.5 V, I_{OL} = −240 μA, V_{IL} = 0.8 V		0.15	V
		Y	V_{CC} = 5.95 V, I_{OL} = −1 mA, V_{IL} = 0.8 V		0.15	
		$\overline{F}$	V_{CC} = 4.5 V, I_{OL} = 8 mA, Y at 0 V		0.5	
		W	V_{CC} = 4.5 V, I_{OL} = 8 mA		0.5	
$I_{O(off)}$	Off-state output current	Y	V_{CC} = 4.5 V, V_{IL} = 0, V_O = 3.11 V		100	μA
		Y	V_{CC} = 0, V_{IL} = 0, V_O = 3.11 V		200	
I_{OH}	High-level output current	$\overline{F}$	V_{CC} = 5.95 V, V_{OH} = 5.95 V		100	μA
I_I	Input current	A	V_{CC} = 4.5 V, V_{IH} = 5.5 V		100	μA
		G			400	
I_{IH}	High-level input current	A	V_{CC} = 4.5 V, V_{IH} = 2.7 V		20	μA
		G			80	
I_{IL}	Low-level input current	A	V_{CC} = 5.95 V, V_{IL} = 0.4 V		250	μA
		G			−1000	
I_{OS}	Short-circuit output	Y	V_{CC} = 5.5 V, V_O = 0		−5	mA
		W		−15	−100	
		Y	V_{CC} = 5.95 V, V_O = 0		−5	
		W		−15	−110	
I_{CCH}	Supply current, all outputs high		V_{CC} = 5.5 V, No load		30	mA
			V_{CC} = 5.95 V, No load		32	
I_{CCL}	Supply current, Y outputs low		V_{CC} = 5.5 V, No load		45	mA
			V_{CC} = 5.95 V, No load		47	

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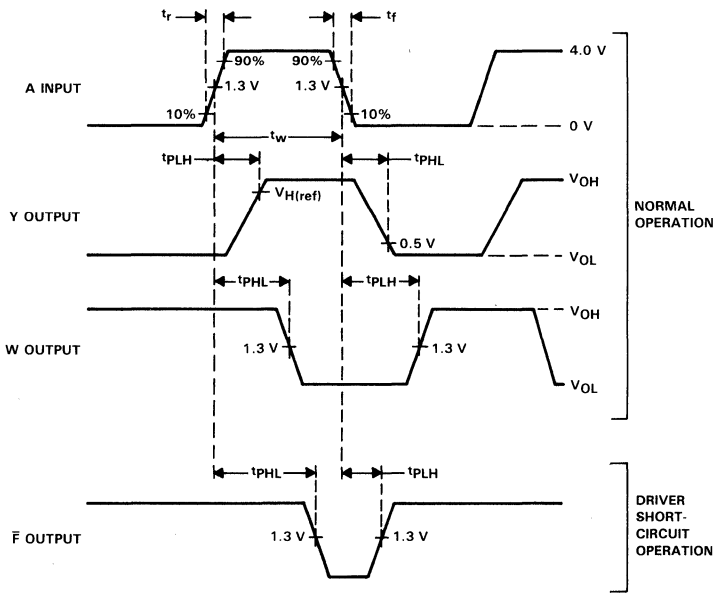
switching characteristics over recommended operating free-air temperature range

PARAMETER		FROM	TO	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	A	Y	V_{CC} = 4.5 V to 5.5 V, R_L = 50 Ω, C_L = 50 pF, $V_{H(ref)}$ = 3.11 V, Input f = 1 MHz See Figures 1 and 2		30	ns
t_{PHL}	Propagation delay time, high-to-low-level output					28	ns
$\frac{t_{PLH}}{t_{PHL}}$	Ratio of propagation delay times				0.3	3	
t_{PLH}	Propagation delay time, low-to-high-level output	A	Y	V_{CC} = 5.25 V to 5.95 V, R_L = 90 Ω, C_L = 50 pF, $V_{H(ref)}$ = 3.9 V, Input f = 5 MHz See Figures 1 and 2		34	ns
t_{PHL}	Propagation delay time, high-to-low-level output					34	ns
t_{PLH}	Propagation delay time, low-to-high-level output	A	W	V_{CC} = 5 V, R_L = 2 kΩ, C_L = 15 pF, See Figures 1 and 2		34	ns
t_{PHL}	Propagation delay time, high-to-low-level output					21	ns
t_{PLH}	Propagation delay time, low-to-high-level output	A	$\overline{F}$	V_{CC} = 5 V, R_L = 2 kΩ, C_L = 15 pF, See Figures 1 and 2		45	ns
t_{PHL}	Propagation delay time, high-to-low-level output					75	ns

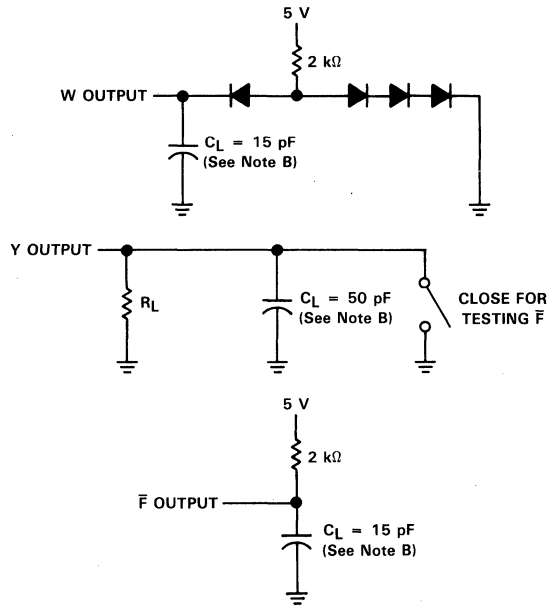
PARAMETER MEASUREMENT INFORMATION



NOTE A: The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r \leq 6$ ns, $t_f \leq 6$ ns, Z_{out} = 50 Ω.

FIGURE 1. INPUT AND OUTPUT VOLTAGE WAVEFORMS

PARAMETER MEASUREMENT INFORMATION



NOTE B: C_L includes probe and stray capacitance.

FIGURE 2. SWITCHING CHARACTERISTICS LOAD CIRCUITS

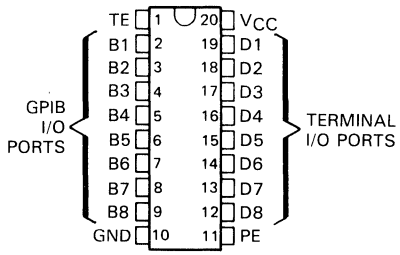
SN75ALS160
OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

D2525, JUNE 1986

MEETS IEEE STANDARD 488-1978 (GPIB)

- 8-Channel Bidirectional Transceiver
- High-Speed Advanced Low-Power Schottky Circuitry
- Low Power Dissipation . . . 46 mW Max per Channel
- Fast Propagation Times . . . 20 ns Max
- High-Impedance P-N-P Inputs
- Receiver Hysteresis . . . 650 mV Typ
- Open-Collector Driver Output Option
- No Loading of Bus When Device is Powered Down (V_{CC} = 0)
- Power-Up/Power-Down Protection (Glitch-Free)

DW, J, OR N PACKAGE
(TOP VIEW)



description

The SN75ALS160 eight-channel general-purpose interface bus transceiver is a monolithic, high-speed, Advanced Low-Power Schottky device designed for two-way data communications over single-ended transmission lines. It is designed to meet the requirements of IEEE Standard 488-1978. The transceiver features driver outputs that can be operated in either the passive-pullup or three-state mode. If Talk Enable (TE) is high, these ports have the characteristics of passive-pullup outputs when Pullup Enable (PE) is low, and of three-state outputs when PE is high. Taking TE low places these ports in the high-impedance state. The driver outputs are designed to handle loads up to 48 milliamperes of sink current.

An active turn-off feature has been incorporated into the bus-terminating resistors so that the device exhibits a high impedance to the bus when V_{CC} = 0. When combined with the SN75ALS161 or SN75ALS162 management bus transceiver, the pair provides the complete 16-wire interface for the IEEE 488 bus.

The SN75ALS160 is manufactured in a 20-pin package and is characterized for operation from 0°C to 70°C.

FUNCTION TABLES

EACH DRIVER

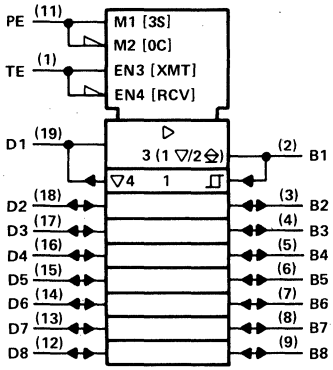
INPUTS			OUTPUT
D	TE	PE	B
H	H	H	H
L	H	X	L
H	X	L	Z†
X	L	X	Z†

EACH RECEIVER

INPUTS			OUTPUT
B	TE	PE	D
L	L	X	L
H	L	X	H
X	H	X	Z

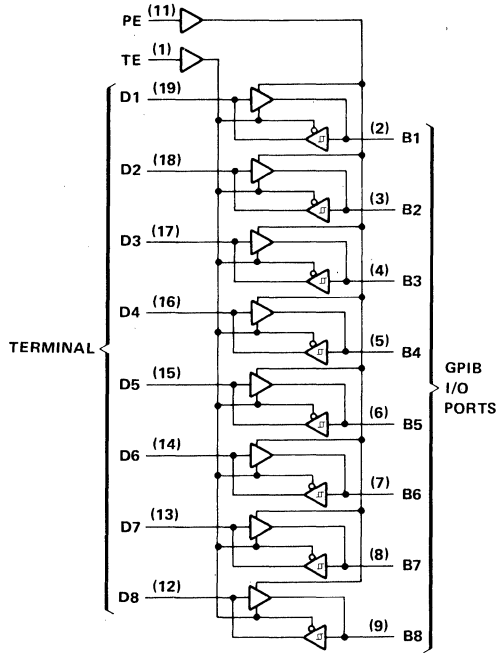
H = high level, L = low level, X = irrelevant,
Z = high-impedance state.
† This is the high-impedance state of a normal 3-state output modified by the internal resistors to V_{CC} and ground.

logic symbol†



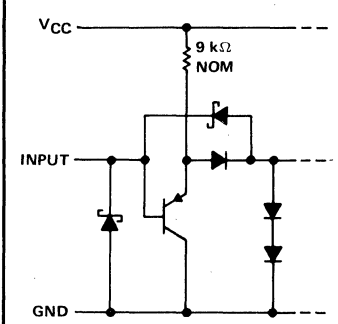
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
▽ Designates 3-state outputs.
⬙ Designates passive-pullup outputs.

logic diagram (positive logic)

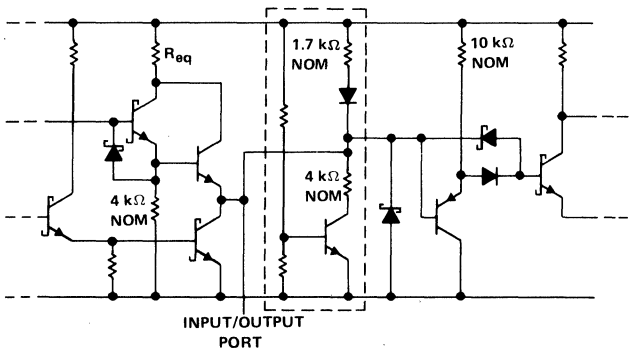


schematics of inputs and outputs

EQUIVALENT OF ALL CONTROL INPUTS



EQUIVALENT OF ALL INPUT/OUTPUT PORTS



Driver output R_{eq} = 30 Ω NOM
Receiver output R_{eq} = 110 Ω NOM
Circuit inside dashed lines is on the driver outputs only.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Low-level driver output current . . . . . 100 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2):
DW package . . . . . 1125 mW
J package . . . . . 1375 mW
N package . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds: DW or N package . . . . 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate the DW package to 720 mW at 70°C at the rate of 9.0 mW/°C, derate the J package to 880 mW at 70°C at the rate of 11.0 mW/°C, and derate the N package to 736 mW at 70°C at the rate of 9.2 mW/°C.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
High-level output current, I_{OH}	Bus ports with pullups active			−5.2	mA
	Terminal ports			−800	μA
Low-level output current, I_{OL}	Bus ports			48	mA
	Terminal ports			16	
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = −18 mA			−0.8	−1.5	V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)	Bus			0.4	0.65		V
V_{OH}‡	High-level output voltage	Terminal	I_{OH} = −800 μA,	TE at 0.8 V	2.7	3.5		V
		Bus	I_{OH} = −5.2 mA,	PE and TE at 2 V	2.5	3.3		
V_{OL}	Low-level output voltage	Terminal	I_{OL} = 16 mA,	TE at 0.8 V		0.3	0.5	V
		Bus	I_{OL} = 48 mA,	TE at 2 V		0.35	0.5	
I_I	Input current at maximum input voltage	Terminal	V_I = 5.5 V			0.2	100	μA
I_{IH}	High-level input current	Terminal,	V_I = 2.7 V			0.1	20	μA
I_{IL}	Low-level input current	PE, or TE	V_I = 0.5 V			−10	−100	μA
$V_{I/O(bus)}$	Voltage at bus port		Driver disabled	$I_{I(bus)}$ = 0	2.5	3.0	3.7	V
				$I_{I(bus)}$ = −12 mA			−1.5	
$I_{I/O(bus)}$	Current into bus port	Power on	Driver disabled	$V_{I(bus)}$ = −1.5 V to 0.4 V	−1.3			mA
				$V_{I(bus)}$ = 0.4 V to 2.5 V	0		−3.2	
				$V_{I(bus)}$ = 2.5 V to 3.7 V			+2.5	
							−3.2	
				$V_{I(bus)}$ = 3.7 V to 5 V	0		2.5	
				$V_{I(bus)}$ = 5 V to 5.5 V	0.7		2.5	
		Power off	V_{CC} = 0,	$V_{I(bus)}$ = 0 V to 2.5 V			−40	μA
I_{OS}	Short-circuit output current	Terminal			−15	−35	−75	mA
		Bus			−25	−50	−125	
I_{CC}	Supply current		No load	Terminal outputs low and enabled		42	56	mA
				Bus outputs low and enabled		52	70	
$C_{i/o(bus)}$	Bus-port capacitance		V_{CC} = 5 V to 0 V, $V_{I/O}$ = 0 to 2 V, f = 1 MHz			30		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ V_{OH} applies to three-state outputs only.

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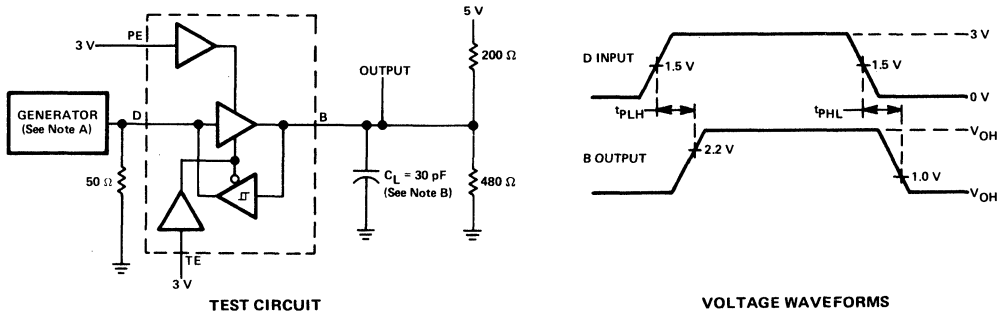
switching characteristics over recommended range of operating free-air temperature (unless otherwise noted), V_{CC} = 5 V

PARAMETER		FROM	TO	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Terminal	Bus	C_L = 30 pF, See Figure 1		10	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					12	20	
t_{PLH}	Propagation delay time, low-to-high-level output	Bus	Terminal	C_L = 30 pF, See Figure 2		5	10	ns
t_{PHL}	Propagation delay time, high-to-low-level output					7	14	
t_{PZH}	Output enable time to high level	TE	Bus	C_L = 15 pF, See Figure 3		11	20	ns
t_{PHZ}	Output disable time from high level					3	10	
t_{PZL}	Output enable time to low level					18	35	
t_{PLZ}	Output disable time from low level					5	20	
t_{PZH}	Output enable time to high level	TE	Terminal	C_L = 15 pF, See Figure 4		5	20	ns
t_{PHZ}	Output disable time from high level					8	20	
t_{PZL}	Output enable time to low level					9	20	
t_{PLZ}	Output disable time from low level					8	20	
t_{en}	Output pull-up enable time	PE	Bus	C_L = 15 pF, See Figure 5		3	10	ns
t_{dis}	Output pull-up disable time					4	12	

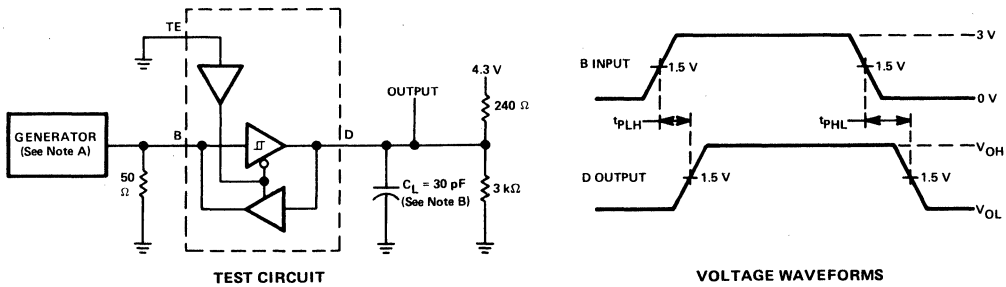
†Typical values are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION



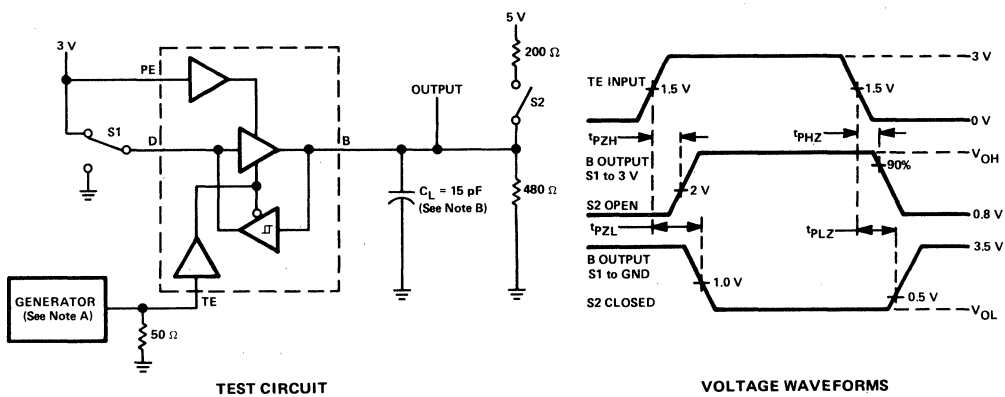
TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 1. TERMINAL-TO-BUS PROPAGATION DELAY TIMES



TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 2. BUS-TO-TERMINAL PROPAGATION DELAY TIMES



TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 3. TE-TO-BUS ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤6 ns, t_f ≤6 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

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PARAMETER MEASUREMENT INFORMATION

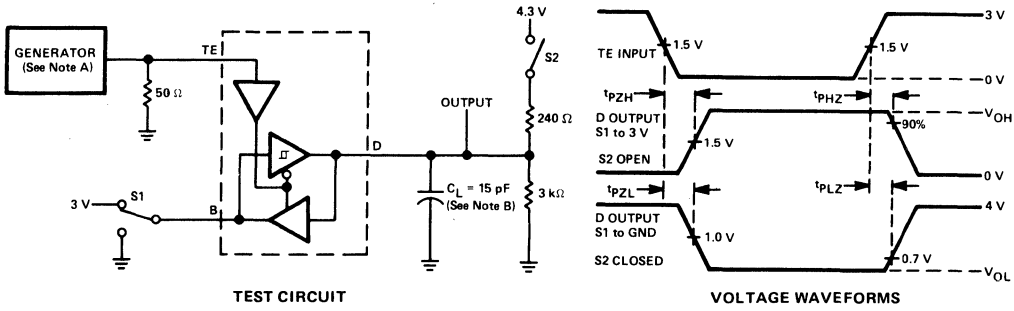

FIGURE 4. TE-TO-TERMINAL ENABLE AND DISABLE TIMES

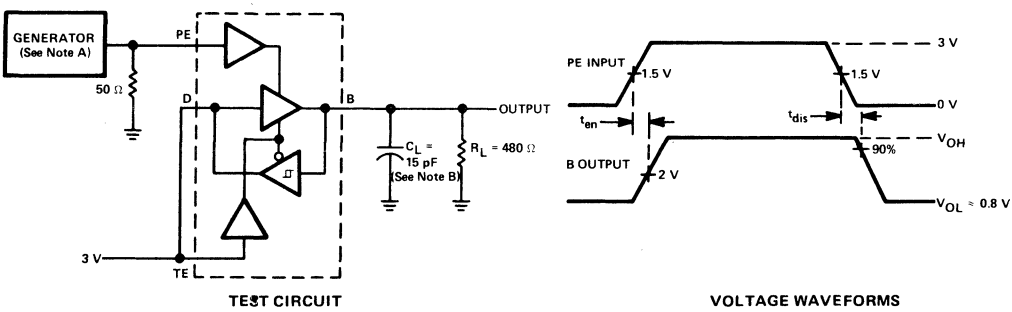

FIGURE 5. PE-TO-BUS PULLUP ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

TERMINAL HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

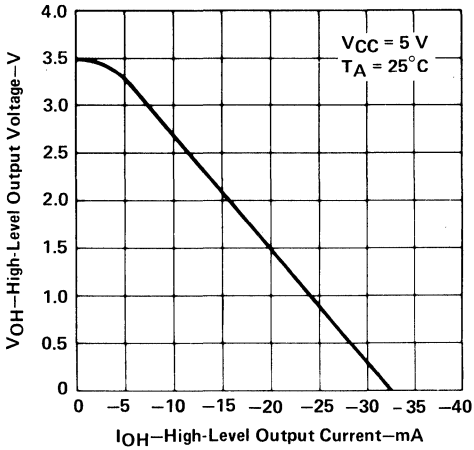

FIGURE 6

TERMINAL LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

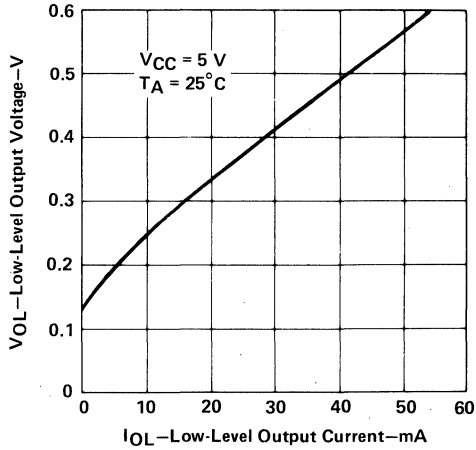

FIGURE 7

TERMINAL OUTPUT VOLTAGE
vs
BUS INPUT VOLTAGE

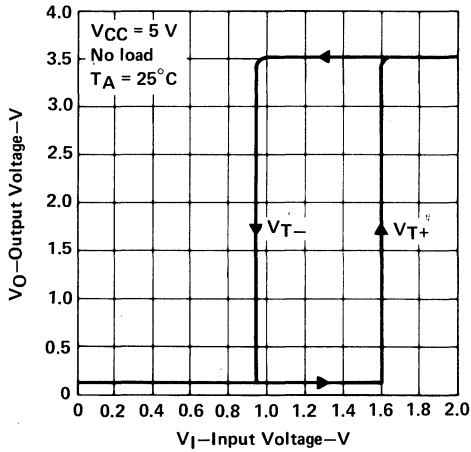

FIGURE 8

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TYPICAL CHARACTERISTICS

BUS HIGH-LEVEL OUTPUT VOLTAGE
vs
BUS HIGH-LEVEL OUTPUT CURRENT

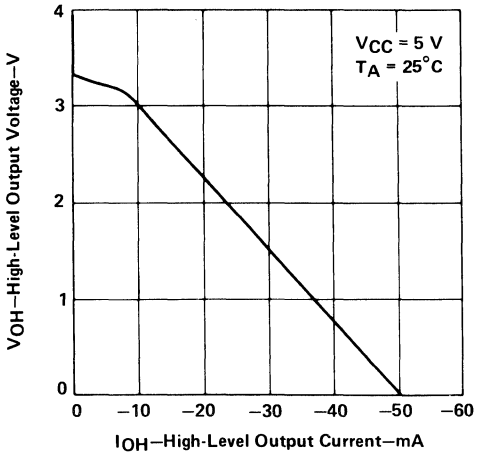


FIGURE 9

BUS LOW-LEVEL OUTPUT VOLTAGE
vs
BUS LOW-LEVEL OUTPUT CURRENT

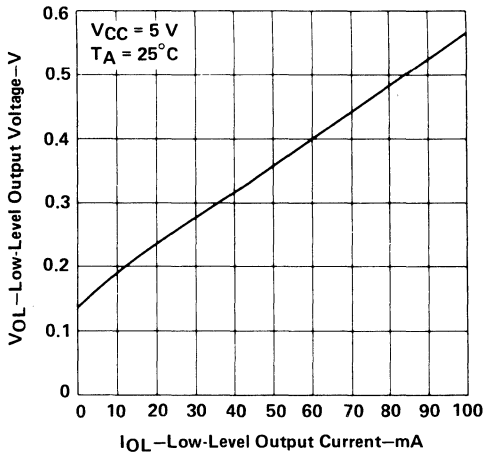


FIGURE 10

BUS OUTPUT VOLTAGE
vs
TERMINAL INPUT VOLTAGE

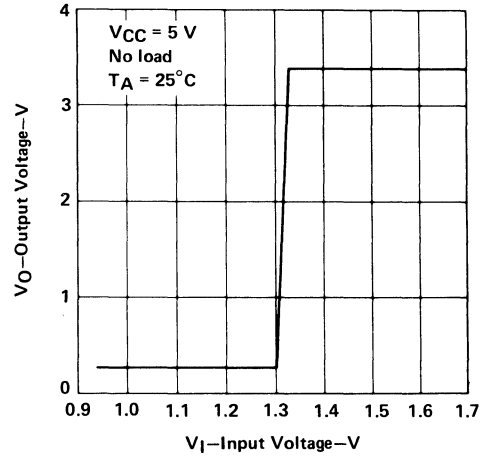


FIGURE 11

BUS CURRENT
vs
BUS VOLTAGE

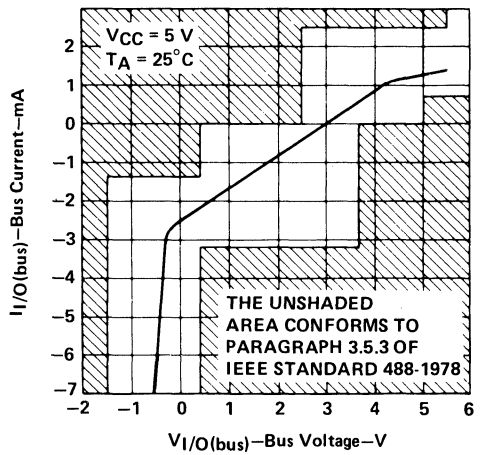


FIGURE 12

3 Interface ALS Circuits

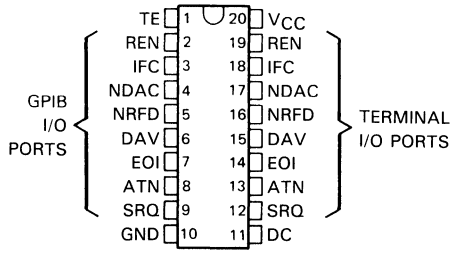
SN75ALS161
OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

D2618, JUNE 1986

MEETS IEEE STANDARD 488-1978 (GPIB)

- 8-Channel Bidirectional Transceiver
- Designed to Implement Control Bus Interface
- Designed for Single Controller
- High-Speed Advanced Low-Power Schottky Circuitry
- Low Power Dissipation . . . 46 mW Max per Channel
- Fast Propagation Times . . . 20 ns Max
- High-Impedance P-N-P Inputs
- Receiver Hysteresis . . . 650 mV Typ
- Bus-Terminating Resistors Provided on Driver Outputs
- No Loading of Bus When Device is Powered Down (V_{CC} = 0)
- Power-Up/Power-Down Protection (Glitch-Free)

DW, J, OR N PACKAGE
(TOP VIEW)



CHANNEL IDENTIFICATION TABLE

NAME	IDENTITY	CLASS
DC	Direction Control	Control
TE	Talk Enable	
ATN	Attention	Bus Management
SRQ	Service Request	
REN	Remote Enable	
IFC	Interface Clear	
EOI	End or Identify	
DAV	Data Valid	Data Transfer
NDAC	Not Data Accepted	
NRFD	Not Ready for Data	

description

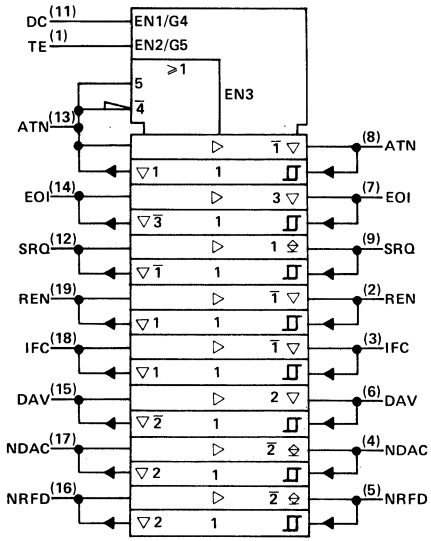
The SN75ALS161 eight-channel general-purpose interface bus transceiver is a monolithic, high-speed, Advanced Low-Power Schottky process device designed to provide the bus-management and data-transfer signals between operating units of a single controller instrumentation system. When combined with the SN75ALS160 octal bus transceiver, the SN75ALS161 provides the complete 16-wire interface for the IEEE 488 bus.

The SN75ALS161 features eight driver-receiver pairs connected in a front-to-back configuration to form input/output (I/O) ports at both the bus and terminal sides. The direction of data through these driver-receiver pairs is determined by the DC and TE enable signals.

The driver outputs (GPIB I/O ports) feature active bus-terminating resistor circuits designed to provide a high impedance to the bus when V_{CC} = 0. The drivers are designed to handle loads up to 48 milliamperes of sink current. Each receiver features p-n-p transistor inputs for high input impedance and a guaranteed hysteresis of 400 millivolts minimum for increased noise immunity. All receivers have 3-state outputs to present a high impedance to the terminal when disabled.

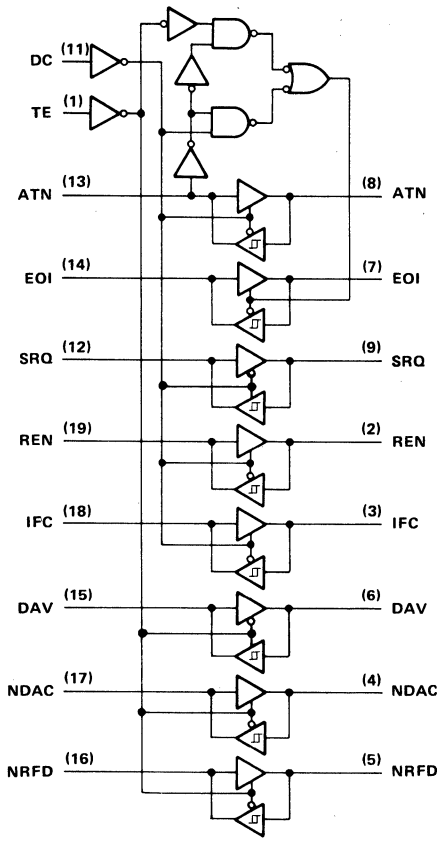
The SN75ALS161 is manufactured in a 20-pin package and is characterized for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
▽ Designates 3-state outputs.
⏀ Designates passive-pullup outputs.

logic diagram (positive logic)



RECEIVE/TRANSMIT FUNCTION TABLE

CONTROLS			BUS-MANAGEMENT CHANNELS					DATA-TRANSFER CHANNELS		
DC	TE	ATN†	ATN†	SRQ (Controlled by DC)	REN (Controlled by DC)	IFC (Controlled by DC)	EOI	DAV (Controlled by TE)	NDAC (Controlled by TE)	NRFD (Controlled by TE)
H	H	H	R	T	R	R	T	T	R	R
H	H	L					R			
L	L	H	T	R	T	T	R	R	T	T
L	L	L					T			
H	L	X	R	T	R	R	R	R	T	T
L	H	X	T	R	T	T	T	T	R	R

H = high level, L = low level, R = receive, T = transmit, X = irrelevant
Direction of data transmission is from the terminal side to the bus side, and the direction of data receiving is from the bus side to the terminal side. Data transfer is noninverting in both directions.
†ATN is a normal transceiver channel that functions additionally as an internal direction control or talk enable for EOI whenever the DC and TE inputs are in the same state. When DC and TE are in opposite states, the ATN channel functions as an independent transceiver only.

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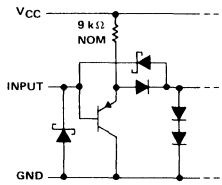
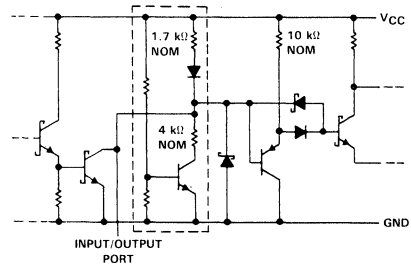
schematics of inputs and outputs

EQUIVALENT OF ALL CONTROL INPUTS

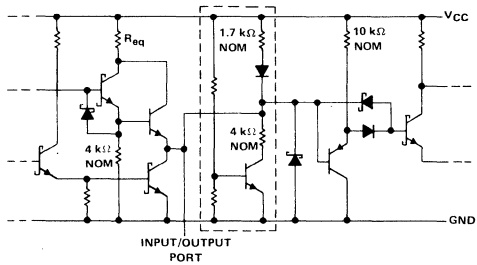


TYPICAL OF SRQ, NDAC, and NRFD GPIB I/O PORT



Circuit inside dashed lines is on the driver outputs only.

TYPICAL OF ALL I/O PORTS EXCEPT SRQ, NDAC, and NRFD GPIB I/O PORTS



Driver output R_{eq} = 30 Ω NOM
Receiver output R_{eq} = 110 Ω NOM
Circuit inside dashed lines is on the driver outputs only.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Low-level driver output current . . . . . 100 mA
Continuous total dissipation at (or below) 25 °C free-air temperature (see Note 2):
DW package . . . . . 1125 mW
J package . . . . . 1375 mW
N package . . . . . 1150 mW
Operating free-air temperature range . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C
Lead temperature 1,6 mm (1/16 inch) from the case for 60 seconds: J package . . . . . 300 °C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds: DW or N package . . . . 260 °C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 25 °C free-air temperature, derate the DW package to 720 mW at 70 °C at the rate of 9.0 mW/°C, derate the J package to 880 mW at 70 °C at the rate of 11.0 mW/°C, and derate the N package to 736 mW at 70 °C at the rate of 9.2 mW/°C.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
High-level output current, I_{OH}	Bus ports with pullups active			−5.2	mA
	Terminal ports			−800	μA
Low-level output current, I_{OL}	Bus ports			48	mA
	Terminal ports			16	
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = −18 mA			−0.8	−1.5	V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)	Bus			0.4	0.65		V
V_{OH}‡	High-level output voltage	Terminal	I_{OH} = −800 μA		2.7	3.5		V
		Bus	I_{OH} = −5.2 mA		2.5	3.3		
V_{OL}	Low-level output voltage	Terminal	I_{OL} = 16 mA			0.3	0.5	V
		Bus	I_{OL} = 48 mA			0.35	0.5	
I_I	Input current at maximum input voltage	Terminal	V_I = 5.5 V			0.2	100	μA
I_{IH}	High-level input current	Terminal and control inputs	V_I = 2.7 V			0.1	20	μA
I_{IL}	Low-level input current		V_I = 0.5 V			−10	−100	μA
$V_{I/O(bus)}$	Voltage at bus port		Driver disabled	$I_{I(bus)}$ = 0	2.5	3.0	3.7	V
				$I_{I(bus)}$ = −12 mA			−1.5	
$I_{I/O(bus)}$	Current into bus port	Power on	Driver disabled	$V_{I(bus)}$ = −1.5 V to 0.4 V	−1.3			mA
				$V_{I(bus)}$ = 0.4 V to 2.5 V	0		−3.2	
				$V_{I(bus)}$ = 2.5 V to 3.7 V			+2.5 −3.2	
				$V_{I(bus)}$ = 3.7 V to 5 V	0		2.5	
				$V_{I(bus)}$ = 5 V to 5.5 V	0.7		2.5	
		Power off	V_{CC} = 0,	$V_{I(bus)}$ = 0 V to 2.5 V			−40	μA
I_{OS}	Short-circuit output current	Terminal			−15	−35	−75	mA
		Bus			−25	−50	−125	
I_{CC}	Supply current		No load, TE and DC low			55	75	mA
$C_{i/o(bus)}$	Bus-port capacitance		V_{CC} = 5 V to 0 V, $V_{I/O}$ = 0 to 2 V, f = 1 MHz			30		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ V_{OH} applies for three-state outputs only.

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switching characteristics over recommended range of operating free-air temperature (unless otherwise noted), V_{CC} = 5 V

PARAMETER		FROM	TO	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Terminal	Bus	C_L = 30 pF, See Figure 1		10	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					12	20	
t_{PLH}	Propagation delay time, low-to-high-level output	Bus	Terminal	C_L = 30 pF, See Figure 2		5	10	ns
t_{PHL}	Propagation delay time, high-to-low-level output					7	14	
t_{PZH}	Output enable time to high level	TE or DC	BUS (ATTN, EOI, REN, IFC, and DAV)	C_L = 15 pF, See Figure 3			30	ns
t_{PHZ}	Output disable time from high level						20	
t_{PZL}	Output enable time to low level						45	
t_{PLZ}	Output disable time from low level						20	
t_{PZH}	Output enable time to high level	TE or DC	Terminal	C_L = 15 pF, See Figure 4			20	ns
t_{PHZ}	Output disable time from high level						25	
t_{PZL}	Output enable time to low level						30	
t_{PLZ}	Output disable time from low level						25	

†All typical values are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

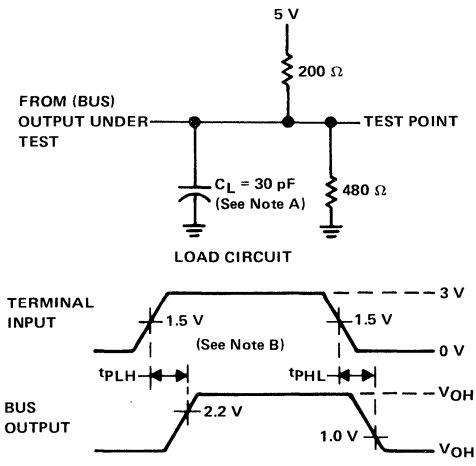


FIGURE 1. TERMINAL-TO-BUS PROPAGATION DELAY TIMES

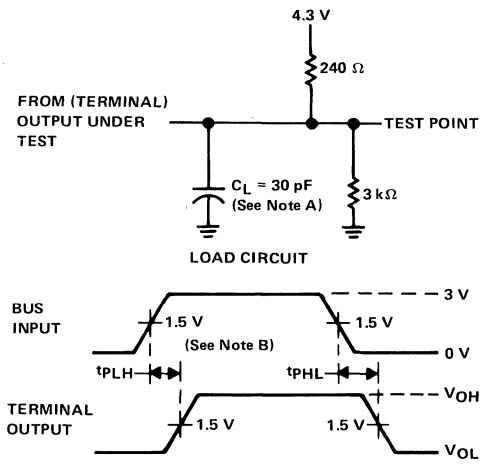
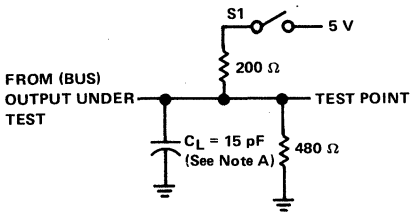


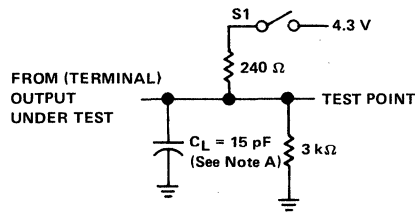
FIGURE 2. BUS-TO-TERMINAL PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤6 ns, t_f ≤6 ns, Z_{out} = 50 Ω.

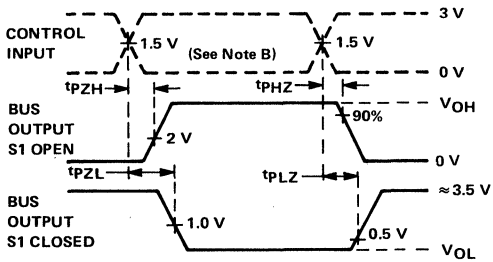
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

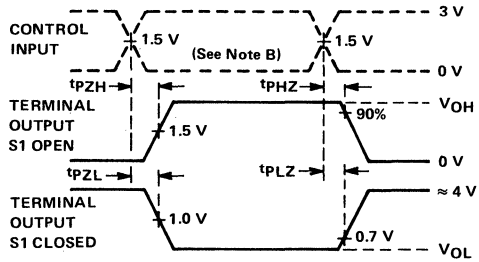


LOAD CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 3. BUS ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORMS

FIGURE 4. TERMINAL ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤6 ns, t_f ≤6 ns, Z_{out} = 50 Ω.

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TYPICAL CHARACTERISTICS

TERMINAL HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

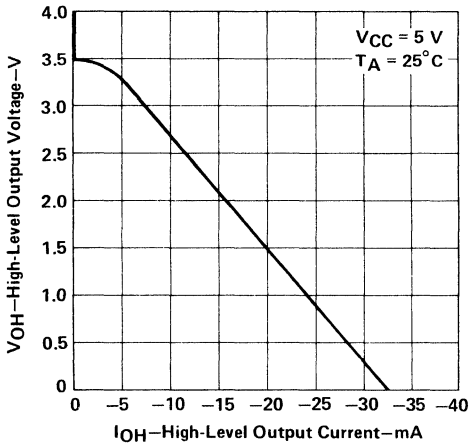


FIGURE 5

TERMINAL LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

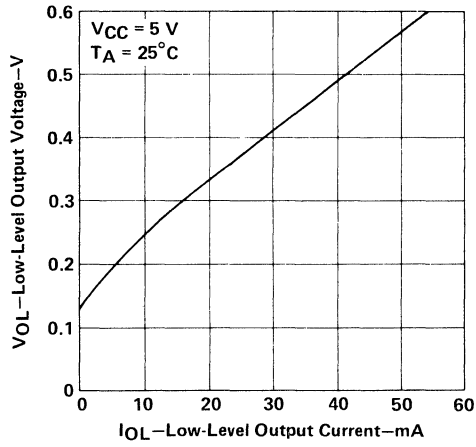


FIGURE 6

TERMINAL OUTPUT VOLTAGE
vs
BUS INPUT VOLTAGE

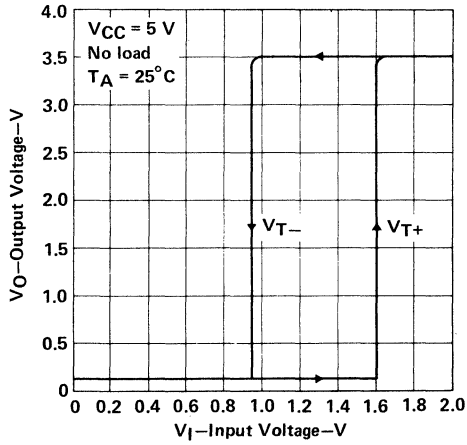


FIGURE 7

TYPICAL CHARACTERISTICS

BUS HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

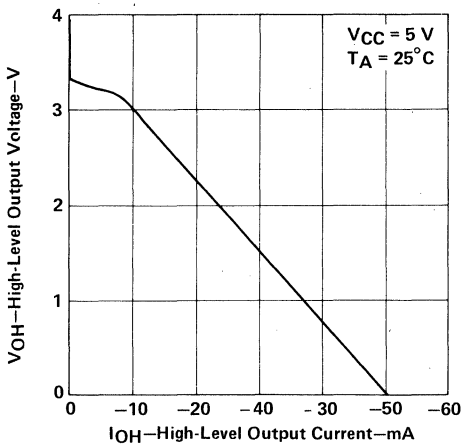


FIGURE 8

BUS-LOW LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

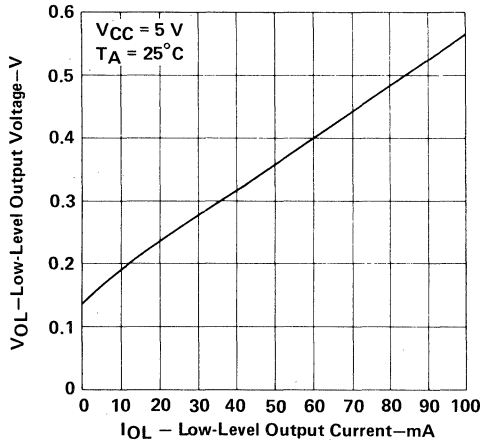


FIGURE 9

BUS OUTPUT VOLTAGE
vs
TERMINAL INPUT VOLTAGE

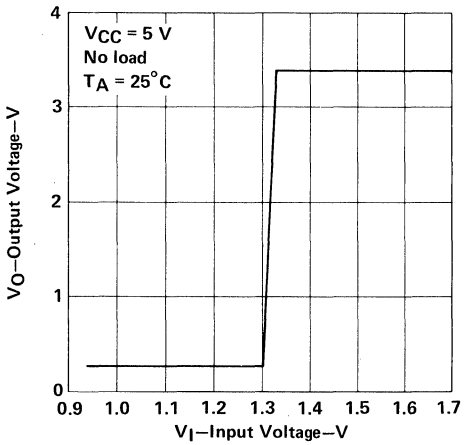


FIGURE 10

BUS CURRENT
vs
BUS VOLTAGE

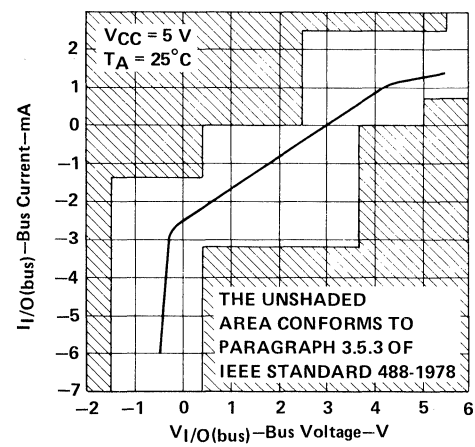


FIGURE 11

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

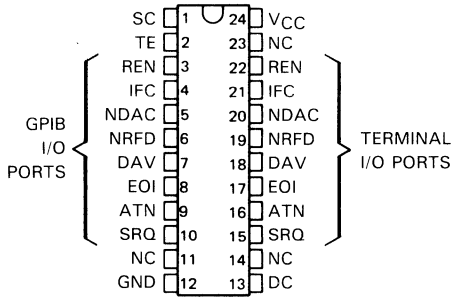
SN75ALS162
OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

D2618, JUNE 1986

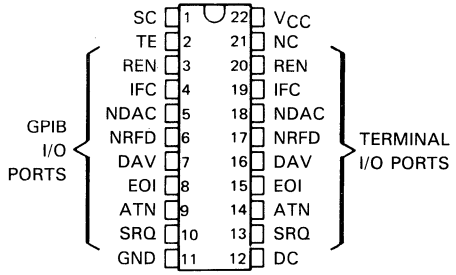
MEETS IEEE STANDARD 488-1978 (GPIB)

- 8-Channel Bidirectional Transceiver
- Designed to Implement Control Bus Interface
- Designed for Multicontrollers
- High-Speed Advanced Low-Power Schottky Circuitry
- Low Power Dissipation . . . 46 mW Max per Channel
- Fast Propagation Times . . . 20 ns Max
- High-Impedance P-N-P Inputs
- Receiver Hysteresis . . . 650 mV Typ
- Bus-Terminating Resistors Provided on Driver Outputs
- No Loading of Bus When Device is Powered Down (V_{CC} = 0)
- Power-Up/Power-Down Protection (Glitch-Free)

DW PACKAGE
(TOP VIEW)



N DUAL-IN-LINE PACKAGE
(TOP VIEW)



NC—No internal connection.

description

The SN75ALS162 eight-channel general-purpose interface bus transceiver is a monolithic, high-speed, Advanced Low-Power Schottky process device designed to provide the bus-management and data-transfer signals between operating units of a multiple-controller instrumentation system. When combined with the SN75ALS160 octal bus transceiver, the SN75ALS162 provides the complete 16-wire interface for the IEEE 488 bus.

The SN75ALS162 features eight driver-receiver pairs connected in a front-to-back configuration to form input/output (I/O) ports at both the bus and terminal sides. The direction of data through these driver-receiver pairs is determined by the DC, TE, and SC enable signals. The SC input allows the REN and IFC transceivers to be controlled independently.

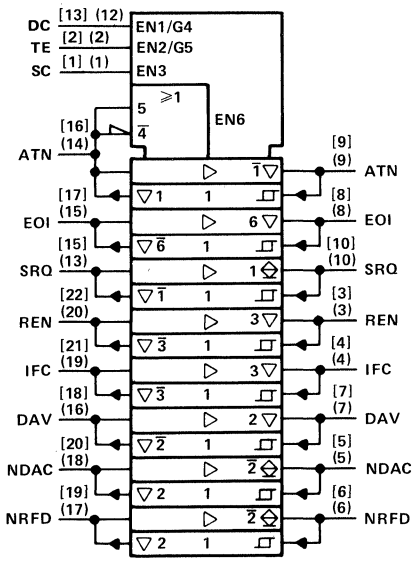
The driver outputs (GPIB I/O ports) feature active bus-terminating resistor circuits designed to provide a high impedance to the bus when V_{CC} = 0. The drivers are designed to handle loads up to 48 milliamperes of sink current. Each receiver features p-n-p transistor inputs for high input impedance and a guaranteed hysteresis of 400 millivolts minimum for increased noise immunity. All receivers have 3-state outputs to present a high impedance to the terminal when disabled.

The SN75ALS162 is manufactured in a 22-pin dual-in-line N package and in 24-pin DW package, and is characterized for operation from 0°C to 70°C.

CHANNEL IDENTIFICATION TABLE

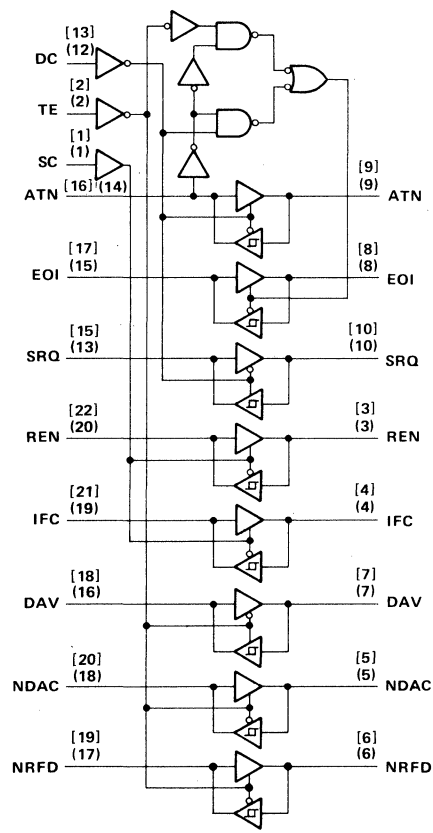
NAME	IDENTITY	CLASS
DC	Direction Control	Control
TE	Talk Enable	
SC	System Control	
ATN	Attention	Bus Management
SRQ	Service Request	
REN	Remote Enable	
IFC	Interface Clear	
EOI	End or Identify	
DAV	Data Valid	Data Transfer
NDAC	Not Data Accepted	
NRFD	Not Ready for Data	

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
▽ Designates 3-state outputs.
⏀ Designates passive-pullup outputs.

logic diagram (positive logic)



[ ] Denotes pin numbers for DW package.
( ) Denotes pin numbers for N package.

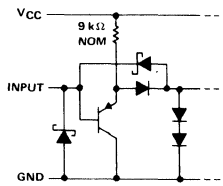
RECEIVE/TRANSMIT FUNCTION TABLE

CONTROLS				BUS-MANAGEMENT CHANNELS				DATA-TRANSFER CHANNELS		
SC	DC	TE	ATN†	ATN† (Controlled by DC)	SRQ (Controlled by DC)	REN (Controlled by SC)	IFC (Controlled by SC)	EOI	DAV (Controlled by TE)	NDAC (Controlled by TE)	NRFD (Controlled by TE)
	H	H	H	R	T			T	T	R	R
	H	H	L					R			
	L	L	H	T	R			R	R	T	T
	L	L	L					T			
	H	L	X	R	T			R	R	T	T
	L	H	X	T	R			T	T	R	R
H						T	T				
L						R	R				

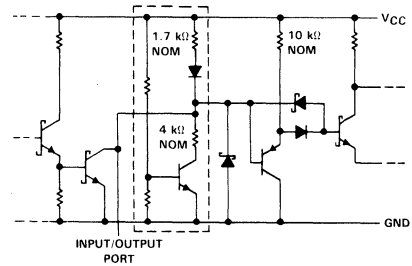
H = high level, L = low level, R = receive, T = transmit, X = irrelevant
Direction of data transmission is from the terminal side to the bus side, and the direction of data receiving is from the bus side to the terminal side. Data transfer is noninverting in both directions.
†ATN is a normal transceiver channel that functions additionally as an internal direction control or talk enable for EOI whenever the DC and TE inputs are in the same state. When DC and TE are in opposite states, the ATN channel functions as an independent transceiver only.

schematics of inputs and outputs

EQUIVALENT OF ALL CONTROL INPUTS

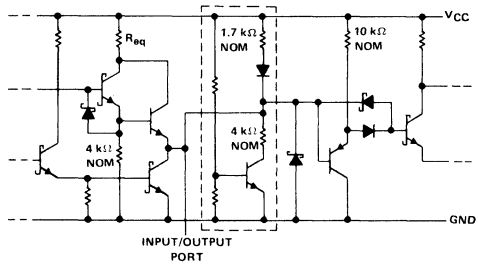


TYPICAL OF SRQ, NDAC, and NRFD GPIB I/O PORT



Circuit inside dashed lines is on the driver outputs only.

TYPICAL OF ALL I/O PORTS EXCEPT SRQ, NDAC, and NRFD GPIB I/O PORTS



Driver output R_{eq} = 30 Ω NOM
Receiver output R_{eq} = 110 Ω NOM
Circuit inside dashed lines is on the driver outputs only.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Low-level driver output current . . . . . 100 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2):
DW package . . . . . 1350 mW
N package . . . . . 1700 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds: DW or N package . . . . . 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate the DW package to 864 mW at 70°C at the rate of 10.8 mW/°C, and derate the N package to 1088 mW at 70°C at the rate of 13.6 mW/°C.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
High-level output current, I_{OH}	Bus ports with 3-state outputs			−5.2	mA
	Terminal ports			−800	μA
Low-level output current, I_{OL}	Bus ports			48	mA
	Terminal ports			16	
Operating free-air temperature, T_A		0		70	°C

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = −18 mA			−0.8	−1.5	V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)	Bus			0.4	0.65		V
V_{OH}‡	High-level output voltage	Terminal	I_{OH} = −800 μA		2.7	3.5		V
		Bus	I_{OH} = −5.2 mA		2.5	3.3		
V_{OL}	Low-level output voltage	Terminal	I_{OL} = 16 mA			0.3	0.5	V
		Bus	I_{OL} = 48 mA			0.35	0.5	
I_I	Input current at maximum input voltage	Terminal	V_I = 5.5 V			0.2	100	μA
I_{IH}	High-level input current	Terminal and control inputs	V_I = 2.7 V			0.1	20	μA
I_{IL}	Low-level input current		V_I = 0.5 V			−10	−100	μA
$V_{I/O(bus)}$	Voltage at bus port		Driver disabled	$I_{I(bus)}$ = 0	2.5	3.0	3.7	V
				$I_{I(bus)}$ = −12 mA			−1.5	
$I_{I/O(bus)}$	Current into bus port	Power on	Driver disabled	$V_{I(bus)}$ = −1.5 V to 0.4 V	−1.3			mA
				$V_{I(bus)}$ = 0.4 V to 2.5 V	0		−3.2	
				$V_{I(bus)}$ = 2.5 V to 3.7 V			+2.5	
							−3.2	
				$V_{I(bus)}$ = 3.7 V to 5 V	0		2.5	
				$V_{I(bus)}$ = 5 V to 5.5 V	0.7		2.5	
		Power off	V_{CC} = 0,	$V_{I(bus)}$ = 0 V to 2.5 V			−40	μA
I_{OS}	Short-circuit output current	Terminal			−15	−35	−75	mA
		Bus			−25	−50	−125	
I_{CC}	Supply current		No load,	TE, DC, and SC low		55	75	mA
$C_{i/o(bus)}$	Bus-port capacitance		V_{CC} = 5 V to 0 V, $V_{I/O}$ = 0 to 2 V, f = 1 MHz			30		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ V_{OH} applies for three-state outputs only.

switching characteristics over recommended range of operating free-air temperature (unless otherwise noted), V_{CC} = 5 V

PARAMETER		FROM	TO	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Terminal	Bus	C_L = 30 pF, See Figure 1		10	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					12	20	
t_{PLH}	Propagation delay time, low-to-high-level output	Bus	Terminal	C_L = 30 pF, See Figure 2		5	10	ns
t_{PHL}	Propagation delay time, high-to-low-level output					7	14	
t_{PZH}	Output enable time to high level	TE, DC, or SC	BUS (ATTN, EOI, REN, IFC, and DAV)	C_L = 15 pF, See Figure 3			30	ns
t_{PHZ}	Output disable time from high level						20	
t_{PZL}	Output enable time to low level						45	
t_{PLZ}	Output disable time from low level						20	
t_{PZH}	Output enable time to high level	TE, DC, or SC	Terminal	C_L = 15 pF, See Figure 4			20	ns
t_{PHZ}	Output disable time from high level						25	
t_{PZL}	Output enable time to low level						30	
t_{PLZ}	Output disable time from low level						25	

†All typical values are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

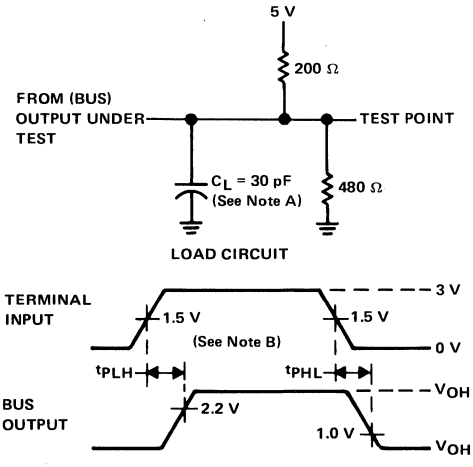

FIGURE 1. TERMINAL-TO-BUS PROPAGATION DELAY TIMES

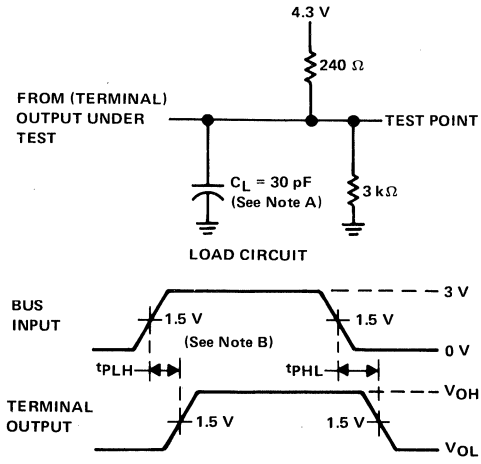

FIGURE 2. BUS-TO-TERMINAL PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤6 ns, t_f ≤6 ns, Z_{out} = 50 Ω.

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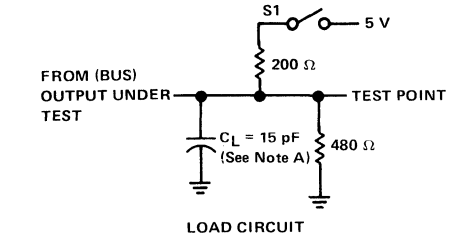
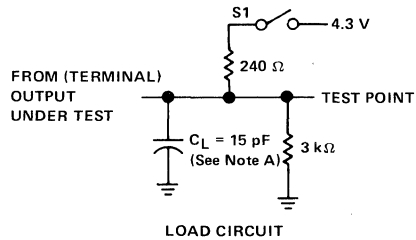
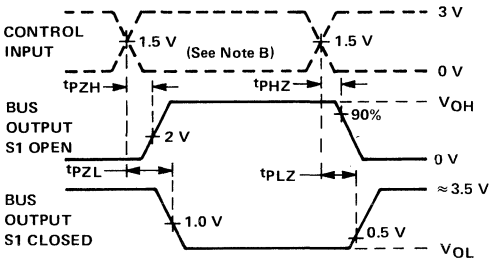
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

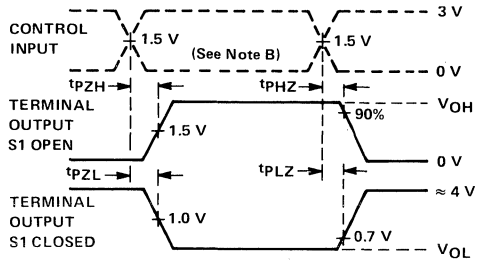


LOAD CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 3. BUS ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORMS

FIGURE 4. TERMINAL ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤6 ns, t_f ≤6 ns, Z_{out} = 50 Ω.

TYPICAL CHARACTERISTICS

TERMINAL HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

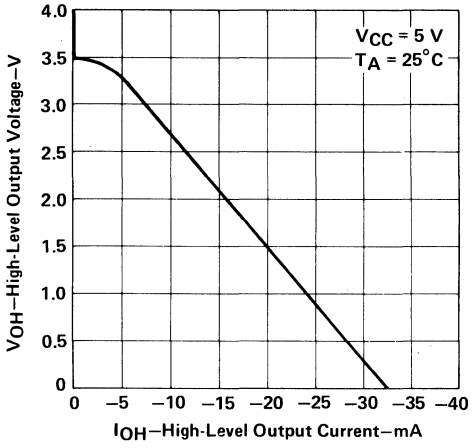


FIGURE 5

TERMINAL LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

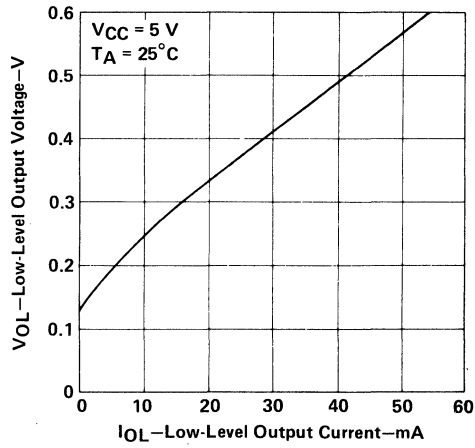


FIGURE 6

TERMINAL OUTPUT VOLTAGE
vs
BUS INPUT VOLTAGE

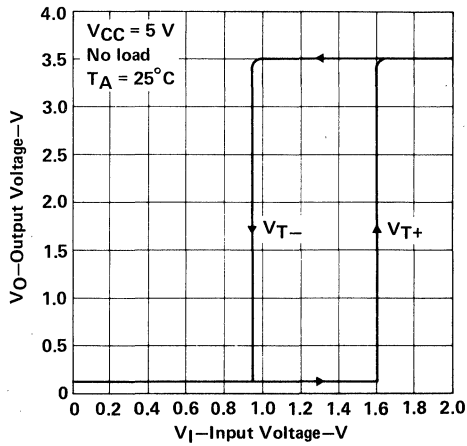


FIGURE 7

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TYPICAL CHARACTERISTICS

BUS HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

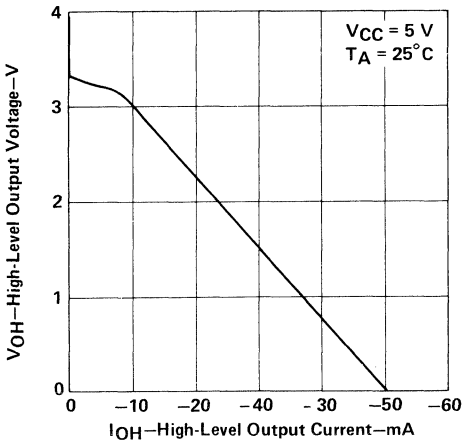


FIGURE 8

BUS-LOW LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

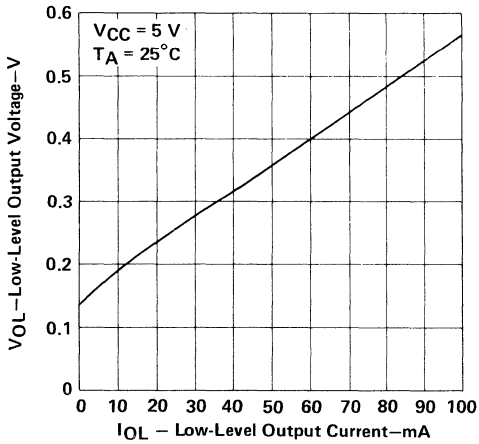


FIGURE 9

BUS OUTPUT VOLTAGE
vs
TERMINAL INPUT VOLTAGE

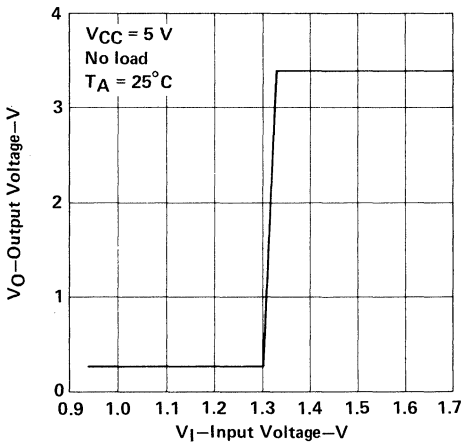


FIGURE 10

BUS CURRENT
vs
BUS VOLTAGE

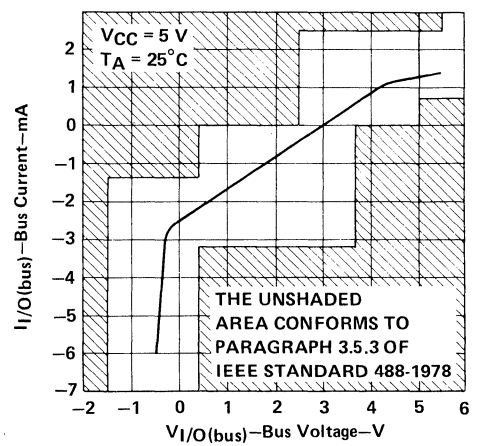


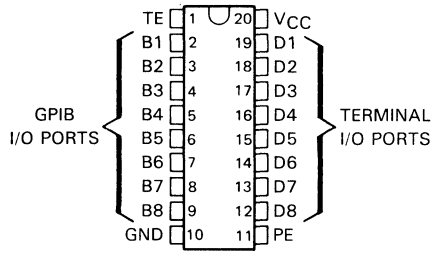
FIGURE 11

SN75ALS163
OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

D2611, JUNE 1986

- 8-Channel Bidirectional Transceivers
- High-Speed Advanced Low-Power Schottky Circuitry
- Low Power Dissipation . . . 46 mW Max per Channel
- Fast Propagation Times . . . 20 ns Max
- High-Impedance P-N-P Inputs
- Receiver Hysteresis . . . 650 mV Typ
- Open-Collector Driver Output Option
- No Loading of Bus When Device is Powered Down (V_{CC} = 0)
- Power-Up/Power-Down Protection (Glitch-Free)

DW, J, OR N PACKAGE
(TOP VIEW)



description

The SN75ALS163 octal general-purpose interface bus transceiver is a monolithic, high-speed, Advanced Low-Power Schottky device. It is designed for two-way data communications over single-ended transmission lines. The transceiver features driver outputs that can be operated in either the open-collector or three-state mode. If Talk Enable (TE) is high, these outputs have the characteristics of open-collector outputs when Pullup Enable (PE) is low and of three-state outputs when PE is high. Taking TE low places the outputs in the high-impedance state. The driver outputs are designed to handle loads of up to 48 milliamperes of sink current. Each receiver features p-n-p transistor inputs for high input impedance and 400 millivolts minimum of guaranteed hysteresis for increased noise immunity.

Output glitches during power-up and power-down are eliminated by an internal circuit that disables both the bus and receiver outputs. The outputs do not load the bus when V_{CC} = 0.

The SN75ALS163 is characterized for operation from 0°C to 70°C.

FUNCTION TABLES

EACH DRIVER

INPUTS			OUTPUT
D	TE	PE	B
H	H	H	H
L	H	X	L
H	X	L	Z
X	L	X	Z

EACH RECEIVER

INPUTS			OUTPUT
B	TE	PE	D
L	L	X	L
H	L	X	H
X	H	X	Z

H = high level, L = low level, X = irrelevant, Z = High-impedance state.

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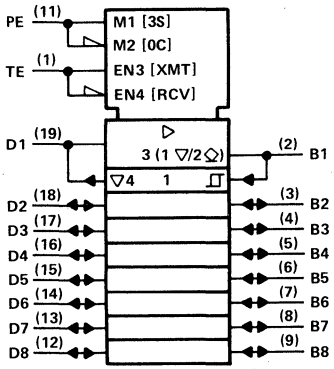
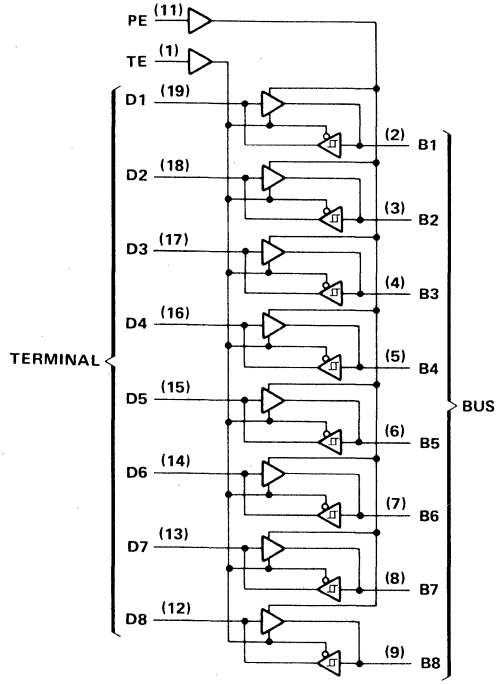
logic symbol†



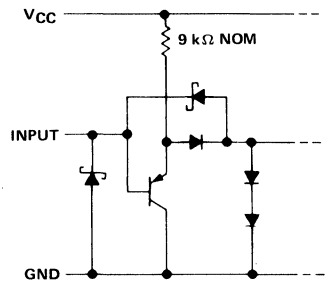
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
▽ Designates 3-state outputs.
◇ Designates open-collector outputs.

logic diagram (positive logic)

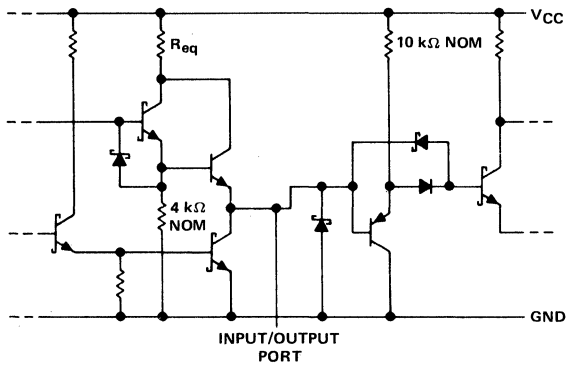


schematics of inputs and outputs

EQUIVALENT OF ALL CONTROL INPUTS



EQUIVALENT OF ALL INPUT/OUTPUT PORTS



Driver output R_{eq} = 30 Ω NOM
Receiver output R_{eq} ≈ 110 Ω NOM

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Low-level driver output current . . . . . 100 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2):
DW package . . . . . 1125 mW
J package . . . . . 1375 mW
N package . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16) inch from the case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds: N package . . . . . 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate the DW package to 720 mW at 70°C at the rate of 9.0 mW/°C, derate the J package to 880 mW at 70°C at the rate of 11.0 mW/°C, and derate the N package to 736 mW at 70°C at the rate of 9.2 mW/°C.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
High-level output current, I_{OH}	Bus ports with pullups active			−10	mA
	Terminal ports			−800	μA
Low-level output current, I_{OL}	Bus ports			48	mA
	Terminal ports			16	
Operating free-air temperature range, T_A		0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = −18 mA			−0.8	−1.5	V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)‡	Bus			0.4	0.65		V
V_{OH}	High level output voltage	Terminal	I_{OH} = −800 μA,	TE at 0.8 V	2.7	3.5		V
		Bus	I_{OH} = −10 mA,	PE and TE at 2 V	2.5	3.3		
V_{OL}	Low-level output voltage	Terminal	I_{OL} = 16 mA,	TE at 0.8 V		0.3	0.5	V
		Bus	I_{OL} = 48 mA,	PE and TE at 2 V		0.35	0.5	
I_{OH}	High-level output current (open-collector mode)	Bus	V_O = 5.5 V, D and TE at 2 V	PE at 0.8 V,			100	μA
I_{OZ}	Off-state output current (3-state mode)	Bus	PE at 2 V, TE at 0.8 V	V_O = 2.7 V			20	μA
				V_O = 0.5 V			−100	
I_I	Input current at maximum input voltage	Terminal	V_I = 5.5 V			0.2	100	μA
I_{IH}	High-level input current	Terminal PE or TE	V_I = 2.7 V			0.1	20	μA
I_{IL}	Low-level input current	Terminal PE or TE	V_I = 0.5 V			−10	−100	μA
I_{OS}	Short-circuit output current	Terminal			−15	−35	−75	mA
		Bus			−25	−50	−125	
I_{CC}	Supply current		No load	Terminal outputs low and enabled		42	56	mA
				Bus outputs low and enabled		52	70	
$C_{i/o(bus)}$	Bus-port capacitance		V_{CC} = 5 V or 0 V, $V_{I/O}$ = 0 to 2 V, f = 1 MHz			30		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}.

switching characteristics over recommended range of operating free-air temperature (unless otherwise noted), V_{CC} = 5 V

PARAMETER		FROM	TO	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Terminal	Bus	C_L = 30 pF, See Figure 1		10	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					12	20	
t_{PLH}	Propagation delay time, low-to-high-level output	Bus	Terminal	C_L = 30 pF, See Figure 2		5	10	ns
t_{PHL}	Propagation delay time, high-to-low-level output					7	14	
t_{PZH}	Output enable time to high level	TE	Bus	C_L = 15 pF, See Figure 3		11	20	ns
t_{PHZ}	Output disable time from high level					3	10	
t_{PZL}	Output enable time to low level					18	35	
t_{PLZ}	Output disable time from low level					5	20	
t_{PZH}	Output enable time to high level	TE	Terminal	C_L = 15 pF, See Figure 4		5	20	ns
t_{PHZ}	Output disable time from high level					8	20	
t_{PZL}	Output enable time to low level					9	20	
t_{PLZ}	Output disable time from low level					8	20	
t_{en}	Output pull-up enable time	PE	Bus	C_L = 15 pF, See Figure 5		3	10	ns
t_{dis}	Output pull-up disable time					4	12	

† All typical values are at T_A = 25°C.

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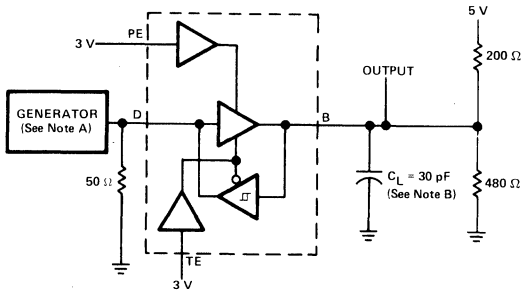
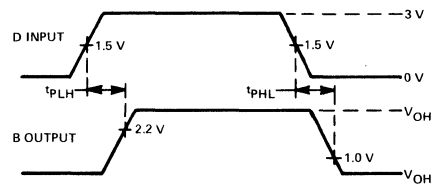
PARAMETER MEASUREMENT INFORMATION

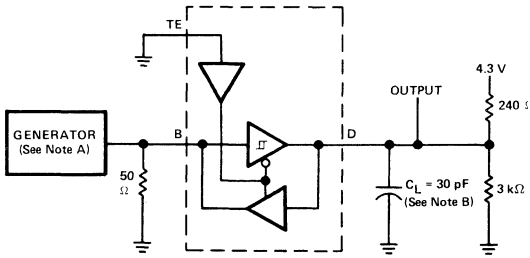


TEST CIRCUIT

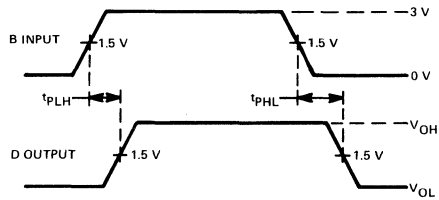


VOLTAGE WAVEFORMS

FIGURE 1. TERMINAL-TO-BUS PROPAGATION DELAY TIMES

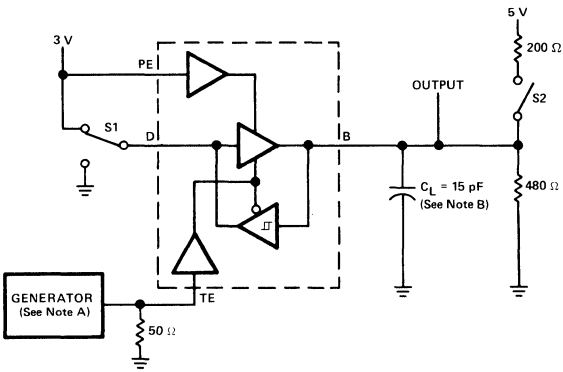


TEST CIRCUIT

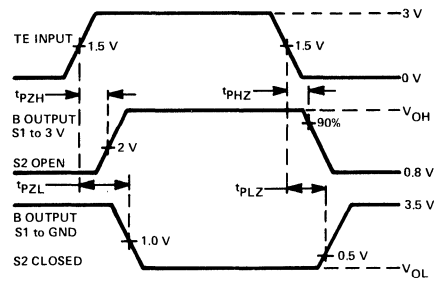


VOLTAGE WAVEFORMS

FIGURE 2. BUS-TO-TERMINAL PROPAGATION DELAY TIMES



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 3. TE-TO-BUS ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION

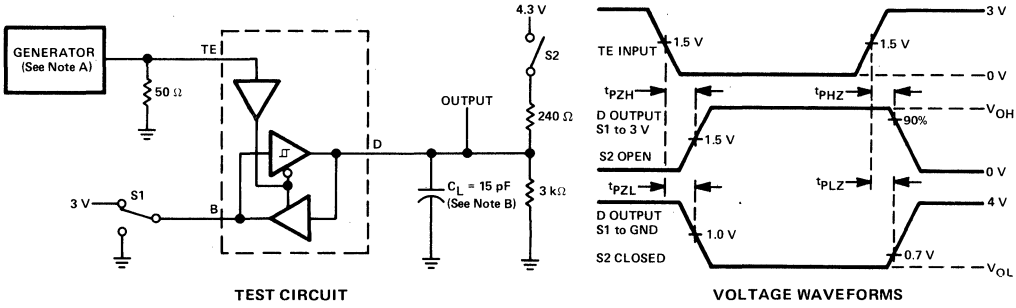


FIGURE 4. TE-TO-TERMINAL ENABLE AND DISABLE TIMES

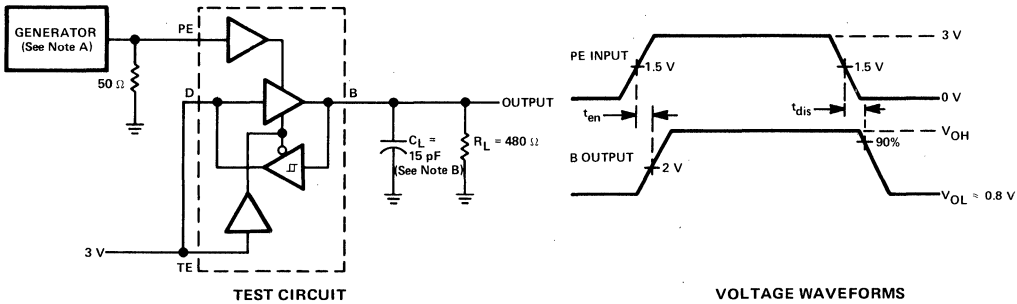


FIGURE 5. PE-TO-BUS PULLUP ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

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TYPICAL CHARACTERISTICS

TERMINAL HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

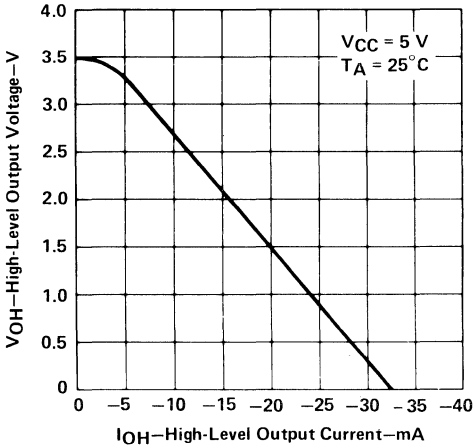

FIGURE 6

TERMINAL LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

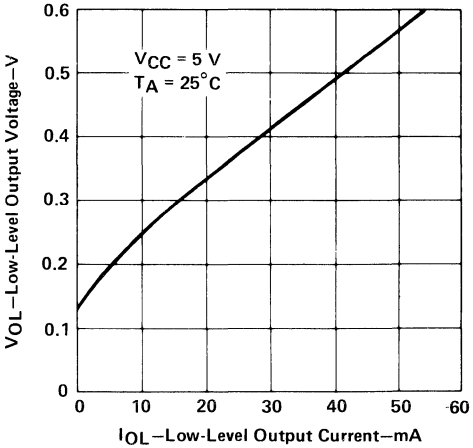

FIGURE 7

TERMINAL OUTPUT VOLTAGE
vs
BUS INPUT VOLTAGE

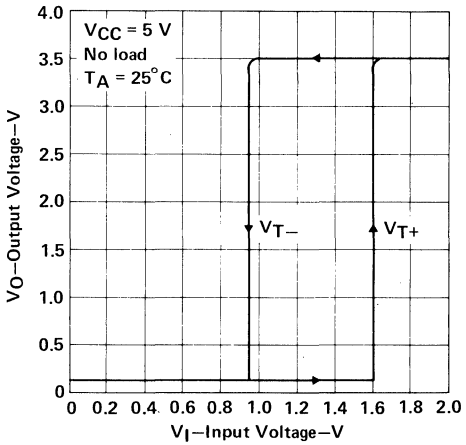

FIGURE 8

TYPICAL CHARACTERISTICS

BUS HIGH-LEVEL OUTPUT VOLTAGE
vs
BUS HIGH-LEVEL OUTPUT CURRENT

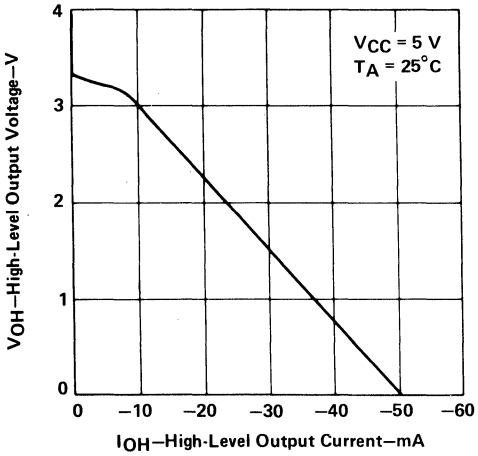

FIGURE 9

BUS LOW-LEVEL OUTPUT VOLTAGE
vs
BUS LOW-LEVEL OUTPUT CURRENT

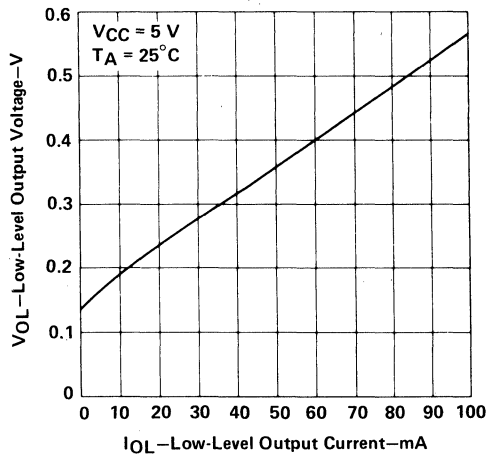

FIGURE 10

BUS OUTPUT VOLTAGE
vs
TERMINAL INPUT VOLTAGE

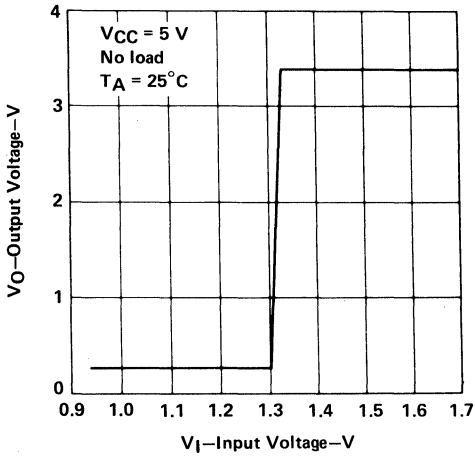

FIGURE 11

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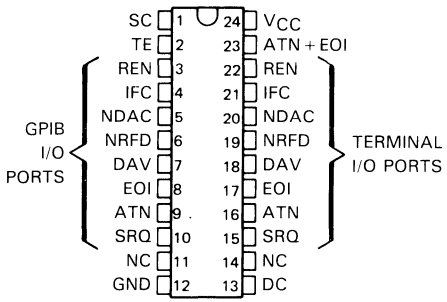
SN75ALS164
OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

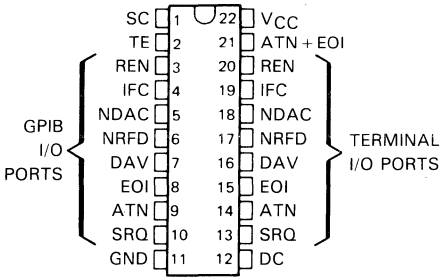
D2908, JUNE 1986

- 8-Channel Bidirectional Transceiver
- Designed to Implement Control Bus Interface
- Designed for Multicontrollers
- High-Speed Advanced Low-Power Schottky Circuitry
- Low Power Dissipation . . . 46 mW Max per Channel
- Fast Propagation Times . . . 20 ns Max
- High-Impedance P-N-P Inputs
- Receiver Hysteresis . . . 650 mV Typ
- Bus-Terminating Resistors Provided on Driver Outputs
- No Loading of Bus When Device is Powered Down (V_{CC} = 0)
- Power-Up/Power-Down Protection (Glitch-Free)

DW PACKAGE
(TOP VIEW)



N DUAL-IN-LINE PACKAGE
(TOP VIEW)



NC—No internal connection.

CHANNEL IDENTIFICATION TABLE

NAME	IDENTITY	CLASS
DC TE SC	Direction Control Talk Enable System Control	Control
ATN SRQ REN IFC EOI	Attention Service Request Remote Enable Interface Clear End or Identify	Bus Management
ATN + EOI	ATN logical OR EOI	Logic
DAV NDAC NRFD	Data Valid Not Data Accepted Not Ready for Data	Data Transfer

description

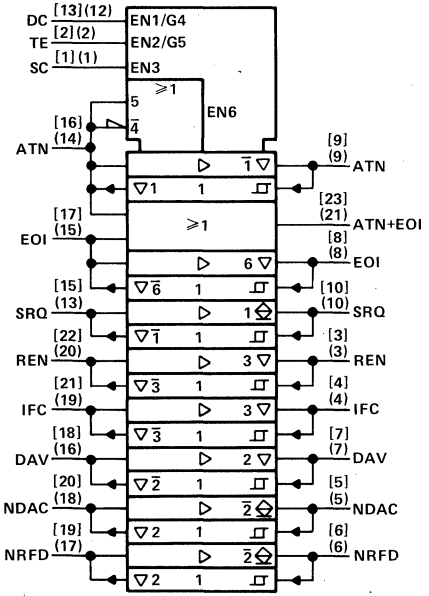
The SN75ALS164 eight-channel general-purpose interface bus transceiver is a monolithic, high-speed, Advanced Low-Power Schottky device designed to meet the requirements of IEEE Standard 488-1978. Each transceiver is designed to provide the bus-management and data-transfer signals between operating units of a multiple-controller instrumentation system. When combined with the SN75ALS160 octal bus transceiver, the SN75ALS164 provides the complete 16-wire interface for the IEEE 488 bus.

The SN75ALS164 features eight driver-receiver pairs connected in a front-to-back configuration to form input/output (I/O) ports at both the bus and terminal sides. All outputs are disabled (at a high-impedance state) during V_{CC} power-up and power-down transitions for glitch-free operation. The direction of data flow through these driver-receiver pairs is determined by the DC, TE, and SC enable signals. The SN75ALS164 is identical to the SN75ALS162 with the addition of an OR gate to help simplify board layouts in several popular applications. The ATN and EOI signals are ORed to pin 21, which is a standard totem-pole output.

The driver outputs (GPIB I/O ports) feature active bus-terminating resistor circuits designed to provide a high impedance to the bus when supply voltage V_{CC} is 0. The drivers are designed to handle loads up to 48 milliamperes of sink current. Each receiver features p-n-p transistor inputs for high input impedance and a guaranteed hysteresis of 400 millivolts minimum for increased noise immunity. All receivers have 3-state outputs to present a high impedance to the terminal when disabled.

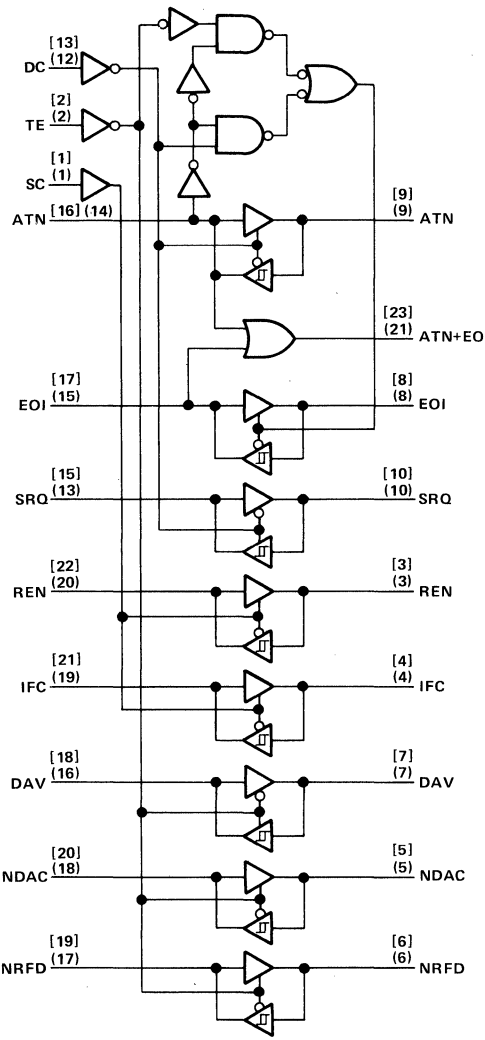
The SN75ALS164 is manufactured in a 22-pin dual-in-line N package and in 24-pin DW package, and is characterized for operation from 0°C to 70°C.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
▽Designates 3-state outputs.
◈ Designates passive-pullup outputs.

logic diagram (positive logic)



[ ] Denotes pin numbers for DW package.
( ) Denotes pin numbers for N package.

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RECEIVE/TRANSMIT FUNCTION TABLE

CONTROLS				BUS-MANAGEMENT CHANNELS					DATA-TRANSFER CHANNELS		
SC	DC	TE	ATN†	ATN† (Controlled by DC)	SRQ (Controlled by DC)	REN (Controlled by SC)	IFC (Controlled by SC)	EOI	DAV (Controlled by TE)	NDAC (Controlled by TE)	NRFD (Controlled by TE)
	H	H	H	R	T			T	T	R	R
	H	H	L					R			
	L	L	H	T	R			R	R	T	T
	L	L	L					T			
	H	L	X	R	T			R	R	T	T
	L	H	X	T	R			T	T	R	R
H						T	T				
L						R	R				

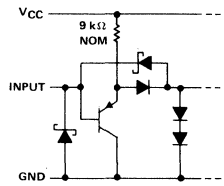
H = high level, L = low level, R = receive, T = transmit, X = irrelevant
Direction of data transmission is from the terminal side to the bus side, and the direction of data receiving is from the bus side to the terminal side. Data transfer is noninverting in both directions.
†ATN is a normal transceiver channel that functions additionally as an internal direction control or talk enable for EOI whenever the DC and TE inputs are in the same state. When DC and TE are in opposite states, the ATN channel functions as an independent transceiver only.

ATN + EOI FUNCTION TABLE

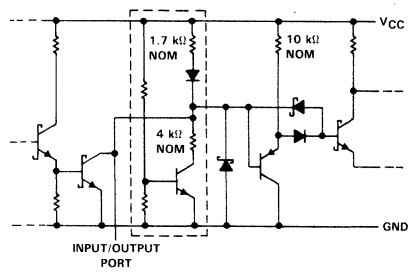
INPUTS		OUTPUT
ATN	EOI	ATN + EOI
H	X	H
X	H	H
L	L	L

schematics of inputs and outputs

EQUIVALENT OF ALL CONTROL INPUTS

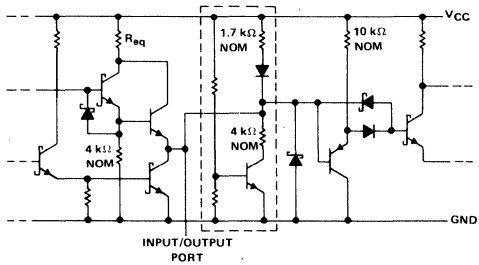


TYPICAL OF SRQ, NDAC, and NRFD GPIB I/O PORT



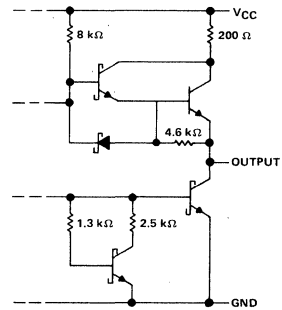
Circuit inside dashed lines is on GPIB I/O ports only.

TYPICAL OF ALL I/O PORTS EXCEPT SRQ, NDAC, and NRFD GPIB I/O PORTS



Driver output R_{eq} = 30 Ω NOM
Receiver output R_{eq} = 110 Ω NOM
Circuit inside dashed lines is on GPIB I/O ports only.

ATN+EOI OUTPUT



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Low-level driver output current . . . . . 100 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2):
DW package . . . . . 1350 mW
N package . . . . . 1700 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16) inch from the case for 10 seconds: DW or N package . . . . 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate the DW package to 864 mW at 70°C at the rate of 10.8 mW/°C, and derate the N package to 1088 mW at 70°C at the rate of 13.6 mW/°C.

TEXAS INSTRUMENTS
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recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
High-level output current, I_{OH}	Bus ports with 3-state outputs			−5.2	mA
	Terminal ports			−800	μA
	ATN + EOI			−400	
Low-level output current, I_{OL}	Bus ports			48	mA
	Terminal ports			16	
	ATN + EOI			4	
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = −18 mA			−0.8	−1.5	V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)	Bus			0.4	0.65		V
V_{OH}‡	High-level output voltage	Terminal	I_{OH} = −800 μA		2.7	3.5		V
		Bus	I_{OH} = −5.2 mA		2.5	3.3		
		ATN + EOI	I_{OH} = −400 μA		2.7			
V_{OL}	Low-level output voltage	Terminal	I_{OL} = 16 mA			0.3	0.5	V
		Bus	I_{OL} = 48 mA			0.35	0.5	
		ATN + EOI	I_{OL} = 4 mA				0.4	
I_I	Input current at maximum input voltage	Terminal§	V_I = 5.5 V			0.2	100	μA
		ATN, EOI	V_I = 5.5 V				200	
I_{IH}	High-level input current	Terminal control	V_I = 2.7 V			0.1	20	μA
		ATN, EOI	V_I = 2.7 V				40	
I_{IL}	Low-level input current	Terminal, control	V_I = 0.5 V			−10	−100	μA
		ATN, EOI	V_I = 0.5 V				−500	
$V_{I/O(bus)}$	Voltage at bus port		Driver disabled	$I_{I(bus)}$ = 0	2.5	3.0	3.7	V
				$I_{I(bus)}$ = −12 mA			−1.5	
$I_{I/O(bus)}$	Current into bus port	Power on	Driver disabled	$V_{I(bus)}$ = −1.5 V to 0.4 V	−1.3			mA
				$V_{I(bus)}$ = 0.4 V to 2.5 V	0		−3.2	
				$V_{I(bus)}$ = 2.5 V to 3.7 V			+2.5 −3.2	
				$V_{I(bus)}$ = 3.7 V to 5 V	0		2.5	
				$V_{I(bus)}$ = 5 V to 5.5 V	0.7		2.5	
		Power off	V_{CC} = 0,	$V_{I(bus)}$ = 0 V to 2.5 V			−40	μA
I_{OS}	Short-circuit output current	Terminal			−15	−35	−75	mA
		Bus			−25	−50	−125	
		ATN + EOI			−10		−100	
I_{CC}	Supply current		No load, TE, DC, and SC low			55	75	mA
$C_{i/o(bus)}$	Bus-port capacitance		V_{CC} = 5 V to 0 V, $V_{I/O}$ = 0 to 2 V, f = 1 MHz			30		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ V_{OH} applies for three-state outputs only.
§ Except ATN and EOI terminal pins.

switching characteristics over recommended range of operating free-air temperature (unless otherwise noted), V_{CC} = 5 V

PARAMETER		FROM	TO	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Terminal	Bus	C_L = 30 pF, See Figure 1		10	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					12	20	
t_{PLH}	Propagation delay time low-to-high-level output	Bus	Terminal	C_L = 30 pF, See Figure 2		5	10	ns
t_{PHL}	Propagation delay time, high-to-low-level output					7	14	
t_{PLH}	Propagation delay time, low-to-high-level output	Terminal ATN or Terminal EOI	ATN+EOI	C_L = 15 pF, See Figure 3		3.5	10	ns
t_{PHL}	Propagation delay time, high-to-low-level output	Terminal ATN or Terminal EOI	ATN+EOI	C_L = 15 pF, See Figure 3		7	15	ns
t_{PZH}	Output enable time to high level	TE, DC, or SC	BUS (ATTN, EOI, REN, IFC, and DAV)	C_L = 15 pF, See Figure 4			30	ns
t_{PHZ}	Output disable time from high level						20	
t_{PZL}	Output enable time to low level						45	
t_{PLZ}	Output disable time from low level						20	
t_{PZH}	Output enable time to high level	TE, DC, or SC	Terminal	C_L = 15 pF, See Figure 5			20	ns
t_{PHZ}	Output disable time from high level						25	
t_{PZL}	Output enable time to low level						30	
t_{PLZ}	Output disable time from low level						25	

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PARAMETER MEASUREMENT INFORMATION

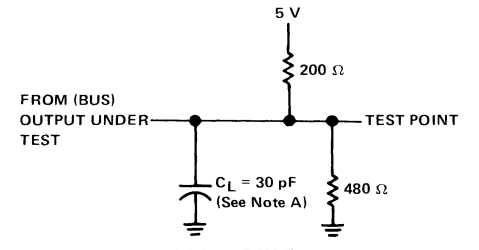


FIGURE 1. TERMINAL-TO-BUS PROPAGATION DELAY TIMES

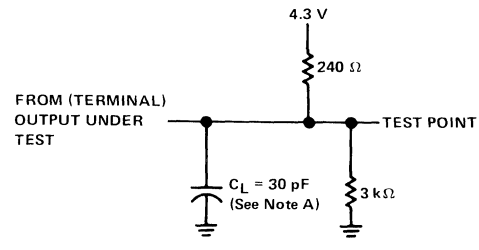
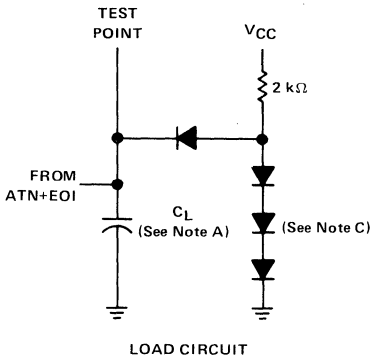


FIGURE 2. BUS-TO-TERMINAL PROPAGATION DELAY TIMES



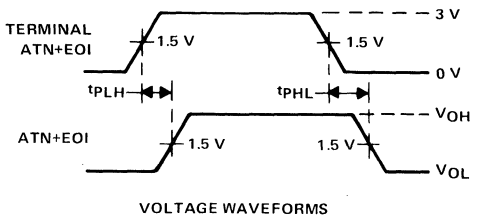
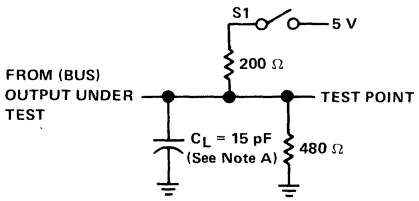


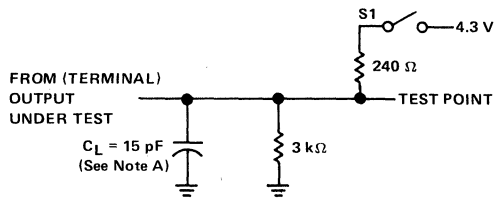
FIGURE 3. ATN + EOI PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤6 ns, t_f ≤6 ns, Z_{out} = 50 Ω.
C. All diodes are 1N916 or 1N3064.

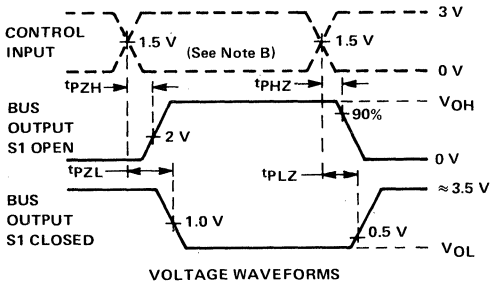
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

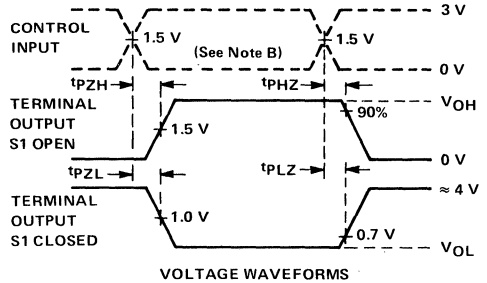


LOAD CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 4. BUS ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORMS

FIGURE 5. TERMINAL ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤6 ns, t_f ≤6 ns, Z_{out} = 50 Ω.

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TYPICAL CHARACTERISTICS

TERMINAL HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

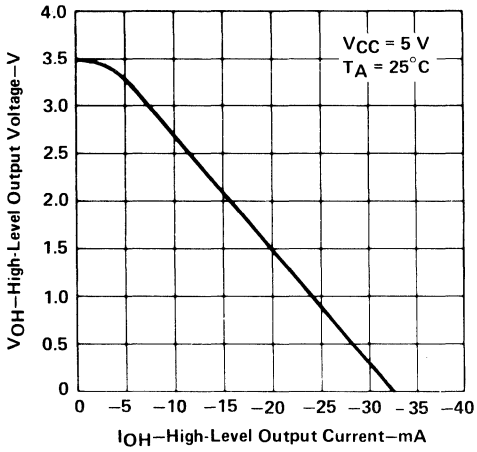

FIGURE 6

TERMINAL LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

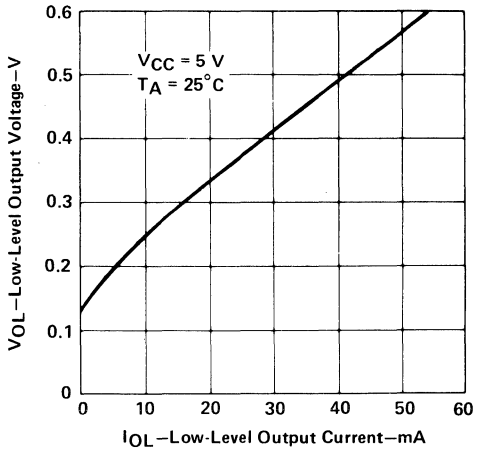

FIGURE 7

TERMINAL OUTPUT VOLTAGE
vs
BUS INPUT VOLTAGE

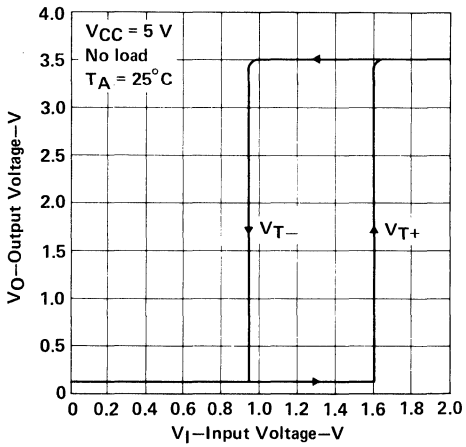

FIGURE 8

TYPICAL CHARACTERISTICS

BUS HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

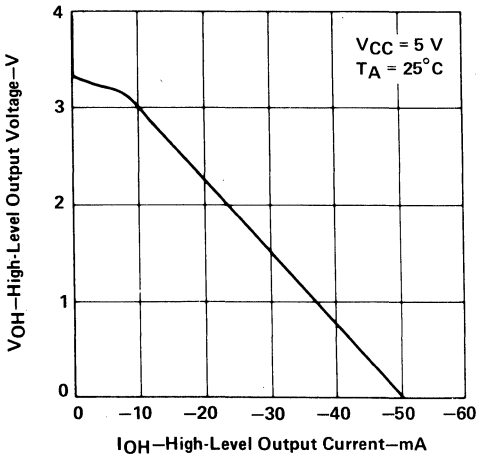

FIGURE 9

BUS LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

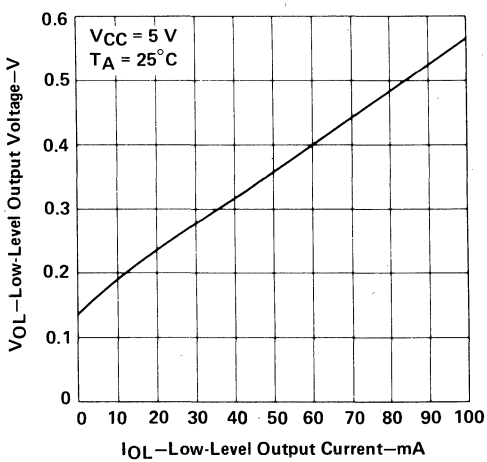

FIGURE 10

BUS OUTPUT VOLTAGE
vs
TERMINAL INPUT VOLTAGE

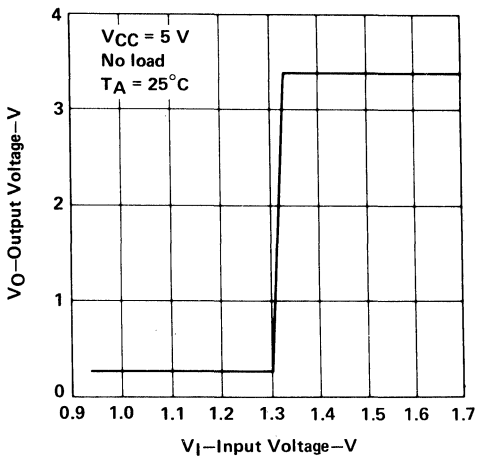

FIGURE 11

BUS CURRENT
vs
BUS VOLTAGE

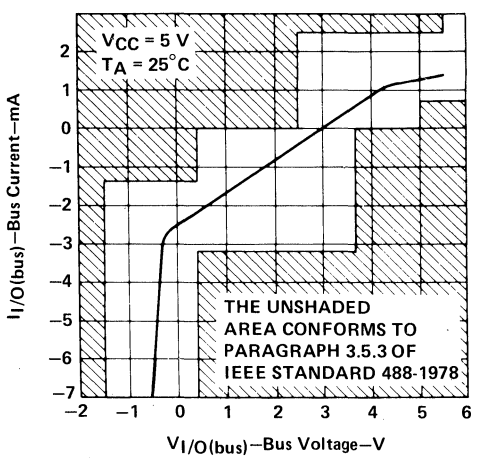

FIGURE 12

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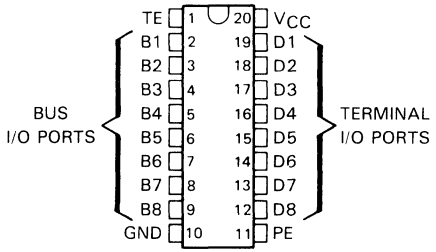
SN75ALS165
OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

D3011, JUNE 1986

MEETS IEEE STANDARD 488-1978 (GPIB)

- 8-Channel Bidirectional Transceiver
- High-Speed Advanced Low-Power Schottky Circuitry
- Low Power Dissipation . . . 46 mW Max per Channel
- Fast Propagation Times . . . 20 ns Max
- High-Impedance P-N-P Inputs
- Receiver Hysteresis . . . 650 mV Typ
- No Loading of Bus When Device is Powered Down (V_{CC} = 0)
- Power-Up/Power-Down Protection (Glitch-Free)
- Driver and Receiver Can Be Disabled Simultaneously

DW, J, OR N PACKAGE
(TOP VIEW)



description

The SN75ALS165 eight-channel general-purpose interface bus transceiver is a monolithic, high-speed, Advanced Low-Power Schottky device designed for two-way data communications over single-ended transmission lines. It is designed to meet the requirements of IEEE Standard 488-1978. The transceiver features driver outputs that can be operated in either the passive-pullup or three-state mode. If Talk Enable (TE) is high, these ports have the characteristics of passive-pullup outputs when Pullup Enable (PE) is low and of three-state outputs when PE is high. Taking TE low places these ports in the high-impedance state. Taking TE and PE low places both the drivers and receivers in the high-impedance state. The driver outputs are designed to handle loads up to 48 milliamperes of sink current.

An active turn-off feature has been incorporated into the bus-terminating resistors so that the device exhibits a high impedance to the bus when V_{CC} = 0. When combined with the SN75ALS161 or SN75ALS162 management bus transceiver, the pair provides the complete 16-wire interface for the IEEE 488 bus.

The SN75ALS165 is manufactured in a 20-pin package and is characterized for operation from 0°C to 70°C.

FUNCTION TABLES

EACH DRIVER

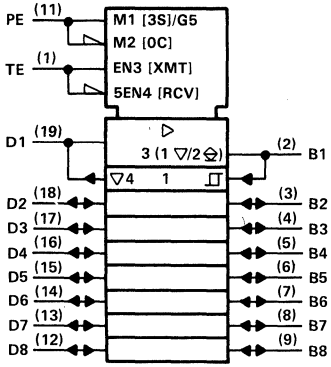
INPUTS			OUTPUT
D	TE	PE	B
H	H	H	H
L	H	X	L
H	X	L	Z†
X	L	X	Z†

EACH RECEIVER

INPUTS			OUTPUT
B	TE	PE	D
L	L	H	L
H	L	H	H
X	H	X	Z
X	X	L	Z

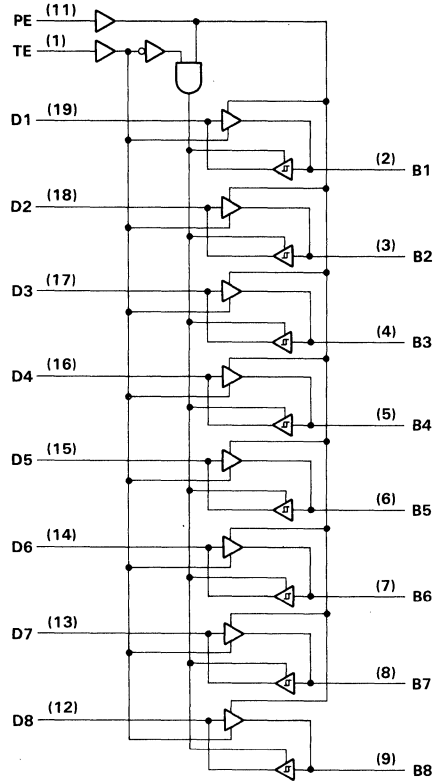
H = high level, L = low level, X = irrelevant,
Z = high-impedance state.
†This is the high-impedance state of a normal 3-state output modified by the internal resistors to V_{CC} and ground.

logic symbol†



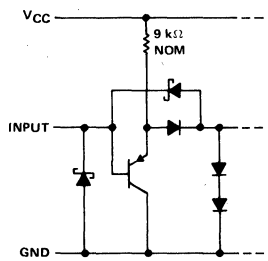
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
▽ Designates 3-state outputs.
⏢ Designates passive-pullup outputs.

logic diagram (positive logic)

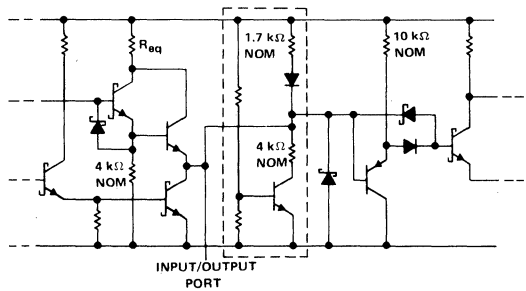


schematics of inputs and outputs

EQUIVALENT OF ALL CONTROL INPUTS



EQUIVALENT OF ALL INPUT/OUTPUT PORTS



Driver output R_{eq} = 30 Ω NOM
Receiver output R_{eq} = 110 Ω NOM
Circuit inside dashed lines is on the driver outputs only.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Low-level driver output current . . . . . 100 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2):
DW package . . . . . 1125 mW
J package . . . . . 1375 mW
N package . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds: DW or N package . . . . 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate the DW package to 720 mW at 70°C at the rate of 9.0 mW/°C, derate the J package to 880 mW at 70°C at the rate of 11.0 mW/°C, and derate the N package to 736 mW at 70°C at the rate of 9.2 mW/°C.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
High-level output current, I_{OH}	Bus ports with pullups active			−5.2	mA
	Terminal ports			−800	μA
Low-level output current, I_{OL}	Bus ports			48	mA
	Terminal ports			16	
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = −18 mA			−0.8	−1.5	V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)	Bus			0.4	0.65		V
V_{OH}‡	High-level output voltage	Terminal	I_{OH} = −800 μA,	TE at 0.8 V	2.7	3.5		V
		Bus	I_{OH} = −5.2 mA,	PE and TE at 2 V	2.5	3.3		
V_{OL}	Low-level output voltage	Terminal	I_{OL} = 16 mA,	TE at 0.8 V		0.3	0.5	V
		Bus	I_{OL} = 48 mA,	TE at 2 V		0.35	0.5	
I_I	Input current at maximum input voltage	Terminal	V_I = 5.5 V			0.2	100	μA
I_{IH}	High-level input current	Terminal and control inputs	V_I = 2.7 V			0.1	20	μA
I_{IL}	Low-level input current		V_I = 0.5 V			−10	−100	μA
$V_{I/O(bus)}$	Voltage at bus port		Driver disabled	$I_{I(bus)}$ = 0	2.5	3.0	3.7	V
				$I_{I(bus)}$ = −12 mA			−1.5	
$I_{I/O(bus)}$	Current into bus port	Power on	Driver disabled	$V_{I(bus)}$ = −1.5 V to 0.4 V	−1.3			mA
				$V_{I(bus)}$ = 0.4 V to 2.5 V	0		−3.2	
				$V_{I(bus)}$ = 2.5 V to 3.7 V			+2.5 −3.2	
				$V_{I(bus)}$ = 3.7 V to 5 V	0		2.5	
				$V_{I(bus)}$ = 5 V to 5.5 V	0.7		2.5	
		Power off	V_{CC} = 0,	$V_{I(bus)}$ = 0 V to 2.5 V			−40	μA
I_{OS}	Short-circuit output current	Terminal			−15	−35	−75	mA
		Bus			−25	−50	−125	
I_{CC}	Supply current		No load	Terminal outputs low and enabled		42	56	mA
				Bus outputs low and enabled		52	70	
$C_{i/o(bus)}$	Bus-port capacitance		V_{CC} = 5 V to 0 V, $V_{I/O}$ = 0 to 2 V, f = 1 MHz			30		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ V_{OH} applies for three-state outputs only.

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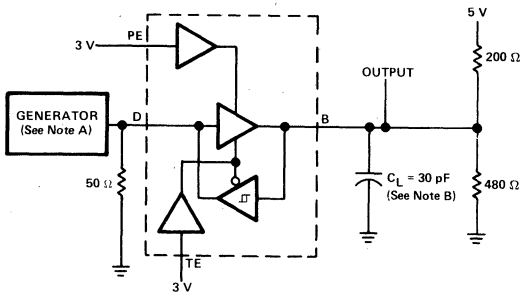
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

switching characteristics over recommended range of operating free-air temperature (unless otherwise noted), V_{CC} = 5 V

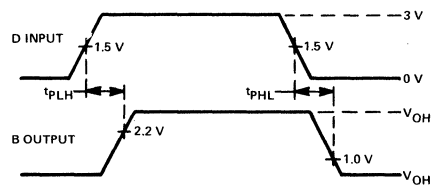
PARAMETER		FROM	TO	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Terminal	Bus	C_L = 30 pF, See Figure 1		10	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					12	20	
t_{PLH}	Propagation delay time, low-to-high-level output	Bus	Terminal	C_L = 30 pF, See Figure 2		5	10	ns
t_{PHL}	Propagation delay time, high-to-low-level output					7	14	
t_{PZH}	Output enable time to high level	TE	Bus	C_L = 15 pF, See Figure 3		11	20	ns
t_{PHZ}	Output disable time from high level					3	10	
t_{PZL}	Output enable time to low level					18	35	
t_{PLZ}	Output disable time from low level					5	20	
t_{PZH}	Output enable time to high level	TE	Terminal	C_L = 15 pF, See Figure 4		5	20	ns
t_{PHZ}	Output disable time from high level					8	20	
t_{PZL}	Output enable time to low level					9	20	
t_{PLZ}	Output disable time from low level					8	20	
t_{en}	Output pull-up enable time	PE	Terminal	C_L = 15 pF, See Figure 5		3	10	ns
t_{dis}	Output pull-up disable time					4	12	

†All typical values are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

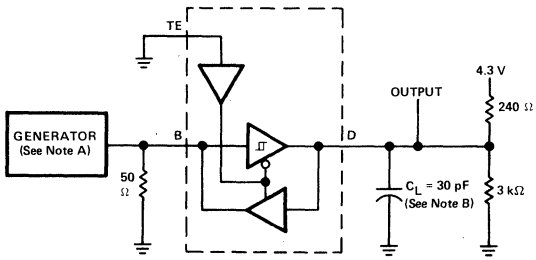


TEST CIRCUIT

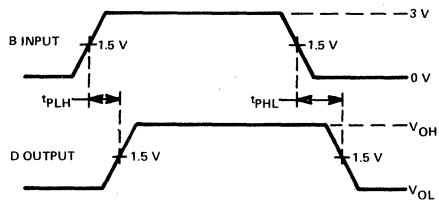


VOLTAGE WAVEFORMS

FIGURE 1. TERMINAL-TO-BUS PROPAGATION DELAY TIMES

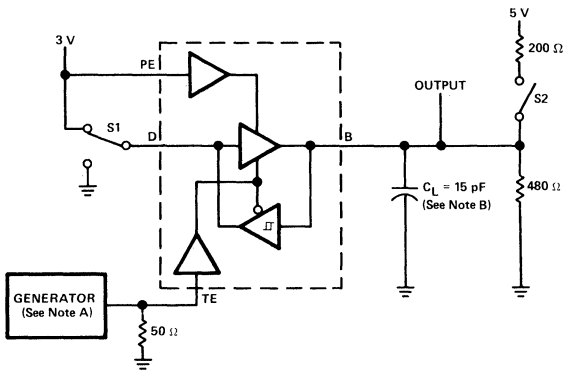


TEST CIRCUIT

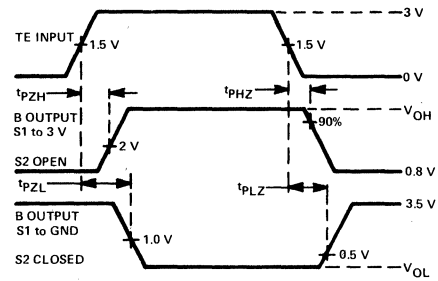


VOLTAGE WAVEFORMS

FIGURE 2. BUS-TO-TERMINAL PROPAGATION DELAY TIMES



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 3. TE-TO-BUS ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

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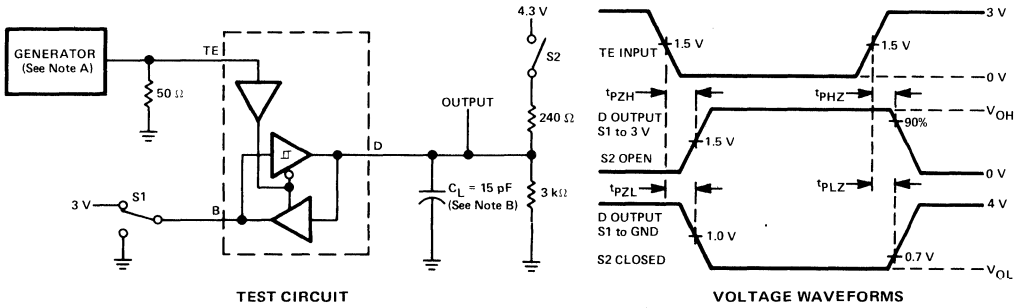
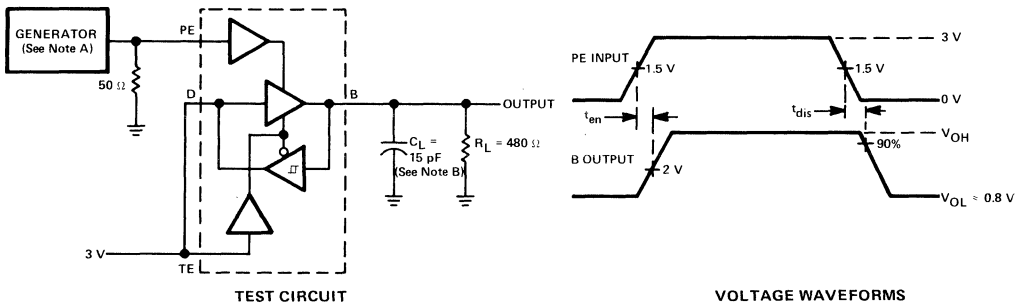
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 4. TE-TO-TERMINAL ENABLE AND DISABLE TIMES



TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 5. PE-TO-BUS PULLUP ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

TERMINAL HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

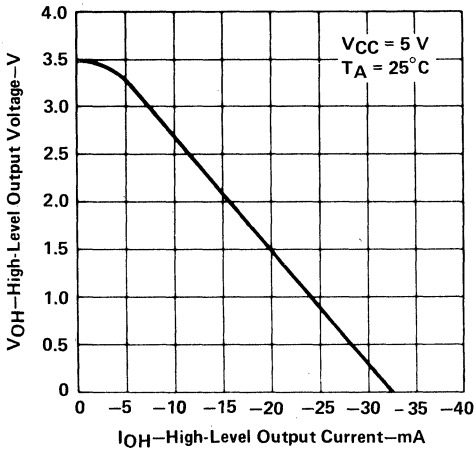


FIGURE 6

TERMINAL LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

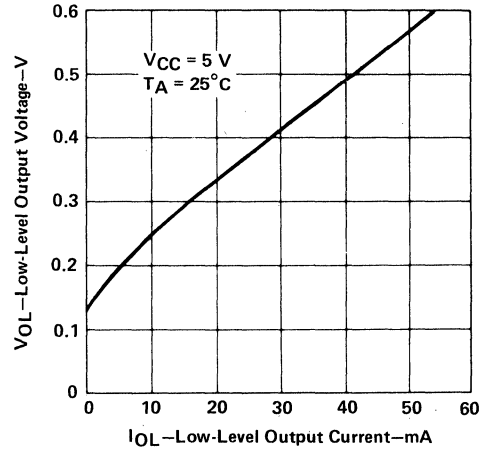


FIGURE 7

TERMINAL OUTPUT VOLTAGE
vs
BUS INPUT VOLTAGE

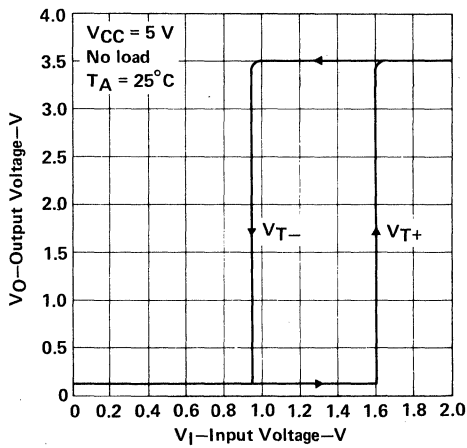


FIGURE 8

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TYPICAL CHARACTERISTICS

BUS HIGH-LEVEL OUTPUT VOLTAGE
vs
BUS HIGH-LEVEL OUTPUT CURRENT

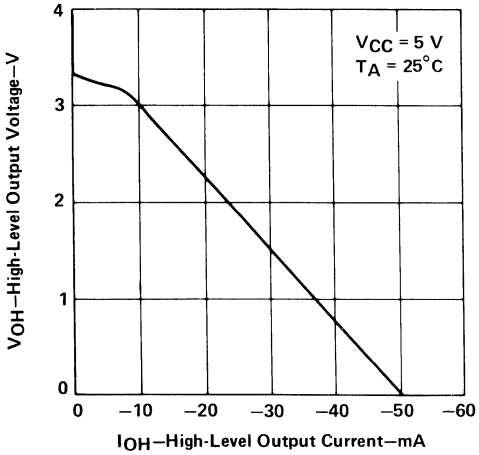


FIGURE 9

BUS LOW-LEVEL OUTPUT VOLTAGE
vs
BUS LOW-LEVEL OUTPUT CURRENT

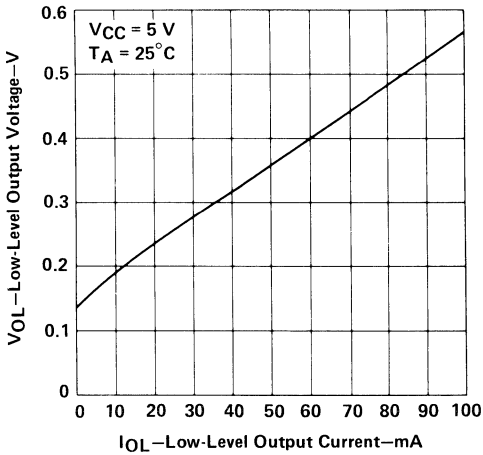


FIGURE 10

BUS OUTPUT VOLTAGE
vs
TERMINAL INPUT VOLTAGE

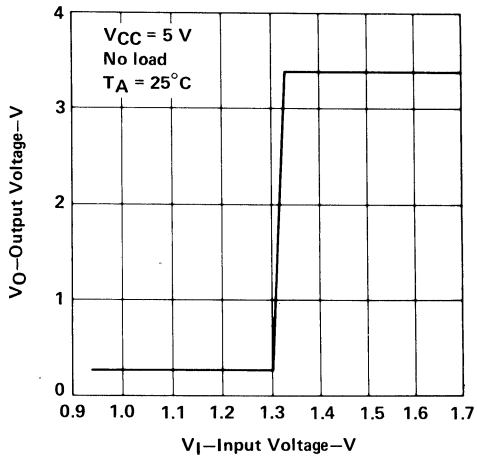
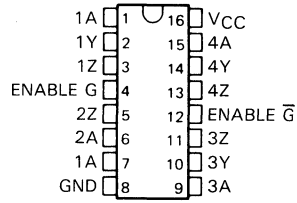


FIGURE 11

D2904, JULY 1985

- Meets EIA Standard RS-422-A
- High-Speed, Low-Power ALS Design
- 3-State TTL Compatible
- Single 5-V Supply Operation
- High Output Impedance in Power-Off Condition
- Complementary Output Enable Inputs
- Improved Replacement for the AM26LS31

SN75ALS192 . . . D, J, N DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

This quadruple complementary-output line driver is designed for data transmission over twisted-pair or parallel-wire transmission lines. It meets the requirements of EIA Standard RS-422-A and is compatible with 3-state TTL circuits. Advanced Low-Power Schottky technology provides high speed without the usual power penalties. Standby supply current is typically only 26 milliamperes, while typical propagation delay time is less than 10 nanoseconds.

FUNCTION TABLE (EACH DRIVER)

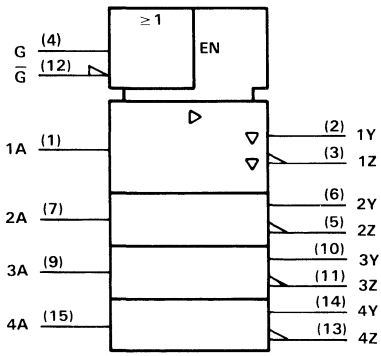
INPUT	ENABLES		OUTPUTS	
A	G	$\overline{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

H = high level, L = low level,
Z = high impedance (off),
X = irrelevant

High-impedance inputs maintain input currents low, less than 1 microampere for a high level and less than 100 microamperes for a low level. Complementary control inputs, G and $\overline{G}$, allow these devices to be enabled at either a high input level or low input level. The SN75ALS192 is capable of data rates in excess of 20 megabits per second and is designed to operate with the SN75ALS193 quadruple line receiver.

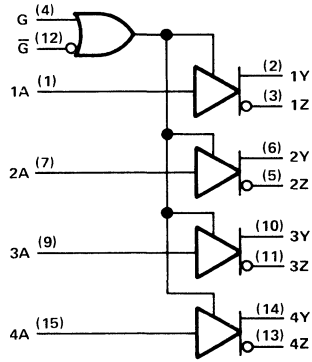
The SN75ALS192 is characterized for operation from 0°C to 70°C.

logic symbol†



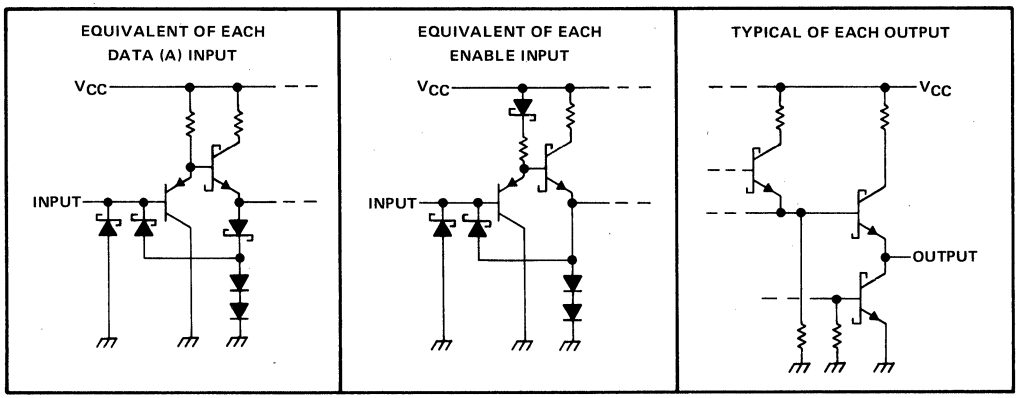
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



3 Interface ALS Circuits

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, V_I . . . . . 7 V
Output off-state voltage . . . . . 5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2):
D package . . . . . 950 mW
J package . . . . . 1000 mW
N package . . . . . 875 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C

NOTES: 1. All voltage values except differential output voltage V_{OD} are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, refer to the Dissipation Derating Table. In the J package, SN75ALS192 chips are glass mounted.

DISSIPATION DERATING TABLE

PACKAGE	T_A = 25°C POWER RATING	DERATING FACTOR	ABOVE T_A	T_A = 70° POWER RATING
D	950 mW	7.6 mW/°C	25°C	608 mW
J (Glass mount)	1000 mW	8.2 mW/°C	28°C	656 mW
N	875 mW	7.0 mW/°C	25°C	560 mW

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recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			−20	mA
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

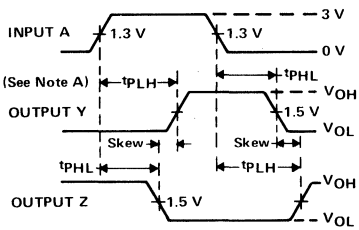
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 4.75 V, I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = 4.75 V, I_{OH} = −20 mA		2.5			V
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, I_{OL} = 20 mA				0.5	V
I_{OZ}	Off-state (high-impedance state) output current	V_{CC} = 5.25 V	V_O = 0.5 V			−20	μA
			V_O = 2.5 V			20	
I_I	Input current at maximum input voltage	V_{CC} = 5.25 V, V_I = 7 V				0.1	mA
I_{IH}	High-level input current	V_{CC} = 5.25 V, V_I = 2.7 V				20	μA
I_{IL}	Low-level input current	V_{CC} = 5.25 V, V_I = 0.4 V				0.2	mA
I_{OS}	Short-circuit output current‡	V_{CC} = 5.25 V		−30		−150	mA
I_{CC}	Supply current (all drivers)	V_{CC} = 5.25 V, All outputs disabled			26	45	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

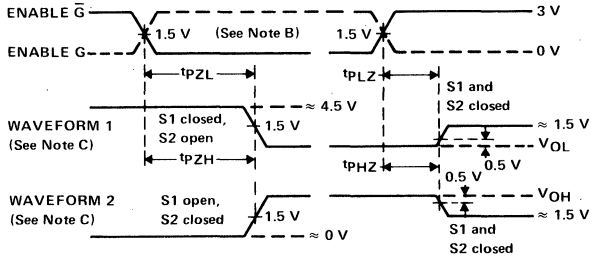
switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 1)

PARAMETER		TEST CONDTIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 30 pF, S1 and S2 open			6	13	ns
t_{PHL}	Propagation delay time, high-to-low-level output				9	14	ns
	Output-to-output skew				3	6	ns
t_{PZH}	Output enable time to high level	R_L = 75 Ω			11	15	ns
t_{PZL}	Output enable time to low level	R_L = 180 Ω			16	20	ns
t_{PHZ}	Output disable time from high level	C_L = 10 pF, S1 and S2 closed			8	15	ns
t_{PLZ}	Output disable time from low level				18	20	ns

PARAMETER MEASUREMENT INFORMATION

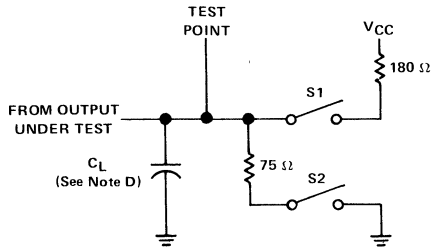


PROPAGATION DELAY TIMES AND SKEW



ENABLE AND DISABLE TIMES

VOLTAGE WAVEFORMS



TEST CIRCUIT

NOTES: A. When measuring propagation delay times and skew, switches S1 and S2 are open.
B. Each enable is tested separately.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the enable inputs. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the enable inputs.
D. C_L includes probe and jig capacitance.
E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_{out} ≈ 50 Ω, t_r ≤ 15 ns, and t_f ≤ 6 ns.

FIGURE 1. SWITCHING TIMES

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TYPICAL CHARACTERISTICS

Y OUTPUT VOLTAGE
vs
DATA INPUT VOLTAGE

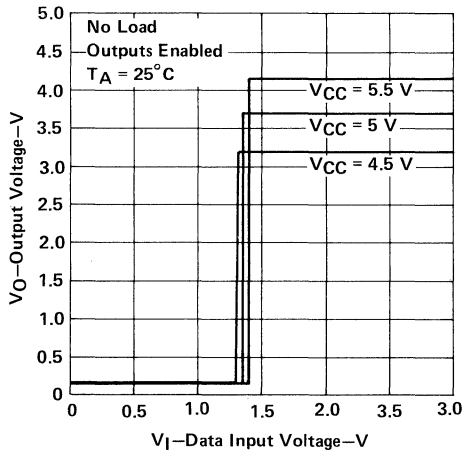

FIGURE 2

Y OUTPUT VOLTAGE
vs
DATA INPUT VOLTAGE

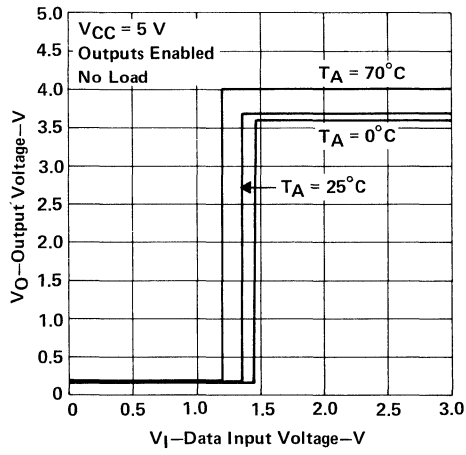

FIGURE 3

Y OUTPUT VOLTAGE
vs
ENABLE G INPUT VOLTAGE

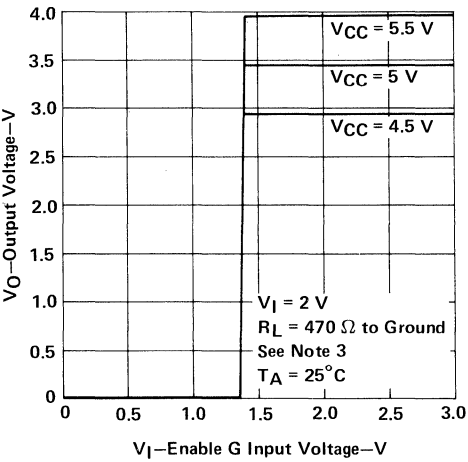

FIGURE 4

Y OUTPUT VOLTAGE
vs
ENABLE G INPUT VOLTAGE

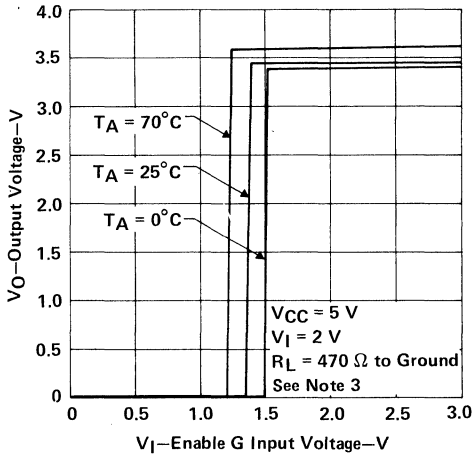

FIGURE 5

NOTE 3: The A input is connected to V_{CC} during the testing of the Y outputs and to ground during the testing of the Z outputs.

TYPICAL CHARACTERISTICS

Z OUTPUT VOLTAGE
vs
ENABLE G INPUT VOLTAGE

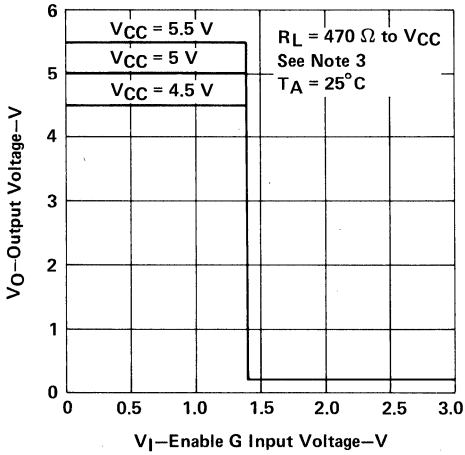

FIGURE 6

Z OUTPUT VOLTAGE
vs
ENABLE G INPUT VOLTAGE

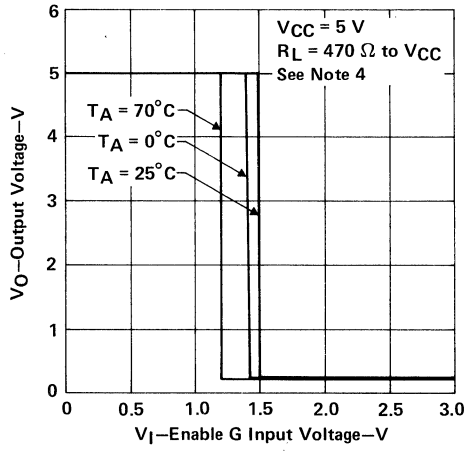

FIGURE 7

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

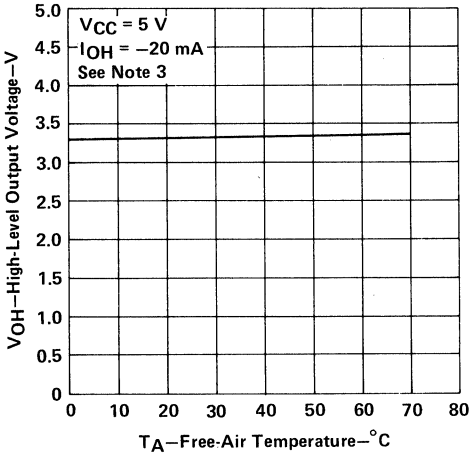

FIGURE 8

HIGH-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

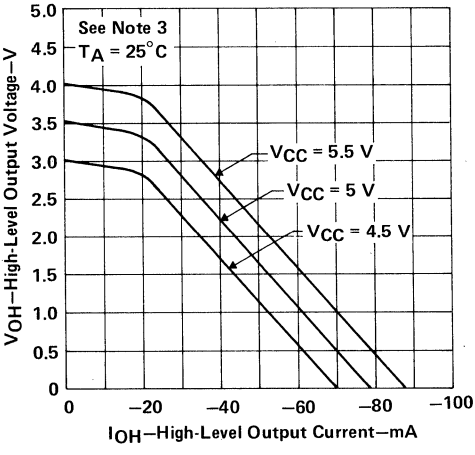

FIGURE 9

NOTES: 3. The A input is connected to V_{CC} during the testing of the Y outputs and to ground during the testing of the Z outputs.
4. The A input is connected to ground during the testing of the Y outputs and to V_{CC} during the testing of the Z outputs.

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TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

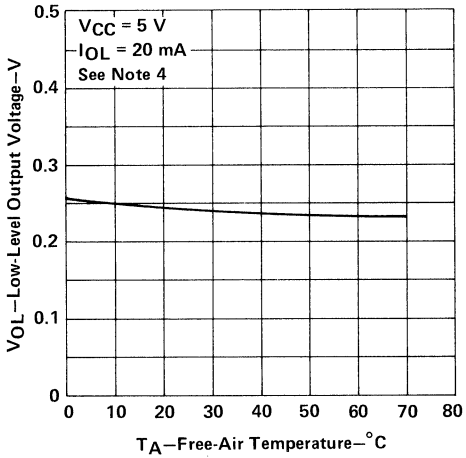

FIGURE 10

LOW-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

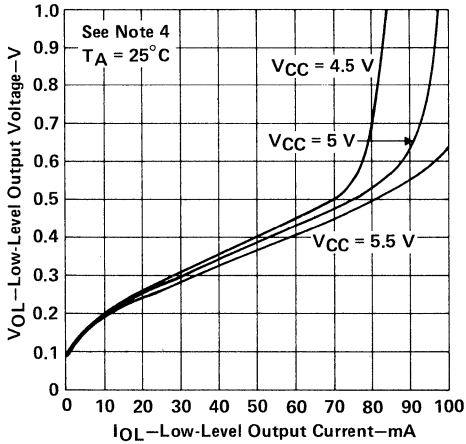

FIGURE 11

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

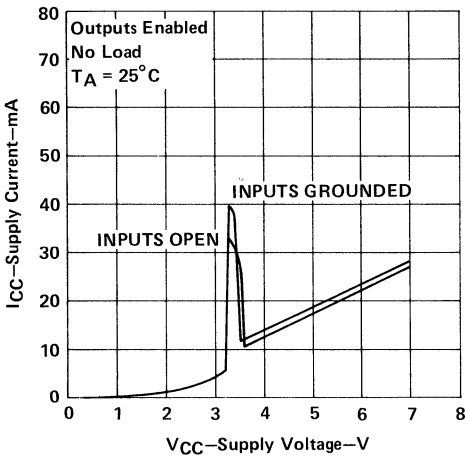

FIGURE 12

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

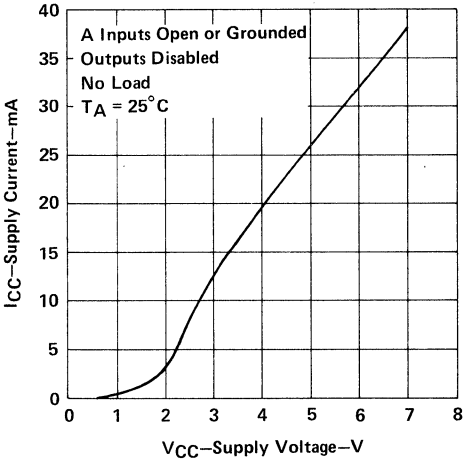

FIGURE 13

NOTES: 3. The A input is connected to V_{CC} during the testing of the Y outputs and to ground during the testing of the Z outputs.
4. The A input is connected to ground during the testing of the Y outputs and to V_{CC} during the testing of the Z outputs.

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
FREQUENCY

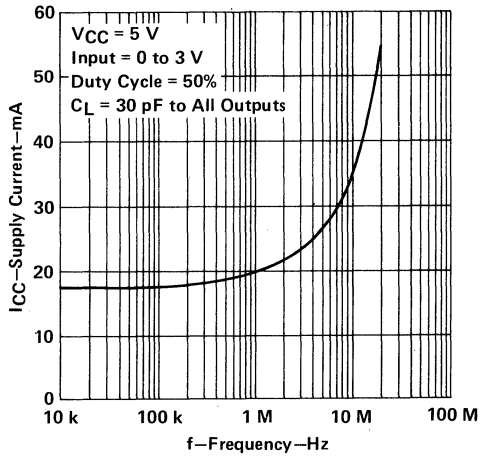

FIGURE 14

TEXAS INSTRUMENTS
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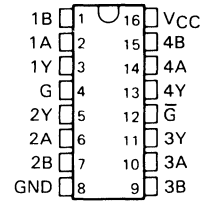
SN75ALS193
QUADRUPLE DIFFERENTIAL LINE RECEIVER WITH 3-STATE OUTPUTS

D2931, JUNE 1986

- Meets EIA Standards RS-422-A, RS-423-A, and RS-485
- Meets CCITT Recommendations V.10, V.11, X.26, and X.27
- Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments
- 3-State Outputs
- Common-Mode Input Voltage Range . . . −7 V to 7 V
- Input Sensitivity . . . ±200 mV
- Input Hysteresis . . . 120 mV Typ
- High Input Impedance . . . 12 kΩ Min
- Operates from Single 5-Volt Supply
- Low I_{CC} Requirements:
  I_{CC} . . . 35 mA Max
- Improved Speed and Power Consumption Compared to AM26LS32A

J DUAL-IN-LINE PACKAGE
(TOP VIEW)



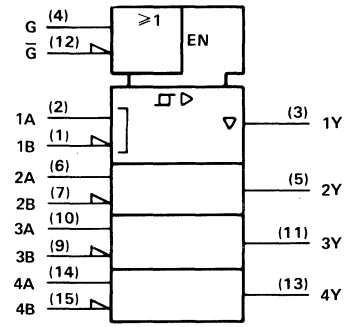
description

The SN75ALS193 is a monolithic quadruple line receiver with three-state outputs designed using Advanced Low-Power Schottky technology. This technology provides combined improvements in bar design, tooling production, and wafer fabrication. This, in turn, provides significantly less power requirements and permits much higher data throughput than other designs. The device meets the specifications of EIA Standards RS-422-A, RS-423-A, and RS-485. It features three-state outputs that permit direct connection to a bus-organized system with a Fail-Safe design that ensures the outputs will always be high if the inputs are open.

The device is optimized for balanced multipoint bus transmission at rates up to 10 megabits per second. The input features high input impedance, input hysteresis for increased noise immunity, and an input sensitivity of ±200 millivolts over a common-mode input voltage range of −7 to 7 volts. It also features active-high and active-low enable functions that are common to the four channels. The SN75ALS193 is designed for optimum performance when used with the SN75ALS192 quadruple differential line driver.

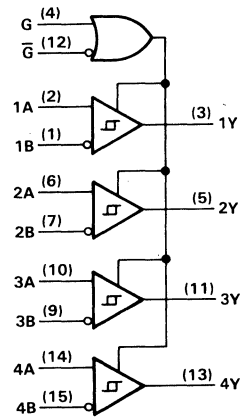
The SN75ALS193 is characterized for operation from 0°C to 70°C.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

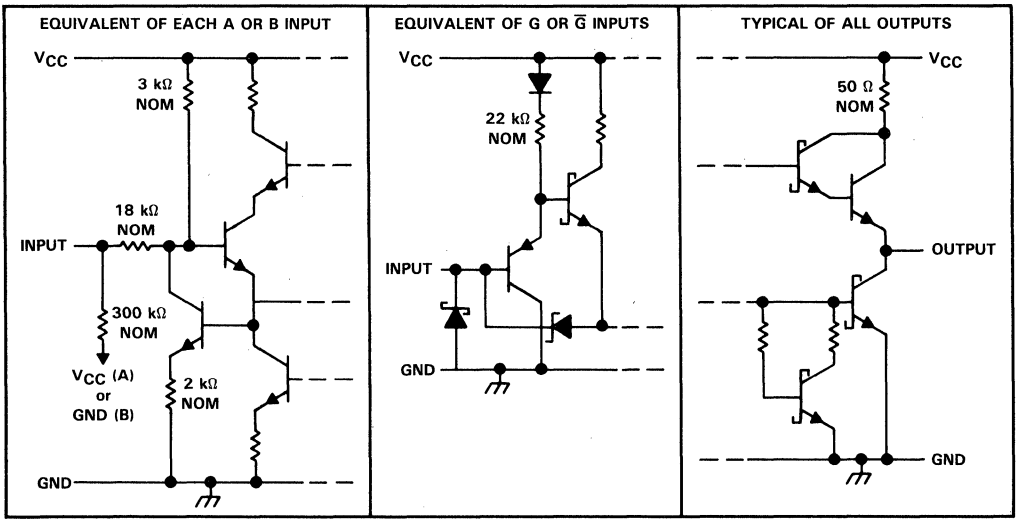


FUNCTION TABLE (EACH RECEIVER)

DIFFERENTIAL A–B	ENABLES G	ENABLES $\overline{G}$	OUTPUT Y
$V_{ID} \geq 0.2$ V	H	X	H
	X	L	H
-0.2 V $< V_{ID} < 0.2$ V	H	X	?
	X	L	?
$V_{ID} \leq -0.2$ V	H	X	L
	X	L	L
X	L	H	Z

H = high level
L = low level
X = irrelevant
? = indeterminate
Z = high-impedance (off)

schematics of inputs and outputs



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, A or B inputs . . . . . ±15 V
Differential input voltage (see Note 2) . . . . . ±15 V
Enable input voltage . . . . . 7 V
Low-level output current . . . . . 50 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3) . . . . . 1025 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds . . . . . 300°C

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.
3. For operation above 25°C free-air temperature, derate to 656 mW at 70°C at the rate of 8.2 mW/°C. In the J package, SN75ALS193 chips are glass mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±7	V
Differential input voltage, V_{ID}			±12	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			−400	μA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended range of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going threshold voltage					200	mV
V_{T-}	Negative-going threshold voltage			−200‡			mV
V_{hys}	Hysteresis§				120		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV,	I_{OH} = −400 μA	2.7	3.6		V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV	I_{OL} = 8 mA			0.45	V
			I_{OL} = 16 mA			0.5	
I_{OZ}	High-impedance-state output current	V_{CC} = 5.25 V	V_O = 2.4 V			20	μA
			V_O = 0.4 V			−20	
I_I	Line input current	Other input at 0 V,	V_I = 15 V		0.7	1.2	mA
		See Note 4	V_I = −15 V		−1.0	−1.7	
I_{IH}	High-level enable-input current		V_{IH} = 2.7 V			20	μA
			V_{IH} = 5.25 V			100	
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				−100	μA
	Input resistance			12	18		kΩ
I_{OS}	Short-circuit output current	V_{ID} = 3 V, See Note 5	V_O = 0,	−15	−78	−130	mA
I_{CC}	Supply current	Outputs disabled			22	35	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the less positive limit is designated minimum, is used in this data sheet for threshold voltage levels only.
§ Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}.

NOTES: 4. Refer to EIA Standard RS-422-A and RS-423-A for exact conditions.
5. Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = −1.5 V to 1.5 V, C_L = 15 pF,			15	22	ns
t_{PHL}	Propagation delay time, high-to-low-level output	See Figure 2			15	22	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See Figure 3		13	25	ns
t_{PZL}	Output enable time to low level				11	25	
t_{PHZ}	Output disable time from high level	C_L = 15 pF,	See Figure 3		13	25	ns
t_{PLZ}	Output disable time from low level				15	22	

TEXAS INSTRUMENTS
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PARAMETER MEASUREMENT INFORMATION

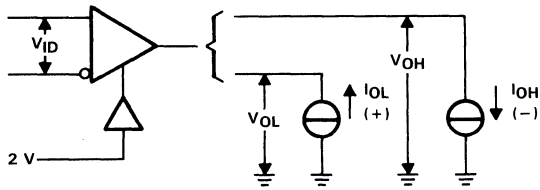
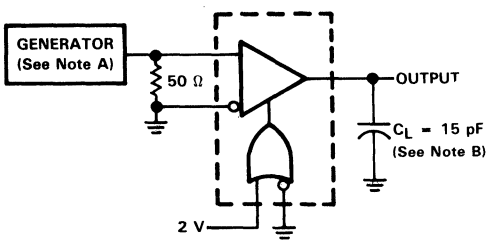
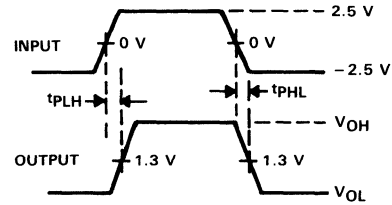


FIGURE 1. V_{OH}, V_{OL}



TEST CIRCUIT

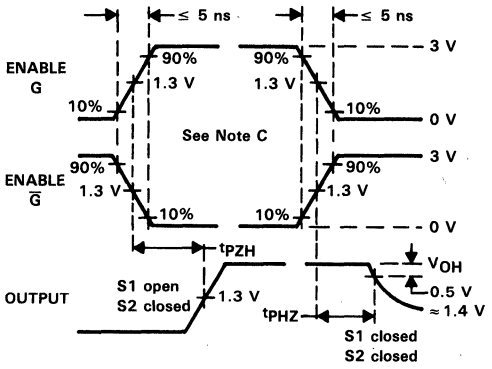


VOLTAGE WAVEFORMS

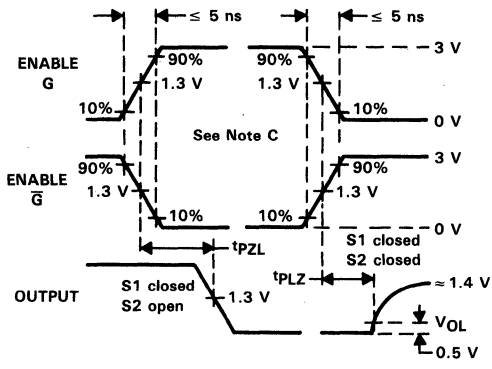
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, Z_{out} = 50 Ω, t_r ≤ 6 ns, t_f ≤ 6 ns.
B. C_L includes probe and jig capacitance.

FIGURE 2. t_{PLH}, t_{PHL}

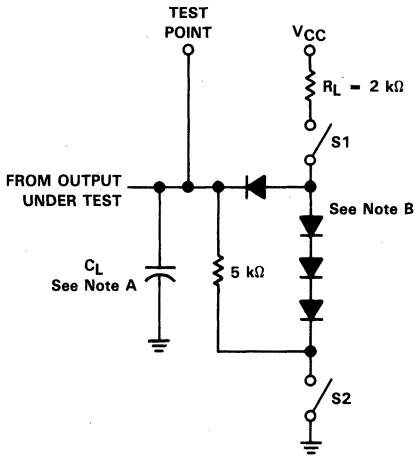
PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS FOR t_{PHZ}, t_{PZH}



VOLTAGE WAVEFORMS FOR t_{PLZ}, t_{PZL}



LOAD CIRCUIT

NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Enable G is tested with $\overline{G}$ high; $\overline{G}$ is tested with G low.

FIGURE 3. t_{PHZ}, t_{PZH}, t_{PLZ}, t_{PZL}

TEXAS INSTRUMENTS
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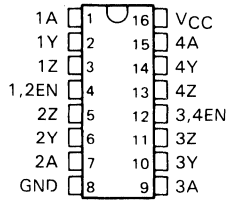
- **Meets EIA Standard RS-422-A**
- **High-Speed ALS Design**
- **3-State TTL-Compatible**
- **Single 5-V Supply Operation**
- **High Output Impedance in Power-Off Condition**
- **Two Pairs of Drivers Independently Enabled**
- **Designed as a Replacement for the MC3487 with Improvements: I_{CC} 50% Lower, Switching Speed 30% Faster**

D, J, OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



FUNCTION TABLE (EACH DRIVER)

INPUT	OUTPUT ENABLE	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	High-Impedance	High-Impedance

H = TTL high level, L = TTL low level, X = irrelevant

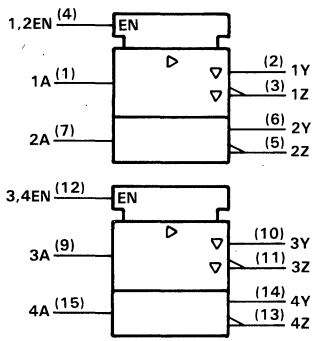
description

This quadruple complementary-output line driver is designed for data transmission over twisted-pair or parallel-wire transmission lines. It meets the requirements of EIA Standard RS-422-A and is compatible with 3-state TTL circuits. Advanced Low-Power Schottky technology provides high speed without the usual power penalty. Standby supply current is typically only 26 milliamperes, while typical propagation delay time is less than 10 nanoseconds and enable/disable times are typically less than 16 nanoseconds.

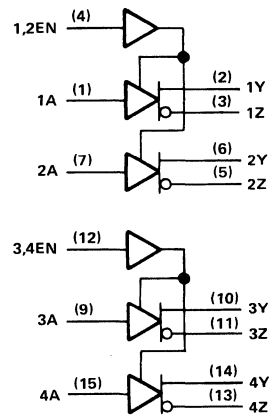
High-impedance inputs keep input currents low, less than 1 microampere for a high level and less than 100 microamperes for a low level. The driver circuits can be enabled in pairs by separate active-high enable inputs. The SN75ALS194 is capable of data rates in excess of 10 megabits per second and is designed to operate with the SN75ALS195 quadruple line receiver.

The SN75ALS194 is characterized for operation from 0°C to 70°C.

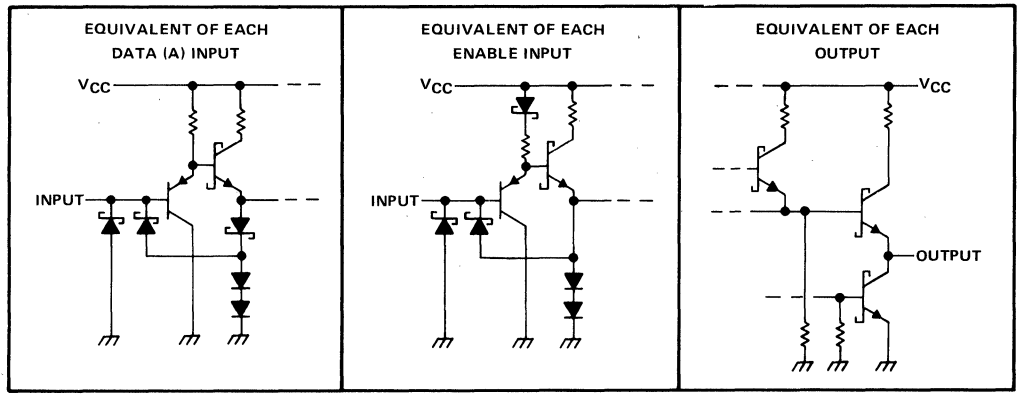
logic symbol



logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, V_I . . . . . 5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2):
D package . . . . . 950 mW
J package . . . . . 1025 mW
N package . . . . . 875 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, refer to the Dissipation Derating Table.

DISSIPATION DERATING TABLE

PACKAGE	T_A = 25°C POWER RATING	DERATING FACTOR	ABOVE T_A	T_A = 70°C POWER RATING
D	950 mW	7.6 mW/°C	25°C	608 mW
J (Glass mount)	1025 mW	8.2 mW/°C	25°C	656 mW
N	875 mW	7.0 mW/°C	25°C	560 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			−20	mA
Low-level output current, I_{OL}			48	mA
Operating free-air temperature, T_A	0		70	°C

TEXAS INSTRUMENTS
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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	I_{OH} = −20 mA		2.5			V
V_{OL}	Low-level output voltage	I_{OL} = 48 mA				0.5	V
VO	Output voltage	I_O = 0		0		6	V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0		2		6	V
$\|V_{OD2}\|$	Differential output voltage	R_L = 100 Ω, See Figure 1		½ V_{OD1}			V
				2			
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage‡					±0.4	V
V_{OC}	Common-mode output voltage					±3	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage‡					±0.4	V
I_O	Output current with power off	V_{CC} = 0	V_O = 6 V			100	μA
			V_O = −0.25 V			−100	
I_{OZ}	High-impedance state output current	Output enables at 0.8 V	V_O = 2.7 V			100	μA
			V_O = 0.5 V			−100	
I_I	Input current at maximum input voltage	V_I = 5.5 V				100	μA
I_{IH}	High-level input current	V_I = 2.7 V				50	μA
I_{IL}	Low-level input current	V_I = 0.5 V				−200	μA
I_{OS}	Short-circuit output current§	V_I = 2 V		−40		−140	mA
I_{CC}	Supply current (all drivers)	V_{CC} = 5.25 V, All outputs disabled			26	45	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDTIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, See Figure 1			6	13	ns
t_{PHL}	Propagation delay time, high-to-low-level output				9	14	ns
	Output-to-output skew				3.5	6	ns
t_{TD}	Differential-output transition time	C_L = 15 pF, See Figure 2			8	14	ns
t_{PZH}	Output enable time to high level	C_L = 50 pF, See Figure 3			9	12	ns
t_{PZL}	Output enable time to low level				12	20	ns
t_{PHZ}	Output disable time from high level				9	14	ns
t_{PLZ}	Output disable time from low level				12	15	ns

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	RS-422-A
V_O	V_{oa}, V_{ob}
$\|V_{OD1}\|$	V_o
$\|V_{OD2}\|$	V_t (R_L = 100 Ω)
$\Delta\|V_{OD}\|$	$\|\|V_t\| - \|\overline{V}_t\|\|$
V_{OC}	$\|V_{os}\|$
$\Delta\|V_{OC}\|$	$\|V_{os} - \overline{V}_{os}\|$
I_{OS}	$\|I_{sa}\|$, $\|I_{sb}\|$
I_O	$\|I_{xa}\|$, $\|I_{xb}\|$

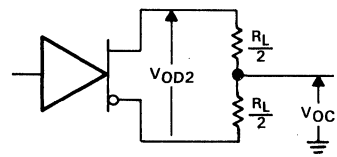

FIGURE 1. DRIVER V_{OD} AND V_{OC}

PARAMETER MEASUREMENT INFORMATION

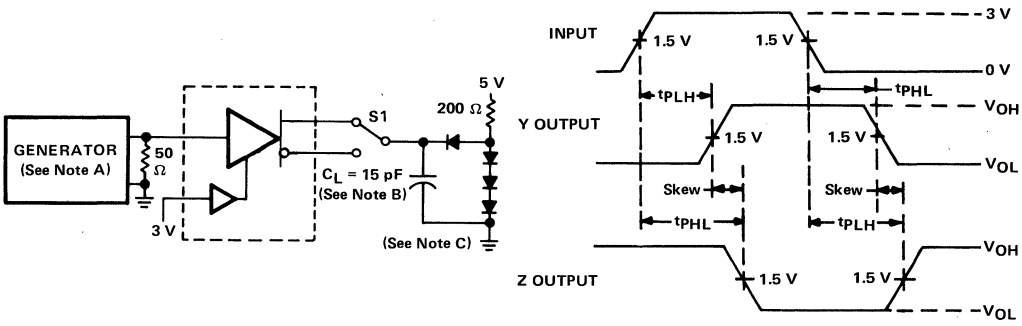

FIGURE 2. PROPAGATION DELAY TIMES

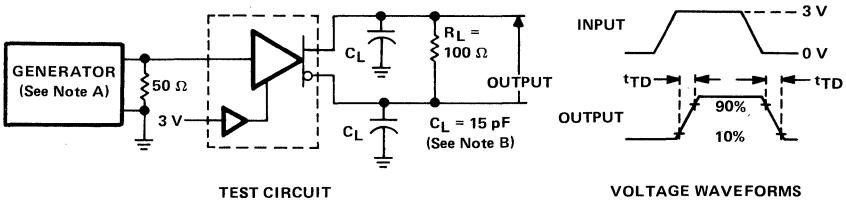

FIGURE 3. DIFFERENTIAL-OUTPUT TRANSITION TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR ≤ 1 MHz, duty cycle = 50%, $Z_O = 50\ \Omega$.
B. C_L includes probe and stray capacitance.
C. All diodes are 1N916 or 1N3064.

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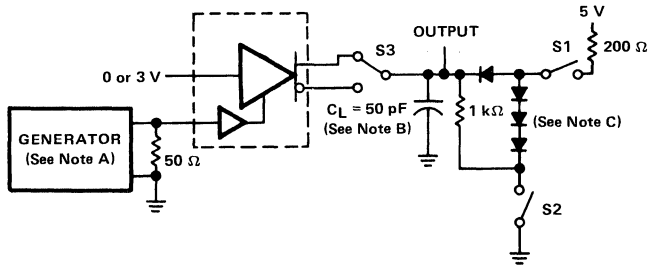
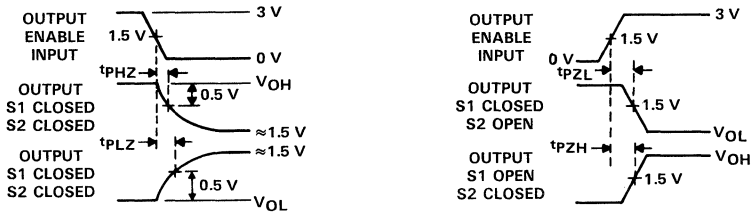
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR ≤ 1 MHz, duty cycle = 50%, Z_O = 50 Ω.
B. C_L includes probe and stray capacitance.
C. All diodes are 1N916 or 1N3064.

FIGURE 4. DRIVER ENABLE AND DISABLE TIMES

TYPICAL CHARACTERISTICS

Y OUTPUT VOLTAGE
vs
DATA INPUT VOLTAGE

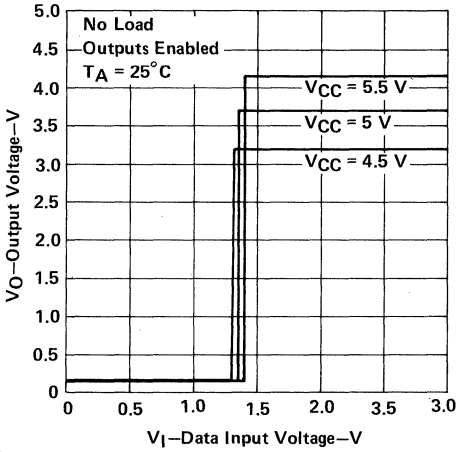


FIGURE 5

Y OUTPUT VOLTAGE
vs
DATA INPUT VOLTAGE

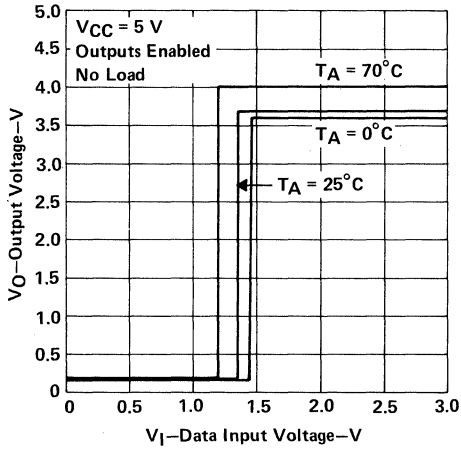


FIGURE 6

Y OUTPUT VOLTAGE
vs
ENABLE G INPUT VOLTAGE

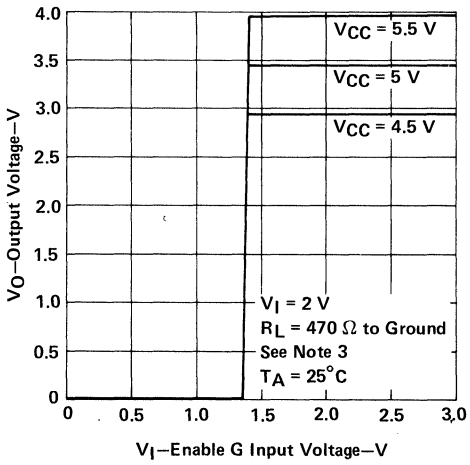


FIGURE 7

Y OUTPUT VOLTAGE
vs
ENABLE G INPUT VOLTAGE

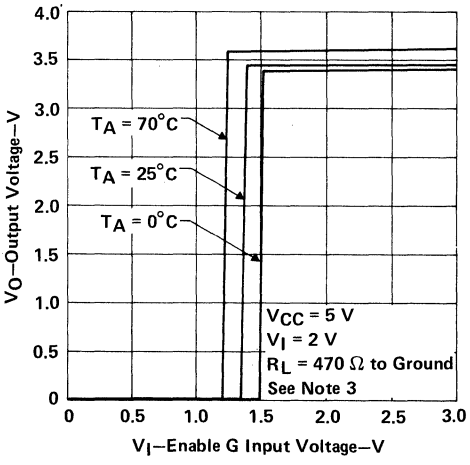


FIGURE 8

NOTE 3: The A input is connected to V_{CC} during the testing of the Y outputs and to ground during the testing of the Z outputs.

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TYPICAL CHARACTERISTICS

Z OUTPUT VOLTAGE
vs
ENABLE G INPUT VOLTAGE

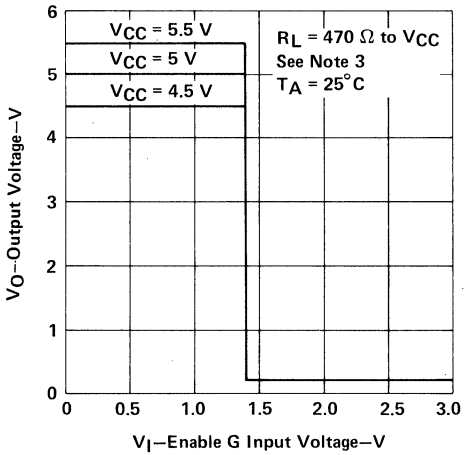

FIGURE 9

Z OUTPUT VOLTAGE
vs
ENABLE G INPUT VOLTAGE

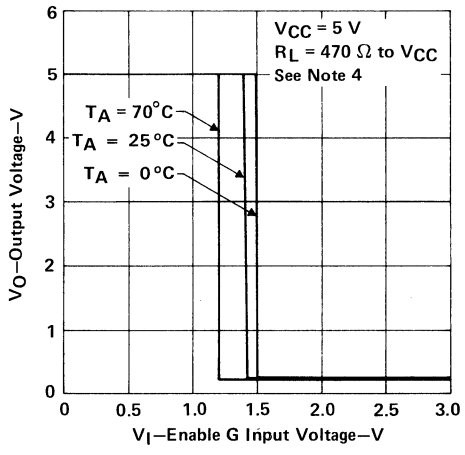

FIGURE 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

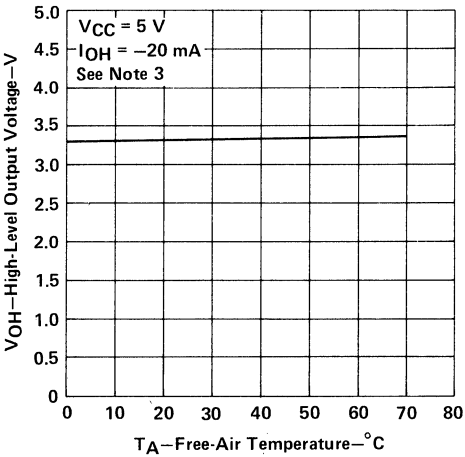

FIGURE 11

HIGH-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

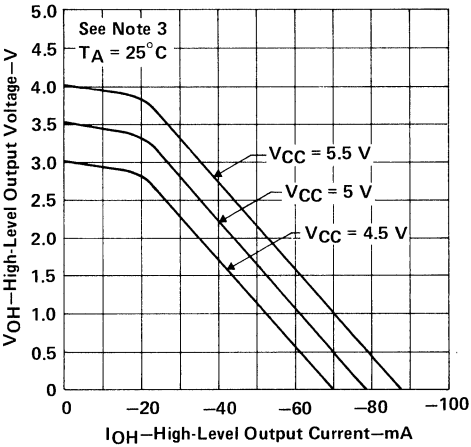

FIGURE 12

NOTES: 3. The A input is connected to V_{CC} during the testing of the Y outputs and to ground during the testing of the Z outputs.
4. The A input is connected to ground during the testing of the Y outputs and to V_{CC} during the testing of the Z outputs.

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

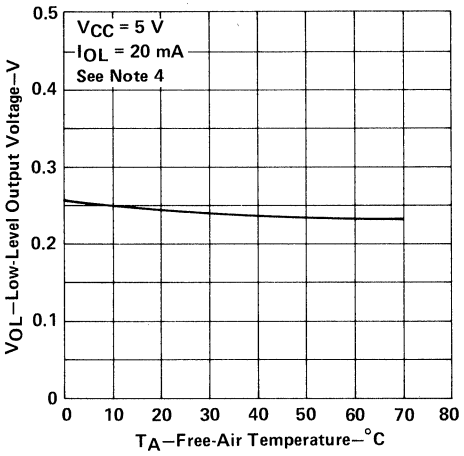

FIGURE 13

LOW-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

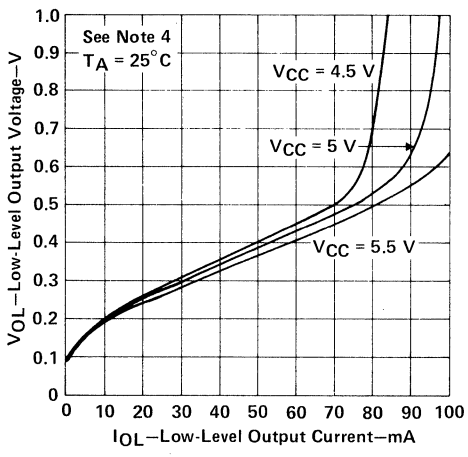

FIGURE 14

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

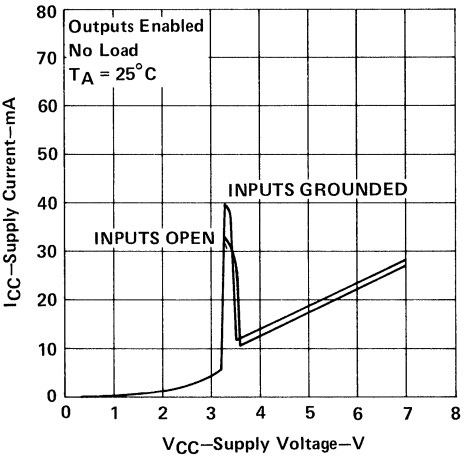

FIGURE 15

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

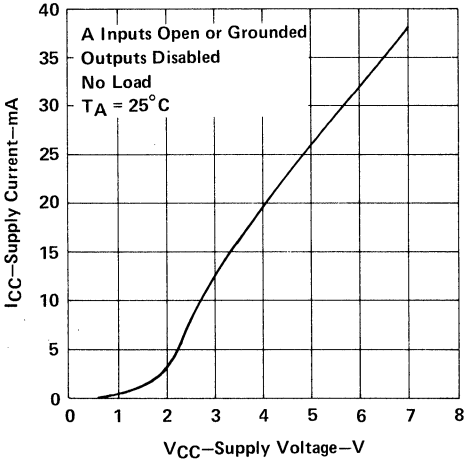

FIGURE 16

NOTE 4: The A input is connected to ground during the testing of the Y outputs and to V_{CC} during the testing of the Z outputs.

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TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
FREQUENCY

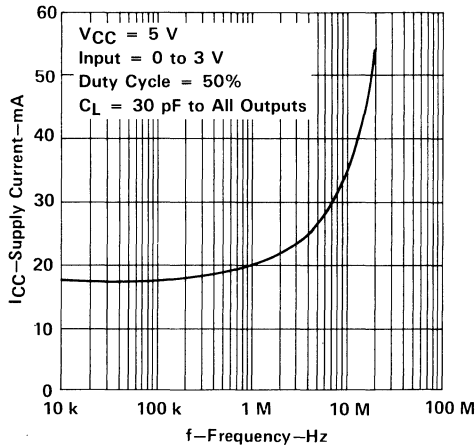


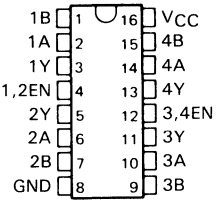
FIGURE 17

SN75ALS195
QUADRUPLE DIFFERENTIAL LINE RECEIVER WITH 3-STATE OUTPUTS

D2928, JUNE 1986

- Meets EIA Standards RS-422-A, RS-423-A, and RS-485
- Meets CCITT Recommendations V.10, V.11, X.26, and X.27
- −7 V to 7 V Common-Mode Range with 200-mV Sensitivity
- 3-State TTL-Compatible Outputs
- High Input Impedance . . . 12 kΩ Min
- Input Hysteresis . . . 120 mV Typ
- Single 5-V Supply Operation
- Low Supply Current Requirement . . . 35 mA Max
- Improved Speed and Power Consumption Compared to MC3486

J PACKAGE
(TOP VIEW)



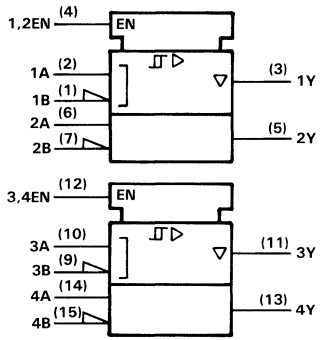
description

The SN75ALS195 is a monolithic quadruple line receiver with three-state outputs designed using Advanced Low-Power Schottky technology. This technology provides combined improvements in bar design, tooling production, and wafer fabrication, providing significantly less power consumption and permitting much higher data throughput than other designs. The device meets the specifications of EIA Standards RS-422-A, RS-423-A and RS-485.

The SN75ALS195 features three-state outputs that permit direct connection to a bus-organized system with a fail-safe design that ensures the outputs will always be high if the inputs are open. The device is optimized for balanced multipoint bus transmission at rates up to 10 megabits per second. The input features high input impedance, input hysteresis for increased noise immunity, and an input sensitivity of ±200 millivolts over a common-mode input voltage range of ±7 volts. It also features an active-high enable function for each of two receiver pairs. The SN75ALS195 is designed for optimum performance when used with the SN75ALS194 quadruple differential line driver.

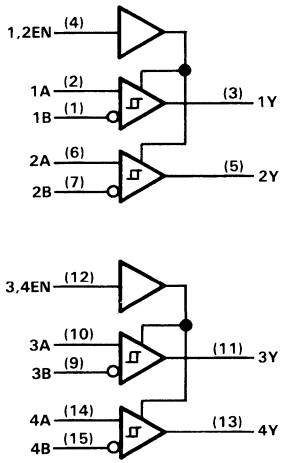
The SN75ALS195 is characterized for operation from 0°C to 70°C.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram

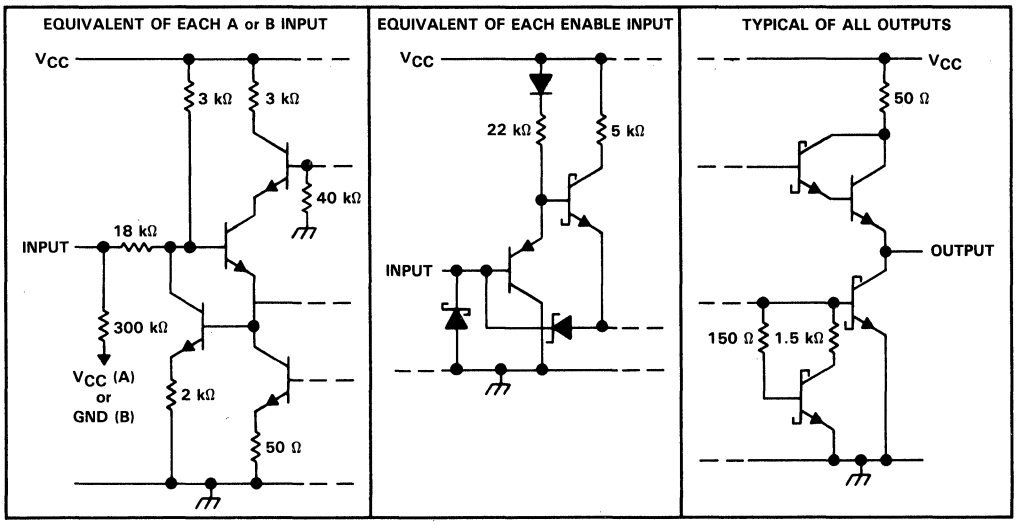


FUNCTION TABLE (EACH RECEIVER)

DIFFERENTIAL A–B	ENABLES G	ENABLES $\overline{G}$	OUTPUT Y
$V_{ID} \geq 0.2$ V	H	X	H
	X	L	H
-0.2 V $< V_{ID} < 0.2$ V	H	X	?
	X	L	?
$V_{ID} \leq -0.2$ V	H	X	L
	X	L	L
X	L	H	Z

H = high level
L = low level
X = irrelevant
? = indeterminate
Z = high-impedance (off)

schematics of inputs and outputs



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, A or B inputs, V_I . . . . . −25 V to ±15 V
Differential input voltage (see Note 2) . . . . . −25 V to ±15 V
Enable input voltage . . . . . 7 V
Low-level output current . . . . . 50 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3) . . . . . 1025 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.
3. For operating above 25°C free-air temperature, derate the J package to to 656 mW at 70°C at the rate of 8.2 mW/°C. In the J package, SN75ALS195 chips are glass mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±7	V
Differential input voltage, V_{ID}			±12	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			−400	μA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going threshold voltage					200	mV
V_{T-}	Negative-going threshold voltage			−200‡			mV
V_{hys}	Hysteresis§				120		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV,	I_{OH} = −400 μA	2.7	3.6		V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV	I_{OL} = 8 mA			0.45	V
			I_{OL} = 16 mA			0.5	
I_{OZ}	High-impedance state output current	V_{IL} = 0.8 V, V_O = 2.7 V	V_{ID} = −3 V,			20	μA
		V_{IL} = 0.8 V, V_O = 0.5 V	V_{ID} = 3 V,			−20	
I_I	Line input current	Other input at 0 V, See Note 4	V_I = 15 V		0.7	1.2	mA
			V_I = −15 V		−1.0	−1.7	
I_{IH}	High-level enable-input current		V_{IH} = 2.7 V			20	μA
			V_{IH} = 5.25 V			100	
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				−100	μA
	Input resistance			12	18		kΩ
I_{OS}	Short-circuit output current	V_{ID} = 3 V, See Note 5	V_O = 0,	−15	−78	−130	mA
I_{CC}	Supply current	Outputs disabled			22	35	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the less positive limit is designated minimum, is used in this data sheet for threshold voltage levels only.
§ Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}.

NOTES: 4. Refer to EIA Standard RS-422-A and RS-423-A for exact conditions.
5. Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = −1.5 V to 1.5 V, C_L = 15 pF,			15	22	ns
t_{PHL}	Propagation delay time, high-to-low-level output	See Figure 2			15	22	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See Figure 3		13	25	ns
t_{PZL}	Output enable time to low level				11	25	
t_{PHZ}	Output disable time from high level	C_L = 15 pF,	See Figure 3		13	25	ns
t_{PLZ}	Output disable time from low level				15	22	

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PARAMETER MEASUREMENT INFORMATION

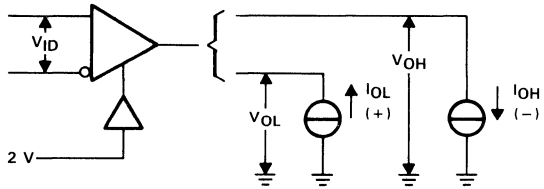
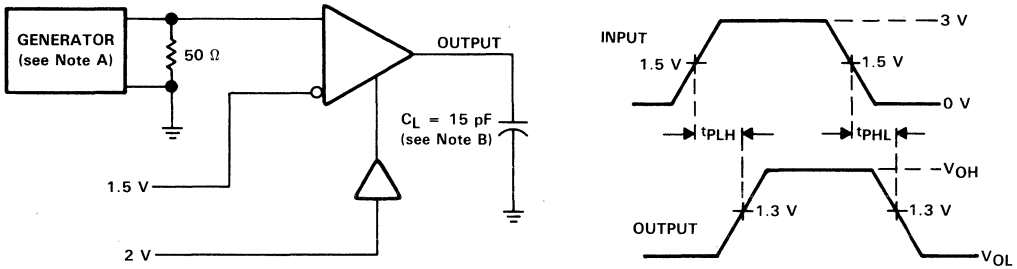
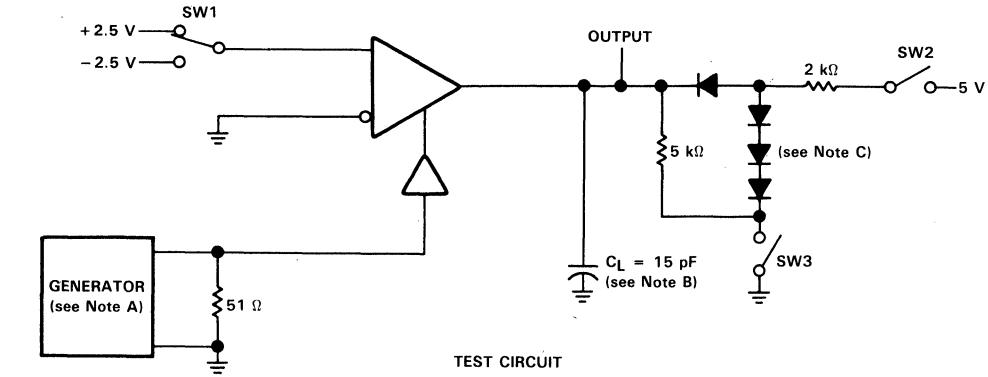


FIGURE 1. V_{OH}, V_{OL}

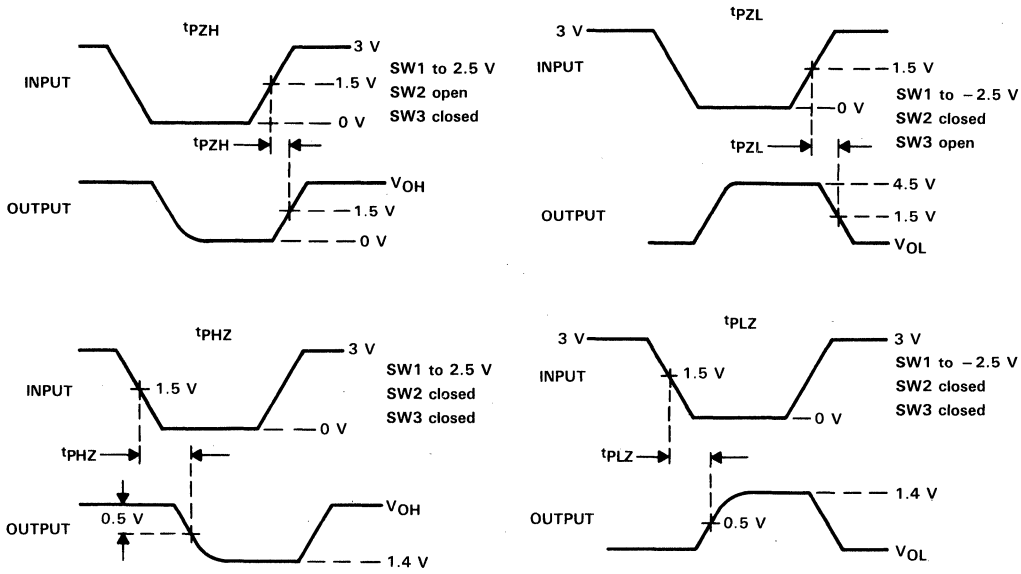


NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, Z_{out} = 50 Ω, t_r ≤ 6 ns, t_f ≤ 6 ns.
B. C_L includes probe and jig capacitance.

FIGURE 2. PROPAGATION DELAY TIMES



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, Z_{out} = 50 Ω, t_r ≤ 6 ns, t_f ≤ 6 ns.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.

FIGURE 3. ENABLE AND DISABLE TIMES

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Advanced Schottky Family

TEXAS INSTRUMENTS

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Advanced Schottky Family (ALS/AS) Application

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List of Illustrations

List of Illustrations (Continued)

List of Tables

INTRODUCTION

The purpose of this Application Report is to assist the designers of high-performance digital logic systems in the use of the new series of Advanced Schottky-clamped* TTL integrated circuits.

Detailed electrical characteristics of these devices are provided and, if available, tables have been included that compare specific parameters of the devices with those of other logic families. In addition, interfamily information is provided to allow system designers to mix logic families in the same circuit. This allows the designer to use the relative merits of each logic family in high preformance state-of-the-art designs.

The major subject areas covered in this Application Report are as follows:

- Advanced Schottky process
- Fanouts
- Transfer characteristics
- Input and output parameters
- Speed and power information
- Noise margins
- Power supply considerations
- Noise sources and their abatement
- Back panel and printed circuit wiring guidelines
- Line driving and receiving

INTRODUCTION TO ADVANCED SCHOTTKY-CLAMPED TTL

Series 54/74 transistor-transistor logic (TTL) has, since its introduction in 1965, become the most popular digital integrated circuit logic family ever offered. Its popularity has allowed the development of high-volume production techniques which have made it the most economical approach to the implementation of major portions of medium-to-high performance digital logic systems. These systems range from simple decision making to highly complex real-time computer installations that handle worldwide data processing.

The proliferation of and economical impact of these digital logic systems has created a demand for constant improvement in efficiency. In response to demand, Texas Instruments examined the advantages gained by Schottky clamping. An increase in speed and performance was discovered in the use of Schottky barrier-diode clamping. The process was patented in the United States and the Schottky series 54S/74S catalog parts were made available in the early 1970s. A series 54LS/74LS was introduced later. The series 54LS/74LS was slower that the 54S/74S series but had a much lower power consumption.

*Integrated Schottky-Barrier-diode-clamped transistor is patented by Texas Instruments Incorporated, U.S. Patent Number 3,463,975.

Recent innovations in integrated circuit design have made it possible to develop two new families: the Advanced Schottky (54AS/74AS) series and the Advanced Low-Power Schottky (54ALS/74ALS) series. The 'ALS and 'AS series provide considerable higher speeds than the 'LS and 'S series, respectively. The 'ALS series offers a substantial reduction in power consumption over the 'LS series, and the 'AS series offers a substantial reduction in power consumption over the 'S series. The 'ALS/'AS series is pin-to-pin compatible with the 'LS/'S series.

SPEED-POWER SLOTS FILLED BY 'ALS AND 'AS TTL

Digital integrated circuits have historically been characterized for both speed and power. The series 54S/74S devices contain 19 mW NAND gates and 125-MHz flip-flops and the series 54LS/74LS devices contain 2-mW NAND gates and 45-MHz flip-flops. Either of these logic families could be used to design a 2-MHz system, therefore categorization strictly on the basis of power and speed is inconclusive with respect to system efficiency. To provide a means of measuring the overall circuit efficiency and performance, a speed-power product efficiency index for integrated circuits was developed. The rating of an integrated circuit is obtained by multiplying the gate propagation delay by the gate power dissipation.

Table 1 provides propagation delay times, power dissipation, and speed-power product for the Texas Instruments TTL series. In addition, it provides flip-flop frequency for each family as an indicator of system performance. The speed-power product rating system (measured in picojoules) is divided into circuits where speed is the prime factor and circuits where low-power is the prime factor. The 'ALS series speed-power product is approximately 4 times less than that of the 'LS series and the 'AS series speed-power product is approximately 4 times less than the 'S series. Figure 1 is a graphic analysis of the speed-power points for the various TTL families.

ADDITIONAL ADVANTAGES OFFERED BY 'ALS AND 'AS DEVICES

The 'ALS and 'AS devices offer the following additional advantages:

1. TTL compatible with 54/74, 54S/74S, 54L/74L, 54LS/74LS, and 54H/74H series gates for selectively upgrading existing systems
2. Suppresses the effects of line ringing and significantly reduces undershoot
3. Higher thresholds (noise immunity) and better stability across operating free-air temperature range
4. Input current requirement reduced by up to 50%

Table 1. Typical Performance Characteristics by TTL Series

CIRCUIT TECHNOLOGY	MINIMIZING POWER					MINIMIZING DELAY TIME				
	FAMILY	PROP DELAY (ns)	PWR DISS (mW)	SPD/PWR PRODUCT (pJ)	MAXIMUM FLIP-FLOP FREQ (MHz)	FAMILY	PROP DELAY (ns)	PWR DISS (mW)	SPD/PWR PRODUCT (pJ)	MAXIMUM FLIP-FLOP FREQ (MHz)
Gold Doped	TTL	10	10	100	35	TTL	10	10	100	35
	L TTL	33	1	33	3	H TTL	6	22	132	50
Schottky Clamped	LS TTL	9	2	18	45	S TTL	3	19	57	125
	'ALS	4	1.2	4.8	70	'AS	1.7	8	13.6	200

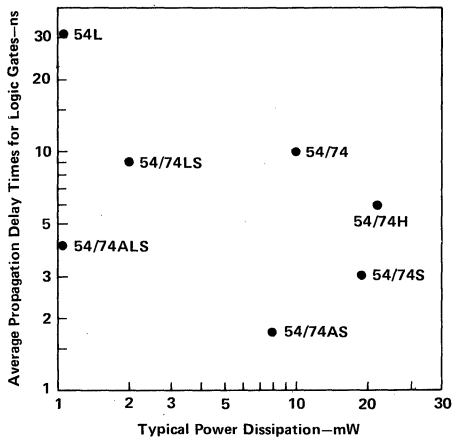


Figure 1. Speed-Power Relationships of Digital Integrated Circuits

5. Fanout is doubled
6. Terminated lines or controlled impedance circuit boards are normally not required.
7. The 'AS series offers shorter propagation delays and higher clock frequencies with relatively low power consumption.
8. The maximum flip-flop frequency has been increased to 200 MHz.

CONCEPTS OF DEFINING SERIES 'AS AND 'ALS

Both the 'ALS and 'AS series are electrically and pinout compatible with existing TTL series. The 'ALS series is suitable for replacing all TTL families except in the very highest frequency applications. Replacement with 'ALS will result in lower power consumption, smaller power supply current spikes, and, in some cases, better noise immunity than the other families. In those cases where a very high operating frequency is required, the 'AS series can be used. The 'AS devices require less than one-half of the supply current of the 'S series and has approximately twice the clocking frequency. The 'ALS devices are ideal for improving effeciency at the lower speeds. The 'AS devices are ideal for replacement of high-speed logic families including ECL 10K series.

Compatibility With Other TTL Families

To ensure complete electrical compatibility in systems using or intending to use a mixture of existing TTL families and the new 'ALS/'AS families, specific guidelines have been implemented. These guidelines ensure the continuation of desirable characteristics and incorporate newer techniques to improve performance and/or simplify the use of TTL families. Figure 2 illustrates the comparison of essential parameters of each family and shows that complete compatibility is maintained throughout the 54/74 families.

Fanout

The compatible ratings for fanout simplify the implementation of logic and provide a freedom of choice in the use of any of the seven performance ranges to design a digital logic system. Any of the Texas Instruments TTL series gates can be used to drive any other gate without the use of an interface or level-shifting circuit. The use of totem-pole-(push-pull) type output stages provides a low output impedance and the capability for both sourcing and sinking current. The output is easily adapted for driving MOS and CMOS circuits as well as the interface circuits between the output and the devices it controls. Figure 3 illustrates fanout capability.

USING THE SCHOTTKY BARRIER DIODE

The Advanced Schottky Family has been developed from two earlier concepts: the Baker Clamp and the Schottky Barrier-Diode (SBD). The use of the Baker Clamp and SBD concepts resulted in the Schottky Clamped Transistor. The Schottky clamped transistor produced the increased switching speed associated with the S series integrated circuits. The additional advances that have led to the development of 'ALS and 'AS gates and the actual gates are discussed later.

Analysis of the Schottky Clamped Transistor

The use of the Baker Clamp, shown in Figure 4, is a method of avoiding saturation of a discrete transistor. The diode forward voltage is 0.3 V to 0.4 V as compared to 0.7 V for the base-emitter junction diode. When the transistor is turned on, base current drives the transistor toward

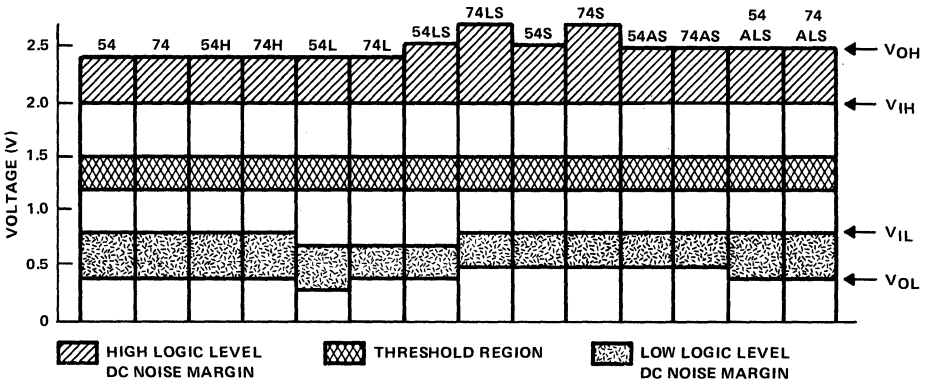


Figure 2. Series 54/74 TTL Family Compatible Levels Showing DC Noise Margins

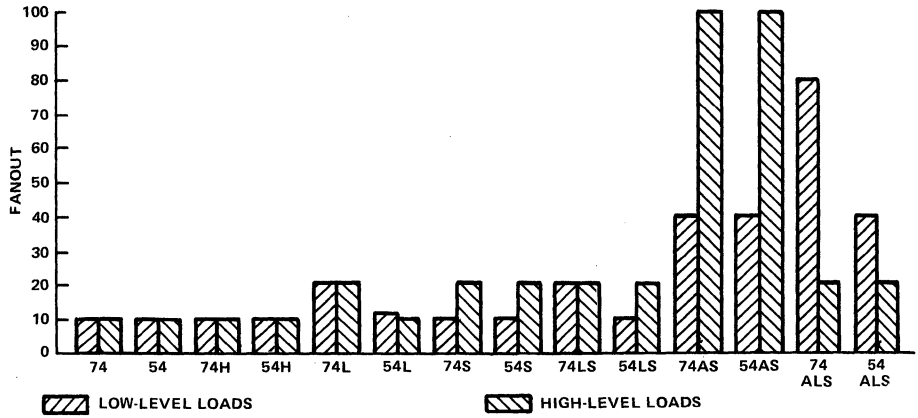


Figure 3. Fanout Capability

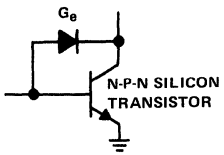


Figure 4. Baker Clamp

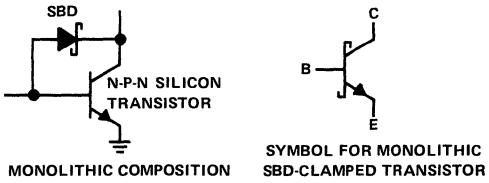


Figure 5. The Schottky-Clamped Transistor

saturation. The collector voltage drops, the germanium diode begins to conduct forward current, and excess base drive is diverted from the base-collector junction of the transistor. This causes the transistor to be held out of deep saturation, the excess base charge to not be stored, and the turn-off time to be dramatically reduced.

A germanium diode cannot be incorporated into a monolithic silicon integrated circuit. Therefore, the germanium diode must be replaced with a silicon diode which has a lower forward voltage drop than the base-collector junction of the transistor. A normal p-n diode will not meet this requirement. The SBD illustrated in Figure 5 can be used to meet the requirement.

The SBD illustrated in Figure 6 is a rectifying metal-semiconductor contact formed between a metal and a highly doped N semiconductor.

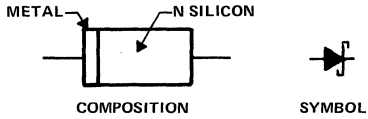


Figure 6. Schottky Barrier-Diode

The qualitative physics of an SBD is illustrated in Figure 7. The valence and conduction bands in a metal overlap make available a large number of free-energy states. The free-energy states can be filled by any electrons which are injected into the conduction band. A finite number of electrons exist in the conduction band of a semiconductor. The number of electrons depends mainly upon the thermal energy and the level of impurity atoms in the material. When a metal-semiconductor junction is formed, free electrons flow across the junction from the semiconductor, via the conduction band, and fill the free-energy states in the metal. This flow of electrons builds a depletion potential across the barrier. This depletion potential opposes the electron flow and, eventually, is sufficient to sustain a balance where there is no net electron flow across the barrier.

Under forward bias (metal positive), there are many electrons with enough thermal energy to cross the barrier potential into the metal. This forward bias is called "hot injection." Because the barrier width is decreased as forward bias V_F increases, forward current will increase rapidly with an increase in V_F.

When the SBD is reverse biased, electrons in the semiconductor require greater energy to cross the barrier. However, electrons in the metal see a barrier potential from the side essentially independent of the bias voltage and a small net reverse current will flow. Since this current flow is relatively independent of the applied reverse bias, the reverse current flow will not increase significantly until avalanche breakdown occurs.

A simple metal-n semiconductor collector contact is an ohmic contact while the SBD contact is a rectifying contact. The difference is controlled by the level of doping in the semiconductor material. As the doping is increased, the contact becomes more ohmic. Figure 8 illustrates the current-voltage characteristics according the doping applied.

Current in the SBD is carried by majority carriers. Current in the p-n junction is carried by minority carriers. The resultant minority carrier storage causes the switching

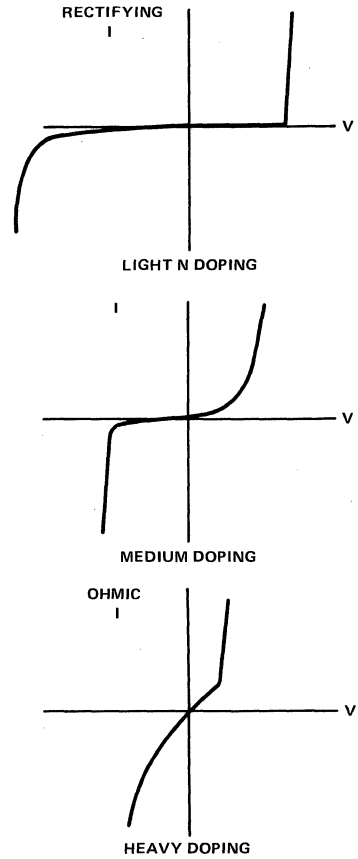


Figure 8. Metal-N Diode Current-Voltage Characteristics

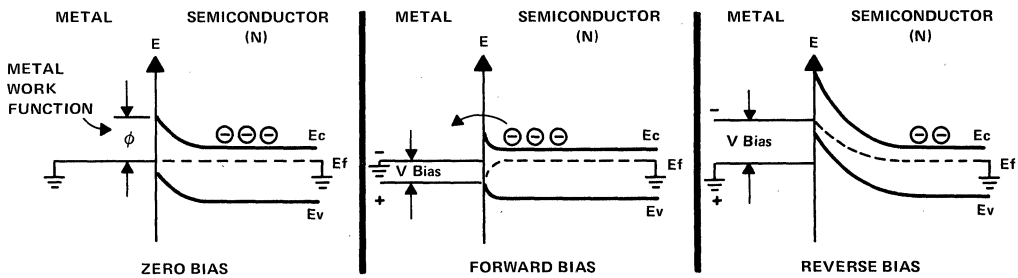


Figure 7. Schottky Barrier-Diode Energy Diagrams

time of a p-n junction to be limited when switched from forward bias to reverse bias. A p-n junction is inherently slower than an SBD even when doped with gold.

Another major difference between the SBD and p-n junction is the forward voltage drop. For diodes of the same surface area, the SBD will have a larger forward current at the same forward bias regardless of the type of metal used. The SBD forward voltage drop is lower at a given current than a p-n junction. Figure 9 illustrates the current carriers and forward current-voltage characteristics differences between the SBD and p-n junction. The SBD meets the requirements of a silicon diode which will clamp a silicon n-p-n transistor out of saturation.

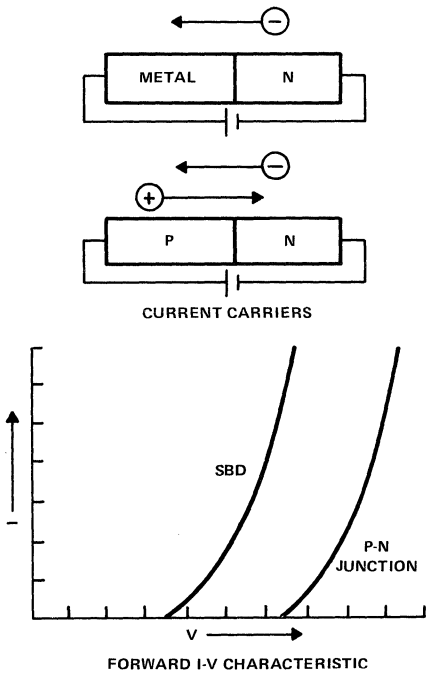


Figure 9. Differences Between P-N and Schottky Barrier-Diodes

The Advanced Schottky process differs from the Schottky process in that it uses ion implantation of impurities instead of diffusion. Ion implantation gives greater control on the depth of doping and resolution. Because of a thinner epitaxial layer and smaller all around geometries, smaller parasitic capacitances are encountered. The performance of the SBD is also enhanced by the use of oxide isolation of the transistors. This reduces the collector-substrate capacitance. Figure 10 illustrates the 'LS/'S process which consists of conventional masks, junction isolation, and a

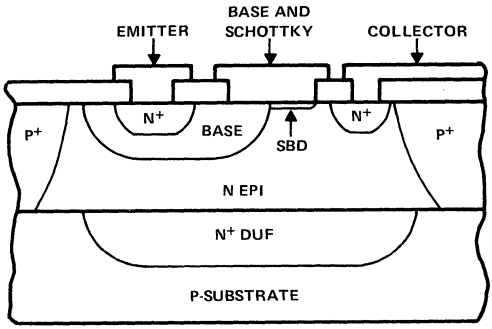


Figure 10. Standard Process ('LS/'S)

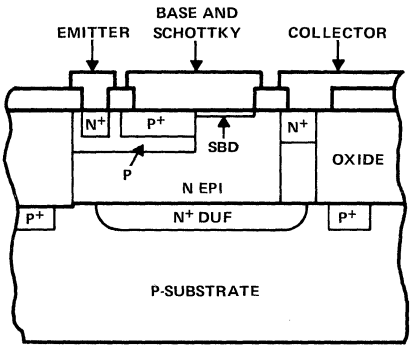


Figure 11. Advanced Process ('ALS/'AS)

standard metal system and Figure 11 illustrates the 'ALS/'AS process which consists of composed masks, ion implantation, oxide isolation, and a standard metal system.

Analysis of 'ALS and 'AS NAND Gates

The 'ALS and 'AS NAND gates in Figures 12 and 13 combine the desirable features of improved TTL circuits with the technological advantages of full Schottky clamping, ion implantation, and oxide isolation to achieve very fast switching times at a reduced speed-power product. The improvements and advantages are as follows:

1. Full Schottky clamping of all saturating transistors virtually eliminates storing excessive base charge and significantly enhances turn-off time of the transistors.
2. Elimination of transistor storage time provides stable switching times across the temperature range.
3. An active turn-off is added to square up the transfer characteristic and provide an improved high-level noise immunity.

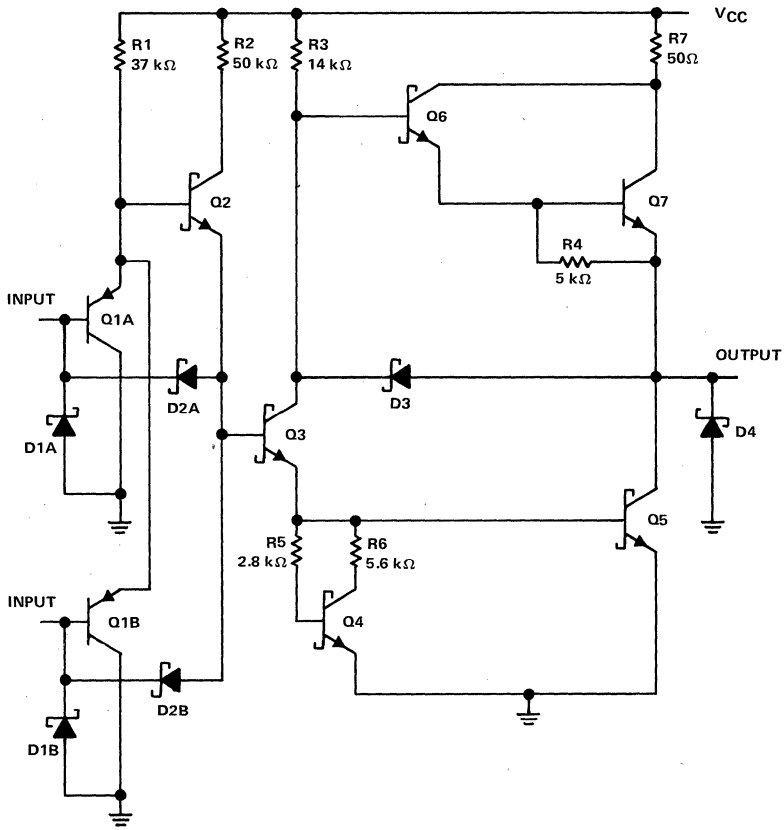


Figure 12. 'ALS00A NAND Gate Schematic

4. Input and output clamping is implemented with Schottky diodes to reduce negative-going excursions on the inputs and outputs. Because of its lower forward voltage drop and fast recovery time, the Schottky input diode provides improved clamping action over a conventional p-n junction diode.
5. The ion implantation process allows small geometries giving less parasitic capacitances so that switching times are decreased.
6. The reduction of the epi-substrate capacitance using oxide isolation also decreases switching times.

A key feature of the 'ALS and 'AS families is the improvement in typical input-threshold voltage. Figure 12 is a schematic diagram of the 'ALS00A NAND gate. Figure 13 is a schematic diagram of the 'AS00 NAND gate. The input threshold voltage of the devices is determined by the equation:

$$VT = V_{BE} \text{ of Q2} + V_{BE} \text{ of Q3} + V_{BE} \text{ of Q5} - V_{BE} \text{ of Q1A (or } V_{BE} \text{ of Q1B)} \quad (1)$$

From Eq. (1) it can be determined that the input threshold voltage is two times V_{BE} or approximately 1.4 V. Low-level input current I_{IL} is reduced in the 'ALS00A/'AS00 gates because of the improved input circuits. Buffering by transistors Q1A (or Q1B) and Q2 causes a significant reduction in low-level input current. Low-level input current is determined by the equation:

$$I_{IL} = V_{CC} - V_{BE} \text{ of Q1A} - V_I/[R(h_{FE} \text{ of Q1A} + 1)] \quad (2)$$

By using Eq. (2) low-level input current is reduced by at least the factor of h_{FE} of Q1A + 1 and is typically -10 μA for the 'ALS00A and -50 μA for the 'AS00. High-level output voltage V_{OH} is determined primarily by V_{CC},

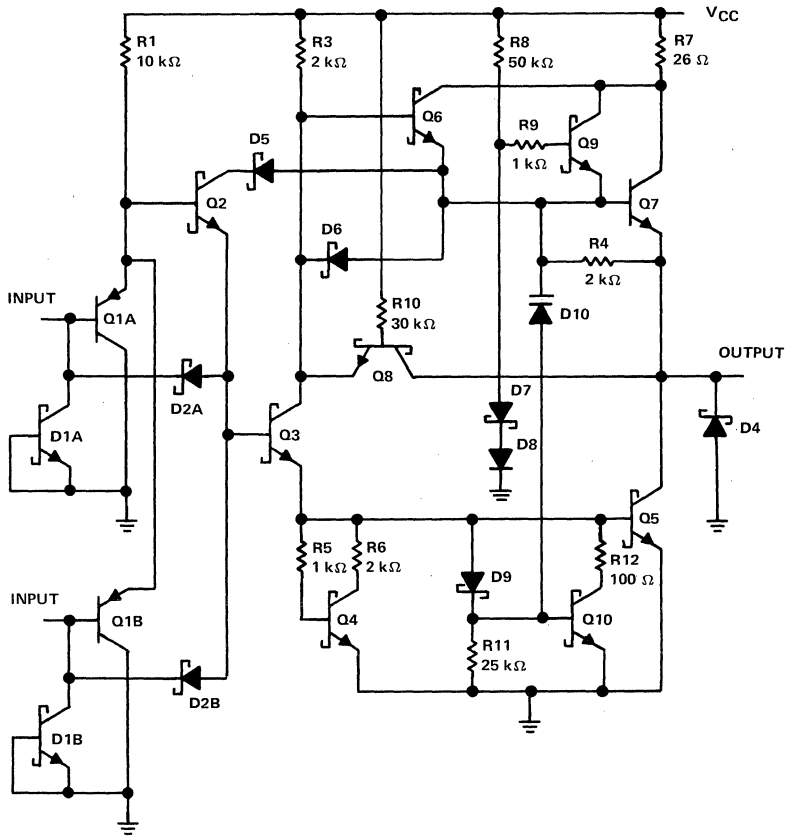


Figure 13. 'AS00 NAND Gate Schematic

resistors R4 and R7, and transistors Q6 and Q7. With no load, the high-level output voltage is approximately equal to $V_{CC} - V_{BE}$ of Q6 because the voltage across resistor R4 is 0 V. For medium-level currents, the high-level output voltage is equal to $V_{CC} - V_{BE}$ of Q6 $- V_{BE}$ of Q7 because of the Darlington gain of transistors Q6 and Q7. The current through resistor R3 is typically less than 1 μA and, therefore, the voltage drop is negligible. As conduction through transistors Q6 and Q7 is increased, the voltage drop across limiting resistor R7 will increase until the Schottky clamping diode of transistor Q6 starts to become forward biased. At this point, the current through resistor R3 (and the voltage drop) is no longer negligible and the high-level output voltage is determined by:

$$V_{OH} = V_{CC} - I_{OH \text{ through } R7} \times R7 - V_{CE} \text{ of Q6} - V_{BE} \text{ of Q7} \quad (3)$$

Low-level output voltage V_{OL} is determined by the turning on of transistor Q5. When the input is high and transistor Q2 is turned on, high-current transistor Q5 is turned on by a current path through transistor Q3 and resistor R3. Sufficient base drive is supplied to keep transistor Q5 fully turned on at an apparent output resistance of 14 Ω for 'ALS and 6Ω for 'AS.

The fanout is up to 40 for a '54ALS device that is driving a '54ALS device and up to 80 for a '74ALS device, that is driving a '74ALS device and provides a guaranteed low-level output current of 4 mA and 8 mA, respectively.

The increase in speed-power product of '54ALS/'74ALS devices, a factor four times better than '54LS/'74LS devices, is due to the design consideration of the quiescent and switching operations of the circuit. In the quiescent state, transistor Q2 allows the use of a reduced low-level input current. This reduces the fanout and reduces the overall quiescent current requirements.

The design of diodes D2 and D3 (or transistor Q8) and transistor Q4 enhances the speed-power product of the device. Transistor Q4 reduces the turn-off time and consequently the current transients caused by conduction

overlap of transistor Q5. The same principle is used by diodes D2 and D3 and transistor Q3 in turning off transistor Q7. In addition, the active turn-off design produces a square transfer characteristic.

The 'AS00 gate has additional circuits not on the 'ALS00A gate. The circuits are added to enhance the throughput of the 'AS Family.

Transistor Q10 has been added as a discharge path for the base-collector capacitance of transistor Q5. Without transistor Q10, rising voltages at the collector of transistor Q5 would force current, via the base-collector capacitance, into the base of transistor Q5 causing it to turn on. However, diode D10 causes transistor Q10 to turn on (during rising voltage) and keeps transistor Q5 turned off. Diodes D6 and D9 serve as a discharge path for capacitor-diode D10.

CIRCUIT PARAMETERS

Worst-case testing of 'ALS/'AS devices provides a margin of safety. [All dc limits shown on the data sheet are guaranteed over the entire temperature range (−55 °C to 125 °C) for series 54ALS/54AS and 0 °C to 70 °C for series 74ALS/74AS)]. In addition, the dc limits are guaranteed over the entire supply voltage range (4.5 V to 5.5 V).

Transfer Characteristics

Since the most common application for a logic gate is to drive a similar logic gate, the input and output logic levels must be compatible. The input and output logic levels for 'ALS/'AS devices are as follows:

- V_{IL} — The voltage value required for a low-level input voltage that guarantees operation
- V_{IH} — The voltage value required for a high-level input voltage that guarantees operation
- V_{OL} — The guaranteed maximum low-level output voltage of a gate
- V_{OH} — The guaranteed minimum high-level output voltage of a gate.

With the exception of high-level ouput voltage (which is a direct function of supply voltage), these values remain virtually unchanged over the temperature range and under normal operating conditions of the device.

Analysis of the input and output response characteristics of 'ALS/'AS TTL gates is necessary to understand the operation of these devices in most system applications. The dc response characteristics can best be depicted by an input voltage V_I versus output voltage V_O transfer plot.

Figure 14 plots the 'ALS/'AS characteristics as compared with members of other TTL logic families.

As shown in Figure 14, the 'ALS and 'AS devices exhibit a much better output savings when compared with standard TTL devices. The better high-level output voltage is primarily because of the active turn off of the low-level output transistor. The diode voltage drop in the normal output is replaced by a low-current V_{BE} voltage drop. This provides

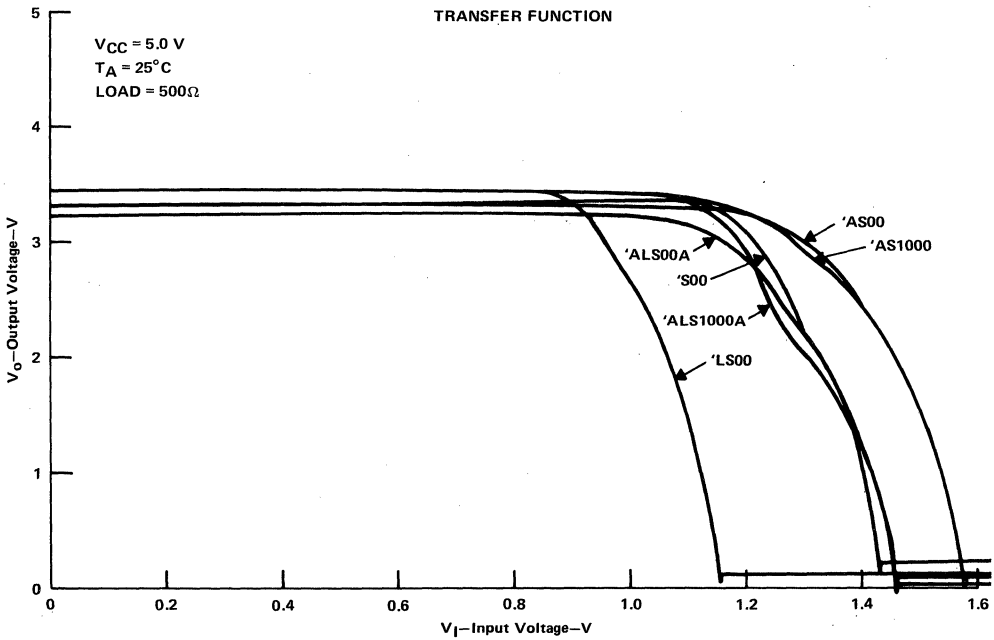


Figure 14. Input Voltage vs Output Voltage of 'ALS/'AS

a better high-level noise immunity in 'ALS and and 'AS over standard TTL devices.

Input Characteristics

To use 'ALS/'AS devices fully, a knowledge of the input and output characteristics is required. This is particularly true when a device interfaces with a device not in the same TTL series. In addition, knowledge of voltage and current relationships for all elements is important for proper design.

Figure 15 illustrates a typical plot for input current I_I versus input voltage, V_I, characteristics for 'ALS/'AS gate inputs during normal operation. A typical series 54/74 characteristic plot is also shown for reference. Any device used to drive a TTL gate must source and sink current. Conventionally, current flowing toward a device input terminal is designated as positive and current flowing out of a device input terminal is designated as negative. Low-level input current is negative current because it flows out of the input terminal. High-level input current is a positive current because it flows into the input terminal.

For transmission line conditions, a more accurate plot of the reverse bias section of these curves is required. These curves, Figure 16, are characteristic of the input clamping diode.

Low-Level Input Current

Figure 17 illustrates the dc equivalent of a standard 'ALS/'AS input circuit and shows the input current paths during a low-level input state. The low-level input current is primarily determined by resistor R1. However, low-level input current is also a function of the supply voltage, the ambient temperature, and the low-level input voltage. To

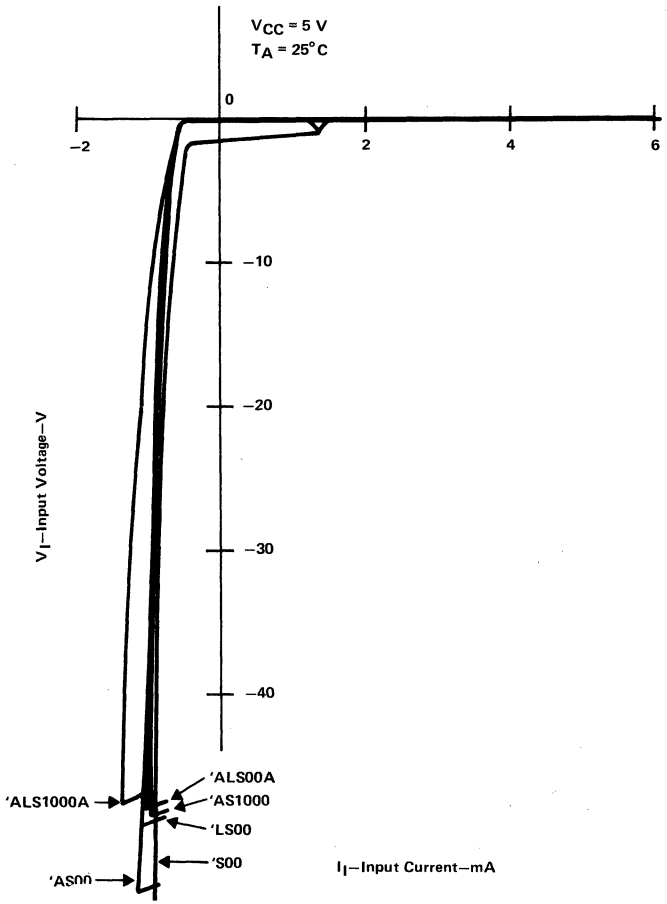


Figure 15. Input Current vs Input Voltage for TTL Families

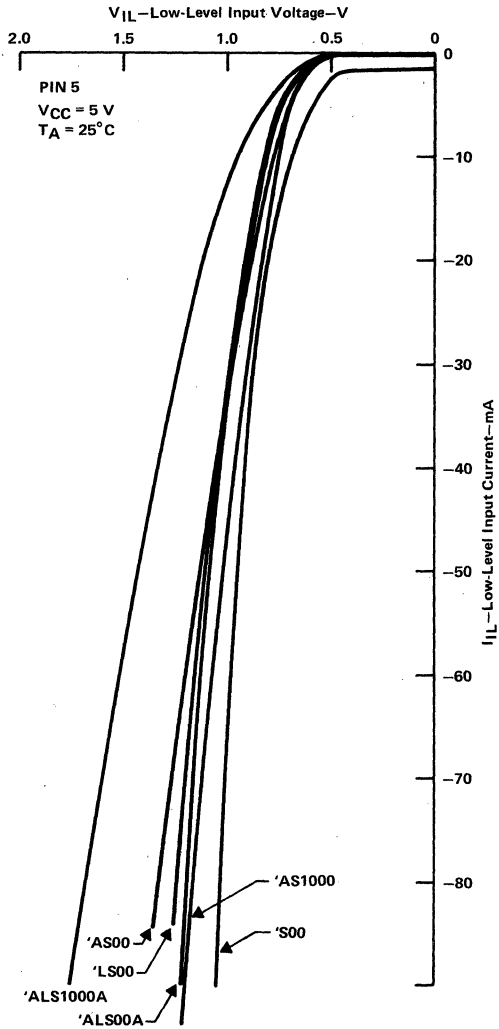


Figure 16. Low-Level Input Current vs High-Level Input Voltage for TTL Families

assure desired device operation under all possible conditions, the worst-case test is performed on all devices. Supply voltage is taken to the highest allowable value to cause the low-level input current to be at a maximum. With the exception of the input under test, all unused inputs are taken to a high level. This enhances any contribution of these inputs to the low-level input current of the emitter under test.

Input Clamping Diode Test

The quality of the input clamping SBD (D2 in Figure 17) is tested by ensuring that the forward voltage drop is not

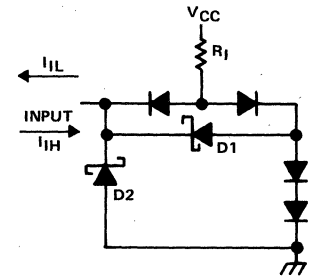


Figure 17. DC Equivalent Input Circuit for Series 'ALS Gate

greater than −1.2 V for 'AS and −1.5 V for 'ALS with a forward current of 18 mA. These values are guaranteed at minimum supply voltage and are valid across the operating temperature range. The characteristic of the input diode is illustrated in Figure 16.

High-Level Input Current

Another input parameter that must be measured and controlled is high-level input current. To ensure desired device operation under all possible conditions, the worst-case test is performed with all unused inputs grounded and supply voltage at its maximum value. This provides the highest value of low-level input current. Those devices with a high-level input current of sufficient magnitude to cause a degradation of high-level output voltage at an output must be screened out.

Input Breakdown Test

An additional high-level input current test is performed to check for base-emitter breakdown under the application of the full range of input voltages. This test is performed under the worst-case supply voltage conditions and is important because the base-emitter junction is small and can easily be overdissipated during the breakdown conditions.

Output Characteristics

The most versatile TTL output configuration is the push-pull (totem-pole) type. The totem-pole output has a low output impedance drive capability at both high and low logic levels. Both 'ALS and 'AS families use this configuration and have fanouts of 40 in both the high- and low-level states.

High-Level Output Characteristics

The ability of the totem-pole output to supply high-level output current is parametrically tested by applying a high-level input current value during measurement of high-level output voltage. However, the quality of the output stage is best indicated by parametrically measuring its current sourcing I_{OS} capability when connected to ground. Figure 18 shows the equivalent output circuit under high-level output conditions.

Figure 19 illustrates typical high-level characteristics. When measuring worst-case high-level output voltage, minimum supply voltage is used. A worst-case low-level

input voltage is applied to an input and all unused inputs are tied to supply voltage.

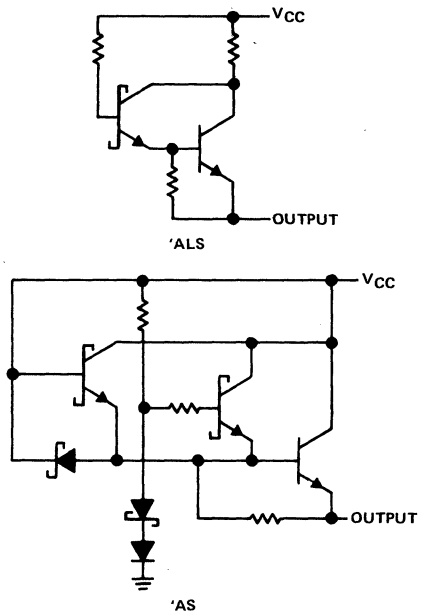


Figure 18. Equivalent Output Circuit for 'ALS/'AS Gates

Low-Level Output Characteristics

Figure 20 shows that section of the output drive circuit which produces a low-level output voltage V_{OL}. This characteristic is also tested at minimum supply voltage. Figure 21 illustrates the typical curve.

Switching Speed

Two switching-speed parameters are guaranteed on Series 'ALS and 'AS gates: propagation delay time for a high-level to a low-level at the output t_{PHL}, and a low-level to high-level transition time t_{PLH}. Both parameters are specified with respect to the input pulse using standard test conditions as follows:

V_{CC} = 4.5 V to 5.5 V
C_L = 50 pF
R_L = 500
T_A = MIN to MAX

Under these conditions, times in the order of 4 ns for 'ALS and 1.7 ns for 'AS are typical. Figures 22 and 23 illustrate how the propagation delay time for 'ALS and 'AS devices vary with load capacitance.

Most current in the output stage is drawn when both output transistors are on (i.e., during output transitions, the average power dissipation of a gate with a totem-pole output increases with operating frequency). This is caused by more high-current transitions per second at the output as the frequency increases. Figure 24 illustrates the effect for both 'ALS and 'AS devices.

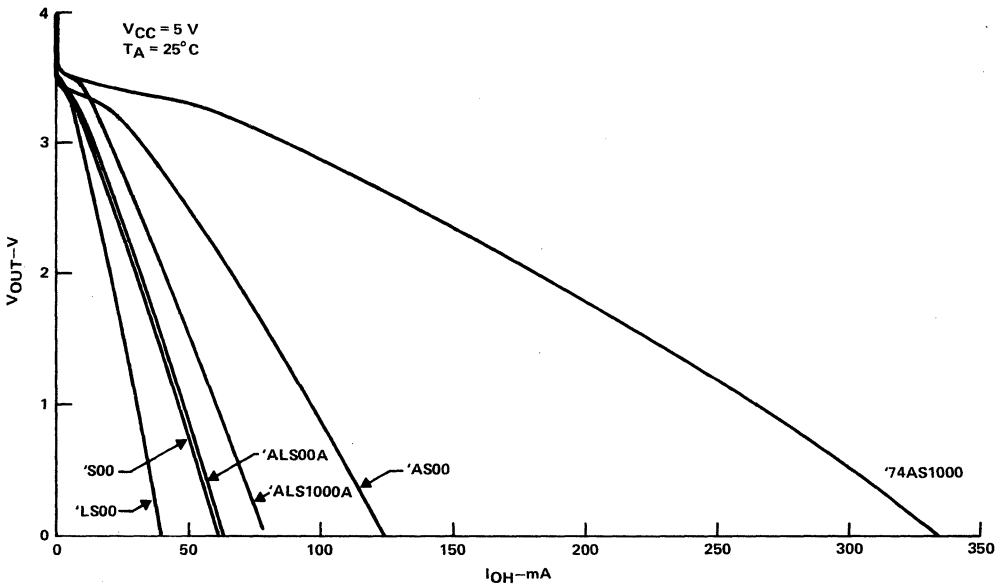


Figure 19. High-Level Output Voltage vs High-Level Output Current

DC Noise Margins

Noise margin is a voltage specification which guarantees the static dc immunity of a circuit to adverse operating conditions. Noise margin is defined as the difference between the worst-case input logic level (V_{IH} minimum or V_{IL} maximum) and the guaranteed worst-case output (V_{OH} minimum or V_{OL} maximum) specified to drive the inputs. Table 2 lists the worst-case output limits for the 'AS and 'ALS families.

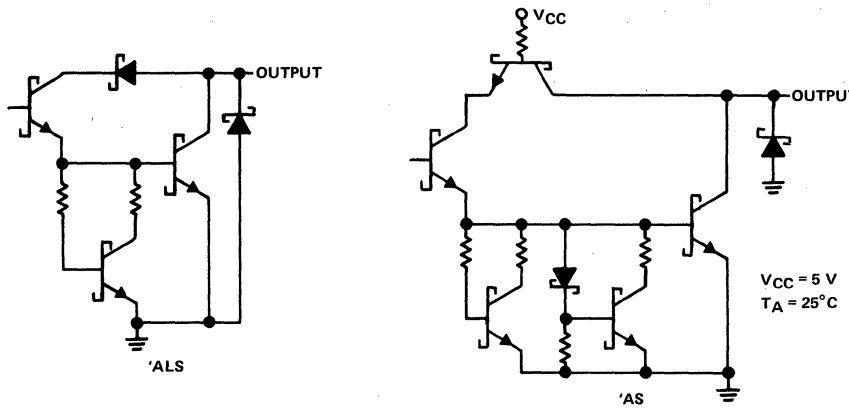


Figure 20. Low-Level Output Circuit for 'ALS/'AS Gates

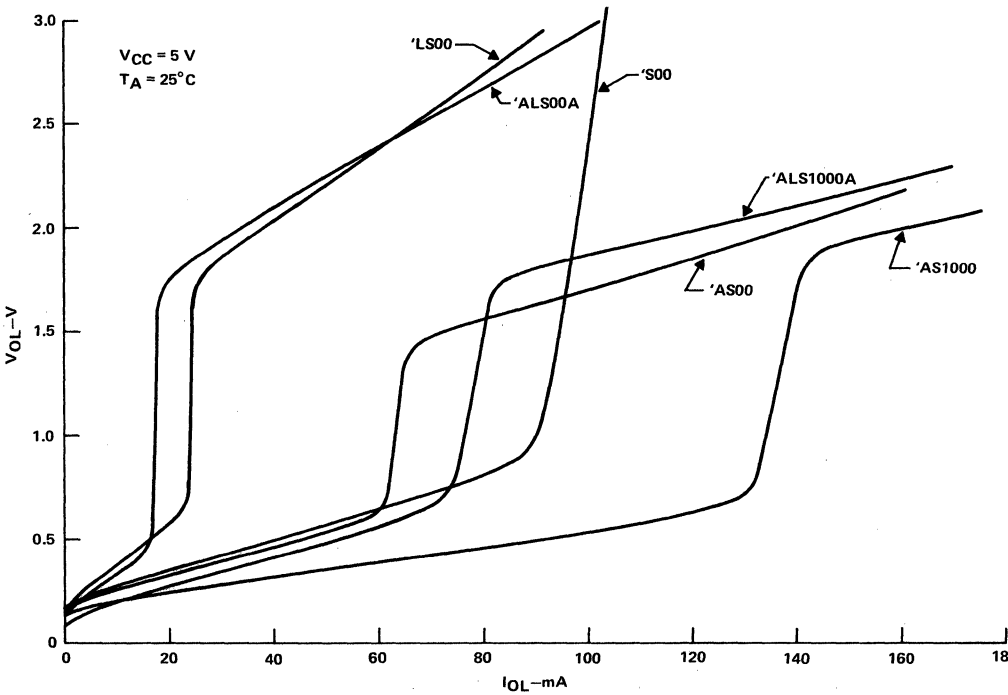


Figure 21. Low-Level Output Voltage vs Low-Level Output Current

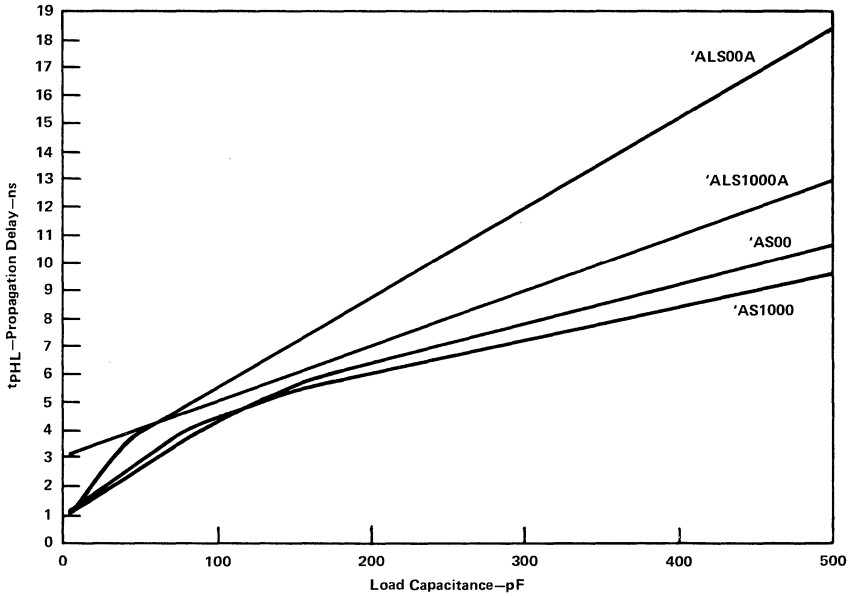


Figure 22. High- to Low-Level Propagation Delay vs Load Capacitance

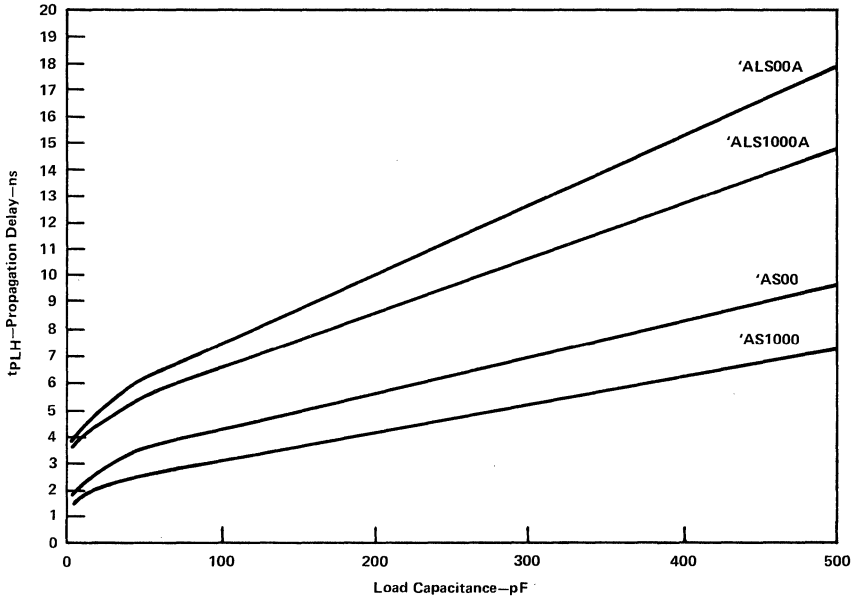


Figure 23. Low- to High-Level Propagation Delay vs Load Capacitance

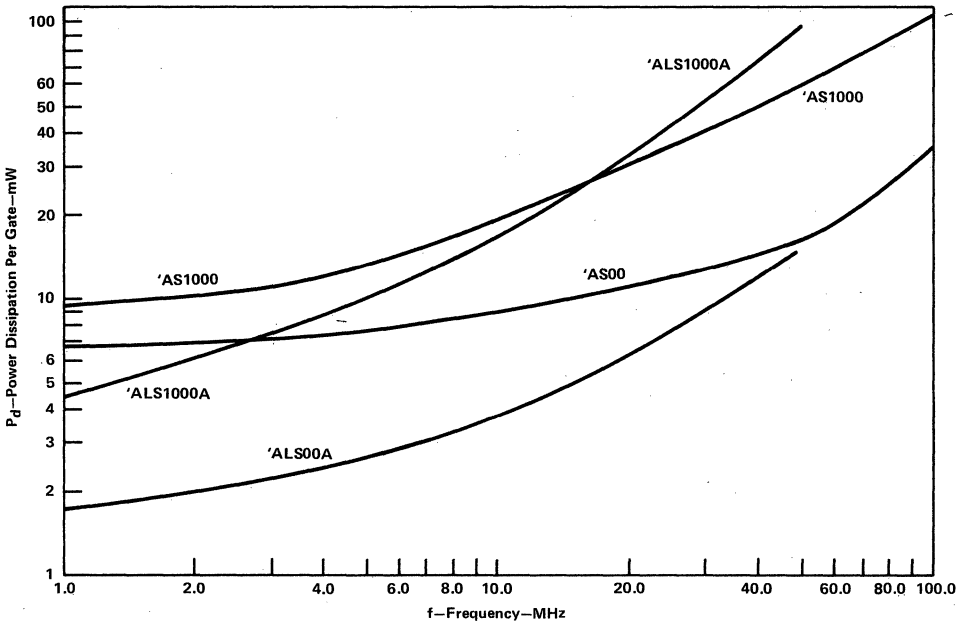


Figure 24. Power Dissipation per Gate vs Frequency

Specified Logic Levels and Thresholds

The high-level noise margin is obtained by subtracting V_{OH} minimum from V_{IH} minimum. The low-level noise margin is obtained by subtracting V_{IL} maximum from V_{OL} maximum. The worst-case high-level noise margin is guaranteed to be at least 500 mV for both 'AS and 'ALS devices and at least 300 mV for low-level noise immunity across the operating free-air temperature ranges.

The usefulness of noise margins at the system design level is the ability of a device to be impervious to noise spikes at the input. The input voltage falls into one of three categories: low-logic state (between ground and 0.8 V), threshold region (between 0.8 V and 2 V), or high-logic state (between 2 V and V_{CC}). If an input voltage remains exclusively in the low-logic or high-logic state, it can undergo any excursions within that state. A level change from 5.5 V to 2 V or from ground to 0.8 V should not affect the output state of the device. To guarantee an expected output level change, the appropriate input has to undergo a change from one input state to the other input state (i.e., a transition through the threshold region). If a device will not remain in the correct state when voltage excursions on the input are occurring, it is violating its truth table.

Noise Rejection

The ability of a logic element to operate in a noise environment involves more than the dc or ac noise margins previously discussed. To present a problem, an externally generated noise pulse must be received into the system and cause a malfunction. Stable logic systems with no storage

Table 2. Worst Case Output Parameters

PARAMETER (V)	'AS (0°C to 70°C)	'ALS (0°C to 70°C)	'AS (−55°C to 125°C)	'ALS (−55°C to 125°C)
V_{IH}(MIN)	2	2	2	2
V_{IL}(MAX)	0.8	0.8	0.8	0.8
V_{OH}(MIN) @ V_{CC} = 4.5 V*	2.5	2.5	2.5	2.5
V_{OL}(MAX)	0.5	0.5	0.5	0.4
High Level Noise Margin ($V_{OH}-V_{IH}$)	0.5	0.5	0.5	0.5
Low Level Noise Margin ($V_{IL}-V_{OL}$)	0.3	0.3	0.3	0.4

*Actual specification for $V_{OH(min)}$ is V_{CC} − 2 V.

elements are practically impervious to ac noise. However, large dc voltages could cause noise problems. Systems with triggerable storage elements or those operating fast enough for the noise to appear as a signal are much more susceptible to noise.

The noise voltage must be radiated or coupled into the circuit. The amount of noise required to develop a given voltage is a function of the circuit impedance. Because of the low output impedance of TTL circuits, noise immunity is improved. Noise is transferred from the source (with some arbitrary impedance) through a coupling impedance to the impedance of the circuit under consideration.

Figure 25 shows a circuit where the coupling impedance is stray capacitance and the load impedance is provided by the gates. The relatively tight coupling of this circuit and the loading effect on the driving source is significant enough

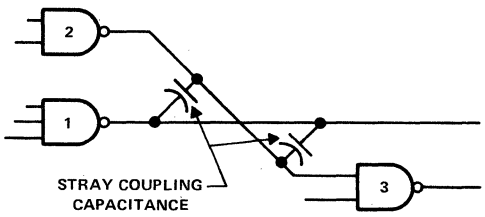


Figure 25. Stray Coupling Capacitance

to be considered. However, since the source effect is difficult to assess and is in a direction to improve rather than degrade the noise rejection, its effects are ignored. This results in a worst-case type of response indication. In the case of radiated noise, the source resistance is a definite factor in noise coupling and essentially replaces the reactive coupling impedance.

By ignoring the driving source impedance to make conditions more nearly standard, it is possible to determine a set of curves relating the developed noise pulse to the noise source amplitude, the noise rise or fall time, the coupling impedance, and the load impedance. Curves have been developed[1] for several different input waveforms. Since the 'ALS waveform is essentially a ramp with a dv/vt of 1 V/ns (approximately 2.5 V/ns for 'AS), the most applicable curve is that for a ramp input.

Figure 26(a) shows the equivalent circuit from which the ramp response plot in Figure 26(b) was developed. The input pulse shown in Figure 26(c) is a ramp input.

$$e_i(t) = \frac{E_i}{T}\ t$$

where

E_i = Maximum input voltage and
T = Total rise time of input voltage

The output pulse is represented analytically by

$$e_0(t) = \frac{E_i}{T}\ RC\left(1 - e^{-\frac{t/T}{RC/T}}\right)$$

$$e_0(i) = E_i\ \tau\left(1 - e^{-i/\tau}\right)$$

where

$$\tau = \frac{RC}{T}$$

$$\theta(i) = \tau\left(1 - e^{-i/\tau}\right)$$

$$\theta(i) = \frac{e_{0(i)}}{E_i}$$

with holding for unit time. This is followed by an exponentially decaying voltage with a time constant τ. Values of τ and i on the figure are normalized by the value of the total rise time of the stimulated noise pulse e_i. Using Figure 26(b), the pulse width and amplitude of the coupled noise pulse can be estimated.

As an example, using the circuit shown in Figure 25, apply a noise pulse of 3 V in amplitude and rising at 1 V/ns

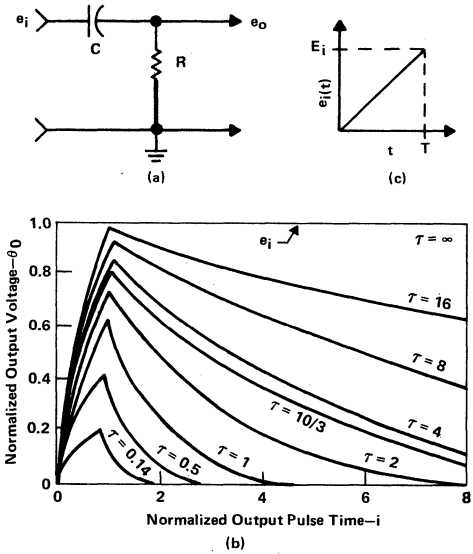


Figure 26. Evaluations of Gate Response to Fast Input Pulses

with gate 2 at a high-logic state. Assume a nominal output impedance of 58 Ω (30 Ω for 'AS) and coupling capacitance of 10 pF. Use the following formula:

$$\text{Total rise time } T = \frac{3\text{ V}}{1\text{ V/ns}^{**}} = 3\text{ ns}^{\dagger}$$

$$\tau = \frac{RC}{T} = \frac{(10 \times 10^{-12})(58)}{3}$$

$$= \frac{0.58 \times 10^{-9}}{3} = 0.19\text{ ns}$$

**2.5 V/ns for 'AS
†1.2 ns for 'AS

To convert the normalized values of τ and i in Figure 26(b) to actual values, multiply by 3 ns. The output voltage scale will be multiplied by 3 V. Using the $\tau = 0.19$ curve gives a peak e_o of 0.57 V (0.19 × 3) and a pulse width of 3 ns at the 50% points. To determine whether this pulse will cause interference, enter these values (0.57 V and 3 ns) on the graph shown in Figure 27. Since the gates have approximately 1.8 V of noise immunity at this point, they should not be affected.

If an open-collector gate is used with a passive 1 kΩ pull-up resistor, the situation would change. Use the following formula:

$$\text{Total rise time} = \frac{3\text{ V}}{1\text{ V/ns}^{**}} = 3\text{ ns}^{\dagger}$$

$$\tau = \frac{(10 \times 10^{-12})(1 \times 10^{3})}{3}$$

$$= \frac{10 \times 10^{-9}}{3} = \frac{10}{3}\text{ ns}$$

**2.5 V/ns for 'AS
†1.2 ns for 'AS

Now the amplitude (from the curves) approaches 2.58 V (0.86 × 3) and the pulse width at the 50% points is approximately 8.52 ns (2.84 × 3). The next gate will propagate this pulse.

This example is an oversimplification. The coupling impedances are complex (but resolvable into RLC series coupling elements) and the gate output impedance changes with load. Our purpose is to show why and how the low impedance of the active TTL output rejects noise and to make a comparison with a passive pull-up.

The ability to operate in a noisy environment is an interaction of the built-in operating margins, the time required for the device to react, and the ease with which a noise voltage is developed. In all cases, except the ability to react to short noise pulses, the TTL design has emhasized noise rejection.

Nothing has been discussed concerning noise in devices other than gate circuits. Many MSI devices are complex gate networks and, because of their small size, are more superior in a noisy environment operation than their discrete gate equivalents. Noise tolerance of latching devices is implied in the setup times, hold times, clock pulse width, data pulse widths, and similar parameters. Output impedances and input noise margins are quite similar to those of the gates and may be treated in a similar manner. If a latching device does become noise triggered, the effective error is stored and does not disappear with the noise.

Parameter measurement information is shown in Figure 28.

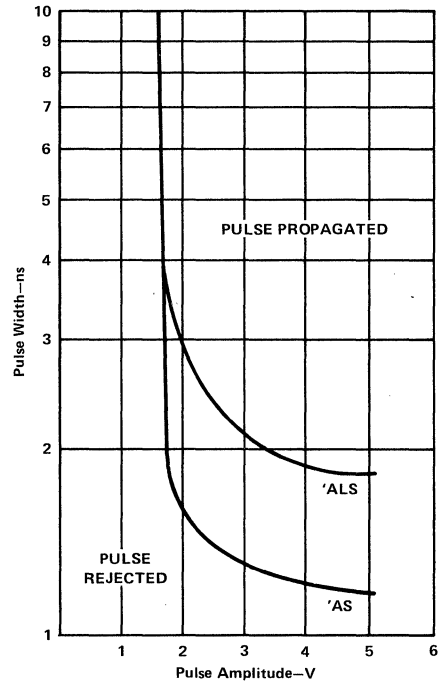
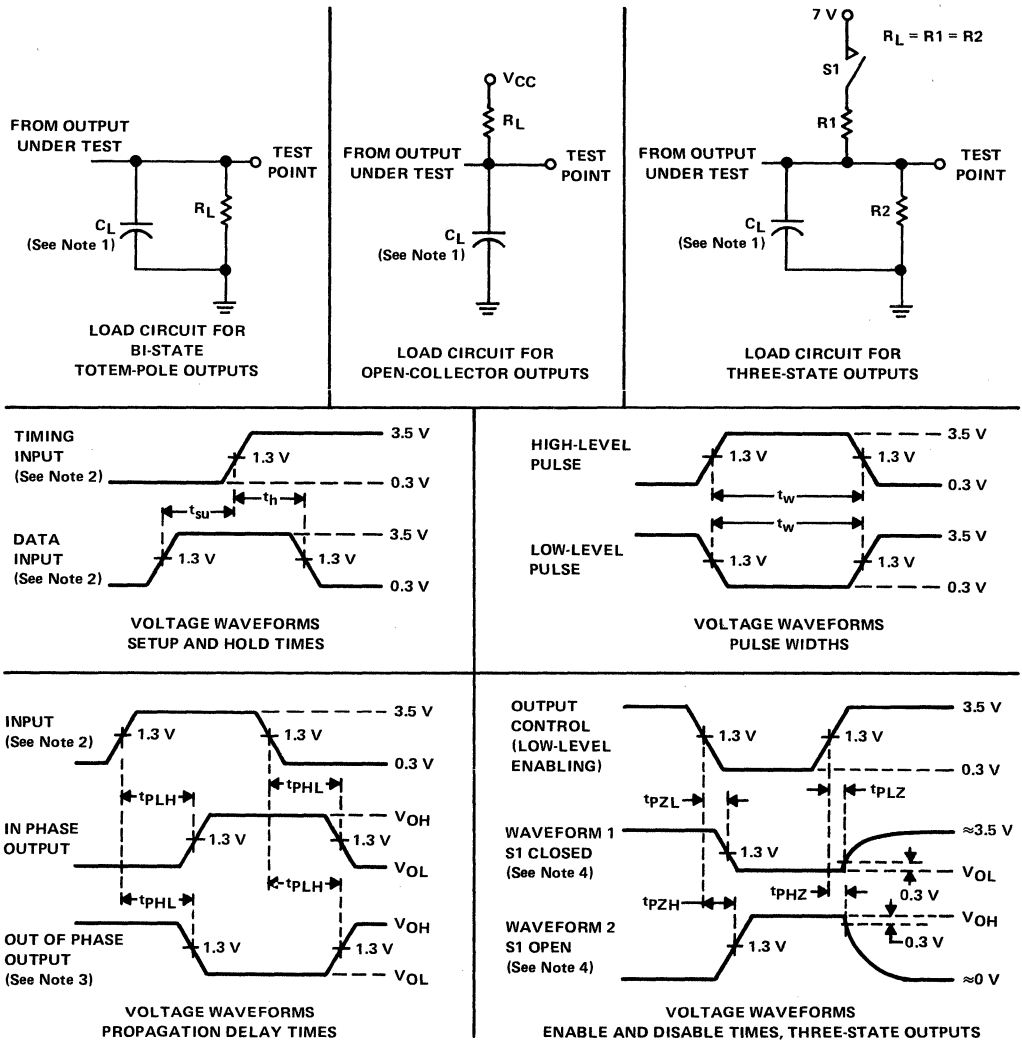


Figure 27. Theoretical Required Pulse Width vs Pulse Amplitude for 'AS and 'ALS Inputs

GUIDELINES FOR SERIES 'ALS/'AS TTL SYSTEM DESIGN

System layout and design requirements for Advanced Schottky TTL circuits are essentially the same as those guidelines which have previously been established and are applicable for all high-performance digital systems. Tables 3 through 6 provide a brief summary of the solutions to most design decisions needed to implement systems using Advanced Schottky TTL. Supplementary data which may be useful for developing specific answers to unique problems is provided later.



NOTES: 1. C_L includes probe and jig capacitance.
2. All input pulses have the following characteristics PRR ≤ 1 MHz, $t_r = t_f$ = 2 ns, duty cycle = 50%.
3. When measuring propagation delay times of 3-state outputs, switch S1 is open.
4. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

Figure 28. Parameter Measurement Information

POWER SUPPLY REGULATION

Power supply regulation cannot be treated as if it is an independent characteristic of the device involved. Power supply regulation, along with temperature range, affects noise margins, fanout, switching-speed, and several other parameters. The characteristics most affected are noise margin and fanout. When these two parameters are within the specified limits, the power-supply regulation will normally be within specified limits. However, on a device where auxiliary parameters are more critically specified, a more restrictive power-supply regulation is normally required. When power-supply regulation is slightly outside the specified limits for TTL devices, the device may still

operate satisfactorily. However, if high ambient-noise levels and extreme temperatures are encountered, failures may occur.

Application of a supply voltage above 7 V (absolute maximum rating) will result in damage to the circuit.

Since power dissipation in the package is directly related to supply voltage, the maximum recommended supply voltage for TTL devices is specified at 5.5 V. This provides an adequate margin to ensure that functional capability and long-term reliability are not jeopardized.

High-level output voltage is almost directly proportional to supply voltage (i.e., a drop in supply voltage causes a drop in high-level output voltage and an increase in supply voltage results in an increase in high-level output voltage). Because of this relationship, high-level output voltage for 'ALS/'AS devices is specified as supply voltage -2 V (V_{CC} -2 V).

Since high-level output voltage is directly related to supply voltage, the output current of the device is also directly related. The output current value is established by choosing output conditions to produce a current that is approximately one-half of the true short-circuit current.

It is advantageous to regulate or clamp the maximum supply voltage at 5.5 V including noise ripple and spikes. When this conditions exists, unused AND and NAND gates can be connected directly to the supply voltage.

Table 3. Guidelines for Systems Design for Advanced Schottky TTL

ITEM	GUIDELINE
Single wire connections	Wire lengths up to approximately 12 inches may be used. A form of ground plane is desirable. Use point-to-point routing rather than parallel. If the wire is longer than 12 inches, use either a dense ground plane with the wire routed as close to it as possible, or use a twisted-pair cable.
Coaxial and twisted-pair cables	Design around approximately 80 Ω to 100 Ω of characteristic impedance. Cross talk increases at higher impedances. Use a coaxial cable of 93 Ω impedance (e.g., Microdot 293−3913). For twisted-pair cable, use number 26 or number 28 wire with the insulation twisted at the rate of 30 turns per foot.
Transmission-line-ground	Ensure that transmission-line ground returns are carried through at both transmitting and receiving ends. V_{CC} decoupling ground, device ground, and transmission-line ground should have a common tie point.
Cross talk	Use point-to-point back-panel wiring to minimize noise pickup between lines. Avoid long unshielded parallel runs. However, if they must be used, they should carry signals that propagate in the same direction.
Reflections	Reflections occur when data interconnects become long enough that 2-line propagation delays are pulse transition times. For series TTL, reflections are normally of no importance for lines shorter than 12 inches.
Resistive pull-up	If fanout of driving output permits, use approximately 300 Ω of resistive pull-up at the receiving end of long cables. This provides added noise margin and more rapid rise times.

Table 4. Guidelines for Printed Circuit Board Layout for Advanced Schottky TTL

ITEM	GUIDELINE
Signal connections	Whenever possible, distribute loads along direct connections. Signal leads should be kept as short as possible. However, lead lengths of up to 15 inches will perform satisfactorily. This is especially for large boards that use a ground plane, ground, and/or V_{CC} plane. In addition, it will perform satisfactorily for small boards using ground mesh or grid. In high-frequency applications, avoid radial fanouts and stubs. If they must be used to drive some loads, reduce lead length proportionally and avoid sharp bends. Normal on-board fanouts and interconnections do not require terminations. Response of lines driving large numbers or highly capacitive loads can be improved with terminations of 300 Ω to V_{CC} and 600 Ω to ground in parallel with the last load if fanout of the driving output permits.
Conductor widths	Signal-line widths down to 0.015 inch are adequate for most signal leads.
Signal-line spacing	Signal-lead spacing on any layer down to 0.015 inch can be used especially if care is taken to avoid adjacent use of maximum length and minimum spacing. Increase spacing wherever layout permits. Pay particular attention to clock and/or other sensitive signals.
Insulator material	Thickness of insulation material used for a multilayer board is not critical. If ground and V_{CC} planes or meshes are used, their capacitive proximity can be used to reduce the number of decoupling capacitors needed and this also supplements the supply bypass capacitor.

Table 5. Guidelines for General Usage of Advanced Schottky TTL

ITEM	GUIDELINE
Power supply	For RF bypass supply primary, maintain ripple and regulation at less than or equal to 10%.
V_{CC} decoupling	Decouple every 2 to 5 packages with RF capacitors of 0.01 to 0.1 μF. Capacitors should be located as near as possible to the decoupled devices. Decouple line driving or receiving devices separately with 0.1 μF capacitors between V_{CC} and the ground pins.
On-board grounding	A ground plane is essential when the PCB is relatively large (over 12 inches). Smaller boards will work with ground and/or V_{CC} mesh or grid.
System grounding	Try to simulate bus bars with a width to thickness ratio greater than or equal to 4. This can be accomplished by multiple parallel wires or by using flat braid. Performance will be enhanced when a copper or silver-copper bus is used. The width to thickness ratio required will vary between systems, but greater than or equal to 4 will satisfy most systems.

Table 6. Guidelines for Gates and Flip-Flops Using Advanced Schottky TTL

ITEM	GUIDELINE
Data input rise and fall times	Reduce input rise and fall times as driver output impedance increases. Rise and fall times should be equal to or less than 15 ns/V and essentially free of noise ripple.
Unused input of AND and NAND gates and unused preset and clear inputs of flip-flops	Tie the unused input of AND and NAND gates and the unused preset and/or clear inputs of flip-flops as follows: 1. Directly to V_{CC}, if the input voltage rating of 5.5 V maximum is not exceeded. 2. Through a resistor equal to or greater than 1 kΩ to V_{CC}. Several inputs can be tied to one resistor. 3. Directly to a used input of the same gate, if maximum fanout of driving device will not be exceeded. Only the high-level loading of the driver is increased. 4. Directly to an unused gate output, if the gate is wired to provide a constant high-level output. Input voltage should not exceed 5.5 V.
Unused input of NOR gates	Tie unused input to used input of same gate, if maximum fanout of driving device will not be exceeded or tie unused input to ground.
Unused gates	Tie input of unused NAND and NOR gates to ground for lowest power drain. Tie inputs of unused AND gates high and use output for driving unused AND or NAND gate inputs.
Increasing gate/buffer fanout	Connect gates of same package in parallel.
Clock pulse of flip-flops	Drive clock inputs with a TTL output. If not available, rise and fall times should be less than 50 ns/V and free of ripple noise spikes.

SUPPLY VOLTAGE RIPPLE

Ripple in the supply voltage is generally considered a part of the supply voltage regulation. However, when combined with other effects (e.g., slow rise times), ripple voltage is more significant.

The effect of ripple voltage V_R can appear on either the supply voltage V_{CC} or the ground supply GND. When ripple appears on the supply voltage, it causes modulation of the input signal. The extent of the effect depends upon circuit parameters and source impedance.

The turning on of transistor Q5, shown in Figures 12 and 13, is controlled by the voltage at the base of transistor Q2 with respect to ground in accordance with the formula:

$$V_B = V_{BE} \text{ of Q2} + V_{BE} \text{ of Q3} + V_{BE} \text{ of Q5}$$

When ripple voltage is modulated onto the input voltage, the amplitude depends on the source impedance (Figure 29). The amplitude can be determined by the following equation:

$$\Delta V_R = V_R\left(\frac{R1/\beta}{R1/\beta + R2}\right)$$

$$= V_R\left(\frac{R1}{R1 + \beta R2}\right)$$

where $R1$ = source impedance
β = gain of transistor Q1.

Ripple voltage has the effect of adding extra pulses to the input signal (Figure 30). When ripple voltage appears in the ground supply, the threshold voltage is modulated and extra pulses occur (Figure 31).

Although decreasing the source impedance will reduce the effects of ripple voltage, it cannot be eliminated entirely because the emitter-base junction has an apparent resistance of approximately 30 Ω. Because of cancellation between the driving gate and the driven gate, low-frequency ripple is not a problem.

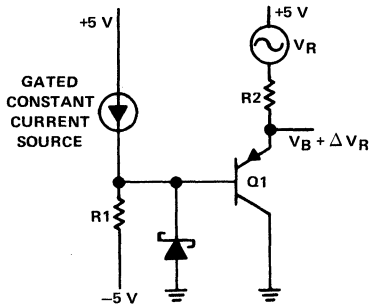


Figure 29. Effect of Source Impedance on Input Noise

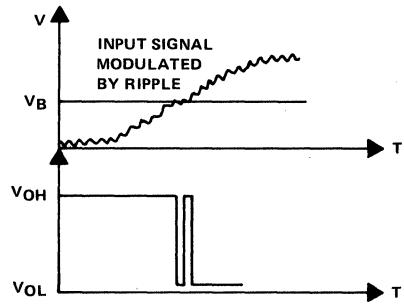


Figure 30. Spurious Output Produced by Supply Voltage Ripple

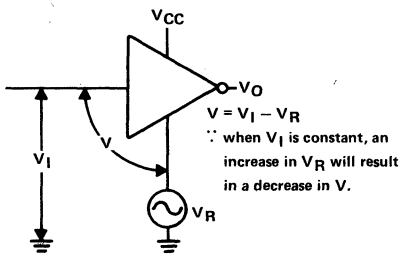


Figure 31. Effect of Ground Noise on Noise Margin

NOISE CONSIDERATIONS

Extraneous voltages and currents (called noise) introduced into a digital logic circuit are discussed in the following paragraphs. Figure 32(a) is a typical digital logic

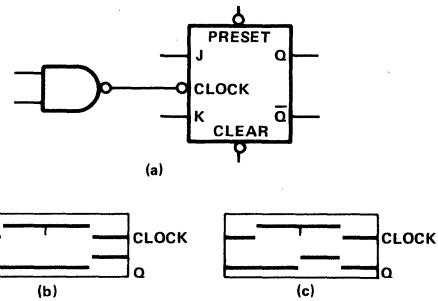


Figure 32. Typical Logic Circuit with Noisy Input

circuit consisting of a NAND gate and a J-K flip-flop. When a small noise pulse is coupled onto the clock input [(Figure 32(b)], the flip-flop does not respond and the Q output is correct. However, when a large noise pulse is coupled onto the clock input [(Figure 32(c)], the flip-flop sees the pulse as a clock transition and an erroneous Q output occurs. Therefore, it is essential to protect digital logic circuits from noise.

Noise Types and Control Methods

The noise types encountered in digital logic systems, their source, and the method of controlling them are as follows:

1. External noise — External noises radiated into the system. The sources include circuit breakers, motor brushes, arcing relay contacts, and magnetic-field-generating. The methods of controlled to be considered are shielding, grounding, or decoupling.
2. Power-line noise — Noise coupled through the ac or dc power distribution system. The initial sources and controlling methods are the same as for external noise.
3. Cross talk — Noise induced into signal lines from adjacent signal lines. Controlling methods to consider are shielding, grounding, decoupling, and, where possible, increasing the distance between the signal lines.
4. Signal-current noise — Noise generated in stray impedances throughout the circuit. The controlling methods to consider are shielding, grounding, decoupling, and, where possible, reduction of stray capacitance in the circuit.
5. Transmission-line reflections — Noise from unterminated transmission lines that cause ringing and overshoot. The method of control is to use, where possible, terminated transmission lines.
6. Supply-current spikes — Noise caused by switching several digital loads simultaneously. The controlling method is to design, where possible, the system so that digital loads are not switched simultaneously.

Shielding

In addition to its own internally generated noise, electrical equipment must operate in an extremely noisy environment. Noise pulses, which may come from a number of sources, consist of an electrostatic field, and electromagnetic field, or both. The noise waveform must be prevented from entering the equipment. This is accomplished by shielding. Since the noise fields are usually changing at a rapid rate, the shield required to exclude them may be very small. For effective exclusion, the sensitive circuits must be completely shielded.

Aluminum or similar materials are effective in stopping electrostatic noise. However, only a ferrous metal can successfully protect equipment against magnetic fields. While it is helpful to connect the system to earth ground, the shield system must be complete and must be grounded to the system ground to prevent the shield from coupling noise into the system.

External noise may be conducted into the system by the power lines. Decoupling and filtering of these lines should be standard design procedure.

Grounding and Decoupling

The total propagation delay is of secondary importance in generation of internal noise. The actual transition time determines the amplitude and frequency spectrum of the generated signal at the higher harmonics. Application of the Fourier integral to series 'ALS/'AS waveforms shows frequency components of significant amplitude that exceed 100 MHz. Because of the frequency spectrum generated when an 'ALS/'AS device switches, a system using these devices must consider problems caused by radio frequency (RF) even though the repetition rates may be only a few megahertz. The transient currents generated by charging capacitors, changes in the levels of dc, line driving, etc., must be considered. In Figure 33 for example, a gate driving a transmission line is represented by a voltage source E, having an output impedance Z_S connected to an impedance Z_0, and loaded with a resistance R_L.

Until after a reflected pulse returns from the termination of the transmitting device, line termination is not a factor in drive current. In a practical TTL circuit, the line termination must be high relative to the line impedance. For explanation purposes, assume that the source voltage is 5 V in amplitude, the output impedance of the source is 50 Ω and the line impedance is 50 Ω. When the source voltage makes the transition from 0 V to 5 V, the voltage across the input of the line V_I is determined by the following equation:

$$V_I = E\frac{Z_0}{Z_S + Z_0} = 2.5 \text{ V}$$

where E = source voltage
Z_0 = line impedance
Z_S = source impedance

For the 50 Ω line to become charged, the current that must flow onto the line is determined by the following equation:

$$I_{line}\ \frac{V_{in}}{Z_0} = \frac{2.5}{50} = 50 \text{ mA}$$

In addition, this current flows in the ground return, which, in this case, is the transmission-line ground. If the line and return are originated and terminated close to the driving and receiving devices, there is no discontinuity in the line. Where the ground is poorly returned, the current flow sees the discontinuity in the cable as a high impedance and a noise spike is generated (i.e., the ground current sees a low impedance and a current cancellation if the ground is properly carried through and, if not, it sees a high impedance). Figure 34 presents a specific example. Assume that the gate driving the line is switched from the high to low state. Current flow is indicated by the arrow marked with an I. Since the line is improperly returned to the driver, a pulse is developed across the impedance. A possible consequence is the false output of gate 3 (G3).

If the ground return is properly connected, the proper results are obtained. The impedance discontinuity is eliminated and current cancellation occurs at the ground point. Undesirable voltage spikes are then eliminated. Two empirical rules to reduce transmission-line currents have been established and have been found to be effective (Figure 35).

1. Carry all returns, including twisted pair and coaxial cables, to a good ground termination. Ground line returns close to the driving and receiving devices.

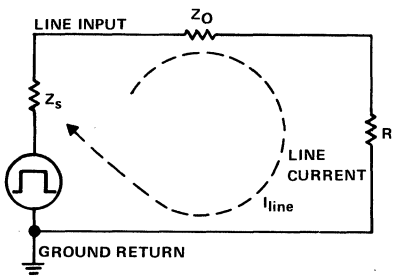
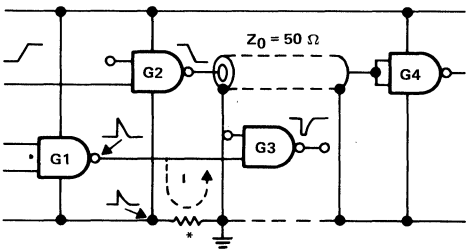


Figure 33. Diagram Representing a Gate Driving a Transmission Line



*Impedance of poor ground return

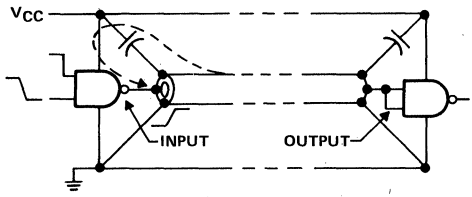
Figure 34. Noise Generation Caused by Poor Transmission-Line Return

2. Decouple the supply voltage of line-driving and line-receiving gates with a 0.1-μF disk ceramic capacitor.

As the devices change state, current levels change because of the different device currents required in each state, the external loading, the transients caused by charging and discharging capacitive loads, and the conduction overlap in the totem-pole output stage. When a gate changes states, its internal supply current changes from high to low (these values are stated on the data sheet for each device). In addition, any capacitance, stray or otherwise, must be charged or discharged for a logic state change. The capacitance must be charged by a current determined by

$$I = C \frac{dv}{dt} \quad (4)$$

If the total stray capacitance on a gate output, the logic-level voltage excursion, and the associated rise or fall times are known, then the ideal-case instantaneous current during the transition can be calculated.

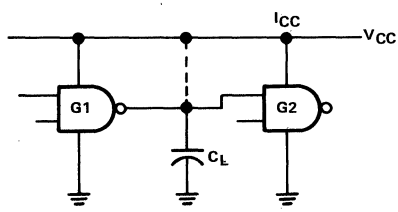


Broken arrow shows path of line-charging current

Figure 35. Ideal Transmission-Line Current Handling

From Eq. (4) it can be determined that the current transient for charging load capacitance will increase with higher speed TTL circuits. Therefore, the Series 54ALS/74ALS devices will have lower transient current than the Series 54AS/74AS devices. Another parameter that should be considered is the value of R7 (shown in Figures 12 and 13). Resistor R7 acts as a limit on the charging current.

The current required for charging load capacitance C_L (Figure 36) is supplied by the supply voltage when the transition is from logic low to logic high at the output of gate 1 (G1). When the output of G1 goes from high to low, the load capacitance is shorted to ground by transistor Q5 (shown in Figures 12 and 13) and has no effect on supply current.



C_L includes all capacitance: stray, device, etc.

Figure 36. Circuit with Effective Capacitive Loading

A characteristic common to all TTL totem-pole output stages contributes an additional current transient when the output changes from a logic low to a logic high. This transient, or spike, is caused by the overlap in conduction of the output transistors Q7 and Q5 (shown in Figures 12 and 13). The situation arises because transistor Q7 can turn on faster than transistor Q5 can turn off. This places a direct circuit consisting of transistors Q7 and Q5 and resistor R4 between supply voltage and ground. For all series 'ALS TTL circuits, the maximum possible peak current can be determined by

$$I_{CC}max = \frac{V_{CC} - V_{CEQ6} - V_{BEQ7} - V_{CEQ5}}{R7}$$

However, due to the active turnoff circuit (consisting of R5, R6, and Q4), Q5 will be only slightly in the linear region and the current spike will be less.

The total supply-current switching transient is then a combination of three major effects: the difference in high-level and low-level supply current, the charging of load capacitance, and the conduction overlap. Tests were performed to demonstrate these effects. The results are shown in Figure 37. Six types of series TTL devices were tested with no load (i.e., the oscilloscope was connected to the output only when measuring V_O and the photographs were double exposed). This was to approximate the effects of conduction overlap isolated from the transient caused by charging load capacitance. Different vertical scales were used on some of the photographs.

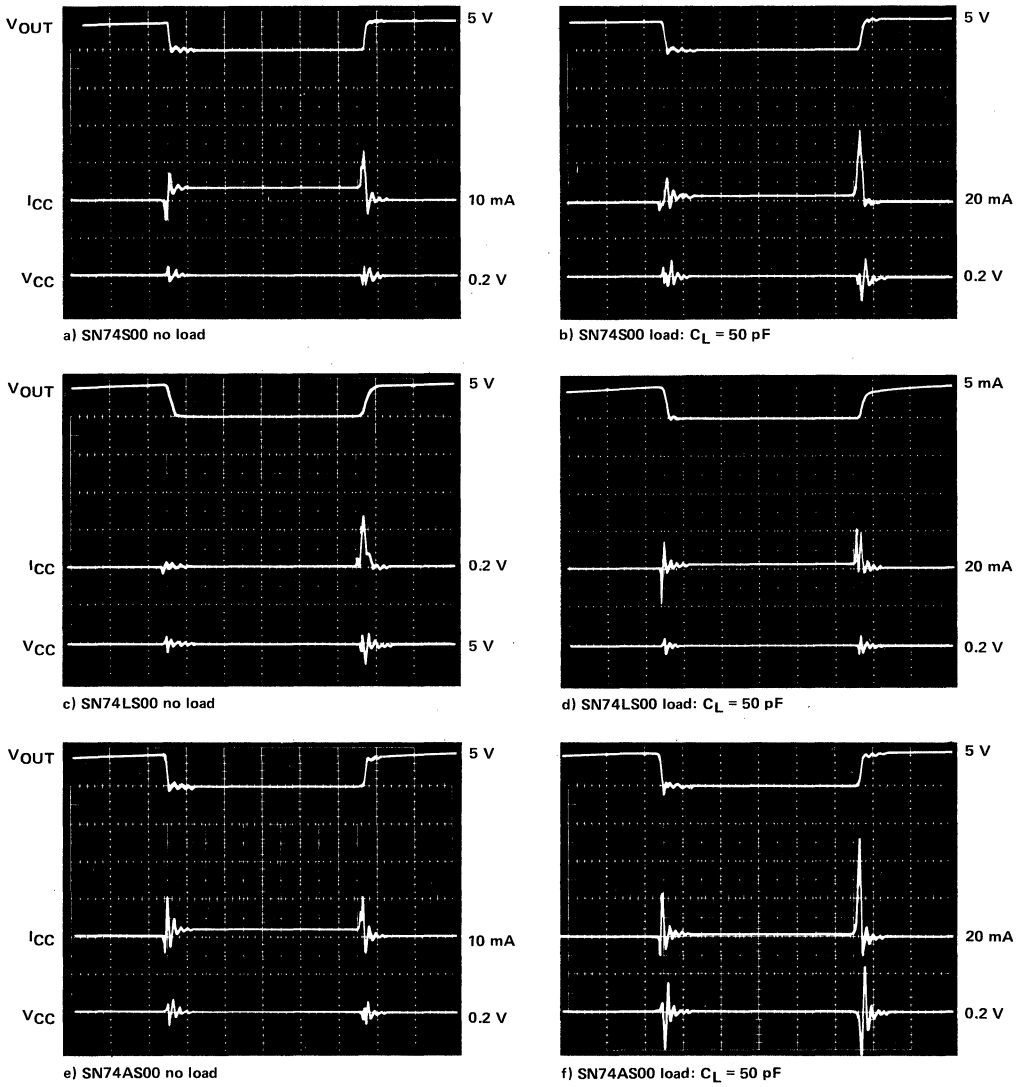
The results are almost as predicted. The low-power devices have the lower transients. Since it is the fastest circuit, the SN74AS00 device should be highest. However, a decrease is shown, and the reason for the decrease is explained (Figure 39). The additional circuits to reduce conduction overlap of the output transistors result in a smaller transient even though the typical switching time is 1.7 ns compared to 9 ns for the Series 54/74LS.

The second series of tests shown in Figure 37 cover a capacitive load of 50 pF. For this test, all of the supply current transient peaks increase in amplitude and width.

Because of the larger transient currents, voltage spikes on the supply voltage measured at the IC package are also increased.

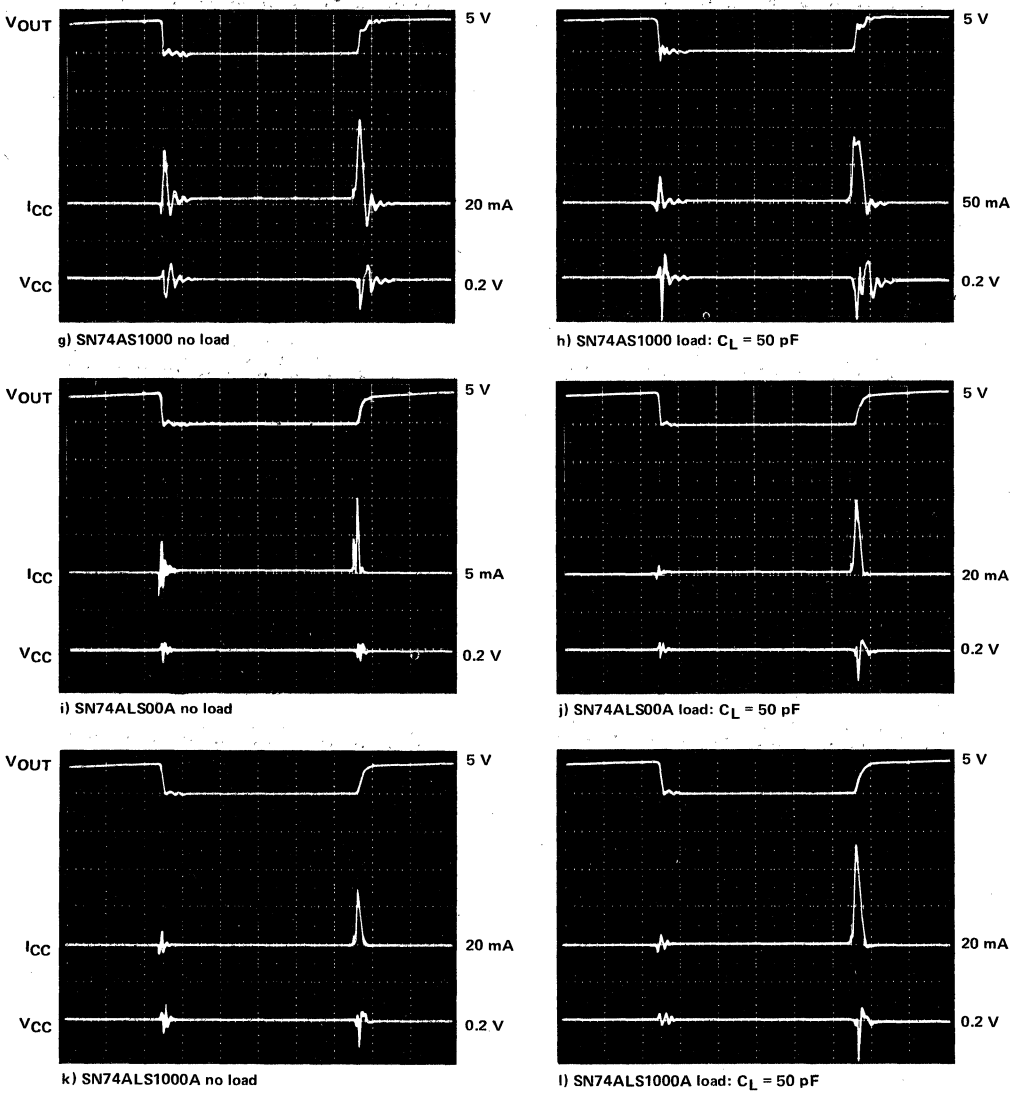
From these tests, it can be concluded that the condition to be avoided (the only one that can be avoided) is unnecessary stray capacitance in circuit wiring. The charging of load capacitance, in most cases, overshadows the other two effects with respect to noise produced on the supply voltage line by switching current transients.

The flow paths of these currents have been investigated to determine the grounding and decoupling necessary to counteract their effects. Supply voltage decoupling may be accomplished by one of two methods. Maintaining low impedance from the individual circuit supply voltage to



NOTES: 1. V_{CC} = 5 V
2. Sweep is 50 ns/division
3. Rise and fall times of input pulse are 1 ns
4. Vertical scales are in units shown per division

Figure 37(a). Supply-Current Transient Comparisons



NOTES: 1. V_{CC} = 5 V
2. Sweep is 50 ns/division
3. Rise and fall times of input pulse are 1 ns
4. Vertical scales are in units shown per division

Figure 37(b). Supply-Current Transient Comparisons

ground is common to both methods. In the first method, the supply voltage line may be considered as a transmission line back to a low impedance supply. The positive bus can be laminated with a ground bus to form a strip transmission line of extremely low impedance. This line can be electrically approximated with lumped capacitances as shown in Figure 38. The inductances are usually a distributed component which must be minimized to lower the line impedance.

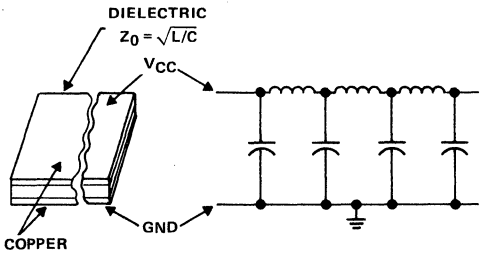


Figure 38. Transmission-Line Power Buses

The second method is to consider the supply voltage bus as a dc connecting element only and to provide a low-impedance path near the devices for the transient currents to be grounded (Figure 39).

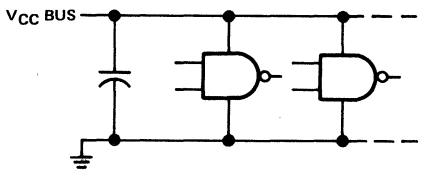


Figure 39. Capacitive Storage Supply Voltage System

For effective filtering and decoupling, the capacitors must be able to supply the change in current for a period of time greater than the pulse width of this current. Since the problem is essentially one of dc changes due to logic state coupled with high-frequency transients associated with the changes, two different values of time constant must be considered. Capacitors combining the high capacitance required for long periods with the low series reactance required for fast transients are prohibitive in cost and size. A good compromise is the arrangement shown in Figure 40.

The typical component values may be found for the RF capacitor C1 by assuming that the parameters have common values as follows:

$\Delta I_{CC} = 50$ mA
$\Delta V = 0.1$ V
$\Delta T = 20$ ns

Then the equation is as follows:

$$C1 = \frac{\Delta I_{CC}}{\Delta V/\Delta T} = \frac{(50)(20) \times 10^{-12}}{0.1/(20 \times 10^{-9})}$$

$$= \frac{50 \times 10^{-3}}{0.1} = 10{,}000 \times 10^{-12}$$

$$= 0.01\ \mu F$$

The same method may be used for the low-frequency capacitor C2. However, the factor ΔT, which was a worst-case transient time for calculating C2, now becomes a bit ambiguous. An analysis of the current cycling on a statistical basis is the best method in all but the simplest systems. The recommended procedure is to decouple using 10 μF to 50 μF capacitors.

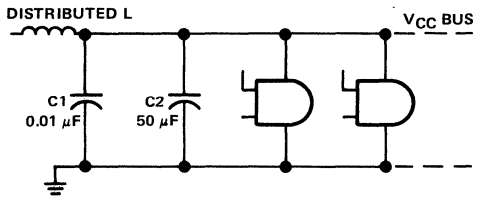


Figure 40. Commonly Used Power Distribution and Decoupling System

A discrete inductance of 2 μH to 10 μH is sometimes used for additional decoupling. However, its benefits are questionable and its usefulness should be evaluated for the individual system. The low-pass filter formed must be capable of keeping the transients confined and off the distribution bus. The possibility of resonance in the inductor or LC combination must be considered.

Noise spikes on the supply voltage line that do not force the gate output below the threshold level do not present a serious problem. Downward spikes as large as 3 V can be tolerated on the supply voltage line without propagating through the logic system. The system designer can be confident that supply voltage noise can be handled even with minimal consideration.

Ground noise, however, cannot be treated lightly. Pulses on a high-impedance ground line can easily exceed the noise threshold. Only if a good ground system is maintained can this problem be overcome. If proper attention is paid to the ground system, noise problems can be minimized.

The concept of a common-ground-plane structure as used in RF and high-speed digital systems is quite different from the concept of the common-ground point as used in low-frequency circuits. The more closely the chassis and ground can approach to being an integral unit, the better the noise suppression characteristics of the system. Consequently, all

parts of the chassis and ground bus system must be bound tightly together both electrically and mechanically. Floating or poorly grounded sections not only break the integrity of the ground system, but may actually act as a noise distribution system.

For grounds and decoupling on printed circuit boards, the most desirable arrangement is a double-clad or multilayer board with a solid ground plane or a mesh. Where component density prohibits this, the ideal should be relaxed only as far as necessary. Cross talk and ground noise can be reduced on large boards with a ground plane. Some suggestions for board grounds where a plane is not practical are as follows:

1. Use as wide a ground strap as possible.
2. Form a complete loop around the board by bringing both sides of the board through separate pins to the system ground.

The supply voltage line can provide part of the ground mesh on the board, provided it is properly decoupled. For a TTL system, a good guideline is 0.01 μF per synchronously driven gate and at least 0.1 μF for each 20 gates, regardless of synchronization. This capacitance may be lumped, but is more effective if distributed over the board. A good rule is to permit no more than 5 inches of wire between any two package supply-voltage points. Radio-frequency-type capacitors must be used for decoupling. Disk ceramics are best. It is sometimes a good practice to decouple the board from the external supply-voltage line with a 2.2 μF capacitor. However, this is optional and the RF capacitors are still required. In addition, it is recommended that gates driving long lines have the supply voltage decoupled at the gate supply voltage terminal and that the capacitor ground, device ground, and transmission-line ground be connected to a common point.

Cross Talk

When currents and voltages are impressed on a connecting line in a system, it is impossible for adjacent lines to remain unaffected. Static and magnetic fields interact and opposing ground currents flow, creating linking magnetic fields. These cross-coupling effects are lumped together and called cross talk.

Back-Panel Interconnections

Interconnecting signal lines can be grouped into three broad categories: coaxial lines, twisted-pair lines, and straight wire lines. Because of the low impedance and shielding characteristics of coaxial cable, its cross talk is minimal and is not a problem with TTL.

Figure 41 illustrates a practical type of signal transmission line. The mutual reactances L_m and C_m which form the noise coupling paths and the line parameters L_s and C_g which govern the line impedance, will vary with the type of line used. Since cross talk is a function of the ratio of the mutual impedances to the line characteristic impedances, the selection of transmission-line type must be at least partially a factor in cross-talk considerations.

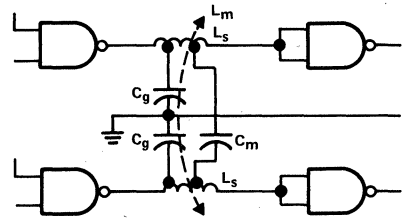


Figure 41. Equivalent Circuit for Sending Line

The use of direct-wired connections is the simplest and lowest cost method, but they are also the poorest for noise rejection. If the lead is not cabled tightly together with similar leads, direct leads up to 12 inches in length can be used.

When the length of the signal line is increased, the line impedance is seen by the driving and receiving gates. As shown in Figure 42, a pulse sent along the sending line G3 and G4 will be coupled via the coupling impedance Z_c onto the receiving line G1 and G2, which can be in either of the two logic states. The extent to which cross talk will occur depends on the type of lines used and their relationship to each other.

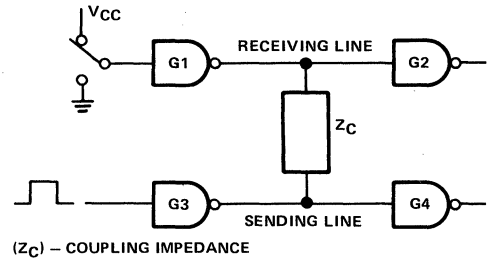


Figure 42. Equivalent Circuit for Cross Talk

The voltage impressed on the sending line by gate G3 is determined by the equation:

$$V_{SL} = \frac{V_{G3}Z_0}{R_{S3} + Z_0} \quad (5)$$

where

V_{G3} = open-circuit logic voltage swing generated by gate G3
R_{S3} = output impedance of gate G3
Z_0 = line impedance
V_{SL} = voltage impressed on the sending line.

The relationship for the equation is illustrated in Figures 43 and 44.

The coupling from the sending line to the receiving line can be represented by taking coupling impedance Z_c into

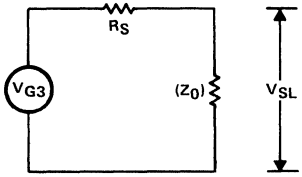


Figure 43. Capacitive Cross Talk Between Two Signal Lines

account. An equivalent circuit to represent the coupling from the sending line to the receiving line is shown in Figure 44.

As the voltage impressed on the sending line propagates farther along the line, it can be represented as voltage source V_{SL} with a source impedance of Z_{01} (Figure 45). V_{SL} is then coupled to the receiving line via the coupling capacitance, where the impedance looking into the line is line impedance in both directions. Therefore the equation becomes

$$V_{RL} = V_{SL} \frac{\frac{Z_0}{2}}{(1.5\ Z_0 + Z_c)}$$

The voltage impressed on the receiving line (V_{RL}) then propagates along the receiving line to gate G2 which can be considered as an open circuit and voltage doubling occurs. Therefore:

$$V_{in(2)} = 2\ V_{RL} = V_{G3}\left(\frac{1}{1.5 + \frac{Z_c}{Z_0}}\right)\left(\frac{Z_0}{RS3 + Z_0}\right)$$

In the switching period, the transistor has a very low output impedance. Then $R_{S3} \ll Z_0$ and $V_{in(2)}$ can be simplified to the following:

$$V_{in(2)} = V_{G3}\left(\frac{1}{1.5 + \frac{Z_c}{Z_0}}\right)$$

The term $V_{in(2)}/V_{G3}$ can be defined as the cross-talk coupling constant.

The worst-case for signal line cross talk occurs when sending and receiving lines are close together but widely separated from a ground return path. The lines then have a high characteristic impedance and a low coupling impedance.

For example, if we assume a coupling impedance of 50 pF at 150 MHz with a line impedance of approximately 200 Ω then:

$$\frac{V_{in(2)}}{V_{G3}} = 0.62$$

This level is unsatisfactory because none of the very high-speed logic circuits has a guaranteed noise margin greater than one-third of the logic swing. Such potential cross talk can be avoided by not using the close spacing of conductors.

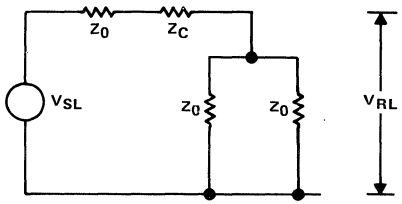


Figure 45. Equivalent Cross-Talk Network

Mutual coupling can be reduced by using coaxial cable or shielded twisted pairs. When mutual inductance and capacitance are decreased, line capacitance is increased and imposes restrictions on the driver. Coaxial cable combines very high mutual impedance with low characteristic impedance and shielding. It effectively eliminates cross talk, but is necessary in only the noisiest environments. Twisted pairs are adequate for most applications and are typically less expensive and easier to use.

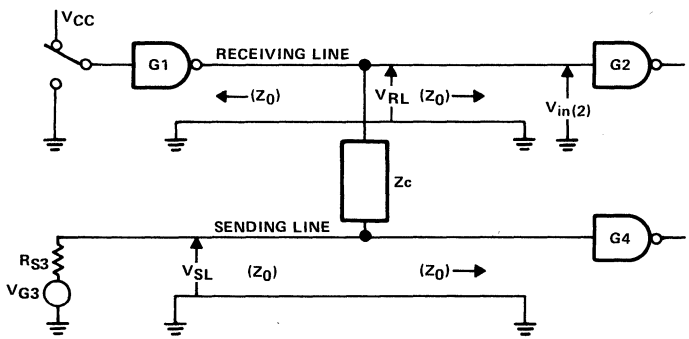


Figure 44. Coupling Impedances Involved in Cross Talk

Printed Circuit Card Conductors

Signal interconnections on a two-sided or multilayer printed circuit card can be grouped into two general categories: microstrip lines and strip lines. The microstrip line (Figure 46) consists of a signal conductor separated from a ground plane by a dielectric insulating material. A strip line (Figure 47) consists of a signal conductor within a dielectric insulating material and the conductor being centered between two parallel conductor planes. The important features of these type of printed circuit conductors are that the impedances are highly predictable, can be closely controlled, and the process is relatively inexpensive because standard printed circuit board manufacturing techniques are used. Typical impedances of these types of conductors with respect to their physical size and relative spacings are shown in Tables 7 and 8.

Table 7. Typical Impedance of Microstrip Lines

Dimensions		Line Impedance	Capacitance
H (mils)	W (mils)	Z_O (Ω)	per Foot (pF)
6	20	35	40
6	15	40	35
15	20	56	30
15	15	66	26
30	20	80	20
30	15	89	18
60	20	105	16
60	15	114	14
100	20	124	13
100	15	132	12

Relative dielectric constant ≈5

Table 8. Typical Impedance of Strip Lines

Dimensions		Line Impedance	Capacitance
H'a = H'b = (mils)	W (mils)	Z_O (Ω)	per Foot (pF)
6	20	27	80
6	15	32	70
10	20	34	67
10	15	40	56
12	20	37	57
12	15	43	48
20	20	44	48
20	15	51	42
30	20	55	39
30	15	61	35

Relative dielectric constant ≈5, and H'a = H'b

Cross talk on a printed circuit board is also a function of the mutual reactances and the line parameters which govern the line impedance. A microstrip line and a strip line are, by definition, conductors placed relatively close to a ground plane. Therefore, they have at least one inherent property which tends to reduce cross talk. In addition, the thickness (H) of the dielectric and the spacing (S) of the conductors can be implemented selectively to reduce the amount of possible cross talk. The effects of these two dimensions on cross talk have been evaluated and are shown graphically in Figure 48. The data shown can be used to estimate the maximum crosstalk which will be encountered under the most unfavorable conditions.

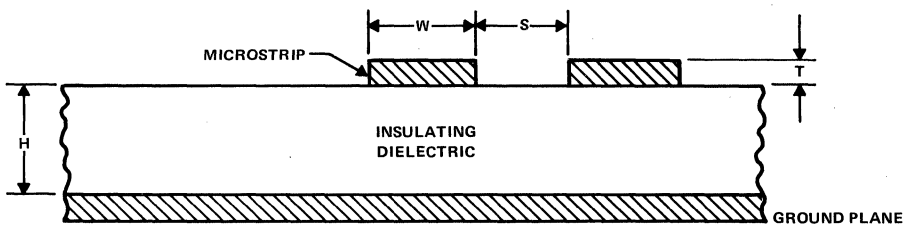


Figure 46. Microstrip Line

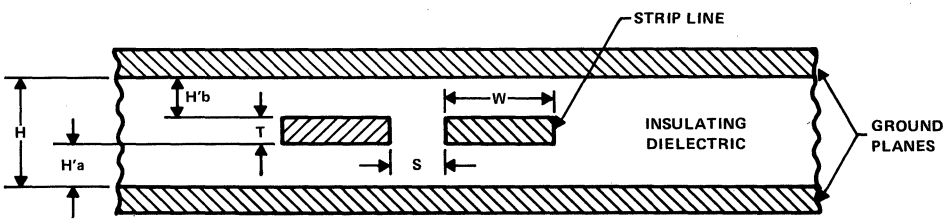


Figure 47. Strip Line

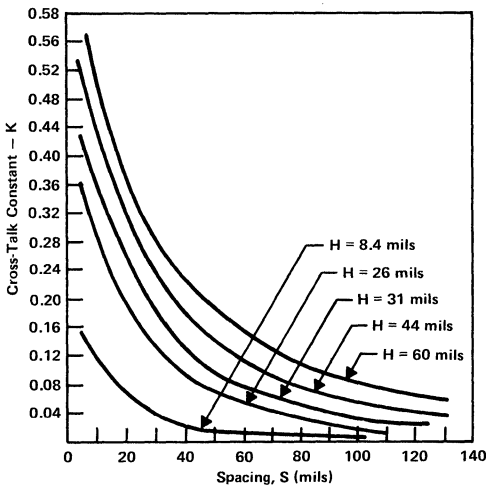


Figure 48. Line Spacing Versus Cross-Talk Constant

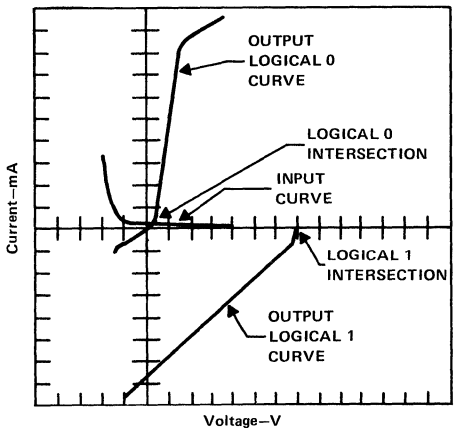


Figure 49. TTL Bergeron Diagram

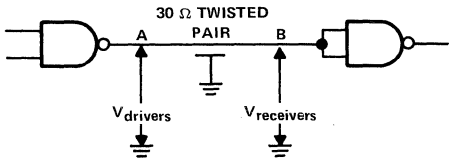


Figure 50. 'ALS/'AS Driving Twisted Pair

Transmission-Line Driving Reflections

When the interconnections used to transfer digital information become long enough so that line propagation delay is equal to or greater than the pulse transition times, the effects of reflections must be considered. These reflections are created because most TTL interconnections are not terminated in their characteristic impedance. Reflections lead to reduced noise margins, excessive delays, ringing, and overshoot. Some method must be used to analyze these reflections. Because neither the gate input nor output impedance is linear, basic transmission-line equations are applicable but unwieldy. Transmission-line characteristics of TTL interconnections can be analyzed by using a simple graphic technique.

Figure 49 shows piecewise linear plots of a gate input and both (logic-high and logic-low) states of the output for a typical TTL device. The output curves are plotted with positive slopes. The input is inverted because it is at the receiving end of a transmission line. The logic-high and logic-low intersections are indicated on the plot. These points are the steady-state values which will be observed on a lossless transmission line (Figure 50).

Figure 50 shows a typical TTL interconnection using a twisted-pair cable which, in this example, has a characteristic impedance of approximately 30 Ω. To evaluate a logic-high to logic-low 'AS transition see Figures 51 and 52. The equation $-1/Z_0$ (Z_0 = 30 Ω), which represents the transmission line, is superimposed on the output characteristic curves in the Bergeron plot. Since evaluation of a logic-high to logic-low transition is desired, the $-1/Z_0$ line starts at the point of intersection of the impedance curves of the input and output for a logic-high state. The slope $-1/Z_0$ then proceeds toward the logic-low output curve. At time t_0, the driver output voltage is determined by the intersection of $-1/Z_0$ and the logic-low output curve (1.2 V). The transmission-line slope now becomes $1/Z_0$ and is drawn toward the input curve. At time t_1 [$t_{(n+1)} - t_n$ = time delay of line], the receiving gate sees −0.7 V. Now the line slope changes back to $-1/Z_0$ and the output curve for a logic low is approached. This action continues until the logic-low intersection is reached. Figure 52 plots driver and receiver voltages versus time for this example.

A logic-low to logic-high transition is treated in approximately the same manner (Figure 53). The Bergeron line $-1/Z_0$ starts at the intersection for a logic low. At time t_0, the driver output rises to 2.2 V and, at time t_1, the receiving gate input goes to approximately 4.35 V. Both output and input voltages are plotted in Figure 54.

Figures 55 through 58 illustrate 'ALS transitions and are treated in the same manner as the 'AS.

The scope photographs in Figures 59 through 66 show the effectiveness of the graphic techniques. In most cases, the calculated and experimental values of voltage steps agree within reason. The ringing that appears for the open wire is not immediately obvious. This is because the input and output curves in this region lie practically along the positive horizontal axis. At the scale used for graphic analysis, it is difficult to go much beyond the first few reflections. The graphic analysis is idealized and stray capacitance and inductance are not considered.

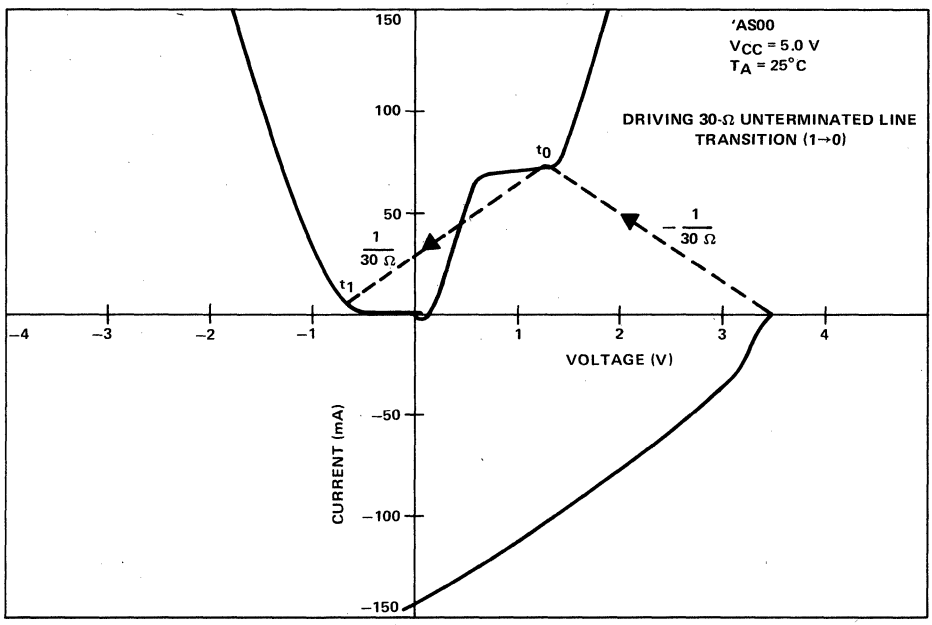


Figure 51. 'AS −ve Transition Bergeron Diagram

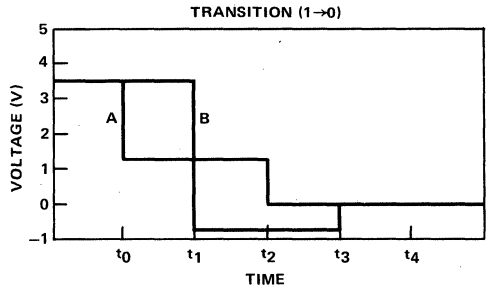


Figure 52. 'AS −ve Voltage/Time Plot

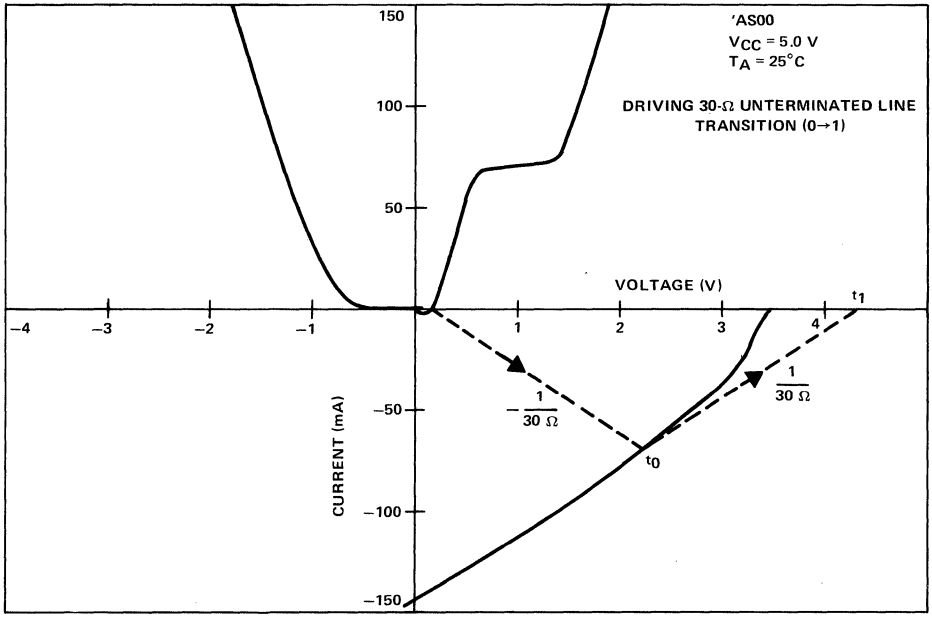


Figure 53. 'AS +ve Transition Bergeron Diagram

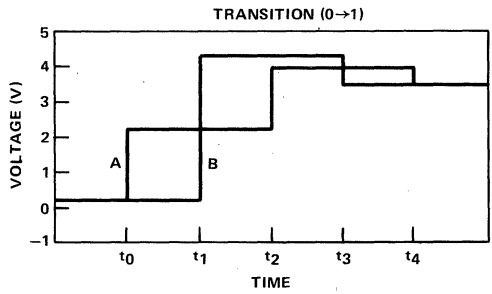


Figure 54. 'AS +ve Voltage/Time Plot

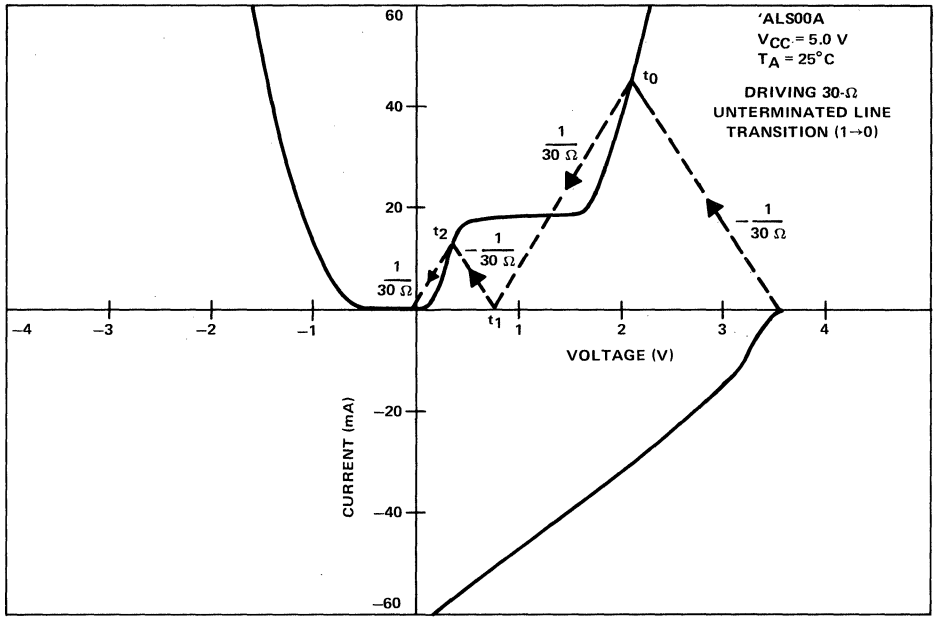


Figure 55. 'ALS −ve Transition Bergeron Diagram

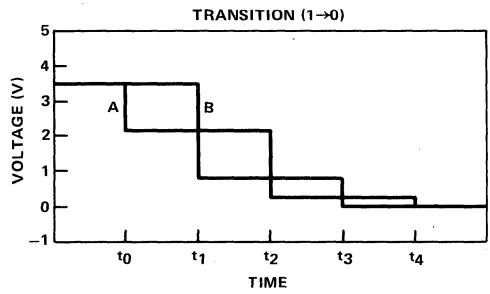


Figure 56. 'ALS −ve Voltage/Time Plot

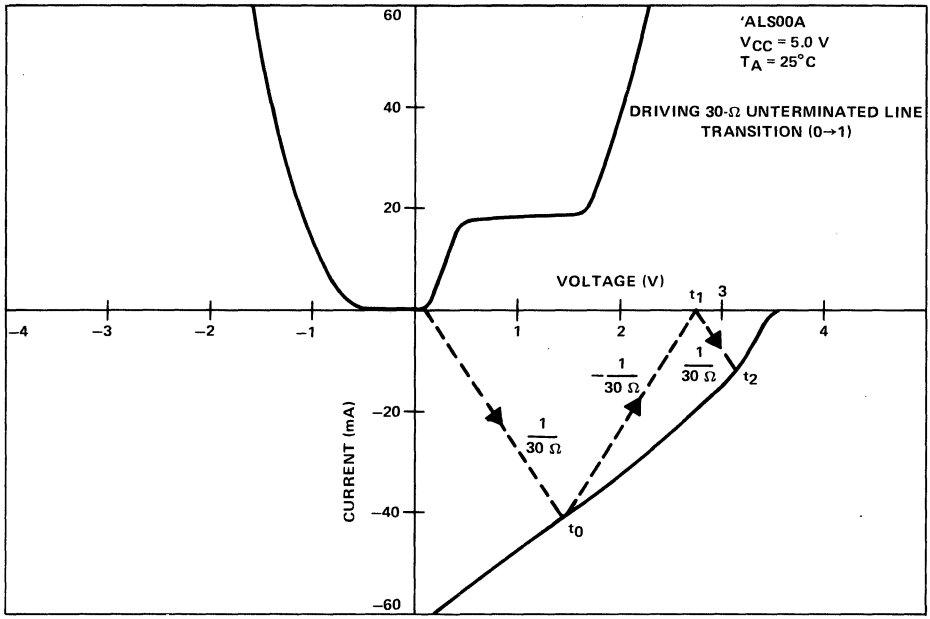


Figure 57. 'ALS +ve Transition Bergeron Diagram

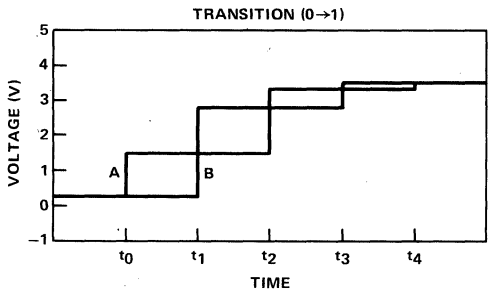


Figure 58. 'ALS +ve Voltage/Time Plot

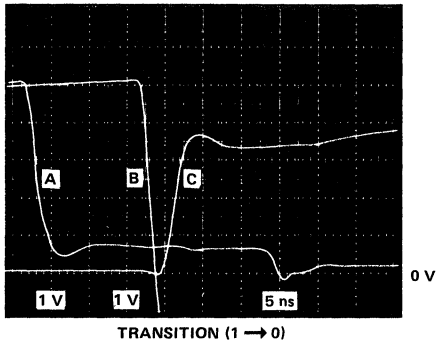


Figure 59. Oscilloscope Photograph of 'AS001 −ve Transition Using 50-Ohm Line

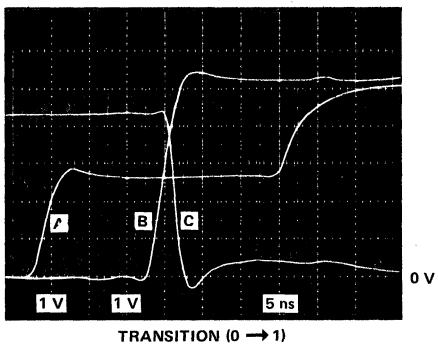


Figure 60. Oscilloscope Photograph of 'AS00 +ve Transition Using 50-Ohm Line

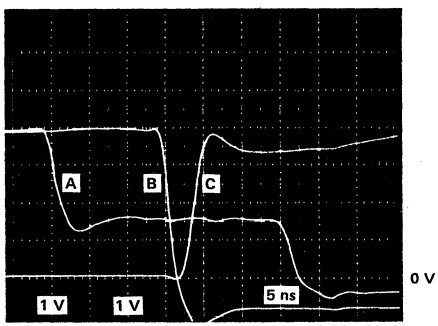


Figure 61. Oscilloscope Photograph of 'AS00 −ve Transition Using 25-Ohm Line

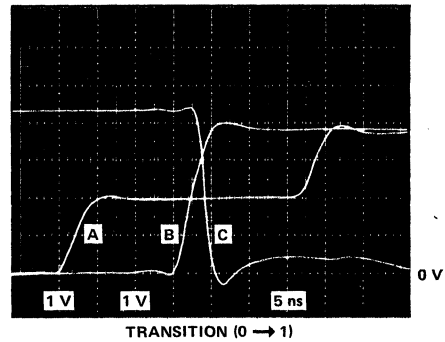


Figure 62. Oscilloscope Photograph of 'AS00 +ve Transition Using 25-Ohm Line

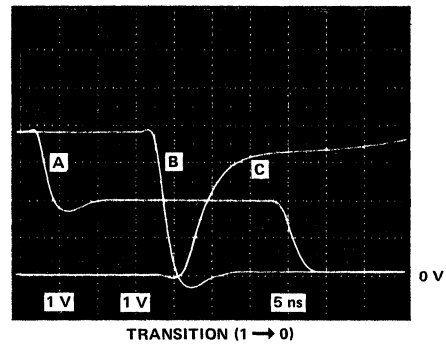


Figure 63. Oscilloscope Photograph of 'ALS00A −ve Transition Using 50-Ohm Line

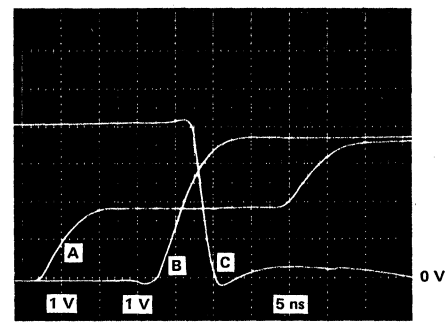


Figure 64. Oscilloscope Photograph of 'ALS00A +ve Transition Using 50-Ohm Line

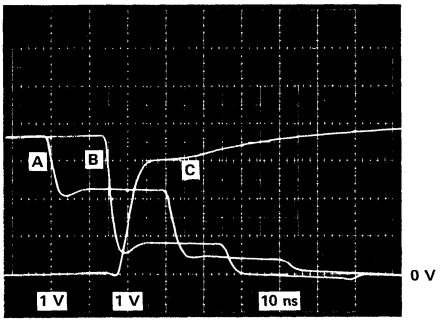


Figure 65. Oscilloscope Photograph of 'ALS00A −ve Transition Using 25-Ohm Line

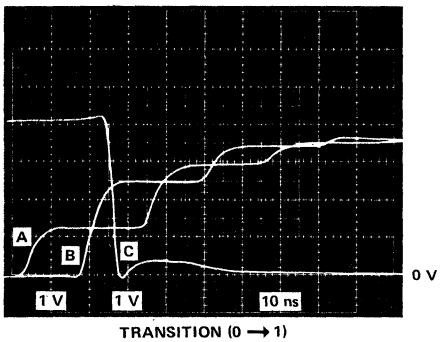


Figure 66. Oscilloscope Photograph of 'ALS00A +ve Transition Using 25-Ohm Line

References

1. W.C. Elmore and M. Sands, *Electronics Experimental Techniques,* McGraw-Hill Book Co., New York, 30ff. (1949).
2. M. Williams and S. Miller, *Series 54ALS/74ALS Schottky TTL Applications B215*, Texas Instruments Limited, Bedford, England, August 1982.

Acknowledgment

This application report is an updated version of Reference 2 with significant contributions by the technical engineering staff at Texas Instruments and particularly by Rock Cozad, Rich Moore, and Bob Strong.

Appendix A
Normalized Load Factors

Normalizing output drive capability and input current requirements can be very useful to designers of systems using two or more of the TI TTL series of devices. It provides a set of load factors (input cuurent requirements in Table A-1), which can be summed and compared directly to the fanout capability (see Table A-2) of the output being considered. The load factor values shown are valid for any input rated at one unit load.

The loading of these type of outputs can be checked from any column. However, most designs use one of the series as the basic building block and, since the tables cover each series individually, the designer has the choice of working from the column containing the normalized fanout. As an example, the designers of a system using series 'AS as the basic circuit will probably find that the use of the 'AS00 and 'AS1000 columns will suit best because both fanout and load factors are expressed for these series of devices.

The use of these simple and easy-to-remember numbers was developed within each series to make the verification of output loading a matter of counting the number of inputs connected to a particular output. When mixtures of series are used, a common denominator (normalized factor) becomes useful.

USE OF TABLES A-1 AND A-2

Every possible combination of the seven 54/74 TTL families is included in these tables. If, for example, the existing system used 74S series logic and it is desired that some of it be replaced by series 74ALS logic, a quick check should be made on whether the 'ALS can be supplied with sufficient input current. By taking the 74S row and 'ALS, column figures of 2.5 and 20 are obtained for high- and low-level loads, respectively (see Table A-1). This indicates that, for high logic levels, two and one-half 'ALS gates can be driven for each 'S series gate removed. However, if more 74S series gates are being driven by this 'ALS device, the fanout between 'ALS and 'S series gate is required, you can now use Table A-2.

The 'ALS row and the 'S column are chosen. The figures are 8 for the high-logic level and 4 for the low-logic level. In this case the lowest figure is taken so that the interconnection is reliable for both logic states. So each 'ALS gate inserted will drive 4 'S series gates.

Table A-1. Normalized Input Currents

SERIES	I/O	INPUT CURRENT (mA)	INPUT CURRENT NORMALIZED								
			'00	'H00	'L00	'LS00	'S00	'AS00	'ALS00A	'AS1000	'ALS1000A
54/7400	HI	0.04	1	0.8	4	2	0.8	2	2	2	2
54/7400	LO	1.6	1	0.8	8.89	4	0.8	3.2	16	3.2	16
54H/74H00	HI	0.05	1.25	1	5	2.5	1	2.5	2.5	2.5	2.5
54H/74H00	LO	2	1.25	1	11.11	5	1	4	20	4	20
54/74L00	HI	0.01	0.25	0.2	1	0.5	0.2	0.5	0.5	0.5	0.5
54/74L00	LO	0.18	0.11	0.09	1	0.45	0.09	0.36	1.8	0.36	1.8
54LS/74LS00	HI	0.02	0.5	0.4	2	1	0.4	1	1	1	1
54LS/74LS00	LO	0.4	0.25	0.2	2.22	1	0.2	0.8	4	0.8	4
54S/74S00	HI	0.05	1.25	1	5	2.5	1	2.5	2.5	2.5	2.5
54S/74S00	LO	2	1.25	1	11.11	5	1	4	20	4	20
54AS/74AS00	HI	0.02	0.5	0.4	2	1	0.4	1	1	1	1
54AS/74AS00	LO	0.5	0.31	0.25	2.78	1.25	0.25	1	5	1	5
54ALS/74ALS00A	HI	0.02	0.5	0.4	2	1	0.4	1	1	1	1
54ALS/74ALS00A	LO	0.1	0.06	0.05	0.56	0.25	0.05	0.2	1	0.2	1
54AS1000	HI	0.02	0.5	0.4	2	1	0.4	1	1	1	1
54AS1000	LO	0.5	0.31	0.25	2.78	1.25	0.25	1	5	1	5
54ALS1000A	HI	0.02	0.5	0.4	2	1	0.4	1	1	1	1
54ALS1000A	LO	0.1	0.06	0.05	0.56	0.25	0.05	0.2	1	0.2	1

Table A-1 is normally used (in combination with Table A-2) when replacing one logic family with another in an existing system.

Table A-2 is normally used when originally designing a system which employs several TTL families to optimize performance.

Table A-2. Fanout Capability (Output Currents Normalized to Input Currents)

SERIES	I/O	OUTPUT CURRENT (mA)	OUTPUT DRIVE NORMALIZED								
			'00	'H00	'L00	'LS00	'S00	'AS00	'ALS00A	'AS1000	'ALS1000A
			*HI 0.04	0.05	0.01	0.02	0.05	0.02	0.02	0.02	0.02
			†LO 1.6	2	0.18	0.4	2	0.5	0.1	0.5	0.1
54/7400	HI	0.4	10	8	40	20	8	20	20	20	20
54/7400	LO	16	10	8	88.89	40	8	32	160	32	160
54H/74H00	HI	0.5	12.5	10	50	25	10	25	25	25	25
54H/74H00	LO	20	12.5	10	111.11	50	10	40	200	40	200
54L00	HI	0.1	2.5	2	10	5	2	5	5	5	5
54L00	LO	2	1.25	1	11.11	5	1	4	20	4	20
74L00	HI	0.2	5	4	20	10	4	10	10	10	10
74L00	LO	3.6	2.25	1.8	20	9	1.8	7.2	36	7.2	36
54LS/74LS00	HI	0.4	10	8	40	20	8	20	20	20	20
54LS00	LO	4	2.5	2	22.22	10	2	8	40	8	40
74LS00	LO	8	5	4	44.44	20	4	16	80	16	80
54S/74S00	HI	1	25	20	100	50	20	50	50	50	50
54S/74S00	LO	20	12.5	10	111.11	50	10	40	200	40	200
54AS/74AS00	HI	2	50	40	200	100	40	100	100	100	100
54AS/74AS00	LO	20	12.5	10	111.11	50	10	40	200	40	200
54ALS/74ALS00A	HI	0.4	10	8	40	20	8	20	20	20	20
54ALS00A	LO	4	2.5	2	22.22	10	2	8	40	8	40
74ALS00A	LO	8	5	4	44.44	20	4	16	80	16	80
54AS1000	HI	40	1000	800	4000	2000	800	2000	2000	2000	2000
54AS1000	LO	40	25	20	222.22	100	20	80	400	80	400
74AS1000	HI	48	1200	960	4800	2400	960	2400	2400	2400	2400
74AS1000	LO	48	30	24	266.67	120	24	96	480	96	480
54ALS1000A	HI	1	25	20	100	50	20	50	50	50	50
54ALS1000A	LO	12	7.5	6	66.67	30	6	24	120	24	120
74ALS1000A	HI	2	65	52	260	130	52	130	130	130	130
74ALS1000A	LO	24	15	12	133.33	60	12	48	240	48	240

*Input Current HI
†Input Curent LO

Appendix B

Letter Symbols, Terms, and Definitions

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronics Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use. The definitions are grouped into sections applying to voltages, currents, switching characteristics, and classification of circuit complexity.

VOLTAGES

V_{IH} High-level input voltage
An input voltage level within the more positive (less negative) of the two ranges of values used to represent the binary variables. A minimum value is specified which is the least-positive (most-negative) value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{IL} Low-level input voltage
An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables. A maximum value is specified which is the most-positive (least-negative) value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{T+} Positive-going threshold voltage
The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, V_{T-}.

V_{T-} Negative-going threshold voltage
The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, V_{T+}.

V_{OH} High-level output voltage
The voltage at an output terminal for a specified output current I_{OH} with input conditions applied that according to the product specification will establish a high level at the output.

V_{OL} Low-level output voltage
The voltage at an output terminal for a specified output current I_{OL} with input conditions applied that according to the product specification will establish a low level at the output.

$V_{O(on)}$ On-state output voltage
The voltage at an output terminal for a specified output current with input conditions applied that according to the product specification will cause the output switching element to be in the on state.

Note: This characteristic is usually specified only for outputs not having internal pull-up elements.

$V_{O(off)}$ Off-state output voltage
The voltage at an output terminal for a specified output current with input conditions applied that according to the specification will cause the output switching element to be in the off state.

Note: This characteristic is usually specified only for outputs not having internal pull-up elements.

CURRENT

I_{IH} High-level input current
The current flowing into* an input when a specified high-level voltage is applied to that input.

I_{IL} Low-level input current
The current flowing into* an input when a specified low-level voltage is applied to that input.

*Current flowing out of a terminal is a negative value.

I_{OH} **High-level output current**
The current flowing into* the output with a specified high-level output voltage V_{OH} applied.

Note: This parameter is usually specified for open-collector outputs intended to drive other logic circuits.

$I_{O(off)}$ **Off-state output current**
The current flowing into* an output with a specified output voltage applied and input conditions applied that according to the product specification will cause the output switching element to be in the off state.

Note: This parameter is usually specified for open-collector outputs intended to drive devices other than logic circuits or for three-state outputs.

I_{OS} **Short-circuit output current**
The current flowing into* an output when that output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potential).

I_{CCH} **Supply current, output(s) high**
The current flowing into* the V_{CC} supply terminal of a circuit when the reference output(s) is (are) at a high-level voltage.

I_{CCL} **Supply current, output(s) low**
The current flowing into* the V_{CC} supply terminal of a circuit when the reference output(s) is (are) at a low-level voltage.

DYNAMIC CHARACTERISTICS

f_{max} **Maximum clock frequency**
The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause a change of output state with each clock pulse.

t_{HZ} **Output disable time (of a three-state output) from high level**
The time between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined high level to a high-impedance (off) state.

t_{LZ} **Output disable time (of a three-state output) from low level**
The time between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined low level to a high-impedance (off) state.

t_{PLH} **Propagation delay time, low-to-high-level output**
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.

t_{PHL} **Propagation delay time, high-to-low-level output**
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

t_{TLH} **Transition time, low-to-high-level output**
The time between a specified low-level voltage and a specified high-level voltage on a waveform that is changing from the defined low level to the defined high level.

t_{THL} **Transition time, high-to-low-level output**
The time between a specified high-level voltage and a specified low-level voltage on a waveform that is changing from the defined high level to the defined low level.

t_w **Average pulse width**
The time between 50% amplitude points (or other specified reference points) on the leading and trailing edges of a pulse.

*Current flowing out of a terminal is a negative value.

t_h **Hold time**
The time interval for which a signal or pulse is retained at a specified input terminal after an active transition occurs at another specified input terminal.

$t_{release}$ **Release time**
The time interval between the release from a specified input terminal of data intended to be recognized and the occurrence of an active transition at another specified input terminal.

Note: When specified, the interval designated "release time" falls within the setup interval and constitutes, in effect, a negative hold time.

t_{su} **Setup time**
The time interval for which a signal is applied and maintained at a specified input terminal before an active transition occurs at another specified input terminal.

t_{ZH} **Output enable time (of a three-state output) to high level**
The time between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined high level.

t_{ZL} **Output enable time (of a three-state output) to low level**
The time between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined low level.

CLASSIFICATION OF CIRCUIT COMPLEXITY

Gate equivalent circuit
A basic unit-of-measure of relative digital-circuit complexity. The number of gate equivalent circuits is that number of individual logic gates that would have to be interconnected to perform the same function.

LSI **Large-scale integration**
A concept whereby a complete major subsystem or system function is fabricated as a single microcircuit. In this context a major subsystem or system, whether logical or linear, is considered to be one that contains 100 or more equivalent gates or circuitry of similar complexity.

MSI **Medium-scale integration**
A concept whereby a complete subsystem or system function is fabricated as a single microcircuit. The subsystem or system is smaller than for LSI, but whether digital or linear, is considered to be one that contains 12 or more equivalent gates or circuitry of similar complexity.

SSI **Small-scale integration**
Integrated circuits of less complexity than medium-scale integration (MSI).

*Current flowing out of a terminal is a negative value.

Metastable Characteristics of Texas Instruments Advanced Bipolar Logic Families

Robert K. Breuninger and Kevin Frank

TEXAS INSTRUMENTS

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INTRODUCTION

At some point in every system designers career, they are faced with the problem of synchronizing two digital signals operating at two different frequencies. This problem is typically solved by synchronizing one of the signals, to the local clock, through a flip-flop. However, this solution presents an awkward dilemma, the setup and hold time specifications associated with the flip-flop are sure to be violated. The metastable characteristics of the flip-flop used can influence overall system reliability. The purpose of this application report is to give the system designer a better understanding of the metastable characteristics pertaining to Texas Instruments Advanced Schottky Bipolar Logic Family.

METASTABLE DEFINITION

Whenever a flip-flops setup and hold time is violated, the flip-flops output response is uncertain. Presently, there is no circuit that can 100% guarantee its response. This is why the device manufacturer does not guarantee its operation. Specifically, the metastable state is defined as that time period when the output of a digital logic device, is not at a logic level 1 (V_{out} less than 2 V) or a logic level 0 (V_{out} greater than 0.8 V), but instead between 0.8 V and 2 V. Since the input data is changing at the time of being clocked, the system designer does not care if the flip-flop goes to either a high or low logic level, just so long as the output does not hang up in the metastable region. The metastable characteristics for a particular flip-flop will determine how long the device stays in the metastable region. This concept is illustrated in the timing diagram of Figure 1.

METASTABLE EVALUATION

Anyone who has tried to evaluate the metastable characteristics for a particular flip-flop, has probably found it is not an easy task. The number of times the output hangs up in the metastable region is extremely small when compared to total number of clock transitions. In addition, the amount of time the output is actually in the metastable region is a variable and dependent on the type of flip-flop used (LS, ALS, AS, etc.).

From the design engineers viewpoint, when using a flip-flop as a data synchronizer, they can no longer use the specified data sheet maximum for propagation delay. Instead, to guarantee reliable system operation, they need to know how long after the specified data sheet maximum they need to wait before using the data. Conventional test equipment is not designed to measure these parameters, so a special test circuit is required for characterizing MTBF (Mean Time Between Failures) and Δt (time between CLK and Q valid). With these two parameters specified, the system designer can make a rational decision about what type of flip-flop to use, and how long to wait before using the data.

Circuit Description

The circuit in Figure 2 can be used in evaluating MTBF and Δt for a selected flip-flop (DUT, Device Under Test). Two 'AS04s are used to detect whenever the Q output of the DUT is in the metastable region. This is accomplished by adjusting the input threshold to 2 V on one inverter and 0.8 V on the other. Notice that input thresholds are adjusted by referencing the ground input pins to 0.6 V and −0.6 V respectively. Therefore, whenever the Q output of the DUT

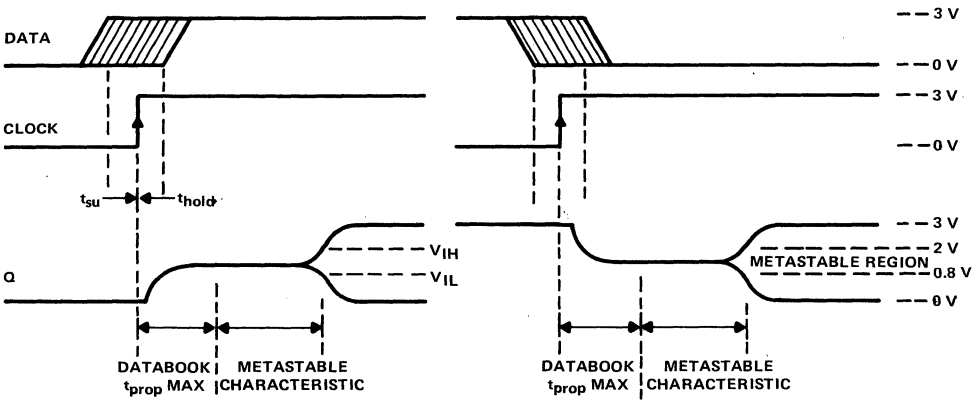


Figure 1. Metastable Timing Diagram

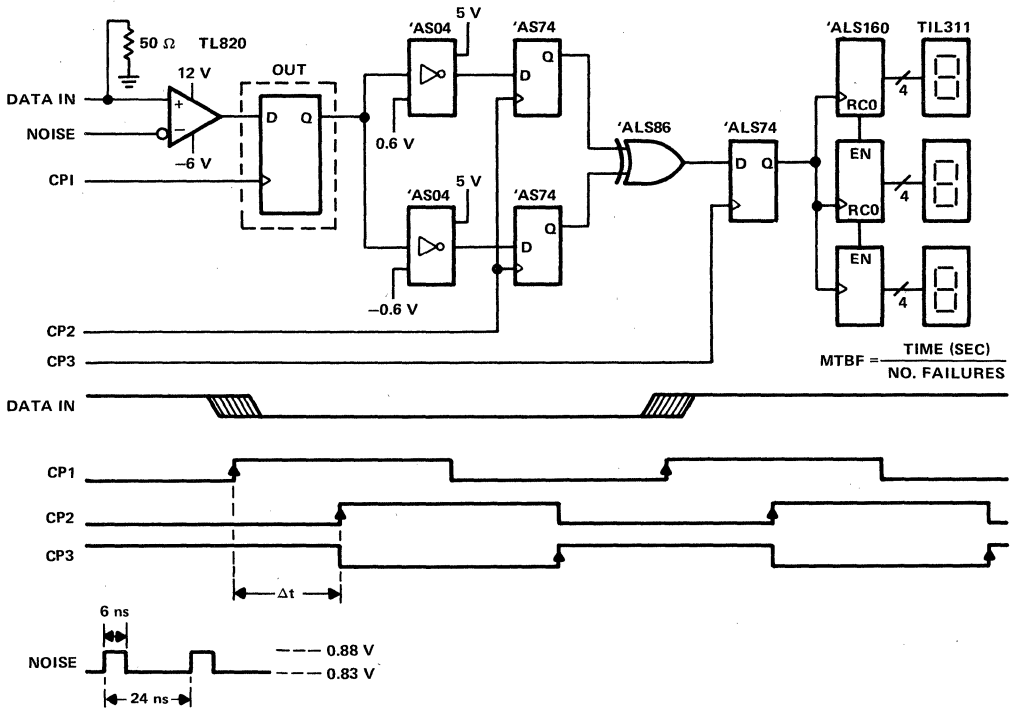


Figure 2. Metastable Evaluation Test Circuit

is between 0.8 V and 2 V, the inverters will be in opposite states. Whenever the Q output of the DUT is higher than 2 V or lower than 0.8 V, both inverters will be at the same logic level. The outputs of the 'AS04s are then clocked (CP2) into two 'AS74s a selected time (Δt) after the DUT clock (CP1). The outputs of the 'AS74s are compared through an 'ALS86 and clocked (CP3) into another 'ALS74. This guarantees against any false clocking by the evaluation circuit. The output of the 'ALS74 is then feed to a series of three 'ALS160 counters, and on into three TIL311s for counter display.

In order to maximize the possibility of forcing the DUT into a metastable state, the input data signal must jitter around the threshold of the input clock. The width of the jitter should equal, or exceed the setup and hold time specification for the device. In our evaluation circuit, this is accomplished by feeding a low level noise signal into the negative input of a TIL820 operational amplifier. The pictures shown in Figure 3 show the noise generated around the DUT clock (CP1) for both input data transitions.

It should be intuitively obvious that the worst-case condition, for any specified input data frequency, will be when the input data **always violates the data setup and hold times**. This condition is shown in the timing diagram of Figure 2. Any other relationship of CP1 to DATA IN, would provide less chance for the device to enter the metastable state. Therefore, it can be concluded that the worst-case condition for a given input data frequency, will be 0.5 times the DUT clock rate where the input data always violates the setup and hold time.

By using the described circuit, MTBF can be determined for several different values of Δt. Plotting this information on semilog paper reveals the metastable characteristics, for the selected flip-flop, at the desired input data frequency.

Test Circuit Limitations

Before we proceed to the AS/ALS test results, it is important to analyze the limitations of our test circuit. In this way, we can better understand its effects on the test results. Two major areas which can greatly affect the test results are not centering the jitter around the input clock, and propagation delay of the 'AS04s. By not centering the jitter around the input clock, the risk of entering the metastable state is reduced. Proper care must be taken to ensure that the jitter is always centered around the input clock to guarantee worst-case conditions.

The propagation delay of the 'AS04s affect the test results because they add propagation delay between the output of the DUT, and the data being clocked into the 'AS74s. For

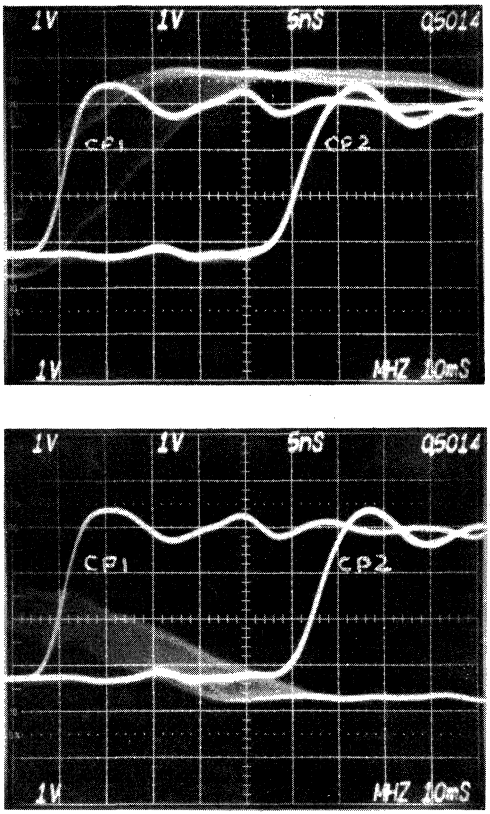


Figure 3. Test Waveforms

example, the output on the DUT may come out of the metastable region, but the 'AS04s may not switch before CP2 occurs. This causes an inappropriate reading. The typical propagation delay of the 'AS04s, **as configured in the test circuit**, is approximately 4 ns. This 4 ns delay should be considered when evaluating the test results. If inverters slower than the 'AS04s are used in the test circuit, a larger offset must be considered.

ALS/AS Test Results

Using the test circuit described in Figure 2, 'ALS74s, 'ALS273s and 'ALS374s were evaluated at several different Δt time periods. The input clock frequency used was 1 MHZ with an input data frequency of 500 kHz. The devices were allowed to run until an appropriate amount of errors were recorded. The number of errors were then divided by the total time the devices were allowed to run. This results in a MTBF for the selected Δt. The information was then recorded on semilog paper for analysis. It was found that all three device types exibited basically the same metastable characteristics within + 3 ns of each other. This was expected since all three device types come from the same technology. The same experiment was performed using AS and LS devices. The average characteristics for all three device families are shown in Figure 4. The 4-ns offset generated by the test circuit has not been subtracted from the data.

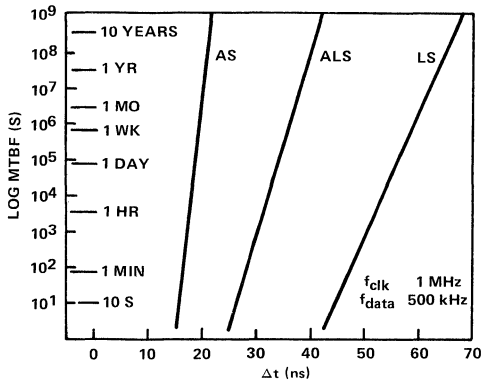


Figure 4. AS/ALS/LS Metastable Characteristics

Other Clock Frequencies

Clock frequencies other than 1 MHz will either increase or decrease the probability of the device entering the metastable state. The faster the frequency, the higher the probability of entering the metastable state. Likewise, the slower the frequency, the lower the probability of entering the metastable state. From the data taken in the above experiment, an equation can be derived for the metastable characteristics at other clock frequencies. Equation (1) relates input clock and data frequency, to metastable characteristics.

Metastable Equation

$$\frac{1}{\text{MTBF}} = f_{cp} \times f_{data} \times C1\ e^{(-C2\ \Delta t)} \qquad (1)$$

As stated earlier, the worst case situation for the test circuit shown in Figure 2, is when the data setup and hold time is always violated. Based on this assumption, the equation is reduced to the following.

$$\frac{1}{\text{MTBF}} = \frac{1}{2} f_{cp}^2 \times C1\ e^{(-C2\ \Delta t)} \qquad (2)$$

The constants C1 and C2 describe the metastable characteristics of the device. From the experimental data graphed in Figure 4, these constants can be solved for each device family. As an example, the constants are solved below for the ALS device family.

C2 is defined by the slope of the line. Picking two data points off the graph yields the following.

$$C2 = \frac{10^8 - 10^2}{40.2 - 28.2}(2.302) = \frac{6}{12}(2.302) = 1.151$$

By plugging C2 into equation 2, along with using one of the data points off the graph, C1 can be solved for.

$$\frac{1}{MTBF} = \frac{1}{2} f_{cp}^2 \times C1\, e^{(-1.51\,\Delta t)}$$

$$\frac{1}{10^8} = \frac{1}{2} (10^6)^2 \times C1\, e^{(-1.151 \times 40.2)}$$

$$C1 = 2.49$$

Inserting C1 and C2 into equation 2, yields the metastable equation for ALS.

$$\frac{1}{MTBF} = \frac{1}{2} f_{cp}^2 \times 2.49\, e^{(-1.151\,\Delta t)}$$

Given this worst-case equation, the system designer can determine the metastable characteristics for ALS when using other input clock frequencies.

The equations for AS and LS can be derived using the same procedure. They are as follows.

AS:

$$\frac{1}{MTBF} = \frac{1}{2} f_{cp}^2 \times 1.53 \times 10^7\, e^{(-2.92\,\Delta t)}$$

LS:

$$\frac{1}{MTBF} = \frac{1}{2} f_{cp}^2 \times 306\, e^{-0.783\,\Delta t)}$$

To get a feel for the effect of changing the input clock frequency, Figure 5 shows the change in the metastable characteristics from 1 MHz to 10 MHz.

METASTABLE CHARACTERISTICS OF PROGRAMMABLE LOGIC

The PAL16R4A and TIBPAL16R4-15 from the programmable logic family were also evaluated. They exhibited very similar characteristics to the ALS curve. This was expected because they utilize the same technology. One important consideration when evaluating programmable logic in the test circuit described, is positioning the jittery data a few nanoseconds before CP1. This compensates for the delay of the AND/OR array which is usually positioned in front of the flip-flop. Remember that the jittery data must be violating the setup and hold time at the input to the flip-flop, not just at the device input. Some experimentation is usually required to find the worst-case condition.

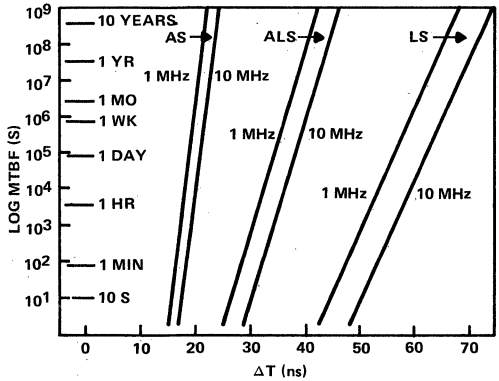


Figure 5. AS/ALS/LS Metastable Characteristics Variation with Frequency

As a general rule, a system designer can usually get a feel for the metastable characteristics of a device by simply looking at the setup and hold time specifications. Usually, the smaller the setup and hold time numbers, the better its metastable characteristics will be. However, in the case of programmable logic, the setup and hold time numbers are not reflective of metastable characteristics. This is because the setup and hold time numbers also reflect the propagation delay time of the AND/OR logic in front of the flip-flops.

SUMMARY

The metastable characteristics of a flip-flop used for data synchronization can greatly affect system reliability. Based on the information presented in this application report, the system designer can make a rational decision about what type of flip-flop to use, and what its metastable characteristics will be.

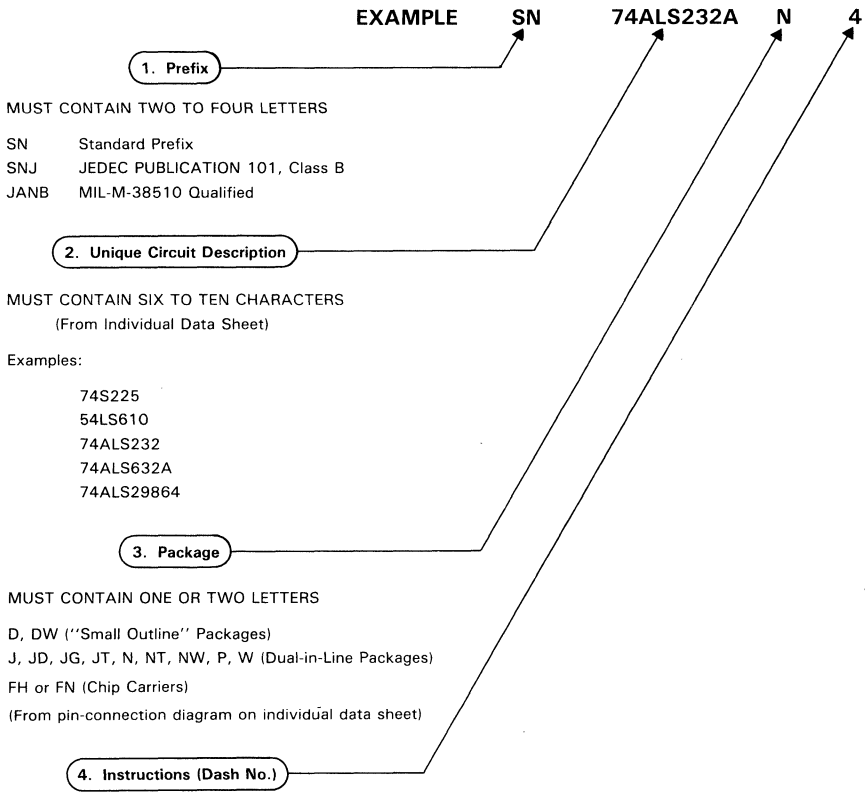
It is easy to see from the experimental data shown in Figure 4, that AS offers the best metastable characteristics. It has a much narrower setup and hold time window, and is quicker to recover once it gets into the metastable region. However, with adequate sampling time, ALS and LS will also perform well. The selection of what type of flip-flop to use must be based on the speed of the application. As a general rule, the faster the flip-flop, the better its metastable characteristics.

We at Texas Instruments believe that the graphs shown and equations derived, represent a reasonable assumption about the metastable characteristics for the device families discussed. However, we strongly recommend that when using flip-flops as data synchronizers, an adequate amount of guardband is allowed between the characteristics shown, and when the output of the flip-flop is actually sampled.

ORDERING INSTRUCTIONS

Electrical characteristics presented in this data book, unless otherwise noted, apply for circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this catalog should include a four-part type number as explained in the following example.



3 PEP processing, level 3 (N or NT packages only)

†These circuits in dual-in-line and "small outline" packages are shipped in one of the carriers shown below. Unless a specific method of shipment is specified by the customer (with possible additional costs), circuits will be shipped in the most practical carrier. Please contact your TI sales representative for the method that will best suit your particular needs.

"Small Outline" (D, DW)
Dual-in-Line (J, JD, JG, JT, N, NT, NW, P, W)

– A-Channel Plastic Tubing

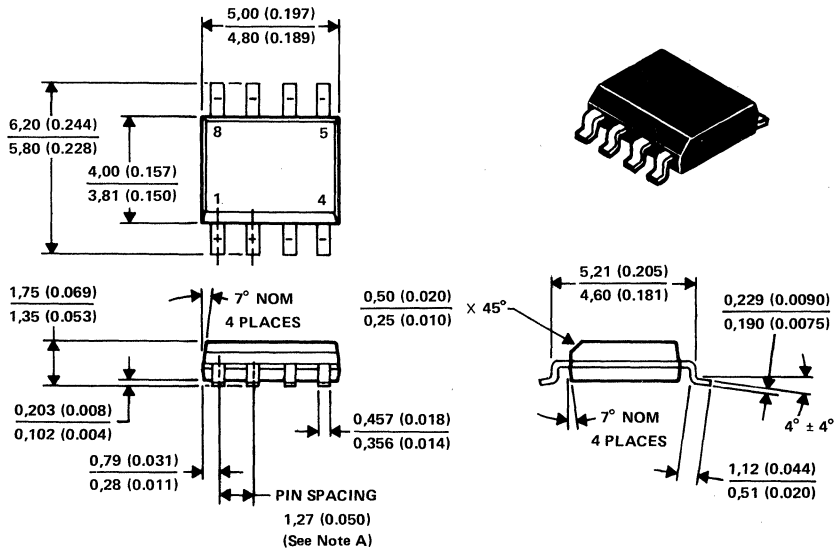
– Tape and Reel

– Barnes Carrier (W only)

D plastic "small outline" packages

Each of these "small outline" packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

8-PIN D PLASTIC



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Body dimensions do not include mold flash or protrusion.
B. Mold flash or protrusion shall not exceed 0,15 (0.006).
C. Leads are within 0,25 (0.010) radius of true position at maximum material dimension.
D. Lead tips to be planar within ±0,051 (0.002) exclusive of solder.

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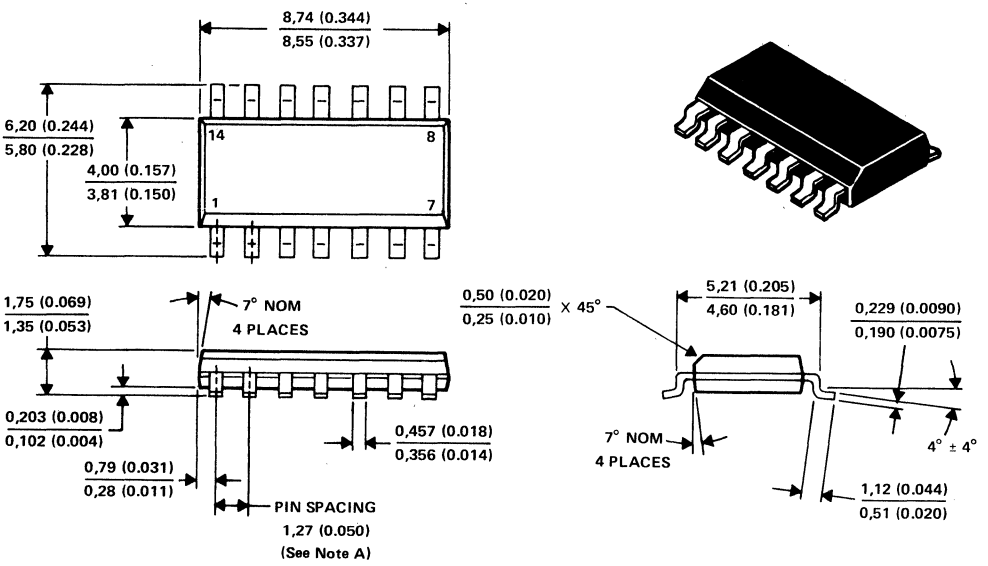
14-PIN D PLASTIC



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

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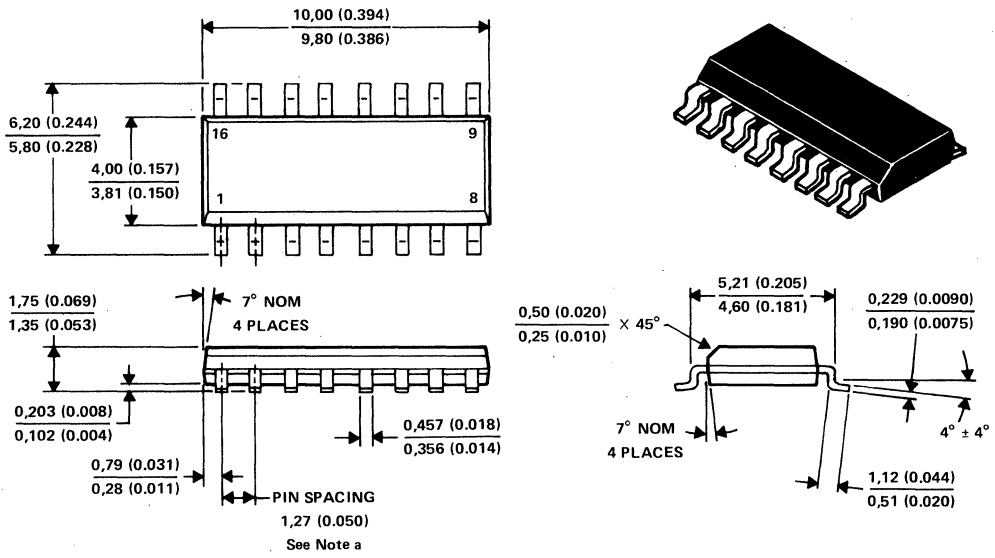
16-PIN D PLASTIC



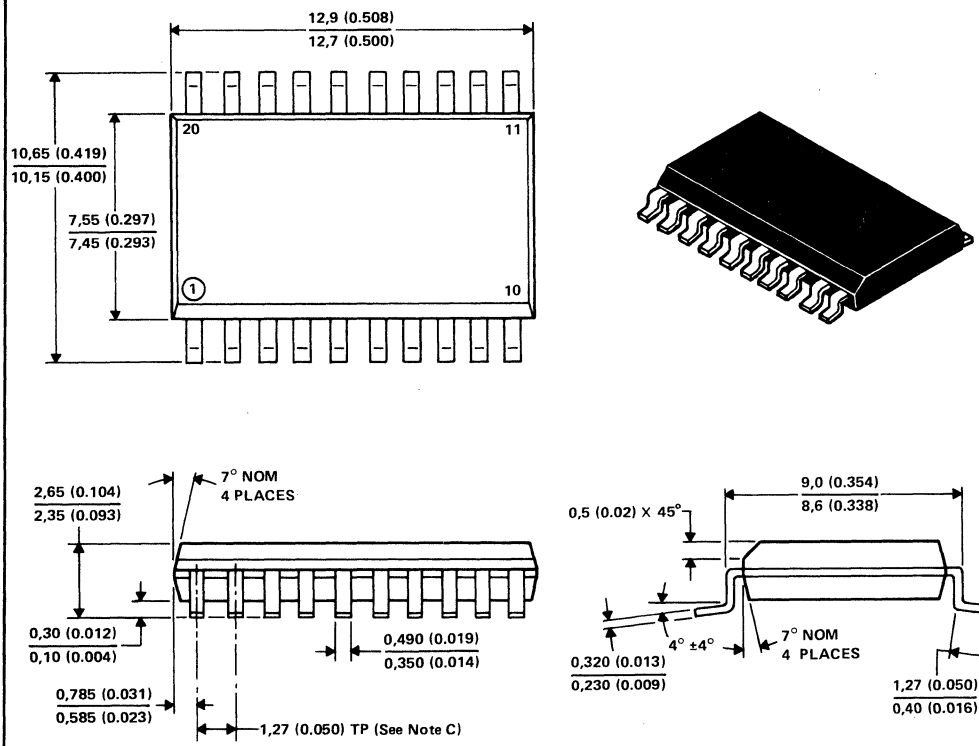
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Body dimensions do not include mold flash or protrusion.
B. Mold flash or protrusion shall not exceed 0,15 (0.006).
C. Leads are within 0,25 (0.010) radius of true position at maximum material dimension.
D. Lead tips to be planar within ±0,051 (0.002) exclusive of solder.

DW plastic "small outline" packages

Each of these "small outline" packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

20-PIN DW PLASTIC



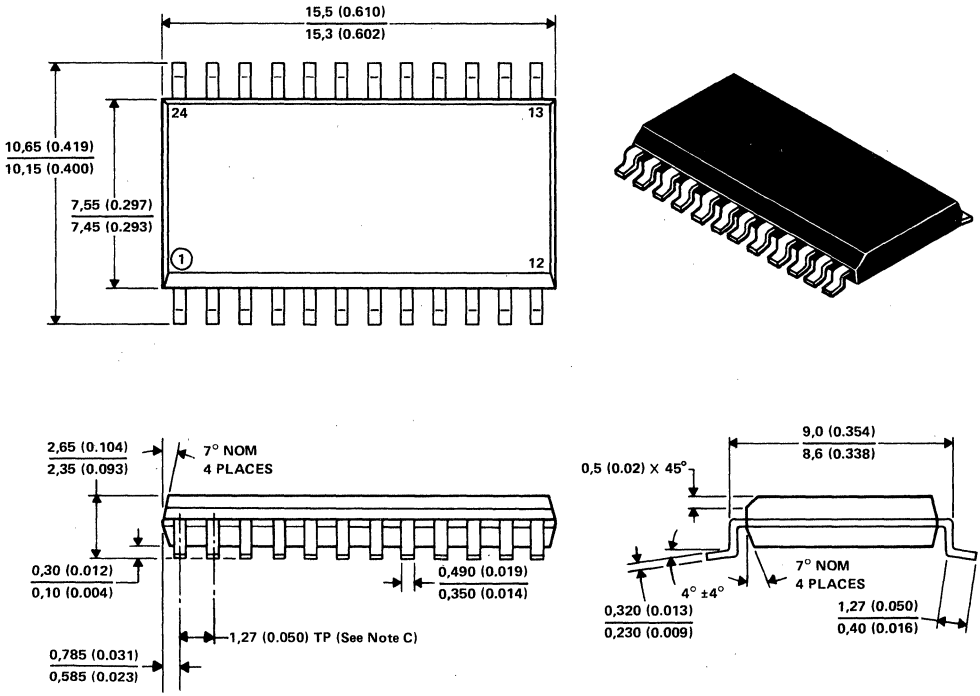
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Body dimensions do not include mold flash or protrusion.
B. Mold flash or protrusion shall not exceed 0,15 (0.006).
C. Leads are within 0,25 (0.010) radius of true position at maximum material dimension.
D. Lead tips to be planar within ±0,051 (0.002) exclusive of solder.

DW plastic "small outline" packages

Each of these "small outline" packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

24-PIN DW PLASTIC



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Body dimensions do not include mold flash or protrusion.
B. Mold flash or protrusion shall not exceed 0,15 (0.006).
C. Leads are within 0,25 (0.010) radius of true position at maximum material dimension.
D. Lead tips to be planar within ±0,051 (0.002) exclusive of solder.

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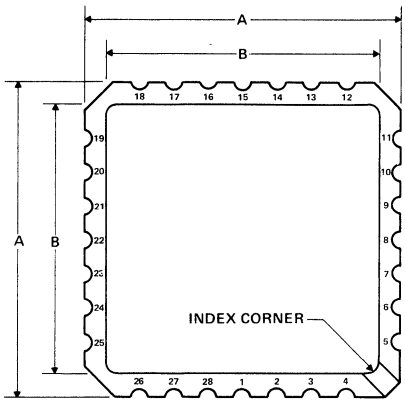
FK ceramic chip carrier packages

Each of these hermetically sealed chip carrier packages has a three-layer ceramic base with a metal lid and braze seal. The packages are intended for surface mounting on solder lands on 1,27 (0.050-inch) centers. terminals require no additional cleaning or processing when used in soldered assembly.

FK package terminal assignments conform to JEDEC Standards 1 and 2.

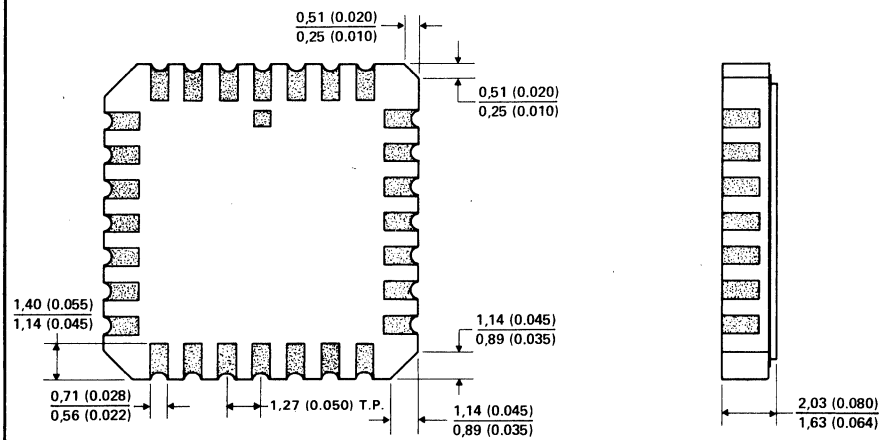
FK CERAMIC CHIP CARRIER
(28-terminal package shown)



CERAMIC CHIP CARRIERS

JEDEC OUTLINE DESIGNATION*	NO. OF TERMINALS	A MIN	A MAX	B MIN	B MAX
MS004CB	20	8,69 (0.342)	9,09 (0.358)	7,80 (0.307)	9,09 (0.358)
MS004CC	28	11,23 (0.442)	11,63 (0.458)	10,31 (0.406)	11,63 (0.458)

*All dimensions and notes for the specified JEDEC outline apply.

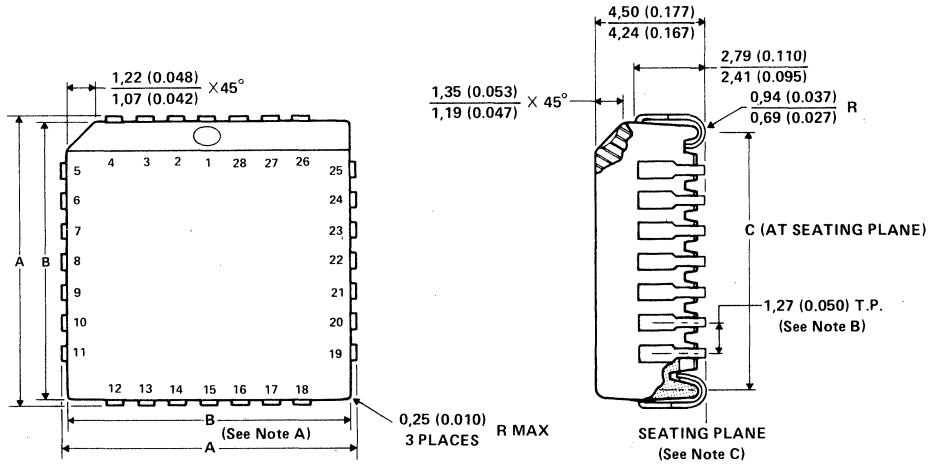


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

FN plastic chip carrier packages

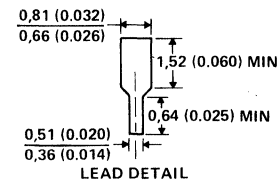
Each of these chip carrier packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound withstands soldering temperatures with no deformation, and circuit performance characteristics remain stable when the devices are operated in high-humidity conditions. The packages are intended for surface mounting on solder lands on 1,27 (0.050) centers. Leads require no additional cleaning or processing when used in soldered assembly.

FN PLASTIC CHIP CARRIER
(28-terminal package used for illustration)



JEDEC OUTLINE	NO. OF TERMINALS	A MIN	A MAX	B MIN	B MAX	C MIN	C MAX
MO 047AA	20	9,78 (0.385)	10,03 (0.395)	8,89 (0.350)	9,04 (0.356)	7,87 (0.310)	8,38 (0.330)
MO 047AB	28	12,32 (0.485)	12,57 (0.495)	11,43 (0.450)	11,58 (0.456)	10,41 (0.410)	10,92 (0.430)
MO 047AC	44	17,40 (0.685)	17,65 (0.695)	16,51 (0.650)	16,66 (0.656)	15,49 (0.610)	16,00 (0.630)
MO 047AE	68	25,02 (0.985)	25,27 (0.995)	24,13 (0.950)	24,33 (0.956)	23,11 (0.910)	23,62 (0.930)

All dimensions and notes for the specified JEDEC outline apply.



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Centerline of center pin each side within 0,10 (0.004) of package centerline as determined by dimension B.
B. Location of each pin is within 0,127 (0.005) of true position with respect to center pin on each side.
C. The lead contact points are planar within 0,10 (0.004)

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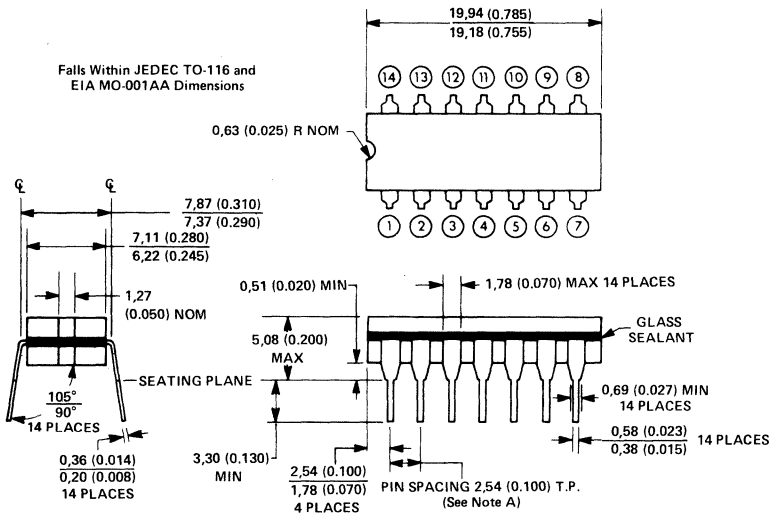
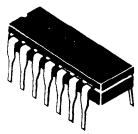
J ceramic dual-in-line packages (including JG, JT, and JW)

Each of these hermetically sealed dual-in-line packages consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The packages are intended for insertion in mounting-hole rows on 7,62 (0.300) or 15,24 (0.600) centers. Once the leads are compressed and inserted sufficient tension is provided to secure the package in the board during soldering. Tin-plated (''bright-dipped'') leads require no additional cleaning or processing when used in soldered assembly.

NOTE: For the 14-, 16-, and 20-pin packages, the letter J is used by itself since these packages are available only in the 7,62 (0.300) row spacing. For the 24-pin packages, if no second letter or row spacing is specified, the package is assumed to have 15,24 (0.600) row spacing.

14-PIN J CERAMIC





ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

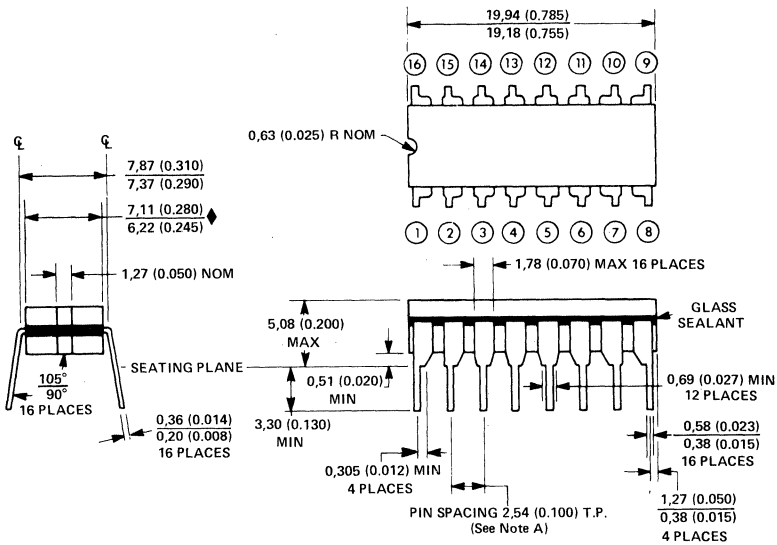
NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

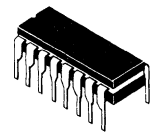
J ceramic dual-in-line packages (including JG, JT, and JW)

Each of these hermetically sealed dual-in-line packages consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The packages are intended for insertion in mounting-hole rows on 7,62 (0.300) or 15,24 (0.600) centers. Once the leads are compressed and inserted sufficient tension is provided to secure the package in the board during soldering. Tin-plated (''bright-dipped'') leads require no additional cleaning or processing when used in soldered assembly.

NOTE: For the 14-, 16-, and 20-pin packages, the letter J is used by itself since these packages are available only in the 7,62 (0.300) row spacing. For the 24-pin packages, if no second letter or row spacing is specified, the package is assumed to have 15,24 (0.600) row spacing.

16-PIN J CERAMIC





♦ For memories of 64 bits and up and a few MSI/LSI products in Series 54/74 and Series 54S/74S that are derived from memory circuit bars, this maximum is 7,62 (0.300). All other dimensions apply without modification.

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

TEXAS INSTRUMENTS
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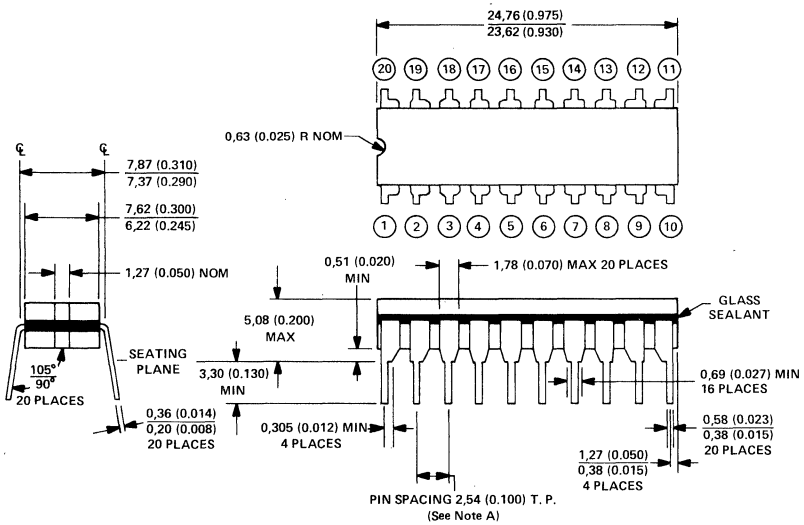
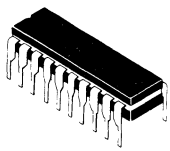
J ceramic dual-in-line packages (including JG, JT, and JW)

Each of these hermetically sealed dual-in-line packages consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The packages are intended for insertion in mounting-hole rows on 7,62 (0.300) or 15,24 (0.600) centers. Once the leads are compressed and inserted sufficient tension is provided to secure the package in the board during soldering. Tin-plated (''bright-dipped'') leads require no additional cleaning or processing when used in soldered assembly.

NOTE: For the 14-, 16-, and 20-pin packages, the letter J is used by itself since these packages are available only in the 7,62 (0.300) row spacing. For the 24-pin packages, if no second letter or row spacing is specified, the package is assumed to have 15,24 (0.600) row spacing.

20-PIN J CERAMIC





ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

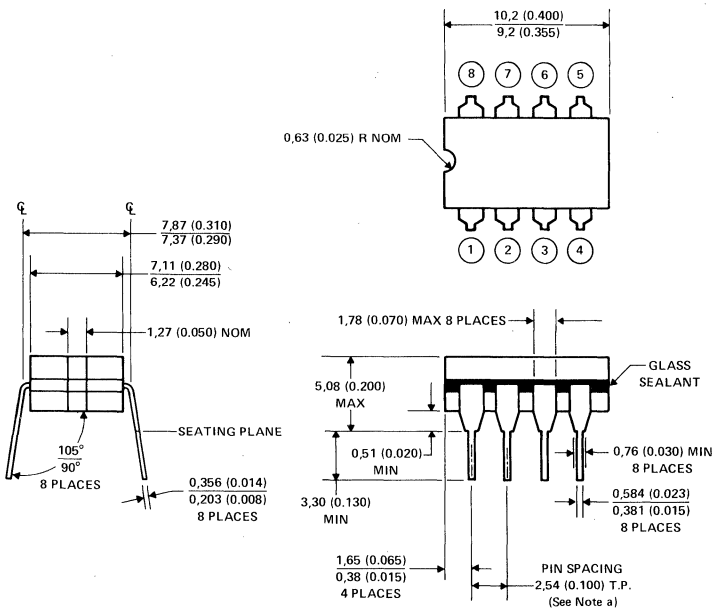
NOTE A: Each pin centerline is located within 0.25 (0.010) of its true longitudinal position.

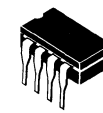
J ceramic dual-in-line packages (including JG, JT, and JW)

Each of these hermetically sealed dual-in-line packages consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The packages are intended for insertion in mounting-hole rows on 7,62 (0.300) or 15,24 (0.600) centers. Once the leads are compressed and inserted sufficient tension is provided to secure the package in the board during soldering. Tin-plated (''bright-dipped'') leads require no additional cleaning or processing when used in soldered assembly.

NOTE: For the 14-, 16-, and 20-pin packages, the letter J is used by itself since these packages are available only in the 7,62 (0.300) row spacing. For the 24-pin packages, if no second letter or row spacing is specified, the package is assumed to have 15,24 (0.600) row spacing.

8-PIN JG CERAMIC





ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

NOTE A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

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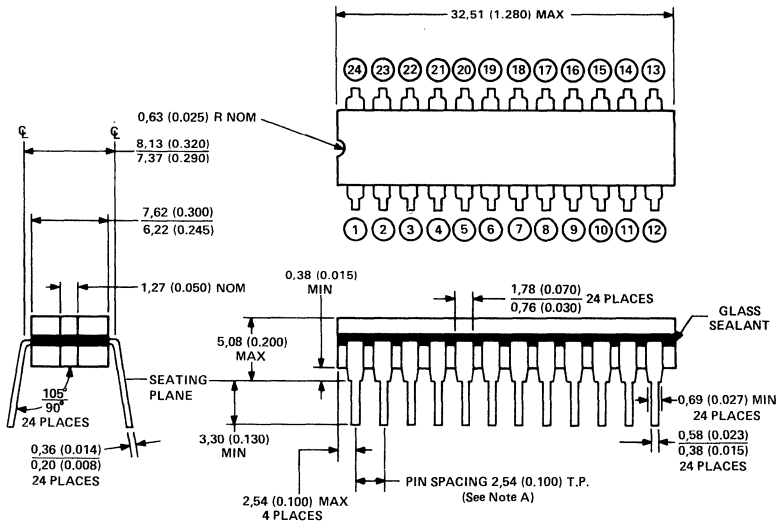
J ceramic dual-in-line packages (including JG, JT, and JW)

Each of these hermetically sealed dual-in-line packages consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The packages are intended for insertion in mounting-hole rows on 7,62 (0.300) or 15,24 (0.600) centers. Once the leads are compressed and inserted sufficient tension is provided to secure the package in the board during soldering. Tin-plated (''bright-dipped'') leads require no additional cleaning or processing when used in soldered assembly.

NOTE: For the 14-, 16-, and 20-pin packages, the letter J is used by itself since these packages are available only in the 7,62 (0.300) row spacing. For the 24-pin packages, if no second letter or row spacing is specified, the package is assumed to have 15,24 (0.600) row spacing.

24-PIN JT CERAMIC, 0.300-INCH ROW SPACING



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

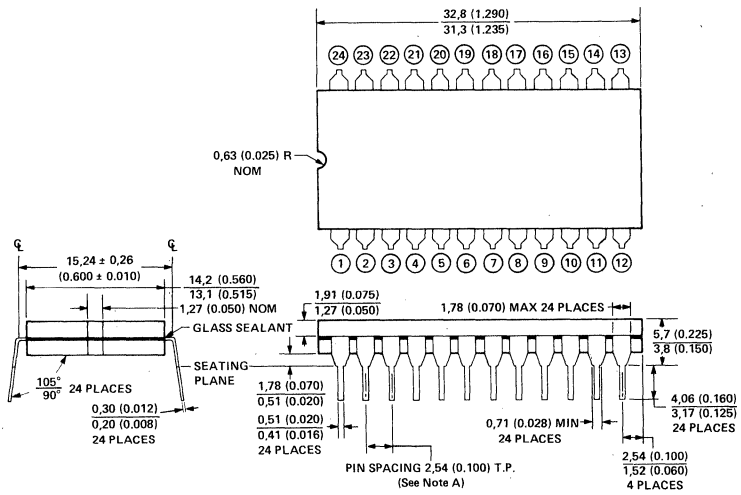
NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

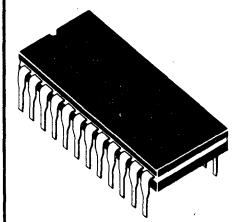
J ceramic dual-in-line packages (including JG, JT, and JW)

Each of these hermetically sealed dual-in-line packages consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The packages are intended for insertion in mounting-hole rows on 7,62 (0.300) or 15,24 (0.600) centers. Once the leads are compressed and inserted sufficient tension is provided to secure the package in the board during soldering. Tin-plated (''bright-dipped'') leads require no additional cleaning or processing when used in soldered assembly.

NOTE: For the 14-, 16-, and 20-pin packages, the letter J is used by itself since these packages are available only in the 7,62 (0.300) row spacing. For the 24-pin packages, if no second letter or row spacing is specified, the package is assumed to have 15,24 (0.600) row spacing.

24-PIN JW CERAMIC





Falls within JEDEC MO-015AA dimensions

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

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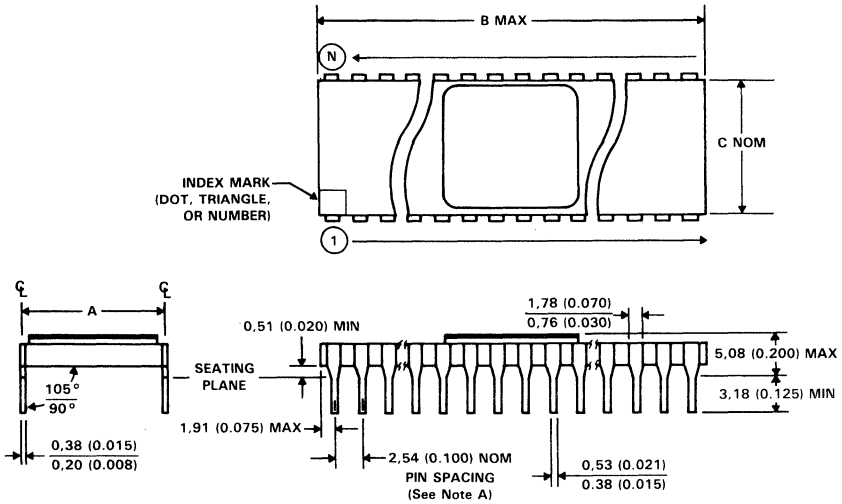
JD ceramic side-braze dual-in-line packages

This is a hermetically sealed ceramic package with a metal cap and side-brazed tin-plated leads.

JD CERAMIC—SIDE-BRAZE



DIM \ PINS (N)	16	18	20	22	24
A +0,51 (+0.020) −0,25 (−0.010)	7,62 (0.300)	7,62 (0.300)	7,62 (0.300)	7,62 (0.300)	7,62 (0.300)
B (MAX)	20,57 (0.810)	23,11 (0.910)	25,65 (1.010)	27,94 (1.100)	30,86 (1.215)
C (NOM)	7,37 (0.290)	7,37 (0.290)	7,37 (0.290)	9,91 (0.390)	7,37 (0.290)

DIM \ PINS (N)	24	28	40	48	52	64
A +0,51 (+0.020) −0,25 (−0.010)	15,24 (0,600)	15,24 (0.600)	15,24 (0.600)	15,24 (0.600)	15,24 (0.600)	22,86 (0.900)
B (MAX)	31,8 (1.250)	36,8 (1,450)	52,1 (2.050)	62,2 (2.450)	67,3 (2.650)	82,6 (3.250)
C (NOM)	15,0 (0.590)	15,0 (0.590)	15,0 (0.590)	15,0 (0.590)	15,0 (0.590)	22,6 (0.890)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

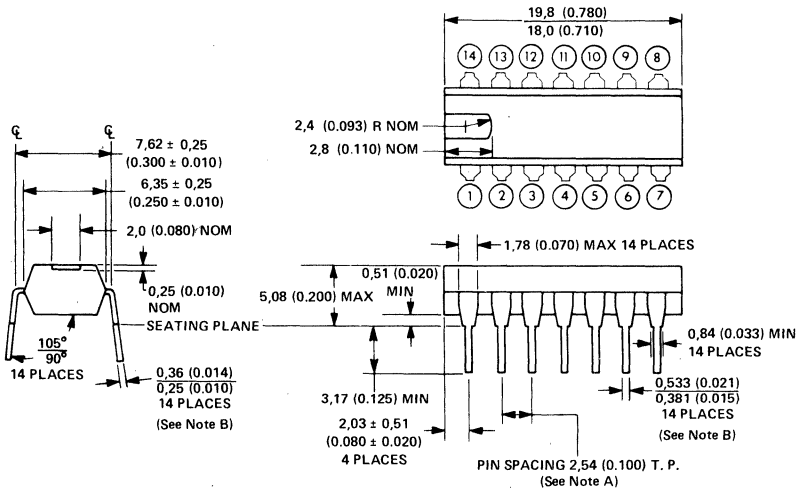
NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

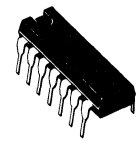
N plastic dual-in-line packages (including NT and NW)

Each of these dual-in-line packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The packages are intended for insertion in mounting-hole rows on 7,62 (0.300), 15,24 (0.600), or 22,86 (0.900) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

NOTE: For all except 24-pin packages, the letter N is used by itself since only the 24-pin package is available in more than one row-spacing. For the 24-pin package, the 7,62 (0.300) version is designated NT; the 15,24 (0.600) version is designated NW. If no second letter or row-spacing is specified, the package is assumed to have 15,24 (0.600) row-spacing.

14-PIN N PLASTIC





Falls Within JEDEC TO-116 and EIA MO-001AA Dimensions

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. For solder-dipped leads, this dimension applies from the lead tip to the standoff.

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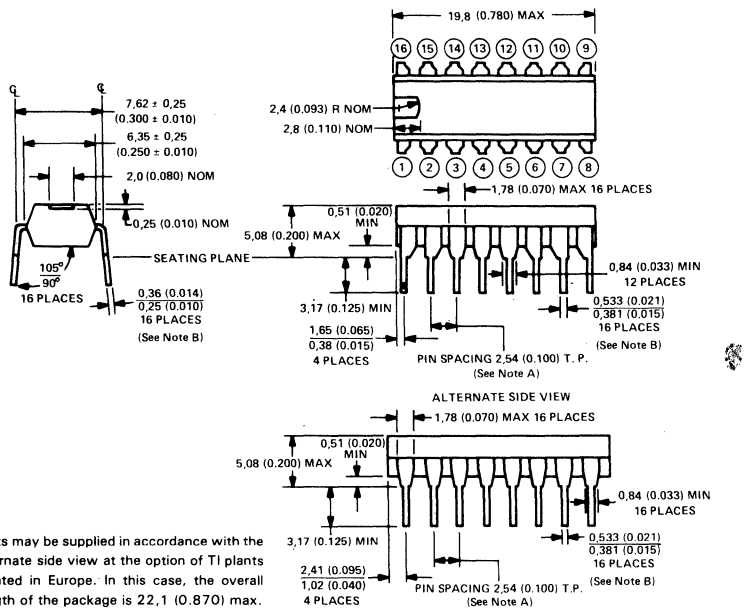
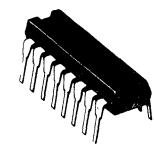
N plastic dual-in-line packages (including NT and NW)

Each of these dual-in-line packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The packages are intended for insertion in mounting-hole rows on 7,62 (0.300), 15,24 (0.600), or 22,86 (0.900) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

NOTE: For all except 24-pin packages, the letter N is used by itself since only the 24-pin package is available in more than one row-spacing. For the 24-pin package, the 7,62 (0.300) version is designated NT; the 15,24 (0.600) version is designated NW. If no second letter or row-spacing is specified, the package is assumed to have 15,24 (0.600) row-spacing.

16-PIN N PLASTIC





Parts may be supplied in accordance with the alternate side view at the option of TI plants located in Europe. In this case, the overall length of the package is 22,1 (0.870) max.

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

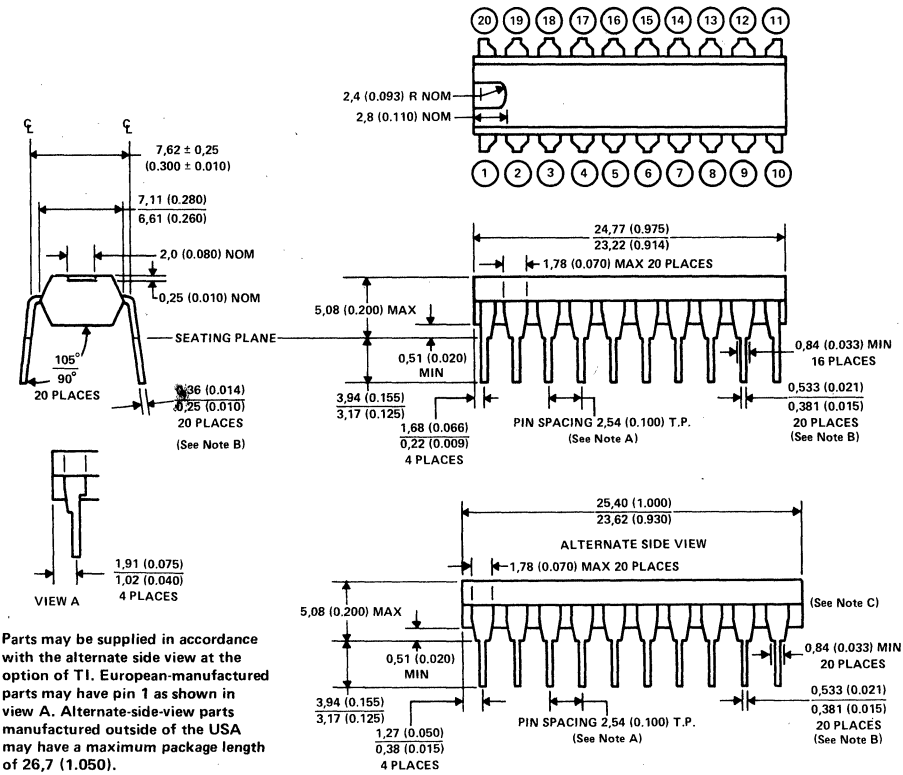
NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. For solder-dipped leads, this dimension applies from the lead tip to the standoff.

N plastic dual-in-line packages (including NT and NW)

Each of these dual-in-line packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The packages are intended for insertion in mounting-hole rows on 7,62 (0.300), 15,24 (0.600), or 22,86 (0.900) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

NOTE: For all except 24-pin packages, the letter N is used by itself since only the 24-pin package is available in more than one row-spacing. For the 24-pin package, the 7,62 (0.300) version is designated NT; the 15,24 (0.600) version is designated NW. If no second letter or row-spacing is specified, the package is assumed to have 15,24 (0.600) row-spacing.

20-PIN N PLASTIC



Parts may be supplied in accordance with the alternate side view at the option of TI. European-manufactured parts may have pin 1 as shown in view A. Alternate-side-view parts manufactured outside of the USA may have a maximum package length of 26,7 (1.050).

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. For solder-dipped leads, this dimension applies from the lead tip to the standoff.
C. Parts may be supplied with a draft angle of 7° typical at the option of TI.

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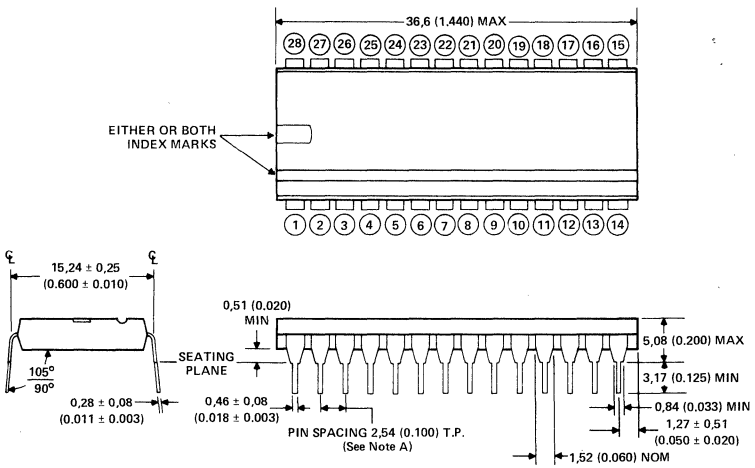
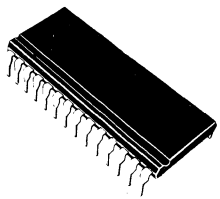
N plastic dual-in-line packages (including NT and NW)

Each of these dual-in-line packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The packages are intended for insertion in mounting-hole rows on 7,62 (0.300), 15,24 (0.600), or 22,86 (0.900) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

NOTE: For all except 24-pin packages, the letter N is used by itself since only the 24-pin package is available in more than one row-spacing. For the 24-pin package, the 7,62 (0.300) version is designated NT; the 15,24 (0.600) version is designated NW. If no second letter or row-spacing is specified, the package is assumed to have 15,24 (0.600) row-spacing.

28-PIN N PLASTIC





ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

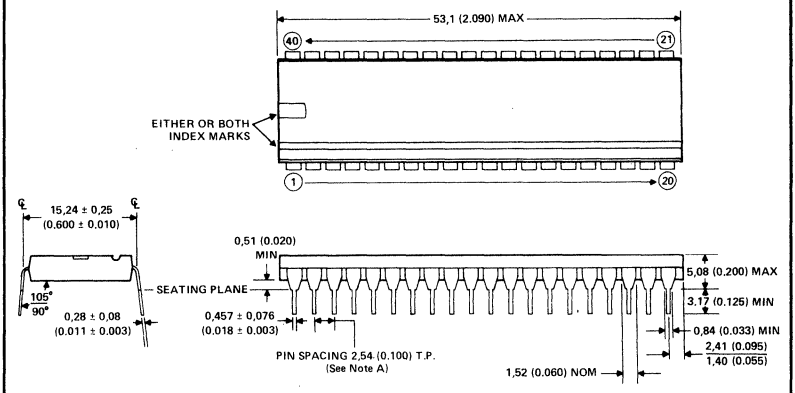
NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. For solder-dipped leads, this dimension applies from the lead tip to the standoff.

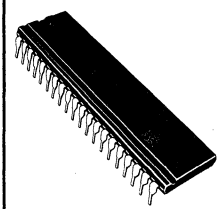
N plastic dual-in-line packages (including NT and NW)

Each of these dual-in-line packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The packages are intended for insertion in mounting-hole rows on 7,62 (0.300), 15,24 (0.600), or 22,86 (0.900) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

NOTE: For all except 24-pin packages, the letter N is used by itself since only the 24-pin package is available in more than one row-spacing. For the 24-pin package, the 7,62 (0.300) version is designated NT; the 15,24 (0.600) version is designated NW. If no second letter or row-spacing is specified, the package is assumed to have 15,24 (0.600) row-spacing.

40-PIN N PLASTIC





ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

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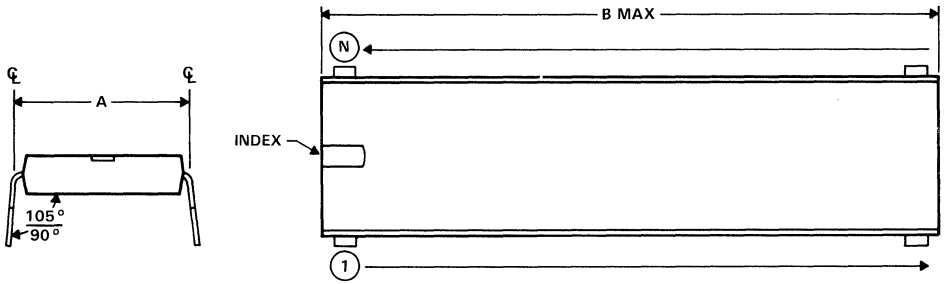
N plastic dual-in-line packages (including NT and NW)

Each of these dual-in-line packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The packages are intended for insertion in mounting-hole rows on 7,62 (0.300), 15,24 (0.600), or 22,86 (0.900) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

NOTE: For all except 24-pin packages, the letter N is used by itself since only the 24-pin package is available in more than one row-spacing. For the 24-pin package, the 7,62 (0.300) version is designated NT; the 15,24 (0.600) version is designated NW. If no second letter or row-spacing is specified, the package is assumed to have 15,24 (0.600) row-spacing.

48-PIN, 52-PIN, AND 64-PIN N PLASTIC



PIN SPACING IS 2,54 (0.100) T.P.
(See Note A)

DIM \ PINS (N)	48	52	64
A ± 0,25 (0.010)	15,24 (0.600)	15,24 (0.600)	22,86 (0.900)
B MAX	62,2 (2.45)	67,3 (2.65)	81,3 (3.20)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

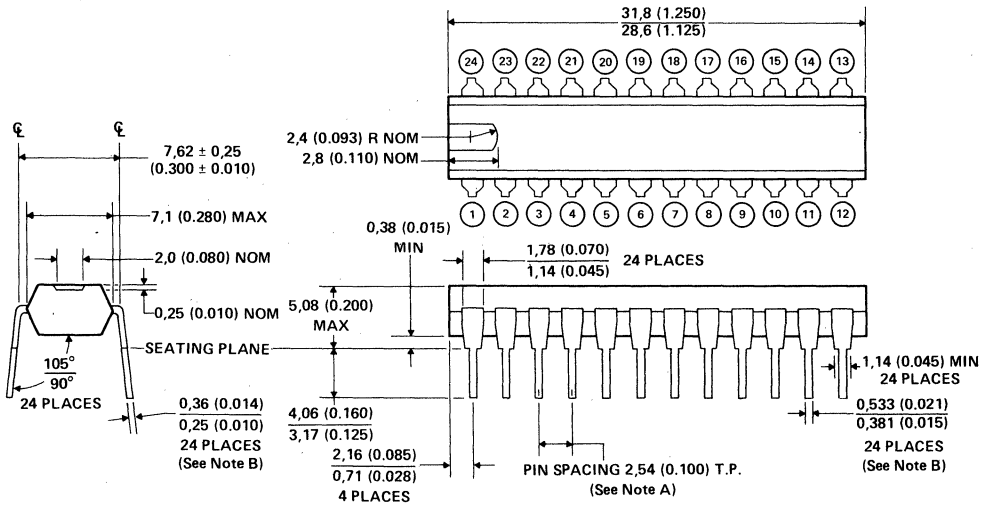
NOTE A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

N plastic dual-in-line packages (including NT and NW)

Each of these dual-in-line packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The packages are intended for insertion in mounting-hole rows on 7,62 (0.300), 15,24 (0.600), or 22,86 (0.900) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

NOTE: For all except 24-pin packages, the letter N is used by itself since only the 24-pin package is available in more than one row-spacing. For the 24-pin package, the 7,62 (0.300) version is designated NT; the 15,24 (0.600) version is designated NW. If no second letter or row-spacing is specified, the package is assumed to have 15,24 (0.600) row-spacing.

24-PIN NT PLASTIC



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. For solder-dipped leads, this dimension applies from the lead tip to the standoff.

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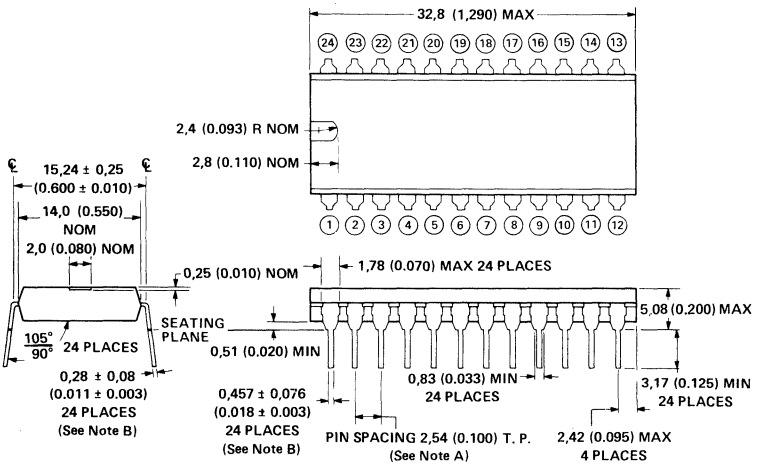
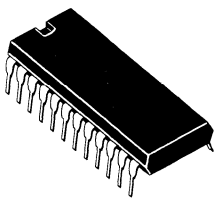
N plastic dual-in-line packages (including NT and NW)

Each of these dual-in-line packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The packages are intended for insertion in mounting-hole rows on 7,62 (0.300), 15,24 (0.600), or 22,86 (0.900) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

NOTE: For all except 24-pin packages, the letter N is used by itself since only the 24-pin package is available in more than one row-spacing. For the 24-pin package, the 7,62 (0.300) version is designated NT; the 15,24 (0.600) version is designated NW. If no second letter or row-spacing is specified, the package is assumed to have 15,24 (0.600) row-spacing.

24-PIN NW PLASTIC





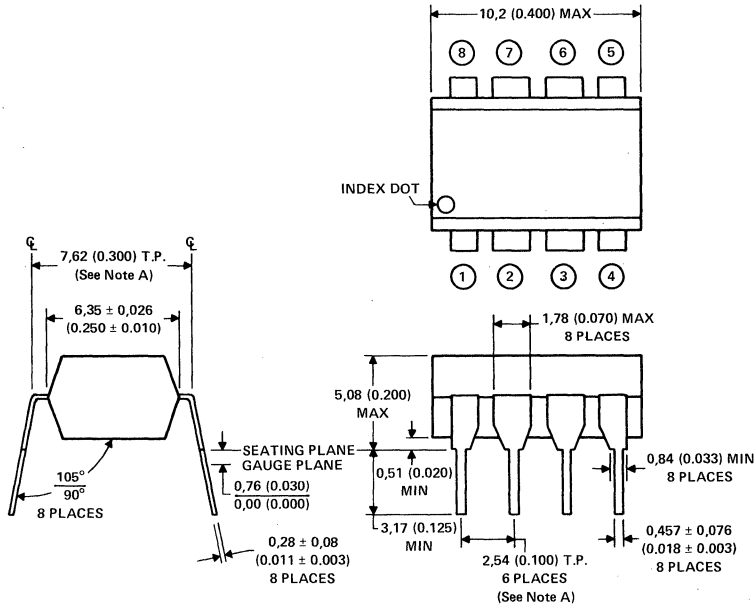
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. For solder-dipped leads, this dimension applies from the lead tip to the standoff.

P dual-in-line plastic package

This dual-in-line package consists of a circuit mounted on an 8-lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62-mm (0.300) centers (see Note A). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Solder-plated leads require no additional cleaning or processing when used in solder assembly.

8-PIN P PLASTIC



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

NOTE: A. Each pin is within 0,13 (0.0005) radius of true position (TP) at the gauge plane with maximum material condition and unit installed.

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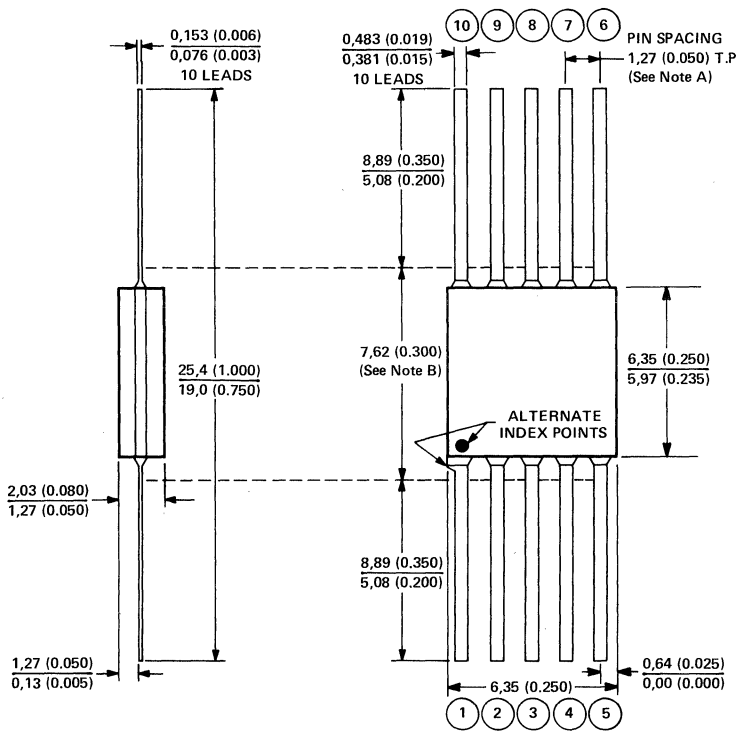
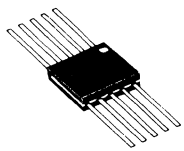
U ceramic flat package

This flat package consists of a ceramic base, ceramic cap, and lead frame. Circuit bars are alloy mounted. Hermetic sealing is accomplished with glass. Leads require no additional cleaning or processing when used in soldered assembly.

10-PIN U CERAMIC





Falls Within JEDEC MO-004AE Dimensions

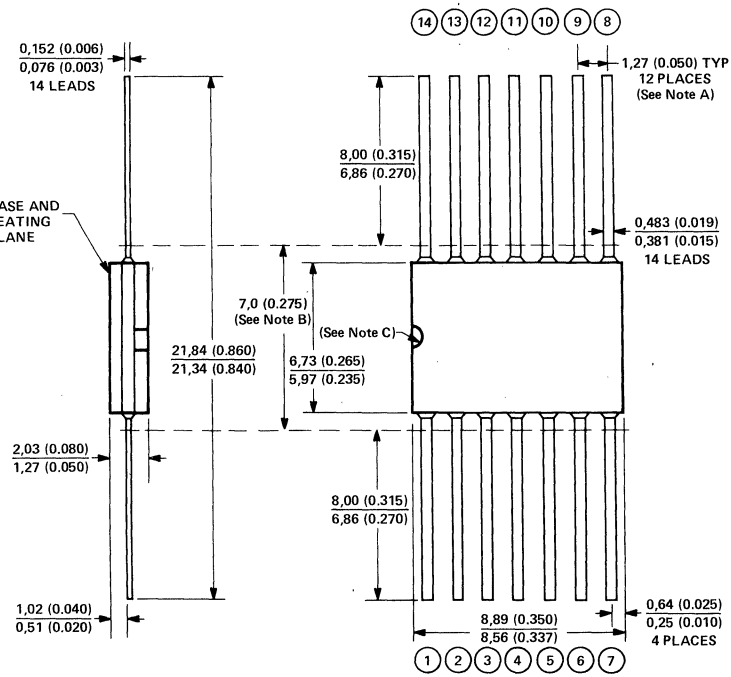
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

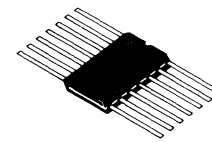
NOTES: A. Leads are within 0.005 radius of true position (T.P.) at maximum material conditions.
B. This dimension determines a zone within which all body and lead irregularities lie.

W ceramic flat packages (including WA and WC)

Each of these hermetically sealed flat packages consists of an electrically nonconductive ceramic base and cap and a lead frame. Hermetic sealing is accomplished with glass. Leads require no additional cleaning or processing when used in soldered assembly.

14-PIN W CERAMIC





Falls Within JEDEC MO-004AA Dimensions

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Leads are within 0,13 (0.005) radius of true position (T.P.) at maximum material condition.
B. This dimension determines a zone within which all body and lead irregularities lie.
C. Index point is provided on cap for terminal identification only.

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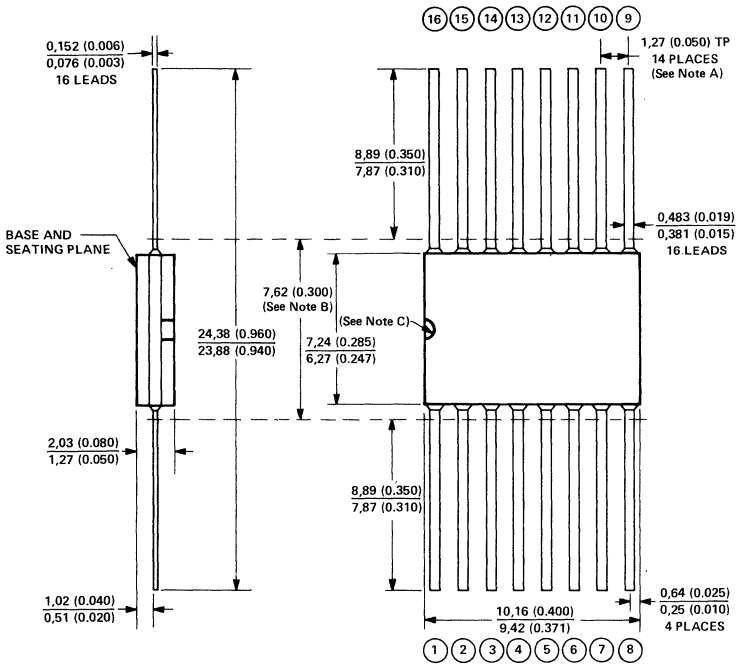
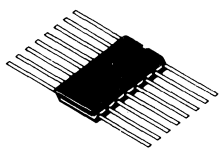
W ceramic flat packages (including WA and WC)

Each of these hermetically sealed flat packages consists of an electrically nonconductive ceramic base and cap and a lead frame. Hermetic sealing is accomplished with glass. Leads require no additional cleaning or processing when used in soldered assembly.

16-PIN W CERAMIC





Falls Within JEDEC MO-004-AA Dimensions

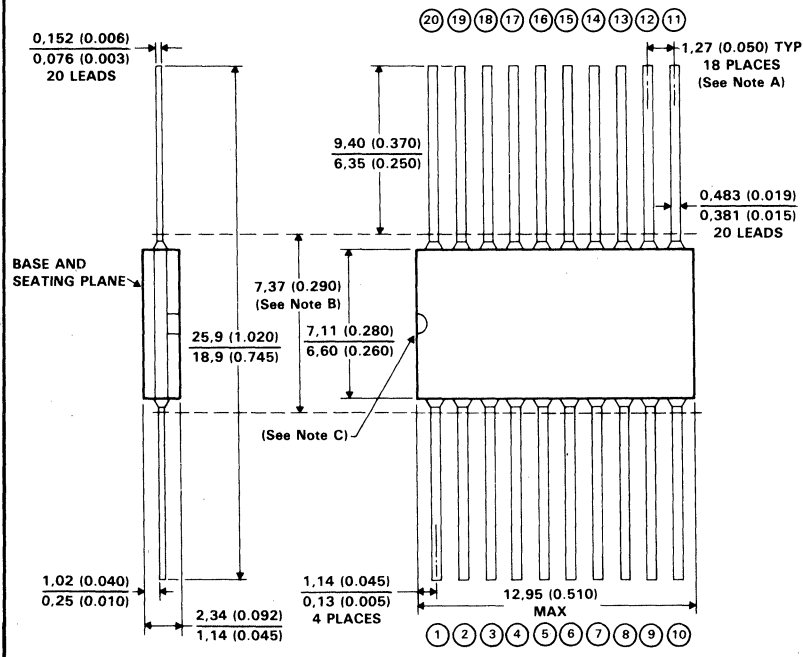
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

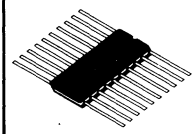
NOTES: A. Leads are within 0,13 (0.005) radius of true position (T.P.) at maximum material condition.
B. This dimension determines a zone within which all body and lead irregularities lie.
C. Index point is provided on cap for terminal identification only.

W ceramic flat packages (including WA and WC)

Each of these hermetically sealed flat packages consists of an electrically nonconductive ceramic base and cap and a lead frame. Hermetic sealing is accomplished with glass. Leads require no additional cleaning or processing when used in soldered assembly.

20-PIN W CERAMIC





ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Leads are within 0,13 (0.005) radius of true position (T.P.) at maximum material condition.
B. This dimension determines a zone within which all body and lead irregularities lie.
C. Index point is provided on cap for terminal identification only.

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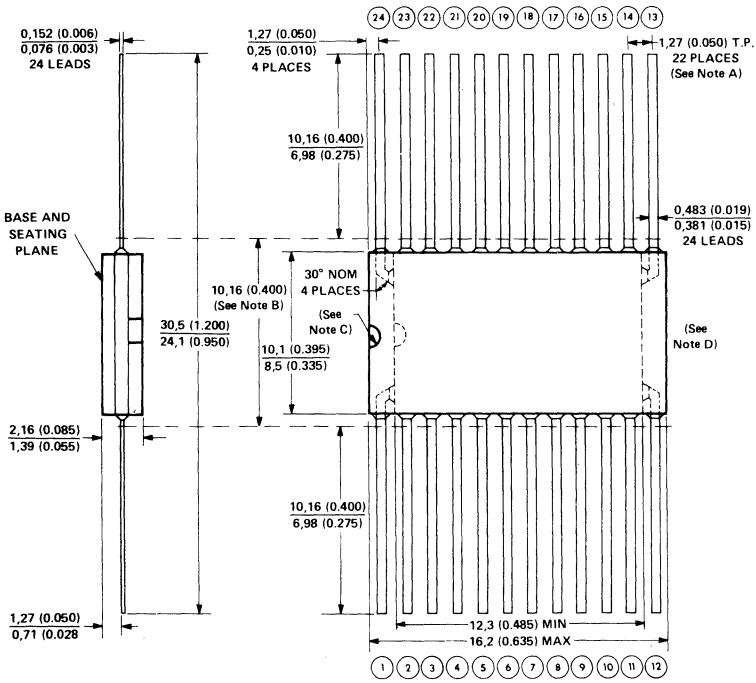
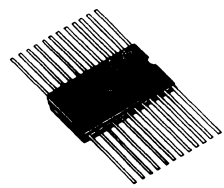
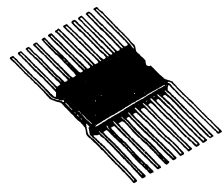
W ceramic flat packages (including WA and WC)

Each of these hermetically sealed flat packages consists of an electrically nonconductive ceramic base and cap and a lead frame. Hermetic sealing is accomplished with glass. Leads require no additional cleaning or processing when used in soldered assembly.

24-PIN W CERAMIC







Falls Within JEDEC MO-019AA Dimensions

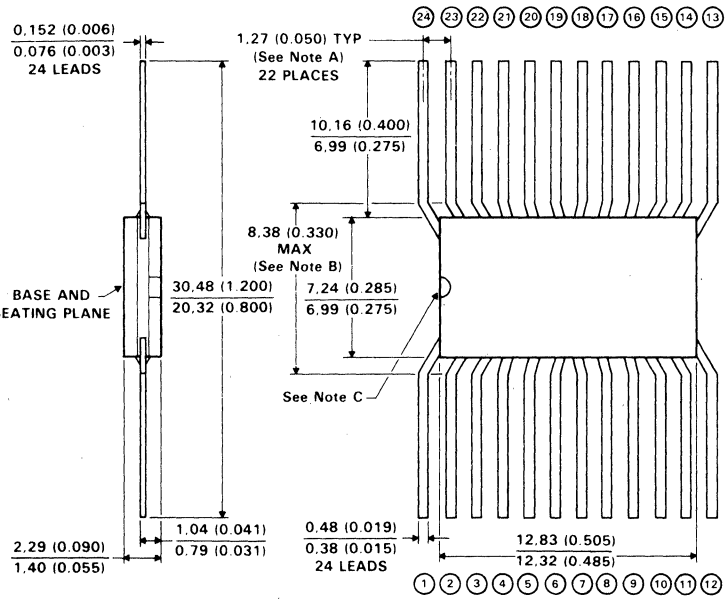
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

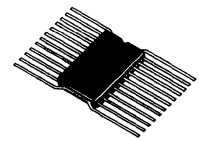
NOTES: A. Leads are within 0,13 (0.005) radius of true position (T.P.) at maximum material condition.
B. This dimension determines a zone within which all body and lead irregularities lie.
C. Index point is provided on cap for terminal identification only.
D. End configuration of 24-pin package is at the option of TI.

W ceramic flat package (including WA and WC)

Each of these hermetically sealed flat packages consists of an electrically nonconductive ceramic base and cap and a lead frame. Hermetic sealing is accomplished with glass. Leads require no additional cleaning or processing when used in soldered assembly.

24-PIN WC CERAMIC





ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Leads are within 0,13 (0.005) radius of true position (T.P.) at maximum material condition.
B. This dimension determines a zone within which all body and lead irregularities lie.
C. Index point is provided on cap for terminal identification only.

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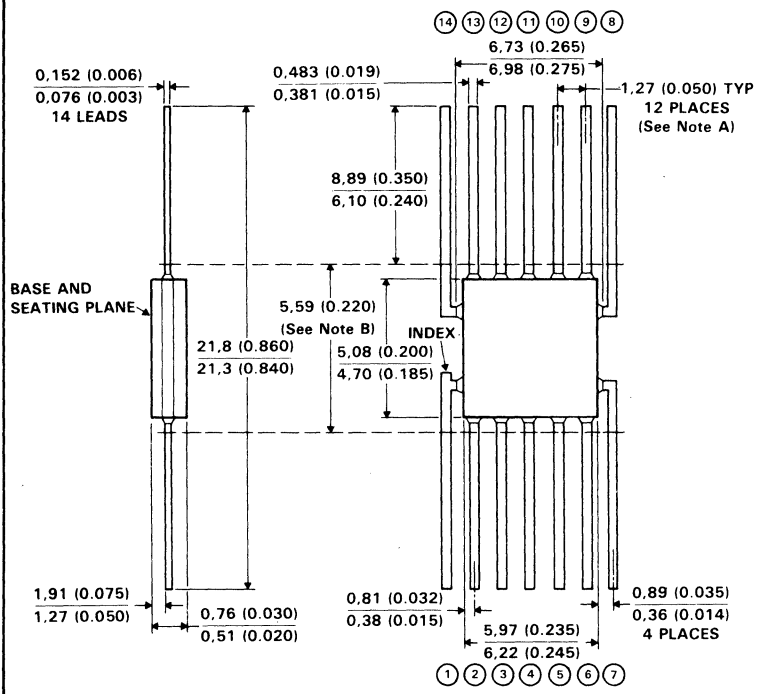
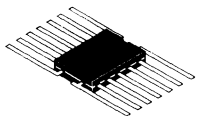
W ceramic flat package (including WA and WC)

Each of these hermetically sealed flat packages consists of an electrically nonconductive ceramic base and cap and a lead frame. Hermetic sealing is accomplished with glass. Leads require no additional cleaning or processing when used in soldered assembly.

14-PIN WA CERAMIC





ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Leads are within 0,13 (0.005) radius of true position (T.P.) at maximum material condition.
B. This dimension determines a zone within which all body and lead irregularities lie.
C. Index point is provided on cap for terminal identification only.
D. End configuration of 24-pin package is at the option of TI.

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