Data Book

Telecommunications Circuits

988/1989

TEXAS INSTRUMENTS

Telecommunications Circuits

Transmission, Switching, Subscriber, and Transient Suppressors

Data Book

1988/1989

Linear Products

General Information 1

Telecommunications Circuits 2

Designer's Information 3

Application Reports 4

Mechanical Data 5

Telecommunications Circuits Data Book

TEXAS INSTRUMENTS

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Revised: June 1988

INTRODUCTION

In just over 100 years, technical advances in the telecommunications industry have made the modern telephone system one of the true wonders of the world. We can now communicate with any part of the world in a matter of seconds. The modern telecommunication system uses digital-transmission techniques, microelectronics, network transmission, and speech-signal processing. The system is controlled by the largest network of interconnected and cooperating computers in the world. This system is on the leading edge of a telecommunication revolution that is making the home and business environment very similar. Remote banking, automated brokerage transactions, home-security monitoring from a distance, food preparation from the office, and robot control will provide the home with technical capabilities similar to those experienced by industry.

Texas Instruments (TI), because of its broad base of reliable multipurpose integrated circuits, has become a versatile and proven leader for components in the telecommunication industry. The TI capability in circuit design, process technology, and automated manufacturing of telecommunications devices has provided the switching, terminal, and transmission components required by the telecommunication industry. To integrate the analog, digital logic, and memory function on one chip, TI has developed the TCM series of telecommunication integrated circuits. TI uses the following processes and technologies:

1. Bipolar, MOS, and mixed (i.e., Bipolar and MOS on a single chip).
2. BIDFET™ process, which combines low-power logic with high-voltage circuits and requires fewer external components because of its variable packing circuitry capability.
3. Silicon-Gate CMOS technology, which allows the interconnection of analog and digital on one chip.

New suface-mount packages (8 to 84 leads) used in the TCM series of integrated circuits include standard DIPs, chip carriers, small outline plastic packages, and quadriform flat packages, which optimize board density with minimum impact on power dissipation. Telecommunication test equipment with handlers and automated assembly bonders strengthen the production capabilities to provide a lower cost to performance ratio. TI continues to improve quality and reliability of telecommunication integrated circuits by improving materials, processes, test methods, and test equipment. In addition, specifications and programs are continuously updated. Quality and performance are monitored throughout all phases of manufacturing.

The telecommunication devices in this data book support central office products, subscriber circuits, transmission circuits, modems, and the digital-signal processor requirements. The demand of the telecommunication industry for growth products has made it practical to develop an entire μ-Law Codec with filter on a single chip. This chip will replace 50 general-purpose integrated circuits.

The rapid growth of the semiconductor content in the telephone system has dramatically altered the protection required against such hazards as lightning and accidental connection to ac lines. Because of faster responses, well defined voltage levels, and reliable operation, previous protection methods are no longer adequate. TI has developed a transient suppressor (TISP) series of devices that provide shunt protection against transient voltages (static, lightning), and protection against damage caused by induction or accidental connection to an ac source.

To achieve a high level of system integration and performance for digital signal processing applications, TI offers the analog interface circuits combining high-resolution A/D and D/A converters, programmable filters, digital control and timing circuits, and programmable input amplifiers and multiplexers.

The alphanumeric index in this data book provides a means of quickly locating the device type. The selection guide includes a description of each device and contains information on key parameters and packaging. The glossary describes the symbols, abbreviations, terms, and definitions used in this data book. The detailed data sheets, quality and reliability assurance and the application reports complete the contents of the data book.

While this volume offers design and specification data only for Telecommunications components, complete technical data for Analog Interface Circuits (AIC), Digital Signal Processing (TMS320 series), and all other TI semiconductor products is available from your nearest TI Field Sales Office, local authorized TI distributor, or by writing directly to:

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We sincerely feel that you will discover the new *1988 Telecommunications Circuits Data Book* to be a significant addition to your collection of technical literature.

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General Information 1

Telecommunications Circuits 2

Designer's Information 3

Application Reports 4

Mechanical Data 5

Contents

	Page
Alphanumeric Index	1-3
Selection Guide	1-5
Glossary	1-11

DEVICE	PAGE	DEVICE	PAGE
DS3680	2-3	TCM4204A	2-141
TCM1501B	2-13	TCM4205A	2-141
TCM1506B	2-13	TCM4207A	2-141
TCM1512B	2-13	TCM5087	2-161
TCM1520A	2-7	TCM5089	2-167
TCM1531	2-13	TCM5092	2-173
TCM1532	2-13	TCM5094	2-179
TCM1536	2-13	TCM78808	2-185
TCM1539	2-13	TIL181	2-205
TCM2203	2-21	TISP1082	2-209
TCM2222	2-29	TISP2180	2-215
TCM2909	2-37	TISP2290	2-215
TCM2910A	2-37	TISP3180	2-219
TCM2912C	2-57	TISP3290	2-219
TCM2913	2-71	TISP4180	2-223
TCM2914	2-71	TISP4290	2-223
TCM2916	2-71	TISP7180	2-227
TCM2917	2-71	TISP7290	2-227
TCM29C13/TCM129C13	2-93	TISP8180	2-231
TCM29C14/TCM129C14	2-93	TISP8290	2-231
TCM29C16/TCM129C16	2-93	TISP9180	2-235
TCM29C17/TCM129C17	2-93	TISP9290	2-235
TCM29C18/TCM129C18	2-115	TLC32040C	2-237
TCM29C19/TCM129C19	2-115	TLC32040I	2-237
TCM3105JE	2-129	TLC32041C	2-237
TCM3105JL	2-129	TLC32041I	2-237

TELECOMMUNICATIONS

telecommunications circuits

DESCRIPTION	FUNCTION	TECHNOLOGY	SUPPLY VOLTAGE	PRODUCT FEATURES	TYPE	PKG	PAGE
AMI/HDB3 Transmission	Encoder/Decoder	NMOS	5 V	AMI or HDB3 encoding Received signal diagnostics Zero to 3 MHz bit rate	TCM2222	16-Pin J	2-29
	Equipment Line Interface	Bipolar	5 V	Serial bipolar data rates up to 3 MHz Low-Q clock extraction Two ALBO taps with 42 dB range Phase adjust for recovered clock Direct interface with TCM2222	TCM2203	28-Pin J	2-21
PCM Interface	CODEC	NMOS	12 V, ±5 V	Provides μ-Law companding Compatible with CCITT recommendations G.711 and G.712 Optional programmable time-slot selection	TCM2909	22-Pin J,N	2-37
				Compatible with CCITT recommendations G.711 and G.712 μ-255-Law encoding and 8th-bit signaling Optional programmable time-slot selection	TCM2910A	24-Pin J,N	2-37

telecommunications circuits (continued)

DESCRIPTION	FUNCTION	TECHNOLOGY	SUPPLY VOLTAGE	PRODUCT FEATURES	TYPE	PKG	PAGE
PCM Interface	Line Filter	NMOS	±5 V	High-pass transmit filter for rejection of all low-frequency noise 6th-order low-pass transmit filter CCITT G.172 compatible AT&T D3/D4 compatible Three-state PWRO+ and PWRO− outputs	TCM2912C	20-Pin J	2-57
	COMBO			Synchronous, μ-Law, A-Law coding Variable data rate Fixed data rate 1.536 MHz, 1.544 MHz, 2.048 MHz	TCM2913	20-Pin J	2-71
				Synchronous/ asynchronous μ-Law, A-Law coding, 8th-bit signaling Variable data rate Fixed data rate 1.536 MHz, 1.544 MHz, 2.048 MHz	TCM2914	24-Pin J, 28-Pin FN	2-71
				Synchronous, μ-Law, variable data rate Fixed data rate 2.048 MHz MHz	TCM2916	16-Pin J	2-71
				Synchronous, A-law, Variable data rate Fixed data rate 2.048 MHz	TCM2917	16-Pin J	2-71

telecommunications circuits (continued)

DESCRIPTION	FUNCTION	TECHNOLOGY	SUPPLY VOLTAGE	PRODUCT FEATURES	TYPE	PKG	PAGE
PCM Interface	COMBO	CMOS	±5 V	Synchronous, μ-Law, A-Law coding Variable data rate Fixed data rate 1.536 MHz, 1.544 MHz, 2.048 MHz	TCM29C13	20-Pin J,DW, DY	2-93
				Synchronous/ asynchronous μ-Law, A-Law coding, 8th-bit signaling Variable data rate Fixed data rate 1.536 MHz, 1.544 MHz, 2.048 MHz	TCM29C14	24-Pin J,DW, 28-Pin FN	2-93
				Synchronous, μ-Law, Variable data rate Fixed data rate 2.048 MHz	TCM29C16	16-Pin J,N	2-93
				Synchronous, A-Law, Variable data rate Fixed data rate 2.048 MHz	TCM29C17	16-Pin J,N	2-93
				Low-cost speech band DSP interface μ-Law encoding	TCM29C18 TCM29C19	16-Pin N	2-115
Modem	Bell 202/CCITT V.23	CMOS	5 V	Asynchronous Half-duplex operation up to 1200 baud Full-duplex operation 1200/150 baud, reversible	TCM3105	16-Pin J	2-129

telecommunications circuits (continued)

DESCRIPTION	FUNCTION	TECHNOLOGY	SUPPLY VOLTAGE	PRODUCT FEATURES	TYPE	PKG	PAGE
Ringers	Telephone Tone Ringer Drivers	BIDFET	40–150 Vac	Output Center Frequency (Hz): 2000	TCM1531	8-Pin P	2-13
				Output Center Frequency (Hz): 2000	TCM1501B	8-Pin P	2-13
				Output Center Frequency (Hz): 1250	TCM1532	8-Pin P	2-13
				Output Center Frequency (Hz): 1250	TCM1512B	8-Pin P	2-13
				Output Center Frequency (Hz): 500	TCM1536	8-Pin P	2-13
				Output Center Frequency (Hz): 500	TCM1506B	8-Pin P	2-13
				Output Center Frequency (Hz): 2000	TCM1539	8-Pin P	2-13
Ring Detector	TTL/MOS Output	BIDFET	40–150 Vac	TTL/MOS output, transient protection	TCM1520A	8-Pin P	2-7
Tone Encoder	DTMF Standard	CMOS	3.5–10 V	SPST/DPST keyboard or electronic input Low impedance tone output	TCM5087	16-Pin N	2-161
				Transmitter switch and mute output DPST keyboard or electronic input Keyboard active output	TCM5089	16-Pin N	2-167
					TCM5092		2-173
					TCM5094		2-179
Suppressor	Transient Voltage Suppressor	Bipolar	58 V	Breakover voltage to common: 82 V max	TISP1082	TO220	2-209
			145 V	Breakover voltage to common: 180 V max	TISP2180	TO220	2-215
			200 V	Breakover voltage to common: 290 V max	TILSP2290	TO220	2-215
			145 V	Breakover voltage to common: 180 V max	TISP3180	TO220	2-219
			200 V	Breakover voltage to common: 290 V max	TISP3290	TO220	2-219

telecommunications circuits (concluded)

DESCRIPTION	FUNCTION	TECHNOLOGY	SUPPLY VOLTAGE	PRODUCT FEATURES	TYPE	PKG	PAGE
Suppressor	Transient Voltage Suppressor	Bipolar	145 V	Breakover voltage to common: 180 v max	TISP4180	TO220	2-223
			200 V	Breakover voltage to common: 290 V max	TISP4290	TO220	2-223
			145 V	Breakover voltage to common: 180 V max	TISP7180	TO220	2-227
			200 V	Breakover voltage to common: 290 V max	TISP7290	TO220	2-227
			145 V	Breakover voltage to common: 180 V max	TISP8180	TO220	2-231
			200 V	Breakover voltage to common: 290 V max	TISP8290	TO220	2-231
			145 V	Breakover voltage to common: 180 V max	TISP9180	TO220	2-235
			200 V	Breakover voltage to common: 290 V max	TISP9290	TO220	2-235
Optocoupler	TTL-Compatible	Bipolar	12 V	Peak high-voltage isolation: 3.54 kV	TIL181	6-Pin CP-7	2-205
Subscriber Line Control Circuits	TTL-Compatible	CMOS	±5 V	Three selectable balance networks	TCM4204A	24-Pin J	2-141
				Three selectable balance networks Three auxiliary relay outputs Ground-start operation	TCM4205A	28-Pin J	2-141
				Flux-canceling option Two selectable balance networks	TCM4207A	24-Pin J	2-141
	Quad Telephone Relay Driver	Bipolar	5 V, −60 V	50-mA output current capability	DS3680	14-Pin D,J,N	2-3
Converter/ Controller	Octal Receiver/ Transmitter	NMOS	5 V	Programmable baud rates: 50 to 19,200	TCM78808	68-Pin FN, HA,HB	2-185

analog interface for digital signal processors

FUNCTION	TRANSFER CHARACTERISTIC	DYNAMIC RANGE	RESOLUTION	SAMPLING RATE	ON-BOARD FILTERS	TYPE	PAGE
High-Performance Combo	Linear	14 Bits	14 Bits	19.2 kHz (Programmable)	Yes (Programmable)	TLC32040† TLC32041†	2-239

†TheTLC32040 and TLC32041 have two differential inputs for the 14 bit A/D and a serial port input for the 14 bit D/A. The A/D conversion accuracy for this device is measured in terms of signal-to-quantization distortion and also in LSB over certain converter ranges. Please refer to the data sheet.

ADC

Analog-to-digital converter. A converter that uniquely represents all analog input values within a specified total input range by a limited number of digital output codes, each of which exclusively represents a fractional part of the total analog input range.

Note: This quantization procedure introduces inherent errors of one-half LSB (least significant bit) in the representation since, within this fractional range, only one analog value can be represented free of error by a single digital output code.

AMI

Alternate Mark Inversion. A pseudoternary signal converting binary digits, in which successive "marks" are normally of alternate positive and negative polarity but equal in amplitude and in which "space" is of zero amplitude.

Address

The number dialed by a calling party that identifies the party called. Also a location or destination in a computer program.

ALBO

Automatic Line Build Out. In digital transmission systems, a circuit that monitors the amplitude of the received digital signal and, based on this information, automatically adjusts its gain and frequency response to correct for the effects of the transmission line.

Aliasing

The occurrence of spurious frequencies in the output of a pulse-coded modulation (PCM) system or ADC that were not present in the input due to foldover of higher frequencies.

Bell Tapping

The undesired activation of the ringer circuit of a telephone caused by dial pulses from a parallel telephone. Also known as tinkling.

Bias (Asymmetrical) Distortion

Distortion affecting a binary modulation scheme whereby the actual mark or space has a longer or shorter duration than the corresponding theoretical duration.

Bit Rate (BPS) Versus Baud Rate

For modems using voice grade telephone lines, the bit rate equals the data rate. The baud rate is the actual number of times per second that the transmitted carrier is modulated or changes state.

BORSCHT

An acronym for the function that must be performed in the central office when digital voice transmission occurs; **B**attery, **O**vervoltage, **R**inging, **S**upervision, **C**oding, **H**ybrid, and **T**est.

Byte

A group of bits treated as a unit. Often equivalent to one alphabetic or numeric character.

CCITT

International Telegraph and Telephone Consultative Committee. An international forum for establishing communication system standards.

Central Office (CO)

The switching equipment that provides local-exchange telephone service for a given geographical area and is designated by the first three digits of the telephone number.

Channel

An electronic communication path. In telecommunications, it is usually a voice bandwidth of 4,000 Hz.

Circuit

An interconnected group of electronic devices or, in telecommunications, the path connecting two or more communications terminals.

C-Message Weighting

A noise weighting used to measure noise on a line that would be terminated by a 500-type telephone set or similar instrument. The resulting noise reading is in dBrnC.

Codec

An assembly comprising an encoder and a decoder in the same unit. A device that produces a coded output from an analog input, and vice versa.

Combo

A single-chip pulse-code-modulated encoder, decoder (PCM codec) and PCM line filter.

Common Battery

A system supplying direct current for the telephone set from the central office.

Compander

A contraction for a compressor-expander; a circuit that compresses the dynamic range of an input signal and expands it back to almost the original form at the output.

Crossbar Switch

An electromechanical switching machine using a relay mechanism with horizontal and vertical input lines (usually 10 to 20). Uses a contact matrix to connect any vertical to any horizontal.

Crosspoint

The element that actually performs the switching function in a telephone system. It may be mechanical using metal contacts or solid state using integrated circuits.

Crosstalk

Undesired voice-band energy transfer from one circuit to another (usually adjacent).

Cutoff Frequency

The frequency above or below which signals are attenuated below a specified value by a circuit or network.

DAC

Digital-to-analog converter. A converter that represents a limited number of different digital input codes by a corresponding number of discrete analog output values.
Note: Examples of input code formats are straight binary, two's complement, and binary-coded decimal.

Data

In telephone systems, any information other than human speech.

Data Set

Telecommunications term for a modem.

Decibel (dB)

A unit of measure of relative power, 10 log (P1/P2), or voltage, 20 log (V1/V2), in terms of the ratio of two values.

dBm

Decibels referenced to one milliwatt; used in communication work as a measure of absolute power values. Zero dBm equals one milliwatt.

dBm0

Noise power referenced to or measured at a zero transmission level point (0TLP).

dBm0p

Noise power in dBm0, measured by a psophometer or noise measuring set having psophometric weighting.

dBrn

Decibels above reference noise. Rated noise power in dB referenced to one picowatt. Zero dBrn equals −90 dBm.

dBrnC

Weighted noise power in dBrn, measured by a noise measuring set with C-message weighting.

dBrnC0

Noise power in dBrnC referenced to or measured at a zero transmission level point (0TLP).

dBW

Decibels referenced to one watt.

Decoder

Any device that modifies transmitted information to a form that can be understood by the receiver.

Demultiplexer

A circuit that distributes an input signal to a selected output line (with more than one output line available).

Dial Pulsing

Transmission of address information by breaking a dc path; the number of breaks corresponds to the decimal digit dialed.

DTMF

Dual-Tone-Multi-Frequency. Use of two simultaneous voice-band tones for dialing.

EIA

Electronic Industries Association. (2001 Eye Street, N.W., Washington, D.C. 20006)

Electromagnetic Spectrum

The total range of wavelengths or frequencies of electromagnetic radiation, extending from the longest radio waves to the shortest known cosmic rays.

Encoder

Any device that modifies information into the desired pattern or form for a specific method of transmission.

ESS

Electronic Switching System. A telephone switching machine using electronics, often combined with electromechanical crosspoints, and usually with a stored-program computer as the control element.

Exchange Area

The territory within which telephone service is provided for a basic charge. Also called the local calling area.

Equalization

The reduction of frequency distortion and/or phase distortion of a circuit by the introduction of networks to compensate for the difference in attenuation, time delay, or both, at the various frequencies in the transmission band.

FCC

Federal Communications Commission. A government agency that regulates and monitors the domestic use of the electromagnetic spectrum for communications.

FCC Part 68

A government document describing the types of equipment that must be registered and the electrical and mechanical standards to be met when connecting equipment to the public telephone network.

Fiber Optics

The process of transmitting infrared and visible light frequencies through a low-loss glass fiber with a transmitting laser or LED.

FSK

Frequency-Shift Keying. A method of transmitting digital information that utilizes two tones; one representing a high level, the other a low level.

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Full Duplex

Simultaneous communication in both directions between two points.

Ground Start

A method of signaling between two machines in which one machine grounds one side of the line and the other machine detects the presence of the ground.

HDB3

High-Density Bipolar Three-line code. See AMI.

Half-Duplex

A circuit that can carry information in both directions but not simultaneously.

Hybrid

In telecommunications, a circuit that divides a signal transmission channel into two channels (i.e., one for each direction) or, conversely, combines two channels into one.

Instruction Code

Digital information that represents an instruction to be performed by a computer.

ISDN

Integrated Services Digital Network. A communication network capable of carrying digitized voice and data multiplexed onto the public network.

Lineside

Refers to the portion of the central office that connects to the local loop.

Local Loop

The voice-band channel connecting the subscriber to the central office.

Longitudinal Balance

A measure of symmetry impedance of a balanced network. Improper longitudinal balance results in poor common-mode rejection.

Loop Current

Flow of dc in the local loop. Indicates that a telephone is in use.

Loss

Attenuation of a signal due to any cause.

Mark

One of the two possible states of a binary information element. The closed circuit and idle state in a teleprinter circuit. See Space.

MTS

Message Telephone Service. The official name for long distance or toll service.

Modem

A device to convert digital data into an analog signal and vice versa so that two electronic devices (e.g., a computer and a data terminal) may communicate over the telephone system. The word modem is a contraction of modulator/demodulator.

Multiplexer

A device for accomplishing simultaneous transmission of two or more signals over a common transmission medium.

Off-Hook

The condition that indicates the active state of a telephone circuit. The opposite condition is On-Hook.

PABX

Private Automated Branch Exchange. Small local automatic telephone office serving extensions in a business complex providing access to the public network.

Parallel Data

The transfer of data simultaneously over two or more wires or transmission links.

Parity

A bit that indicates whether the number of "ones" in a bit string is odd or even.

PBX

Private Branch Exchange. A telephone exchange serving an individual organization and having connection to a public telephone exchange.

Period

The time between successive similar points of a repetitive signal.

Phase

The time or angle that a signal is delayed with respect to some reference position.

POTS

Plain Old Telephone Service. An acronym used by the telephone industry for conventional telephone service.

PSK

Phase Shift-Keyed modulation. A method of placing data of a carrier signal by modifying the phase of the carrier wave.

Psophometric Weighting

A noise weighting recommended by the CCITT for use in a noise measuring set or psophometer.

PCM

Pulse-Coded Modulation. That form of modulation in which the modulating signal is sampled and then quantized and coded, so that each element of information is represented in digital form by a serial bit stream.

Quantizing Noise

An undesirable random signal caused by the error of approximation in a quantizing process. It may be regarded as noise arising in the pulse-code modulation process due to the code-derived facsimile not exactly matching the waveform of the original message.

Register

A storage element for one or more bits of digital information.

Ring

The alerting signal to the subscriber or terminal equipment. Also, the name for one conductor of the wire pair comprising the local loop, designated by R.

Ring Trip

During ring signaling, the detection of the off-hook condition and removal of the ring signal from the line by the switch.

Serial Data

The transfer of data over a single wire in a sequential pattern.

Sidetone

That portion of the speaker's voice that is fed back to his receiver.

Simplex

A circuit that can carry information in only one direction (e.g., broadcasting.)

SLCC

Subscriber Line Control Circuits. A family of CMOS LSI circuits which provide the hybrid, supervisor and controlling functions in a single package.

SLIC

Subscriber Line Interface Circuit. In digital transmission of voice, the circuit that performs some or all of the interface functions at the central office. See BORSCHT.

Space

One of the two possible states of a binary information element. The open-circuit or no-current state of a teleprinter.

State

A condition of an electronic device, especially a computer, that is maintained until an internal or external occurrence causes change.

S by S

Step-by-Step system. An electromechanical telephone switching system in which the switches are controlled directly by digits dialed by the calling party.

Subscriber Loop

See Local Loop.

Supervision

The function of monitoring and controlling the status of a call.

TDM

Time Division Multiplexing. A communication system technique that separates information from channel inputs and places them on a carrier in specific positions of time.

Tip

One conductor of the wire pair composing the local loop and designated by T. Usually the more positive of the two conductors.

Toll Center

A major telephone distribution center that distributes calls from one major metropolitan area to another.

Transhybrid Loss

In a telphone hybrid, the measure of the isolation between the receive and transmit ports. It is also a measure of the balance between the two matched windings of a hybrid transformer.

Transmission Link

The path over which information flows from sender to receiver.

Trunk

A transmission channel connecting two switching machines.

Trunkside

That portion of the central office that connects to trunks going to other switching offices.

Voice-Grade Line

A local loop, or trunk, having a bandpass of approximately 300 to 3,000 Hz.

Wideband Circuit

A transmission facility having a bandwidth greater than that of a voice-grade line.

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General Information 1

Telecommunications Circuits 2

Designer's Information 3

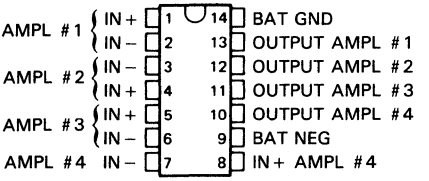
Application Reports 4

Mechanical Data 5

D2758, MARCH 1986

- Designed for −52-V Battery Operation
- 50-mA Output Current Capability
- Input Compatible with TTL and CMOS
- High Common-Mode Input Voltage Range
- Very Low Input Current
- Fail-Safe Disconnect Feature
- Built-In Output Clamp Diode
- Direct Replacement for National DS3680 and Fairchild μA3680

D, J OR N PACKAGE
(TOP VIEW)

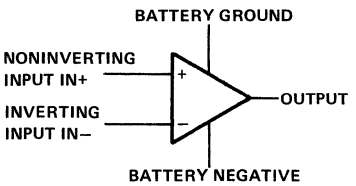


description

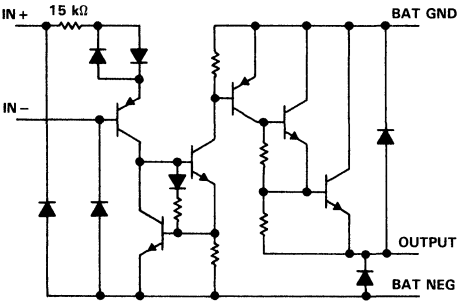
The DS3680 telephone relay driver is a monolithic integrated circuit designed to interface −48-volt relay systems to TTL or other systems in telephone applications. It is capable of sourcing up to 50 milliamperes from standard −52-volt battery power. To reduce the effects of noise and IR drop between logic ground and battery ground, these drivers are designed to operate with a common-mode input range of ±20 volts referenced to battery ground. The common-mode input voltages for the four drivers can be different, so a wide range of input elements can be accommodated. The high-impedance inputs are compatible with positive TTL and CMOS levels or negative logic levels. A clamp network is included in the driver outputs to limit high-voltage transients generated by the relay coil during switching. The complementary inputs ensure that the driver output will be "off" as a fail-safe condition when either output is open.

The DS3680 is characterized for operation from −25°C to 85°C.

symbol (each driver)



schematic diagram (each driver)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range at BAT NEG, V_{B-} . . . . . −70 V to 0.5 V
Input voltage with respect to BAT GND . . . . . −70 V to 20 V
Input voltage with respect to BAT NEG . . . . . −0.5 V to 70 V
Differential input voltage, V_{ID} (see Note 2) . . . . . ±20 V
Output current: resistive load . . . . . −100 mA
inductive load . . . . . −50 mA
Inductive output load . . . . . 5 H
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3):
D package . . . . . 900 mW
J package . . . . . 1025 mW
N package . . . . . 1650 mW
Operating free-air temperature range . . . . . −25°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C
N package . . . . . 260°C

NOTES: 1. All voltages are with respect to the BAT GND terminal, unless otherwise specified.
2. Differential input voltages are at the noninverting input terminal IN+ with respect to the inverting input terminal IN−.
3. For operation above 25°C free-air temperature, derate linearly at the rate of 7.2 mW/°C for the D package, 8.2 mW/°C for the J package, and 13.2 mW/°C for the N package.

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{B-}	−10	−60	V
Input voltage, either input	−20†	20	V
High-level differential input voltage, V_{IDH}	2	20	V
Low-level differential input voltage, V_{IDL}	−20†	0.8	V
Operating free-air temperature, T_A	−25	85	°C

†The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for input voltage levels.

electrical characteristics over recommended operating free-air temperature range, V_{B-} = −52 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
I_{IH}	High-level input current (into IN+)	V_{ID} = 2 V			40	100	μA
		V_{ID} = 7 V			375	1000	
I_{IL}	Low-level input current (into IN+)	V_{ID} = 0.4 V			0.01	5	μA
		V_{ID} = −7 V			−1	−100	
$V_{O(on)}$	On-state output voltage	I_O = 50 mA,	V_{ID} = 2 V		−1.6	−2.1	V
$I_{O(off)}$	Off-state output current	$V_O = V_{B-}$	V_{ID} = 0.8 V		−2	−100	μA
			Inputs open		−2	−100	
I_R	Clamp diode reverse current	V_O = 0			2	100	μA
V_{OK}	Output clamp voltage	I_O = 50 mA			0.9	1.2	V
		I_O = −50 mA,	V_{B-} = 0		−0.9	−1.2	
$I_{B(on)}$	On-state battery current	All drivers on			−2	−4.4	mA
$I_{B(off)}$	Off-state battery current	All drivers off			−1	−100	μA

‡All typical values are at T_A = 25°C.

switching characteristics V_{B-} = −52 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{on}	Turn-on time	V_{ID} = 3-V pulse, R_L = 1 kΩ,		1	10	μs
t_{off}	Turn-off time	L = 1 H, See Figure 1		1	10	μs

PARAMETER MEASUREMENT INFORMATION

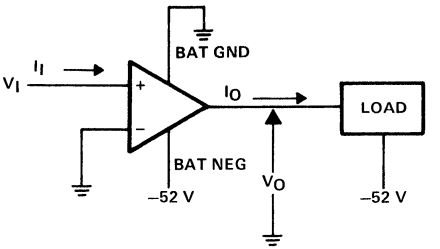
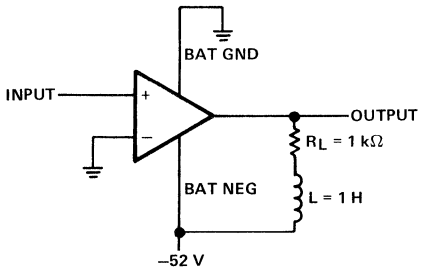
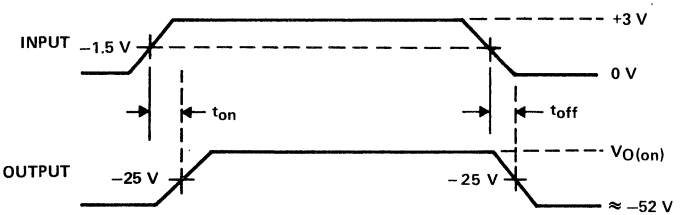


FIGURE 1. GENERALIZED TEST CIRCUIT, EACH DRIVER



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 2. SWITCHING CHARACTERISTICS, EACH DRIVER

TYPICAL APPLICATION DATA

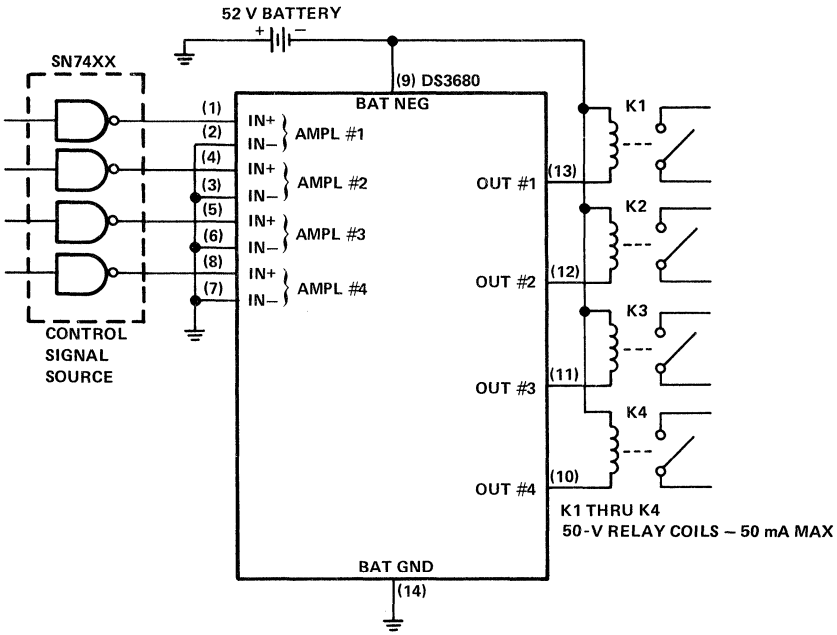
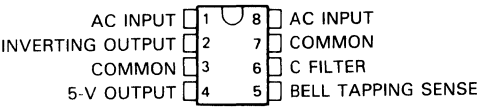


FIGURE 3. RELAY DRIVER

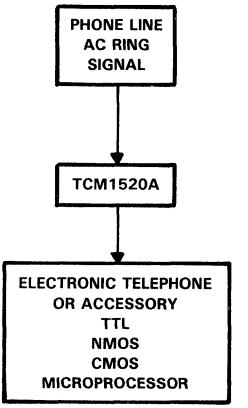
D2860, OCTOBER 1984—REVISED JANUARY 1988

- **On-Chip 150-V Bridge Diode Configuration**
- **Reliable BIDFET† Technology**
- **High Standby Impedance . . . 1 MΩ Typ**
- **Efficient High-Voltage Operation**
- **Output Compatible with TTL, NMOS, and CMOS**
- **Built-In 5-V Series Regulator**
- **Built-In Lightning and Transient Protection**

P PACKAGE
(TOP VIEW)



TCM1520A APPLICATION



description

The TCM1520A is a monolithic ring detection integrated circuit designed for use in isolated or nonisolated telephone applications. The device uses a modified form of the Texas Instruments BIDFET† technology to combine low-voltage CMOS and high-voltage bipolar input/output circuitry. It features efficient high-voltage (40 V to 150 V) operation with a typical current drain of 1 mA.

During standby, the input impedance is approximately 1 MΩ or greater, which will prevent any interference with parallel "off-hook" telephones transmitting DTMF or voice frequencies. The device achieves such a high input impedance with an on-chip series zener diode that does not conduct until the voltage across Pins 1 and 8 exceeds 8 V. When the voltage across Pins 1 and 8 exceeds 18 V, the internal switch is closed, which bypasses the 6.8-V zener diode and series resistor. This allows more efficient power transfer to the load when the device is in the operating mode. In the operating mode, the impedance of the device varies from 30 kΩ to 7 kΩ over the ring signal of 40 V at 16 Hz to 150 V at 68 Hz and is reasonably independent of the output load.

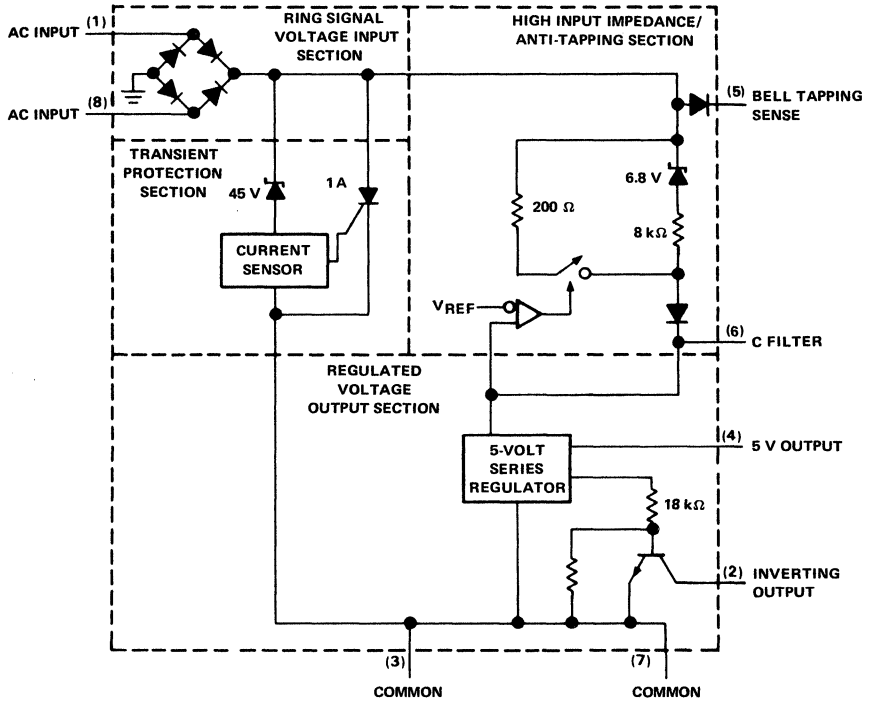
In typical telephone applications, the TCM1520A is activated through the telephone line by a ring voltage of 40 V at 16 Hz to 150 V at 68 Hz. The TCM1520A generates a signal suitable to drive an optocoupler or TTL, NMOS, or CMOS logic. The 5-V Output (pin 4) may be used as a supply source for optocouplers or low-power logic. This output is noninverting and will be at a high-level during ringing.

The TCM1520A incorporates lightning and transient protection that is designed to suppress lightning strikes of 1.5-kV amplitude and 200 μs duration. The TCM1520A also features built-in circuitry to avoid tapping or false triggering due to transients.

Caution. These devices have limited built-in gate protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

†BIDFET — Bipolar, Double-Diffused, N-channel and P-channel MOS transistors on the same chip — patented process.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Continuous supply voltage at pin 6 (see Note 1)	40 V
Continuous differential input voltage, V_{ID} (Pins 1 and 8)	40 V
Continuous output current, I_O	12 mA
Continuous SCR on-state input current (see Note 2)	200 mA
SCR on-state input current, $I_{I(on)}$ (duration $\leq 200\ \mu s$) (see Note 2)	900 mA
Continuous total dissipation (see Note 3)	1000 mW
Operating free-air temperature range	−20°C to 70°C
Storage temperature range	−40°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to pin 7.
2. SCR on-state input current is the current at the input when the SCR turns on.
3. For operation above 25°C free-air temperature, derate to 640 mW at 70°C at the rate of 8 mW/°C.

recommended operating conditions

	MIN	NOM	MAX	UNIT
High-level input voltage, V_{IH}			40	V
Low-level input voltage, V_{IL}			5	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range, R_L = open, $C_{(fltr)}$ = 10 μF (unless otherwise noted)

detector section

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{(BR)CEX}$	Collector-emitter output breakdown voltage, Pin 2	V_i ≤ 5 V (rms),	I_O = 5 μA	45			V
V_{OL}	Low-level output voltage, Pin 2	V_i = 25 V (rms),	I_O = 1.6 mA			1	V
V_{T+}	Positive-going threshold voltage				18	25	V
V_{T-}	Negative-going threshold voltage			6	7		V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)				11		V
$Z_{I(off)}$	Standby input impedance	V_i = 3 V,	f ≤ 20 kHz		10		MΩ
Z_{ring}	Impedance when ringing	V_{id} = 40 V,	f = 16 Hz		30		kΩ
		V_{id} = 130 V,	f = 20 Hz		20		kΩ
$I_{I(on)}$	On-state input current, SCR¶	See Note 4		55		110	mA
$V_{I(on)}$	On-state input voltage, SCR	See Note 4		50		100	V
$I_{I(hold)}$	Input holding current, SCR	See Note 4		100			μA
V_O	Output voltage, Pin 4	V_I = 40 V,	R_L = 10 kΩ	4.25		5.75	V
	Shunt voltage, Pin 6	I_I = 10 mA		38		50	V
	Operating current	V_I = 40 V,	Output open		1	1.6	mA

switching characteristics at 25 °C operating free-air temperature, f = 20 Hz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{on}	Turn-on time	V_I = 40 V			100	ms
$t_{(off)}$	Turn-off time	V_I = 40 V		175		ms
		V_I = 60 V to 150 V		300		

† All characteristics are measured with a 2.2 kΩ resistor connected to pin 1 and a 0.47 μF capacitor connected at pin 1 in series with the input signal, unless otherwise noted.
‡ All typical values are at T_A = 25 °C.
¶ This is the input current required to turn on the SCR.
NOTE 4: These parameters are measured using pulse techniques (t_w ≤ 200 μs, duty cycle ≤ 5%) with terminal pin 6 grounded.

PARAMETER MEASUREMENT INFORMATION

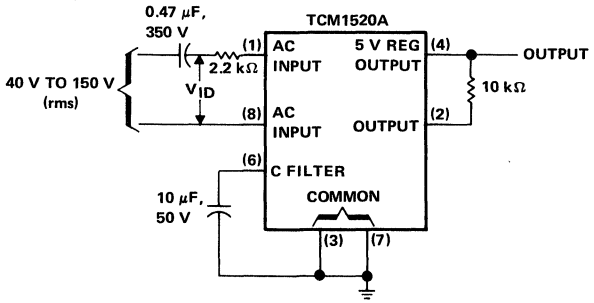


FIGURE 1. SWITCHING TEST CIRCUIT

TYPICAL CHARACTERISTICS

CAPACITOR VOLTAGE (PIN 6)
vs
DC INPUT VOLTAGE (PINS 1 AND 8)

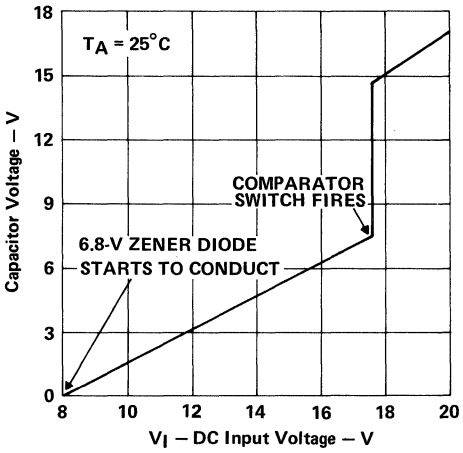


FIGURE 2

OUTPUT VOLTAGE (PIN 4)
vs
CAPACITOR VOLTAGE (PIN 6)

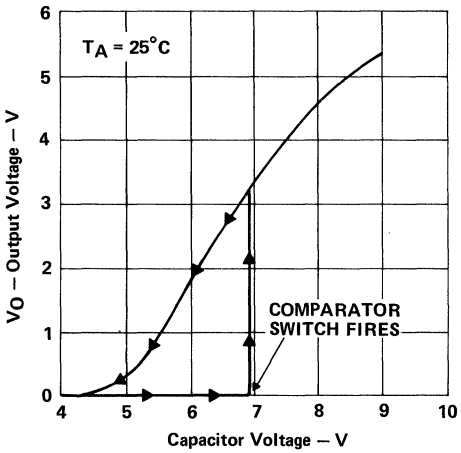


FIGURE 3

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

TYPICAL APPLICATION DATA

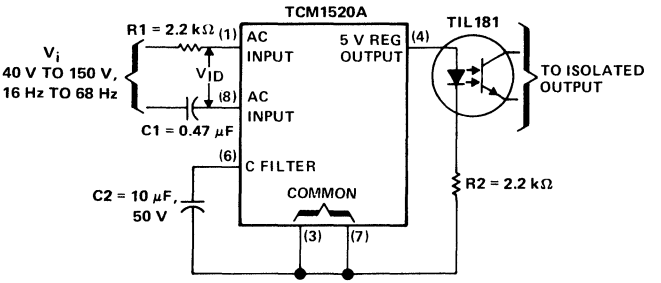


FIGURE 4. ISOLATED CONFIGURATION

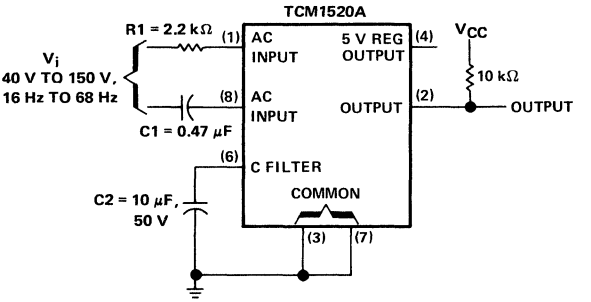


FIGURE 5. NONISOLATED CONFIGURATION

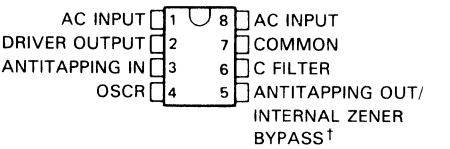
NOTE: See Table 1 for component functions.

TABLE 1. COMPONENT FUNCTIONS

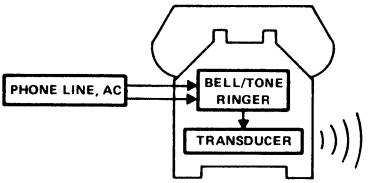
COMPONENT	FUNCTION
R1	Limits current into SCR during high voltage transients and aids in dial pulse rejection.
R2	Limits current into light-emitting diode.
C1	Blocks dc battery voltage in standby and aids in filtering dial pulses. Smaller values of C1 improve tapping immunity.
C2	Stores energy from the ring signal to power the 5-V regulator.
OPTOCOUPLER	Provides ground and transient isolation between the host system and the telephone line.

- **Electronic Replacement for Electromechanical Telephone Bell When Used with Transducer**
- **Designed to Meet or Exceed FCC Part 68 Class B Ringer Requirements**
- **Low-Cost External Component Requirements**
- **Low External Component Count**
- **High Standby Input Impedance . . . 1 MΩ Typ**
- **Low Ringer Equivalency Number . . . < 1 Typ**
- **Single-Ended High-Voltage Output Compatible with Piezo Transducer or Transformer-Coupled Speaker**
- **Reliable BIDFET† Process Technology Provides Efficient High-Voltage Operation**
- **On-Chip High-Voltage Full-Wave Diode Bridge Rectifier and Output Voltage Regulator**
- **On-Chip Circuitry Provides Ring Rejection of Rotary Dial Transients, Lightning, and Induced High-Voltage Transients**
- **On-Chip Thyristor Coupled with Additional External Components Provides Enhanced Rejection of Dial Pulses**
- **TCM1501B, TCM1512B, and TCM1506B are Improved Direct Replacements for TCM1501A, TCM1512A, and TCM1506A, Respectively**
- **Requires Only a Single-Value Oscillator Resistor Which Eliminates Binning Codes of the TCM15XXA Series**

P DUAL-IN-LINE PACKAGE
(TOP VIEW)



† Antitapping Output for TCM1531, TCM1532, TCM1536, and TCM1539. Internal Zener Bypass for B-suffix versions.



TYPICAL CHARACTERISTICS
TELEPHONE TONE RINGER DRIVER FAMILY

PART NO.	NOMINAL OUTPUT CENTER FREQUENCY (Hz)	WARBLE RATIO (f_H:f_L)	NOMINAL WARBLE FREQ. (Hz)
TCM1531, TCM1501B	2000	8:7	7.8
TCM1532, TCM1512B	1250	8:7	9.8
TCM1536, TCM1506B	500	5:4	7.8
TCM1539	2000	5:4	31.2

description

The TCM1531, TCM1532, TCM1536, TCM1539, TCM1501B, TCM1506B, and TCM1512B are monolithic integrated circuit telephone tone ringer drivers that, when coupled with an appropriate transducer, replace the electromechanical bell. These devices are designed, using BIDFET† technology, for use with either a Piezo transducer or an inexpensive transformer-coupled speaker to produce a pleasing tone composed of a high frequency (f_H) alternating with a low frequency (f_L) resulting in a warble frequency. Each device is powered and activated by the telephone line ring voltage, which may vary from 40 volts to 150 volts rms at frequencies from 15.3 hertz to 68 hertz.

During low voltage (off-hook) standby, typical input impedance is greater than 1 megohm; this prevents interference with telephone DTMF or voice signals without the use of expensive mechanical switches. This high standby impedance is achieved with an on-chip series zener diode that is activated by a differential input voltage of typically 8.9 volts at pins 1 and 8. A voltage level of typically 17 volts differential at pins

Caution. These devices have limited built-in gate protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

†BIDFET — Bipolar, double-diffused, N-channel and P-channel, MOS transistors on the same chip—patented process.

description (continued)

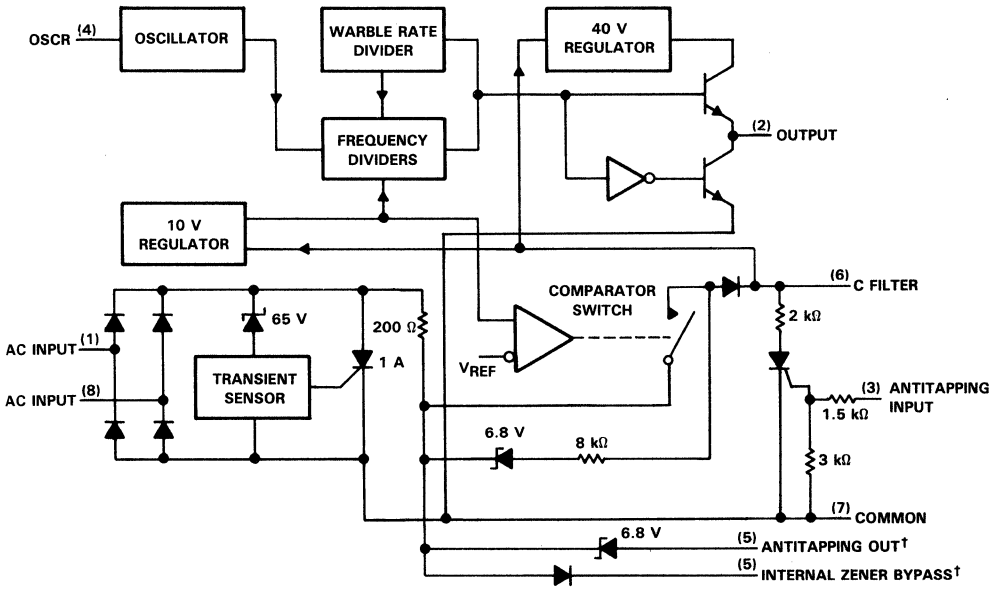
1 and 8 deactivates the internal zener diode, allowing for more efficient power transfer to the load when the device is in the operating mode. During ringing, the impedance of the applied circuit (see Figures 4, 5 and 6) varies from 30 kilohms to 8 kilohms over the Class B ring signal, and is reasonably independent of the output load.

These devices feature lightning and transient protection circuitry designed to withstand transients of 1.5 kilovolt for up to 200 microseconds duration when used with the proper external circuitry (see Figures 4 and 5). In addition, an on-chip thyristor coupled with an external resistor and capacitor circuit will reject dial pulses from parallel telephones so that false ringing (tapping) will not occur (see Typical Application Data).

The TCM1501B, TCM1506B, and TCM1512B have a provision for bypassing the internal series diode with one of lower voltage, thereby lowering the turn-on threshold of the device. If the antitapping thyristor is used with these devices, an external zener diode must be added in series with pin 5.

These telephone tone ringer drivers may be used in nontelephone communications applications. For example, the devices can be used with a few external components to produce an inexpensive and highly efficient alarm (see Figure 6).

functional block diagram



†Antitapping output for TCM1531, TCM1532, TCM1536, and TCM1539. Internal Zener Bypass for B-suffix versions.

absolute maximum ratings

Continuous peak-to-peak input voltage, pin 1 to pin 8 (see Note 1) . . . . . 110 V
Continuous dc input voltage at pin 6 . . . . . 55 V
Negative dc voltage, any pin . . . . . −1.2 V
Continuous output current, I_O, at pin 2 . . . . . 12 mA
Continuous output current, pin 5 and pin 6 . . . . . 30 mA
Continuous SCR on-state input current, pin 1 to pin 8 . . . . . 200 mA
SCR on-state input current, pin 1 to pin 8 (duration ≤200 μs) . . . . . 900 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 1000 mW
Operating free-air temperature range . . . . . −40°C to 85°C
Storage temperature range . . . . . −40°C to 125°C

NOTES: 1. For applications requiring ≥ 38 Vrms, an external resistor and capacitor are required to prevent damage to the device (see Note 3). Tip and ring may be connected interchangeably to either pin 1 or pin 8.
2. For operation above 25°C free-air temperature, derate linearly at the rate of 8 mW/°C.

recommended operating conditions

	MIN	MAX	UNIT
RMS input voltage, V_I (f = 15.3 Hz to 68 Hz) (see Note 3)	40	150	V
Resistor between OSCR and COMMON, R_{osc}	120	180	kΩ
Operating free-air temperature, T_A	−20	70	°C

NOTE 3: Input voltage is applied to pins 1 and 8 through a series 2.2 kΩ ± 10% resistor and a 0.47 μF ± 10% capacitor (see Figures 4, 5, and 6).

electrical characteristics at 25°C free-air temperature, R_L = open, $C_{(fltr)}$ = 10 μF, f = 20 Hz (unless otherwise noted), see Figure 2

detector section

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Ringing start threshold voltage	Pin 5 open, R_L = 4 kΩ		19	28	V
Ringing start threshold rms voltage	Pin 5 open, R_L = 4 kΩ, f = 15.3 Hz			40	V
Ringing stop threshold voltage	Pin 5 open, R_L = 4 kΩ	7	11		V
Ringing start threshold voltage	Antitapping thyristor activated		40		V
Pin 3 voltage required to activate antitapping thyristor			1		V
Pin 3 input current required to activate antitapping thyristor			0.2		mA
Standby input impedance	V_i = 3 V, f ≤ 20 kHz	0.1	1		MΩ
	V_i = 3 V, f ≤ 20 kHz (see Note 5)		10		kΩ
Impedance when ringing	V_i = 40 V, R_L = 4 kΩ, f = 15.3 Hz		25		kΩ
	V_i = 130 V, R_L = 4 kΩ		22		
Operating current	Pin 2 open, V_I = 40 V			1.3	mA
Low-level input current	V_I = 5 V			20	μA
SCR trigger voltage (pin 1 to pin 8)	All pins open, I_I ≤ 125 mA (see Note 4)	50	60	100	V
SCR trigger current (pin 1 to pin 8)	All pins open, V_I ≤ 100 V (see Note 4)	55	80	110	mA
SCR input hold current	(see Note 4)		10		mA

NOTES: 4. These parameters are measured using pulse techniques (t_w ≤ 200 μs, duty cycle ≤ 5%).
5. Pin 5 connected to pin 6, and pin 6 connected to pin 7 through a 100 Ω resistor.

electrical characteristics at 25°C free-air temperature, $C_{(fltr)}$ = 10 μF, f = 20 Hz (unless otherwise noted), see Figure 2

output section

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
Output voltage, pin 2	V_I = 17 V,	I_O = 2 mA,	See Note 6		10		V
	V_I = 50 V,	I_O = 5 mA,	See Note 6		44		
	V_i = 40 V,	I_O = 2 mA,	f = 16 Hz		8		
	V_i = 150 V,	I_O = 2 mA,	f = 15.3 Hz		40		
Output voltage, pin 6 (See Note 7)	V_I = 150 V,	f = 15.3 to 68 Hz				55	V
High-level output current	V_I = 50 V,	V_{OH} = 43 V			−15		mA
Low-level output current	V_I = 50 V,	V_{OL} = 1.5 V,	See Note 6		11		mA

NOTES: 6. Devices must be forced to the required output state by taking pin 4 to 8 V and toggling to 0 V as required. This stops the on-chip oscillator.

7. Normal device operation requires that a capacitor be connected from pin 6 to common (pin 7). A 10 μF capacitor is recommended for optimum antitapping vs turn-off-time performance of the circuit. Increasing or decreasing the value of this capacitor will respectively increase or decrease the antitapping capabilities of the circuit.

oscillator section

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Output tone frequency High tone frequency/ Low tone frequency	R_{osc} = 150 kΩ ± 1%	TCM1531, TCM1501B	1983/1736	2133/1867	2283/1998	Hz
		TCM1532, TCM1512B	1239/1085	1333/1167	1427/1249	
		TCM1536, TCM1506B	516/414	555.5/445.5	595/477	
		TCM1539	2066/1653	2222/1778	2378/1903	
Warble frequency	R_{osc} = 150 kΩ ± 1%	TCM1531, TCM1501B		7.8		Hz
		TCM1532, TCM1512B		9.8		
		TCM1536, TCM1506B		7.8		
		TCM1539		31.2		
Temperature coefficient of frequency	T_A = −20°C to 70°C			±0.05		%/°C

PARAMETER MEASUREMENT INFORMATION

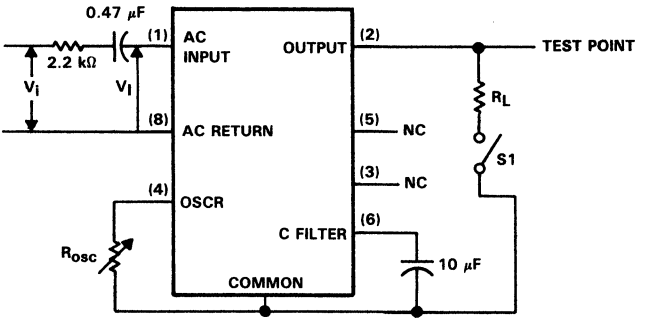


FIGURE 1. TEST CIRCUIT

TYPICAL CHARACTERISTICS

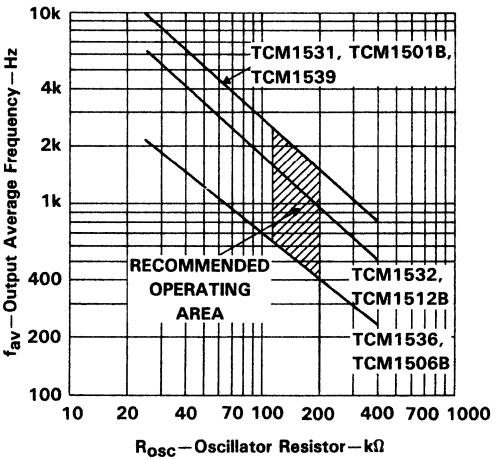


FIGURE 2. OSCILLATOR RESISTOR vs OUTPUT AVERAGE FREQUENCY

TYPICAL APPLICATIONS

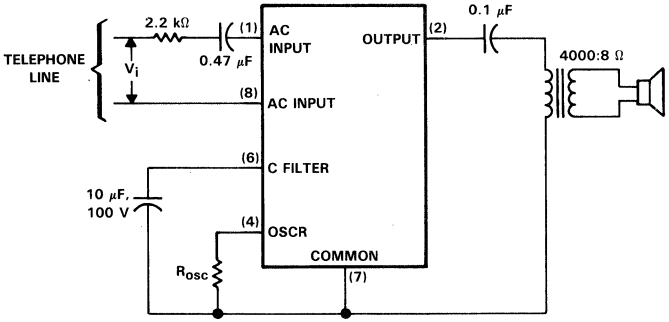


FIGURE 3. TELEPHONE APPLICATION—SPEAKER DRIVE

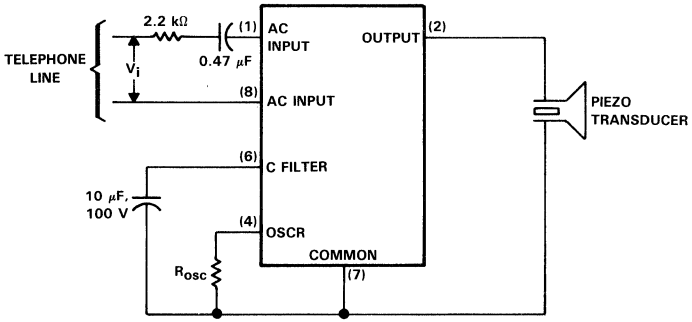
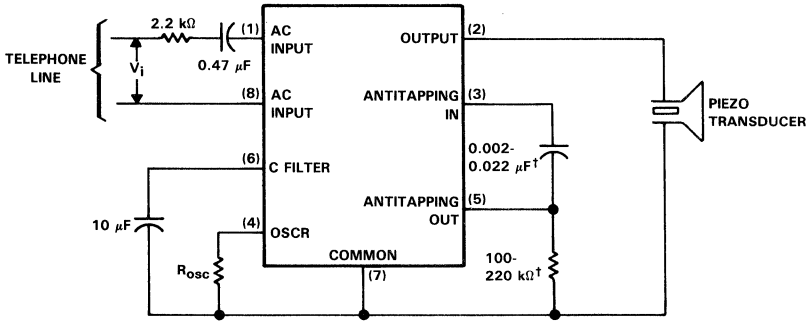


FIGURE 4. TELEPHONE APPLICATION—PIEZO DRIVE

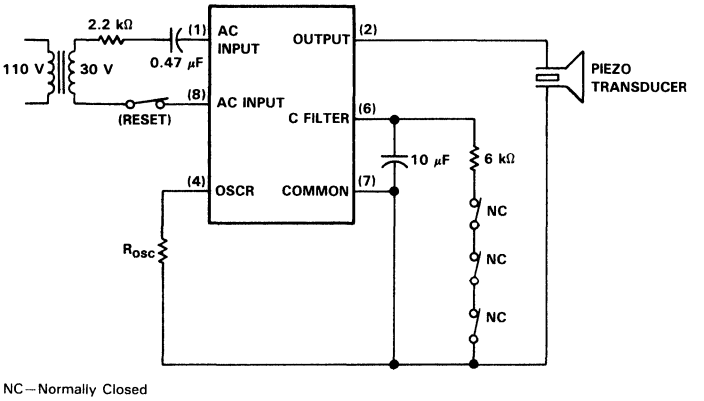


† Optimum values to be determined by specific antitapping requirements.

FIGURE 5. TELEPHONE APPLICATION, IMPROVED ANTITAPPING CIRCUIT

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

TYPICAL APPLICATIONS



NC—Normally Closed

FIGURE 6. ALARM SYSTEM CONFIGURATION

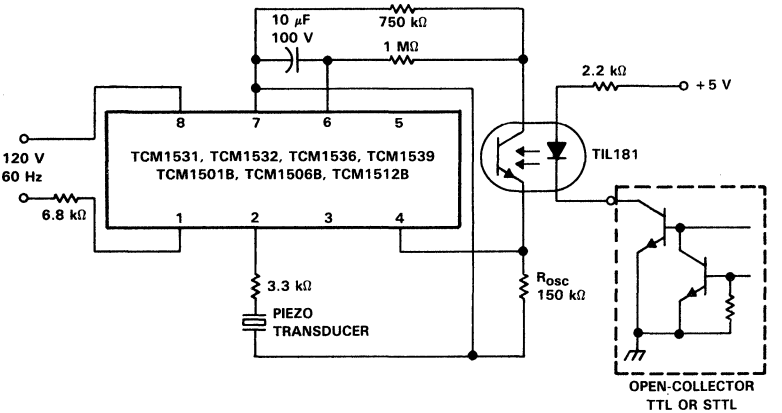


FIGURE 7. NONTELEPHONE APPLICATION

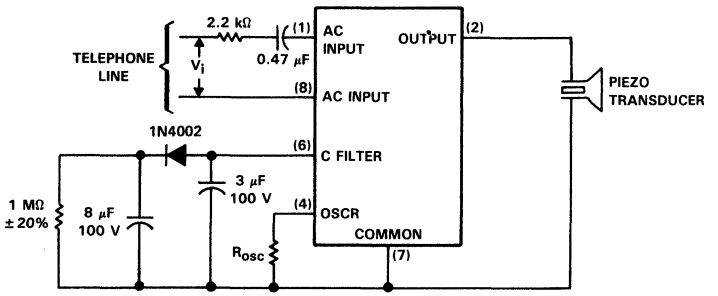
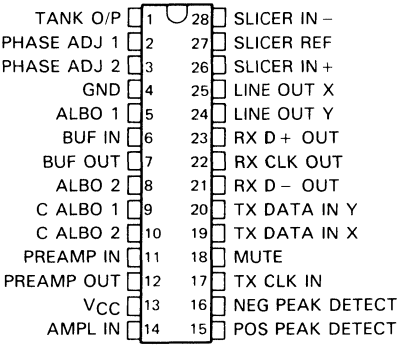


FIGURE 8. TELEPHONE APPLICATION—PIEZO DRIVE FAST RING SIGNAL CUTOFF

D2861, AUGUST 1985—REVISED DECEMBER 1987

- **Transmits and Receives Serial Bipolar Data at Up to 3 Mbit/s Using Two Twisted-Wire Pairs.**
- **Low-Q Clock Extraction**
- **Two ALBO (Automatic Line Build Out) Taps with a Range of 42 dB**
- **On-Chip Amplifier with 50-dB Open-Loop Voltage Amplification**
- **Phase Adjustment for Recovered Clock**
- **Direct Interface with the TCM2222 AMI/HDB3 (Alternate Mark Inversion/High-Density Bipolar, Third Order) Encoder/Decoder**
- **Receive Line Signal Loss Detection with Mute Output**
- **Bipolar Technology**

TCM2203
J
DUAL-IN-LINE PACKAGE
(TOP VIEW)

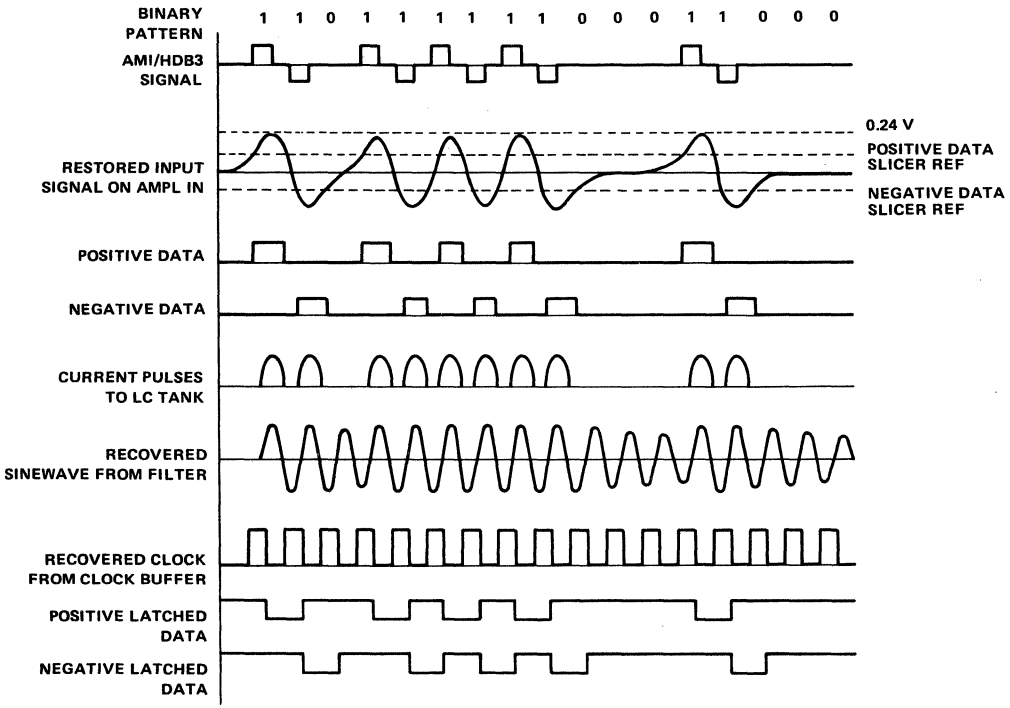


description

The TCM2203 is designed to perform the interface function between the bipolar data encoder/decoder (e.g., TCM2222) and the line. The TCM2203 consists of a receiver that extracts clock information and reshapes the data waveforms, and a transmitter that interfaces bipolar data to the line. Detection of receive signal loss is performed and a mute output is available. Auto-adaptive slicing level ensures excellent jitter and error performance.

The TCM2203 is characterized for operation from 0°C to 70°C.

typical timing diagram



NOTE: A low logic level on RX DATA OUT represents a received pulse, or a "mark." RX DATA OUT is latched on the falling edge of RX CK OUT, and tracks the input signal when RX CK OUT is high.

absolute maximum ratings over free-air operating temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 15 V
Continuous total dissipation at 25°C free-air temperature . . . . . 1 W
Operating free-air temperature range . . . . . −10°C to 85°C

NOTE 1: Voltage is with respect to network ground.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5.0	5.5	V
Operating free-air temperature, T_A		0		70	°C
V_{IL}	TX Data in Y			0.80	V
V_{IL}	TX Data in X			0.80	V
V_{IH}	TX CLK in	3.0			V

electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	SECTION	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	RX D+ out RX D− out RX CLK out	V_{CC} = 5 V, I_{OH} = 40 μA	4.5	4.8		V
I_{IL} I_{IH}	TX Data in Y TX Data in X TX CLK in	V_{IL} = 0 V, V_{IH} = 5 V			±50 ±50	μA
On-state impedance	ALBO			25	50	Ω
Off-state impedance		V_{P-P} = 480 mV	9	11		kΩ
Dynamic resistance matching error				2%		
Transconductance‡ (referenced to pin 14)			0.11	0.15		s
Input impedance	Buffer	f_Q = 1 MHz	10	20		kΩ
Output impedance				40		Ω
Voltage amplification			4.5	5.3	6.0	dB
Input impedance	Pre-Amp	f = 1 MHz	40	60		kΩ
Output impedance	Preamplifier	f_Q = 1 MHz		50		Ω
Open-loop voltage amplification		V_{CC} = 5 V, V_F = 1 MHz	42	46		dB
Unity-gain frequency				40		MHz
Input impedance	Phase slicer amplilfier	f_Q = 1 MHz	7	11		kΩ
Voltage amplification (each output)			4.5	5.3	6.0	dB
Capacitance-driving capability, peak detect pins					0.1	μF
Input impedance	Clock Slicer	f_Q = 2 MHz	100	150		kΩ
Voltage amplification		f_Q = 2 MHz		60		dB
Input-to-output delay		f_Q = 2 MHz, PHASE ADJ CAP = 75 pF		60		ns
Peak-to-peak eye amplitude	Data Slicer	V_{CC} = 5 V		480		mV
Data slicing level				50%		
Clock slicing level§				66%		
Negative-going threshold voltage	Mute	V_{CC} = 5 V		3.3		V
Positive-going threshold voltage				3.5		
Leakage	RX D+ OUT, RX D− OUT	V_{OH} = 5 V			50	μA
Low-level output voltage, V_{OL}		I_{OL} = 2 mA		0.85	1	V
Leakage	LINE OUT X, LINE OUT Y	V_{OH} = 5 V			50	μA
Low-level output voltage, V_{OL}		I_{OL} = 20 mA		0.9	1.1	V
Leakage	Mute	V_{OH} = 5 V			50	μA
Low-level output voltage, V_{OL}	Mute	I_{OL} = 1 mA		250	400	mV
Output rise time, t_r	LINE OUT X, LINE OUT Y	R_L = 220 Ω		50	100	ns
Output fall time, t_f		R_L = 220 Ω		50	100	ns
Supply current, I_{CC}		V_{CC} = 5 V		25	40	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Transconductance is defined as the change in current for each diode string divided by the change in peak-to-peak voltage at pin 14.
§ Clock slicing level is the data level at which the TANK O/P puts out a current pulse.

TYPICAL CHARACTERISTICS

EYE DIAGRAM REGULATION
(AT INPUT OF 6- dB AMPLIFIER)

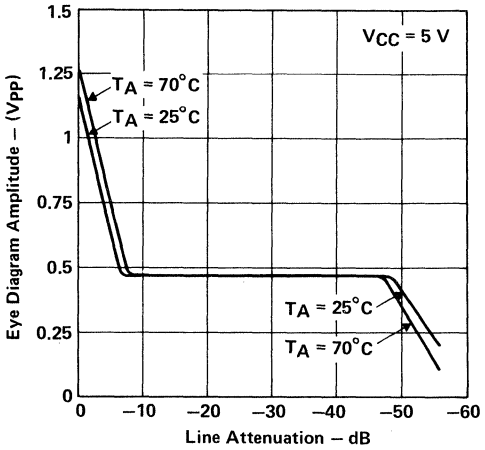


FIGURE 1

TYPICAL PREAMPLIFIER VOLTAGE
AMPLIFICATION CHARACTERISTICS

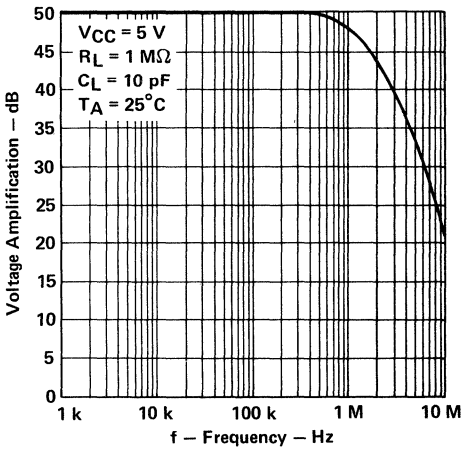


FIGURE 2

TYPICAL PREAMPLIFIER PHASE CHARACTERISTICS

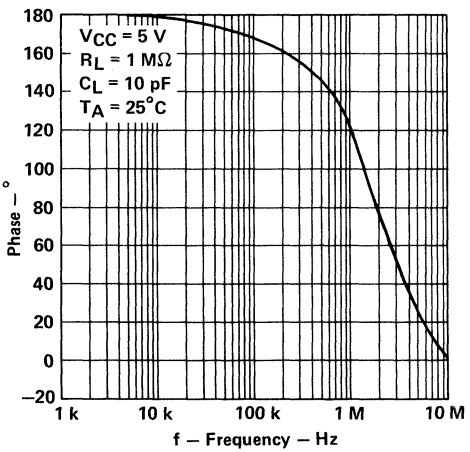


FIGURE 3

PREAMPLIFIER OPEN-LOOP VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

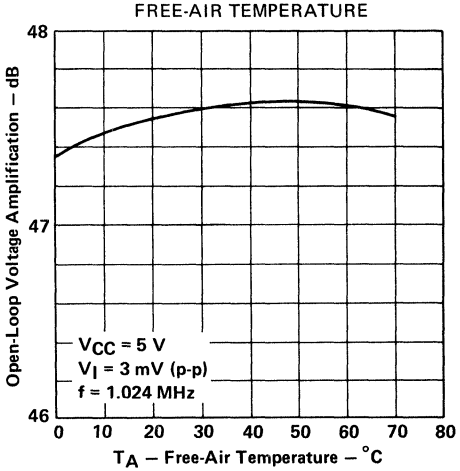


FIGURE 4

TEXAS INSTRUMENTS
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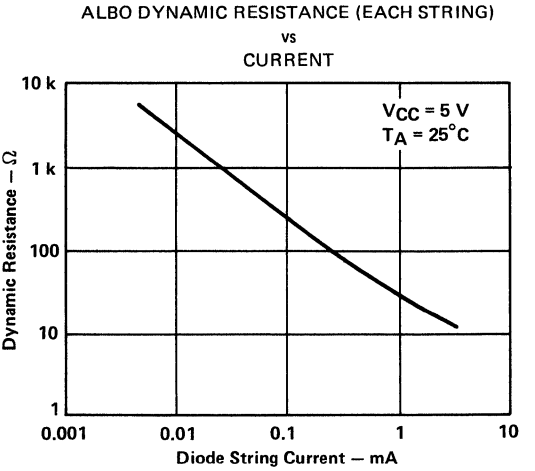


FIGURE 5

PRINCIPLES OF OPERATION

general

The TCM2203 is designed to form the interface between a bipolar decoder/encoder and the transmission line. It is optimized for 1.536 MHz, 1.544 MHz, and 2.048 MHz operation, but is capable of operating at 3.152 MHz and low frequency for special applications. The TCM2203 can be considered in two separate parts, a transmitting section and a receiving section.

receiving section

This section performs three functions: signal restoration, clock recovery, and data slicing. It also detects loss of incoming signal and flags this condition by taking the mute output high.

signal restoration

The incoming signal is typically very distorted and exhibits considerable intersymbol interference. The input section must restore the signal to provide a clear eye diagram to the data and clock slicer. An amplifier with open-loop voltage amplification of 50 dB with externally adjusted gain, together with the bode networks and associated ALBO taps, give a dynamic range of up to 36 dB (6 dB to 42 dB). This allows positioning of the terminal at any line length (within the limits of ALBO dynamic range) from repeater or like transmitter.

Equalization of the line characteristics is performed by a simple external series LC network buffered by the 6-dB amplifier. The restored signal from the 6-dB phase splitter (controlled to 0.48 V peak-to-peak) is sent to two peak detectors that store the peak values on external capacitors. The average peak values are then summed to provide a signal level, which is compared to a V_{CC}-derived reference to form an error signal level. This error signal level controls the current in the ALBO strings. As ALBO string current increases, the dynamic resistance of the string decreases and more signal is shunted to ground. In this way, automatic gain control and automatic line build out are acheived. Typically, there is frequency response contouring associated with the automatic gain control to compensate for the responses of different lengths of line.

clock extraction

The received signal contains its own clock information, which must be extracted in the receive section. An averaged peak input signal is derived from the sum of the positive and negative peak detectors. The negative peak detector is actually the positive peak of AMPL IN inverted. Alternately, the peak average sum is equal to the sum of the averaged absolute values of the negative and positive peaks. When the negative or positive pulse at AMPL IN exceeds 66% of the averaged peak value, a current pulse occurs at the TANK O/P output. These current pulses are filtered by a tuned-primary transformer-coupled circuit to extract the clock and drive the slicer inputs. The slicer converts the sinewave into a binary square-wave clock signal. The transformer-coupled tuned-primary circuit sets the clock extraction Q. The slicer is a high-gain 60-dB comparator that minimizes conversion of amplitude modulation in the sine wave to phase modulation in the recovered square wave clock.

data slicing

The data comparators trigger whenever the signal goes above 50% of the average peak values from the peak detectors. This data is then presented to the data latches and latched into the output buffers by the falling edge of the recovered clock. When the RX CLK OUT is high, RX D− OUT and RX D+ OUT track the comparators. The clock buffer trigger circuit can be externally phase adjusted with a 5-pF to 75-pF trim capacitor across PHASE ADJ 1 and PHASE ADJ 2 to set the falling edge exactly to the center of the data pulses. This maximizes jitter acceptance and noise immunity.

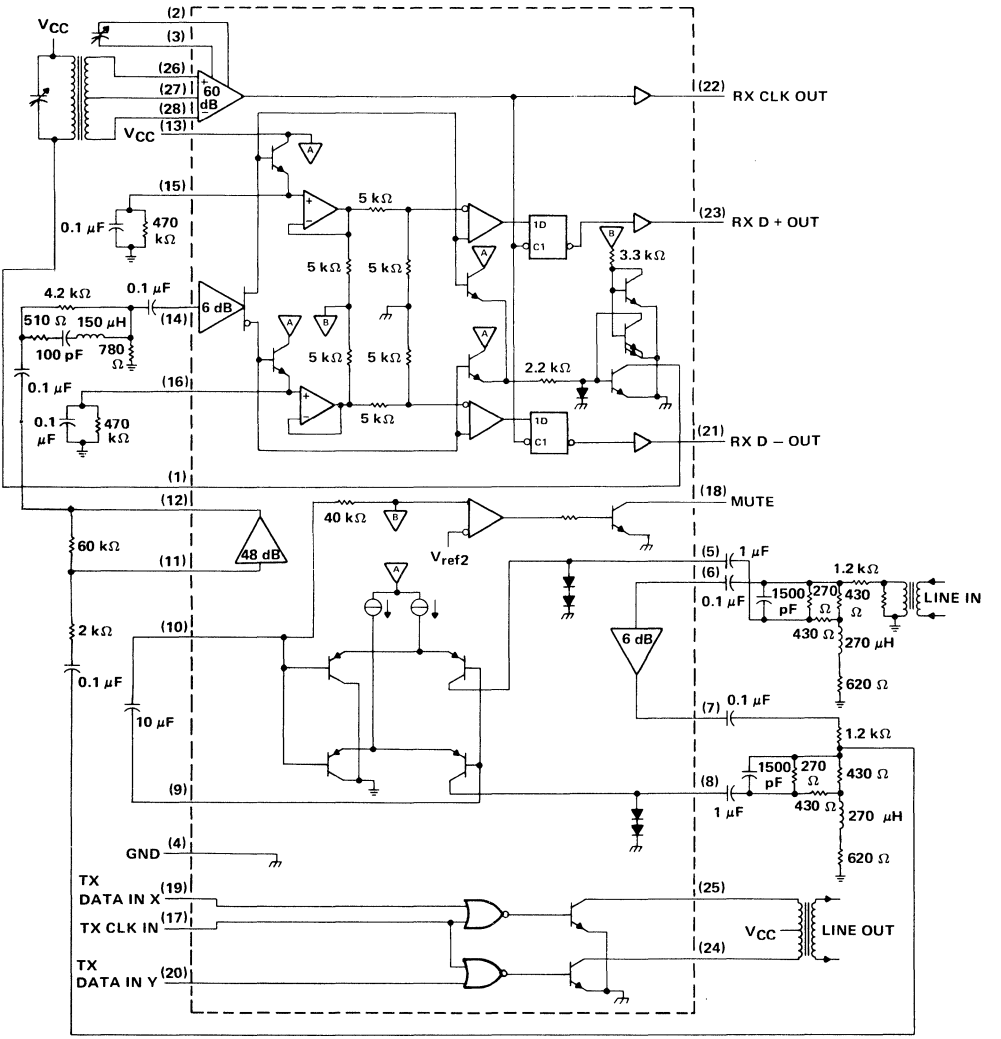
receive signal loss detection

The average peak data values are half-summed to give a dc value that is compared to an internal reference relative to V_{CC}. When the value falls below 33% of the nominal value after ALBO gain control, the MUTE output goes high.

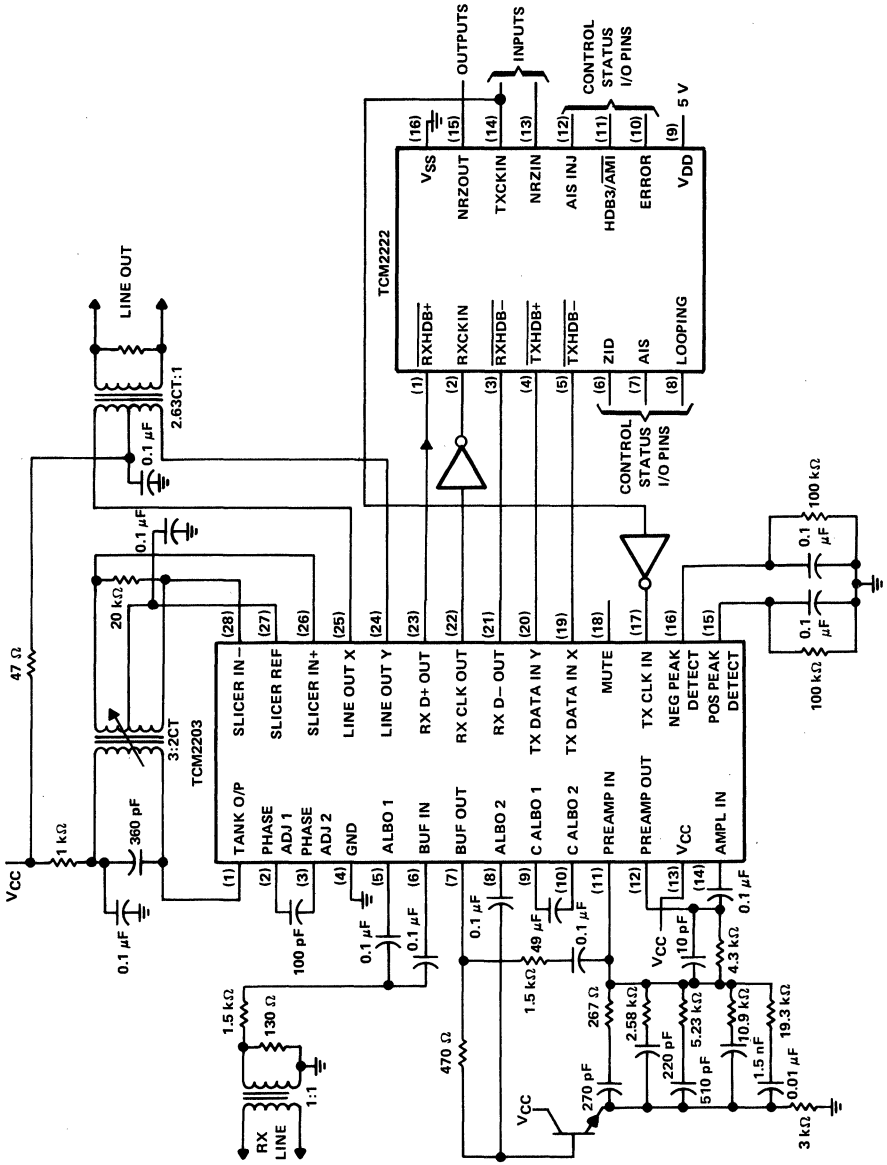
transmitting section

The transmitting section gates the signals applied to TX DATA IN X and TX DATA IN Y with the signal applied to TX CLK IN. The gated signals are then applied to the line outputs. The line output pulse duration is one-half of the bit period. The LINE OUT X and LINE OUT Y outputs are open-collector n-p-n transistors. Each collector will sink 20 milliamperes when the appropriate TX DATA IN input and TX CLK IN are at low levels.

TYPICAL APPLICATION DATA



TYPICAL APPLICATION DATA

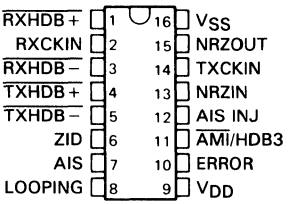


TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

D2894, OCTOBER 1985—REVISED DECEMBER 1987

- **AMI or HBD3 Encoding of Binary Data**
- **Simultaneous Decoding of Received AMI or HDB3 Signal**
- **Static Logic Allows Zero to 3-MHz Bit Rate**
- **Seven Outputs for Received-Signal Diagnostics**
- **Reliable NMOS Technology**
- **Single 5-V Supply**

J PACKAGE
(TOP VIEW)



description

The TCM2222 performs three functions: encoding, decoding, and signal monitoring.

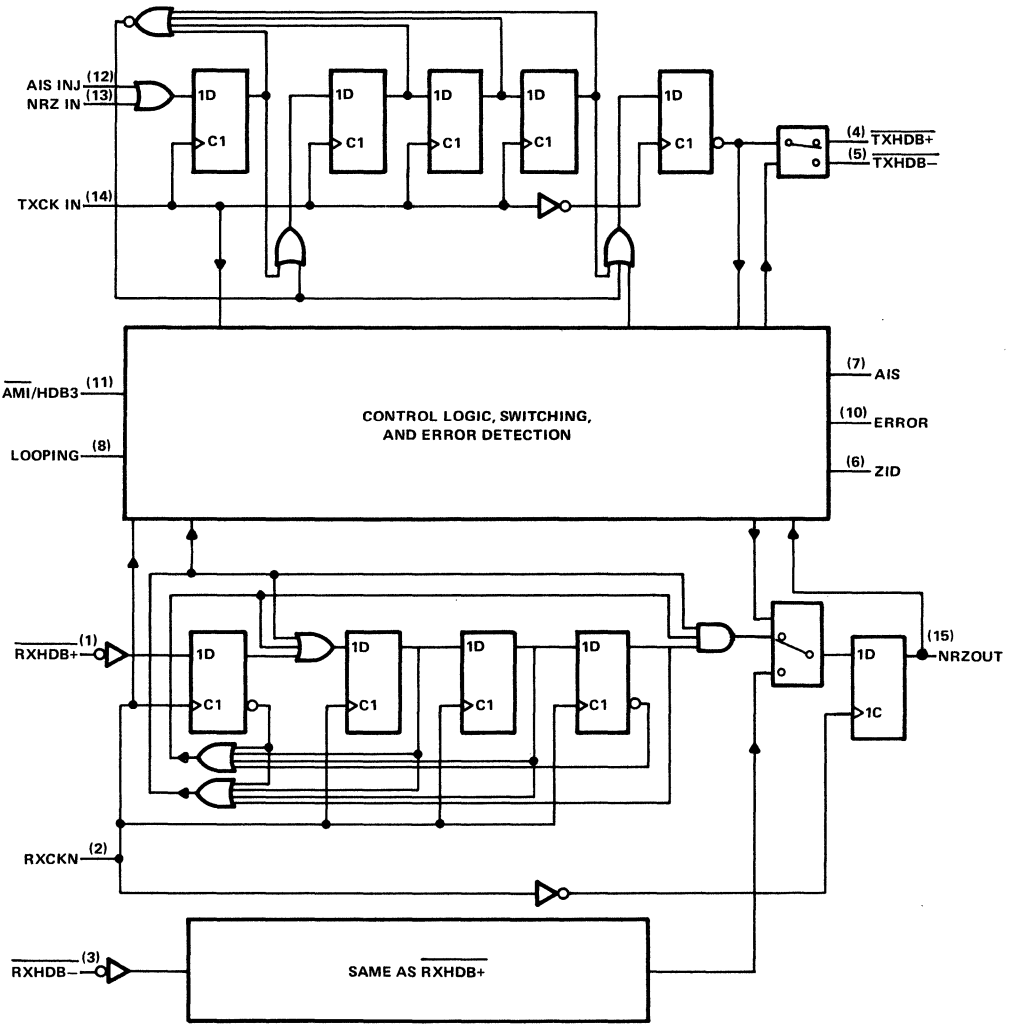
In the encoding section, a binary non-return-to-zero (NRZ) signal is converted to a ternary signal to improve its transmission characteristics. In the decoding section, a received ternary signal is independently converted into a binary form. In the signal-monitoring section, the received ternary signal in the decoder is checked for various diagnostics, and errors that are found are flagged.

The TCM2222 can be directly connected to the TCM2203 line interface device to form a complete equipment transmission interface.

The TCM2222 is characterized for operation from 0°C to 70°C.

Caution. These devices have limited built-in gate protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

functional block diagram



PIN FUNCTIONAL DESCRIPTION

PIN NAME	PIN NO.	DESCRIPTION
AIS	7	Alarm Inhibit Signal output. High when an alarm-inhibit consisting of essentially all highs is received from the line.
AIS INJ	12	Alarm Inhibit Signal Injection input. Forces the alarm inhibit signal (all pulses) onto outputs $\overline{\text{TXHDB}+}$ and $\overline{\text{TXHDB}-}$.
$\overline{\text{AMI}}$/HDB3	11	Alternate Mark Inversion ($\overline{\text{AMI}}$) or High-Density Bipolar-Three (HDB3) control input. When high, HDB3 is selected. When low, $\overline{\text{AMI}}$ is selected
ERROR	10	Error output. Goes high for one-half cycle at every error found in the incoming line signal.
NRZIN	13	Serial binary Non-Return-to-Zero (NRZ) data input.
NRZOUT	15	Non-Return-to-Zero output. Binary NRZ data recovered from the $\overline{\text{RXHDB}+}$ and $\overline{\text{RXHDB}-}$ inputs. "Stuffing" sequence pulses are removed when the $\overline{\text{AMI}}$/HDB3 control input is high.
RXCKIN	2	Clock from PCM transceiver. $\overline{\text{RXHDB}+}$ and $\overline{\text{RXHDB}-}$ data are clocked in on the rising edge of RXCKIN.
$\overline{\text{RXHDB}+}$	1	Receive High-Density Bipolar Positive input. One of two data inputs to the decoder section. A low level indicates a positive pulse from the line.
$\overline{\text{RXHDB}-}$	3	Receive High-Density Bipolar Negative input. One of two data inputs to the decoder section. A low level indicates a negative pulse from the line.
TXCKIN	14	Transmit Clock input. The NRZIN input data is clocked in on the rising edge of TXCKIN.
$\overline{\text{TXHDB}+}$	4	Transmit High-Density Bipolar Positive output. Low when a positive pulse is sent to the line.
$\overline{\text{TXHDB}-}$	5	Transmit High-Density Bipolar Negative output. Low when a negative pulse is sent to the line.
V_{DD}	9	Positive supply voltage, 5 V ±10%.
V_{SS}	16	Supply ground (0 V).
ZID	6	Incoming Zero Detection output. High when a sequence of 128 consecutive lows is received from the line. Disabled in the $\overline{\text{AMI}}$ mode.

absolute maximum ratings over free-air operating temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . 0.3 V to 7 V
Input voltage, V_I . . . . . −0.3 V to 20 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 1375 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds . . . . . 300°C

NOTES 1: All voltages are with respect to V_{SS}.
2. For operation above 25°C free-air temperature, derate linearly to 880 mW at 70°C at the rate of 11 mW/°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply ground		0		V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	All outputs except $\overline{TXHDB\pm}$	V_{DD} = 5 V, I_{OH} = −120 μA	2.4			V
		$\overline{TXHDB+}$, $\overline{TXHDB-}$	V_{DD} = 5 V, I_{OH} = − 40 μA	4.2			
V_{OL}	Low-level output voltage	All outputs except $\overline{TXHDB\pm}$	V_{DD} = 5 V, I_{OL} = 2.4 mA			0.4	V
		$\overline{TXHDB+}$, $\overline{TXHDB-}$	V_{DD} = 5 V, I_{OL} = 2 mA			0.4	
I_{IH}	High-level input current		V_{DD} = 5.5 V, V_{IH} = 2.4 V			10	μA
I_{IL}	Low-level input current		V_{DD} = 5.5 V, V_{IL} = 0.4 V			−10	μA
I_{DD}	Supply current		V_{DD} = 5 V		60	75	mA
C_i	Input capacitance					20	pF

timing requirements, transmit and receive sections

PARAMETER		MIN	MAX	UNIT
t_{su1}	Setup time, NRZIN before TXCKIN↑	40		ns
t_{h1}	Hold time NRZIN after TXCKIN↑	40		ns
t_{su2}	Setup time, $\overline{RXHDB\pm}$ before RXCKIN↑	40		ns
t_{h2}	Hold time, $\overline{RXHDB\pm}$ after RXCKIN↑	40		ns
t_{r1}	Rise time, RXCKIN		25	ns
t_{f1}	Fall time, RXCKIN		15	ns

switching characteristics, transmit and receive sections

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
t_{r2}	Rise time, $\overline{TXHDB\pm}$	C_L = 25 pF,	I_{OH} = −40 μA		40	ns
t_{f2}	Fall time, $\overline{TXHDB\pm}$	C_L = 25 pF,	I_{OL} = 2 mA		40	ns
t_{r3}	Rise time, NRZOUT	C_L = 50 pF,	I_{OH} = −120 μA		100	ns
t_{f3}	Fall time, NRZOUT	C_L = 50 pF,	I_{OL} = 2.4 mA		100	ns
t_{w1}	Pulse duration, ERROR output	I_{OH} = −120 μA, C_L = 25 pF,	I_{OL} = 2.4 mA, t_{cC} = 488 ns	200		ns
t_{pd1}	Propagation delay, TXCKIN to $\overline{TXHDB\pm}$	I_{OH} = −40 μA, C_L = 25 pF	I_{OL} = 2 mA,	50	200	ns

PARAMETER MEASUREMENT INFORMATION

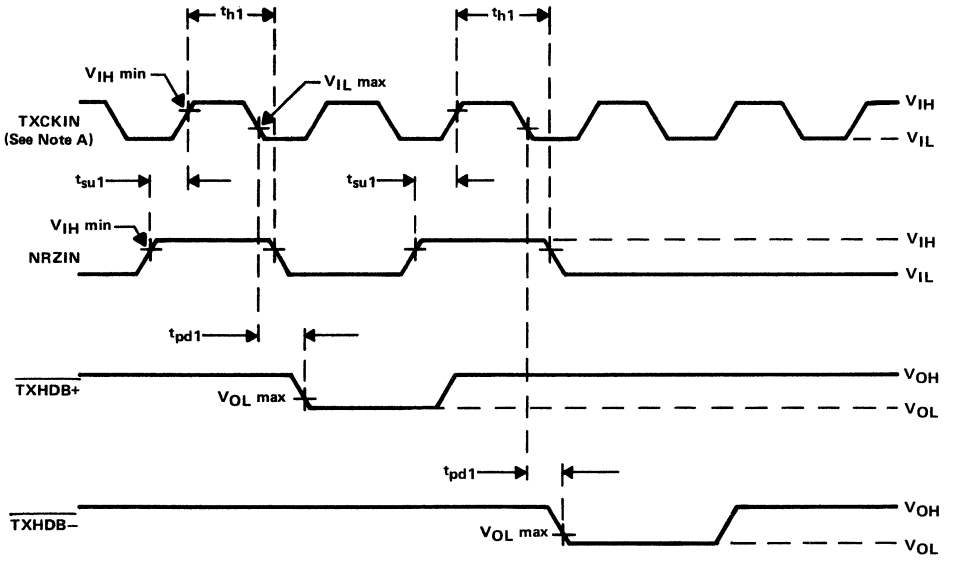


FIGURE 1. TRANSMIT CHANNEL TIMING INFORMATION (AMI MODE†)

NOTE A: The CLKSENSE is low and the rising edge of the TXCKIN is used to strobe NRZIN.
†In the HDB3 mode, the pulses on $\overline{\text{TXHDB}}\pm$ are delayed three additional clock periods.

PARAMETER MEASUREMENT INFORMATION

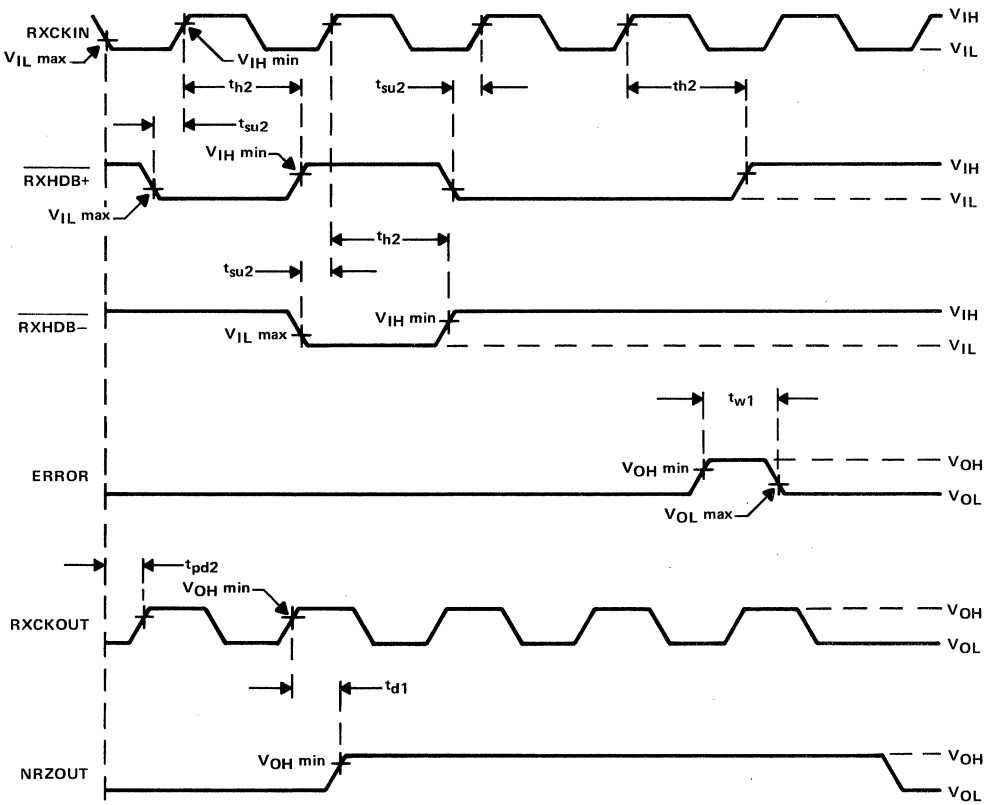


FIGURE 2. RECEIVE CHANNEL TIMING INFORMATION (AMI MODE†)

†In the HDB3 mode, NRZOUT is delayed three additional clock periods.

PRINCIPLES OF OPERATION

The TCM2222 combines a coder section and a decoder section to which a signal monitor function is attached. It can operate at clock frequencies from zero to 3 MHz in either the AMI or HDB3 modes. The AMI or HDB3 mode is selected by the $\overline{\text{AMI}}$/HDB3 input.

Binary data at the NRZIN input is clocked into the coder on the rising edge of TXCKIN. In the AMI mode a logic high at NRZIN causes an output at either $\overline{\text{TXHDB}}+$ or $\overline{\text{TXHDB}}-$ on the falling edge of TXCKIN. In the HDB3 mode, the output appears on the falling edge of TXCKIN 3.5 clock cycles later. This delay allows the insertion of extra pulses due to sequences of four consecutive lows. When the AIS INJ input is high, data at NRZIN is ignored and an "all highs" signal is transmitted with alternate outputs on $\overline{\text{TXHDB}}+$ and $\overline{\text{TXHDB}}-$ every clock cycle.

Ternary data received at $\overline{\text{RXHDB}}-$ or $\overline{\text{RXHDB}}+$ is clocked into a decoder on the rising edge of RXCKIN. In the AMI mode, the decoded data is output on NRZOUT on the falling edge of RXCKIN 0.5 clock cycles later. In the HDB3 mode, the receiver recognizes violation pulses and removes any pulse sequences added by the originating equipment, and outputs the decoded data 3.5 clock cycles later.

If the LOOPING input is high, the decoder ignores data received on $\overline{\text{RXHDB}}+$ or $\overline{\text{RXHDB}}-$ and uses data at the $\overline{\text{TXHDB}}+$ and $\overline{\text{TXHDB}}-$ outputs. In addition, RXCKIN is ignored and TXCKIN is used to control the decoder timing. In the AMI mode there is a 1.5-clock-cycle delay from NRZIN to NRZOUT. In the HDB3 mode the delay is 7.5 clock cycles.

A signal monitor circuit associated with the decoder monitors the received ternary signal and diagnoses the presence of particular conditions. There are three received signal diagnostic outputs. The three outputs are as follows:

ERROR This output flags an error in the received signal by pulsing high for 0.5 clock cycles. In the AMI mode an error is two consecutive pulses of the same polarity. In the HDB3 mode an error can be either the same as the AMI error (provided it is not part of a violation stuffing sequence) or an incorrect stuffing sequence. On power up, the ERROR output remains high until the RXCKIN input is functioning.

ZID This flag is set high if a sequence of 128 incoming lows is detected. It is inhibited when the device is in AMI mode. The output is latched if the RESET input is low.

AIS The AIS output goes high when two frames of 512 bits each, each containing no more than two lows, is received. If the reset input is low, the output is latched. This flag is set if a sequence of continuous highs is detected.

Other pin functions are as follows:

RESET A positive transition on this input resets the ZID and AIS outputs for one cycle of RXCKIN. They are then free to be set again when their diagnostic condition occurs. RESET can be used in the normally high mode, in which the outputs are not latched but continuously reflect the current diagnostic status.

ternary data transmission

Ternary signals are used in telecommunications to transmit data over long distances because they offer improved transmission characteristics compared to binary signals. The requirements are:

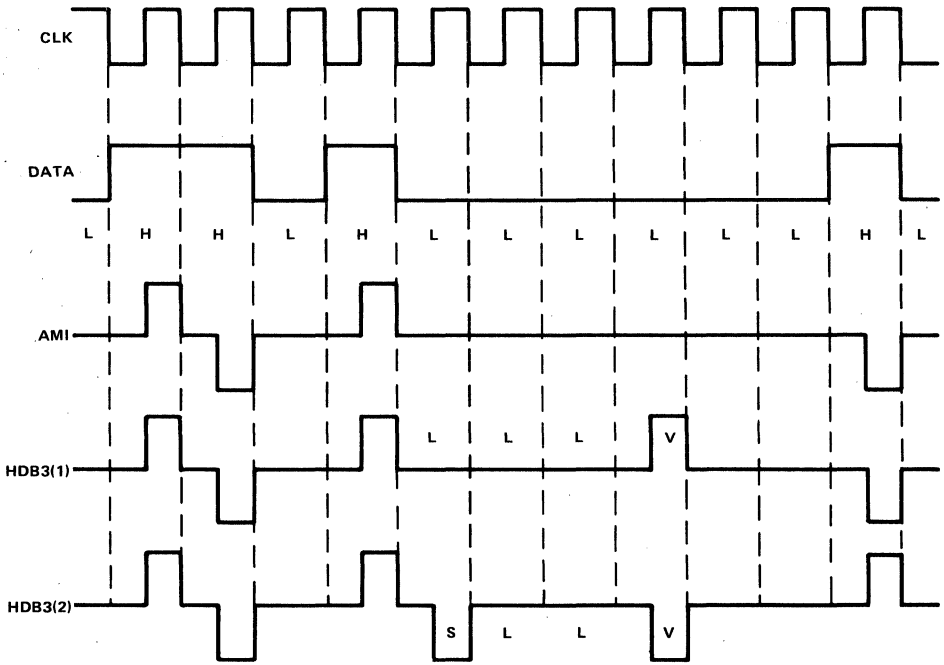
Narrow bandwidth for good signal-to-noise ratio.
Minimum high-frequency content to allow wider repeater spacing.
No dc component in the signal to allow inexpensive transformer coupling without distortion.
Timing information carried with the data to allow extraction of the clock.
Error detection to flag faults and enable their location.

PRINCIPLES OF OPERATION

The ternary signal is bipolar. It has a zero center level, which is the rest condition, and positive and negative levels of equal amplitude. The simplest form of coding is Alternate Mark Inversion (AMI) in which successive logic highs in the binary signal are transmitted alternately as positive or negative pulses. Logic lows are transmitted as a zero level. The disadvantage of this type of coding is that no timing information is contained in a succession of logic lows, requiring the remote receiver to use a high-Q (crystal-controlled) clock extraction circuit if long successions of lows are to be received.

To improve the timing content, high-density bipolar third-order coding (HDB3) can be used. This is identical to AMI except that four successive lows cause the insertion of a violation bit that is a logic high pulse of the same polarity as the previous logic high pulse (see Figure 3). This increases the timing information and allows the use of a low-Q LC tank circuit in the clock extractor. The extra bits are removed by the decoder, introducing a transmission delay of four cycles.

In order to maintain zero dc content, the violation bit must be the same polarity as the previous bit but of opposite polarity to the previous violation bit. To replace four consecutive lows, there are two possible sequences of pulses; LLLV if there is an odd number of logic highs since the last violation bit, or SLLV if there is an even number of logic highs. In this notation S represents a "stuffing" bit of opposite polarity than the previous pulse and V represents a "violation" bit of the same polarity.



NOTE 3: In the HDB3(1) signal, the previous violation bit was negative. In the HDB3(2) signal, the previous violation bit was positive.

FIGURE 3. TERNARY DATA TRANSMISSION TIMING DIAGRAM

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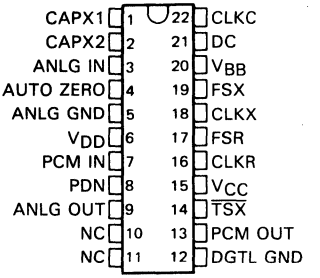
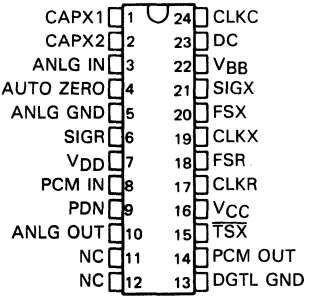
D2664, JUNE 1982—REVISED MARCH 1986

- **TCM2909 Provides μ-Law Companding in 22-Pin Package**
- **TCM2910A is Designed to be Interchangeable with Intel 2910A**
- **Compatible with CCITT Recommendations G.711 and G.712**
- **μ-255-Law Encoding and 8th-bit Signaling (TCM2910A only) Compatible with AT&T D-Type Channel Banks**
- **TTL-Compatible Digital Inputs and Outputs**
- **Optional Programmable Time-Slot Selection**
- **Low Operating Power Consumption:**
  Active . . . . . 230 mW Typical
  Power-Down Mode . . . . . 33 mW Typical
- **±5% Power Supplies: +12 V, +5 V, −5 V**
- **High-Reliability, Advanced N-Channel MOS Technology**
- **Low External Component Count**
- **PEP Processing Available**

TCM2909
J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



TCM2910A
J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



NC—No internal connection

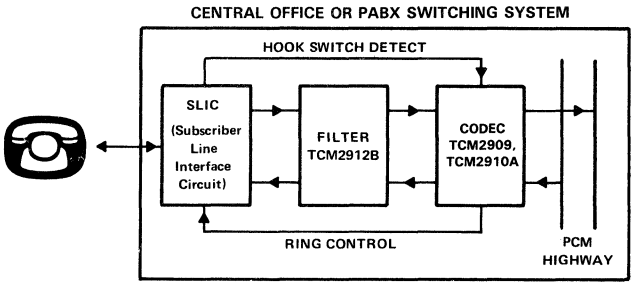
description

The TCM2909 and TCM2910A are single-chip pulse-code-modulated encoders/decoders (PCM codecs) that provide all the functions required to interface a full duplex (4-wire) voice telephone circuit with a time-division-multiplexed (TDM) system. Integrated into the codecs are circuits for signaling interface, PCM time-slot control logic, analog-to-digital (A/D) conversion, and digital-to-analog (D/A) conversion. Primary applications of the devices include:

- Line interface for digital transmission and switching of T1 Carrier, PABX, and Central Office telephone systems
- Subscriber line concentrators
- Digital encryption systems
- Digital voice-band data storage systems
- Digital signal processing

The TCM2909 and TCM2910A are characterized for operation from 0°C to 70°C.

Caution. These devices have limited built-in gate protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.



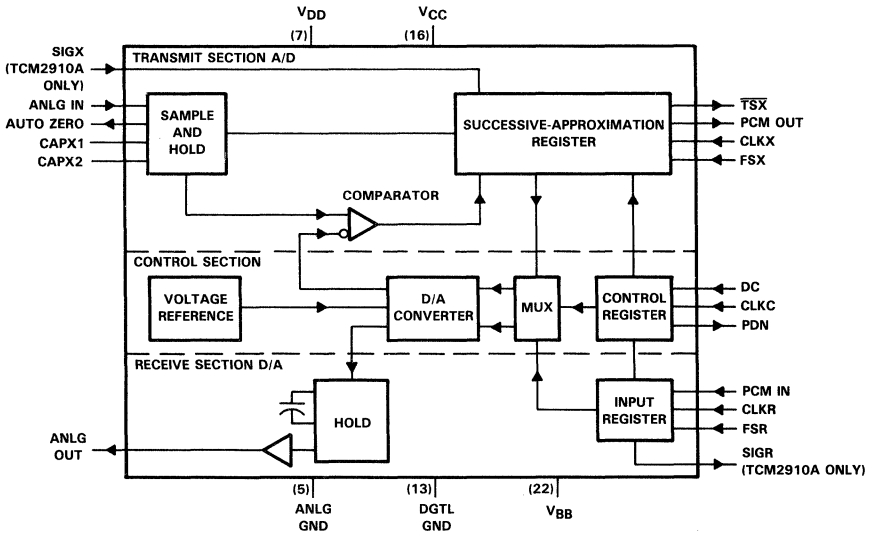
functional description

The TCM2909 and TCM2910A are designed to perform the transmit (encoding or A/D conversion) and receive (decoding or D/A) conversion) functions in a pulse-code-modulated system.

The functions of the codec are control, transmit, and receive. The control section consists of a precision voltage reference, a digital-to-analog converter, a multiplexer, and a control register. The voltage reference supplies the D/A-converter resistor ladder network with an accurate, stable reference. The analog output, in turn, is used to determine the A/D output as well as the D/A output. The control register multiplexes incoming receive and outgoing transmit data into the D/A converter.

The control section also enhances the basic codec function with programmable time-slot allocation and power-down circuits. These circuits allow dynamic allocation of both receive and transmit time slots. In small systems this feature could significantly reduce per-channel hardware for the first level of switching. In larger systems the time-slot selection circuits can be disabled, and time-slot allocation can be performed at a common system location. With either system design, the codec can be powered down during periods of inactivity, thereby significantly reducing average system power consumption.

functional block diagram



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NAME	PIN TCM2909	PIN TCM2910A	DESCRIPTION
ANLG GND	5	5	Analog return common to the transmit and receive analog circuits. Not connected to DGTL GND internally.
ANLG IN	3	3	Analog input to be encoded into a PCM word. The signal on this pin is sampled at the same rate as the transmit frame synchronization pulse, FSX, and the sample value is held in the external capacitors connected at the CAPX1 and CAPX2 pins.
ANLG OUT	9	10	Analog output. The voltage present on this pin is the decoded value of the PCM word received on PCM IN and is held constant between two conversions.
AUTO ZERO	4	4	This output is the same as the most significant bit of the encoded PCM word (5 V for negative, −5 V for positive inputs).
CAPX1	1	1	Connection for the transmit holding (analog sampling) capacitor.
CAPX2	2	2	Connection for the transmit holding (analog sampling) capacitor.
CLKC	22	24	Clock input to clock in the data on the DC pin that defines the mode of operation of the codec. When CLKC is connected to V_{CC}, DC becomes an active-low chip select. TTL-compatible.
CLKR	16	17	Clock input that defines the bit rate on the receive PCM highway (1.544 megabits per second for a T1 carrier). The maximum rate is 2.1 megabits per second at 50% duty cycle. TTL-compatible.
CLKX	18	19	Transmit clock input defining the bit rate on the transmit PCM highway. It is typically 1.544 megabits per second. Maximum rate is 2.1 megabits per second at 50% cycle. TTL-compatible.
DC	21	23	Data input to program the codec for either the direct or microcomputer mode of operation. TTL-compatible.
DGTL GND	12	13	Ground return common to the logic power supply, V_{CC}.
FSR	17	18	Frame synchronization pulse for the receive PCM highway. Resets the internal time-slot counter for the receive section. Maximum frame synchronization repetition rate is 12 kHz. Also used to differentiate between nonsignaling frames and signaling frames for the receive side. TTL-compatible.
FSX	19	20	Frame synchronization pulse for the transmit PCM highway. Resets the internal time-slot counter for the transmit section. Maximum repetition rate is 12 kHz. Also used to differentiate between nonsignaling frames and signaling frames on the transmit section. TTL-compatible.
NC	10	11	No internal connection. It is recommended that this pin be connected to ANLG GND.
NC	11	12	No internal connection. It is recommended that this pin be connected to ANLG GND.
PCM IN	7	8	Receive PCM highway (serial bus) interface. The codec serially receives a PCM word (8 bits) through this pin at the time defined by FSR, CLKR, and the contents of the receive control register.
PCM OUT	13	14	Output of the encoder onto the PCM highway. The 8-bit PCM word is serially sent out as defined by FSX, CLKX, and the control register. TTL three-state output capable of driving two TTL loads (4 mA).
PDN	8	9	Power-down output is active (high) when the codec is in the power-down state. The open-drain output is capable of sinking one TTL load (1.6 mA).
SIGR		6	Signaling output SIGR is updated with the 8th bit of the receive PCM word on signaling frames, and is latched between two signaling frames. TTL-compatible.
SIGX		21	Signaling input. This digital input is transmitted as the 8th bit of the PCM word on the PCM OUT pin in signaling frames. TTL-compatible.
$\overline{TSX}$	14	15	Normally high, the transmit time-slot output goes low while the codec is transmitting a PCM word on PCM OUT. Time-slot information is used for diagnostic purposes and also to gate the data on the PCM OUT pin to the PCM transmit highway. The open-drain output is capable of sinking two TTL loads (3.2 mA).
V_{BB}	20	22	Supply voltage (−5 V ±5%) referenced to ANLG GND.
V_{CC}	15	16	Supply voltage (5 V ±5%) referenced to DGTL GND.
V_{DD}	6	7	Supply voltage (12 V ±5%) referenced to ANLG GND.

operation

The TCM2909 and TCM2910A are capable of operating as transmitters and receivers in any of the 64 channels of a PCM system. The receive and transmit sections can be assigned to the same channel (time slot) or to different channels, and assignments can be changed under microcomputer control to meet changing system needs. Table 1 shows the control options.

TABLE 1. OPERATION CONTROL CONFIGURATIONS

CONTROL SIGNALS		OPERATION
CLKC	DC	
L	X	Undefined operation
V_{CC}	H	Power-down or standby operational status
V_{CC}	L	Direct-control operation. Receive and transmit in the first time slot.
↓	X	Microcomputer-control operation. Clock in one of 8 bits of the control word at the DC input.

Bits 1 and 2 (See Figure 3)

0	0	Load bits 3 through 8 into transmit and receive time-slot counters.
0	1	Load bits 3 through 8 into transmit counter only.
1	0	Load bits 3 through 8 into receive counter only.
1	1	Power down (Bits 3 through 8 are irrelevant).

Bits 3 through 8 for time-slot assignments 1 through 64. The time-slot numbers equal one more than the decimal equivalent represented by bits 3 (MSB) through 8 (LSB) using positive logic.

Time slot	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8
1	0	0	0	0	0	0
2	0	0	0	0	0	1
•	•	•	•	•	•	•
6	0	0	0	1	0	1
•	•	•	•	•	•	•
63	1	1	1	1	1	0
64	1	1	1	1	1	1

H = high level, L = low level, see digital interface table.
X = irrelevant, ↓ = V_{CC}-to-low transition.

In microcomputer control operation, the control word at DC is divided into a mode selection (bits 1 and 2) and a time-slot assignment (bits 3 through 8). In mode 00 both the receive and transmit time-slot counters are addressed, and they both receive the same subsequent 6-bit time-slot assignment. In mode 01 the transmit time-slot counter is addressed for time-slot assignment. Mode 10 assigns a time-slot only for the receive section. Mode 11 puts the device in the standby operational status and ignores the remaining 6 bits of the control word. Specific functional considerations for microcomputer-control operation are:

- All 8 negative-going transitions of CLKC must occur within 125 microseconds for the frame rate of 8 kilobits per second. The first transition of CLKC may occur anywhere within a frame. The CLKC pin should be a TTL low level after time-slot assignment is completed.
- A dead period of 250 microseconds (2 frames) must be observed between the first positive transition of CLKC in a time-slot assignment and that of any subsequent time-slot assignment.
- It is recommended that either mode 00 or mode 01 be transmitted to the control register during power-up or system initialization to ensure that a valid time-slot is always transmitted.

- The receive or the transmit section of the codec will operate only after both sections have been assigned a time-slot. Therefore, transmit-only and receive-only time-slot allocation is not allowed.
- Clocking the control register while the codec is active may cause an increase in idle-channel noise.

Direct-control operation is implemented by connecting the CLKC pin to +5 volts (V_{CC}) and using the DC pin as the chip select pin. When the DC pin is held low, the device transmits in the channel following FSX and receives in the channel following FSR. On the other hand, when the DC pin is held high, the device is in the power-down state. Operational considerations for direct time-slot allocation are:

- At least two framing pulses must occur after DC goes low to ensure that the codec is in direct-control status.
- Three frames (375 microseconds) are required to enter direct operation after power supply requirements are met and all clocks are available.
- After DC is brought high, two framing pulses are required to put the codec into the standby mode.
- The TCM2909 or TCM2910A can replace a 2910 codec even though the CLKC characteristics are not the same for the two devices.

encoding mode

The analog input signal sampled at the ANLG IN pin is held by an external capacitor on pins CAPX1 and CAPX2. This sampling is done synchronously with the transmit time-slot assigned to the device. The eight-bit digital PCM word will be transmitted on the PCM OUT pin in the frame immediately following the frame in which the analog signal was sampled. See Table 3.

decoding mode

When the assigned receive time-slot occurs, the eight-bit digital PCM word is retrieved from the PCM highway on the PCM IN pin. The word is converted from digital to analog and held with an internal capacitor until the next assigned receive time-slot update. See Table 3.

signaling

These devices are compatible with per-channel signaling and are capable of differentiating between the signaling and nonsignaling frames. A signaling frame is one in which the eighth bit of the PCM word contains signaling information while the seven most significant bits are normal information bits. The signaling frame is designated by the framing pulse (FSX or FSR) whose length is extended to two full clock periods as shown in the timing diagrams. A framing pulse of a nonsignaling frame is one full clock period in length. During a transmit signaling frame, the level present on the SIGX pin (of the TCM2910A) is substituted for the 8th bit of the PCM word. During a receive signaling frame the value of the 8th bit of the PCM word of the receive channel will be put on the SIGR pin (of the TCM2910A) and the signal level will remain unchanged until it is updated by the next signaling frame. The remaining 7 bits will be decoded according to the procedure in CCITT Recommendation G.733. See Figure 1 and Figure 2 for transmit and receive timing diagrams.

framing

These devices are compatible with the D3/D4 framing format (T1 framing), which inserts a 193rd bit after the 24th serial channel (8 bits per channel) frame. The extra bit raises the clock frequency (CLKX and CLKR) from 1.536 MHz to 1.544 MHz.

standby operation

The codec provides for powering down to standby status from both microcomputer-control and direct-control operation. The power consumption is reduced from 230 mW to 33 mW. Standby operation results in the powering down of all the codec functions except the DC, CLKC, SIGX†, SIGR†, and PDN inputs. Also, PCM OUT is forced into a high-impedance state thus helping to ensure that the PCM bus will not be driven. The SIGR† output is held low to provide a known condition until changed by a signaling frame after reactivation.

In microcomputer-control operation, the power-down state is invoked by clocking in 11 at the DC inputs as described in Table 1. In direct operation the power-down state is called by taking the DC pin high and connecting clock CLKC pin to V_{CC}. Recovery from the power-down condition is accomplished by forcing DC to the low level and allowing at least 2 frame synchronization pulses to occur.

internal reset

The TCM2909 and TCM2910A are designed to aid the user by eliminating certain system power-interruption problems. Three of the most common of these problems are:

(1) Plugging a card into a "hot" system thus causing spikes on the common power supplies
(2) Various transients such as caused by duplicated power supply faults or power feeder faults
(3) Transients and spikes that result from turning the power supplies on.

These devices are tolerant of transients in the negative power supply (V_{BB}) provided that V_{BB} remains more negative than −3.5 volts. The device will go into the power-down (standby) status if, during power up (single-card or system), V_{CC} or V_{DD} is supplied after V_{BB} or if a transient causes the positive power supplies to drop below approximately 2 volts. Since $\overline{TSX}$ is inhibited in standby operation, any codec in this status can be detected easily.

companding

The amplitude distribution of a speech message is not uniform. Moreover, the probability of occurrence for a small amplitude is greater than the probability for large amplitudes. Advantage can be taken of this fact by "compressing" digital resolution into the lower signal amplitude during transmission and "expanding" the signal upon the reception, thus increasing the overall signal-to-noise ratio. CCITT has defined this function and entitled it the μ-law.

$$f(x) = \text{sgn}(x)\,\frac{\ln + [1 + \mu|x|]}{\ln (1 + \mu)} \quad \text{for: } -1 \leq x \leq 1$$

where $\mu = 255$, x is the normalized input, and sgn(x) is the sign of x. A continuous implementation of f(x) would be impossible, therefore a piecewise continuous approximation of f(x) is used. The approximation divides the function into 16 segments, and each segment is divided into 16 equal intervals except for the first interval of the first segment. Refer to CCITT Recommendation G.711 for the segment and interval implementation details of the μ-law used for these circuits.

† TCM2910A only

absolute maximum ratings

V_{CC}, V_{DD}, ANLG GND, and DGTL GND with respect to V_{BB} . . . . . −0.3 V to 20 V
All inputs and outputs with respect to V_{BB} . . . . . −0.3 V to 20 V
Temperature under bias . . . . . −10°C to 80°C
Storage temperature range . . . . . −65°C to 150°C

NOTE: Stresses in excess of absolute maximum ratings may permanently damage the device. Functional operation outside the recommended operating conditions is not guaranteed. Prolonged exposure to absolute maximum ratings may have an adverse effect on device characteristics.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD} (see Note 1)	11.4	12	12.6	V
Supply voltage, V_{CC}	4.75	5	5.25	V
Supply voltage, V_{BB}	−4.75	−5	−5.25	V
Ground voltages (ANLG GND and DGTL GND)		0		V
Auto-zero resistor, R1 (see Figures 9 and 10)			150	kΩ
Auto-zero resistor, R2 (see Figures 9 and 10)			330	Ω
Auto-zero resistor, R3 (see Figures 9 and 10)			470	kΩ
Analog coupling capacitor, C1 (see Figures 9 and 10)			0.1	μF
Analog coupling capacitor, C2 (see Figure 10)			0.3	μF
Analog sampling capacitor, CAPX, for 8-kHz sampling rate (see Figures 9 and 10)	1600	2000	2400	pF
Operating free-air temperature, T_A	0		70	°C

NOTE 1: Voltages at the analog input, analog output, and V_{DD} terminals are with respect to the analog ground terminal. All other voltages are referenced to the digital ground terminal unless otherwise noted.

electrical characteristics over recommended ranges of operating free-air temperature and supply voltages (unless otherwise noted)

digital interface

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{IH}	High-level input voltage			2		V
V_{IL}	Low-level input voltage				0.6	V
I_{IH}	High-level input current		V_I = 5.5 V		10	μA
I_{IL}	Low-level input current		V_I = 0 V		−10	μA
V_{OH}	High-level output voltage (see Note 2)	PCM OUT	I_{OH} = 15 mA	2.4		V
		SIGR†	I_{OH} = 80 μA	2.4		
V_{OI}	Low-level output voltage	PCM OUT	I_{OL} = 4 mA		0.4	V
		SIGR†	I_{OL} = 0.5 mA		0.4	
		PDN	I_{OL} = 1.6 mA		0.4	
		$\overline{TSX}$	I_{OL} = 3.2 mA		0.4	

analog interface

PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
Analog-input impedance (between ANLG IN and CAPX1) in series with CAPX to ANLG GND during sampling of ANLG IN	V_I = −3.1 V to 3.1 V	125	300	500	Ω
Small-signal impedance at ANLG OUT	V_O = −3.1 V to 3.1 V	100	180	300	Ω
Decoder output offset voltage	Serial 11111111 to PCM IN	−50		50	mV
Encoder input offset voltage (see Note 3)	Serial 11111111 from PCM OUT	−5	1.5	5	mV
Peak negative output voltage at auto zero§	400 kΩ to ANLG GND	V_{BB}+2	V_{BB}		V
Peak positive output voltage at auto zero		V_{CC}−2	V_{CC}		V

power supplies

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
I_{DD1}	V_{DD} standby current	V_{DD} = 12.6 V, V_{CC} = 5.25 V, V_{BB} = −4.75 V, f_{CLK} = 2.048 MHz, See Note 4		0.7	1.1	mA
I_{CC1}	V_{CC} standby current			4	7	mA
I_{BB1}	V_{BB} standby current			−1.4	−2.5	mA
I_{DD2}	V_{DD} operating current			11	16	mA
I_{CC2}	V_{CC} operating current			13	21	mA
I_{BB2}	V_{BB} operating current			−4	−7.5	mA

† TCM2910A only.

‡ Typical values are at V_{DD} = 12 V, V_{CC} = 5 V, V_{BB} = −5 V, and T_A = 25°C.

§ Limits are expressed as magnitudes. For example, if V_{BB} = −5 V, the typical value is −5 V and the minimum value is −3 V.

NOTES: 2. PDN and $\overline{TSX}$ outputs are open-drain n-channel transistors that only sink current to DGTL GND. External pull-up devices are required to source current.

3. External auto-zero must be used when the required input offset is less than ±4 code steps or approximately 2.7 mV. The external auto-zero circuit shown in Figure 10 will bias the codec at the zero-crossing point and reduce the input offset voltage to zero.

4. These measurements apply to the microcomputer and direct modes. All output pins are left open, the dc input (pin 23) is at 5 V for standby current and at 0 V for operating current. All other input pins are grounded with the clocks operating.

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operating characteristics over recommended ranges of supply voltages and operating free-air temperature, R_L = 600 Ω (unless otherwise noted)

gain and dynamic range

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Digital milliwatt response	Nominal supply voltages, T_A = 25°C, See Note 5 and Figure 6	5.53	5.63	5.73	dBm
Temperature coefficient of digital milliwatt response	Nominal supply voltages, See Note 5		−0.001	−0.002	dB/°C
Change in digital milliwatt response	Supply voltages changing ±5%, T_A = 25°C, See Note 5			±0.07	dB
RMS input dynamic voltage range using dc and ac tests	Nominal supply voltages, T_A = 25°C, See Note 6 and Figure 6	2.17	2.20	2.23	V
Temperature coefficient of RMS input dynamic voltage range	Nominal supply voltages, See Note 6			−0.5	mV/°C
Change in RMS input dynamic voltage range	Supply voltages changing ±5%, T_A = 25°C, See Note 6			±18	mV
RMS output dynamic voltage range	Nominal supply voltages, T_A = 25°C	2.13	2.16	2.19	V
Temperature coefficient of RMS output dynamic voltage range	Nominal supply voltages			−0.5	mV/°C
Change in RMS output dynamic voltage range	Supply voltages changing ±5%, T_A = 25°C			±18	mV
Self-loop gain	P_I = 0 dBm0 at 1.02 kHz, See Note 7 and Figure 5		−0.2		dB

† Typical values are at V_{DD} = 12 V, V_{CC} = 5 V, V_{BB} = −5 V, and T_A = 25°C.

NOTES: 5. The input to PCM IN is a repetitive digital word sequence specified in CCITT Recommendation G.711. Measurement is made at ANLG OUT. Limits are not corrected for (six x)/x degradation and no C-message-weighted filter is used. See Table 2.

6. In the dc procedure, the positive and negative clipping levels are measured and dynamic voltage range is calculated. In the ac procedure, a sinusoidal input signal to ANLG IN is used and input dynamic voltage range is measured directly.

7. The codec acts as both encoder and decoder (PCM OUT = PCM IN) in a digital loop-back configuration. Specified gain is in addition to normal (sin x)/x insertion loss. See Note 8.

8. In the term (sin x)/x

$$x = \pi \frac{\text{measurement frequency}}{\text{sampling frequency}}$$

gain tracking error at f = 1.02 kHz

PARAMETER	TEST CONDITIONS	MOST NEG.	MOST POS.	UNIT
End-to-end gain tracking error (see Figure 4)	P_I = −37 dBm0 to 0 dBm0	−0.4	0.4	dB
	P_I = −50 dBm0 to −37 dBm0	−0.8	0.8	
	P_I = −55 dBm0 to −50 dBm0	−2.4	2.4	
Half-channel gain tracking error (encoder only with ideal decoder) See Figure 6	P_I = −37 dBm0 to 0 dBm0	−0.3	0.3	dB
	P_I = −50 dBm0 to −37 dBm0	−0.9	0.9	
	P_I = −55 dBm0 to −50 dBm0	−1.5	1.5	
Half-channel gain tracking error (decoder only with ideal encoder) See Figure 6	P_I = −37 dBm0 to 0 dBm0	−0.3	0.3	dB
	P_I = −50 dBm0 to −37 dBm0	−0.9	0.9	
	P_I = −55 dBm0 to −50 dBm0	−1.5	1.5	

operating characateristics over recommended ranges of supply voltages and operating free-air temperature, R_L = 600 Ω (unless otherwise noted) (continued)

transmission characteristics (see Figure 6), f = 1.02 kHz (unless otherwise noted)

PARAMETER		MIN	TYP†	MAX	UNIT
Signal-to-total-distortion ratio, C-message weighting, end-to-end			See Figure 7		
Signal-to-total-distortion ratio, C-message weighting, (half-channel)			See Figures 6 & 7		
Harmonic distortion (2nd or 3rd overtone) measured at ANLG OUT, P_I = 0 dBm0 See Figure 6.			−48	−44	dB
Encoder idle-channel noise measured at mid-tread (no quantizing noise) C-message weighting with no signaling	No external auto zero See Figure 9		2	10	dBrncO
	With external auto zero See Figure 10		8		
Encoder idle-channel noise measured at the riser (quantizing noise included) C-message weighting, no signaling				17	dBrncO
Encoder idle-channel noise measured at mid-tread (no quantizing noise), C-message weighting, 6th and 12th frame signaling per AT&T System requirements	No external auto zero See Figure 9		10	13	dBrncO
	With external auto zero See Figure 10		13		
Decoder idle-channel noise, no sign-bit toggling, no signaling, quiet code (serial 11111111 to PCM IN)			−10	7	dBrncO
Decoder idle-channel noise with sign-bit toggling, no signaling, quiet code (serial 11111111 to PCM IN)			13	17	dBrncO

power supply rejection and crosstalk attenuation

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
SVRR1	V_{DD} supply voltage rejection ratio	Decoder alone,	See Note 9	45	55		dB
SVRR2	V_{BB} supply voltage rejection ratio	Decoder alone,	See Note 9	35	38		dB
SVRR3	V_{CC} supply voltage rejection ratio	Decoder alone,	See Note 9	50	80		dB
SVRR4	V_{DD} supply voltage rejection ratio	Encoder alone		50	75		dB
SVRR5	V_{BB} supply voltage rejection ratio	Encoder alone		45	70		dB
SVRR6	V_{CC} supply voltage rejection ratio	Encoder alone		50	85		dB
SVRR7	V_{DD} supply voltage rejection ratio	Self loop,	See Note 10	40	50		dB
SVRR8	V_{BB} supply voltage rejection ratio	Self loop,	See Note 10	35	38		dB
SVRR9	V_{CC} supply voltage rejection ratio	Self loop,	See Note 10	50	80		dB
a_x	Crosstalk attenuation	See Figure 8,	See Note 11	75	>80		dB

clock timing requirements over recommended ranges of operating conditions (see Note 12)

PARAMETER		MIN	MAX	UNIT
$t_{c(CLK)}$	Clock period for CLKX, CLKR (2.048-MHz systems)	485		ns
t_r, t_f	Rise and fall times for CLKX, CLKR, and CLKC	5	30	ns
$t_{w(CLK)}$	Clock pulse duration for CLKX, CLKR, and CLKC	215		ns
	Clock duty cycle [$t_{w(CLK)}/t_{c(CLK)}$] for CLKX and CLKR	45	55	%

† Typical values are for T_A = 25°C and nominal power supply voltages.

NOTES: 9. With the test device acting as a decoder, a 200-mV peak-to-peak, 1,02 kHz signal is applied to the appropriate supply pin and measurements are made at the remote encoder output with the decoder in idle-channel conditions.

10. With the test device acting as encoder and decoder, a 200-mV peak-to-peak, 1.02-kHz signal is applied to the appropriate supply pin and measurements are made at the decoder output with the encoder in idle-channel conditions.

11. The analog input power is 0 dBm0 at 1.02 kHz and the decoder is under idle-channel conditions. Measurement is made at ANLG OUT.

12. All timing parameters are referenced to 2 V except t_{pd3} and t_{pd5}, which reference a high-impedance state.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

transmit timing requirements over recommended ranges of operating conditions (see Note 12)

PARAMETER		MIN	MAX	UNIT
$t_{conv(X)}$	Analog input conversion time referenced to leading edge of transmit time slot (see Note 13)	20		time slots
$t_{d(FSX)}$	Frame sync delay time	20	150	ns
$t_{su(SIGX)}$	Setup time before Bit 7 falling edge	0		ns
$t_{h(SIGX)}$	Hold time after Bit 8 falling edge	100		ns

receive timing requirements over recommended ranges of operating conditions (see Note 12)

PARAMETER		MIN	MAX	UNIT
$t_{conv(R)}$	Analog output update from leading edge of the channel time slot	7 1/16		time slots
$t_{d(FSR)}$	Frame sync delay time	20	150	ns
$t_{su(PCM\ IN)}$	Receive data setup time	20		ns
$t_{h(PCM\ IN)}$	Receive data hold time	60		ns

control (microcomputer operation) timing requirements over recommended ranges of operating conditions

PARAMETER		MIN	MAX	UNIT
$t_{su(DC)}$	Control data setup time	100		ns
$t_{h(DC)}$	Control data hold time	100		ns

propagation delay times over recommended ranges of operating conditions (see Note 12 and timing diagrams)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{pd1}	From rising edge of transmit clock Bit 1 to Bit 1 data valid at PCM OUT (data enable time on time-slot entry)	C_L = 0 to 100 pF	50	180	ns
t_{pd2}	From falling edge of transmit clock Bit n to Bit n+1 data valid at PCM OUT (data valid time)	C_L = 0 to 100 pF	80	230	ns
t_{pd3}	From falling edge of transmit clock Bit 8 to Bit 8 Hi-Z at PCM OUT (data float time on time-slot exit)	C_L = 0, See Note 13	75	245	ns
t_{pd4}	From rising edge of transmit clock Bit 1 to $\overline{TSX}$ active (low) (time-slot enable time)	C_L = 0 to 100 pF	30	220	ns
t_{pd5}	From falling edge of transmit clock Bit 8 to $\overline{TSX}$ inactive (high) (time-slot disable time)	C_L = 0, See Note 13	70	225	ns
t_{pd6}	From falling edge of receive clock Bit 8 on signaling frames to updated signaling bit on SIGR output (receive signaling update time)			1000	ns

NOTES: 12. All timing parameters are referenced to 2 V except t_{pd3} and t_{pd5}, which reference a high-impedance state.
13. The 20-time-slot minimum ensures that the complete A/D conversion will take place under any combination of receive interrupt of asynchronous operation of the codec. If only the transmit channel is operated, the A/D conversion can be completed in a minimum of 11 time slots.

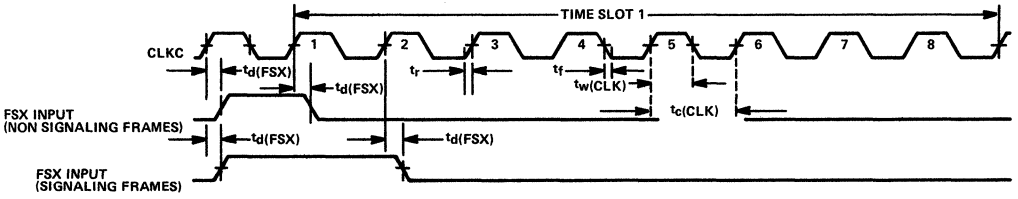

FIGURE 1a. TRANSMIT FRAME SYNCHRONIZATION TIMING

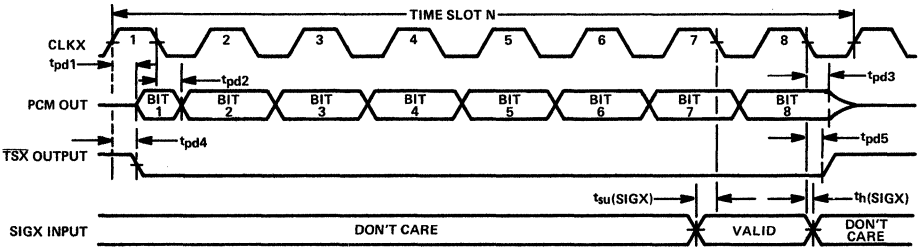

FIGURE 1b. TRANSMIT OUTPUT TIMING

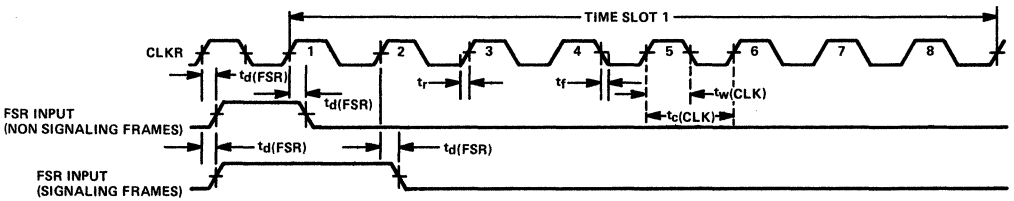

FIGURE 2a. RECEIVE FRAME SYNCHRONIZATION TIMING

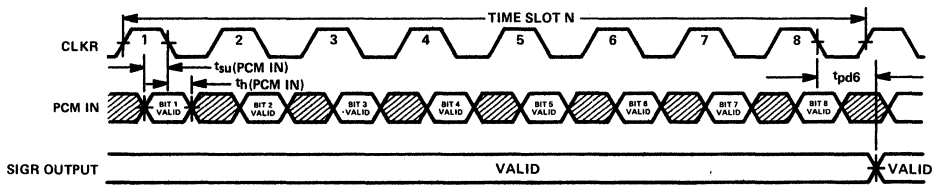

FIGURE 2b. RECEIVE INPUT TIMING

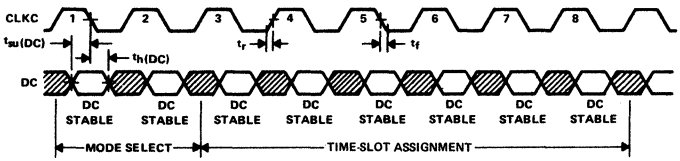

FIGURE 3. CONTROL TIMING

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POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

PARAMETER MEASUREMENT INFORMATION

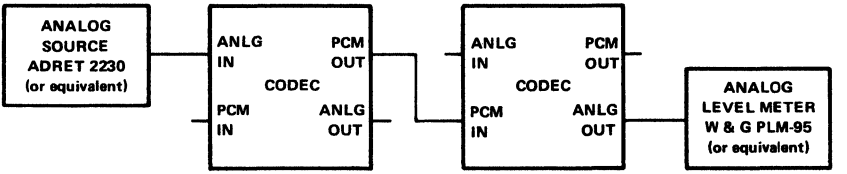

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FIGURE 4. END-TO-END GAIN TEST CIRCUIT

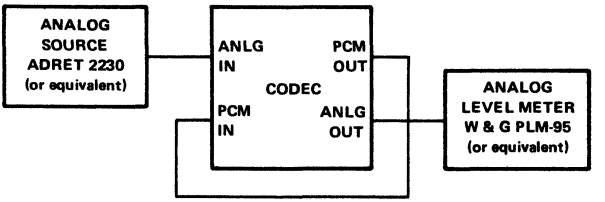

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FIGURE 5. SELF-LOOP GAIN TEST CIRCUIT

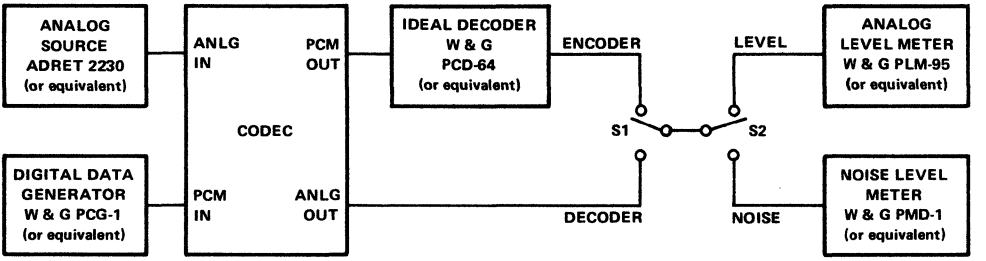

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FIGURE 6. TRANSMISSION PARAMETER TEST CIRCUIT

PARAMETER MEASUREMENT INFORMATION

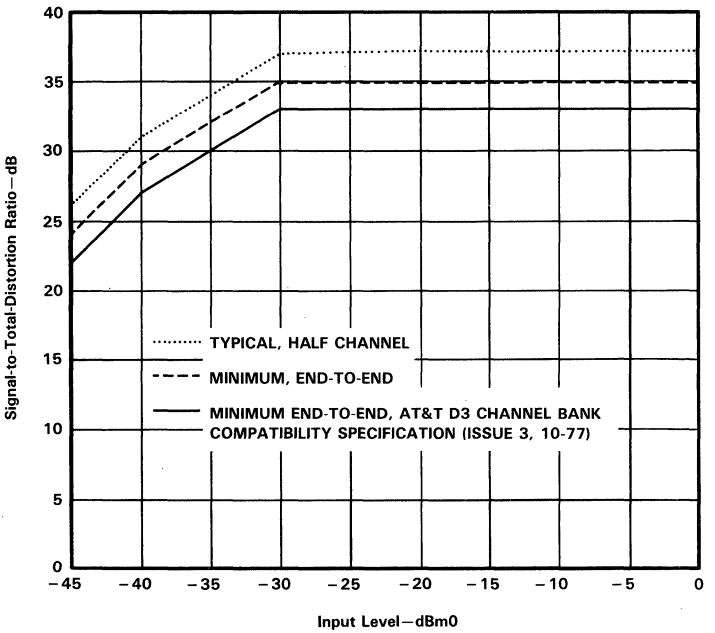
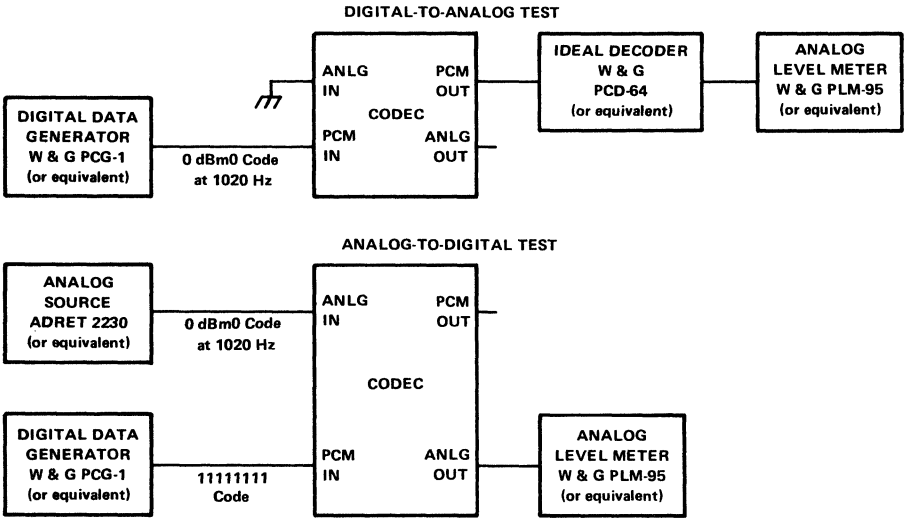


FIGURE 7. SIGNAL-TO-TOTAL DISTORTION RATIO

PARAMETER MEASUREMENT INFORMATION



W & G: WANDEL AND GOLTERMANN

FIGURE 8. CROSSTALK ATTENUATION TEST CIRCUIT

TABLE 2. μ-LAW DIGITAL WORD SEQUENCE FOR THE DIGITAL MILLIWATT RESPONSE PER CCITT RECOMMENDATION G.711

		Bit Number							
		1	2	3	4	5	6	7	8
Word Number	1	0	0	0	1	1	1	1	0
	2	0	0	0	0	1	0	1	1
	3	0	0	0	0	1	0	1	1
	4	0	0	0	1	1	1	1	0
	5	1	0	0	1	1	1	1	0
	6	1	0	0	0	1	0	1	1
	7	1	0	0	0	1	0	1	1
	8	1	0	0	1	1	1	1	0

TYPICAL APPLICATION INFORMATION

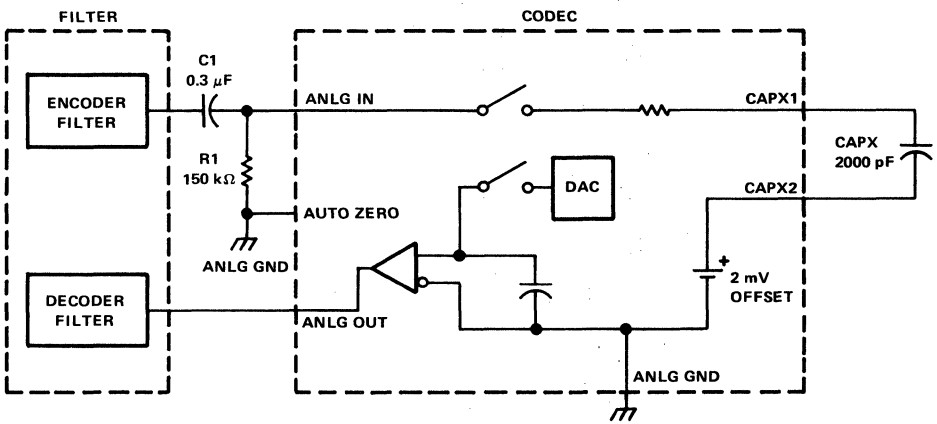


FIGURE 9. ANALOG INTERFACE WITHOUT EXTERNAL AUTO ZERO

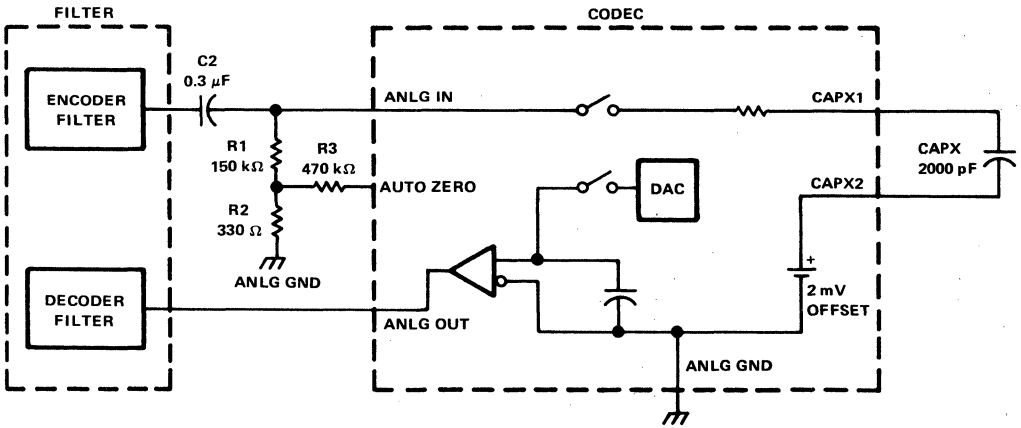


FIGURE 10. ANALOG INTERFACE WITH EXTERNAL AUTO ZERO

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TYPICAL APPLICATION INFORMATION

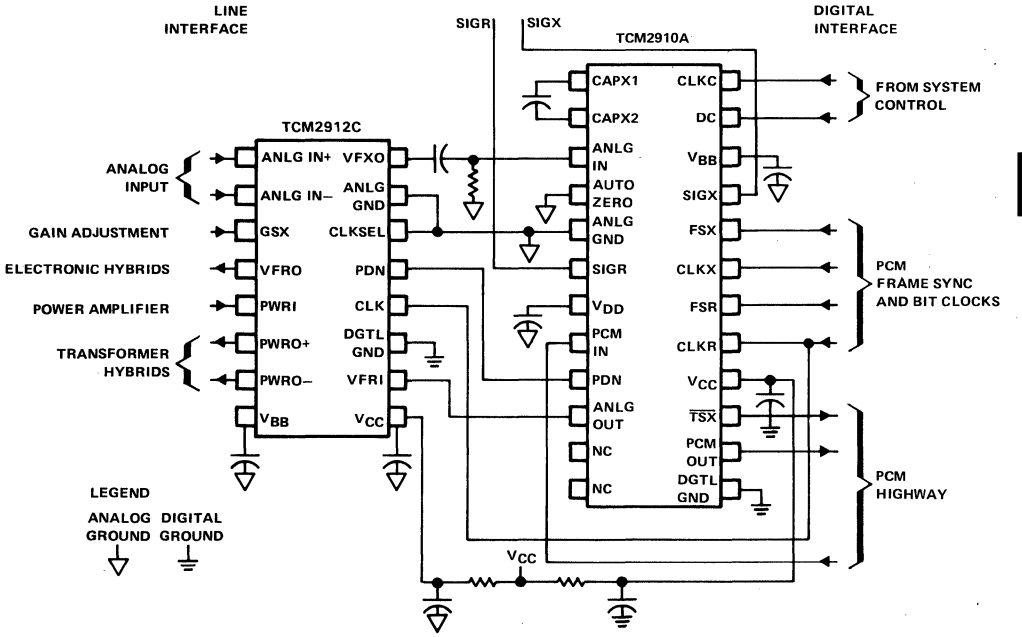

FIGURE 11. TCM2910A INTERFACE WITH TCM2912C FILTER

TABLE 3a. μ-LAW POSITIVE INPUT VALUES
Reproduced from CCITT† (Volume III — 2 on Line Transmission) Recommendation G.711 on Pulse Code Modulation of Voice Frequencies

1	2	3	4	5	6	7	8
Segment number	Number of intervals × interval size	Value at segment end points	Decision value number n	Decision value x_n (see Note A)	Character signal (see Note B) — Bit number 1 2 3 4 5 6 7 8	Value at decoder output y_n (see Note C)	Decoder output value number
		8159	(128)[D]	(8159)			
			127	7903	1 0 0 0 0 0 0 0	8031	127
8	16 × 256				(see Note E)		
			113	4319			
		4063	112	4063	1 0 0 0 1 1 1 1	4191	112
7	16 × 128				(see Note E)		
			97	2143			
		2015	96	2015	1 0 0 1 1 1 1 1	2079	96
6	16 × 64				(see Note E)		
			81	1055			
		991	80	991	1 0 1 0 1 1 1 1	1023	80
5	16 × 32				(see Note E)		
			65	511			
		479	64	479	1 0 1 1 1 1 1 1	495	64
4	16 × 16				(see Note E)		
			49	239			
		223	48	223	1 1 0 0 1 1 1 1	231	48
3	16 × 8				(see Note E)		
			33	103			
		95	32	95	1 1 0 1 1 1 1 1	99	32
2	16 × 4				(see Note E)		
			17	35			
		31	16	31	1 1 1 0 1 1 1 1	33	16
	15 × 2				(see Note E)		
			2	3			
1					1 1 1 1 1 1 1 0	2	1
↓	1 × 1		1	1	1 1 1 1 1 1 1 1		
			0	0		0	0

NOTES: A. 8159 normalized value units correspond to the value of the on-chip voltage reference.
B. The PCM word on the highways is the same as the one shown in column 6.
C. The voltage output on the ANLG OUT lead is equal to the normalized value given in the table, augmented by an offset. The offset value is approximately 15 mV.
D. X_{128} is a virtual decision value.
E. The PCM word corresponding to positive input values between two successive decision values numbered n and n + 1 (see column 4) is (255 − n) expressed as a binary number.

†The International Telegraph and Telephone Consultative Committee. Published by the International Telecommunication Union, Geneva, Switzerland.

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TABLE 3b. μ-LAW NEGATIVE INPUT VALUES
Reproduced from CCITT† (Volume III — 2 on Line Transmission) Recommendation G.711 on Pulse Code Modulation of Voice Frequencies

1	2	3	4	5	6	7	8
Segment number	Number of intervals × interval size	Value at segment end points	Decision value number n	Decision value x_n (see Note A)	Character signal (see Note B) Bit number 1 2 3 4 5 6 7 8	Value at decoder output y_n (see Note C)	Decoder output value number
▲			0	0		0	0
	1 × 1				0 1 1 1 1 1 1 1		
			1	−1			
1					0 1 1 1 1 1 1 0	−2	1
			2	−3			
	15 × 2				(see Note D)		
		−31	16	−31			
					0 1 1 0 1 1 1 1	−33	16
			17	−35			
2	16 × 4				(see Note D)		
		−95	32	−95			
					0 1 0 1 1 1 1 1	−99	32
			33	−103			
3	16 × 8				(see Note D)		
		−223	48	−223			
					0 1 0 0 1 1 1 1	−231	48
			49	−239			
4	16 × 16				(see Note D)		
		−479	64	−479			
					0 0 1 1 1 1 1 1	−495	64
			65	−511			
5	16 × 32				(see Note D)		
		−991	80	−991			
					0 0 1 0 1 1 1 1	−1023	80
			81	−1055			
6	16 × 64				(see Note D)		
		−2015	96	−2015			
					0 0 0 1 1 1 1 1	−2079	96
			97	−2143			
7	16 × 128				(see Note D)		
		−4063	112	−4063			
					0 0 0 0 1 1 1 1	−4191	112
			113	−4319			
					(see Note D)		
8	16 × 256		126	−7647			
					0 0 0 0 0 0 0 1	−7775	126
			127	−7903			
					0 0 0 0 0 0 0 0	−8031	127
		−8159	(128)E	(−8159)			

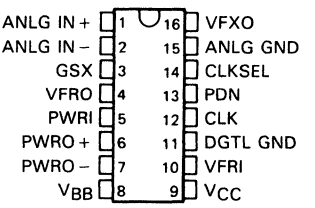
NOTES: A. 8159 normalized value units correspond to the value of the on-chip voltage reference.
B. The PCM word on the highways is the same as the one shown in column 6.
C. The voltage output on the ANLG OUT lead is equal to the normalized value given in the table, augmented by an offset. The offset value is approximately 15 mV.
D. The PCM word corresponding to positive input values between two successive decision values numbered n and n + 1 (see column 4) is (255 − n) expressed as a binary number.
E. X_{128} is a virtual decision value.

†The International Telegraph and Telephone Consultative Committee. Published by the International Telecommunication Union, Geneva, Switzerland.

D2788, SEPTEMBER 1983—REVISED DECEMBER 1987

- **High-Pass Transmit Filter for Rejection of All Low-Frequency Noise:**
  - **16 Hz . . . . . 70 dB Typical**
  - **50 Hz . . . . . 35 dB Typical**
  - **60 Hz . . . . . 30 dB Typical**
- **6th-Order Low-Pass Transmit Filter for Improved Performance**
- **Low Standby Power Consumption**
- **Improved Envelope Delay Characteristics**
- **Excellent Power Supply Rejection Ratio**
- **CCITT G.712 as well as AT&T D3/D4 Compatible**
- **TTL- and CMOS-Compatible**
- **Reliable N-Channel MOS Process**
- **Pin-For-Pin Functional Replacement for Intel 2912A**
- **Improved Noise Performance**
- **Three-State PWRO+ and PWRO− Outputs**

J
DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

The TCM2912C is a monolithic integrated circuit designed to implement the transmit and receive signal filters of a PCM line or trunk termination. The transmit and receive passband filter sections are implemented using switched capacitor techniques.

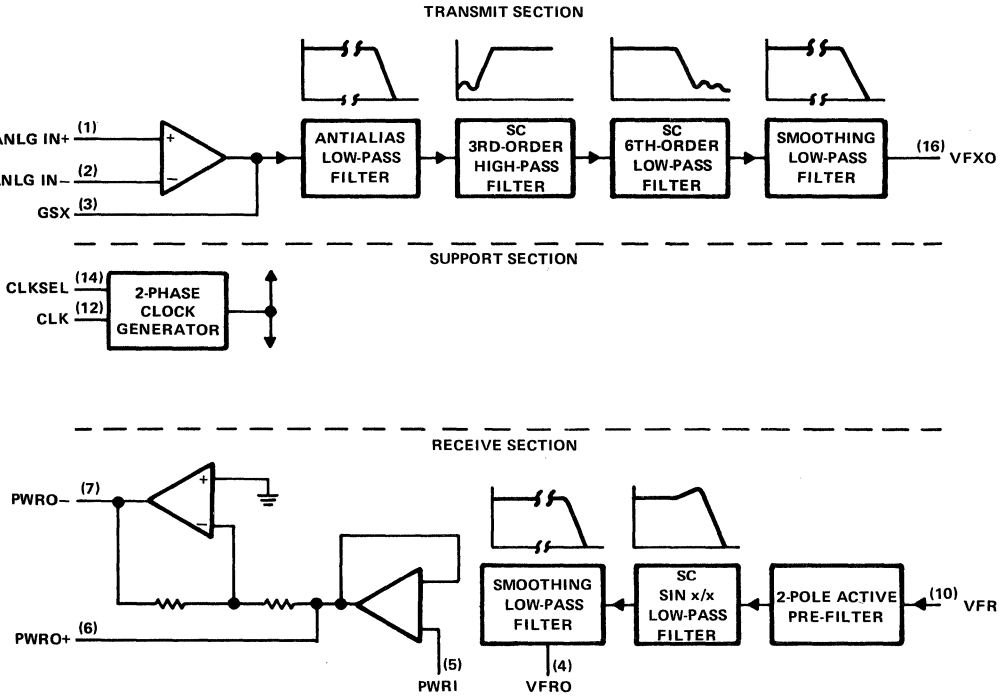
The TCM2912C is primarily used in telephone system applications for switching, transmission, and remote concentration. The transmit section provides a high-pass filter to ensure rejection of all low-frequency noise as well as the anti-aliasing function required for an 8 kHz sampling system. A sixth-order low-pass filter is provided in the transmit section for improved performance. The receive section has a smoothing low-pass filter and sin x/x correction required for interface with TCM2910A or TCM2911A codecs. The TCM2912C eliminates high-frequency switching noise for direct interface with transformer or electronic hybrids. The power-down mode (standby) can be directly controlled by TCM2910A or TCM2911A type codecs. When the TCM2912C is in the power-down mode, all outputs are in a high-impedance state.

The -3 versions are identical to the standard versions except that gain relative to gain at 1 kHz is −0.7 dBm minimum.

The TCM2912C is characterized for operation from 0°C to 70°C.

Caution. These devices have limited built-in gate protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

system block diagram



The TCM2912C system block diagram is divided into three sections: transmit, receive, and support. The transmit section provides bandpass filtering to eliminate unwanted switching and low-frequency noise signals. The receive section provides a 2-pole active pre-filter to filter out high-frequency components that are present on the analog output of the codec. Since the filter is a sampled data system, the components could alias down into the voice band and create low-frequency gain tracking and S/Q problems. Following the pre-filter is a sixth-order low-pass filter that provides sin x/x correction for the codec. The receive section provides sin x/x correction for the codec and elimination of high-frequency switching signals. The receive section has optional output buffers. The support section provides clock generation.

PIN NAME	NO.	DESCRIPTION
ANLG GND	15	Analog return common to the transmit and receive analog circuits. Not connected to DGTL GND internally.
ANLG IN−	2	Inverting input of the gain adjustment operational amplifier on the transmit filter
ANLG IN+	1	Analog input of the transmit filter. The ANLG IN+ signal comes from the 2- to 4-wire hybrid in the case of a 2-wire line and goes through the high-pass filter and antialiasing filter before being sent to the codec for encoding.
CLK	12	Clock input. Three clock frequencies can be used: 1.536 MHz, 1.544 MHz, or 2.048 MHz. Frequency is selected by CLKSEL (pin 14).
CLKSEL	14	Clock frequency selection. Input must be connected to V_{BB}, V_{CC}, or ground to reflect the master clock frequency at pin 12 (CLK). When tied to V_{BB}, CLK is 1.536 MHz. When tied to ground, CLK is 1.544 MHz. When tied to V_{CC}, CLK is 2.048 MHz.
DGTL GND	11	Digital ground return for internal clock generator.
GSX	3	Output of the gain adjustment operational amplifier on the transmit filter. Used for gain setting of the transmit filter.
PDN	13	Control input for standby power-down mode. An internal pullup to 5 volts is provided for interface to the codec PDN outputs.
PWRI	5	High-impedance input to the power driver amplifiers on the receive side of interface to transformer hybrids. When taken to the low level (tied to V_{BB}), the power amplifiers are powered down.
PWRO−	7	Inverting side of power amplifiers. Power driver output capable of directly driving transformer hybrids.
PWRO+	6	Noninverting side of the power amplifiers. Power driver output capable of directly driving transformer hybrids.
V_{BB}	8	−5 V ±5% referenced to ANLG GND
V_{CC}	9	5 V ±5% referenced to ANLG GND
VFRI	10	Analog input of the receive filter, interface to the codec analog output for PCM applications. The receive filter provides the sin x/x correction needed for sample-and-hold-type codec outputs to give unity gain. The input voltage range is directly compatible with TCM2910A codecs.
VFRO	4	Analog output of the receive filter. Provides a direct interface to electronic hybrids. For a transformer hybrid application, VFRO is tied to PWRI and a dual balanced output is provided on pins PWRO+ and PWRO−.
VFXO	16	Analog output of the transmit filter. The output voltage range is directly compatible with the TCM2910A codecs.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . −0.3 V to 14 V
Output voltage, V_O all outputs (see Note 1) . . . . . −0.3 V to 14 V
Output current, I_O (all outputs) . . . . . ±50 mA
Continuous total dissipation at 25°C free-air temperature (see Note 2) . . . . . 1375 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds . . . . . 300°C

NOTES: 1. Voltage values are with respect to V_{BB}.
2. For operation above 25°C free-air temperature, derate linearly to 880 mW at 70°C at the rate of 11 mW/°C.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (see Note 3)		4.75	5	5.25	V
V_{BB}	Supply voltage (see Note 3)		−4.75	−5	−5.25	V
	DGTL GND voltage with respect to ANLG GND			0		V
V_{IH}	High-level input voltage	All inputs except CLKSEL	2.2			V
V_{IL}	Low-level input voltage	All inputs except CLKSEL and PWRI			0.8	V
		PWRI	V_{BB}		$V_{BB}+0.5$	
	Clock select input voltage	For 2.048 MHz	$V_{CC}-0.5$		V_{CC}	V
		For 1.544 MHz	ANLG GND − 0.5		0.8	
		For 1.536 MHz	V_{BB}		$V_{BB}+0.5$	
R_L	Load resistance	At GSX, VFXO, or VFRO	10			kΩ
		At PWRO+ or PWRO− (single-ended)	300			Ω
		At PWRO+ and PWRO− (differential)	600			
C_L	Load capacitance	At GSX, VFXO, or VFRO			25	pF
		At PWRO+ or PWRO− (single-ended)			100	
		At PWRO+ and PWRO− (differential)			200	
T_A	Operating free-air temperature		0		70	°C

NOTE 3: Voltages at analog inputs, analog outputs, V_{CC}, and V_{BB} terminals are with respect to the ANLG GND terminal. All other voltages are referenced to the DGTL GND terminal unless otherwise noted.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature

digital interface

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
I_I	Input current	PDN	V_I = GND to V_{CC}		−100	μA
		CLKSEL	V_I = V_{BB} to 2.2 V		1	
		CLK	V_I = 0.8 V to 2.2 V		1	

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (continued)

supply current

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_{CC}	Supply current from V_{CC}	Standby	PDN at 2.2 V			0.4	mA
		Operating	Power amplifiers active		12	15	
		Operating	Power amplifiers inactive, PWRI at V_{BB}		9	11	
I_{BB}	Supply current from V_{BB}	Standby	PDN = 2.2 V			−0.4	mA
		Operating	Power amplifiers active		−12	−15	
		Operating	Power amplifiers inactive, PWRI at V_{BB}		−9	−11	

transmit amplifier input

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input leakage current at ANLG IN+, ANLG IN−	V_I = −2.2 V to 2.2 V			±100	nA
Input offset voltage at ANLG IN+, ANLG IN−				±25	mV
Output voltage swing at GSX	R_L = 10 kΩ	±2.5			V
Common-mode rejection at ANLG IN+, ANLG IN−	V_I = −1.6 V to 1.6 V (−3 dBm0)	60			dB
Common-mode rejection at ANLG IN+, ANLG IN−	V_I = −2.2 V to 2.2 V (0 dBm0)	60	90		dB
DC open-loop voltage amplification at GSX		72	77		dB
Open-loop unity gain bandwidth at GSX			1		MHz
Input resistance at ANLG IN+, ANLG IN−		10			MΩ

transmit filter

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
DC output offset voltage at VFXO	ANLG IN+ connected to ANLG GND, Amplifiers at unity gain			±100	mV
Output voltage swing at 1 kHz at VFXO	RL ≥ 10 kΩ	±3.2			V
Output resistance at VFXO			1	2	Ω

receive filter

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
DC output offset voltage at VFRO	VFRI connected to ANLG GND			±100	mV
Output voltage swing at VFRO	R_L = 10 kΩ	±3.2			V
Input leakage current at VFRI	V_I = −3.2 V to 3.2 V			1	μA
Input resistance at VFRI		1			MΩ
Output resistance at VFRO			1	2	Ω

† All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (continued)

receive filter driver amplifier

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
Output voltage across R_L at PWRO+, PWRO−	Single ended connection, R_L connected to ANLG GND	R_L = 10 kΩ	±3.2			V
		R_L = 600 Ω	±2.9			
		R_L = 300 Ω	±2.5			
Differential output voltage swing at PWRO+, PWRO−	Balanced connection, R_L connected between PWRO+ and PWRO−	R_L = 20 kΩ	±6.4			V
		R_L = 1200 Ω	+5.8			
		R_L = 600 Ω	+5			
DC output offset voltage at PWRO+, PWRO−	PWRI connected to ANLG GND				±50	mV
Input leakage current at PWRI	V_I = −3.2 V to 3.2 V				±0.5	μA
Input resistance at PWRI			10			MΩ
Output resistance at PWRO+, PWRO−	$I_O \leq$ 10 mA, V_O = −3 V to 3 V			1	2	Ω

power supply rejection (see Note 4)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
SVRR1	V_{CC} supply voltage rejection ratio	Transmit channel only	30	45		dB
SVRR2	V_{BB} supply voltage rejection ratio	Transmit channel only	30	45		dB
SVRR3	V_{CC} supply voltage rejection ratio	Receive channel only	30	45		dB
SVRR4	V_{BB} supply voltage rejection ratio	Receive channel only	30	45		dB

† All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C.

NOTE 4: With the test device acting as a transmitter (or receiver), a 200-mV peak-to-peak 1.02-kHz signal is applied to the appropriate supply pin and measurements are made at the VFXO (or VFRO) output with the receiver (or transmitter) and power amplifiers in idle channel conditions.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (continued)

transmit filter transfer

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
Gain relative to gain at 1 kHz with 0-dBm0 input signal	Gain-setting operational amplifier at unity gain, 0-dBm0 reference measured at VFXO (see Note 5)	16.67 Hz		−80	−60	dBm
		50 Hz			−30	
		60 Hz			−25	
		200 Hz	−1.2		−0.125	
		300 Hz to 3 kHz	−0.125		0.125	
		3.3 kHz	−0.35		0.1	
		3.4 kHz (TCM2912C-3)	−0.7		−0.1	
		3.4 kHz (TCM2912C)	−1		−0.1	
		4 kHz			−14	
		4.6 kHz and above			−35	
Absolute passband gain at VFXO	f = 1 kHz, R_L = 10 kΩ		2.8	3	3.2	dB
Gain variation with temperature	f = 1 kHz, Signal level = 0 dBm0			0.0008		dB/°C
Gain variation with supply voltage	f = 1 kHz, Signal level = 0 dBm0, Supply variation = ±5%			0.04		dB/V
Crosstalk attenuation, receive to transmit at VFXO	VFRI = 1.6 V rms, f = 1 kHz, ANLG IN− connected to GSX, ANLG IN+ connected to ANLG GND		70	80		dB
Single-frequency distortion products	f = 1 kHz, Signal level = 0 dBm0 at VFXO				−48	dB
	f = 1 kHz, Signal level = 3 dBm0 at VFXO Gain-setting operational amplifier at 20-dB gain				−45	
Total C-message noise at VFXO	Gain setting operational amplifier at unity gain			4	6	dBrnC0
	Gain setting operational amplifer at 20-dB gain			4	6	
Differential envelope delay time	f = 1 kHz to 2.6 kHz			60	80	μs
Absolute delay time				100	150	μs

†All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C.
NOTE 5: A 0-dBm0 signal is equivalent to 1.1 V rms at ANLG IN+ and 1.6 V rms output at VFXO.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (continued)

receive filter transfer

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
Gain relative to 1 kHz with 0 dBm0 input signal		0 dBm0 measured at VFRO	below 200 Hz	−0.2		0.125	dBm
			200 Hz	−0.2		0.125	
			300 Hz to 3 kHz	−0.125		0.125	
			3.3 kHz	−0.35		0.03	
			3.4 kHz (TCM2912-3)	−0.7		−0.1	
			3.4 kHz (TCM2912)	−1		−0.1	
			4 kHz			−14	
			4.6 kHz and above			−35	
Absolute passband gain at VFRO		f = 1 kHz, R_L = 10 kΩ		−0.2		0.2	dB
Gain variation with temperature		f = 1 kHz, Signal level = 0 dBm0			0.0002		dB/°C
Gain variation with supply voltage		f = 1 kHz, Signal level = 0 dBm0, Supply variation = ±5%			0.04		dB/V
Crosstalk attenuation, transmit to receive at VFRO		ANLG IN− connected to GSX, ANLG IN+ at 1.1 V rms, f = 1 kHz, VFRI connected to ANLG GND		70	76		dB
Single-frequency distortion products		f = 1 kHz, Input signal = 0 dBm0				−48	dB
		f = 1 kHz, Input signal = 3 dBm0				−45	
Total C-message noise at VFRO		Measured at VFRO			4	6	dBrnC0
Differential envelope delay time		f = 1 kHz to 2.6 kHz			25	80	μs
Absolute delay time	VFRO				110	140	μs
	PWRO−				120	180	

†All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C

TRANSFER CHARACTERISTICS OF THE
TRANSMIT SECTION

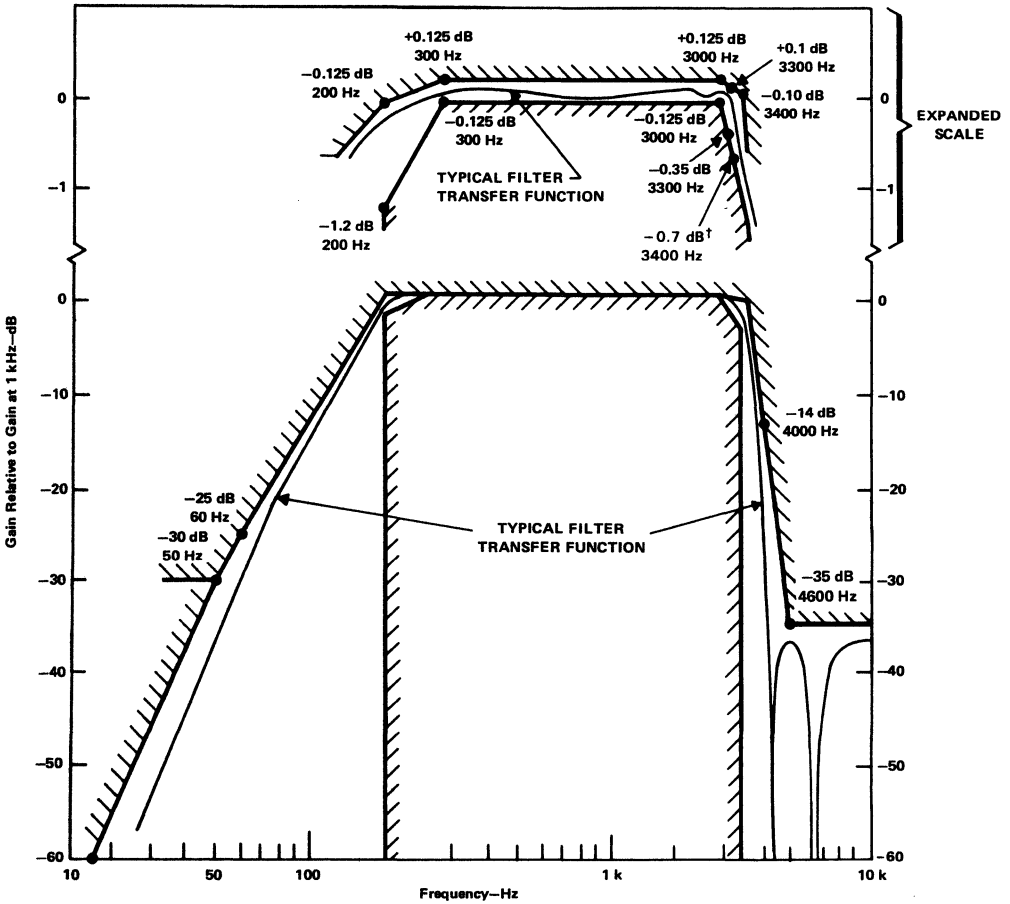


FIGURE 1

†Applies to the TCM2912C-3 only.

TRANSFER CHARACTERISTICS OF THE
RECEIVE SECTION

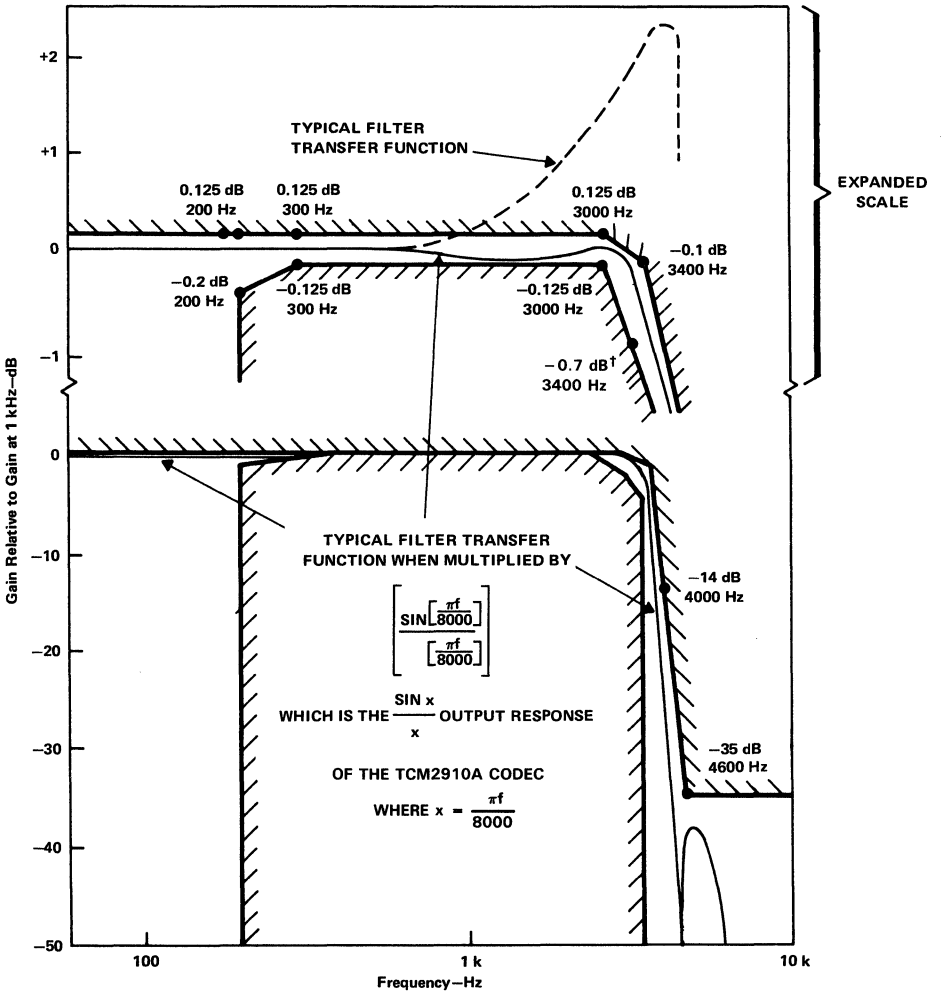
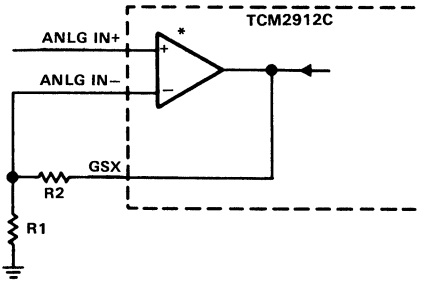


FIGURE 2

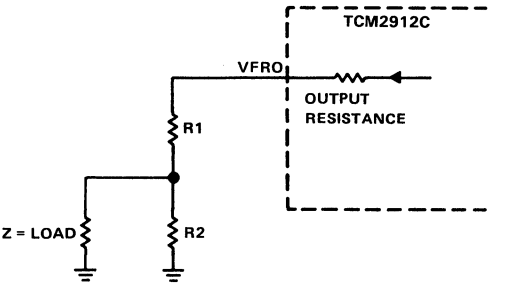
†Applies to the TCM2912C-3 only.

TYPICAL APPLICATION DATA



*GAIN = 1 (R2/R1)

FIGURE 3. PASSBAND GAIN ADJUSTMENT



$$R_T = R1 + \frac{R2 \cdot Z}{R2+Z} = 10\ k\Omega$$

FIGURE 4. OUTPUT GAIN ADJUSTMENT FOR RECEIVE FILTER IF DRIVER AMPLIFIER IS NOT USED.

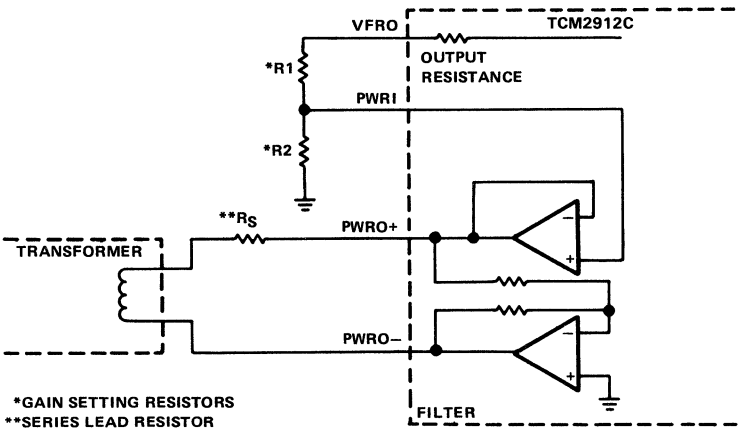


FIGURE 5. TYPICAL CONNECTION FOR OUTPUT DRIVER AMPLIFIER WITH EXTERNAL GAIN ADJUST

TYPICAL CHARACTERISTICS

DEPARTURE FROM LINEAR PHASE
TCM2912C
TRANSMIT SECTION

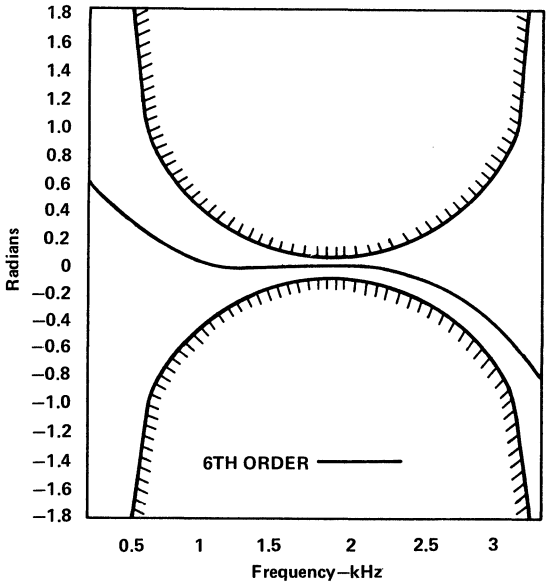
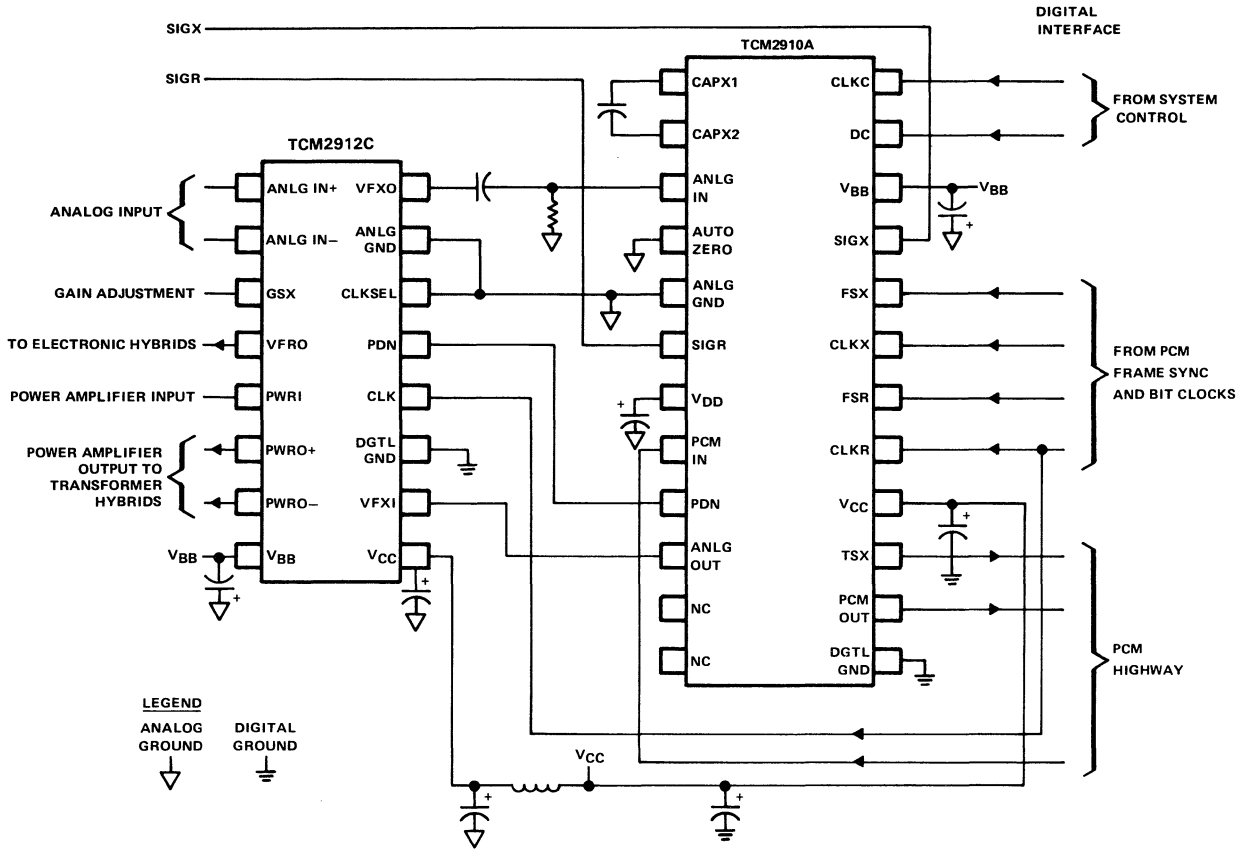


FIGURE 6

FROM: *DIGITAL CHANNEL BANK REQUIREMENTS AND OBJECTIVES*, AT&T, JUNE 1978, PUB 43801, PARAGRAPH 13.4.



NOTE: CLK = 1.544 MHz, with CLKSEL connected to ANLG GND.

FIGURE 7. TCM2912C INTERFACE WITH TCM2910A CODEC

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D2765, SEPTEMBER 1983—REVISED JUNE 1988

NOT RECOMMENDED FOR NEW DESIGN

- **For New Design Refer to TCM29C13, TCM29C14, TCM29C16, and TCM29C17.**

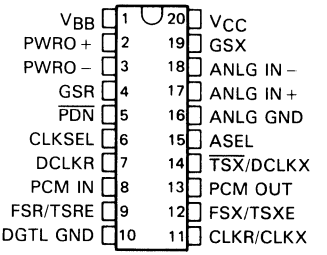
FEATURE TABLE

FEATURE	2913	2914	2916	2917
Number of Pins:				
24		X		
20	X			
16			X	X
μ-law/A-law Coding:				
μ-law	X	X	X	
A-law	X	X		X
Data Timing Rates:				
Variable Mode				
64 kHz to 2.048 MHz	X	X	X	X
Fixed Mode				
1.536 MHz	X	X		
1.544 MHz	X	X		
2.048 MHz	X	X	X	X
Loopback Test Capability		X		
8th-Bit Signaling		X		

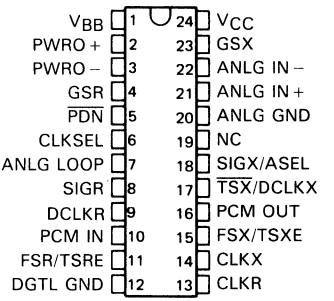
description

The TCM2913, TCM2914, TCM2916, and TCM2917 are single-chip pulse-code-modulated encoders and decoders (PCM codecs) and PCM line filters. These devices provide all the functions required to interface a full-duplex (4-wire) voice telephone circuit with a time-division-multiplexed (TDM) system. These

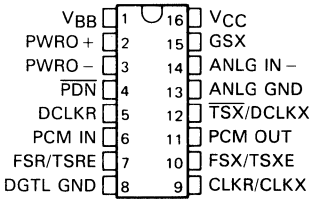
TCM2913
J DUAL-IN-LINE PACKAGE
(TOP VIEW)



TCM2914
JW DUAL-IN-LINE PACKAGE
(TOP VIEW)



TCM2916, TCM2917
J DUAL-IN-LINE PACKAGE
(TOP VIEW)



Caution. These devices have limited built-in gate protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

description (continued)

devices are intended to replace the TCM2910A in tandem with the TCM2912C. Primary applications of the devices include:

- Line Interface for Digital Transmission and Switching of T1 Carrier, PABX, and Central Office Telephone Systems
- Subscriber Line Concentrators
- Digital Encryption Systems
- Digital Voice Band Data Storage Systems
- Digital Signal Processing

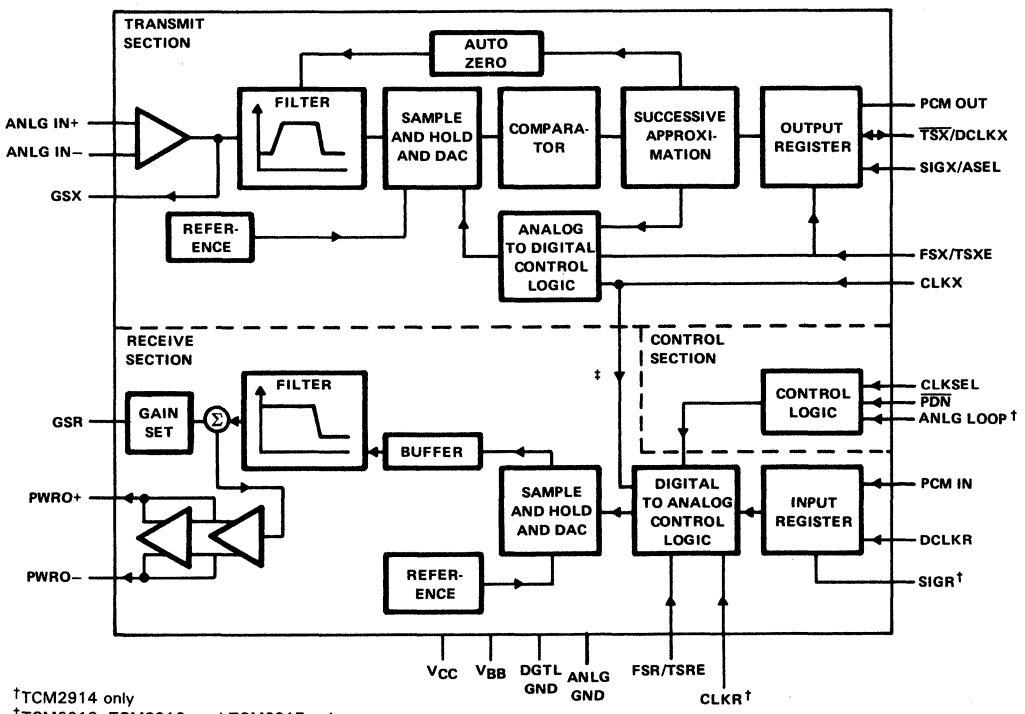
These devices are designed to perform the transmit encoding (A/D conversion) and receive decoding (D/A conversion) as well as the transmit and receive filtering functions in a pulse-code-modulated system. They are intended to be used at the analog termination of a PCM line or trunk.

The TCM2913, TCM2914, TCM2916, and TCM2917 provide the bandpass filtering of the analog signals prior to encoding and after decoding. These combination devices perform the encoding and decoding of voice and call progress tones as well as the signaling and supervision information.

The TCM2913, TCM2914, TCM2916, and TCM2917 are characterized for operation from 0°C to 70°C.

The TCM2913-3 version is identical to the standard version except that maximum encoder milliwatt response and digital milliwatt response are ±0.40 dBm0.

functional block diagram



†TCM2914 only
‡TCM2913, TCM2916, and TCM2917 only

PIN			NAME	DESCRIPTION
TCM2913	TCM2914	TCM2916 TCM2917		
1	1	1	V_{BB}	Most negative supply voltage; input is −5 V ±5%.
2	2	2	PWRO+	Noninverting output of power amplifier. Can drive transformer hybrids or high-impedance loads directly in either a differential or a single-ended configuration.
3	3	3	PWRO−	Inverting output of power amplifier; functionally identical with and complementary to PWRO+.
4	4		GSR	Input to the gain-setting network on the output power amplifier. Transmission level can be adjusted over a 12-dB range depending upon the voltage at GSR.
5	5	4	$\overline{PDN}$	Power-down select. The device is inactive with a TTL low-level input to this pin and active with a TTL high-level input to the pin.
6	6		CLKSEL	Clock frequency selection. Input must be connected to V_{BB}, V_{CC}, or ground to reflect the master clock frequency. When tied to V_{BB}, CLK is 2.048 MHz. When tied to ground, CLK is 1.544 MHz. When tied to V_{CC}, CLK is 1.536 MHz.
	7		ANLG LOOP	Provides loopback test capability. When this input is TTL high, PWRO+ is internally connected to ANLG IN.
	8		SIGR	Signaling bit output, receive channel; in a fixed-data-rate mode, outputs the logical state of the 8th bit (LSB) of the PCM word in the most recent signaling frame.
7	9	5	DCLKR	Selects fixed or variable data-rate operation. When this pin is connected to V_{BB}, the device operates in the fixed-data-rate mode. When DCLKR is not connected to V_{BB}, the device operates in the variable-data-rate mode, and DCLKR becomes the receive data clock, which operates at frequencies from 64 kHz to 2.048 MHz.
8	10	6	PCM IN	Receive PCM input. PCM data is clocked in on this pin on eight consecutive negative transitions of the receive data clock, which is CLKR in fixed-data-rate timing and DCLKR in variable-data-rate timing.
9	11	7	FSR/TSRE	Frame synchronization clock input/time slot enable for receive channel. In the fixed-data-rate mode, FSR distinguishes between signaling and non-signaling frames by a double- or single-length pulse, respectively. In the variable-data-rate mode, this signal must remain high for the duration of the timeslot. The receive channel enters the standby state when FSR is TTL low for 300 ms.
10	12	8	DGTL GND	Digital ground for all internal logic circuits. Not internally connected to ANLG GND.
11	13	9	CLKR	Receive master clock and data clock for the fixed-data-rate mode. Receive master clock only for variable-data-rate mode. CLKR and CLKX are internally connected together for TCM2913, TCM2916, and TCM2917.

PIN			NAME	DESCRIPTION
TCM2913	TCM2914	TCM2916 TCM2917		
11	14	9	CLKX	Transmit master clock and data clock for the fixed-data-rate mode. Transmit master clock only for variable data rate mode. CLKR and CLKX are internally connected for the TCM2913, TCM2916, and TCM2917.
12	15	10	FSX/TSXE	Frame synchronization clock input/time-slot enable for transmit channel. Operates independently of, but in an analagous manner to, FSR/TSRE. The transmit channel enters the standby state when FSX is TTL low for 300 ms.
13	16	11	PCM OUT	Transmit PCM output. PCM data is clocked out on this output on eight consecutive positive transitions of the transmit data clock, which is CLKX in fixed-data-rate timing and DCLKX in variable-data-rate timing.
14	17	12	$\overline{\text{TSX}}$/DCLKX	Transmit channel time slot strobe (output) or data clock (input) for the transmit channel. In the fixed-data-rate mode, this pin is an open-drain output to be used as an enable signal for a three-state buffer. In the variable-data rate mode, DCLKX becomes the transmit data clock, which operates at TTL levels from 64 kHz to 2.048 MHz.
15	18		SIGX/ASEL	Used to select between A-law and μ-law operation. When connected to V_{BB}, A-law is selected. When connected to V_{CC} or ground, μ-law is selected. When not connected to V_{BB}, it is a TTL-level input that is transmitted as the eighth bit (LSB) of the PCM word during signaling frames on the PCM OUT pin (TCM2914 only). SIGX/ASEL is internally connected to provide μ-law operation for TCM2916 and A-law operation for TCM2917.
16	20	13	ANLG GND	Analog ground return for all internal voice circuits. Not internally connected to DGTL GND.
17	21		ANLG IN+	Noninverting analog input to uncommitted transmit operational amplifier. Internally connected to ANLG GND on TCM2916 and TCM2917.
18	22	14	ANLG IN−	Inverting analog input to uncommitted transmit operational amplifier.
19	23	15	GSX	Output terminal of internal uncommitted operational amplifier. Internally, this is the voice signal input to the transmit filter.
20	24	16	V_{CC}	Most positive supply voltage; input is 5 V ± 5%.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . −0.3 V to 15 V
Output voltage, V_O . . . . . −0.3 V to 15 V
Input voltage, V_I . . . . . −0.3 V to 15 V
Digital ground voltage . . . . . −0.3 V to 15 V
Continuous total dissipation at (or below) 25°C free-air temperature . . . . . See Dissipation Rating Table
Operating free-air temperature range (under bias) . . . . . −10°C to 80°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J or JW package . . . . . 300°C

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 80°C$ POWER RATING
J	1375 mW	11.0 mW/°C	25°C	770 mW
JW	1375 mW	no derating		1375 mW

NOTE 1: Voltage values for maximum ratings are with respect to V_{BB}.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (see Note 2)		4.75	5	5.25	V
V_{BB}	Supply voltage		−4.75	−5	−5.25	V
	DGTL GND voltage with respect to ANLG GND			0		V
V_{IH}	High-level input voltage, all inputs except CLKSEL		2.2			V
V_{IL}	Low-level input voltage, all inputs except CLKSEL				0.8	V
	Clock select input voltage	For 2.048 MHz	V_{BB}		$V_{BB}+0.5$	V
		For 1.544 MHz	0		0.5	
		For 1.536 MHz	$V_{CC}-0.5$		V_{CC}	
R_L	Load resistance	At GSX	10			kΩ
		At PWRO+ and/or PWRO−	300			Ω
C_L	Load capacitance	At GSX			50	pF
		At PWRO+ and/or PWRO−			100	
T_A	Operating free-air temperature		0		70	°C

NOTE 2: Voltages at analog inputs and outputs, V_{CC}, and V_{BB} terminals are with respect to the ANLG GND terminal. All other voltages are referenced to the DGTL GND terminal unless otherwise noted.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature

supply current, f_{DCLK} = 2.048 MHz, outputs not loaded

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_{CC}	Supply current from V_{CC}	Operating			14	19	mA
		Standby	FSX, FSR = V_{IL} after 300 ms		1.2	2.4	
		Power-down	PDN = V_{IL} after 10 μs		0.5	1	
I_{BB}	Supply current from V_{BB}	Operating			−18	−24	mA
		Standby	FSX, FSR = V_{IL} after 300 ms		−1.2	−2.4	
		Power-down	PDN = V_{IL} after 10 μs		−0.5	−1	
	Power dissipation	Operating			140	226	mW
		Standby	FSX, FSR = V_{IL} after 300 ms		12	25	
		Power down	PDN = V_{IL} after 10 μs		5	10.5	

digital interface

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	PCM OUT	I_{OH} = −9.6 mA	2.4			V
		SIGR	I_{OH} = −1.2 mA	2.4			
V_{OL}	Low-level output voltage at PCM OUT, TSX, SIGR		I_{OL} = 3.2 mA			0.4	V
I_{IH}	High-level input current, any digital input		V_I = 2.2 V to V_{CC}			10	μA
I_{IL}	Low-level input current, any digital input		V_I = 0 to 0.8 V			10	μA
C_i	Input capacitance				5	10	pF
C_o	Output capacitance				5		pF

transmit amplifier input

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input current at ANLG IN+, ANLG IN−	V_I = −2.17 V to 2.17 V			±100	nA
Input offset voltage at ANLG IN+, ANLG IN−	V_I = −2.17 V to 2.17 V			±25	mV
Common-mode rejection at ANLG IN+, ANLG IN−	V_I = −2.17 V to 2.17 V	55			dB
Open-loop voltage amplification at GSX		5000			
Open-loop unity-gain bandwidth at GSX			1		MHz
Input resistance at ANLG IN+, ANLG IN−		10			MΩ

receive filter output

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Output offset voltage PWRO+, PWRO− (single-ended)	Relative to ANLG GND		120		mV
Output resistance at PWRO+, PWRO−			1		Ω

†All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C.

gain and dynamic range, V_{CC} = 5 V, V_{BB} = −5 V, T_A = 25°C (unless otherwise noted) (see Notes 3, 4, and 5)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Encoder milliwatt response (transmit gain tolerance)		Signal input = 1.064 V rms	Standard versions		±0.08	±0.18	dBm0
			TCM2913-3		±0.18	±0.40	
Encoder milliwatt response variation with temperature and supplies		T_A = 0°C to 70°C, Supplies = ±5%				±0.07	dB
Digital milliwatt response (receive tolerance gain) relative to zero-transmission level point		Signal input per CCITT G.711 Output signal = 1 kHz	Standard versions		±0.08	±0.18	dBm0
			TCM2913-3		±0.18	±0.40	
Digital milliwatt response variation with temperature and supplies		T_A = 0°C to 70°C, Supplies = ±5%				±0.07	dB
Zero-transmission-level point, transmit channel (0 dBm0)	μ-law	R_L = 600 Ω			2.76		dBm
	A-law				2.79		
	μ-law	R_L = 900 Ω			1		
	A-law				1.03		
Zero-transmission-level point, receive channel (0 dBm0)	μ-law	R_L = 600 Ω			5.76		dBm
	A-law				5.79		
	μ-law	R_L = 900 Ω			4		
	A-law				4.03		

NOTES: 3. Unless otherwise noted, the analog input is a 0-dBm0, 1020-Hz sine wave, where 0 dBm0 is defined as the zero-reference point of the channel under test. This corresponds to an analog signal input of 1.064 V rms, or an output of 1.503 V rms.
4. The input amplifier is set for unity gain. The digital input is a PCM bit stream generated by passing a 0-dBm0, 1020-Hz sine wave through an ideal encoder.
5. Receive output is measured single-ended in the maximum-gain configuration. To set the output amplifier for maximum gain, GSR is connected to PWRO− and the output is taken at PWRO+. All output levels are (sin x)/x corrected.

gain tracking over recommended ranges of supply voltage and operating free-air temperature, reference level = −10 dBm0

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Transmit gain tracking error, sinusoidal input	−3 to −40 dBm0		±0.25	dB
	−40 to −50 dBm0		±0.5	
	−50 to −55 dBm0		±1.2	
Receive gain tracking error, sinusoidal input	−3 to −40 dBm0		±0.25	dB
	−40 to −50 dBm0		±0.5	
	−50 to −55 dBm0		±1.2	

noise over recommended ranges of supply voltage and operating free-air temperature

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Transmit noise, C-message weighted	ANLG IN+ = ANLG GND, ANLG IN− = GSX		15	dBrnC0
Transmit noise, C-message weighted with eighth-bit signaling (TCM2914 only)	ANLG IN+ = ANLG GND, ANLG IN− = GSX, 6th frame signaling		18	dBrnC0
Transmit noise, psophometrically weighted	ANLG IN+ = ANLG GND, ANLG IN− = GSX		−75	dBm0p
Receive noise, C-message weighted quiet code	PCM IN = 11111111 (μ-law) PCM IN = 10101010 (A-law) measured at PWRO+		11	dBrnC0
Receive noise, C-message weighted sign bit toggled	Input to PCM IN is zero code with sign bit toggled at 1-kHz rate		12	dBrnC0
Receive noise, psophometrically weighted	PCM = lowest positive decode level		−79	dBm0p

power supply rejection and crosstalk attenuation over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{CC} supply voltage rejection ratio, transmit channel	f = 0 to 30 kHz	Idle channel, supply signal = 200 mV p-p, f measured at PCM OUT		−30		dB
	f = 30 to 50 kHz			−45		
V_{BB} supply voltage rejection ratio, transmit channel	f = 0 to 30 kHz	Idle channel, supply signal = 200 mV p-p, f measured at PCM OUT		−30		dB
	f = 30 to 50 kHz			−55		
V_{CC} supply voltage rejection ratio, receive channel (single-ended)	f = 0 to 30 kHz	Idle channel, supply signal = 200 mV p-p, narrow-band, f measured at PWRO+		−20		dB
	f = 30 to 50 kHz			−45		
V_{BB} supply voltage rejection ratio, receive channel (single-ended)	f = 0 to 30 kHz	Idle channel, supply signal = 200 mV p-p, narrow-band, f measured at PWRO+		−20		dB
	f = 30 to 50 kHz			−45		
Crosstalk attenuation, transmit-to-receive (single-ended)		ANLG IN+ = 0 dBm0, f = 1.02 kHz, unity gain, PCM IN = lowest decode level measured at PWRO+	71			dB
Crosstalk attenuation, receive-to-transmit (single-ended)		PCM IN = 0 dBm0, f = 1.02 kHz, ANLG IN+ = ANLG GND, measured at PCM OUT	71			dB

†All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

distortion over recommended ranges of supply voltage and operating free-air temperature

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Transmit signal to distortion ratio, sinusoidal input (see Note 6)	ANLG IN+ = 0 to −30 dBm0	36			dB
	ANLG IN+ = −30 to −40 dBm0	30			
	ANLG IN+ = −40 to −45 dBm0	25			
Receive signal to distortion ratio, sinusoidal input (see Note 6)	ANLG IN+ = 0 to −30 dBm0	36			dB
	ANLG IN+ = −30 to −40 dBm0	30			
	ANLG IN+ = −40 to −45 dBm0	25			
Transmit single-frequency distortion products	AT&T Advisory #64 (3.8), Input signal = 0 dBm0			−46	dBm0
Receive single-frequency distortion products	AT&T Advisory #64 (3.8), Input signal = 0 dBm0			−46	dBm0
Intermodulation distortion, end-to-end Spurious out-of-band signals, end-to-end	CCITT G.712 (7.1)			−35	dBm0
	CCITT G.712 (7.2)			−49	
	CCITT G.712 (6.1)			−25	dBm0
	CCITT G.712 (9)			−40	
Transmit absolute delay time to PCM OUT	Fixed data rate, CLKS = 2.048 MHz, Input to ANLG IN+ = 1.02 kHz at 0 dBm0		245		μs
Transmit differential envelope delay time relative to transmit absolute delay time	f = 500 Hz to 600 Hz		170		μs
	f = 600 Hz to 1000 Hz		95		
	f = 1000 Hz to 2600 Hz		45		
	f = 2600 Hz to 2800 Hz		105		
Receive absolute delay time to PWRO+	Fixed data rate, f_{CLKR} = 2.048 MHz, Digital input is DMW codes		190		μs
Receive differential envelope delay time relative to transmit absolute delay time	f = 500 Hz to 600 Hz		45		μs
	f = 600 Hz to 1000 Hz		35		
	f = 1000 Hz to 2600 Hz		85		
	f = 2600 Hz to 2800 Hz		110		

†All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C.
NOTE 6. CCITT G.712 — Method 2.

transmit filter transfer over recommended ranges of supply voltage and operating free-air temperature (see Figure 1)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Gain relative to gain at 1.02 kHz	Input amplifier set for unity gain, Noninverting maximum gain output, Input signal at ANLG IN is 0 dBm0	16.67 Hz		−30	dB
		50 Hz		−25	
		60 Hz		−23	
		200 Hz	−1.8	0.125	
		300 Hz to 3 kHz	−0.125	0.125	
		3.3 kHz	−0.35	0.03	
		3.4 kHz	−0.7	−0.1	
		4 kHz		−14	
		4.6 kHz and above		−32	

receive filter transfer over recommended ranges of supply voltage and operating free-air temperature(see Figure 2)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Gain relative to gain at 1.02 kHz	Input signal at PCM IN is 0 dBm0	Below 200 Hz		0.125	dB
		200 Hz	−0.5	0.125	
		300 Hz to 3 kHz	−0.125	0.125	
		3.3 kHz	−0.35	0.03	
		3.4 kHz	−0.7	−0.1	
		4 kHz		−14	
		4.6 kHz and above		−30	

clock timing requirements over recommended ranges of supply voltage and operating free-air temperature (see timing diagrams)

	PARAMETER	MIN	TYP†	MAX	UNIT
$t_{c(CLK)}$	Clock period for CLKX, CLKR (2.048-MHz systems)	488			ns
t_r, t_f	Rise and fall times for CLKX and CLKR		5	30	ns
$t_{w(CLK)}$	Pulse duration for CLKX and CLKR (see Note 7)	220			ns
$t_{w(DCLK)}$	Pulse duration for DCLK (f_{DCLK} = 64 Hz to 2.048 MHz) (see Note 8)	220			ns
	Clock duty cycle [$t_{w(CLK)}/t_{c(CLK)}$] for CLKX and CLKR	45	50	55	%

†All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C.

transmit timing requirements over recommended ranges of supply voltage and operating free-air temperature, fixed-data-rate mode (see timing diagrams)

	PARAMETER	MIN	MAX	UNIT
$t_{d(FSX)}$	Frame sync delay time	100	$t_{c(CLK)}-100$	ns
$t_{su(SIGX)}$	Setup time before Bit 7 falling edge (TCM2914 only)	0		ns
$t_{h(SIGX)}$	Hold time after Bit 8 falling edge (TCM2914 only)	0		ns

propagation delay times over recommended ranges of operating conditions, fixed-data-rate mode (see timing diagrams)

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{pd1}	From rising edge of transmit clock to Bit 1 data valid at PCM OUT (data enable time on time slot entry) (see Note 8)	C_L = 0 to 100 pF	0	145	ns
t_{pd2}	From rising edge of transmit clock Bit n to Bit n + 1 data valid at PCM OUT (data valid time)	C_L = 0 to 100 pF	0	145	ns
t_{pd3}	From falling edge of transmit clock Bit 8 to Bit 8 Hi-Z at PCM OUT (data float time on time slot exit) (see Note 8)	C_L = 0	60	215	ns
t_{pd4}	From rising edge of transmit clock Bit 1 to TSX active (low) (time slot enable time)	C_L = 0 to 100 pF	0	145	ns
t_{pd5}	From falling edge of transmit clock Bit 8 to TSX inactive (high) (time slot disable time) (see Note 8)	C_L = 0	60	190	ns
t_{pd6}	From rising edge of channel time slot to SIGR update (TCM2914 only)		0	2	μs

NOTES: 7. FSX CLK must be phase locked with the CLKX, FSR CLK must be phase locked with CLKR.
8. Timing parameters t_{pd1}, t_{pd3}, and t_{pd5} are referenced to the high-impedance state.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

receive timing requirements over recommended ranges of supply voltage and operating free-air temperature, fixed-data-rate mode (see timing diagrams)

PARAMETER		MIN	MAX	UNIT
$t_{d(FSR)}$	Frame sync delay time	100	$t_{c(CLK)}-100$	ns
$t_{su(PCM\ IN)}$	Setup time before Bit 7 falling edge (TCM2914 only)	10		ns
$t_{h(PCM\ IN)}$	Hold time after Bit 8 falling edge (TCM2914 only)	60		ns

transmit timing requirements over recommended ranges of supply voltage and operating free-air temperature, variable-data-rate mode (see timing diagrams)

PARAMETER		MIN	MAX	UNIT
$t_{d(TSDX)}$	Timeslot delay time from DCLKX (see Note 9)	140	$t_{d(DCLKX)}-140$	ns
$t_{d(FSX)}$	Frame sync delay time	100	$t_{c(CLK)}-100$	ns
$t_{c(DCLKX)}$	Clock period for DCLKX	488	15620	ns

propagation delay times over recommended ranges of operating conditions, variable-data-rate mode (see Note 10 and timing diagrams)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{pd7}	Data delay time from DCLKX	C_L = 0 to 100 pF	0	100	ns
t_{pd8}	Data delay from timeslot enable to PCM OUT	C_L = 0 to 100 pF	0	50	ns
t_{pd9}	Data delay from time slot disable to PCM OUT	C_L = 0 to 100 pF	0	80	ns
t_{pd10}	Data delay time from FSX	$t_{d(TSDX)}$ = 80 ns	0	140	ns

receive timing requirements over recommended ranges of supply voltage and operating free-air temperature, variable-data-rate mode (see timing diagrams)

PARAMETER		MIN	MAX	UNIT
$t_{d(TSDR)}$	Timeslot delay time from DCLKR (see Note 11)	140	$t_{d(DCLKR)}-140$	ns
$t_{d(FSR)}$	Frame sync delay time	100	$t_{c(CLK)}-100$	ns
$t_{su(PCM\ IN)}$	Setup time before Bit 7 falling edge	10		ns
$t_{h(PCM\ IN)}$	Hold time after Bit 8 falling edge	60		ns
$t_{c(DCLKR)}$	Clock period for DCLKR	488	15620	ns
$t_{d(SER)}$	Timeslot end receive time	0		ns

64-kilobit operation timing requirements over recommended ranges of supply voltage and operating free-air temperature,variable-data-rate mode

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{FSLX}	Transmit frame sync minimum down time	FSX = TTL high for remainder of frame	488		ns
t_{FSLR}	Receive frame sync minimum down time	FSR = TTL high for remainder of frame	1952		ns
t_{DCLK}	Pulse duration data clock			10	μs

NOTES: 9. t_{FSLX} minimum requirement overrides the $t_{d(TSDX)}$ maximum requirement for 64-kHz operation.
10. Timing parameters t_{pd8} and t_{pd9} are referenced to a high-impedance state.
11. t_{FSLR} minimum requirement overrides the $t_{d(TSDR)}$ maximum requirement for 64-kHz operation.

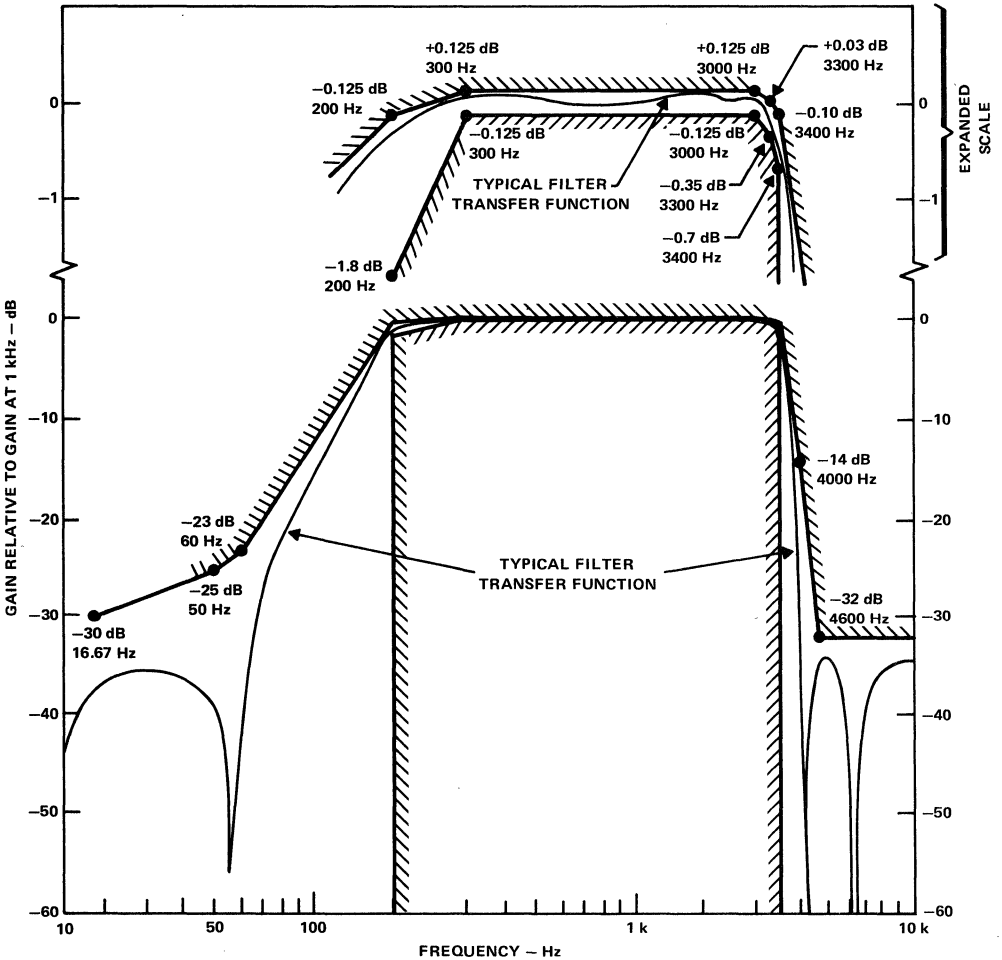
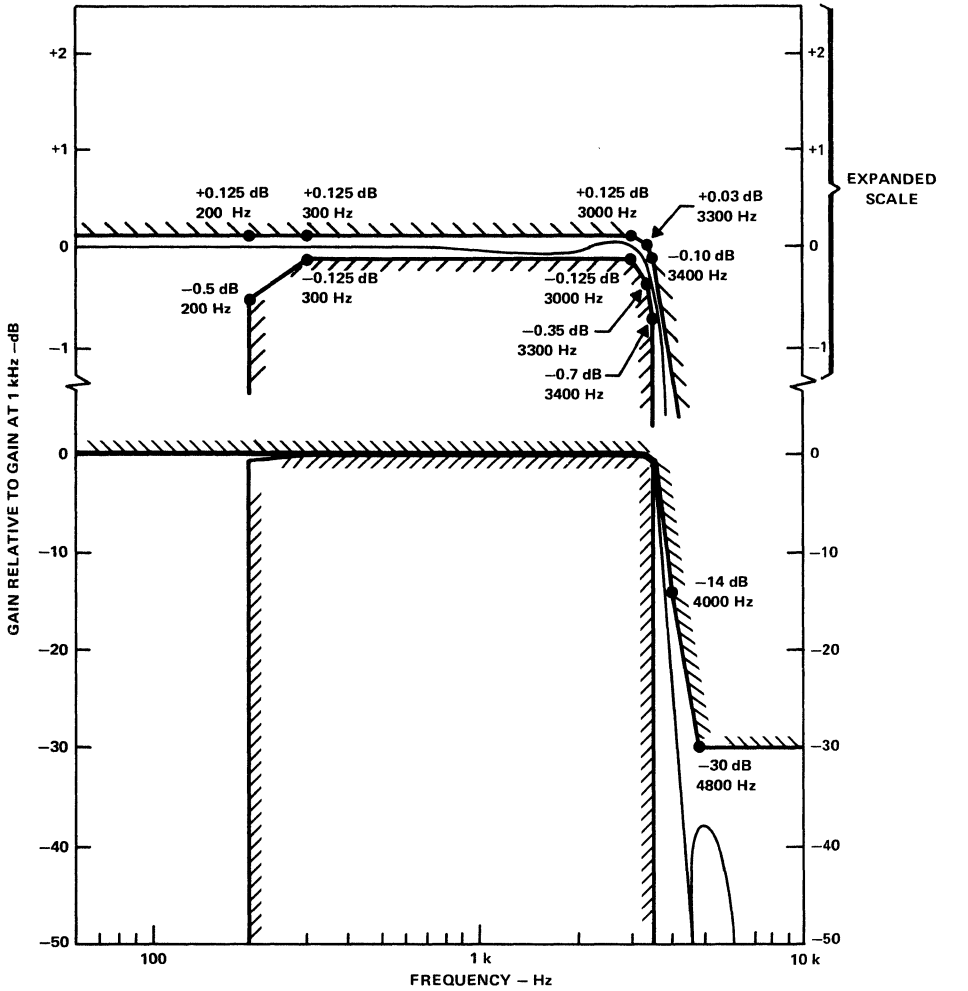


FIGURE 1. TRANSFER CHARACTERISTICS OF THE TRANSMIT FILTER

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265



NOTE: This is a typical transfer function of the receiver filter component.

FIGURE 2. TRANSFER CHARACTERISTIC OF THE RECEIVE FILTER

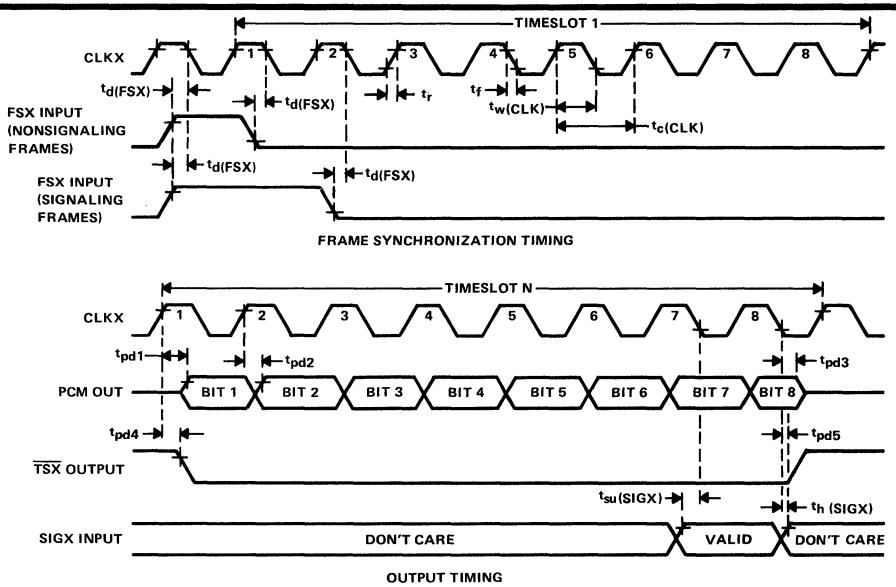


FIGURE 3. TRANSMIT TIMING (FIXED-DATA-RATE)

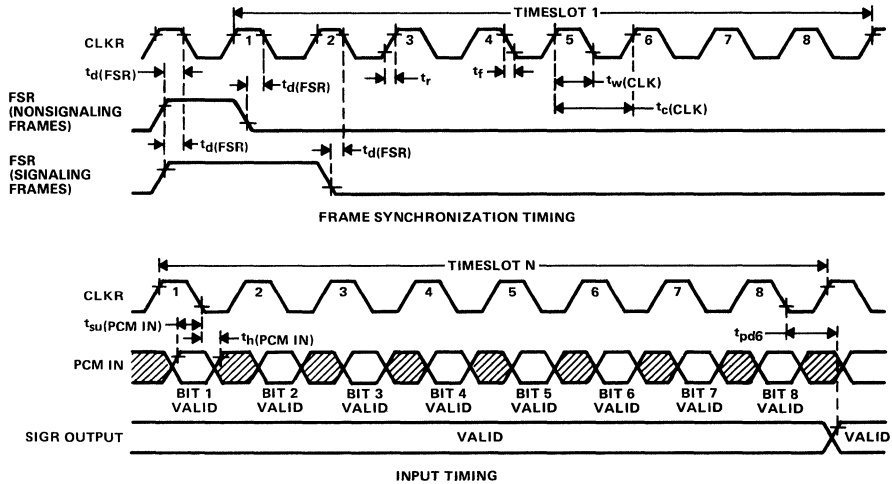


FIGURE 4. RECEIVE TIMING (FIXED-DATA-RATE)

NOTES: A. Inputs are driven from 0.45 V to 2.4 V. Time intervals are referenced to 2 V if the high level is indicated and 0.8 V if the low level is indicated.

B. BIT 1 = MSB = Sign Bit and is clocked in first on the PCM-IN pin or is clocked out first on the PCM-OUT pin. BIT 8 = LSB = Least Significant Bit and is clocked in last on the PCM-IN pin or is clocked out last on the PCM-OUT pin.

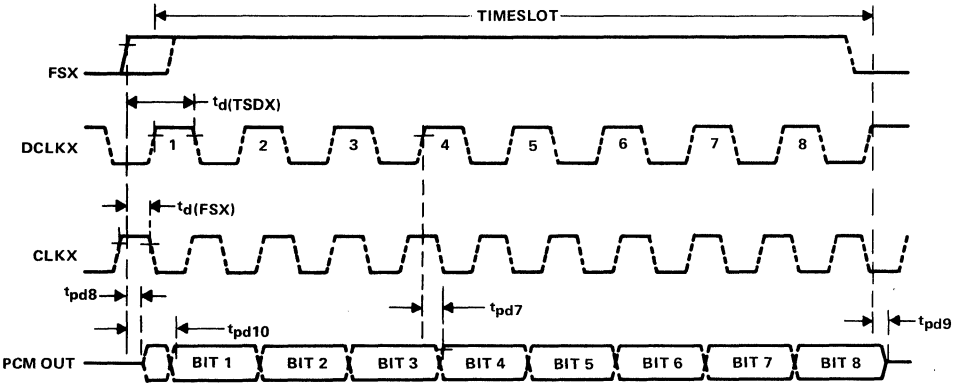
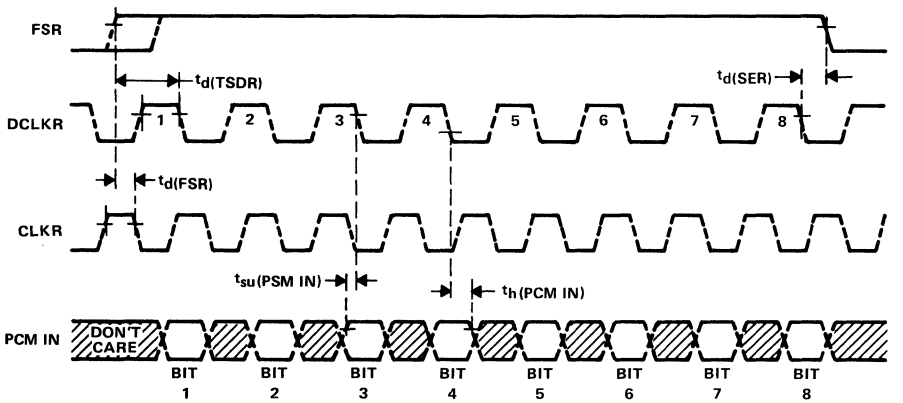


FIGURE 5. TRANSMIT TIMING (VARIABLE-DATA-RATE)



NOTES: B. BIT 1 = MSB = Sign Bit and is clocked in first on the PCM-IN or is clocked out first on the PCM-OUT pin. BIT 8 = LSB = Least Significant Bit and is clocked in last on the PCM-PIN or is clocked out last on the PCM-OUT pin.
C. All timing parameters referenced to V_{IH} and V_{IL} except t_{pd8} and t_{pd9}, which are referenced to a high-impedance state.

FIGURE 6. RECEIVE TIMING (VARIABLE-DATA-RATE)

GENERAL OPERATION

system reliability features

The TCM2913, TCM2914, TCM2916, or TCM2917 is powered up in four steps:
V_{CC} and V_{BB} supply voltages are applied.
All clocks are connected.
TTL high is applied to $\overline{PDN}$.
FSX and/or FSR synchronization pulses are applied.

On the transmit channel, digital outputs PCM out and $\overline{TSX}$ are held in high-impedance state for approximately four frames (500 μs) after power up or application of V_{BB} or V_{CC}. After this delay, PCM OUT, $\overline{TSX}$, and signaling are functional and will occur in the proper timeslot. The analog circuits on the transmit side require approximately 60 ms to reach their equilibrium value due to the autozero circuit settling time. Thus valid digital information, such as for on/off hook detection, is available almost immediately, while analog information is available after some delay.

On the receive channel, the digital output SIGR is also held low for a maximum of four frames after power up or application of V_{BB} or V_{CC}. SIGR will remain low until it is updated by a signalling frame.

To further enhance system reliability, PCM OUT and $\overline{TSX}$ will be placed in a high-impedance state approximately 20 μs after an interruption of CLKX. SIGR will be held low approximately 20 μs after an interruption of CLKR. These interruptions could possible occur with some kind of fault condition.

power-down and standby operations

To minimize power consumption, a power-down mode and three standby modes are provided.

For power down, an external TTL low signal is applied to the $\overline{PDN}$ pin. It is not sufficient to remove the TTL high voltage to $\overline{PDN}$. In the absence of a signal, the $\overline{PDN}$ pin floats to TTL high and the device remains active. In the power-down mode, the average power consumption is reduced to an average of 5 mW.

The standby modes give the user the option of putting the entire device on standby, putting only the transmit channel on standby, or putting only the receive channel on standby. To place the entire device on standby, both FSX and FSR are held at TTL low. For transmit-only operation, FSX is high and FSR is held low. For receive-only operation, FSR is high and FSX is held low. See Table 1 for power down and standby procedures.

The first TSX pulse that occurs after power-up or removal from standby mode may not be exactly 8 data bits long. In applications that require a valid first TSX, such as Digital Signal Processing, the TCM29C13, TCM29C14, TCM29C16, and TCM29C17 are recommended.

TABLE 1. POWER DOWN AND STANDBY PROCEDURES

DEVICE STATUS	PROCEDURE	TYPICAL POWER CONSUMPTION	DIGITAL OUTPUT STATUS
Power down	$\overline{PDN}$ = TTL low	5 mW	$\overline{TSX}$ and PCM OUT are in a high-impedance state; SIGR goes to TTL low within 10 μs.
Entire device on standby	FSX and FSR are TTL low	12 mW	$\overline{TSX}$ and PCM OUT are in a high-impedance state; SIGR goes to TTL low within 300 ms.
Only transmit on standby	FSX is TTL low FSR is TTL high	70 mW	$\overline{TSX}$ and PCM OUT are placed in a high-impedance state within 300 ms.
Only receive on standby	FSR is TTL low FSX is TTL high	110 mW	SIGR is placed in a high-impedance state within 300 ms.

fixed-data-rate timing (see Figure 7)

Fixed-data-rate timing is selected by connecting DCLKR to V_{BB}. It uses master clocks CLKX and CLKR, frame synchronizer clocks FSX and FSR, and output $\overline{TSX}$. FSX and FSR are 8-kHz inputs that set the sampling frequency and distinguish between signaling and nonsignaling frames by their pulse width. A frame synchronization pulse one master clock wide designates a nonsignaling frame, while a double width sync pulse enables the signaling function (TCM2914 only). Data is transmitted on the PCM OUT pin on the first eight positive transitions of CLKX following the rising edge of FSX. Data is received on the PCM IN pin on the first eight falling edges of CLKR following FSX. A digital-to-analog (D/A) conversion is performed on the received digital word and the resulting analog sample is held on an internal sample-and-hold capacitor until transferred to the receive filter.

The clock selection pin (CLKSEL) is used to select the frequency of CLKX and CLKR (TMC2913 and TCM2914 only). The TCM2913 and TCM2914 fixed data rate mode can operate with frequencies of 1.536 MHz, 1.544 MHz, or 2.048 MHz. The TCM2916 and TCM2917 fixed data rate mode operates at 2.048 MHz only.

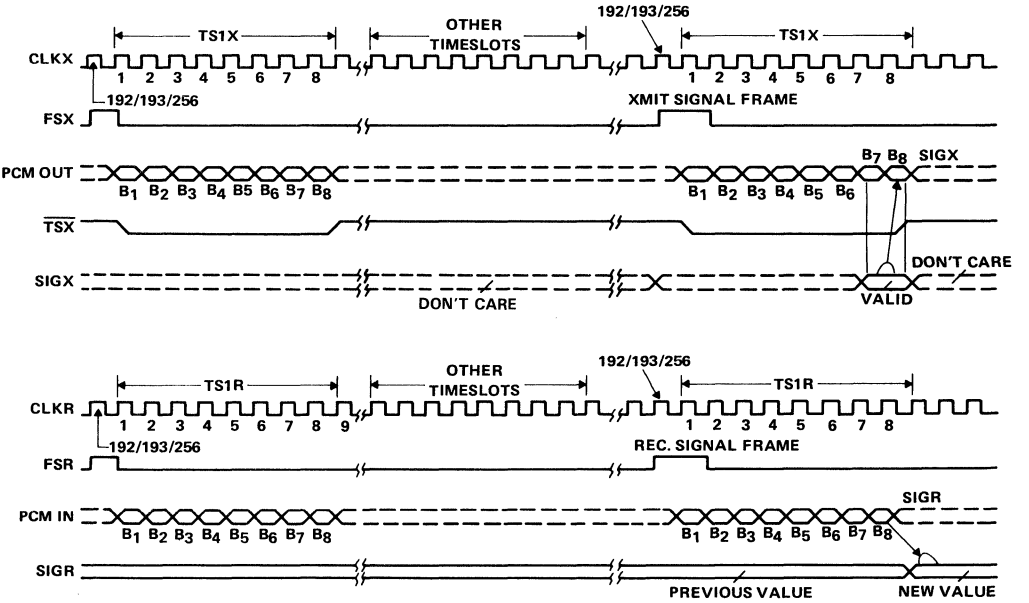


FIGURE 7. SIGNALING TIMING (FIXED-DATA-RATE ONLY)

variable data rate timing

Variable-data-rate timing is selected by connecting DCLKR to the bit clock for the receive PCM highway rather than to V_{BB}. It uses master clocks CLKX and CLKR, bit clocks DCLKX and DCLKR, and frame synchronization clocks FSX and FSR.

Variable-data-rate timing allows for a flexible data frequency. The frequency of the bit clocks can be varied from 64 kHz to 2.048 MHz. The bit clocks can be asynchronous in the TCM2914, but must be synchronous in the TCM2913, TCM2916, and TCM2917. Master clocks in types TCM2913 and TCM2914 are restricted to frequencies of operation of 1.536 MHz, 1.544 MHz, or 2.048 MHz as in the fixed-data-rate timing mode. The master clock for the TCM2916 and TCM2917 is restricted to 2.048 MHz.

While FSX/TSXE input is high, PCM data is transmitted from PCM OUT onto the highway on the next eight consecutive positive transitions of DCLKX. Similarly, while the FSR/TSRE input is high, the PCM word is received from the highway by PCM IN on the next eight consecutive negative transitions of DCLKR.

The transmitted PCM word will be repeated in all remaining timeslots in the 125 μs frame as long as DCLKX is pulsed and FSX is held high. This feature, which allows the PCM word to be transmitted to the PCM highway more than once per frame, if desired, is available only with variable-data-rate timing. Signaling is allowed only in the fixed-data-rate mode because the variable-data-rate mode provides no means with which to specify a signaling frame.

signaling

The TCM2914 (only) provides 8th-bit signaling in the fixed-data-rate timing mode. Transmit and receive signaling frames are independent of each other and are selected by a double-width frame sync pulse on the appropriate channel. During a transmit signaling frame, the signal present on SIGX is substituted for the least significant bit (LSB) of the encoded PCM word. In a receive signaling frame, the codec will decode the seven most significant bits in accordance with CCITT G.733 recommendations, and output the logical state of the LSB on the SIGR pin until it is updated in the next signaling frame. Timing relationships for signaling operations are shown n Figure 9. The signaling path is used to transmit digital signaling information such as ring control, rotary dial pulses, and off-hook and disconnect supervision. The voice path is used to transmit prerecorded messages as well as the call progress tones; dial tone, ring-back tone, busy tone, and re-order tone.

asynchronous operation

The TCM2914 can be operated with asynchronous clocks in either the fixed- or variable-data-rate modes. In order to avoid crosstalk problems associated with special interrupt circuits, the design of the TCM2913 and TCM2914 includes separate digital-to-analog converters and voltage references on the transmit and receive sides to allow completely independent operation of the two channels.

In either timing mode, the master clock, data clock, and timeslot strobe must be synchronized at the beginning of each frame. Specifically, in the variable-data-rate mode the rising edge of CLKX must occur within $t_{d(FSX)}$ ns before the rise of FSX, while the leading edge of DCLKX must occur within t_{TSDX} ns of the rise of FSX. CLKX and DCLKX are synchronized once per frame but may be of different frequencies. The receive channel operates in a similar manner and is completely independent of the transmit timing (see variable data rate timing diagrams). This approach requires the provision of two separate master clocks but avoids the use of a synchronizer, which can cause intermittent data conversion errors.

analog loopback

A distinctive feature of the TCM2914 is its analog loopback capability. With this feature, the user can test the line circuit remotely by comparing the signals sent into the receive channel (PCM IN) with those generated on the transmit channel (PCM OUT). The test is accomplished by sending a control signal that internally connects the analog input and output ports. When ANLG LOOP is TTL high, the receive output (PWRO+) is internally connected to ANLG IN+, GSR is internally connected to PWRO−, and ANLG IN− is internally connected to GSX (see Figure 8).

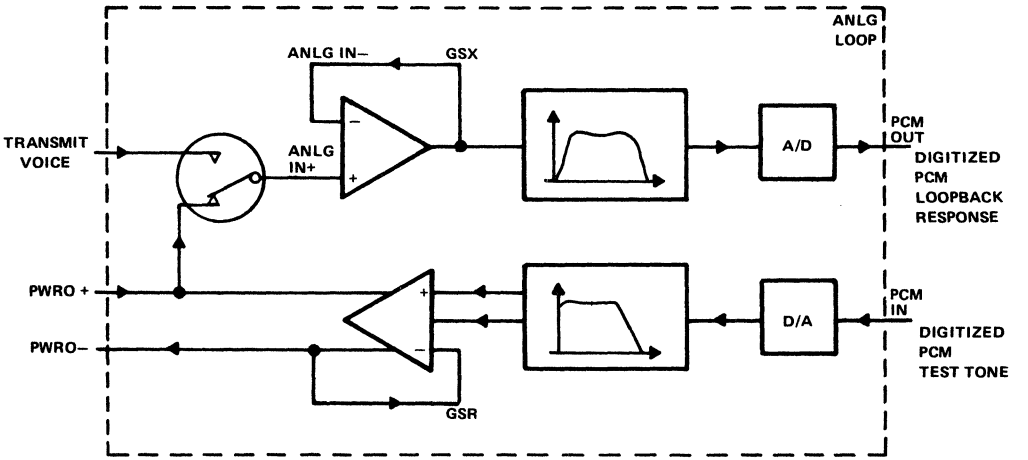


FIGURE 8. TCM2914 ANALOG LOOPBACK CONFIGURATION

Due to the difference in the transmit and receive transmission levels, a 0 dBm0 code into PCM IN will emerge from PCM OUT as a 3-dBm0 code, an implicit gain of 3 dB. Because of this, the maximum signal that can be tested by analog loopback is 0 dBm0.

precision voltage references

No external components are required with the TCM2913, TCM2914, TCM2916, and TCM2917 to provide the voltage references. Voltage references that determine the gain and dynamic range characteristics of the device are generated internally. A difference in subsurface charge density between two suitably implanted MOS devices is used to derive a temperature- and bias-stable reference voltage. These references are calibrated during the manufacturing process.Separate references are supplied to the transmit and receive sections, and each is calibrated independently. Each reference value is then further trimmed in the gain setting operational amplifiers to a final precision value. Manufacturing tolerances can be achieved of typically ±0.04 dB in absolute gain for each half channel, providing the user a significant margin to compensate for error in other board components.

conversion laws

The TCM2913 and TCM2914 provide pin-selectable μ-law operation as specified by CCITT G.711 recommendation. A-law operation is selected when the ASEL pin is connected to V_{BB}. Signaling is not allowed during A-law operation. The TCM2916 is μ-law only. The TCM2917 is A-law only.

The μ-law operation is effectively selected by not selecting A-law operation. If the ASEL pin is connected to V_{CC} or GND, the device is in μ-law operation. If μ-law operation is selected, SIGX is a TTL-level input that can be used in the fixed data rate timing mode to modify the LSB of the PCM output in signaling frames.

transmit operation

transmit filter

The input section provides gain adjustment in the passband by means of an on-chip uncommitted operational amplifier. The load impedance to ground (ANLG GND) at the amplifier output (GSX) must be greater than 10 kΩ in parallel with less than 50 pF. The input signal on the ANLG IN + pin can be either ac or dc coupled. The input operational amplifier can also be used in the inverting mode or differential amplifier mode.

A low-pass antialiasing section is included on the device. This section provides 35-dB attenuation at the sampling frequency. No external components are required to provide the necessary antialiasing function for the switched capacitor section of the transmit filter.

The passband section provides flatness and stopband attenuation that fulfills the AT&T D3/D4 channel bank transmission specification and CCITT recommendation G.712. The TCM2913, TCM2914, TCM2916, and TCM2917 specifications meet or exceed digital class 5 central office switching systems requirements.

A high-pass section configuration was chosen to reject low-frequency noise from 50- and 60-Hz power lines, 17-Hz European electric railroads, ringing frequencies and their harmonics, and other low-frequency noise. Even with the high rejection at these frequencies, the sharpness of the band edge gives low attenuation at 200 Hz. This feature allows the use of low-cost transformer hybrids without external components.

encoding

The encoder internally samples the output of the transmit filter and holds each sample on an internal sample and hold capacitor. The encoder performs an analog-to-digital conversion on a switched capacitor array. Digital data representing the sample is transmitted on the first eight data clocks bits of the next frame.

The autozero circuit corrects for dc offset on the input signal to the encoder. The autozero circuit uses the sign bit averaging technique. The sign bit from the encoder output is long-term averaged and subtracted from the input to the encoder. All dc offset is removed from the encoder input waveform.

receive operation

decoding

The serial PCM word is received at the PCM IN pin on the first eight data clock bits of the frame. Digital-to-analog conversion is performed and the corresponding analog sample is held on an internal sample-and-hold capacitor. This sample is transferred to the receive filter.

receive filter

The receive section of the filter provides passband flatness and stopband rejection that fulfills both the AT&T D3/D4 specification and CCITT recommendation G.712. The filter contains the required compensation for the (sin x)/x response of such decoders.

receive output power amplifiers

A balanced output amplifier is provided to allow maximum flexibility in output configuration. Either of the two outputs can be used single-ended (i.e., referenced to ANLG GND) to drive single-ended loads. Alternatively, the differential output will directly drive a bridged load. The output stage is capable of driving loads as low as 300 ohms single-ended to a level of 12 dBm or 600 ohms differentially to a level of 15 dBm.

The receive channel transmission level may be adjusted between specified limits by manipulation of the GSR input. GSR is internally connected to an analog gain-setting network. When GSR is connected to PWRO−, the receive level is at maximum. When GSR is connected to PWRO+, the level is minimum. The output transmission level is adjusted between 0 and −12 dB as GSR is adjusted (with an adjustable resistor) between PWRO+ and PWRO−.

Transmission levels are specified relative to the receive channel output under digital milliwatt conditions (i.e., when the digital input at PCM IN is the eight-code sequence specified in CCITT recommendation G.711).

TYPICAL APPLICATION DATA

output gain set design considerations (see Figure 9)

PWRO+ and PWRO− are low-impedance complementary outputs. The voltages at the nodes are:
V_{O+} at PWRO+
V_{O-} at PWRO−
$V_O = V_{O+} - V_{O-}$ (total differential response)

R1 and R2 are a gain-setting resistor network with the center tap connected to the GSR input.

A value greater than 10 kΩ and less than 100 kΩ for R1 + R2 is recommended because of the following:
The parallel combination of R1 + R2 and R_L sets the total loading.
The total capacitance at the GSR input and the parallel combination of R1 and R2 define a time constant which has to be minimized to avoid inaccuracies.

V_A represents the maximum available digital milliwatt output response (V_A = 3.06 V rms).

$$\text{Where } A = \frac{1 + (R1/R2)}{4 + (R1/R2)}$$

$$V_O = A \cdot V_A$$

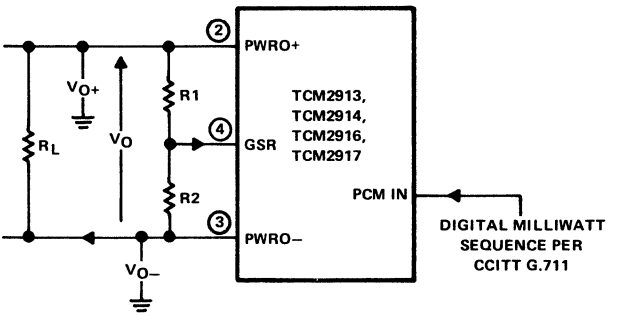


FIGURE 9. GAIN-SETTING CONFIGURATION

D2765, APRIL 1986 – REVISED JUNE 1988

- **Replaces Use of TCM2910A in Tandem with TCM2912C**
- **Reliable Silicon-Gate CMOS Technology**
- **Low Power Consumption:**
  Operating Mode . . . 80 mW Typical
  Power-Down Mode . . . 5 mW Typical
- **Excellent Power Supply Rejection Ratio Over Frequency Range of 0 to 50 kHz**
- **No External Components Needed for Sample, Hold, and Auto-Zero Functions**
- **Precision Internal Voltage References**
- **Direct Replacement for Intel 2913, 2914, 2916, and 2917**
- **TCM29C13N-3 is Primarily Used for Low-Cost DSP Applications with TMS320CXX**

FEATURE TABLE

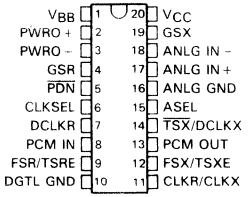
FEATURE	129C13 29C13	129C14 29C14	129C16 29C16	129C17 29C17
Number of Pins:				
24		X		
20	X			
16			X	X
μ-law/A-law Coding:				
μ-law	X	X	X	
A-law	X	X		X
Data Timing Rates:				
Variable Mode				
64 kHz to 2.048 MHz	X	X	X	X
Fixed Mode				
1.536 MHz	X	X		
1.544 MHz	X	X		
2.048 MHz	X	X	X	X
Loopback Test Capability		X		
8th-Bit Signaling				

description

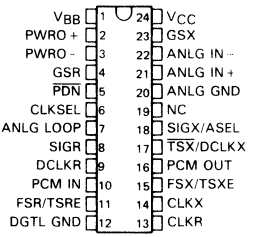
The TCM129C13, TCM129C14, TCM129C16, TCM129C17, TCM29C13, TCM29C14, TCM29C16, and TCM29C17 are single-chip pulse-code-modulated encoders and decoders (PCM codecs) and PCM line filters. These devices provide all the functions required to interface a full-duplex (4-wire) voice telephone circuit with a time-division-multiplexed (TDM) system. These devices are intended to replace the TCM2910A in tandem with the TCM2912C. Primary applications of the devices include:

- Line Interface for Digital Transmission and Switching of T1 Carrier, PABX, and Central Office Telephone Systems
- Subscriber Line Concentrators
- Digital Encryption Systems
- Digital Voice Band Data Storage Systems
- Digital Signal Processing

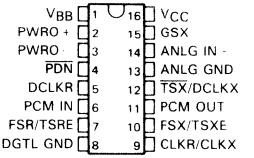
TCM129C13 . . . DW, DY, J, OR N PACKAGE
TCM29C13 . . . DW, DY, J, OR N PACKAGE
TCM29C13N-3 . . . N PACKAGE
(TOP VIEW)



TCM129C14 . . . DW OR JW PACKAGE
TCM29C14 . . . DW OR JW PACKAGE
(TOP VIEW)



TCM129C16, TCM129C17 . . . J OR N PACKAGE
TCM29C16, TCM29C17 . . . J OR N PACKAGE
(TOP VIEW)



Caution. These devices have limited built-in gate protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

description (continued)

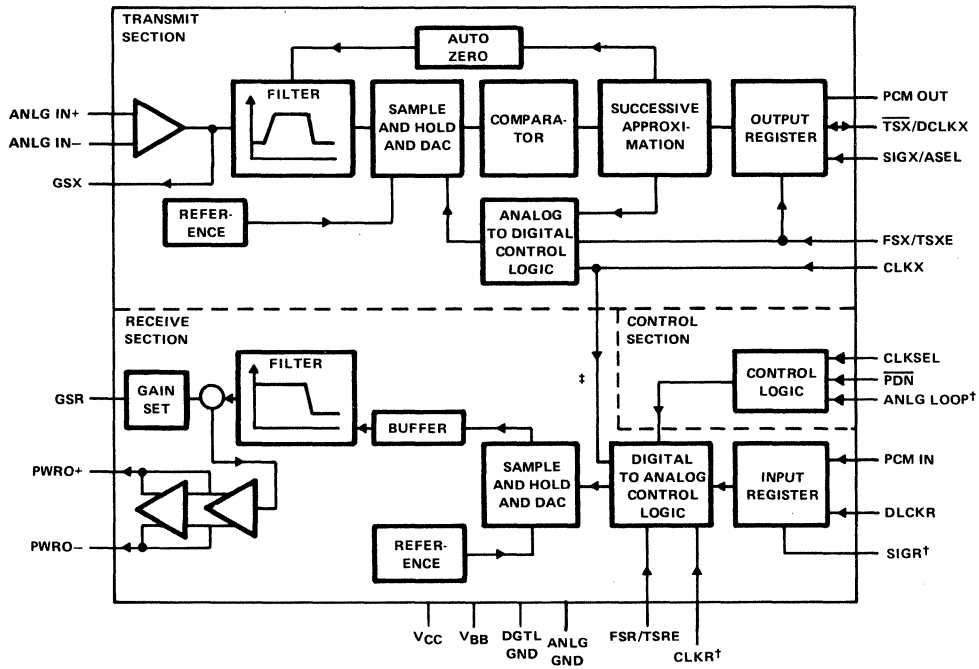
These devices are designed to perform the transmit encoding (A/D conversion) and receive decoding (D/A conversion) as well as the transmit and receive filtering functions in a pulse-code-modulated system. They are intended to be used at the analog termination of a PCM line or trunk.

The TCM129C13, TCM129C14, TCM129C16, TCM129C17, TCM29C13, TCM29C14, TCM29C16, and TCM29C17 provide the bandpass filtering of the analog signals prior to encoding and after decoding. These combination devices perform the encoding and decoding of voice and call progress tones as well as the signaling and supervision information.

The TCM29C13N-3 is the same as the TCM29C13N except for certain parameters as indicated in the specification section.

The TCM129C13, TCM129C14, TCM129C16, and TCM129C17 are characterized for operation from −40°C to 85°C. The TCM29C13, TCM29C14, TCM29C16, and TCM29C17 are characterized for operation from 0°C to 70°C.

functional block diagram



†TCM129C14 and TCM29C14 only
‡TCM129C13, TCM129C16, TCM129C17, TCM29C13, TCM29C16, and TCM29C17 only.

PIN			NAME	DESCRIPTION
TCM129C13 TCM29C13	TCM129C14 TCM29C14	TCM129C16 TCM129C17 TCM29C16 TCM29C17		
1	1	1	V_{BB}	Most negative supply voltage; input is −5 V ±5%.
2	2	2	PWRO+	Noninverting output of power amplifier. Can drive transformer hybrids or high-impedance loads directly in either a differential or a single-ended configuration.
3	3	3	PWRO−	Inverting output of power amplifier; functionally identical with and complementary to PWRO+.
4	4		GSR	Input to the gain-setting network on the output power amplifier. Transmission level can be adjusted over a 12-dB range depending upon the voltage at GSR.
5	5	4	$\overline{PDN}$	Power-down select. The device is inactive with a TTL low-level input to this pin and active with a TTL high-level input to the pin.
6	6		CLKSEL	Clock frequency selection. Input must be connected to V_{BB}, V_{CC}, or ground to reflect the master clock frequency. When tied to V_{BB}, CLK is 2.048 MHz. When tied to ground, CLK is 1.544 MHz. When tied to V_{CC}, CLK is 1.536 MHz.
	7		ANLG LOOP	Provides loopback test capability. When this input is high, PWRO+ is internally connected to ANLG IN.
	8		SIGR	Signaling bit output, receive channel; in a fixed-data-rate mode, outputs the logical state of the 8th bit (LSB) of the PCM word in the most recent signaling frame.
7	9	5	DCLKR	Selects fixed or variable data-rate operation. When this pin is connected to V_{BB}, the device operates in the fixed-data-rate mode. When DCLKR is not connected to V_{BB}, the device operates in the variable-data-rate mode, and DCLKR becomes the receive data clock, which operates at frequencies from 64 kHz to 2.048 MHz
8	10	6	PCM IN	Receive PCM input. PCM data is clocked in on this pin on eight consecutive negative transitions of the receive data clock, which is CLKR in fixed-data-rate timing and DCLKR in variable-data-rate timing.
9	11	7	FSR/TSRE	Frame synchronization clock input/time slot enable for receive channel. In the fixed-data-rate mode, FSR distinguishes between signaling and non-signaling frames by a double- or single-length pulse, respectively. In the variable-data-rate mode, this signal must remain high for the duration of the timeslot. The receive channel enters the standby state when FSR is TTL low for 300 ms.
10	12	8	DGTL GND	Digital ground for all internal logic circuits. Not internally connected to ANLG GND.
11	13	9	CLKR	Receive master clock and data clock for the fixed-data-rate mode. Receive master clock only for variable-data-rate mode. CLKR and CLKX are internally connected together for TCM129C13, TCM129C16, TCM129C17, TCM29C13, TCM29C16, and TCM29C17.

PIN			NAME	DESCRIPTION
TCM129C13 TCM29C13	TCM129C14 TCM29C14	TCM129C16 TCM129C17 TCM29C16 TCM29C17		
11	14	9	CLKX	Transmit master clock and data clock for the fixed-data-rate mode. Transmit master clock only for variable data rate mode. CLKR and CLKX are internally connected for the TCM129C13, TCM129C16, TCM129C17, TCM29C13, TCM29C16, and TCM29C17.
12	15	10	FSX/TSXE	Frame synchronization clock input/time-slot enable for transmit channel. Operates independently of, but in an analagous manner to, FSR/TSRE. The transmit channel enters the standby state when FSX is low for 300 ms.
13	16	11	PCM OUT	Transmit PCM output. PCM data is clocked out on this output on eight consecutive positive transitions of the transmit data clock, which is CLKX in fixed-data-rate timing and DCLKX in variable-data-rate timing.
14	17	12	$\overline{\text{TSX}}$/DCLKX	Transmit channel time slot strobe (output) or data clock (input) for the transmit channel. In the fixed-data-rate mode, this pin is an open-drain output to be used as an enable signal for a three-state buffer. In the variable-data rate mode, DCLKX becomes the transmit data clock, which operates at TTL levels from 64 kHz to 2.048 MHz.
15	18		SIGX/ASEL	Used to select between A-law and μ-law operation. When connected to V_{BB}, A-law is selected. When connected to V_{CC} or ground, u-law is selected. When not connected to V_{BB}, it is a TTL-level input that is transmitted as the eighth bit (LSB) of the PCM word during signaling frames on the PCM OUT pin (TCM129C14 and TCM29C14 only). SIGX/ASEL is internally connected to provide μ-law operation for TCM129C16 and TCM29C16 and A-law operation for TCM129C17 and TCM29C17.
16	20	13	ANLG GND	Analog ground return for all internal voice circuits. Not internally connected to DGTL GND.
17	21		ANLG IN+	Noninverting analog input to uncommitted transmit operational amplifier. Internally connected to ANLG GND on TCM129C16, TCM29C16, TCM129C17, and TCM29C17.
18	22	14	ANLG IN−	Inverting analog input to uncommitted transmit operational amplifier.
19	23	15	GSX	Output terminal of internal uncommitted operational amplifier. Internally, this is the voice signal input to the transmit filter.
20	24	16	V_{CC}	Most positive supply voltage, input is 5 V ± 5%.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . −0.3 V to 15 V
Output voltage, V_O . . . . . −0.3 V to 15 V
Input voltage, V_I . . . . . −0.3 V to 15 V
Digital ground voltage . . . . . −0.3 V to 15 V
Continuous total dissipation at (or below) 25°C free-air temperature . . . . . 1375 mW
Operating free-air temperature range: TCM129C_ . . . . . −40°C to 85°C
TCM29C_ . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW, DY, or N package . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J or JW package . . . . . 300°C

NOTES: 1. Voltage values for maximum ratings are with respect to V_{BB}.

recommended operating conditions (see Note 2)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (see Note 3)		4.75	5	5.25	V
V_{BB}	Supply voltage		−4.75	−5	−5.25	V
	DGTL GND voltage with respect to ANLG GND			0		V
V_{IH}	High-level input voltage, all inputs except CLKSEL		2.2			V
V_{IL}	Low-level input voltage, all inputs except CLKSEL				0.8	V
	Clock select input voltage	For 2.048 MHz	V_{BB}		V_{BB}+0.5	V
		For 1.544 MHz	0		0.5	
		For 1.536 MHz	V_{CC}−0.5		V_{CC}	
R_L	Load resistance	At GSX	10			kΩ
		At PWRO+ and/or PWRO−	300			Ω
C_L	Load capacitance	At GSX			50	pF
		AT PWRO+ and/or PWRO−			100	
T_A	Operating free-air temperature	TCM129C_	−40		85	°C
		TCM29C_	0		70	

NOTES: 2. To avoid any possible damage and reliability problems to these CMOS devices when applying power, the following sequence should be followed:
(1) Connect ground
(2) Connect the most negative voltage
(3) Connect the most positive voltage
(4) Connect the input signals
When powering down the device, follow the above steps in reverse order. If the above procedure cannot be followed, connect a diode between V_{BB} and digital ground, cathode to DGND, anode to V_{BB}.
3. Voltages at analog inputs and outputs, V_{CC}, and V_{BB} terminals are with respect to the ANLG GND terminal. All other voltages are referenced to the DGTL GND terminal unless otherwise noted.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature

supply current, f_{DCLK} = 2.048 MHz, outputs not loaded

PARAMETER‡		TEST CONDITIONS	TCM129C__ __ TYP†	TCM129C__ __ MAX	TCM29C__ __ TYP†	TCM29C__ __ MAX	UNIT
I_{CC} Supply current from V_{CC}	Operating		8	13	7	9	mA
	Standby	FSX or FSR at V_{IL} after 300 ms	0.7	1.5	0.5	1	
	Power-down	$\overline{PDN}$ V_{IL} after 10 μs	0.4	1	0.3	0.8	
I_{BB} Supply current from V_{BB}	Operating		−8	−13	−7	−9	mA
	Standby	FSX or FSR at V_{IL} after 300 ms	−0.7	−1.5	−0.5	−1	
	Power-down	$\overline{PDN}$ V_{IL} after 10 μs	−0.4	−1	−0.3	−0.8	
Power dissipation	Operating		80	130	70	90	mW
	Standby	FSX or FSR at V_{IL} after 300 ms	7	15	5	10	
	Power down	$\overline{PDN}$ V_{IL} after 10 μs	4	10	3	8	

digital interface

PARAMETER			TEST CONDITONS	TCM129C__ __ MIN	TYP†	MAX	TCM29C__ __ MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	PCM out	I_{OH} = −9.6 mA	2.4			2.4			V
		SIGR	I_{OH} = −1.2 mA	2.4			2.4			
V_{OL}	Low-level output voltage at PCM out, TSX, SIGR		I_{OL} = 3.2 mA			0.5			0.4	V
I_{IH}	High-level input current, any digital input		V_I = 2.2 V to V_{CC}			12			10	μA
I_{IL}	Low-level input current, any digial input		V_I = 0 to 0.8 V			12			10	μA
C_i	Input capacitance				5	10		5	10	pF
C_o	Output capacitance				5			5		pF

transmit amplifier input

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input current at ANLG IN+, ANLG IN−	V_I = −2.17 V to 2.17 V			±100	nA
Input offset voltage at ANLG IN+, ANLG IN−	V_I = −2.17 V to 2.17 V			±25	mV
Common-mode rejection at ANLG IN+, ANLG IN−	V_I = −2.17 V to 2.17 V	55			dB
Open-loop voltage amplification at GSX		5000			
Open-loop unity-gain bandwidth at GSX			1		MHz
Input resistance at ANLG IN+, ANLG IN−		10			MΩ

receive filter output

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Output offset voltage PWRO+, PWRO− (single-ended)	Relative to ANLG GND		80		mV
Output resistance at PWRO+, PWRO−			1		Ω

†All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C.

gain and dynamic range, V_{CC} = 5 V, V_{BB} = −5 V, T_A = 25°C (unless otherwise noted) (see Notes 4, 5, and 6)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Encoder milliwatt response (transmit gain tolerance)		Signal input = 1.064 V rms for μ-law	Standard version		±0.04	±0.2	dBm0
		Signal input = 1.068 V rms for A-law	TCM29C13N-3		±0.2	±0.5	
Encoder milliwatt response (nominal supplies and temperature)		T_A = 0°C to 70°C, Supplies = ±5%				±0.08	dB
Digital milliwatt response (receive tolerance gain) relative to zero-transmission level point		Signal input per CCITT G.711, Output signal = 1 kHz	Standard version		±0.04	±0.2	dBm0
			TCM29C13N-3		±0.2	±0.5	
Digital milliwatt response variation with temperature and supplies		T_A = 0°C to 70°C, Supplies = ±5%				±0.08	dB
Zero-transmission-level point, transmit channel (0 dBm0)	μ-law	R_L = 600 Ω			2.76		dBm
	A-law				2.79		
	μ-law	R_L = 900 Ω			1.00		
	A-law				1.03		
Zero-transmission-level point, receive channel (0 dBm0)	μ-law	R_L = 600 Ω			5.76		dBm
	A-law				5.79		
	μ-law	R_L = 900 Ω			4.00		
	A-law				4.03		

NOTES: 4. Unless otherwise noted, the analog input is a 0-dBm0, 1020-Hz sine wave, where 0 dBm0 is defined as the zero-reference point of the channel under test. This corresponds to an analog signal input of 1.064 V rms, or an output of 1.503 V rms.
5. The input amplifier is set for unity gain, noninverting. The digital input is a PCM bit stream generated by passing a 0-dBm0, 1020-Hz sine wave through an ideal encoder.
6. Receive output is measured single-ended in the maximum-gain configuration. To set the output amplifier for maximum gain, GSR is connected to PWRO− and the output is taken at PWRO+. All output levels are (sin x)/x corrected.

gain tracking over recommended ranges of supply voltage and operating free-air temperature, reference level = −10 dBm0

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Transmit gain tracking error, sinusoidal input	3 to −40 dBm0		±0.25	dB
	−40 to −50 dBm0		±0.5	
	−50 to −55 dBm0		±1.2	
Receive gain tracking error, sinusoidal input	3 to −40 dBm0		±0.25	dB
	−40 to −50 dBm0		±0.5	
	−50 to −55 dBm0		±1.2	

noise over recommended ranges of supply voltage and operating free-air temperature

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Transmit noise, C-message weighted	ANLG IN+ = ANLG GND, ANLG IN− = GSX		15	dBrnC0
Transmit noise, C-message weighted with eighth-bit signaling (TCM129C14 and TCM29C14 only)	ANLG IN+ = ANLG GND, ANLG IN− = GSX, 6th frame signaling		18	dBrnC0
Transmit noise, psophometrically weighted	ANLG IN+ = ANLG GND, ANLG IN− = GSX		−75	dBm0p
Receive noise, C-message weighted quiet code	PCM IN = 11111111 (μ-law) PCM IN = 10101010 (A-law) measured at PWRO+		11	dBrnC0
Receive noise, C-message weighted sign bit toggled	Input to PCM IN is zero code with sign bit toggled at 1-kHz rate		12	dBrnC0
Receive noise, psophometrically weighted	PCM = lowest positive decode level		−79	dBm0p

power supply rejection and crosstalk attenuation over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{CC} supply voltage rejection ratio, transmit channel	f = 0 to 30 kHz	Idle channel, supply signal = 200 mV p-p, f measured at PCM OUT		−30		dB
	f = 30 to 50 kHz			−45		
V_{BB} supply voltage rejection ratio, transmit channel	f = 0 to 30 kHz	Idle channel, supply signal = 200 mV p-p, f measured at PCM OUT		−30		dB
	f = 30 to 50 kHz			−55		
V_{CC} supply voltage rejection ratio, receive channel (single-ended)	f = 0 to 30 kHz	Idle channel, supply signal = 200 mV p-p, narrow-band, f measured at PWRO+		−20		dB
	f = 30 to 50 kHz			−45		
V_{BB} supply voltage rejection ratio, receive channel (single-ended)	f = 0 to 30 kHz	Idle channel, supply signal = 200 mV p-p, narrow-band, f measured at PWRO+		−20		dB
	f = 30 to 50 kHz			−45		
Crosstalk attenuation, transmit-to-receive (single-ended)		ANLG IN+ = 0 dBm0, f = 1.02 kHz, unity gain, PCM IN = lowest decode level, measured at PWRO+	71			dB
Crosstalk attenuation, receive-to-transmit (single-ended)		PCM IN = 0 dBm0, f = 1.02 kHz, Measured at PCM OUT	71			dB

†All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C.

distortion over recommended ranges of supply voltage and operating free-air temperature

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Transmit signal to distortion ratio, sinusoidal input (CCITT G.712 – Method 2)	ANLG IN+ = 0 to −30 dBm0	36			dB
	ANLG IN+ = −30 to −40 dBm0	30			
	ANLG IN+ = −40 to −45 dBm0	25			
Receive signal to distortion ratio, sinusoidal input (CCITT G.712 – Method 2)	ANLG IN+ = 0 to −30 dBm0	36			dB
	ANLG IN+ = −30 to −40 dBm0	30			
	ANLG IN+ = −40 to −45 dBm0	25			
Transmit single-frequency distortion products	AT&T Advisory #64 (3.8), Input signal = 0 dBm0			−46	dBm0
Receive single-frequency distortion products	AT&T Advisory #64 (3.8), Input signal = 0 dBm0			−46	dBm0
Intermodulation distortion, end-to-end Spurious out-of-band signals, end-to-end	CCITT G.712 (7.1)			−35	dBm0
	CCITT G.712 (7.2)			−49	
	CCITT G.712 (6.1)			−25	dBm0
	CCITT G.712 (9)			−40	
Transmit absolute delay time to PCM OUT	Fixed data rate, f_{CLKX} = 2.048 MHz, Input to ANLG IN+ 1.02 kHz at 0 dBm0		245		μs
Transmit differential envelope delay time relative to transmit absolute delay time	f = 500 Hz to 600 Hz		170		μs
	f = 600 Hz to 1000 Hz		95		
	f = 1000 Hz to 2600 Hz		45		
	f = 2600 Hz to 2800 Hz		105		
Receive absolute delay time to PWRO+	Fixed data rate, f_{CLKR} = 2.048 MHz, Digital input is DMW codes		190		μs
Receive differential envelope delay time relative to transmit absolute delay time	f = 500 Hz to 600 Hz		45		μs
	f = 600 Hz to 1000 Hz		35		
	f = 1000 Hz to 2600 Hz		85		
	f = 2600 Hz to 2800 Hz		110		

† All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C.

transmit filter transfer over recommended ranges of supply voltage and operating free-air temperature (see Figure 1)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Gain relative to gain at 1.02 kHz	Input amplifier set for unity gain, Noninverting maximum gain output, Input signal at ANLG IN+ is 0 dBm0	16.67 Hz		−30	dB
		50 Hz		−25	
		60 Hz		−23	
		200 Hz	−1.8	−0.125	
		300 Hz to 3 kHz	−0.15	0.15	
		3.3 kHz	−0.35	0.03	
		3.4 kHz	−1	−0.1	
		4 kHz		−14	
		4.6 kHz and above		−32	
		3.4 kHz (TCM29C13N-3 only)	−1.4	−0.1	

receive filter transfer over recommended ranges of supply voltage and operating free-air temperature (see Figure 2)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Gain relative to gain at 1.02 kHz	Input signal at PCM IN is 0 dBm0	Below 200 Hz		0.15	dB
		200 Hz	−0.5	0.15	
		300 Hz to 3 kHz	−0.15	0.15	
		3.3 kHz	−0.35	0.03	
		3.4 kHz	−1	−0.1	
		4 kHz		−14	
		4.6 kHz and above		−30	
		3.4 kHz (TCM29C13N-3 only)	−1.4	−0.1	

clock timing requirements over recommended ranges of supply voltage and operating free-air temperature (see timing diagrams)

	PARAMETER	MIN	TYP†	MAX	UNIT
$t_{c(CLK)}$	Clock period for CLKX, CLKR (2.048-MHz systems)	488			ns
t_r, t_f	Rise and fall times for CLKX and CLKR	5		30	ns
$t_{w(CLK)}$	Pulse duration for CLKX and CLKR (see Note 7)	220			ns
$t_{w(DCLK)}$	Pulse duration for DCLK (f_{DCLK} = 64 Hz to 2.048 MHz) (see Note 7)	220			ns
	Clock duty cycle [$t_{w(CLK)}/t_{c(CLK)}$] for CLKX and CLKR	45	50	55	%

† All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C.

transmit timing requirements over recommended ranges of supply voltage and operating free-air temperature, fixed-data-rate mode (see timing diagrams)

	PARAMETER	MIN	MAX	UNIT
$t_{d(FSX)}$	Frame sync delay time	100	$t_{c(CLK)}-100$	ns
$t_{su(SIGX)}$	Setup time before Bit 7 falling edge (TCM129C14 and TCM29C14 only)	0		ns
$t_{h(SIGX)}$	Hold time after Bit 8 falling edge (TCM129C14 and TCM29C14 only)	0		ns

propagation delay times over recommended ranges of operating conditions, fixed-data-rate mode (see timing diagrams)

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{pd1}	From rising edge of transmit clock to Bit 1 data valid at PCM OUT (data enable time on time slot entry) (see Note 8)	C_L = 0 to 100 pF	0	145	ns
t_{pd2}	From rising edge of transmit clock Bit n to Bit n + 1 data valid at PCM OUT (data valid time)	C_L = 0 to 100 pF	0	145	ns
t_{pd3}	From falling edge of transmit clock Bit 8 to Bit 8 Hi-Z at PCM OUT (data float time on time slot exit) (see Note 8)	C_L = 0	60	215	ns
t_{pd4}	From rising edge of transmit clock Bit 1 to TSX active (low) (time slot enable time)	C_L = 0 to 100 pF	0	145	ns
t_{pd5}	From falling edge of transmit clock Bit 8 to TSX inactive (high) (timeslot disable time) (see Note 8)	C_L = 0	60	190	ns
t_{pd6}	From rising edge of channel time slot to SIGR update (TCM129C14 and TCM29C14 only)		0	2	μs

NOTES: 7. FSX CLK must be phase locked with the CLKX, FSR CLK must be phase locked with CLKR.
8. Timing parameters t_{pd1}, t_{pd3}, and t_{pd5} are referenced to the high-impedance state.

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receive timing requirements over recommended ranges of supply voltage and operating free-air temperature, fixed-data-rate mode (see timing diagrams)

PARAMETER		MIN	MAX	UNIT
$t_{d(FSR)}$	Frame sync delay time	100	$t_{c(CLK)}-100$	ns
$t_{su(PCM\ IN)}$	Setup time before Bit 7 falling edge (TCM129C14 and TCM29C14 only)	10		ns
$t_{h(PCM\ IN)}$	Hold time after Bit 8 falling edge (TCM129C14 and TCM29C14 only)	60		ns

transmit timing requirements over recommended ranges of supply voltage and operating free-air temperature, variable-data-rate mode (see timing diagrams)

PARAMETER		MIN	MAX	UNIT
$t_{d(TSDX)}$	Timeslot delay time from DCLKX (see Note 9)	140	$t_{d(DCLKX)}-140$	ns
$t_{d(FSX)}$	Frame sync delay time	100	$t_{c(CLK)}-100$	ns
$t_{c(DCLKX)}$	Clock period for DCLKX	488	15620	kHz

propagation delay times over recommended ranges of operating conditions, variable-data-rate mode (see Note 10 and timing diagrams)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{pd7}	Data delay time from DCLKX	C_L = 0 to 100 pF	0	100	ns
t_{pd8}	Data delay from timeslot enable to PCM OUT	C_L = 0 to 100 pF	0	50	ns
t_{pd9}	Data delay from time slot disable to PCM OUT	C_L = 0 to 100 pF	0	80	ns
t_{pd10}	Data delay time from FSX	$t_{d(TSDX)}$ = 80 ns	0	140	ns

receive timing requirements over recommended ranges of supply voltage and operating free-air temperature, variable-data-rate mode (see timing diagrams)

PARAMETER		MIN	MAX	UNIT
$t_{d(TSDR)}$	Timeslot delay time from DCLKR (see Note 11)	140	$t_{d(DCLKR)}-140$	ns
$t_{d(FSR)}$	Frame sync delay time	100	$t_{c(CLK)}-100$	ns
$t_{su(PCM\ IN)}$	Setup time before Bit 7 falling edge	10		ns
$t_{h(PCM\ IN)}$	Hold time after Bit 8 falling edge	60		ns
$t_{c(DCLKR)}$	Data clock frequency	488	15620	ns
$t_{(SER)}$	Timeslot end receive time	0		ns

64-kilobit operation timing requirements over recommended ranges of supply voltage and operating free-air temperature, variable-data-rate mode

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{FSLX}	Transmit frame sync minimum down time	FSX = TTL high for remainder of frame	488		ns
t_{FSLR}	Receive frame sync minimum down time	FSR = TTL high for remainder of frame	1952		ns
t_{DCLK}	Pulse duration, data clock			10	μs

NOTES: 9. t_{FSLX} minimum requirement overrides the $t_{d(TSDX)}$ maximum requirement for 64-kHz operation.
10. Timing parameters t_{pd8} and t_{pd9} are referenced to a high-impedance state.
11. t_{FSLR} minimum requirement overrides the $t_{d(TSDR)}$ maximum requirement for 64-kHz operation.

CLK, CLKR, and CLKX Selection Requirements for DSP Based Applications

1) It should be noted that the CLKX, CLKR, CLK must be selected as follows:

CLKSEL PIN	CLK, CLKR, CLKX (BETWEEN 1.0 MHz to 3.0 MHz)	DEVICE TYPE
−5 V†	= (256) × (Frame Sync Frequency)	TCM129C13/14/16/17
		TCM29C13/14/16/17
0 V	= (193) × (Frame Sync Frequency)	TCM129C13/14
		TCM29C13/14
+5 V	= (192) × (Frame Sync Frequency)	TCM129C13/14
		TCM29C13/14

E.G.: For Frame Sync Frequency = 9.6 kHz

CLKSEL PIN	CLK, CLKR, CLKX (BETWEEN 1.0 MHz to 3.0 MHz)	DEVICE TYPE
−5 V†	=2.4576 MHz	TCM129C13/14/16/17
		TCM29C13/14/16/17
0 V	= 1.8528 MHz	TCM129C13/14
		TCM29C13/14
+5 V	= 1.8432 MHz	TCM129C13/14
		TCM29C13/14

†CLKSEL is internally set to −5 V for TCM129C16/17 and TCM29C16/17.

2) Corner frequency at 8 kHz Frame Sync Frequency = 3kHz

Therefore, the corner frequency = (3/8) × (Frame Sync Frequency). (For nonstandard frame sync.)

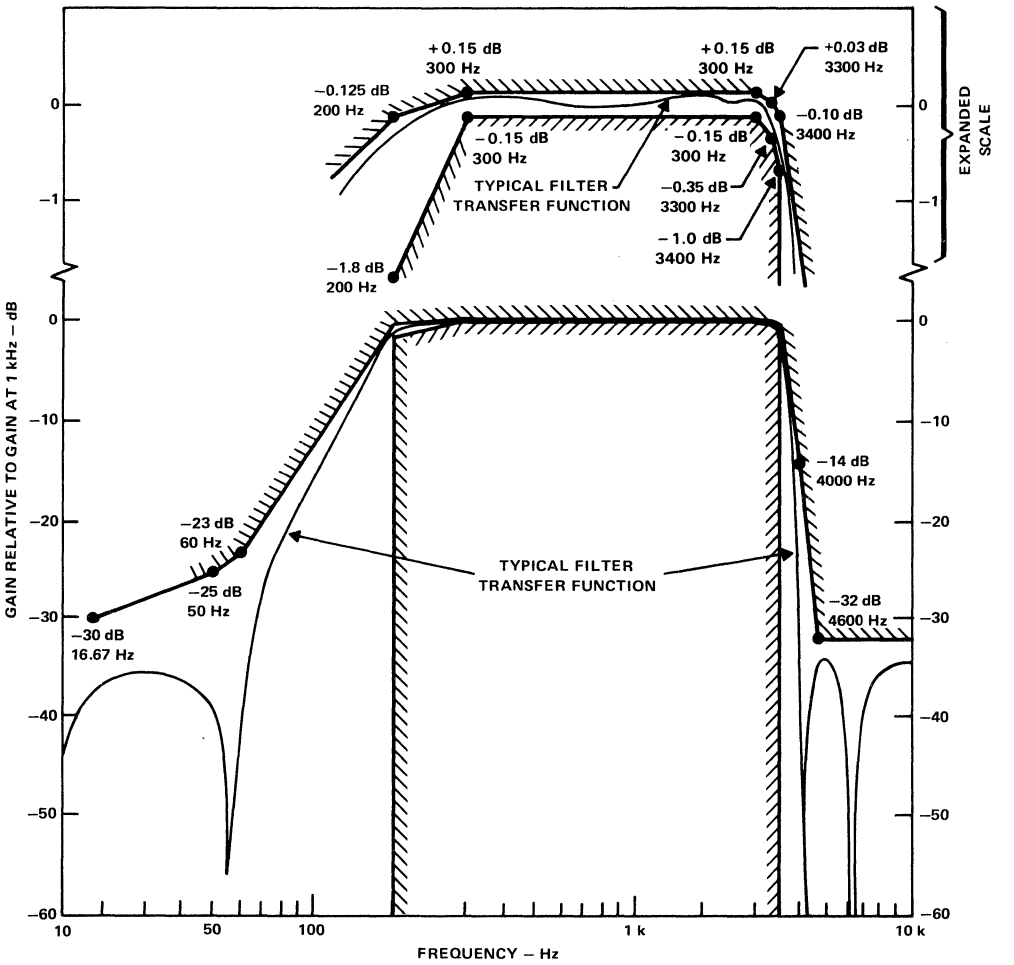
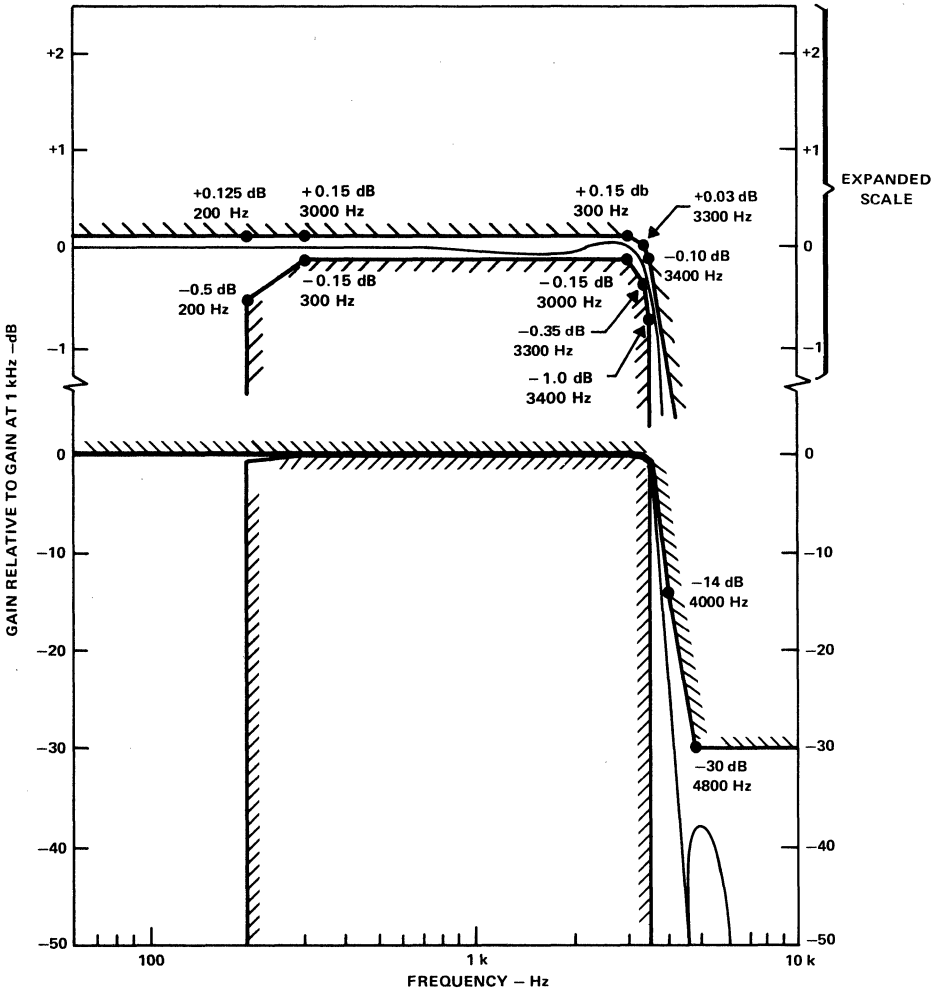


FIGURE 1. TRANSFER CHARACTERISTICS OF THE TRANSMIT FILTER



NOTE: This is a typical transfer function of the receive filter component.

FIGURE 2. TRANSFER CHARACTERISTIC OF THE RECEIVE FILTER

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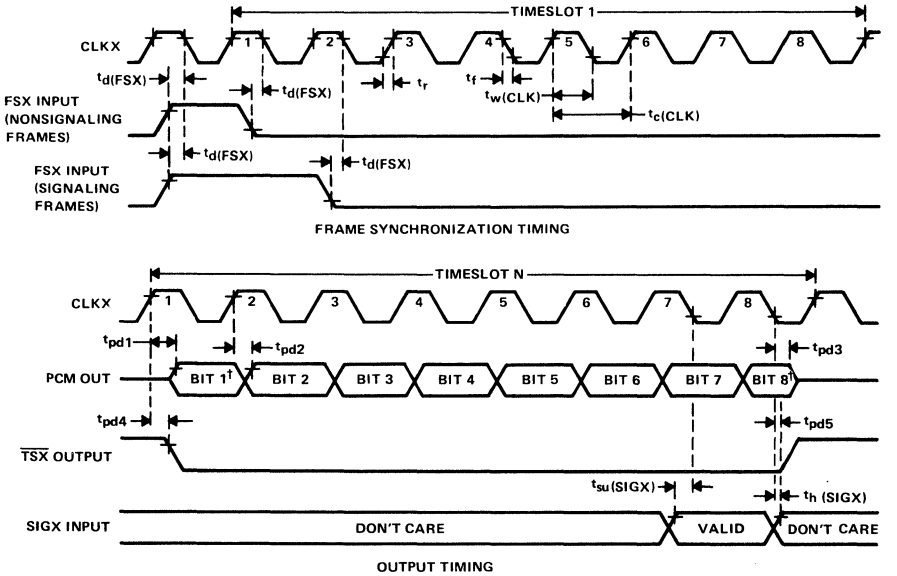


FIGURE 3. TRANSMIT TIMING (FIXED-DATA-RATE)

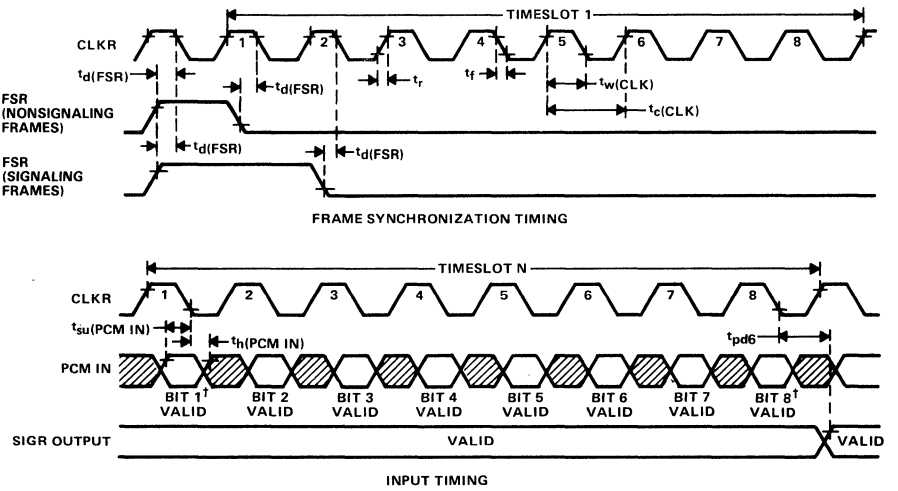


FIGURE 4. RECEIVE TIMING (FIXED-DATA-RATE)

NOTE: Inputs and driven from 0.45 V to 2.4 V. Time intervals are referenced to 2 V if the high level is indicated and 0.8 V if the low level is indicated.

†Bit 1 = MSB = SIGN BIT and is clocked in first on the PCM-IN pin or clocked out first on the PCM-OUT pin. BIT 8 = LSB = LEAST SIGNIFICANT BIT and is clocked in last on the PCM-IN pin or is clocked out last on the PCM-OUT pin.

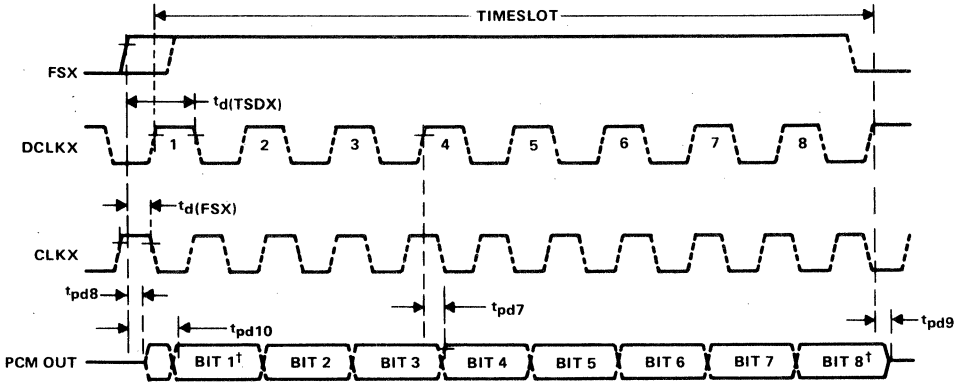
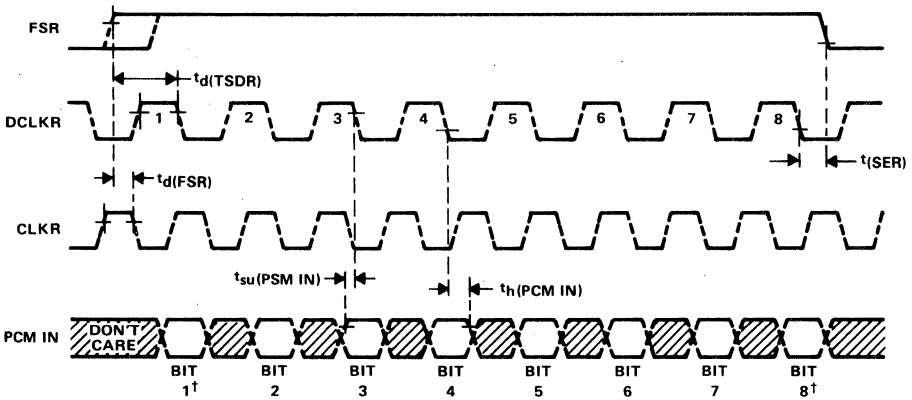


FIGURE 5. TRANSMIT TIMING (VARIABLE-DATA-RATE)



NOTE: All timing parameters referenced to V_{IH} and V_{IL} except t_{pd8} and t_{pd9}, which reference a high-impedance state.

FIGURE 6. RECEIVE TIMING (VARIABLE-DATA-RATE)

NOTE: All timing parameters, referenced to V_{IH} and V_{IL} except t_{pd8} and t_{pd9}, which reference a high-impedance state.
†Bit 1 = MSB = SIGN BIT and is clocked in first on the PCM-IN pin or clocked out first on the PCM-OUT pin. BIT 8 = LSB = LEAST SIGNIFICANT BIT and is clocked in last on the PCM-IN pin or is clocked out last on the PCM-OUT pin.

GENERAL OPERATION

system reliability features

The TCM129C13, TCM129C14, TCM129C16, TCM129C17, TCM29C13, TCM29C14, TCM29C16, and TCM29C17 are powered up in four steps:

V_{CC} and V_{BB} supply voltages are applied.
All clocks are connected.
TTL high is applied to $\overline{PDN}$.
FSX and/or FSR synchronization pulses are applied.

On the transmit channel, digital outputs PCM OUT and $\overline{TSX}$ are held in high-impedance state for approximately four frames (500 μs) after power up or application of V_{BB} or V_{CC}. After this delay, PCM OUT, $\overline{TSX}$, and signaling are functional and will occur in the proper timeslot. The analog circuits on the transmit side require approximately 60 ms to reach their equilibrium value due to the autozero circuit settling time. Thus valid digital information, such as for on/off hook detection, is available almost immediately, while analog information is available after some delay.

On the receive channel, the digital output SIGR is also held low for a maximum of four frames after power up or application of V_{BB} or V_{CC}. SIGR will remain low until it is updated by a signalling frame.

To further enhance system reliability, PCM OUT and $\overline{TSX}$ will be placed in a high-impedance state approximately 20 μs after an interruption of CLKX. SIGR will be held low approximately 20 μs after an interruption of CLKR. These interruptions could possible occur with some kind of fault condition.

power-down and standby operations

To minimize power consumption, a power-down mode and three standby modes are provided.

For power down, an external low signal is applied to the $\overline{PDN}$ pin. It is not sufficient to remove the high voltage to $\overline{PDN}$. In the absence of a signal, the $\overline{PDN}$ pin floats to high and the device remains active. In the power-down mode, the average power consumption is reduced to an average of 5 mW.

The standby modes give the user the option of putting the entire device on standby, putting only the transmit channel on standby, or putting only the receive channel on standby. To place the entire device on standby, both FSX and FSR are held at low. For transmit-only operation, FSX is high and FSR is held low. For receive-only operation, FSR is high and FSX is held low. See Table 1 for power down and standby procedures.

TABLE 1. POWER DOWN AND STANDBY PROCEDURES

DEVICE STATUS	PROCEDURE	TYPICAL POWER CONSUMPTION	DIGITAL OUTPUT STATUS
Power down	$\overline{PDN}$ low	3 mW	$\overline{TSX}$ and PCM OUT are in a high-impedance state; SIGR goes to low within 10 μs.
Entire device on standby	FSX and FSR are low	3 mW	$\overline{TSX}$ and PCM OUT are in a high-impedance state; SIGR goes to low within 300 ms.
Only transmit on standby	FSX is low FSR is high	40 mW	$\overline{TSX}$ and PCM OUT are placed in a high-impedance state within 300 ms.
Only receive on standby	FSR is low FSX is high	30 mW	SIGR is placed in a high-impedance state within 300 ms.

fixed-data-rate timing (see Figure 7)

Fixed-data-rate timing is selected by connecting DCLKR to V_{BB}. It uses master clocks CLKX and CLKR, frame synchronizer clocks FSX and FSR, and output $\overline{TSX}$. FSX and FSR are 8-kHz inputs that set the sampling frequency and distinguish between signaling and nonsignaling frames by their pulse durations. A frame synchronization pulse one master clock period long designates a nonsignaling frame, while a double-length sync pulse enables the signaling function (TCM129C14 and TCM29C14 only). Data is transmitted on the PCU OUT pin on the first eight positive transitions of CLKX following the rising edge of FSX. Data is received on the PCM IN pin on the first eight falling edges of CLKR following FSX. A digital-to-analog (D/A) conversion is performed on the received digital word and the resulting analog sample is held on an internal sample-and-hold capacitor until transferred to the receive filter.

The clock selection pin (CLKSEL) is used to select the frequency of CLKX and CLKR (TCM129C13, TCM129C14, TCM29C13, and TCM29C14 only). The TCM129C13, TCM129C14, TCM29C13, and TCM29C14 fixed-data-rate mode can operate with frequencies of 1.536 MHz, 1.544 MHz, or 2.048 MHz. The TCM129C16, TCM129C17, TCM29C16, and TCM29C17 fixed data rate mode operates at 2.048 MHz only.

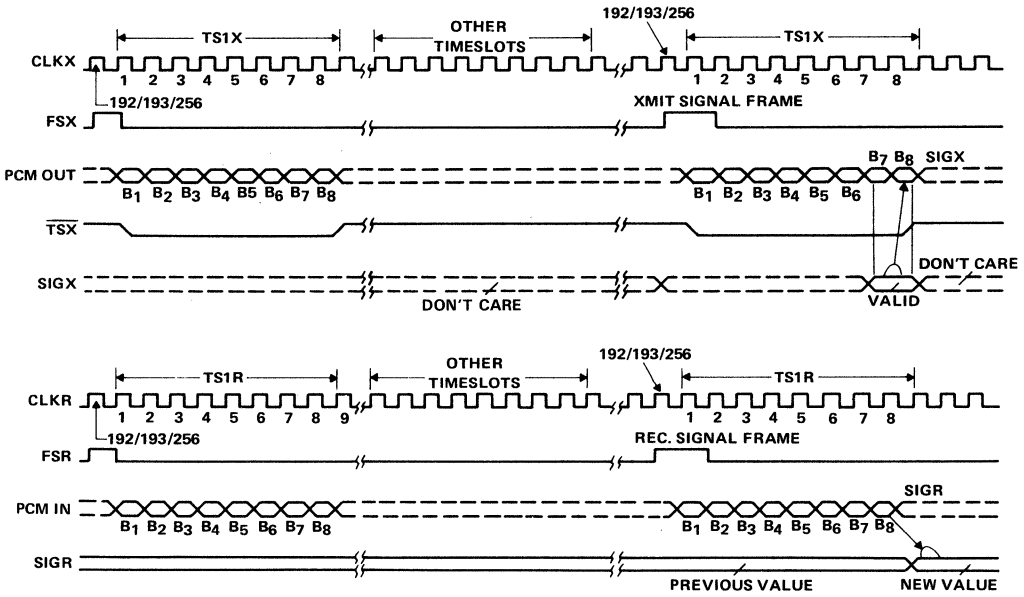


FIGURE 7. SIGNALING TIMING (FIXED-DATA-RATE ONLY)

variable data rate timing

Variable-data-rate timing is selected by connecting DCLKR to the bit clock for the receive PCM highway rather than to V_{BB}. It uses master clocks CLKX and CLKR, bit clocks DCLKX and DCLKR, and frame synchronization clocks FSX and FSR.

Variable-data-rate timing allows for a flexible data frequency. The frequency of the bit clocks can be varied from 64 kHz to 2.048 MHz. The bit clocks can be asynchronous in the TCM129C14 and TCM29C14, but must be synchronous in the TCM129C13, TCM129C16, TCM129C17, TCM29C13, TCM29C16, and TCM29C17. Master clocks in types TCM129C13, TCM129C14, TCM29C13, and TCM29C14 are restricted to frequencies of operation of 1.536 MHz, 1.544 MHz, or 2.048 MHz as in the fixed-data-rate timing mode. The master clock for the TCM129C16, TCM129C17, TCM29C16, and TCM29C17 is restricted to 2.048 MHz.

While FSX/TSXE input is high, PCM data is transmitted from PCM OUT onto the highway on the next eight consecutive positive transitions of DCLKX. Similarly, while the FSR/TSRE input is high, the PCM word is received from the highway by PCM IN on the next eight consecutive negative transitions of DCLKR.

The transmitted PCM word will be repeated in all remaining timeslots in the 125 μs frame as long as DCLKX is pulsed and FSX is held high. This feature, which allows the PCM word to be transmitted to the PCM highway more than once per frame, if desired, is available only with variable-data-rate timing. Signaling is allowed only in the fixed-data-rate mode because the variable-data-rate mode provides no means with which to specify a signaling frame.

signaling

The TCM29C14 (only) provides 8th-bit signaling in the fixed-data-rate timing mode. Transmit and receive signaling frames are independent of each other and are selected by a double-width frame sync pulse on the appropriate channel. During a transmit signaling frame, the signal present on SIGX is substituted for the least significant bit (LSB) of the encoded PCM word. In a receive signaling frame, the codec will decode the seven most significant bits in accordance with CCITT G.733 recommendations, and output the logical state of the LSB on the SIGR pin until it is updated in the next signaling frame. Timing relationships for signaling operations are shown n Figure 9. The signaling path is used to transmit digital signaling information such as ring control, rotary dial pulses, and off-hook and disconnect supervision. The voice path is used to transmit prerecorded messages as well as the call progress tones; dial tone, ring-back tone, busy tone, and re-order tone.

asynchronous operation

The TCM129C14 and TCM29C14 can be operated with asynchronous clocks in either the fixed- or variable-data-rate modes. In order to avoid crosstalk problems associated with special interrupt circuits, the design of the TCM129C13, TCM129C14, TCM29C13, and TCM29C14 includes separate digital-to-analog converters and voltage references on the transmit and receive sides to allow completely independent operation of the two channels.

In either timing mode, the master clock, data clock, and timeslot strobe must be synchronized at the beginning of each frame. Specifically, in the variable-data-rate mode the rising edge of CLKX must occur within $t_{d(FSX)}$ ns before the rise of FSX, while the leading edge of DCLKX must occur within t_{TSDX} ns of the rise of FSX. CLKX and DCLKX are synchronized once per frame but may be of different frequencies. The receive channel operates in a similar manner and is completely independent of the transmit timing (see variable data rate timing diagrams). This approach requires the provision of two separate master clocks but avoids the use of a synchronizer, which can cause intermittent data conversion errors.

analog loopback

A distinctive feature of the TCM129C14 and TCM29C14 is their analog loopback capability. With this feature, the user can test the line circuit remotely by comparing the signals sent into the receive channel (PCM IN) with those generated on the transmit channel (PCM OUT). The test is accomplished by sending a control signal that internally connects the analog input and output ports. WhenANLG LOOP is TTL high, the receive output (PWRO+) is internally connected to ANLG IN+, GSR is internally connected to PWRO−, and ANLG IN− is internally connected to GSX (see Figure 8).

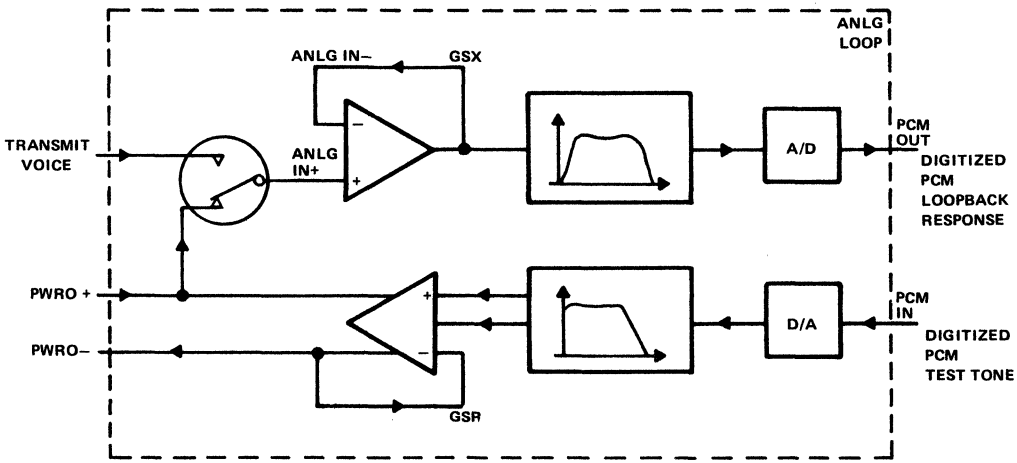


FIGURE 8. TCM129C14 AND TCM29C14 ANALOG LOOPBACK CONFIGURATION

Due to the difference in the transmit and receive transmission levels, a 0 dBmO code into PCM IN will emerge from PCM OUT as a 3-dBmO code, an implicit gain of 3 dB. Because of this, the maximum signal that can be tested by analog loopback is 0 dBmO.

precision voltage references

No external components are required with the devices to provide the voltage references. Voltage references that determine the gain and dynamic range characteristics of the device are generated internally. A difference in subsurface charge density between two suitably implanted MOS devices is used to derive a temperature- and bias-stable reference voltage. These references are calibrated during the manufacturing process.Separate references are supplied to the transmit and receive sections, and each is calibrated independently. Each reference value is then further trimmed in the gain setting operational amplifiers to a final precision value. Manufacturing tolerances can be achieved of typically ±0.04 dB in absolute gain for each half channel, providing the user a significant margin to compensate for error in other board components.

conversion laws

The TCM129C13, TCM129C14, TCM29C13, and TCM29C14 provide pin-selectable μ-law operation as specified by CCITT G.711 recommendation. A-law operation is selected when the ASEL pin is connected to V_{BB}. Signaling is not allowed during A-law operation. The TCM129C16 and TCM29C16 are μ-law only. The TCM129C17 and TCM29C17 are A-law only.

The μ-law operation is effectively selected by not selecting A-law operation. If the ASEL pin is connected to V_{CC} or GND, the device is in μ-law operation. If μ-law operation is selected, SIGX is a TTL-level input that can be used in the fixed data rate timing mode to modify the LSB of the PCM output is signaling frames.

transmit operation

transmit filter

The input section provides gain adjustment in the passband by means of an on-chip uncommitted operational amplifier. the load impedance to ground (ANLG GND) at the amplifier output (GSX) must be greater than 10 kΩ in parallel with less than 50 pF. The input signal on the ANLG IN + pin can be either ac or dc coupled. The input operational amplifier can also be used in the inverting mode or differential amplifier mode.

A low-pass antialiasing section is included on the device. This section provides 35-dB attenuation at the sampling frequency. No external components are required to provide the necessary antialiasing function for the switched capacitor section of the transmit filter.

The passband section provides flatness and stopband attenuation that fulfills the AT&T D3/D4 channel bank transmission specification and CCITT recommendation G.712. The device specifications meet or exceed digital class 5 central office switching systems requirements.

A high-pass section configuration was chosen to reject low-frequency noise from 50- and 60-Hz power lines, 17-Hz European electric railroads, ringing frequencies and their harmonics, and other low-frequency noise. Even with the high rejection at these frequencies, the sharpness of the band edge gives low attenuation at 200 Hz. This feature allows the use of low-cost transformer hybrids without external components.

encoding

The encoder internally samples the output of the transmit filter and holds each sample on an internal sample and hold capacitor. The encoder performs an analog-to-digital conversion on a switched capacitor array. Digital data representing the sample is transmitted on the first eight data clocks bits of the next frame.

The autozero circuit corrects for dc offset on the input signal to the encoder. The autozero circuit uses the sign bit averaging technique. The sign bit from the encoder output is long-term averaged and subtracted from the input to the encoder. All dc offset is removed from the encoder input waveform.

receive operation

decoding

The serial PCM word is received at the PCM IN pin on the first ight data clock bits of the frame. Digital-to-analog conversion is performed and the corresponding analog sample is held on an internal sample-and-hold capacitor. This sample is transferred to the receive filter.

receive filter

The receive section of the filter provides passband flatness and stopband rejection that fulfills both the AT&T D3/D4 specification and CCITT recommendation G.712. The filter contains the required compensation for the (sin x)/x response of such decoders.

receive output power amplifiers

A balanced output amplifier is provided to allow maximum flexibility in output configuration. Either of the two outputs can be used single-ended (i.e., referenced to ANLG GND) to drive single-ended loads. Alternatively, the differential output will directly drive a bridged load. The output stage is capable of driving loads as low as 300 ohms single-ended to a level of 12 dBm or 600 ohms differentially to a level of 15 dBm.

The receive channel transmission level may be adjusted between specified limits by manipulation of the GSR input. GSR is internally connected to an analog gain-setting network. When GSR is connected to PWRO−, the receive level is at maximum. When GSR is connected to PWRO+, the level is minimum. The output transmission level is adjusted between 0 and −12 dB as GSR is adjusted (with an adjustable resistor) between PWRO+ and PWRO−.

Transmission levels are specified relative to the receive channel output under digital milliwatt conditions (i.e., when the digital input at PCM IN is the eight-code sequence specified in CCITT recommendation G.711).

TYPICAL APPLICATION DATA

output gain set design considerations (see Figure 9)

PWRO+ and PWRO− are low-impedance complementary outputs. The voltages at the nodes are:

V_{O+} at PWRO+
V_{O-} at PWRO−
$V_{OD} = V_{O+} - V_{O-}$ (total differential response)

R1 and R2 are a gain-setting resistor network with the center tap connected to the GSR input.

A value greater than 10 kΩ and less than 100 kΩ for R1 + R2 is recommended because of the following:

The parallel combination of R1 + R2 and R_L sets the total loading.
The total capacitance at the GSR input and the parallel combination of R1 and R2 define a time constant that has to be minimized to avoid inaccuracies.

V_A represents the maximum available digital milliwatt output response (V_A = 3.06 V rms).

$$V_{OD} = A \cdot V_A$$

$$\text{Where } A = \frac{1 + (R1/R2)}{4 + (R1/R2)}$$

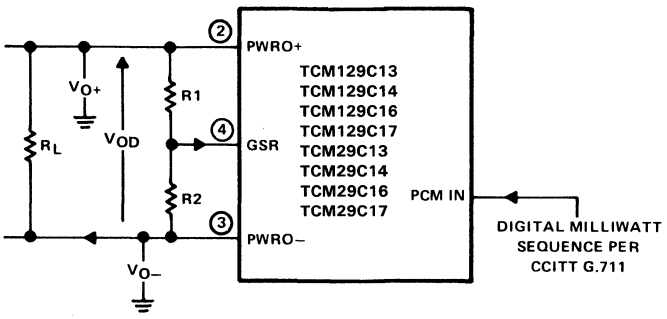
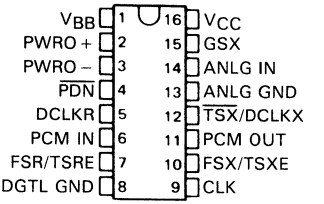


FIGURE 9. GAIN-SETTING CONFIGURATION

D3036, AUGUST 1987—REVISED JUNE 1988

- **Reliable Silicon-Gate CMOS Technology**
- **Low Power Consumption**
  Operating Mode . . . 80 mW
  Power-Down Mode . . . 5 mW
  μ-Law Coding
- **Excellent Power Supply Rejection Ratio Over Frequency Range of 0 to 50 kHz**
- **No External Components Needed for Sample, Hold, and Auto-Zero Functions**
- **Precision Internal Voltage References**
- **Single Chip Contains A/D, D/A, and Associated Filters**

N DUAL-IN-LINE PACKAGE
(TOP VIEW)



FEATURE TABLE

16 Pins
μ-Law Coding
Variable Mode:
64 kHz to 2.048 MHz
Fixed Mode:
2.048 MHz (TCM129C18, TCM29C18),
1.536 MHz (TCM129C19, TCM29C19)
8-Bit Resolution
12-Bit Dynamic Range

description

The TCM129C18, TCM129C19, TCM29C18, and TCM29C19 are low-cost single-chip pulse-code-modulated encoders and decoders (PCM codecs) and PCM line filters. These devices incorporate both the A/D and D/A functions, an anti-aliasing filter (A/D), and a smoothing filter (D/A). These devices are ideal for use with the TMS320 family members, particularly those featuring a serial port such as the TMS32020, TMS32011, and TMS320C25.

Primary applications of these devices include:

Digital Encryption Systems
Digital Voice-Band Data Storage Systems
Digital Signal Processing

These devices are designed to perform encoding of analog input signals (A/D conversion) and decoding of digital PCM signals (D/A conversion). They are useful for implementation in the analog interface of a digital-signal processing system. Both devices also provide band-pass filtering of the analog signals prior to encoding and smoothing after decoding.

The analog input is encoded into an 8-bit digital representation by use of the μ-law encoding scheme (CCITT G.711) which equates to 12 bits of resolution for low amplitude signals. Similarly, the decoding section converts 8-bit PCM data into an analog signal with 12 bits of dynamic range. The filter characteristics (bandpass) for the encoder and decoder are determined by a single clock input (CLK). The filter roll-off (−3 dB) is derived by:

$f_{CO} = k \cdot f_{CLK}/256$ for the TCM129C18 and TCM29C18 or $f_{CO} = k \cdot f_{CLK}/192$ for the TCM129C19 and TCM29C19

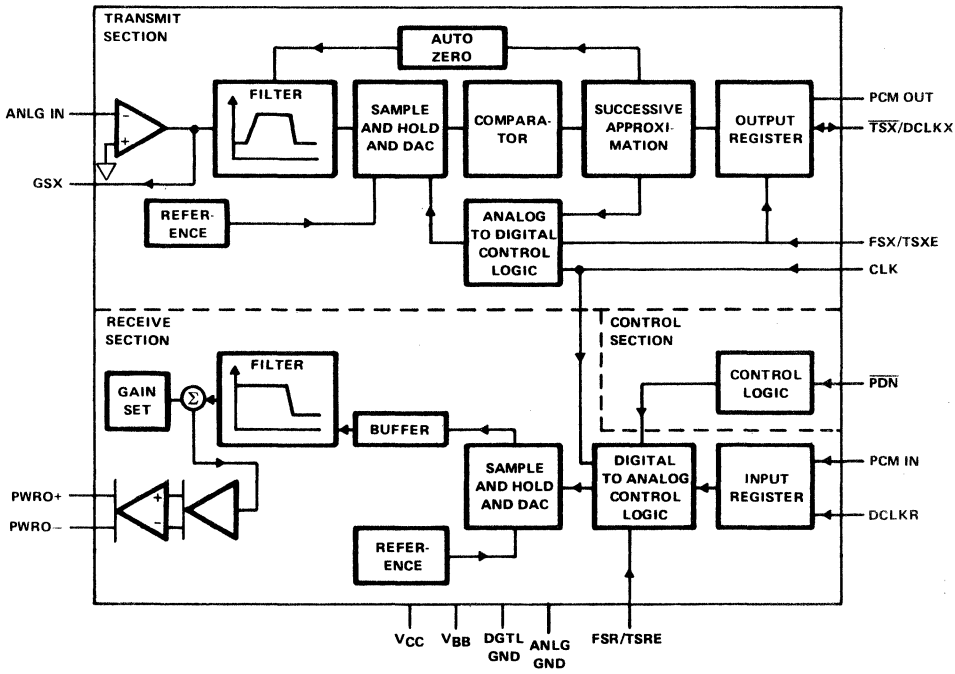
where k has a value of 0.44 for the high-frequency roll-off point, and a value of 0.019 for the low-frequency roll-off point.

description (continued)

The sampling rate of the ADC is determined by the Frame Sync Clock, FSX; the sampling rate of the DAC is determined by the Frame Sync Clock, FSR. Once a conversion is initiated by FSX or FSR, data is clocked in or out on the next consecutive eight clock pulses in the fixed data rate mode. Likewise, data may also be transferred on the next eight consecutive clock pulses of the data clocks, DCLKX and DCLKR, in the variable data rate mode. In the variable data rate mode, DCLKX and DCLKR are independent, but must be in the range from $f_{CLK}/32$ to f_{CLK}.

The TCM129C18 and TCM129C19 are characterized for operation over the temperature range of −40°C to 85°C. The TCM29C18 and TCM29C19 are characterized for operation over the temperature range of 0°C to 70°C.

functional block diagram



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NAME	PIN	DESCRIPTION
ANLG IN	14	Inverting analog input to uncommitted transmit operational amplifier
ANLG GND	13	Analog ground return for all voice circuits. Not internally connected to digital ground.
CLK	9	Master clock and data clock for the fixed data rate mode. Master (filter) clock only for variable data-rate mode. This clock is used for both the transmit and receive sections.
DCLKR	5	When this pin is connected to V_{BB}, the device operates in the fixed-data-rate mode. When DCLKR is not connected to V_{BB}, the device operates in the variable-data-rate mode and DCLKR becomes the receive data clock, which operates at frequencies from 64 kHz to 2.048 MHz.
DGTL GND	8	Digital ground for all internal logic circuits. Not internally connected to analog ground.
FSR/TSRE	7	Frame sync clock input/time-slot enable for the receive channel. In the variable-data-rate-mode, this signal must remain high for the duration of the time-slot. The receive channel enters the standby state when FSR is TTL low for 30 ms.
FSX/TSXE	10	Frame synchronization clock input/time-slot enable for transmit channel. Operates independently of, but in an analogous manner to FSR/TSRE. The transmit channel enters the standby state when FSX is low for 300 ms.
GSX	15	Output terminal of internal uncommitted operational amplifier. Internally, this is the voice signal input to the transmit filter.
PCM IN	6	Receive PCM input. PCM data is clocked in on this pin on eight consecutive negative transitions of the receive data clock, which is CLKR in fixed-data-rate timing and DCLKR in variable-data-rate timing.
PCM OUT	11	Transmit PCM output. PCM data is clocked out of this output on eight consecutive positive transitions of the transmit data clock, which is CLKX in fixed-data-rate timing and DCLKX in variable-data-rate timing.
$\overline{PDN}$	4	Power-Down Select. On the TCM129C18 and the TCM29C18, the device is inactive with a TTL low-level input and active with a TTL high-level input to the pin. On the TCM129C19 and the TCM29C19, this pin must be connected to a TTL high level.
PWRO+	2	Noninverting output of power amplifier can drive transformer hybrids or high-impedance loads directly in either a differential or a single-ended configuration.
PWRO−	3	Inverting output of power amplifier, functionally identical to PWRO+
$\overline{TSX}$/DCLKX	12	Transmit channel time slot strobe (output) or data clock (input). In the fixed-data-rate mode, this is an open-drain output to be used as an enable signal for a three-state-buffer. In the variable-data-rate mode, DCLKX becomes the transmit data clock, which operates at TTL levels from 64 kHz to 2.048 MHz.
V_{BB}	1	Negative supply voltage, −5 V ±5%.
V_{CC}	16	Positive supply voltage, 5 V ±5%.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . −0.3 to 15 V
Output voltage, V_O . . . . . −0.3 to 15 V
Input voltage, digital inputs, V_I . . . . . −0.3 to 15 V
Digital ground voltage . . . . . −0.3 to 15 V
Operating free-air temperature range . . . . . −10°C to 80°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: Voltage values for maximum ratings are with respect to V_{BB}.

recommended operating conditions (see Note 2)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (see Note 3)		4.75	5	5.25	V
V_{BB}	Supply voltage		−4.75	−5	−5.25	V
	DGTL GND voltage with respect to ANLG GND			0		V
V_{IH}	High-level input voltage, all inputs except ANLG IN		2.2			V
V_{IL}	Low-level input voltage, all inputs except ANLG IN				0.8	V
V_{IPP}	Peak-to-peak analog input voltage				4.2	V
R_L	Load resistance	GSX	10			kΩ
		PWRO+ and/or PWRO−	300			Ω
C_L	Load capacitance	GSX			50	pF
		PWRO+ and/or PWRO−			100	
T_A	Operating free-air temperature	TCM129C18 or TCM129C19	−40		85	°C
		TCM29C18 or TCM29C19	0		70	

NOTES: 2. To avoid any possible damage and reliability problems to these CMOS devices when applying power, the following sequence should be followed:
(1) Connect ground
(2) Connect the most negative voltage
(3) Connect the most positive voltage
(4) Connect the input signals.
When powering down the device, follow the above steps in reverse order. If the above procedure cannot be followed, connect a diode between V_{BB} and DGTL GND, cathode to DGTL GND, anode to V_{BB}.
3. Voltages at analog inputs and outputs, V_{CC} and V_{BB} terminals are with respect to the ANLG GND terminal. All other voltages are referenced to the DGTL GND terminal unless otherwise noted.
4. Analog input signals that exceed 4.2 V peak-to-peak may contribute to clipping and preclude correct A/D conversion. The digital code representing values higher than 4.200 V is 10000000. For values more negative than 4.200 V, the code is 0000000.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature

supply current, fdclk = 2.048 MHz, outputs not loaded

PARAMETER			TEST CONDITIONS	TCM129CXX		TCM29CXX		UNIT
				MIN	MAX	MIN	MAX	
I_{CC}	Supply current from V_{CC}	operating			14		10	mA
		standby	FSX or FSR at V_{IL} after 300 ms		1.5		1.2	
		power down	$\overline{PDN}$ at V_{IL} after 10 μs		1.2		1	
I_{BB}	Supply current from V_{BB}	operating			−14		−10	mA
		standby	FSX or FSR at V_{IL} after 300 ms		−1.5		−1.2	
		power down	$\overline{PDN}$ at V_{IL} after 10 μs		−1.2		−1	

digital interface

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage, PCM OUT	I_{OH} = −9.6 mA	2.4			V
		I_{OH} = −0.1 mA	3.5			
V_{OL}	Low-level output voltage, $\overline{TSX}$	I_{OL} = 3.2 mA			0.5	V
I_{IH}	High-level input current, any digital input	V_I = 2.2 V to V_{CC}			12	μA
I_{IL}	Low-level input current, any digital input	V_I = 0 to 0.8 V			12	μA
C_i	Input capacitance			5	10	pF
C_o	Output capacitance			5	10	pF

†All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C.

transmit side (A/D) characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input offset current at ANLG IN	V_I = −2.17 V to 2.17 V		1		pA
Input offset voltage at ANLG IN	V_I = −2.17 V to 2.17 V			±25	mV
Input bias current	V_I = −2.17 V to 2.17 V			±100	nA
Open-loop voltage amplification at GSX		5000			
Unity-gain bandwidth at GSX			1		MHz
Input resistance at ANLG IN		10			Ω
Gain tracking error with sinusoidal input (see Notes 5, 6, and 7)	3 dBm0 to −40 dBm0, REF level = −10 dBm0			±0.5	dB
	−40 dBm0 to −50 dBm0, REF level = −10 dBm0			±2.5	
Transmit gain tolerance	V_i = 1.06 V, f = 1.02 kHz	0.95		1.19	Vrms
Noise	Ref max output level: 200 Hz to 3 kHz			−70	dB
Supply voltage rejection ratio, V_{CC} or V_{BB}	f = 0 to 30 kHz, (measured at PCM OUT) idle channel, Supply signal = 200 mV P-P	−20			dB
Crosstalk attenuation, transmit-to-receive (single-ended)	ANLG IN = 0 dBm, f = 1 kHz unity gain, PCM IN = lowest decode level, measured at PWRO+	62			dB
Signal-to-distortion ratio, with sinusoidal input (see Note 8)	ANLG IN = 0 to −30 dBm0	33			dB
	ANLG IN = −30 to −40 dBm0	27			
	ANLG IN = −40 to −45 dBm0	22			
Absolute delay time to PCM OUT	Fixed data rate, FCLKX = 2.048 MHz, input to ANLG IN = 1 kHz at 0 dB		245		μs

receive side (D/A) characteristics (see Note 9)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Output offset voltage PWRO+ and PWRO− (single-ended)	Relative to ANLG GND			±200	mV
Output resistance at PWRO+ and PWRO−			1	2	Ω
Gain tracking error with sinusoidal input (see Notes 5, 6, and 7)	3 dBm0 to −40 dBm0, REF level = −10 dBm0			±0.5	dB
	−40 dBm0 to −50 dBm0, REF level = −10 dBm0			±2.5	
Receive gain tolerance	V_i = 1.06 V, f = 1.02 kHz	1.34		1.69	Vrms
Noise	Ref max output level: 200 Hz to 3 kHz			−70	dB
Supply voltage rejection ratio, V_{CC} or V_{BB} (single-ended)	f = 0 to 30 kHz, idle channel, Supply signal = 200 mV P-P, narrow band, frequency at PWRO+	−20			dB
Crosstalk attenuation, receive-to-transmit (single-ended)	PCM IN = 0 dB, Frequency = 1 kHz at PCM OUT	60			dB
Signal-to-distortion ratio, sinusoidal input (see Note 8)	ANLG IN = 0 dBm0 to −30 dBm0	33			dB
	ANLG IN = −30 dBm0 to −40 dBm0	27			
	ANLG IN = −40 dBm0 to −45 dBm0	22			
Absolute delay time to PWRO+	Fixed data rate, FCLKX = 2.048 MHz		190		μs

†All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C.

NOTES: 5. Unless otherwise noted, the analog input is a 0-dBm0, 1020-Hz sine wave, where 0 dBm0 is defined as the zero-reference point of the channel under test. This corresponds to an analog signal input of 1.064 V rms, or an output of 1.503 V rms.
6. The input amplifier is set for unity gain. The digital input is a PCM bit stream generated by passing a 0-dBm0, 1020-Hz sine wave through an ideal encoder.
7. The TCM129C18, TCM129C19, TCM29C18, and TCM29C19 are internally connected to set PWRO+ and PWRO− to 0dBm. All output levels are (sin x)/x corrected.
8. CCITT G.712 – Method 2.
9. The receive side (D/A) characteristics are referenced to a 600-Ω termination.

propagation delay times over recommended ranges of operating conditions, fixed-data-rate mode (see timing diagrams)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{pd1}	From rising edge of transmit clock to bit 1 data valid at PCM OUT (data enable time on time slot entry)	C_L = 0 to 100 pF	0	145	ns
t_{pd2}	From rising edge of transmit clock bit n to bit n+1 data valid at PCM OUT (data valid time)	C_L = 0 to 100 pF	0	145	ns
t_{pd3}	From falling edge of transmit clock bit 8 to bit 8 Hi-Z at PCM OUT (data float time on time slot exit)	C_L = 0	60	215	ns
t_{pd4}	From rising edge of transmit clock bit 1 to TSX active (low) (time slot enable time)	C_L = 0 to 100 pF	0	145	ns
t_{pd5}	From falling edge of transmit clock bit 8 to TSX inactive (high) (timeslot disable time)	C_L = 0	60	190	ns

propagation delay times over recommended ranges of operating conditions, variable-data-rate mode

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{pd6}	From DCLKX	C_L = 0 to 100 pF	0	100	ns
t_{pd7}	From time slot enable to PCM OUT	C_L = 0 to 100 pF	0	50	ns
t_{pd8}	From time slot disable to PCM OUT	C_L = 0 to 100 pF	0	80	ns
t_{pd9}	From FSX	$t_{d(TSDX)}$ = 140 ns	0	140	ns

clock timing requirements over recommended ranges of supply voltage and operating free-air temperature (see timing diagrams)

PARAMETER		MIN	TYP†	MAX	UNIT
$t_{c(CLK)}$	Clock period for CLK, (2.048-MHz systems)	488			ns
t_r, t_f	Rise and fall times for CLK	5		30	ns
$t_{w(CLK)}$	Pulse duration for CLK	220			ns
$t_{w(DCLK)}$	Pulse duration for DCLK (f_{DCLK} = 64 Hz to 2.048 MHz)	220			ns
	Clock duty cycle [$t_{w(CLK)}/t_{c(CLK)}$] for CLK	45	50	55	%

transmit timing requirements over recommended ranges of supply voltage and operating free-air temperature, fixed-data-rate mode (see timing diagrams)

PARAMETER		MIN	MAX	UNIT
$t_{d(FSX)}$	Frame sync delay time	100	$t_{c(CLK)} - 100$	ns

receive timing requirements over recommended ranges of supply voltage and operating free-air temperature, fixed-data-rate mode (see timing diagrams)

PARAMETER		MIN	MAX	UNIT
$t_{d(FSR)}$	Frame sync delay time	100	$t_{c(CLK)} - 100$	ns

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transmit timing requirements over recommended ranges of supply voltage and operating free-air temperature, variable-data-rate mode

	PARAMETER	MIN	MAX	UNIT
$t_{d(TSDX)}$	Delay time, timeslot from DCLKX (see Note 10)	140	$t_{w(DCLKX)} - 140$	ns
$t_{d(FSX)}$	Delay time, frame sync	100	$t_{c(CLK)} - 100$	ns
$t_{w(DCLKX)}$	Pulse duration, DCLKX	488	15620	ns

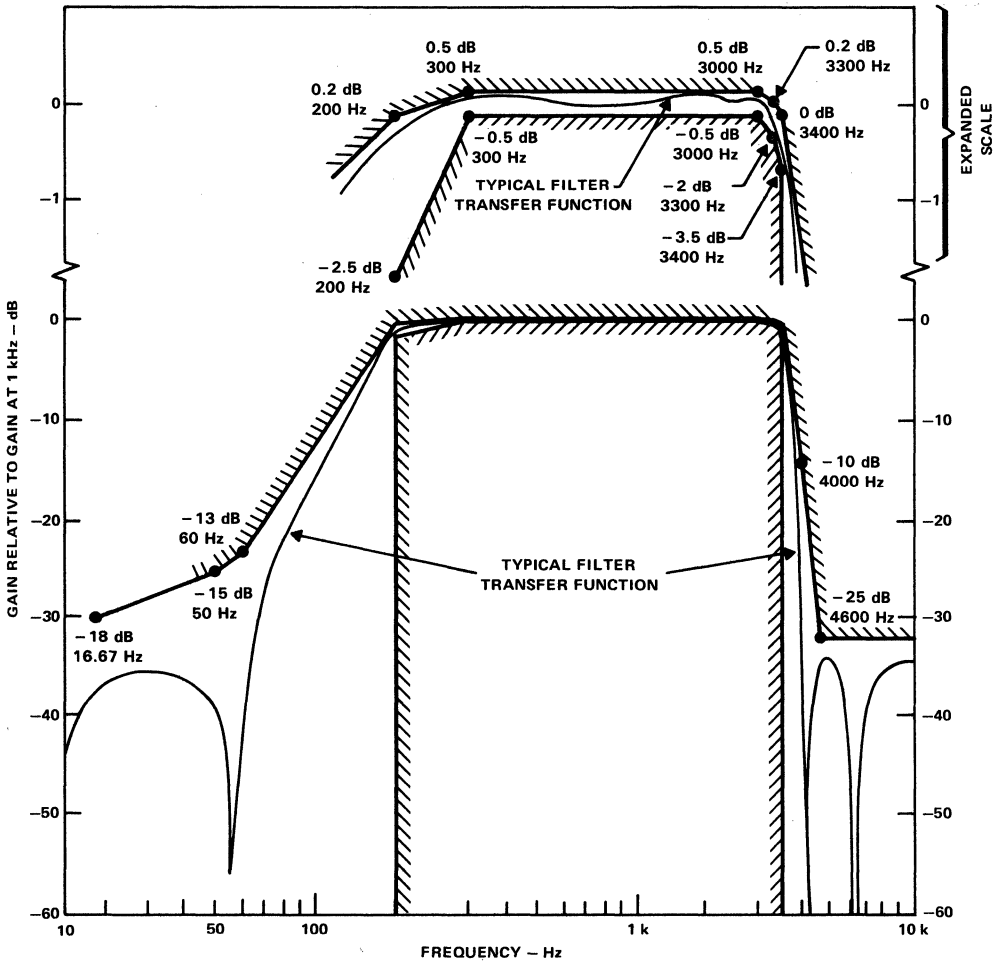
receive timing requirements over recommended ranges of supply voltage and operating free-air temperature, variable-data-rate mode

	PARAMETER	MIN	MAX	UNIT
$t_{d(TSDR)}$	Delay time, timeslot from DCLKR (see Note 11)	140	$t_{w(DCLKR)} - 140$	ns
$t_{d(FSR)}$	Delay time, frame sync $T_{C(CLK)}$	100	$t_{c(CLK)} - 100$	ns
$t_{su(PCM\ IN)}$	Setup time, before bit 7 falling edge	10		ns
$t_{h(PCM\ IN)}$	Hold time after bit 8 falling edge	60		ns
$t_{w(DCLKR)}$	Pulse duration, DCLKR	488	15620	ns
$t_{(SER)}$	Time slot end receive time	0		ns

64-kbit operation timing requirements over recommended ranges of supply voltage and operating free-air temperature, variable-data-rate mode

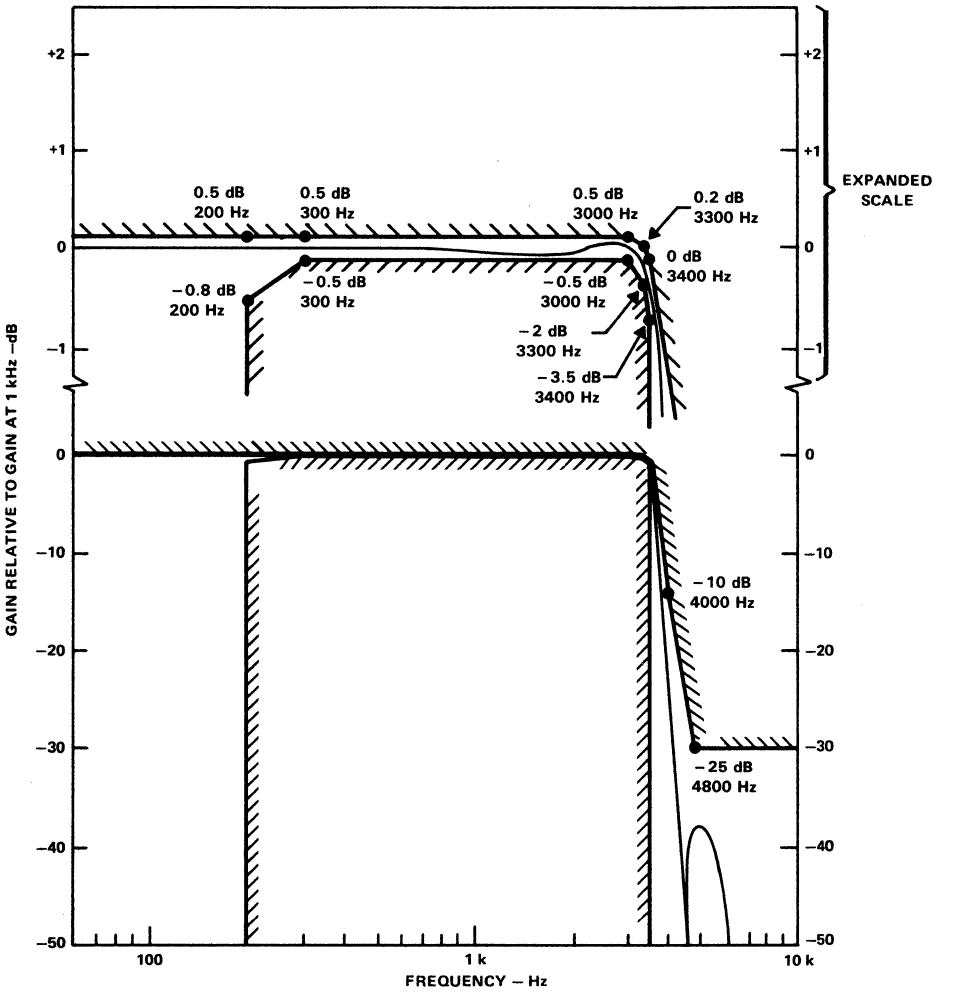
	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{FSLX}	Transmit frame sync minimum down time	FSX = TTL high for remainder of frame	488		ns
t_{FSLR}	Receive frame sync minimum down time	FSR = TTL high for remainder of frame	1952		ns
t_{wCLK}	Pulse duration, data clock			10	μs

NOTES: 10. t_{FSLX} min requirement overrides the $t_{d(TSCDX)}$ max requirement for 64-kHz operation.
11. t_{FSLR} min requirement overrides the $t_{c(TSDR)}$ max requirement for 64-kHz operation.



NOTE: This is a typical transfer function of the receiver filter component.

FIGURE 1. TRANSFER CHARACTERISTICS OF THE TRANSMIT FILTER



NOTE: This is a typical transfer function of the receiver filter component.

FIGURE 2. TRANSFER CHARACTERISTIC OF THE RECEIVE FILTER

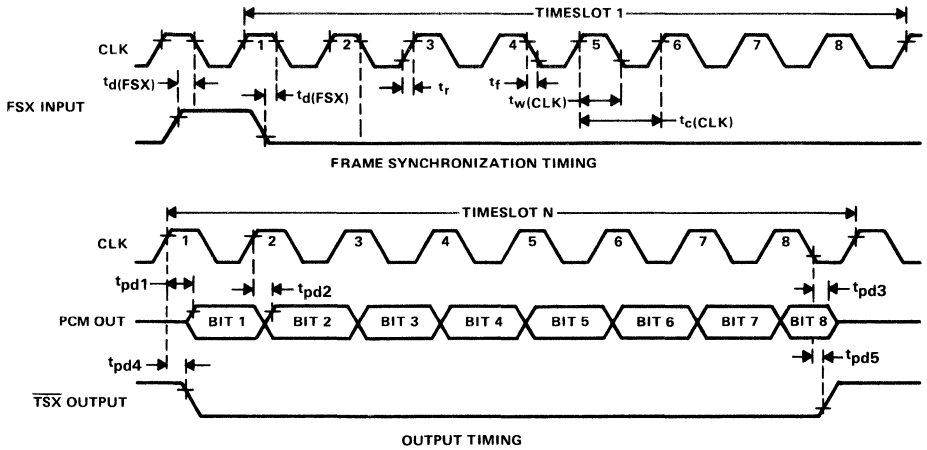


FIGURE 3. TRANSMIT TIMING (FIXED-DATA-RATE)

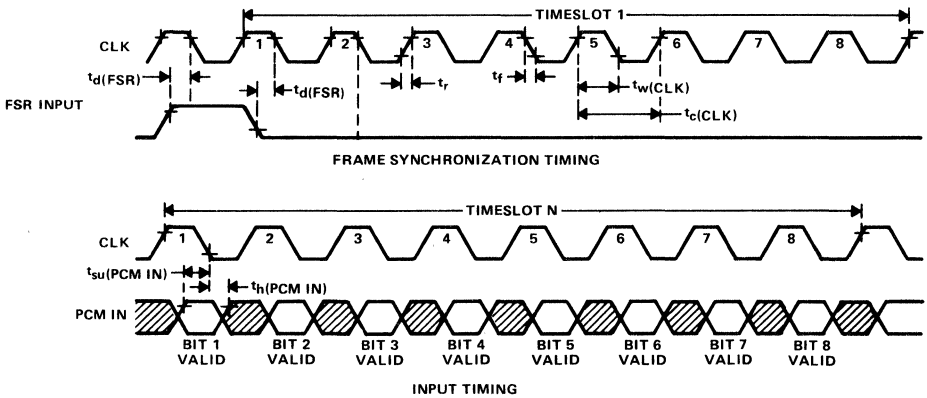


FIGURE 4. RECEIVE TIMING (FIXED-DATA-RATE)

NOTES: A. Inputs are driven from 0.45 V to 2.4 V. Time intervals are referenced to 2 V if the high level is indicated and 0.8 V if the low level is indicated.

B. Bit 1 is the most significant bit (MSB) and is clocked in first on the PCM IN input or is clocked out first on the PCM OUT output. Bit 8 is the least significant bit (LSB) and is clocked in last on the PCM IN input or is clocked out last on the PCM OUT output.

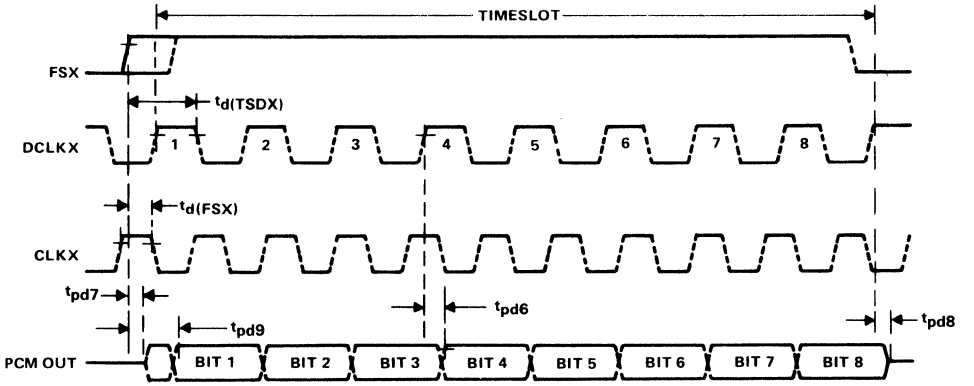
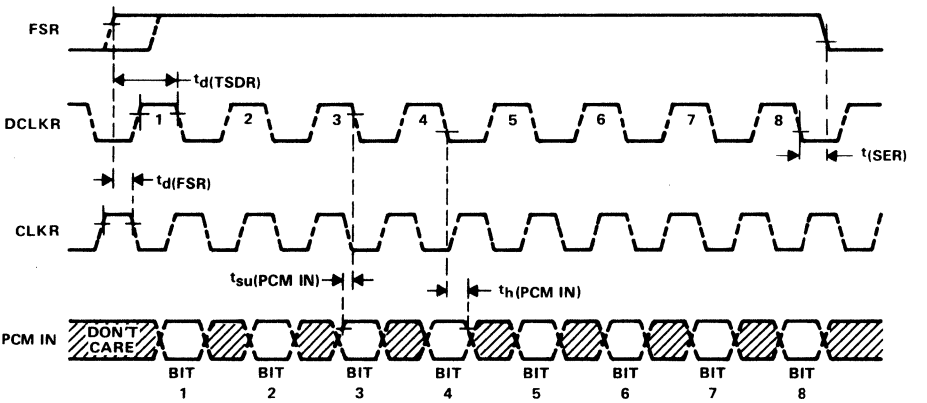


FIGURE 5. TRANSMIT TIMING (VARIABLE-DATA-RATE)



NOTE: All timing parameters referenced to V_{IH} and V_{IL} except t_{pd7} and t_{pd8}, which reference a high-impedance state.

FIGURE 6. RECEIVE TIMING (VARIABLE-DATA-RATE)

GENERAL OPERATION

system reliability features

The TCM129C18, TCM129C19, TCM29C18, and TCM29C19 are powered up in four steps:

V_{CC} and V_{BB} supply voltages are applied.
All clocks are connected.
TTL high is applied to $\overline{PDN}$.
FSX and/or FSR synchronization pulses are applied.

On the transmit channel, digital outputs PCM OUT and $\overline{TSX}$ are held in high-impedance state for approximately four frames (500 μs) after power up or application of V_{BB} or V_{CC}. After this delay, PCM OUT, $\overline{TSX}$, and signaling are functional and will occur in the proper timeslot. The analog circuits on the transmit side require approximately 60 ms to reach their equilibrium value due to the autozero circuit settling time. Thus valid digital information, such as for on/off hook detection, is available almost immediately, while analog information is available after some delay.

To further enhance system reliability, PCM OUT and $\overline{TSX}$ will be placed in a high-impedance state approximately 20 μs after an interruption of CLKX. These interruptions could possibly occur with some kind of fault condition.

power-down and standby operations

To minimize power consumption, a power-down mode and three standby modes are provided.

For power down, an external TTL low signal is applied to the $\overline{PDN}$ pin. It is not sufficient to remove the TTL high voltage to $\overline{PDN}$. In the absence of a signal, the $\overline{PDN}$ pin floats to TTL high and the device remains active. In the power-down mode, the average power consumption is reduced to an average of 5 mW.

The standby modes give the user the option of putting the entire device on standby, putting only the transmit channel on standby, or putting only the receive channel on standby. To place the entire device on standby, both FSX and FSR are held at TTL low. For transmit-only operation, FSX is high and FSR is held low. For receive-only operation, FSR is high and FSX is held low. See Table 1 for power down and standby procedures.

TABLE 1. POWER DOWN AND STANDBY PROCEDURES

DEVICE STATUS	PROCEDURE	TYPICAL POWER CONSUMPTION	DIGITAL OUTPUT STATUS
Power down	$\overline{PDN}$ = TTL low	5 mW	$\overline{TSX}$ and PCM OUT are in a high-impedance state
Entire device on standby	FSX and FSR are TTL low	12 mW	$\overline{TSX}$ and PCM OUT are in a high-impedance state
Only transmit on standby	FSX is TTL low FSR is TTL high	70 mW	$\overline{TSX}$ and PCM OUT are placed in a high-impedance state within 300 ms.
Only receive on standby	FSR is TTL low FSX is TTL high	110 mW	

fixed-data-rate timing (see Figure 3 and 4)

Fixed-data-rate timing is selected by connecting DCLKR to V_{BB}. It uses master clock CLK, frame synchronizer clocks FSX and FSR, and output $\overline{TSX}$. FSX and FSR are 8-kHz inputs that set the sampling frequency. Data is transmitted on the PCM OUT pin on the first eight positive transitions of CLK following the rising edge of FSX. Data is received on the PCM IN pin on the first eight falling edges of CLK following FSX. A digital-to-analog (D/A) conversion is performed on the received digital word and the resulting analog sample is held on an internal sample-and-hold capacitor until transferred to the receive filter.

The TCM129C18 and TCM29C18 operate at 2.048 MHz only. The TCM129C19 and TCM29C19 operate at 1.536 MHz only.

variable data rate timing

Variable-data-rate timing is selected by connecting DCLKR to the bit clock for the receive PCM highway rather than to V_{BB}. It uses master clock CLK, bit clocks DCLKX and DCLKR, and frame synchronization clocks FSX and FSR.

Variable-data-rate timing allows for a flexible data frequency. The frequency of the bit clocks can be varied from 64 kHz to 2.048 MHz. The bit clocks must be synchronous; however, the master clock is restricted to 2.048 MHz.

While FSX/TSXE input is high, PCM data is transmitted from PCM OUT onto the highway on the next eight consecutive positive transitions of DCLKX. Similarly, while the FSR/TSRE input is high, the PCM word is received from the highway by PCM IN on the next eight consecutive negative transitions of DCLKR.

The transmitted PCM word will be repeated in all remaining timeslots in the 125 μs frame as long as DCLKX is pulsed and FSX is held high. This feature, which allows the PCM word to be transmitted to the PCM highway more than once per frame, if desired, is available only with variable-data-rate timing.

asynchronous operation

In either timing mode, the master clock, data clock, and timeslot strobe must be synchronized at the beginning of each frame. Specifically, in the variable-data-rate mode the rising edge of CLK must occur within $t_{d(FSX)}$ ns before the rise of FSX, while the leading edge of DCLKX must occur within t_{TSDX} ns of the rise of FSX. CLK and DCLKX are synchronized once per frame but may be of different frequencies. The receive channel operates in a similar manner and is completely independent of the transmit timing (see variable data rate timing diagrams).

transmit operation

transmit filter

The input section provides gain adjustment in the passband by means of an on-chip uncommitted operational amplifier. The load impedance to ground (ANLG GND) at the amplifier output (GSX) must be greater than 10 kΩ in parallel with less than 50 pF. The input signal on the ANLG IN pin can be either ac or dc coupled.

A low-pass antialiasing section is included on the device. This section provides 35-dB attenuation at the sampling frequency. No external components are required to provide the necessary antialiasing function for the switched capacitor section of the transmit filter.

The passband section provides flatness and stopband attenuation that fulfills the AT&T D3/D4 channel bank transmission specification and CCITT recommendation G.712. The device specifications meet or exceed digital class 5 central office switching systems requirements.

A high-pass section configuration was chosen to reject low-frequency noise from 50- and 60-Hz power lines, 17-Hz European electric railroads, ringing frequencies and their harmonics, and other low-frequency noise. Even with the high rejection at these frequencies, the sharpness of the band edge gives low attenuation at 200 Hz. This feature allows the use of low-cost transformer hybrids without external components.

encoding

The encoder internally samples the output of the transmit filter and holds each sample on an internal sample and hold capacitor. The encoder performs an analog-to-digital conversion on a switched capacitor array. Digital data representing the sample is transmitted on the first eight data clock bits of the next frame.

The autozero circuit corrects for dc offset on the input signal to the encoder. The autozero circuit uses the sign bit averaging technique. The sign bit from the encoder output is long-term averaged and subtracted from the input to the encoder. All dc offset is removed from the encoder input waveform.

receive operation

decoding

The serial PCM word is received at the PCM IN pin on the first eight data clock bits of the frame. Digital-to-analog conversion is performed and the corresponding analog sample is held on an internal sample-and-hold capacitor. This sample is transferred to the receive filter.

receive filter

The receive section of the filter provides passband flatness and stopband rejection that fulfills both the AT&T D3/D4 specification and CCITT recommendation G.712. The filter contains the required compensation for the (sin x)/x response of such decoders.

receive output power amplifiers

A balanced output amplifier is provided to allow maximum flexibility in output configuration. Either of the two outputs can be used single-ended (i.e., referenced to ANLG GND) to drive single-ended loads. Alternatively, the differential output will directly drive a bridged load. The output stage is capable of driving loads as low as 300 ohms single-ended to a level of 12 dBm or 600 ohms differentially to a level of 15 dBm.

Transmission levels are specified relative to the receive channel output under digital milliwatt conditions (i.e., when the digital input at PCM IN is the eight-code sequence specified in CCITT recommendation G.711).

output gain

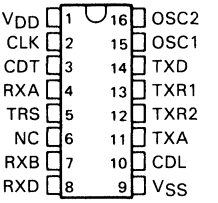
The devices are internally connected to set the PWRO+ and PWRO− to 0 dBm.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

D2662, NOVEMBER 1985—REVISED APRIL 1986

- **Single-Chip Frequency-Shift-Keying (FSK) Modem**
- **Meets Both Bell 202 and CCITT V23 Specifications**
- **Transmit Modulation at 75, 150, 600, and 1200 Baud**
- **Receive Demodulation at 5, 75, 150, 600, and 1200 Baud**
- **Half-Duplex Operation Up to 1200 Baud Transmit and Receive**
- **Full-Duplex Operation Up to 1200 Baud Transmit and 150 Baud Receive**
- **On-Chip Group Delay Equalization and Transmit/Receive Filtering**
- **Carrier-Detect-Level Adjustment and Carrier-Fail Output**
- **Single 5-V Power Supply**
- **Low Power Consumption**
- **Reliable CMOS Silicon Gate Technology**

J DUAL-IN-LINE PACKAGE
(TOP VIEW)



NC—No internal connection

Caution. These devices have limited built-in gate protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

description

The TCM3105 is a single-chip asynchronous Frequency Shift Keying (FSK) voiceband modem that uses silicon gate CMOS technology to implement a switched capacitor architecture. It is pin selectable (TXR1, TXR2, and TRS inputs) for a wide range of transmit/receive baud rates and is compatible with the applicable BELL 202 or CCITT V23 standards. Operation is fully reversible, thereby allowing both forward and backward channels to be used simultaneously.

The transmitter is a programmable frequency synthesizer that provides two output frequencies (on TXA), representing the 'marks' and 'spaces' of the digital signal present on the TXD input.

The receive section is responsible for the demodulation of the analog signal appearing at the RXA input and is based on the principle of frequency-to-voltage conversion. This section contains a group delay equalizer (to correct phase distortion), automatic gain control, carrier detect level adjustment, and bias distortion adjustment, thereby optimizing performance and giving the lowest possible bit error rate.

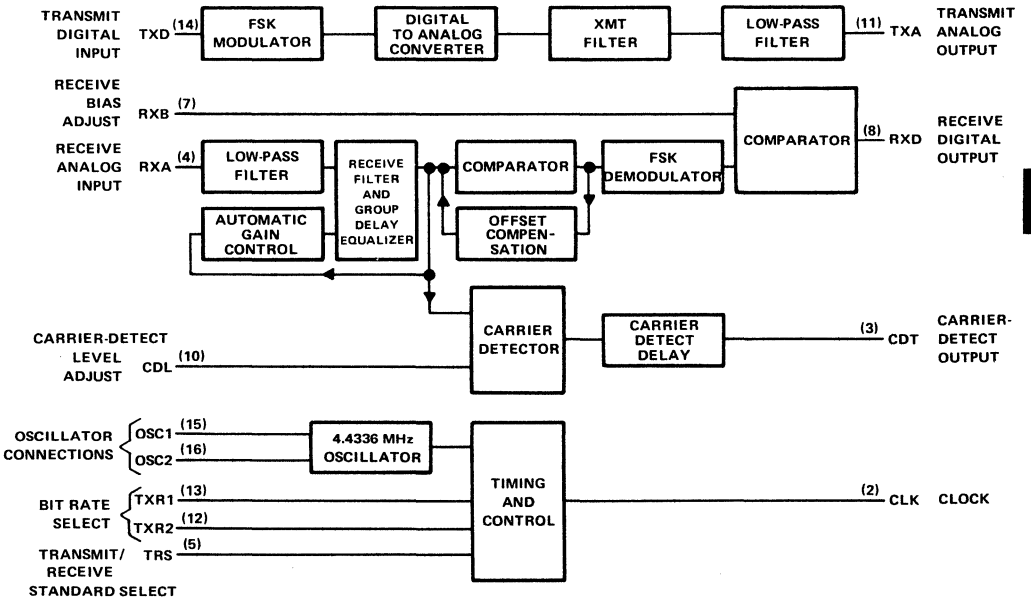
Carrier-detect information is given to the system by means of the carrier-detect circuits, which set a flag on the CDT output if the level of received in-band energy falls below a value set on the CDL input for a specified minimum duration.

The TCM3105JE is characterized for operation from −40°C to 85°C. The TCM3105JL is characterized for operation from 0°C to 70°C.

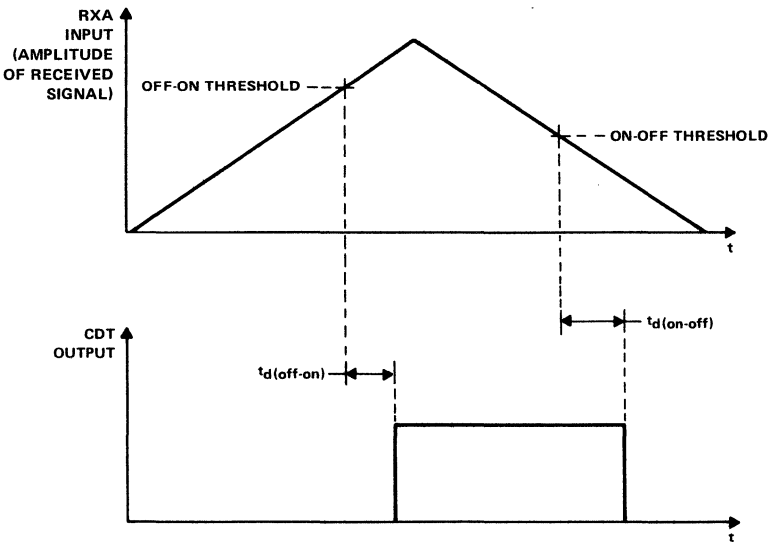
PIN FUNCTIONAL DESCRIPTION

PIN		DESCRIPTION
NO.	NAME	
1	V_{DD}	Positive supply voltage
2	CLK	Output for a continuous clock signal at 16 times the highest selected (transmit or receive) bit rate
3	CDT	Carrier-Detect Output. A low-level output indicates carrier failure
4	RXA	Receive Analog Input to which the received line signal must be ac coupled
5	TRS	Transmit/Receive Standard Select Input, which, with TXR1 and TXR2, sets the standard bit rates and mark/space frequencies
6	NC	No internal connection
7	RXB	Receive Bias Adjust for external adjustment of the decision threshold of the final comparator to minimize bias distortion
8	RXD	Receiver Digital Output for the demodulated received data in positive logic. The high logic level is a mark and the low logic level is a space.
9	V_{SS}	Most negative supply voltage (normally ground); connected to substrate
10	CDL	Carrier Detect Level Adjust for external adjustment of carrier detect threshold
11	TXA	Transmit Analog Output for the modulated signal, which must be ac coupled
12	TXR2	Bit Rate Select 2 input, which, along with TXR1 and TRS, sets the bit rates and mark/space frequencies
13	TXR1	Bit Rate Select 1 input, which, along with TXR2 and TRS, sets the bit rates and mark/space frequencies
14	TXD	Transmit Digital Input for input data to the transmitter in positive logic. The high logic level is a mark and the low logic level is a space. The data can be accepted at any speed from zero to the selected speed and may be totally asynchronous.
15	OSC1	Oscillator connections. The crystal (typically 4.4336 MHz) is connected to these pins. If an external clock is used, OSC2 is left open and the clock is connected to OSC1.
16	OSC2	

functional block diagram



timing diagram



absolute maximum ratings over free-air operating temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . −0.3 V to 10 V
Input voltage, V_I (any input) . . . . . −0.3 to V_{DD}
Operating free-air temperature range: TCM3105JE . . . . . −55°C to 85°C
TCM3105JL . . . . . −10°C to 70°C
Storage temperature range . . . . . −55°C to 150°C

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

	TCM3105JE			TCM3105JL			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}	4	5	5.5	4	5	5.5	V
High-level input voltage, V_{IH}	2		V_{DD}	2		V_{DD}	V
Low-level input voltage, V_{IL}	0		0.8	0		0.8	V
Analog input level, peak-to-peak (ac coupled)		0.30	0.78		0.30	0.78	V
Clock frequency, f_{clock}	4.4334	4.4336	4.4338	4.4334	4.4336	4.4338	MHz
Analog load impedance at TXA	50			50			kΩ
Operating free-air temperature range, T_A	−40		85	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		TCM3105JE			TCM3105JL			UNIT
					MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage	RXD, CDT, CLK	I_{OH} = −100 μA		2.4		V_{DD}	2.4		V_{DD}	V
V_{OL}	Low-level output voltage	RXD, CDT, CLK	I_{OL} = 1.6 mA		V_{SS}		0.4	V_{SS}		0.4	V
	Analog output voltage level, peak-to-peak	TXA	V_{DD} = 4 V	R_L = 50 kΩ, C_L = 100 pF		1.55			1.55		V
			V_{DD} = 5 V		1.4	1.9	2.3	1.4	1.9	2.3	
			V_{DD} = 5.5 V			2.1			2.1		
	Adjust voltage	RXB	V_{DD} = 5 V		2.3	2.7	3.1	2.3	2.7	3.1	V
		CDL			2.8	3.3	3.9	2.8	3.3	3.9	
	Analog output dc offset	TXA				$V_{DD}/2$			$V_{DD}/2$		V
	Digital input current	TXD, TRS, TXR1, TXR2	V_I = 0 to V_{DD}				±1			±1	μA
	Analog input current	RXA					±15			±15	μA
	Bias input current	RXB, CDL	V_I = 3 V				±150			±150	μA
I_{DD}	Supply current		V_{DD} = 4 V			3	6		3	5	mA
			V_{DD} = 5 V			5	10		5	8	
			V_{DD} = 5.5 V			8	16		8	12	
C_i	Input capacitance, all inputs		f = 1 MHz			10			10		pF
C_o	Output capacitance, all inputs		f = 1 MHz			10			10		pF
	Phase jitter						200			200	μs
	Bias distortion‡						±15%			±15%	
	Carrier detect threshold, off-on§				−45.5		−43	−45.5		−43	dBm
	Carrier detect threshold, on-off§				−48		−45.5	−48		−45.5	dBm
	Carrier detect hysteresis				2.5	2.8		2.5	2.8		dBm

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Bias distortion is the departure from a 50% duty cycle when a series of alternating mark and space tones is received.
§This is the threshold with the CDL input properly adjusted.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TCM3105JE			TCM3105JL			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
$t_{d(off\text{-}on)}$	Carrier detect off-to-on delay time	RX = 600 or 1200 b/s	12		25	12		25	ms
		RX = 5, 75, or 150 b/s	48		80	48		80	
$t_{d(on\text{-}off)}$	Carrier detect on-to-off delay time	RX = 600 or 1200 b/s	12		20	12		20	ms
		RX = 5, 75, or 150 b/s	48		75	48		75	
	Transmit frequency deviation from assignment (see Table 1)	f_{clock} = 4.4336 MHz		±1			±1		Hz

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

PRINCIPLES OF OPERATION

The TCM3105 FSK modem is made up of four functional circuits. The circuits are the transmitter, the receiver, a carrier detector, and control and timing (See Figure 1).

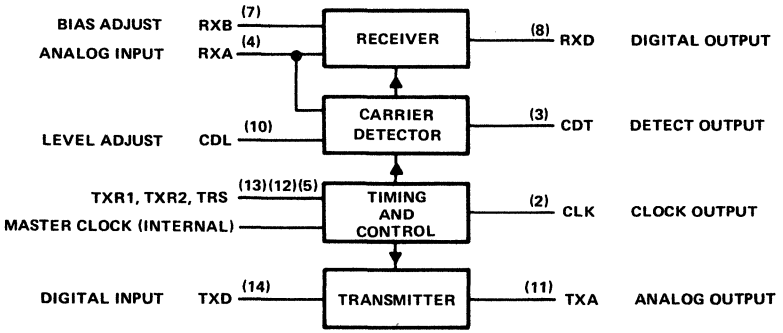


FIGURE 1. TCM3105 SYSTEM PARTITIONING

transmitter

The transmitter comprises a phase coherent FSK modulator, a transmit filter, and a transmit amplifier. The modulator is a programmable frequency synthesizer that drives the output frequencies by variable division of the oscillator frequency (4.4336 MHz). The division ratio is set by the states of the Transmit/Receive Standard input (TRS), the Bit Rate Select inputs (TXR1 and TXR2), and the Digital Data input (TXD).

A switched-capacitor low-pass filter limits the harmonics and noise outside the transmit band and the characteristics of this filter are set by the frequency select inputs as previously described. The harmonics introduced by the transmit filter clock are removed by a continuous low-pass filter.

The transmitter output level varies with power supply voltage and so must be compensated in the 2-wire to 4-wire converter to give a constant output level to the line.

receiver

A continuous low-pass anti-aliasing filter is followed by the receive amplifier, which automatically controls the gain to give a constant output level from the receive filter. The receive filter limits the bandwidth of the signal presented to the demodulator, reducing out-of-band interference, and has very high rejection of the transmit channel frequencies. These are typically present at much higher levels than the received signal.

The group delay equalizer is a switched-capacitor network that compensates the delay introduced by the receive filter and the network. The output from the equalizer is then limited to give an FSK modulated squarewave that is presented to the demodulator.

The demodulator is an edge-triggered multivibrator that triggers off positive and negative going edges. The output of the demodulator is, therefore, a stream of constant-length pulses at a frequency that is double the frequency of the limited input signal. The dc component of this signal is proportional to the received frequency and is extracted by a switched-capacitor, low-pass, post-demodulator filter.

The variation of dc level with received frequency is presented to a comparator that slices at a level externally fixed by the RXB bias adjustment pin. This voltage depends on received bit rate and internal offsets. The comparator output is then the received data at the RXD output.

carrier detect

The carrier detect circuits comprise an energy detector and digital delay. The energy detector compares the total signal level at the output of the receive filter to an externally set threshold level on the CDL input. The comparator has a 2.5-dB hysteresis and a delay to allow for momentary signal loss and to prevent oscillation. The output of the detector is available on the CDT pin where a high level indicates that a carrier is present. The data output is clamped to a MARK condition when the carrier detect output switches off at the end of transmission.

control and timing

An on-chip oscillator runs from an external 4.4336-MHz crystal connected between the OSC1 and OSC2 pins or an external signal driving OSC1. A clock signal equal to 16 times the highest selected bit rate (transmit or receive) is available on the CLK output.

The single-supply rail means that all analog functions are referenced to an internally generated reference. All analog inputs and output must be ac coupled.

transmit and receive modes

The various modes of operation of the TCM3105 are given in Table 1. The data convention is that a logic high is a mark and a logic low is a space.

TABLE 1. MODES OF OPERATION

STANDARD	TRS	TXR1	TXR2	TRANSMITTED BAUD RATE	RECEIVED BAUD RATE	TRANSMIT FREQUENCY ASSIGNMENTS (Hz)	RECEIVE FREQUENCY ASSIGNMENTS (Hz)	CLK FREQUENCY (kHz)
CCITT V.23	L	L	L	1200	1200	M 1300 S 2100	M 1300 S 2100	19.11
	H	L	L	1200	75	M 1300 S 2100	M 390 S 450	19.11
	L	L	H	600	75	M 1300 S 1700	M 390 S 450	9.56
	H	L	H	600	600	M 1300 S 1700	M 1300 S 1700	9.56
	L	H	L	75	1200	M 390 S 450	M 1300 S 2100	19.11
	H	H	L	75	600	M 390 S 450	M 1300 S 1700	9.56
	L	H	H	75	75	M 390 S 450	M 390 S 450	1.19
BELL 202	$\overline{CLK}$	L	L	1200	1200	M 1200 S 2200	M 1200 S 2200	19.11
	$\overline{CLK}/8$	L	H	1200	150	M 1200 S 2200	M 387 S 487	19.11
	$\overline{CLK}/8$	L	H	1200	5	M 1200 S 2200	M 387 S 0	19.11
	CLK	H	L	150	1200	M 387 S 487	M 1200 S 2200	19.11
	CLK	H	H	150	150	M 387 S 487	M 387 S 487	2.39
	CLK†	H†	L†	5	1200	M 387	M 1200	19.11
	H†	H†	H†			S 0	S 2200	
	H	H	H	Transmit Disabled	1200	Transmit Disabled	M 1200 S 2200	19.11

H = high level, L = low level
†In these modes, the modulation is controlled by the TRS and TXR2 pins. TXD is tied high.

APPLICATION INFORMATION

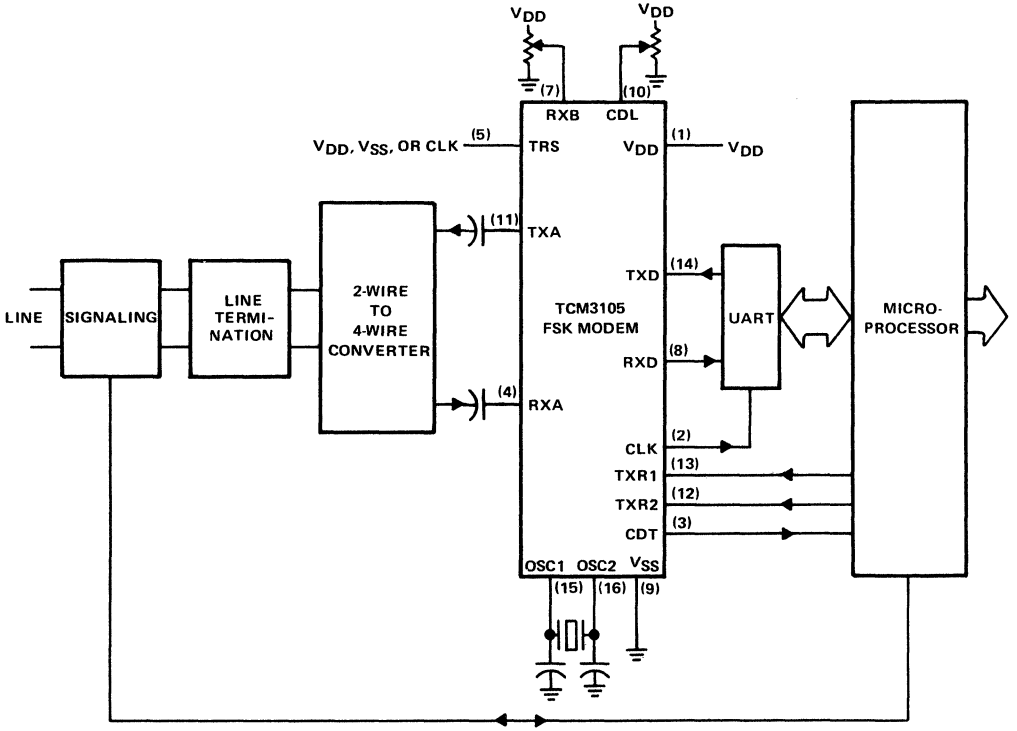


FIGURE 2. TYPICAL SYSTEM CONFIGURATION

APPLICATION INFORMATION

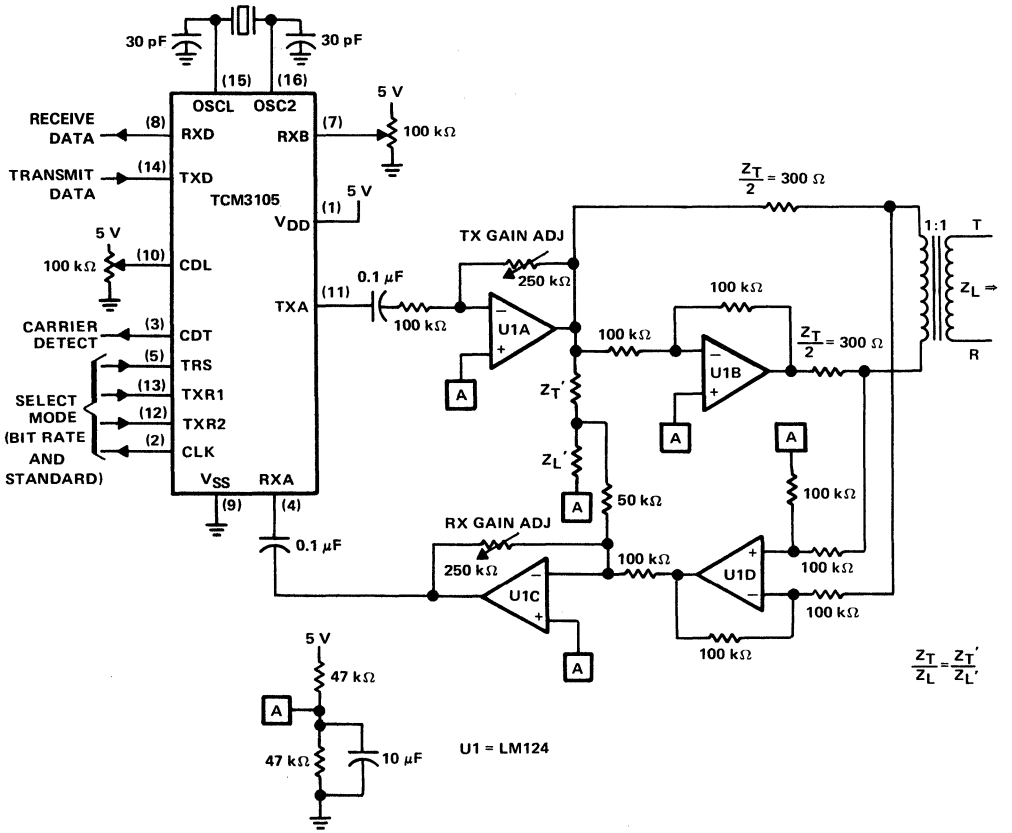


FIGURE 3. TELEPHONE LINE INTERFACE CIRCUIT

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APPLICATION INFORMATION

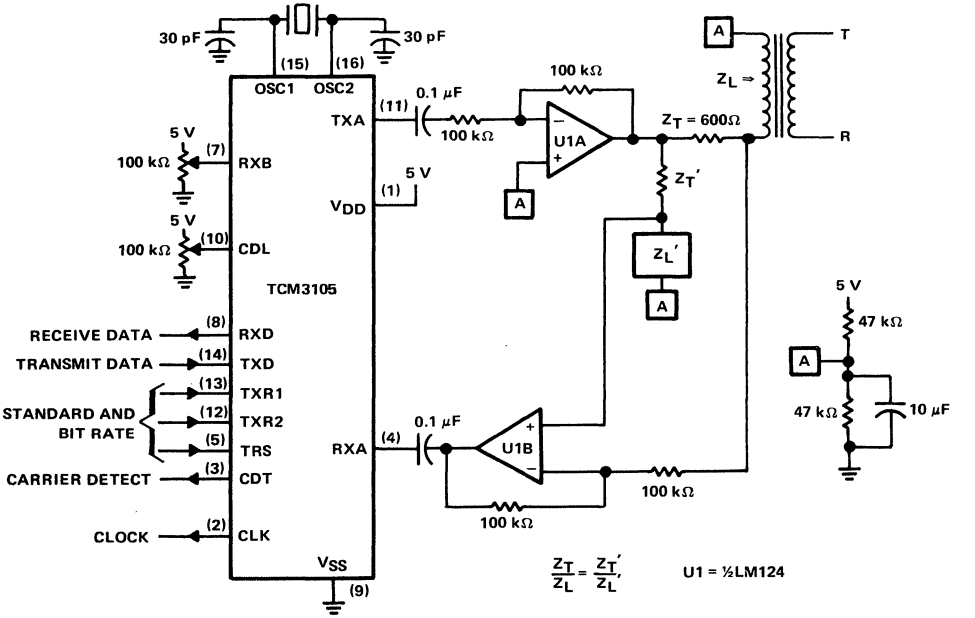
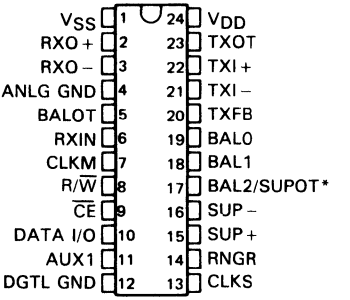


FIGURE 4. SIMPLIFIED TELEPHONE LINE INTERFACE CIRCUIT

D2729, NOVEMBER 1983—REVISED APRIL 1988

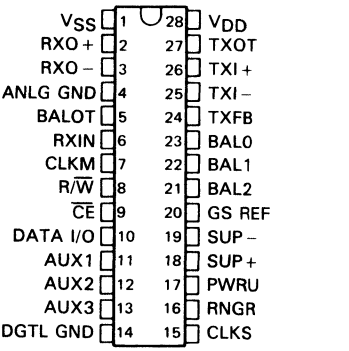
- **Per-Channel-Programmable Single-Chip Subscriber-Line-Control Circuit (SLCC)**
- **Programmable TX and RX Gain**
- **Digital Inputs and Outputs are Compatible with TTL Levels**
- **±5 V Power Supplies**
- **Software-Selectable External Balance Networks**
- **On-Off Hook Detection, Ring Trip**
- **TCM4205A Provides Control of the Three Auxiliary Relays and Ground Start Supervision**
- **Serial Interface to Microprocessor**
- **High-Reliability Silicon-Gate CMOS Technology**
- **TCM4207A Uses a Flux Canceling Technique that Allows Use of a Smaller Transformer**

TCM4204A, TCM4207A . . . J PACKAGE
(TOP VIEW)



*BAL2 for TCM4204A, SUPOT for TCM4207A

TCM4205A . . . J PACKAGE
(TOP VIEW)



description

The TCM4204A, TCM4205A, and TCM4207A are subscriber-line-control circuits (SLCC) designed to provide all the functions of a complete voice-band PCM channel when used in conjunction with appropriate codec and filter circuits. The TCM4205A enhancement of the TCM4204A brings out two additional relay control pins (AUX2) and (AUX3), an external reference for ground-start applications (GS REF), and a pin for control of an external power supply (PWRU). The TCM4207A replaces BAL2 with a filtered analog output (SUPOT) that can be used in flux canceling applications.

The primary applications for these devices include:

Transmission Systems and Switching Systems
2-Wire Interface 4-Wire Interface
Subscriber Line Concentrators

These devices are characterized for operation from 0°C to 70°C.

Caution. These devices have limited built-in gate protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

analog section

Separate Programmable Attenuators: 63 steps covering a 12.6-dB range in 0.2-dB steps
6-dB Differential RX amplification for driving a 900-ohm load to a peak of 3.2 V
Software-selectable external balance networks. Electronic 2-wire to 4-wire conversion.
Software-controlled analog loopback
Separate RX and TX paths allow true 4-wire operation.

supervision

Normal loop-start and/or ground-start supervision
Ring trip supervision
Supervision function provided with minimal, low cost external components.

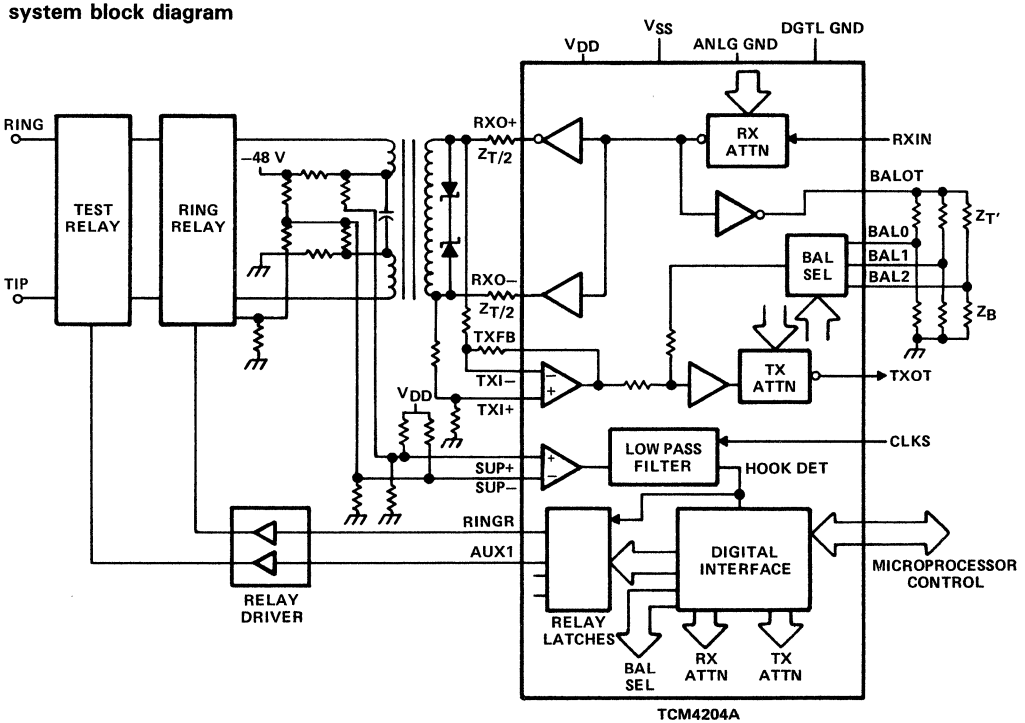
digital interface

Simple four-pin serial interface provides easy-to-use microprocessor interface.
Clocks can be any of the standard PCM clock frequencies.
Power fault detection lets user know when RAM has been affected by a supply fault.

software control

Up to three external balance networks
Transmit and receive attenuators
Power down, standby, voice, or loopback modes of operation
Ring relay and up to three auxiliary relays.

system block diagram



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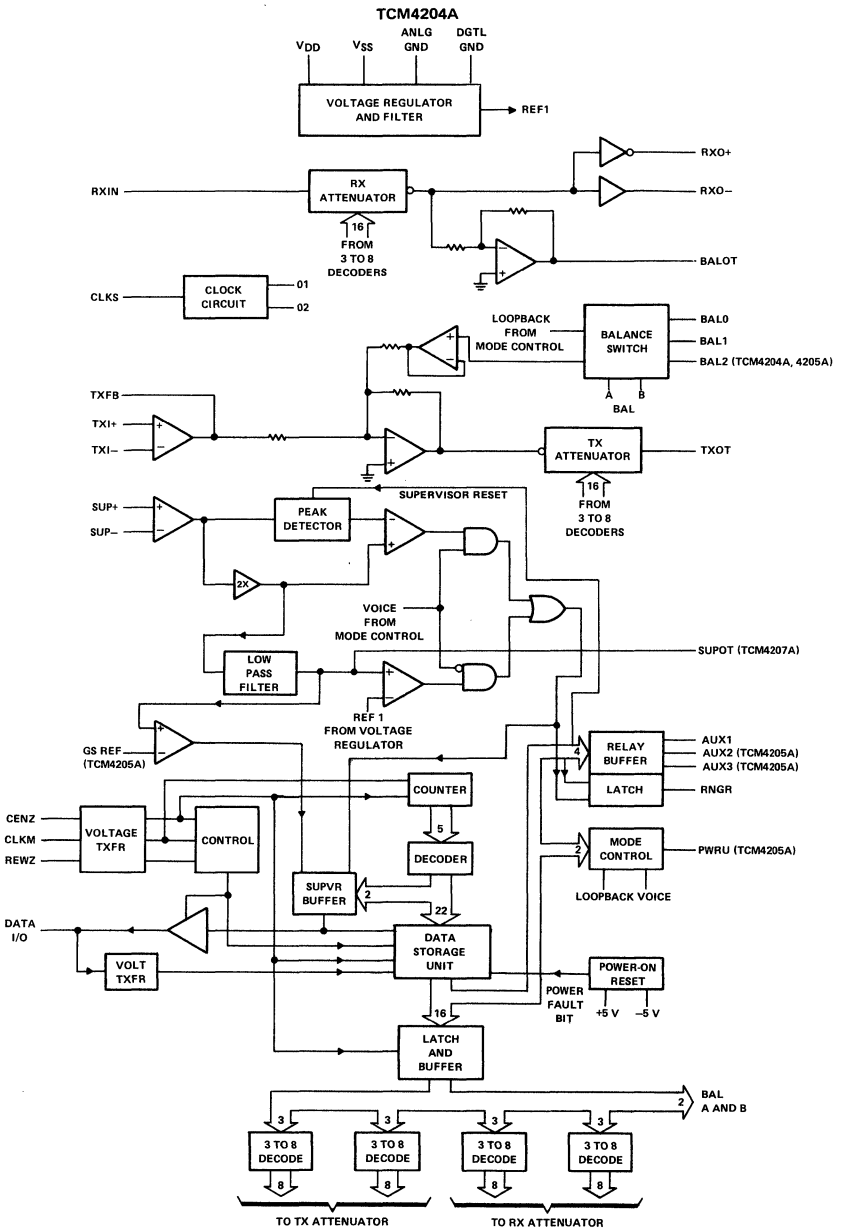
functional block diagram (positive logic)



NAME	PIN			DESCRIPTION
	TCM4204A	TCM4205A	TCM4207A	
ANLG GND	4	4	4	Analog ground
AUX1	11	11	11	Latched digital outputs for relay control
AUX2		12		
AUX3		13		
BAL0	19	23	19	Analog input to balance network selection
BAL1	18	22	18	
BAL2	17	21		
BALOT	5	5	5	A buffered form of the RX signal for application to the external balance network
$\overline{CE}$	9	9	9	Chip enable. Activated by a logic low input.
CLKM	7	7	7	Digital clock input that advances the pointer counter of the digital storage unit (DSU) allowing the information in the DSU to be accessed. When R/$\overline{W}$ and $\overline{CE}$ are low, information on the DATA I/O pin is latched into the DSU by the falling edge of CLKM.
CLKS	13	15	13	A continuous clock input (from 1.536 to 2.048 MHz) used for internal logic. This signal is not synchronous with any other signal.
DATA I/O	10	10	10	Digital data input/output. When $\overline{CE}$ is low and R/$\overline{W}$ is high, the DATA I/O pin is in the output mode. When $\overline{CE}$ is low and R/$\overline{W}$ is low, the DATA I/O pin is in the input mode. When $\overline{CE}$ is high, the DATA I/O pin is in the high-impedance state.
DGTL GND	12	14	12	Digital ground
GS REF		20		Analog reference voltage input used for ground start supervision.
PWRU		17		Decoded digital output of Mode Control used to control an external power supply.
RNGR	14	16	14	Latched digital output to control the ring relay. The output turns off (low) when off-hook is detected, but the controller must program the ring bit low to ensure that the output remains low.
RXIN	6	6	6	Analog input to the receive section
RXO+	2	2	2	Complementary analog output of the receive amplifier
RXO−	3	3	3	
R/$\overline{W}$	8	8	8	Digital input control for the direction of response of the digital storage unit. A logic high on R/$\overline{W}$ sets the DSU to transmit information. A logic low on R/$\overline{W}$ enables the DSU to receive information.
SUP+	15	18	15	Differential analog supervision inputs. Inputs to SUP+ and SUP− are used to detect off-hook status during normal and ringing supervision.
SUP−	16	19	16	
SUPOT			17	Filtered supervisory analog output
TXFB	20	24	20	Feedback out of TX input amplifier
TXI+	22	26	22	Analog differential inputs to TX input amplifier
TXI−	21	25	21	
TXOT	23	27	23	Analog output of TX output amplifier
V_{DD}	24	28	24	Supply voltage (5 V ±5%)
V_{SS}	1	1	1	Supply voltage (−5 V ±5%) referenced to ANLG GND

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} . . . . . 6 V
Supply voltage, V_{SS} . . . . . −6 V
Input/output voltage: digital . . . . . V_{DD} + 0.3 V to GND − 0.3 V
analog . . . . . V_{DD} + 0.3 V to V_{SS} − 0.3 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 125°C

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD} (see Note 1)		4.75	5.25	V
Supply voltage, V_{SS} (see Note 2)		−4.75	−5.25	V
High-level input voltage, V_{IH}		2.4		V
Low-level input voltage, V_{IL}			0.8	V
DC voltage at either supervision input (SUP+ or SUP−)			±2.5	V
SUPOT voltage			±3	V
DC offset voltage at analog input to RX section (RXIN)			±25	mV
DC offset voltage at transmit inputs (TXI+ and TXI−)			±25	mV
Load capacitance, C_L	BALOT, TXOT, SUPOT, TXFB		25	pF
	RXO+, RXO−		100	
Load resistance, R_L	BALOT, TXOT, SUPOT, TXFB	5	100	kΩ
	RXO+, RXO−	300		Ω
Rise time (any logic input), t_r			100	ns
Fall time (any logic input), t_f			100	ns
Clock frequency f_{CLKS}		1.536	2.048	MHz
Operating free-air temperature, T_A		0	70	°C

NOTES: 1. Reference is to DGTL GND and ANLG GND.
2. Reference is to ANLG GND.

static electrical characteristics over recommended operating free-air temperature range, V_{DD} = 5 V, V_{SS} = −5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = −0.4 mA	4.6			V
V_{OL}	Low-level output voltage		I_{OL} = 1.6 mA			0.4	V
	Differential voltage between V_{DD} and V_{SS} required to initiate POR (power-on-reset)		dV_{DD}/dt > 1 V/ms	6		8	V
	Differential voltage between SUP+ and SUP− required to initiate off-hook condition		Voice mode, SUP− at DGTL GND DSU bit 23 high	−20	0	25	mV
			Standby and power-down mode, SUP− at DGTL GND	20	50	100	
I_I	Input current, analog	SUP+, SUP−	V_I = 3 V			1	μA
			V_I = −3 V			−1	
		RXIN, TXI+, TXI−, BAL0, BAL1, BAL2	V_I = 5 V			1	
			V_I = −5 V			−1	
I_{IH}	High-level input current		V_I = 5 V			1	μA
I_{IL}	Low-level input current		V_I = 0			−1	μA
I_{OH}	High-level output current	digital	V_{OH} = 2.5	−1.6			mA
		data	V_{OH} = 0 (continuous)	−10			
I_{OL}	Low-level output current	digital	V_{OL} = 2.5 V	1.6			mA
		data	V_{OL} = 5 V (continuous)	55			
	Analog output offset voltage	TXOT	Loopback mode, TXI+/TXI− at ANLG GND			±50	mV
		TXFB	TXI+ at ANLG GND,TXI− tied to TXFB, Loopback mode			±25	
		RXO+	Voice mode, RXIN at ANLG GND			±75	
		RXO−	Voice mode, RXIN at ANLG GND			±75	
		SUPOT	SUP+ and SUP− at ANLG GND		220		
	Receive output dc leakage current (See Note 3)		Standby or power-down mode, RXO+ connected to RXO− through a 600 Ω resistor			±20	μA
I_{DD}	Supply current		On hook, power-down mode			3	mA
			On hook, voice mode			9	
			Off hook, power-down mode			6	
			Off hook, voice mode			13	
I_{SS}	Supply current		On hook, power-down mode			−3	mA
			On hook, voice mode			−9	
			Off hook, power-down mode			−6	
			Off hook, voice mode			−13	

†All typical values are at V_{DD} = 5 V, V_{SS} = −5 V, T_A = 25°C.
NOTE 3: If used with a center-tapped transformer (with center tap connected to GND), the output leakage current will increase.

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dynamic characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
	Receive output dynamic range (RXO+, RXO−)		Input to RXIN = −75 dBm to 3 dBm, R_L = 900 Ω to ANLG GND, Receive channel attenuator set to code 100111 (0 dB), f = 1.02 kHz	−74 to 3	−75 to 3.1		dBm
	Receive output dynamic range (BALOT)		Input to RXIN = −75 dBm to 3 dBm, R_L = 5 kΩ to ANLG GND, Receive channel attenuator set to code 100111 (0 dB), f = 1.02 kHz	−74 to 3	−75 to 3.1		dBm
	Transmit output dynamic range (TXOT)		Loopback mode, Input = −75 dBm to 3 dBm. R_L = 5 kΩ to ANLG GND, Transmit channel attenuator set to code 111111 (0 dB), f = 1.02 kHz	−74 to 3	−75 to 3.1		dBm
	Transmit output dynamic range (TXFB)		Input = −75 dBm to 3 dBm, R_L = 5 kΩ to ANLG GND, Transmit input amplifier set for unity gain, Transmit attenuator set to 0 dB, f = 1.02 kHz	−74 to 3	−75 to 3.1		dBm
	Supervision output dynamic range (SUPOT)		Input to SUP+ = 75 mV to 750 mV (rms), SUP− at ANLG GND, R_L = 100 kΩ to ANLG GND, f = 5 Hz	−14 to 6	−13.8 to 6.2		dBm
	Frequency response of supervision circuits	0 to 10 Hz	SUP− at ANLG GND, Input to SUP+ = −10 dBm0‡, f_{clock} = 2.048 MHz			8	dB
		16.6 Hz				−45	
		15 Hz to 65				−30	
		66 Hz or greater				−40	
C_i	Input capacitance	Data	$\overline{CE}$ high			14	pF
		All others				7.5	
$t_{d(POR)}$	Delay time to power-on reset		V_{DD} − V_{SS} switched from 10 V to 6 V	100		200	ns
Z_i	Input impedance, (any input or I/O)			1			MΩ
Z_o	Output impedance	Digital outputs	I_O = −200 μA			100	Ω
		TXOT, BALOT, TXFB				50	
		SUPOT				1	kΩ
		RXO+, RXO−	Voice mode, I_O = −10 μA		1	3	Ω

†All typical values are at V_{DD} = 5 V, V_{SS} = −5 V, T_A = 25°C.
‡0 dBmO is the zero-reference point of the channel under test. This corresponds to a voltage of 1520 mV (rms) on inputs and outputs, with attenuators set for 0 dB.

ac characteristics — half channel† over recommended ranges of supply voltage and operating free-air temperature

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Frequency response	50 Hz to 200 Hz	R_L = 900 Ω to ANLG GND, V_I = 0 dBm0, Ref = 1.020 kHz	−0.2	0.2	dB
	200 Hz to 300 Hz		−0.1	0.1	
	300 Hz to 4 kHz		−0.05	0.05	
Level (gain) tracking	V_i = 0, −10, −20, −30 dBm0	R_L = 900 Ω to ANLG GND, f = 1.020 kHz	−0.05	0.05	dB
	V_i = −40, −50 dBm0		−0.1	0.1	
Idle channel noise		R_L = 900 Ω to ANLG GND		8	dBrnc0
Total distortion	V_i = 0 dBm0 to −30 dBm0	R_L = 900 Ω to ANLG GND, f = 1.020 kHz		−50	dB
	V_i = −30 dBm0 to −40 dBm0			−45	
	V_i = −40 dBm0 to −50 dBm0			−40	
Total harmonic distortion	V_i = 3 dBm0, f = 1.020 kHz			−55	dB
Phase Delay time (carrier)	1 kHz			20	μs
	1.8 kHz			20	
Absolute delay time	500 Hz to 600 Hz			30	μs
	600 Hz to 1 kHz			20	
	1 kHz to 2.6 kHz			10	
	2.6 kHz to 2.8 kHz			30	
Departure from linear phase	600 Hz to 1 kHz			±0.1	rad
	1 kHz to 1.3 kHz			±0.05	
	1.3 kHz to 2.3 kHz			±0.05	
	2.3 kHz to 2.7 kHz			+0.04 −0.05	
	2.7 kHz to 3.1 kHz			±0.1	
Supply-voltage sensitivity (see Note 4)	50 Hz to 4 kHz	V_{DD} changing 200 mV p-p		−40	dB
		V_{SS} changing 200 mV p-p		−40	
	4 kHz to 50 kHz	V_{DD} changing 200 mV p-p		−25	
		V_{SS} changing 200 mV p-p		−25	

†Transmit channel is tested with input amplifier set for unity gain. Receive and transmit attenuators are set to 0 dB.

NOTE 4: The receiver supply-voltage sensitivity is the differential RXO+-to-RXO− noise referenced to supply noise. It is assumed that the feed transformer will reject common-mode RXO+/RXO− noise and, therefore, the common-mode supply-voltage sensitivity is not specified.

system characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figures 9 and 10)

PARAMETER	FREQUENCY RANGE	TEST CONDITIONS	MIN	MAX	UNIT
Return loss (see Note 5)	200 Hz to 500 Hz	Z_L = 900 Ω + 2.2 μF		−25	dB
	500 Hz to 1 kHz			−35	
	1 kHz to 2.5 kHz			−40	
	2.5 kHz to 3.4 kHz			−35	
Transhybrid loss (see Note 5)	200 Hz to 500 Hz	Z_L = 900 Ω + 2.2 μF		−25	dB
	500 Hz to 1 kHz			−35	
	1 kHz to 2.5 kHz			−40	
	2.5 kHz to 3.4 kH			−35	
Longitudinal balance (see Note 5)	60 Hz to 500 Hz	2-wire to 4-wire		−66	dB
	500 Hz to 1 kHz			−50	
	1 kHz to 4 kHz			−58	
	200 Hz to 4 kHz	4-wire to 2-wire		−60	

NOTE 5: The return loss, the transhybrid loss, and the longitudinal balance are functions of external components, primarily the battery feed transformer or its functional replacement. The SLCC will not materially change the return loss or the longitudinal balance. The imbalance in transhybrid loss caused by phase or gain errors in the SLCC will be less than those listed.

SLCC — microprocessor timing requirements over recommended ranges of supply voltage and operating free-air temperature

	PARAMETER	MIN	MAX	UNIT
t_a	Access time from $\overline{CE}$↓		140	ns
$t_{c(CLK)}$	Clock period for CLKM	2000		ns
t_r, t_f	Rise and fall times for CLKM	5		ns
t_v	Output data valid after CLKM	80		ns
$t_{w(CLKH)}$	Pulse duration CLKM high	550		ns
$t_{w(CLKL)}$	Pulse duration CLKM low	300		ns
$t_{en(CLK)}$	Internal read/write enable after CLKM		250	ns
$t_{en(R/\overline{W})}$	Enable time, Input after R/$\overline{W}$↓		250	ns
$t_{dis(\overline{CE})}$	Disable time, output after $\overline{CE}$↑		180	ns
t_{su1}	Setup time, CLKM↓ before R/$\overline{W}$↑	50		ns
t_{su2}	Setup time, data before CLKM↓ (see Note 6)	180		ns
t_{su3}	Setup time, CE↓ before CLKM↑ (see Notes 7 and 8)	180		ns
	Duty cycle, CLKM (see Note 9)	10	90	%

NOTES: 6. The R/$\overline{W}$ input must be a logic low.
7. If the user is not interested in reading bit 0, t_{su3} can be a minimum of 30 ns.
8. The R/$\overline{W}$ input must be a logic high.
9. As long as the minimum high and low pulse durations are observed, the CLKM duty cycle is $t_{w(CLKH)}/[t_{w(CLKL)} + t_w$ (CLKH)].

supervision timing characteristics over recommended ranges of operating conditions (see Figure 4)

normal loop supervision timing characteristics, f_{CLKS} = 2.048 MHz

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PHL}	Propagation time high-to-low, hook status bit	Standby mode, SUP− = GND,		75	100	ms
t_{PLH}	Propagation time low-to-high, hook status bit	SUP+ changing from		60	100	ms
$t_{PHL} - t_{PLH}$	Differential propagation time	0 V to 200 mV or from			±20	ms
t_{nr}	Maximum noise rejection duration time	200 mV to 0 V	10			ms

ground key/ground start supervision timing characteristics (TCM4205A only)

PARAMETER		MIN	MAX	UNIT
t_{PHL}	Propagation time high-to-low, ground start bit		150	ms
t_{PLH}	Propagation time low-to-high, ground start bit		150	ms
$t_{PHL} - t_{PLH}$	Differential propagation time		±20	ms
t_{nr}	Maximum noise rejection duration time	10		ms

ring trip detection timing characteristic

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{rt}	Ring trip detect time	Standby mode, SUP− = GND, SUP+ changing from 0 V to 200 mV		55	100	ms

microprocessor internal polling timing requirement

PARAMETER	MIN	MAX	UNIT
Microprocessor polling interval		100	ms

†All typical values are at V_{DD} = 5 V, V_{SS} = −5 V, T_A = 25°C.

PRINCIPLES OF OPERATION

mode control

The SLCC can be forced into one of four modes by the microprocessor (see Figure 1 for mode states and Table 1 for the recommended mode control sequence). The mode control functions are as follows:

Voice operation — All circuits powered up. PWRU output pin is set high.

Power down — Audio circuits are powered down, supervisory circuits are powered up, and the PWRU output pin is set low.

Loopback — Normal balance circuit is interrupted allowing the transmit output to follow the receive input. All other circuits are powered up.

Standby — Audio circuits are powered down, supervisory circuits are powered up, and the PWRU output pin is set high. The internal power-on reset (POR) circuit sets the SLCC to this mode at power up.

TABLE 1. RECOMMENDED MODE CONTROL SEQUENCE

BITS A	BITS B	FUNCTION
L	H	Power Down
L	L	Standby
H	L	Voice
H	H	Loopback

PRINCIPLES OF OPERATION

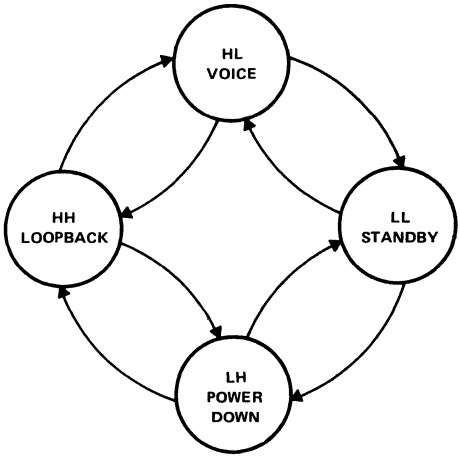


FIGURE 1. MODE CONTROL STATE DIAGRAM

internal power-down states

The internal power down states are the standby mode and the power-down mode. The only difference between the two states is the level of the PWRU output. In the standby mode, PWRU is set high and in the power-down mode, PWRU is set low. The PWRU output can be used to control an external dc-to-dc converter for floating constant-current-feed applications or to drive a status indicator.

standby mode

1. All analog functions except supervision and all logic functions except microprocessor interface and registers are powered down.
2. PWRU output is set high.

power-down mode

1. All analog functions except supervision and all logic functions except microprocessor interface and registers are powered down.
2. PWRU output is set low.

PRINCIPLES OF OPERATION

digital control and microprocessor interface

The data storage unit contains 24 bits of R/$\overline{W}$ (Read/Write) and RO (Read Only) data. The R/$\overline{W}$ data is used to control attenuation, balance, relay selection, and mode of operation. The RO data provides supervisory status information.

The microprocessor uses the $\overline{CE}$, DATA I/O, R/$\overline{W}$, and CLKM input lines to control and time access to the data. When $\overline{CE}$ is toggled from high to low, the serial data sequence is started at bit 0 and the pointer may be sequenced through the 24 data bits. The pointer is advanced by low-to-high transitions of CLKM. In addition, $\overline{CE}$ enables the read and write functions. When $\overline{CE}$ is high, the DATA I/O pin is in the high-impedance state, and the CLKM and R/$\overline{W}$ inputs are ignored.

R/$\overline{W}$ determines whether DATA is an input or an output. When R/$\overline{W}$ is high, DATA I/O is an output and can be read. When R/$\overline{W}$ is low, DATA I/O is an input and can be written.

CLKM has another important function. CLKM must be high for a minimum time defined by t_{en}(CLK) to write data to the DATA I/O pin. It is during this time that all the internal gates get set up to receive the data latched in by the falling edge of CLKM.

microprocessor timing for read operation (see Figure 2)

During the read operation, $\overline{CE}$ goes low and sets the data storage unit (DSU) pointer to bit 0. The setup time (t_a) must pass before bit 0 appears on the DATA I/O line. To advance the DSU pointer, a positive transition of CLKM is needed. CLKM can be raised after the appropriate setup time (t_{su3}). The pointer is then advanced to bit 1. Following this positive transition of CLKM, an internal setup time, t_{en}(CLK), must pass before the correct data from bit 1 appears on DATA I/O. Between this time and the next positive transition of CLKM, the data at bit 1 can be read. The next transition of CLKM advances the pointer to bit 2. Following the internal setup time, the data at bit 2 appears on the DATA I/O line. The time available for reading bit 2 is determined, in this case, by $\overline{CE}$ also going high. The DATA I/O line now goes back to the high impedance state. The time required for this to occur is given by $t_{dis}(\overline{CE})$.

microprocessor timing for write operation (see Figure 3)

In this case, we have to assume $\overline{CE}$ has been low for a long time if we are to look at the N clock edge for CLKM. R/$\overline{W}$ starts out high and, after t_{en}(CLK) elapses, goes low. DATA I/O starts out as an output, while R/$\overline{W}$ is high, which is connected to bit N-1. When CLKM goes high, the pointer is advanced to bit N. R/$\overline{W}$ can go low after t_{en}(CLK). DATA I/O is converted to an input after t_{en}(R/$\overline{W}$. NOTE: In addition to R/$\overline{W}$ being low, CLKM must be high during the time DATA I/O is changing from output to input. Following this time, the data on DATA I/O is valid. CLKM can go low and clock the data into bit N after the minimum setup time, (t_{su2}). The data just clocked in to bit N can be read if R/$\overline{W}$ is now raised. R/$\overline{W}$ can be raised after (t_{su1}). Following data valid time (t_v), the data can be read at bit N.

PRINCIPLES OF OPERATION

TABLE 2. REGISTER MAP

BIT NUMBER	FUNCTION	DATA TYPE	POWER ON RESET
0	On/Off Hook	R0	X
1	Ground Start	R0	X
2	Power Fault	R/$\overline{W}$	H
3	Ring Relay	R/$\overline{W}$	L
4	AUX1 Relay	R/$\overline{W}$	L
5	AUX2 Relay	R/$\overline{W}$	L
6	AUX3 Relay	R/$\overline{W}$	L
7	Mode Control A	R/$\overline{W}$	L
8	Mode Control B	R/$\overline{W}$	L
9	Rx Atten Bit 5 (MSB)	R/$\overline{W}$	L
10	Rx Atten Bit 4	R/$\overline{W}$	L
11	Rx Atten Bit 3	R/$\overline{W}$	L
12	Rx Atten Bit 2	R/$\overline{W}$	L
13	Rx Atten Bit 1	R/$\overline{W}$	L
14	Rx Atten Bit 0 (LSB)	R/$\overline{W}$	L
15	Tx Atten Bit 5 (MSB)	R/$\overline{W}$	L
16	Tx Atten Bit 4	R/$\overline{W}$	L
17	Tx Atten Bit 3	R/$\overline{W}$	L
18	Tx Atten Bit 2	R/$\overline{W}$	L
19	Tx Atten Bit 1	R/$\overline{W}$	L
20	Tx Atten Bit 0 (LSB)	R/$\overline{W}$	L
21	Balance Select A	R/$\overline{W}$	L
22	Balance Select B	R/$\overline{W}$	L
23	Supervisor Reset	R/$\overline{W}$	L

attenuator characteristics

Both attenuators have identical characteristics but are separately controlled. The characteristics of the attenuators are as follows:

1. 63 steps (reference Table 3)
2. Receiver range of 4.8 dB gain to −7.8 dB loss (differential)
3. Transmitter range of 0 dB to −12.6 dB loss
4. Step size of 0.2 dB typical
5. The accuracy of any attenuator setting is ±1 step size.

lead options

The TCM4204A (24-pin constant-voltage option) is designed to provide the minimum set of features required by the largest proportion of world-wide needs. The TCM4204A has the following:

1. Three separate external balance networks
2. Two relay outputs (TTL); one output dedicated to ring and one auxiliary output.

The TCM4205A (28-pin ground-start option) has the following:

1. Three separate external balance networks
2. Four relay outputs (TTL); one dedicated to ring and three auxiliary outputs
3. An input to set the ground-start trip level.

The TCM4207A (24-pin flux-canceling option) has the following:

1. Two separate external balance networks
2. Two relay outputs (TTL); one output dedicated to ring and one auxiliary output
3. One filtered analog output (16.6 Hz at CLKS = 2.048 MHz) that is an analog representation of the dc voltage (< 10 Hz) between the supervisory inputs.

TABLE 3. ATTENUATOR CODES

ATTENUATOR CODE		TRANSMIT†	RECEIVE
DECIMAL	BINARY	CHANNEL	CHANNEL‡
0	000000	−12.6 dB	−7.8 dB
1	000001	−12.4 dB	−7.6 dB
2	000010	−12.2 dB	−7.4 dB
3	000011	−12.0 dB	−7.2 dB
4	000100	−11.8 dB	−7.0 dB
5	000101	−11.6 dB	−6.8 dB
6	000110	−11.4 dB	−6.6 dB
7	000111	−11.2 dB	−6.4 dB
8	001000	−11.0 dB	−6.2 dB
9	001001	−10.8 dB	−6.0 dB
10	001010	−10.6 dB	−5.8 dB
11	001011	−10.4 dB	−5.6 dB
12	001100	−10.2 dB	−5.4 dB
13	001101	−10.0 dB	−5.2 dB
14	001110	−9.8 dB	−5.0 dB
15	001111	−9.6 dB	−4.8 dB
16	010000	−9.4 dB	−4.6 dB
17	010001	−9.2 dB	−4.4 dB
18	010010	−9.0 dB	−4.2 dB
19	010011	−8.8 dB	−4.0 dB
20	010100	−8.6 dB	−3.8 dB
21	010101	−8.4 dB	−3.6 dB
22	010110	−8.2 dB	−3.4 dB
23	010111	−8.0 dB	−3.2 dB
24	011000	−7.8 dB	−3.0 dB
25	011001	−7.6 dB	−2.8 dB
26	011010	−7.4 dB	−2.6 dB
27	011011	−7.2 dB	−2.4 dB
28	011100	−7.0 dB	−2.2 dB
29	011101	−6.8 dB	−2.0 dB
30	011110	−6.6 dB	−1.8 dB
31	011111	−6.4 dB	−1.6 dB
32	100000	−6.2 dB	−1.4 dB
33	100001	−6.0 dB	−1.2 dB
34	100010	−5.8 dB	−1.0 dB
35	100011	−5.6 dB	−0.8 dB
36	100100	−5.4 dB	−0.6 dB
37	100101	−5.2 dB	−0.4 dB
38	100110	−5.0 dB	−0.2 dB
39	100111	−4.8 dB	0.0 dB
40	101000	−4.6 dB	+0.2 dB
41	101001	−4.4 dB	+0.4 dB
42	101010	−4.2 dB	+0.6 dB
43	101011	−4.0 dB	+0.8 dB
44	101100	−3.8 dB	+1.0 dB
45	101101	−3.6 dB	+1.2 dB
46	101110	−3.4 dB	+1.4 dB
47	101111	−3.2 dB	+1.6 dB
48	110000	−3.0 dB	+1.8 dB
49	110001	−2.8 dB	+2.0 dB
50	110010	−2.6 dB	+2.2 dB
51	110011	−2.4 dB	+2.4 dB
52	110100	−2.2 dB	+2.6 dB
53	110101	−2.0 dB	+2.8 dB
54	110110	−1.8 dB	+3.0 dB
55	110111	−1.6 dB	+3.2 dB
56	111000	−1.4 dB	+3.4 dB
57	111001	−1.2 dB	+3.6 dB
58	111010	−1.0 dB	+3.8 dB
59	111011	−0.8 dB	+4.0 dB
60	111100	−0.6 dB	+4.2 dB
61	111101	−0.4 dB	+4.4 dB
62	111110	−0.2 dB	+4.6 dB
63	111111	0.0 dB	+4.8 dB

†Transmit input amplifier set for unity gain.

‡Output measured differentially across RXO+ and RXO−.

PARAMETER MEASUREMENT INFORMATION

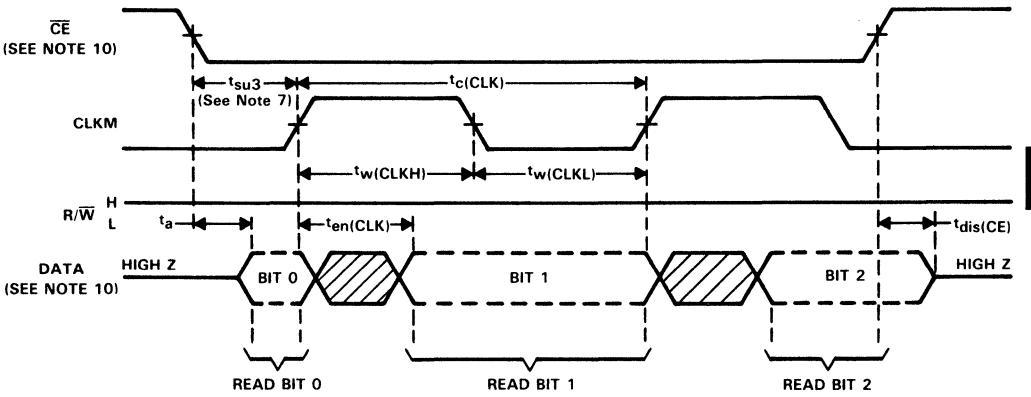


FIGURE 2. SLCC – MICROPROCESSOR TIMING REQUIREMENTS FOR READ OPERATION

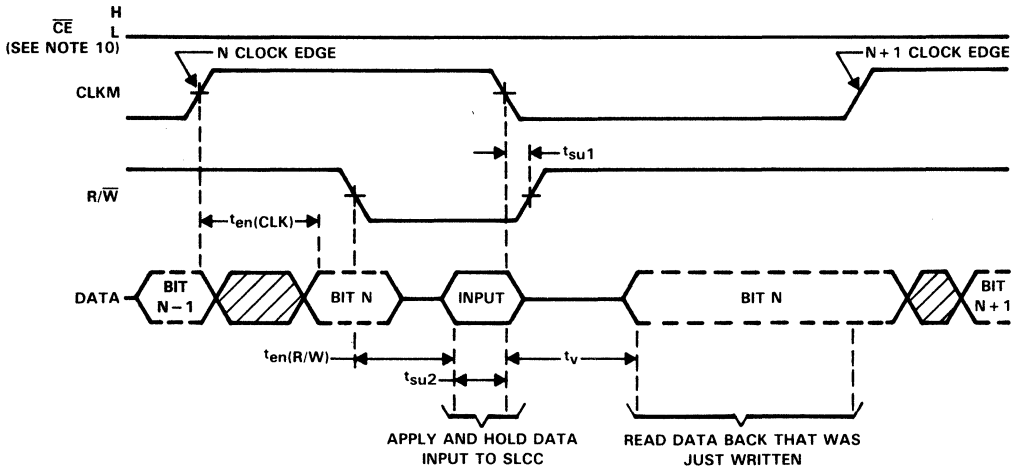


FIGURE 3. SLCC – MICROPROCESSOR TIMING REQUIREMENTS FOR WRITE OPERATION

NOTES: 7. If the user is not interested in reading bit 0, t_{su3} can be a minimum of 30 ns.

10. The DATA pin is an input, an output, or in a high-impedance state. When $\overline{CE}$ is low, the DATA pin will be either an input or an output depending upon the condition of R/$\overline{W}$. When R/$\overline{W}$ is high and $\overline{CE}$ is low, the DATA pin is an output that a microprocessor can poll. When R/$\overline{W}$ is low and $\overline{CE}$ is low, the DATA pin is an input. Dashed lines on the DATA signal indicate that the data on the DATA pin is coming from the SLCC. Solid lines on the DATA signal indicate that the data on the DATA pin is coming from the system. Each time the $\overline{CE}$ input goes low, the bit pointer is reset to bit zero. All rise and fall times are assumed to be 20 ns or less; therefore, timing requirements are shown referenced to 50% of the rising or falling slope of the waveform. A write operation can only be performed when CLKM is high. When CLKM is low, only a read operation can be performed.

PARAMETER MEASUREMENT INFORMATION

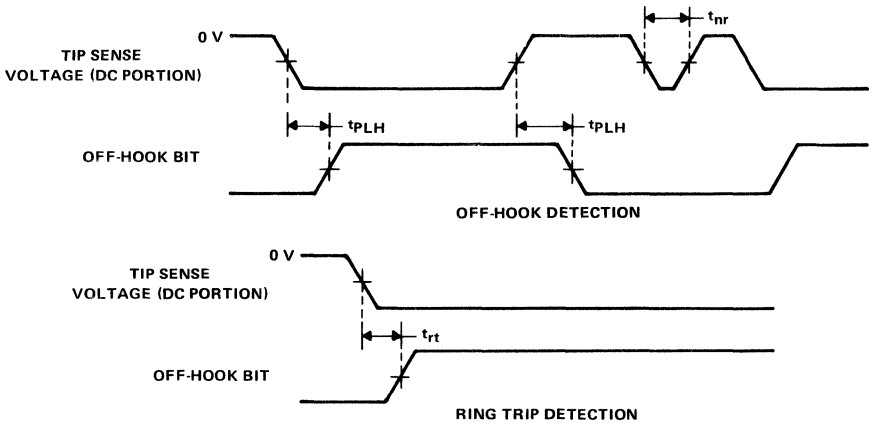
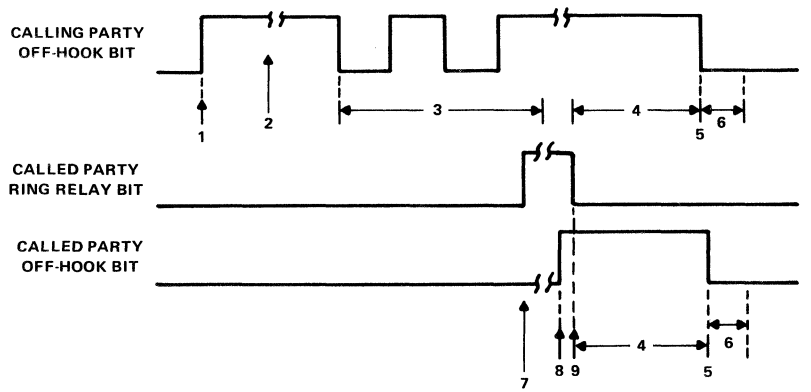


FIGURE 4. SUPERVISION TIMING WAVEFORMS

TYPICAL APPLICATION DATA



1 OFF-HOOK
2 VOICE MODE SET UP BY MICROPROCESSOR
3 DIAL PULSE COLLECTION
4 VOICE (CONVERSATION)
5 ON-HOOK
6 MICROPROCESSOR DETECTS ON-HOOK BY READING BIT "0" AND SET SYSTEM TO STANDBY MODE
7 MICROPROCESSOR ENABLES BIT "3" RING RELAY ON
8 MICROPROCESSOR DETECTS OFF-HOOK BY READING BIT "0"
9 MICROPROCESSOR DISABLES BIT "3" AND SETS THE SLCC TO VOICE MODE

FIGURE 5. MICROPROCESSOR INTERNAL POLLING (TYPICAL SEQUENCE)

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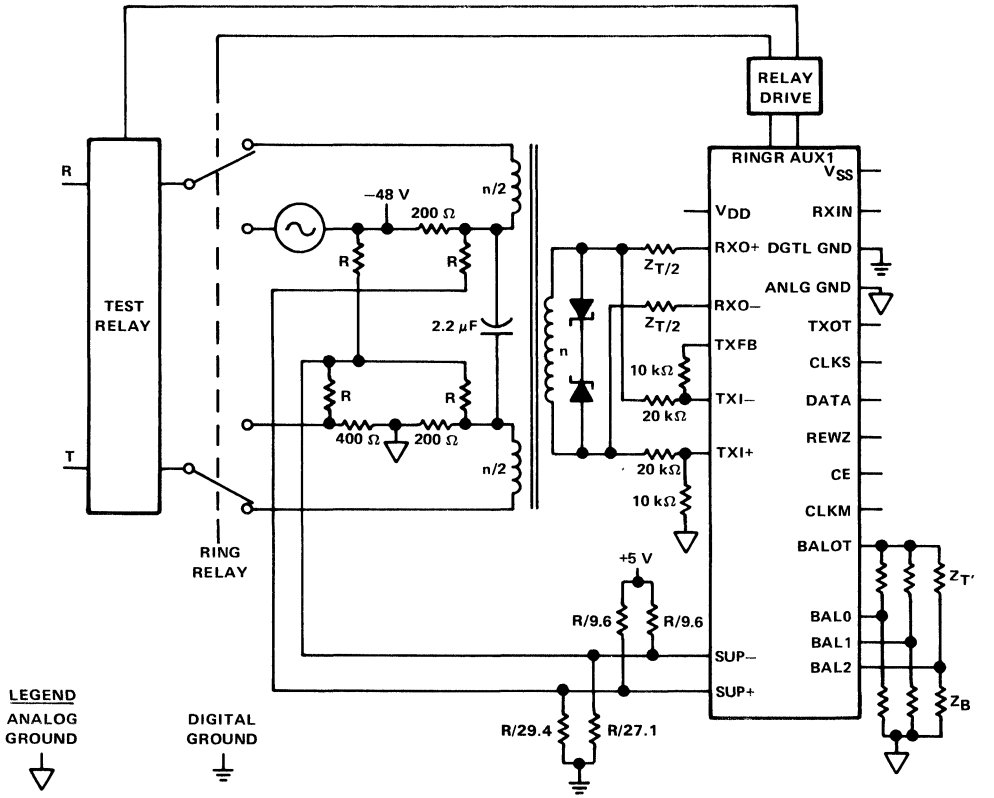
TYPICAL APPLICATION DATA (see Notes 11 and 12)

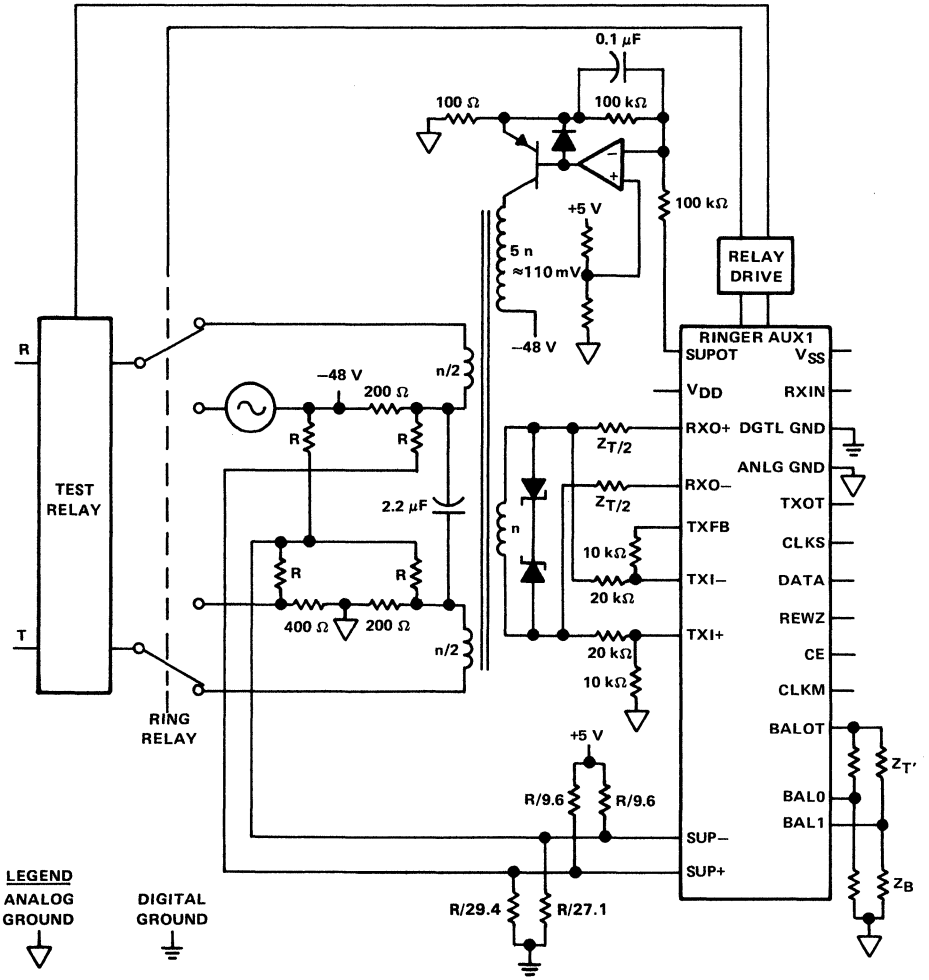


Typically, R = 600 kΩ

FIGURE 6. TCM4204A, TCM4205A SLCC STANDARD SUBSCRIBER LINE

NOTES: 11. All resistors should have tolerances of ±1% or better.
12. If the battery-feed transformer is center tapped on the SLCC side, it is recommended that the center tap be left disconnected.

TYPICAL APPLICATION DATA (see Notes 11 and 12)



Typically, R = 600 kΩ

FIGURE 7. TCM4207A SLCC STANDARD SUBSCRIBER LINE

NOTES: 11. All resistors should have tolerances of ±1% or better.
12. If the battery-feed transformer is center tapped on the SLCC side, it is recommended that the center tap be left disconnected.

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TYPICAL APPLICATION DATA (see Notes 11 and 12)

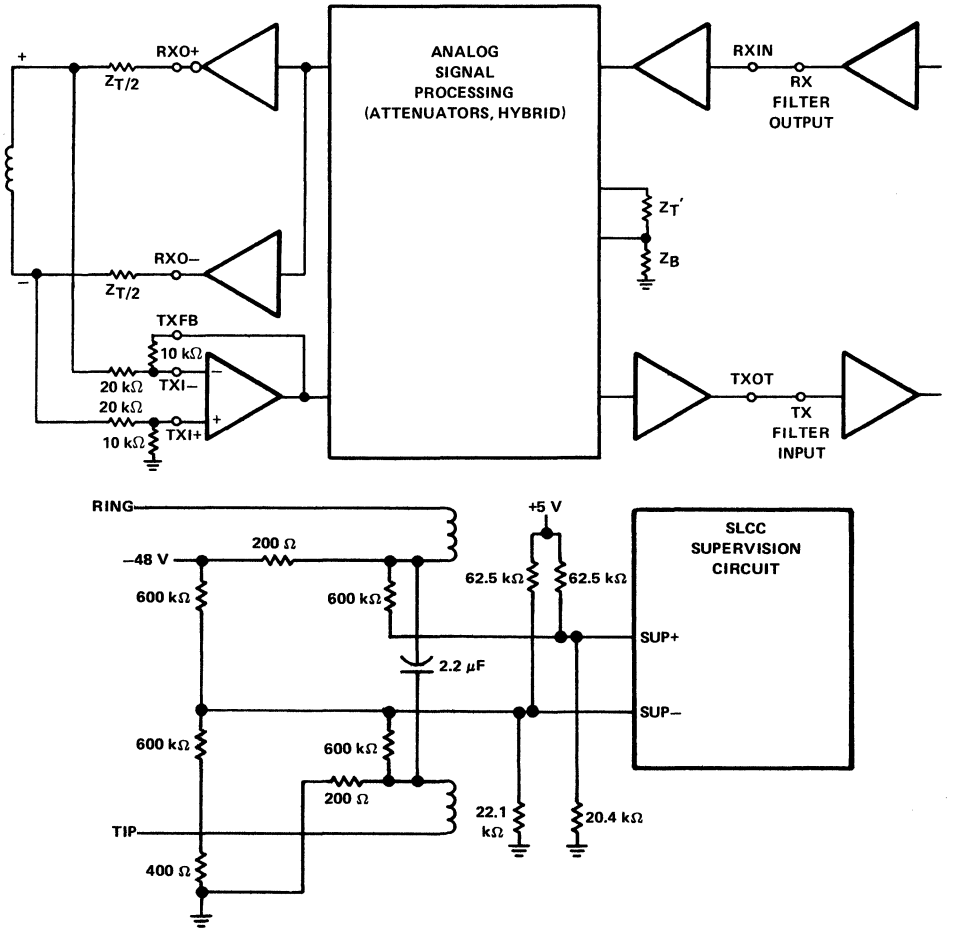


FIGURE 8. INPUT/OUTPUT OFFSETS

NOTES: 11. All resistors should have tolerances of ±1% or better.
12. If the battery-feed transformer is center tapped on the SLCC side, it is recommended that the center tap be left disconnected.

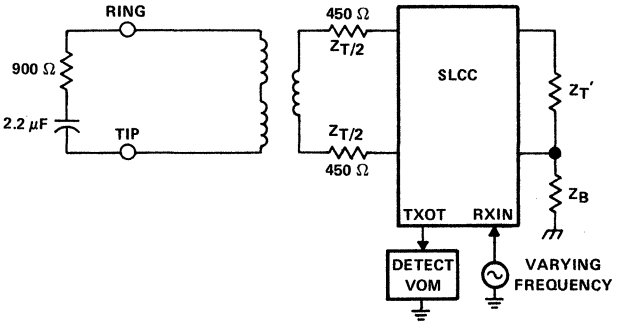


FIGURE 9. STRUCTURAL THL TEST CIRCUIT

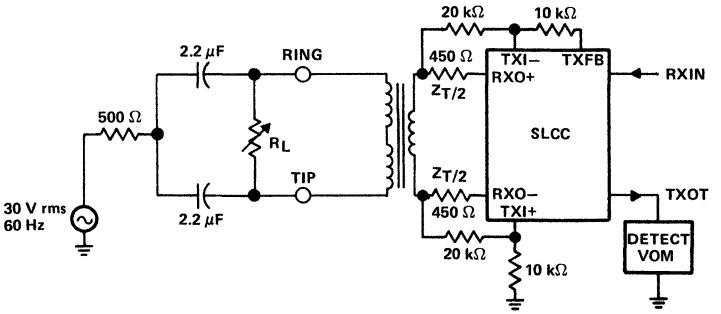
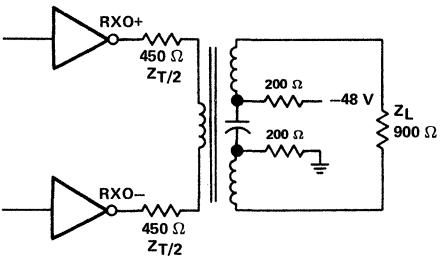


FIGURE 10. LONGITUDINAL REJECTION TEST CIRCUIT



SIGNAL LEVEL AT 900 Ω	ACROSS 900 Ω	DIFFERENTIAL RMS RXO+, RXO–	SINGLE ENDED RXO+, RXO–
6 dBmo	1.8 Vrms	5.34 Vrms	+3.78 Vpp
0 dBmo	0.95 Vrms	2.68 Vrms	+1.89 Vpp
–10 dBmo	0.30 Vrms	0.85 Vrms	+0.60 Vpp
–20 dBmo	95 mVrms	0.27 Vrms	+189 mVpp
–30 dBmo	30 mVrms	85 mVrms	+60 mVpp
–40 dBmo	9.5 mVrms	27 mVrms	+18.9 mVpp
–60 dBmo	950 μVrms	2.7 mVrms	+1.89 mVpp
–80 dBmo	95 μVrms	270 μVrms	+189 μVpp

FIGURE 11. SIGNAL LEVELS, 2W SIDE

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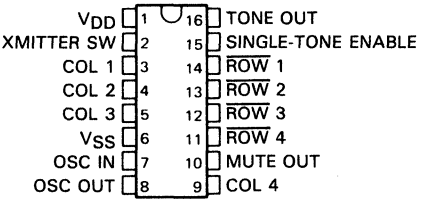
D2650, NOVEMBER 1982—REVISED OCTOBER 1984

- **Low-Cost TV Color-Burst Crystal Sine-Wave Input Produces Highly Accurate and Stable Tones**
- **Device Powered Directly by Telephone or Small Batteries**
- **Keyboard or Electronic Input Capability**
- **Dual-Tone and Single-Tone Capability**
- **Minimal Standby Power Requirement**
- **Total Harmonic Distortion Meets EIA Standard RS-470**
- **PEP3 Processing Available**
- **Wide Supply-Voltage Range**
- **Minimal Parts Required**
- **Single-Tone Production Can be Inhibited**
- **Auxiliary Switching Outputs: One Bipolar Transistor and One CMOS Gate**
- **Designed to be Interchangeable with Mostek MK5087**

N DUAL-IN-LINE PACKAGE
(TOP VIEW)



Caution. These devices have limited built-in gate protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

description

The TCM5087 tone encoder is a CMOS integrated circuit designed specifically to generate the dial tones used in dual-tone telephone dialing systems. It requires a sine-wave input normally supplied by a low-cost TV color-burst crystal at 3.579545 MHz to generate eight different audio sinusoidal frequencies. With this input the encoder generates dial tones that are very low in total harmonic distortion and comply with standard Dual-Tone Multi-Frequency (DTMF) specifications without any need for frequency adjustment.

When generating a dual-tone signal, the encoder generates one column tone and one row tone and adds them for its output. The table below presents the frequencies produced by the tone encoder with the 3.579545-MHz TV-crystal signal input. Any deviation in this frequency will be reflected in the frequency output. The tolerance of the crystal is normally 0.02%.

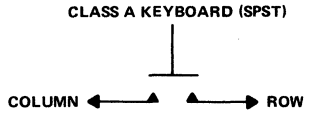
TONE	DTMF STANDARD (Hz)	ENCODER OUTPUT* (Hz)	ERROR FROM STANDARD* (%)
Row 1	697	701.3	+0.62
Row 2	770	771.4	+0.19
Row 3	852	857.2	+0.61
Row 4	941	935.1	−0.63
Column 1	1209	1215.9	+0.57
Column 2	1336	1331.7	−0.32
Column 3	1477	1471.9	−0.35
Column 4	1633	1645	+0.73

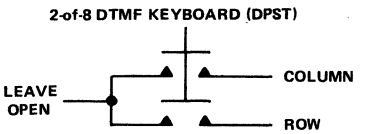
*Using an input signal from a 3.579545-MHz crystal.

operation

keyboard and electronic inputs

The specific tone or tones generated are determined by inputs designated $\overline{\text{ROW}}$ 1 through $\overline{\text{ROW}}$ 4 and COLUMN 1 through COLUMN 4. The inputs are normally received from a 2-of-8 DTMF (DPST) keyboard, a Class A (SPST) keyboard, or an electronic circuit. Unlike dynamic or scanned inputs, the static inputs of the TCM5087 do not generate noise. See function table for input and output description.





single-tone enable input

This input inhibits the generation of single tones when taken low. All other chip functions remain unchanged. If the input is high or left open, single-tone operation is enabled.

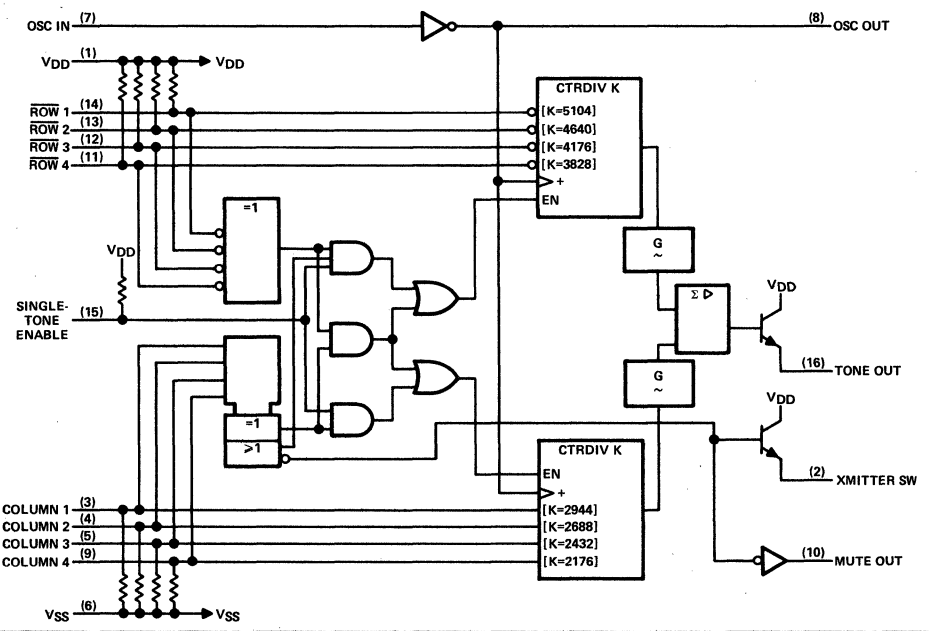
transmitter switch output

This output is at high impedance when one or more of the column inputs are active and is high when all column inputs are inactive. The output is the emitter of a bipolar transistor whose collector is at V_{DD}.

mute output

The mute output is high when one or more column inputs are active and is low when all column inputs are inactive.

functional block diagram



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TONE ENCODER FUNCTION TABLE

INPUT COMBINATIONS†	TONE OUTPUT		MUTE OUTPUT	TRANSMITTER SWITCH OUTPUT
	PIN 15‡ OPEN	PIN 15‡ AT V_{SS}		
0 rows 0 columns	0	0	L	H
1 row 1 column	Row and column	Row and column	H	Hi-Z
2 or more rows 1 column	column	0	H	Hi-Z
1 row 2 or more columns	Row	0	H	Hi-Z
2 or more rows 2 or more columns	0	0	H	Hi-Z
0 rows 1 column	Column	0	H	Hi-Z
0 rows 2 or more columns	0	0	H	Hi-Z
1 or more rows 0 columns	0	0	L	H

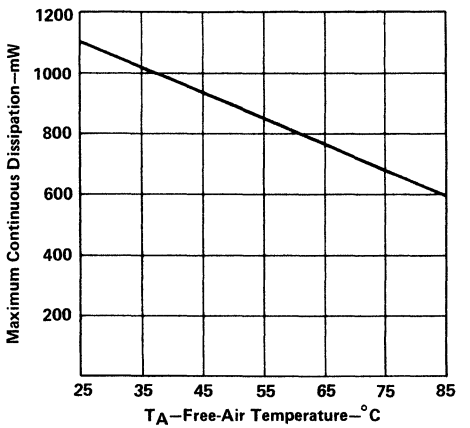
†Row inputs will be active (on) when the input voltage is at a low level ($V_I \leq V_{IL}$), and column inputs are active at a high input level. Under keyboard control, connecting a row input to a column input activates both.
‡Pin 15 is the single-tone disable input.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} (see Note 1) . . . . . 13.5 V
Input voltage range . . . . . −0.3 V to V_{DD} + 0.3 V
Output voltage range . . . . . −0.3 V to V_{DD} + 0.3 V
Continuous power dissipation at 25°C free-air temperature (see Note 2) . . . . . 1150 mW
Operating free-air temperature range . . . . . −30°C to 70°C
Storage temperature range . . . . . −55°C to 150°C

NOTES: 1. All voltage values are with respect to the V_{SS} terminal.
2. For operation above 25°C free-air temperature see the Dissipation Derating Curve.

DISSIPATION DERATING CURVE



recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		3.5		10	V
High-level input voltage, V_{IH}	Row inputs (off)	0.9 V_{DD}		V_{DD}	V
	All other inputs	0.7 V_{DD}		V_{DD}	
Low-level input voltage, V_{IL}	Column inputs (off)	V_{SS}		0.1 V_{DD}	V
	All other inputs	V_{SS}		0.3 V_{DD}	
Contact resistance between row and column inputs				100	Ω
Tone-output load resistance, R_L	$V_{DD} \leq 5$ V		620		Ω
	$V_{DD} > 5$ V		330		Ω
Operating free-air temperature, T_A		−30		70	°C

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
Column or row input resistance				10			kΩ
Single-tone-enable input resistance to V_{DD}			T_A = 25°C	20		100	kΩ
V_{OH}	High-level output voltage	Mute output	V_{DD} = 3 V, I_{OH} = 0.2 mA,	2			V
			V_{DD} = 10 V, I_{OH} = 0.5 mA	9			
		Transmitter switch output	V_{DD} = 3.5 V, I_{OH} = −15 mA	1.5	2.5		
			V_{DD} = 10 V, I_{OH} = − 40 mA	8			
V_{OL}	Low-level output voltage, mute output		V_{DD} = 3 V, I_{OL} = −0.2 mA			0.5	V
			V_{DD} = 10 V, I_{OL} = −0.5 mA			0.5	
I_{OL}	Off-state current transmitter switch output		V_{DD} = 10 V, V_O = 0 V			10	μA
I_{DDstby}	Standby supply current with outputs unloaded		V_{DD} = 3.5 V		0.25	100	μA
			V_{DD} = 10 V		0.5	200	
I_{DDop}	Operating current		V_{DD} = 3.5 V, See Note 3		1	2	mA
			V_{DD} = 10 V, See Note 3		5	10	

operating characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MIN	TYP	MAX	UNIT
Output rms voltage	Row tone	R_L = 330 Ω to 1 kΩ,	317	400	500	mV
	Column tone	T_A = 25°C	396	500	630	
Preemphasis (column tone to row tone)			1	2	3	dB
Dual-tone output distortion (see Note 4)		$V_{DD} \geq 4$ V			−20	dB
Quiescent tone-output power					−80	dBm
Tone-output rise time (see Note 5)				3	5	ms

†Unless otherwise noted, test conditions are: R_L = 620 Ω for $V_{DD} \leq 5$ V or R_L = 330 Ω for $V_{DD} > 5$ V. Crystal parameters are the following: f = 3.579545 MHz ±0.02%, R_S < 100 Ω, C_L = 18 pF, C_M = 0.02 pF, C_H = 5 pF, L_M = 96 mH.

NOTES: 3. Operating current is measured with all outputs unloaded, one row input connected to one column input, and normal oscillator input.

4. Distortion is expressed as the ratio of total out-of-band power relative to the total fundamental power for the dual tone.

5. This is the time required for output to change from its quiescent value to 90% of its final rms value.

output waveforms

Typical row and column stairstep approximations of sinusoidal outputs are shown in Figures 1 and 2. The row and column outputs are added together resulting in a typical dual-tone waveform as shown in Figure 3. Spectral analysis of this dual-tone waveform shows that all harmonic and intermodulation distortions are typically 30 dB below the strongest column-tone fundamental.

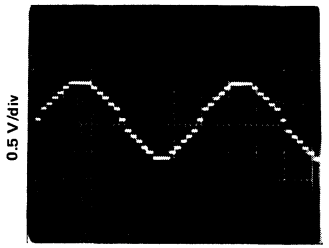


FIGURE 1

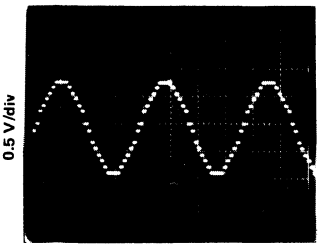


FIGURE 2

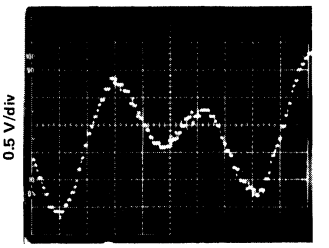


FIGURE 3

distortion considerations

The following formula is used to calculate the total harmonic distortion of a single row or a single column:

$$THD = \left(\frac{\sqrt{V_{2f}^2 + V_{3f}^2 + V_{4f}^2 + V_{5f}^2 + \ldots + V_{nf}^2}}{V_{1f}} \right) \times 100\%$$

where V_{2f} is the second harmonic of the fundamental frequency V_{1f} waveform and so on. The dual-tone total harmonic distortion is:

$$THD = \left(\frac{\sqrt{V_{2R}^2 + V_{3R}^2 + \ldots + V_{nR}^2 + V_{2C}^2 + \ldots V_{nC}^2 \pm V_{IMD}^2}}{\sqrt{V_{FR}^2 + V_{FC}^2}} \right) \times 100\%$$

where V_{FR} and V_{FC} are the row and column fundamental frequency waveforms, and V_{2R} and V_{2C}, etc., are the corresponding harmonics.

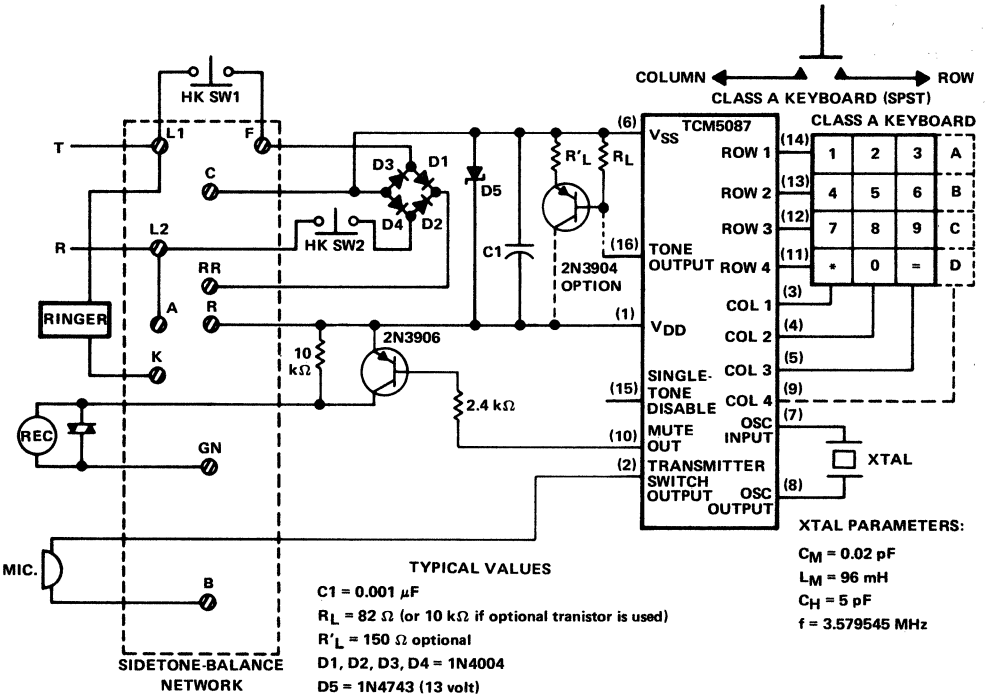
The total intermodulation distortion is:

$$V_{IMD}^2 = (V_{1R} + V_{1C})^2 + (V_{1R} - V_{1C})^2 + \ldots + (V_{nr} + V_{nC})^2 + (V_{nR} - V_{nC})^2$$

A relatively simple method of distortion measurement uses a spectrum analyzer to relate the harmonics to the fundamental frequency waveform. The tone encoder spectrum indicates the harmonics and intermodulation distortion at least 30 dB down relative to the column tone.

Another method for distortion measurement of the dual-tone waveform is to compare the total power in the fundamental frequencies with the total power in the various harmonics plus intermodulation on a signal analyzer. The encoders provide an output distortion of -20 dB maximum when operated between 3.5 volts and 10 volts. If operated between 3 volts and 3.5 volts, some clipping occurs at the output causing the distortion to exceed the -20 dB level.

TYPICAL APPLICATIONS DATA



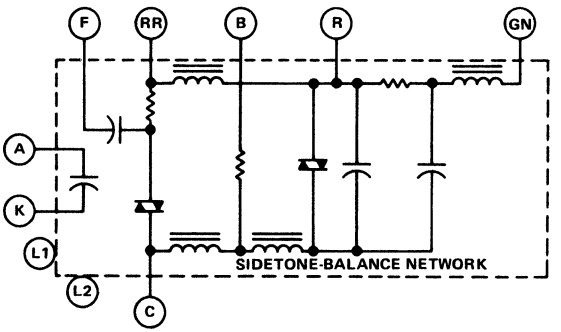


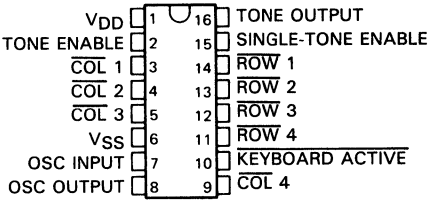
FIGURE 4. TYPICAL APPLICATION USING HYBRID COIL SIDETONE-BALANCE NETWORK, ELECTRONIC SWITCHING, AND LOW-COST (CLASS A) KEYBOARD

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

D2651, NOVEMBER 1982—REVISED OCTOBER 1984

- **Low-Cost TV Color-Burst Crystal Sine-Wave Input Produces Highly Accurate and Stable Tones**
- **Device Powered Directly by Telephone or Small Batteries**
- **Keyboard or Electronic Input Capability**
- **Dual-Tone and Single-Tone Capability**
- **Minimal Standby Power Requirement**
- **Total Harmonic Distortion Meets EIA Standard RS-470**
- **PEP3 Processing Available**
- **Wide Supply-Voltage Range**
- **Minimal External Parts Required**
- **Single-Tone Production Can be Inhibited**
- **Separate Tone Enable Provided**
- **Auxiliary Switching Bipolar Transistor Available**
- **Designed to be Interchangeable with Mostek MK5089**

N PACKAGE
(TOP VIEW)



Caution. These devices have limited built-in gate protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

description

The TCM5089 tone encoder is a CMOS integrated circuit designed specifically to generate the dial tones used in dual-tone telephone dialing systems. It requires a sine-wave input normally supplied by a low-cost TV color-burst crystal at 3.579545 MHz to generate eight different audio sinusoidal frequencies. With this input the encoder generates dial tones that are very low in total harmonic distortion and comply with standard Dual-Tone Multi-Frequency (DTMF) specifications without any need for frequency adjustment.

When generating a dual-tone signal, the encoder generates one column tone and one row tone and adds them for its output. The table below presents the frequencies produced by the tone encoder with the 3.579545-MHz TV-crystal signal input. Any deviation in this frequency will be reflected in the frequency output. The tolerance of the crystal is normally 0.02%.

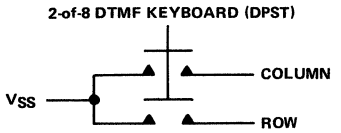
TONE	DTMF STANDARD (Hz)	ENCODER OUTPUT* (Hz)	ERROR FROM STANDARD* (%)
Row 1	697	701.3	+0.62
Row 2	770	771.4	+0.19
Row 3	852	857.2	+0.61
Row 4	941	935.1	−0.63
Column 1	1209	1215.9	+0.57
Column 2	1336	1331.7	−0.32
Column 3	1477	1471.9	−0.35
Column 4	1633	1645	+0.73

*Using an input signal from a 3.579545-MHz crystal.

operation

keyboard and electronic inputs

The specific tone or tones generated are determined by inputs designated $\overline{\text{ROW}}$ 1 through $\overline{\text{ROW}}$ 4 and $\overline{\text{COLUMN}}$ 1 through $\overline{\text{COLUMN}}$ 4. These input levels are normally received from a 2-of-8 DTMF (DPST) keyboard or from an electronic circuit. Unlike dynamic or scanned inputs, the static inputs of the TCM5089 do not generate any noise. See function table for input and output description.



single-tone enable input

This inhibits the generation of single tones when taken low or left open. However, all other chip functions remain unchanged. If the input is high, single-tone operation is enabled.

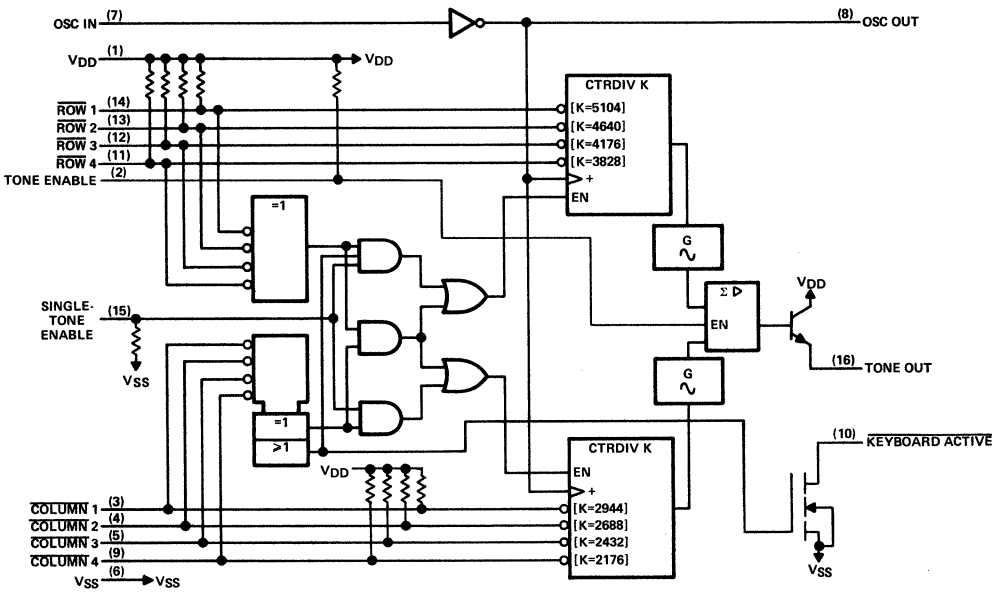
tone enable input

The tone enable input, when low, disables the tone output of the encoder. Other chip functions remain unchanged.

keyboard active output

This output provides for switching of an external receiver, transmitter, or other functions. The output is low whenever one or more column inputs are active and at a high impedance when all column inputs are inactive.

functional block diagram



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TONE ENCODER FUNCTION TABLE

INPUT COMBINATIONS†	TONE OUTPUT			KEYBOARD ACTIVE OUTPUT
	PIN 2 OPEN‡ PIN 15 at V_{DD}‡	PIN 2 OPEN‡ PIN 15 at V_{SS}‡	PIN 2 AT V_{SS}‡	
0 rows 0 Columns	0	0	0	Hi-Z
1 row 1 column	Row and column	Row and column	0	L
2 or more rows 1 column	column	0	0	L
1 row 2 or more columns	Row	0	0	L
2 or more rows 2 or more columns	0	0	0	L
0 rows 1 column	Column	0	0	L
0 rows 2 or more columns	0	0	0	L
1 or more rows 0 columns	0	0	0	Hi-Z

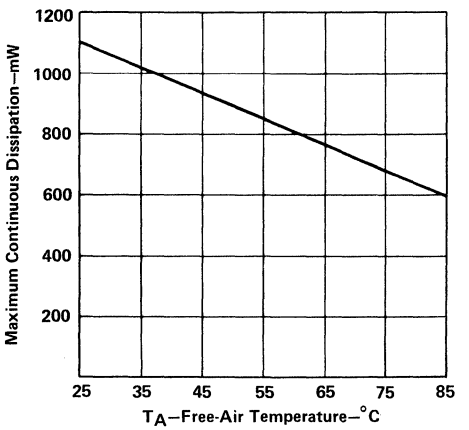
†An inactive level can be produced by an open circuit. Under voltage-level control, row and column inputs will be active when low as defined by V_{IL} in recommended operating conditions.
‡Pin 15 is the single-tone enable input; Pin 2 is the tone-enable input.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} (see Note 1) . . . . . 13.5 V
Input voltage range . . . . . −0.3 V to V_{DD} + 0.3 V
Output voltage range . . . . . −0.3 V to V_{DD} + 0.3 V
Continuous power dissipation at 25°C free-air temperature (see Note 2) . . . . . 1150 mW
Operating free-air temperature range . . . . . −30°C to 70°C
Storage temperature range . . . . . −55°C to 150°C

NOTES: 1. All voltage values are with respect to the V_{SS} terminal.
2. For operation above 25°C see the Dissipation Derating Curve.

DISSIPATION DERATING CURVE



recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	3		10	V
High-level input voltage, any input, V_{IH}	0.7 V_{DD}		V_{DD}	V
Low-level input voltage, any input, V_{IL}	V_{SS}		0.3 V_{DD}	V
Operating free-air temperature, T_A	−30		70	°C

electrical characteristics over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Input resistance, single-tone input to V_{SS}		20		100	kΩ
I_{OH}	High-level output current, keyboard active output	V_O = 5 V†			2	μA
I_{OL}	Low-level output current, keyboard active output	V_O = 0.5 V†	−500			μA
I_{DDstby}	Standby power supply current	V_{DD} = 10 V, See Note 3			200	μA
I_{DDop}	Operating power supply current	V_{DD} = 3.5 V, See Note 4			2	mA

operating characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS‡	MIN	TYP	MAX	UNIT
Output rms voltage	Row tone	V_{DD} = 3.5 V, R_L = 10 kΩ	235		365	mV
	Column tone		275		516	
Preemphasis (column-tone to row-tone)		R_L = 10 kΩ	2.4		3	dB
Dual-tone output distortion (see Note 5)		V_{DD} ≥ 3.5 V, R_L = 10 kΩ			−20	dB
Quiescent tone-output power		R_L = 10 kΩ			−80	dBm
Tone-output rise time (see Note 6)				2.8	5	ms

†V_O is the dc bias on the keyboard-active output.
‡Crystal parameters are as follows: f = 3.579545 MHz ±0.02%, R_S ≤ 100 Ω, C_L = 18 pF, C_M = 0.02 pF, and L_M = 96 mH.

NOTES: 3. Standby power supply current is measured with no inputs activated.
4. Operating current is measured with all outputs unloaded, one row inut and one column input active, and normal oscillator input.
5. Distortion is expressed as the ratio of total out-of-band power relative to the total fundamental power for the dual tone.
6. This is the time required for the output to change from its quiescent value to 90% of its final rms value.

output waveforms

Typical row and column stairstep approximations of sinusoidal outputs are shown in Figures 1 and 2. The row and column outputs are added together resulting in a typical dual-tone waveform as shown in Figure 3. Spectral analysis of this dual-tone waveform shows that all harmonic and intermodulation distortions are typically 30 dB below the strongest column-tone fundamental.

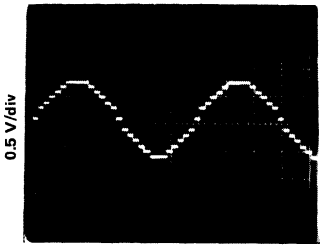


FIGURE 1

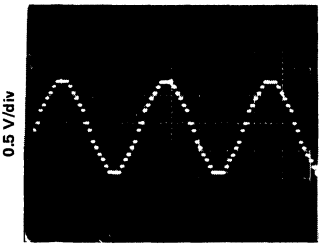


FIGURE 2

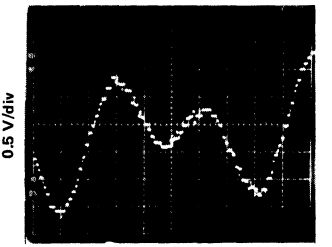


FIGURE 3

distortion considerations

The following formula is used to calculate the total harmonic distortion of a single row or a single column:

$$THD = \left(\frac{\sqrt{V_{2f}^2 + V_{3f}^2 + V_{4f}^2 + V_{5f}^2 + \ldots + V_{nf}^2}}{V_{1f}} \right) \times 100\%$$

where V_{2f} is the second harmonic of the fundamental frequency V_{1f} waveform and so on. The dual-tone total harmonic distortion is:

$$THD = \left(\frac{\sqrt{V_{2R}^2 + V_{3R}^2 + \ldots + V_{nR}^2 + V_{2C}^2 + \ldots V_{nC}^2 \pm V_{IMD}^2}}{\sqrt{V_{FR}^2 + V_{FC}^2}} \right) \times 100\%$$

where V_{FR} and V_{FC} are the row and column fundamental frequency waveforms, and V_{2R} and V_{2C}, etc. are the corresponding harmonics.

The total intermodulation distortion is:

$$V_{IMD}^2 = (V_{1R} + V_{1C})^2 + (V_{1R} - V_{1C})^2 + \ldots + (V_{nr} + V_{nC})^2 + (V_{nR} - V_{nC})^2$$

A relatively simple method of distortion measurement uses a spectrum analyzer to relate the harmonics to the fundamental frequency waveform. The tone encoder spectrum indicates the harmonics and intermodulation distortion at least 30 dB down relative to the column tone.

Another method for distortion measurement of the dual-tone waveform is to compare the total power in the fundamental frequencies with the total power in the various harmonics plus intermodulation on a signal analyzer. The encoders provide an output distortion of −20 dB maximum when operated between 3.5 volts and 10 volts. If operated between 3 volts and 3.5 volts, some clipping occurs at the output causing the distortion to exceed the −20 dB level.

APPLICATIONS INFORMATION

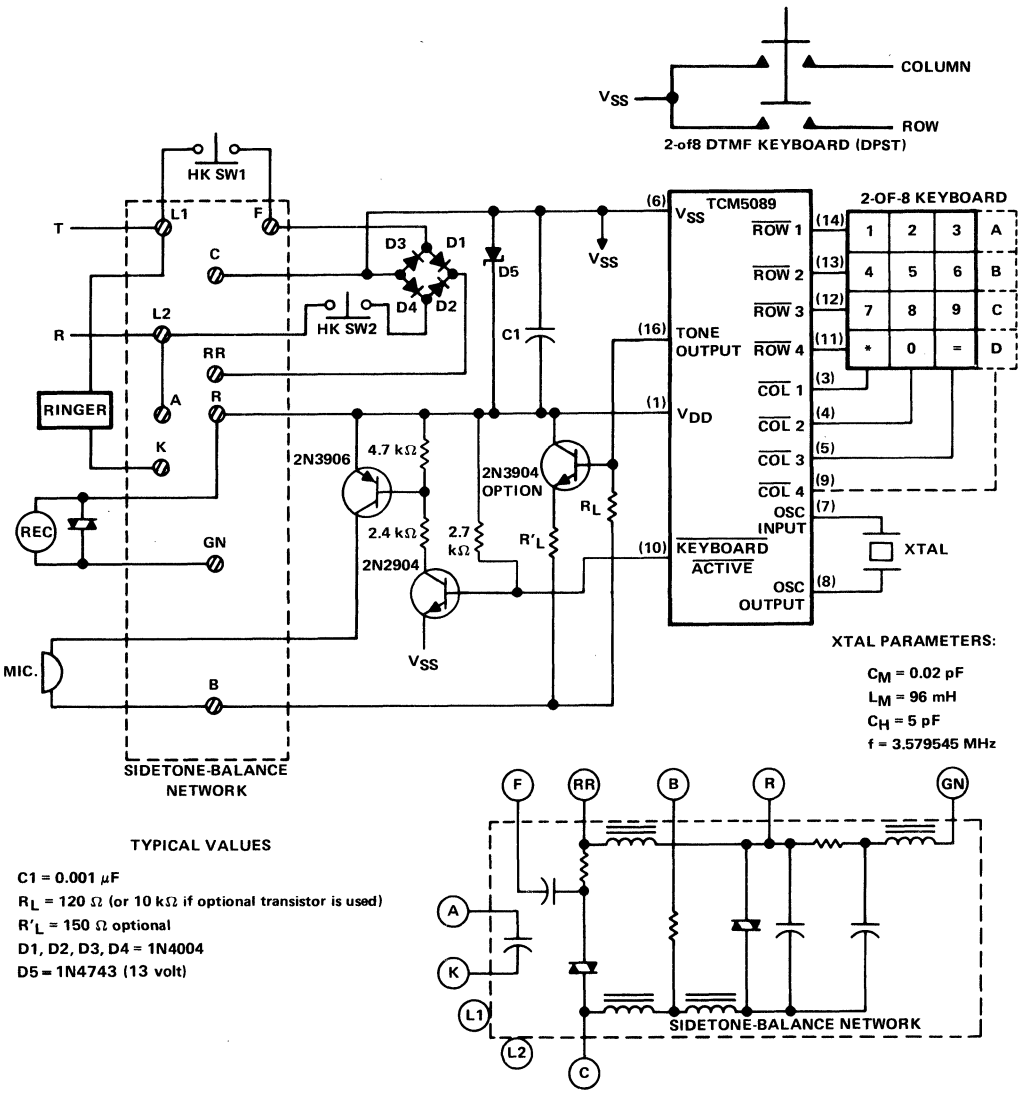
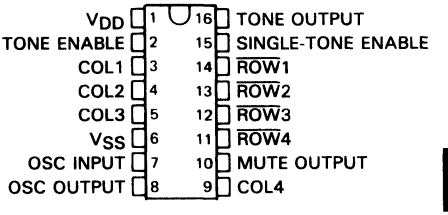


FIGURE 4. TYPICAL APPLICATION USING HYBRID COIL SIDETONE-BALANCE NETWORK, ELECTRONIC SWITCHING, AND LOW-COST (CLASS A) KEYBOARD

D2652, NOVEMBER 1982—REVISED APRIL 1988

- **Low-Cost TV Color-Burst Crystal Sine-Wave Input Produces Highly Accurate and Stable Tones**
- **Device Powered Directly by Telephone or Small Batteries**
- **Keyboard or Electronic Input Capability**
- **Dual-Tone and Single-Tone Capability**
- **Minimal Standby Power Requirement**
- **Total Harmonic Distortion Meets Industry Standards**
- **PEP3 Processing Available**
- **Wide Supply-Voltage Range**
- **Minimal Parts Required**
- **Single-Tone Production Can Be Inhibited**
- **Auxiliary Switching Outputs: One Bipolar Transistor and One CMOS Gate**
- **Designed to be Interchangeable with Mostek MK5092**

N PACKAGE
(TOP VIEW)



Caution. These devices have limited built-in gate protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

description

The TCM5092 tone encoder is a CMOS integrated circuit designed specifically to generate the dial tones used in dual-tone telephone dialing systems. It requires a sine-wave input normally supplied by a low-cost TV color-burst crystal at 3.579545 MHz to generate eight different audio sinusoidal frequencies. With this input the encoder generates dial tones that are very low in total harmonic distortion and comply with standard Dual-Tone Multi-Frequency (DTMF) specifications without any need for frequency adjustment.

When generating a dual-tone signal, the encoder generates one column tone and one row tone and adds them for its output. The table below presents the frequencies produced by the tone encoder with the 3.579545-MHz TV-crystal signal input. Any deviation in this frequency will be reflected in the frequency output. The tolerance of the crystal is normally 0.02%.

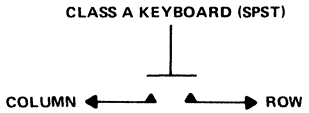
TONE	DTMF STANDARD (Hz)	ENCODER OUTPUT* (Hz)	ERROR FROM STANDARD* (%)
Row 1	697	701.3	+0.62
Row 2	770	771.4	+0.19
Row 3	852	857.2	+0.61
Row 4	941	935.1	−0.63
Column 1	1209	1215.9	+0.57
Column 2	1336	1331.7	−0.32
Column 3	1477	1471.9	−0.35
Column 4	1633	1645	+0.73

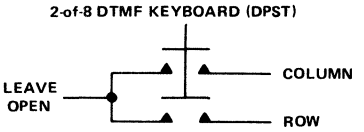
*Using an input signal from a 3.579545-MHz crystal.

operation

keyboard and electronic inputs

The specific tone or tones generated are determined by inputs designated $\overline{\text{ROW}}1$ through $\overline{\text{ROW}}4$ and COLUMN 1 through COLUMN 4. The inputs are normally received from a 2-of-8 DTMF (DPST) keyboard, a Class A (SPST) keyboard, or an electronic circuit. Unlike dynamic or scanned inputs, the static inputs of the TCM5092 do not generate any noise. See function table for input and output description.





single-tone enable input

This input inhibits the generation of single tones when taken low. However, all other chip functions remain unchanged. If the input is high, single-tone operation is enabled.

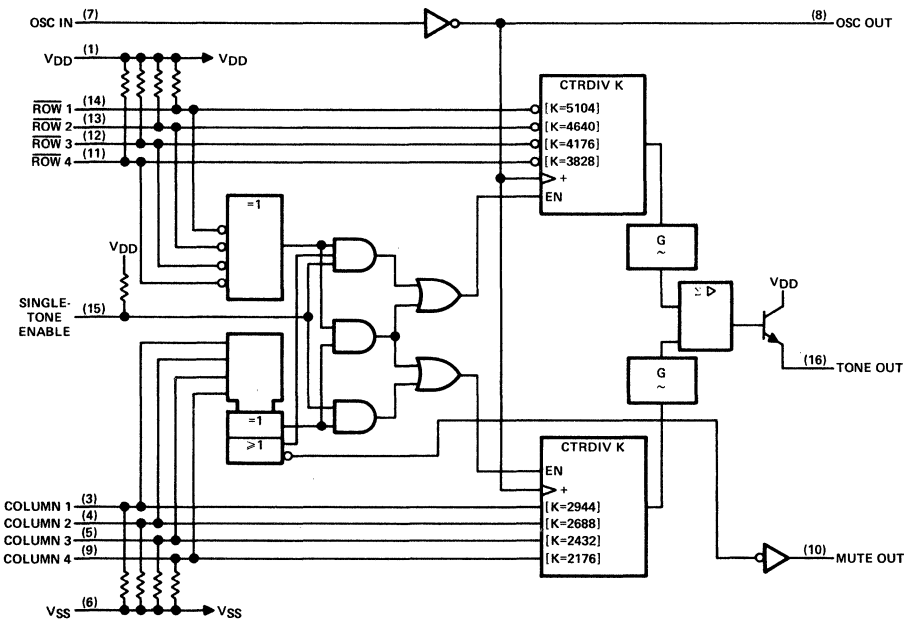
tone enable input

A low logic level at this input inhibits tone generation of the encoder. Other chip functions remain unchanged.

mute output

The mute output is high when any column input is active and is low when all column inputs are inactive.

functional block diagram



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

TONE ENCODER FUNCTION TABLE

INPUT COMBINATIONS†	TONE OUTPUT			MUTE OUTPUT
	PIN 2 OPEN,‡ PIN 15 OPEN‡	PIN 2 OPEN,‡ PIN 15 AT V_{SS}‡	PIN 2 AT V_{SS}‡	
0 rows 0 columns	0	0	0	L
1 row 1 column	Row and column	Row and column	0	H
2 or more rows 1 column	column	0	0	H
1 row 2 or more columns	Row	0	0	H
2 or more rows 2 or more columns	0	0	0	H
0 rows 1 column	Column	0	0	H
0 rows 2 or more columns	0	0	0	H
1 or more rows 0 columns	0	0	0	L

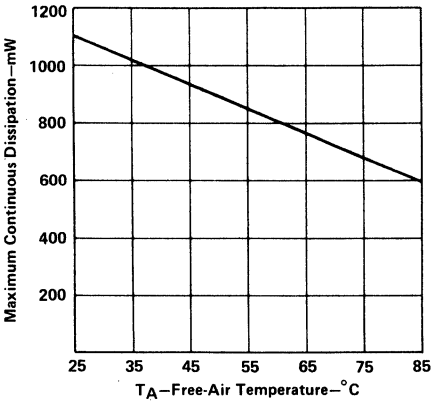
†Row inputs will be active (on) when the input voltage is at a low level ($V_I \leq V_{IL}$), and column inputs are active at a high input level. Under keyboard control, connecting a row input to a column input will activate both.
‡Pin 15 is the single-tone enable input; pin 2 is the tone-enable input.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} (see Note 1) . . . . . 13.5 V
Input voltage range . . . . . -0.3 V to V_{DD} + 0.3 V
Output voltage range . . . . . -0.3 V to V_{DD} + 0.3 V
Continuous power dissipation at 25°C free-air temperature (see Note 2) . . . . . 1150 mW
Operating free-air temperature range . . . . . -30°C to 70°C
Storage temperature range . . . . . -55°C to 150°C

NOTES: 1. All voltage values are with respect to the V_{SS} terminal.
2. For operation above 25°C free-air temperature, see the Dissipation Derating Curve.

DISSIPATION DERATING CURVE



recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		3.5		10	V
High-level input voltage, V_{IH}	Row inputs (off)	0.9 V_{DD}		V_{DD}	V
	All other inputs	0.7 V_{DD}		V_{DD}	
Low-level input voltage, V_{IL}	Column inputs (off)	V_{SS}		0.1 V_{DD}	V
	All other inputs	V_{SS}		0.3 V_{DD}	
Contact resistance between row and column inputs				1000	Ω
Tone-output load resistance, R_L	V_{DD} < 5 V, V_B = −1.5 V†		620		Ω
	V_{DD} ≥ 5 V, V_B = −3.5 V†		330		Ω
Operating free-air temperature, T_A		−30		70	°C

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage, mute output		V_{DD} = 3 V, I_{OH} = 0.2 mA,	2			V
			V_{DD} = 10 V, I_{OH} = 0.5 mA	9			
V_{OL}	Low-level output voltage, mute output		V_{DD} = 3 V, I_{OL} = −0.2 mA			0.5	V
			V_{DD} = 10 V, I_{OL} = −0.5 mA			0.5	
I_I	Input current	Column inputs	V_{DD} = 3 V, V_I = 2.1 V			130	μA
			V_{DD} = 10 V, V_I = 7 V			545	
		Row inputs	V_{DD} = 3 V, V_I = 0.9 V			−130	μA
			V_{DD} = 10 V, V_I = 3 V			−545	
$I_{DD\ stby}$	Standby supply current		V_{DD} = 10 V, See Note 3			200	μA
$I_{DD\ op}$	Operating current		V_{DD} = 5 V, T_A = 25°C, See Note 4			10	mA

operating characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS‡	MIN	TYP	MAX	UNIT
Output rms voltage	Row tone	V_{DD} = 3.8 V, V_B = 1.5 V†, T_A = 25°C	422		531	mV
		V_{DD} = 10 V, V_B = 3.5 V†, T_A = 25°C	441		555	
	Column tone	V_{DD} = 3.8 V, V_B = 1.5 V†, T_A = 25°C	528		664	
		V_{DD} = 10 V, V_B = 3.5 V†, T_A = 25°C	551		693	
Preemphasis (column tone to row tone)			1		3	dB
Output distortion	Dual-tone	V_{DD} ≥ 5 V, T_A = 25°C, See Note 5			−20	dB
Quiescent tone-output power					−80	dBm
Tone-output rise time (see Note 6)		V_{DD} = 3.8 V, V_B = 1.5 V†			5	ms
		V_{DD} = 10 V, V_B = 3.5 V†			5	

†V_B is the negative dc bias applied to the tone output through R_L.
‡Unless otherwise noted, test conditions are : R_L = 620 Ω for V_{DD} < 5 V or R_L = 330 Ω for V_{DD} ≥ 5 V. Crystal parameters are the following: f = 3.579545 MHz ±0.02%, R_S = 100 Ω, C_L = 18 pF, C_H = 5 pF, C_M = 0.02 pF, L_M = 96 mH.

NOTES: 3. Standby supply current is measured with all outputs unloaded and no inputs activated.
4. Operating supply current is measured with all outputs unloaded, one row input connected to one column input, and normal oscillator input.
5. Distortion measurements are in terms of the total out-of-band power relative to the total column and row fundamental power.
6. This is the time required for output to change from its quiescent value to 90% of its final rms value.

output waveforms

Typical row and column stairstep approximations of sinusoidal outputs are shown in Figures 1 and 2. The row and column outputs are added together resulting in a typical dual-tone waveform as shown in Figure 3. Spectral analysis of this dual-tone waveform shows that all harmonic and intermodulation distortions are typically 30 dB below the strongest column-tone fundamental.

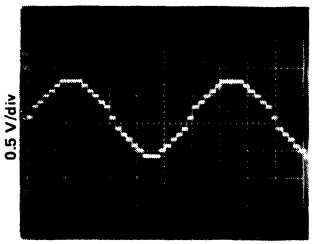


FIGURE 1

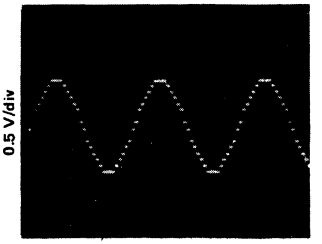


FIGURE 2

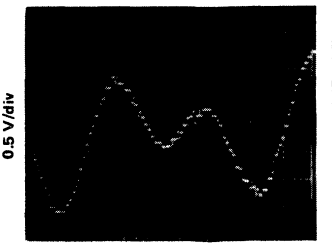


FIGURE 3

distortion considerations

The following formula is used to calculate the total harmonic distortion of a single row or a single column:

$$\text{THD} = \left(\frac{\sqrt{V_{2f}^2 + V_{3f}^2 + V_{4f}^2 + V_{5f}^2 + \ldots + V_{nf}^2}}{V_{1f}}\right) \times 100\%$$

where V_{2f} is the second harmonic of the fundamental frequency V_{1f} waveform and so on. The dual-tone total harmonic distortion is:

$$\text{THD} = \left(\frac{\sqrt{V_{2R}^2 + V_{3R}^2 + \ldots + V_{nR}^2 + V_{2C}^2 + \ldots V_{nC}^2 \pm V_{IMD}^2}}{\sqrt{V_{FR}^2 + V_{FC}^2}}\right) \times 100\%$$

where V_{FR} and V_{FC} are the row and column fundamental frequency waveforms, and V_{2R} and V_{2C}, etc., are the corresponding harmonics.

The total intermodulation distortion is:

$$V_{IMD}^2 = (V_{1R} + V_{1C})^2 + (V_{1R} - V_{1C})^2 + \ldots + (V_{nr} + V_{nC})^2 + (V_{nR} - V_{nC})^2$$

A relatively simple method of distortion measurement uses a spectrum analyzer to relate the harmonics to the fundamental frequency waveform. The tone encoder spectrum indicates the harmonics and intermodulation distortion at least 30 dB down relative to the column tone.

Another method for distortion measurement of the dual-tone waveform is to compare the total power in the fundamental frequencies with the total power in the various harmonics plus intermodulation on a signal analyzer. The encoders provide an output distortion of −20 dB maximum when operated between 3.5 volts and 10 volts. If operated between 3 volts and 3.5 volts, some clipping occurs at the output causing the distortion to exceed the −20 dB level.

APPLICATIONS INFORMATION

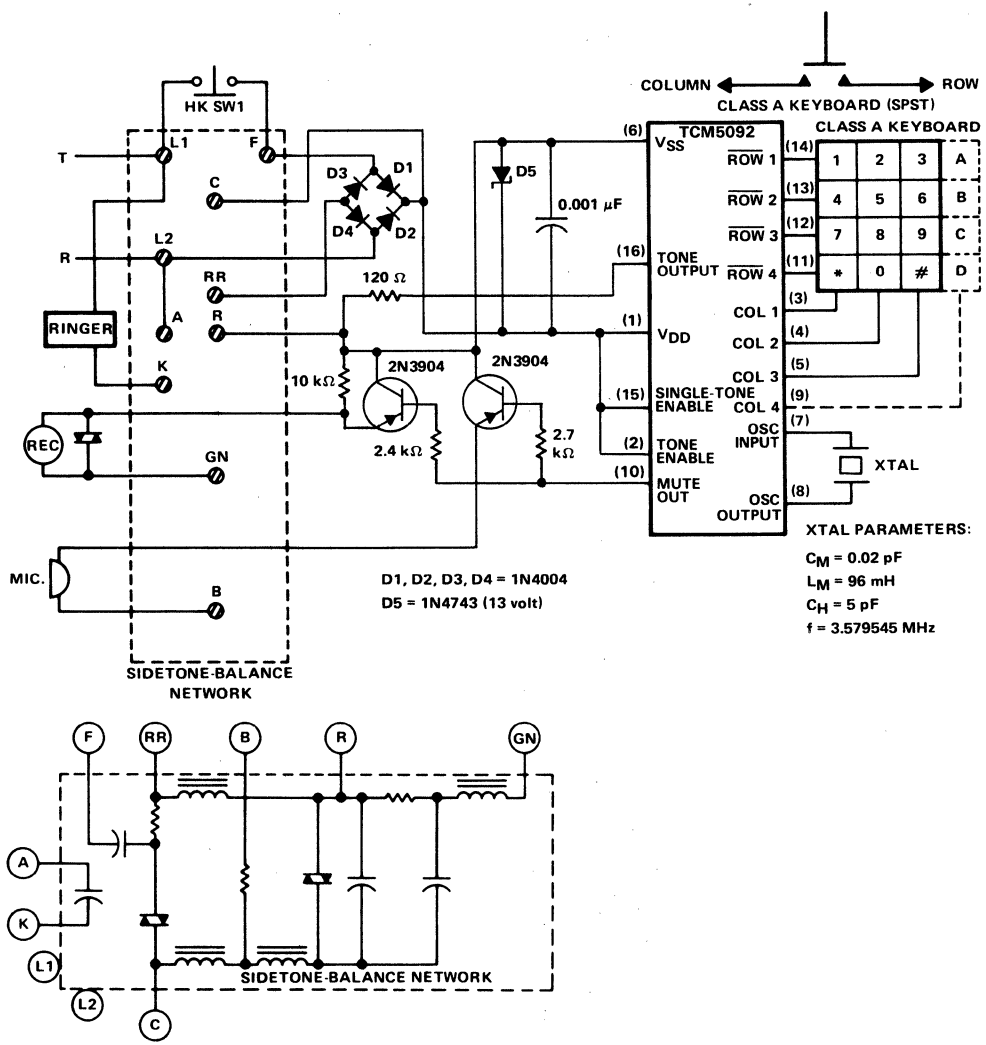


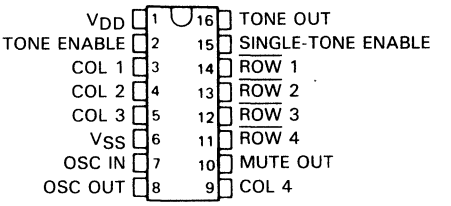
FIGURE 4. TYPICAL APPLICATION USING HYBRID COIL SIDETONE-BALANCE NETWORK, ELECTRONIC SWITCHING, AND LOW-COST (CLASS A) KEYBOARD

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

D3099, OCTOBER 1987—REVISED FEBRUARY 1988

- **Low-Cost TV Color-Burst Crystal Sine-Wave Input Produces Highly Accurate and Stable Tones**
- **Device Powered Directly by Telephone or Small Batteries**
- **Keyboard or Electronic Input Capability**
- **Dual-Tone and Single-Tone Capability**
- **Minimal Standby Power Requirement**
- **Total Harmonic Distortion Meets Industry Standards**
- **PEP3 Processing Available**
- **Wide Supply-Voltage Range**
- **Minimal Parts Required**
- **Single-Tone Production Can Be Inhibited**
- **Auxiliary Switching Outputs: One Bipolar Transistor and One CMOS Gate**
- **Mute Output Can Switch at $V_{DD} \geq 1.7$ V**
- **Designed to be Interchangeable with Mostek MK5094**

N PACKAGE
(TOP VIEW)



description

The TCM5094 tone encoder is a CMOS integrated circuit designed specifically to generate the dial tones used in dual-tone telephone dialing systems. It requires a sine-wave input normally supplied by a low-cost TV color-burst crystal at 3.579545 MHz to generate eight different audio sinusoidal frequencies. With this input, the encoder generates dial tones that are very low in total harmonic distortion and comply with standard Dual-Tone Multi-Frequency (DTMF) specifications without any need for frequency adjustment.

When generating a dual-tone signal, the encoder generates one column tone and one row tone and adds them for its output. The table below presents the frequencies produced by the tone encoder with the 3.579545-MHz TV-crystal signal input. Any deviation in this frequency will be reflected in the frequency output. The tolerance of the crystal is normally 0.02%.

TONE	DTMF STANDARD (Hz)	ENCODER OUTPUT* (Hz)	ERROR FROM STANDARD* (%)
Row 1	697	701.3	+0.62
Row 2	770	771.4	+0.19
Row 3	852	857.2	+0.61
Row 4	941	935.1	−0.63
Column 1	1209	1215.9	+0.57
Column 2	1336	1331.7	−0.32
Column 3	1477	1471.9	−0.35
Column 4	1633	1645	+0.73

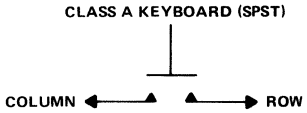
*Using an input signal from a 3.579545-MHz crystal.

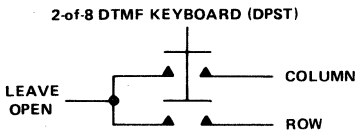
Caution. These devices have limited built-in gate protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

operation

keyboard and electronic inputs

The specific tone or tones generated are determined by inputs designated $\overline{\text{ROW}}$ 1 through $\overline{\text{ROW}}$ 4 and COLUMN 1 through COLUMN 4. The inputs are normally received from a 2-of-8 DTMF (DPST) keyboard, a Class A (SPST) keyboard, or an electronic circuit. Unlike dynamic or scanned inputs, the static inputs of the TCM5094 do not generate any noise. See function table for input and output description.





single-tone enable input

This input inhibits the generation of single tones when taken low. However, all other chip functions remain unchanged. If the input is high or left open, single-tone operation is enabled.

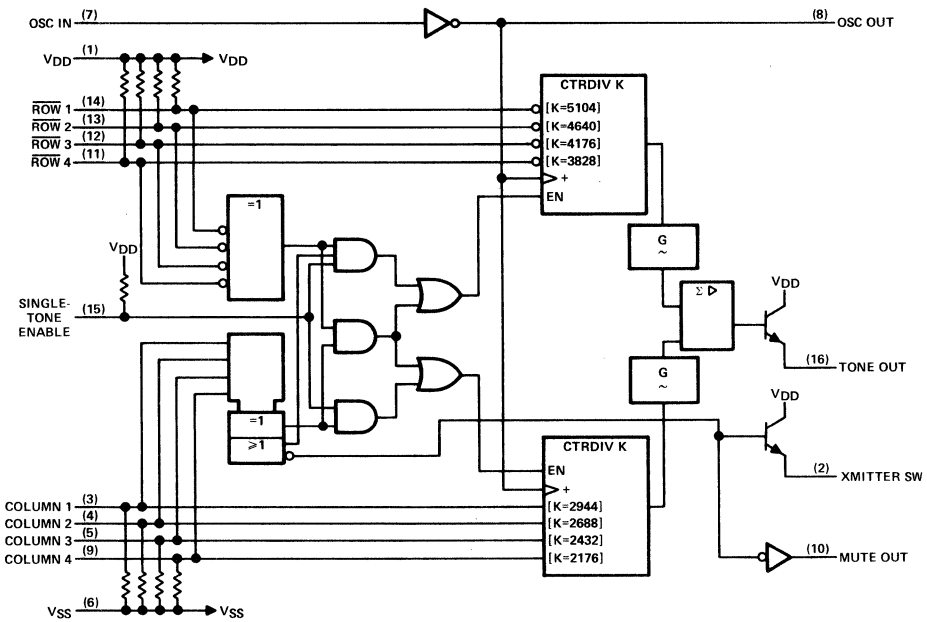
tone-enable input

A low logic level at this input inhibits tone generation of the encoder. Other chip functions remain unchanged.

mute output

The mute output is high when any column input is active and is low when all column inputs are inactive. The mute output operates with V_{DD} as low as 1.7 V.

functional block diagram



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TONE ENCODER FUNCTION TABLE

INPUT COMBINATIONS†	TONE OUTPUT			MUTE OUTPUT
	PIN 2 OPEN,‡ PIN 15 OPEN‡	PIN 2 OPEN,‡ PIN 15 AT V_{SS}‡	PIN 2 AT V_{SS}‡	
0 rows 0 columns	0	0	0	L
1 row 1 column	Row and column	Row and column	0	H
2 or more rows 1 column	Column	0	0	H
1 row 2 or more columns	Row	0	0	H
2 or more rows 2 or more columns	0	0	0	H
0 rows 1 column	Column	0	0	H
0 rows 2 or more columns	0	0	0	H
1 or more rows 0 columns	0	0	0	L

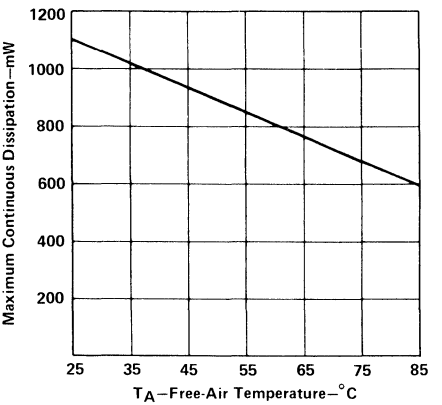
†Row inputs will be active (on) when the input voltage is at a low level ($V_I \leq V_{IL}$), and column inputs are active at a high input level. Under keyboard control, connecting a row input to a column input will activate both.
‡Pin 15 is the single-tone enable input; pin 2 is the tone enable input.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} (see Note 1) . . . . . 13.5 V
Input voltage range . . . . . -0.3 V to V_{DD} + 0.3 V
Output voltage range . . . . . -0.3 V to V_{DD} + 0.3 V
Continuous power dissipation at 25°C free-air temperature (see Note 2) . . . . . 1150 mW
Operating free-air temperature range . . . . . −30°C to 70°C
Storage temperature range . . . . . −55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. All voltage values are with respect to the V_{SS} terminal.
2. For operation above 25°C free-air temperature, see the Dissipation Derating Curve.

DISSIPATION DERATING CURVE



recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		3.5		10	V
High-level input voltage, V_{IH}	Row inputs (off)	0.9 V_{DD}		V_{DD}	V
	All other inputs	0.7 V_{DD}		V_{DD}	
Low-level input voltage, V_{IL}	Column inputs (off)	V_{SS}		0.1 V_{DD}	V
	All other inputs	V_{SS}		0.3 V_{DD}	
Contact resistance between row and column inputs				1000	Ω
Tone-output load resistance, R_L	V_{DD} < 5 V		620		Ω
	V_{DD} ≥ 5 V		330		
Operating free-air temperature, T_A		−30		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage, mute output		V_{DD} = 1.7 V, I_{OH} = 0.2 mA	1		V
			V_{DD} = 10 V, I_{OH} = 0.5 mA	9		
V_{OL}	Low-level output voltage, mute output		V_{DD} = 1.7 V, I_{OL} = −0.2 mA		0.5	V
			V_{DD} = 10 V, I_{OL} = −0.5 mA		0.5	
I_I	Input current	Column Inputs	V_{DD} = 3 V, V_I = 2.1 V		130	μA
			V_{DD} = 10 V, V_I = 7 V		545	
		Row Inputs	V_{DD} = 3 V, V_I = 0.9 V		−130	μA
			V_{DD} = 10 V, V_I = 3 V		−545	
I_{DDstby}	Standby supply current		V_{DD} = 10 V, See Note 3		200	μA
I_{DDop}	Operating current		V_{DD} = 5 V, T_A = 25°C, See Note 4		10	mA

operating characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MIN	MAX	UNIT
Output rms voltage	Row tone	V_{DD} = 3.8 V, R_L = 320 Ω, T_A = 25°C	360	453	mV
		V_{DD} = 10 V, R_L = 320 Ω, T_A = 25°C	452	569	
	Column tone	V_{DD} = 3.8 V, R_L = 320 Ω, T_A = 25°C	387	487	
		V_{DD} = 10 V, R_L = 320 Ω, T_A = 25°C	486	612	
Preemphasis (column tone to row tone)		T_A = 25°C	1	3	dB
Output distortion	Dual-tone	V_{DD} ≥ 5 V, T_A = 25°C, See Note 5		−20	dB
Quiescent tone-output power				−80	dBm
Tone-output rise time (see Note 6)		V_{DD} = 3.8 V		5	ms
		V_{DD} = 10 V		5	

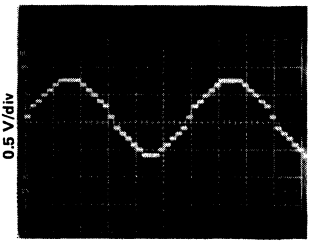
†Unless otherwise noted, test conditions are: R_L = 620 Ω for V_{DD} < 5 V or R_L = 330 Ω for V_{DD} ≥ 5 V. Crystal parameters are the following: f = 3.579545 MHz ±0.02%, R_S < 100 Ω, C_L = 18 pF, C_H = 5 pF, C_M = 0.02 pF, L_M = 96 mH.

NOTES: 3. Standby supply current is measured with all outputs unloaded and no inputs activated.
4. Operating supply current is measured with all outputs unloaded, one row input connected to one column input, and normal oscillator input.
5. Distortion measurements are in terms of the total out-of-band power relative to the total column and row fundamental power.
6. This is the time required for output to change from its quiescent value to 90% of its final rms value.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

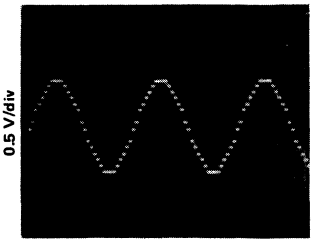
output waveforms

Typical row and column stairstep approximations of sinusoidal outputs are shown in Figures 1 and 2. The row and column outputs are added together resulting in a typical dual-tone waveform as shown in Figure 3. Spectral analysis of this dual-tone waveform shows that all harmonic and intermodulation distortions are typically 30 dB below the strongest column-tone fundamental.



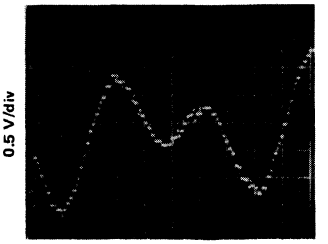
0.2 ms/div

FIGURE 1



0.2 ms/div

FIGURE 2



0.2 ms/div

FIGURE 3

distortion considerations

The following formula is used to calculate the total harmonic distortion of a single row or a single column:

$$THD = \left(\frac{\sqrt{V_{2f}^2 + V_{3f}^2 + V_{4f}^2 + V_{5f}^2 + \ldots + V_{nf}^2}}{V_{1f}} \right) \times 100\%$$

where V_{2f} is the second harmonic of the fundamental frequency V_{1f} waveform and so on. The dual-tone total harmonic distortion is:

$$THD = \left(\frac{\sqrt{V_{2R}^2 + V_{3R}^2 + \ldots + V_{nR}^2 + V_{2C}^2 + \ldots V_{nC}^2 \pm V_{IMD}^2}}{\sqrt{V_{FR}^2 + V_{FC}^2}} \right) \times 100\%$$

where V_{FR} and V_{FC} are the row and column fundamental frequency waveforms, and V_{2R} and V_{2C}, etc., are the corresponding harmonics.

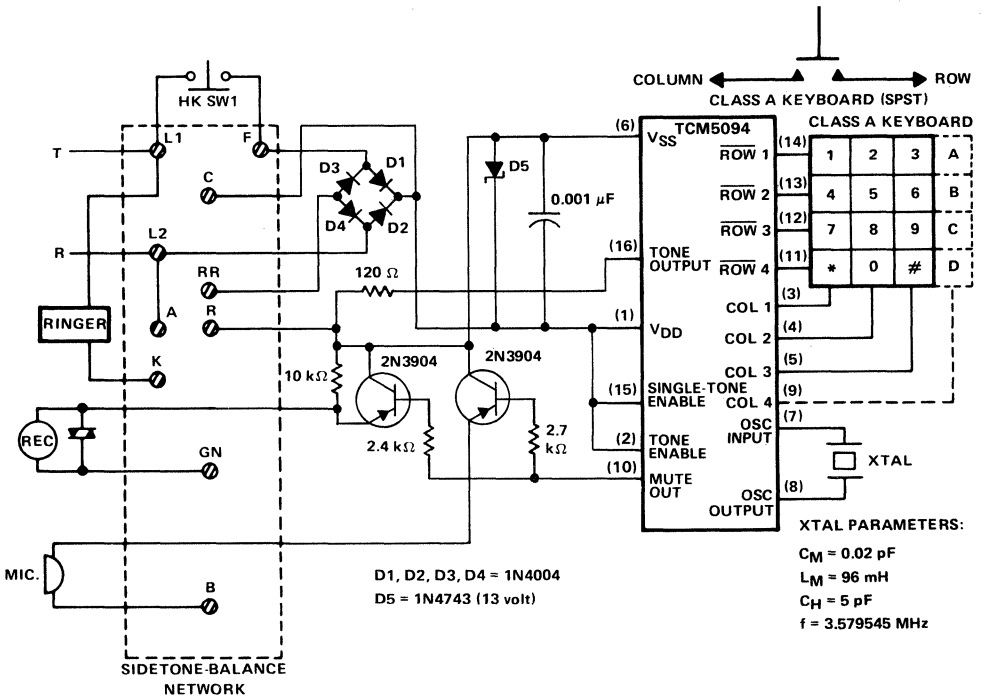
The total intermodulation distortion is:

$$V_{IMD}^2 = (V_{1R} + V_{1C})^2 + (V_{1R} - V_{1C})^2 + \ldots + (V_{nr} + V_{nC})^2 + (V_{nR} - V_{nC})^2$$

A relatively simple method of distortion measurement uses a spectrum analyzer to relate the harmonics to the fundamental frequency waveform. The tone encoder spectrum indicates the harmonics and intermodulation distortion at least 30 dB down relative to the column tone.

Another method for distortion measurement of the dual-tone waveform is to compare the total power in the fundamental frequencies with the total power in the various harmonics plus intermodulation on a signal analyzer. The encoders provide an output distortion of -20 dB maximum when operated between 3.5 volts and 10 volts. If operated between 3 volts and 3.5 volts, some clipping occurs at the output causing the distortion to exceed the -20 dB level.

APPLICATIONS INFORMATION



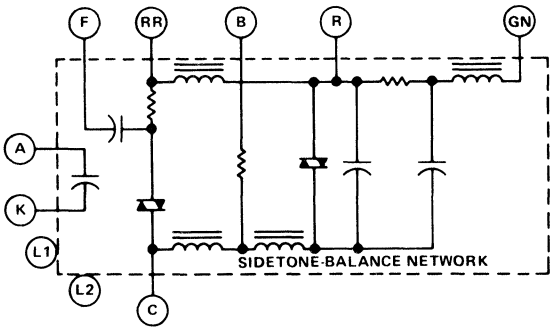


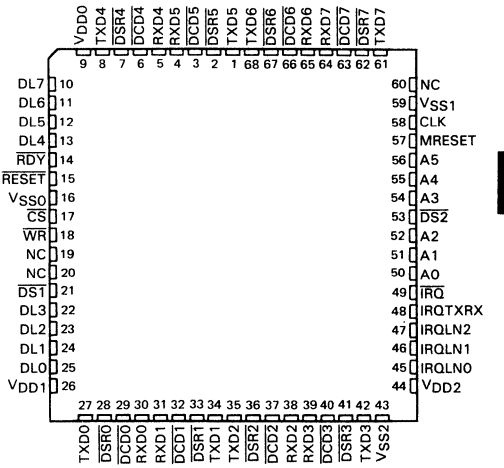
FIGURE 4. TYPICAL APPLICATION USING HYBRID COIL SIDETONE-BALANCE NETWORK, ELECTRONIC SWITCHING, AND LOW-COST (CLASS A) KEYBOARD

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

D2941, APRIL 1986—REVISED AUGUST 1987

- **Eight Independent Full-Duplex Serial Data Lines**
- **Programmable Baud Rates Individually Selectable for the Transmitter/Receiver of Each Line (50 to 19,200 Baud)**
- **Summary Registers Allow a Single Read to Detect a Data Set Change or to Determine the Cause of an Interrupt on Any Line**
- **Triple Buffers for Each Receiver**
- **Device Scanner Mechanism Reports Interrupt Requests Due to Transmitter/Receiver Interrupts**
- **Independently Programmable Lines for Interrupt-Driven Operation**
- **Modem Status Change Detection for Data Set Ready (DSR) and Data Carrier Detect (DCD) Signals**
- **Programmable Interrupts for Modem Status Changes**
- **Synchronizes Critical Read-Only Registers**
- **Replaces Eight Signetics 2661 UARTs**
- **Direct Second Source to DEC DC349 (78808)**

FN, HA, OR HB PACKAGE
(TOP VIEW—LID UP FOR HA OR HB)



NC—No internal connection

PACKAGE DESIGNATIONS

DESCRIPTION	TI	DEC
Cerquad Gull-Wing	HA	GA
Cerquad Straight	HB	FA
Plastic PLCC	FN	

description

The TCM78808 octal asynchronous receiver/transmitter is designed for the new generations of asynchronous serial communications and for microcomputer systems. The device performs the basic operations necessary for simultaneous reception and transmission of asynchronous messages on eight independent lines.

On-chip baud rate generation allows the designer to select and program any one of 16 rates between 50 and 19,200 baud. Baud rates are selectable for each receiver and transmitter. A built-in scanning mechanism provides an alternative to the customary polling of status registers.

The TCM78808 functions as a serial-to-parallel, parallel-to-serial converter/controller. It can be programmed by a microprocessor to provide different characteristics for each of its eight serial data lines (stop bits, parity, character length, baud rates, etc.). Each individual serial line functions as a one-line UART-type device.

An integral interrupt scanner checks for device interrupt conditions on the eight lines of the TCM78808. Its scanning algorithm is designed to give priority to receivers over transmitters. The scanner can also be programmed to check for interrupts due to changes in modem control signals (DSR and DCD).

The TCM78808 contains two types of programmable registers: line specific and summary. The six line-specific registers provide independent control of each of the eight serial lines. Two summary registers consolidate information about the current state of all eight lines and allow programs to service device interrupts quickly and efficiently.

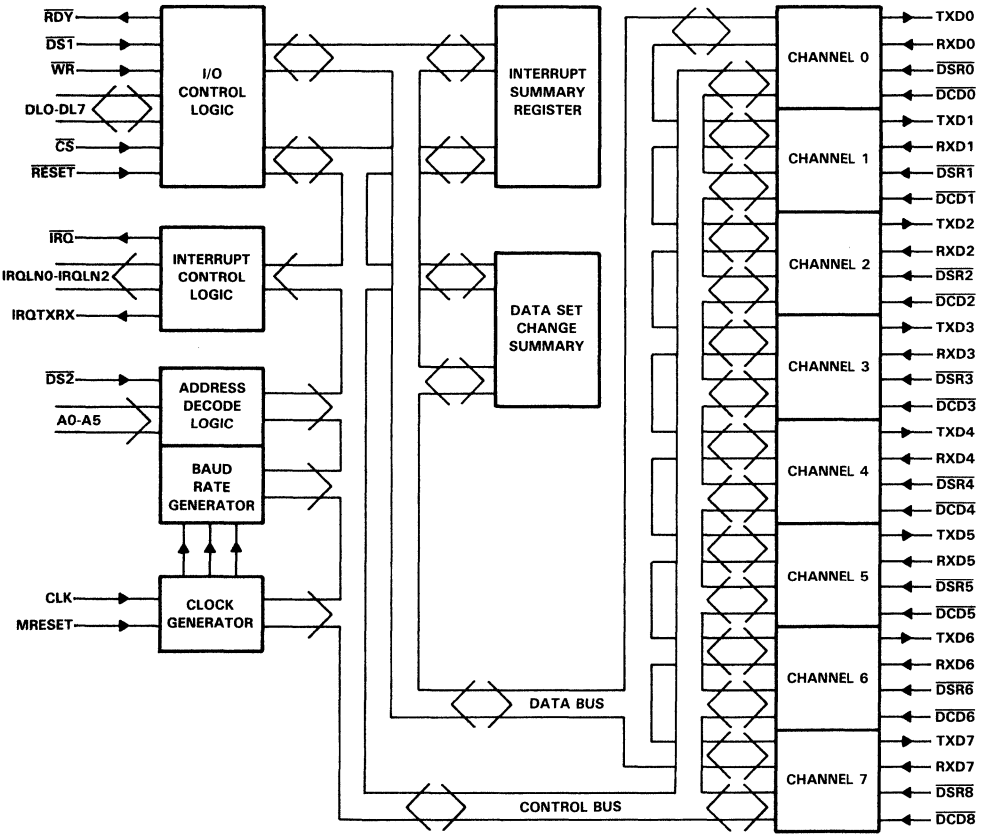
Each of the eight serial data lines in the TCM78808 has a set of line-specific registers for buffering data into and out of the line and for external control of line characteristics. The receiver buffer register comprises a character assembly register plus a two-entry, first-in first-out (FIFO) buffer. The transmitter holding register provides similar functions on the output side. Information about the current state of the given line is contained in the (read-only) status register. Two mode registers control communications parameters. One mode register handles stop bits, parity, character length, and modem control interrupt enable (MCIE). The second mode register sets the incoming and outgoing baud rates. The command register controls various other functions of the given line.

The TCM78808 has a pair of summary registers that provide the current status of all eight serial data lines. This makes it possible to determine that line status has changed with a single read operation. The (read-only) interrupt summary register indicates that an interrupt has occurred and contains both the line number that generated the interrupt and the corresponding direction of flow (transmitter or receiver). With both MCIEs set and receiver interrupt enabled, the interrupt summary register will respond to changes in $\overline{DSR}$ or $\overline{DCD}$. The data-set-change summary register monitors changes in $\overline{DSR}$ or $\overline{DCD}$ on a line-by-line basis and indicates whether a modem status change has occurred on each data line subsequent to the last time the corresponding bit was cleared.

The TCM78808 is characterized for operation from 0°C to 70°C.

SIGNAL	DESCRIPTION
A0 THRU A5	Address bits 0 through 5 select the internal registers in the TCM78808.
CLK	Clock input for timing
$\overline{CS}$	Chip Select. When low, activates the TCM78808 to receive and transmit data over data lines DL0 through DL7.
$\overline{DCD0}$ THRU $\overline{DCD7}$	Data-Set Carrier Detect inputs monitor data-set carrier detect signals from modems.
DL0 THRU DL7	Data Lines 0 through 7 receive and transmit the parallel data.
$\overline{DS1}$, $\overline{DS2}$	Data Strobes 1 and 2 receive timing information for data transfers. The $\overline{DS1}$ and $\overline{DS2}$ inputs must be connected together.
$\overline{DSR0}$ THRU $\overline{DSR7}$	Data Set Ready inputs monitor data-set-ready signals from modems.
$\overline{IRQ}$	Interrupt Request output requests a processor interrupt.
IRQLN0 THRU IRQLN2	Interrupt Request Line number outputs indicate the line number of the originating interrupt request.
IRQTXRX	Interrupt Request Transmit/Receive output indicates whether an interrupt request is for transmitting or receiving data.
MRESET	Manufacturing Reset. For manufacturing use
$\overline{RDY}$	Ready output indicates when the TCM78808 is ready to participate in data-transfer cycles.
$\overline{RESET}$	Reset input initializes the internal logic.
RXD0 THRU RXD7	Receive Data inputs accept asynchronous bit-serial data input streams.
TXD0 THRU TXD7	Transmit Data output provides asynchronous bit-serial data output streams.
V_{DD0} THRU V_{DD2}	5-V nominal power supply
V_{SS0} THRU V_{SS2}	Ground reference
$\overline{WR}$	Write input specifies direction of data transfer on the DL0 through DL7 lines.

functional block diagram



absolute maximum ratings over operating free-air temperature range

Supply voltage, V_{DD} (see Note 1) . . . . . 7 V
Input voltage, V_I . . . . . −5 V to 7 V
Input current, I_I . . . . . −30 mA to 5 mA
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: All voltage values are with respect to V_{SS1} and V_{SS2}.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range, V_{DD} = 5.25 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage		V_{DD} = 4.75 V, I_{OH} for DL0 thru DL7 = −1 mA, I_{OH} for all other (except $\overline{IRQ}$ and $\overline{RDY}$) = −2 mA	2.4		V
V_{OL}	Low-level output voltage		V_{DD} = 4.75 V, I_{OL} for DL0 thru DL7 = 5.5 mA, I_{OL} for all other = 3.5 mA		0.4	V
I_{IH}	High-level input current		V_I = 5.25 V		10	μA
I_{IL}	Low-level input current		V_I = 0		−10	μA
I_{OS}†	Short-circuit output current	DL0-DL7	V_{DD} = 5.25 V	−50	−180	mA
		All other outputs except $\overline{IRQ}$ and $\overline{RDY}$		−30	−110	
I_{OZH}‡	Off-state output current, high-level voltage applied		V_O = 2.4 V		−10	μA
I_{OZL}‡	Off-state output current, low-level voltage applied		V_O = 0.4 V		10	μA
I_{DD}	Supply current		V_{DD} = 5 V, T_A = 25°C		240	mA
C_i	Input capacitance				4	pF
C_{io}§	Input/output capacitance				5	pF

† Not more than one output should be short circuited at a time, and the duration of the short should not exceed 1 second.
‡ All 3-state output drivers are wired in an I/O configuration. The parameters include the driver and receiver input currents.
§ This parameter includes the capacitive loads of the output driver and the receiver input.

bus read and write timing requirements (see Figures 3 and 4)

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{w1}	Pulse duration, $\overline{DS1}$/$\overline{DS2}$ low	$\overline{WR}$ high	0.18	10	μs
t_{w2}	Pulse duration, $\overline{DS1}$/$\overline{DS2}$ high		450		ns
t_{w3}	Pulse duration, $\overline{DS1}$/$\overline{DS2}$ low	$\overline{WR}$ low	0.13	10	μs
t_{su1}	Setup time, A5-A0 valid before $\overline{DS1}$ and $\overline{DS2}$		30		ns
t_{su2}	Setup time, $\overline{WR}$ high before $\overline{DS1}$ and $\overline{DS2}$		30		ns
t_{su3}	Setup time, $\overline{CS}$ low before $\overline{DS1}$ and $\overline{DS2}$		30		ns
t_{su4}	Setup time, DL7-DL0 valid before $\overline{DS1}$ and $\overline{DS2}$		0		ns
t_{h1}	Hold time, A5-A0 valid after $\overline{DS1}$ and $\overline{DS2}$		10		ns
t_{h2}	Hold time, $\overline{WR}$ high or low after $\overline{DS1}$ and $\overline{DS2}$		10		ns
t_{h3}	Hold time, $\overline{CS}$ high after $\overline{DS1}$ and $\overline{DS2}$		10		ns
t_{h4}	Hold time, DL7-DL0 valid after $\overline{DS1}$ and $\overline{DS2}$ high		30		ns
t_v	Valid time, DL7-DL0 after $\overline{DS1}$ and $\overline{DS2}$ high		0		ns

write switching characteristics (see Figures 3 and 4)

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{en}	Enable time	C_L = 150 pF		165	ns
t_{dis}	Disable time	C_L = 50 pF		50	ns
		C_L = 100 pF		60	
		C_L = 150 pF		65	
t_{pd1}	Propagation delay time, from $\overline{CS}$ low to $\overline{RDY}$ low	C_L = 50 pF		90	ns
t_{pd2}†	Propagation delay time, from $\overline{CS}$ high to $\overline{RDY}$ high	C_L = 50 pF		210	ns
t_{pd3}	Propagation delay time, from $\overline{DS1}$ and $\overline{DS2}$ low to DL7-DL0 valid	C_L = 150 pF		165	ns
t_{pd4}†	Propagation delay time, from $\overline{DS1}$ and $\overline{DS2}$ low to $\overline{IRQ}$ high	C_L = 50 pF		635	ns

† Total rise time is dependent upon internal delay plus the pull-up delay introduced by the external resistor being used. Parameter t_{pd2} is calculated from $t_{pd2} = 500\ RC_L$, and t_{pd4} is calculated from $t_{pd4} = 75 + RC_L$ where R = value of the resistor that connects to C_L in Figure 1.

write timing requirements (see Figure 5)

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
f_{clock}	Clock frequency		4.9		MHz
t_{w4}	Pulse duration, clock high or low		95		ns
t_{w5}	Pulse duration, $\overline{RESET}$ low		1		μs
t_{w6}	Pulse duration, DCD7-DCD0 and $\overline{DSR7}$-$\overline{DSR0}$ high or low		1		μs
t_{w7}	Pulse duration, TXD7-TXD0 high or low		250		ns
t_{su5}	Setup time, $\overline{DS1}$ and $\overline{DS2}$ high before RESET low		900		ns
t_{h5}	Hold time, $\overline{DS1}$ and $\overline{DS2}$ high after RESET		1		μs
t_{d1}	Delay time, IRQLN2-IRQLN0 and IRQTXRX valid to $\overline{IRQ}$ low	C_L = 50 pF	100		ns
t_{d2}	Hold time, IRQLN2-IRQLN0 and IRQTXRX valid after $\overline{IRQ}$ high	C_L = 50 pF	100		μs

PARAMETER MEASUREMENT INFORMATION

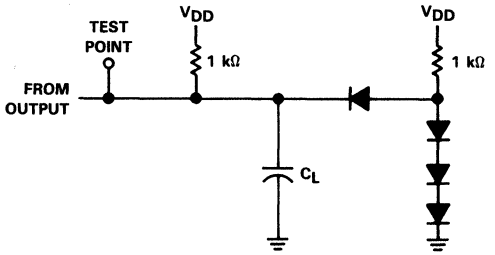


FIGURE 1. STANDARD OUTPUT LOAD CIRCUIT

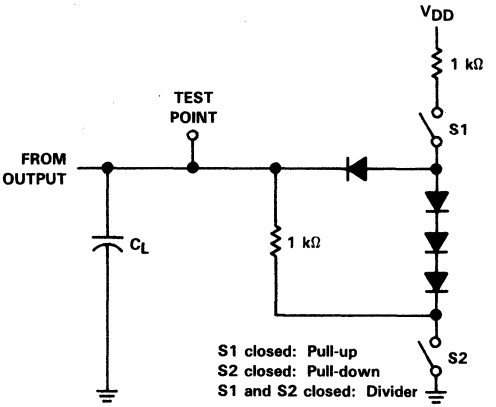


FIGURE 2. 3-STATE OUTPUT LOAD CIRCUIT

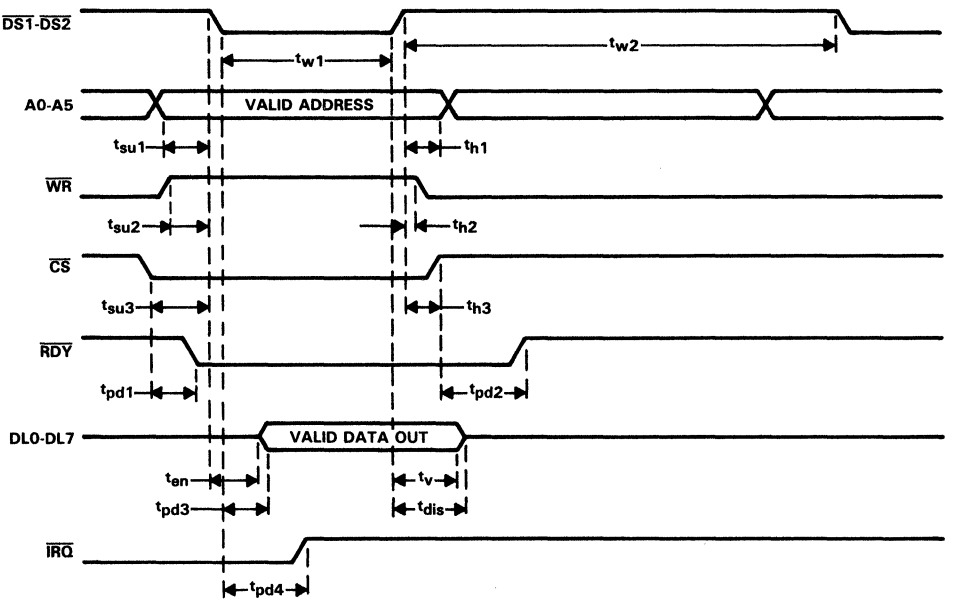


FIGURE 3. BUS READ CYCLE TIMING WAVEFORMS

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PARAMETER MEASUREMENT INFORMATION

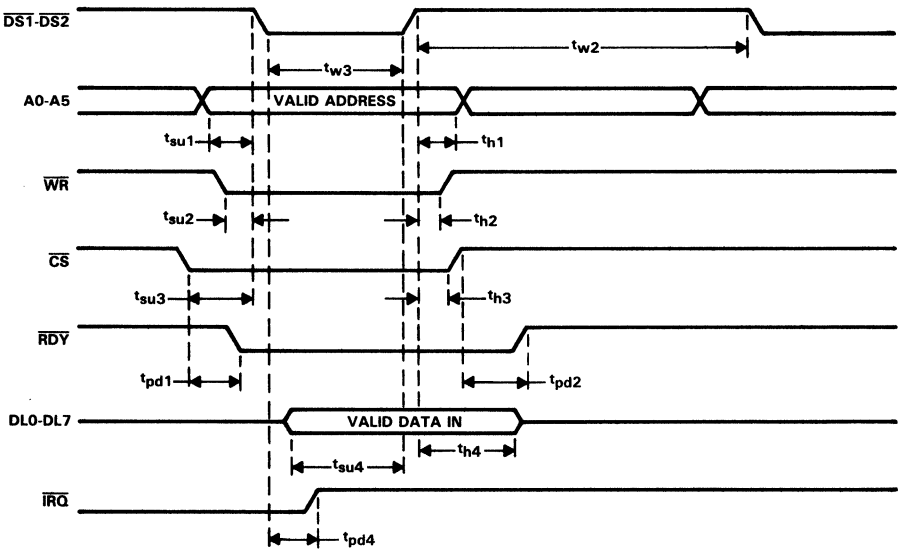


FIGURE 4. BUS WRITE CYCLE TIMING WAVEFORMS

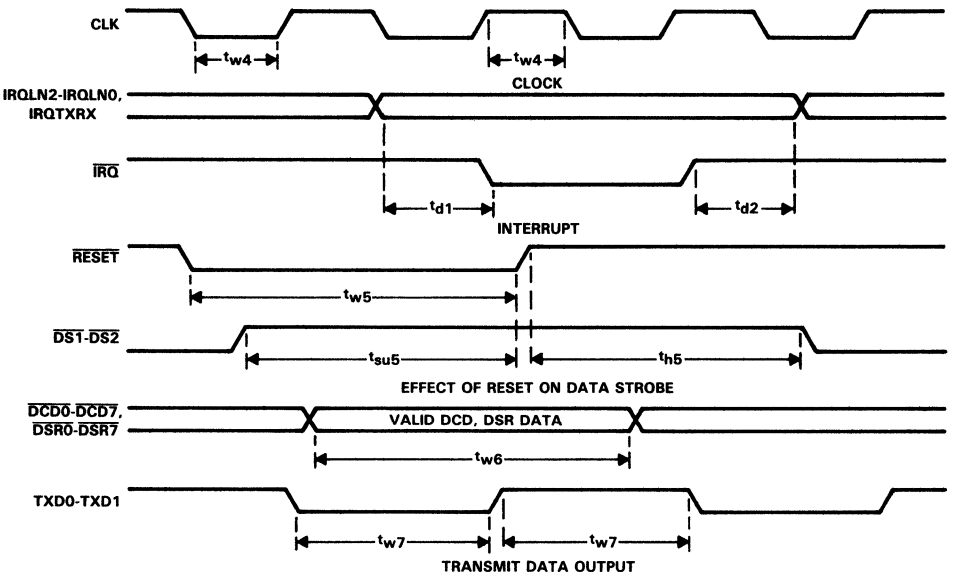
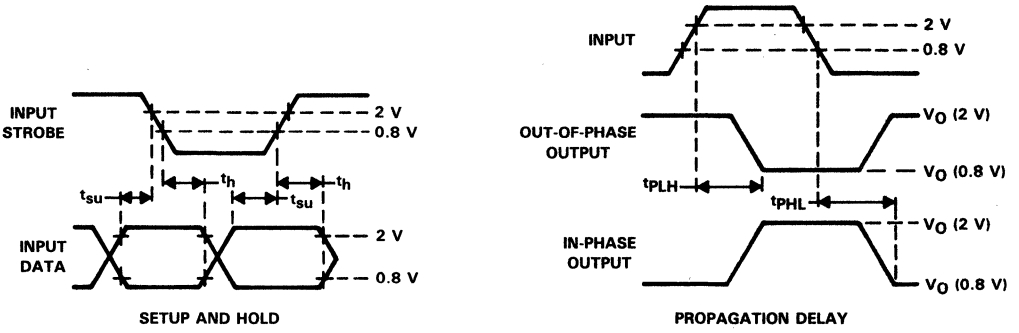


FIGURE 5. MISCELLANEOUS SIGNAL TIMING

PARAMETER MEASUREMENT INFORMATION



NOTE: $t_{pd} = t_{PLH}$ or t_{PHL}

FIGURE 6. VOLTAGE WAVEFORMS

PRINCIPLES OF OPERATION

electrical operation

data and address

data lines (DL7 through DL0)

These lines are used for the parallel transmission and reception of data between the CPU and the TCM78808. The receivers are activated by the data strobe ($\overline{DS1}$, $\overline{DS2}$) signal. The output drivers are active only when the chip select ($\overline{CS}$) signal is low (active), the data strobe ($\overline{DS1}$, $\overline{DS2}$) signal goes low (active), and the write ($\overline{WR}$) signal is high (inactive). The drivers will become inactive (high impedance) within 50 ns when one or more of the following occurs: the chip select ($\overline{CS}$) signal goes high, the data strobe ($\overline{DS1}$, $\overline{DS2}$) goes high, or the write ($\overline{WR}$) signal goes low.

address lines (A5 through A0)

These lines select which internal register is accessible through the data I/O lines (DL7 through DL0) when the data strobe ($\overline{DS1}$, $\overline{DS2}$) and chip select ($\overline{CS}$) signals are low. Table 1 lists the addresses corresponding to each register. The receiver buffer and transmitter holding register for each line have the same address. When the ($\overline{WR}$) signal is high, the address accesses the receiver buffer register. When $\overline{WR}$ is low, it accesses the transmitter holding register.

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PRINCIPLES OF OPERATION

TABLE 1. TCM78808 REGISTERS ADDRESS SELECTION

ADDRESS LINE†						READ/ WRITE	REGISTER
A5	A4	A3	A2	A1	A0		
L	L	L	L	L	L	Read	Line 0 Receiver Buffer
L	L	L	L	L	L	Write	Line 0 Transmitter Holding
L	L	L	L	L	H	Read	Line 0 Status
L	L	L	L	H	L	Read/Write	Line 0 Mode Registers 1 and 2
L	L	L	L	H	H	Read/Write	Line 0 Command
L	L	H	L	L	L	Read	Line 1 Receiver Buffer
L	L	H	L	L	L	Write	Line 1 Transmitter Holding
L	L	H	L	L	H	Read	Line 1 Status
L	L	H	L	H	L	Read/Write	Line 1 Mode Registers 1 and 2
L	L	H	L	H	H	Read/Write	Line 1 Command
L	H	L	L	L	L	Read	Line 2 Receiver Buffer
L	H	L	L	L	L	Write	Line 2 Transmitter Holding
L	H	L	L	L	H	Read	Line 2 Status
L	H	L	L	H	L	Read/Write	Line 2 Mode Registers 1 and 2
L	H	L	L	H	H	Read/Write	Line 2 Command
L	H	H	L	L	L	Read	Line 3 Receiver Buffer
L	H	H	L	L	L	Write	Line 3 Transmitter Holding
L	H	H	L	L	H	Read	Line 3 Status
L	H	H	L	H	L	Read/Write	Line 3 Mode Registers 1 and 2
L	H	H	L	H	H	Read/Write	Line 3 Command
H	L	L	L	L	L	Read	Line 4 Receiver Buffer
H	L	L	L	L	L	Write	Line 4 Transmitter Holding
H	L	L	L	L	H	Read	Line 4 Status
H	L	L	L	H	L	Read/Write	Line 4 Mode Registers 1 and 2
H	L	L	L	H	H	Read/Write	Line 4 Command
H	L	H	L	L	L	Read	Line 5 Receiver Buffer
H	L	H	L	L	L	Write	Line 5 Transmitter Holding
H	L	H	L	L	H	Read	Line 5 Status
H	L	H	L	H	L	Read/Write	Line 5 Mode Registers 1 and 2
H	L	H	L	H	H	Read/Write	Line 5 Command
H	H	L	L	L	L	Read	Line 6 Receiver Buffer
H	H	L	L	L	L	Write	Line 6 Transmitter Holding
H	H	L	L	L	H	Read	Line 6 Status
H	H	L	L	H	L	Read/Write	Line 6 Mode Registers 1 and 2
H	H	L	L	H	H	Read/Write	Line 6 Command
H	H	H	L	L	L	Read	Line 7 Receiver Buffer
H	H	H	L	L	L	Write	Line 7 Transmitter Holding
H	H	H	L	L	H	Read	Line 7 Status
H	H	H	L	H	L	Read/Write	Line 7 Mode Registers 1 and 2
H	H	H	L	H	H	Read/Write	Line 7 Command
X	X	X	H	L	L	Read	Interrupt Summary
X	X	X	H	L	H	Read	Data Set Change Summary

†X = Either L or H

PRINCIPLES OF OPERATION

bus transaction control

chip select ($\overline{CS}$)

This signal, when low, permits data transfers through the DL7 through DL0 lines to or from the internal registers. Data transfer is controlled by the data strobe ($\overline{DS1}$, $\overline{DS2}$) signal and the write ($\overline{WR}$) signal.

data strobe ($\overline{DS1}$, $\overline{DS2}$)

The data strobe inputs ($\overline{DS1}$ and $\overline{DS2}$) must be connected together. This input receives timing information for data transfers. During a write cycle, the CPU activates the data strobe signal when valid output data is available and deactivates the data strobe signal before the data is removed. During a read cycle, the CPU activates the data strobe signal, and the TCM78808 transfers the valid data.

When the data strobe signal is high, the DL7 through DL0 lines are in a high-impedance state.

write ($\overline{WR}$)

The write ($\overline{WR}$) signal specifies the direction of data transfer on the DL7 through DL0 pins by controlling the direction of their transceivers. If the $\overline{WR}$ signal is low during a data transfer (with the $\overline{CS}$, $\overline{DS1}$, and $\overline{DS2}$ signals also low), the TCM78808 receives data from DL7 through DL0. If the $\overline{WR}$ signal is high during a write data transfer, the TCM78808 drives data onto the DL7 through DL0 lines.

interrupt request ($\overline{IRQ}$)

The $\overline{IRQ}$ output is an active-low, open-drain output. The integral interrupt scanner drives the $\overline{IRQ}$ signal low when it has detected an interrupt condition on one of the eight serial data lines.

interrupt request transmit/receive (IRQTxRx)

This signal indicates when the interrupt scanner stops and activates $\overline{IRQ}$ because of a transmitter interrupt condition (IRQTxRx = H) or because of a receiver interrupt condition (IRQTxRx = L). The signal is valid only while the $\overline{IRQ}$ signal is low. The state of IRQTxRx signal also appears as bit 0 of the interrupt summary register.

interrupt request line number (IRQLN2 through IRQLN0)

These lines indicate the line number at which the TCM78808 interrupt scanner stopped and activated the interrupt request ($\overline{IRQ}$) signal. The number on these lines is valid only while the $\overline{IRQ}$ signal is low. Line IRQLN2 is the high-order bit, and the IRQLN0 line is the low-order bit.

The state of these signals also appears as bits in the interrupt summary register: IRQLN2 as bit 3, IRQLN1 as bit 2, and IRQLN0 as bit 1. Table 2 shows the line numbers corresponding to settings of IRQLN2 through IRQLN0.

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TABLE 2. TCM78808 INTERRUPT REQUEST LINE INDICATIONS

IRQLN2	IRQLN1	IRQLN0	INTERRUPT REQUEST LINE NUMBER
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

serial data

transmit data (TXD7 through TXD0)

These outputs transmit the asynchronous bit-serial data streams. They remain at a high level when no data is being transmitted and at a low level when the TxBRK bit in the command register of the associated line is set.

receive data (RXD7 through RXD0)

These lines accept asynchronous bit-serial data streams. The input signals must remain at the high level for at least one-half bit time before a high-to-low transition is recognized. A high-to-low transition is required to signal the beginning of a start bit and initiate data reception.

modem signals

data set ready ($\overline{DSR7}$ through $\overline{DSR0}$)

These eight inputs, one for each serial data line on the TCM78808, are typically connected via intervening level converters to the data set ready outputs of modems. A TTL low at a $\overline{DSR}$ pin causes the $\overline{DSR}$ bit (bit 7) in the status register of the corresponding line to be activated. A TTL high at a $\overline{DSR}$ pin causes the $\overline{DSR}$ bit in the status register of the corresponding line to be inactive. A change of this input from high to low or low to high causes the activation of the data set change (DSCHNG) bit that corresponds to this line in the data set change summary register. Changes from one level to the other and back again that occur within 1 μs may not be detected.

carrier detect ($\overline{DCD7}$ through $\overline{DCD0}$)

These eight inputs, one for each serial data line of the TCM78808, are typically connected through intervening level converters to the received-line-signal-detect (also called carrier-detect) outputs of modems. A TTL low at a $\overline{DCD}$ input causes the $\overline{DCD}$ bit of the corresponding line status register to be deactivated. A change of this input from high to low or low to high causes the activation of the data-set-change (DSCHNG) bit that corresponds to this line in the data-set-change summary register. Changes from one level to the other and back again that occur within 1 μs may not be detected.

PRINCIPLES OF OPERATION

general control signals

ready ($\overline{RDY}$)

The $\overline{RDY}$ output is an open-drain output. Upon detecting a negative transition of $\overline{CS}$, the TCM78808 activates the $\overline{RDY}$ signal to indicate readiness to take part in data transfer cycles. The $\overline{RDY}$ signal deactivates on the trailing edge of $\overline{CS}$.

reset ($\overline{RESET}$)

When the $\overline{RESET}$ input goes low, the TxD7 through TxD0 lines are low, and all internal status bits listed in the Architecture Summary paragraph are cleared.

manufacturing reset (MRESET)

This signal is for manufacturing use only. The input should be connected to ground for normal operation.

clock signals

clock input (CLK)

All baud rates and internal clocks are derived from this input. Normal operating frequency is 4.9152 MHz ±0.1%, and duty cycle is 50 ±5%.

architecture summary

line-specific registers

Each of the eight serial data lines has a set of registers for buffering data into and out of the line and for external control of the line characteristics. These registers are selected for access by setting the appropriate address on lines A5 through A0. Lines A5 through A3 select one of the eight data lines . Lines A2 through A0 select the specific register for that line. Refer to Table 1 for the register address assignments.

receiver buffer register

Each line receiver consists of a character-assembly register and a two-entry FIFO that is the receiver buffer register. When the RxEN bit in a line command register is set, received characters are moved automatically into the line receiver buffer as soon as they have been deserialized from the associated communications line. When there are characters in this FIFO, the RxRDY bit is set in the status register for the line.

The activation of the RxRDY signal for a line that already has the RxIE bit of its command register set causes the interrupt scanner logic to stop and generate an interrupt condition (the $\overline{IRQ}$ signal is low). When the receiver buffer is read, the interrupt condition is cleared (the $\overline{IRQ}$ signal is high), and the interrupt scanner resumes operation.

If there is another entry in a line FIFO, the RxRDY bit remains active. When the interrupt scanner reaches this line again, the activation of RxRDY causes the scanner to halt and generate another interrupt ($\overline{IRQ}$ goes low).

The $\overline{RESET}$ signal clears the RxEN bit and initializes the receiver logic. The RxRDY flag is cleared, and the receiver buffer register outputs become undefined. Any data in the FIFO at that time is lost.

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PRINCIPLES OF OPERATION

transmitter holding register

Each line has a transmitter holding register that can be written to. When the TxEN bit in the line command register is set and the serialization logic becomes idle, characters are automatically moved from the output of this register into the transmitter serialization logic.

When this register is empty, the TxRDY bit in the line status register is set. If the transmitter interrupt enable (TxIE) bit in the line command register is also set, the interrupt scanner logic halts and generates an interrupt condition. If a character is then loaded into the register, the interrupt is cleared, and the scanner resumes operation.

The $\overline{\text{RESET}}$ signal also initializes the transmitter logic. The TxRDY flag is cleared, and the transmitter holding register contents are lost. The transmitter enable (TxEN) bit in the line command register is also cleared by $\overline{\text{RESET}}$. Software clearing of TxEN alone produces results different from the full $\overline{\text{RESET}}$ in that the transmitter holding register contents are not lost. They are transmitted when TxEN is set again.

status register

Each line has a read-only status register that provides information about the current state of the given line. This register indicates the readiness of a line for transmission or reception of data and flags error conditions in its bit fields. Figure 7 shows the format of the status register. Table 3 lists the flag bits in each register.

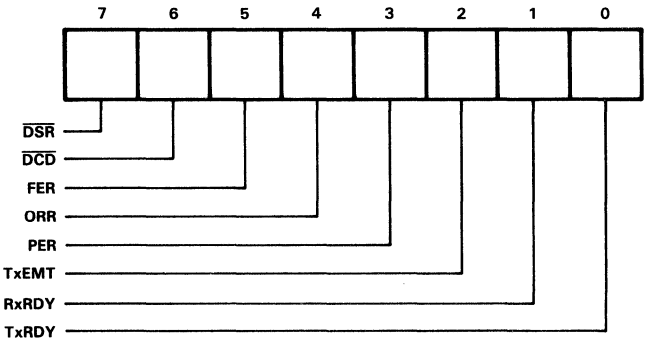


FIGURE 7. TCM78808 STATUS REGISTERS (LINE 0 THROUGH 6) FORMAT

TABLE 3. TCM78808 STATUS REGISTERS (LINES 0 THROUGH 7) DESCRIPTION

BIT	DESCRIPTION
7	$\overline{DSR}$ (Data Set Ready). This bit is the inverted state of the $\overline{DSR}$ line.
6	DCD (Data Set Carrier Detect). This bit is the inverted state of the DCD line.
5	FER (Frame Error). Set when the received character currently displayed in the receiver buffer register was not framed by a stop bit. Only the first stop bit is checked to determine that a framing error exists. Subsequent reading of the receiver buffer register that indicates all zeros (including the parity bit, if any) can be interpreted as a Break condition. This bit is cleared by clearing RxEN (bit 2) of the command register, by $\overline{RESET}$, or by setting the reset error RERR (bit 4) of the command register.
4	ORR (Overrun error). Set when the character in the receiver buffer was not read before another character was received. Cleared by clearing RxEN (bit 2) of the command register, by $\overline{RESET}$, or by setting reset error RERR (bit 4) of the command register.
3	PER (Parity Error). If parity is enabled and this bit is set, the received character in the receiver buffer register has an incorrect parity bit. This bit is cleared by clearing RxEN (bit 2) of the command register, by $\overline{RESET}$, by setting reset error RERR (bit 2) of the command register, or by reading the current character in the receiver buffer register.
2	TxEMT (Transmitter Empty). Set when the transmitter serialization logic for the associated line has completed transmission of a character, and no new character has been loaded into the transmission holding register. Cleared by loading the transmitter holding register, by clearing TxEN(0) of the command register, or by $\overline{RESET}$.
1	RxRDY (Receiver Buffer Ready). When set, a character has been loaded into the FIFO buffer from the deserialization logic. Cleared by reading the receiver buffer register, by clearing RxEN (bit 2) in the command register, or by $\overline{RESET}$.
0	TxRDY (Transmitter Holding Register Ready). When set, this bit indicates that the transmitter holding register is empty. Cleared when the program has loaded a character into the transmitter holding register, when the transmitter for this line is disabled by clearing TxEN (bit 0) in the command register, or $\overline{RESET}$. This bit is initially set when the transmitter logic is enabled by the setting of the TxEN (bit 0) and the transmitter holding register is empty. This bit is not set when the automatic echo or remote loopback modes are programmed. Data can be overwritten if a consecutive write is performed while TxRDY is cleared.

mode registers 1 and 2

These read/write registers control the attributes (including parity, character length, and line speed) of the communications line.

Each of the eight communications lines has two of these registers, both accessed by the same address on A5 through A0. Successive access operations (either read or write, in any combination) alternate between the two registers at that address by use of an internal pointer. The first operation addresses mode register 1. The pointer is reset to point to mode register 1 by $\overline{RESET}$ or by a read of the command register for this line. These registers should not be accessed by bit-oriented instructions that do read/modify/write cycles such as the PDP-11 BIS, BIC, and BIT instructions.

Figure 8 shows the format of mode registers 1, and Table 4 describes the function of the register information.

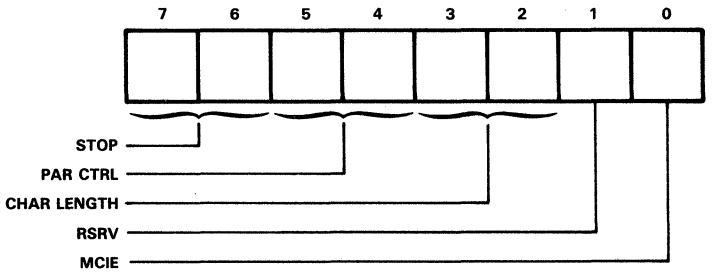


FIGURE 8. TCM78808 MODE REGISTERS 1 (LINE 0-6) FORMAT

TABLE 4. TCM78808 MODE REGISTERS 1 (LINES 0 THROUGH 6) DESCRIPTION

BIT	DESCRIPTION
7,6	STOP. These bits determine the number of stop bits that are appended to the transmitted characters as follows. These bits are cleared by $\overline{\text{RESET}}$. Bit 7 / Bit 6 / Stop Bits L / L / Invalid L / H / 1.0 H / L / 1.5 H / H / 2.0
5,4	PAR CTRL (Parity control). These bits determine parity as follows and are cleared by $\overline{\text{RESET}}$. (X = either H or L) Bit 5 / Bit 4 / Parity Type H / H / Even L / H / Odd X / L / Disabled
3,2	CHAR LENGTH (Character length). These bits determine the length (excluding start bit, parity, and stop bits) of the characters received and sent. Received characters of less than 8 bits are "right aligned" in the receiver buffer with unused high-order bits equal to zero. Parity bits are not shown in the receiver buffer. The character length bits are cleared by $\overline{\text{RESET}}$. The character length bits are defined as follows: Bit 3 / Bit 2 / Bit Length L / L / 5 L / H / 6 H / L / 7 H / H / 8
1	RSRV. Reserved and cleared by $\overline{\text{RESET}}$.
0	MCIE (Modem control interrupt enable). When set and RxIE (bit 5) of the command register is set, the modem control interrupts are enabled. Refer to the interrupt Scanner and Interrupt Handling information. Cleared by $\overline{\text{RESET}}$.

Figure 9 shows the format of mode registers 2, and Table 5 indicates the baud rate selections of the register. Bits 7 through 4 of mode register 2 control the transmitter baud rate, and bits 3 through 0 control the receiver baud rate. These registers are cleared by $\overline{\text{RESET}}$.

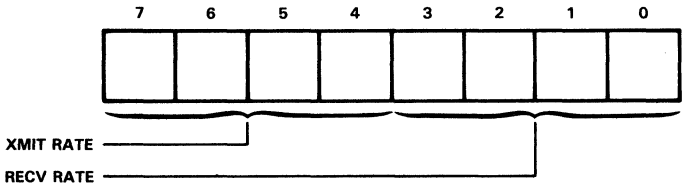


FIGURE 9. TCM78808 MODE REGISTERS 2 (LINE 0 THROUGH 6) FORMAT

PRINCIPLES OF OPERATION

TABLE 5. TCM78808 MODE REGISTERS 2 (LINES 0 THROUGH 6) DESCRIPTION

BIT	DESCRIPTION
7-0	XMIT RATE/RECV RATE (Transmitter/Receiver Rate). Selects the baud rate of the transmitter (bits 7 through 4) and receiver (bits 3 through 0) as follows:

Transmitter Bits				Receiver Bits				Nominal	Actual	Error†
7	6	5	4	3	2	1	0	Rate	Rate	(percent)
L	L	L	L	L	L	L	L	50	same	—
L	L	L	H	L	L	L	H	75	same	—
L	L	H	L	L	L	H	L	110	109.09	0.826
L	L	H	H	L	L	H	H	134.5	133.33	0.867
L	H	L	L	L	H	L	L	150	same	—
L	H	L	H	L	H	L	H	300	same	—
L	H	H	L	L	H	H	L	600	same	—
L	H	H	H	L	H	H	H	1200	same	—
H	L	L	L	H	L	L	L	1800	1745.45	3.03
H	L	L	H	H	L	L	H	2000	2021.05	1.05
H	L	H	L	H	L	H	L	2400	same	—
H	L	H	H	H	L	H	H	3600	3490.91	3.03
H	H	L	L	H	H	L	L	4800	same	—
H	H	L	H	H	H	L	H	7200	6981.81	3.03
H	H	H	L	H	H	H	L	9600	same	—
H	H	H	H	H	H	H	H	19200	same	—

† The frequency of the clock input (CLK) is 4.9152 MHz. The clock input may vary by 0.1%. This variance results in an error that must be added to the error listed in the error column.

command register

These read/write registers control various functions on the selected line. Figure 10 shows the format of the command registers, and Table 6 describes the function of the register information.

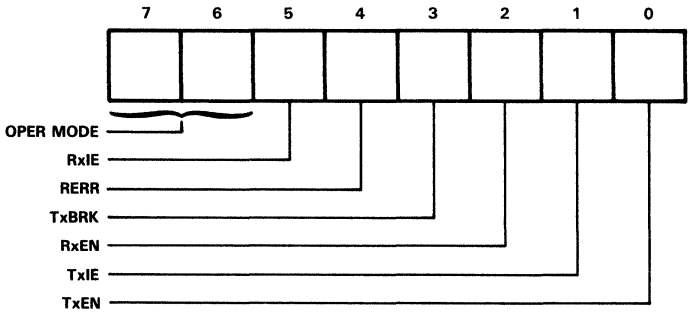


FIGURE 10. TCM78808 COMMAND REGISTERS (LINE 0 THROUGH 6) FORMAT

PRINCIPLES OF OPERATION

TABLE 6. TCM78808 COMMAND REGISTERS (LINES 0 THROUGH 7) DESCRIPTION

BIT	DESCRIPTION
7,6	OPER MODE (Operation Mode). These bits control the operating mode of the channel as follows. These bits are cleared by $\overline{\text{RESET}}$. Bit 7 / Bit 6 / Operating Mode L / L / Normal operation L / H / Automatic echo H / L / Local loopback H / H / Remote loopback
5	RxIE (Receiver Interrupt Enable). When set, the RxRDY flag (bit 1) of the status register for this line will generate an interrupt.
4	RERR (Reset Error). When set, this bit clears the framing error, overrun error, and parity error of the status register associated with this line. This bit is cleared by $\overline{\text{RESET}}$. It is not self-clearing.
3	TxBRK (Transmit Break). When set, this bit forces the appropriate TxD7-TxD0 line to the spacing state at the conclusion of the character presently being transmitted. When the program clears this bit, normal operation is restored, and any character pending in the transmitter holding register is moved into the serialization logic and transmitted. The minimum break length obtainable is twice the character length plus 1 bit time. The maximum break length depends on the amount of time between the program setting and clearing this bit, but is an integral number of bit times. This bit is cleared by $\overline{\text{RESET}}$.
2	RxEN (Receiver Enable). When set, this bit enables the receiver logic. When cleared, it stops the assembling of the received character, clears all receiver error bits and the RxRDY (bit 1) of the status register, clears any receiver interrupt conditions associated with this line, and initializes all receiver logic. This bit is cleared by $\overline{\text{RESET}}$.
1	TxIE (Transmit Interrupt Enable). When set, the state of the associated TxRDY flag (bit 0) of the status register is made available to the interrupt scanner logic. When the interrupt scanner logic scans this line, it determines if the TxRDY flag is set and, if so, generates an interrupt.
0	TxEN (Transmitter Enable). When set, this bit enables the transmitter logic. When cleared, it inhibits the serialization of the characters that follow, but the serialization of the current character is completed. It also clears the TxRDY flag (bit 0) of the status register, clears any transmitter interrupt conditions associated with the transmitter holding register, and initializes all transmitter logic except that associated with the transmitter holding register. The character in the transmitter holding register is retained so that XON/XOFF situations can be properly processed. This bit is cleared by $\overline{\text{RESET}}$.

Bits 5 through 0 enable the line receiver and transmitter, enable handling of interrupts, initiate the transmission of break characters, and reset error bits for the line. Refer to the "Interrupt Scanner and Interrupt Handling" paragraphs for detailed interrupt information. Bits 7 and 6 control the operating mode of the line. The four modes that can be set are normal operation, automatic echo, local loopback, and remote loopback.

normal operation

The serial data received is assembled in the receiver logic and transferred in parallel to the receiver buffer register. The RxEN bit must be set. Data to be transmitted is loaded in parallel into the transmitter holding register, then automatically transferred into the transmitter logic and serialized for transmission. The TxEN bit must be set.

automatic echo

The serial data received is assembled into parallel form in the receiver logic (the RxEN bit must be set) and transferred to the receiver buffer register. Arriving serial data is also routed to the line's TxDn pin for serial output. TxEN is ignored, and the transmitter logic is disabled. TxRDY flags and TxEMT indications are cleared. No transmitter interrupts are generated.

local loopback

The serial data from the RxDn input is ignored, and the receiver serial input receives data from the transmitter serial output. That data is assembled into parallel form in the receiver logic (the RxEN bit must be set) and transferred to the receiver buffer register where it can be read by the program. Data to be transmitted to the receiver is loaded in parallel form into the transmitter holding register from which it is automatically moved into the transmitter logic and serialized for transmission. The TxEN bit must be set. The transmission goes only to the receiver serial input; the TxDn output is held high. As in normal operation, transmission and reception baud rates are controlled by the transmitter speed and receiver speed entries in mode register 2.

remote loopback

The serial data received on the RxDn line is returned to the TxDn line without further action. No data is received or transmitted. The RxRDY, TxRDY, and TxEMT flags are disabled. The TxEN and RxEN bits of the command register are held cleared, causing the transmitter and receiver logic to be disabled.

summary registers

The TCM78808 contains two registers that summarize the current status of all eight serial data lines, making it possible to determine that a line status has changed with a a single read operation. These registers are selected for access by setting the appropriate address on inputs A2 through A0. Because the registers are shared by eight serial lines, the line-selection bits A5 through A3 are ignored when these registers are accessed. Refer to "Interrupt Scanner and Interrupt Handling" for detailed interrupt information.

interrupt summary register

This read-only register indicates that a transmitter or receiver interrupt condition has occurred and indicates the line number that generated the interrupt. Figure 11 shows the format of the interrupt summary register, and Table 7 describes register information.

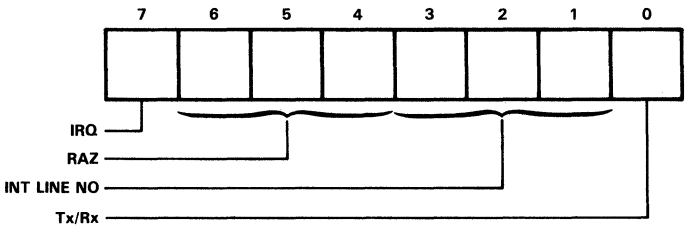


FIGURE 11. TCM78808 INTERRUPT SUMMARY REGISTER FORMAT

PRINCIPLES OF OPERATION

TABLE 7. TCM78808 INTERRUPT SUMMARY REGISTER DESCRIPTION

BIT	DESCRIPTION
7	IRQ (Interrupt Request). When set, this bit indicates that the interrupt scanner has found an interrupting condition among the eight serial lines of the TCM78808. These conditions also result in activating the IRQ signal.
6,5,4	RAZ (Read as Zero). Not used
3,2,1†	INT LINE NO (Interrupting Line Number). These bits indicate the line number upon which an interrupting condition was found. These bits correspond to the IRQLN2-IRQLNO signals: bit 3 = IRQLN2, bit 2 = IRQLN1, and bit 1 = IRQLNO. See Table 2.
0†	Tx/Rx (Transmit/Receive). This bit indicates whether the interrupting condition was caused by a transmitter (Tx/Rx = 1) or a receiver (Tx/Rx = 0). This bit corresponds to the IRQTxRx signal of the TCM78808 and is set when IRQTxRx is set.

† Bits 3-0 above represent the outputs of a free-running counter and are valid only when bit 7 is set.

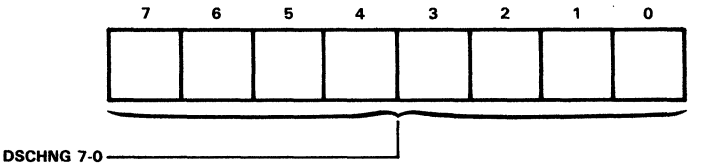


FIGURE 12. TCM78808 DATA SET CHANGE SUMMARY REGISTER FORM

When the MCIE bit in a line mode register 1 is set and RxIE is also set, the modem control interrupts are enabled for that line. If DSCHNG for that line is then set, the interrupt scanner will halt and generate an interrupt. The data set change summary register bits are cleared by writing a high into the bit position. A program that uses this register should read and save a copy of its contents. The copy can then be written back to the register to clear the bits that were set. The system interrupts should be disabled, and writeback should directly follow the read operation.

The $\overline{\text{RESET}}$ signal disables and initializes the data set change logic. When the $\overline{\text{RESET}}$ signal is high, future changes in $\overline{\text{DSR}}$ and $\overline{\text{DCD}}$ are reported as they occur.

interrupt scanner and interrupt handling

The interrupt scanner is a 4-bit counter that sequentially checks lines 0 through 7 for a receiver interrupt (counter positions 0 through 7) and then checks the lines in the same order for a transmitter interrupt (counter positions 8 through 15). If the scanner detects an interrupt condition, it stops, and the $\overline{\text{IRQ}}$ signal goes low. An interrupt must be serviced by software, or no other interrupt request can be posted.

The scanner determines that a line has a receiver interrupt if the line receiver buffer is ready and receiver interrupts are enabled for that line (RxRDY and RxIE = H) or if either of the line modem status signals has changed state and both receiver and modem control interrupts are enabled for that line (DSCHNG, RxIE, and MCIE all high).

The scanner determines that a line has a transmitter interrupt if the line's transmitter holding the register is empty and transmitter interrupts are enabled for that line (TxRDY and TxIE both high).

PRINCIPLES OF OPERATION

When the scanner detects an interrupt, it reports the line number on the IRQ2-IRQ0 lines. The IRQTxRx signal is high for a transmitter interrupt and is low for a receiver interrupt. The appropriate bits are also updated in the interrupt summary register. The $\overline{IRQ}$ line goes high, and the scanner is restarted for each of the following three types of interrupt conditions:

1. Reading the receiver buffer or resetting the RxIE bit of the interrupting line for the first type of receiver interrupt previously described.
2. Resetting the MCIE, RxIE, or DSCHNG bit of the interrupting line for the second type of receiver interrupt previously described.
3. Loading the transmitter holding register or resetting the TxIE bit of the interrupting line for transmitter interrupts.

If the scanner was originally stopped by a receiver interrupt condition, the scanner resumes sequential operation from where it stopped, thus providing receivers with equal priority. If the scanner was stopped by a transmitter condition, the scanner restarts from position 0 (line receiver), thus giving receivers priority over transmitters.

edge-triggered and level-triggered interrupt systems

If the interrupt system of the TCM78808 is used only for generating interrupts for the RxRDY and/or TxRDY flags, the $\overline{IRQ}$ line can be connected to a processor having either edge-triggered or level-triggered interrupt capability. If the modem control interrupts are being used (MCIE in mode register 1 = 1), the $\overline{IRQ}$ line can be connected only to a processor that uses level-triggered interrupts.

modem handling

The TxEMT (transmitter empty) bit of the status register is typically used to indicate when a program can disable the transmission medium, as when deactivating the request-to-send line of a modem. A typical program will load the last character for transmission and then monitor the TxEMT bit of the status register.

The setting of the TxEMT bit to indicate that transmission is complete may occur a substantial time after the loading of the last character. After the last character is loaded, one character is in the transmitter holding register, and one character is in the serialization logic. Therefore, it will be two character times before the transmission process is completed. Waiting for the TxRDY signal to be set before monitoring the TxEMT status shortens this by one character time because the TxRDY status bit indicates that there are no characters in the transmitter holding register. The times involved are calculated by taking the reciprocal of the baud rate being used, multiplying by the number of bits per character [a start bit - 5, 6, 7, or 8 data bits (plus parity bit if enabled) and 1, 1.5, or 2 stop bits], and multiplying by either two characters or one depending on when TxEMT monitoring begins.

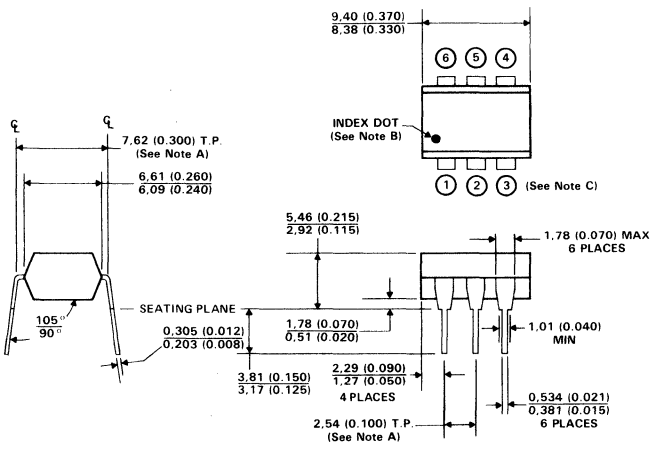
D2906, OCTOBER 1985—REVISED MARCH 1988

COMPATIBLE WITH STANDARD TTL INTEGRATED CIRCUITS

- **Gallium Arsenide Diode Infrared Source Optically Coupled to a Silicon N-P-N Phototransistor**
- **High Direct-Current Transfer Ratio**
- **High-Voltage Electrical Isolation . . . 2.5 kV rms (3.535 kV peak)**
- **Plastic Dual-In-Line Package**
- **High-Speed Switching: t_r = 2 μs Typ, t_f = 2 μs Typ**
- **UL Recognized — File #E65085**
- **Primarily Used with Telephone Ring Detector TCM1520A and Tone Drivers TCM1501B, TCM1506B, TCM1512B, TCM1531, TCM1532, TCM1536, and TCM1539**

mechanical data

The package consists of a gallium arsenide infrared-emitting diode and an n-p-n silicon phototransistor mounted on a 6-pin lead frame encapsulated within an electrically nonconductive plastic compound. The case will withstand soldering temperature with no deformation and device performance characteristics remain stable when operated in high-humidity conditions. Unit weight is approximately 0.52 grams.



NOTES: A. Leads are within 0,13 mm (0.005 inch) radius of true position (T.P.) with maximum material condition and unit installed.
B. Pin 1 identified by index dot.
C. Terminal connections:

1. Anode	Infrared-emitting diode
2. Cathode	
3. No internal connection	
4. Emitter	Phototransistor
5. Collector	
6. Base	

FALLS WITHIN JEDEC MO-001AM DIMENSIONS

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

CP-7

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Input-to-output voltage ..... ±2.5 kV rms (±3.535 kV peak)
Collector-base voltage ..... 70 V
Collector-emitter voltage (see Note 1) ..... 30 V
Emitter-collector voltage ..... 7 V
Emitter-base voltage ..... 7 V
Input-diode reverse voltage ..... 3 V
Input-diode continuous forward current at (or below) 25°C free-air temperature (see Note 2) ..... 100 mA
Continuous power dissipation at (or below) 25°C free-air temperature
Infrared-emitting diode (see Note 3) ..... 150 mW
Phototransistor (see Note 4) ..... 150 mW
Total, infrared-emitting diode plus phototransistor (see Note 5) ..... 250 mW
Storage temperature range ..... −55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTES: 1. This value applies when the base-emitter diode is open-circuited.
2. Derate linearly to 100°C free-air temperature at the rate of 1.33 mA/°C.
3. Derate linearly to 100°C free-air temperature at the rate of 2 mW/°C.
4. Derate linearly to 100°C free-air temperature at the rate of 2 mW/°C.
5. Derate linearly to 100°C free-air temperature at the rate of 3.33 mW/°C.

electrical characteristics at 25°C free-air temperature

PARAMETER			TEST CONDITIONS			MIN	TYP	MAX	UNIT
$V_{(BR)CBO}$	Collector-base breakdown voltage		I_C = 10 μA,	I_E = 0,	I_F = 0	70			V
$V_{(BR)CEO}$	Collector-emitter breakdown voltage		I_C = 1 mA,	I_B = 0,	I_F = 0	30			V
$V_{(BR)EBO}$	Emitter-base breakdown voltage		I_E = 10 μA,	I_C = 0,	I_F = 0	7			V
I_R	Input diode static reverse current		V_R = 3 V					10	μA
$I_{C(on)}$	On-state collector current	Phototransistor operation	V_{CE} = 0.4 V,	I_F = 0.8 mA,	I_B = 0	100			μA
			V_{CE} = 0.4 V,	I_F = 10 mA,	I_B = 0	5			mA
		Photodiode operation	V_{CB} = 0.4 V,	I_F = 16 mA,	I_E = 0	7	20		μA
$I_{C(off)}$	Off-state collector current	Phototransistor operation	V_{CE} = 10 V,	I_F = 0,	I_B = 0		1	50	nA
		Photodiode operation	V_{CB} = 10 V,	I_F = 0,	I_E = 0		0.1	20	
h_{FE}	Transistor static forward current transfer ratio		V_{CE} = 5 V,	I_C = 10 mA,	I_F = 0	200	550		
V_F	Input diode static forward voltage		I_F = 16 mA				1.2	1.4	V
$V_{CE(sat)}$	Collector-emitter saturation voltage		I_C = 5 mA,	I_F = 10 mA,	I_B = 0		0.25	0.4	V
r_{IO}	Input-to-output internal resistance		V_{in-out} = ±500 V,	See Note 6		10^{11}			Ω
C_{io}	Input-to-output capacitance		V_{in-out} = 0,	f = 1 MHz,	See Note 6		1	1.3	pF

NOTE 6: These parameters are measured between both input-diode leads shorted together and all the phototransistor leads shorted together.

switching characteristics at 25°C free-air temperature

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise time	Phototransistor operation	V_{CC} = 10 V, $I_{C(on)}$ = 2 mA, R_L = 100 Ω, See Test Circuit A of Figure 1		2	10	μs
t_f	Fall time				2	10	
t_r	Rise time	Photodiode operation	V_{CC} = 10 V, $I_{C(on)}$ = 20 μA, R_L = 1 kΩ, See Test Circuit B of Figure 1		1		μs
t_f	Fall time				1		

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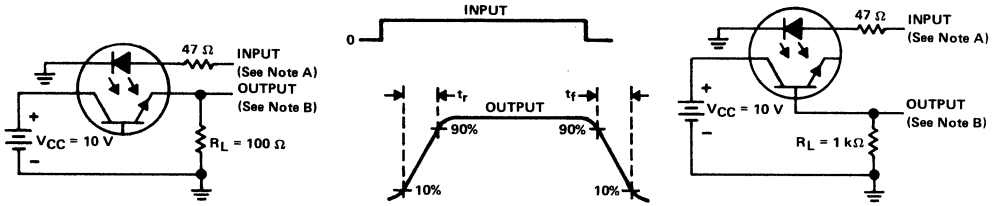
PARAMETER MEASUREMENT INFORMATION

Adjust amplitude of input pulse for:
$I_{C(on)}$ = 2 mA (Test Circuit A) or
$I_{C(on)}$ = 20 μA (Test Circuit B)



TEST CIRCUIT A
PHOTOTRANSISTOR OPERATION

VOLTAGE WAVEFORMS

TEST CIRCUIT B
PHOTODIODE OPERATION

NOTES: A. The input waveform is supplied by a generator with the following characteristics: Z_{out} = 50 Ω, $t_r \leq$ 15 ns, duty cycle ≈ 1%, t_w = 100 μs.
B. The output waveform is monitored on an oscilloscope with the following characteristics: $t_r \leq$ 12 ns, $R_{in} \geq$ 1 MΩ, $C_{in} \leq$ 20 pF.

FIGURE 1. SWITCHING TIMES

TYPICAL CHARACTERISTICS

COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

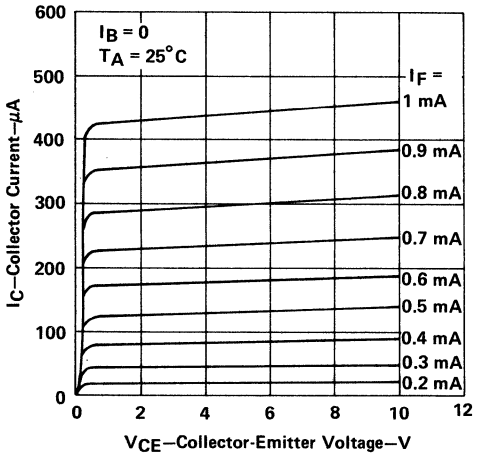


FIGURE 2

COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

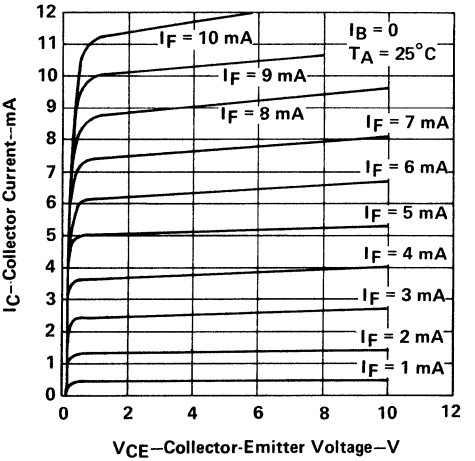


FIGURE 3

TYPICAL CHARACTERISTICS

PHOTOTRANSISTOR COLLECTOR CURRENT
vs
INPUT DIODE FORWARD CURRENT

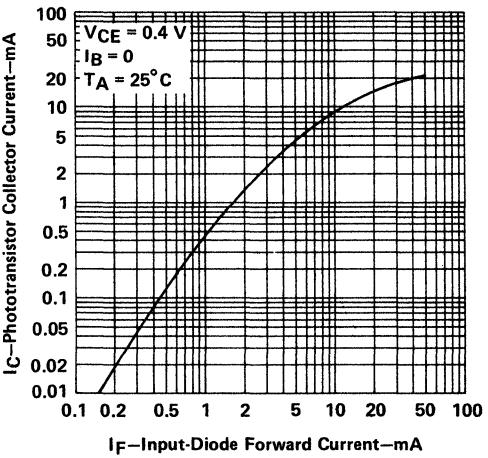


FIGURE 4

RELATIVE ON-STATE COLLECTOR CURRENT
vs
FREE-AIR TEMPERATURE

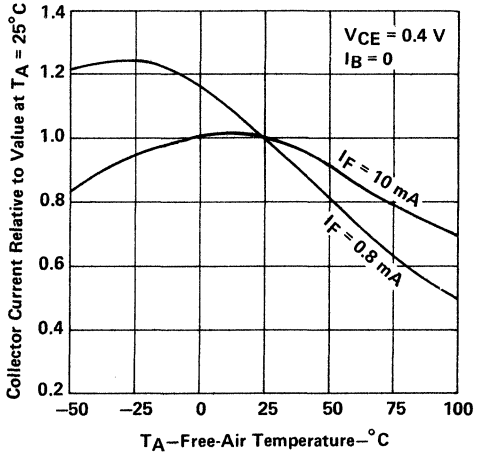


FIGURE 5

NORMALIZED TRANSISTOR STATIC FORWARD CURRENT TRANSFER RATIO
vs
COLLECTOR CURRENT

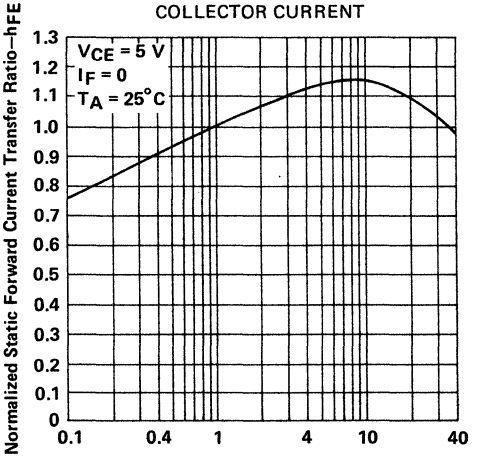


FIGURE 6

NORMALIZED TRANSISTOR STATIC FORWARD CURRENT TRANSFER RATIO
vs
FREE-AIR TEMPERATURE

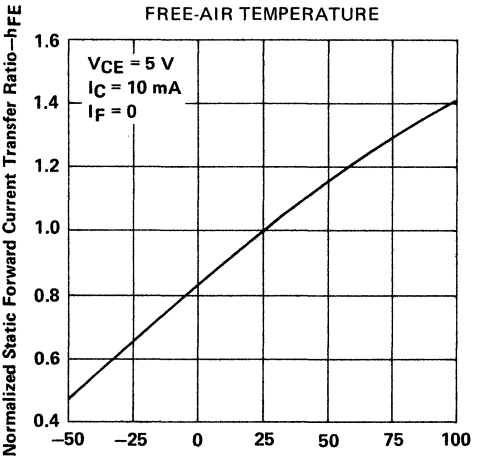


FIGURE 7

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FOR APPLICATIONS IN TELECOMMUNICATIONS EQUIPMENT

- **Breakover Voltage to Common . . . 82 V Max**
- **Reference Voltage . . . 58 V Min**
- **Surge Current 8/20 μs . . . 150 A**
- **Holding Current . . . 150 mA Min**

description

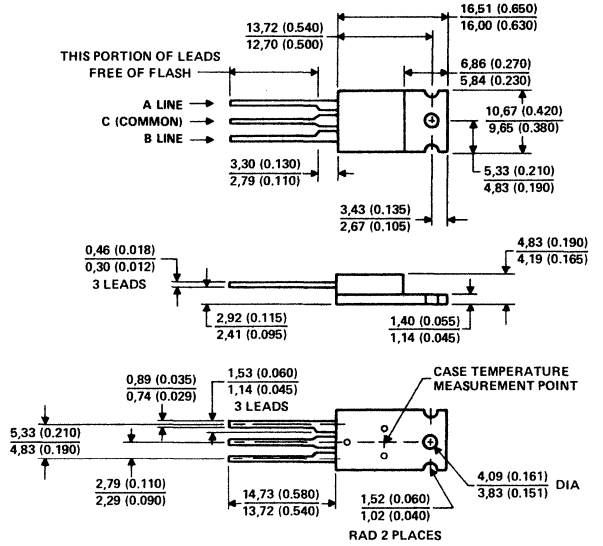
The TISP1082 is designed specifically for telephone line card protection against lightning and transients induced by ac lines when A and B are connected to the TIP and RING circuits. These devices consist of two asymmetrical suppressor sections that will suppress voltage transients between terminals A and C, B and C, and A and B.

Negative transients are initially clipped by zener action until the voltage rises to the breakover level, which causes the device to crowbar. The high crowbar holding current prevents dc latchup as the transient subsides. Positive transients are clipped by diode action. A to B characteristics are symmetrical, and the crowbar action of the device suppresses transients.

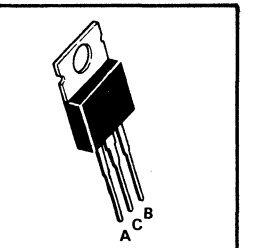
These monolithic protection devices are fabricated in ion-implanted planar structures to ensure precise and symmetrical breakover level.

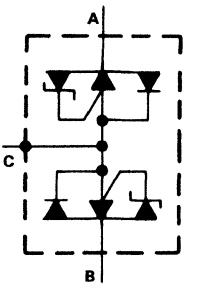
mechanical data

THE COMMON PIN IS IN ELECTRICAL CONTACT WITH THE MOUNTING PAD



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES





DEVICE SCHEMATIC

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

Nonrepetitive peak on-state pulse current, 8/20 μs (see Notes 1, 2, and 3) ..... 150 A
Nonrepetitive peak on-state current, t_W = 10 μs, half sine-wave (see Notes 2 and 3) ..... 15 A
Peak rate of rise of on-state current ..... 250 A/μs
Operating junction temperature ..... 150°C
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −40°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 230°C

NOTES: 1. The notation "8/20 μs" refers to a waveshape having a rise time of 8 μs and a duration of 20 μs ending at 50% of the peak value (see ANSI Standard C62.1).
2. Above 70°C, derate linearly to zero at 150°C case temperature.
3. This value applies when the case temperature is at (or below) 70°C. The surge may be repeated after the device has returned to thermal equilibrium.

electrical characteristics for the A and B terminals†, T_J = 25°C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_Z	Reference voltage	I_Z = −1 mA	−58			V
I_D	Off-state current	V_D = ±50 V			±10	μA
C_{off}	Off-state capacitance	V_D = 0, f = 1 kHz, See Note 4		1	5	pF

† Polarity may be determined arbitrarily.

electrical characteristics for the A and C or the B and C terminals‡, T_J = 25°C

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_Z	Reference voltage	I_Z = −1 mA		−58			V
α_{VZ}	Temperature coefficient of reference voltage				0.1		%/°C
$V_{(BO)}$	Breakover voltage	See Note 5				−82	V
$I_{(BO)}$	Breakover current	See Note 5		−0.15	−0.6		A
V_F	Forward voltage	I_F = 5 A,	See Notes 5 and 6			3	V
V_{TM}	Peak on-state voltage	I_T = −5 A,	See Notes 5 and 6		−2.2	−3	V
I_H	Holding current	See Note 5		−150			mA
dv/dt	Critical rate of rise of off-state voltage	See Note 7				−5	kV/μs
I_D	Off-state current	V_D = −50 V				−10	μA
C_{off}	Off-state capacitance	V_D = 0, See Note 4	f = 1 kHz,		300	500	pF

‡ Polarity is determined at terminal A or B with respect to C.

NOTES: 4. These capacitance measurements employ a three-terminal capacitance bridge incorporating a guard circuit. The third terminal and the mounting tab are connected to the guard terminal of the bridge.
5. These parameters must be measured using pulse techniques, t_W = 100 μs, duty cycle ≤2%.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 3,2 mm (0.125 inch) of the device body.
7. The critical dv/dt is measured using a linear rate of rise with the maximum voltage limited to 80% of V_Z min.

thermal characteristics

	PARAMETER	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance	3.5	°C/W
$R_{\theta JA}$	Junction-to-free-air thermal resistance	62.5	°C/W

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PARAMETER MEASUREMENT INFORMATION

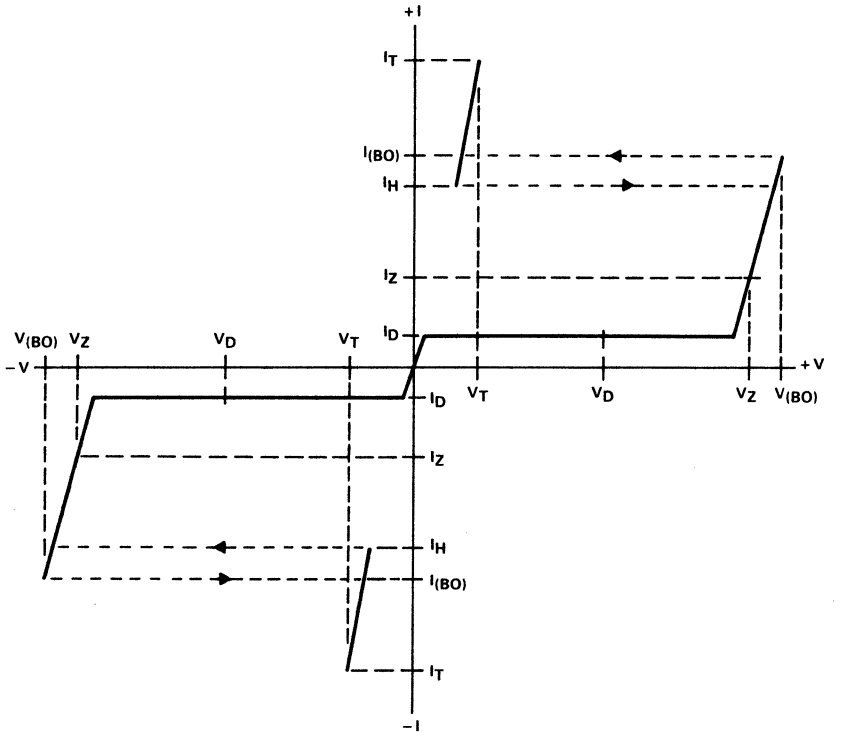


FIGURE 1. VOLTAGE-CURRENT CHARACTERISTICS FOR TERMINALS A AND B†

† Polarity may be determined arbitrarily.

PARAMETER MEASUREMENT INFORMATION

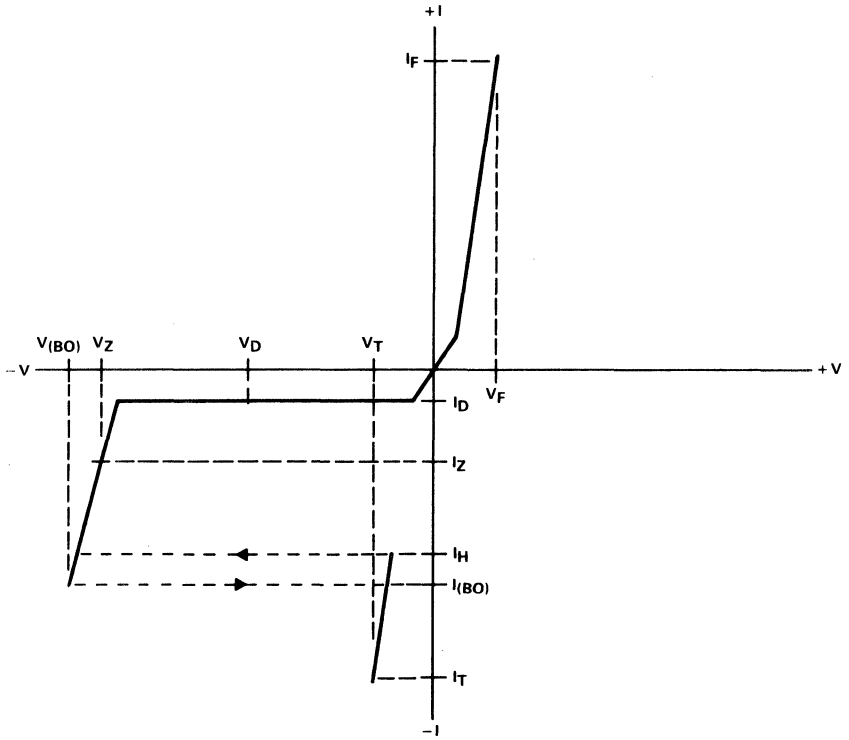


FIGURE 2. VOLTAGE-CURRENT CHARACTERISTICS FOR TERMINALS A AND C OR B AND C‡

‡ Polarity is determined at terminal A or B with respect to C.

TYPICAL APPLICATION DATA

The breakover voltage represents the highest level of stress applied to the system being protected by the suppressor. With an increase in ambient temperature, the reference voltage (the level at which transient voltage clipping just begins) increases at typically 0.09%/°C. Breakover current, however, decreases at typically −0.06%/°C, but operating along the reference resistance line reduces its effect. The net result is that the breakover voltage level is only slightly dependent on ambient temperature.

D-C lockup: The suppressor will remain in a crowbar condition as long as the line can supply a short-circuit current greater than the holding current, I_H. To prevent this from happening, the following conditions must be obtained:

$$\frac{V_{battery}}{R_{line}} < I_H$$

Continuous operation: Line short-circuits to external power supplies can result in overdissipation of the suppressor. Conventional protection techniques such as the use of fuses or PTC thermistors should be used to eliminate or reduce the fault current.

FOR APPLICATIONS IN TELECOMMUNICATIONS EQUIPMENT

- **Breakover Voltage to Common**
  TISP2180 . . . 180 V Max
  TISP2290 . . . 290 V Max
- **Reference Voltage**
  TISP2180 . . . 145 V Min
  TISP2290 . . . 200 V Min
- **Surge Current 8/20 μs . . . 150 A**
- **Holding Current . . . 150 mA Min**

description

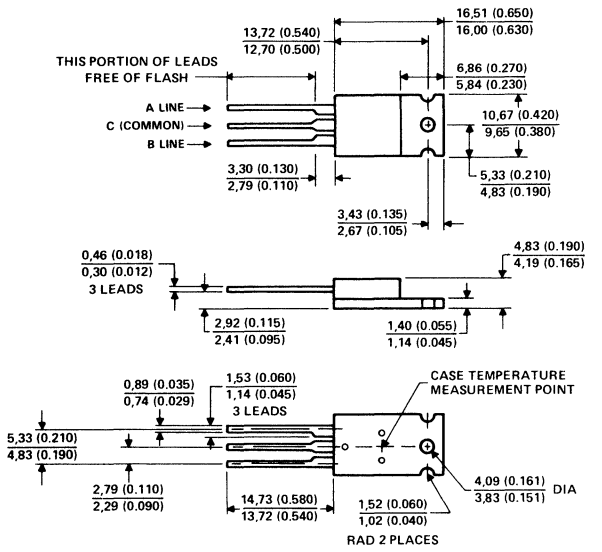
The TISP2000 series is designed specifically for telephone line card protection against lightning and transients induced by ac lines when A and B are connected to the TIP and RING circuits. The TISP2180 and TISP2290 consist of two bidirectional suppressor sections connected to a common C terminal. They will suppress voltage transients between terminals A and C, B and C, and A and B.

Transients are initially clipped by zener action until the voltage rises to the breakover level, which causes the device to crowbar. The high crowbar holding current prevents dc latchup as the transient subsides.

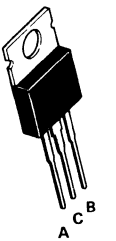
These monolithic protection devices are fabricated in ion-implanted planar structures to ensure precise and symmetrical breakover control.

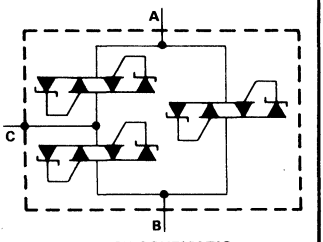
mechanical data

THE COMMON PIN IS IN ELECTRICAL CONTACT WITH THE MOUNTING PAD



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES





DEVICE SCHEMATIC

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

Nonrepetitive peak on-state pulse current 8/20 μs (see Notes 1, 2, and 3) . . . . . 150 A
Nonrepetitive peak on-state current, t_W = 10 ms, half sine-wave (see Notes 2 and 3) . . . . . 15 A
Peak rate of rise of on-state current . . . . . 250 A/μs
Operating junction temperature . . . . . 150°C
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −40°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 230°C

NOTES: 1. The notation "8/20 μs" refers to a waveshape having a rise time of 8 μs and a duration of 20 μs ending at 50% of the peak value (see ANSI Standard C62.1).
2. Above 70°C, derate linearly to zero at 150°C case temperature.
3. This value applies when the case temperature is at (or below) 70°C. The surge may be repeated after the device has returned to thermal equilibrium.

electrical characteristics for the A and B terminals†, T_J = 25°C

PARAMETER		TEST CONDITIONS	TISP2180			TISP2290			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_Z	Reference voltage	I_Z = ±1 mA	±145			±200			V
I_D	Off-state current	V_D = ±50 V			±10			±10	μA
C_{off}	Off-state capacitance	V_D = 0, f = 1 kHz, See Note 4		40	100		40	100	pF

electrical characteristics for the A and C or the B and C terminals†, T_J = 25°C

PARAMETER		TEST CONDITIONS	TISP2180			TISP2290			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_Z	Reference voltage	I_Z = ±1 mA	±145			±200			V
αV_Z	Temperature coefficient of reference voltage			0.1			0.1		%/°C
$V_{(BO)}$	Breakover voltage	See Notes 5 and 6			±180			±290	V
$I_{(BO)}$	Breakover current	See Note 5	±0.15		±0.6	±0.15		±0.6	A
V_{TM}	Peak on-state voltage	I_T = ±5 A, See Notes 5 and 6		±2.2	±3		±1.9	±3	V
I_H	Holding current	See Note 5	±150			±150			mA
dv/dt	Critical rate of rise of off-state voltage	See Note 7			5			5	kV/μs
I_D	Off-state current	V_D = ±50 V			±10			±10	μA
C_{off}	Off-state capacitance	V_D = 0, f = 1 kHz, See Note 4		110	200		110	200	pF

†Polarity may be determined arbitrarily.

NOTES: 4. These capacitance measurements employ a three-terminal capacitance bridge incorporating a guard circuit. The third terminal and the mounting tab are connected to the guard terminal of the bridge.
5. These parameters must be measured using pulse techniques, t_W = 100 μs, duty cycle ≤ 2%.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 3,2 mm (0.125 inch) from the device body.
7. The critical dv/dt is measured using a linear rate of rise with the maximum voltage limited to 80% of V_Z min.

thermal characteristics

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance			3.5	°C/W
$R_{\theta JA}$	Junction-to-free-air thermal resistance			62.5	°C/W

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PARAMETER MEASUREMENT INFORMATION

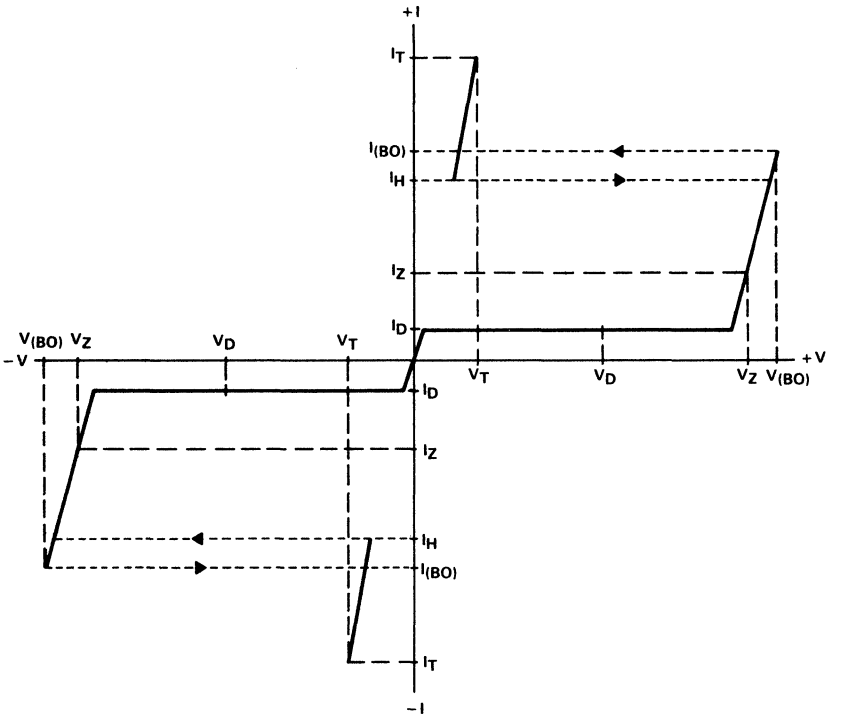


FIGURE 1. VOLTAGE-CURRENT CHARACTERISTICS FOR ANY PAIR OF TERMINALS†

†Polarity may be determined arbitrarily.

TYPICAL APPLICATION DATA

The breakover voltage represents the highest level of stress applied to the system being protected by the suppressor. With an increase in ambient temperature, the reference voltage (the level at which transient voltage clipping just begins) increases at typically 0.09%/°C. Breakover current, however, decreases at typically −0.06%/°C, but operating along the reference resistance line reduces its effect. The net result is that the breakover voltage level is only slightly dependent on ambient temperature.

D-C lockup: The suppressor will remain in a crowbar condition as long as the line can supply a short-circuit current greater than the holding current, I_H. To prevent this from happening, the following conditions must be obtained.:

$$\frac{V_{battery}}{R_{line}} < I_H$$

Continuous operation: Line short-circuits to external power supplies can result in overdissipation of the suppressor. Conventional protection techniques such as the use of fuses or PTC thermistors should be used to eliminate or reduce the fault current.

FOR APPLICATIONS IN TELECOMMUNICATIONS EQUIPMENT

- **Breakover Voltage to Common**
  TISP3180 . . . 180 V Max
  TISP3290 . . . 290 V Max
- **Reference Voltage**
  TISP3180 . . . 145 V Min
  TISP3290 . . . 200 V Min
- **Surge Current 8/20 μs . . . 150 A**
- **Holding Current . . . 150 mA Min**

description

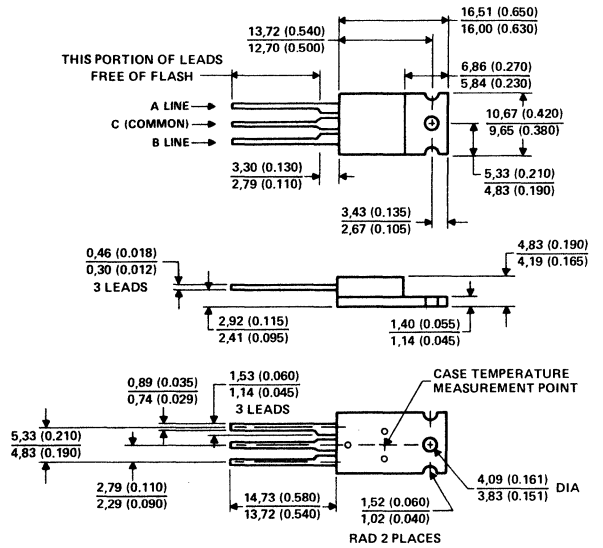
The TISP3000 series is designed specifically for telephone line card protection against lightning and transients induced by ac power lines when A and B are connected to the TIP and RING circuits. The TISP3180 and TISP3290 consist of two bidirectional suppressor sections connected to a common C terminal. They will suppress voltage transients between terminals A and C, B and C, and A and B.

Transients are initially clipped by zener action until the voltage rises to the breakover level, which causes the device to crowbar. The high crowbar holding current prevents dc latchup as the transient subsides.

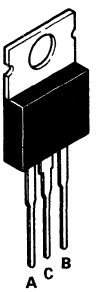
These monolithic protection devices are fabricated in ion-implanted planar structures to ensure precise and symmetrical breakover control.

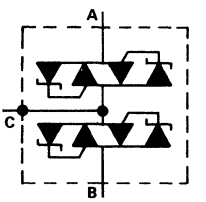
mechanical data

THE COMMON PIN IS IN ELECTRICAL CONTACT WITH THE MOUNTING PAD



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES





DEVICE SCHEMATIC

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

Nonrepetitive peak on-state pulse current 8/20 μs (see Notes 1, 2, and 3)	150 A
Nonrepetitive peak on-state current, t_W = 10 ms, half sine-wave (see Notes 2 and 3)	15 A
Peak rate of rise of on-state current	250 A/μs
Junction temperature	150°C
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−40°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	230°C

NOTES: 1. The notation "8/20 μs" refers to a waveshape having a rise time of 8 μs and a duration of 20 μs ending at 50% of the peak value (see ANSI Standard C62.1).
2. Above 70°C, derate linearly to zero at 150°C case temperature.
3. This value applies when the case temperature is at (or below) 70°C. The surge may be repeated after the device has returned to thermal equilibrium.

electrical characteristics for the A and B terminals†, T_J = 25°C

PARAMETER		TEST CONDITIONS	TISP3180			TISP3290			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_Z	Reference voltage	I_Z = ±1 mA	±290			±400			V
I_D	Off-state current	V_D = ±50 V			±10			±10	μA
C_{off}	Off-state capacitance	V_D = 0, f = 1 kHz, See Note 4		0.5	5		0.5	5	pF

electrical characteristics for the A and C or the B and C terminals†, T_J = 25°C

PARAMETER		TEST CONDITIONS	TISP3180			TISP3290			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_Z	Reference voltage	I_Z = ±1 mA	±145			±200			V
αV_Z	Temperature coefficient of reference voltage				0.1			0.1	%/°C
$V_{(BO)}$	Breakover voltage	See Notes 5 and 6			±180			±290	V
$I_{(BO)}$	Breakover current	See Note 5	±0.15		±0.6	±0.15		±0.6	A
V_{TM}	Peak on-state voltage	I_T = ±5 A, See Notes 5 and 6		±2.2	±3		±1.9	±3	V
I_H	Holding current	See Note 5	±150			±150			mA
dv/dt	Critical rate of rise of off-state voltage	See Note 7			5			5	kV/μs
I_D	Off-state current	V_D = ±50 V			±10			±10	μA
C_{off}	Off-state capacitance	V_D = 0, f = 1 kHz, See Note 4		105	250		95	250	pF

†Polarity may be determined arbitrarily.

NOTES: 4. These capacitance measurements employ a three-terminal capacitance bridge incorporating a guard circuit. The third terminal and the mounting tab are connected to the guard terminal of the bridge.
5. These parameters must be measured using pulse techniques, t_W = 100 μs, duty cycle ≤ 2%.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 3,2 mm (0.125 inch) from the device body.
7. The critical dv/dt is measured using a linear rate of rise with the maximum voltage limited to 80% of V_Z min.

thermal characteristics

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance			3.5	°C/W
$R_{\theta JA}$	Junction-to-free-air thermal resistance			62.5	°C/W

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PARAMETER MEASUREMENT INFORMATION

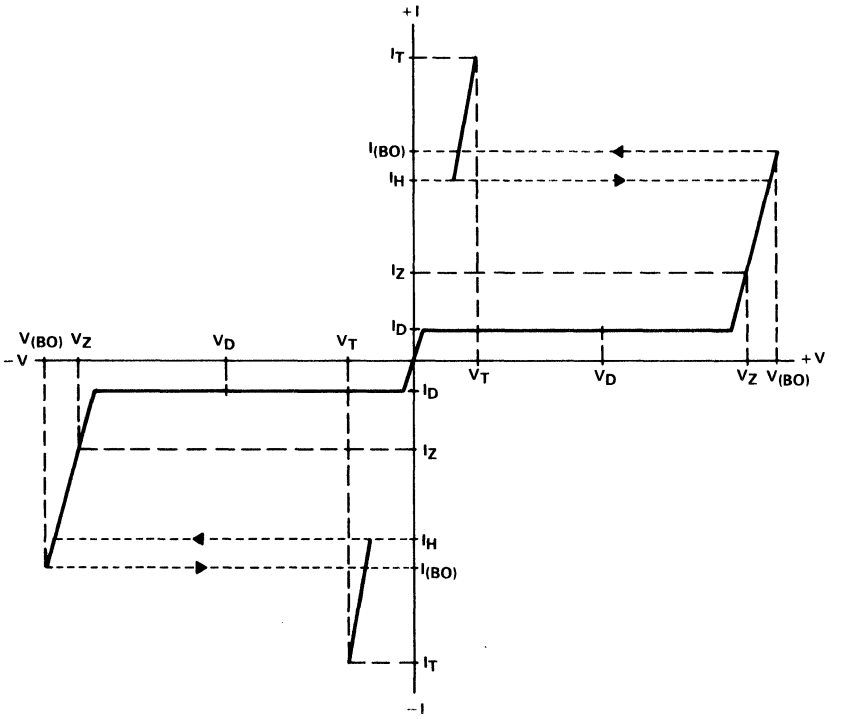


FIGURE 1. VOLTAGE-CURRENT CHARACTERISTICS FOR ANY PAIR OF TERMINALS†

†Polarity may be determined arbitrarily.

TYPICAL APPLICATION DATA

The breakover voltage represents the highest level of stress applied to the system being protected by the suppressor. With an increase in ambient temperature, the reference voltage (the level at which transient voltage clipping just begins) increases at typically 0.09%/°C. Breakover current, however, decreases at typically −0.06%/°C, but operating along the reference resistance line reduces its effect. The net result is that the breakover voltage level is only slightly dependent on ambient temperature.

D-C lockup: The suppressor will remain in a crowbar condition as long as the line can supply a short-circuit current greater than the holding current, I_H. To prevent this from happening, the following conditions must be obtained.:

$$\frac{V_{battery}}{R_{line}} < I_H$$

Continuous operation: Line short-circuits to external power supplies can result in overdissipation of the suppressor. Conventional protection techniques such as the use of fuses or PTC thermistors should be used to eliminate or reduce the fault current.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

FOR APPLICATIONS IN TELECOMMUNICATIONS EQUIPMENT

- **Breakover Voltage to Common**
  TISP4180 . . . 180 V Max
  TISP4290 . . . 290 V Max
- **Reference Voltage**
  TISP4180 . . . 145 V Min
  TISP4290 . . . 200 V Min
- **Surge Current 8/20 μs . . . 150 A**
- **Holding Current . . . 150 mA Min**

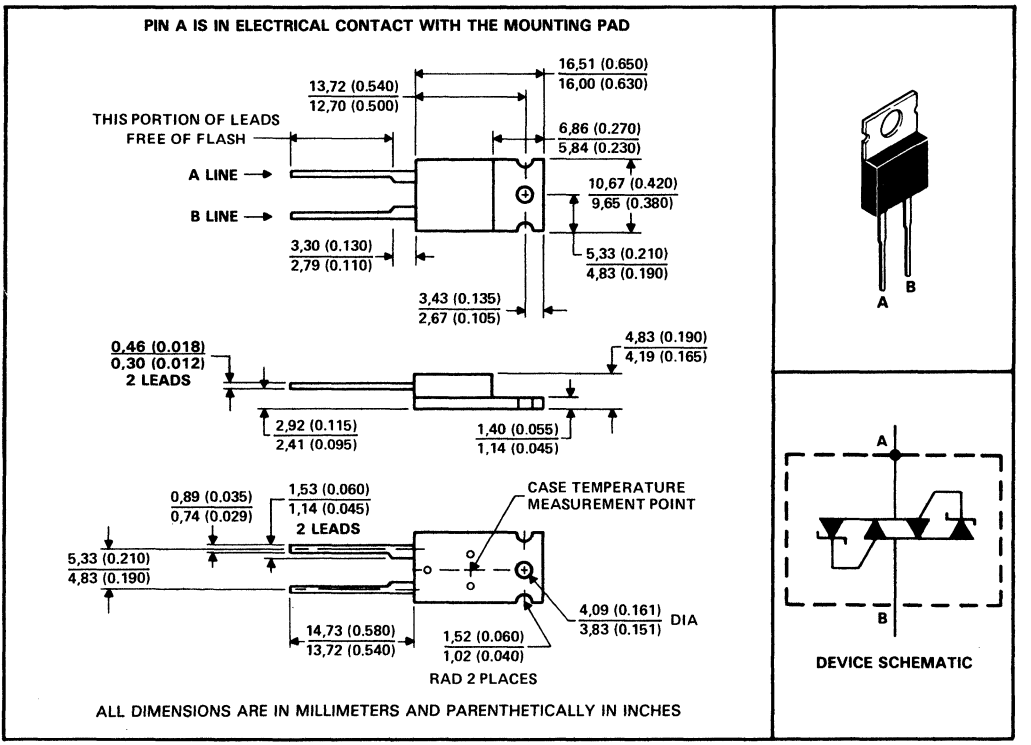
description

The TISP4000 series is designed specifically for telephone line card protection against lightning and transients induced by ac power lines. The TISP4180 and TISP4290 consist of a bidirectional suppressor element connecting the A and B terminals. They will suppress interwire transients.

Transients are initially clipped by zener action until the voltage rises to the breakover level, which causes the device to crowbar. The high crowbar holding current prevents dc latchup as the transient subsides.

These monolithic protection devices are fabricated in ion-implanted planar structures to ensure precise and symmetrical breakover control.

mechanical data



absolute maximum ratings at 25°C case temperature (unless otherwise noted)

Nonrepetitive peak on-state pulse current 8/20 μs (see Notes 1, 2, and 3) . . . . . 150 A
Nonrepetitive peak on-state current, t_W = 10 ms, half sine-wave (see Notes 2 and 3) . . . . . 15 A
Peak rate of rise of on-state current . . . . . 250 A/μs
Junction temperature . . . . . 150°C
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −40°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 230°C

NOTES: 1. The notation "8/20 μs" refers to a waveshape having a rise time of 8 μs and a duration of 20 μs ending at 50% of the peak value (see ANSI Standard C62.1).
2. Above 70°C, derate linearly to zero at 150°C case temperature.
3. This value applies when the case temperature is at (or below) 70°C. The surge may be repeated after the device has returned to thermal equilibrium.

electrical characteristics†, T_J = 25°C

PARAMETER		TEST CONDITIONS	TISP4180			TISP4290			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_Z	Reference voltage	I_Z = ±1 mA	±120			±200			V
α_{VZ}	Temperature coefficient of reference voltage				0.1			0.1	%/°C
$V_{(BO)}$	Breakover voltage	See Notes 4 and 5			±180			±290	V
$I_{(BO)}$	Breakover current	See Note 4	±0.15		±0.6	±0.15		±0.6	A
V_{TM}	Peak on-state voltage	I_T = ±5 A, See Notes 4 and 5		±2.2	±3		±1.9	±3	V
I_H	Holding current	See Note 4	±150			±150			mA
dv/dt	Critical rate of rise of off-state voltage	See Note 6			5			5	kV/μs
I_D	Off-state current	V_D = ±50 V			±10			±10	μA
C_{off}	Off-state capacitance	V_D = 0, f = 1 kHz, See Note 7		110	200		110	200	pF

†Polarity may be determined arbitrarily.

NOTES: 4. These capacitance measurements employ a three-terminal capacitance bridge incorporating a guard circuit. The third terminal and the mounting tab are connected to the guard terminal of the bridge.
5. These parameters must be measured using pulse techniques, t_W = 100 μs, duty cycle ≤ 2%.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 3,2 mm (0.125 inch) from the device body.
7. The critical dv/dt is measured using a linear rate of rise with the maximum voltage limited to 80% of V_Z min.

thermal characteristics

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance			3.5	°C/W
$R_{\theta JA}$	Junction-to-free-air thermal resistance			62.5	°C/W

PARAMETER MEASUREMENT INFORMATION

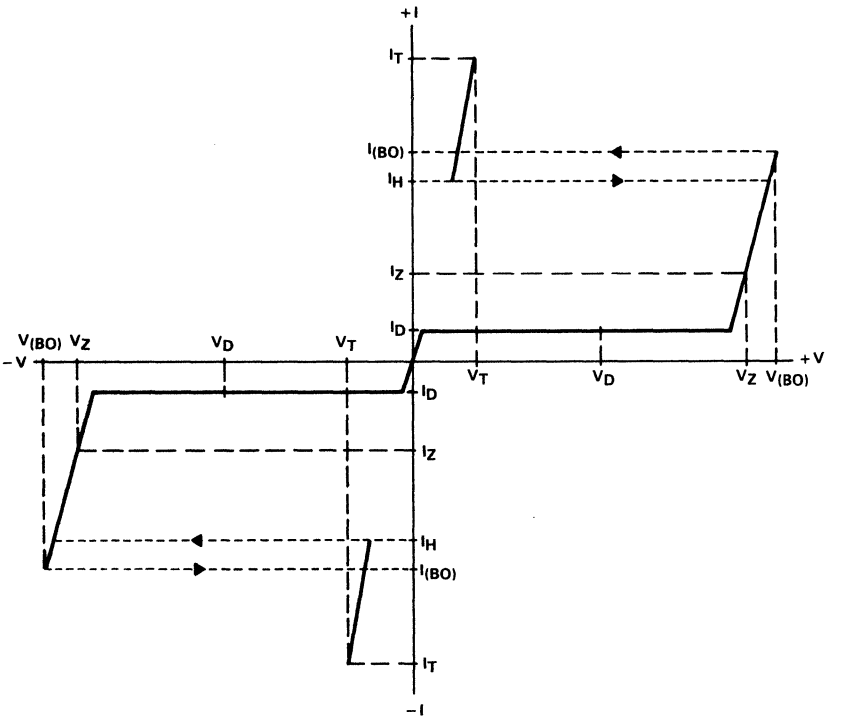


FIGURE 1. VOLTAGE-CURRENT CHARACTERISTICS†

†Polarity may be determined arbitrarily.

TYPICAL APPLICATION DATA

The breakover voltage represents the highest level of stress applied to the system being protected by the suppressor. With an increase in ambient temperature, the reference voltage (the level at which transient voltage clipping just begins) increases at typically 0.09%/°C. Breakover current, however, decreases at typically −0.06%/°C, but operating along the reference resistance line reduces its effect. The net result is that the breakover voltage level is only slightly dependent on ambient temperature.

D-C lockup: The suppressor will remain in a crowbar condition as long as the line can supply a short-circuit current greater than the holding current, I_H. To prevent this from happening, the following conditions must be obtained.:

$$\frac{V_{battery}}{R_{line}} < I_H$$

Continuous operation: Line short-circuits to external power supplies can result in overdissipation of the suppressor. Conventional protection techniques such as the use of fuses or PTC thermistors should be used to eliminate or reduce the fault current.

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FOR APPLICATIONS IN TELECOMMUNICATIONS EQUIPMENT

- **Breakover Voltage to Common**
  TISP7180 . . . 180 V Max
  TISP7290 . . . 290 V Max
- **Surge Current 8/20 μs**
  TISP7180 . . . 100 A
  TISP7290 . . . 150 A
- **Reference Voltage**
  TISP7180 . . . 145 V Min
  TISP7290 . . . 200 V Min
- **Holding Current . . . 150 mA Min**

description

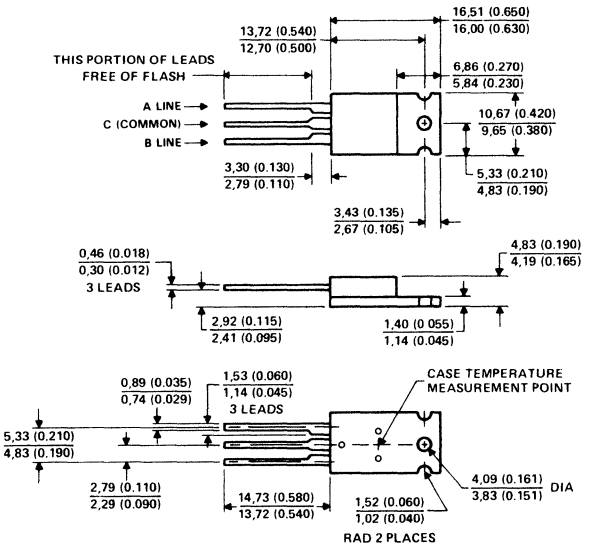
The TISP7000 series is designed specifically for telephone line card protection against lightning and transients induced by ac power lines. The TISP7180 and TISP7290 consist of three bidirectional suppressor sections that will suppress voltage transients between terminals A and C, B and C, and A and B.

Transients are initially clipped by zener action until the voltage rises to the breakover level, which causes the device to crowbar. The high crowbar holding current prevents dc latchup as the transient subsides.

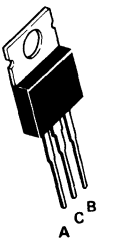
These monolithic protection devices are fabricated in ion-implanted planar structures to ensure precise and symmetrical breakover control.

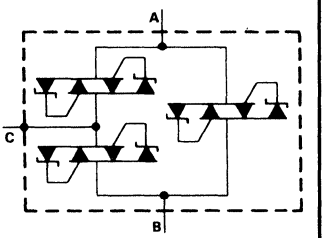
mechanical data

THE COMMON PIN IS IN ELECTRICAL CONTACT WITH THE MOUNTING PAD



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES





DEVICE SCHEMATIC

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

Nonrepetitive peak on-state pulse current 8/20 μs (see Notes 1, 2, and 3) . . . . . 150 A
Nonrepetitive peak on-state current, t_W = 10 ms, half sine-wave (see Notes 2 and 3) . . . . . 15 A
Peak rate of rise of on-state current . . . . . 250 A/μs
Junction temperature . . . . . 150°C
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −40°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 230°C

NOTES: 1. The notation "8/20 μs" refers to a waveshape having a rise time of 8 μs and a duration of 20 μs ending at 50% of the peak value (see ANSI Standard C62.1).
2. Above 70°C, derate linearly to zero at 150°C case temperature.
3. This value applies when the case temperature is at (or below) 70°C. The surge may be repeated after the device has returned to thermal equilibrium.

electrical characteristics for the A and B terminals†, T_J = 25°C

PARAMETER		TEST CONDITIONS	TISP7180			TISP7290			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_Z	Reference voltage	I_Z = ±1 mA	±145			±200			V
I_D	Off-state current	V_D = ±50 V			±10			±10	μA
C_{off}	Off-state capacitance	V_D = 0, f = 1 kHz, See Note 4		40	100		40	100	pF

electrical characteristics for the A and C or the B and C terminals†, T_J = 25°C

PARAMETER		TEST CONDITIONS	TISP7180			TISP7290			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_Z	Reference voltage	I_Z = ±1 mA	±145			±200			V
αV_Z	Temperature coefficient of reference voltage				0.1			0.1	%/°C
$V_{(BO)}$	Breakover voltage	See Notes 5 and 6			±180			±290	V
$I_{(BO)}$	Breakover current	See Note 5	±0.15		±0.6	±0.15		±0.6	A
V_{TM}	Peak on-state voltage	I_T = ±5 A, See Notes 5 and 6		±2.2	±3		±1.9	±3	V
I_H	Holding current	See Note 5	±150			±150			mA
dv/dt	Critical rate of rise of off-state voltage	See Note 7			5			5	kV/μs
I_D	Off-state current	V_D = ±50 V			±10			±10	μA
C_{off}	Off-state capacitance	V_D = 0, f = 1 kHz, See Note 4		70	150		70	150	pF

†Polarity may be determined arbitrarily.

NOTES: 4. These capacitance measurements employ a three-terminal capacitance bridge incorporating a guard circuit. The third terminal and the mounting tab are connected to the guard terminal of the bridge.
5. These parameters must be measured using pulse techniques, t_W = 100 μs, duty cycle ≤ 2%.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 3,2 mm (0.125 inch) from the device body.
7. The critical dv/dt is measured using a linear rate of rise with the maximum voltage limited to 80% of V_Z min.

thermal characteristics

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance			3.5	°C/W
$R_{\theta JA}$	Junction-to-free-air thermal resistance			62.5	°C/W

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PARAMETER MEASUREMENT INFORMATION

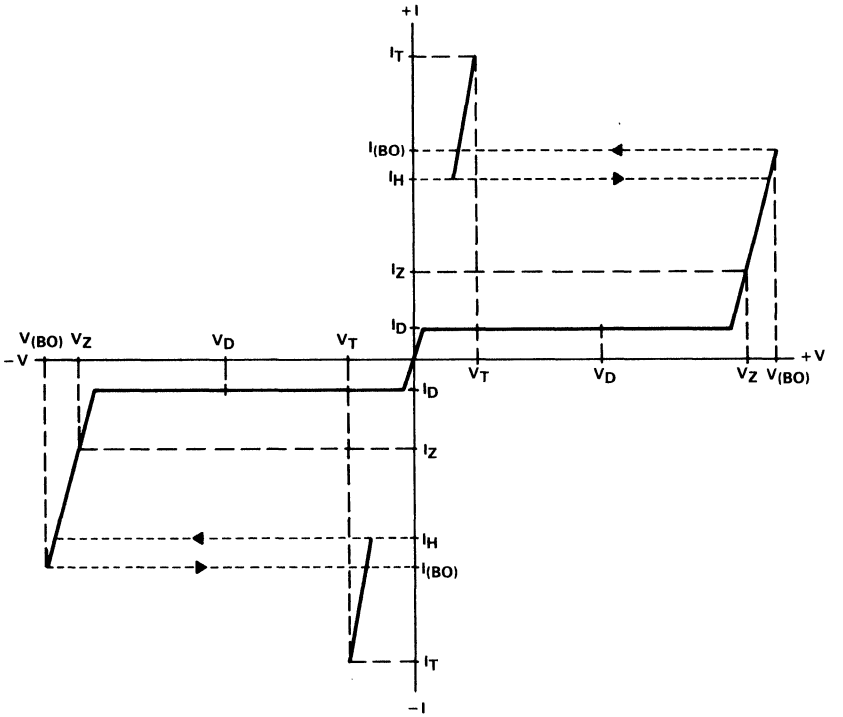


FIGURE 1. VOLTAGE-CURRENT CHARACTERISTICS FOR ANY PAIR OF TERMINALS†

†Polarity may be determined arbitrarily.

TYPICAL APPLICATION DATA

The breakover voltage represents the highest level of stress applied to the system being protected by the suppressor. With an increase in ambient temperature, the reference voltage (the level at which transient voltage clipping just begins) increases at typically 0.09%/°C. Breakover current, however, decreases at typically −0.06%/°C, but operating along the reference resistance line reduces its effect. The net result is that the breakover voltage level is only slightly dependent on ambient temperature.

D-C lockup: The suppressor will remain in a crowbar condition as long as the line can supply a short-circuit current greater than the holding current, I_H. To prevent this from happening, the following conditions must be obtained.:

$$\frac{V_{battery}}{R_{line}} < I_H$$

Continuous operation: Line short-circuits to external power supplies can result in overdissipation of the suppressor. Conventional protection techniques such as the use of fuses or PTC thermistors should be used to eliminate or reduce the fault current.

FOR APPLICATIONS IN TELECOMMUNICATIONS EQUIPMENT

- **Breakover Voltage to Common**
  TISP8180 . . . 180 V Max
  TISP8290 . . . 290 V Max
- **Surge Current 8/20 μs**
  TISP8180 . . . 100 A
  TISP8290 . . . 150 A
- **Reference Voltage**
  TISP8180 . . . 145 V Min
  TISP8290 . . . 200 V Min
- **Holding Current . . . 150 mA Min**

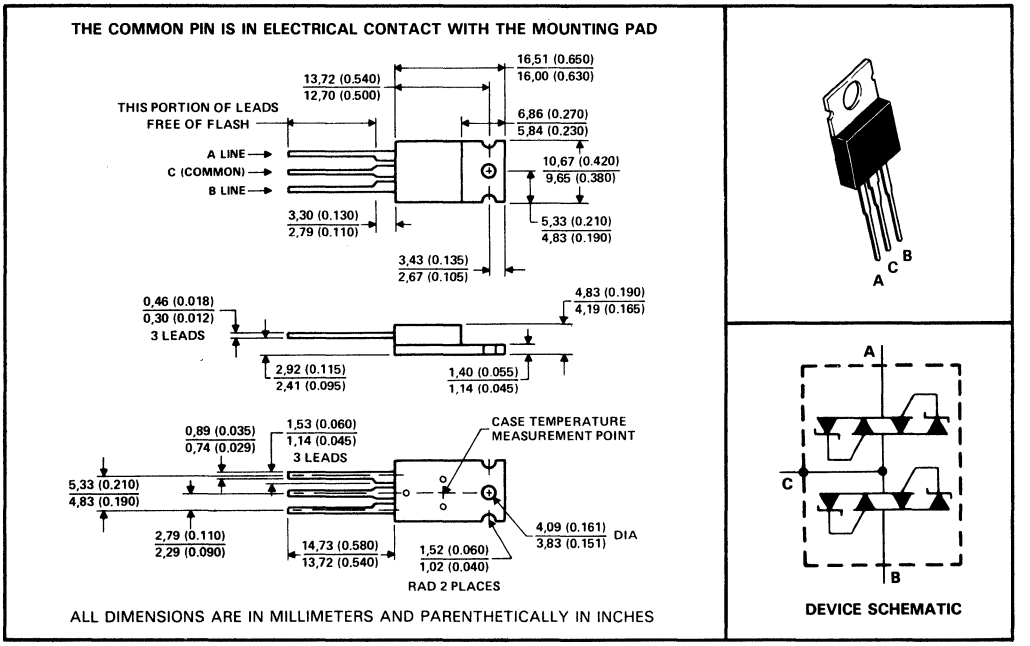
description

The TISP8000 series is designed specifically for telephone line card protection against lightning and transients, induced by ac lines when A and B are connected to the TIP and RING circuits. The TISP8180 and TISP8290 consist of two bidirectional suppressor sections that will suppress voltage transients between terminals A and C, B and C, and A and B.

Transients are initially clipped by zener action until the voltage rises to the breakover level, which causes the device to crowbar. The high crowbar holding current prevents dc latchup as the transient subsides.

These monolithic protection devices are fabricated in ion-implanted planar structures to ensure precise and symmetrical breakover control.

mechanical data



absolute maximum ratings at 25°C case temperature (unless otherwise noted)

Nonrepetitive peak on-state pulse current 8/20 μs (see Notes 1, 2, and 3) . . . . . 150 A
Nonrepetitive peak on-state current, t_W = 10 ms, half sine-wave (see Notes 2 and 3) . . . . . 15 A
Peak rate of rise of on-state current . . . . . 250 A/μs
Junction temperature . . . . . 150°C
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −40°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 230°C

NOTES: 1. The notation "8/20 μs" refers to a waveshape having a rise time of 8 μs and a duration of 20 μs ending at 50% of the peak value (see ANSI Standard C62.1).
2. Above 70°C, derate linearly to zero at 150°C case temperature.
3. This value applies when the case temperature is at (or below) 70°C. The surge may be repeated after the device has returned to thermal equilibrium.

electrical characteristics for the A and B terminals†, T_J = 25°C

PARAMETER		TEST CONDITIONS	TISP8180			TISP8290			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_Z	Reference voltage	I_Z = ±1 mA	±290			±400			V
I_D	Off-state current	V_D = ±50 V			±10			±10	μA
C_{off}	Off-state capacitance	V_D = 0, f = 1 kHz, See Note 4		0.5	5		0.5	5	pF

electrical characteristics for the A and C or the B and C terminals†, T_J = 25°C

PARAMETER		TEST CONDITIONS	TISP8180			TISP8290			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_Z	Reference voltage	I_Z = ±1 mA	±145			±200			V
α_{VZ}	Temperature coefficient of reference voltage				0.1			0.1	%/°C
$V_{(BO)}$	Breakover voltage	See Notes 5 and 6			±180			±290	V
$I_{(BO)}$	Breakover current	See Note 5	±0.15		±0.6	±0.15		±0.6	A
V_{TM}	Peak on-state voltage	I_T = ±5 A, See Notes 5 and 6		±2.2	±3		±1.9	±3	V
I_H	Holding current	See Note 5	±150			±150			mA
dv/dt	Critical rate of rise of off-state voltage	See Note 7			5			5	kV/μs
I_D	Off-state current	V_D = ±50 V			±10			±10	μA
C_{off}	Off-state capacitance	V_D = 0, f = 1 kHz, See Note 4		70	150		70	150	pF

†Polarity may be determined arbitrarily.

NOTES: 4. These capacitance measurements employ a three-terminal capacitance bridge incorporating a guard circuit. The third terminal and the mounting tab are connected to the guard terminal of the bridge.
5. These parameters must be measured using pulse techniques, t_W = 100 μs, duty cycle ≤ 2%.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 3,2 mm (0.125 inch) from the device body.
7. The critical dv/dt is measured using a linear rate of rise with the maximum voltage limited to 80% of V_Z min.

thermal characteristics

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance			3.5	°C/W
$R_{\theta JA}$	Junction-to-free-air thermal resistance			62.5	°C/W

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PARAMETER MEASUREMENT INFORMATION

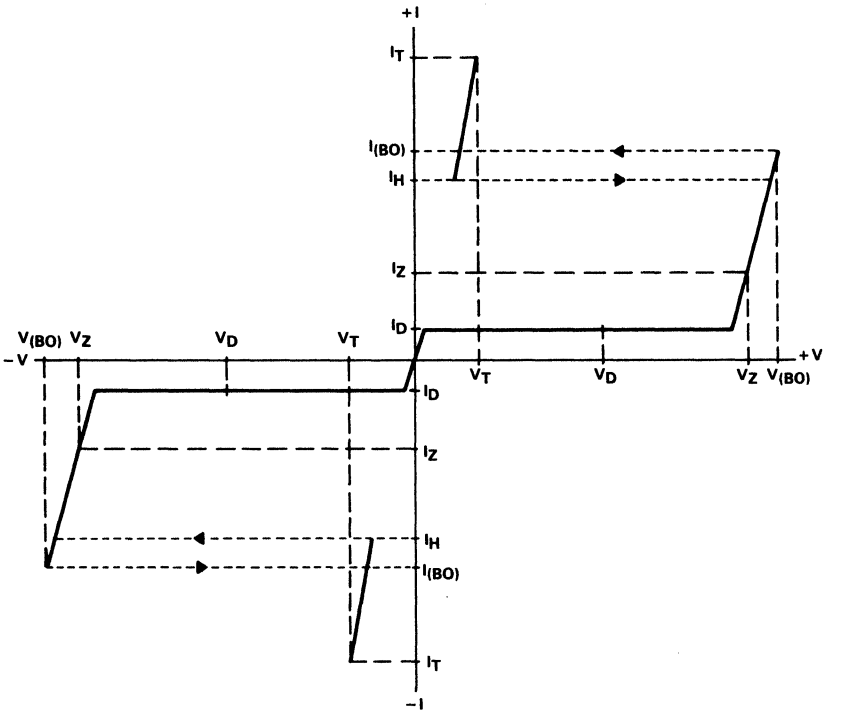

FIGURE 1. VOLTAGE-CURRENT CHARACTERISTICS FOR ANY PAIR OF TERMINALS†

†Polarity may be determined arbitrarily.

TYPICAL APPLICATION DATA

The breakover voltage represents the highest level of stress applied to the system being protected by the suppressor. With an increase in ambient temperature, the reference voltage (the level at which transient voltage clipping just begins) increases at typically 0.09%/°C. Breakover current, however, decreases at typically −0.06%/°C, but operating along the reference resistance line reduces its effect. The net result is that the breakover voltage level is only slightly dependent on ambient temperature.

D-C lockup: The suppressor will remain in a crowbar condition as long as the line can supply a short-circuit current greater than the holding current, I_H. To prevent this from happening, the following conditions must be obtained.:

$$\frac{V_{battery}}{R_{line}} < I_H$$

Continuous operation: Line short-circuits to external power supplies can result in overdissipation of the suppressor. Conventional protection techniques such as the use of fuses or PTC thermistors should be used to eliminate or reduce the fault current.

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FOR APPLICATIONS IN TELECOMMUNICATIONS EQUIPMENT

- **Breakover Voltage to Common**
  TISP9180 . . . 180 V Max
  TISP9290 . . . 290 V Max
- **Surge Current 8/20 μs**
  TISP9180 . . . 100 A
  TISP9290 . . . 150 A
- **Reference Voltage**
  TISP9180 . . . 145 V Min
  TISP9290 . . . 200 V Min
- **Holding Current . . . 150 mA Min**

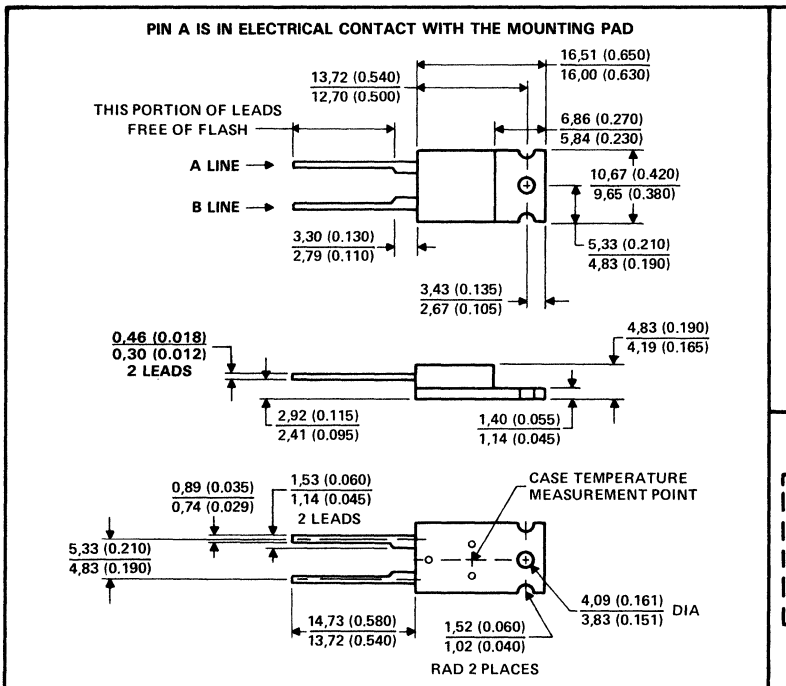
description

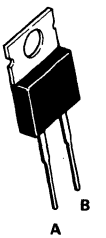
The TISP9000 series is designed specifically for telephone line card protection against lightning and transients, induced by ac power lines. The TISP9180 and TISP9290 consist of a bidirectional suppressor element that will suppress voltage transients between terminals A and B. These devices also suppress interwire voltage transients.

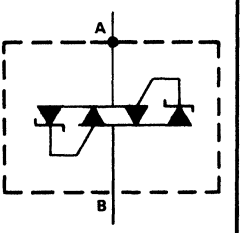
Transients are initially clipped by zener action until the voltage rises to the breakover level, which causes the device to crowbar. The high crowbar holding current prevents dc latchup as the transient subsides.

These monolithic protection devices are fabricated in ion-implanted planar structures to ensure precise and symmetrical breakover control.

mechanical data







DEVICE SCHEMATIC

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

Nonrepetitive peak on-state pulse current 8/20 μs (see Notes 1, 2, and 3)	150 A
Nonrepetitive peak on-state current, t_W = 10 ms, half sine-wave (see Notes 2 and 3)	15 A
Peak rate of rise of on-state current	250 A/μs
Junction temperature	150°C
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−40°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	230°C

NOTES: 1. The notation "8/20 μs" refers to a waveshape having a rise time of 8 μs and a duration of 20 μs ending at 50% of the peak value (see ANSI Standard C62.1).
2. Above 70°C, derate linearly to zero at 150°C case temperature.
3. This value applies when the case temperature is at (or below) 70°C. The surge may be repeated after the device has returned to thermal equilibrium.

electrical characteristics†, T_J = 25°C

PARAMETER		TEST CONDITIONS	TISP9180			TISP9290			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_Z	Reference voltage	I_Z = ±1 mA	±145			±200			V
α_{VZ}	Temperature coefficient of reference voltage				0.1			0.1	%/°C
$V_{(BO)}$	Breakover voltage	See Notes 5 and 6			±180			±290	V
$I_{(BO)}$	Breakover current	See Note 5	±0.15		±0.6	±0.15		±0.6	A
V_{TM}	Peak on-state voltage	I_T = ±5 A, See Notes 5 and 6		±2.2	±3		±1.9	±3	V
I_H	Holding current	See Note 5	±150			±150			
dv/dt	Critical rate of rise of off-state voltage	See Note 7			5			5	kV/μs
I_D	Off-state current	V_D = ±50 V			±10			±10	μA
C_{off}	Off-state capacitance	V_D = 0, f = 1 kHz, See Note 4		110	200		110	200	pF

†Polarity may be determined arbitrarily.

NOTES: 4. These capacitance measurements employ a three-terminal capacitance bridge incorporating a guard circuit. The third terminal and the mounting tab are connected to the guard terminal of the bridge.
5. These parameters must be measured using pulse techniques, t_W = 100 μs, duty cycle ≤ 2%.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 3,2 mm (0.125 inch) from the device body.
7. The critical dv/dt is measured using a linear rate of rise with the maximum voltage limited to 80% of V_Z min.

thermal characteristics

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance			3.5	°C/W
$R_{\theta JA}$	Junction-to-free-air thermal resistance			62.5	°C/W

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PARAMETER MEASUREMENT INFORMATION

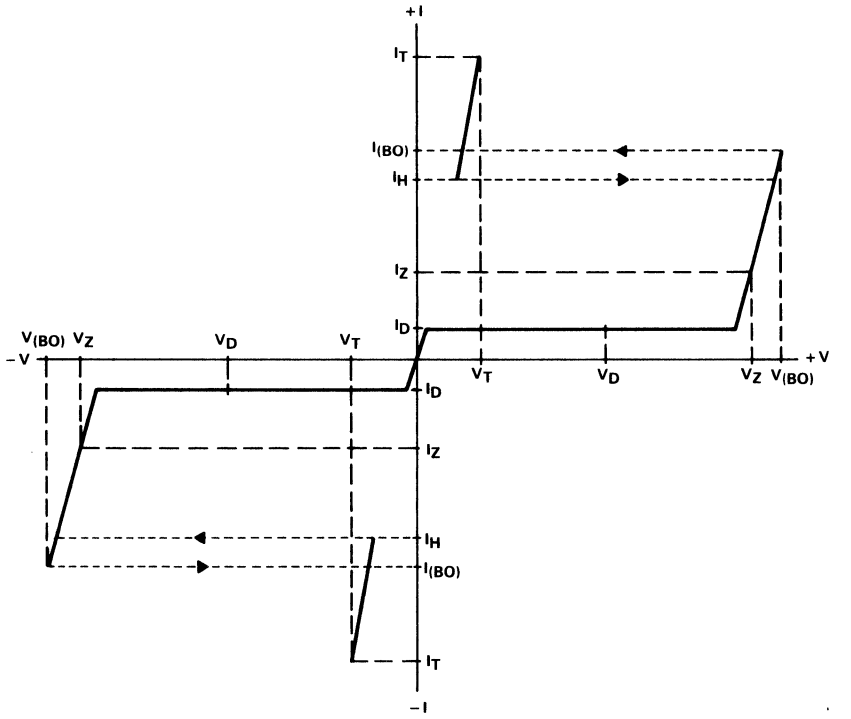

FIGURE 1. VOLTAGE-CURRENT CHARACTERISTICS†

†Polarity may be determined arbitrarily.

TYPICAL APPLICATION DATA

The breakover voltage represents the highest level of stress applied to the system being protected by the suppressor. With an increase in ambient temperature, the reference voltage (the level at which transient voltage clipping just begins) increases at typically 0.09%/°C. Breakover current, however, decreases at typically −0.06%/°C, but operating along the reference resistance line reduces its effect. The net result is that the breakover voltage level is only slightly dependent on ambient temperature.

D-C lockup: The suppressor will remain in a crowbar condition as long as the line can supply a short-circuit current greater than the holding current, I_H. To prevent this from happening, the following conditions must be obtained.:

$$\frac{V_{battery}}{R_{line}} < I_H$$

Continuous operation: Line short-circuits to external power supplies can result in overdissipation of the suppressor. Conventional protection techniques such as the use of fuses or PTC thermistors should be used to eliminate or reduce the fault current.

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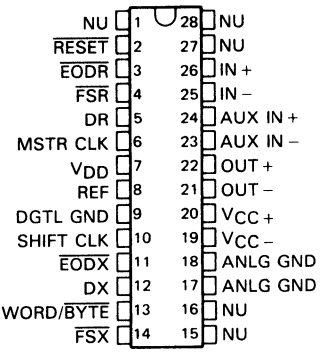
D2964, SEPTEMBER 1987—REVISED FEBRUARY 1988

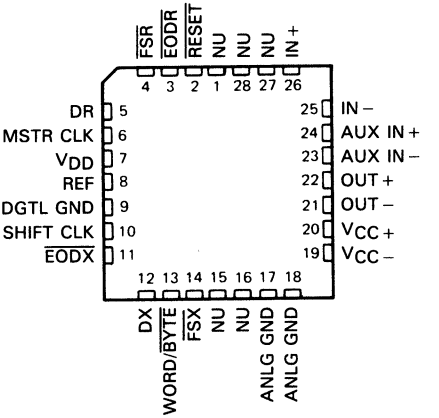
- **Advanced LinCMOS™ Silicon Gate Process Technology**
- **14-Bit Dynamic Range ADC and DAC**
- **10-Bit ADC and DAC Linearity Over Any 10-Bit Range**
- **Variable ADC and DAC Sampling Rate Up to 19,200 Samples per Second**
- **Switched-Capacitor Antialiasing Input Filter and Output-Reconstruction Filter**
- **Serial Port for Direct Interface to TMS32011, TMS320C17, TMS32020, and TMS320C25 Digital Processors**
- **Synchronous or Asynchronous ADC and DAC Conversion Rates with Programmable Incremental ADC and DAC Conversion Timing Adjustments**
- **Serial Port Interface to SN74299 Serial-to-Parallel Shift Register for Parallel Interface to TMS32010, TMS320C15, or Other Digital Processors**

PART NUMBER	DESCRIPTION
TLC32040	Analog Interface Circuit with internal reference. Also a plug-in replacement for TLC32041.
TLC32041	Analog Interface Circuit without internal reference.

N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NU—Nonusable; no external connection should be made to these pins.

description

The TLC32040 and TLC32041 are complete analog-to-digital and digital-to-analog input/output systems, each on a single monolithic CMOS chip. This device integrates a bandpass switched-capacitor antialiasing input filter, a 14-bit-resolution A/D converter, four microprocessor-compatible serial port modes, a 14-bit-resolution D/A converter, and a low-pass switched-capacitor output-reconstruction filter. The device offers numerous combinations of Master Clock input frequencies and conversion/sampling rates, which can be changed via digital processor control.

Typical applications for this IC include modems (7.2-, 8-, 9.6-, 14.4-, and 19.2-kHz sampling rate), analog interface for digital signal processors (DSPs), speech recognition/storage systems, industrial process control, biomedical instrumentation, acoustical signal processing, spectral analysis, data acquisition, and instrumentation recorders. Four serial modes, which allow direct interface to the TMS32011, TMS320C17, TMS32020, and TMS320C25 digital signal processors, are provided. Also, when the transmit and receive sections of the Analog Interface Circuit (AIC) are operating synchronously, it will interface to two SN74299 serial-to-parallel shift registers. These serial-to-parallel shift registers can then interface in parallel to the

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description (continued)

TMS32010, TMS320C15, other digital signal processors, or external FIFO circuitry. Output data pulses are emitted to inform the processor that data transmission is complete or to allow the DSP to differentiate between two transmitted bytes. A flexible control scheme is provided so that the functions of the IC can be selected and adjusted coincidentally with signal processing via software control.

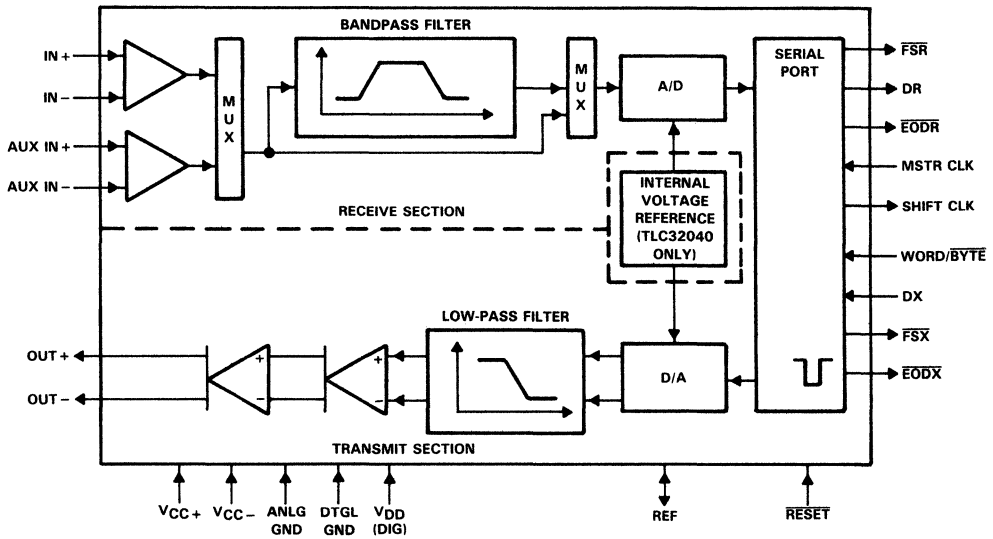
The antialiasing input filter comprises seventh-order and fourth-order CC-type (Chebyshev/elliptic transitional) low-pass and high-pass filters, respectively, and a fourth-order equalizer. The input filter is implemented in switched-capacitor technology and is preceded by a continuous time filter to eliminate any possibility of aliasing caused by sampled data filtering. When no filtering is desired, the entire composite filter can be switched out of the signal path. A selectable, auxiliary, differential analog input is provided for applications where more than one analog input is required.

The A/D and D/A converters each have 14 bits of resolution with 10 bits of integral linearity guaranteed over any 10-bit range. The A/D and D/A architectures guarantee no missing codes and monotonic operation. An internal voltage reference is provided on the TLC32040 to ease the design task and to provide complete control over the performance of the IC. The internal voltage reference is brought out to a pin and is available to the designer. Separate analog and digital voltage supplies and grounds are provided to minimize noise and ensure a wide dynamic range. Also, the analog circuit path contains only differential circuitry to keep noise to an absolute minimum. The only exception is the DAC sample-and-hold, which utilizes pseudo-differential circuitry.

The output-reconstruction filter is a seventh-order CC-type (Chebyshev/elliptic transitional low-pass filter with a fourth-order equalizer) and is implemented in switched-capacitor technology. This filter is followed by a continuous-time filter to eliminate images of the digitally encoded signal.

The TLC32040I and TLC32041I are characterized for operation from −40°C to 85°C, and the TLC32040C and TLC32041C are characterized for operation from 0°C to 70°C.

functional block diagram



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PRINCIPLES OF OPERATION

analog input

Two sets of analog inputs are provided. Normally, the IN+ and IN− input set is used; however, the auxiliary input set, AUX IN+ and AUX IN−, can be used if a second input is required. Each input set can be operated in either differential or single-ended modes, since sufficient common-mode range and rejection are provided. The gain for the IN+, IN−, AUX IN+, and AUX IN− inputs can be programmed to be either 1, 2, or 4 (see Table 2). Either input circuit can be selected via software control. It is important to note that a wide dynamic range is assured by the differential internal analog architecture and by the separate analog and digital voltage supplies and grounds.

A/D bandpass filter, A/D bandpass filter clocking, and A/D conversion timing

The A/D bandpass filter can be selected or bypassed via software control. The frequency response of this filter is presented in the following pages. This response results when the switched-capacitor filter clock frequency is 288 kHz. Several possible options can be used to attain a 288-kHz switched-capacitor filter clock. When the filter clock frequency is not 288 kHz, the filter transfer function is frequency-scaled by the ratio of the actual clock frequency to 288 kHz. The low-frequency roll-off of the high-pass section is 300 Hz. However, the high-pass section low-frequency roll-off can be changed to 200 Hz with a metal-mask option.

The Internal Timing Configuration and AIC DX Data Word Format sections of this data sheet indicate the many options for attaining a 288-kHz bandpass switched-capacitor filter clock. These sections indicate that the RX Counter A can be programmed to give a 288-kHz bandpass switched-capacitor filter clock for several Master Clock input frequencies.

The A/D conversion rate is then attained by frequency-dividing the 288-kHz bandpass switched-capacitor filter clock with the RX Counter B. Thus, unwanted aliasing is prevented because the A/D conversion rate is an integral submultiple of the bandpass switched-capacitor filter sampling rate, and the two rates are synchronously locked.

A/D converter performance specifications

Fundamental performance specifications for the A/D converter circuitry are presented in the A/D converter operating characteristics section of this data sheet. The realization of the A/D converter circuitry with switched-capacitor techniques provides an inherent sample-and-hold.

analog output

The analog output circuitry is an analog output power amplifier. Both noninverting and inverting amplifier outputs are brought out of the IC. This amplifier can drive transformer hybrids or low-impedance loads directly in either a differential or single-ended configuration.

D/A low-pass filter, D/A low-pass filter clocking, and D/A conversion timing

The frequency response of this filter is presented in the following pages. This response results when the low-pass switched-capacitor filter clock frequency is 288 kHz. Like the A/D filter, the transfer function of this filter is frequency-scaled when the clock frequency is not 288 kHz. A continuous-time filter is provided on the output of the D/A low-pass filter to greatly attenuate any switched-capacitor clock feedthrough.

The D/A conversion rate is then attained by frequency-dividing the 288-kHz switched-capacitor filter clock with TX Counter B. Thus, unwanted aliasing is prevented because the D/A conversion rate is an integral submultiple of the switched-capacitor low-pass filter sampling rate, and the two rates are synchronously locked.

PRINCIPLES OF OPERATION (continued)

asynchronous versus synchronous operation

If the transmit section of the AIC (low-pass filter and DAC) and receive section (bandpass filter and ADC) are operated asynchronously, the low-pass and band-pass filter clocks are independently generated from the Master Clock signal. Also, the D/A and A/D conversion rates are independently determined. If the transmit and receive sections are operated synchronously, the low-pass filter clock drives both low-pass and bandpass filters. In synchronous operation, the A/D conversion timing is derived from, and is equal to, the D/A conversion timing. (See description of the WORD/$\overline{\text{BYTE}}$ pin in the Pin Functional Description Section.)

D/A converter performance specifications

Fundamental performance specifications for the D/A converter circuitry are presented in the D/A converter operating characteristics section of the data sheet. The D/A converter has a sample-and-hold that is realized with a switched-capacitor ladder.

system frequency response correction

Sin x/x correction circuitry is performed in digital signal processor software. The system frequency response can be corrected via DSP software to ± 0.1 dB accuracy to a band-edge of 3000 Hz for all sampling rates. This correction is accomplished with a first-order digital correction filter, which requires only seven TMS320 instruction cycles. With a 200-ns instruction cycle, seven instructions represent an overhead factor of only 1.1% and 1.3% for sampling rates of 8 and 9.6 kHz, respectively (see the sin x/x Correction Section for more details).

serial port

The serial port has four possible modes that are described in detail in the Functional Pin Description Section. These modes are briefly described below and in the Functional Description for Pin 13, WORD/$\overline{\text{BYTE}}$.

1. The transmit and receive sections are operated asynchronously, and the serial port interfaces directly with the TMS32011 and TMS320C17.
2. The transmit and receive sections are operated asynchronously, and the serial port interfaces directly with the TMS32020 and the TMS320C25.
3. The transmit and receive sections are operated synchronously, and the serial port interfaces directly with the TMS32011 and TMS320C17.
4. The transmit and receive sections are operated synchronously, and the serial port interfaces directly with the TMS32020, TMS320C25, or two SN74299 serial-to-parallel shift registers, which can then interface in parallel to the TMS32010, TMS320C15, to any other digital signal processor, or to external FIFO circuitry.

operation of TLC32040 with internal voltage reference

The internal reference of the TLC32040 eliminates the need for an external voltage reference and provides overall circuit cost reduction. Thus, the internal reference eases the design task and provides complete control over the performance of the IC. The internal reference is brought out to a pin and is available to the designer. To keep the amount of noise on the reference signal to a minimum, an external capacitor may be connected between REF and ANLG GND.

PRINCIPLES OF OPERATION (continued)

operation of TLC32040 or TLC32041 with external voltage reference

The REF pin may be driven from an external reference circuit if so desired. This external circuit must be capable of supplying 250 μA and must be adequately protected from noise such as crosstalk from the analog input.

reset

A reset function is provided to initiate serial communications between the AIC and DSP and to allow fast, cost-effective testing during manufacturing. The reset function will initialize all AIC registers, including the control register. After a negative-going pulse on the $\overline{\text{RESET}}$ pin, the AIC will be initialized. This initialization allows normal serial port communications activity to occur between AIC and DSP (see AIC DX Data Word Format section).

loopback

This feature allows the user to test the circuit remotely. In loopback, the OUT+ and OUT− pins are internally connected to the IN+ and IN− pins. Thus, the DAC bits (d15 to d2), which are transmitted to the DX pin, can be compared with the ADC bits (d15 to d2), which are received from the DR pin. An ideal comparison would be that the bits on the DR pin equal the bits on the DX pin. However, in practice there will be some difference in these bits due to the ADC and DAC output offsets.

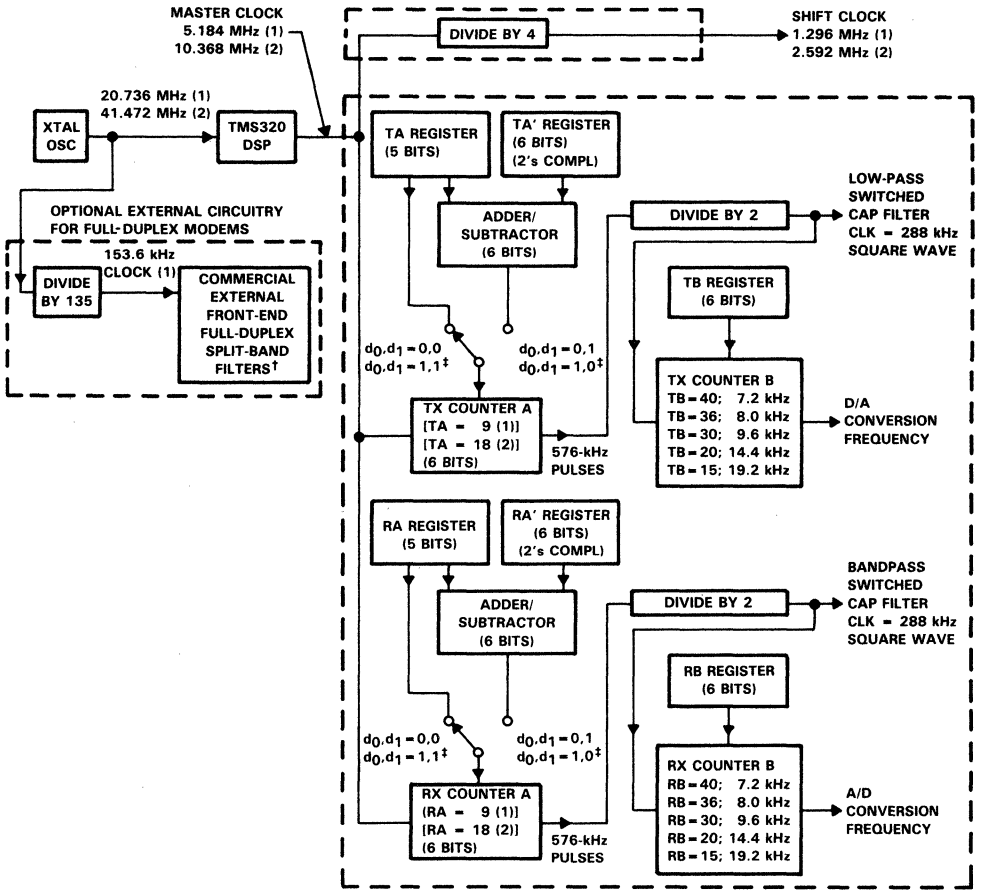
The loopback feature is implemented with digital signal processor control by transmitting the appropriate serial port bit to the control register (see AIC Data Word Format section).

PIN NAME	PIN NO.	I/O	DESCRIPTION
ANLG GND	17,18		Analog ground return for all internal analog circuits. Not internally connected to DGTL GND.
AUX IN+	24	I	Noninverting auxiliary analog input stage. This input can be switched into the bandpass filter and A/D converter path via software control. If the appropriate bit in the Control register is a 1, the auxiliary inputs will replace the IN+ and IN− inputs. If the bit is a 0, the IN+ and IN− inputs will be used (see the AIC DX Data Word Format section).
AUX IN−	23	I	Inverting auxiliary analog input (see the above AUX IN+ pin description).
DGTL GND	9		Digital ground for all internal logic circuits. Not internally connected to ANLG GND.
DR	5	O	This pin is used to transmit the ADC output bits from the AIC to the TMS320 serial port. This transmission of bits from the AIC to the TMS320 serial port is synchronized with the SHIFT CLK signal.
DX	12	I	This pin is used to receive the DAC input bits and timing and control information from the TMS320. This serial transmission from the TMS320 serial port to the AIC is synchronized with the SHIFT CLK signal.
$\overline{\text{EODR}}$	3	O	(See the WORD/$\overline{\text{BYTE}}$ pin description and the Serial Port Timing Diagram.) During the word-mode timing, this signal is a low-going pulse that occurs immediately after the 16 bits of A/D information have been transmitted from the AIC to the TMS320 serial port. This signal can be used to interrupt a microprocessor upon completion of serial communications. Also, this signal can be used to strobe and enable external serial-to-parallel shift registers, latches, or external FIFO RAM, and to facilitate parallel data bus communications between the AIC and the serial-to-parallel shift registers. During the byte-mode timing, this signal goes low after the first byte has been transmitted from the AIC to the TMS320 serial port and is kept low until the second byte has been transmitted. The TMS32011 can use this low-going signal to differentiate between the two bytes as to which is first and which is second.

PIN NAME	PIN NO.	I/O	DESCRIPTION
$\overline{EODX}$	11	O	(See the WORD/$\overline{BYTE}$ pin description and the Serial Port Timing Diagram.) During the word-mode timing, this signal is a low-going pulse that occurs immediately after the 16 bits of D/A converter and control or register information have been transmitted from the TMS320 serial port to the AIC. This signal can be used to interrupt a microprocessor upon the completion of serial communications. Also, this signal can be used to strobe and enable external serial-to-parallel shift registers, latches, or an external FIFO RAM, and to facilitate parallel data-bus communications between the AIC and the serial-to-parallel shift registers. During the byte-mode timing, this signal goes low after the first byte has been transmitted from the TMS320 serial port to the AIC and is kept low until the second byte has been transmitted. The TMS32011 can use this low-going signal to differentiate between the two bytes as to which is first and which is second.
$\overline{FSR}$	4	O	In the serial transmission modes, which are described in the WORD/$\overline{BYTE}$ pin description, the $\overline{FSR}$ pin is held low during bit transmission. When the $\overline{FSR}$ pin goes low, the TMS320 serial port will begin receiving bits from the AIC via the DR pin of the AIC. The most significant DR bit will be present on the DR pin before $\overline{FSR}$ goes low. (See Serial Port Timing and Internal Timing Configuration Diagrams.)
$\overline{FSX}$	14	O	When this pin goes low, the TMS320 serial port will begin transmitting bits to the AIC via the DX pin of the AIC. In all serial transmission modes, which are described in the WORD/$\overline{BYTE}$ pin description, the $\overline{FSX}$ pin is held low during bit transmission (see Serial Port Timing and Internal Timing Configuration Diagrams).
IN+	26	I	Noninverting input to analog input amplifier stage
IN−	25	I	Inverting input to analog input amplifier stage
MSTR CLK	6	I	The Master Clock signal is used to derive all the key logic signals of the AIC, such as the Shift Clock, the switched-capacitor filter clocks, and the A/D and D/A timing signals. The Internal Timing Configuration diagram shows how these key signals are derived. The frequencies of these key signals are synchronous submultiples of the Master Clock frequency to eliminate unwanted aliasing when the sampled analog signals are transferred between the switched-capacitor filters and the A/D and D/A converters (see the Internal Timing Configuration).
OUT+	22	O	Noninverting output of analog output power amplifier. Can drive transformer hybrids or high-impedance loads directly in either a differential or a single-ended configuration.
OUT−	21	O	Inverting output of analog output power amplifier. Functionally identical with and complementary to OUT+.
REF	8	I/O	For the TLC32040, the internal voltage reference is brought out on this pin. For the TLC32040 and TLC32041, an external voltage reference can be applied to this pin.
$\overline{RESET}$	2	I	A reset function is provided to initialize the TA, TA′, TB, RA, RA′, RB, and control registers. This reset function initiates serial communications between the AIC and DSP. The reset function will initialize all AIC registers including the control register. After a negative-going pulse on the $\overline{RESET}$ pin, the AIC registers will be initialized to provide an 8-kHz data conversion rate for a 5.184-MHz master clock input signal. The conversion rate adjust registers, TA′ and RA′, will be reset to 1. The CONTROL register bits will be reset as follows (see AIC DX Data Word Format section). d7 = 1, d6 = 1, d5 = 1, d4 = 0, d3 = 0, d2 = 1 This initialization allows normal serial-port communication to occur between AIC and DSP.
SHIFT CLK	10	O	The Shift Clock signal is obtained by dividing the Master Clock signal frequency by four. This signal is used to clock the serial data transfers of the AIC, described in the WORD/$\overline{BYTE}$ pin description below (see the Serial Port Timing and Internal Timing Configuration diagram).
V_{DD}	7		Digital supply voltage, 5 V ±5%
V_{CC+}	20		Positive analog supply voltage, 5 V ±5%
V_{CC-}	19		Negative analog supply voltage −5 V ±5%

PIN NAME	NO.	I/O	DESCRIPTION
WORD/$\overline{\text{BYTE}}$	13	I	This pin, in conjunction with a bit in the CONTROL register, is used to establish one of four serial modes. These four serial modes are described below. *AIC transmit and receive sections are operated asynchronously.* The following description applies when the AIC is configured to have asynchronous transmit and receive sections. If the appropriate data bit in the Control register is a 0 (see the AIC DX Data Word Format), the transmit and receive sections will be asynchronous. L Serial port directly interfaces with the serial port of the TMS32011 and communicates in two 8-bit bytes. The operation sequence is as follows (see Serial Port Timing diagrams). 1. The $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ pin is brought low. 2. One 8-bit byte is transmitted or one 8-bit byte is received. 3. The $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ pin is brought low. 4. The $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ pin emits a positive frame-sync pulse that is four Shift Clock cycles wide. 5. One 8-bit byte is transmitted or one 8-bit byte is received. 6. The $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ pin is brought high. 7. The $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ pin is brought high. H Serial port directly interfaces with the serial port of the TMS32020 and communicates in one 16-bit word. The operation sequence is as follows (see Serial Port Timing diagrams): 1. The $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ pin is brought low. 2. One 16-bit word is transmitted or one 16-bit word is received. 3. The $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ pin is brought high. 4. The $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ pin emits a low-going pulse. *AIC transmit and receive sections are operated synchronously.* If the appropriate data bit in the Control register is a 1, the transmit and receive sections will be configured to be synchronous. In this case, the bandpass switched-capacitor filter and the A/D conversion timing will be derived from the TX Counter A, TX Counter B, and TA, TA′, and TB registers, rather than the RX Counter A, RX Counter B, and RA, RA′, and RB registers. In this case, the AIC $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ timing will be identical during primary data communication; however, $\overline{\text{FSR}}$ will not be asserted during secondary data communication since there is no new A/D conversion result. The synchronous operation sequences are as follows (see Serial Port Timing diagrams). L Serial port directly interfaces with the serial port of the TMS32011 and communicates in two 8-bit bytes. The operation sequence is as follows (see Serial Port Timing diagrams): 1. The $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ pins are brought low. 2. One 8-bit byte is transmitted and one 8-bit byte is received. 3. The $\overline{\text{EODX}}$ and $\overline{\text{EODR}}$ pins are brought low. 4. The $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ pins emit positive frame-sync pulses that are four Shift Clock cycles wide. 5. One 8-bit byte is transmitted and one 8-bit byte is received. 6. The $\overline{\text{EODX}}$ and $\overline{\text{EODR}}$ pins are brought high. 7. The $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ pins are brought high. H Serial port directly interfaces with the serial port of the TMS32020 and communicates in one 16-bit word. The operation sequence is as follows (see Serial Port Timing diagrams): 1. The $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ pins are brought low. 2. One 16-bit word is transmitted and one 16-bit word is received. 3. The $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ pins are brought high. 4. The $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ pins emit low-going pulses. Since the transmit and receive sections of the AIC are now synchronous, the AIC serial port, with additional NOR and AND gates, will interface to two SN74299 serial-to-parallel shift registers. Interfacing the AIC to the SN74299 shift register allows the AIC to interface to an external FIFO RAM and facilitates parallel, data bus communications between the AIC and the digital signal processor. The operation sequence is the same as the above sequence (see Serial Port Timing diagrams).

INTERNAL TIMING CONFIGURATION



$$\text{SCF Clock Frequency} = \frac{\text{Master Clock Frequency}}{2 \times \text{Contents of Counter A}}$$

NOTE: Frequency 1, 20.736 MHz, is used to show how 153.6 kHz (for a commercially available modem split-band filter clock), popular speech and modem sampling signal frequencies, and an internal 288-kHz switched-capacitor filter clock can be derived synchronously and as submultiples of the crystal oscillator frequency. Since these derived frequencies are synchronous submultiples of the crystal frequency, aliasing does not occur as the sampled analog signal passes between the analog converter and switched-capacitor filter stages. Frequency 2, 41.472 MHz, is used to show that the AIC can work with high-frequency signals, which are used by high-speed digital signal processors.

†Split-band filtering can alternatively be performed after the analog input function via software in the TMS320.

‡These control bits are described in the AIC DX Data Word Format section.

explanation of internal timing configuration

All of the internal timing of the AIC is derived from the high-frequency clock signal that drives the Master Clock input pin. The Shift Clock signal, which strobes the serial port data between the AIC and DSP, is derived by dividing the Master Clock input signal frequency by four.

$$\text{SCF Clock Frequency} = \frac{\text{Master Clock Frequency}}{2 \times \text{Contents of Counter A}}$$

$$\text{Conversion Frequency} = \frac{\text{SCF Clock Frequency}}{\text{Contents of Counter B}}$$

$$\text{Shift Clock Frequency} = \frac{\text{Master CLock Frquency}}{4}$$

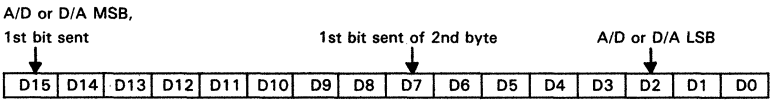
TX Counter A and TX Counter B, which are driven by the Master Clock signal, determine the D/A conversion timing. Similarly, RX Counter A and RX Counter B determine the A/D conversion timing. In order for the switched-capacitor low-pass and bandpass filters to meet their transfer function specifications, the frequency of the clock inputs of the switched-capacitor filters must be 288 kHz. If the frequencies of the clock inputs are not 288 kHz, the filter transfer function frequencies are scaled by the ratios of the clock frequencies to 288 kHz. Thus, to obtain the specified filter responses, the combination of Master Clock frequency and TX Counter A and RX Counter A values must yield 288-kHz switched-capacitor clock signals. These 288-kHz clock signals can then be divided by the TX Counter B and RX Counter B to establish the D/A and A/D conversion timings.

TX Counter A and TX Counter B are reloaded every D/A conversion period, while RX Counter A and RX Counter B are reloaded every A/D conversion period. The TX Counter B and RX Counter B are loaded with the values in the TB and RB Registers, respectively. Via software control, the TX Counter A can be loaded with either the TA Register, the TA Register less the TA' Register, or the TA Register plus the TA' Register. By selecting the TA Register less the TA' Register option, the upcoming conversion timing will occur earlier by an amount of time that equals TA' times the signal period of the Master Clock. By selecting the TA Register plus the TA' Register option, the upcoming conversion timing will occur later by an amount of time that equals TA' times the signal period of the Master Clock. Thus, the D/A conversion timing can be advanced or retarded. An identical ability to alter the A/D conversion timing is provided. In this case, however, the RX Counter A can be programmed via software control with the RA Register, the RA Register less the RA' Register, or the RA Register plus the RA' Register.

The ability to advance or retard conversion timing is particularly useful for modem applications. This feature allows controlled changes in the A/D and D/A conversion timing. This feature can be used to enhance signal-to-noise performance, to perform frequency-tracking functions, and to generate nonstandard modem frequencies.

If the transmit and receive sections are configured to be synchronous (see WORD/$\overline{\text{BYTE}}$ pin description), then both the low-pass and bandpass switched-capacitor filter clocks are derived from TX Counter A. Also, both the D/A and A/D conversion timing are derived from the TX Counter A and TX Counter B. When the transmit and receive sections are configured to be synchronous, the RX Counter A, RX Counter B, RA Register, RA' Register, and RB Registers are not used.

AIC DR or DX word bit pattern



AIC DX data word format section

d15	d14	d13	d12	d11	d10	d9	d8	d7	d6	d5	d4	d2	d1	d0	COMMENTS
primary DX serial communication protocol															
← d15 (MSB) through d2 go to the D/A converter register												→	0	0	The TX and RX Counter A's are loaded with the TA and RA register values. The TX and RX Counter B's are loaded with TB and RB register values.
← d15 (MSB) through d2 go to the D/A converter register												→	0	1	The TX and RX Counter A's are loaded with the TA + TA' and RA + RA' register values. The TX and RX Counter B's are loaded with the TB and RB register values. NOTE: d1 = 0, d0 = 1 will cause the next D/A and A/D conversion periods to be changed by the addition of TA' and RA' Master Clock cycles, in which TA' and RA' can be positive or negative or zero. Please refer to Table 1. AIC Responses to Improper Conditions.
← d15 (MSB) through d2 go to the D/A converter register												→	1	0	The TX and RX Counter A's are loaded with the TA − TA' and RA − RA' register values. The TX and RX Counter B's are loaded with the TB and RB register values. NOTE: d1 = 1, d0 = 0 will cause the next D/A and A/D conversion periods to be changed by the subtraction of TA' and RA' Master Clock cycles, in which TA' and RA' can be positive or negative or zero. Please refer to Table 1. AIC Responses to Improper Conditions.
← d15 (MSB) through d2 go to the D/A converter register												→	1	1	The TX and RX Counter A's are loaded with the TA and RA register values. The TX and RX Counter B's are loaded with the TB and RB register values. After a delay of four Shift Clock cycles, a secondary transmission will immediately follow to program the AIC to operate in the desired configuration.

NOTE: Setting the two least significant bits to 1 in the normal transmission of DAC information (Primary Communications) to the AIC will initiate Secondary Communications upon completion of the Primary Communications.

Upon completion of the Primary Communication, $\overline{FSX}$ will remain high for four SHIFT CLOCK cycles and will then go low and initiate the Secondary Communication. The timing specifications for the Primary and Secondary Communications are identical. In this manner, the Secondary Communication, if initiated, is interleaved between successive Primary Communications. This interleaving prevents the Secondary Communication from interfering with the Primary Communications and DAC timing, thus preventing the AIC from skipping a DAC output. It is important to note that in the synchronous mode, $\overline{FSR}$ will not be asserted during Secondary Communications.

secondary DX serial communication protocol

x x | ← to TA register →| x x| ← to RA register → | 0 0	d13 and d6 are MSBs (unsigned binary)
x | ← to TA′ register →| x | ← to RA′ register → | 0 1	d14 and d7 are 2's complement sign bits
x | ← to TB register →| x | ← to RB register → | 1 0	d14 and d7 are MSBs (unsigned binary)
x x x x x x x x d7 d6 d5 d4 d3 d2 1 1 | ← CONTROL REGISTER → |	d2 = 0/1 deletes/inserts the bandpass filter d3 = 0/1 disables/enables the loopback function d4 = 0/1 disables/enables the AUX IN+ and AUX IN− pins d5 = 0/1 asynchronous/synchronous transmit and receive sections d6 = 0/1 gain control bits (see Gain Control Section) d7 = 0/1 gain control bits (see Gain Control Section)

reset function

A reset function is provided to initiate serial communications between the AIC and DSP. The reset function will initialize all AIC registers, including the control register. After power has been applied to the AIC, a negative-going pulse on the $\overline{\text{RESET}}$ pin will initialize the AIC registers to provide an 8-kHz A/D and D/A conversion rate for a 5.184 MHz master clock input signal. The AIC, excepting the CONTROL register, will be initialized as follows (see AIC DX Data Word Format section):

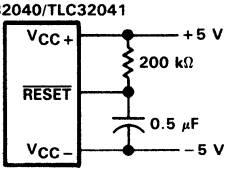
REGISTER	INITIALIZED REGISTER VALUE (HEX)
TA	9
TA′	1
TB	24
RA	9
RA′	1
RB	24

The CONTROL register bits will be reset as follows (see AIC DX Data Word Format section):

d7 = 1, d6 = 1, d5 = 1, d4 = 0, d3 = 0, d2 = 1

This initialization allows normal serial port communications to occur between AIC and DSP. If the transmit and receive sections are configured to operate synchronously and the user wishes to program different conversion rates, only the TA, TA′, and TB register need to be programmed, since both transmit and receive timing are synchronously derived from these registers (see the Pin Descriptions and AIC DX Word Format sections).

The circuit shown below will provide a reset on power-up when power is applied in the sequence given under Power-Up Sequence. The circuit depends on the power supplies' reaching their recommended values a minimum of 800 ns before the capacitor charges to 0.8 V above DGTL GND.



power-up sequence

To ensure proper operation of the AIC, and as a safeguard against latch-up, it is recommmended that a Schottky diode with a forward voltage less than or equal to 0.4 V be connected from V_{CC-} to ANLG GND (see Figure 17). In the absence of such a diode, power should be applied in the following sequence: ANLG GND and DGTL GND, V_{CC-}, then V_{CC+} and V_{DD}. Also, no input signal should be applied until after power-up.

AIC responses to improper conditions

The AIC has provisions for responding to improper conditions. These improper conditions and the response of the AIC to these conditions are presented in Table 1 below.

AIC register constraints

The following constraints are placed on the contents of the AIC registers:

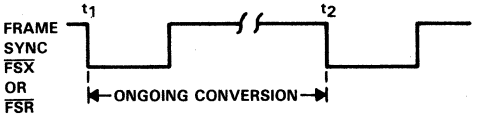
1. TA register must be > 1.
2. TA' register can be either positive, negative, or zero.
3. RA register must be > 1.
4. RA' register can be either positive, negative, or zero.
5. (TA register ± TA' register) must be > 1.
6. (RA register ± RA' register) must be > 1.
7. TB register must be > 1.

TABLE 1. AIC RESPONSES TO IMPROPER CONDITIONS

IMPROPER CONDITION	AIC RESPONSE
TA register + TA' register = 0 or 1 TA register − TA' register = 0 or 1	Reprogram TX Counter A with TA register value
TA register + TA' register < 0	MODULO 64 arithmetic is used to ensure that a positive value is loaded into the TX Counter A, i.e., TA register + TA' register + 40 HEX is loaded into TX Counter A
RA register + RA' register = 0 or 1 RA register − RA' register = 0 or 1	Reprogram RX Counter A with RA register value
RA register + RA' register = 0 or 1	MODULO 64 arithmetic is used to ensure that a positive value is loaded into RX Counter A, i.e., RA register + RA' register + 40 HEX is loaded into RX Counter A
TA register = 0 or 1 RA register = 0 or 1	AIC is shut down
TB register = 0 or 1	Reprogram TB register with 24 HEX
RB register = 0 or 1	Reprogram RB register with 24 HEX
AIC and DSP cannot communicate	Hold last DAC output

improper operation due to conversion times being too close together

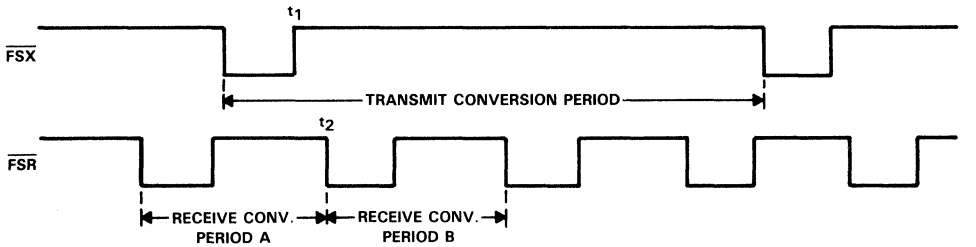
If the difference between two successive D/A conversion frame syncs is less that 1/19.2 kHz, the AIC operates improperly. In this situation, the second D/A conversion frame sync occurs too quickly and there is not enough time for the ongoing conversion to be completed. This situation can occur if the A and B registers are improperly programmed or if the A + A' register or A − A' register result is too small. When incrementally adjusting the conversion period via the A + A' register options, the designer should be very careful not to violate this requirement (see diagram below).



$t_2 - t_1 \geq 1/19.2$ kHz

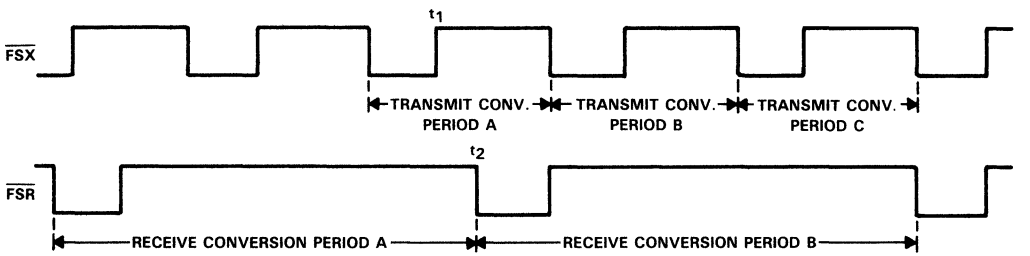
asynchronous operation — more than one receive frame sync occurring between two transmit frame syncs

When incrementally adjusting the conversion period via the A + A′ or A − A′ register options, a specific protocol is followed. The command to use the incremental conversion period adjust option is sent to the AIC during a $\overline{FSX}$ frame sync. The ongoing conversion period is then adjusted. However, either Receive Conversion Period A or B may be adjusted. For both transmit and receive conversion periods, the incremental conversion period adjustment is performed near the end of the conversion period. Therefore, if there is sufficient time between t1 and t2, the receive conversion period adjustment will be performed during Receive Conversion Period A. Otherwise, the adjustment will be performed during Receive Conversion Period B. The adjustment command only adjusts one transmit conversion period and one receive conversion period. To adjust another pair of transmit and receive conversion periods, another command must be issued during a subsequent $\overline{FSX}$ frame (see figure below).



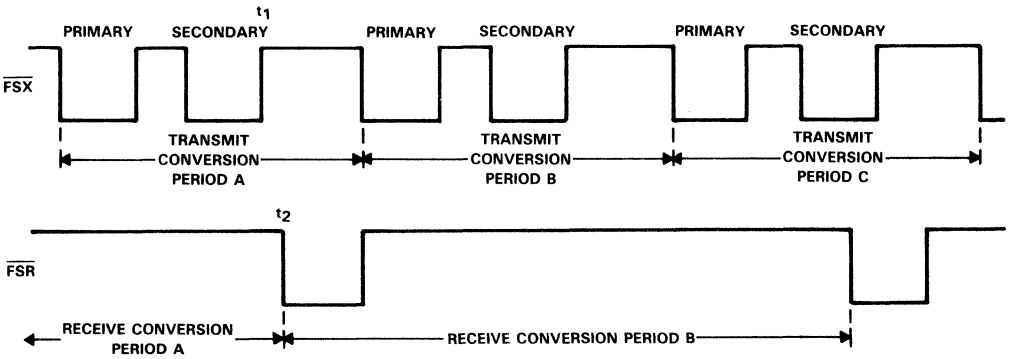
asynchronous operation — more than one transmit frame sync occurring between two receive frame syncs

When incrementally adjusting the conversion period via the A + A′ or A − A′ register options, a specific protocol is followed. For both transmit and receive conversion periods, the incremental conversion period adjustment is performed near the end of the conversion period. The command to use the incremental conversion period adjust options is sent to the AIC during a $\overline{FSX}$ frame sync. The ongoing transmit conversion period is then adjusted. However, three possibilities exist for the receive conversion period adjustment in the diagram as shown in the figure below. If the adjustment command is issued during Transmit Conversion Period A, Receive Conversion Period A will be adjusted if there is sufficient time between t1 and t2. Or, if there is not sufficient time between t1 and t2, Receive Conversion Period B will be adjusted. Or, the receive portion of an adjustment command may be ignored if the adjustment command is sent during a receive conversion period, which is already being or will be adjusted due to a prior adjustment command. For example, if adjustment commands are issued during Transmit Conversion Periods A, B, and C, the first two commands may cause Receive Conversion Periods A and B to be adjusted, while the third receive adjustment command is ignored. The third adjustment command is ignored since it was issued during Receive Conversion Period B, which already will be adjusted via the Transmit Conversion Period B adjustment command.



asynchronous operation — more than one set of primary and secondary DX serial communication occurring between two receive frame sync (see AIC DX Data Word Format section)

The TA, TA', TB, and control register information that is transmitted in the secondary communications is always accepted and is applied during the ongoing transmit conversion period. If there is sufficient time between t1 and t2, the TA, RA', and RB register information, which is sent during Transmit Conversion Period A, will be applied to Receive Conversion Period A. Otherwise, this information will be applied during Receive Conversion Period B. If RA, RA', and RB register information has already been received and is being applied during an ongoing conversion period, any subsequent RA, RA', or RB information that is received during this receive conversion period will be disregarded (see diagram below).



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1)	−0.3 V to 15 V
Supply voltage, V_{DD}	−0.3 V to 15 V
Output voltage, V_O	−0.3 V to 15 V
Input voltage, V_I	−0.3 V to 15 V
Digital ground voltage	−0.3 V to 15 V
Operating free-air temperature range: TLC32040I, TLC32041I	−40°C to 85°C
TLC32040C, TLC32041C	0°C to 70°C
Storage temperature range	−65°C to 150°C
Case temperature for 10 seconds: FN package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package	260°C

NOTE 1: Voltage values for maximum ratings are with respect to VCC−.

recommended operating conditions

PARAMETER		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+} (see Note 2)		4.75	5	5.25	V
Supply voltage, V_{CC-} (see Note 2)		−4.75	−5	−5.25	V
Digital supply voltage, V_{DD} (see Note 2)		4.75	5	5.25	V
Digital ground voltage with respect to ANLG GND, DGTL GND			0		V
Reference input voltage, $V_{ref(ext)}$ (see Note 2)		2		4	V
High-level input voltage, V_{IH}		2		$V_{DD}+0.3$	V
Low-level input voltage, V_{IL} (see Note 3)		−0.3		0.8	V
Load resistance at OUT+ and/or OUT−, R_L		300			Ω
Load capacitance at OUT+ and/or OUT−, C_L				100	pF
MSTR CLK frequency (see Note 4)		0.075	5	10.368	MHz
Analog input amplifier common mode input voltage (see Note 5)				±1.5	V
A/D or D/A conversion rate				19.2	kHz
Operating free-air temperature, T_A	TLC32040I, TLC32041I	−40		85	°C
	TLC32040C, TLC32041C	0		70	

NOTES: 2. Voltages at analog inputs and outputs, REF, V_{CC+}, and V_{CC-}, are with respect to the ANLG GND terminal. Voltages at digital inputs and outputs and V_{DD} are with respect to the DGTL GND terminal.
3. The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels and temperature only.
4. The bandpass and low-pass switched-capacitor filter response specifications apply only when the switched-capacitor clock frequency is 288 kHz. For switched-capacitor filter clocks at frequencies other than 288 kHz, the filter response is shifted by the ratio of switched-capacitor filter clock frequency to 288 kHz.
5. This range applies when (IN+ − IN−) or (AUX+ − AUX−) equals ±6 V.

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{DD} = 5 V (unless otherwise noted)

total device, MSTR CLK frequency = 5.184 MHz, outputs not loaded

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	V_{DD} = 4.75 V, I_{OH} = −300 μA	2.4			V
V_{OL}	Low-level output voltage	V_{DD} = 4.75 V, I_{OL} = 2 mA			0.4	V
I_{CC+}	Supply current from V_{CC+}				25	mA
I_{CC-}	Supply current from V_{CC-}				−25	mA
I_{DD}	Supply current from V_{DD}	$f_{MSTR\ CLK}$ = 10.368 MHz			7	mA
V_{ref}	Internal reference output voltage		3		3.2	V
αV_{ref}	Temperature coefficient of internal reference voltage				100	ppm/°C
r_o	Output resistance at REF			100		kΩ

receive amplifier input

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
	A/D converter offset error (filters bypassed)			10	50	mV
	A/D converter offset error (filters in)			10	50	mV
CMRR	Common-mode rejection ratio at IN+, IN−, or AUX+, AUX−	See Note 6		55		dB
r_I	Input resistance at IN+, IN− or AUX IN+, AUX IN−, REF			100		kΩ

transmit filter output

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OO}	Output offset voltage at OUT+ or OUT− (single-ended relative to ANLG GND)			15	50	mV
V_{OM}	Maximum peak output voltage swing across R_L at OUT+ or OUT− (single-ended)	$R_L \geq 300\ \Omega$, Offset voltage = 0	±3			V
V_{OM}	Maximum peak output voltage swing between OUT+ and OUT− (differential output)	$R_L \geq 600\ \Omega$	±6			V

†All typical values are at T_A = 25°C.

NOTE 6: The test condition is a 0-dBm, 1-kHz input signal with an 8-kHz conversion rate.

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{DD} = 5 V (unless otherwise noted)

specific modem specifications, SCF clock frequency = 288 kHz

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Attenuation of second harmonic of A/D input signal	single-ended	V_{in} = −0.1 dB to −30 dB referred to V_{ref}, See Note 7	65	70		dB
	differential		65	70		
Attenuation of third and higher harmonics of A/D input signal	single-ended	V_{in} = −0.1 dB to −30 dB referred to V_{ref}, See Note 7	60	65		dB
	differential		60	65		
Attenuation of second harmonic of D/A input signal	single-ended	V_{in} = −0 dB to −30 dB referred to V_{ref}, See Note 7	65	70		dB
	differential		65	70		
Attenuation of third and higher harmonics of D/A input signal	single-ended	V_{in} = −0 dB to −30 dB referred to V_{ref}, See Note 7	60	65		dB
	differential		60	65		

gain and dynamic range

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Absolute transmit gain tracking error while transmitting into 600 Ω (see Note 8)	−48 dB to 0 dB signal range (0 dB relative to V_{ref})		±0.05	±0.15	dB
Absolute receive gain tracking error (see Note 8)	−48 dB to 0 dB signal range (0 dB relative to V_{ref})		±0.05	±0.15	dB

power supply rejection and crosstalk attenuation

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{CC+} or V_{CC-} supply voltage rejection ratio, receive channel	f = 0 to 30 kHz	Idle channel, supply signal at 200 mV p-p measured at DR (ADC output)		30		dB
	f = 30 kHz to 50 kHz			45		
V_{CC+} or V_{CC-} supply voltage rejection ratio, transmit channel (single-ended)	f = 0 to 30 kHz	Idle channel, supply signal at 200 mV p-p measured at OUT+		30		dB
	f = 30 kHz to 50 kHz			45		
Crosstalk attenuation, transmit-to-receive (single-ended)				80		dB

†All typical values are at T_A = 25°C.

NOTES: 7. The test condition is a 1-kHz input signal with an 8-kHz conversion rate. The load impedance for the DAC is 600 Ω.
8. Gain tracking is relative to the absolute gain at 1-kHz and 0 dB (0 dB relative to V_{ref}).

delay distortion, SCF clock frequency = 288 kHz ±2%, input (IN+ – IN–) is ±3-V sinewave

Please refer to filter response graphs for delay distortion specifications.

bandpass filter transfer function with 300-Hz high-pass roll-off (see curves), SCF clock frequency = 288 kHz ±2%, input (IN+ – IN–) is a ±3-V sinewave (see Note 9)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Gain relative to gain at 1 kHz	Input signal reference is 0 dB	f = 100 Hz		–45	dB
		f = 150 Hz		–33	
		300 Hz ≤ f ≤ 3.4 kHz	–0.5	0.5	
		f = 4 kHz		–16	
		f ≥ 4.6 kHz		–60	

bandpass filter transfer function with 200-Hz high-pass roll-off (see curves), SCF clock frequency = 288 kHz ±2%, input (IN+ – IN–) is a ±3-V sinewave (see Note 9)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Gain relative to gain at 1 kHz	Input signal reference is 0 dB	f = 100 Hz		–37	dB
		f = 150 Hz		–12	
		300 Hz ≤ f ≤ 3.4 kHz	–0.5	0.5	
		f = 4 kHz		–16	
		f ≥ 4.6 kHz		–60	

low-pass filter transfer function, SCF clock frequency = 288 kHz ±2% (see Note 9)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Gain relative to gain at 1 kHz	Output signal reference is 0 dB	f ≤ 3.4 kHz	–0.5	0.5	dB
		f = 3.6 kHz		–6	
		f = 4 kHz		–30	
		f ≥ 4.4 kHz		–60	

serial port

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –300 μA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.4	V
I_I	Input current				±10	μA
C_I	Input capacitance			15		pF
C_O	Output capacitance			15		pF

† All typical values are at T_A = 25°C.

NOTE 9: The above filter specifications are guaranteed for a switched-capacitor filter clock range of 288 kHz ±2%. For switched-capacitor filter clocks at frequencies other than 288 kHz ±2%, the filter response is shifted by the ratio of switched-capacitor filter clock frequency to 288 kHz.

operating characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{DD} = 5 V

A/D converter (2's complement output, 14-bit resolution)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Integral nonlinearity, f = 4.5 kHz to 19.2 kHz (See Note 10)	bit 1 thru bit 10	Sixteenth full scale		± ½		bit 1
	bit 2 thru bit 11	Eighth full scale		± ½		bit 2
	bit 3 thru bit 12	Quarter full scale		± ½		bit 3
	bit 4 thru bit 13	Half full scale		± ½		bit 4
	bit 5 thru bit 14	Full scale		± ½		bit 5
Conversion rate			1		20	kHz
Signal-to-distortion ratio (V_{in} = −0.1 dB to −18 dB or −18 dB to −3 dB with gain = 4X, 0 dB relative to V_{ref})		1-kHz input signal with an 8-kHz conversion	60	65		dB
Equivalent input noise (relative to 600 Ω at the ADC input)		Inputs grounded		75		μV rms

D/A converter (2's complement input, 14-bit resolution)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Integral linearity, f = 4.5 kHz to 19.2 kHz (See Note 10)	bit 1 thru bit 10	Sixteenth full scale		± ½		bit 1
	bit 2 thru bit 11	Eighth full scale		± ½		bit 2
	bit 3 thru bit 12	Quarter full scale		± ½		bit 3
	bit 4 thru bit 13	Half full scale		± ½		bit 4
	bit 5 thru bit 14	Full scale		± ½		bit 5
Signal-to-distortion ratio (V_{in} = −0.1 dB to −18 dB, 0 dB relative to V_{ref})		1-kHz input signal into 600 Ω with an 8-kHz conversion rate	60	65		dB
Conversion time			1		20	kHz

noise (measurement includes low-pass and bandpass switched-capacitor filters)

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
Transmit noise	single-ended	DX input = 00000000000000, constant input code	200	225	μV rms
	differential		300	350	μV rms
			9		dBrnc0
Receive noise (see Note 11)		Inputs grounded, gain = 1	300	350	μV rms
			9		dBrnc0

timing requirements

serial port recommended input signals

	PARAMETER	MIN	MAX	UNIT
$t_{c(MCLK)}$	Master clock cycle time	95		ns
$t_{r(MCLK)}$	Master clock rise time		10	ns
$t_{f(MCLK)}$	Master clock fall time		10	ns
	Master clock duty cycle	42%	58%	
	$\overline{RESET}$ pulse duration (see Note 12)	800		ns
$t_{su(DX)}$	DX setup time before SCLK↓	20		ns
$t_{h(DX)}$	DX hold time after SCLK↓	$t_{c(SCLK)}/2$		ns

†All typical values are at T_A = 25°C.

NOTES: 10. Integral linearity for the A/D and D/A converters is guaranteed over the conversion frequency range of 4.5 kHz to 19.2 kHz. Over this range the slew rates of the A/D and D/A converters' sample-and-hold circuits are adequate to guarantee the above integral linearity specifications.

11. This noise is referred to the input with a buffer gain of one. If the buffer gain is two or four, the noise figure will be correspondingly reduced. The noise is computed by statistically evaluating the digital output of the A/D converter.

12. $\overline{RESET}$ pulse duration is the amount of time that the reset pin is held below 0.8 V after the power supplies have reached their recommended values.

operating characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{DD} = 5 V (continued)

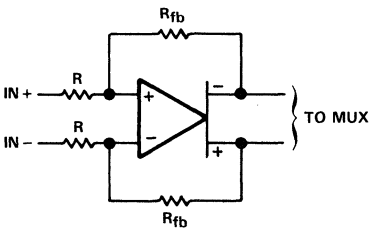
serial port — AIC output signals

	PARAMETER	MIN	MAX	UNIT
$t_{c(SCLK)}$	Shift clock (SCLK) cycle time	380		ns
$t_{f(SCLK)}$	Shift clock (SCLK) fall time		50	ns
$t_{r(SCLK)}$	Shift clock (SCLK) rise time		50	ns
	Shift clock (SCLK) duty cycle	45	55	%
$t_{d(CH-FL)}$	Delay from SCLK↑ to $\overline{FSR}/FSX$↓		90	ns
$t_{d(CH-FH)}$	Delay from SCLK↑ to $\overline{FSR}/FSX$↑		90	ns
$t_{d(CH-DR)}$	DR valid after SCLK↑		90	ns
$t_{dw(CH-EL)}$	Delay from SCLK↑ to $\overline{EODX}/\overline{EODR}$↓ in word mode		90	ns
$t_{dw(CH-EH)}$	Delay from SCLK↑ to $\overline{EODX}/\overline{EODR}$↑ in word mode		90	ns
$t_{f(EODX)}$	$\overline{EODX}$ fall time		15	ns
$t_{f(EODR)}$	$\overline{EODR}$ fall time		15	ns
$t_{db(CH-EL)}$	Delay from SCLK↑ to $\overline{EODX}/\overline{EODR}$↓ in byte mode		100	ns
$t_{db(CH-EH)}$	Delay from SCLK↑ to $\overline{EODX}/\overline{EODR}$↑ in byte mode		100	ns

TABLE 2. GAIN CONTROL TABLE
(ANALOG INPUT SIGNAL REQUIRED FOR FULL-SCALE A/D CONVERSION)

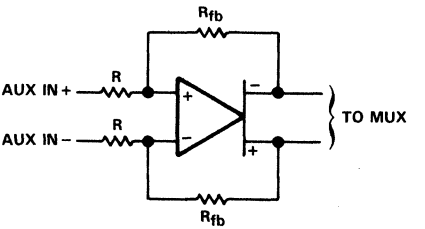
INPUT CONFIGURATIONS	CONTROL REGISTER BITS		ANALOG INPUT†	A/D CONVERSION RESULT
	d6	d7		
Differential configuration	1	1	±6 V	full-scale
Analog input = IN+ − IN−	0	0		
= AUX+ − AUX−	1	0	±3 V	full-scale
	0	1	±1.5 V	full-scale
Single-ended configuration	1	1	±3 V	half-scale
Analog input = IN+ − ANLG GND	0	0		
= AUX+ − ANLG GND	1	0	±3 V	full-scale
	0	1	±1.5 V	full-scale

† In this example, V_{ref} is assumed to be 3 V. In order to minimize distortion, it is recommended that the analog input not exceed 0.1 dB below full scale.



R_{fb} = R for d6 = 1, d7 = 1
d6 = 0, d7 = 0
R_{fb} = 2R for d6 = 1, d7 = 0
R_{fb} = 4R for d6 = 0, d7 = 1

FIGURE 1. IN+ AND IN− GAIN CONTROL CIRCUITRY



R_{fb} = R for d6 = 1, d7 = 1
d6 = 0, d7 = 0
R_{fb} = 2R for d6 = 1, d7 = 0
R_{fb} = 4R for d6 = 0, d7 = 1

FIGURE 2. AUX+ AND AUX− GAIN CONTROL CIRCUITRY

TEXAS INSTRUMENTS
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sin x/x correction section

The AIC does not have sin x/x correction circuitry after the digital-to-analog converter. Sin x/x correction can be accomplished easily and efficiently in digital signal processor (DSP) software. Excellent correction accuracy can be achieved to a band edge of 3000 Hz by using a first-order digital correction filter. The results, which are shown below, are typical of the numerical correction accuracy that can be achieved for sample rates of interest. The filter requires only seven instruction cycles per sample on the TMS320 DSPs. With a 200-ns instruction cycle, nine instructions per sample represents an overhead factor of 1.4% and 1.7% for sampling rates of 8000 Hz and 9600 Hz, respectively. This correction will add a slight amount of group delay at the upper edge of the 300–3000-Hz band.

sin x/x roll-off for a zero-order hold function

The sin x/x roll-off for the AIC DAC zero-order hold function at a band-edge frequency of 3000 Hz for the various sampling rates is shown in the table below.

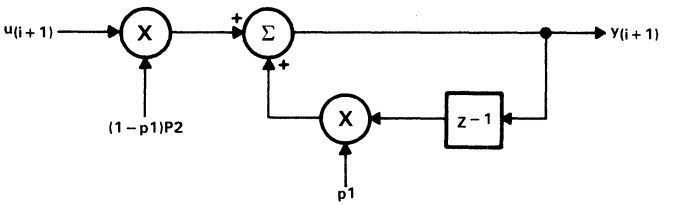
TABLE 3. sin x/x ROLL-OFF

f_s (Hz)	$20 \log \frac{\sin \pi f/f_s}{\pi f/f_s}$ (f = 3000 Hz) (dB)
7200	−2.64
8000	−2.11
9600	−1.44
14400	−0.63
19200	−0.35

Note that the actual AIC sin x/x roll-off will be slightly less than the above figures, because the AIC has less than a 100 percent duty cycle hold interval.

correction filter

To compensate for the sin x/x roll-off of the AIC, a first-order correction filter shown below, is recommended.



The difference equation for this correction filter is:

$$y_{i+1} = p2(1-p1)\,(u_{i+1}) + p1\,y_i$$

where the constant p1 determines the pole locations.

The resulting squared magnitude transfer function is:

$$|H(f)|^2 = \frac{p2^2\,(1-p1)^2}{1 - 2p1\cos(2\pi f/f_S) + p1^2}$$

correction results

Table 4 below shows the optimum p values and the corresponding correction results for 8000 Hz and 9600 Hz sampling rates.

TABLE 4

f (Hz)	ERROR (dB) f_S = 8000 Hz p1 = −0.14813 p2 = 0.9888	ERROR (dB) f_S = 9600 Hz p1 = −0.1307 p2 = 0.9951
300	−0.099	−0.043
600	−0.089	−0.043
900	−0.054	0
1200	−0.002	0
1500	0.041	0
1800	0.079	0.043
2100	0.100	0.043
2400	0.091	0.043
2700	−0.043	0
3000	−0.102	−0.043

TMS320 software requirements

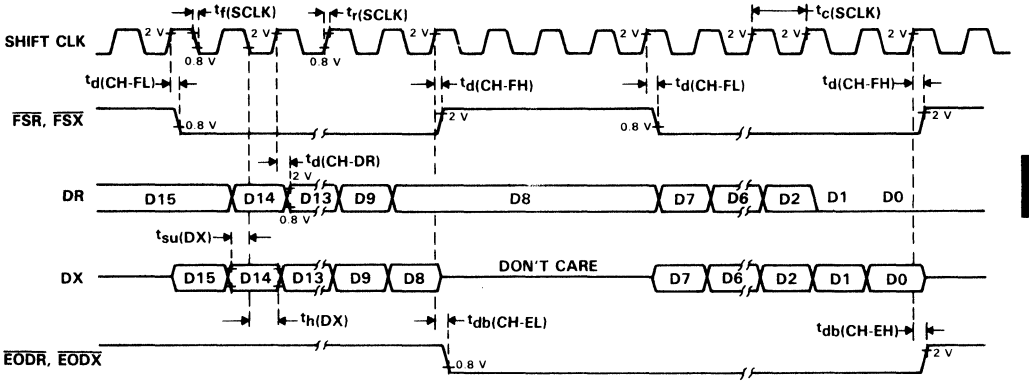
The digital correction filter equation can be written in state variable form as follows:

$$Y = k1Y + k2U$$

where k1 equals p1 (from the preceding page), k2 equals (1 − p1)p2 (from the preceding page), Y is the filter state, and U is the next I/O sample. The coefficients k1 and k2 must be represented as 16-bit integers. The SACH instruction (with the proper shift) will yield the correct result. With the assumption that the TMS320 processor page pointer and memory configuration are properly initialized, the equation can be executed in seven instructions or seven cycles with the following program:

```
ZAC
LT K2
MPY U
LTA K1
MPY Y
APAC
SACH (dma), (shift)
```

byte-mode timing



word-mode timing

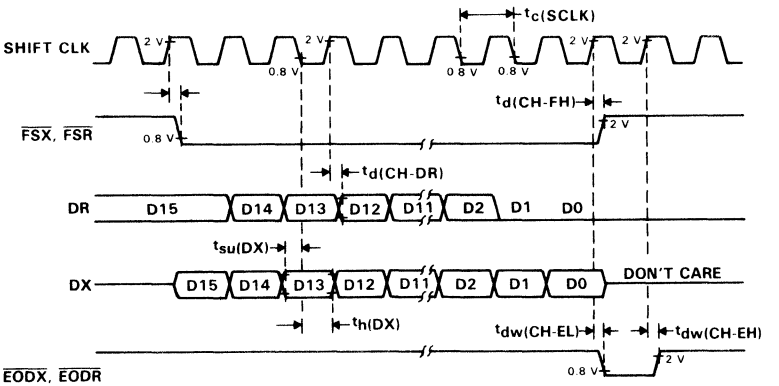


FIGURE 3. SERIAL PORT TIMING

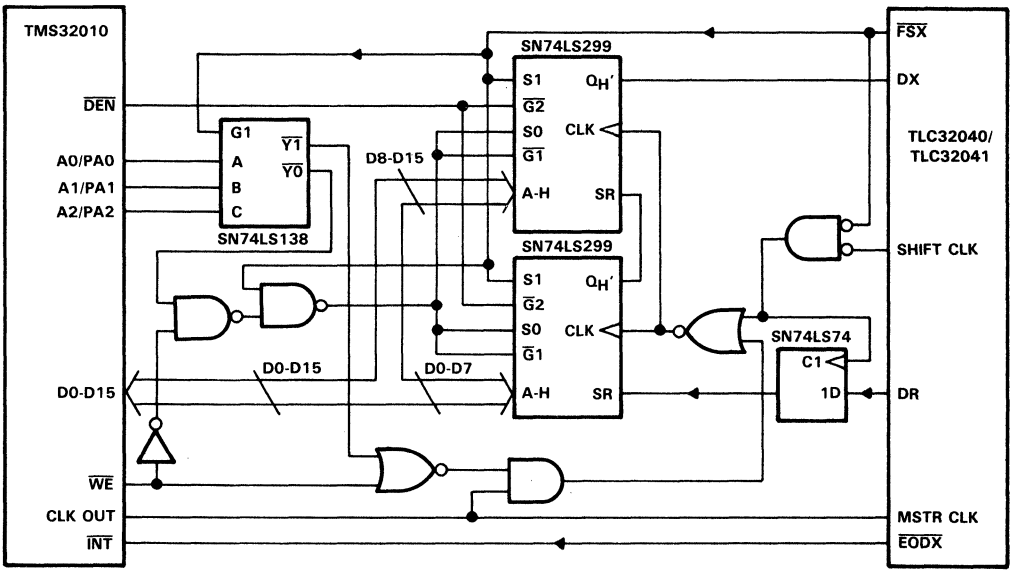
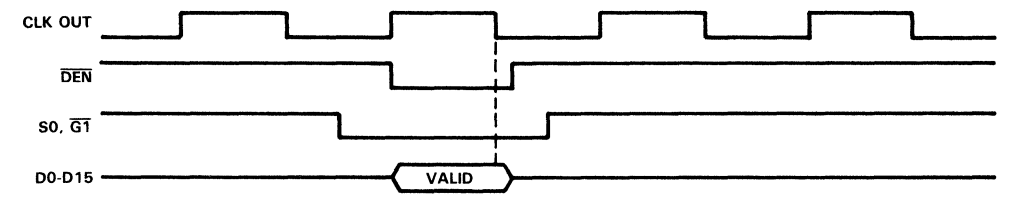


FIGURE 4. TMS32010-TLC32040/TLC32041 INTERFACE CIRCUIT

in instruction timing



out instruction timing

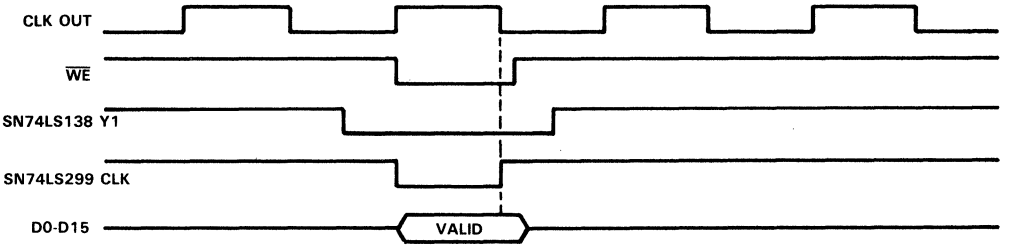
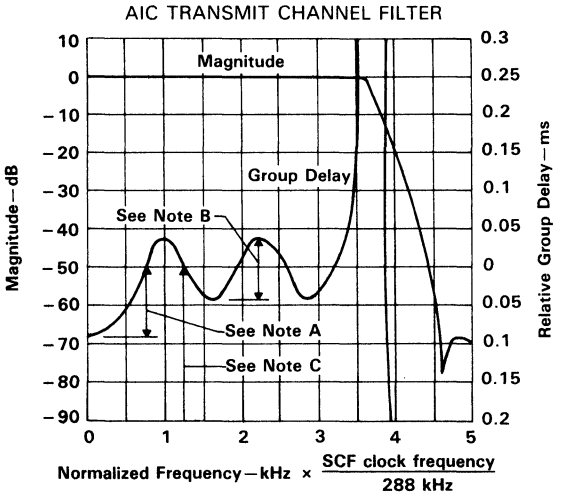


FIGURE 5. TMS32010-TLC32040/TLC32041 INTERFACE TIMING

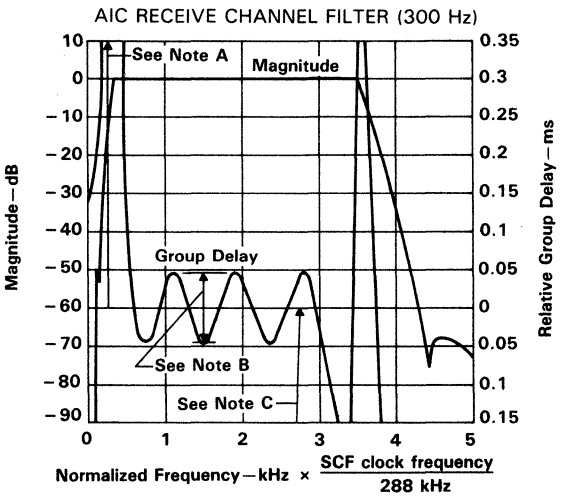
TYPICAL CHARACTERISTICS



NOTES: A. Maximum relative delay (0 Hz to 600 Hz) = 125 μs.
B. Maximum relative delay (600 Hz to 3000 hz) = ±50 μs.
C. Absolute delay (600 Hz to 3000 Hz) = 700 μs.
D. Test conditions are V_{CC+}, V_{CC-}, and V_{DD} within recommended operating conditions, SCF clock f = 288 kHz ±2%, input = ±3-V sinewave, and T_A = 25°C.

FIGURE 6

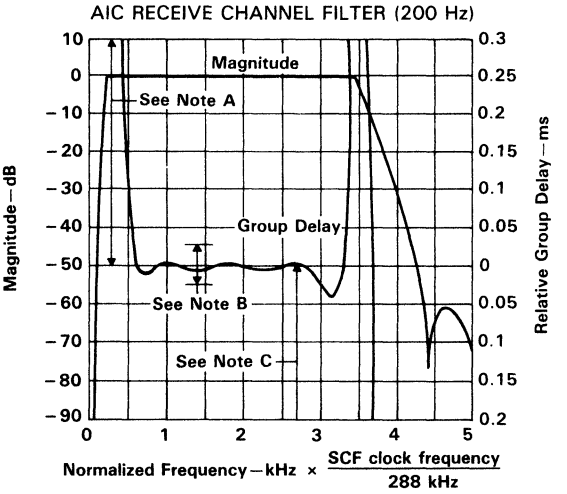
TYPICAL CHARACTERISTICS



NOTES: A. Maximum relative delay (200 Hz to 600 Hz) = 3350 μs.
B. Maximum relative delay (600 Hz to 3000 Hz) = ±50 μs.
C. Absolute delay (600 Hz to 3000 Hz) = 1230 μs
D. Test conditions are V_{CC+}, V_{CC-}, and V_{DD} within recommended operating conditions, SCF clock f = 288 kHz ±2%, input = ±3-V sinewave, and T_A = 25°C.

FIGURE 7

TYPICAL CHARACTERISTICS



NOTES: A. Maximum relative delay (200 Hz to 600 Hz) = 3350 μs.
B. Maximum relative delay (600 Hz to 3000 Hz) = ±50 μs.
C. Absolute delay (600 Hz to 3000 Hz) = 1080 μs.
D. Test conditions are V_{CC+}, V_{CC-}, and V_{DD} within recommended operating conditions, SCF clock f = 288 kHz ±2%, input = ±3-V sinewave, and T_A = 25°C.

FIGURE 8

TYPICAL CHARACTERISTICS

A/D SIGNAL-TO-DISTORTION RATIO
vs
INPUT SIGNAL

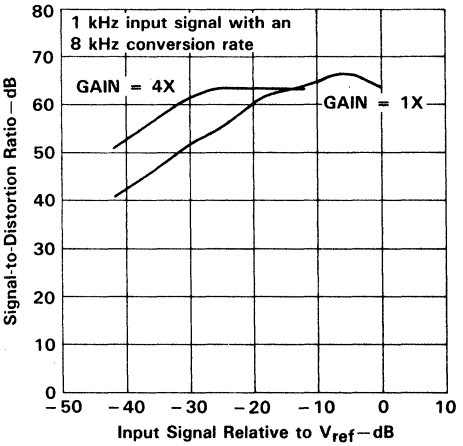


FIGURE 9

A/D GAIN TRACKING
(GAIN RELATIVE TO GAIN
AT 0 dB INPUT SIGNAL)

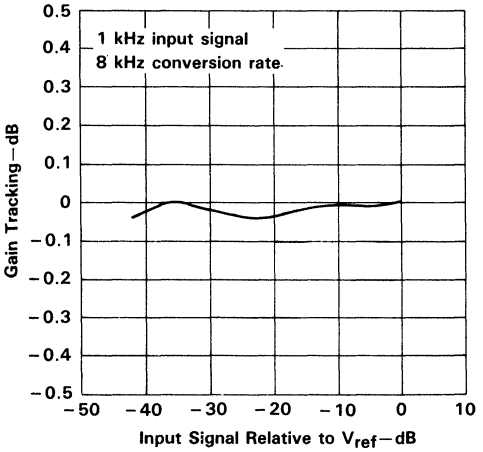


FIGURE 10

D/A CONVERTER SIGNAL-TO-DISTORTION RATIO
vs
INPUT SIGNAL

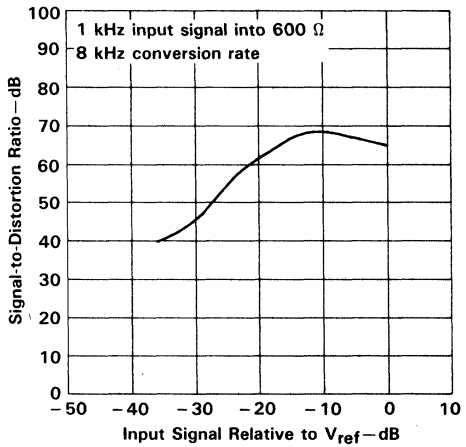


FIGURE 11

D/A GAIN TRACKING
vs
(GAIN RELATIVE TO GAIN
AT 0 dB INPUT SIGNAL)

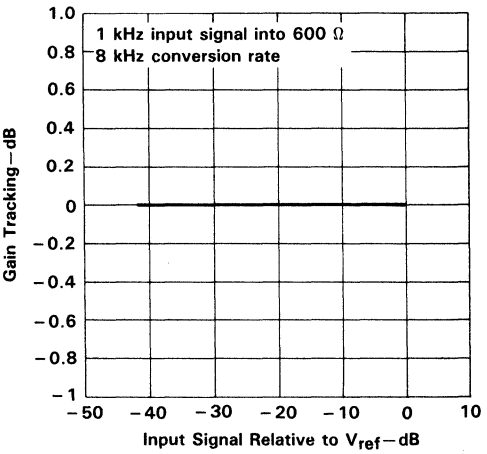


FIGURE 12

NOTE: Test conditions are V_{CC+}, V_{CC-}, and V_{OD} within recommended operating conditons, SCF clock f = 288 kHz +2%, and T_A = 25°C.

TYPICAL CHARACTERISTICS

ATTENUATION OF SECOND HARMONIC OF A/D INPUT
vs
INPUT SIGNAL

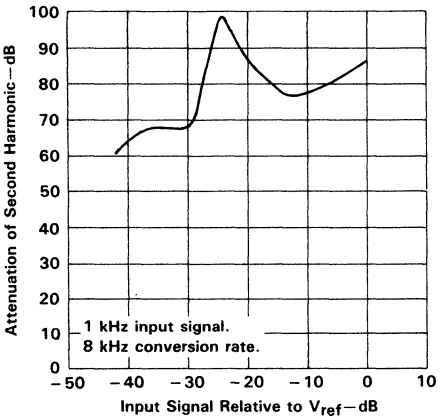


FIGURE 13

ATTENUATION OF THIRD HARMONIC OF A/D INPUT
vs
INPUT SIGNAL

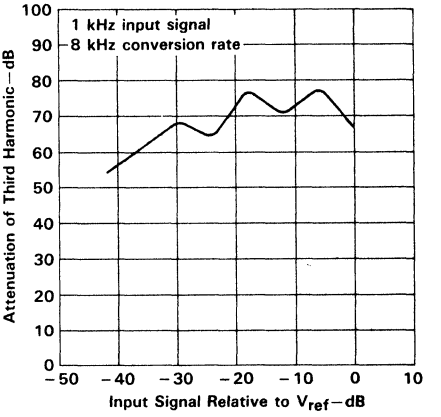


FIGURE 14

ATTENUATION OF SECOND HARMONIC OF D/A INPUT
vs
INPUT SIGNAL

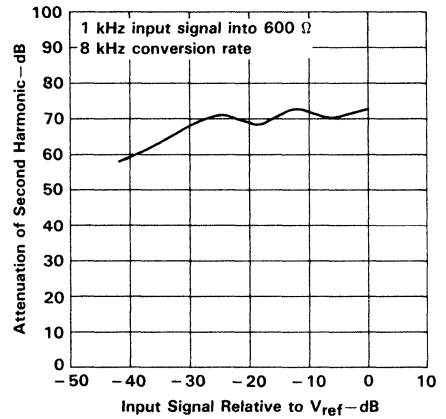


FIGURE 15

ATTENUATION OF THIRD HARMONIC OF D/A INPUT
vs
INPUT SIGNAL

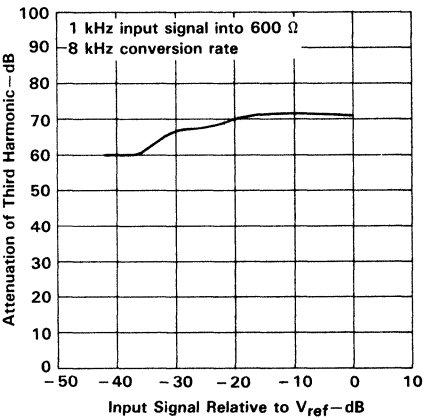
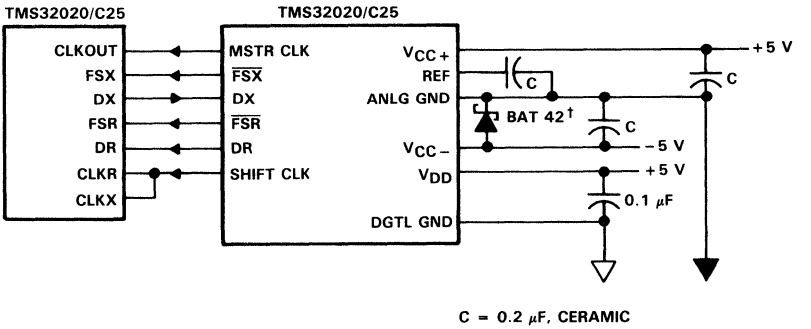


FIGURE 16

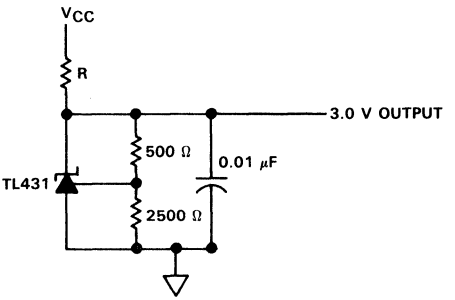
NOTE: Test conditions are V_{CC+}, V_{CC-}, and V_{OD} within recommended operating conditons, SCF clock f = 288 kHz +2%, and T_A = 25°C.

TYPICAL APPLICATION INFORMATION



C = 0.2 μF, CERAMIC

FIGURE 17. AIC INTERFACE TO THE TMS32020/C25 SHOWING DECOUPLING CAPACITORS AND SCHOTTKY DIODE†



FOR: V_{CC} = 12 V, R = 7200 Ω
V_{CC} = 10 V, R = 5600 Ω
V_{CC} = 5 V, R = 1600 Ω

FIGURE 18. EXTERNAL REFERENCE CIRCUIT FOR TLC32041

†Thomson Semiconductors

General Information 1

Telecommunications Circuits 2

Designer's Information 3

Application Reports 4

Mechanical Data 5

Contents

	Page
Guidelines for Handling Electrostatic-Discharge Sensitive Devices (ESDS) and Assemblies	3-3
Quality and Reliability Assurance	3-9

Guidelines for Handling Electrostatic-Discharge Sensitive (ESDS) Devices and Assemblies†

1.0 SCOPE

1.1 This specification establishes the requirements for methods and materials used to protect electronic devices and assemblies which are susceptible to damage or degradation from electrostatic discharge (ESD). The electrostatic charges referred to in this specification are generated and stored on surfaces of ordinary plastics, most common textile garments, ungrounded human bodies, and many other commonly used materials, not generally recognized as being electrostatic generators. The passage of these charges through an electrostatic-sensitive device may result in catastrophic failure or performance degradation of the part.

1.2 The part types (packaged or unpackaged) for which these requirements are applicable include, but are not limited to the following:

(a) All metal-oxide semiconductor (MOS) devices, e.g., CMOS, PMOS, etc.
(b) Junction field-effect transistors (JFET)
(c) Bipolar digital and linear circuits
(d) Op Amps, monolithic microcircuits with MOS compensating networks, on-board MOS capacitors, or other MOS elements
(e) Hybrid microcircuits
(f) Thin film passive devices.

1.3 Definitions

1.3.1 Conductive material: Material having a maximum surface resistivity of 10^5 Ω/square.
1.3.2 Static dissipative material: Material having surface resistivity between 10^5 and 10^9 Ω/square.
1.3.3 Antistatic material: Material having a surface resistivity between 10^9 and 10^{14} Ω/square.
1.3.4 Electrostatic discharge (ESD): A transfer of electrostatic charge between bodies at different electrostatic potentials caused by direct contact or induced by an electrostatic field.
1.3.5 Surface resistivity (generally called sheet resistance or sheet resistivity): The resistance between two electrodes forming opposite sides of the square. It is measured in ohms per square, and the size of the square is immaterial.
1.3.6 Volume resistivity: Also referred to as bulk resistivity. It is normally determined by measuring the resistance (R) of a square of material (surface resistivity) and multiplying this value by the thickness (T).
1.3.7 Ionizer: Equipment that generates positive and negative ions, either by electrostatic means or by means of a radioactive energy source, in an airstream, that distributes a layer of low velocity ionized air over a work area to neutralize static charges.
1.3.8 Close proximity: For the purpose of this specification 6 inches or less.
1.3.9 Magazine: A-frame slide pack or rail for dual-in-line or other semiconductor packages.
1.3.10 Static: Used in this document as a short form of electrostatic.

1.4 Device Sensitivity per Test Circuit of Method 3015, MIL-STD-883 for ICs, or Method 1020, MIL-STD-750 for Discretes

1.4.1 Devices are categorized according to their susceptibility to damage resulting from electrostatic discharge (ESD), and the type of packaging required to adequately protect them.
1.4.1.1 Device electrostatic sensitivity

Category	ESD Sensitivity (V)	Minimum Protective Packaging
1	20-2000	A conductive container or an antistatic container within an electrostatic field shielding barrier
2	> 2000	An antistatic container

†Based on TI's internal ESD specification and JEDEC publication No. 108, *Distributor Requirements for Handling Electrostatic-Discharge Sensitive (ESDS) Devices.*

1.4.2 Category "1" devices are to be identified and labeled by the device manufacturer.

1.4.3 Devices are to be protected from ESD damage from receipt at incoming inspection through assembly, test, and shipment of completed equipment.

2.0 APPLICABLE REFERENCE DOCUMENTS

2.1 The following reference documents of the latest issue in effect can provide additional information on ESD controls.

DOD-HDBK-263 Electrostatic Discharge Control Handbook for Protection
DOD-STD-1686 Electrostatic Discharge Control Program
EIA Interim Standard IS-5-A Packaging Materials Standards for ESD Sensitive Items
MIL-M-38510 Microcircuits, General Specification
MIL-STD-883 Test Methods and Procedures for Microelectronics
MIL-S-19491 Semiconductor Devices, Packaging of
MIL-M-55565 Microcircuits, Packaging of
NAVSEA SE 003-11-TRN-010 Electrostatic Discharge Training Manual
MIL-STD-750 Test Methods for Semiconductor Devices
TRS-3A EOS/ESD Technology Abstracts (RADC)
MIL-STD-129 Marking for Shipment and Storage
MIL-S-19500 General Specification for Semiconductor Devices

2.2 In case of conflict between requirements of this document and reference documents, this document shall have precedence.

3.0 FACILITIES FOR STATIC-FREE WORK STATION

3.1 The minimum acceptable static-free work station shall consist of the work surface covered with a static dissipative or conductive material attached to ground through a 1 MΩ ± 10% resistor and a grounding wrist strap with integral 1 MΩ ± 10% resistor for each operator. The air ionizer is recommended to provide maximum effectiveness of the static-free work station. If the air ionizer is not used, static dissipative or conductive smocks must be worn by the operators. The static dissipative or conductive smocks will provide some additional protection but are not equivalent to ionizers in improving the effectiveness of the static-free work station. If it is not possible to eliminate insulator materials at the static-free work station, the ionizer must be utilized. If the wrist strap is connected to the static dissipative mat, rather than directly to ground, it shall be connected to the same metallic button or contact used to ground the mat. Ground shall utilize earth ground, refer to Figure 1. Conductive floor tile or mats along with conductive shoes or heel straps may be used in lieu of the conductive wrist straps for nonseated personnel where the use of grounded wrist strap is hazardous or impractical. The Site Safety Engineer (or person designated by the ESD Coordinator) must review and approve all electrical connections at the static-free work station prior to its implementation.

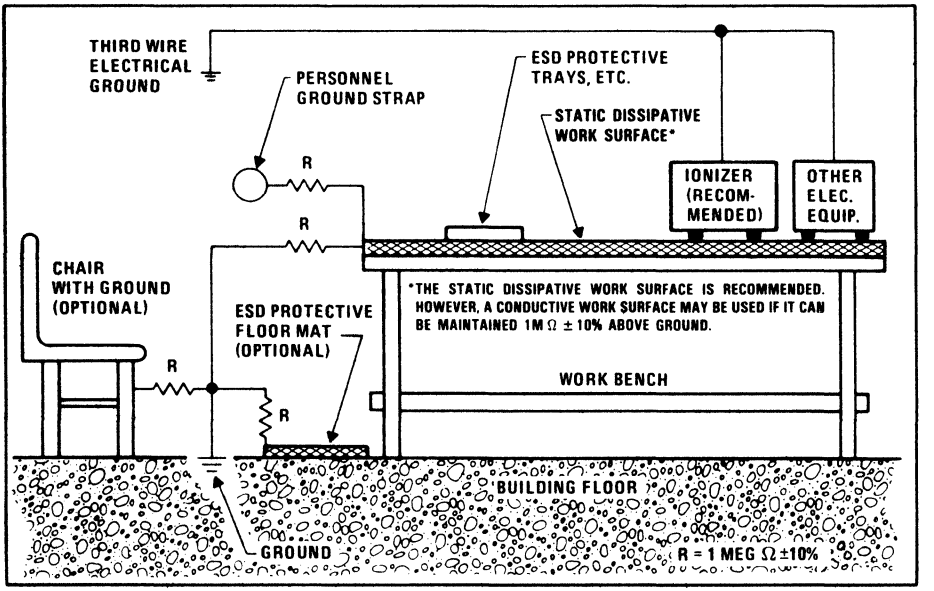
3.1.1 Air ionizer: Table ionizers shall be positioned so that the devices at the static-free work stations are within a 4-foot arc measured by a vertical line from the face of the ionizer and 45 degrees on each side of this line. The ionizer shall be aimed at the devices and operator's hands rather than at the operator. Ceiling ionizers shall be mounted within 6 feet of the work surface. Devices shall not be brought closer than 1 foot from the emitting surface of an ionizer.

3.2 General Grounding Requirements are to be in Accordance with Table I.

Table I. General Grounding Requirements

	Treated or Intrinsic Antistatic or Conductive Material	Static Dissipative Material	Grounded to Common Point
Handling Equipment/Handtools	X		
Metal Parts of Fixtures and Tools			X
Handling Trays/Tubes	X	X	
Plastic Racks/Bins	X	X	
Table Tops/Floor Mats	X	X	X*
Personnel			X Using Wrist Strap*

*With 1 ΩM ± 10% safety resistor (See Figure 1)



All electrical equipment sitting on the static dissipative work surface must be hard grounded and must be isolated from the static dissipative work surface.

NOTE: Earth ground consists of a metal pipe or rod inserted at least three (3) feet into the earth. All static-free work stations in a single building may utilize a single earth ground.

Figure 1. Static-Free Work Station

3.3 ESD Labels and Signs in Work Areas

3.3.1 ESD caution signs at work stations and work areas and labels on ESDS parts and containers shall be consistent in color, symbols, and appropriate instructions.

3.3.2 Signs shall be posted at all work stations performing any handling operations with ESDS items. These signs shall contain the following information, or its equivalent.

> **CAUTION**
>
> **STATIC CAN DAMAGE COMPONENTS**
>
> Do not handle ESDS items unless grounding wrist strap is properly worn and grounded. Do not let clothing contact or come in close proximity to ESDS items.

3.3.3 Labels shall be affixed to all containers containing ESDS items at a place readily visible and proper for the intended purpose. Additionally, labels must be consistently placed on containers and packages at a standard location to eliminate mishandling.

3.3.4 The use of ESD signs and labels, and their information content shall be the responsibility of the Area Supervisor and the ESD Coordinator to assure consistency and compatibility throughout the ESDS device routing.

3.4 Relative Humidity Control

3.4.1 Since relative humidity has a significant impact on the generation of static electricity, where possible, the work area should be maintained within the following relative humidity range: 40%-60%.

3.4.2 Where it is possible to control the relative humidity, it should be set for some value within the above range and maintained as closely as possible to avoid static voltage monitor variations.

4.0 PREPARATION FOR WORKING AT STATIC-FREE WORK STATION

4.1 A work station with a static dissipative work surface connected to ground through a 1 MΩ ± 10% resistor, a grounding wrist strap with the ground wire connected to the grounding point of the static dissipative work surface or equivalent footware and conductive flooring per paragraph 3.1, and an ionizer or a static dissipative or conductive smock constitute a static-free work station (Figure 1). An operator is properly grounded when the wrist strap is in snug (no slack) contact with the bare skin, usually positioned on the left wrist for a right-handed operator. The wrist strap, or equivalent footware per paragraph 3.1, must be worn the entire time an operator is at a static-free work station.

CAUTION
Personnel shall never be attached to ground without the presence of the 1.0 MΩ ± 10% series resistor in the ground wire.

4.2 If possible, operators should avoid touching leads or contacts even though grounded.

4.3 An operator's clothing should never make contact or come in close proximity with ESDS items. Operators must be especially careful to prevent any ESDS items (being handled) from touching their clothing. If static dissipative or conductive smocks are not used, long sleeves must be rolled up or covered with antistatic sleeve protector banded to the bare wrist which shall "cage" the sleeve at least as far up as the elbow. If static dissipative or conductive smocks are used (in lieu of air ionizers), they must completely cover long sleeves. The smock manufacturer's cleaning instructions must be followed.

4.4 Only cotton gloves, antistatic gloves, or antistatic finger cots (free of reactive elements such as chlorine, phosphorus, etc.) may be used when handling ESDS items.

4.5 Any person not properly prepared, as outlined in paragraphs 4.3 and 4.4 while at or near the work station, shall not touch or come in close proximity with any ESDS items.

4.6 It is the responsibility of the operator and the Area Supervisor to ensure that the static-free work area is clear of unnecessary static hazards, including such personal items as plastic coated cups or wrappers, plastic cosmetic bottles or boxes, combs, tissue boxes, cigarette packages, cellophane tape, and vinyl or plastic purses. All work-related items, including information sheets, fluid containers, tools, and parts carriers must be those approved by the distributor ESD Coordinator for use at the static-free work station.

5.0 GENERAL HANDLING PROCEDURES AND REQUIREMENTS

5.1 All ESDS items must be received in a closed antistatic/conductive container and must not be removed from the container except at a static-free work station. All protective folders or envelopes holding documentation (lot travelers, etc.) shall be made of nonstatic-generating material.

5.2 Each packing (outermost) container and package (internal or intermediate) shall have a brightly colored warning label (black letters on a yellow background) attached, stating the following information or equivalent:

The warning label shall be legible to normal vision at a distance of 3 feet.

5.3 ESDS items are to remain in their protective containers except when actually in work at the static-free station.

5.4 Before removing the items from their protective container, the operator should:

5.4.1 Place the container on the static dissipative work station surface (see para. 5.1)

5.4.2 Make sure the wrist strap fits snugly around the wrist and is electrically connected to the ground receptacle on the static dissipative work surface, then touch hands to the static dissipative work surface.

5.5 All operations on the items should be performed with the items in contact with the static dissipative work surface as much as possible. Do not allow conductive magazine to touch hard grounded test gear on the work surface.

5.6 In cases where it is impossible or impractical to ground the operator with a wrist strap, a conductive shoe strap may be used along with conductive tile/mats, per paragraph 3.1.

5.7 When the operator moves from any other place to the static-free station, the start-up procedure shall be the same as in paragraph 4.0.

5.8 The ionizer (if used) shall be in operation prior to presenting any ESDS items to the static-free station, and shall be in operation during the entire time period the items are at the station.

5.9 "Plastic snow" polystyrene foam, "peanuts," or other high-dielectric materials shall never come in contact with or be used around electrostatic sensitive items, unless they have been treated with an antistat (often resulting in a pink color) as evidenced by the generation of less than ± 100 volts when rubbed vigorously against any insulator.

5.10 ESDS items shall not be transported or stored in trays, tote boxes, vials, or similar containers made of untreated plastic material unless items are protectively packaged in conductive material.

6.0 PACKAGING REQUIREMENTS

6.1 Packaging of ESDS items is to be in accordance with section 1.4.1. Tape and plain plastic bags are prohibited inside the minimum protective packaging per paragraph 1.4.1.1.

6.2 Outer and inner containers are to be marked as outlined in section 5.2.

6.3 Conductive magazines/boxes may be used in lieu of conductive bags.

7.0 SPECIFIC HANDLING PROCEDURES FOR ESDS ITEMS

7.1 Stockroom Operations

7.1.1 Containers of ESDS items are not to be accepted into stock unless properly packaged and adequately identified as containing ESDS items.

7.1.2 Items may be removed from the protective container (magazine/bag, etc.) for the purpose of subdividing for order issue only by a properly grounded operator at an approved static-free station as defined in sections 3.0 and 4.0.

7.1.3 All subdivided lots must be carefully repackaged in protective containers (magazine/bag, etc.) prior to removal from the static-free work station and labeled to indicate that the package(s) contain ESDS items. If it is suspected that a ESDS item is not adequately protected, do not transfer it to another container, return it to the originator for disposition unless the originator is a Customer. In that case, the Distributor's Representative should contact the Customer and negotiate an appropriate disposition.

7.1.4 It is the responsibility of the Stockroom Supervisor to ensure that all personnel assigned to this operation are familiar with handling procedures as outlined in this specification. A copy of this specification, or an in-house procedure meeting the requirements of this specification, is to be available in the vicinity so that it is accessible to the operators. Stock handlers and all others who might have occasion to move stock are to be instructed to avoid contact with unprotected ESDS items.

7.2 Packing Operations

7.2.1 ESDS items are not to be accepted into the packing area unless they are contained in a static-protected bag or conductive container.

7.2.2 An ESDS item delivered to the packer within an approved container or bag and found to be in order regarding identification shall be packed in the standard shipping carton or other regular packaging material. Containers are to be labeled in accordance with section 5.2.

7.2.3 Any void-fillers shall be made of an approved material.

8.0 AUDIT PROVISIONS

8.1 ESD Coordinator: An ESD coordinator shall be appointed for each site to assure that the following requirements are met.

8.2 Auditing

8.2.1 Each operation handling ESDS devices shall be audited a minimum of once each quarter for compliance with all terms of this specification. Ground continuity and the presence of uncontrolled static voltages (any voltage exceeding ± 100 V) are considered critical and shall be checked more frequently as specified below.

8.2.2 Ground Continuity (minimum of once a week): Ground connections (grounding wrist strap, ground wires on cords, etc.) shall be checked for electrical continuity. The presence of a 1 MΩ ± 10% resistor in the ground connections between both the operator wrist straps to the work surface and the work surface to ground connector must be verified.

8.2.3 Grounded Conditions (minimum of once a week): A visual inspection shall be made to determine full compliance with this specification at static-free work stations during handling of ESDS items, including operator being grounded as required, ESDS items not being handled in unprotected or unauthorized areas, and no static-generating materials (except as allowed by 3.1) at the static-free work station.

8.2.4 Sleeve Protectors (minimum of once a week): A visual check shall be made to determine that each operator wearing loose-fitting or long-sleeved clothing either has sleeves properly rolled or covered with sleeve protectors properly grounded to the bare skin at the wrist. Sleeve protectors are not required if static dissipative or conductive smocks are used.

8.2.5 Static Voltage Levels (minimum of once a week): In addition to the visual inspections, an inspection using an electrostatic voltmeter shall be made to check for uncontrolled electrostatic voltages (any voltage exceeding ± 100 V) at or near electrostatic-controlled work stations. If static dissipative or conductive smocks are used, they shall also be checked to the same level.

8.2.6 Conductive Floor Tiles (minimum of once a month): Conductive floors must have a resistance of not less than 100 kΩ from any point on the tile to earth ground. Also, resistance from any point-to-point on the tile floor 3 feet apart shall be not less than 100 kΩ. The test methods to be used are ASTM-F-150-72 and NFPA 99.

8.2.7 Conductive Floor Mats (minimum of once a week): Ground connection through a 1MΩ ± 10% safety resistor shall be checked for continuity. Mat must be clean and free of tears or holes.

8.2.8 Ionizer operation (minimum of once a month): Air ionizers are to be checked for balanced ionization in accordance with manufacturer's recommendations.

8.2.9 If a noncompliant condition is found, no additional parts may be processed through that area until the noncompliant condition is corrected.

8.3 Records: Written records must be kept of all audits (paragraph 8.2) for at least 1 year.

9.0 TRAINING

9.1 It is the responsibility of the ESD coordinator to make sure that all personnel handling ESDS devices receive ESD training initially and every 12 months thereafter to maintain proficiency. Training should include static fundamentals, a review of applicable parts of this specification, and actual applications in the work area.

9.2 Training records shall be maintained for each individual. The records shall show dates of training and the topics covered.

Quality and Reliability Assurance

Texas Instruments has improved the quality and reliability of integrated circuits through routine updating of existing specifications and programs as well as advancements in materials, processes, test equipment, and test methods. Since the early sixties, these programs have provided cumulative improvements to increase average outgoing quality (AOQ) and reliability by more than an order of magnitude.

Stringent performance and manufacturing standards are defined prior to product design to assure leadership in the industry. In addition, the following product/process qualifications and evaluations are performed to assure that these standards are met on every device released to the market:

- Verification of manufacturability through testing of bar compatibility with piece parts and automated assembly techniques and equipment
- Proof of process repeatability through definition of minimum acceptable assembly and test yields
- Testing to data sheet limits through test program certification and guard bands between probe, final test, and QRA final acceptance
- Assurance of quality performance through a comprehensive statistical process control program coupled with tight product acceptance standards
- Assessment of device reliability performance through an extensive reliability test and qualification program.

Quality is . . .

a product's degree of conformance to its specified parameters. It pertains to the probability of defective units existing in a given lot when received by the user. Although zero defects is a goal, the probability of some level of defective units still exists in any lot of mass produced items. The number of defective units received by the user is a function of the average outgoing quality (AOQ) achieved by the supplier.

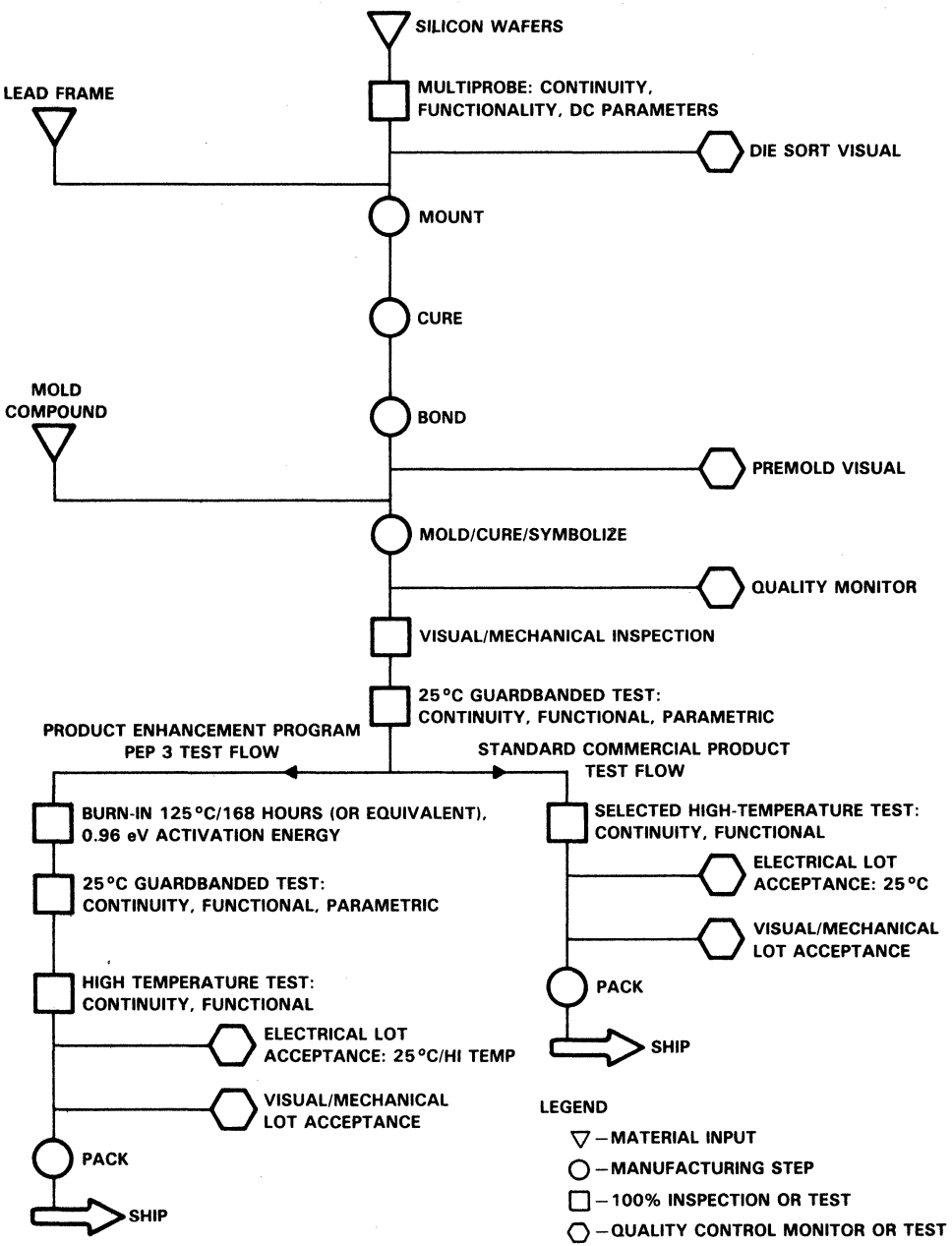
Reliability is . . .

a measurement of how well an initially good product will perform over time to its specified characteristics. Semiconductor failures occur primarily during the early-life phase of operation. A continually diminishing failure rate can be expected until the wear-out phases is eventually reached. System reliability is improved if these potential early-life failures are removed.

The following process flows for plastic and ceramic packages show the extensive efforts used to maintain high quality and reliability standards for Telecommunication products from Texas Instruments. These flows apply to TCM prefix devices only.

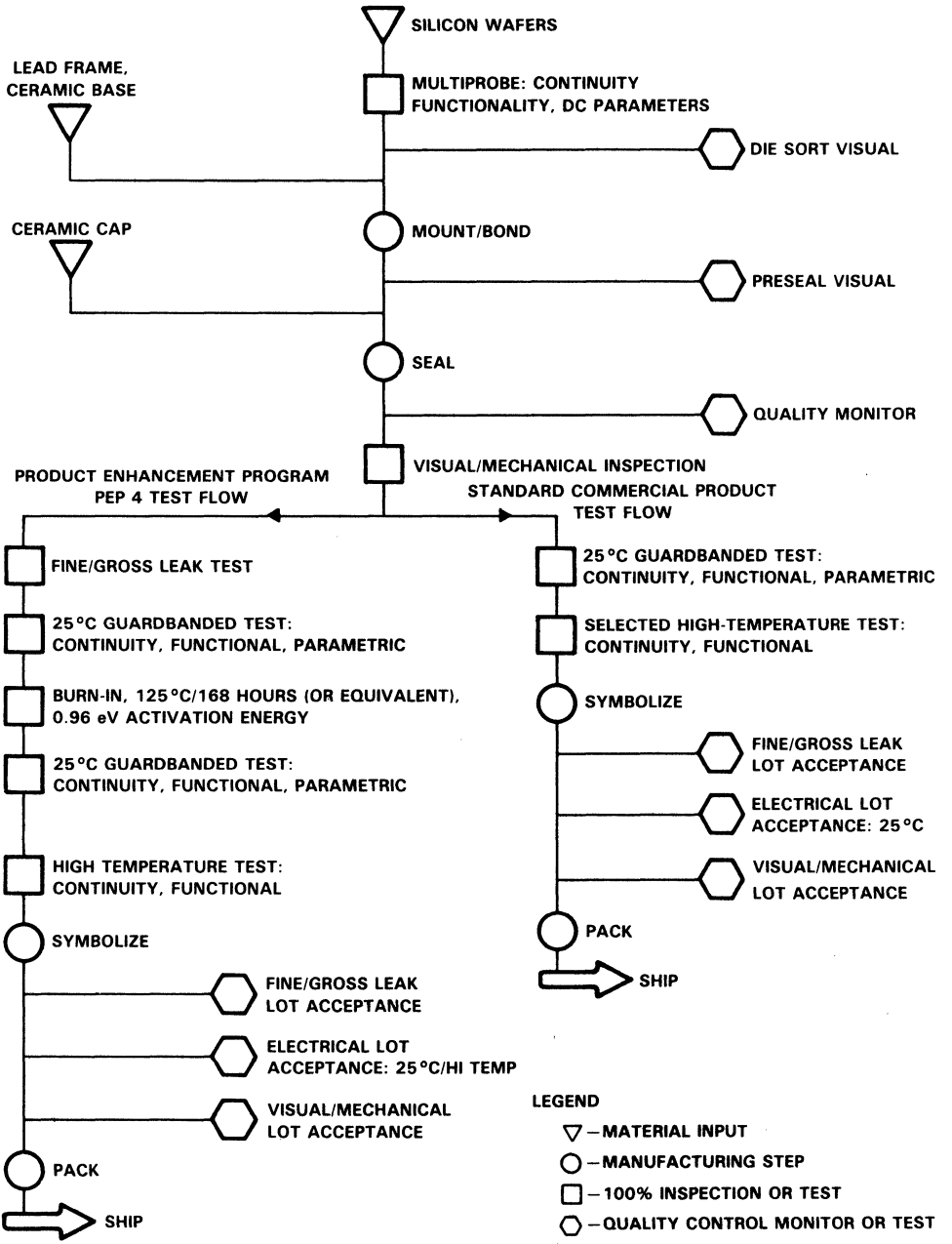
TELECOMMUNICATION PRODUCTS PROCESS FLOW†

PLASTIC PACKAGE



† Applies to TCM prefix devices only.

TELECOMMUNICATION PRODUCTS PROCESS FLOW†
CERAMIC PACKAGE



† Applies to TCM prefix devices only.

General Information 1

Telecommunications Circuits 2

Designer's Information 3

Application Reports 4

Mechanical Data 5

Contents

	Page
FSK Modems	4-3
TCM2203 Line Interface Circuits and TCM2222 HDB3/AMI Encoder/Decoder	4-21
TISP Series Transient Suppressors	4-37
Designing with the TCM1500 Bell Tone Ringer/Detector Family	4-73
Subscriber Line Control Circuits	4-101

FSK Modems

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes in the devices or the device specifications identified in this publication without notice. TI advises its customers to obtain the latest version of device specifications to verify, before placing orders, that the information being relied upon by the customer is current.

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Contents

	Page
Basic Principles of Modem Operation	4-7
Introduction to the TCM3105	4-8
Modes of Operation of the TCM3105	4-9
Architectural Description of the TCM3105	4-10
Transmitter	4-12
Receiver	4-12
Carrier Detect	4-13
Timing and Control	4-13
Description of the Line Interface	4-13
FCC Registration	4-13
Two-to-Four Wire Converter Operation	4-14
Description of the Carrier Detect Adjustment	4-16
Description of the Receive Bias Adjustment	4-17
Output Jitter Measurement	4-19
Conclusion	4-20

List of Illustrations

Figure		*Page*
1	Typical Modem System Configuration	4-7
2	TCM3105 Pinout	4-9
3	Bell 202 and CCITT V.23 Channel Assignments	4-9
4	TCM3105 Functional Block Diagram	4-11
5	Typical Application Circuit	4-15
6	Simplified Two-to-Four Wire Converter	4-16
7	CDL Bias Level vs Carrier Detect Threshold	4-17
8	RXB Bias Level vs RXD Bias Distortion	4-18
9	Loopback Circuit Diagram	4-18
10	Jitter Timing Diagram	4-19

List of Tables

		Table
1	Pinout Description	4-8
2	TCM3105 Modes of Operation	4-10
3	4.4336 MHz Crystal Manufacturers	4-13

Basic Principles of Modem Operation

A modem is a device that enables two digital electronic systems to communicate over the telephone network. To accomplish this, the digital signals must be converted to analog signals. The short pulses used by digital equipment contain high frequency components that are not supported by the limited bandwidth of telephone networks (300 Hz - 3400 Hz).

There are two major schemes of modulation used in modems for telephone networks. These are Frequency Shift Keying (FSK) and Phase Shift Keying (PSK). In FSK, serial data is modulated so that a "mark" is represented by a sine wave of one frequency, and a "space" is represented by a different frequency. In PSK, transitions in the digital bit stream are represented as shifts in phase angle of a single carrier frequency. The FSK concept is used by the TCM3105. The telephone network is a single-twisted pair of wires, usually 24 or 26 gauge. Two separate paths of communication are required by digital equipment systems in order to communicate with each other. Each system must have transmit and receive capability. This interface is supplied by the modem. Full duplex operation is the simultaneous transmission and reception on a single pair of wires. A two-to-four-wire converter, or hybrid as it is called in the telecommunications industry, is required (see Figure 1). This device removes the transmitted data from the receive path so that transmitted data does not interfere with valid received data.

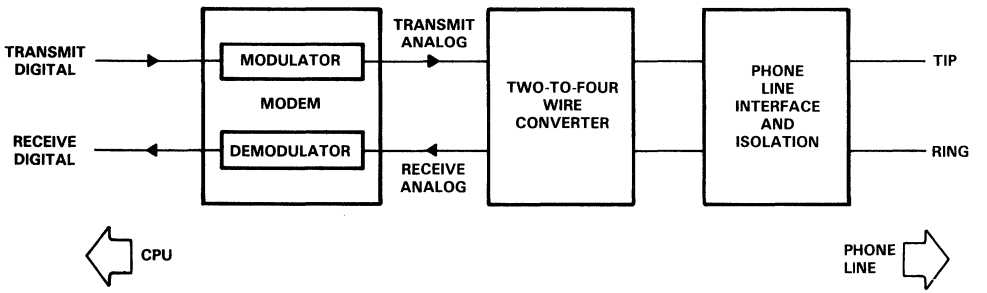


Figure 1. Typical Modem System Configuration

The two-to-four-wire converter requires matching the ranges of telephone network impedances. The impedance of the telephone network varies from line to line due to manufacturing and installation tolerances of the communications hardware. It is difficult to obtain good cancellation in a mass-produced piece of equipment.

Four separate frequencies, two transmit and two receive, are used to properly balance the two-to-four-wire converter. This is to ensure that transmitted and received data do not interfere with each other.

The TCM3105

The TCM3105 provides a majority of the functions required of a medium speed FSK modem in a single 16-pin DIP. The device is manufactured using silicon-gate complementary MOS technology. The TCM3105 features single 5-V supply operation and typical power consumption of approximately 40 mW. This makes the device ideally suited for use in battery operated equipment applications, as well as in standard applications. The TCM3105 device pinout is shown in Figure 2. Refer to pin description listed in Table 1 for the function and significance of each pin.

The TCM3105 is characterized for operation from 0°C to 70°C (JL suffix) as well as over the extended free-air temperature range of −40°C to +85°C (JE suffix).

Table 1. Pinout Description

PIN NAME	PIN NO.	I/O	DESCRIPTION
CDL	10	I	Carrier Detect Level—Sets the threshold level for the carrier detect decision. Refer to Description of the Carrier Detect Adjustment paragraph.
CDT	3	O	Carrier Detect — A high logic level output indicates the presence of a carrier at the RXA pin.
CLK	2	O	Clock — Continuous output clock signal at 16 times the highest selected transmit or receive baud rate.
OSC1 OSC2	15 16		Oscillator 1 and 2 — Input connections for external 4.4336 MHz crystal. See Table 2 for list of crystal manufacturers. If an external clock input is provided, then the OSC1 pin is left open and the clock is connected to the OSC2 pin.
RXA	4	I	Receive Analog — This input is referenced to an internal voltage and must be ac coupled.
RXB	7	I	Receive Bias Adjust — This input sets the threshold level of the slicer that allows the bias distortion on the RXD pin to be minimized. Refer to Description of the Receive Bias Adjustment paragraph.
RXD	8	O	Receive Digital Output — Outputs the demodulated receive data in positive logic, i.e., a mark is indicated by a high level and a space is indicated by a low level. The RXD output pin will remain high if there is no analog input on the RXA pin.
TRS	5	I	Transmit/Receive Standard Select Input — This pin along with TXR1 and TXR2 select the standard and mode to be used. See Table 1.
TXD	14	I	Transmit Digital — Digital input to the modulator in positive logic, i.e., a mark is indicated by a high level and a space is indicated by a low level. The data can be accepted at any rate from zero up to the selected baud rate and may be totally asynchronous.
TXR1 TXR2	13 12	I I	Transmit Rate 1 and 2 — These signals along with TRS set the standard and mode to be used. See Table 1.
V_{DD}	1		Positive supply voltage — 5 volts nominal.

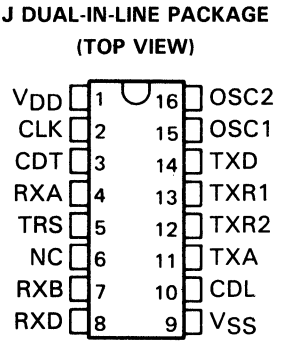
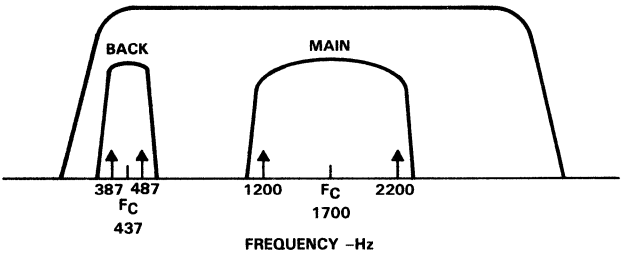
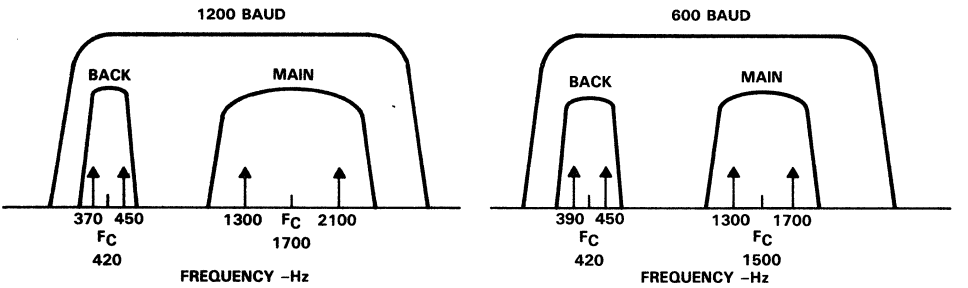


Figure 2. TCM3105 Pinout



(a) Bell 202 Channel Assignments



(b) CCITT V.23 Channel Assignments

Figure 3. Bell 202 & CCITT V.23 Channel Assignments

Modes of Operation of the TCM3105

The TCM3105 is an FSK type modem that is designed to implement the Bell 202 and CCITT V.23 Standards (see Figure 3), which define mark and space frequencies, and the maximum data rate that can be transmitted for a given mark/space pair.

The TCM3105 can be placed into a given mode of operation by applying the proper signals to the TRS (Transmit/Receive Status) and the TXR1 and TXR2 (Transmit Rates 1 and 2) input pins. The various modes of operation for the modems are summarized in Table 2. The CLK signal pin operates at a clock frequency of 16 times that of the selected receive or transmit bit rate, whichever is higher.

Table 2. TCM3105 Modes of Operation

Standard	TRS	TXR1	TXR2	Transmit Bit Rate (Bit/s)	Receive Bit Rate (Bit/s)	Transmit Freq (Hz)	Receive Freq (Hz)	Clock (kHz)
CCITT V.23	0	0	0	1200	1200	M 1300 S 2100	M 1300 S 2100	19.11
	1	0	0	1200	75	M 1300 S 2100	M 390 S 450	19.11
	0	0	1	600	75	M 1300 S 1700	M 390 S 450	9.56
	1	0	1	600	600	M 1300 S 1700	M 1300 S 1700	9.56
	0	1	0	75	1200	M 390 S 450	M 1300 S 2100	19.11
	1	1	0	75	600	M 390 S 450	M 1300 S 1700	9.56
	0	1	1	75	75	M 390 S 450	M 390 S 450	1.19
BELL 202	$\overline{CLK}$	0	0	1200	1200	M 1200 S 2200	M 1200 S 2200	19.11
	$\overline{CLK}$/8	0	1	1200	150	M 1200 S 2200	M 387 S 487	19.11
	$\overline{CLK}$/8	0	1	1200	5	M 1200 S 2200	M 387 S 0	19.11
	CLK	1	0	150	1200	M 387 S 487	M 1200 S 2200	19.11
	CLK	1	1	150	150	M 387 S 487	M 387 S 487	2.39
	*	1	*	5	1200	M 387 S 0	M 1200 S 2200	19.11
	1	1	1	Transmit Disabled	1200	Transmit Disabled	M 1200 S 2200	19.11

*In this mode, the modulation is controlled by the TRS and TXR2 inputs, TXD is set to 1.

If TRS = CLK & TXR2 = 0, then TXA = 387 Hz
If TRS = 1 & TXR2 = 1, then TXA = 0 Hz

Architectural Description of the TCM3105

The modem has four main functional blocks: a transmitter, a receiver, a carrier detector, and timing and control (see Figure 4).

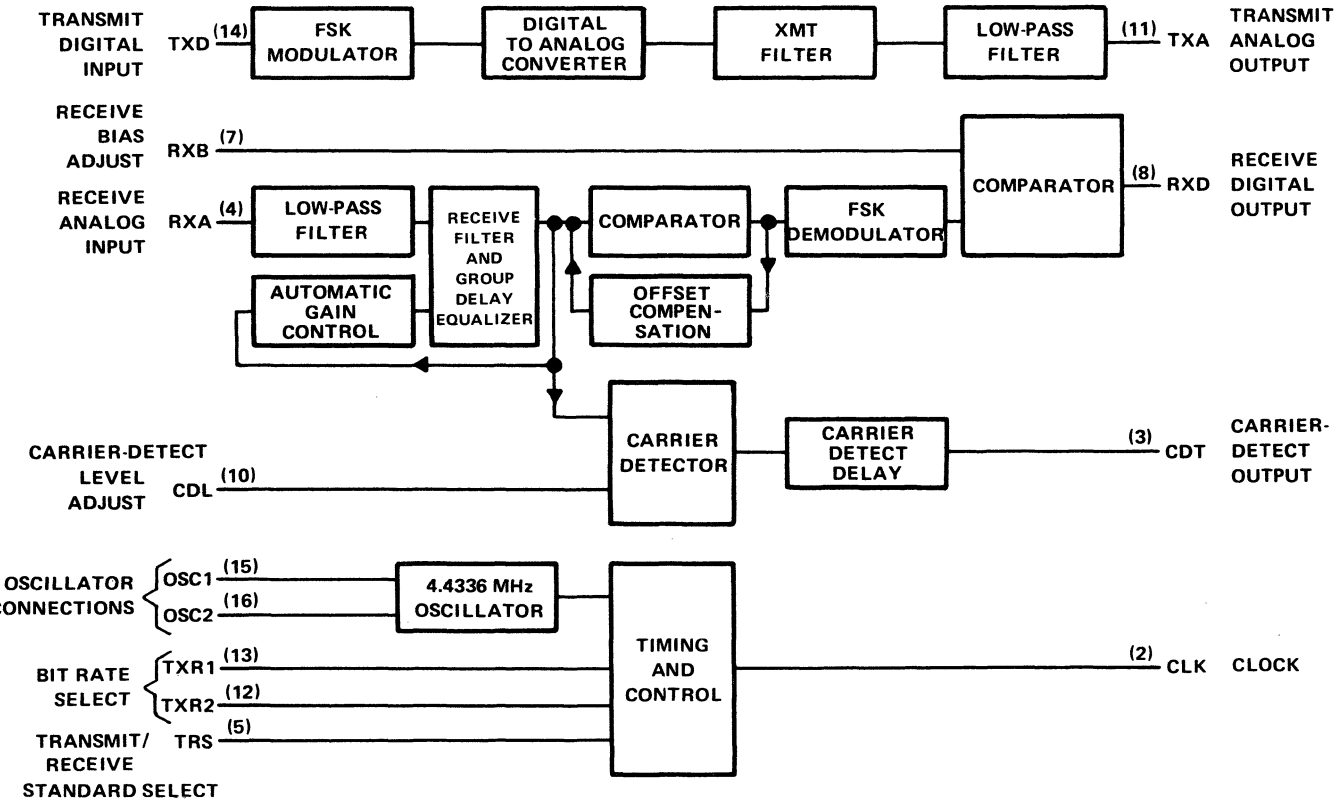


Figure 4. TCM3105 Functional Block Diagram

Transmitter

The transmitter consists of a phase-coherent FSK modulator with a transmit filter and transmit amplifier. The modulator is a programmable frequency synthesizer that obtains the required output frequencies for the modem by dividing the 4.4336 MHz master clock. The division ratio is set by the states of the TXD (Transmit Digital), TXR1, TXR2 and TRS inputs (see Table 2). The transmit filter consists of a switched-capacitor filter stage and a continuous-time filter stage. The switched-capacitor filter samples at a rate dependent upon the transmit frequency selected. This arrangement offers the optimum rejection of out-of-band terms, regardless of the transmit frequency. The continuous-time filter is a second-order Bessel function filter that rejects the clock feedthrough from the switched capacitor filter. The analog output (TXA) pin of the modem is dc biased at approximately 50% of the supply voltage and should be coupled to the two-to-four-wire converter. The overall transmit gain is adjustable within the two-to-four-wire converter.

Receiver

The receiver section consists of an antialiasing prefilter, receive amplifier, receive filter, compromise line equalizer, limiter, demodulator, post demodulator filter, and slicer.

The antialiasing prefilter is a continuous-time low-pass filter that prevents aliasing of high frequency components and sets the band limits of the input signal.

The receive amplifier is part of the receive filter. The receive filter is an elliptic switched-capacitor design, composed of three sections. The first section is a filter that has a high discrimination against the transmit frequencies. The second section is a bandpass filter that includes an automatic gain control function to regulate the amplitude of the signal to the slicer. The last stage is a low-pass filter that attenuates high frequency interference. Overall, the receive filter attenuates broadband interference and removes out-of-band energy that would interfere with demodulation.

The compromise line equalizer is a switched-capacitor equalizer that compensates for the group delay distortion of the receive filter and telephone network. The output of the equalizer is converted to a square wave by a hard limiter.

The demodulator is a conventional monostable multivibrator configured to trigger on the rising and falling edges of the limiter output. The output of the demodulator is a train of fixed-length pulses at a frequency equal to twice that of the received analog signal. Thus, the dc component of this signal is proportional to the frequency of the received signal.

The post demodulator filter is a switched-capacitor low-pass filter that extracts the dc component from the output of the demodulator.

The final stage of the receiver is a slicer that has an externally adjusted reference voltage applied to the RXB (Receive Bias) pin. The RXB reference voltage is necessary to compensate for offsets introduced in the switched-capacitor circuitry. The output of the slicer is the RXD (Receive Digital) pin. The RXB reference voltage need not be readjusted when changing modes of operation, as the modem compensates internally.

Carrier Detector

The carrier detector section consists of an in-band energy detector and a digital delay. The energy detector measures the total energy level at the output of the receive filter and compares this level to a bias level that is set at the CDL (Carrier Detect Level) output pin. The CDT (Carrier Detect) pin is a logic high in the presence of a carrier.

A degree of protection against false output, due to brief signal dropouts, is present. The energy detector is buffered by a short time delay qualifier before the carrier detect signal is sent through to the CDT pin. In addition, the detector exhibits approximately 4 dB of hysteresis to prevent output oscillation.

Timing and Control

The timing is controlled by an external 4.4336 MHz crystal oscillator. Refer to Table 3 for a list of suggested crystal manufacturers. From this master frequency, the timing section generates all the clock control signals and supplies the CLK output signal.

Table 3. 4.4336 MHz Crystal Manufacturers

Manufacturer	CL	Tolerance	Comments
Midland-Ross PH. 414-763-3591	20 pF	±0.005% @ 25°C	Stock Number C 1721N Part Number MPC 18 Requires a 27 pF capacitor from each leg to ground
CTS Knights PH. 815-786-8411	20 pF	±0.005%	Part Number R 1335-5BA4433619 Requires a 27 pF capacitor from each leg to ground
Erie Frequency Control PH. 717-249-2232	30 pF	±0.005%	Part Number L 01-0096-004433618 Requires a 50 pF capacitor from each leg to ground
Seiko Instruments PH. 213-530-8777	15 pF	±0.005%	No Part Number Available Requires a 15 pF capacitor from each leg to ground

Description of the Interface Line

FCC REGISTRATION

The Federal Communications Commission (FCC) has imposed certain restrictions on terminal equipment, including modems, that is connected to the telephone network. FCC Part 68 documents these requirements, which include the following limitations: leakage current, hazardous voltage, signal power, and on-hook impedance. Any device connected to the telephone network must conform to these requirements and be assigned an FCC registration number. The primary interest to modem designers is the hazardous voltage requirements and leakage current limitations. The most practical way to meet the FCC requirements is to electrically isolate the modem from the telephone network with a transformer. This is the most widely accepted method for interfacing direct-connect modems to the telephone network.

Preassembled direct connect devices that perform the modem-to-telephone network interface are available. These devices have typically been assigned an FCC registration number and they include many features such as line powering, ring detection and regulation of loop current. One manufacturer of such products is Cermetek Microelectronics.

FCC registration is not required when the modem is acoustically coupled to the telephone network through a telephone handset. However, this method presents serious drawbacks because telephone sets have very different frequency responses, which make high performance acoustically-coupled modems difficult to design.

TWO-TO-FOUR WIRE CONVERTER OPERATION

The two-to-four-wire converter is part of a typical telephone network interface (see Figure 5). This circuit is necessary to interface the two separate digital channels (transmit and receive) to the single-pair telephone network. A simplified two-to-four-wire converter is shown in Figure 6. This is one of several possible solutions.

To understand how the converter operates, the signal is traced from the transmit input to the receive output. A signal entering the transmit node is buffered by U1A and the output signal is placed across an effective load of $Z_T + Z_L$ in parallel with $Z_T' + Z_L'$. The signal across Z_L is then placed on the telephone network via a transformer. A signal being received from the telephone network is buffered by U1B and placed at the receive node. To reduce the amount of the transmit signal that appears at the receive node, U1B is used in the differential mode to cancel two transmit signals that are 180 degrees out of phase with one another. The two transmit signals appearing at U1B must be of comparable levels. By correctly selecting Z_T' and Z_L', the transmit signals at U1B will be approximately of the same level. Z_T' and Z_L' should be selected to satisfy the following equation:

$$\frac{Z_T}{Z_L} = \frac{Z_T'}{Z_L'}$$

Note: The above equation does not have a restriction on the absolute magnitude of Z_T' and Z_L', only on the ratio of the two. They are therefore scaled versions of the termination and line impedances. This scaling allows small capacitances and large resistances to be incorporated in the network.

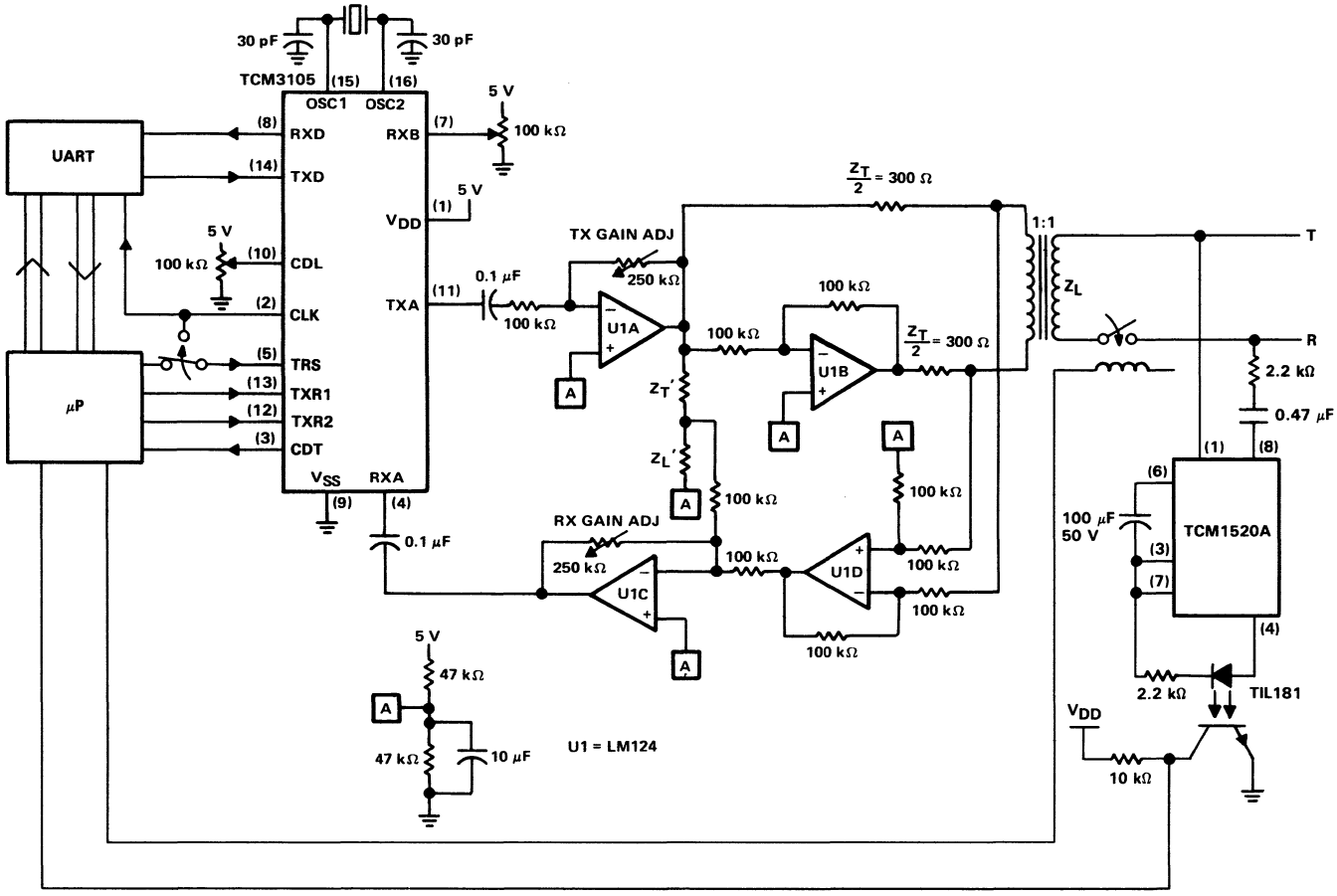


Figure 5. Typical Application Circuit

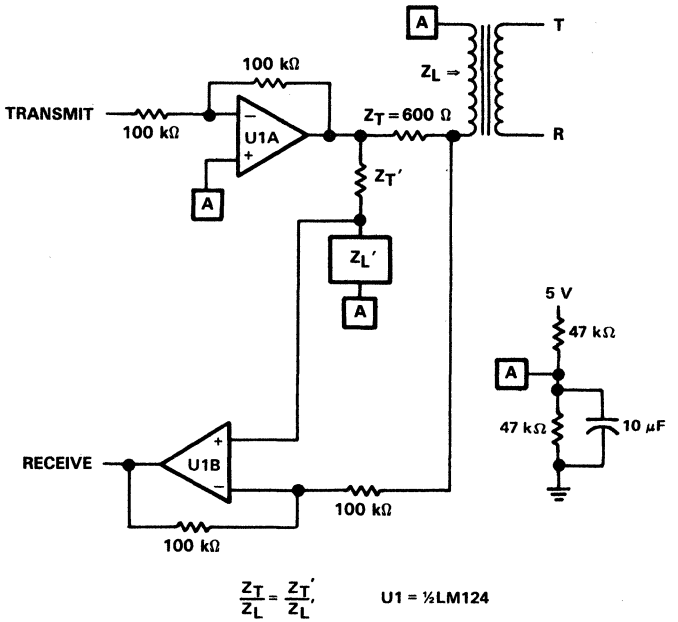


Figure 6. Simplified Two-to-Four Wire Converter

Description of the Carrier Detect Adjustment

The threshold of the carrier detect circuitry in a modem can be adjusted by an external voltage bias at the CDL pin. The minimum detected level is set between the limits of −55 dBm to −35 dBm. A plot of the threshold versus the bias at the CDL pin is shown in Figure 7. The procedure for adjusting CDL is as follows:

1. Apply 4 V to the CDL pin.
2. Place the correct inputs to pins TXR1, TXR2, and TRS so that the TCM3105 is in the desired mode. Refer to Table 2.
3. Apply an ac-coupled, sinusoidal signal to the RXA pin at a frequency between the mark and space frequencies for the mode selected. The amplitude of this signal is set to the lowest signal level that is desired for the modem to detect. A nominal signal level is −44 dBm.
4. The CDT pin should be low.
5. Decrease the voltage at the CDL pin until the voltage at the CDT pin becomes high.

Note: The TCM3105 has a carrier detect delay of 20 ms to 80 ms depending on the receive rate selected. A wait for this delay to time out is required before the CDT pin is monitored.

6. The carrier detect level adjustment is now set.

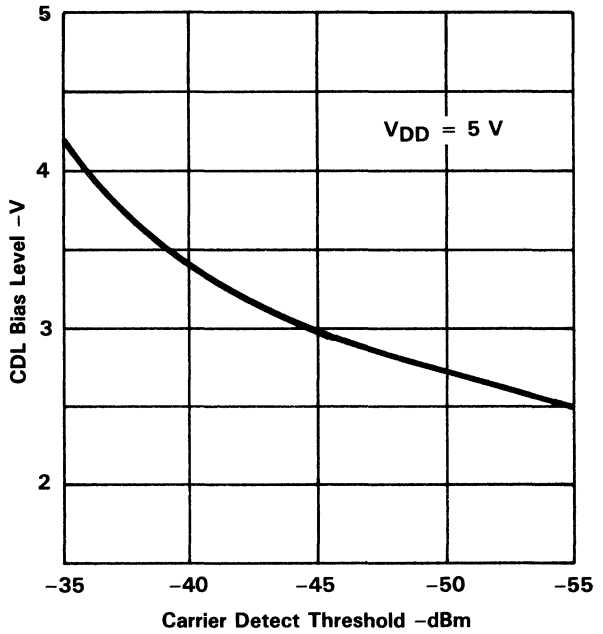


Figure 7. CDL Bias Level vs Carrier Detect Threshold

Description of the Receive Bias Adjustment

An adjustment of the bias voltage at the RXB pin is required to minimize the bias distortion of the demodulated receive signal at the RXD pin. The bias voltage applied to the RXB pin is used by the slicer to set an internal threshold. A plot of the bias distortion of the RXD signal versus the bias level at the RXB pin is shown in Figure 8. The receive bias can be adjusted by one of two methods.

Method 1

1. Apply the desired signals to pins TXR1, TXR2, and TRS to set the modem in the 1200 baud transmit/1200 baud receive half-duplex mode (for either CCITT V.23 or Bell 202 Standards).
2. Set the modem in the loopback mode (as shown in Figure 9). The attenuator ensures that the analog signal from the TXA pin to the RXB pin is less than 0.78 V peak to peak.
3. Apply a ground to V_{DD} and a 600 Hz square wave to the TXD pin.
4. Monitor the RXD pin with an oscilloscope and adjust the voltage at the RXB pin until the output signal at the RXD pin has a 50% duty cycle.

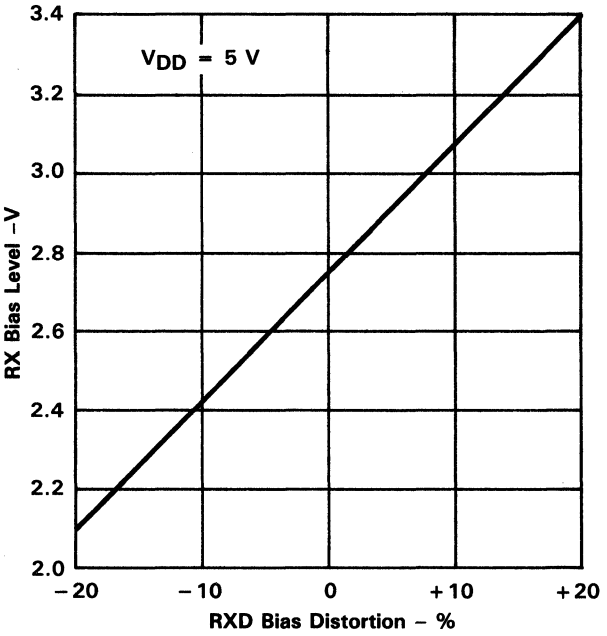


Figure 8. RXB Bias Level vs RXD Bias Distortion

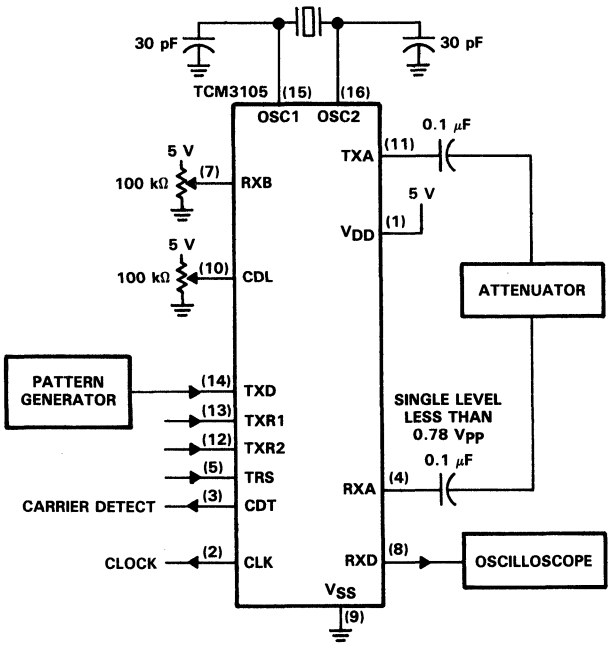


Figure 9. Loopback Circuit Diagram

Method 2

1. Apply the desired signals to pins TXR1, TXR2, and TRS to set the TCM3105 in any proper mode.
2. Apply a signal with an amplitude of less than 0.78 V peak to peak to the RXA pin. The frequency of the input signal should be exactly in the middle of the mark and space frequencies for the mode selected.

   For example, if the Bell 202 1200 baud receive mode is selected, the signal should then have a frequency of 1700 Hz which is the center of the mark frequency of 1200 Hz and the space frequency of 2200 Hz.
3. Apply 3.5 V to the RXB pin, and the RXD pin should exhibit a mark (or high).

   Reduce the voltage at the RXB pin until RXD pin exhibits a low (space), then increase the voltage at the RXB pin until the RXD pin exhibits a high (mark). The bias at the RDX pin is now set.

   Either method will correctly set the bias required for the RXB pin to minimize the bias distortion. Once the adjustment has been set for one particular mode of operation, no further adjustment should be necessary for the remaining modes. The bias distortion should not vary with the baud rate.

Output Jitter Measurement

To measure the demodulated receive output data jitter at the RXD pin, it is necessary to set the modem into a loopback mode (see Figure 9). Apply the proper signals to pins TRS, TXR1, and TXR2 to place the modem in the 1200 baud transmit/1200 baud receive half duplex mode (for either CCITT V.23 or Bell 202). Apply a ground to V_{DD} and a 600 Hz square wave to the TXD pin. With an oscilloscope (set for leading edge triggered) look at the signal at the RXD pin. It should appear as illustrated in Figure 10. The jitter of the output is the difference between T_{max} and T_{min}.

Notes: A. Section VII must be accomplished before the jitter measurement.

B. 4.4336 MHz is from a 4.43361875 MHz crystal (European color burst crystal).

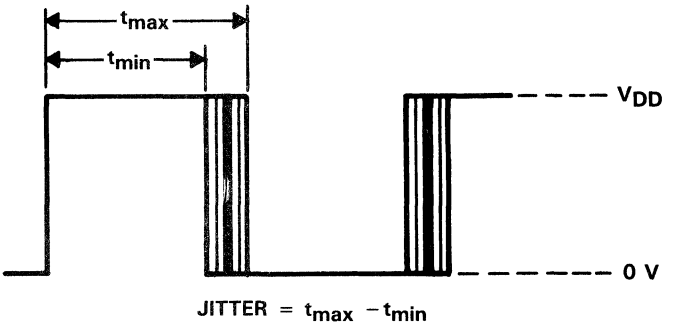


Figure 10. Jitter Timing Diagram

Conclusion

The TCM3105 Modem is a simple solution for many medium-speed data communications systems. On a single chip, there is a FSK modulator/demodulator with all the necessary filtering and equalization to provide full asynchronous operation up to 1200 baud. A complete data communications solution with the TCM3105 can be implemented with a minimal amount of design effort and chip count. The low-power consumption (40 mW typ) and the extended operating temperature range (−40°C to 85°C for the JE suffix) make the TCM3105 ideal for battery operated equipment that must withstand a harsh environment. Refer to the TCM3105 data sheet for detailed specifications.

TCM2203 Line Interface Circuit and TCM2222 HDB3/AMI Encoder/Decoder

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TEXAS INSTRUMENTS

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Contents

Title	Page
INTRODUCTION	4-25
THEORY OF OPERATION	4-26
Transmitter	4-26
Receiver	4-26
Signal Restoration	4-26
Data Detection	4-29
Clock Recovery	4-29
SYSTEM DESIGN	4-29
Transmitter Circuit	4-29
Receiver Circuit	4-29
Line Transformer	4-31
ALBO Filter	4-31
Preamplifier	4-33
Equalizer	4-33
Peak Detector	4-34
Mute Output	4-34
Clock Recovery	4-34
T1 Board Adjustment Procedure	4-34
SUMMARY	4-35
REFERENCES	4-35

List of Illustrations

Figure	*Title*	*Page*
1	Data Transmission System Block Diagram	4-25
2	Normalized Power Spectral Density	4-26
3	Data Encoding Formats	4-26
4	Transmitter Circuit Diagram	4-27
5	Transmit Timing Diagram	4-27
6	Typical Transmission Line Transfer Characteristics	4-27
7	Line Build-Out Transfer Function	4-27
8	Receiver Block Diagram	4-28
9	Receive Signal Eye Diagram	4-31
10	T1 System Block Diagram	4-31
11	T1 Circuit Schematic	4-32
12	Output Pulse Requirements	4-33
13	Filter Responses	4-34

INTRODUCTION

Texas Instruments TCM2203 Line Interface Circuit is designed to interface Pulse Code Modulated (PCM) data between a digital transcoder such as the Texas Instruments TCM2222 and a transmission line. The TCM2203 can transmit and receive data at rates up to 3 megabits per second using four wires (two twisted pairs).

The TCM2203 is designed to meet the requirements for AT&T T1 data transmission of 1.544 megabits per second[1] as well as the CCITT counterpart of 2.048 megabits per second. The TCM2203 is not limited to these requirements and can be used in custom designs at frequencies up to 3 megabits per second. The TCM2203 can be used for applications such as the Integrated Services Digital Network (ISDN) primary access rate (23B channels + one D channel) of 1.544 megabits per second.

The TCM2203 line interface circuit[2] consists of two separate sections. The transmit section uses encoded digital data and clock information to produce bipolar Return to Zero (RZ) pulses on a transmission line. The receive section takes bipolar RZ pulses which have been attenuated by a transmission line, restores the signal and recovers both the encoded data and clock information. A transcoder is used to produce the encoding and decoding required between a Non Return to Zero (NRZ) bit serial data stream and the line interface circuit. Figure 1 is a block diagram showing a typical implementation using the TCM2203 line interface and the TCM2222 transcoder.[3] The TCM2222 performs three functions: encoding, decoding, and signal monitoring.

The T1 Carrier uses Alternate Mark Inversion (AMI) coding. This scheme transmits alternate polarity pulses for successive logic high signals. No pulse is transmitted for a logic low. AMI coding offers two advantages; no dc signal content allowing transformer coupling, and the primary signal component at one-half the data rate allowing a reduced system bandwidth. This is illustrated by the Normalized Power Spectral Density detail shown in Figure 2.

The inherent flaw of AMI coding is the inability of the receiver to maintain clock integrity when a long string of continuous zeros is transmitted. To avoid this problem AT&T limits the number of consecutive zeros to 15. The problem can also be eliminated by using a coding scheme which sends a violation code (consecutive pulses of the same polarity) to represent a specific series of zeros. European systems use High-Density Bipolar Three-line substitution coding (HDB3), and Bipolar with Eight-Zero Substitution coding (B8ZS) is planned for implementation in the U.S. Figure 3 illustrates AMI, HDB3, and B8ZS coding. The TCM2203 is compatible with each of these schemes.

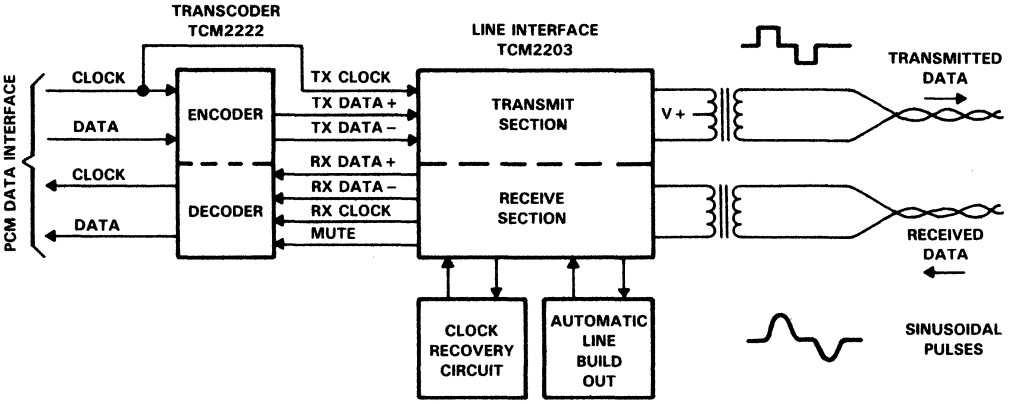


Figure 1. Data Transmission System Block Diagram

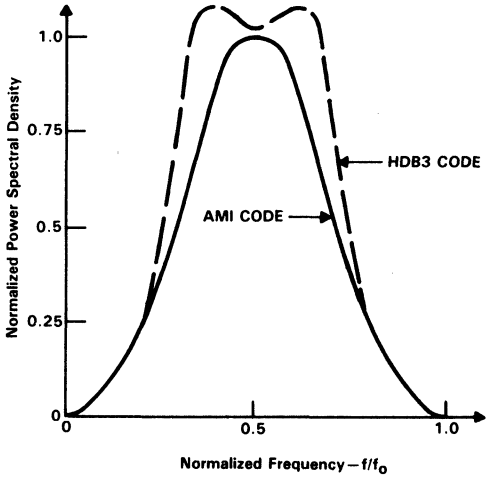
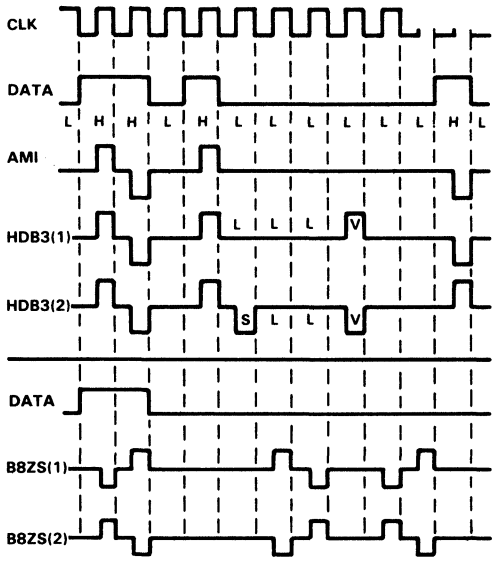


Figure 2. Normalized Power Spectral Density



NOTES:
1. In the HDB3(1) signal, the previous violation bit was negative. In the HDB3(2) signal, the previous violation bit was positive.
2. In B8ZS(1), the last pulse prior to the violation bit was positive. In B8ZS(2), the last pulse was negative.
3. V is a violation bit.
4. S is a stuffing bit.

Figure 3. Data Encoding Formats

THEORY OF OPERATION

Transmitter

The TCM2203 transmitter converts the digital data and clock signals from the transcoder to bipolar current pulses.

The transmitter section schematic is shown in Figure 4. Three signals comprise the transmit data input to the TCM2203; TX DATA IN X, TX DATA IN Y, and TX CLK IN. The data input signals are fed to two separate NOR gates. The other input to each gate is TX CLK IN. The output of each NOR gate feeds the base of a transistor. The collectors are outputs from the TCM2203 (LINE OUT X and LINE OUT Y). Whenever TX CLK IN is logic low and either TX DATA IN X or TX DATA IN Y is logic low, one of the transistors will be turned on (Figure 5). When either of the output transistors is turned on current will flow in one-half of the line output transformer primary. Current in the primary of the line transformer causes either a positive or a negative pulse to be induced on the secondary.

Receiver

The receiver section of the TCM2203 performs signal restoration, data detection, and clock recovery.

Signal Restoration

Figure 6 describes the typical transmission line transfer function variation with line length. As length increases, the overall attenuation increases due to the resistive component of the line impedance. In addition to this flat attenuation, there is a frequency dependent attenuation that varies with line length. The frequency dependent attenuation is caused by the increased reactive component (primarily capacitive) of the line impedance at longer lengths. The transmitted signal is also distorted by reflections due to mismatches in line termination. The resulting amplitude and frequency distortion degrades the data and increases the error rate. Signal restoration is accomplished by using a filter network to provide a complimentary transfer function which, when combined with the transmission line transfer function, will provide a flat frequency response over the portion of the spectrum where the signal energy is concentrated. The attenuation for a transmission line and the required complimentary transfer function is given in Figure 7. The TCM2203 can implement a network and feedback system which automatically varies the complimentary transfer function, thereby accommodating variations in the transmission line.This is called an Automatic Line Build-Out (ALBO).

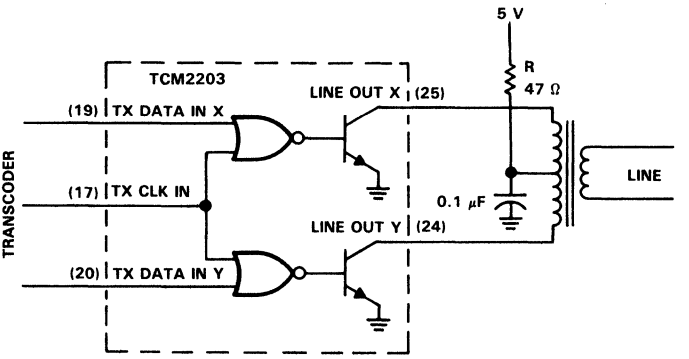


Figure 4. Transmitter Circuit Diagram

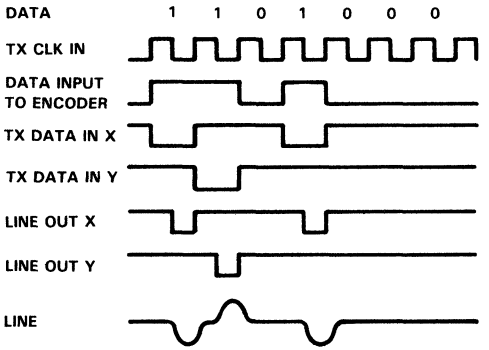


Figure 5. Transmit Timing Diagram

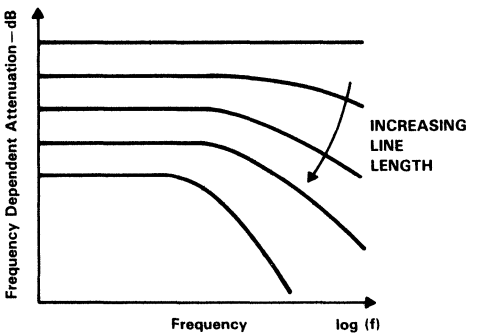


Figure 6. Typical Transmission Line Transfer Characteristics

The TCM2203 ALBO is based on the assumption that the transmitted signal has a constant amplitude at the transmitter and that the amplitude of the signal at the receiver can be used to predict the transmission line transfer function.

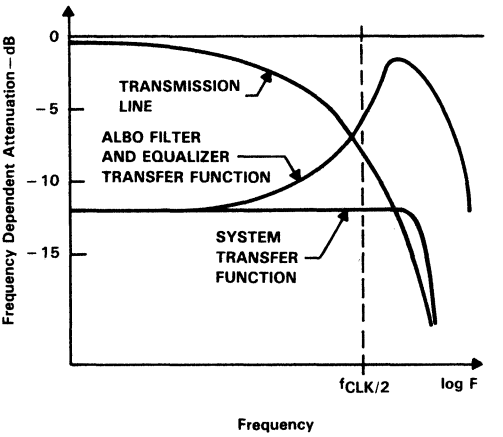


Figure 7. Line Build-Out Transfer Function

The information derived from the signal amplitude can then be used to control the shape of the complimentary transfer function used to restore the signal.

The TCM2203 ALBO system (Figure 8) operates as follows:

1. The received signal after passing through the filter network is input to an amplifier and phase splitter (pin 14). The phase splitter outputs are peak detected and stored on two capacitors (pins 15 & 16).
2. The stored peak values are averaged and the resulting signal is fed to a transconductance amplifier.
3. The output current from the transconductance amplifier is fed to two diode strings. The diode strings serve as variable dynamic resistances. The diode string outputs (ALBO1 & ALBO2) are used to control the transfer function of the filter circuits.

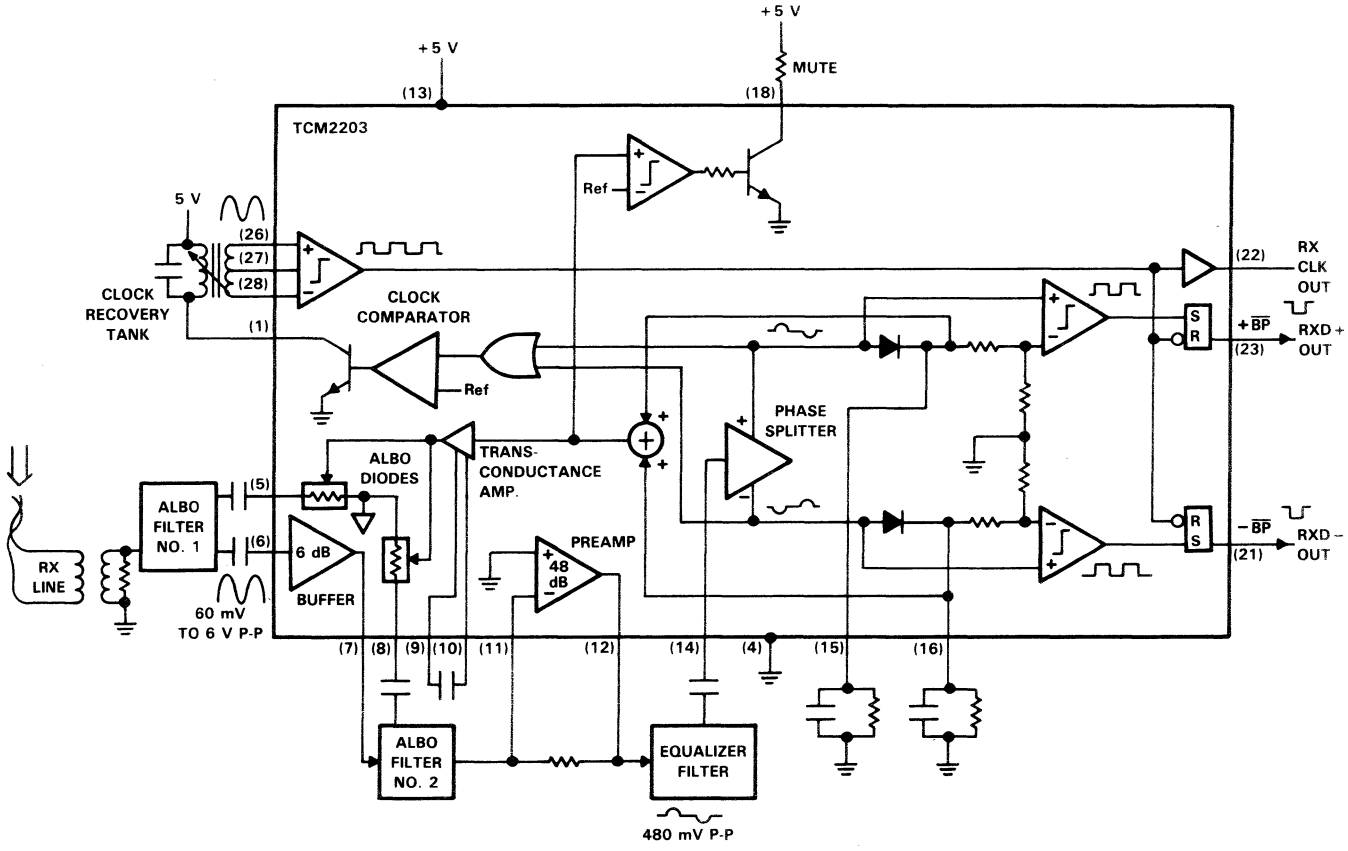


Figure 8. Receiver Block Diagram

The TCM2203 receiver section provides two amplifiers (6 dB fixed gain buffer and 48 dB adjustable gain preamplifier) in addition to the two ALBO pins which can be used to construct the signal restoration circuit.

Data Detection

The data detection circuit (see Figure 8) operates as follows:

1. The signals from the phase splitter amplifier are fed to two comparators.
2. The signals are compared to one-half of the stored peak values. The comparator outputs are then latched in two flip-flops using the extracted clock signal.
3. The two flip-flop complements, (RXD + OUT and RXD − OUT), are brought out on pins 23 and 21.

The two data signals RXD + OUT and RXD − OUT are sent with the recovered clock RX CLOCK OUT to a transcoder for decoding and error detection.

Clock Recovery

The TCM2203 clock recovery circuit is a low-Q circuit using a tuned LC network. The low Q circuit is used to minimize false clocks due to noise. Clock recovery is accomplished as follows:

1. The data signals from the phase splitter are combined to produce a full wave rectified signal. The rectified signal is compared to the clock threshold which is two-thirds the average of the stored peak signal values.
2. That portion of the pulse which exceeds the clock threshold value is used to control a drive transistor. The open collector of the drive transistor (pin 1) is connected to the primary of the clock recovery transformer.
3. The output transistor injects current pulses into the tuned primary circuit of the transformer. The tuned primary extracts the clock term from the current pulses.
4. The extracted clock signal is fed from the transformer secondary to pins 26 & 28 of the TCM2203. The sinewave is converted to a square wave with a 60 dB gain comparator. A phase-shifting capacitor connected to pins 2 and 3 optimizes the clock phase relative to the data.
5. The recovered clock is sent to the data detection circuit flip-flops, then buffered, and output on pin 22.

The eye diagram in Figure 9 indicates the signal thresholds for data and clock decisions.

SYSTEM DESIGN

The TCM2203 is capable of working with different data encoding formats and over a range of frequencies, however circuit design and component selection must be based on specific system parameters. The information in the following sections is based on the T1 Demonstration Circuit. Figure 10 is a block diagram showing the circuit consisting of two stages of ALBO plus a fixed equalizer. Figure 11 is the circuit schematic of the demonstration circuit. All of the circuit references and reference designators in the following descriptions are from the schematic in Figure 11. Table 1, T1 Demo Parts list follows the schematic in Figure 11.

Transmitter Circuit

The TCM2203 output drive transistors can sink 20 mA (I_{OL}) with a saturation voltage of 1 V (V_{OL}). R19 and C14 provide a filter and current limit for the output drive. The output transformer T2 is an AEI Magnetics Part No. 327-0044.[4] This transformer has a 2.71:1 turns ratio. The transformer must have a secondary inductance of more than 6 mH and a Q of less than 6, both measured at 1MHz in order to meet the output pulse requirements shown in Figure 12. Pulse timing is a function of the transformer design, reflected transmission line impedance, output driver current and system clock. The pulse amplitude is a function of the transformer turns ratio, output transistor saturation voltage (V_{OL}), transmission line impedance, and power supply voltage.

Receiver Circuit

The receiver design consists of the input transformer and all of the filter components associated with signal restoration. The transfer function of the restoration circuit is the combination of two ALBO circuits, two amplifiers and the equalizer. Figure 13 shows the transfer functions of the Preamp, the equalizer, and a single ALBO stage at three different ALBO resistances (25 ohms, 430 ohms, and 10000 ohms).

The TCM2203 is a single supply voltage part and all of the analog signal inputs are internally biased. Capacitors must be used to couple the signals between the TCM2203 and the external filter components.

Table 1. T1 Demo Circuit Parts List

QTY	REFERENCE	DESCRIPTION
1	C1	1500 pF, 100 V, CERAMIC DISK CAPACITOR
3	C2-C4	0.1 μF, 50 V, CERAMIC DISK CAPACITOR
1	C5	1500 pF, 100 V, CERAMIC DISK CAPACITOR
3	C6-C7, C9	0.1 μF, 50 V, CERAMIC DISK CAPACITOR
1	C8	10 μF, 25 V, TANTALUM ELECTROLYTIC CAPACITOR
2	C10, C18	100 pF 200 V, CERAMIC DISK CAPACITOR
2	C11, C12	0.1 μF 50 V, CERAMIC DISK CAPACITOR
1	C13	15-60 pF, VARIABLE CAPACITOR
3	C14-C16	0.1 μF 50 V, CERAMIC DISK CAPACITOR
1	C17	39 pF 200 V, CERAMIC DISK CAPACITOR
4	C19-C22	0.1 μF 50 V, CERAMIC DISK CAPACITOR
1	C23	100 μF 20 V, TANTALUM ELECTROLYTIC CAPACITOR
1	C24	1.0 μF, 50 V, CERAMIC DISK CAPACITOR
2	C25, C27	10 μF, 25 V, TANTALUM ELECTROLYTIC CAPACITOR
1	C26	0.1 μF, 50 V, CERAMIC DISK CAPACITOR
7	D1-D7	RED LED TIL-220
3	J1A, J1B, J2A,	BANANA JACK
3	J2B, J7A, J7B	BANANA JACK
4	J3-J6	PCB MOUNT BNC JACK
2	L1-L2	270 μH AXIAL LEAD INDUCTOR, NYTRONICS
1	L3	150 μH AXIAL LEAD INDUCTOR, NYTRONICS
2	R1, R22	130 Ω, 1/4 W, 1%, METAL FILM RESISTOR
2	R2, R7	1.2 kΩ, 1/4 W, 1%, METAL FILM RESISTOR
4	R3, R4, R8, R10	430 Ω, 1/4 W, 1%, METAL FILM RESISTOR
2	R5, R9	270 Ω, 1/4 W, 1%, METAL FILM RESISTOR
2	R6, R11	620 Ω, 1/4 W, 1%, METAL FILM RESISTOR
1	R12	2.0 kΩ, 1/4 W, 1%, METAL FILM RESISTOR
1	R13	62 kΩ, 1/4 W, 1%, METAL FILM RESISTOR
1	R14	4.2 kΩ, 1/4 W, 1%, METAL FILM RESISTOR
1	R15	510 Ω, 1/4 W, 1%, METAL FILM RESISTOR
1	R16	750 Ω, 1/4 W, 1%, METAL FILM RESISTOR
2	R17, R18	100 kΩ, 1/4 W, 5%, CARBON FILM RESISTOR
1	R19	47 Ω, 1/4 W, 5%, CARBON FILM RESISTOR
1	R20	1 kΩ, 1/4 W, 5%, CARBON FILM RESISTOR
1	R21	20 kΩ, 1/4 W, 1%, METAL FILM RESISTOR
1	R30	4.7 kΩ, 1/4 W, 5%, CARBON FILM RESISTOR
7	R23, R24, R25, R26 R27, R28, R29	470 Ω, 1/4 W, 5%, CARBON FILM RESISTOR
1	S1	4 POLE ST DIP SWITCH
1	T1	1:1 PULSE XFMR AIE MAGNETICS P.N. 327-0045
1	T2	2.71:1 PULSE XFMR AIE MAGNETICS P.N. 327-0044
1	T3	3:2 PULSE XFMR AIE MAGNETICS P.N. 327-0049
1	U1	TCM2203 LINE INTERFACE
1	U2	TCM2222 AMI/HDB3 ENCODER/DECODER
1	U3	SN74HC04 HEX INVERTER

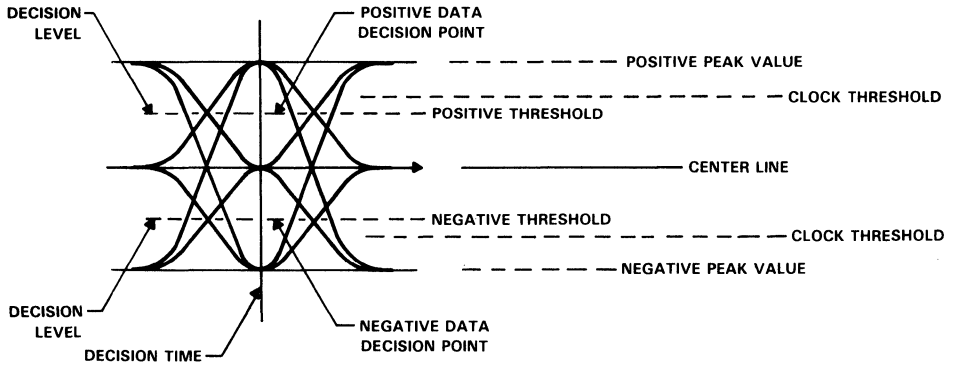


Figure 9. Receive Signal Eye Diagram

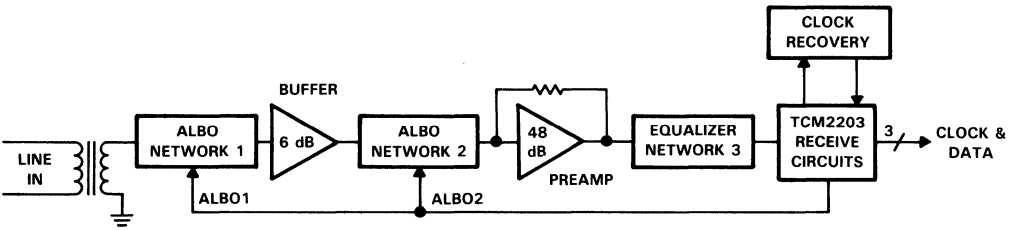


Figure 10. T1 System Block Diagram

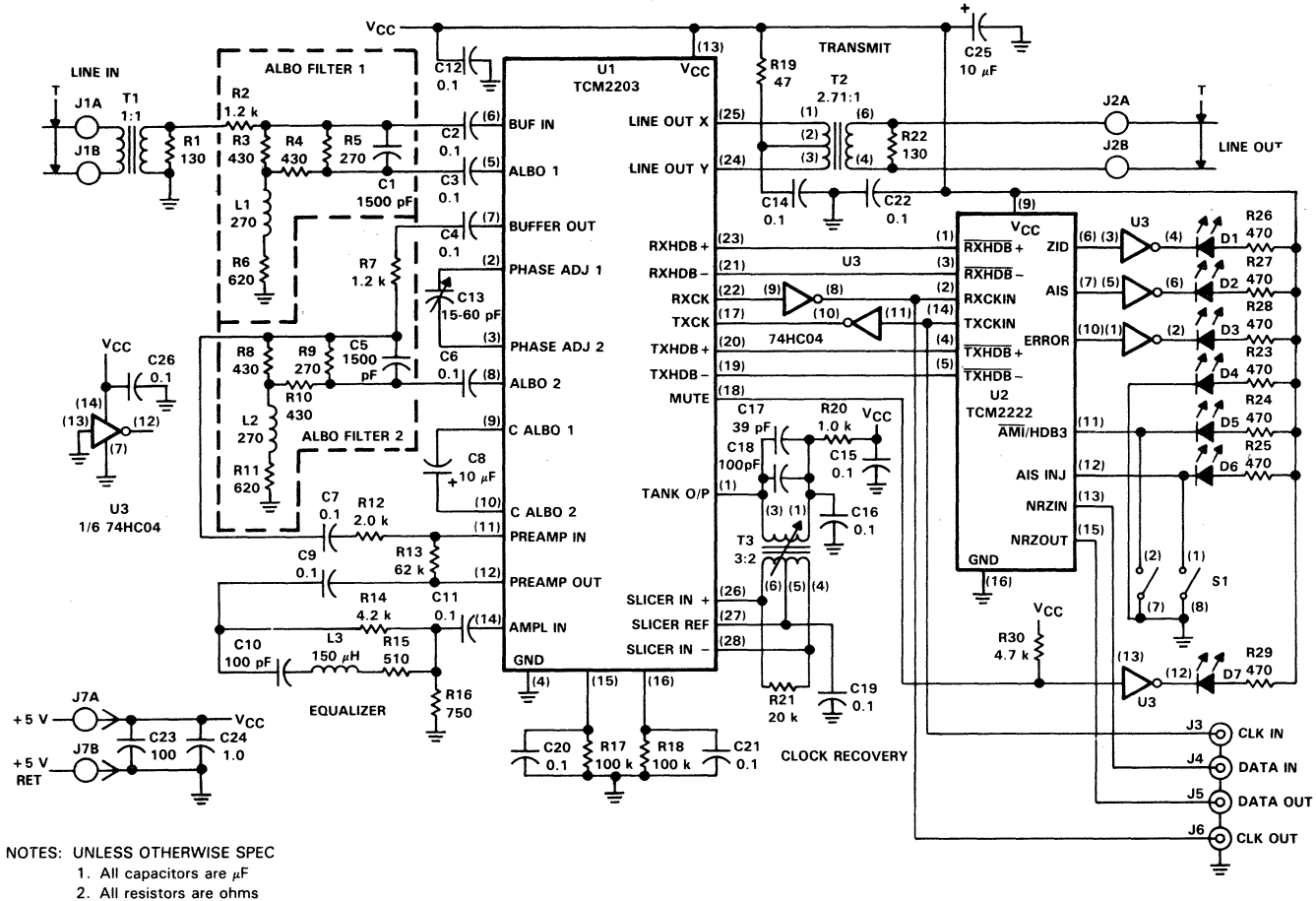
Line Transformer

The receive transformer should have a 1:1 winding ratio with a primary inductance greater than 6 mH and a Q of less than 6 measured at 1 MHz. The AIE Magnetics Part No. 327-0045 meets these requirements.

ALBO Filter

The ALBO filter circuit must provide a transfer function which can be controlled with a variable resistance. The configuration chosen is a bridge T filter as originally described by H. W. Bode.[6] Two identical bridge T circuits are used in this implementation. The received signal is coupled directly to the first ALBO circuit consisting of R2-R6, C1 and L1. C3 couples the ALBO diode to the filter and C2 couples the ALBO filter output to the Buffer amplifier. The transfer function of this filter is plotted in Figure 13. The dynamic resistance RALBO of the ALBO diodes ranges from 25 ohms to 10K ohms typical. When RALBO = 25 ohms, the attenuation increases with frequency; this occurs for a short transmission line (maximum received amplitude). When RALBO = 430 ohms, the attenuation is flat; this occurs at nominal line length. When RALBO = 10K ohms, the attenuation decreases with frequency; this occurs for long transmission lines. This single ALBO circuit has a dynamic range of 15 dB at one-half f_{clk}. The two ALBO circuits can provide a range of 30 dB. AT&T CB113 specifies performance with cable losses of 7.5 dB to 35 dB (27.5 dB dynamic range).

The first and second ALBO filters are isolated by the 6 dB buffer amplifier. The buffer output (pin 7) is coupled to the second ALBO circuit with C4. The use of two ALBO filters provides an advantage in filter performance, however this advantage is also accompanied by an overall increase in signal attenuation. Care must be exercised in both circuit design and in circuit board layout to prevent noise from being coupled into the data signal especially prior to the preamplifier. The 6 dB buffer has a low output impedance, however the load placed on the output should be greater than 600 ohms to minimize distortion.



NOTES: UNLESS OTHERWISE SPEC
1. All capacitors are μF
2. All resistors are ohms

Figure 11. T1 Circuit Schematic

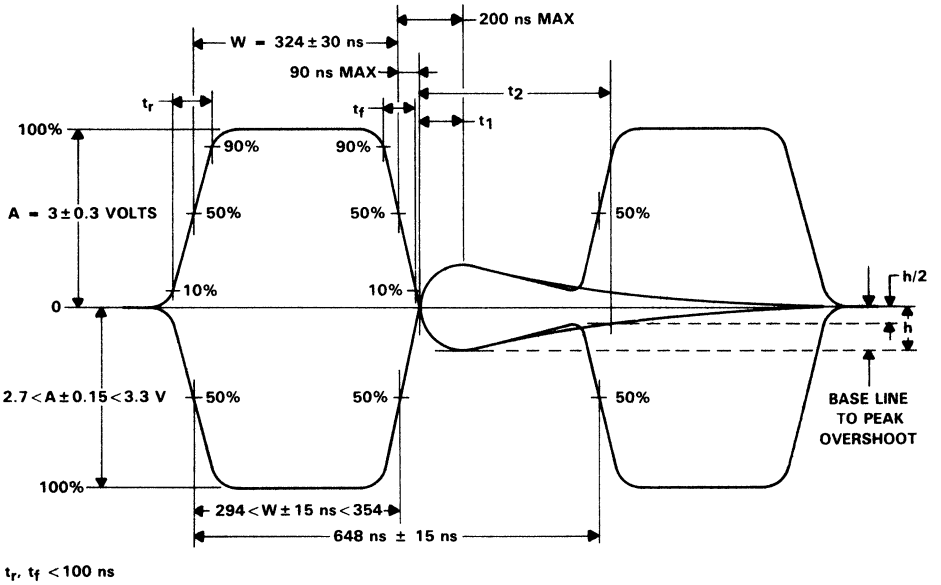


Figure 12. Output Pulse Requirements[5]

Preamplifier

The preamplifier with adjustable gain compensates for signal loss due to transmission line and filter circuits. Resistor R13 sets the preamplifier gain and is chosen to provide a 480 mV peak-to-peak signal at pin 14 when the transmission line attenuation is maximum (35 dB).

Equalizer

The equalizer filter is located between the preamp output and pin 14. It is designed to accommodate the nominal length transmission line. The equalizer and ALBO filters combined transfer function should provide a flat attenuation to a frequency greater than one-half the data clock f_{clk} (refer to Figures 7 and 13). Typically, the system response should be flat to at least 0/7 f_{clk}. The equalizer filter response should be a peak with the peak at the resonant frequency f_0. The response for frequencies below f_0 should be the complimentary function of the nominal transmission line. From Equation 1; f_0 is 1.29 MHz and from Equation 2; we can see that the filter peak is well above one-half f_{clk}. Equation 3 describes the filter attenuation for frequencies below $f_0/10$. Equation 4 describes the attenuation at f_0 and Equation 5 describes the attenuation above $10F_0$. The ratio of L and C determine the slope of the transfer function with the resistor values providing the attenuation levels.

$$f_0 = \frac{1}{2\pi\sqrt{L_3 C_{10}}} = 1.29 \text{ MHz} \quad (1)$$

$$\frac{f_0}{f_{clk}} = \frac{1.29 \text{ MHz}}{1.544 \text{ MHz}} = 0.8 \quad (2)$$

For $f = \frac{f_0}{10}$

$$\frac{V_{out}}{V_{in}} \simeq \frac{R16}{R16+R14} \simeq 0.152 \ (-16.4 \text{ dB}) \quad (3)$$

For $f = f_0$

$$\frac{V_{out}}{V_{in}} \simeq \frac{R16}{R16+R15} \simeq 0.595 \ (-4.5 \text{ dB}) \quad (4)$$

For $f = 10f_0$

$$\frac{V_{out}}{V_{in}} \simeq \frac{R16}{R16+R14} \simeq 0.152 \ (-16.4 \text{ dB}) \quad (5)$$

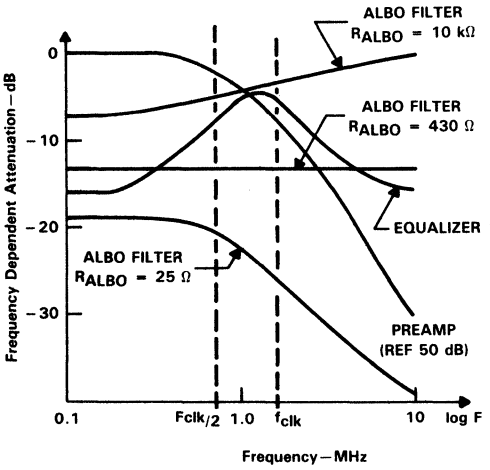


Figure 13. Filter Responses

Peak Detector

Networks C20, R17, C21, and R18 are used to store the outputs from the peak detectors. The values of both networks should be the same. The time constants of these circuits determine how quickly the receiver can respond to changing signal conditions. The time constant of this network needs to be relatively long (typically 10 ms) compared to the received signal to prevent oscillation.

Mute Output

The MUTE circuit compares the averaged peak signal amplitudes to 33% of the nominal (480 mV peak-to-peak) amplitude. When the received signal falls below the 33% reference, the MUTE output transistor is turned off (logic high) to indicate loss of data signal. The peak detector circuit time constant determines the delay time between loss of received signal and the MUTE output. The current on this output should be limited to 1 mA.

Clock Recovery

The clock recovery circuit is an LC tuned circuit. The transformer T3 is designed to resonate at 1.544 mHz with a 150 pF capacitor across the primary. The capacitor should be a high quality capacitor with a low temperature coefficient. Resistor R21 is chosen to lower the circuit Q to between 80 and 100 in order to conform to the T1 specification; the transformer Q with the secondary open is approximately 190. Clock recovery circuit Q will directly influence clock jitter. Capacitor C13 adjusts the phase of the recovered clock relative to the data.

Transformer Design: The clock recovery transformer must be designed with minimum primary to secondary capacitance and with attention given to making both halves of the secondary winding symmetrical.

T1 Board Adjustment Procedure (see Figure 11)

Adjustment:

1. Connect a transmission line (maximum of three feet) between the LINE IN (J1) jack and the LINE OUT (J2) jack.
2. Connect 5 V to the J7A jack and 5 V return to the J7B jack.
3. Apply a 1.544 MHz TXCK to the CLK IN (J3) connector.
4. Apply a T1 carrier signal with an all "ones" data pattern to the DATA IN (J4) connector.
5. With the oscilloscope externally triggered on the T1 carrier word, adjust transformer T3 for the maximum peak-to-peak signal at TCM2203 U1 pin 28.
6. Change the carrier data pattern at J4 to a "one" followed by 15 "zeroes".
7. Trigger the oscilloscope on the RXCK waveform at TCM2203 U1 pin 22.
8. Readjust transformer T3 the minimum amount necessary to minimize the jitter on RXCK at TCM2203 U1 pin 22.
9. Connect the oscilloscope probes to TCM2203 U1 pin 14 (AMPL IN) and U1 pin 22 (RXCK).
10. Retrigger the oscilloscope on the T1 carrier word.
11. Adjust C13 until the falling edge of RXCK coincides with the peak amplitude of the received data pulse at AMPL IN.

SUMMARY

The TCM2203 Line Interface Circuit along with the TCM2222 transcoder are excellent choices for designing PCM data transmission systems. The chip architecture is modular allowing for numerous system configurations. The circuit described uses two ALBO filters and an Equalizer. However, a single ALBO filter can be used alone or in conjunction with a resistive attenuator connected to the other ALBO pin. The adaptive data and clock thresholds provide excellent noise immunity and minimize clock jitter.

Circuit design should incorporate:

1. Adequate power supply decoupling.
2. Ground plane construction to minimize noise.
3. Physical isolation of the receive and transmit components.

This circuit involves both digital signals and high frequency ac signals. System design should also consider rf radiation restrictions.

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TISP Series
Transient Suppressors

TEXAS
INSTRUMENTS

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Contents

Page

INTRODUCTION 4-41

BASIC CHARACTERISTICS 4-41
- CONSTRUCTION 4-41
- OPERATION 4-42
- EQUIVALENT MODEL 4-42
- MODEL ANALYSIS 4-43
  - Definition of Symbols 4-43
  - Voltage Below V_Z 4-44
  - Avalanche Region 4-44
  - Breakover 4-44
  - Regenerative Condition 4-46
  - Negative Voltages 4-46

DEFINITION OF DC PARAMETERS 4-47
- DEVICE CHARACTERISTICS 4-47
  - TISP1XXX 4-47
  - TISP2XXX 4-48
  - TISP3XXX 4-49
- ON-HOOK CONDITIONS 4-50
- RINGING CONDITIONS 4-50
  - Battery-Backed Ringing 4-51
  - Ground-Backed Ringing 4-52
  - Balanced Ringing 4-53
- TEST ACCESS 4-54
- MINOR TRANSIENTS 4-54
- SLIC ONLY PROTECTION 4-54
- HOLDING CURRENT I_H 4-55

AC LINE CONTACT CONDITIONS 4-56
- DESIGN CONSIDERATIONS 4-56
- CONFIGURATION 4-57
- THE PROTECTION NETWORK 4-58
  - Fuses 4-59
  - PTC Thermistors 4-59
  - Transient Suppressor 4-61

Contents (Continued)

	Page
AC GENERATOR	4-62
Graphical Analysis	4-62
RMS Generator Current	4-64
SYSTEM EFFECTS OF GENERATOR PEAK VOLTAGE AMPLITUDE	4-64
$\sqrt{2} \times V_{GEN} < V_Z$, TISP2XXX and TISP3XXX Families	4-64
$\sqrt{2} \times V_{GEN} < V_Z$, TISP1XXX Family	4-65
$\sqrt{2} \times V_{GEN} > V_Z$, TISP2XXX and TISP3XXX Families	4-66
$\sqrt{2} \times V_{GEN} > V_Z$, TISP1XXX Family	4-66
ANALYSIS OF FUSE PROTECTED SYSTEMS	4-66
ANALYSIS OF PTC PROTECTED SYSTEMS	4-68
SUMMARY	4-70
REFERENCES	4-71

List of Illustrations

Figure	*Title*	*Page*
1	Typical Applications Circuits	4-42
2	Two Transistor Analogy of the Thyristor	4-43
3	Circuit Analogy for Avalanche Conditions	4-44
4	Circuit Analog for Breakover Conditions	4-45
5	Circuit Analog for Holding Current Condition	4-46
6	TISP1XXX Characteristics	4-47
7	TISP2XXX AC, BC, and AB Characteristic	4-48
8	TISP3XXX Characteristics	4-49
9	Battery-Backed Ringing Circuit	4-51
10	Ground-Backed Ringing Circuit	4-52
11	Balanced Ringing Circuit	4-53
12	SLIC Only Protection Circuit	4-54
13	TISP2290 Normalized Holding Current Versus Junction Temperature	4-56
14	AC Line Contact Testing	4-58
15	Protection Network	4-58
16	Typical Fusing Characteristic	4-59
17	PTC Resistance Versus Temperature	4-60
18	PTC AC Resistance Locus Versus Temperature	4-61
19	Voltage Generator Load Line and Waveforms	4-62
20	TISP2XXX and TISP3XXX AC Line Contact Conditions	4-65
21	TISP1XXX AC Line Contact Conditions	4-66
22	RMS Current Versus Time for Fuse Protection	4-67
23	RMS Current Versus Generator Resistance	4-68
24	RMS Current Versus PTC Resistance	4-69
25	RMS Current Versus Average Suppressor Power	4-70

Introduction

The rapid growth of the semiconductor content in telephone systems has dramatically altered the kind of protection required against such hazards as lightning and accidental connection to ac lines. Protection methods developed for the previous generation of exchange interfaces and subscriber sets are no longer adequate. New protection devices must offer faster response, well defined voltage levels, reliable operation, and no interference with normal system operation.

Texas Instruments has developed three families of transient suppressors that cover the most common subscriber line interface circuit (SLIC) configurations. These bidirectional devices provide shunt protection against transient static voltages between the wires of an exchange pair or from either wire to ground. In addition, they are capable of providing protection against damage from induction from, or even accidental connection to, some kinds of ac sources.

This report describes the important characteristics of the TISP1XXX, TISP2XXX, and TISP3XXX families of transient suppressors, defines the dc parameters, and discusses the various system stresses under ac line contact testing.

Basic Characteristics

Construction

The successful and reliable operation of any protection system depends to a large extent on the design and fabrication of the components used. The active part of the TISP transient suppressor is a silicon chip structured with alternate layers of P and N type material. The chip is fabricated using Texas Instruments Ion-Implanted Planar (I^2P) process which permits precise control of the electrical characteristics, extremely stable parameters, and the monolithic integration of two bidirectional suppressors on a single chip.

The chip's back surface has a multimetal system deposited on it to ensure good contacting and solderability. In assembly, the back is soldered to a plated copper tab which acts as the common connection for the two suppressors and provides a thermal path for heat losses to the external ambient. Two soldered connections are made to the chip's top surface metallization pattern to bring out the active suppressor leads. A third central lead is soldered and keyed to the copper tab to provide the common connection. All the leads are formed from punched and plated 0,38 mm copper strip. The chip is protected against mechanical and environmental damage by a nonflammable plastic cap which is filled with epoxy.

Operation

The TISP series of shunt protectors are breakover-voltage-triggered, high-holding-current, bidirectional devices (Figure 1). Voltage transients are initially clipped by avalanche action until the protector current rises to the breakover level, which causes the device to trigger to the "on" state. Spurious triggering is avoided by ensuring the breakover current is greater than 150 mA and the dv/dt rating is better than 5 kV/μs. After breakover, the protector's low voltage condition allows it to sink very large currents without incurring the temperature and voltage rise of conventional "zener" protectors. A high holding current, which is greater than 150 mA at 25°C and 100 mA at 70°C, avoids system dc latch-up as the transient subsides.

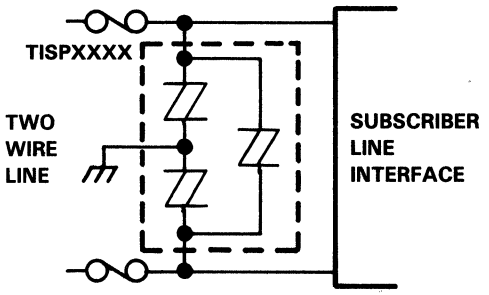


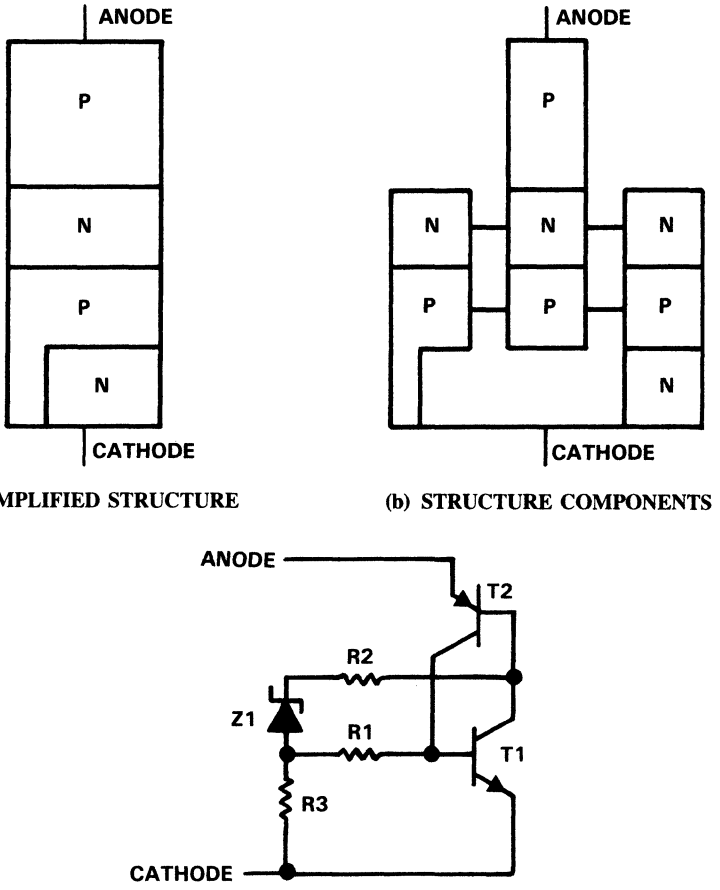
Figure 1. Typical Applications Circuit

The high thermal mass of the TO-220 package copper tab strongly contributes to the device protection performance with short- and medium-duration transients. Long-term transients, such as shorts to outside voltage supplies, can be protected against by the use of fuses or positive temperature coefficient (PTC) thermistors to terminate or reduce the fault current.

Under normal operating conditions, the TISP series presents negligible loading on the telephone line due to its very low leakage planar construction and precise avalanche voltage.

Equivalent Model

Each protector section consists of two opposing thyristors connected in parallel to give bidirectional operation. It is sufficient to analyze only one thyristor in the appropriate polarity as the two thyristors are almost symmetrical in structure. Figure 2 shows how the PNPN thyristor structure can be segmented into a PNP transistor, T2, and an NPN transistor, T1, with a common collector-base junction. Triggering occurs by collector-base junction avalanche breakdown depicted in the equivalent circuit by zener diode Z1 and the normal slope resistance R2. The thyristor's P gate region is shorted by the cathode metallization to produce a low-value resistance, the equivalent shown as resistors R1 and R3 across the NPN transistor's base-emitter junction to give the thyristor its high holding current.



(a) SIMPLIFIED STRUCTURE

(b) STRUCTURE COMPONENTS

(c) CIRCUIT EQUIVALENT

Figure 2. Two-Transistor Analog of the Thyristor

Model Analysis

This analysis is extremely simplistic and is only intended to provide an overview of the device's operation to enable designers to estimate how it will interact with system voltage and current conditions.

Definition of Symbols

V_{BE1} — Transistor, T1, base-emitter voltage
V_{BE2} — Transistor, T2, base-emitter voltage
V_Z — Zener diode avalanche voltage
$\alpha 1$ — Transistor, T1, alpha current gain
$\alpha 2$ — Transistor, T2, alpha current gain

Voltages Below V_Z

As the voltage is increased from zero, the only current flowing will be due to junction and surface leakage, which will be very small. Data sheet measurements of leakage are performed at the typical dc voltage level of −50 V.

Avalanche Region

When the applied voltage exceeds $V_Z + V_{BE2}$, the thyristor will start to conduct. The onset of the avalanche region is defined as the voltage developed across the suppressor at a current level of 1 mA. At a current level of I_X, the terminal voltage, V_X, in Figure 3 will be:

$$V_X = V_{BE2} + V_Z + I_X(R2 + R3)(1 - \alpha_2) + R3I_X\alpha_2$$

giving

$$V_X = V_{BE2} + V_Z + I_X[R3 + R2(1 - \alpha_2)]$$

Differentiating this with respect to I_X gives the avalanche slope resistance, R_A, which is:

$$R_A = R3 + R2(1 - \alpha_2)$$

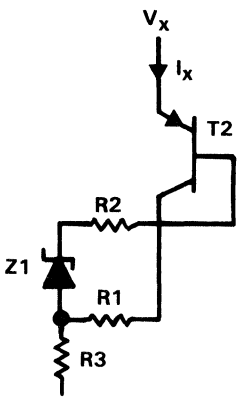


Figure 3. Circuit Analogy for Avalanche Condition

Experienced transistor users might have expected the PNP transistor, T2, to avalanche initially at $BV_{BE2} + BV_{CBO2}$, breaking back to BV_{CEO} as the current increased. In practice, this effect is negligible, because to block in the negative direction transistor T2 must be implemented with a low gain, α_2, which results in the two breakdown voltages being almost equal.

Breakover

The avalanche characteristic terminates with the regenerative turn-on of transistors T1 and T2. This initiates when the voltage drop across resistors R1 and R3 in Figure 4 reaches V_{BE1} at a current level of I_{BO}.

Thus:

$$V_{BE1} = I_{BO}R3 + I_{BO}\alpha_2 R1$$

giving

$$I_{BO} = \frac{V_{BE1}}{R3 + \alpha_2 R1}$$

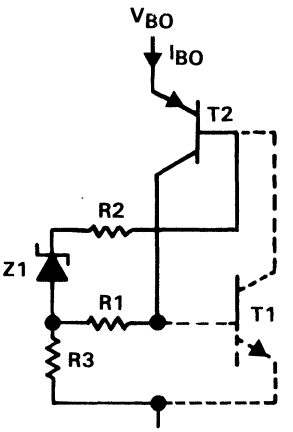


Figure 4. Circuit Analogy for Breakover Condition

The breakover voltage level, V_{BO}, will be the value of V_X when $I_X = I_{BO}$. Substituting and simplifying gives:

$$V_{BO} = V_{BE2} + V_Z + \frac{V_{BE1}[R3 + R2(1 - \alpha_2)]}{R3 + \alpha_2 R1}$$

The above equation predicts the voltage excursion from initial avalanche to breakover will be:

$$\frac{V_{BE1}[R3 + R2(1 - \alpha_2)]}{R3 + \alpha_2 R1}$$

When the suppressor triggers "on", its current will greatly increase, ensuring that regeneration is maintained. Consider a voltage source, V_S, and internal resistance, R_S, at breakover.

$$V_S = V_{BO} + I_{BO}R_S$$

Neglecting the thyristor "on" voltage drop, the crowbar current, I_{TM}, will be:

$$I_{TM} = \frac{V_S}{R_S} = I_{BO} + \frac{V_{BO}}{R_S}$$

This is the initial crowbar current. In cases where V_S is time variant, much higher current values can be achieved later in the suppression cycle. The 5 A "on" voltage level is specified as 3 V maximum for TISP series devices.

Regenerative Condition

After breakover has occurred, the transistors will remain in conduction until the current drops to a critical value called the holding current, I_H, whereupon regeneration stops and the transistor pair delatches. If the system continues to supply current with sufficient voltage compliance, the voltage will rise until it is limited by the avalanche characteristic. The base current available to drive transistor T1 in Figure 5 is:

$$\alpha_2 I_H - \frac{V_{BE1}}{R1 + R3}$$

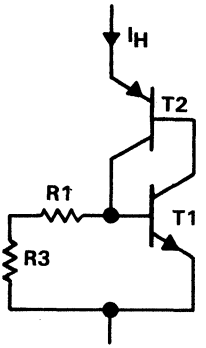


Figure 5. Circuit Analogy for Holding Current Condition

Its base current requirement to maintain regeneration is:

$$\frac{I_H(1 - \alpha_2)(1 - \alpha_1)}{\alpha_1}$$

When these two values are equal, regeneration is just maintained. Setting these two equations equal and simplifying gives:

$$I_H = \left(\frac{V_{BE1}}{R1 + R3}\right)\left(\frac{\alpha_1}{\alpha_1 + \alpha_2 - 1}\right)$$

Because the alpha current gain of the NPN transistor, T1, will be close to unity, the holding current equation may be approximated to:

$$I_H = \frac{V_{BE1}}{(R1 + R3)\alpha_2}$$

Negative Voltages

Reverse voltages are blocked by the reverse biased base-emitter junction of PNP transistor, T2, and the only current flowing will be due to junction and surface leakage.

The reverse breakdown voltage of the base-emitter junction is designed to be higher than the breakover voltage so that the opposing thyristor limits the voltage in the negative polarity.

Definition of DC Parameters

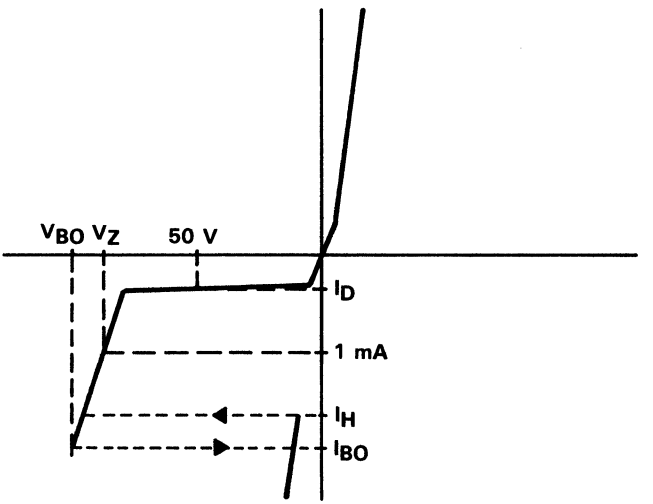
Device Characteristics

The two outer TO-220 package leads, each connected to a line wire, are termed A and B. The center lead, termed C, is the ground connection. Thus, wire-to-ground voltages are V_{AC} and V_{BC}, and the wire-to-wire voltage is V_{AB}.

TISP1XXX

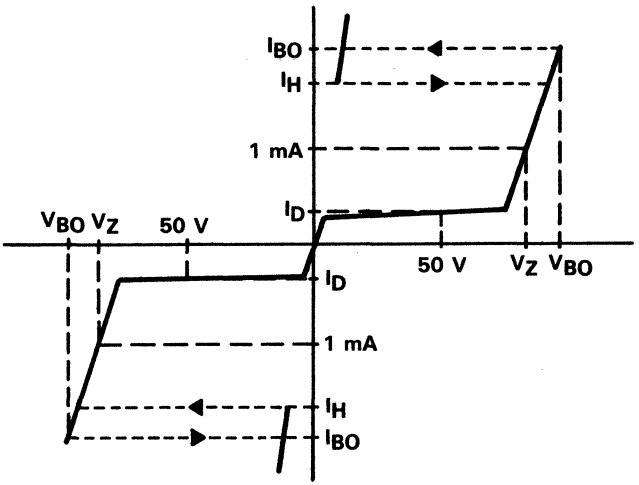
Figure 6(a) shows the wire-to-ground characteristics of the TISP1XXX family of suppressors. For positive voltages, the devices have a forward biased diode characteristic. The negative characteristic is that of a voltage-triggered thyristor. For this report, the relevant measurement points on this characteristic are:

I_D — The leakage current at the test voltage V_D
V_Z — The initial clipping or avalanche voltage measured at 1 mA.
I_{BO} — The current level (pulsed) at which the device triggers to the "on" state.
I_H — The current at which the device triggers back to the "off" state.



(a) AC AND BC CHARACTERISTIC

Figure 6. TISP1XXX Characteristics



(b) AB CHARACTERISTIC

Figure 6. TISP1XXX Characteristics

Figure 6(b) shows the wire-to-wire, symmetrical, voltage-triggered thyristor characteristic of the TISP1XXX family. These devices start to clip wire-to-wire and negative wire-to-ground voltages at V_Z.

TISP2XXX

Figure 7 shows the symmetrical, voltage-triggered thyristor characteristic of the TISP2XXX family of suppressors. At the current levels being considered, there is little

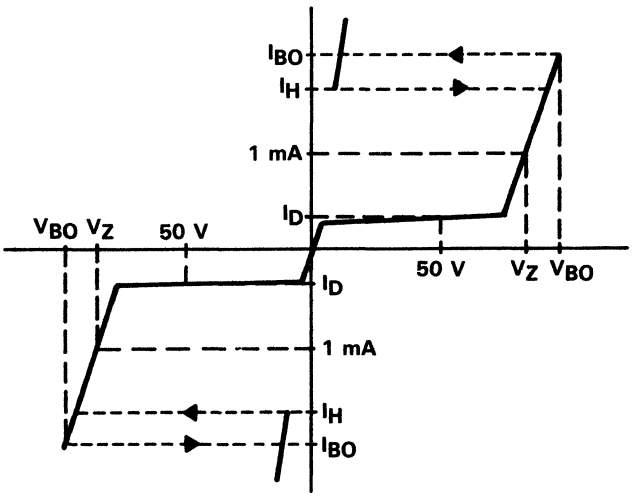
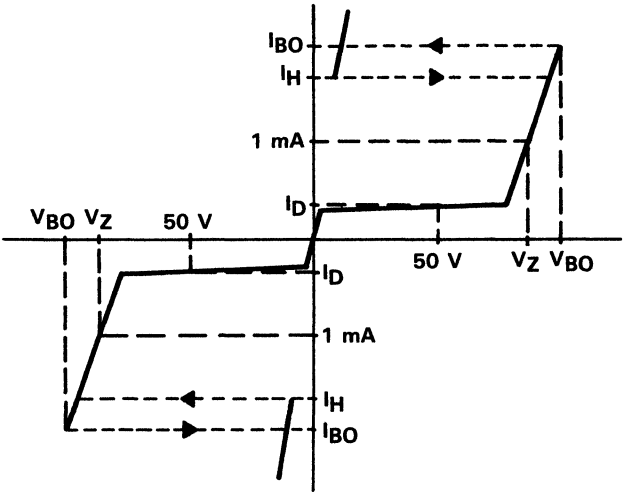


Figure 7. TISP2XXX AC, BC, and AB Characteristics

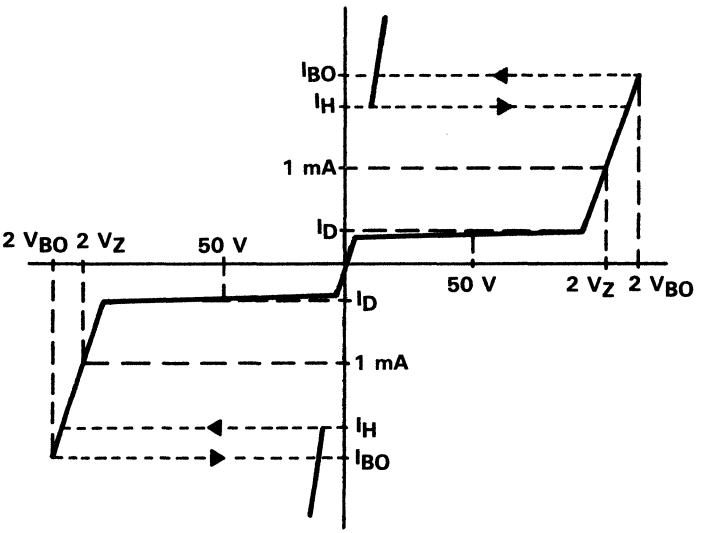
difference between the wire-to-ground and the wire-to-wire characteristics. Thus, these devices start to clip both wire-to-ground and wire-to-wire voltages at V_Z.

TISP3XXX

Figure 8(a) shows the wire-to-ground, symmetrical, voltage-triggered thyristor characteristic of the TISP3XXX family of transient suppressors. In this respect, it is the same as the TISP2XXX family. The difference between the two families occurs in the



(a) AC AND BC CHARACTERISTICS



(b) AB CHARACTERISTIC

Figure 8. TISP3XXX Characteristics

wire-to-wire characteristic. Figure 8(b) shows the TISP3XXX devices start to clip wire-to-wire voltages at $2V_Z$. Although the suppressors are monolithically integrated into a single chip, the TISP3XXX devices provide the same functionality as two bidirectional single-wire suppressor chips with a common ground connection.

On-Hook Conditions

When the telephone is on hook, its dc line loading is negligible. Typically, one wire of the line would be close to ground potential and the other wire would be at the line driving source potential, normally about −50 V (the exchange battery).

Under these conditions, the dc line loading is limited to a current value which will not activate the dc off-hook detection circuit. Loading values of several mA are often permissible, and it would be reasonable to allow 20% of this for suppressor leakage under worst case conditions, e.g., 0.5 mA.

The suppressor leakage current increases with temperature, and its value is the sum of surface and bulk leakages. The significance of any particular component will depend on the temperature and the family being considered. Under normal conditions, the device junction will be almost the same as the local ambient. The example given of 0.5 mA and 50 V would cause a junction-to-ambient differential of about 1.5°C (0.5 mA × 50 V × 62.5°C/W). If the maximum exchange temperature were 70°C, the required specification would be:

$$I_D < 500\ \mu A \quad T_{CASE} = 71.5°C,\ V_D = -50\ V$$

In practice, consideration also needs to be given to the off-hook detection circuit to determine the effective system leakage current of the suppressor. Ideally, it should only monitor the dc flowing wire-to-wire (I_{AB} is a guarded three terminal measurement). Typically, wire-to-ground leakage will also contribute to the monitored current. For example, the Texas Instruments European SLIC IC system would sense an effective current $I_{AB} + (I_{AC} - I_{BC})/(2)$ (all these currents are quoted as three terminal guarded measurements). In this situation, the most prudent way to specify the leakage current measurement is with the third (floating) terminal connected to the most positive potential to maximize the leakage. Thus, if the the current through A and B were to be measured with A negative, it would be $-I_{AB/C}$, and if B were negative (A positive), then it would be $-I_{BA/C}$.

Ringing Conditions

It is normal to apply (battery) dc voltage as well as the ring voltage to the line during the ringing condition. There are several ways in which this can be implemented, and the most common configurations are examined in the following subsections. The maximum battery voltage is designated V_{BATM} and the peak of the maximum ringing voltage $V_{RINGPKM}$. It is assumed that ringing conditions cause the greatest voltage excursions in normal operation and so set the voltage limits.

Battery-Backed Ringing

In the configuration of Figure 9, one wire has the series combination of battery and ring generator applied to it while the other wire is returned to ground. If the line is unloaded (worst case condition) only one terminal of the suppressor will be exercised, the other being at 0 V. Clearly in this arrangement, the maximum voltage wire-to-wire will be the same as the wire-to-ground and the TISP2XXX family, with its completely symmetrical characteristics, will give the most effective suppression.

The maximum negative voltage will be $V_{BATM} + V_{RINGPKM}$ and the maximum positive voltage will be $V_{RINGPKM} - V_{BATM}$. In this case, the negative excursion dominates and defines the value of avalanche voltage V_Z to avoid peak clipping.

Clipping would not normally reduce the ringing power significantly and, typically, insufficient current ($< I_{BO}$) is available to trigger the suppressor and grossly distort the negative peaks. Clipping needs to be avoided to remove the possibility of false off-hook detection. This could occur because clipping causes partial rectification of the ringing voltage, resulting in a net circuit dc which is then interpreted by the off-hook detector as the telephone handset being picked up. Temperature effects on voltages have been taken into account for the suppressor avalanche, V_Z, the battery, and the ring generator. Normally, the quoted battery and ring generator levels comprehend the exchange temperature variation. The temperature coefficient of avalanche breakdown, S_Z, is about 0.1%/°C. Thus, to cover operation down to a minimum exchange temperature of T_{MIN}, the required 25°C avalanche voltage, V_Z, would be:

$$V_Z = \frac{V_{BATM} + V_{RINGPKM}}{1 + \frac{T_{MIN} - 25}{1000}}$$

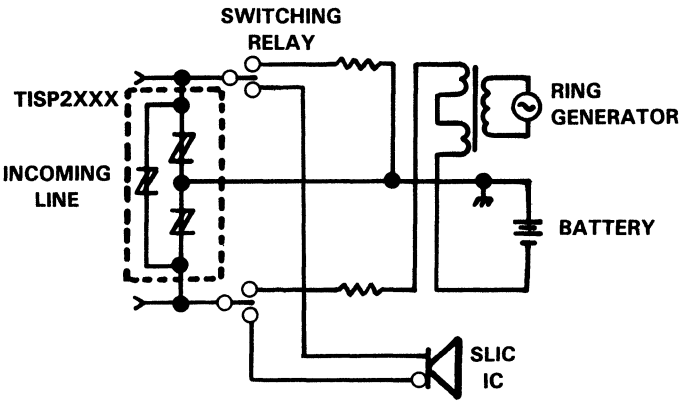


Figure 9. Battery-Backed Ringing Circuit

If, for example, $V_{BATM} = -58$ V and if the ringing voltage were 95 V_{RMS}, then the minimum avalanche voltage, V_Z, should be:

$$V_Z = 58 + (\sqrt{2} \times 95) = 192 \text{ V}$$

For a minimum exchange temperature of −15°C, the 25°C measurement becomes:

$$V_Z = \frac{192}{1 + \frac{-15 - 25}{1000}} = 200 \text{ V}$$

When the effects due to line and bell loading are taken into account, this typically results in 5% to 10% extra safety margin in clipping level.

Ground-Backed Ringing

In the configuration of Figure 10, one wire has the battery connected to it and the other has the ground referenced ring generator. In the unloaded case, the peak voltages on the wires will be $-V_{BATM}$ on the battery wire and $\pm V_{RINGPKM}$ on the ring generator wire. Usually the ringing voltage will be the largest and will set the wire-to-ground avalanche requirement. However, the wire-to-wire voltage will be greater than this, being $V_{BATM} + V_{RINGPKM}$, necessitating the use of a TISP3XXX series device which has a wire-to-wire rating of $2V_Z$.

Taking the values used in the battery-backed ringing case gives a 25 °C value of V_Z wire-to-ground of:

$$V_Z = \frac{V_{RINGPKM}}{1 + \frac{T_{MIN} - 25}{1000}} = \frac{\sqrt{2} \times 95}{1 + \frac{-15 - 25}{1000}} = 140 \text{ V}$$

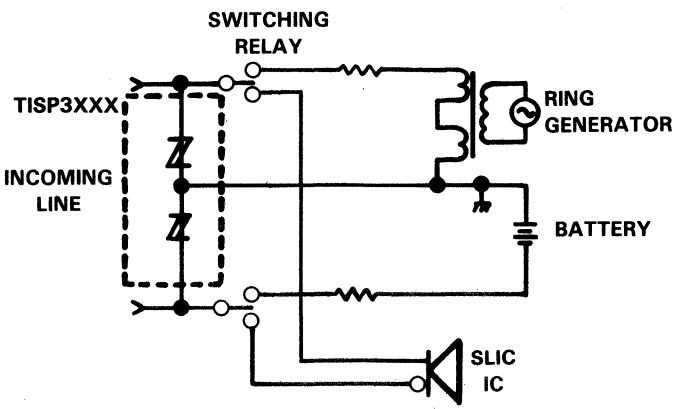


Figure 10. Ground-Backed Ringing Circuit

The peak voltage between the wires will be the sum of the battery and generator voltages, which was found to be 192 V in the previous subsection. Also, the 25°C requirement was found to be 200 V. This is comfortably inside the 2 × 140 = 280 V wire-to-wire avalanche rating that results from the TISP3XXX structure.

Again, the practical effects of line and bell loading increase the clipping safety margin.

Balanced Ringing

In the configuration of Figure 11, the battery is connected to one wire and the ringing voltage is shared equally between the two wires to balance its voltage with respect to ground. The battery wire will have peak voltages of ($V_{RINGPKM}/2$) − V_{BATM} and −($V_{RINGPKM}/2$) + V_{BATM}. The other wire will have ±$V_{RINGPKM}/2$. Between the wires, there will be a peak voltage of: $V_{RINGPKM}$ + V_{BATM}. Allowing for temperature effects gives 25 °C avalanche voltages of:

$$V_Z = \frac{\frac{V_{RINGPKM}}{2} + V_{BATM}}{1 + \frac{T_{MIN} - 25}{1000}}$$

$$V_{Z(AB)} = \frac{V_{RINGPKM} + V_{BATM}}{1 + \frac{T_{MIN} - 25}{1000}}$$

If the earlier example values are substituted, then V_Z > 130 V and $V_{Z(AB)}$ > 200 V. Again, this is an application for the TISP3XXX series of devices.

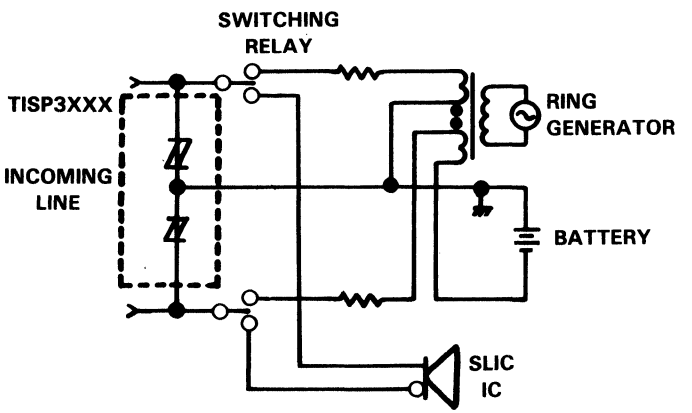


Figure 11. Balanced Ringing Circuit

Test Access

In fault finding and preventative maintenance operations, test signals are applied to the line and SLIC. If the applied voltage levels exceed normal telephone operation, these levels would determine V_Z. Extremely high levels of test signal to the line and correspondingly high V_Z requirements could lead to the loss of adequate SLIC protection. In this situation, the transient suppressor should be connected to the SLIC side of the test access relay so that V_Z can be set by normal system operating levels and SLIC protection maintained.

Minor Transients

The pervasive nature of the telephone network means the possibility of induced transients is very high. While the energy levels of these may not be substantial, they can cause the voltage to rise to a level which makes the suppressor clip. Pulse dialing telephones, which periodically short the line, can, under certain conditions, also cause suppressor clipping. This situation is aggravated by the increasing use of electronic ringers, such as the TCM1506, whose antitapping function is achieved electronically rather than by bell loading. Obviously, the interference level would be compounded if breakover occurred. Under these conditions, a reasonable compromise is to make $I_{BO} = I_H$ for the minimum values.

SLIC Only Protection

Certain integrated SLIC implementations utilize medium-voltage IC technology and cannot be subjected to ringing voltage levels. This is not a major problem, as it is possible to configure the system to switch out the SLIC during the ringing operation. In this case, a transient suppressor on the line would not provide complete SLIC protection. Adequate protection can be achieved by the use of a TISP1XXX transient suppressor connected directly across the SLIC output. This configuration is shown in Figure 12.

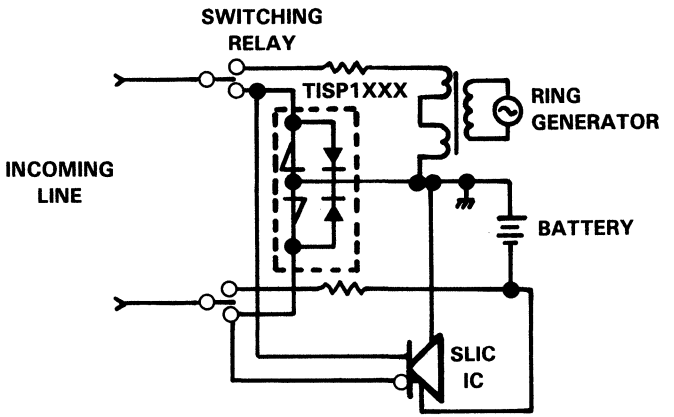


Figure 12. SLIC Only Protection Circuit

Typically, the supply lines to the IC are 0 V and battery. Sometimes, the battery voltage may be boosted to comprehend long lines and an additional +5 V supply used for logic interfacing. The TISP1XXX family of transient suppressors ensures the SLIC is protected against positive voltages by having a forward biased diode characteristic in this direction. In the negative direction, the value of V_Z will be set by the SLIC output swing which will be $V_{BATM} - V_{SAT}$, where V_{SAT} is the saturation voltage of the IC's driver stage. Using the previous values of voltage and temperature and assuming V_{SAT} = 2 V gives a 25°C value of V_Z wire-to-ground of:

$$V_Z = \frac{V_{BATM} - V_{SAT}}{1 + \frac{T_{MIN} - 25}{1000}}$$

$$= \frac{58 - 2}{1 + \frac{-15 - 25}{1000}}$$

$$\approx 58 \text{ V}$$

In operation, both wires of the line will be negative and the wire-to-wire voltage magnitude will be less than the value of V_Z calculated above.

Holding Current I_H

Large single pulse transients will exercise the suppressor in the following manner. When the transient's leading edge reaches the line card, it will override the existing voltages until the suppressor starts to clip. In nondiode cases, once the current in the suppressor exceeds I_{BO}, the suppressor saturates, absorbing the transient current at low voltage.

As the transient current decays, the saturated suppressor will be left carrying whatever current the system can provide. The worst case condition is for negative transients when the suppressor could be left with the line dc feed current, I_{dc} (in the case of a positive transient current, negative dc feed current would actually help to terminate the crowbar action of the suppressor). It is necessary that the suppressor recover from this condition so that normal system operation is resumed. This can be ensured by making $I_{dc} < I_H$ over the system operating temperature range. Although the junction temperature of the suppressor will rise as a result of the transient, it quickly cools back to the system ambient due to the high thermal capacity of the TO-220 copper tab.

The variation of I_H with temperature is not linear, as shown in Figure 13, but up to about 80°C, it is approximately −0.8%/°C. In this range, the resultant 25°C value of I_H can be approximated by:

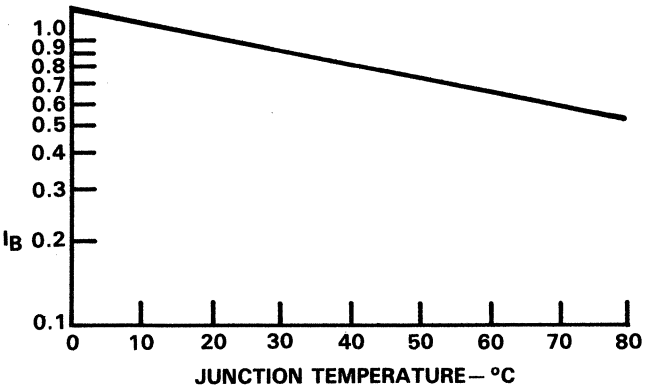


Figure 13. TISP2290 Normalized Holding Current Versus Junction Temperature

$$I_H = I_{dc} / \left[1 - 0.8\left(\frac{T_{MAX} - 25}{100}\right)\right]$$

Using the previous example values and setting, the maximum-high-temperature I_{dc} at 100 mA (for a maximum temperature of 70°C ambient) gives:

$$I_H = 100 / \left[1 - 0.8\left(\frac{70 - 25}{100}\right)\right] = \frac{100}{0.64} \approx 156 \text{ mA}$$

This quantifies the value of I_H expected at 25°C. However, the system designer should specify the exact requirement, i.e., $I_H > 100$ mA at 70°C ambient, rather than an iterated value. If the maximum value of I_{dc} varies substantially with temperature, the minimum holding current requirements should be quoted at several temperatures. This should only be necessary in extreme cases as even the crudest semiconductor current limit is −0.5%/°C and copper coils are −0.4%/°C.

When the suppressor unlatches, there is often sufficient transient energy left to force the suppressor into its avalanche region until all the transient's energy is dissipated. Under these conditions, it is desirable that I_{BO} is comparable with I_H, otherwise there is not a stable dc operating locus and high level oscillations can occur until the current falls below I_{BO} value.

AC Line Contact Conditions

Design Considerations

There can be a great diversity in ac line contact specifications between the various central office and PABX applications. In this introductory note, only the general principles will be addressed rather than specific cases. The Texas Instruments TISP1XXX, TISP2XXX, and TISP3XXX transient suppressor families provide

excellent peak voltage limitation due to their voltage-triggered crowbar action on the low frequency test waveform. This action completely protects the following SLIC against overvoltage. The major parameters of this overvoltage shunt protector will have been set by normal exchange operation, SLIC voltage ratings, and lightning withstand requirements. The ac line contact issues are mainly thermal, in particular, the package dissipation capability.

In contrast, the series overcurrent protector has most of its major parameters defined by normal exchange operation and the ac line contact conditions. It is necessary to understand the interaction of the series and shunt protectors under ac line contact conditions in order to determine the series protector specification. As the interaction depends on the respective specifications, the development tends to be iterative. Generally the loop will be:

1. Choose some appropriate initial values for the series protector.
2. Establish the ac voltage source and resistance values that the protection network and the system can withstand without failure.
3. Compare these with required test levels.
4. Repeat the design exercise until the desired level of protection is achieved.

When failure occurs, even though it may be at test levels far beyond the specification, it should be in a safe manner without creating fumes or flames. Shunt protectors are expected to fail by shorting, and thereby continue to protect the SLIC. In the Texas Instuments TO-220 packaged TISPXXXX transient suppressors, soldered connections are made to the chip, thereby avoiding any possibility of bond wires fusing and creating an open circuit. Consideration has also been given to the current carrying capability of suppressor to SLIC PCB tracking to ensure this does not act as a fuse and open circuit the shunt protection. Certain specifications will concede minor damage during testing, provided it is easily repairable. Generally, this is to cover the use of series fuses in the line for protection.

Configuration

Figure 14 shows a typical SLIC system with the protection, test access, and ringing being separately identified. Depending on the system design requirements, the latter two items could be placed either before or after the protection as described in the Definition of DC Parameters section. The ac line contact generator consists of a defined voltage source, V_{GEN}, and output resistance, R_{GEN}, operating at a frequency which is normally specified as 50 to 60 Hz. The generator values can be singular or defined between maximum and minimum limits.

Testing is done with the generator connected between common (ground) and one or both of the line wires. In some cases, the generator will also be connected between the two line wires. The application period can be continous, periodic, or for a specified time.

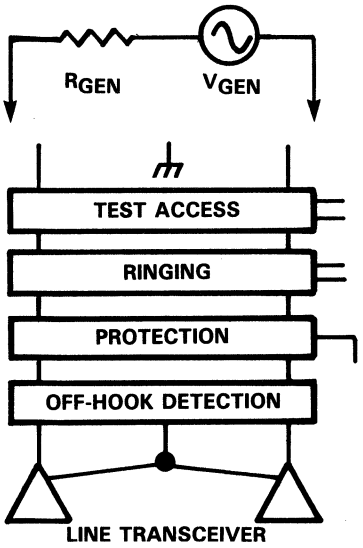


Figure 14. AC Line Contact Testing

The Protection Network

In the protection network, Figure 15, the TISP transient protector provides shunt overvoltage protection, and twin fuses, fusible resistors, or PTC thermistors are used for series overcurrent protection.

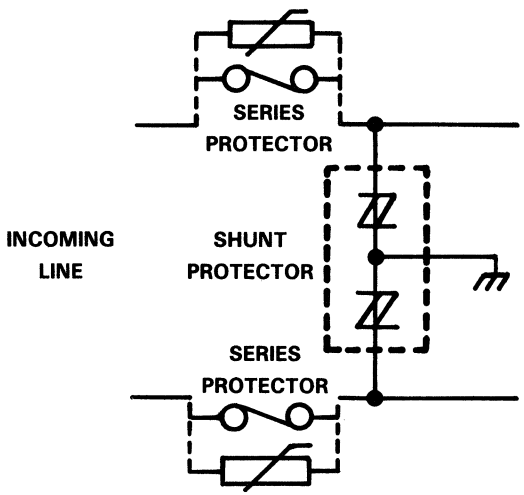


Figure 15. Protection Network

Fuses

A protection policy based on fusing provides the "ultimate" protection for the severest overloads by isolating the equipment, but automatically dictates board rework after an overstress. In this situation, it matters little if it is the fuse which needs replacing due to overcurrent, or the transient suppressor due to overdissipation. Fuse performance can be made relatively insensitive to temperature and be extremely stable in spite of overloads close to the fusing level.

It is imperative that "nuisance" fusing does not occur in normal operation or during the specified lightning test. As a result, the fusing current versus time characteristic tends to be of a TT or T nature (i.e., slow blow, antisurge, or time lag fusing, see Reference 1). For example, a fuse expected to carry 100 mA dc on a continous basis might only be guaranteed to fuse at currents above 250 mA dc. Moreover, for a period of 1 s, currents in excess of 1 A rms could be required to cause fusing. In this situation, it may be possible with certain ac contact tests to set up rms current levels which overdissipate the shunt protector in the long term, causing it to short without blowing the fuse.

Figure 16 shows a typical fusing characteristic. The problem area tends to occur at the longer time periods (> 10 s) where the TISP TO-220 package-to-ambient thermal time constant starts to dominate the maximum suppressor dissipation.

PTC Thermistors

Thermistor based protection systems are intended to recover once the overload is removed. During the ac line contact condition, the rms current, I_{GEN}, flowing through

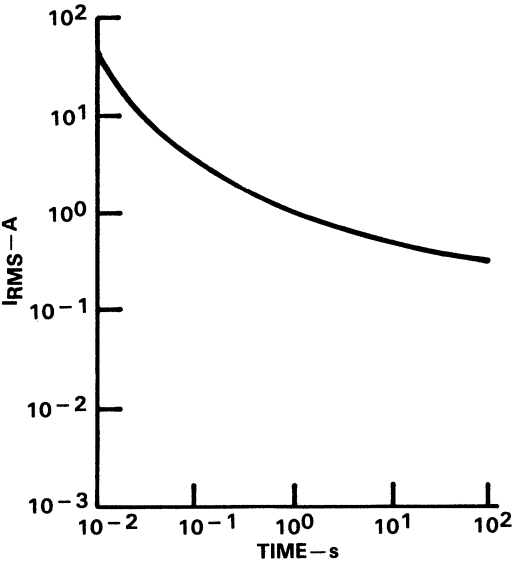


Figure 16. Typical Fusing Characteristic

the thermistor causes heating. When the PTC temperature rises to a critical "switch" temperature, its dynamic resistance starts to increase dramatically as shown in Figure 17 (often four to seven orders of magnitude) reducing I_{GEN}. Finally, an equilibrium is reached where the $I_{GEN}^2 R_{PTC}$ losses are just sufficient to maintain the temperature which corresponds to that value of R_{PTC}. Depending on the overload current level, the reaction time of the PTC can vary from less than a second to several minutes. When the overload is removed, it may take several tens of seconds before the PTC resistance has dropped sufficiently to allow normal system operation.

It is usual for the PTCs to be supplied in pairs with guarantees on matching with age and overload for line balance considerations. It is important that the "switching" temperature is considerably above the maximum exchange ambient temperature to avoid premature "switching" and to lessen the effects of ambient temperature on the overload conditions. Self-heating due to the line dc and voltage drop considerations, leads to typical PTC 25°C resistance values from a few ohms to several hundred ohms.

Determination of the protection circuit operating point is complicated by the PTC's nonlinear resistance-current characteristic, shown in Figure 18. Initially, as the voltage applied to the PTC is gradually increased from zero, the PTC has a constant resistance which is shown by the vertical portion of the characteristic. The linear increase of current with increasing applied voltage continues until the PTC reaches its "switching" temperature and the resistance starts to increase. When this starts to happen, the current level, I_{MAX}, is given by:

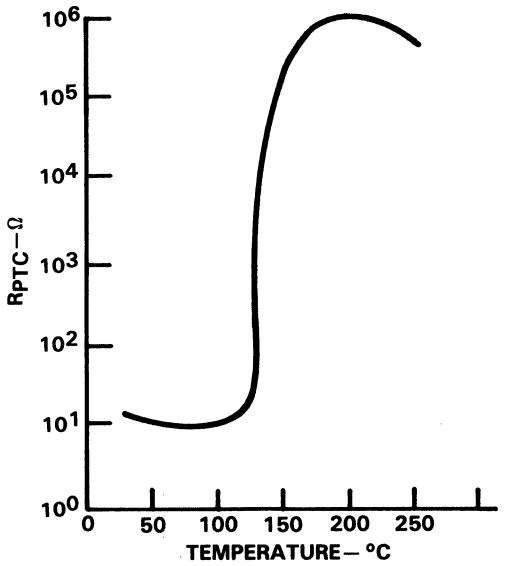


Figure 17. PTC Resistance Versus Temperature

$$I_{MAX} = \sqrt{\frac{T_C - T_{amb}}{R_{PTCamb} \times \theta_{PTC-amb}}}$$

where:

T_C = the "switching" temperature
T_{amb} = the ambient temperature
R_{PTCamb} = the initial PTC resistance
$\theta_{PTC-amb}$ = the PTC's thermal resistance to ambient.

On reaching this condition, further increases in applied voltage result in decreasing current (although the power dissipated by the PTC increases slightly). This condition is shown by the sloping part of the characteristic in Figure 18. Very high continuously applied voltages can cause excessive temperatures to occur. Under these conditions, the PTC's resistance starts to decrease with further increases in voltage, which leads to a rapid increase in dissipated power. Such situations are potentially unstable and could lead to PTC failure.

Transient Suppressor

The major parameters of the TISP transient suppressors were discussed in the first two sections of this report. The major device losses will be caused by operation in the avalanche (zener) region and the saturated (on) condition. The TISP1XXX family has a diode clipping characteristic for positive wire-to-ground voltages that maximizes the positive half cycles in the series protector. This enhances the series protector operation when compared with the symmetrical TISP2XXX and TISP3XXX families, which will inhibit current flow until the avalanche level, V_Z, is exceeded.

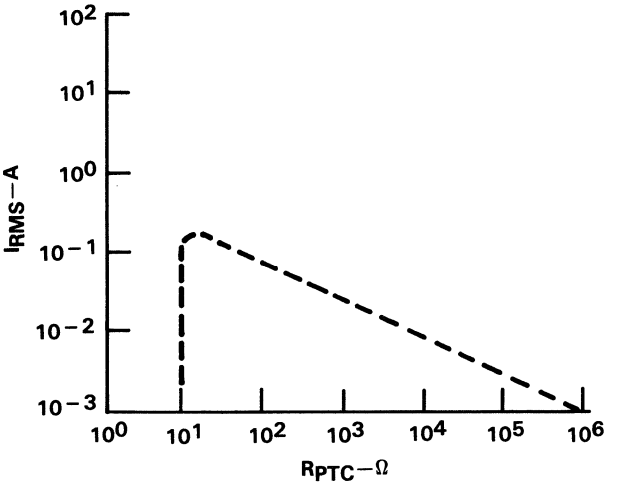


Figure 18. PTC AC Resistance Locus Versus Temperature

As far as the transient suppressor heating is concerned, the junction temperature rise will be governed by the chip's thermal capacity for periods below 10 ms, by the substantial TO-220 copper-tab thermal capacity (about 1 Joule/°C) for periods in the 10 s range, and finally by the junction-to-ambient thermal resistance over much longer periods (typically 50°C/W without an external heatsink).

AC Generator

Test specifications generally call up single phase type voltage generators with $0 < V_{GEN} < 250$ V (rms) and source impedances of $4 < R_{GEN} < 2000\ \Omega$. Worst case short circuit current capability is in the range of 6 A to 15 A (rms).

Graphical Analysis

A first pass analysis of the system operating conditions can be made graphically. This will establish the major system parameters and identify sets of conditions warranting more intensive examination. The analysis is simplified by combining the generator source resistance, R_{GEN}, and the series protector resistance together as a single resistance, R_S. If fuse protection is used, the few extra ohms is only significant at very low values of generator resistance (unless the fuse blows, of course). PTCs however, can increase the net resistance, R_S, considerably, sometimes to hundreds of kilohms when heated. Figure 19 shows how the test generator can be considered as a load line, of slope R_S, drawn from a sinusoidally moving point on the horizontal axis of the symmetrical suppressor characteristic, which corresponds to the instantaneous value of generator voltage. For clarity, only the positive quadrant of the characteristic is shown. Specific voltage levels A, B, C, and D are highlighted where the suppressor operation changes or values are maximum.

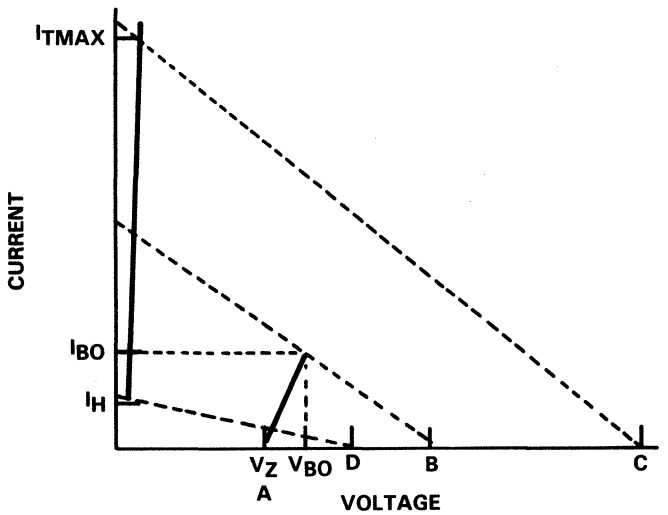


Figure 19. Voltage Generator Load Line and Waveforms

The suppressor starts to clip, causing current flow, when the instantaneous value of generator voltage, denoted by the lower case letters v_{gen}, reaches V_Z at point A.

When point B is reached, breakover occurs and the instantaneous value of the generator voltage, v_{gen}, is:

$$v_{gen} = V_{BO} + I_{BO} \times R_S$$

where V_{BO} and I_{BO} are the suppressor's breakover voltage and current.

For a given value of rms generator voltage, V_{GEN}, the maximum value of source resistance, R_{SCMAX}, which will just initiate breakover is given by:

$$R_{SCMAX} = \frac{V_{GEN}\sqrt{2} - V_{BO}}{I_{BO}}$$

In operation, as the suppressor warms up, the breakover current, I_{BO} will decrease, causing the critical value of source resistance, R_{SCMAX}, to increase. This can lead to situations where the suppressor initially only avalanches rather than triggering due to $R_S > R_{SCMAX}$, resulting in a high suppressor power dissipation but a low rms current. As the suppressor warms up, the decrease in breakover current, I_{BO}, allows the original value of source resistance to initiate triggering. The mean dissipation in the suppressor then drops substantially but the rms current greatly increases, enhancing the potential operation of the series protection. Because of this, the possible rms current range is not a continous spectrum but has a gap between the avalanche and the crowbar modes of operation. This aspect is further considered in the Analysis of Fuse Protected Systems subsection.

In the "on" condition for TISP2XXX and TISP3XXX devices and for the TISP1XXX diode operation, the peak value of suppressor current, I_{TMAX}, caused by the peak value of generator voltage at C will be approximately given by:

$$I_{MAX} = \frac{V_{GEN}\sqrt{2}}{R_S}$$

Point D illustrates the condition where the load line intersects the avalanche characteristic as the holding current is reached and, once delatching occurs, the suppressor clamps for the second time in that half cycle. If the "on" voltage of the suppressor at the holding current, I_H, is V_{TH}, then the critical value of source resistance, R_{SZ}, for this to happen is:

$$R_{SZ} = \frac{V_Z - V_{TH}}{I_H}$$

Usually, in practice, this condition only occurs over a narrow range of generator values. More typically, the unlatching point is reached when the instantaneous generator voltage is below the avalanche voltage, V_Z, and hence a second period of avalanche conduction does not occur.

RMS Generator Current

Because the protection system is nonlinear and temperature sensitive, the calculation or measurement of rms current and power is not straightforward. Based on the above analysis, it is possible to devise a simple computer simulation of the protection system. This model can be used to establish the full range of operating conditions with practical measurements as verification checks.

In the practical tests, true rms meters (rather than those types which scale peak or mean values) should be used. They should have a wide frequency response and large peak-to-rms capability to avoid overload inaccuracies. The rms current due to thermal effects in the protection elements often rapidly changes with time, and some form of data logging system greatly aids the analysis of the series element operating conditions. Oscilloscopes which permit the multiplication of the instantaneous suppressor voltage and current can be used to determine the dissipation levels. Accurate zeroing of the signals is very important to avoid substantial errors because usually one large quantity is multiplied by a much smaller one. In the avalanche region, dissipation can be the product of a high voltage and a small current, while in the saturated condition, it is the product of a low voltage and a typically high current.

System Effects of Generator Peak Voltage Amplitude

This subsection considers the system effects as the generator voltage amplitude is varied from below the transient suppressor avalanche voltage, V_Z, to the maximum available. Only the wire-to-ground test condition will be discussed, but the same general principles, appropriately modified to comprehend the suppressor A-B characteristics, can be applied to the wire- to-wire situation. The discussion will concentrate on the latest generation of "transformerless" SLICs because they are the most susceptible to failure under ac line contact.

$\sqrt{2} \times V_{GEN} < V_Z$, TISP2XXX and TISP3XXX Families

Under these conditions, the transient suppressor will not be exercised at all, but the output stage of the SLIC may be, if connected to the line at that time. Although many of the specifications are not definitive about the SLIC condition during this test, it would be reasonable to examine the situation when the SLIC is in an active-state, driving the appropriate line current into a simulated line impedance, to comprehend any potential service problems.

The reaction of the SLIC to this condition strongly depends on the design implementation. Often, there will be several feedback loops employed to stabilize operating conditions and minimize dissipation. One scenario could be the SLIC control system would interpret the ac line contact as a common mode signal, which it would try to counter by driving an antiphase current.

Another possibility, particularly for unidirectional systems which do not have a sink and source capability on each wire, is that the control loops would be totally overloaded, leading to the output stage switching and driving high peak currents into

the test generator. Both these conditions could lead to abnormally high dissipation in the SLIC output section, leading to device failure. Obviously some form of thermal shutdown incorporated in the SLIC design would guard against this.

The average voltage from the generator is zero and some SLIC loops may treat this test as a resistive load (= R_S) to ground. This condition could then be reasonably safe because wire shorts to ground obviously have to be considered in any SLIC design.

The performance of the system under these conditions is purely a function of the SLIC implementation. It is doubtful that the SLIC will produce rms currents high enough to cause the series protection to operate.

$\sqrt{2} \times V_{GEN} < V_Z$ TISP1XXX Family

The TISP1XXX family has a diode characteristic for positive voltages. Thus most of the current from the generator during the positive half cycle will be shunted to ground. If the SLIC is capable of sinking current from the generator, the ac voltage from the generator system will be displaced by a dc voltage of $I_{LINE} \times R_{GEN}$ in the negative direction. Hence the positive voltage period will be made shorter than the negative voltage period and the TISP1XXX diode will conduct for less than 180° over a complete cycle.

Similar comments on the SLIC operation as in the previous subsection apply, but in this case there is a real chance the series protection elements will operate for source resistances under several hundred ohms, due to the higher rms current caused by the diode clipping.

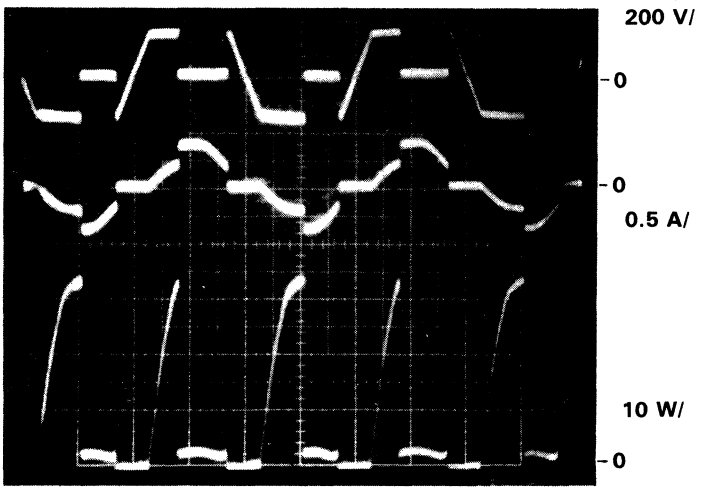


Figure 20. TISP2XXX and TISP3XXX AC Line Contact Conditions

$\sqrt{2} \times V_{GEN} > V_Z$, TISP2XXX and TISP3XXX Families

This situation will result in suppressor conduction if the SLIC is not active. As discussed earlier the reaction of an active SLIC depends on the implementation, but typically it can be expected to introduce asymmetry into the positive and negative clipping of the ac waveform. For simplicity the following assumes the SLIC is inactive.

In this condition, Figure 20, the suppressor will definitely avalanche and depending on the generator values, it may trigger "on" (See Graphical Analysis subsection).

$\sqrt{2} \times V_{GEN} > V_Z$, TISP1XXX Family

In this condition, Figure 21, the positive voltage excursion will be clipped as before when the voltage was less than V_Z. Also the suppressor will avalanche in the negative direction and depending on the generator values, it may trigger "on" (See Graphical Analysis subsection).

Analysis of Fuse Protected Systems

Figure 22 reproduces the fusing characteristic from Figure 16. In this example a fuse resistance of 6 Ω is assumed, a voltage generator range of 0 to 250 V rms, and generator resistance of 4 Ω and 2000 Ω. The TISP transient suppressor rms current capability will vary with the device type, dissipation mode, test generator, circuit configuration used, temperature, and test time. Semiconductor ratings are usually well controlled but obviously the quoted values will be worst case. The suppressor dissipation curves shown dotted are based on a 150-V symmetrical type device. When the source resistance, R_S, is very low the main dissipation is from "on" condition

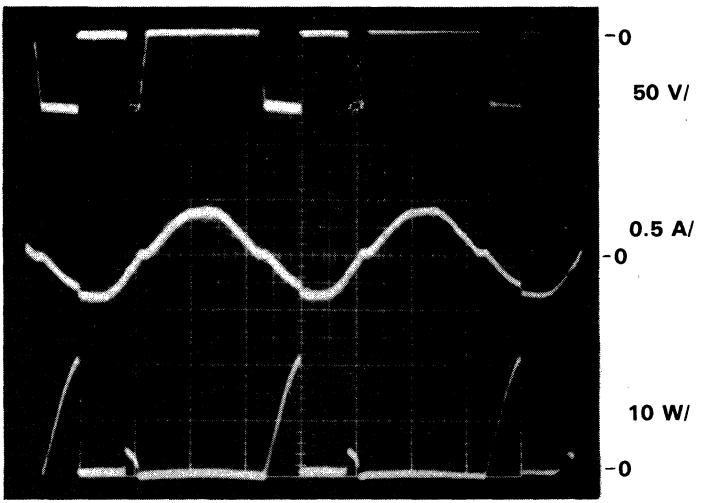


Figure 21. TISP1XXX AC Line Contact Conditions

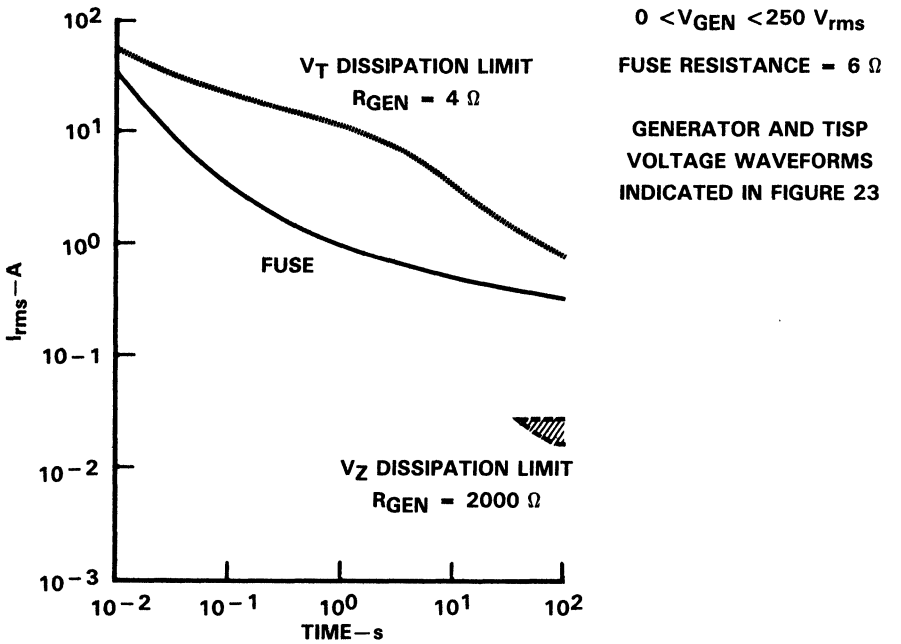


Figure 22. RMS Current Versus Time for Fuse Protection

losses with very little loss from the avalanche mode. Hence this curve can be regarded as generalized for the specified suppressor.

Due to the reasons explained in the Graphical Analysis subsection, high source resistances will greatly restrict the current levels and possibly give excessive dissipation in the avalanche mode. The avalanche dissipation area for this case will be highly specific to generator values and will occur only quite some time after the start of the test. It is also unlikely in this case that a second curve due to "on" condition dissipation limits would be possible due to the very restricted current flow leading to minimal saturated dissipation.

The 4-Ω generator case causes very large currents to flow because the suppressor can easily trigger. As indicated in Figure 23, the current varies between 8 A rms and 24 A rms with the specified generator voltage range. For this range of currents the fusing current is always below the suppressor saturated dissipation limit curve, and the fuse will operate in under 150 ms.

The 2000-Ω generator case severely limits the current. As indicated in Figure 23, a current of 75 mA to 120 mA flows when only avalanching occurs. At higher voltages the suppressor dissipates power in the avalanche and saturated modes. Medium voltages will only dissipate power in the avalanche mode. The worst case power dissipation occurs when the peak current is just below the breakover level. In the short term even this level of power dissipation is acceptable, but often this rms current is insufficient to

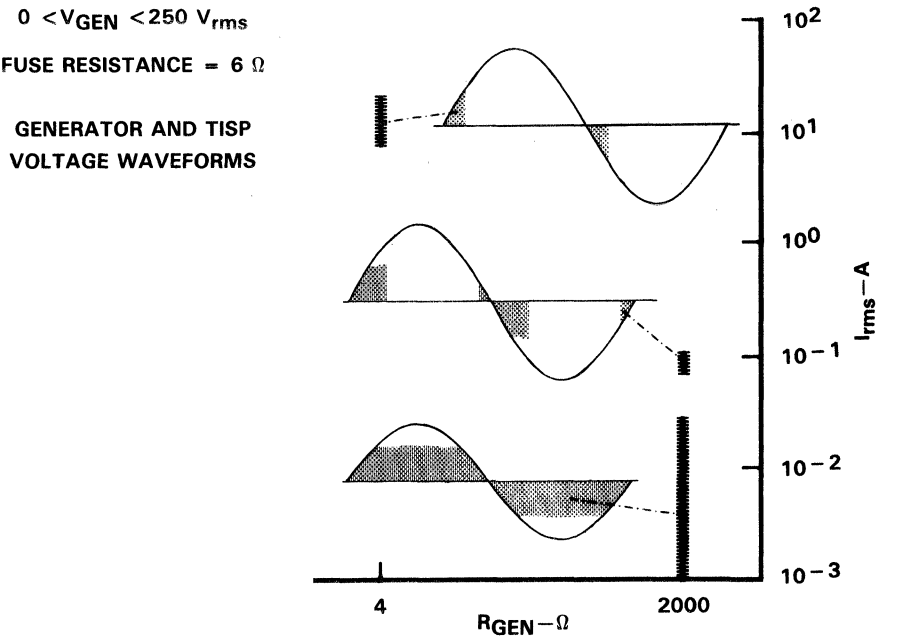


Figure 23. RMS Current Versus Generator Resistance

guarantee fusing. Hence in the longer term (if the generator application is of a continuous nature) then the suppressor could overheat and possibly fail. The time scale for this to happen will be governed by the thermal package-to-ambient parameters and the dissipation level. This creates the " ⌒ " shaped potential failure area in Figure 22 for periods greater than 10 s and the specified generator levels.

This has been a very simplistic analysis of the conditions. Fusing curves are often based on dc tests, however, because the transient suppressor parameters are temperature dependent (principally I_{BO} and I_H) and the rms system current will be changing with time which will modify the fusing characteristic. In addition, fuses, being thermal in nature, will tend to fail at specific points in the ac cycle (Reference 1). Another factor neglected is whether the SLIC is shunting the suppressor and passing additional current through the fuse.

Analysis of PTC Protected Systems

Figure 24 reproduces the PTC characteristic given in Figure 18. Also shown are the rms currents which would flow when a 150-V symmetrical suppressor is used. Curves are shown for minimum, 4 Ω, and maximum, 2000 Ω, generator resistance, R_{GEN} and for two suppressor junction temperatures. The reason for showing device curves for high and low temperatures is that some idea of the working point trajectory can be gained.

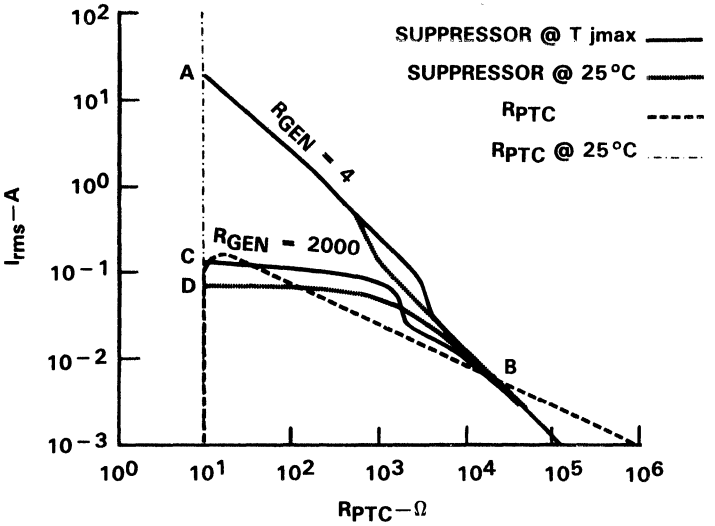


Figure 24. RMS Current Versus PTC Resistance

Initially, the 4-Ω generator resistance combines with the unheated 10-Ω PTC resistance to give the working point A. As the PTC heats up due to the high current, a stable working point is achieved at B. Initially, the suppressor heavily saturates but as the resistance increases a temperature sensitive point is reached when saturation stops. This condition is shown by the step in the suppressor's current characteristic. Although the rms current drops considerably at this point, there is still thermal inequality in the PTC for its dissipated power which is only removed when point B is reached.

When the generator resistance is 2000 Ω, the initial working point is D. This condition is stable for the PTC but the suppressor power loss curves, shown in Figure 25, indicate excessive long term dissipation. As the suppressor warms up, breakover occurs, and dissipation is reduced. A working point which is just stable occurs at C. In practice, due to thermal capacity differences and thermal coupling, the final working point is more likely to be at B.

Although operating end points can be predicted using this method, computer simulation or practical testing is necessary to ensure the devices do not fail during the intermediate period.

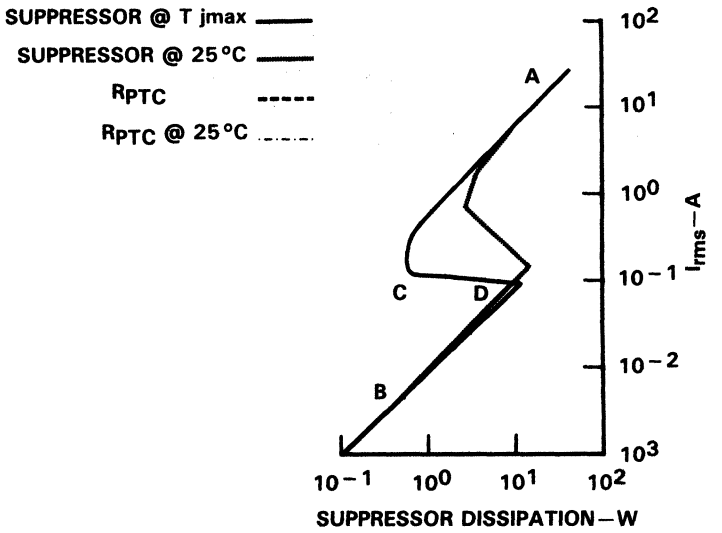


Figure 25. RMS Current Versus Average Suppressor Power

Summary

The TISP transient suppressors provide telephone designers with a new cost-effective way to protect the increasing number of semiconductors, particularly integrated circuits, in their equipment. Specifications for the main dc parameters I_D, I_H, I_{BO}, and V_Z can be determined from system parameters:

1. on-state and off-state line currents
2. on-state line current variation with temperature
3. maximum values of battery and ringing voltages
4. maximum value of test voltages
5. maximum negative voltage voltage of the SLIC.

The example values used in this report represent only typical system requirements.

The basic evaluation techniques for ac line contact shown in this report will identify critical areas for further study. The effects on the system of other shunt elements have been ignored to simplify the presentation at the risk of inaccuracy at high values of source resistance, R_S. Some of the ac data used is not normally specified in this form by the industry, although it is available in other forms. With the increasing popularity of crowbar suppressors, it is hoped that manufacturers will start to provide data in a form compatible with computer analysis and design.

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1. Electric Fuses, A. Wright & P. G. Newbery, Peter Peregrinus Ltd.
2. PTC Materials Technology, 1955-1980, B. M. Kulwicki, Advances in Ceramics, Volume 1, Grain Boundary Phenomena in Electronic Ceramics, 1981, The American Ceramic Society.

Designing with the TCM1500 Bell Tone Ringer/Detector Family

TEXAS INSTRUMENTS

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Contents

Title	Page
INTRODUCTION	4-77
FEATURES	4-77
RINGER FUNCTIONAL DESCRIPTION	4-77
Pin Configuration	4-79
Ringer Output Frequency Options	4-79
Types of Transducers	4-80
Telephone Applications	4-80
Driving a Piezo Transducer	4-80
Driving a Speaker	4-80
Output Characteristics	4-81
Ringer Equivalency Number (REN)	4-81
Tighter Frequency Control	4-83
Additional Applications	4-83
Turning Ringer Circuit ON/OFF with a TTL Output	4-83
Interfacing the TCM1520A Ring Detector	4-85
Autoanswer MODEM	4-89
TCM1520A as a Low Current Power Supply	4-89
μC Control of Ringer	4-89

Appendixes

A	Impedance vs Frequency Curves for Various Values of Capacitors	4-91
B	Kyocera Piezoelectric Acoustic Generator Specifications	4-93

List of Illustrations

Figure	*Title*	*Page*
1	Dial Pulse Transients	4-77
2	Functional Block Diagram	4-78
3	TCM1501B/TCM1506B/TCM1512B Pin Configuration	4-79
4	TCM1520A Ring Detector Pin Configuration	4-79
5	Driving a Piezo Transducer	4-79
6	Optional Circuit for Sharp Cut-Off Ring Signal	4-80
7	Driving a Speaker	4-81
8	TCM1501B Output Characteristics	4-81
9	Equivalent Circuit for REN Analysis	4-82
10	Simplified Ringer Equivalent Circuit	4-83
11	TCM1501B Laboratory Measurements—Impedance vs Frequency	4-84
12	Controlling Ringer with a TTL Output	4-86
13	TCM1520A with Isolated Supply	4-86
14	TCM1520A Drive Capability	4-87
15	TCM1520A with Nonisolated Supply	4-88
16	Autoanswer Modem Application	4-88
17	Small Current Power Supply	4-89
18	Using TCM1520A to Detect Ring Signal and μC to Drive TCM1512B	4-90

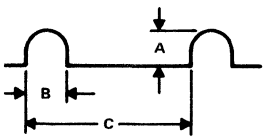
INTRODUCTION

TI's patented BIDFET† process has allowed the combination of high-voltage circuitry to handle signals of up to 150 V and low voltage CMOS technology for dense logic, thus enabling Texas Instruments to offer a series of monolithic ICs that will detect the ring signal on a telephone line. The purpose of this report is to explore the use of these circuits in different applications and understand various technical issues.

FEATURES

Some of the common features of the TCM1501B, TCM1506B, TCM1512B, and TCM1520A include:

1. Lightning Protection: When used in series with the proper resistor and capacitor, these devices will withstand 1500 V/200 μs transients.
2. Antitapping: These devices are designed to ignore high voltage transients generated by dial pulses from a parallel phone, as shown in Figure 1.



A	B	C
800 V	2 ms	50 ms
200 V	10 ms	60 ms

Figure 1. Dial Pulse Transients

3. High Standby Impedance: In the absence of a ring signal, these devices are powered down and present a shunt impedance of greater than 100 kΩ (typically 1 MΩ).
4. High Voltage Output: The output drive capability is up to 40 V peak to peak for the TCM1501B, TCM1506B, and TCM1512B. The TCM1520A has TTL/MOS compatible output.
5. The ICs require a minimum number of external components.

RINGER FUNCTIONAL DESCRIPTION

A functional block diagram of the ringer series and 1520A ring detector is shown in Figures 2(a) and (b). The network formed by C_1 (the dc blocking capacitor), 2.2-kΩ current limiting resistor and the full wave bridge rectifier supply the IC power from the phone lines. The rectified ac ring signal is filtered by an external 10 μF/100-V capacitor connected between pins 6 and 7. The value of C_1 will determine the minimum input voltage. Value of C_1 along with the filter capacitor also affects the turn-on time of the IC. The filter capacitor value with the internal IC circuitry is used to suppress dial tapping. Tapping is a false ringing of the bell due to pulses on the phone line from rotary dials or pulse dialing ICs.

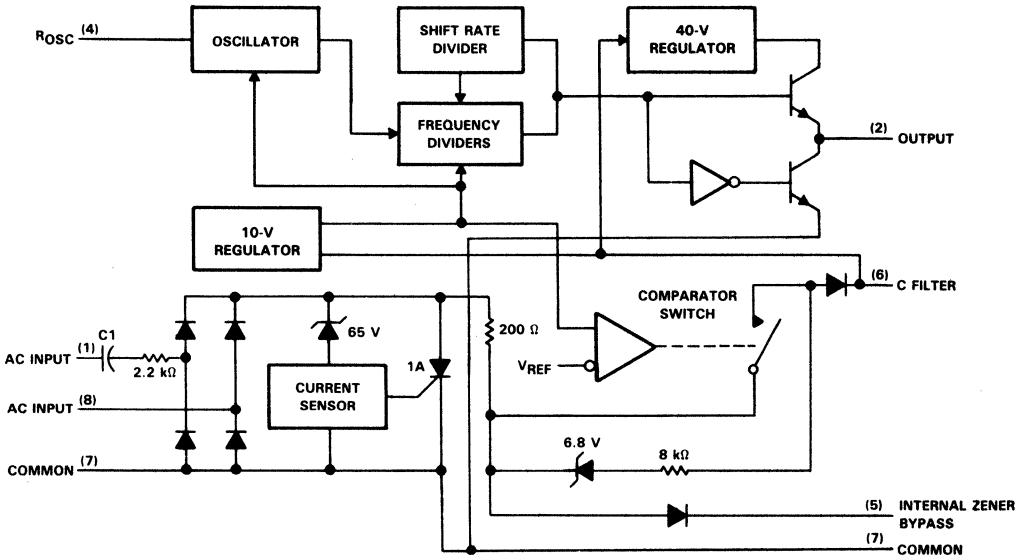
The IC is kept off (in standby) until the incoming signal across pins 1 and 8 reaches a peak voltage of approximately 8.9 V. This threshold can be lowered by externally connecting pin 5 with a lower value zener and resistor to pin 6. Since the IC is kept off below 8.9 V, the IC offers a standby impedance of approximately 1 MΩ to 3 Vrms signals, thus offering minimum distortion to DTMF or voice signals. However, when the voltage across the IC pins 1 and 8 reaches a threshold of approximately 17 V, an internal switch is closed which bypasses the 6.8-V zener, thus allowing maximum energy transfer to the load.

The TCM1501B, TCM1505B, TCM1506B, and TCM1512A have built-in 10-V and 40-V regulators. The 10-V regulator drives the CMOS oscillator and the audio generator section, while the 40-V regulator drives the push-pull output.

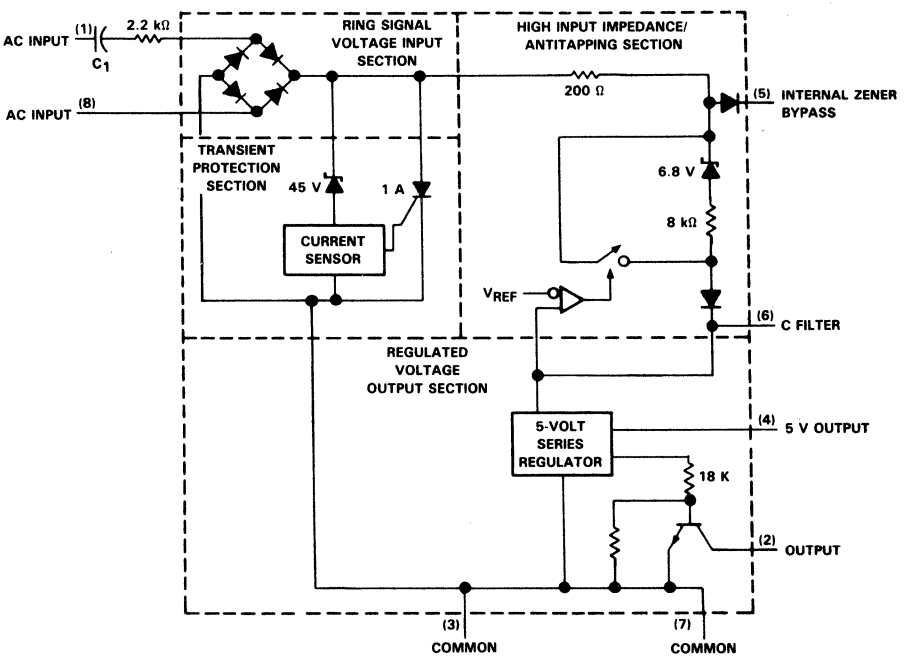
The TCM1520A ring detector has a 5-V regulator only whose output is brought out to pin 4.

The TCM1501B through TCM1512B series and the TCM1520A have a built-in transient protection circuitry which consists of a high current SCR triggered by a sense

†BIDFET—Bipolar, double-diffused, N-channel and P-channel MOS transistors on the same chip—patented process.



(a) TCM1501B, TCM1506B, TCM1512B, TCM1513B



(b) TCM1520A

Figure 2. Functional Block Diagram

circuit through a 65-V or 45-V zener. The external 2.2-kΩ resistor is necessary to dissipate the energy when the SCR is turned on.

Pin Configuration

Pin configurations for this series of monolithic ICs are depicted in Figures 3—5. Pin functions are listed in Table 1.

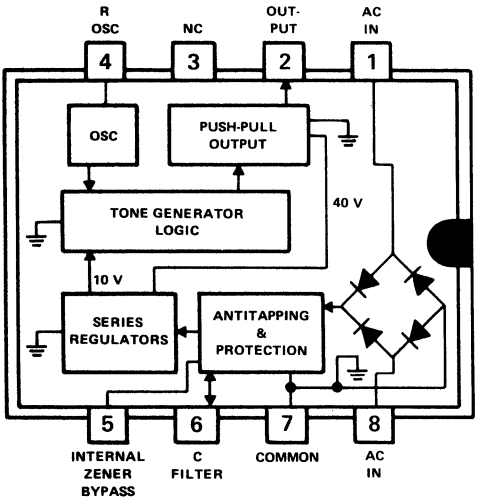


Figure 3. TCM1501B/TCM1506B/TCM1512B Pin Configuration

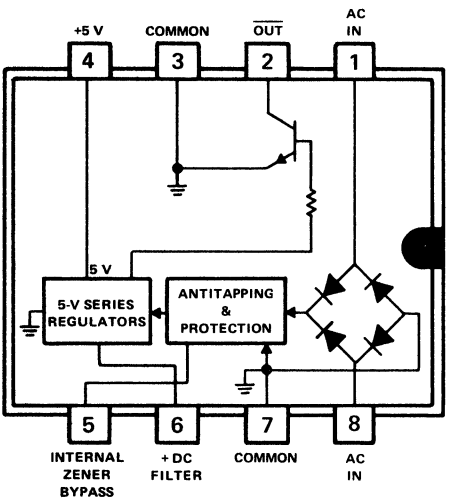


Figure 4. TCM1520A Ring Detector Pin Configuration

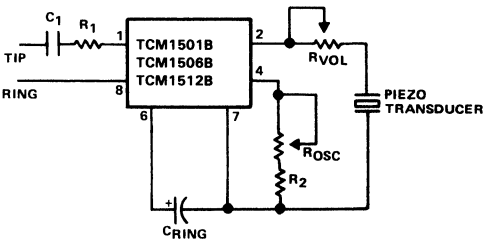


Figure 5. Driving a Piezo Transducer

Table 1. Pin Functions

Pin Number	Function	
1, 8	AC INPUT	Internally limited to 65 V maximum
2	OUTPUT	40 V P-P (TCM1501B, TCM1506B, TCM1512B) Low Active Open Collector (TCM1520A)
3	NC	(TCM1501B, TCM1506B, TCM1512B)
	COMMON	(TCM1520A)
4	ROSC	Resistor between this pin and ground will adjust oscillator frequency (TCM1501B, TCM1506B, TCM1512B).
	+5 V	Five volt dc output (TCM1520A)
5	Internal Zener Bypass	Normally NC externally—a resistor between this pin and pin 6 will lower threshold voltage of ac input that will generate an output.
6	C FILTER	Capacitor to GND stores charge until voltage threshold is surpassed to generate output.
7	COMMON	

Ringer Output Frequency Options

TCM1501B through TCM1512B devices output a square wave that warbles between two audible frequencies. The warble rate and the center frequency are determined by a mask option at the time of manufacturing. An external resistor selects this center frequency. Table 2 lists the various standard ring detector drivers, the center frequency, and warble ratio options.

Table 2. Ringer Output Frequency Options

PART NO.	RECTIFIER TYPE	OUTPUT TYPE	NOMINAL OUTPUT CENTER FREQUENCY (Hz)	WARBLE RATIO	WARBLE FREQUENCY (Hz)
TCM1501B	Full Wave Bridge	Single Ended	2000	5:4	7.8
TCM1506B	Full Wave Bridge	Single Ended	500	5:4	7.8
TCM1512B	Full Wave Bridge	Single Ended	1250	8:7	9.8
TCM1520A	Full Wave Bridge	TTL/MOS Logic	N/A	N/A	N/A

Types of Transducers

All of these devices will drive either a piezoelectric transducer or a speaker except the TCM1520A whose output is a MOS/TTL compatible level.

Maximum energy is delivered to the transducer if the driver output impedance of 4 kΩ is matched to the transducer. For a speaker, an audio transformer is generally required. The choice of piezo device is complicated by the fact that the impedance changes with frequency. Further information on transducer selection may be found in the section on "Ringer Equivalency Number" and Appendixes A and B.

Telephone Applications

Driving a Piezo Transducer

The most obvious application for this device is to detect the ring signal and drive the ringer in an electronic telephone. Figure 5 is the schematic diagram for such an application.

The function and value of each component in Figure 5 is as follows:

C_1 This is a dc blocking capacitor in series with the telephone line. It must pass the ring signal which can be up to 150 Vrms (212 V_{PK}). The value of this capacitor should be as small as possible and still pass enough energy to properly drive the ringer. A common choice for this capacitor would be 0.47 μF, 250 V.

R_1 This resistor is required to dissipate power resulting from a high voltage transient. During a voltage transient (up to 1500 V for 200 μs), the ring detector driver becomes a virtual short, thus shunting the surge of current to ground. This surge of current can be as high as 0.9 A provided the voltage is dropped across R_1. The value should be 2.2 kΩ, ¼ W.

C_{RING} This capacitor is used to store energy from the ring signal and when the input voltage at pins 1 and 8 reach approximately 17 V, the circuit will issue the ring signal. The lower limit of the capacitor value is determined by the time constant required to ignore bell-tapping, while an upper limit is set by the ring turn-on time. After the capacitor reaches its threshold, it continues to charge to approximately 65 V (45 V on TCM1520A). A suitable value for this capacitor is 10 μF, 100 V. This capacitor will also determine the turn-on and turn-off time of the ringer. Should a sharper cut-off of the ring signal be desired, a suggested circuit is shown in Figure 6.

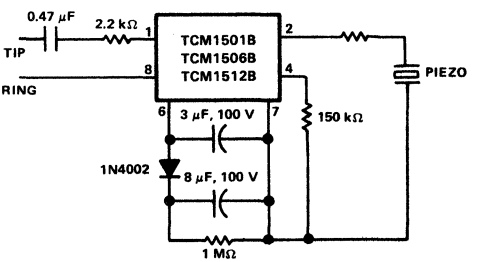


Figure 6. Optional Circuit (for Sharp Cut-off Ring Signal)

R_2 This resistor is present to limit the minimum resistance between pin 4 and ground. A good choice is 150 kΩ.

R_{VOL} This potentiometer allows volume adjustment. A 250-kΩ potentiometer will allow adjustment from full loud to barely audible. If volume adjustment is not required, instead of the potentiometer, a fixed resistor of 0.5 kΩ to 2 kΩ may be used.

PIEZO For a telephone application such as this, the impedance of the transducer must be approximately 4 kΩ to best match the output of the detector/driver. One choice that meets this requirement is a Kyocera KBS-27DB-3A. (See further discussion in section on Ringer Equivalency Number.)

Driving a Speaker

The circuit in Figure 7 will also drive a speaker. The only difference is that a speaker, which is normally 8 Ω, should be matched to the 4-kΩ output with a transformer. Figure 7 shows how the speaker should be connected.

The values and functions of each component in Figure 7 are as follows:

R_{VOL} This potentiometer provides volume control.

C_2 This capacitor blocks dc and should have a low impedance to the detector driver output frequencies. A suitable value is 0.1 μF, 40 V.

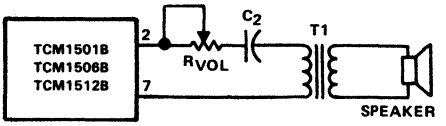


Figure 7. Driving a Speaker

Output Characteristics

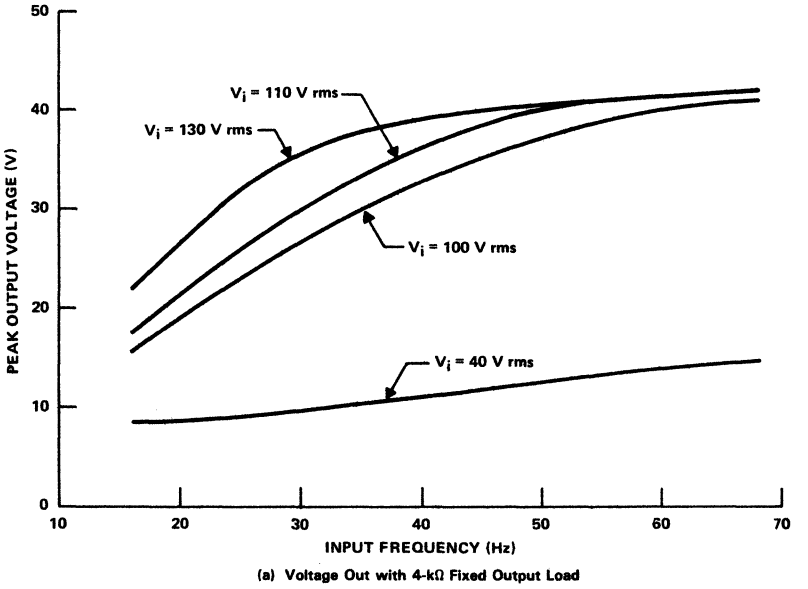
The output voltage and the output power curves of the TCM1501B ringer as a function of input frequency at various input voltages are shown in Figures 8 (a) and (b), respectively. The device is capable of putting out well over 80 mW into a 4-kΩ load with an input signal greater than 110 V, 60 Hz.

Ringer Equivalency Number (REN)

The REN of a ringer circuit is a number that reflects the minimum amount of impedance that is presented to the telephone line during ringing. A standard ringer is defined to be 8000 Ω and have a REN of 1. The following equation may be used to calculate the REN of a nonstandard ringer:

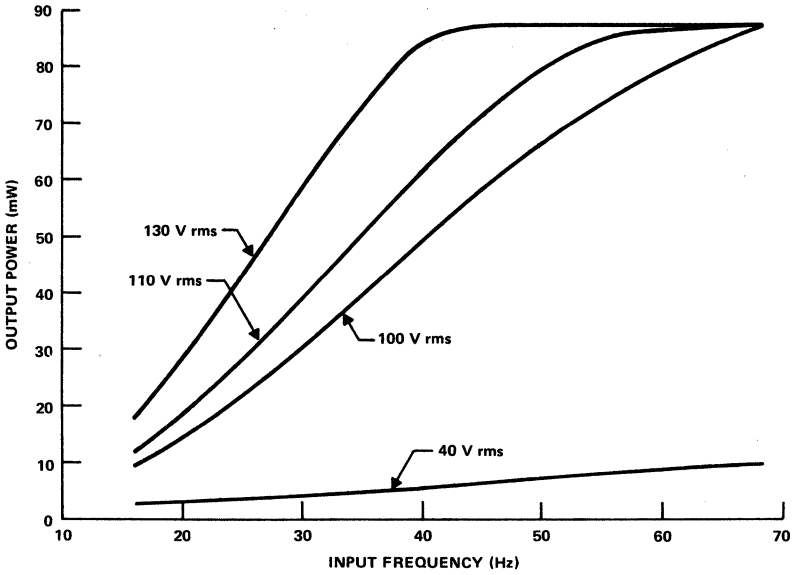
$$REN = \frac{8000}{|Z|}$$

where $|Z|$ is the magnitude of the impedance of the ringer circuit.



(a) Voltage Out with 4-kΩ Fixed Output Load

Figure 8. TCM1501B Output Characteristics



(b) Output Energy with 4-kΩ Fixed Output Load

Figure 8. TCM1501B Output Characteristics (Cont'd)

To estimate the REN of ringer circuits utilizing one of the TCM1500 family ICs, the circuit in Figure 9 may be used. For purposes of simplifying the analysis of this circuit, the diodes in the bridge as well as the 65-V zener may be assumed ideal. Also, once C_{RING} is charged up, it is effectively out of the circuit as far as REN is concerned. The fact that the 65-V zener is in parallel with the 40-kΩ resistance complicates things when the ringing voltage tries to exceed 65 V. The 40-kΩ resistance represents the power used by the CMOS logic circuitry and is so large compared to the impedance of the parallel load that it may be ignored. A further simplification of the equivalent circuit may be drawn as indicated in Figure 10. Notice that the load appears as a resistive impedance even though the piezo device is basically a capacitive device. This is due to the voltage regulators that supply the output drivers that drive the piezo device.

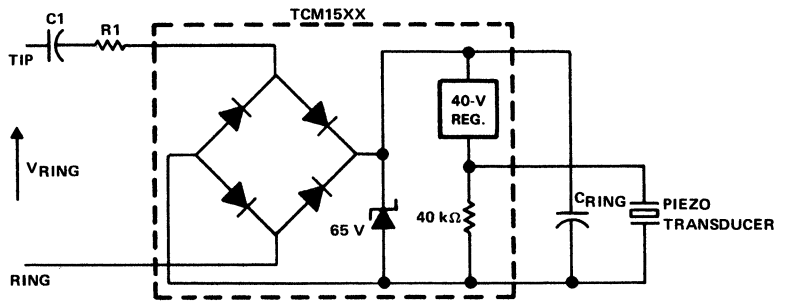


Figure 9. Equivalent Circuit for REN Analysis

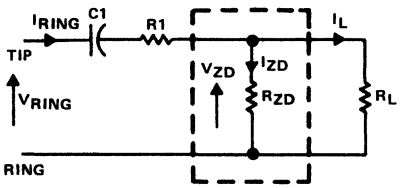


Figure 10. Simplified Ringer Equivalent Circuit

The REN analysis is as follows:

1. Assuming worst case values of Ringer Voltage (V_{RING}) and frequency (f_{ring}), let V_{RING} = 150 V_{rms} (the zener is clamping)
   let f_{ring} = 68 Hz (Class B ringer per FCC part 68)
2. Known values are:
   C_1 = 0.47 μF R_1 = 2.2 kΩ
   R_L = 6 kΩ (from Kyocera impedance graph)
3. Calculate R_{ZD} (equivalent resistance of zener diode)

$$R_{ZD} = \frac{V_{ZD}}{I_{ZD}}$$

where V_{ZD} = 65 volts
and $I_{ZD} = I_{RING} - I_L$

$$\text{where } I_L = \frac{V_L}{R_L} = \frac{65}{6000} = 10.8\ (10^{-3})\ \text{A}$$

$$\text{and } I_{RING} = \frac{V_{C1} + V_{R1}}{Z_{C1} + Z_{R1}}$$

$$Z_{C1} = \frac{1}{j2\pi f_{RING} C} = -j4980\ \Omega$$

$$Z_{R1} = R_1 = 2200\ \Omega$$

$$V_{C1} + V_{R1} = 150 - 65 = 85 \text{ volts}$$

$$I_{RING} = \frac{85}{2200 - j4980} = \frac{85}{5444\ \underline{/-66.16°}}$$

$$= 15.6\ (10^{-3})\underline{/66.16°}\ \text{A}$$

$$I_{ZD} = 15.6\ (10^{-3})\underline{/66.16°} - 10.8\ (10^{-3})$$
$$= (6.30 + j\ 14.26 - 10.8)\ (10^{-3})$$
$$= (-4.5 + j\ 14.26)\ (10^{-3})$$
$$= 14.95\ (10^{-3})\ \underline{-/72.48°}\ \text{A}$$

now since V_{ZD} and I_{ZD} are in phase (resistive), the angle may be dropped

$$R_{ZD} = \frac{65}{14.95\ (10^{-3})}$$

$$R_{ZD} = 4348\ \Omega$$

4. Calculate parallel equivalent for R_{ZD} and R_L

$$R_{ZD} \parallel R_L = \frac{R_{ZD} R_L}{R_{ZD} + R_L} = \frac{(4348)\ (6000)}{4348 + 6000}$$

$$= 2521\ \Omega$$

5. Calculate overall equivalent impedance Z

$$Z = Z_{C1} + Z_{R1} + R_{ZD} \parallel R_L$$
$$= -j4980 + 2200 + 2521$$
$$= -j4980 + 4721 = 6862\ \underline{/-46.71°}\ \Omega$$

6. Calculate REN:

$$REN = \frac{8000}{|Z|} = \frac{8000}{6862}$$

$$REN = 1.165$$

It is important to note that only in the absolute worst case situation of 150 V rms, 68-Hz ring signal would the REN be as high 1.165. If the ring signal is more tightly controlled, as is the case with most PBXs, the REN would typically be less than 0.5. However, if the series blocking capacitor is large and the current limiting resistor is small, the REN could be much greater.

Figure 11(a) through 11(c) show, respectively, the typical laboratory measurements for impedance vs frequency for the TCM1501B ringer with output open, output shorted and with Kyocera KBS-27D8 piezo transducer, taken at different voltages. Figure 11(d) shows the impedance variation of Kyocera Piezo KBS-27D8-3A with frequency. As is obvious, the impedance of the TCM1501B ranges approximately from 8 kΩ to 30 kΩ and is fairly independent of the load connected to its output.

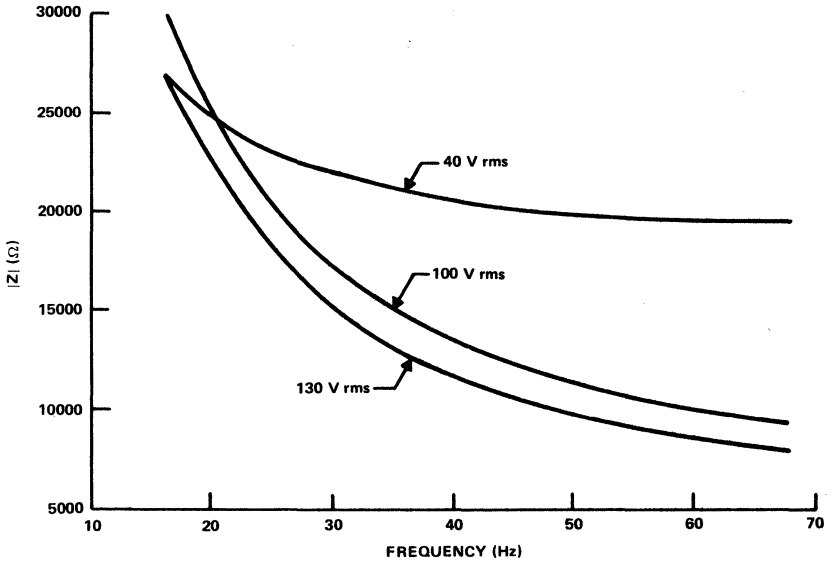
Tighter Frequency Control

Due to normal process variations from one lot to another, the oscillator frequency can vary somewhat from the nominal values listed in Table 2. To obtain these center frequencies, the designer may either use a potentiometer as in the application in Figure 6, or use standard 1% resistor values. The 1% resistor will cause it to oscillate within ±5% of the nominal frequency. If a fixed resistor is used to set frequency, it takes the place of both the R_{osc} potentiometer and R_2.

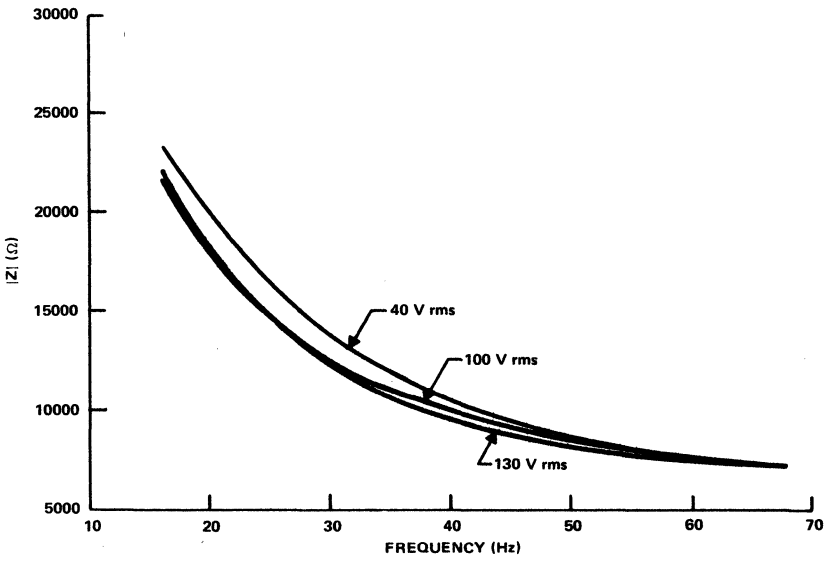
Additional Applications

Turning Ringer Circuit ON/OFF with a TTL Output

Figure 12 shows how an open-collector output of a TTL or STTL device may be used to disable the ring output of the TCM1512B. When the open-collector input goes low, the optoisolator switches ON, placing a voltage on pin 4 that is sufficient to swamp out the internal oscillator. While there are other means of shutting off the ringer, this is a low-voltage high-impedance method that provides isolation.

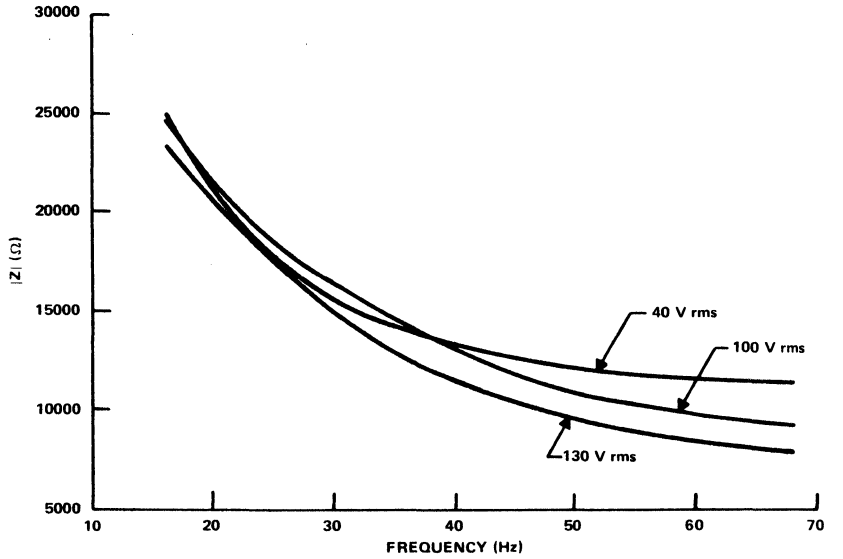


(a) Output Open

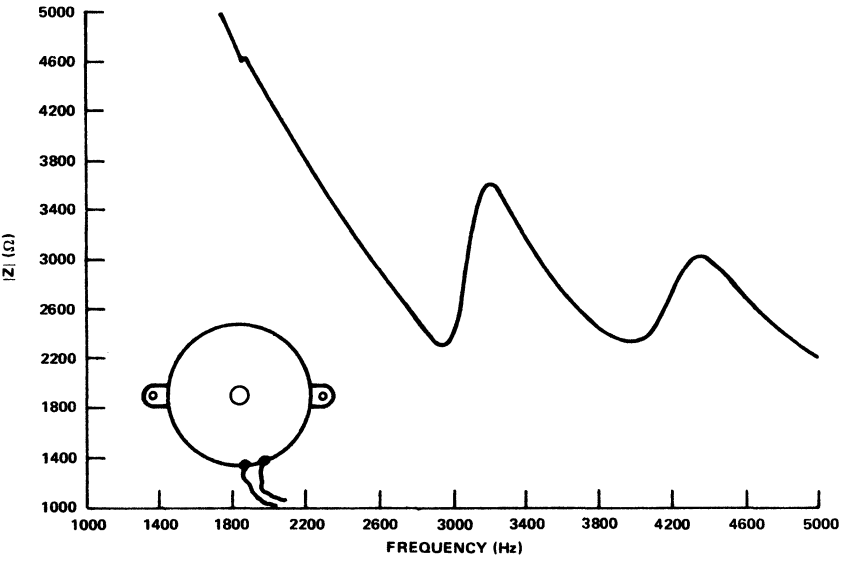


(b) Output Shorted

Figure 11. TCM1501B Laboratory Measurements—Impedance vs Frequency



(c) With Kyocera KBS-27-DB-3A Piezo



(d) Kyocera Piezo KBS-27DB-3A in Stand Alone Mode

Figure 11. Laboratory Measurements — Impedance vs Frequency (Cont'd)

Interfacing the TCM1520A Ring Detector

The TCM1520A may be interfaced to allow either isolated or nonisolated supplies. Figure 13 shows a typical telephone application which uses an optocoupler to keep the phone lines isolated. When a ring signal is applied, the 10-μF capacitor charges until pins 1 and 8 pass the 17-V threshold, at which time pin 4 outputs +5 V turning the optocoupler on. This causes the transistor portion of the optocoupler to saturate, providing a low signal to the μP or logic block.

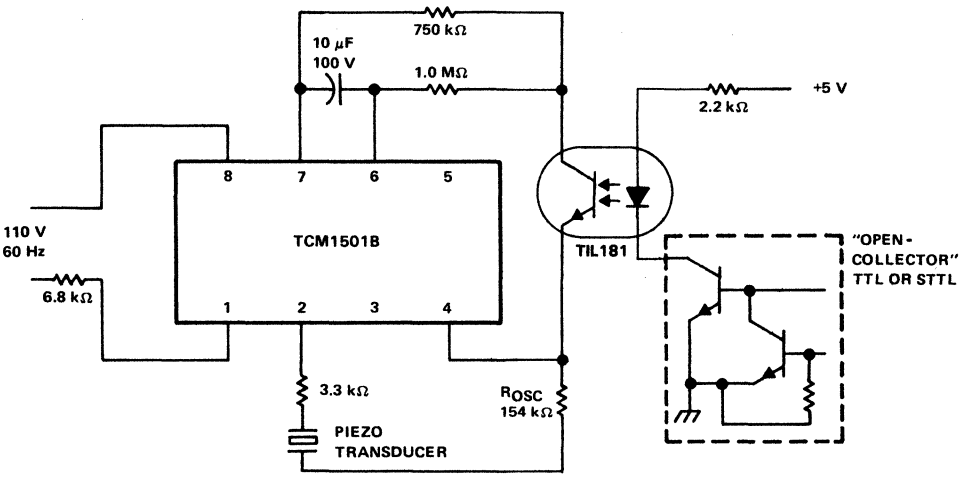


Figure 12. Controlling Ringer with a TTL Output

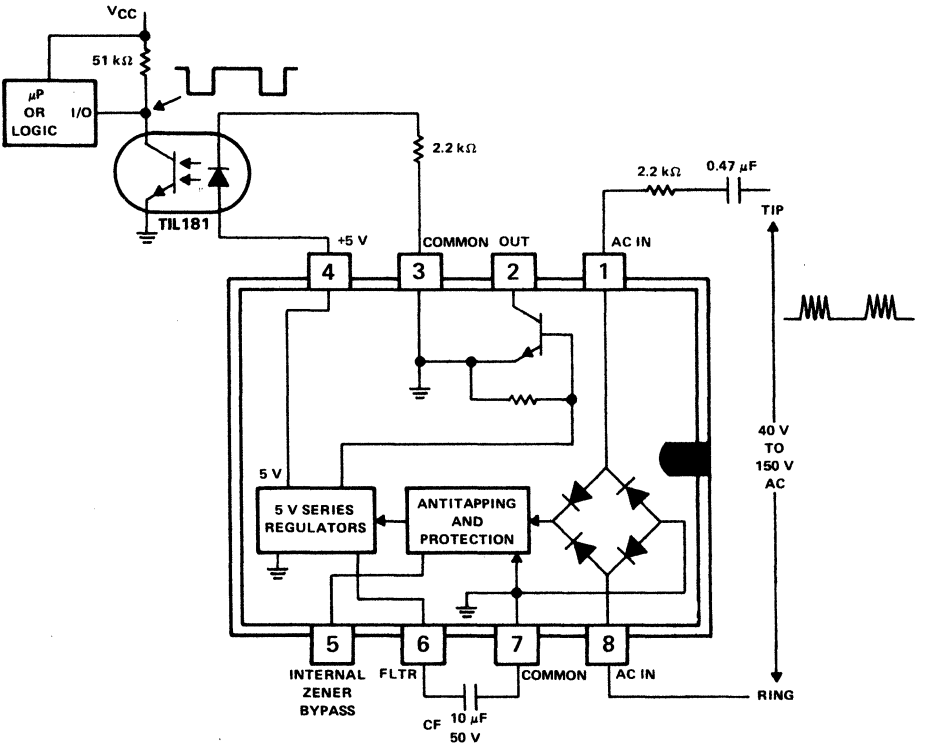
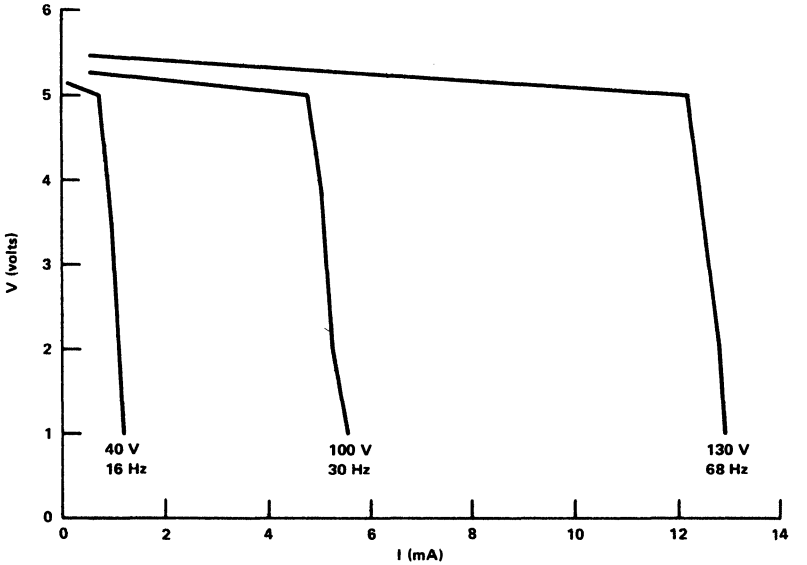
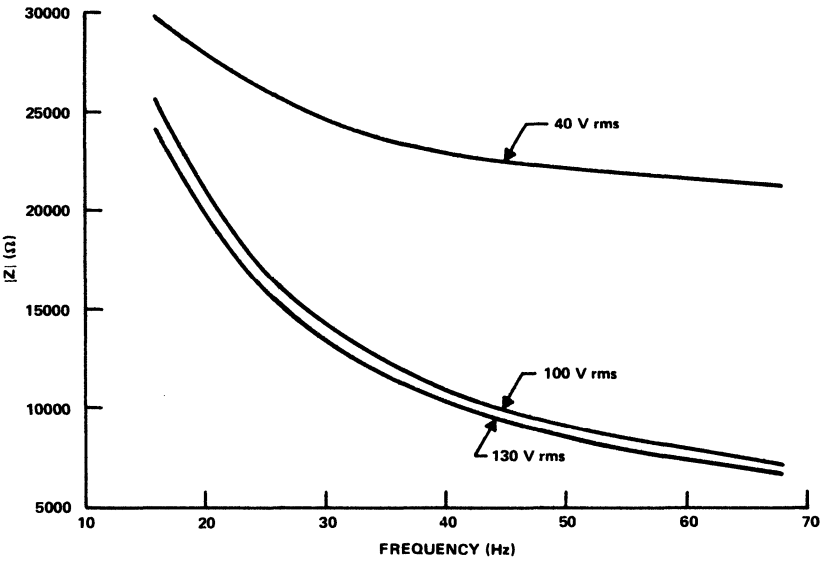


Figure 13. TCM1520A with Isolated Supply

The drive capability of the TCM1520A is a function of the input Tip-Ring voltage and frequency. Figure 14(a) shows the typical output voltage vs load curves at different input ring signals. Figure 14(b) shows the typical impedance vs frequency curves of TCM1520A at different input voltages.



(a) OUTPUT VOLTAGE vs LOAD



(b) OUTPUT OPEN

Figure 14. TCM1520A Drive Capability

Figure 15 illustrates one example of how to interface to the TCM1520A when isolation is not required. The 10-kΩ resistor is required only if the opposite sense of the output signal is desired.

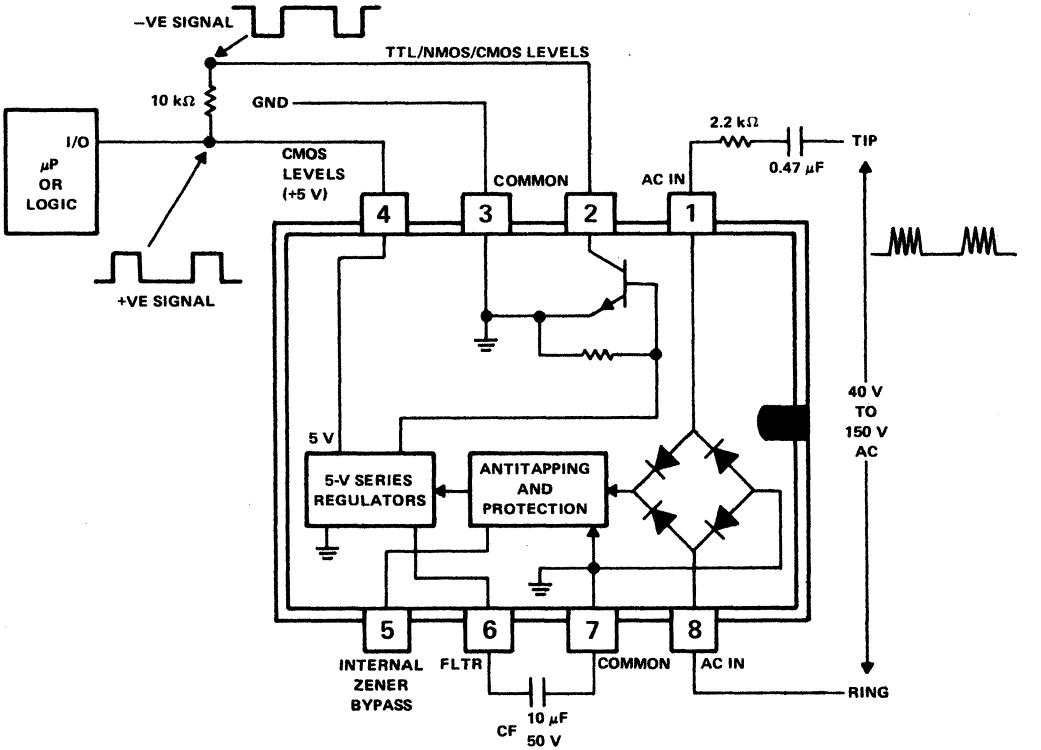


Figure 15. TCM1520A with Nonisolated Supply

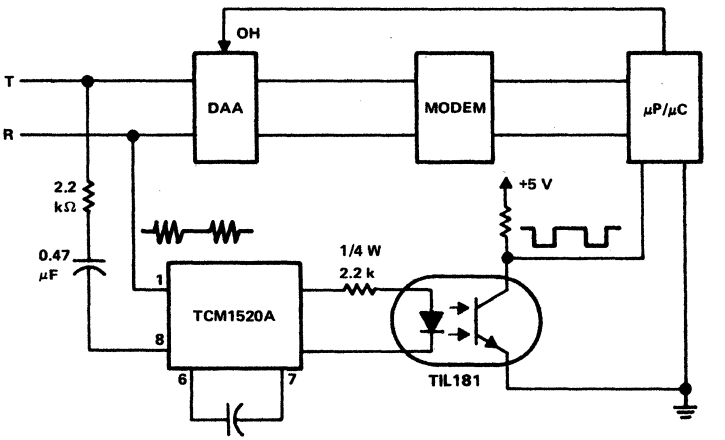


Figure 16. Autoanswer Modem Application

Autoanswer MODEM

Figure 16 shows how the TCM1520A may be used to design an autoanswer MODEM. The incoming ring signal is detected by the TCM1520A which drives an optoisolator to give a MOS/TTL compatible signal to the μP. The μP on recognizing a valid ring signal gives an off-hook (OH) signal to DAA (Direct Access Arrangement), thus answering the "phone." The transmitting device can now send the carrier and start data transmission. The TCM1520A goes in the standby mode offering a better than 1-MΩ impedance to signals below 5 V rms, thus offering no signal degradation to transmit or receive audio signals.

TCM1520A as a Low Current Power Supply

The TCM1520A may also be used as an inexpensive 5-V power supply as shown in Figure 17. This circuit may be plugged directly into a standard 110 V, 60 Hz wall outlet and a regulated 5 V is available at pin 4. The current drive capability in this configuration is dependent upon the series limiting resistor. With a 6.8-kΩ resistor, as shown, the drive capability is about 7 mA.

μC Control of Ringer

Figure 18 shows how a TCM1512B and a TCM1520A may be used to detect a ring signal and then let a microcomputer decide whether to ring the ringer or not. The TCM1520A is used to detect the presence of a ring signal. The TCM1512B is used to drive the piezo transducer. The ringer disable switch could be used to tell the microprocessor whether to ring the ringer or start the tape recorder.

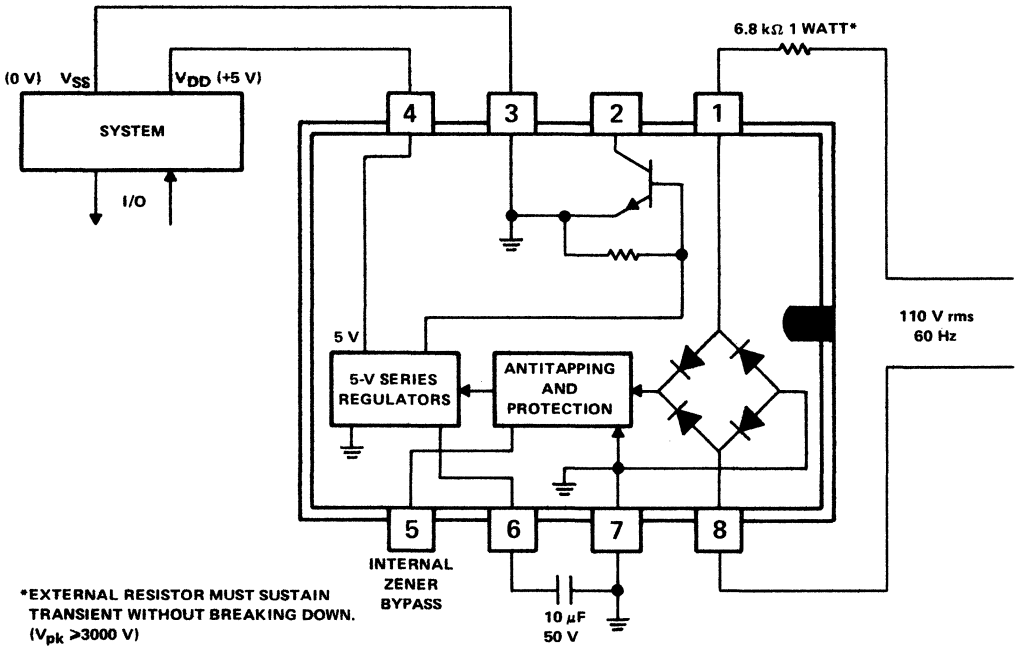


Figure 17. Small Current Power Supply

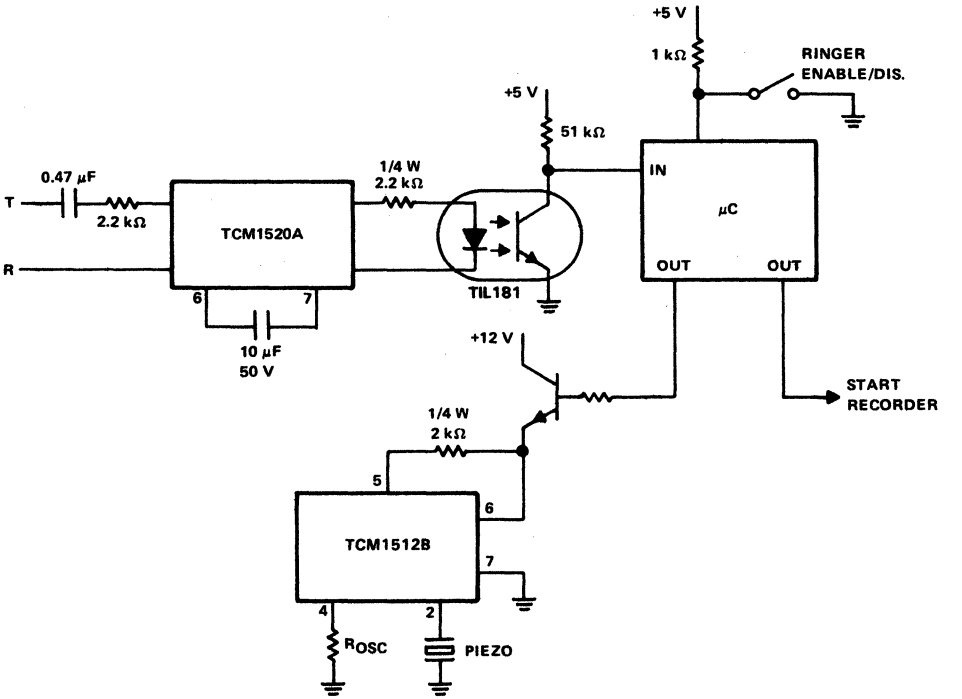
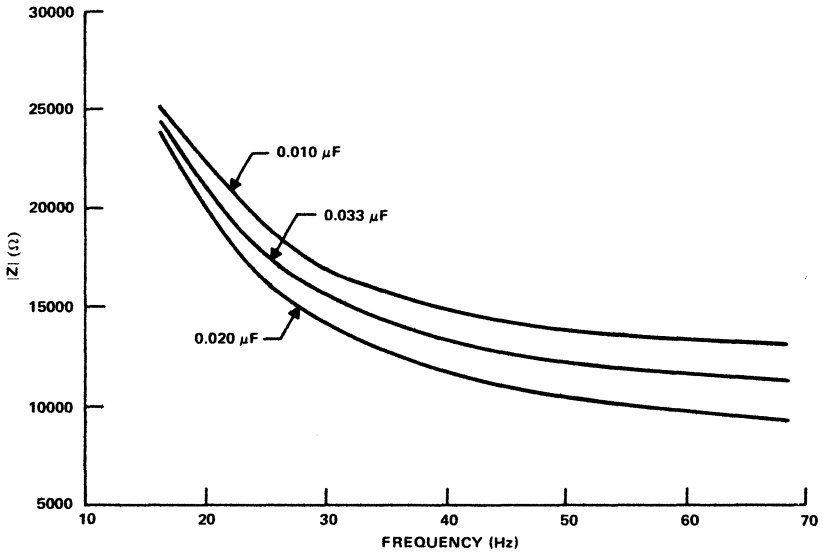


Figure 18. Using TCM1520A to Detect Ring Signal and μC to Drive TCM1512B

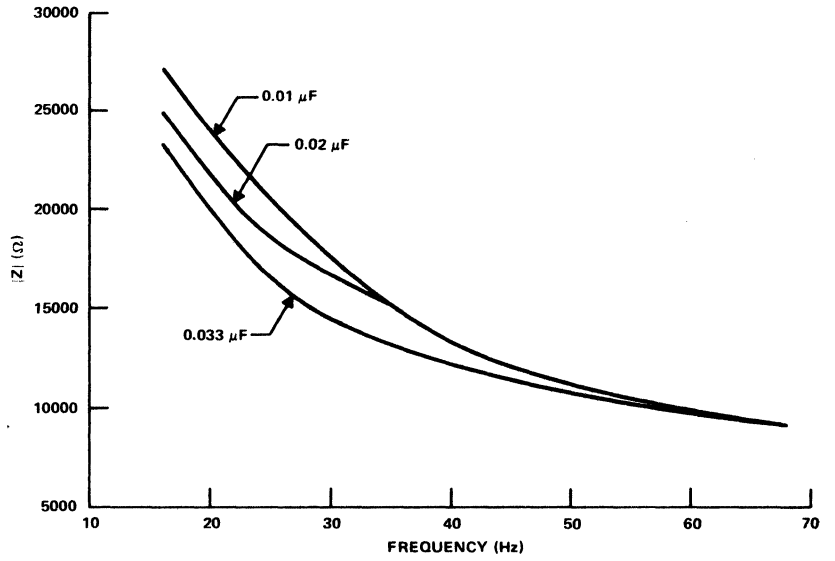
APPENDIX A

Impedance vs Frequency Curves for Various Values of Capacitors to Simulate Piezo Performance

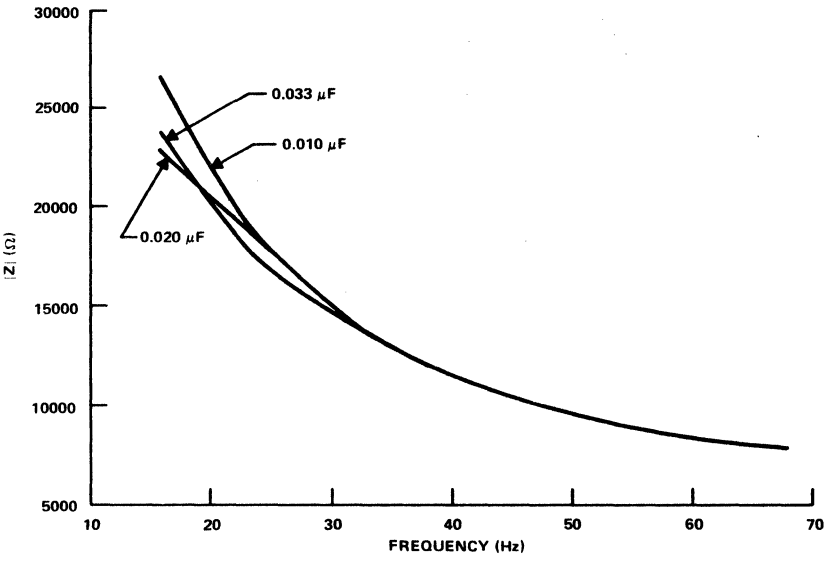


(a) V_{IN} = 40 V rms

Figure A-1. TCM1501B Using Capacitors to Simulate Piezo Performance



(b) V_{IN} = 100 V rms



(c) V_{IN} = 130 V rms

Figure A-1. TCM1501B Using Capacitors to Simulate Piezo Performance (Cont'd)

APPENDIX B

Kyocera Piezoelectric Acoustic Generator Specifications

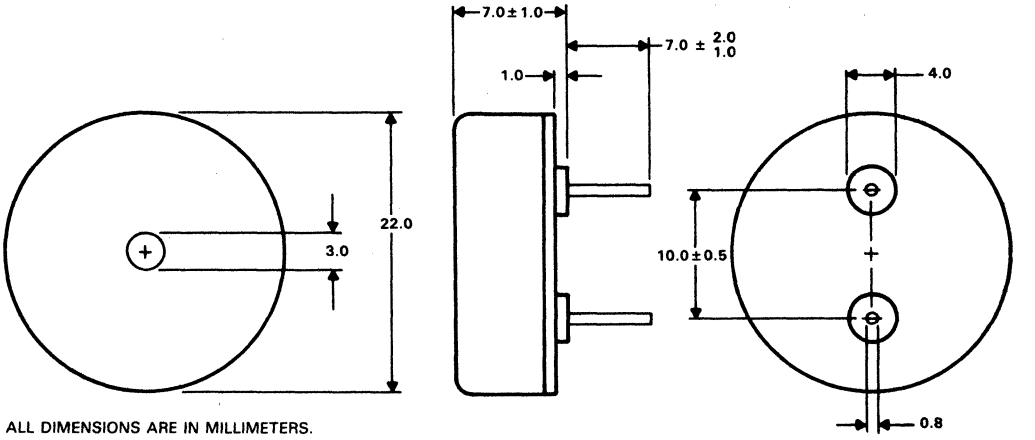
Contact your local Kyocera International, Inc. representative for further details on their devices.

Headquarters: Kyocera International, Inc.
8611 Balboa Avenue
San Diego, CA 92123
(619) 279-8310

Texas: Kyocera International, Inc.
13771 N. Central Expressway
Suite 733
Dallas, Texas 75243
(214) 234-2408

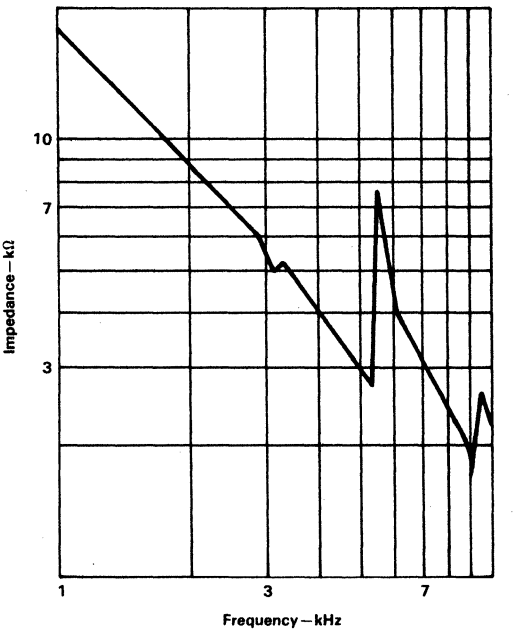
SPECIFICATIONS

PIEZOELECTRIC ACOUSTIC GENERATOR ELEMENT KBS-20DB-3P



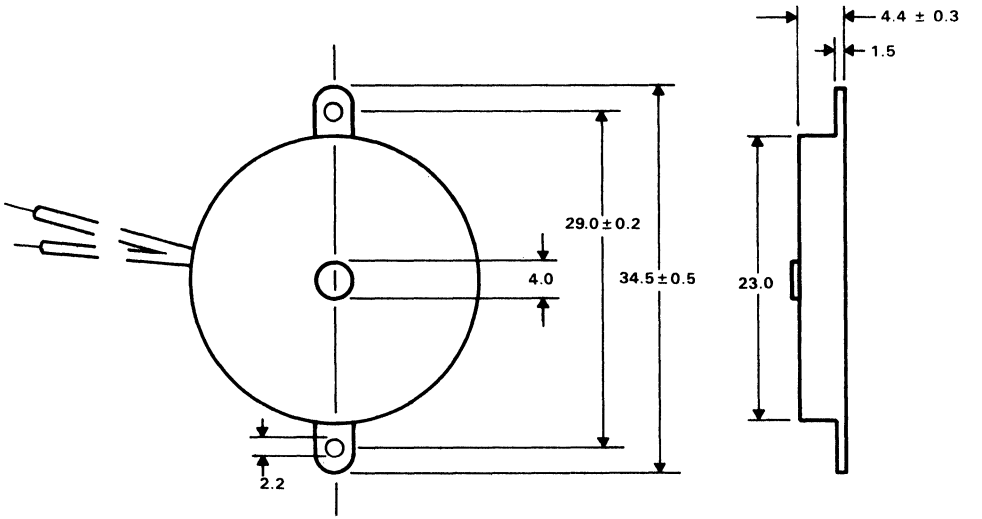
ALL DIMENSIONS ARE IN MILLIMETERS.

1) Working Temperature : −20°C ~ +60°C
2) Resonant Frequency : 3.5 ± 0.5 kHz
3) Resonant Impedance : 7.5 kΩ MAX
4) Capacitance : 10,000 pF ± 30%
5) Applied Voltage (nominal) : 10 V_{p-p}
   Applied Voltage (maximum) : 50 V_{p-p}



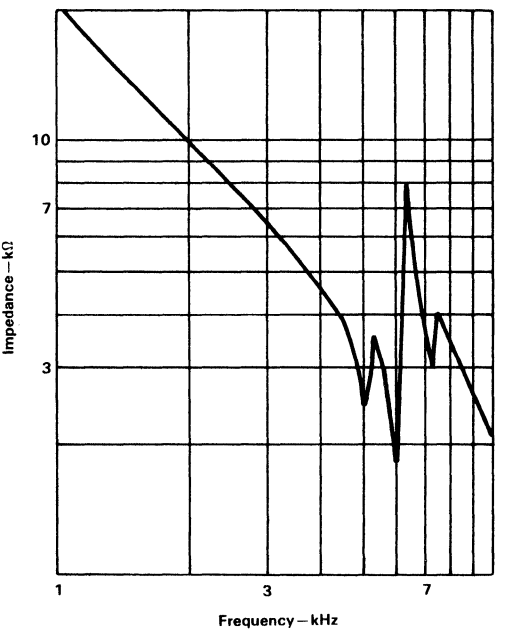
SPECIFICATIONS

PIEZOELECTRIC ACOUSTIC GENERATOR ELEMENT KBS-20DB-5A



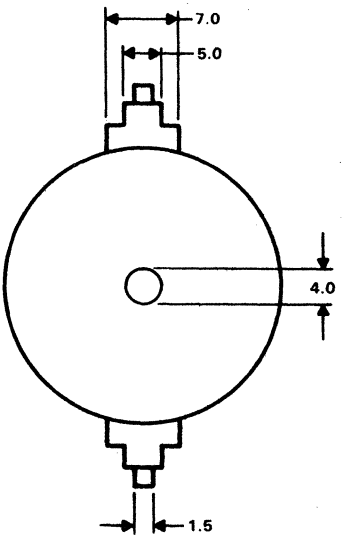
ALL DIMENSIONS ARE IN MILLIMETERS.

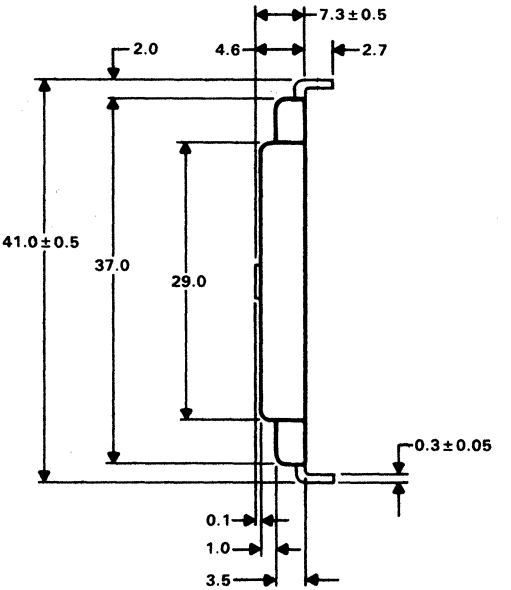
1) Working Temperature : −20 °C ~ +60 °C
2) Resonant Frequency : 6 ± 2 kHz
3) Resonant Impedance : 3 kΩ MAX
4) Capacitance : 10,000 pF ± 30%
5) Applied Voltage (nominal) : 10 V_{p-p}
   Applied Voltage (maximum) : 50 V_{p-p}



SPECIFICATIONS

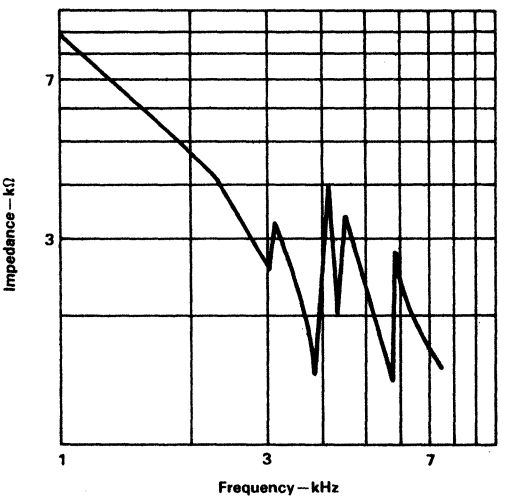
PIEZOELECTRIC ACOUSTIC GENERATOR ELEMENT KBS-27DB-3T





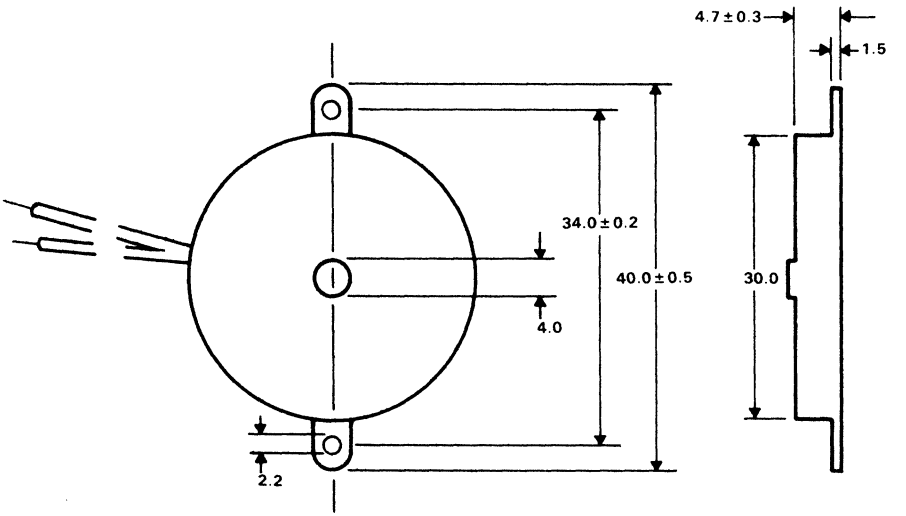
ALL DIMENSIONS ARE IN MILLIMETERS.

1) Working Temperature : −20°C ~ +60°C
2) Resonant Frequency : 3.8 ± 1 kHz
3) Resonant Impedance : 3 kΩ MAX
4) Capacitance : 20,000 pF ± 30%
5) Applied Voltage (nominal) : 10 V_{p-p}
   Applied Voltage (maximum) : 50 V_{p-p}



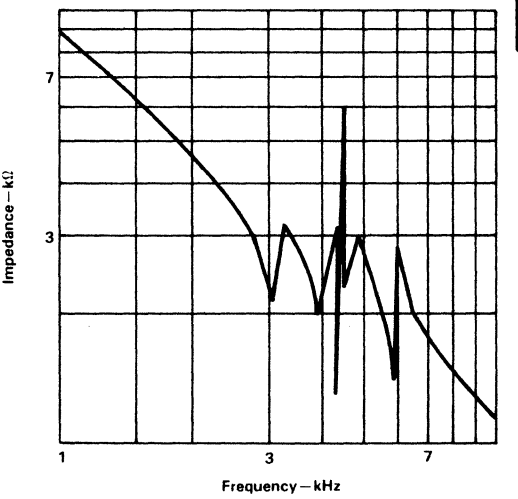
SPECIFICATIONS

PIEZOELECTRIC ACOUSTIC GENERATOR ELEMENT KBS-27DB-3A



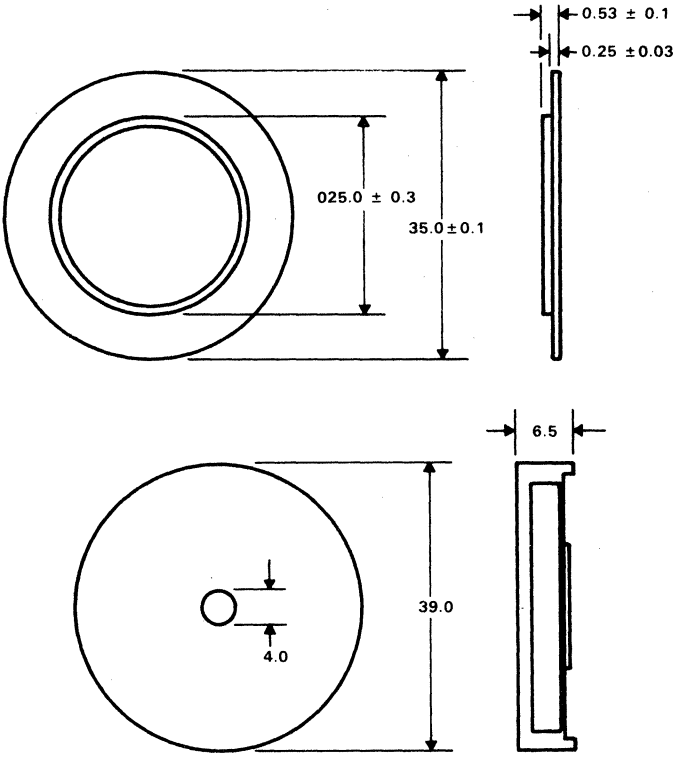
ALL DIMENSIONS ARE IN MILLIMETERS.

1) Working Temperature : −20°C ~ +60°C
2) Resonant Frequency : 3.8 ± 1 kHz
3) Resonant Impedance : 2.5 kΩ MAX
4) Capacitance : 20,000 pF ± 30%
5) Applied Voltage (nominal) : 10 V_{p-p}
   Applied Voltage (maximum) : 50 V_{p-p}



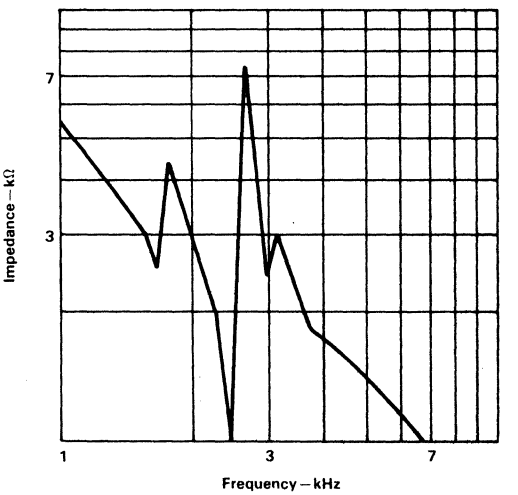
SPECIFICATIONS

PIEZOELECTRIC ACOUSTIC GENERATOR ELEMENT KBS-35DB-3A

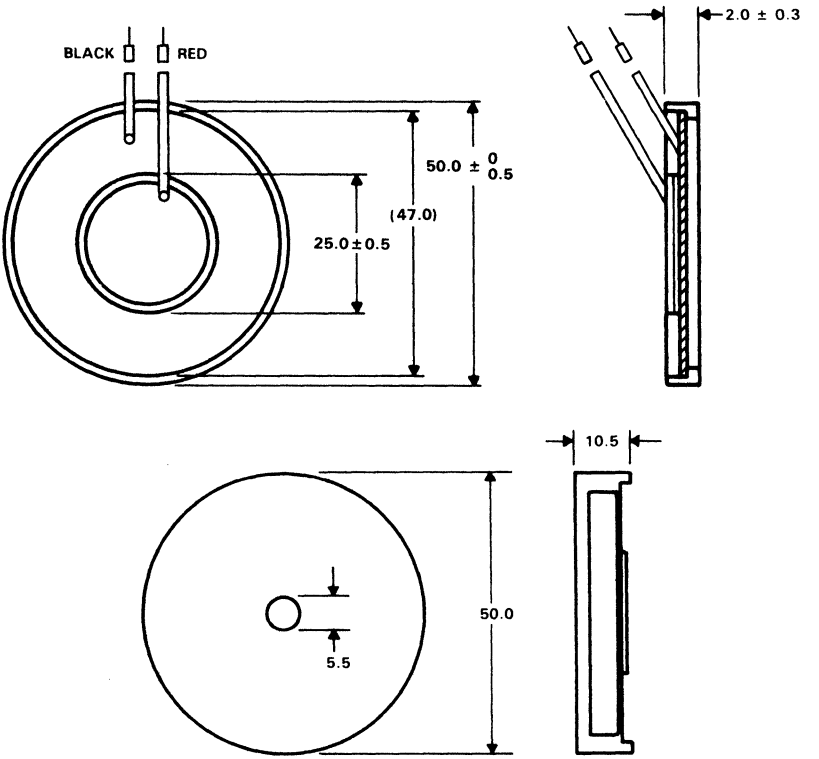


ALL DIMENSIONS ARE IN MILLIMETERS.

1) **Working Temperature** : −20°C ~ +60°C
2) **Resonant Frequency** : 2.9 ± 0.5 kHz
3) **Resonant Impedance** : 200 Ω MAX
4) **Capacitance** : 30,000 pF ± 30%
5) **Applied Voltage (nominal)** : 10 V_{p-p}
   Applied Voltage (maximum) : 50 V_{p-p}

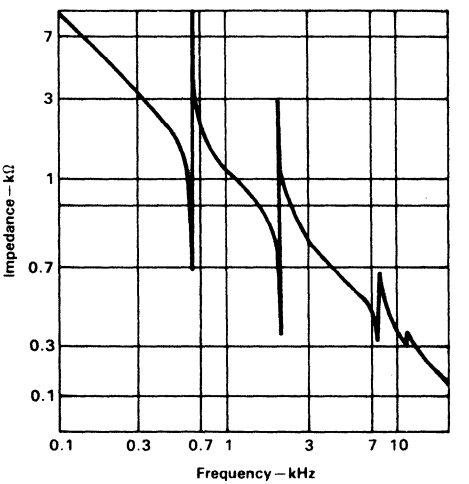


PIEZOELECTRIC ACOUSTIC GENERATOR ELEMENT KBS-50DL-05C



ALL DIMENSIONS ARE IN MILLIMETERS.

1) Working Temperature : −20°C ~ +60°C
2) Resonant Frequency : 0.55 ± 0.25 kHz
3) Resonant Impedance : 700 Ω MAX
4) Capacitance : 120,000 pF ± 30%
5) Applied Voltage (nominal) : 10 V_{p-p}
   Applied Voltage (maximum) : 50 V_{p-p}



Application Reports

Subscriber Line Control Circuits

TEXAS INSTRUMENTS

IMPORTANT NOTICE

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Contents

Title	Page
Introduction	4-105
High-Voltage Functions	4-106
Battery Feed	4-106
Over-Voltage Protection	4-106
Ringing	4-106
Test	4-106
Low-Voltage Functions	4-106
Supervision	4-106
Codec and Filter	4-106
Hybrid	4-107
Theory of Operation	4-107
Signaling	4-107
Ring Signaling	4-107
Dial-Pulse Signaling	4-107
Device Description	4-108
Digital Functions	4-108
Analog Functions	4-108
Supervision Functions	4-110
Functional Description	4-112
TCM4204A	4-112
TCM4205A	4-112
TCM4207A	4-112
System Design	4-112
Supervision Circuit	4-112
Hybrid Circuit	4-119
Flux-Cancelling Drive Circuit	4-120
Conclusion	4-125

List of Illustrations

Figure	*Title*	*Page*
1	Typical Arrangement of the BORSCHT Functions	4-105
2	Dial Pulse Timing Diagram	4-108
3	Internal Configuration of the SLCC	4-109
4	Filter Characteristics as a Function of CLKS Input	4-111
5	Typical Loop Start Application for the TCM4204A	4-113
6	Off-Hook Loop Current Path During Nonringing Condition	4-114
7	Supervision Voltage vs Loop Current	4-114
8	Supervision Circuit Block Diagram	4-116
9	Off-Hook Loop Current Path During Ringing Condition	4-117
10	SLCC Hybrid Function Amplifier Configuration	4-119
11	SUPOT as a Function of Supervisor Input	4-121
12	SUPOT as a Function of Loop Current	4-122
13	High-Impedance Drive Circuit for Flux-Cancelling Winding	4-123
14	TCM4207A SLCC Standard Subscriber Line	4-124

Introduction

In a typical telephone network, the subscriber device (usually a telephone) is connected to a pair of wires called the tip and ring. This pair of wires, known as the subscriber or local loop, connects the subscriber apparatus to the central office (CO) or private branch exchange (PBX). The CO or PBX contains many line cards, each of which interfaces with one or more local loops.

Line-card functions are similar for CO and PBX, with the PBX requirements being less stringent. The functions of line cards are commonly known as the BORSCHT functions. This term is an acronym that stands for **B**attery feed, **O**ver-voltage protection, **R**inging, **S**upervision, **C**odec and filter, **H**ybrid, and **T**est. The arrangement of the BORSCHT functions for a single local loop is illustrated in Figure 1. These functions can be separated into two groups: high voltage and low voltage. In the high-voltage group are battery feed, over-voltage protection, ringing, and test, while the remaining functions fall into the low-voltage group.

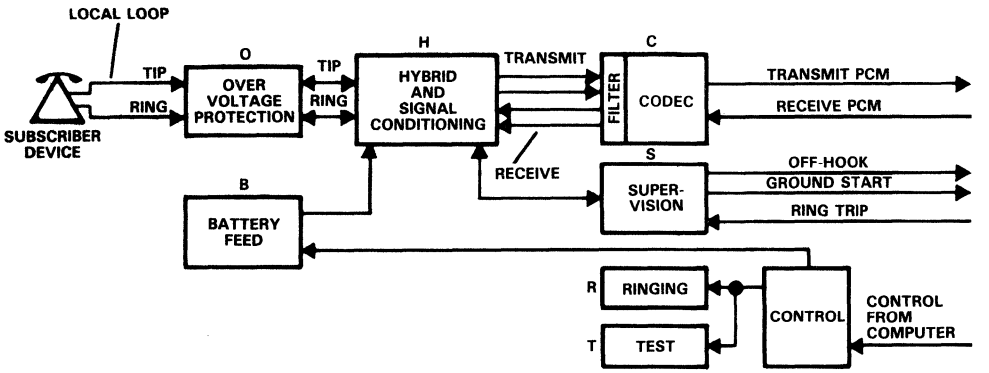


Figure 1. Typical Arrangement of the BORSCHT Functions

In recent years, the trend has been towards increasing the packing density for the CO and PBX. This goal has been realized through the use of LSI circuits to perform one or more of the BORSCHT functions. This in turn has enabled the number of lines handled by each line card to be increased from one to as many as eight. These circuits not only have decreased the space per line ratio for CO components, but also have reduced the cost per line and have improved reliability.

Texas Instruments initial step towards consolidation of the BORSCHT functions was the introduction of the TCM2910 and TCM2911 Codecs and the TCM2912 filter. System integration was further advanced by combining both Codec and filter on the TCM2913 and TCM2914 combos. Today, however, Texas Instruments has further integrated the line card by providing hybrid, supervision, and controlling functions with a family of CMOS LSI circuits called the Subscriber Line Control Circuits (SLCC). Offered are three versions of the SLCC (TCM4204A, TCM4205A, and TCM4207A), each of which is designed for a specific application. (See Functional Description.)

High-Voltage Functions

Battery Feed

The battery-feed function provides the loop with a dc current to power the telephone and is usually supplied by a 48-V battery. For long rural lines, a higher voltage is often used (96 V).

Over-Voltage Protection

Over-voltage protection suppresses high-voltage transients induced by lightning or high-voltage utility lines.

Ringing

This function supplies a ring signal to the subscriber device by switching a ring generator onto the local loop. The signal is typically a 90 V rms sine wave at 20 Hz and is gated for one second on with three seconds off.

Test

Testing involves the use of relays to provide access to the local loop and to the switching circuits in order to test the line.

Low-Voltage Functions

Supervision

When the subscriber apparatus is taken off-hook, the local loop is closed and a dc current is allowed to flow. The supervisor function monitors this loop current to determine when the telephone goes on- or off-hook. It is also used to perform dial-pulse accumulation when rotary-dial telephones are used. Dial pulses are generated by opening and closing the loop in rapid succession.

Codec and Filter

The Codec function is performed when an analog line is interfaced with a digital trunk. Encoding is carried out on the analog signal from the loop, and decoding is performed on the bit stream from the trunk. A voice-band filter (300 Hz to 3500 Hz) is used before encoding and after decoding.

Hybrid

The hybrid function separates the bidirectional voice signals from the two-wire loop into distinct transmit and receive paths. This separation facilitates the use of analog repeater amplifiers or digital processing circuits. The hybrid function is named for the specialized transformer that has traditionally performed this two-wire to four-wire conversion.

Theory of Operation

Signaling

In addition to the supervision signaling previously described, two other types of signaling are used: ring and dial pulse signaling.

Ring Signaling

A ring signal is initiated in the CO or PBX and is used to alert the subscriber to an incoming call. The ring signal is injected onto the local loop by switching a ring generator in series with the battery.

The ring signal in the United States is a sine wave ranging in frequency from 15.3 Hz to 68 Hz, and in amplitude from 40 V rms to 150 V rms. The signal is gated on and off in a particular 'cadence.' A typical ring signal in the U.S. is 90 V rms at 20 Hz gated for one second on and three seconds off.

Dial-Pulse Signaling

Dial pulses are generated by making and breaking the subscriber loop in rapid succession. Figure 2 shows loop current as a function of time during dialing. In the United States, the recommended timing requirements for dial pulses are given by the Electronics Industries Association RS-470 standard. This document specifies a pulse period from 91 to 125 ms, with a percent break between 58 and 64. Here, percent break is defined as follows:

$$[(\text{break duration})/(\text{break duration} + \text{make duration})] \times 100$$

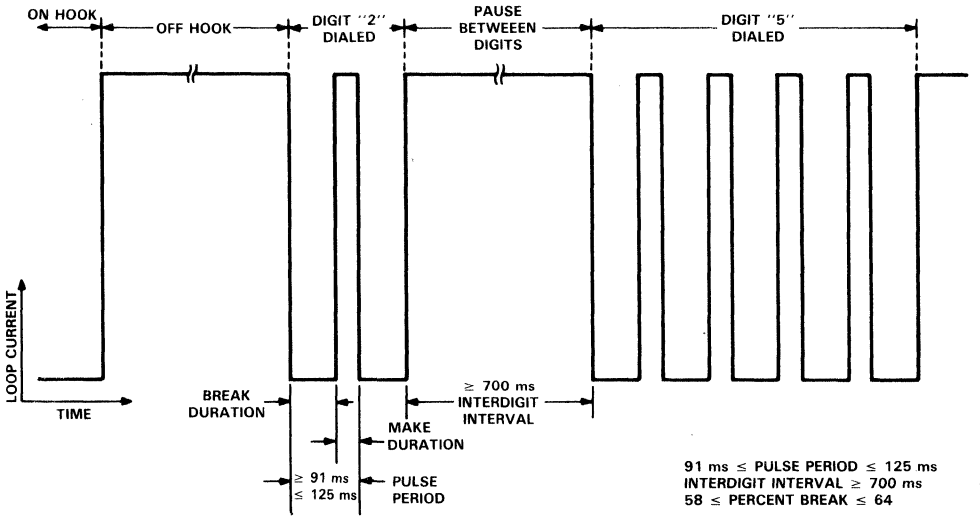


Figure 2. Dial Pulse Timing Diagram

Device Description

The pin functions of TI's three SLCCs are given in Table 1, and the functional block diagram is shown in Figure 3. Each SLCC can be divided conceptually into digital, analog, and supervisor functions.

Digital Functions

The heart of the digital section of the SLCC is a 24-bit data storage unit (DSU). This DSU contains bits of read only and read/write data to provide hook status, relay control, transmit and receive gain control, and line-balance selection.

The bits in the DSU are accessed through a single DATA pin. A low transition on the chip enable input ($\overline{CE}$) causes the DATA pin to change from a high impedance to an active state, and sets the pointer/counter to bit 0. The pointer is advanced by a positive transition on the clock (CLKM) input. The read/write ($R/\overline{W}$) input determines the direction of information flow on the DATA pin. See the TCM4204A data sheet for a detailed timing diagram.

Analog Functions

The analog functions consist of the receive and transmit signal paths, with attenuators, and the hybrid function. The receive and transmit attenuators increase the versatility of the SLCC. The receive path gain is variable from –7.8 dB to +4.8 dB in 0.2-dB increments. The transmit path gain is variable from –12.6 dB to 0.0 dB in 0.2-dB increments.

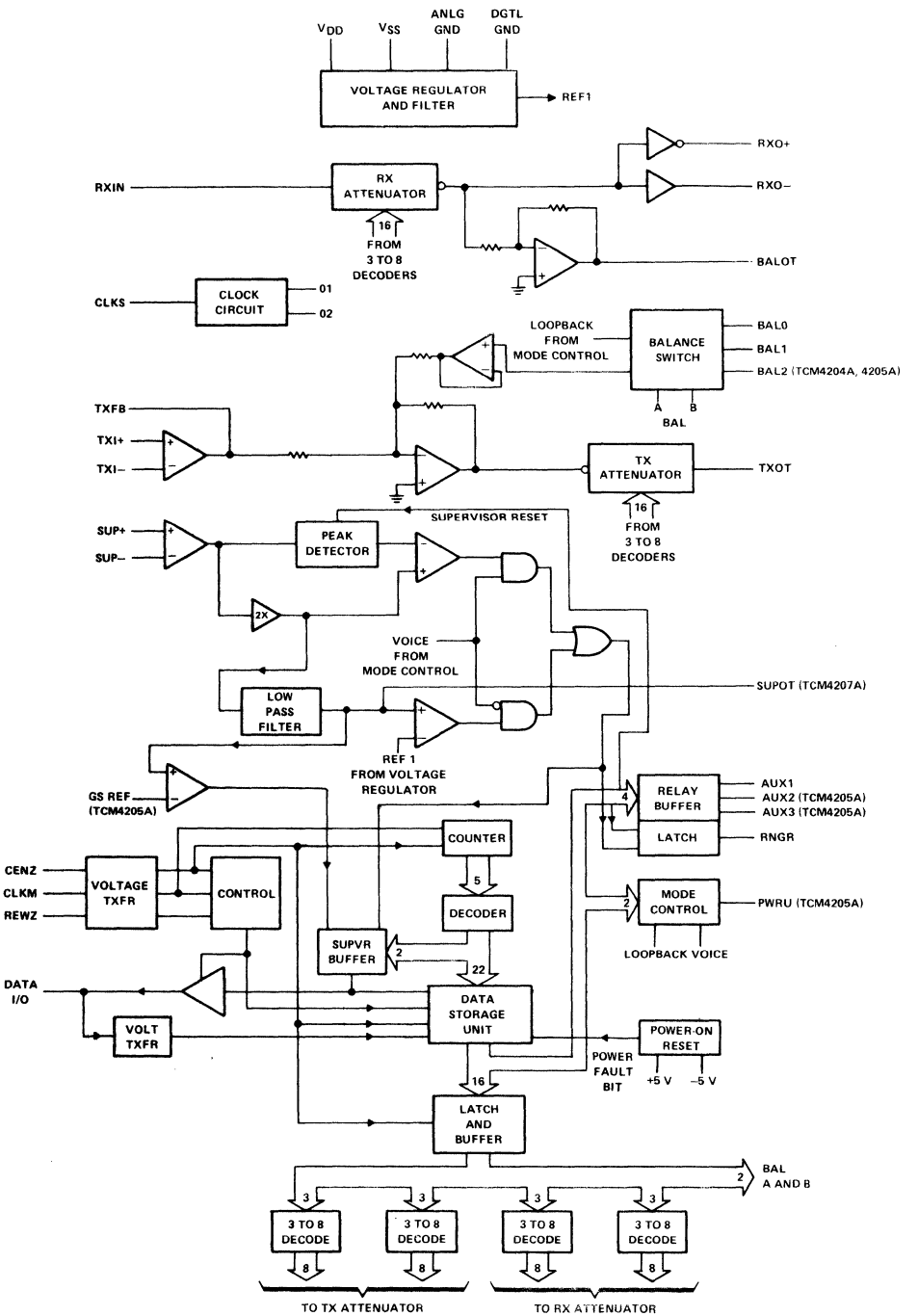


Figure 3. Internal Configuration of the Subscriber Line Control Circuits

Table 1. Pin Functional Description

NAME	PIN			DESCRIPTION
	TCM4204A	TCM4205A	TCM4207A	
ANLG GND	4	4	4	Analog ground
AUX1 AUX2 AUX3	11	11 12 13	11	Latched digital outputs for relay control
BAL0 BAL1 BAL2	19 18 17	23 22 21	19 18	Analog input to balance network selection
BALOT	5	5	5	A buffered form of the RX signal for application to the external balance network
$\overline{CE}$	9	9	9	Chip enable. Activated by a logic low input.
CLKM	7	7	7	Digital clock input that advances the pointer counter of the digital storage unit (DSU) allowing the information in the DSU to be accessed. When R/$\overline{W}$ and $\overline{CE}$ are low, information on the DATA I/O pin is latched into the DSU by the falling edge of CLKM.
CLKS	13	15	13	A continuous clock input (from 1.536 to 2.048 MHz) used for internal logic. This signal is not synchronous with any other signal.
DATA I/O	10	10	10	Digital data input/output. When $\overline{CE}$ is low and R/$\overline{W}$ is high, the DATA I/O pin is in the output mode. When $\overline{CE}$ is low and R/$\overline{W}$ is low, the DATA I/O pin is in the input mode. When $\overline{CE}$ is high, the DATA I/O pin is in the high-impedance state.
DGTL GND	12	14	12	Digital ground
GS REF		20		Analog reference voltage input used for ground start supervision.
PWRU		17		Decoded digital output of Mode Control used to control an external power supply.
RNGR	14	16	14	Latched digital output to control the ring relay. The output turns off (low) when off-hook is detected, but the controller must program the ring bit low to ensure that the output remains low.
RXIN	6	6	6	Analog input to the receive section
RXO+ RXO−	2 3	2 3	2 3	Complementary analog output of the receive amplifier
R/$\overline{W}$	8	8	8	Digital input control for the direction of response of the digital storage unit. A logic high on R/$\overline{W}$ sets the DSU to transmit information. A logic low on R/$\overline{W}$ enables the DSU to receive information.
SUP+ SUP−	15 16	18 19	15 16	Differential analog supervision inputs. Inputs to SUP+ and SUP− are used to detect off-hook status during normal and ringing supervision.
SUPOT			17	Filtered supervisory analog output
TXFB	20	24	20	Feedback out of TX input amplifier
TXI+ TXI−	21 22	25 26	21 22	Analog differential inputs to TX input amplifier
TXOT	23	27	23	Analog output of TX output amplifier
V_{DD}	24	28	24	Supply voltage (5 V ±5%)
V_{SS}	1	1	1	Supply voltage (−5 V ±5%) referenced to ANLG GND

Supervision Functions

Line supervision is performed using differential inputs SUP+ and SUP−. When loop current flows, a voltage appears across the inputs from an external resistor network. The low-pass filter (LPF) shown in Figure 3 is used when off-hook detection is required during ringing. The LPF is a switched-capacitor filter, and its cutoff frequency is determined by the frequency of the input CLKS. Figure 4 shows the filter characteristics as a function of CLKS frequency. The LPF filters out the ac component from the supervision signal to detect a valid off-hook condition during ringing. The output of the LPF is used to set

bit 0 (on/off-hook) of the DSU. By virtue of the CLKS input, the SLCC can be used with any frequency ring generator. With the SLCC in the voice mode of operation, the LPF is ignored. This condition allows dial pulses to pass undistorted to the DSU.

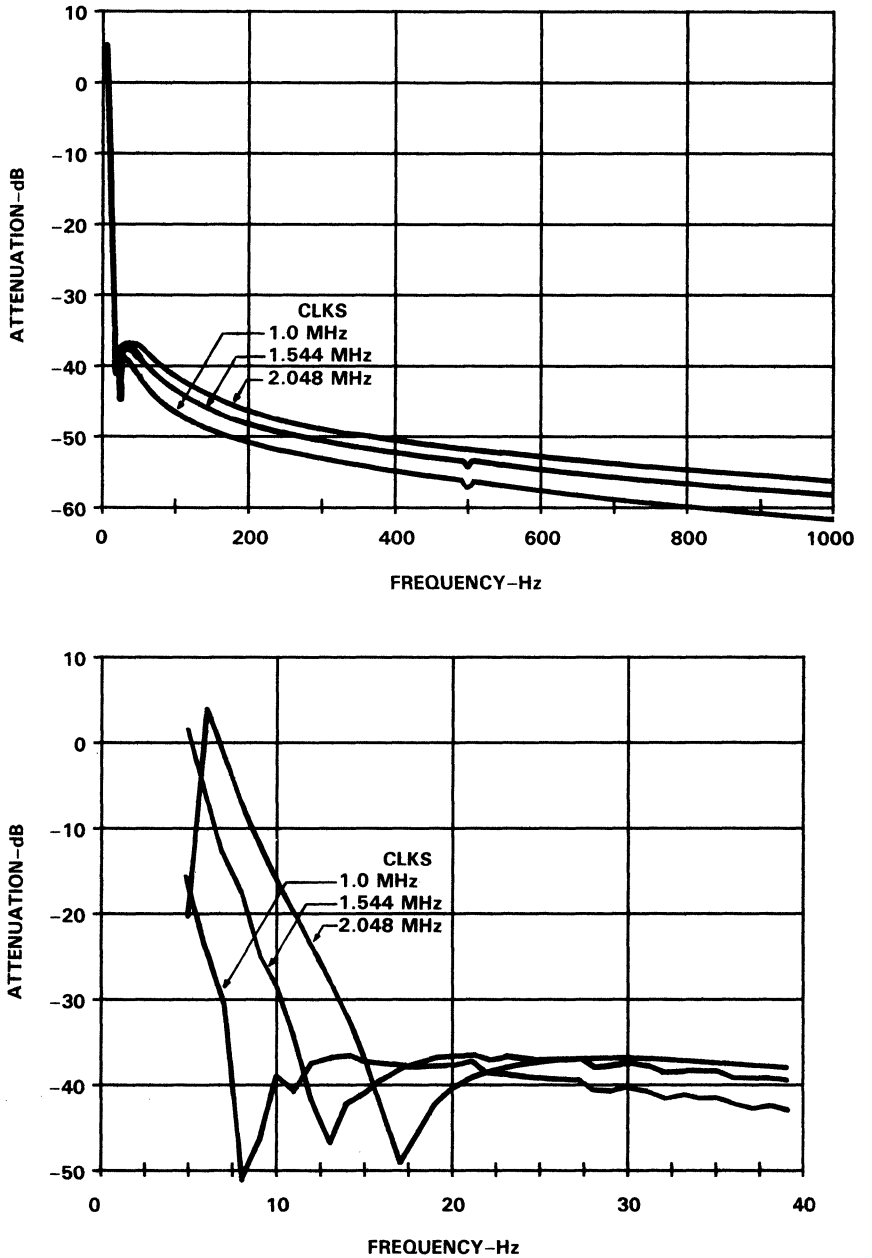


Figure 4. Filter Characteristics as a Function of CLKS Input

Functional Description

The three versions of the SLCC (TCM4204A, TCM4205A, TCM4207A) have some functional differences. Each is designed to accommodate a different type of application, as outlined below.

TCM4204A

The TCM4204A, a 24-pin device, is configured to operate in a standard loop-start CO or PBX environment. It provides a ring relay output, plus one auxiliary output to control the test relay. A provision for three balance networks allows the same card to operate on virtually any length of line through a simple software manipulation.

TCM4205A

The TCM4205A is a 28-pin version of the SLCC and is ideal for ground-start applications. It performs all those functions found in the TCM4204A, with the addition of two extra relay outputs, a PWRU pin used to signal the power supply, and a GS REF ground-start reference input.

TCM4207A

The TCM4207A is identical to the TCM4204A aside from the addition of a supervisor output, which replaces one of the line-balance networks. This supervisor output provides a voltage that is proportional to the supervisor input-voltage. The output is used in driving a flux-cancelling winding in the battery-feed transformer.

System Design

Supervision Circuit

A typical application of the TCM4204A in a loop-start system is shown in Figure 5. In the normal (nonringing) state, the loop current (typically 20 mA to 80 mA) flows through the path defined in Figure 6. The loop current causes an IR drop across each of the 200-Ω resistors, which shifts the voltage levels on the supervision inputs (SUP+ and SUP–). Figure 7 gives SUP+ and SUP– voltages as a function of loop current. When the differential voltage between the two exceeds the threshold, the SLCC responds by setting the hook-status bit in the DSU to a logic high, indicating the off-hook condition.

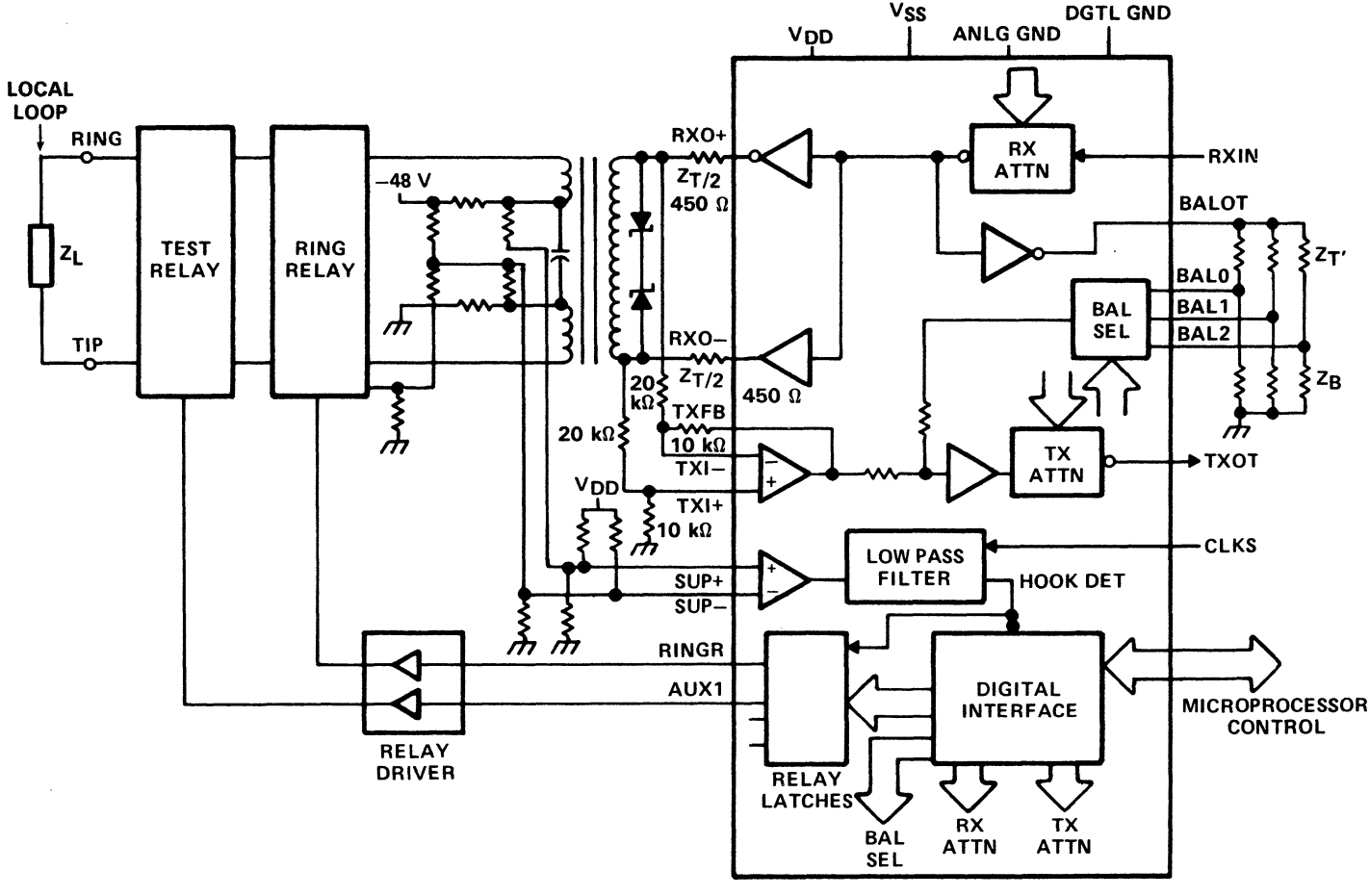


Figure 5. Typical Loop Start Application for the TCM4204A

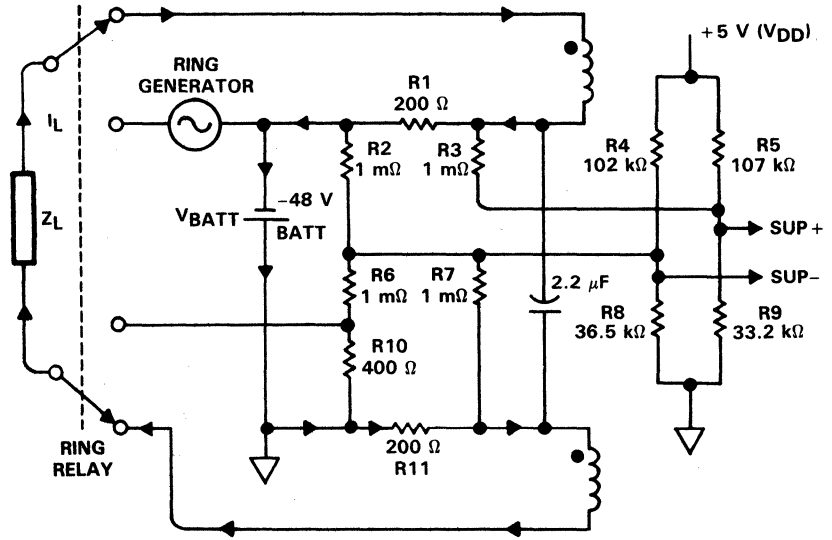


Figure 6. Off-Hook Loop Current Path During Nonringing Condition

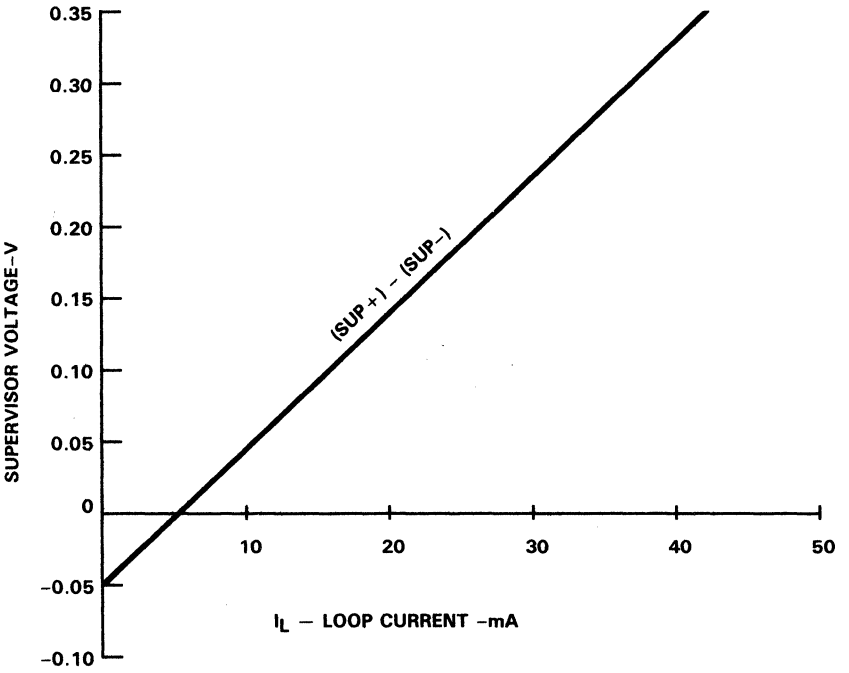


Figure 7. Supervision Voltage vs Loop Current

A detailed diagram of the supervision circuitry of the SLCC is given in Figure 8. The details of supervisor operation are as follows:

1. A differential voltage across the SUP+ and SUP– inputs, referenced positive on SUP+ is required to initiate the off-hook condition (bit 0 high) in the standby or power-down mode.
2. Initial off-hook detection is always done in the standby or power-down mode.
3. The voltage across SUP+ and SUP– required for off-hook detection is 50 mV.
4. For rejection of the ring signal, the supervisor information is filtered with a switched capacitor low-pass filter when not in the voice mode.
5. When the ring bit is set high, an off-hook detection causes the ring relay output to go low; however, the ring bit must be reset to low by the controller before the controller changes the SLCC to the voice mode.
6. The voltage on either SUP input should always be between -2 V and +2.5 V. Outside this range, the supervision circuits become non-linear and the SUP inputs may require significant current. For this reason it is recommended that SUP+ and SUP– both be near 0 V for no-loop current.
7. After initial off-hook detection, the SLCC should always be placed into the voice mode.
8. When the SLCC is placed in the voice mode, on-hook is detected using a peak-detector circuit. The peak-detector samples and stores the peak value of the SUP differential voltage. On-hook is detected when the SUP voltage falls below half the stored voltage. This circuit provides the ability to detect dial pulses and on-hook at the termination of a call.
9. The peak-detector circuit capacitor is discharged to 0 V whenever the SLCC is placed in the ring mode or when the Supervisor reset bit is set to a high. The Supervisor Reset should be used if off-hook is detected during standby mode to eliminate any accumulated charge on the capacitor due to noise.

If the subscriber returns to on-hook status while the Supervisor Reset bit is being used, then the SLCC cannot accurately detect the on-hook condition since, both the SUP voltage and the peak detector are at 0 V. This inability can be prevented by providing a dc bias-voltage in the reverse direction on the SUP+ and SUP– inputs when no loop current is flowing.

During pulse dialing, the loop current is pulsed off and on approximately ten times per second. When the SLCC is in the voice mode (set through the microprocessor interface), the supervisor information from SUP+ and SUP– is routed through a peak detector circuit, bypassing the low-pass filter. The pulses toggle the hook status bit in the DSU as the loop current is pulsed. The controlling microprocessor monitors this bit and counts the dial pulses. Dial-pulse accumulation can be accomplished only in the voice mode, because the low-pass filter will distort the dial pulses.

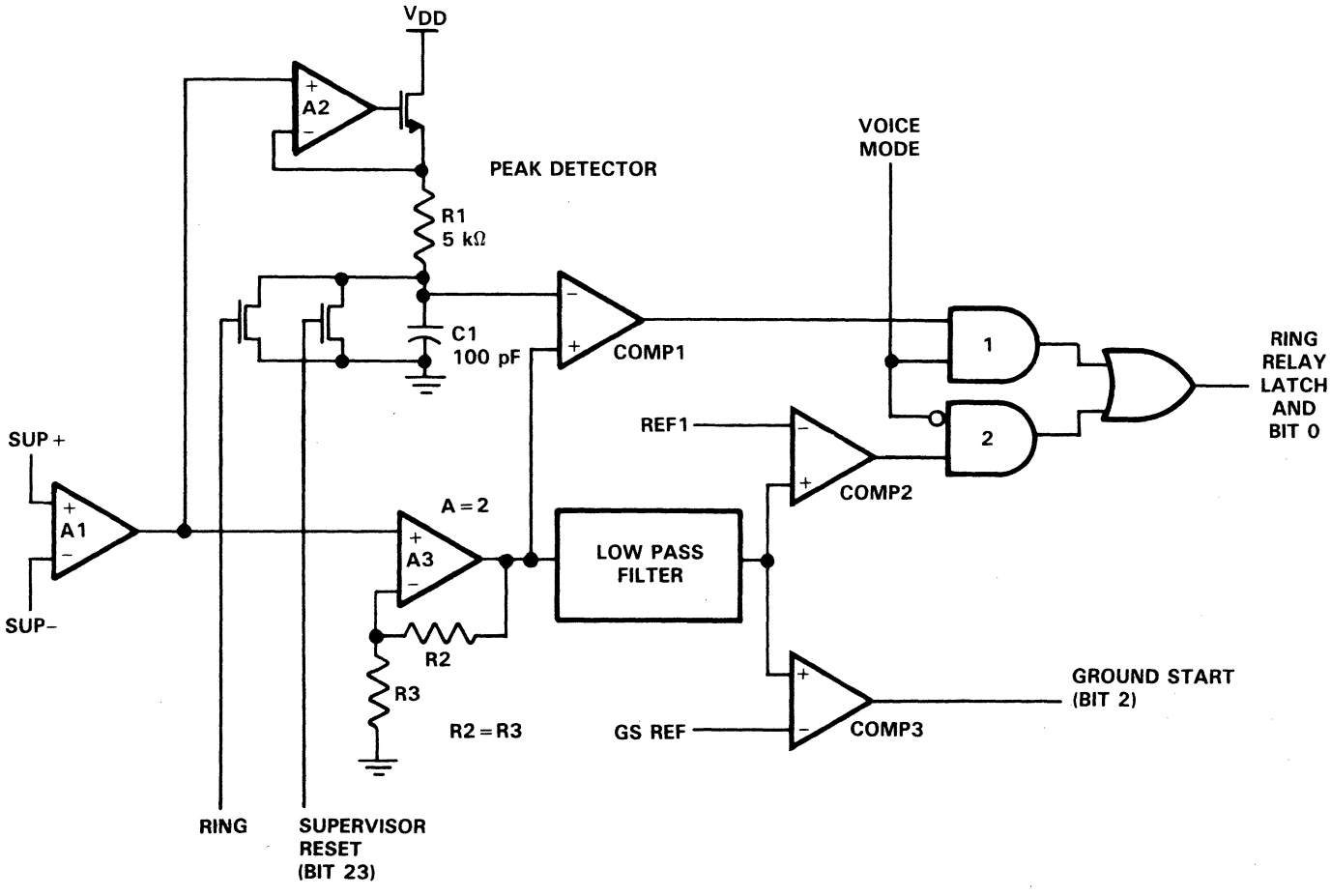


Figure 8. Supervision Circuit Block Diagram

Ring-trip is the supervisor function which involves detecting off-hook during the ringing condition and resetting the ring relay. The SLCC must be in the standby or power-down mode when the ring bit is set to allow the LPF to reject the ring signal from the supervisor information.

When the ring relay is activated, the system is reconfigured as shown in Figure 9. The off-hook dc current path has been traced to illustrate the ring-trip function. When the telephone goes off-hook in the ringing condition, the IR drop across the 400-Ω resistor causes the potential at the SUP– input to drop below that at the SUP+ input. The SLCC automatically turns off the ring relay output when the hook status bit has been set. The controller must then reset the ring bit as soon as an off-hook condition has been determined.

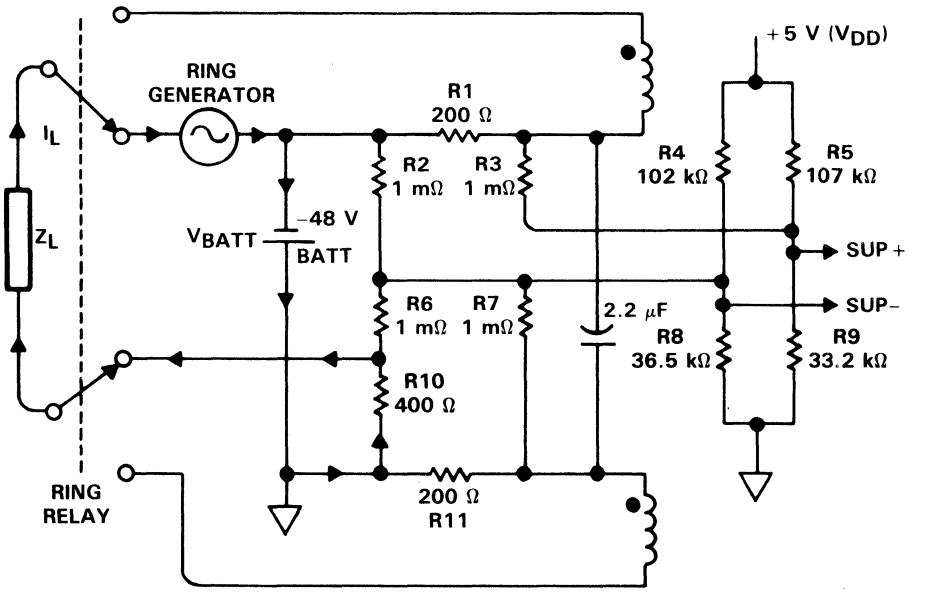


Figure 9. Off-Hook Loop Current Path During Ringing Condition

The Supervision circuit shown in detail on Figure 6 and Figure 8 was designed to the following criteria:

1. A 10-mA loop current represents off-hook.
2. A -50-mV reverse bias exists when the loop current equals 0.

The simplified loop equations are as follows:

1. Nonringing condition:

$$V_{SUP+} = [V_{DD}(1/R5) + V_{BATT}(1/R3) + I1(R1)(1/R3)]/[1/R5) + (1/R9) + (1/R3)]$$

$$V_{SUP-} = [V_{DD}(1/R4) + V_{BATT}(1/R2) - Il(R11)(1/R7)]/[(1/R2) + (1/(R6 + R10)) + (1/R8) + (1/R4) + (1/R7)]$$

2. Ringing condition:

$$V_{SUP+} = [V_{DD}(1/R5) + V_{BATT}(1/(R3 + R1))]/[(1/(R1 + R3)) + (1/R9) + (1/R5)]$$

$$V_{SUP-} = [V_{DD}(1/R4) + V_{BATT}(1/R2) - Il(R10)(1/R6)]/[(1/R2) + (1/(R7 + R11)) + (1/R6) + (1/R8) + 1/R4)]$$

Circuit values:

Derived values	Typical Values
R1 = 200 Ω	200 Ω
R2 = R	1 MΩ
R3 = R	1 MΩ
R4 = R/9.8	102 kΩ
R5 = R/9.4	107 kΩ
R6 = R	1 MΩ
R7 = R	1 MΩ
R8 = R/27.2	36.5 kΩ
R9 = R/29.6	33.2 kΩ
R10 = 400 Ω	400 Ω
R11 = 200 Ω	200 Ω
V_{DD} = 5 V	
V_{BB} = −48 V	
Typically R = 1 MΩ	

Substitution of the circuit values yields the following:

Nonringing condition:

$$V_{SUP+} = (5)I_L - 0.025 \text{ V}$$
$$V_{SUP-} = (-5)I_L + 0.025 \text{ V}$$
$$V_{SUP+} - V_{SUP-} = (10)I_L - 0.050 \text{ V}$$

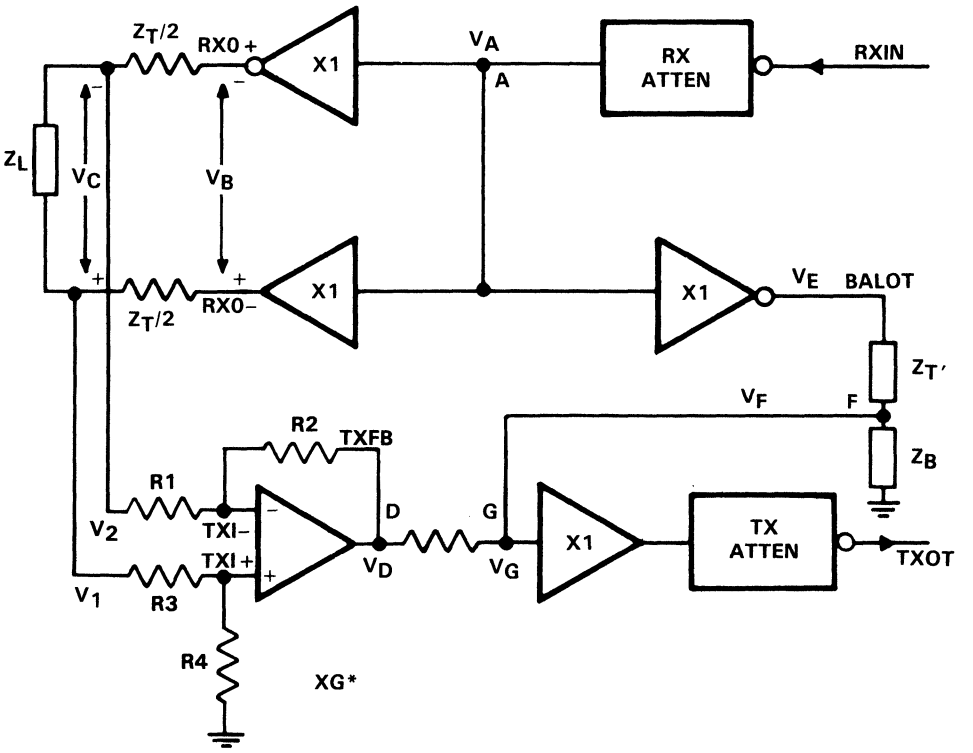
Ringing condition:

$$V_{SUP+} = -0.025 \text{ V}$$
$$V_{SUP-} = (-10)I_L + 0.025 \text{ V}$$
$$V_{SUP+} - V_{SUP-} = (10)I_L - 0.050 \text{ V}$$

NOTE: I_L is in mA

Hybrid Circuit

Figure 5 shows that any signal that is applied at the receive input (RXIN) will appear across the transmit-amplifier inputs. The hybrid prevents the received signal from being returned on the transmit output (TXOT). The SLCC performs the hybrid function with the amplifier configuration of Figure 10. With a proper balance network, the receive signals at nodes D and F will be equal in amplitude and opposite in phase, cancelling completely at node G.



*The gain of this amplifier is set by the user. If R1/R2 = R3/R4, the output is $V_O = \frac{R2}{R1}(V_1 - V_2)$, or G = R2/R1.

Figure 10. SLCC Hybrid Function Amplifier Configuration

In the illustration, the gains of all internal amplifiers are unity, except for the transmit-input amplifier, which has a gain G that is set by the user with external resistors. The impedance Z_T is the termination impedance and Z_L is the line impedance, which is reflected through the battery-feed transformer.

Analysis of the hybrid can be accomplished by assuming that a signal is applied at RXIN such that $V_A = 1$ V. By tracing the signal to the various nodes, the following voltages are obtained:

$V_A = 1$ V
differential voltage $V_B = 2$ V
differential voltage $V_C = 2[Z_L/(Z_T + Z_L)]$ V
$V_D = 2G[Z_L/(Z_T + Z_L)]$ V
$V_E = -1$ V
$V_F = -Z_B/(Z_T' + Z_B)$ V

For proper signal cancellation:

$$V_D = -V_F \text{ or}$$
$$2G[Z_L/(Z_T + Z_L)] = Z_B/(Z_T' + Z_B)$$
$$(1/2G)[Z_T/Z_L + 1] = Z_T'/Z_B + 1$$
$$1/2G[(Z_T/Z_L) + 1] = Z_T'/Z_B + 1$$

If G is set to 1/2, for proper signal cancellation:

$$Z_T/Z_L = Z_T'/Z_B$$

NOTE: If G is not equal to 1/2, proper balance cannot be obtained.

The impedances Z_T' and Z_B can be scaled versions of Z_T and Z_L. By scaling the impedances up, large resistors and small capacitors can be used in the balance networks. The impedance of the three balance networks in parallel must be greater than 10 kΩ to prevent loading the balance output (BALOT).

Flux-Cancelling Drive Circuit

In the CO or PBX, the dc loop current flows through the transformer coil. This dc current in turn produces a dc flux in the core of the transformer. As the size of the transformer decreases, its core tends to become saturated at lower flux levels. In order to use the smaller transformers required to conserve space, a means of preventing core saturation is necessary.

Many transformers now have a flux-cancelling winding. This extra winding provides a means of generating a dc core-flux to oppose that created by the local loop. Normally, the CO-side to subscriber-side turns ratio is 1:1. If the CO or subscriber-side has n turns, the flux-cancelling winding usually has 3 n to 5 n turns. By forcing a current through the flux-cancelling winding that is 1/3 (for 3 n turns) to 1/5 (for 5 n turns) of the loop current, the dc core-flux is kept at 0, even for large loop currents. Using the standard dot convention, if the loop current flows into the dot on the subscriber side, the flux-cancelling current must flow out of the dot in the flux-cancelling winding.

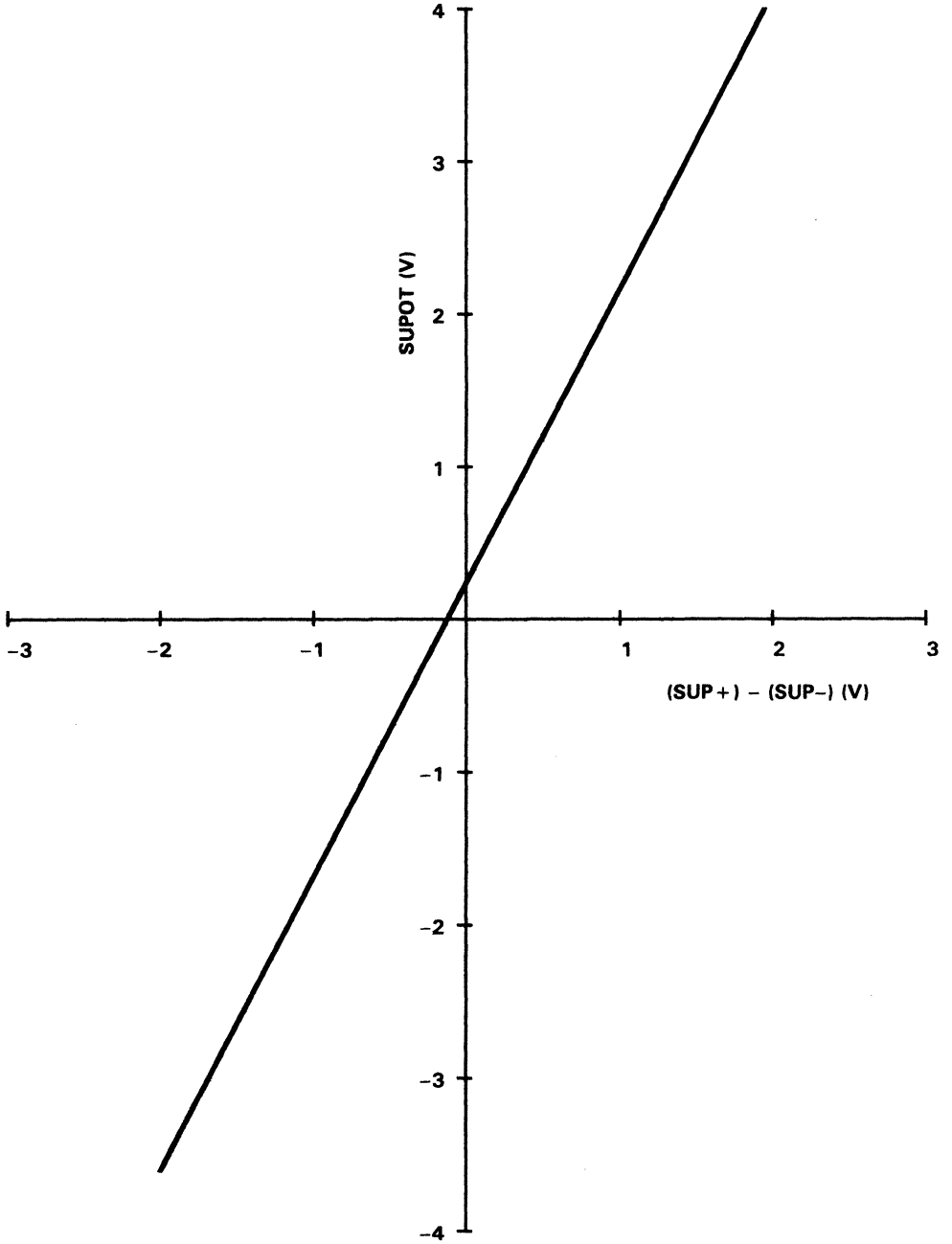


Figure 11. SUPOT as a Function of Supervision Input

Driving the flux-cancelling winding of the transformer requires a high impedance current source. This fact is indicated by the impedance transformation across the transformer. If a transformer has a flux-cancelling to subscriber-side turns ratio of n:1, the flux-cancelling drive circuit impedance is reflected to the CO side as 1/n its actual value. For a turns ratio of 5:1, which is a typical value, the impedance is reflected as 1/25th of its value. Unless the impedance of the drive circuit is high, it will load the output from the CO.

Figure 11 is a plot of SUPOT versus differential supervision input-voltage, (SUP+) -(SUP-). SUPOT is a high impedance output that provides a voltage twice that of the differential input. From Figures 7 and 11, a plot of SUPOT versus loop current is obtained (see Figure 12).

The linear relationship between SUPOT and loop current allows the use of a voltage-controlled current source as the flux-cancelling winding drive circuit. Figure 13 is one possible example. The voltage at node A is the negative of SUPOT. Proper choice of R1 provides the correct flux-cancelling current. Since the voltage at node A exactly follows SUPOT, this circuit offers a very high impedance to the transformer.

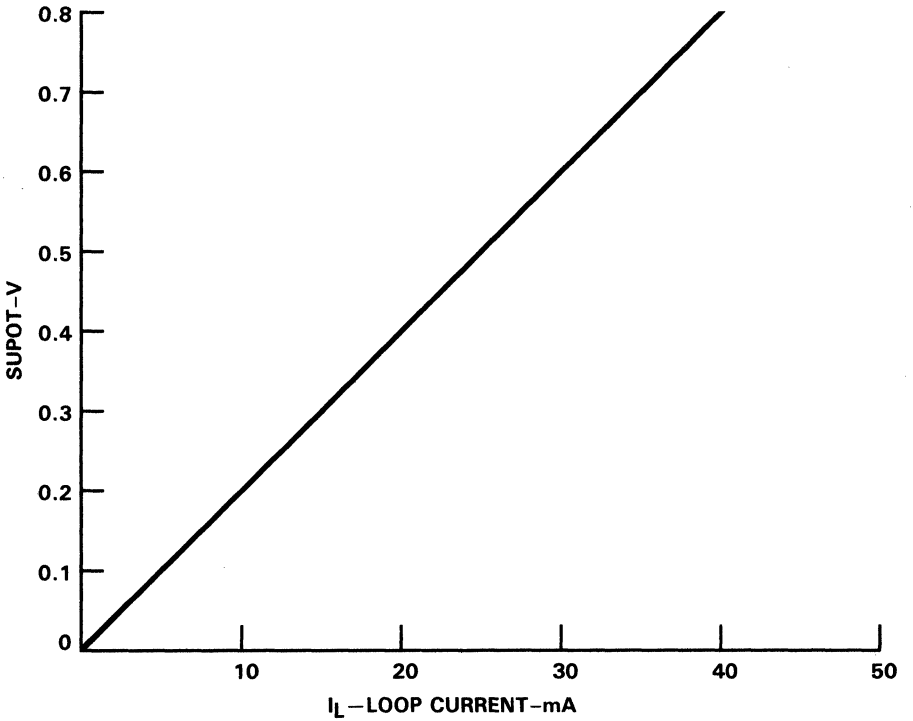


Figure 12. SUPOT as a Function of Loop Current

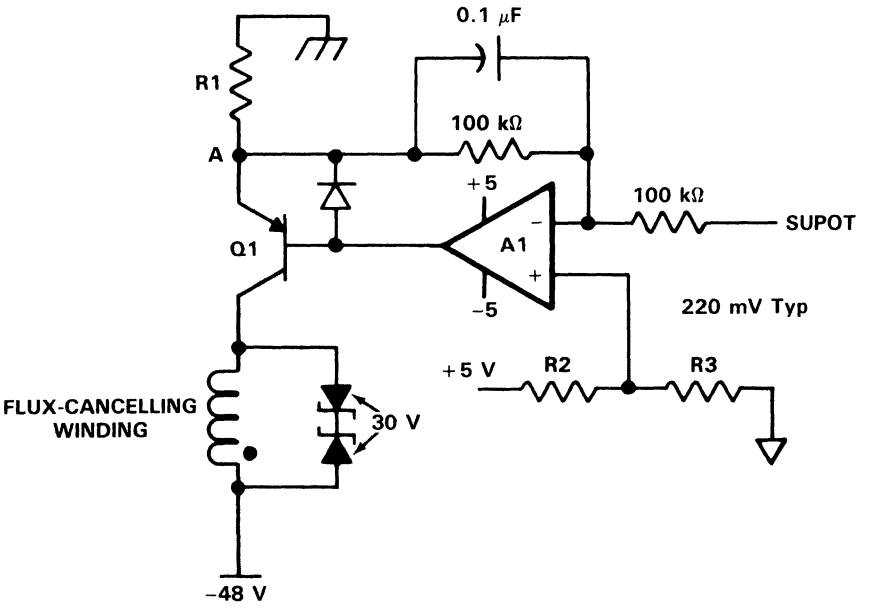


Figure 13. High-Impedance Drive Circuit for a Flux-Cancelling Winding

Increasing the gain of the op-amp circuit and adjusting R1 accordingly minimizes the dissipation of power in Q1. The upper limit on R1 is determined by the maximum current that must be provided, plus the dc resistance of the winding. At maximum current, Q1 must remain out of saturation; that is, $V_{CE} > V_{CE(sat)}$.

A design example is a flux-cancelling to subscriber-to-CO turns ratio of 5:1:1. From Figure 12, notice that at 0 mA loop current SUPOT is 0 V, and at 20 mA loop current SUPOT is 0.4 V. These points give a slope of (0.4 - 0)/(0.02 -0) = 20. Since only one fifth the loop current is required, R1 is chosen as 20 × 5 = 100. The power dissipated in Q1 is the following:

$$P_{diss} = I_C \times V_{CE}$$
$$= I_C[48 - I_C(R1 + RW)]$$
$$= I_C[48 - RT \times I_C]; \; RT = R1 + RW$$

where RW is the dc resistance of the winding. The maximum power dissipation occurs where the first derivative is 0:

$$dP_{diss}/dI_C = 48 - 2RT \times I_C = 0$$
$$I_C = 24/RT$$

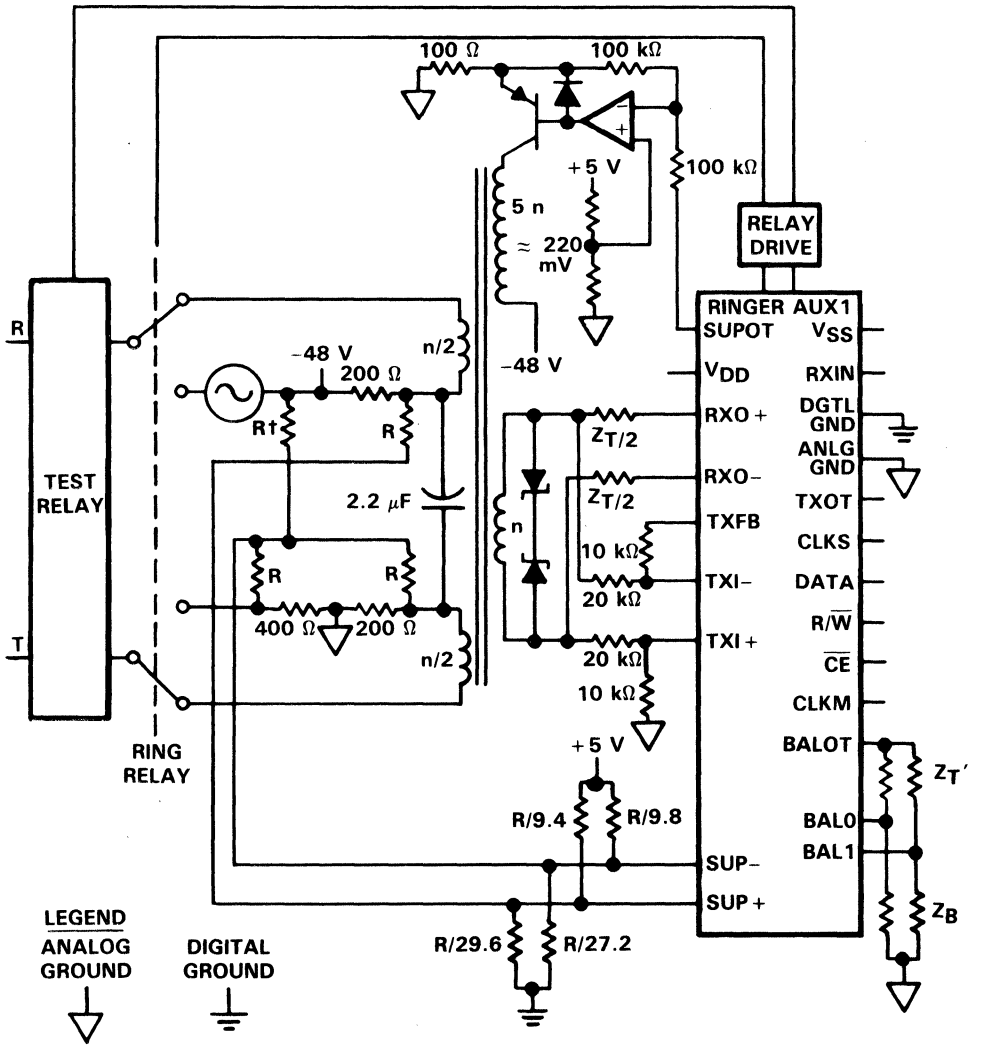
Substituting this value into the power equation gives

$$P_{diss}(max) = (24/RT)[48 - RT(24/RT)]$$
$$= 24/RT$$
$$= 576/RT.$$

The collector-to-emitter breakdown voltage of Q1 must be considered. This transistor must tolerate a V_{CEO} of 48 V, and one possible component for this position is the 2N2905A.

The operational amplifier A1 in the diagram can be any inexpensive circuit that will operate from +5 V to -5 V, such as the MC1458 dual op-amp.

Figure 14 shows a TCM4207A application with the flux-cancelling drive circuit.



†Typically, R = 1 mΩ

Figure 14. TCM4207A SLCC Standard Subscriber Line

Conclusion

The Subscriber Line Control Circuits from Texas Instruments offer all low-voltage line-card functions on a single CMOS IC. This solution provides high performance while using less board space than conventional solutions. The low power consumption (typically 75 mW) of the SLCC also gives it improved reliability over other solutions. For further specifications of the TCM4204A series, refer to the data sheet elsewhere in this book.

Contents

	Page
Ordering Instructions	5-3
Mechanical Data	5-5

Electrical characteristics presented in this data book, unless otherwise noted, apply for the circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-correction diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this data book should include a four-part type number as explained in the following example.

EXAMPLE: TCM 2222 J -00

Prefix

MUST CONTAIN THREE OR FOUR LETTERS

TCM . . . . . TI Telecommunication Products
TIL . . . . . TI Optoelectronics Products
TISP . . . . . TI Transient Voltage Suppressors
TLC . . . . . TI Linear Silicon-Gate CMOS Products

Unique Circuit Description

MUST CONTAIN THREE TO EIGHT CHARACTERS
(From Individual Data Sheets)

Examples: 181 32041C
2222 29C13N-3
3180

Package

MUST CONTAIN ONE OR TWO LETTERS

D, DW, DY, FN, HA, HB, J, JT, JW, KC, N, NT, NW, P
(From Pin-Connection Diagrams on Individual Data Sheet)

Instructions (Dash No.)

MUST CONTAIN TWO NUMBERS

-00 No special Instructions
-10 Solder-dipped leads (N and NT packages only)

Circuits are shipped in one of the carriers below. Unless a specific method of shipment is specified by the customer (with possible additional costs), circuits will be shipped on the most practical carrier.

(D,DW,DY,J,JT,JW,N,NT,NW,P)
—Slide Magazines
—A-Channel Plastic Tubing
—Barnes Carrier
—Sectioned Cardboard Box
—Individual Cardboard Box

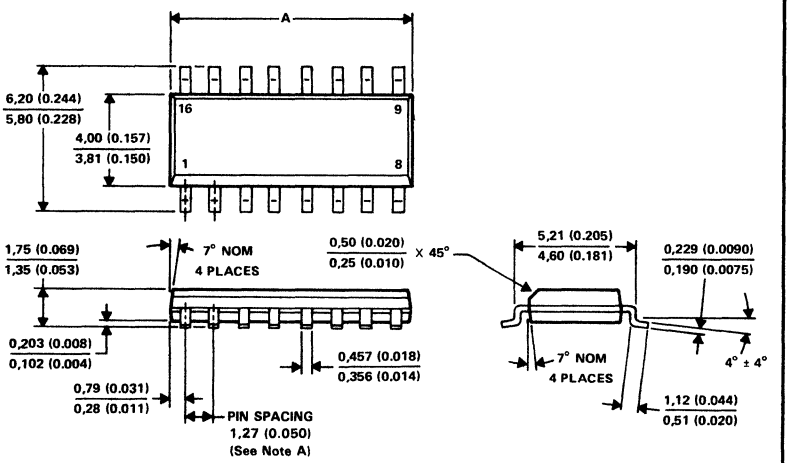
Chip Carriers (FN)
—Anti-Static Plastic Tubing
Flat (HA, HB)
—Wells Carrier

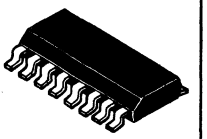
Power Tab (KC)
—Sleeves

D008, D014, and D016 plastic "small outline" packages

Each of these "small outline" packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

D008, D014, and D016
(16-pin package used for illustration)





DIM \ PINS	8	14	16
A MIN	4,80 (0.189)	8,55 (0.337)	9,80 (0.386)
A MAX	5,00 (0.197)	8,74 (0.344)	10,00 (0.394)

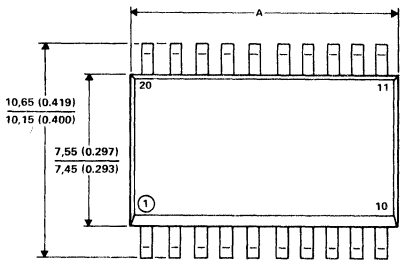
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

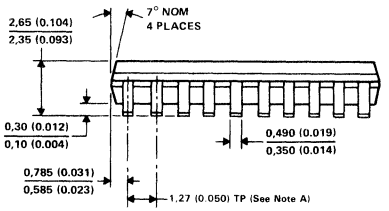
NOTES: A. Leads are within 0,25 (0.010) radius of true position at maximum material dimension.
B. Body dimensions do not include mold flash or protrusion.
C. Mold flash or protrusion shall not exceed 0,15 (0.006).
D. Lead tips to be planar within ±0,051 (0.002) exclusive of solder.

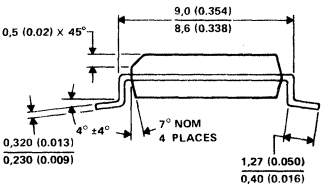
DW016, DW020, DW024, and DW028 plastic "small outline" packages

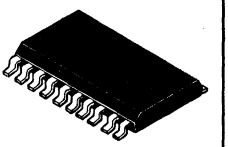
Each of these "small outline" packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

DW016, DW020, DW024, and DW028
(20-pin package used for illustration)









DIM \ PINS	16	20	24	28†
A MIN	10,16 (0.400)	12,70 (0.500)	15,29 (0.602)	17,68 (0.696)
A MAX	10,36 (0.408)	12,90 (0.508)	15,49 (0.610)	17,88 (0.704)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

†The 28-pin package drawing is presently classified as Advance Information.

NOTES: A. Leads are within 0,25 (0.010) radius of true position at maximum material dimension.
B. Body dimensions do not include mold flash or protrusion.
C. Mold flash or protrusion shall not exceed 0,15 (0.006).
D. Lead tips to be planar within ±0,051 (0.002) exclusive of solder.

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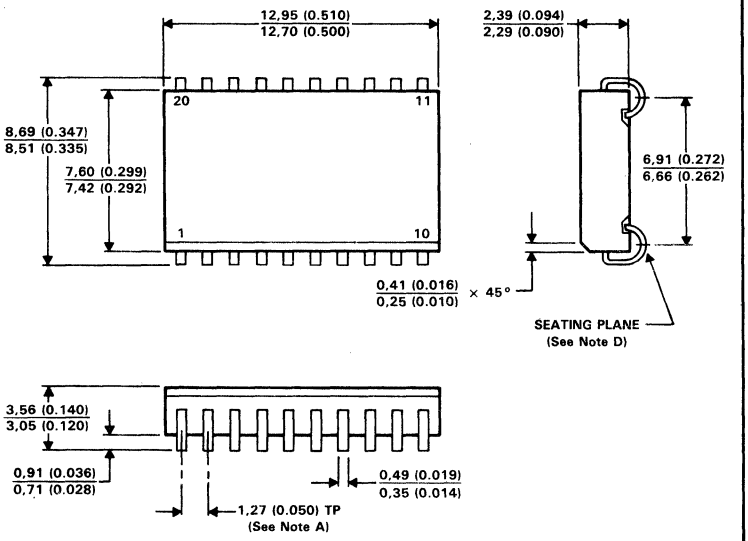
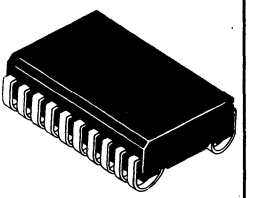
DY020 plastic "small outline" package

This "small outline" package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

DY020





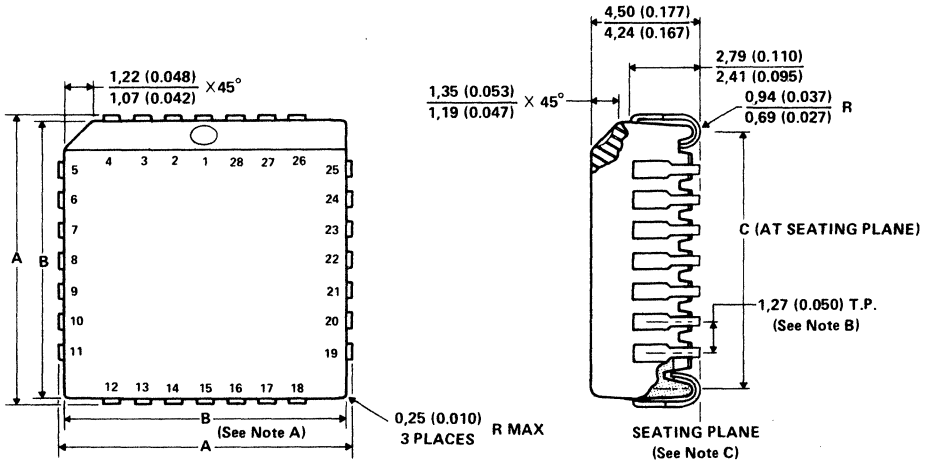
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Leads are within 0,25 (0.010) radius of true position at maximum material dimension.
B. Body dimensions do not include mold flash or protrusion.
C. Mold flash or protrusion shall not exceed 0,15 (0.006).
D. Formed leads to be planar within 0,10 (0.004) exclusive of solder.

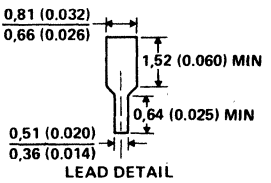
FN020, FN028, FN044, FN068, and FN084 plastic chip carrier packages

Each of these chip carrier packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound withstands soldering temperatures with no deformation, and circuit performance characteristics remain stable when the devices are operated in high-humidity conditions. The packages are intended for surface mounting on solder lands on 1,27 (0.050) centers. Leads require no additional cleaning or processing when used in soldered assembly.

FN020, FN028, FN044, FN068, and FN084
(28-terminal package used for illustration)



JEDEC OUTLINE	NO. OF TERMINALS	A MIN	A MAX	B MIN	B MAX	C MIN	C MAX
MO-047AA	20	9,78 (0.385)	10,03 (0.395)	8,89 (0.350)	9,04 (0.356)	7,87 (0.310)	8,38 (0.330)
MO-047AB	28	12,32 (0.485)	12,57 (0.495)	11,43 (0.450)	11,58 (0.456)	10,41 (0.410)	10,92 (0.430)
MO-047AC	44	17,40 (0.685)	17,65 (0.695)	16,51 (0.650)	16,66 (0.656)	15,49 (0.610)	16,00 (0.630)
MO-047AE	68	25,02 (0.985)	25,27 (0.995)	24,13 (0.950)	24,33 (0.956)	23,11 (0.910)	23,62 (0.930)
MO-047AF	84	30,10 (1.185)	30,35 (1.195)	29,21 (1.150)	29,41 (1.158)	27,69 (1.090)	28,70 (1.130)



All dimensions and notes for the specified JEDEC outline apply.

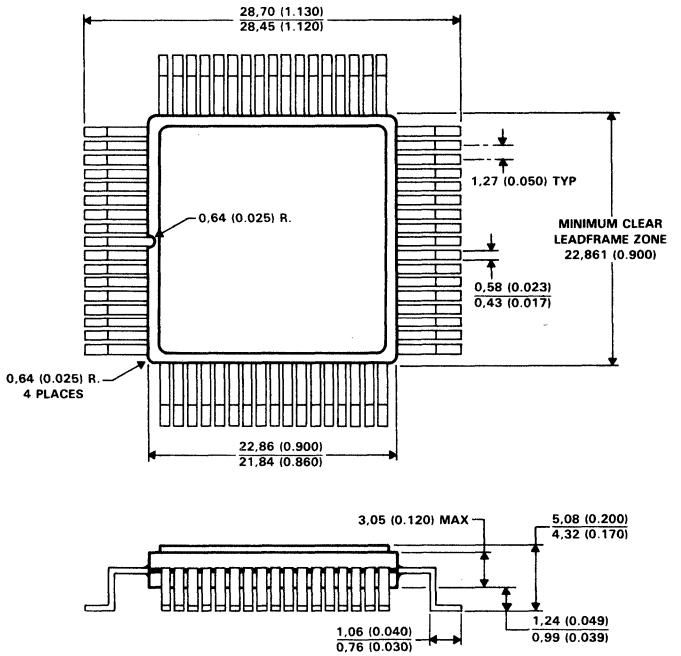
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Centerline of center pin each side is within 0,10 (0.004) of package centerline as determined by dimension B.
B. Location of each pin is within 0,127 (0.005) of true position with respect to center pin on each side.
C. The lead contact points are planar within 0,10 (0.004).

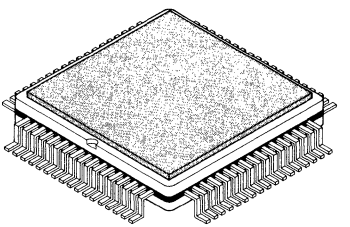
HA068 quadriform flat package

The 68-pin HA package is housed in a quadriform flat package. It is hermetically sealed with 0.05-inch-lead spacing configured with gull-wing bent leads for surface mounting capability.

HA068



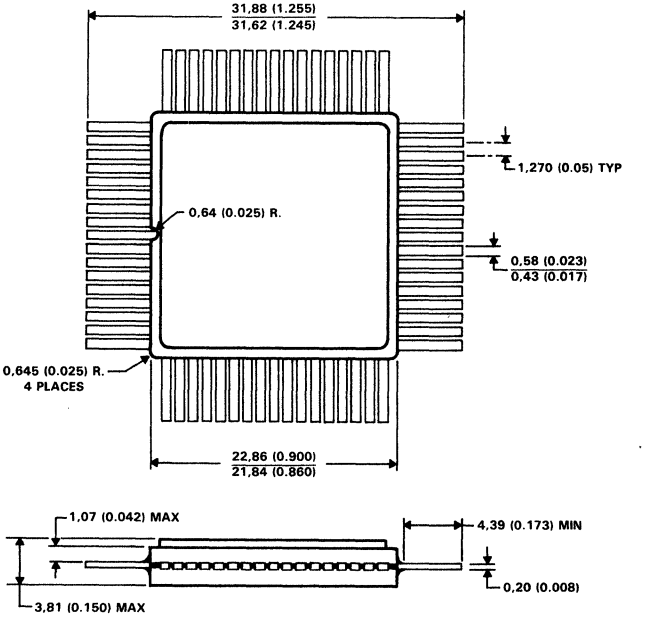
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES



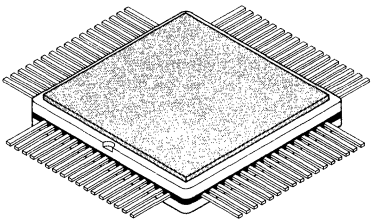
HB068 quadriform flat package

The 68-pin HB package is housed in a quadriform flat package. It is hermetically sealed with 0.05-inch-lead spacing configured with straight leads for surface mounting capability.

HB068



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES



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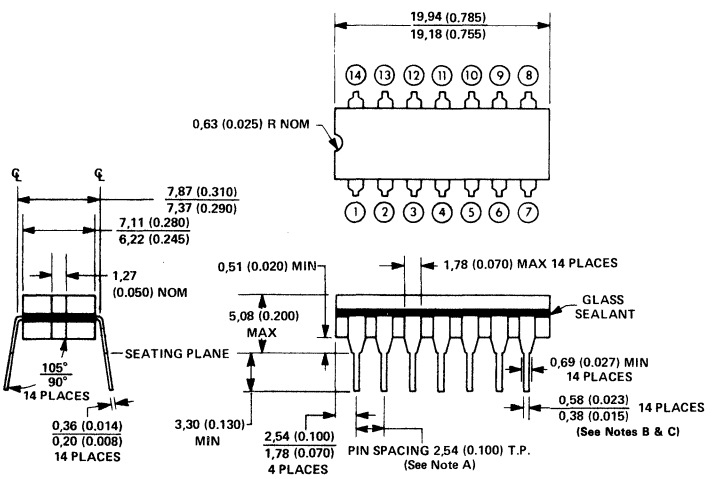
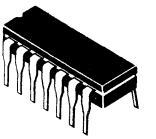
J014 ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.

J014





Falls Within JEDEC TO-116 and EIA MO-001AA Dimensions

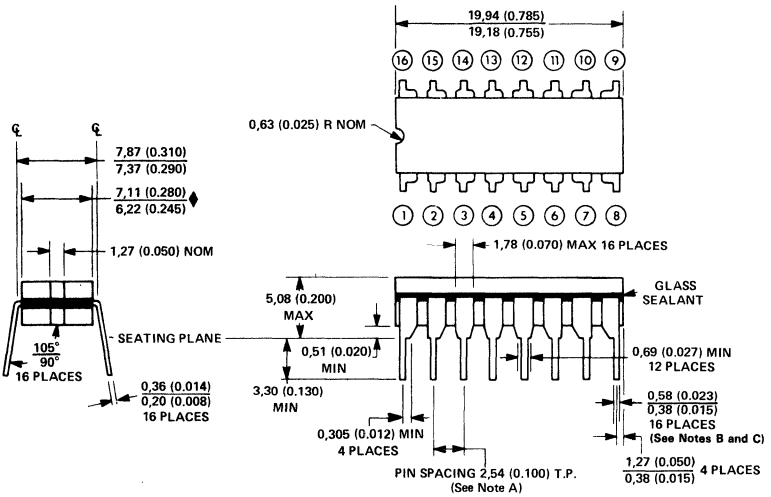
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

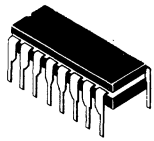
NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above the seating plane.

J016 ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated (''bright-dipped'') leads require no additional cleaning or processing when used in soldered assembly.

J016





♦ For memories of 64 bits and up, a few MSI/LSI products in Series 54/74 and Series 54S/74S that are derived from memory circuit bars, and complex HCMOS parts, this maximum is 7,62 (0.300). All other dimensions apply without modification.

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above the seating plane.

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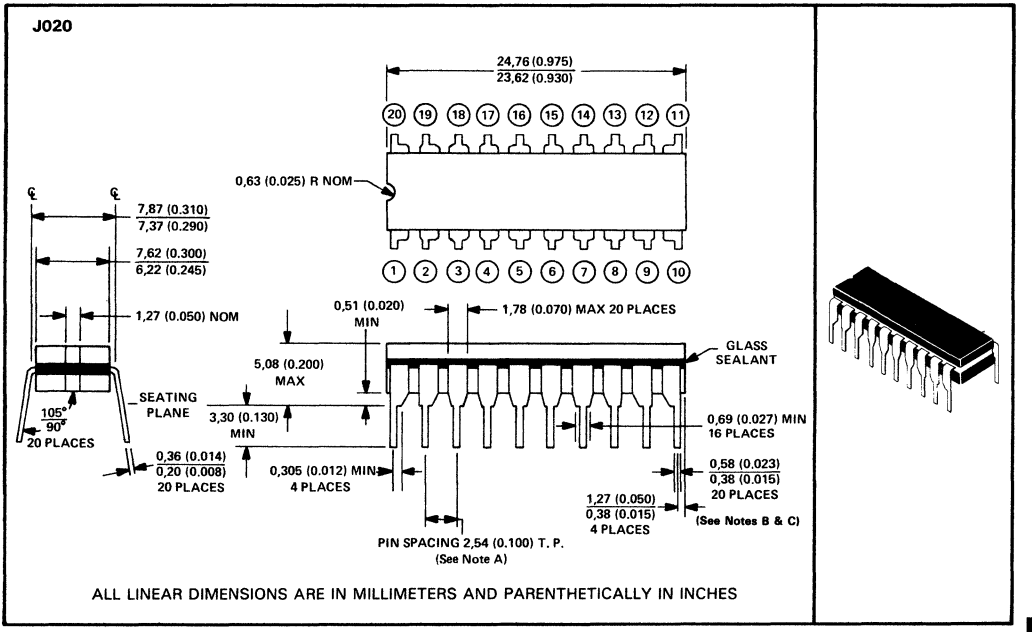
J020 ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated (''bright-dipped'') leads require no additional cleaning or processing when used in soldered assembly.

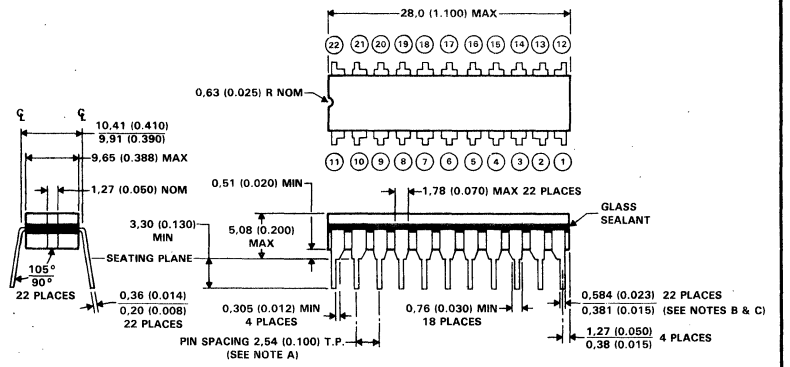


NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above the seating plane.

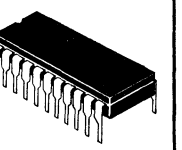
J022 ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows 10,16 (0.400) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.

J022



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

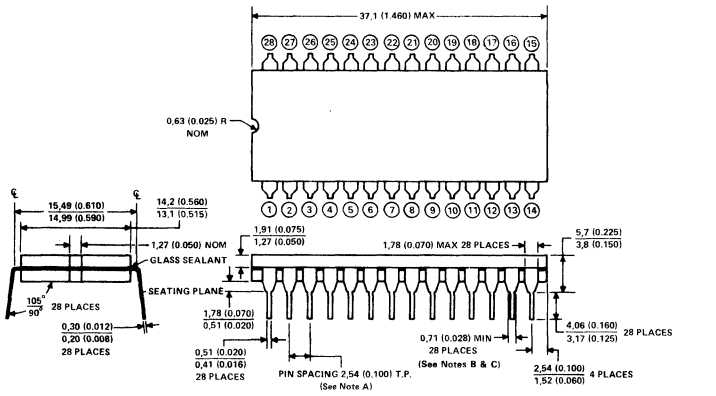


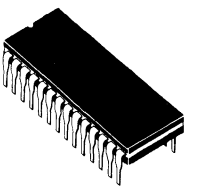
NOTES: A. Each pin centerline is located within 0,25 (0.10) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above the seating plane.

J028 ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 15,24 (0.600) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated (''bright-dipped'') leads require no additional cleaning or processing when used in soldered assembly.

J028





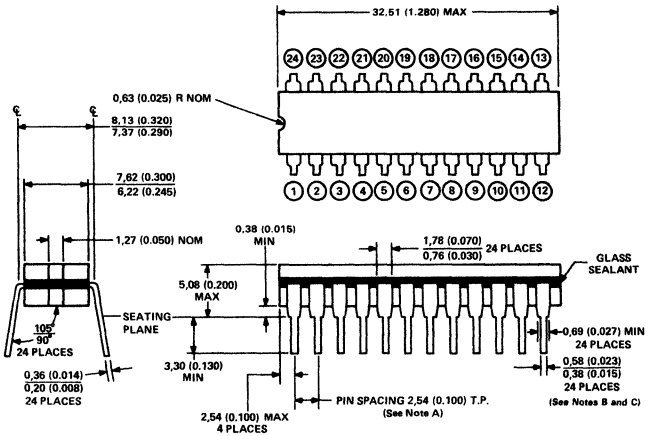
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

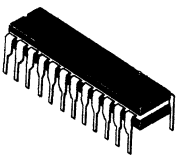
NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above the seating plane.

JT024 ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.

JT024





ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above the seating plane.

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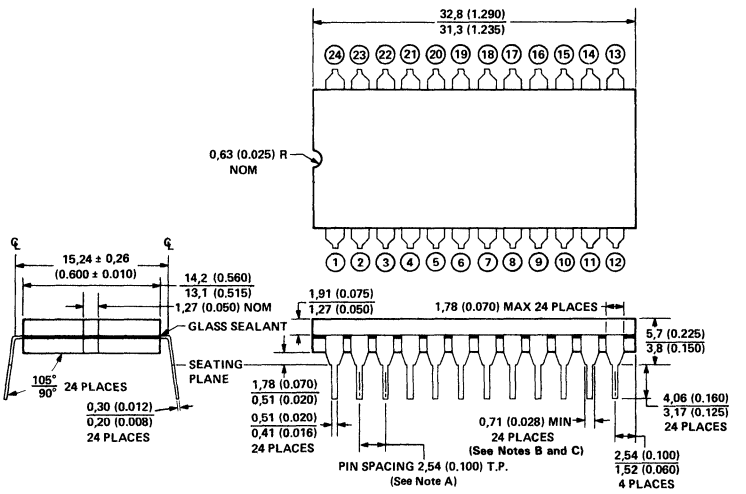
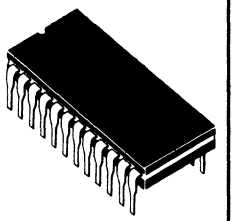
JW024 ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 15,24 (0.600) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or procesing when used in soldered assembly.

JW024





Falls Within JEDEC MO-015AA Dimensions

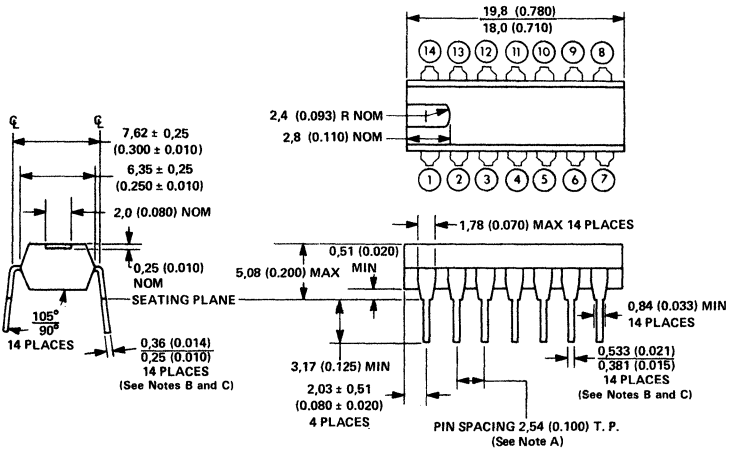
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

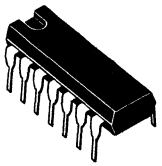
NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above the seating plane.

N014 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The packages are intended for insertion in mounting-hole rows on 7,62 (0.300) centers (see Note A). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

N014





Falls Within JEDEC TO-116 and EIA MO-001AA Dimensions

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above the seating plane.

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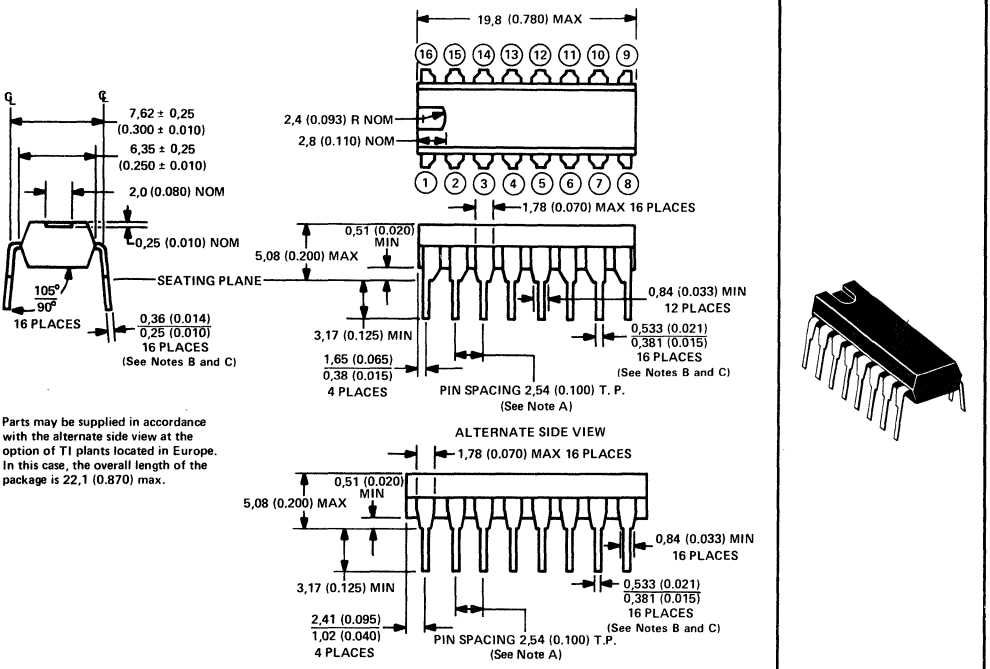
N016 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

N016



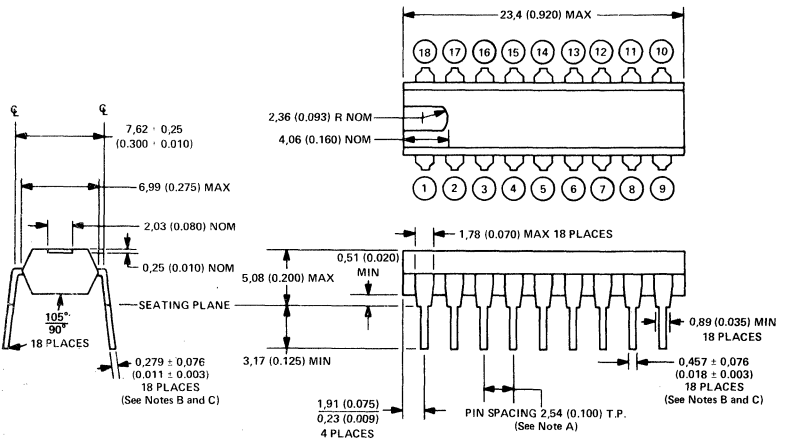
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

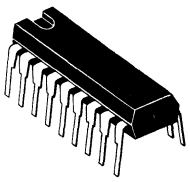
N018 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

N018



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES



NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

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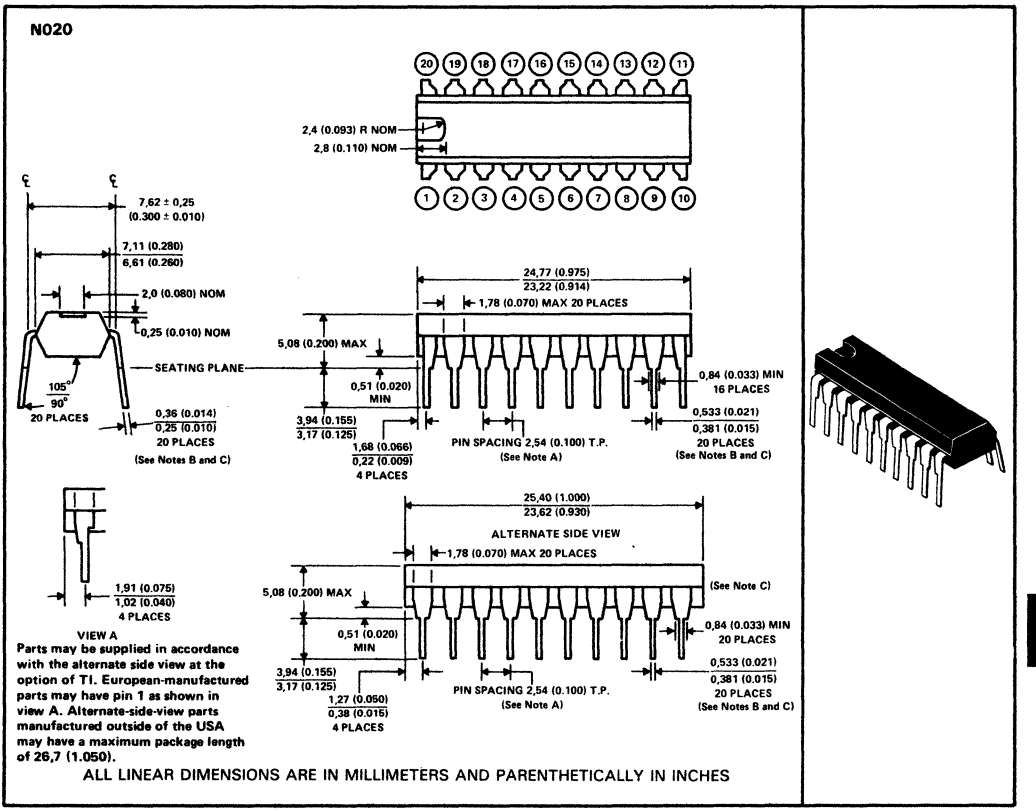
N020 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.



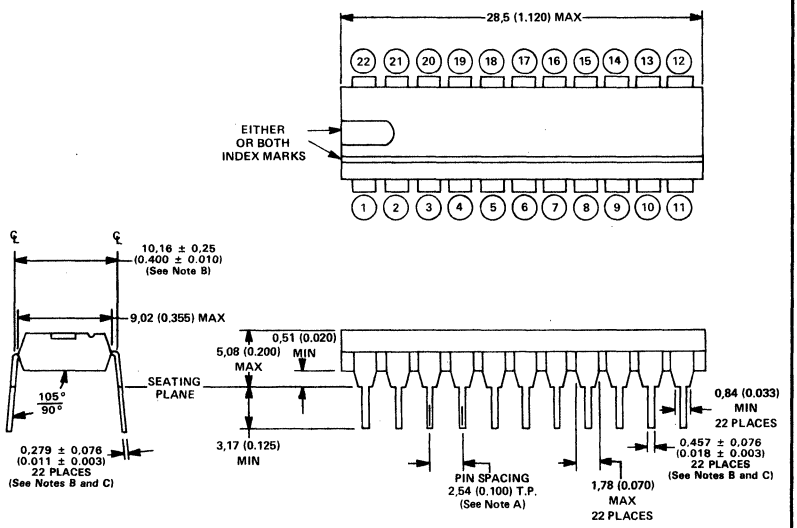
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

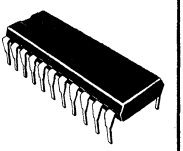
NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

N022 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 10,16 (0.400) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

N022





ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

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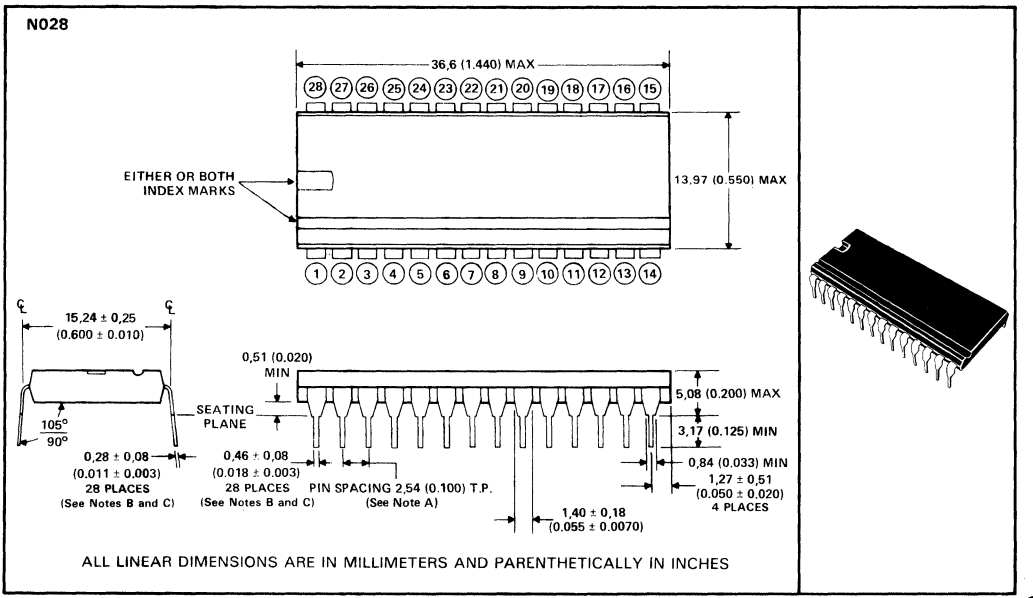
N028 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 15,24 (0.600) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.



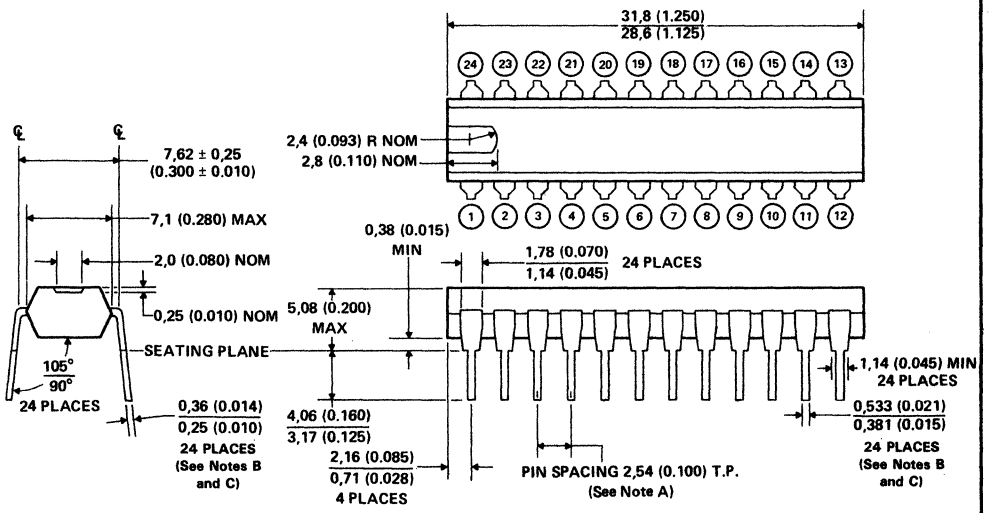
NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

NT024 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

NOTE: For all except 24-pin packages, the letter N is used by itself since only the 24-pin package is available in more than one row-spacing. For the 24-pin package, the 7,62 (0.300) version is designated NT; the 15,24 (0.600) version is designated NW. If no second letter or row-spacing is specified, the package is assumed to have 15,24 (0.600) row-spacing.

NT024



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

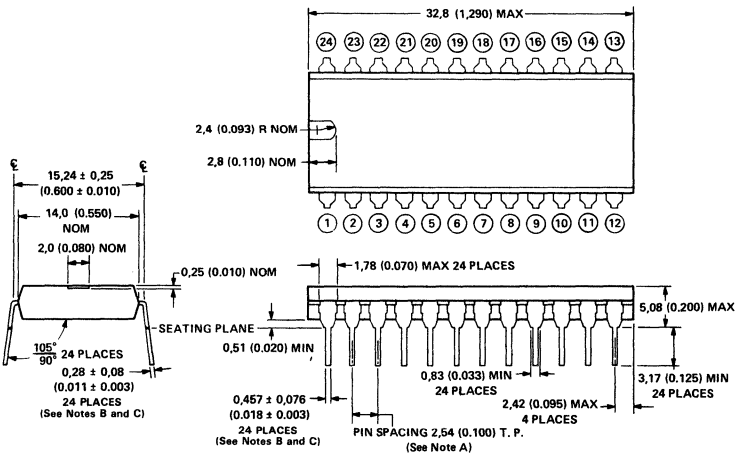
NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above the seating plane.

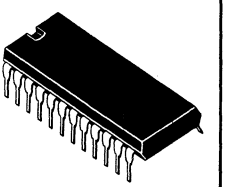
NW024 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 15,24 (0.600) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

NOTE: For all except 24-pin packages, the letter N is used by itself since only the 24-pin package is available in more than one row-spacing. For the 24-pin package, the 7,62 (0.300) version is designated NT; the 15,24 (0.600) version is designated NW. If no second letter or row-spacing is specified, the package is assumed to have 15,24 (0.600) row-spacing.

NW024





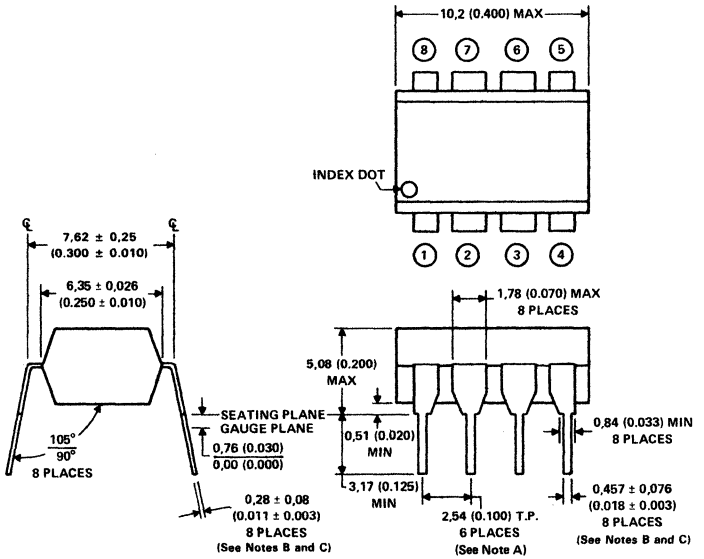
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

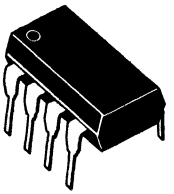
NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

P008 dual-in-line plastic package

This package consists of a circuit mounted on an 8-pin lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers (See Note A). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Solder-plated leads require no additional cleaning or processing when used in soldered assembly.

P008





ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

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